## **Chapter 6**

# **Further Exploration of Graphene/Semiconductor Interfaces**

### **6.1 Introduction and Background**

Unlike the preceding chapters, which were presented in journal-like format insomuch as they covered a single topic, were composed of published data, and contained a single experimental description, this chapter is instead a collection of vignettes on topics that I explored but was unable to publish on prior to the completion of my doctoral degree. With this in mind, the sections that follow in this chapter are self-contained to the extent that it was reasonable to do so, including short, independent introduction, experimental, and discussion sections for each. Included topics in this chapter are:

- The effect of bilayer and trilayer graphene as protective layers for silicon surface protection
- The use of pristine monolayer graphene to prevent silicide formation
- The use of a home-built CVD to grow monolayer graphene
- The effect of different etch methods on the identity and concentration of impurities at the graphene/silicon interface
- The deposition of metal oxides on graphene surfaces using atomic layer deposition methods

# 6.2 Bilayer and trilayer graphene as protective layers for silicon surfaces

In chapter 4, pristine monolayer graphene is used as a protective coating to prevent the passivation of silicon surfaces in aqueous photoanodic conditions. However, this protective ability is clearly incomplete as noted by the lack of perfect stabilization over longer time periods as well as under high light intensity (~1 sun) conditions. We hypothesized that the reason for this imperfect stability is the polycrystalline nature of the CVD grown graphene as well as damage to the graphene coatings during transfer onto the silicon surface. For this reason, we proposed that a second or third layer of graphene transferred to the surface should make graphene more likely to cover any damaged or damage-prone sites on the graphene sheets below it and therefore translate to better stability. In order to test this hypothesis, we repeated the procedures described in chapter 4 with the modification that multiple sheets of graphene were transferred to the silicon electrodes prior to photoelectrochemical testing in aqueous electrolyte. The J-t behavior of mono-, bi-, and trilayer graphene under  $\sim$ 33 mW cm<sup>-2</sup> illumination from an ENH bulb in aqueous 350 mM Fe(CN) $_{6}^{4-}$  - 50 mM Fe(CN) $_{6}^{3-}$  electrolyte is depicted in figures 6.1ac.



**Figure 6.1a.** J-t behavior of monolayer graphene-covered n-Si electrode in aqueous 350 mM  $\text{Fe}(\text{CN})_6^{4-}$  – 50 mM  $\text{Fe}(\text{CN})_6^{3-}$  electrolyte under ~33 mW cm<sup>-2</sup> illumination from an ENH bulb. The loss of photocurrent over 75,000 s is suggestive of passivation of the silicon surface.



**Figure 6.1b.** J-t behavior of bilayer graphene-covered n-Si electrode in aqueous 350 mM  $Fe(CN)_6^{4-} - 50 \text{ mM } Fe(CN)_6^{3-}$  electrolyte under ~33 mW cm<sup>-2</sup> illumination from an ENH bulb. The stable photocurrent over 75,000 s is suggestive of a stable silicon surface.



**Figure 6.1c** J-t behavior of trilayer graphene-covered n-Si electrode in aqueous 350 mM  $Fe(CN)_6^{4-} - 50 \text{ mM } Fe(CN)_6^{3-}$  electrolyte under ~33 mW cm<sup>-2</sup> illumination from an ENH bulb. The stable photocurrent over 75,000 s is suggestive of a stable silicon surface.

From the data in figures 6.1a-c, it appears that additional layers of graphene led to improved stability of the photocurrent when compared to monolayer graphene-covered silicon photoanodes. Additionally, the J-E behavior of trilayer graphene-covered np<sup>+</sup>Si photoelectrodes was explored (figure 6.2).



**Figure 6.2.** J-E behavior of a trilayer graphene-covered np<sup>+</sup>Si photoelectrode in aqueous  $350 \text{ mM Fe}(\text{CN})_6^{4-} - 50 \text{ mM Fe}(\text{CN})_6^{3-}$  electrolyte under ~1 sun illumination from an ENH bulb over 2 potential sweeps at 30 mV s<sup>-1</sup>.

The data in figure 6.2 shows that the trilayer graphene imparts stability to graphenecovered Si photoanodes even under higher light intensity conditions and at higher current densities than those depicted in figure 6.1. The  $E_{oc}$  was consistent with bare np<sup>+</sup>Si  $E_{oc}$ values and the fill factor was consistent with the fill factors for other graphene-covered silicon surfaces in aqueous 350 mM Fe(CN)<sub>6</sub><sup>4-</sup> – 50 mM Fe(CN)<sub>6</sub><sup>3-</sup> electrolyte.

These results are promising in suggesting that additional layers of graphene are useful in improving stability, but there are a number of questions that remain. While these results are interesting, I found it difficult to consistently reproduce these results. This may be because of weak adhesion between the graphene layers or because the additional transfer steps introduce additional damage to the graphene surface. Using as-grown multilayer graphene sheets to measure the protective ability of multiple layers of graphene would be a valuable experiment. Also, testing the stability of very small electrode areas would also be interesting insomuch as very small electrodes (<1 mm<sup>2</sup>) would be less likely to include damaged or reaction-prone graphene sections that are the hypothesized 'weak points' in the protection scheme. Further, successfully obtaining consistent bilayer and trilayer graphene-covered silicon photoelectrodes would allow the examination of the energetics and electronics of the silicon/graphene interface.

#### 6.3 Monolayer graphene to prevent silicide formation

In chapter 5, the ability to prevent the formation of platinum silicide during evaporation of platinum onto silicon surfaces was demonstrated with fluorinated graphene. Prior to this demonstration, similar experiments were undertaken using pristine monolayer graphene at the Pt/Si interface. Approximately 20 nm of Pt was deposited on monolayer graphene-covered n-Si and also on freshly HF etched n-Si. Each sample was loaded into a UHV chamber analyzed via XPS. Then, each sample treated with bombardment from an argon ion source. Using this sputtering method, a thin (~0.5 nm) section of the surface layer was removed, and the freshly exposed surface was analyzed via XPS. The hypothesis was that if graphene prevents silicide formation, depth profiling would indicate an abrupt junction and the absence of platinum silicide (PtSi) between the Pt and Si in the graphene-covered sample, but would indicate the presence of PtSi at the graphene-free junction. The results of this experiment are shown in in figures 6.3 and 6.4.



**Figure 6.3** (bottom left) XP depth profiling spectrum of the Pt 4f region of an Pt/Si interface fabricated by Pt evaporation. The large peaks at 71 and 74 eV are indicative of a pure Pt species. The 71 eV and 74 eV peaks are the peaks early in the depth profiling and as the depth profile moves deeper into the sample, the Pt 4f doublet at 72 and 76 eV appears. Peaks at 72 and 76 eV are suggestive of a platinum silicide (PtSi).<sup>1</sup> (bottom right) XP depth profiling spectrum of the Pt 4f region of an Pt/Gr/Si interface fabricated by Pt evaporation. The large peaks at 71 and 74 eV are indicative of a pure Pt species. The 71 eV and 74 eV peaks are the peaks early in the depth profiling and as the depth profiling spectrum of the Pt 4f region of an Pt/Gr/Si interface fabricated by Pt evaporation. The large peaks at 71 and 74 eV are indicative of a pure Pt species. The 71 eV and 74 eV peaks are the peaks early in the depth profiling and as the depth profile moves deeper into the sample, the Pt 4f doublet at 72 and 76 eV appears. The PtSi peaks in this spectrum are smaller in ratio to the original Pt 4f doublet than the equivalent ratio in the graphene-free interface.



**Figure 6.4.** (bottom left) Representative Pt 4f XP spectra from the Pt/Si depth profiling experiment depicted in figure 6.3. The spectrum with large double at 71 and 74 eV is the pure Pt 4f phase after the initial sputtering step. The spectrum with the doublet at 72 and 76 eV is the PtSi phase at the point with the largest PtSi peak area. It is noted that there is no pure Pt phase in this spectrum, consistent with the formation of a pure silicide phase. (bottom right) Representative Pt 4f XP spectra from the Pt/Gr/Si depth profiling experiment depicted in figure 6.3. The spectrum with large double at 71 and 74 eV is the pure Pt 4f phase after the initial sputtering step. The spectrum with large double at 71 and 74 eV is the pure Pt 4f phase after the initial sputtering step. The spectrum with the doublet at 72 and 76 eV is the PtSi phase at the point with the largest PtSi peak area. At no point during depth profiling was a surface that had PtSi but no Pt phase present.

From the data in figures 6.3 and 6.4, it appears that graphene does prevent silicide formation to a certain extent based on the low ratio of PtSi to Pt peak area at the Pt/Gr/Si interface with respect to the PtSi to Pt peak area ratio in the graphene-free Pt/Si interface. It is not clear, however, whether it is capable of entirely preventing silicide formation as the XPS at the Pt/Gr/Si interface still indicates the presence of PtSi. The presence of the PtSi signal in the XP spectrum may also be the result of the high energy Ar<sup>+</sup> ions forcing Pt atoms past the graphene layer and forming PtSi via a knock-on effect of sputtering. In order to probe this possibility, the experimental procedure was modified. Instead of depositing 20 nm of Pt via evaporation, only ~3 nm of Pt was deposited. Because the sensitivity depth of the XPS instrument is approximately 8 nm, using a thin Pt layer allowed us to probe the Pt/Si and Pt/Gr/Si interface without need for depth profiling via sputtering. The experimental procedure was similar to that used to probe the ability of fluorinated graphene to prevent silicide formation described in chapter 5. Initially, two interfaces were compared: a Pt/Si-H interface where the Si sample had been etched in HF just prior to evaporation of Pt onto the surface, and a Pt/Gr/Si surface in which the Si had been etched in HF prior to graphene transfer to the Si surface (figure 6.5).



**Figure 6.5.** XP spectra of the Pt 4f region of Pt/Si-H and Pt/Gr/Si interfaces. The presence of two doublet sets of peaks in the Pt/Si-H interface spectrum as well as their peak positions (low binding energy doublet: 71 and 74 eV, high binding energy doublet: 72 and 76 eV), is consistent with formation of PtSi. The single set of doublet peaks in the Pt/Gr/Si interface spectrum is consistent with the inhibition of silicide formation.

The data in figure 6.5 suggests that pristine monolayer graphene does prevent silicide formation. However, silicon oxide layers are known to inhibit platinum silicide formation and the wet transfer methods used to transfer graphene to silicon are known to generate a thin oxide layer at the Si/Gr interface (chapter 4).<sup>1, 2</sup> The ability of thin layers of SiO<sub>x</sub> to inhibit silicide formation was confirmed by taking a silicon sample, cleaning it with organic solvent (methanol, isopropanol, acetone), but not etching in HF prior to evaporation of Pt, giving a SiO<sub>x</sub>/Pt interface. Figure 6.6 compares the XP spectra of SiO<sub>x</sub>/Pt and Pt/Gr/Si interfaces.



**Figure 6.6.** XP spectra of the Pt 4f regions of SiO<sub>x</sub>/Pt and Pt/Gr/Si interfaces. In both spectra, the presence of a single doublet at 71 and 74 eV suggests that no PtSi phase was formed.

Because SiO<sub>x</sub> was also effective at inhibiting PtSi formation, and it is known that SiO<sub>x</sub> is present at the Gr/Si interface, it was no longer clear that graphene was the reason for the inhibition of PtSi formation at Pt/Gr/Si interfaces. In order to understand whether graphene was able to inhibit PtSi formation without the presence of a thin SiO<sub>x</sub> layer, methylated Si (111) surfaces were employed. Unlike hydride-terminated surfaces, methylated silicon surfaces do not form a substantial oxide layer upon graphene transfer (chapter 5). Thus, the ability of Si-Me and Si-Me/Gr interfaces to prevent PtSi formation on evaporation of Pt onto the respective surfaces was probed via XPS (figure 6.7). This suggests that graphene does indeed inhibit silicide formation.



**Figure 6.7.** XP spectra of the Pt 4f region of Pt/Si-Me and Pt/Gr/Si-Me interfaces. The presence of two doublet sets of peaks in the Pt/Si-Me interface spectrum as well as their peak positions (low binding energy doublet: 71 and 74 eV, high binding energy doublet: 72 and 76 eV), is consistent with formation of PtSi. The single set of doublet peaks in the Pt/Gr/Si-Me interface spectrum is consistent with the inhibition of silicide formation.

Additional study of the generality of the ability of graphene to prevent Si/metal interactions should be explored, but I note here that some work in this vein has been done by other groups.<sup>3-6</sup> Study of the J-E behavior of these interfaces to understand the equilibrium energetics of the interface would constitute additional novel work.

# 6.4 Fabrication of graphene chemical vapor deposition (CVD) chamber and monolayer graphene growth

There has been an extensive effort by many research teams across the world to understand and improve graphene growth techniques.<sup>7-10</sup> While most of the CVD grown graphene used in this thesis was obtained from collaborators at Columbia University or purchased from ACS Materials Inc., we decided that it would be valuable to have our own graphene growth source in order to gain further control over the variables that may affect the results of our graphene based experiments. Thus, a home-built graphene chemical vapor deposition chamber was fabricated by Ron Grimm, Fan Yang, and myself (Figure 6.8).



**Figure 6.8.** Home-built graphene CVD system (Toto). In the center of the image, the tube furnace and associated glass tube chamber are present. In the upper left, the MFCs used to control flow rates for Ar,  $H_2$ , and  $CH_4$  can be observed. On the right, the pressure gauges can be seen.

The CVD system has a number of useful features, including the ability to attain pressures as low at  $10^{-6}$  Torr and temperatures as high as  $1100 \,^{\circ}$ C. Flow rates for each gas are: CH<sub>4</sub> (0.3-200 sccm), H<sub>2</sub> (1-50 sccm) and argon (2-100 sccm). The ability to attain high temperature and low pressure make it useful in the graphene annealing steps noted in Chapters 4 and 5.

This home-built CVD system was used under a number of different conditions in order to grow monolayer graphene sheets. Using the conditions described in the appendix of chapter 4 and in Petrone, et. al, monolayer graphene was grown.<sup>11</sup> However, we desired to grow graphene with larger grain sizes. Following literature precedent, we lowered the  $CH_4$  partial pressure during the initial phase of growth. This led to the graphene crystals observed via optical microscopy as seen in figure 6.9. Briefly, the recipe proceeded as follows: Cu foil was loaded into the growth chamber and the chamber was evacuated to  $(5 \times 10^{-5})$  Torr. The chamber was then heated to 1000 °C while flowing 40 sccm H<sub>2</sub>. After 30 minutes at 1000 °C, the H<sub>2</sub> flow rate was modified to 50 sccm and the CH<sub>4</sub> flow rate was set to 0.5 sccm while maintaining 1000 °C. This was the graphene growth. After one hour, the furnace was cooled quickly using a fan. During the cooling process, the flow rates used in the previous step were maintained (50 sccm  $H_{2}$ ) 0.5 sccm CH<sub>4</sub>) until the temperature reached <300 °C. Once the furnace was cooled below 300 °C, all flows were ceased and the furnace was allowed to cool to room temperature. Modifying this recipe to include a high flow rate  $CH_4$  step (25 sccm H2, 100 sccm CH<sub>4</sub> at 1000 °C after the growth step noted above) led to continuous monolayer films with Raman spectra consistent with low defect, monolayer graphene (figures 6.10a, 6.10b).



**Figure 6.9.** Optical image of graphene grown using a low  $CH_4$  flow rate recipe. The grown graphene was transferred to 300nm  $SiO_2$  using the PMMA transfer methods described in chapters 4 and 5. The large crystals visible in this image are suggestive of large (~50 µm on a side) single crystals of graphene. It is also clear that a continuous sheet of monolayer graphene was not formed during this growth.

![](_page_14_Picture_2.jpeg)

**Figure 6.10a.** Optical image of graphene grown using the modified low/high  $CH_4$  flow rate recipe. The grown graphene was transferred to 300nm  $SiO_2$  using the PMMA transfer methods described in chapters 4 and 5. A continuous sheet of monolayer graphene appears to be present. A small rip in the top center of the image gives contrast to highlight covered and uncovered sections of  $SiO_2$ . The Raman in figure 610.b confirms the monolayer nature of the graphene.

![](_page_15_Figure_0.jpeg)

**Figure 6.10b.** Raman spectrum of graphene grown using the modified low/high  $CH_4$  flow rate recipe. The grown graphene was transferred to 300nm SiO<sub>2</sub> using the PMMA transfer methods described in chapters 4 and 5. The large D/G peak ratio (~1350 cm<sup>-1</sup> vs. 1580 cm<sup>-1</sup> peaks) just low-defect graphene and the G/2D peak ratio (1580 cm<sup>-1</sup> vs. 2680 cm<sup>-1</sup>) suggest monolayer graphene.

The data in figures 6.9 and 6.10 suggest that the home-built graphene CVD is capable of producing high quality, continuous graphene sheets. Further study is needed to determine the consistency with which the CVD instrument produces high quality graphene. Assuming this can be determined, the ability to grow graphene with varying grain sizes in a polycrystalline sheet opens the possibility of correlating the ability of graphene to act as a protective layer with the grain size of the polycrystalline sheet. Additionally, bilayer and trilayer graphene should be growable as well, and can be used to compare the protective ability as well as the electronics of as-grown multilayer graphene sheets against protective ability and electronics of multilayer graphene sheets formed by multiple transfer processes.

# 6.5 Impurities at the graphene/silicon interface after different transfer procedures

A goal throughout this thesis was to understand how graphene and silicon interact in terms of the equilibrium energetics of the interface as well as the stability. One of the key challenges in probing this interface is the atomically thin nature of graphene. Because graphene is atomically thin and limited in electronic states, it is reasonable to assume that it is prone to transfer damage and susceptible to changes in electronic state or structure as a result of minute amounts of impurities. Compounding this problem is the fact that using CVD graphene requires that the graphene surface come in contact with a number of different chemicals from the etchants required to remove the copper foil, the polymer layer used to handle the graphene without the Cu foil, and residual Cu after etching. The focus of this section is to briefly understand the effects of modifying the transfer procedure on the graphene/silicon interface.

One of the most commonly employed etch steps to separate CVD-grown graphene from the copper growth substrate uses an aqueous FeCl<sub>3</sub> solution to oxidize the copper foil. Specifically, after graphene growth on the Cu foil, a PMMA layer was spincasted over the graphene layer, followed by a ~30 minute etch in FeCl<sub>3</sub> (aq), transfer of the resulting PMMA/Gr layer to three consecutive clean water baths. The H<sub>2</sub>O washed PMMA/Gr layers were then transferred to the substrate of interest, baked at 80 °C for 10 minutes in air, followed by removal of PMMA by immersion in acetone, and finally an anneal under 95:5 Ar/H<sub>2</sub> gas for two hours (referred to the 'standard' transfer). This was also the most commonly employed etch step in this thesis. Common XP spectra of the resulting Gr/Si interface are depicted in figure 6.11 and an optical image of graphene transferred to  $300 \text{ nm SiO}_2/\text{Si}$  is shown in figure 6.12.

![](_page_17_Figure_2.jpeg)

**Figure 6.11.** (Top left, bottom left) XP survey spectra of Gr/Si interfaces after the 'standard' transfer. The Fe 2p region of the survey spectra is highlighted. (Top right, bottom right). XP spectra of the Fe 2p region of the samples represented on the left. Both  $Fe^{0}$  and  $FeO_{x}$  have been observed. Anecdotally,  $FeO_{x}$  is much more commonly observed that  $Fe^{0}$ .

![](_page_18_Picture_0.jpeg)

**Figure 6.12.** Optical microscopy image of graphene transferred to  $300 \text{ nm SiO}_2/\text{Si}$  using the 'standard' transfer method. The purple hue near the edges of the image are uncovered SiO<sub>2</sub>.

From the data in figures 6.11 and 6.12, it is clear that the 'standard' transfer procedure results in graphene that is continuous on the scale of the substrate it is transferred to, but also that there are Fe impurities left at the surface. As these iron impurities are known to p-dope the graphene surface, we also explored another common etch technique that employs an aqueous ammonium persulfate (APS) solution instead of FeCl<sub>3</sub> to etch the Cu foil.<sup>12, 13</sup> The advantage in using APS is that because it is an organic oxidizer, it cannot leave metallic impurities at the Gr/Si interface, thus reducing the likelihood of doping of the graphene surface via an impurity left at the surface. Using the APS etching method, the XP spectrum of a Gr/Si interface in figure 6.13 was obtained. An optical image of a 300 nm SiO<sub>2</sub>/Si interface is shown in figure 6.14.

![](_page_19_Figure_0.jpeg)

Figure 6.13 XP survey spectra of Gr/Si interfaces after the APS transfer.

![](_page_19_Picture_2.jpeg)

**Figure 6.14.** Optical microscopy image of graphene transferred to 300 nm SiO<sub>2</sub>/Si using the APS transfer. The uncovered SiO<sub>2</sub> is predominantly on the right side of the image.

As seen figures 6.13 and 6.14, the APS transfer produces interfaces that are free of iron impurities, but the resulting graphene interface is heavily damaged. This has been attributed to interaction of the APS with the PMMA as APS is known to cross-link and thereby might cause the PMMA to strain the graphene as its morphology changes. It should be noted that APS has been reported as an etchant by other laboratories without reporting issues with cracked graphene.

In order to try and solve both the issues of removing Fe impurities while also ensuring transfer of a continuous layer of graphene, a 'modified FeCl<sub>3</sub>' transfer procedure was explored. This procedure is outlined in scheme 6.1.

![](_page_20_Figure_2.jpeg)

Scheme 6.1. 'Modified FeCl<sub>3</sub>' transfer procedure. This procedure was modified from the procedure suggested by Liang, et. al.<sup>12</sup>

The rationale behind scheme 6.1 is the inclusion of dilute acidic and basic washes, akin to the well-known SC-1 and SC-2 clean procedures common in the semiconductor industry, to remove metallic impurities without damaging the graphene surface. The XP spectrum of the Gr/Si interface resulting from a 'modified FeCl<sub>3</sub>' clean can be seen in figure 6.15 and an optical image of a 300 nm SiO<sub>2</sub>/Si interface fabricated from a 'modified FeCl<sub>3</sub>' is shown in figure 6.16.

![](_page_21_Figure_1.jpeg)

**Figure 6.15.** (left) XP survey spectra of Gr/Si interfaces after the 'modified FeCl<sub>3</sub>' transfer. (right). XP spectra of the Fe 2p region of the samples represented on the left.

![](_page_22_Picture_0.jpeg)

**Figure 6.16.** Optical microscopy image of graphene transferred to 300 nm  $SiO_2/Si$  using the 'modified FeCl<sub>3</sub>' transfer method. The purple hue near the edges of the image are uncovered  $SiO_2$ .

From the data in figures 6.15 and 6.16, it is clear that the 'modified FeCl<sub>3</sub>' transfer reduced the amount of Fe impurities at the Gr/Si interface with respect to the 'standard' transfer while also reducing the damage to the graphene surface with respect to the APS transfer method.

Transferring graphene to substrates cleanly while minimizing damage to the graphene itself is challenging and is an active area of research.<sup>9, 10, 14, 15</sup> With regards to future study of the Gr/Si interface, one should always take care to ensure that their graphene is transferring cleanly and without damage by utilizing XPS, Raman spectroscopy, and optical microscopy, particularly when CVD graphene is being employed. Many of the issues that one hopes to avoid (damage to the surface, unintended

impurities) can be avoided through the use of single crystal graphene flakes obtained via micromechanical cleavage of an HOPG surface. While using single crystal graphene flakes is advantageous for the reasons noted above, it has the disadvantage of being significantly more challenging to obtain and manipulate said flakes, and it limits the size of the interface to the size of obtainable single graphene flakes, which can often be below  $100 \ \mu m^2$ . That said, using single crystal graphene flakes to understand the inherent properties of the Gr/Si interface in tandem with CVD graphene to understand how the impurities left by the graphene transfer methods affect the Gr/Si chemical and electrochemical behavior on large scale interfaces is a promising future venue for this work.

#### 6.6 ALD deposition on monolayer graphene

ALD deposition of metal oxides on pristine graphene surfaces has been demonstrated with a number of metals, including platinum, hafnium, and aluminum.<sup>16-18</sup> Without additional treatment, deposition is generally observed at defects in pristine graphene sheets, as these sites provide reactive centers to seed metal oxide growth.<sup>18</sup> This makes ALD deposition of graphene an interesting candidate method for 'sealing' the defective sites that may be the source of failure in graphene-based protective coatings. In order to test the hypothesis that ALD coatings may cover defect sites on graphene and improve the ability of the modified graphene to prevent passivation at silicon surfaces, I exposed monolayer graphene on Cu foil to the following ALD experimental procedure: The Gr/Cu foil was placed in the center of the reaction chamber, and the chamber was evacuated with a rotary vane pump. A valve connecting the reaction chamber to a TDMAT [tetrakis(dimethylamido)titanium] vapor source (source heated to 75 °C) was opened for 0.1 seconds. After a 15 second wait time, a valve connecting the reaction chamber to an  $H_2O$  source (source at room temperature) was opened for 0.015 seconds. This was followed by another 15 second wait time. The process of pulsing in TDMAT followed by H<sub>2</sub>O was repeated for 22 cycles. We assumed this would produce approximately 1 nm of TiO<sub>2</sub> near reaction sites, as previous work in the group suggested that 5 nm TiO<sub>2</sub> was observed after 100 cycles. Analysis of the XP spectrum of the resulting Gr/Cu foil suggested that  $TiO_2$  was deposited on the graphene surface (Figure 6.17).

![](_page_25_Figure_0.jpeg)

**Figure 6.17.** XP spectrum of the Ti 2p region of a Gr/Cu foil after exposure to ALD conditions. The presence of measureable Ti 2p counts at 459 and 464 eV suggests that the ALD method was successful at depositing  $TiO_2$  on the graphene surface

Using the transfer methods described in Chapters and 5, the TiO<sub>2</sub> modified graphene was transferred to moderately doped n-Si and tested photoelectrochemically in aqueous 350 mM  $\text{Fe}(\text{CN})_6^{4-}$  – 50 mM  $\text{Fe}(\text{CN})_6^{3-}$  electrolyte for photoactivity and stability (Figure 6.18, Figure 6.19)

![](_page_26_Figure_0.jpeg)

**Figure 6.18.** J-E behavior of ALD TiO<sub>2</sub> modified-graphene covering n-Si electrode in aqueous 350 mM  $\text{Fe}(\text{CN})_6^{4-} - 50 \text{ mM Fe}(\text{CN})_6^{3-}$  electrolyte over 3 potential sweeps at 30 mV s<sup>-1</sup> under ~33 mW cm<sup>-2</sup> illumination from an ENH lamp.

![](_page_26_Figure_2.jpeg)

**Figure 6.19.** J-t behavior of ALD  $\text{TiO}_2$  modified-graphene covering n-Si electrode in aqueous 350 mM Fe(CN)<sub>6</sub><sup>4-</sup> – 50 mM Fe(CN)<sub>6</sub><sup>3-</sup> electrolyte over 25,000 s under ~33 mW cm<sup>-2</sup> illumination from an ENH lamp.

The data in figures 6.18 and 6.19 suggest that the  $TiO_2$  does not destroy the photoactivity of the Si/Gr/electrolyte interface. Without additional experimentation and trials, it is yet unclear whether the  $TiO_2$  improves the stability of this interface, but it does

not prevent stability from being observed. Future work in this area should explore whether other metals are compatible with the ALD deposition method (XPS), explore whether the metals are deposited uniformly or at defect sites (SEM, AFM), and determine whether the deposition improves the ability of the graphene protective coating to inhibit deleterious reactions at semiconductor surfaces (electrochemistry, XPS). Additionally, the presence of graphene at the semiconductor surface could be used to probe the effect of preventing a SiTiO<sub>x</sub> or SiO<sub>x</sub> interface from forming at Si/TiO<sub>2</sub> junctions that have been recently studied in our group.<sup>19</sup>

## 6.7 Conclusion

Graphene can be used for a myriad of purposes.<sup>20-24</sup> In this chapter, and in this thesis, I have explored just a small number of these purposes as they relate to the graphene/silicon interface under photoelectrochemical conditions. The key to understanding how graphene interacts with silicon under these conditions is to be fastidiously careful in device fabrication and to demand consistency in results. While I regret that I was not always able to live up to these rigorous standards, I believe time and effort will reveal the true nature of this interface, and I hope that in some small way I have helped lay the groundwork for future scientists to continue exploring this field.

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