Heteroepitaxy of Group IV and Group III-V semiconductor alloys on Si for photovoltaic applications

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"We are like tenant farmers chopping down the fence around our house for fuel when we should be using Nature's inexhaustible sources of energy – sun, wind and tide... I'd put my money on the sun and solar energy. What a source of power! I hope we don't have to wait until oil and coal run out before we tackle that."

Thomas Edison, in conversation with Henry Ford and Harvey Firestone

Abstract

Photovoltaic energy conversion represents a economically viable technology for realizing collection of the largest energy resource known to the Earth – the sun. Energy conversion efficiency is the most leveraging factor in the price of energy derived from this process. This thesis focuses on two routes for high efficiency, low cost devices: first, to use Group IV semiconductor alloy wire array bottom cells and epitaxially grown Group III-V compound semiconductor alloy top cells in a tandem configuration, and second, GaP growth on planar Si for heterojunction and tandem cell applications.

Metal catalyzed vapor-liquid-solid grown microwire arrays are an intriguing alternative for wafer-free Si and SiGe materials which can be removed as flexible membranes. Selected area Cu-catalyzed vapor-liquid solid growth of SiGe microwires is achieved using chlorosilane and chlorogermane precursors. The composition can be tuned up to 12% Ge with a simultaneous decrease in the growth rate from 7 to 1 μm min^{-1}. Significant changes to the morphology were observed, including tapering and faceting on the sidewalls and along the lengths of the wires. Characterization of axial and radial cross sections with transmission electron microscopy revealed no evidence of defects at facet corners and edges, and the tapering is shown to be due to in-situ removal of catalyst material during growth. X-ray diffraction and transmission electron microscopy reveal a Ge-rich crystal at the tip of the wires, strongly suggesting that the Ge incorporation is limited by the crystallization rate.

Tandem $Ga_{1-x}In_xP$/Si microwire array solar cells are a route towards a high efficiency, low cost, flexible, wafer-free solar technology. Realizing tandem Group III-V compound semiconductor/Si wire array devices requires optimization of materials growth and device performance. GaP and $Ga_{1-x}In_xP$ layers were grown heteroepitaxially with metalorganic chemical vapor deposition on Si microwire array substrates. The layer morphology and crystalline quality have been studied with scanning electron microscopy and transmission electron microscopy, and they provide a baseline for the growth and characterization of a full device stack. Ultimately, the complexity of the substrates and the prevalence of defects

resulted in material without detectable photoluminescence, unsuitable for optoelectronic applications.

Coupled full-field optical and device physics simulations of a $Ga_{0.51}In_{0.49}P/Si$ wire array tandem are used to predict device performance. A 500 nm thick, highly doped "buffer" layer between the bottom cell and tunnel junction is assumed to harbor a high density of lattice mismatch and heteroepitaxial defects. Under simulated AM1.5G illumination, the device structure explored in this work has a simulated efficiency of 23.84% with realistic top cell SRH lifetimes and surface recombination velocities. The relative insensitivity to surface recombination is likely due to optical generation further away from the free surfaces and interfaces of the device structure.

Finally, GaP has been grown free of antiphase domains on Si (112) oriented substrates using metalorganic chemical vapor deposition. Low temperature pulsed nucleation is followed by high temperature continuous growth, yielding smooth, specular thin films. Atomic force microscopy topography mapping showed very smooth surfaces (4-6 ÅRMS roughness) with small depressions in the surface. Thin films ($\sim$ 50 nm) were pseudomorphic, as confirmed by high resolution x-ray diffraction reciprocal space mapping, and 200 nm thick films showed full relaxation. Transmission electron microscopy showed no evidence of antiphase domain formation, but there is a population of microtwin and stacking fault defects.

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Music has been an important part of my life since my high school years. I've had the privilege of playing in the Caltech jazz and concert bands during my time here at Caltech. Bill Bing is one of the nicest people I have ever met and a fantastic musician and conductor. His retirement next year marks the end of an era for student and community music at Caltech that anyone would be hard pressed to come close to. Playing in the jazz band under Barb Catlin's direction has been a great honor – she is always ready to challenge the musicians in the band to play challenging music, and I've become a better musician as a result. Both Bill and Barb are always ready to lend a shoulder or ear in good times and bad. My band mates over the years, among them Jeff Thompson, Ajay Limaye, Jeremy Yager, Zach Aitken, Matt Abrahamson, Austin Minnich, Will Rose, Muir Morrison, Matt Davis, Mike Post, Kris Kokame, Sam Gill, Megan Sumida, Sung Byun, and Rob Usiskin, were all a pleasure to hang and play music with.

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The content of this thesis has been drawn from the following publications.

- C. T. Chen, S. Aloni, R. Saive, H. S. Emmer, and H. A. Atwater, "Antiphase domain free growth of GaP on Si (112) with metalorganic chemical vapor deposition," *in preparation.*

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- C. T. Chen, H. S. Emmer, S. Aloni, and H. A. Atwater, "GaP/Si Heterojunction Solar Cells," in *Photovoltaics Specialists Conference (PVSC), 2015 42nd IEEE*, New Orleans, LA, 2015.

- C. T. Chen, D. B. Turner-Evans, H. S. Emmer, S. A. Aloni, and H. A. Atwater, "Design and Growth of III-V on Si Microwire Array Tandem Solar Cells," in *Photovoltaics Specialists Conference (PVSC), 2013 39th IEEE*, Tampa, FL, 2013, pp. 3397-3401.

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Chapter 1

Introduction

1.1 Energy, Climate, and the 21st Century

As put forward by Richard Smalley in his "Terawatt Challenge" [78], energy and atmospheric CO_2 are among the most pressing challenges facing the world in the nascent 21st century.

The greenhouse effect was discovered by Joseph Fourier in 1820. When he considered the energy balance between the sun and the Earth, he found that the temperature of the Earth was only sustainable if the atmosphere absorbed some thermal energy. Over the past 200 years, it has become common knowledge that CO_2, whether of natural or anthropogenic origin, is a major contributor to greenhouse warming of the atmosphere. Furthermore, CO_2 concentrations in the atmosphere have reached their highest level in 800,000 years at 402 ppm.[1] Atmospheric CO_2 levels pose a serious threat to the chemistry of the atmosphere and oceans. The Intergovermental Panel on Climate Change is certain that both the Earth's atmosphere and ocean have seen increases in temperature since the 1950's and that some of the changes observed are very significant.[2] Furthermore, 95% of scientists agree that

[1] National Oceanic and Atmospheric Administration, "Greenhouse gas benchmark reached."

[2] IPCC, Climate Change 2013: The Physical Science Basis - Summary for Policymakers, Observed Changes in the Climate System, p.2

greenhouse gas emissions and other human activities have likely caused the majority of this warming effect.[3] The potential consquences of greenhouse gas induced warming are quite dire, with dramatic impacts on coastal communities, rainfall, and glacial ice.

Higher atmospheric CO_2 levels will also lead to acidification as the gas is absorbed into the world's oceans [3], leading to disruption of aquatic and terrestrial ecosystems worldwide. One example of this is with coral, which may simply dissolve [62]. The potential impacts of this and other disruptions to marine ecosystems cannot be understated.

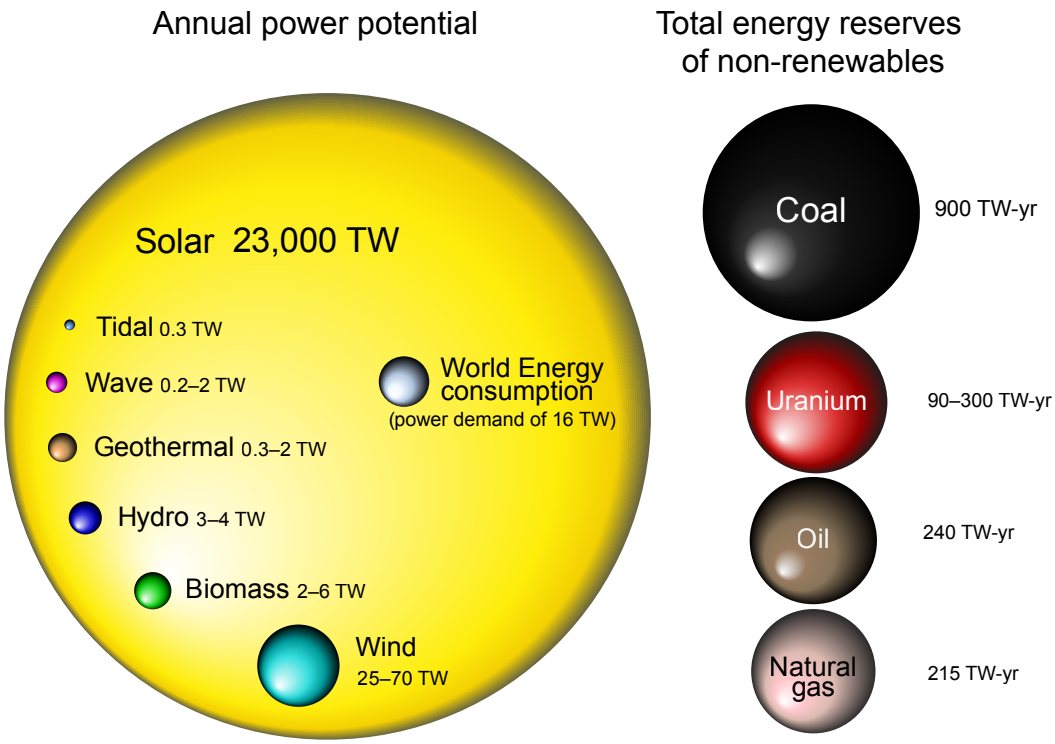


FIGURE 1.1: Graphical depiction of annual renewable energy potential and total nonrenewable energy reserves compared to annual energy consumption. Based on R. Perez, "A Fundamental Look at Energy Reserves of the Planet," 2009.

Currently the energy market is dominated by fossil fuels in the form of coal, oil, and natural gas. Fossil fuels do have tremendous advantages in energy density and stability. However,

[3]IPCC, Climate Change 2014: Synthesis Report - Summary for Policymakers

alternative energy technologies will become economically viable as the costs of finding new fossil fuel sources and higher atmospheric CO_2 concentrations increase. By far the most plentiful and sustainable source of energy is found in solar radiation. As depicted pictorially in Figure 1.1, incident sunlight on the surface of the Earth represents a total energy three orders of magnitude greater than total world energy consumption and dwarfs the total potential annual renewable energy production of both other renewable technologies and the terrestrial reserves of non-renewable sources of energy.

1.2 Photovoltaics

1.2.1 The photovoltaic effect

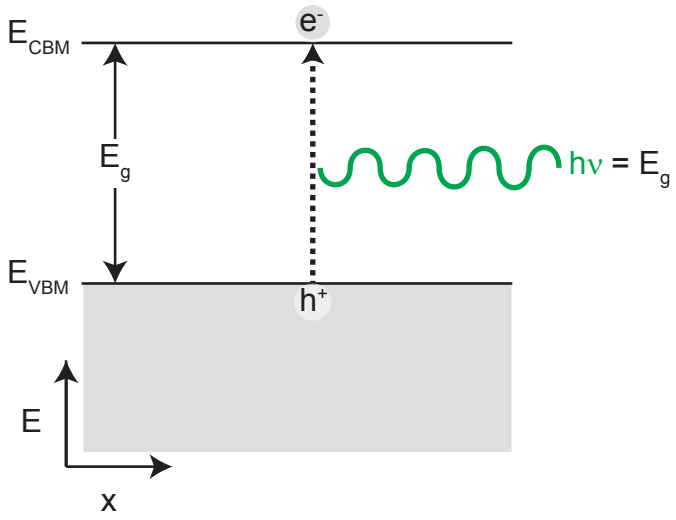


FIGURE 1.2: Light absorption depicted in a hypothetical semiconductor.

Harnessing the energy potential of incident solar radiation requires the conversion of electromagnetic energy into a useful form. This can be done by taking advantage of the photovoltaic effect in semiconductor materials. Semiconductors are characterized by an energy bandgap which separates bound electrons in the valence from free electrons in the conduction band. Photons with energy greater than or equal to the bandgap can be absorbed by the semiconductor, promoting an electron from the bound energy band into the free electron energy band (Figure 1.2). Photoexcited electrons in the conduction band leave behind empty states in the valence band. These empty states, or holes, behave like positively charged particles, and electrons in the conduction band can recombine with holes in the valence band. Energy in excess of the bandgap is quickly lost by thermalization, while light with energy less than the bandgap is not absorbed and is simply transmitted through the material. Generation of electron hole pairs and their collection at contacts of opposite polarity are the basis of photovoltaic devices.

1.2.2 The solar resource

Light absorption by various components of the atmosphere, most notably water and greenhouse gases, reduces the incident flux and power of solar irradiation by about 18% [28]. Furthermore, light is scattered by molecules and particulates, resulting in the scattering of 3% to space and 7% to Earth [28], resulting in a considerable fraction of diffuse light. Standard spectra are derived from the standard space spectrum, AM0, where AM stands for air mass index ($AM = (cos\,\theta)^{-1}$, where θ is the angle of incidence). Almost all measurements are typically done with the AM1.5G or global spectrum, which includes diffuse light contributions, or the AM1.5D or direct spectrum, which only includes direct light [1]. The AM1.5G spectrum is plotted in Figure 1.3.

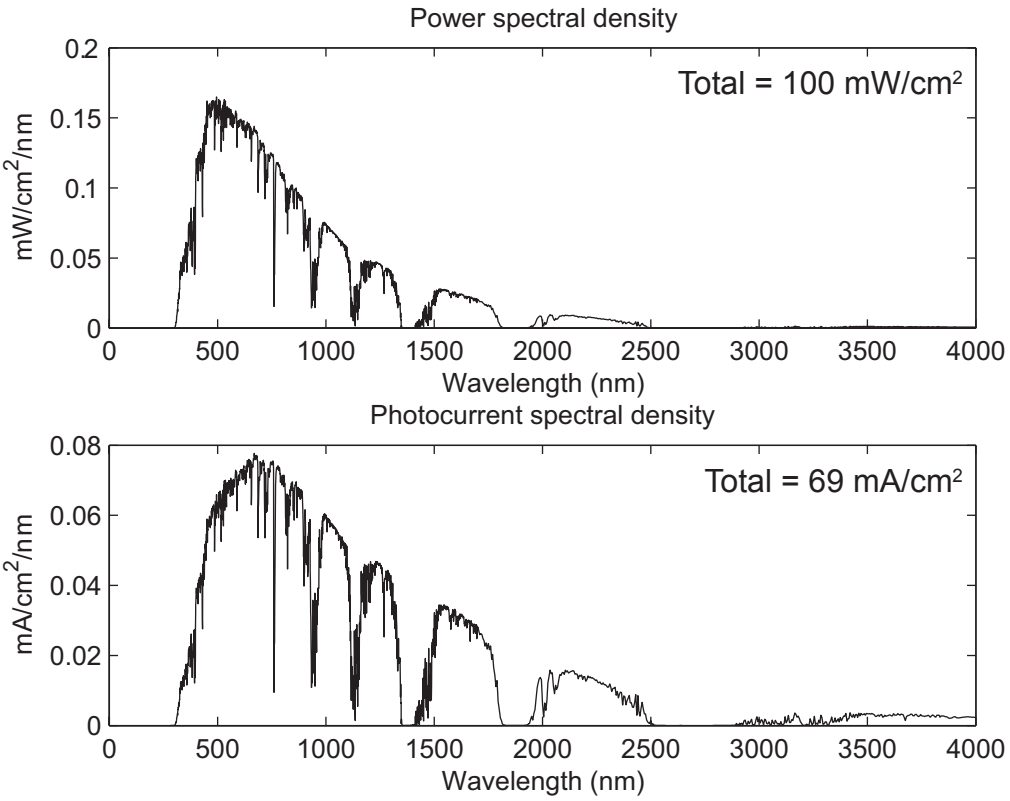


FIGURE 1.3: AM1.5G spectrum power and photocurrent spectral density. Figure courtesy of Dr. Michael Kelzenberg.

1.2.3 Photovoltaic devices

Figure 1.4 depicts the current-voltage plot of a hypothetical solar cell for both illuminated (light IV, LIV) and dark conditions. In the dark, a solar cell behaves much like a typical diode. Under illumination, current generated by absorbed light can be collected at the contacts of the device.

At open circuit, the generated electron-hole pairs are separated by electric fields in the device and recombine slowly. The difference in population of carriers on either side of the junction results in a potential difference between the two contacts, known as the open circuit voltage (V_{OC}). Intuitively, the V_{OC} will decrease with increasing defect or impurity

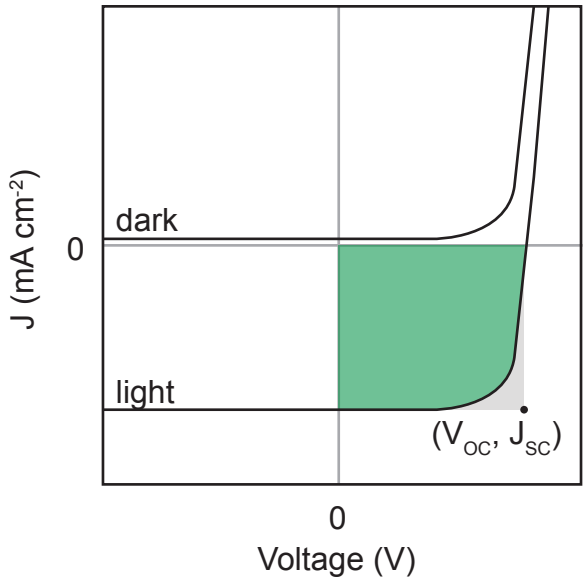


FIGURE 1.4: Hypothetical LIV curve for a solar cell.

density, as an increase in the recombination rate will reduce the number of generated charge carriers, resulting in a lower potential difference. The V_{OC} is thus a good measure of carrier recombination in the bulk or at the surfaces of a photovoltaic device.

At short circuit, current can flow freely through the device, and charge carriers recombine at the contacts. This results in the short circuit current (J_{SC}), which corresponds to the amount of optical generation in the material.

The maximum power point of a photovoltaic device is represented here schematically as $P_m = J_m \cdot V_m$. An ideal photovoltaic device will have a maximum power point $P_m^{ideal} = J_{SC} \cdot V_{OC}$. The fill fraction, FF, is the ratio of P_m^{ideal} and P_m, represented graphically by the ratio between the areas of the gray and green regions in Figure 1.4.

$$FF = \frac{P_m}{J_{SC} \cdot V_{OC}} \tag{1.1}$$

The efficiency, η, is simply the ratio of P_m and the total power input from the sun, $P_{in} = 100$ mW cm^{-2} for the AM1.5G spectrum.

$$\eta = \frac{J_{SC} \cdot V_{OC} \cdot FF}{P_i n} \tag{1.2}$$

1.2.4 Limits of photovoltaic efficiency

The "detailed balance" or Shockley-Queisser limit [75] represents an upper bounds on the efficiency of photovoltaic light absorption can be calculated. In this approximation, the sun is treated as a black body and the absorption and emission of the solar cell is calculated assuming all of the above bandgap light is absorbed. The difference between the absorption and emission is the current of the device, which can then be used to calculate other thermodynamic quantities. In this approximation, ideal single junction absorbers are limited to $\sim$ 33% efficiency [75]. By taking into account inherent losses, single junction silicon solar cells have a theoretical maximum of 29.8% efficiency [84]. The greatest source of loss in a single junction solar cell is due to carrier thermalization [67]. By incorporating multiple cells, the energy in the solar spectrum can be extracted in a more optimal manner, as depicted in Figure 1.5. By moving to a multijunction architecture, the detailed balance efficiency is greatly increased; without considering any constraints on the choice of bandgaps, an ideal tandem cell has 42.2% detailed balance AM1.5G efficiency, while an ideal triple junction cell has a detailed balance efficiency of 47.2% [5].

1.2.5 A photovoltaics renaissance

Global energy consumption in 2012 was 104,406 TWh.[4] The global energy business is a multi-trillion dollar business. Energy production with solar photovoltaics represents a

[4]International Energy Agency, "Key World Energy Statistics,"
`http://www.iea.org/publications/freepublications/publication/keyworld2014.pdf`

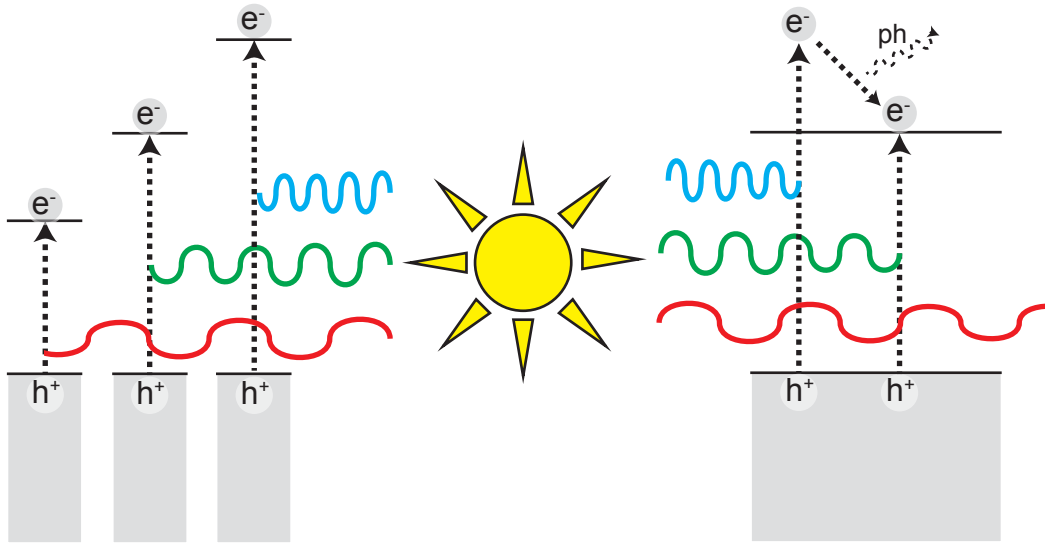


FIGURE 1.5: Multijunction solar cells reduce loss from the thermalization of electrons excited by above bandgap photons to the conduction band edge and recovers energy from below bandgap photons compared to a single junction.

market opportunity that can capitalize on the desire for distributed energy generation and the impending impacts of climate change.

In the past ten years, photovoltaics have gone from a niche industry to a significant contributor to the future energy landscape in the US. As of 2015, the photovoltaics industry has outstripped flat panel displays to become the largest optoelectronic industry, and, furthermore, photovoltaics is now approaching the scale of the complementary metal oxide semiconductor industry. Deutsche Bank now predicts that solar will reach grid parity in 80% of world markets by 2017.[5]

Silicon is the dominant technology in the microelectronics and photovoltaics industries. However, the capabilities afforded by silicon-based technologies are rapidly approaching their limits. After years of following Moore's Law, the size of silicon transistor technologies

[5]Deutche Bank, "Deutsche Bank's 2015 solar outlook: accelerating investment and cost competitiveness." `https://www.db.com/cr/en/concrete-deutsche-banks-2015-solar-outlook.htm`

is rapidly approaching a minimum practical limit. Silicon solar cells have reached record efficiencies of 25.6% [50] after over a decade of the 25.0% world record [23]. 25% efficiency has been demonstrated with a manufacturable process [79].

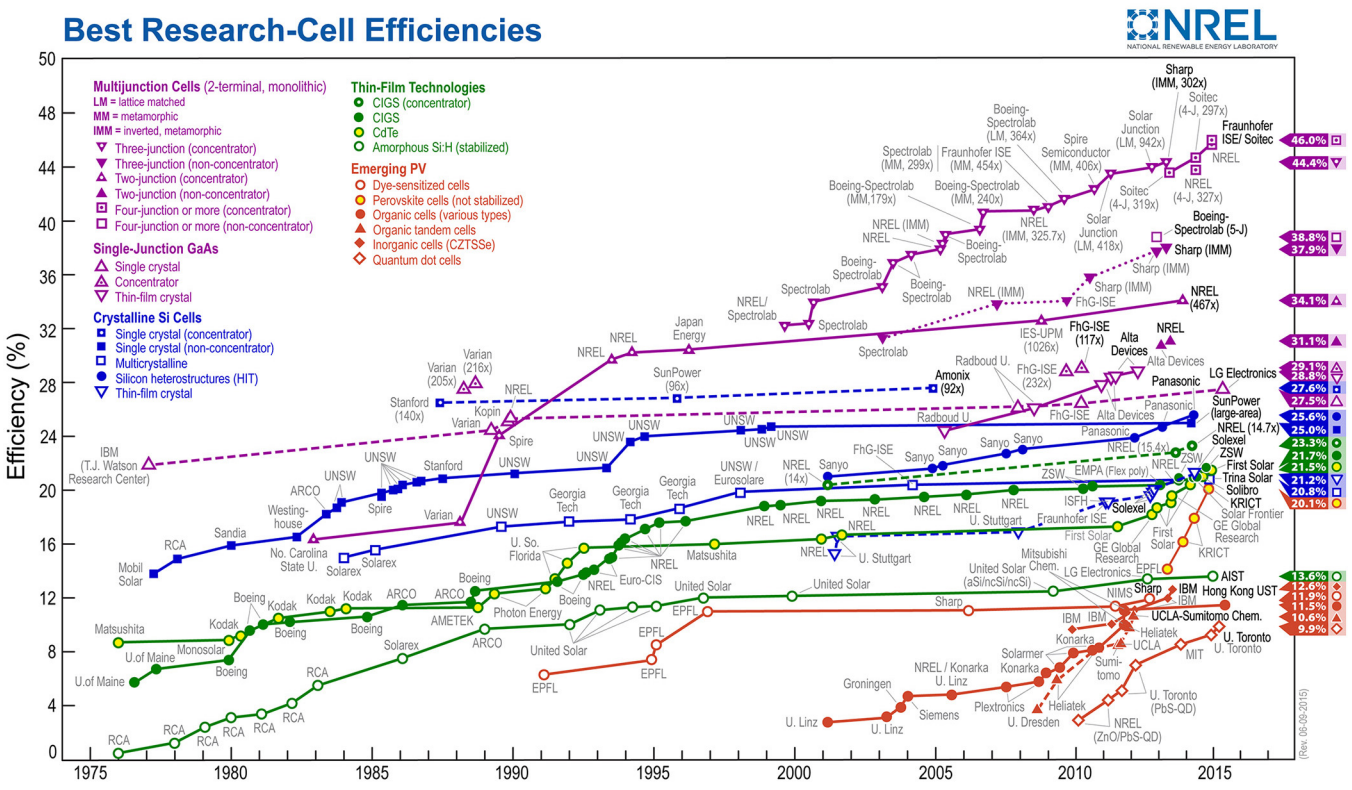


FIGURE 1.6: Historical chart of best research cell efficiencies compiled by the National Center for Photovoltaics. This plot is courtesy of the National Renewable Energy Laboratory, Golden, CO.

Group III-V compound semiconductors have been used in a diverse array of electronic and optoelectronic capacities, enabling faster transistors, better power electronics, efficient and tunable light sources in the form of light emitting diodes and semiconductor lasers, and high performance single and multijunction photovoltaic devices. Chief among their strengths is a direct bandgap, affording strong light absorption and emission characteristics, and the ability to tune the bandgap from near the ultraviolet to the near-infrared by making two, three, or even higher number component alloy systems. Photovoltaic devices based on these materials hold many of the efficiency records (Figure 1.6), a testament to the significant advantages that they possess compared to crystalline silicon or other thin film compound semiconductor technologies.

Despite their merits, solar cells based on Group III-V compound semiconductors are limited in their application by cost. Ge, GaAs, and InP wafers are much more expensive than Si, in part due to the lack of economies of scale and, in the case of the Group III-V compound semiconductors, challenges in growing high quality material. High quality materials are deposited using chemical vapor deposition or evaporation processes. Expense is incurred due to the low rate of deposition, chemical precursors, and vacuum requirements. Even with wafer reuse through epitaxial liftoff, estimates of cost place single junction GaAs solar cell production at $13/W today [94]. By switching to a tandem Group III-V compound semiconductor/Si device, efficiencies greater than a single junction can be reached with significantly lower cost today ($4/W, [94]).

1.3 Scope of this thesis

In the timespan of my doctoral work, the landscape of the solar photovoltaic device industry has been upended by very inexpensive, high performance Si solar cells. At the outset, the high quality Si wafers were thought to be too expensive, and much effort was placed into looking for competing thin film technologies. This motivated the work on Si microwire array growth in the Atwater group as a route towards eliminating Si wafers from the cost

equation through layer release and wafer reuse. However, energy conversion efficiency is the most leveraging property of a photovoltaic device, and these arrays would be limited to lower efficiencies due to high incorporation of the metallic catalyst during growth. Higher efficiences can be achieved by integrating Group III-V compound semiconductor top cells. This forms the motivation for my work on Group IV alloy microwire growth and the investigations of Group III-V compound semiconductor on wire array structures experimentally and computationally.

- *Chapter 2 – Group IV alloy microwire array growth*
  SiGe microwire arrays were grown to enable lattice matched growth of tandem III-V/SiGe microwire solar cells with high efficiency. Lattice matching typically results in higher material quality and reduces cost by eliminating lengthy growth of step-graded buffers to grow highly mismatched materials [94].

- *Chapter 3 – Group III-V compound semiconductor growth on Si microwire arrays*
  The growth of Group III-V compound semiconductors on Si microwire arrays was explored. Si microwires initally served as an analogue for SiGe microwire substrates with nearly lattice matched growth of GaP. Direct growth of highly mismatched GaInP was pursued in lieu of high Ge content SiGe microwire arrays.

- *Chapter 4 – Optoelectronic design of Group III-V compound semiconductor on Si microwire tandem cells*
  Coupled full-wave optical and drift-diffusion device physics simulations were performed to elucidate the performance potential of GaInP on Si microwire array tandem cells.

- *Chapter 5 – MOCVD of GaP on Si for c-Si photovoltaics*
  In the last chapter, epitaxial GaP is grown on Si substrate, with potential application as a heterojunction partner or as a virtual substrate for GaAsP or GaInP top cell growth. Modern growth techniques and characterization were applied to growth on Si (112) and Si (001) substrates. High quality layers are realized on Si (112).

1.4 Contributions to this thesis

Dr. Mike Kelzenberg, Dr. Daniel Turner-Evans, and Hal Emmer rehabilitated and automated the Si wire array growth CVD and added the ability to grow with $GeCl_4$. I had very minor contributions in building a small He leak testing cart around an SRS RGA200 residual gas analyzer to assist in the process. Their many man-hours of leak testing, LabView coding, and troubleshooting made the SiGe wire array growth work possible.

Hal Emmer was a vital partner in the growth of SiGe wire arrays. We worked together in preparing growth substrates, developing growth parameters and initial characterization with optical microscopy and SEM. Hal's contributions to our characterization were invaluable – he led the efforts on getting high quality SEM images and EDS compositional analysis. Not included in this thesis are his efforts to measure the electronic properties of the wires (which proved to be no easy task, thanks to the extreme taper of the wires) and his work on optical measurements of the SiGe wire array bandgaps with absorption and photoconductivity.

Dr. Emily Warmann provided the detailed balance code used to generate isoefficiency contours for series connected tandem cells under 1 sun AM1.5G illumination.

In addition to the upkeep of the D-Star MOCVD at the Molecular Foundry, Shaul Aloni provided valuable support and advice throughout. He performed some of the TEM characterization and analysis in the work on SiGe microwires and GaInP on Si microwire arrays. Tevye Kuykendall also provided assistance with the care and feeding of the MOCVD from time to time. Virginia Altoe made sure the SEM's were running and assisted with some of the TEM characterization.

Chapter 2

Group IV semiconductor alloy microwire array growth

2.1 Background

2.1.1 Vapor-liquid-solid growth with a metal catalyst

Metal catalyzed vapor-liquid-solid (VLS) growth of silicon was discovered in 1964 [89]. Even at that early time, there was some interest in studying the growth [19] and properties of the "whiskers" that resulted. The confluence of interest in "nano"-sized materials and the development of robust and readily available nanoscale characterization methods in the early 2000's led to an explosion in research into the fundamental growth mechanisms, materials properties, and applications of nanowires. As depicted in Figure 2.1, substrates for VLS growth are prepared with a layer of the metal catalyst deposited either as a thin film or in colloid form. After heating, the metal melts and forms droplets in contact with the substrate surface. Introduction of the constituent elements of the semiconductor of interest as chemical precursors or from a pulsed laser plume. VLS growth is named due to the presence of all three phases during the growth. It has been successfully applied to many

materials systems, including but not limited to Si [89], Ge [19], GaAs [49], InP [90], and alloys therein for the Group IV semiconductors and Group III-V compound semiconductors.

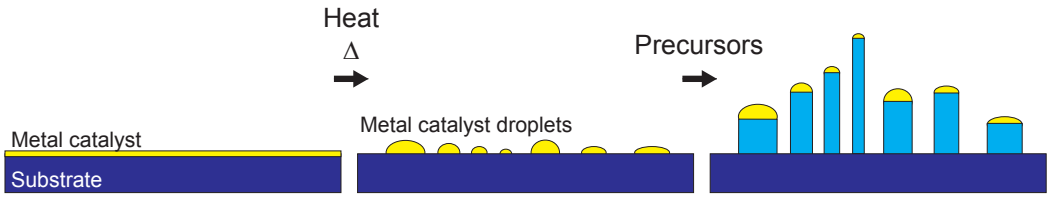


FIGURE 2.1: Schematic of a typical vapor-liquid-solid growth process.

The VLS growth process takes advantage of the thermodynamics of alloy formation and phase formation upon cooling. To illustrate this, it is necessary to review a simple eutectic temperature vs. composition phase diagram. Figure 2.2 depicts a simple eutectic phase diagram for hypothetical elements "A" and "B." There are several things to note about this phase diagram. First, the eutectic point, at which solid and liquid phases are in equilibrium, exists at the temperature $T_{eutectic}$ and composition $x_{eutectic}$. At temperatures higher than $T_{eutectic}$, a mixture of A and B at $x_{eutectic}$ is liquid, and below $T_{eutectic}$ the mixture is solid. If you add more of A or B to the system, the system will begin to form solid material of the same material. VLS exploits these principles in growing one material, such as Si, with a metal catalyst.

Figure 2.3 depicts a typical VLS growth process for Si wires on a Si substrate with a metal catalyst. First, the catalyst is heated to the eutectic temperature (1). At this point, the metal begins to react with the Si substrate, incorporating Si until it reaches $x_{eutectic}$ (2). As it is heated past $T_{eutectic}$, the catalyst liquifies and forms a droplet on the wafer surface (3). Then Si is introduced in the form of a physical or gaseous source, such as $SiCl_4$. This increases the amount of Si in the catalyst droplet until it is favorable to form solid Si (4). Solid material nucleates at the catalyst/Si interface, starting the wire growth until Si is no

longer delivered to the droplet. Finally, the wires are cooled to room temperature, leaving a solid wire with a solid catalyst particle at the tip of the wire (5).

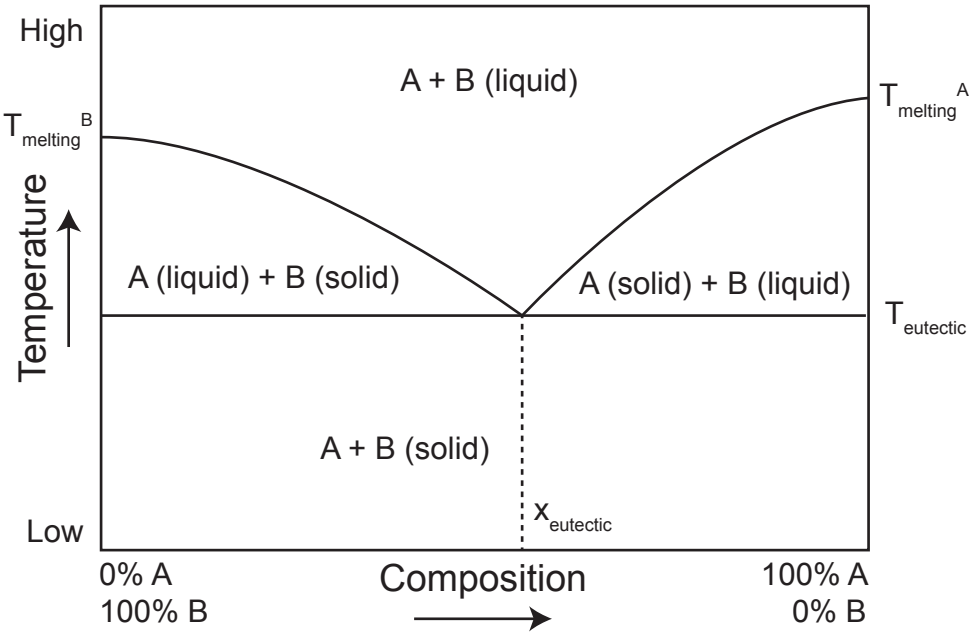


FIGURE 2.2: Typical eutectic phase diagram.

2.1.2 Silicon microwire array photovoltaics

The Atwater and Lewis groups at Caltech began their forays into nanowire-type photovoltaics through theoretical investigations by Dr. Brendan Kayes [31]. Employing analytical solutions to Poisson's equation in the radial junction geometry, he found that wire type geometries could tolerate low minority carrier diffusion lengths, but perhaps the most surprising insight was found in a much larger optimal size scale than typically explored by others in the nanowire community, with radii on the order of 1-1.5 μm versus 100-300 nm [15, 35, 36]. Due to the very small volumes of semiconductor materials in these structures, wires with smaller radii are much more sensitive to variations in doping density; in extreme cases, errors in doping density can lead to a fully depleted wire with disastrous

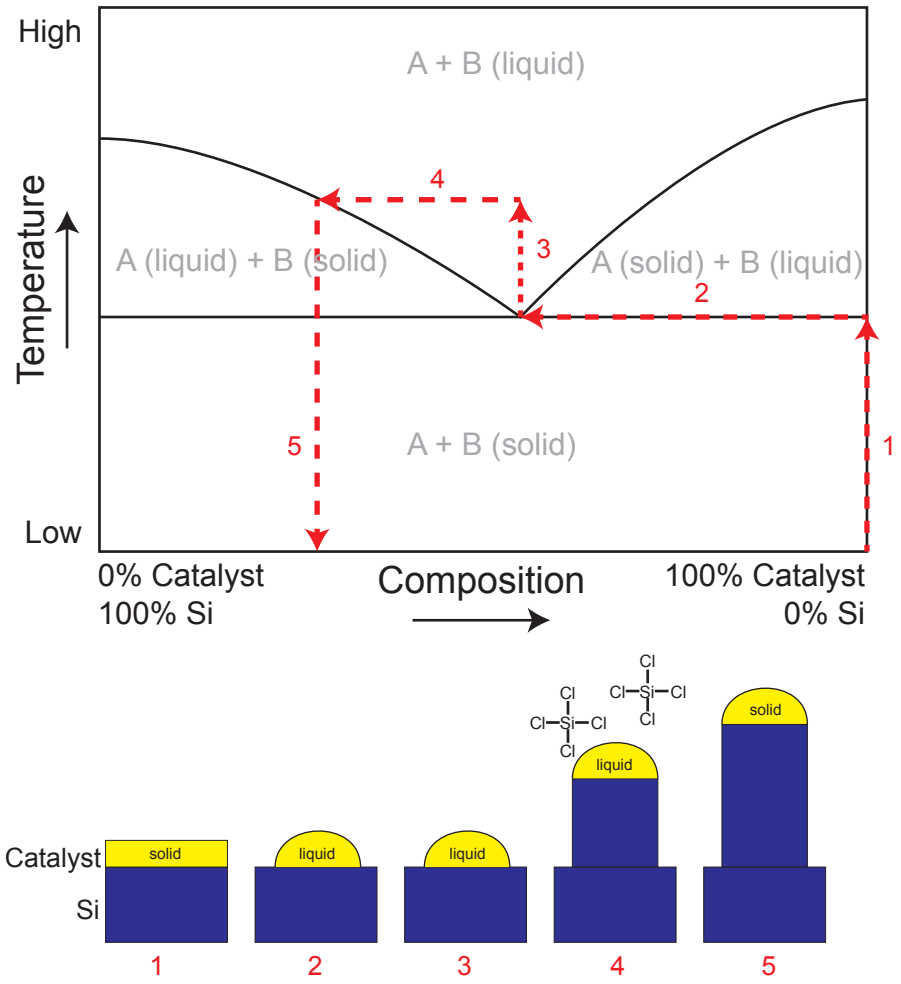


FIGURE 2.3: Schematic of vapor-liquid-solid growth on a typical eutectic phase diagram.

effects on carrier transport. Experimental work in realizing ensembles of wires culminated in lithographically patterned arrays of Au and Cu-catalyzed Si wires grown at atmospheric pressure with silicon tetrachloride in H_2 ambient with a hot wall, home-built CVD at 1000 °C [32]. Furthermore, after infilling the wire arrays with polymeric material it was possible to use a razor blade to "peel" the wires from the wafer surface [66]. After peel-off, the arrays were decoupled from the wafer in a flexible membrane, and the substrate could be reused for further wire array growth [81].

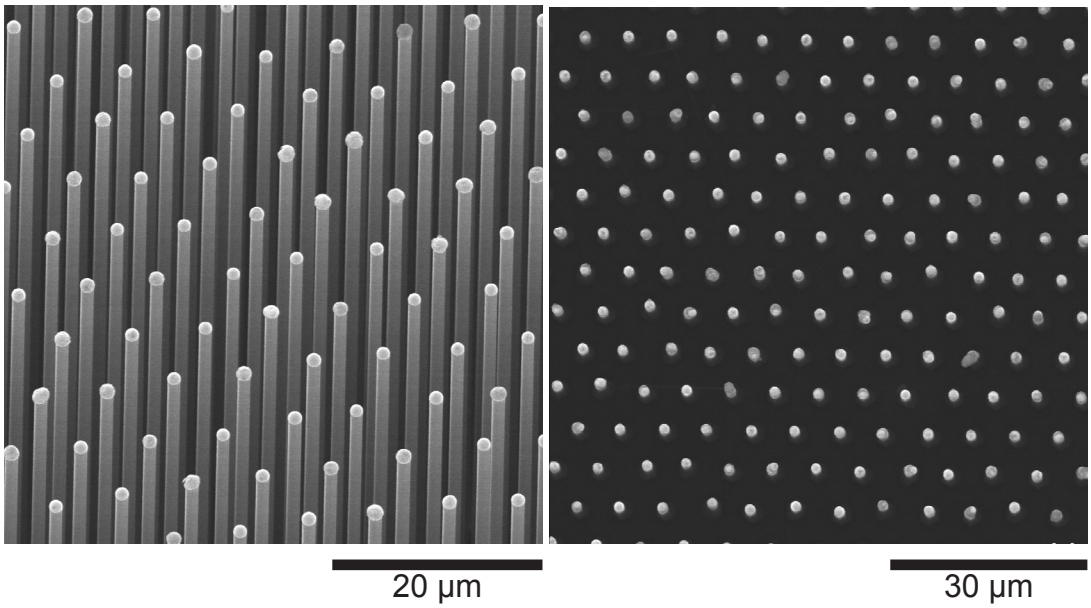


FIGURE 2.4: SEM images of a Si microwire array viewed from 30°off normal incidence (left) and from normal incidence (right).

After these initial successes, silicon microwire arrays became the foundation of several dissertations in the area of photovoltaic and photoelectrochemical devices. The highly ordered nature of the wire arrays coupled with their near-wavelength scale feature size makes them fantastic optical absorbers, which lends itself well to both applications. Dr. Michael Kelzenberg performed a thorough experimental study of the optical properties of the wire arrays and compared them to full-wave finite-difference time-domain (FDTD) simulations of the wire array, where he found that wire array exceeded the $4n^2$ limit in the infrared [33]. The limits of photovoltaic performance were explored experimentally with single wires by Dr. Kelzenberg [34] and in small ensembles of wires by Dr. Morgan Putnam [69], where the experimentally demonstrated limits of efficiency were 17% and 8%, respectively. Large area growth on 6" wafer substrates was also demonstrated, an initial step towards mass production of Si microwire material (see Appendix A).

To further extend the possibilities afforded by microwire arrays in photovoltaics, my thesis work has focused on making devices more efficient by enabling the growth of SiGe alloys. We

investigated growing $Si_{1-x}Ge_x$ alloys with silicon and germanium tetrachloride. Our goal was to achieve full tunability across the entirety of the materials system, thereby enabling near lattice matched tandem device growth for detailed balance efficiencies exceeding 40%. While we fell short of this goal, our results yield a temperature and process window in which the highly ordered array geometry can be achieved with Ge content up to 12%. Furthermore, we identify the catalyst as a reservoir in Ge-rich gas phase compositions.

2.2 SiGe microwire array growth

$Si_{1-x}Ge_x$ microwire arrays could serve as the basis for increasing the intrinsic efficiency potential of wire array solar cells. Higher efficiencies can be achieved by introducing a high bandgap top cell material onto the wires to create a tandem device. The Group III-V compound semiconductor alloys are ideally suited for such an application, but alloys with the ideal 1.7 eV bandgap are heavily lattice mismatched with respect to Si, making the growth of such materials quite challenging. A $Si_{1-x}Ge_x$ bottom cell would allow for high theoretical efficiencies ($> 40\%$) with minimal lattice mismatch when paired with a $GaAs_yP_{1-y}$ top cell (Figure 2.5). Realizing these tandem devices requires both the development of the SiGe wire array bottom cell and the Group III-V compound semiconductor top cell, which will be covered in Chapter 3. Optoelectronic simulation assisted design of wire array tandem cells will be discussed in Chapter 4. Realizing SiGe wire array growth requires a suitable catalyst and catalyst for the VLS growth process.

2.2.1 Prior work on SiGe nanowires

SiGe nanowires have been of particular interest for the ability to independently tune composition and size [2]. A majority of the existing work in the literature has been focused on vapor-liquid-solid growth of $Si_{1-x}Ge_x$ nanowires using silane and germane precursors with Au catalysts at low pressures [27, 30, 42, 44, 45, 70, 98], and full compositional control has

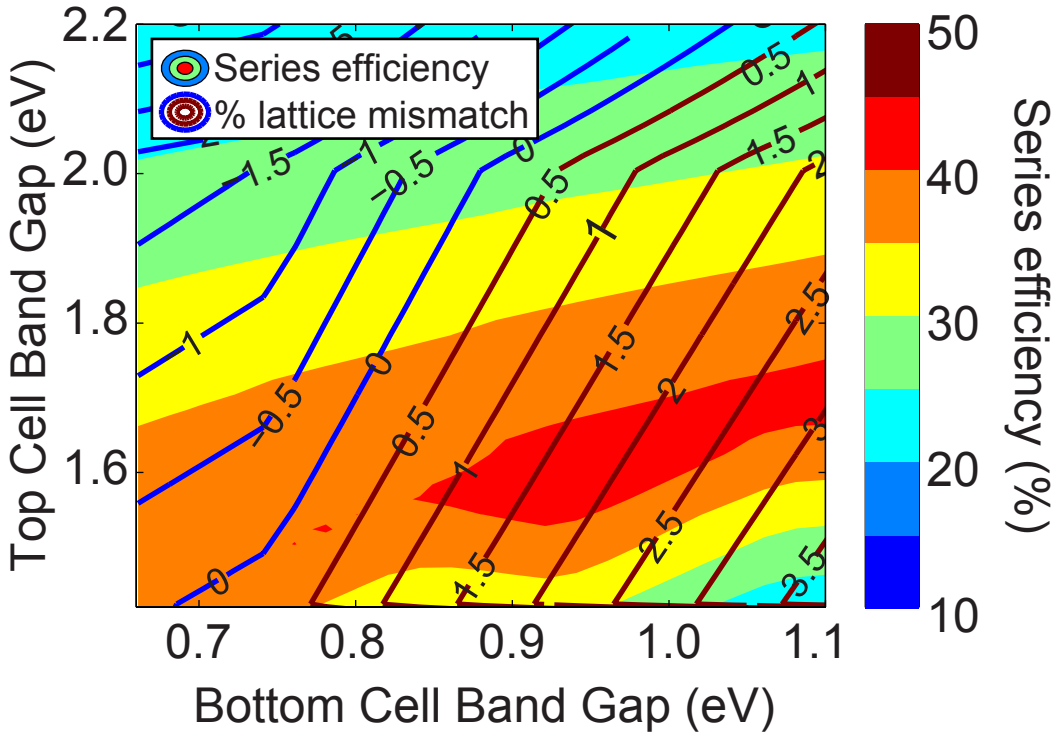


FIGURE 2.5: Lattice mismatch of a $GaAs_{1-y}P_y/Si_{1-x}Ge_x$ tandem overlaid on detailed balance efficiency under AM1.5G illumination. Detailed balance calculations performed by Emily Warmann.

been demonstrated [18, 42]. Significant progress has been made in the development of axial [16, 93] and radial heterostructures with sharp interfaces. In contrast to much of the existing work, atmospheric pressure Cu-catalyzed vapor-liquid-solid growth with tetrachlorosilane has been shown to generate vertically aligned, monodisperse arrays of microwires with micron scale diameters and heights. However, retaining the benefits of Cu versus Au catalyst has implications on the thermodynamics of VLS growth.

2.2.2 Catalyst selection

Au is typically the catalyst metal of choice for VLS growth due to the lack of secondary phases with a most materials, which which Si [58] and Ge [59] are good examples. In contrast, Cu has several secondary phases in its phase diagram with Si [60]. However, this has not been shown to be an issue in the growth of wire arrays with Cu catalysts. Ge growth also looks like it is possible for Cu catalysts, with a similarly complicated phase diagram [61]. However, one issue that stands out is the difference in eutectic temperature for Cu-Si versus Cu-Ge at 802 °C and 640 °C, respectively. This could lead to issues in the driving force for formation of Ge versus Si-rich alloys. There is also a slight difference in the solubility limits of Si and Ge in liquid Cu at 31% and 36%, respectively. However, despite these hurdles to growth with Cu catalyst, Au was never considered due to its extreme effect on electronic properties.

2.2.3 Precursor selection

Finally, the choice of Ge precursor was made for $GeCl_4$, as it has decomposition temperatures more similar to $SiCl_4$ than GeH_4. No recent work using $GeCl_4$ has been reported for SiGe nanowire growth, although it was one of the first "whisker" growth precursors [19]. Soman *et al.* found that in thin film growth contamination from adventitious Ge species on reactor surfaces made growth with $GeCl_4$ less reproducible than GeH_4 [80]. This presented problems during experimental realization of SiGe microwire arrays.

2.2.4 Experimental approach

We prepared high purity (6N, Alfa Aesar) Cu-catalyst decorated Si (111) substrates using standard photolithographic liftoff processes as described earlier (see Section A.1.1). Substrates were cleaved into 1 × 1 cm pieces and loaded onto a quartz boat, which was then inserted into the CVD tube at 750 °C with N_2 flow. The "Big Blue" system was then

evacuated and refilled with research grade H_2 up to just above atmospheric pressure before opening the exhaust valve to the scrubber. The CVD tube was then heated to 1000 °C under H_2 flow and allowed to reach thermal equilibrium before precursor introduction. Typical growth parameters include 1 slm of H_2 carrier gas, bubbled H_2 carrier gas through a nominally 32 °C $GeCl_4$ cylinder, and collection of the overpressure from a $SiCl_4$ cylinder heated to 85 °C. These values correspond to molar flow rates of 0-98 μmol min^{-1} $GeCl_4$, 430 μmol min^{-1} $SiCl_4$, and 4×10^4 μmol min^{-1} H_2. After growth, samples were cooled slowly to 750 °C inside the tube with an H_2 purge during the initial stage of the cool transitioning to a N_2 purge. The tube was then evacuated and refilled with N_2 before being pulled out of the hot zone of the CVD furnace for a faster cool to near room temperature.

As the conditions for growing high fidelity, high Ge content SiGe microwire arrays lie in a fairly large phase space, we decided to split the problem into two separate approaches. Dr. Daniel Turner-Evans focused on pure Ge wire array growth on Si and Ge substrates, and his results are reported in his thesis [85]. Our approach was to start with good Si wire array growth conditions and to slowly introduce Ge. Best results were obtained by starting with the reactor in a state which produces high fidelity Si microwire arrays before slowly increasing the amount of $GeCl_4$ flow from run to run. The quality of the wire array growth was evaluated first by eye and then by using the Hitachi S-4100 FE-SEM tool. Growth proceeded iteratively using feedback from the previous run before steady state conditions were reached. Periodically, wire array growth would become highly disordered (Figure 2.6), which we attribute to sidewall deposition of Ge containing species [80]. This behavior could be rectified by coating the inside of the reactor with silicon by doing multiple silicon wire array growths. Similar behavior was also found by cleaning the tube with anhydrous HCl gas at 1100 °C under nitrogen flow.

High resolution SEM imaging was done on an FEI Nova 200 dual beam SEM/FIB system by first aligning to the growth axis and then tilting to 30° off normal incidence. Energy dispersive spectroscopy (EDS) was also performed to measure composition using an Ametek

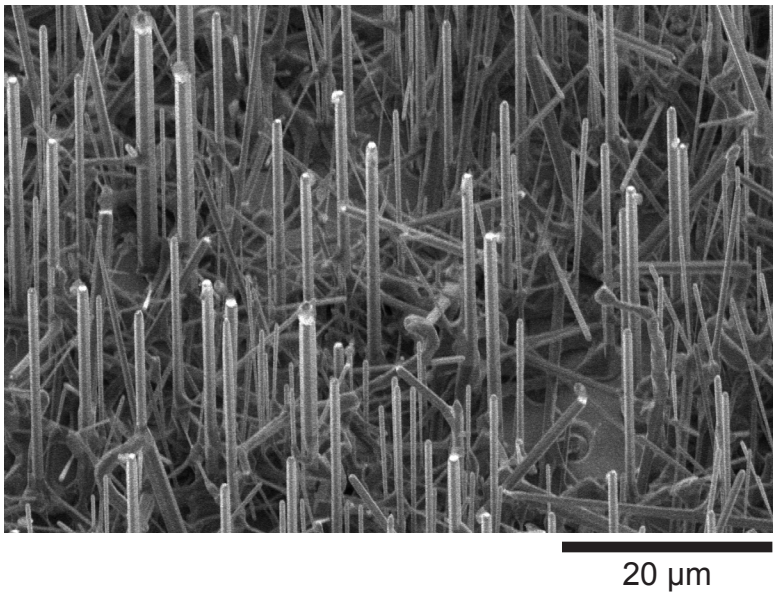


FIGURE 2.6: SEM micrograph of disordered SiGe microwire array growth resulting from air introduced through a leak in the reactor or tube contamination by Ge containing species.

EDAX Genesis 7000 with a sapphire detector. High resolution x-ray diffractometry was performed on a Panalytical X'Pert Pro, with a hybrid x-ray mirror/2-bounce monochromator and a 3 × 220 Ge analyzer with a sealed Xe proportional detector. Reciprocal space maps were collected after first aligning to the (111) or (153) peak of the Si substrate. Relaxation was calculated using the methodology of Zhylik *et al.* [99] (described in Appendix B) and comparing the calculated composition to the composition measured using EDS. Electron transparent radial and axial cross sections of single wires were prepared using standard focused ion beam milling techniques in either a FEI Nova 600 or FEI Versa 3D dual beam system as described in Appendix C. TEM characterization in this work was done on a JEOL 2100-F 200 kV FE-TEM and a FEI Technai TF30UT 300 kV FE-TEM.

2.3 SiGe microwire morphology and composition

In general, as the flow of $GeCl_4$ was increased, the morphology of the wires began to develop a tapered geometry (Figure 2.7). At low $GeCl_4$ flow rates, the wire arrays appear to be very similar to their pure Si counterparts, and a close look reveals the introduction of small inwards sloping facets parallel to the growth front and perpendicular to the growth direction. At relatively high $GeCl_4$ flow rates, the wires are very heavily tapered, with significant faceting on the sidewalls of the wires parallel to the growth front. As expected, the Ge content of the wire arrays increase with increasing Ge flow. The calculated gas phase composition ([Ge]/[IV]) is always greater than that of the resulting wire array. The difference could be the result of differences between the reactivity of chlorogermane and chlorosilane on the catalyst or the sidewalls, leading to differences in the supersaturated catalyst or gas phase compositions, respectively. The growth rate also changes dramatically, falling from 7 μm min^{-1} to 1 μm min^{-1} as Ge molar flow fraction was increased to 18.6% (Figure 2.8). In fact, attempts to grow with a gas phase Ge molar fraction of 25.7% resulted in little to no growth (Figure 2.9). The changes in morphology and growth rate were unexpected and became a significant focus of our investigation.

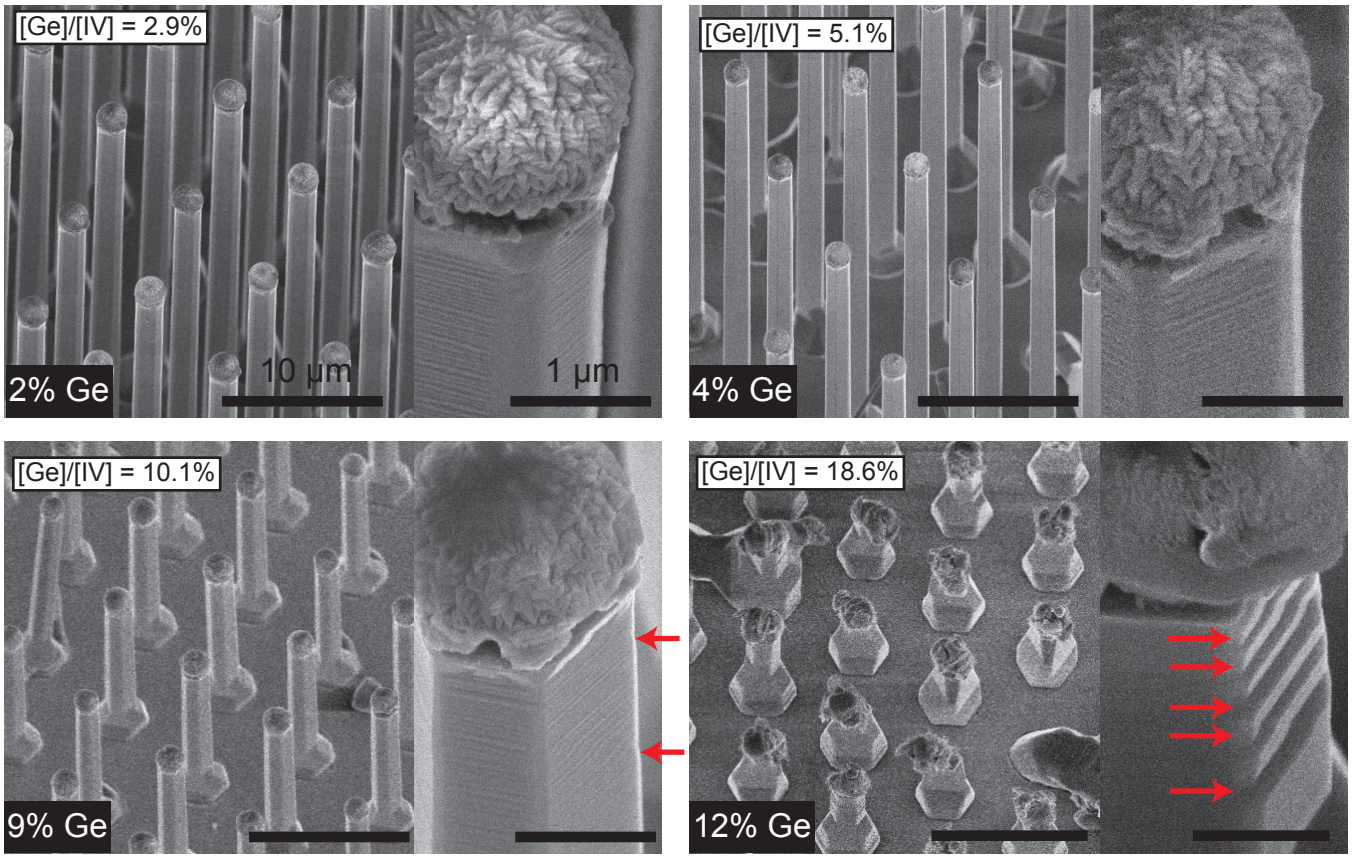


FIGURE 2.7: Scanning electron micrographs of $Si_{1-x}Ge_x$ wire arrays grown with increasing $GeCl_4$ flow rates and constant $SiCl_4$ flow for 10 minutes. The growth rate drops from 7 μm min^{-1} at the lowest to 1 μm min^{-1} at the highest [Ge]/[IV] ratio. Inward sidewall facets are marked with red arrows. SEM images collected by Hal Emmer.

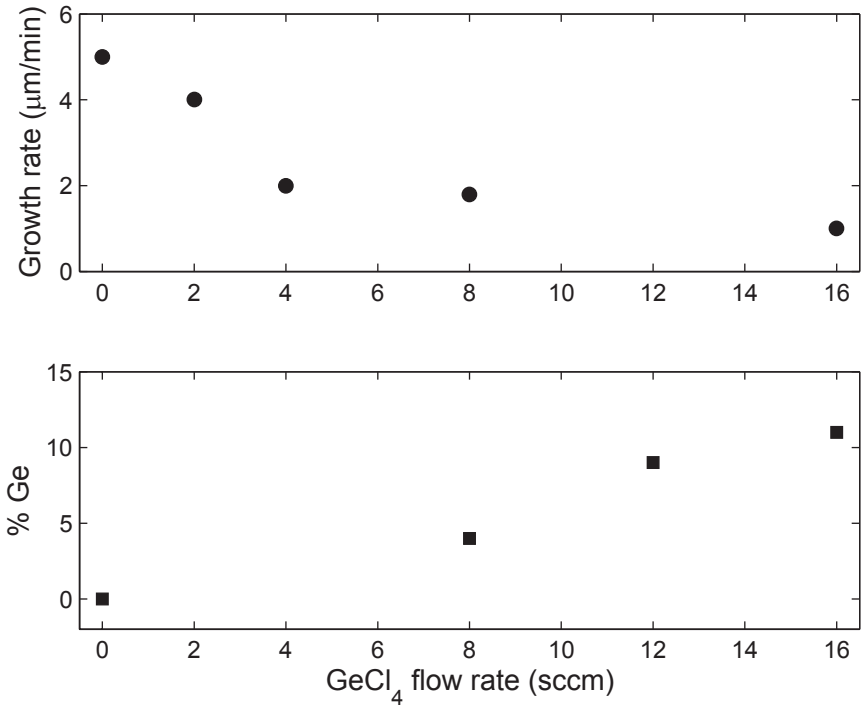


FIGURE 2.8: Growth rate and Ge content as a function $GeCl_4$ flow.

As the growth time is increased at [Ge]/[IV] = 18.6%, tapering of the wire continues with large sidewall facets oriented perpendicular to the growth direction along the length of the wire and a clear reduction in the volume of the catalyst particle (Figure 2.10). Despite the tapering, the wires can be grown to 60 μm in height, which has been shown by Kelzenberg *et al.* [33] to be necessary for full absorption of the solar spectrum.

Reports of Si and SiGe tapered nanowire growth have attributed tapered wires to undesired sidewall deposition [44, 68] and in-situ etching of the metal catalyst [44, 63]. Hannon *et al.* observed similar faceting in Si nanowires after introducing a growth interruption, which they attributed to catalyst migration between the first and second growth phase [25]. Pure Si microwire arrays were grown at elevated temperatures of 1050 °C and 1100 °C to encourage etching and evaporation of the catalyst during the growth process. The resulting wire arrays had morphologies, depicted in Figure 2.11, were more or less identical to those observed

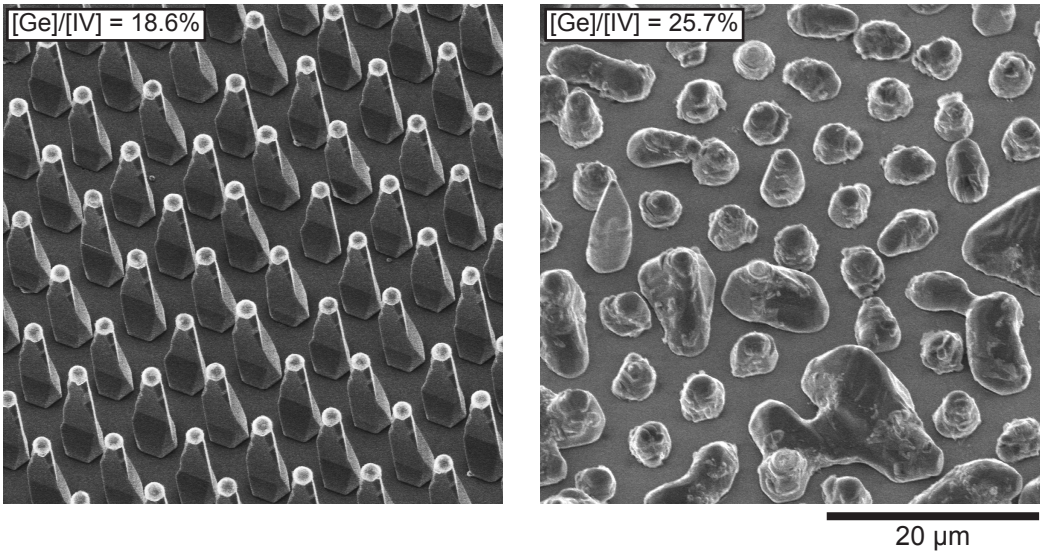


FIGURE 2.9: Scanning electron micrographs of SiGe microwire arrays grown with [Ge]/[IV] = 18.6% (left) and 25.7% (right).

for the SiGe wire arrays, which is clear evidence of increased catalyst removal with higher $GeCl_4$ flow rates.

The sidewall faceting likely results from competing energetics when catalyst material is removed; cylindrical growth is normally stable [56], but the catalyst size, and therefore shape, is perturbed until it is energetically favorable for the catalyst diameter to reduce, returning to the preferred shape while creating non-vertical solid wire surfaces. A similar effect is likely responsible for the wide wire bases, due to the difference in the surface energy between the catalyst particle and the SiO_2 growth mask during initiation compared to the vapor environment during growth. Step by step, our proposed mechanism for the wire faceting is depicted in Figure 2.12 and proceeds as follows:

1. Stable vertical growth proceeds with a well defined catalyst droplet contact angle.

2. Catalyst removal reduces droplet volume, leading to a change in the contact angle and an eventual depinning of the triple junction edge when a critical value is reached.

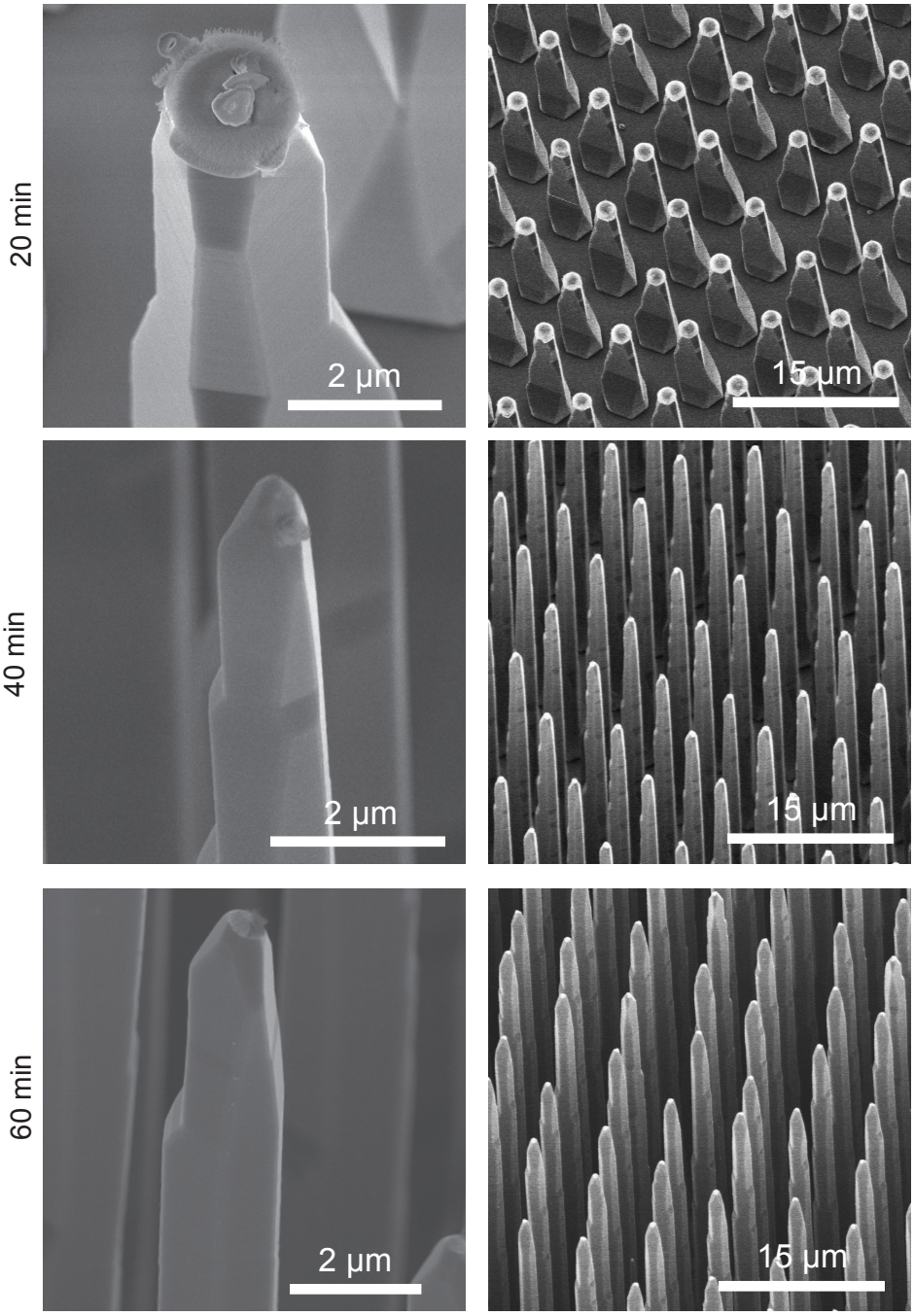


FIGURE 2.10: Wire arrays grown at [Ge]/[IV] = 18.6% for an extended period of time as imaged with scanning electron microscopy. The wires have a highly faceted, tapered morphology that persists over long growth times with minimal catalyst volume left after longer growth times. SEM images collected by Hal Emmer.

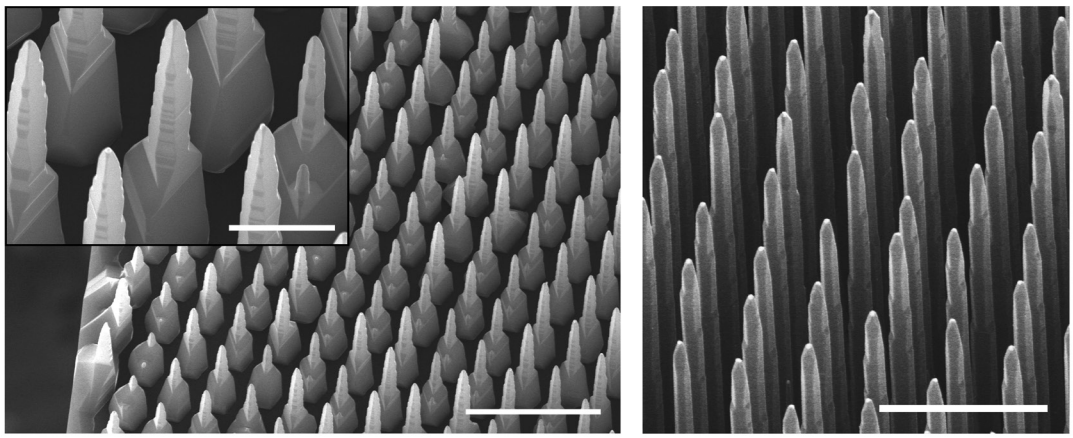


FIGURE 2.11: Morphological comparison of Si wires grown at elevated temperatures (left) and SiGe wire arrays (right). SEM images collected by Hal Emmer.

3. Unstable triple junction edge changes conformation while growth proceeds, leaving the inwards sloping facet.

4. Stable contact angle is reached and the triple junction stabilizes.

5. Vertical growth proceeds until catalyst removal induces another conformational change.

Reducing the $Si_{1-x}Ge_x$ growth temperature to 950 °C was also attempted, and resulted in a large increase in disordered growth compared to perfect, vertical wire array growth, and we could not fairly compare its effects on the wire morphology. We attribute this change to decreased HCl sidewall etching. Attempts to grow pure Ge microwire arrays with Au and Cu catalysts at lower temperatures (800 °C) resulted in similarly disordered growths [85].

2.4 Crystallographic orientation

XRD is a powerful materials characterization tool that allows us to interrogate the crystallographic alignment of the wire array relative to that of the host Si (111) substrate. The large area of the x-ray beam as compared to the sample interrogates a large fraction of the wires

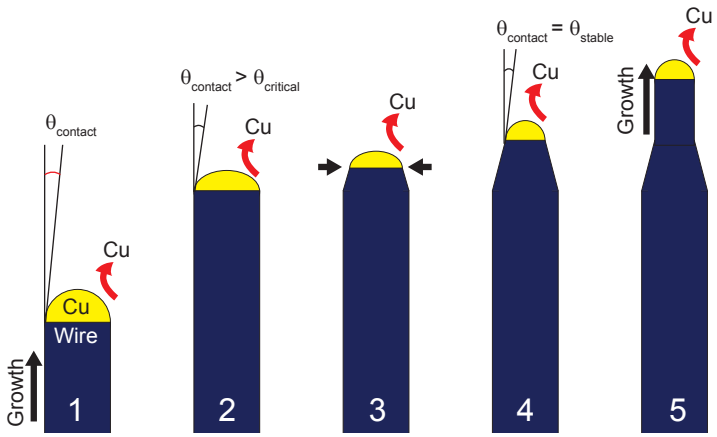


FIGURE 2.12: Schematic of inward sidewall facet formation mechanism. Removal of the material from the catalyst is assumed throughout and labeled with a red arrow. Vertical wire growth proceeds with some contact angle (1), becomes unstable after removal of enough catalyst (2), unpins the triple junction while vertical growth continues (3) before reaching a new equilibrium (4) where vertical growth proceeds (5) until the process repeats.

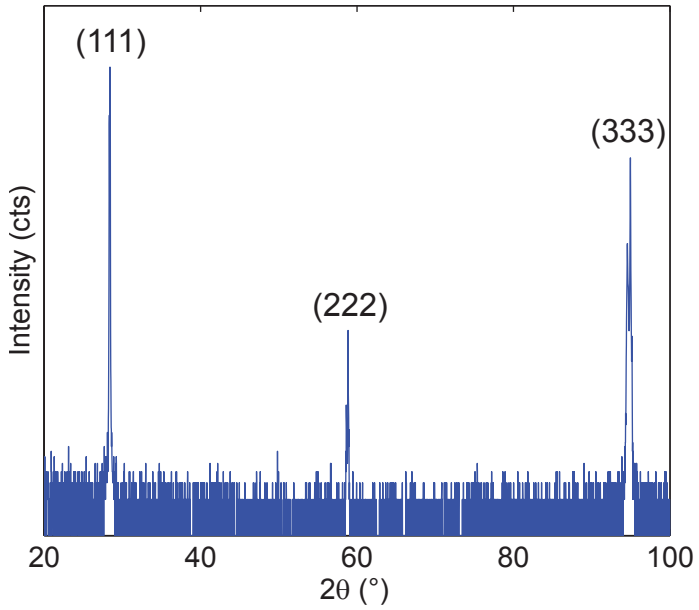


FIGURE 2.13: Representative XRD spectrum of SiGe wire arrays showing crystallographically oriented growth matching the Si(111) growth substrate. Intensity is plotted on a logarithmic scale.

on any given sample. As found with their pure Si wire array counterparts, the SiGe wire arrays are single phase and aligned epitaxially with the growth substrate (a representative x-ray spectrum is shown in Figure 2.13).

In mismatched epitaxial growth, the epilayer typically grows initially as a strained layer on top of the host substrate material. As growth proceeds, the strain energy eventually exceeds the energy required to nucleate strain relieving defects in the crystal lattice in the form of dislocations. Wire-type structures have been found to allow stress relief by their radial geometry; since the wire is not constrained by the crystal lattice of the substrate or other epitaxially grown materials, it can relieve strain radially without the formation of dislocations or other defects. However, this effect has been primarily explored in the realm of nanoscale structures, and even they are not immune to the formation of other undesirable defects, such as phase separation [54]. Thus, it is of import to determine the mechanism of strain relief in the SiGe wire arrays.

Clear shifts in the 2θ-ω rocking curves of the (333) peaks can be seen as the gas phase Ge composition is increased (Figure 2.14). In fact, by cross comparing the composition of the wire arrays measured using EDS to the composition we expect from the position of the layer peak, we find that these values match, and from this we can infer that the wires are fully relaxed. However, this is by no means a fullproof derivation of the strain state, and further investigation with the measurement of asymmetric peaks is necessary to prove full relaxation. Furthermore, we see evidence of a second peak at lower 2θ values indicative of a Ge-rich phase.

2.4.1 Relaxation and crystallographic defects

In general, determination of the strain state and relaxation of an epitaxial material can be done by measuring the peak positions of asymmetric peaks, which contain information about the out-of-plane and in-plane lattice constants. For substrates grown on a (111) orientation, the (135) family of peaks gives in-plane lattice constant information about

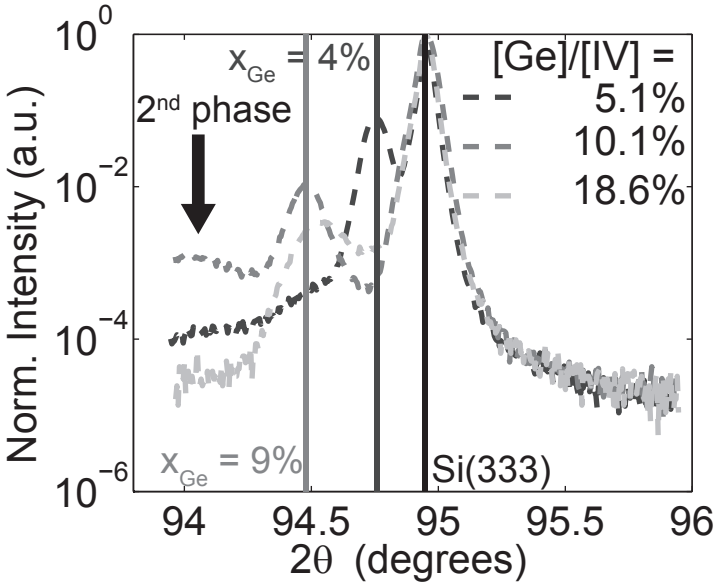


FIGURE 2.14: Three XRD 2θ-ω rocking curves of the (333) peaks of the Si substrate and the SiGe wires plotted with intensity normalized to the substrate peak.

the six equivalent [110] surface parallel directions. This, however, would require six full reciprocal space maps for a single sample, which is intractable on the Panalytical X'Pert Pro diffractometer. Instead, a single peak position at (153) was taken to provide a partial estimation of the strain state of the system. A representative set of reciprocal space maps are provided in Figure 2.15. To aid in interpretation of the data, the wire array chosen does not have a lower intensity, higher Ge-content peak. The peak positions from the asymmetrical scan were then used to compute the relaxation of the film (see Appendix B for details). All of the wire arrays measured in this way were found to be fully relaxed. To attempt to determine the mechanism of strain relief, single wires were processed into electron-transparent cross sections for characterization in the TEM.

TEM imaging of radial and axial cross sections taken along the length of a single $Si_{0.91}Ge_{0.09}$ wire seen in Figure 2.16 are single crystalline and phase pure, consistent with the x-ray diffraction measurements. Pure Si nano- and microwires have been observed to be hexagonal or dodecagonal, corresponding to a combination of (110) and (112) facets [71, 96].

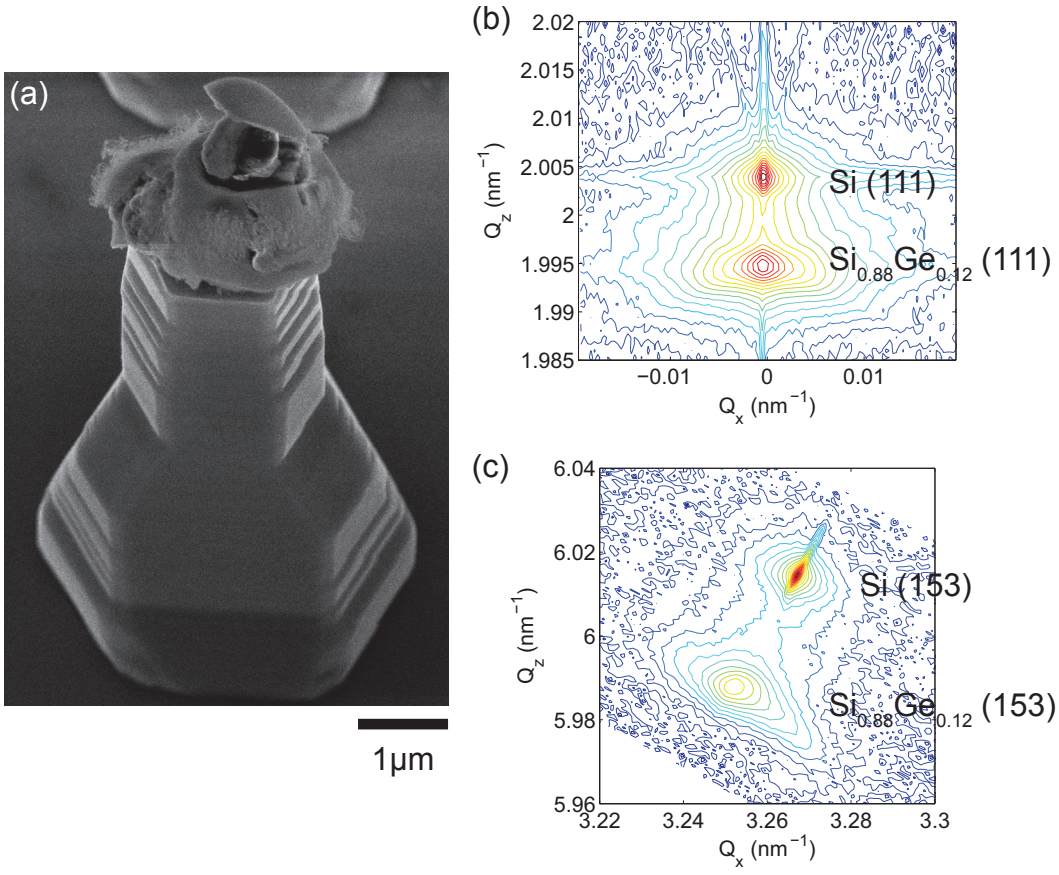


FIGURE 2.15: Reciprocal space mapping of a $Si_{0.88}Ge_{0.12}$ wire array. (a) Scanning electron micrograph of a single wire on the substrate viewed from 30°off normal incidence. RSM's of (b) symmetric (111) and (c) asymmetric (153) layer and substrate peaks

By comparing the selected area diffraction pattern and transmission electron microscopy images, the radial facets along the length of a single $Si_{0.91}Ge_{0.09}$ wire can also be indexed to the (110) and (112) directions. The difference in symmetry implies that the introduction of $GeCl_4$ changes the surface energy of the facets enough to cause significant changes from pure Si wire growth.

Importantly, we observed no evidence of crystalline defects in the bulk of the wires which could result from strain relief, suggesting that the strain relieves outward from the substrate

axis since the wires present traction-free surfaces in these directions. Furthermore, we observed no evidence of stacking fault or twin formation associated with the surface faceting [73]. Axial cross sections along the length of wires with and without an observed Ge-rich phase in x-ray diffraction were also defect free and phase pure, without any evidence of sidewall epitaxy.

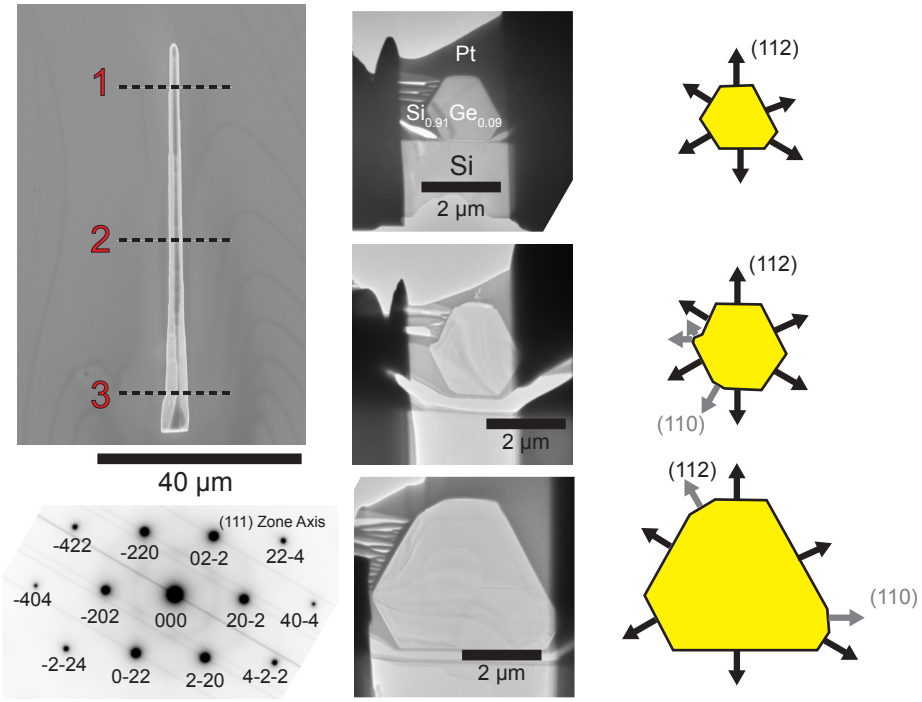


FIGURE 2.16: Radial cross sections along the length of a single $Si_{0.91}Ge_{0.09}$ wire were characterized with transmission electron microscopy. Left - Scanning electron micrograph of wire with dashed lines overlaid on approximate radial cross section locations above a representative SAD pattern. Center - TEM of each radial cross section. Right - corresponding schematics of indexed sidewall facets below. TEM data collected by Dr. Shaul Aloni.

2.4.2 Determining the origin of the Ge-rich phase

The bulk crystallinity and phase purity of the wire arrays were characterized with x-ray diffraction. All wire arrays are epitaxial with respect to the substrate, but in some cases

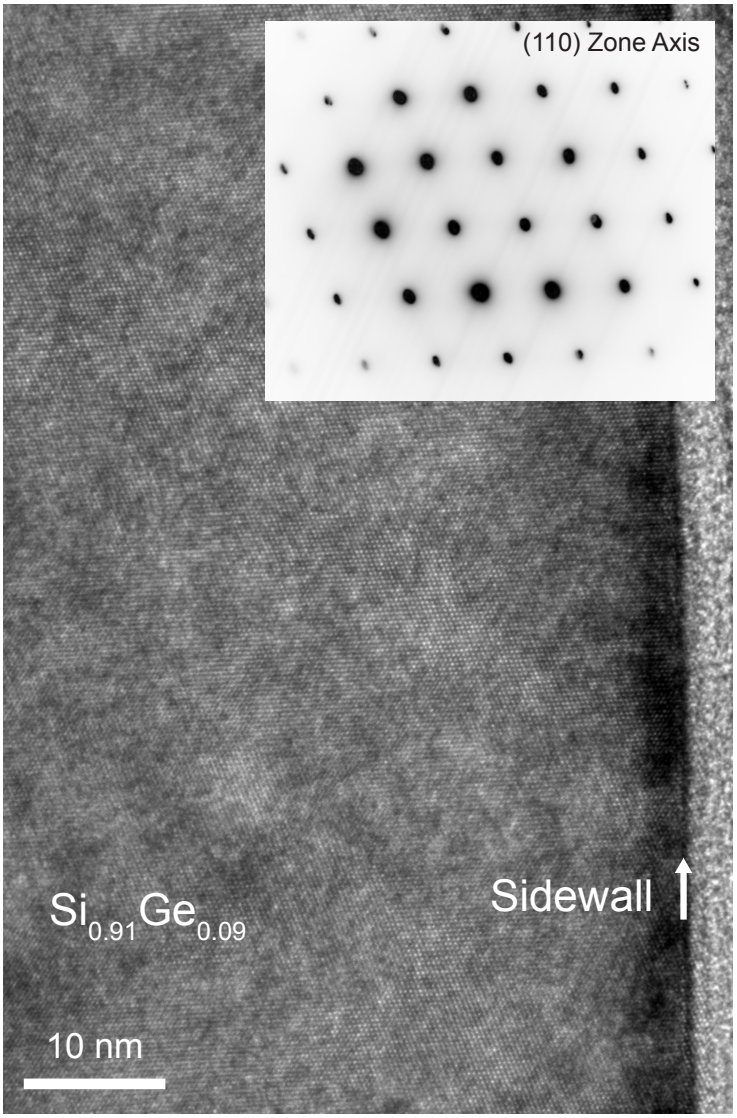


FIGURE 2.17: Axial cross section of a second $Si_{0.91}Ge_{0.09}$ wire sidewall and a corresponding selected area diffraction pattern. The arrow marks the location of the wire sidewall and is oriented in the [111] growth direction. Contrast at the sidewall is likely an artifact of FIB milling. TEM image collected by Dr. Shaul Aloni.

multiple $Si_{1-x}Ge_x$ phases are observed. Two representative reciprocal space maps of wire arrays are presented in Figure 2.18. The reciprocal space map of the symmetric (111) peak of the highly tapered $Si_0.91Ge_{0.09}$ wires indicates the wires are single phase and epitaxial with respect to the Si (111) substrate (Figure 2.18a). A partial determination of the strain state of the $Si_0.91Ge_{0.09}$ wire array using the symmetrical (111) and asymmetrical (135) peak positions shows that the wires are fully relaxed. In the second case, the shorter $Si_{0.9}Ge_{0.1}$ wire array appears to have some residual Cu catalyst, and the reciprocal space map indicates a second phase with significantly higher Ge content at much lower intensity (Figure 2.18b). While the dominant Si-rich phase is fully relaxed, the strain state of the Ge-rich phase could not be determined due to the low contribution to the diffracted signal. Overall, the presence of a Ge-rich phase did not correspond to any specific growth conditions or morphological features. To investigate the origin of this effect, cross sections of individual wires were prepared and characterized with transmission electron microscopy.

However, closer examination of the wire tips reveals the presence of a region which is compositionally distinct from the bulk of the wire or the Cu catalyst, regardless of whether the wires appeared to be single phase or double phase in x-ray diffraction measurements (Figure 2.19). The presence of this phase is clearly seen in high angle annular dark field imaging as a region appearing brighter than the bulk of the wire, suggesting significant compositional contrast, and the interface between the two regions appears to be abrupt. Energy-dispersive x-ray spectroscopic mapping of Ge, Si, and Cu reveals significant Ge enrichment in these regions compared to the bulk of the wire, sharp interfaces between the two regions, and no Cu content except beyond the noise level at the catalyst location. Point and area spectra taken from the Ge-rich regions reveal enrichment of up to $Si_{0.43}Ge_{0.57}$ and $Si_{0.22}Ge_{0.78}$ for the single and double phase wires, respectively. These observations imply that the catalyst is Ge-rich during the growth process, and that the second phase forms either after precursor flow has ceased or as the sample is cooled.

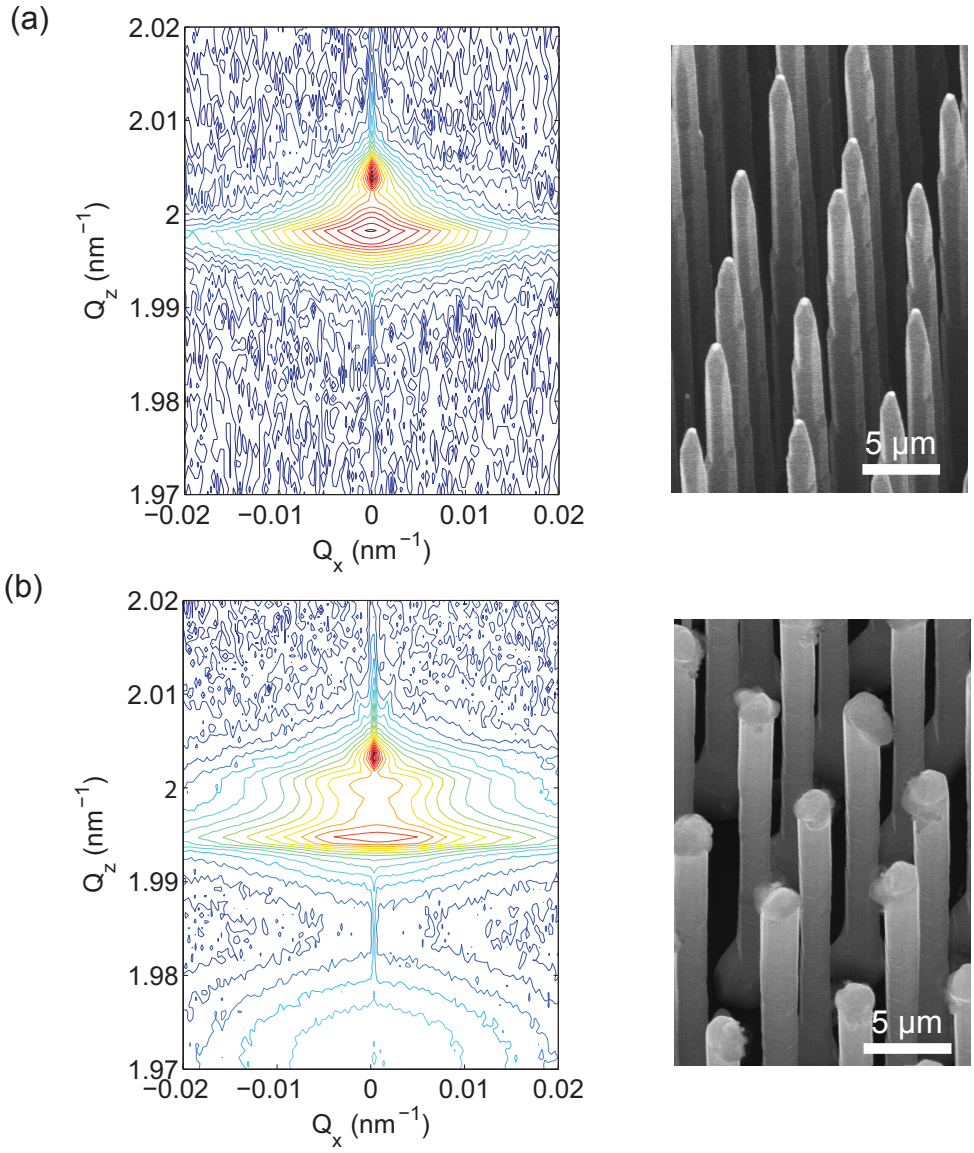


FIGURE 2.18: High resolution x-ray diffraction reciprocal space maps. (a) depicts the symmetric (111) peaks of the $Si_{0.91}Ge_{0.09}$ wire array. This map is qualitatively representative of all single-phase wire arrays. The wires are fully relaxed. (b) depicts the symmetric (111) peaks of a $Si_{0.9}Ge_{0.1}$ wire array with a second $Si_{1-x}Ge_x$ peak at lower intensity and higher Ge content.

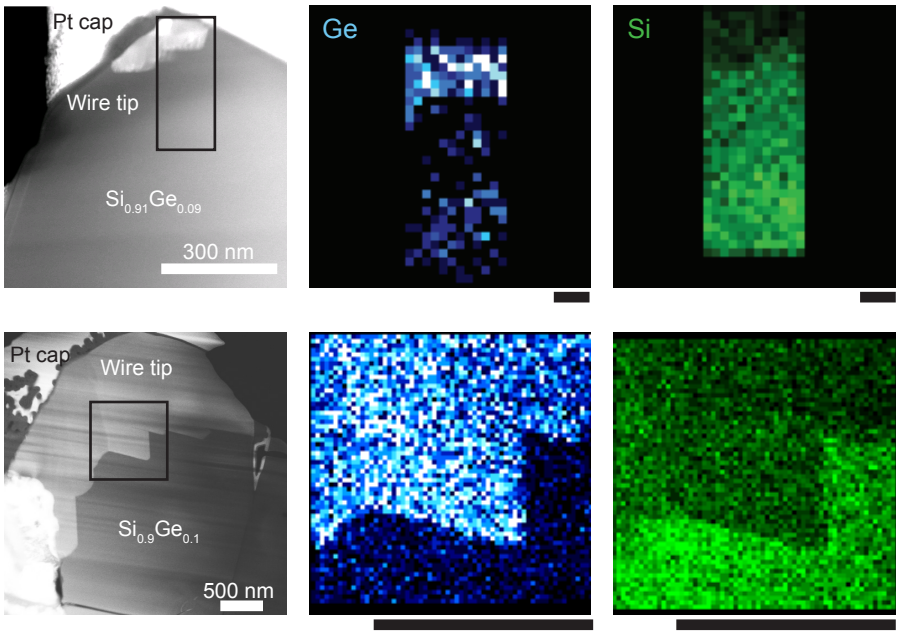


FIGURE 2.19: Axial cross sections of $Si_{0.91}Ge_{0.09}$ (top row) and $Si_{0.9}Ge_{0.1}$ (bottom row) wires representative of the single and double phase wire arrays, respectively. High angle annular dark field images collected with scanning transmission electron microscopy (left) of each of the wire tips reveals clear compositional contrast between the tip and bulk. Energy-dispersive spectroscopic mapping confirms this finding, revealing a Ge-rich crystal nucleating at the very tip of the wire in both cases. Point and area spectra collected in the Ge-rich regions for the single and double phase wires show compositions of $Si_{0.43}Ge_{0.57}$ and $Si_{0.22}Ge_{0.78}$, respectively. Scale bars below each map measure 50 nm.

2.5 Outlook

As discussed earlier, the highest Ge content of 12% was achieved at [Ge]/[IV] = 18.6%, and attempts to grow with [Ge]/[IV] = 25.7% resulted in little to no growth. Our observations, namely the tapering due to catalyst removal with increasing chlorogermane flow and evidence of a Ge-rich catalyst during growth, strongly suggest that $Si_{1-x}Ge_x$ wire arrays are limited to $\leq$ 12% Ge content when grown with Cu catalysts and chlorinated precursors at atmospheric pressure. There are several possible explanations for this. Examination of the Cu-Si and Cu-Ge phase diagrams shows a large difference in eutectic temperature (802 °C vs. 640 °C) and a small difference in the solubility of Si and Ge in liquid Cu (31% vs. 36%),

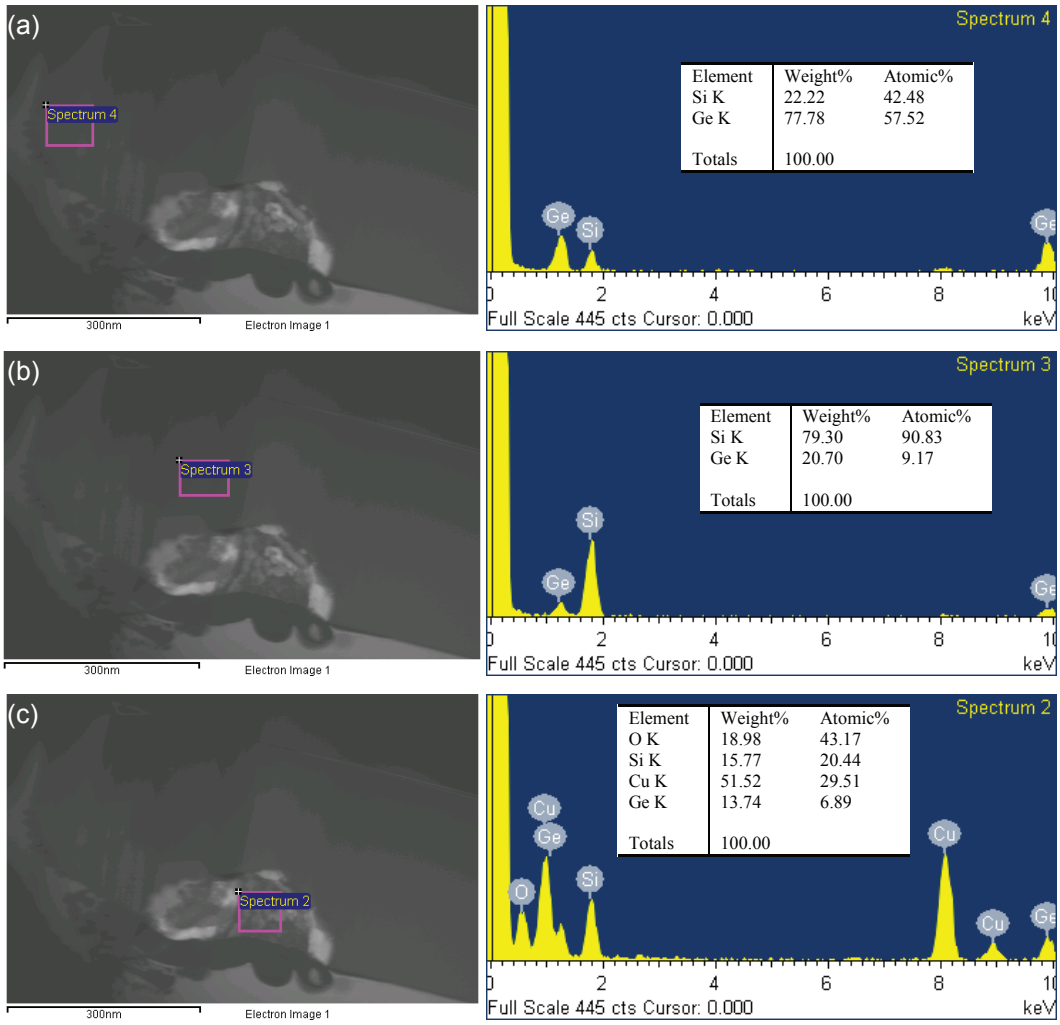


FIGURE 2.20: EDAX spectra from select regions of the double phase $Si_{0.9}Ge_{0.1}$ wire.

both of which could play a role in the enrichment of the Cu catalyst and the reduction in growth rate due to a smaller driving force for nucleation of Ge-rich versus Si-rich alloys. While both of these issues could be mitigated by moving to Au catalyst, the minority carrier lifetime of the wire material would suffer [6, 26]. Furthermore, at growth temperatures, the liquid catalyst droplet is saturated with Si before precursors are introduced because it is in direct contact with the Si substrate, which favors initial Si-rich supersaturation. Reducing the $SiCl_4$ flow rate while keeping the $GeCl_4$ flow rate constant did not result in higher

compositional content. Once growth begins, the strain energy of nucleating alloy material with increased Ge content may also play a key role in preventing higher Ge incorporation as the size of the wires leads to their strain relief behavior being more bulk-like. This would explain the Ge enrichment of the catalyst compared to the growing solid wire material. All in all, the thermodynamic limitations of growing with a Cu catalyst likely represents a fundamental limit to the growth of $Si_{1-x}Ge_x$ alloy microwires.

Hal Emmer performed initial electronic characterization on a sample with approximately 10% Ge content, doped in-situ with a 4 SCCM flow of 0.25% BCl_3 diluted in H_2. BCl_3 does not induce sidewall epitaxy in the growth of Cu-catalyzed Si or SiGe microwire arrays grown with $SiCl_4$ and $GeCl_4$, unlike what has been reported for diborane in Au-catalyzed SiGe nanowire growth [63, 65]. This dopant flow yields resistivities of 0.1 Ω-cm in pure silicon wires. Four point probe measurements on this sample yielded a resistivity of 18.7 ± 4.3 Ω-cm, implying a lower level of doping than for growth of pure silicon microwires.

All in all, the efforts in wire arrays have yielded results suggesting that efficiencies of up to 17% are possible with the wire array devices [34]. While this may have been an interesting number in 2007 (or to a limited extent in 2009), the prevalence of cheap, high lifetime silicon wafers has made competing with silicon a very difficult proposition. However, wire arrays still possess fascinating optical properties, making them ripe for further study as analogues to material with high surface area to volume ratio and high lifetime. Another fruitful avenue of study lies in fabricating high lifetime wire arrays by using top-down etching techniques, an effort which has already begun in earnest.

Chapter 3

Group III-V compound semiconductor growth on Si microwire arrays

3.1 Background

As mentioned earlier, the goal of this work is to enable a high efficiency, Group III-V compound semiconductor top cell on a Si or SiGe bottom cell. In lieu of a high Ge content SiGe wire array substrate, our focus changed from lattice matched growth to lattice mismatched growth. Furthermore, the limitations of the MOCVD reactor makes growing $GaAs_{1-y}P_y$, which would be 2% lattice mismatched to a SiGe bottom cell, impossible. Instead, $Ga_yIn_{1-y}P$ must be used, which requires 5% lattice mismatch for the ideal 1.7 eV top cell bandgap (Figure 3.1).

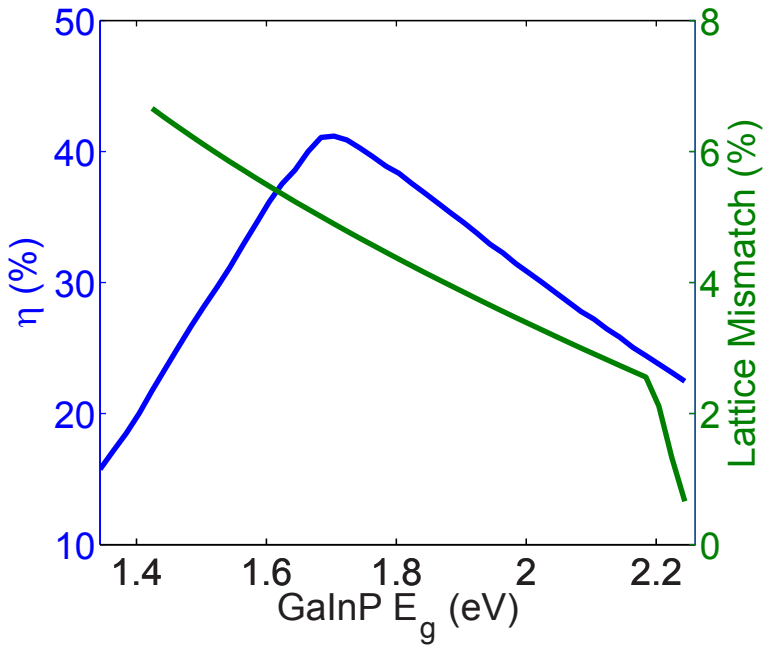


FIGURE 3.1: Predicted detailed balance efficiency (left) and lattice mismatch (right) of a $Ga_{1-y}In_yP$/Si tandem as a function of top cell band gap under AM1.5G illumination. Detailed balance calculations performed by Emily Warmann.

3.1.1 Accomodating lattice mismatch

This extreme lattice mismatch must be relaxed in the structures as they are being grown. The "metamorphic" approach used in high efficiency multijunction solar cells accomodates the relaxation of this strain energy by growing discrete layers with a well defined compositional or lattice mismatch difference relative to the layers below it. Careful design of the the grading layer composition and thicknesses allows for full relaxation by slowly introducing mismatch and threading dislocations and allowing them to glide and annihilate at free surfaces (Figure 3.2a). For example, the offcut and polarity of III-V wafers impacts the velocity of dislocation glide in the GaInP alloys, allowing for the efficient relaxation of strain until the alloy becomes InP-like. At this point, a buffer can be engineered with thicker layers in light of the slower relaxation rate.

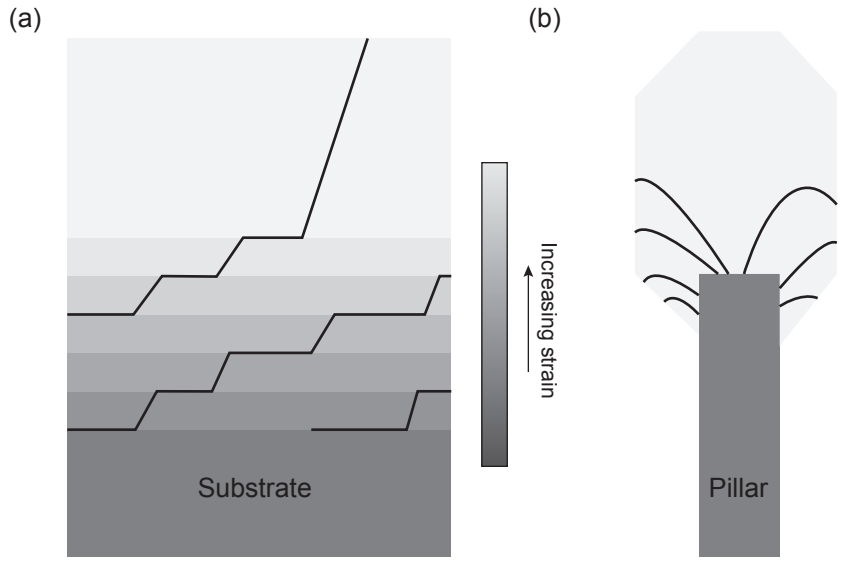


FIGURE 3.2: Schematic illustrations of strain relief techniques. (a) Metamorphic strain relief using step-graded buffers to promote efficient strain relief and minimize defect density in the active layer. (b) Annihilation of dislocations on the free surfaces of a pillar based geometry, yielding a low density of defects in a large fraction of the mismatched material. After [11].

Typical metamorphic designs relax on the order of 2% lattice mismatch. Therefore, the 5% lattice mismatch is quite extreme in comparison. However, this is not unprecedented – recent work from the von Kanel group at ETH Zurich explored the growth of Ge on etched Si micropillars, which have a 4% lattice mismatch. With the appropriate growth conditions, threading dislocations grow outwards and annihilate on the sidewalls of the growing layer, yielding a large fraction of dislocation free material (Figure 3.2b). If this behavior could be produced in a heavily mismatched Group III-V compound semiconductor top cell grown on Si, high quality top cell material could be produced.

3.1.2 Geometry

The wire array geometry has been touted for the ability to tolerate lower materials quality by orthogonalizing the light absorption and carrier collection directions. While this still holds

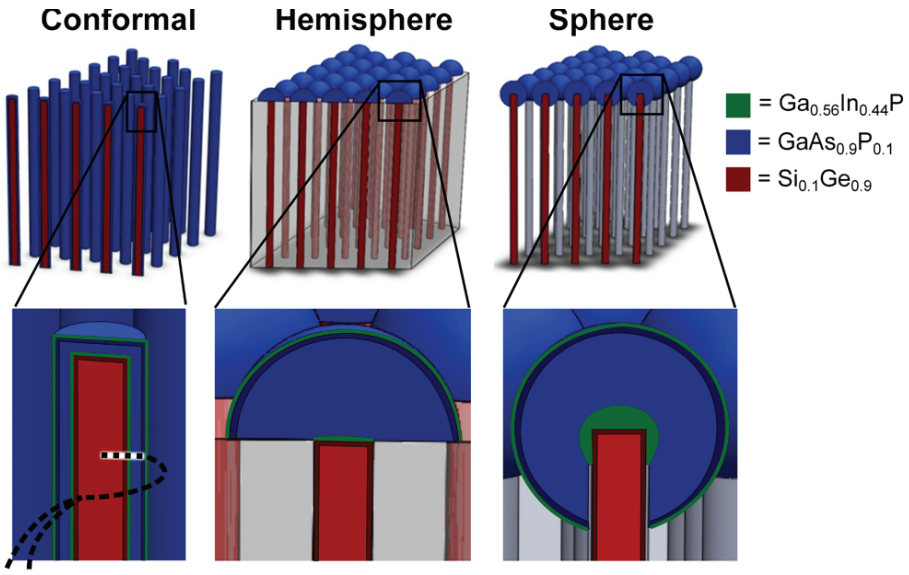


FIGURE 3.3: Geometries of simulated lattice matched $GaAs_{0.9}P_{0.1}/Si_{0.1}Ge_{0.9}$ tandem explored by Dr. Daniel Turner Evans. Taken from [86]

true for materials grown radially on the wire, the details of light absorption impact the types of geometries considered. Dr. Daniel Turner-Evans found that the FDTD simulated light absorption in the top cell of lattice matched GaAsP/SiGe tandem wire arrays were close to the predicted Beer-Lambert absorption. He attributed this near ray-optical behavior to the efficient light absorption in direct gap semiconductors. As a result, the performance of "conformal" geometries were overall worse than geometries with concentrated the Group III-V compound semiconductor material at the tips of the wire as hemispheres or ellipsoids, denoted in Figure 3.3 as "hemispherical" and "spherical" growth [86]. This should in principle allow for higher performance.

3.2 Experimental details

3.2.1 Si microwire array growth

It must be noted that the exact method of preparation changed drastically over the duration of this project. In general, wire arrays were primarily grown on 1 × 1 cm Si (111) substrates. Substrates were cleaved from full 6" wafers with photolithographically patterned periodic Cu catalyst locations as described in Appendix A either by hand or by using a Dynatex GST-150 scriber breaker tool. Almost all of the wire arrays were grown in the "Big Blue" SiGe CVD tool described in 2. In a process identical to that described in Chapter 2, substrates were loaded onto a quartz boat which was then inserted into the CVD tube at 750 °C under N_2 flow. The system was then evacuated and refilled with research grade H_2 up to just above atmospheric pressure before opening the exhaust valve to the scrubber. The CVD tube was then heated to 1000 °C under H_2 flow and allowed to reach thermal equilibrium before precursor introduction. Typical growth parameters include 1 slm of H_2 carrier gas and collection of the overpressure from a $SiCl_4$ cylinder heated to 85 °C. These values correspond to molar flow rates of 430 μmol min^{-1} $SiCl_4$ and 4×10^4 μmol min^{-1} H_2. After growth, samples were cooled slowly to 750 °C inside the tube with an H_2 purge during the initial stage of the cool transitioning to a N_2 purge. The tube was then evacuated and refilled with N_2 before being pulled out of the hot zone of the CVD furnace for a faster cool to near room temperature.

3.2.2 Preparation for selective epitaxy

After growth, the wires were cleaned in a series of etching solutions to prepare for thermal oxidation.

1. Remaining surface oxide stripped in BHF for 10 minutes
2. RCA 1 clean: 15 minute etch in 1:1:5 NH_4OH, H_2O_2 and DI water at 75 °C

3. Thorough rinse in DI water
4. BHF dip to remove chemical oxide
5. RCA 2 clean: 15 minute etch in 1:1:6 HCl, H_2O_2 and DI water at 75 °C
6. Thorough rinse in DI water
7. BHF dip to remove chemical oxide
8. 1.5 minute etch in 30 weight % KOH in DI water at room temperature
9. Thorough rinse in DI water
10. BHF dip to remove native oxide
11. RCA 2 clean: 15 minute etch in 1:1:6 HCl, H_2O_2 and DI water at 75 °C
12. Thorough rinse in DI water
13. BHF dip to remove native oxide
14. Load sample into tube furnace under N_2 flow at 400 °C
15. Heat to 1100 °C and grow thermal oxide under O_2 flow for 1 hour and 10 minutes
16. Cool and remove sample from furnace

In order to achieve the geometries found to be useful in a Group III-V compound semiconductor on microwire device, we pattern the thermal oxide by infilling the wire array with polymeric material and etching away the exposed oxide layer. The most reproducible results were achieved by infilling with mounting wax. After heating oxidized samples on a hotplate to $>$ 120 °C, pieces of wax were applied to the surface of the hot wire arrays, depositing large amounts which then wicked out over the surface over several minutes. While this method results in poor control of the wax height, the designs of interest are in general close to the completely filled limit. The arrays were then cooled to room temperature and loaded into an oxygen plasma asher, where they were ashed at 300W and 300 mT p_{O_2} for

30 minutes to expose the tips of the wires. The exposed thermal oxide was removed in buffered hydrofluoric acid, and the remaining wax was removed in an acetone bath before rinsing with isopropyl alcohol and water.

3.2.3 MOCVD growth at the Molecular Foundry

Immediately prior to growth, wire arrays were cleaned in RCA 1 and RCA 2 etches with care taken to minimize the time in buffered hydrofluoric acid solutions before each etch and before loading into the reactor glovebox. Planar Si wafer equivalents were used as control and process monitoring samples, with Si (111), (110), (211), and (100).

Typical growth parameters are depicted in Table 3.1. Initiation of the growth process generally fell into three stages. First, a high temperature anneal was used to try and remove any residual contamination and to allow surfaces to reconstruct under hydrogen flow. Second, precursors were introduced at low temperatures in a "nucleation" step. Finally, after heating under TBP flow, high temperature growth was performed.

	T (° C)	**TBP**	**TMGa**	**TMIn**	**V/III**
GaP					
Nucleation	530	3205	61.8	–	51.9
Growth	680	3205	61.8	–	51.9
$Ga_{0.7}In_{0.3}P$					
Nucleation	530	3205	61.8	16.2	35.3
Growth	680	3205	61.8	16.2	35.3

TABLE 3.1: Typical growth conditions of GaP and GaInP on wire arrays. Precursor flows denoted in μmol min^{-1}.

3.3 Results

3.3.1 GaP

Developing growth parameters for GaP on Si was a major effort that took several years to realize any useful results. Unfortunately, those results did not appear to be translatable to wire array morphologies without further study. However, the primary results of our studies in growing GaP on Si microwires are shown here.

3.3.1.1 Initial results

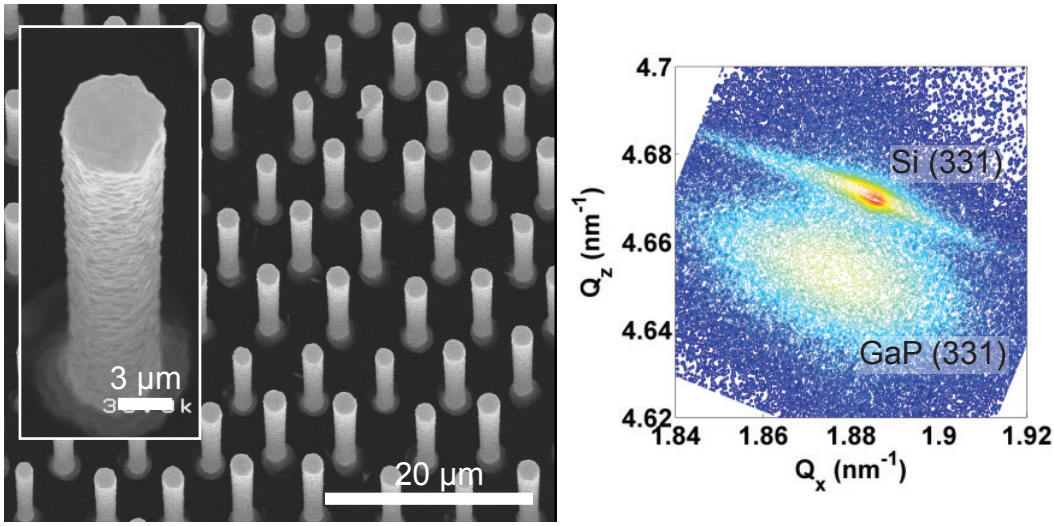


FIGURE 3.4: Initial results of GaP growth on wire arrays. SEM images (left) show conformal coatings with almost no growth on the thermal oxide. (331) reciprocal space map shows a great deal of peak broadening, indicative of high defect density.

To avoid complications related to substrate preparation, initial GaP growths were performed with a minimum of processing done to the wire arrays prior to growth. As seen in Figure 3.4, fully conformal coatings along the length of the wires were achieved. Most notably, the thermal oxide remaining on the planar surface of the wire array substrate served as an

excellent inhibitor of GaP growth. XRD of the GaP coated wire arrays indicated textured epitaxial growth on the wires, with significant broadening in both ω and ω-2θ. Further improvements in growth parameters and substrate preparation would be needed to improve material quality.

3.3.1.2 Branched morphologies

Branched wire array structures have been of interest for increased surface area for electrochemical processes and possibly increased solar absorption. Fairly early in our efforts, we were able to generate branched GaP nanowires while trying different growth conditions. After a lower temperature nucleation step, the TBP pressure controller setpoint was dropped from 1500 to 800 torr. Pressure controllers work by changing the size of an orifice to regulate the pressure. Dropping the setpoint results in the controller to open fully until the new setpoint pressure is reached. As a result, this must have seeded the surface with an excess amount of TMGa, resulting in Ga droplets being formed on the surface. These droplets likely resulted in VLS growth of GaP nanowires. Detailed investigation of this phenomena was not pursued after several failed attempts to more systematically replicate seeding the surface with Ga droplets.

3.3.1.3 Selective epitaxy

As mentioned previously, selective epitaxy allows us to access different geometric conformations of Group III-V compound semiconductor material on the wires, yielding benefits due to a majority of light absorption being concentrated in direct gap top cell tips and ideally allowing for threading dislocations to annihilate further away from material actively participating in light absorption and electron-hole pair separation. Using the scheme presented earlier in the chapter, Si microwire substrates with varying amounts of exposed Si were

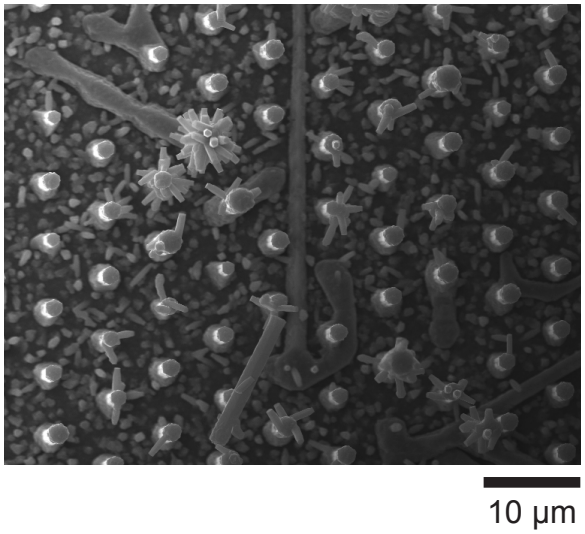


FIGURE 3.5: SEM image of branched GaP nanowires grown on Si microwire arrays.

prepared. By changing the amount of exposed Si from long to short, morphologies approximating the "conformal" and "spherical" geometries were achieved (Figure 3.6). Detailed study of the crystallographic properties was carried out with XRD and TEM.

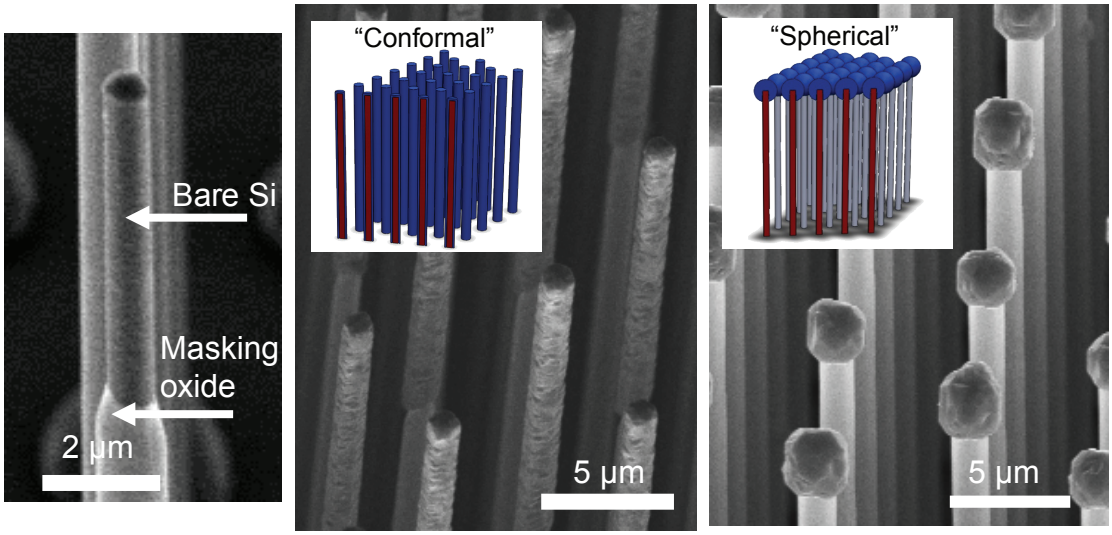


FIGURE 3.6: Geometries enabled by selective epitaxy.

Figure 3.7 depicts a representative example of conformal GaP growth. In general, the morphology of the layers remained similar to the preliminary experiments on wire arrays without intentionally patterned selective epitaxy masking oxide. Morphology is a great indicator of crystalline quality – virtually all surface features have their origin in crystallographic strain or defects. Therefore, we expect a significant defect concentration in the wires, based upon the rough appearing morphology. XRD clearly showed that the layers were epitaxial, and the prescence of defects was confirmed with TEM of radial cross sections of single wires coated with GaP. Almost all of the defects originate at the GaP/Si interface. Nano-beam diffraction of the representative sample shown in Figure 3.7 shows 1/2 order spots, consistent with stacking fault formation [4].

Representative data for the spherical type geometry is presented in Figure 3.8. Compared to its conformal counterpart, the axial cross section characterized with TEM shows lower defect density overall. However, many defects still originate from the Si/GaP interface, and XRD reciprocal space mapping shows similar peak breadths in the ω and ω-2θ directions. This is clearly seen in HRTEM images of the top and left sides of the wire, where defects emanate from the interface. Diffractograms taken from these images contain 1/3 order spots, which are consistent with $\Sigma 3$ twin array formation, and streaking defects, which are consistent with stacking faults [4]. These defects have been observed in planar GaP grown on Si, especially when growing on orientations other than (001) [55].

3.3.2 $\mathbf{Ga_{1-x}In_xP}$

3.3.2.1 Planar controls on GaP(001)

To limit the effects of the wire array substrates on composition and growth parameters, several sets of layers were grown on GaP (001) orientated substrates. One representative sample is shown here in Figure 3.9. The crosshatch morphology evident in the microscope image is indicative of strain relief by dislocation motion. The layers are indeed epitaxial, with clear peak locations for each of the different material layers. In this particular sample,

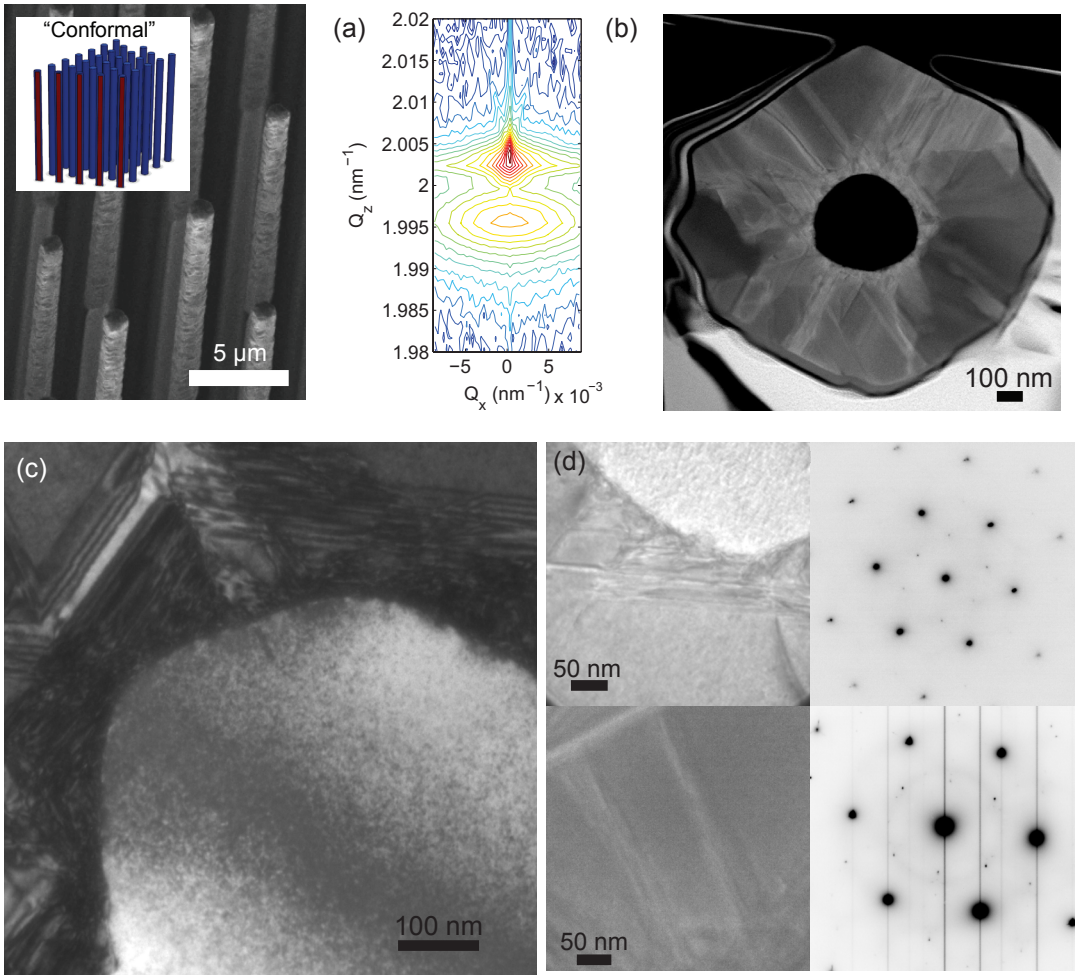


FIGURE 3.7: XRD and TEM characterization of "conformal" growth. (a) (111) reciprocal space map shows reduced peak broadening compared to earlier efforts. (b) HAADF STEM imaging of a radial cross section reveals high defect density in the GaP. (c) BF image of wire and initial GaP layers provides more defect contrast. (d) Nano-beam diffraction in the regions on the (left) show 1/2 order peaks indicative of defects.

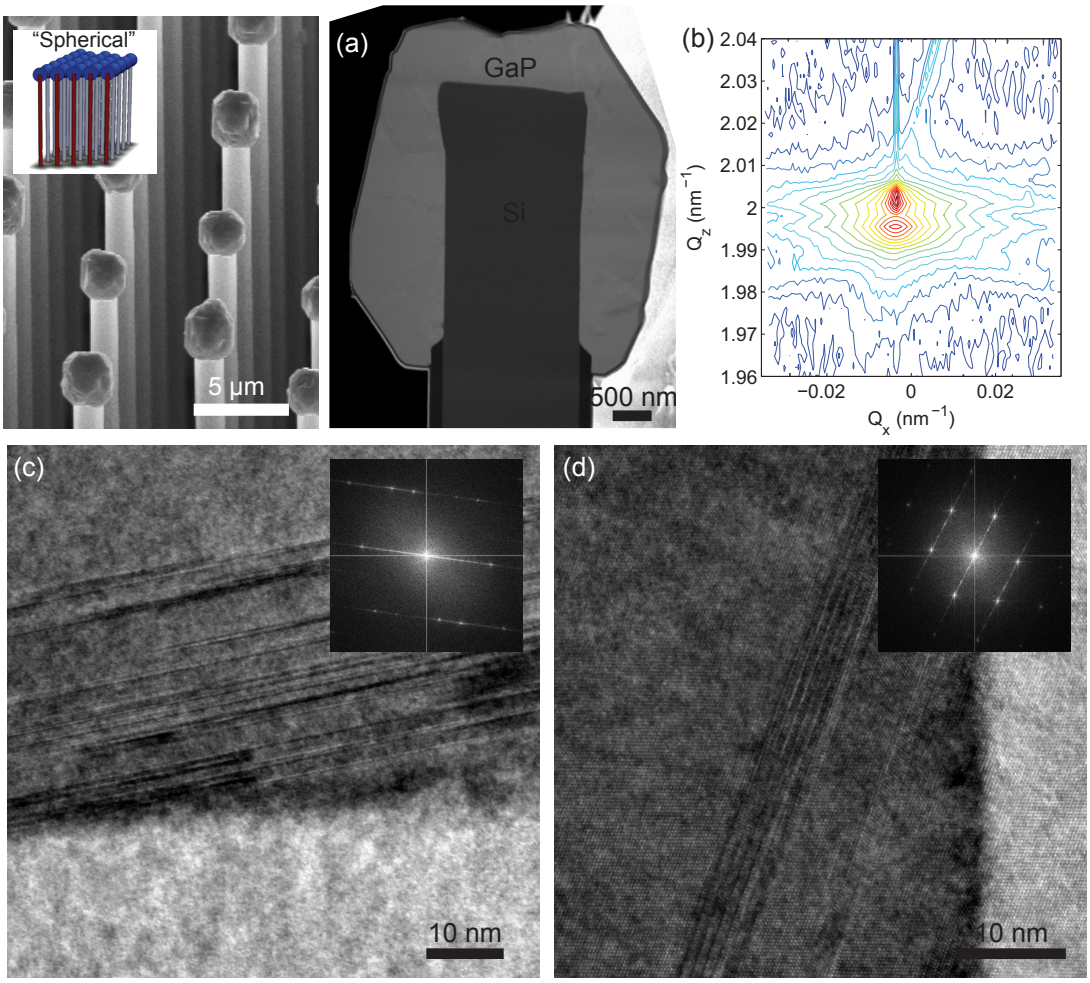


FIGURE 3.8: XRD and TEM characterization of "spherical" geometry. (a) HAADF STEM image shows clear compositional contrast between the GaP and Si wire. (b) (111) RSM shows similar peak width to the "conformal" samples. (c) HRTEM of the GaP/Si interface at the top of the wire with inset diffractogram. (d) HRTEM of the GaP/Si interface along the left side of the wire with inset diffractogram.

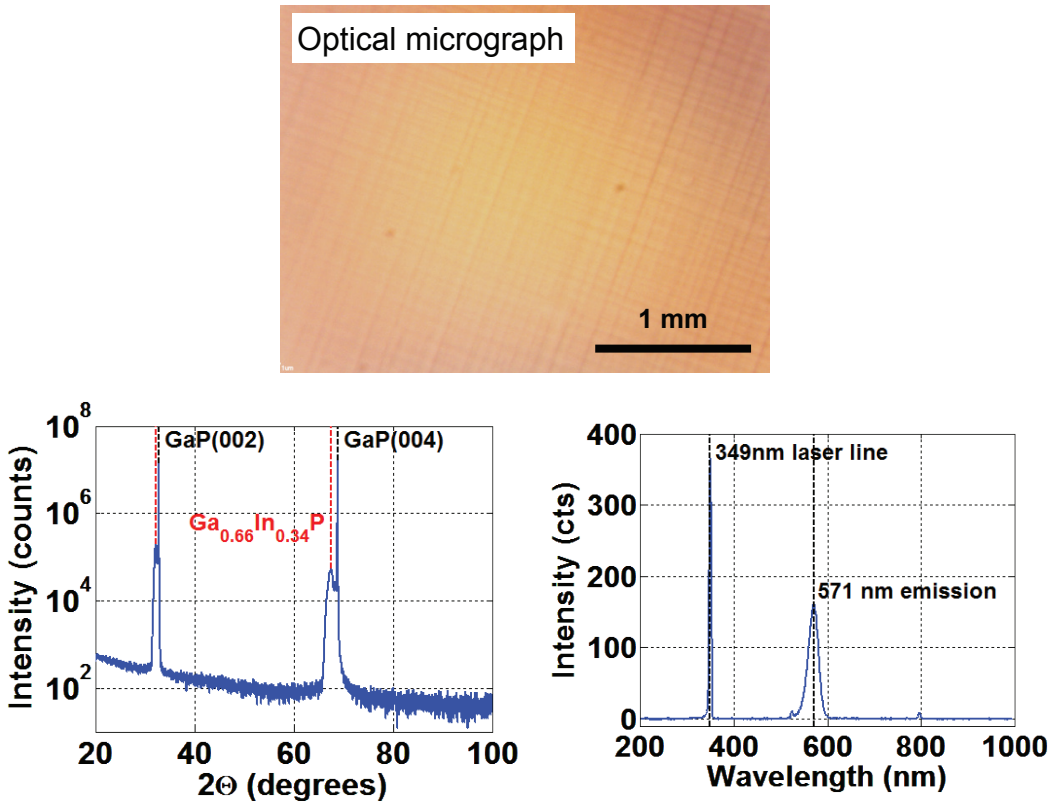


FIGURE 3.9: Planar GaInP graded stack with luminescence on GaP (001).

extrapolation of the composition of the layer with highest In contenct from the layer peak position yields a value of 34% In. Room temperature photoluminescence measurements using a UV laser diode revealed emission at 571 nm, which matches the $\sim$ 2.2 eV bandgap expected from XRD. The knowledge gained from these control experiments was then used for the microwire array growth experiments.

3.3.2.2 Step-graded buffer growth on wire substrates

All of the GaInP work on microwire arrays focused on samples approximating the "spherical" geometry, as those were found to be more efficient overall in coupled optoelectronic simulations [86]. The first set of samples grown were step graded GaInP layers, similar to

the layers grown on the planar controls. Single wires were processed using the FIB into electron-transparent membranes for TEM characterization. As clearly seen in Figure 3.10, a large network of defects emanate from the GaP/Si interface throughout the entirety of the coating. Clear compositional contrast between each of the layers is seen in Z contrast imaging (Figure 3.10b). Closer investigation of the GaP/Si interface with HRTEM (Figure 3.10c) shows a large number of $\Sigma 3$ microtwin arrays along each of the three possible habits. This suggests that these defects may be an intrinsic feature of growing on the complex, multifaceted microwire array surfaces.

EDAX was used to evaluate the compositional profile within the step graded GaInP stack (Figure 3.11). Clear compositional contrast can be seen between each of the layers, with no evidence of interdiffusion. Voids can also be seen most clearly in the map of the P signal. A maximum of 23% In is reached, below the indirect-direct band gap transition (Figure 3.12). Even if the material were defect free, the photoluminescence signal would be very low compared to a direct gap sample.

3.3.2.3 Double heterostructure growth on wire substrates

Samples were grown with higher In content in a double heterostructure configuration. By sandwiching the GaInP emitting material in higher bandgap AlInP, photogenerated electron-hole pairs would be trapped inside the material and forced to recombine. The target design of a structure grown on an $Ga_{1-x}In_xP$ step-graded buffer is shown in Figure 3.13a. Unfortunately, no photoluminescence signal was measured, so single wires were processed into electon thin samples for TEM analysis. Due to the size of the structure, it was necessary to thin in steps along the wire itself, leading to some of the horizontal features in the STEM image. As seen in Figure 3.13b, contrast between each of the layers confirms their step-graded nature, with clear contrast between the AlInP and GaInP layers. Voids also exist primarily along the sides of the structure in the GaInP, but there exists a large amount of material that appears to be void-free at the top of the wire. Additionally, the thickness of the layers is not uniform around the structure, with thicker material

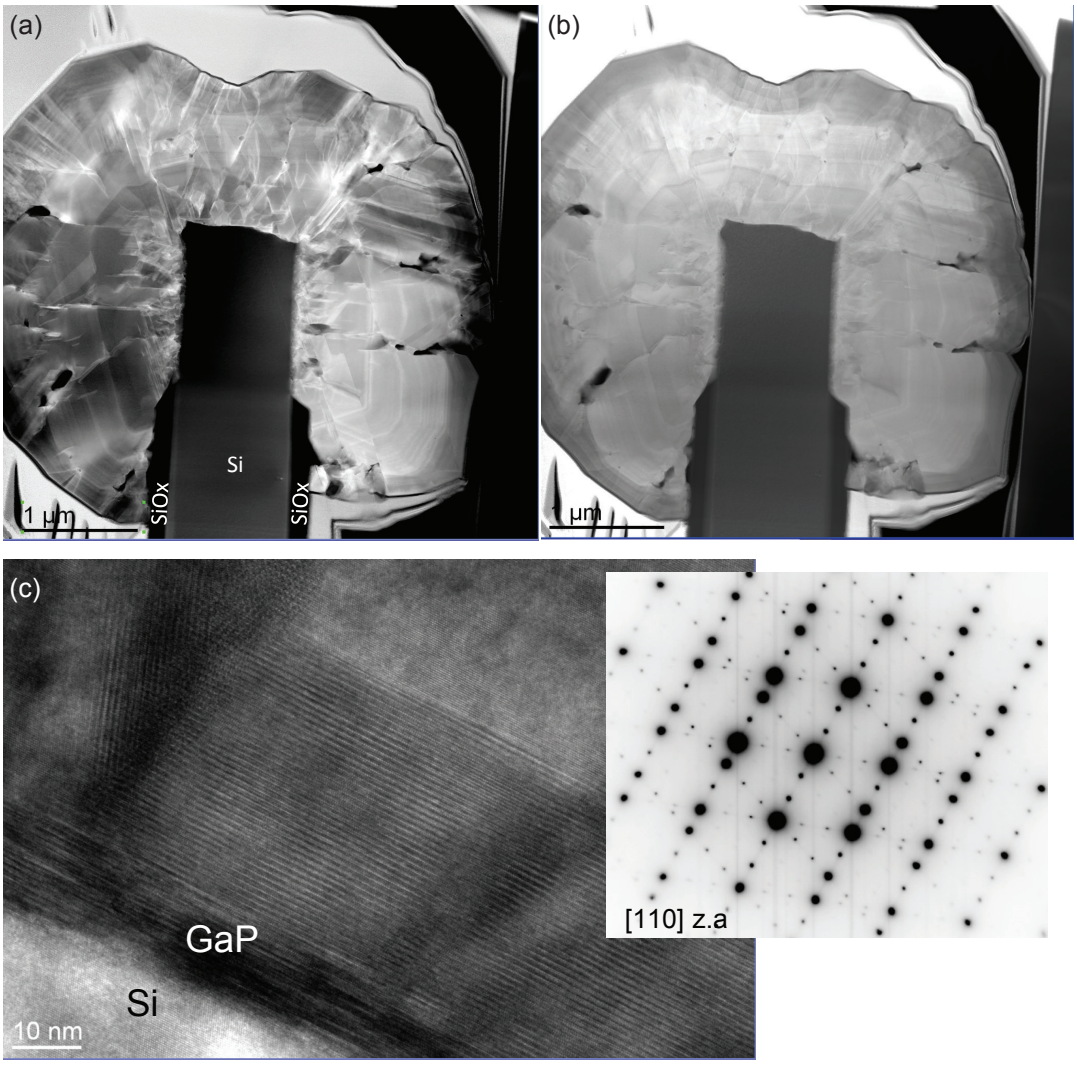


FIGURE 3.10: HADDF STEM image of GaInP graded buffer grown on a silicon microwire. (a) Diffraction contrast STEM image. (b) Z contrast TEM image. (c) HRTEM of GaP/Si interface reveals a dense network of Σ3 microtwin arrays.

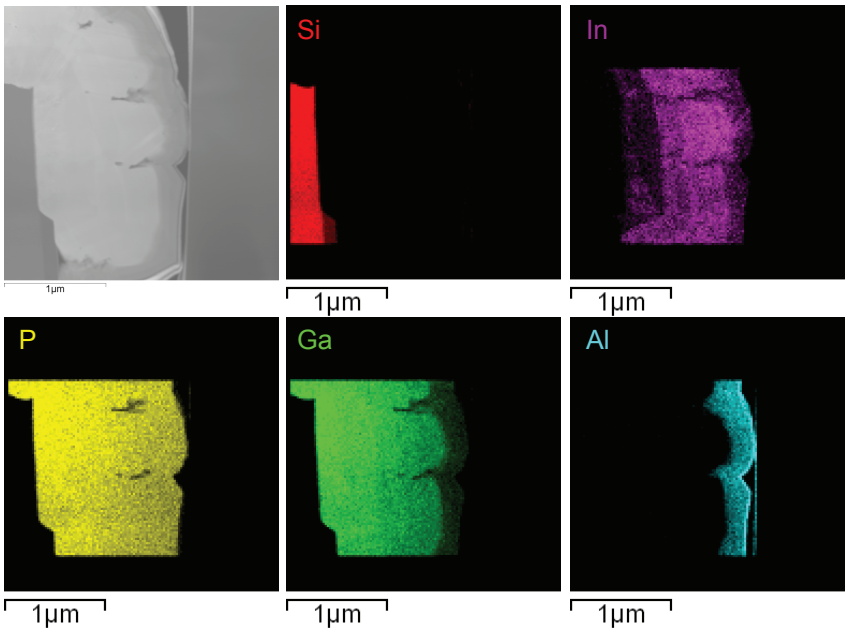


FIGURE 3.11: EDAX mapping of the GaInP graded buffer on Si microwire.

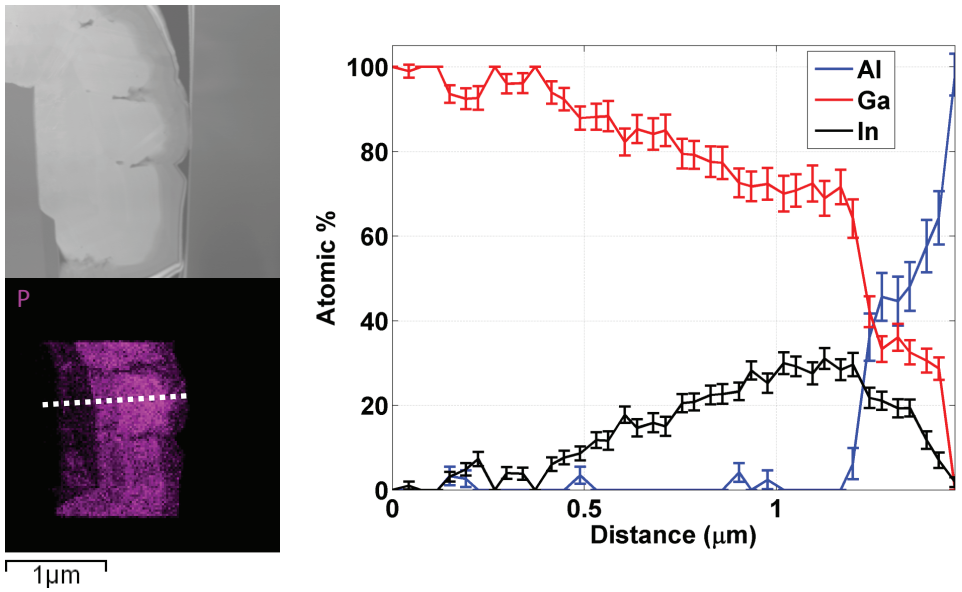


FIGURE 3.12: EDAX linescan of the GaInP graded buffer on Si microwire.

located directly above the wire that becomes thinner along the sides – this is most clearly seen in the AlInP window layers. This could be an indication of mass transport becoming an issue as the material grown on the arrays approaches a close packed structure [11]. Within the buffer, fine-features in the STEM image stand out (Figure 3.13c). Indium containing III-phosphides such as $Ga_{1-x}In_xP$ are known to undergo phase segregation during growth [12], which poses significant challenges with growing step-graded buffers , and the three-dimensional nature of the wire substrate could also play a role in encouraging phase separation [54, 72].

TEM characterization of the structure also yielded further insights (Figure 3.14. A great deal of diffraction contrast can be seen in the TEM image, likely indicative of high defect density. HRTEM imaging of the GaP/Si interfaces at the top and sidewalls of the wire reveal the presence of a thin interfacial layer ($\sim$ 1-2 nm thick), which is likely a sign of intermixing due to excess Ga precursor flux during the nucleation step, and defects can be seen in the GaP layers. Diffractograms taken in the HRTEM images of the Si and GaP alone reveal 1/3 order diffraction spots indicating $\Sigma 3$ twins at each of these interfaces (Figure 3.15).

Finally, EDAX was used to evaluate the composition of each of the layers. A linescan of the layers is presented in Figure 3.16. The peak indium weight percentage in the GaInP corresponds to a layer with $Ga_{0.29}In_{0.71}P$, and the window layers appear to have a composition of $Al_{0.23}Ga_{0.36}In_{0.41}P$.

3.4 Routes towards improved material quality

3.4.1 Geometrical considerations

Wire arrays dramatically increase the surface area presented to the MOCVD effluents during growth. The effects of this can be seen clearly in the difference between the thickness of planar layers and wire array coatings with the same growth time. Selective epitaxy with dielectric masks have also been explored for the growth of highly mismatched materials. In

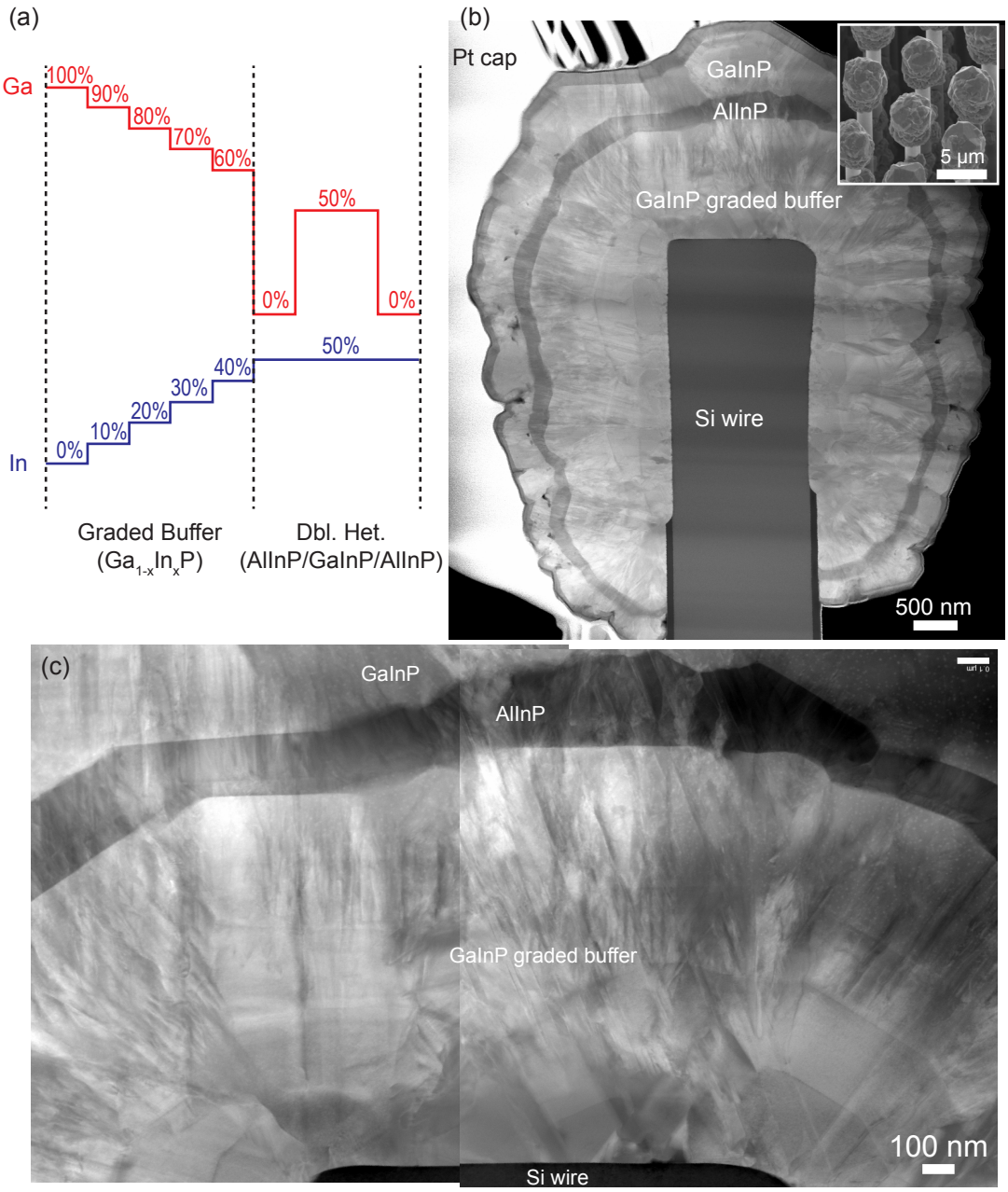


FIGURE 3.13: AlInP/GaInP/AlInP double heterostructure grown on a Si microwire. (a) Targeted layer design. (b) Z-contrast HAADF STEM image of a single wire with an SEM image of the array inset. (c) Higher resolution Z-constrast STEM imaging of the graded buffer above the wire.

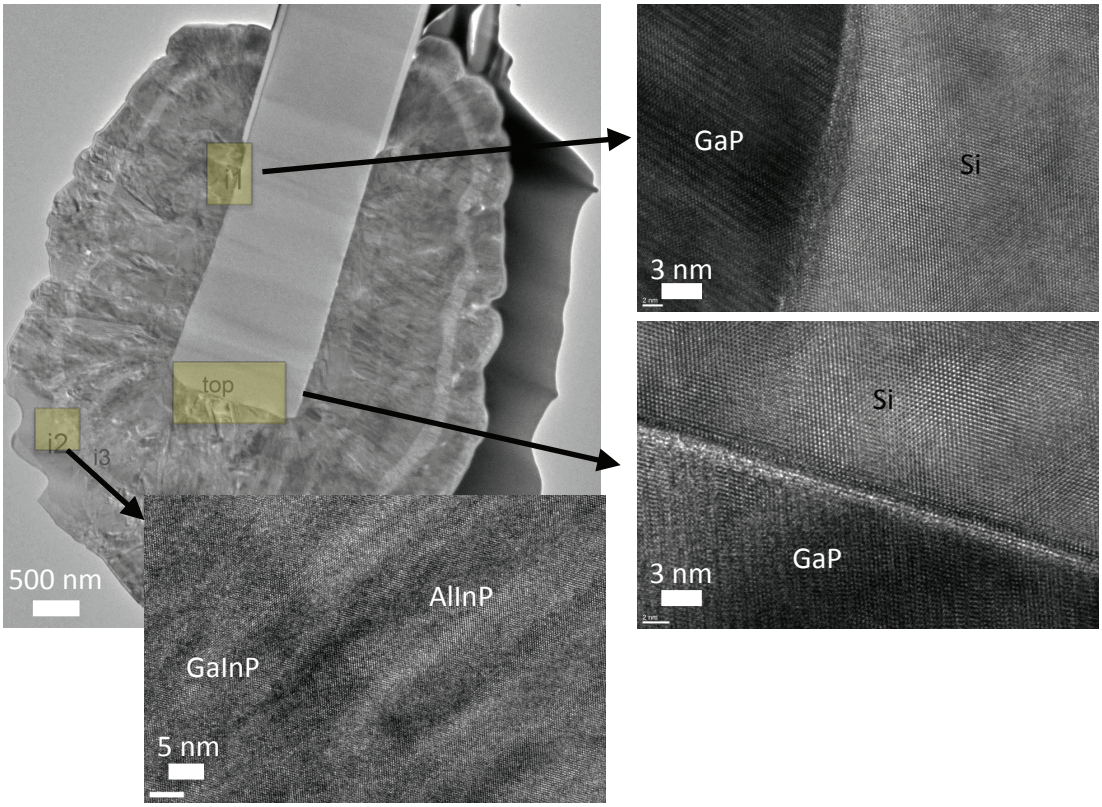


FIGURE 3.14: TEM imaging of the AlInP/GaInP/AlInP double heterostructure with HRTEM insets of GaP/Si and AlInP/GaInP interfaces.

this work, a simple model for the enhancement in growth rate assuming that the concentration of precursors supplied to any give location stays the same across the surface, resulting in a local increase in the amount of available precursors if part of the surface is masked. Following Galuchet *et al.* [13], we can express the filling fraction, F, which can be expressed quite simply in terms of the surface area of the structured material ($A_{structured}$), and the projected area (A_{planar}).

$$F = \frac{A_{structured}}{A_{planar}} \tag{3.1}$$

Assuming that the local concentration of precursors leads to enhancement of the growth

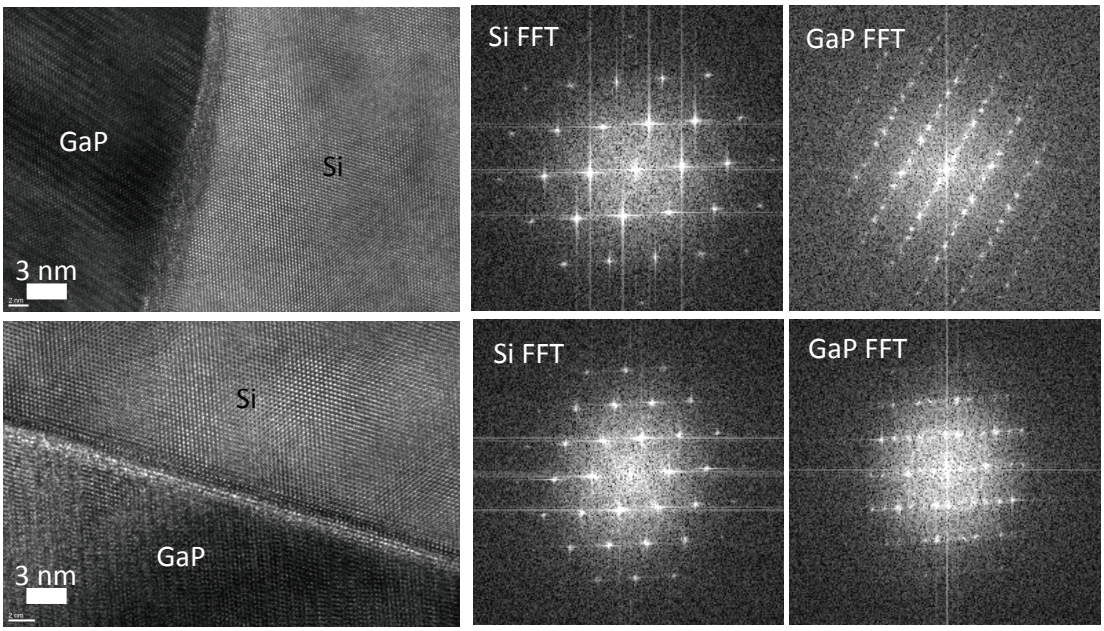


FIGURE 3.15: Σ3 microtwinning at the GaP/Si interface with diffractograms of Si and GaP areas.

rate, we can easily calculate an effective growth rate, R_{eff}, as the inverse of the filling fraction.

$$R_{eff} = F^{-1} \tag{3.2}$$

We can examine the effect of selective epitaxy on the local effective growth rate for a given wire geometry with simple assumptions about the geometry of the wire arrays. For simplicity, we make the following assumptions:

1. Wires are perfect cylinders with uniform diameter and height.
2. The amount of exposed wire material, h, is constant throughout the array.
3. All wires are identical.

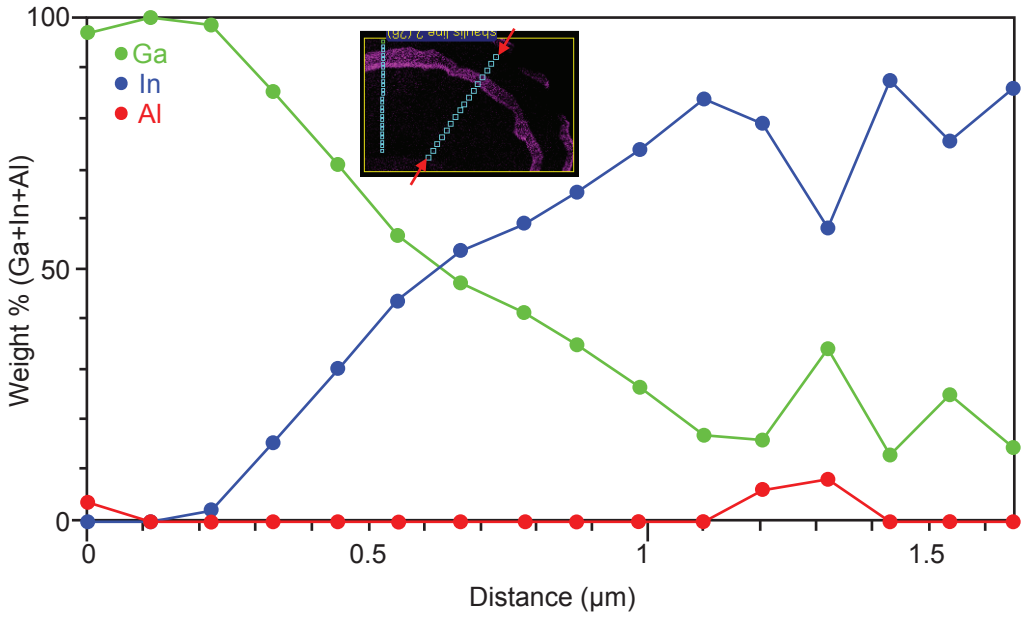


FIGURE 3.16: EDAX line profile of Ga, In and Al composition in weight percent.

These assumptions allow the exposed surface area of a masked wire array to be calculated, as shown in Figure 3.17. There, we have calculated the effective growth rate as a function of h for square and hexagonal arrangements of microwire arrays with different diameters (d) and pitch (a). The straightforward implication is that as the amount of material exposed is decreased, the growth rate is enhanced up to two orders of magnitude compared to a planar surface. This has several important implications on real wire arrays. In particular, the geometries of the indivdual wires are variable across any given array, which can result from errors in photolithography, liftoff, surface contamination, and growth conditions. Even if these errors are mitigated, some nonuniformity in the wire heights exists across an array, likely a result of the relative depletion of precursors at the center of an array versus at the edges.

Initial attempts at verifying these simple calculations were made by using the higher quality GaP nucleation and growth parameters discussed in Chapter 5. Single wires were thinned

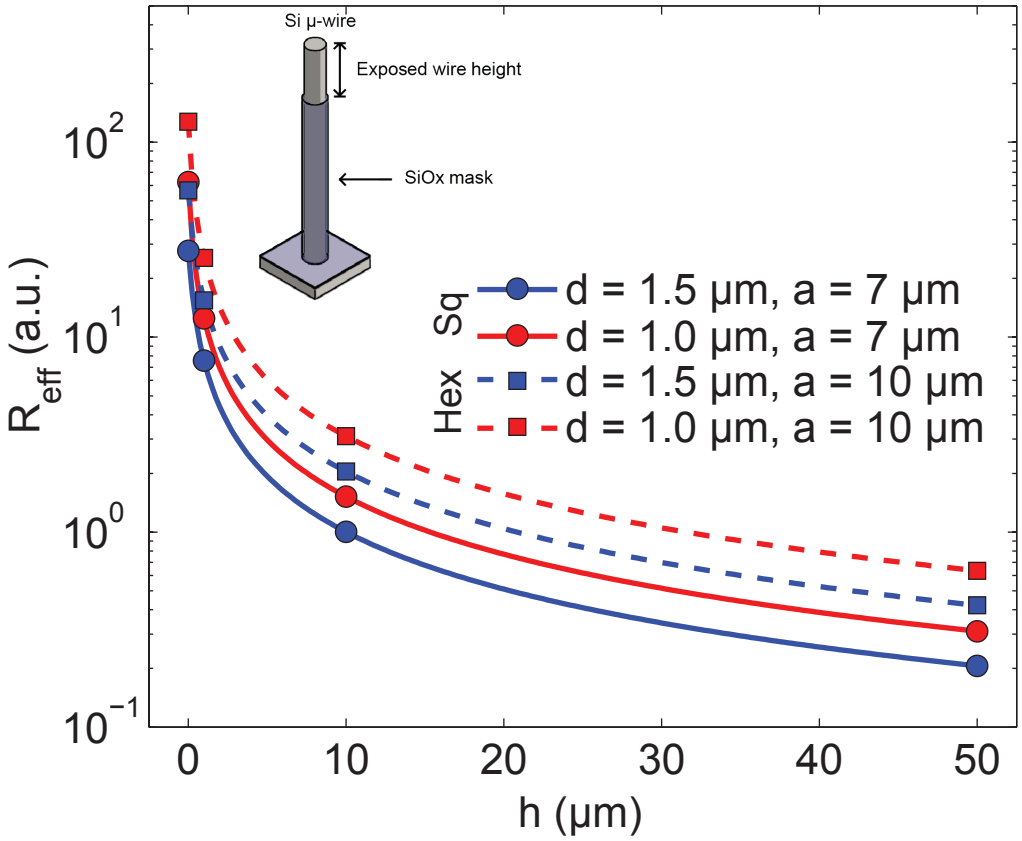


FIGURE 3.17: Effective growth rate of wire arrays as a function of exposed height.

into electron transparent sections for EDS analysis. For the wire where $R_{eff} > 1$, high defect density can be seen in the GaP layer both above the wire and along the sidewall 3.18. Selected area diffraction (SAD) patters of these regions attest to the defected nature, with a population of 1/3 order spots visible in both locations. For the wire with $R_{eff} < 1$, the low effective growth rate leads to defects where different regions are growing together, and the defect density is quite low within single domains (Figure 3.19). This is by no means a fair comparison due to how thin the layer is compared to the other case, but it is at least promising for future applications.

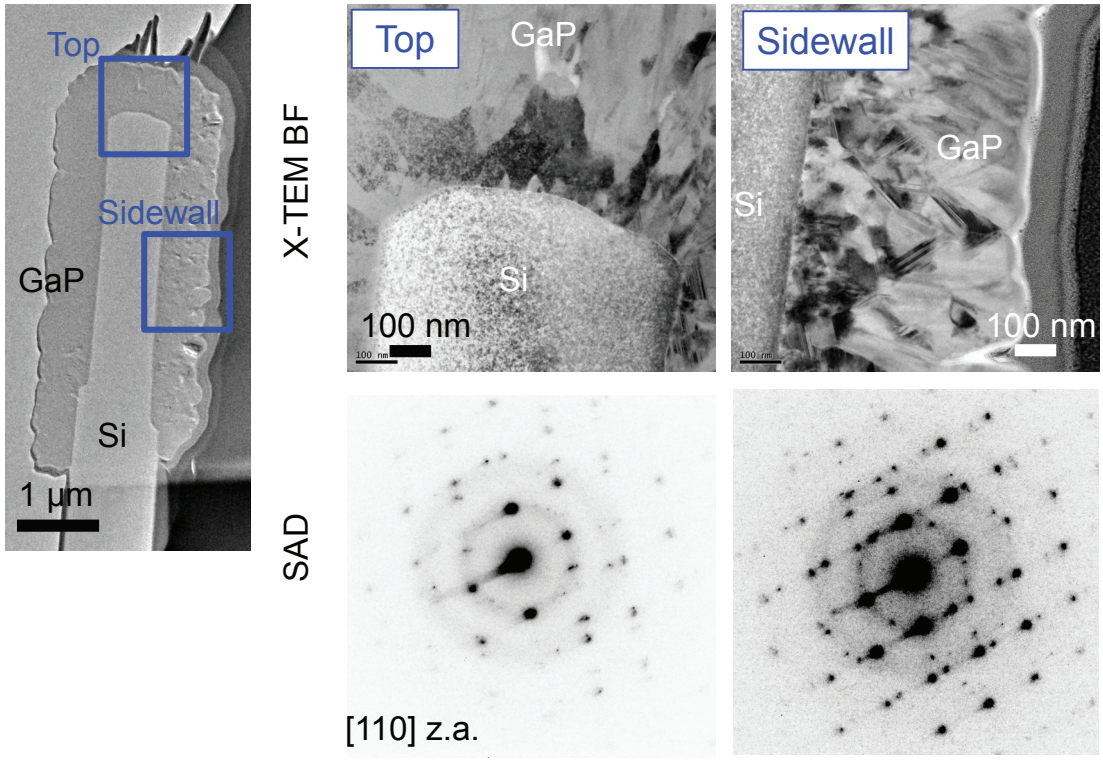


FIGURE 3.18: TEM of a GaP layer grown on a wire with $R_{eff} > 1$.

3.4.2 Direct integration of nano-sized geometries on planar Si

From the growth studies detailed in this chapter, it is clear that defects at the Si/III-V interface play a major role in disrupting the material quality of layers grown on the Si microwire arrays. These defects likely serve as highly active non-radiative recombination centers, preventing any measurable photoluminescence in all of the highly mismatched, direct gap $Ga_{1-x}In_xP$ on planar Si wafers or VLS grown wire arrays. Both polar-on-nonpolar and lattice mismatch defects can be avoided entirely by moving to nanoscale growth geometries, such as nanowires, nanoplates and nanocrystallites. The small surface area of the Si/III-V interface limits or eliminates the possibility of forming polar-on-nonpolar defects, and the traction-free surfaces of these nanoscale structures allow for strain relief outwards from the substrate.

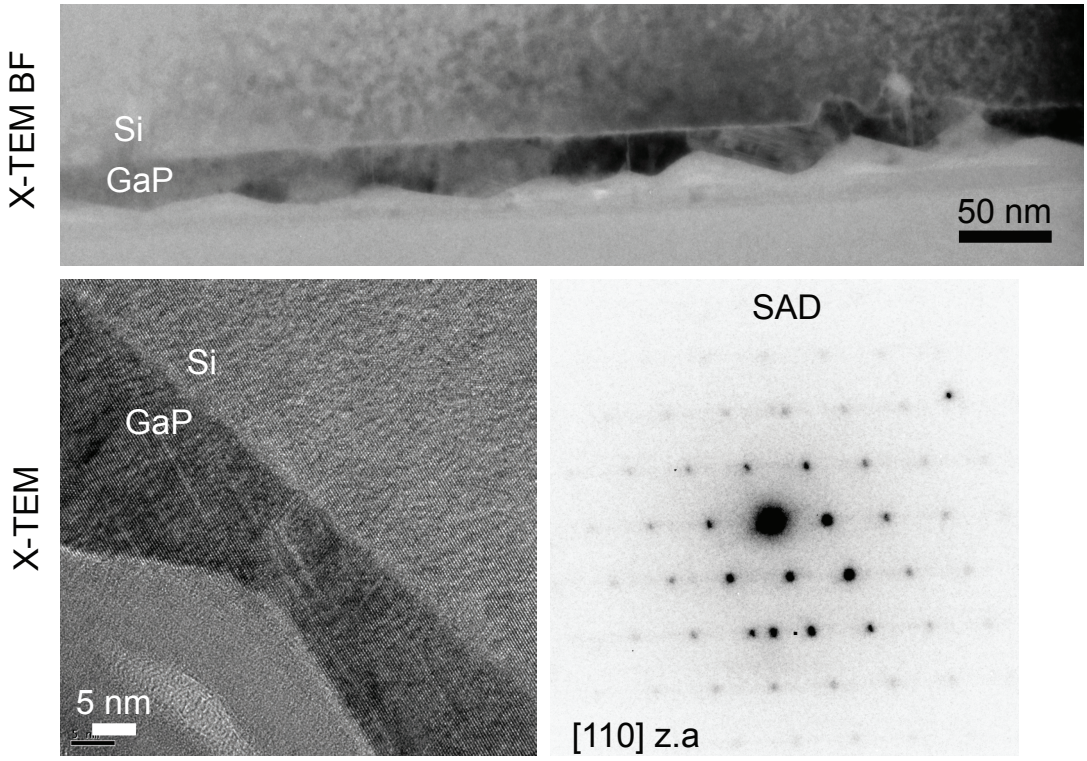


FIGURE 3.19: TEM of a GaP layer grown on a wire with $R_{eff} < 1$.

As mentioned previously, the economics of solar have changed drastically over the course of my PhD. High lifetime Si wafers are now cheap and widely available. As such, it is conceivable to replace the low lifetime VLS-grown Si microwire arrays with either planar wafered Si or high lifetime, etched Si micropillar arrays. Beyond increased Si material quality, moving to top-down fabrication allows for the arbitrary selection of substrate orientations. The substrate orientation has very profound effects on the material quality due to different propensities to form defects [55] and strain relaxation mechanisms [43], and the best results for Ge grown on Si micropillars have been for the (001) orientation [11]. Use of the (001) or (112) orientation would allow the transfer of the knowledge gained from planar thin film growth in Chapter 5 to future etched pillar structures. The simple calculations for effective growth rate also suggests that moving to sparse arrays would allow for low precursor utilization and/or higher growth rates. Furthermore, axial heterostructures consisting of Si

micropillars and Group III-V epitaxially grown pillars could serve as more effective light absorbers, allowing for precise tuning of the optical properties of the device.

The future is ripe for further investigation of Group III-V on Si heterostructures on Si.

Chapter 4

Optoelectronic design of Group III-V compound semiconductor on Si microwire tandem cells

4.1 Background

As discussed in Chapters 2 and 3, one of the primary goals of my doctoral work was to realize a tandem microwire array solar cell. While the potential efficiency of a hypothetical device was considered, detailed balance efficiency represents an upper limit to what is achievable. Detailed device modeling incorporating known materials parameters allows for the incorporation of more realistic loss mechanisms, including but not limited to Shockley-Reed-Hall, Auger, and surface recombination, as well as details of the physics of carrier transport. For near or sub-wavelength features, full-wave electromagnetic simulations are necessary to accurately reproduce optical behavior, and the wire array devices definitely fall into this category. This chapter will present two simulated wire array tandem cell designs, both of which could conceivably be fabricated using the methods described in

previous chapters. The implications of the optoelectronic simulations on device design will be presented.

4.1.1 Simulation methods

The finite-difference time-domain (FDTD) method is used to solve Maxwell's equations iteratively. As the name implies, the partial differential form of Maxwell's equations are solved by converting the derivatives to finite differences. The electric and magnetic field components are arranged in an interpenetrating Yee lattice. Using a "leapfrog" algorithm, the magnetic and electric field are updated one after another in a single timestep.

Optical and device physics models were carried out using the Synopsys Sentaurus TCAD package. Details of the implementation and source code can be found in Appendix E. Sentaurus EMW, a full field, finite difference time domain (FDTD) electromagnetic simulation tool, was used to simulate the optical properties of the full device structure in 2D. To mimic a wire array, horizontal boundaries were assumed to be periodic, with a back reflector modeled as a perfect electrical conductor and a perfectly matched layer above the structure. Shockley-Reed-Hall (SRH) recombination was considered in all of the layers, while Auger and radiative recombination were also considered in each of the Group III-V compound semiconductor layers. Doping dependent mobility and lifetime were also considered in the GaInP and Si, while constant mobility was assumed for the AlInP.

4.1.2 Prior work

Coupled optoelectronic device design has been a focus of the Si microwire project for quite some time. Dr. Michael Kelzenberg devoted significant study to the optical properties of the wire arrays [33] and their performance in devices [34] with coupled FDTD and device physics simulations. Using both analytical and computational methods, Dr. Daniel Turner-Evans studied the performance of lattice matched GaAsP on SiGe wire array structures [86]. In this work, he found that the highly absorbing direct gap GaAsP could have its optical

absorption approximated using the Beer-Lambert relation, a surprising finding. This result motivates our selection of "spherical" geometries which resemble a lollipop or cotton swab, as the increased GaAsP material in a "conformal" core-shell geometry would contribute very little to the overall optical absorption while increasing the junction area. The spherical geometry also has the added benefit of being demonstrated by MOCVD growth in Chapter 3.

4.2 Simulated device designs

For a Si bottom cell, an ideal top cell with a bandgap of 1.7 eV, such as ordered $Ga_{0.45}In_{0.55}P$ or disordered $Ga_{0.35}In_{0.65}P$ alloys, would yield a detailed balance efficiency of 41%. Our simulated devices incorporate a $Ga_{0.51}In_{0.49}P$ top cell with a bandgap of 1.89 eV, which results in a detailed balance efficiency of 35%. $Ga_{0.51}In_{0.49}P$ cells with $Al_{0.5}In_{0.5}P$ window layers, utilized successfully in high efficiency triple junction solar cells for several years, have been studied thoroughly and thus lend themselves to realistic predictions of device performance despite lower efficiency potential.

4.2.1 Requirements for a tandem wire array device

Tandem photovoltaic devices require two independent photovoltaic cells optically in series. High energy light must be absorbed by the high bandgap cell leaving the low energy light to be absorbed by the low bandgap cell. In practice, tandem cells are arranged optically and electronically in series. This avoids the need for a second set of contacts, but this also requires a tunnel junction to provide electrical contact between the two cells. A tunnel contact is typically realized by using two heavily doped layers of opposite polarity. Each subcell must contain a homo- or heterojunction which enables carrier separation and collection.

Fabrication of such a device would first comprise VLS wire growth, followed by cleaning, oxidation and masking of the wire to enable in-diffusion of the radial junction. After in-diffusion, all of the oxide on the surface would be removed and a second oxidation and masking step would be performed to allow for masking of the subsequent compound semiconductor growth.

One of the major challenges of realizing a nano- or microscale device is to develop an effectively transparent top contact scheme. To simplify our simulation and analysis, a perfect contact, without optical or electrical losses, is placed directly on top of each of the wires.

4.2.2 Highly mismatched growth on a Si wire

The device structure (Figure 4.1) was chosen to mimic experimentally observed geometries and other experimental constraints. In particular, a 200 nm thick thermal oxide (SiOx) is patterned on the sidewalls of the Si wire, leaving only the top 2 μm of the wire in contact with the top cell. This layer is used as a mask for selective epitaxy only at the very ends of the wire. Additionally, a 500 nm thick, highly defective, heavily doped "buffer" layer has been introduced between the Si wire bottom cell and the tunnel junction. The 3.9% lattice mismatch with the Si bottom cell will result in defects due to the need for strain relief in the III-V top cell. It is assumed that any defects due to lattice mismatch and heteroepitaxy are concentrated in this region, with the consequence of low material quality. The defective buffer layer was assumed to have a low $\tau_{SRH} = 1$ ps. A summary of the layer materials, doping levels, and geometric parameters in the full device stack is given in Table 4.1.

4.2.3 Graded buffer growth on a Si wire

Instead of growing GaInP directly on the Si wire, a more realistic approach would be to start with GaP and grow a step graded buffer of $Ga_{1-x}In_xP$ up to the desired composition for the top cell. Complex refractive indices for the $Ga_{1-x}In_xP$ alloys were generated by shifting the

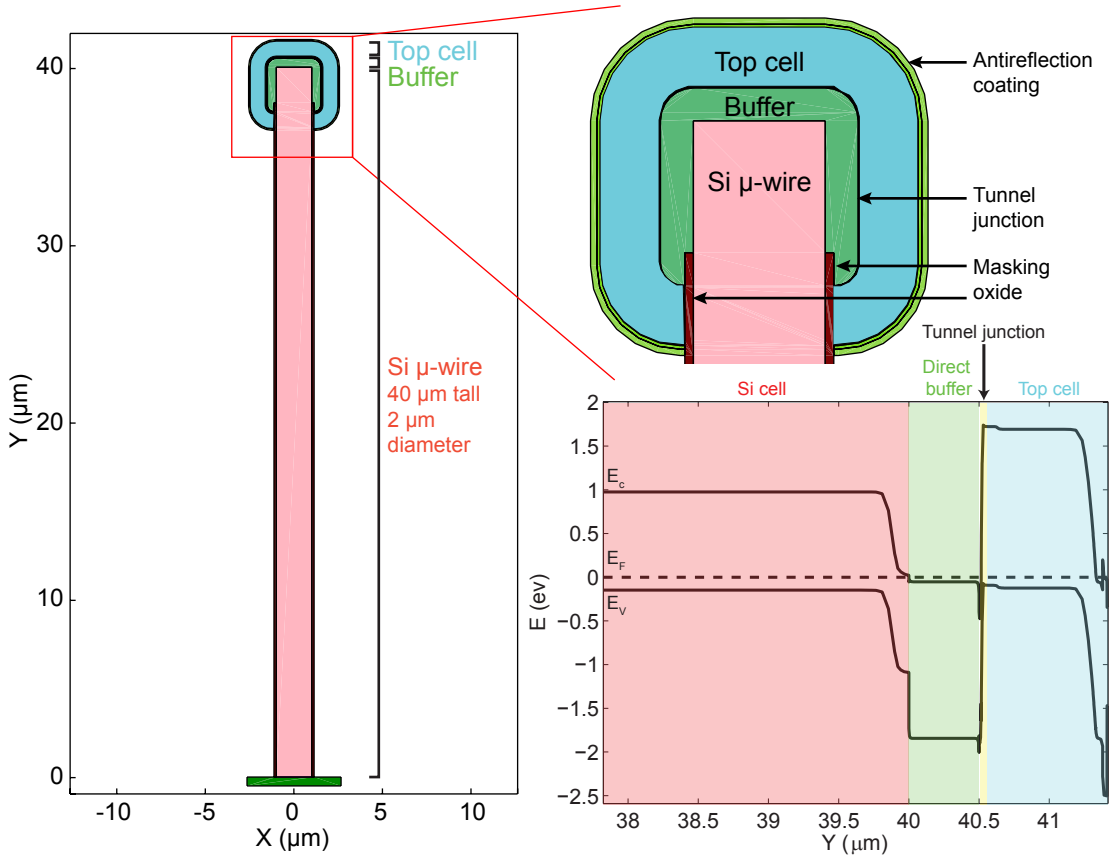


FIGURE 4.1: The simulated 2D device geometry for highly mismatched growth on a Si wire. A 500 nm thick highly doped $Ga_{0.51}In_{0.49}P$ "buffer," considered to be where defects are grown out of the III-V material and therefore highly defective, bridges the heteroepitaxial interface between the Si wire bottom cell and the III-V top cell structure. The different components of the tandem device can be seen clearly in the band diagram (bottom right).

known values for $In_{0.49}Ga_{0.51}P$ and GaP to match the bandgap to the absorption onset for the direct and indirect bandgap alloys, respectively (Figure 4.2). Furthermore, Sentaurus Device also automatically interpolates the other materials properties of the alloy layers.

The simulated geometry is depicted in Figure 4.3, and the details of the layers are in Table 4.2. The graded buffer layers were assumed to be relatively defective and to have a low τ_{SRH} = 1 ps. The indirect-direct transition can also be seen in the band diagram of the device in Figure 4.3. At the transition, the density of states at the band edge changes abruptly,

Layer	Material	Thickness	Doping (cm^{-3})
Antireflection coating	MgF	95 nm	
	TiOx	55 nm	
Window	$Al_{0.5}In_{0.5}P$	30 nm	$n = 2.0 \times 10^{18}$
Emitter	$Ga_{0.51}In_{0.49}P$	50 nm	$n = 2.0 \times 10^{18}$
Base	$Ga_{0.51}In_{0.49}P$	700 nm	$p = 1.2 \times 10^{17}$
Back surface field	$Ga_{0.51}In_{0.49}P$	100 nm	$p = 4.0 \times 10^{17}$
Tunnel junction	$Ga_{0.51}In_{0.49}P$	15 nm	$p = 1.0 \times 10^{19}$
	$Ga_{0.51}In_{0.49}P$	15 nm	$n = 1.8 \times 10^{18}$
Buffer	$Ga_{0.51}In_{0.49}P$	500 nm	$n = 1.8 \times 10^{18}$
Wire emitter	Si	Gaussian, 5 μm tall radial junction	$n = 1.0 \times 10^{19}$
Wire base	Si	40 μm height, 5.3 μm pitch	$p = 1.0 \times 10^{17}$
Back reflector	Perfect electrical conductor		

TABLE 4.1: Layer parameters for simulated wire array tandem device

leading to a change in the conduction band and valence band offset between the indirect and direct alloy.

4.2.4 Planar tandem with a graded buffer

To aid in interpreting the simulation results, a planar version of the tandem wire device with a graded buffer was considered. It is important to note that direct comparison of structured layers with planar layers is not always straightforward – often it is best to renormalize the thickness of the planar layers such that the total volume of material is conserved. As seen with the previous set of simulations, the need to "filter" the spectrum with the top cell before allowing any light to interact with the bottom cell necessitates near close-packing of the top cell material.

In this study, layers of identical thickness are considered for both the planar and wire array case. The planar Si wafer is assumed to have a thickness of 250 μm for full light absorption.

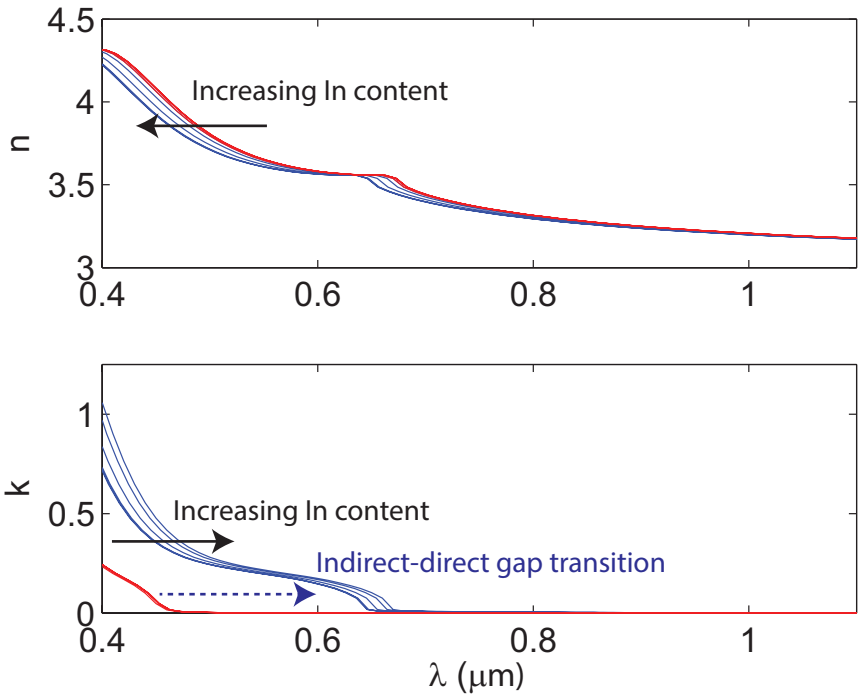


FIGURE 4.2: Interpolated complex refractive indices for $Ga_{1-x}In_xP$ alloys. The indirect alloy indices were generated by shifting the absorption onset of GaP to match the expected bandgap of the alloy, and the direct gap alloy indices were generated by doing the same with $In_{0.49}Ga_{0.51}P$.

In comparison, the Si wire arrays are merely 40 μm tall, which is not enough to absorb the entirety of the solar spectrum.

4.3 Results of optical simulations

4.3.1 Optical response of wire array devices

The case of the highly mismatched growth on a Si wire will be considered first. Generation profiles for AM1.5G illumination were computed by simulating the 2D device behavior under illumination by a plane wave of different wavelengths between 400 and 1100 nm in 50

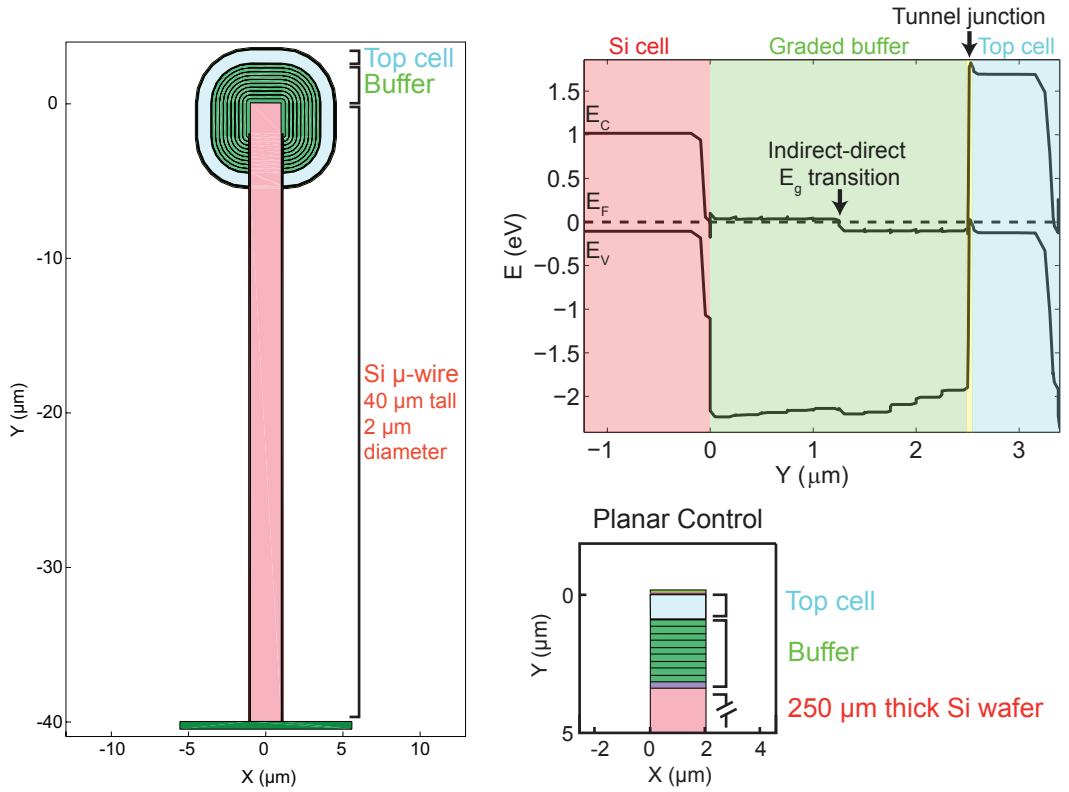


FIGURE 4.3: Modelled device geometry for a wire array tandem device utilizing graded buffer growth (left). The band diagram of the device (top right) is identical to that for the planar control (bottom right).

nm increments at normal incidence (Figure 4.4). Appropriate weighting parameters from a binned AM1.5G spectrum were applied to each of the simulated wavelengths to create optical generation profiles (Figure 4.5).

For the case of the graded buffer on a Si wire, reflection and absorption results from the single wavelength simulations are plotted in Figure 4.5b. The persistence of absorption in the step graded buffer suggests that increasing the top cell thickness should yield additional current that is currently lost to the buffer and the bottom cell. Also, off-normal incidence could yield higher absorption as observed in the case of Si μ-wire arrays.

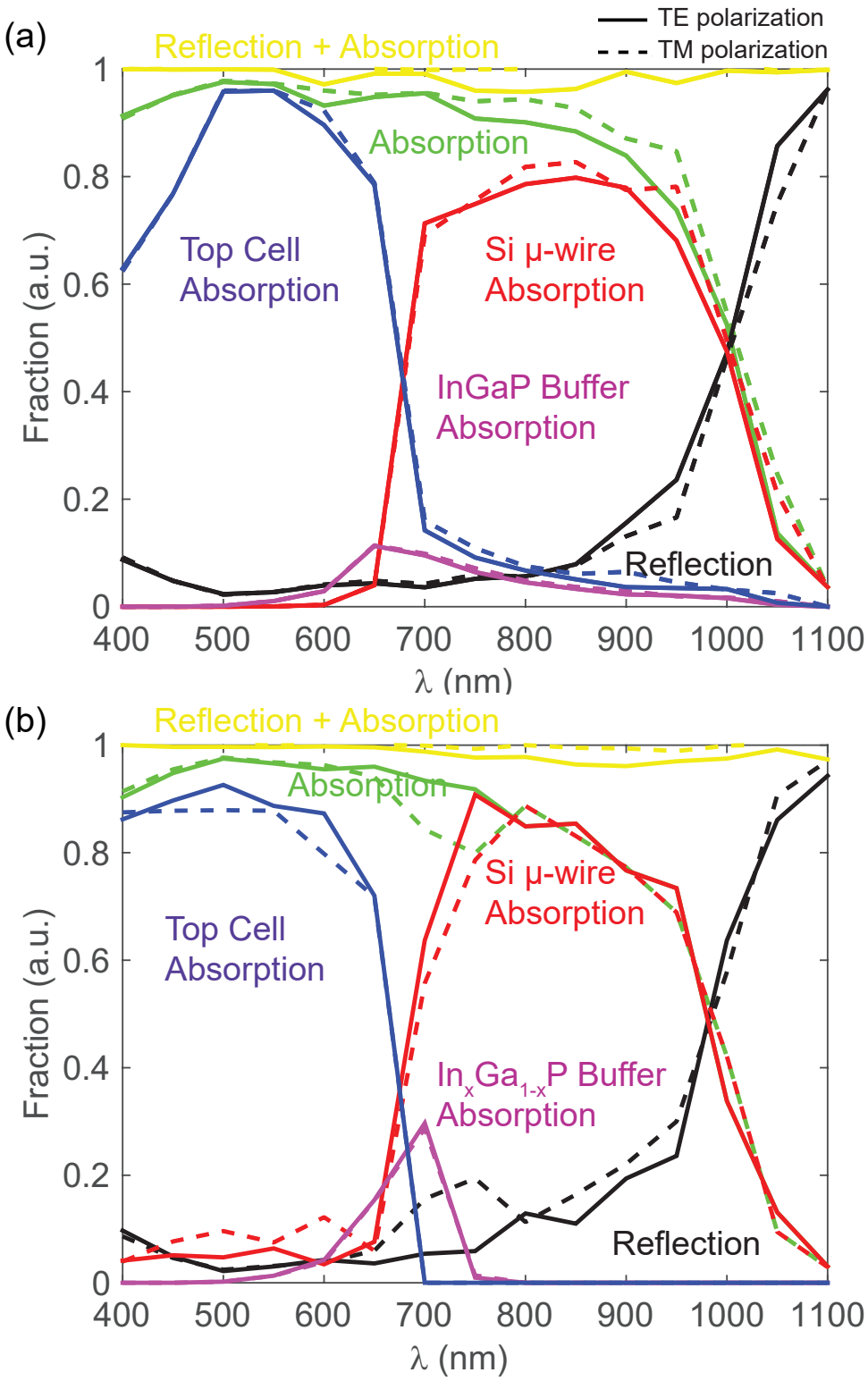


FIGURE 4.4: Fraction of light reflected and absorbed in different parts of the (a) highly mismatched and (b) graded buffer tandem device stacks under TE and TM (solid and dashed, respectively) polarized plane wave illumination.

Layer	Material	Thickness	Doping (cm^{-3})
Antireflection coating	MgF	95 nm	
	TiOx	55 nm	
Window	$Al_{0.5}In_{0.5}P$	30 nm	$n = 2.0 \times 10^{18}$
Emitter	$Ga_{0.51}In_{0.49}P$	50 nm	$n = 2.0 \times 10^{18}$
Base	$Ga_{0.51}In_{0.49}P$	700 nm	$p = 1.2 \times 10^{17}$
Back surface field	$Ga_{0.51}In_{0.49}P$	100 nm	$p = 4.0 \times 10^{17}$
Tunnel junction	$Ga_{0.51}In_{0.49}P$	15 nm	$p = 1.0 \times 10^{19}$
	$Ga_{0.51}In_{0.49}P$	15 nm	$n = 1.8 \times 10^{18}$
Buffer	$Ga_{0.55}In_{0.45}P$	250 nm	$n = 1.8 \times 10^{18}$
	$Ga_{0.60}In_{0.40}P$	250 nm	$n = 1.8 \times 10^{18}$
	$Ga_{0.65}In_{0.35}P$	250 nm	$n = 1.8 \times 10^{18}$
	$Ga_{0.70}In_{0.30}P$	250 nm	$n = 1.8 \times 10^{18}$
	$Ga_{0.75}In_{0.25}P$	250 nm	$n = 1.8 \times 10^{18}$
	$Ga_{0.80}In_{0.20}P$	250 nm	$n = 1.8 \times 10^{18}$
	$Ga_{0.85}In_{0.15}P$	250 nm	$n = 1.8 \times 10^{18}$
	$Ga_{0.90}In_{0.10}P$	250 nm	$n = 1.8 \times 10^{18}$
	$Ga_{0.95}In_{0.05}P$	250 nm	$n = 1.8 \times 10^{18}$
	GaP	250 nm	$n = 1.8 \times 10^{18}$
Wire emitter	Si	Gaussian,5 μm tall radial junction	$n = 1.0 \times 10^{19}$
Wire base	Si	40 μm height, 5.3 μm pitch	$p = 1.0 \times 10^{17}$
Back reflector	Perfect electrical conductor		

TABLE 4.2: Layer parameters for simulated wire array tandem device

4.3.2 Comparison of optical generation

A map of the optical generation was calculated by weighted integration of the contributions from each single wavelength simulation to match the AM1.5G solar spectrum (Figure 4.5). Light is focused into the Si μ-wire core by the III-V cladding, and the indirect gap $Ga_{1-x}In_xP$ alloys can be easily identified as the regions with lower generation rates.

By integration in each region of the device, optical generation currents can be calculated and compared to the spectral current window available to each cell material and the planar control (Table 4.3). Optical generation for the planar control was calculated using the

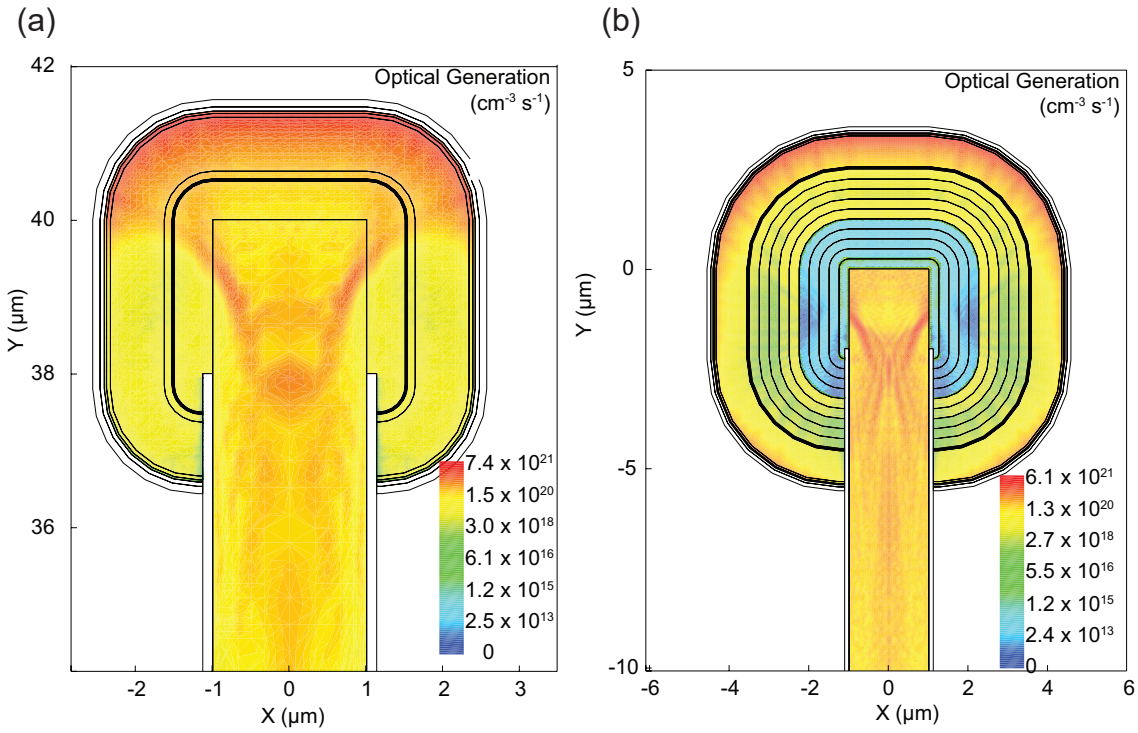


FIGURE 4.5: Optical generation profiles generated by integration of single wavelength simulations and weighting to match the AM1.5G spectrum.

	Si	Buffer	Top Cell
Spectrum	25.3	–	16.9
Mismatched growth	16.2	1.6	14.2
Graded buffer	15.5	0.77	12.8
Planar	21.3	0.36	16.5

TABLE 4.3: Optical generation current in mA cm^{-2} of the spectral windows for each cell and integrated from the simulated optical generation maps for the wire and planar geometries.

transfer matrix method. Clearly, the amount of generated current in the wire geometry is inferior for both the top and bottom cell compared to the planar geometry. For the Si bottom cell, the difference in optical generation current is a consequence of the small volume of absorber material in the wire geometry. The difference in the top cell is somewhat unexpected. The current hypothesis is that the rounded edges of the top cell reduce the performance of the antireflection coating. The ARC was designed for normal incidence light, and the rounded edges effectively change the incidence angle. However, attempts to further optimize the cell by adjusting the thickness of the top cell absorber layer were hindered by the additional computational complexity.

4.4 Results of device simulations

4.4.1 Highly mismatched growth on a Si wire

Of particular interest are the effects of minority carrier SRH lifetime (τ), which is a proxy for material quality, and carrier mobility, which is negatively affected by defects in the growth of these materials. The surface recombination velocities (SRV's) of all interfaces were set to 100 cm/s to limit their effect on device performance. With these conditions, the tandem structure considered is capable of exceeding 20% efficiency over a wide range of lifetime values (Table 4.4), with an upper limit of 22.88% efficiency with good material quality, $\tau_{SRH} = 1$ ns. Furthermore, efficiencies greater than the predicted 17% for Si wire arrays alone are possible at sub-100 ps lifetimes.

Top cell τ_{SRH}	10 ps	100 ps	1 ns	10 ns
Fill factor (%)	76.86	84.38	86.87	88.86
V_{oc} (V)	1.657	1.778	1.876	1.912
J_{sc} (mA cm^{-2})	12.98	14.04	14.04	14.04
Efficiency (%)	16.53	21.06	22.88	23.85

TABLE 4.4: Simulated highly mismatched growth tandem device performance as a function of top cell SRH lifetime

More realistic surface recombination physics was introduced to the device simulations to better predict experimental performance. These simulations assumed 1 ns top cell SRH lifetime. The Si/SiOx interface is assumed to be well understood and reasonably passive (SRV = 100 cm/s). Several interfaces within the device stack could detract from device performance. The GaInP/SiOx interface, resulting from III-V growth out and over a portion of the SiOx, is purely a result of wire geometry and cannot be passivated in-situ. Other than the Si/SiOx interface, the SRV at each of the interfaces was changed from 100 to 10^4 cm/s. The efficiency of the structure dropped from 22.88 to 22.84%. The minimal effect of these large changes in SRV can be explained in part by the band structure, whereby minority carrier barriers, at the front surfaces of both cells and also at the back surface of the top cell, help reduce recombination statistics by repelling minority carriers. However, this does not explain the insensitivity to the 850 nm long interfaces on either side of the wire between the top cell GaInP and SiOx. Instead, the difference could be due to the greater portion of the optical generation (Figure **??**) occurring away from this interface as light is guided into the wire core by the higher index top cell material.

4.4.2 Comparison of graded buffer growth on a Si wire and planar cell

The results of the optical simulations were then coupled into a finite element Poisson equation solver. Identical materials parameters were utilized for the wire array and planar geometries. For both the wire and planar cases, τ in the Si was set to 1 μs, a realistic value for the Si μ-wires. For the buffer layers, τ was set to 1 ps. Surface recombination velocities are summarized in Table 4.5.

For the 1 ns top cell lifetime case, the LIV measurements indicate a very slim performance advantage for the wire versus planar geometry (Figure 4.6 and Table 4.6). As expected from the optical generation currents, the single junction performance of the top and bottom cells are quite different between the two geometries. Most strikingly, the Jsc of the wire bottom cell is much higher than that of the planar cell despite a much lower volume of material

Material 1	Material 2	SRV (cm s^{-1})
Si	SiO_2	20
Si	$Ga_{1-x}In_xP$	200
$Ga_{1-x}In_xP$	$Ga_{1-x}In_xP$	1.5
$Ga_{1-x}In_xP$	AlInP	100 [64]
$Ga_{1-x}In_xP$	SiO_2	10^4 [8]
AlInP	TiOx	10^4

TABLE 4.5: SRV's assumed in device simulations

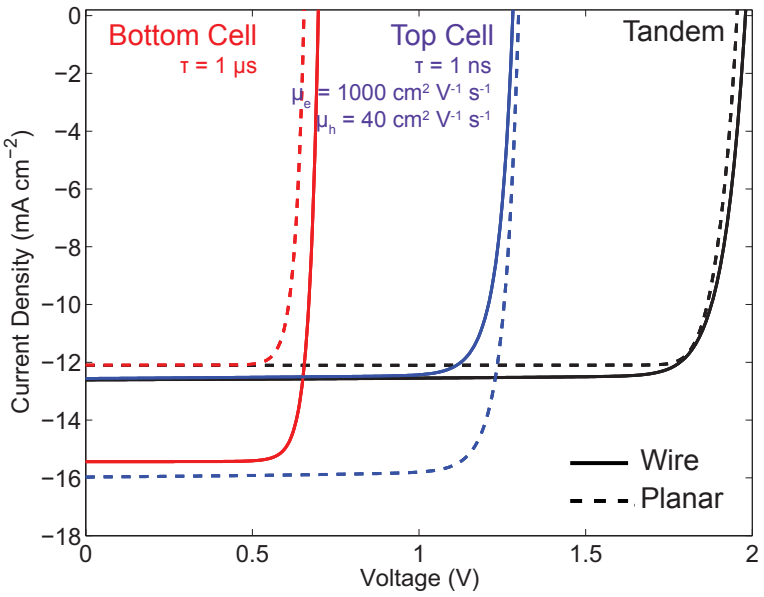


FIGURE 4.6: Comparison of LIV curves for simulated wire and planar devices operated in tandem and single junction configurations.

	Jsc (mA cm^{-2})	Voc (V)	FF (%)	η (%)
Wire tandem	12.61	1.981	85.90	21.5
Top cell	12.56	1.283	83.99	13.5
Bottom cell	15.44	0.698	83.60	9.0
Planar tandem	12.11	1.956	89.76	21.3
Top cell	15.98	1.300	84.18	17.5
Bottom cell	12.10	0.655	83.62	6.6

TABLE 4.6: Summary of PV figures of merit from simulated LIV measurements of wire and planar devices in tandem and single junction configuration.

and lower optical generation overall (Table 4.3), a testament to the advantages of the radial junction with relatively low (1 μs) minority carrier SRH lifetime.

To evaluate the effect of top cell material quality, both the minority carrier SRH lifetime and mobility in the top cell absorber material were varied (Figure 4.7). Notably, the wire geometry allows for higher short circuit current (Jsc) and open circuit voltage (Voc), but lower fill factors lead to lower efficiencies except for $\tau = 1$ ns. Since the wire device is top cell current limited, the effect of reducing the minority carrier lifetime is more pronounced compared to to the bottom cell limited planar case. The lower fill factors overall could be a consequence of increased junction area. The majority and minority carrier mobilities assumed for each case are shown in Table 4.7. As the mobility is decreased, the wire arrays possess higher Jsc's and Voc's, but the reduced FF results leads to little to no efficiency advantage.

Case	μ_e (cm^2 V^{-1} s^{-1})	μ_h (cm^2 V^{-1} s^{-1})
A	1000 [74]	40 [29]
B	500	20
C	100	4

TABLE 4.7: Carrier mobilities assumed in device simulations for Figure 4.7.

4.5 Conclusions

Despite a desire to realize a high performance tandem wire array solar cell design, the conclusion of the efforts so far points to a challenging route for higher efficiencies than planar geometries. In particular, the combination of a desire to replicate experimentally achieved geometries and the computational complexity of the wire array designs limited the optical design and ultimate performance of the tandem device designs. More radical designs will be needed in order to realize higher efficiencies. One important and straightforward result is that the reduced absorption requirements of the tandem device allows the use of shorter wire arrays without additional optical elements. This reinforces the need to use

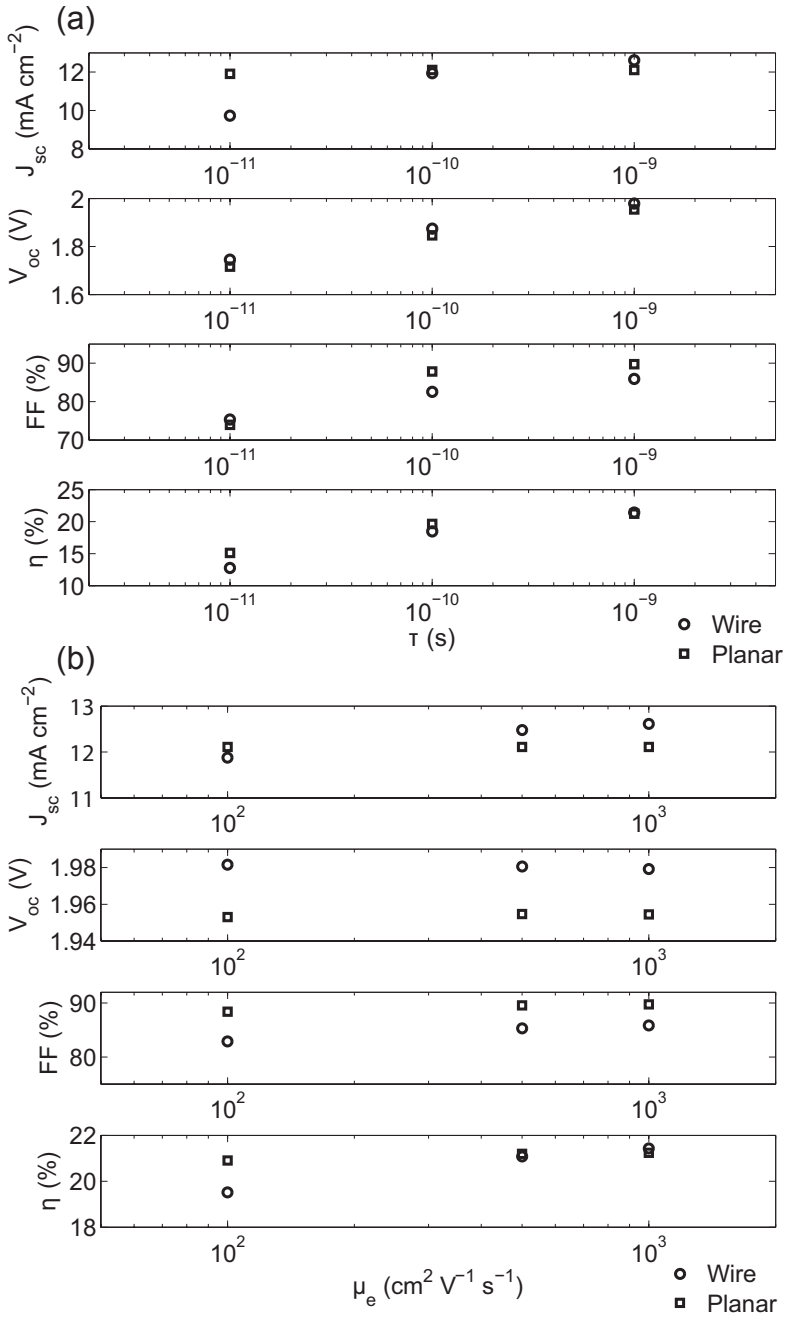


FIGURE 4.7: Simulated performance of wire and planar tandem devices as a function of (a) SRH lifetime and (b) minority carrier mobility.

optoelectronic modelling for design of structured tandem and multijunction solar cells, as the light trapping characteristics of single junction cells can be greatly relaxed with the spectral filtering offered by a multijunction design.

Chapter 5

MOCVD of GaP on Si for c-Si photovoltaics

Gallium phosphide is an ideal starting point for the integration of Group III-V compound semiconductor materials on Si. GaP and Si are almost lattice matched, allowing for a minimal introduction of mismatch related defects. However, the primary limitation of GaP is a large indirect bandgap and poor light absorption characteristics as a result, making it less useful as an active absorber layer. Despite, this, there are two potential routes towards increasing the efficiency of c-Si photovoltaics.

First, GaP can be used as a heterojunction partner for c-Si, serving as a "carrier-selective contact" [48]. Si heterojunction solar cells based on a-Si hold the world records for single junction Si cell efficiency and open circuit voltage. GaP has less parasitic light absorption, lower sheet resistance, and a larger bandgap than a-Si, but in order to realize these superior attributes, device designs must maintain an extremely well passivated surface, which for a-Si on Si results in surface recombination velocities < 1 cm/s and is the root of the demonstrated record open circuit voltages. Simulations of n-GaP/p-Si heterojunctions have demonstrated the capability to hit $> 26\%$ efficiency [46].

Second, GaP can be used as a virtual substrate for the epitaxial growth of a direct gap, highly lattice mismatch InGaP or GaAsP top cell directly on Si. Commercially realized "metamorphic" designs incorporate step-graded buffers to relieve strain sequentially through a series of thick, high bandgap layers [17], and this design can also be implemented on Si if an appropriate GaP virtual substrate is found [22].

In both of these cases, there is a present need for low defect density, high electronic quality growth. This chapter presents our results for GaP growth on (112) oriented Si with MOCVD. A two-step pulsed low temperature nucleation and continuous high temperature growth process developed for the (001) orientation allows us to grow GaP thin films of reasonable quality on both (112) and (001) orientations of Si. In particular, the films grown on (112) are smoother and have high crystalline quality as characterized by x-ray diffraction. Transmission electron microscopy of thin and thick films do not show evidence of antiphase domain formation. Microtwin and stacking fault defects are present in the films, likely a result of a non-ideal nucleation recipe. Further optimization of this growth could lead to high quality GaP virtual substrates on Si for integration of other Group III-V optoelectronic devices.

5.1 Background

5.1.1 Polar on non-polar defects

If we consider a hypothetical Si surface during homoepitaxial growth, any Si atom that makes it to the surface can bind to the surface without any consequences on the symmetry of the lattice. Furthermore, while it may be energetically favorable for the Si to bind to specific sites on a given surface, the exact configuration of these sites and the order in which they are filled have minimal consequences as long as no "empty" sites are left as voids in the material – in other words, the Si atoms are indistinguishable. In contrast, if for the same hypothetical Si surface we now consider the growth of GaP, the Ga and P atoms are

distinguishable, and their relative position to one another influences the crystal symmetry and local bonding. The "polar-on-nonpolar" defects important in GaP growth on Si fall into two categories – stacking errors, where the ordering of the crystal planes as they are stacked upon one another is changed, and anti-site defects, where, for instance, a Ga atom occupies a site that should typically be for a P site or vice versa.

Stacking errors in polar on non-polar growth manifest along the close-packed crystal planes in materials. To illustrate this, we can consider the face-centered cubic and hexagonally close-packed lattices. They can both be constructed by stacking hexagonally close packed spheres. The three non-equivalent stacking locations can be arranged in the order ABCABCBAC yield the face-centered cubic lattice. Stacking faults result from the addition or removal of extra planes in the stacking process, *e.g.* ABCAABC or ABABCABC. Twin defects are mirror planes in the stacking process (ABCABCBACBA). Both of these defects are commonly seen in the growth of GaP on Si [55].

Antiphase defects occur when two domains with different polarities grow together, resulting in non-ideal bonding arrangements, *i.e.*, Ga-Ga and P-P bonding. These domains interact strongly with dislocations, pinning dislocation motion and causing dislocation multiplication, thus reducing the electronic quality of lattice mismatched material. Efficient strain relaxation in growth of GaP/GaAs on Si/Ge was found to be greatly impeded by antiphase domains [24, 55], which serve to pin misfit dislocation motion and lead to dislocation multiplication [41]. Furthermore, the antiphase boundaries, due to their energetically unfavorable bonding, are high energy boundaries that should have significant effects on the electronic structure at interfaces. This should result in the formation of deep electronic level trap states and reduce carrier mobility [37]. For the standard (001) orientation, antiphase domains were found to form due to the presence of single atomic steps, each of which shifts the crystallographic relationship between two domains by 1/4 of a unit cell, leading to the characteristic Ga-Ga or P-P/As-As bonding of an antiphase domain boundary.

5.1.2 Solving the polar on non-polar problem

For the reasons outlined earlier, many researchers became interested in the integration of GaP and, more notably, GaAs on Si and Ge substrates in the early 1980s. Two notable approaches emerged: to use a substrate orientation other than (001) or to use a heavily offcut (4-6°) (001) substrate [38]. Ultimately, growth on heavily offcut (001) substrates won out [40], and the development of antiphase domain free GaAs on Ge began in earnest.

While the challenge of integrating GaAs on Ge is a solved problem, several outstanding issues complicate the growth of GaP on Si. First, the lattice mismatch and coefficient of thermal expansion mismatch are much greater for GaP and Si compared to GaAs and Ge, leading to a lattice mismatch of 0.36% at 300K and $\geq 0.50\%$ at relevant growth temperatures compared to 0.12%. Second, the Ge surface reconstruction can be manipulated at much lower growth temperatures compared to Si, where by annealing at 640 °C in UHV can yield double-stepped Ge (001) surfaces [76], while temperatures of $\geq$ 760 °C are necessary for realizing a double-stepped Si (001) surface [20].

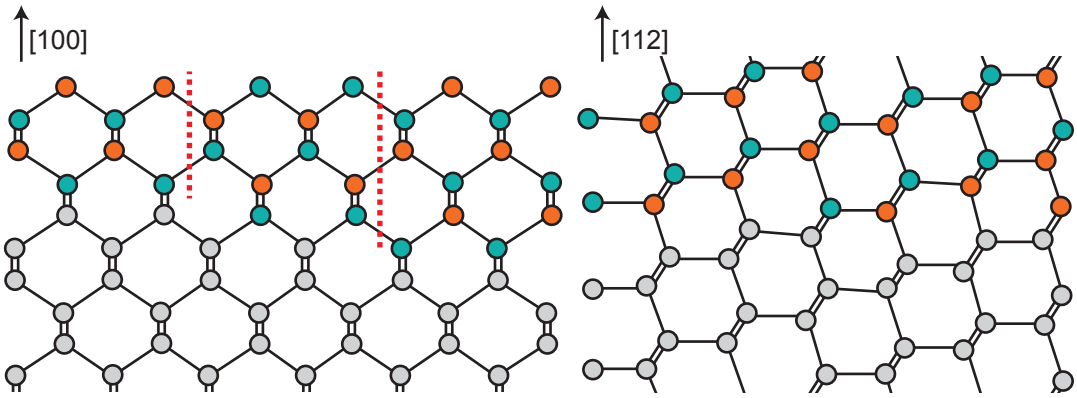


FIGURE 5.1: Schematic comparison of APD formation during GaP growth on single steppedSi (001) and (112). Antiphase boundaries marked in red. Based on [38].

By carefully preparing an offcut (001) surface, virtually all of the steps present will be two atomic layers tall, a strategy which has been employed with great success for growth of

GaAs on Si and Ge [38]. Recently, several groups have made major strides in the integration of GaP on Si (001) substrates [9, 20, 21, 47, 77, 88]. These groups utilize careful surface preparation, including in-situ growth of Si, high temperature annealing to recover a double-stepped surface reconstruction and a carefully tuned pulsed nucleation scheme. Grassman *et al.* were able to demonstrate complete elimination of all nucleation related defects, achieving high quality templates for further Group III-V compound semiconductor growth with both molecular beam epitaxy [20] and metalorganic chemical vapor deposition (MOCVD) [21, 88]. Another approach for eliminating antiphase domain formation is to grow on orientations where their formation is not favored [39]. Kroemer *et al.* postulated that growth on (112) orientations should be free of antiphase domains due to a difference in the bonding preferences of Group III and Group V atoms on the surface [38]. To this end, they demonstrated antiphase domain-free GaP and GaAs on Si (112) [87, 95]. This strategy appears to have been superseded after discovery of high quality GaAs growth on double-stepped Ge (001) [40].

5.2 Experimental details

5.2.1 Sample preparation

In this study, thin films were grown on (112) and (001) oriented substrates for comparison purposes. The (112) oriented wafers were nominally on axis, while the (001) oriented wafers were intentionally offcut 6° towards the [111] direction to encourage double step formation. Wafers were cleaved into nominally 1 × 1 cm pieces using a scriber-breaker tool to allow for growth on up to four substrates in a single process run using a 3 in. quartz wafer with laser-cut holes. Prior to growth, substrates were sonicated in water, acetone, isopropyl alcohol, and water to remove any particulate contamination or residue from wafer handling. Following the degreasing step, substrates were sequentially etched in RCA 1 (1:1:5 NH_4OH, H_2O_2, H_2O, 75 °C) and RCA 2 (1:1:6 HCl, H_2O_2, H_2O, 75 °C) for 10 minutes each to remove residual organic and metallic contamination. Immediately before loading into the

N2 purged reactor glovebox, substrates were etched in 6:1 Buffered Oxide Etch (Transene Company, Inc.) to remove the clean surface oxide. X-ray photoelectron studies of substrates cleaned and transferred in vials sealed in the nitrogen-purged reactor glovebox with minimal exposure to air only during mounting on the XPS chuck did not show significant trace chemical contamination.

5.2.2 Growth conditions

Prior to growth, substrates were annealed at 750 °C for 5 minutes before being cooled to the nucleation temperature. The low temperature (450 °C) pulsed nucleation scheme consisted of steps by which TEG and TBP were introduced intermittently into the chamber in a fashion akin to atomic layer epitaxy. The TEG pulse was calibrated by performing 80 cycles of pulsed growth and fitting x-ray reflectometry data [57] and comparing to the expected 4 unit cell thickness on the (001) orientation. All of the films grown in this work used cycles consisting of a 5 s pulse of TEG at 12.7 μmol min^{-1}, followed by a 10 s pulse of TBP at 3205 μmol min^{-1} and a 15 s purge. Thin film growth was initiated with 20 cycles of pulsed, low temperature growth, heated to 575 °C under TBP flow, and capped with traditional continuous growth. Growth rates of 0.6 μm h-1 were achieved with TEG and TBP molar flow rates of 63.5 and 3205 μmol min^{-1} for a V/III ratio of 50.5. A homoepitaxial Si capping layer, found to be essential in minimizing or eliminating defect formation in growth of GaP on Si (001) substrates [20, 88], was not grown due to reactor limitations.

5.3 Results

5.3.1 Initial results with TMGa

In parallel with our growth efforts on coating Si microwire arrays with GaP, planar reference samples were grown on Si wafers with (001), (111), (011), and (112) orientations. (001)

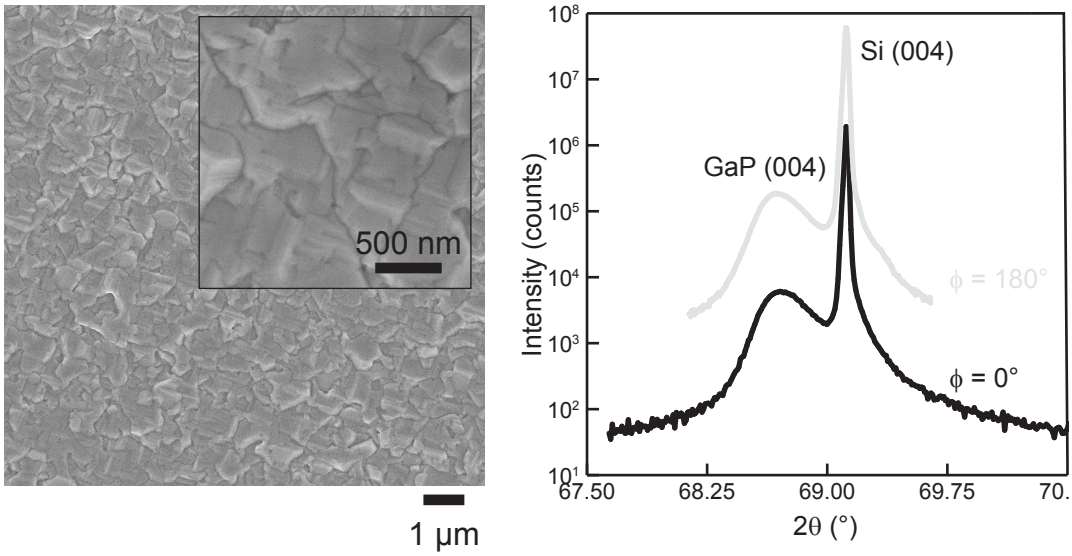


FIGURE 5.2: Representative SEM image (left) and x-ray rocking curves (right) for a planar GaP thin film grown using the microwire array coating growth recipe and TMGa.

was chosen for ease of comparison to literature results, while (111) was chosen as it is nominally the top surface of the microwire array. (011) and (112) are the sidewall facets of the wires. Since our focus was on developing an understanding of the growth on the wire arrays, a majority of the characterization efforts were directed towards coated wires. Figure 5.2 depicts some representative results from the wire array growth recipe being applied to a planar GaP layer on Si (001). The layers are clearly growing three-dimensionally, with multiple crystals growing together after nucleation. Despite the polycrystalline appearance, they are in fact epitaxial, but with some texturing associated with the alignment between crystals. High quality GaP thin films were not achieved with the wire array coating growth recipes.

5.3.2 Optimization of GaP nucleation layer

Optimization of the growth procedure for planar thin films began after a helpful conversation with Dr. Tyler Grassman at the IEEE Photovoltaics Specialists Conference in 2013. In a

conversation with him, he mentioned that both they and the groups based out of Phillipps University Marburg had no success with ALE nucleation in the MOCVD until they switched to TEGa from TMGa. My personal hypothesis is that the larger molecular weight and therefore lower vapor pressure of TEGa allows for better control of the Ga deposition on the wafer surface.

The second important change was a calibration of the MOCVD surface temperature using the Al-Si eutectic, following the procedure laid out in Mizutani [53]. This calibration method takes advantage of the large emissivity of the Al-Si eutectic versus an Al thin film. As the eutectic forms at precisely 580 °C, the actual surface temperature can be inferred from a pyrometer reading by heating the surface through the transformation. In the MOCVD reactor, the temperature of the susceptor is feedback controlled via a thermocouple mounted in the center of an annular graphite heater mounted directly below the susceptor. A pyrometer is mounted vertically above the reactor with line of sight to the sample surface through a quartz window.

1. A Si wafer with 100 nm of Al is loaded into the reactor.
2. The setpoint temperature of the thermocouple is raised to near the eutectic transition.
3. The setpoint temperature is raised slowly through the eutectic transition while the setpoint and pyrometer temperatures are recorded.
4. The eutectic transition is assumed to occur when the apparent surface temperature of the sample increases abruptly.
5. The difference between the Au-Si eutectic temperature (580 °C) and the pyrometer measured surface temperature of a bare Si wafer at the eutectic transformation is applied as a correction factor for all pyrometer measured Si surface temperatures.

Figure 5.3 depicts the results of the temperature calibration. The eutectic transformation happens at $\sim$ 509 °C, a full 71 °C lower than what was expected. As such, all of growth done with TMGa had surface temperatures $\sim$ 71 °C hotter than what we were expecting.

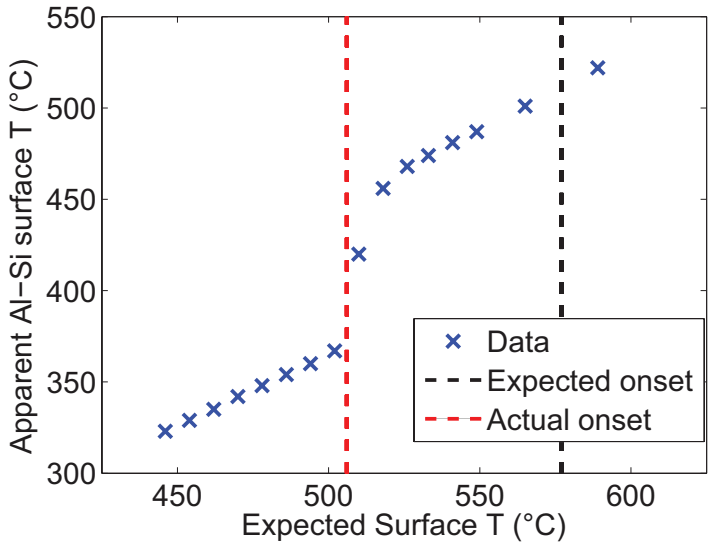


FIGURE 5.3: Pyrometer measured apparent surface temperature of a thermally evaporated 100 nm thick Al film deposited on Si wafer versus pyrometer measured apparent surface temperature of a bare Si wafer.

The combination of changing to TEGa and calibrating the pyrometer temperature reading led to a dramatic improvement in the quality of the films grown (Figure 5.4). Instead of rough, three-dimensional growth, the films coalesce and grow in a more two-dimensional fashion.

The nucleation layer thickness was further optimized by growing thicker films with ALE to allow for easy measurement by x-ray reflectometry (XRR). A total of 80 cycles of ALE were performed to optimally yield 40 monolayers of GaP on Si (001). The molar flow of TEGa was adjusted while the exposure time was held constant to vary the total Ga coverage. After deposition, the thickness of the films was measured with XRR and fit using MOTOFIT [57] with calculated values of the scattering length density for Si and GaP from the NIST Center for Neutron Scattering neutron activation and scattering calculator[1]. Fitting was accomplished by first adjusting the scale and background factors to match the onset and

[1]http://www.ncnr.nist.gov/resources/activation/

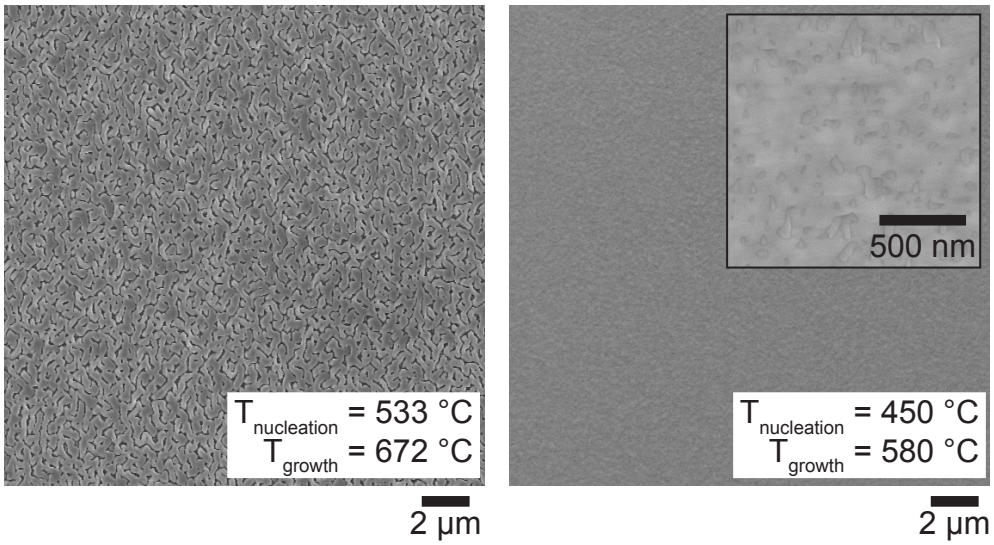


FIGURE 5.4: SEM images of GaP thin films grown before (left) and after (right) temperature calibration.

then allowing the thickness to be fit. The final fitting was accomplished by setting the scale, background, thickness, and scattering length densities as free parameters.

5.3.3 Optimized nucleation and thin film morphology

Thin films comprising only the nucleation layer and $\sim$ 50 nm growth were grown on Si (112) and (001) offcut 6° towards [111] substrates simultaneously. As mentioned earlier, the nucleation layer was optimized to yield an appropriate thickness for 10 unit cells on (001) oriented substrates. Atomic force microscopy was used to image and characterize the surfaces of the films (Figure 5.6). Nucleation of GaP on the (112) orientation leads to a rough nucleation layer with 3.7 nm RMS roughness (Figure 5.6a), likely due to the lack of optimization for this surface orientation, but the $\sim$ 50 nm thick film, having experienced both the low temperature pulsed nucleation and high temperature continuous growth, is actually smoother with a reduced RMS roughness of 0.5 nm (Figure 5.6b). In contrast, optimized nucleation of GaP on Si yields 1.5 nm RMS roughness on (001) oriented substrates,

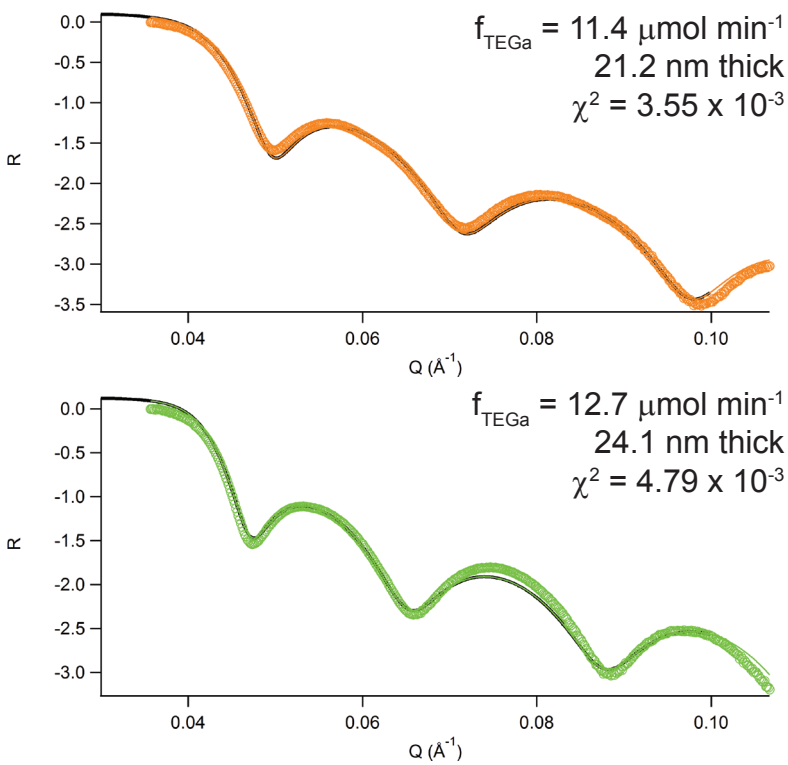


FIGURE 5.5: XRR curves for 80 ALE cycles with two TEGa molar flows and fitting results from MOTOFIT.

and subsequent high temperature growth for a total of $\sim$ 50 nm layer thickness preserves the RMS roughness of the nucleation layer (Figure 5.6c,d). The topography of the $\sim$ 50 nm thick film on (001) has pits with surface protrusions consistent with literature reports of films containing antiphase domain defects.16 As surface features and roughness are closely correlated with defects in epitaxially grown films, the relative smoothness of the films grown on (112) motivated further exploration of the crystalline quality.

5.3.4 X-ray diffraction of GaP on Si

Films grown on both orientations were epitaxial with respect to their substrates as characterized by high resolution x-ray diffraction (Figure 5.7). X-ray spectra show single orientation growth for both orientations as shown in Figure 5.7a,b. Reciprocal space mapping was

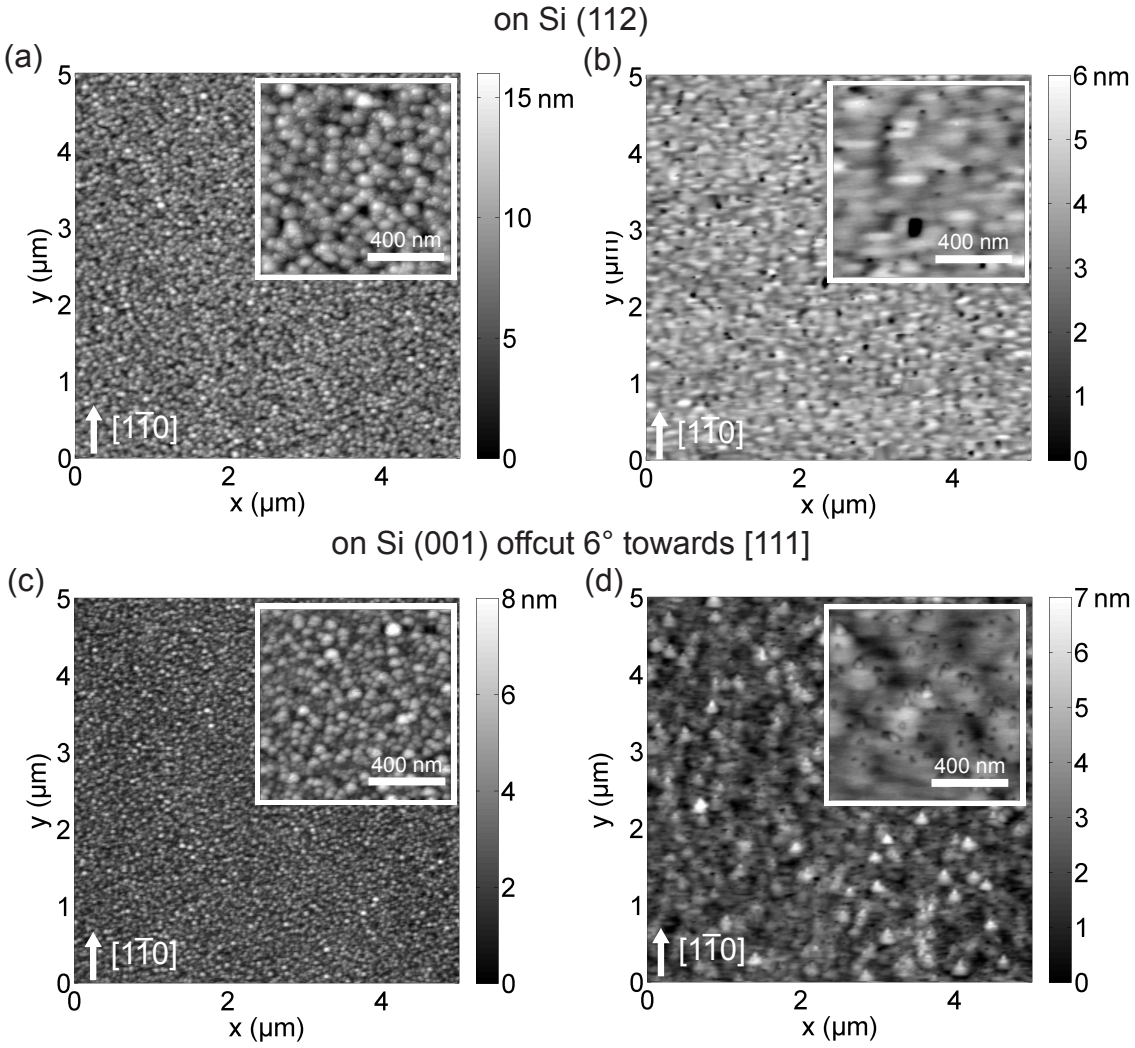


FIGURE 5.6: Atomic force microscopy topography maps of low temperature, pulsed nucleation (a) and subsequent high temperature continuous growth of a 50 nm thick film (b) show the growth of high quality thin films on Si (112). Analogous images of growth on Si (001) offcut 6° towards [111] are shown in (c) and (d).

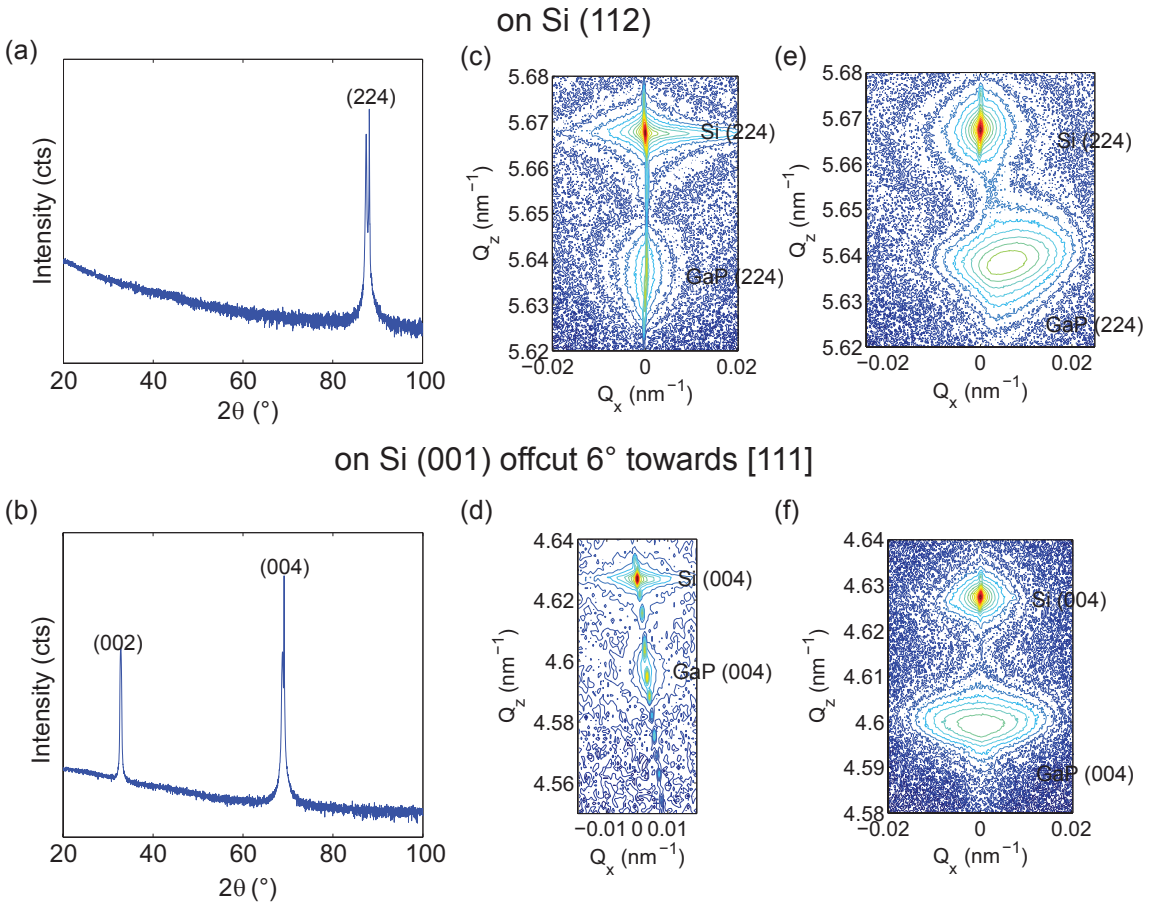


FIGURE 5.7: High resolution x-ray diffractometry of films grown on Si (112) and Si (001) offcut 6° towards [111] substrates. (a), (b) x-ray diffraction spectra of $\sim$ 200 nm thick films. The amorphous background is due to the use of a glass slide onto which the 1 $\times$ 1 cm sample is mounted. (c), (d) reciprocal space maps of $\sim$ 50 nm thick films. (e), (f) reciprocal space maps of $\sim$ 200 nm thick films.

utilized to extract detailed information about the strain state and defect density in these films. Mapping of $\sim$ 50 nm thick films revealed single substrate peaks with Pendellösung oscillations present in scans of the symmetric (224) and (004) substrate and layer peaks on the (112) and (001) oriented substrates, respectively (Figure 5.7c,d). The layer peak for the thin film grown on vicinal (001) has a full width half maximum of 36 arcseconds in the ω direction, matching the width of the substrate peak, and the layer peak for the thin film grown on (112) has a wider full width half max of 12 arcseconds, almost identical to that of the substrate (11 arcseconds). These results are indicative of low crystallographic defect density in these films. When the incident beam is aligned on the [011] direction, the (001) oriented film exhibits a 0.32° tilt, consistent with literature results [82]. Asymmetric reciprocal space maps for these films show that these films are not relaxed on both orientations, consistent with a thickness below the critical thickness for GaP on Si.

Reciprocal space mapping was also employed for much thicker films on the order of 200 nm in thickness. Symmetric maps (Figure 5.7e,f) show layer peak ω full width half maxima of 345 arcseconds for growth on (112) versus 460 arcseconds for growth on vicinal (001). GaP grown on (112) is fully relaxed along the surface parallel [110] and [111] orthogonal directions by comparing the peak position of the (044) and (333) asymmetric layer and substrate peaks. Full relaxation along these directions is important, as partial relaxation along the [110] direction has been observed in strained layer superlattices grown on (112) due to the primary slip system acting only on stress in the [111] direction [52]. GaP grown on (001) offcut 6° towards [111] is only 96% relaxed, likely due to antiphase domains pinning misfit dislocation motion.13 These promising results for thin films grown on (112) oriented Si motivated further investigation with transmission electron microscopy.

5.3.5 Transmission electron microscopy

Cross sections of $\sim$ 50 nm thick layers grown on both Si orientations were prepared for transmission electron microscopy analysis (Figure 5.8). Particular emphasis was placed on determining the presence of antiphase domain defects. Bright field and dark field images

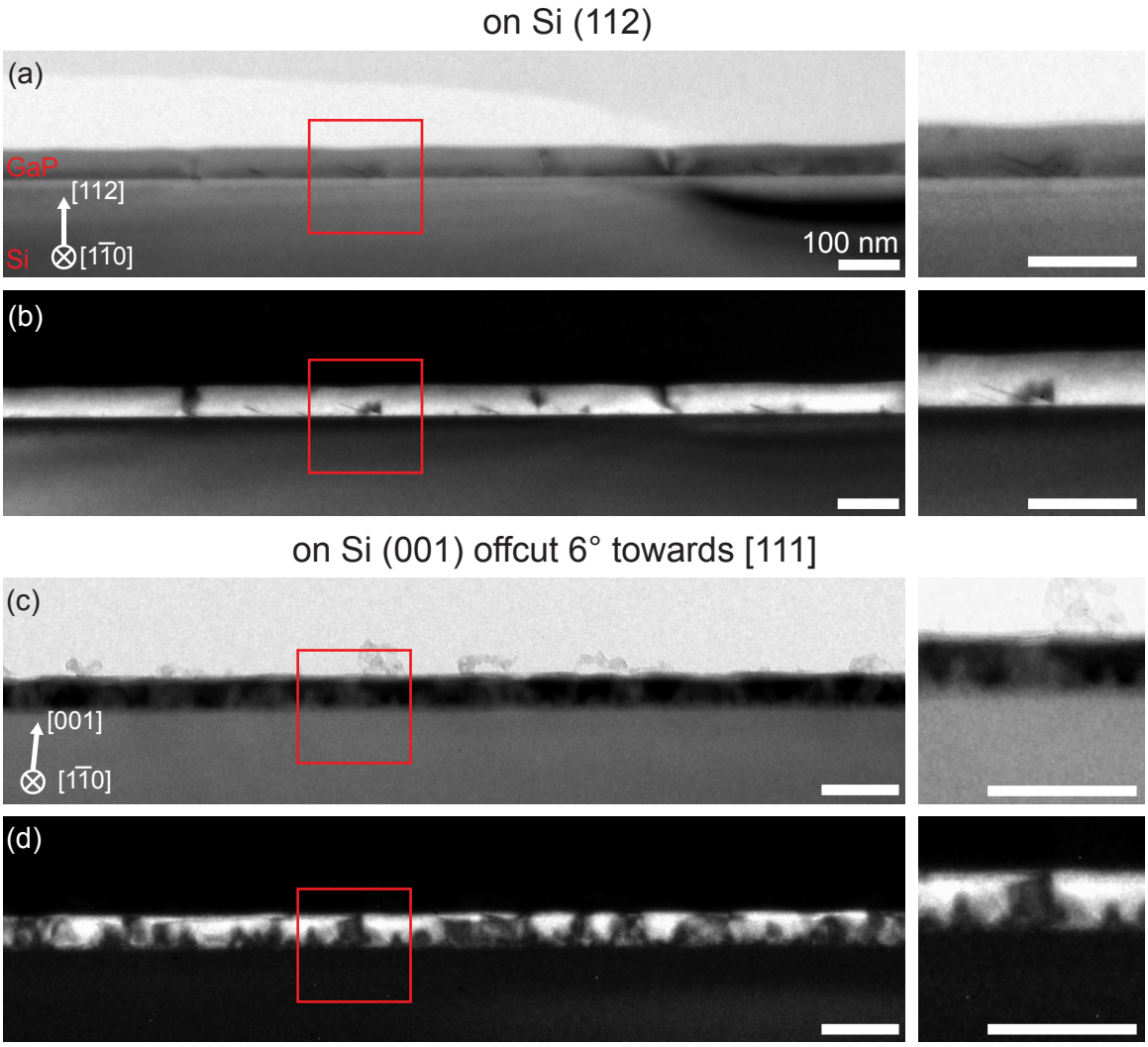


FIGURE 5.8: Cross sectional transmission electron microscopy of a $\sim$ 50 nm thick GaP thin film on Si (112) shows no evidence of antiphase domains in $\mathbf{g}_{200}$ two beam (a) bright field and (b) dark field imaging. In contrast, a thin film grown concurrently on Si (001) offcut 6° towards [111] reveals a high density of antiphase domains in $\mathbf{g}_{200}$ two beam (c) bright field and (d) dark field imaging. Contrast and brightness were adjusted in the inset bright field images to aid in identification of antiphase domains. Scale bars represent 100 nm.

were collected in the $\mathbf{g}_{200}$ two-beam condition. Films grown on Si (112) have limited defect density, and all of the defects in the bright field images (Figure 5.8a) have identical contrast in the dark field images (Figure 5.8b). In the case of films grown on Si (001) offcut 6° towards [111], the bright field images (Figure 3c) show a high density of defects originating from the GaP/Si interface, and the corresponding dark field image (Figure 5.8d) contains the same features with reversed contrast, confirming that these are antiphase domains. Plan view transmission electron microscopy (Figure 5.9) shows the same behavior, with no evidence of antiphase domain formation on Si (112). Antiphase domains are clearly seen in $\mathbf{g}_{200}$ imaging of the plan view sample grown on Si (001) offcut 6° towards [111].). However, twins and stacking faults are present in the films, as seen in the $\mathbf{g}_{111}$ dark field image for growth on (112). Reduced defect density should be achievable by optimization of the nucleation conditions for the (112) orientation.

In conclusion, we have demonstrated growth of high quality, antiphase domain-free GaP on Si (112) substrates using a two-step low temperature pulsed nucleation and high temperature continuous growth. Compared to films grown on Si (001) offcut 6° towards [111], epitaxial thin films are smoother below and above the critical thickness of GaP on Si as measured by atomic force microscopy, and thicker films reach full relaxation at 200 nm thickness. Transmission electron microscopy in cross section and plan view confirm a lack of antiphase domain defects in films grown on (112) versus definitive proof of those defects in films grown on (001) offcut 6° towards [111]. A small population of microtwin and stacking fault defects still exist, which could be removed by further optimization of the TEGa flow rates during nucleation.

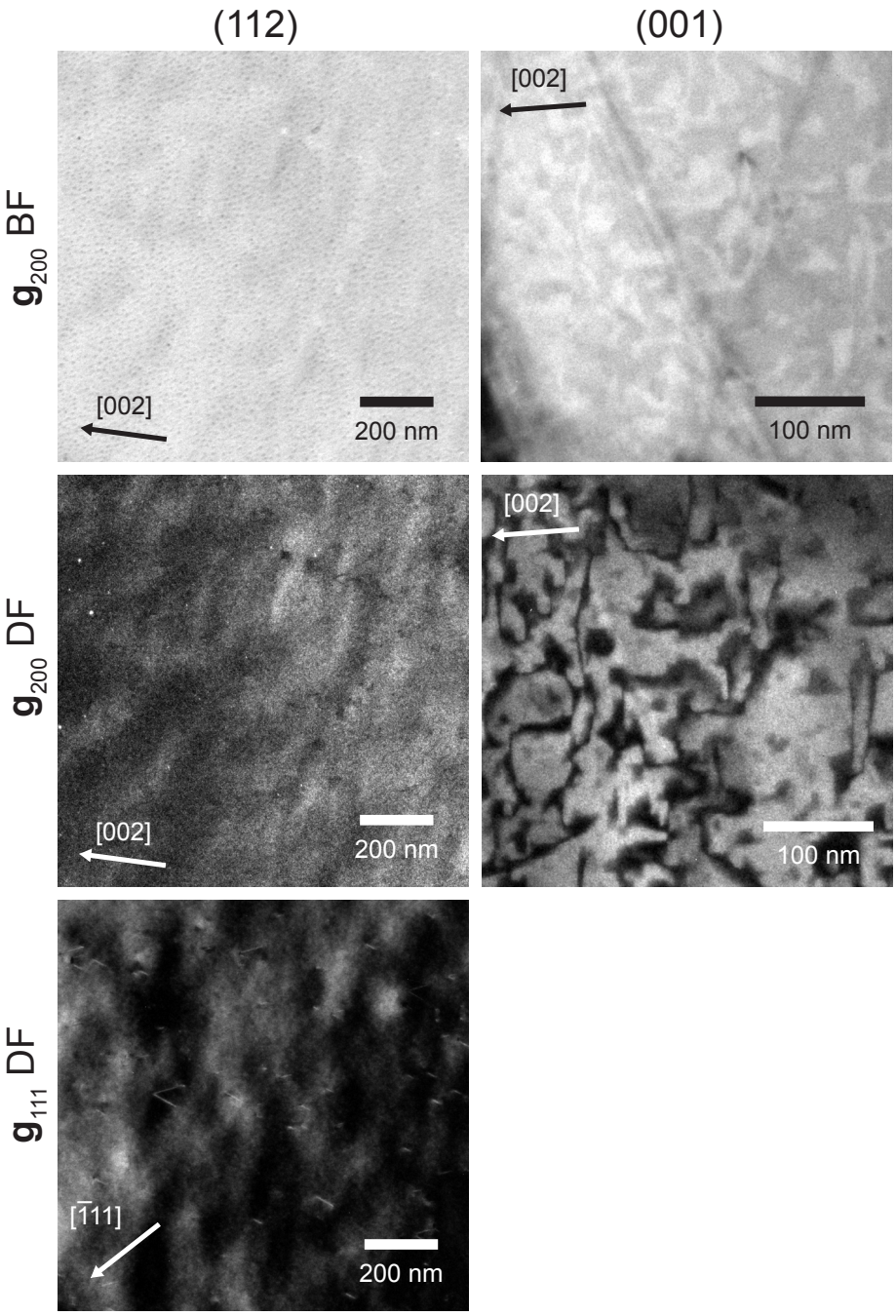


FIGURE 5.9: Plan view transmission electron microscopy of $\sim$ 50 nm thick GaP thin films on Si (112) (left) and Si (001) offcut 6° towards [111] (right).

Chapter 6

Conclusions and future directions

6.1 Microwire array photovoltaics

6.1.1 Group IV alloy microwire arrays

Single crystal, epitaxial SiGe alloy microwire arrays were grown with Ge content up to 12%. Wire arrays with high fidelity and large wire heights were grown, although the growth conditions appeared to be much more sensitive to reactor conditions. Further investigation of the wire with TEM and EDAX found Ge-rich layers at the tips of the wires, insinuating that the catalyst is Ge-rich relative to the growing wire material during the growth. The Ge content could be limited by the chemistry of the Cu-Ge-Si system or simply by strain.

While lattice matched top cell growth on these compositions will not result in a high efficiency device, they could serve as a lattice and coefficient of thermal expansion matched substrate for GaP growth. However, the advent of cheap, high quality Si supercedes the need for low lifetime VLS-grown wire arrays. Independent of photovoltaic applications, two possible routes to increasing the Ge content would be to explore the use of an alternative catalyst, such as Au, or to try patterning and growing wires with smaller radii. In the case of the former, Au has eutectic temperatures almost equal for mixtures with Si and

Ge, and in the case of the latter, strain relief should become more readily available through traction-free relaxation at the wire base as the radius of a wire is decreased. The availability of high lifetime Si motivates the use of top-down patterning techniques to achieve similar geometries. Efforts in the group have already yielded promising results towards this end.

Looking towards the future, the likely thermodynamically limited growth of the wires and the low price of high lifetime Si wafers precludes any further investigation of Cu-catalyzed growth. However, the geometries explored in these studies could serve as valuable prototypes for top-down etched structures using wet chemical techniques, such as metal-assisted chemical etching, or reactive ion etching. Realizing structures in etched LPCVD grown planar SiGe is not likely to be a fruitful endeavor, as the monetary costs of such an approach will likely present a major challenge to commercial application. If geometric control of wire diameter can be achieved, there could also be room for careful study of the optical properties of potential structures with FDTD.

6.1.2 Group III-V compound semiconductor/Si microwire array tandems

Overall, MOCVD growth of GaP and GaInP on Si microwire arrays proved to be an extremely challenging endeavor. High quality materials were not realized. Complications due to the complex, three-dimensional substrate are likely at the root of many of the defects seen in the layers grown on Si wire arrays. Initial attempts to compensate for the effects of the geometry on the growth rate are promising. Coupled optoelectronic simulations based on experimentally achieved geometries show potential for reaching > 20 % efficiencies.

Future efforts in realizing a tandem wire array device should focus on radically different designs. Top-down wire array fabrication on Si (001) substrates should yield wires with top facets more amenable to GaP growth. The growth rate should be optimized for the geometry given. Optoelectronic simulations will provide insights into interesting geometries. Nanowires, in particular, are quite promising from a optics and materials growth

point of view [90]. They could be coupled with planar or top-down etched wire array materials to yield high efficiency tandem devices with minimal use of expensive organometallic precursors.

6.2 MOCVD of GaP on Si for c-Si photovoltaics

High quality GaP thin films were grown on Si (112) substrates using the ALE nucleation approach published by others in the field [20, 21, 88]. Our results confirmed the earlier work done by Herbert Kroemer *et al.* [95], finding that this orientation completely inhibited the formation of antiphase domains. Films grown on Si (001) with the same growth conditions contained a significant fraction of antiphase domains. Surprisingly, thick films on (112) relaxed fully, making them tenable for integration of step-graded buffers for GaAsP or GaInP top cells.

Other groups are making great strides in the area of GaP on Si integration. The ALE nucleation and high temperature growth have been developed to the point of antiphase domain-free growth on Si (001) substrates [21]. Furthermore, recent developments out of the National Renewable Energy Laboratory suggest that similar results can be achieved with an As_2 pretreatment anneal rather than careful annealing and homoepitaxial Si growth [92], which could be an easier route to obtaining full surface coverage of double steps. Similar treatment of ultra-high vacuum CVD SiGe layers also allows for antiphase domain-free growth on these substrates [51]. However, the lifetime of Si wafers after heat treatment is an area that needs further investigation to isolate the source of effective lifetime degradation [14].

Another promising route for tandem integration is with epitaxial liftoff and wafer bonding. This eliminates the need for epitaxial growth on Si, removing the lengthy step-graded buffer growth. Many groups are investigating the development of the transparent bonding layer [83] and devices [7, 10, 91, 97]. Another possibility is to look into van der Waals epitaxy, utilizing graphene or another 2D material as a substrate for growth. This route could lead

to direct growth of highly mismatched materials, as perfect van der Waals epitaxy should not be influenced by the underlying crystalline substrate. However, obtaining good material quality remains a significant challenge despite some promising results with GaN.

Appendix A

Large area Si microwire array growth

A.1 Large area Si microwire growth

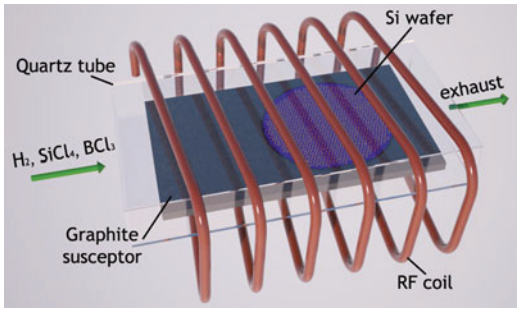


FIGURE A.1: Schematic of the large area wire CVD growth chamber. © 2012 IEEE

Wafer scale growth was achieved by purchasing a new CVD reactor capable of growing on 6" silicon wafers. The system is a FirstNano Easytube 3000[1] equipped with a rectangular quartz tube with RF heating of a SiC-coated graphite susceptor (Figure A.1). The "cold wall" process enabled by the RF heating was intended to reduce silicon deposition on

[1] Affectionately nicknamed the "Eviltube 3000"

the sidewalls of the tube during growth, thereby enabling higher precursor utilization and longer tube lifetimes. Temperature feedback control was regulated by using a thermocouple inserted into a quartz sheath fitted into the center of the susceptor. A single 6" wafer sits on top of the susceptor.

A.1.1 Preparation of growth substrates

6" wafer substrates were prepared using a standard photolithographic liftoff process.

1. Degenerately doped wafers with 300-500 nm of thermal oxide (Addison Engineering) were loaded onto a spinner and cleaned with acetone and isopropyl alcohol sequentially.
2. After being removed from the spinner chuck, the wafers were placed into an oven at 120 °C for at least 10 minutes to drive off any excess water on the surface.
3. The wafers were then loaded into an empty wafer carrier with a small open container of hexamethyldisilazane for 10 minutes to promote photoresist adhesion.
4. Shipley S1813 photoresist was then spun on at 4000 rotations per minute. Special care had to be taken to apply enough photoresist to cover the entire wafer. Care was taken in removing the edge bead with a swab and any excess photoresist on the backside of the wafer with wipes, both moistened in acetone, before placing the wafers onto hotplates heated to 115 °C for one minute each.
5. Exposure was conducted with a mask consisting of 3 μm dots on a 7 μm pitch on a hexagonal grid. The best results were achieved by using "vacuum contact."
6. Development consisted of a 90 second soak in MF319 with gentle agitation, followed by a thorough DI rinse.
7. Prior to removing the exposed oxide, a hard bake was done at 115 °C for ten minutes.
8. Oxide removal was done in Buffered HF Improved (Transene) to yield the exposed Si surface without overetching.

9. After drying the wafers thoroughly with a N_2 gun, 400 nm of high purity Cu (99.9999%, Alfa Aesar) was deposited using electron beam evaporation.

10. Liftoff proceeded in acetone, followed by rinses in isopropyl alcohol and water before drying.

A.1.2 Outlook

While we were successful in scaling growth of wire arrays up to 6" wafers, there were many challenges associated with this process [2].

First and foremost, the design of the rectangular reactor tube was such that achieving the positive or negative pressure necessary for even the most rudimentary leak testing was impossible. From our experience with the homebuilt wire growth CVD, run-to-run reproducibility was only achieved after careful He leak testing of all of the components during reactor assembly, leak rate testing between each run, and periodic He leak testing of all elastomeric seals. Without these diagnostic capabilities, there was no systematic method by which to test individual components of the large area wire growth CVD. Furthermore, there is no way to prove that there is a leak in the system. The manufacturer insisted that the vacuum pumped double o-ring seal was enough to prove no leaks were present, but widespread evidence of exposure to chlorine containing gases was present in the form of corrosion on stainless steel parts in the reactor cabinet and in the lab in general. A deep dive of the literature revealed that one group has had success in purging the double o-ring seal with N_2 instead of pulling vacuum [9].

Second, without the loading area encased in a nitrogen purged glovebox, the reactor sidewalls were exposed to ambient air every single time the system was opened. The interior surfaces of the reactor were at the mercy of the ambient humidity, and short of purging

[2] As the point of this document is to archive the experimental details, I think it's important to address some of the issues associated with production on this scale for future generations of graduate students.

samples in the reactor for inordinate amounts of time, residual moisture and oxygen levels could not be controlled.

Third, while photolithography on 6" wafers is possible to do in the Kavli Nanoscience Institute, it is by no means easy to apply photoresist, develop, deposit, and liftoff multiple wafers. The uniformity of the patterns after exposure and liftoff also had plenty of room for improvement.

All of these issues made developing a 6" wire array growth process quite challenging. The first two issues could be resolved by moving to a reactor geometries that enable low or high vacuum leak testing techniques which can be housed inside of a nitrogen purged glovebox assembly to eliminate the effects of ambient humidity. Other issues, such as undesirable deposition on the reactor parts and throughput, could be tackled by thinking carefully about the reactor design. The epitaxial Si CVD reactors being developed by Applied Materials, Solexel, and Crystal Solar could provide valuable ideas and inspiration for a future Si wire growth CVD prototype.

Appendix B

Calculation of lattice relaxation from HRXRD RSM's on non-standard orientations

Unfortunately, Panalytical X'Pert Epitaxy does not generate suitable results for non-standard orientations. To work around this limitation, a simple Excel spreadsheet was constructed. This section is a brief walkthrough of the calculations performed in this spreadsheet.

First, the expected d-spacings were calculated for the provided asymmetric and symmetric peak for both the substrate and the film material.

$$d = \frac{a}{\sqrt{h^2 + k^2 + l^2}} \tag{B.1}$$

The tilt, α, between the asymmetric and symmetric peaks was calculated. Let $[hkl]$ represent the symmetric peak and $[h'k'l']$ represent the asymmetric peak.

$$\alpha = cos^{-1} \frac{[h\vec{k}l] \cdot [h'\vec{k}'l']}{|[h\vec{k}l]||[h'\vec{k}'l']|} \tag{B.2}$$

Then, the expected peak locations for the substrate were calculated.

$$\omega = sin^{-1} \frac{\lambda}{2d} \tag{B.3}$$

$$2\theta = 2\omega \tag{B.4}$$

$$\omega' = sin^{-1} \frac{\lambda}{2d'} \pm \alpha \tag{B.5}$$

$$2\theta' = 2\, sin^{-1} \frac{\lambda}{2d'} \tag{B.6}$$

The difference between measured peak locations for the substrate and film were calculated.

$$\Delta\omega = {\omega_{film}}^m - {\omega_{substrate}}^m \tag{B.7}$$

$$\Delta 2\theta = {2\theta_{film}}^m - {2\theta_{substrate}}^m \tag{B.8}$$

And likewise for $\Delta\omega'^m$ and $\Delta 2\theta'^m$.

With these values, we arrive at corrected measured peak locations assuming the measured peak locations are simply a reference.

$$\omega_{film}^{corr} = \omega + \Delta\omega \tag{B.9}$$

$$2\theta_{film}^{corr} = 2\theta + \Delta 2\theta \tag{B.10}$$

Then, the d-spacings in the x-direction (surface parallel) are calculated for the substrate, film, and measured films.

$$d_x = \frac{\lambda}{cos\,\omega - cos\,(2\theta - \omega)} \tag{B.11}$$

Finally, the relaxation is calculated as

$$R_x = \frac{{d_x}^{film,corr} - {d_x}^{substrate}}{{d_x}^{film} - {d_x}^{substrate}} \tag{B.12}$$

Appendix C

Preparation of TEM samples using SEM/FIB

All of the specific steps are denoted with bullet points.

First, a protective capping layer is deposited on the area of interest. This cap is necessary to prevent damage to the area of interest. Use a two-step process with electron beam initiation followed by fast ion beam deposition to avoid damaging the surface.

- Pt electron beam induced deposition (EBID) – 5 kV, high current
  Need a continuous conformal coating in the area to assist in promoting deposition versus milling.
- Pt ion beam induced deposition (IBID) – 30 kV
  General rule of thumb - 3 pA μm^{-2} and at least 2 μm of material.

Next, cuts are made into the surface to define the TEM membrane.

- FIB "Regular Cross Section" – 30 kV, 3 nA
  One cross section for each side, 180°rotation. Typically needs to be at least two or

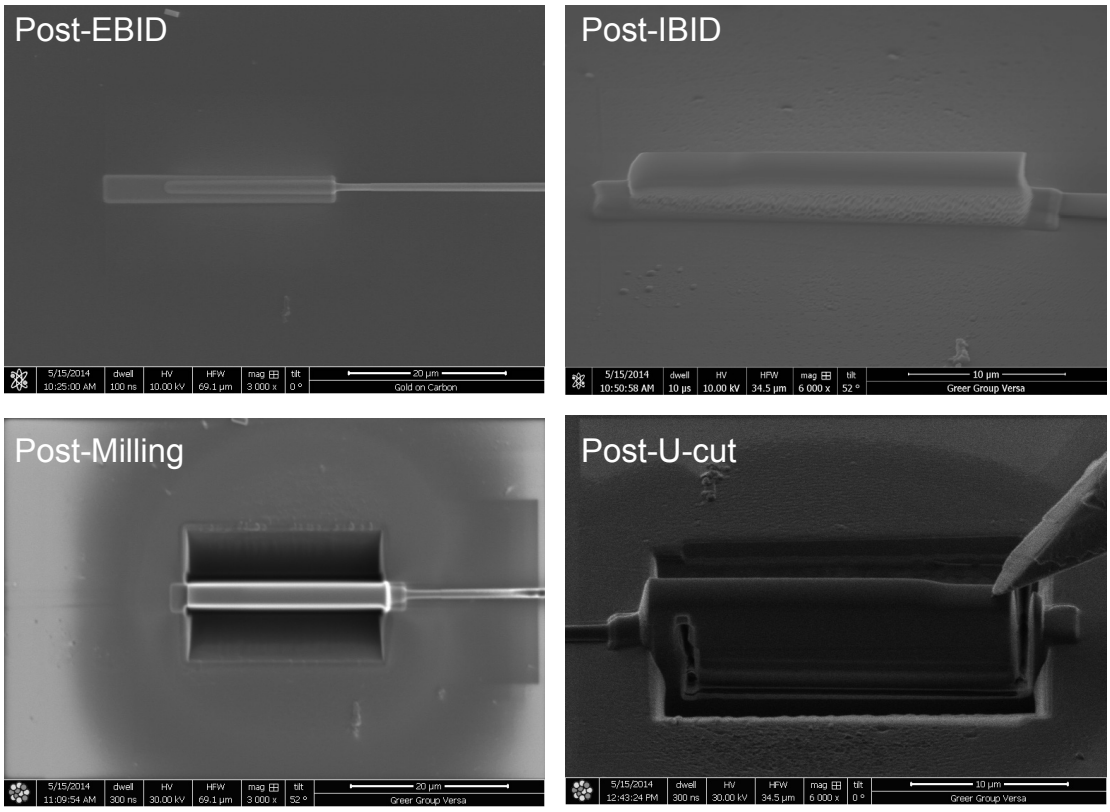


FIGURE C.1: SEM and FIB images of procedures done on the host or sacrificial substrate.

three times as deep as the area of interest and 5-10 μm long to allow for enough clearance of the FIB to allow cut-out of the membrane.

- FIB "Cleaning Cross Section" – 30 kV, 3 nA
  A smaller cut on each side of the membrane to remove any redeposited material.

Then, a U-cut is made in the membrane to prepare it for removal.

- FIB "Rectangle" – 30 kV, 3 nA
  Rectangular cuts are made to liberate one side of the of the membrane while leaving the other side mostly intact. An example of this can be seen in Figure C.1. The

cut should be ceased immediately after breaking through to the other side to avoid redeposition effects.

- FIB "Cleaning Cross Section – 30 kV, 3 nA
  Used to clean up the other side of the membrane after cutting through.

Finally, a micromanipulator is inserted and maneuvered such that the tip contacts the free side of the membrane (Figure C.1). A small Pt weld is made to attach the manipulator tip, and then the U-cut is finished to liberate the membrane.

- FIB "Pt dep" – 30 kV
  Again, staying under 3 pA μm^{-2} is recommended to avoid milling. A small weld is made. Overkill is layers on the order of μms, but it is sometimes useful...

- FIB "Rectangle" – 30 kV, 3 nA
  Punching through the rest of the U-cut. Again, optimizing for material removal vs. redeposition is key to finishing the cut. Higher currents can help.

Next, the liberated membrane is moved to a Cu half-grid and placed into contact with one of the pillars on the grid and welded on before blowing away the manipulator weld. The welding is done with the same considerations for material deposition versus etching discussed beforehand.

After removing the manipulator weld, the thinning process begins. Three critical goals must be balanced during the thinning.

1. Milling rate vs. damage
   The energy of the ions is the dominant input into the amount of implantation and damage. As the sample is thinned, the accelerating voltage should be lowered to limit the amount of damaged versus pristine material.

2. Thickness vs. remaining Pt cap

   The Pt cap serves as a sacrificial layer to prevent direct milling of the surface by the ion beam. As the sample is thinned, the amount of Pt remaining will be reduced. Extra Pt at the start of the process is important.

3. Size of thin region vs. mechanical stability

   Mechanical buckling will occur if the span of the thin region is too large. Several approaches can be taken to mitigate this issue. The typical approach is to thin in a "staircase" fashion, moving to a smaller thinning window sequentially.

This portion of the thinning will require optimization for sample materials and geometries. As a rule of thumb, the final thinning step will be essential to determining the fraction of damaged material. 5 kV final milling/cleaning step will leave 80% of the membrane undamaged, while 500 V will lead to almost no damage whatsoever (96%). 2 kV is suitable for Si, while most compound semiconductors will do worse.

Appendix D

Using the Agilent D-Star MOCVD at the Molecular Foundry

D.1 Metalorganic chemical vapor deposition

Along with molecular beam epitaxy, metalorganic chemical vapor deposition (MOCVD) is one of the premiere methods of growing high quality compound semiconductor layers with precise control of layer composition and thickness, enabling the growth of highly complex electronic devices, including high mobility transistors, high sensitivity photodetectors, light emitting diodes, solid state lasers, and photovoltaic devices. MOCVD is also known as metalorganic chemical vapor phase epitaxy (MOVPE) and organometallic chemical vapor phase epitaxy (OMVPE). As the name implies, MOCVD is a subset of CVD which uses organometallic precursors. These materials typically come in the solid or liquid phase, and they are introduced to the reactor by flowing H_2 or N_2 carrier gas and collecting the partial pressure after flowing past or bubbling through the material.

For the Group III-V compound semiconductors of interest in this thesis, typical precursors include trimethylgallium, trimethylindium, and trimethylaluminum. Arsine and phosphine

are the most commonly used Group V precursor, but due to the safety issues associated with their toxicity and pyrophoric nature, the work in this thesis has used tertiarybutylphosphine (TBP). TBP posesses additional benefits due to its lower decomposition temperature, which allows growth with lower thermal budgets. Table D.1 contains a list of all of the precursors used in this work and some of their physical properties. Also included are fitted coefficients for the partial pressure of each material at a given temperature T. The partial pressure can be calculated as:

$$log_{10} P\,[torr] = A - \frac{B}{T\,[K]} \tag{D.1}$$

Precursor	Abbrev.	MP (°C)	BP (°C)	A	B (K)	P (torr) @ T (°C)
Trimethylaluminum	TMAl	15	126	8.224	2134.83	7.8 @ 18
Trimethylgallium	TMGa	-15.8	55.8	8.501	1824	114.6 @ 10
Triethylgallium	TEGa	-82.5	143	8.083	2162	2.8 @ 10
Trimethylindium	TMIn	88	135.8	10.520	3014	1.5 @ 18
Tertiarybutylphosphine	TBP	4	54	7.586	1539	141.5 @ 10

TABLE D.1: List of MOCVD precursors and their properties. A and B refer to the coeffecients of Equation D.1, which can be used to calculate the partial pressure of each species.

With the partial pressure, the temperature of the bubbler and the flow rate, the molar flow rate f can be calculated assuming the concentration of precursor is in the dilute regime, such that the behavior of the gas overall is closer to ideal.

$$f\,[mol\,min^{-1}] = \frac{P_{precursor}}{P_{bubbler}} \frac{V\,[L\,min^{-1}]}{V_{H_2}\,[L\,mol^{-1}]} \tag{D.2}$$

where V_{H_2} is simply the molar volume of an ideal gas at temperature T given by:

$$V_{H_2}[L\,mol^{-1}] = \frac{62.3637 \times T\,[K]}{P_{bubbler}\,[torr]} \tag{D.3}$$

Key parameters for MOCVD growth include the reactor pressure, substrate surface temperature, and V/III ratio, the ratio between the total molar flow of Group V and Group III precursors.

D.2 System Overview

The Agilent D-Star phosphide MOCVD at the Foundry is based on a Thomas Swan Epitor II close coupled showerhead reactor heavily modified for computer control. Susceptors for the system made of tungsten or glassy carbon can hold a single 2" or 3" wafer, and 1×1 cm chips can be loaded by using a custom laser-cut 3" quartz wafer. A resistive heater below the susceptor allows for sample heating. Temperature feedback is provided by a thermocouple in close proximity to the back surface of the susceptor, and a vertically mounted pyrometer allows for measurement of the sample temperature.

D.2.1 Control

The reactor components are depicted in Figure D.1. The inputs into the reactor are split into two sides. The "A" side is populated with Group III precursors and liquid/solid phase dopant precursors, and the "B" side is populated with Group V precursors and gas phase sources. Both sides have a "run" line flowing to the chamber and a "vent" line flowing to the exhaust to allow for equilibration of precursor flow before introduction to the reactor chamber.

The control racks for the system are depicted in Figure D.2. The leftmost rack houses a vacuum setpoint butterfly valve controller, a few vacuum gauge controllers and a temperature readout (not pictured) for thermocouples monitoring bubbler bath temepratures. The center rack houses the reactor temperature controller, substrate rotation controller, and a large panel of MFC and BPC controllers. The rightmost rack houses the opto-isolator boards for the system, which can be used to manually actuate valves and with the automated control

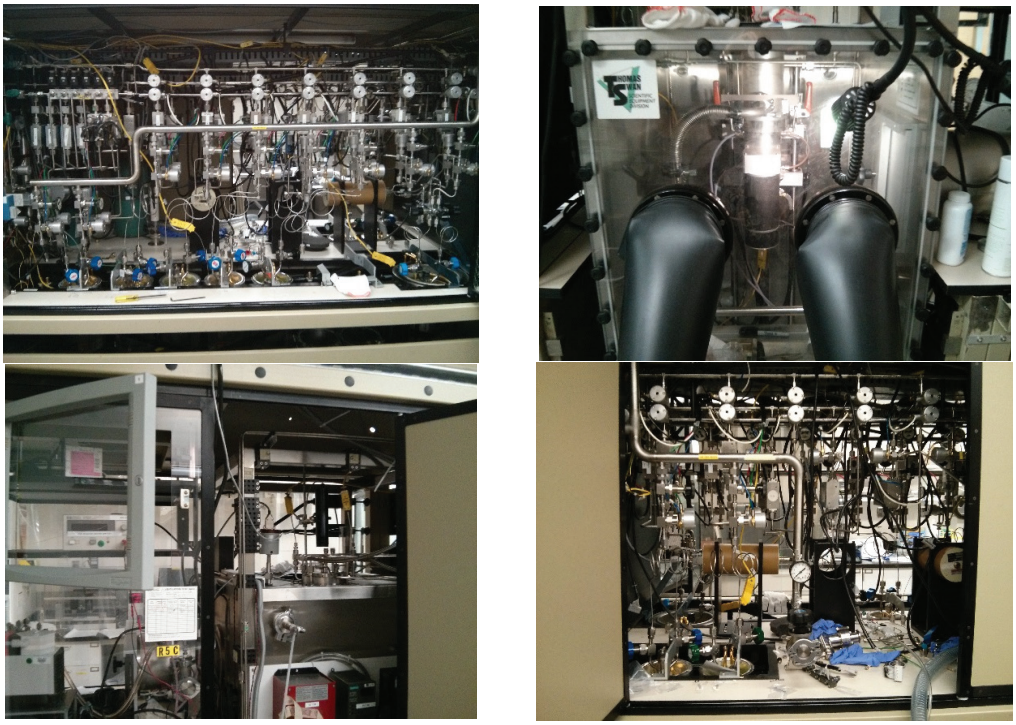


FIGURE D.1: Overview of reactor components. "A" side bubblers and flow control (top left) and the reactor chamber glovebox (top right) are located on the right side of the room facing the hallways. The rear of the reactor glovebox (bottom left) and the "B" side bubblers and flow control (bottom right) are located on the right side.

software. During normal operation, the run line MFC's are set to 4 slm of carrier gas flow each, and the vent line MFC's are set to 5 slm of carrier gas flow each for a total of 18 slm. Refer to Figure D.3 for the location of flow/pressure controls and typical setpoints for the reactor flow and purges.

D.2.2 Precursor flow control

To enable precise bubbled precursor flow, each bubbler is equipped with a separate flow and pressure control loop (Figure D.4). An MFC is used to control flow into the loop from the carrier gas manifold, and a hand valve mounted between the MFC and the manifold can be used to isolate the control loop. Pneumatically controlled inlet and outlet valves regulate



FIGURE D.2: Control racks for the Agilent MOCVD.

the flow into and out of the bubbler, and a bypass valve bridges two together for use when precursor flow is not necessary. A pressure controller is mounted between the control loop and valves, allowing flow into the "run" or "vent" lines. In addition, a hand valve allows for access to the control loop through a leak check manifold. This valve should be left closed during normal use.

D.2.3 Software, flow control and hardware labeling

Unfortunately, there are several levels of labeling of each precursor. Each MFC/BPC combination is labeled, but the label does not correspond to the material loaded in the bubbler. This label can also be different in the control software. To add yet more confusion, the full scale values on the flow control board and in the control software can be different than

Run A 4 slm	**Vent A** 5 slm	**Run B** 4 slm	**Vent B** 5 slm	**Reactor purge** 1 slm
TMIn 0-500 sccm	**TMAl1** 0-2 slm	**TMAl2** 0-1000 sccm	**TMGa** 0-500 sccm	**TEGa2** 0-10 sccm
As1 0-200 sccm	**As2** X	***P 1*** *X*	***P2*** *X*	***DTBSi*** *X*
TMAA ?	**TMSb** 0-100	***CBr4*** *X*	***Disilane*** *X*	**Alt 1** 0-500 sccm
AMU 1 *X*	***AMU 2*** *X*	***AMU 3*** *X*	***AMU 4*** *X*	***Alt 2*** *X*
BMU 1 *X*	***BMU 2*** *X*	**Top Port purge** 50 sccm	**Pyrometer purge** 100 sccm	**Annular purge** 4 slm
DTBSi BPC *X*	***Exhaust N2*** *X*	***Exhaust Air*** *X*	***H2 manifold P*** *X*	*X*
TMIn BPC 400 torr	**Cp2Mg BPC** 400 torr	**TMAl2 BPC** 1500 torr	**TEGa1 BPC** 1200 torr	**TEGa2 BPC** 1450 torr
TMAA BPC 100 torr	**TMSb BPC** 1500 torr	***CBr4 BPC*** *X*	**Alt 1 BPC** 400 torr	***Alt 2 BPC*** *X*

FIGURE D.3: Typical reactor setpoints on board arranged in order of their rack position. Values typically set during growth are highlighted in green. Grey backgrounds indicate items not used during growth. White backgrounds are used for flow control, and unless units are noted, these values are the zero to full scale value from the controller.

the MFC full scale flow value. To de-obfuscate this mess, the labeling, material, flow, and pressure control breakdown is presented for the system in Tables D.2, D.3, and D.4.

Label	**Mat.**	**T (° C)**	**F (sccm)**	**C.F.**	**PC label**	**PC Ctrl**	**PC C.F.**	**P (torr)**
TMIn	TMIn	18	500	5	TMIn	Y	1	400
Empty	Empty							
Empty	Empty							
TEGa1	TEGa	10	500	5	TEGa1	Y	1	1500
TEGa2	TMGa	10	10	0.1	TEB	Y	0.02	1500
TMAl1	Cp_2Mg	18	2000	2	DEZn	Y	10	400
TMAl2	CBr_4	18	100	0.1	–	Y	1	1500
Alt1	TMAl	18	500	1	Alt1	N	–	400
Alt2	Empty							

TABLE D.2: Group III precursor labels in order from right to left in cabinet.

Correction factors for the flow control board and software are calculated as follows:

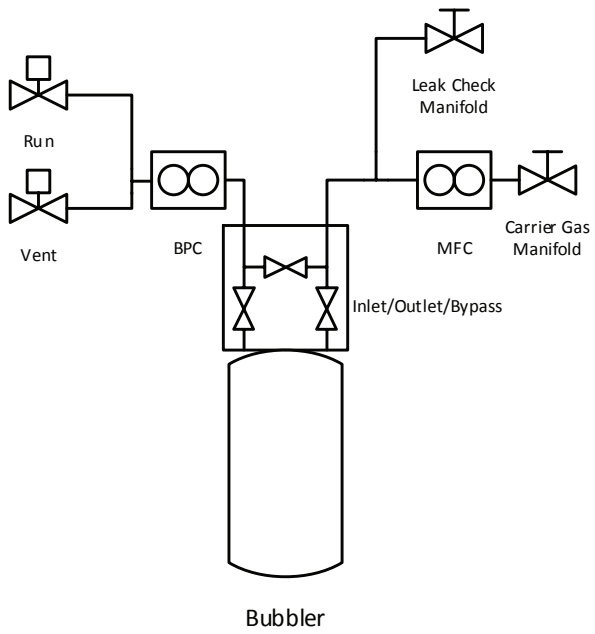


FIGURE D.4: Schematic of bubbler flow and pressure control loop.

Label	**Mat.**	**T (° C)**	**F (sccm)**	**C.F.**	**PC Ctrl**	**PC C.F.**	**P (torr)**
TMSb	TBP	10	500	5	N	–	1500
TMAA	DMHz						

TABLE D.3: Group V precursor labels in order from left to right in cabinet.

Label	**Gas**	**F (sccm)**	**C.F.**	**PC Ctrl**	**PC C.F.**	**Dilution (ppm)**
As1	Empty		Used for P1	Used for P1	Used for P1	
As2	Empty					
P1	SiH_4 in H_2	4.46	40	Y	40	215
P2	Empty					

TABLE D.4: Gas source precursor labels in order from left to right in cabinet.

$$[Actual flow] = [Correction factor] \times [Input flow] \tag{D.4}$$

D.3 Instructions

D.3.1 Unloading manually

1. Turn off the heater power supply.
2. Close hand valves on all bubblers.
3. Switch pressure controller to "local" and push "open".
4. Ramp run A and run B flows to zero. Switch top port, pyrometer and annular purge from "manual" to "off". Ramp annular purge flow to zero.
5. Close "H2 to Manf" (auto to off) and open "N2 to Manf" (off to on).
6. Close run and vent ins (Mistic 0:6-9, auto to off).
7. Wait for run and vent flows to zero.
8. Close run outs (Mistic 0:10 and 13 auto to off).
9. Close purge valve (Mistic 0:15). Allow reactor purge flow to go to zero.
10. Close "Vent to Exh" (Mistic 5:8, auto to off). Watch chamber exhaust pump vacuum drop to 200 mTorr.
11. Push "closed" on the pressure controller. Close "Main Exhaust Valve" (Mistic 5:10, auto to off). Open "Vent to Exh" (Mistic 5:8, off to auto).
12. Open "Purge H2" (Mistic 0:15, off to auto). Let chamber come up to 700 torr (about 3 minutes).
13. Ramp reactor purge flow to zero. Close purge valve (Mistic 0:15, auto to off).

D.3.2 Pumping down manually

1. Open main exhaust valve (Mistic 5:10, off to auto).
2. Switch pressure controller to "local". Press "A" and wait for the pressure to drop. Ramp down pressure from setpoint A to E to keep the valve open below 10%. Once it reaches the 300 torr range, push "open", and wait for 5 minutes.
3. Close "Vent to Exh" (Mistic 5:8, auto to off). Watch chamber exhaust pump vacuum drop to 200 mTorr.
4. Push "closed" on the pressure controller. Close "Main Exhaust Valve" (Mistic 5:10, auto to off). Open "Vent to Exh" (Mistic 5:8, off to auto).
5. Watch the pressure increase over 2 minutes. If the total increase is greater than 2 Torr, then bring the reactor back up to pressure and check for a leak. Otherwise, continue onwards.
6. Open the main exhaust valve (Mistic 5:10, off to auto). Push "open" and then "E" on the pressure controller.
7. Close "N2 to Manf" (Mistic 0:5, on to off) and open "H2 to Manf" (Mistic 0:4, off to auto).
8. Check to make sure the run A, run B, reactor purge, and annular purge flows are ramped down to zero. Then open "Purge H2" (Mistic 0:15, off to auto).
9. Set reactor purge to 0.5 slm and allow it to stabilize. Ramp up to 1 slm.
10. Open vent ins (Mistic 0:7-8, off to auto). Allow vent A and vent B to stabilize at 5 slm.
11. Check that run A and run B are set to zero. Open run outs and then ins (Mistic 0:6,9,10,13). Set run A and run B to 0.5 slm and allow it to stabilize. Ramp run A and run B up to 4 slm.

12. Make sure top port and pyrometer purge flows are set to 50 and 100 sccm. Switch them from off to on.

13. Check that annular purge flow is set to zero. Set annular purge flow to 0.3 slm, turn on the controller, and allow it to stabilize. Ramp up the flow to 4 slm.

D.3.3 Running your recipe

1. Turn substrate rotation on (center cabinet, green button).

2. Start OMSW main control panel.

3. Ramp substrate rotation up to 25 rpm in 5 rpm increments. You have to press the button in order to set the rotation rate.

4. Press "Clear Errors". Wait for message.

5. Press "Clear Tables". Wait for message.

6. Press "Download a Recipe". Select your recipe file. Proceed onwards without waiting for download complete message.

7. Turn on the heater power supply.

8. Open hand valves for all bubblers used in growth.

9. Wait for "File download complete" message. Then press "Start run".

Appendix E

Synopsys Sentaurus TCAD for Tandem Wire Array Simulations

E.1 Introduction

`swb`	Workbench	Wrapper to enable passing parameters and data between tools and scripting. Also contains tools for design of experiments (not used here).
`epi`	Epi	Easy generation of layered structures. Enables passing information about these structures to sde.
`mpr`	MatPar	Automated management of materials parameter files.
`sde`	Structure Editor	Structure generation and position dependent materials property definition on grid.
`snmesh`	Meshing	Generation of an equivalent tensor mesh for FDTD simulation.
`emw`	EMW	FDTD simulation using tensor meshes defined in snmesh.
`sdevice`	Device	Drift-diffusion device physics simulation. Interpolation and integration of optical generation profiles onto the device mesh.
`inspect`	Inspect	Post-processing of results from sdevice for display.

Table E.1: List of Sentaurus tools used during simulation

Basic familiarity with the Sentaurus software package is assumed here. Please refer to the manual or an appropriate tutorial before referring to these notes. A summary of the tools used here is in Table E.1.

The workflow summarized here is somewhat different than those utilized by other members of the group. Since the FDTD optical simulations are the rate limiting step, the optical and device simulations are decoupled, and the results of the optical simulations can be fed into the device simulations as they become available.

E.2 Optical simulation

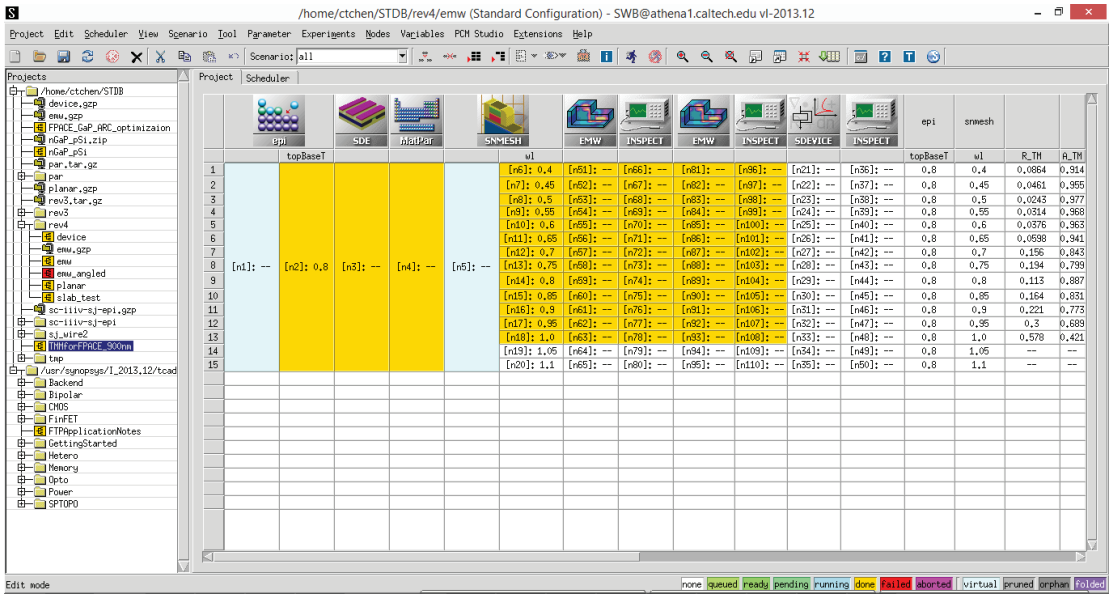


FIGURE E.1: Basic workflow in `swb` for the optical simulations of a wire tandem device.

E.2.1 Setting up the device geometry

With the sheer number of device layers in a tandem type structure, defining each of the layers and their parameters can be quite lengthy. Synopsys recently integrated two helpful

tools: one to assist in creating layers, Epi, and another to assist in generating materials parameters files, Matpar. While Epi is set up to generate a planar structure, the information from Epi can be used to generate arbitrary geometric structures as well.

LISTING E.1: `Epi` source code for generating GaInP tandem with step-graded buffer on Si

```
1  #-------------------------,,,,,,,
2  # Chris Chen - Epi command file for generating parameter files for GaInP, AlGaInP
       cells,,,,,,
3  # Based on code provided by Synopsys,,,,,,,
4  #-------------------------,,,,,,,
5  # Global section,,,,,,,
6  # Total width of device given in um,,,,,,,
7  $global Xmin=0, Xmax=2,,,,,,
8  $global topContact=cathode, bottomContact=anode,,,,,,
9  $global append columnNames lifetime,,,,,,,
10 $global diameter=2,,,,,,,
11 #$global dXmin=0.25, dXmax=0.25,,,,,,
12 #$global dYmin=0.05, dYmax=0.25,,,,,,
13 #$global generate=tdr,,,,,,,
14 ,,,,,,,
15 #-------------------------,,,,,,,
16 # Layers section (ENABLED),,,,,,,
17 # Region, Material, SourceParFile, Thickness, Doping, MoleFrac, Refinement, Lifetime
18 ,,,,,,,
19 ar2,MgF,,0.095,,,,-1
20 ar1,TiOx,,0.055,,,,-1
21 topfsf,AlInP,,0.029,4.00E+18,0.5,(mbox 0.001 1.5 ud)(yref 0.005),1.00E-12
22 topem  ,GaInP,,0.05,1.80E+18,0.51,(yref 0.005)(mbox 0.001 1.5 ud),1.00E-09
23 topbase,GaInP,,0.77,-1.20E+17,0.51,(yref 0.1)(mbox 0.001 1.5 ud),1.00E-09
24 topbsf,GaInP,,0.03,-2.00E+18,0.51,(mbox 0.001 1.5 ud)(yref 0.005),1.00E-12
25 tdp,GaInP,,0.015,-4.00E+19,0.51,(yref 0.0005),1.00E-12
26 # introduce a thin metal layer as series connector instead of using non local
       tunneling model ,,,,,,,
27 "# #if [string match ""*tdmetal*"" ""@stack@""]",,,,,,,
28 # tdmetal,Gold,tdmetal.par,0.001,,,,
29 # #endif,,,,,,,
30 tdn,GaInP,,0.015,1.00E+19,0.51,(yref 0.0005),1.00E-12
31 buf9,GaInP_45,,0.25,4.00E+18,0.45,(yref 0.1)(mbox 0.01 1.5 ud),1.00E-12
32 buf8,GaInP_40,,0.25,4.00E+18,0.4,(yref 0.05)(mbox 0.005 1.5 ud),1.00E-12
33 buf7,GaInP_35,,0.25,4.00E+18,0.35,(yref 0.05)(mbox 0.005 1.5 ud),1.00E-12
```

```
34 buf6,GaInP_30,,0.25,4.00E+18,0.3,(yref 0.05)(mbox 0.005 1.5 ud),1.00E-12
35 buf5,GaInP_25,,0.25,4.00E+18,0.25,(yref 0.05)(mbox 0.005 1.5 ud),1.00E-12
36 buf4,GaInP_20,,0.25,4.00E+18,0.2,(yref 0.05)(mbox 0.005 1.5 ud),1.00E-12
37 buf3,GaInP_15,,0.25,4.00E+18,0.15,(yref 0.05)(mbox 0.005 1.5 ud),1.00E-12
38 buf2,GaInP_10,,0.25,4.00E+18,0.1,(yref 0.05)(mbox 0.005 1.5 ud),1.00E-12
39 buf1,GaInP_5,,0.25,4.00E+18,0.5,(yref 0.05)(mbox 0.005 1.5 ud),1.00E-12
40 GaP,GaP,,0.25,4.00E+18,,(yref 0.05)(mbox 0.005 1.5 ud),1.00E-12
41 wire,Silicon,,40,(-2.0E16)(erf 1.0E+19  0 0.05 u),,(yref 0.05)(mbox 0.001 1.05 u)(
       mbox 0.001 1.5 d),1.00E-03
42 # botfsf,GaInP,,0.03,7.00E+18,0.51,(mbox 0.0001 15 ud)(yref 0.005),
43 # botem  ,GaAs,,0.1,2.00E+18,,(yref 0.005)(mbox 0.001 15 ud),
44 # botbase,GaAs,,2.539,-1.00E+17,,(yref 0.1)(mbox 0.001 1.5 ud),
45 # botbsf,GaInP,,0.05,-2.00E+18,0.51,(mbox 0.001 1.5 ud)(yref 0.005),
46 # # Generate the distributed Bragg reflector,,,,,,,
47 # $repeat 10,,,,,,,
48 # dbrhigh$i,AlGaAs,,0.058,-1.00E+18,0.1,(mbox 0.001 1.2 both),
49 # dbrlow$i,AlGaAs,,0.069,-1.00E+18,0.8,(mbox 0.001 1.2 both),
50 # $end,,,,,,,
51 # substrate,GaAs,,1,-1.00E+18,,(mbox 0.01 1.2 up),
52 ,,,,,,,
53 #-------------------------,,,,,,,
54 # Parameter file section,,,,,,,
55 #---------,,,,,,,
56 # Material,,,,,,,
57 ,MgF,MgF.par,,,,,
58 ,TiOx,TiOx.par,,,,,
59 ,AlInP,AlInP.par,,,0.5,,
60 ,GaInP,GaInP.par,,,0.51,,
61 ,GaInP_45,GaInP_45.par,,,0.45,,
62 ,GaInP_40,GaInP_40.par,,,0.4,,
63 ,GaInP_35,GaInP_35.par,,,0.35,,
64 ,GaInP_30,GaInP_30.par,,,0.3,,
65 ,GaInP_25,GaInP_25.par,,,0.25,,
66 ,GaInP_20,GaInP_20.par,,,0.2,,
67 ,GaInP_15,GaInP_15.par,,,0.15,,
68 ,GaInP_10,GaInP_10.par,,,0.1,,
69 ,GaInP_5,GaInP_5.par,,,0.05,,
70 ,GaP,GaP.par,,,,,
71 ,Silicon,Si.par,,,,,
72 ,Oxide,Oxide.par,,,,,
73 ,Silver,Ag.par,,,,,
```

```
,Gas,air-nk.par,,,,,
,AlOx,Al2O3.par,,,,,
,,,,,,,
#---------,,,,,,,
# Interface,,,,,,,
#,AlInP/GaInP,semiconductor-interface.par,,,,,
#,GaInP/GaInP,semiconductor-interface.par,,,,,
```

Using the scripting language built into all of the Sentaurus, the data from Epi can be read into Sentaurus Structure Editor. The structure information defined in Epi is then used to generate a structure file algorithmically using the tcl scripting capabilities built into the Sentaurus Workbench preprocessor.

LISTING E.2: `sde` source code for generating GaInP tandem with step-graded buffer on Si

```
;;;
```

```
26
27 (define SiLT    1E-3  ) ;; [s]
28 (define GaInPLT   1E-9  ) ;; [s]
29 (define windowLT  1E-9  ) ;; [s]
30 (define defectLT  1E-12 ) ;; [s]
31
32 (define diameter 2)
33 (define SiOx_th 0.11)
34 (define height !(
35   source n@node|epi@_epi.tcl
36   puts $epi(region,wire,thickness)
37 )! )
38 (define mask 2)
39
40 ;; ARC parameters, optimized for a planar AlInP slab
41 (define MgFT      0.095 ) ;; [um]
42 (define TiOxT     0.055 ) ;; [um]
43
44 ;; Output file parameters
45 (define fname   "n@node@_bnd"   )   ;;
46 (define elname  "n@node@_el_msh"  )   ;;
47
48 ;; REFINEMENT CONSTANTS
49 (define tiny 0.025)
50 (define lo_dx 0.025)
51 (define hi_dx  0.25)
52
53 ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
54 ; Structure Creation
55 ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
56 (display "Create ALL THE THINGS \n")
57
58 (sdegeo:set-default-boolean "BAB")
59
60 (sdegeo:create-rectangle
61   (position (* diameter -0.5) 0 0)
62   (position (* diameter 0.5) (* -1 height) 0 )
63   "Silicon" "wire")
64
65 (sdegeo:create-rectangle
66   (position (- (* diameter -0.5) SiOx_th) (* height -1)  0)
```

```
67    (position (+ (* diameter 0.5) SiOx_th) (* mask -1) 0)
68    "Oxide" "oxide")
69
70
71  ;; Begin Tcl code insert
72  !(
73    # Load variables from Epi
74    source n@node|epi@_epi.tcl
75
76    set num_regions [expr $epi(matdef,1,row)-1]
77    set mask  2
78    set offset 0
79    set wd 2
80
81    puts ";; num regions $num_regions"
82
83    for {set i 1} {$i < $num_regions} {incr i} {
84      set row [expr $num_regions-$i]
85
86      foreach {key test} [array get epi "region,*,region"] {
87        if { $row == $epi(region,$test,row)} {
88          set th [expr $epi(region,$test,thickness)]
89          set top [expr $offset + $th]
90          set bot [expr -1*($mask + $offset + $th)]
91          set dx [expr 0.5*$wd + $offset + $th ]
92          set mat "$epi(region,$test,material)"
93          puts ";; $row : $test"
94          puts "(sdegeo:create-rectangle"
95          puts "\t(position (* $dx -1) $bot 0)"
96          puts "\t(position $dx $top 0)"
97          puts "\t\"$mat\" \"$test\")"
98
99          set offset [expr $offset + $th]
100
101         puts "(sdegeo:fillet-2d (list"
102         puts "\t(car (find-vertex-id (position -$dx $bot 0)))"
103         puts "\t(car (find-vertex-id (position $dx $bot 0)))"
104         puts "\t(car (find-vertex-id (position -$dx $top 0)))"
105         puts "\t(car (find-vertex-id (position $dx $top 0))) )"
106         puts "\t$offset )"
107
```

```
108           break
109         }
110       }
111     }
112
113     set toplim [expr $offset + 3.5]
114     set pitch [expr $wd + $offset]
115
116     puts ";; Gas for EMW simulation"
117     puts ";; Top of the world: $toplim"
118     puts ";; Pitch: $pitch"
119     puts "(sdegeo:create-rectangle"
120     puts "\t(position (* (+ $wd $offset) -1) (* $epi(region,wire,thickness) -1) 0)"
121     puts "\t(position (+ $wd $offset) (+ $offset 3.5) 0)"
122     puts "\t\"Gas\" \"gas\" )"
123
124     puts ";; back reflector"
125     puts "(sdegeo:create-rectangle"
126     puts "\t(position (* (+ $wd $offset) -1) (* $epi(region,wire,thickness) -1) 0)"
127     puts "\t(position (+ $wd $offset) (- (* $epi(region,wire,thickness) -1) 0.5) 0)"
128     puts "\t\"Silver\" \"br\" )"
129
130 )!
131 ;; End Tcl code insert
132
133 (display "save-boundary") (newline)
134 (sdeio:save-tdr-bnd "all" (string-append fname ".tdr"))
135 ;;;
```

```
146       puts "(sdedr:define-constant-profile-region \"$region\_LTe\" \"$region\_LTe\"
      \"$region\" 0 \"Replace\")"
147       puts "(sdedr:define-constant-profile-region \"$region\_LTh\" \"$region\_LTh\"
      \"$region\" 0 \"Replace\")"
148     }
149   }
150 )!
151 ;; End Tcl code insert
152
153 ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
154 ; Dopant Placement
155 ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
156
157 ;; wire cell doping
158
159 ;; bkg doping
160 (sdedr:define-constant-profile "wire" "BoronActiveConcentration" 5.0E17)
161 (sdedr:define-constant-profile-region "wire" "wire" "wire" 0 "Replace")
162
163 ;; Gaussian emitter doping (courtesy of DBTE)
164 (sdedr:define-refinement-window "wireemtop" "Line"
165   (position (* diameter -0.5) 0 0)
166   (position (* diameter 0.5) 0 0))
167 (sdedr:define-refinement-window "wireemleft" "Line"
168   (position (* diameter -0.5) 0 0)
169   (position (* diameter -0.5) (* height -0.75) 0))
170 (sdedr:define-refinement-window "wireemleft" "Line"
171   (position (* diameter 0.5) 0 0)
172   (position (* diameter 0.5) (* height -0.75) 0))
173 (sdedr:define-gaussian-profile "wireem" "PhosphorusActiveConcentration"
174   "PeakPos" 0 "PeakVal" 1.0E+19 "Length" 0.05 "Erf" "Factor" 0.)
175 (sdedr:define-analytical-profile-placement "wireemtop" "wireem" "wireemtop" "Positive
      " "NoReplace" "Eval")
176 (sdedr:define-analytical-profile-placement "wireemright" "wireem" "wireemright" "
      Negative" "NoReplace" "Eval")
177 (sdedr:define-analytical-profile-placement "wireemleft" "wireem" "wireemleft" "
      Positive" "NoReplace" "Eval")
178
179 ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
180 ; Mesh Refinement
181 ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
```

```
# This section has been turned off for the EMW only simulations
#if 0
;; Global refinement
(sdedr:define-refinement-size "REF_global" 0.5 0.5 0 0.5 0.5 0)
(sdedr:define-refinement-window "WIN_global" "Rectangle"
  (position (* pitch -0.5) 0 0 )
  (position (* pitch 0.5) (+ height defectT tjT tjT topBaseT topEmitterT windowT
    TiOxT MgFT 3.5) 0)   )
(sdedr:define-refinement-placement "REF_global" "REF_global" "WIN_global")

;; Doping refinement
;(sdedr:define-refinement-size "doping" 0.1 0.05 0 0.1 0.05 )
;(sdedr:define-refinement-function "doping" "DopingConcentration" "MaxTransDiff" 1)
;(sdedr:define-refinement-placement "doping" "RefinementDefinition_Si" "WIN_global")

;; Bottom contact
(sdedr:define-refinement-window "WIN_bottom_contact" "Rectangle"
  (position (* diameter -0.5) 0 0)
  (position (* diameter 0.5) 0.2 0) )
(sdedr:define-multibox-size "SIZE_bottom_contact" hi_dx hi_dx hi_dx lo_dx 1 1.5)
(sdedr:define-multibox-placement "PLACE_bottom_contact" "SIZE_bottom_contact" "
    WIN_bottom_contact")

;; Si uw bottom cell refinement
(sdedr:define-refinement-window "WIN_Si_top" "Rectangle"
  (position (* diameter -0.5) height 0)
  (position (* diameter 0.5) (- height 0.2) 0) )
(sdedr:define-multibox-size "SIZE_Si_top" hi_dx hi_dx hi_dx lo_dx 1 -1.5)
(sdedr:define-multibox-placement "PLACE_Si_top" "SIZE_Si_top" "WIN_Si_top")

(sdedr:define-refinement-window "WIN_Si_R" "Rectangle"
  (position (- (* diameter 0.5) 0.2) (- height SiEmitterH 0.2) 0)
  (position (* diameter 0.5) height 0) )
(sdedr:define-multibox-size "SIZE_Si_R" hi_dx hi_dx lo_dx lo_dx -1.5 -1.5)
(sdedr:define-multibox-placement "PLACE_Si_R" "SIZE_Si_R" "WIN_Si_R")

(sdedr:define-refinement-window "WIN_Si_L" "Rectangle"
  (position (* diameter -0.5) (- height SiEmitterH 0.2) 0)
  (position (+ (* diameter -0.5) 0.2) height 0) )
(sdedr:define-multibox-size "SIZE_Si_L" hi_dx hi_dx lo_dx lo_dx 1.5 1.5)
(sdedr:define-multibox-placement "PLACE_Si_L" "SIZE_Si_L" "WIN_Si_L")
```

```
221
222 ; Defect region interface refinement
223 (extract-refwindow (find-face-id (position 0 (+ height defectT) 0)) "WIN_defect")
224 (sdedr:define-refinement-size "SIZE_defect" hi_dx hi_dx lo_dx lo_dx)
225 (sdedr:define-refinement-function "SIZE_defect" "MaxLenInt" "GaInP" "GaInP" 5e-3 1.5)
226 (sdedr:define-refinement-function "SIZE_defect" "MaxLenInt" "GaInP" "Silicon" 5e-3
        1.5)
227 (sdedr:define-refinement-placement "PLACE_defect" "SIZE_defect" "WIN_defect")
228
229 ; Base region interface refinement
230 (extract-refwindow (find-face-id (position 0 (+ height defectT tjT tjT topBaseT) 0))
        "WIN_topBase")
231 (sdedr:define-refinement-size "SIZE_topBase" hi_dx hi_dx lo_dx lo_dx)
232 (sdedr:define-refinement-function "SIZE_topBase" "MaxLenInt" "GaInP" "GaInP" 5e-3
        1.5)
233 (sdedr:define-refinement-placement "PLACE_topBase" "SIZE_topBase" "WIN_topBase")
234
235 ; Window region interface refinement
236 ;(extract-refwindow (find-face-id (position 0 (+ height defectT tjT tjT topBaseT
        topEmitterT windowT) 0)) "WIN_window")
237 ;(sdedr:define-refinement-size "SIZE_window" hi_dx hi_dx lo_dx lo_dx)
238 ;(sdedr:define-refinement-function "SIZE_window" "MaxLenInt" "AlInP" "GaInP" 5e-3
        1.5)
239 ;(sdedr:define-refinement-function "SIZE_window" "MaxLenInt" "AlInP" "TiOx" 5e-3 1.5)
240 ;(sdedr:define-refinement-placement "PLACE_window" "SIZE_window" "WIN_window")
241
242 ; Tunnel junction refinement
243 ;(extract-refwindow (find-face-id (position 0 (+ height defectT tjT
244
245 ; Constant refinement for window and tunnel junction
246 (sdedr:define-refinement-size "SIZE_tiny" tiny tiny tiny tiny)
247 (sdedr:define-refinement-region "PLACE_tj_n" "SIZE_tiny" "REGION_tj_n")
248 (sdedr:define-refinement-region "PLACE_tj_p" "SIZE_tiny" "REGION_tj_p")
249
250 # (sdedr:define-refinement-region "PLACE_window" "SIZE_tiny" "REGION_window")
251 #endif
252
253
254 ;;---------------------------------------
255 ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
256 ; MESHING!
```

```
;;;
```

```
21    InspectFile    = "@plot@"
22    LogFile   = "@log@"
23    TotalTimeSteps = 10000000
24    NumberOfThreads = maximum
25  }
26
27  ComplexRefractiveIndex {
28    WavelengthDep = {Real,Imag}
29  }
30
31
32  ## BOUNDARY CONDITIONS
33
34  Boundary {
35    Type    = Periodic
36    Sides   = {X}
37  }
38
39  Boundary {
40    Type    = CPML
41    Sides   = {Y}
42  }
43
44  PECMedia {
45    Region = {"br"}
46  }
47
48  ## EXCITATION
49
50  PlaneWaveExcitation {
51    BoxCorner1  = (@<-pitch*0.5>@, @<topOfTheWorld - 2>@, 0)
52    BoxCorner2  = (@< pitch*0.5>@, @<topOfTheWorld - 2>@, 0)
53    Theta   = 180
54    Psi   = 0
55    Wavelength  = @<1000.*@wl@>@
56    Intensity = 0.1
57    Nrise   = 4
58  }
59
60  ## SENSORS AND EXTRACTORS
61
```

```
62  Plot {
63    Name  = "n@node@_Eabs"
64    Quantity = {AbsElectricField, AbsMagneticField}
65    FinalPlot = yes
66  }
67
68  Extractor {
69    Name    = "n@node@_a"
70    Quantity  = {AbsorbedPhotonDensity}
71  }
72
73  Sensor {
74    Name    = "total"
75    Quantity  = PhotonFluxDensity
76    BoxCorner1  = (@< pitch*-0.5>@, @<topOfTheWorld - 3>@, 0)
77    BoxCorner2  = (@< pitch*0.5>@, @<topOfTheWorld - 3>@, 0)
78    Mode    = {Integrate}
79  }
80
81  Sensor {
82    Name    = "reflected"
83    Quantity  = PhotonFluxDensity
84    BoxCorner1  = (@< pitch*-0.5>@, @<topOfTheWorld - 1>@, 0)
85    BoxCorner2  = (@< pitch*0.5>@, @<topOfTheWorld - 1>@, 0)
86    Mode    = {Integrate}
87  }
88
89  Sensor {
90    Name       = "absorbed_total"
91    Quantity   = absorbedPhotonDensity
92    BoxCorner1 = (@< pitch*-0.5>@, @< height *-1 >@, 0)
93    BoxCorner2 = (@< pitch*0.5>@, topOfTheWorld, 0)
94    Mode       = {Integrate}
95  }
96
97  # Begin Tcl code insert
98  !(
99    # Load variables from Epi
100   source n@node|epi@_epi.tcl
101
102   # Add code to integrate absorbedPhotonDensity from EMW simulation for each region
```

```
103   foreach {key region} [array get epi "region,*,region"] {
104     puts "Sensor {"
105     puts "\tName\t=\"absorbed_$region\""
106     puts "\tQuantity\t= absorbedPhotonDensity"
107     puts "\tRegion\t= {\"$region\"}"
108     puts "\tMode\t= {Integrate}"
109     puts "}"
110   }
111 )!
112
113 Detector {
114   Tolerance = 1e-3
115 }
```

E.2.3 Creating generation maps and integrating optical generation

The field profiles generated by each FDTD simulation is weighted by the AM1.5G spectrum interpolated onto the device mesh.

Finally, the total generation current is considered. Separating the optics from the device physics allows for independent optimization before extracting the device physics.

Listing E.4: Code/emw/inspect_ins.cmd

```
1  load_library extend
2  set gc "[file tail [file rootname @plot@]]"
3  proj_load "$gc.plt"
4
5
6  set factor [expr 1e-12*1.6e-19*1e3/(2e-8)]
7
8  set p_Si [ ds_getValue $gc "IntegrSilicon OpticalGeneration" ]
9  set g_Si [ expr $p_Si*$factor ]
10 ft_scalar G_Si [format %.4g $g_Si]
11
12 #if 0
13 set p_GaInP [ ds_getValue $gc "IntegrGaInP OpticalGeneration" ]
14 set g_GaInP [ expr $p_GaInP*$factor ]
15 ft_scalar G_GaInP [format %.4g $g_GaInP]
```

```
16 #endif
17
18
19 set p_buf9 [ ds_getValue $gc "Integrbuf9 OpticalGeneration" ]
20 set p_buf8 [ ds_getValue $gc "Integrbuf8 OpticalGeneration" ]
21 set p_buf7 [ ds_getValue $gc "Integrbuf7 OpticalGeneration" ]
22 set p_buf6 [ ds_getValue $gc "Integrbuf6 OpticalGeneration" ]
23 set p_buf5 [ ds_getValue $gc "Integrbuf5 OpticalGeneration" ]
24 set p_buf4 [ ds_getValue $gc "Integrbuf4 OpticalGeneration" ]
25 set p_buf3 [ ds_getValue $gc "Integrbuf3 OpticalGeneration" ]
26 set p_buf2 [ ds_getValue $gc "Integrbuf2 OpticalGeneration" ]
27 set p_buf1 [ ds_getValue $gc "Integrbuf1 OpticalGeneration" ]
28 set p_buf0 [ ds_getValue $gc "IntegrGaP OpticalGeneration" ]
29
30 set g_buf [expr ($p_buf9+$p_buf9+$p_buf8+$p_buf7+$p_buf6+$p_buf5+$p_buf4+$p_buf3+
       $p_buf2+$p_buf1+$p_buf0)*$factor]
31 ft_scalar G_buf [format %.4g $g_buf]
32
33 set p_topfsf [ ds_getValue $gc "IntegrAlInP OpticalGeneration" ]
34 set p_topem [ ds_getValue $gc "Integrtopem OpticalGeneration" ]
35 set p_topbase [ ds_getValue $gc "Integrtopbase OpticalGeneration" ]
36 set p_topbsf [ ds_getValue $gc "Integrtopbsf OpticalGeneration" ]
37 set g_topcell [expr ($p_topem+$p_topbase+$p_topbsf+$p_topfsf)*$factor]
38 ft_scalar G_topcell [format %.4g $g_topcell]
39
40
41 set p_tdp [ ds_getValue $gc "Integrtdp OpticalGeneration" ]
42 set p_tdn [ ds_getValue $gc "Integrtdn OpticalGeneration" ]
43 set g_tj [expr ($p_tdp+$p_tdn)*$factor]
44 ft_scalar G_tj [format %.4g $g_tj]
```

E.3 Device simulation

E.3.1 Defining additional contacts

Since the device physics simulation includes options for probing the performance of individual junctions, the Structure Editor code includes preprocessor flags for defining additional

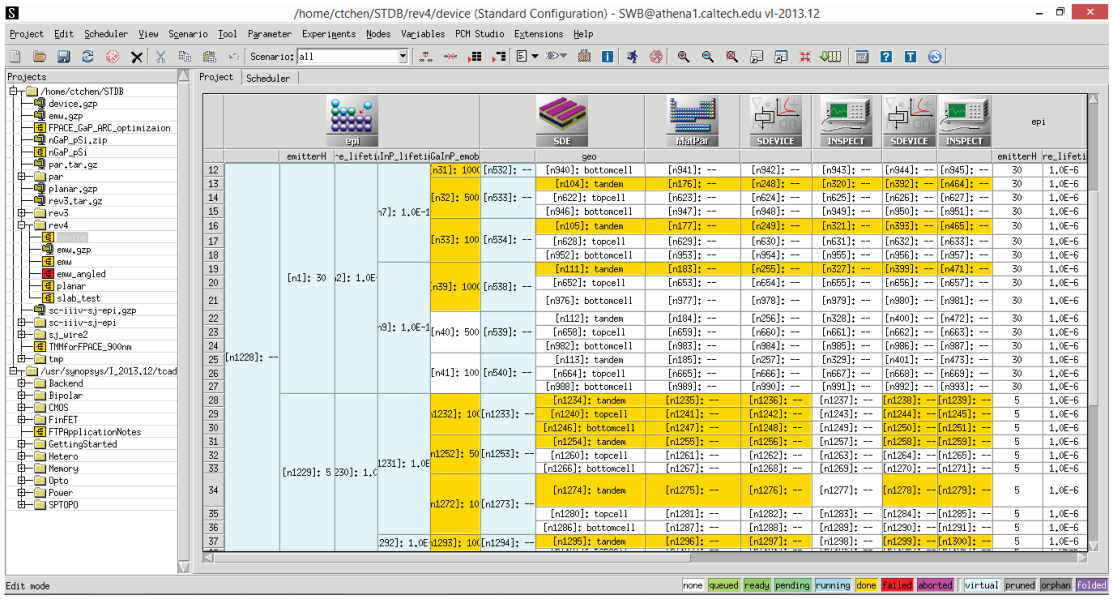


FIGURE E.2: Basic workflow in `swb` for the device simulations of a wire tandem device.

contacts.

LISTING E.5: Code/device/sde_dvs_diff.txt

```
#if [string match "topcell" "@geo@"]
  (display "add additional contact \n")
  (sdegeo:define-contact-set "middle" 4 (color:rgb 0 1 0) "##")
  (sdegeo:set-current-contact-set "middle")
  (sdegeo:define-2d-contact (find-edge-id (position 0 2.53  0)) "middle")
#elseif [string match "bottomcell" "@geo@"]
  (display "add additional contact \n")
  (sdegeo:define-contact-set "middle" 4 (color:rgb 0 1 0) "##")
  (sdegeo:set-current-contact-set "middle")
  (sdegeo:define-2d-contact (find-edge-id (position 0 0 0)) "middle")
#endif
```

E.3.2 Simulation

LISTING E.6: Code/device/sdevice1_des.cmd

```
* Sentaurus Device - Tandem Wire Array Device Simulation
```

```
2  * Chris Chen (c) 2015
3  * Based on code by Synopsys, Dr. Mike Kelzenberg, and Dr. Daniel Turner-Evans
4
5  # Make sure that Epi has been run to provide the variables necessary for the Tcl
       inserts
6  #setdep @node|epi@
7  #if ![file exists n@node|epi@_epi.tcl]
8    # Epi tcl file doesn't exist. Run epi first!
9    #exit
10 #endif
11
12
13 File  {
14   *-Input
15       Grid    = "n@node|sde@_el_msh.tdr"
16       LifeTime = "n@node|sde@_el_msh.tdr"
17       Parameters ="@parameter@"
18       OpticalGenerationInput = "n@node|sdevice@_des.tdr"
19   *-Output
20       Plot    = "@tdrdat@"
21       Current = "@plot@"
22       Output  = "@log@"
23       NonLocalPlot = "n@node@_nl"
24 }
25
26
27 Electrode {
28   { Name="cathode"  Voltage=0 hRecVelocity = 100} * top contact
29   { Name="anode"  Voltage=0 eRecVelocity = 100} * bottom contact
30   #if ![string match "tandem" "@geo@"]
31   * Middle contact defined for single cell simulations
32   { Name="middle"  Voltage=0 eRecVelocity = 100}  * bottom contact
33   #endif
34 }
35
36
37 Physics {
38     AreaFactor = @<1.0E+11/5.559/2>@ * to get current in mA/cm^2
39
40     Fermi
41     Recombination( SRH )
```

```
42      ThermionicEmission
43
44        eBarrierTunneling "TD_NLM" (
45              Band2Band
46              TwoBand
47        )
48
49        hBarrierTunneling "TD_NLM"(
50              Band2Band
51              TwoBand
52        )
53
54      Optics (
55            OpticalGeneration (
56          ReadFromFile (
57              Scaling =0
58              TimeDependence (
59                    WaveTime = (0.9, 10)
60                    Scaling = 1.0
61              )
62          )
63            )
64        )
65  }
66
67  * Begin materials/region physics definitions!
68  * Initialize all GaInP region physics models from Epi
69  !(
70    source n@node|epi@_epi.tcl
71
72    foreach {key region} [array get epi "region,*,region"] {
73      if {[string match "GaInP*" "$epi(region,$region,material)"]} {
74        puts "Physics (region=\"$region\") {"
75        puts "\tMobility(ConstantMobility)"
76        puts "\tRecombination(Radiative Auger)"
77        puts "\tMoleFraction ( xFraction = $epi(region,$region,xMole) )"
78        puts "}"
79      }
80
81    }
82  )! * tcl script for writing out all GaInP region physics
```

```
83
84  * Explicit materials physics model definitions
85  Physics (material="Silicon") {
86    Mobility (
87      DopingDependence
88      HighFieldSaturation
89    )
90  }
91
92  Physics (material="AlInP") {
93      EffectiveIntrinsicDensity(NoBandgapNarrowing)
94      Mobility( ConstantMobility  )
95      Recombination( Radiative ) # no Auger model currently defined!
96      # Recombination( Radiative  Auger )
97  }
98
99  * Begin interface physics definitions!
100
101 #if 1
102 !(
103   source "n@node|epi@_epi.tcl"
104   foreach {key interface} [array get epi "matintdef,*,material"] {
105     puts "Physics (materialInterface=\"$interface\") {"
106     puts "\tRecombination (surfaceSRH)"
107     puts "}\n"
108   }
109 )!
110 #else
111 Physics (materialInterface="Silicon/GaP") {
112     Recombination(surfaceSRH)
113 }
114
115 Physics (materialInterface="TiOx/AlInP") {
116     Recombination(surfaceSRH)
117 }
118
119 Physics (materialInterface="Oxide/Silicon") {
120     Recombination(surfaceSRH)
121 }
122
123 Physics (materialInterface="Oxide/GaInP") {
```

```
124     Recombination(surfaceSRH)
125 }
126 #endif
127
128
129
130 Plot {
131   xMoleFraction Doping DonorConcentration AcceptorConcentration
132   eEffectiveStateDensity hEffectiveStateDensity EffectiveIntrinsicDensity
        IntrinsicDensity
133   eDensity hDensity SpaceCharge
134   eQuasiFermiPotential hQuasiFermiPotential BandGap ConductionBandEnergy
        ValenceBandEnergy ElectronAffinity
135   ElectricField ElectricField/vector ElectrostaticPotential
136   eLifetime hLifetime SRH Auger TotalRecombination SurfaceRecombination
        RadiativeRecombination
137   eCurrent/Vector hCurrent/Vector current/vector
138   eMobility hMobility eVelocity hVelocity
139   SRH Auger TotalRecombination SurfaceRecombination RadiativeRecombination
140   BarrierTunneling
141   eBarrierTunneling hBarrierTunneling
142   NonLocal
143   OpticalGeneration
144 }
145
146 NonLocalPlot ((0, 0)) {
147   ConductionBand  ValenceBand
148   hDensity  eDensity
149   hQuasiFermi  eQuasiFermi
150   NonLocal
151 }
152
153 Math {
154   -CheckUndefinedModels
155     RhsMin = 1E-12
156     Extrapolate
157     Derivatives
158     RelErrControl
159     Iterations = 10
160     ExtendedPrecision
161     Digits = 7
```

```
162     Notdamped = 100
163     ErrRef(electron) = 1E0
164     ErrRef(hole) = 1E0
165     ExitOnFailure
166     Number_of_Threads = 8
167     StackSize = 20000000  * 20MB; needed for NewRayTracer
168     Method=ParDiso
169   #Method=ILS
170     NonLocal "TD_NLM" (
171         RegionInterface = "tdn/tdp"
172         Length=15e-7           # [cm] distance to anchor point
173         Permeation = 15e-7
174     )
175
176     DirectCurrent
177
178   # Cylindrical(0.0)
179
180     Transient = BE
181     TransientDigits = 7
182     TransientErrRef(electron) = 1E0
183     TransientErrRef(hole) = 1E0
184
185   * CNormPrint
186 }
187
188 Solve {
189
190     NewCurrentPrefix = "tmp_"
191
192     Coupled  { poisson }
193     Plot( FilePrefix = "n@node@_Banddgm")
194 #   Coupled  { poisson electron }
195 #   Coupled  { poisson hole }
196 #   Coupled  { poisson electron hole }
197     Transient (
198       InitialStep=1e-18 MaxStep =0.2 MinStep = 1e-40 Increment=2
199       InitialTime=0 FinalTime=1
200     ){ Coupled (Iterations=10) {Poisson Electron Hole  } }
201
202
```

```
203     NewCurrentPrefix = "Light_IV"
204
205   #if [string match "topcell" "@geo@"]
206     Quasistationary (
207       InitialStep=1e-4 MaxStep =5e-3 MinStep = 1e-30 Increment=1.7 DoZero
208       Goal{ voltage = -1.3 Name="cathode" }
209     ){ Coupled {Poisson Electron Hole  }
210        Plot( FilePrefix = "n@node@_Banddgm_Jsc" Time = (0) )
211      }
212
213     Save( FilePrefix = "tmp_n@node@_Banddgm_Jsc" )
214
215     NewCurrentPrefix = "tmp_2"
216
217     Quasistationary (
218       InitialStep=1e-2 MaxStep =0.1 MinStep = 1e-30 Increment=1.5 DoZero
219       Goal{ current = 0 Name="cathode" }
220     ){ Coupled {Poisson Electron Hole  }
221      }
222        Plot( FilePrefix = "n@node@_Banddgm_Voc")
223   #elseif [string match "bottomcell" "@geo@"]
224     Quasistationary (
225       InitialStep=1e-4 MaxStep =5e-3 MinStep = 1e-30 Increment=1.7 DoZero
226       Goal{ voltage = 0.7 Name="anode" }
227     ){ Coupled {Poisson Electron Hole  }
228        Plot( FilePrefix = "n@node@_Banddgm_Jsc" Time = (0) )
229      }
230
231     Save( FilePrefix = "tmp_n@node@_Banddgm_Jsc" )
232
233     NewCurrentPrefix = "tmp_2"
234
235     Quasistationary (
236       InitialStep=1e-2 MaxStep =0.1 MinStep = 1e-30 Increment=1.5 DoZero
237       Goal{ current = 0 Name="anode" }
238     ){ Coupled {Poisson Electron Hole  }
239      }
240        Plot( FilePrefix = "n@node@_Banddgm_Voc")
241   #else
242     Quasistationary (
243       InitialStep=1e-4 MaxStep =5e-3 MinStep = 1e-30 Increment=1.7 DoZero
```

```
244       Goal{ voltage = 2.1 Name="anode" }
245     ){ Coupled {Poisson Electron Hole  }
246        Plot( FilePrefix = "n@node@_Banddgm_Jsc" Time = (0) )
247      }
248
249     Save( FilePrefix = "tmp_n@node@_Banddgm_Jsc" )
250
251     NewCurrentPrefix = "tmp_2"
252
253     Quasistationary (
254       InitialStep=1e-2 MaxStep =0.1 MinStep = 1e-30 Increment=1.5 DoZero
255       Goal{ current = 0 Name="anode" }
256     ){ Coupled {Poisson Electron Hole  }
257      }
258        Plot( FilePrefix = "n@node@_Banddgm_Voc")
259
260   #endif
261
262   System("rm -f tmp*") *remove the plot we dont need anymore.
263   System("rm -f tmp2*") *remove the plot we dont need anymore.
264 }
```

E.3.3 Extracting Useful Parameters

Listing E.7: Code/device/inspect1_ins.cmd

```
1
2  # Plot light J-V and P-V curves and extract Photovoltaic parameters
3  # or Plot dark J-V characteristics
4
5  # #setdep @node|sdevice1@
6
7  set N     @node@
8  set i     @node:index@
9
10 # proj_load  @plot@ PLT_JV($N)
11 proj_load  Light_IVn@previous@_des.plt PLT_JV($N)
12
13 #- Automatic alternating color assignment tied to node index
14 #-------------------------------------------------------------------#
```

```
15 set COLORS  [list orange green blue red violet brown orange magenta]
16 set NCOLORS [llength $COLORS]
17 set color   [lindex  $COLORS [expr $i%$NCOLORS]]
18
19 #if [string match "topcell" "@geo@"]
20 # Plot light J-V characteristics and extract PV parameters
21 cv_createDS J($N)  "PLT_JV($N) cathode OuterVoltage" "PLT_JV($N) cathode TotalCurrent
       "
22
23 cv_inv J($N) y
24
25 cv_create V($N)  "PLT_JV($N) cathode OuterVoltage" "PLT_JV($N) cathode OuterVoltage"
26
27 cv_createWithFormula P($N)  "<V($N)>*<J($N)>" A A
28 cv_display P($N) y2
29
30 cv_setCurveAttr J($N)  "light-JV" $color solid  2 circle 3 defcolor 1 defcolor
31 cv_setCurveAttr P($N)  "light-PV" $color dashed  2 none 3 defcolor 1 defcolor
32
33 gr_setAxisAttr X {Voltage (V)}  16 {} 0 black 1 14 0 5 0
34 gr_setAxisAttr Y {Current Density (mA/cm^2)} 16 -30 0  black 1 14 0 5 0
35 gr_setAxisAttr Y2 {Power (mW/cm^2)} 16 0 26  black 1 14 0 5 0
36
37 # Extract Photovoltaic parameters
38 # Extract short circuit current density, Jsc [mA/cm^2]
39 set Jsc($N) [cv_compute "vecvaly(<J($N)>,0)" A A A A]
40 ft_scalar Jsc [format %.2f [expr -1*$Jsc($N)]]
41
42 # Extract open circuit voltage, Voc [V]
43 set Jmin [cv_compute "vecmin(<J($N)>)" A A A A]
44 if {$Jmin <= 0} {
45   set Voc($N) [expr [cv_compute "veczero(<J($N)>)" A A A A]]
46 } elseif {$Jmin <= 1e-6} {
47   set Voc($N) [expr [cv_compute "vecvalx(<J($N>,$Jmin)" A A A A]]
48 }
49 ft_scalar Voc [format %.4f [expr -1*$Voc($N)]]
50
51 # Extract fill factor (FF), maximum power outpout (Pm [mW/cm2]) and efficiency (eff)
52   set Ps 100 ;#Incident light power density for AM1.5g radiation in mW/cm^2
53
54 if {$Voc($N) < 0} {
```

```
55    set Pm($N) [cv_compute "vecmax(<P($N)>)" A A A A]
56    ## fillfactor in %
57    set FF($N) [expr $Pm($N)/($Voc($N)*$Jsc($N))*100]
58    ## efficiency in % (mW/cm^2/(100mW/cm^2)*100%)
59    set Eff($N) [expr $Pm($N)/$Ps*100]
60  }
61  #else
62
63  # Plot light J-V characteristics and extract PV parameters
64  cv_createDS J($N)  "PLT_JV($N) anode OuterVoltage" "PLT_JV($N) anode TotalCurrent"
65
66  cv_inv J($N) y
67
68  cv_create V($N)  "PLT_JV($N) anode OuterVoltage" "PLT_JV($N) anode OuterVoltage"
69
70  cv_createWithFormula P($N)  "<V($N)>*<J($N)>" A A
71  cv_display P($N) y2
72
73  cv_setCurveAttr J($N)  "light-JV" $color solid  2 circle 3 defcolor 1 defcolor
74  cv_setCurveAttr P($N)  "light-PV" $color dashed  2 none 3 defcolor 1 defcolor
75
76  gr_setAxisAttr X {Voltage (V)}  16 0 {} black 1 14 0 5 0
77  gr_setAxisAttr Y {Current Density (mA/cm^2)} 16 0 30  black 1 14 0 5 0
78  gr_setAxisAttr Y2 {Power (mW/cm^2)} 16 0 26  black 1 14 0 5 0
79
80  # Extract Photovoltaic parameters
81  # Extract short circuit current density, Jsc [mA/cm^2]
82  set Jsc($N) [cv_compute "vecvaly(<J($N)>,0)" A A A A]
83  ft_scalar Jsc [format %.2f $Jsc($N)]
84
85  # Extract open circuit voltage, Voc [V]
86  set Jmin [cv_compute "vecmin(<J($N)>)" A A A A]
87  if {$Jmin <= 0} {
88    set Voc($N) [expr [cv_compute "veczero(<J($N)>)" A A A A]]
89  } elseif {$Jmin <= 1e-6} {
90    set Voc($N) [expr [cv_compute "vecvalx(<J($N>,$Jmin)" A A A A]]
91  }
92  ft_scalar Voc [format %.4f $Voc($N)]
93
94  # Extract fill factor (FF), maximum power outpout (Pm [mW/cm2]) and efficiency (eff)
95    set Ps 100 ;#Incident light power density for AM1.5g radiation in mW/cm^2
```

```
96
97  if {$Voc($N) > 0} {
98    set Pm($N) [cv_compute "vecmax(<P($N)>)" A A A A]
99    ## fillfactor in %
100   set FF($N) [expr $Pm($N)/($Voc($N)*$Jsc($N))*100]
101   ## efficiency in % (mW/cm^2/(100mW/cm^2)*100%)
102   set Eff($N) [expr $Pm($N)/$Ps*100]
103 }
104
105 #endif
106 ft_scalar Pm [format %.4f $Pm($N)]
107 ft_scalar FF  [format %.4f $FF($N)]
108 ft_scalar Eff  [format %.4f $Eff($N)]
```

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