

I

A RECIRCULATING CHARGE-COUPLED DEVICE

II

THE MERCURY SELENIDE ON N-SILICON SCHOTTKY BARRIER

Thesis by

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ii

to my mother
from the land of oz

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ABSTRACT

A recirculating charge-coupled device structure has been devised. Entrance and exit gates allow a signal to be admitted, recirculated a given number of times, and then examined. In this way a small device permits simulation of a very long shift register without passing the signal through input and output diffusions. An oscilloscope motion picture demonstrating degradation of an actual circulating signal has been made. The performance of the device in simulating degradation of a signal by a very long shift register is well fit by a simple model based on transfer inefficiency.

Electrical properties of the mercury selenide on n-type chemically-cleaned silicon Schottky barrier have been studied. Barrier heights measured were 0.96 volts for the photoresponse technique and 0.90 volts for the current-voltage technique. These are the highest barriers yet reported on n-type silicon.

TABLE OF CONTENTS

	page
I. A RECIRCULATING CHARGE-COUPLED DEVICE	1
A. Overview	1
B. Introduction	4
C. Device Construction and Operation	7
D. Experimental Results	10
E. Charge Transfer Model	13
F. Frequency and Temperature Dependence	16
G. Conclusion	19
H. Appendices	20
I. References	23
II. THE MERCURY SELENIDE ON N-SILICON SCHOTTKY BARRIER	24
A. Overview	24
B. Background and Motivation	26
C. Sample Preparation	30
D. Measurements	32
E. Results	36
F. Conclusion	39
G. References	40

I. A RECIRCULATING CHARGE-COUPLED DEVICE

A. OVERVIEW

Following its invention at Bell Telephone Laboratories in 1970, the Charge-Coupled Device (CCD) quickly became an important member of the family of semiconductor devices. The CCD approach has permitted construction of digital memories with far more bits per unit area than possible with other techniques. It has permitted the construction of high-resolution imaging devices without the cumbersome vacuum tubes and electron beams normally required. It has permitted the simple construction of complex devices like analog delay lines and transversal filters- devices which formerly required elaborate circuits with many parts.

The CCD uses the technology developed for the manufacture of planar integrated electronic circuits on semiconductor crystal surfaces. Unlike most integrated circuits, however, the CCD cannot be simulated by wiring together a number of discrete transistors and other devices. It will only work when made with the microscopic integrated technology.

In the CCD, information is represented by packets of charge at the interface between the semiconductor and a dielectric insulator. This charge is confined by creating

"wells" in the electric potential at the semiconductor surface. The wells are created and manipulated by clock voltages applied to electrodes on the surface of the insulator. In this way, a potential well can move across the semiconductor surface. The charge flows along, always moving to the region of lowest energy.

The dynamic response of the stored charge to the manipulation of the semiconductor surface potential determines the operating characteristics of a CCD. This response is determined by device geometry and by transport phenomena- diffusion, drift in the fringing electric field between gate electrodes, and mutual repulsion of the like charges. These limitations imposed by transport phenomena are affected by operating parameters- including clock frequency and temperature.

Two questions to ask when evaluating the CCD approach for a particular application are: (1) How long a device can one build, that is, how many transfers can a charge packet endure before the information it contains is lost; and (2) how are the characteristics of the device changed at low temperature?

The first question is particularly relevant to digital memory and analog delay line applications. Such devices require long registers so that the number of bits or samples stored is large compared to the number of input

and output ports.

The second question is relevant to infrared imaging devices. For such applications the device must often be cooled or it will be saturated by its own self-blackbody radiation.

This work describes a special device designed to explore the first question and discusses its use in both of these areas of interest.

B. INTRODUCTION

The typical Charge-Coupled Device (CCD)(1) shift register made on the surface of a semiconductor crystal consists of (1) an input device, usually a junction and adjacent gate; (2) the CCD channel itself with its array of overlapping gates to propel the signal down the device; and (3) the output device, an amplifier for boosting the small signal charge to a useful level. See figure 1.



Figure 1. A Typical CCD Shift Register

The output signal is a delayed function of the input signal after being influenced by all three of these components, and positive separation of input, channel, and output effects can be difficult. A technique has been conceived independently by the author and by the technical staff of the Hughes Aircraft Company which permits separation of CCD channel effects from input/output effects. Using a CCD with a closed-path channel, a signal can be

admitted, recirculated a number of times (like automobiles on a racetrack), and then examined, by appropriate clocking of a few control electrodes. The output is then studied as a function of the number of "laps" the signal made around the device, and the degradation caused by increasing the number of transfers examined. Figure 2 is a block diagram of the arrangement.

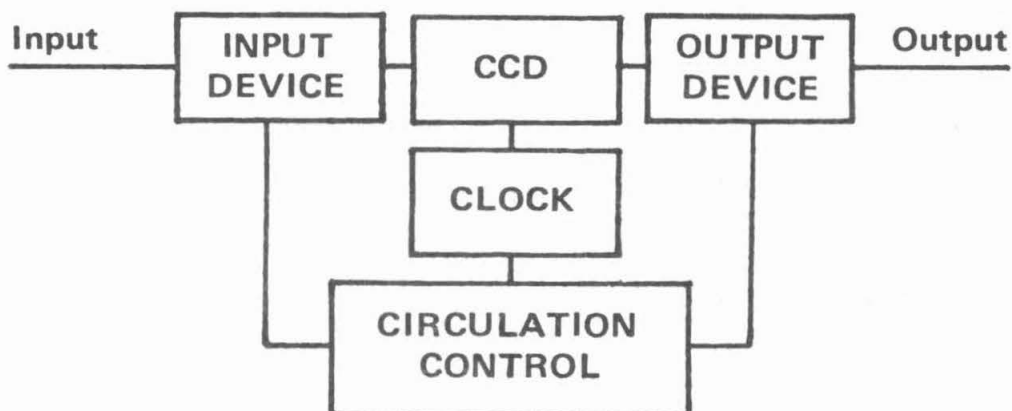


Figure 2. Block Diagram of Recirculating CCD Setup

One might be tempted to use an ordinary linear CCD to simulate a long shift register by admitting a signal shorter than the device and passing it back and forth from end to end before examination. The uncertainties associated with direction reversal, inability to provide bias charge ("fat zero") in the reverse direction, and complex clocking scheme required all discourage this

approach. The recirculating CCD has none of these problems.

This recirculating method of using a small device to simulate a very long shift register is somewhat like the feedback approach taken by Levine (2), except that this scheme avoids repeated passing of the signal through input and output diffusions. Levine's method (Figure 3) of

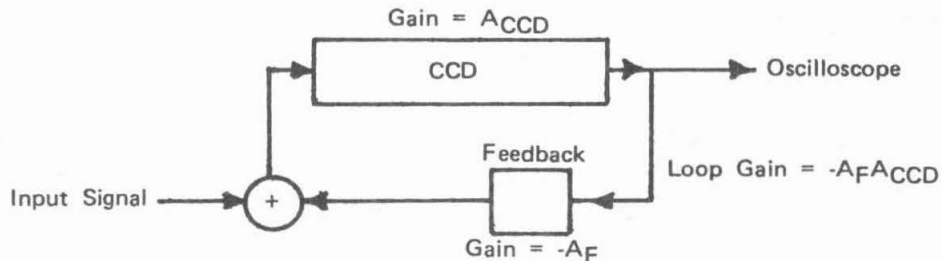


Figure 3. Levine's Method of Negative Feedback

negative feedback provides a self-regulating circulating bias charge, which has some advantages in the measurement of charge transfer efficiency. In the recirculating CCD, the potential wells eventually fill with thermally-generated charge, as in a long linear device. Hence the recirculating CCD is a realistic simulation of an operating long shift register.

C. DEVICE CONSTRUCTION AND OPERATION

The device was fabricated on silicon by Hughes Aircraft Company, Newport Beach, California, with two-phase aluminum-polysilicon overlapping gate technique (3) with a surface p-channel width of $10\ \mu\text{m}$ and a length of $20\ \mu\text{m}$ per stage, or $40\ \mu\text{m}$ per bit. These dimensions were modified at the "corners" of the closed-path channel. Figure 4 is a plan of the n^+ channel-stop diffusion made to define the device area. Constructed as a long rectangle with 32 stages (16 bits) on each side, the device has

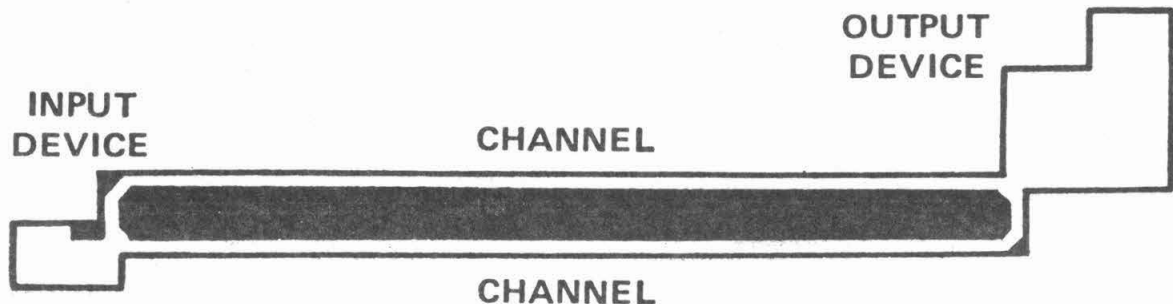


Figure 4. Plan of Recirculating CCD

a total storage capacity of 32 bits. Placing input and output structures at opposite ends means any odd multiple of 16 bits delay can be achieved with suitable clocking.

Figure 5 is an enlargement of one corner showing the input scheme. The "corner" polysilicon storage gate is overlapped by two aluminum channel gates and a third aluminum input gate connecting it with the input

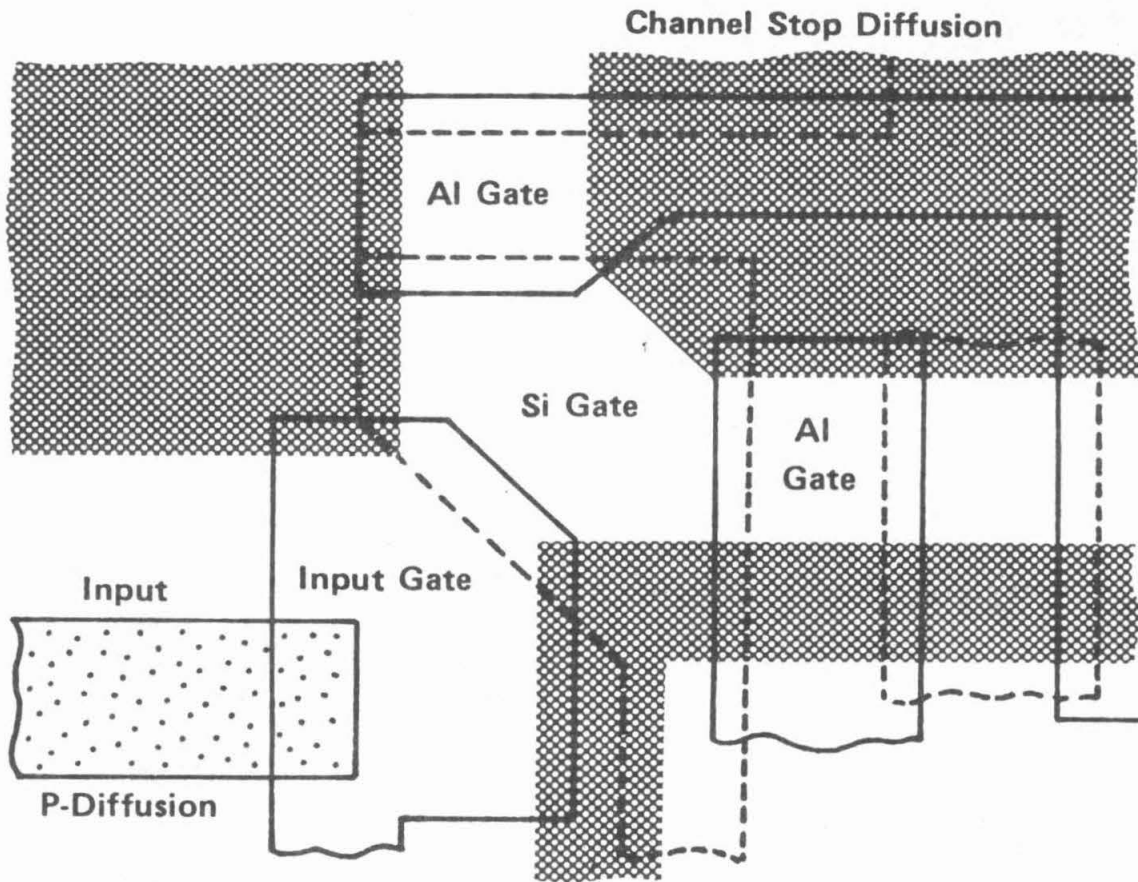


Figure 5. Input Arrangement

diffusion. When the storage gate is "on," strobing the input gate admits charge into the channel from the diffusion.

A similar arrangement is used for the output. An output gate connects the channel storage polysilicon gate with a floating output diffusion. Turning this gate on "hard" diverts the flow of charge from the channel into the output diffusion where it is sensed by an on-chip

source-follower transistor. Another transistor resets the diffusion between output bits.

In operation, the shift register gates above the channel are clocked continuously. The output gate is first turned on for 32 bits to display the stored signal. Then the input gate is strobed for 32 bits to admit a new input signal. This is circulated as many "laps" as desired before being displayed. Each output cycle is immediately followed by an input to provide a frequently refreshed display.

D. EXPERIMENTAL RESULTS

The device has been operated at clock frequencies between 20 Khz and 1 Mhz at both room temperature and 77 °K, the latter by simply immersing it in liquid nitrogen. For an input of an alternating sequence of four "ones" and four "zeroes," figure 6 shows the output obtained for several delays, clocking at 100 Khz. Initially, the signal introduced includes a "fat zero" bias charge of about 20% of a full well. Rapid degradation of the first data bit is caused by loading the signal into an essentially empty channel. From the oscilloscope display, a motion picture has been made of the device output by increasing the delay by 32 bits for each two frames. This movie provides an interesting qualitative view of the degradation of the circulating signal. Measurement of these photographs and calculation of the fractional loss per transfer yield the data plotted in figure 7. These measurements were made on the leading bit of the last packet of "ones" in each case, initially and after several hundred transfers. The gradual thermal filling of all buckets, important after several thousand transfers, was ignored.

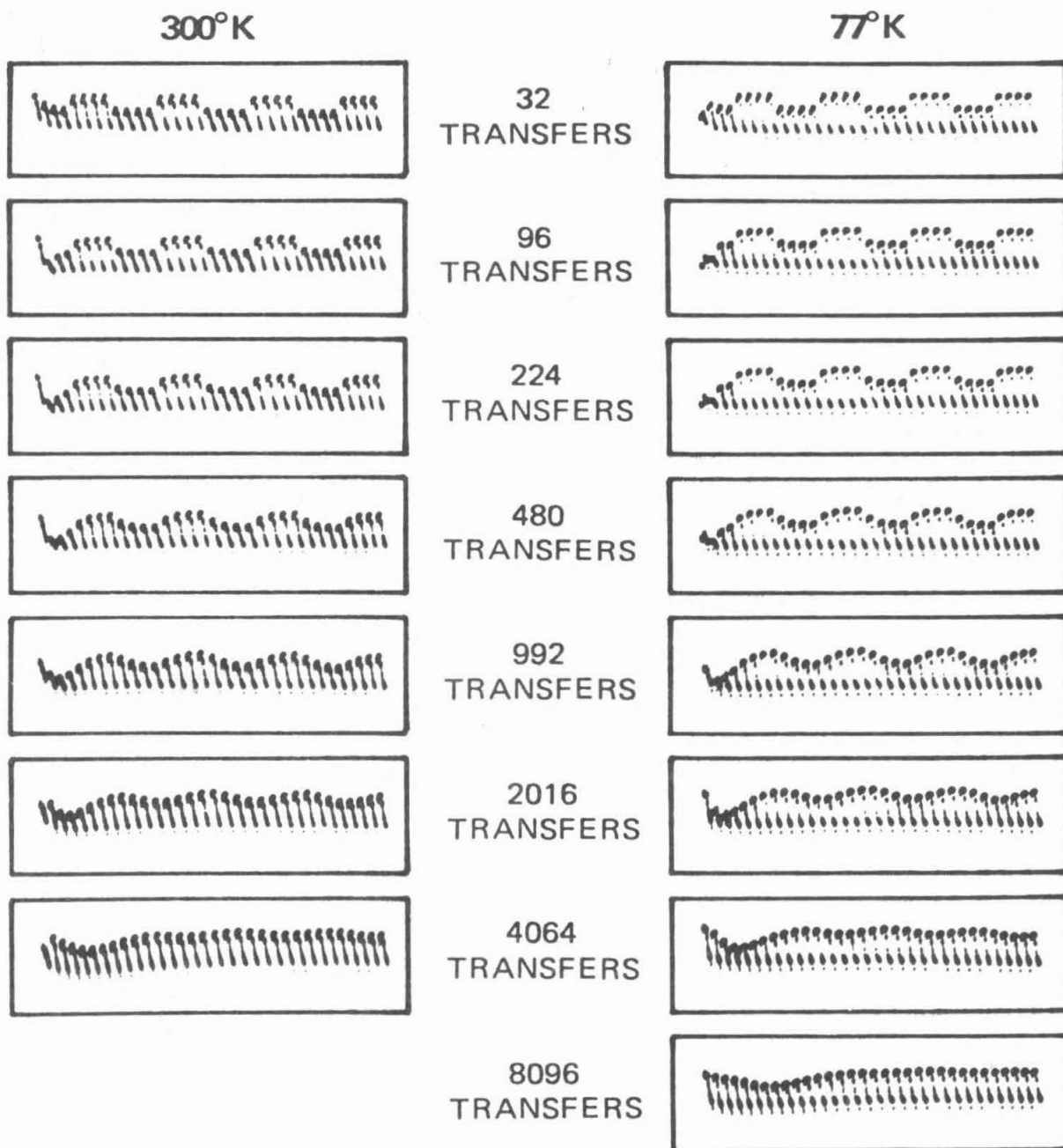


Figure 6. CCD Output for Various Delays with 100 Khz Clock

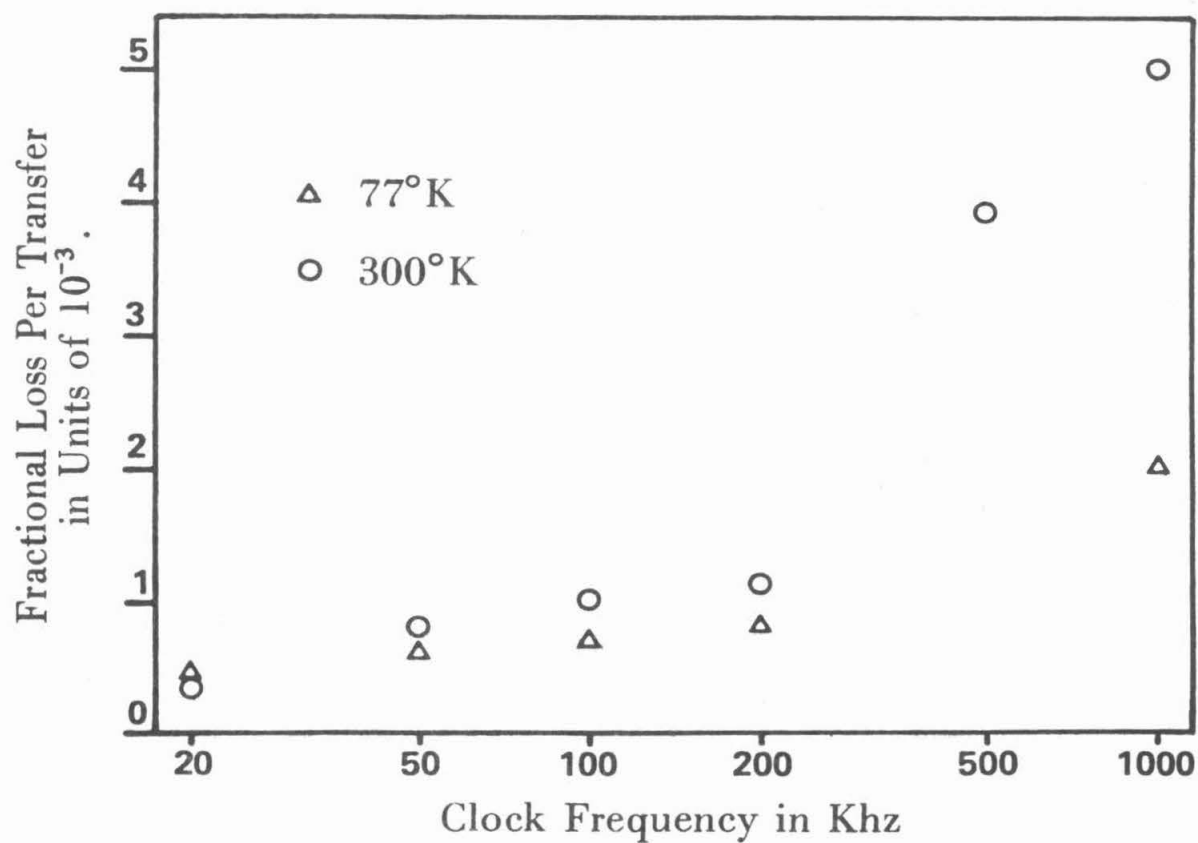


Figure 7. Charge Transfer Efficiency as a Function of Clock Frequency and Temperature

E. CHARGE TRANSFER MODEL

The appearance of the degraded output signal, as recorded in the movie frames, can be compared to that predicted by a simple model of the charge transfer process. Consider a 32-bit signal circulating in the device, where the bit heights (sizes of charge packets) are given by B_n , $n = 1, 2, \dots, 32$. At time t , the size of bit N is $B_N(t)$. One transfer later, the size of bit N is $B_N(t+1)$. Time, in a clocked system, is an integer.

When a bit is transferred from bucket to bucket, a fraction α makes the move. A fraction ϵ is left behind and added to the next bit. Generally $\alpha + \epsilon = 1$, but because of charge trapping effects this equality can be violated.

Suppose at time $t = 0$ a single bit, B_0 , has the value 1 and all the other bits are 0. At time $t = 1$, $B_0 = \alpha$ and $B_1 = \epsilon$. Applying this rule repeatedly gives table 1. Note that the terms in each line are simply the terms in the expansion of $(\alpha + \epsilon)^t$, that is,

$$B_n(t) = \binom{t}{n} \epsilon^n \alpha^{t-n}$$

where $\binom{t}{n}$ is the binomial coefficient, $\binom{t}{n} = \frac{t!}{n!(t-n)!}$

This simple model assumes that ϵ is independent of the size of the charge packet. By letting $\alpha + \epsilon = 1$, and

		BIT NUMBER				
		B ₀	B ₁	B ₂	B ₃	B ₄
TIME	t=0	1				
	t=1	α	ϵ			
	t=2	α^2	$2\alpha\epsilon$	ϵ^2		
	t=3	α^3	$3\alpha^2\epsilon$	$3\alpha\epsilon^2$	ϵ^3	
	t=4	α^4	$4\alpha^3\epsilon$	$6\alpha^2\epsilon^2$	$4\alpha\epsilon^3$	ϵ^4
						ETC

Table 1. Spreading of Charge in a Single Bit Caused by Transfer Inefficiency.

using the values of ϵ plotted in figure 7 for the data displayed in figure 6, namely

$$\begin{aligned}\epsilon &= 0.0011 \text{ at } 300 \text{ }^\circ\text{K, clocking at } 100 \text{ Khz} \\ \epsilon &= 0.0007 \text{ at } 77 \text{ }^\circ\text{K, clocking at } 100 \text{ Khz,}\end{aligned}$$

plots of computed output as a function of the number of transfers can be produced by superposing a solution of the above form for each "1" bit in the data pattern admitted into the CCD. These plots are displayed as figure 8 for the same cases as the data displayed in figure 6.

The agreement in appearance between the observed output and that predicted by the model is strong, and confirms that this simple model describes the transfer process satisfactorily, at least for small numbers of transfers.

At very large numbers of transfers, say above 4000, the model suggests a larger signal than that actually observed. This is due to the growing importance of the

thermally generated charge which eventually fills all the potential wells.

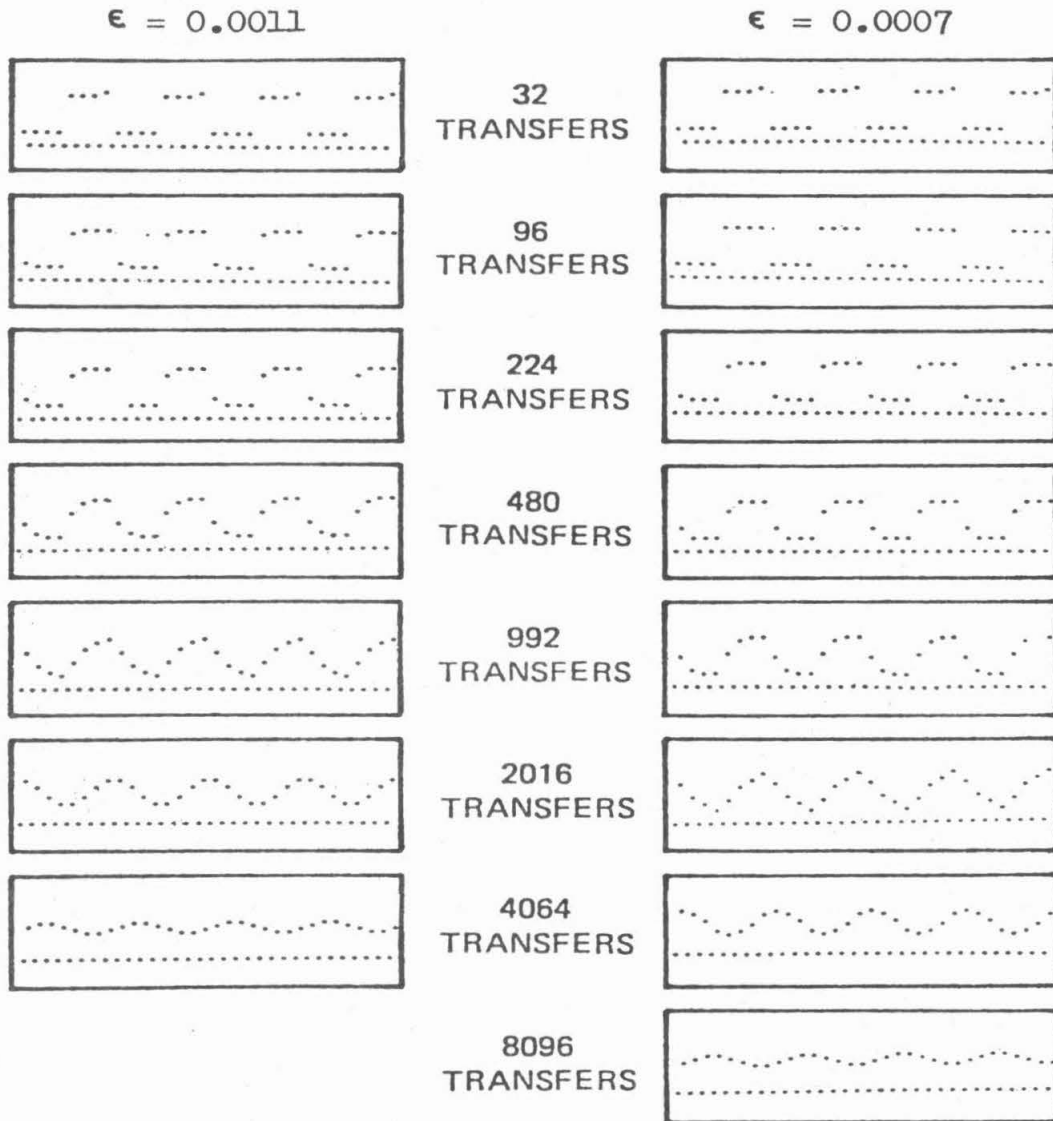


Figure 8. CCD Output Predicted by Simple Model

F. FREQUENCY AND TEMPERATURE DEPENDENCE

The transfer inefficiency in the previous section is a measured quantity strongly dependent on device construction and electrical parameters. Some investigation of this relationship is required to explain the observed temperature and frequency dependence reported in figure 7. As discussed by Mohsen, et al., (4) CCD transfer inefficiency at low clock frequencies is dominated by trapping of charge in interface states, particularly those states under the edges of the gates parallel to the channel. At high frequencies, transfer inefficiency is dominated by incomplete free charge transfer. Modeling a device similar in size to the recirculating CCD, Mohsen, et al., determined that the change from one regime to the other could be expected at a clock frequency around 500 KHz.

Such a transition occurs in the data recorded for the recirculating CCD. Figure 7 is reproduced, with lines sketched in, as figure 9. The two regimes are indicated.

At high frequencies, the free charge transfer in a small device is limited primarily by the mobility of minority carriers in the inversion layer. Leistiko, et al., (5) report an increase in inversion layer hole mobility of about a factor of 4.5 on cooling from room temperature to 77°K. The observed decrease in transfer inefficiency by a

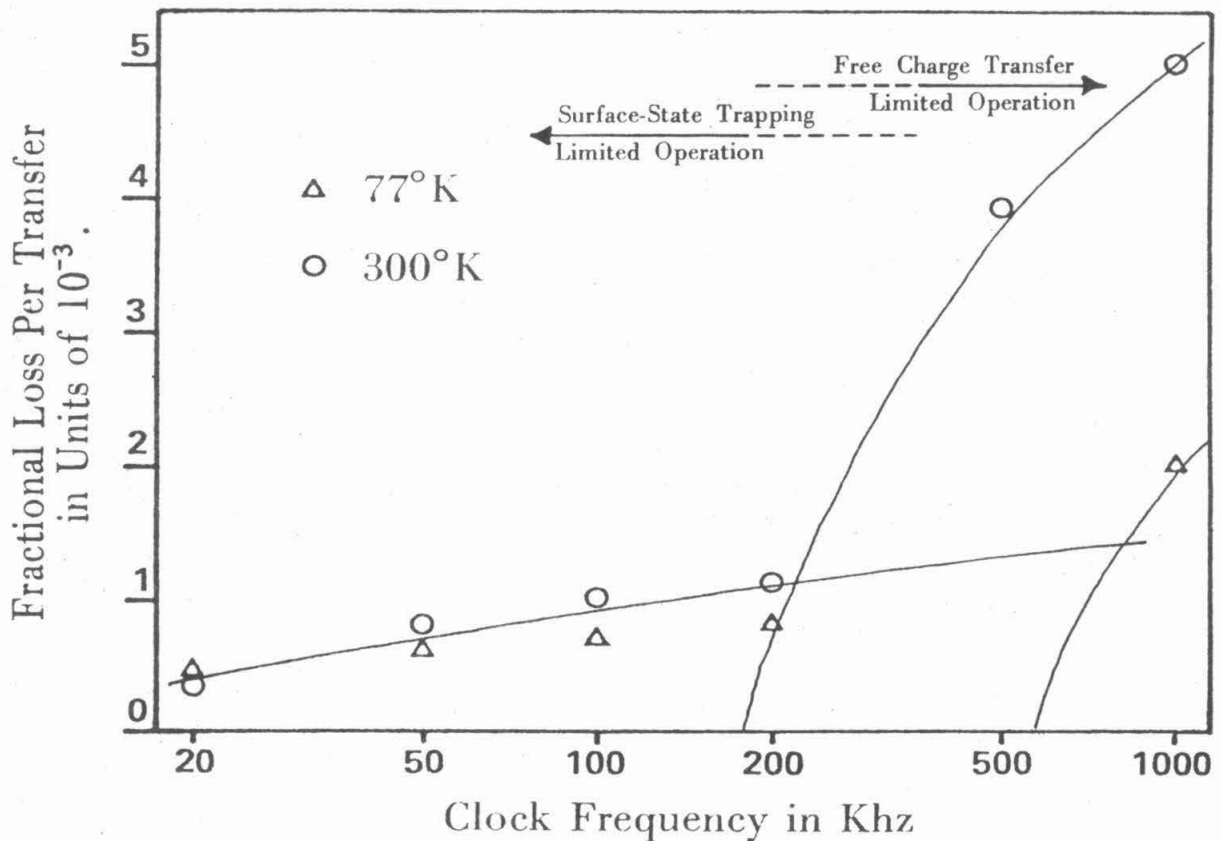


Figure 9. General Regions of Recirculating CCD Operation as Suggested by Mohsen, et. al. (4).

factor of 2.5 should be considered good agreement. The last stages of charge transport are controlled by mobility-limited drift in the fringing electric fields between the gates, and by diffusion. According to the Einstein relation, $D = \frac{kT}{q}\mu$, a drop in temperature by a factor of four and an increase in mobility by a factor of 4.5 increases the diffusion coefficient by only about 10%. The relative importance of fringing field drift and diffusion in transporting the last bit of charge is a

function of device geometry and process parameters- diffusion could dominate a device with very long gates, or one made on a heavily-doped substrate that would limit the penetration of the fringing field.

At low clock frequencies (below ~ 200 Khz) the recirculating CCD evaluated here shows little temperature dependence of the transfer inefficiency. The slight increase with frequency could be caused by various forms of interface state trapping, all of which, according to Mohsen, et al., (4) would tend to cause such an increase; or it could be merely a "tail" on the high-frequency operation.

G. CONCLUSION

A recirculating charge-coupled device has been devised and fabricated. Its performance in simulating degradation of a signal by a very long shift register is well fit by a simple model based on transfer inefficiency. Frequency and temperature dependence of the observed transfer inefficiency are consistent with basic models of CCD operation.

H. APPENDICES

EXPERIMENTAL OBSERVATION OF SIGNAL DEGRADATION IN RECIRCULATING CHARGE-COUPLED DEVICES

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ABSTRACT

A circular charge-coupled device structure has been devised. Entrance and exit gates allow a signal to be admitted, recirculated a given number of times, and then examined. In this way a small device permits simulation of very long shift registers (whose length depends on the number of recirculations) without passing the signal through input and output diffusions. Maximum length is limited by transfer efficiency effects and thermal generation, and is greater at low temperature. In a surface mode device clocked at 100 KHz, delays of 8000 transfers (4000 "bits") have been observed at 77°K. An oscilloscope motion picture demonstrating degradation of an actual circulating signal will be shown. Dependence of observed transfer efficiency on temperature and clock frequency will be discussed.

INTRODUCTION

The typical Charge-Coupled Device (CCD)[1] shift register produces an output signal which is a delayed function of the input signal after being degraded by (1) the CCD input device, (2) the CCD channel itself, and (3) the output device. Positive separation of these three effects can be difficult. A technique has been devised which permits separation of CCD channel effects from input/output effects. Using a CCD with a closed path channel, a signal can be admitted, recirculated a number of times (like automobiles on a racetrack), and then examined, by appropriate clocking of the control electrodes. The output is then studied as a function of the number of "laps" the signal made around the device, and the degradation caused by increasing the number of transfers examined. Figure 1 is a block diagram of the procedure.

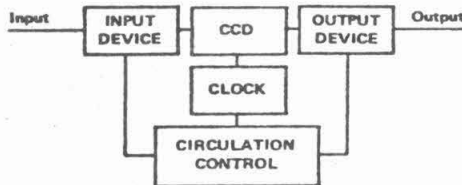


Fig. 1. Block Diagram of Setup.

This method of using a small device to simulate a very long shift register is somewhat like the feedback approach taken by Levine [2], except that this scheme avoids repeated passing of the signal through input and output diffusions. Levine's method of negative feedback provides a self-regulating circulating bias charge, which has some advantages in the measurement of charge transfer efficiency. In the recirculating CCD, the potential wells eventually fill with thermally-generated charge, as in a long linear device. Hence the recirculating CCD is a realistic simulation of an operating long shift register.

DEVICE AND OPERATION

The device was fabricated with two-phase aluminum-polysilicon overlapping gate technique [3] with a surface p-channel width of 10 μm (0.4 mil) and a length of 20 μm (0.8 mil) per stage, or 40 μm per bit. These dimensions were modified at the "corners" of the closed-path channel. Figure 2 is a map of the device without gates. Constructed as a long rectangle with 32 stages (16 bits) on each side, the device has a total storage capacity of 32 bits. Placing input and output structures at opposite ends means any odd multiple of 16 bits delay can be achieved with suitable clocking.

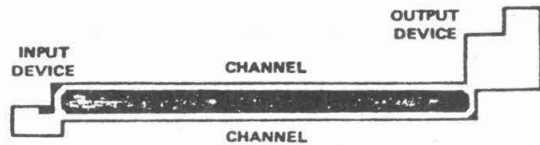


Fig. 2. Plan of Recirculating CCD.

Figure 3 is an enlargement of one corner showing the input scheme. The "corner" polysilicon storage gate is overlapped by two aluminum channel gates and a third aluminum input gate connecting it with the input diffusion. When the storage gate is "on," strobing the input gate admits charge into the channel from the diffusion.

A similar arrangement is used for the output. An output gate connects the channel storage polysilicon gate with a floating output diffusion. Turning this gate on "hard" diverts the flow of charge from the channel into the output diffusion where it is sensed by an on-chip source-follower transistor. Another transistor resets the diffusion between output bits.

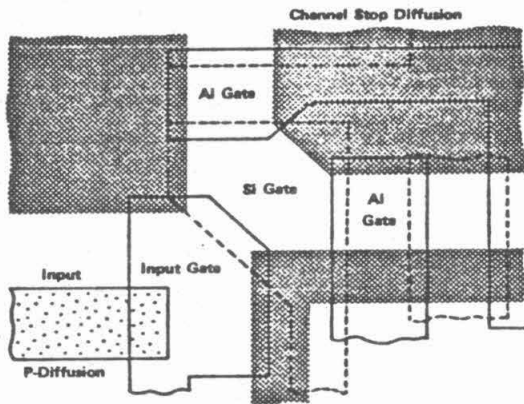


Fig. 3. Input Arrangement.

In operation, the shift register gates above the channel are clocked continuously. The output gate is first turned on for 32 bits to display the stored signal. Then the input gate is strobed for 32 bits to admit a new input signal. This is circulated as many "laps" as desired before being displayed. Each output cycle is immediately followed by an input to provide a frequently refreshed display.

EXPERIMENTAL RESULTS

The device has been operated at clock frequencies between 20Khz and 1 Mhz at both room temperature and 77°K, the latter by simply immersing it in liquid nitrogen. For an input of an alternating sequence of four "ones" and four "zeros," figure 4 shows the output obtained for several delays, clocking at 100 KHz. Initially, the signal introduced includes a "fat zero" bias charge of about 20% of a full well. Rapid degradation of the first data bit is caused by loading the signal into an essentially empty channel. From the oscilloscope display, a motion picture has been made of the device output by increasing the delay by 32 bits for each two frames. This movie provides an interesting qualitative view of the degradation of the circulating signal. Measurement of these photographs and calculation of the fractional loss per transfer yield the data plotted in figure 5. These measurements were made on the leading bit of the last packet of "ones" in each case, and the gradual thermal filling of all buckets was ignored.

SUMMARY

A recirculating charge-coupled device has been devised and fabricated. By simulating a very long shift register, it has been used to measure charge transfer efficiency at two temperatures and various clock frequencies. Comparison of this data with theoretical models has not yet been done.

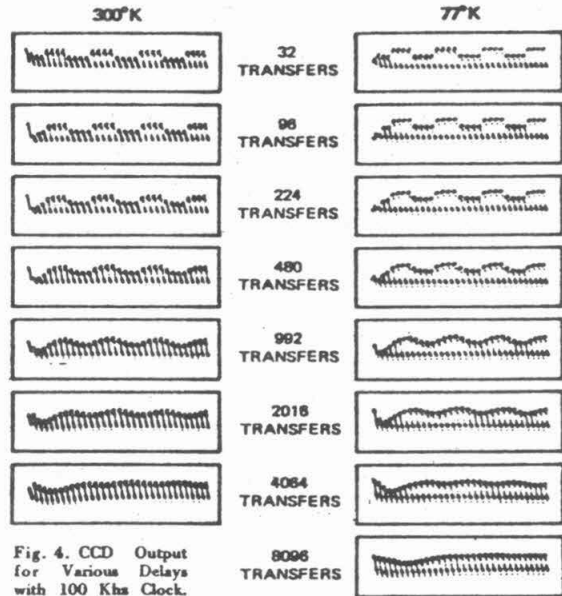


Fig. 4. CCD Output for Various Delays with 100 KHz Clock.

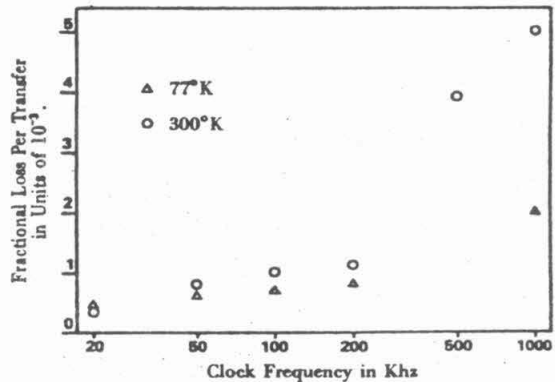


Fig. 5. Charge Transfer Efficiency as a Function of Clock Frequency and Temperature.

ACKNOWLEDGEMENT

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Appendix 2. Interactive Computer Program used for
Transfer Inefficiency Modeling of
Recirculating CCD.

```

    DIMENSION BUCKET(32), COPY(32), PLOT(64)
  1  CONTINUE
    WRITE (5,100)
100  FORMAT (13H FULL BUCKET?)
    READ (5,105) FULL
105  FORMAT (1F4.0)
    WRITE (5,110)
110  FORMAT (10H FAT ZERO?)
    READ (5,105) FAT
    DO 5 I=1,32
      BUCKET(I)=FAT
    5  CONTINUE
    DO 10 I=1,4
      DO 15 J=1,4
        K=8*I+J-4
        BUCKET(K)=FULL
    15  CONTINUE
    10  CONTINUE
    WRITE (5,115)
115  FORMAT (11H TRANSFERS?)
    READ (5,120) NTRAN
120  FORMAT (I5)
    WRITE (5,125)
125  FORMAT (17H GENERATION RATE?)
    READ (5,145) GEN
145  FORMAT (F6.0)
    WRITE (5,130)
130  FORMAT (15H LOSS/TRANSFER?)
    READ (5,145) EPSI
    DO 25 I=1,NTRAN
      DO 30 J=1,32
        COPY(J)=BUCKET(J)
    30  CONTINUE
    DO 35 J=2,32
      BUCKET(J)=EPSI*COPY(J-1)+(1.-EPSI)*COPY(J)+GEN*(1.-COPY(J))
    35  CONTINUE
    BUCKET(1)=EPSI*COPY(32)+(1.-EPSI)*COPY(1)+GEN*(1.-COPY(1))
    25  CONTINUE
    DO 45 I=1,64
      PLOT(I)=0.
    45  CONTINUE
    DO 50 I=1,32
      PLOT(2*I)=BUCKET(I)
    50  CONTINUE
    CALL TTYPLT (PLOT,64,0.,1.,20)
    WRITE (5,200)
200  FORMAT (6H MORE?)
    READ (5,210) IF
210  FORMAT (I1)
    IF (IF .EQ. 0) GO TO 1
    STOP
  END

```

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II. THE MERCURY SELENIDE ON N-SILICON SCHOTTKY BARRIER

A. OVERVIEW

In most cases, when a junction is made between a metal and a semiconducting material an electric potential barrier results. This barrier causes the magnitude of the electric current flowing across the junction to depend strongly on the sign of the voltage across the device- the basic property of a rectifier. These devices, called Schottky barriers, are of considerable scientific and technological interest.

The height of the potential barrier is determined jointly by the properties of the metal and the semiconductor; particularly the density of electronic states at the semiconductor surface, the electron affinity of the semiconductor, and the vacuum work function or electronegativity of the metal. For a given semiconductor, forming junctions with metals of different work functions provides a tool for studying the semiconductor surface state density. For this reason, the discovery of any metal more electronegative than those previously known suggests many experiments exploring the properties of semiconductors.

Technologically, the Schottky barrier can be used as

a solar cell for converting light into electrical energy. In this role the maximum open-circuit voltage- closely related to the power conversion efficiency- is limited by the barrier height. Hence highly electronegative metals, which form high barriers, are of much practical interest.

It was recently suggested that the compound mercury selenide (HgSe) is more electronegative than any other known metal (6). This work explores the Schottky barrier formed between this substance and chemically-cleaned n-type silicon.

B. BACKGROUND AND MOTIVATION

When a Schottky barrier is made by evaporating a metallic contact onto the surface of a semiconductor, the equilibrium position of the semiconductor Fermi level at the interface is determined by the vacuum work function or electronegativity of the metal and by the properties of the semiconductor. It has been recognized for many years that in this respect semiconductors fit into two broad classes (1,2)- "ionic" materials in which the Schottky barrier height is strongly dependent on the properties of the metal, and "covalent" materials where the barrier changes only slightly as different metals are used. This difference in behavior can be explained by considering the density of states in the semiconductor bandgap at the interface (3). If there are many of these states, the barrier height can be insensitive to the properties of the metal because only a slight shift of the Fermi level at the surface is needed to provide the charge required to accommodate various metal work functions. This is the behavior observed in covalent semiconductors. If the surface-state density is small, this charge can only be provided by the fixed charge of a depletion region, and considerable changes in band-bending can be required when changing from one metal to another. This is the

behavior observed in ionic semiconductors.

For any given semiconductor, varying the metal electronegativity and observing the behavior of the Schottky barrier height provide a tool for exploring the surface state density.* As the most electronegative elemental metal, gold (Au), until recently, was the limit on this test.

Strong motivation for seeking materials of higher electronegativity comes from the work of Turner and Rhoderick on n-type silicon. Figure 1, from their data (4), shows why. Schottky barrier height ϕ_B is plotted as a function of vacuum work function ϕ_M for various metals and two different surface preparations. (Recent measurements (5) have probably changed the best values of some of these work functions, but the idea remains sound.) For barriers made on silicon cleaved in vacuum, the barrier height is nearly independent of the metal - the "covalent" behavior discussed above. For silicon surfaces chemically prepared the dependence is considerably increased - reminiscent of "ionic" materials. This increase results from the reduction in surface-state density caused by

*The electronegativity of a metal is monotonically related to its vacuum work function. The two differ by a nearly-constant term associated with "a surface dipole layer caused by a distortion of the electron cloud at the surface" (1).

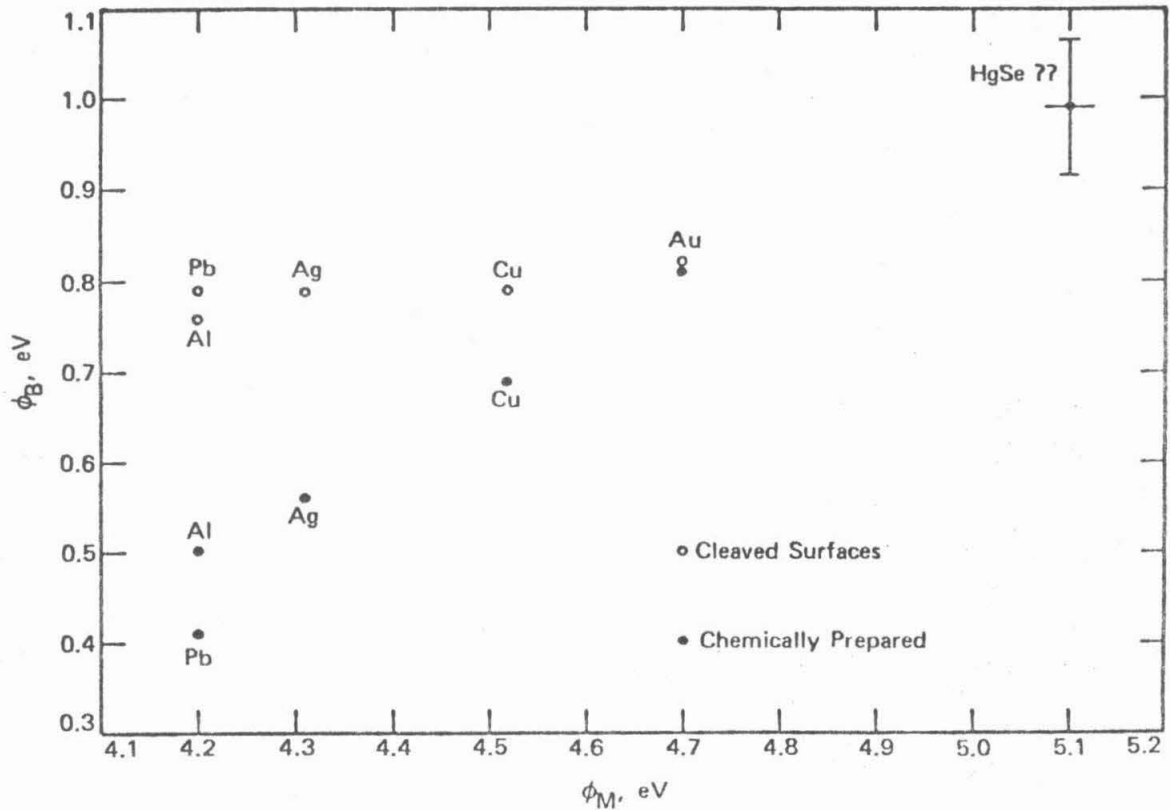


Figure 1. Barrier Height ϕ_B vs. Work Function ϕ_M for Different Metals and Surface Treatments

"passivation" of the surface by the thin silicon dioxide (SiO_2) layer produced by the cleaning process.

The two lines cross in the vicinity of gold. This suggests that a device made with a very highly electro-negative ($> \text{Au}$) material on n-type silicon might exhibit a higher barrier than any previously observed. The recent work of Best, et al. (6), shows that Mercury Selenide (HgSe) is a suitable material.

From barrier height measurements on ionic materials, Best et al. estimated that the effective electronegativity of HgSe is approximately 2.9 on the Pauling (7) scale. On this scale, gold is 2.4 and silver is 1.9. Hence the difference between HgSe and Au is the same as that between Au and Ag. If the difference in barrier heights were the same, the HgSe barrier on n-type silicon could be as high as 0.98 volt, as suggested by the uncertainty bar in figure 1. This work investigated that possibility.

Such a large barrier on n-type silicon would be of considerable technological interest. In a Schottky barrier solar cell, the maximum open-circuit voltage is limited by the barrier height. While this voltage is not likely to approach the maximum voltage of a diffused-junction solar cell (which is limited by the bandgap), the relative ease of fabrication of the Schottky barrier device makes it an attractive and competitive approach. Any increase in the maximum observed barrier height can only improve the chances of the Schottky barrier solar cell becoming a practical, useful device.

C. SAMPLE PREPARATION

Silicon wafers, $\langle 111 \rangle$, with epitaxial layers were used. The 0.015 Ω -cm Sb-doped substrate made an ohmic contact relatively simple. Schottky barriers were made on the 2.2-2.6 μm thick, phosphorous-doped epi layer. The epi doping concentration was about $3 \times 10^{16}/\text{cm}^3$. As determined by capacitance-voltage measurements, it varied by less than a factor of two from wafer to wafer. The wafers were cut into six parts so that comparisons could be made between devices made on pieces of as near identical composition as possible.

The silicon wafers were supplied by Hewlett-Packard with thick ($\sim 0.4 \mu\text{m}$) oxide layers. When a specimen was to be used, this oxide was stripped with hydrofluoric acid and the wafer rinsed repeatedly with high-purity water and spun dry. The metal deposition to make the Schottky barrier was performed immediately. The specimen was never in room air longer than five minutes- three minutes was typical.

Mercury Selenide was deposited by evaporating selenium in a mercury-vapor atmosphere with the apparatus and method developed by Best, et al. (6). The modified version reported by Scranton, Best, and McCaldin was used (8). The Se evaporation was shuttered, and deposition of

the HgSe took about ten minutes. The vacuum system used was dedicated to this process only.

For standardization, Au and Ag were evaporated onto other silicon specimens in other vacuum systems. When possible, the same piece of screen (metal with an array of $1.8 \times 10^{-4} \text{ cm}^2$ holes for defining dots) was used- in all cases parts of the same "lot" of screen were used.

Ohmic contacts were made to the back sides of the substrates by rubbing cold indium onto them and annealing quickly with a soldering iron. This annealing caused no noticeable change in device characteristics. A good ohmic contact could be made by cold rubbing alone, but the risk of physical damage to the devices was higher, and this was done only to confirm that the heating did no damage.

D. MEASUREMENTS

Schottky barrier heights for Ag, Au, and HgSe on the n-type silicon material were measured using photoresponse, current-voltage, and capacitance-voltage techniques (1). In general, measurements of Au and Ag gave results consistent with previous work (4) and require no further discussion. The HgSe information is new and will be discussed for each case.

1. Photoresponse

Figure 2 is a typical plot of the square root of the photoresponse R in arbitrary units as a function of photon energy, made using a Gaertner monochromator with a resolution of $0.01 \mu\text{m}$. Figure 3 is an expansion of the steep portion of figure 2 (for a different device), made using a SPEX monochromator with a resolution of $0.002 \mu\text{m}$.

For figure 2, a straight line tangent to the straight portion of the curve intersects the energy axis at about 0.96 volts. The expanded figure 3 is consistent with this but suggests a possible error of around 0.03 volts.

The theoretical relationship employed in this measurement, namely

$$R \sim (h\nu - h\nu_0)^2$$

where $h\nu_0$ is the barrier height, is strictly valid only

Figure 2 LEFT. Square Root of Photoresponse in Arbitrary Units for HgSe on n-Si Schottky Barrier.

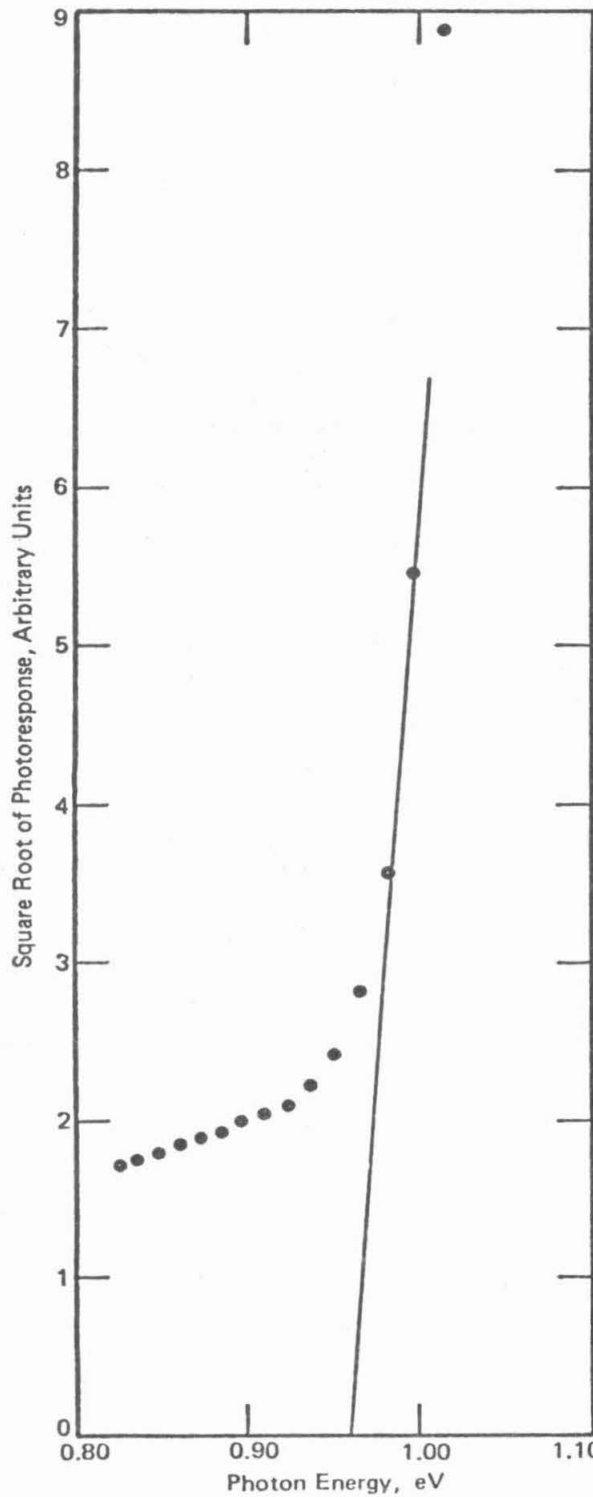
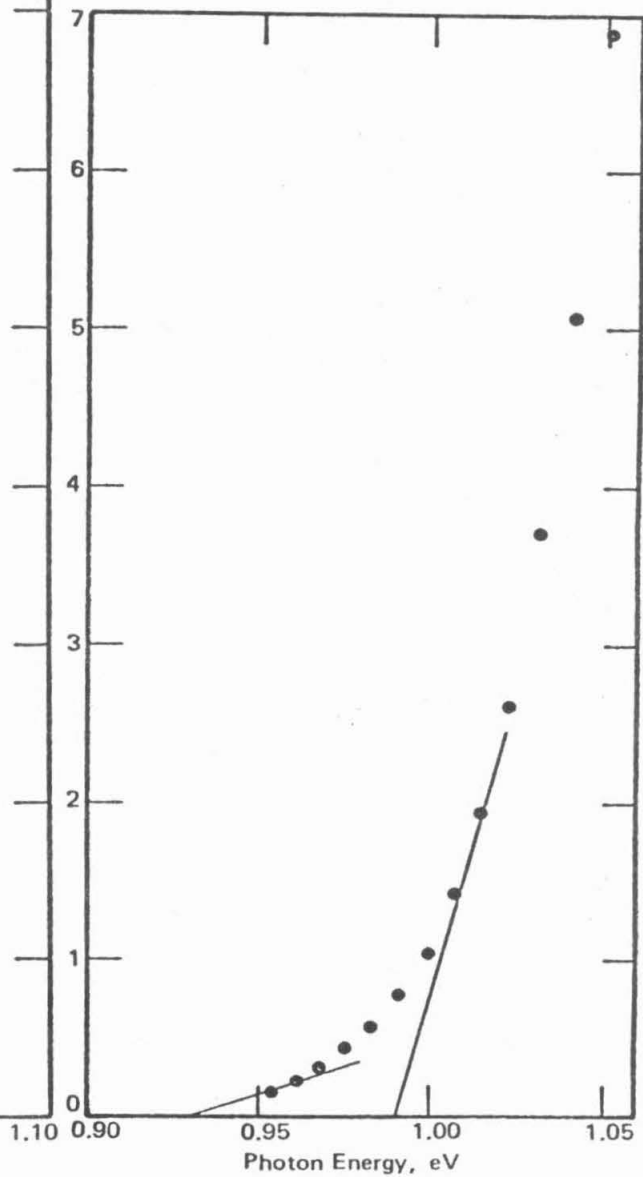


Figure 3 BELOW. Expansion of steep portion of Figure 2. Square Root of Photoresponse in Arbitrary units for HgSe on n-Si Schottky Barrier.



for photon energies more than about $3kT$ greater than the barrier height. In this case, the barrier is only about $6kT$ below the bandgap and it is not possible to meet this criterion rigorously. The straight-line portion of the barrier photoresponse could be concealed in the bandgap response. The worst consequence of this would be a barrier higher than that observed. Hence 0.96 ± 0.03 volts is a lower limit on the barrier as determined by this method.

2. Current-Voltage

Current-Voltage measurements for HgSe varied over a small range and appeared to depend on the exact conditions of deposition, as reflected in the visual appearance of the material. In general, HgSe dots which appeared slightly pinkish (as distinct from silvery) exhibited the highest barriers. The I-V characteristic for such a device is plotted in figure 4, along with plots for Ag and Au devices made by evaporation through the same screen onto pieces of the same wafer. The barrier for HgSe is ~ 0.1 volt higher than that for gold, or approximately 0.90 volt. The mean of a number of such measurements of high barriers on different samples (all "pinkish") is also 0.9 volts. The color changes and barrier shifts are probably due to slight variations in stoichiometry; unfortunately no method was available to study this.

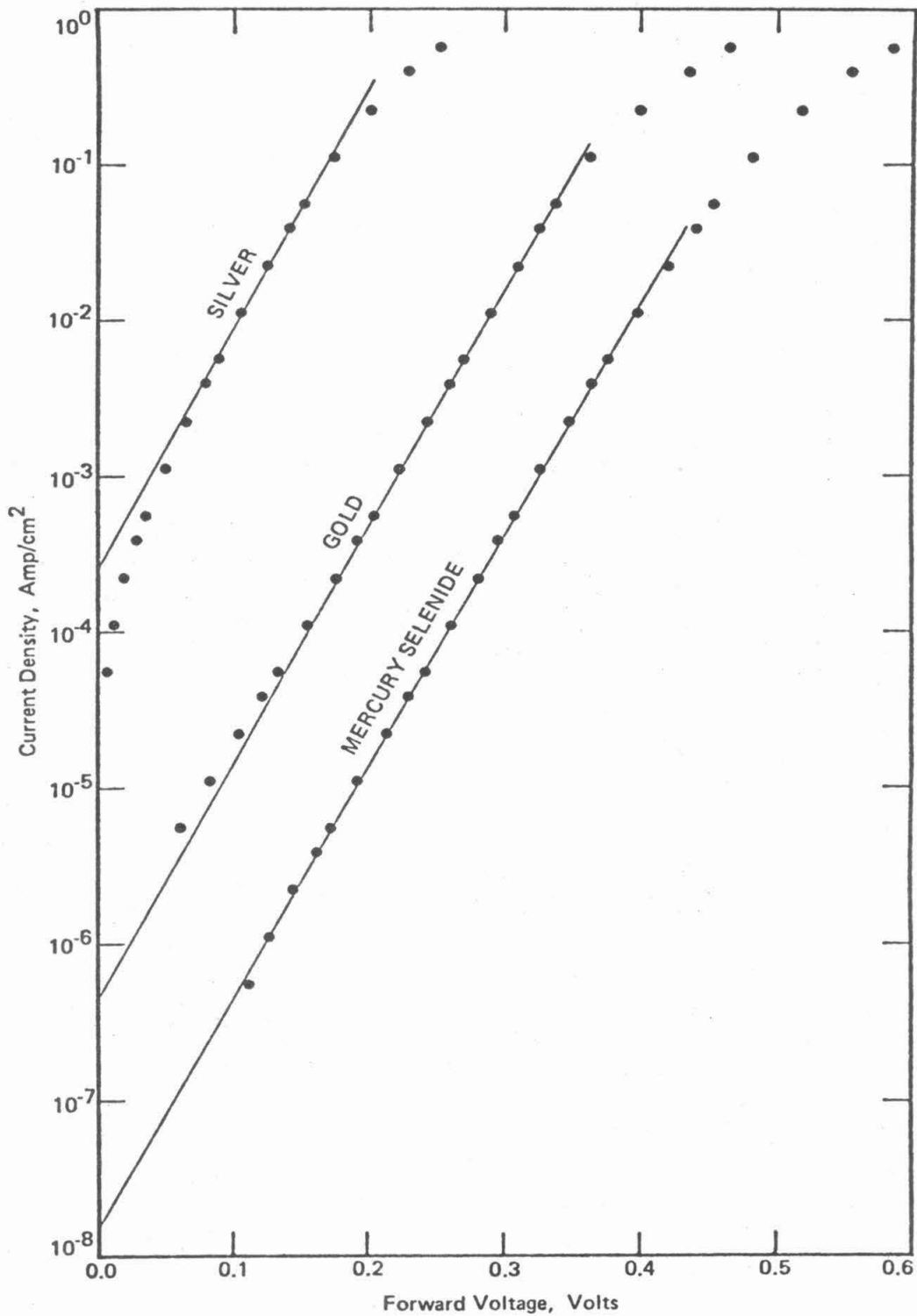


Figure 4. I-V Characteristics for Ag, Au, and HgSe on n-Si Schottky Barriers. All devices evaporated through same screen onto pieces of same silicon wafer.

3. Capacitance-Voltage

Capacitance-Voltage measurements for Au and Ag barriers were consistent with accepted values, but measurements for HgSe did not yield useful information. Measurements varied over a wide range from below gold (about 0.75 volt) almost to the silicon bandgap (about 1.1 volt).

E. RESULTS

A summary of the measurements is presented in table 1.

Metal	Ag	Au	HgSe
C-V	.65	.78	-
I-V	.62	.80	.90
Photo	.61	.79	.96

TABLE 1. Summary of Results. HgSe errors are estimated as ± 0.03 volt.

Use of the barrier height for HgSe to estimate the surface state density of the chemically cleaned silicon requires knowledge of the vacuum work function for HgSe. This has not been measured. Figure 5 is a plot of work function, as determined by Thanailakis (5), vs. Pauling electronegativity for various metals. Assuming a straight-

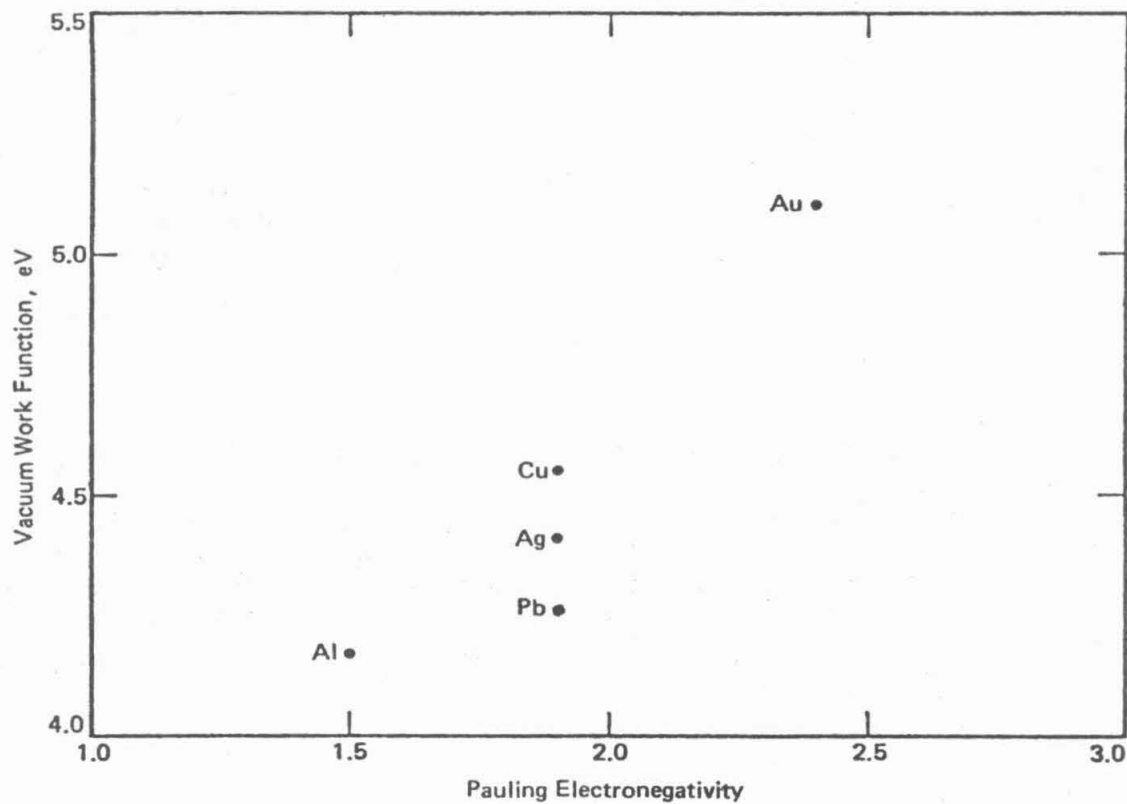


Figure 5. Vacuum Work Function (according to (5)) vs. Pauling Electronegativity for Various Metals.

line relationship, the vacuum work function for HgSe can be estimated as 5.5 volts.

Cowley and Sze (9) showed that an approximate form for the barrier height is

$$\phi_B = \gamma(\phi_M - A) + (1 - \gamma)(E_g - \phi_0)$$

where A is the electron affinity of the semiconductor, ϕ_0 is the "neutral level" for surface states with respect to the top of the valence band, E_g is the energy gap, and

$$\gamma = \frac{\kappa \epsilon_0}{\kappa \epsilon_0 + q \delta N_S}$$

where κ is the dielectric constant of the interfacial layer, δ is its thickness, and N_S is the density of surface states.

As the metal is changed from gold to HgSe, we have a change in barrier height $\Delta\phi_B = 0.14$ volt, and a change in work function $\Delta\phi_M = 0.4$ volt, so that $\gamma = 0.35$. Hence

$$N_S \sim \frac{2 \kappa \epsilon_0}{q \delta}$$

The thickness of the oxide layer resulting from chemical cleaning was measured by thin-film ellipsometry for some of the silicon samples used in the barrier measurements. An average thickness of 7×10^{-8} cm was measured. If we assume the dielectric constant, 4, of the bulk oxide is applicable to the interfacial layer, we calculate that $N_S \sim 6 \times 10^{12}/\text{cm}^2\text{-eV}$ in the portion of the bandgap "scanned" by the Fermi level when gold is replaced by HgSe. The Fermi level is positioned ϕ_B below the conduction band edge. The room temperature bandgap E_g of silicon is 1.12 volts. Hence for gold barriers the Fermi level is 0.32 volt above the valence band edge; for HgSe the number is about 0.2 volt. This is a region of the bandgap where the surface state density is changing rapidly with energy. The average density in the region for ther-

mally grown oxides is about $4 \times 10^{11}/\text{cm}^2\text{-eV}$ (10), or more than an order of magnitude lower than that indicated by the present work. This is not unusual, in that commercial low- N_s oxides for MOS transistor work are normally grown at high temperatures. The variations in barrier height observed in the I-V measurements could partially result from varying N_s caused by slight variations in surface preparation. This effect is believed to be smaller than that caused by stoichiometric fluctuations because the measurements for Au and Ag barriers showed much less scatter.

F. CONCLUSION

Properties of the Mercury Selenide on n-type silicon Schottky barrier have been studied. Photoresponse measurements indicate a barrier height of 0.96 ± 0.03 volt, and current-voltage measurements indicate a barrier height of 0.90 volt. These are the highest Schottky barriers to be reported on n-type silicon. The surface-state density estimated from these measurements is consistent with that determined by other methods.

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