WIRELESS PARYLENE-BASED RETINAL IMPLANT

Thesis by

Jay Han-Chieh Chang

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ABSTRACT

Wireless Parylene-Based Retinal Implant

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Doctor of Philosophy in Electrical Engineering
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The degeneration of the outer retina usually causes blindness by affecting the photoreceptor cells. However, the ganglion cells, which consist of optic nerves, on the middle and inner retina layers are often intact. The retinal implant, which can partially restore vision by electrical stimulation, soon becomes a focus for research. Although many groups worldwide have spent a lot of effort on building devices for retinal implant, current state-of-the-art technologies still lack a reliable packaging scheme for devices with desirable high-density multi-channel features. Wireless flexible retinal implants have always been the ultimate goal for retinal prosthesis. In this dissertation, the reliable packaging scheme for a wireless flexible parylene-based retinal implants has been well developed. It can not only provide stable electrical and mechanical connections to the high-density multi-channel (1000+ channels on 5 mm × 5 mm chip area) IC chips, but also survive for more than 10 years in the human body with corrosive fluids.

The device is based on a parylene-metal-parylene sandwich structure. In which, the adhesion between the parylene layers and the metals embedded in the parylene layers have been studied. Integration technology for high-density multi-channel IC chips has also been addressed and tested with dummy and real 268-channel and 1024-channel retinal IC chips. In addition, different protection

schemes have been tried in application to IC chips and discrete components to gain the longest lifetime. The effectiveness has been confirmed by the accelerated and active lifetime soaking test in saline solution. Surgical mockups have also been designed and successfully implanted inside dog's and pig's eyes. Additionally, the electrodes used to stimulate the ganglion cells have been modified to lower the interface impedance and shaped to better fit the retina. Finally, all the developed technologies have been applied on the final device with a dual-metal-layer structure.

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CLOSSARY

AMD – age-related macular degeneration

ASCII – American Standard Code for Information Interchange

ASIC – Application Specific Integrated Circuit

ASTM – American Society for Testing and Materials

BGA – ball grid array

CL-I^2 – Chip-level Integrated Interconnect

CMOS – complementary metal–oxide–semiconductor

CT – computed tomography

CVD – chemical vapor deposition

DIP – dual in-line package

DRIE – deep reactive ion etching

EDM – electric discharge machining

EDP – ethylene diamine pyrocatechol

FDA – Food and Drug Administration

HARM – high-aspect-ratio micromachining

HF – hydrofluoric acid

HNA – hydrofluoric acid, nitric acid and acetic acid

IC – integrated circuit

ID – identification

ISO – International Organization for Standardization

KOH – potassium hydroxide

LIGA – Lithographie, Galvanoformung, Abformung (Lithography, Electroplating, and

Molding)

LOR – lift-off resist

MEMS – micro-electro-mechanical systems

MFI – MicroFlex interconnect

MRI – magnetic resonance imaging

MTTF – mean time to failure

PCB – printed circuit board

PDMS – polydimethylsiloxane

PR – photoresist

PSG – phosphosilicate glass

RF – radio frequency

RFID – radio frequency identification

RIE – reactive ion etching

RLC – resistor-inductor-capacitor

RP – retinitis pigmentosa

SAP – silicone adhesion promoter

SEM – scanning electron microscope

SNR – signal-to-noise ratio

SOI – silicon on insulator

TMAH – tetramethylammonium hydroxide

TTL – transistor-transistor logic

USP – United States Pharmacopeia

WHO – World Health Organization

1 INTRODUCTION

1.1 Retinal Prosthesis

In normal human vision, as shown in Figure 1.1, the light enters the eye through the cornea, the pupil, and is focused by the transparent crystalline lens. The light then goes through the vitreous body which is filled with vitreous humor, through the layers of the inner retina, and it is ultimately focused onto the photoreceptors of the outer retina. Along the pathway, the delicate retina performs significant visual processing works. According to the World Health Organization (WHO), the two most common leading causes of blindness induced by degenerative retinal diseases are the age-related macular degeneration (AMD) and retinitis pigmentosa (RP). The defects will damage the outer photoreceptors and cause the loss of the cone and rod receptors in the eye. Blindness due to such outer retinal diseases have affected several million people in the world. In fact, it has been estimated by The Eye Diseases Prevalence Research Group and the National Eye Institute that AMD alone will affect more than three million people in the United States by the year 2020 [1]. In addition, the prevalence of RP has been estimated to be approximately 1 in 4000 [2]. Recent evidence has shown that gene, drug, and nutrition therapies could be some possibilities for the treatment of such diseases [3-4]. However, such treatments, in reality, are still very far away from being used in clinical practice, and have a number of ethical and political barriers to their implementation. Therefore, blindness still cannot be treated in the end.

In 1994, Dr. Humayun et al. reported the results to electrically stimulate vertebrate retinas [5] as another possible treatment for these retinal diseases. The main idea is to bypass the damaged photoreceptors in the normal visual route. In this study, damaged bullfrog eyecups and rabbit eyes, were stimulated with platinum electrodes and the results showed that surface electrical stimulation of the inner retina in normal eyes and in eyes with outer retinal degeneration can induce a localized

retinal response. The ganglion cell layers which consist of optical nerves can be electrically stimulated to construct localized vision signals in patients [6-9]. This is so called “Retinal Prosthesis”, a possible treatment for patients with devastating blindness due to outer retinal disease.

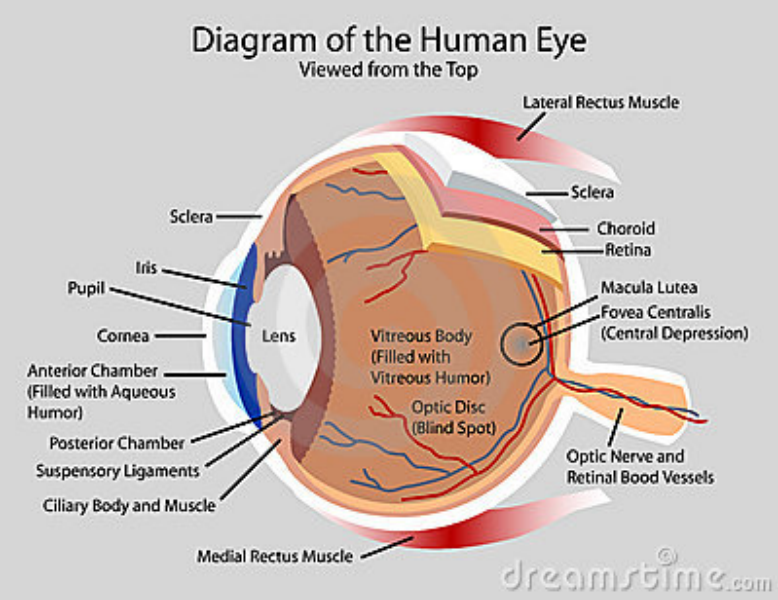


Figure 1.1. Diagram of the human eyeball structure.
(Image courtesy from www.glogster.com)

There are now a large variety of approaches to artificial vision, each with their own advantages and disadvantages. Among them, the main stimulation schemes are epiretinal and subretinal approaches, which differ by the location of the implanted devices and stimulation sites. For the epiretinal approach, as shown in Figure 1.2, an electrode array is placed directly on the retina from its anterior aspect. For the subretinal approach, an electrode or photodiode array is placed within the layers of the retina [10]. The state-of-the-art epiretinal prosthesis has been successfully demonstrated as a prototype of 60-electrode device, developed by Second Sight Medical Products, Inc. in patients [11]. Although still not enabling such activities of daily living as newspaper reading and facial recognition, blind patients can differentiate between a plate, a cup, and a knife, in a high-contrast

environment free from background distracters, which is already a huge achievement of engineering and medicine. Furthermore, subjects have been shown to be able to determine direction of movement of parallel white bars on a black background, as well as locate white squares within a quadrant of otherwise black space [12]. Also, patients have demonstrated their ability to read large letters simply by scanning the camera mounted on their head back and forth over the image displayed in front of them.

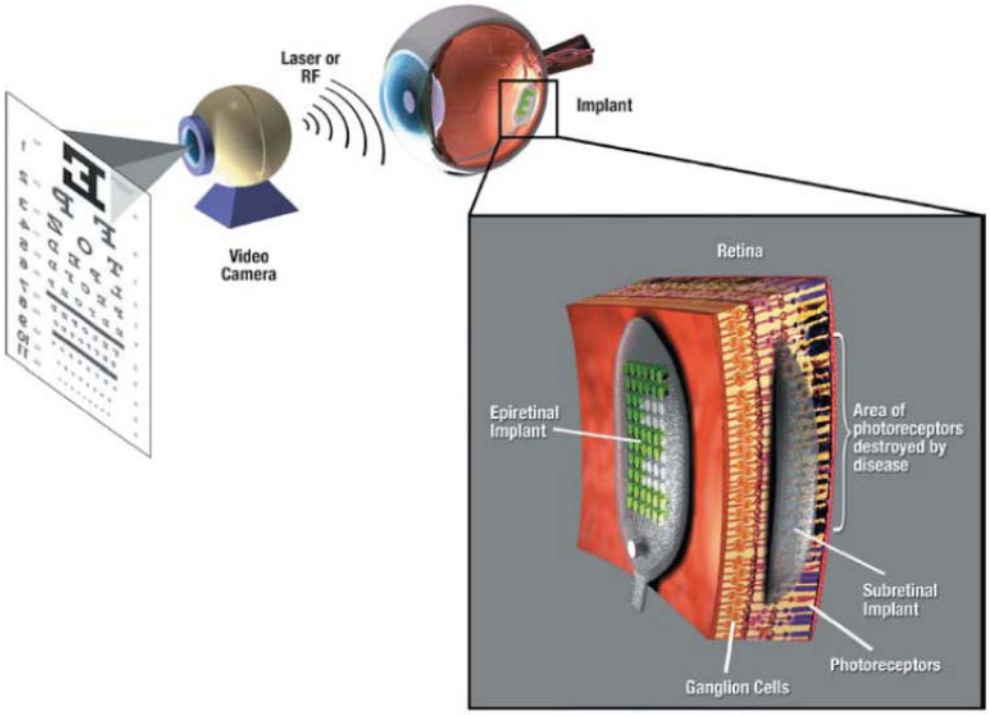


Figure 1.2. System overview and comparison of locations of epiretinal and subretinal implants [13].

The basic components of the retinal prosthesis system are almost the same, as shown in Figure 1.3: an external camera is mounted on a glass to take videos and pictures to general the raw signals. The signals will be then wirelessly sent into the eye and further analyzed by internal circuitry to generate the stimulation signals. The stimulation signals will then be sent to electrodes to stimulate the retina ganglion cells to partially restore some useful vision.

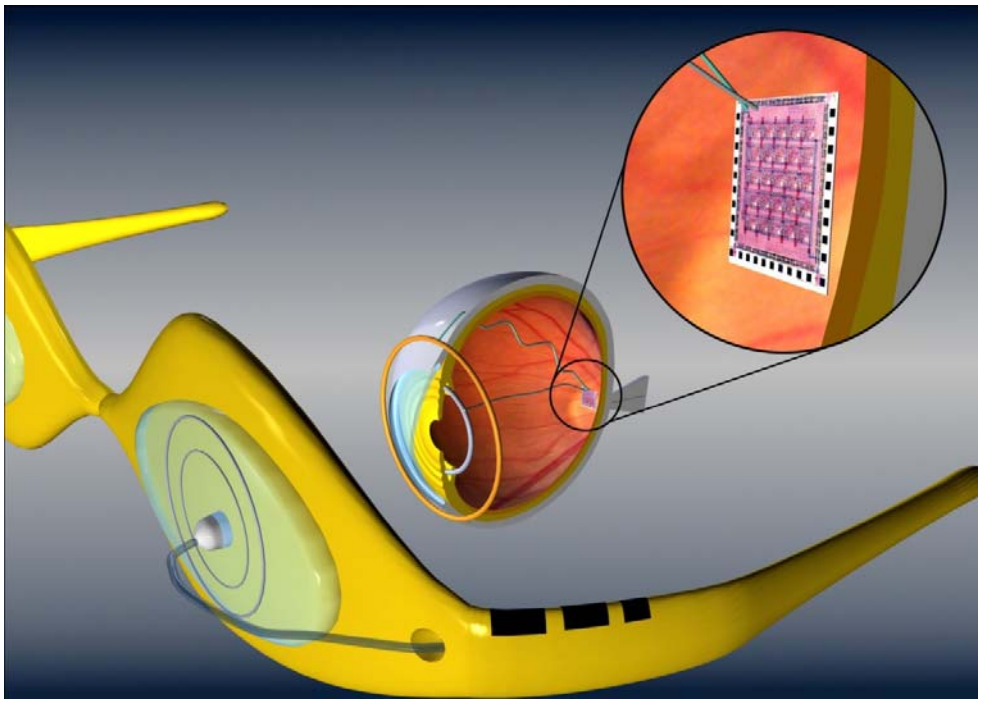


Figure 1.3. Basic components for the retinal implant system.
(Image courtesy from www.thinfilmsblog.com)

1.2 MEMS Technology

Micro-electro-mechanical system (MEMS), the acronym which originated in the United States, is also referred to as Microsystems Technology (MST) in Europe and Micromachines in Japan. MEMS is a fabrication technology applied to build small integrated devices and systems that consist of both mechanical and electrical components [14-15]. Because of its root in the IC industry, MEMS devices are fabricated using integrated circuit (IC) batch processing techniques and typically can range from 0.1 to 100 micrometer in sizes. Usually, these devices are able to detect, control and actuate on the micro scale, and response on the macro scale. Fabrication processes such as bulk and surface micromachining can selectively remove parts of the substrate, such as silicon, or add some additional structural layers to form the mechanical and electromechanical components and devices. While

integrated circuits (IC) are designed and fabricated to take advantages of the electrical properties of the silicon, MEMS technology exploits both its electrical and mechanical properties, thus resulting in broader application. MEMS is an integrated technology in micro-scale. It can consist of many microstructures, such as sensors, actuators, and electronics, all of them are integrated onto single silicon substrate. Among them, sensors can first detect the changes in the system's environment by measuring the mechanical, thermal, magnetic, chemical or electromagnetic data and phenomena. Electronics can then process this information. After that, the actuators can react and create some form of changes to the environment. In addition, MEMS devices are usually very small, and their components are usually in micro scale. Levers, gears, pistons, and motors have all been fabricated by MEMS technology. Figure 1.4 shows a potential complexity of MEMS system with the addition of independently-structured layers.

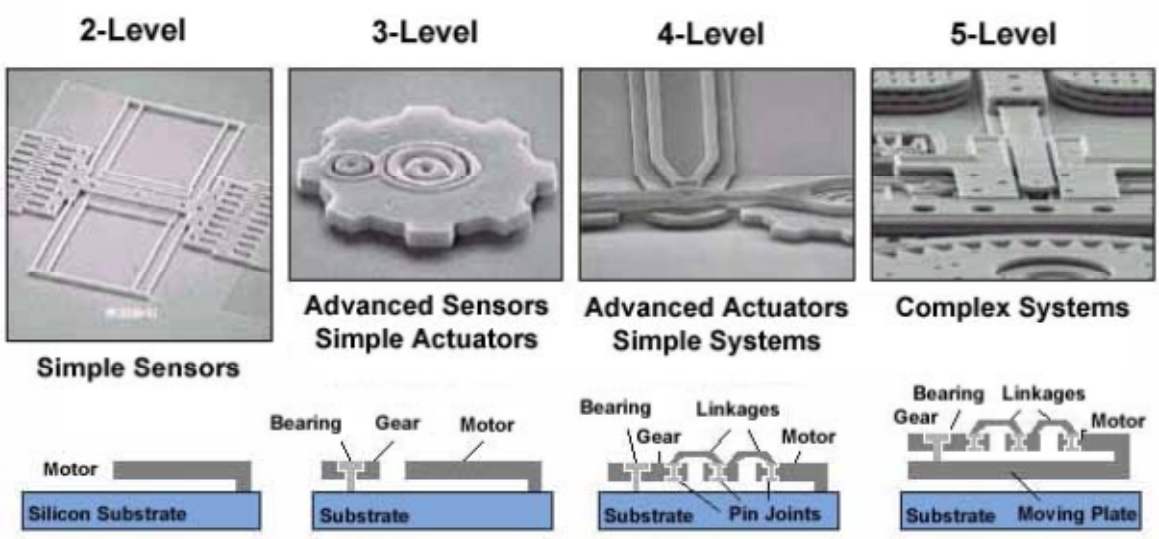


Figure 1.4. Complexity of MEMS device by structure layers [15].

MEMS has many diverse advantages, in micro-scale, as a fabrication technology. Many previously unrelated fields have been connected together by the interdisciplinary nature of MEMS technology. Besides, the batch fabrication techniques of MEMS also enable the manufactured

devices to be more stable and reliable. In addition, MEMS provides the foundation for the manufacture technology of products that cannot be replaced by other methods. All these factors make MEMS potentially a more popular and broader technology than integrated circuit (IC) microchips technology. However, there are still many challenges and technological difficulties associated with the miniaturization that need to be studied and overcome before MEMS technology can really realize its overwhelming potential around the world.

When it comes to the history of MEMS, from a very early vision in the early 1950's, MEMS has gradually made its way out of research laboratories and into everyday products. In the mid-1990's, MEMS components began to appear in numerous commercial products and applications including accelerometers used to control airbag in vehicles, pressure sensors for medical applications, and inkjet printer heads. Today, MEMS devices are also found in projection displays and used for micropositioners in data storage systems. However, the most important potential for MEMS devices lies in the new applications on the biomedical and process control areas.

The following lists the major history of MEMS which is useful to show its diversity, challenges, and application [16]:

1947 Realization of transistors.

1958 Silicon strain gauges commercially available.

1959 "There's Plenty of Room at the Bottom" – Richard Feynman gives a milestone presentation at California Institute of Technology.

1961 First silicon pressure sensor demonstrated.

1967 Invention of surface micromachining. Westinghouse creates the Resonant Gate Field Effect Transistor, (RGT). Description of use of sacrificial material to free micromechanical devices from the silicon substrate.

1970 First silicon accelerometer demonstrated.

1979 First micromachined inkjet nozzle demonstrated.

1982 Disposable blood pressure transducer demonstrated.

1982 "Silicon as a Mechanical Material" [17]. Instrumental paper to entice the scientific community – reference for material properties and etching data for silicon.

1982 LIGA Process.

1988 First MEMS conference held.

1992 MCNC starts the Multi-User MEMS Process (MUMPS) sponsored by Defense Advanced Research Projects Agency (DARPA).

1992 First micromachined hinge demonstrated.

1993 First surface micromachined accelerometer sold (Analog Devices, ADXL50).

1994 Deep Reactive Ion Etching is patented.

1995 BioMEMS rapidly develops.

2000 MEMS optical-networking components become big business.

MEMS can be further divided into three different classifications; bulk micromachining, surface micromachining, and high-aspect-ratio micromachining (HARM), which includes technology such as LIGA (a German acronym from Lithographie, Galvanoformung, Abformung translated as lithography, electroforming, and molding). Traditional macro-scale fabrication techniques are beneficial for building three dimensional (3D) shapes and devices, but they might be limited on applications for structures with smaller size because the nature of the low complexity. However, MEMS fabrication technology uses IC batch processing, which applies photolithography and other associated dry and wet etching processes, to perform the addition or subtraction of two dimensional (2D) layers on a substrate. Therefore, the 3D structure of MEMS devices can be fabricated by the patterning and interaction of the 2D layers. Additional layers can be added by thin-film deposition or other bonding techniques.

1.2.1 Photolithography

Photolithography is the technique used to transfer copies of a master pattern onto the other substrate, such as silicon wafers. This step provides pattern resolution high enough to achieve miniaturization. The photo-definable material, photoresist, is very light sensitive and can be selectively removed by shining ultraviolet (UV) light on a specific area. Figure 1.5 shows the comparison of the fabrication process between positive and negative photoresist. A thin layer of photoresist is first spin coated on the oxide layer. Then a photomask, consisting of a transparent glass plate coated with an opaque chromium (Cr) pattern, is then placed in contact with the photoresist coated surface. The wafer is then exposed by the UV radiation in order to transfer the pattern on the mask to the photoresist, which is then developed in the developer solution. The UV radiation induces the chemical reaction on the exposed areas of the photoresist. After the UV radiation step, the positive photoresist is enhanced by UV radiation while the negative photoresist is weakened. In developing process, the developer removes either the exposed areas (positive photoresist) or the unexposed areas (negative photoresist) of the photoresist. The pattern of photoresist-coated (positive photoresist) or bare (negative photoresist) oxides is then left on the wafer surface. The resulting photoresist pattern is either the positive or negative image of the original master pattern of the photomask. The chemical, such as hydrochloric acid, is applied to remove the uncovered oxide from the exposed areas of the photoresist. After that, hot sulphuric acid is used to remove the remaining photoresist to complete the whole process. This chemical only removes the photoresist but not the oxide layer on the silicon, resulting in a oxide pattern left on the silicon surface. The final left oxide is the copy of the master photomask pattern and is used as the mask in the subsequent processes.

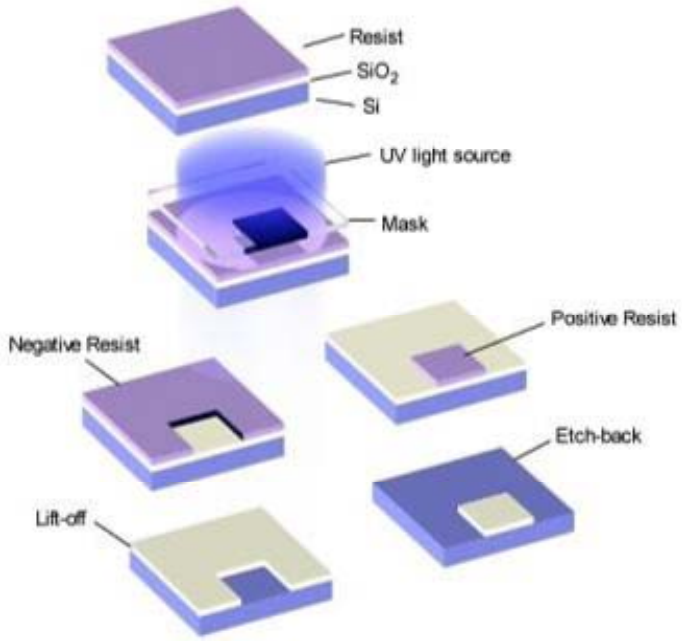


Figure 1.5. Comparison of the fabrication process between positive and negative photoresist. (Image courtesy of NCSU soft lithography from Wiki)

1.2.2 Bulk Micromachining

Bulk micromachining is the fabrication process applied to remove part of the bulk substrate. It is a subtractive process used to create large pits, grooves and channels on the original substrate, as shown in Figure 1.6. Bulk micromachining can be performed by using wet etching with corrosive etchants or a dry etching method such as reactive ion etching (RIE) or deep reactive ion etching (DRIE). Materials such as silicon and quartz are commonly used for wet etching, while silicon, metals, plastics and ceramics are usually used for dry etching.

1.2.2.1 Wet Etching

Wet etching is usually applied in order to remove the materials on substrates by immersing in a chemical etchant liquid bath. These chemical etchants can be isotropic or anisotropic. Among them, isotropic etchants etch the materials at the same rate in all directions, and consequently etch materials

under the etching masks at the same rate as they etch through the material. This is the so called "undercutting". The most common solution of the isotropic etchant for silicon is HNA, which consists of a mixture of hydrofluoric acid (HF), nitric acid (HNO_3) and acetic acid (CH_3COOH). Isotropic etchants are limited by the geometry of the structure to be etched. Etch rates can slow down and in some cases they can stop by introduction of the diffusion limiting factors. However, this effect can be minimized by agitation of the chemical etchant liquid bath, resulting in structures with near perfectly rounded surfaces [18]. Anisotropic etchants, on the other hand, etch faster in a specific crystal direction. Potassium hydroxide (KOH) is the most common anisotropic etchant used in process because it is comparatively safer. Besides, ethylene diamine pyrocatechol (EDP), tetra-methyl-ammonium-hydroxide (TMAH), and hydrazine water are the other common anisotropic etchants used in MEMS process. Structures formed in the substrate by wet etching are dependent on the crystal orientation of the silicon wafer substrate. Such anisotropic etchants etch faster in the crystal direction perpendicular to the (110) plane. However, they etch slower in the direction perpendicular to the (100) plane. The direction perpendicular to the (111) plane is also etched very slowly. Silicon wafers, originally cut from a large ingot of silicon grown from single seed silicon, are cut according to the crystallographic plane. They can be supplied in terms of the orientation of the surface plane. Dopant levels introduced in the substrate can affect the etching rate of KOH. They can effectively stop the etching if the dopant levels are high enough. Boron is one of the typical dopants which is commonly used in IC fabrication process. It is introduced into the silicon by the diffusion process. This can be used to selectively etch specific regions in the silicon, leaving doped areas unaffected during wet etching process. By combining the anisotropic etching with etching stops, various silicon microstructures can be bulk micromachined.

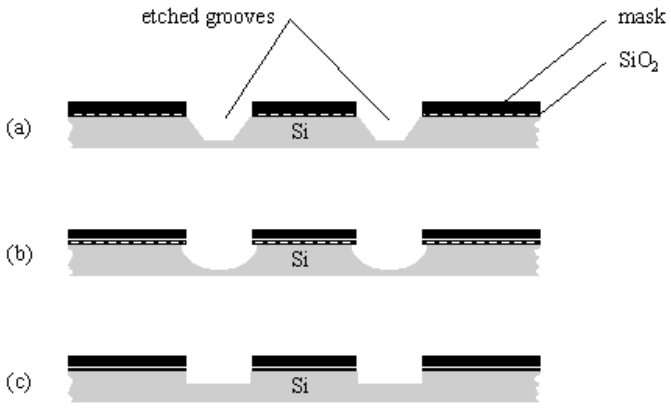


Fig 1.6. Comparison of the bulk micromachining process: (a) Anisotropic etching. (b) Isotropic etching. (c) RIE.
(Image courtesy from terpconnect.umd.edu)

1.2.2.2 Dry Etching

Unlike wet etching with corrosive liquid or etchants, dry etching usually applies plasma-based reactive gases or vapors to perform the etching process, and it is usually at high temperatures. Reactive ion etching (RIE), the most common form of dry etching method for MEMS process, utilizes the radio frequency (RF) power as the additional energy to drive the chemical reaction on the targeted substrate to be etched. The physical bombardment by the energetic and reactive ions is accelerated towards the targeted substrate to be etched within a plasma phase to supply the additional energy needed for the reaction. As a result, the etching can occur at much lower temperatures than those usually needed at temperatures above 1000ºC. Besides, RIE is not limited by the crystal structures in the silicon structure. Therefore, deep trenches and pits, or even any shapes with vertical walls, can be etched by RIE [18]. Deep Reactive Ion Etching (DRIE) is a much higher aspect-ratio etching process than RIE. In this technology, protective polymer is deposited and high-density plasma etching is performed to achieve higher aspect ratios, as shown in Figure 1.7. The etching rates in dry etching process depend on the time, concentration, temperature, and material to be etched.

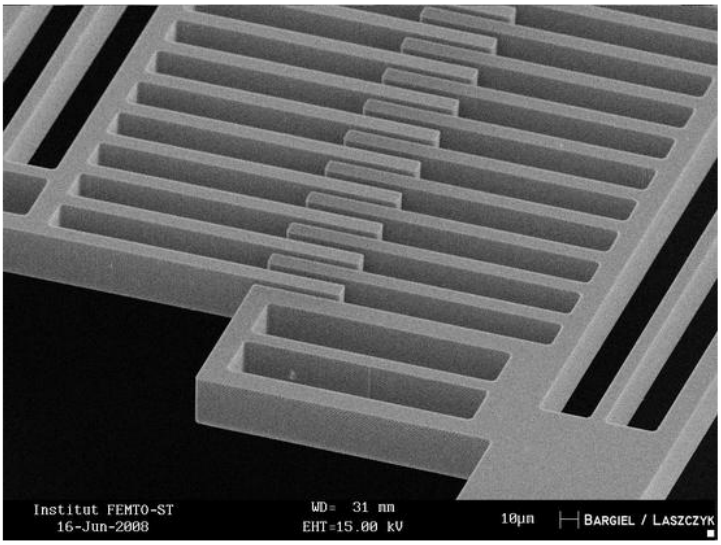


Fig 1.7. Electrostatic comb-drive actuator fabricated by Deep Reactive Ion Etching (DRIE) of silicon-on-insulator (SOI) wafer.
(Image courtesy from www.actmost.eu)

The most noticeable difference in the fabrication process of MEMS from traditional integrated circuit fabrication is the ability to modify the substrate with the two basic techniques: surface micromachining and bulk micromachining, as shown in Figure 1.8. Bulk micromachining features inside the substrate, while surface micromachining is based on the deposition and etching of different structure layers on top of the substrate. In the following, the detail will be introduced.

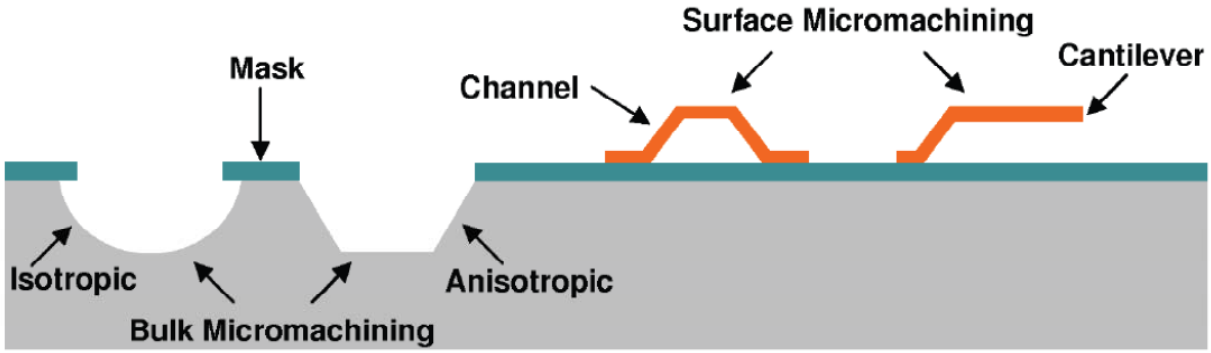


Figure 1.8. Comparison of bulk micromachining and surface micromachining in cross-sectional view.

1.2.3 Surface Micromachining

Surface micromachining focus on the processing above the substrate, mainly using the substrate as a foundation layer to build the other structures. Surface micromachining was originated in the 1980's and is the contemporary MEMS fabrication technology. Because this process does not depend on the etching characteristics of the substrate, various materials, such as soda lime, metals, and silicon on insulators (SOI) are also used in this process. Material is added to the substrate in the form of thin film layers on the substrate surface by deposition or bonding. These layers can either be the main structural layers or act as the spacers (sacrificial layers) for a suspended structure, which will be removed later by wet etching. Among them , common sacrificial materials include photoresist and oxide. Hence the surface micromachining process usually consists of films with two different materials. One is the main structural material and the other is the sacrificial material. The sacrificial material is first deposit on the substrate and patterned by dry etching process. Subsequently, these main structure layers are deposited on top of the sacrificial material and then dry etched to pattern the microstructure. The sacrificial material is finally wet etched away to release the final microstructure. Additionally, introduction of each additional layer will also result in higher difficulty in fabrication because of the increasing level of complexity. The process of a typical surface micromachined cantilever beam is shown in Figure 1.9 (Left). Here, the oxide sacrificial layer is first deposited on the silicon substrate surface by photolithography process as the sacrificial layer. A polysilicon layer is then deposited and patterned by RIE processes to form a cantilever beam with a pad anchored on the silicon substrate. The wafer is then wet etched to remove the sacrificial oxide layer. The beam is finally released and left on the silicon substrate. Even more complicated MEMS structures, such as sliding structures, actuators, and free moving mechanical gears, can be achieved using structural polysilicon and sacrificial layer, like photoresist and oxides.

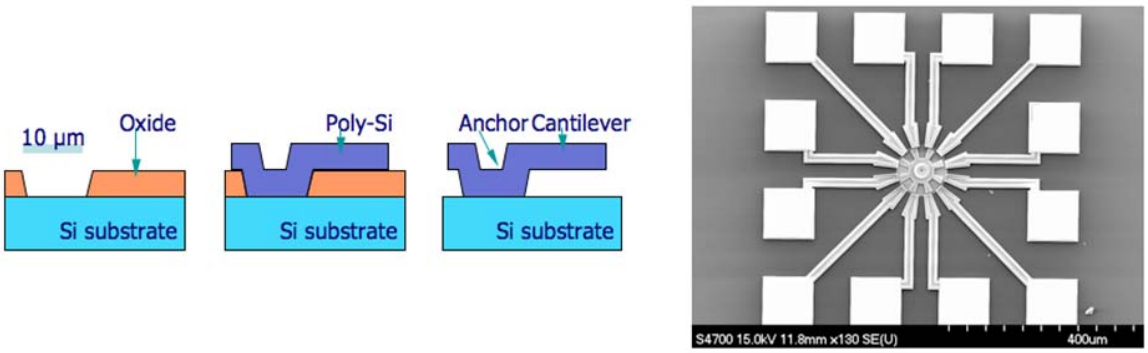


Figure 1.9. (Left) Illustration of surface micromachining process. (Right) Polysilicon micromotor fabricated using a surface micromachining process.
(Image courtesy from www.mems-exchange.org)

Figure 1.9 (Right) shows another example: the polysilicon micromotor fabricated using a surface micromachining process. In this device, five mechanical levels of micromachined polysilicon can be achieved using Sandia Ultra-Planar Multi-Level Technology (SUMMiT). The key point of the surface micromachining process depends on the ability to successfully remove all of the sacrificial layers to free the structural elements so that the micromotor can be actuated.

1.2.4 High-aspect-ratio Micromachining

High-aspect-ratio micromachining (HARM) is a process which utilizes micromachining to fabricate structures followed by injection molding or embossing. Electroforming technique can also be applied to replicate microstructures in metals. HARM is one of the most popular technologies for replicating microstructures because the nature of high-performance but low-cost. Commercial products fabricated by HARM include microfluidic structures, such as molded nozzle plates which can be used for inkjet printing, and the microchannel plates in medical diagnostic applications. Among them, the materials that can be used in HARM are the electroformable metals and plastics, such as polyimide, acrylate, and polycarbonate.

1.2.4.1 LIGA

LIGA is an important fabrication process for high-aspect-ratio microstructures by tooling and replication [19]. It exposes a thick acrylic resist of PMMA under a lithographic mask by applying X-ray synchrotron radiation, as shown in Figure 1.10. The exposed areas are then chemically dissolved. Metals are subsequently electroformed in areas where the materials are removed. The tools insert for the succeeding molding step are then defined. LIGA has the capability of creating very well fabricated microstructures up to 1000 μm high. However, LIGA usually has the limitation on the need having access to an X-ray synchrotron facility.

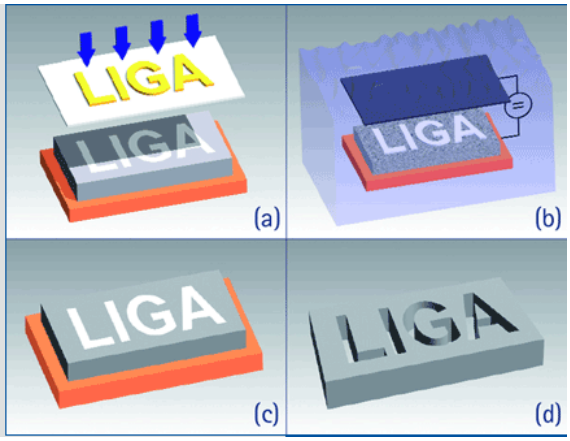


Figure 1.10. LIGA process: (a) Exposure. (b) Electroplating. (c) Finishing to height. (d) Removal of the substrate.
(Image courtesy from www.micro-works.de)

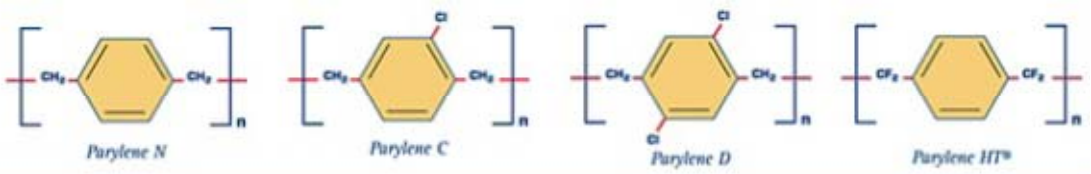
1.2.4.2 Laser Micromachining

Laser micromachining processes usually are not fast enough for effective MEMS fabrication process because the unparallel nature. However, they are still useful in some micromachining areas, such as making a mold. For example, excimer laser micromachining technique is applied particularly for the micromachining on plastics and polymers because those materials cannot removed by traditional processes like burning or vaporization. Besides, materials adjacent to the laser area are not melted or damaged by the heat from lasers. Although not very popular, laser micromachining have

found some other applications in MEMS area. Among them, laser cutting, laser drilling, laser annealing, and etching are the most common applications.

1.3 Parylene

Parylene is the trade name for members of a unique family of plastic polymers which are deposited by the dimer of para-xylylene (di-para-xylylene, or DPXN) [21]. It was first discovered by Dr. Michael Mojzesz Szwarc at the University of Manchester, England, in 1947 and commercialized by Union Carbide Corporation in 1965 [22]. Parylene is used in various industries because of its many excellent properties. Among them, the major application is in the electronics industry for the application on the printed circuit board (PCB) coating. Here, parylene protects the electronic devices against damages from moisture and corrosive etchants. Figure 1.11 shows the chemical structures of the three most commonly used parylene types: parylene-N, parylene-C, and parylene-D. A new parylene variant, which is called parylene-HT is also demonstrated here. In which, parylene-N is poly-para-xylylene, a completely linear and highly crystalline polymer; parylene-C is essentially parylene-N with a chlorine atom replacing one of the aromatic hydrogens; parylene-D is very similar to parylene-C, but with two aromatic hydrogens being replaced with chlorine atoms. The benzene backbone of the parylene family makes them very chemically inert. At the same time, the polyethylene-like interconnect makes them flexible. More detailed electrical, mechanical, thermal, barrier, as well as optical properties of parylene family can be found on a parylene vendor's website.



Vaporizer	170°C	170°C	170°C	155°C
Pyrolysis	650°C	690°C	700°C	750°C

Figure 1.11. Chemical structure of Parylene-N, -C, -D, and-HT and the process temperature.

A list of selected properties of parylene-N, -C, -D and -HT is shown in Table 1.1. Parylene exhibits outstanding mechanical strength and flexibility as a thin film coating. With Young's modulus of around 4 GPa (similar to Nylon) and an elongation-to-break percentage of more than 200%, parylene-C is a perfect membrane material on bio-MEMS applications.

Besides, parylene is also an excellent electrical insulator with high electrical resistivity. For example, the breakdown voltage for 1 μm thick parylene is over 200 volts. Because the parylene film is highly conformal and pinhole free, it is also an excellent barrier to gas and moisture with moderate thickness. In addition, parylene is extremely inert to many chemicals and solvents. Based on the manufacturer's study, solvents have a minor swelling effect on parylene-N, -C, and -D, with a 3% maximum increase in film thickness. The swelling is found to be completely reversible after the solvents are removed by vacuum drying. Inorganic reagents, except for oxidizing agents at elevated temperatures, have little effect on parylene. Optically, parylene is transparent in the visible light range. It only absorbs light under 280 nm in wavelength, which unfortunately limits its UV applications. Due to their slightly different chemical structures, the four types of parylene also differ in properties. Parylene-N has very good gap penetration characteristics. However, parylene-N also has the slowest deposition rate. Parylene-D can withstand higher temperature than parylene-C. Parylene-C has a useful combination of electrical and physical properties, plus a very low permeability to water vapor and other corrosive gases. Moreover, the deposition rate of parylene-C is

faster than that of the other two. Parylene-C is hence the better choice for most traditional biomedical applications. Parylene-HT is the new variant, and is expected to be a good prospect with its better thermal stability, improved electrical properties, increased UV stability, better crevice penetration, lower coefficient of friction, and better barrier properties [23]; it is also ISO 10993 biocompatible [24-26].

The parylene deposition process, called Gorham process [27], and the involved chemical processes are illustrated in Figure 1.12. The process starts with placing parylene dimer (di-para-xylylene), a stable compound in granular form, into the vaporizer, and the substrate to be coated into the deposition chamber. The whole system is pumped down to medium vacuum. The dimer is then heated in the vaporizer and sublimes into vapor at around 180 °C. The dimer vapor enters the pyrolysis furnace, controled at 690 °C, where the parylene dimers are dissembled into identical monomers (para-xylylene). In the room-temperature deposition chamber, the monomers reunite on all exposed surfaces in the form of polymers (poly-(para-xylylene)). The deposition takes place at the molecular level. The monomers are extremely active molecules which have a mean free path on the order of 1 mm (under deposition pressure of around 100 mTorr), resulting in superior penetration ability and a high degree of conformability to the exposed surfaces. Also, the coated substrate temperature never increases more than a few degrees beyond ambient temperature. Additional components of the parylene coating system include a mechanical vacuum pump and associated cold trap for pressure control. The process of parylene-C is almost identical to all four types of parylene, except for some minor differences in the setting of pyrolysis temperature and deposition pressure. Typical deposition thickness ranges from five to tens of microns. It can also be deposited as thin as hundreds of angstroms as a semi-permeable structure for the application on filters. The deposition thickness can be controlled by the amount of dimer placed in the vaporizer. The normal deposition rate of parylene- C is about 3 μm per hour. It is directly proportional to the square of the monomer concentration and inversely proportional to the absolute temperature. However, higher deposition

rates can result in films with poor quality, which often appears as a opaque milky film, in contrast to the normal clear transparent ones.

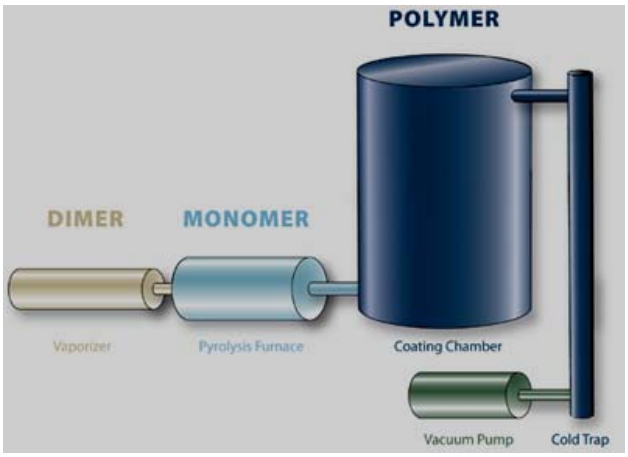


Figure 1.12. Illustration of the deposition system of Parylene and the process flow.

Table 1.1 Important properties of Parylene-N, -C, -D, -HT, and PDMS [28-29].

Property	Parylene N	Parylene C	Parylene D	Parylene HT	PDMS [29]
Dielectric Strength (V/mil), 1 mil film	7,000	5,600	5,500	5,400	610 [75] (1 mm film)
Dielectric Constant 60 Hz 1 kHz 1 MHz	2.65 2.65 2.65	3.15 3.10 2.95	2.84 2.82 2.80	2.21 2.20 2.17	2.3-2.8
Young's Modulus (psi)	350,000	400,000	380,000	--	52 – 126
Index of Refraction	1.661	1.639	1.669	--	1.4
Yield Strength (psi)	6,100	8,000	9,000	--	325
Elongation to Break (%)	20-250	200	10	--	210 – 310 [30]
Coefficient of Friction Static Dynamic	0.25 0.25	0.29 0.29	0.33 0.31	0.145 0.130	-- 0.43-0.51 [31]
Density (g/cm^3)	1.10-1.12	1.289	1.418	--	$9.7*10^{-4}$
Melting Point (°C)	420	290	380	>450	-49.9 – 40
Thermal Conductivity at 25 °C (10^{-4} cal/(cm*s*°C))	3.0	2.0	--	--	3.6

Water Absorption (% after 24 hours)	< 0.1	< 0.06	< 0.1	< 0.01	-- (depends on cure conditions)
Specific Heat at 20 °C (cal/g*°C)	0.20	0.17	--	--	0.35

1.4 Integration Technology

1.4.1 Traditional Chip Integration Technology

Soldering

Soldering, as shown in Figure 1.13, is a bonding process used to connect two separate metals together with a third metal which usually has a much lower melting temperature compared to the other two metals that need to be connected together. In addition to the physical reaction, there is also a chemical reaction happened in the soldering bonding process. Soldering bonding process is mainly applied to create a convenient and fast joint to make a good electrical contact between two separate metals. Solders typically do not provide very high mechanical strength because of the soft nature of popular solder materials. Soldering process is used extensively in the electronics industry for discrete components connected with printed circuit boards (PCBs). Its advantage is the easy application for quick and dirty bonding of discrete components with PCBs for bench testing, but the physical weakness of the solder bonding, toxicity of the materials, local heat problem necessary for bonding, and its inability to connect small and dense array pads makes soldering a less attractive choice than other more advanced technologies.

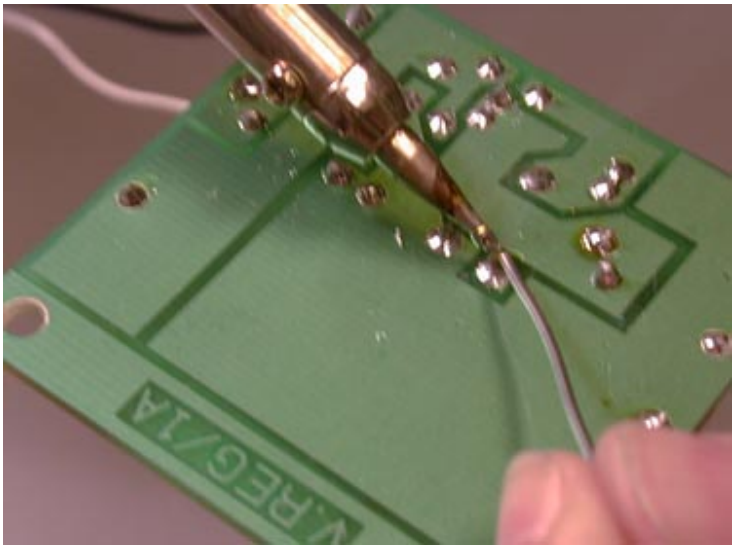


Figure 1.13. Demonstration of soldering.
(Image courtesy from letsmakerobots.com)

Wire Bonding

Wire bonding, as shown in Figure 1.14, is a process used to connect an on-chip pad and a substrate pad with a fine conducting wire. This substrate may be another chip or the bonding pads on PCBs. Popular materials for wire bonding include gold (Au) and aluminum (Al). The main advantage of wire bonding technology is the low-cost characteristics. However, the disadvantages include the requirements of larger bonding pads with size of around 100 × 100 μm^2, and larger bonding pitch with size of around 200 μm. Besides, wire bonding requires large quantities of gold. It also has lower production rate, relatively poor electrical performance, and variations in bonding geometry. The robustness and reliability are also serious issues. In addition, it cannot be used on flexible PCBs for implant application since the wire bonder can easily damage the flexible substrates.

To date, the most advanced wire bonders can achieve up to around 14 wires per second. Therefore, it remains more competitive than flip chip bonding for up to 500 I/Os per chip. The greatest advantage of wire bonding is its process flexibility and the sheer quantity of wire bonders. In

addition, the wire bonding technology is extremely flexible: changes in die size can be accommodated without noticeable additional costs.

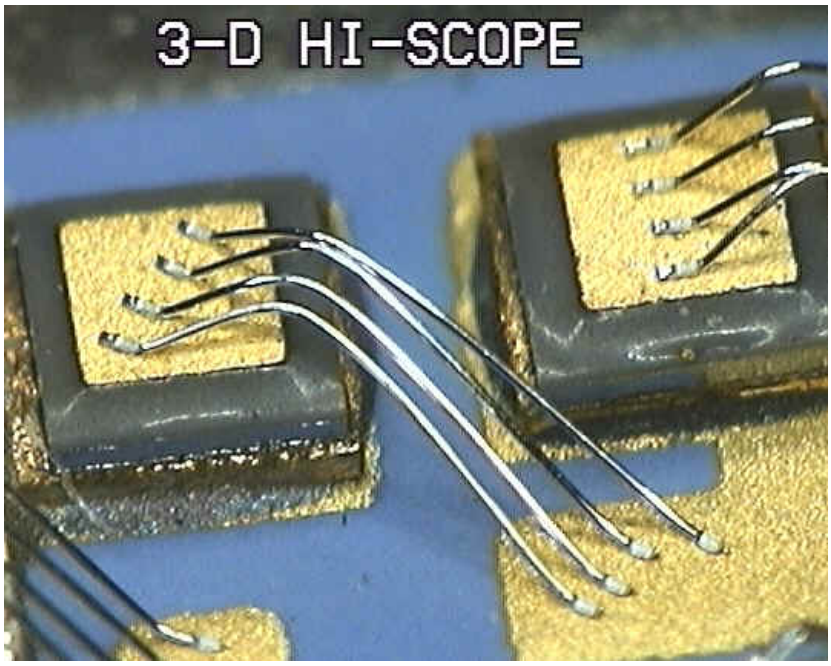


Figure 1.14. Demonstration of wire bonding.
(Image courtesy from www.caltexsci.com)

Flip Chip

Flip chip bonding technique, as shown in Figure 1.15, is developed to make electrical connection between the face-down components onto substrates, carriers, and PCBs by solder bumps on the chip bonding pads. Since wire bonding, the older technology which is gradually replaced by flip chip, uses face-up chips with a fine wire connection to each pad, therefore, the huge impedance contributed by the fine and long wire might be an issue. However, in flip chip, the interconnect length between the chip and the substrate is much shorter, and thus the impedance of interconnect is well controlled to be smaller. This is part of the reason that flip chip is applied in high clock speed applications. In addition to its better electrical property, the flip chip bonding is also capable of

connecting all I/Os in a single process step. Besides, the solder bumps can be placed over the whole chip surface, which implies the ability to make connections to the chip with significantly higher I/O density. This advantage allows additional power and ground connection, which is possible to further increase the electrical performance.

While the flip chip bonding technique benefits the devices with high performance, its high cost is still the main challenge and limitation for main stream applications. Thus, much effort and attention continues to be made to reduce the costs. Besides, the toxic joint materials, solder bumps, are totally not desirable for implantable devices. Additionally, the global heating needed during bonding process also limits its application on some substrates which cannot stand at high temperatures.

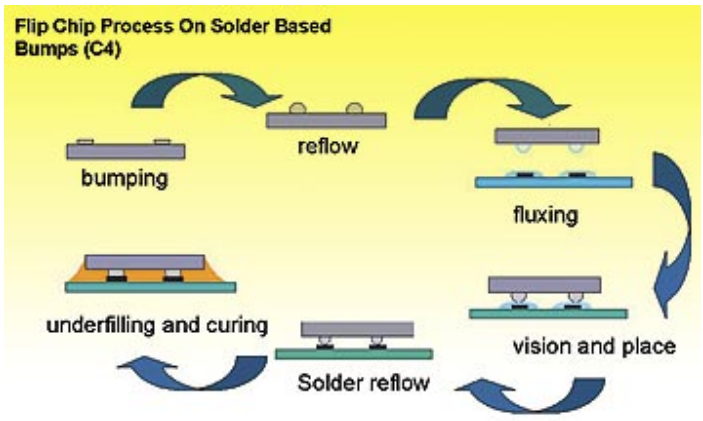


Figure 1.15. Demonstration of the process of flip chip assembly. (Image courtesy from www.chipscalereview.com)

1.4.2 State-of-the-art Chip Integration Technology

1.4.2.1 Microflex

Microflex (MFI) is a new three-dimensional (3D) interconnect technique developed by the Fraunhofer Institute for Biomedical Engineering in Germany. Meyer et al. [32] utilizes a polyimide based multiple strand flexible ribbon cable with a photolithography patterned double metallization layer embedded in it. The pitch and the shape of the metal pads on the polyimide based device

correspond to the bonding pads on the chip. The via-hole of the contact pads on the ribbon cable is then filled with metal balls or wedges applied by a commercial wire bonder. The metal pair is welded and results in a mechanically stable and electrically reliable contact. This technology, though derived from the common wire bonding technology, is specifically designed and developed to integrate the passive and active electronic components to the electrodes, as shown in Figure 1.16.

The applied materials, such as polyimide substrate, platinum, and irridium, in this technology showed an excellent biocompatibility during *in vitro* and *in vivo* testing. In addition, this substrate has also proved to be non-cytotoxic according to the international standard DIN EN ISO 10993. Also, in chronic implantations in the sciatic nerve of rats and on the retina of rabbits, they caused no significant tissue reactions or alterations. The Microflex technology can also be applied to three-dimensional (3D) structures and the density is comparable to that of the flip chip technology. Several ultrasound array sensors, retinal stimulators (EPIRET), and multiplexer modules have been integrated successfully with this technology [32–35].

The current device, EPIRET 3, has transmitting coils on external glasses and an internal receiver coil and chip secured in the eye in place of the lens, as shown in Figure 1.17. It can transfer energy and data from the external power source to the implant. Based on the design of epiretinal prosthesis, the stimulator was placed slightly inferior to the fovea and fixed with retinal tacks. In an exploratory human trial in 2009, the device was implanted for four weeks to observe the safety of the device and how well it would work. There was mild inflammatory response in some of the six patients which were treatable by local antibiotic and steroids, but they decided there was no lasting damage from the prosthesis. Four of the six patients gained light perception, one gained hand movement, and one had no light perception [36]. However, more clinical trials are still needed to demonstrate the long-term biocompatibility. Besides, the mechanical properties of the bond on the substrate have yet to be tested as well. In addition, its tedious and low yield process also makes it difficult and costly to integrate device with high density electrodes.

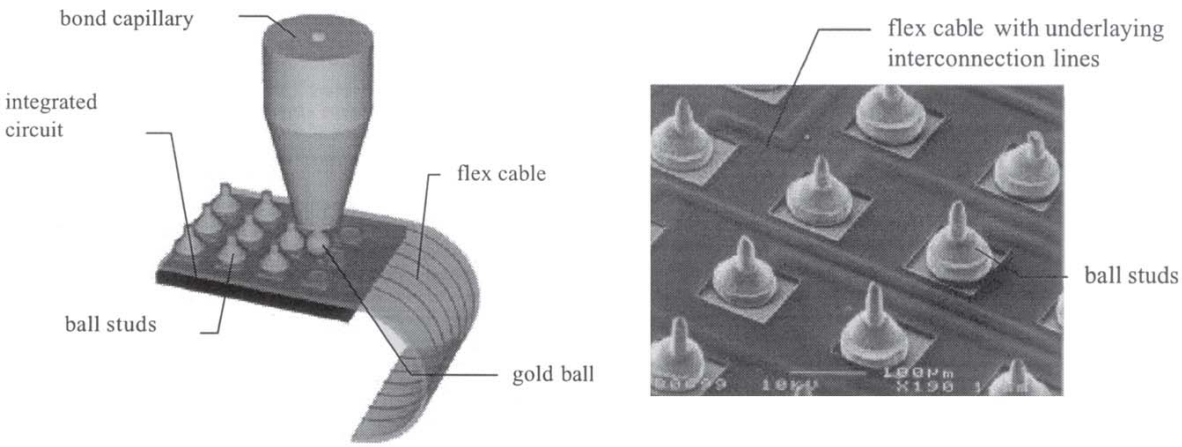


Figure 1.16. (Left) Overview of the Microflex technique. (Right) SEM pictures of the contact array. [34]

Figure 1.17. Final implant with parylene C and silicone rubber encapsulation [35].

1.4.2.2 Boston Retinal Implant Project

Dr. Wyatt and Dr. Rizzo from Massachusetts Institute of Technology developed a subretinal implant device aiming to achieve the goal of visual prosthesis [37]. This device is also based on the polyimide substrate. The host flexible circuit was made by defining the metal trace with width of 50 μm on the host polyimide substrate using the lift-off process by photolithography. All of the

prosthesis components were then assembled on the host polyimide substrate. Because the period for the animal surgical implantation trials was limited, these traces were fabricated from a Cu/Ni/Au metallization which were commonly used in industry for microelectronics. Besides, the coils were fabricated from Cu wire. Standard surface-mounted components were used for all the off-chip power supply parts, and these were assembled on the flex circuit substrate using conventional wave soldering techniques. The ASICs were mounted by stud bumping with 75-μm-high Au bumps, followed by flip-chip die attachment to the host substrate. The stud bumping was also used for the flex-to-flex connections between the flex circuits and the electrode arrays.

Although this device has gone through several *in vivo* studies, the integration approach proved to be prone to reliability problems. Also, the encapsulation coating by PDMS has less reliable performance relative to other biocompatible coatings.

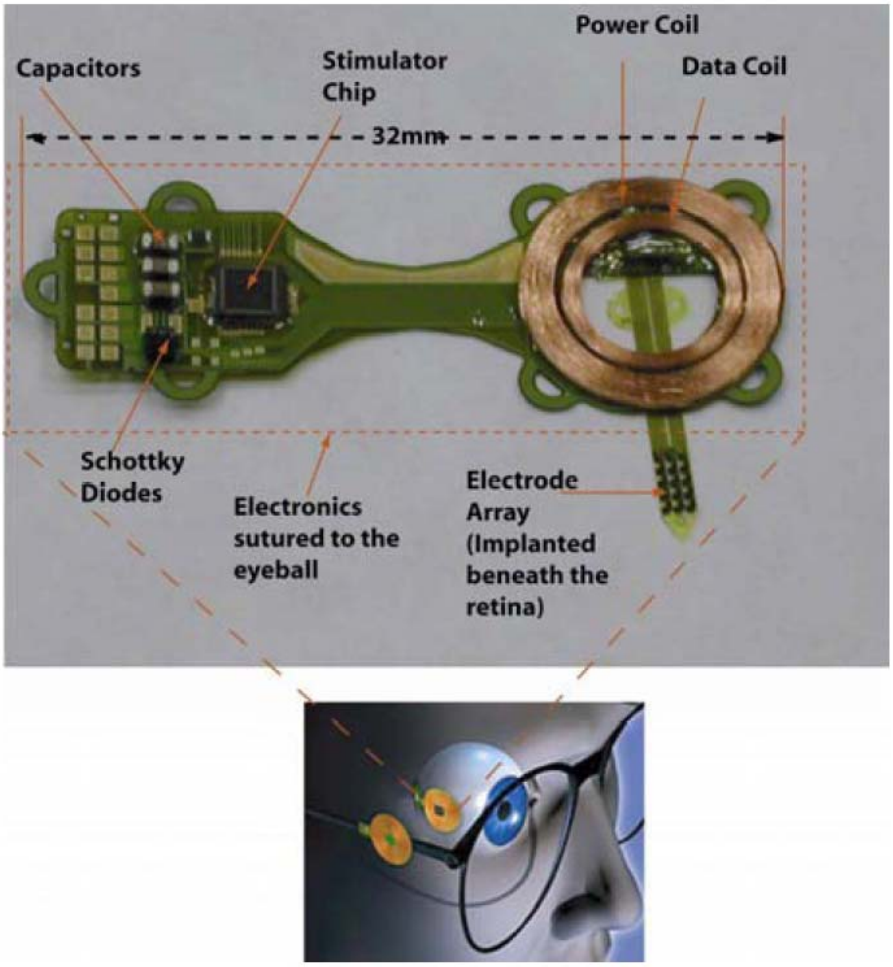


Figure 1.18. Schematic representation of the minimally invasive ab-externo approach. The transmitter coils are placed outside on a pair of eyeglasses and the receiver coils and the stimulator chip are placed on the eyeball. The electrode array is placed in the subretinal space through a scleral flap [37].

1.4.2.3 California Institute of Technology—CL-I^2

Rodger and Li et al., have developed a chip level integrated interconnect (CL-I^2) and further extended to an embedded chip integration technology and successfully demonstrated by integrating the flexible polymer (parylene) substrate RF coil with commercially available IC chips and other passive discrete components [38-39]. Figure 1.19 illustrates the conceptual schematic of this approach. In which, individual prefabricated chips and passive components can be embedded in a

carrier silicon wafer and directly integrated with an MEA and with, ultimately RF coil power and data connections. Finally, all the components will be further sealed with a parylene coating.

The cavity matching the chip dimension is first etched on the parylene-on-silicon substrate for chip placement by DRIE. After the chip is dropped into the cavity, parylene deposition is performed again to seal the chip and serve as the insulation between two metal layers. Then, the metal is deposited and a photolithography step is done to make the electrical connection between the pads on the chip and the other pads on outside components. The structure is finally released by back etching of the silicon substrate.

The parylene substrate to be integrated with the chip is based on the parylene-based skin technology which has been well characterized both *in vitro* and *in vivo* and is also approved by the FDA for long-term human implantations. However, the alignment problem that arises during the "chip-drop" could severely affect the feasibility of this technology. The surface flatness inside the cavity will limit the metal connectivity over a step. Furthermore, the low alignment efficiency of the bonding pads on the chip with the metal bonding pads embedded in the parylene skin renders the integration inefficient.

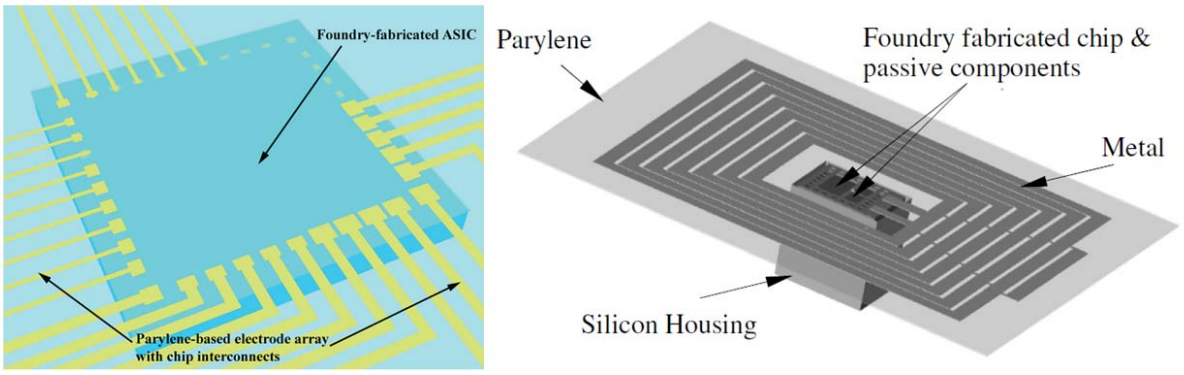


Figure 1.19. (Left) Illustration of the CL-I^2 packaging concept [38]. (Right) Concept of embedded chip integration [39].

1.5 Layout of the Dissertation

Chapter 2 first introduces the overview of the requirements for device packaging, and two generations of parylene flex fabrication. It also describes the integration technology for high-density multi-channel retinal IC chips. Other technologies related to the integration are also discussed. Besides, details on how to build a parylene flex with reliable metals and strong adhesion are also addressed. Chapter 3 demonstrates the application of photo-patternable adhesives on chip integration technology. The setup is built and the bonding force is measured. Functionalities of two real retinal IC chips are also successfully tested via the parylene flex to further confirm the effectiveness. Chapter 4 focuses on the lifetime study and surgical mockup design. The long-term packaging reliability is proved by accelerated and active lifetime soaking test. In addition, the mockups for 512-channel and 1024-channel retinal IC chips are both successfully implanted in a dog's and pig's eye. Chapter 5 presents the final wireless 1024-channel retinal implant device. A parylene flex with a dual-metal-layer structure is first successfully built to relax the metal interconnections. Treatments on stimulating output electrodes are also studied. Complete integration of the 1024-channel retinal IC chip, discrete components, and coils with parylene flex is also introduced here.

1.6 Summary

This chapter introduced the mechanism of the retinal prosthesis and the two most common leading causes of blindness induced by degenerative retina: age-related macular degeneration (AMD) and retinitis pigmentosa (RP). MEMS technologies, including photolithography, bulk, surface, high-aspect-ratio, and laser micromachining, that are used to build the all parylene flex in this thesis were also described here. Biocompatible materials, parylene-family, were also studied here and all the properties were compared. Traditional chip integration technologies, such as soldering, wire bonding,

and flip chips, and state-of-the art chip integration technology with a bio-device were also discussed in order to compare the pros and cons. A reliable high-density packaging scheme that allows stimulating circuitries to be integrated with the bio-device is definitely in high demand, but current state-of-the-art technologies still lack the ability to demonstrate high-density multi-channel connection to commercial IC chips. Parylene-family with high biocompatibility which is compatible with MEMS technology is believed to be one of the best materials on the implant application. Therefore, a flexible parylene flex combined with integration technologies which will be discussed in the following chapters will be used to address the issues and to achieve full system integration.

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2 HIGH-DENSITY MULTI-CHANNEL CHIP INTEGRATION

2.1 Introduction

Recent research on retinal implants has asked for more reliable and biocompatible hermetic packaging techniques with integrated circuits (IC). Besides, high-density multi-channel IC interconnects also become a major requirement to realize high-resolution application on electrical stimulation and recording. Previously proposed integration methods by other groups in order to achieve this goal include: CMOS/MEMS integrated process to eliminate the post-fabrication connection [1-5]; wire bonding technique to bond pads on chip to pads on substrate individually [6]; flip chip bonding technique for array connections [7-8].

However, these proposed connection methods, unfortunately, either have heat problems or can only be used for low density connections. Besides, flip chip bonding is also toxic which cannot be used for implantation. Thus, in order to overcome these challenges, our previous group members Rodger and Wen also developed a biocompatible chip-level integrated interconnect (CL-I^2) packaging technology [9]. In which, the IC chip is first arranged inside a pre-etched cavity on a wafer by DRIE and then connected to electrodes with a combination of traditional photolithography and metallization process. However, this method is still very sensitive to the surface roughness of the cavity after etching because the metal lines across a high step can result in unreliable electrical connection. Besides, the alignment is also a serious issue. Current state-of-the-art IC technology is able to achieve 1,024 stimulating electrodes on a very small chip area [9-10]. However, the real retinal implant that are currently in use or under development still lack the high-density multi-channel connection techniques which limit the further development of the number of electrodes

significantly. Besides, these systems also suffer from complicated IC integration schemes or depend heavily on process variables [11-12]. In order to bridge the gap between the number of the real functional electrodes and the number of electrodes that can be fabricated, we develop here the high-density multi-channel chip integration technology. It can not only overcome the connection challenges but also accommodate the increasing number of retinal prosthetic chips [13], which is a potentially versatile, biocompatible, flexible and reliable process. In addition, it also provides an excellent alternative for applications on IC integration and discrete component packaging, from fast prototyping to full system integration.

Parylene-C is a proven protective biocompatible material and has been widely used for coating devices due to its biocompatibility [14-15]. It is also a good material for implant applications [16]. In addition, studies from Rodger et al. [17] during an *in vivo* chronic rabbit eye implantation indicated no adverse immune response caused by implanted parylene-C. However, serious delamination due to low adhesion between parylene-C and silicon substrates or other materials often happens even during the standard MEMS processes such as metal lift-off and sacrificial photoresist releasing in acetone and ST-22 photoresist stripper. We believe it comes from bad surface cleaning on the coated surface, which will later cause severe failure and damage to the devices, as shown in Figure 2.1.

Ray et al. [18] utilized XeF_2 surface roughening (with 6.5 μm of silicon removal), parylene anchoring, parylene melting, and A-174 adhesion promoter to either increase surface area or enhance mechanical adhesion of parylene to silicon. However, among them, parylene anchoring required advanced DRIE techniques. Parylene melting needed to be done in nitrogen filled oven at 350°C. The effectiveness of A-174 adhesion promoter was limited by the thermal budget. Besides, all these methods are based on complicated procedures that have low yield and require long preparation time. Therefore, simple surface treatments which can enhance good interface adhesion between the deposited parylene-C and the coated surface are highly desirable. Interestingly, we have observed

that parylene-C deposition on a clean hydrophobic surface often provides a good interface adhesion from its chemical structure. In this chapter, we investigated several different chemical and plasma treatments to study the effectiveness of the adhesion enhancement. Several parameters were used to quantify these adhesion treatments including peeling force, soaking undercut rate, and vertical attack bubble density (VABD).

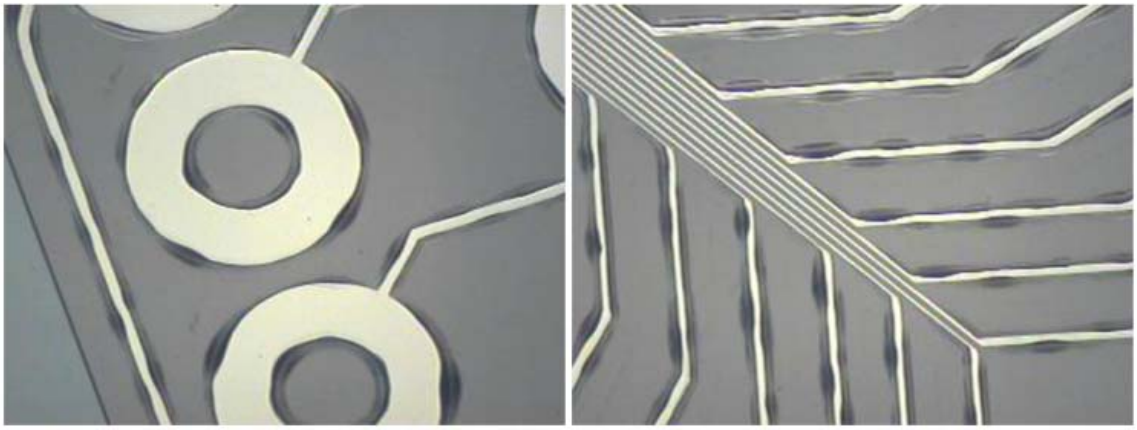

Figure 2.1. Parylene cracks occur on the edges of the metal lines; resulting in solution attack and causes delamination.

2.2 Overview of Requirements for Device Packaging

As shown in Figure 2.2, a wireless working retinal implant device basically includes a reliable parylene flex integrated with high-density multi-channel retinal IC chip, discrete components (capacitors, resistors. inductors, and oscillators), and coils (power and data coils). Due to the limitation of cut (~3mm) on eyeball and high resolution (1024 pixels) requirement, the width of metal lines for interconnection embedded in parylene flex will be very small. Besides, the density of pads on chip will be very high. For the parylene flex itself, it is basically a parylene-metal-parylene sandwich structure. In which, the reliability of metals and adhesion between each layer need to be well studied to build a reliable parylene flex with high yield. For the integration, a reliable

connection technique between parylene flex and high-density multi-channel retinal IC chip needs to be developed to create a strong bonding between them to survive during surgical manipulation.

The electrodes used to stimulate the retina is also very important. Firstly, the interface impedance needs to be decreased to allow the current send from the retinal chip to go through. Secondly, its shape also needs to be modified to better fit the retina. In order to satisfy the limitation of cut on eyeball, and allow 1000+ metal interconnections well allocate on this small area, attention also needs to be paid on the configuration of the device. Mockups have to be designed for surgical implantation trials. Finally, the lifetime of the whole device implanted in human body is also an important issue. When the device is implanted, the corrosive body fluid will continuously attack and corrode the device. A desired target of lifetime is 10 years which depends on the protection on the device.

In the following chapters, I will introduce the details about how to build a reliable parylene flex, how to create a strong bonding between the high-density multi-channel retinal IC chip and parylene flex, how to treat the electrodes, how to design the configuration of the device, and how to extend the lifetime of the whole device.

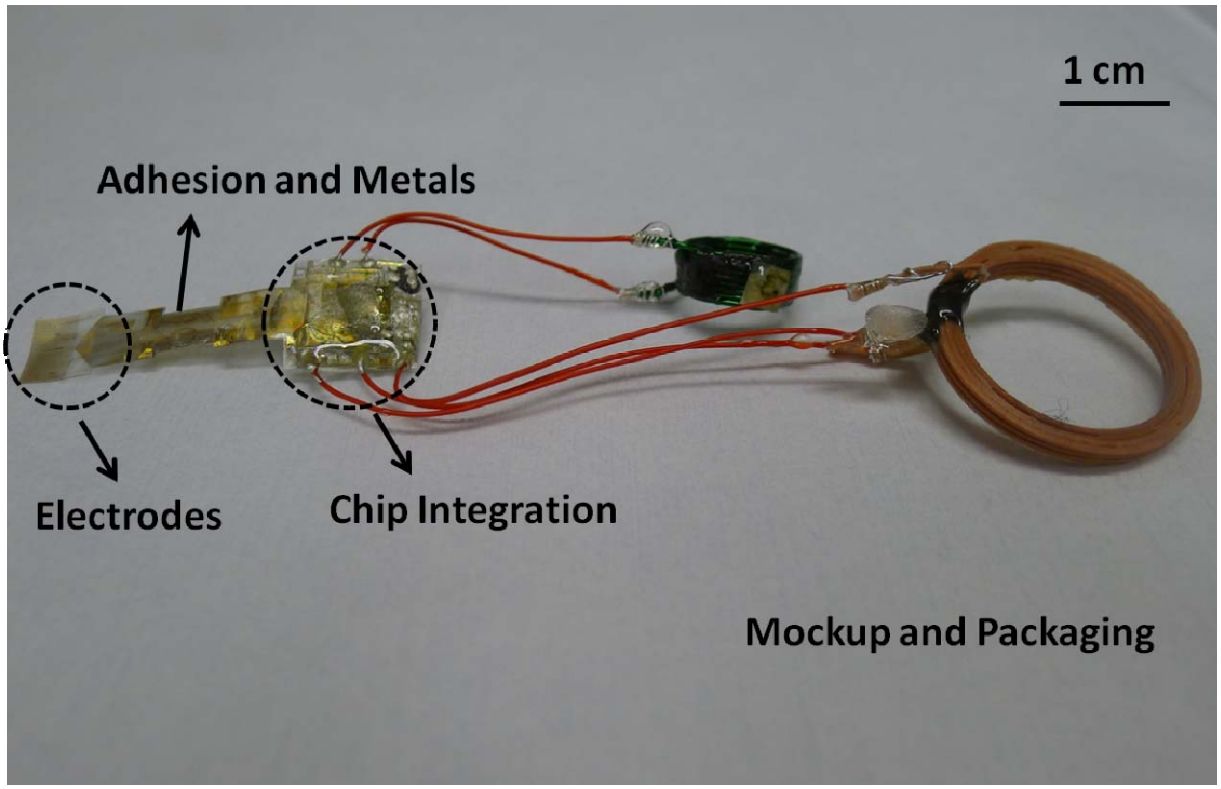

Figure 2.2. Requirements of packaging issues for a wirelessly flexible parylene-based retinal implant device.

2.3 Device Design

2.3.1 Metals

Metals embedded in parylene flex are for interconnections and used to send signal from retinal IC chip to the stimulating output electrodes for stimulation. In consideration of the biocompatibility, Titanium (Ti) and Gold (Au) combination were applied on the device. Ti was served as the adhesion layer between parylene and Au, and Au was served as the main metal layer to conduct current. All the processes of metallization in this thesis were based on lift-off process. Figure 2.3 showed the process flow. First, LOR3B (a lift-off photoresist from MicroChem) was spun on parylene (3K RPM; 100 ramp; 40 second), and baked in oven at 140°C for 15 minutes. Then, AZ1518 was spun on LOR3B with the same parameters, and baked in oven at 100°C for 30 minutes. After exposure by

UV light, the sample was developed in the AZ340 diluted solution (AZ340: DI water = 1:4). Dummy wafer with the same photoresist was highly recommended as the first step to get the best exposure and developing time. Undercut, as shown in Figure 2.4, needed to be checked every 5~10 seconds to make sure it is not over-developed. For the metal lines with very small pitch and separation, the pattern can be easily peeled off by over-developing and thus the lift-off process was failed. Ti/Au (0.2μm/3μm) was then deposited on the sample by E-beam deposition machine. Oxygen plasma descum was recommended to apply on the sample to further enhance the adhesion between parylene and metals. The sample was then soaked in Acetone for 2 hours to lift-off the non-desired metal parts. Ultrasonic bath and cotton swab can help accelerate the lift-off process. After rinsed by DI water, the sample was then soaked in ST22 to remove the LOR3B photoresist at 100°C for 2 hours. PSR and DI water were the final steps used to clean the samples to complete the whole lift-off process.

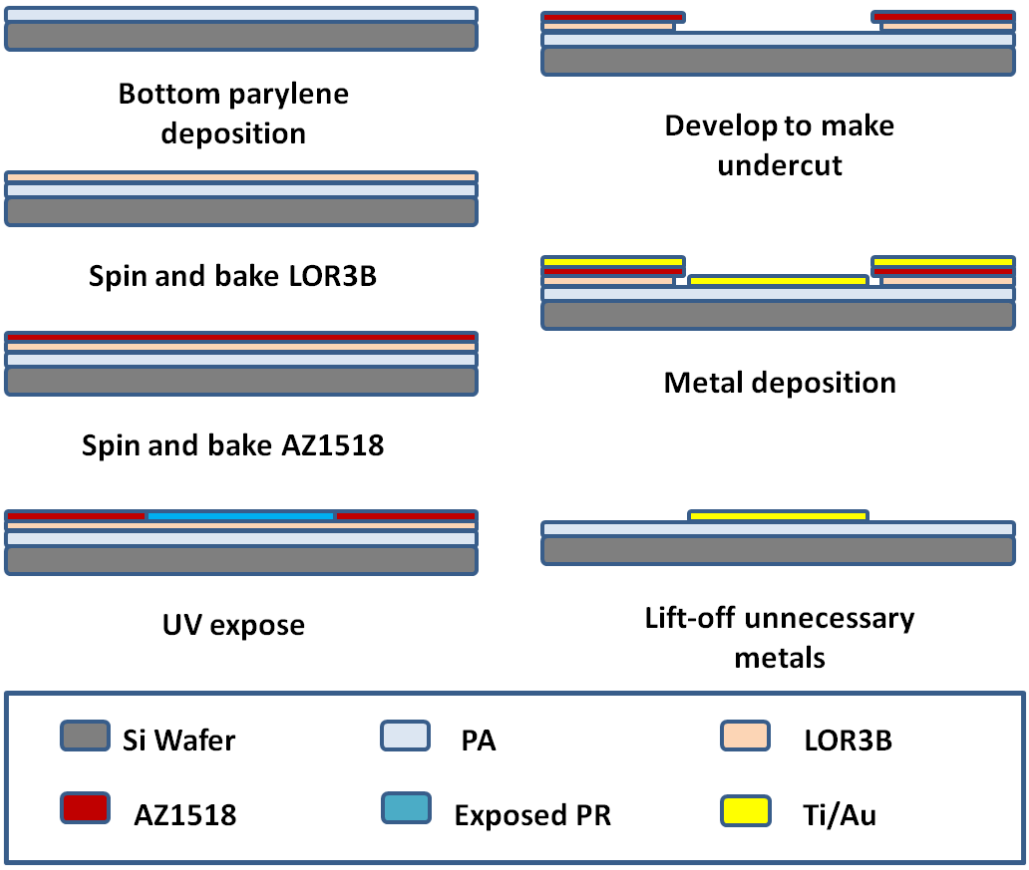

Figure 2.3. Lift-off process flow on parylene substrate.

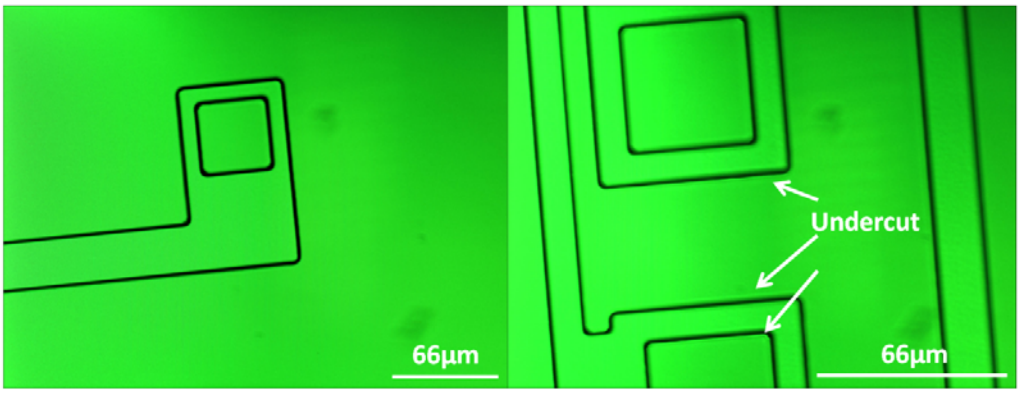

Figure 2.4. Comparison of patterns on sample after development without (Left) and with (Right) undercut.

2.3.2 FIRST-GENERATION PARYLENE-C FLEX FABRICATION

As shown in Figure 2.5 [19], the fabrication process of the first-generation flexible parylene-C flex started with a 5 μm parylene-C deposition on HMDS treated silicon wafers which will help the devices to be released from DI water, followed by Ti/Au metal lift-off process to provide electrical connection. A top parylene-C (~8 μm) was then deposited to complete the parylene-metal–parylene sandwich skin structure. AZ4620 photoresist was spun on the wafer as the parylene-C etching mask. Finally, electrode sites and the device contour were then defined by two-step oxygen plasma.

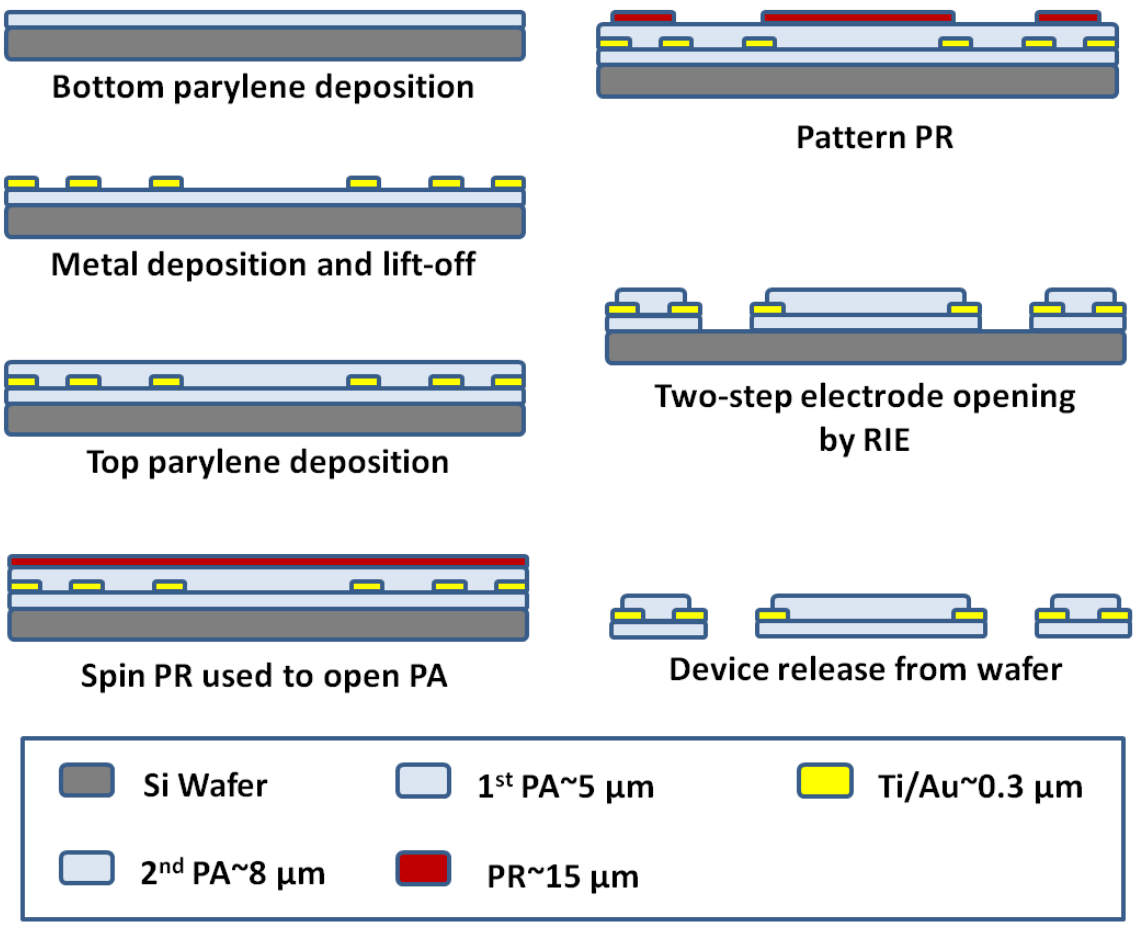

Figure 2.5. Fabrication process flow of the first-generation parylene-C flex.

2.3.3 SECOND-GENERATION PARYLENE-C FLEX FABRICATION

As shown in Figure 2.6 [20], the fabrication process of the second-generation flexible parylene-C flex started with a 5 μm parylene-C deposition on HMDS treated silicon wafers, followed by Ti/Au metal lift-off process to provide electrical connection. A top and thick parylene-C (~40 μm) was then deposited to complete the parylene-metal–parylene sandwich skin structure. Aluminum (Al) was deposited on the wafer as the parylene-C etching mask for the thick parylene. AZ1518 photoresist was then used to pattern the Al layer. Finally, electrode sites and the device contour were then defined by two-step oxygen plasma.

The main difference between first-generation and second-generation parylene flex is the thickness of top parylene layer. Different masks thus need to be applied to etch the structure.

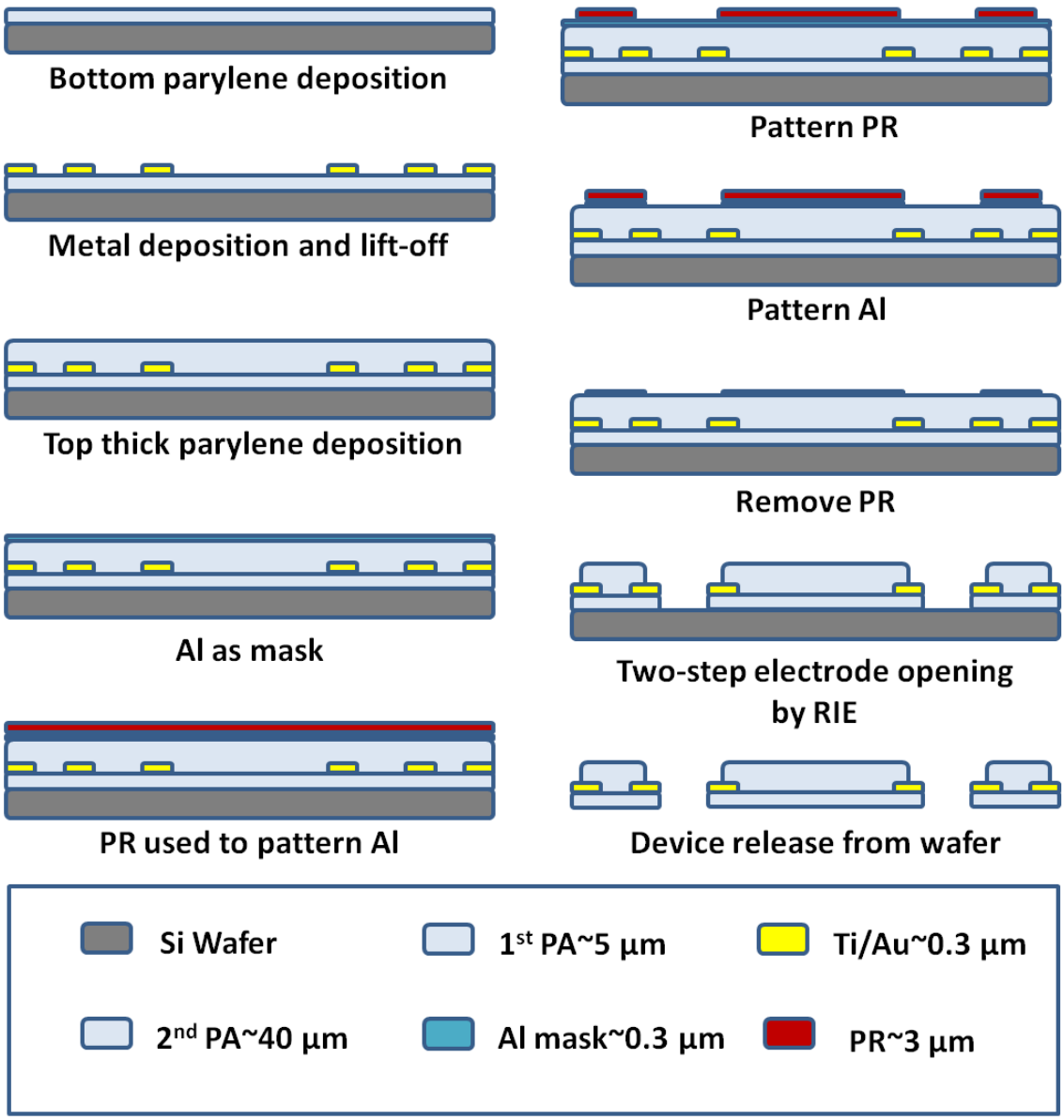

Figure 2.6. Fabrication process flow of the second-generation parylene-C flex.

2.4 Device Packaging

2.4.1 Alignment and Squeegee

After parylene flex was designed and fabricated, the next important step is how to integrate the parylene device with the high-density multi-channel retinal IC chips. The first chip we were trying to integrate is the 256-channel stimulation chip with a dimension of 5.3 mm × 5.1 mm × 700 μm. It includes 239-channel stimulating pads and 120+ input testing pads. Among them, 45 peripheral pads are for input voltages, clocks, and testing outputs. The pad size is 100 μm × 100 μm, and the smallest separation is only 42 μm. Basically, more than 300 very small bonding pads need to be connected without open and short circuits to functionalize this system, which is a very time-consuming and labor-intensive task. Therefore, a special connection technique has to be developed.

We first designed and fabricated the dummy chips with exactly the same pad layout but with conduction metal traces on substrate only (no circuit underneath). The alignment between the parylene devices with the IC chips was done under microscope. The resolution and accuracy is around 10 μm, as shown in Figure 2.7. Then, the commercially available conductive epoxy (MG Chemicals) was mixed well with a 1:1 ratio and the viscosity also needed to be well controlled. Because the parylene flex substrate has pre-designed cavities which were etched through in the fabrication process, the cavities can be served as the screen for this squeegee process after the dummy chip is aligned with the parylene flex substrate under microscope. A rubber squeegee was then used to get some epoxy and push it across the surface uniformly, so the epoxy can be filled into the cavities in the parylene flex substrate, and electrically and mechanically connect the parylene flex substrate with the high-density multi-channel dummy chip, as shown in Figure 2.8. After around 15 minutes of waiting for the conductive epoxy retained in the cavities to dry a little bit, acetone was then used to clean the top surface of the parylene flex to avoid a shortage happened on the top surface. The conductive epoxy can be then fully cured at room temperature after 4 hours. After curing, the adhesion is very strong that even acetone cannot remove it.

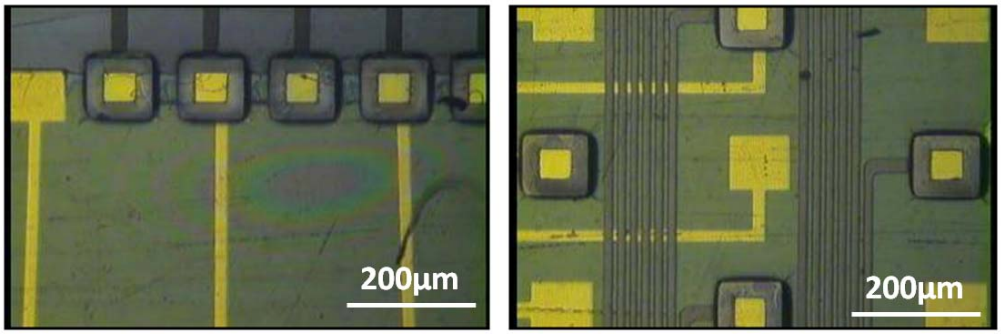

Figure 2.7. Alignment of the bonding pads with the metal pads on the chip. Alignment accuracy of 10µm can be achieved.

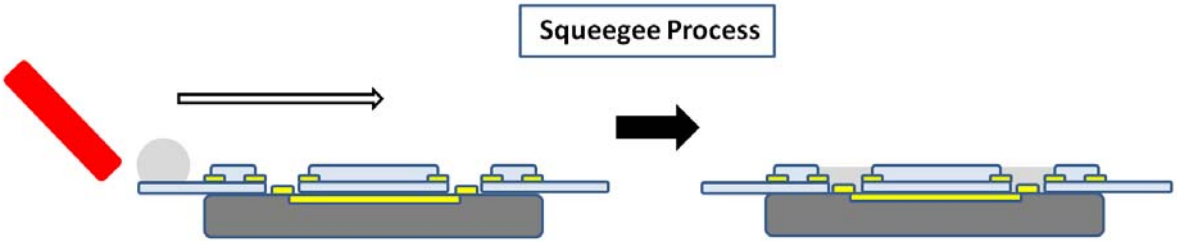

Figure 2.8. Squeegee process: After alignment, the rubber squeegee is used to push the excess conductive epoxy away from the surface into the cavities to make connections between parylene flex and chips.

2.4.2 Squeegee Issues

At this stage, this conductive epoxy squeegee process with the current fabricated parylene flex is not very reliable and stable because the cavities designed in the parylene flex have low aspect ratio and sometimes cannot retain the conductive epoxy very well. Thus, an additional photoresist lithography step was used to increase the aspect ratio of the cavities to make this process more reliable. A negative photoresist, SU-8, was used to create a higher well which can retain most of the conductive epoxy after squeegee process, as shown in Figure 2.9 (Left). An experiment was conducted to determine the optimized aspect ratio for these cavities after evaluating the bonding

efficacy. The epoxy footprints shown in Figure 2.9 (Right) showed that, after this additional step, there were no open circuits happened, which indicates that the conductive epoxy were retained very well in the cavity with high aspect ratio. Figure 2.10 (Left) also showed the surface of the parylene-C flex after conductive epoxy squeegee process and cleaned by acetone, and Figure 2.10 (Right) showed the profile of the bonding epoxy bumps examined by WYCO; the maximum height of the applied conductive epoxy is around 20 μm, and the height of the examined conductive epoxy bumps are very uniform to provide stable connections.

In addition, another advantage of this SU-8 layer is the high plasma etching resistance because of the epoxy nature of SU-8. Therefore, it can be also used as a mask to etch through a very thick parylene flex at the same time without an additional mask. This property can also be utilized to eliminate the thick photoresist cracking problem during RIE etching. However, the only trade-off of this process step is that SU-8 is not removable after photolithography patterning.

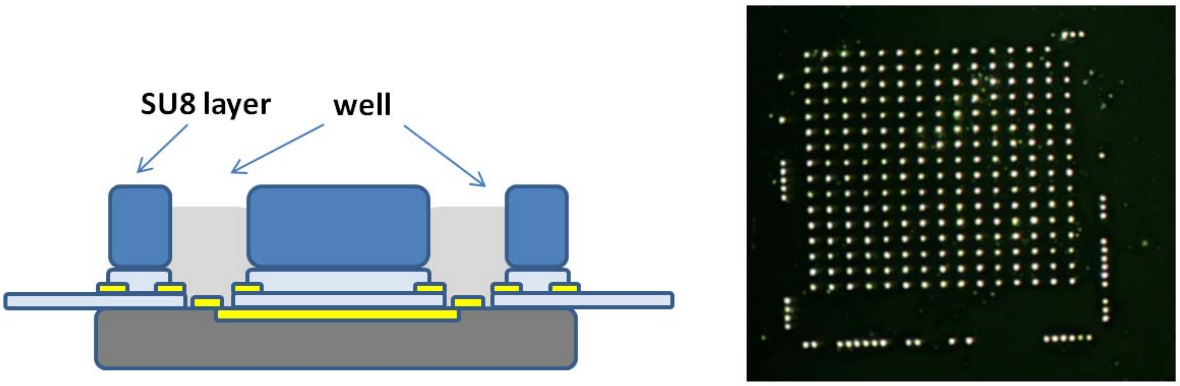

Figure 2.9. (Left) Add a layer of patternable epoxy to increase the aspect ratio. (Right) Footprint on a testing substrate with SU-8 wall after squeegee process.

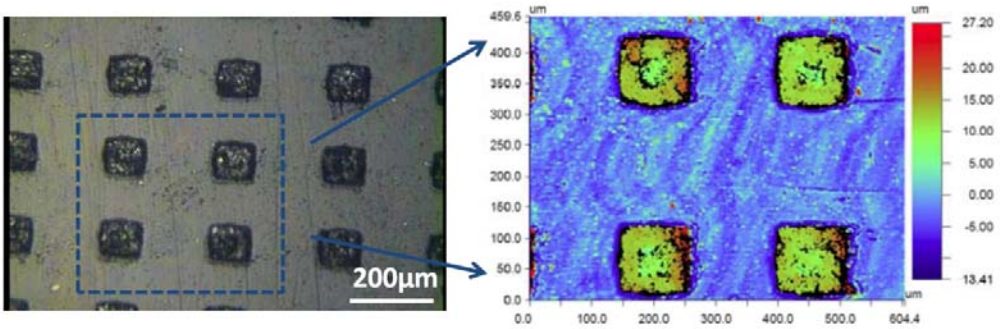

Figure 2.10. (Left) The surface of the bonding pads after squeegee and surface cleaning. (Right) The surface profile of the bonded conductive epoxy; average height is around 20 µm.

The peripheral pads need to be connected is also another issue that we need to pay special attention. They are located only around 10~20 µm from the edge. Figure 2.11 (Left) showed that the parylene flex near the edge would sometimes be more easily damaged than the other areas during the conductive epoxy squeegee process because of the transition of the squeegee process from an area with back support to an area without support at all. Due to the force distribution, the damages on edges could easily happen. If the embedded metals got damaged, the total system might be failed.

A PDMS chip molding technique was thus developed to fix this problem and to increase the connection yield and effectiveness of the conductive epoxy squeegee process, as shown in Figure 2.11 (Right). Dummy chip was first attached on a container. Then, the well-mixed liquid PDMS was poured on top of this dummy chip to create a cavity for the real IC chip. After the PDMS was cured according to the recipe from datasheet, the real IC chip can be fitted into the cavity. The PDMS mold was then cut with a razor blade to create the suitable size and shape to be aligned with the parylene flex. By further extending the area for conductive epoxy squeegee process, the peripheral critical pads can be well connected without damaging the parylene flex near the edge of the chip.

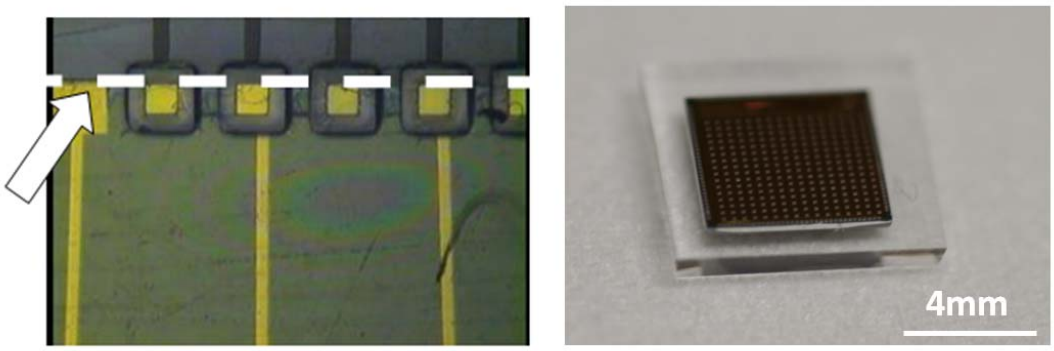

Figure 2.11. (Left) Edge of the chip-where the squeegee process may become a problem. (Right) PDMS mold fitted with a 256 channel stimulation chip.

2.4.3 Laser Cutting

Besides the issue of conductive epoxy squeegee process, another short circuit issue was also found and needed to be further studied. In the fabrication process, defects and contamination during wafer transport or handling can easily happen. Sometimes, the short circuits and open circuits of neighboring traces became unavoidable. If the short circuits occur on stimulation electrode interconnections, these short circuit defects may have little to no effect to the overall functionality of the system. However, they may have very serious effect when the defects occur on critical input lines or power supply lines. The entire system would not functionalize without the working critical input lines and the power supply lines. As a result, the repairing methods were developed with a UV laser cutting system to fix these defects. Figure 2.12 (Left) showed a case of short circuit of neighboring traces due to particle contamination during photoresist lift-off lithography process. This type of issues could occur on either stimulation or chip input lines and could have adverse effect of the functionality of the system and must be fixed. A method was presented here to etch away the shorted metal by laser cutting with a UV laser trimming system. The software on the laser trimming system allowed the user to control the power, size, frequency of each pulse, and the number of total pulses emitted to enables the laser's ability to selectively etch away different materials.

In order to fix short circuits which were embedded in the parylene flex itself, the top parylene must be etched away first to expose the metals underneath. After the metals were exposed, the power of the laser can be fine tuned to slowly cut the shorted metal in order not to damage the bottom layer parylene which might retain as much of the original structure as possible. An additional coating of parylene needed to be done after this process to protect the etched area as an insulation layer. This step can also prevent the soaking failure after implantation inside subject's body. This process was shown in Figure 2.12 (Right).

Another possibility that the shortage underneath the parylene flex due to low viscosity during squeegee process can also be fixed with this laser cutting method. Shown in Figure 2.13 (Left), the conductive epoxy overflowed underneath the parylene film and shorted the neighboring metal pads even though there is no shortage on the top surface of the parylene flex. Ultraviolet (UV) laser can thus be used to cut through the film first and etch away the shorted conductive epoxy underneath, as shown in Figure 2.13 (Right). Conduction test showed that the shorted neighboring pads can be successfully separated electrically with this UV laser cutting process.

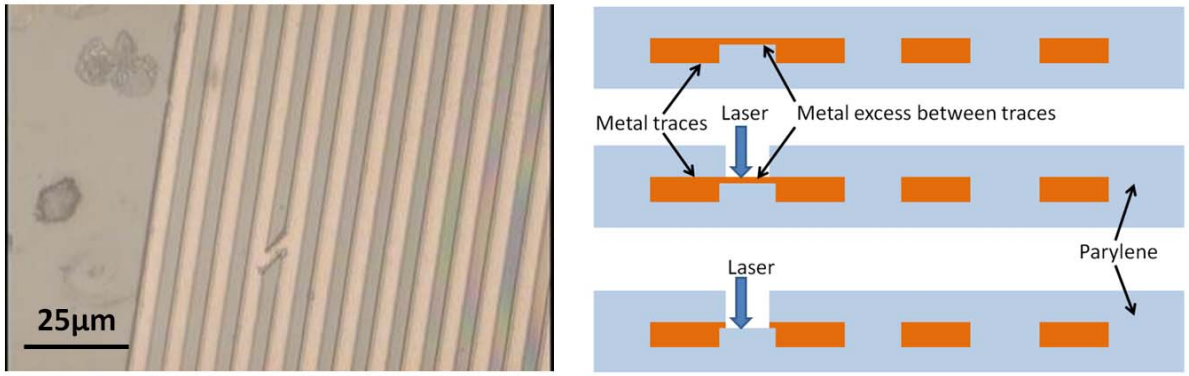

Figure 2.12. (Left) Short circuit defect on dense metal lines. (Right) Short circuit defect repair process.

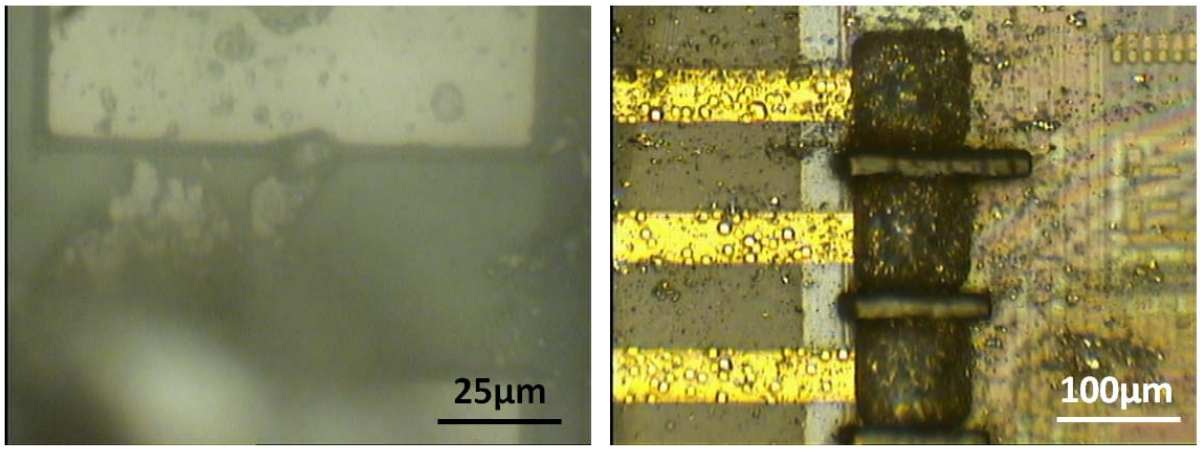

Figure 2.13. (Left) Shortage of neighboring metal pads underneath the parylene film due to low viscosity of the conductive epoxy. (Right) Electrically isolate the neighboring pads after UV laser cleaning.

2.4.4 Device Testing

In order to measure the connection yield, a high-density multi-channel dummy chip was first fixed inside the PDMS mold, aligned with the parylene flex under microscope with around 10µm resolution, bonded by conductive epoxy squeegee process, and cured to test the functionality of the system, as shown in Figure 2.14 (Left). Result showed all the required bonding pads can be bonded in less than 1 minute after alignment. On average, less than 10 fixes, including both short circuits and open circuits (can be fixed by multiple squeegee process), were needed after each chip bonding. Almost 100% of the pads were functional after this repairing process. This resulted in a connection yield higher than 96% before repairing and almost 100% after repair process, as shown in Figure 2.14 (Right).

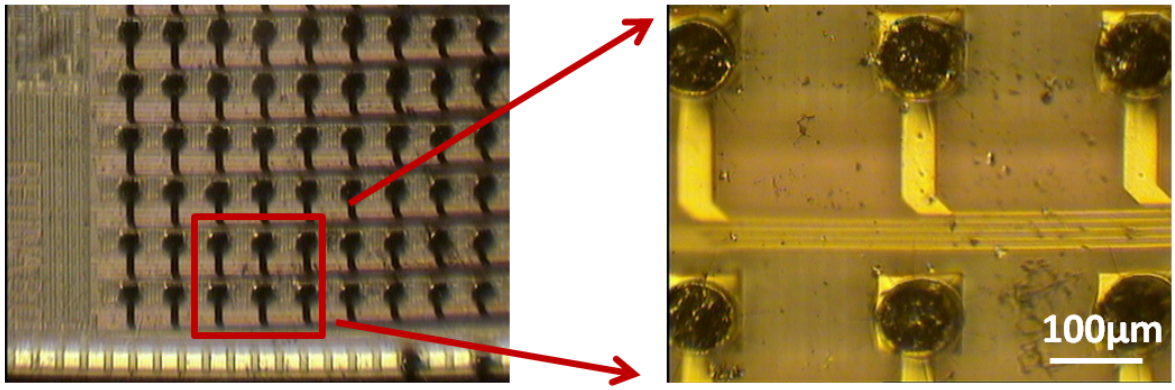

Figure 2.14. (Left) Dummy chip integration with squeegee technique. (Right) On average, less than 10 fixes for short and open circuits are needed after each chip bonding. 100% of the pads are functional after these repairs.

2.5 Adhesion-Enhancement Surface Treatment

2.5.1 DEVICE DESIGN AND FABRICATION

500-µm-thick single-side polished silicon wafers were used in this experiment. Figure 2.15. showed the process steps of different treatments for parylene-to-silicon and parylene-to-parylene interfaces. Samples without any treatment and samples cleaned by diluted HF were also fabricated as comparison controls. Then, all investigated interface treatments were done on freshly HF-cleaned silicon or parylene-C surfaces. Buffer HF treatment was done by dipping with 30 seconds in the container. Hexane, toluene, and P.C. treatments were carried out by spinning chemicals onto the wafer. The recipe for CF_4 plasma was 400 Watt, 200 mtorr, and 15 minutes in a plasma etcher.

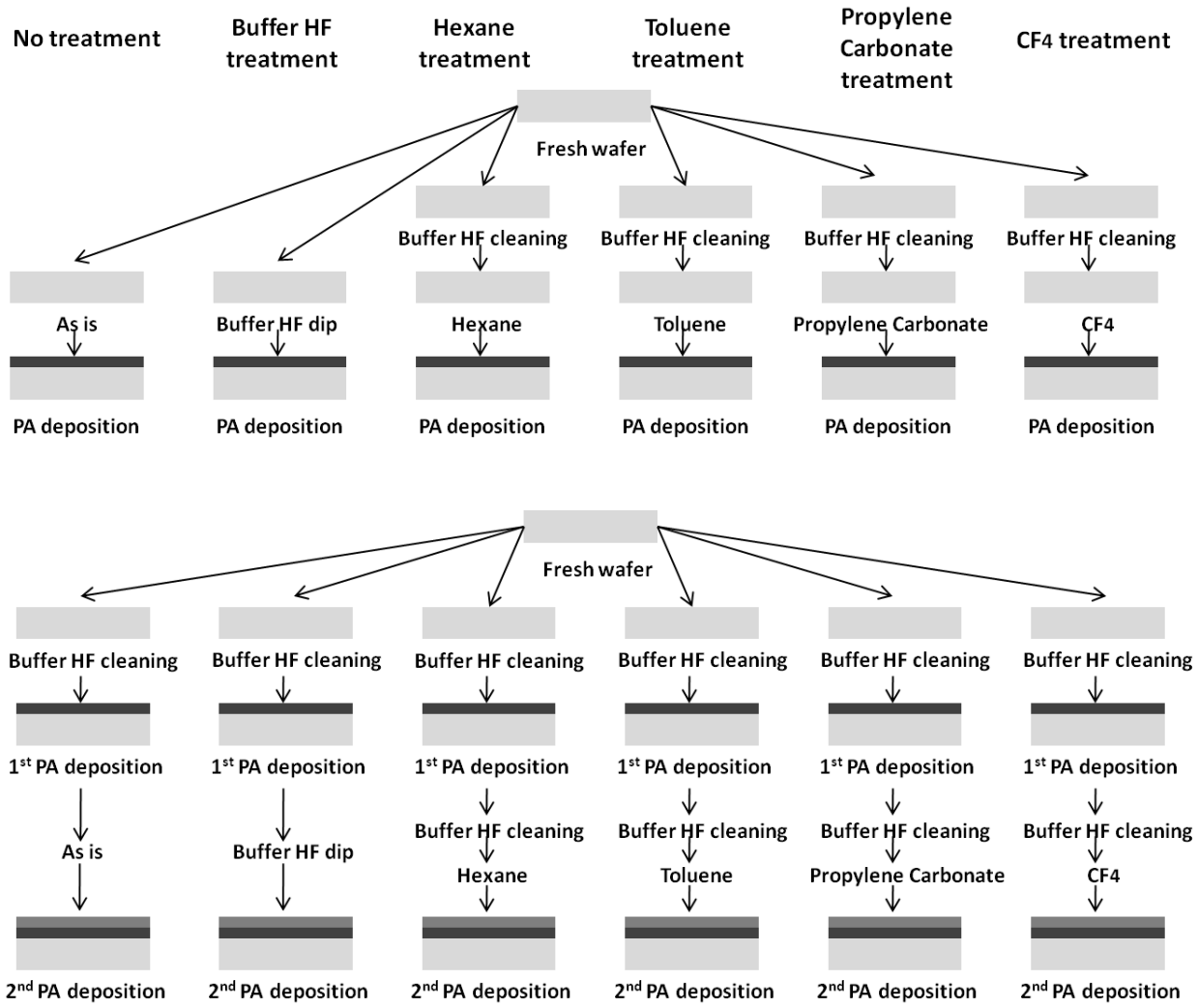

Figure 2.15. Process steps of different treatments: (Top) treatment for interface of silicon and parylene. (Bottom) Treatment for interface of parylene and parylene.

We designed two layouts to accommodate the different types of adhesion tests. Figure 2.16 showed the structure of the samples for peeling test experiment. The thickness of the top parylene is 10μm since this thickness of parylene is easy to handle in peeling test and the bottom layer is 5μm that is simpler to etch. Figure 2.17 illustrated the samples for soaking test experiment. The top parylene is 5μm since the soaking undercut and VABD were expected to be faster to be observed on

thinner deposited parylene. The bottom is 10μm to make sure we get the desired interface easily. O_2 plasma was used to etch the trench to get the desired interface in RIE. After the devices were fabricated and diced, the 2-μm-thick sacrificial photoresist was released in acetone, resulting in the partial-peeled parylene film, which facilitated the peeling tests later on, as shown in Figure 2.18.

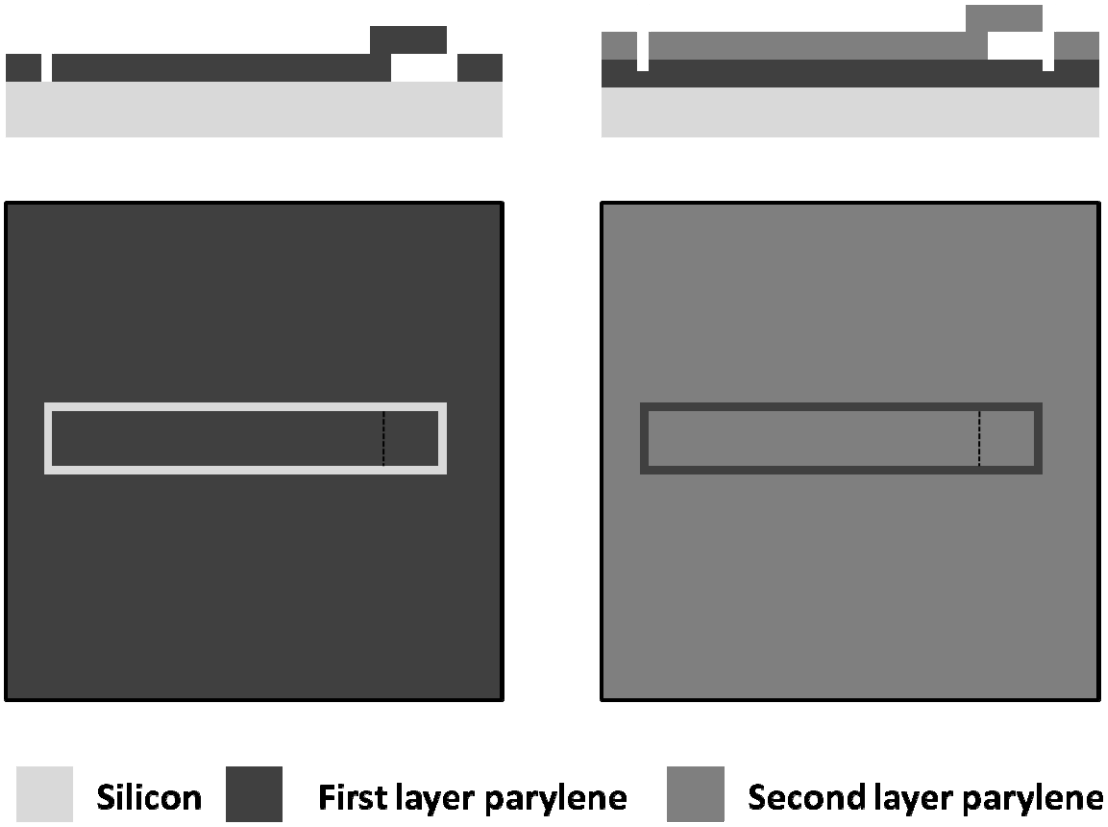

Figure 2.16. Sample layouts for peeling tests. (Left) Peeling test between parylene and silicon. (Right) Peeling test between parylene and parylene.

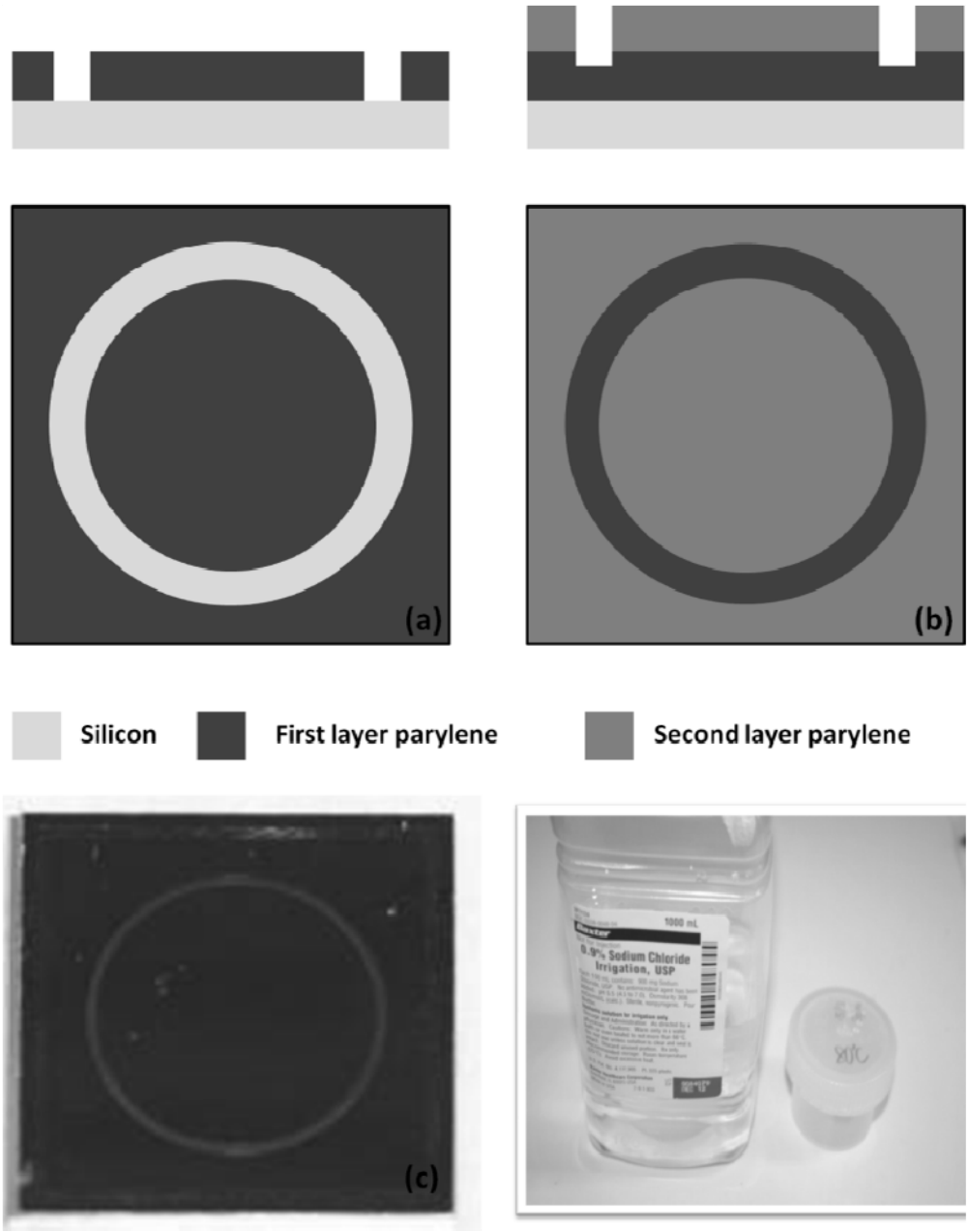

Figure 2.17: Sample layouts for soaking tests (a) between parylene and silicon and (b) between parylene and parylene. (c) Fabricated sample for soaking test. (Bottom right) 0.9 wt% NaCl solution.

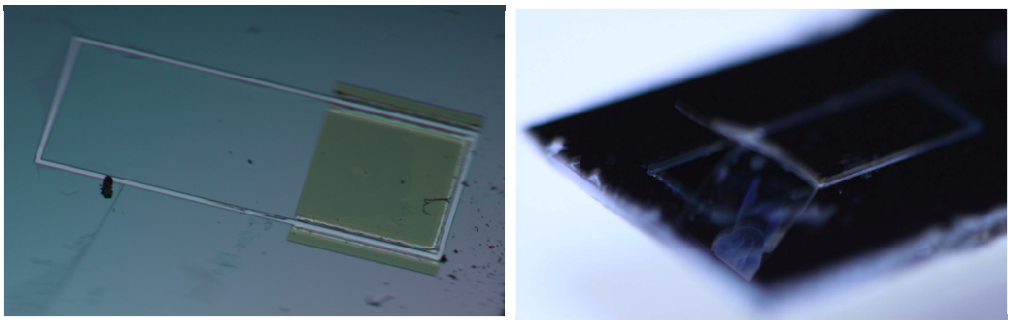

Figure 2.18. (Left) Fabricated sample with sacrificial PR for peeling test. (Right) Partially released film at initial condition for peeling test after PR releasing.

2.5.2 EXPERIMENTS AND RESULTS

2.5.2.1 Peeling Test

Figure 2.19 (a) showed the setup of peeling test. A force gauge (CHECKLINE) was fixed on a motorized stage. The partially released film was pulled at 90 degree with a speed of 100 μm/s. Data were collected and analyzed by a computerized data acquisition program. Figure 2.19 (b) showed the time v.s. force plot of a parylene film being pulled off from substrates. Section A is the elastic part of the pulling process, where section B represents the occurrence of rupture and section C represents the residual constant force. The maximum forces achieved were recorded in Table 2.1 and it can occur either just before the film started to peel away from the substrate or just before it was torn. Figures 2.19 (c) and (d) showed the SEM images of the peeled interfaces, where the parylene-to-parylene interface is much rougher than that of the parylene-to-silicon interface. Peeling test results showed that the P.C. treated samples require the maximum peeling forces among all samples, and the annealing degrades the peeling force for almost all parylene-to-silicon samples while it enhances the force for all parylene-to-parylene samples. This degradation of the force between silicon and parylene was believed to come from the removal of physically absorbed water in silicon at the annealing temperature (200°C), which leaves hydroxyl groups in contact with the parylene film [21].

The annealing at 200°C is above the glass transition temperature of parylene-C, where recrystallization and intermolecular mixing in parylene greatly enhance the adhesion force.

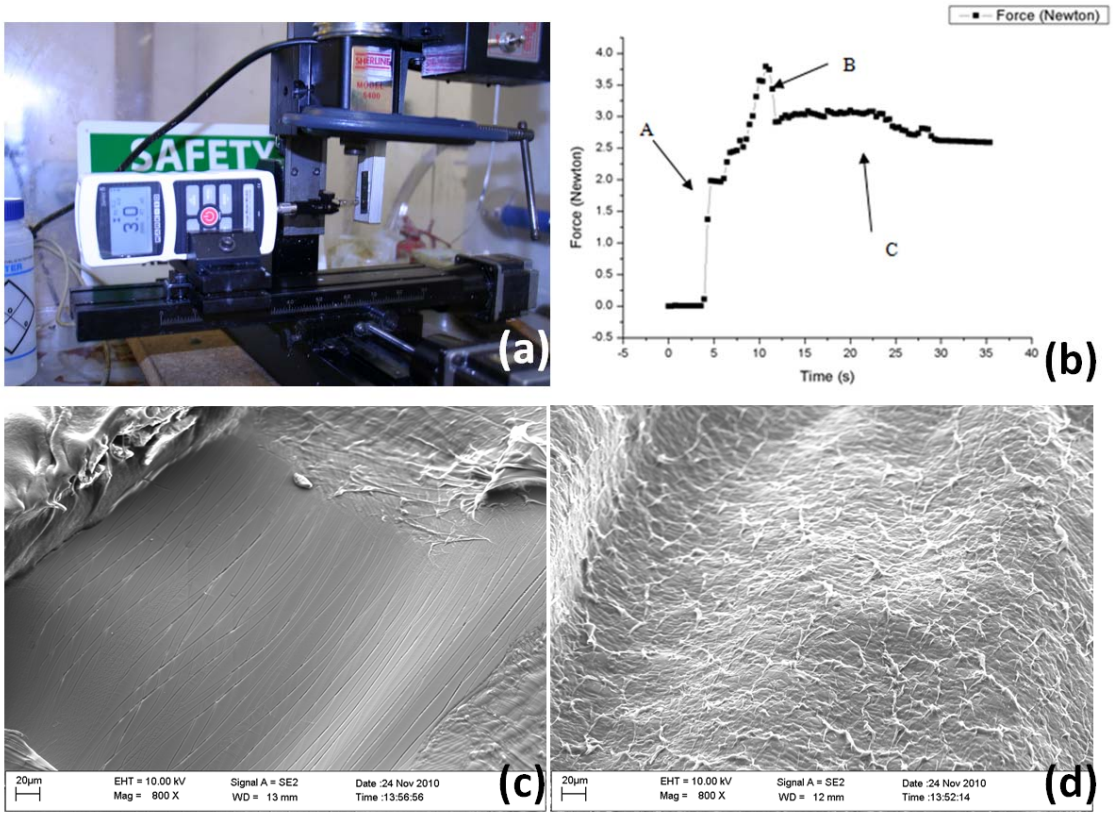

Figure 2.19. (a) Setup of peeling test. (b) Time v.s. Force plot of a parylene film being pulled away from the substrate. SEM of the peeled interface of (c) parylene-silicon and (d) parylene-parylene.

Table 2.1. Maximum force readings of the peeling test (n=5)

	Silicon-Parylene			Parylene-Parylene		
Treatment	Annealed	Force (mN)	Tear?	Annealed	Force (mN)	Tear?
No	No	178±32	No	No	476±19	Yes
No	Yes	165±27	No	Yes	≥1500	Yes
HF	No	730±72	Yes	No	591±43	Yes
HF	Yes	436±43	Yes	Yes	≥1500	Yes
Hexane	No	720±58	Yes	No	631±45	Yes
Hexane	Yes	546±27	Yes	Yes	≥1500	Yes
Toluene	No	752±44	Yes	No	675±38	Yes
Toluene	Yes	515±18	Yes	Yes	≥1500	Yes
P.C.	No	892±41	Yes	No	1032±73	Yes
P.C.	Yes	658±38	Yes	Yes	≥1500	Yes
CF_4	No	214±16	No	No	854±27	Yes
CF_4	Yes	192±21	No	Yes	≥1500	Yes

2.5.2.2 Soaking Test

In the accelerated soaking test experiments, samples were immersed in 70°C, 80°C, and 90°C saline, as shown in Figure 2.20, acetone, and ST-22 to simulate device fabrication processes including life time test, metal lift-off, and sacrificial photoresist releasing. Daily observation on the undercut rate of the interface and VABD was done to examine the effects of adhesion enhancement. The Mean-Time-to-Failure (MTTF) of the adhesion for the parylene coated device can be calculated by these data. The Arrhenius model was used to extrapolate the MTTF at body temperature [22] by taking MTTF at two data points at a higher temperature. The equation of the relationship at a given system temperature T (in Kelvin) is expressed by:

$$MTTF = A exp(-E_a/KT) \qquad [2\text{-}1]$$

where A is the pre-exponential constant, E_a is the activation energy of failures (in eV), and k is the Boltzmann's constant (8.62×10^{-5} eV–K^{-1}).

In saline, both the undercut rate and VABD showed that the hexane and toluene treated samples have better effects on the parylene-to-silicon interface, while P.C. and CF_4 treatments compare favorably to others on the parylene-to-parylene adhesion for non-annealed samples, as shown in Table 2.2. As for the thermal effect, we baked the samples in a vacuum oven at 200°C to simulate the thermal condition during fabrication process including photoresist backing, metal deposition, lift-off in hot solution, and plasma dry etching. The results showed that the annealing dramatically increased the undercut rate, which suggests that the adhesion on all samples were reduced but the appearance of bubbles were prevented as expected.

In ST-22, both parameters implied that hexane, toluene and P.C. treated samples provided better adhesion enhancement on both the parylene-to-silicon and the parylene-to-parylene interfaces. The

results also showed that annealing increased the undercut rate as well but failed to reduce bubble density as ST-22 was able to penetrate parylene films regardless of the treatments.

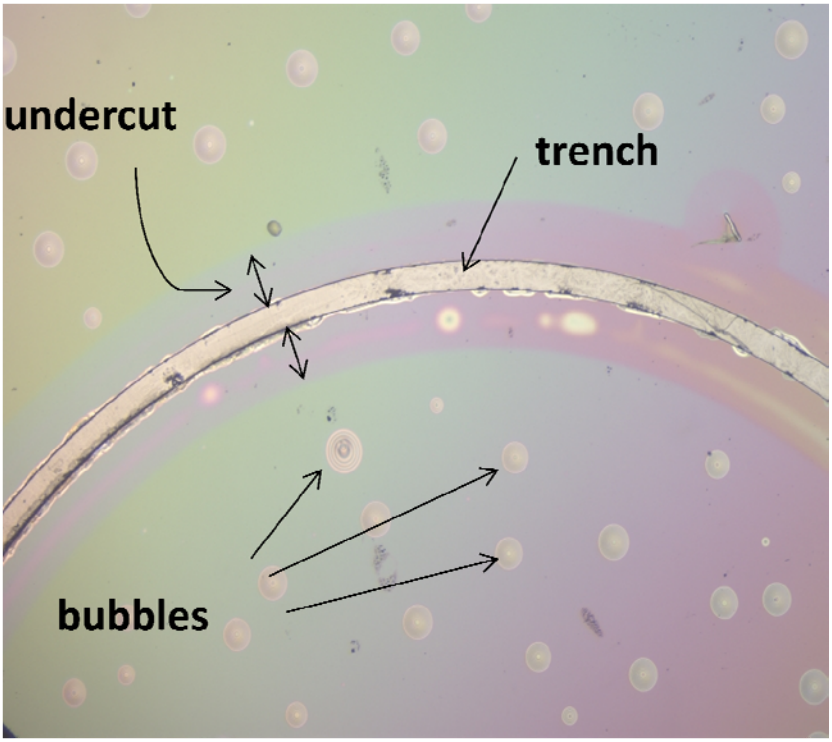

Figure 2.20. Undercut and vertical attack bubbles after soaking in saline (0.9 wt% NaCl solution)and ST-22. The trench is 200μm.

Table 2.2. Soaking tests (n=5) to observe undercut and vertical attack bubble density (V.A.B.D.)

	Silicon-Parylene				Parylene-parylene			
Treatment	Annealed	Soaked in	Undercut (μm/day)	V.A.B.D. (/mm^2·day)	Annealed	Soaked in	Undercut (μm/day)	V.A.B.D. (/mm^2·day)
No	No	Saline	>50	1.29±0.57	No	Saline	0.70±0.25	0.45±0.07
No	Yes	Saline	>50	~0	Yes	Saline	16.66±2.18	~0

HF	No	Saline	0.65±0.08	0.45±0.22	No	Saline	0.55±0.09	0.68±0.09
HF	Yes	Saline	8.45±1.72	~0	Yes	Saline	31.32±3.81	~0
Hexane	No	Saline	0.34±0.07	0.34±0.11	No	Saline	0.18±0.03	0.21±0.03
Hexane	Yes	Saline	3.01±0.93	~0	Yes	Saline	19.44±3.27	~0
Toluene	No	Saline	0.41±0.08	0.11±0.02	No	Saline	0.21±0.04	0.23±0.03
Toluene	Yes	Saline	6.02±0.87	~0	Yes	Saline	22.35±2.98	~0
P.C.	No	Saline	1.92±0.34	0.23±0.10	No	Saline	0.14±0.04	~0
P.C.	Yes	Saline	15.66±2.16	~0	Yes	Saline	35.29±5.76	~0
CF_4	No	Saline	>50	1.32±0.47	No	Saline	0.17±0.05	6.36±1.17
CF_4	Yes	Saline	>50	~0	Yes	Saline	17.77±2.54	~0
No	No	ST22	28.76±7.95	46±8	No	ST22	15.06±3.11	137±48
No	Yes	ST22	16.67±6.16	88±13	Yes	ST22	12.50±3.77	75±8
HF	No	ST22	2.81±0.66	108±16	No	ST22	6.02±0.76	29±3
HF	Yes	ST22	9.04±1.75	98±21	Yes	ST22	27.17±5.91	75±23
Hexane	No	ST22	2.27±0.81	71±22	No	ST22	5.03±1.08	29±6
Hexane	Yes	ST22	18.12±3.79	112±25	Yes	ST22	17.16±2.98	57±11
Toluene	No	ST22	3.75±0.73	100±17	No	ST22	4.02±1.21	25±6
Toluene	Yes	ST22	15.06±4.71	137±19	Yes	ST22	11.53±3.04	72±0.11
P.C.	No	ST22	1.99±0.47	12±3	No	ST22	3.01±0.61	29±5
P.C.	Yes	ST22	6.41±1.23	37±8	Yes	ST22	21.08±3.49	63±16
CF_4	No	ST22	11.75±2.51	152±41	No	ST22	10.04±2.11	178±34
CF_4	Yes	ST22	24.76±6.32	113±39	Yes	ST22	25.86±4.78	125±41

2.6 Dry Mechanical Liftoff Technology

Parylene-C, a biocompatible material, was selected as the main structure and packaging material in neural interface devices because of its many favorable properties [23]. The parylene-metal-parylene sandwich skin structures which consist of one metal layer between two parylene layers were also largely utilized in our retinal implant application [24]. Due to the limit of the size of the cut on eyeball, line width of less than 10μm was often needed to be achieved in our application. The standard metal line etching process, however, was greatly affected by the isotropic etching time and the metal etching solution, which means thin metal lines are very easily to be etched away and the maximum achievable resolution becomes difficult to control. On the other hand, lift-off process is an alternative to metal etching. Unlike metal etching process where the metal was deposited before the lithography step, lift-off process required the lithography steps to be taken before the metal deposition so the metals can be deposited in the "trenches" to achieve very high resolution metal lines. In addition to the regular photoresist used in the standard lithography process, a special photoresist for liftoff purpose: Lift-off Resist (LOR) was also developed by Microchem Corp. (Newton, MA, USA) [25].

However, it was found that patterning metal features by classical metal liftoff process on bottom parylene-C layer is still a time-consuming and difficult process. Besides, some residues of metal particles, causing by particles left on substrates during photoresist spinning, can be easily observed after liftoff process which might cause unwanted short circuits between metal lines. In addition, scratch and cracks, causing by cotton rods used to help remove metal residues during liftoff process, also happened on metals which might affect the electrical properties of the entire devices, as shown in Figure 2. 21.

Here, we proposed a new method to pattern metals directly on parylene-C film by mechanical lift-off using SU-8 sacrificial masks. The estimated process time of this method was less than half of the time compared to classical metal lift-off process. Most importantly, it is a dry process without soaking parylene-C film in acetone or high temperature photoresist stripper (ST-22) for a long time

(~4 hours), as shown in Table 2.3, which will prevent delamination and increase lifetime of parylene devices as well [26]. Features from 10μm to 300μm in diameter and width were successfully patterned on parylene-C film by this method. Smaller feature sizes can also be achieved by high-resolution masks. Metal lines with testing pads from 10μm to 100μm wide and 1cm long were also fabricated and tested to evaluate their resistances. The results showed that there was almost no observable difference in resistance among theoretical values, metals patterned by classical lift-off, and metals patterned by our proposed dry mechanical lift-off process, which validates the feasibility of this method to be applied to pattern metals on parylene-C films.

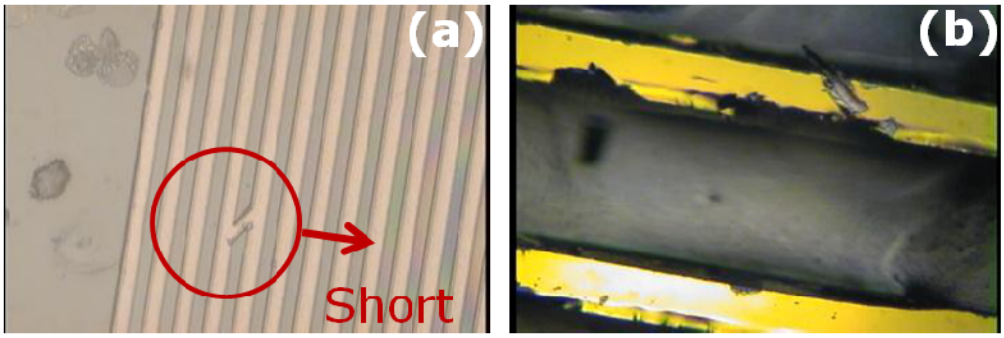

Figure 2.21. (a) Particles left on parylene-C substrate during liftoff photoresist spinning will cause the unwanted short circuits between two metal lines. (b) Cotton rods were often used during classical metal liftoff process to help remove the metal residues which will easily damage the metal surfaces to affect the electrical properties.

Table 2.3. The estimated time of the wet process

Solution	Acetone	ST-22	Total
Time	~2hr	~2hr	>4hr

Motivation

During our parylene-C device process, patterning metals on parylene-C film was found to take the most of the time in the whole process. Besides, many defects on metal patterns can also be found after this long process. We were thinking a way to solve those problems: if we can pre-pattern a mask on parylene-C film before metal deposition and peel off this sacrificial mask afterward, all these problems can be solved. However, the requirement on this mask is: 1. to have desired adhesion to parylene-C film, (e.g. not too strong or too weak), 2. easy to be patterned by photolithography process, 3. and the features of less than 10 μm can be achieved.

Therefore, several tested samples were designed and tested in high temperature saline solution to examine their adhesion to parylene-C films by daily undercut observation to find out the best materials to be sacrificial masks.

2.6.1 Design of Soaking Samples

Figure 2.22 showed the basic structure of the soaking samples. Uniform trenches were developed away by developing solution or etched away by O_2 plasma. The width of trenches was carefully measured by P15 surface profiler which was served as the reference to calculate the undercut rates. Different interface treatments were done on the interfaces between parylene-C films and the coated masks to examine the adhesion affected by the treatments.

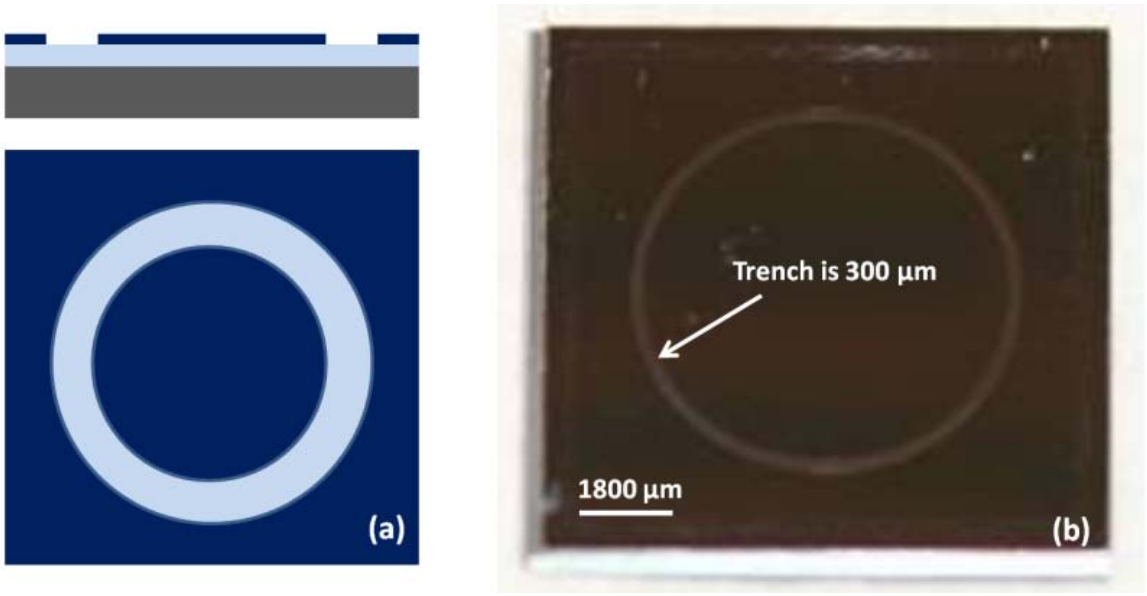

Figure 2.22. (a) Sample layout for soaking test. (b) Real fabricated device with 300µm trench.

2.6.2 Examination of Undercut Rates

Figure 2.23 showed the soaking results. The saline solution can go inside the interface uniformly between parylene-C films and the coated masks to form the so called “undercut” for us to examine the adhesion. Undercut was observed under microscope and images were taken to be precisely calculated .

SU-8, a negative photoresist, can have strong adhesion to parylene-C film after hard bake at 120°C [27]. However, soaking tests, as shown in Table 2.4, showed that the adhesion between SU-8 and parylene-C film decreased a lot without hard bake. Besides, SU-8 can be easily patterned by photolithography on parylene-C film with features of sizes less than 10 µm. Therefore, this kind of SU-8 satisfies all the requirements of our desired masks and hence can serve as sacrificial masks for metallization on parylene-C film.

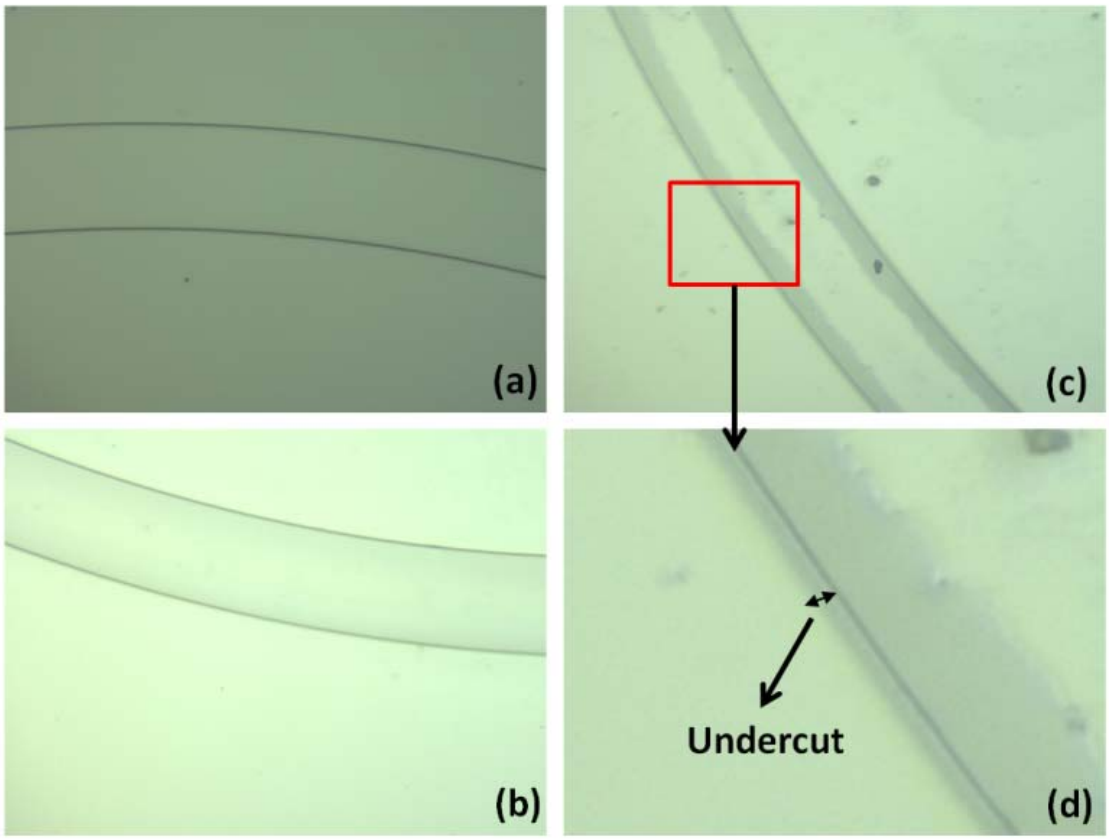

Figure 2.23. (a) Trench of the initial soaking device (0 days). (b) Trench of the soaking device with hard-bake after 7 days. (c) Trench of the soaking device with micro-90 detergent treatment after 7 days. (d) Close-up view of (c); undercut can be easily observed.

Table 2.4. Undercut rate of the samples soaked in high temperature saline by different interface treatments (μm/day)

Treatment	Hard-bake	No treatment	Micro-90 detergent
Undercut	~0	12.85	12.48

2.6.3 Fabrication Process

As shown in Figure 2.24, our fabrication process started with SU-8 spin coating on parylene-C films, followed by pre-bake at 65°C. The samples were then exposed by UV light to pattern the desired features. Next, samples were post-bake at 95°C before developing the uncross-linked SU-8. Ultrasonic bath was also used to accelerate the developing process. After metal deposition (Ti/Au) by E-beam, the sacrificial SU-8 masks were peeled off from parylene-C films to complete the whole dry mechanical lift-off process.

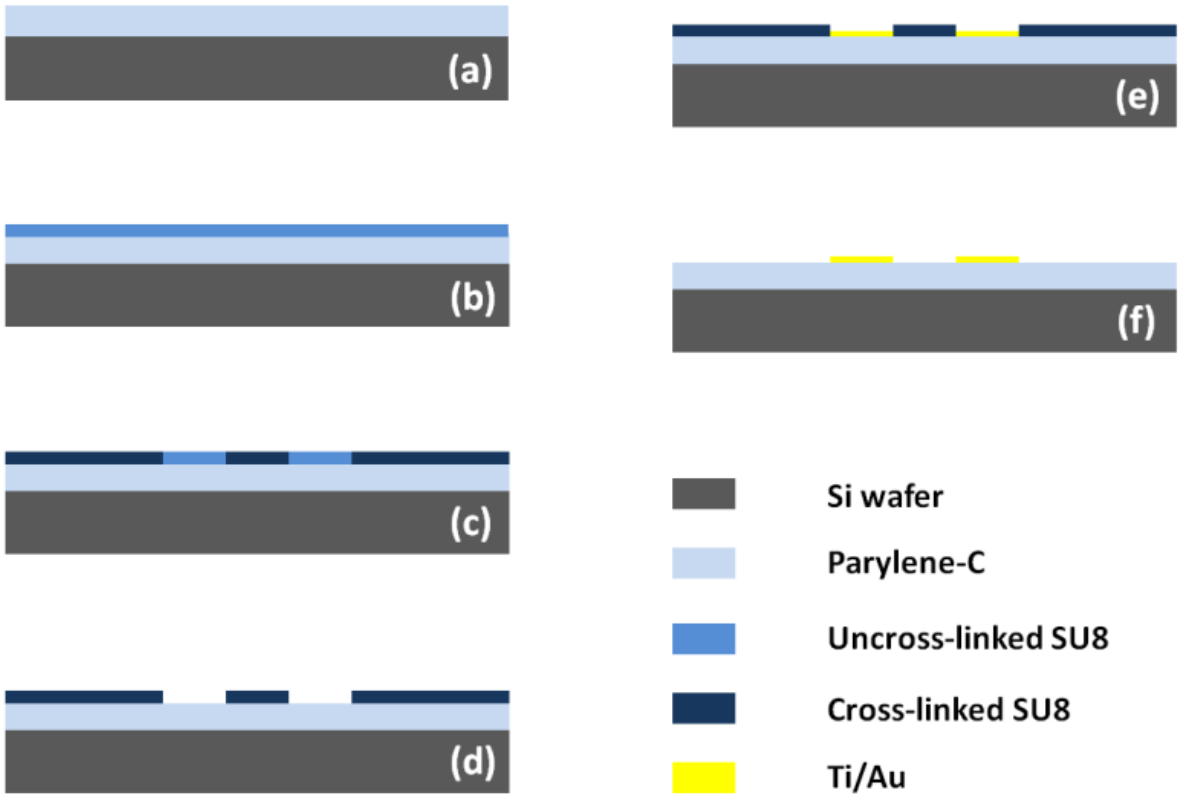

Figure 2.24. Fabrication process of the direct metallization on parylene-C film by sacrificial SU-8 masks. (a) Deposit parylene-C film on silicon wafer, (b) spin coat SU-8 with desired thickness on parylene-C film, followed by pre-soft bake, (c) expose by UV light and post bake, (d) develop the uncross-linked SU-8, (e) metal (Ti/Au)deposition by E-beam, and (f) peel off SU-8 mask.

As shown in Figure 2.25, experiments showed that thinner SU-8 layer (~15μm) can easily be peeled from parylene-C substrates by tweezers in seconds before and after metal deposition because of its flexibility. In addition, there were almost no visible residues or damages left on parylene-C films after dry peeling process.

Features with sizes of as small as 10 μm in diameter and width can also be fabricated on parylene-C film, as shown in Figure 2.26. The smaller feature sizes can also be achieved by high-resolution masks. It was noted that the sacrificial SU-8 masks became more brittle after metal deposition which might be easily broken and hence needs to be more careful to implement the peeling process. In addition, metal lines with different widths were also patterned on parylene-C film, as shown in Figure 2.27, to compare to the resistances of the metal lines formed by different methods.

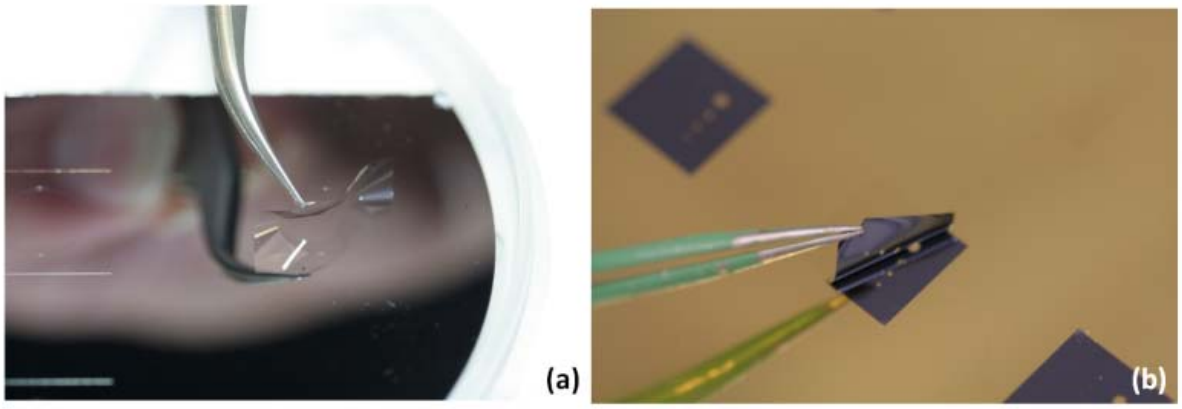

Figure 2.25. (a) 15μm thick SU-8 is highly flexible. (b) After metal deposition, sacrificial SU-8 mask can be easily peeled off by tweezers in seconds, and no visible residues were observed.

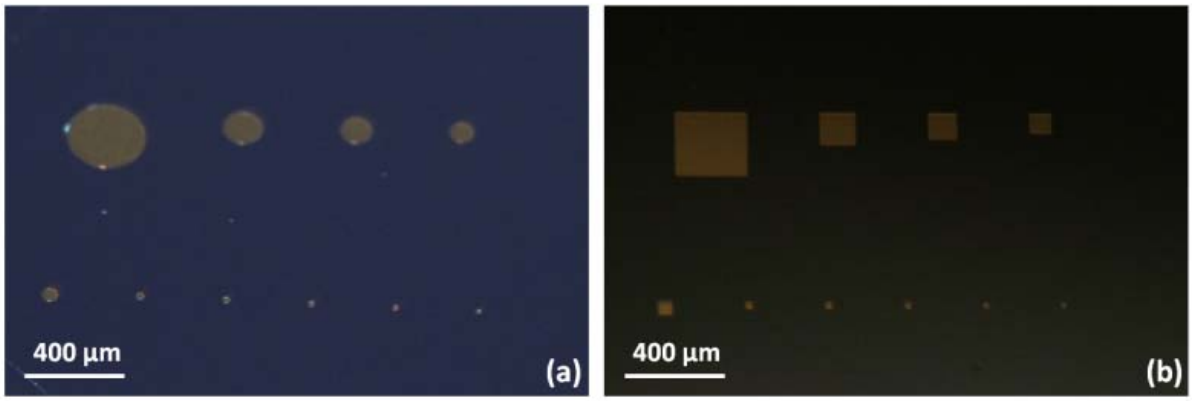

Figure 2.26. (a) Circles from 10µm to 300µm in diameter can be fabricated on parylene-C film by sacrificial SU-8 masks. (b) Squares from 10µm to 300µm in side length can also be fabricated on parylene-C film.

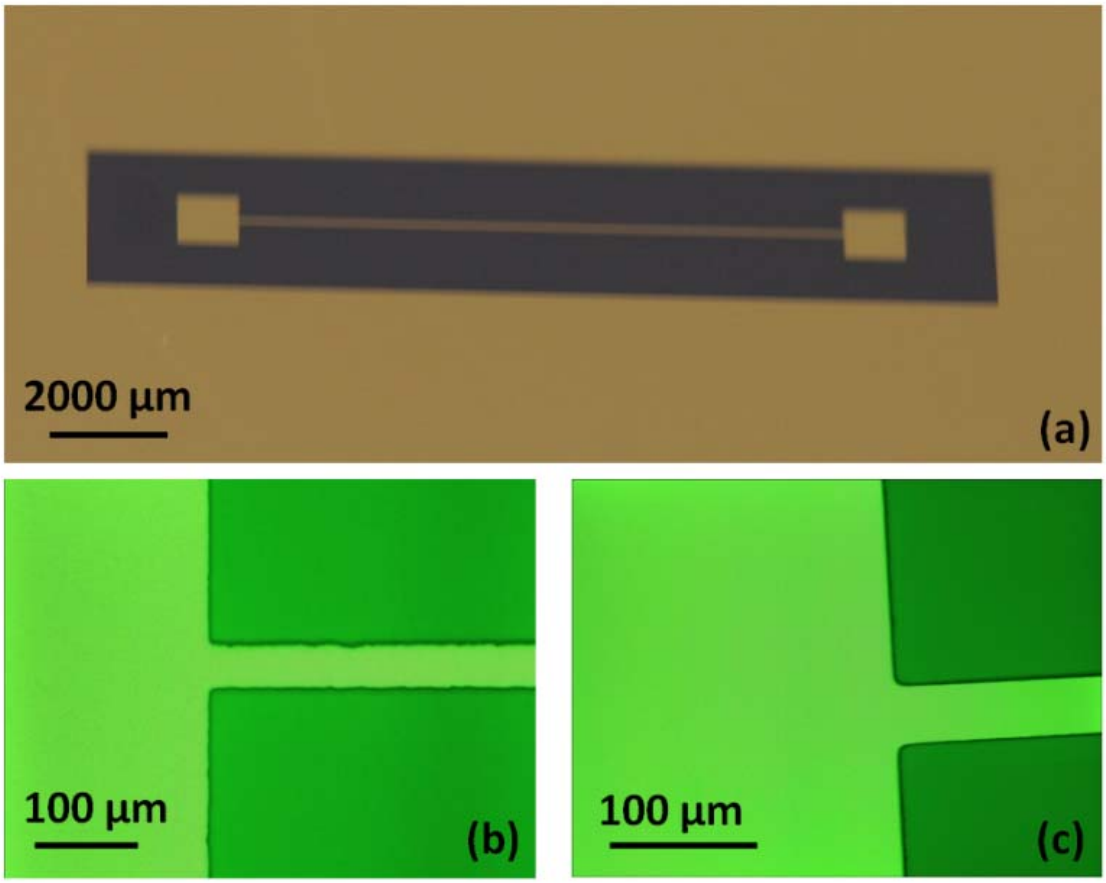

Figure 2.27: (a) Image of 1cm long and 40μm wide metal line along with two metal pads. (b) Microscopic image of the pattern fabricated by liftoff process. (c) Microscopic image of the pattern fabricated by sacrificial SU-8 masks.

2.6.4 Discussion

For the different metal pattern techniques, in addition to the time, the most important parameters are the smallest feature sizes and the resistances of the patterned metals.

2.6.4.1 SU-8 Thickness

SU-8 masks with different thicknesses were tried on parylene-C films to compare the easiness of removal from parylene-C films after metal deposition. It was found that thicker SU-8 masks are much stronger after metal deposition compared to the thinner ones. However, there were observable residues and even damages left on parylene-C films for these thicker SU-8 masks after peeling process which is totally not desirable. Therefore, even extra care was needed to be paid on the peeling process, thinner SU-8 masks of around 15 μm were still chosen to be applied on this dry mechanical lift-off process.

2.6.4.2 Smallest Feature

For our dry mechanical lift-off process, the smallest feature size only depends on the smallest feature size that SU-8 can be achieved. Theoretically, features as small as less than 10 μm can be achieved by high-resolution masks which are good enough for MEMS application.

2.6.4.3 Comparison of Resistance

Metal lines with different widths from 10 μm to 100 μm and 1 cm long were patterned on parylene-C substrate to compare to the resistances of the metal lines formed by different methods. The theoretical electrical resistance of a wire was calculated by:

$$R = \rho L/A = L/\sigma A \qquad [2\text{-}2]$$

where ρ is resistivity, σ is conductivity, L is the length of the wire, and A is the cross sectional area of the wire.

In our case, the metal structure was Ti (20nm) and Au (230nm) and we used the resistivity of Au (22.14 nΩ/m@20°C [28]) to represent metals to simplify the calculation. As shown in Figure 2.28, there were almost no observable differences in resistance among the theoretical value of metals, metals patterned by classical wet chemical lift-off process, and metals patterned by our dry mechanical lift-off process.

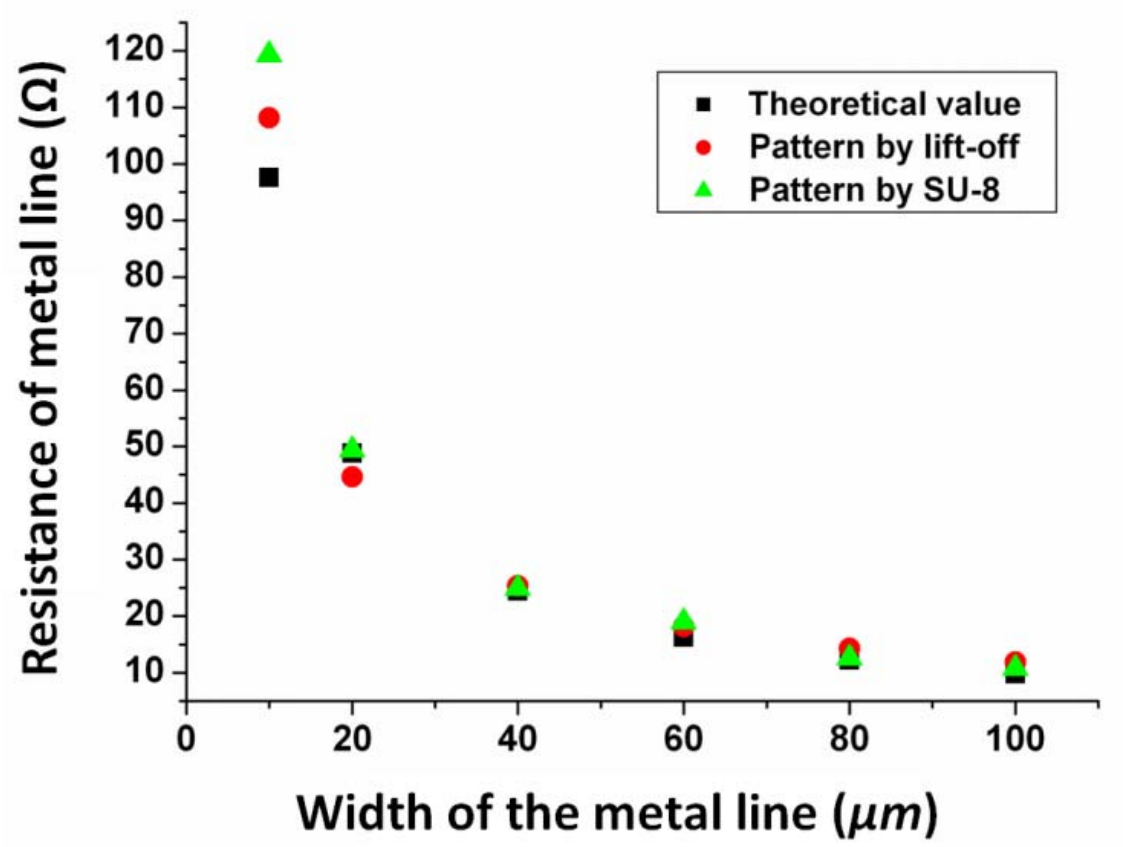

Figure 2.28. Comparison of the resistance of the metal lines patterned by different methods.

2.7 Summary

In this chapter, the overall requirements for device packaging were first introduced and discussed. The first and second generations of parylene flex were designed and fabricated. Then, a flexible parylene flex chip integration technology has been successfully demonstrated by integrating high-density multi-channel retinal dummy chips. Much effort has been put to optimize the fabrication process of parylene flex and integration technology for high-density multi-channel IC chips to achieve a fully functional system. This chapter also presented several techniques to either solve or alleviate some of these fabrication and integration issues. These include a high-density squeegee technique for multi-channel metal pad bonding, screen printing, SU8 layer to increase aspect ratio of the bonding well, short circuit and open circuit repairment using laser ablation, and a PDMS holder to house the IC chip and further extend the squeegee area during bonding process. It is believed that this new technique can be further improved to achieve 10,000 connections within an area of 1 cm^2.

Besides, several chemical and plasma treatments to enhance the adhesion between parylene-C to silicon and parylene-C to parylene-C were also investigated to study their effectiveness on adhesion promotion. We also simulated the possible conditions that happen frequently during fabrication process by soaking samples in saline, acetone, and ST-22. Parameters including peeling force, undercut rate, and VABD were used to quantify the effects on these adhesion enhancements. P.C. was proved to provide the best results in peeling test while hexane, toluene, and P.C. showed better effects in soaking test. The thermal effect will degrade the peeling force for all parylene-to-silicon samples but enhance the force for all parylene-to-parylene samples. Annealing can reduce the adhesion but help prevent the vertical attack bubbles. In summary, P.C. is the most promising chemical to enhance adhesion on both interfaces from our results.

In addition, we presented a new fabrication method to replace classical wet chemical lift-off by employing dry mechanical lift-off of SU-8 mask to pattern metals on parylene-C film. This kind of

SU-8 without hard bake process had proper adhesion to parylene-C films, and was easily to be patterned with small feature sizes by photolithography. Sacrificial SU-8 masks with different thicknesses were tested in order to find out the best trade-off between the feature sizes and the easiness of removal from paryelene-C film after metal deposition. The 15 μm thick SU-8 liftoff mask was found to be highly flexible and can be peeled off mechanically from parylene-C film by tweezers in seconds without any visible residues. Features from 10 μm to 300 μm in diameter and width were successfully patterned on parylene-C film by this method. Metal lines with testing pads from 10 μm to 100 μm wide and 1 cm long were also fabricated and tested to evaluate their resistances. The results showed that metals of small feature sizes (< 10 μm) and similar resistances can be patterned on parylene-C directly by our proposed SU-8 mechanical lift-off method. This new technique provided an alternative way to pattern metals on parylene-C film which benefits the application in MEMS area.

In summary, we proposed the techniques to optimize the parylene flex by enhancing adhesion between each layer and creating reliable metal layers embedded in parylene flex. We also described how to build a high-density multi-channel chip integration technology with high yield and integration of dummy chips with parylene flex was applied to demonstrate its effectiveness.

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3 PHOTO-PATTERNABLE ADHESIVES AND THEIR APPLICATIONS

3.1 Introduction

Although high-density multi-channel chip connection can be achieved by conductive epoxy squeegee technique developed in Chapter 2, there are still many issues which needs to be solved. Firstly, there was no fixation between IC chip and parylene flex during squeegee process. Misalignment can easily happen when rubber squeegee was applied during the process. Secondly, short circuit problem caused by conductive epoxy overflowed underneath parylene flex can also easily happen. Thirdly, the PDMS mold to house the IC chip was too big to be implanted inside eyeball. Fourthly, the mechanical connection depended only on conductive epoxy which occupied less than 2% of the total area. Delamination can easily happen, and it is especially serious during surgery. Therefore, a more reliable technology needs to be developed to create a strong bonding between the parylene flex and the retinal IC chip, further enhancing the reliability of this technique.

Silicon wafer bonding has become an important processing technique in the packaging of MEMS field to build a multilayer 3D structure and encapsulation [1-2]. Generally, anodic bonding, glass frit bonding, and adhesive bonding are the three major branches of bonding techniques. Anodic bonding was reported to create hermetic and strong bonds between two contacted wafers by high temperature (150ºC~500ºC) and high electric field (200V~1500V) [3]. Glass frit bonding, which requires an inorganic melting glass layer as the intermediate bonding material, was also popular to form a reliable bonding with curing temperature between 400ºC and 1100ºC [4]. However, both anodic and glass frit bonding require special and expensive equipments. Besides, those harsh conditions, including high temperature and high electric field, cannot be applied to MEMS with polymer structures.

For low temperature bonding, however, adhesive bonding technique with photo-patternable characteristics is still attractive. This low-cost bonding technology, which uses polymer materials as the intermediate layers, requires relatively low processing temperature (lower than 200ºC) and has the high tolerance to surface topography. In addition, it also enables the selective wafer bonding by applying adhesives on designated areas.

Parylene-C, a biocompatible polymer with superior properties, has drawn more and more attention in bioMEMS fields recently. Adhesion enhancement for parylene-C deposition on silicon by physical and chemical treatments has been studied by our group [5-6]. However, the bonding between separate parylene-C sheet and silicon substrate remain the reliability issues. In this chapter, we studied a low-temperature adhesive bonding technique between parylene-C and silicon by photo-patternable adhesives. All the processing conditions, including bonding temperature, bonding pressure, bonding time, and surface treatments, were investigated and optimized. Epoxy-based SU-8 (a negative photoresist) and AZ-4620 (a positive photoresist) from Microchem Co were selected as the materials to demonstrate this technique because of their photo-patternability and ease of spin-coating. The ASTM peeling tests were applied on all samples under various bonding conditions to verify the bonding forces. This technique was also applied on high-density multi-channel chip integration for retinal implant as a demonstration.

3.2 Motivation

One of the biggest challenges that a prosthetic implant has to overcome is the reliable packaging of integrated circuit (IC) chips with bio-devices to stand corrosive body fluids when implanted. This is especially true for complex neural implants and retinal implants because hundreds of or thousands of electrodes may need to be connected to the necessary IC chips [7]. In comparison, a pacemaker has only one stimulating channel and a cochlear implants requires only 5 to 6 stimulating electrodes

to be able to regain hearing capabilities of an impaired patient [8]. In addition, in order to avoid possible infection and medical complications, it is desirable to have prosthetic devices completely inside a subject's body. This means that technologies for integration, connection and packaging of IC chips for high-lead-count implant devices are of high demand. We had previously shown that aligned electrical connection can be done between parylene-C interfaces and high density multi-channel chips by conductive epoxy squeegee technique [9], where a PDMS mold, as shown in Figure 3.1, was used to house the IC chips and serve as the safety squeegee buffer zone. However, it is too big to be implanted inside human eyeball (<1~2 cm^3). In addition, since the adhesion only relied on conductive epoxy contacting less than 2% of the total connection area, delamination could easily happen when even a small force was applied to the assembled devices. This was especially serious during surgery. Since the next generation intraocular retinal prosthetics require the whole device, including coils, electrodes, stimulation chip and other ASICs, to be fitted inside a human eyeball, the device must be further optimized both in terms of size and surgical complexity.

Here, then, we investigated a new chip packaging technique to improve the yield in two ways: (1) to enhance "gluing" area from 2% to 94% by reflowing photoresist in high temperature vacuum oven and (2) to cover the unnecessary pads for testing only to avoid shortage happening underneath parylene-C flex during conductive epoxy squeegee connection as well. In order to validate this technology, chips designed with 268 connections to mimic the real retinal IC chips under development were used for the measurement of connection yield. In addition, after squeegee connection and encapsulation by thick parylene-C coating, the connected chips have gone through accelerated soaking tests in high temperature saline solution. The results showed that this new technique combined with additional parylene-C coating does provide high connection yield and is a promising method for micro implant devices.

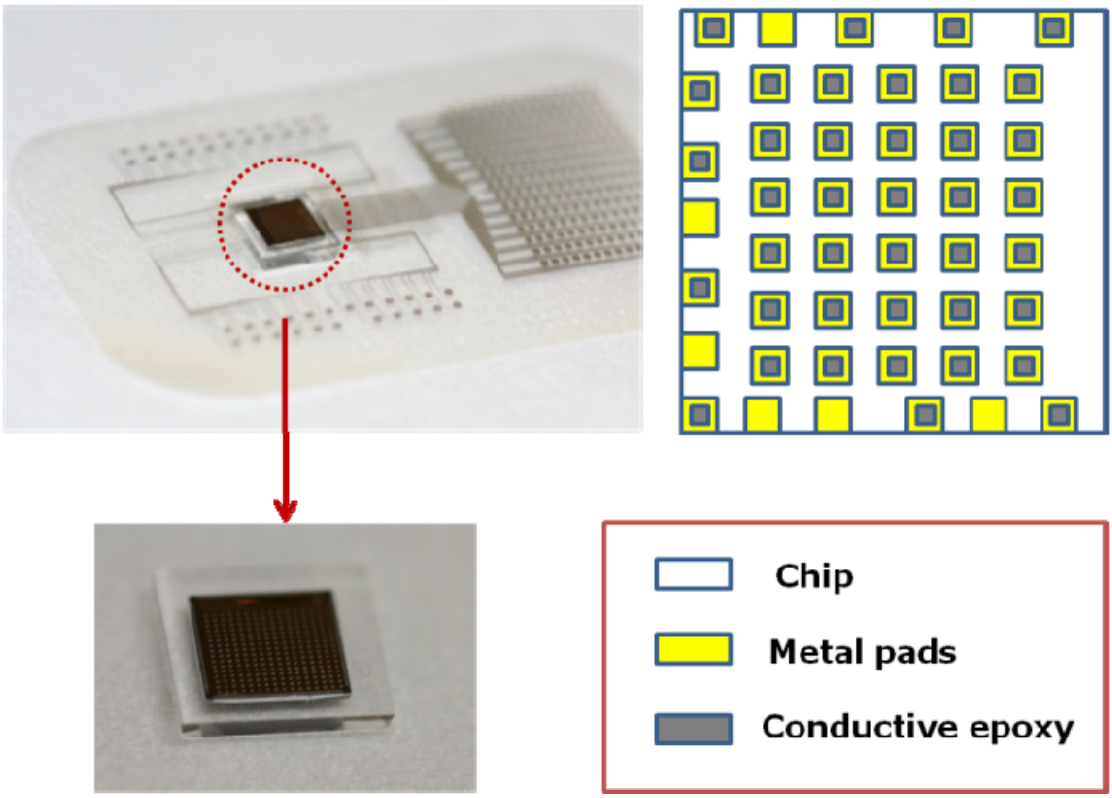


Figure 3.1. Former connection technology that requires an additional PDMS holder to house the IC chips; the adhesion between parylene-C and chips only relies on conductive epoxy, which occupies less than 2% of the total contacting area.

3.3 Investigation of photo-patternable adhesives

3.3.1 EXPERIMENTAL PROCEDURE AND SETUP

Single-side polished 4-inch wafer with 500 µm thickness was employed and cleaned. The photo–patternable adhesives were first spin-coated on silicon wafers with HMDS and oxygen plasma treatments for better adhesion. Standard photolithography process was then applied to define the bonding pads. Focusing on the application on chip integration [10], SU-8 with 13µm and 28µm thickness, and AZ4620 with 10µm and 19µm thickness were selected to create suitable aspect ratios of the cavity. The silicon wafers were then diced by diamond blade into samples. A clean 30µm

parylene-C film treated by oxygen plasma was then aligned with the diced wafers under microscope, and the structure was further sandwiched by two glass slides for better protection.

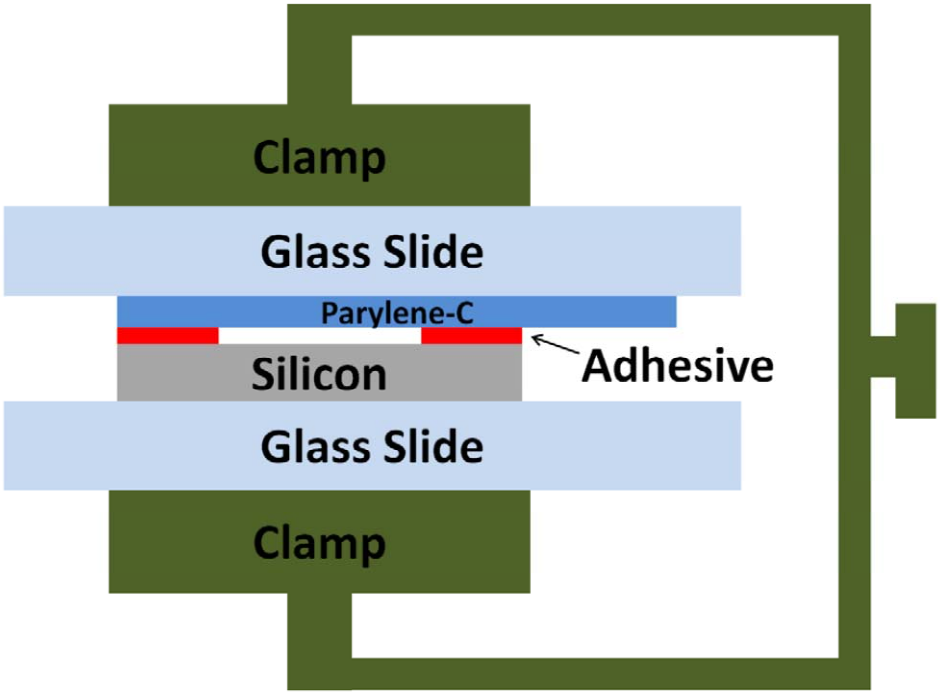


Figure 3.2. Schematic representation of a clamp as the bonding tool on the testing samples.

Figure 3.2 showed the photo-patternable adhesive bonding process. A clamp was used as the bonding tool to make good contact and apply constant force on the testing samples. The heating process was operated in vacuum oven and the maximum testing temperature was set as 150ºC to prevent IC chips from damage. Figure 3.3 showed the cross-sectional SEM images of the samples bonded by photo-patternable adhesives. The bonding pads were well defined with desired thickness and the shape of the microstructures was not changed during bonding process. Besides, the flexible intermediate adhesives will not cause the residual stress after bonding. In order to examine and quantify the bonding effect, the peeling force was measured by a force gauge setup, as shown in Figure 3.4, to investigate the bonding force. Selective bonding property was also demonstrated on

samples with 0.75 cm^2 bonding area. Force gauge was fixed on a motorized stage to pull the partially peeled film at 90 degree to the substrate with a speed of 100μm/s. Maximum forces were recorded to compare the peeling forces under different bonding conditions. Each data point represents the average of five measurements.

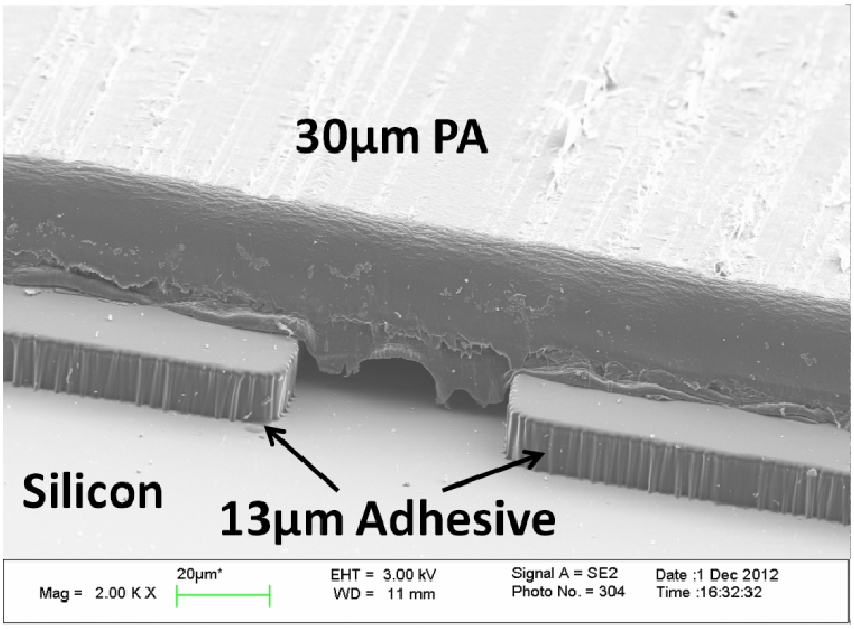


Figure 3.3. Cross-sectional SEM image of the adhesive bonding between parylene sheet and silicon (2MPa, 130ºC). The shape of the microstructure keeps the same after the bonding process and the bonding pads are well defined.

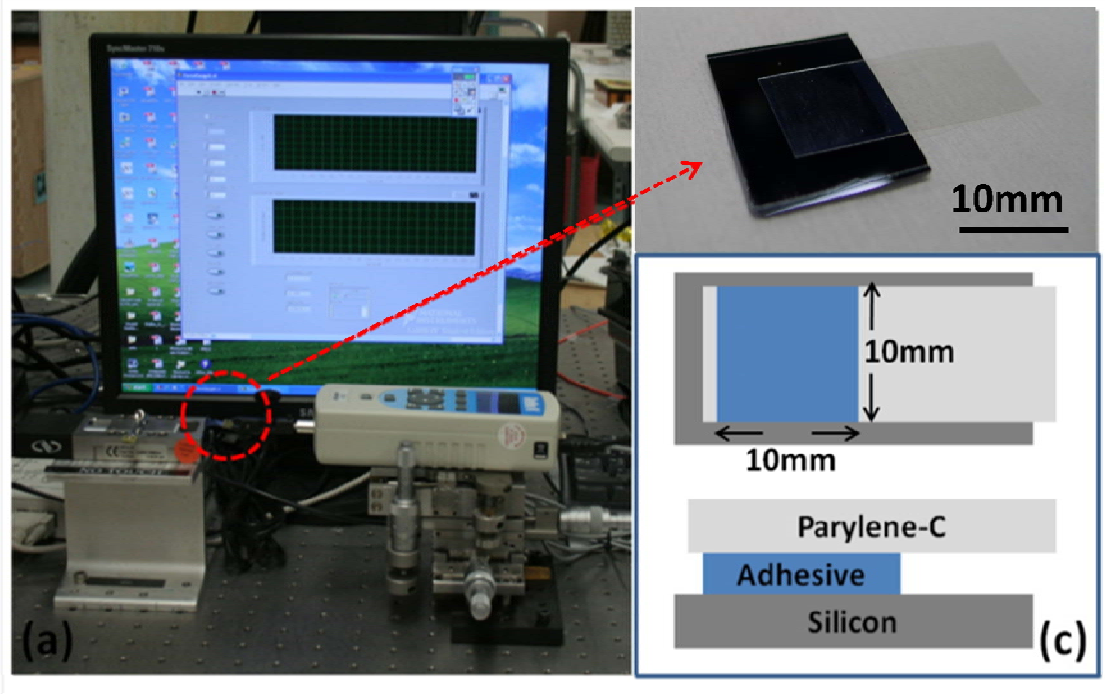


Figure 3.4. (a) Setup of the force gauge to measure the peeling force. (b) Real testing sample after bonding. (c) Schematic representation of the testing sample with top view and cross-sectional view.

3.3.2 RESULTS AND DISCUSSION

Various bonding parameters, including temperature, pressure, time, and surface treatments, for the photo-patternable adhesive bonding are used in this study. The bonding pressure corresponds to the torque applied by the wrench. The following equations are used to calculate the bonding pressure [11]:

$$F = \frac{T}{K \times d} \qquad [3\text{-}1]$$

$$P = \frac{F}{A} \qquad [3\text{-}2]$$

Where T is a torque applied by the wrench; K is the nut factor of the material; d is the diameter of the bolt; F is the load applied by the tighten bolt; A is the bonded area; P is the bonding pressure. Figure 3.5 showed the peeling force as a function of bonding temperature with 1 hour bonding time and the results showed that basically the higher the bonding temperature, the stronger the bonding

will be for the temperature range under 150ºC. Figure 3.6 showed the peeling force as a function of bonding pressure. The peeling force increased continuously as bonding pressure increases up to 8.4 N/cm^2 at 150ºC for 1 hour.

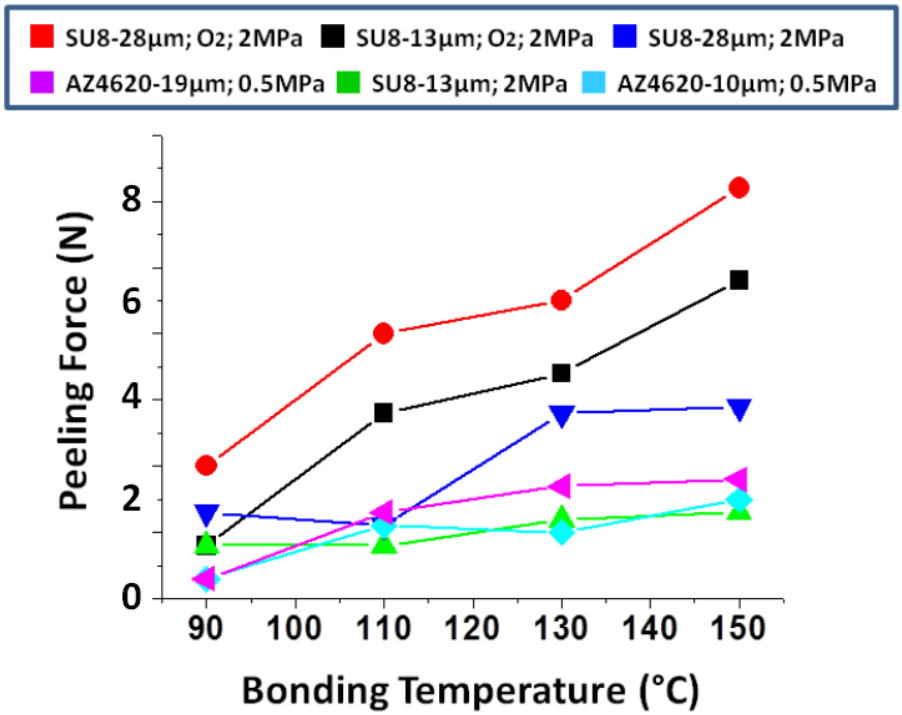


Figure 3.5. Peeling force v.s. bonding temperature for various photo-patternable adhesives.

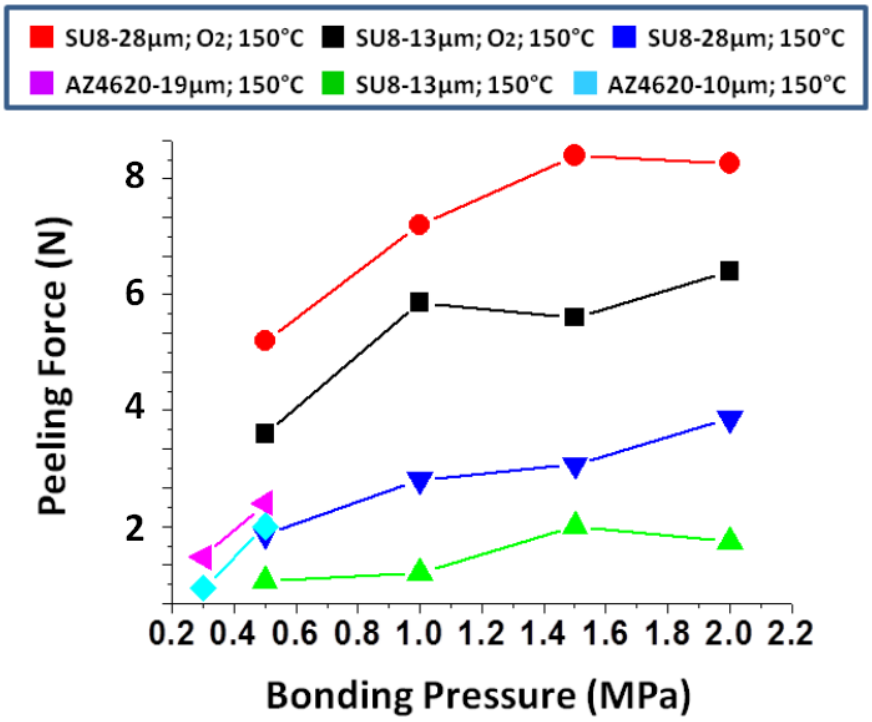


Figure 3.6. Peeling force v.s. bonding pressure for various photo-patternable adhesives.

When the bonding pressure was smaller, the air gaps generated by the uneven surface layer made the peeling force weaker. SU-8 with epoxy feature produced higher bonding force than AZ-4620. It was cross-linked on exposure to UV light and increases chemical resistance after UV exposure. Besides, SU-8 can be used to construct features with high aspect ratio more easily than AZ-4620. Bonding temperature under 90ºC and bonding pressure under 0.5MPa were also tested. However, the peeling force was too weak to be measured repeatedly. This might be due to the insufficient reflow and cure of the adhesives during bonding process. Besides, bonding will become very weak when the bonding temperature was much lower than the glass transition temperature (Tg). Figure 3.7 showed the interface of patterned adhesive before and after peeling test. SEM images showed that the interface was very uniform which means parylene sheet has good contact and bonding with photo-patternable adhesives. Parylene-C film treated by oxygen plasma dramatically enhanced the bonding

for SU-8. However, this phenomenon was not obvious for AZ4620. SU-8 treated by oxygen plasma has weak bonding strength because of the removal of uncrosslinked material from the surface [12]. For the adhesive bonding, it is necessary to have residue uncross-linked SU-8 to allow reflow during the bonding process.

SU-8 microstructure will not deform even under bonding pressure as high as 2MPa where the maximum bonding formed, as shown in Figure 3.8(a), but AZ-4620 can only stand the pressure up to 0.5MPa. Although most of the bonding happened at interface, thickness-dependent peeling force was still observed which is more obvious on SU-8 structure with parylene samples treated by oxygen plasma. One possible reason is the remained uncrosslinked SU-8 further enhance the bonding. The effect of bonding time on bonding strength was also investigated and the results revealed that it has almost no effect on the bonding strength after the samples were heated more than one hour, as shown in Figure 3.8(b), which implies most of the reflow process happened in the first hour.

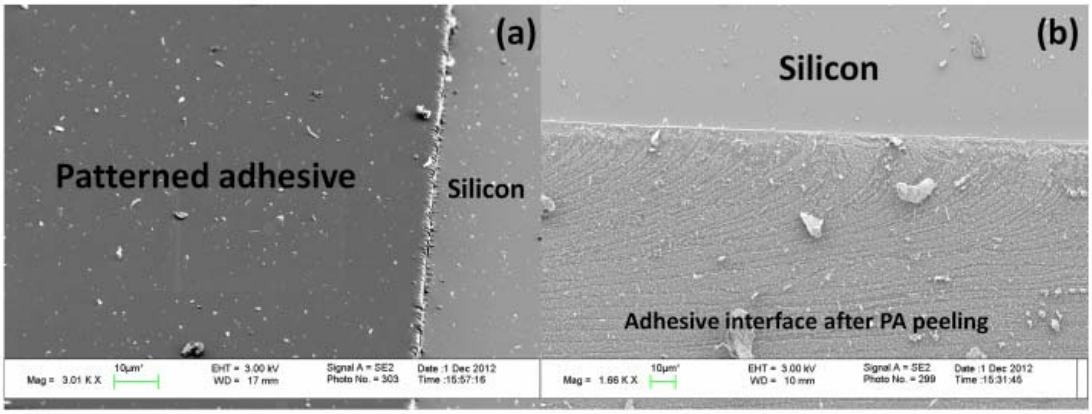


Figure 3.7. Adhesive interface before (a) and after (b) peeling test.

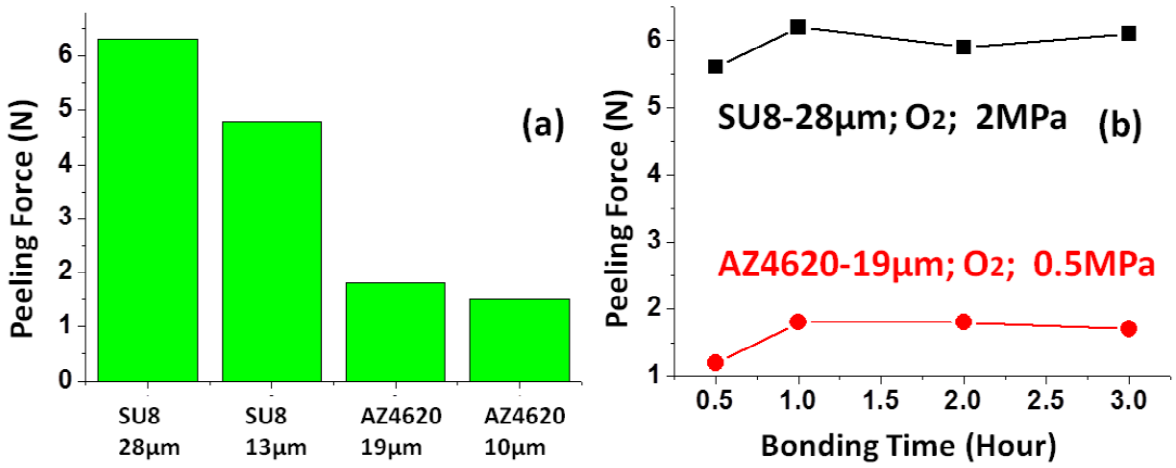


Figure 3.8. (a) Maximum peeling forces of different photo-patternable adhesives. (b) Peeling force v.s. bonding time for different photo-patternable adhesives.

3.4 Applications on high-density multi-channel chip integration

In order not to use the PDMS mold during connection process, a custom chip holder was designed and fabricated. Chips were first secured in the holder, and all the chip pattern lithography, including photoresist spinning, baking, exposing, and developing was done on this holder in series, as shown in Figure 3.9. After chip integration with parylene-C flex by photo-patternable adhesive bonding technology plus conductive epoxy squeegee connection technique, chips can be released from the back side of the mold, which will be beneficial for the whole device to be implanted inside eyeball. Dummy chips with conductive traces were fabricated to simulate the real chip and special pads were pre-connected in fabrication for connection yield measurement.

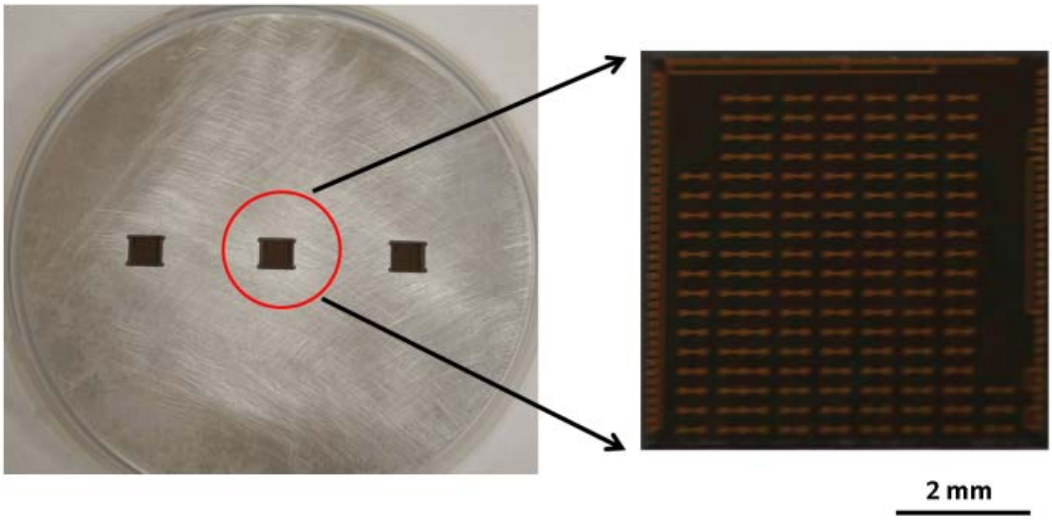


Figure 3.9. Custom holder for chip assembly technique; all lithography was done on this holder which also served as the safety buffer zone for squeegee.

The mask, as shown in Figure 3.10, was designed only to expose specific metal pads which also served as the alignment marks. Resolution of around 5μm can be achieved. AZ4620 and SU-8 photoresist were chosen in this process due to their better reflow property [13]. The patterned adhesives were then baked at 140°C for 30 minutes in vacuum oven and its smooth surface formed by reflow also helped the conductive epoxy to refill, as shown in Figure 3.11. Besides, the side lengths were almost the same before and after baking so that the reflown photoresist wouldn't cover the whole metal pads to affect conductivity.

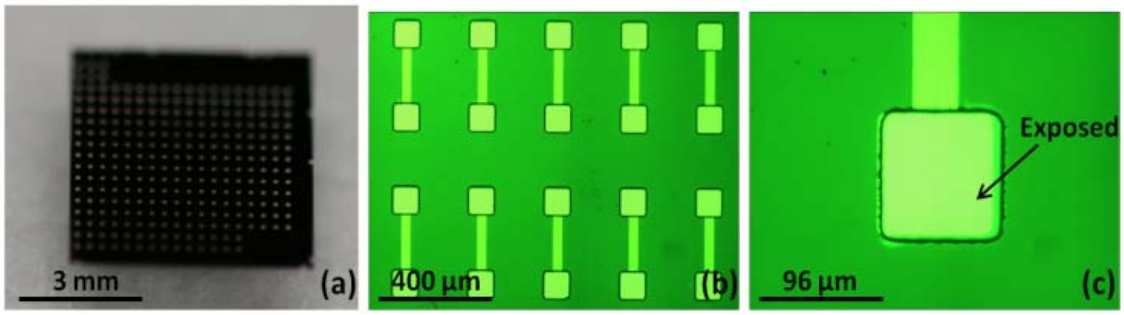


Figure 3.10. (a) Dummy chip for assembly yield test; pads also served as alignment marks. (b)&(c) Metal pads were exposed; resolution of around 5μm could be achieved.

Our previous work only relied on conductive epoxy which was fed through the cavity embedded in parylene-C flex substrate to make both electrical and mechanical connections; the new assembly technique relied both on conductive epoxy and photo-patternable adhesives as the glue. In fact, after applying photo-patternable adhesives (as glue here) to the chips, the total gluing area between parylene-C substrate and a chip was increased from 2% to 94%, as shown in Figure 3.12. Note that the unnecessary pads for testing only were also covered to avoid shortage happening underneath parylene-C interface during squeegee connection process. The high-density connections between the chip and the parylene-C flex substrate were again done by conductive epoxy squeegee, while the custom holder provided the safety buffer zone for squeegee to totally replace the function of PDMS holders [14].

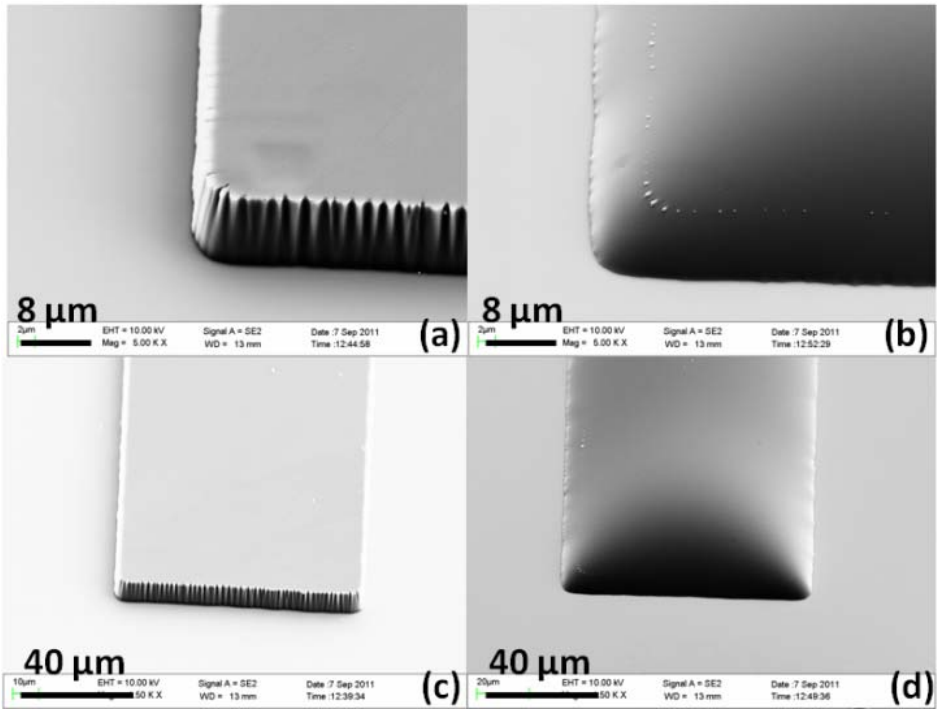


Figure 3.11. (a) Unbaked AZ4620. (b) AZ4620 baked at 140°C for 30 minutes in vacuum oven; slope formed by reflow will be beneficial for conductive epoxy to be fed through. (c)&(d) Side lengths show no change before and after baking.

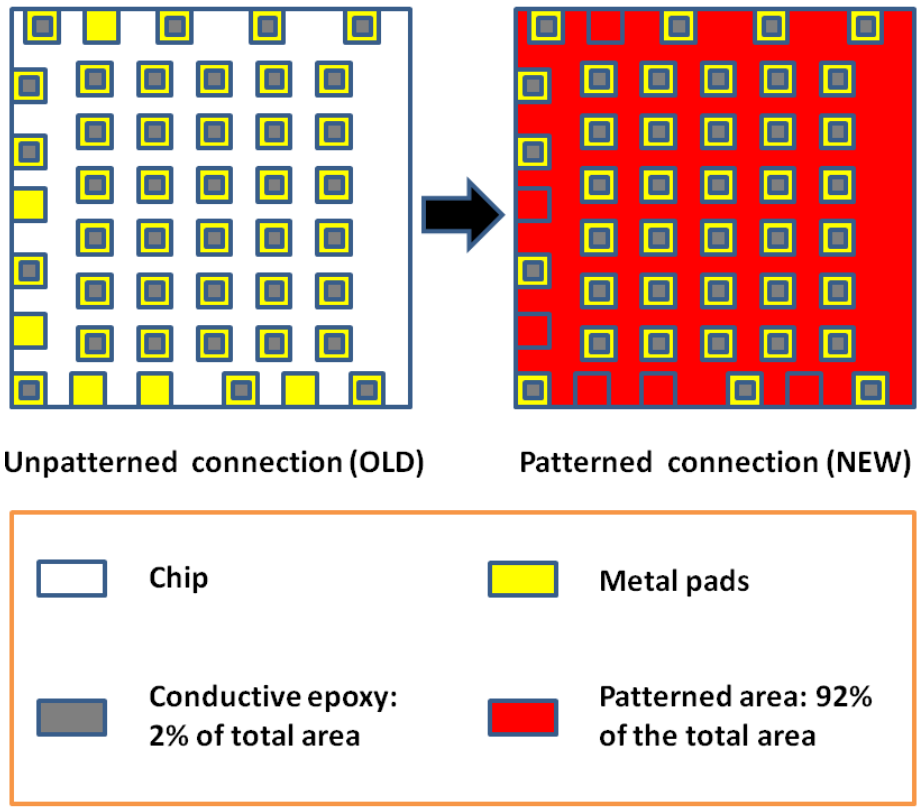


Figure 3.12. Gluing area was increased from 2% to 94% (2%+92%) by the extra photoresist used as glue. Note that unnecessary pads were covered to avoid shortage.

3.4.1 YIELD TEST

The parylene-C interconnecting substrate hosts all the electronic components (application specific integrated circuits), which were interconnected via 3.7μm wide metallization traces. As shown in Figure 3.13, the discrete components (mostly capacitors) on the right hand side were mounted and connected by conductive epoxy to make electrical connection. There are also two suture holes for the device to be fixed on eyeball. Besides, the multi-electrode array on the left hand side will be placed on the macula and fixed by retinal tack. The interconnection part is only 2mm wide because of the limitation of surgery cut on eyeball for surgery consideration.

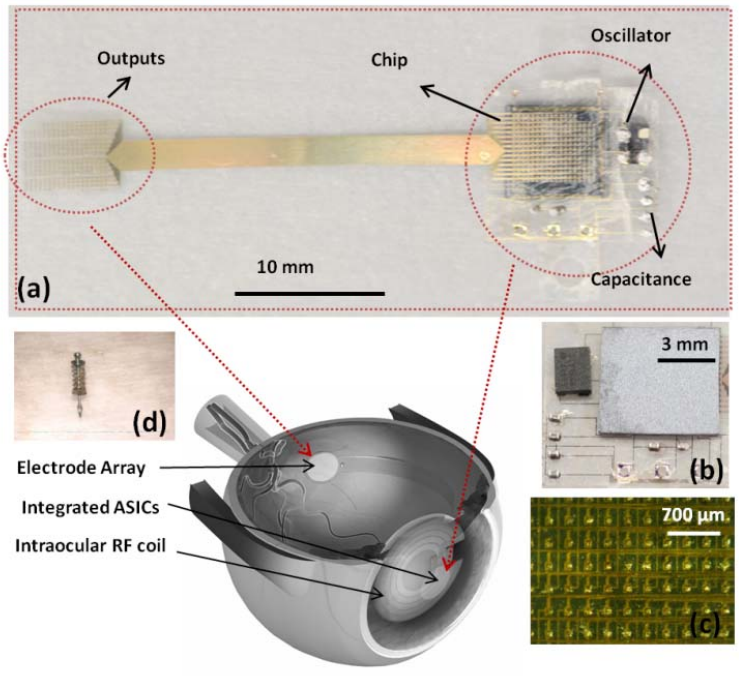


Figure 3.13. (a) Dummy chip and discrete components integrated with surgical parylene flex. (b) Backside of the dummy chip and discrete components. (c) Close-up view of the high-density multi-channel chip integration. (d) Retinal tack used to fix stimulating electrodes on retina.

As shown in Figure 3.14, we measured the connection yield right after squeegee by probing the stimulating electrodes. Afterwards, an additional thick parylene-C was coated on the entire device (except the output electrodes) to insulate and stabilize the connection, and to protect the metals embedded in parylene-C substrate from corrosive body fluids. The connection yield was then recorded again after this coating. Finally, we soaked the devices in 90°C saline solution for 5 days as well as recorded the connection yield again. The results in Figure 3.15 showed that the yield of the device with the new gluing technique is satisfactory (~98%), while the yield without the new technique is significantly lower (~88%).

For the connections without adhesive gluing techniques, most of the disconnections happened at peripheral pads where delamination force was applied to mostly.

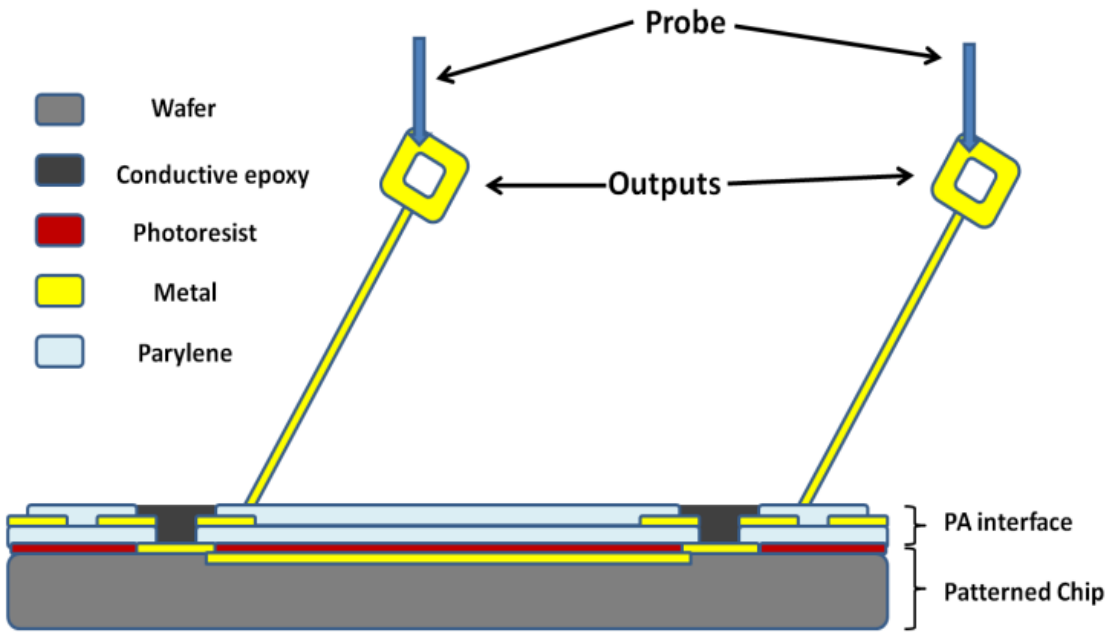


Figure 3.14. Setup of the measurement; the electrode array outputs (the electrode end that will be placed on macula) were probed to check the connection.

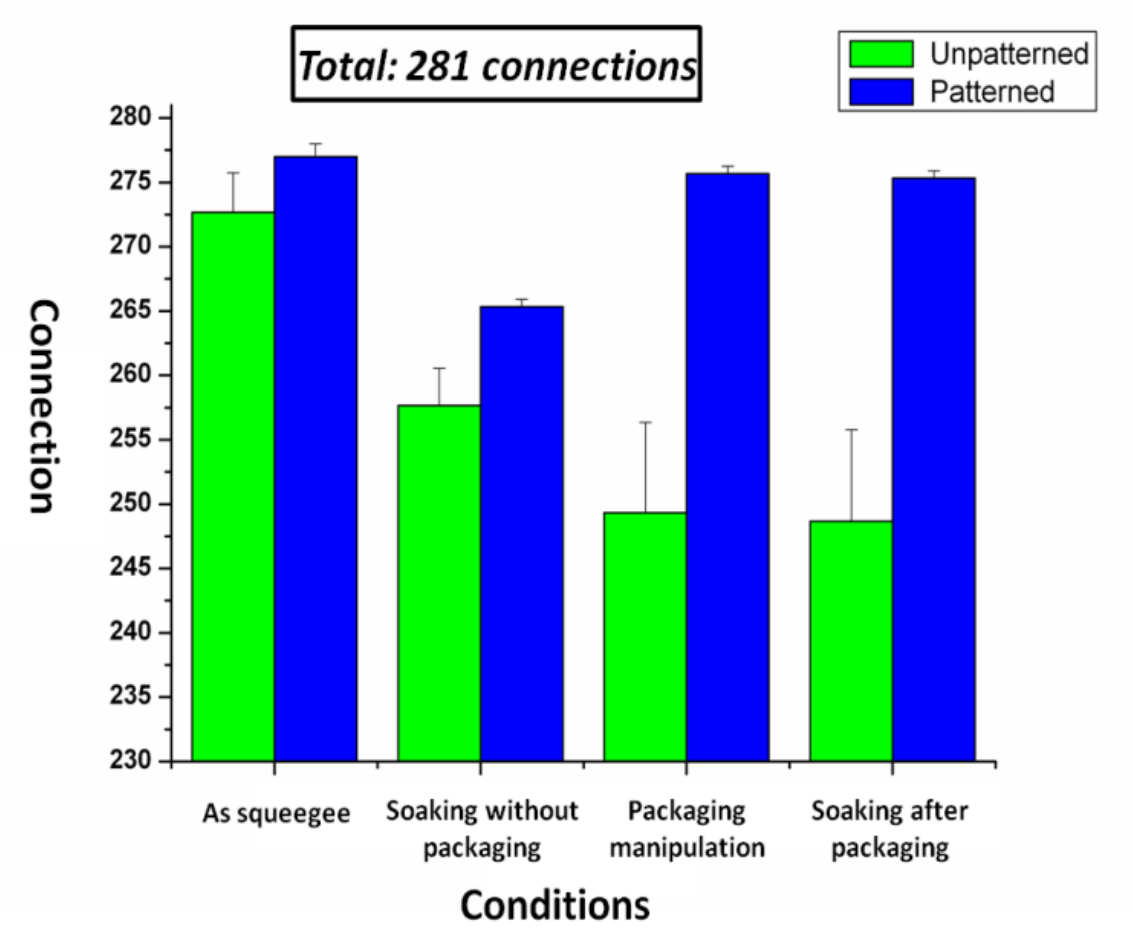


Figure 3.15. Connection yields under 4 different conditions; reliability tests were carried out after squeegee connection, encapsulation by parylene-C coating, and accelerated soaking in 90°C saline. The results show that our new technique combined with thick parylene-C coating do provides a high connection yield.

3.4.2 LIMITS OF THE PROPOSED TECHNOLOGY

To explore the limits of the minimal pad size and separation for this new technique, dummy chips with different pad separations and sizes were designed and fabricated for measurement. The results, shown in Figure 3.16, showed that high connection yield (>90%) can be achieved for pads as small as 40μm by 40μm and with a 40μm separation in between.

Failures on even smaller pad sizes and separation came from the open channels due to small cavity embedded in parylene-C flex substrates. Based on the current results, it implied that this new technique, when combined with a laser repairmen technique (not reported here), can be applied to as much as 10,000 connections within an area of 6mm by 6mm, which is satisfactory for current retinal prosthetic application.

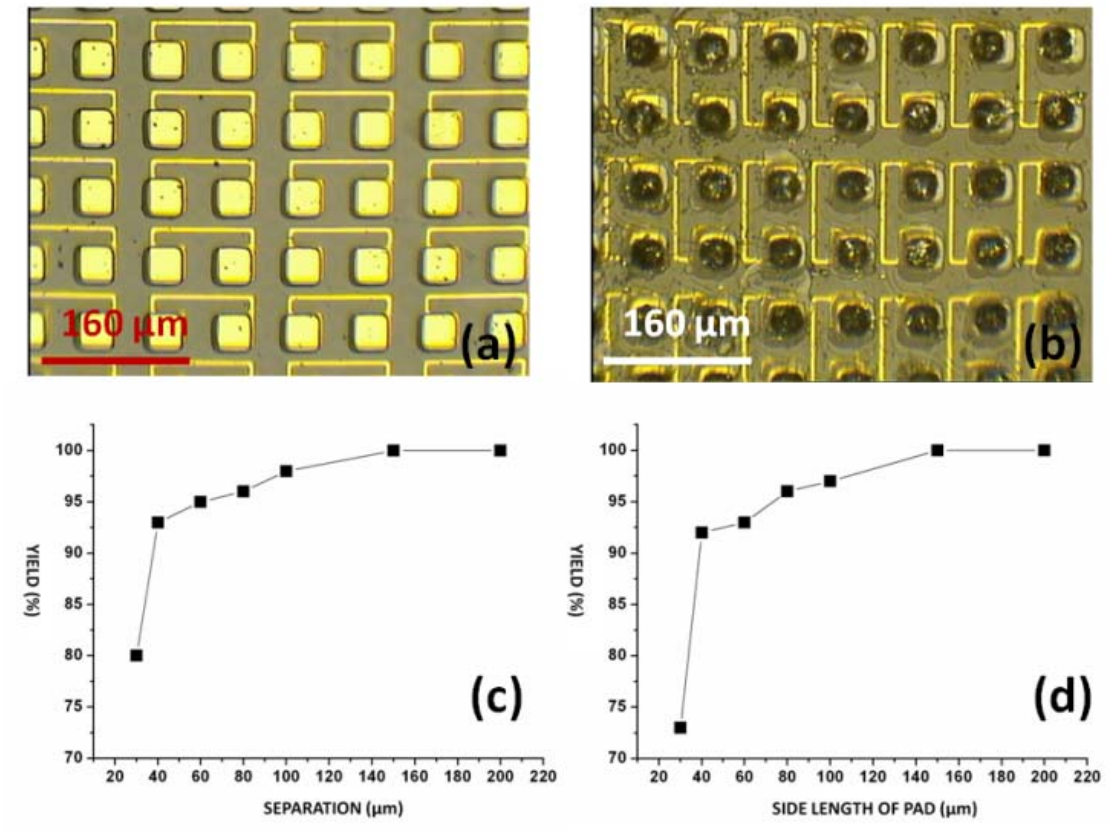


Figure 3.16. (a) Dummy chips with 40µm by 40µm pad size and 40µm separation. (b) Connection between parylene substrate and dummy chip. (c) Yield v.s. separation of pads. (d) Yield v.s. side length of pads. The results show that high connection yield (>90%) can be achieved for pads as small as 40µm by 40µm and with a 40µm separation in between.

3.5 Real chip functional testing

As a demonstration, this photo-patternable adhesive bonding technique was applied on a 268-channel dummy conduction chips and real 268-channel and 1024-channel IC chips in order to integrate with parylene-C surgical device for retinal implant, as shown in Figure 3.17. The purpose of this application was to further enhance the bonding between the parylene devices and IC chips, which is crucial for surgical handling. Besides, it also guaranteed that no movement will happen during the conductive epoxy squeegee process to make electrical and mechanical connections. The spatial resolution of bonding pads built by SU-8 can be 5 μm. After patterning the adhesives on chips, the bonding area was dramatically increased from 2% (conductive epoxy only) to 94% (conductive epoxy plus photo-patternable adhesives), as shown in Figure 3.18. The adhesives can also cover the unnecessary bonding pads to avoid shortage happen. The measured connection yield on conduction chips was improved from 92% to 98%.

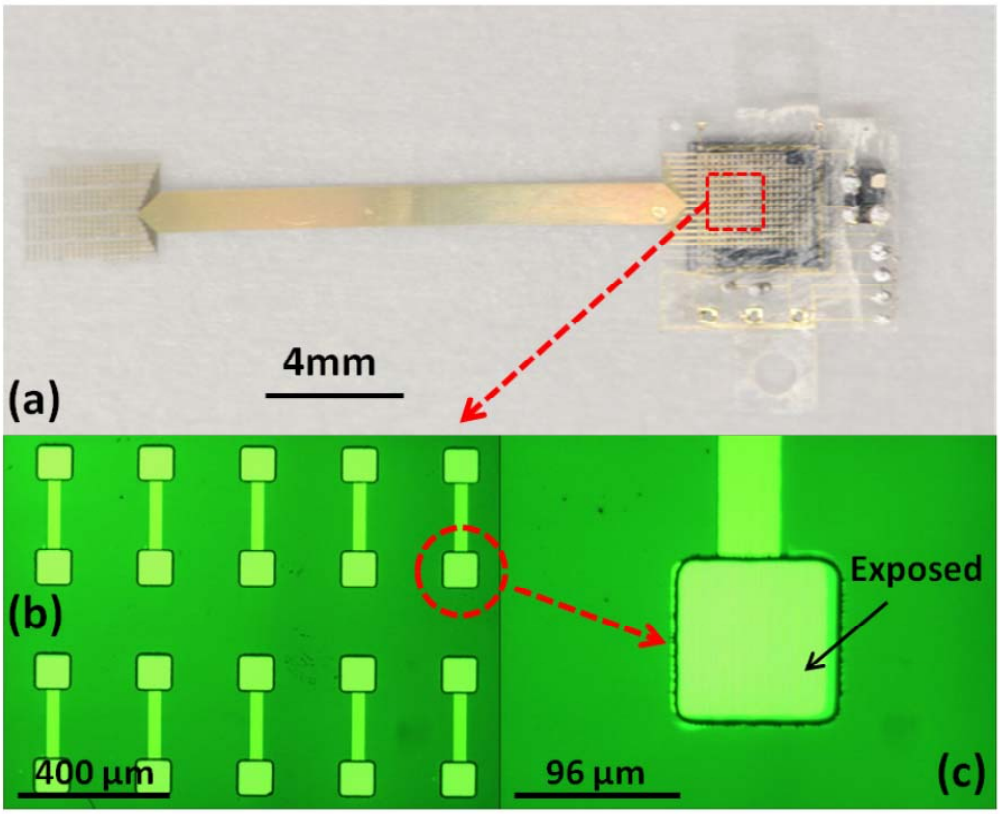


Figure 3.17. (a) Surgical parylene-C device connected with silicon chip and discrete components. (b)(c) Only desired metal pads are exposed; other area is covered by photo-patternable adhesives. The alignment accuracy can be improved to be around 5 µm.

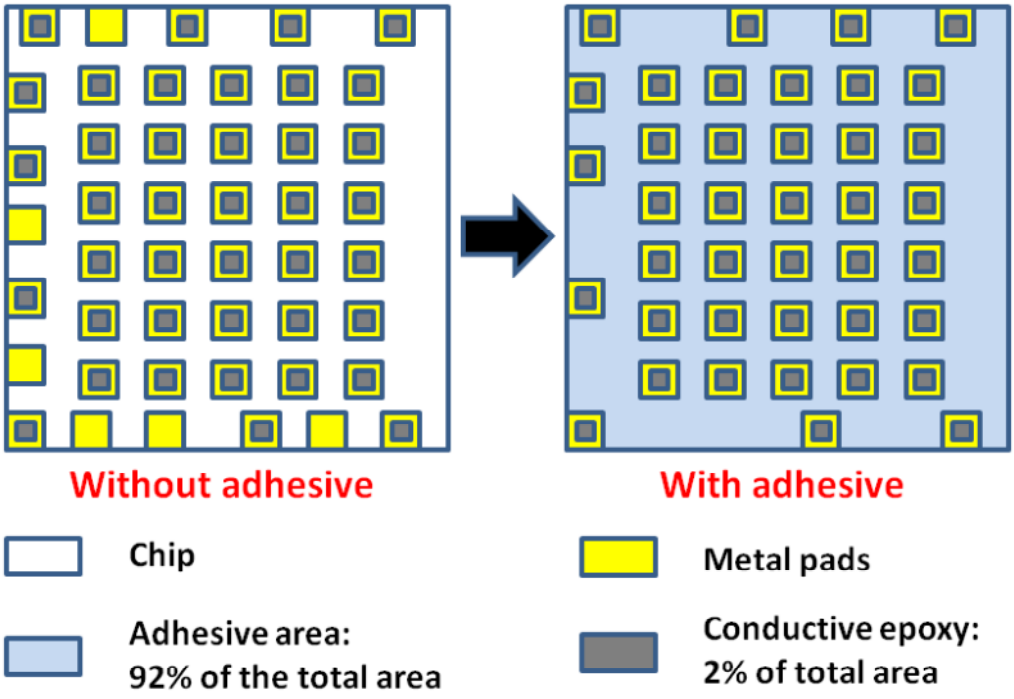


Figure 3.18. Gluing area is increased from 2% to 94 (2+92)%. Unnecessary pads are also covered to avoid electrical shortage during conductive epoxy squeegee process.

3.5.1 Testing on 268-channel chip integration

This technique was further applied to the real 268-channel retinal IC chips, as shown in Figure 3.19. The pad size is 96 µm × 96 µm, and the separation is only 50 µm. 30 crucial pads on peripheral are needed to be connected to get a functional system. The technology was applied on this chip, and only crucial pads on peripheral were exposed for connection, as shown in Figure 3.20. Basic chip functionalities, including oscillator assembly, clock level shifter, and low voltage rectifier, were successfully tested with high yield to verify its effectiveness, as shown in Figure 3.21.

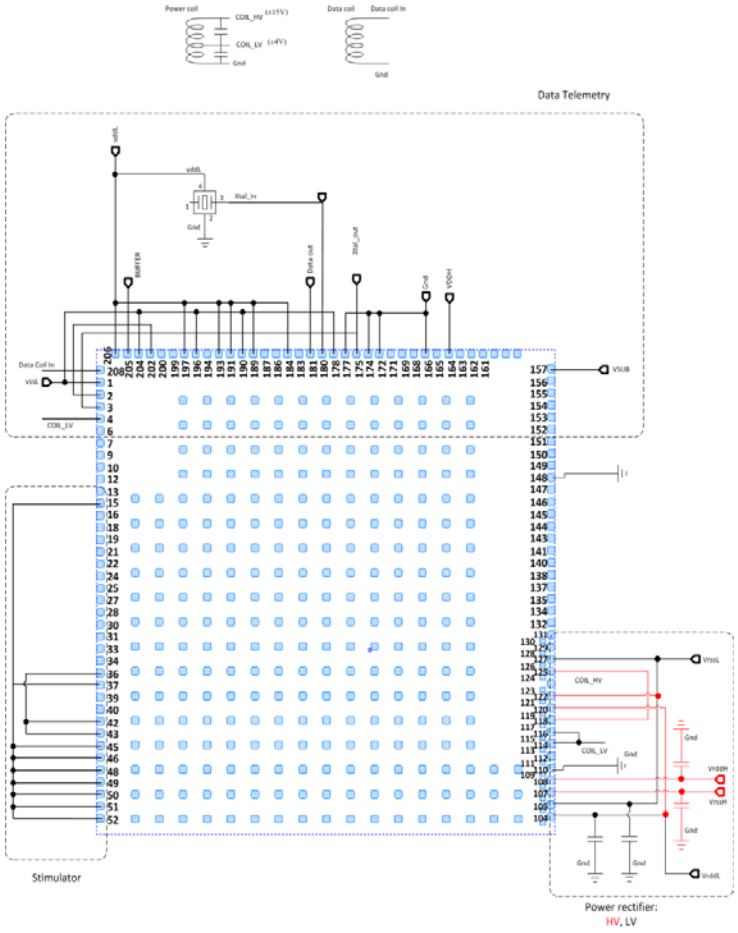


Figure 3.19. Layout and wiring diagram of the real 268-channel retinal IC chip.

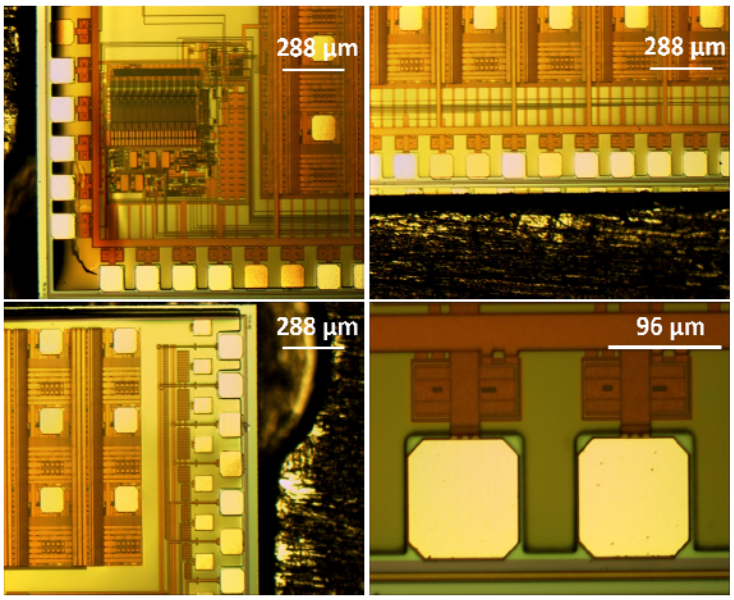


Figure 3.20. Only desired metal pads were exposed; other area and pads for testing only were covered by photo-patternable adhesives.

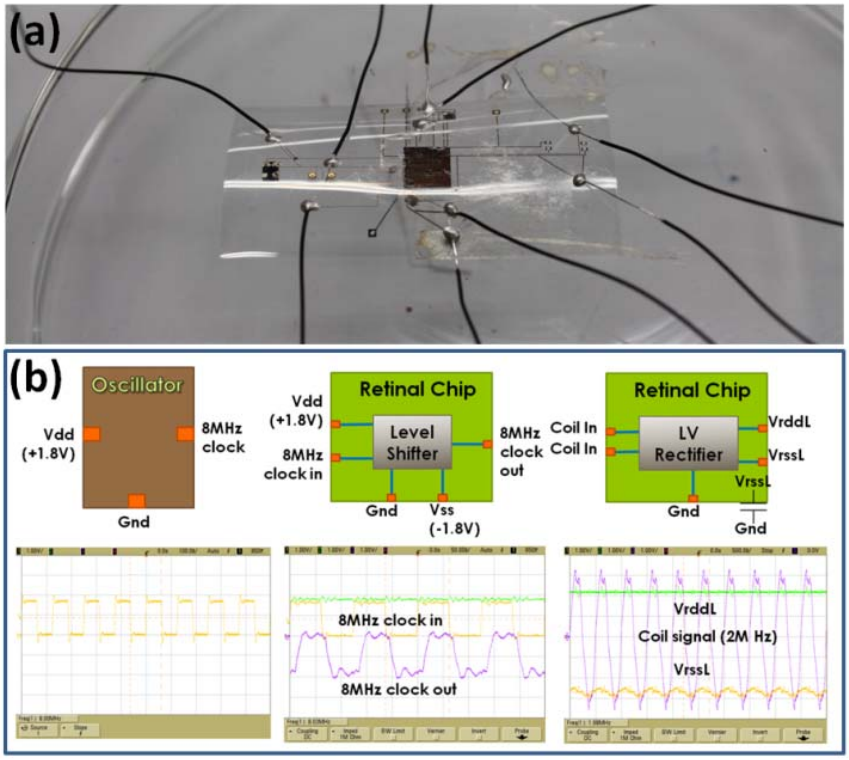
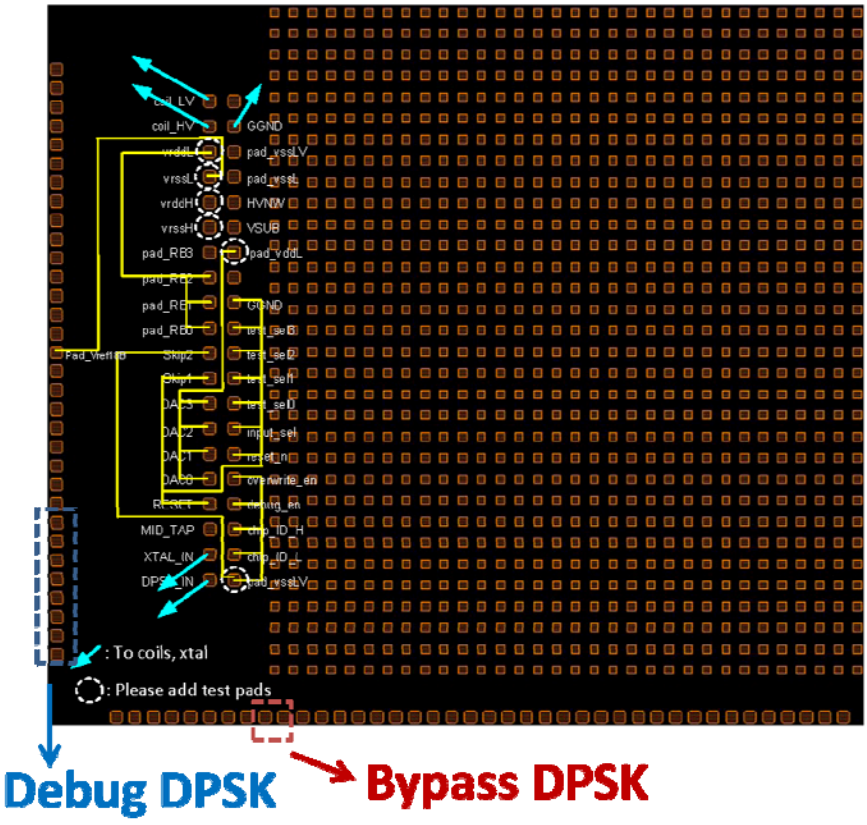


Figure 3.21. (a) Real 268-channel retinal IC chip integration by photo-patternable adhesives and conductive epoxy squeegee techniques. (b) Successful functional signal testing including oscillator assembly, clock level shifter, and low voltage rectifier.

3.5.2 Testing on 1024-channel chip integration

We also applied this technique on the real 1024-channel retinal IC chips, as shown in Figure 3.22. The chip size is around 6 mm × 6 mm. The input pad size is 96 μm × 96 μm, with a separation of 104 μm in center and 54 μm on peripheral. The output pad size is 66 μm × 66 μm, with an average separation of 90 μm. There are 41 critical pads needed to be connected, in which five of them are for debugging DPSK data function, and three of them are for bypassing DPSK. Figure 3.23 showed the parylene flex integrated with this 1024-channel retinal IC chip by conductive epoxy squeegee technique, and the connection between the parylene flex and the critical pads on retinal IC chip can be seen very clearly.

The tested power coil from USC (center-tapped receiver coil), as shown in Figure 3.24, was first tested and proved to have similar inductance ratio and even better Q factor compared to the litz-wire coil used in UCLA's demo system. Therefore, this center-tapped coil can be used as the receiver coil, working with the transmission coil from UCLA, and can also be further applied on the implanted device. This coil can successfully induce correct voltages for the 1024 channel retinal IC chip and was used as the receiver power coil for the whole system. With correct induced voltage from the receiver power coil, all correct DC voltages including VrddL, VrddH, VrssL, and VrssH were successfully tested via wires through parylene flex with high yield, as shown in Figure 3.25. Besides, the crystal oscillator output with 16MHz signal can also be measured to drive the chip, as shown in Figure 3.26. Further testing on data communication and stimulators were also performed. However, for some uncertain reasons, the correct DC voltages suddenly became AC voltages that cannot drive the data communication. Since the signal still can be measured through the parylene flex, apparently the integration between the retinal IC chip and parylene flex still worked well. Besides, the metals embedded in parylene flex were also in a good condition to allow current and signal send in. However, more detailed testing needs to be done to debug.



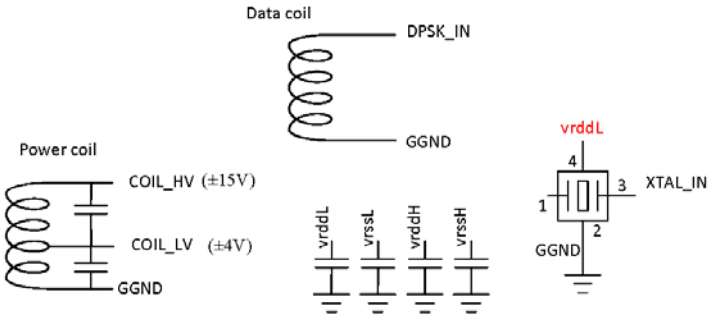


Figure 3.22. Layout and wiring diagram of the real 1024-channel retinal IC chip.

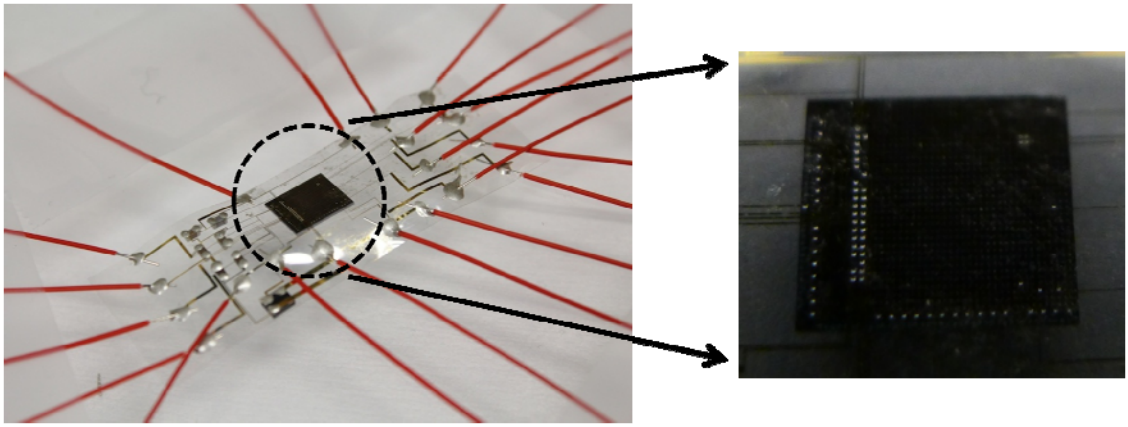
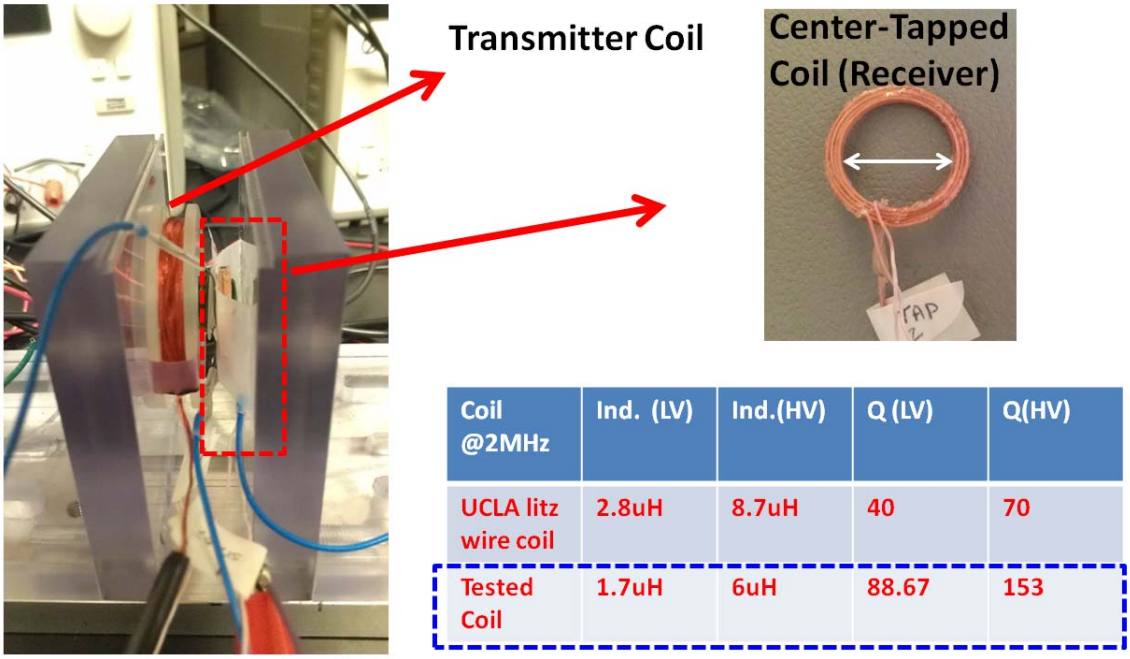


Figure 3.23. Parylene flex integrated with 1024-channel retinal IC chip, and the connection of critical pads can be seen very clearly.



Coil @2MHz	Ind. (LV)	Ind.(HV)	Q (LV)	Q(HV)
UCLA litz wire coil	2.8uH	8.7uH	40	70
Tested Coil	1.7uH	6uH	88.67	153

Figure 3.24. The tested power coil from USC (center-tapped receiver coil) has similar inductance ratio and better Q factor compared to the litz-wire coil used in UCLA's demo system. It can successfully induce correct voltages for the 1024 channel retinal IC chip and was used as the power coil for the whole system.

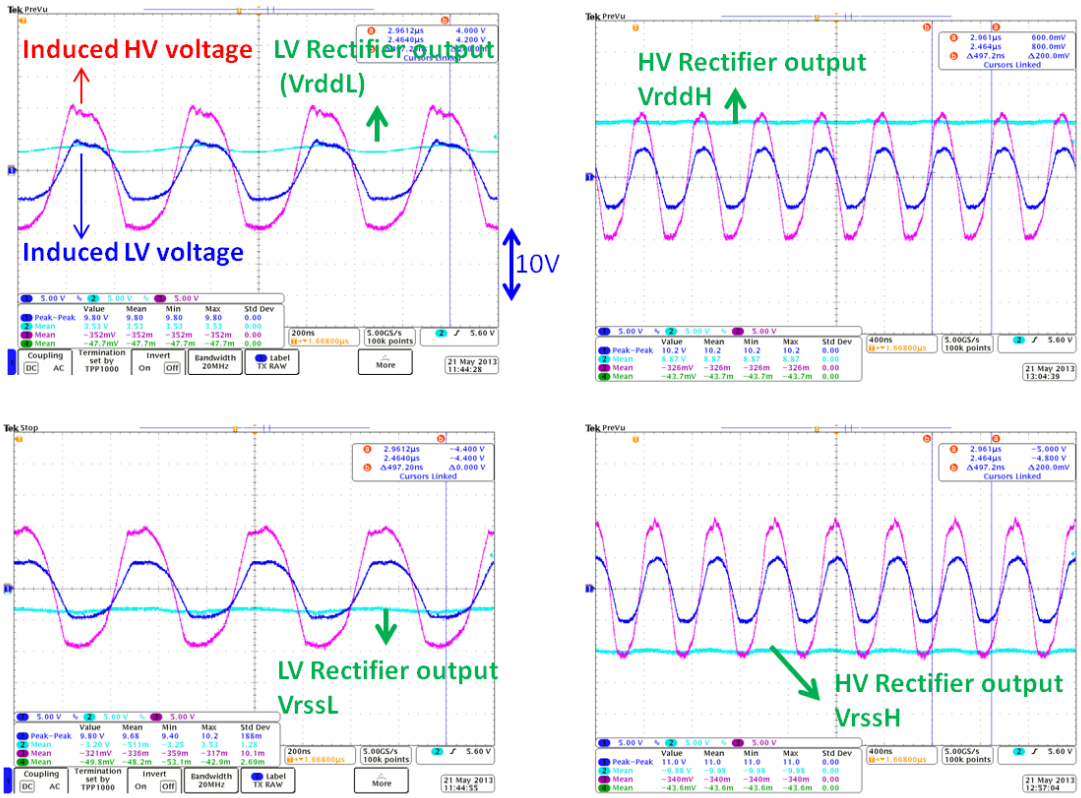


Figure 3.25. With correct induced voltage from the receiver power coil, all correct DC voltages including VrddL, VrddH, VrssL, and VrssH were successfully tested via wires through parylene flex with high yield.

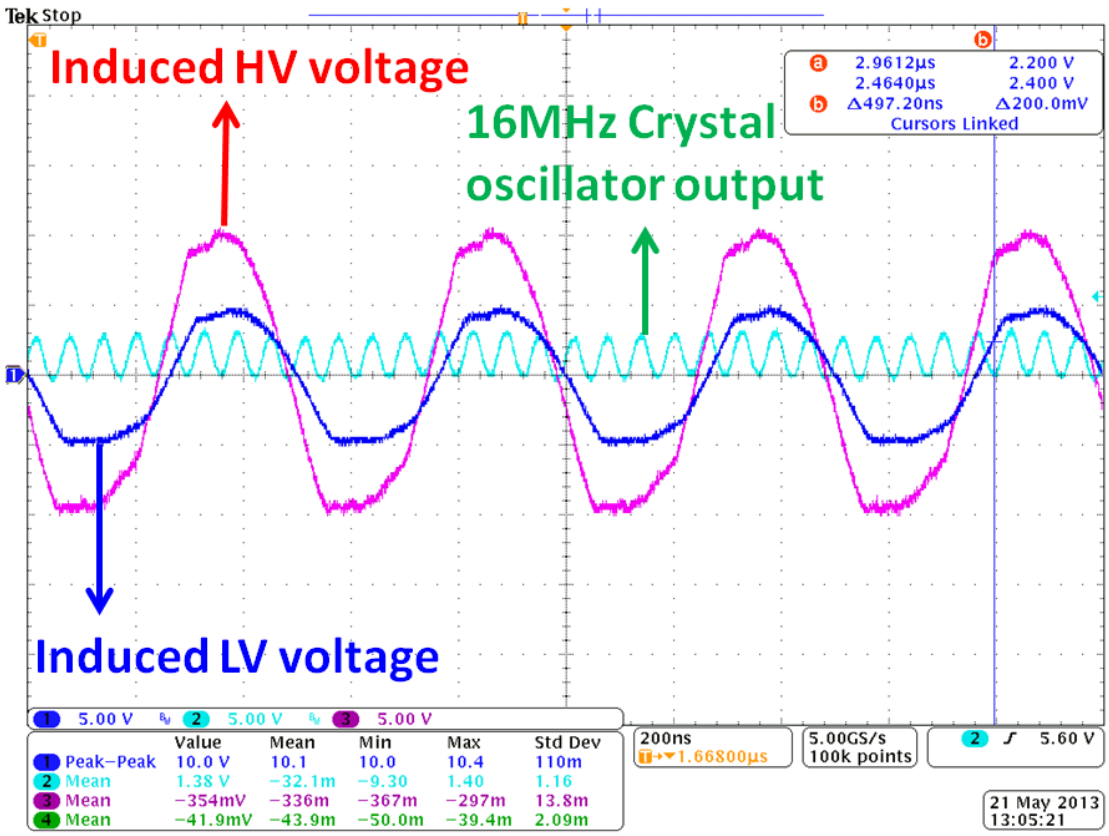


Figure 3.26. With correct induced voltage from the receiver power coil, the crystal oscillator output with 16MHz signal was successfully tested via wires through parylene flex with high yield.

3.6 Summary

Parylene-C has become a more and more popular material for BioMEMS implant applications due to its good biomedical properties [15-16]. It was also used as an intermediate layer for silicon wafer bonding [17-18]. However, the bonding between parylene-C and silicon was still problematic for a long time. In this chapter, a low-temperature bonding between parylene-C and silicon using photo-patternable adhesives was presented. This method can not only determine the bonding pads but also reduce the residual stress in the packaging. Its application on high-density multi-channel chip integration was also demonstrated. Two commercially available photo-patternable materials, i.e., SU-8 and AZ-4620, with stable characteristics were chosen to demonstrate this method. The processing

conditions were optimized in terms of the bonding temperature, pressure, time, and surface treatment. The peeling force was measured by ASTM peeling tests under various bonding conditions. The results showed that the epoxy-based SU-8 is better than AZ-4620 as an adhesive material with a peeling force up to 8.4 N/cm^2 with 28 μm thickness SU-8 at 2MPa, 150ºC for 1 hour. This low-temperature bonding technique allowed selectively local area bonding. Besides, bonding without applying a high electric field is especially suitable for the integration with microelectronics in MEMS packaging.

This new chip packaging technique by photo-patternable adhesives for the assembly of retinal prosthesis device was further described here. Here, a photoresist was used as glue to attach a chip to the targeted parylene-C flex so that 94% of the chip area was used as attachment to prevent delamination. As a validation, dummy chips with 268 connections were used to assess the connection yield. The results showed that this new technique, combined with an additional parylene-C coating, provided a high connection yield (>90%) and is a promising method for high-lead-count implant devices. This technique was further applied to the real 268-channel and 1024-channel retinal IC chips connection process. Gluing area was greatly enhanced and the connection yield was improved as well. Measured signals from real chips further verified the effectiveness of this technology. This low-cost and low-temperature bonding process was proven to enable the sealing of MEMS structures. This new packaging technology is promising to be applied to 10,000 connections within an area as small as 36mm^2, a chip size reasonable for retinal implants [19].

Although many implantable devices have been developed by micro-electrical-mechanical system (MEMS) technology to assemble IC chips to some microfabricated devices, there is still room for better packaging technology to be researched, especially for high-lead-count retinal and neural implants. In this chapter, we have proposed a new technique which is more reliable and repeatable to assemble IC chips to a parylene-C flex for retinal implant application.

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4 LIFETIME STUDY OF PACKAGING AND SURGICAL MOCKUP

4.1 Introduction

An important function of an encapsulating coating on electronic integration is to provide a moisture barrier that can prevent corrosion to the underneath structural materials, so the water vapor transmission rate (WVTR) is an important parameter that can quantify the effectiveness of the protection barrier. Biocompatible silicones have been used as encapsulation layer for decades but it is known that most silicones tend to have a rather large WVTR due to their porous structure. One way to reduce the WVTR by adding another parylene-C coating on silicone was reported to seal the silicone layer and can have very good adhesion to it [1]. However, the parylene-C coated bio-compatible silicone layer tends to be thick and can lose its elastic flexibility.

Table 4.1. Water vapor transmission rate (WVTR) of common materials used to protect parylene-based device.

Materials	WVTR (g.mm/m².day)@37°C
PA-C	0.08
PA-HT	0.22
PA-D	0.09
Epoxy	0.94
Silicone	47
Metal	~0.000006

On the other hand, Parylene-C has been extensively used in biomedical devices and interfaces as a structural material or a conformal and bio-compatible coating [2]. It has also become a packaging material because of its many favorable properties. The water permeability and the chemical stability of parylene-C have also been studied [3-4], and the results showed that parylene-C is a very good bioinert insulator and parylene-C protected electrodes can survive a sufficiently long time with metals sandwiched by 9.2 μm parylene-C on each side. Therefore, a new protection scheme of parylene-metal-parylene flexible composite sandwich layer with lower WVTR, as shown in Table 4.1, was studied here to replace the traditional silicone-parylene combination, as shown in Figure 4.1. It not only has low WVTR but also preserves the flexibility that is crucial for devices such as retinal implants. Besides, an advanced protection scheme was also proposed after examining the current failure modes and was proved to have better protection .

A complete wireless retinal implant requires high-density multi-channel IC chips, discrete components (caps, inductors, and oscillators), and coils (power and data coils) to be packaged with high-density stimulating electrode array as shown in Figure 4.2. We have shown that high connection yield for both chips and discrete components can be achieved in MEMS 2012 [5]. The important next step is thus to improve the protective packaging for long lifetime of the retinal implant in human body. In this chapter, we studied the use of parylene-metal-parylene sandwich layer as an encapsulating coating to protect the implant devices. Devices without any protection, with parylene-C-only protection, and with parylene-C coated bio-compatible silicone protection were compared to each other. These packaging schemes were tested under active soaking conditions. The observed failure modes were examined and analyzed. The lifetime at body temperature of the devices with various protection layers were modeled by Arrhenius relationship [6].

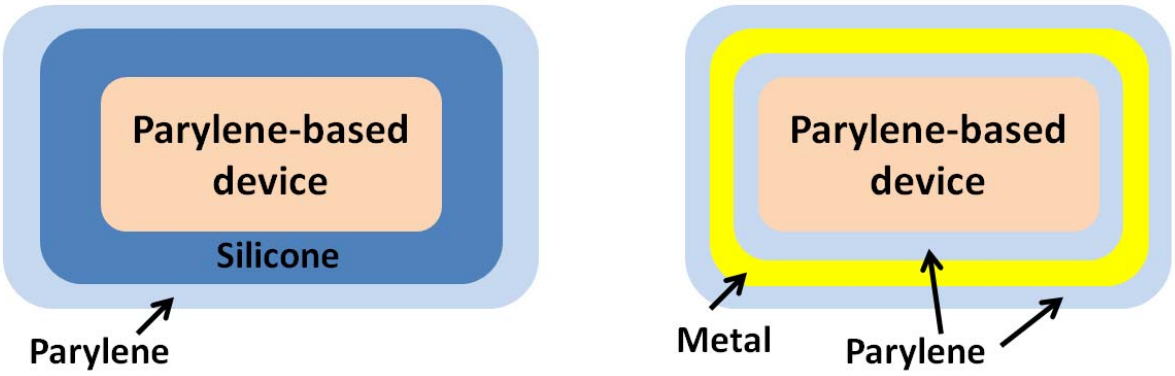


Figure 4.1. (Left) Parylene-based device protected by traditional silicone-parylene combination. (Right)Parylene-based device protected by the proposed parylene-metal-parylene protection scheme.

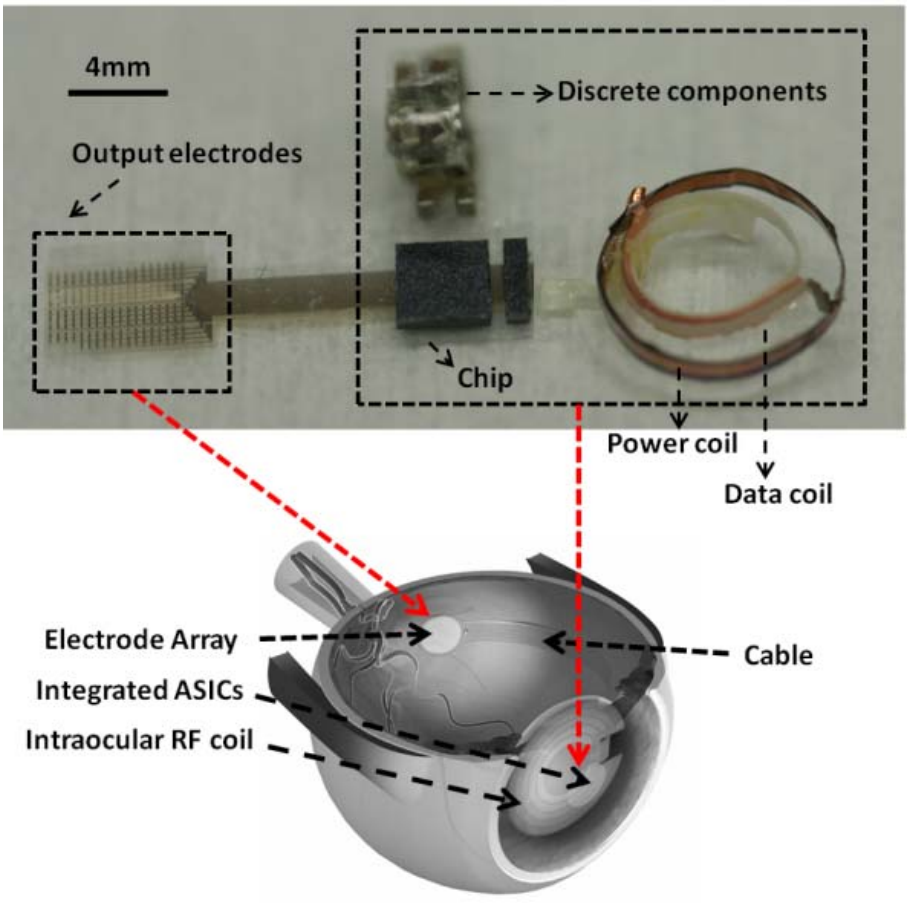


Figure 4.2. Schematic representation of the retinal implant connected with IC chips, coils, and discrete components.

Two of the most common retinal degenerative diseases worldwide are the age-related macular degeneration (AMD) and retinitis pigmentosa (RP). Several millions of people will be affected by these two diseases in the next ten years by estimation [7-8]. Blurry central vision and tunnel vision are the typical symptoms of the these two diseases respectively, as shown in Figure 4.3. Even though gene therapies, drug and nutritional therapies [9-10] have been and are being developed to lower the rate of such occurrence, AMD and RP still caused the loss of rod and cone receptors in the eye and blindness in the long run will become inevitable. Visual prosthesis, a technique which aims to solve these problems and to regain eyesight for AMD and RP patients, then becomes a possible and feasible current choice for research and development around the world. Many groups have put much effort to develop multi-electrode arrays for retinal prosthetic applications [11-12]. However, even the most advanced prostheses do not have enough stimulating electrodes to restore vision to the desirable functional capability, like facial recognition or large-sized letter reading. Currently, the most advanced retinal implant approved by Food and Drug Administration (FDA) is the Second Sight's 60-channel Argus II implant [13]. However, this technology has not yet reached the minimally desirable number of channels around 1,000.

In this chapter, a system design and its packaging for a 512-channel epiretinal implant was presented using a parylene flex technology. A special 3-coil (i.e., two extraocular and one intraocular coils) wireless power transfer system with high efficiency up to 36.5% and a separate intraocular data coil were employed for this system [14]. The two intraocular power and data coils were arranged in a co-planar fashion to save space due to surgical consideration. An implant mechanical model, i.e., a real device but without real IC chips, connected with dummy chips, discrete components (i.e., capacitors, inductors, and resistors) and two intraocular coils was optimized for component

placement and surgical insertion into an eye. The maximum surgically allowable pulling force of the proposed epiretinal implant was measured using creep test by a DMA machine to be 8N, which provides a large safety margin for surgery. Note that the following work is ongoing for a real implant with working IC chips. The IC chips are independently developed by Manuel Monge et al. from the Mixed-mode Integrated Circuits and Systems group at Caltech. Details of the chip was published in ISSCC 2013 [15]. The packaging scheme for the 1024-channel retinal IC chip was also proposed and demonstrated with parylene flex technology. With suitable thickness on the stimulating electrode area, the surgical mockup can be successfully implanted in a dog's eye.

Figure 4.3. (a) Normal vision; (b) Blurry central vision for AMD patients; (c) Tunnel vision for RP patients.

4.2 Lifetime Study and Analysis

MEMS technology has been used more and more on biomedical application for neural prosthetic implantation [16-17]. These devices, however, will have to endure harsh and corrosive body fluids [18]. Therefore, biostable and hermetic-like packaging is needed to protect the implant. This work reported the package reliability of parylene-based retinal implant using active (i.e., with electrical signals applied) and accelerated lifetime soaking test in saline. Commercial amplifier chips, dummy conduction chips, and discrete components were tested and the failure modes were examined. It was found that the proposed parylene-metal-parylene flexible composite sandwich layers indeed have

longer lifetime than traditional inflexible silicone-parylene combination. In addition, the chip size effect on lifetime was observed that smaller chips have longer lifetime under the same protection.

4.2.1 DEVICE DESIGN, FABRICATION, AND INTEGRATION

Commercial amplifier chips, discrete components, and resistor chips were first integrated and packaged, as shown in Figure 4.4, before soaking test to estimate the lifetime at body temperature. Among them, commercial amplifier chips with transistors belong to the active component, and the discrete components and resistor chips belong to the passive components. They are the crucial components of the retinal implant system. Therefore, how we protected these components will affect the lifetime of the whole system tremendously.

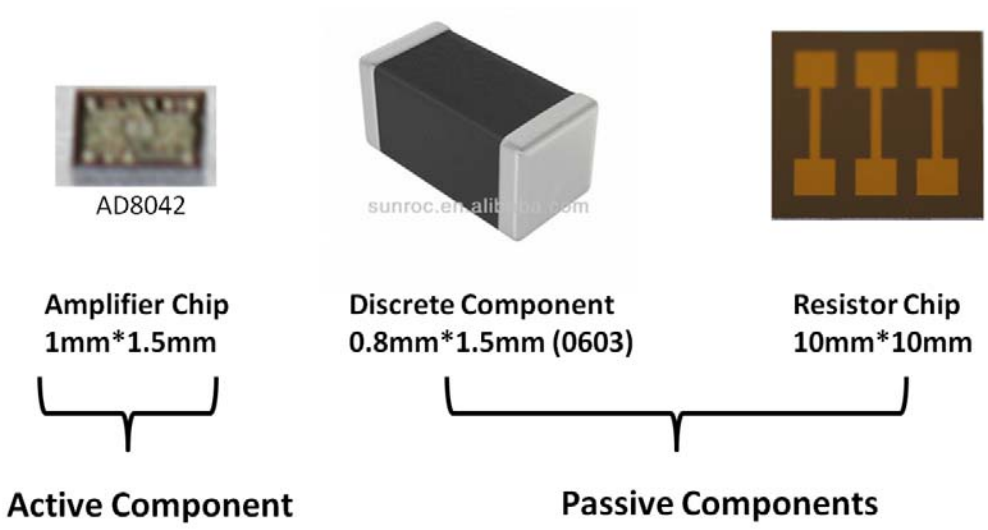


Figure 4.4. Commercial amplifier chips, discrete components, and resistor chips were first integrated and packaged before soaking test.

Commercially available amplifier bare dies (AD8042), with die size (mils) 45×65, were used to be packaged and tested with our technology. In order to handle and integrate the small bare dies, a

parylene pocket [19] structure on parylene substrate was designed and fabricated, as shown in Figure 4.5. First, 5 μm of parylene-C was deposited on the HMDS treated silicon wafers as the bottom substrate of the pocket. Sacrificial photoresist of 1 μm was coated on the bottom parylene-C substrate and patterned by photolithography process to create a sacrificial area to accommodate the bare dies. After cleaning by diluted hydrofluoric acid, another 5 μm parylene-C was deposited to encapsulate the sacrificial layer and serve as the base layer for metal deposition. Ti/Au (0.02/0.3 μm) metal combination was then patterned on parylene-C layer by lift-off process for electrical connection by e-beam evaporation. A final and top parylene-C layer of 5 μm was then deposited to complete the sandwich structure. Electrodes and device outlines were opened by oxygen plasma to finish the fabrication. Figure 4.6 showed the schematics of the process flow to demonstrate how to open the pocket and insert the chip. After the device releasing from wafer in DI water, sacrificial photoresist was first dissolved in acetone to create a space for the small amplifier chip. The pocket can be then opened by a tool like a spatula, and the chip can be successfully inserted into the pocket. Wafer dicing tapes can be applied to temporarily fix the pocket device so the pocket can be opened from the bottom substrate. Figure 4.7 showed the real pictures of each step. After the chips were inserted into the pocket, the metal pads on the chip were then aligned with the metal bonding pads on the pocket structure under microscope. An alignment accuracy of around 10 μm can be achieved, which is more than enough for bonding pads with a size of 110 μm × 110 μm. Conductive epoxy adhesive (MG Chemicals) was used and manually applied on top of the pads individually using needles to make the electrical and mechanical connection, as shown in Figure 4.8. In order to measure the signal, five small bonding pads were needed to be connected well. Wires were also connected to the pre-designed through holes on metal layers by conductive epoxy for external functional testing. Power supply and function generator were then connected to the pocket devices and “active” signal can be constantly monitored using an oscilloscope (HP 54503A). The mean time to failure (MTTF) of this system is defined as the time when the signal is lost.

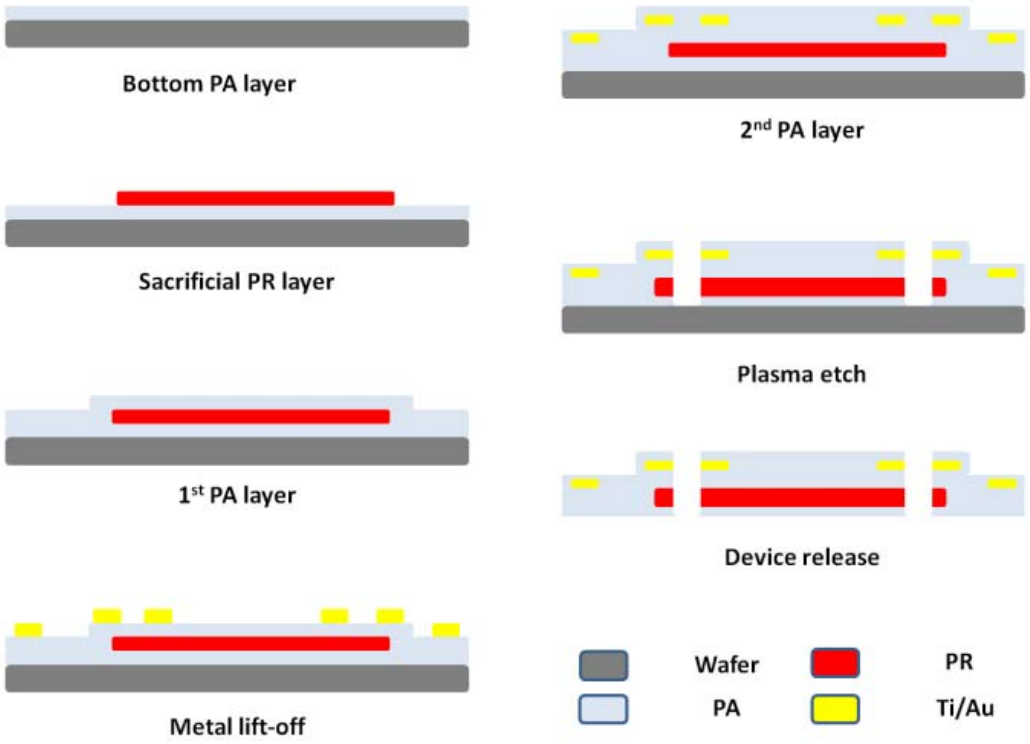


Figure 4.5. Fabrication process of the parylene-C pocket structure. The sacrificial area is designed to be 2 mm×2 mm to accommodate the bare die (1.6mm×1.1mm×200 μm) and it leaves some space for chip insertion and movement. The pocket structure can provide support to the chip to make alignment.

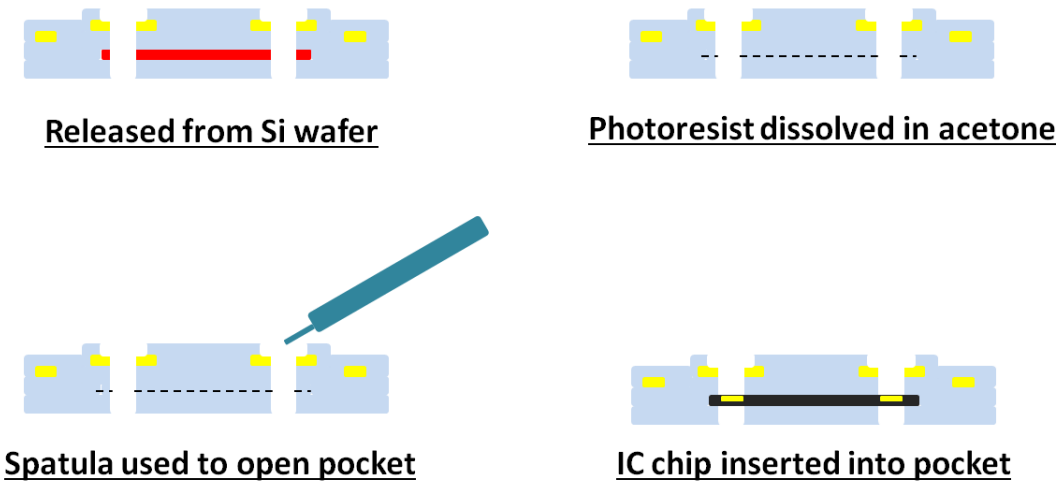


Figure 4.6. Schematics of the process flow to show how to open pocket and insert chip.

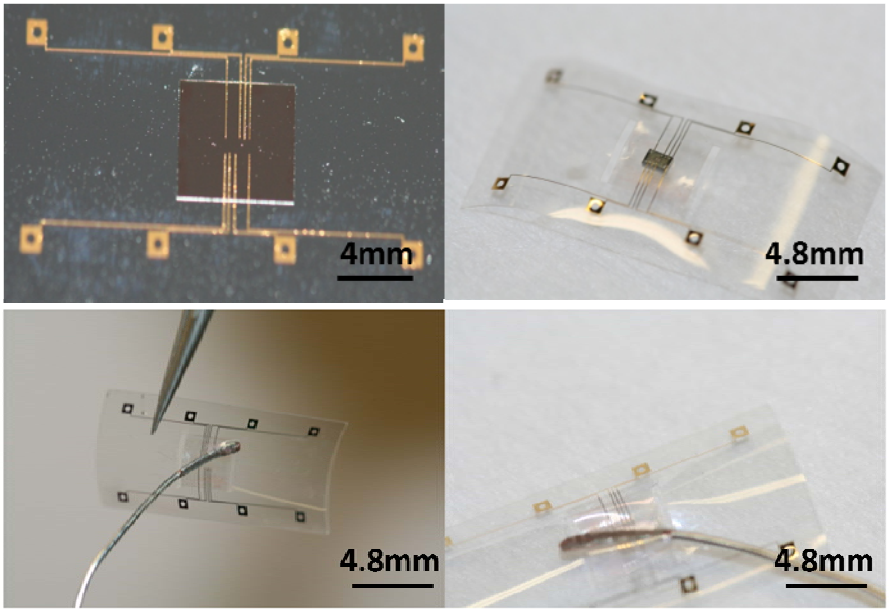


Figure 4.7. Parylene pocket is opened by spatula after releasing the sacrificial photoresist. With wafer dicing tape as a fixation substrate, the pocket becomes easier to open.

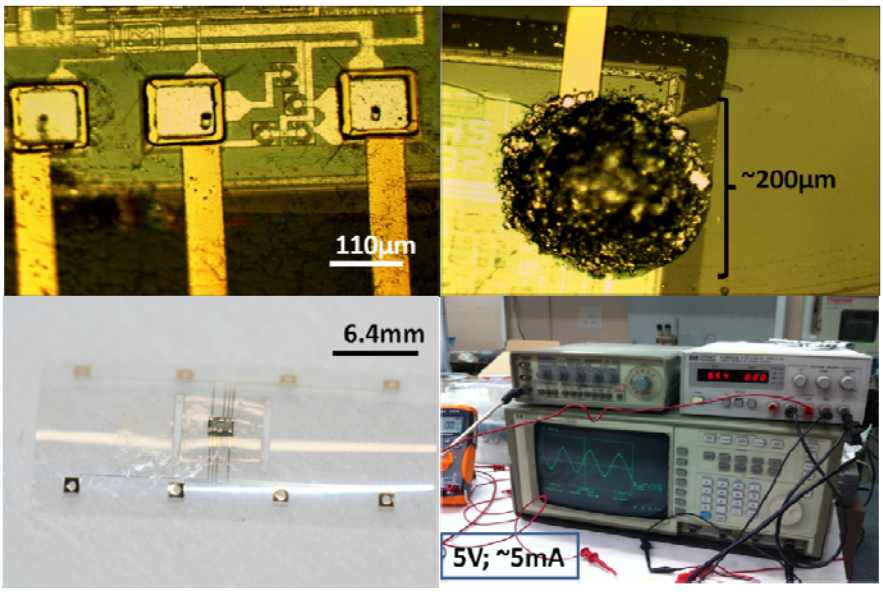


Figure 4.8. (Top left) A chip is inserted and aligned; Alignment accuracy of 10µm can be achieved. (Top right; bottom left) Conductive epoxy is applied to make connection; the size of conductive epoxy drop is 200µm in diameter. (Bottom right) Signal is monitored by oscilloscope.

Discrete components, such as resistors, inductors, and caps, were also packaged to build a series RLC circuit. Because the size and bonding pads of the discrete components are much bigger than amplifier bare dies, no pocket structures were needed for this integration. The fabrication process of this device and integration of this system can be seen here [1]. Figure 4.9 showed the measurement result with the following parameters: resistance is negligible; capacitance is 0.91 μF; inductance is 100 pH. The resonant frequency can be calculated by the following equation:

$$w = 2\pi f = \frac{1}{\sqrt{L \times C}} \qquad [4\text{-}1]$$

The measurement result of resonant frequency as a functional indicator with the impedance analyzer was around 13.7 MHz, while the theoretical resonant frequency was calculated to be 16.684 MHz. The connecting wires and conductive epoxy contributed to the offset. The mean time to failure (MTTF) of this system is defined as the time when the resonant frequency can't be measured anymore.

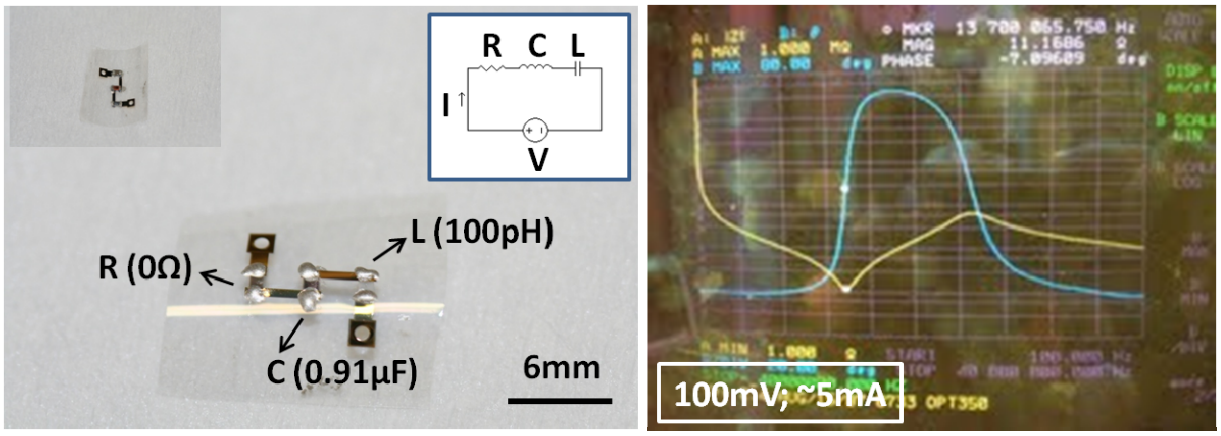


Figure 4.9. (Left) Top and back side of the series RLC circuit built by discrete components. (Right) Resonant frequency is measured by impedance analyzer.

Dummy conduction chips with different sizes were designed to compare the "size effect" on

lifetime, as shown in Figure 4.10. The fabrication process of the parylene device and the integration are the same as those for discrete components. Figure 4.10 also showed the measurement setup of active soaking test for dummy conduction chip. Power supply, multi-meter, and dummy conduction chip soaked in saline were arranged in series. The current was continuously sent in and the change of the current was constantly monitored by multi-meter to calculate the changes of resistance. The MTTF of this system is defined as the time when 50% change in the line resistance happens.

Figure 4.11. showed the line resistance v.s. time of samples coated by 40μm parylene-C only soaked in high temperature saline solution. The subset shows the difference of chip size of dummy conduction chips. The soaking data showed that chips with smaller size under the same protection have longer lifetime. Besides, at lower temperature, the integration also has longer lifetime as expected.

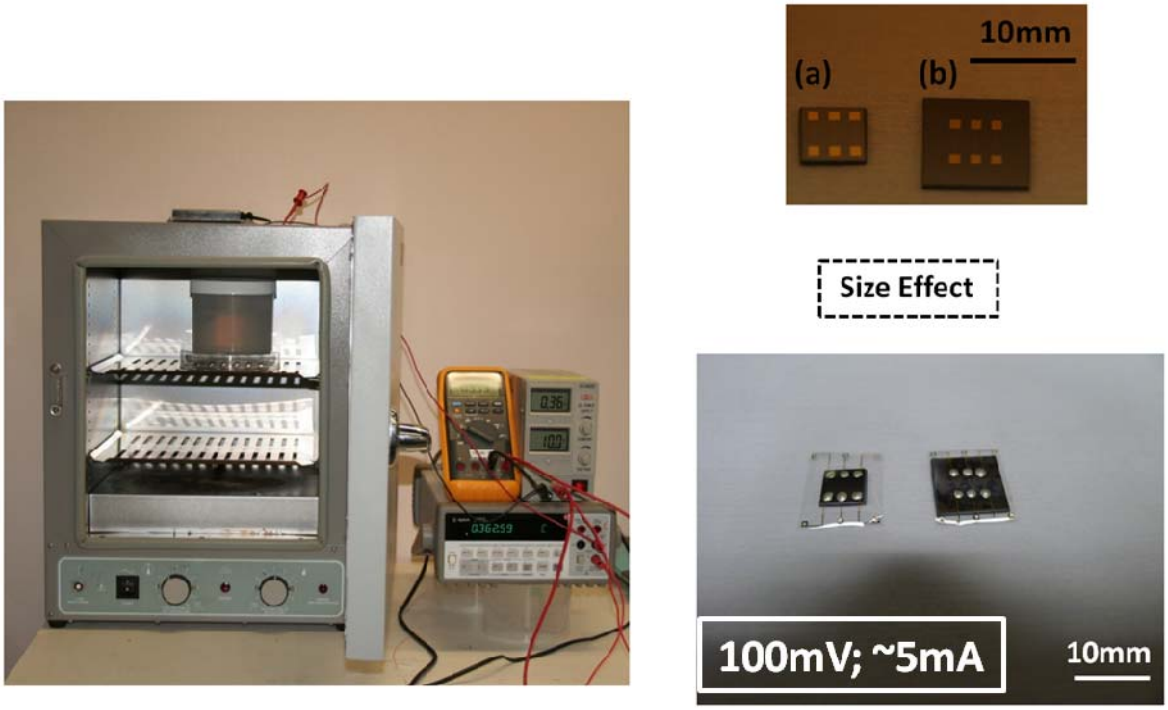


Figure 4.10. Measurement setup of active soaking test for dummy conduction chip. Power supply, multi-meter, and dummy conduction chip soaked in saline are arranged in series. Door is opened to

show the setup inside.

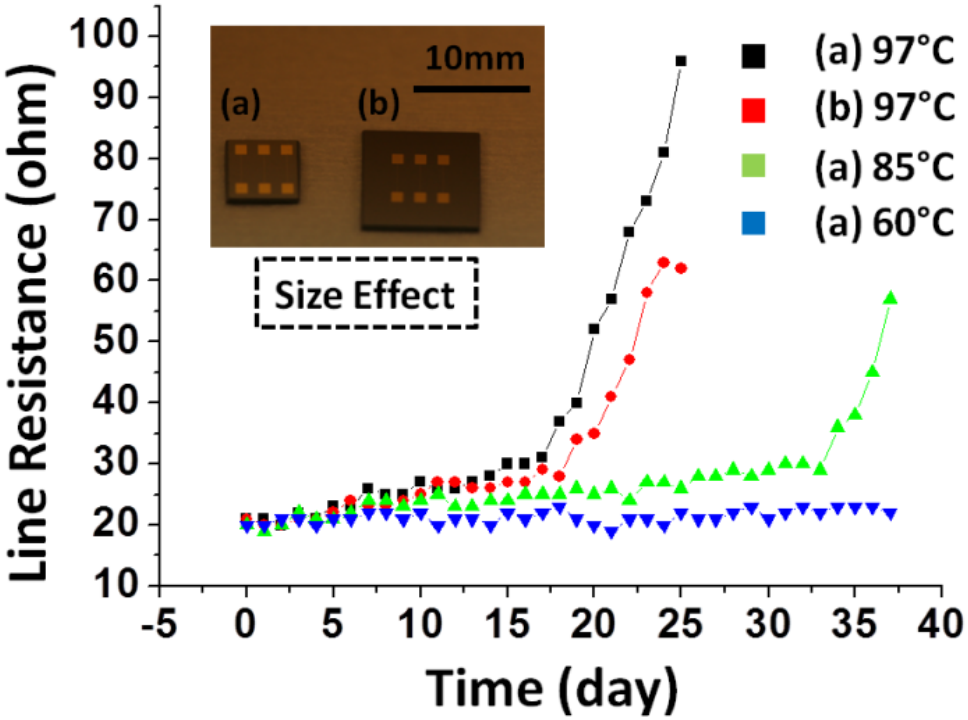


Figure 4.11. Line resistance v.s. time of samples coated by 40μm parylene-C only soaked in high temperature saline solution. The subset shows the difference of chip size of dummy conduction chips.

4.2.2 EXPERIMENTAL RESULTS

Water vapor permeation is one of the main causes of failure in parylene devices when implanted. In order to create better protection, bio-compatible metals, such as Titanium (Ti), Gold (Au), and Platinum (Pt) combination, were chosen as the metals in parylene-metal-parylene flexible composite protection layers to protect devices from water vapor corrosion. WVTR of 0.5μm metals with high flexibility is lower than that of 5mm-thick silicone by theoretical calculation. Advantageously, the device was still highly flexible after this sandwich layer protection, as shown in Figure 4.12. However, extra care needed to be taken of the metal coating. Samples need to be fixed at around 45º

to the metal source and both sides need to be coated in turn to create continuous metal film to ensure good encapsulation. In addition, the holder must be constantly rotated to create uniform metal film.

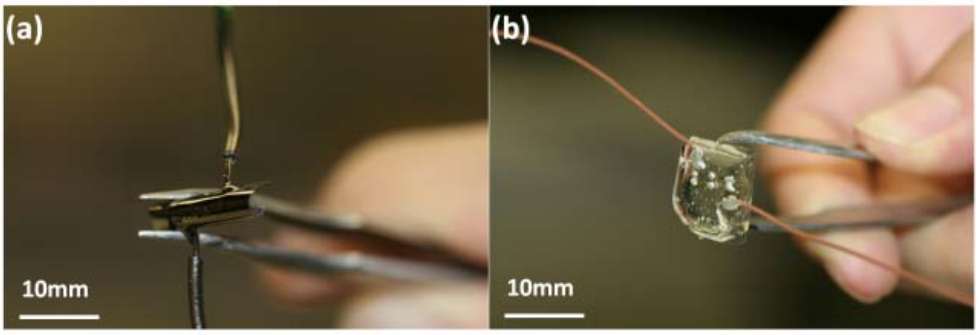


Figure 4.12. (a) After sandwich layer protection, the device is still highly flexible. (b) Device becomes inflexible after coating with thick silicone; thickness needs to be more than 5mm.

Devices without any protection, with 40 μm parylene-C-only protection, and with parylene-C coated bio-compatible silicone were also prepared for comparison, as shown in Figure 4.13 (Schematics), and Figure 4.14 (Real picture). Samples were then tested under active soaking conditions. All tests were performed in saline (0.9wt% NaCl solution), which is a typical to mimic body fluids. The saline solution was replaced every three days to maintain its constant concentration. In the active soaking tests, different failure mechanisms, as shown in Figure 4.15, were observed on samples such as bubbles on parylene, corrosion of metal pads, interface delamination, and corrosion of conductive epoxy which will increase the line resistance to fail the connection and functionality of the whole system. Among them, corrosion of metal pads and conductive epoxy were found to be the major failure modes which can gradually result in the open connection. For the samples without protection soaked in saline, after the power supply was connected, the breakdown hole on the thin parylene was first observed. It is probably because the high electric field concentration in area which contains particles and defects that the electrochemical reaction was accelerated at this defect point. The water vapor can penetrate the thin parylene layer of device itself to damage the exposed metals

very quickly, especially under a bias field [6], as shown in Figure 4.16. Therefore, the corrosion of the metals embedded in parylene is the main reason of failure in this kind of devices. For the samples with thick parylene and other protection, uniform bubbles around the whole device were first observed and water vapor gradually diffused through the protection to attack the device, as shown in Figure 4.17. Corrosion of conductive epoxy also contributed to the failure in these samples. For some samples with bad parylene coating protection, water vapor can go through very easily. Therefore, failure mechanism is the same as the samples without protection. Samples with better protection (lower WVTR) were observed to have longer lifetime. Besides, chip with smaller size has longer lifetime under the same protection. Table 4.2 showed that the passive components, such as dummy conduction chip and discrete components, under proposed protection can survive in 97ºC saline solution for more than 44 days. For the active component, amplifier chip, the lifetime is around 37 days. The reason of shorter lifetime comes from the smaller bonding pads which are easier to be corroded by saline, hence fail faster the connection.

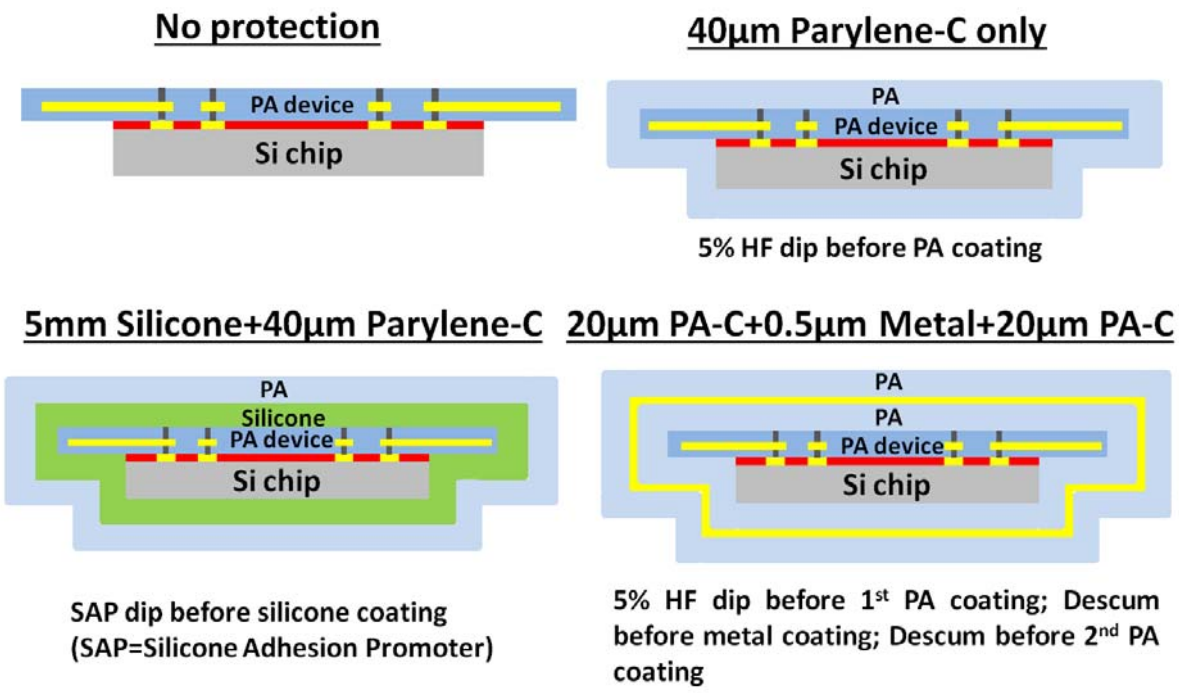


Figure 4.13. Schematics of proposed packaging scheme and other protection for comparison.

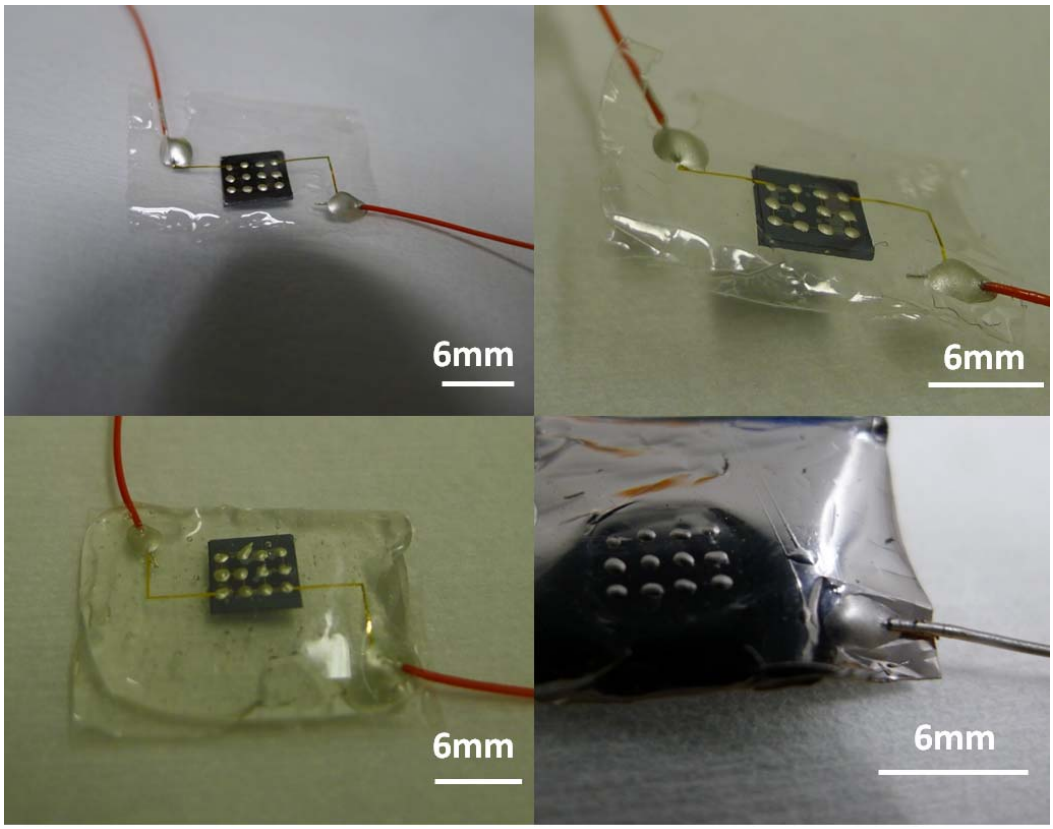


Figure 4.14. High-density multi-channel chip integration protected by different packaging schemes. (Top left) No protection; (Top right) 40 µm parylene-C only; (Bottom left) 5mm silicone + 40 µm parylene-C; (Bottom right) 20 µm parylene-C + 0.5 µm metal + 20 µm parylene-C.

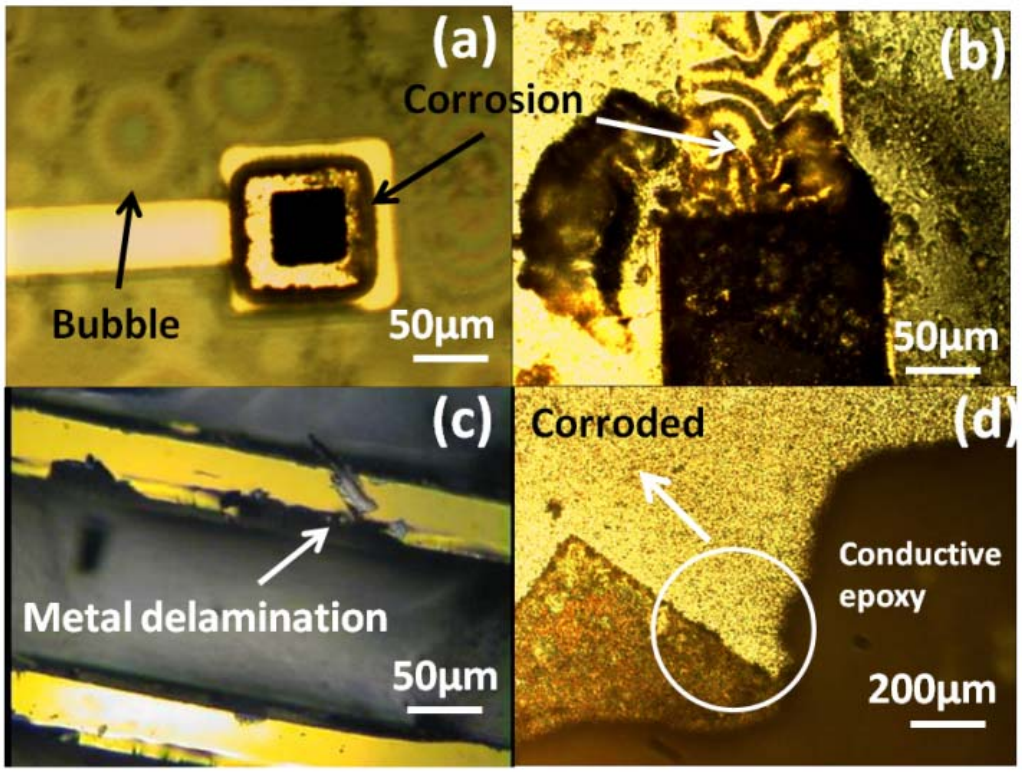


Figure 4.15. Observed failure modes, including bubbles and corrosion, on parylene devices (a), corrosion of sandwiched metals (b), delamination of metal traces on dummy chips (c), and corrosion of conductive epoxy (d), respectively, are found after soaking.

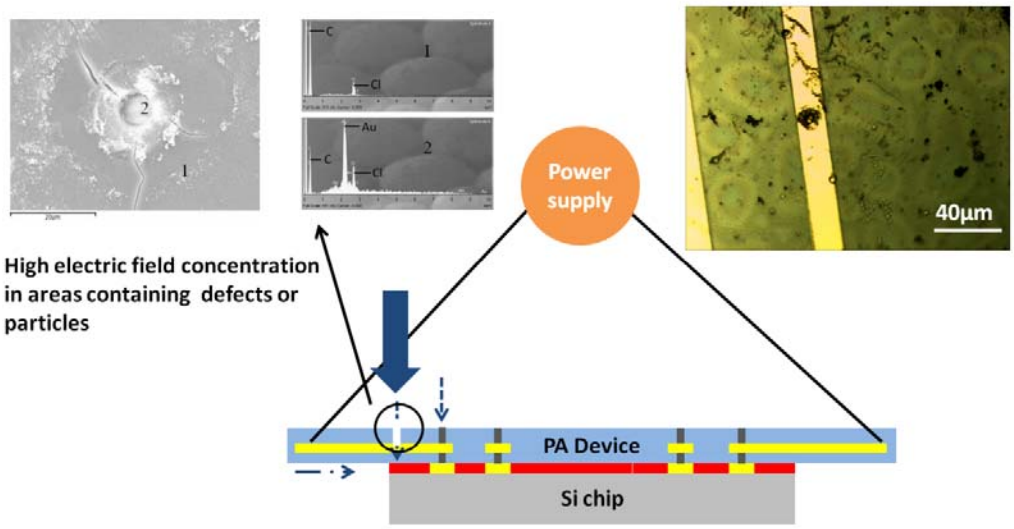


Figure 4.16. Samples without protection, water vapor can penetrate the thin parylene layer of device itself to damage the metals very quickly, especially under a bias field [6].

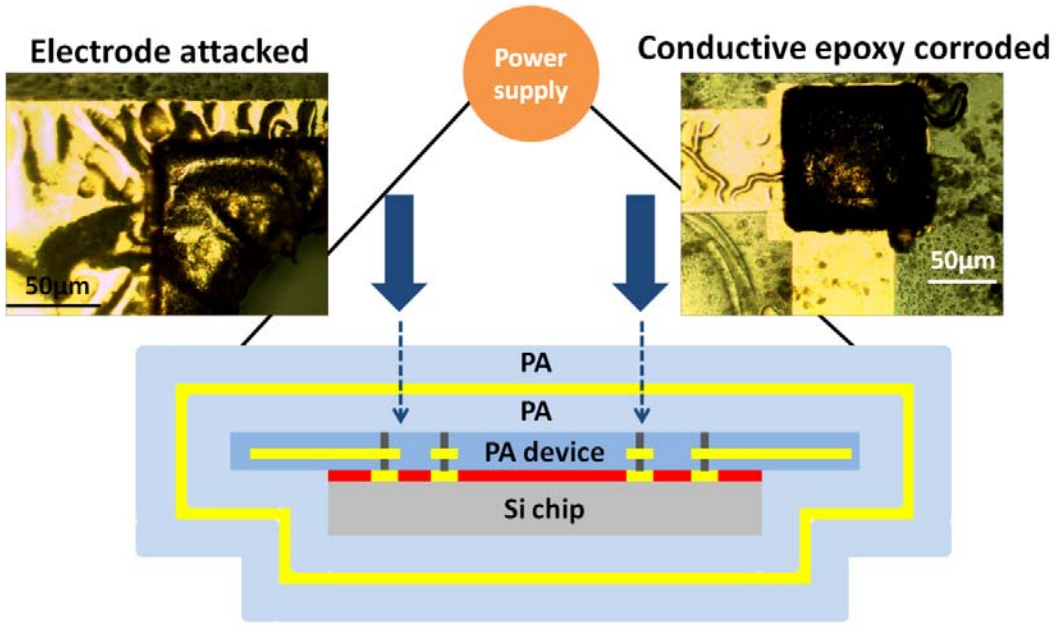


Figure 4.17. Samples with thick parylene and other protection, uniform bubbles around the whole device are first observed and water vapor gradually diffuses through the protection to attack the device.

The approximated Arrhenius relationship [2] was used here to extrapolate MTTF at body temperature and is expressed:

$$MTTF \sim A exp(-\frac{Ea}{kT}) \quad [4\text{-}2]$$

Where A is the pre-exponential constant; Ea (eV) is the activation energy; and k is the Boltzmann's constant. The failure modes are based on the serious corrosion of metal pads and conductive epoxy. According to the Arrhenius relationship, the lifetime translates to more than 7.5 years, and 6.7 years (a desirable target) for passive and active components of survival period in human body temperature of 37ºC. This new packaging structure was proved to be an acceptable choice for implantable devices.

Table 4.2. MTTF of various tested samples are recorded and calculated to estimate the lifetime at 37°C under different protections.

Samples	Protection	97°C (day)	85°C (day)	60°C (day)	Ea (eV)	37°C	Flexibility
Dummy conduction chip	A	1.6	2.5	5	-0.41	20 days	YES
	B	17	34	100+	-0.66	2.5 years	YES
	C	41	84	100+	-0.68	7 .1 years	NO
	D	44	90	100+	-0.68	**7.5 years**	**YES**
Commercial amplifier chip	A	1.5	2.4	7	-0.46	24 days	YES
	B	15	28	100+	-0.59	1.5 years	YES
	C	35	69	100+	-0.64	4.7 years	NO
	D	37	78	100+	-0.70	**6.7 years**	**YES**
Discrete components	A	1.6	2.8	11	-0.53	41 days	YES
	B	19	39	100+	-0.68	3.3 years	YES
	C	40	83	100+	-0.68	6.9 years	NO
	D	46	95	100+	-0.69	**8.1 years**	**YES**
A: No protection B: 40µm PA C: Silicone+40µm PA D: 20µm PA+0.5µm Metal+20µm PA							

From the results of the previous experiment with parylene-metal-parylene packaging protection, for the samples with thick parylene and other protection, it was found that the dominating failure mode came from the water vapor diffusion through the thick protection barrier first. Then, the electrodes and conductive epoxy got corroded by the water vapor and thus the failure happened. It is anticipated that the lifetime will be extended if the packaging layer is even thicker (lower WVTR) which will take more time for the water vapor to diffuse through. However, heat dissipation might be another new issue with thicker protection because parylene has bad thermal conductivity. In view of this issue, a new proposed packaging scheme with a thin glass on top of the device was then proposed. Glass slide has very low WVTR and very high thermal conductivity, as shown in Table 4.3, both of them are beneficial for the protection on small implantable devices. Besides, in order to better simulate the real condition of the retinal IC chip integration, high-density multi-channel dummy chips were designed and fabricated, as shown in Figure 4.18. The corresponding parylene flex was also designed accordingly. After aligned under microscope, integration was done by conductive epoxy squeegee technique and the resistance was monitored as a functional indicator.

Table 4.3. Thermal conductivity of the materials.

Material	Thermal Conductivity-K-W/m.K
Air	0.024
Al	205
Si	149
Cu	401
Glass	1.05
Gold	310
Plastic	0.03
Pt	70
PA-C	0.072
Teflon	0.23
Silicone	0.7~3

1 W/(m.K) = 1 W/(m.°C) = 0.85984 kcal/(hr.m.°C) = 0.5779 Btu/(ft.hr.°F)

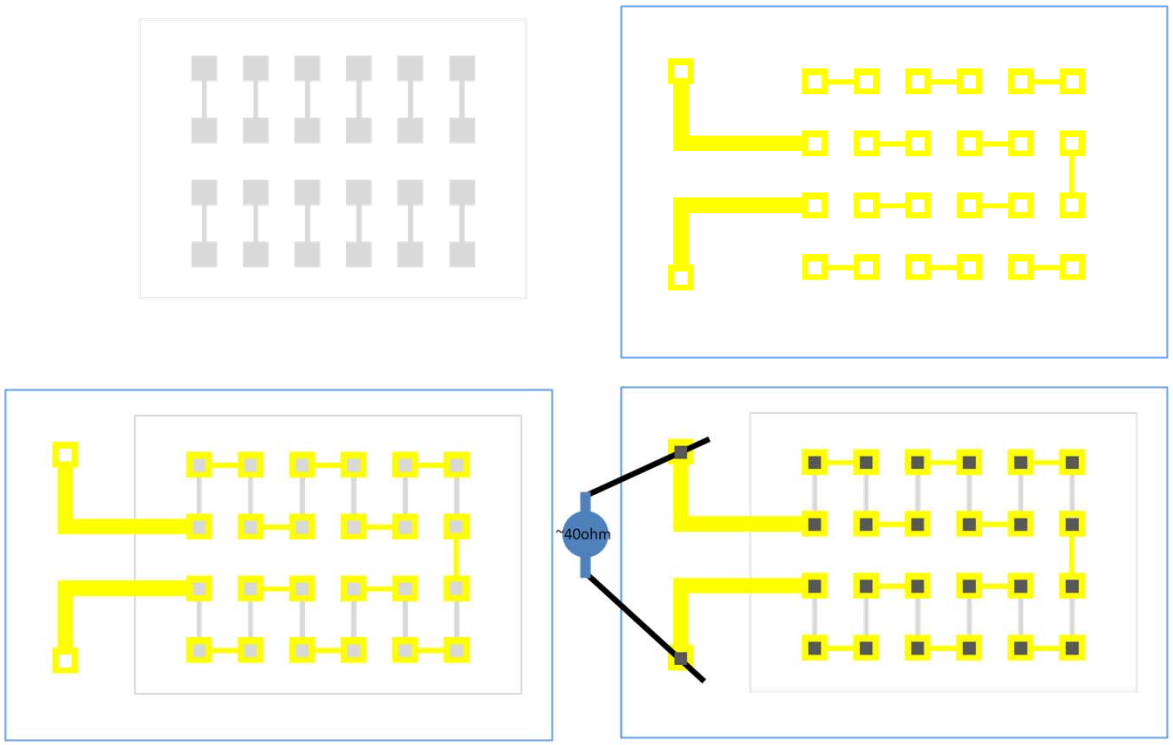


Figure 4.18. Concept of high-density multi-channel chip integration and testing setup. (Top left) High-density multi-channel dummy chip; (Top right) Corresponding parylene flex; (Bottom left) Chip integration by squeegee process; (Bottom right) Testing setup.

The thin glass slide (~100 µm) was first cut by dicing saw to get the desired size. Then, it was attached on the top of the device to cover the electrodes and conductive epoxy by adhesives. Additional adhesives were expected to cover the whole device, followed by another parylene-C coating. In this protection scheme, three different interfaces including glass-adhesive, parylene-adhesive, and silicon-adhesive were generated and the most suitable adhesives to these interfaces needed to be well studied and selected, as shown in Figure 4.19. Biocompatible epoxy and biocompatible silicone were selected as the adhesive to apply on different interfaces with and without surface treatments and undercut rates in high temperature (97°C) saline solution was observed and recorded, as shown in Figure 4.20. It is found that biocompatible silicone has very low undercut rate

to all the substrates treated by silicone adhesion promoter (SAP). Besides, silicone is still more flexible than epoxy comparatively. Therefore, biocompatible silicone was selected as the adhesives in this packaging scheme.

Figure 4.21 showed the schematic and real picture of the parylene device with new packaging scheme with a thin glass on top of the device. Accelerated lifetime active soaking test was also performed on this sample, and the result showed that water vapor cannot go through the glass to attack the electrodes and corrode the conductive epoxy after diffusion through other protection layer. The only way to damage the sample was to undercut along the interface between thin glass slide and parylene device with a very slow rate, as shown in Figure 4.22. The recorded lifetime is thus extended to more than 10 years which is a desirable target, as shown in Table 4.4. Even longer lifetime can be expected once the size of glass slide was increased and the better interface treatment was applied.

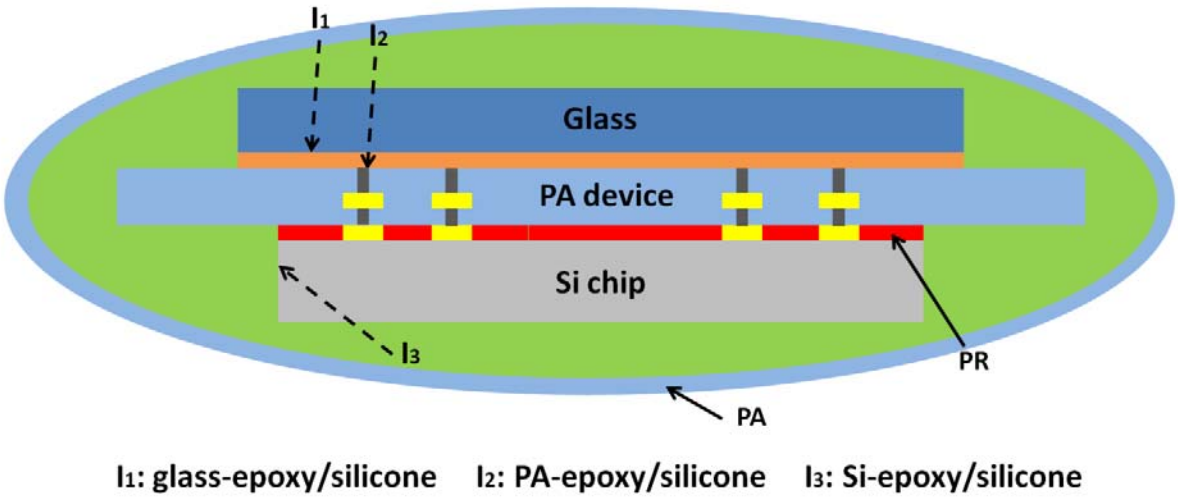


Figure 4.19. New packaging scheme with a glass on top for further protection. Adhesive was used to cover the whole device. Adhesives to three different interfaces including glass, parylene, and silicon need to be well selected.

Si substrate			
		N	SAP
UNDERCUT (um/day)	Epoxy	36.6	4.3
	Silicone	10.2	1.9
Glass substrate			
		N	SAP
UNDERCUT (um/day)	Epoxy	20.5	5.6
	Silicone	11.3	2.2
PA substrate			
		N	SAP
UNDERCUT (um/day)	Epoxy	10.4	3.5
	Silicone	29.7	3.4

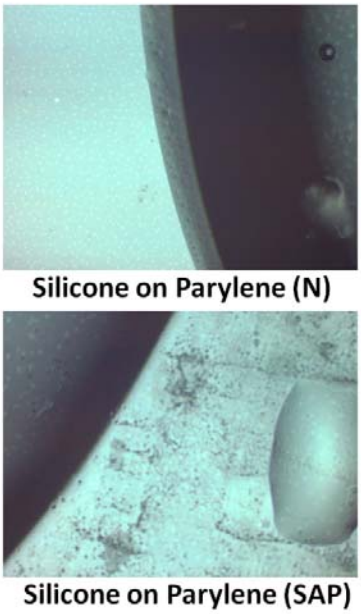
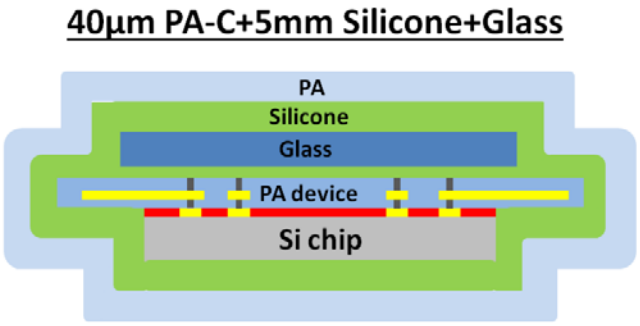


Figure 4.20. Investigation of adhesives to different interfaces by undercut observation before and after interface treatments. N: no treatment; SAP: silicone adhesion promoter.



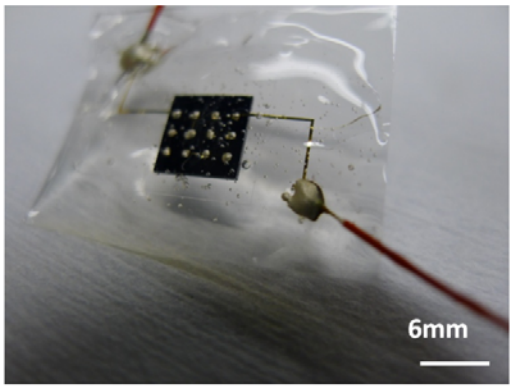


Figure 4.21. (Left) Schematic of the new packaging scheme. (Right) High-density multi-channel chip integration protected by new packaging scheme.

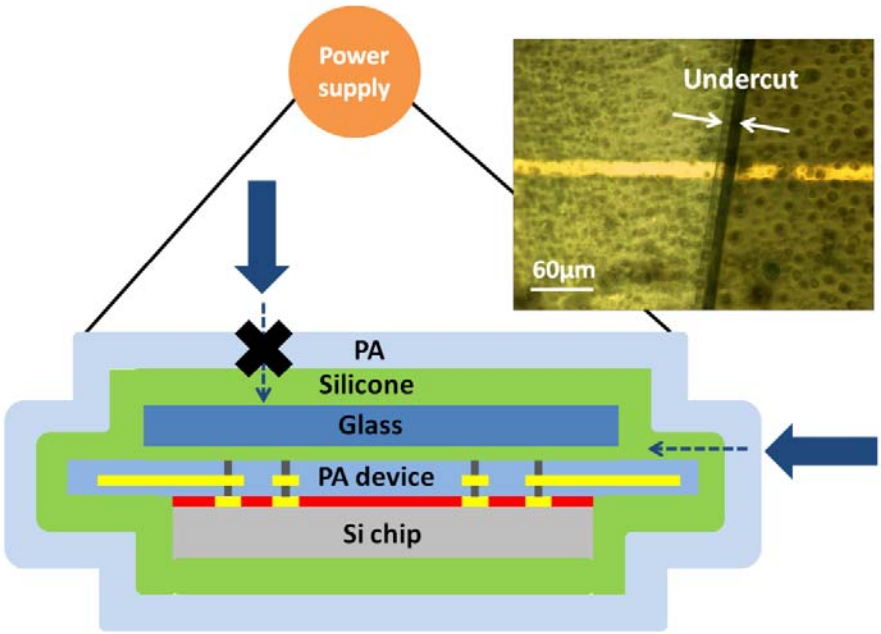


Figure 4.22. Failure mode on new packaging scheme: Saline can't diffuse through the glass directly to attack the electrodes and corrode the conductive epoxy. It can only slowly go through the interface.

Table 4.4. MTTF of various tested samples were recorded and calculated to estimate the lifetime at 37°C under different protections.

Protection	97°C (day)	85°C (day)	Ea (eV)	37°C
A	1.7	2.6	-0.40	20 days
B	15	31	-0.69	2.7 years
C	40	82	-0.68	6.9 years
D	42	87	-0.69	7.7 years
E	59	107	-0.68	10.3 years
A: No Protection B: 40µm PA C: 5mm silicone+40µm PA D: 20µm PA+0.5µm Metal+20µm PA E: 40µm PA+5mm silicone+glass				

4.3 Surgical Mockup Design and *In Vivo* Test

4.3.1 512-Channel Chip

4.3.1.1 THE 3-COIL WIRELESS POWER TRANSFER

To wirelessly power the whole epiretinal system, a 3-coil wireless power transfer system was used as shown in Figure 4.23. The flexible and foldable MEMS intraocular foil receiver coil, L3, features a Q factor of 24 (at the operating frequency of 10MHz), a diameter of 10mm and a weight of 10mg in saline [20]. This coil was placed inside the lens capsule. The intermediate coil, L2, is a hand-wounded Litz buffer coil to enhance coupling coefficients κ12 and κ23 due to its high Q factor and close proximity to receiver coil. Because of the additional intermediate coil, the overall power transfer efficiency of the design was measured to be as high as 36.5% with one inch separation between the primary transmitter coil, L1, and the intraocular receiver coil, L3.

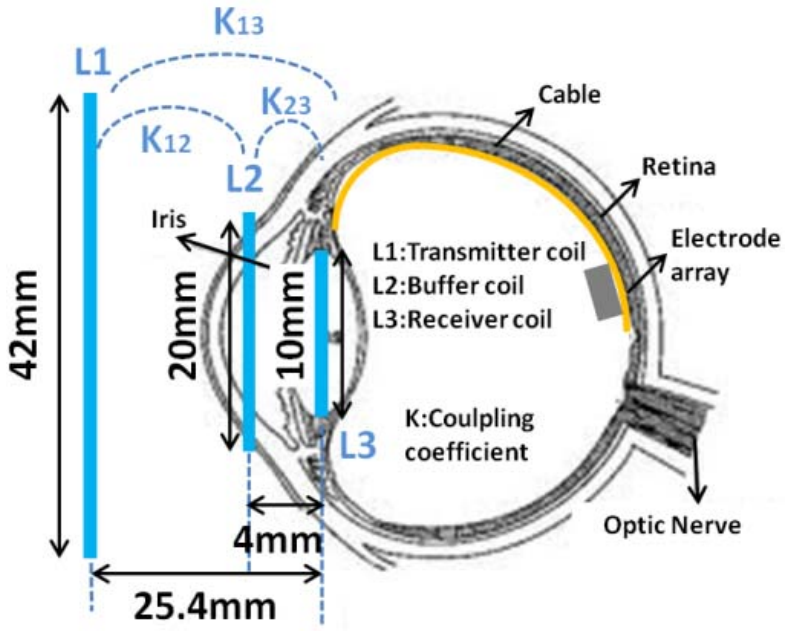


Figure 4.23. The 3-coil scheme for inductive power transfer.

4.3.1.2 SIMULATION OF THE INTERFERENCE BETWEEN COILS

For surgical and placement consideration, it is the best to have the power and data coils in a co-planar fashion. However, the co-planar placement has the largest interference issue between the power and data coils. To analyze the interference between power and data coils, a model of the coil system was built using high frequency structural simulator (HFSS), as shown in Figure 4.24. Coil 1 is defined as the receiver coil of the data coil, with 3 mm, 5 mm, and 7 mm inner diameter; coil 2 is defined as the receiver coil of the intraocular power coil, with 10mm inner diameter; coil 3 is defined as the transmitting data coil, with 20 mm in diameter; coil 4 is defined as the transmitting power coil, with 42mm in diameter. The thickness of the coils is 2 mm and the separation between the receiving and transmitting coils is set to be one inch.

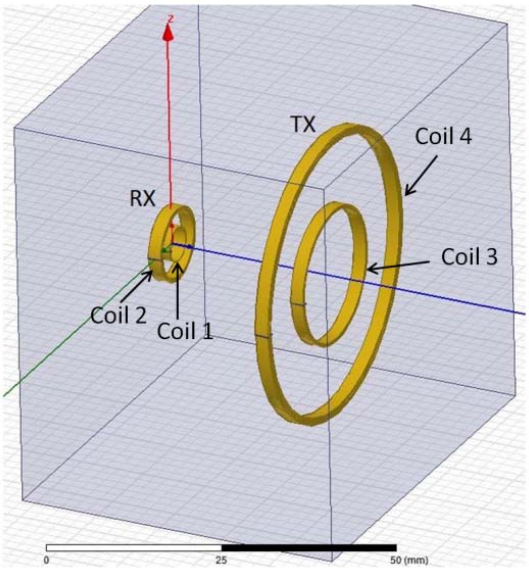


Figure 4.24. A model of the coil system is built using HFSS for the coil interference analysis.

Figure 4.25 showed the simulation result. Scattering parameters (S-parameters), describing the

electrical behavior of linear electrical networks, from coil 4 to coil 1 and from coil 3 to coil 1 were simulated for us to estimate the interference between power and data coils. The resonating capacitors are 30 pF for coil 1, 700 pF for coil 2 and coil 3, and 600 pF for coil 4. At the frequency of 160 MHz where the data coil operates, an interference signal at 10 MHz coming from the power coil will cause a 20 dB higher coupling compared to the data coil.

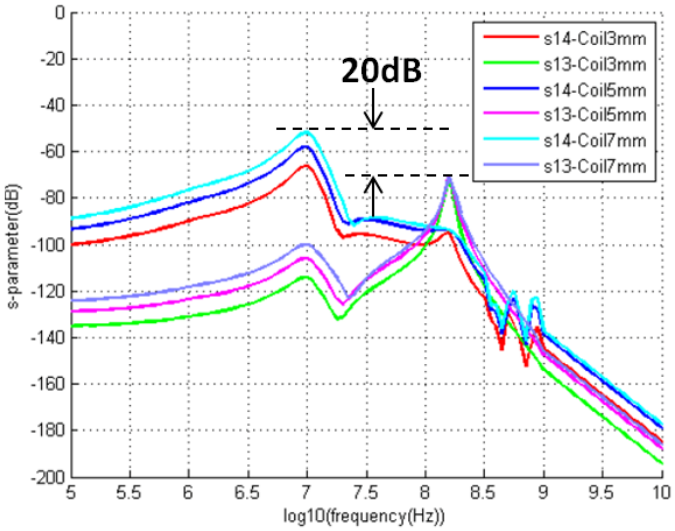


Figure 4.25. S-parameters from coil 4 to coil 1 and from coil 3 to coil 1 with different inner diameters of coil 1.

In order to reduce interference from the power coil to the data coil, two notch filters, as shown in Figure 4.26, were added to the circuit. The notch filters, built by RLC circuits, can decrease the coupling in the data path. They reduce the coupling at 10MHz (i.e., the power transfer frequency), making possible to demodulate data at 160 MHz. It is also possible to tune the resonant frequency to increase the gain at 160 MHz which will be better for data transfer. The only drawback is that 6 more extra discrete components will be added to the whole system. However, our surgical design can

tolerate this issue so that not too much volume will be added to the device.

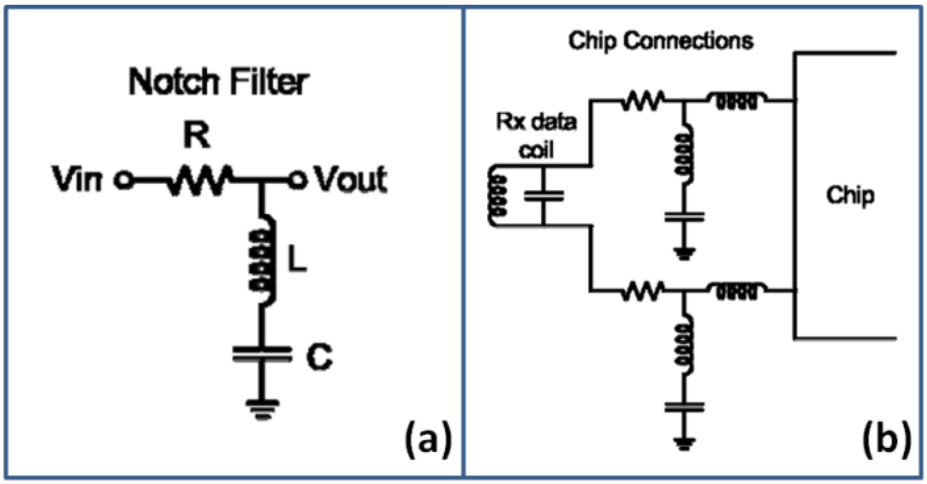


Figure 4.26. (a) A Notch filter. (b) Two Notch filters are connected to the system.

4.3.1.3 THE FLEXIBLE MECHANICAL MODEL

The surgical procedure for the insertion and fixation of the implant is very important. To this end, a parylene flex mechanical model was designed and fabricated, as shown in Figure 4.27, to be packaged with silicon chips, discrete components (including capacitors, inductors, and resistors), and coils. A mold was designed to house the silicon chips for one-time conductive epoxy squeegee connection process to increase the connection yield. All the discrete components were placed on a parylene flex tail. A single retinal tack hole (100 μm in diameter) and two suture holes (2mm in diameter) were also designed for the implant to be fixed on designated tissues inside eyeball. Biocompatible silicone was used for further protection after all the process [21]. Based on the high flexibility of the parylene flex implant and low interference between power and data coils with notch filters, the parylene tail can be wrapped around the chips and the coils can be put together in a co-

planar fashion, as shown in Figure 4.28, which will be beneficial for surgical insertion and placement. The packaging shown here is based on a two-chip master/slave architecture with two notch filters (built by 6 discrete components), and 17 discrete components. However, the final goal of on-going chip development is to have only one single IC chip and fewer discrete components.

The current mechanical model, as shown in Figure 4.29, has been tested for *in vivo* implantation at the Keck School of Medicine of the University of Southern California. The size of the model can fit the pig's eyeball well without damaging the tissues, and the part of the stimulating electrode can reach the retina.

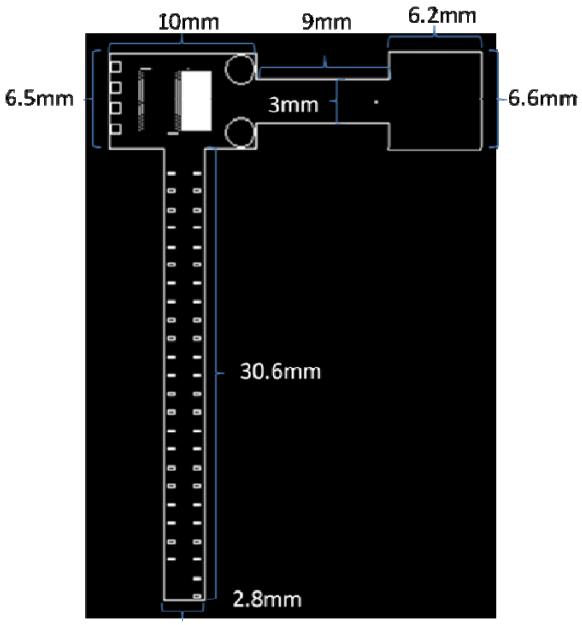


Figure 4.27. A parylene flex mechanical model for 512-channel retinal IC chip was designed and fabricated.

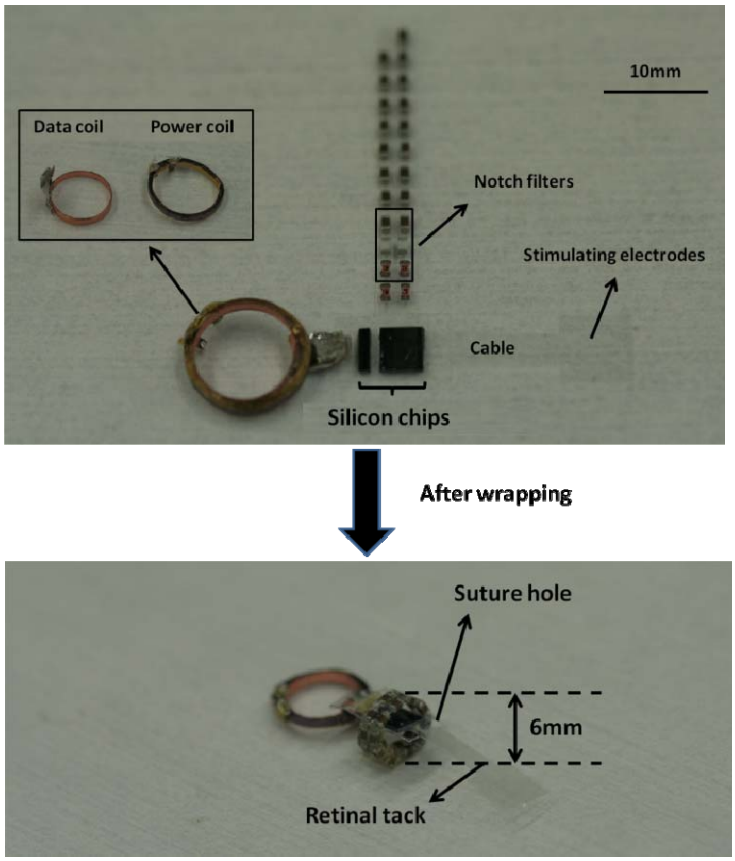


Figure 4.28. Demonstration of a parylene flex mechanical model before and after wrapping with silicon chips, discrete components, and coils.

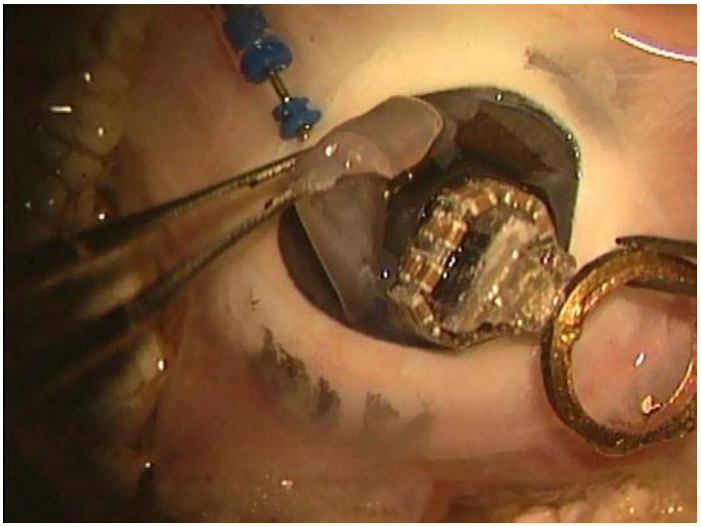


Figure 4.29. Successful in vivo implantation process in a pig's eye.

4.3.2 1024-Channel Chip

The 1024-channel retinal IC chip was designed by Dr. Wentai Liu's group in UCLA [22]. Based on the chip design, only 6 capacitors and one oscillator are needed to functionalize the whole system. Besides, the power and data coil can be placed in a concentric fashion without interference issue. Comparatively, the surgical mockup for this chip integration is more straightforward. The only concern on the mockup for this chip is how to well allocate the 1024 interconnections in the parylene interconnection with only 3 mm wide range.

Figure 4.30 showed the schematic design of the surgical mockup for the 1024-channel chip. If all the 1024 interconnections have to go through the 3 mm range, the pitch of less than 3mm needed to be achieved with single metal layer. The process is too difficult and unstable. Figure 4.31 showed the modified design that there are three ways for the 1024 connections to go through the interconnection area and the distribution and density can be much relaxed. After folding, the interconnection area is still 3 mm. Figure 4.32 showed the surgery procedure in a dog's eye. With the current design, the device was sitting on the retina nicely and the geometry of the device allowed the electrode array positioned on the retina at around 5 mm~8 mm away from optic nerves, as shown in Figure 4.33. In which, there are a bunch of ganglion cells to stimulate, and that position is still at the back of the eye (straight on the retina), which would allow surgeons easily to observe through the lens of the eye, and more easily to find out the device when doing the follow-ups (OCT, Ultrasound, and so on). Smaller incision is generally better as the bigger incision could change the pressure in the eye, and cause the difficulty in maintaining the ocular integrity, thus induce severe bleeding and retinal detachment. The size of the incision is similar to the diameter of the retina of the dog's eye, which is about 18-22 mm. For reference, the diameter of the pig's eye is about 20-23 mm, and that of human's eye is about 22-25 mm. For dog, the incision is exactly 3.5 mm away from the cornea. If incision is too close to

cornea, the surgical tool will hit the lens; if it's too far, the retina will be cut through easily. 3.5 mm is a space that allow the surgical tool to go through the eye between the lens and retina.

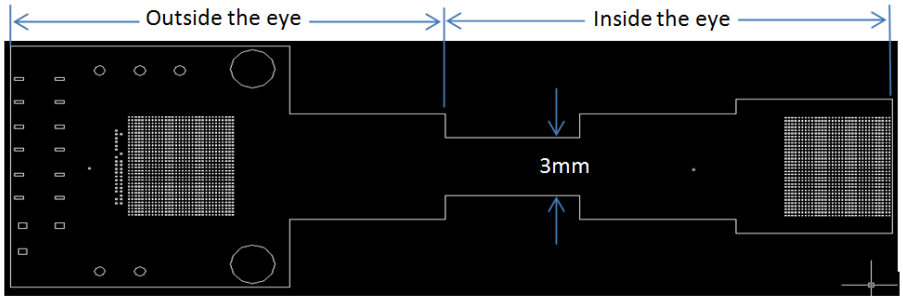


Figure 4.30. Schematic design of the surgical mockup for the 1024-channel chip.

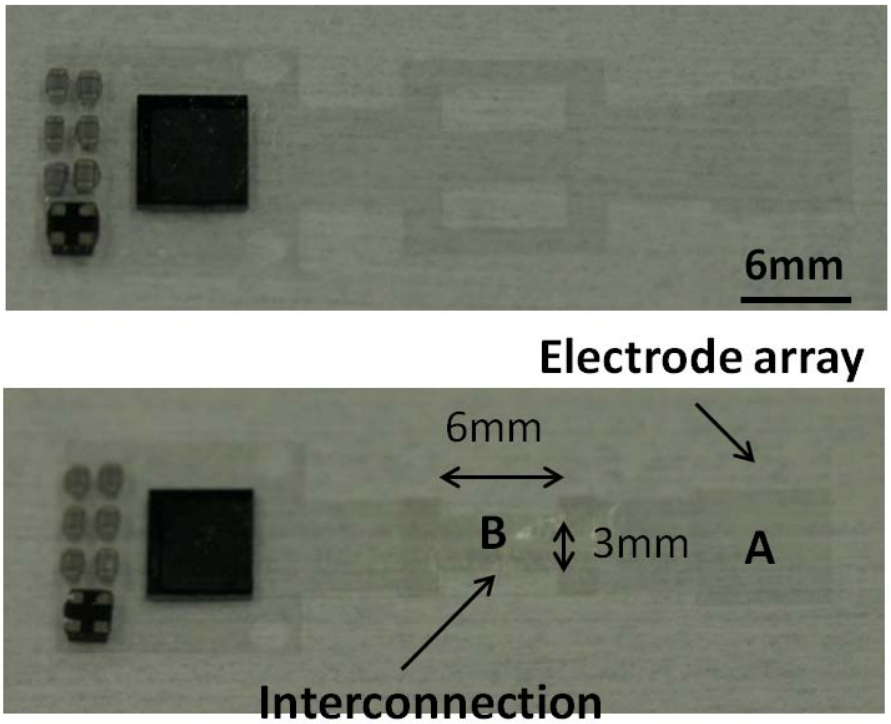


Figure 4.31. Parylene surgical mockup integrated with IC chip and discrete components before and after folding.

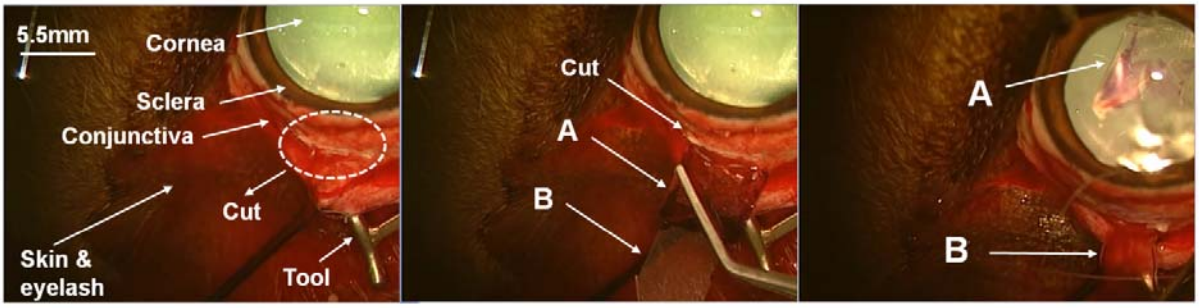


Figure 4.32. Successful in vivo implantation process in a dog's eye.

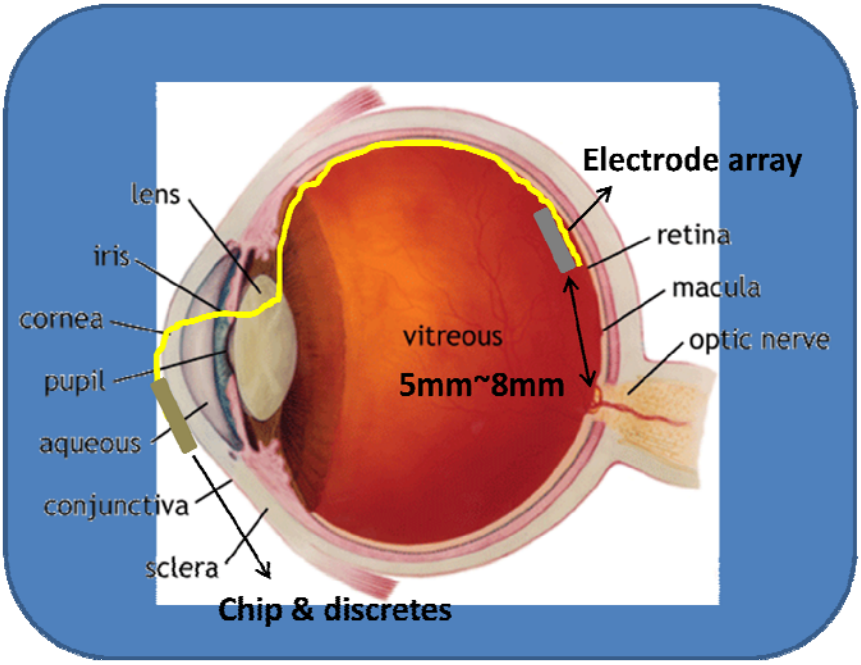


Figure 4.33. Schematic diagram to show that the electrode array was positioned on the retina at around 5 mm~8 mm away from optic nerves.

After successful in vivo implantation with parylene only surgical mockup in a dog's eye, we also fabricated real parylene device with metal conduction, as shown in Figure 4.34, integrated with retinal IC chip, discrete components, and coils, to do the implantation trial. Figure 4.35 showed the implantation process. The electrode was first folded a little bit to fit the size of the cut on eyeball,

which is around 2~3 mm. The electrode was then inserted into the cut carefully. However, due to the rigidity of the electrode, the insertion process was blocked. Besides, the insertion process also bent and damaged the device itself because of the mechanical force, as shown in Figure 4.36. The rigidity of the electrode comes from the thicker parylene structure which is necessary for the conductive epoxy squeegee process. In this failed sample, the thickness of the parylene-based electrode is more than 50 µm. However, this issue can be easily solved by etching some parylene on the electrode part. Therefore, the new parylene device with thinner electrode part was fabricated, as shown in Figure 4.37, which demonstrated much more flexibility. This time, the softer electrode, which is around 35 µm, can be easily folded to fit the size of the cut on eyeball. Besides, after insertion, the electrode can be easily pressed down to contact with the retina. Then, the suture was operated to fix the device and protect the cut. Retinal tack was also used to fix the electrode on the retina. The IC part which consists of retinal IC chip and discrete components, was fixed through suture holes near the cornea. Finally, the electrode on the retina was re-checked after fixing the IC part and it still stayed well, as shown in Figure 4.38.

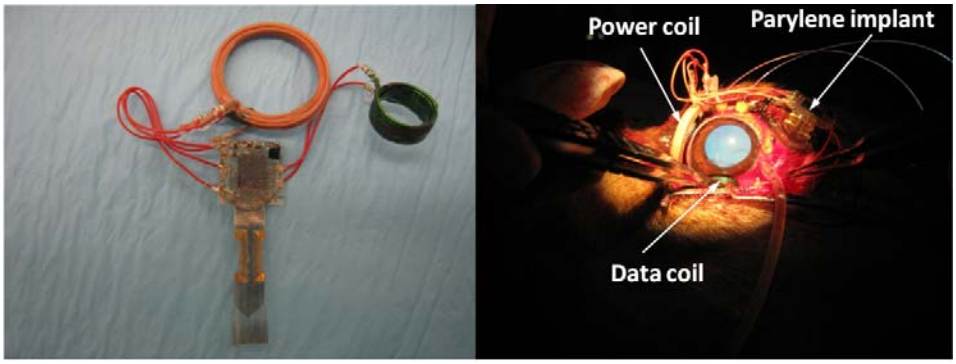


Figure 4.34. (Left) Parylene surgical mockup with metal connections integrated with IC chip, discrete components, and coils before implant. (Right) In vivo implantation trial in a dog's eye.

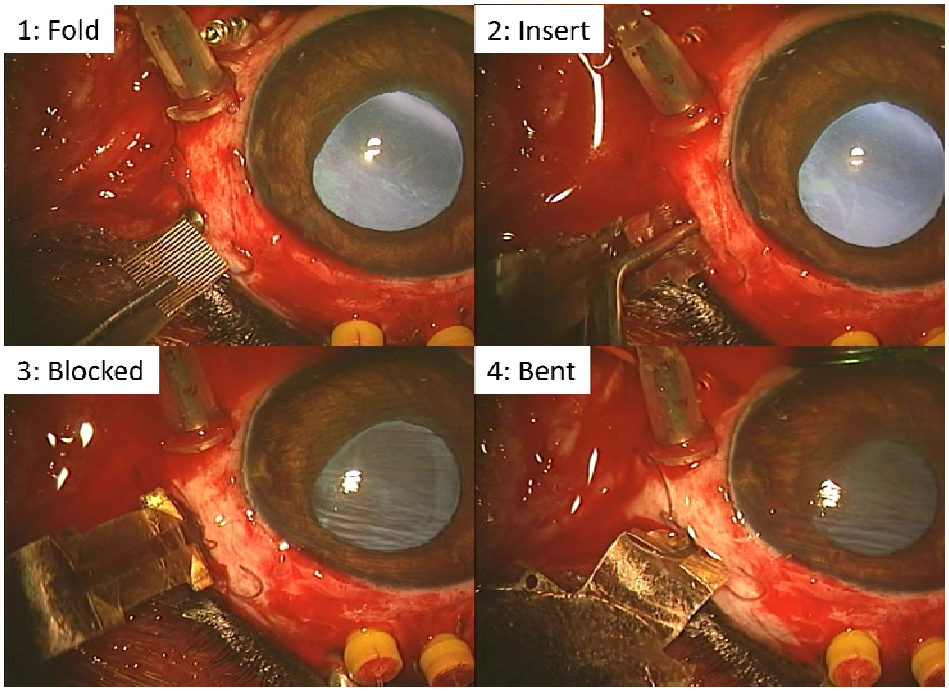


Figure 4.35. In vivo implantation trial in a dog's eye. (1) The electrode was first folded to fit the size of the cut on eyeball. (2) The electrode was then inserted into the cut. (3) Due to the rigidity of the electrode, the insertion process was blocked. (4) The insertion process also bent and damaged the device itself.

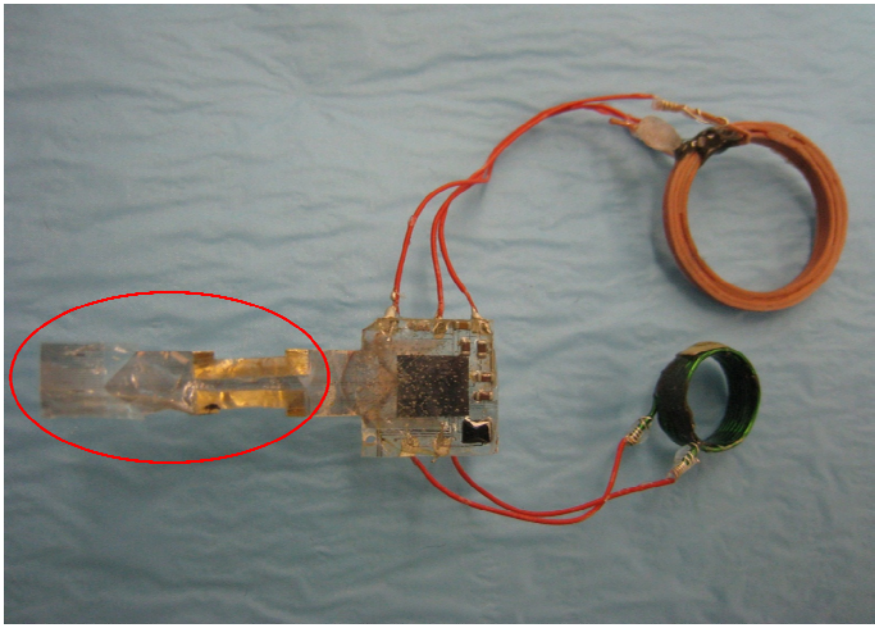


Figure 4.36. After implantation process trial, the mockup was bent and damaged.

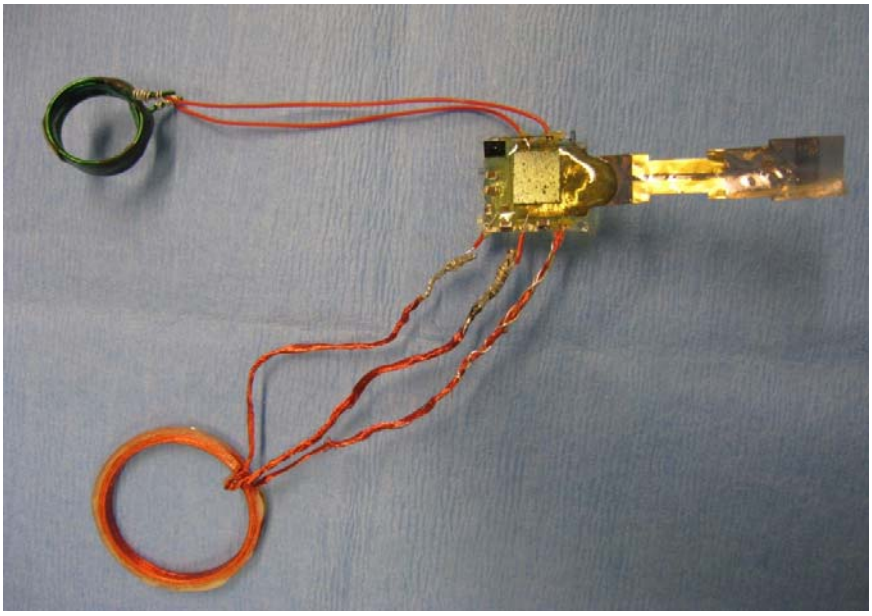


Figure 4.37. Softer (thinner) parylene surgical mockup with metal connections integrated with IC chip, discrete components, and coils before implant.

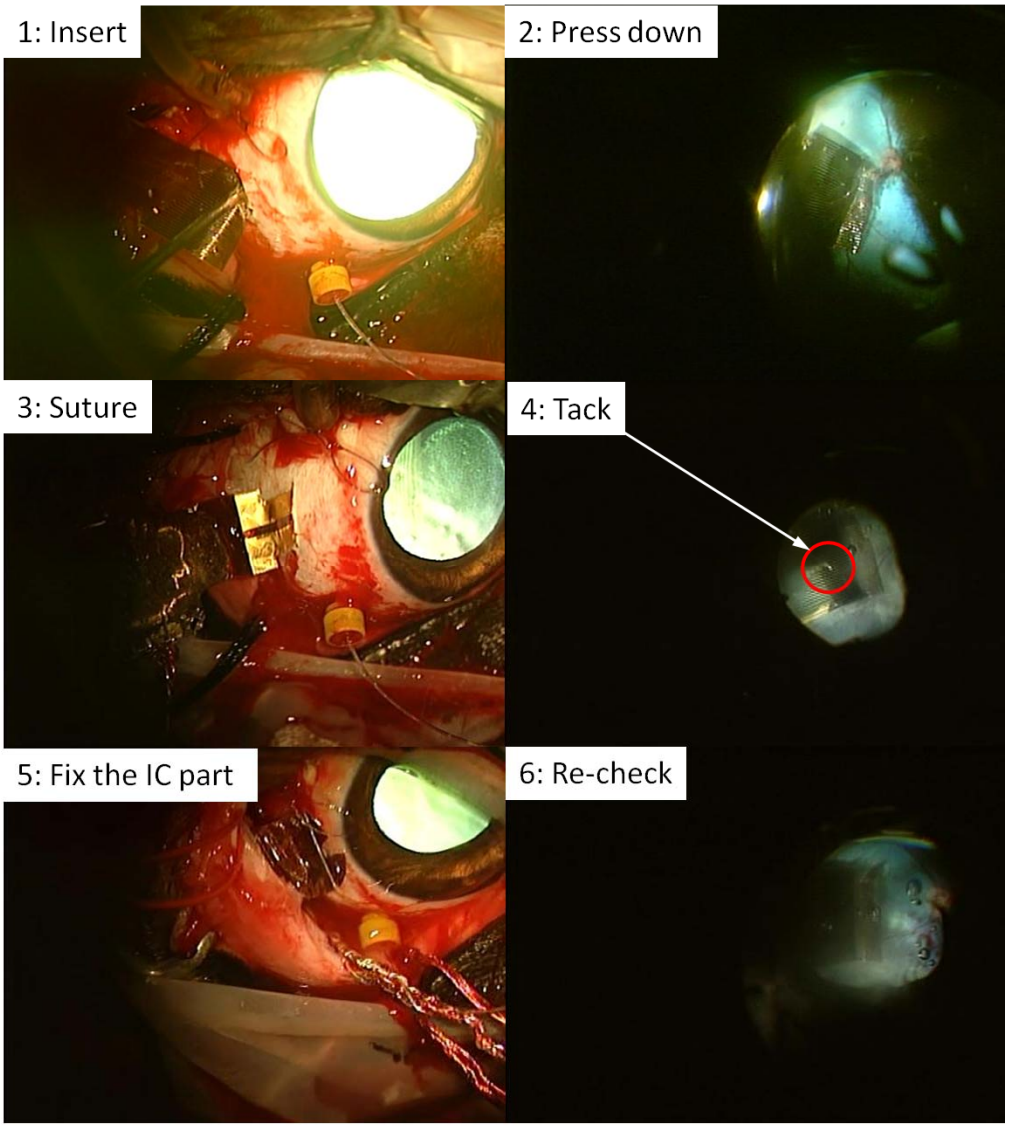


Figure 4.38. In vivo implantation trial in a dog's eye. (1) The softer electrode can be easily folded to fit the size of the cut on eyeball. (2) After insertion, the electrode can be pressed down to contact with the retina . (3) Suture was operated.(4)Retinal tack was used to fix the electrode on the retina. (5) The IC part was fixed through suture holes near the cornea. (6) Re-check the electrode on the retina after fixing the IC part.

4.3.3 MAXIMUM PULLING FORCE

In order to ensure that the parylene flex survives possible large surgical forces, maximum pulling forces on our parylene flex substrates were tested, as shown in Figure 4.39, using a dynamic

mechanical analysis (DMA) machine Q800 from TA instruments [23-24]. The size of the samples was designed to be 5 mm by 10 mm to fit the geometry factor of the machine. Creep test with a constant loading stress at body temperature of 37ºC was performed on the samples. Before the creep test started, we waited for 30 minutes of sample soaking in saline to ensure that the thermal equilibrium with the targeted temperature. Then, a constant stress was applied onto the samples for 10 minutes to measure the changes of the strain. The stress was then removed for 10 minutes to observe the recovery behavior. The maximum strain of the samples was measured to be 2.7% at an applied stress of 33.2 MPa. In brief, the samples can burden an applied force as high as 8 N during surgery, which was confirmed by our collaborating surgeons to be a very large safety margin for surgical handling. The additional parylene and silicone protection coating is believed to further increase the maximum allowable force.

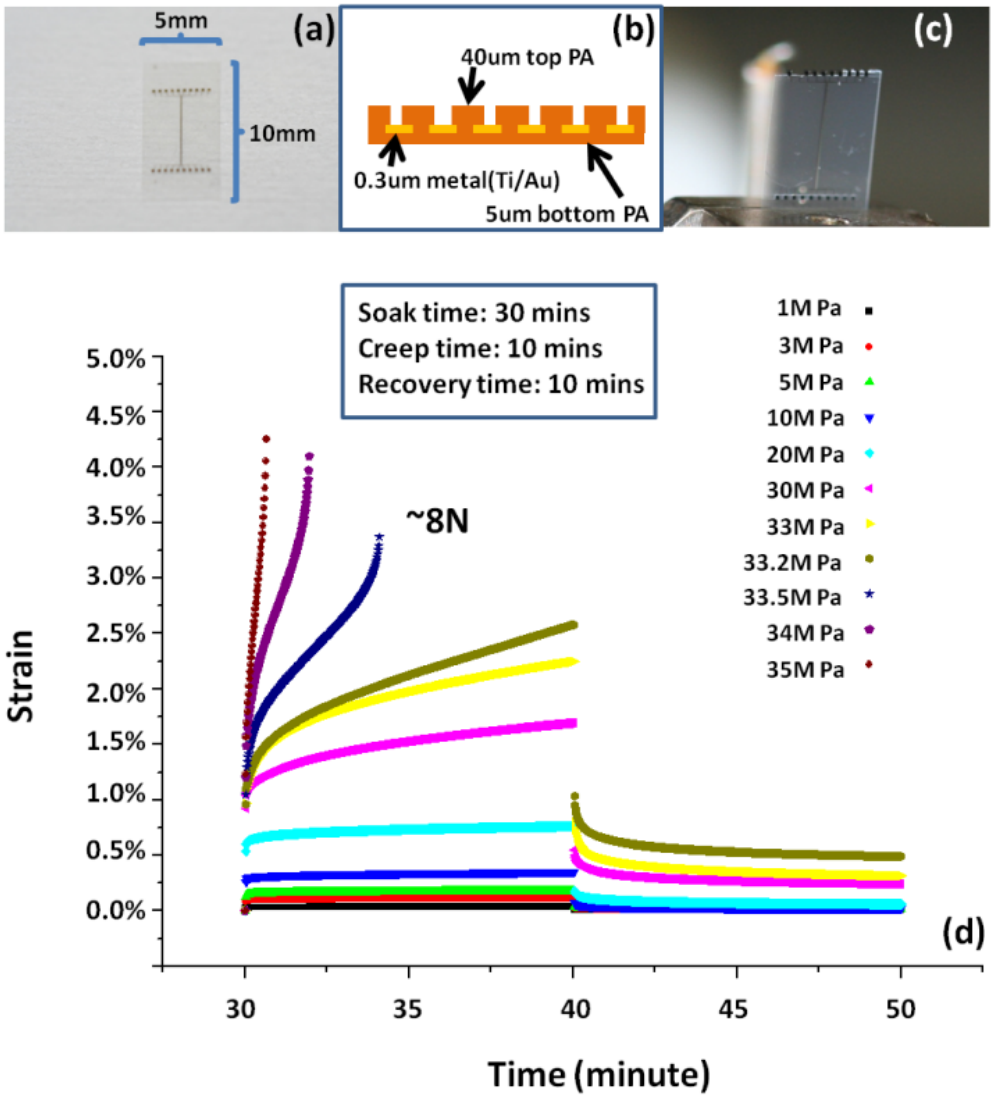


Figure 4.39. (a) Parylene flex test sample. (b) Cross-section of the tested sample. (c) Broken sample caused by over-stress. (d) Creep test at body temperature of 37°C.

4.4 Summary

In this chapter, a new packaging scheme using parylene-metal-parylene flexible composite protection coating was studied. Both active and passive components, including amplifier chip, discrete components, and dummy conduction chips, were tested. Parylene pocket structure was

specially designed to integrate the small amplifier chip. Samples were tested under active soaking condition to mimic the real implant conditions. Different failure modes were observed on samples with different protections. Chip with smaller size was found to have longer lifetime under the same protection and the mechanism should be further studied. The soaking data proved that this new packaging scheme has better protection and can be applied on implant devices.

In view of the current failure modes, a modified packaging scheme with a thin glass slide on the top of the device was proposed to further improve the protection. With biocompatible silicone as the adhesives and suitable interrface treatment, the lifetime of the device protected by this scheme can survive for more than 10 years at body temperature, which is a desirable target for implant device.

In addition, a proposed packaging for a 512-channel epiretinal implant was also presented here. The 3-coil wireless power transfer system with high transfer efficiency and data coils were included in this system. Simulation of the coil interference by Cadence was investigated and analyzed to show that adding two notch filters could solve the interference issues. Accordingly, a parylene flex implant model was designed and fabricated to include the chips, discrete components, and coils. In the model, the power and data coils were put in a coplanar fashion. Also, there was a parylene flex tail with all discrete components and later the tail was wrapped around the chips. This mockup has been successfully implanted inside a pig's eye.

The surgical mockup for the 1024-channel chip was also designed and fabricated. The main issue in this design is how to allocate all the 1024 interconnections in parylene with only 3 mm range. A special design was proposed to much relax the distribution of the 1024 interconnections, and the width of the interconnection is still 3 mm after folding. This mockup has been also successfully implanted inside a dog's eye. Besides, the maximum allowable pulling force of the parylene flex was also measured by a DMA machine to be 8 N, which provides a large safety margin for surgery.

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5 1024-CHANNEL RETINAL PROSTHESIS

5.1 Introduction

Figure 5.1. showed the simulation results of the facial recognition ability for blind people stimulating by different numbers of channels, and it is very clear that 1000-pixel is almost the minimum requirement for the blind people to distinguish one from the other. Around the world, much effort has been put to develop high-density multi-electrode arrays for retinal prosthetic applications [1-2] in recent years. However, even the most advanced prostheses do not have enough stimulating channels to restore vision to the desirable functional capability, like facial recognition or large-sized letter reading. The main issue is the lack of reliable high-density multi-channel chip integration technology. Currently, the most advanced retinal implant approved by Food and Drug Administration (FDA) is the Second Sight's 60-channel Argus II implant [3]. However, this technology has not yet reached the minimally desirable number of channels around 1,000. With the technology developed in chapters mentioned before, we have the full ability to build a wirelessly flexible parylene-based retinal implant device.

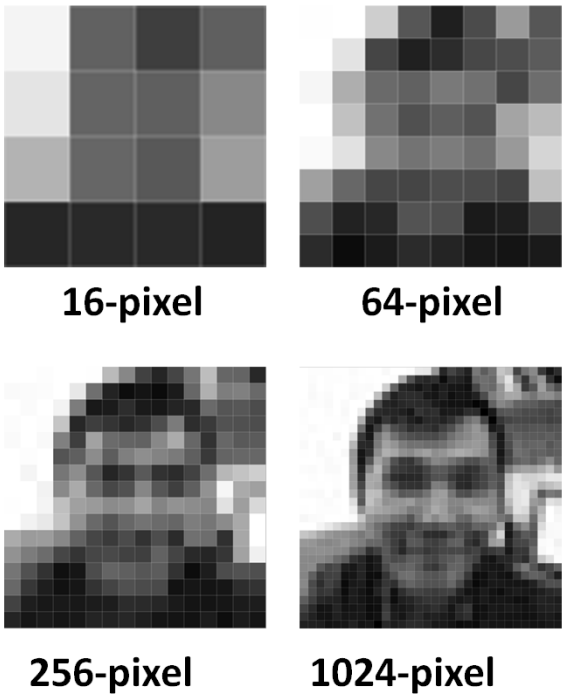

Figure 5.1. The simulation result of the facial recognition ability for blind people stimulating by different numbers of channels.

In this chapter, a final device with the single-metal-layer structure was first tried. Then, a fabrication process of final device with the dual-metal-layer structure was also proposed. Besides, multi-electrode array (MEA) has been addressed and studied. The surface on the MEA has to be treated in order to improve the charge transfer properties at the electrode/tissue interface. To be more specifically, the interface impedance of electrodes used to stimulate the retina needs to be modified to allow the current deliver from retinal IC chip to the ganglion cells. Materials such as platinum (Pt), iridium (Ir) oxide, stainless steel, titanium nitride, and tungsten have been tried on the electrodes for neural recording [4]. Besides, the thin-film Pt-Ir alloy by electro-deposition developed in USC also demonstrated many advantages over other methods in the surface modification of bio-electronic devices [5]. Currently, this method is believed to be the best surface modification on electrodes for the long-term implant. Here, we developed the Pt-black electro-deposition to quickly lower the

interface impedance of the electrodes for an acute implant. The technique of group electroplating was also introduced to modify more than 1000 electrodes at the same time. In addition, the shape of the electrodes was also treated to better fit the retina. In the end, the method on the integration of all the components was introduced to build a fully functional system.

5.2 Device Design

Based on the design in Figure 4.30, parylene flex with the single-metal-layer structure can be designed and fabricated with 5 μm pitch (2.3 μm metal line + 2.7 μm separation), as shown in Figure 5.2. The patterns of metals can survive stably by lift-off process within a small range. However, in order to accommodate all the requirements of surgery consideration and components allocation, the metal interconnections embedded in parylene flex will be easily longer than 3 cm. Besides, there will be many turns on the design due to the high lead count, in which damages will easily happen.

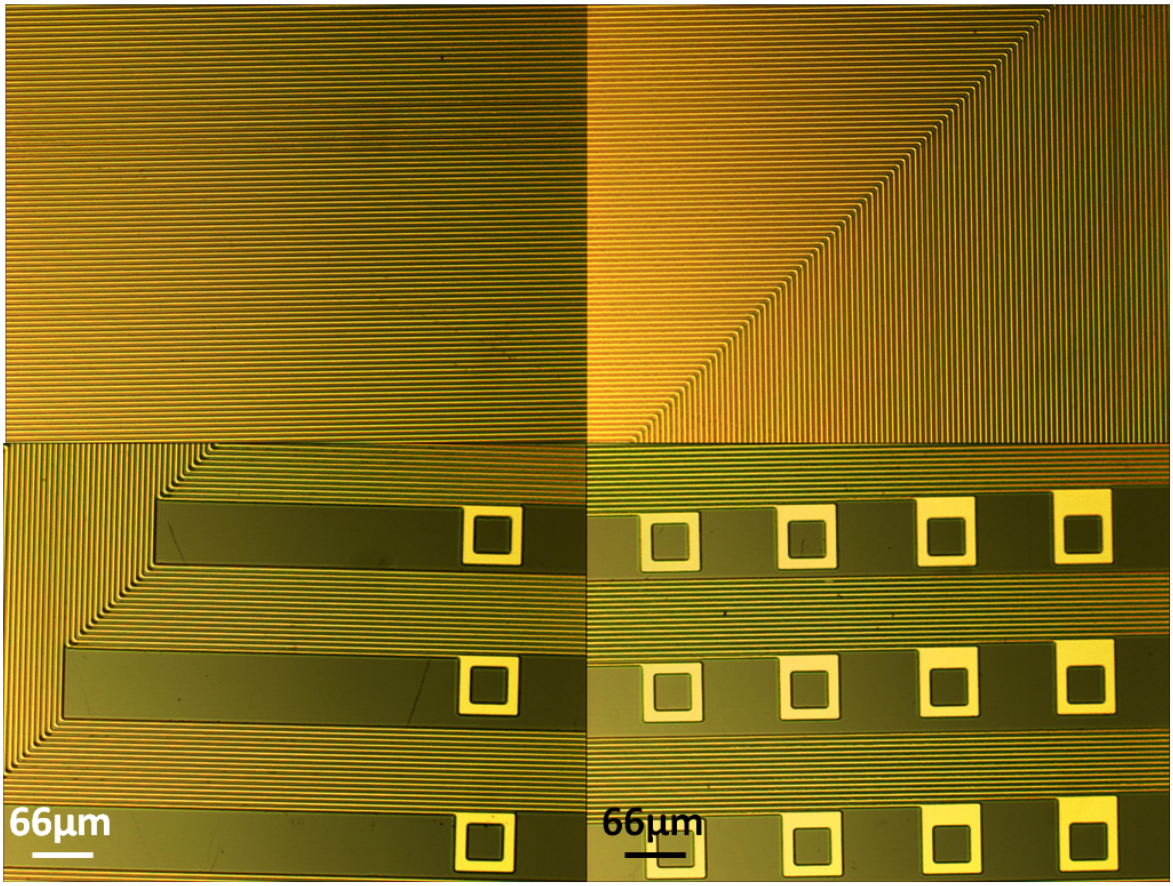

Figure 5.2. Microscopic pictures of metal patterns with 5 µm pitch.

In order to develop a more reliable fabrication process, a final device with the dual-metal-layer structure was proposed. The number of pitch was doubled to be 10 µm, which can be reliably built on parylene substrate. Figure 5.3 showed the mask design for the dual-metal-layer fabrication process. The first mask stood for the first half of output electrodes and all the input electrodes. The second mask was designed for the second half output electrodes. The third mask was used to open the electrodes and define the contour. Single retinal tack hole and two suture holes were also designed on this mask which will be beneficial for the surgical manipulation.

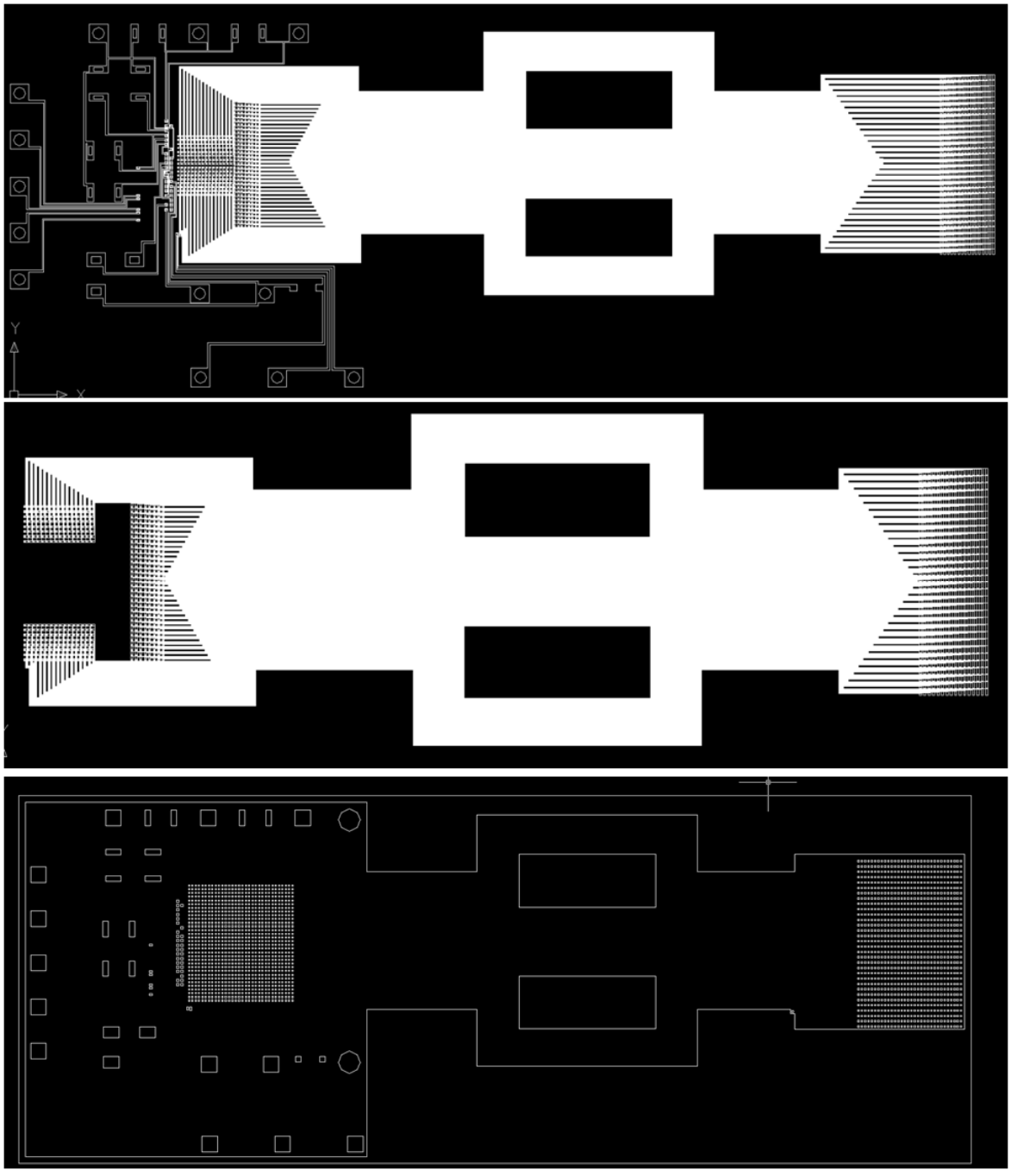

Figure 5.3. Mask design for the final device with dual-metal-layer: (Top) Mask for the first metal layer. (Middle) Mask for the second metal layer. (Bottom) Mask for the electrode opening.

Figure 5.4 showed the first metal layer on the first parylene substrate. The metal with 10 μm

pitch was well defined. Second layer parylene was then deposited to cover the first metal layer as the insulation. Oxygen plasma was treated before parylene deposition to physically enhance the adhesion. The photolithography was applied on the second parylene layer to get the undercut, as shown in Figure 5.5. The second metal layer was then successfully patterned on the second parylene layer. Metal patterns with 10 µm pitch can be repeatedly and reliably built at turns, as shown in Figure 5.6. This fabrication process was believed to be much more reliable than the single-metal-layer process.

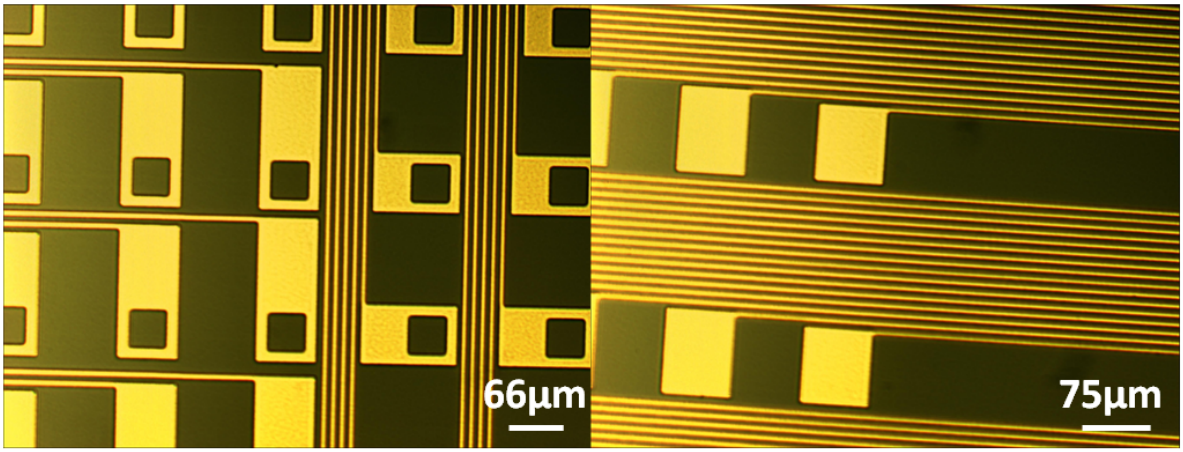

Figure 5.4. The first metal layer on the first paryelene substrate: (Left) Electrodes used to connect with IC chip. (Right) Electrodes used to stimulate retina.

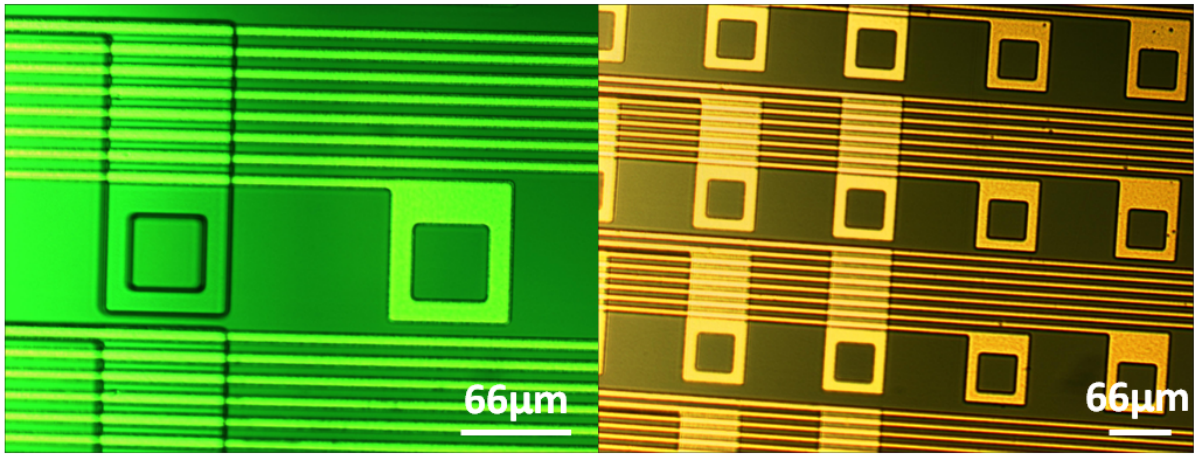

Figure 5.5. (Left) Photolithography was applied on the second parylene layer. (Right) Second metal layer was successfully patterned on the second parylene layer.

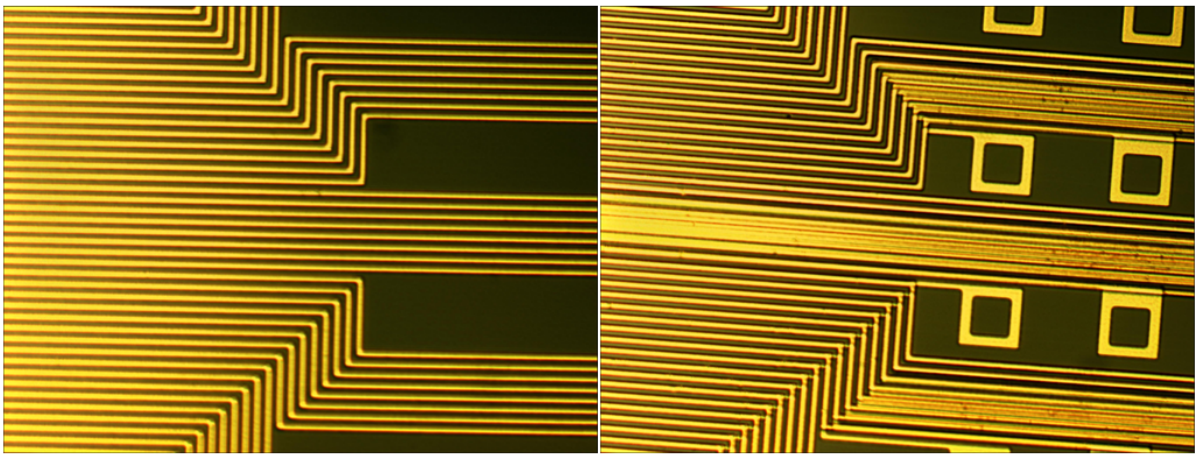

Figure 5.6. (Left) First metal layer with 10 µm pitch. (Right) Second metal layer with 10 µm pitch; some overlap can be seen.

5.3 Multi-Electrode Array (MEA)

5.3.1 Electroplating

Because of the limitation of cut on eyeball, the 1024 electrodes have to be arranged on an area which is around 7 mm × 7 mm. Therefore, each electrode has to be small to give an acceptable spatial resolution. However, smaller electrodes inherently suffer from high impedance which may result in tissue damaged by the high charge density stimulation [6]. Impedance reductions can be achieved by electroplating the micro-electrode array (MEA) with Pt-black to increase the effective surface area without extending the geometric area of an electrode. Besides, by reducing the interface impedance between the electrode and tissue, the voltage needed to drive the current will also decrease and the total power consumption of the devices could be lowered as well. Current plating methods include direct current (DC) and pulsed current. In order to lower the interface impedance as much as possible

(2 orders as a desired target), DC plating was selected for the dense Pt-black electro-deposition. The setup can be seen in Figure 5.7. Samples were first rinsed in ethanol and cleaned by 10 Hz biphasic current in 0.9% wt NaCl solution for 1 minutes. The plating solution was 1% wt. chloroplatinic acid, 0.0025% wt. hydrochloric acid, and 0.01% wt. lead acetate in water. Pt wire was used as the anode electrode. The DC current was 200 mA/cm^2 for 30 seconds. Ultrasonic agitation was used while plating to greatly enhance the adhesion.

Since the final device has more than 1000 stimulating output electrodes in contact with the tissue, it is impossible to electroplate the single electrode on by one for more than 1000 times. Besides, the small input electrodes which served as the contact point for the setup are not easy to connect. A group electroplating technique was thus proposed, as shown in Figure 5.8. Aluminum (Al) layer was first deposited on the whole sample. Then, it was patterned by AZ1518 to only keep the desired parts that cover and group all the input electrodes. The sample was then soaked in the electroplating bath and the output electrodes were plated by Pt-black. Finally, the Al layer was removed by Al etchant to complete the whole process.

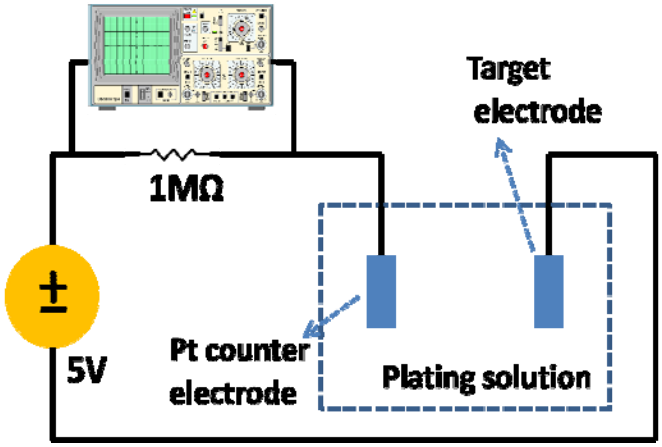

Figure 5.7. Electroplating setup.

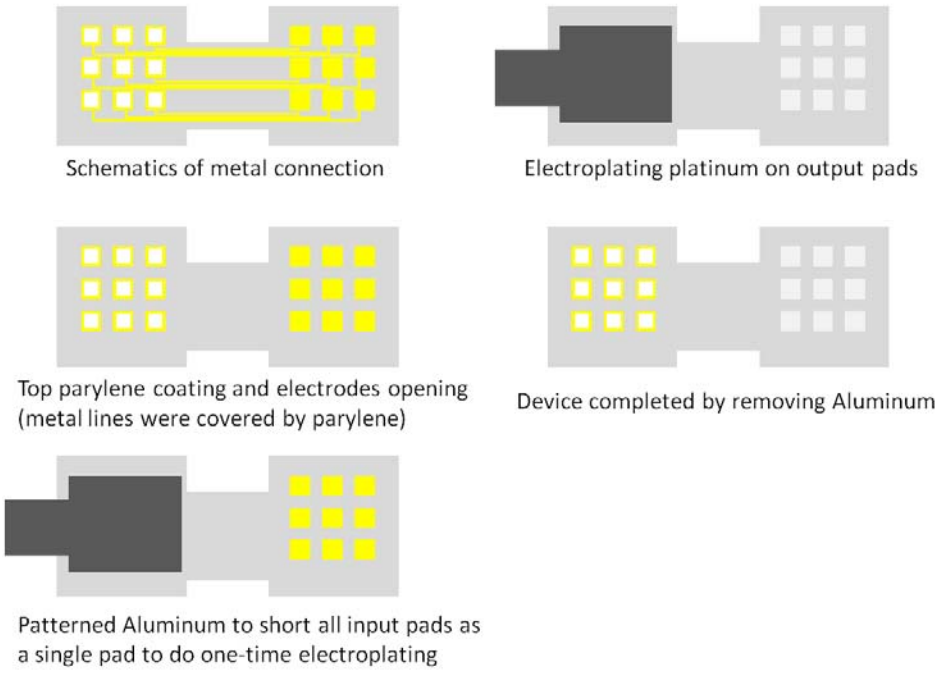

Figure 5.8. Process flow of the group electroplating technique.

The fabricated samples with 16 electrode array on wafer was shown in Figure 5.9. The size of each electrode is 66 μm × 66 μm. The interface impedance of the electrodes was tested before and after electroplating, and saline solution (0.9% wt NaCl) was used as the conductive media to simulate body fluid, as shown in Figure 5.10. Although the samples can be released from the wafer before electroplating process, it was found that samples on wafer are still more mechanically reliable during the electroplating process. A special holder was designed to allow the plating process of samples on wafer directly without wasting too much plating solution.

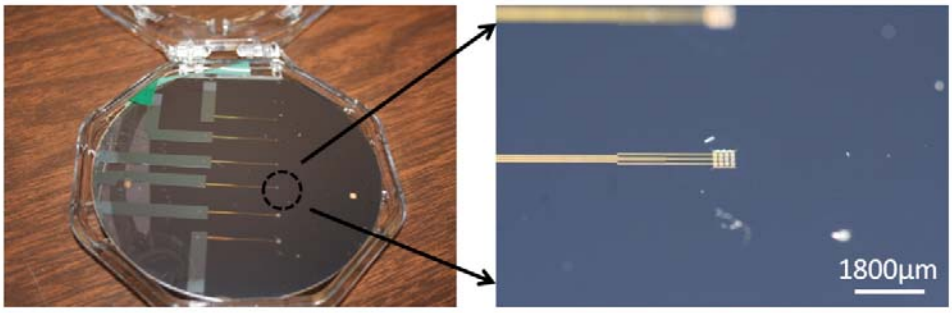

Figure 5.9. (Left)Fabricated sample with 16 electrode array. (Right) Closed-up view of the 16 electrode array.

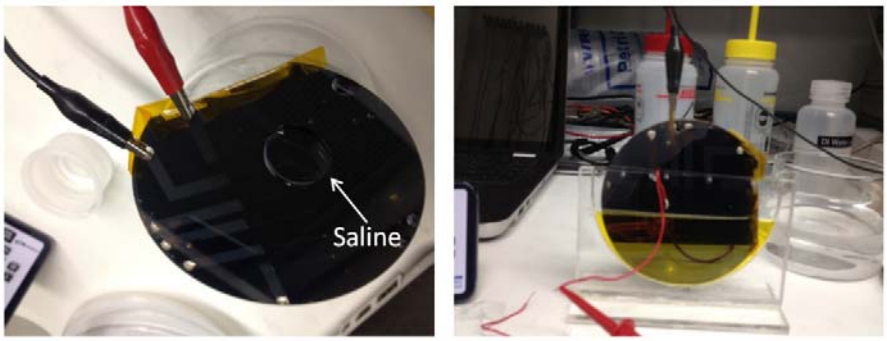

Figure 5.10. (Left) The impedance of sample was tested before and after electroplating; saline was used as a conductive media. (Right) Special holder was designed to allow the plating process of samples done on wafer directly.

Figure 5.11 showed the microscopic picture before and after electroplating. The electrodes after plating were covered by Pt-black very well. Figure 5.12 showed the SEM pictures before and after plating with different magnification. The surface after plating was much rougher than the surface before plating. The measures surface roughness data from profiler, as shown in Figure 5.13, also confirmed the fact that Pt-black was successfully electrodeposited on the gold surface.

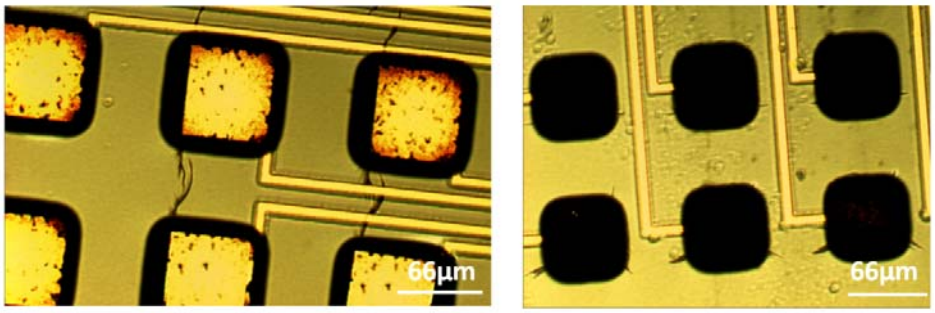

Figure 5.11. Microscopic pictures before (Left) and after (Right) plating.

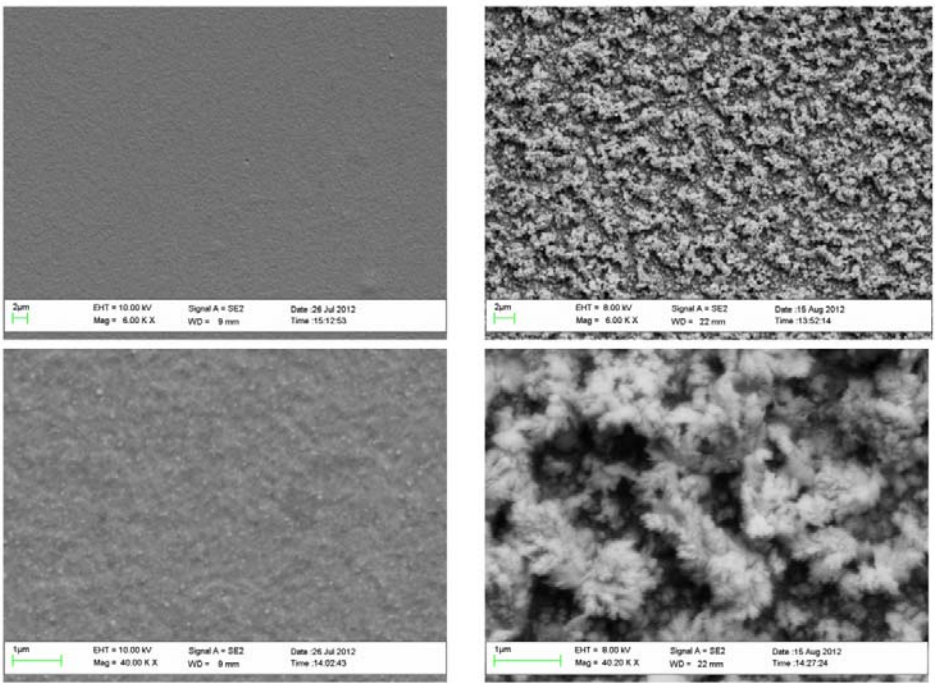

Figure 5.12. SEM pictures of the surface before and after plating with different magnification. (Top Left) Un-plated gold surface with 6K magnification; (Bottom left) Un-plated gold surface with 40K magnification; (Top right) Gold surface plated by Pt-black by DC current with 6K magnification; (Bottom right) Gold surface plated by Pt-black by DC current with 40K magnification.

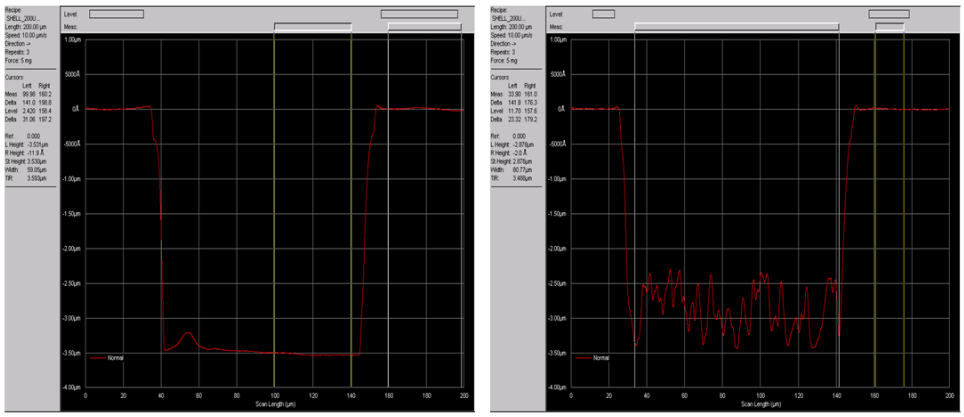

Figure 5.13. Measured surface roughness data before (Left) and after (Right) plating.

Figure 5.14 showed the measured data of impedance *v.s.* frequency and phase *v.s.* frequency. After biphasic cleaning and plating, the impedance of 16 electrode array dropped around 2 orders. The phase angle dropped about 20 degrees, which further confirms the increase of effective surface area (capacitance) and the polarization at the electrode/electrolyte indeed decreased.

This data can be further analyzed by the constant phase element, as shown in Figure 5.15. The overall impedance was contributed by the faradaic resistance (chemical reaction) in parallel with the constant phase element (double layer), and it can be represented on Nyquist plot with a phase of 90n°.

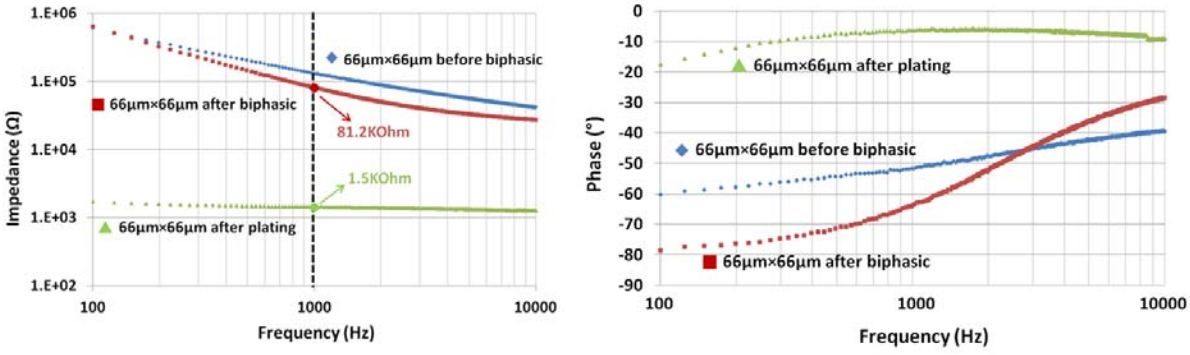

Figure 5.14. Measure data of (Left) Impedance v.s. frequency and (Right) phase v.s. frequency.

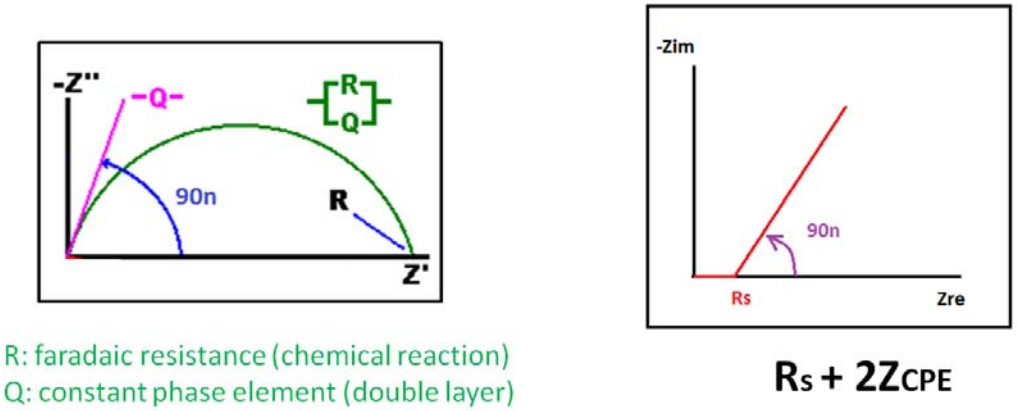

Figure 5.15. (Left) Impedance model. (Right) Impedance on Nyquist plot.

Figure 5.16 showed the measured impedance data on Nyquist plot before and after plating, and the result showed that the impedance of the 16 electrode array after plating is 1.4KΩ. The two regions can be explained with the finite length transmission line model. Under high frequency, the pores seem "infinitely long" to the solution, hence the resistance and capacitance are distributed as a constant phase element (CPE). Under low frequency, solution is able to travel to the end of the pore and the capacitance becomes constant C = ΔC*L (L is length of the pore), the equivalent model becomes a constant capacitor and resistor in parallel.

Randles circuit model, as shown in Figure 5.17, was applied to further analyze the impedance. John E. B. Randles is one of the most important theorists in the field of electrochemistry. In 1947, he devised this circuit model to describe the electrode-electrolyte junction [7]. He described the electrode-electrolyte interface as a capacitor, the Helmholtz double-layer capacitance, in parallel with an charge transfer impedance, all in series with a solution resistance. The charge transfer impedance is composed of a resistance and the Warburg impedance. Usually, the Warburg impedance is mostly negligible at the frequencies used in electrical stimulation. As a result, the junction circuit model can

be simplified as a resistor, R_{CT}, in parallel with a capacitor, C_{DL}, all in series with a solution resistance, R_S. At lower frequencies, the parallel circuit has a huge effect on the total impedance. However, at higher frequencies, the impedance is dominated by the solution resistance only because the capacitor acts as a short circuit. According to the circuit theory, we can get the interface impedance of single electrode is much lower than 11.2KΩ.

The maximum output current of the 1024-channel chip from UCLA is about 300uA with a 10V supply voltage on chip. A estimation of acceptable electrode impedance is around 30K~40KΩ. The tissue impedance is around 20KΩ, and the total impedance should be lower than 30KΩ which satisfy the requirement of the 1024-channel chip.

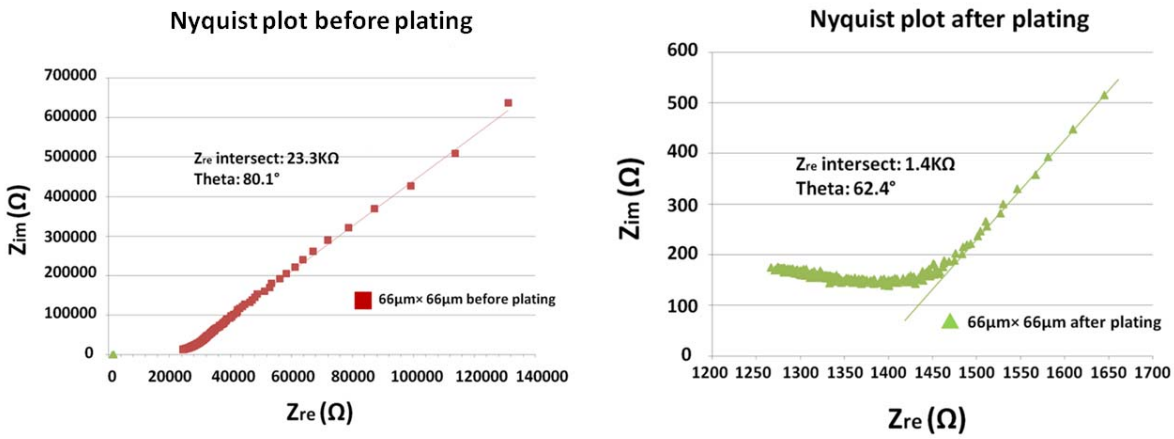

Figure 5.16. Nyquist plot of the impedance before (Left) and after (Right) plating.

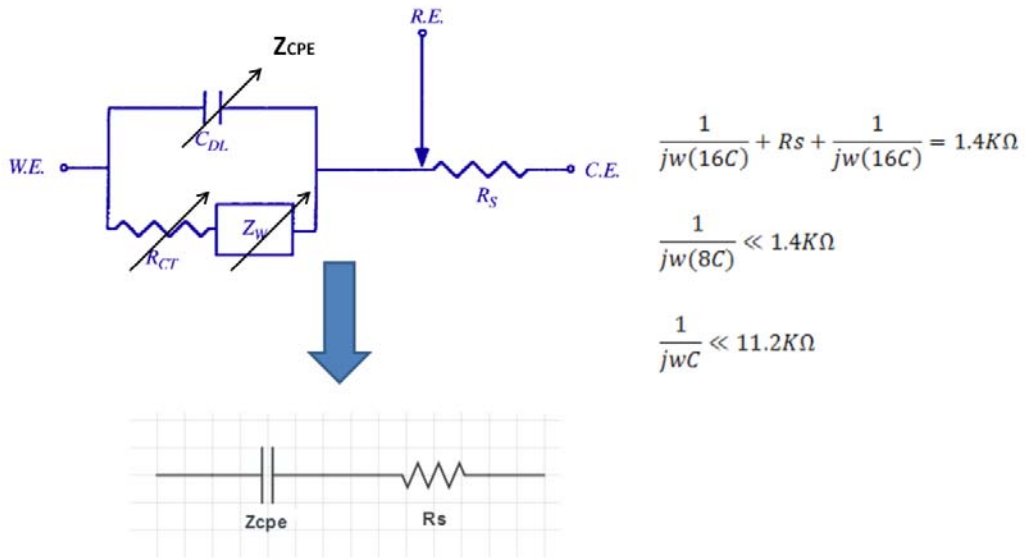

Figure 5.17. Randles circuit model for electrode/electrolyte interface. W.E.: working electrode; R.E.: reference electrode; C.E.: counter electrode.

5.3.2 Thermoforming

Besides the impedance, the shape of the electrode is also an important issue. With a correct shape, the stimulating electrode can be better attached to the tissue which is beneficial for the stimulation. Luckily, the parylene array can be easily shaped by thermoforming at temperature higher than its glass transition temperature. The glass transition temperature of as-deposit parylene was reported to be between 50~80°C [8]. However, our processed parylene had been heated up beyond 100°C, resulting in changes of glass transition temperature. Therefore, it is reasonable to anneal the sample between 150°C~200°C. Most importantly, this annealing process has to be done in vacuum oven that the parylene-based device will not get oxidized. The electrode array were shaped using a custom 6061 aluminum mold comprising a recessed concave region and a mating stainless steel sphere ball that approximates the curvature of the canine retina (diameter ~22 mm). During the annealing process, the electrode array region was sandwiched between the mating sphere ball and

molding surface, and the cable is pressed flat against the aluminum surface. We have discovered that this conformation will be maintained throughout follow-up integration, protection, and implantation process. It is important to note that, during the annealing process, parylene electrode array will easily get stuck to the oxide surfaces, such as glass slides. Therefore, it is important to use a material such as metal or aluminum foil to enable the electrode array release in the end after the annealing process. A photograph of the final mold used was shown in Figure 5.18, and electrodes of the real device shaped by the mold was shown in Figure 5.19.

Figure 5.18. (Left) Schematic of the mold used to shape the electrodes to fit the retina. (Right) Real picture of the final mold.

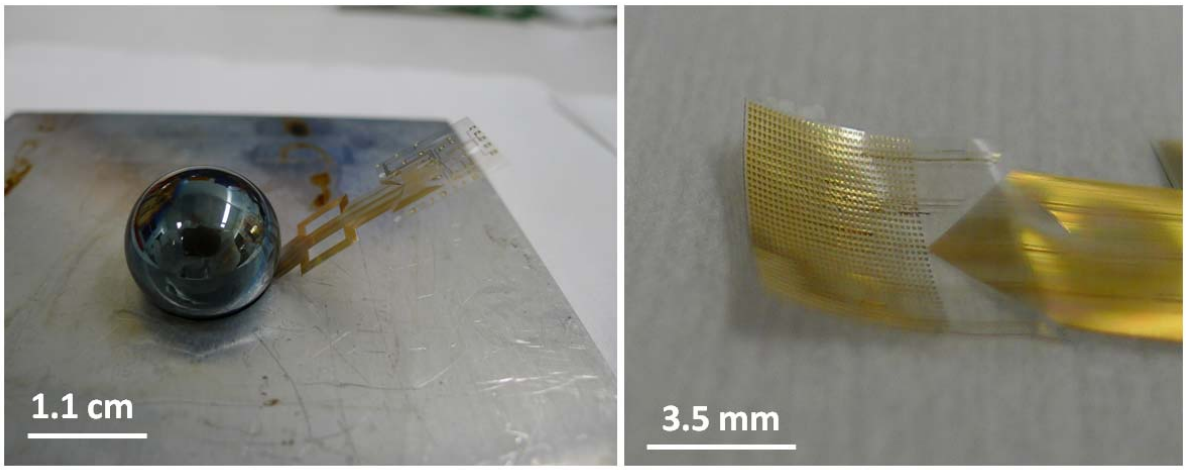

Figure 5.19. (Left) Electrodes were shaped by the mold. (Right) After shaping, the electrodes were well shaped.

5.4 Integration of IC chip, Discrete Components, and Coils

IC chip with smaller high-density and multi-channel bonding pads (pad size is smaller than 100 μm × 100 μm; pitch is smaller than 200 μm) was connected with the parylene flex by conductive epoxy squeegee technique, as shown in Figure 5.20. Other discrete components with bigger bonding pads, such as caps and oscillator, were connected with parylene flex manually by conductive epoxy using needles, as shown in Figure 5.21. Power and data coils with bigger bonding pads were also connected with parylene flex manually by conductive epoxy using needles. The front side of the integration was then protected by the protection scheme with combination of glass and silicone which was developed in Chapter 4; the back side was also covered by silicone. Additional thick parylene was further deposited for better protection, as shown in Figure 5.22. The whole integrated device was then implanted inside eyeball. In which, the electrode array was fixed by the retinal tack and the IC part was sutured on the eyeball.

Figure 5.23 illustrated the complete process flow to build a wirelessly flexible parylene-based retinal implant device. After parylene flex with dual-metal-layer was fabricated, the output electrode array was first curved by the aluminum mold. Pt-black was then electroplated on the gold surface of electrodes to lower the interface impedance. Conductive epoxy squeegee technique was then applied to integrate the high-density multi-channel retinal IC chip. Other discrete components and coils were connected by conductive epoxy using needles. The whole integration was then protected by the proposed packaging scheme. A thin glass slide was specially placed on the top of the chip to further protect the connections to the chip, hence much extend the lifetime of the device.

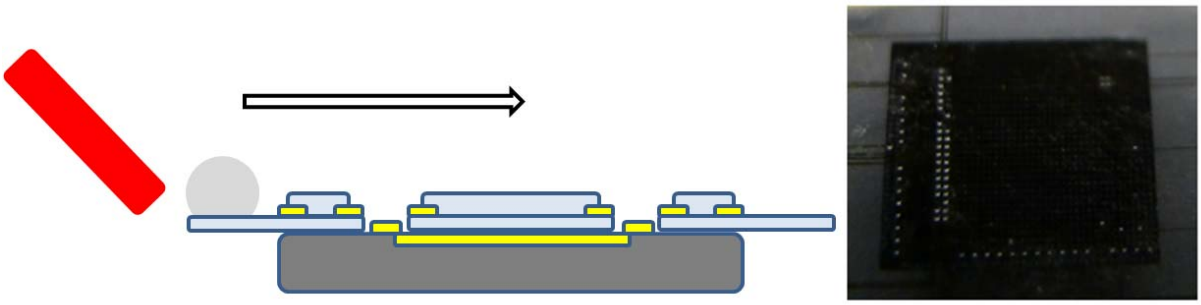

Figure 5.20. Conductive epoxy squeegee technique built for high-density multi-channel chip.

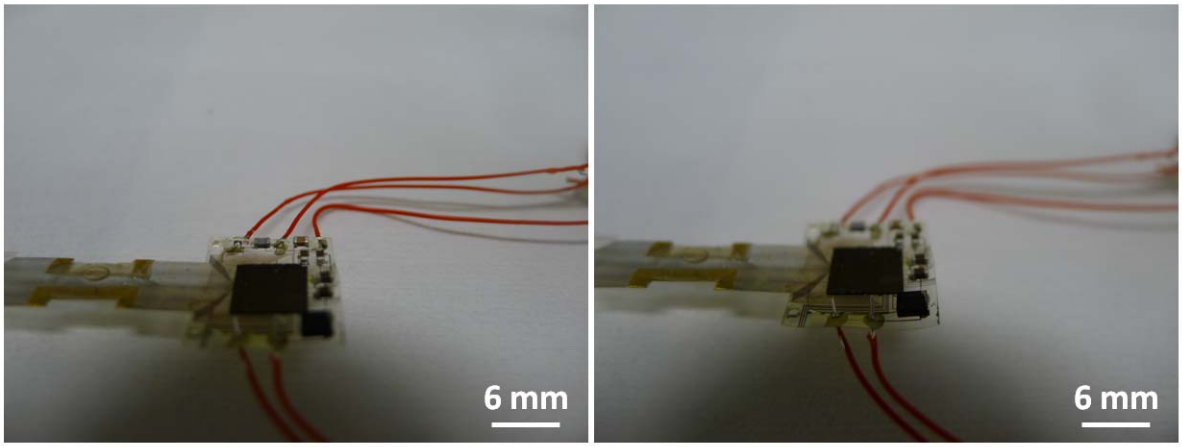

Figure 5.21. Discrete components and coils with bigger bonding pads were connected by conductive epoxy using needles.

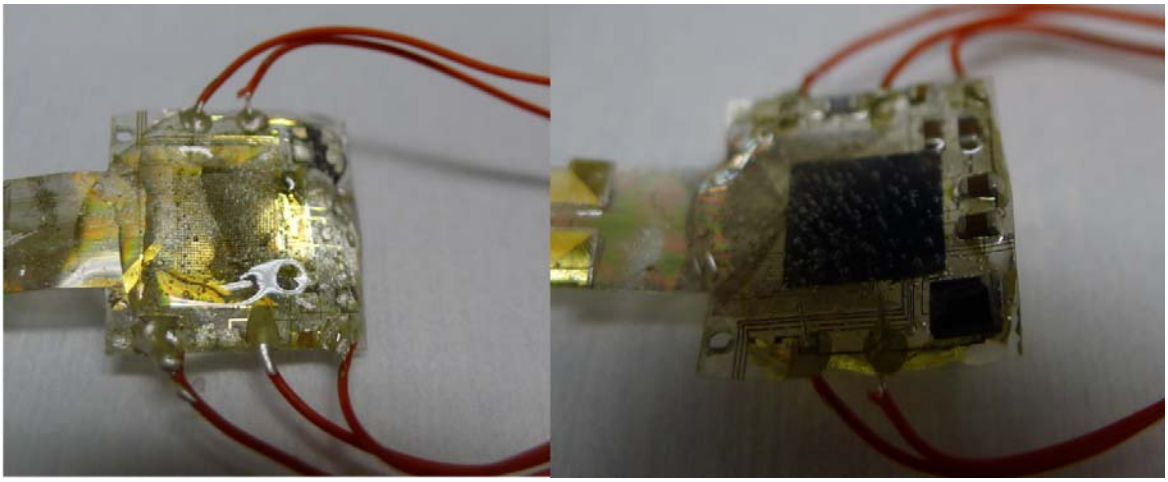

Figure 5.22. Front side and back side of the integration after protection coating.

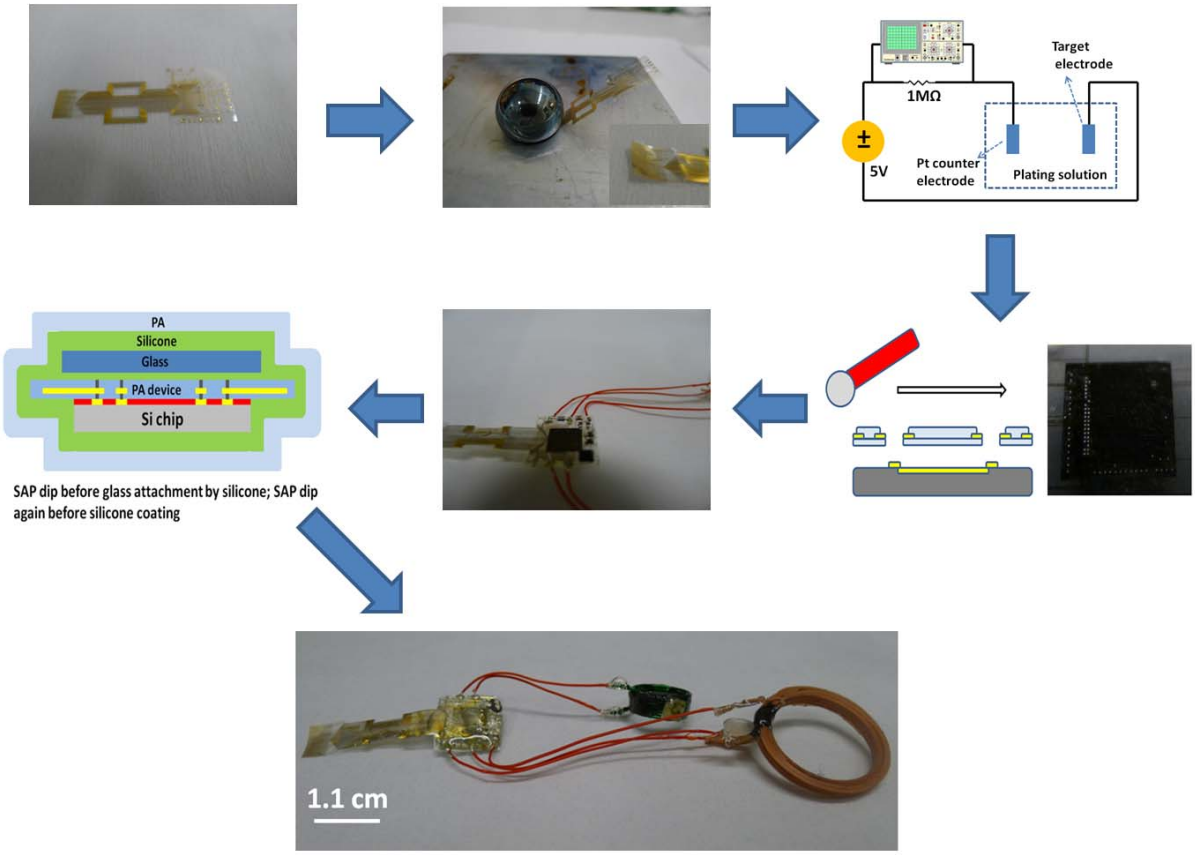

Figure 5.23. Complete flow illustrating how to build a wirelessly flexible parylene-based retinal

implant device.

5.5 Summary

The more reliable and repeatable dual-metal-layer fabrication process of parylene flex was developed. It is designed to integrate with the 1024-channel retinal IC chip. The pitch of the metal interconnections can be relaxed to be 10 μm which is a very safe number for metallization by lift-off process.

Electroplated Pt-black modified electrodes exhibited higher charge storage capacity and lower electrochemical interface impedance (around 2 orders) relative to original untreated gold electrodes on biomedical applications, which are beneficial for stimulation. They are capable of transferring large amounts of safe electrical charges to the biological tissues to decrease the damages of the tissue. This method can also be applied on various electrically conductive surfaces and are valuable alternative to other conventional techniques, such as thin film deposition and metal plating. Although the lifetime is shorter, it is still good enough for an acute implant. The total impedance of modified electrodes and tissue impedance can satisfy the specification of the 1024-channel retinal IC chip. Besides, the retinal electrode array was shaped to better fit on retina using a custom aluminum mold comprising a recessed concave region and a mating stainless steel sphere ball. It was annealed in vacuum oven with a temperature higher than the glass transition temperature of processed parylene device.

The integration of IC chip, discrete components, and coils with parylene flex were also demonstrated in this chapter. High-density multi-channel retinal IC chips can be connected by conductive epoxy squeegee technique; other discrete components and coils can be connected by conductive epoxy using needles. Protection scheme was also applied on the integration to extend the

lifetime. Last, the complete process flow of how to build a wirelessly flexible parylene-based retinal implant device was also illustrated.

5.6 Reference

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6 CONCLUSION

This dissertation is aimed to help regain eyesight for RP and AMD patients by visual prosthesis. Bio-compatible material, parylene-C, has been selected as the main substrate materials because of many favorable properties. MEMS micromachining technologies have been utilized to monolithically fabricate the micro-scale parylene device for retinal implant. In Chapter 1, MEMS technology, Parylene, traditional and state-of-the-art chip integration technologies have been introduced. In Chapter 2, the basic requirement of packaging for parylene-based retina implant device was first addressed and discussed. Two different generations of parylene-C flex fabrication have been studied. In which, techniques for metal fabrication with around 10 μm pitch were specially investigated and a quick dry mechanical liftoff technology used to pattern metals on parylene was developed. Chemical surface treatments to enhance adhesion for parylene layers were investigated and P.C. was found to be the best chemical to create clean hydrophobic surface which is desirable for parylene adhesion. Peeling tests and soaking tests were both performed to confirm the effectiveness. Based on the technologies here, we were able to build a reliable and stable parylene-based device for retinal implant. The device packaging and integration were also studied here. Conductive epoxy squeegee technique can make high-density multi-channel IC chip connection, and laser cutting can solve the short circuit issue. However, several issues including misalignment and weak adhesion between IC chip and parylene flex still existed at this stage.

In Chapter 3, photo-patternable adhesives were investigated and applied on the high-density multi-channel retinal IC chip integration in order to create a more stable interface. Experimental procedure and setup were studied and peeling force was measured to compare the various adhesives with different thickness. SU-8 with 28 μm was proved to be the best candidate for our application to

stand the maximum peeling force, and it is currently used in our integration technology. Dummy chips were designed to examine the connection yield and find out the limits of this technology. According to the experimental results, this new packaging technology is promising to be applied to 10,000 connections within an area as small as 36mm^2. Real 268-channel and 1024-channel retinal IC chips from UCLA were integrated with parylene flex by this technology and functionalities have been successfully tested to confirm the effectiveness.

In Chapter 4, a new reliable packaging, parylene-metal-parylene flexible composite protection coating, was studied. Both active and passive components, including amplifier chip, discrete components, and dummy conduction chips, were tested. Parylene pocket structure was specially designed to integrate the small amplifier chip. Samples were tested under active soaking condition to mimic the real implant conditions. Different failure modes to fail the connections were observed on samples with different protections. Chip with smaller size was found to have longer lifetime under the same protection. The soaking data proved that this new packaging scheme has better protection and can be applied on implant devices. Based on the current failure mode, another new protection scheme with one more thin glass to better cover the electrodes and conductive epoxy was purposed. The only failure mode observed in this scheme was the very slow diffusion along the interface between the thin glass and the parylene flex, and the lifetime of the protected chip is more than 10 years, which is a very desirable number for implant. Besides, a proposed packaging for a 512-channel epiretinal implant was presented. The 3-coil wireless power transfer system with high transfer efficiency and data coils were included in this system. Simulation of the coil interference by Cadence was investigated and analyzed to show that adding two notch filters could solve the interference issues. Accordingly, a parylene flex implant model was designed and fabricated to include the chips, discrete components, and coils. In the model, the power and data coils were put in a coplanar fashion. Also, there was a parylene flex tail with all discrete components and later the tail

was wrapped around the chips. This mockup has been successfully implanted inside a pig's eye. In addition, the packaging scheme for a 1024-channel retinal IC chip was also presented. In consideration of the high lead count, two wings were specially designed to relax the density of the metal lines. After folding, the interconnection area was still 3 mm to fit the limitation of the cut on eyeball. Because of the nature of the high power requirement for this chip, the power coil designed for this chip was much bigger than the one for the 512-channel chip, which makes the implant more difficult and bloody. However, the device itself has been successfully implanted inside a dog's eye and the geometry of the current design allowed the device sitting on the retina nicely and the electrode array positioned on the retina at around 5mm~8mm away from optic nerves. The maximum allowable pulling force of the parylene flex was also measured by a DMA machine to be 8N, which provides a large safety margin for surgery.

In Chapter 5, the parylene device with dual-metal-layer for retinal implant was designed and fabricated. The Pt-black electroplating technique was applied on the MEA to lower the interface impedance to allow the stimulating current delivered to the tissues for an acute implant. Thermoforming technique was also performed to shape the MEA to better fit the retina. Curing temperature higher than the glass transition temperature is necessary. Finally, photo-patternable adhesives and squeegee techniques were applied to make connection to the retinal IC chip and other discrete components were connected by the conductive epoxy with needle. The whole integration was then protected by the packaging scheme developed in Chapter 4.

The two major technologies developed in this dissertation include the high-density multi-channel conductive epoxy squeegee technique with photo-patternable adhesives and the long-term protection scheme which extends the lifetime to more than 10 years. With these techniques, we are supposed to be able to build a integrated device for long-term implant. However, in order to achieve a reliable totally intraocular retinal implant working system, more effort has to be spent on building more

stable and compact coils for long-term implantation. Besides, more reliable retinal IC chips with lower power must be developed at the same time.