Chapter 5

Synthesis of Polymer Dielectric Layers for Organic Thin-Film Transistors via Surface-Initiated Ring-Opening Metathesis Polymerization

5.1 Abstract

Polymer-based dielectric layers for use in electronic devices such as thin-film transistors (TFTs), capacitors, and other logic elements have attracted much attention for their low cost, processability, and tunable properties. Current methods for incorporating organic materials into these devices are either not ideal or not possible when applied to the deposition of polymer dielectric materials. The living ring-opening metathesis polymerization (ROMP) of strained, cyclic olefins can provide a method for growing organic polymers from a surface. ROMP would allow for pinhole-free dielectrics with controlled layer thickness and tunable electronic and surface properties by growing a covalently attached polymer from the surface. Furthermore, ROMP from surfaces is unique in its ability to polymerize monomers from either solution or vapor phase and can be performed under mild ambient conditions, afford polymer growth in minutes, and allow for flexibility in polymer structure and dielectric layer composition. We have shown the feasibility of producing TFTs and capacitors using surface attached ROMP polymers as a layer of dielectric material. Preliminary results indicate that this method will allow for highly tunable materials with desired properties. The ability to grow conformal polymer layers on any topology will be very important as device dimensions and applications change.

5.2 Introduction

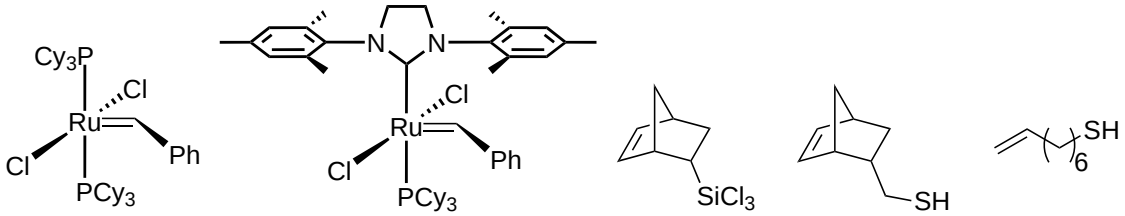
The use of organic materials in electronic devices such as field effect transistors (FETs) and light emitting diodes (LEDs) has become an attractive approach toward decreasing weight and cost, simplifying production, and increasing versatility of these devices. Electronic devices containing polymer layers have been incorporated into applications such as active-matrix displays[1–3] and integrated circuits.[4, 5]

For optimal FET performance, a polymer dielectric layer should be chemically and electrically compatible, with the organic semiconductor facilitating a smooth interface between adjacent layers.[6] Low leakage and tunable dielectric properties are

also desirable. This requires that the layer be pinhole-free, with controlled thickness and composition.

Current methods for depositing polymer layers include spin-coating, ink-jet printing, and screen printing.[7–9] Unlike these methods, surface-initiated polymerizations can produce densely packed, conformal layers over any surface topology. Compared with other surface-initiated polymerization methods, ring-opening metathesis polymerization (ROMP) allows mild conditions and short reaction times. Therefore, we have chosen to investigate surface-initiated ROMP (SI-ROMP) as a method for forming polymer dielectric layers.

SI-ROMP has been demonstrated from Au, Si, and Si/SiO_2 surfaces using catalyst **1** and a variety of linking molecules.[10–12] Conformal block copolymers grown on Au nanoparticles demonstrated the living nature of SI-ROMP with catalyst **1**.[13] We report here that SI-ROMP polymer layers can be used as the dielectric layer in electronic devices, either alone or in tandem with an inorganic dielectric layer. We also report that, as with solution-phase ROMP,[14] catalyst **2** is more active than catalyst **1** in SI-ROMP (Figure 5.1).



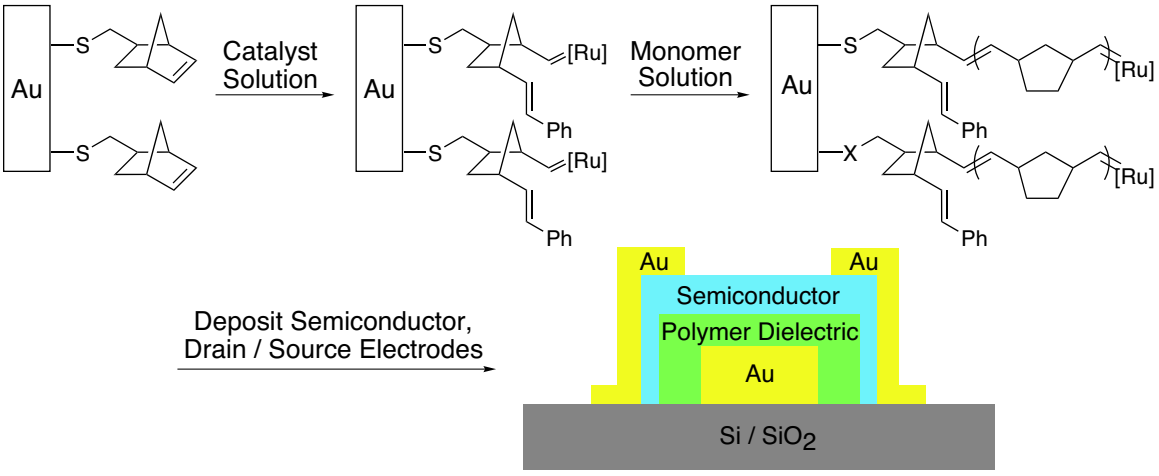
1 **2** **3** **4** **5**

Figure 5.1: Catalysts and linking molecules employed in SI-ROMP.

Polymer dielectric layers covalently attached to Au or Si/SiO_2 surfaces were formed via ROMP from surface-tethered metathesis catalysts (Scheme 5.1). Exposure of a self-assembled monolayer (SAM) of a linking molecule (**3**, **4** or **5**)[15] (Figure 5.1) to a solution of catalyst (**1** or **2**), followed by subsequent exposure to a solution of monomer, generated the polymer film. Between each of these steps, the surfaces were extensively rinsed with solvent to remove chemically unbound material.

Many variables were found to significantly affect the thickness and uniformity

Scheme 5.1: Construction of an FET using a SI-ROMP polymer dielectric layer (**4** shown as example linker).



of SI-ROMP polymer films. Most importantly, catalyst **2** is far more active than catalyst **1**. Given identical reaction conditions, films produced from catalyst **2** are up to 10 times thicker than those produced from catalyst **1**. For example, using **4** as the linker, films produced after 15 min of exposure to a 3 M solution of norbornene at room temperature (rt) are nearly 2.5 μm in thickness using catalyst **2**, versus 250 nm with catalyst **1**. Furthermore, catalyst **2** produces polymer films greater than 300 nm thick from 1 M monomer solutions, whereas catalyst **1** requires concentrations in excess of 3 M to produce equivalent films.

Polymerization conditions were also found to affect SI-ROMP films. Decreased thicknesses result for polymerizations conducted above rt, or for prolonged periods of time ($>$ 1 h). Almost no film remains after 24 h of polymerization time, suggesting that, as in solution-phase ROMP, secondary metathesis (chain transfer) reactions are occurring between growing chains. Slower than ROMP, and promoted by elevated temperature,[16] secondary metathesis in SI-ROMP would lead to chain termination and generation of polymer fragments that are no longer covalently attached to the substrate.

Smooth, pinhole-free dielectric films are important, since the overlaying semiconductor layer of an FET must continuously bridge the source and drain contacts.[17]

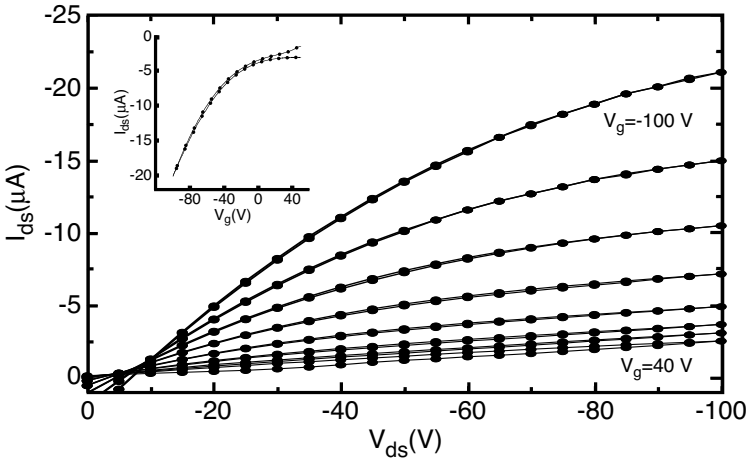


Figure 5.2: Current-voltage characteristics of an FET produced by lamination, containing a SI-ROMP polynorbornene dielectric layer. The drain bias was swept from 0 to -100 V and back at gate biases between 40 and -100 V in 20 V steps. Inset shows drain current as gate voltage was swept from 40 to -100 V and back.

Electrical shorting between the gate and drain and/or source electrodes was observed due to pinholes present in untreated SI-ROMP polynorbornene films. Annealing at 135 °C for 15 min densifies the films and significantly reduces the number of pinholes, resulting in relatively smooth, unshorted films.

Construction of FETs (as shown in Scheme 5.1) was demonstrated using the lamination method.[18] A SI-ROMP polymer dielectric layer was grown on a Au strip gate electrode (1000 Å thick, 1 mm wide) using linker **4**, catalyst **2**, and a 3 M norbornene solution. The thickness of the resulting polynorbornene film was 1.2 μm with a capacitance of 3 nF cm^{-2} measured at 20 Hz. After annealing, a 400 Å layer of pentacene was vapor deposited over the polymer dielectric. This was pressed against a separate PDMS substrate containing parallel Au strips as drain and source electrodes spaced 240 μm apart. A representative current-voltage (I/V) diagram for the resulting FETs is shown in Figure 5.2. Ranges for mobility and on/off ratio were 0.1–0.3 cm^2 V^{-1} s^{-1} and 10–100, respectively.[6] Little to no hysteresis was observed for these devices (see inset of Figure 5.2), indicating minimal charge buildup between the dielectric and semiconducting layers.

In addition to the lamination method, direct deposition of Au drain/source elec-

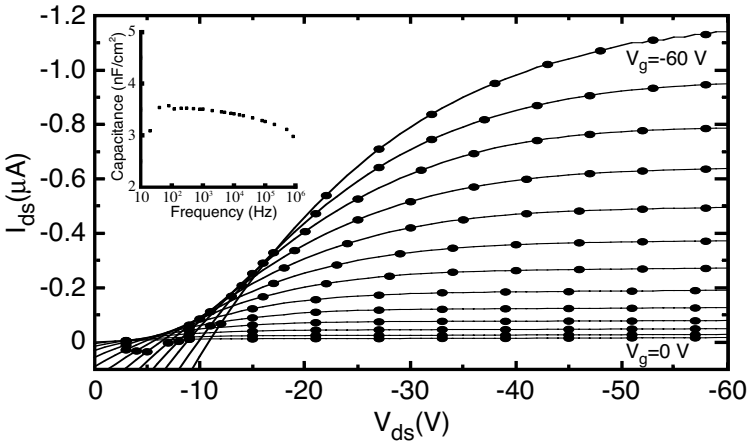


Figure 5.3: Current-voltage characteristics of an FET produced by direct deposition of the semiconductor layer and Au drain/source electrodes over a SI-ROMP polynorbornene dielectric layer grown from a Au gate electrode. The drain bias was swept from 0 to -60 V at gate biases between 0 and -60 V in 5 V steps. Inset shows capacitance of a polynorbornene capacitor as a function of frequency. The leakage current is due to the unpatterned gate and organic semiconducting layers.

trodes over the pentacene semiconducting layer also produced functioning FETs. Example I/V characteristics for these devices are shown in Figure 5.3. As seen in previous studies, mobilities and on/off ratios (up to 10^{-2} cm^2 V^{-1} s^{-1} and 100, respectively) were lower than those for the laminated devices due to partial degradation of the pentacene layer by the metal deposition.[18] The capacitance of the SI-ROMP dielectric films for these devices was found to have no significant frequency dependence down to 20 Hz (see inset of Figure 5.3).

Finally, FETs were constructed using a SI-ROMP polymer dielectric layer covalently bound to a Si/SiO_2 (either native or thermally grown oxide) surface. Working devices were constructed using either catalyst (**1** or **2**), linker **3**, and 2 M norbornene solutions.

Apart from washing extensively with solvent, no effort was made to remove residual (covalently bound or imbedded) catalyst from the polymer films. Rutherford backscattering spectroscopy (RBS) and medium energy ion scattering (MEIS) measurements, however, indicated exceptionally low surface concentrations of Ru for catalyst-functionalized SAMs as well as the washed films. Increasing the concen-

tration of ruthenium bonded to the SAM may result in denser films and less leakage.

These devices demonstrate that surface-initiated polymer dielectric layers are both chemically and electrically compatible with other FET component layers. In general, a high yield ($> 90\%$) of working TFTs was obtained only with annealed dielectric films at least 1 μm thick. Further optimization of polymer growth conditions, yielding higher graft densities and reduced surface roughness, should allow the use of thinner films as well as improve the compatibility between the polymer film and organic semiconductor.[19]

For devices using patterned (e.g., striped Au) substrates, the SI-ROMP polymer grows conformally over the gate electrode, eliminating the need to pattern the dielectric. Furthermore, spin-coated dielectric layers tend to be thinner at the edges of the electrode, leading to a lower breakdown voltage. In contrast, the thickness of the surface-grown polymer layer can be about the same at the edges as for the flat surface, illustrating a clear advantage of SI-ROMP.

In conclusion, construction of FETs using SI-ROMP polymer dielectric layers has been demonstrated. Mild reaction conditions, short reaction times, and simple solution processing methods make SI-ROMP an attractive method for constructing polymer dielectric layers. Layer thicknesses ranging from below 100 nm to above 2 μm are accessible simply by varying the polymerization conditions. Research is underway in optimizing FET device characteristics, as well as incorporating SI-ROMP block copolymers into organic-based FETs.

5.3 Experimental Section

Materials. Acetone, isopropyl alcohol, ethanol, 8-bromo-1-octene, tetrahydrofuran (anhydrous), hexamethyldisilathiane, tetrabutylammoniumfluoride (1.0 M in THF with 5% H_2O), and bicyclo[2.2.1]hept-2-ene (norbornene) were used as received from Aldrich. Dichloromethane (Aldrich, anhydrous) was degassed prior to use by sparging with argon. 1,2-dichloroethane (Aldrich, anhydrous) was first filtered through a plug of neutral alumina (Brockman Grade I; this procedure is necessary in

order to have film growth), and then degassed by sparging with argon. 5-(Bicycloheptenyl)trichlorosilane (**3**) was purchased from Gelest, Inc., and used as received. Bicyclo[2.2.1]hept-5-ene-2-methanethiol (**4**) was prepared as described in the literature.[20] Catalysts **1**[21] and **2**[22]were prepared as described in the literature. 7-Octene-1-thiol (**5**) was prepared according to a literature procedure,[23] with 8-bromo-1-octene as starting material.

Substrate Preparation and Metal/Organic Semiconductor Deposition. Silicon wafers containing a 3000 Å thermally grown oxide layer were obtained from Silicon Quest International. Gold substrates (typically composed of a 500 or 1000 Å layer of gold over a 50 or 100 Å layer of titanium, both vacuum deposited in an e-beam evaporator) were prepared on silicon wafers containing a native oxide layer (Silicon Quest International). Substrates were cut into 1 cm^2 squares, individually cleaned by sequential washings with acetone, deionized water, and ^{i}PrOH, and dried in a stream of dry nitrogen (N_2). The substrates were then soaked in a boiling solution of $H_2O/H_2O_2/NH_4OH$ (5:1:1) for 30 min, washed with water and ^{i}PrOH, and dried with dry N_2.

Surface Functionalization. In a typical procedure using gold substrates, self-assembled monolayers (SAMs) were formed by submerging freshly cleaned substrate squares in a filtered solution of thiol in absolute EtOH (typically 0.5 or 0.75 mM) for 24 h. The squares were then removed and washed, first with EtOH, then with ^{i}PrOH before being dried in a stream of dry N_2. Using Si/SiO_2 substrates, freshly cleaned squares were submerged for 6 h in a 0.5 wt% solution of trichlorosilane in pentane in a N_2 glovebox. The squares were then removed, sonicated for 5 min each in toluene (2 times), 50/50 toluene/acetone, and acetone, and dried in a stream of dry N_2.

Reaction of the olefin-functionalized substrates with catalyst was done in dichloromethane solutions of catalyst **1** or **2** (typically 13 or 25 mM) at room temperature (rt) or 40 °C. After the prescribed length of time, the squares were removed from solution, washed thoroughly with dichloromethane, and dried under N_2. They were then immediately placed in a fresh, filtered solution of norbornene in 1,2-dichloroethane and allowed to react for a prescribed length of time at rt or 40 °C. The squares were

then washed thoroughly with dichloromethane and dried under vacuum.

Device Construction. For the FETs using a gold strip as the gate electrode deposited on SiO_2 (both lamination and direct deposition methods), linker **4** and catalyst **2** were used. Catalyst attachment and norbornene polymerization were done at rt for 10 min and 15 min, respectively. The thickness of the polynorbornene film was 1.2 μm for the lamination devices, and ranged from 800 to 1100 nm for the direct deposition samples. In mobility calculations, a width (W) of 2–3 mm and length (L) of 1 mm were used for the laminated devices. A width of 940 μm and length of 240 μm were used for the direct deposition devices.

For the FETs using Si/SiO_2 as gate electrode, catalyst attachment was done with dichloromethane solutions of catalyst **1** or **2** at rt for 10 min, and the polymerizations were carried out with 1,2-dichloroethane solutions of norbornene (between 2 and 4 M) at rt, times varying between 15 and 40 min. The thickness of the polynorbornene films, which were very smooth and did not require annealing, ranged between 230 and 800 nm, but only those films thicker than 600 nm were used to make TFTs.

The organic semiconducting layer of pentacene (Aldrich) was deposited by thermal evaporation under vacuum (typically to a thickness of 300 Å). Gold overlayers were deposited in an e-beam evaporator under vacuum.

Characterization. Ellipsometric measurements were performed on a Rudolph Ellipsometer AutoEL. Profilometric measurements were measured using a Dektak 3030. Current-voltage characteristics were obtained with a Hewlett-Packard (HP) 4155A semiconductor parameter analyzer. AFM Tapping Mode data was acquired on a JEOL JSPM-4210 scanning probe microscope in a nitrogen environment. "NON-CONTACT ULTRASHAR" silicon cantilevers were purchased from NT-MDT, Ltd. Rutherford backscattering spectroscopy (RBS) and medium energy ion scattering (MEIS, a low energy ultrahigh resolution variant of RBS) were performed at the Rutgers University ion scattering facility. 1.5 MeV He ions (in RBS) and 100 keV protons (in MEIS) were used to quantify film composition and thickness.

5.4 Acknowledgements

The authors thank the National Science Foundation, Office of Naval Research, NJCOOE, and Lucent Technologies for financial support, and Dr. Brian Connell and Daniel P. Sanders for advice on this manuscript.

References Cited

[1] Rogers, J. A.; Bao, Z. *J. Polym. Sci. Part A: Polym. Chem.* **2002,** *40,* 3327–3334.

[2] Sheraw, C. D.; Zhou, L.; Huang, J. R.; Gundlach, D. J.; Jackson, T. N.; Kane, M. G.; Hill, I. G.; Hammond, M. S.; Campi, J.; Greening, B. K.; Francl, J.; West, J. *Appl. Phys. Lett.* **2002,** *80,* 1088–1090.

[3] Huitema, H. E. A.; Gelinck, G. H.; van der Putten, J. B. P. H.; Kuijk, K.; Hart, C. M.; Cantatore, E.; Herwig, P. T.; van Breemen, A. J. J. M.; de Leeuw, D. M. *Nature* **2001,** *414,* 599.

[4] Gelinck, G. H.; Geuns, T. C. T.; de Leeuw, D. M. *Appl. Phys. Lett.* **2000,** *77,* 1487–1489.

[5] Crone, B. K.; Dodabalapur, A.; Sarpeshkar, R.; Filas, R. W.; Lin, Y. Y.; Bao, Z.; O'Neill, J. H.; Li, W.; Katz, H. E. J. *Appl. Phys.* **2001,** *89,* 5125–5132.

[6] Performance as measured by mobility and on/off ratio. See Katz, H. E.; Bao, Z. J. *Phys. Chem. B* **2000**, *104*, 671–678.

[7] Halik, M.; Klauk, H.; Zschieschang, U.; Schmid, G.; Radlik, W.; Weber, W. *Adv. Mater.* **2002,** *14,* 1717–1721.

[8] Bao, Z. N.; Feng, Y.; Dodabalapur, A.; Raju, V. R.; Lovinger, A. *J. Chem. Mat.* **1997,** *9,* 1299–1301.

[9] Kawase, T.; Sirringhaus, H.; Friend, R. H.; Shimoda, T. *Adv. Mater.* **2001,** *13,* 1601–1604.

[10] Weck, M.; Jackiw, J. J.; Rossi, R. R.; Weiss, P. S.; Grubbs, R. H. *J. Am. Chem. Soc.* **1999,** *121,* 4088–4089.

[11] Juang, A.; Scherman, O. A.; Grubbs, R. H.; Lewis, N. S. *Langmuir* **2001,** *17,* 1321–1323.

[12] Kim, N. Y.; Jeon, N. L.; Choi, I. S.; Takami, S.; Harada, Y.; Finnie, K. R.; Girolami, G. S.; Nuzzo, R. G.; Whitesides, G. M.; Laibinis, P. E. *Macromolecules* **2000,** *33,* 2793–2795.

[13] Watson, K. J.; Zhu, J.; Nguyen, S. T.; Mirkin, C. A. *J. Am. Chem. Soc.* **1999,** *121,* 462–463.

[14] Bielawski, C. W.; Grubbs, R. H. *Angew. Chem., Int. Ed.* **2000,** *39,* 2903–2906.

[15] In general, films produced with linker **4** were thicker than those produced with linker **5**. Catalyst attachment is likely more efficient with **4**; the reasons for this are currently under investigation.

[16] Choi, T. L.; Grubbs, R. H. *Angew. Chem., Int. Ed.* **2003,** *42,* 1743–1746.

[17] Bao, Z. N.; Rogers, J. A.; Katz, H. E. *J. Mater. Chem.* **1999,** *9,* 1895–1904.
[18] Loo, Y. L.; Someya, T.; Baldwin, K. W.; Bao, Z.; Ho, P.; Dodabalapur, A.; Katz, H. E.; Rogers, J. A. *Proc. Natl. Acad. Sci. USA* **2002,** *99,* 10252–10256.
[19] Increased grain-size was observed when pentacene was deposited over SI-ROMP polymer layers that had been annealed.
[20] Inokuma, S.; Sugie, A.; Moriguchi, K.; Shimomura, H.; Katsube, J. *Heterocycles* **1982,** *19,* 1909–1913.
[21] Schwab, P.; Grubbs, R. H.; Ziller, J. W. *J. Am. Chem. Soc.* **1996,** *118,* 100–110.
[22] Sanford, M. S.; Ulman, M.; Grubbs, R. H. *J. Am. Chem. Soc.* **2001,** *123,* 749–750.
[23] Hu, J.; Fox, M. A. *J. Org. Chem.* **1999,** *64,* 4959–4961.