Chapter 7

Wideband, Cryogenic, Very-Low Noise Amplifiers

This chapter discusses design and measurements of two wideband LNAs designed on both the NGC and OMMIC processes. The first LNA is designed to cover 1–20 GHz with < 10 K noise temperature and > 30 dB gain cryogenically, and the second design covers 8–50 GHz. These designs were fabricated on both the 100% and 75% In NGC processes.

All of the MMIC LNAs employ common-source stages. Large devices with inductive source degeneration are used in first stages of the amplifiers to improve match and bring real part of optimum noise impedance, R_{opt}, close to 50 Ohm. Thus, the first stage tends to be the bandwidth-limiting stage and in order to compensate, inductive peaking is used to enhance high-frequency gain. Subsequent stages employ smaller transistors with shunt and/or series inductive peaking to achieve flat gain over the bandwidth. Furthermore, two-finger devices were used on all stages of all designs in order to avoid potential instability sometimes observed on devices with more fingers (assuming same total gate periphery) [95].

Because the transistor characterization results of the previous chapter were not available during design phase of the LNAs presented herein, they were designed using foundry small-signal models. In the case of NGC, the SSM was provided at a single bias point as mentioned previously and this model was used for LNA design. The OMMIC SSM is applicable at 300 K only, therefore the OMMIC LNAs were designed for room temperature.

7.1 Measurement Setups

7.1.1 Wafer-probed S-Parameters at 300 K

At least half of the MMICs fabricated in each foundry were first tested at room temperature using wafer-probes for S-parameters up to 50 GHz at a range of bias values. The bias values were selected to be fairly conservative as the goal of the tests were to confirm functionality rather than performance.

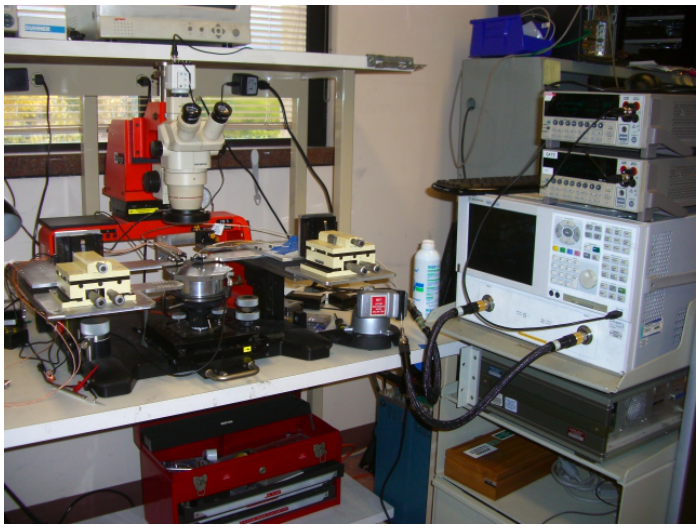


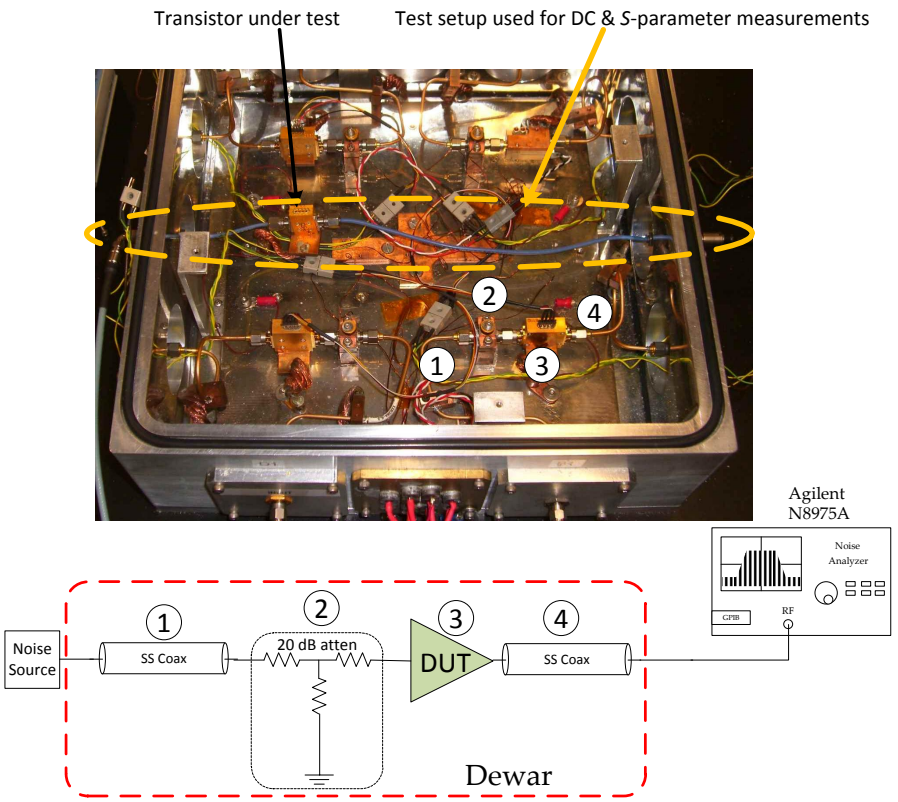
Figure 7.1: Photograph of the test setup for wafer-probed S-parameter measurements at 300 K. The bias is provided using three Keithley KE2400 DC supplies, one of which is not shown in the photo.

The test station employs Picoprobe's 67A-GSG-120 coplanar probes with 120 μm pitch. Calibration is performed using the GGB Industries' CS-5 calibration substrates with the appropriate calibration coefficients loaded onto the Agilent PNA. The calibration is checked periodically during tests to ensure there is no drift. A photo of the test setup is presented in Figure 7.1.

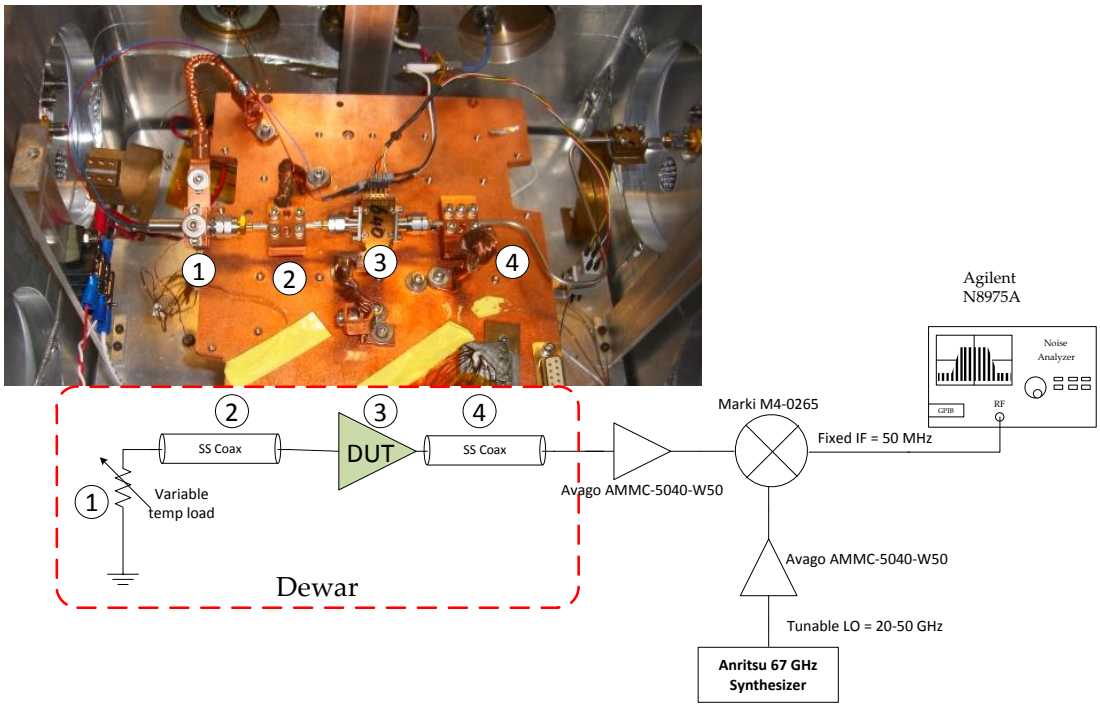
7.1.2 Cryogenic noise

Block diagrams of the cold attenuator and hot/cold load test setups used in LNA noise measurements are provided in Figure 7.2(a) and (b), respectively. The cold attenuator method is used for measurements up to 18 GHz. The input and output stainless steel coaxial cables are heat sunk to the 77 K stage. The test setup is regularly calibrated against a reference amplifier and the uncertainty in noise temperature measurements is ± 1 Kelvin.

Despite its significantly higher measurement duration, the hot/cold load setup is preferred for 50 GHz LNA measurements, because poor input return loss of the LNAs coupled with low ENR from the noise source above 30–35 GHz with the 10 dB cold attenuator produced unreliable results. The output of the device under test (DUT) is down-converted with a variable local oscillator (LO), which is provided by a 67 GHz Anritsu synthesizer and controlled by the noise figure analyzer (NFA), producing a fixed IF frequency of 50 MHz. The test setup works up to 50 GHz; however, uncertainty in measurements grows rapidly above 43 GHz due to gains of the post-amplifier and LO driver amplifier rolling off. The uncertainty up to 40 GHz is estimated to be ± 2 Kelvin.

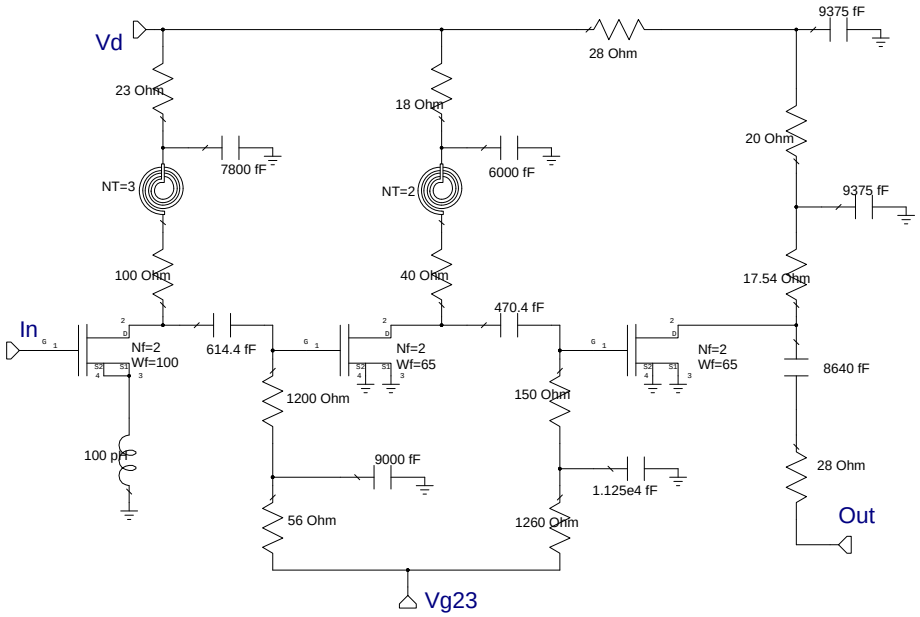


(a)

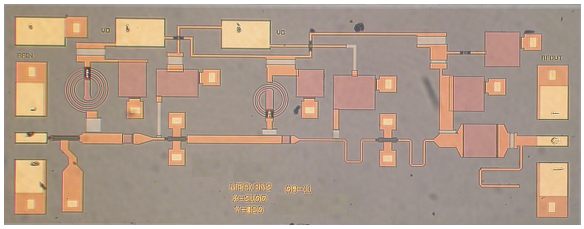


(b)

Figure 7.2: Block diagrams of the (a) cold attenuator, (b) hot/cold load test setups used for LNA noise temperature measurements



(a)



(b)

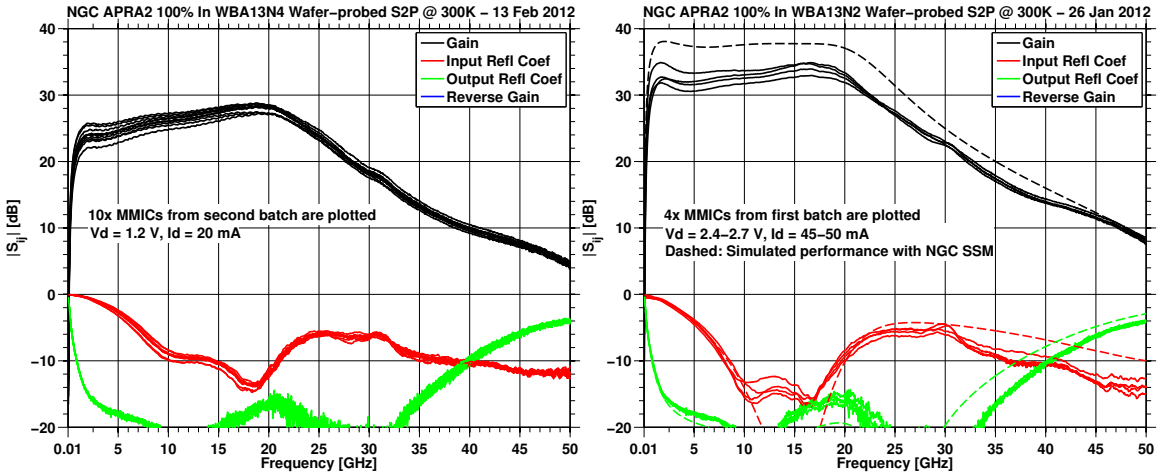
Figure 7.3: (a) Schematic, and (b) chip micrograph of the 1–20 GHz NGC LNA. In the schematic, Nf is number of fingers and Wf is finger length in micrometers of the transistor

7.2 NGC 1–20 GHz LNA

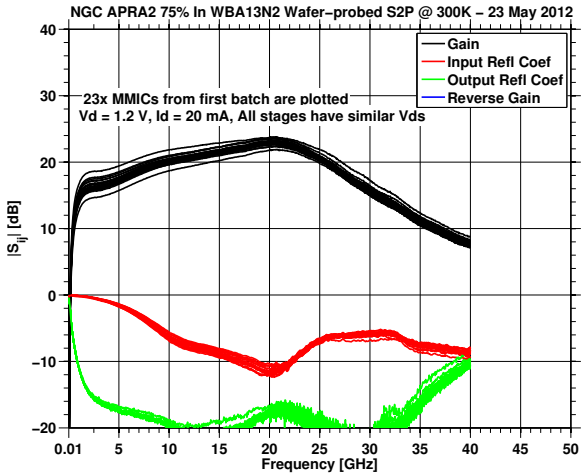
The NGC 1–20 GHz LNA consists of three stages with the following device sizes from input to output: 2f200, 2f130, and 2f130 μm. Figure 7.3 displays the schematic and chip micrograph of the LNA.

The wafer-probed S-parameters of MMICs from both the 100% and 75% In wafers appear in Figure 7.4. For the 100% In MMICs, two sets of curves with different bias conditions are presented. In the first case (left half of Figure 7.4(a)), the 100% In MMICs are biased at $V_{DS} = 1.2$ V, $I_{DS} = 20$ mA with gate biases chosen such that all three stages of the MMIC have approximately 0.7 V drain-source voltage drop on the transistor. This is also what was done for the 75% MMICs in part (b). This corresponds to about 20 mA/mm current density in the first stage, which is very low for room-temperature operation. In the right half of part (a), the MMICs are biased at higher drain voltage and current which is closer to the bias of the original SSM.

A large gain slope is observed on LNAs from either process at low bias. The reason for this is



(a)



(b)

Figure 7.4: Wafer-probed S-parameters of NGC 1–20 GHz LNAs from (a) 100% and (b) 75% In wafers. In part (a), two sets of curves are shown with different bias conditions. The simulated performance of the MMIC using NGC 100% In SSM is plotted using dashed lines biased at $V_{DS} = 1$ V and I_{DS} =300 mA/mm (i.e., $\sim$ 140 mA total MMIC drain current). Chips from the first and second batches are from the same wafer and are identical.

three fold:

1. The first stage has the biggest transistor and thus, has the highest gain at low frequencies and when it is biased at such low current density, the low-frequency gain suffers due to the fact that the gain of the stage is a function of the gate-to-drain capacitor C_{gd} in addition to the transconductance. The reason the first-stage bias was so low is due to a design error in selecting appropriate resistor values for the drain resistors of each stage. In particular, the first stage has the highest resistor value on the drain. This error has somewhat smaller impact in packaged LNA results, because the on-chip drain bias line was cut and two separate drain voltages were provided to the chip;

2. Series inductive peaking used in between second and third stages to increase the gain bandwidth to 20 GHz. This causes a bias-dependent gain peak at the upper end of the frequency band and exacerbates the gain slope;

3. Difference in the foundry-specified SSM and the observed discrete device characteristics.

Another observation from these plots is the lower gain of the 75% In devices by about 5-8 dB when biased similarly to the 100% MMICs. This is in agreement with the discrete device measurements of the previous section where it was observed that the 75% In g_m was roughly 20% lower. When biased at higher drain voltage and current, the 100% MMICs display fairly good input and output match despite the limitations in small-signal modeling. There is still a sizable gain slope and the "average" gain is lower than that predicted by the SSM which also agrees with the difference in measured g_m and that predicted by the small-signal model.

A wafer-probed MMIC is then installed in a coaxial package as shown in Figure 7.5. The input matching network has not been optimized and is a 70 Ω transmission line on a 15-mil-thick Duroid 6002 printed circuit board (PCB) followed by a section of 50 Ω microstrip on 15-mil-thick alumina board. The first-stage gate bias is brought in via a 5 kΩ resistor. The off-chip bypassing is accomplished by three 47pF Skyworks single-layer capacitors next to the chip in addition to 0.01 μF surface-mount capacitors on the DC board. The input AC coupling capacitor is a Skyworks 22pF single-layer capacitor. The on-chip drain bias line on the MMIC is cut and two drain bias voltages are provided. In particular, the first-stage drain bias is connected to the drain power supply directly with some bypassing. The drain bias of the second and third stages, however, have a series 50 Ω resistor (appears right above the three bypass capacitors next to the chip in Figure 7.5) in order to reduce the intrinsic drain voltage on these transistors when the MMIC is biased to optimize first-stage performance.

The measured and simulated scattering parameters and input noise temperature of the LNA at 22 K physical temperature are provided in Figure 7.6 along with the measured noise and gain of the 75% In MMIC in green. The simulations are performed by modifying g_m and g_{ds} of the

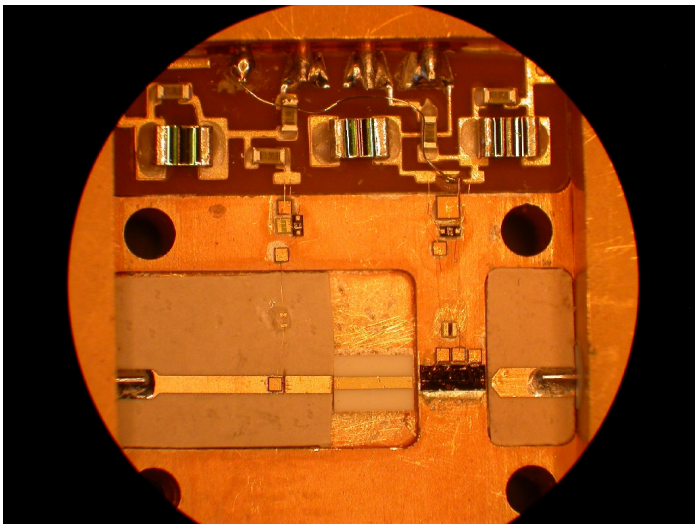


Figure 7.5: Photograph of the NGC 100% In 1–20 GHz LNA

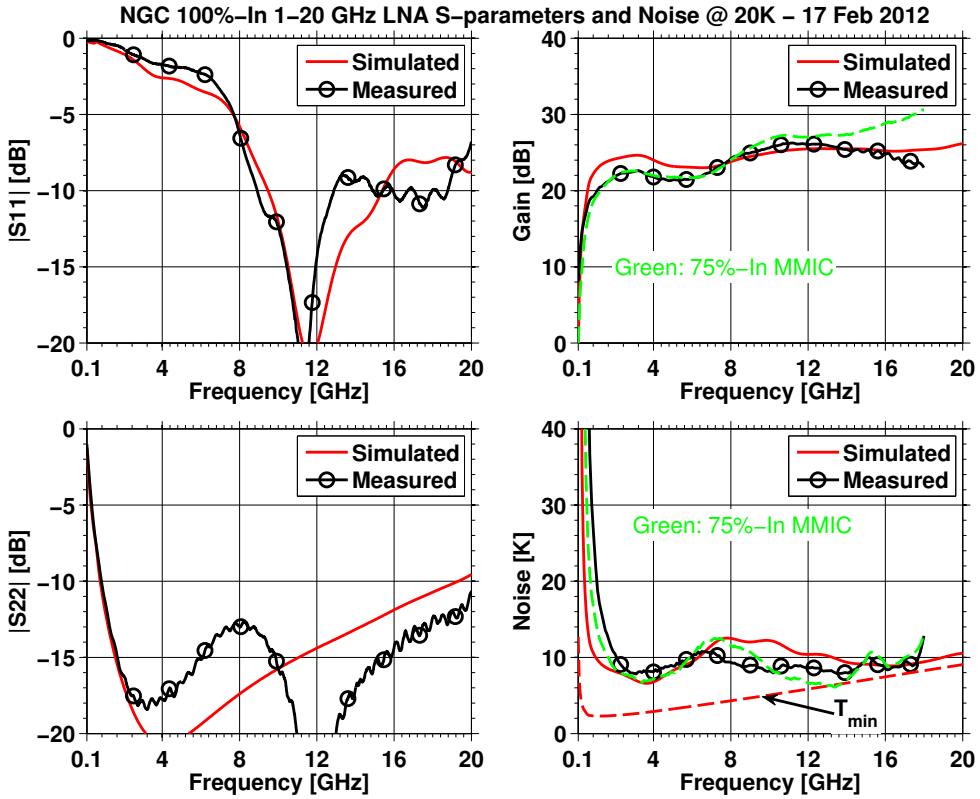
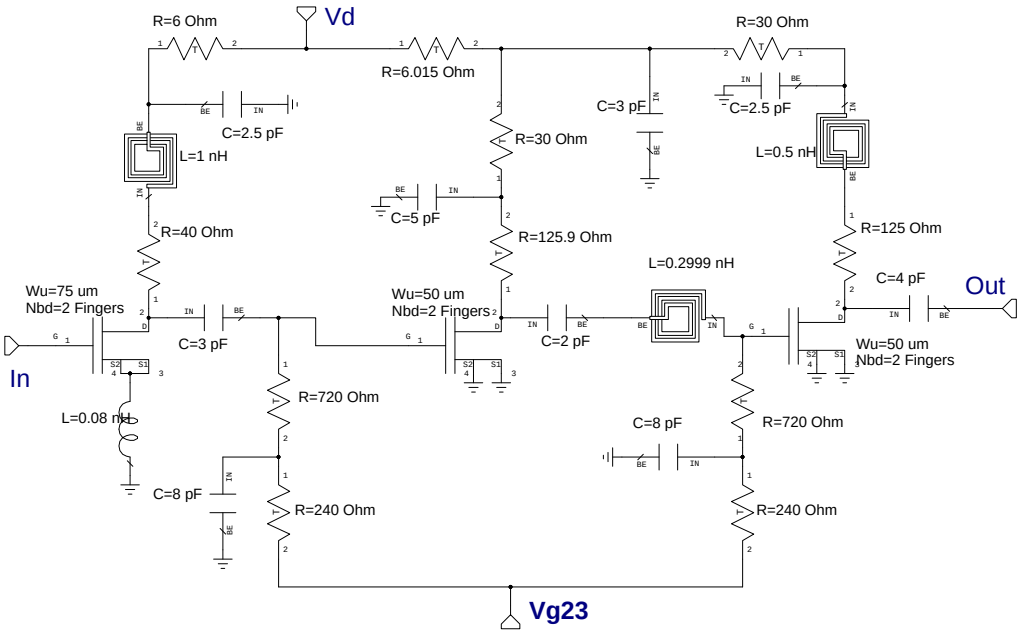


Figure 7.6: Comparison of simulated (red) and measured (black) performance of the 1–20 GHz LNA on NGC's 100% In 35 nm process at 22 Kelvin physical temperature. The supply voltage is 1.2 V with total drain current of 12.6 mA. Simulations include the input matching network. The green dashed gain and noise curves are measured results of the 75% 1–20 GHz LNA.

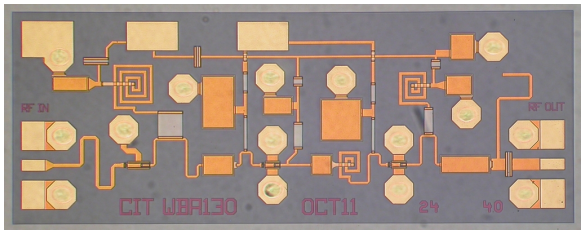
SSM per discrete HEMT measurements of the previous chapter at the measured bias for each stage. The agreement between the modeled and measured S-parameters is quite good considering the aforementioned limitations. The input return loss is poor below 7 GHz and is approximately 10 dB or higher from 10 to 18 GHz. Comparison of Figures 7.4 and 7.6 reveals that the primary reason for the poor input return loss is the matching network. It has not been optimized at all and was pieced together using available parts in the laboratory. The output return loss is higher than 10 dB over the entire frequency band.

The measured noise is $\leq$ 10 K from 2 to 17 GHz and compares well with the simulations which also use the results of the T_{drain} measurements from the previous chapter. It is seen that the minimum noise temperature of the MMIC is notably higher than that of a single transistor. One of the reasons for this is the inclusion of a shot noise source between gate and drain of the first-stage device whose power spectral density is taken to be proportional to total gate current instead of sum of absolute values of I_{GD} and I_{GS} because these were not measured. Due to the high R_{opt}, this noise source degrades T_{min} by approximately 1 Kelvin for 0.5 μA gate leakage on the 100% devices. The increased T_{min} may also be due to the fact that the MMIC was not measured at the optimum noise bias; however, the effect of this is thought to be quite small given the fairly flat T_{min} versus bias performance demonstrated in Chapter 6. Furthermore, the T_{min} value calculated in the previous chapter is for a four-finger device versus the two-finger transistors on the MMIC. Nevertheless, the measured noise approaches T_{min} at the upper end of the band.

Four 100% and one 75% MMICs were tested cryogenically. All of the 100% LNAs suffered from low-frequency oscillations and the results presented herein are from the only 100% LNA measurement that yielded respectable noise over the desired frequency range without stability issues. The oscillations, which were not observed on the 75% MMIC, mainly occurred below 1 GHz and exhibited strong dependence on bias of the second and third stages. Many tests have been performed to pinpoint the source of the instability such as measuring the same MMIC in different coaxial packages, trying many different off-chip bypass arrangements including different capacitor values, different resistor values in between capacitors to prevent resonance, etc. Moreover, it was noted that the MMICs oscillated even with the first stage pinched off. All of these empirical observations combined with the fact that 75% MMIC could not be made to oscillate suggest impact ionization, especially the strong inductive behavior of the drain impedance, as the source of the instability. In fact, understanding these results was one of the motivations for the discrete HEMT characterization of the previous chapter.



(a)



(b)

Figure 7.7: (a) Schematic, and (b) chip micrograph of the 1–20 GHz OMMIC LNA. In the schematic, Nbd is number of fingers and Wu is finger length in micrometers of the transistor.

7.3 OMMIC 1–20 GHz LNA

This LNA was designed primarily for cryogenic use but the design utilizes the OMMIC design kit SSM values intended for 300K. Fortunately, good results were obtained at both 300K and 20K temperatures. The amplifier consists of three common-source stages with 2f150, 2f100 and 2f100 μm transistors. The schematic and chip micrograph appear in Figure 7.7.

Figure 7.8 plots the wafer-probed S-parameter measurements of the first eight MMICs biased identically which, due to small threshold voltage variations, yields slightly different drain currents. It is seen that there is excellent uniformity in performance at 300 K. Furthermore, at this conservative bias the chips have $>$ 30 dB gain up to 25 GHz as opposed to the design target of 20 GHz. The input impedance is poor but matchable to 50 Ω beyond 10 GHz. The output return loss is decent, but worse than the simulated performance of $>$ 10 dB.

One of the wafer-probed MMICs, serial number 2416, is installed in a coaxial package as shown

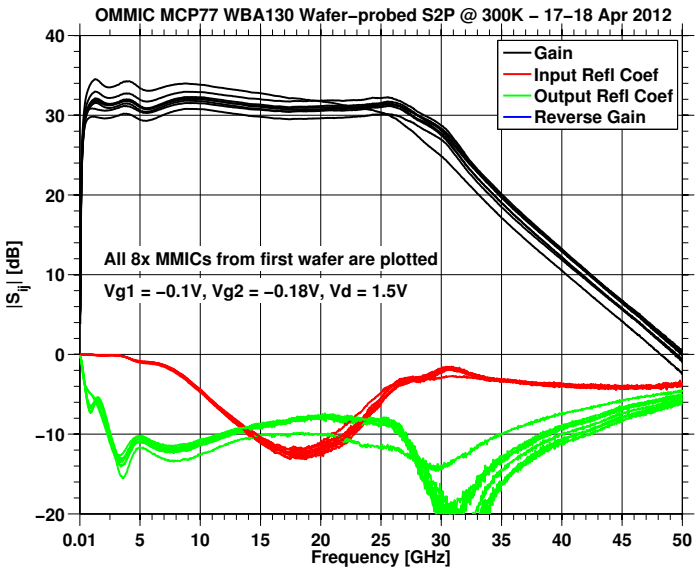


Figure 7.8: Wafer-probed S-parameters of eight OMMIC 1–20 GHz LNAs. The MMICs are biased at identical gate and drain voltages with $I_{DS} = 20 - 25$ mA.

in Figure 7.9. The input matching network has not been optimized and is a simple, 9.5 mm-long, 70 Ω transmission line on a 15-mil-thick Duroid 6002 PCB. It is made by stitching together parts of existing PCBs in the lab. The first-stage gate bias is brought in via a 10 kΩ resistor. The off-chip bypassing is accomplished by 68pF Skyworks single-layer capacitors next to the chip in addition to 0.01 μF surface-mount capacitors on the DC board. The input AC coupling capacitor is a Skyworks 22 pF single-layer capacitor. The measured best input noise temperature and the corresponding S-parameters at room temperature are plotted in Figure 7.10 at the optimum noise bias along with the simulated performance. The simulations are performed at the measurement bias using the discrete device measurements presented previously. The agreement between the two data sets is excellent.

The measured gain is approximately 38 dB and the gain flatness is very good. The measured input match is slightly worse than the simulations which is likely due to small parasitic effects in the SMA connector, the input matching network and the single-layer AC coupling capacitor at the MMIC input. The input return loss needs improvement across the entire frequency range. However, it is worth pointing out that the input return loss of the MMIC alone is better than this performance, and the degradation is mainly due to the input matching network which is not matching the input but bringing the input impedance closer to Z_{opt} of the MMIC. The output match is better than 10 dB from 1.5 to 16 GHz. The input noise temperature at 300 K is impressive, < 80 K (noise figure < 1.06 dB) up to 16 GHz.

Similar to the NGC 1–20 GHz LNA, the simulated MMIC minimum noise temperature deviates from that of the transistor. While the gate leakage of the OMMIC devices are much lower than that of NGC 100% In devices, it still contributes non-negligible noise due to 300 Kelvin ambient

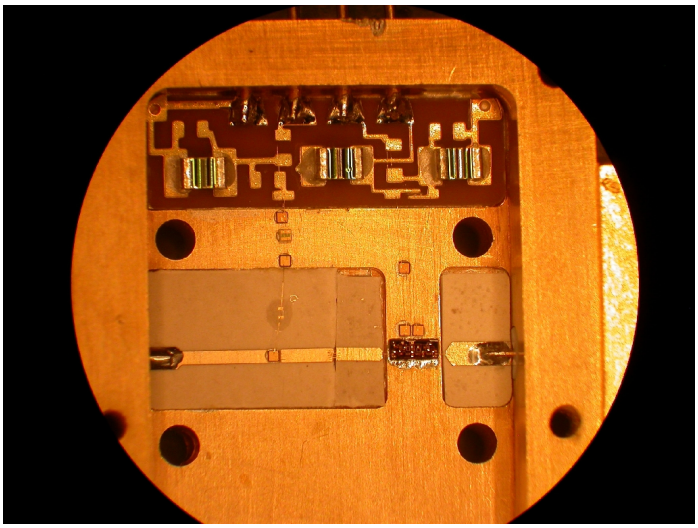


Figure 7.9: Photograph of the OMMIC 1–20 GHz LNA

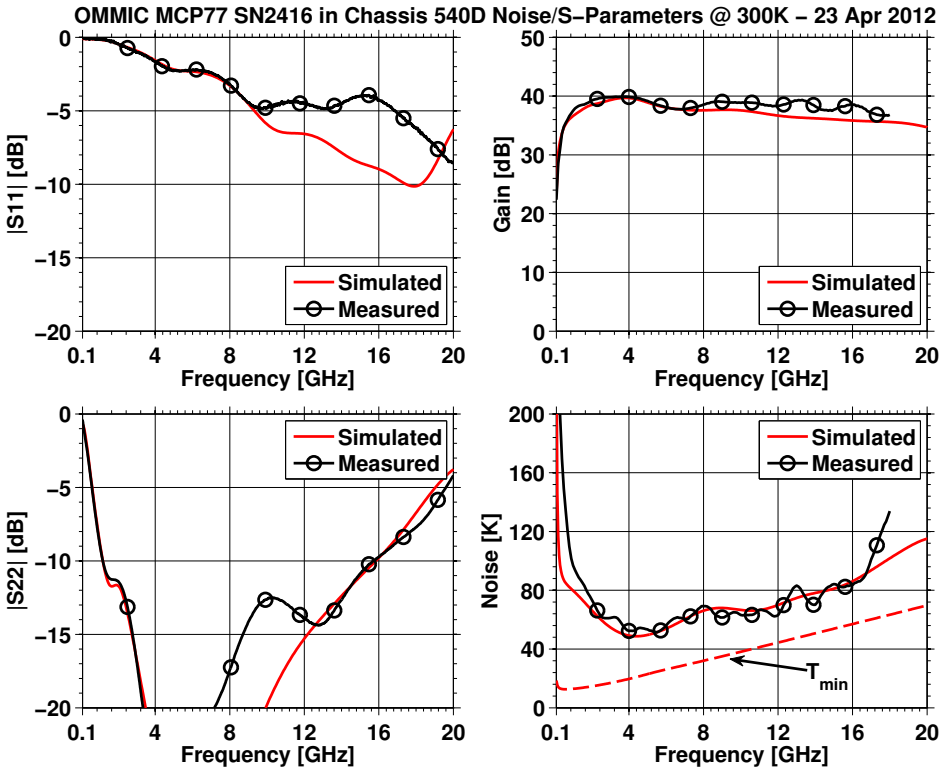


Figure 7.10: Comparison of simulated and measured performance of the 1–20 GHz LNA on OMMIC's D007IH process at 300 Kelvin physical temperature. Agreement between the two data sets is excellent with the exception of a constant gain offset versus frequency. The supply voltage is 2 V with total drain current of 38 mA. Simulations include the input matching network.

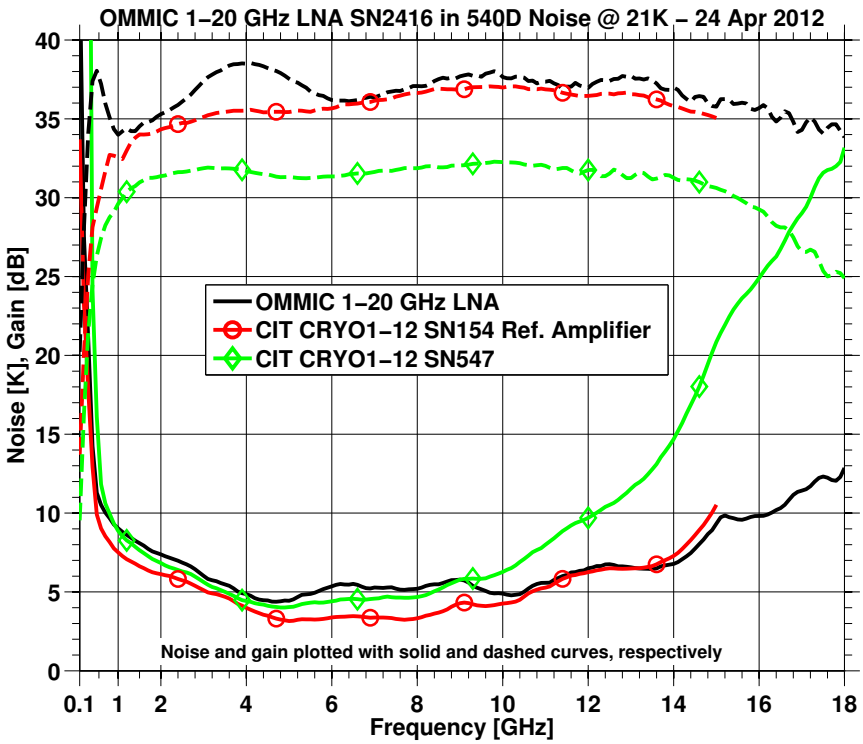


Figure 7.11: Measured input noise temperature and gain of the OMMIC 1–20 GHz LNA at 21 Kelvin physical temperature showing excellent performance over more than two decades of bandwidth (i.e., 0.7 to 16 GHz). The supply voltage is 1 V with total drain current of 16 mA. Also plotted is the performance of a typical and the best 1–12 GHz 130 nm InP LNAs both developed at Caltech.

temperature, e.g., from 5 to 13 K at 1 GHz and 23 to 26 K at 6 GHz due to 1.4 μA gate leakage current. Another reason for the difference is loss preceding the transistor which is very small, but contributes significant noise at 300 K. Another point the T_{min} curve underlines is the sub-optimal input matching network design at the upper end of the frequency band.

The cryogenic input noise temperature and gain of this LNA appear in Figure 7.11 along with those of a typical and the best (reference) 1–12 GHz LNAs developed at Caltech. This LNA achieves $<$ 10 K noise from 0.7 to 16 GHz and 12 K at 18 GHz with measured noise on the order of 5 K from 4 to 10 GHz. In comparison with the typical 130 nm, InP-based, 1–12 GHz LNA, the OMMIC LNA provides much improved noise above 9 GHz. Overall, it works as well as the best InP-based amplifier while its biggest disadvantage is the poor input match as shown in Figure 7.12, which is addressed in the next design iteration (see Section 7.6).

LNAs consuming very low DC power are of interest to THz astronomy where they serve as IF amplifiers following SIS or HEB mixers operating at or below 4 K ambient temperature. In such an application, reducing power consumption decreases the total heat load on the cooler and enables collocation of the LNA and the mixer. The OMMIC 1–20 GHz LNA exhibits $<$ 10 K from 2 to 14 GHz at 3 mW DC power consumption, as shown in Fig. 7.13. While not shown here for brevity,

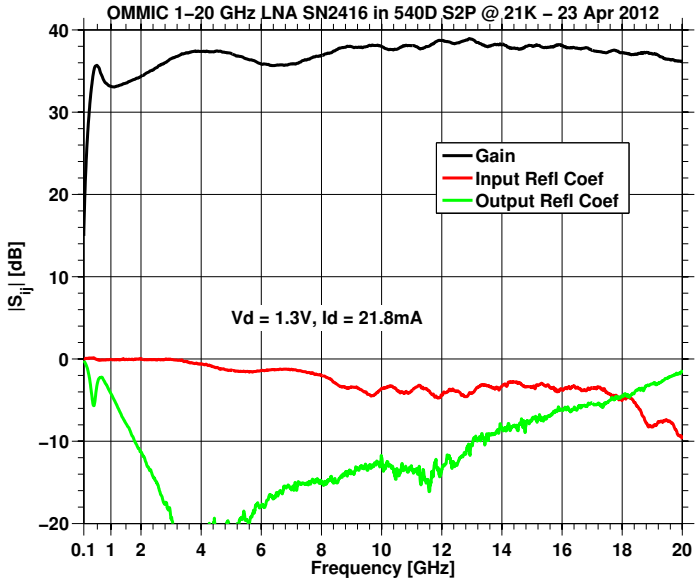


Figure 7.12: Measured cryogenic scattering parameters of the 1–20 GHz OMMIC LNA. The bias is slightly different than that of the noise measurements; however, the performance difference was observed to be very small.

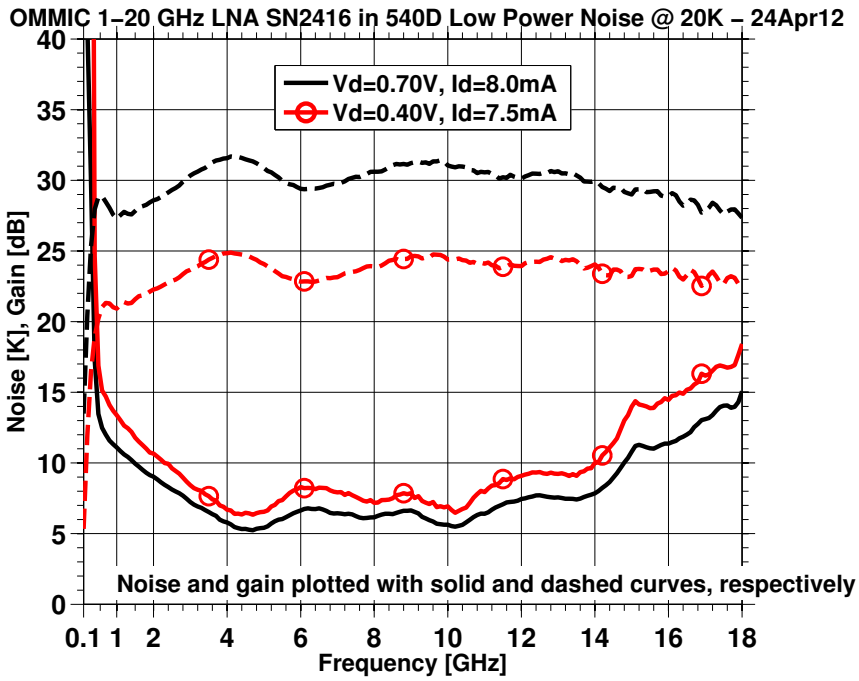
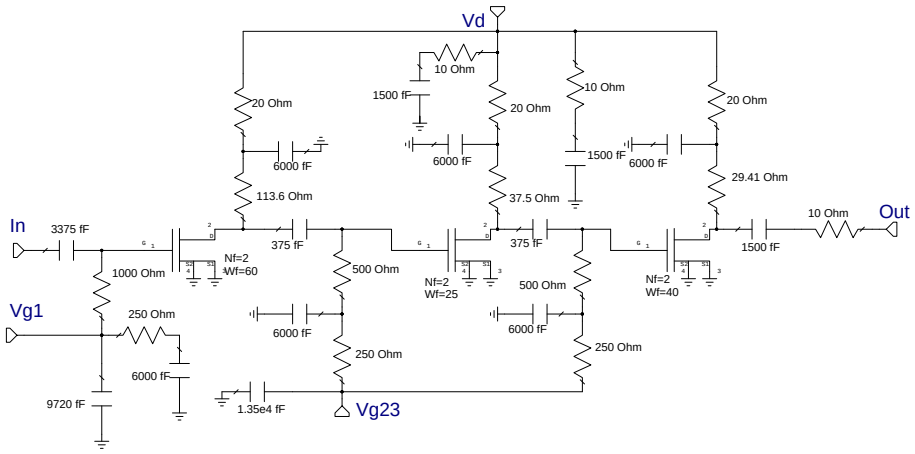
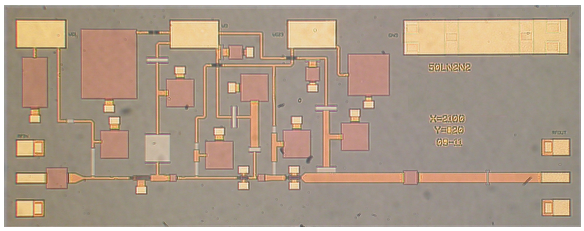


Figure 7.13: Measured cryogenic noise and gain of the 1–20 GHz OMMIC LNA under low-power operation

it achieves $>$ 15 dB power gain and $\sim$ 20 K input noise temperature at 8 GHz with less than 1 mW power consumption from 0.25 V drain supply. As such, it is a very attractive candidate for IF amplifiers in following superconducting mixers, especially if the LNA is collocated with the mixer such that impact of poor input match is minimized.



(a)



(b)

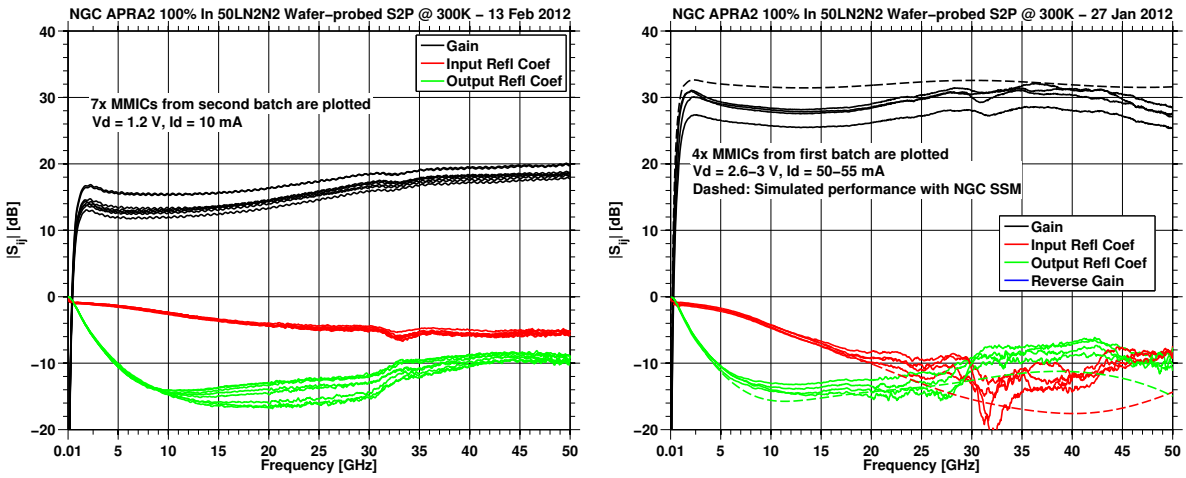
Figure 7.14: (a) Schematic, and (b) chip micrograph of the 8–50 GHz NGC LNA

7.4 NGC 8–50 GHz LNA

The 8–50 GHz LNA comprises three stages with 2f120, 2f50 and 2f80 μm transistors. Unlike the lower frequency LNAs, the first-stage gate bias is on chip. A chip micrograph and the LNA schematic are provided in Figure 7.14.

The wafer-probed, room-temperature scattering parameters appear in Figure 7.15 for two bias conditions. Similar to the 1–20 GHz NGC LNAs, the MMICs exhibit more gain variability with frequency in comparison with the simulations and significant gain slope under low bias which is again due in part to error in drain resistor value. Unlike the low-frequency LNAs, however, the input and output match of the MMICs operated near the NGC SSM bias are notably worse than simulations. Results from 75% In MMICs are not included due to very limited testing performed on those chips.

A V-band chassis was designed to test the 50 GHz MMICs in a coaxial package. It uses Anritsu V-band glass beads and sliding contacts to make solid electrical connection with the 5-mil-thick, 50 Ω alumina boards at the input and the output. Similar to the other LNAs presented above, the off-chip bypass capacitors are 47 pF Skyworks single-layer capacitors. While this MMIC also suffers from the design error regarding the drain resistor values, the on-chip drain line is not cut and one common drain voltage is used. It is reasonable to expect some improvement in the results presented



(a) (b)

Figure 7.15: Wafer-probed S-parameters of NGC 100% In 8–50 GHz LNAs with total drain current of approximately (a) 10 mA at 1.2 V, and (b) 50 mA at 2.8 V. Chips from the first and second batches are from the same wafer and are identical.

in this section if the drain lines were to be separated between first and subsequent stages.

The measured and simulated scattering parameters and input noise temperature are provided in Figure 7.17, where the simulations incorporate the measured g_m, g_{ds}, and T_{drain} in the small-signal model. The only caveat is that T_{drain} values from measurements were reduced manually because otherwise the simulated noise was considerably higher than measured noise throughout the band. This manual adjustment is in line with the earlier observation that impact ionization increases T_{drain}, but this should mostly be at low frequencies, i.e., < 10 GHz and the noise performance at higher frequencies should not be affected as severely. Nevertheless, the manually adjusted T_{drain} values are still obtained from measurements, but at a bias point prior to onset of impact ionization.

The agreement between predictions and measurements is mediocre for input and output return loss. This is primarily due to inadequate modeling of the V-band glass-bead and sliding contact attachment to the 50 Ω alumina traces. Nonetheless, the simulations are fairly close to the "mean" level of measurements for most of the frequency band. The measured gain is, as expected, low and exhibits considerable slope.

The simulated and measured noise performance are somewhat different, especially above 20 GHz due in part to inadequate modeling of the MMIC packaging. In spite of that, the measured noise temperature is still ≤ 20 K from 6 to 40 GHz at 30 mW power consumption and is reasonably close to simulated minimum noise temperature T_{min} above 20 GHz. Also plotted in the same figure is the input noise temperature of another MMIC (green dashed) which exhibits better performance, i.e., $T_n \sim T_{min}$ throughout the upper half of the frequency range. This improvement is due to two factors:

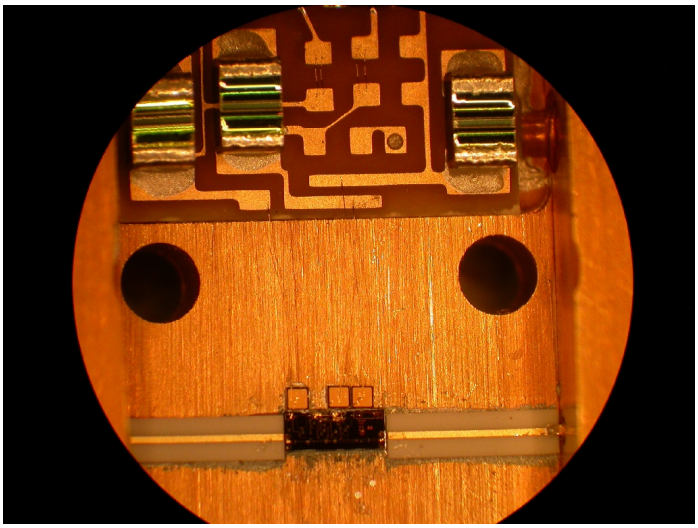


Figure 7.16: Photograph of the NGC 100% In 8–50 GHz LNA

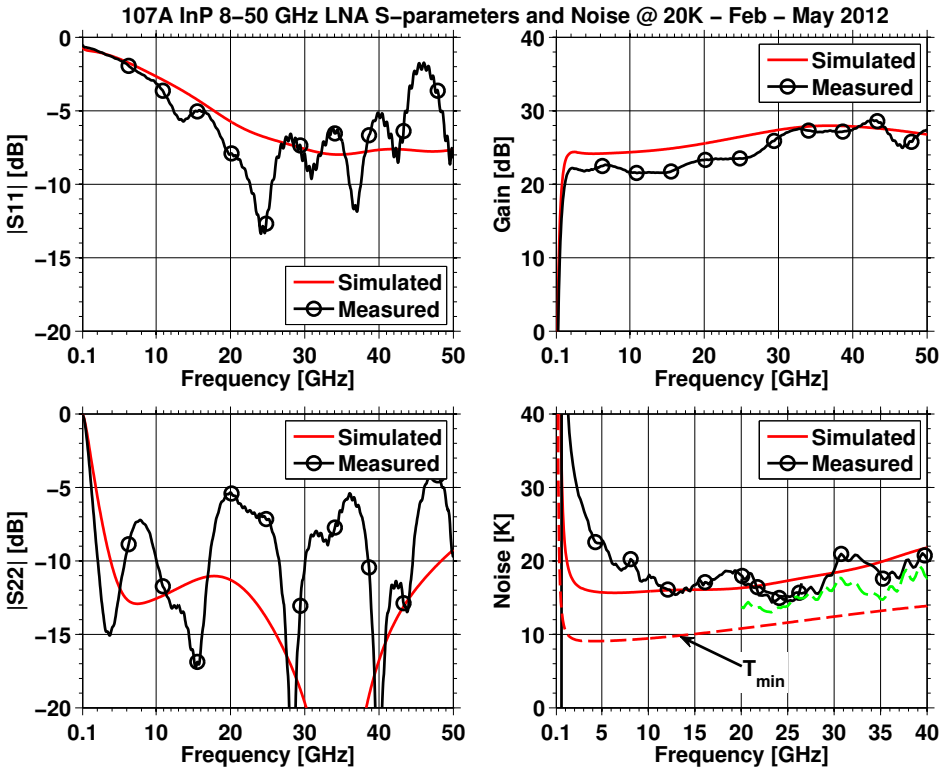
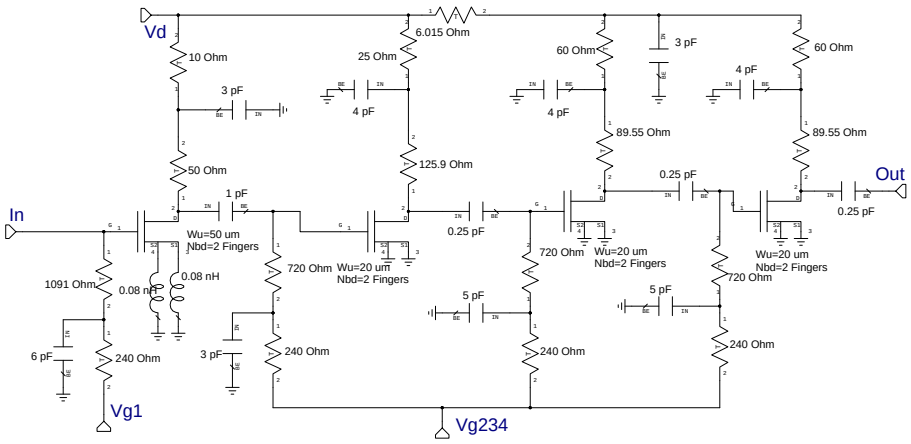


Figure 7.17: Comparison of simulated (red) and measured (black) performance of the 8–50 GHz LNA on NGC's 100% In 35 nm process at 22 Kelvin physical temperature. The supply voltage is 1.3 V with total drain current of 23.6 mA. Also plotted in green dashed is measured noise of another 8–50 GHz 100% In MMIC.

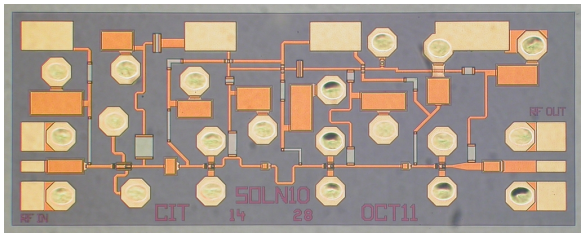
1. Improvements to the test setup: A few months after the initial MMIC was tested, an attenuator was incorporated following the DUT outside the dewar and the post-amplifier bias was adjusted. Prior to these changes, the second MMIC performed almost identical to the one plotted in black;

2. Packaging: Some time after the tests, it was noticed that the V-band sliding contacts were not epoxied as instructed by Anritsu;

The first MMIC could not be tested after these changes, because it was re-used elsewhere. However, it is reasonable to conjecture that the test setup and the sliding contact attachment may have had a signature on the results. The as-measured noise performance of this amplifier is somewhat higher than the existing cryogenic LNAs, but may possibly be closer to the state of the art once more careful and reliable tests are performed. In addition, this LNA spans much wider frequency range than the currently available ones, most of which usually only cover a waveguide band, e.g., 26–40 GHz.



(a)



(b)

Figure 7.18: (a) Schematic and (b) chip micrograph of the 8–50 GHz OMMIC LNA

7.5 OMMIC 8–50 GHz LNA

The final LNA presented is the 8–50 GHz OMMIC design, which, unlike the other designs, is a four-stage amplifier. The first stage consists of a 2f100 μm device followed by three stages employing 2f40 μm transistors. The first-stage gate bias is once again on chip. The circuit schematic and a chip micrograph appear in Figure 7.18.

The first nine MMICs were wafer-probed at 300 K and their S-parameters are displayed in Figure 7.19 along with the expected performance per simulations. The most important observation is the large gain slope. The gain peaks around 50 GHz and the peak location in frequency exhibits strong bias dependence. The input and output return loss both approach 0 dB near the gain peak. Moreover, both deviate considerably from simulations as the gain slope starts to dominate the frequency response. This suggests that these are all due to the same phenomenon which is thought to be due to feedback from the output of the fourth stage to that of the second stage. The only way a similar effect could be reproduced in simulations was by tweaking the resonance frequency of the bypass capacitors on the second-stage drain and the drain bias line such that their response becomes inductive at lower frequency than the OMMIC SSM predicts.

The MMIC is installed in the same V-band package as the NGC 50 GHz LNA. The gate DC bias lines have series resistors to prevent possible resonance with the surface-mount capacitors.

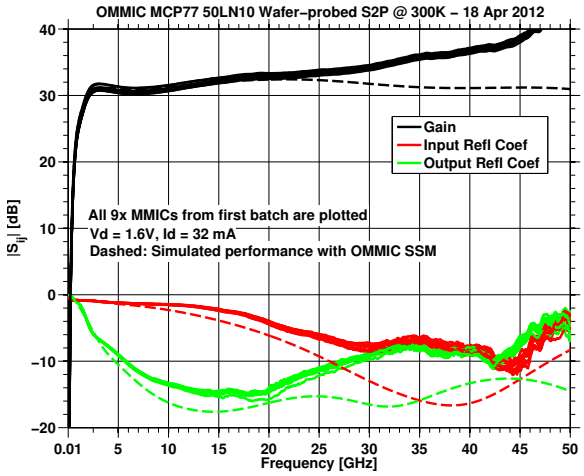


Figure 7.19: Wafer-probed S-parameters of nine OMMIC 8–50 GHz LNAs biased with total drain current of 32 mA at 1.6 V. Simulated performance is plotted using dashed curves.

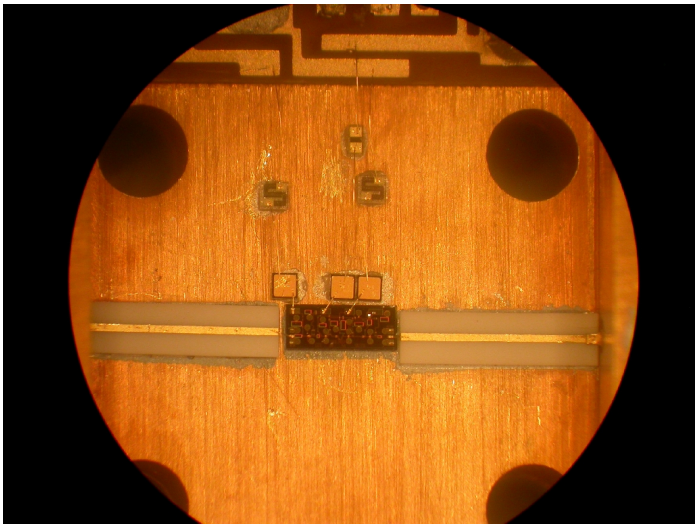


Figure 7.20: Photograph of the OMMIC 8–50 GHz LNA

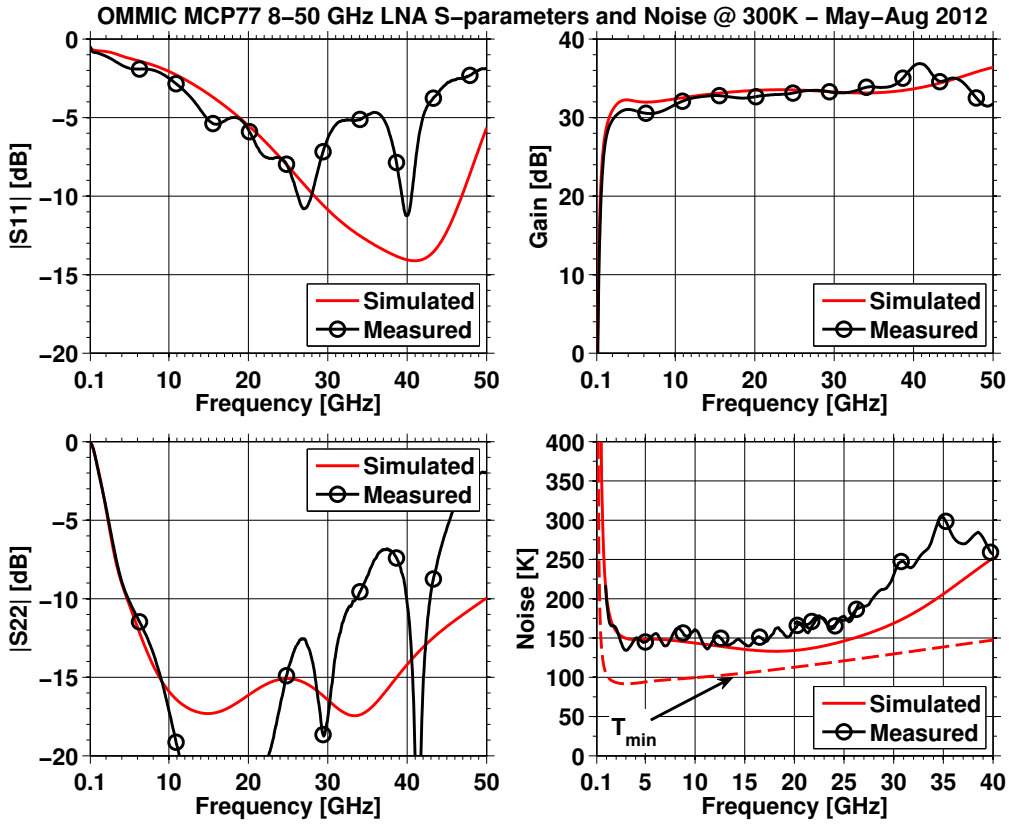


Figure 7.21: Comparison of simulated (red) and measured (black) performance of the OMMIC 8–50 GHz LNA at room temperature. The supply voltage is 1.85 V with total drain current of 35 mA.

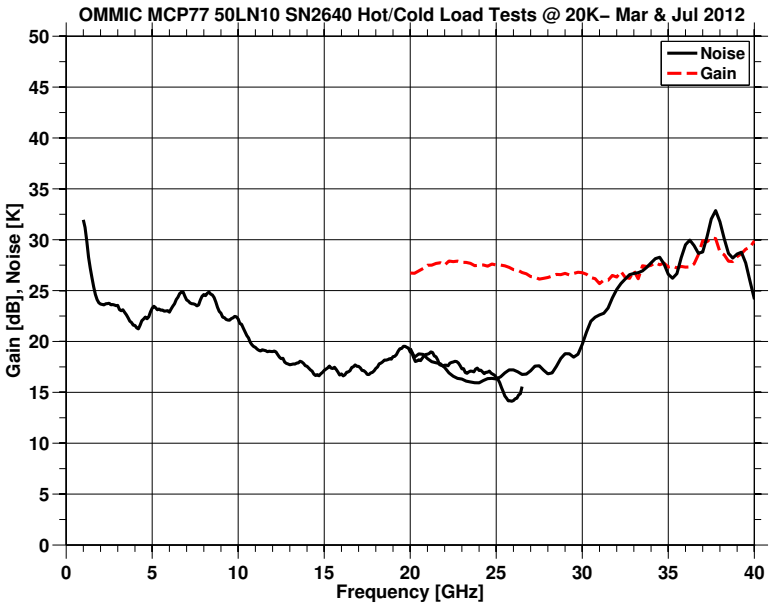


Figure 7.22: Measured input noise temperature (black solid) and gain (red dashed) of the OMMIC 8–50 GHz LNA at 21 Kelvin physical temperature. The supply voltage is 1 V with total drain current of 11 mA. Cryogenic gain was not measured between 1 and 20 GHz.

Also included is a series 10 Ω resistor on the drain bias line for the same purpose. The measured performance at room temperature is compared to simulations in Figure 7.21. The agreement between the data sets is quite reasonable, especially up to 30 GHz. The room-temperature noise performance is poor compared to other published results [24]; however, this LNA covers a much wider frequency range, nearly a decade bandwidth. The degradation in noise above 30 GHz is also thought to be related to the feedback mechanism mentioned above.

Finally, Figure 7.22 presents cryogenic noise and gain of the LNA which was measured after the 50 GHz noise test set was upgraded (see Section 7.4). The noise is 5-10 K higher than the NGC 50 GHz LNA and the gain is somewhat lower. The latter is related to the DC bias which is quite low. It was selected to minimize 40 GHz noise by measuring the noise temperature of the MMIC using the hot/cold load method at a single frequency (the same approach was used for the NGC 50 GHz LNA). Overall, the performance is respectable given the DC power consumption; however, it needs improvement to be useful in radio astronomy.

7.6 Revised Designs

As alluded to earlier, revised designs are submitted to both foundries. The revisions were primarily made based on the discrete device characterization results of the prior chapter with the exception of the T_{drain} results which were not available at the time.

In particular, the revised NGC 1–20 GHz LNA was targeted for the 75% In wafer whereas the revised 8–50 GHz LNA is intended for the 100% In wafer. Number of changes were kept to a minimum to reduce uncertainty as much as possible with the primary improvements being:

1. the drain resistor design error was fixed on both LNAs which will enable operation in wider range of DC bias;
2. all stages are designed to operate with low intrinsic drain-source voltage, e.g., ˜ 0.4–0.5 V;
3. $>$ 30 dB gain with much less slope;
4. improved input and output return loss at the target DC bias point;
5. drain bias lines of the first and subsequent stages are separated on chip to reduce potential feedback. The MMICs are still designed to operate off of a single drain supply; however, the two on-chip drain lines are intended to be tied together after RF bypassing.

Only the OMMIC 1–20 GHz LNA is revised for the second iteration and it is split into two designs: 1) 1-18 GHz LNA; 2) 1–12 GHz LNA. For both, the primary goal was to improve input return loss while maintaining, or if possible improving, all other performance metrics. The revisions, again based on discrete transistor measurements, were a bit more "radical" on these designs and include:

1. all stages are designed to operate with low intrinsic drain-source voltage, e.g., ˜ 0.4–0.5 V;
2. transistors with four or more fingers are employed instead of two-finger devices only;
3. drain bias lines of the first and subsequent stages are separated like the new NGC MMICs;
4. better than 10 dB input return loss for $f > 5$ GHz and much better output return loss on both designs;
5. 1–12 GHz LNA employs feedback for the first time in published HEMT LNA literature and also employs large first- and second-stage devices. This increases power consumption but helps reduce low-frequency noise in addition to bringing R_{opt} closer to 50 Ω.

7.7 Cryogenic Performance of Coupling Capacitors

The 1–20 GHz LNAs presented herein do not have on-chip gate bias for the first stage. Consequently, the packaged amplifiers employ off-chip, single-layer AC coupling capacitors which must be resonance-free over the entire bandwidth of the MMICs and low loss to ensure impact on input noise temperature and S-parameters of the LNA is minimal. In order to quantify the impact of coupling capacitors on measured noise of amplifiers, cryogenic microwave performance of five capacitors, four single-layer and one surface-mount, are evaluated. In particular, effective noise contribution of each capacitor is calculated using cryogenic scattering parameter measurements. The five capacitors tested to date are:

1. Dielectric Labs Milli-Cap 82 pF multi-layer, size 50 mil by 20 mil;
2. Presidio Components 4 pF, size 12 mil by 12 mil;
3. Presidio Components 10 pF, size 15 mil by 15 mil;
4. Skyworks 10 pF, 9 mil by 12 mil;
5. Skyworks 22 pF, 15 mil by 18 mil.

Each capacitor is mounted, in series configuration, in a V-band package (same as the one used for 50 GHz LNAs) with 50 Ω input and output alumina microstrip lines. The packaged capacitor is characterized by measuring its S-parameters up to 50 GHz both at room and cryogenic temperatures. The packaging effects on the measurements are mostly de-embedded via measurements of a thru package. The cryogenic measurements were performed at 77 K by dipping the packaged capacitor in liquid nitrogen (Figure 7.23). In the following, the capacitor performance is assumed unchanged from 77 to 22 K.

Let the effective loss of the capacitor be defined as the reciprocal of its available gain with $R_{gen} = 50\,\Omega$, i.e.,

$$L_{eff} \equiv \frac{1 - |s_{22}|^2}{|s_{21}|^2}, \tag{7.1}$$

then, input noise temperature of the capacitor followed by the MMIC LNA is given simply by the Friis' formula for noise [88]

$$T_n = T_{cap} + L_{eff} T_{LNA} \tag{7.2}$$

where T_{LNA} is the noise temperature of the LNA, and the noise temperature of the capacitor T_{cap}—a lossy, passive two port—is obtained using Bosma's theorem [96]

$$T_{cap} = T_{phys} \frac{1 - |s_{22}|^2 - |s_{21}|^2}{|s_{21}|^2} = T_{phys} \left(L_{eff} - 1 \right). \tag{7.3}$$

Figure 7.23: Measurement setup for cryogenic capacitor tests

T_{phys} is the physical temperature of the capacitor, namely 300 or 22 K. Then, the effective noise contribution due to ohmic losses in the capacitor is defined as

$$\Delta T \equiv T_n - T_{LNA} = (T_{phys} + T_{LNA})\,(L_{eff} - 1)\,. \tag{7.4}$$

Here, s_{21} represents the de-embedded transmission coefficient while no de-embedding is performed on s_{22}.

Figure 7.24 presents the calculated noise contribution of the five capacitors. For these plots, T_{LNA} is assumed to be 55 and 5 Kelvin at room and cryogenic temperatures, respectively. The effect of the capacitor reactance is negligible above 1 GHz for values $>$ 10 pF. The ripples in response around 12 and 18 GHz are remnants of package effects after de-embedding. From the noise contribution perspective, the two Skyworks capacitors perform the best. However, their performance starts to degrade above 12 GHz with the 10 pF capacitor exhibiting slightly wider bandwidth. Presidio 4 pF capacitor achieves even wider bandwidth without any resonances; however, its noise contribution is significantly higher thereby limiting its use for extremely low-noise applications. Dielectric Labs 82 pF Milli-Cap is an SMT single-layer capacitor with the data sheet indicating resonance-free and low-loss operation up to 40 GHz. The measurements reveal significantly different performance; however, it is possible that there are artifacts due to mounting of the SMT capacitor in the coaxial package (e.g. capacitor is installed on 4-mil-wide microstrip trace) which could explain some of the unexpected performance degradation.

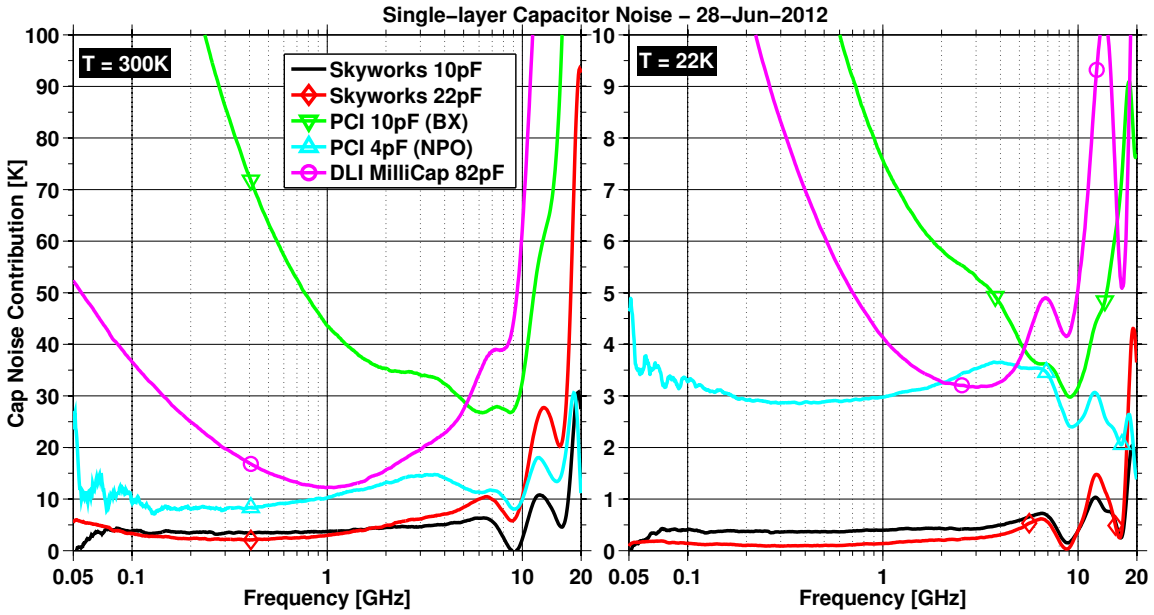


Figure 7.24: Effective noise contribution due to ohmic loss of five microwave capacitors at 300 and 22 K

7.8 Conclusions

In this chapter, the measurements of 1–20 and 8–50 GHz LNAs on Northrop Grumman Corporation's 35 nm InP and OMMIC's 70 nm GaAs processes have been discussed at length. The results have been extensively compared to simulated performance using discrete HEMT results of the previous chapter, and in general, the agreement was observed to be very good.

Of the LNAs presented, three stand out by improving the state of the art in noise and bandwidth of cryogenic LNAs:

1. the OMMIC 1–20 GHz LNA achieved $\leq$ 10 K from 0.7 to 16 GHz and $\sim$ 5 K over half of that band with approximately 15 mW DC power consumption. Furthermore, it performs very well under ultra-low-power operation with $\leq$ 10 K noise temperature from 2 to 14 GHz at 3 mW;

2. the low-frequency InP LNA measured $\leq$ 10 K from 2 to 17 GHz, but exhibited large gain slope due mostly to limited SSM availability and design error in drain resistor values;

3. the NGC 8–50 GHz LNA achieves $<$ 20 K noise from 6 to 40 GHz which is only slightly higher than state-of-the-art Ka-band amplifiers in the literature, but covers a much wider frequency band.

All LNAs exhibit poor input return loss which is addressed in the next design iteration in addition to correcting the large gain slopes observed on NGC LNAs.

The results of this chapter highlight the trade-off between low-frequency noise temperature and

bandwidth of ultra-wideband LNAs. In particular, improving the former requires large first-stage devices with R_{opt} values closer to 50 Ω in addition to significant inductive source degeneration. However, both degrade high-frequency noise and gain of the LNAs. On the other hand, small devices in the first stage not only move R_{opt} away from 50 Ω, but also makes the input impedance of the LNA very difficult to match. This further complicates the LNA design as the amount of matching one can do is very limited to begin with in ultra-wideband applications.