Chapter 6

Discrete HEMT Characterization

Knowledge of eight numbers, four complex and four real, are required to determine the microwave small-signal and noise performance of any two-port network at one frequency. The four complex numbers specify the current-voltage behavior of the two-port while the four real numbers are needed to completely characterize its noise performance. The determination of the former is predominantly accomplished by measuring the scattering parameters with the aid of a vector network analyzer (VNA). It is common to augment the scattering parameter measurements with DC measurements of transistor's $I - V$ characteristics.

Cryogenic measurement of a two-port's noise parameters, on the other hand, is much more difficult [70, 19]. Even at room temperature, they are measured with a dedicated test setup through lengthy tests. Therefore, the noise parameters are not explicitly measured in this work. Instead, they are inferred by using an extracted small-signal model and one 50 Ω noise measurement [71]. This approach requires a pre-determined model for the device under test. In the case of microwave transistors, Pospieszalski's FET noise model has been used widely and is employed herein [69].

6.1 Measurement Setup for DC and S-Parameters

The discrete devices investigated in this research were characterized with DC and S-parameter measurements in three stages:

1. On-chip measurements with wafer-probes at 300 K;
2. Measurements of the transistor in coaxial module at 300 K (see Figure 6.1);
3. Measurements of the transistor in coaxial module at 20 K.

While the first two data sets seem redundant, having them is very valuable in de-embedding the package effects at room temperature as well as ensuring there is no performance change when the calibration chips are diced to install the transistor in coax module. The DC measurements are

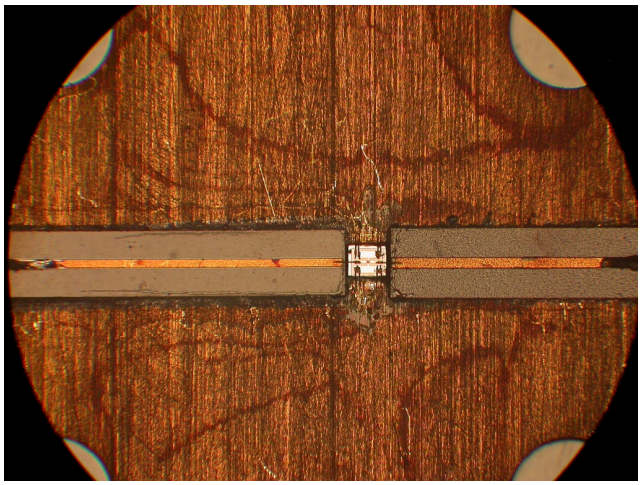

Figure 6.1: Photo of a discrete transistor in the coaxial module with K-connectors

performed with maximum 20 and 50 mV step sizes in gate and drain biases, respectively. The S-parameters are saved over a wide range of DC bias from 0.01 to 20 GHz.

Cryogenic measurements are performed with the transistor module installed in a cryostat with a copper strap to the cold head and connected to the VNA via two flexible coax cables which are not heat sunk to the cryostat cold head, as shown in top half of Figure 7.2(a) (in the red ellipse). The lack of cold straps on the flexible cables increases the physical temperature of the coaxial module; however, this increase is small and was observed to have no consequence on the measurements. Cryogenic S-parameters are de-embedded to the input of the transistor by using measurements of a short standard from the calibration chip in the same module as the transistor at 20 K.

6.2 DC Measurements

As mentioned earlier, transistors from the three processes (NGC 100%, NGC 75%, OMMIC) with varying gate widths were characterized extensively; however, only results from the largest and smallest devices are presented as they are sufficient to demonstrate the most important features. In the following, the large device means 2f200 μm for NGC and 2f150 μm for OMMIC, while the small device sizes are 2f50 μm for NGC and 2f40 μm for OMMIC.

Figure 6.2 plots drain current density as a function of drain and gate biases at room and cryogenic temperatures for the small transistor while those of the large devices are provided in Figure 6.3. Figures 6.4 and 6.5 present the extrinsic DC transconductance, namely

$$g_{m,DC} = \frac{dI_{DS}}{dV_{GS}} \tag{6.1}$$

of the small and large devices, respectively. The key observations from the room-temperature results

are:

1. All devices show well-behaved and smooth response in terms of $g_{m,DC}$ and drain-source resistance r_{ds};

2. The peak $g_{m,DC}$ measured on the small transistors are 2.5, 1.8 and 1.6 S/mm for the 100%, 75%, and OMMIC devices, respectively, which are considerably different than those in Table 5.1;

3. The transconductance per unit width shows size dependence on the NGC 100% transistors. For example, the 2f50 μm device achieves peak transconductance of 2.5 S/mm whereas the 2f200 μm transistor only attains ˜ 1.6 S/mm. Tests on multiple transistors of identical sizes indicate that this is not due to device variability. The NGC 75% devices also exhibit some size dependence, but the OMMIC transistors do not.

The measurements at 20 K reveal some interesting features, namely:

1. The NGC 100% devices exhibit kinks—sudden current increase with small increase in V_{DS}—yielding large changes in output conductance;

2. The DC transconductance of the same devices is greatly enhanced with $V_{DS} > 0.4$ V and $I_{DS} < 200$ mA/mm;

3. The small OMMIC and NGC 75% transistors show very slight g_m enhancements with $V_{DS} \geq 0.8$ V and I_{DS} around 200-300 mA/mm;

4. The smaller devices on all processes display these features more prominently;

5. The drain current of the 2f40 μm OMMIC transistor begins to level out under high drain bias. A similar but more severe behavior was also observed on a different OMMIC 2f150 μm device as well as a few 100% NGC transistors. The OMMIC transistor was tested with a light-emitting diode which showed that the impact of light stimulation is quite small.

In total, eight NGC 100%, three NGC 75%, and four OMMIC transistors were DC characterized cryogenically. All of the 100% devices showed similar kinks, with the ones presented herein being among the less severe of all measured. All three 75% transistors performed at least as good as the ones shown here. One of the OMMIC devices exhibited time-varying DC characteristics, another small device showed kinks on par with the 2f200 μm 100% NGC device of this section, and the remaining two performed well.

Another FET parameter of interest in applications requiring extremely low noise is gate leakage current. It constitutes a shot noise source, therefore must be minimized [72]. It cannot be controlled by the circuit designer, but rather is a process parameter that is fairly dependent on gate passivation.

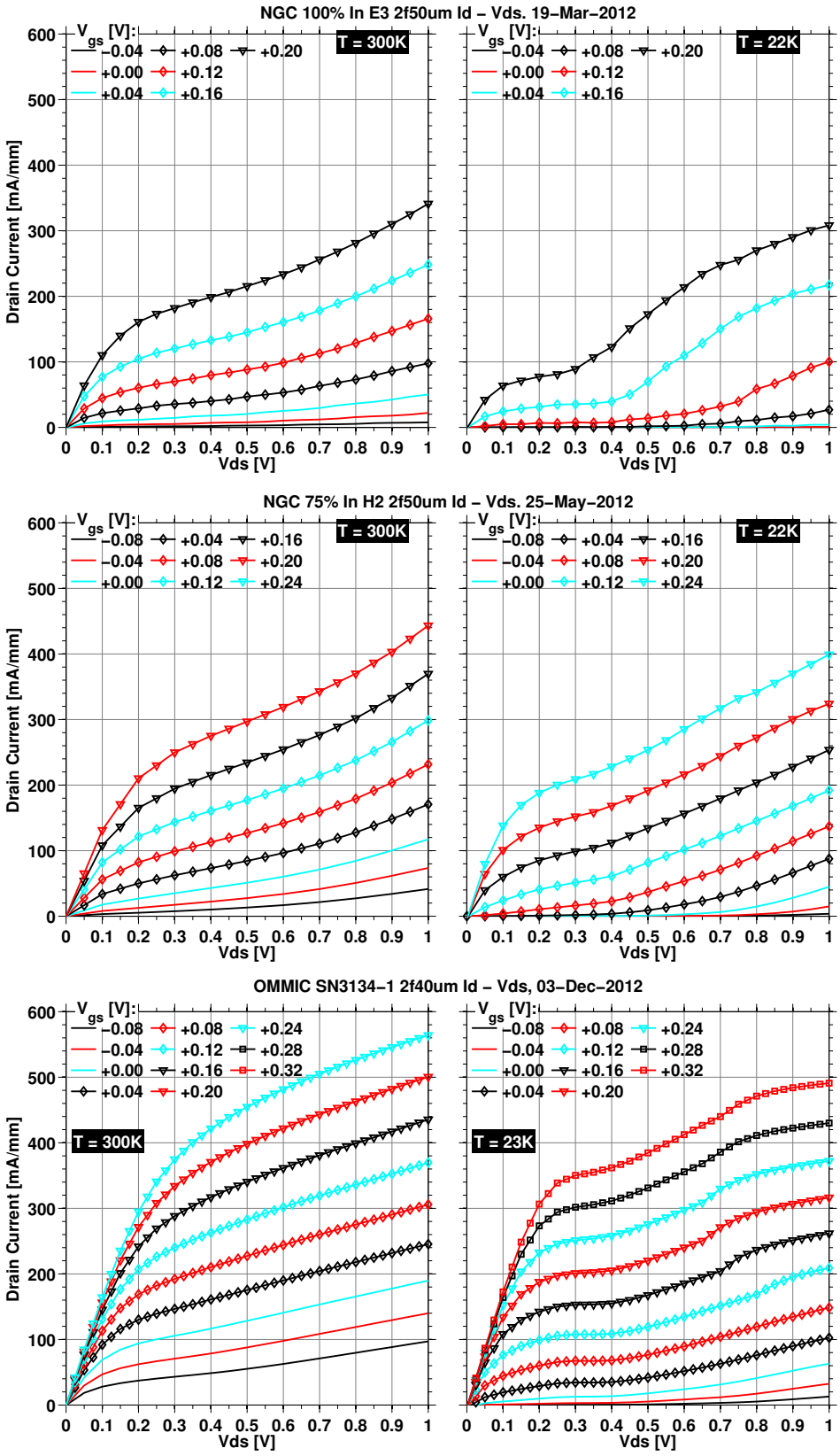

Figure 6.2: Measured $I_{DS} - V_{DS}$ of NGC 100% 2f50 μm (top), NGC 75% 2f50 μm (middle), and OMMIC 2f40 μm devices

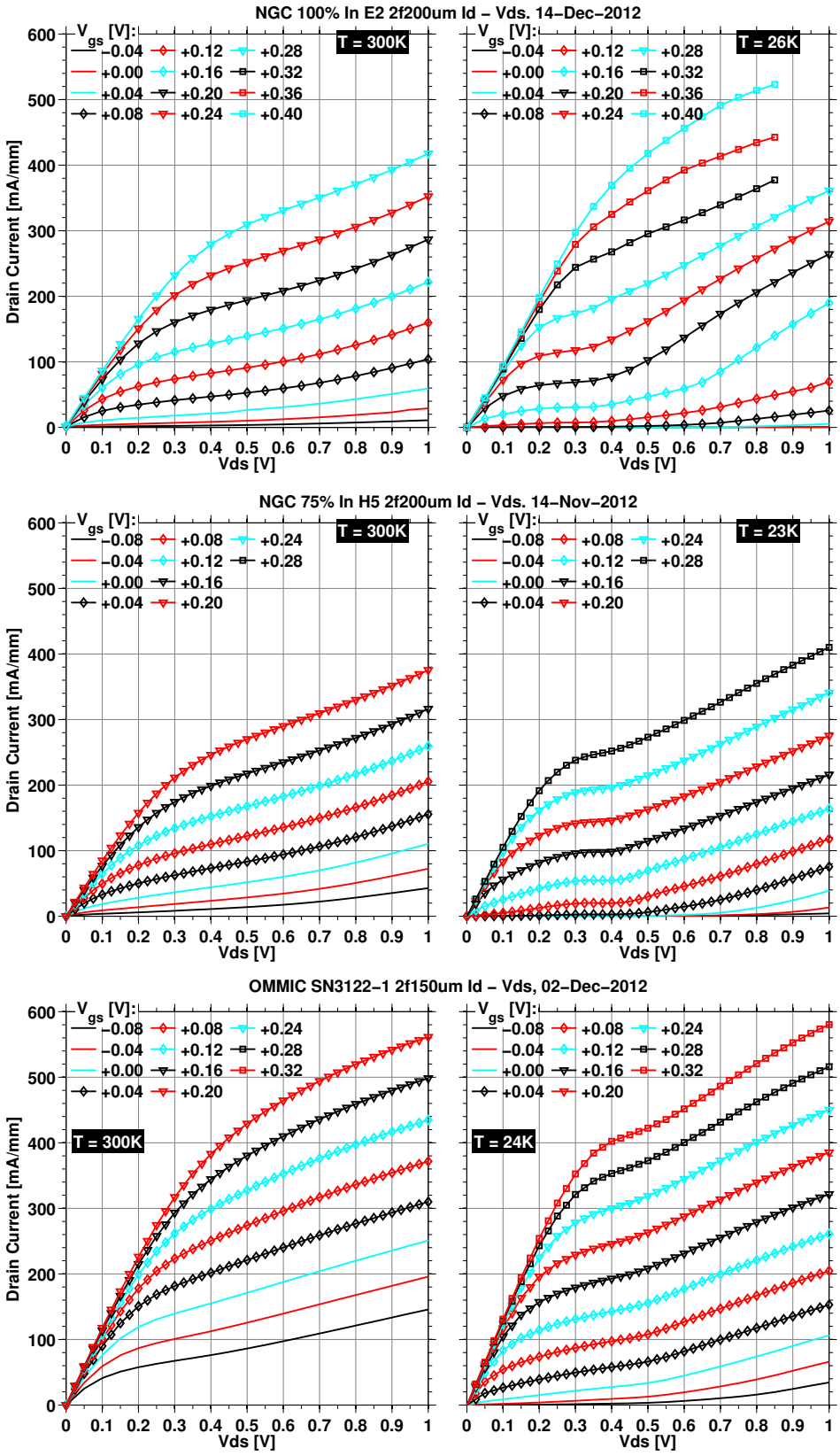

Figure 6.3: Measured $I_{DS} - V_{DS}$ of NGC 100% 2f200 μm (top), NGC 75% 2f200 μm (middle), and OMMIC 2f150 μm devices

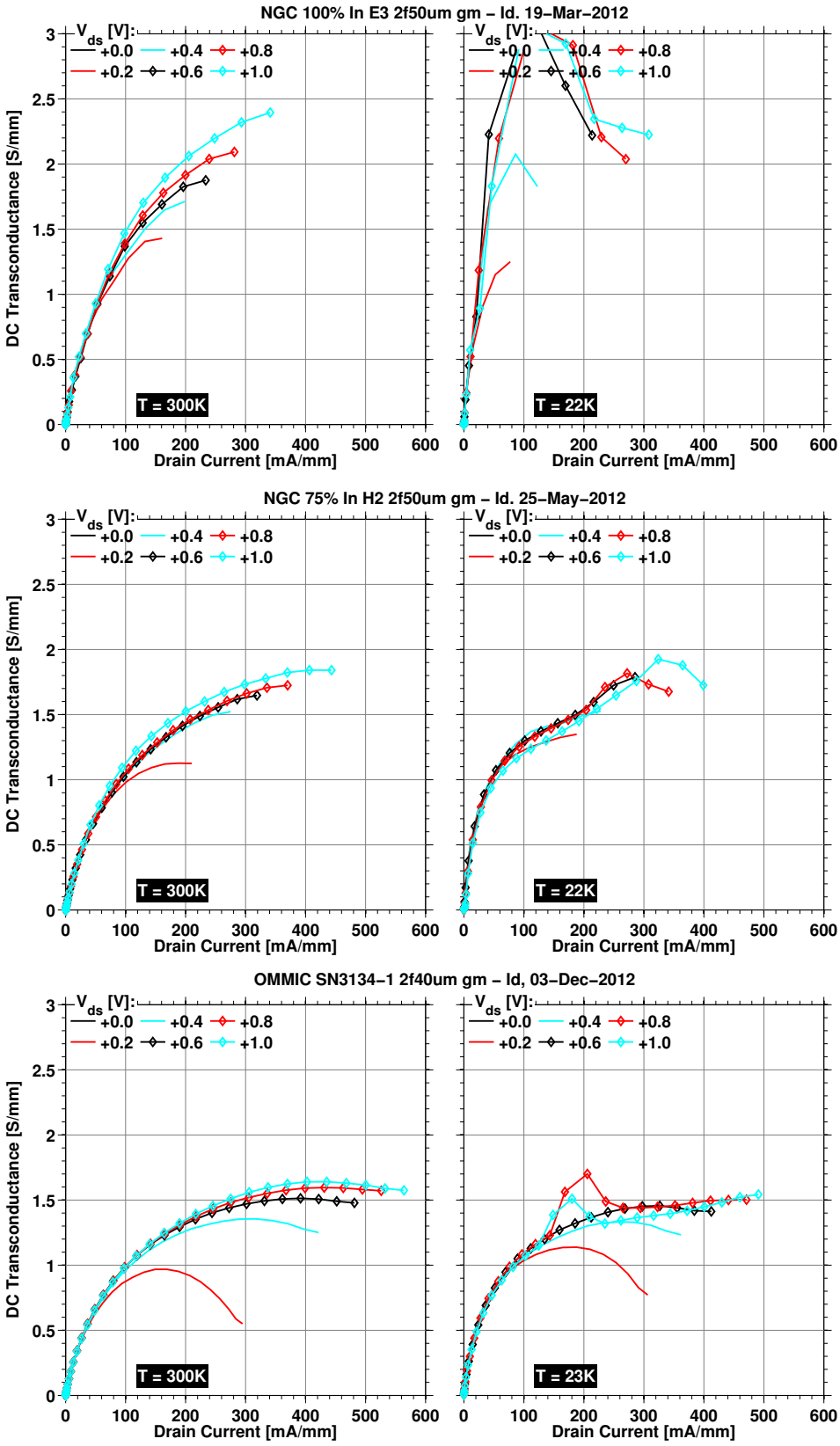

Figure 6.4: Measured extrinsic DC transconductance of NGC 100% 2f50 μm (top), NGC 75% 2f50 μm (middle), and OMMIC 2f40 μm devices

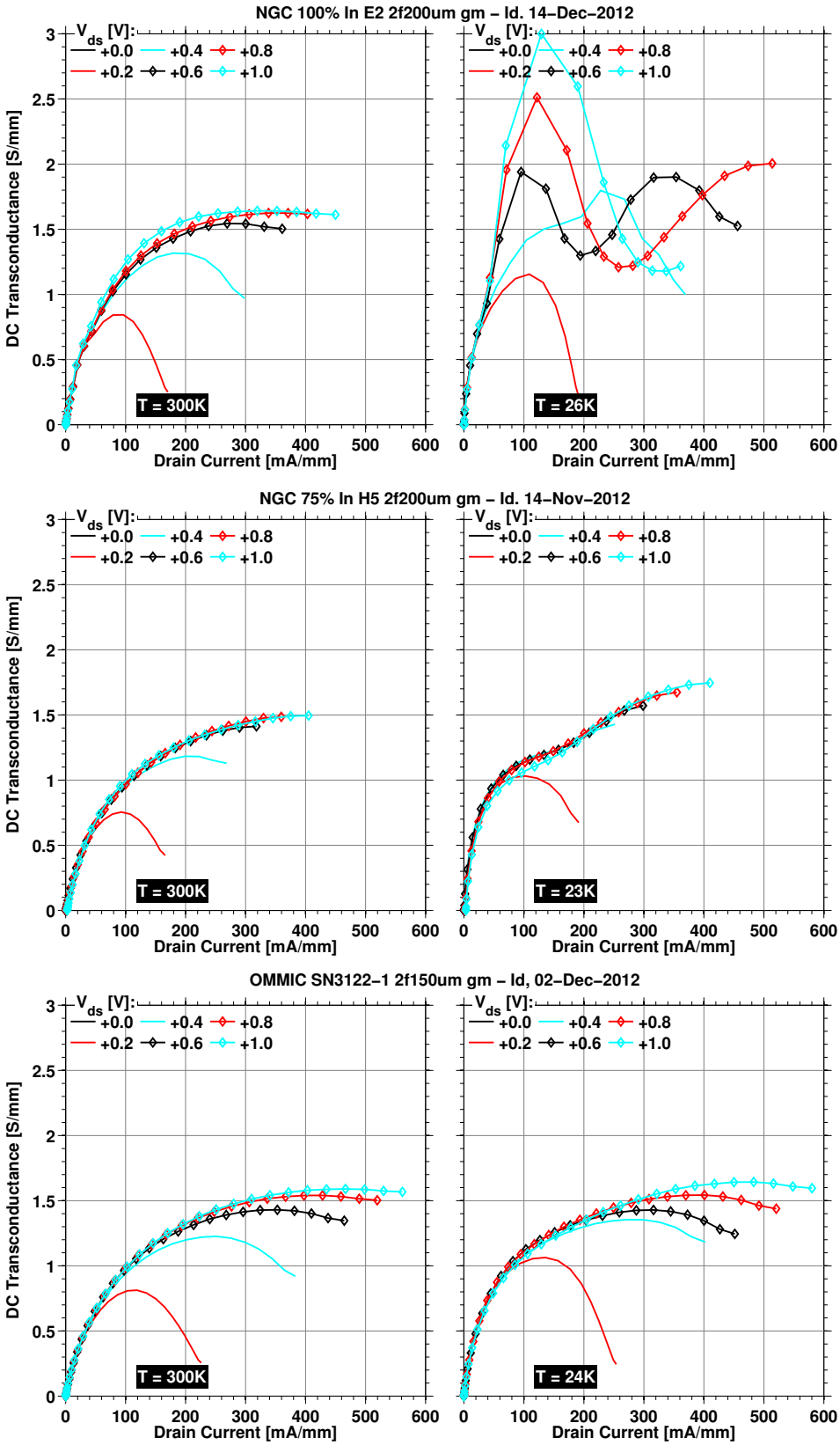

Figure 6.5: Measured extrinsic DC transconductance of NGC 100% 2f200 μm (top), NGC 75% 2f200 μm (middle), and OMMIC 2f150 μm devices

The gate leakage current of the transistors presented in this section have also been measured and the results appear in Figures 6.6 and 6.7.

All devices show significant gate leakage at room temperature. The measured leakage of the 100% devices is fairly typical among the eight we have tested; however, the small NGC 75% and OMMIC transistors shown here display above average gate leakage compared to others tested. This is attributed to chip-to-chip variability, which was observed to be significant for gate leakage. In all three processes, the large transistors are less leaky than small ones. As a reference, the increase in 50 Ω noise temperature due to 1 μA of gate leakage is approximately 0.39 K at 20 K physical temperature.

The gate leakage plots reveal another interesting feature: the bell-shaped response at high drain bias. It is visible on all devices to different extents at 300 K. It, along with total gate leakage, is much reduced cryogenically; however, it is still significant for the 100% transistor and is barely discernible on the other two. The bias range where this occurs correlates strongly with the bias range where the devices show $g_{m,DC}$ enhancement which suggests that these two symptoms are due to the same phenomenon.

Both kinks in the $I_{DS} - V_{DS}$ characteristics and bell-shaped gate leakage current have been empirically observed on HEMTs for almost three decades. The former is sometimes attributed to the so-called *kink effect* due to traps in the semiconductor [73, 74, 75], while the bell-shaped gate leakage is commonly interpreted as a symptom of *impact ionization.* Impact ionization, sometimes known as avalanche breakdown, occurs when energetic free electrons in the channel collide with semiconductor atoms in the lattice thereby generating new electron-hole pairs. The newly generated electrons are swept by the high electric field in the channel which causes *increased* I_{DS}. The corresponding holes are attracted by the relatively negative-biased gate-source region where some tunnel through the gate Schottky barrier resulting in *increased* I_{GS}. The remaining holes accumulate in the gate-source and buffer regions attracting more electrons. This positive feedback system then continues to build up. Impact ionization is exacerbated by the high indium content due to the lower energy barrier to generate new electron-hole pairs; thus, is especially more prominent on the NGC 100% transistors.

There is, however, a third interpretation that says that both phenomena are due to impact ionization [76, 77, 78, 79, 80, 81] which is the gist of the argument made herein. While the DC results of this section alone are not sufficient to demonstrate this point fully, the microwave measurements of the next section offer more clues to origins of these phenomena. In particular, Reuter and others [76, 77, 78] have shown that impact ionization also causes inductive drain impedance up to a few GHz in short-channel MOSFET, HFET, and HEMT transistors at room temperature. Such inductive output impedance is indeed observed on most of the transistors tested during this research as explained next.

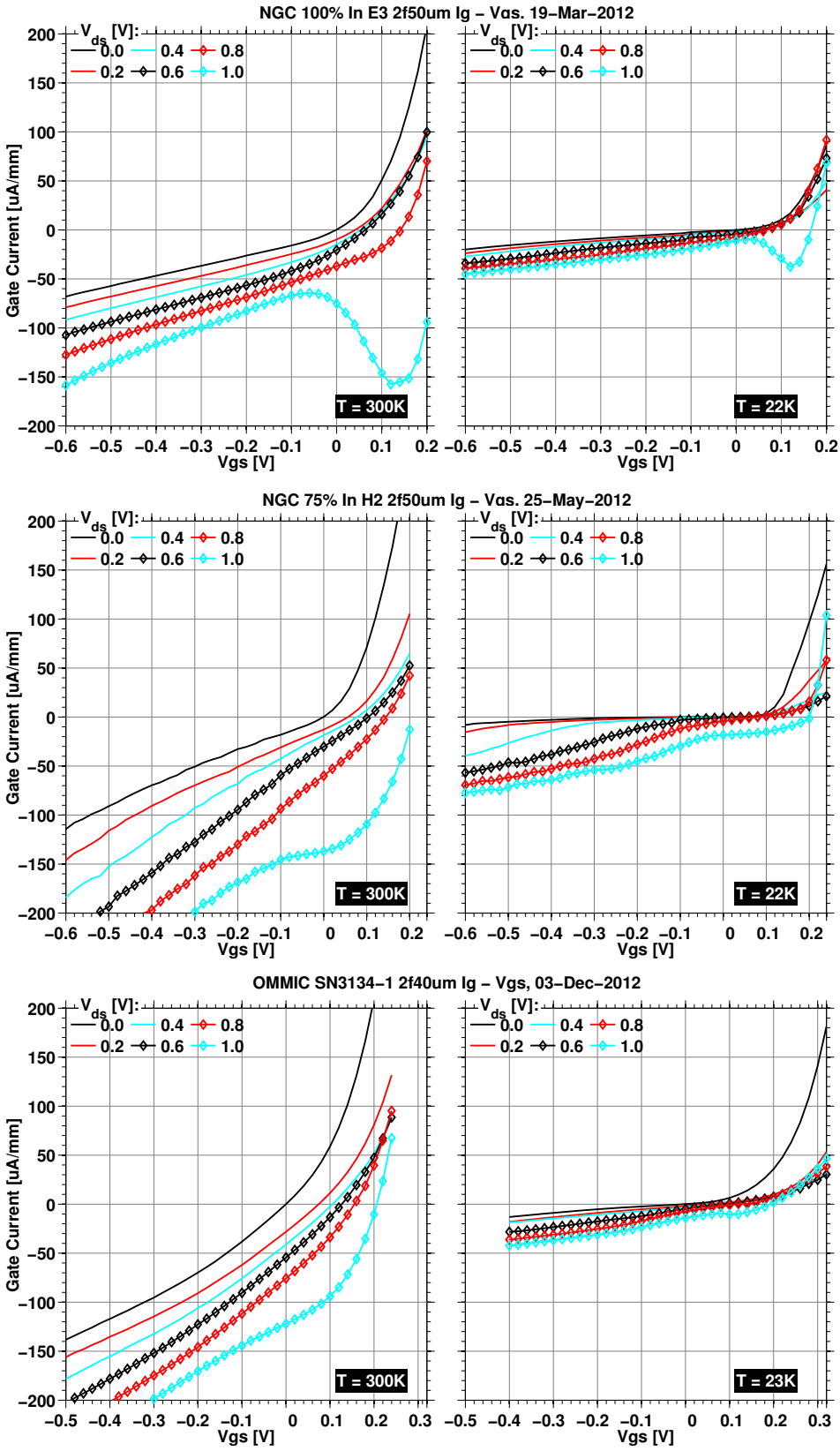

Figure 6.6: Measured $I_{GS} - V_{GS}$ of NGC 100% 2f50 μm (top), NGC 75% 2f50 μm (middle), and OMMIC 2f40 μm devices

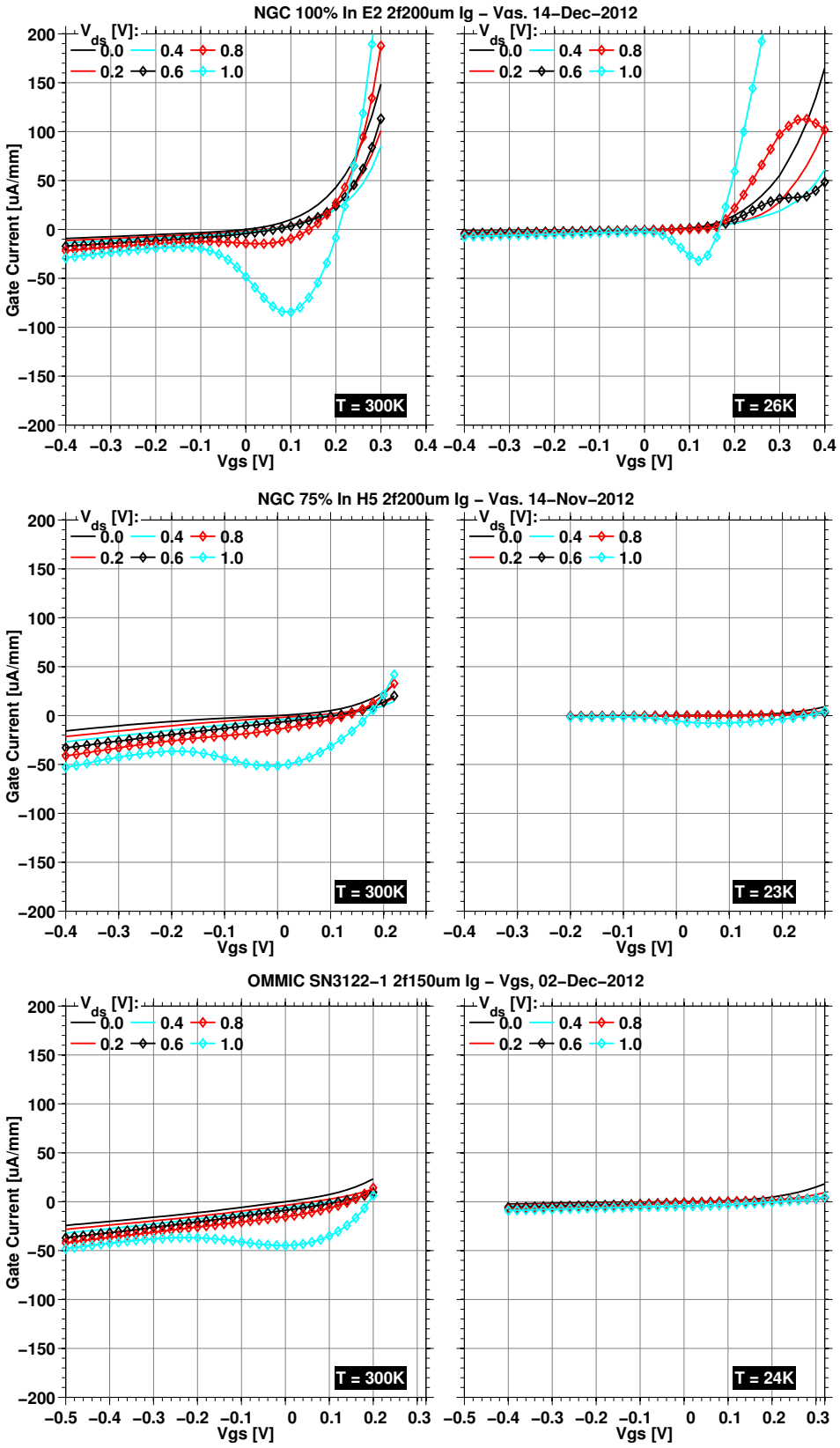

Figure 6.7: Measured $I_{GS} - V_{GS}$ of NGC 100% 2f200 μm (top), NGC 75% 2f200 μm (middle), and OMMIC 2f150 μm devices

6.3 S-Parameter Measurements

In addition to DC tests, almost all of the transistors were also characterized cryogenically by measuring their scattering parameters over wide range of DC bias. In this research, this extensive database of S-parameters is used for two purposes: 1) to evaluate effects of impact ionization on microwave performance; 2) to perform small-signal model extraction for use in transistor noise modeling as detailed in the next section. The first half of this section discusses the former.

6.3.1 Inductive drain impedance

Figure 6.8 illustrates measured, de-embedded scattering parameters of the NGC 100% 2f50 and 2f200 μm transistors up to 10 GHz at 300 and 20 K. In particular, the plots include output reflection coefficient and gain of each device under two different current bias with $V_{DS} = 0.8$ V.

It is seen that both transistors do in fact exhibit inductive output impedance at either temperature. This inductive loop, as it is seen on the Smith chart, is smaller at 300 K under low current bias, and expands considerably when the transistor is cooled or bias is increased. At 20 Kelvin physical temperature and under high bias where impact ionization is more prominent, the loop expands to the extent that negative output resistance is observed on the small transistor. Additionally, further increasing drain bias current shrinks the inductive loop which is consistent with decrease in impact ionization as gate bias is increased causing smaller gate-drain voltage drop.

All of the 100% NGC transistors measured cryogenically showed inductive output impedance in addition to the $I - V$ kinks and bell-shaped gate leakage. Moreover, the inductive loop expands outside the Smith chart at cryogenic temperature over a range of bias settings on all size transistors except the 2f200 μm presented in Figure 6.8(b). In comparison, the 75% NGC and the OMMIC transistors also displayed inductive output impedance; however, the loop was seen to span significantly smaller frequency range and exhibited much less expansion under cooling.

6.3.2 Small-Signal model extraction

Calculation of element values in HEMT small-signal models has been investigated extensively in the literature [82, 83, 84, 85, 86, 87]. The approach usually involves comparison of measurements to a small-signal model based on device physics which can take on slightly different forms depending on the application. The model used in this work appears in Figure 6.9 and is one of the most widely used for HEMTs in microwave and millimeter-wave frequencies [69]. In Figure 6.9, the components of the intrinsic FET are the bias-dependent small-signal parameters while the parasitic components (with capital subscripts) are assumed constant versus bias.

Even with an extensive collection of measurements, the problem of finding the element values usually entails solution of an overdetermined set of equations because of the large number of un-

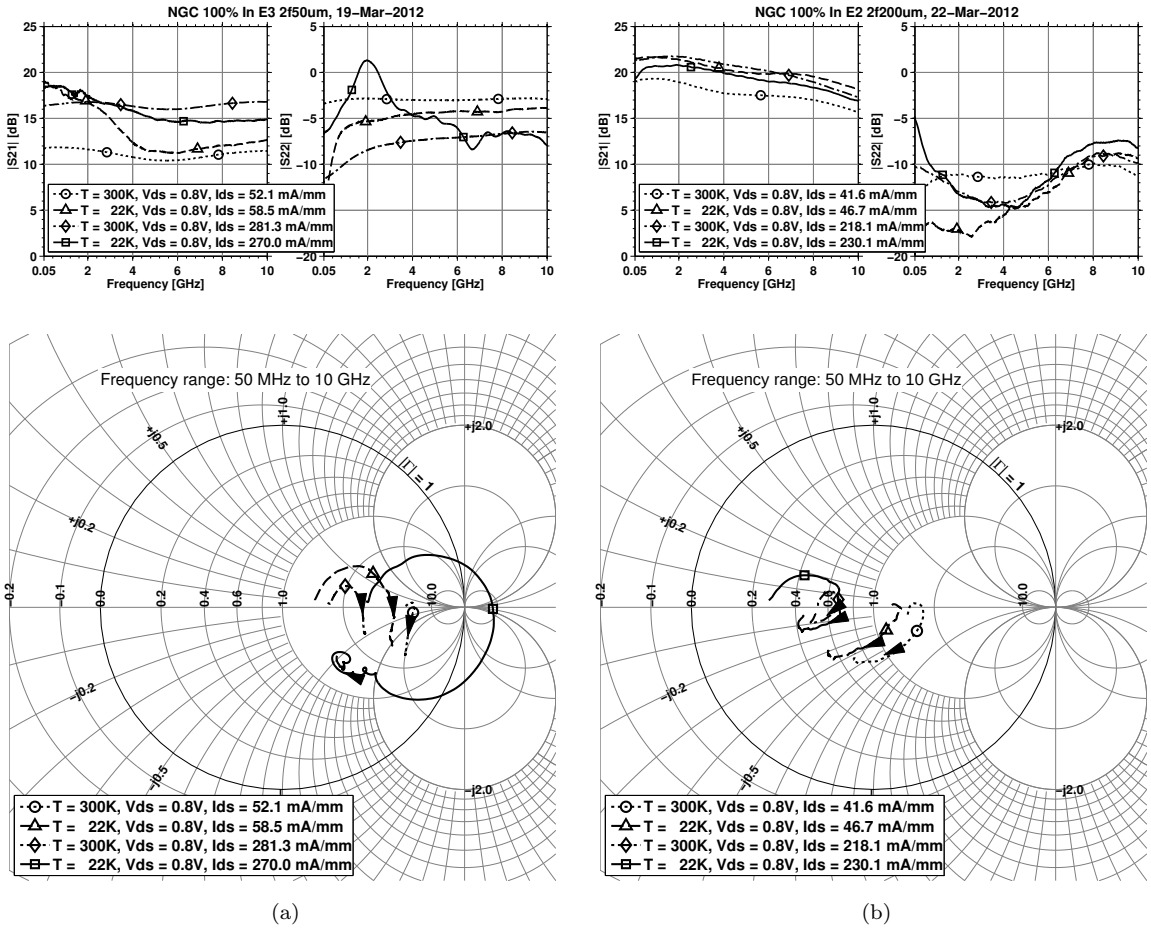

Figure 6.8: Measured, cryogenic S_{22} and S_{21} of the 2f50 and 2f200 μm NGC 100% transistors. The measurements are de-embedded to the edge of the devices which are the same devices as those presented in Section 6.2.

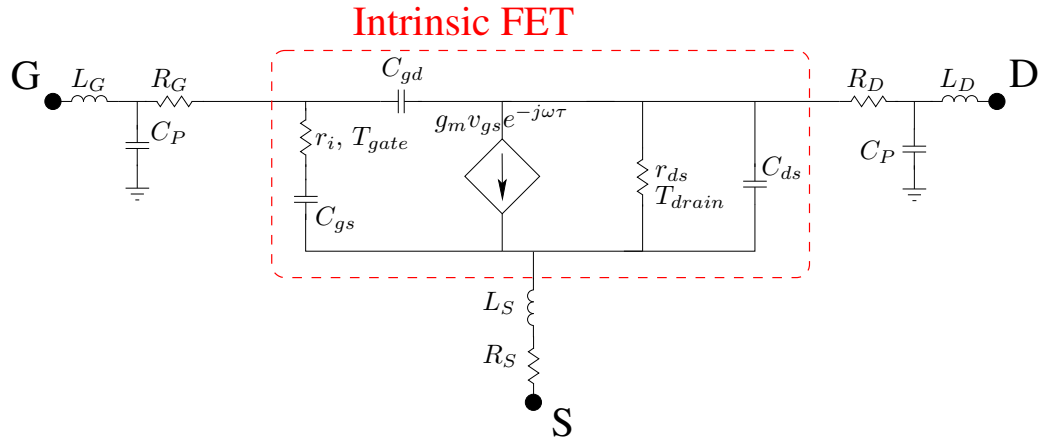

Figure 6.9: The HEMT small-signal model used in this work

knowns. Thus, the obtained values are not unique and some frequently turn out to be physically impossible (e.g., negative or extremely large/small values). Moreover, the element calculation has to be repeated for each bias point of interest. This is a formidable task and is not pursued in this research. Instead, a hybrid approach is taken that can be summarized as:

1. Determine the parasitic element values from foundry specifications and cold-FET measurements,
2. Estimate r_{ds} and g_m from measured, de-embedded low-frequency S-parameters,
3. Tweak the foundry-specified capacitor and r_i values to fit model to measurements at two or three bias points, and
4. Assume a certain bias dependence for the capacitors and r_i such that the values agree with those obtained in step 3,

where the first two steps follow the "hot-FET/cold-FET" method outlined in [85]. While this approach may not be the most robust or accurate for calculating the element values, it should be sufficiently accurate for the goals in this research: 1) evaluating microwave effects of impact ionization; 2) low-frequency noise modeling.

6.3.2.1 Parasitic resistances

The first step in the SSM extraction is determination of parasitic element values. This is accomplished via wafer-probed DC and S-parameter measurements with the gate of the transistor forward biased using a current source. The vector network analyzer is calibrated to the tip of the wafer-probes using CS-5 calibration substrate[1]. Then, the VNA ports are extended to the edge of the transistor using the short- and open-calibration standards included on the calibration chip from each process. This step is critical as lack of or incorrect port extension would yield under- or over-estimation of extrinsic elements in the FET small-signal model.

A small and a large device from each process were tested as the gate current was varied from 1 μA to 20 mA. The resulting gate voltages were recorded as well as the S-parameters for gate currents above 1 mA. Using the simplified small-signal model of the HEMT under forward-bias [85], values of the parasitic resistors and inductors can be obtained from the following equations:

$$\begin{aligned} Z_{11} &= R_G + R_S + \frac{R_{ch}}{3} + R_{dy} + j\omega\left(L_G + L_S\right) \\ Z_{12} &= R_S + \frac{R_{ch}}{2} + j\omega L_S \\ Z_{22} &= R_D + R_S + R_{ch} + j\omega\left(L_D + L_S\right) \end{aligned} \tag{6.2}$$

[1] GGB Industries, Florida, USA

where Z_{ij} are the impedance parameters [88]; R_{ch} is the channel resistance; R_{dy} is the dynamic resistance of the gate diode. An implicit assumption in these equations is that the measurements are performed at sufficiently low frequency such that the pad capacitance C_P can be ignored. The channel resistance is assumed to be zero which is reasonable for short gate-length devices such as the ones investigated in this work. The dynamic resistance of the diode is given by

$$R_{dy} = n\frac{kT}{qI_G} \tag{6.3}$$

where n is the diode ideality factor; k is the Boltzmann's constant; T is the ambient temperature; q is the electronic charge and I_G is the forward-bias gate current [85]. R_{dy} is either calculated using this equation if the diode ideality factor is known, or not calculated at all, because extrapolating $\Re\{Z_{11}\}$ versus $1/I_G$ to $1/I_G \to 0$ yields

$$\lim_{I_G \to \infty} \Re\{Z_{11}\} = R_G + R_S. \tag{6.4}$$

Since R_S is given by $\Re\{Z_{12}\}$, R_G and R_D are easily determined.

The second way of estimating $R_G + R_S$ is by using the DC current-voltage relationships. In particular, total resistance obtained by using Ohm's law is given as

$$\frac{V_{GS,i} - V_{GS,i-1}}{I_{G,i} - I_{G,i-1}} = R_G + R_S + \underbrace{\frac{nkT}{q}\frac{2}{(I_{G,i} + I_{G,i-1})}}_{R_{dy}} + R_{cable} \tag{6.5}$$

where $V_{GS,i}$ and $I_{G,i}$ are the ith recorded gate voltage and current, respectively, and R_{cable} is the total DC resistance in the test setup cables (easily measured by replacing device under test with a short). This method requires knowledge of the diode ideality factor. For OMMIC devices, $n = 1.67$, obtained from OMMIC's large-signal model, is used. For the NGC devices, $n = 1.5$ is assumed. R_S is obtained from the cold-FET method. The results from both techniques appear in Table 6.1 normalized to total gate periphery W_{tot}, i.e.,

$$\begin{aligned} R_G &= R_{G0}\frac{W_{tot}}{N_f^2} \\ R_S &= R_{S0}\frac{1}{W_{tot}} \\ R_D &= R_{D0}\frac{1}{W_{tot}} \end{aligned} \tag{6.6}$$

It is seen that determination of R_{G0} using the small devices is problematic which is most likely due to difficulty in obtaining a reliable gate finger resistance measurement on short finger widths. In addition, normalization in (6.6) amplifies any errors in measurement. In general, the values obtained

	Method	OMMIC		NGC 100%		NGC 75%	
		2f40	2f150	2f50	2f200	2f50	2f200
R_{G0} $[\frac{\Omega\text{-finger}^2}{\text{mm}}]$	Cold-FET	454	121	454	164	477	153
	DC	112	96	262	146	205	148
	Foundry	200/3		400/3		400/3	
	Final	80		140		140	
R_{S0} [Ω-mm]	Cold-FET	0.23	0.19	0.25	0.21	0.19	0.17
	Foundry	0.2		0.12		0.12	
	Final	0.2		0.19		0.19	
R_{D0} [Ω-mm]	Cold-FET	0.26	0.3	0.21	0.42	0.24	0.36
	Foundry	0.29		0.015		0.015	
	Final	0.29		0.3		0.3	

Table 6.1: Values of extrinsic resistors for OMMIC and NGC devices

from these analyses are fairly close to foundry-specified values also listed in the same table and the final values used in the rest of the thesis are chosen to be roughly the average of measurements and foundry specifications (ignoring the outlier measurements from small devices). The parasitic inductor values are obtained from the foundry small-signal models

$$L_{G0}\,[\text{pH-finger/mm}] = \begin{cases} 338 & \text{OMMIC} \\ 233 & \text{NGC} \end{cases}$$

$$L_{S0}\,[\text{pH/finger}] = \begin{cases} 1.6 & \text{OMMIC} \\ 1 & \text{NGC} \end{cases}$$

$$L_{D0}\,[\text{pH-finger/mm}] = \begin{cases} 398 & \text{OMMIC} \\ 87 & \text{NGC} \end{cases}$$

which are scaled as

$$L_G = L_{G0}\frac{W_{tot}}{N_f}$$

$$L_S = L_{S0}N_f$$

$$L_D = L_{D0}\frac{W_{tot}}{N_f}$$

assuming $N_f \geq 2$. Because the extracted small-signal models are primarily used for low frequencies—i.e., around 1 GHz—,these values are deemed to be sufficiently accurate.

6.3.2.2 Simplified hot-FET method: r_{ds} and g_m

Once device parasitics are known, microwave parameters of the intrinsic FET are easily obtained by transforming the de-embedded S-parameters to Z-parameters, subtracting the signature of the parasitics

$$\mathbf{Z}^{int} = \begin{bmatrix} Z_{11} - R_S - R_G - j\omega\left(L_G + L_S\right) & Z_{12} - R_S - j\omega L_S \\ Z_{21} - R_S - j\omega L_S & Z_{22} - R_S - R_D - j\omega\left(L_D + L_S\right) \end{bmatrix}, \tag{6.7}$$

and inverting $\mathbf{Z}^{int}$ to obtain the Y-parameters as the π-topology of the small-signal model naturally lends itself to admittance representation. Then, the drain-source resistance r_{ds} is given by

$$r_{ds} = \frac{1}{\Re\left\{Y_{22}\right\}} \tag{6.8}$$

and the intrinsic transconductance by

$$g_m = \sqrt{\Re\left\{Y_{21}\right\}^2 + \left(\Im\left\{Y_{21}\right\} + \omega C_{gd}\right)^2 \left[1 + \left(\omega C_{gs} r_i\right)^2\right]} \tag{6.9}$$

Explicit expressions for r_i, C_{gs}, and C_{gd} can be obtained using the results in [85] to extract values for g_m; however, this is not pursued because extraction of r_i, C_{gs}, and C_{gd} is tricky even with closed-form equations. It tends to be sensitive to noise in measurements and can yield unrealistic values.

Therefore, a different approach is followed here. Noting that the transistor is in source-degenerated common-source configuration, the closed-form expression for the intrinsic RF transconductance is found to be

$$g_m\left(S_{21}\right) = \frac{-A_v\left(R_{load} + r_{ds} + R_S\right)}{A_v r_{ds} R_S - R_{load} r_{ds}} \quad \text{with} \quad A_v \equiv \frac{10^{S_{21}/20}}{2} \tag{6.10}$$

where $R_{load} = 50\,\Omega$ and S_{21} is the measured, de-embedded gain (note that this is not the intrinsic S_{21}).

These steps are carried out in MATLAB using some specially written scripts as well as some publicly available functions for matrix manipulations[2]. The cryogenic results are presented in Figure 6.10 overlaid with those obtained from DC measurements. The drain-source conductance $g_{ds} = \frac{1}{r_{ds}}$ is plotted instead of r_{ds} as the former is more commonly used in device physics literature. It is obtained using the simplified hot-FET method and the scattering parameters between 1 and 2.5 GHz. The plots reveal couple of important observations:

NGC 100%: There is significant difference between r_{ds} and g_m obtained with the two methods. This device, as shown above, exhibits the most severe signs of impact ionization among the

[2] `http://www.mathworks.com/matlabcentral/fileexchange/6080-s-parameter-toolbox-+-z-y-h-g-abcd-t`

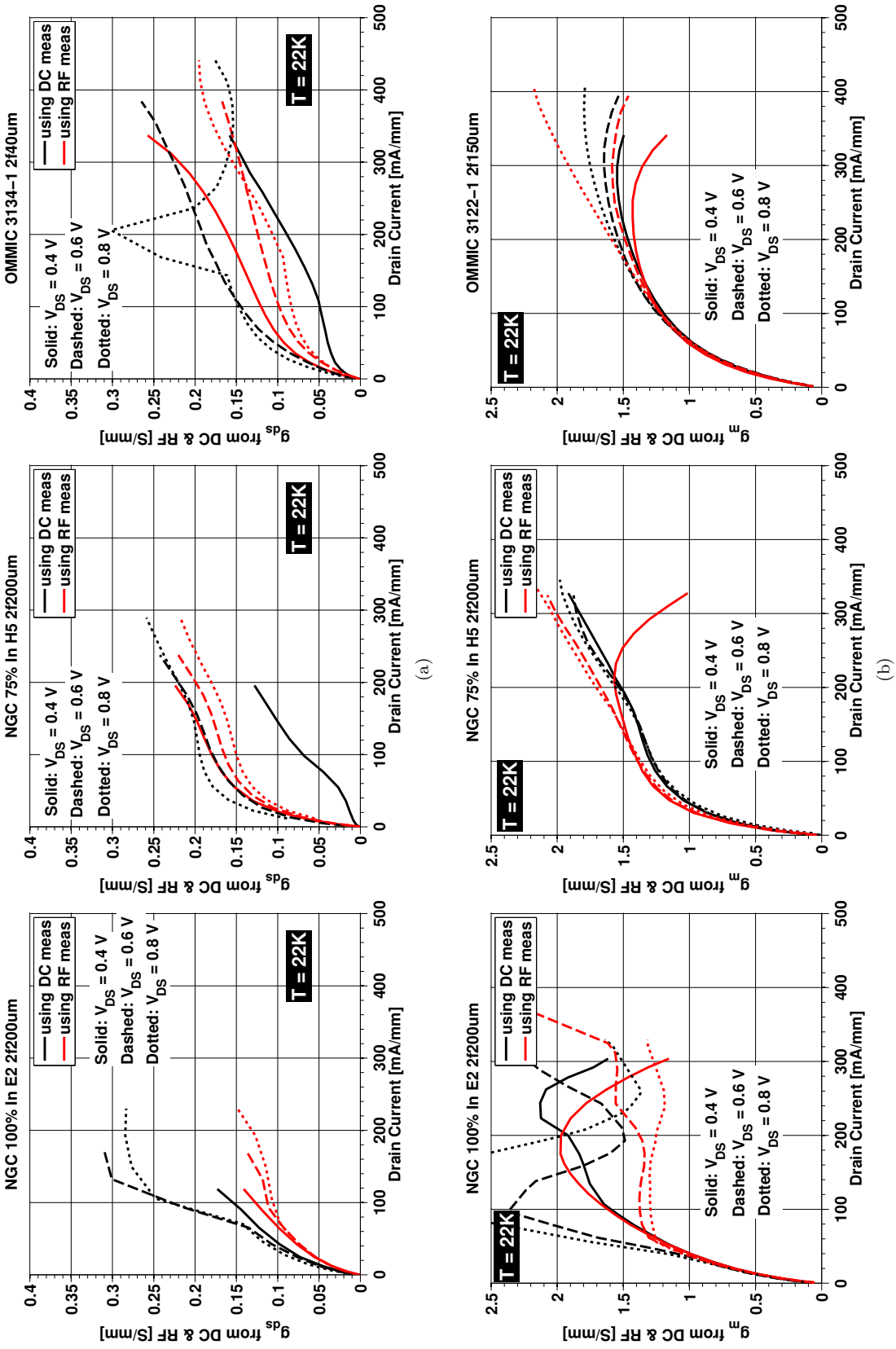

Figure 6.10: Comparison of DC and RF (a) g_{ds} and (b) g_m (intrinsic) of the NGC 100%, NGC 75% and OMMIC transistors

large transistors tested. While the RF g_m is much smoother than $g_{m,DC}$, it still shows large fluctuations, especially at $V_{DS} = 0.6$ V, and the transconductance at $V_{DS} = 0.8$ V seems to reach a plateau at very low current density. The difference in the drain-source conductance is very large except at low drain bias. That the DC and RF g_{ds} are so different is expected when traps are considered, which because of their time constant cannot respond to high-frequency signals [81]. However, these curves also suggest that traps alone are not sufficient to explain all features of the measurements.

NGC 75%: With the exception of g_{ds} at $V_{DS} = 0.4$ V, the difference between the two data sets is much smaller and g_{ds} show smoother response. The RF g_m is slightly higher, but its shape closely follows the DC curves except at $V_{DS} = 0.4$ V and $I_{DS} > 200$ mA/mm where it begins to roll off.

OMMIC: First, it should be noted that the RF g_{ds} results are measured on the small OMMIC device, because that is the only size cryogenically tested for S-parameters. Consequently, the plotted DC g_{ds} curves are also from the same transistor. The jump in g_{ds} at 200 mA/mm correlates with the $g_{m,DC}$ enhancement seen in Figure 6.4. Also, a slope change is observed on the RF g_{ds} near the same bias. There is considerable difference between RF and DC g_{ds}; however, shape of the curves at a given drain bias look fairly similar. The transconductance curves of the large OMMIC transistor look very similar for both methods.

6.3.2.3 Remaining elements of the small-signal model: Capacitors and r_i

In order to complete the small-signal model extraction, the values for the capacitors C_{gs}, C_{gd}, C_{ds} and the gate-source resistance r_i need to be computed. As alluded to earlier, the OMMIC small-signal model includes values for all of these components as a function of bias at 300 K. Therefore, for the three capacitors in the OMMIC transistor model, the values are taken directly from the foundry-specified SSM. As a check, these numbers have been verified with measurements at room temperature at a couple of bias points.

On the other hand, the NGC SSM was only provided at $V_{DS} = 1$ V and $I_{DS} = 300$ mA/mm for a 2f30 μm 100% device. Therefore, values for the three capacitors have been estimated by manually fitting measured, de-embedded S-parameters to modeled results at a handful of bias points. The bias dependence of capacitors is then assumed to be identical to that of OMMIC transistors. Because of the observed size dependence of the device parameters even after normalizing to total gate periphery, this process is carried out once for the 2f200 μm transistor and once for the 2f50 μm device.

This leaves r_i as the only unknown to determine. It is sometimes called the gate-charging resistor and is very difficult to measure accurately as it is a very small resistance in series with two resistors of approximately comparable magnitude and a very large reactance. As such, it is usually either

assumed constant or obtained from model fitting to S-parameter data. The latter approach is not straightforward because the values obtained for r_i tend not to be unique and the process has to be repeated for each bias point of interest. In order to alleviate these issues, the following approach is taken to estimate r_i at room temperature:

1. Obtain an estimate by comparing wafer-probed, de-embedded S-parameter measurements to simulations at two or three bias points,

2. Restrict the range of values r_i can take by using low-frequency 50 Ω input noise temperature $T_{50,\,1\mathrm{GHz}}$ measurements (see next section) using measured values of r_{ds}, g_m , R_G, R_S and assuming r_i is an ohmic-type resistor at ambient temperature [69],

3. Further restrict possible values of r_i by restricting the temperature of r_{ds}, T_{drain}, to a reasonable, expected range, e.g., 2000–3000 K at room temperature.

While this method does not necessarily guarantee uniqueness, the resulting values should be reasonably accurate. The bias dependence of r_i is then assumed to be similar to that provided in the OMMIC small-signal model, i.e.,

$$r_i\left(I_{DS}\right) = \alpha \tanh\left(\frac{1}{100} I_{DS}\right) + 0.1 \tag{6.11}$$

where α is 0.1 for OMMIC and 0.05 for NGC and are picked by fitting predicted values to the values obtained in step 1. Units of I_{DS} and r_i are mA/mm and Ω-mm, respectively. This assumed functional form is quite similar to expected bias dependence of C_{gs} [65].

The temperature dependence of the small-signal model elements is another source of complication. For r_{ds} and g_m, the measured values are used. The capacitor values are assumed to decrease 10% from 300 to 20 Kelvin, which is somewhat conservative as others have estimated 15-20% decrease [89]. r_i is assumed unchanged. The parasitic resistor values are halved cryogenically. The values for all the small-signal model elements are provided in the next section as a function of bias and temperature.

6.4 T_{drain} Measurements

Another consequence of impact ionization has been reported to be significantly increased minimum noise figure at low frequencies [76]. In order to characterize noise performance of the NGC and OMMIC transistors and evaluate effects of impact ionization, 50 Ω input noise temperature $T_{50,\,1\mathrm{GHz}}$ was measured at room and cryogenic temperatures from which T_{drain} of the Pospieszalski model was extracted for the large devices from all processes.

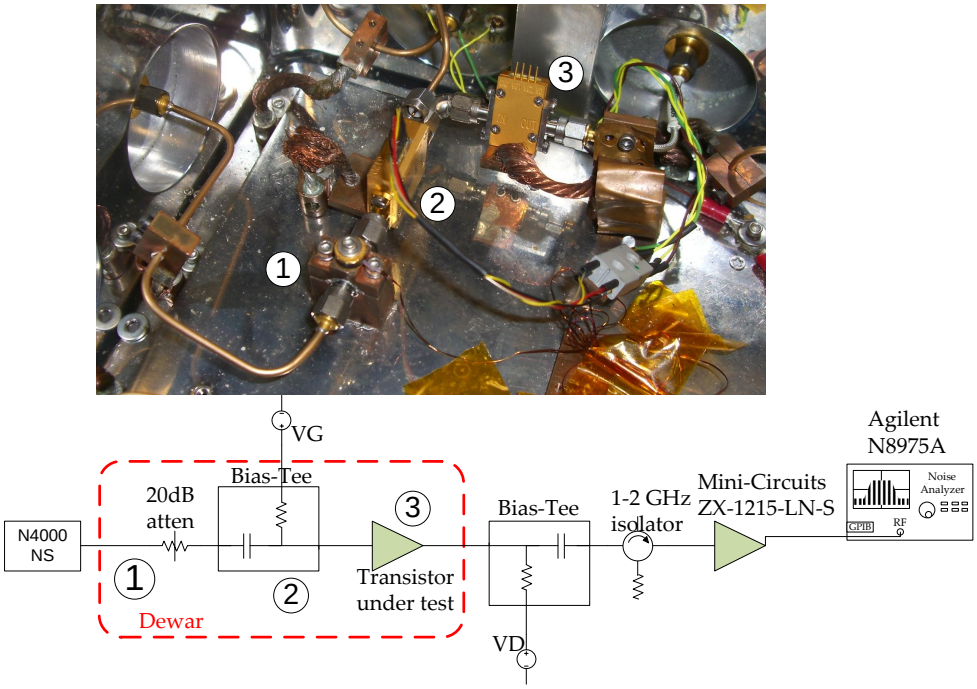

Figure 6.11: T_{drain} measurement setup block diagram.

6.4.1 Measurement setup

The single 50 Ω noise measurement required to model a two-port's noise performance could be performed cryogenically in a number of ways [90]; however, the most common approach is the cold attenuator method because of its good accuracy and relative insensitivity to uncertainty in excess noise ratio [90, 19]. This approach is used for the T_{drain} measurements.

The block diagram of the test setup used in T_{drain} measurements is displayed in Figure 6.11. The cold 20 dB attenuator is followed by a custom-built resistive bias-tee (R =50 kΩ and C =22 pF) to provide gate bias for the device under test. The bias-tee loss was measured cryogenically and taken into account in the noise measurements. The drain bias is provided through a Mini-Circuits ZX85-12G+ wideband bias-tee outside the dewar. The isolator following the bias-tee facilitates calculation of the second-stage noise contribution as a function of transistor output reflection coefficient [91, 92]. Specifically, let T_{50} and s_{21} represent the measured 50 Ω noise temperature—corrected by the noise figure analyzer (NFA)—and voltage gain of the transistor in linear units. Using the expression for output resistance of the transistor in source-degenerated common-source configuration, i.e.,

$$r_{out} = r_{ds}\,(1 + g_m R_S) + R_S, \tag{6.12}$$

the drain reflection coefficient is obtained

$$\Gamma_{out} = \frac{r_{out} - 50}{r_{out} + 50}. \tag{6.13}$$

The noise contribution of the back-end as a function of output reflection coefficient is found to be

$$T_{backend,corr} = \left(T_{backend} + 300\,|\Gamma_{out}|^2\right) \frac{1}{1 - |\Gamma_{out}|^2}. \tag{6.14}$$

where $T_{backend}$ is the noise temperature of the second stage with 50 Ω generator impedance and is measured separately. Then, the 50Ω noise temperature measurement corrected for drain reflection coefficient is

$$T_{50,\,1\mathrm{GHz}} = T_{50} - 300\frac{|\Gamma_{out}|^2}{|s_{21}|^2}. \tag{6.15}$$

The second-stage amplifier (with respectably low input noise temperature) is included to increase measurement SNR as the gain of a discrete device could be quite low depending on bias.

In the cold attenuator method, precise knowledge of the temperature of the cold attenuator's center conductor T_{atten} is necessary to achieve accurate results as any uncertainty in T_{atten} translates directly into uncertainty in measured noise temperature. The attenuator's physical temperature is measured with a thermo-couple mounted above it. However, because the attenuator is heat sunk from the outside, there is usually a temperature offset between the thermo-couple reading and the temperature of the attenuator's center conductor. This offset is determined through noise measurements of a reference amplifier calibrated at a laboratory such as NIST.

Despite being heat sunk to the cold head, the bias-tee increases the thermal resistance at the center conductor of the attenuator, thereby increasing the offset temperature by ˜1 Kelvin. As a matter of fact, an earlier version of this test setup employed the Mini-Circuits ZX85-12G+ bias-tee in the dewar as well. However, the thermal resistance of the bias-tee was so large that the attenuator offset temperature increased by more than 10 K as measured using a reference amplifier. On the other hand, the custom bias-tee has two disadvantages: 1) it has higher lowest frequency operation, e.g., 500 MHz; 2) on devices with significant gate leakage, there is significant voltage drop across the resistor in the bias-tee.

6.4.2 Theory

The T_{50} measurements are carried out at 1 GHz which is high enough to avoid $1/f$ noise corner frequency and low enough that device capacitances can be treated as open. Figure 6.12 shows the simplified, low-frequency HEMT small-signal model with the pertinent noise sources. The parasitic gate and source access resistances R_G and R_S, respectively, contribute thermal noise at the physical temperature T_{phys}. The noise contribution of drain access resistance R_D is ignored as it is after

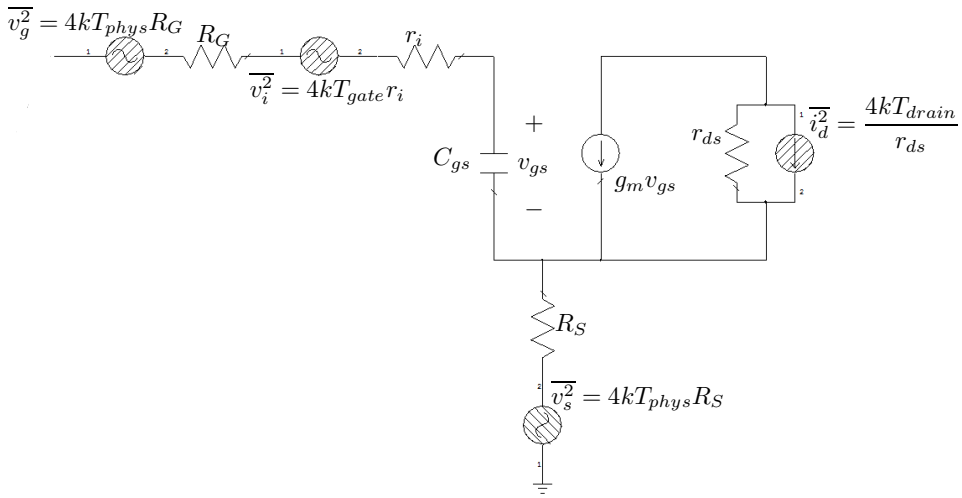

Figure 6.12: Simplified HEMT small-signal model used for T_{drain} extraction.

the gain stage. The small-signal gate-source and drain-source resistances r_i and r_{ds}, respectively, are functions of transistor bias and are assigned noise temperatures T_{gate} and T_{drain} to model the HEMT noise [69]. As mentioned previously, in this work r_i is considered as an ohmic-type resistance generating thermal noise with $T_{gate} = T_{phys}$.

Defining the total gate-source resistance as

$$R_{GS} \equiv R_G + r_i + R_S. \tag{6.16}$$

the total noise power produced at the input is easily calculated from the simplified SSM as

$$\overline{v_{in}^2} = 4kT_{phys}R_{GS} + \frac{4kT_{drain}}{r_{ds}}\frac{1}{g_m^2} \tag{6.17}$$

Then, the input noise temperature of the transistor driven with a 50 Ω source is simply

$$T_{50} = \frac{\overline{v_{in}^2}}{4k \cdot 50} \tag{6.18}$$

Consequently, T_{drain} is given by,

$$T_{drain} = \left(T_{50} - T_{phys}\frac{R_{GS}}{50}\right) g_m^2 r_{ds} 50 \tag{6.19}$$

As both T_{drain} and the small-signal model element values are known, the transistor performance including gain and noise can now be modeled. Before proceeding with the latter, a quick overview of fundamental two-port noise equations is provided. Noise temperature of a two-port at an arbitrary

generator impedance $Z_{gen} = R_{gen} + jX_{gen}$ can be written as [93]

$$T_n = T_{min} + NT_0 \frac{|Z_{gen} - Z_{opt}|^2}{R_{gen} R_{opt}} \tag{6.20}$$

Here, T_{min} is the minimum noise temperature; $T_0 = 290$ K; $Z_{opt} = R_{opt} + jX_{opt}$ is the generator impedance that yields $T_n = T_{min}$; and N is a parameter invariant under lossless transformations and quantifies sensitivity of T_n with respect to generator impedance. The noise measure is given by [69]

$$M = \frac{T_n}{T_0} \frac{1}{1 - \frac{1}{G_a}}, \tag{6.21}$$

where G_a is the available gain of the two-port, from which the cascaded noise temperature T_{CAS} at an arbitrary generator impedance is easily obtained as [70]

$$T_{CAS} = T_0 M = \frac{T_n}{T_0} \frac{1}{1 - \frac{1}{G_a}} \tag{6.22}$$

which is close to T_n when the available gain of the stage is high.

Pospieszalski [69] derived closed-form expressions for all of these quantities for the intrinsic FET. They are repeated here for the sake of completeness and also because they are modified to use total gate resistance R_{GS} instead of r_i :

$$T_{min} = 2\frac{f}{f_T} \sqrt{g_{ds} R_{GS} T_{gate} T_{drain} + \left(\frac{f}{f_T}\right)^2 g_{ds}^2 R_{GS}^2 T_{drain}^2} + 2\left(\frac{f}{f_T}\right)^2 g_{ds} R_{GS} T_{drain} \tag{6.23}$$

$$NT_0 = \frac{T_{min}}{2} \left(1 + \frac{R_{GS}}{R_{opt}}\right)^{-1} \tag{6.24}$$

$$R_{opt} = \sqrt{\left(\frac{f_T}{f}\right)^2 \frac{R_{GS}}{g_{ds}} \frac{T_{gate}}{T_{drain}} + R_{GS}^2}, \qquad X_{opt} = \frac{1}{\omega C_{gs}} \tag{6.25}$$

$$f_T = \frac{g_m}{2\pi \left(C_{gs} + C_{gd}\right)} \tag{6.26}$$

where it is noted that the definition of f_T in [69] neglects C_{gd}. Available gain with arbitrary generator impedance is given as

$$\frac{1}{G_a} = \frac{1}{G_{a,max}} + \frac{g_g}{R_{gen}} |Z_{gen} - Z_{opt,G}|^2 \tag{6.27}$$

where $Z_{opt,G}$ is the generator impedance realizing maximum available gain $G_{a,max}$. The expressions

for these are

$$Z_{opt,G} = R_{GS} + j\frac{1}{\omega C_{gs}} \tag{6.28}$$

$$G_{a,max} = \left(\frac{f_T}{f}\right)^2 \frac{1}{4 g_{ds} R_{GS}} \tag{6.29}$$

$$g_g = \left(\frac{f}{f_T}\right)^2 g_{ds}. \tag{6.30}$$

Finally, the generator impedance minimizing the noise measure is [69]

$$Z_{opt,M} = R_{GS}\left[\sqrt{\left(\frac{T_{gate}}{T_{drain}} - 1\right)^2 + \frac{R_{opt}^2}{R_{GS}^2} - 1} - \frac{T_{gate}}{T_{drain}}\right] + j\frac{1}{\omega C_{gs}}. \tag{6.31}$$

These equations are now used along with $T_{50,\,1\mathrm{GHz}}$ measurements to model noise performance of the large transistors from each process.

6.4.3 Results

Figure 6.13 presents the measured quantities g_m, r_{ds}, and $T_{50,\,1\mathrm{GHz}}$ in addition to the derived T_{drain}. T_{CASmin} and available gain at the generator impedance that yields T_{CASmin} are plotted in Figure 6.14 at 6 and 100 GHz. Finally, calculated f_T, f_{max}, and noise current $\overline{i_d^2}$ are provided in Figure 6.15.

The most important observation from these plots is the sizable increase in all noise temperatures of all devices when V_{DS} is increased from 0.6 to 0.8 V at both temperatures. This increase is largest on the NGC 100% device which further suggests the occurrence of strong impact ionization. Moreover, this noise increase is contrary to what manufacturers' small-signal models predict. It is, however, consistent with the LNA measurements of the next chapter. There is little performance change between 0.4 and 0.6 V which suggests the devices are not very sensitive to drain bias. That is, until the onset of impact ionization when noise degrades significantly.

It is also interesting to note that the NGC 75% devices perform as well as the 100% devices noise-wise at W-band. Slightly lower available gain of these transistors, however, imply lower f_T's which would limit their use in THz applications. The OMMIC device exhibits the lowest T_{drain} over bias and temperature, and at 6 GHz exhibit performance on par with those of the NGC InP devices. As expected, it also has the lowest f_T/f_{max} values. Consequently, the OMMIC process seems to be most applicable to radio astronomy applications up to about 50 GHz.

Figure 6.16 plots T_{CASmin} and $\Re\{Z_{opt,M}\}$ versus frequency at $V_{DS} = 0.4$, 0.6, 0.8 V for 4-finger transistors from the three processes. Calculations are carried out on larger transistors at lower frequencies in order to ensure $\Re\{Z_{opt,M}\}$ is relatively closer to 50 Ω. These curves reinforce the

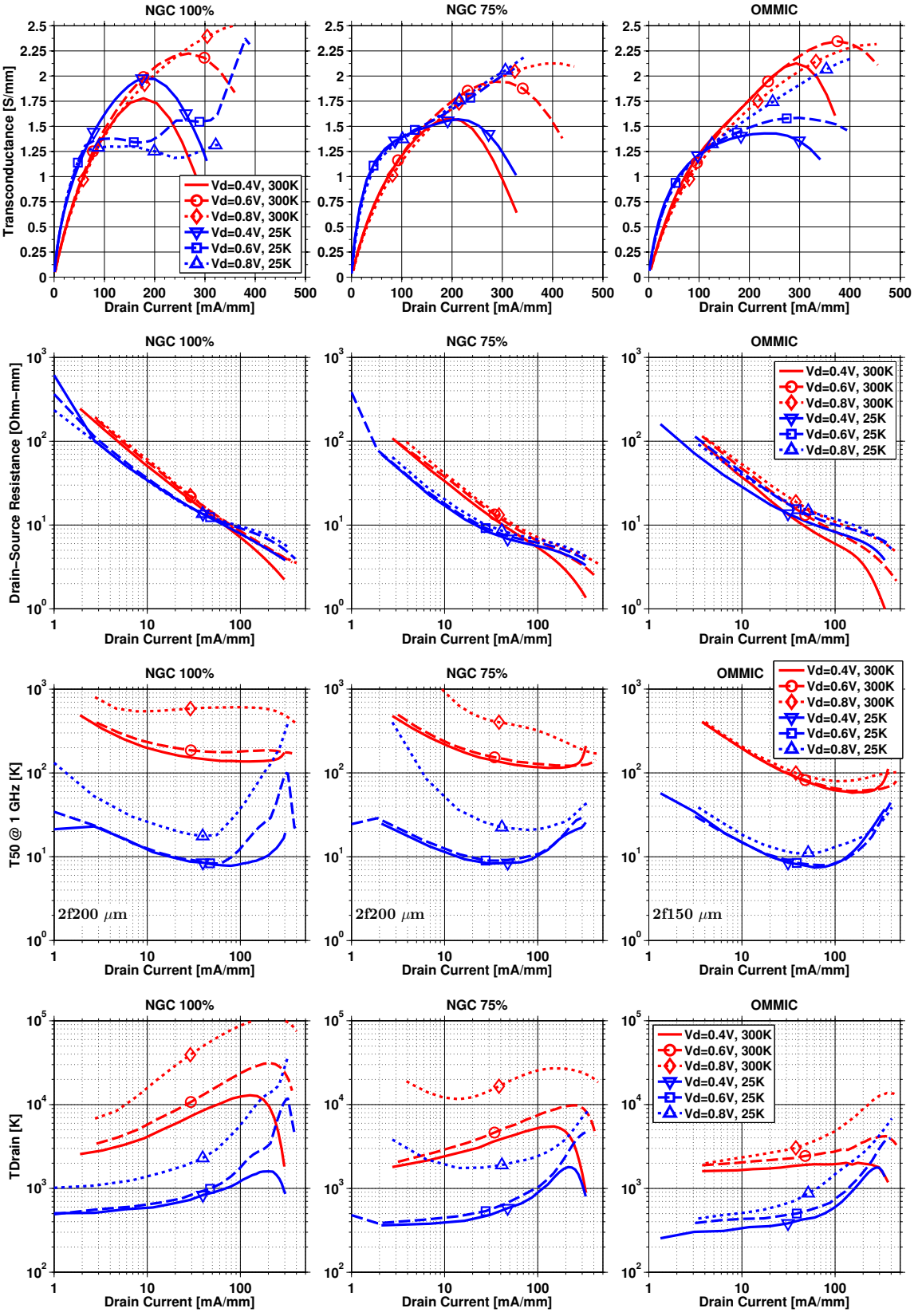

Figure 6.13: Measured g_m, r_{ds}, $T_{50,1\text{GHz}}$, and derived T_{drain} of the NGC and OMMIC devices

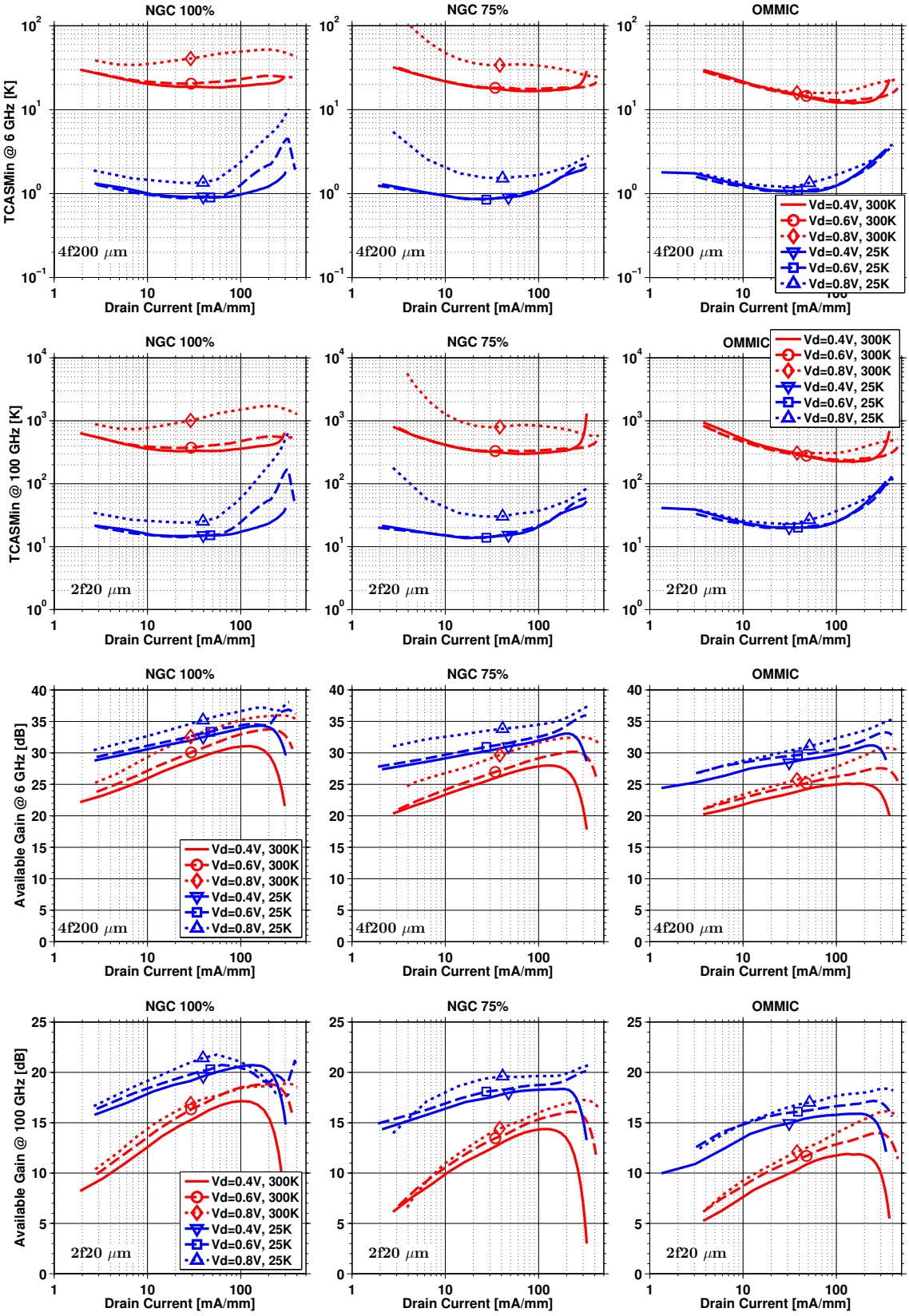

Figure 6.14: Minimum cascaded noise temperature and available gain at 6 and 100 GHz of the NGC and OMMIC transistors

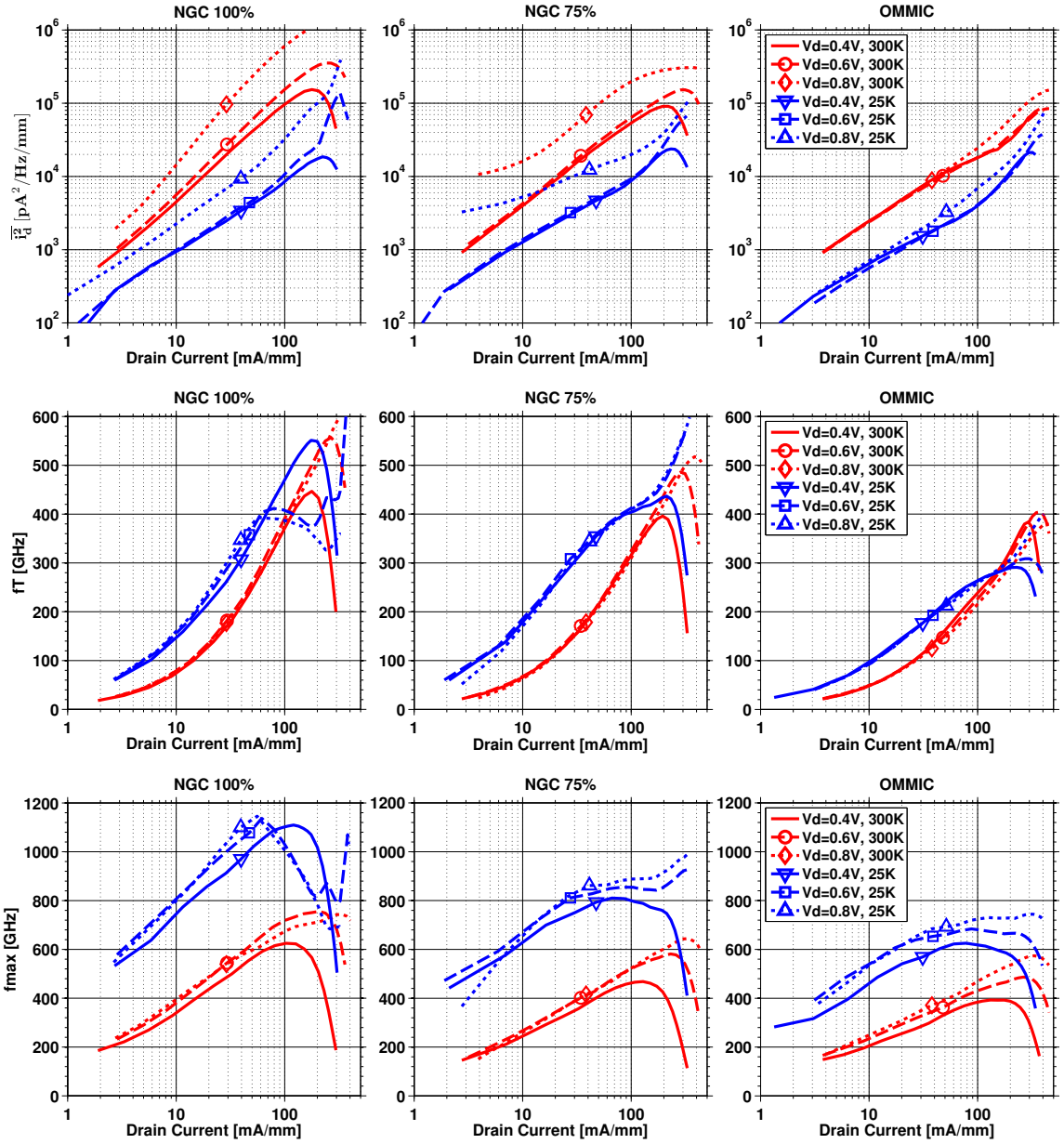

Figure 6.15: Drain noise current (normalized to gate periphery), f_T, and f_{max} of the NGC and OMMIC transistors

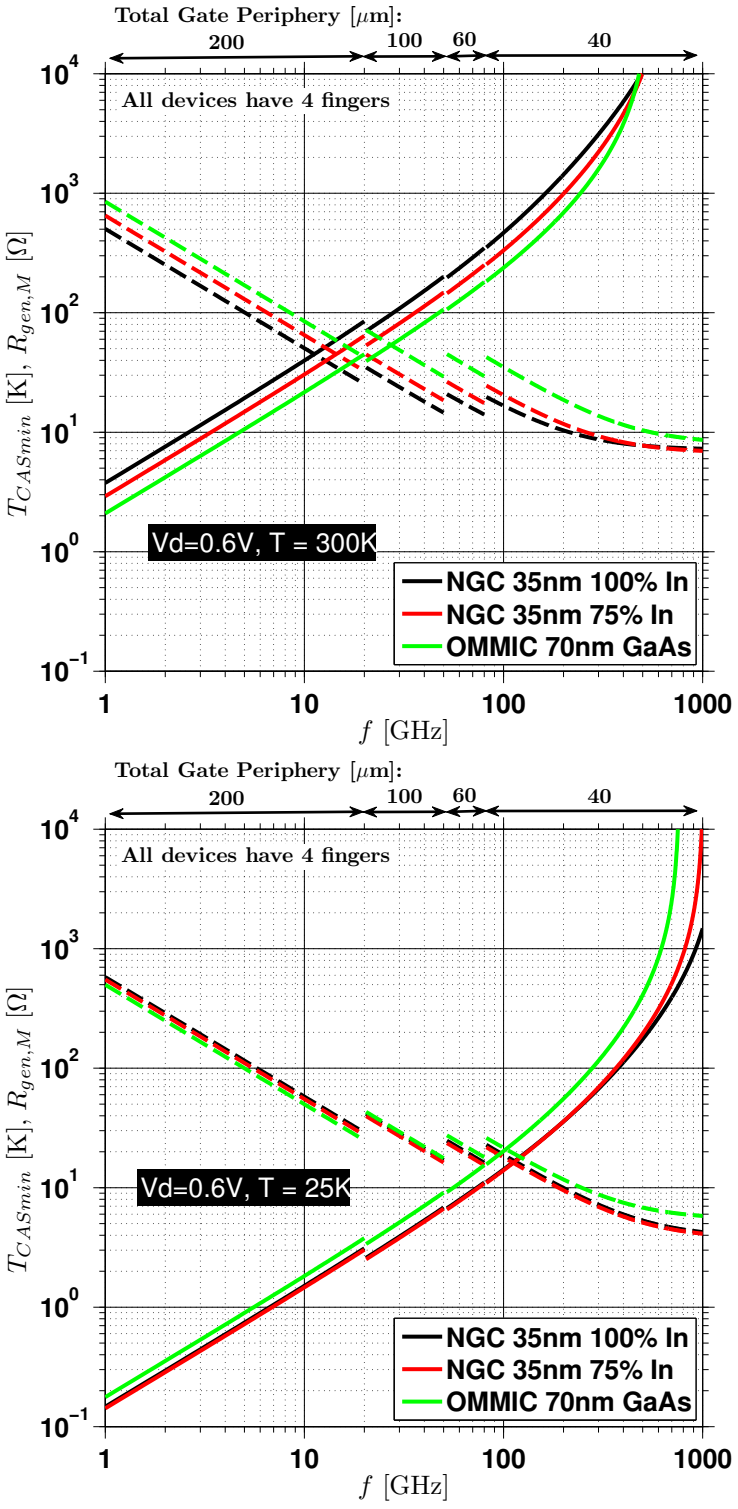

Figure 6.16: T_{CASmin} (solid) and $\Re\{Z_{gen,M}\}$ (dashed) of the three processes versus frequency at 300 K (top) and 25 K (bottom). $I_{DS} = 100$, 150 mA/mm at 300 K and $I_{DS} = 25$, 40 mA/mm at 25 K for NGC and OMMIC devices, respectively.

earlier observation regarding the suitability of the 100% NGC devices for THz applications. They also show that the OMMIC transistor is within 1–2 Kelvin of the NGC 75% transistor up to 50 GHz beyond which its noise begins to diverge slowly. $V_{DS} = 0.6$ V appears to be the optimum drain bias for $f > 250$ GHz.

The validity of T_{CASmin} predictions at $V_{DS} = 0.8$ V beyond 20 GHz is questionable. This is because the noise measurements performed at 1 GHz are affected by impact ionization; however, S-parameter measurements of previous section points to negligible effect on small-signal performance at such high frequencies which is consistent with measurements of NGC 100% LNAs at W-band [16, 94].

Tables 6.2-6.7 provide the small-signal parameters, measurements and the derived quantities at the three drain bias voltages.

6.5 Conclusions

DC, microwave, and noise performance of GaAs mHEMT and InP pHEMT transistors were presented for both room and cryogenic temperatures. Measurements indicate occurrence of impact ionization on all devices with the 100% In pHEMT devices exhibiting the most severe signs. The transistors' output characteristics exhibit kinks whose occurrence seems to be well correlated with onset of impact ionization based not only on DC tests but also cryogenic S-parameter and noise measurements. Further, the first reported measurements of T_{drain} versus bias of HEMT transistors at both temperatures were presented showing the 70 nm OMMIC GaAs process to be on par with the 35 nm NGC InP process at frequencies below 50 GHz.

A method of T_{drain} determination by 1 GHz discrete transistor measurements has been demonstrated with reasonable but questionable results for prediction of minimum cascaded noise temperature, T_{CASmin}, at 6 GHz and 100 GHz. The main limitations of the method are:

1. The accuracy of T_{drain} at 300K depends strongly on accurate values of the gate circuit resistances because their thermal noise can dominate the $T_{50,\,1\mathrm{GHz}}$ measurement. This is much less the case at cryogenic temperatures;

2. It is assumed that T_{drain} (as well as all other SSM element values) are independent of frequency. This assumption is especially questionable in the case of impact ionization. Future measurements of T_{drain} from 0.5 to 5 GHz would be interesting;

3. It should be recognized that the assignment of the drain noise to the effective temperature, T_{drain}, of r_{ds} is questionable. An assignment to a drain noise current generator, $\overline{i_d^2}$, may provide a better comparison with theory. r_{ds} is a function of $\frac{dV_{DS}}{dI_{DS}}$ while the drain noise is more likely to be a function of I_{DS};

Table 6.2: Small-signal model parameters at $V_{DS} = 0.4$ V

I_{DS}		r_i	r_{ds}	g_m	C_{gs} [fF]		C_{gd} [fF]	
[mA/mm]		[Ω]	[Ω]	[mS]	4f200	2f20	4f200	2f20
				300 K				
20	100%	0.3	142.2	86.2	55.5	7.4	51.2	4.3
	75%	0.3	93.6	75.4	55.5	7.4	51.2	4.3
	OMM	0.6	100	70.7	92.5	9.3	43.6	4.4
50	100%	0.37	64.5	178.9	65.2	8.7	50.1	4.2
	75%	0.37	44.7	154.9	65.2	8.7	50.1	4.2
	OMM	0.73	46.9	153.5	108.7	10.9	42.7	4.3
100	100%	0.44	35.8	283.4	73.1	9.8	48.6	4.1
	75%	0.44	27.1	241	73.0	9.7	48.7	4.1
	OMM	0.88	30	244.2	121.6	12.2	41.5	4.2
150	100%	0.48	24.4	345.1	78.3	10.4	47.9	4.0
	75%	0.48	19.4	296.2	78.3	10.4	47.9	4.0
	OMM	0.95	23.1	302	130.4	13.0	40.8	4.1
				25 K				
20	100%	0.3	104.3	131.4	50.0	6.7	46.1	3.8
	75%	0.3	54.1	152.7	50.0	6.7	46.1	3.8
	OMM	0.6	88.2	112.2	83.3	8.3	39.3	3.9
50	100%	0.37	59.2	225.7	58.7	7.8	45.1	3.8
	75%	0.37	33.8	233.8	58.7	7.8	45.1	3.8
	OMM	0.73	54.9	185.7	97.8	9.8	38.4	3.8
100	100%	0.44	39.4	323.5	65.7	8.8	43.8	3.7
	75%	0.44	28.1	277.8	65.7	8.8	43.8	3.7
	OMM	0.88	41.4	243.4	109.6	11.0	37.3	3.7
150	100%	0.48	30.6	381.4	70.4	9.4	43.1	3.6
	75%	0.48	24.9	298.6	70.4	9.4	43.1	3.6
	OMM	0.95	35.7	270.3	116.9	11.7	36.8	3.7

Table 6.3: Small-signal model parameters at $V_{DS} = 0.6$ V

I_{DS}		r_i	r_{ds}	g_m	C_{gs} [fF]		C_{gd} [fF]	
[mA/mm]		[Ω]	[Ω]	[mS]	4f200	2f20	4f200	2f20
				300 K				
20	100%	0.3	150.8	87.0	54.8	7.3	46.5	3.9
	75%	0.3	106.7	73.9	54.8	7.3	46.5	3.9
	OMM	0.6	131.1	68.4	91.4	9.1	39.6	4.0
50	100%	0.36	71.8	182.7	68.0	9.1	44.5	3.7
	75%	0.37	51.1	153.3	68.6	9.1	44.4	3.7
	OMM	0.73	64.4	144.5	114.3	11.4	37.9	3.8
100	100%	0.44	42.4	293.5	76.7	10.2	42.7	3.6
	75%	0.44	32.5	243.1	76.7	10.2	42.7	3.6
	OMM	0.88	41.9	233.4	127.8	12.8	36.4	3.6
150	100%	0.48	32.1	367.1	83.2	11.1	41.2	3.4
	75%	0.48	25.8	304.6	83.2	11.1	41.2	3.4
	OMM	0.95	32.9	299	138.7	13.9	35.1	3.5
				25 K				
20	100%	0.3	110.0	133.2	49.4	6.6	41.8	3.5
	75%	0.3	58.7	149.9	49.4	6.6	41.8	3.5
	OMM	0.6	126.0	104.2	82.3	8.2	35.6	3.6
50	100%	0.37	60.7	234.3	61.7	8.2	40.0	3.3
	75%	0.36	36.8	230.3	61.4	8.2	40.0	3.3
	OMM	0.73	67.9	181.1	102.1	10.2	34.1	3.4
100	100%	0.44	45.7	275.1	69.0	9.2	38.4	3.2
	75%	0.44	30.8	278.1	69.0	9.2	38.4	3.2
	OMM	0.88	50.6	243.8	115.1	11.5	32.7	3.3
150	100%	0.48	39.0	270.4	74.9	10.0	37.1	3.1
	75%	0.48	27.6	305.6	74.9	10.0	37.1	3.1
	OMM	0.95	44.5	276.0	124.9	12.5	31.6	3.2

Table 6.4: Small-signal model parameters at $V_{DS} = 0.8$ V

I_{DS}		r_i	r_{ds}	g_m	C_{gs} [fF]		C_{gd} [fF]	
[mA/mm]		[Ω]	[Ω]	[mS]	4f200	2f20	4f200	2f20
				300 K				
20	100%	0.3	158.6	84.3	56.2	7.5	43.5	3.6
	75%	0.3	112.4	69.5	56.1	7.5	43.5	3.6
	OMM	0.6	151.5	66.4	93.6	9.4	37.1	3.7
50	100%	0.36	71.4	173.4	69.5	9.3	41.0	3.4
	75%	0.37	54.6	145.2	69.5	9.3	41.0	3.4
	OMM	0.73	78.9	139	115.8	11.6	35.0	3.5
100	100%	0.44	40.1	280.3	79.9	10.6	38.4	3.2
	75%	0.44	35.7	230.4	79.9	10.6	38.4	3.2
	OMM	0.88	54.6	224.8	133.1	13.3	32.8	3.3
150	100%	0.48	30.3	351.4	87.0	11.6	36.3	3.0
	75%	0.48	29.6	290.2	86.8	11.6	36.3	3.0
	OMM	0.95	45.9	286.0	144.7	14.5	31.0	3.1
				25 K				
20	100%	0.3	107.2	134.6	50.2	6.7	39.2	3.3
	75%	0.3	65.1	141.3	50.1	6.7	39.2	3.3
	OMM	0.6	125.5	103.7	84.3	8.4	33.4	3.3
50	100%	0.36	62.0	235.9	62.5	8.3	36.9	3.1
	75%	0.36	40.4	222.8	62.5	8.3	36.9	3.1
	OMM	0.73	75.1	179.4	104.2	10.4	31.5	3.1
100	100%	0.44	48.5	258.9	71.9	9.6	34.6	2.9
	75%	0.44	33.7	273.8	71.9	9.6	34.6	2.9
	OMM	0.88	59.1	242.1	119.8	12.0	29.5	2.9
150	100%	0.48	42.2	259.9	78.2	10.4	32.7	2.7
	75%	0.48	30.4	304.6	78.2	10.4	32.7	2.7
	OMM	0.95	51.2	282.9	130.4	13.0	27.9	2.8

Table 6.5: Measured and corrected $T_{50,1\text{GHz}}$ and derived parameters at $V_{DS} = 0.4$ V. All parameters, except those that are marked, are for 4f200 μm device size. OMMIC $R_G = R_S = 1\,\Omega$ and NGC $R_G = 1.75\Omega$, $R_S = 0.95\Omega$ at 300 K. These values are halved cryogenically.

I_{DS}		T_{50}‡	T_{drain}	i_d	T_{CASmin} [K]		$Z_{gen,M}$ [Ω]				G_{av} [dB]		f_T	f_{max}
[mA/mm]		[K]	[K]	[pA/$\sqrt{\text{Hz}}$]	6GHz	100GHz*	R 6GHz	X 6GHz	R 100GHz*	X 100GHz*	6GHz	100GHz*	[GHz]	
300 K														
	100%	165.2	5881	47.8	18.9	330.1	98.1	478.5	37.2	215.3	27.8	14.4	128.2	434.6
20	75%	163.9	2925	41.5	18.8	339.8	98.6	478.5	36.5	215.3	24.8	11.5	112.1	309.0
	OMM	125.2	1732	30.9	17.6	371.5	91.3	286.9	42.9	172.1	22.9	9.1	82.5	254.3
	100%	142.6	9445	89.9	18.5	331.1	102.4	407	38.9	183.1	30.0	16.4	246.8	562.6
50	75%	128.6	4166	71.7	17.0	303.8	111.1	407	41.2	183.1	26.8	13.4	213.6	405.8
	OMM	78.6	1914	47.5	14.0	270.1	119.6	244.2	57.1	146.5	24.3	10.9	161.3	332.9
	100%	137.3	12437	138.5	19.2	360.1	101.4	362.9	38.9	163.3	31.0	17.1	370.3	623.8
100	75%	117.1	5232	103.2	16.7	306.5	115.7	363.6	43.2	163.6	27.9	14.3	315.2	462.0
	OMM	62.2	1949	59.9	12.2	228.1	144.1	218.1	69.7	130.9	25.0	11.8	238.1	383.8
	100%	137.8	12674	169.2	20.1	390.9	98.2	338.9	37.9	152.5	30.9	16.8	435.3	603.2
150	75%	115.2	5491	125.1	17.2	324.0	114	339	42.7	152.5	27.9	14.2	373.7	461.4
	OMM	58.2	1939	68.1	11.9	222.6	151.4	203.4	73.6	122	25.1	11.8	280.6	392.1
25 K														
	100%	9.7	668	18.8	0.9	14.7	92.6	531.3	36.1	239.1	31.5	18.8	217.5	862.2
20	75%	9.1	429	20.9	0.9	13.8	91.9	533.3	35.7	240.0	29.9	17.2	252.1	712.8
	OMM	10.1	355	14.9	1.1	20.5	77.8	318.5	39.6	191.1	28.1	14.6	145.6	540
	100%	8.1	888	28.8	0.9	15	98.3	452.1	38.4	203.5	32.9	19.9	346	1014.8
50	75%	8.5	592	31.1	0.9	15.4	90.8	452.2	35.5	203.5	31.1	18.0	358.6	795.5
	OMM	7.8	433	20.9	1.1	20.2	86	271.3	44.7	162.8	29.0	15.5	216.8	609.5
	100%	8.2	1216	41.3	1.0	17.2	95.2	403.6	37.7	181.6	33.9	20.6	469.9	1101.7
100	75%	10.3	891	41.8	1.1	20.8	77.9	404.1	31.2	181.8	31.9	18.3	403.8	799.9
	OMM	8.2	599	28.3	1.2	24.9	80.8	242.0	43.3	145.2	29.8	15.8	263.6	618.2
	100%	9.0	1500	52.0	1.1	20.2	86.9	377.0	34.7	169.7	34.3	20.7	534.8	1094.5
150	75%	14.3	1354	54.8	1.4	29.4	62.1	376.7	25.7	169.5	32.7	18.3	418.6	773.1
	OMM	11.1	909	37.5	1.6	34.8	66.0	226.9	36.8	136.2	30.5	15.9	279.9	598.3

*: Calculated for a 2f20 μm transistor; ‡ : $T_{50,\,1\text{GHz}}$ measurements collected on NGC 2f200μm and OMMIC 2f150μm devices

Table 6.6: Measured and corrected $T_{50,1\text{GHz}}$ and derived parameters at $V_{DS} = 0.6$ V. All parameters, except those that are marked, are for 4f200 μm device size. OMMIC $R_G = R_S = 1\,\Omega$ and NGC $R_G = 1.75\Omega$, $R_S = 0.95\Omega$ at 300 K. These values are halved cryogenically.

I_{DS}		T_{50}‡	T_{drain}	i_d	T_{CASmin} [K]		$Z_{gen,M}$ [Ω]				G_{av} [dB]		f_T	f_{max}
[mA/mm]		[K]	[K]	[pA/$\sqrt{\text{Hz}}$]	6GHz	100GHz*	R 6GHz	X 6GHz	R 100GHz*	X 100GHz*	6GHz	100GHz*	[GHz]	
300 K														
	100%	199.3	8514	55.8	20.5	369.2	90.7	483.7	34.6	217.7	29.1	15.4	136.6	483.5
20	75%	179.9	3672	43.6	19.1	346.3	97.2	484.2	36.1	217.9	25.7	12.3	115.8	341.0
	OMM	127.4	2177	30.3	17.1	346.9	93.8	290.4	44.8	174.2	24	10.3	83.0	292.9
	100%	178.3	15145	107.9	21.3	408.3	89.2	390.4	34.2	175.7	31.4	17.3	258.2	619.6
50	75%	142.4	5484	77.0	18.1	335.2	104.6	387.0	38.7	174.1	27.7	14.1	215.8	438.5
	OMM	80.9	2454	45.9	14.4	276	116.2	232.2	56.2	139.3	25.2	11.8	151.1	366.2
	100%	180.1	23672	175.6	23.1	473.6	84.7	345.9	33.1	155.6	33.0	18.5	391.3	718.5
100	75%	128.2	7458	112.5	17.8	336.8	109.2	346.0	40.6	155.7	29.1	15.3	324.0	520.6
	OMM	65.5	2762	60.4	13.0	241.9	135.9	207.6	66.8	124.5	26.2	12.9	226.1	430.6
	100%	184	28874	222.8	24.6	530.9	80.6	318.7	31.9	143.4	33.5	18.8	469.4	746.2
150	75%	123.4	8716	136.5	18.0	350.8	108.9	318.7	40.5	143.4	29.7	15.8	389.4	554.9
	OMM	61	3015	71.1	12.8	238	141.5	191.2	70.1	114.7	26.7	13.3	273.6	456.5
25 K														
	100%	10	729	19.1	0.9	14.3	95.6	538.3	36.9	242.2	32.1	19.3	231.9	930.1
20	75%	10	496	21.6	0.9	14.1	91.3	539.3	35.2	242.7	30.5	17.7	260.5	762.1
	OMM	10.6	449	14.0	1.1	19.9	78.9	322.9	40.4	193.8	29.1	15.7	140.2	615.7
	100%	8.3	1017	30.4	0.9	15.3	98.6	430.0	37.9	193.5	33.5	20.4	366.7	1089.1
50	75%	9.2	693	32.3	0.9	16.3	88.3	432.3	34.1	194.5	31.6	18.4	361.2	835.1
	OMM	8.2	541	21.0	1.1	20.9	83.5	260.1	43.6	156.1	29.8	16.2	211.5	660.5
	100%	12.5	1778	46.3	1.3	24.6	73.8	384.3	29.3	172.9	34.4	20.4	407.6	1030.2
100	75%	10.8	1034	43.0	1.1	21.5	77.1	384.4	30.4	173	32.6	18.7	411.9	854.5
	OMM	8.4	751	28.6	1.3	25.3	79.5	230.7	42.9	138.4	30.7	16.6	262.5	680.8
	100%	21.2	2682	61.6	1.8	41.4	52.7	354.1	22.1	159.4	34.5	19.6	384.2	887.5
150	75%	14.1	1548	55.6	1.4	29.4	63.6	354.1	25.7	159.4	33.3	18.9	434.2	844.7
	OMM	10.4	1100	36.9	1.6	33.7	67.1	212.5	37.5	127.5	31.4	16.8	280.7	670.2

*: Calculated for a 2f20 μm transistor; ‡ : $T_{50,\,1\text{GHz}}$ measurements collected on NGC 2f200μm and OMMIC 2f150μm devices

Table 6.7: Measured and corrected $T_{50,1\text{GHz}}$ and derived parameters at $V_{DS} = 0.8$ V. All parameters, except those that are marked, are for 4f200 μm device size. OMMIC $R_G = R_S = 1\,\Omega$ and NGC $R_G = 1.75\Omega$, $R_S = 0.95\Omega$ at 300 K. These values are halved cryogenically.

I_{DS}		T_{50}‡	T_{drain}	i_d	T_{CASmin} [K]		$Z_{gen,M}$ [Ω]				G_{av} [dB]		f_T	f_{max}
[mA/mm]		[K]	[K]	[pA/$\sqrt{\text{Hz}}$]	6GHz	100GHz*	R 6GHz	X 6GHz	R 100GHz*	X 100GHz*	6GHz	100GHz*	[GHz]	
300 K														
	100%	569	29132	100.7	38.6	916.3	49.6	472.3	21.8	212.5	31.5	16.1	134.4	487.6
20	75%	505.5	12260	77.6	36.1	848.2	52.9	472.6	22.5	212.7	28.1	12.9	110.9	338.5
	OMM	137.1	2661	31.1	17.9	365.2	89.5	283.4	43.3	170	24.6	10.8	80.9	308.5
	100%	602.3	58178	212.1	45.1	1236	43.9	382.8	20.6	172.2	33.8	17.6	249.1	595.5
50	75%	383.3	19136	139.1	34.5	832.7	56.4	381.9	23.8	171.8	30.2	14.8	209	440.6
	OMM	91.7	3423	48.9	15.9	307.3	106.1	229.1	52.3	137.4	26.3	12.6	146.7	394.4
	100%	608.9	87979	347.9	49.4	1507	41.3	332.2	20.4	149.5	35.2	18.4	377	673.7
100	75%	320.0	25552	198.7	33.5	836.8	59.3	332.2	25.1	149.5	31.6	16.0	309.9	522.6
	OMM	79.7	4820	69.8	15.8	306.9	112.3	199.3	56.8	119.6	27.8	14.0	215.7	469.3
	100%	600.2	102863	432.7	51.5	1664.6	40.2	305.0	20.4	137.3	35.7	18.6	453.7	700.8
150	75%	268.6	27051	224.8	31.5	781.4	63.8	305.6	26.4	137.5	32.1	16.6	374.9	571.5
	OMM	81.2	6696	89.7	17.1	341.8	106.3	183.4	54.9	110.0	28.8	14.8	259.1	510.4
25 K														
	100%	20.9	1713	29.7	1.4	24.5	63.1	530.1	25.0	238.6	33.9	20.3	238.6	940.3
20	75%	31.2	1762	38.7	1.6	32.1	49.0	531.2	20.0	239.1	33.2	19.0	250.6	770.4
	OMM	13.3	580	16	1.2	23.6	69.2	315.1	35.8	189.1	29.7	15.9	139.9	613.7
	100%	18	2710	49.1	1.4	27.6	62.9	425.2	25.0	191.4	35.7	21.6	376.9	1130
50	75%	22	1991	52.2	1.6	31.8	53.7	425.6	21.7	191.5	33.9	19.6	356.1	862.8
	OMM	11.1	858	25.1	1.3	26.5	69.5	254.7	37.1	152.8	31.0	17.0	210.2	691.8
	100%	37.8	5743	80.8	2.4	60.0	40.6	369.3	17.8	166.2	36.6	21.0	387.0	1008
100	75%	21.3	2430	63.1	1.7	37.2	52.2	369.1	21.6	166.1	34.5	19.6	409.3	887.8
	OMM	13.1	1479	37.2	1.7	36.8	60.2	221.5	33.8	132.9	32.3	17.7	258.1	723.6
	100%	73.5	10132	115.1	3.6	118.1	27.5	339.4	14.2	152.7	37.2	20.1	373.1	897.4
150	75%	23.8	3056	74.5	1.9	45.1	47.7	339.3	20.2	152.7	35.0	19.7	437.2	891.3
	OMM	15.3	2070	47.3	2.0	46.8	53.1	203.5	31.1	122.1	33.0	17.9	284.6	728.3

*: Calculated for a 2f20 μm transistor; ‡ : $T_{50,\,1\text{GHz}}$ measurements collected on NGC 2f200μm and OMMIC 2f150μm devices

4. Much attention must be paid to the accuracy of the 1 GHz noise measurements. Factors such as calibration accuracy of the noise source, losses in DC bias tees, extrinsic vs intrinsic g_m, and correction for post-amplifier noise in the presence of a mismatched output of the test transistor must be considered;

5. Gate leakage current, which constitutes a shot noise source, is neglected in this development. While total gate leakage is easily obtained from $I-V$ measurements, what is needed is the individual components of gate leakage, i.e., $I_G = I_{GS} + I_{GD}$ from which the shot noise source can be modeled using $\overline{i_g^2} = 2q\left(|I_{GS}| + |I_{GD}|\right)$. Inclusion of this noise source would lower predicted T_{drain} measurements presented herein.