Part II

Compound-Semiconductor LNAs

Chapter 5

Introduction to Two State-of-the-Art HEMT Processes

The second part of the thesis focuses on room-temperature and cryogenic performance of discrete high-electron mobility transistors (HEMTs) and microwave monolithic integrated circuit (MMIC) LNAs achieving very low noise over decade bandwidths from two state-of-the-art HEMT processes: 35 nm InP pHEMT and 70 nm GaAs mHEMT, whose key features are presented in Table 5.1. The first chapter of this part of the thesis introduces the key features of the processes. The second chapter provides detailed DC, microwave, and noise characterization of discrete transistors. Finally, the LNA designs are presented in the third chapter of this part.

As alluded to in the Introduction, indium phosphide (InP) pseudomorphic HEMT (pHEMT) transistors have long been the semiconductor of choice for extremely low-noise amplifiers operating in RF, microwave and millimeter-wave bands due their superior noise and gain performance up through 150 GHz [13, 14, 15, 16, 17, 18]. On the other hand, among all semiconductors InP experiences the slowest development due to its niche market; thus, it also tends to be the most expensive.

Recent trends in radio astronomy are in the direction of increased number of elements, be it dishes or focal plane elements, simultaneously covering decade bandwidths. Such systems necessitate very large number of ultra-widebandwidth LNAs with low power consumption. Due to increasing number of receiving elements, there is renewed emphasis on cost, yield and process stability. This leads to reconsideration of GaAs which is commercially more attractive and thus, has enjoyed more investment in process development in recent years [22, 23, 24].

5.1 70 nm GaAs mHEMT

OMMIC's 70 nm GaAs mHEMT process, referred to as D007IH, employs InGaAs-InAlAs-InGaAs-InAlAs epitaxy with 52%/70% indium content on a metamorphic buffer over GaAs semi-insulating substrate as shown in Figure 5.1 [65]. The transistors are depletion mode and use double-mushroom

	NGC 100% pHEMT	NGC 75% pHEMT	OMMIC mHEMT
L_g [nm]	35	35	70
Channel	InAs	$In_{0.75}Ga_{0.25}As$	$In_{0.7}Ga_{0.3}As$
Substrate	InP	InP	GaAs
Substrate Thickness [μm]	50	50	100
f_T [GHz]	> 500	> 500	300
f_{max} [GHz]	> 500	> 500	350
max g_m [mS/mm]	2300	˜1700	2500
max I_{DS} [mA/mm]	900	N/A	600
V_{BD} [V]	2.5 (D-S)	N/A	3 (G-D)

Table 5.1: Key features, provided by the foundries, of the NGC and OMMIC HEMT processes at 300K

gates. The key features of the process are summarized in Table 5.1.

Scalable small-signal model (SSM) of the transistor as a function of bias as well as microwave models for all passive components of the process are provided by OMMIC. No temperature dependence except for ohmic loss of passive components is available in the design kit. Due to the lack of temperature dependence in the transistor model, the design of all OMMIC LNAs presented herein was performed at 300 K.

In addition to the MMIC LNAs, calibration chips were also fabricated (see Figure 5.2 for a micro photograph). The chip includes short-open-load-thru (SOLT) standards and four transistors of sizes 2f40, 2f80, 2f150, and 8f800 μm. The OMMIC LNA designs use the first three of the four sizes; discrete 2f40 and 2f150 μm devices have been characterized extensively as explained in the next chapter.

5.2 35 nm InP pHEMT

Northrop Grumman Corporation's (NGC) 35 nm InP HEMT process is still under development and has produced record-breaking results above 75 GHz [66, 17, 67, 20, 21, 68]. The active layer profile is shown in Figure 5.3 [18]. A typical, experimental run in this process includes two wafers with 75% and 100% indium mole fractions in the active InGaAs layer. The key features of both 75% and 100% devices are listed in Table 5.1.

Small-signal model of a two-finger device with 30 μm total gate periphery (2f30 μm) at $V_{DS} =$ 1 V and $I_{DS} = 300$ mA/mm was provided by NGC for the 100% devices. The only temperature dependence included in the SSM is that of T_{drain} of the Pospieszalski model [69] and thermal noise

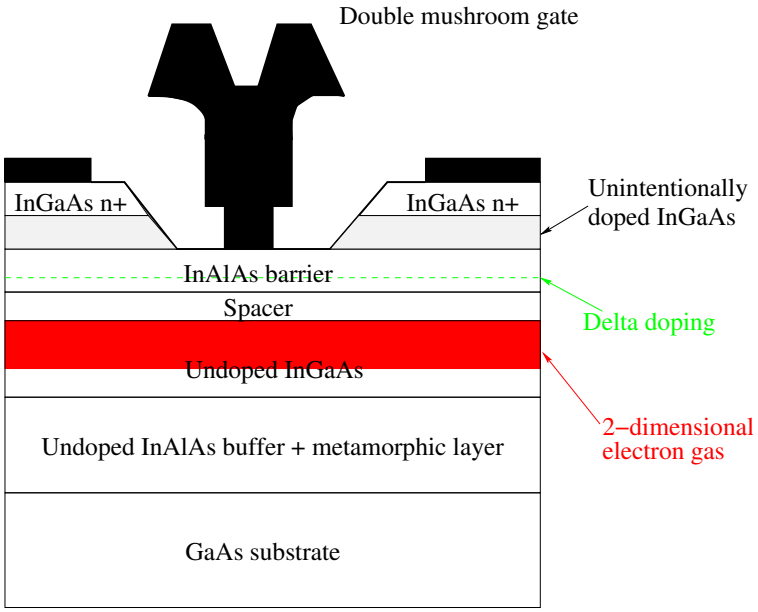

Figure 5.1: Active layer profile of OMMIC's 70 nm GaAs mHEMT

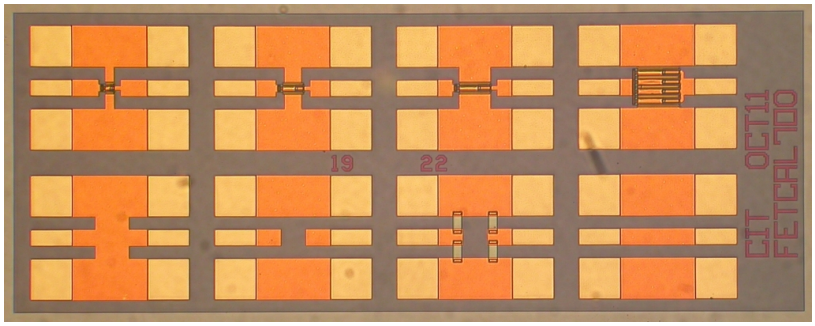

Figure 5.2: Micrograph of the OMMIC calibration chip

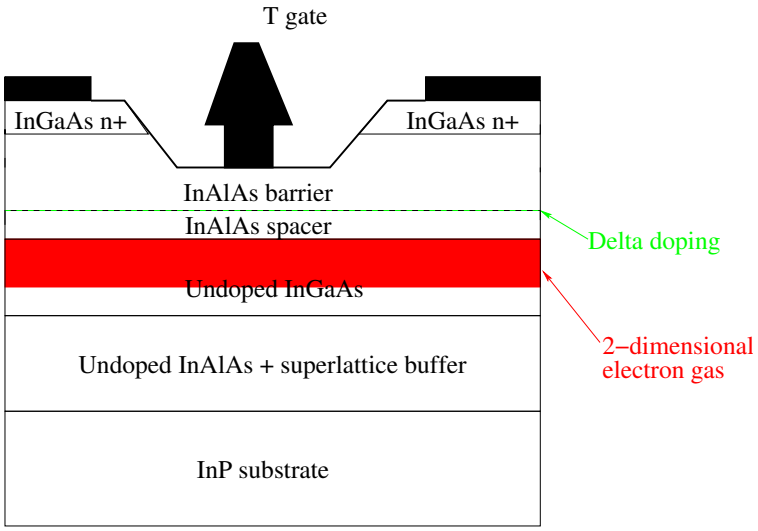

Figure 5.3: Active layer profile of NGC's 35 nm InP pHEMT

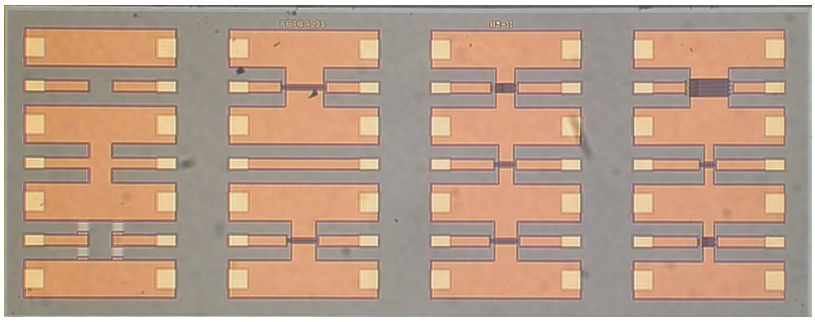

Figure 5.4: Micrograph of the NGC calibration chip

of all resistors. A scalable SSM was then generated to use in the LNA designs presented herein.

Calibration chips were fabricated on the NGC process as well and in addition to the SOLT standards, the following size transistors were included: 2f200, 2f130, 2f120, 2f80, 2f50, 4f200, 4f120, 8f800 μm. At least two of each size has been wafer-probed at room temperature; detailed measurements of discrete 2f50 and 2f200 μm devices are provided in the next chapter.