C h a p t e r 3

THERMAL CONDUCTIVITY REDUCTION IN PHONONIC NANOMESH STRUCTURES

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Controlling the thermal conductivity of a material independent of its electrical conductivity is a goal for researchers working on thermoelectric materials for energy applications [1,2] and for the cooling of integrated circuits [3]. In principle, the thermal conductivity κ and the electrical conductivity σ, may be independently optimized in semiconducting nanostructures because different length scales are associated with the heat carrying phonons and the electrical current carrying charges. Phonons are scattered at surfaces and interfaces, so κ generally decreases as the surface-to-volume ratio increases. By contrast σ is less sensitive to decreasing nanostructure size, although, at sufficiently small sizes, it will degrade via charger carrier scattering at interfaces [4]. Here we demonstrate an approach to independently controlling κ based upon altering the phonon band structure of a semiconductor thin film via the formation of a nanomesh film. Nanomesh phononic films are patterned with periodic spacings that are comparable to or shorter than the phonon mean-free-path. The results for the nanomesh films are compared against an equivalently prepared array of Si nanowires. The nanowire array possesses a significantly higher surface-to-volume ratio, but the nanomesh structure exhibits a substantially lower thermal conductivity. Bulk-like electrical conductivity is preserved. We argue that this points

towards coherent mechanism for lowering the thermal conductivity.

3.1 Introduction

The efficiency of a thermoelectric material is inversely proportional to the thermal conductivity, κ. Nanoscale structures are being explored for both reducing κ and for enhancing and decoupling the two other relevant parameters, the electrical conductivity (σ) and the thermopower (S), from each other and from κ [1,2,3]. For reducing κ, most work has focused on enhancing phonon scattering mechanisms [1,2]. Here we experimentally demonstrate a reduction in κ through the architectural modification of a thin Si film. Two sizes of nanomesh films, a nanowire array, and a continuous thin film, were fabricated from 20-25 nm thick Si films, and fully suspended for thermal conductivity measurements. The nanomesh films are square rigid structures, with inclusions at a periodic spacing of 385 nm and 34 nm. The nanowire array was comprised of >100 28×20 nm^2 cross-section nanowires. We find that κ is reduced as a consequence of both film architecture and feature size. Comparison of κ for the 34 nm nanomesh with our reference structures indicates that architecture can contribute at least a factor of 2 reduction in κ, a result that is not readily explained by enhanced phonon scattering, but may point towards coherent mechanisms for lowering thermal conductivity. We also demonstrate the effective decoupling of electronic and thermal conductivities. Our work suggests that Si nanomesh arrays may exhibit a peak ZT>1, and our results may be generally applicable to the design of thermoelectric materials.

The values of κ measured in nanoscale systems are often compared to the thermal conductivity of the bulk amorphous material (κ_{min}) [5]; and the characteristic length scales are compared to the dominant values of the heat carrying phonon mean-free-paths Λ and wavelengths λ [6]. For bulk Si at room temperature, κ_{min}~1 W/m-K, Λ~300 nm and λ~1-2 nm. Reductions in κ, through increased boundary scattering, are realized when system dimensions are smaller than Λ, as in the case of thin films, superlattices and nanowires. Alternatively, κ may also be reduced by elastic scattering when features are comparable to λ, such as in various classes of nanostructured bulk materials [7-9]. Finally, κ may be reduced through confinement altered phonon bands when features are smaller than λ [10]. For 10-20 nm diameter Si nanowires, or for larger, surface roughened nanowires, κ is reduced by as much as two orders of magnitude relative to bulk crystalline Si and approaches κ_{min} [11-13]. The size-dependent reduction in κ occurs through the modification of scattering relaxation rates with preserved bulk-like phonon band structure. There have been proposals to use coherent phonon processes to modify the phonon band structure. For example, the use of periodic superlattice structures can influence the phonon group velocity [6]. However, scattering at the superlattice interfaces can partially or wholly mask such effects, meaning that incoherent scattering dominates the thermal properties of these systems as well [6,14-16]. Here we report that periodic, single crystal nanomesh structures, patterned at a scale where phonon band structure modifications can be observed, provide a route towards low-κ materials. We find that reductions in κ can be attributed to the nanomesh superstructure, rather than to classical size-effects. These results demonstrate

that thin-film nanoengineering provides an attractive approach for the design and fabrication of low-κ materials.

Fully suspended Si nanomesh films (Figure 1a, b) are fabricated starting from a <100> silicon-on-insulator (SOI) thin film. Electronic properties are chosen by boron diffusion doping of the initial thin film [18]. We fabricated three reference devices: (1) a Si thin film (TF); (2) an array of rectangular cross-section Si nanowires (NWA); and (3) a larger feature-size mesh that was defined by electron-beam lithography (EBM). The drawings and table of Figure 2a summarize the relevant dimensions, which were chosen to permit direct comparison of the structures. We present results on two similar nanomesh devices (NM1 and NM2), with the same periodicity and thin film thickness, and a small difference in the size of holes (see table of Figure 2a). The thickness T is nearly identical for all devices, and the nanowire cross-section areas are similar to the grid lines within the nanomesh films. The devices are fully suspended (Figure 1c) between two freestanding membranes (Figure 1d) that define the hot and the cold end for heat transport measurements. Temperature-dependent values of κ are determined by measuring the amount of heat generated by the resistive heater on one of the membranes and the temperature difference between the hot and the cold side [19]. For details on methods see Methods.

Figure 2d summarizes κ measurements on the two nanomesh devices and the reference structures. κ for the TF is about 17 W/m-K at room temperature. The decrease from bulk Si κ=148 W/m-K is consistent with published results [20], and originates from the thickness

of the film. The reduced cross-section of the nanowires that comprise the NWA leads to a further reduction to κ=3.5 W/m-K at room temperature, a result that is again consistent with published results from us and others [11,12]. To calculate κ of the nanomesh and EBM films, an approximation is applied in which the mesh structure is treated as two intersecting arrays of rectangular channels (Figure 2e; only one array of channels is highlighted). In nanomesh devices, these channels resemble the nanowires in the NWA; in the EBM they are wide ribbons. The heat transport is essentially diffusive; λ is an order of magnitude smaller than any of the dimensions in either the EBM or the nanomesh films [6]. As a result, only the channels running along the temperature gradient contribute significantly to the thermal conductance through the device; the perpendicular channels are effectively isothermal. In the EBM device, there is only a small increase in boundary scattering, compared to the TF, since Λ is predominantly defined by the similar thickness T in both devices. Accordingly, the EBM has comparable κ to the TF.

The equivalent channel approximation is likely less accurate for the nanomesh due to the round shape of the holes and the fact that the grid line width is comparable to the pitch. However, κ is only overestimated by this approximation, so that the room temperature measurement of 1.9 W/m-K only represents the upper limit for the actual κ. A reduction of at most 20% for the nanomesh films relative to the nanowires in the NWA would be expected if we consider only the small difference in size between the equivalent channels and the nanowires. Similarly, a significant increase in κ would be expected for the

nanomesh films relative to the NWA if we considered only the relative surface-to-volume ratios. The measured κ for the nanomesh films is, however, a factor of 2 smaller that that of the NWA.

Matthiessen's rule, $\tau^{-1} = \tau_{imp}^{-1} + \tau_U^{-1} + \tau_B^{-1}$, captures the dominant phonon scattering mechanisms. Here τ represents the total phonon relaxation time, and the subscripts imp, U, and B, respectively, refer to impurity scattering, Umklapp processes, and boundary scattering. We do not expect τ_U or τ_{imp} to vary between similarly doped devices (Figure 3). Surface roughness can influence on τ_B [13]. However, relative to the NWA, there is less or equal roughness present in the nanomesh films where fabrication processes can introduce roughness only to the walls of the holes, compared to the entire length of nanowire side surfaces. Plus, the surface-to-volume ratio of the nanomesh is actually significantly smaller (see table in Figure 2a). Thus, the reduction in κ for the nanomesh relative to the NWA is a consequence of the superstructure and the related modification of the bulk phonon dispersions.

We tentatively ascribe the observed drop in κ to a coherent effect in which holes play the role of Bragg reflectors – similar to the coherent phonon processes that are invoked in certain superlattice thin films. The periodicity of the superstructure – either the one introduced by the holes in the nanomeshes, or by the alternating thin-film layers in superlattices – modifies the phonon band structure by reducing the Brillouin zone (BZ). In superlattice structures, scattering of thermal phonons at the successive interfaces between

the composite layers can dominate over such coherent mechanisms. However, the superstructure of the nanomesh is imposed within a single crystalline piece of material where coherence may be readily maintained. In addition, the period of the superstructure is on the order of the mean-free-path of the thermal phonons (Λ>25 nm [21]), enabling the observation of wave-like effects that can emerge from the BZ reduction [22]. As a consequence, phonon bands are folded 62 times (superstructure period/Si lattice parameter) and considerably flattened compared to bulk Si bands. BZ reduction effects have been studied theoretically in superlattices [16,22-25], where the treatment is equivalent in the case of cross-plane transport, and all contributions to κ are considered to be spectral quantities: $\kappa(T) \propto \int_{\lambda} C_{v,\lambda}(T) v_{\lambda}^{2} \tau_{\lambda}(T) d\lambda$. Adopting these results, we expect no corrections at 300 K in the specific heat $C_{v,\lambda}$. The relaxation times τ_{λ} may change in periodic structures, but only for small periods and at low temperatures [23,24]. Therefore, we expect the most significant contribution to κ reduction to come from the decrease of the phonon group velocity v_{λ}, as a direct consequence of the flattening of phonon bands [25]. A complete phonon band structure modeling will be necessary to estimate the extent of κ reduction in our system, but in the case of superlattices factors of 2 – 10 have been found [25], which are consistent with the nanomesh results. Theoretical modeling of Si three-dimensional phononic crystals indicates that the phonon band flattening, such as observed in our nanomeshes, may lead to thermal conductivities below κ_{min} [26]. Highly voided materials, such as nanoporous Si, have been shown via molecular dynamics modeling to exhibit low κ [21,27,28], but the results published to date have largely focused only on boundary

scattering mechanisms. Theoretical simulations of very thin (2-3 nm diameter) Si nanowires have indicated that an amorphous surface layer can yield a temperature-independent and low value of κ [29]. However, our nanostructures are not in this regime, and we do not observe the surface-to-volume ratio effects on κ that would be expected from this mechanism.

Two highly doped nanomesh devices exhibited metallic-like electrical conductivity that followed the bulk trend [30] in both temperature dependence and magnitude (Fig 3). We are currently investigating structural and dimensional variations of these nanomesh films with the goal of more fully understanding the relationship between materials architecture and thermal conductivity.

Methods

The devices were prepared on silicon-on-insulator wafers (Soitec Inc.). The wafers were pre-doped by thermally diffusing a spin-on-dopant (Boron A; Filmtronics, Inc.) using rapid thermal annealing at 820°C for 3 minutes. The wafer sheet resistance indicated a doping concentration of $2x10^{19}$ cm^{-3}. All devices were fabricated by transferring a device-defining pattern from a Pt mask into the Si epilayer (Figure 1a) by CF_4/He reactive ion etching. The TF and EBM devices were patterned by electron-beam lithography, and NWA nanowires and NM nanomeshes by the SNAP technique [17] (Figure 1a). The precise thickness T of the devices is determined by measuring the Si epilayer thickness with an atomic force

microscope. The other size parameters listed in Figure 2a were determined from scanning electron microscope images.

We have developed a fabrication protocol that allows thermal conductivity measurements on fully suspended (i.e. without oxide support) nanowires and nanomeshes, and applied it to nanowires as thin as 20x28 nm^2. The measurement platform (Figure 1d) is suspended over the Si handle layer (black in Figure 1a) and consists of two symmetric sets of membranes with serpentine Pt heaters/temperature sensors, and beams with heater/sensor leads. The active device region is fully suspended between the membranes. The platform consists of layers that reinforce the structure and provide protection during the gas-phase suspension of the device. The bottom layer is the same Si epilayer as in the device region. Such contact with the device, referred to as the monolithic contact, reduces considerably the thermal resistance between the membranes and the device, and enables accurate measurements of thermal conductivity. For structural integrity, a 250 nm low-stress silicon-nitride film is deposited by plasma enhanced chemical vapor deposition (PECVD by STS Multiplex). Then, a 20 nm Ti adhesion layer and 60 nm thick Pt heaters/sensors and leads are deposited on top of silicon-nitride by electron-beam assisted evaporation (CHA; Semicore). A 200 nm capping layer of poly(monochloro-*p*-xylylene), or parylene-C (SCS parylene deposition system), completes the layered structure. The platform was defined by e-beam lithography and Al metallization, and then transferred by oxygen plasma etching in order to remove parylene, and CF_4 plasma to remove silicon-nitride and buried oxide. The device region was protected during etching by a 100 nm layer of Al, which was deposited directly on top of the device and underneath the silicon-nitride and parylene layers.

Afterwards, All was removed by a phosphoric acid based etchant. At this point, the device and the measurement platform are defined on top of the Si handle layer. The device is released in two gas-phase etching steps. First, a 6% polymethyl methacrylate (PMMA 950) e-beam resist is spun on the device to protect the Si device, and two openings on either side of the membranes were patterned by e-beam lithography. Then, an isotropic XeF_2 etch (custom pulsed etching system) was applied in order to release the platform and the device from the Si handle layer. The overall etch time is about 2 minutes at 2000 mTorr and at room temperature. The PMMA layer is then removed using an acetone bath and supercritical drying (Automegasamdri-915B, Tousimis). In the final step, the device is released from the remaining buried oxide layer (blue in Figure 1a). A home-built HF vapor etcher equipped with a wafer heating stage was designed for homogeneous and stiction-free oxide removal at elevated temperatures. The etching process is performed in vapors of the mixture of HF (49%) and isopropyl alcohol with the wafer heated to a temperature of ~80°C. A complete removal of 125 nm buried oxide is achieved in ~30 minutes. The platform was sufficiently protected from HF damage by the top parylene layer and the bottom Si epilayer. The sample is wire-bonded to a chip, and promptly inserted into the high-vacuum cryostat (VPF-475, Janis research). The thermal conductance measurement procedure and the detailed error analysis are described in [19]. Electrical conductivity was measured on separate unsuspended devices with e-beam lithography defined Pt four-point contacts.

Measurement Procedure

Li Shi et al. have detailed measurement and analysis procedures in their report of thermal and thermoelectric property measurements of one-dimensional nanostructures on suspended device platforms [19]. We adapted their platform and procedures to enable measurements of thermal conductance on monolithically-fabricated, fully-suspended devices on SOI substrates. We refer the reader to their work for details on the procedures. In the following, we briefly summarize our adaptation.

In our measurement platform, the sample is bridged between a pair of suspended membrane "islands", as previously described in the **Device Fabrication** section. Each membrane contains a set of serpentine Pt lines that serves as a PRT and is suspended by four long (~70 μm) beams along which the electrical connections are routed. One of the PRTs also serves as a heater and measures the hot side temperature. The other measures the cold side temperature. (Figure 5)

The cryostat is ramped to a set temperature T_0 at a rate of <3 K min^{-1} to minimize thermal stresses on the suspended structure. After the cryostat temperature has stabilized, a current source (Keithley 6221) is used to supply a small sinusoidal current $i_{ac,h}$ ~ 250 nA at frequency f_h > 700 Hz on top of a dc current I to the heating PRT. The differential resistances R_h (resistance of the serpentine element) and R_L (resistance of the lead) of the heating PRT are measured simultaneously with a pair of lock-in amplifiers (Stanford Research Systems SRS830). Another SRS830 lock-in is used to source a sinusoidal current $i_{ac,s}$ ~ 250 nA at frequency f_s through a high-precision 10 MΩ metal film resistor (Vishay

Sfernice CNS020) to the sensing PRT, while measuring the differential resistance R_s. These measurements are repeated for the entire set of dc currents before the cryostat is ramped to another set temperature, upon which the measurement cycle repeats.

At the conclusion of the experiment, the set of $R_s(I=0)$ and $R_h(I=0)$ acquired at various temperatures T_0 is fitted using linear least squares regression to obtain $dR_s(I=0)/dT$ and $dR_h(I=0)/dT$. The temperature rise of the heating and sensing PRTs are then given as

$$\Delta T_h = \frac{\Delta R_h(I)}{\frac{dR_h(I=0)}{dT}};$$

$$\Delta T_s = \frac{\Delta R_s(I)}{\frac{dR_s(I=0)}{dT}};$$

The Joule heat developed in the heating PRT and its leads are $Q_h = I^2R_h$ and $2Q_L = 2I^2R_L$ and we can thus calculate the beam and sample thermal conductances.

$$G_b = \frac{Q_h + Q_L}{\Delta T_h + \Delta T_s}$$

$$G_s = G_b \frac{\Delta T_s}{\Delta T_h - \Delta T_s}$$

Uncertainty of the Thermal Conductivity δ_κ

The thermal conductivity is obtained from the measured thermal conductance of each sample and the geometrical factor ($\kappa = G_s \times$ geometrical factor), i.e. the cross-section and length of the equivalent channels for the NM and EBL NM; and the exact cross section and length of the NWA and TF samples. The geometrical factor (G.F.) for the NWA, EBL NM,

NM can be described by G.F. = L/(n×T×W) where L represents the length of the system across the measurement platform, n is the number of wires or equivalent channels, T is the thickness of the silicon epilayer, and W is the width of a nanowire or equivalent channel (Figure 2a). The number of nanowires can be calculated by dividing the total width of the sample W_0, by the pitch of the wire or the equivalent channel array P. Thus, G.F = (P×L)/(W_0×T×W). Therefore, the uncertainty of the thermal conductivity can be evaluated by

$$\frac{\delta_\kappa}{\kappa} = \sqrt{\left(\frac{\delta G_s}{G_s}\right)^2 + \left(\frac{\delta P}{P}\right)^2 + \left(\frac{\delta L}{L}\right)^2 + \left(\frac{\delta W_0}{W_0}\right)^2 + \left(\frac{\delta T}{T}\right)^2 + \left(\frac{\delta W}{W}\right)^2}$$

The uncertainty of the measured G_s is determined as previously described.

For the NM, $P = 34.6 \pm 1.9$ nm, $L = 7.31 \pm 0.07$ μm, $W_0 = 7.28 \pm 0.04$ μm, $W = 22.81 \pm 2.33$ nm as determined by SEM. $T = 22.3 \pm 1.3$ nm based on AFM measurements at five different positions of the SOI wafer. $G_s = 26.32 \pm 0.51$ nW/K at 250 K. As a result, $\kappa = 1.80 \pm 0.23$ W/m-K.

For the NWA, $P = 34.4 \pm 1.6$ nm, $L = 8.45 \pm 0.13$ μm, $W_0 = 7.71 \pm 0.21$ μm, $W = 28.25 \pm 1.46$ nm, $T = 20.1 \pm 1.2$ nm, $G_s = 56.81 \pm 1.14$ nW/K at 250 K giving $\kappa = 3.40 \pm 0.33$ W/m-K.

Thermopower

The thermopwer or the Seebeck coefficient (S) is obtained based on previously reported methodology (Chapter 2; [10]). All the devices under investigation are p-type boron doped. As can be seen from Figure 6, bulk-like thermopower [31] is observed for all the nanomesh devices. For NM devices with doping concentration lower than $1\times10^{19}\,cm^{-3}$, the Seebeck coefficient peaks at lower temperature ~ 150K and can possibly be attributed to phonon-drag effect.

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Figure 1A

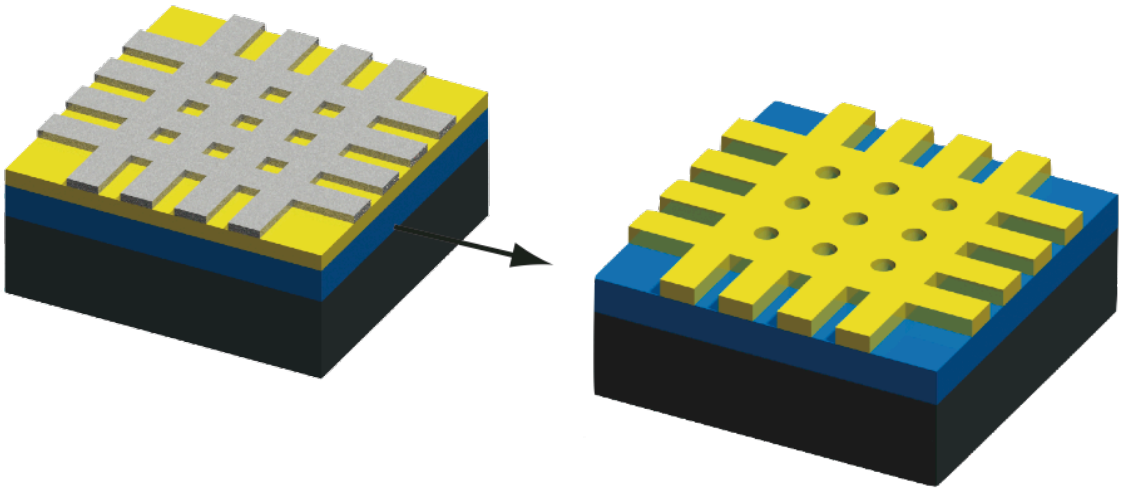


Figure 1B

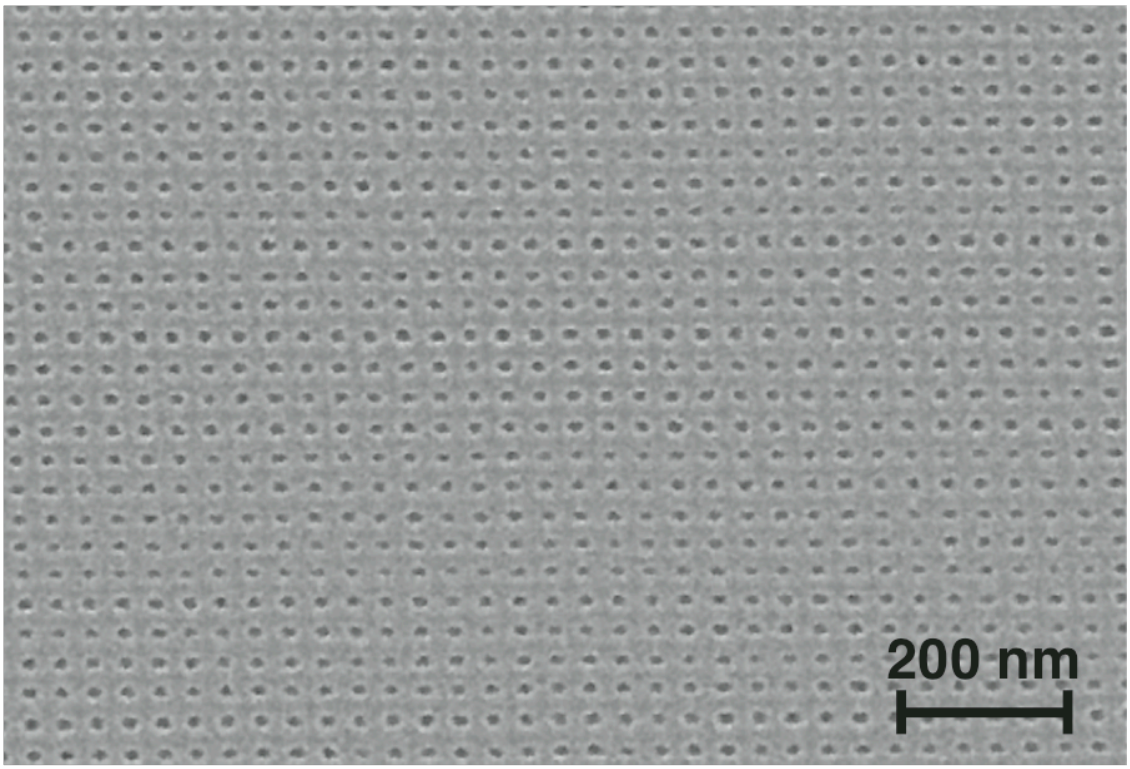


Figure 1C

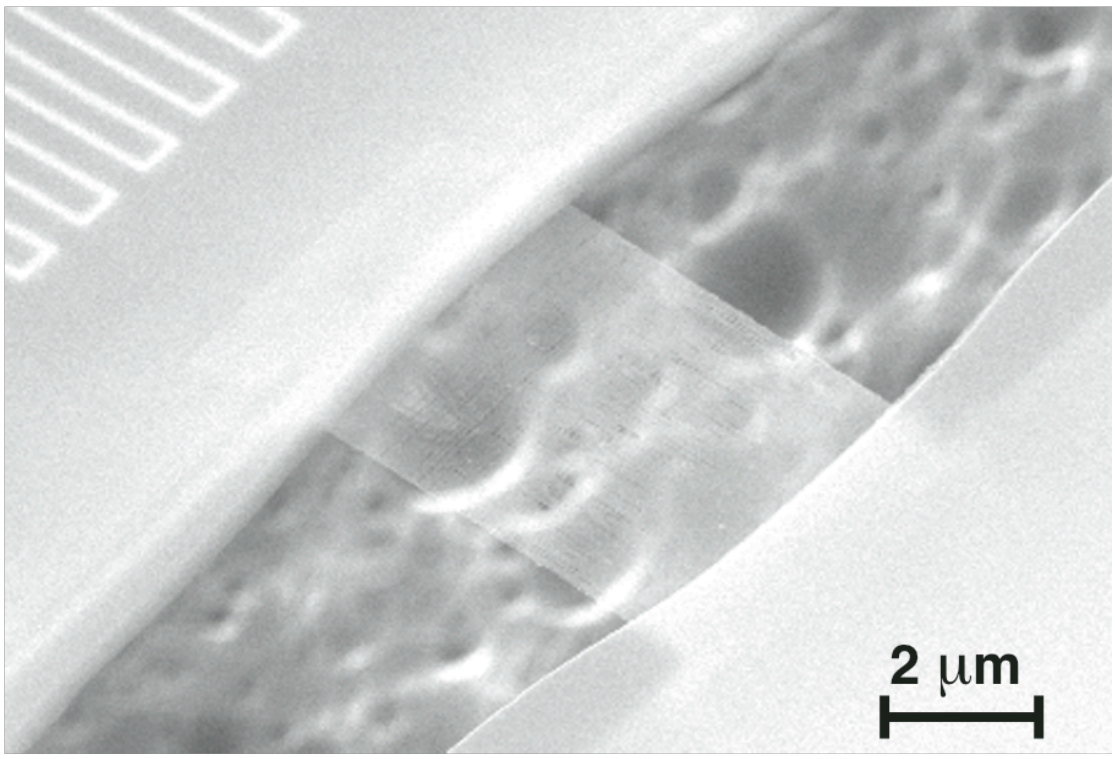


Figure 1D

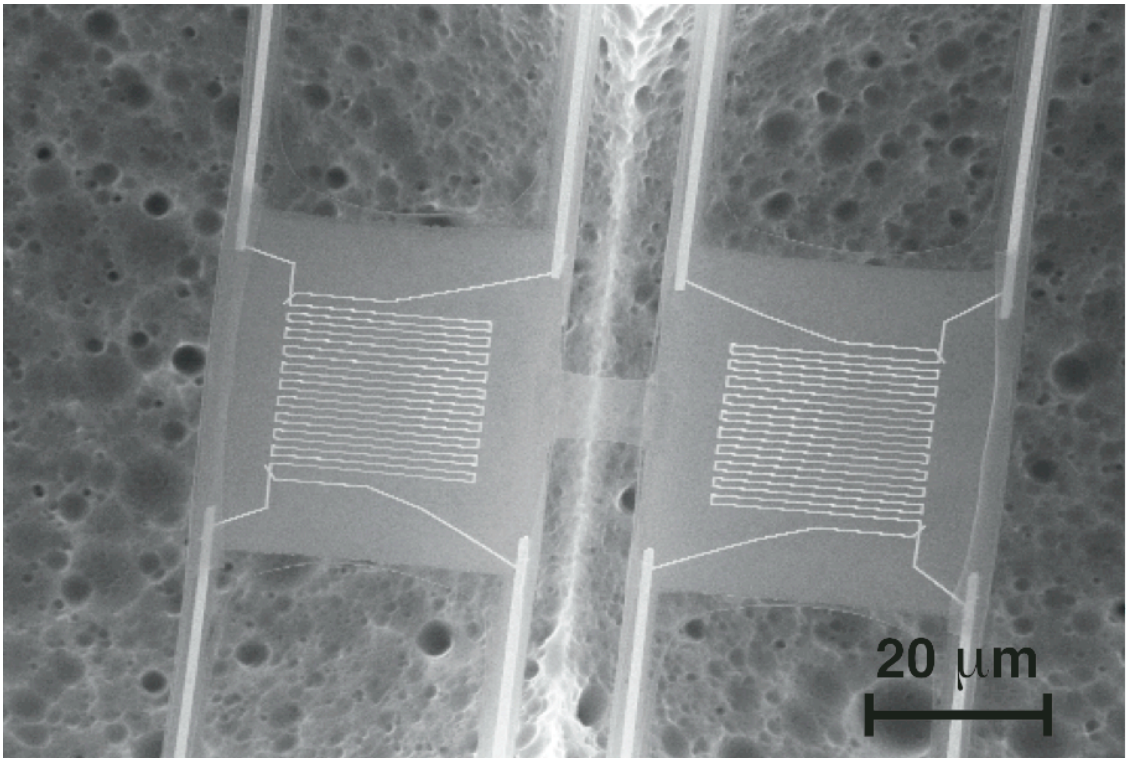
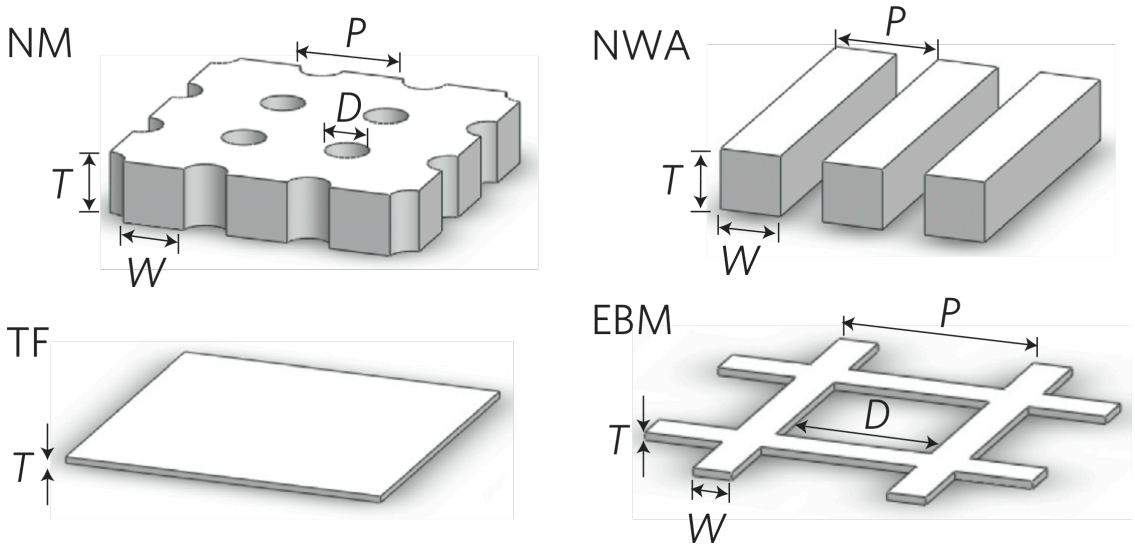


Figure 2A



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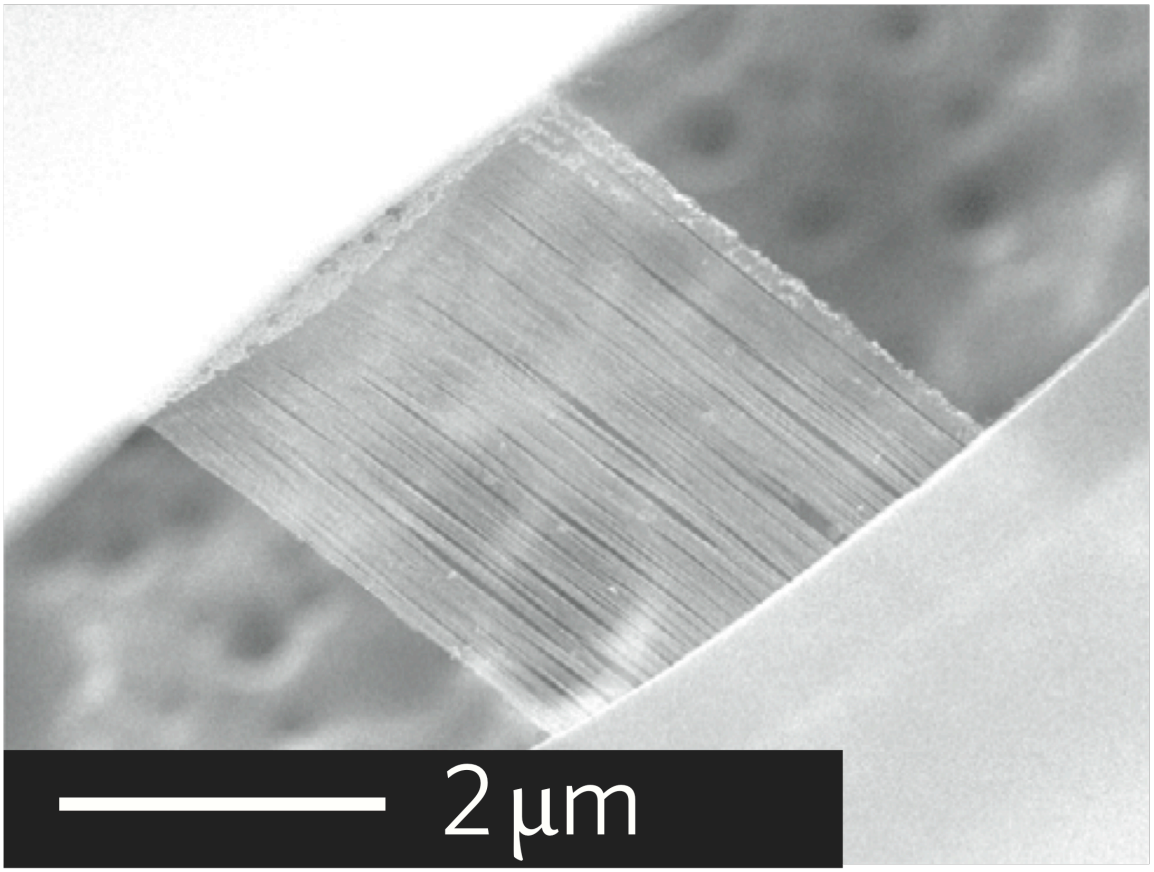

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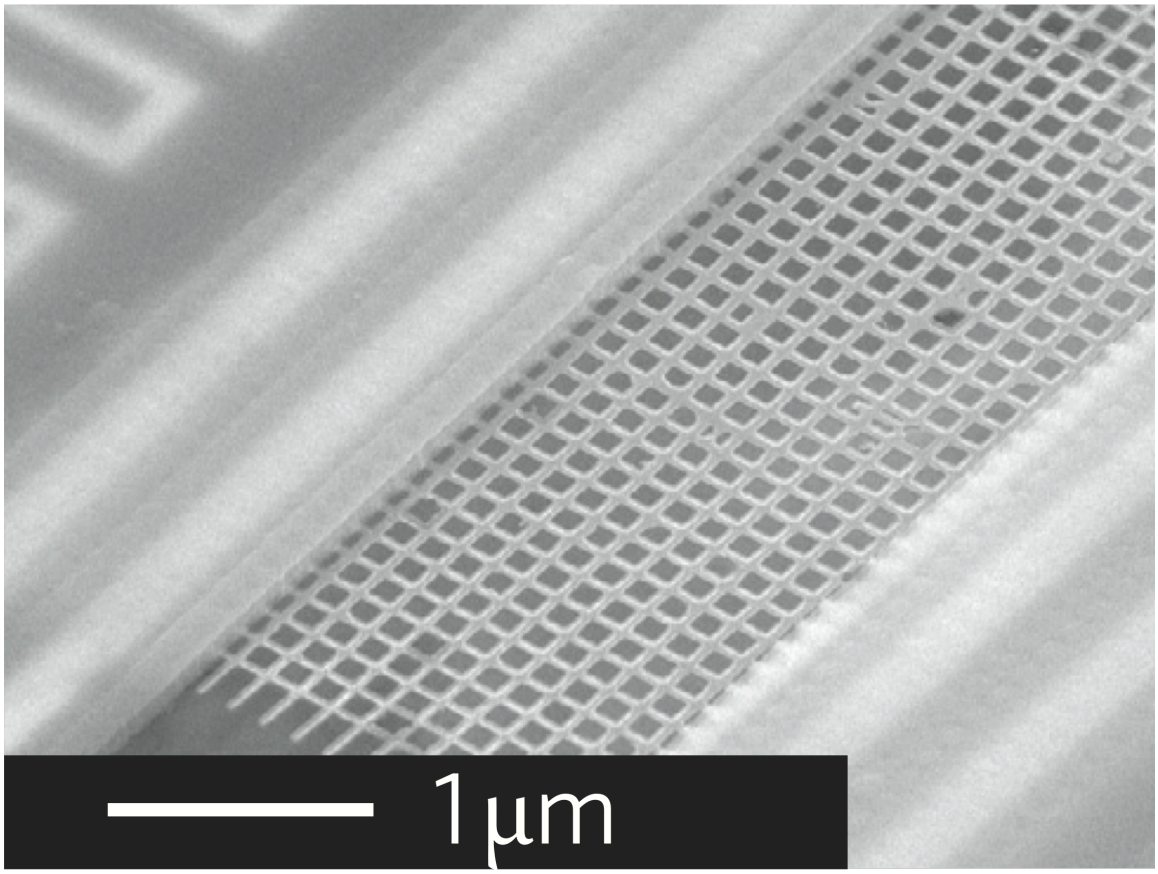

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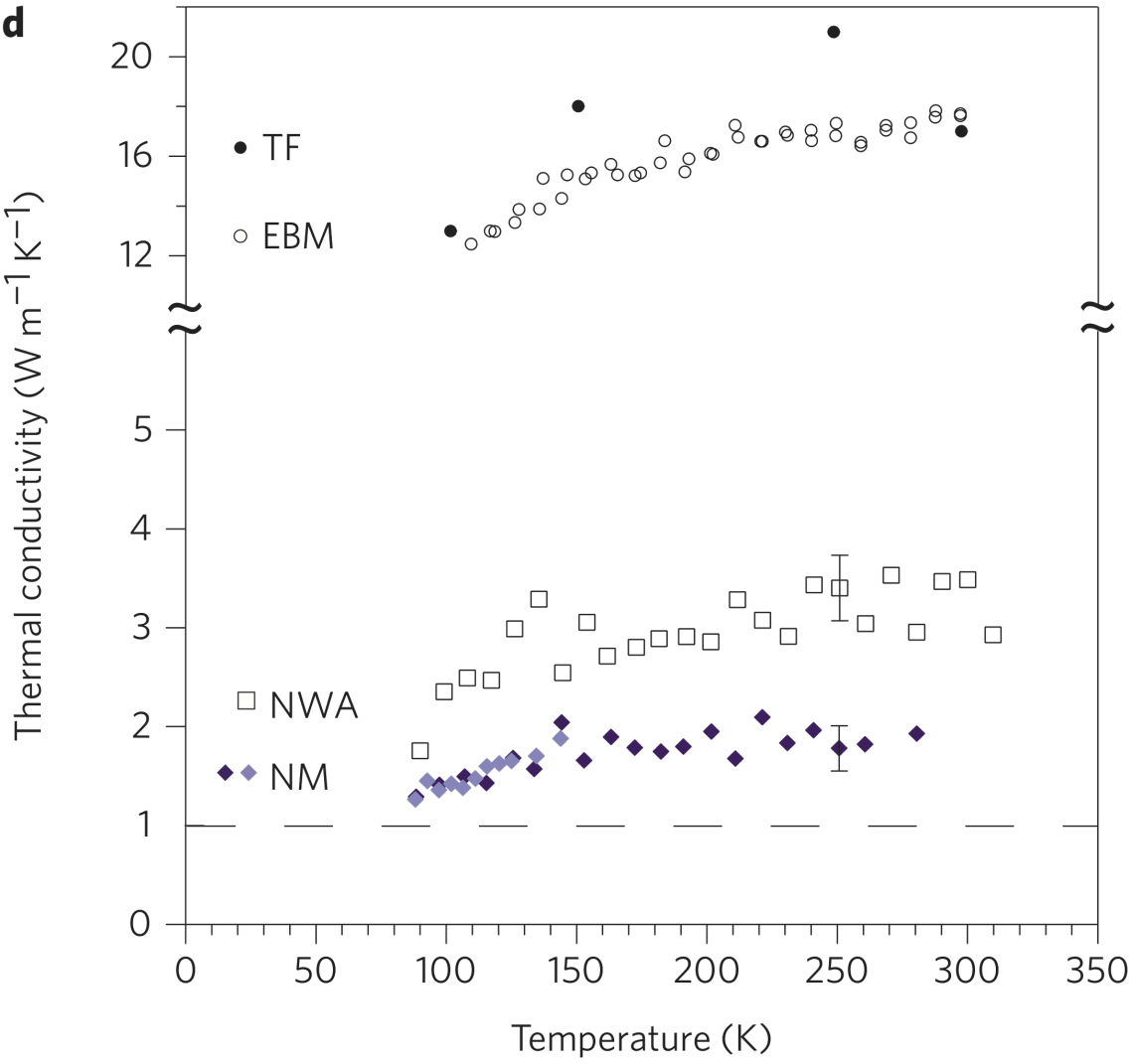
d
Thermal conductivity (W m^{-1} K^{-1})
20
16
12
5
4
3
2
1
0
TF
EBM
NWA
NM
0
50
100
150
200
250
300
350
Temperature (K)

Figure 2E

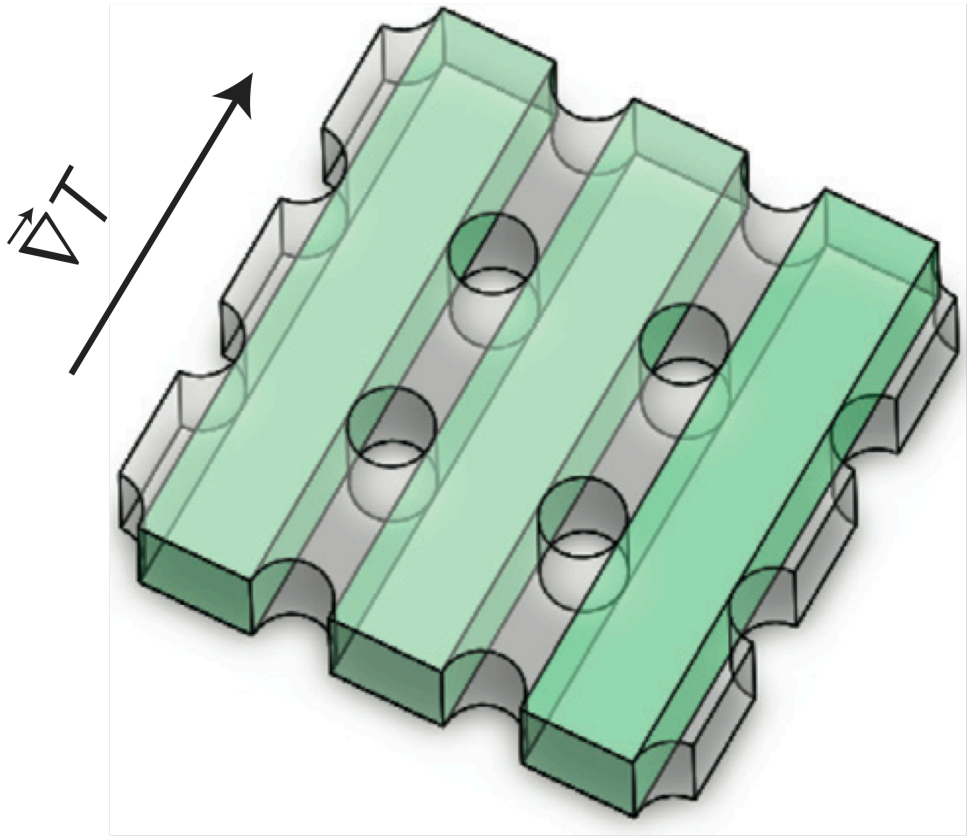

Figure 3

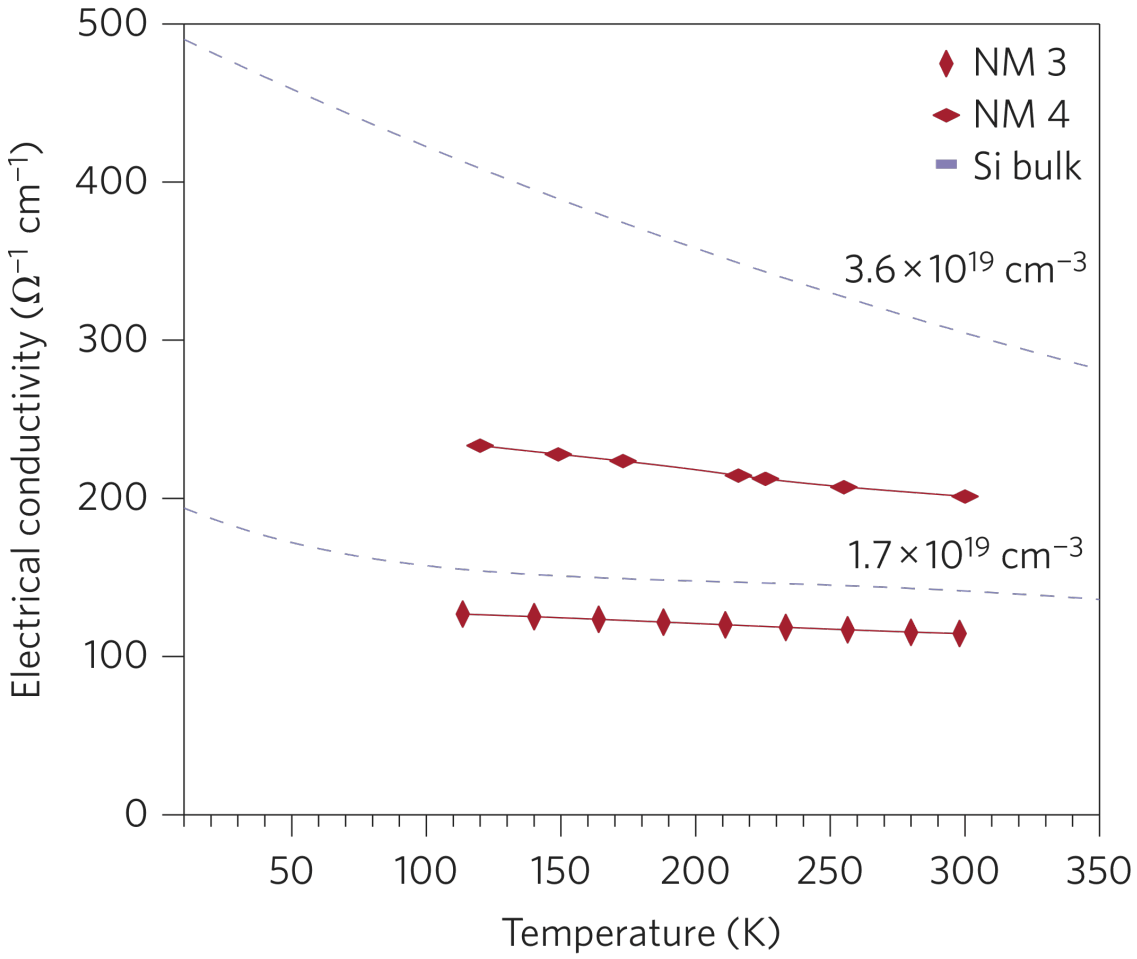
NM 3
NM 4
Si bulk
3.6×10^19 cm^−3
1.7×10^19 cm^−3
Electrical conductivity (Ω^−1 cm^−1)
Temperature (K)
500
400
300
200
100
0
50
100
150
200
250
300
350

Figure 4

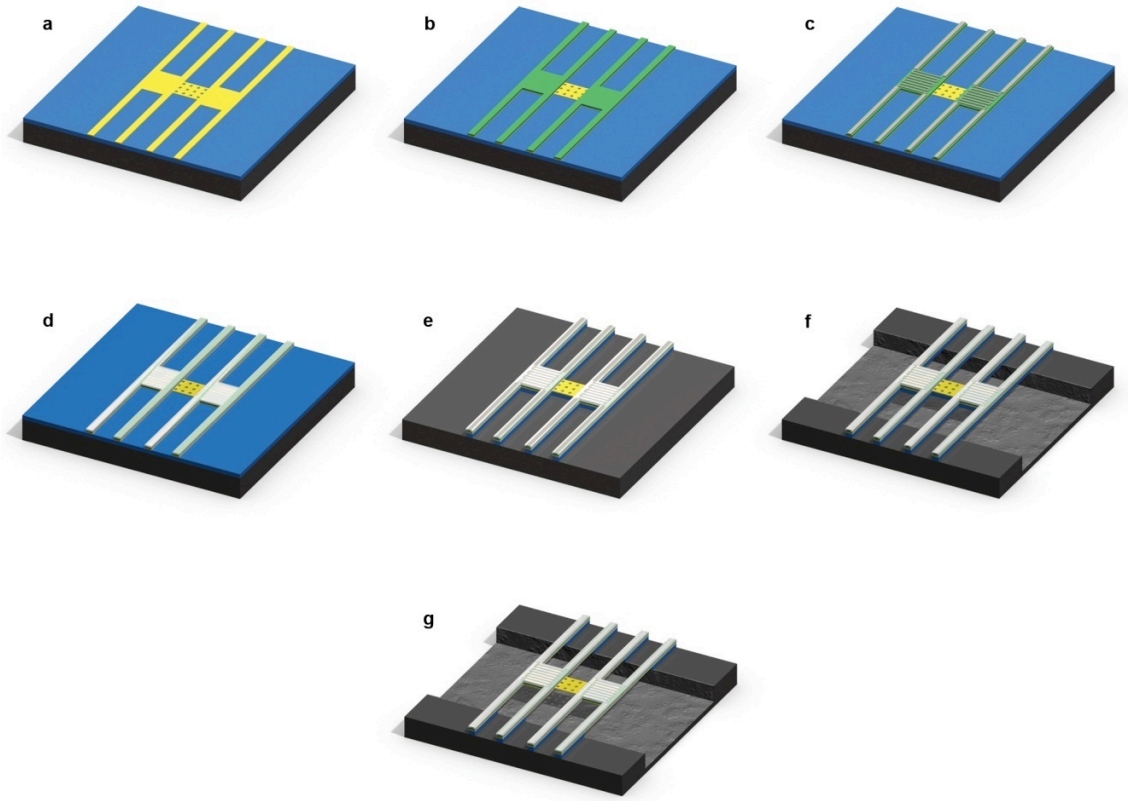

Figure 5

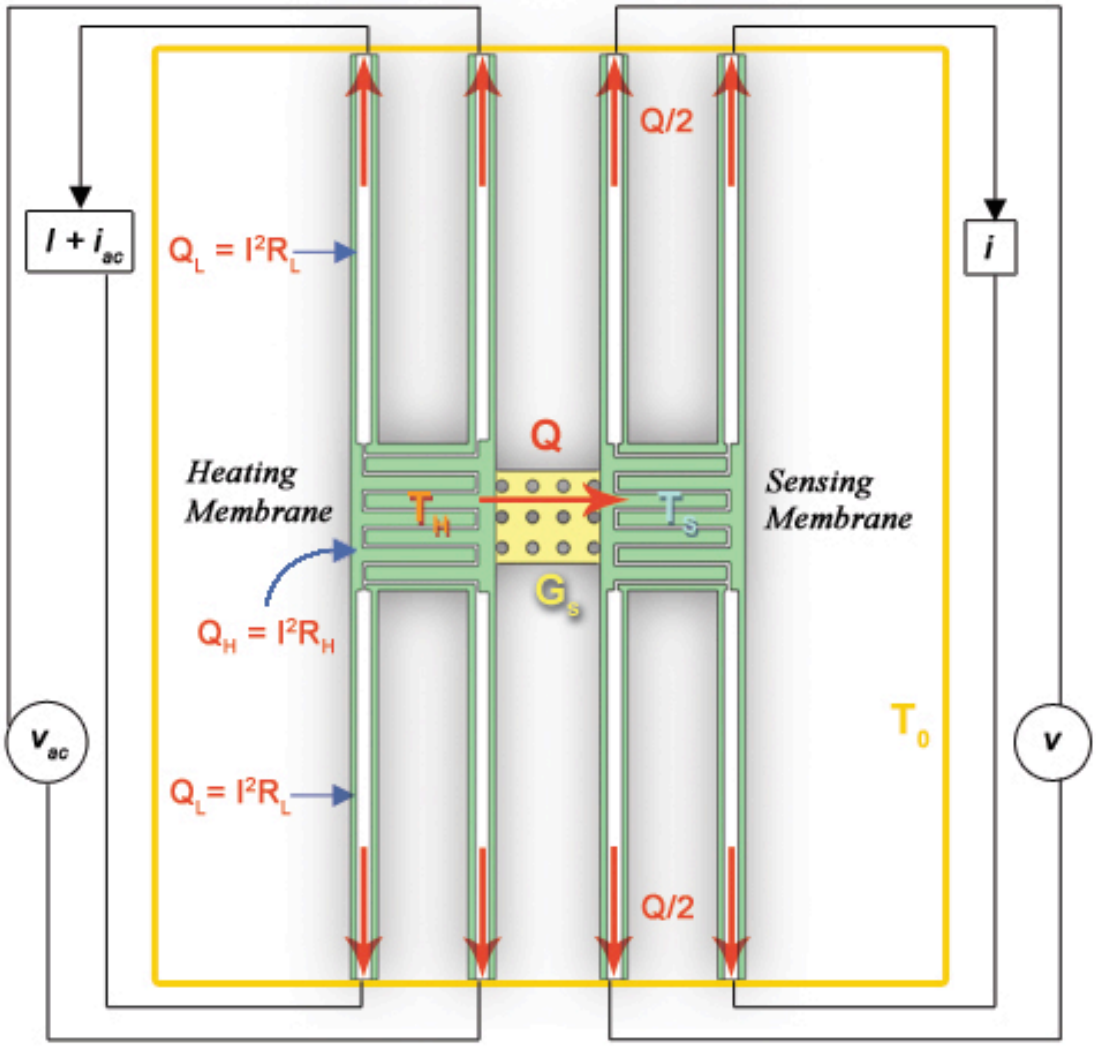
I + i_ac
Q_L = I²R_L
Q/2
i
Q
Heating Membrane
T_H
T_S
Sensing Membrane
G_S
Q_H = I²R_H
T_0
V_ac
V
Q_L = I²R_L
Q/2

Figure 6

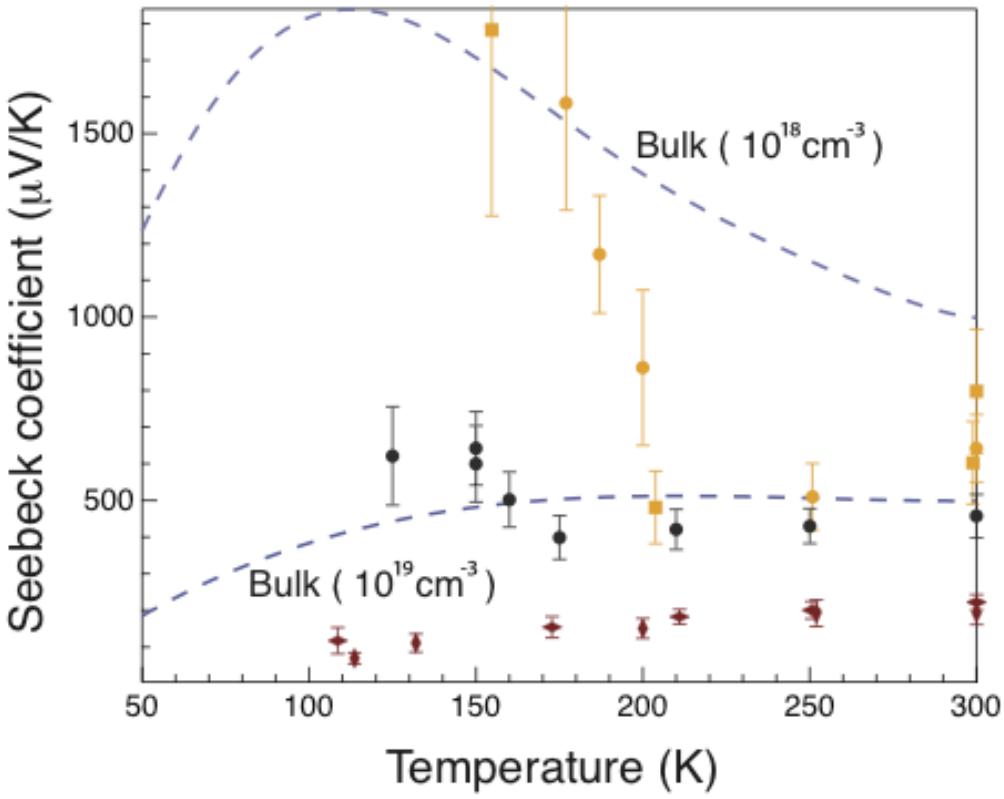
Seebeck coefficient (μV/K)
1500
1000
500
50
100
150
200
250
300
Temperature (K)
Bulk (10^18 cm^-3)
Bulk (10^19 cm^-3)

Table 1

Table 1 | Dimensions, including surface-to-volume ratios, of the two nanomesh films (NM1 and NM2) and three reference systems (TF, EBM and NWA).

	T (nm)	*W* (nm)	*D* (nm)	*P* (nm)	Surface/Volume (nm^{-1})
TF	25	-	-	-	0.08
EBM	22	115	270	385	0.07
NWA	20	28	-	-	0.17
NM 1	22	23	11	34	0.12
NM 2	22	18	16	34	0.14

Dimensions are as shown in Fig. 2a.

Figure Captions

Figure 1 Silicon nanomesh device

a. Silicon nanomesh films are fabricated on silicon-on-insulator wafers by transferring the pattern of two intersecting Pt nanowire arrays (grey) into the Si epilayer (yellow). The intersecting Pt nanowire arrays are created using the superlattice nanowire pattern transfer (SNAP) technique, which translates the layer spacings within a GaAs/$Al_xGa_{(1-x)}As$ superlattice into the width and pitch of a nanowire array [17]. Two successive SNAP processes are needed to make an intersecting array. In the image, blue layer represents the buried silicon-dioxide, and black is the Si handle layer **b.** Scanning electron micrograph of a part of a Si nanomesh film, showing a uniform square-lattice matrix of cylindrical holes (scale bar 200 nm). The nanomesh films can be up to 10 × 10 μm^2 in area. **c.** Scanning electron micrograph of a fully released, transparent nanomesh film suspended between two membranes (scale bar 2 μm). **d.** Lower magnification micrograph showing suspended membranes with Pt heaters/sensors together with the suspended beams carrying the leads for thermal conductivity measurements (scale bar 20 μm).

Figure 2 Device geometries and thermal conductivity measurements.

a. The geometry and dimensions, including surface-to-volume ratios, of the nanomesh films and three reference systems. **b.** SEM image of suspended nanowires in the NWA device, and **c.** the suspended EBM device. **d.** Comparative plot of thermal conductivity measurements on two different nanomesh devices (diamonds) and the three reference

devices. The TF and EBM devices have similar thermal conductivities as a result of their similar film thickness. The NWA nanowires have lower thermal conductivity reflecting their larger surface-to-volume ratio compared to TF and EBM (note the discontinuity in the y-axis). The nanomesh devices, though with significantly lower surface-to-volume ratio compared to NWA, exhibit a factor of two lower thermal conductivity. The error bars on the selected points are representative for the measurements (see Supplemental information for detailed error analysis) **e.** In order to calculate thermal conductivity from measured thermal conductance, the heat is assumed to flow through equivalent, green highlighted channels. The thermal gradient does not have a component perpendicular to these channels. The actual conduction cross-section can only be larger if we account for the interconnecting parts between channels. This approximation gives the upper bound value for the thermal conductivity in nanomeshes.

Figure 3 Electrical conductivity measurements.

Four-point measurements of the electrical conductivity (red diamonds) of two nanomesh films, both p-type doped with boron to nominal concentration $2.0 \times 10^{19} cm^{-3}$. Small spatial variations in doping levels of Si epilayers are standard with spin-cast doping, and this is reflected in different electrical conductivities of the two nominally equally doped devices. Electrical measurements are performed on separate but identically processed devices as the ones used for thermal conductivity measurements. Both nanomesh devices exhibit values that are comparable to bulk Si thin film (dashed lines; adopted from [30]). The results

imply that the nanomesh films are relatively defect-free and that bulk Si electrical properties are preserved in the high-doping range.

Figure 4. Device fabrication.

The scale of the device is exaggerated from reality for better visualiztion. (a) Silicon nanomesh with monolithically-defined silicon device platform. (Yellow). (b) Device platform with silicon-nitride film as the structural backbone. (c) Ti/Pt heater/sensor defined on to the platform. (d) Parylene C conformally deposited on to the platform. (e) Buried oxide removed by RIE1 process. (f) Si handle layer etched by XeF_2. (g) Device fully suspended by buried oxide removal with HF vapor.

Figure 5. **Schematic diagram for the thermal conductivity measurement platform**.

T_H and T_S represent the temperatures of the heating and sensing membranes respectively. T_0 is the substrate temperature. Q_H, Q_L represents the amount of heat generated by the heater and the lead, respectively. Q is the amount of heat transported through the sample and G_s is the thermal conductance of the sample.

Figure 6. Seebeck coefficient measurements.

Thermopower measurements on multiple p-type NM devices with different carrier concentrations are compared to bulk Si thermopower in the oping impurity concentration range from 10^{18} to 10^{19} cm^{-3}. Red symbols represent two sets of data on devices doped at $2x10^{19}$ cm^{-3} (twice that of the dashed line representing bulk Si doped at 10^{19}); black symbols $4x10^{18}$ cm^{-3}; and yellow symbols two sets of data at $2x10^{18}$ cm^{-3}.