

Chapter 2

HEAT TRANSPORT IN SILICON NANOWIRES AND THE SILICON NANOWIRE THERMOELECTRICS

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The focus of this chapter is on the experimental results of the thermal conductivity of silicon nanowires and the thermoelectric performance of silicon nanowires. A quick overview of the thermoelectric phenomenon is given in the beginning of the chapter to address the critical role that semiconductors with ultra-low thermal conductivities play in this field.

2.1 Introduction

It's been over a century since the first discovery of thermoelectricity by Seebeck [1] in the 1820s. Thermoelectric materials convert temperature gradient into electrical power and vice versa. Moreover, thermoelectric devices are solid-state particle exchange devices, which require neither moving parts nor the use of environmentally harmful chemicals. However, the thermoelectric materials find only niche applications mainly because of their low efficiency. Before the year 2000, the most efficient thermoelectric material the Be_2Te_3 and its alloys with Sb or Se [2], with an efficiency just 10 percent of the Carnot engine operating at room temperature. The most efficient thermoelectric material researchers have found to date is the nanostructured thin-film superlattices of Be_2Te_3 and Sb_2Te_3 [3].

The efficiency of the thermoelectric materials is commonly described by the thermoelectric dimensionless figure-of-merit [4]

$$ZT = \frac{S^2 \sigma T}{\kappa}. \quad (2.1)$$

S is the thermopower (or Seebeck coefficient) and has the unit volts/Kelvin; σ is the electrical conductivity and κ represents the thermal conductivity of the material. ZT is related to power efficiency by equation 2.2. When $ZT \rightarrow \infty$, the efficiency approaches the Carnot limit.

$$\eta = \frac{\Delta T}{T_{Hot}} \frac{\sqrt{1+ZT} - 1}{\sqrt{1+ZT} + \frac{T_{Cold}}{T_{Hot}}} . \text{(2.2)}$$

It is obvious from equation 2.1 that a high ZT thermoelectrics is capable of generating large electromotive force from a small temperature gradient, i.e., large Seebeck coefficient; in addition, a good thermoelectrics should at the same time be a good electrical conductor in order to minimize the heat loss by Joule heat. In terms of heat transport, a good thermoelectric material is a good thermal insulator, i.e., the thermal conductivity should be low so that the temperature gradient can be sustained. However, materials that meet all three of the criteria are yet to be found. The reason lies in the fact that these three material parameters are inter-correlated. Modifying one of the parameters would result in adverse effects on the other two. For instance, increasing charge carrier concentration could readily enhance the electrical conductivity of semiconductors. However, these carriers not only carry charges but also act as heat transporters. As the number of charge carriers increases, the thermal conductivity of the material system is also raised. Wiedemann-Franz law describes the ratio of the electrical conductivity and the thermal conductivity contributed by charge carriers with a constant consisting of the Lorenz number (L) and temperature (T) (equation 2.3). Such adverse effect is particularly discernible in most metals and highly doped semiconductors material systems, where the dominant current and heat transport medium is the charge carriers [5].

$$\sigma / \kappa_e = LT . \text{(2.3)}$$

In semiconductors, lattice vibrations or phonons are the dominant contributors to heat transport [6-8], indicating that interfering with the phonon dynamic could effectively lead to a suppressed thermal conductivity. Debye suggested that, in the gas-kinetic model, the heat transport in an elastic medium travels with the sound velocity v and mean-free-path ℓ :

$$\kappa = \frac{1}{3} C_v v \ell . \quad (2.4)$$

Nanostructures with one or more dimensions smaller or comparable to the phonon mean-free path are expected to greatly influence the phonon dynamics through boundary scattering [2]. In addition, phonon mean-free path ℓ_{ph} , in general, has a characteristic length scale much larger than that of the charge carriers ℓ_e . Take single crystalline silicon for example, $\ell_{ph} \sim 300 \text{ nm} \gg \ell_e \sim 1\text{-}2 \text{ nm}$ [9]. Such length scale difference permits nanostructuring a strategy to reduce thermal conductivity without modifying the electronic transport properties. In other words, it provides an efficient route to decouple the thermal conductivity and the thermoelectric power factor ($S^2\sigma$).

In this chapter, thermal conductivities of silicon nanowires with crosssections 10 nm x 20 nm and 20 nm x 20 nm as well as their thermoelectric power factors, are investigated experimentally. Silicon nanowires are found to exhibit ZT as high as 1.2 at 200K. On several nanowire samples with 10 nm x 20 nm cross-section, thermal conductivity lower than the amorphous limit is also observed. The fabrication methods, measurement methodology, and results are discussed in the following sections followed, by a short

review of the recent theoretical studies on the thermal transport mechanism in silicon nanowires.

2.2 Device Fabrication

The silicon nanowires are fabricated by the superlattice nanowire pattern transfer technique (SNAP [10,11], Figure 1). In short, the process starts from a GaAs/AlGaAs superlattice, the GaAs layers are then selectively etched back by $\text{NH}_4\text{OH}/\text{H}_2\text{O}_2$ water solution ($V_{98\%\text{NH}_4\text{OH}}:V_{30\%\text{H}_2\text{O}_2}:V_{\text{H}_2\text{O}} = 1:20:300$) resulting in a comb-like structure. Next, Pt metal is deposited onto this structure by electron beam-assisted physical vapor deposition (PVD). Separately, silicon-on-insulator (SOI) wafers from which the nanowires are made were prepared. The SOI is pre-oxidized by thermal oxidation and thinned down by the removal of the oxide layer with buffered oxide etchant (BOE; 49% NH_4F , 51% HF). The starting SOI thickness and the thermal oxidation process (dry oxidation at 1000 °C) defines the final SOI thickness. The SOI wafers are either boron-doped or phosphorus-doped by thermally driven diffusion doping process. The doping concentration is controlled by the annealing temperature and confirmed by four-point sheet resistance measurement. Typically, the wafer can be boron-doped to $5 \times 10^{19} \text{ cm}^{-3}$ with the annealing temperature of 850 °C and phosphorus-doped to $3 \times 10^{19} \text{ cm}^{-3}$ at 950 °C. The superlattice master is then dropped on the epoxy-coated (by spin coating) p-type or n-type SOI, followed by curing the epoxy at 180 °C for 45 minutes. The superlattice master is then released by the phosphoric/ H_2O_2 etching solution. The platinum metal wire array is left on top of the wafer and serves as the etching

mask after the superlattice removal. Directional CF_4 plasma dry etching is utilized to transfer the pattern into the SOI. The plasma etching is performed on the Plasmtherm SLR 710 reactive ion etcher. A CF_4/He gas mixture with a flow rate of 20 sccm/30 sccm is introduced into the chamber. The plasma is ignited at 40 MHz radiofrequency with a power of 40 watts. The gas pressure is controlled at 10 mtorr. The DC bias is about 80 volts. The etching process is monitored by endpoint detection with the application of laser interferometry. Lastly, the platinum is removed by aqua regia solution (HNO_3/HCl). The width and the spacing of the resulting wires are pre-determined by the thickness of the AlGaAs layer and the GaAs layer, respectively. Figure 2 shows the highly uniform high-density silicon nanowires made by the SANP technique.

After the wires are made, heaters and contact electrodes are defined by e-beam lithography with a 3% polymeric e-beam resist PMMA/chlorobenzene solution. Ti (20 nm)/Pt (180 nm) and Ti (20 nm)/Pt (100 nm) are deposited by e-beam PVD for the heaters and electrodes, respectively. For the purpose of measuring the thermal conductivity of the wires, the device is further suspended over an 800 mm x 800 mm hole. Briefly, a 1600 mm² area of oxide was removed by CF_4 plasma with the device active region protected by 6% PMMA. Next, XeF_2 gas was introduced to isotropically etch the underlying silicon handle layer. See Figure 3.

2.3 Measurement

2.3.1 Electrical conductivity/resistivity measurement

Electrical conductivities of the nanowires are measured by a four-point probe setup. Briefly, electrical current is sourced (Keithley 2400 source meter) through the two outer electrodes placed at the two ends of the nanowire array. The voltage drop is obtained by a voltage meter (Keithley 6500 nanovolt meter) via another inner pair of electrodes (see also Figure 3). The resistance of the nanowire array is obtained by the slope of the linear regression fit to the I-V curve. Atomic force microscope (AFM) and scanning electron microscope (SEM) measurements provide the geometric information needed for the resistivity calculation. Typically, the resistivity is about $7 \times 10^{-4} \Omega\text{-cm}$ for highly doped nanowires. Extra care is taken in order to achieve a good ohmic contact before the resistivity measurement. First, monolithic contacts are designed to increase the contact area. Secondly, the devices are briefly dipped into dilute BOE ($V_{\text{BOE}}:V_{\text{H}_2\text{O}} = 1:100$) for a couple of seconds to remove the native oxide right before metal deposition. After metallization, the devices are subject to forming gas ($\text{N}_2/\text{H}_2 = 95/5$) anneal at $475 \text{ }^\circ\text{C}$ for 5 minutes to anneal the contact as well as hydrogen terminate the silicon surface.

2.3.2 Seebeck coefficient measurement

Seebeck coefficient measurements require accurate detection of the voltage drop, ΔV , and the temperature difference, ΔT , across the nanowire arrays when the heater is turned on. ΔV could be easily obtained via the two inner electrodes and a voltage meter. However, to determine ΔT is less straightforward. Two platinum resistive thermometers (same as the two electrodes for I-V measurements) are used for this purpose. Specifically, the resistances of the thermometers were measured as a function of heater power. From the

linear regression, we get the ratio $\Delta R/\Delta W$. Another set of resistance measurements is carried out as a function of the cryostat temperature, yielding the ratio $\Delta R/\Delta T$. The temperature difference across the wire array per unit heater power could be readily obtained by multiplying these two values. Thus, ΔT across the wires can be deduced once the heater power is known. (equation **2.5**). Typically, the temperature difference across the wire array is less than 5K.

$$\Delta T = W \left(\frac{\Delta R_H \Delta T_H}{\Delta W \Delta R_H} - \frac{\Delta R_C \Delta T_C}{\Delta W \Delta R_C} \right). \quad (2.5)$$

2.3.3 Thermal conductivity measurement

The thermal conductivity of the sample is measured based on a similar method developed by Shi et. al. [12]. Consider the equivalent thermal circuit of the device platform (Figure 4), at steady state, the heat source to the system is the heater (Q_h , heat generated from the serpentine part) plus the two current source leads of the heater ($2Q_L$). Ignoring the heat loss due to air conduction (which is valid when the system is at a vacuum condition of $< 5 \times 10^{-6}$ torr) and radiative transfer, the heat transferred from the hot to the cold end through the sample should be equal to the heat dissipated to the environment via the leads at the cold end. Thus,

$$Q_s = K_s \times (T_h - T_c) = K_L \times T_c + \left(\frac{1}{K_{ox}} + \frac{1}{K_h} \right)^{-1} \times T_c = \left(K_L + \frac{K_{ox} K_h}{K_{ox} + K_h} \right) T_c. \quad (2.6)$$

Also, due to the temperature difference between the hot side and the environment, heat could also dissipate into the environment from the leads on the hot side.

$$Q_L + K_L T_h + \left(\frac{1}{K_{ox}} + \frac{1}{K_h}\right)^{-1} T_h = Q_L + \left(K_L + \frac{K_{ox} K_h}{K_{ox} + K_h}\right) T_h. \quad (2.7)$$

Obeying energy conservation,

$$Q_L + \left(K_L + \frac{K_{ox} K_h}{K_{ox} + K_h}\right) (T_c + T_h) = Q_h + 2Q_L. \quad (2.8)$$

where $K_b \equiv K_L + \frac{K_{ox} K_h}{K_{ox} + K_h}$, is the total thermal conductance of the leads on each side.

From equation 2.8, we get

$$K_b = \frac{Q_h + Q_L}{T_c + T_h}. \quad (2.9)$$

Combining equations 2.9 and 2.6,

$$K_s = K_b \frac{T_c}{T_h - T_c}. \quad (2.10)$$

The thermal conductance of the sample (K_s) is thus obtained by measuring Q_h , Q_L , T_h , and T_c . Since the nanowire array is fabricated on a thin oxide substrate, differential measurement is performed to determine the thermal conductance of the silicon nanowires. Basically, the thermal conductance is measured before and after the nanowire array is selectively etched with XeF₂ gas. The thermal conductance of the nanowire array can be retrieved by the subtraction of the two values, $K_{(ox+NWs)} - K_{ox} = K_{NWs}$. Finally, the thermal conductivity, κ_{NW} , of the wires is calculated by taking the device geometry into account.

2.4 Results and Discussions: p-Type Nanowires

2.4.1 Electrical conductivity

Figure 5 shows the electrical conductivity of p-type nanowires with different wire widths and doping concentrations. The bulk device measured here is a film with 520 nm (width) x 1 mm (length) x 35 nm (height). As one can clearly see, the electrical conductivity of the 20-nm-wide nanowires is about 90% of the bulk-like film (red curve). The bulk-like electrical conductivity could be attributed to the fact that the carrier mean-free path is an order of magnitude smaller than the critical dimension of the sample, hence, the increase of surface-to-volume ratio by scaling down from bulk to 20 nm wires does not adjust the scattering mechanism from similarly processed bulk samples. The 10-nm-wide wires, however, have much smaller electrical conductivity than the bulk (~ 10%). The reason could be attributed to lower wire quality, i.e., more surface defects and surface roughness that are inherent in the narrower wire systems.

2.4.2 Thermal conductivity

The thermal conductivity (Figure 6) drops sharply with shrinking NW cross section; a two orders of magnitude decrease in thermal conductivity relative to the bulk is observed for the 10-nm-wide NWs. For all NWs measured, S / κ ratio leads to a significant enhancement of ZT relative to the bulk. The higher resolution thermal conductivity measurements on the 10 nm and 20 nm devices reveal that the thermal conductivity of silicon nanowires could be lower than the amorphous limit of silicon, $\kappa_{\min} = 0.99$ W/m-K (Figure 6).

2.4.3 The amorphous limit

In 1987, D. G. Cahill and R. O. Pohl found experimentally that *the minimum phonon mean-free-path is one half of a wavelength*. In the high temperature limit (i.e., shortest wavelength), the wavelength is twice the average inter-atomic distance. As a result, the minimum thermal conductivity of a material is reached when the mean-free-path equals the average inter-atomic distance [13]. Such situation is in essence the Einstein's energy random walk model, which states that heat transport in crystals is a random walk process of thermal energy between neighboring atoms oscillating with random phases. (G. A. Slack in 1979 proposed that Einstein's random walk model represents systems with minimum thermal conductivities. At the time, Slack assumed the minimum mean-free-path to be the Debye wavelength.) Disordered crystals exhibit thermal conductivities approaching to values predicted by Einstein's model, lower values have yet to be demonstrated by introducing higher disorder. This lower-limit of thermal conductivities is called the amorphous limit [14,15].

It is worth-noting that the phonons are described by the Debye model using bulk sound speeds with no optical modes. The 1/2 value is an order-of-magnitude estimate and is difficult to determine precisely. Also, κ_{\min} is proportional to the transverse and longitudinal acoustic speeds of sound. These are reduced in our nanowires at long wavelengths because the modes become one dimensional, particularly in the 10 nm nanowires. The ratio of the one-dimensional to two dimensional longitudinal speeds of sound is $[(1+n)(1-2n)/(1-n)]^{1/2}=0.87$, where $n=0.29$ is the Poisson ratio [16] of Si. The transverse acoustic speed goes

to zero at long wavelength because $v \propto k^2 d$ where d is the nanowire width. Therefore, the bulk κ_{\min} estimate in the amorphous limit is invalid for our nanowires and values smaller than κ_{\min} are attainable. However, a more detailed *ab initio* study is required to get a further understanding of how the thermal conductivity is lower than the amorphous limit.

4.2.4 Thermopower of the silicon nanowires

The square value of the thermopower of various wires as a function of temperature is shown in Figure 7. Most of the moderately doped p-type nanowires showed peaks around 200K. Similar peaks have been observed in some of the metals and lightly doped semiconductors at temperatures lower than 50K [17]. Such a phenomenon is explained by the phonon-drag mechanism.

The thermoelectric power contains two main sources: the diffusion thermopower caused by the diffusion of charge carriers, S_d , and thermopower generated by incorporating the momentum transfer between the phonons and the charge carriers, or phonon-drag thermopower, S_{ph} .

$$S = S_d + S_{ph} \cdot \quad (2.11)$$

The diffusion thermopower is described by Mott's formula [17,18], equation 2.12, and is linearly dependent on T.

$$S_d = \frac{\pi^2}{3} \left(\frac{k_B T}{e} \right) \left(\frac{d \ln \sigma(\epsilon)}{d \epsilon} \right). \quad (2.12)$$

2.4.5 Phonon-drag

When temperature gradient exists in the system, not only charge carriers but also phonons carry thermal energy and migrate from hot to cold. If the charge carrier-phonon interaction is sufficiently large, charge-carriers could be swept along with the phonons. This is basically the origin of the phonon-drag thermopower.

At sufficiently low temperatures, the phonon-phonon scattering can be neglected. Assume the phonon-gas model, the amount of pressure exerted on the charge carriers by the phonon gas through collision, is

$$p = \frac{1}{3}U_v(T). \quad (2.13)$$

$U_v(T)$ is the phonon internal energy per unit volume, or phonon energy density. A temperature gradient dT/dx also creates a pressure gradient of the phonon gas dp/dx . The additional electric field resulting from the momentum transfer between the charge carriers and phonons under such temperature/pressure gradient will equal the force exerted on the charge carriers by the phonon stream at steady-state, i.e.,

$$Ne\epsilon_x + F_x = 0$$

$$Ne\epsilon_x - \frac{1}{3} \frac{dU}{dT} \frac{dT}{dx} = 0$$

$$\frac{\epsilon_x}{dT/dx} = \frac{1}{3} \frac{C_{ph}}{Ne}.$$

Therefore, the phonon-drag thermopower can be shown as [17]

$$S_{ph} = \frac{1}{3} \frac{C_{ph}}{Ne}. \quad (2.14)$$

C_{ph} is the volume lattice specific heat, N is the number of conducting carriers per unit volume, and e represents the charge per carrier. Equation **2.14** predicts what may be called the “full phonon-drag” at low temperature. “Full” refers to the assumption that the phonon momentum is transferred completely to charge carriers. Accordingly to Debye’s prediction on the temperature dependence of the volume specific heat at low temperature $C_{ph} \propto T^3$ (Chapter 1), the phonon-drag thermopower also inherits such temperature dependence $S_{ph} \propto T^3$ at $T \rightarrow 0$.

Combining this and the previously mentioned T linear dependent on the diffusion thermopower, we can come to an expression that predicts the thermopower value as

$$S = S_d + S_{ph} = aT + bT^3. \quad (2.15)$$

(a and b are constants.)

At higher temperature, to a first approximation, equation **2.14** should be modified by a correction factor $\tau_p / (\tau_p + \tau_{pe})$, since other phonon scatterings have to be taken into account.

$$S_{ph} = \frac{C_{ph}}{3Ne} \frac{\tau_p}{\tau_p + \tau_{pe}}$$

τ_p is the overall relaxation time regarding other phonon scattering processes. τ_{pe} is the relaxation time of phonon-charge carrier scattering. At sufficiently high temperature $T \geq \theta_D$, $C_{ph} \approx 3N_0 k_B$ (Dulong-Petit limit; Chapter 1). N_0 is the number of atoms per unit volume. Thus,

$$S_{ph} \propto \frac{k_B}{e} \frac{\tau_p}{\tau_p + \tau_{pe}} \quad . \quad (2.16)$$

In such temperature, τ_{pe} is a constant and $\tau_p \propto 1/T$. Therefore, $S_{ph} \propto 1/T$.

As in the case of three-phonon scatterings, the electron-phonon scattering can also be categorized into normal processes (momentum conserved) and Umklapp processes (reciprocal lattice vector involved). Either type could give rise to phonon-drag thermopower, however, large momentum change involved in the Umklapp process could result in larger phonon-drag thermopower. In addition, the momentum reversal nature of the process could also create S_{ph} with opposite sign. The chance of the occurrence of the electron-phonon Umklapp process depends strongly on the distance between the distorted Fermi surface and the Brillouin zone boundary (or the relative magnitude of the electron wave vector and the reciprocal lattice vector) and can be characterized by $\exp(-\theta^*/T)$. θ^* represents the characteristic temperature of the spacing [17].

As the temperature increases, the anharmonicity becomes non-negligible. The number of phonons with energy q is given by Bose-Einstein equation,

$$N = \frac{1}{e^{\theta/T} - 1} \quad . \quad (2.17)$$

At $T \gg q$, $1/t_{ph} \sim N \sim T$. Hence, $S_{ph} \sim 1/T$. In other words,

$$S = S_d + S_{ph} = aT + b/T \quad . \quad (2.18)$$

Whereas at medium temperature range, $50K < T \ll q$ for metal and $200K < T \ll q$ for the p-type nanowires, the full Bose-Einstein equation should be applied. Thus,

$$S = aT + b \left[e^{\theta/T} - 1 \right] . \quad (2.19)$$

Taking $\theta=640\text{K}$ and fitting equation **2.19** to the experimental thermopower curve with a, b as parameters, we find that the linear term corresponds well to the thermopower of the bulk film, as well as to the one of the highly doped p-type nanowires that showed only the diffusion thermopower. See Figure **8**. This directly proves that the thermopower peak shown in the p-type devices is due to the phonon-drag effect.

5. Results and Discussions: N-Type Nanowires

5.1 Electrical conductivity

The electrical conductivity of the 20-nm-wide n-type nanowires also has a bulk-like value. Figure 9 shows the conductivity curves for three nanowire systems with different dopant concentrations. The conductivities in these systems are about 98%, 80%, and 70% of the bulk value, respectively.

5.2 Inter-valley scattering mechanism

Figure 10 plots the thermopower of the n-type 20-nm-wide nanowires as a function of temperature. No obvious phonon-drag was observed in the temperature window from 300K down to 100K. The theory that can account for this phenomenon is elaborated as follows. For indirect band-gap semiconductors, such as Si and Ge, the electrons in these materials are located in degenerate conduction band minima at the proximity of the Brillouin zone edge. In addition to intra-band scattering by phonons, electrons can be scattered from one degenerate valley to another via inter-valley scattering (Figure 11). The inter-valley

scattering process was found more important than the intra-valley scattering in relaxing the momentum and energy of conduction electrons [19, 20]. Phonons responsible for the intervalley scattering (either g or f process) are those at the Brillouin zone edge with large wave vectors and short lifetimes. Moreover, these phonons with large momentum render the charge carrier-phonon scattering mostly to Umklapp process, which is adverse to phonon-drag. Therefore, if the dominant electron-phonon scattering mechanism in n-type nanowire is the inter-valley scattering, one would have to cool the temperature down to at least less than 50K to be able to observe the phonon-drag, due to the fact that these phonons have substantially shorter wavelength than those in the p-type scattering events.

6. Conclusion

From the current results, we find that: 1) The electrical conductivity in the nanowires is bulk-like. 2) Phonon drag effect causes an approximately four fold increase in the thermopower as compared to bulk Si. 3) There is an ultra-small thermal conductivity, as small as 0.76 W/m-K for 10 nm SiNWs, possibly due to the dimensional cross over in this systems. All together with these discoveries, we are able to show the thermoelectric figure-of-merit of 1.2 (about 100 times larger than its bulk counterpart) with p-type silicon nanowires. The thermoelectric properties of n-type silicon nanowires are also investigated. Electrical and thermal conductivity similar to those p-type nanowires are observed. However, no phonon-drag is detected in n-type nanowires due to the dominant intervalley electron-phonon scattering process.

Further parameter optimization: by doping, geometry, composition (for instance, SiGe), phonon engineering, charge carrier scattering mechanisms, the birth of a silicon-based system with a ZT equal to 3, and efficiency comparable to conventional refrigerators can be expected in the near future.

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Figure 1.

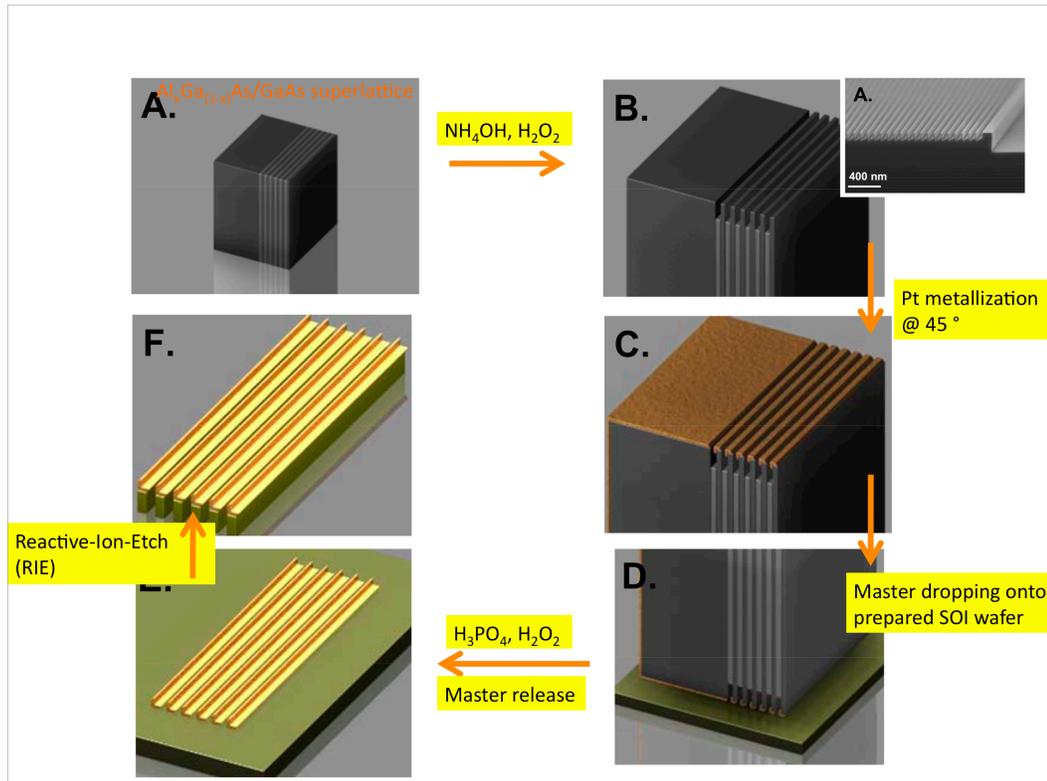


Figure 2.

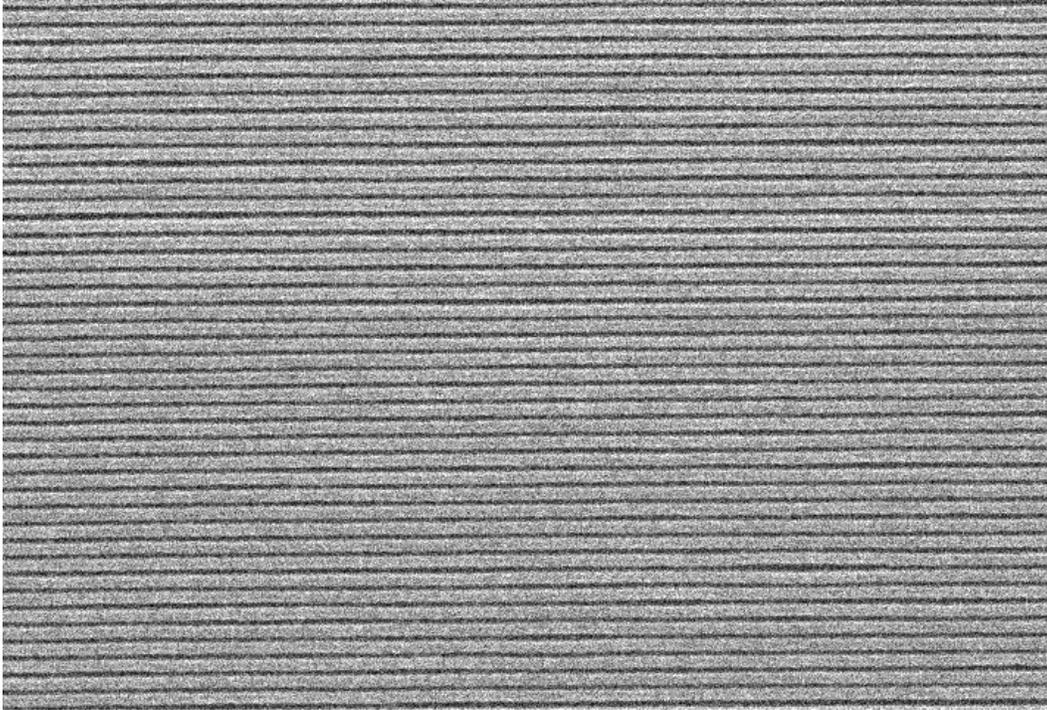


Figure 3.

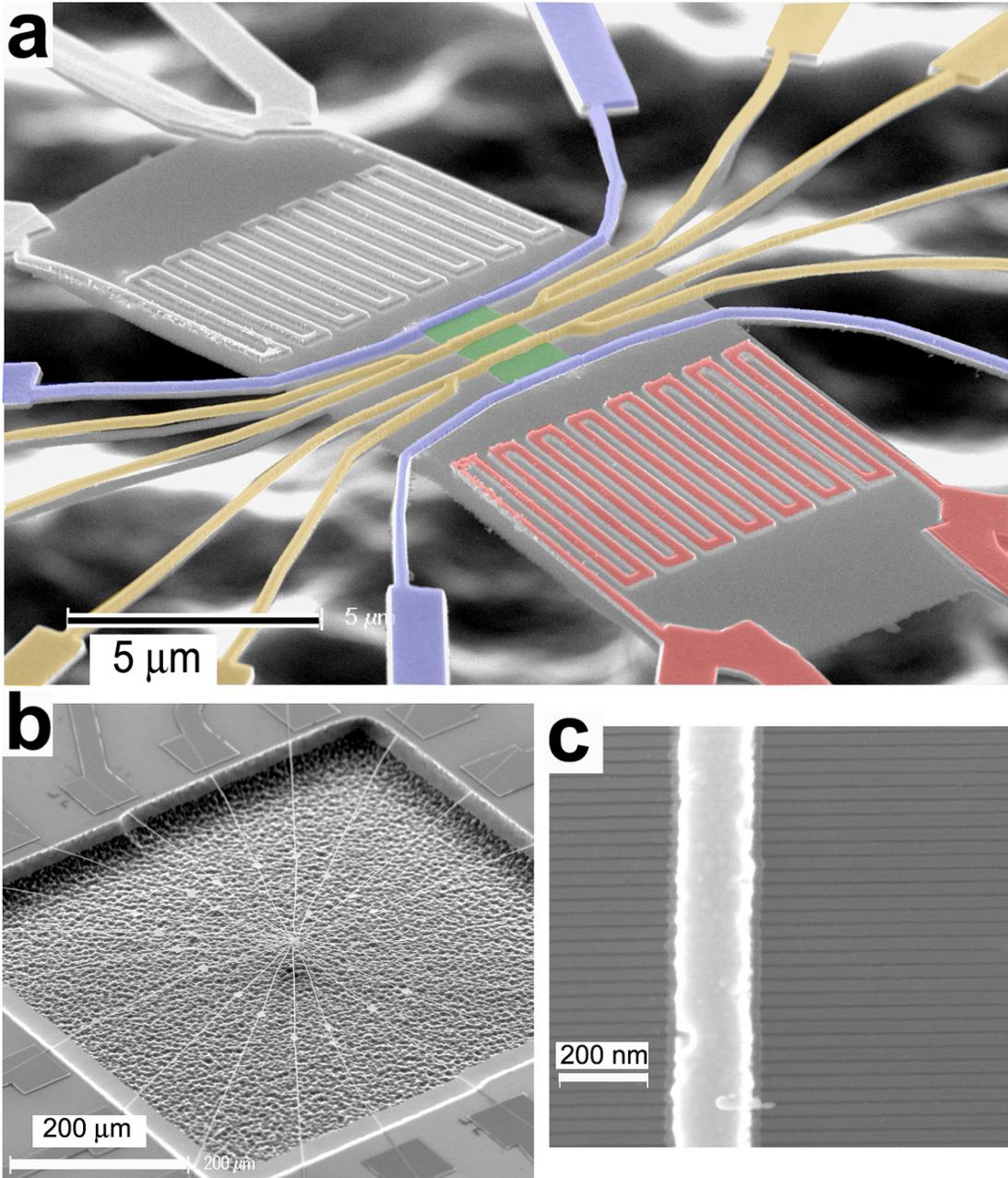


Figure 4.

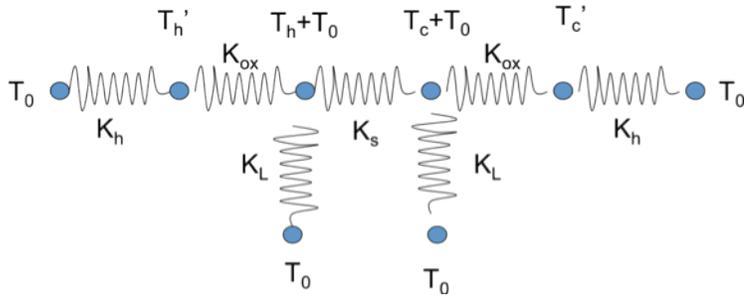


Figure 5.

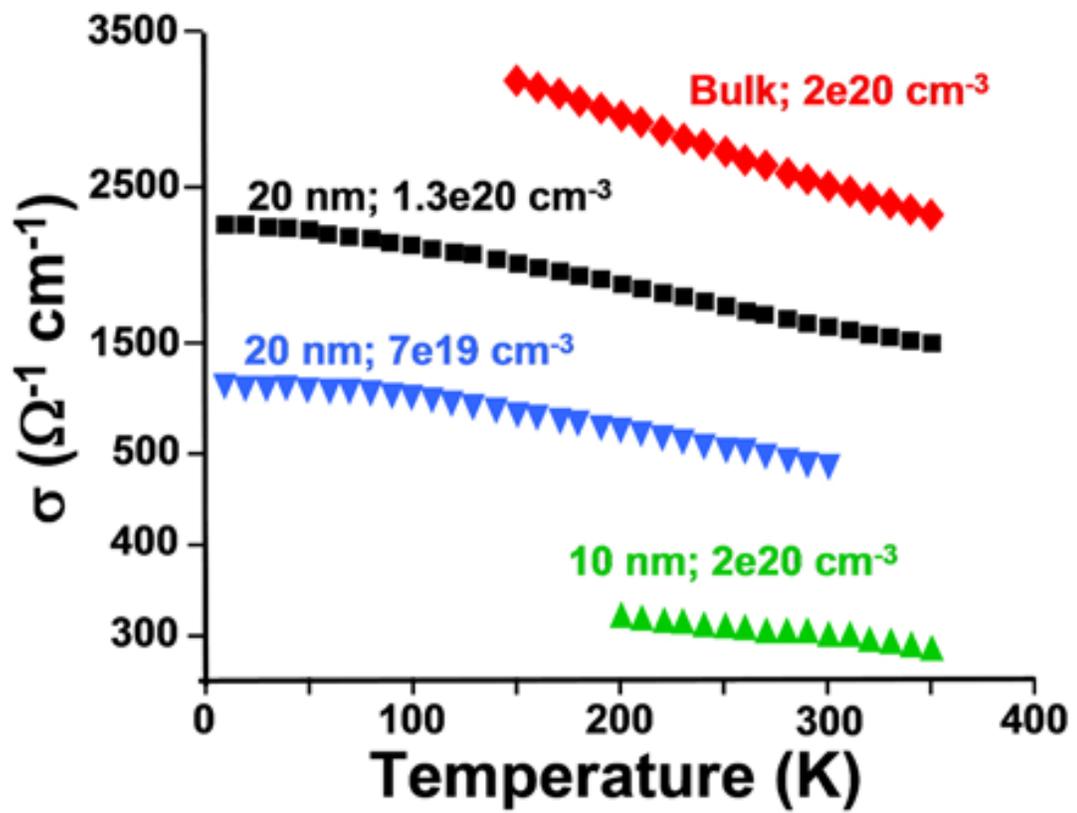


Figure 6.

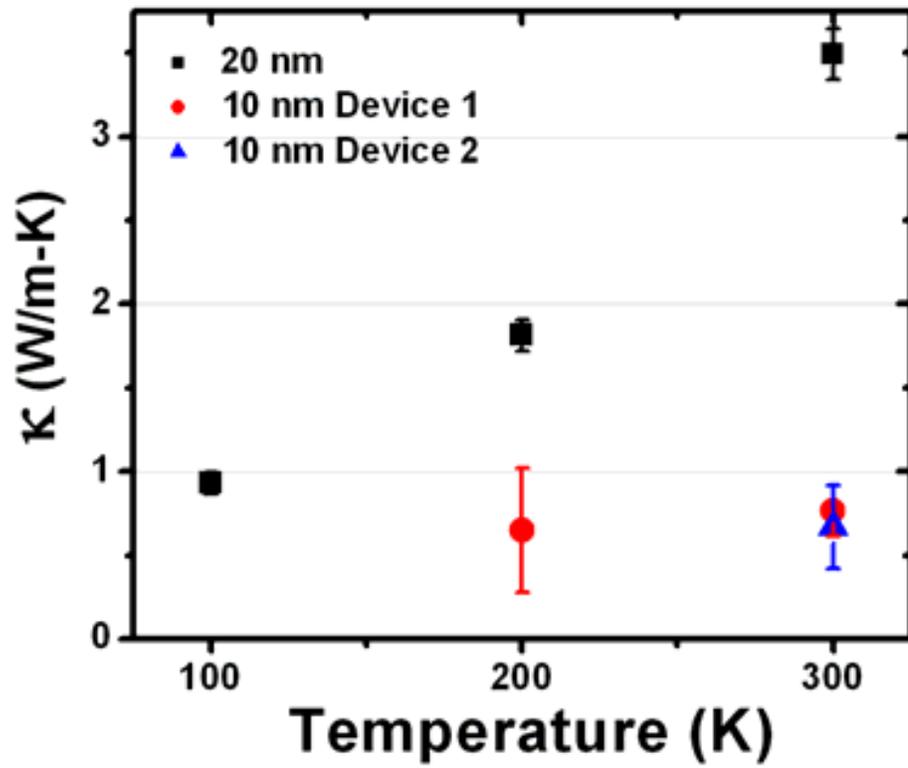


Figure 7.

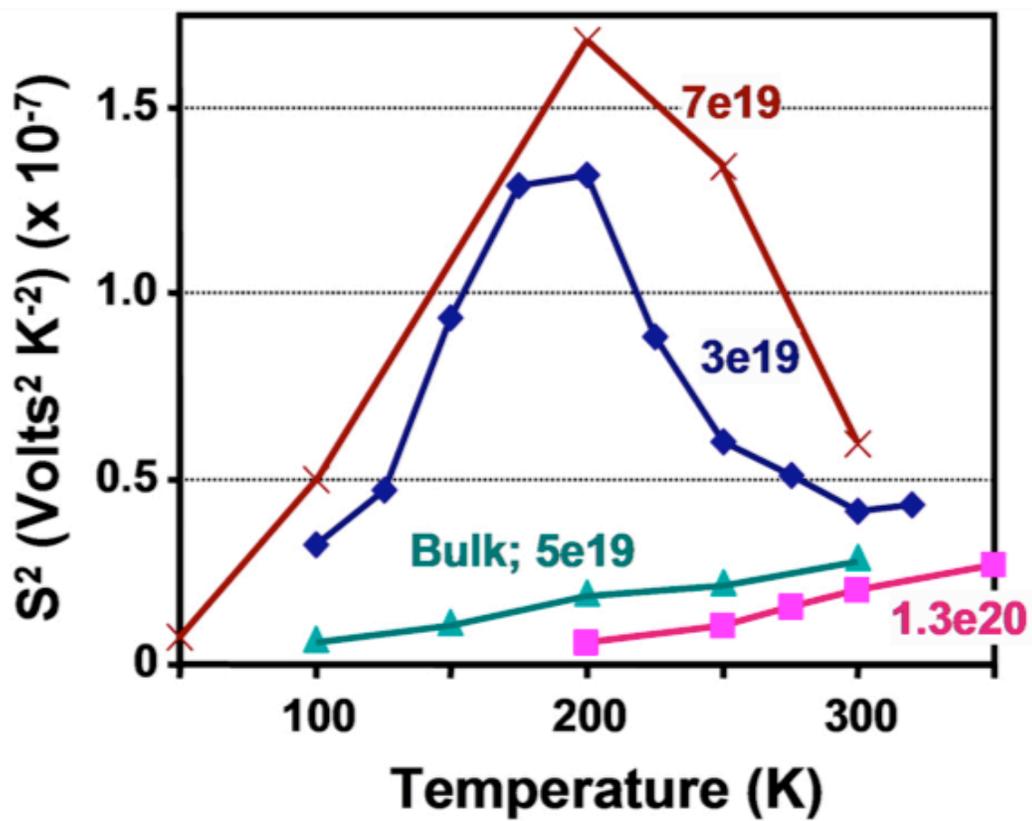


Figure 8.

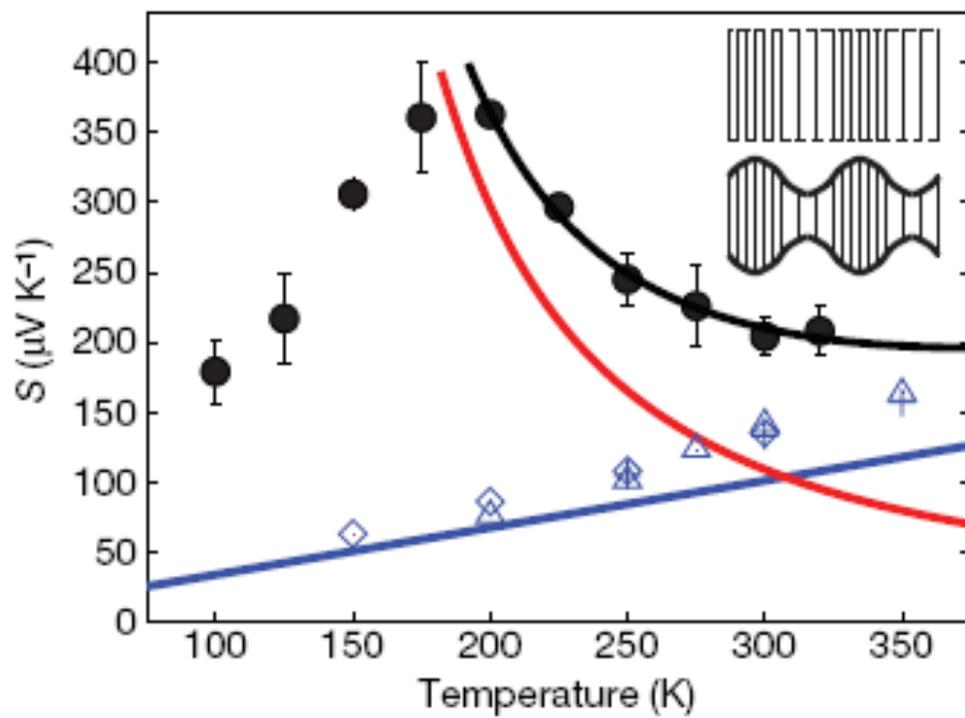


Figure 9.

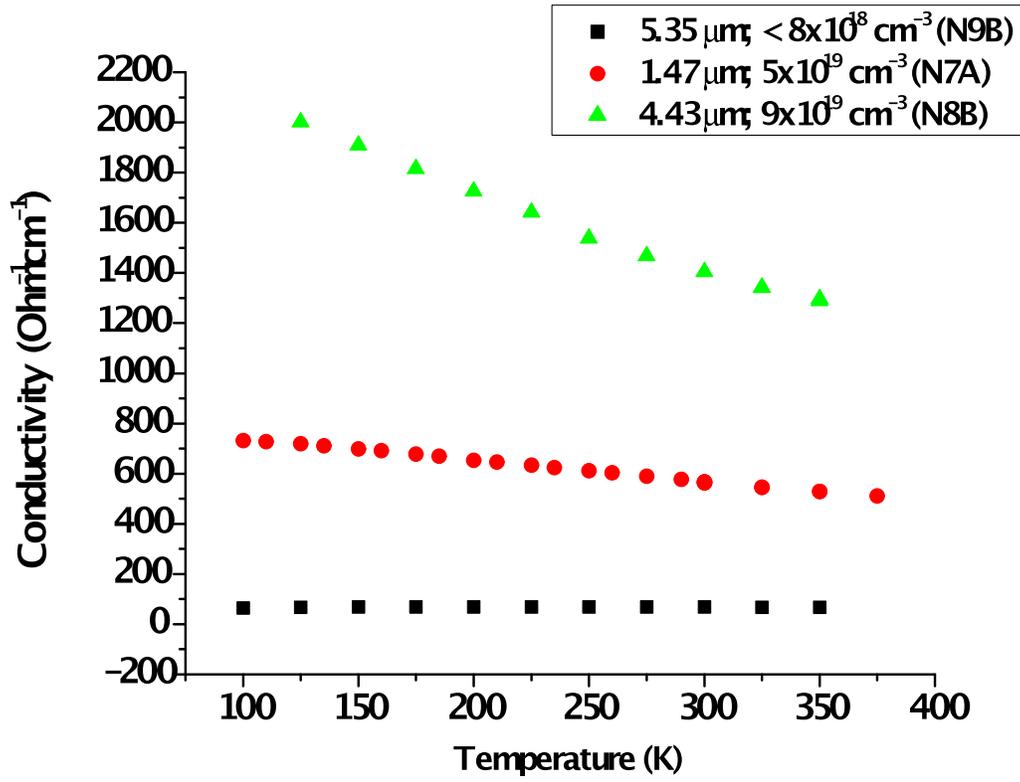


Figure 10.

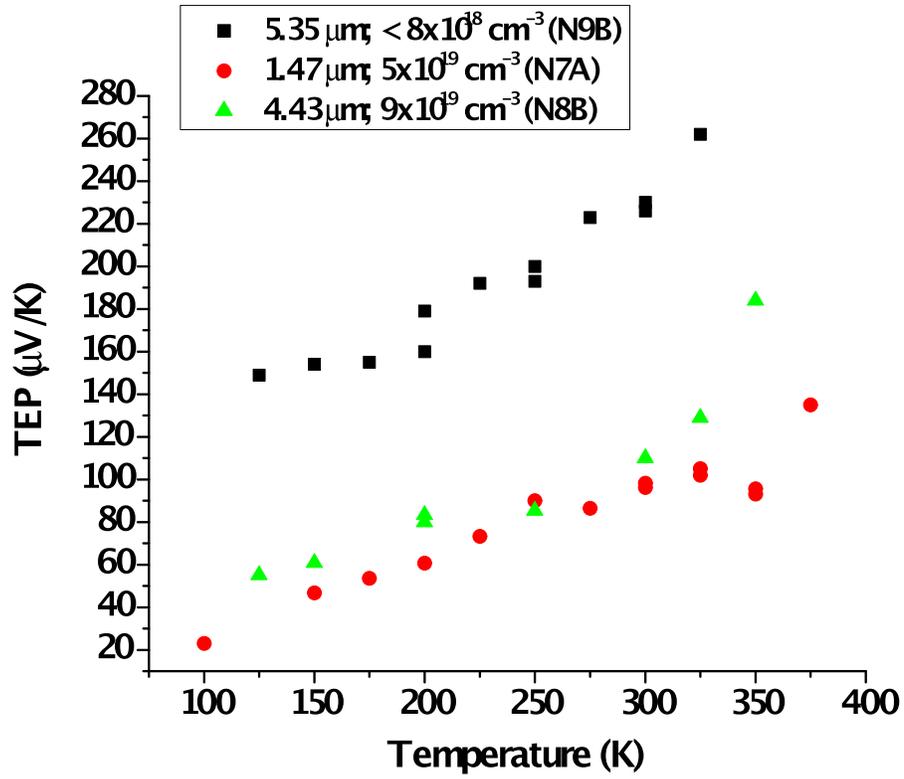


Figure 11.

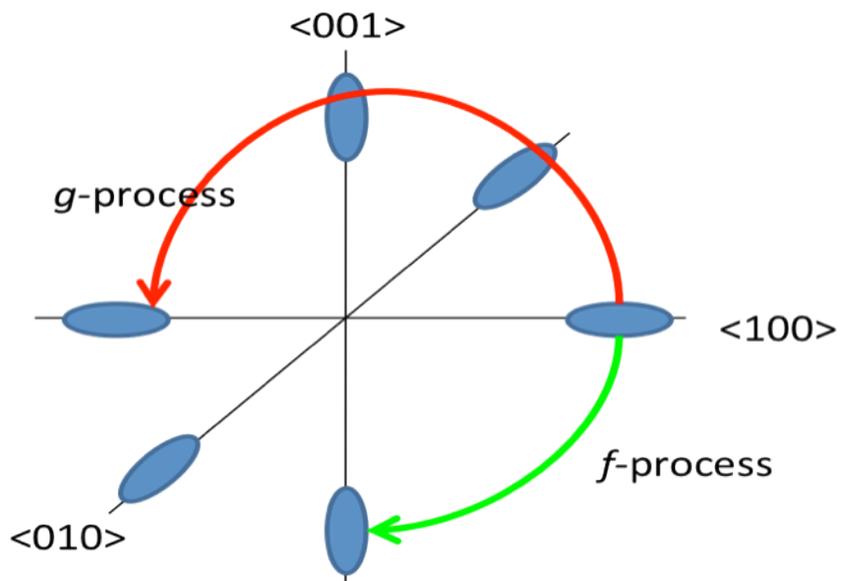


Figure Captions

Figure 1. Superlattice Nanowire Pattern Transfer

(A) An imaginary figure depicting the $\text{Al}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ superlattice. (B) The $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer is selectively etched back by NH_4OH solution creating a comb-like structure (inset). (C) The superlattice is metalized by e-beam assisted physical vapor deposition at an angle of 45° . (D) The superlattice is dropped onto a silicon-on-insulator wafer. A epoxy-PMMA adhesion layer is pre-spun on the wafer. After positioning the superlattice master, the epoxy is cured at 180°C for 40 minutes. Then, the entire wafer is placed in a phosphoric acid solution for 4.5 hours. (E) Metal wire array is left behind on the SOI wafer after releasing the superlattice master. (F) Reactive-ion-etching is exploited at this step to transfer the metal wire pattern into the SOI.

Figure 2. Scanning electron micrograph image of a 20-nm-wide, 34-nm-pitch silicon nanowire array made by SNAP process

Figure 3. SEM images of the device

(a) This false color image of a suspended platform shows all electrical connections. The central green area is the Si NW array. The NWs are not well-resolved at this magnification. The grey region underlying the NWs and the electrodes is the 150 nm thick buried oxide (BOX) layer sandwiched between the top Si(100) single crystal film from which the NWs are fabricated, and the underlying Si wafer. The underlying Si wafer has

been etched back to suspend the measurement platform, placing the background of this image out of focus. **(b)** Low resolution micrograph of the same suspended platform. The 20 electrical connections to the heaters and various electrodes radiate outwards and support the device. **(c)** High resolution image of an array of 20 nm wide Si NWs with a Pt electrode.

Figure 4. Equivalent thermal circuit of the measurement platform

The equivalent thermal circuit of our device. T_0 denotes the cryostat temperature. T_h (T_c) is the temperature increase measured by the resistive thermometer at the hot (cold) end of the nanowire array. T_h' / T_c' is the temperature of the right (on-state)/ left (off-state) heater. K_{ox} , K_L , K_h , and K_s represent the thermal conductance of the oxide, the thermometer leads, the heater, and the sample.

Figure 5. Temperature dependent electrical conductivity of boron-doped silicon nanowires.

Representative electrical conductivity data for Si NWs and microwires; p-type doping levels are indicated. All NWs are 20nm in height.

Figure 6. Thermal conductivity of the silicon nanowires. The temperature dependence of the thermal conductivity (κ).

Figure 7. Thermopower of the silicon nanowires. The temperature dependence of the square of the thermopower for 20 nm x 20 nm (= 400 nm²) Si NWs at various p-type doping concentrations (indicated on the graph).

Figure 8. Thermopower fit to equation 3.18

Thermopower calculation plotted along with experimental data (black points) from a 20-nm-wide Si nanowire p-type doped at $3 \times 10^{19} \text{ cm}^{-3}$. The black curve is the fitted expression for the total thermopower $S_e + S_{ph}$. The red curve is the phonon contribution S_{ph} and the blue line is the electronic term S_e arising from the fit. The experimental error bars represent 95% confidence limits. The blue data points are experimental values for bulk wires (doping $2 \times 10^{20} \text{ cm}^{-3}$; crosses), 10-nm-wide nanowires (doping $7 \times 10^{19} \text{ cm}^{-3}$; diamonds), and 20-nm-wide wires (doping $1.3 \times 10^{20} \text{ cm}^{-3}$; triangles) where only a linear-T electronic contribution was found. The inset shows the character of a three dimensional bulk longitudinal acoustic phonon mode (top) and a one dimensional mode when the wavelength is larger or of the order of the width (bottom). The one-dimensional mode incorporates the existence of the boundary by transverse expansion (or compression) for longitudinal compression (or expansion). The ratio of the transverse strain to the longitudinal strain is the Poisson ratio (0.29 for Si).

Figure 9. n-type 20nm silicon nanowire conductivity vs T curves. The temperature dependent electrical conductivity data of three n-type SiNWs doped at three different dopant concentrations.

Figure 10. n-type 20nm silicon nanowire thermopower vs T curves. The temperature dependent thermopower data of three n-type SiNWs doped at three different dopant concentrations.

Figure 11. Schematics of the e-ph scattering mechanisms at the conduction band minima. The constant energy surface diagram of the conduction band of silicon. The red and green curves describe the f and g -processes respectively.