NANOSTRUCTURED SILICON THERMOELECTRICS

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To My Wife, Yi-Chun Iris Chen and My Parents,

Hsueh-Erh Hsu Yu and Jung-Tsung Yu

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ABSTRACT

The thesis discusses the thermoelectric properties of silicon nanostructures with a particular focus on their heat transport phenomenon. The aim of this thesis work is to design ultra-low thermal conductivity materials based on fundamental phonon physics. Silicon nanowires and silicon nanomeshes are the model nanostructure systems investigated in this thesis.

Degenerately boron-doped silicon nanowires (20 nm x 20 nm cross section) exhibit thermal conductivity, depending on the temperature of interest, roughly two orders of magnitude smaller than bulk silicon with similar impurity concentration. The reduction in thermal conductivity is presumably from increased boundary scattering of the thermal phonons. For smaller nanowire systems (e.g., 10 nm x 20 nm cross section), thermal conductivity lower than the amorphous limit is also observed. Dimensional crossover of the thermal phonons in these ultra-small nanowire systems is proposed to explain the thermal conductivity reduction. Thermoelectric figure-of-merit ZT~1, a two order of magnitude improvement is achieved in 20 nm x 20 nm silicon nanowires at 200K.

Silicon nanomeshes are designed to further reduce the thermal conductivity of silicon. The 2-D hole-array is patterned on the silicon nanomesh film as Bragg reflectors to slow down the phonon group velocity. From the direct thermal conductivity measurement via suspended microstructure platform, the coherent scattering mechanism effectively reduces the thermal conductivity of silicon by a factor of two from the nanowire value. In essence, the phononic metamaterial approach essentially creates a new class of silicon-based

material with distinct phonon properties, in other words, the theoretical lower limit of thermal conductivity of silicon based on bulk dispersions no longer applies to the phononic nanomeshes. In addition, silicon nanomeshes exhibit bulk-like electrical conductivity rendering them potential high efficiency thermoelectrics.

In Chapter 1, an introduction to the lattice thermal conductivity is given to point out the key parameters affecting the phonon transport, e.g., scattering mechanisms, phonon dispersions and phonon density-of-states. The thermoelectrics fundamentals are given in Chapter 2, as are the experimental results on silicon nanowires. The fabrication and measurement methodologies are also explained in this chapter. In Chapter 3, the phonon transport mechanism of the silicon nanomesh, a new class of phononic metamaterial, is investigated. A coherent phonon scattering mechanism is used to explain the unexpected phonon behaviors. A complete fabrication process flow is also developed in this chapter in order to fully release the nanostructure from the substrate for precise and accurate thermal conductivity measurement. In the last part of the thesis (Chapter 4), the phononic nanomesh approach is extended to a nanomesh superlattice structure. The architectural design is to incorporate interfacial thermal resistance or the Kapitza resistance to further reduce the thermal conductivity of silicon. In addition, device architecture consisting of self-assembled quantum dots is proposed to enhance the thermoelectric efficiency by energy-filtering mechanism.

TABLE OF CONTENTS

LIST OF FIGURES

Chapter II

Chapter III

Chapter IV

C h a p t e r 1

INTRODUCTION TO THERMAL CONDUCTIVITY

This chapter aims to review the fundamental heat transport theory in bulk materials.

The general approach to calculate the lattice thermal conductivity is to solve the Boltzmann transport equation under the relaxation time approximation, while the scattering cross section is calculated by perturbation theory [1,2].

$$\kappa_i = \frac{1}{(2\pi)^3}\sum_n \int \left(\upsilon_{\mathbb{k},n}\cdot\hat{i}\right)^2 \tau_{\mathbb{k},n} C_{ph}(\mathbb{k},n)\, d\mathbb{k} \text{ . } \textbf{(1.1)}$$

The summation is over all the phonon modes n. $\hat{i}$ is a unit vector along a principle crystal axis and the temperature gradient. $\mathbb{k}$ is the wave vector. C_{ph} is the specific heat per phonon mode for frequency ω. $\upsilon_{\mathbb{k},n}$ is the phonon velocity for the nth mode at wave vector $\mathbb{k}$. The specific heat (*vide infra*) is written as

$$C_{ph} = \frac{\hbar^2\omega^2}{k_B T^2}\frac{\exp\left(\hbar\omega / k_B T\right)}{\left[\exp\left(\hbar\omega / k_B T\right)-1\right]^2} \text{ . } \textbf{(1.2)}$$

In case of isotropic $\upsilon_{\mathbb{k}}$,

$$\kappa = \frac{4\pi}{3}\frac{1}{(2\pi)^3}\sum_n \int \upsilon_{\mathbb{k},n}^2 \tau_{\mathbb{k},n} C_{ph}(\mathbb{k},n)\, g(\mathbb{k},n)\, d\mathbb{k} \text{ . } \textbf{(1.3)}$$

$g(\mathbb{k},n)$ is the phonon density-of-states and can be written as $g(\mathbb{k},n)d\mathbb{k} = \left(\omega^2 / \upsilon^3\right)d\omega$ in Debye's limit (i.e., $\omega = \upsilon\mathbb{k}$). Thus,

$$\kappa = \frac{1}{3}\frac{1}{2\pi^2}\sum_n \int_0^{\omega_{0,n}} \frac{\tau_{\omega,n}}{\upsilon_{\omega,n}} C_{ph}(\omega,n)\omega^2 \, d\omega \,. \textbf{(1.4)}$$

$\omega_{0,n}$ is the maximum frequency for the n-th phonon branch.

According to equation **1.1-1.4**, accurate descriptions of the phonon band diagram and the scattering mechanisms are critical for reliable prediction and calculation of the thermal conductivity. This chapter will review the expressions for the specific heat and the scattering rates. Several important lattice thermal conductivity models and their applicable conditions are also discussed. In addition, methodologies for modeling the phonon band diagram will be briefly described.

Specific Heat C_V [2,3]

Thermodynamically, the volume specific heat is defined as

$$C_V = (\frac{\partial U}{\partial T})_V \,. \textbf{(1.5)}$$

Lattice vibrations are generally simplified as harmonic oscillators. In this model, every vibration energy level is spaced by the Planck energy $\hbar\omega$, with the zero-point energy $\frac{1}{2}\hbar\omega$. ω is the vibration frequency of the mode. For phonons, the population distribution is described by the Bose-Einstein distribution, $D_{n,\mathbb{k}}(\omega,T) = \left[\exp(\hbar\omega_{n,\mathbb{k}} / k_B T) - 1\right]^{-1}$. $D_{n,\mathbb{k}}(\omega,T)$ is called the occupation number, or, in the context of lattice dynamics, the phonon number. Thus, the total energy of the phonons in a particular branch is then given as

$$U_{n,\mathbb{k}}(\omega,T) = \hbar\omega_{n,\mathbb{k}}\left[\frac{1}{2} + D_{n,\mathbb{k}}(\omega,T)\right]. \textbf{(1.6)}$$

Note that the phonon number depends on temperature and the vibration frequency. The total internal energy of the crystal is the summation of $U(\omega,T)$ over all the phonon branch and wave vectors, $\sum_{n,\mathbb{k}} U_{n,\mathbb{k}}(\omega,T)$. Taking the temperature derivative of $\sum_{n,\mathbb{k}} U_{n,\mathbb{k}}$, we obtain the specific heat as

$$C_V = \sum_{n,\mathbb{k}} \frac{\hbar^2\omega_{n,\mathbb{k}}^2}{k_B T^2} \frac{\exp\left(\hbar\omega_{n,\mathbb{k}} / k_B T\right)}{\left[\exp\left(\hbar\omega_{n,\mathbb{k}} / k_B T\right) - 1\right]^2}. \textbf{(1.7)}$$

In Einstein's model proposed in 1907, every atom is oscillating independently at a same frequency, ω_E. The internal energy of the system is then given as

$$U = 3N\hbar\omega_E\left(D(\omega_E,T) + \frac{1}{2}\right) = 3N\frac{\hbar\omega_E}{\exp(\hbar\omega_E / kT) - 1} + 3N\frac{\hbar\omega_E}{2}. \textbf{(1.8)}$$

N is the number of atoms. From equation **1.8**, the specific heat could be derived as

$$C_V = \frac{\partial U}{\partial T} = 3Nk\left(\frac{\hbar\omega_E}{kT}\right)^2 \frac{\exp(\frac{\hbar\omega_E}{kT})}{\left(\exp(\frac{\hbar\omega_E}{kT}) - 1\right)^2}. \textbf{(1.9)}$$

In the low temperature limit, $T \to 0$

$$C_{V,ph} \approx e^{-\hbar\omega_E / kT}. \textbf{(1.10)}$$

In this model, the specific heat drops exponentially as temperature goes to absolute zero. However, such fast decay does not fit well to the experimental results, which demonstrate that the specific heat decreases with T^3 dependence rather than the activation process-like decay.

As in equation **1.6**, the internal energy of the crystal lattice is a function of phonon frequency. It is thus convenient to re-write equations **1.6** and **1.7** as integrals of the phonon frequencies:

$$U = \int \hbar\omega \left[\frac{1}{2} + D(\omega,T) \right] g(\omega) d\omega \text{ . } \textbf{(1.11)}$$

$$C_{V,ph} = \frac{\partial}{\partial T} \int \hbar\omega D(\omega,T) g(\omega) d\omega \text{ . } \textbf{(1.12)}$$

$g(\omega)$ is defined as the density-of-states. As such, the number of phonon modes within ω and $\omega + d\omega$ is $g(\omega)d\omega$. For a 3-dimensional isotropic crystal,

$$g(\omega)d\omega = \frac{\int d^3k}{\Delta^3 k} = \frac{\int d^3k}{(2\pi / a)^3} \text{ . } \textbf{(1.13)}$$

a is the lattice constant of the crystal. Further mathematical deduction yields that

$$g(\omega)d\omega = \frac{a^3}{2\pi^2} \frac{k^2}{d\omega / dk} d\omega \text{ . } \textbf{(1.14)}$$

In the Debye model, rather than treating the phonons as individual random oscillators, the atoms vibrate collectively in a wave-like fashion. The phonon branch is assumed to be non-dispersive (i.e., $\omega = \upsilon k$). Thus,

$$g(\omega) = a^3\omega^2 / 2\pi^2\upsilon^3 \text{ . } \textbf{(1.15)}$$

The linear dispersion is applicable to acoustic phonons at low frequencies. The Debye model fails to predict the specific heat for high-frequency phonons, as the dispersion at high frequencies deviate from linearity. Approximating the first Brillouin zone by a sphere with the same volume, we can now calculate the specific heat of the lattice vibrations (two transverse modes and one longitudinal mode) in Debye's model by integrating equation **1.11**,

$$U = \frac{3a^3}{2\pi^2 \upsilon^3} \int_0^{\omega_D} \omega^2 \frac{\hbar\omega}{\exp(\frac{\hbar\omega}{kT}) - 1} d\omega = 9NkT(\frac{T}{\theta})^3 \int_0^{x_D} dx \frac{x^3}{e^x - 1}. \textbf{(1.16)}$$

N is the number of atoms in the first BZ; θ is the Debye temperature of the material ($\theta = \frac{\hbar\omega_D}{k_B} = \frac{\hbar\upsilon_g}{k}\sqrt[3]{6\pi^2 N}$). ω_D is the vibration frequency at the Debye temperature. $x_D \equiv \hbar\omega_D / kT$. In equation **1.16**, the $\int \frac{1}{2}\hbar\omega g(\omega) d\omega$ term is omitted for simplicity, as our goal here is to find the expression for specific heat. Taking the temperature derivative of equation **1.16**, we find:

$$C_{V,ph} = \frac{1}{2\pi^2 \upsilon^3} \int_0^{\omega_D} \frac{\hbar^2 \omega^4}{k_B T^2} \frac{\exp(\hbar\omega / k_B T)}{\left[\exp(\hbar\omega / k_B T) - 1\right]^2} d\omega = 9Nk\left(\frac{T}{\theta}\right)^3 \int_0^{x_D} \frac{x^4 e^4}{\left(e^x - 1\right)^2} dx .$$

Debye's model predicts a T^3 dependency of thermal conductivity when $T \to 0$.

$$C_{V,ph} = \frac{12\pi^4}{5} Nk(\frac{T}{\theta})^3 \propto T^3 . \textbf{(1.17)}$$

In the high-temperature limit, defined as $\hbar\omega \gg k_B T$, $\frac{1}{2} + D_{n,\mathbb{k}}(\omega, T)$ approaches $k_B T / \hbar\omega$, thus, $U_{n,\mathbb{k}}(\omega, T) \approx k_B T$. As a result, all the phonon modes have the same energy as $k_B T$ at the high-temperature limit. Since the number of normal modes equals the number of degree of freedom 3N (N: number of atoms), $\sum_{n,\mathbb{k}} U_{n,\mathbb{k}} \approx 3Nk_B T$, $C_{V,ph} \approx 3Nk_B$ at high temperatures. This is the Dulong-Petit law, which empirically states that at high temperatures all the specific heat saturates to a constant independent of the material.

Phonon Relaxation Time τ

The phonon relaxation time is a collective parameter governed by various phonon scattering processes. It is highly dependent on the material systems, and the dominant mechanisms in most cases are the isotope/impurity scattering, the boundary scattering, the Umklapp process, and the three-phonon normal process. Matthiessen's rule proposes that the resistivity of a system with distinct scattering mechanisms is the sum of the individual resistivities alone [2]. Thus,

$$\frac{1}{\tau} = \sum_i \frac{1}{\tau_i}. \quad \textbf{(1.18)}$$

In cases when τ is wave vector $\mathbb{k}$ dependent, the conductivity is proportional to some average $\bar{\tau}$. Thus, Matthiessen's rule is modified as

$$\frac{1}{\tau} = \sum_i \frac{1}{\bar{\tau}_i}. \quad \textbf{(1.19)}$$

Developing the expressions for the relaxation times is non-trivial, especially for the three-phonon processes. In the following paragraphs, we discuss the scattering time expressions for the various processes in some commonly seen models. Due to the fact that many of the relaxation processes are dependent on the phonon frequencies, as well as the characteristics of the dispersions of the phonon branches, some fundamental assumptions are applied in the scattering time expressions in each model that limit the validity of the expressions to certain phonons at particular temperature ranges.

Lattice Thermal Conductivity Models

The behavior of the lattice thermal conductivity is qualitatively described by the early work of Debye and Peierls: (1) the lattice thermal conductivity at very low temperatures depends strongly on the size and shape of the crystal (long phonon mean-free-path) and increases with the specific heat (T^3 dependence) as temperature goes up. (2) The lattice thermal conductivity starts to decline as the temperature reaches high enough (~ $0.1\theta_D$), when the Umklapp processes start being dominate. (3) At the peak of the thermal conductivity, its value is sensitive to crystal imperfection such as impurities, isotopes, and defects. Following Debye and Peierls' work, several models have been proposed to better describe the thermal conductivity characteristics:

1. The Klemens Model [4]

In the Klemens model, the thermal conductivity for different scattering mechanisms are calculated separately and the total thermal conductivity in this model is given as

$$\frac{1}{\kappa} = \sum_i \kappa_i^{-1} . \textbf{(1.20)}$$

In the Klemens model the phonon-point defect (defects with mass difference such as isotopes, impurities, etc.) scattering is given as

$$\frac{1}{\tau_{I,j}} = \frac{\pi}{6} V' \Gamma g(\omega) \omega^2 = \frac{V' \Gamma}{4\pi \upsilon_j^3} \omega^4 . \textbf{(1.21)}$$

$$\Gamma = \frac{\sum_i (c_i M_i)^2 - \left(\sum_i c_i M_i \right)^2}{\left(\sum_i c_i M_i \right)^2} . \textbf{(1.22)}$$

$\tau_{I,j}$ is the phonon-impurity relaxation time of the j phonon branch; V' is the atomic volume; Γ is the so-called mass-fluctuation phonon scattering parameter. c_i and M_i denote the concentration and the mass of the point defects (e.g., isotopes or the impurities). In equation **1.20**, the Debye model phonon density-of-state (equation **1.15**) is assumed. Under such assumption, the expression fails for the zone edge high frequency phonons as the dispersion curve turns convex-up, rendering a higher density-of-state.

Note that the point-defect scattering *is strongly dependent on the phonon frequency, group velocity, and impurity content*. The $\tau^{-1} \propto \omega^4$ relation is similar to the Rayleigh scattering in photons. It has been experimentally confirmed that the impurity level has a large effect on the thermal conductivity. For example, the highly enriched ^{70}Ge (99.99%) sample has maximum thermal conductivity 14 times higher than the $^{70/76}$Ge sample (43% of ^{70}Ge; 48% of ^{76}Ge; 9% others) [1].

2. The Callaway model [5]

In 1959 Joseph Callaway developed a model to calculate the lattice thermal conductivity valid at low temperatures (2.5K to 100K). In Callaway's model, an isotropic Debye-like phonon spectrum is assumed, i.e., no distinction between longitudinal and transverse phonons and the phonon branches are non-dispersive. The scattering mechanisms considered in this model are:

a. Isotope/point impurity scattering

In Callaway's model, the isotope scattering takes the form proposed by Klemens (i.e., $\tau_I^{-1} = A\omega^4$). A is a fitting parameter which depends on the mass-fluctuation phonon scattering parameter and the phonon velocity as in the Klemens model.

Assumptions and validity: (I) Debye-like phonon spectrum and the Debye's description of the density-of-states. Therefore, this expression applies to low temperature region where Debye's model is valid. **(II) An averaged phonon velocity for longitudinal and transverse branches.**

b. Boundary scattering

$\tau_B^{-1} = \upsilon_B / L_0$; υ_B is the average speed of sound. L_0 is the characteristic length of the sample.

Assumptions and validity: (I) Since no specularity factor is incorporated, the Callaway model assumes that the scattering at the surface boundary is purely diffusive. (II) Again, the speed of sound is the averaged phonon velocity for longitudinal and transverse branches.

c. Three-phonon normal process

$\tau_N^{-1} = B_2 T^3 \omega^2$ B_2 is a fitting parameter which depends on the Gruneisen constant and the phonon velocity. The expression was derived by Herring [6] for longitudinal phonon scattering under momentum conservation conditions at low temperatures.

Assumptions and validity: Low-temperature longitudinal phonons.

d. Umklapp process

$\tau_U^{-1} = B_1 T^3 \omega^2$ B_1 is a fitting parameter which contains the exponential temperature factor $\exp(-\theta / bT)$ as suggested by Peierl, the phonon velocity, the Gruneisen constant, and the Debye temeperature.

Assumptions and validity: The Umklapp process expression in Callaway's model is neither a high-temperature nor a low-temperature assumption; thus, the model fails to describe the Umklapp process, limiting the model to the low-temperature region where the Umklapp process is negligible.

The overall relaxation time is

$$\tau = \left(\upsilon_B L_0^{-1} + B_1 T^3 \omega^2 + A\omega^4 + B_2 T^3 \omega^2 \right)^{-1} . \textbf{(1.23)}$$

The thermal conductivity can thus be expressed as [7]

$$\kappa = \frac{1}{2\pi^2 \upsilon_B} \int_0^{\omega_D} \frac{\hbar^2 \omega^4 k_B T^{-2}}{\upsilon_B L_0^{-1} + \left(B_1 + B_2\right) T^3 \omega^2 + A\omega^4} \frac{\exp(\hbar\omega / k_B T)}{\left[\exp\left(\hbar\omega / k_B T\right) - 1\right]^2} d\omega . \textbf{(1.24)}$$

The three-phonon normal process is incorporated in equation **1.24**; such treatment assumes the normal process as a resistive scattering process. However, the three-phonon normal process does not contribute to thermal resistance, since the phonon momentum is conserved. Thus, in the original Callaway's model, an additional correction term was introduced to counteract errors by treating the normal process as entirely resistive. The correction term is usually neglected because it is found to be small in most cases, where the normal process relaxation time is much longer than the resistive process [5].

The Callaway's model assumes a non-dispersive phonon spectrum with no distinction in the phonon modes. Therefore, the model fails to explain the thermal conductivity of

materials with highly dispersive phonon spectrums at high temperatures such as germanium and silicon. Moreover, the relaxation time expressions for the three-phonon normal and Umklapp processes are over-simplified from reality. *Thus the model predicts the thermal conductivity behavior well only at low temperatures ($\leq 0.1\theta_D$) where the Debye-like phonon spectrum is a good approximation and only the isotope/impurity scattering and boundary scattering are important*.

3. The Holland model [2]

Distinct from the Klemens and the Callaway models, the analysis of lattice thermal conductivity in Holland's model explicitly considers the contribution by both the transverse and longitudinal phonons.

a. Isotope scattering

$$\tau_I^{-1} = A\omega^4$$

b. Boundary scattering

$$\tau_B^{-1} = \upsilon_B / FL_0$$

The speed of sound is defined as the average phonon velocity $\upsilon_B^{-1} = (1/3)\left(2\upsilon_T^{-1} + \upsilon_L^{-1}\right)$. T , L represents the transverse and longitudinal acoustic phonons respectively. F is the specularity parameter introduced for partially diffusive boundary scattering.

The expressions of isotope scattering and boundary scattering in the Holland model are essentially the same as those in the Callaway model, except that the boundary scattering is not fully diffusive in the Holland model.

The Holland model attempts to capture the high-temperature ($T > 0.1\theta_D$) characteristic of the thermal conductivity behavior. Therefore, the expressions for the three-phonon normal and Umklapp processes are modified from the Callaway model.

c. Three-phonon normal process

$$\tau_{N,T}^{-1} = B_T \omega T^4 \text{ for } 0 \le \omega < \omega_1$$

$$\tau_{N,L}^{-1} = B_L \omega^2 T^3 \text{ for } 0 \le \omega \le \omega_3$$

These relaxation time expressions were derived by Herring [6] for *low- temperature longitudinal and transverse acoustic phonons*. Note that in the Callaway model, only the longitudinal acoustic phonon is considered in the normal process. Although these expressions are derived for low-temperature acoustic phonons, it is sufficient for fitting the thermal conductivities, since at high temperatures the normal process becomes negligible.

d. Umklapp scattering

$$\tau_{U,T}^{-1} = \frac{B_{U,T}\omega^2}{\sinh(x)} \text{ for } \omega_1 \le \omega \le \omega_2$$

$$\tau_{U,T}^{-1} = 0 \text{ for } \omega < \omega_1$$

In the Holland model, the Umklapp process is absent at $\omega \le \omega_1$ (or $\theta \le \theta_1$) and only the transverse modes are considered.

Combining the scattering mechanisms, one gets

$$\tau_T^{-1} = \upsilon_B / FL + A\omega^4 + \tau_{U,T}^{-1}$$

$$\tau_L^{-1} = \upsilon_b / FL + A\omega^4 + B_L \omega^2 T^3 .$$

As stated earlier, the Holland model takes into account the contribution of thermal conductivity from both the transverse and longitudinal phonons [2]:

$$\kappa = \kappa_T + \kappa_L$$

$$\kappa = \frac{2}{3}\int_0^{\theta_T/T} \frac{C_T T^3 x^4 e^x (e^x-1)^{-2} dx}{\tau_T^{-1}} + \frac{1}{3}\int_0^{\theta_L/T} \frac{C_L T^3 x^4 e^x (e^x-1)^{-2} dx}{\tau_L^{-1}}.$$

The thermal conductivity can be further written as

$$\kappa = \frac{2}{3}\int_0^{\theta_1/T} \frac{C_1 T^3 x^4 e^x (e^x-1)^{-2} dx}{\upsilon_B / FL + Am^4 x^4 T^4 + B_{N,T} m x T^5} + \frac{2}{3}\int_{\theta_1/T}^{\theta_2/T} \frac{C_2 T^3 x^4 e^x (e^x-1)^{-2} dx}{\upsilon_B / FL + Am^4 x^4 T^4 + \frac{B_{U,T} m^2 x^2 T^2}{\sinh(x)}} +$$

$$\frac{1}{3}\int_0^{\theta_L/T} \frac{C_L T^3 x^4 e^x (e^x-1)^{-2} dx}{\upsilon_B / FL + Am^4 x^4 T^4 + B_{N,L} m^2 x^2 T^5}$$

$i = T, L;\ x = \hbar\omega / k_B T;\ \theta_i = k_B \omega_i / \hbar;\ C_i = \left(k_B / 2\pi^2 \upsilon_i\right)\left(k_B / \hbar\right)^3.$

Assumption: In the Holland model, the transverse acoustic phonon is assumed to have three constant velocities depending on the phonon frequency range - i.e., the transverse phonon has a constant velocity at low frequencies $\omega < \omega_1$, and the velocity decreases abruptly and remains constant between ω_1 and ω_2. For phonons with frequencies above ω_2 the phonon velocity is zero.

In summary, the Holland model considers the contribution of thermal conductivity both from the longitudinal and the transverse phonons. It also applies two averaged phonon group velocities to crudely describe the phonon dispersions. Distinct from the Callaway model, the Holland model uses different expressions for the relaxation mechanisms. Overall speaking, the Holland model captures the thermal conductivity characteristics better than the Callaway model at higher temperatures.

Following Callaway and Holland, there have been several modifications to the thermal conductivity model. These modifications are aimed to better capture the temperature dependence over a broader range. Basically, the focus of the later work has been primarily on achieving a better description in the phonon dispersions rather than developing new thermal conductivity models.

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C h a p t e r 2

HEAT TRANSPORT IN SILICON NANOWIRES AND THE SILICON NANOWIRE THERMOELECTRICS

(Parts of this chapter are reproduced with permission from: Boukai, A. I.; Bunimovich, Y.; Tahir-Kheli, J.; Yu, J.-K.; Goddard, W. A.; Heath, J. R. Nature *451*, 168 - 171, **2008**)

The focus of this chapter is on the experimental results of the thermal conductivity of silicon nanowires and the thermoelectric performance of silicon nanowires. A quick overview of the thermoelectric phenomenon is given in the beginning of the chapter to address the critical role that semiconductors with ultra-low thermal conductivities play in this field.

2.1 Introduction

It's been over a century since the first discovery of thermoelectricity by Seebeck [1] in the 1820s. Thermoelectric materials convert temperature gradient into electrical power and vice versa. Moreover, thermoelectric devices are solid-state particle exchange devices, which require neither moving parts nor the use of environmentally harmful chemicals. However, the thermoelectric materials find only niche applications mainly because of their low efficiency. Before the year 2000, the most efficient thermoelectric material the Be_2Te_3 and its alloys with Sb or Se [2], with an efficiency just 10 percent of the Carnot engine operating at room temperature. The most efficient thermoelectric material researchers have found to date is the nanostructured thin-film superlattices of Be_2Te_3 and Sb_2Te_3 [3].

The efficiency of the thermoelectric materials is commonly described by the thermoelectric dimensionless figure-of-merit [4]

$$ZT = \frac{S^2 \sigma T}{\kappa} \text{. (2.1)}$$

S is the thermopower (or Seebeck coefficient) and has the unit volts/Kelvin; σ is the electrical conductivity and κ represents the thermal conductivity of the material. ZT is related to power efficiency by equation **2.2**. When $ZT \to \infty$, the efficiency approaches the Carnot limit.

$$\eta = \frac{\Delta T}{T_{Hot}} \frac{\sqrt{1+ZT}-1}{\sqrt{1+ZT}+\frac{T_{Cold}}{T_{Hot}}} \textbf{ . (2.2)}$$

It is obvious from equation **2.1** that a high ZT thermoelectrics is capable of generating large electromotive force from a small temperature gradient, i.e., large Seebeck coefficient; in addition, a good thermoelectrics should at the same time be a good electrical conductor in order to minimize the heat loss by Joule heat. In terms of heat transport, a good thermoelectric material is a good thermal insulator, i.e., the thermal conductivity should be low so that the temperature gradient can be sustained. However, materials that meet all three of the criteria are yet to be found. The reason lies in the fact that these three material parameters are inter-correlated. Modifying one of the parameters would result in adverse effects on the other two. For instance, increasing charge carrier concentration could readily enhance the electrical conductivity of semiconductors. However, these carriers not only carry charges but also act as heat transporters. As the number of charge carriers increases, the thermal conductivity of the material system is also raised. Wiedemann-Franz law describes the ratio of the electrical conductivity and the thermal conductivity contributed by charge carriers with a constant consisting of the Lorenz number (L) and temperature (T) (equation **2.3**). Such adverse effect is particularly discernible in most metals and highly doped semiconductors material systems, where the dominant current and heat transport medium is the charge carriers [5].

$$\sigma / \kappa_e = LT \textbf{ . (2.3)}$$

In semiconductors, lattice vibrations or phonons are the dominant contributors to heat transport [6-8], indicating that interfering with the phonon dynamic could effectively lead to a suppressed thermal conductivity. Debye suggested that, in the gas-kinetic model, the heat transport in an elastic medium travels with the sound velocity υ and mean-free-path ℓ:

$$\kappa = \frac{1}{3} C_v \upsilon \ell \,. \quad \textbf{(2.4)}$$

Nanostructures with one or more dimensions smaller or comparable to the phonon mean-free path are expected to greatly influence the phonon dynamics through boundary scattering [2]. In addition, phonon mean-free path ℓ_{ph}, in general, has a characteristic length scale much larger than that of the charge carriers ℓ_e. Take single crystalline silicon for example, $\ell_{ph} \sim$ 300 nm $\gg$ $\ell_e \sim$1-2 nm [9]. Such length scale difference permits nano-structuring a strategy to reduce thermal conductivity without modifying the electronic transport properties. In other words, it provides an efficient route to decouple the thermal conductivity and the thermoelectric power factor ($S^2\sigma$).

In this chapter, thermal conductivities of silicon nanowires with crosssections 10 nm x 20 nm and 20 nm x 20 nm as well as their thermoelectric power factors, are investigated experimentally. Silicon nanowires are found to exhibit ZT as high as 1.2 at 200K. On several nanowire samples with 10 nm x 20 nm cross-section, thermal conductivity lower than the amorphous limit is also observed. The fabrication methods, measurement methodology, and results are discussed in the following sections followed, by a short

review of the recent theoretical studies on the thermal transport mechanism in silicon nanowires.

2.2 Device Fabrication

The silicon nanowires are fabricated by the superlattice nanowire pattern transfer technique (SNAP [10,11], Figure 1). In short, the process starts from a GaAs/AlGaAs superlattice, the GaAs layers are then selectively etched back by NH_4OH/H_2O_2 water solution ($V_{98\%NH4OH}$:$V_{30\%H2O2}$:V_{H2O} = 1:20:300) resulting in a comb-like structure. Next, Pt metal is deposited onto this structure by electron beam-assisted physical vapor deposition (PVD). Separately, silicon-on-insulator (SOI) wafers from which the nanowires are made were prepared. The SOI is pre-oxidized by thermal oxidation and thinned down by the removal of the oxide layer with buffered oxide etchant (BOE; 49%NH_4F, 51%HF). The starting SOI thickness and the thermal oxidation process (dry oxidation at 1000 °C) defines the final SOI thickness. The SOI wafers are either boron-doped or phosphorus-doped by thermally driven diffusion doping process. The doping concentration is controlled by the annealing temperature and confirmed by four-point sheet resistance measurement. Typically, the wafer can be boron-doped to $5x10^{19}$ cm^{-3} with the annealing temperature of 850 °C and phosphorus-doped to $3x10^{19}$ cm^{-3} at 950 °C. The superlattice master is then dropped on the epoxy-coated (by spin coating) p-type or n-type SOI, followed by curing the epoxy at 180 °C for 45 minutes. The superlattice master is then released by the phosphoric/H_2O_2 etching solution. The platinum metal wire array is left on top of the wafer and serves as the etching

mask after the superlattice removal. Directional CF_4 plasma dry etching is utilized to transfer the pattern into the SOI. The plasma etching is performed on the Plasmtherm SLR 710 reactive ion etcher. A CF_4/He gas mixture with a flow rate of 20 sccm/30 sccm is introduced into the chamber. The plasma is ignited at 40 MHz radiofrequency with a power of 40 watts. The gas pressure is controlled at 10 mtorr. The DC bias is about 80 volts. The etching process is monitored by endpoint detection with the application of laser interferometry. Lastly, the platinum is removed by aqua regia solution (HNO_3/HCl). The width and the spacing of the resulting wires are pre-determined by the thickness of the AlGaAs layer and the GaAs layer, respectively. Figure 2 shows the highly uniform high-density silicon nanowires made by the SANP technique.

After the wires are made, heaters and contact electrodes are defined by e-beam lithography with a 3% polymeric e-beam resist PMMA/chlorobenzene solution. Ti (20 nm)/Pt (180 nm) and Ti (20 nm)/Pt (100 nm) are deposited by e-beam PVD for the heaters and electrodes, respectively. For the purpose of measuring the thermal conductivity of the wires, the device is further suspended over an 800 mm x 800 mm hole. Briefly, a 1600 mm^2 area of oxide was removed by CF_4 plasma with the device active region protected by 6% PMMA. Next, XeF_2 gas was introduced to isotropically etch the underlying silicon handle layer. See Figure 3.

2.3 Measurement

2.3.1 Electrical conductivity/resistivity measurement

Electrical conductivities of the nanowires are measured by a four-point probe setup. Briefly, electrical current is sourced (Keithley 2400 source meter) through the two outer electrodes placed at the two ends of the nanowire array. The voltage drop is obtained by a voltage meter (Keithley 6500 nanovolt meter) via another inner pair of electrodes (see also Figure 3). The resistance of the nanowire array is obtained by the slope of the linear regression fit to the I-V curve. Atomic force microscope (AFM) and scanning electron microscope (SEM) measurements provide the geometric information needed for the resistivity calculation. Typically, the resistivity is about $7x10^{-4}$ Ω-cm for highly doped nanowires. Extra care is taken in order to achieve a good ohmic contact before the resistivity measurement. First, monolithic contacts are designed to increase the contact area. Secondly, the devices are briefly dipped into dilute BOE (V_{BOE}:V_{H2O} = 1:100) for a couple of seconds to remove the native oxide right before metal deposition. After metallization, the devices are subject to forming gas (N_2/H_2 = 95/5) anneal at 475 °C for 5 minutes to anneal the contact as well as hydrogen terminate the silicon surface.

2.3.2 Seebeck coefficient measurement

Seebeck coefficient measurements require accurate detection of the voltage drop, ΔV, and the temperature difference, ΔT, across the nanowire arrays when the heater is turned on. ΔV could be easily obtained via the two inner electrodes and a voltage meter. However, to determine ΔT is less straightforward. Two platinum resistive thermometers (same as the two electrodes for I-V measurements) are used for this purpose. Specifically, the resistances of the thermometers were measured as a function of heater power. From the

linear regression, we get the ratio ΔR/ΔW. Another set of resistance measurements is carried out as a function of the cryostat temperature, yielding the ratio ΔR/ΔT. The temperature difference across the wire array per unit heater power could be readily obtained by multiplying these two values. Thus, ΔT across the wires can be deduced once the heater power is known. (equation **2.5**). Typically, the temperature difference across the wire array is less than 5K.

$$\Delta T = W\left(\frac{\Delta R_H \Delta T_H}{\Delta W \Delta R_H} - \frac{\Delta R_C \Delta T_C}{\Delta W \Delta R_C}\right). \textbf{(2.5)}$$

2.3.3 Thermal conductivity measurement

The thermal conductivity of the sample is measured based on a similar method developed by Shi et. al. [12]. Consider the equivalent thermal circuit of the device platform (Figure 4), at steady state, the heat source to the system is the heater (Q_h, heat generated from the serpentine part) plus the two current source leads of the heater ($2Q_L$). Ignoring the heat loss due to air conduction (which is valid when the system is at a vacuum condition of $< 5\text{x}10^{-6}$ torr) and radiative transfer, the heat transferred from the hot to the cold end through the sample should be equal to the heat dissipated to the environment via the leads at the cold end. Thus,

$$Q_s = K_s \times (T_h - T_c) = K_L \times T_C + \left(\frac{1}{K_{ox}} + \frac{1}{K_h}\right)^{-1} \times T_c = \left(K_L + \frac{K_{ox} K_h}{K_{ox} + K_h}\right) T_c. \textbf{(2.6)}$$

Also, due to the temperature difference between the hot side and the environment, heat could also dissipate into the environment from the leads on the hot side.

$$Q_L + K_L T_h + (\frac{1}{K_{ox}} + \frac{1}{K_h})^{-1} T_h = Q_L + (K_L + \frac{K_{ox} K_h}{K_{ox} + K_h}) T_h . \quad \textbf{(2.7)}$$

Obeying energy conservation,

$$Q_L + (K_L + \frac{K_{ox} K_h}{K_{ox} + K_h})(T_c + T_h) = Q_h + 2Q_L \quad \textbf{. (2.8)}$$

where $K_b \equiv K_L + \frac{K_{ox} K_h}{K_{ox} + K_h}$, is the total thermal conductance of the leads on each side.

From equation **2.8**, we get

$$K_b = \frac{Q_h + Q_L}{T_c + T_h} \quad \textbf{. (2.9)}$$

Combining equations **2.9** and **2.6,**

$$K_s = K_b \frac{T_c}{T_h - T_c} \quad \textbf{. (2.10)}$$

The thermal conductance of the sample (K_s) is thus obtained by measuring Q_h, Q_L, T_h, and T_c. Since the nanowire array is fabricated on a thin oxide substrate, differential measurement is performed to determine the thermal conductance of the silicon nanowires. Basically, the thermal conductance is measured before and after the nanowire array is selectively etched with XeF_2 gas. The thermal conductance of the nanowire array can be retrieved by the subtraction of the two values, $K_{(ox+NWs)} - K_{ox} = K_{NWs}$. Finally, the thermal conductivity, κ_{NW}, of the wires is calculated by taking the device geometry into account.

2.4 Results and Discussions: p-Type Nanowires

2.4.1 Electrical conductivity

Figure 5 shows the electrical conductivity of p-type nanowires with different wire widths and doping concentrations. The bulk device measured here is a film with 520 nm (width) x 1 mm (length) x 35 nm (height). As one can clearly see, the electrical conductivity of the 20-nm-wide nanowires is about 90% of the bulk-like film (red curve). The bulk-like electrical conductivity could be attributed to the fact that the carrier mean-free path is an order of magnitude smaller than the critical dimension of the sample, hence, the increase of surface-to-volume ratio by scaling down from bulk to 20 nm wires does not adjust the scattering mechanism from similarly processed bulk samples. The 10-nm-wide wires, however, have much smaller electrical conductivity than the bulk (~ 10%). The reason could be attributed to lower wire quality, i.e., more surface defects and surface roughness that are inherent in the narrower wire systems.

2.4.2 Thermal conductivity

The thermal conductivity (Figure 6) drops sharply with shrinking NW cross section; a two orders of magnitude decrease in thermal conductivity relative to the bulk is observed for the 10-nm-wide NWs. For all NWs measured, S/κ ratio leads to a significant enhancement of ZT relative to the bulk. The higher resolution thermal conductivity measurements on the 10 nm and 20 nm devices reveal that the thermal conductivity of silicon nanowires could be lower than the amorphous limit of silicon, κ_{min} =0.99 W/m-K (Figure 6).

2.4.3 The amorphous limit

In 1987, D. G. Cahill and R. O. Pohl found experimentally that *the minimum phonon mean-free-path is one half of a wavelength*. In the high temperature limit (i.e., shortest wavelength), the wavelength is twice the average inter-atomic distance. As a result, the minimum thermal conductivity of a material is reached when the mean-free-path equals the average inter-atomic distance [13]. Such situation is in essence the Einstein's energy random walk model, which states that heat transport in crystals is a random walk process of thermal energy between neighboring atoms oscillating with random phases. (G. A. Slack in 1979 proposed that Einstein's random walk model represents systems with minimum thermal conductivities. At the time, Slack assumed the minimum mean-free-path to be the Debye wavelength.) Disordered crystals exhibit thermal conductivities approaching to values predicted by Einstein's model, lower values have yet to be demonstrated by introducing higher disorder. This lower-limit of thermal conductivities is called the amorphous limit [14,15].

It is worth-noting that the phonons are described by the Debye model using bulk sound speeds with no optical modes. The l/2 value is an order-of-magnitude estimate and is difficult to determine precisely. Also, κ_{min} is proportional to the transverse and longitudinal acoustic speeds of sound. These are reduced in our nanowires at long wavelengths because the modes become one dimensional, particularly in the 10 nm nanowires. The ratio of the one-dimensional to two dimensional longitudinal speeds of sound is $[(1+n)(1-2n)/(1-n)]^{1/2}=0.87$, where n=0.29 is the Poisson ratio [16] of Si. The transverse acoustic speed goes

to zero at long wavelength because $\upsilon \propto k^2 d$ where d is the nanowire width. Therefore, the bulk $\kappa_{\min}$ estimate in the amorphous limit is invalid for our nanowires and values smaller than $\kappa_{\min}$ are attainable. However, a more detailed *ab initio* study is required to get a further understanding of how the thermal conductivity is lower than the amorphous limit.

4.2.4 Thermopower of the silicon nanowires

The square value of the thermopower of various wires as a function of temperature is shown in Figure 7. Most of the moderately doped p-type nanowires showed peaks around 200K. Similar peaks have been observed in some of the metals and lightly doped semiconductors at temperatures lower than 50K [17]. Such a phenomenon is explained by the phonon-drag mechanism.

The thermoelectric power contains two main sources: the diffusion thermopower caused by the diffusion of charge carriers, S_d, and thermopower generated by incorporating the momentum transfer between the phonons and the charge carriers, or phonon-drag thermopower, S_{ph}.

$$S = S_d + S_{ph}. \quad \textbf{(2.11)}$$

The diffusion thermopower is described by Mott's formula [17,18], equation **2.12,** and is linearly dependent on T.

$$S_d = \frac{\pi^2}{3}\left(\frac{k_B^2 T}{e}\right)\left(\frac{d\ln\sigma(\varepsilon)}{d\varepsilon}\right). \quad \textbf{(2.12)}$$

2.4.5 Phonon-drag

When temperature gradient exists in the system, not only charge carriers but also phonons carry thermal energy and migrate from hot to cold. If the charge carrier-phonon interaction is sufficiently large, charge-carriers could be swept along with the phonons. This is basically the origin of the phonon-drag thermopower.

At sufficiently low temperatures, the phonon-phonon scattering can be neglected. Assume the phonon-gas model, the amount of pressure exerted on the charge carriers by the phonon gas through collision, is

$$p = \frac{1}{3} U_V(T). \quad \textbf{(2.13)}$$

$U_V(T)$ is the phonon internal energy per unit volume, or phonon energy density. A temperature gradient dT/dx also creates a pressure gradient of the phonon gas dp/dx. The additional electric field resulting from the momentum transfer between the charge carriers and phonons under such temperature/pressure gradient will equal the force exerted on the charge carriers by the phonon stream at steady-state, i.e.,

$$Ne\varepsilon_x + F_x = 0$$

$$Ne\varepsilon_x - \frac{1}{3}\frac{dU}{dT}\frac{dT}{dx} = 0$$

$$\frac{\varepsilon_x}{dT/dx} = \frac{1}{3}\frac{C_{ph}}{Ne}.$$

Therefore, the phonon-drag thermopower can be shown as [17]

$$S_{ph} = \frac{1}{3}\frac{C_{ph}}{Ne} \quad \textbf{. (2.14)}$$

C_{ph} is the volume lattice specific heat, N is the number of conducting carriers per unit volume, and e represents the charge per carrier. Equation **2.14** predicts what may be called the "full phonon-drag" at low temperature. "Full" refers to the assumption that the phonon momentum is transferred completely to charge carriers. Accordingly to Debye's prediction on the temperature dependence of the volume specific heat at low temperature $C_{ph} \propto T^3$ (Chapter 1), the phonon-drag thermopower also inherits such temperature dependence $S_{ph} \propto T^3$ at $T \to 0$.

Combining this and the previously mentioned T linear dependent on the diffusion thermopower, we can come to an expression that predicts the thermopower value as

$S = S_d + S_{ph} = aT + bT^3$. **(2.15)**

(a and b are constants.)

At higher temperature, to a first approximation, equation **2.14** should be modified by a correction factor $\tau_p / \left(\tau_p + \tau_{pe}\right)$, since other phonon scatterings have to be taken into account.

$$S_{ph} = \frac{C_{ph}}{3Ne} \frac{\tau_p}{\tau_p + \tau_{pe}}$$

τ_p is the overall relaxation time regarding other phonon scattering processes. τ_{pe} is the relaxation time of phonon-charge carrier scattering. At sufficiently high temperature $T \geq \theta_D$, $C_{ph} \approx 3N_0 k_B$ (Dulong-Petit limit; Chapter 1). N_0 is the number of atoms per unit volume. Thus,

$$S_{ph} \propto \frac{k_B}{e}\frac{\tau_p}{\tau_p + \tau_{pe}} \quad \textbf{. (2.16)}$$

In such temperature, τ_{pe} is a constant and $\tau_p \propto 1/T$. Therefore, $S_{ph} \propto 1/T$.

As in the case of three-phonon scatterings, the electron-phonon scattering can also be categorized into normal processes (momentum conserved) and Umklapp processes (reciprocal lattice vector involved). Either type could give rise to phonon-drag thermopower, however, large momentum change involved in the Umklapp process could result in larger phonon-drag thermopower. In addition, the momentum reversal nature of the process could also create S_{ph} with opposite sign. The chance of the occurrence of the electron-phonon Umklapp process depends strongly on the distance between the distorted Fermi surface and the Brillouin zone boundary (or the relative magnitude of the electron wave vector and the reciprocal lattice vector) and can be characterized by $\exp(-\theta^*/T)$. θ^* represents the characteristic temperature of the spacing [17].

As the temperature increases, the anharmonicity becomes non-negligible. The number of phonons with energy q is given by Bose-Einstein equation,

$$N = \frac{1}{e^{\theta/T} - 1} \quad \textbf{. (2.17)}$$

At T >> q, $1/t_{ph} \sim N \sim T$. Hence, $S_{ph} \sim 1/T$. In other words,

$$S = S_d + S_{ph} = aT + b/T \quad \textbf{. (2.18)}$$

Whereas at medium temperature range, 50K < T << q for metal and 200K < T << q for the p-type nanowires, the full Bose-Einstein equation should be applied. Thus,

$$S = aT + b\left[e^{\theta/T} - 1\right] \quad \textbf{. (2.19)}$$

Taking q=640K and fitting equation **2.19** to the experimental thermopower curve with a, b as parameters, we find that the linear term corresponds well to the thermopower of the bulk film, as well as to the one of the highly doped p-type nanowires that showed only the diffusion thermopower. See Figure **8**. This directly proves that the thermopower peak shown in the p-type devices is due to the phonon-drag effect.

5. Results and Discussions: N-Type Nanowires

5.1 Electrical conductivity

The electrical conductivity of the 20-nm-wide n-type nanowires also has a bulk-like value. Figure 9 shows the conductivity curves for three nanowire systems with different dopant concentrations. The conductivities in these systems are about 98%, 80%, and 70% of the bulk value, respectively.

5.2 Inter-valley scattering mechanism

Figure 10 plots the thermopower of the n-type 20-nm-wide nanowires as a function of temperature. No obvious phonon-drag was observed in the temperature window from 300K down to 100K. The theory that can account for this phenomenon is elaborated as follows. For indirect band-gap semiconductors, such as Si and Ge, the electrons in these materials are located in degenerate conduction band minima at the proximity of the Brillouin zone edge. In addition to intra-band scattering by phonons, electrons can be scattered from one degenerate valley to another via inter-valley scattering (Figure 11). The inter-valley

scattering process was found more important than the intra-valley scattering in relaxing the momentum and energy of conduction electrons [19, 20]. Phonons responsible for the intervalley scattering (either g or f process) are those at the Brillouin zone edge with large wave vectors and short lifetimes. Moreover, these phonons with large momentum render the charge carrier-phonon scattering mostly to Umklapp process, which is adverse to phonon-drag. Therefore, if the dominant electron-phonon scattering mechanism in n-type nanowire is the inter-valley scattering, one would have to cool the temperature down to at least less than 50K to be able to observe the phonon-drag, due to the fact that these phonons have substantially shorter wavelength than those in the p-type scattering events.

6. Conclusion

From the current results, we find that: 1) The electrical conductivity in the nanowires is bulk-like. 2) Phonon drag effect causes an approximately four fold increase in the thermopower as compared to bulk Si. 3) There is an ultra-small thermal conductivity, as small as 0.76 W/m-K for 10 nm SiNWs, possibly due to the dimensional cross over in this systems. All together with these discoveries, we are able to show the thermoelectric figure-of-merit of 1.2 (about 100 times larger than its bulk counterpart) with p-type silicon nanowires. The thermoelectric properties of n-type silicon nanowires are also investigated. Electrical and thermal conductivity similar to those p-type nanowires are observed. However, no phonon-drag is detected in n-type nanowires due to the dominant intervalley electron-phonon scattering process.

Further parameter optimization: by doping, geometry, composition (for instance, SiGe), phonon engineering, charge carrier scattering mechanisms, the birth of a silicon-based system with a ZT equal to 3, and efficiency comparable to conventional refrigerators can be expected in the near future.

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Figure 1.

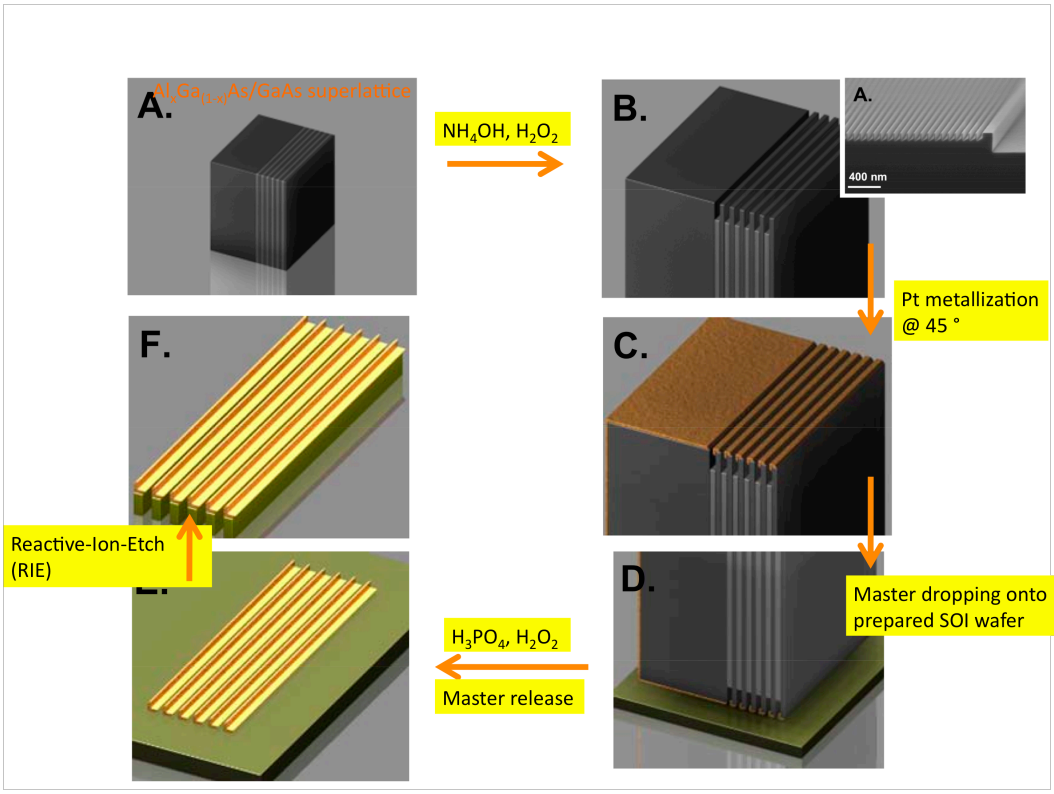
A.
$Al_xGa_{(1-x)}As$/GaAs superlattice
NH_4OH, H_2O_2
B.
A.
400 nm
Pt metallization
@ 45 °
C.
D.
Master dropping onto
prepared SOI wafer
H_3PO_4, H_2O_2
Master release
F.
Reactive-Ion-Etch
(RIE)

Figure 2.

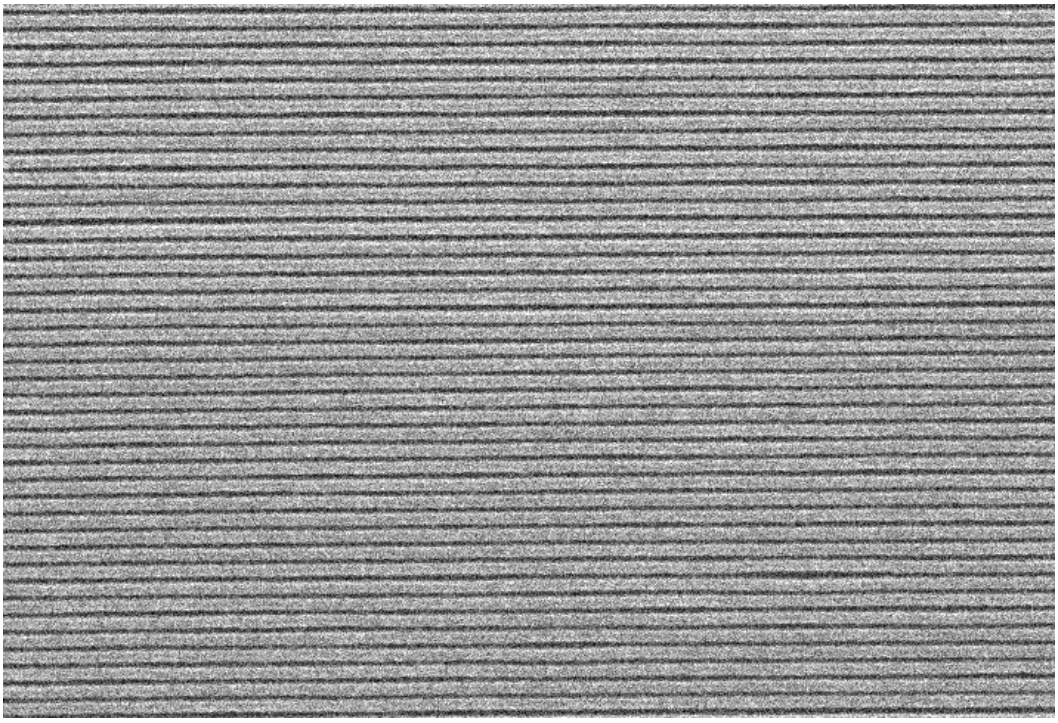

Figure 3.

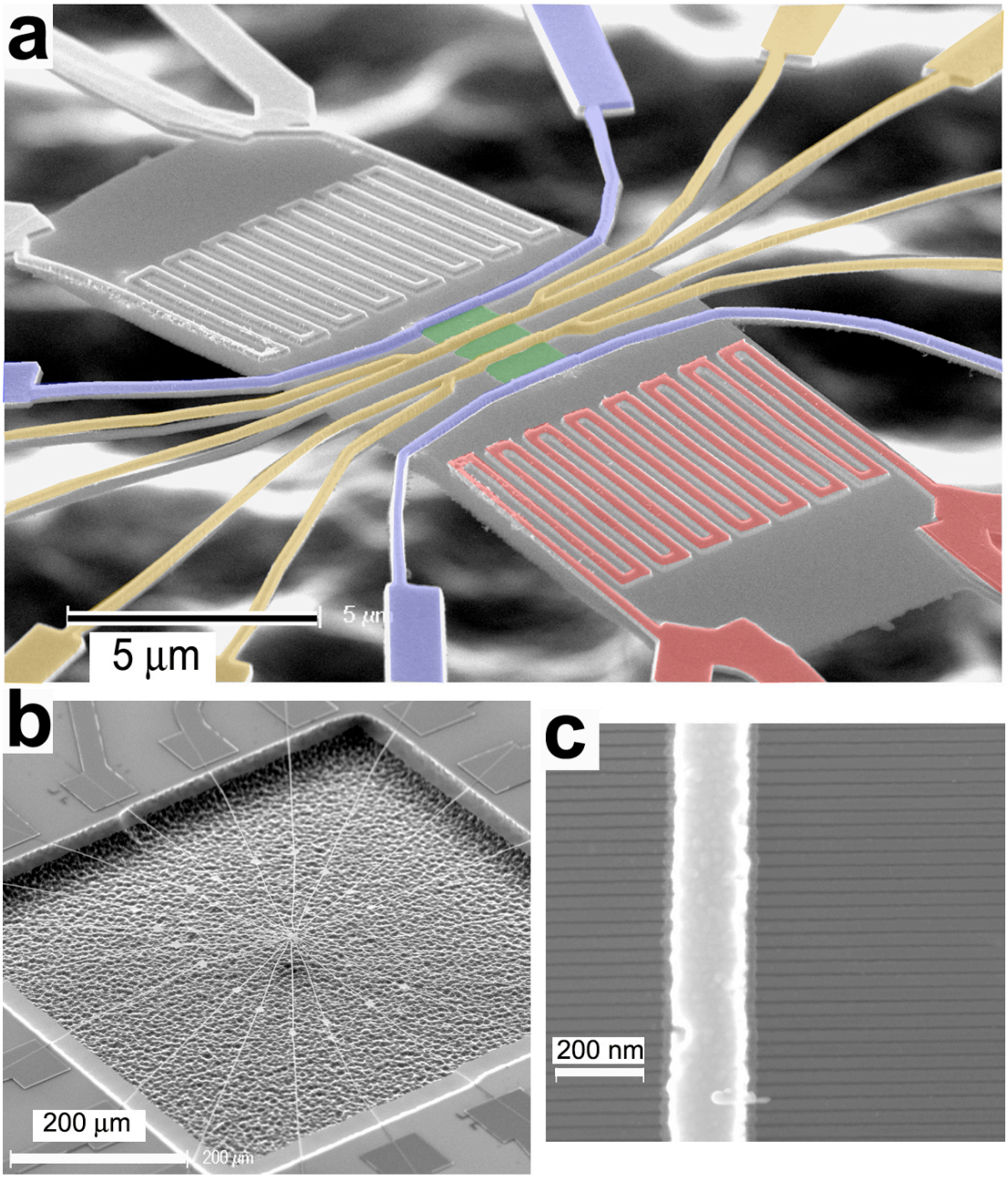

Figure 4.

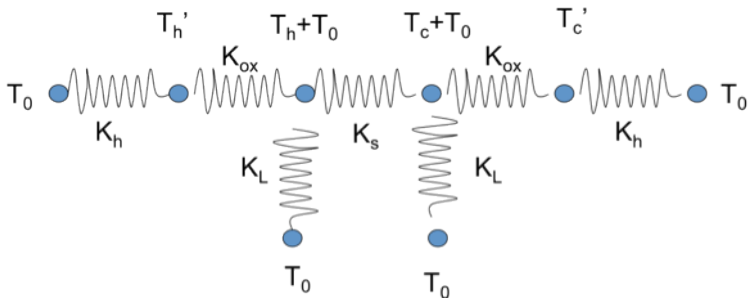

Figure 5.

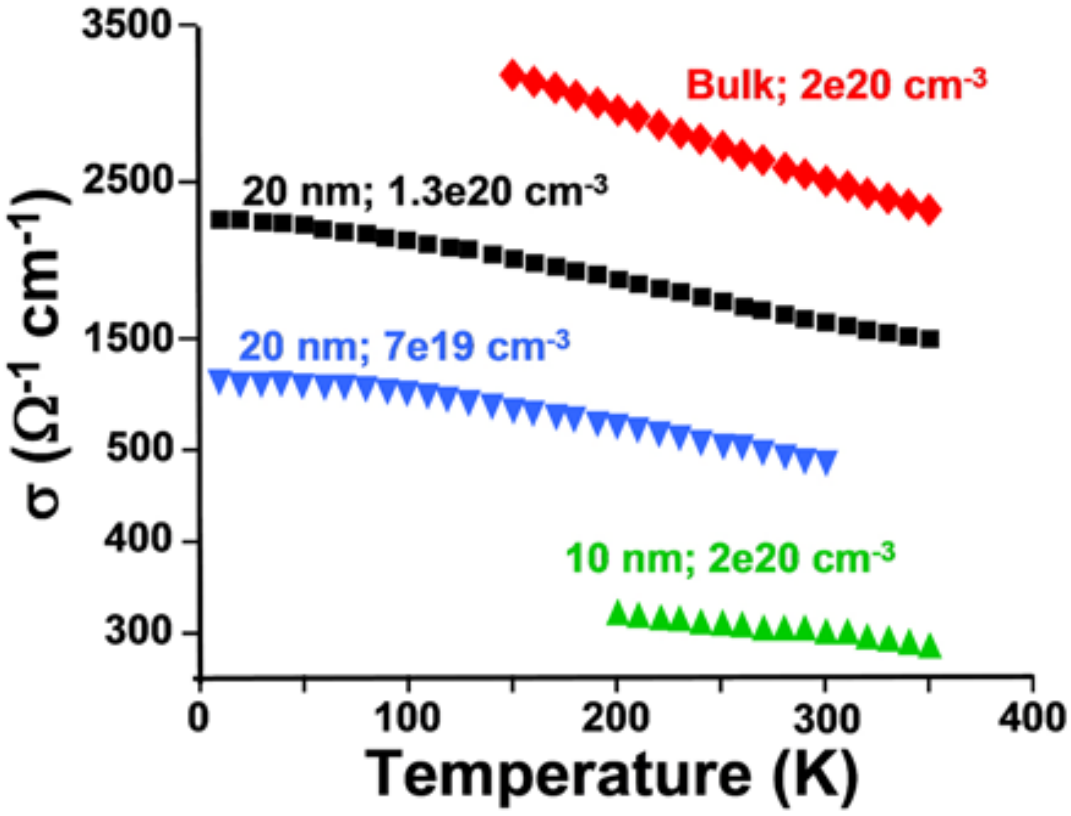

Figure 6.

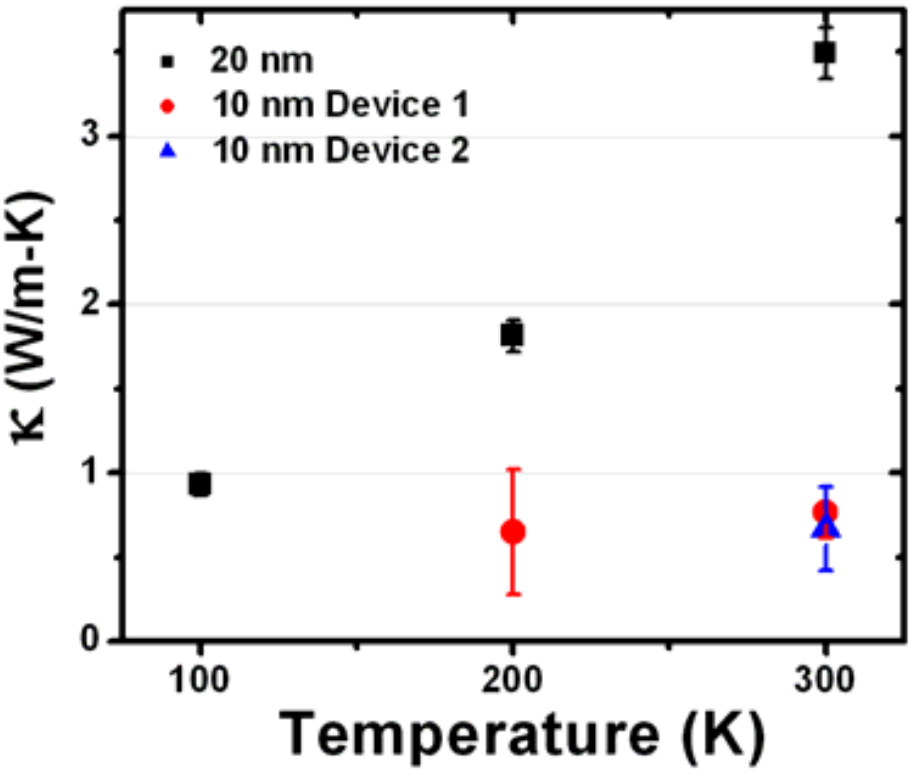
20 nm
10 nm Device 1
10 nm Device 2
κ (W/m-K)
0
1
2
3
100
200
300
Temperature (K)

Figure 7.

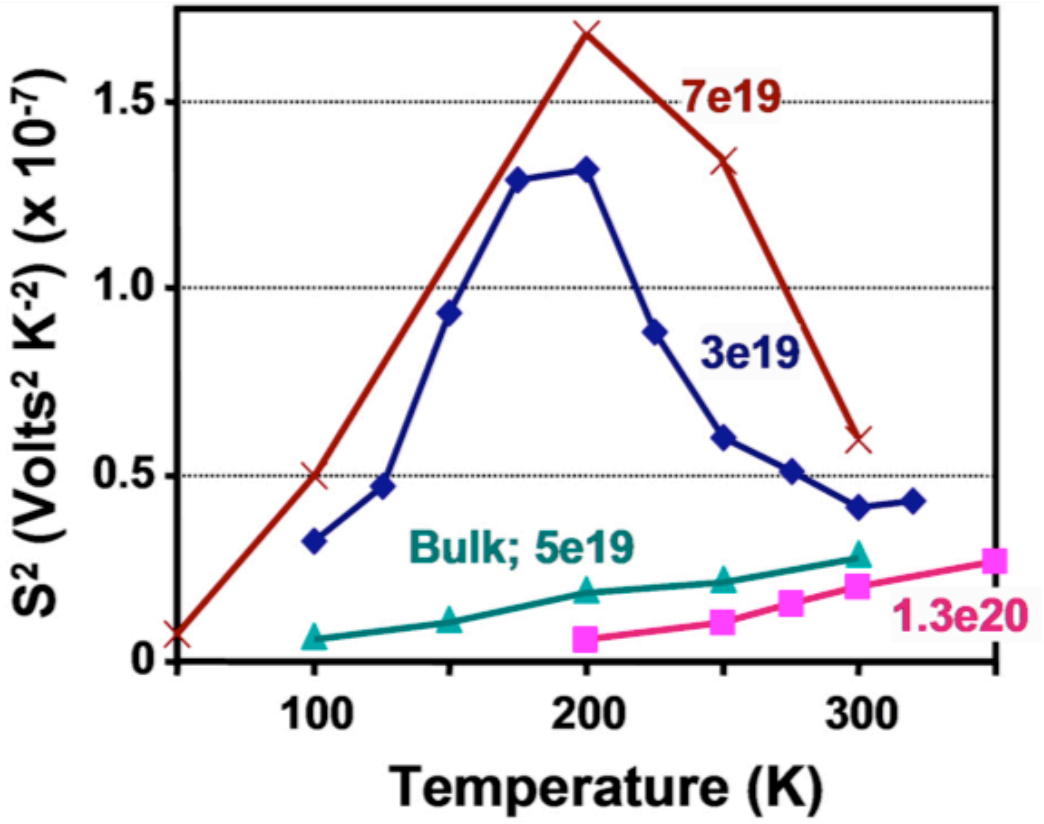
S² (Volts² K⁻²) (x 10⁻⁷)
1.5
1.0
0.5
0
100
200
300
Temperature (K)
7e19
3e19
Bulk; 5e19
1.3e20

Figure 8.

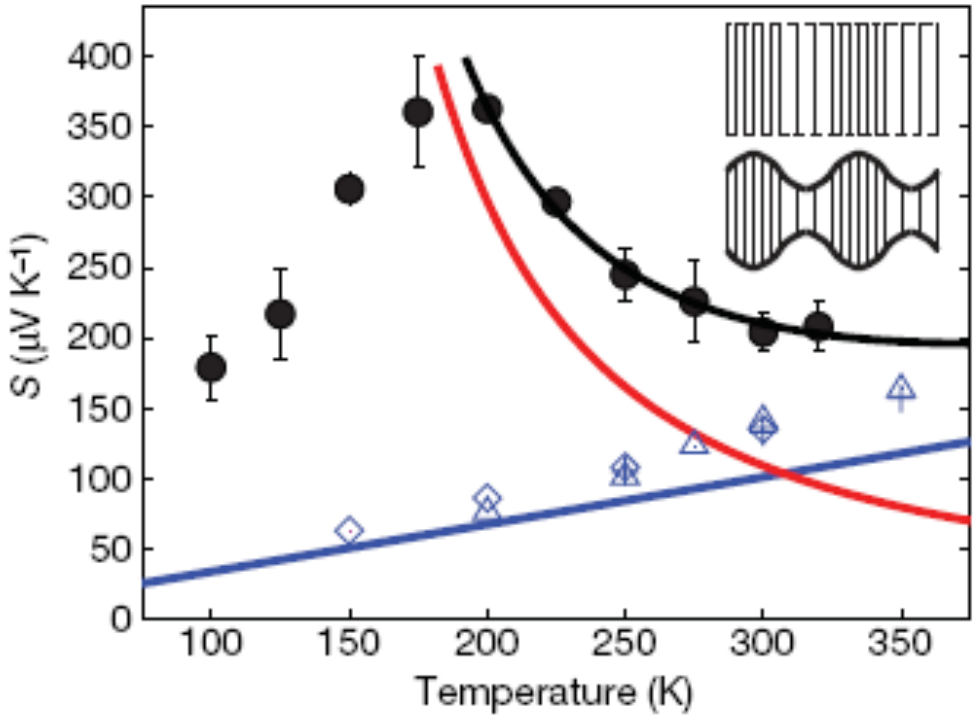
S (μV K-1)
400
350
300
250
200
150
100
50
0
100
150
200
250
300
350
Temperature (K)

Figure 9.

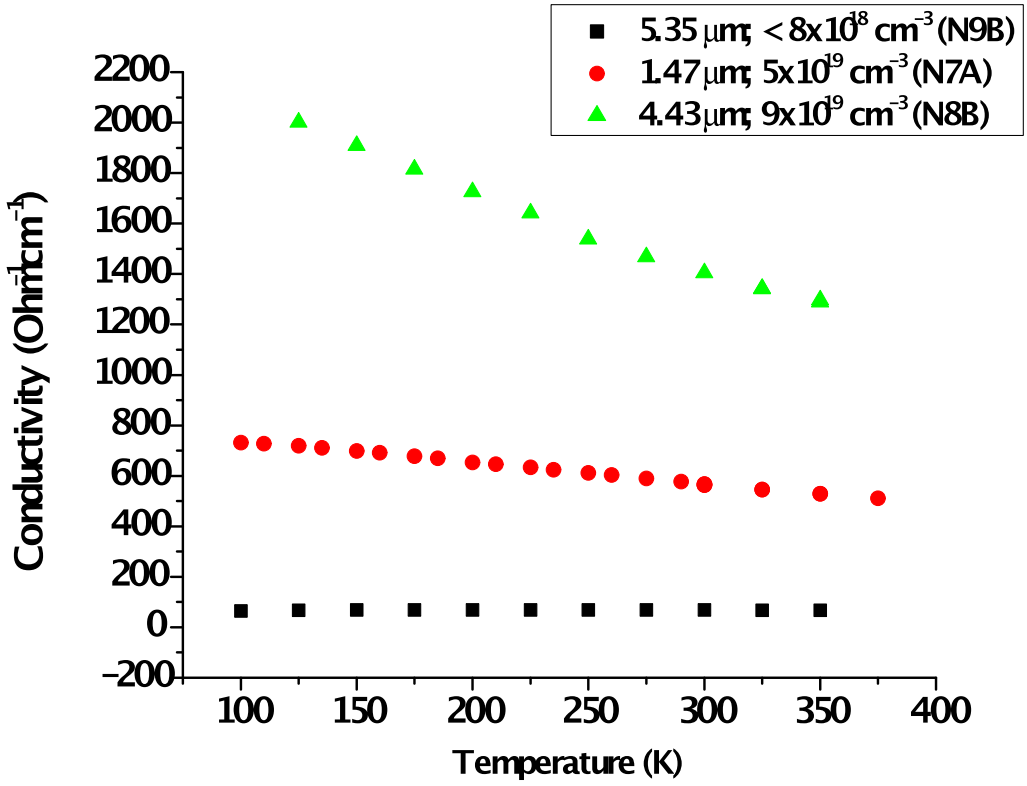
5.35 μm; < 8x10^18 cm^-3 (N9B)
1.47 μm; 5x10^19 cm^-3 (N7A)
4.43 μm; 9x10^19 cm^-3 (N8B)
Conductivity (Ohm^-1cm^-1)
2200
2000
1800
1600
1400
1200
1000
800
600
400
200
0
-200
100
150
200
250
300
350
400
Temperature (K)

Figure 10.

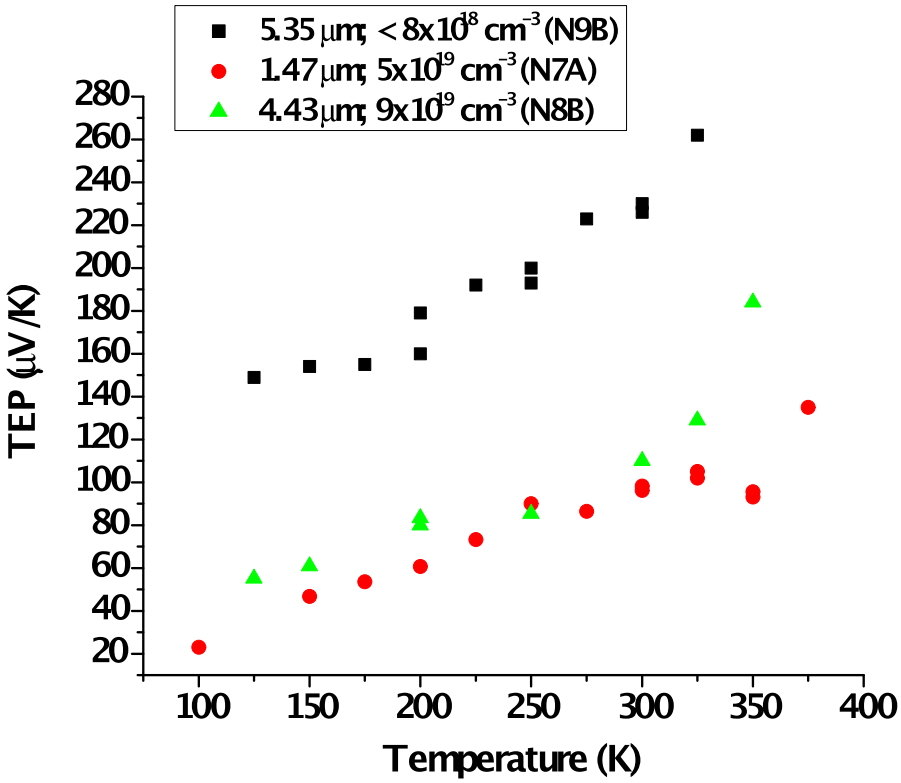
5.35 μm; < 8x10^18 cm^-3 (N9B)
1.47 μm; 5x10^19 cm^-3 (N7A)
4.43 μm; 9x10^19 cm^-3 (N8B)
TEP (μV/K)
Temperature (K)
280
260
240
220
200
180
160
140
120
100
80
60
40
20
100
150
200
250
300
350
400

Figure 11.

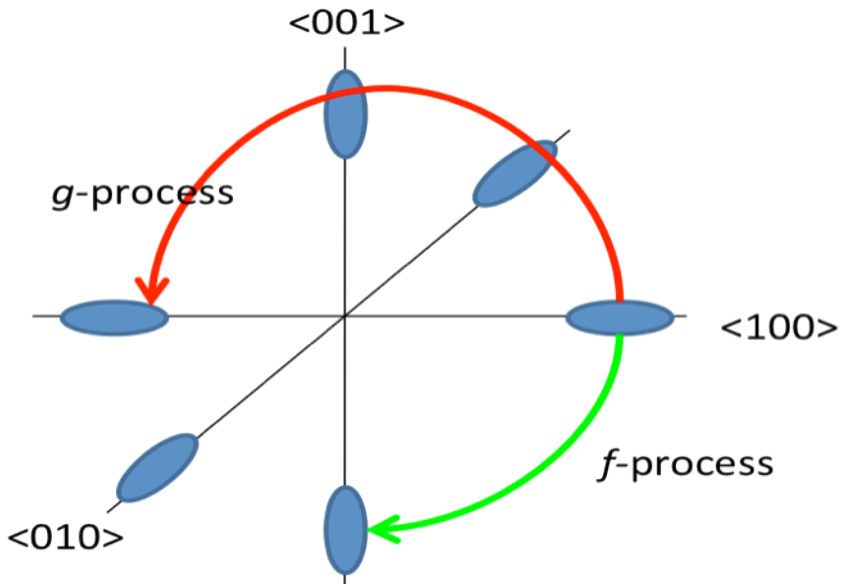

Figure Captions

Figure 1. Superlattice Nanowire Pattern Transfer

(A) An imaginary figure depicting the $Al_xGa_{1-x}As/GaAs$ superlattice. (B) The $Al_xGa_{1-x}As$ layer is selectively etched back by NH_4OH solution creating a comb-like structure (inset). (C) The superlattice is metalized by e-beam assisted physical vapor deposition at an angle of 45°. (D) The superlattice is dropped onto a silicon-on-insulator wafer. A epoxy-PMMA adhesion layer is pre-spun on the wafer. After positioning the superlattice master, the epoxy is cured at 180°C for 40 minutes. Then, the entire wafer is placed in a phosphoric acid solution for 4.5 hours. (E) Metal wire array is left behind on the SOI wafer after releasing the superlattice master. (F) Reactive-ion-etching is exploited at this step to transfer the metal wire pattern into the SOI.

Figure 2. Scanning electron micrograph image of a 20-nm-wide, 34-nm-pitch silicon nanowire array made by SNAP process

Figure 3. SEM images of the device

(a) This false color image of a suspended platform shows all electrical connections. The central green area is the Si NW array. The NWs are not well-resolved at this magnification. The grey region underlying the NWs and the electrodes is the 150 nm thick buried oxide (BOX) layer sandwiched between the top Si(100) single crystal film from which the NWs are fabricated, and the underlying Si wafer. The underlying Si wafer has

been etched back to suspend the measurement platform, placing the background of this image out of focus. **(b)** Low resolution micrograph of the same suspended platform. The 20 electrical connections to the heaters and various electrodes radiate outwards and support the device. **(c)** High resolution image of an array of 20 nm wide Si NWs with a Pt electrode.

Figure 4. Equivalent thermal circuit of the measurement platform

The equivalent thermal circuit of our device. T_0 denotes the cryostat temperature. T_h (T_c) is the temperature increase measured by the resistive thermometer at the hot (cold) end of the nanowire array. T_h' /T_c' is the temperature of the right (on-state)/ left (off-state) heater. K_{ox}, $K_{L,}$ K_h, and K_s represent the thermal conductance of the oxide, the thermometer leads, the heater, and the sample.

Figure 5. Temperature dependent electrical conductivity of boron-doped silicon nanowires. Representative electrical conductivity data for Si NWs and microwires; p-type doping levels are indicated. All NWs are 20nm in height.

Figure 6. Thermal conductivity of the silicon nanowires. The temperature dependence of the thermal conductivity (**κ**).

Figure 7. Thermopower of the silicon nanowires. The temperature dependence of the square of the thermopower for 20 nm x 20 nm (= 400 nm^2) Si NWs at various p-type doping concentrations (indicated on the graph).

Figure 8. Thermopower fit to equation 3.18

Thermopower calculation plotted along with experimental data (black points) from a 20-nm-wide Si nanowire p-type doped at 3 x 10^{19} cm^{-3}. The black curve is the fitted expression for the total thermopower $S_e + S_{ph}$. The red curve is the phonon contribution S_{ph} and the blue line is the electronic term S_e arising from the fit. The experimental error bars represent 95% confidence limits. The blue data points are experimental values for bulk wires (doping 2 x 10^{20} cm^{-3}; crosses), 10-nm-wide nanowires (doping 7x10^{19} cm^{-3}; diamonds), and 20-nm-wide wires (doping 1.3x10^{20} cm^{-3}; triangles) where only a linear-T electronic contribution was found. The inset shows the character of a three dimensional bulk longitudinal acoustic phonon mode (top) and a one dimensional mode when the wavelength is larger or of the order of the width (bottom). The one-dimensional mode incorporates the existence of the boundary by transverse expansion (or compression) for longitudinal compression (or expansion). The ratio of the transverse strain to the longitudinal strain is the Poisson ratio (0.29 for Si).

Figure 9. n-type 20nm silicon nanowire conductivity vs T curves. The temperature dependent electrical conductivity data of three n-type SiNWs doped at three different dopant concentrations.

Figure 10. n-type 20nm silicon nanowire thermpower vs T curves. The temperature dependent thermopower data of three n-type SiNWs doped at three different dopant concentrations.

Figure 11. Schematics of the e-ph scattering mechanisms at the conduction band minima. The constant energy surface diagram of the conduction band of silicon. The red and green curves describe the *f* and *g*-processes respectively.

C h a p t e r 3

THERMAL CONDUCTIVITY REDUCTION IN PHONONIC NANOMESH STRUCTURES

(Parts of this chapter are reproduced with permission from: Yu, J.-K.; Mitrovic, S.; Tham, D.; Varghese, J.; Heath, J. R. Nature Nanotechnology *5*, 718-721, **2010**)

Controlling the thermal conductivity of a material independent of its electrical conductivity is a goal for researchers working on thermoelectric materials for energy applications [1,2] and for the cooling of integrated circuits [3]. In principle, the thermal conductivity κ and the electrical conductivity σ, may be independently optimized in semiconducting nanostructures because different length scales are associated with the heat carrying phonons and the electrical current carrying charges. Phonons are scattered at surfaces and interfaces, so κ generally decreases as the surface-to-volume ratio increases. By contrast σ is less sensitive to decreasing nanostructure size, although, at sufficiently small sizes, it will degrade via charger carrier scattering at interfaces [4]. Here we demonstrate an approach to independently controlling κ based upon altering the phonon band structure of a semiconductor thin film via the formation of a nanomesh film. Nanomesh phononic films are patterned with periodic spacings that are comparable to or shorter than the phonon mean-free-path. The results for the nanomesh films are compared against an equivalently prepared array of Si nanowires. The nanowire array possesses a significantly higher surface-to-volume ratio, but the nanomesh structure exhibits a substantially lower thermal conductivity. Bulk-like electrical conductivity is preserved. We argue that this points

towards coherent mechanism for lowering the thermal conductivity.

3.1 Introduction

The efficiency of a thermoelectric material is inversely proportional to the thermal conductivity, κ. Nanoscale structures are being explored for both reducing κ and for enhancing and decoupling the two other relevant parameters, the electrical conductivity (σ) and the thermopower (S), from each other and from κ [1,2,3]. For reducing κ, most work has focused on enhancing phonon scattering mechanisms [1,2]. Here we experimentally demonstrate a reduction in κ through the architectural modification of a thin Si film. Two sizes of nanomesh films, a nanowire array, and a continuous thin film, were fabricated from 20-25 nm thick Si films, and fully suspended for thermal conductivity measurements. The nanomesh films are square rigid structures, with inclusions at a periodic spacing of 385 nm and 34 nm. The nanowire array was comprised of >100 28×20 nm^2 cross-section nanowires. We find that κ is reduced as a consequence of both film architecture and feature size. Comparison of κ for the 34 nm nanomesh with our reference structures indicates that architecture can contribute at least a factor of 2 reduction in κ, a result that is not readily explained by enhanced phonon scattering, but may point towards coherent mechanisms for lowering thermal conductivity. We also demonstrate the effective decoupling of electronic and thermal conductivities. Our work suggests that Si nanomesh arrays may exhibit a peak ZT>1, and our results may be generally applicable to the design of thermoelectric materials.

The values of κ measured in nanoscale systems are often compared to the thermal conductivity of the bulk amorphous material (κ_{min}) [5]; and the characteristic length scales are compared to the dominant values of the heat carrying phonon mean-free-paths Λ and wavelengths λ [6]. For bulk Si at room temperature, κ_{min}~1 W/m-K, Λ~300 nm and λ~1-2 nm. Reductions in κ, through increased boundary scattering, are realized when system dimensions are smaller than Λ, as in the case of thin films, superlattices and nanowires. Alternatively, κ may also be reduced by elastic scattering when features are comparable to λ, such as in various classes of nanostructured bulk materials [7-9]. Finally, κ may be reduced through confinement altered phonon bands when features are smaller than λ [10]. For 10-20 nm diameter Si nanowires, or for larger, surface roughened nanowires, κ is reduced by as much as two orders of magnitude relative to bulk crystalline Si and approaches κ_{min} [11-13]. The size-dependent reduction in κ occurs through the modification of scattering relaxation rates with preserved bulk-like phonon band structure. There have been proposals to use coherent phonon processes to modify the phonon band structure. For example, the use of periodic superlattice structures can influence the phonon group velocity [6]. However, scattering at the superlattice interfaces can partially or wholly mask such effects, meaning that incoherent scattering dominates the thermal properties of these systems as well [6,14-16]. Here we report that periodic, single crystal nanomesh structures, patterned at a scale where phonon band structure modifications can be observed, provide a route towards low-κ materials. We find that reductions in κ can be attributed to the nanomesh superstructure, rather than to classical size-effects. These results demonstrate

that thin-film nanoengineering provides an attractive approach for the design and fabrication of low-κ materials.

Fully suspended Si nanomesh films (Figure 1a, b) are fabricated starting from a <100> silicon-on-insulator (SOI) thin film. Electronic properties are chosen by boron diffusion doping of the initial thin film [18]. We fabricated three reference devices: (1) a Si thin film (TF); (2) an array of rectangular cross-section Si nanowires (NWA); and (3) a larger feature-size mesh that was defined by electron-beam lithography (EBM). The drawings and table of Figure 2a summarize the relevant dimensions, which were chosen to permit direct comparison of the structures. We present results on two similar nanomesh devices (NM1 and NM2), with the same periodicity and thin film thickness, and a small difference in the size of holes (see table of Figure 2a). The thickness T is nearly identical for all devices, and the nanowire cross-section areas are similar to the grid lines within the nanomesh films. The devices are fully suspended (Figure 1c) between two freestanding membranes (Figure 1d) that define the hot and the cold end for heat transport measurements. Temperature-dependent values of κ are determined by measuring the amount of heat generated by the resistive heater on one of the membranes and the temperature difference between the hot and the cold side [19]. For details on methods see Methods.

Figure 2d summarizes κ measurements on the two nanomesh devices and the reference structures. κ for the TF is about 17 W/m-K at room temperature. The decrease from bulk Si κ=148 W/m-K is consistent with published results [20], and originates from the thickness

of the film. The reduced cross-section of the nanowires that comprise the NWA leads to a further reduction to κ=3.5 W/m-K at room temperature, a result that is again consistent with published results from us and others [11,12]. To calculate κ of the nanomesh and EBM films, an approximation is applied in which the mesh structure is treated as two intersecting arrays of rectangular channels (Figure 2e; only one array of channels is highlighted). In nanomesh devices, these channels resemble the nanowires in the NWA; in the EBM they are wide ribbons. The heat transport is essentially diffusive; λ is an order of magnitude smaller than any of the dimensions in either the EBM or the nanomesh films [6]. As a result, only the channels running along the temperature gradient contribute significantly to the thermal conductance through the device; the perpendicular channels are effectively isothermal. In the EBM device, there is only a small increase in boundary scattering, compared to the TF, since Λ is predominantly defined by the similar thickness T in both devices. Accordingly, the EBM has comparable κ to the TF.

The equivalent channel approximation is likely less accurate for the nanomesh due to the round shape of the holes and the fact that the grid line width is comparable to the pitch. However, κ is only overestimated by this approximation, so that the room temperature measurement of 1.9 W/m-K only represents the upper limit for the actual κ. A reduction of at most 20% for the nanomesh films relative to the nanowires in the NWA would be expected if we consider only the small difference in size between the equivalent channels and the nanowires. Similarly, a significant increase in κ would be expected for the

nanomesh films relative to the NWA if we considered only the relative surface-to-volume ratios. The measured κ for the nanomesh films is, however, a factor of 2 smaller that that of the NWA.

Matthiessen's rule, $\tau^{-1} = \tau_{imp}^{-1} + \tau_U^{-1} + \tau_B^{-1}$, captures the dominant phonon scattering mechanisms. Here τ represents the total phonon relaxation time, and the subscripts imp, U, and B, respectively, refer to impurity scattering, Umklapp processes, and boundary scattering. We do not expect τ_U or τ_{imp} to vary between similarly doped devices (Figure 3). Surface roughness can influence on τ_B [13]. However, relative to the NWA, there is less or equal roughness present in the nanomesh films where fabrication processes can introduce roughness only to the walls of the holes, compared to the entire length of nanowire side surfaces. Plus, the surface-to-volume ratio of the nanomesh is actually significantly smaller (see table in Figure 2a). Thus, the reduction in κ for the nanomesh relative to the NWA is a consequence of the superstructure and the related modification of the bulk phonon dispersions.

We tentatively ascribe the observed drop in κ to a coherent effect in which holes play the role of Bragg reflectors – similar to the coherent phonon processes that are invoked in certain superlattice thin films. The periodicity of the superstructure – either the one introduced by the holes in the nanomeshes, or by the alternating thin-film layers in superlattices – modifies the phonon band structure by reducing the Brillouin zone (BZ). In superlattice structures, scattering of thermal phonons at the successive interfaces between

the composite layers can dominate over such coherent mechanisms. However, the superstructure of the nanomesh is imposed within a single crystalline piece of material where coherence may be readily maintained. In addition, the period of the superstructure is on the order of the mean-free-path of the thermal phonons (Λ>25 nm [21]), enabling the observation of wave-like effects that can emerge from the BZ reduction [22]. As a consequence, phonon bands are folded 62 times (superstructure period/Si lattice parameter) and considerably flattened compared to bulk Si bands. BZ reduction effects have been studied theoretically in superlattices [16,22-25], where the treatment is equivalent in the case of cross-plane transport, and all contributions to κ are considered to be spectral quantities: $\kappa(T) \propto \int_{\lambda} C_{v,\lambda}(T) v_{\lambda}^{2} \tau_{\lambda}(T) d\lambda$. Adopting these results, we expect no corrections at 300 K in the specific heat $C_{v,\lambda}$. The relaxation times τ_{λ} may change in periodic structures, but only for small periods and at low temperatures [23,24]. Therefore, we expect the most significant contribution to κ reduction to come from the decrease of the phonon group velocity v_{λ}, as a direct consequence of the flattening of phonon bands [25]. A complete phonon band structure modeling will be necessary to estimate the extent of κ reduction in our system, but in the case of superlattices factors of 2 – 10 have been found [25], which are consistent with the nanomesh results. Theoretical modeling of Si three-dimensional phononic crystals indicates that the phonon band flattening, such as observed in our nanomeshes, may lead to thermal conductivities below κ_{min} [26]. Highly voided materials, such as nanoporous Si, have been shown via molecular dynamics modeling to exhibit low κ [21,27,28], but the results published to date have largely focused only on boundary

scattering mechanisms. Theoretical simulations of very thin (2-3 nm diameter) Si nanowires have indicated that an amorphous surface layer can yield a temperature-independent and low value of κ [29]. However, our nanostructures are not in this regime, and we do not observe the surface-to-volume ratio effects on κ that would be expected from this mechanism.

Two highly doped nanomesh devices exhibited metallic-like electrical conductivity that followed the bulk trend [30] in both temperature dependence and magnitude (Fig 3). We are currently investigating structural and dimensional variations of these nanomesh films with the goal of more fully understanding the relationship between materials architecture and thermal conductivity.

Methods

The devices were prepared on silicon-on-insulator wafers (Soitec Inc.). The wafers were pre-doped by thermally diffusing a spin-on-dopant (Boron A; Filmtronics, Inc.) using rapid thermal annealing at 820°C for 3 minutes. The wafer sheet resistance indicated a doping concentration of $2x10^{19}$ cm^{-3}. All devices were fabricated by transferring a device-defining pattern from a Pt mask into the Si epilayer (Figure 1a) by CF_4/He reactive ion etching. The TF and EBM devices were patterned by electron-beam lithography, and NWA nanowires and NM nanomeshes by the SNAP technique [17] (Figure 1a). The precise thickness T of the devices is determined by measuring the Si epilayer thickness with an atomic force

microscope. The other size parameters listed in Figure 2a were determined from scanning electron microscope images.

We have developed a fabrication protocol that allows thermal conductivity measurements on fully suspended (i.e. without oxide support) nanowires and nanomeshes, and applied it to nanowires as thin as 20x28 nm^2. The measurement platform (Figure 1d) is suspended over the Si handle layer (black in Figure 1a) and consists of two symmetric sets of membranes with serpentine Pt heaters/temperature sensors, and beams with heater/sensor leads. The active device region is fully suspended between the membranes. The platform consists of layers that reinforce the structure and provide protection during the gas-phase suspension of the device. The bottom layer is the same Si epilayer as in the device region. Such contact with the device, referred to as the monolithic contact, reduces considerably the thermal resistance between the membranes and the device, and enables accurate measurements of thermal conductivity. For structural integrity, a 250 nm low-stress silicon-nitride film is deposited by plasma enhanced chemical vapor deposition (PECVD by STS Multiplex). Then, a 20 nm Ti adhesion layer and 60 nm thick Pt heaters/sensors and leads are deposited on top of silicon-nitride by electron-beam assisted evaporation (CHA; Semicore). A 200 nm capping layer of poly(monochloro-*p*-xylylene), or parylene-C (SCS parylene deposition system), completes the layered structure. The platform was defined by e-beam lithography and Al metallization, and then transferred by oxygen plasma etching in order to remove parylene, and CF_4 plasma to remove silicon-nitride and buried oxide. The device region was protected during etching by a 100 nm layer of Al, which was deposited directly on top of the device and underneath the silicon-nitride and parylene layers.

Afterwards, All was removed by a phosphoric acid based etchant. At this point, the device and the measurement platform are defined on top of the Si handle layer. The device is released in two gas-phase etching steps. First, a 6% polymethyl methacrylate (PMMA 950) e-beam resist is spun on the device to protect the Si device, and two openings on either side of the membranes were patterned by e-beam lithography. Then, an isotropic XeF_2 etch (custom pulsed etching system) was applied in order to release the platform and the device from the Si handle layer. The overall etch time is about 2 minutes at 2000 mTorr and at room temperature. The PMMA layer is then removed using an acetone bath and supercritical drying (Automegasamdri-915B, Tousimis). In the final step, the device is released from the remaining buried oxide layer (blue in Figure 1a). A home-built HF vapor etcher equipped with a wafer heating stage was designed for homogeneous and stiction-free oxide removal at elevated temperatures. The etching process is performed in vapors of the mixture of HF (49%) and isopropyl alcohol with the wafer heated to a temperature of ~80°C. A complete removal of 125 nm buried oxide is achieved in ~30 minutes. The platform was sufficiently protected from HF damage by the top parylene layer and the bottom Si epilayer. The sample is wire-bonded to a chip, and promptly inserted into the high-vacuum cryostat (VPF-475, Janis research). The thermal conductance measurement procedure and the detailed error analysis are described in [19]. Electrical conductivity was measured on separate unsuspended devices with e-beam lithography defined Pt four-point contacts.

Measurement Procedure

Li Shi et al. have detailed measurement and analysis procedures in their report of thermal and thermoelectric property measurements of one-dimensional nanostructures on suspended device platforms [19]. We adapted their platform and procedures to enable measurements of thermal conductance on monolithically-fabricated, fully-suspended devices on SOI substrates. We refer the reader to their work for details on the procedures. In the following, we briefly summarize our adaptation.

In our measurement platform, the sample is bridged between a pair of suspended membrane "islands", as previously described in the **Device Fabrication** section. Each membrane contains a set of serpentine Pt lines that serves as a PRT and is suspended by four long (~70 μm) beams along which the electrical connections are routed. One of the PRTs also serves as a heater and measures the hot side temperature. The other measures the cold side temperature. (Figure 5)

The cryostat is ramped to a set temperature T_0 at a rate of <3 K min^{-1} to minimize thermal stresses on the suspended structure. After the cryostat temperature has stabilized, a current source (Keithley 6221) is used to supply a small sinusoidal current $i_{ac,h}$ ~ 250 nA at frequency f_h > 700 Hz on top of a dc current I to the heating PRT. The differential resistances R_h (resistance of the serpentine element) and R_L (resistance of the lead) of the heating PRT are measured simultaneously with a pair of lock-in amplifiers (Stanford Research Systems SRS830). Another SRS830 lock-in is used to source a sinusoidal current $i_{ac,s}$ ~ 250 nA at frequency f_s through a high-precision 10 MΩ metal film resistor (Vishay

Sfernice CNS020) to the sensing PRT, while measuring the differential resistance R_s. These measurements are repeated for the entire set of dc currents before the cryostat is ramped to another set temperature, upon which the measurement cycle repeats.

At the conclusion of the experiment, the set of $R_s(I=0)$ and $R_h(I=0)$ acquired at various temperatures T_0 is fitted using linear least squares regression to obtain $dR_s(I=0)/dT$ and $dR_h(I=0)/dT$. The temperature rise of the heating and sensing PRTs are then given as

$$\Delta T_h = \frac{\Delta R_h(I)}{\frac{dR_h(I=0)}{dT}};$$

$$\Delta T_s = \frac{\Delta R_s(I)}{\frac{dR_s(I=0)}{dT}};$$

The Joule heat developed in the heating PRT and its leads are $Q_h = I^2R_h$ and $2Q_L = 2I^2R_L$ and we can thus calculate the beam and sample thermal conductances.

$$G_b = \frac{Q_h + Q_L}{\Delta T_h + \Delta T_s}$$

$$G_s = G_b \frac{\Delta T_s}{\Delta T_h - \Delta T_s}$$

Uncertainty of the Thermal Conductivity δ_κ

The thermal conductivity is obtained from the measured thermal conductance of each sample and the geometrical factor ($\kappa = G_s \times$ geometrical factor), i.e. the cross-section and length of the equivalent channels for the NM and EBL NM; and the exact cross section and length of the NWA and TF samples. The geometrical factor (G.F.) for the NWA, EBL NM,

NM can be described by G.F. = L/(n×T×W) where L represents the length of the system across the measurement platform, n is the number of wires or equivalent channels, T is the thickness of the silicon epilayer, and W is the width of a nanowire or equivalent channel (Figure 2a). The number of nanowires can be calculated by dividing the total width of the sample W_0, by the pitch of the wire or the equivalent channel array P. Thus, G.F = (P×L)/(W_0×T×W). Therefore, the uncertainty of the thermal conductivity can be evaluated by

$$\frac{\delta_\kappa}{\kappa} = \sqrt{\left(\frac{\delta G_s}{G_s}\right)^2 + \left(\frac{\delta P}{P}\right)^2 + \left(\frac{\delta L}{L}\right)^2 + \left(\frac{\delta W_0}{W_0}\right)^2 + \left(\frac{\delta T}{T}\right)^2 + \left(\frac{\delta W}{W}\right)^2}$$

The uncertainty of the measured G_s is determined as previously described.

For the NM, $P = 34.6 \pm 1.9$ nm, $L = 7.31 \pm 0.07$ μm, $W_0 = 7.28 \pm 0.04$ μm, $W = 22.81 \pm 2.33$ nm as determined by SEM. $T = 22.3 \pm 1.3$ nm based on AFM measurements at five different positions of the SOI wafer. $G_s = 26.32 \pm 0.51$ nW/K at 250 K. As a result, $\kappa = 1.80 \pm 0.23$ W/m-K.

For the NWA, $P = 34.4 \pm 1.6$ nm, $L = 8.45 \pm 0.13$ μm, $W_0 = 7.71 \pm 0.21$ μm, $W = 28.25 \pm 1.46$ nm, $T = 20.1 \pm 1.2$ nm, $G_s = 56.81 \pm 1.14$ nW/K at 250 K giving $\kappa = 3.40 \pm 0.33$ W/m-K.

Thermopower

The thermopwer or the Seebeck coefficient (S) is obtained based on previously reported methodology (Chapter 2; [10]). All the devices under investigation are p-type boron doped. As can be seen from Figure 6, bulk-like thermopower [31] is observed for all the nanomesh devices. For NM devices with doping concentration lower than $1\times10^{19}\,cm^{-3}$, the Seebeck coefficient peaks at lower temperature ~ 150K and can possibly be attributed to phonon-drag effect.

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Figure 1A

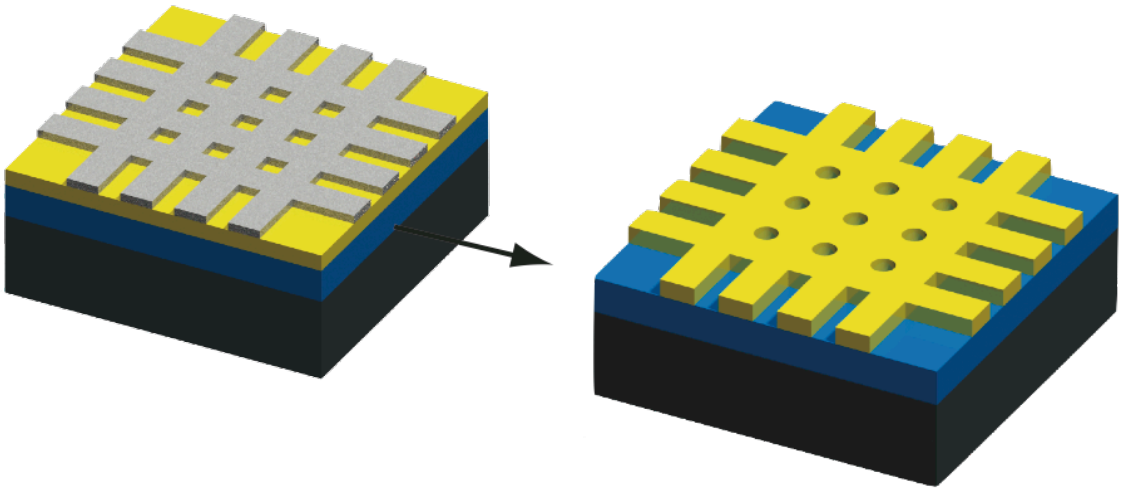


Figure 1B

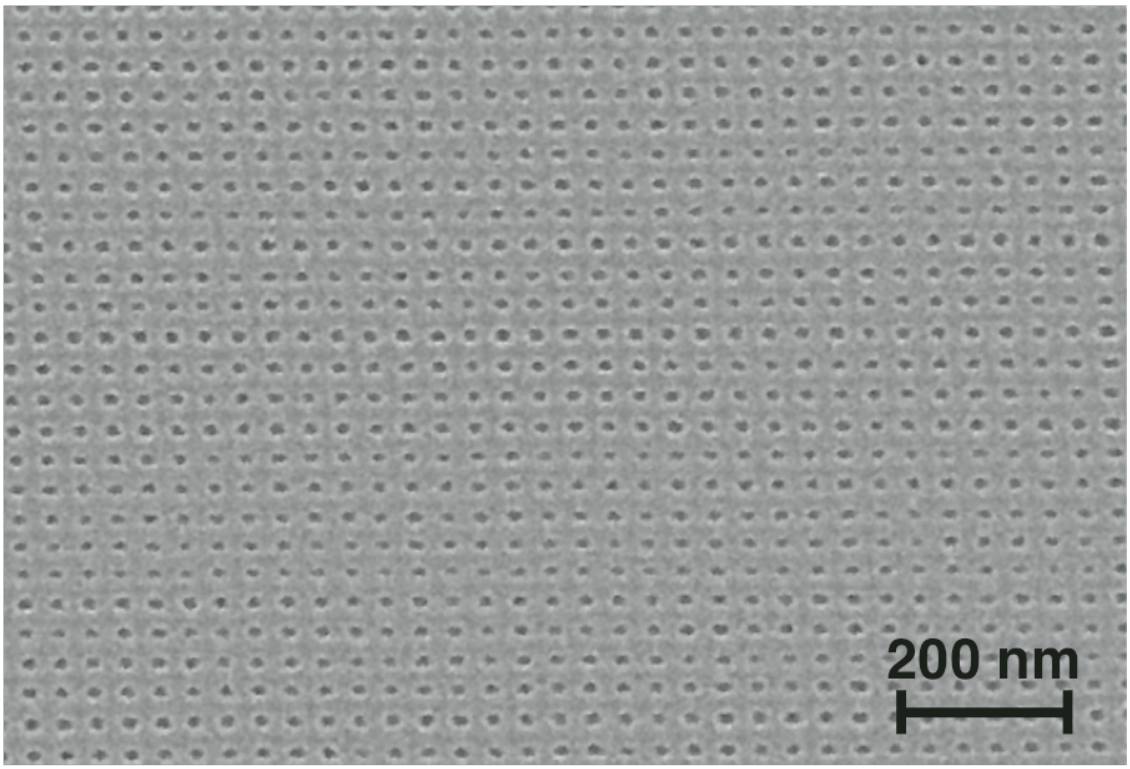


Figure 1C

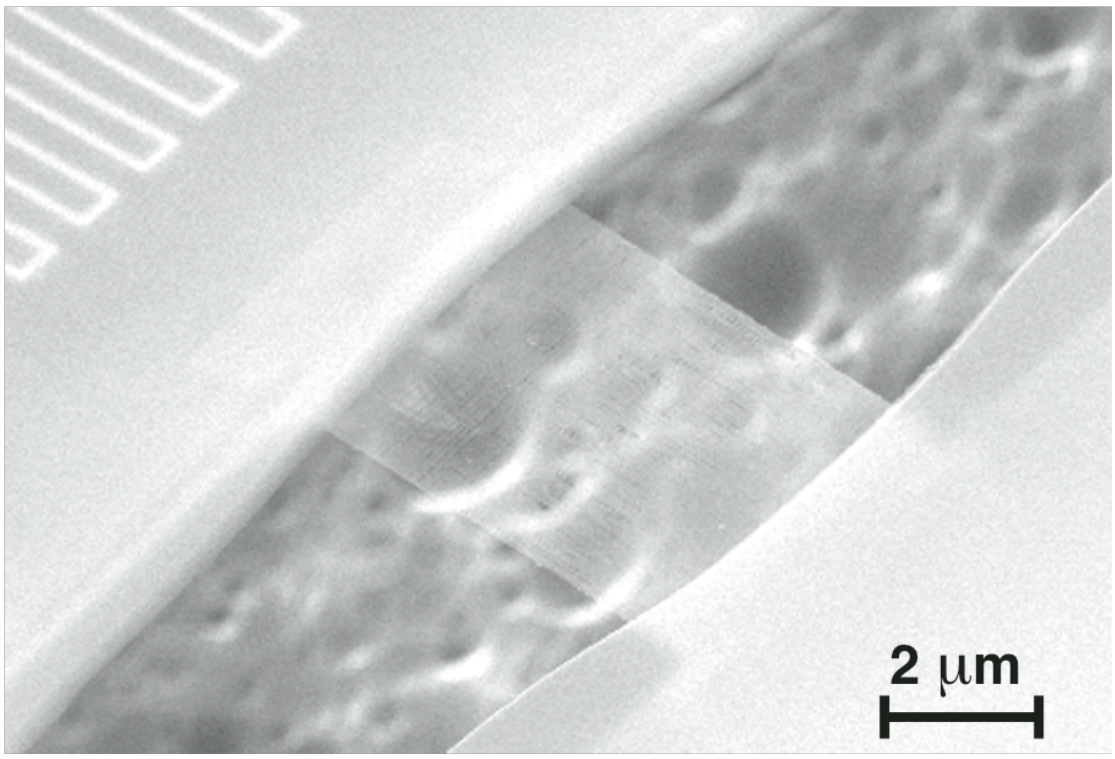


Figure 1D

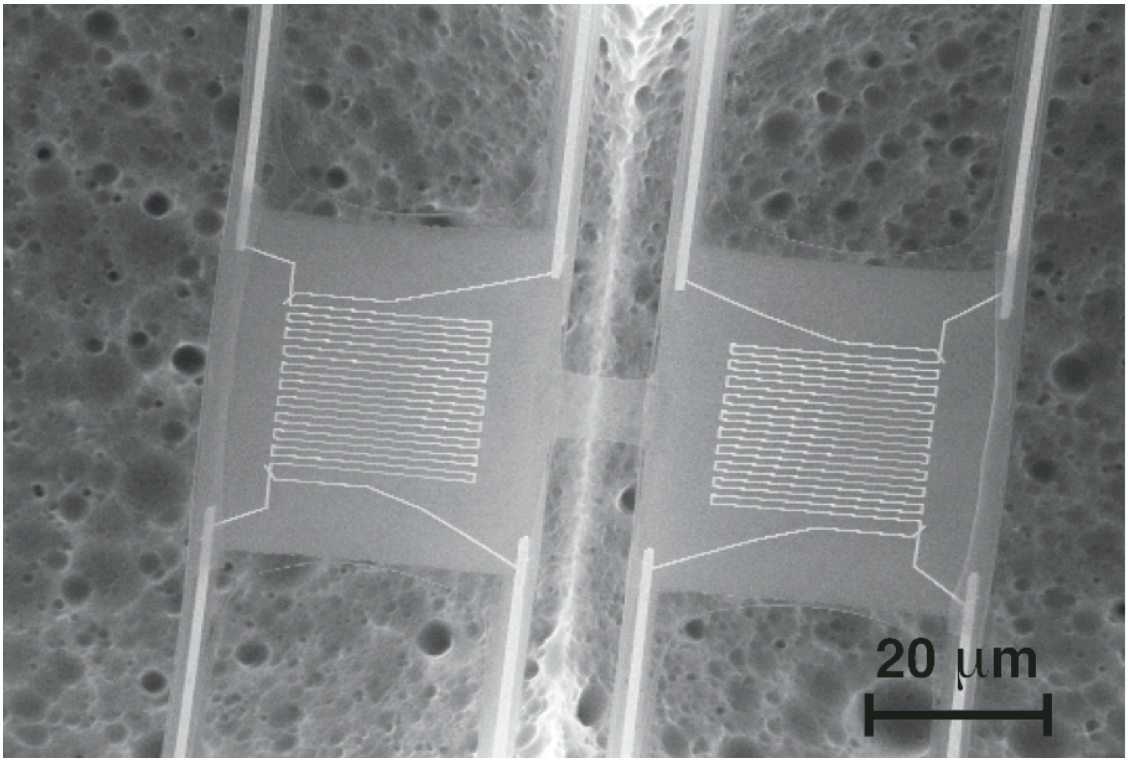
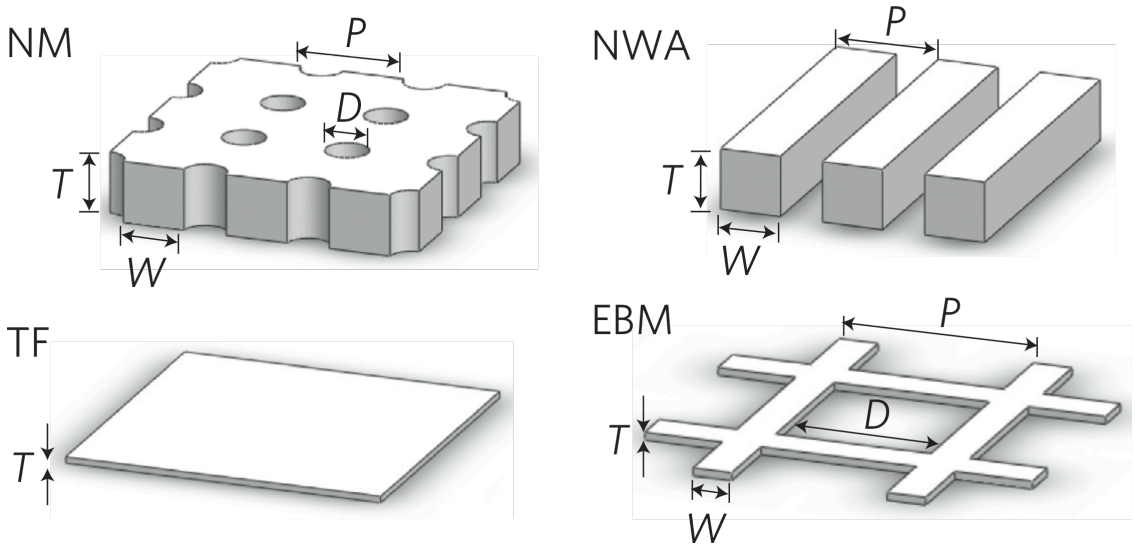


Figure 2A



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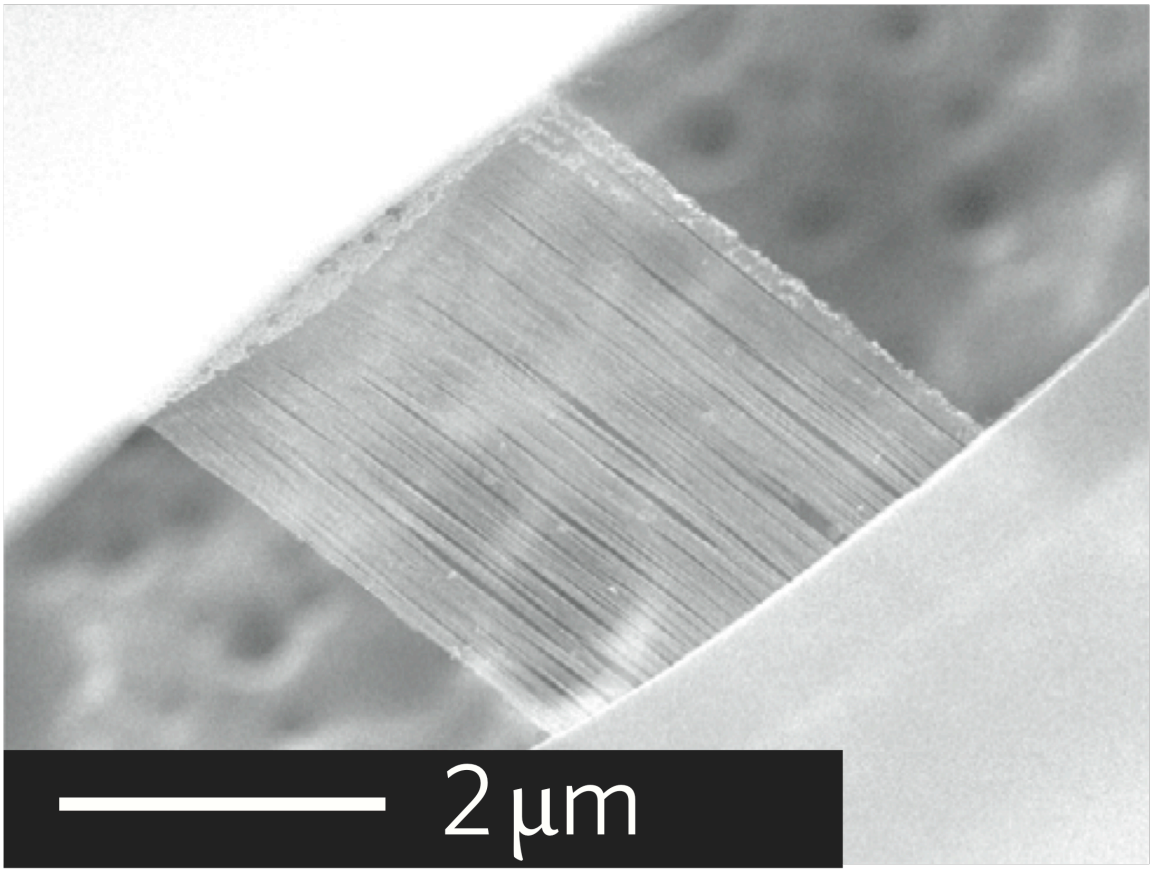

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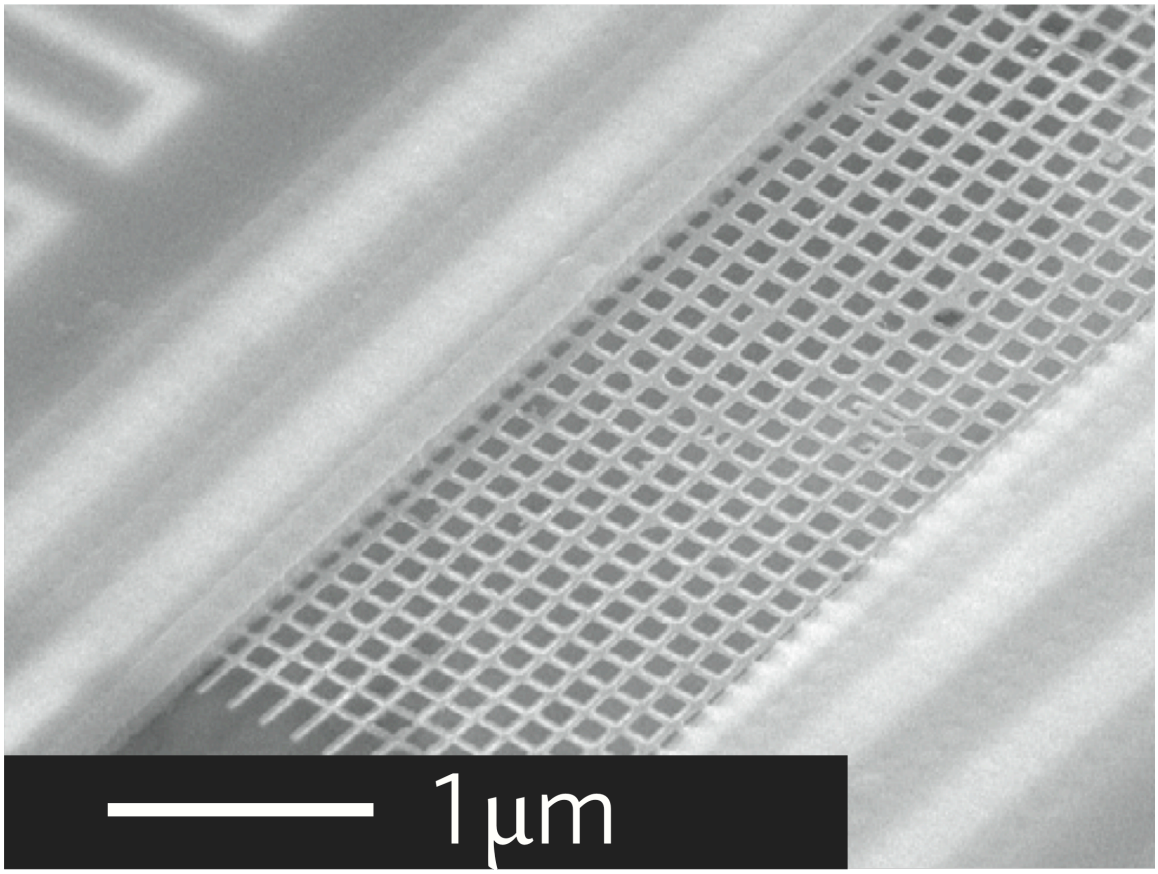

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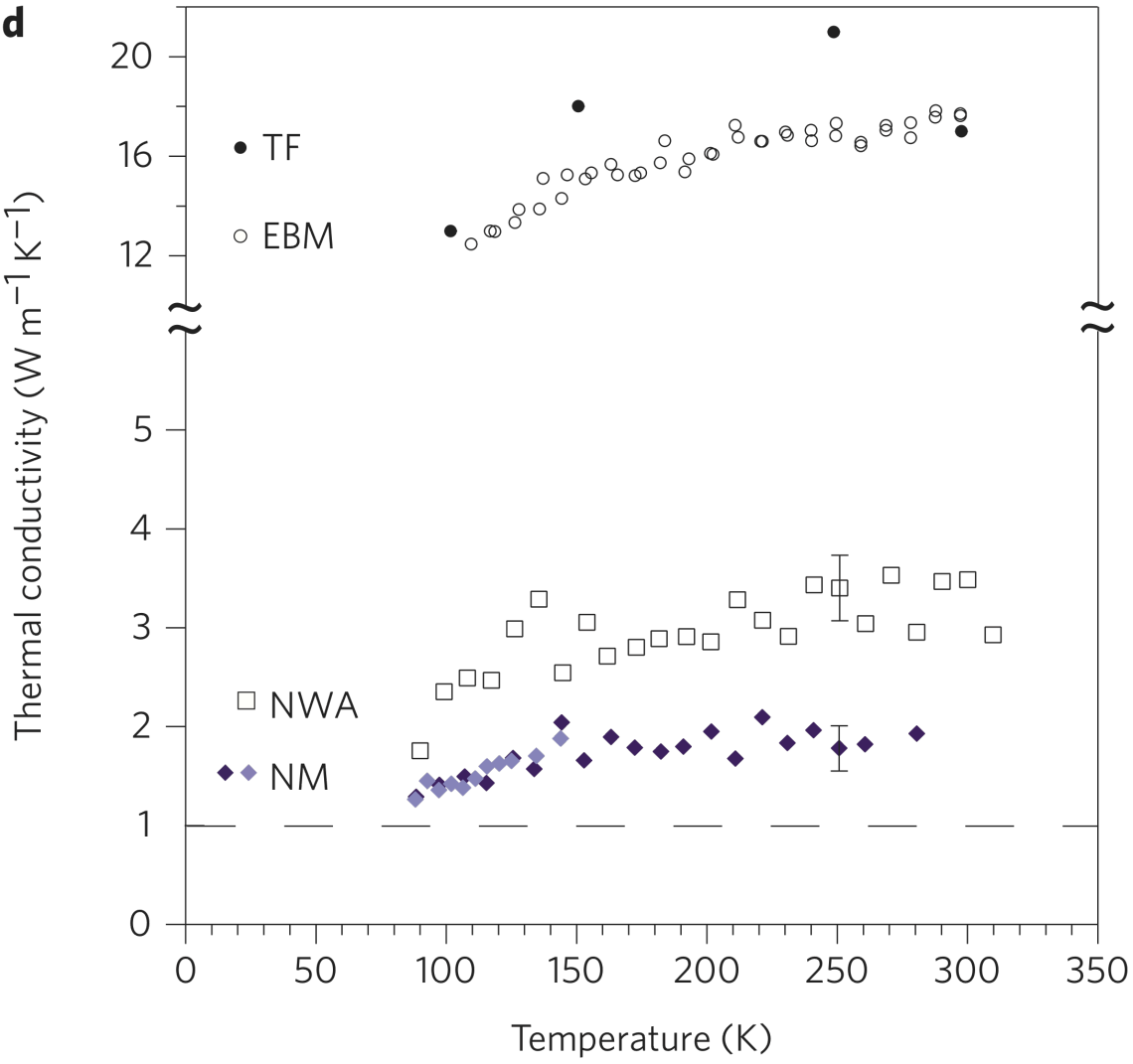
d
Thermal conductivity (W m^{-1} K^{-1})
20
16
12
5
4
3
2
1
0
TF
EBM
NWA
NM
0
50
100
150
200
250
300
350
Temperature (K)

Figure 2E

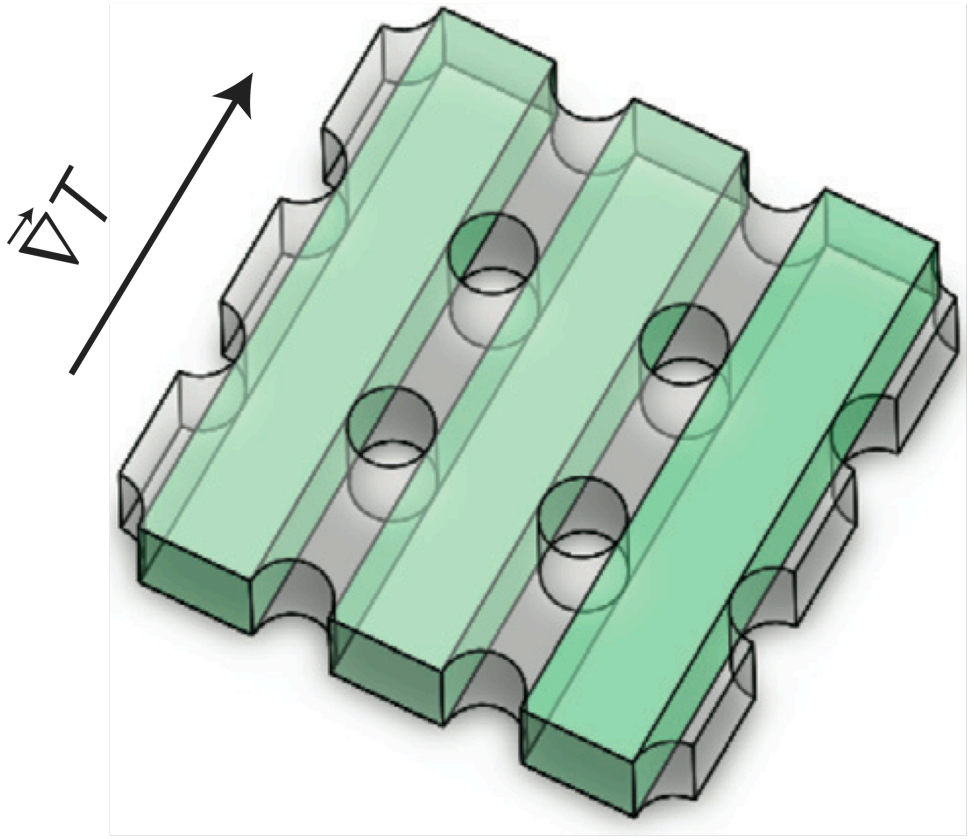

Figure 3

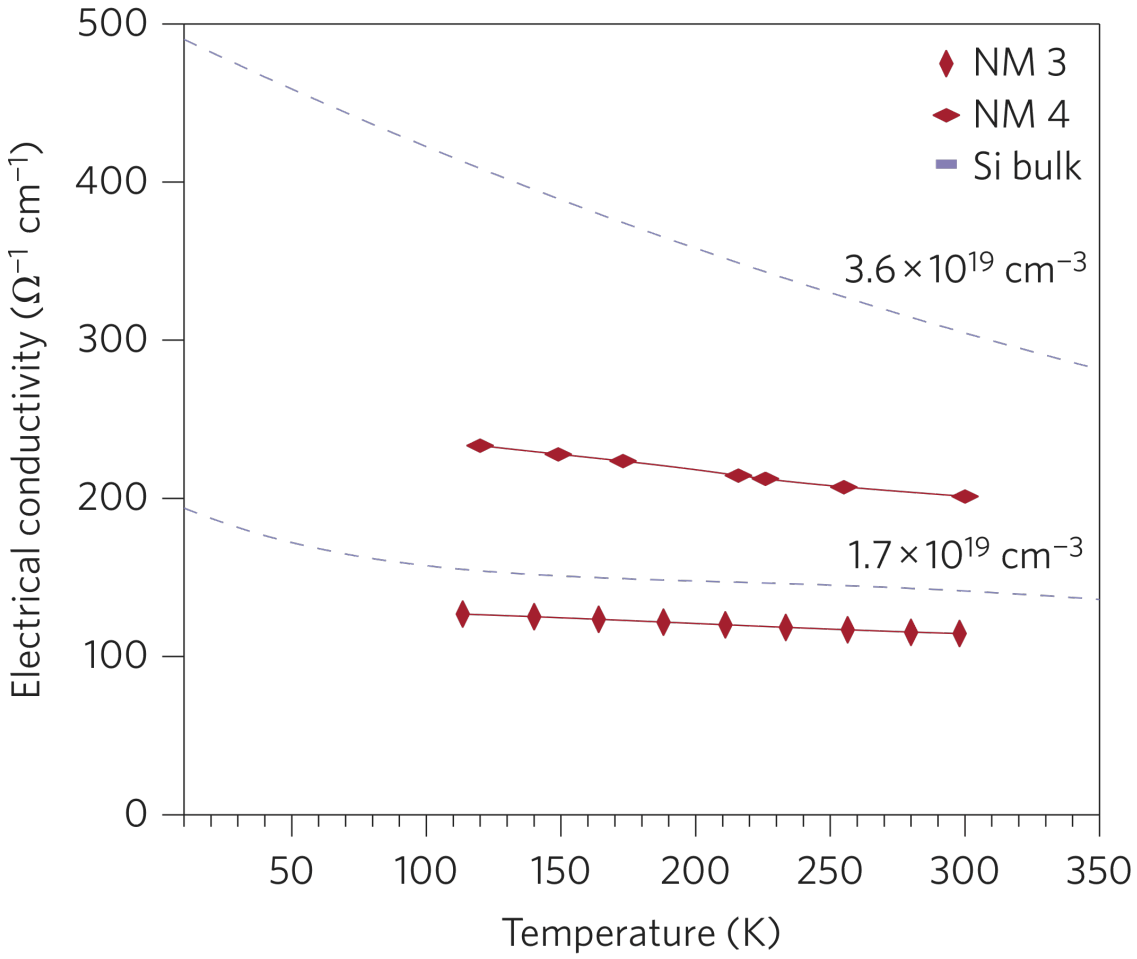
NM 3
NM 4
Si bulk
3.6×10^19 cm^−3
1.7×10^19 cm^−3
Electrical conductivity (Ω^−1 cm^−1)
Temperature (K)
500
400
300
200
100
0
50
100
150
200
250
300
350

Figure 4

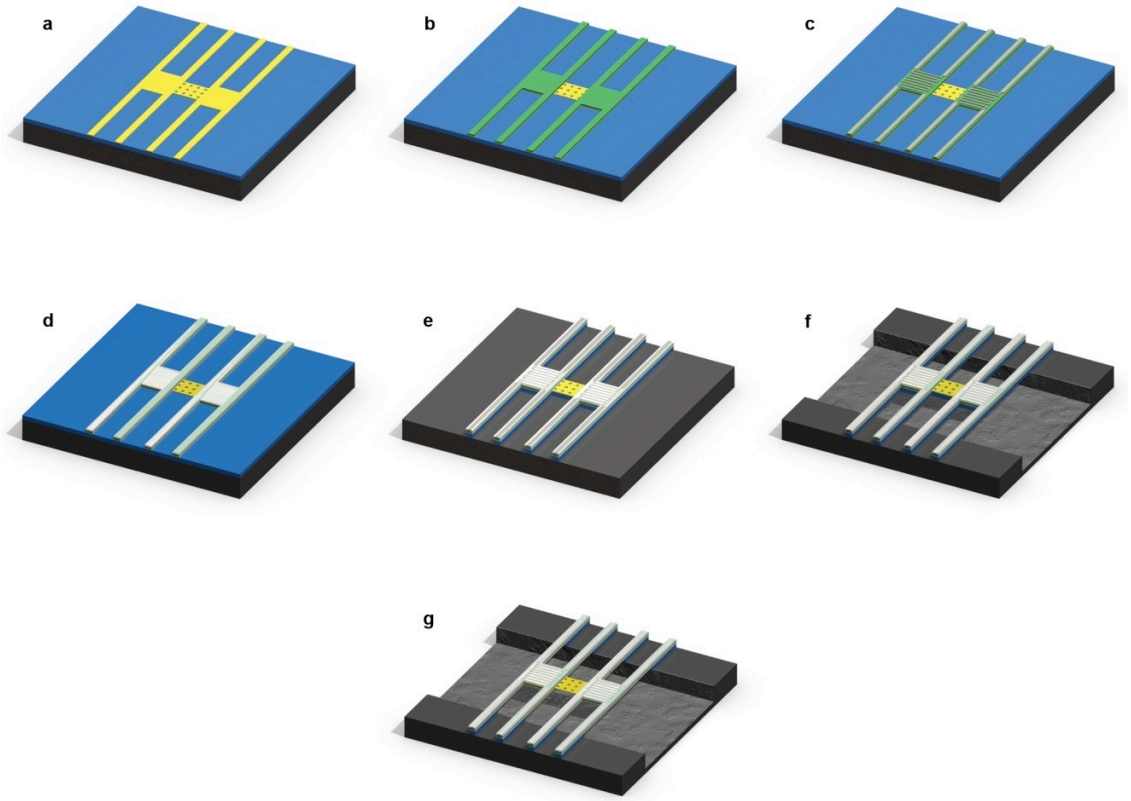

Figure 5

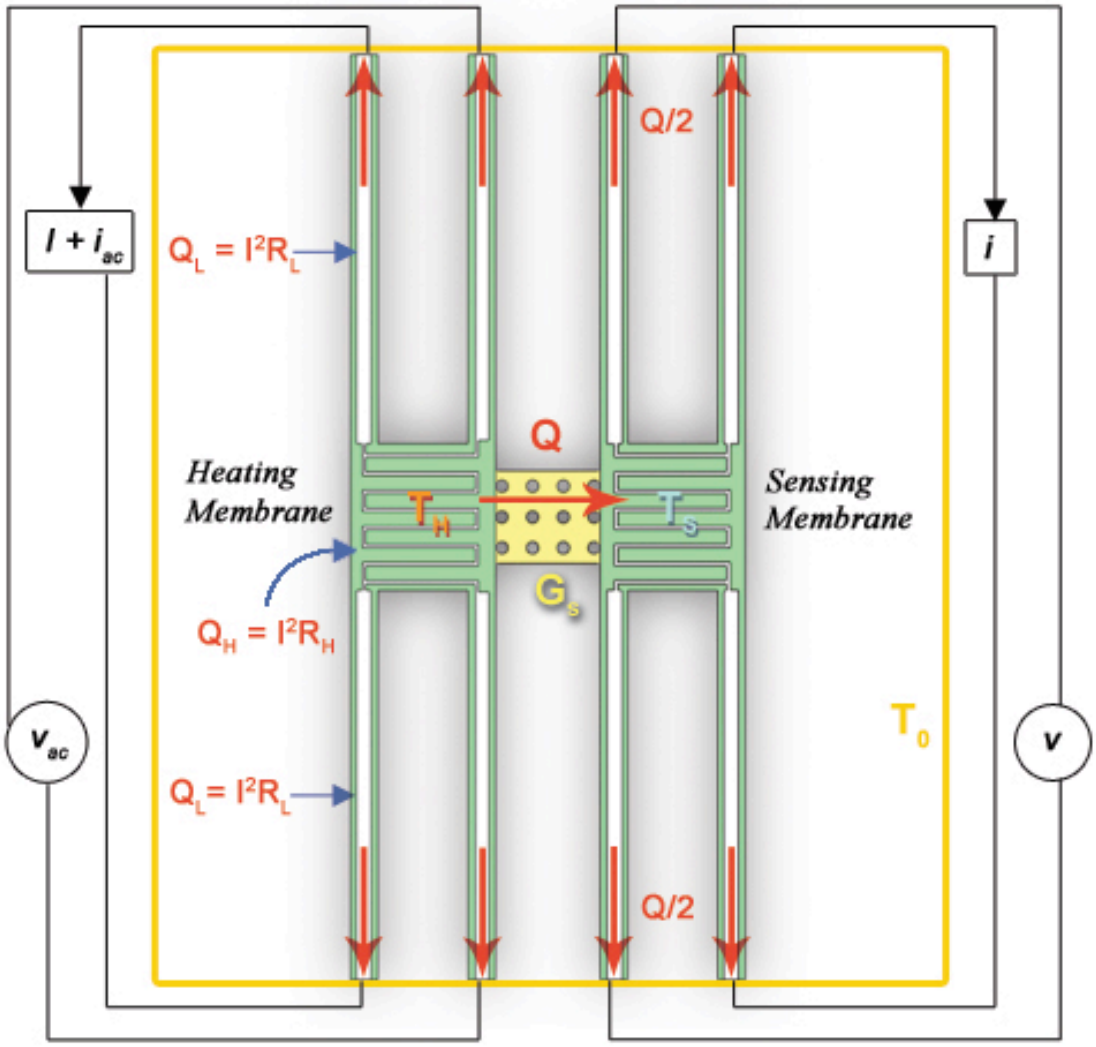
I + i_ac
Q_L = I²R_L
Q/2
i
Q
Heating Membrane
T_H
T_S
Sensing Membrane
G_S
Q_H = I²R_H
T_0
V_ac
V
Q_L = I²R_L
Q/2

Figure 6

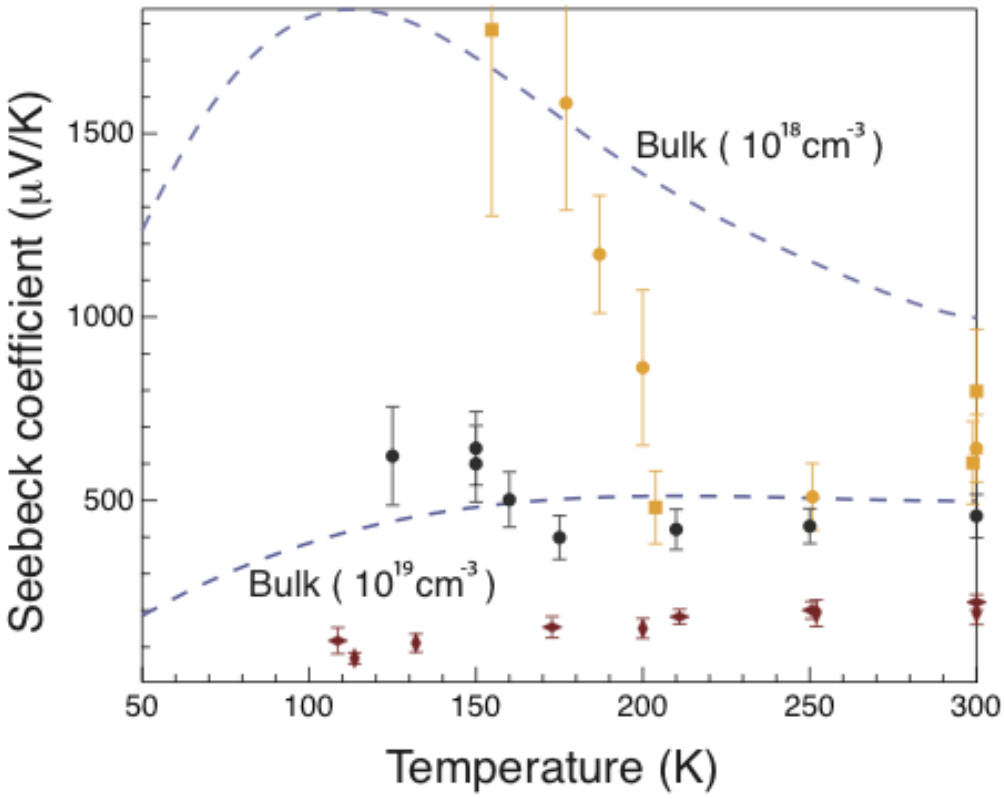
Seebeck coefficient (μV/K)
1500
1000
500
50
100
150
200
250
300
Temperature (K)
Bulk (10^18 cm^-3)
Bulk (10^19 cm^-3)

Table 1

Table 1 | Dimensions, including surface-to-volume ratios, of the two nanomesh films (NM1 and NM2) and three reference systems (TF, EBM and NWA).

	T (nm)	*W* (nm)	*D* (nm)	*P* (nm)	Surface/Volume (nm^{-1})
TF	25	-	-	-	0.08
EBM	22	115	270	385	0.07
NWA	20	28	-	-	0.17
NM 1	22	23	11	34	0.12
NM 2	22	18	16	34	0.14

Dimensions are as shown in Fig. 2a.

Figure Captions

Figure 1 Silicon nanomesh device

a. Silicon nanomesh films are fabricated on silicon-on-insulator wafers by transferring the pattern of two intersecting Pt nanowire arrays (grey) into the Si epilayer (yellow). The intersecting Pt nanowire arrays are created using the superlattice nanowire pattern transfer (SNAP) technique, which translates the layer spacings within a GaAs/$Al_xGa_{(1-x)}As$ superlattice into the width and pitch of a nanowire array [17]. Two successive SNAP processes are needed to make an intersecting array. In the image, blue layer represents the buried silicon-dioxide, and black is the Si handle layer **b.** Scanning electron micrograph of a part of a Si nanomesh film, showing a uniform square-lattice matrix of cylindrical holes (scale bar 200 nm). The nanomesh films can be up to 10 × 10 μm^2 in area. **c.** Scanning electron micrograph of a fully released, transparent nanomesh film suspended between two membranes (scale bar 2 μm). **d.** Lower magnification micrograph showing suspended membranes with Pt heaters/sensors together with the suspended beams carrying the leads for thermal conductivity measurements (scale bar 20 μm).

Figure 2 Device geometries and thermal conductivity measurements.

a. The geometry and dimensions, including surface-to-volume ratios, of the nanomesh films and three reference systems. **b.** SEM image of suspended nanowires in the NWA device, and **c.** the suspended EBM device. **d.** Comparative plot of thermal conductivity measurements on two different nanomesh devices (diamonds) and the three reference

devices. The TF and EBM devices have similar thermal conductivities as a result of their similar film thickness. The NWA nanowires have lower thermal conductivity reflecting their larger surface-to-volume ratio compared to TF and EBM (note the discontinuity in the y-axis). The nanomesh devices, though with significantly lower surface-to-volume ratio compared to NWA, exhibit a factor of two lower thermal conductivity. The error bars on the selected points are representative for the measurements (see Supplemental information for detailed error analysis) **e.** In order to calculate thermal conductivity from measured thermal conductance, the heat is assumed to flow through equivalent, green highlighted channels. The thermal gradient does not have a component perpendicular to these channels. The actual conduction cross-section can only be larger if we account for the interconnecting parts between channels. This approximation gives the upper bound value for the thermal conductivity in nanomeshes.

Figure 3 Electrical conductivity measurements.

Four-point measurements of the electrical conductivity (red diamonds) of two nanomesh films, both p-type doped with boron to nominal concentration $2.0 \times 10^{19} cm^{-3}$. Small spatial variations in doping levels of Si epilayers are standard with spin-cast doping, and this is reflected in different electrical conductivities of the two nominally equally doped devices. Electrical measurements are performed on separate but identically processed devices as the ones used for thermal conductivity measurements. Both nanomesh devices exhibit values that are comparable to bulk Si thin film (dashed lines; adopted from [30]). The results

imply that the nanomesh films are relatively defect-free and that bulk Si electrical properties are preserved in the high-doping range.

Figure 4. Device fabrication.

The scale of the device is exaggerated from reality for better visualiztion. (a) Silicon nanomesh with monolithically-defined silicon device platform. (Yellow). (b) Device platform with silicon-nitride film as the structural backbone. (c) Ti/Pt heater/sensor defined on to the platform. (d) Parylene C conformally deposited on to the platform. (e) Buried oxide removed by RIE1 process. (f) Si handle layer etched by XeF_2. (g) Device fully suspended by buried oxide removal with HF vapor.

Figure 5. **Schematic diagram for the thermal conductivity measurement platform**.

T_H and T_S represent the temperatures of the heating and sensing membranes respectively. T_0 is the substrate temperature. Q_H, Q_L represents the amount of heat generated by the heater and the lead, respectively. Q is the amount of heat transported through the sample and G_s is the thermal conductance of the sample.

Figure 6. Seebeck coefficient measurements.

Thermopower measurements on multiple p-type NM devices with different carrier concentrations are compared to bulk Si thermopower in the oping impurity concentration range from 10^{18} to 10^{19} cm^{-3}. Red symbols represent two sets of data on devices doped at $2x10^{19}$ cm^{-3} (twice that of the dashed line representing bulk Si doped at 10^{19}); black symbols $4x10^{18}$ cm^{-3}; and yellow symbols two sets of data at $2x10^{18}$ cm^{-3}.

C h a p t e r 4

FUTURE DIRECTIONS:

QUANTUM DOT ENERGY FILTERING THERMOELECTRIC DEVICES

In this section, enhancement of the thermoelectric power factor ($S^2\sigma$; S: Seebeck coefficient, σ: electrical conductivity) of silicon is proposed by thermionic energy filtering approach. Fe_2O_3 quantum dots are assembled along the silicon device as non-volatile electrical field effect centers for potential energy barrier introduction. Electron-beam lithography (EBL) and dip-coating process are applied to define the spatial arrangement of the quantum dots. In this work, clusters of a few (3-5 particles) quantum dots are assembled with a periodicity of 100 nm. The thermionic energy barriers are expected to selectively scatter low energy carriers, causing asymmetric energy distribution of the carrier relaxation time, resulting in an enhanced Seebeck coefficient. The periodic energy barrier also resembles superlattice geometry electronically with no physical interfaces.

Introduction

According to Mott's formula [1], the magnitude of thermopower is proportional to the energy derivative of electrical conductivity at the Fermi level.

$$S = \frac{\pi^2}{3}\left(\frac{k_B^2 T}{e}\right)\left(\frac{d\ln\sigma(E)}{dE}\right)_{E=E_F} \quad \textbf{. (4.1)}$$

Therefore, engineering materials with asymmetric electrical conductivity distribution function at the Fermi energy could lead to large a Seebeck coefficient, resulting in high ZT materials [2]. To better understand the recent approaches to enhance the Seebeck coefficient, we expand the electrical conductivity in the Mott's formula to a function of electronic density-of-state (DOS), carrier relaxation time, and carrier group velocity.

$$S = \frac{\pi^2 k_B^2 T}{3e}\left[\frac{\partial \ln DOS}{\partial E} + \frac{\partial \ln \tau(E)}{\partial E} + \frac{\partial \ln \upsilon^2(E)}{\partial E}\right]_{E=E_F} \quad \textbf{. (4.2)}$$

It becomes obvious that one way to create asymmetric electrical conductivity distribution is through nano-structuring. It has been proposed that low-dimensional materials could introduce sharp features in the density-of-state (DOS) *via* confinement [3]. Another approach is by introducing resonant levels at the Fermi energy by impurities. Such resonant levels would distort the electronic DOS of the host material, creating an enhanced thermopower [4].

Thermionic energy filtering is another approach to enhance thermopower. In brief, a potential energy barrier is used to selectively scatter low-energy charge carriers and therefore creates an asymmetric charge carrier relaxation time distribution. According to Mott's formula, such asymmetric distribution in carrier relaxation time could result in a larger Seebeck coefficient. Several reports have demonstrated improvements in thermoelectric efficiency *via* energy filtering. Examples are thin film superlattices (SLs),

nano-inclusions, and nano-grains. However, these examples involve sophisticated molecular beam expitaxy (MBE), phase separation, and hot pressing techniques with restricted material compositions. In this chapter, I propose to exploit the electric field effect created by charge-injected quantum dots for creating the potential energy barriers. Such novel device design provides a controllable way to optimize the barrier height without the restriction of material systems. In addition, the position of the energy barriers could also be controlled with nanometer precision.

The first part of this proposal will focus on the theoretical background of energy filtering and a short literature review on the subject. The experiment design, device geometry, charge-injection mechanisms, and control of potential energy barrier height will be covered in the second part of this proposal.

Part I: Energy Filtering -- Theory and Literature Review

Classically, transport coefficients can be derived from solving the Boltzmann transport equation. The Seebeck coefficient can be expressed as below under the relaxation time approximation (i.e., the transport process is much slower than the relaxation process) and small local deviation from equilibrium (linearized Boltzmann equation).

$$S \equiv \frac{k_B}{q} \frac{\int \sigma(E) \frac{(E - E_F)}{k_B T} dE}{\int \sigma(E) dE} \propto \langle E - E_F \rangle \text{. (4.3)}$$

q is the unit charge, E_F is the Fermi energy, k_B is the Boltzmann constant. $\sigma(E)$ is the differential conductivity and represents the contribution of charge carrier with energy E to the total conductivity; the denominator in the above expression describes the total electrical conductivity. Note that the Mott's formula is derived from equation **4.3** in the particular cases of degenerate semiconductors or metals. The differential conductivity is related to the carrier relaxation time $\tau(E)$, the group velocity $\upsilon(E)$, the density-of-state $D(E)$, and the Fermi-Dirac distribution function $-\partial f/\partial E$.

$$\sigma(E) \sim q^2\tau(E)\upsilon^2(E)D(E)(-\frac{\partial f}{\partial E}). \textbf{(4.4)}$$

From equation **4.4**, the magnitude of the Seebeck coefficient is proportional to the average energy carried by the charge carriers relative to the Fermi energy. In other words, material with an optimized Seebeck coefficient should has highly asymmetric differential conductivity at the Fermi level. A normal energy distribution of the differential conductivity with Fermi level at the peak maximum results in zero thermopower.

The thermopower can be enhanced in a material if the low energy charge carriers are readily removed. This is essentially the main theme of thermionic energy filtering concept. Such concept is also supported by the energy-dependent thermopower of heavily doped n-type $Si_{80}Ge_{20}$ alloy calculated by Gang Chen *et al.* [5]. The calculation implies that the overall thermopower is enhanced when the low-energy carriers are effectively scattered.

There is a trade-off between the electrical conductivity and thermopower. In principle, as the doping concentration is increased, which corresponds to higher electrical conductivity in general, the Fermi energy moves deeper in the band, resulting in a more symmetric differential conductivity and hence a smaller Seebeck coefficient. This is due to the square root dependence of the band structure on energy. Such trade-off, however, could be avoided by energy filtering. To elaborate more, as the Fermi level is pushed deeper into the conduction band, the differential conductivity asymmetry is still attained when the low energy carriers are scattered selectively by potential energy barriers. In such a scheme, large electrical conductivity and enhanced Seebeck coefficient could be achieved at the same time.

In the past decade, the concept of improving thermoelectric power factor $S^2\sigma$ by an energy filtering approach has been investigated theoretically [6,7] and experimentally. Shakouri et al. demonstrated an increase of the power factor in $In_{0.53}Ga_{0.47}As/In_{0.53}Ga_{0.28}Al_{0.19}As$ superlattices over bulk [8]. Heremans et al. and Martin et al. showed that an energy-filtering effect occurred at the grain boundaries of the PbTe-nanocomposites [9,10]. Another example is the Pt nanocrystal embedded Sb_2Te_3 [11], where the interfaces between the nanocrystal and the host matrix facilitate the carrier filtering process. Although energy filtering has been proven possible, the aforementioned demonstrations are limited to restricted material systems and the control over the energy barrier as well as the interface/boundary quality remains a critical issue for further thermoelectrics performance optimization.

In this work, I propose a novel way of exploiting the energy filtering concept in enhancing the thermoelectric power factor. In stead of physical material barriers, electric-field-induced potential energy barriers will be used in this study to achieve energy filtering. Charge-injected quantum dots assembled on the semiconductors will be utilized as the electric field effect centers. Silicon nanowire and silicon nanomesh structures will be used as proof-of-principle systems in this work. These two material systems have been demonstrated to be potential high efficient thermoelectric materials due to their ultra-low thermal conductivities [12,13]. A further improvement on the thermoelectric power factor will ensure the materials useful renewable energy sources. Detailed device geometry as well as working principles will be described in the following sections.

Part II: Experimental Design and Device Working Principle

Device fabrication

Silicon nanowire arrays and silicon nanomesh samples will be fabricated using the superlattice nanowire pattern transfer technique (SNAP) as decribed in previous chapters. After the nanowire array or the nanomesh are fabricated, the contact electrodes and the heaters will be defined by electron-beam lithography (EBL) and e-beam assisted metallization followed by atomic layer deposition (ALD) of the dielectric layer HfO_2 on top of the active silicon. The contact electrodes will be serving as voltage probes and resistive thermometers for the Seebeck coefficient measurements. At the same time, the contact electrodes are used for electrical conductivity measurements. The heaters are used to create the temperature gradient across the device by DC joule heating.

Next, EBL is again used to open patterns of spin-coated poly(methyl methacrylate) or PMMA resist on the device for quantum assembly. The quantum dots are assembled by dip-coating method as reported previously [14]. The device will then be dipped into acetone to lift-off the PMMA resist and the unwanted quantum dots. At last, another dielectric layer will be deposited by ALD followed by the metallization of gate electrode to complete the device. In this device geometry, the QDs are isolated from the ambient by the oxide dielectric and thus are working as floating gates after charge injection. Figure **1** shows the schematics of the device geometry.

Electrical conductivity and Thermopower measurements

Electrical conductivity of the samples will be measured with and without gate potential by a four-point probe setup. Briefly, the gate potential and the strength of the electric field are controlled by injecting different amounts of charge into the quantum dots through the gate electrode. The voltage bias on the gate electrode is then removed. Next, the electrical current is sourced (Keithley 2400 source meter) through two outer electrodes placed at the two ends of the sample. The voltage drop is obtained by a voltage meter (Keithley 6500 nanovolt meter) via another inner pair of electrodes. The resistance of the sample is obtained by the slope of the linear regression fit to the I-V curve.

Thermopower measurements require accurate detection of the voltage drop, ΔV, and the temperature difference, ΔT, across the sample. ΔV will be obtained via the two inner electrodes (same device configuration as described previously in electrical measurement section) and a voltage meter. ΔT, on the other hand, can be determined by the resistive

thermometer design. In short, an ac current will be sourced through the thermometer electrode while the ac voltage drop is read out by another pair of leads on the same thermometer. The resistance of the thermometer will then be determined and the temperature of the thermometer can also be obtained by fitting the resistance to the temperature vs. resistance calibration curve. Detailed temperature detection procedure can be found in Chapter 3 and the report by Yu et. al [13].

Energy barriers by electric field effects (EFE)

In a field-effect transistor (FET), the EFE is used to control the shape of the conducting channel; in other words, it controls the conductivity of the charge carrier in the semiconductor device. The EFE functions as a physical gate that regulates the flow of charge carriers from the source terminal to the drain terminal. Applying this scheme to a TE element, the source terminal is the heat source (hot end) and the drain terminal is the heat sink (cold end). In a p-type depletion mode transistor (normally "on" at zero gate voltage), a positive bias on the gate depletes the holes in the channel a down-regulates the carrier flow. In the case when the source-to-drain voltage V_{DS} is much smaller than the gate bias V_G, which is the case in the proposed device scheme ($V_{DS} \sim 1-10mV$ and $V_G \sim 0.1-10V$), the gate functions as a variable transistor and the device is in linear mode or ohmic mode. The relation between the source-to-drain current I_{DS} and the gate voltage can be described as:

$$I_{DS} = I_{DSS}\left[1-\left(\frac{V_G}{V_G(off)}\right)\right]^2 \quad \textbf{. (4.5)}$$

I_{DSS} represents the source-to-drain current at zero gate voltage. $V_G(off)$ represents the "off" state gate voltage. In essence, the applied voltage introduces an energy barrier on the conduction channel; the larger the gate voltage or EFE, the higher the energy barrier. In this proposal, we use charge-injected quantum dots as floating gate materials to create the energy barriers to selectively scatter the low energy charge carriers.

Quantum dot size and the barrier height

In enhanced-mode metal-oxide-semiconductor field effect transistors (MOSFET), the threshold voltage represents the gate voltage required to cause the forming of charge carrier flow (inversion layer) at the oxide-semiconductor interface of the transistor. In electronically erasable and programmable nonvolatile memory devices, charge injection or tunneling into the floating gate causes the threshold voltage shift. The magnitude of the threshold voltage shift is related to device parameters such as oxide thickness and dielectric constants. In floating gate memory devices, the amount of charge stored in the floating gate also controls the threshold shift. Physically, the threshold shift reflects the strength of the electric field from the charged quantum dot over the transistor.

Hanafi et al. showed that the threshold shift of the quantum dot memory device could be described as [15]

$$\Delta V_T = \frac{qn_{QD}}{\varepsilon_{ox}}\left(t_{oxide} + \frac{1}{2}\frac{\varepsilon_{ox}}{\varepsilon_{Si}} r_{QD}\right) \quad \textbf{. (4.6)}$$

q is the magnitude of electronic charge, n_{QD} represents the density of quantum dots, ε are the permittivities, t_{ox} is the thickness of the control oxide, and r_{QD} is the size of the quantum dot. Based on this expression, the potential energy barrier introduced by the quantum dots could be controlled by the amount of charge stored in the quantum dots, the density of the dots, the size of the dots, and the thickness of the control oxide as well as the oxide materials. In this proposed study, we will explore these parameters to optimize the power factor of the device.

Charging quantum dots with the control gate voltage

The charge is injected into the quantum dots by Fowler-Norheim tunneling mechanism when a bias voltage is applied at the control gate. The required control voltage to inject the charge is found to be [16]

$$\Delta V_{GS} = (\text{quantum energy level spacing} + \text{charging energy}) / q \cdot (1 + \frac{C_{tt}}{C_{CG}}) \quad \textbf{. (4.7)}$$

C_{tt} is the dot-to-channel capacitance and C_{CG} is the gate-to-dot capacitance. The quantum dot charging energy is related to the size of the quantum dot and the number of electron/hole by the following equation [17]

$$\Delta E = \frac{(nq)^2}{C_{QD}} = \frac{(nq)^2}{4\pi\varepsilon_0\varepsilon_r r} \quad \textbf{. (4.8)}$$

Equations (4.6)-(4.8) provide us useful guidance in controlling the energy barrier by changing the size of the quantum dots, the magnitude of the control gate voltage and the oxide thickness.

Working principle

In this proposal, quantum dot clusters (QDC) are assembled periodically in proximity to the TE material. After charge injection, each QDC creates a local electric field that induces energy barriers for selectively scattering off the low energy charge carriers. The periodic electric field generated by the QDC resembles the energy barriers in the cross plane thin film superlattice (Figure 2). As depicted in Figure 2, although the electrical conductivity is generally high for heavily doped semiconductors with Fermi level deep into the band, the thermopower in this case is often times small because the Fermi level lies very close to the differential conductivity peak maximum. The trade off between the electrical conductivity and the thermopower renders the heavily doped semiconductor unattractive for thermoelectric applications. Exploiting the potential energy barriers generated by the charge-injected quantum dots, we can enhance the thermopower by creating asymmetry in the energy distribution of electrical conductivity, with little adverse effect on the total electrical conductivity.

Conclusion

Silicon nanowires and silicon nanomeshes exhibit thermal conductivities two orders of magnitude smaller than the bulk silicon. Experimental evidences imply that these material systems could achieve ZT greater than 2 if optimized. In this proposal, we expect to enhance the thermoelectric power factor of these silicon nanostructures by an energy filtering approach. Unlike conventional energy filtering approaches based on superlattices with restricted material systems, this proposed work uses electric field effect to generate

potential energy barriers for charge carrier scattering. The barrier heights are readily controlled by the amount of charges injected into the quantum dots, the size of the dots, and the thickness of the dielectric layers. Such device architecture has no physical interfaces along the charge carrier transport path, whereas in superlattices the imperfections of the interfaces often times reduce carrier mobility. Lastly, the proposed device scheme is in principle applicable to all semiconductor TE systems.

PHONONIC SUPERLATTICE THERMOELECTRIC DEVICES

In Chapter 3, we demonstrated that exploiting the phonon wave nature could effectively reduce the lattice thermal conductivity in silicon, while maintaining bulk-like electrical properties. According to theory, discernible wave interference requires the mean-free-path (or the coherent length) of the phonons to larger or of the same order as the characteristic lengths of the sample (Chapter 3 and reference [18]). In the case of silicon nanomeshes, the pitch of the Bragg reflectors (voids in the film) is similar to the phonon mean-free-path set by the critical dimensions in the sample (i.e., ~ 20 nm). Under such conditions, the phonon wave-nature is important and the band folding effect is observed.

Although the coherent scattering mechanism in the nanomesh length scale (a few tens of nanometers) provides a possible route to approach or break the lower thermal conductivity limit of silicon predicted with bulk dispersion (Chapter 2), scaling up the nanomesh structure in bulk materials for large scale applications is technologically challenging. In this section, a phononic superlattice structure fabricated in a bulk silicon film is proposed to reduce the thermal conductivity of the material by both the aforementioned phononic crystal (PnC) mechanism as well as by an additional thermal boundary resistance introduced at the interfaces of the PnC and the blank silicon. The structure can be readily fabricated with modern lithography techniques and is highly scalable.

Kapitza resistance was first discovered in 1941 [19] and states that a temperature discontinuity is present at the boundary when heat is conducted from solid to liquid. Later, Kapitza resistance was also recognized at the interface of two acoustically dissimilar materials (i.e., materials with distinct phonon band structures). Two models have been widely applied to describe the Kapitza resistance: the acoustic mismatch model (AMM) and the diffuse mismatch model (DMM) [20]. In this section, the proposed superlattice structure consists of repeating units of patterned phononic crystal segment and continuous silicon film (Figures 3 and 4). Kapitza resistance is expected to arise at the surface of the patterned voids. Additionally, the interfaces of the patterned segment and the continuous film are also potential locations for the interfacial thermal resistances if the patterned area has noticeable band folding. Under such conditions, increasing the number of superlattice units will substantially reduce the thermal conductivity of the sample.

Device Fabrication

The phononic superlattices are made from SOI wafers with 340 nm SOI and a 1−μm-thick buried oxide layer. The following processes flow explicitly lists all the fabrication steps required in making the device.

1. Thermal oxidation 40 min at 1000°C dry oxidation --> 50 nm oxide. The thermal oxide is used as the etching mask in the later step.
2. 3% PMMA e-beam lithography (120x; 3000, 3000, 1.0; poly fill). This step is to define the hole pattern on the wafer.
3. CF_4 plasma etch. Recipe: CF_4-no-h. Etch time ~ 7 min. (CF_4/He 20 sccm/30 sccm, 10 mtorr, 60 -> 40 Watt). Note: the PMMA is consumed at the end of this etching step.

4. O_2 plasma clean (O_2; 20 sccm; 20 mtorr; 70 watt, 1 min)

5. UCLA DRIE (Bosch process. 6 sec x 2)

6. CF4_no_h again to remove the top thermal oxide (~ 7 min)

7. E-beam lithography to define the heaters/thermometers/leads.

Writing parameters:

thermometers (L2): 200x; 150; 250; SS:1.0; line dose 1.6

heaters (L3): 200x; 250; 250; SS 1.0; AD 500

leads pads (L4): 200x; 700; 700; SS 3.0; AD 500

leads (inner; L5): 120x; 150; 250; SS 1.0; LD 1.4

leads (outer; L6): 50x; 800; 800; SS 5.0; AD 500

(Metal deposition: Ti/Pt = 200/1200 A)

8. Wire bonding pad contacts (Ti/Pt/Au=200/300/2400A)

9. Deposit 6000 A of Al at a rate of 3 A/second by e-beam PVD (CHA) for device and monitlithic contact definition and a monitor area on the side for film thickness check. (a nice lift-off takes 5-6 hours.)

E-beam writing parameters for these features:

Device protection & Monolithic contact(Layer 8): 120x; 700, 700, SS 3.0; AD 500

Monitor section (L 9): same as above

10. Use swab to paste some 3% PMMA on the outer part of the device for reserving the silicon. Bake the PMMA at 180C for 1min.

11. Silicon etch. RIE Recipe: SF6_ENPD. Etching time ~2 min plus 30 second extra etch.

12. Remove PMMA with acetone bath --> this could take up to 10 min or more because the PMMA is thick!

13. Remove Al by PAE (100°C for 5 min)

14. Al deposition again for the suspending beams and membranes. (6000 A; 3 A/S)

Layer 10& 11 same writing recipe as L8&L9.

15. After lift-off, spin 6% PMMA at 2000 rpm and bake at 180C for 1 min. (This is necessary to protect the metal leads from damage by the long plasma etch in the later steps)

16. E-beam lithography to open up windows for oxide etch.

17. Oxide etch. Etch recipe CF4_jk. The 6% 2000 rpm PMMA could survive under such plasma condition for 23 min.

18. Remove the PMMA with O_2 plasma (20 sccm, 20 mtorr, 70 watt for 2 min) + acetone bath (5 min).

19. Repeat step 15-18 until the oxide etch is completed. (total etch time~ 70 min)

20. PAE at 80 deg C 7 min followed by PRX-127 at 120C for 15 min.

20. Spin 6% PMMA at 4000 rpm for E-beam lithography of XeF_2 gas inlets.

21. XeF_2 etch at 1700 mtorr 3-4 pulses, 15 seconds for each pulse etch.

22. O2_ENDP2 for removing the PMMA (~7 minutes).

Figure 3 depicts the scanning electron micrographs of the devices on substrate and suspended with different numbers of PnC-Si interfaces. The diameters of the holes are ~130nm with a pitch of 340 nm; and the hole array is arranged in square lattice. Figures 3b-3d are phononic superlattices with various numbers of interfaces. The area ratio of the patterned section and the un-patterned section is kept the same for these samples.

Measurements

The thermal conductance of the samples is measured with the same methodology as mentioned in Chapter 2. The buried oxide layer under the silicon phononic superlattice is not etched because its contribution to the overall thermal conductance of the sample is at most 10 percent among all the samples measured.

Preliminary Results and Discussions

Figure 4 exhibits thermal conductance results of the silicon film with no hole pattern and three phononic superlattices with 8, 16, and 32 interfaces. A slight adjustment in the thermal conductivity is observed between the sample with 8 interfaces and 32 interfaces. The sample with 16 superlattice interfaces appears to have the lowest thermal conductivity among the samples measured.

Interfacial thermal resistance emerges between materials with dramatically different acoustic properties or phonon band structures. Therefore, a strong band folding effect in the phononic section is prerequisite for substantial thermal conductivity reduction in the phononic superlattices. For such, hole arrays with pitch smaller than the phonon mean-free-path is required. Ju et al. predicted that the mean-free-path of the dominant thermal phonon in silicon at room temperature is close to 300 nm [21]. The phononic superlattices fabricated in this study have holes patterned at a pitch of 340 nm, which is right at the same region as the predicted characteristic length scale. Hole arrays with smaller pitches are

expected to introduce enhanced wave effect at the patterned section. Another future direction for effective reduction in thermal conductivity could be a more complex hole pattern, such as the hexagonal hole pattern (Figure 5). As suggested by Mohammadi et al., a hexagonal phononic crystal creates a broader phonon band gap than the square lattice phononic crystals [22].

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Figure 1

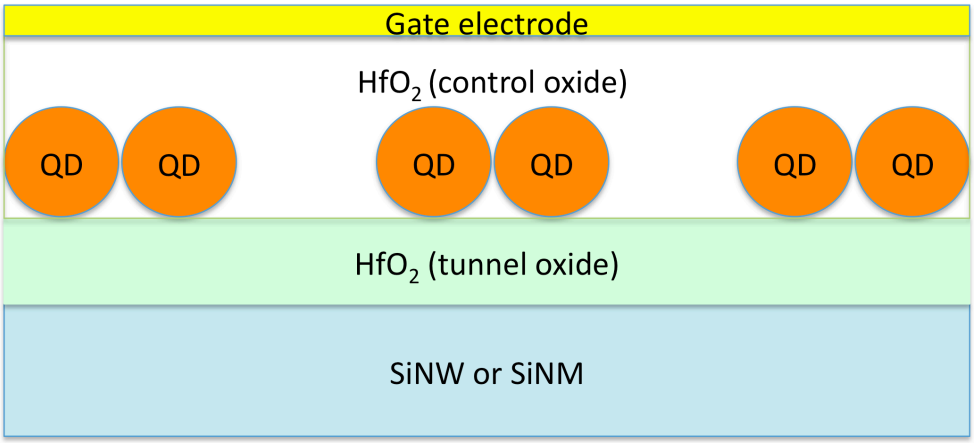
Gate electrode
HfO_2 (control oxide)
QD
QD
QD
QD
QD
QD
HfO_2 (tunnel oxide)
SiNW or SiNM

Figure 2

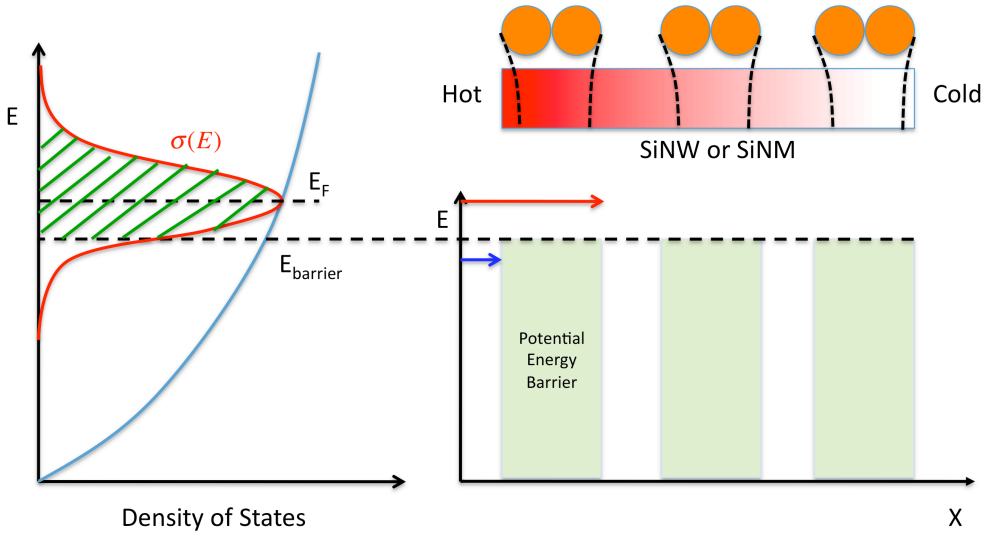
E
$\sigma(E)$
E_F
$E_{barrier}$
Density of States
Hot
Cold
SiNW or SiNM
E
Potential
Energy
Barrier
X

Figure 3

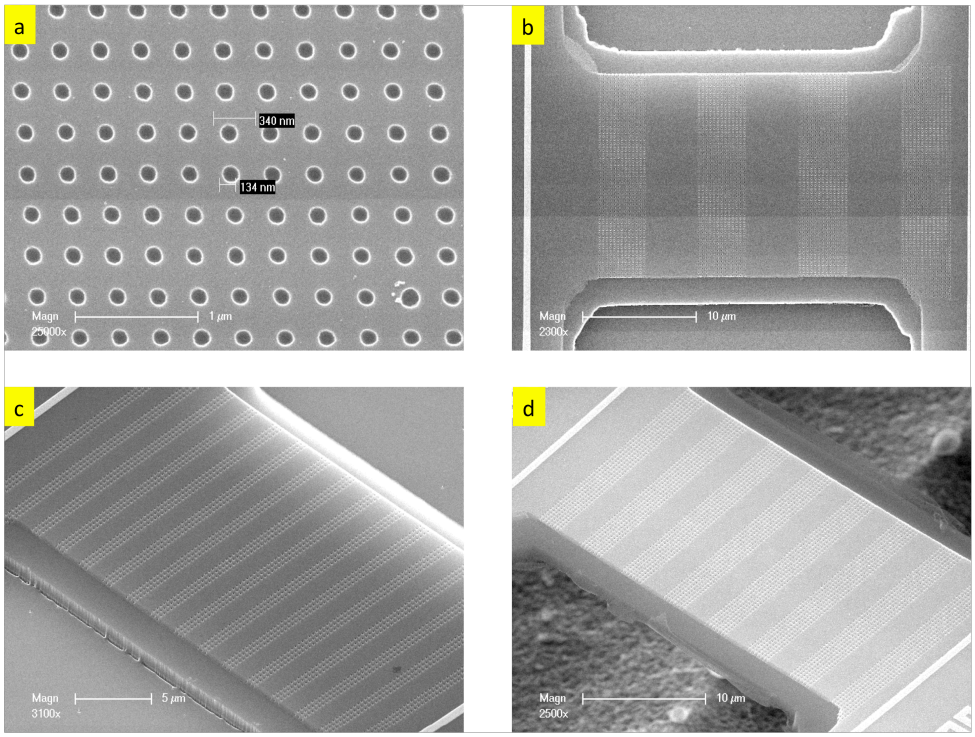
a
340 nm
134 nm
Magn
25000x
1 µm
b
Magn
2300x
10 µm
c
Magn
3100x
5 µm
d
Magn
2500x
10 µm

Figure 4

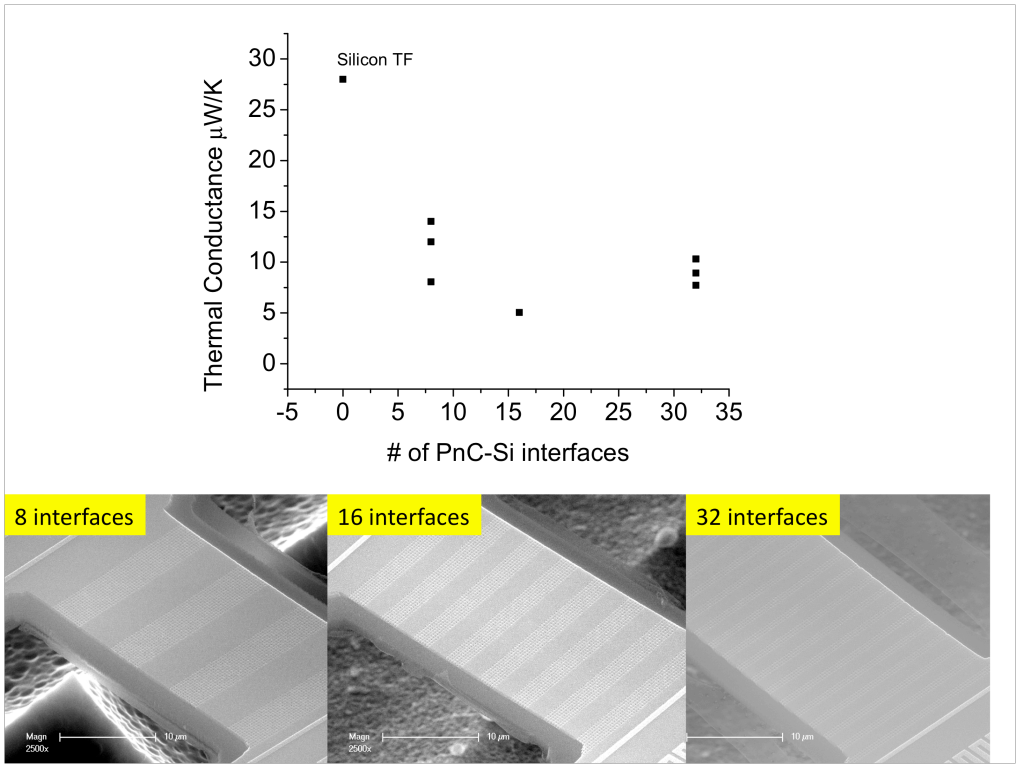
Thermal Conductance µW/K
Silicon TF
# of PnC-Si interfaces
8 interfaces
16 interfaces
32 interfaces

Figure 5

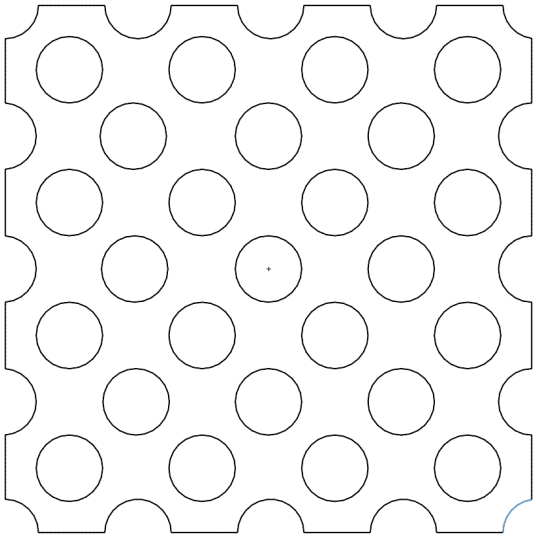

Figure Captions

Figure 1. Schematics of the device architecture.

The quantum dots are embedded in the dielectric layer and serve as electric field centers for the energy filtering devices.

Figure 2. Charged quantum dots serve as electric field centers that create potential energy barriers in the conduction carrier transport path in silicon. These energy barriers reject the low-energy carriers (blue arrow) as high-energy carriers (red arrow and the shaded area on the left) have less influence transporting through. Such energy dependent carrier filtering effect generates asymmetry in the differential conductivity $\sigma(E)$, therefore enhancing the thermopower of the material.

Figure 3. SEM images of the phononic superalattices. (a) a zoom-in image of the hole pattern on the silicon. (b) device with 8 interfaces. (c) device with 32 interfaces. (d) a suspended device with 16 interfaces for thermal conductance characterization.

Figure 4. Thermal conductance of the 320nm thick silicon film and the phononic superlattices with 8, 16, and 32 interfaces. All the samples are suspended with the buried oxide. The devices are sectioned to the same length and width for direct conductance comparison. The buried oxide layer (a separate sample with the same geometrical factors) exhibits thermal conductance around 1 μW/K (data not shown).

Figure 5. Hexagonal phononic crystal structure.