C h a p t e r 4

FUTURE DIRECTIONS:

QUANTUM DOT ENERGY FILTERING THERMOELECTRIC DEVICES

In this section, enhancement of the thermoelectric power factor ($S^2\sigma$; S: Seebeck coefficient, σ: electrical conductivity) of silicon is proposed by thermionic energy filtering approach. Fe_2O_3 quantum dots are assembled along the silicon device as non-volatile electrical field effect centers for potential energy barrier introduction. Electron-beam lithography (EBL) and dip-coating process are applied to define the spatial arrangement of the quantum dots. In this work, clusters of a few (3-5 particles) quantum dots are assembled with a periodicity of 100 nm. The thermionic energy barriers are expected to selectively scatter low energy carriers, causing asymmetric energy distribution of the carrier relaxation time, resulting in an enhanced Seebeck coefficient. The periodic energy barrier also resembles superlattice geometry electronically with no physical interfaces.

Introduction

According to Mott's formula [1], the magnitude of thermopower is proportional to the energy derivative of electrical conductivity at the Fermi level.

$$S = \frac{\pi^2}{3}\left(\frac{k_B^2 T}{e}\right)\left(\frac{d\ln\sigma(E)}{dE}\right)_{E=E_F} \quad \textbf{. (4.1)}$$

Therefore, engineering materials with asymmetric electrical conductivity distribution function at the Fermi energy could lead to large a Seebeck coefficient, resulting in high ZT materials [2]. To better understand the recent approaches to enhance the Seebeck coefficient, we expand the electrical conductivity in the Mott's formula to a function of electronic density-of-state (DOS), carrier relaxation time, and carrier group velocity.

$$S = \frac{\pi^2 k_B^2 T}{3e}\left[\frac{\partial \ln DOS}{\partial E} + \frac{\partial \ln \tau(E)}{\partial E} + \frac{\partial \ln \upsilon^2(E)}{\partial E}\right]_{E=E_F} \quad \textbf{. (4.2)}$$

It becomes obvious that one way to create asymmetric electrical conductivity distribution is through nano-structuring. It has been proposed that low-dimensional materials could introduce sharp features in the density-of-state (DOS) *via* confinement [3]. Another approach is by introducing resonant levels at the Fermi energy by impurities. Such resonant levels would distort the electronic DOS of the host material, creating an enhanced thermopower [4].

Thermionic energy filtering is another approach to enhance thermopower. In brief, a potential energy barrier is used to selectively scatter low-energy charge carriers and therefore creates an asymmetric charge carrier relaxation time distribution. According to Mott's formula, such asymmetric distribution in carrier relaxation time could result in a larger Seebeck coefficient. Several reports have demonstrated improvements in thermoelectric efficiency *via* energy filtering. Examples are thin film superlattices (SLs),

nano-inclusions, and nano-grains. However, these examples involve sophisticated molecular beam expitaxy (MBE), phase separation, and hot pressing techniques with restricted material compositions. In this chapter, I propose to exploit the electric field effect created by charge-injected quantum dots for creating the potential energy barriers. Such novel device design provides a controllable way to optimize the barrier height without the restriction of material systems. In addition, the position of the energy barriers could also be controlled with nanometer precision.

The first part of this proposal will focus on the theoretical background of energy filtering and a short literature review on the subject. The experiment design, device geometry, charge-injection mechanisms, and control of potential energy barrier height will be covered in the second part of this proposal.

Part I: Energy Filtering -- Theory and Literature Review

Classically, transport coefficients can be derived from solving the Boltzmann transport equation. The Seebeck coefficient can be expressed as below under the relaxation time approximation (i.e., the transport process is much slower than the relaxation process) and small local deviation from equilibrium (linearized Boltzmann equation).

$$S \equiv \frac{k_B}{q} \frac{\int \sigma(E) \frac{(E - E_F)}{k_B T} dE}{\int \sigma(E) dE} \propto \langle E - E_F \rangle \text{. (4.3)}$$

q is the unit charge, E_F is the Fermi energy, k_B is the Boltzmann constant. $\sigma(E)$ is the differential conductivity and represents the contribution of charge carrier with energy E to the total conductivity; the denominator in the above expression describes the total electrical conductivity. Note that the Mott's formula is derived from equation **4.3** in the particular cases of degenerate semiconductors or metals. The differential conductivity is related to the carrier relaxation time $\tau(E)$, the group velocity $\upsilon(E)$, the density-of-state $D(E)$, and the Fermi-Dirac distribution function $-\partial f/\partial E$.

$$\sigma(E) \sim q^2\tau(E)\upsilon^2(E)D(E)(-\frac{\partial f}{\partial E}). \textbf{(4.4)}$$

From equation **4.4**, the magnitude of the Seebeck coefficient is proportional to the average energy carried by the charge carriers relative to the Fermi energy. In other words, material with an optimized Seebeck coefficient should has highly asymmetric differential conductivity at the Fermi level. A normal energy distribution of the differential conductivity with Fermi level at the peak maximum results in zero thermopower.

The thermopower can be enhanced in a material if the low energy charge carriers are readily removed. This is essentially the main theme of thermionic energy filtering concept. Such concept is also supported by the energy-dependent thermopower of heavily doped n-type $Si_{80}Ge_{20}$ alloy calculated by Gang Chen *et al.* [5]. The calculation implies that the overall thermopower is enhanced when the low-energy carriers are effectively scattered.

There is a trade-off between the electrical conductivity and thermopower. In principle, as the doping concentration is increased, which corresponds to higher electrical conductivity in general, the Fermi energy moves deeper in the band, resulting in a more symmetric differential conductivity and hence a smaller Seebeck coefficient. This is due to the square root dependence of the band structure on energy. Such trade-off, however, could be avoided by energy filtering. To elaborate more, as the Fermi level is pushed deeper into the conduction band, the differential conductivity asymmetry is still attained when the low energy carriers are scattered selectively by potential energy barriers. In such a scheme, large electrical conductivity and enhanced Seebeck coefficient could be achieved at the same time.

In the past decade, the concept of improving thermoelectric power factor $S^2\sigma$ by an energy filtering approach has been investigated theoretically [6,7] and experimentally. Shakouri et al. demonstrated an increase of the power factor in $In_{0.53}Ga_{0.47}As/In_{0.53}Ga_{0.28}Al_{0.19}As$ superlattices over bulk [8]. Heremans et al. and Martin et al. showed that an energy-filtering effect occurred at the grain boundaries of the PbTe-nanocomposites [9,10]. Another example is the Pt nanocrystal embedded Sb_2Te_3 [11], where the interfaces between the nanocrystal and the host matrix facilitate the carrier filtering process. Although energy filtering has been proven possible, the aforementioned demonstrations are limited to restricted material systems and the control over the energy barrier as well as the interface/boundary quality remains a critical issue for further thermoelectrics performance optimization.

In this work, I propose a novel way of exploiting the energy filtering concept in enhancing the thermoelectric power factor. In stead of physical material barriers, electric-field-induced potential energy barriers will be used in this study to achieve energy filtering. Charge-injected quantum dots assembled on the semiconductors will be utilized as the electric field effect centers. Silicon nanowire and silicon nanomesh structures will be used as proof-of-principle systems in this work. These two material systems have been demonstrated to be potential high efficient thermoelectric materials due to their ultra-low thermal conductivities [12,13]. A further improvement on the thermoelectric power factor will ensure the materials useful renewable energy sources. Detailed device geometry as well as working principles will be described in the following sections.

Part II: Experimental Design and Device Working Principle

Device fabrication

Silicon nanowire arrays and silicon nanomesh samples will be fabricated using the superlattice nanowire pattern transfer technique (SNAP) as decribed in previous chapters. After the nanowire array or the nanomesh are fabricated, the contact electrodes and the heaters will be defined by electron-beam lithography (EBL) and e-beam assisted metallization followed by atomic layer deposition (ALD) of the dielectric layer HfO_2 on top of the active silicon. The contact electrodes will be serving as voltage probes and resistive thermometers for the Seebeck coefficient measurements. At the same time, the contact electrodes are used for electrical conductivity measurements. The heaters are used to create the temperature gradient across the device by DC joule heating.

Next, EBL is again used to open patterns of spin-coated poly(methyl methacrylate) or PMMA resist on the device for quantum assembly. The quantum dots are assembled by dip-coating method as reported previously [14]. The device will then be dipped into acetone to lift-off the PMMA resist and the unwanted quantum dots. At last, another dielectric layer will be deposited by ALD followed by the metallization of gate electrode to complete the device. In this device geometry, the QDs are isolated from the ambient by the oxide dielectric and thus are working as floating gates after charge injection. Figure **1** shows the schematics of the device geometry.

Electrical conductivity and Thermopower measurements

Electrical conductivity of the samples will be measured with and without gate potential by a four-point probe setup. Briefly, the gate potential and the strength of the electric field are controlled by injecting different amounts of charge into the quantum dots through the gate electrode. The voltage bias on the gate electrode is then removed. Next, the electrical current is sourced (Keithley 2400 source meter) through two outer electrodes placed at the two ends of the sample. The voltage drop is obtained by a voltage meter (Keithley 6500 nanovolt meter) via another inner pair of electrodes. The resistance of the sample is obtained by the slope of the linear regression fit to the I-V curve.

Thermopower measurements require accurate detection of the voltage drop, ΔV, and the temperature difference, ΔT, across the sample. ΔV will be obtained via the two inner electrodes (same device configuration as described previously in electrical measurement section) and a voltage meter. ΔT, on the other hand, can be determined by the resistive

thermometer design. In short, an ac current will be sourced through the thermometer electrode while the ac voltage drop is read out by another pair of leads on the same thermometer. The resistance of the thermometer will then be determined and the temperature of the thermometer can also be obtained by fitting the resistance to the temperature vs. resistance calibration curve. Detailed temperature detection procedure can be found in Chapter 3 and the report by Yu et. al [13].

Energy barriers by electric field effects (EFE)

In a field-effect transistor (FET), the EFE is used to control the shape of the conducting channel; in other words, it controls the conductivity of the charge carrier in the semiconductor device. The EFE functions as a physical gate that regulates the flow of charge carriers from the source terminal to the drain terminal. Applying this scheme to a TE element, the source terminal is the heat source (hot end) and the drain terminal is the heat sink (cold end). In a p-type depletion mode transistor (normally "on" at zero gate voltage), a positive bias on the gate depletes the holes in the channel a down-regulates the carrier flow. In the case when the source-to-drain voltage V_{DS} is much smaller than the gate bias V_G, which is the case in the proposed device scheme ($V_{DS} \sim 1-10mV$ and $V_G \sim 0.1-10V$), the gate functions as a variable transistor and the device is in linear mode or ohmic mode. The relation between the source-to-drain current I_{DS} and the gate voltage can be described as:

$$I_{DS} = I_{DSS}\left[1-\left(\frac{V_G}{V_G(off)}\right)\right]^2 \quad \textbf{. (4.5)}$$

I_{DSS} represents the source-to-drain current at zero gate voltage. $V_G(off)$ represents the "off" state gate voltage. In essence, the applied voltage introduces an energy barrier on the conduction channel; the larger the gate voltage or EFE, the higher the energy barrier. In this proposal, we use charge-injected quantum dots as floating gate materials to create the energy barriers to selectively scatter the low energy charge carriers.

Quantum dot size and the barrier height

In enhanced-mode metal-oxide-semiconductor field effect transistors (MOSFET), the threshold voltage represents the gate voltage required to cause the forming of charge carrier flow (inversion layer) at the oxide-semiconductor interface of the transistor. In electronically erasable and programmable nonvolatile memory devices, charge injection or tunneling into the floating gate causes the threshold voltage shift. The magnitude of the threshold voltage shift is related to device parameters such as oxide thickness and dielectric constants. In floating gate memory devices, the amount of charge stored in the floating gate also controls the threshold shift. Physically, the threshold shift reflects the strength of the electric field from the charged quantum dot over the transistor.

Hanafi et al. showed that the threshold shift of the quantum dot memory device could be described as [15]

$$\Delta V_T = \frac{qn_{QD}}{\varepsilon_{ox}}\left(t_{oxide} + \frac{1}{2}\frac{\varepsilon_{ox}}{\varepsilon_{Si}} r_{QD}\right) \quad \textbf{. (4.6)}$$

q is the magnitude of electronic charge, n_{QD} represents the density of quantum dots, ε are the permittivities, t_{ox} is the thickness of the control oxide, and r_{QD} is the size of the quantum dot. Based on this expression, the potential energy barrier introduced by the quantum dots could be controlled by the amount of charge stored in the quantum dots, the density of the dots, the size of the dots, and the thickness of the control oxide as well as the oxide materials. In this proposed study, we will explore these parameters to optimize the power factor of the device.

Charging quantum dots with the control gate voltage

The charge is injected into the quantum dots by Fowler-Norheim tunneling mechanism when a bias voltage is applied at the control gate. The required control voltage to inject the charge is found to be [16]

$$\Delta V_{GS} = (\text{quantum energy level spacing} + \text{charging energy}) / q \cdot (1 + \frac{C_{tt}}{C_{CG}}) \quad \textbf{. (4.7)}$$

C_{tt} is the dot-to-channel capacitance and C_{CG} is the gate-to-dot capacitance. The quantum dot charging energy is related to the size of the quantum dot and the number of electron/hole by the following equation [17]

$$\Delta E = \frac{(nq)^2}{C_{QD}} = \frac{(nq)^2}{4\pi\varepsilon_0\varepsilon_r r} \quad \textbf{. (4.8)}$$

Equations (4.6)-(4.8) provide us useful guidance in controlling the energy barrier by changing the size of the quantum dots, the magnitude of the control gate voltage and the oxide thickness.

Working principle

In this proposal, quantum dot clusters (QDC) are assembled periodically in proximity to the TE material. After charge injection, each QDC creates a local electric field that induces energy barriers for selectively scattering off the low energy charge carriers. The periodic electric field generated by the QDC resembles the energy barriers in the cross plane thin film superlattice (Figure 2). As depicted in Figure 2, although the electrical conductivity is generally high for heavily doped semiconductors with Fermi level deep into the band, the thermopower in this case is often times small because the Fermi level lies very close to the differential conductivity peak maximum. The trade off between the electrical conductivity and the thermopower renders the heavily doped semiconductor unattractive for thermoelectric applications. Exploiting the potential energy barriers generated by the charge-injected quantum dots, we can enhance the thermopower by creating asymmetry in the energy distribution of electrical conductivity, with little adverse effect on the total electrical conductivity.

Conclusion

Silicon nanowires and silicon nanomeshes exhibit thermal conductivities two orders of magnitude smaller than the bulk silicon. Experimental evidences imply that these material systems could achieve ZT greater than 2 if optimized. In this proposal, we expect to enhance the thermoelectric power factor of these silicon nanostructures by an energy filtering approach. Unlike conventional energy filtering approaches based on superlattices with restricted material systems, this proposed work uses electric field effect to generate

potential energy barriers for charge carrier scattering. The barrier heights are readily controlled by the amount of charges injected into the quantum dots, the size of the dots, and the thickness of the dielectric layers. Such device architecture has no physical interfaces along the charge carrier transport path, whereas in superlattices the imperfections of the interfaces often times reduce carrier mobility. Lastly, the proposed device scheme is in principle applicable to all semiconductor TE systems.

PHONONIC SUPERLATTICE THERMOELECTRIC DEVICES

In Chapter 3, we demonstrated that exploiting the phonon wave nature could effectively reduce the lattice thermal conductivity in silicon, while maintaining bulk-like electrical properties. According to theory, discernible wave interference requires the mean-free-path (or the coherent length) of the phonons to larger or of the same order as the characteristic lengths of the sample (Chapter 3 and reference [18]). In the case of silicon nanomeshes, the pitch of the Bragg reflectors (voids in the film) is similar to the phonon mean-free-path set by the critical dimensions in the sample (i.e., ~ 20 nm). Under such conditions, the phonon wave-nature is important and the band folding effect is observed.

Although the coherent scattering mechanism in the nanomesh length scale (a few tens of nanometers) provides a possible route to approach or break the lower thermal conductivity limit of silicon predicted with bulk dispersion (Chapter 2), scaling up the nanomesh structure in bulk materials for large scale applications is technologically challenging. In this section, a phononic superlattice structure fabricated in a bulk silicon film is proposed to reduce the thermal conductivity of the material by both the aforementioned phononic crystal (PnC) mechanism as well as by an additional thermal boundary resistance introduced at the interfaces of the PnC and the blank silicon. The structure can be readily fabricated with modern lithography techniques and is highly scalable.

Kapitza resistance was first discovered in 1941 [19] and states that a temperature discontinuity is present at the boundary when heat is conducted from solid to liquid. Later, Kapitza resistance was also recognized at the interface of two acoustically dissimilar materials (i.e., materials with distinct phonon band structures). Two models have been widely applied to describe the Kapitza resistance: the acoustic mismatch model (AMM) and the diffuse mismatch model (DMM) [20]. In this section, the proposed superlattice structure consists of repeating units of patterned phononic crystal segment and continuous silicon film (Figures 3 and 4). Kapitza resistance is expected to arise at the surface of the patterned voids. Additionally, the interfaces of the patterned segment and the continuous film are also potential locations for the interfacial thermal resistances if the patterned area has noticeable band folding. Under such conditions, increasing the number of superlattice units will substantially reduce the thermal conductivity of the sample.

Device Fabrication

The phononic superlattices are made from SOI wafers with 340 nm SOI and a 1−μm-thick buried oxide layer. The following processes flow explicitly lists all the fabrication steps required in making the device.

1. Thermal oxidation 40 min at 1000°C dry oxidation --> 50 nm oxide. The thermal oxide is used as the etching mask in the later step.
2. 3% PMMA e-beam lithography (120x; 3000, 3000, 1.0; poly fill). This step is to define the hole pattern on the wafer.
3. CF_4 plasma etch. Recipe: CF_4-no-h. Etch time ~ 7 min. (CF_4/He 20 sccm/30 sccm, 10 mtorr, 60 -> 40 Watt). Note: the PMMA is consumed at the end of this etching step.

4. O_2 plasma clean (O_2; 20 sccm; 20 mtorr; 70 watt, 1 min)

5. UCLA DRIE (Bosch process. 6 sec x 2)

6. CF4_no_h again to remove the top thermal oxide (~ 7 min)

7. E-beam lithography to define the heaters/thermometers/leads.

Writing parameters:

thermometers (L2): 200x; 150; 250; SS:1.0; line dose 1.6

heaters (L3): 200x; 250; 250; SS 1.0; AD 500

leads pads (L4): 200x; 700; 700; SS 3.0; AD 500

leads (inner; L5): 120x; 150; 250; SS 1.0; LD 1.4

leads (outer; L6): 50x; 800; 800; SS 5.0; AD 500

(Metal deposition: Ti/Pt = 200/1200 A)

8. Wire bonding pad contacts (Ti/Pt/Au=200/300/2400A)

9. Deposit 6000 A of Al at a rate of 3 A/second by e-beam PVD (CHA) for device and monitlithic contact definition and a monitor area on the side for film thickness check. (a nice lift-off takes 5-6 hours.)

E-beam writing parameters for these features:

Device protection & Monolithic contact(Layer 8): 120x; 700, 700, SS 3.0; AD 500

Monitor section (L 9): same as above

10. Use swab to paste some 3% PMMA on the outer part of the device for reserving the silicon. Bake the PMMA at 180C for 1min.

11. Silicon etch. RIE Recipe: SF6_ENPD. Etching time ~2 min plus 30 second extra etch.

12. Remove PMMA with acetone bath --> this could take up to 10 min or more because the PMMA is thick!

13. Remove Al by PAE (100°C for 5 min)

14. Al deposition again for the suspending beams and membranes. (6000 A; 3 A/S)

Layer 10& 11 same writing recipe as L8&L9.

15. After lift-off, spin 6% PMMA at 2000 rpm and bake at 180C for 1 min. (This is necessary to protect the metal leads from damage by the long plasma etch in the later steps)

16. E-beam lithography to open up windows for oxide etch.

17. Oxide etch. Etch recipe CF4_jk. The 6% 2000 rpm PMMA could survive under such plasma condition for 23 min.

18. Remove the PMMA with O_2 plasma (20 sccm, 20 mtorr, 70 watt for 2 min) + acetone bath (5 min).

19. Repeat step 15-18 until the oxide etch is completed. (total etch time~ 70 min)

20. PAE at 80 deg C 7 min followed by PRX-127 at 120C for 15 min.

20. Spin 6% PMMA at 4000 rpm for E-beam lithography of XeF_2 gas inlets.

21. XeF_2 etch at 1700 mtorr 3-4 pulses, 15 seconds for each pulse etch.

22. O2_ENDP2 for removing the PMMA (~7 minutes).

Figure 3 depicts the scanning electron micrographs of the devices on substrate and suspended with different numbers of PnC-Si interfaces. The diameters of the holes are ~130nm with a pitch of 340 nm; and the hole array is arranged in square lattice. Figures 3b-3d are phononic superlattices with various numbers of interfaces. The area ratio of the patterned section and the un-patterned section is kept the same for these samples.

Measurements

The thermal conductance of the samples is measured with the same methodology as mentioned in Chapter 2. The buried oxide layer under the silicon phononic superlattice is not etched because its contribution to the overall thermal conductance of the sample is at most 10 percent among all the samples measured.

Preliminary Results and Discussions

Figure 4 exhibits thermal conductance results of the silicon film with no hole pattern and three phononic superlattices with 8, 16, and 32 interfaces. A slight adjustment in the thermal conductivity is observed between the sample with 8 interfaces and 32 interfaces. The sample with 16 superlattice interfaces appears to have the lowest thermal conductivity among the samples measured.

Interfacial thermal resistance emerges between materials with dramatically different acoustic properties or phonon band structures. Therefore, a strong band folding effect in the phononic section is prerequisite for substantial thermal conductivity reduction in the phononic superlattices. For such, hole arrays with pitch smaller than the phonon mean-free-path is required. Ju et al. predicted that the mean-free-path of the dominant thermal phonon in silicon at room temperature is close to 300 nm [21]. The phononic superlattices fabricated in this study have holes patterned at a pitch of 340 nm, which is right at the same region as the predicted characteristic length scale. Hole arrays with smaller pitches are

expected to introduce enhanced wave effect at the patterned section. Another future direction for effective reduction in thermal conductivity could be a more complex hole pattern, such as the hexagonal hole pattern (Figure 5). As suggested by Mohammadi et al., a hexagonal phononic crystal creates a broader phonon band gap than the square lattice phononic crystals [22].

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Figure 1

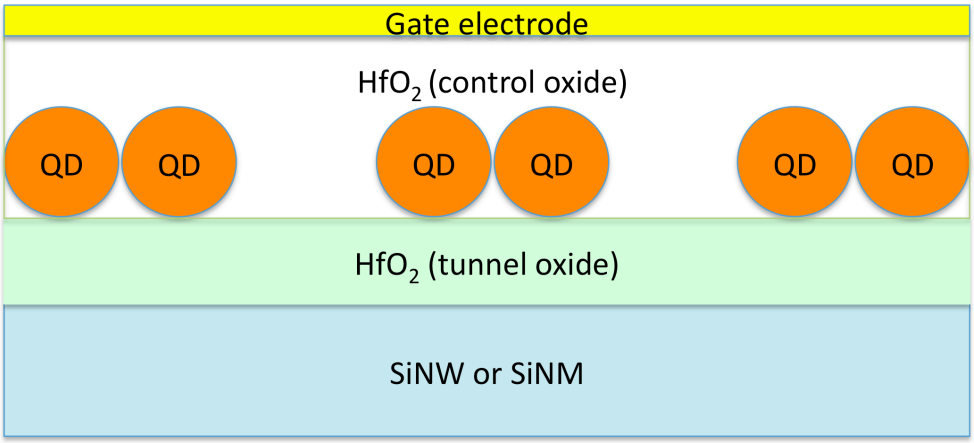
Gate electrode
HfO_2 (control oxide)
QD
QD
QD
QD
QD
QD
HfO_2 (tunnel oxide)
SiNW or SiNM

Figure 2

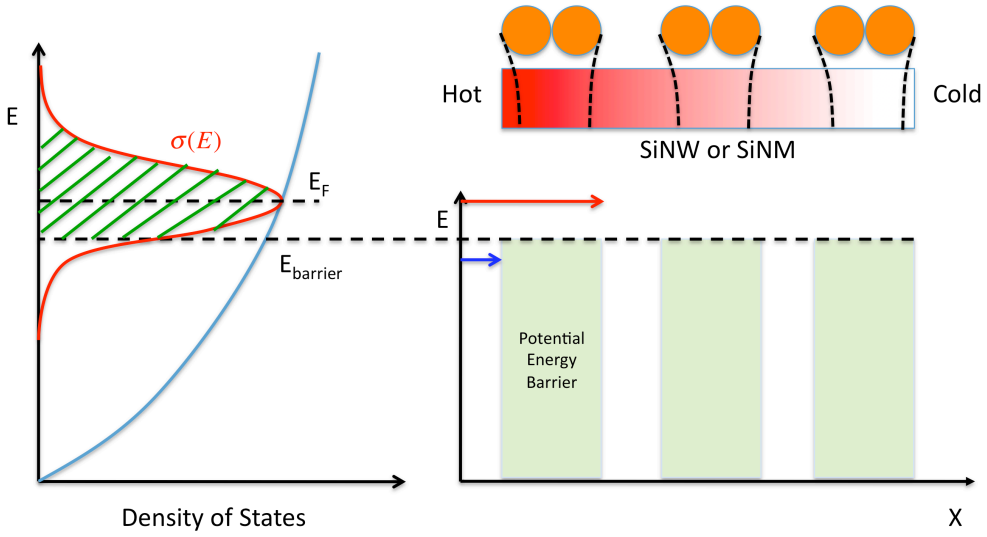
E
$\sigma(E)$
E_F
$E_{barrier}$
Density of States
Hot
Cold
SiNW or SiNM
E
Potential
Energy
Barrier
X

Figure 3

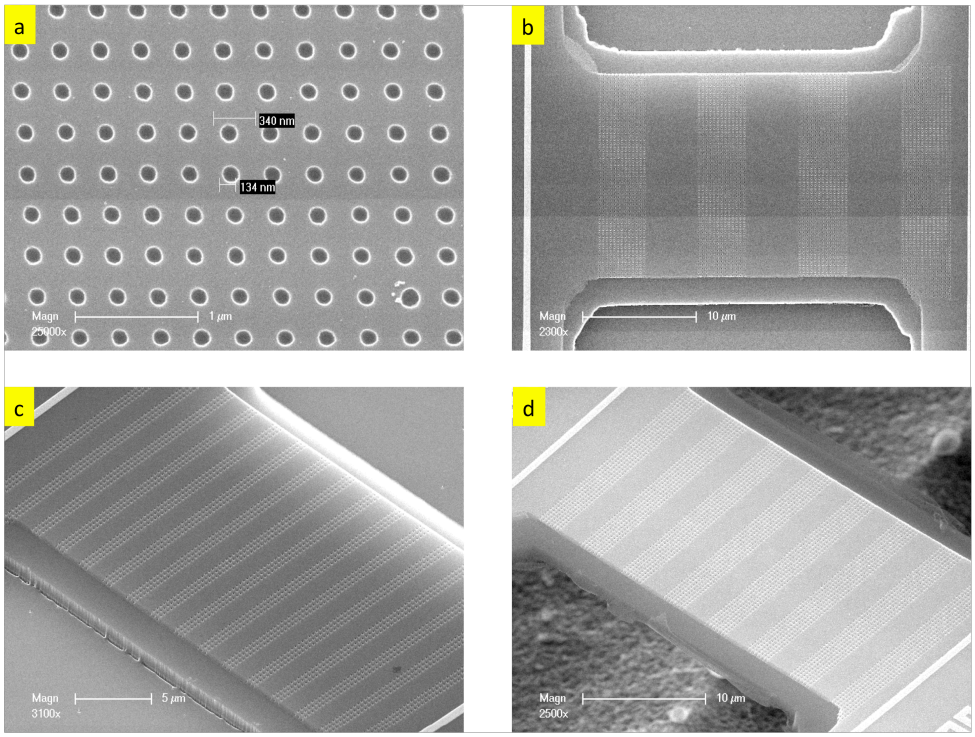
a
340 nm
134 nm
Magn
25000x
1 µm
b
Magn
2300x
10 µm
c
Magn
3100x
5 µm
d
Magn
2500x
10 µm

Figure 4

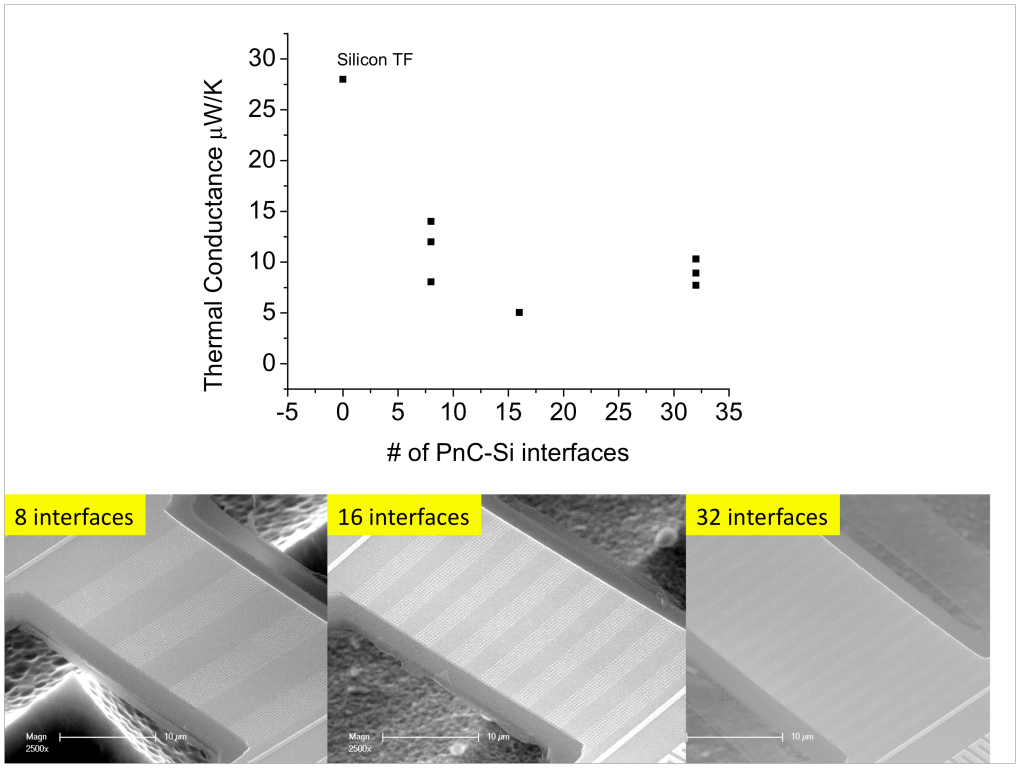
Thermal Conductance µW/K
Silicon TF
# of PnC-Si interfaces
8 interfaces
16 interfaces
32 interfaces

Figure 5

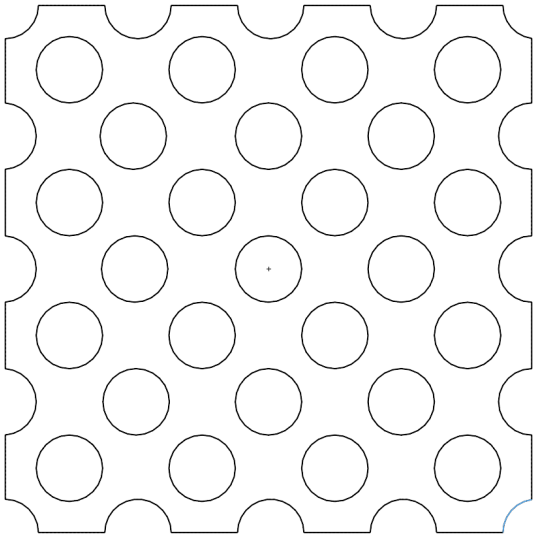

Figure Captions

Figure 1. Schematics of the device architecture.

The quantum dots are embedded in the dielectric layer and serve as electric field centers for the energy filtering devices.

Figure 2. Charged quantum dots serve as electric field centers that create potential energy barriers in the conduction carrier transport path in silicon. These energy barriers reject the low-energy carriers (blue arrow) as high-energy carriers (red arrow and the shaded area on the left) have less influence transporting through. Such energy dependent carrier filtering effect generates asymmetry in the differential conductivity $\sigma(E)$, therefore enhancing the thermopower of the material.

Figure 3. SEM images of the phononic superalattices. (a) a zoom-in image of the hole pattern on the silicon. (b) device with 8 interfaces. (c) device with 32 interfaces. (d) a suspended device with 16 interfaces for thermal conductance characterization.

Figure 4. Thermal conductance of the 320nm thick silicon film and the phononic superlattices with 8, 16, and 32 interfaces. All the samples are suspended with the buried oxide. The devices are sectioned to the same length and width for direct conductance comparison. The buried oxide layer (a separate sample with the same geometrical factors) exhibits thermal conductance around 1 μW/K (data not shown).

Figure 5. Hexagonal phononic crystal structure.