Appendix A

Electronic circuitry

A.1 Designing printed circuit boards

Printed circuit boards provide a convenient platform for assembling electronic circuits. Comprised of sandwiches of alternating insulating and conducting layers (including signal traces and reference planes), proper PCB designs can be a challenging task. Nonetheless, PCB design is one of the most important tasks in achieving optimal performance of the final system. For example, the track length of the PCBs can be shortened to reduce the overall delay[a], and the tracks can be patterned for controlled line impedance in the high-frequency domain by way of transmission lines. In this appendix, I discuss basic technical considerations for designing electronic circuits and for producing PCBs[326,327] with a few examples of digital and analog circuits I have used in the lab. In the 'lab 2 disc', you can find more electronic files for the PCB boards (e.g., high-voltage amplifier, bias coil controller, and phase-sensitive detectors) designed since 2006. For an in-depth treatment of PCB designs and instructions, I refer to ref.[327].

Printed circuit board technology has made great improvements in manufacturing tolerance and board density over the years, but the basic construction layout has not changed significantly. PCB are made out of patterned copper sheets (with etching) on a dielectric insulator such as FR-4 epoxy fiberglass. A simple multilayer PCB consists of (from top to bottom): A silkscreen, top solder mask, top copper plane, inner ground plane, inner power plane, bottom copper plane, bottom solder mask. The silkscreen layer outlines the components and texts (yellow ink). The front and back planes form the component footprints, whereby the vias and traces are etched away. This allows to interconnect components on the same plane (traces) and components from the top to the bottom planes (vias). It is a good practice to order the board with solder masks to prevent solder bridges from forming between adjacent pads and traces.

Also, it may be useful to begin with a multilayer (e.g., 4-plane) board if you have high-power or high-frequency components which may cause electromagnetic interference (EMI) radiation. The two additional copper planes serve as the power and ground planes. This may be useful for high-speed digital circuits, where

[a]For modern digital circuits, it is common to find clock speeds greater than 1 GHz. For high-frequency analog components, the servo bandwidth may be limited simply by the propagation distance of the signals.

one can reduce the power wiring inductance and impedance to the high-speed components. By placing the tracks on the inner planes (i.e., creating a stripline), the outer conducting planes can shield high-frequency radiation and improve the noise immunity of the circuit. Since any through-hole pad on a four-layer board can be connected to or isolated from either of these planes, the ground and power planes can also be used to reroute the signals.

Here is a standard workflow for developing a simple PCB board:

1. Capture the schematics and circuit diagrams.
2. Design component footprints.
3. Establish PCB outline.
4. Set up design rules.
5. Place components.
6. Manually route traces and auto-router.
7. Export into Gerber format.

While there are excellent programs available at low cost, I have used a free CAD program (also a PCB manufacturer), called 'ExpressPCB', for drawing the schematics and the PCB layouts and for ordering the boards.

A.2 Multilayer board design

A.2.1 Vias

A via connects (top and bottom) layers on the PCB using plated through holes (PTH) technology. The PCB board is drilled and the inner surface (of the cylinder) is plated with silver. For connecting to high-power planes, the via's size should be chosen with care (see section A.2.3). For multilayer design, vias can also be formed between the inner layers (buried vias), and between the outer layer and one of the internal layers (blind vias). For smaller sizes < 6 mil, microvias can be formed to achieve higher component density by deforming the copper plane with a high-power laser. Note that vias cause discontinuity in the line impedance for $\nu > 10$ MHz, and surface mount components are preferable for connecting the pins to traces (or a patterned transmission line for microwave frequency, section A.2.3).

A.2.2 Pads

A pad is a small conducting surface made out of copper used for a component pin. As a standard, it is useful to identify the ground pin (or pin #1) of the component with a square pad, and the signals with round pads.

An anti-pad can be used to isolate the pin to the copper plan. A thermal pad can be used to restrict the heat flow when the pin is connected to one of the copper planes. For PTH vias, as a general rule of thumb, it is good to keep a pad-to-hole ratio of 2:1.

A.2.3 Traces

A trace connects two points on the PCB by etching away the copper plane. The trace on the PCB is a copper stripline (rectangular cross-section) not a wirebound (circular cross-section), and the depth is set by the PCB manufacturer (typically, $d \simeq 1.5$ mil). A tricky problem is to set the width w of the trace for a given length l. This requires several considerations including power and heat management (for high-current traces), breakdown voltage in atmosphere and dielectric constant of FR4 (for high-voltage traces), and wire impedances (for high-frequency signal traces and digital logic), as further described in section A.3. When placing a trace, it is usually good to keep a space of > 7 mil between the traces and between any adjacent conducting pads. Otherwise, the etching process may develop hairline shorts or openings. I also refer to the concepts of 'electric clearance' and 'creepage distance' in section A.3.2. For narrow traces below $w < 12$ mil, it is good to put a chamfer for a 90° bend, formed with two short 45° angle bends. To avoid crosstalk between two traces above a ground plane, it is good to decrease the distance between the plane and trace as much as possible, and increase the distances between traces. The crosstalk coupling between two traces scales as $\propto \frac{l}{(1+(\Delta d/\Delta h)^2)}$, where Δd is the shortest distance between the two traces, Δh is the distance from the ground place to the traces, and l is the length of the traces. With most CAD programs, one can write a design rule to specify the minimum trace widths and maximum bending angles at the fabrication tolerances of the PCB manufacturer.

A.2.4 Planes

A plane is an uninterrupted conductive area of the entire PCB layer. Traces are formed by etching out a plane and by isolating from the power planes to distribute power and signals to the PCB components. It is very important to have at least one dedicated power and ground planes as low-impedance reference planes. If the system is composed of mixed analog and digital circuits, it is important to separate analog and digital ground and power planes. The analog ground plane should be placed below the analog power plane, and the digital ground plane underneath the digital power plane, with no overlap among the four planes (check the vias!). The analog and digital traces will run on the surface of the PCB board, while the inner planes will shield the analog components from the high-frequency radiation and noise of the digital ground. For high-frequency application, it is good to avoid the signal traces on the ground plane, as the discontinuity in the ac current flow can lead to EMI. While an uninterrupted ground plane can be thought as a reasonably good low-impedance reference, for traces running with high-frequency (> 1 MHz) current, the inductive coupling sets a specific path for the return loop current, which tends to minimize the loop area. The return current, thus, flows on the

ground plane underneath the signal traces[b]. For high-current application, it may be good to consider putting a star ground or a split ground plane to the main power filter.

A.2.5 Components

There are many types of packaging available today, some of which include PTH components, surface mount, and wirebound components. Metallic components such as heat sinks, crystals, switches, connectors may cause shorts if placed over traces on the top layer. If one must be placed above the trace of the top layer, it may be important to consider the dielectric constant of the surface mask (i.e., the green insulating layer on the surface planes). Wirebound components, which usually have a nice integrated heat sink, are useful for high-power applications. Both the PTH and wirebound components may be detrimental for high-frequency applications as the discontinuity in the solder joint may cause EMI radiation or significant voltage attenuation from the high-contact impedance (see section A.3.3). In this case, it may be a good idea to find an alternative surface mount component.

A.3 Technical considerations

A.3.1 Leakage resistance

Leakage resistance is a static circuit board effect, where contaminants on the PCB surface (e.g., flux residues) cause leakage currents across the circuit nodes. Ref.[327] suggests a simple cleaning method: (1) wipe the PCB with isopropanol, (2) wash with deionized water, and (3) bake at $85°C$ for a few hours. Another method to prevent leakage currents is to "guard" the sensitive signal tracks and power lines by surrounding with the ground planes exposed above the coating in order to sink the leakage current.

A.3.2 Electrical clearance and creepage distance for high-voltage applications

The electrical clearance is the minimum distance between two conductive high-voltage traces, where a dielectric breakdown occurs between the traces by air ionization (depending on humidity, altitude, and temperature). According to ref.[327], it is good to restrict the minimum distance between tracks to 315 mil. Similarly, a creepage distance is the shortest distance between two conductive traces, whereby the dielectric breakdown occurs along the insulation (FR4, relative dielectric permittivity $\epsilon_{\text{FR4}} \simeq 4.5$ and dielectric breakdown $\simeq 40$ kV/mm). It is important to keep the tracks separated with distances larger than the creepage distance to avoid localized conduction on the insulating surface by electric discharges.

A.3.3 High-frequency electrical transmission lines

The induction of a copper trace plays an important role for high-frequency analog devices and for high-speed digital logic. A wire inductance (for wirebound components) is given by $L_{\text{wire}} = 0.2$ (nH/mm) $\times l[\ln(2l/r) - 0.75]$, where r is the radius of the wirebound. A strip inductance (e.g., for copper trace) is $L_{\text{strip}} = 0.2$ (nH/mm) $\times l[\ln(2l/(w+h)) + 0.22(w+h)/l + 0.5]$. For optimal EMI reduction, high-frequency signal traces should be embedded in the internal layers between power or ground planes, forming a stripline transmission line, where the power planes shield the high-frequency radiation.

First, it is important to determine whether or not a transmission line is needed. For a high-speed logic with rise/fall time t_r, the trace needs to be terminated with their characteristic impedance if the track length l is greater than the characteristic length $l_c = v_s t_r$, where the signal travels conservatively at a speed of $v_s \simeq 2$ in/ns. Similarly, in the analog domain, an active non-inverting amplifier with a maximum bandwidth of f_m has an equivalent rise time $t_r = 0.35/f_m$. Thus, one should consider transmission line techniques when placing signal tracks with $l > l_c = v_s t_r$. There are two typical high-frequency transmission lines (i.e., microstrip and stripline transmission lines), which are relatively simple to fabricate on a PCB. The determination of the parameters to obtain a good transmission line depends on the thickness of the dielectric layer to the reference plane, dielectric permittivity of the insulating layer, the routing copper thickness, and the trace width. Note that vias cause discontinuities in the characteristic impedance of a transmission line.

A.3.3.1 Microstrip transmission line

A simple method for a two-layer PCB is to use the ground plane and a signal trace for controlled impedance, as shown in Fig. A.1a. This geometry is known as a microstrip transmission line[326]. The characteristic impedance of a microstrip is given by

$$Z_{\text{micro}} \simeq \frac{87}{\sqrt{1.41 + \epsilon_{\text{FR4}}}} \ln[6h/\pi(0.8w + t)]. \tag{A.1}$$

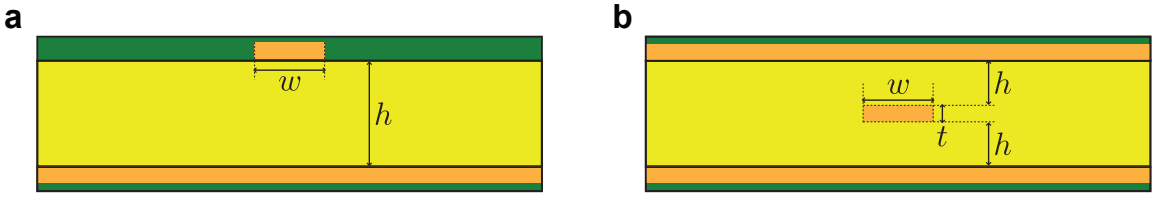

Figure A.1: **Controlled impedance transmission lines. a**, Microstrip transmission line. **b**, Stripline transmission line. The layer thickness t and depth h are usually set by the manufacturer. By choosing the width w of the track, one can control the impedance of the transmission line. The green layer is the insulating silk screen, the yellow layer is the dielectric FR-4 glass epoxy, and the gold layer is the copper which forms a conductive layer.

[b] In reality, the finite conductivity of the copper plane sets a finite area of the return loop, where the return loop flows 'close' to the signal trace.

In addition to the characteristic impedance Z_{micro}, the microstrip has a characteristic line capacitance of C_{micro} (pF/in) $\simeq \frac{0.67(\epsilon_{\text{FR4}}+1.41)}{\ln[6h/\pi(0.8w+t)]}$. In most cases, the thickness h of the insulating FR4 layer is set by the manufacturer, and the only controlled parameter is the width w of the track. By setting the value of w, the impedance Z_{micro} can be set to typical values of 50 Ω or 75 Ω for impedance matching. For typical value of $\epsilon_{\text{FR4}} = 4$ with $h \gg t$, $w/h \simeq 2$ gives 50 Ω impedance. The signal propagates in the microstrip transmission line at a velocity of v_{micro} (in/ps) $= \frac{1}{85\sqrt{0.475\epsilon_{\text{FR4}}+0.67}}$.

A.3.3.2 Stripline transmission line

For a multilayer PCB, a preferred choice is to pattern a stripline transmission line for the signal track, by embedding the signal trace between the power and ground plane, as shown in Fig. A.1b. A sandwich of the two low-impedance ground planes and the embedded signal trace forms a symmetric stripline. Because of the inductive coupling, the return current paths for the high-frequency signal trace are located on the planes directly above and below the signal trace (see section A.2.4). Thus, the high-frequency signal is tightly confined within the signal trace (see also section A.3.4), thereby minimizing emissions and shielding the tracks from the environment.

The characteristic impedance of a stripline transmission line is given by

$$Z_{\text{strip}} = \frac{60}{\sqrt{\epsilon_{\text{FR4}}}} \ln[6(t+2h)/\pi(0.8w+t)]. \tag{A.2}$$

In addition, a symmetric stripline has a characteristic capacitance of C_{strip} (pF/in) $\simeq \frac{1.41\epsilon_{\text{FR4}}}{\ln[3.81h/(0.8w+t)]}$. The signal propagates in the stripline transmission line at v_{strip} (in/ps) $= \frac{1}{85\sqrt{\epsilon_{\text{FR4}}}}$.

A.3.4 High-frequency skin effect

Signal currents at high frequencies tends to flow through the perimeter of the conductive trace due to inductive coupling. The skin depth causes an effective conduction area of ac-current flow smaller than the cross-section of the trace. In addition to the effects of impedance at higher frequencies, the skin effect results in an increase of resistance at higher frequency. The skin depth d_{skin} for copper is approximately given by $d_{\text{skin}} \sim 2$ (μm $\sqrt{\text{GHz}}$) $/\sqrt{f}$. Assuming an effective cross-section for the current flow by a flat-top profile $A = w \times d_{\text{skin}}$, the resistance for copper is then $R_{\text{skin}} \sim 8 \times 10^{-3}$ ($\Omega/\sqrt{\text{GHz}}$) $\sqrt{f}(l/w)$ (see Eq. A.3). For dc-currents, see section A.3.6.

A.3.5 Stray capacitance

The capacitance between two conducting layers with a distance d and area A is $C_{\text{plate}} = 8.9\epsilon_{\text{FR4}}$ (aF/mm) $\times A/d$ (see Fig. A.1), where $d = h$ (Fig. A.1a) or $d = 2h + t$ (Fig. A.1b). A voltage noise V_n on one plane can capacitively couple to another plane with a coupling voltage of $\delta V_c = V_n Z_1/(Z_1 + Z_2)$ where Z_1 is the

circuit impedance and $Z_2 = -i/wC_{\text{plate}}$. To prevent capacitive coupling between two signal traces and two planes, one may insert a ground plane, acting as a Faraday shield between the noise source and the affected circuit.

A.3.6 High-current thermal management

A general rule of thumb is to keep the temperature increase to $\Delta T \lesssim 10^{\circ}C$. The sheet resistance of a trace is given by

$$R_{\text{trace}} = \rho_{\text{electric}} l/wd, \tag{A.3}$$

where $\rho_{\text{electric}} = 1.7 \times 10^{-6}$ Ω cm is the electric resistivity for copper at $T = 300$ K and l is the length of the track[c]. The temperature rise is then $\Delta T = \theta P_{\text{trace}}$, where $P_{\text{trace}} = I^2 R_{\text{trace}}$ is the power dissipation across the trace and $\theta = \rho_{\text{thermal}} l/wd$ is the thermal resistance of copper. The thermal resistivity of copper is $\rho_{\text{thermal}} \simeq 0.25$ cm $^{\circ}C/W$. For reference, the currents required to have $\sim 10^{\circ}C$ increase in temperature for standard track widths are shown in Table A.1. By connecting the signals to an active component (e.g., operational amplifier) in a Kelvin configuration, one can mitigate for the errors arising from the voltage drop across the signal trace, but it requires a negative feedback. Instead of using traces to ground the pins, star-grounding[326] to the main power filter or the usage of split ground planes (causing an effective star grounding) helps to obtain a good ground with low impedance[d].

Table A.1: **Thermal management of a copper trace.** We show the current I_{trace} required for a $10^{\circ}C$ increase in temperature for a sheet copper of depth $d = 1.5$ mil with various width w.

w (mil)	I_{trace} (A)
10	0.3
15	0.4
20	0.7
25	1
50	2
100	4

[c]For low-impedance circuits, one may need to also consider the temperature of coefficient for copper $\sim 0.5\%$ per $^{\circ}C$ at 300 K. Also note that the manufacturer often quotes the trace thickness d in the units of ounces of copper per ft^2, with common thicknesses 0.5 oz, 1 oz, 2 oz. For power traces, it is good to use 2 oz.

[d]Instead of using a ground trace, it is generally a good idea to have a ground plane, as the plane can be used as a low-impedance reference.

A.4 Control logic and buffer circuits

For the experiments in chapters 6–9, the slow cycling rate 40 Hz for the laser cooling and trapping stages is derived from a time base of the digital pulse generator (SRS DG535), which in turn triggers two phase-locked 16-output digital delay generators (SRS DG645). The overall system provides robustness compared to the previous generation (chapters 3–5) by integrating with proper buffer and line drivers (SN74ABTH25245) for better impedance matching and for sinking the large amount of current when "power gating" multiple single-photon avalanche photodiodes[e] (Perkin Elmer SPCM SQRH-16). The experimental repetition rate (2 MHz) is synchronized to a master clock running at 100 MHz (time base, 25 ppm 100 MHz crystal oscillator, with rms jitter of < 400 ps) via downconversion. A multiplexed pulse generator (quantum composer 9518^{+}) is controlled by Labview through USB interface. The TTL pulses generated from the quantum composer in burst mode are fed into a control logic, which relay or inhibit the signals conditioned on the photoelectric event at the SPCMs, with the rising edges of the pulses corresponding to the instants of detection.

As shown in Fig. A.2, the logic circuit consists of (i) dozens of control logic and gate pulse circuits, (ii) a memory gate pulse generator, and (iii) a field 1 sync circuit. Here, I describe the functions of each of the components: (i) The control logic relays the signal if the memory pulse (mem) is high. (ii) For the memory gate pulse generator, a field 1 pulse (red line) is split into multiple paths by a high-speed 1-8 clock distributor (CDC341), with one arm triggering a monostable multivibrator (74LS123ND) on the rising edge for a maximum wait time of τ_w (ns) $= 6 + 0.05C_m$ (pF) $+ 0.45R_m$ (kΩ)$C_m + 11.6R_m$, thereby relaying a logical 0 up to τ_w regardless of the input. If the monostable multivibrator detects a falling edge in the clear signal (CLR, black line) at $\tau_m < \tau_w$, the output (memory pulse) is raised to a logical 1-state (green line). Otherwise, the output is raised to t_w regardless of the state of CLR. In turn, the clear signal (CLR, black line) is generated from a triggered delay generator with programmable delay τ_m. (iii) The photoelectric detection event of field 1 can arrive randomly within the detection window. Field 1 sync circuit relays a pulse synchronized to the external master clock if a field 1 is registered.

In Fig. A.3, I show the printed circuit board for the control logic and the line drivers. All outputs of the logic circuit undergo a set of line drivers to provide proper impedance matching. The track lengths are significantly shorter than the characteristic length $l_c = v_s t_r$ given the typical rise-time of the logic ~ 1 ns (section A.3.3). Long tracks are optimized by employing microstrip transmission lines and line drivers.

[e] The bias voltage in the APD is abruptly turned off in $\ll 1\mu s$ by sinking ~ 380 mA at the gate voltage input of SPCM SQRH-16. When the bias voltage is zero, we can send significant amount of light onto the APD for acquiring the lock of interferometers without modifying the noise characteristics and quantum efficiency of the detector.

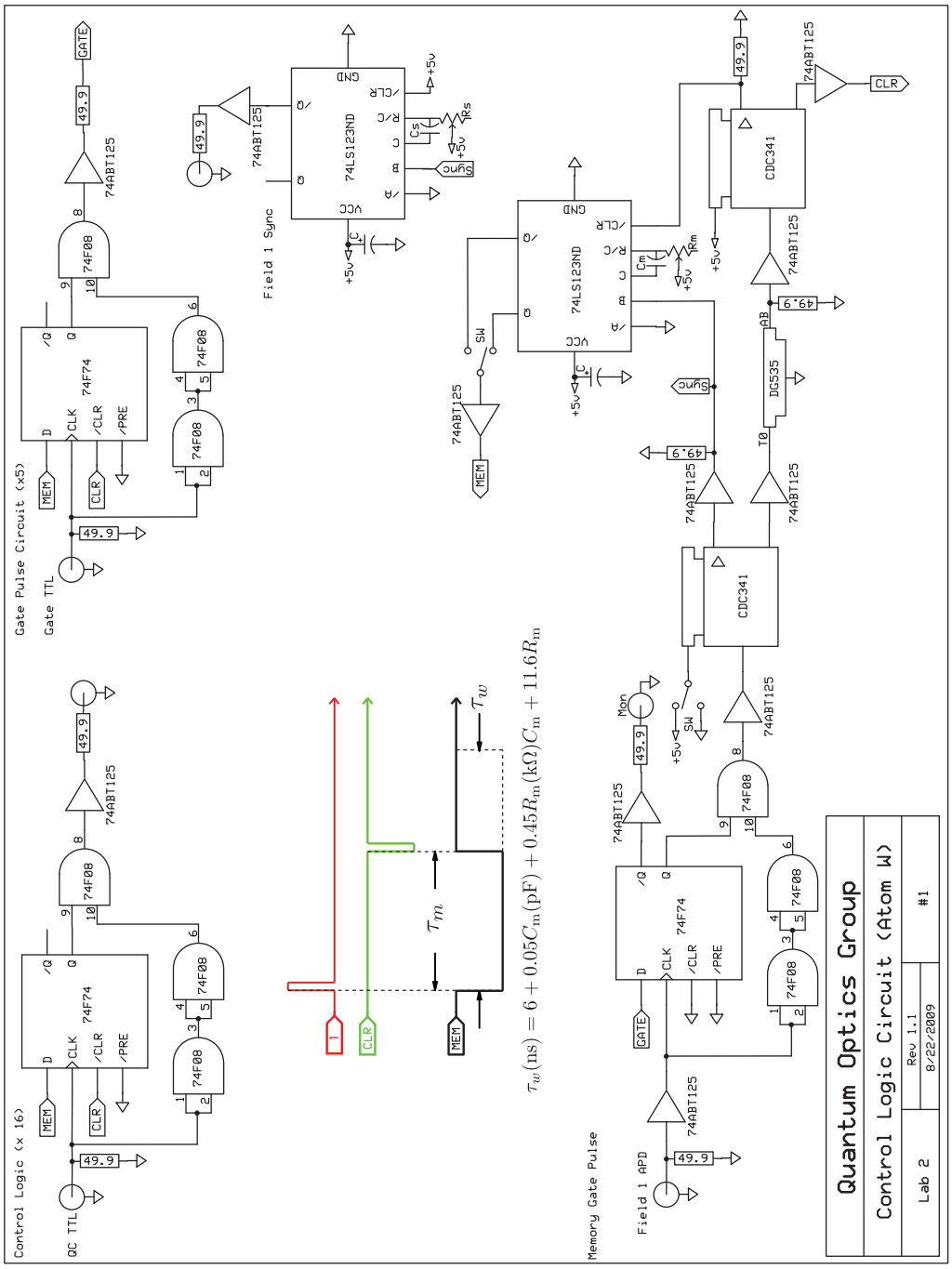

Figure A.2: **Circuit diagram for conditional control logic for triggering and relaying various signals.** The logic circuit consists of (i) control logic and gate pulse circuits, (ii) a memory gate pulse generator, and (iii) a field 1 sync circuit.

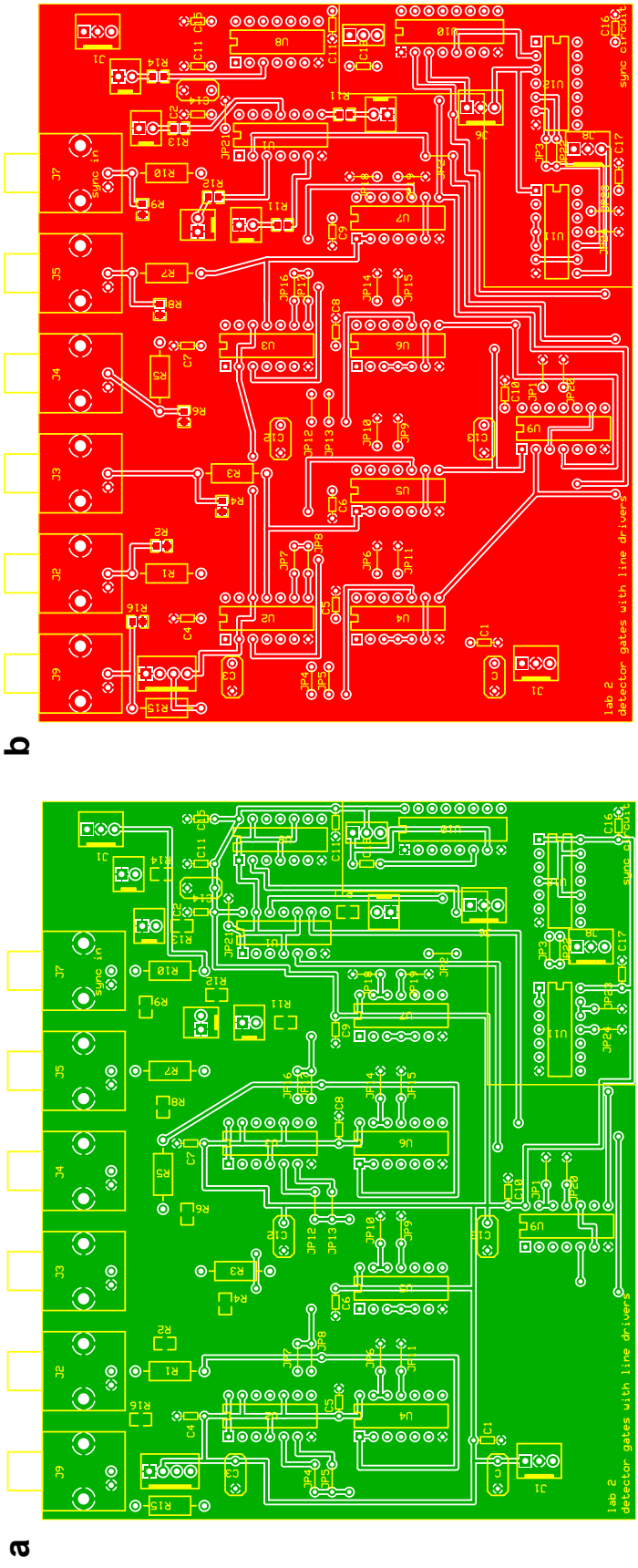

Figure A.3: **PCB board for conditional control logic for triggering and relaying various signals.** The logic circuit consists of (i) control logic and gate pulse circuits, (ii) a memory gate pulse generator, and (iii) a field 1 sync circuit.

A.5 Laser diode current controller

The diode laser systems in our group have evolved over time. While the mechanical aspects of the laser systems remain largely the same, new types of lasers have been introduced to lab 2, including an external cavity interference filter laser[f 151,328]. Because of obsolete parts in the previous design of our group (by Joseph Buck), Aki and I redesigned the laser diode controllers, including the current controller, temperature controller, and FET modulation board. The current controller is still based on the original design[329] by K. G. Libbrecht and J. L. Hall, but I made some improvements to the circuit in a source/sink configuration in terms of temperature stability and noise characteristics of the circuit. Also, an override function was added. The temperature controller[330] and the FET modulation board remain the same, where we replaced the obsolete voltage reference.

I show the circuit design for the laser current controller in Fig. A.4 and the PCB layout in Fig. A.5. A negative (positive) voltage regulator, LM337 (LM317), provides the stable supply voltage with slow turn-on and current limit to the diode laser in the sink (source) mode. The precision voltage reference, LM399 (or LTZ1000 for better thermal stability 0.05 ppm$/^\circ C$) is heavily filtered to reduce noise, and the RC network in the LT1028 circuit provides stable operation with low noise. The Vishay sense resistor (VHP-4) is wired in a Kelvin configuration for dc-current stability. Low-level current modulation (Mod) is used for driving the error signal from dc to ~ 10 MHz, and an ac-coupled input (RF in) is used for RF-sideband modulation.

[f] More details on the interference filter laser, which Julien and I built during his visit in the summer of 2008, can be found in my lab notes.

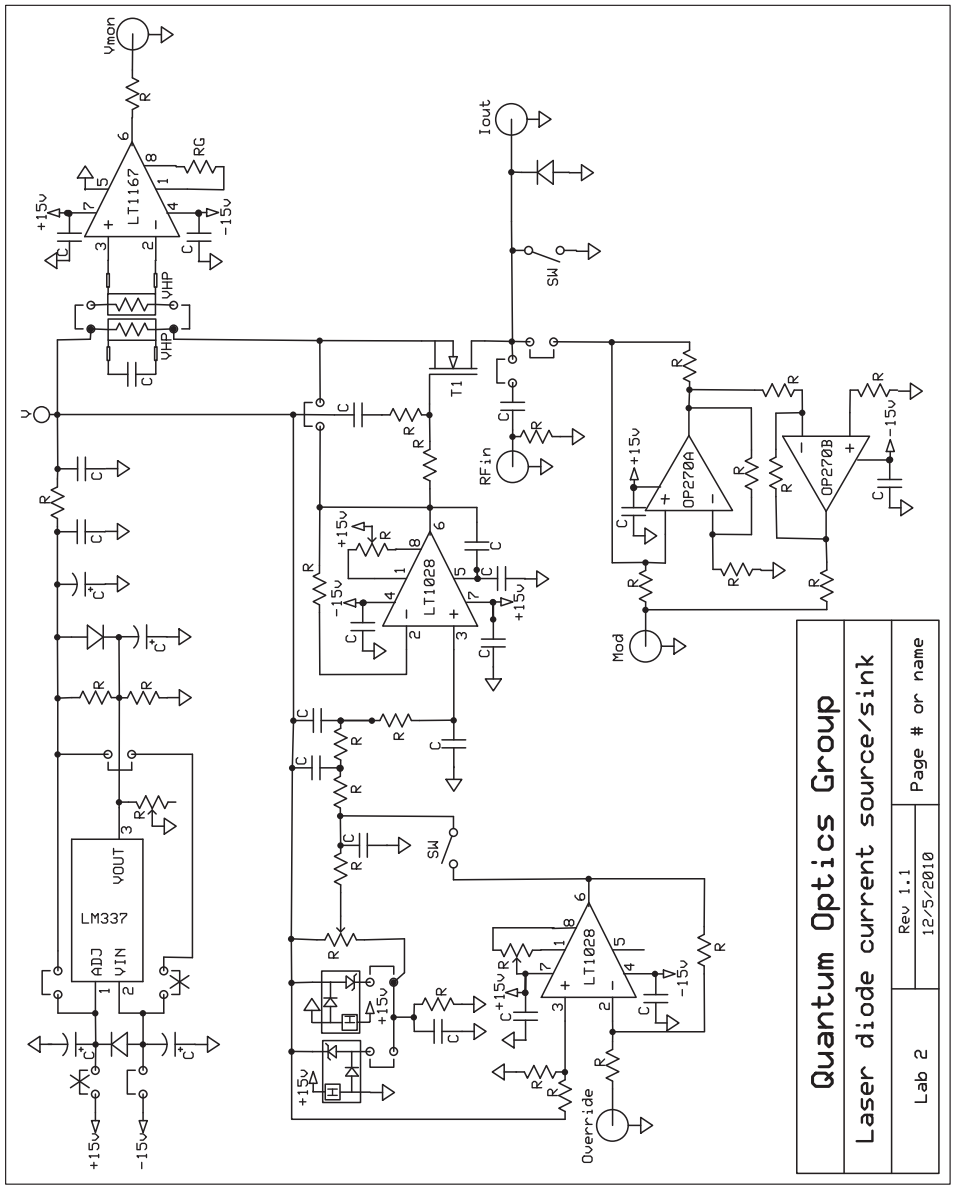

Figure A.4: **Circuit diagram for diode laser current controller.** The circuit diagram is shown for a current sink. For an analogous current source circuit, one needs to replace the negative voltage regulator LM337 with a positive one LM317, and connect the voltage reference LTZ1000 in a opposite manner.

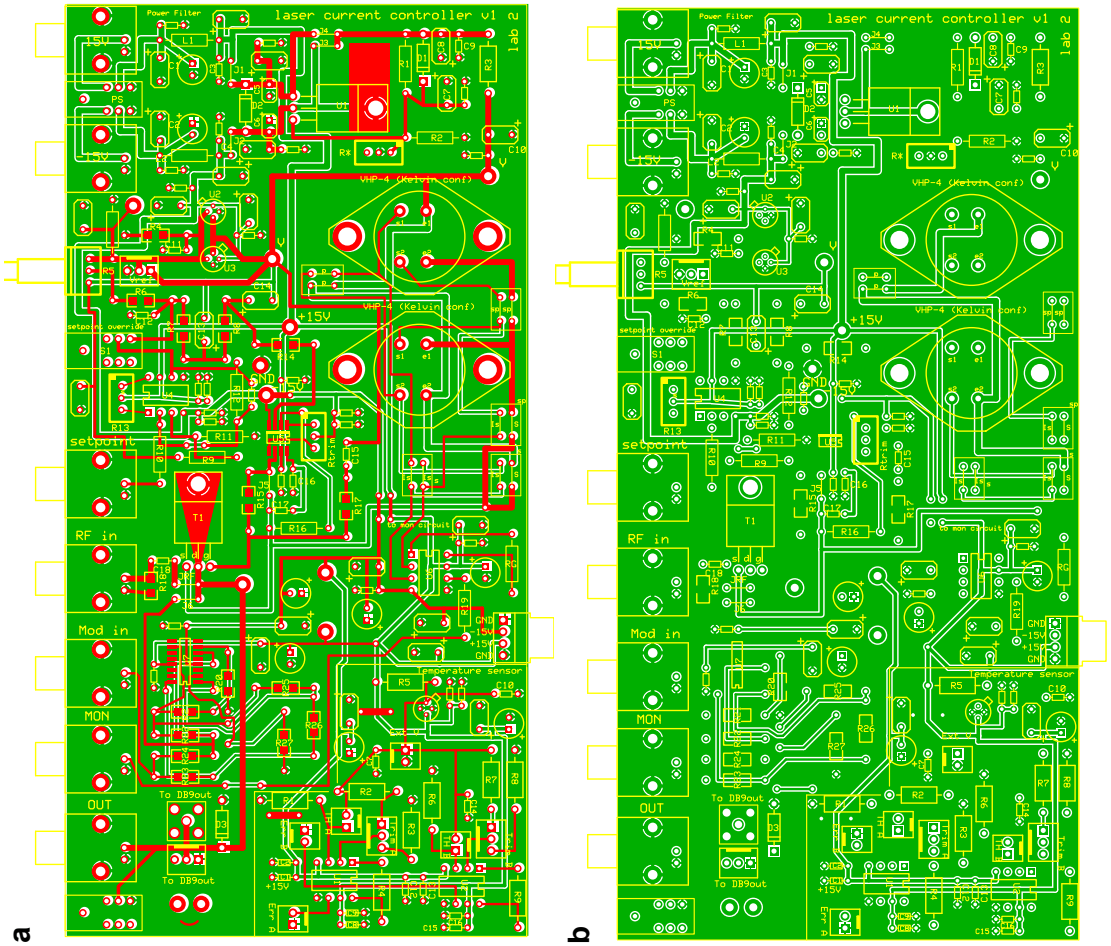

Figure A.5: **PCB board for laser diode current controller.** The circuit diagram is shown for a current sink. For an analogous current source circuit, one needs to replace the negative voltage regulator LM337 with a positive one LM317, and connect the voltage reference LTZ1000 in a opposite manner. The PCB also includes a small area dedicated for the temperature sensor with a bridge circuit.

A.6 Locking circuits for interferometers and intensity stabilization

For the experiments in chapters 8–9, we locked the verification interferometer via an *ex-situ* phase modulation spectroscopy. An important part of this technique is the capability to acquire and stabilize the interferometric phase to ϕ_0, to sample and hold (S&H) the phase ϕ_0 value over the experimental duration t_d, and to feed-forward an offset phase $\phi_{\text{exp}} = \phi_0 + \delta\phi$ during t_d. The power gating and the MEMS switches protects the single photon APDs from the strong reference laser. During the experimental phase, the reference laser is extinguished to > 180 dB, and the MEMS switches reroute the fiber optical channels to the single-photon detectors.

The active component of our interferometric stabilization scheme is a fiber stretching module (PZ1, Optiphase) with modulation constant $\beta = 0.4$ rad/V over dc $-$ 20 kHz (see Fig. 8.6). The phase is modulated at ~ 88 kHz (generated from SRS SR830) above the first resonance at $\nu_m \simeq 55$ kHz. The phase modulation is switched off by rf-switches (Minicircuit ZASWA-2-50DR) during t_w. The reference laser is monitored by a photodetector (or by a custom inline evanescent power tap PIN Si-detector, Oz optics OPM-11), resulting in the signal V_{pd}. Two lock-in amplifiers (SRS SR830 and SR510) demodulate the signals V_{pd} to generate error signals V_{der}. The error signal V_{der} and the photodiode signal V_{pd} are fed into the phase stabilization servo, as shown by Fig. A.6. Depending on the application, the two signals are summed or subtracted (i.e., $V_{\text{err}} = \alpha V_{\text{der}} \pm (1-\alpha)V_{\text{pd}}$). The P gain is controlled either by the proportional non-inverting amplifier or by changing the modulation depth, and the I gain is controlled by the integrator (with the variable capacitor). The phase stabilization servo bandwidth is limited to ~ 10 kHz by a Sallen-Key type low pass filter to avoid exciting ν_m of the stretching modules. A set of TTLs (S&H TTL and jump TTL) controls the sample and hold (S&H, LF398), and the jump operations (low-noise switch, MAX319) in the servo. The output of the servo is amplified by a high-voltage ($0-1$ kV) amplifier (Burleigh PZ70), which drives the fiber stretching modules (PZ1, Optiphase). This circuit was modified to stabilize the intensity of a diode laser. The set-point of the lock (i.e., phase set value ϕ_0 or intensity set value I_0) can be monitored at the set-point output and controlled by the error-signal bias point. The jump potentiometer controls the feedforward voltage for $\delta\phi$. For reference, I show the PCB layout for the phase stabilization and intensity stabilization servo in Fig. A.7.

A.7 Other electronics

In the "lab 2 disc", I compile more electronic circuitries in lab 2: Low-noise bias coil controller and servo, buffer circuits, laser current controller and temperature controller, high-voltage amplifier, digital clock distribution circuit, photodiode trans-impedance amplifier, phase-sensitive detector, phase stabilizer, laser diode protection board, piezo servo, dc high-voltage source, temperature sensor, controller for voltage-controlled oscillator (VCO), and high-Q phase reference with a phase-locked dielectric resonator oscillator (PDRO, Herley-CTI).

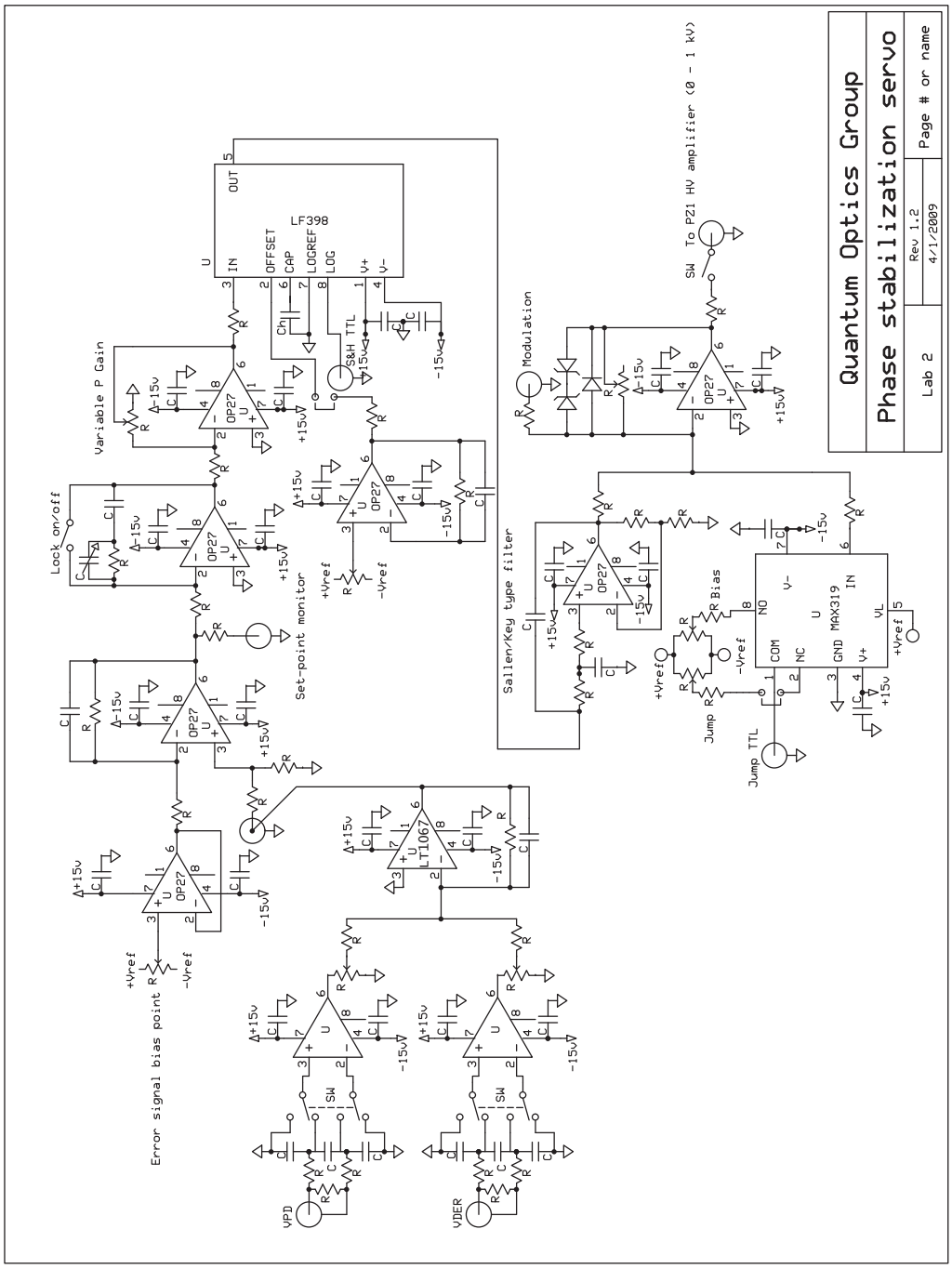

Figure A.6: **Circuit diagram for phase stabilization and intensity stabilization servo.** After acquiring the lock during the laser cooling and trapping period, LF398 samples and holds the output value of the servo during t_d, where the phase of the interferometer is set to ϕ_0. The jump TTL is initiated 3 ms afterwards to trigger a ultra-low noise switch MAX319 to offset the phase to $\phi_{\text{exp}} = \phi_0 + \delta\phi$ of the interferometer. The output of the servo is amplified by Burleigh PZ70.

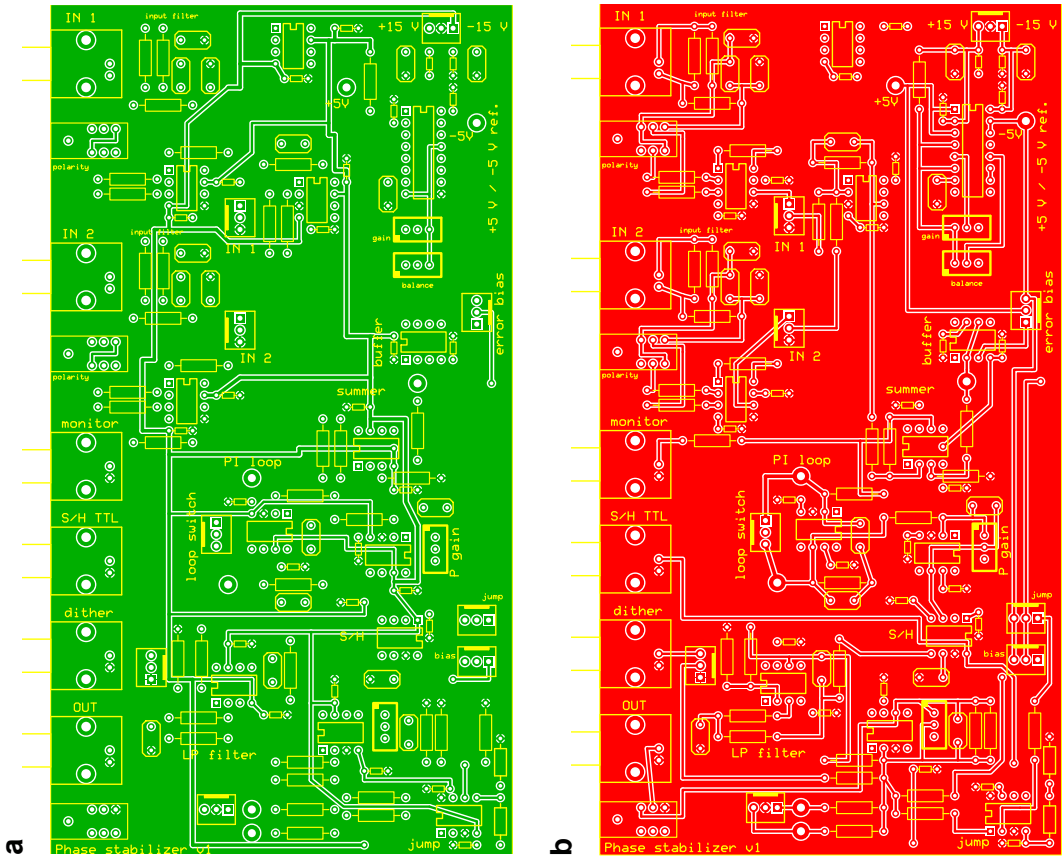

Figure A.7: **PCB board for locking interferometers and intensity stabilization.** After acquiring the lock during the laser cooling and trapping period, LF398 samples and holds the output value of the servo during t_d, where the phase of the interferometer is set to ϕ_0. The jump TTL is initiated 3 ms afterwards to trigger a ultra-low noise switch MAX319 to offset the phase to $\phi_{\text{exp}} = \phi_0 + \delta\phi$ of the interferometer. The output of the servo is amplified by Burleigh PZ70.