Synthesis of PWM and Quasi-Resonant DC-to-DC Power Converters

Thesis by
Dragan Maksimović

In Partial Fulfillment of the Requirements
for the Degree of
Doctor of Philosophy

California Institute of Technology
Pasadena, California

1989
(Submitted January 12, 1989)

Acknowledgements

I wish to thank my advisor, Professor Slobodan Ćuk and co-advisor, Professor R. D. Middlebrook, for accepting me in the Caltech Power Electronics Group, and for their guidance, generous support and encouragement.

I would like to acknowledge the financial support of Caltech (in the form of a Graduate Fellowship) and of the following corporations who supported my Graduate Research Assistantships: Boeing Electronics, GTE Communication Systems, IBM, Merlin Gerin, Rockwell International and General Dynamics.

Credit is due to all present and former members of the Power Electronics Group who have enriched the laboratory with useful computer programs and tools. Thanks go to Steve Freeland for inspiring discussions and for LaTeX files that have been invaluable in the preparation of this thesis. I am grateful to my fellow colleagues for their friendship.

Abstract

Synthesis of DC-to-DC converter topologies in the two largest families – PWM and Quasi-Resonant (QR) – is completed in this thesis.

In a PWM converter, two linear time-invariant networks, consisting of only capacitors and inductors, source and load, are switched at constant frequency with duty ratio D. From defining assumptions, several general properties of PWM converter networks are derived. The established general properties interrelate the number of elements, attainable DC conversion ratio $M(D)$, and features such as continuous terminal currents or possible coupling of inductors.

Based on matrix representation of the converter topology, the systematic synthesis procedure for generation of PWM converters with a given number of reactive elements is constructed. A prescribed set of requirements is the input for the procedure. The requirements may include desired DC conversion ratio, continuous terminal currents, possible coupling of inductors and a given number of switches. In particular, the number of switches implemented as transistors can be specified. Outputs of the procedure are complete classes of PWM converters that satisfy the input requirements. A number of useful PWM topologies, which have not been identified before, are uncovered. A comparison of members of the classes is included.

Several extensions of PWM converters are considered, including insertion of the isolation transformer and two discontinuous operating modes for which unified DC analyses are completed.

Quasi-Resonant converters are defined as two-switch PWM converter networks to which resonant elements are added. Synthesis of QR converters is based on the recognition that there are only a finite number of topologically distinct positions for resonant elements within a two-switch PWM parent converter. If a single resonant inductor and a single resonant capacitor are added to a two-switch PWM topology, examination of

all possible positions yields a total of six QR classes, which come in dual pairs. Two pairs are identified as known QR classes, namely, Zero-Current/Zero-Voltage (ZV/ZC) and Zero-Current/Zero-Voltage Quasi-Square-Wave (ZC-QSW/ZV-QSW). The remaining two classes, named Off-Resonant and On-Resonant Quasi-PWM (Q_f-PWM/Q_n-PWM), have not been recognized so far. The names originate from the fact that Q-PWM converters can be regarded as PWM converters operating in both discontinuous modes simultaneously. The synthesis procedure can be generalized to encompass additional resonant elements. As an example, classes of Zero-Current and Zero-Voltage Multi-Resonant (ZC-MR/ZV-MR) converters are formally defined.

In contrast to square-wave switch waveforms in PWM converters, all QR topologies exhibit smooth quasi-sinusoidal waveforms and therefore reduced switching losses. Of particular interest are operating modes in which all switching transitions are at zero current or at zero voltage.

A study of operating modes and a DC analysis unified with respect to all PWM parents and all topological variations are carried out for four selected classes of QR Converters – Q_n-PWM, ZV, ZV-QSW, and ZV-MR. It is emphasized that for a QR converter, topology alone is not sufficient to derive DC conversion properties. Subject to different switch implementations and control timing, the emerging operating modes can result in vastly different behavior of the same converter topology.

Two switch implementations are considered – conventional, with one controllable switch and one diode, and the one that resembles the technique of synchronous rectification – with two controllable switches. In the first case, with the exception of converters in two Q-PWM classes, only variable-frequency control is applicable. However, if both switches are controllable, constant-frequency control is restored in all QR classes, and several novel operating modes of practical interest are uncovered.

Various QR classes and operating modes are compared with respect to sets of switching transitions, sensitivity to parasitic elements, available operating region, frequency range and stresses on switching devices. The role of free parameters in various design trade-offs is exposed, thus allowing a designer to select and realize the topology best suited for a particular application.

Contents

Acknowledgements iii

Abstract v

1 Introduction 1

2 DC-to-DC Power Conversion 5

2.1 Definition and Basic Properties of DC-to-DC Converters 5

2.2 Ideal Switched-Mode DC-to-DC Converters 7

2.3 An Overview of Switched-Mode DC-to-DC Converter Features 10

2.4 Approaches to Synthesis of Switched-Mode Converters 13

3 PWM DC-to-DC Converters 17

3.1 Definition of PWM Converters 18

3.2 Algebraic Representation of the Converter Topology 23

3.3 DC Conversion Ratio 25

3.4 Some General Properties of PWM Converters 29

3.5 Some General Properties of Two-Switch PWM Converters 32

3.6 A Unifying Analysis Method for Two-Switch DC-to-DC Converters . . . 34

4 Synthesis of PWM DC-to-DC Converters 37

4.1 Representation of the Converter Topology 38

4.2 Scope of the Synthesis Procedure 39

4.3 Synthesis of Second-Order PWM Converters 41

4.4 Synthesis of Fourth-Order PWM Converters 46

4.5 Results of the Synthesis Procedure 57

5 Extensions of PWM Converter Topologies **75**

5.1 Insertion of Isolation Transformers 75

5.2 Discontinuous Operating Modes 78

5.3 Converters with a Floating Load 86

5.4 Output Capacitor Transformation 87

6 Synthesis of Quasi-Resonant DC-to-DC Converters **89**

6.1 Quasi-Resonant Converters: Motivation and Basic Properties 90

6.2 Synthesis of Quasi-Resonant Converters with Two Resonant Elements . . 95

6.3 Synthesis of More Complex Quasi-Resonant Converters 98

6.4 Operating Modes of Quasi-Resonant Converters 100

6.5 DC analysis of QR converters 102

7 On-Resonant, Quasi-PWM Converters **105**

7.1 Operating States and Operating Modes 105

7.2 DC Analysis 109

7.3 Experimental Verification 113

8 Zero-Voltage Converters **119**

8.1 Operating States 119

8.2 Operating Modes 121

8.3 Variable-Frequency Control: DC Analysis 125

8.4 Constant-Frequency Control: DC Analysis 129

8.5 Experimental Verification 132

9 Zero-Voltage, Quasi-Square-Wave Converters **137**

9.1 Operating States 137

9.2 Operating Modes 139

9.3 Variable-Frequency Control: DC Analysis 142

9.4 Constant-Frequency Control: DC Analysis 145

9.5 Experimental Verification 151

10 Zero-Voltage, Multi-Resonant Converters **155**

10.1 Operating States 156

10.2 Operating Modes 158

10.3 Variable-Frequency Control: DC Analysis 163

10.4 Constant-Frequency Control: DC Analysis 170

10.5 Experimental Verification 179

11 A Comparison of Quasi-Resonant Converters **187**

11.1 Switching Losses 187

11.2 Operation Region, Frequency Range and Switch Stresses 189

12 Conclusions **207**

A 2L1C Converter Cells **211**

B DC Analyses of Quasi-Resonant Converters: Numerical Procedures **213**

B.1 On-Resonant, Quasi-PWM Converters 213

B.2 Zero-Voltage, Quasi-Square-Wave Converters 215

B.3 Zero-Voltage, Multi-Resonant Converters 217

References **221**

Chapter 1

Introduction

Power converters are systems that process electrical power from input, where the power source generates a certain current or voltage waveform and level, to output, where the waveform or level is changed in a controlled manner. Ideally, power is processed with 100% efficiency, that is, with no power loss in the converter itself. Depending on whether input and output waveforms are constant or time-varying, converters are classified as DC-to-DC, DC-to-AC, AC-to-DC and AC-to-AC. This thesis is focused on DC-to-DC switched-mode converters.

Power supply is a "dumb" but unfortunately indispensable part of every signal processing electronic system. It is not uncommon for it to take more space and weight and even to consume more power than all other "intelligent" parts of the system together. Hence, a continuous demand for smaller, lighter and more efficient power converters has motivated, in one way or another, much of the research and design efforts in the field of Power Electronics, including the work presented in this thesis.

Ever since the advent of fast semiconductor switches enabled practical realization of switched-mode converters, the number of applications for them has grown and the applications have diversified steadily. In particular, widespread applications of DC-to-DC converters include power supplies for a countless variety of electronic systems, systems for utilization of solar energy and DC motor drivers. Moreover, DC-to-DC converters are often found as basic building blocks for other types of power converters.

An increasing number of new applications has motivated a search for converters that could meet new requirements or outperform existing converters. Considered mainly an intuitive process, introduction of new converters has been rightfully accredited to designer's ingenuity. Since the understanding of power conversion principles has matured over the years, a different approach to the construction of power converters with certain

sets of properties has evolved. Thus, in [10], the problem of *synthesis* of complete classes of power converters is posed and solved analytically. Following the same approach, construction of a systematic synthesis procedure for generation of complete classes of PWM DC-to-DC converters is carried out in this thesis. The term "PWM" (pulse-width modulation) is used to denote "conventional" converters with approximately square-wave voltage and current waveforms.

In Chapter 2, basic principles of DC-to-DC switched-mode power conversion are reviewed. Emphasis is put on how various required or desirable features of power converters relate to the way that converter elements are interconnected or, as we shall say from now on, to the *converter topology*. Essential converter properties, such as complexity of the converter network, efficiency and steady-state and dynamic response are all related, sometimes exclusively, to the converter topology.

In Chapter 3, the family of PWM DC-to-DC converters is formally defined, and several general results are derived from defining assumptions. A connection is found between complexity of the converter network and a function (called *DC conversion ratio*) that relates output voltage or current level to input voltage or current level. As in [22], the DC model of a PWM converter is established and related to the converter topology. Based on this quite general framework, a completely formalized synthesis procedure is constructed in Chapter 4 and is executed via a simple computer program in order to generate complete sets of second-order and fourth-order PWM converters with up to four switches. Among astonishingly numerous converter topologies, many of which have not been recognized so far, converters with a specified set of properties are sorted out and compared. Several extensions of PWM converters, including discontinuous operating modes and insertion of the isolation transformer, are treated in Chapter 5 in a systematic and unified manner.

The incentive to increase the frequency at which switched-mode converters are operated is motivated by the fact that correspondingly smaller values and hence sizes and weights of energy storage components should result in smaller and lighter converters. However, the inevitable increase in switching power losses puts a practical upper bound on the usable frequency range. *Resonant* converter topologies overcome some of the

switching loss mechanisms attributed to PWM converters and offer the possibility of extending the usable frequency range toward higher frequencies. In contrast to sharp transitions in current and voltage waveforms of PWM converters, the resonant converters operate with smooth, quasi-sinusoidal, *resonant* waveforms leading to reduced losses ascribed to switching transitions. A common name *Quasi-Resonant* (QR) converters, adopted from [14], is used in this thesis for all converters constructed from a PWM converter by addition of resonant capacitors and inductors. Not long after the first class (named Zero-Current) of QR converters was introduced in [12], numerous variations appeared [13], followed by introduction of other classes (Zero-Voltage [14], Quasi-Square-Wave [17,18], Multi-Resonant [16]) with even more topological variations. In the course of proliferation of new converters, much-needed results toward understanding of fundamental topological properties and, even more importantly, toward unified analysis of seemingly countless and often confusing QR variations started to appear. Most notably, in [20], topological rules encompassing all topological variations are formulated for Zero-Voltage and Zero-Current classes, and the analysis is unified with respect to all variations and all underlying PWM converters.

In Chapter 6, synthesis of QR converters is based on the recognition that starting from a PWM topology with two switches, resonant elements can be placed in only two distinct positions with respect to the switches – in a cut-set with a switch or in a loop with a switch. Then, all possible combinations with a single resonant inductor and a single resonant capacitor are examined, giving rise to a total of six classes of QR converters. Two new classes are uncovered and a proper place is found for all other QR classes introduced before. It is possible to extend recursively the synthesis procedure to encompass QR topologies with more than two resonant elements.

The approach adopted in the synthesis of QR converters also allows application of a unified DC analysis of numerous QR topological variations that result from different PWM converters or variations in positions of resonant elements. Such analysis, which follows the method first proposed in [20], is completed in Chapters 7 through 10 for selected classes of QR converters. It is recognized that in addition to topology, a study of possibly non-unique *operating modes* is necessary in order to fully understand properties

and relative merits of QR converters. The study of Chapters 7 through 10 reveals a number of operating modes that have not been identified before or for which no analytic results have been obtained. In particular, it is demonstrated that in contrast to QR converters with conventional implementation of switches (a single transistor and a single diode), QR converters with two transistor switches can be operated and controlled at *constant switching frequency*. This is important since variable-frequency ripple and noise generated by variable-frequency converters are much more difficult to handle.

In Chapter 11 a comparison of QR converters is undertaken, aimed to provide a prospective designer with results necessary in order to successfully compare, select, and finally design the converter best suited for a given application.

Original results presented in this thesis are summarized in the concluding chapter.

Chapter 2

DC-to-DC Power Conversion

In this chapter, DC-to-DC converters and switched-mode converters in particular, are introduced along with the terminology used in subsequent chapters. DC-to-DC converters are inherently non-linear and/or time-varying electrical networks that process DC power at one voltage or current level to a different voltage or current level with, ideally, 100% efficiency.

Issues relevant for analysis, design and application of switched-mode converters are discussed briefly in Section 2.3 with emphasis on how they relate to the results of this thesis. The fact that all converter features are, often exclusively, a function of the way converter elements are interconnected, motivates the study on systematic synthesis of converter topologies. Most importantly, once complete classes of converter topologies are generated, it is possible to decide which particular topology is best suited for a given application.

Earlier approaches to the problem of synthesis of switched-mode converters are reviewed in Section 2.4.

2.1 Definition and Basic Properties of DC-to-DC Converters

Consider a two-port electrical network N consisting of lumped, two-terminal, possibly non-linear and/or time-varying resistors, capacitors and (possibly coupled) inductors. Resistors are defined as elements for which voltage v across it and current i through it satisfy

$$f(v,i,t) = 0\,, vi \geq 0\,, \forall t\,, \tag{2.1}$$

while standard definitions [31] are adopted for reactive elements (capacitors and inductors). Ports of the network are designated as input and output. The input port is

terminated by an ideal, DC, non-zero voltage or current source. The output port is terminated by a possibly non-linear and/or time-varying load resistor. Voltage and current at the input and at the output are denoted by v_g, i_g and v_{out}, i_{out}, respectively. Zero initial conditions are assumed for the network states. Define the average or DC value $\overline{y}$ of a function of time $y(t)$ by

$$\overline{y} \equiv \lim_{T\to\infty} \frac{1}{T} \int_0^T y(\tau)dt\,. \tag{2.2}$$

If $y(t)$ is periodic in time, $\overline{y}$ coincides with the average over one period. Then, voltage (M_v) and current (M_i) DC conversion ratios are defined by

$$M_v \equiv \frac{\overline{v}_{out}}{\overline{v}_g}, \tag{2.3}$$

$$M_i \equiv \frac{\overline{i}_{out}}{\overline{i}_g}. \tag{2.4}$$

The following definition of a DC-to-DC converter is taken from [1]:

Definition 2.1 *Network N together with source and load is a DC-to-DC converter iff*[1] $|M_v| > 1$ *or* $|M_i| > 1$.

Load of a DC-to-DC converter is not necessarily linear, time-invariant (LTI). In fact, it is usually both time-varying and non-linear. However, since in general the load characteristic is not predictable, we may postulate that the load is LTI and consider the effects of its time-variation and/or non-linearity separately.

The following proposition gives two basic necessary conditions that must be satisfied by the elements of a DC-to-DC converter [1]:

Proposition 2.1 *In a DC-to-DC converter with a linear, time-invariant load resistor R:*

1. *there is at least one non-linear and/or time-varying resistor* R_1 *for which* $\overline{v}_1\overline{i}_1 > 0$ *and at least one non-linear and/or time-varying resistor* R_2 *for which* $\overline{v}_2\overline{i}_2 < 0$;
2. *there is at least one reactance.*

The fact that DC-to-DC converters are inherently non-linear and/or time-varying electrical networks proved to be the major problem in developing comprehensive analysis and modeling methods.

[1] "iff" stands for "if and only if."

2.2 Ideal Switched-Mode DC-to-DC Converters

The major task of a power conversion system is to process power in a controlled manner with the least possible amount of power loss. Efficiency of power converters, defined as the ratio of output to input power, is analogous to distortion (conceived here in a very broad sense) in signal-processing systems. Ideal efficiency of 100% can be achieved only if all components of a converter are lossless. This is why in power converters the role of inevitable non-linear and/or time-varying resistors is devoted exclusively to switches. An ideal switch is a resistor for which the characteristic $f(v,i,t) = 0$ is defined by one and only one of the following two expressions:

$$v = 0\,, \qquad \text{for } t \text{ when the switch is in ON position}\,, \tag{2.5}$$

$$i = 0\,, \qquad \text{for } t \text{ when the switch is in OFF position}\,. \tag{2.6}$$

Ideal switches are lossless elements since instantaneous dissipated power is equal to zero for all t. A switch is *controllable* if transition from ON to OFF position and vice versa is subject to some external control signal. Now we can define ideal switched-mode DC-to-DC converters:

Definition 2.2 *An ideal switched-mode DC-to-DC converter is a DC-to-DC converter in which all resistors apart from the load are ideal switches.*

Henceforth, only switched-mode DC-to-DC converters will be considered. By Proposition 2.1, there are at least two switches and one reactance in any switched-mode DC-to-DC converter.

Suppose that there are n_s switches in a DC-to-DC converter. A vector whose elements assume values ON or OFF corresponding to positions of n_s ordered switches is denoted the *operating state* of the converter. There are at most 2^{n_s} operating states and for each state the converter network N reduces to the network N_i, which consists of source, load and reactances only. Change from state to state is called *state transition* and it is instantaneous by the assumption on ideal switches. State transition is *controllable* if at least one of the controllable switches changes its position in compliance to some external signal.

Switched-mode converters are operated such that a sequence of operating states is repeated periodically. Time interval T_p, which elapses between successive repetitions of operating states, is called the *switching period.* Valid operation of a converter is defined as follows:

Definition 2.3 *For a switched-mode DC-to-DC converter, a periodic sequence of operating states is called an operating mode if:*

1. *every switch changes its position at least once during a switching period;*
2. *at least one of the state transitions is controllable;*
3. *for the vector of converter state variables, there exists a periodic solution with a period equal to the switching period.*

By Assumption 1, all switches are necessary for proper operation of a switched-mode converter. The second assumption makes sure that external control over the converter is possible. For some examples of DC-to-DC converters there exist steady-state solutions with a period that is an arbitrary integer multiple of T_p. Each solution may lead to different DC conversion and dynamic properties of the converter [25]. Assumption 3 is introduced in order to focus only on the solutions of most practical interest.

2.2.1 Control Strategies for Switched-Mode DC-to-DC Converters

In switched-mode DC-to-DC converters, control over DC conversion ratio M_v or M_i can be accomplished only through control over state transitions. Suppose that a converter operates in a mode with j_o state transitions out of which j_c are controllable. Only the intervals between two controllable transitions can be varied by external command. In general, any number from one to j_c intervals can be subject to external control while others are kept constant, thus giving rise to various control strategies.

If $j_c = 1$, there is only one possible control strategy in which the control over the conversion ratio is achieved by varying the switching frequency $f_s = 1/T_p$.

If $j_c = 2$, four control strategies are possible, in general. If time between two controllable transitions is denoted by T_c, possible control strategies are:

1. constant-frequency, duty-ratio control, $T_p = const.$;

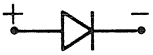
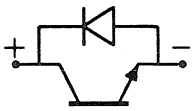
switch implementation	constraints
transistor 	$v \geq 0$ $i \geq 0$
diode 	$v \leq 0$ $i \geq 0$
current bidirectional 	$v \geq 0$
voltage bidirectional 	$i \geq 0$

Table 2.1: Switch implementation

2. variable-frequency, constant-pulse-width control, $T_c = const.$;

3. variable-frequency, constant-pause control, $T_p - T_c = const.$;

4. variable-frequency, variable-pulse-width control.

Duty ratio D in the constant-frequency control is defined by

$$D \equiv T_c/T_p\,. \tag{2.7}$$

The constant-frequency control is usually preferred over the variable-frequency control since filtering components can be optimized to suppress current and voltage ripples at switching frequency and its harmonics. Also, noise generated by variable-frequency converters is more difficult to handle, and in some applications it cannot be tolerated.

2.2.2 Switch Implementation

Characteristics of ideal switches coincide with axes in the v–i plane. In practice, parts of the characteristics are implemented by semiconductor devices – transistors and diodes, as indicated in Table 2.1. It should be noted that MOS transistors, which alternate bipolars as controllable switches, are inherently current-bidirectional.

Implementation of a four-quadrant switch requires two current-bidirectional switches in series or two voltage-bidirectional switches in parallel. Unless otherwise noted, it will

be assumed that except for constraints in Table 2.1, switch implementations are ideal (lossless and allow instantaneous switching).

2.3 An Overview of Switched-Mode DC-to-DC Converter Features

In this section a brief overview of essential features of switching converters is presented. The overview is arranged as a glossary of pertinent issues with the intention of emphasizing what problems related to analysis, modeling, design and application of DC-to-DC power converters are tackled in this thesis.

Converter topology describes how source, load, reactive elements and switches are interconnected in a converter network. In particular, if the converter network N consists of single-port elements only, converter topology is a synonym for the corresponding graph G with edges labeled after the elements of the network. All converter properties and features are, often exclusively, related to converter topology. Hence, ability to construct systematically all possible topologies is necessary in order to meet design requirements or to select topology best suited for a given application. Synthesis of the two largest families of switched-mode converter topologies, namely, PWM and Quasi-Resonant, is undertaken in this thesis.

DC conversion ratio is an essential property of DC-to-DC converters. Assuming that a converter operates in a specified mode, DC characteristics of the converter are in the form $F(M, \tau_c, R) = 0$, where M is the DC conversion ratio and τ_c is the vector of controllable intervals. Function F depends on the converter topology *and* the particular operating mode. The operating mode may not be unique for the topology. Thus, a PWM converter operates in the continuous conduction mode assumed by Definition 3.1 of Chapter 3, but only if circuit parameters satisfy certain conditions. Otherwise, operation in other modes, called discontinuous modes, is possible, as discussed in Chapter 5. Furthermore, in Chapters 7 through 10, it is shown that in addition to topology, a study of possible operating modes is necessary in order to understand DC conversion properties of Quasi-Resonant converters.

Efficiency is a figure of merit for power converters. Of course, it depends on how close converter elements are to ideal. However, assuming that the same elements are

always available, efficiency depends on the converter topology as effectively exposed in the comparison of PWM converters generated by the synthesis procedure of Chapter 4. Also, the essential motivation behind the development of Quasi-Resonant converters is to reduce or eliminate some of the switching losses inherent in the PWM topologies. Hence, in Chapters 7 through 11, where selected classes of QR converters are studied, particular attention is given to the operating modes for which switching losses are minimized.

Switch voltage stress and current stress are the parameters that decide the choice of semiconductor devices used to implement the switches. It is shown (Section 3.5) that voltage and current stresses are identical for all two-switch PWM converters that share the same DC conversion ratio. However, for other PWM and Quasi-Resonant converters, topologies are subject to comparison with respect to switch stresses.

For lower losses on parasitic resistances, more efficient filtering and lower generated noise, it is preferred that *input and output terminal waveforms* be continuous (ideally, DC only). This feature depends solely on the converter topology, and it appears as one of the parameters for comparison of PWM converters generated by the synthesis procedure of Chapter 4. A relation between the feature of continuous terminal currents and attainable conversion ratios for PWM converters is found in Section 3.4.

Coupling of inductors on a single magnetic core is possible if all inductors share identical or proportional voltage waveforms [29]. The coupled-inductor technique yields sizable savings in size and weight of converter magnetics. Moreover, because of the ripple stirring phenomena, beneficial filtering effects can be obtained [29,30]. Again, the possibility of integrating magnetic elements is a property of the converter topology alone, and it is pointed out in comparison tables of Chapter 4. A relation between this feature and attainable conversion ratios is found in Section 3.4.

DC isolation is an ubiquitous requirement in all off-line power supplies. It can be provided if the power supply includes a switched-mode converter with an isolation transformer. The problem of inserting an isolation transformer is treated in Section 5.1 as one of the extensions of PWM converter topologies.

Complexity of a converter is measured by the number of reactive components, switches and controllable switches in particular. Evidently, it is a function of the converter topol-

ogy alone. The trade-off between increased complexity and required or preferred features is behind many of the results in the thesis. Most notably, for PWM converters, a result that gives the minimum possible complexity for a specified DC conversion ratio is found in Section 3.4. Also, for Quasi-Resonant converters it is demonstrated how constant-frequency control can be implemented at the expense of an increased number of controllable switches.

Dynamic response of DC-to-DC converters is a response of input/output and state variables to time variations of the source voltage or current, load, and/or lengths of controllable intervals. It is relevant for the design of the control loop for regulation of the output voltage (or current). In general, dynamic response is a function of the converter topology, operating mode, control strategy and the algorithm that assigns lengths of controllable intervals. Assuming that the operating mode of a converter is known, the small-signal dynamic response in the vicinity of a steady-state solution has been solved for PWM converters [22] and (exactly) for ideal switched-mode converters in general [25]. Except for a study of possible operating modes and steady-state solutions, which are necessary prerequisites, dynamic response and control problems are outside the scope of this thesis.

Switching noise, radiated (EMI) and conducted, is generated by a switched-mode converter because of the switching action inside the converter power stage. Minimization of generated noise is an important system consideration. The issue is not addressed directly in this thesis. However, the feature of continuous terminal waveforms and the shape of current/voltage waveforms inside a converter, which are discussed in the thesis, affect the amount of generated noise. In particular, it can be debated whether or not smooth, quasi-sinusidal waveforms in Quasi-Resonant converters contribute to lower level of radiated noise.

Size, weight and cost considerations, which are evidently correlated to all of the above issues, are not directly addressed in this thesis.

2.4 Approaches to Synthesis of Switched-Mode Converters

2.4.1 PWM Converters

For more than a decade now, applications for switching converters have diversified and their number has increased rapidly. This trend was accompanied by the search for new converter topologies with properties to match the new application requirements or to outperform the existing topologies. Along the way, approaches to synthesis of switched-mode converters evolved steadily.

Elementary single inductor PWM converters – buck, boost and buck-boost – emerged from intuitive understanding of switched-mode conversion principles. Introduction of some other converter circuits such as the Watkins-Johnson converter [3] and the Sepic converter [4] could also be ascribed to the intuitive approach.

In a search for new converter topologies, elementary converters were subject to various circuit manipulations. Thus, for example, a cascade of a boost and a buck converter led to discovery of the Ćuk converter [5]. Other circuit manipulation techniques included inversion of source and load, duality transformation [23] or differential connection of the load across the outputs of two converters [6].

The concept of a converter cell defined as a converter less source and load was introduced in [8]. Assuming that one of the input and one of the output terminals are connected, the converter cell is a three-terminal network. The ports can be terminated by the source and the load in six possible ways, thus generating up to six converter topologies. In [9], this approach was applied to a large number of converter cells extracted from the existing converter topologies. The concept of the converter cell is useful for compact classification of converter topologies but does not provide a means of constructing original converter networks.

A completely different approach was devised in [10]. The main idea was to find an algebraic representation for the converter topology so that synthesis of complete classes of converters can be reduced to synthesis of all possible algebraic representations. Since entries in matrix representations of a network topology are -1, 0 and 1, generation of *all* possible topologies with a given complexity is a well-defined problem. The importance of this approach is that the synthesis of converters is formulated and solved analytically

rather than intuitively or by various circuit manipulations. However, the choice for algebraic representation in [10] was not quite adequate, so that generated classes of converters were later found incomplete [9]. A major deficiency of the synthesis procedure in [10] is that switches are not taken into account rigorously. Nevertheless, the approach for synthesis of PWM converters undertaken in Chapter 4 is based on the same idea of synthesis of matrix representations, and it can be considered as a refinement and extension of the work in [10].

2.4.2 Quasi-Resonant Converters

The class of Zero-Current, Quasi-Resonant converters was introduced by suggesting a way to insert resonant components around the switches in a PWM converter [12]. The introduction and further developments of Quasi-Resonant converters were motivated by the fact that switching losses in a PWM converter can be reduced if switch voltage and current waveforms are shaped appropriately.

After the introduction of the first class of QR converters, it was immediately recognized that there are many possible ways to insert the resonant components and that operating modes depend on switch implementation [13]. Consequently, topological rules that govern all possible positions of resonant elements in a Zero-Current converter are formulated in [15]. Later on, modifications that led to classes of Zero-Voltage and Multi-Resonant converters were introduced in [14] and [16], respectively. Concurrently, a circuit manipulation technique is devised in [17] to generate various Quasi-Resonant modifications of two-switch PWM topologies.

In [20], redundancies are removed from topological rules for generation of Zero-Current and Zero-Voltage converters. Furthermore, by introduction of a unifying analysis approach, it is shown that numerous possible positions of resonant elements added to a two-switch PWM topology result in converters that share identical DC conversion properties. The conversion and dynamic properties of Quasi-Resonant converters are related to well-known DC conversion properties of the parent PWM topology.

In this thesis, a synthesis method for Quasi-Resonant converters is founded on two basic concepts – first, that a Quasi-Resonant converter is a modification of a PWM topol-

ogy, and second, that modification of the PWM topology can be formalized by means of topological rules. Based on these two ideas, the synthesis method and consequently analyses of selected Quasi-Resonant classes are presented in Chapters 6 through 11.

Chapter 3

PWM DC-to-DC Converters

The main purpose of this chapter is to set up a framework for construction of a systematic synthesis procedure in Chapter 4.

The family of PWM DC-to-DC converters is formally defined in Section 3.1, and an algebraic representation of the complete PWM converter topology is constructed in Section 3.2.

Under the small-ripple assumption, a general DC model of PWM converters follows from the *state-space averaging* analysis method [21,22]. Furthermore, in [10], it is demonstrated that the DC model can be explicitly linked to the converter topology. In Section 3.3, it is shown how these known results follow from defining assumptions imposed on PWM converters.

Original results of this chapter are lumped in Propositions 3.1 through 3.9 in which some general topological properties of PWM converters are established. The properties involve complexity of the converter network, attainable DC conversion ratios and features such as continuous terminal currents and possible coupling of magnetic elements. Relevant practical implications of these results are indicated. In particular, in Section 3.6, it is shown that a unifying analysis method, originally devised in [20] for two classes of Quasi-Resonant converters, can be generalized and applied to all classes of switched-mode converters in which converter's DC network is the same as DC network of a two-switch PWM converter.

Elementary graph theoretic terms and results used in this chapter and in subsequent chapters are with reference to [24] or [31].

3.1 Definition of PWM Converters

The family of PWM DC-to-DC converters is formally defined in this section. Defining assumptions, regarding allowed elements and their interconnections in the converter network, are motivated by the objectives of achieving a certain DC conversion ratio with the ideal efficiency of 100% and the least possible number of elements.

Definition 3.1 *An ideal PWM DC-to-DC converter is a network N for which Assumptions A1 through A5 are satisfied:*

A1: N consists of only the following elements:

1. A single DC voltage source, V_g, or a single DC current source, I_g.
2. A single LTI load resistor R.
3. A set of LTI inductors, $\mathcal{L} = \{L_i,\ i = 1, \ldots, n_l\}$.
4. A set of LTI capacitors, $\mathcal{C} = \{C_i,\ i = 1, \ldots, n_c\}$, $n_c + n_l \geq 1$.
5. A set of switches, $\mathcal{S} = \{S_i,\ i = 1, \ldots, n_s\}$, $n_s \geq 1$, such that

$$S_i \in \mathcal{S} \Leftrightarrow S_i \text{ is } \begin{cases} \text{ON} & \text{if } kT_p \leq t < kT_p + DT_p \\ \text{OFF} & \text{otherwise,} \end{cases} \tag{3.1}$$

   where $T_p = const.$, $0 < D < 1$ and k is any integer.

6. A set of switches, $\hat{\mathcal{S}} = \{\hat{S}_i,\ i = 1, \ldots, \hat{n}_s\}$, $\hat{n}_s \geq 1$, which are ON iff the switches in $\mathcal{S}$ are OFF.

A2: The load R forms a loop with a subset of elements in $\mathcal{C} \cup \{V_g\}$ or a cut-set with a subset of elements in $\mathcal{L} \cup \{I_g\}$.

A3: Let N_1 (N_2) denote the network to which N reduces when switches in $\mathcal{S}$ ($\hat{\mathcal{S}}$) are ON. Let G, G_1, G_2 be the graphs corresponding to the networks N, N_1, N_2, respectively. Then, in G_i, $i = 1, 2$, and therefore in G, there are no loops consisting only of elements in $\mathcal{C} \cup \{V_g\}$ nor cut-sets consisting only of elements in $\mathcal{L} \cup \{I_g\}$.

A4: G is a non-separable graph.

A5: In G, there are neither loops nor cut-sets that consist only of switches in $\mathcal{S}$ or only of switches in $\hat{\mathcal{S}}$.

To achieve the ideal efficiency of 100%, only lossless elements are allowed in the converter network by Assumption A1. Source and load are connected through a combination of switches, capacitors and inductors. Three types of lossless magnetic elements commonly used in practical converter circuits are excluded by Definition 3.1: coupled inductors, switched coupled inductors and transformers. The restriction is introduced to allow for simple systematic and general treatment of PWM converters. The loss of generality is circumvented by including coupled inductors and transformers as extensions of ideal PWM topologies. As discussed in Chapter 4, in order to reduce the number of switches, a single inductor and four switches can be replaced by a pair of switched coupled inductors and two switches. Insertion of isolation transformers is discussed in Chapter 5.

Since only single-port, lumped elements are allowed by Assumption A1, the correspondence between the converter network N and its graph G is trivial. Assuming that edges in the graph G are labeled after the elements they represent, the graph G contains all information about the converter topology.

Assumptions on the operation of switches describe PWM converters as networks with periodically varying structure. The scope is limited to converters with *two* linear time-invariant structures switched at constant frequency. Pulse-width modulation (PWM) is used to vary the duty ratio D in order to control the DC conversion ratio. The unique operating mode of an ideal PWM converter is described by the periodic sequence of states

$$\text{PWM operating mode: } \cdots \rightarrow \boxed{\text{ON-OFF}} \rightarrow \boxed{\text{OFF-ON}} \rightarrow \cdots , \tag{3.2}$$

where the first label (ON or OFF) corresponds to the position of switches in $\mathcal{S}$, while the second label denotes the position of switches in $\hat{\mathcal{S}}$.

Output voltage (or current) of a DC-to-DC converter must be essentially DC with a small AC ripple. This is ensured by Assumption A2.

Assumption A3 imposes restrictions on the topology of repeatedly switched networks N_1 and N_2. Suppose that there is a capacitor-only loop in G. Then, one of the ca-

		load R	
		in a loop with capacitors	in a cut-set with inductors
input source	V_g	voltage to voltage	voltage to current
	I_g	current to voltage	current to current

Table 3.1: Four types of PWM DC-to-DC converters.

pacitors in the loop can be removed and the values of the remaining capacitors can be adjusted so that operation of the circuit is completely unaltered. Therefore, in this case, Assumption A3 is well justified. However, A3 is more restrictive – capacitor-only loops are excluded from both G_1 and G_2. There are capacitor-only DC-to-DC converters in which capacitor-only loops in N_1 and N_2 are repeatedly switched. These converters have practical applications as voltage multipliers or dividers, but they are beyond our interest here because the conversion ratio cannot be controlled by varying the duty ratio D [1]. It is interesting to note that in some cases a capacitive voltage divider can be judiciously embedded in a PWM converter, as demonstrated in [11].

Assumptions A4 and A5 are necessary conditions for a converter to be realized with a minimum number of elements. Assumption A4 requires that all parts of the converter network be electrically connected. If G is separable, only the non-separable subgraph of G that contains both V_g and R takes part in power conversion.

To justify Assumption A5, suppose that there exists a cut-set in G consisting only of switches in $\mathcal{S}$. At least one of the switches is superfluous since no current can flow through a switch in the ON position if all other switches in the cut-set are OFF. Therefore, one switch can be replaced by a short without affecting operation of the circuit. Similarly, a switch can be removed if it forms a loop with other switches that belong to the same set. From Assumption A5 it follows that G_1 and G_2 must be connected (possibly separable) graphs.

3.1.1 Types of PWM Converters

Definition 3.1 allows for four types of DC-to-DC conversion as indicated in Table 3.1. In practical applications, ideal current source I_g can be emulated by a voltage source

node $\longleftrightarrow$ mesh
cut-set $\longleftrightarrow$ loop
tree branch $\longleftrightarrow$ link

Table 3.2: Dual graph-theoretic terms.

voltage $\longleftrightarrow$ current
charge $\longleftrightarrow$ flux

Table 3.3: Dual electrical variables.

in series with an inductor. This transformation effectively converts a current-input converter into a voltage-input converter. Similarly, voltage input can be converted to current input by replacing the voltage source with a capacitor and a current source in parallel. Current output can be converted to voltage output by placing a capacitor across the load and conversely, voltage output can be converted to current output by placing an inductor in series with the load. Having these straightforward transformations in mind, it is sufficient to consider only one type of PWM converter without loss of generality. Unless otherwise noted, we shall consider only voltage-to-voltage PWM converters, since they are most commonly found in practice.

3.1.2 Duality Relation for PWM DC-to-DC Converters

In graph theory, duality is a symmetrical relation between connected (possibly oriented) planar graphs. The definition of duality relation and the procedure for construction of dual graphs and networks are adopted from [31]. Dual graph-theoretical terms are summarized in Table 3.2. The duality relation holds for electrical networks with singled-port elements and with planar graphs. It includes the correspondence between electrical variables as shown in Table 3.3. Let σ be a statement concerning the behavior of an electrical network N for which the dual network N' exists. Let σ' be the statement obtained from σ by replacing every term or quantity by its dual. Importance of the duality relation for electrical networks stems from the *duality principle* [31],

$$\sigma \text{ (for } N) \Leftrightarrow \sigma' \text{ (for } N') \ . \tag{3.3}$$

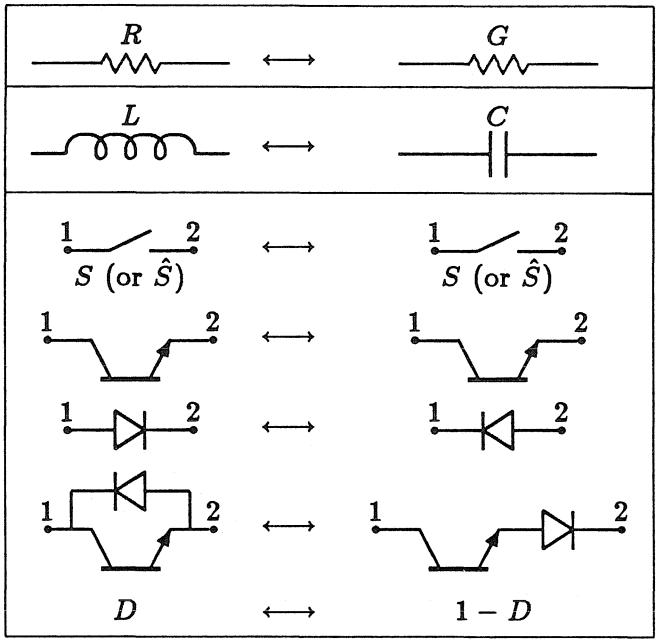


Table 3.4: Dual elements in PWM converters.

PWM DC-to-DC converters as defined in Section 3.1 are electrical networks consisting of only single-port elements. Assuming that the corresponding graph is planar, duality relations and duality principle are applicable. For elements allowed in PWM converters, duality relations are shown in Table 3.4. Switch is the only element not found in LTI networks. An ideal switch is a four-quadrant device with characteristics that coincide with axes in the $v - i$ plane. A dual device has the same characteristics but with i and v axes interchanged. Therefore, a switch is dual to itself. However, as short and open are dual, switches in S and $\hat{S}$ are dual if the control variable D is kept unchanged, or, as indicated in Table 3.4, switches in S ($\hat{S}$) are dual to themselves but with $D' \equiv 1 - D$ dual to D. By interchanging i and v axes in their characteristics, dual switch implementations in Table 3.4 are easily found. Networks dual to PWM converters are defined by the dual of Definition 3.1. It is easy to verify that the dual of a PWM converter is again a PWM converter. Voltage input (output) is dual to current input (output). Hence, the dual of a voltage-to-voltage converter with a DC conversion ratio $M_v(D) \equiv V_{out}/V_g$ is a current-to-current converter with $M_i'(D) \equiv I_{out}'/I_g'$.

3.2 Algebraic Representation of the Converter Topology

PWM voltage-to-voltage converter topology is identified with the graph G in which each edge is labeled after the corresponding element (V_g, R, C, L, S or $\hat{S}$). The following property follows directly from the defining assumptions:

Proposition 3.1 *In a voltage-to-voltage PWM converter:*

1. *Elements of* $\mathcal{T} = \{V_g\} \cup \mathcal{C}$ *constitute a tree for* G_i, $i = 1, 2$.
2. *Elements of* $\mathcal{T}_s = \{V_g\} \cup \mathcal{C} \cup \mathcal{S}$ *(or* $\hat{\mathcal{T}}_s = \{V_g\} \cup \mathcal{C} \cup \hat{\mathcal{S}}$*) constitute a tree for* G.

Proof: loops containing only capacitors and possibly V_g are not allowed by Assumption A3. Suppose that subgraph $\mathcal{T}$ of G_i is not connected or that there is a node in G_i which is not in $\mathcal{T}$. Since G_i is connected and since R is in a loop with elements of $\mathcal{T}$, there must be a cut-set that consists only of inductors. This is not possible by Assumption A3. Hence, $\mathcal{T} = \{V_g\} \cup \mathcal{C}$ is a tree for G_i, $i = 1, 2$. There cannot be a loop that consists only of elements in $\mathcal{T}_s$, since Assumption A3 would be violated when switches in $\mathcal{S}$ are ON. Also, there cannot be a cut-set consisting only of elements in $\mathcal{L} \cup \hat{\mathcal{S}}$. It follows that $\mathcal{T}_s$ is connected and that it contains all nodes of G. Hence, it is a tree for G. The proof for $\hat{\mathcal{T}}_s$ is completely analogous. $\lhd$

If $\mathcal{T}_s$ is chosen for the tree of G, the fundamental loop matrix $\mathbf{F_n}$ for G has the following form:

$$\mathbf{F}_n^{(1+n_l+\hat{n}_s)\times(1+n_c+n_s)} = \left[\begin{array}{c|c} \mathbf{F}_{n1} & \mathbf{F}_s \\ \hline \mathbf{F}_{\hat{s}} & \mathbf{F}_{\hat{s}s} \end{array}\right]. \tag{3.4}$$

Columns of $\mathbf{F}_n$ correspond to the elements of the tree, ordered as $\{V_g\}$, $\mathcal{C}$, $\mathcal{S}$, while rows correspond to the remaining elements, ordered as $\{R\}$, $\mathcal{L}$, $\hat{\mathcal{S}}$. The matrix is partitioned such that $\mathbf{F}_{n1}$ is the fundamental loop matrix for the graph G_1 representing the converter network when the switches in $\mathcal{S}$ are ON, provided that the tree $\mathcal{T} = \{V_g\} \cup \mathcal{C}$ is chosen for G_1.

Now we are in position to show that in a PWM converter, the number of switches in $\mathcal{S}$ must be equal to the number of switches in $\hat{\mathcal{S}}$.

Proposition 3.2 *In a PWM converter,* $\hat{n}_s = n_s$.

Proof: by Proposition 3.1, in a voltage-to-voltage PWM converter, voltage across any switch $S \in \mathcal{S}$ is a linear combination of voltages across the elements of $\hat{\mathcal{T}}_s$. Moreover, any linear combination of voltages across switches in $\mathcal{S}$ is a linear combination of voltages across the elements of $\hat{\mathcal{T}}_s$. Such a linear combination must include at least one $\hat{S}$-switch voltage since otherwise there would be a loop consisting only of elements in $\mathcal{S}$ (which is not possible by Assumption A5) or only of elements in $\mathcal{T}_s$ (which is not possible by Proposition 3.1). Hence, rows of the matrix $\mathbf{F}_{\hat{s}s}$ must be linearly independent. By a dual argument, columns of $\mathbf{F}_{\hat{s}s}$ must be linearly independent. Therefore, n_s is necessarily equal to $\hat{n}_s$ and, moreover, $\mathbf{F}_{\hat{s}s}$ must be a non-singular matrix. In a voltage-to-current PWM converter, it is easy to verify that $\{R\} \cup \hat{\mathcal{T}}_s$ is a tree and since there cannot be a loop consisting only of elements in $\{R\} \cup \mathcal{S}$, Proposition 3.2 follows again. By the duality principle, Proposition 3.2 holds for all types of PWM DC-to-DC converters. $\lhd$

Matrix entries in Eq. (3.4) can be further partitioned such that matrices representing interconnections among elements in different sets are defined:

$$\mathbf{F}_{n1}^{(1+n_l)\times(1+n_c)} = \left[\begin{array}{c|c} f_{rg} & \mathbf{f}_{rc}^T \\ \hline \mathbf{f}_{g1} & \mathbf{F}_1 \end{array}\right], \tag{3.5}$$

$$\mathbf{F}_s^{(1+n_l)\times n_s} = \left[\begin{array}{c} \mathbf{0} \\ \hline \mathbf{F}_{ls} \end{array}\right], \tag{3.6}$$

$$\mathbf{F}_{\hat{s}}^{n_s\times(1+n_c)} = \left[\begin{array}{c|c} \mathbf{f}_{\hat{s}g} & \mathbf{F}_{\hat{s}c} \end{array}\right]. \tag{3.7}$$

The fundamental loop matrix $\mathbf{F}_{n2}$ for the graph G_2, corresponding to the converter network when the switches in $\mathcal{S}$ are OFF, can be partitioned in the same manner as $\mathbf{F}_{n1}$. The first row, which corresponds to load R, is the same in $\mathbf{F}_{n1}$ and $\mathbf{F}_{n2}$. This is a consequence of Assumption A2. Relations,

$$\mathbf{f}_{g2} = \mathbf{f}_{g1} - \mathbf{F}_{ls}\mathbf{F}_{\hat{s}s}^{-1}\mathbf{f}_{\hat{s}g}, \tag{3.8}$$

$$\mathbf{F}_2 = \mathbf{F}_1 - \mathbf{F}_{ls}\mathbf{F}_{\hat{s}s}^{-1}\mathbf{F}_{\hat{s}c}, \tag{3.9}$$

can be found from Eqs. (3.4) through (3.7).

3.3 DC Conversion Ratio

DC conversion ratio M is an essential property of DC-to-DC converters. The aim of this section is to show that general DC model [22] and its link to algebraic representation of the converter topology [10] hold for PWM converters formally defined in Section 3.1.

If inductor currents ($\mathbf{i}_l$) and capacitor voltages ($\mathbf{v}_c$) are chosen for the state variables of the converter, the following state-space description is obtained:

$$\dot{\mathbf{x}}(t) = \mathbf{A}(t)\mathbf{x}(t) + \mathbf{b}(t)V_g\,, \tag{3.10}$$

$$v_{out}(t) = \mathbf{c}^T\mathbf{x}(t) + dV_g\,, \tag{3.11}$$

where

$$(\mathbf{A}(t)\,,\ \mathbf{b}(t)) = \begin{cases} (\mathbf{A}_1\,,\ \mathbf{b}_1) & \text{if } kT_p \le t < kT_p + DT_p\,, \\ (\mathbf{A}_2\,,\ \mathbf{b}_2) & \text{otherwise}\,. \end{cases} \tag{3.12}$$

The state-space parameter matrices and vectors can be expressed in terms of components of the fundamental loop matrices [32],

$$\mathbf{A}_i = \mathbf{P}^{-1}\left[\begin{array}{c|c} \mathbf{0} & \mathbf{F}_i \\ \hline -\mathbf{F}_i^T & -\mathbf{G} \end{array}\right], \tag{3.13}$$

$$\mathbf{b}_i = \mathbf{P}^{-1}\left[\begin{array}{c} \mathbf{f}_{gi} \\ \hline -\mathbf{g} \end{array}\right], \tag{3.14}$$

$$\mathbf{c}^T = \left[\begin{array}{c|c} \mathbf{0} & \mathbf{f}_{rc}^T \end{array}\right], \tag{3.15}$$

$$d = f_{rg}\,, \tag{3.16}$$

where

$$\mathbf{x}(t) = \begin{bmatrix} \mathbf{i}_l(t) \\ \mathbf{v}_c(t) \end{bmatrix},\ \mathbf{P} = diag(L_1,\ldots,L_{n_l},C_1,\ldots,C_{n_c}),\ \mathbf{G} = \frac{1}{R}\begin{bmatrix} \left.\begin{matrix} \mathbf{f}_{rc}^T \\ \vdots \\ \mathbf{f}_{rc}^T \end{matrix}\right\} j \\ \mathbf{0} \\ \vdots \\ \mathbf{0} \end{bmatrix} \tag{3.17}$$

and,

$$\mathbf{g}^T = \left[\underbrace{f_{rg} \cdots f_{rg}}_{j} \; 0 \cdots 0 \right] . \tag{3.18}$$

It is assumed, without loss of generality, that first j capacitors are in a loop with load R.

Since $\mathbf{A}(t)$, $\mathbf{b}(t)$ in Eq. (3.10) are piecewise continuous in time, the state-space equations have a unique solution for all finite t [33]. Moreover, since the switching of two linear, time-invariant networks is periodic, it is possible to describe a PWM converter as a sampled-data system that is linear and time-invariant for $D = const.$ Denote $\mathbf{x}(kT_p) \equiv \mathbf{x}(k)$. Then,

$$\mathbf{x}(k+1) = \Phi(D)\mathbf{x}(k) + \phi(D)\, V_g \,, \tag{3.19}$$

where

$$\Phi(D) = e^{\mathbf{A}_2(1-D)T_p} e^{\mathbf{A}_1 D T_p} \,, \tag{3.20}$$

$$\phi(D) = e^{\mathbf{A}_2(1-D)T_p} \left[e^{\mathbf{A}_1 D T_p} \int_0^{DT_p} e^{-\mathbf{A}_1 \tau} \mathbf{b}_1 d\tau + \int_0^{(1-D)T_p} e^{-\mathbf{A}_2 \tau} \mathbf{b}_2 d\tau \right] . \tag{3.21}$$

For any bounded input V_g, the system described by Eq. (3.19) will have a unique, bounded steady-state solution if the homogeneous part is asymptotically stable, or if

$$\det(z_p \mathbf{I} - \Phi(D)) = 0 \;\Rightarrow\; |z_p| < 1 \,. \tag{3.22}$$

Since networks N_1 and N_2 consist of passive elements, the poles, $\{z_p\}$, cannot be outside the unit circle. Moreover, practical PWM converters must have a unique, bounded steady-state solution since all reactances are strictly passive. However, if an ideal PWM converter has a pole $z_p = 1$, a non-zero DC input V_g may cause unbounded response of the system described by Eq. (3.19). Response of the practical circuit would depend on parasitic lossy elements, resulting in unacceptable power loss. A sufficient condition for existence of a unique, bounded steady-state solution is that

$$\det(\mathbf{I} - \Phi(D)) \neq 0 \,. \tag{3.23}$$

The steady-state solution,

$$V_{out}(kT_p) \equiv v_{out}(kT_p)|_{k\to\infty} = \left[\mathbf{c}^T (\mathbf{I} - \Phi(D))^{-1} \phi(D) + d \right] V_g \,, \tag{3.24}$$

is found by taking $\mathbf{x}(k+1) = \mathbf{x}(k)$. Finally, general expression for the DC conversion ratio of a voltage-to-voltage PWM converter can be found by averaging the output voltage over a single period T_p,

$$M(D) = \frac{V_{out}}{V_g} = \frac{\frac{1}{T_p}\int_0^{T_p} v_{out}(t)dt}{V_g}, \text{ with } v_{out}(0) = V_{out}(kT_p). \tag{3.25}$$

Here, $v_{out}(t)$ is easily found as the solution to Eqs. (3.10) and (3.11) with known initial conditions.

3.3.1 Small-Ripple Assumption

One of the important practical requirements for all DC-to-DC converters is that output voltage is essentially DC with a relatively small AC ripple. The exact amount of allowed voltage ripple depends on the particular application. For example, the ripple defined as ratio of peak-to-peak to DC value of the output voltage should be typically 1% or less in standard $5V$-output power supplies of digital electronic systems. Thus, in order to sufficiently attenuate the AC ripple that results from the switching action, low-pass filtering must be inherent in any switched-mode converter. As a result of the filtering, voltages across the capacitors in the loop with load R are essentially DC. Voltage ripples across other capacitors and current ripples in inductor currents are not necessarily small. However, since larger ripples imply higher losses on parasitic elements and higher voltage and current stresses on switching devices, it is not unusual that all AC ripples are relatively small in practical designs. The small ripple is a result of the fact that natural frequencies associated with the switched linear networks N_1 and N_2 are much lower than the switching frequency, $f_s \equiv 1/T_p$.

For the purpose of systematic generation and comparison of converter topologies, the *small-ripple assumption* – the assumption that T_p can be made arbitrarily small – can be postulated even without any further justification. The analysis and derivation of general topological properties is greatly simplified without any loss of generality. Converters in which the small-ripple assumption is *purposely* abandoned are treated in Section 5.2 as extensions of PWM topologies.

3.3.2 DC Conversion Ratio for $T_p \to 0$

In the limit $T_p \to 0$, the matrix $e^{\mathbf{A}T_p} \to \mathbf{I} + \mathbf{A}T_p$ and DC model,

$$\mathbf{0} = \left[\begin{array}{c|c} \mathbf{0} & \mathbf{F} \\ \hline -\mathbf{F}^T & -\mathbf{G} \end{array}\right] \left[\begin{array}{c} \mathbf{I}_L \\ \hline \mathbf{V}_C \end{array}\right] + \left[\begin{array}{c} \mathbf{f}_g \\ \hline -\mathbf{g} \end{array}\right] V_g \,, \tag{3.26}$$

$$V_{out} = \mathbf{f}_{rc}^T \mathbf{V}_C + f_{rg} V_g \,, \tag{3.27}$$

is obtained, where

$$\mathbf{F} \equiv D\mathbf{F}_1 + (1-D)\mathbf{F}_2 \,, \tag{3.28}$$

$$\mathbf{f}_g \equiv D\mathbf{f}_{g1} + (1-D)\mathbf{f}_{g2} \,. \tag{3.29}$$

This is a result derived in [10], following the *state-space averaging* analysis method in [21,22]. When $T_p \to 0$, $\mathbf{x}(t) \to \mathbf{X}$; i.e., all inductor currents and capacitor voltages are DC only. In this case, DC model equations simply state that average voltages across inductors and average currents through capacitors must be zero, provided that a steady-state solution exists. A necessary and sufficient condition for existence of a *unique* solution to Eq. (3.26) is

$$\det \left[\begin{array}{c|c} \mathbf{0} & \mathbf{F} \\ \hline -\mathbf{F}^T & -\mathbf{G} \end{array}\right] \neq 0 \,. \tag{3.30}$$

It is important to note that condition (3.30) is equivalent to condition (3.23) for sufficiently small T_p, but not in general. Consider, for example, PWM converter in Fig. 3.1. Condition (3.30) is satisfied and, indeed, for $T_p << \sqrt{LC}$, the output voltage is $V_{out} = DV_g$, as predicted by the DC model. However, if $D = 0.5$ and $T_p = 2\pi\sqrt{LC}$, it is easy to verify that condition (3.23) is not satisfied and that the output voltage blows up as shown in Figure 3.1.

The following proposition gives an important consequence regarding topology of PWM converters that satisfy condition (3.30).

Proposition 3.3 *In a voltage-to-voltage PWM converter for which there exists a unique solution to DC model equations, the number of capacitors is equal to the number of inductors.*

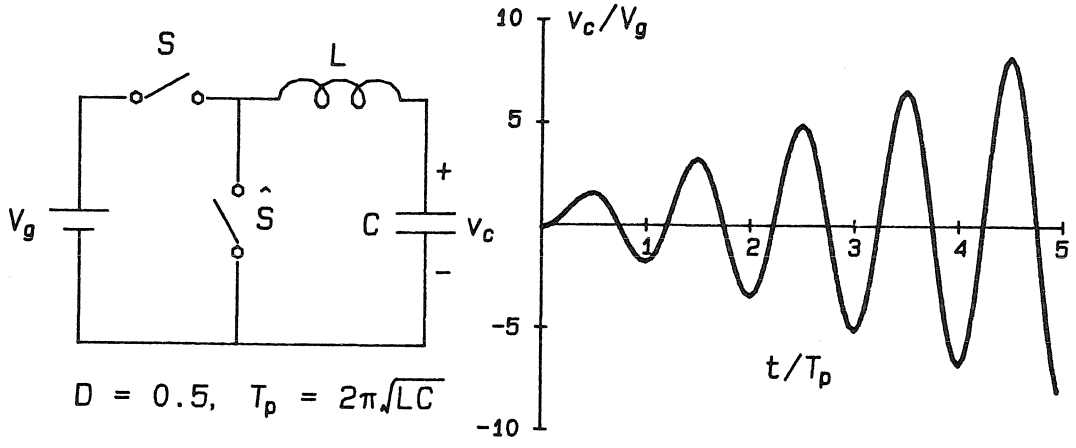


Figure 3.1: A PWM converter with unbounded response although $\det \mathbf{F} \neq 0$.

Proof: if $n_l > n_c$, or $n_c > n_l + 1$, the matrix in condition (3.30) is singular trivially. However, if $n_c = n_l + 1$, and condition (3.30) is satisfied, it follows that $\mathbf{I}_L = \mathbf{0}$ and, consequently, $V_{out} = 0$; i.e., DC-to-DC conversion is not possible. Thus, n_c must be equal to n_l. $\lhd$

With $n_c = n_l$, condition (3.30) reduces to:

$$\det \mathbf{F} \neq 0\,. \tag{3.31}$$

Provided that condition (3.31) is satisfied, the unique solution to DC model, Eqs. (3.26) and (3.27), is given by

$$\mathbf{I}_L = \mathbf{F}^{-T}\left[\mathbf{G}\mathbf{F}^{-1}\mathbf{f}_g - \mathbf{g}\right] V_g\,, \tag{3.32}$$

$$\mathbf{V}_C = -\mathbf{F}^{-1}\mathbf{f}_g V_g\,, \tag{3.33}$$

$$M(D) = -\mathbf{f}_c^T\mathbf{F}^{-1}\mathbf{f}_g + f_{rg}\,. \tag{3.34}$$

3.4 Some General Properties of PWM Converters

It is clear that for $T_p \to 0$, $M(D)$ is a ratio of polynomials in D, $M(D) = P(D)/Q(D)$. Define the degree of the DC conversion ratio by

$$\deg M(D) \equiv \max(\deg P(D),\ \deg Q(D))\,. \tag{3.35}$$

The following results relate the degree of the conversion ratio to complexity of a PWM converter and to some special features, namely, possible coupling of inductors and continuous terminal currents.

Proposition 3.4 *If* $\det \mathbf{F} \neq 0$ *for a voltage-to-voltage PWM converter, then*

$$\deg M(D) \leq \min(n, n_s) . \tag{3.36}$$

Proof: from Eqs. (3.9) and (3.28),

$$\mathbf{F} = \mathbf{F}_1 - \mathbf{F}_{ls}\mathbf{F}_{\hat{s}s}^{-1}\mathbf{F}_{\hat{s}c} + D\mathbf{F}_{ls}\mathbf{F}_{\hat{s}s}^{-1}\mathbf{F}_{\hat{s}c} . \tag{3.37}$$

From the solution (3.34) of DC model equations, we have that

$$\deg Q(D) \leq \deg \det \mathbf{F} . \tag{3.38}$$

Therefore,

$$\begin{aligned} \deg Q(D) &\leq \operatorname{rank}(\mathbf{F}_{ls}\mathbf{F}_{\hat{s}s}^{-1}\mathbf{F}_{\hat{s}c}) \\ &\leq \min(\operatorname{rank}(\mathbf{F}_{ls}), \operatorname{rank}(\mathbf{F}_{\hat{s}c})) \\ &\leq \min(n, n_s) . \end{aligned} \tag{3.39}$$

Suppose that source V_g and an arbitrary capacitor $C_i \in \mathcal{C}$ interchange their positions in the converter network. It is easy to verify that the new network is a PWM converter. Moreover, since complexity of the network is not altered, determinant of the matrix $\mathbf{F}_{new}$ for the new converter is a polynomial in D of a degree at most equal to $\min(n, n_s)$. By noting that $\det \mathbf{F}_{new}$ is in the numerator of V_{C_i}/V_g for the original converter, the proof is completed. $\lhd$

Proposition 3.4 states that a voltage-to-voltage PWM converter with a conversion ratio of degree $m \geq 1$ must have at least m inductors, m capacitors and $2m$ switches.

Beneficial coupling of inductors is possible if the inductors share identical voltage waveforms. Proposition 3.5 relates this condition to a possible degree of $M(D)$.

Proposition 3.5 *If* k *inductors share identical voltage waveforms in a voltage-to-voltage PWM converter for which* $\det \mathbf{F} \neq 0$, $\deg M(D) \leq n - k + 1$.

Proof: Suppose that first k inductors share identical voltage waveforms; i.e.,

$$v_{L_1} = v_{L_2} = \ldots = v_{L_k}, \quad \forall t\,. \tag{3.40}$$

Inductor voltages are linearly independent combinations of capacitor voltages and possibly V_g. Hence, Eqs. (3.40) represent a system of $k-1$ linearly independent equations in capacitor voltages and V_g. The coefficients in these equations are independent of D. By assumption, there is a unique solution to DC model equations so that there can be at most $n-k+1$ linearly independent equations in capacitor voltages and V_g with coefficients that depend on D. $\lhd$

For a converter in which all inductors can be coupled and realized on a single magnetic core, $M(D)$ is necessarily of degree one.

Finally, the following property relates the feature of continuous input and output currents to the degree of $M(D)$. Input current is the current supplied by the input voltage source V_g. Output current can be defined unambiguously only if load R is in parallel with a single capacitor. Then, output current is defined as the sum of the load current and the output capacitor current.

Proposition 3.6 *In a voltage-to-voltage PWM converter that has a single capacitor in parallel with load R and for which* $\det \mathbf{F} \neq 0$,

1. *if input current is continuous,* $\deg P(D) \leq n-1$.
2. *if output current is continuous,* $\deg Q(D) \leq n-1$.

Proof: if input current is continuous, then

$$(\mathbf{f}_{g1}^T - \mathbf{f}_{g2}^T)\mathbf{I}_L = 0. \tag{3.41}$$

If $\mathbf{f}_{g1}^T - \mathbf{f}_{g2}^T = \mathbf{0}$, then $\mathbf{f}_g$ does not depend on D. Since there is a single capacitor across the load, $f_{rg} = 0$ so that $\deg P(D)$ is at most equal to $n-1$. If, however, $\mathbf{f}_{g1}^T - \mathbf{f}_{g2}^T \neq \mathbf{0}$, there can be at most $n-1$ equations in inductor current with coefficients that depend on D. Hence, $\deg M(D) \leq n-1$. The proof for part 2 is exactly the same except that $\mathbf{f}_{gi}$ is replaced by the column of $\mathbf{F}_i$ corresponding to the capacitor across the load. $\lhd$

For example, Proposition (3.6) states that a voltage-to-voltage PWM converter with a single capacitor across the load and both input and output currents continuous must have at least two inductors and two capacitors.

3.5 Some General Properties of Two-Switch PWM Converters

In a PWM converter, the minimum number of switches is two – one S-switch and one $\hat{S}$-switch. Two-switch PWM converters and converters derived from two-switch converters by insertion of an isolation transformer are most frequently used in practical applications. Hence, general topological properties of two-switch PWM converters are of particular interest.

The first property is a corollary of Proposition 3.1:

Proposition 3.7 *In a two-switch PWM converter:*

1. *Switch S, switch $\hat{S}$ and a non-empty set of inductors $\mathcal{L}_{on} \subseteq \mathcal{L}$ form a cut-set.*
2. *Switch S, switch $\hat{S}$, a set of capacitors $\mathcal{C}_{off} \subseteq \mathcal{C}$, and possibly V_g form a loop. Denote the set of all elements in the loop less switches by $\mathcal{V}_{off}$. $\mathcal{V}_{off}$ is non-empty.*

Proof: By Proposition 3.1, $\{S\} \cup \mathcal{C} \cup \{V_g\}$ is a tree for the graph G. Since there are no inductor-only cut-sets, the fundamental cut-set for S must include $\hat{S}$. If only S and $\hat{S}$ are in the cut-set, both switches could be removed without affecting operation of the circuit. But S and $\hat{S}$ are the only switches in the converter network. Hence, the fundamental cut-set for S must include a non-empty set of inductors. Part 2 follows by a dual argument. $\lhd$

Define the following quantities:

$$I_{on} \equiv \sum_{\mathcal{L}_{on}} I_i \,, \tag{3.42}$$

$$V_{off} \equiv \sum_{\mathcal{V}_{off}} V_i \,. \tag{3.43}$$

It is assumed that reference orientation is always chosen such that $I_{on} > 0$ and $V_{off} > 0$. Note that if $I_{on} = 0$ (or $V_{off} = 0$), both switches could be removed (or shorted) without affecting operation of the circuit. But, then, the circuit is not a valid DC-to-DC converter, so that both quantities must be positive.

By definition, voltage V_{off} is equal to the voltage across the switch when it is OFF, while I_{on} is the current through the switch when it is ON. Hence, switch voltage and current stresses in a two-switch PWM converter are given by V_{off} and I_{on} respectively.

The next proposition is instrumental in deciding whether or not the coupled-inductors technique is applicable to a certain two-switch topology.

Proposition 3.8 *In a two-switch PWM converter, all inductors in $\mathcal{L}_{on}$ share the same voltage waveforms.*

Proof: take $\hat{\mathcal{T}}_s$ for a tree of G. By assumption, S, $\hat{S}$ and inductors in $\mathcal{L}_{on}$ form a cut-set. Every loop that contains one element in the cut-set must contain another element from the cut-set. In particular, the fundamental loop for every inductor in $\mathcal{L}_{on}$ must contain $\hat{S}$ since this is the only tree branch in the cut-set. It follows that every two inductors in $\mathcal{L}_{on}$ are in a loop with a set of capacitors, possibly V_g and no switches. By the small-ripple assumption, voltages across all capacitors are DC only. Hence, all inductors in $\mathcal{L}_{on}$ share identical voltage waveforms. $\lhd$

Proposition 3.8 implies that all inductors in $\mathcal{L}_{on}$ can be realized on a single magnetic core with possibly beneficial, coupled-inductor filtering effects.

The next property relates the switch stress quantities to external quantities in a two-switch PWM converter:

Proposition 3.9 *If $M(D) = P(D)/Q(D)$ is the DC conversion ratio of a two-switch voltage-to-voltage PWM converter for which* $\det \mathbf{F} \neq 0$, *then*

$$\frac{V_{off}}{V_g} = \frac{1}{|Q(D)|}, \tag{3.44}$$

$$\frac{I_{on}}{I_{out}} = \frac{1}{|Q(D)|}. \tag{3.45}$$

Proof: Starting from the converter network N, construct a new network N_{dc} by shorting all inductors and removing all capacitors. The network N_{dc} consisting of four elements (V_g, S, $\hat{S}$ and R) must be connected by the following argument. Suppose that the corresponding graph G_{dc} is not connected. Then, in G, and therefore in G_i, $i = 1, 2$, there is a capacitor-only cut-set. But then, columns in $\mathbf{F}$ corresponding to capacitors in the cut-set are linearly dependent so that $\det \mathbf{F} = 0$, which is a contradiction. Now suppose that in G_{dc}, S and $\hat{S}$ form a cut-set. Then, in G there exists a cut-set that contains both switches and a possibly empty set of capacitors. This, together with Proposition 3.7(1) implies that inductors in $\mathcal{L}_{on}$ form a cut-set with a possibly empty

set of capacitors. In this case, however, $I_{on} = 0$, which is a contradiction. By a dual argument, S and $\hat{S}$ in G_{dc} do not form a loop. It follows that G_{dc} must have three nodes and that $\{V_g, S\}$ or $\{V_g, \hat{S}\}$ form a tree for G_{dc}.

Without loss of generality, assume that elements of $\{V_g, \hat{S}\}$ form a tree for G_{dc}. Then,

$$V_{out} = \alpha \bar{v}_{\hat{s}} + \beta V_g \,, \tag{3.46}$$

or, since the average voltage across $\hat{S}$-switch is DV_{off},

$$M(D) = \frac{P(D)}{Q(D)} = \alpha D \frac{V_{off}}{V_g} + \beta \,, \tag{3.47}$$

where $\alpha, \beta \in \{-1, 0, 1\}$. Denote $V_{off}/V_g = X(D)/Y(D)$. $Y(D)$ must be equal to $Q(D)$ since $M(D)$ is of degree 1. Then, $X(D)$ must be equal to a constant γ and $\gamma\alpha \neq 0$. Since V_g and $\hat{S}$ form a tree, V_{off} must be equal to V_g for $D = 0$. But $|Q(0)| = |\det \mathbf{F}_1| = 1$ since $\mathbf{F}_1$ is the fundamental loop matrix for network N_1. Hence, $|\gamma| = 1$ and the sign of γ is chosen so that V_{off} is positive.

The second part of Proposition 3.7 follows by a dual argument after noting that $M(D) = I_g/I_{out}$ and by interchanging V_{out} with I_g and V_{off} with I_{on}. $\lhd$

One important consequence of Proposition 3.9 is that *all* two-switch converters with the same DC conversion ratio impose identical voltage and current stresses on switching devices regardless of the number of reactances and the specific topology.

Another consequence, previously conjectured in [20], is that

$$\frac{V_{off}}{I_{on}} = \frac{V_g}{I_{out}} = \frac{R}{M}. \tag{3.48}$$

This property leads to a general analysis method for two-switch DC-to-DC converters derived from two-switch PWM converters, as discussed in the next section.

3.6 A Unifying Analysis Method for Two-Switch DC-to-DC Converters

A switched-mode converter with two switches is depicted in Fig. 3.2 as a linear, time-invariant, four-port LC network Γ with source V_g, load R and switches S and $\hat{S}$ attached to the ports. Since average voltage across every inductor and average current

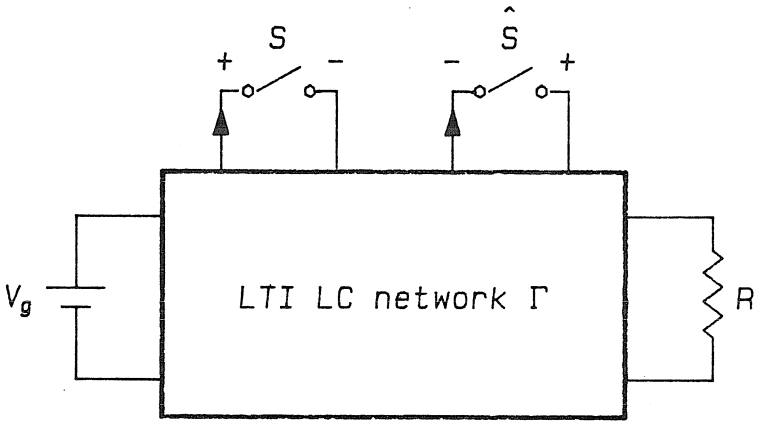


Figure 3.2: Structure of a two-switch DC-to-DC Converter.

through every capacitor in Γ must be equal to zero, applying the averaging operator to the converter network is equivalent to shorting all inductors and removing all capacitors. The resulting DC network, Γ_{DC}, consists of only interconnections among the four ports.

Suppose that the converter in Fig. 3.2 has the same DC network as some PWM converter with DC conversion ratio $M(D)$. Then, Kirchhoff's voltage and current laws for the loop and the cut-set of Proposition 3.7 yield

$$\overline{v}_S + \overline{v}_{\hat{S}} = \overline{v}_{off} \equiv V_{off}\,, \tag{3.49}$$

$$\overline{i}_S + \overline{i}_{\hat{S}} = \overline{i}_{on} \equiv I_{on}\,. \tag{3.50}$$

In general, v_{off} and i_{on} need not be DC quantities. Therefore, V_{off} and I_{on} should not be regarded as switch stresses but only as average values of v_{off} and i_{on} waveforms. Since there is no power loss in the converter,

$$\overline{v}_S \overline{i}_S = \overline{v}_{\hat{S}} \overline{i}_{\hat{S}}\,. \tag{3.51}$$

Define *equivalent duty ratio*, m, by

$$m \equiv \frac{\overline{v}_{\hat{S}}}{V_{off}} = \frac{\overline{i}_S}{I_{on}}\,. \tag{3.52}$$

From Eqs. (3.49) through (3.51), it is easy to verify that two expressions for m are equivalent.

The DC conversion ratio, M, of the converter in Fig. 3.2 becomes

$$M = M(m)\,, \tag{3.53}$$

where $M(\cdot)$ is the function inherited from the *parent* PWM converter, which has the same DC network. This result is not immediately useful since the equivalent duty ratio m is not known. In general, m is a function of the vector τ_c of controllable intervals for the specific operating mode and the ratio V_{off}/I_{on},

$$m = m(\tau_c, \frac{V_{off}}{I_{on}})\,. \tag{3.54}$$

Quantities V_{off} and I_{on} appear only in the ratio since Γ is a linear network. Now, the significance of Eq. (3.48) becomes apparent since the equivalent duty ratio can be expressed as a function of the converter external quantities only:

$$m = m(\tau_c, \frac{V_g}{I_{out}}) = m(\tau_c, \frac{R}{M})\,. \tag{3.55}$$

Of the two forms for the equivalent duty ratio, the one in terms of input voltage and output load current is more convenient. If the second form is used, the DC conversion ratio M appears on both sides of the equation $M = M(m)$. The final goal of DC analysis is to find M as function of τ_c and R, but an explicit solution for M may not exist. If, however, the first form is used, one need determine only the equivalent duty ratio while the DC conversion ratio M as a function of τ_c, V_g and I_{out} follows simply by substituting m as an argument of $M(\cdot)$. The unifying aspect of the analysis method stems from the fact that the equivalent duty ratio is *independent* of the parent PWM topology.

This analysis method was originally proposed in [20], where it was used in the analysis of two classes of Quasi-Resonant converters. In this thesis, generality of the method is demonstrated by its application to DC analyses of PWM converters in discontinuous modes (Section 5.2) and to DC analyses of various classes and operating modes of Quasi-Resonant converters in Chapters 7 through 10. In all cases, in order to apply the method, only the condition that the converter's DC network is the same as the DC network of some PWM converter needs to be verified.

Chapter 4

Synthesis of PWM DC-to-DC Converters

Based on the results of Chapter 3, construction of a synthesis procedure for PWM DC-to-DC converters is undertaken in this chapter. The idea that systematic synthesis of converter topologies can be reduced to systematic generation of matrix representations for the converter topology is not new [10]. In the implementation, however, the approach in this chapter departs from the one in [10] at the very beginning – in the choice of the algebraic representation for the converter topology. Distinctive feature of the new approach is that switches (their position and implementation) are taken into account as essential parts of the converter topology.

As discussed in Section 4.1, a PWM converter can be represented by a pair of incidence matrices for the graphs G_1 and G_2, corresponding to the switched LTI networks N_1 and N_2. The synthesis procedure based on this matrix representation encompasses construction of viable pairs of incidence matrices, insertion of switches in order to obtain complete converter networks and, finally, implementation of switches as transistors, diodes, current-bidirectional, voltage-bidirectional or four-quadrant switches.

In Sections 4.3 and 4.4, two cases of practical interest are considered in detail – second-order and fourth-order converters with up to four switches, a common input and output terminal and a single capacitor across the load. It is found that the complete class of second-order converters contains six well-known members. Results of the synthesis of fourth-order converters are presented in Section 4.5. Among 27 two-switch converters, there are seven step-down, seven step-up, nine step-up/step-down and four topologies with DC conversion ratios that change sign at $D = 0.5$. All of these converters were previously found in [9], but now it is possible to claim that classes of two-switch converters are complete. There are 522 fourth-order, four-switch converters. Systematic search through these topologies reveals a number of previously unrecognized single-transistor

converters with conversion ratios of degree two.

In all cases, a comparison is made among converters that share the same DC conversion ratio. It is shown that conversion efficiency can be vastly different solely because of variations in the converter topology. Results of the comparison are confirmed experimentally.

The main contribution of this chapter is the completely formalized synthesis procedure which, in contrast to previous work, guarantees that complete classes of PWM converters are constructed. Also, novel converter topologies and the comparison of converters in generated classes are the results of practical interest.

4.1 Representation of the Converter Topology

An essential step in the development of an analytic synthesis procedure is selection of the matrix representation for the converter topology. In Chapter 3, a PWM topology was represented by the fundamental loop matrix $\mathbf{F}_n$. This matrix representation, which includes S-switch currents and $\hat{S}$-switch voltages as additional states of the system, was instrumental in derivation of general properties of PWM converters and DC model equations.

For a given complexity, i.e., a given number of capacitors, inductors and switches, all converters can be generated simply by constructing all possible matrices $\mathbf{F}_n$. Clearly, there are only a finite number of possible topologies since, by definition, entries in the fundamental loop matrix are -1, 0 or 1. Practical difficulties arise from the fact that for some choices of entries, $\mathbf{F}_n$ may not represent a realizable network. The problem of checking realizability can be completely avoided if an alternative matrix representation is selected.

Two linear, time-invariant networks are repeatedly switched in a PWM converter. The pair of graphs (G_1, G_2) is unique for the converter topology with graph G. However, since switches are not represented explicitly in G_1 and G_2, the converse may not be true. Thus, if the pair (G_1, G_2) should represent the converter topology unambiguously, an algorithm for insertion of switches needs to be specified.

Fundamental loop or cut-set matrices are not appropriate matrix representations

of the pair (G_1, G_2) since graphs G_1 and G_2 may be separable, and relative position of parts cannot be retrieved from the fundamental matrices. Although irrelevant for electrical operation of the circuit, the exact position of the parts is decisive for the position and possible implementation of switches. Information about the complete converter network is preserved if, instead, graphs G_1 and G_2 are represented by the corresponding incidence matrices, $\mathbf{H}_1$ and $\mathbf{H}_2$. Again, by definition, entries in the incidence matrices are -1, 0 or 1. Therefore, this matrix representation, together with an algorithm for insertion of switches, can be used as the basis for the systematic synthesis procedure in which generation of all converters with a given number of reactive elements is reduced to construction of all possible pairs $(\mathbf{H}_1, \mathbf{H}_2)$. Since it is easy to construct only incidence matrices that represent realizable networks, the emerging synthesis procedure becomes technically simple and intuitively appealing.

If the tree $\mathcal{T}$ is chosen for the graphs G_1 and G_2 and if the edges are ordered as $\{V_g\}$, $\mathcal{C}$, $\{R\}$, $\mathcal{L}$, we have

$$\mathbf{H}_i = \left[\begin{array}{c|c} \mathbf{T}_i & \mathbf{E}_i \end{array} \right] . \tag{4.1}$$

Columns of $\mathbf{T}_i$ and $\mathbf{E}_i$ correspond to branches and chords of G_i. The fundamental loop matrices can be found from

$$\mathbf{F}_{ni} = \mathbf{E}_i^T \mathbf{T}_i^{-T} , \tag{4.2}$$

so that DC model of Section 3.3 can be utilized in the synthesis procedure.

4.2 Scope of the Synthesis Procedure

The goal of the synthesis procedure is not only to generate all possible topologies but also to sort out the converters with a prescribed set of properties and to make a systematic comparison among them. Any combination of properties that depend on the converter topology alone can be chosen as a criterion for the extraction of converters:

1. number of capacitors and inductors,

2. number of switches,

3. number of transistor switches,

4. DC conversion ratio $M(D)$,

5. continuous input and/or output current,

6. possible coupling of inductors.

The framework described so far is completely general because the matrix representation and its connection to DC conversion ratio are valid for PWM topologies of arbitrary complexity, i.e., converters with an arbitrary, finite number of reactive elements and switches. Therefore, the synthesis procedure emerging from this framework is quite general as well. In this chapter, however, the synthesis procedure will be developed in detail and applied only to cases of practical interest.

Structure of PWM converters encompassed by the synthesis procedure is depicted in Fig. 4.1. It is assumed that load R is in a loop with a single capacitor C_1. Source V_g and load R share a common node (ground), and the box named *converter cell* (as in [8,9]) consists of n inductors, $n-1$ capacitors and $2n_s$ switches. Converters with a floating load or with a load in a loop with more than one capacitor and (possibly) V_g are treated in Chapter 5 as extensions of topologies generated by the synthesis procedure.

Two cases are considered:

1L cell (second-order) converters, with $n = 1$ and $1 \leq n_s \leq 2$,

2L1C cell (fourth-order) converters, with $n = 2$ and $1 \leq n_s \leq 2$.

Virtually all required or preferred features of DC-to-DC converters can be implemented by second-order and fourth-order converters. Since more complex converters have inevitably lower efficiency, higher size, weight and cost, hardly any practical application could be found for converters of higher complexity. Thus, limited scope of the synthesis procedure is well justified.

The synthesis procedure for second-order and fourth-order converters is completely formalized. The number of second-order converter topologies is sufficiently small so that the procedure can be carried out by hand. For fourth-order converters, however, the synthesis procedure is implemented in a simple computer program so that the otherwise formidable task of enumerating and sorting out surprisingly large number of converter topologies is accomplished efficiently.

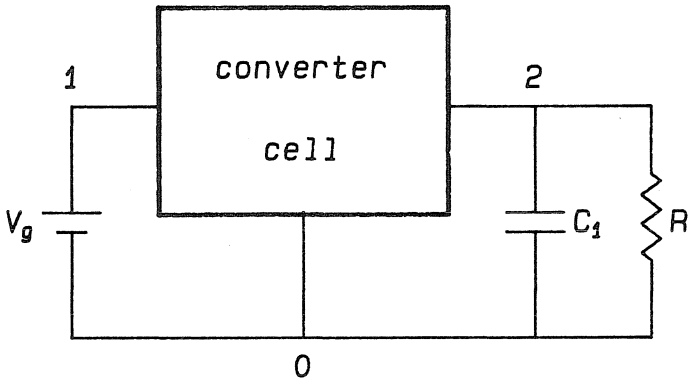


Figure 4.1: Structure of PWM DC-to-DC converters encompassed by the synthesis procedure.

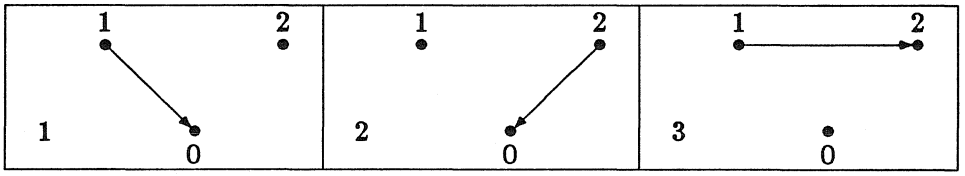


Table 4.1: Possible positions of the inductor in a second-order PWM converter.

4.3 Synthesis of Second-Order PWM Converters

4.3.1 Enumeration of Second-Order (1L) Converter Topologies

The problem of enumeration of converter topologies is equivalent to the problem of enumeration of all possible pairs of incidence matrices $(\mathbf{H}_1, \mathbf{H}_2)$ that represent distinct PWM topologies.

Since the converter cell contains only one element, graphs G_1 and G_2 have three nodes. The inductor can be connected between any two nodes, as shown in Table 4.1 where possible positions of the inductor edge are enumerated. The inductor position is labeled by a number of the form $i.s$, where $i \in \{1,2,3\}$ denotes the position of the non-oriented inductor edge according to Table 4.1, while $s \in \{1,2\}$ denotes orientation of the edge. We take $s = 1$ to denote orientations as in Table 4.1 and $s = 2$ to denote the opposite orientation. Now, instead of the pair of incidence matrices, the pair of numbers $(i_1.s_1, i_2.s_2)$ can be used equivalently. The total number of pairs is $(3 \times 2)^2 = 36$. Because

representation is not unique and because some representations may lead to networks that are not PWM converters or for which there is no steady-state solution, the total number of distinct second-order PWM DC-to-DC converters is much smaller.

4.3.2 Elimination of Redundant Cases

Redundant cases arise because representation of the converter topology by the pair $(i_1.s_1, i_2.s_2)$ is not unique. The topology is invariant under the simultaneous change of orientation of any edge in both graphs. Furthermore, the order of switched networks does not affect the resulting topology. Redundant pairs are eliminated by the following rules:

1. The same converter results if orientation of the inductor edge is changed in both graphs. Redundant cases are avoided by taking

$$s_1 \equiv 1; \quad s_2 \equiv s \in \{1, 2\}. \tag{4.3}$$

   Since orientation $s_1 = 1$ is taken by default in one graph, a legitimate pair is of the form $(i_1, i_2.s)$. The number of pairs under consideration is reduced to 18.

2. Pairs $(i_1, i_2.s)$ and $(i_2.s, i_1)$ represent identical converter topologies with S-switches and $\hat{S}$-switches interchanged, i.e., with conversion ratios $M(D)$ and $M(1-D)$, respectively. To avoid redundant cases, require that

$$i_1 \leq i_2, \tag{4.4}$$

   which further reduces the number of eligible pairs to 12.

4.3.3 Elimination of Degenerate Cases

The term "degenerate" is used to denote cases in which the pair $(\mathbf{H}_1, \mathbf{H}_2)$ represents a switched electrical network that is not a valid DC-to-DC converter with a unique, bounded steady-state solution:

Definition 4.1 *Pair* $(\mathbf{H}_1, \mathbf{H}_2)$ *is non-degenerate if and only if the corresponding DC model equations have a unique, bounded steady-state solution and* $\deg M(D) \geq 1$.

In the case of 1L converter cells, it follows easily that the pair $(\mathbf{H}_1, \mathbf{H}_2)$ is degenerate if and only if the position of the inductor edge (i) is the same in both graphs. Thus, all degenerate cases are eliminated by the condition

$$i_1 \neq i_2 \,, \tag{4.5}$$

which leaves only 6 distinct and non-degenerate pairs representing all second-order PWM DC-to-DC converters with the structure shown in Fig. 4.1.

4.3.4 Insertion of Ideal Switches

Once a pair of incidence matrices is proved to be non-degenerate, the actual converter with ideal switches could be drawn by inspection of two networks consisting of only three elements. However, the problem of constructing the complete converter network with switches needs to be solved explicitly in order to complete the synthesis procedure.

The goal of a switch-insertion procedure is to construct a single network N with a *minimum* number of ideal switches such that it reduces to network N_1 when S-switches are ON and to network N_2 when $\hat{S}$-switches are ON.

By assumption, the column that corresponds to the inductor edge is the fourth column in the incidence matrices $\mathbf{H}_1$ and $\mathbf{H}_2$. Let x_1 and x_2 be the nodes in graphs G_1 and G_2 to which the inductor edge is incident; i.e.,

$$\mathbf{H}_1(x_1, 4) = \mathbf{H}_2(x_2, 4) \neq 0 \,. \tag{4.6}$$

If $x_1 = x_2$, the inductor end is fixed and no switches are necessary. If, however, $x_1 \neq x_2$, an S-switch and a $\hat{S}$-switch are inserted as shown in Fig. 4.2. The total number of switches can be two, if only one inductor end is switched, or four, if both ends are switched.

Switched Coupled Inductors

In the outlined procedure, four switches are required in the case in which both inductor ends are switched. In this case, however, one inductor and four switches can be replaced by a pair of switched coupled inductors and two switches, as shown in Fig. 4.3. Here, the term "switched" is used to distinguish coupled inductors with pulsating cur-

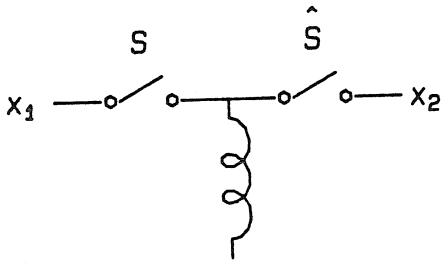


Figure 4.2: Insertion of switches for second-order converters.

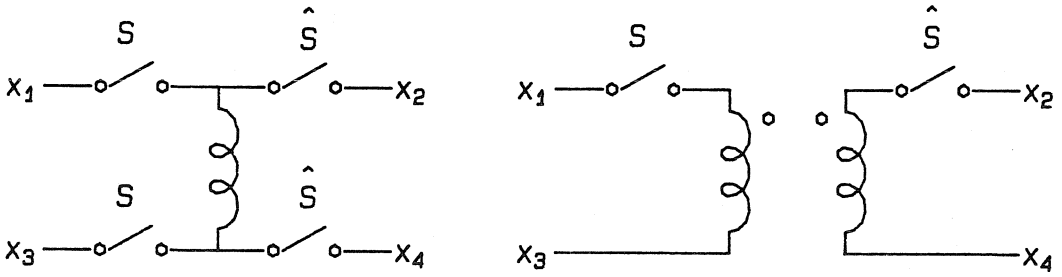


Figure 4.3: A pair of switched coupled inductors and two switches can replace an inductor and four switches.

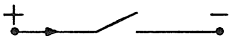
rents from coupled inductors with continuous currents. Switched coupled inductors are electrically equivalent to a single inductor and the order of the system is not increased after the transformation in Fig. 4.3.

4.3.5 Implementation of Switches

In the previous section, a converter with ideal switches is constructed from a pair of switched linear networks. Ideal switches are four-quadrant devices; i.e., they block the voltage and pass the current of either polarity. In practical circuits, however, unidirectional switches (transistors and diodes) are used whenever possible. Therefore, the implementation of ideal switches needs to be resolved in the synthesis procedure.

Consider an ideal switch in the PWM converter network. By Proposition 3.1, voltage V_s across the switch in the OFF position and current I_s through the switch in the ON position are linear combinations of capacitor voltages and inductor currents, respectively.

Since the position of ideal switches is determined by the switch-insertion procedure, V_s and I_s can be computed from the solution of DC model equations. In the computation of V_s and I_s, the usual reference orientations for voltage and current are assumed:



Under the small-ripple assumption, all capacitor voltages and inductor currents are DC only. Consequently, V_s and I_s are also DC quantities and, in general, they are functions of the control variable D.

Several cases are possible, depending on the sign of V_s and I_s on $0 < D < 1$:

1. $V_s I_s > 0$: the switch can be implemented as a *transistor* (bipolar or MOS) since it has to block the voltage and pass the current of the same polarity;

2. $V_s I_s < 0$: the switch can be implemented as a *diode* since it has to block the voltage and pass the current of the opposite polarity;

3. $V_s > 0$ (or $V_s < 0$), I_s changes polarity : the switch can be implemented as *current-bidirectional*;

4. $I_s > 0$ (or $I_s < 0$), V_s changes polarity : the switch can be implemented as *voltage-bidirectional*;

5. both V_s and I_s change polarity : the switch has to be *four-quadrant*.

At this point it is interesting to recall the result of Proposition 2.1, which implies that there must be at least one switch for which $V_s I_s > 0$ (transistor, or *inverter* switch) and at least one switch for which $V_s I_s < 0$ (diode, or *rectifier* switch), for every fixed duty ratio D.

Bidirectional and four-quadrant switches can be implemented as transistors (inverters) or as diodes (rectifiers) if the range of duty ratio D is restricted so that cases 1 or 2 apply.

4.3.6 Complete Set of Second-Order PWM DC-to-DC Converters

All six pairs representing second-order PWM DC-to-DC converters with a common input/output (ground) terminal are listed in Table 4.2, and the networks are readily

	pair	M(D)	converter
1	(1,2.1)	$-D/(1-D)$	buck-boost (inverting)
2	(1,2.2)	$D/(1-D)$	buck-boost (non-inverting)
3	(1,3.1)	$1/(1-D)$	boost
4	(2,3.1)	D/(2D-1)	inverse Watkins-Johnson
5	(1,3.2)	(2D-1)/D	Watkins-Johnson
6	(3,2.2)	D	buck

Table 4.2: All second-order PWM DC-to-DC converters.

identified as well-known converter topologies. The converters are shown in Fig. 4.4. Inverting buck-boost (1), boost (3) and buck (6) converters can be obtained by attaching source and load to rotations of the converter cell 1 in Fig. 4.5. Non-inverting buck-boost (2), inverse Watkins-Johnson (4) and Watkins-Johnson (5) converters result from rotations of the cell 2 with four switches. For these three converters, the number of switches can be reduced if the inductor is replaced by a pair of switched coupled inductors, as shown in the right-hand side of Fig. 4.4.

4.4 Synthesis of Fourth-Order PWM Converters

4.4.1 Enumeration of Fourth-Order (2L1C) Converter Topologies

In this case, the converter cell has three components – one capacitor and two inductors. This capacitor, output capacitor and input voltage source are tree branches for the graphs G_1 and G_2, while inductor edges and load R are the chords. There are 4 nodes in G_i and all possible positions of capacitor and inductor edges are enumerated in Tables 4.3 and 4.4.

The pair $(\mathbf{H}_1, \mathbf{H}_2)$ can be represented equivalently by the pair $(i_1 j_1 k_1 . s_1, i_2 j_2 k_2 . s_2)$, where $i_1, i_2 \in \{1,2,3\}$ denote the position of the capacitor C_2; $j_1, j_2 \in \{1,2,3,4,5,6\}$ denote the position of the inductor L_1; $k_1, k_2 \in \{1,2,3,4,5,6\}$ denote the position of the inductor L_2; and $s_1, s_2 \in \{1,2,3,4,5,6,7,8\}$ indicate the orientation of the edges according to Table 4.5, with + reference orientation shown in Tables 4.3 and 4.4. The

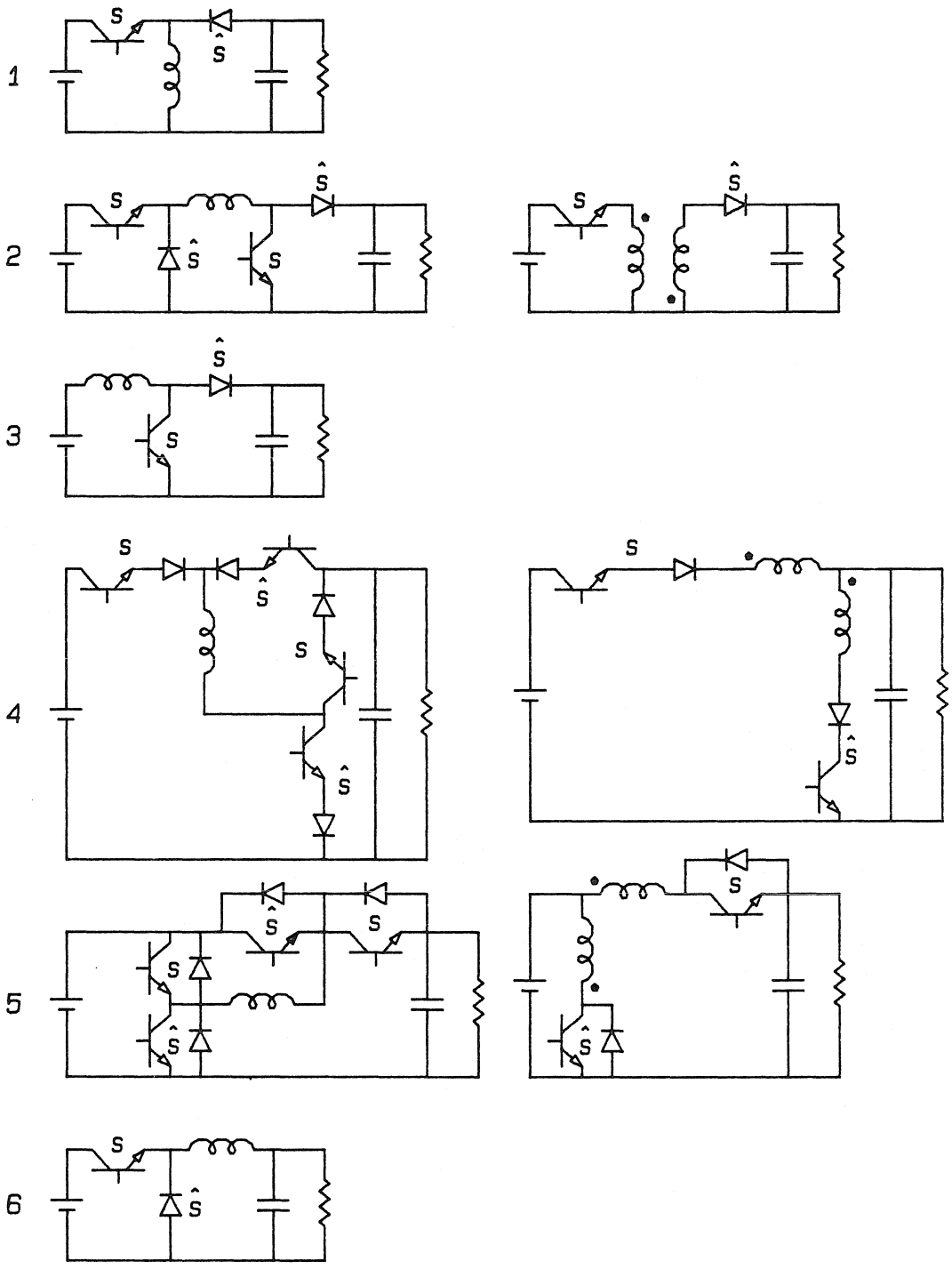


Figure 4.4: Second-order PWM DC-to-DC converters.

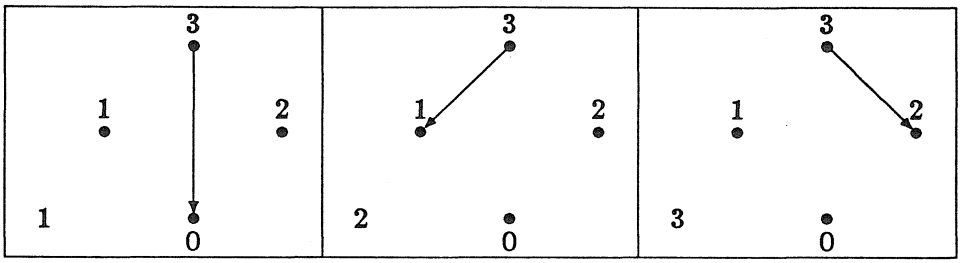


Table 4.3: Possible positions of the capacitor edge in a fourth-order PWM converter.

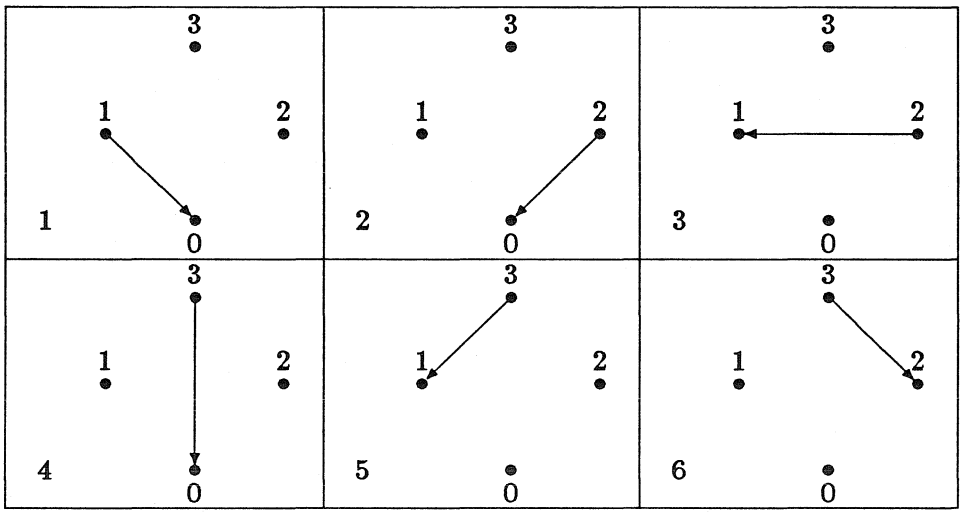


Table 4.4: Possible positions of the inductor edge in a fourth-order PWM converter.

s	C_2	L_1	L_2
1	+	+	+
2	+	+	−
3	+	−	+
4	+	−	−
5	−	+	+
6	−	+	−
7	−	−	+
8	−	−	−

Table 4.5: Orientation of the edges in a fourth-order PWM converter.

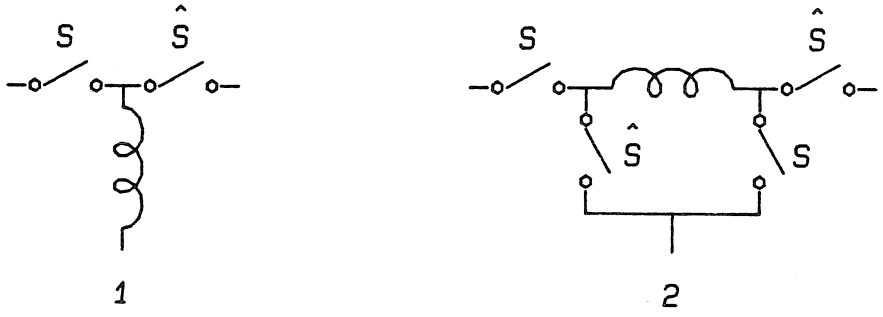


Figure 4.5: 1L converter cells.

total number of pairs is 746496, but since many pairs are redundant or degenerate, the total number of converter topologies is much smaller.

4.4.2 Elimination of Redundant Cases

Converter topology resulting from the pair $(\mathbf{H}_1, \mathbf{H}_2)$ is invariant under the permutation of columns that correspond to the same type of elements, under the simultaneous change of sign of any subset of columns in both matrices and under the change in order of incidence matrices. The following set of rules is established to avoid redundant cases in the enumeration scheme:

1. The same converter results if orientation of any subset of edges in both graphs is changed simultaneously. Therefore, take

$$s_1 \equiv 1\,, \quad s_2 \equiv s \in \{1,2,3,4,5,6,7,8\}\,. \tag{4.7}$$

   Since $s_1 \equiv 1$ is now taken by default, the pair takes the form $(i_1 j_1 k_1, i_2 j_2 k_2.s)$.

2. Pairs $(i_1 j_1 k_1, i_2 j_2 k_2.s)$ and $(i_2 j_2 k_2.s, i_1 j_1 k_1)$ represent the same topology and hence require that

$$i_1 j_1 k_1 \leq i_2 j_2 k_2\,. \tag{4.8}$$

3. Inductor edges L_1 and L_2 or, equivalently, numbers j_1, j_2 and k_1, k_2, can be interchanged without affecting the converter topology. Redundant cases are eliminated

by the following set of conditions:

$$j_1 \leq k_1 \,, \tag{4.9}$$

$$if \;\; j_1 = k_1 \;\; then \;\; j_2 \leq k_2 \,, \tag{4.10}$$

$$if \;\; i_1 = i_2 \;\; then \;\; j_1 k_1 \leq k_2 j_2 \,. \tag{4.11}$$

For example, topologies emerging from (145, 226) and (154, 262) are identical and condition (4.9) will retain only the first pair. Also, (144, 226) and (144, 262) are identical and the latter is removed by condition (4.10). Finally, as an example, (226, 254) and (245, 262) are identical, but only the first one satisfies condition (4.11). In these examples, orientation s is not specified because it is assumed that it can take all possible values.

After all conditions for elimination of redundant cases are applied, the total number of eligible pairs is 26080.

4.4.3 Elimination of Degenerate Cases

Given a pair $(\mathbf{H}_1, \mathbf{H}_2)$ or, equivalently, $(i_1 j_1 k_1, i_2 j_2 k_2 . s)$, the DC model is constructed using Eq. (4.2), and both conditions of Definition 4.1 are easily verified using Eqs. (3.31) and (3.34). Thus, all degenerate cases can be eliminated in a straightforward manner.

In order to eliminate trivial variations of the converter topologies, *strictly non-degenerate* pairs are defined as follows:

Definition 4.2 *Pair* $(\mathbf{H}_1, \mathbf{H}_2)$ *is strictly non-degenerate if it is non-degenerate and none of converter states (capacitor voltages or inductor currents) is identically zero at DC.*

The motivation behind Definition 4.2 is to extract only fourth-order topologies in which all four energy storage elements participate in filtering or in energy transfer. Systematic search through the cases that are non-degenerate but are not strictly non-degenerate reveals that two energy storage elements, a capacitor and an inductor, form a loop or a cut-set in both switched networks. Conversely, a series (parallel) $L - C$ combination can be added between any two nodes (in series with any element) of a PWM DC-to-DC converter without changing its DC conversion properties. Thus, the added combination

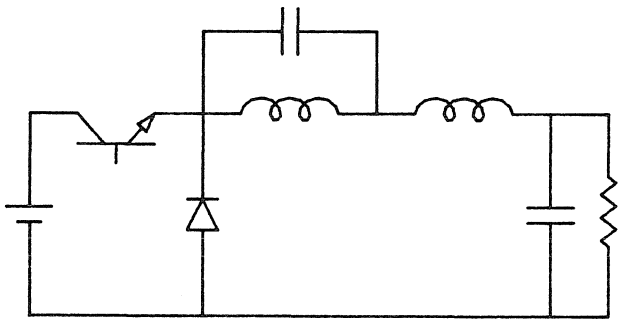


Figure 4.6: Buck converter with a parallel L-C network used for filtering.

is superfluous for energy transfer. Under the small-ripple assumption, a series $L-C$ combination is a very large impedance at the fundamental and the harmonics of the switching frequency. Similarly, a parallel combination is a very small impendance at and above the switching frequency. Hence, addition of a series or parallel $L-C$ combination does not contribute to filtering effects and again, the added combination is superfluous. It should be noted, however, that there are at least two cases when adding a series or parallel $L-C$ combination to a PWM converter may have beneficial filtering effects. First, if the small-ripple approximation is abandoned, an $L-C$ combination could be tuned to suppress the fundamental or any selected harmonic of the switching frequency. For example, a buck converter with this type of filtering is shown in Fig. 4.6. Another interesting possibility arises if the added inductor can be coupled with an existing inductor in order to accomplish the coupled-inductor filtering effects. For example, inductors in the buck converter of Fig. 4.7 can be coupled with the coupling coefficient adjusted so that all current ripple is stirred from L_1 to L_2. Proposition 3.8 gives a simple guideline for adding a series $L-C$ combination to any two-switch topology such that coupling of inductors is possible.

In any case, the addition of a series or parallel $L-C$ combination can be regarded as an optional modification of any existing converter topology. Henceforth, in the synthesis procedure of fourth-order converters, we shall consider only strictly non-degenerate converter topologies without loss of generality. The number of strictly non-degenerate pairs

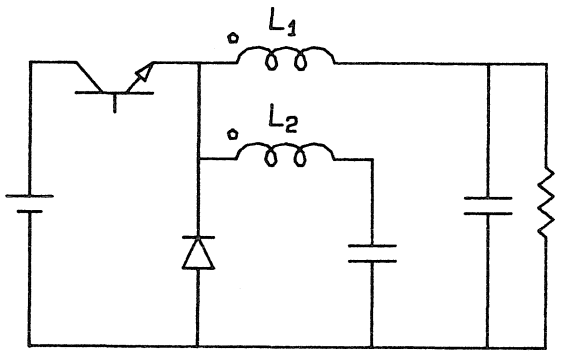


Figure 4.7: Buck converter with a series L-C network used to obtain the output current with zero AC ripple.

representing fourth-order PWM converters is 7146.

4.4.4 Insertion of Ideal Switches

The number of pairs representing fourth-order topologies is so large that it would be nearly impossible to explore all pairs of linear networks and insert the switches by inspection. Besides, no matter how simple linear networks N_1 and N_2 are, classes of generated topologies cannot be regarded as complete unless a switch-insertion procedure is well defined. Thus, a formalized switch-insertion procedure is necessary in order to complete the synthesis task. Furthermore, once construction of the converter network with ideal switches and the procedure for switch implementation are formalized, search for converter topologies with a prescribed number of switches, and with a prescribed number of transistor switches can be performed.

The switch-insertion procedure scans through the columns of incidence matrices corresponding to elements of the 2L1C cell, starting with the third column, corresponding to the capacitor C_2 branch.

Let x_1 and x_2 be "from" nodes and y_1 and y_2 "to" nodes for the capacitor C_2 branch in graphs G_1 and G_2 respectively; that is,

$$\mathbf{H}_1(x_1, 3) = \mathbf{H}_2(x_2, 3) = -1\,, \tag{4.12}$$

$$\mathbf{H}_1(y_1,3) = \mathbf{H}_2(y_2,3) = 1\,. \tag{4.13}$$

All possible cases for the capacitor C_2 are resolved as follows:

1. $\underline{x_1 = x_2 \textit{ and } y_1 = y_2}$: the C_2 branch is fixed and no switches are necessary.

2. $\underline{x_1 \neq x_2 \textit{ and } y_1 = y_2}$: an S-switch and a $\hat{S}$-switch are inserted between nodes x_1 and x_2 as shown in Fig. 4.8. In this case none of the switched nodes (x_1, x_2) can be node 3. This is because exactly one capacitor node has to be node 3 and if, say $x_1 = 3$, then

$$x_2 \neq 3 \Rightarrow y_2 = y_1 = 3 \Rightarrow x_1 \neq 3\,, \tag{4.14}$$

which is a contradiction. Therefore, $x_1, x_2 \in \{0,1,2\}$ and $y_1 = y_2 = 3$. The case $x_1 = x_2$ and $y_1 \neq y_2$ is completely analogous.

3. $\underline{x_1 \neq x_2 \textit{ and } y_1 \neq y_2}$: In this case, one x-node is node 3 and one y-node is 3. Assume, without loss of generality, that $x_1 = 3$ and $y_2 = 3$. Two switches are introduced as shown in Fig. 4.9.

The switch-insertion procedure proceeds with columns corresponding to the inductor edges. Let z_1 and z_2 be "from" (or "to") nodes of the inductor (L_1 or L_2) edge, in graphs G_1 and G_2, respectively; that is,

$$\mathbf{H}_1(z_1,l) = \mathbf{H}_2(z_2,l) \neq 0\,, \tag{4.15}$$

where $l = 5$ for the inductor L_1 edge and $l = 6$ for the inductor L_2 edge. The following cases are possible:

1. $\underline{z_1 = z_2 \neq 3}$: the inductor end is fixed and no switches are necessary.

2. $\underline{z_1 = z_2 = 3}$: if node 3 is switched (case 3 for the C_2 branch), then two switches are necessary as shown in Fig. 4.10. If node 3 is fixed (case 1 or 2 for the C_2 branch), no switches are necessary.

3. $\underline{z_1 \neq z_2}$: two switches are necessary, as shown in Fig. 4.11.

If the procedure calls for insertion of switches between the pair of nodes where the switches have already been inserted, the insertion is skipped. Thus, only necessary

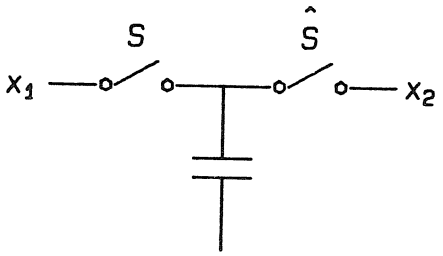


Figure 4.8: Insertion of switches in the case in which one capacitor end is switched.

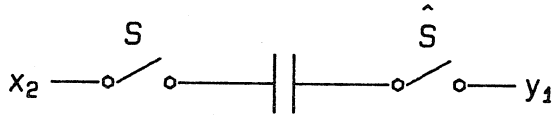


Figure 4.9: Insertion of switches in the case in which both capacitor ends are switched.

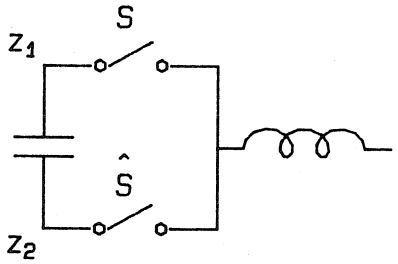


Figure 4.10: Insertion of switches in the case in which the inductor edge is incident to the switched node 3.

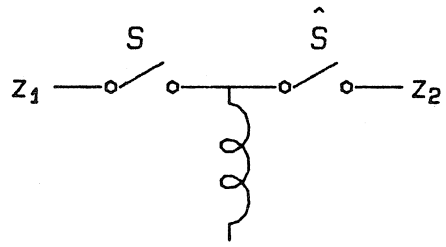


Figure 4.11: Insertion of switches in the case in which the inductor edge is incident to different nodes in networks N_1 and N_2.

switches are introduced, always in $S - \hat{S}$ pairs. By construction, the number of switches can be any even integer from 2 to 10.

The switch-insertion procedure outlined so far guarantees that the resulting network N reduces to the network N_1 when S-switches are ON, and to the network N_2 when $\hat{S}$-switches are ON. By construction, N is a PWM network since it satisfies all assumptions of Definition 3.1. It can be shown that given a pair of networks N_1 and N_2, network N (with minimum number of switches and graph G) is *unique* if and only if switches in S ($\hat{S}$) do not form a path in G of length greater than one. For the synthesis procedure, the necessity part of the proof is important. Suppose that a subset of k switches in S ($\hat{S}$) forms a path in the network N generated by the switch-insertion procedure. Then, one can construct additional k networks that satisfy the same assumptions as network N. First, add another switch such that it closes the loop with the switches in the path. Then, remove one of the k switches in the path. Of course, in order to generate all possible networks, the process has to be repeated for every switch-only path of length greater than one. Clearly, resulting networks are completely equivalent to the original network N with respect to DC conversion properties, number of switches and number of reactances. However, implementation of switches may be different. If the number of switches is limited to four, there can be at most one switch-only path of length two. In addition to the original network generated by the switch-insertion procedure, at most two other networks need to be examined. For each network with ideal switches, implementation of switches is carried out as explained in Section 4.3.5.

4.4.5 Summary of the Synthesis Procedure

In this section, steps of the synthesis procedure are summarized in a form that resembles the flowgraph of the computer program in which the procedure is implemented.

STEP 0 SELECT INPUT REQUIREMENTS

0.1 If the number of switches is prescribed, set flag A and assign n_s^*.

0.2 If the number of transistors is prescribed, set flag B and assign n_t^*.

0.3 If specific DC conversion ratio is required, set flag C and assign $M^*(D)$.

0.4 If continuous input current is required, set flag D.

0.5 If continuous output current is required, set flag E.

0.6 If the possible coupling of inductors is required, set flag F.

STEP 1 FIND THE NEXT PAIR, $(i_1 j_1 k_1, i_2 j_2 k_2 . s)$,

such that conditions of Sections 4.4.1 and 4.4.2 are satisfied. Exit if the last pair was generated.

STEP 2 FIND THE DC MODEL

2.1 Construct incidence matrices, $\mathbf{H}_1$ and $\mathbf{H}_2$, using Tables 4.3 through 4.5.

2.2 Compute fundamental loop matrices, $\mathbf{F}_{n1}$ and $\mathbf{F}_{n2}$, using Eq. (4.2).

2.3 Go back to STEP 1 if condition (3.31) for existence of a unique, steady-state solution is not satisfied.

2.4 Compute $\mathbf{I}_L$, $\mathbf{V}_C$ and $M(D)$ from Eqs. (3.32) through (3.34).

2.5 Go back to STEP 1 if:

2.5.1 $\deg M(D) = 0$.

2.5.2 $I_{Li} = 0$ $(i = 1, 2)$ or $V_{C2} = 0$.

2.5.3 Flag C is set and $M(D) \neq M^*(D)$.

2.5.4 Flag D is set and input current is pulsating.

2.5.5 Flag E is set and output current is pulsating.

2.5.6 Flag F is set and inductor voltages are not identical.

STEP 3 CONSTRUCT THE NETWORK WITH IDEAL SWITCHES

3.1 Insert ideal switches following the procedure of Section 4.4.4.

3.2 Go back to STEP 1 if flag A is set and $n_s \neq n_s^*$.

STEP 4 FIND SWITCH IMPLEMENTATIONS

4.1 Evaluate I_s and V_s for each of the switches and decide if the switch is transistor, diode, current-bidirectional, voltage bidirectional, or four-quadrant, as described in Section 4.3.5.

4.2 If flag B is set and $n_s = 2$, check to see if two S-switches or two $\hat{S}$-switches form a path and repeat STEP 4.1 for two additional variations of switch positions.

4.3 Go back to STEP 1 if flag B is set and $n_t \neq n_t^*$.

STEP 5 DISPLAY CONVERTER TOPOLOGY

and return to STEP 1.

4.5 Results of the Synthesis Procedure

Various applications of the synthesis procedure for fourth-order PWM converters are discussed in this section. First, all possible strictly non-degenerate 2L1C cells with two and four ideal switches are found. Then, complete classes of strictly non-degenerate single-transistor converters with prescribed DC conversion ratio are presented.

Conversion ratios of most practical interest are of degree one: step-down, $M(D) = D$, step-up, $M(D) = 1/(1-D)$, and step-up/step-down, $|M(D)| = D/(1-D)$. These conversion ratios can be realized by second-order converters, as shown in Section 4.3.6. However, fourth-order converters are required to fulfill additional requirements such as possible coupled-inductor filtering and continuous terminal currents.

Converters with $M(D) = D^2$, $|M(D)| = D^2/(1-D)$, $M(D) = 1/(1-D)^2$ or $M(D) = D^2/(1-D)^2$ can be used in applications where large step-down or step-up is required without transformer or in applications (such as laboratory power supplies) where an extremely large range of DC conversion ratios is necessary. By Proposition 3.4, these converters must have at least two inductors, two capacitors and four switches.

Members of the classes with prescribed conversion ratios are compared with respect to conduction losses, switch stresses and features of continuous terminal currents and the possibility of coupling of inductors.

4.5.1 2L1C Cells With Two Switches

There are five cells in this class (Fig. 4.12). Coupling of inductors is possible in converters generated from cells 1 and 3. Input and output currents are continuous in converters generated from cells 3 and 4. Since only cell 3 is symmetrical, a total of 27

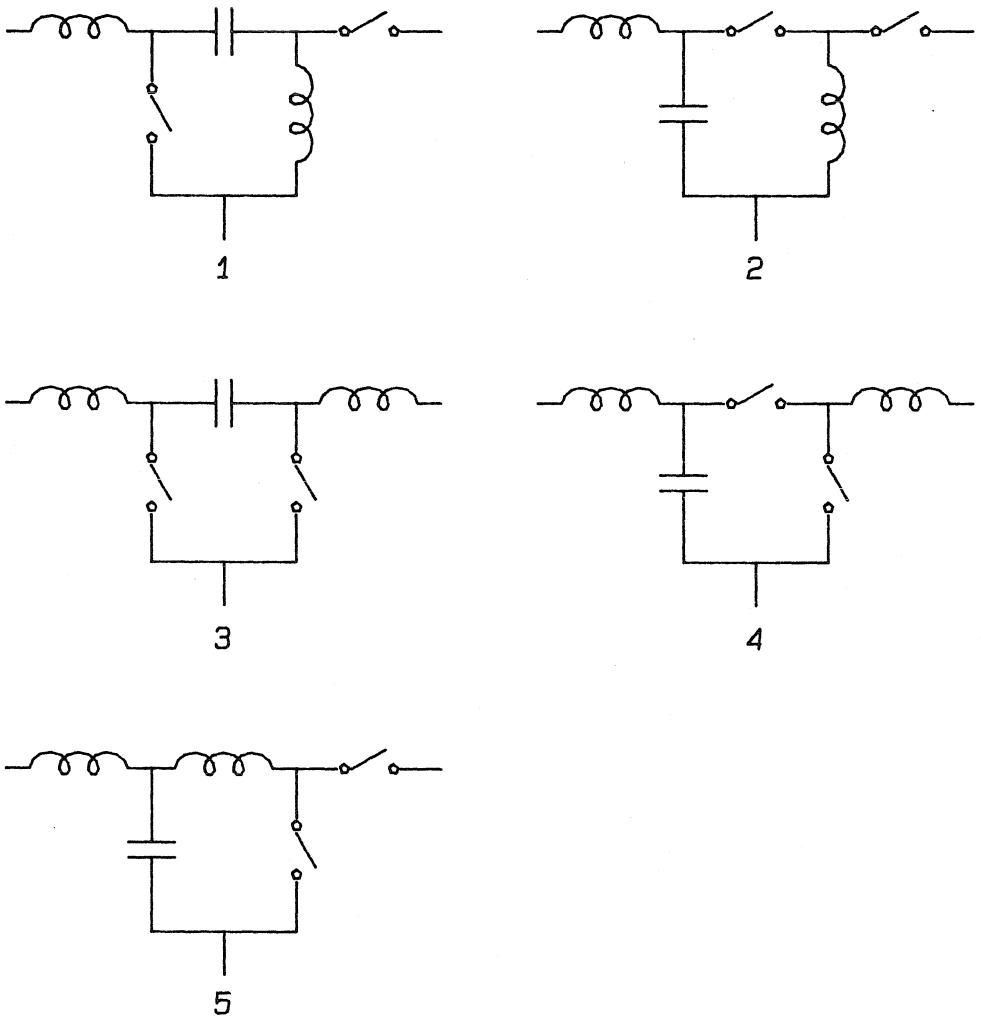


Figure 4.12: 2L1C converter cells with two switches.

#	P	I_{C_1rms}	I_{C_2rms}	I_{grms}	I_{L_1}	I_{L_2}	I	O	C
1	+	0	$\sqrt{M(1-M)}$	M	1	M	√	√	–
2	+	0	0	$\sqrt{M}$	1	1	–	√	–
3	+	0	$\sqrt{M(1-M)}$	M	1	$1-M$	√	√	–
4	+	0	0	$\sqrt{M}$	1	1	–	√	–
5	+	0	$\sqrt{M(1-M)}$	M	$1-M$	M	√	√	√
6	+	$\sqrt{M(1-M)}$	$\sqrt{M(1-M)}$	M	1	M	√	–	–
7	+	$\sqrt{M(1-M)}$	$\sqrt{M(1-M)}$	$\sqrt{M}$	1	$1-M$	–	–	–

Table 4.6: Comparison of fourth-order, two-switch, step-down converters.

converters can be generated by attaching source and load to cell rotations [9].

4.5.2 2L1C Cells With Four Switches

There are 89 cells in this class. Only one cell is counted in cases when the position of switches in the cell is not unique. All cells are listed in Appendix A. Since four cells are symmetrical, 522 fourth-order, four-switch, strictly non-degenerate PWM converters can be generated.

4.5.3 Fourth-Order, Two-Switch, Step-Down Converters

There are seven strictly non-degenerate, fourth-order, two-switch, step-down (SD) converters with $M(D) = D$. All SD converters are shown in Fig. 4.13. By Proposition 3.9, switch voltage and current stresses are the same for all SD topologies. Under the small-ripple assumption, the voltage stress is equal to the input voltage, while the current stress is equal to the output current. Parameters relevant for comparison of SD topologies are summarized in Table 4.6. Column P shows if the topology is inverting polarity of the input voltage (−) or not (+). Columns I and O show whether input (I) or output (O) current is continuous, while column C indicates whether inductors L_1 and L_2 can be coupled on a single magnetic core.

For purpose of comparison, rms currents for all elements are found under the small-ripple assumption. Thus, if only AC ripple current flows through an element, the entry

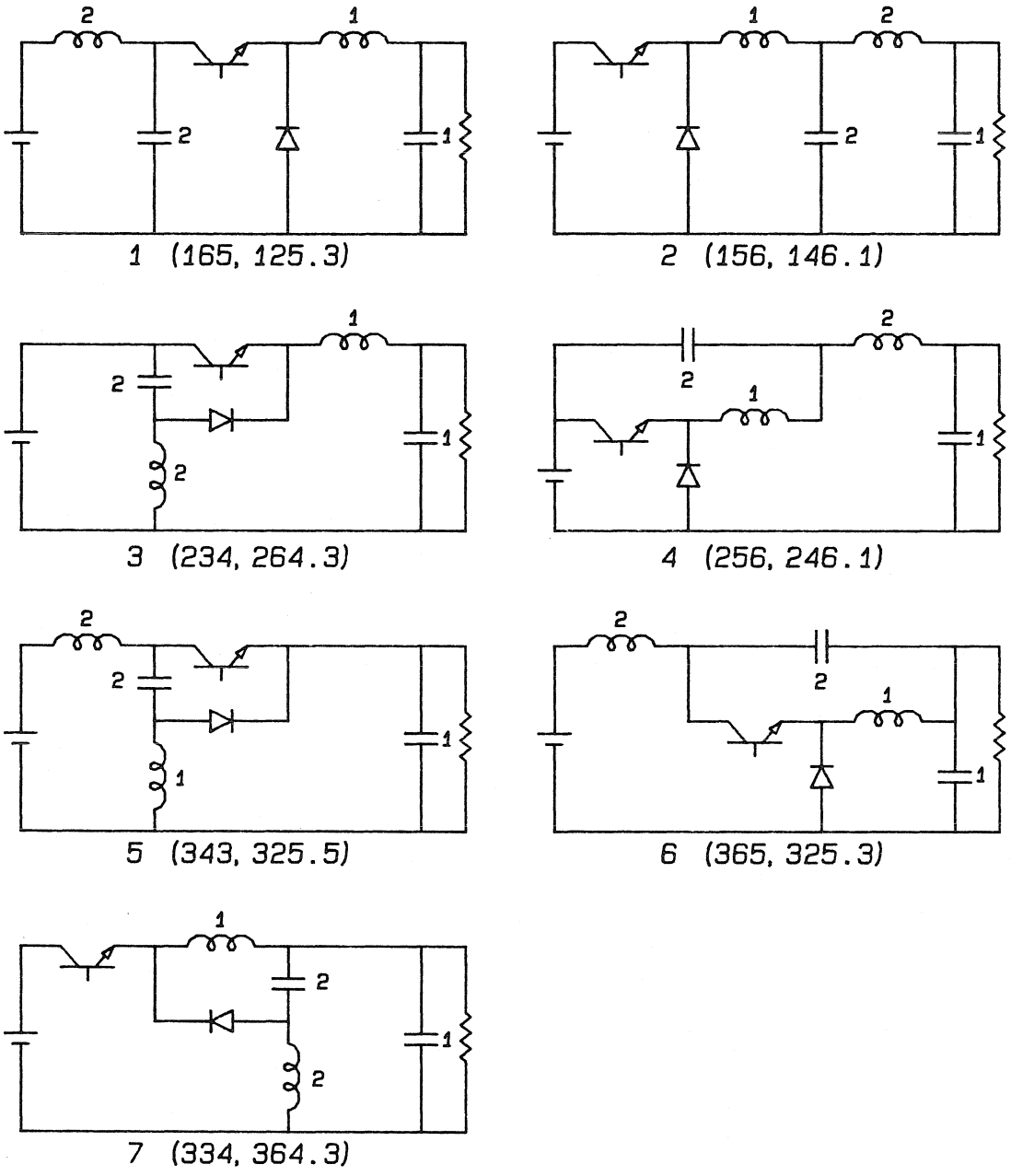


Figure 4.18: Fourth-order converters with $M(D) = D$.

#	P	I_{C_1rms}	I_{C_2rms}	I_{grms}	I_{L_1}	I_{L_2}	I	O	C
1	+	0	$\sqrt{M-1}$	M	M	1	$\surd$	$\surd$	–
2	+	$\sqrt{M-1}$	0	M	M	M	$\surd$	–	–
3	+	0	$\sqrt{M-1}$	M	M	$M-1$	$\surd$	$\surd$	–
4	+	$\sqrt{M-1}$	0	M	M	M	$\surd$	–	–
5	+	0	$\sqrt{M-1}$	M	$M-1$	1	$\surd$	$\surd$	$\surd$
6	+	0	$\sqrt{M-1}$	$\sqrt{M^2+M-1}$	M	1	–	$\surd$	–
7	+	$\sqrt{M-1}$	$\sqrt{M-1}$	$\sqrt{M^2+M-1}$	M	$M-1$	–	–	–

Table 4.7: Comparison of fourth-order, two-switch, step-up converters.

in the comparison table is zero. Suppose that there is a small parasitic resistance (r_e) in series with each converter element. Everything else being the same, the most efficient topology is the one for which the sum $\sum r_e I_{erms}^2$ is minimal. Of course, particular values of parasitic resistances are required in order to make exact comparison. However, one can assume that parasitic resistances for both capacitors and V_g are equal to r_c ($r_c > 0$) and that both inductors have a series resistance equal to r_l ($r_l > 0$). Under this assumption, it follows that SD(5) is the most efficient topology. If, in addition, $r_l = r_c = r$, the power loss that is due to parasitic resistances of converter elements is shown in Fig. 4.15(a) as a function of the conversion ratio M. The power loss is normalized to rI_{out}^2.

Topology SD(5) features continuous input and output currents and the possibility of coupling the inductors. Converters SD(1) and SD(3) have continuous input and output currents, too. Converters SD(1) and SD(2) are simply second-order buck converters with input or (additional) output filtering.

4.5.4 Fourth-Order, Two-Switch, Step-Up Converters

All step-up (SU) converters with $M(D) = 1/(1-D)$ can be obtained from SD converters by replacing the role of input and output terminals and transistor/diode switches. Voltage stress for switches is equal to $V_g/(1-D)$, while current stress is equal to $I_{out}/(1-D)$ for all converters. Table 4.7 contains the parameters for comparison of SU converters. SU converters are numbered in the same order as SD topologies from

#	P	I_{C_1rms}	I_{C_2rms}	I_{grms}	I_{L_1}	I_{L_2}	I	O	C
1	–	0	$\sqrt{\lvert M\rvert}$	$\lvert M\rvert$	$1+\lvert M\rvert$	1	√	√	–
2	–	$\sqrt{\lvert M\rvert}$	0	$\sqrt{\lvert M\rvert+M^2}$	$1+\lvert M\rvert$	$1+\lvert M\rvert$	–	–	–
3	–	0	$\sqrt{\lvert M\rvert}$	$\lvert M\rvert$	$1+\lvert M\rvert$	$\lvert M\rvert$	√	√	–
4	–	$\sqrt{\lvert M\rvert}$	0	$\sqrt{\lvert M\rvert+M^2}$	$1+\lvert M\rvert$	$1+\lvert M\rvert$	–	–	–
5	–	0	$\sqrt{\lvert M\rvert}$	$\lvert M\rvert$	$\lvert M\rvert$	1	√	√	√
6	–	0	$\sqrt{\lvert M\rvert}$	$\sqrt{\lvert M\rvert+M^2}$	$1+\lvert M\rvert$	1	–	√	–
7	–	$\sqrt{\lvert M\rvert}$	$\sqrt{\lvert M\rvert}$	$\lvert M\rvert$	$1+\lvert M\rvert$	$\lvert M\rvert$	√	–	–
8	+	$\sqrt{\lvert M\rvert}$	$\sqrt{\lvert M\rvert}$	$\lvert M\rvert$	$\lvert M\rvert$	1	√	–	√
9	+	0	$\sqrt{\lvert M\rvert}$	$\sqrt{\lvert M\rvert+M^2}$	1	$\lvert M\rvert$	–	√	√

Table 4.8: Comparison of fourth-order, two-switch, step-up/step-down converters.

which they originate.

4.5.5 Fourth-Order, Two-Switch, Step-Up/Step-Down Converters

There are nine strictly non-degenerate step-up/step-down (SUSD) converters with $|M(D)| = D/(1-D)$ (Fig. 4.14). Parameters for comparison are displayed in Table 4.8. Switch voltage and current stresses are the same as in SU converters. Converter SUSD(5) is the well-known Ćuk converter [5], SUSD(8) is the Sepic converter [4], while SUSD(9) is the inverse Sepic converter. The other converters in this class can be classified as buck-boost converters with additional filtering. Coupling of inductors is possible in SUSD(5, 8, 9), while converters SUSD(1, 3, 5) exhibit continuous input and output currents. All converters except SUSD(8,9) invert the voltage polarity.

Comparison of conduction losses in SUSD topologies, as functions of the conversion ratio M, is illustrated in Fig. 4.16. Losses are calculated relative to rI_{out}^2 in step-down and step-up regions, under the same assumption as for SD converters.

Experimental Verification

For experimental verification, same control circuit and same components are used to build nine SUSD converters. The first objective of the experiments is to confirm that

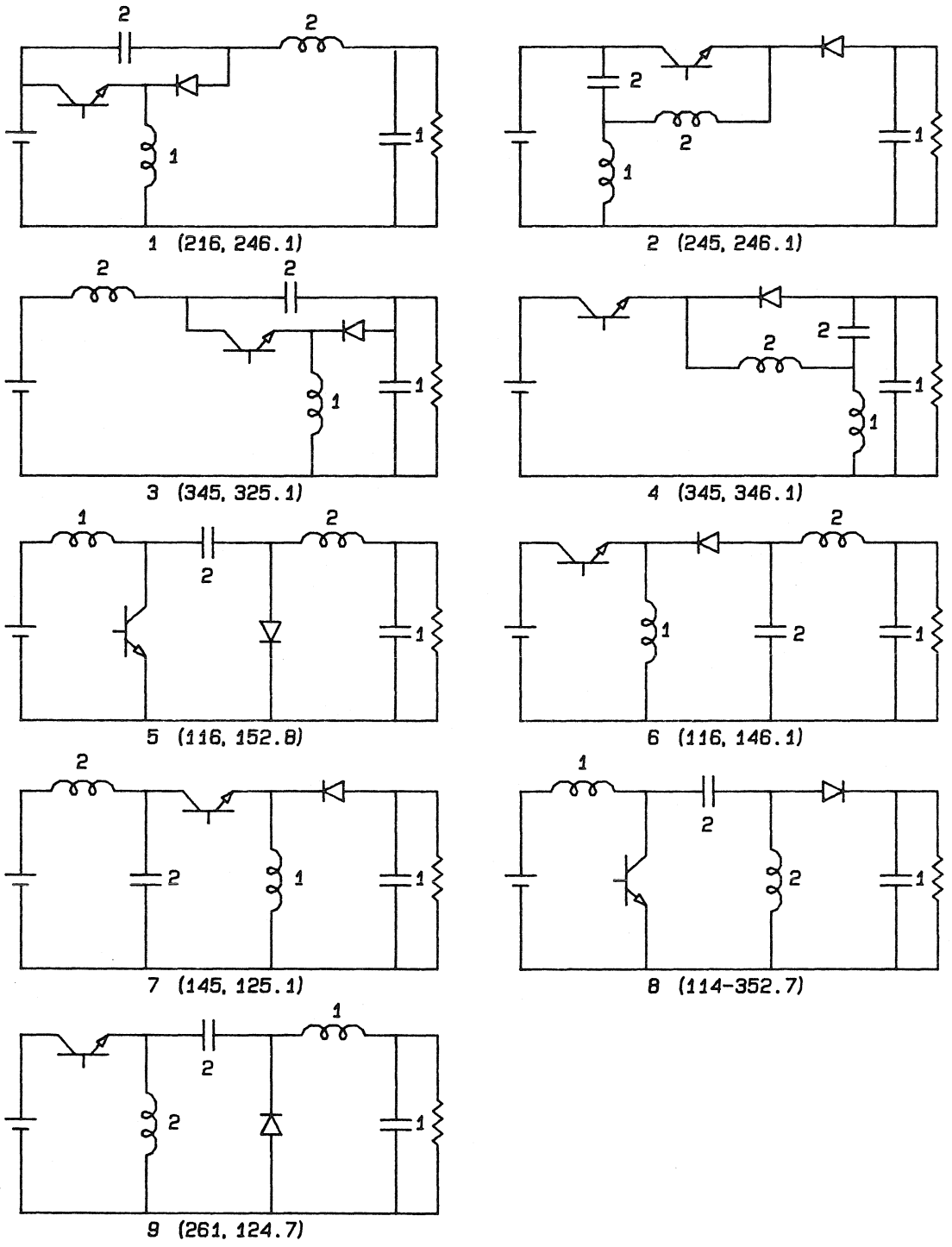


Figure 4.14: Fourth-order converters with $|M(D)| = D/(1-D)$.

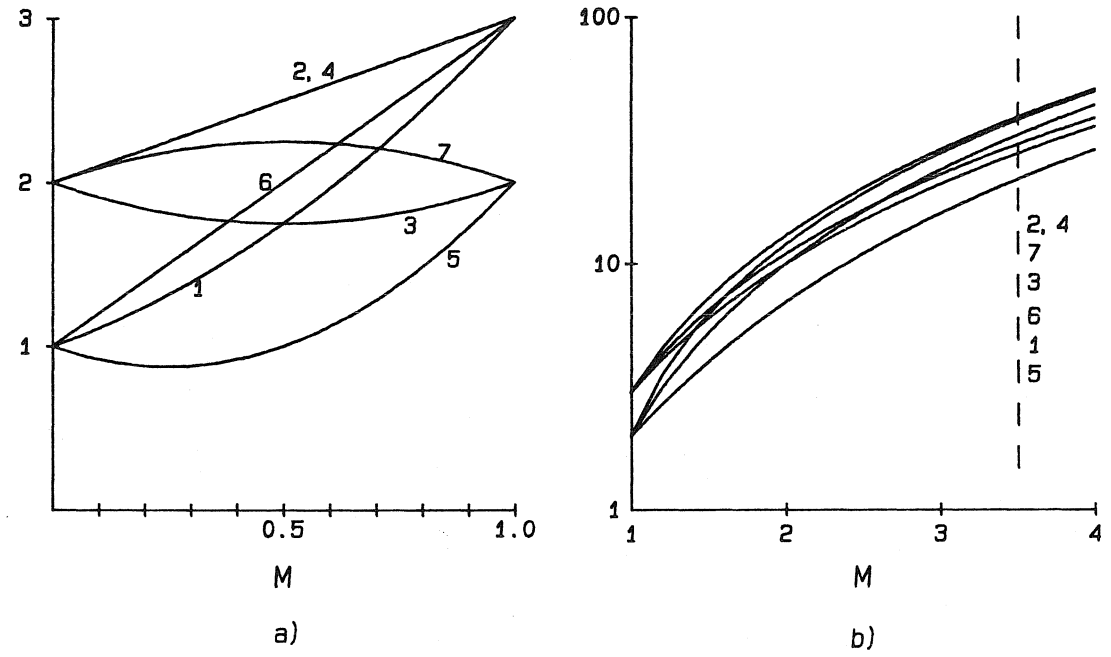


Figure 4.15: Power loss in SD converters (a) and SU converters (b), normalized to rI_{out}^2, where r is the parasitic series resistance of the elements in $\{V_g\} \cup \mathcal{C} \cup \mathcal{L}$.

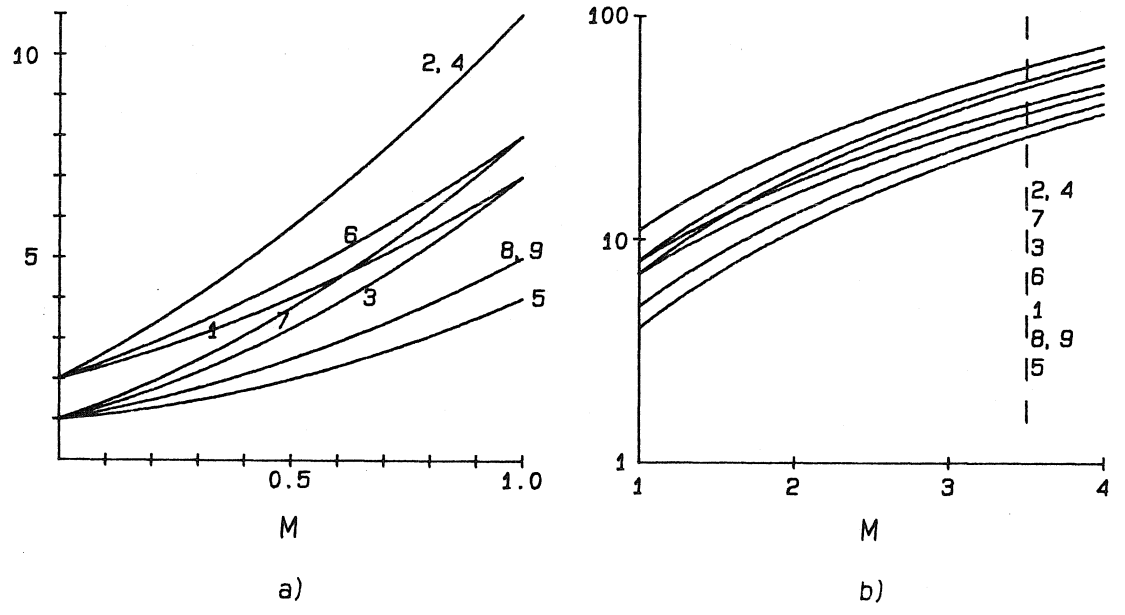


Figure 4.16: Power loss in SUSD converters operating as step-down (a) or as step-up (b), normalized to rI_{out}^2, where r is the parasitic series resistance of the elements in $\{V_g\} \cup \mathcal{C} \cup \mathcal{L}$.

all SUSD converters (some of which are not commonly utilized in practice) operate as expected. Another objective is to illustrate how conversion efficiency can be substantially different solely because of different interconnections among converter components.

Parameters of the experimental circuits are:

- source: $V_g = 10V$,
- inductors: $L = 500\mu H$, $r_l = 0.27\Omega$,
- capacitors: $C = 150\mu F$, $r_c = 0.15\Omega$,
- transistor: IRF540,
- diode: UES1303,
- switching frequency: $f_s = 100kHz$.

Efficiency is measured at two operating points, one in the step-down region and one in the step-up region. For each converter topology, V_{out} and I_{out} are kept constant by adjusting the duty ratio. Variations in conversion efficiency result in different currents drawn from the input source.

Results of the experiment shown in Table 4.9 indicate clearly how large differences in efficiency can be ascribed to the topology alone. As predicted, at both operating points, the Ćuk converter (SUSD(5)) is the most efficient topology. Positions of other topologies are also in agreement with plots in Fig. 4.16.

V_{out}	I_{out}	$\eta(1)$	$\eta(2)$	$\eta(3)$	$\eta(4)$	$\eta(5)$	$\eta(6)$	$\eta(7)$	$\eta(8)$	$\eta(9)$
$5V$	$1.2A$	67.3	58.8	70.3	58.7	76.4	67.0	69.8	75.1	74.5
$20V$	$0.4A$	81.6	78.0	80.2	77.7	83.6	81.3	80.4	83.2	83.5

Table 4.9: Measured efficiency $\eta(i)[\%]$ of the experimental step-up/step-down converters SUSD(1) through SUSD(9).

Since all two-switch 2L1C cells are represented in SUSD converters, experimental verification of the remaining two-switch, fourth-order converters is omitted.

4.5.6 Fourth-Order, Two-Switch Converters for DC/AC inversion

Out of 27 fourth-order converters with two switches, seven are step-down, seven are step-up and nine are step-up/step-down. The remaining four converters are shown in Fig. 4.17. A distinctive feature of these topologies is that the output voltage of either polarity can be obtained. DC conversion ratio,

$$M(D) = \begin{cases} \frac{1-2D}{1-D} & \text{for 1 and 3} \\ \frac{1-D}{1-2D} & \text{for 2 and 4} \end{cases}, \tag{4.16}$$

changes polarity at $D = 0.5$, so that DC-to-AC inversion can be achieved by varying the duty ratio. It should be noted, however, that for converters 2 and 4 the conversion ratio $M(D)$ is not defined at $D = 0.5$, indicating that the actual conversion ratio in the vicinity of $D = 0.5$ depends largely on the lossy parasitic elements that are not encompassed by the ideal DC model. Therefore, converters 2 and 4 are of less practical interest.

Converters 1 and 3 require current-bidirectional switches, while 2 and 4 require voltage-bidirectional switches. In all four cases, coupling of inductors is possible. Voltage and current stresses on the switches are equal in converters 1 and 3. A major advantage of the converter 1 is that its output current is continuous. Furthermore, AC ripple of the output current can be reduced ideally to zero by proper coupling of inductors.

4.5.7 Single-Transistor Converters with $M(D) = D^2$

Because of the finite switching speed and finite lengths of switching transitions, a transistor switch in a practical PWM converter cannot operate with ON-time less than a certain minimum. Minimum ON-time results in a minimum possible duty ratio and consequently in a minimum attainable conversion ratio. Clearly, the lower limit for the attainable conversion ratio increases with switching frequency. This is why a DC conversion ratio $M(D) = D^2$ can be useful in applications where large step-down ratio is required without a step-down transformer.

A fourth-order converter that achieves the conversion ratio $M(D) = D^2$ can be constructed in a straightforward manner by cascading two second-order, step-down (buck) converters [2]. Two transistor switches are required in the cascade converter. The synthesis procedure is used to search for single-transistor topologies with the same DC

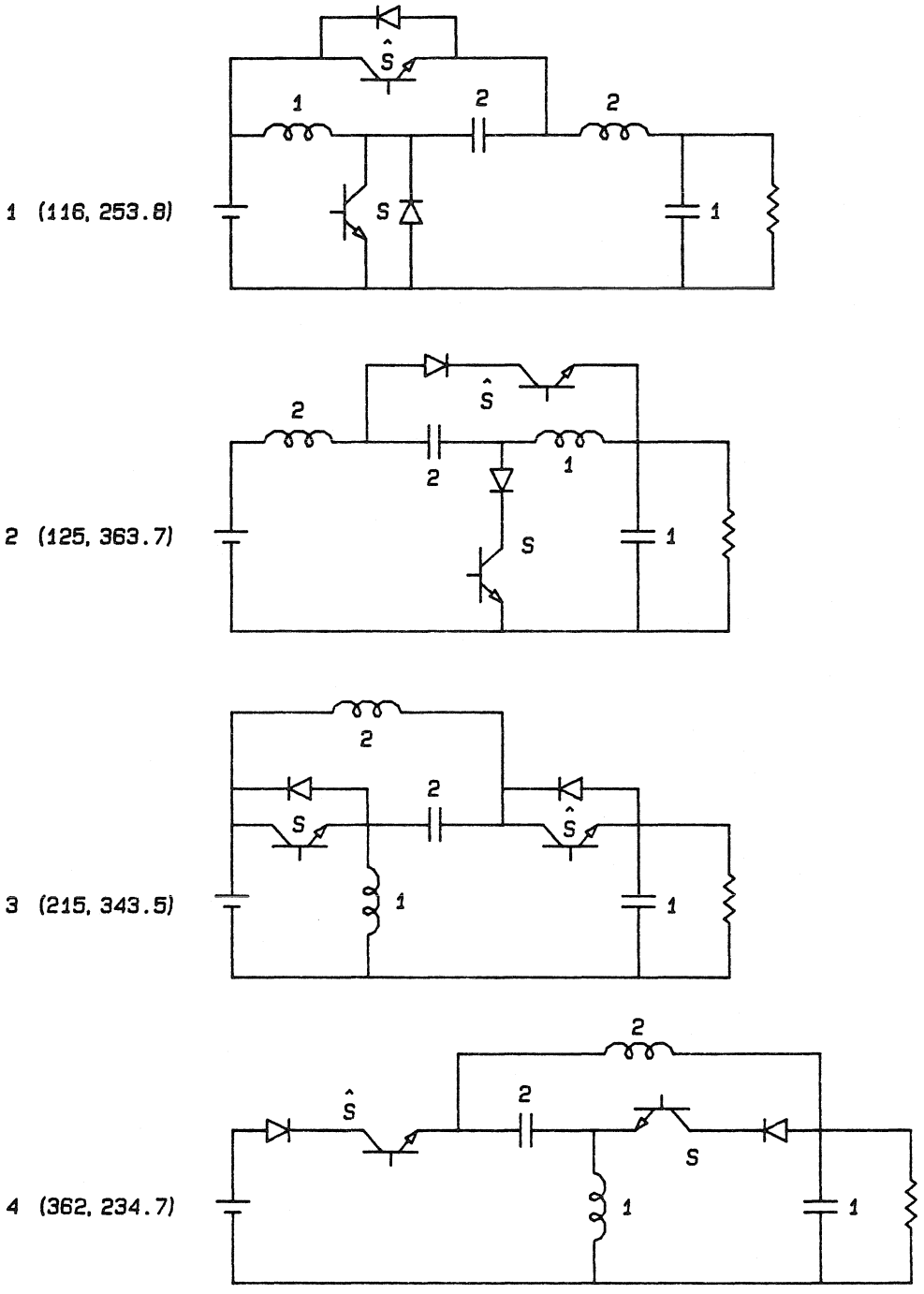
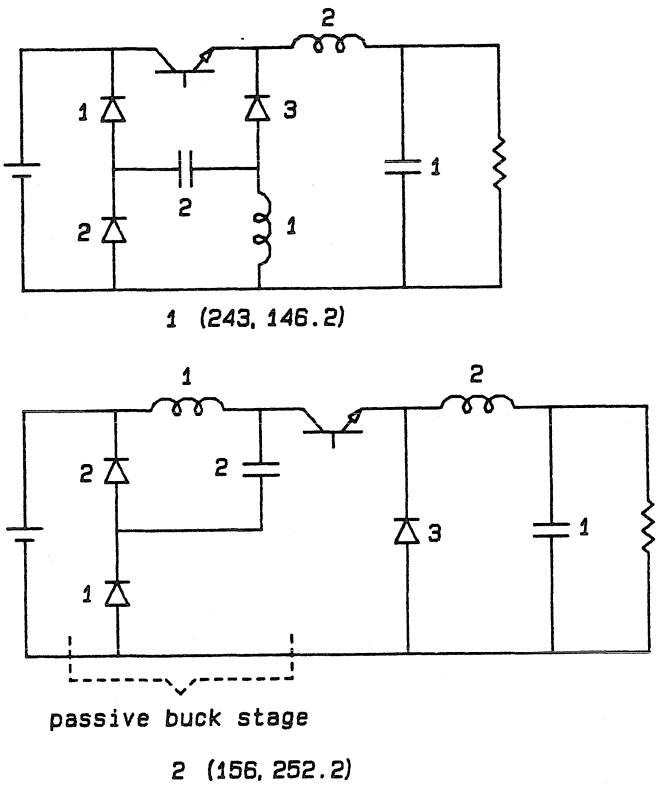


Figure 4.17: Fourth-order, two-switch converters suitable for DC-to-AC inversion.



	1	2
P	+	
V_{tpeak}	$1+D$	
I_{trms}	$\sqrt{D}$	
V_{d1peak}	1	
$\overline{I}_{d1}$	$D(1-D)$	
V_{d2peak}	1	
$\overline{I}_{d2}$	$D(1-D)$	
V_{d3peak}	D	
$\overline{I}_{d3}$	$1-D$	
I_{C_1rms}	0	
I_{C_2rms}	$\sqrt{D(1-D)}$	
I_{grms}	$D\sqrt{D}$	
I_{L_1rms}	$1-D$	D
I_{L_2rms}	1	
I	–	
O	$\surd$	
C	–	

Figure 4.18: Single-transistor converters with $M(D) = D^2$.

conversion ratio. Two step-down/step-down (SD^2) topologies are found and shown in Fig. 4.18 together with parameters relevant for comparison.

In both converters, transistor and diode D_1 conduct simultaneously. When the transistor switch is ON, diode D_1 provides a path for the L_1 inductor current in $SD^2(1)$, while in $SD^2(2)$, D_1 conducts the current $I_2 - I_1 = 1 - D$.

Parameters for the two topologies are the same except for the inductor L_1 current. In applications that require a large step-down ratio, it is more likely that the steady-state duty ratio is less than 0.5 so that $SD^2(2)$ is a better choice with respect to conduction losses.

It is interesting to note that converter $SD^2(2)$ can be regarded as a cascade of a passive buck (L_1, C_2, D_1, D_2) and an active buck $(L_2, C_1, transistor, D_3)$ stage. Switching inside the passive buck stage is enforced by the input current of the active stage. Therefore, the passive buck can precede *any* converter with pulsating input current, multiplying its conversion ratio by D. Moreover, since the passive buck itself has pulsating input current, $n-1$ passive buck stages can be cascaded in a row with a single, active buck stage to obtain a single-transistor converter with $M(D) = D^n$.

4.5.8 Single-Transistor Converters with $M(D) = 1/(1-D)^2$

Four single-transistor step-up/step-up (SU^2) converters with $M(D) = 1/(1-D)^2$ are found by the synthesis procedure. The converters are shown in Fig. 4.19. Note that S-switches (transistor and diode D_1) form a path of length two in topologies $SU^2(1,3,4)$. In these three cases, the position of switches is not unique, as discussed in Section 4.4.4. Two transistors are required in the two remaining topological variations. Voltage and current stresses for all switching devices are the same in all four converters. Converters $SU^2(1,4)$ have continuous input currents, while all converters have pulsating output currents. In particular, the rms current for the output capacitor of $SU^2(4)$ is larger than in other topologies since the output current in this converter attains both positive and negative values. Thus, with respect to conduction losses on parasitic resistances, $SU^2(1)$ is the preferred choice. Since transistor voltage stress is equal to the output voltage, no advantage over a single SU converter is achieved.

Converters $SU^2(1)$ and $SU^2(4)$ are dual to converters $SD^2(1)$ and $SD^2(2)$, respectively. Two sixth-order converters with $M(D) = D^2$ are dual to $SU^2(2,3)$ converters.

The final remark is that the $SU^2(1,2,3)$ converters can be regarded as modifications of the basic second-order boost stage. Proceeding in the same manner, it is possible to construct single-transistor converters with $M(D) = 1/(1-D)^n$.

4.5.9 Single-Transistor Converters with $|M(D)| = D^2/(1-D)$

Converters in this class are suitable for applications where an extremely large *range* of conversion ratios is required. D^2 in the numerator extends the range for low duty ratios,

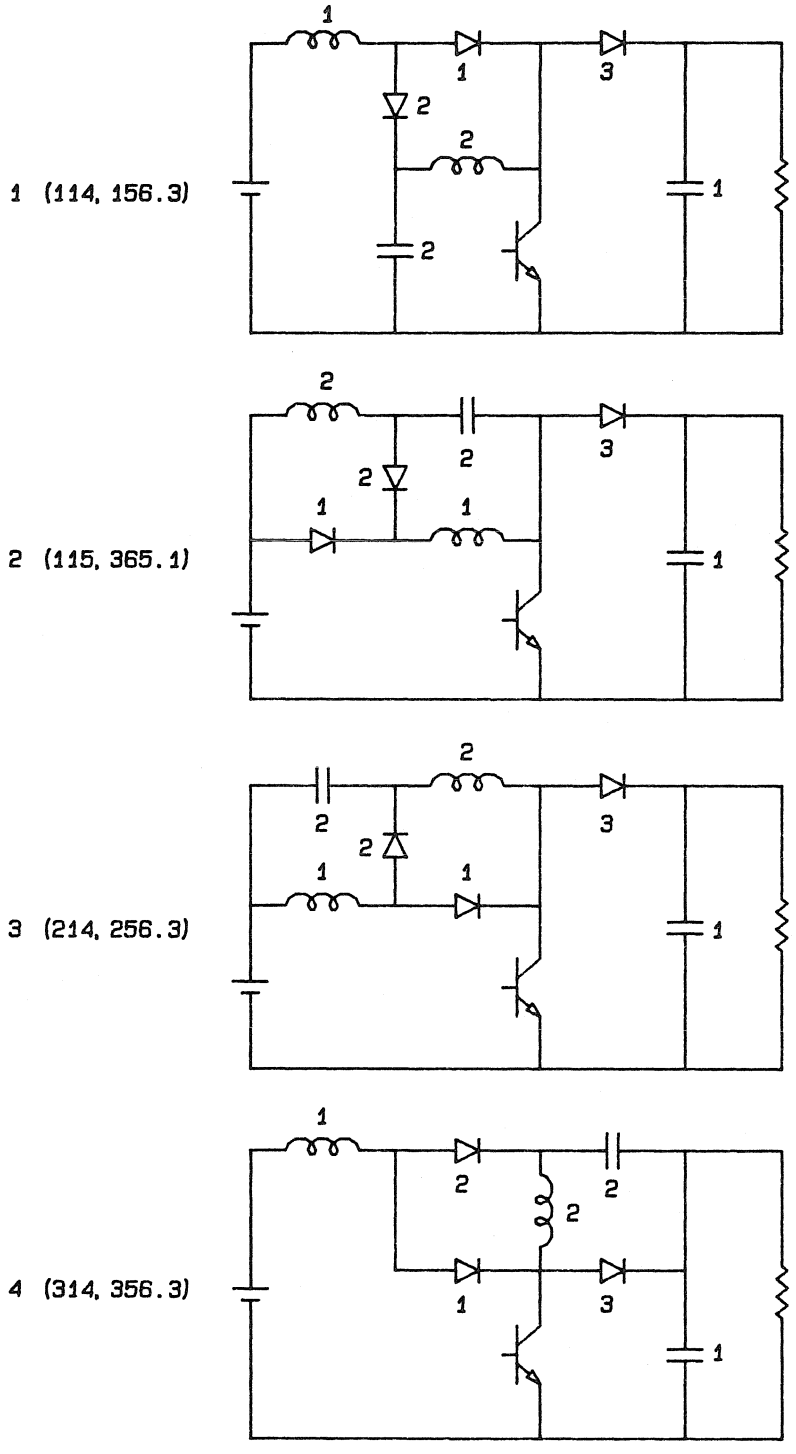


Figure 4.19: Single-transistor converters with $M(D) = 1/(1-D)^2$.

where it is limited by the minimum ON-time of the transistor switch, while $1 - D$ in the denominator still provides step-up function at higher duty ratios. Three converters in this class are shown in Fig. 4.20.

Most of the parameters are the same for all three SD^2SU topologies. Converters $SD^2SU(1,3)$ have continuous output currents. Converter $SD^2SU(1)$ has the lowest sum of inductor currents and the lowest sum of average diode currents. Thus, it represents the most favorable choice with respect to conduction losses. On the contrary, voltage stress for diode D_2 is largest in $SD^2SU(1)$. In all three topologies, transistor and diode D_1 are the S-switches.

4.5.10 Single-Transistor Converters with $|M(D)| = D^2/(1-D)^2$

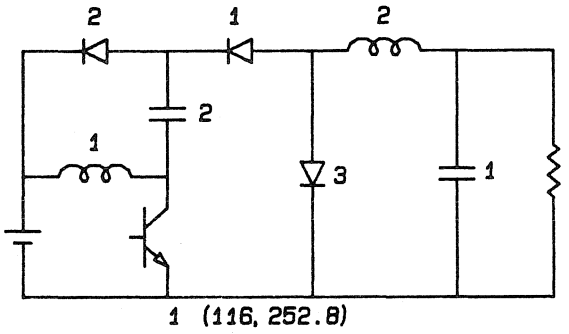
Among fourth-order converters, the potential range of DC conversion ratios is largest if $M(D) = D^2/(1-D)^2$. The only single-transistor converter that offers this conversion ratio is shown in Fig. 4.21. Unfortunately, the converter operates properly only for $D \leq 0.5$. For $D > 0.5$, diodes D_1 and D_2 clamp the output voltage to V_g so that step-up function is not possible.

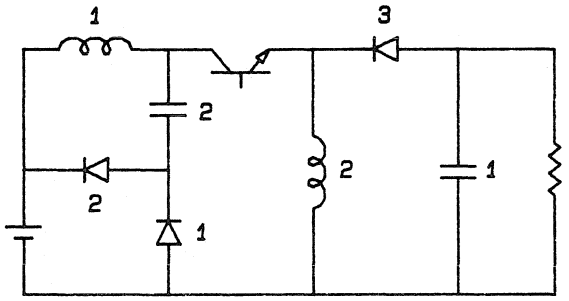
4.5.11 Single-Transistor Converters with Conversion Ratios of Degree Two: Experimental Verification

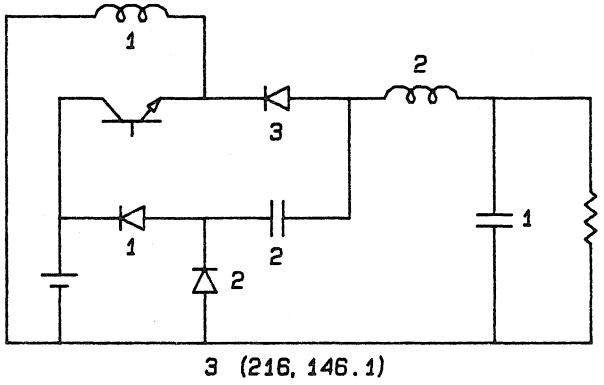
Experimental converters are built using the same control circuit and the same set of components. Parameters of the experimental circuits are:

- inductors: $L = 280\mu H$, $r_l = 0.06\Omega$,
- capacitors: $C = 150\mu F$, $r_c = 0.15\Omega$,
- transistor: IRF540,
- diodes: UES1303,
- switching frequency: $f_s = 100kHz$.

It is verified that experimental converters exhibit predicted conversion ratios. Moreover, as in the experimental verification of SUSD converters, efficiency is compared at specific operating points.







	1	2	3
P	–		
V_{tpeak}	$\frac{1}{1-D}$		
I_{trms}	$\frac{\sqrt{D}}{1-D}$		
V_{d1peak}	1		
$\overline{I}_{d1}$	D		
V_{d2peak}	$\frac{1}{1-D}$	1	1
$\overline{I}_{d2}$	D		
V_{d3peak}	$\frac{D}{1-D}$		
$\overline{I}_{d3}$	$1-D$	1	1
I_{C_1rms}	0	$\sqrt{\frac{D}{1-D}}$	0
I_{C_2rms}	$\sqrt{\frac{D}{1-D}}$		
I_{grms}	$\frac{D\sqrt{D}}{1-D}$		
I_{L_1rms}	$\frac{D}{1-D}$	$\frac{D}{1-D}$	$\frac{1}{1-D}$
I_{L_2rms}	1	$\frac{1}{1-D}$	1
I	–		
O	√	–	√
C	–		

Figure 4.20: Single-transistor converters with $|M(D)| = D^2/(1-D)$.

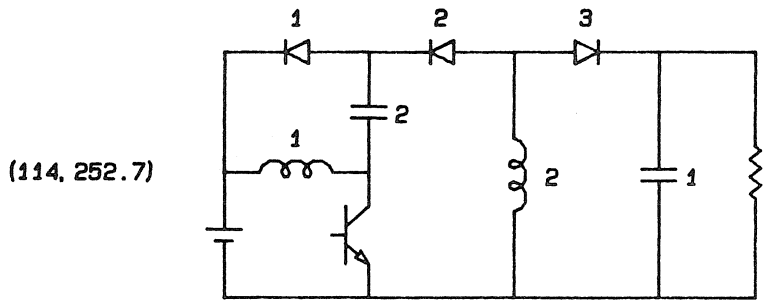


Figure 4.21: A single-transistor converter with $M(D) = D^2/(1-D)^2$.

			SD^2		SD^2SU		
V_g	V_{out}	I_{out}	$\eta(1)$	$\eta(2)$	$\eta(1)$	$\eta(2)$	$\eta(3)$
$50V$	$5V$	$2.3A$	70.8	71.3	66.2	62.5	62.9

Table 4.10: Measured efficiency of the experimental SD^2 and SD^2SU converters.

Results of the measurements for SD^2 and SD^2SU converters are shown in Table 4.10. An operating point with large step-down ratio is chosen to emulate conditions in a possible, practical application. As predicted, $SD^2(2)$ is more efficient than $SD^2(1)$, and $SD^2SU(1)$ is the most efficient converter among SD^2SU topologies. SD^2 converters are more efficient than SD^2SU converters, as could have been inferred from the comparison tables. Results for SU^2 converters, in Table 4.11, confirm the prediction that $SU^2(1)$ is the most favorable choice with respect to conduction losses, although deviations may be considered marginal.

V_g	V_{out}	I_{out}	$\eta(1)$	$\eta(2)$	$\eta(3)$	$\eta(4)$
$5V$	$25V$	$0.13A$	74.9	74.0	74.1	74.6

Table 4.11: Measured efficiency of experimental SU^2 converters.

Chapter 5

Extensions of PWM Converter Topologies

In Chapters 3 and 4 several restrictions are imposed on the structure and the operating mode of a PWM DC-to-DC converter. Isolation transformers are excluded, and a unique operating mode is postulated by Definition 3.1. Furthermore, the DC model of PWM converters is established under the small-ripple assumption. Finally, the scope of the synthesis procedure in Chapter 4 is limited to converters with a common input and output terminal and with a single filtering capacitor across the load.

In this chapter, the restrictions are removed to the extent that can be justified from a practical point of view. A sufficient condition for the possibility of inserting an isolation transformer in a PWM converter is found in Section 5.1. In Section 5.2, it is shown how selective removal of the small-ripple assumption results in two additional operating modes of PWM converters, namely, discontinuous inductor current mode (DICM) and discontinuous capacitor voltage mode (DCVM). Both modes are known and corresponding DC analyses are published for selected PWM converters [23,26]. An original contribution of Section 5.2 is that DC analysis of discontinuous modes is unified for *all* two-switch PWM converters of arbitrary order.

Construction of converters with a floating load is discussed in Section 5.3. A transformation that puts the load in a loop with more than one filtering capacitor is proposed in Section 5.4.

5.1 Insertion of Isolation Transformers

Isolation transformers are commonly used in DC-to-DC converters for several reasons. The transformer provides galvanic isolation, which is mandatory in DC-to-DC converters supplied directly from the rectified utility line ("off line"). Furthermore, the

transformer's primary-to-secondary turns-ratio multiplies the original DC conversion ratio, thus providing an additional step-down or step-up. Either polarity of the output voltage is available simply by selecting the reference end of the secondary winding. Finally, an isolation transformer with multiple secondary windings can be used to construct DC-to-DC converters with multiple outputs.

In this section, insertion of an isolation transformer is treated as an extension of a PWM converter topology. Usually, it is intuitively clear whether or not insertion of a transformer is possible. However, a formalized transformer insertion procedure is needed, not only as a practical tool, but also to clarify how operation of the isolation transformer is related to the converter topology.

Three types of transformers are encountered in switched-mode converters. In a *true AC* transformer there is no DC bias, and the AC flux swing is symmetrical around the origin. Energy is transferred during the entire switching cycle. Hence, a true AC transformer yields the highest possible utilization of its magnetic core. In a *forward* transformer, energy is transferred during only one part of the switching cycle. During that part, flux in the core is excited from zero to some maximum value. The rest of the switching cycle is used to reset the flux back to zero. Finally, a pair of switched coupled inductors can also provide isolation. This type of transformer is called *flyback*. A flyback transformer, being electrically equivalent to a single inductor, operates with an AC flux centered around some DC bias.

Converters in which DC isolation can be achieved using a single transformer are of prime interest. The following proposition gives a sufficient condition for insertion of an isolation transformer while the insertion procedure is detailed in the proof.

Proposition 5.1 *Starting with a PWM converter network N, construct a new network N_x by shorting an inductor L_x, by removing a capacitor C_x or by removing a switch S_x. Insertion of a (perfect) transformer is possible if there exists an element (L_x, C_x or S_x) such that graph G_x corresponding to the network N_x is separable and if there is no loop in N_x containing both source V_g and load R.*

Proof: insertion of an isolation transformer can be demonstrated in three different cases. In each case, we show that operation of the converter with a (perfect) transformer is not

altered.

Case 1: Suppose that after shorting an inductor L_x in the converter network N, the resulting network N_x has a separable graph. Then, a flyback isolation transformer can be inserted as shown in Fig. 5.1. Assuming that the isolation transformer is perfect and with 1:1 turns-ratio, voltages and currents at terminals 1'-2' and 1"-2" are unaltered. Therefore, all voltage and current waveforms in the circuit and consequently the DC conversion ratio are the same as without the transformer.

Case 2: Suppose that the graph of the network N_x is separable after capacitor C_x is removed from N. Then, a true AC isolation transformer can be inserted as shown in Fig. 5.2. Suppose that the isolation transformer is ideal with 1:1 turns-ratio. Voltages and currents at terminals 1'-2' and 1"-2" are not affected so that there is no change in operation of the circuit. If, however, the transformer is perfect, additional magnetizing current flows through the transformer windings. Under the small-ripple assumption, the magnetizing current amounts to a negligible AC ripple. Note that the order of the converter network is increased by two.

Case 3: If removal of a switch S_x results in the network N_x with a separable graph, a forward transformer can be inserted as shown in Fig. 5.3. If the DC voltage across the terminals 1'-2' (or 1"-2") in Fig. 5.3 is zero, there is, or there can be, an inductor placed between the terminals. However, this inductor would satisfy the conditions for Case 1, and a flyback isolation transformer could be inserted instead of the forward transformer. Assuming that DC voltages across terminals 1'-2' and 1"-2" are not equal to zero, an additional switch is necessary for insertion of the forward transformer. Switches S_x' and S_x'' are turned ON and OFF simultaneously. If the transformer is ideal, equivalence between terminal waveforms in the new converter and in the original converter is trivial. Suppose that the transformer is perfect. With both switches in the ON position, either primary or secondary (but not both) is in a loop with a set of capacitors and possibly V_g. If this was not the case, in one of the switched networks there would be an inductor-only cut-set or a capacitor-only loop, which is not possible by Assumption A3 of Definition 3.1. Suppose, without loss of generality, that the primary is in a loop with capacitors and possibly V_g, while the secondary is in a cut-set with inductors when S_x' and S_x'' are

ON. Energy is transferred through the transformer and at the same time the core flux density increases from zero to some maximum value. Under the small-ripple assumption, the magnetizing current is negligible. When the switches are OFF, there is no energy transfer, and a path for the magnetizing current has to be provided in order to reset the core flux to zero. The circuit for resetting the core is implicit in Fig. 5.3. The order of the converter network is increased by one. $\lhd$

If the switch S_x in Fig. 5.3 is implemented as a transistor or as a diode, implementation of the switch S_x' is the same except in the case when the diode would provide a DC path that shorts the source. Consider, for example, $SU^2(1,2,3)$ converters in Fig. 4.19. In all three cases, diode D_3 satisfies the condition for insertion of a forward transformer. However, S_x' has to be implemented as a transistor. Switch S_x'' can be implemented as a diode.

Conditions of Proposition 5.1 are not always necessary for insertion of an isolation transformer. Consider a PWM converter to which an inductor can be added without disturbing its DC conversion properties. In fact, an inductor can always be added in parallel with any existing inductor or, more generally, in a loop with existing inductors. Since n_l becomes larger than n_c, the steady-state solution for the converter states (assuming that it exists) is not unique. Nevertheless, the converter may still have a unique steady-state solution for the output DC voltage. If the added inductor satisfies conditions of Proposition 5.1, a flyback transformer can be inserted as in Case 1. For example, a flyback isolation transformer can be inserted in the converter SUSD(6) of Fig. 4.14, as illustrated in Fig. 5.4, although conditions of Proposition 5.1 are not satisfied.

5.2 Discontinuous Operating Modes

Under the small-ripple assumption, all capacitor voltages and inductor currents in a PWM converter are essentially DC quantities. For converters with one switch implemented as a transistor and the other switch implemented as a diode, this implies that the stress voltage V_{off} and the stress current I_{on} are also DC quantities and that the diode switch conducts current I_{on} throughout the period $(1-D)T_p$. The operating mode in which the transistor and the diode are never ON or OFF simultaneously is usu-

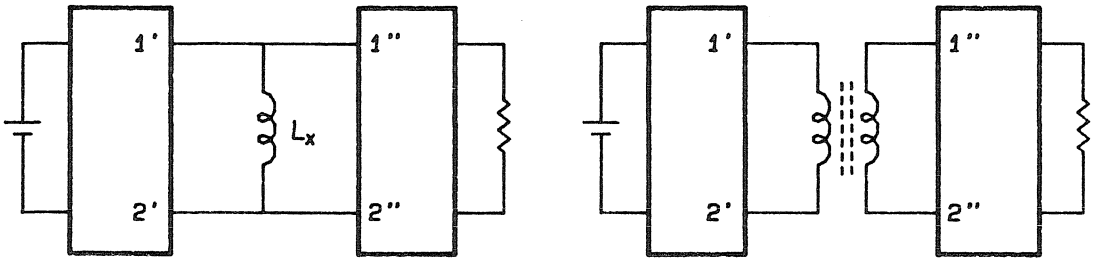


Figure 5.1: Insertion of a flyback transformer.

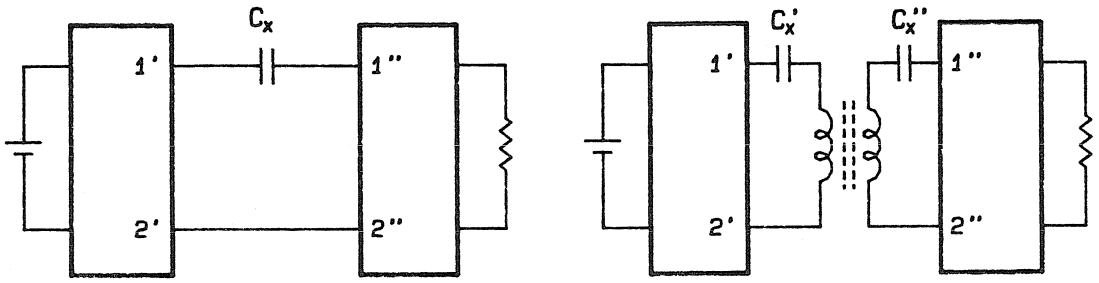


Figure 5.2: Insertion of a true AC isolation transformer.

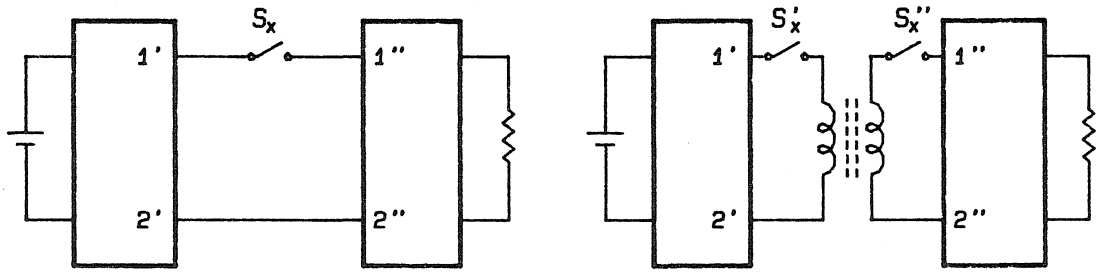


Figure 5.3: Insertion of a forward transformer.

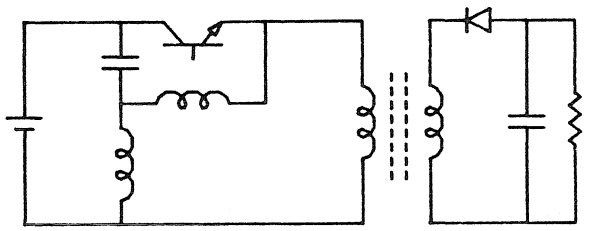


Figure 5.4: Flyback isolation transformer in the SUSD(6) converter.

ally called the *continuous conduction mode* (CCM). This operating mode is assumed by Definition 3.1.

In this section, we consider two different cases when the small-ripple assumption is removed in a two-switch PWM converter with one transistor and one diode. In the first case, the assumption is imposed on all capacitors, while it is removed from an inductor (or inductors) in $\mathcal{L}_{on}$. Recall that inductors in $\mathcal{L}_{on}$ carry currents that contribute to I_{on}. The mode of operation, called the *discontinuous inductor current mode* (DICM) [23,26], results from the fact that the AC current ripple in i_{on} is not negligible compared to the average value I_{on}. The DC conversion ratio and conditions at the boundary between DICM and CCM modes are found in Section 5.2.1. The analysis is unified for PWM converters with one transistor, one diode and an arbitrary number of reactances.

The second case is dual to the first case – the small-ripple assumption is retained for all inductors, while it is abandoned for a capacitor (or capacitors) in $\mathcal{C}_{off}$. By definition, capacitors in $\mathcal{C}_{off}$ carry voltages which contribute to V_{off}. The operating mode that results from the fact that the AC ripple in v_{off} is not negligible compared to the average value V_{off} is called the *discontinuous capacitor voltage mode* (DCVM) [26]. In Section 5.2.2 unified results for DCVM are obtained directly from the results for DICM by applying the duality principle.

The two discontinuous modes (DICM and DCVM) are found by removing the small-ripple assumption from inductors in $\mathcal{L}_{on}$ *or* from capacitors in $\mathcal{C}_{off}$. It is quite natural to ask what operating mode would result if the small-ripple assumption is removed from inductors in $\mathcal{L}_{on}$ *and* capacitors in $\mathcal{C}_{off}$, simultaneously. The answer to this question

is postponed until Chapter 6 where it is shown that this previously neglected mode of operation of PWM converters can be viewed as an operating mode of a class of Quasi-Resonant converters. The corresponding unified DC analysis is presented in Chapter 7.

5.2.1 Discontinuous Inductor Current Mode

Operation in the discontinuous inductor current mode is recognized by the fact that the diode switch ceases to conduct before the end of a switching cycle. By Proposition 3.8, inductors in $\mathcal{L}_{on}$ sustain identical voltage waveforms. During the period D_cT_p, while the transistor switch is ON, voltage across every inductor in $\mathcal{L}_{on}$ is equal to $V_{off} - \overline{v}_d$. Note that control-variable D_c is defined in the same manner as the duty ratio D for PWM converters in the continuous conduction mode. When the transistor switch is OFF, voltage across every inductor in $\mathcal{L}_{on}$ is $-\overline{v}_d$, as long as the diode current is positive. Assuming that the diode ceases to conduct before the end of the switching period, we have

$$L_e \frac{di_{on}}{dt} = V_{off} - \overline{v}_d\,, \quad 0 < t \leq D_cT_p\,, \tag{5.1}$$

$$L_e \frac{di_{on}}{dt} = -\overline{v}_d\,, \quad DT_p < t \leq D_1T_p\,, \tag{5.2}$$

$$i_{on} = 0\,, \quad D_1T_p < t < T_p\,. \tag{5.3}$$

Equivalent inductance L_e is inductance of the parallel combination of inductors in $\mathcal{L}_{on}$,

$$\frac{1}{L_e} \equiv \sum_{\mathcal{L}_{on}} \frac{1}{L_i}\,. \tag{5.4}$$

A typical waveform of the current i_{on} in DICM is depicted in Fig. 5.5. DICM is described by the following periodic sequence of states:

$$\text{DICM: } \cdots \rightarrow \boxed{\text{ON-OFF}} \rightarrow \boxed{\text{OFF-ON}} \rightarrow \boxed{\text{OFF-OFF}} \rightarrow \cdots\,, \tag{5.5}$$

In each state, positions of the S-switch (transistor) and the $\hat{S}$-switch (diode) are indicated. Unified DC analysis of converters operating in DCIM is based on the general approach outlined in Section 3.6. The condition that the converter network in DICM is identical to the network of some two-switch PWM parent at DC is trivially satisfied since the converter topology is not changed at all. We seek the equivalent duty ratio m ($m \equiv \overline{v}_d/V_{off}$) as a function of the control variable D_c and the ratio V_g/I_{out}.

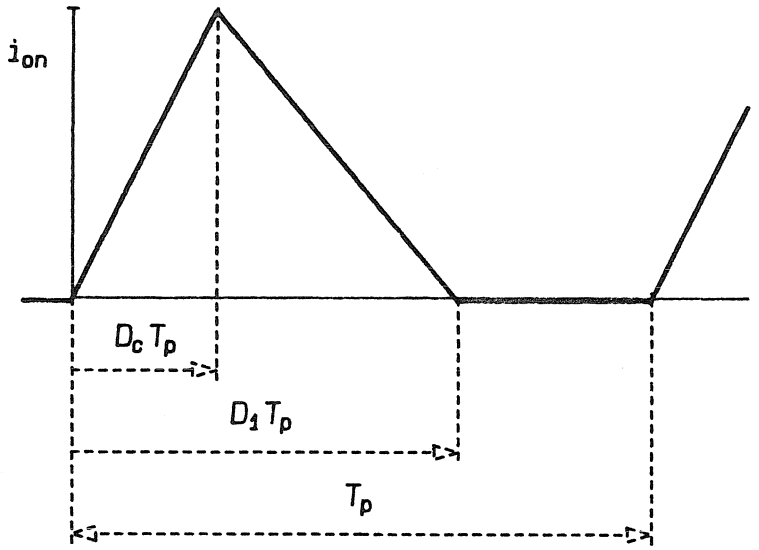


Figure 5.5: Typical waveform of the current i_{on} in the discontinuous inductor current mode.

If the average of i_{on} is evaluated over one switching cycle, we get

$$\bar{i}_{on} = I_{on} = \frac{1}{2}\frac{V_{off} - \overline{v}_d}{L_e} D_c D_1 T_p \,. \tag{5.6}$$

The average voltage across every inductor has to be zero in steady state. Therefore,

$$D_c V_{off} = D_1 \overline{v}_d \,. \tag{5.7}$$

Using the fact that $V_{off}/I_{on} = V_g/I_{out}$, Eqs. (5.6) and (5.7) can be solved for the equivalent duty ratio m,

$$m = \frac{D_c^2}{\frac{I_{out}}{I_\alpha} + D_c^2} \,, \tag{5.8}$$

where

$$I_\alpha \equiv \frac{V_g}{2 L_e f_s} \,. \tag{5.9}$$

The expression for m is valid for any two-switch PWM parent converter. The conversion ratio in DICM is equal to $M(m)$ where $M(\cdot)$ is the function inherited from the parent PWM converter with DC conversion ratio $M(D)$ in CCM.

An alternative general expression for the DC conversion ratio,

$$D_c = \sqrt{\frac{k_\alpha M D(M)}{1 - D(M)}} \,, \tag{5.10}$$

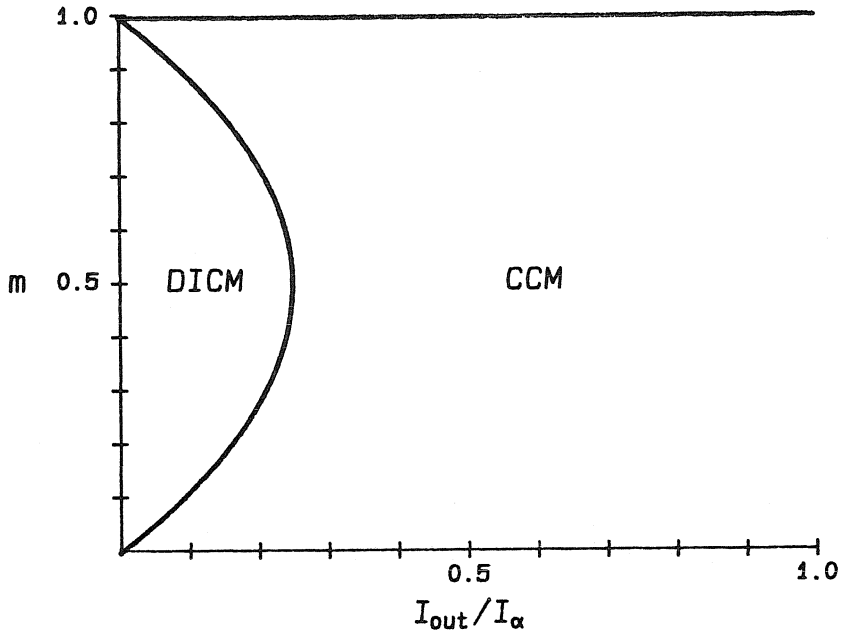


Figure 5.6: The DICM/CCM operating regions for two-switch PWM converters.

follows from the fact that $V_g/I_{out} = R/M$. Here, R is the load resistance at DC, $R \equiv V_{out}/I_{out}$, while $D(M)$ is the inverse of the function $M(D)$ for the parent PWM converter. Parameter k_α lumps together all relevant circuit parameters,

$$k_\alpha \equiv \frac{2L_e f_s}{R}. \tag{5.11}$$

The DC characteristic given by Eq. (5.10) is in its inverse form – the control variable D_c is found as a function of the conversion ratio M. The explicit form, $M = M(D_c, k_\alpha)$, can be obtained by inverting Eq. (5.10) for any given $D(M)$.

Converters operate in DICM as long as $D_1 \leq 1$. In the load-to-output plane, the boundary curve between the DICM and CCM operating regions is found by noting that results for DICM and CCM must coincide at the boundary. By substituting $D_c = m$ in Eq. (5.8), we get the boundary curve,

$$\frac{I_{out}}{I_\alpha} = m(1-m). \tag{5.12}$$

The operating regions for DICM and CCM are shown in Fig. 5.6. The boundary condition can also be found in terms of the parameter k_α. Critical value $k_{\alpha c}$ at the boundary is

$$k_{\alpha c} = \frac{D_c(1-D_c)}{M(D_c)}, \tag{5.13}$$

$M(D)$	$D(M)$	conversion ratio in DICM	$k_{\alpha c}$
D	M	$D_c = \sqrt{\frac{k_\alpha M^2}{1-M}}$	$1 - D_c$
$\frac{D}{1-D}$	$\frac{M}{1+M}$	$D_c = \sqrt{k_\alpha} M$	$(1 - D_c)^2$
$\frac{1}{1-D}$	$\frac{M-1}{M}$	$D_c = \sqrt{k_\alpha M(M-1)}$	$D_c(1 - D_c)^2$
$\frac{2D-1}{D}$	$\frac{1}{2-M}$	$D_c = \sqrt{\frac{k_\alpha M}{1-M}}$	$\frac{D_c^2(1-D_c)}{2D_c-1}$
$\frac{D}{2D-1}$	$\frac{M}{2M-1}$	$D_c = \sqrt{\frac{k_\alpha M^2}{M-1}}$	$(1 - D_c)(2D_c - 1)$

Table 5.1: DC conversion properties of two-switch PWM converters operating in the discontinuous inductor current mode.

and operation in DICM is for $k_\alpha < k_{\alpha c}$. Since $k_\alpha \to 0$ as $R \to \infty$, any PWM converter enters DICM for sufficiently large load resistance R.

It is important to note that the conversion ratio in DCIM is the same for all PWM converters which share the same DC conversion ratio $M(D)$, regardless of the specific topology. In Table 5.1 the conversion ratio in DICM and critical value for $k_{\alpha c}$ are found for possible conversion ratios (in CCM) of degree one. It can be verified that entries in the first three rows of Table 5.1 agree with the results previously found for specific PWM converters in [23].

Current-Bidirectional Converters

The discontinuous inductor current mode is a consequence of the fact that the diode is a current-unidirectional switch. If the $\hat{S}$-switch is implemented as a current-bidirectional switch, the continuous conduction mode is maintained for any output current for which $V_{out} I_{out} \geq 0$. If, in addition, both switches are implemented as current bidirectional, the operating region in the continuous conduction mode includes the quadrant $V_{out} I_{out} < 0$. In other words, power can be transferred from the source to the load and vice versa. Current-bidirectional (two-quadrant) PWM converters are utilized in applications such as battery chargers/dischargers [7].

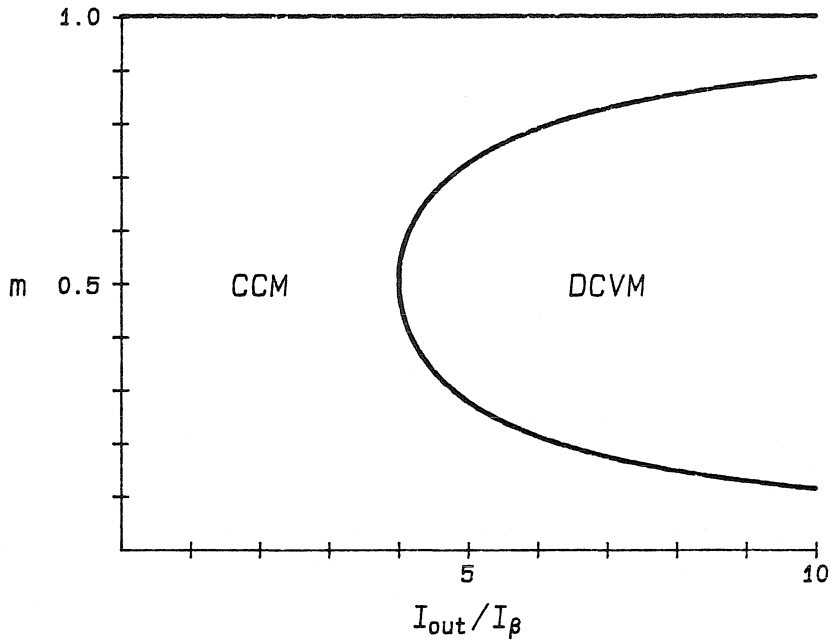


Figure 5.7: The CCM/DCVM operating regions for two-switch PWM converters.

5.2.2 Discontinuous Capacitor Voltage Mode

The discontinuous capacitor voltage mode (DCVM) is dual to the discontinuous inductor current mode. Therefore, all results for DCVM follow directly from the results of the previous section and duality relations of Section 3.1.2. The equivalent duty ratio is

$$m = 1 - \frac{(1-D_c)^2}{\frac{I_\beta}{I_{out}} + (1-D_c)^2}, \tag{5.14}$$

where

$$I_\beta \equiv 2V_g C_e f_s, \tag{5.15}$$

$$\frac{1}{C_e} \equiv \sum_{C_{off}} \frac{1}{C_i}. \tag{5.16}$$

In the load-to-output plane, the boundary curve between DCVM and CCM is

$$\frac{I_{out}}{I_\beta} = \frac{1}{m(1-m)}. \tag{5.17}$$

The operating regions for CCM and DCVM are shown in Fig. 5.7. The general expression for the DC conversion ratio is

$$D_c = 1 - \sqrt{\frac{k_\beta(1-D(M))}{MD(M)}}, \tag{5.18}$$

where

$$k_\beta \equiv 2RC_e f_s \,. \tag{5.19}$$

The critical value for the parameter k_β is given by

$$k_{\beta c} = D_c(1 - D_c)M(D_c) \,. \tag{5.20}$$

The converter operates in DCVM if $k_\beta \leq k_{\beta c}$.

While DICM can occur in any PWM topology, a necessary and sufficient condition for the existence of DCVM is that $\mathcal{C}_{off}$ is non-empty. Indeed, if $V_{off} = V_g = const.$, the PWM converter operates in CCM for an arbitrary large load current. However, if there exists a capacitor in the loop with the switches S and $\hat{S}$, the equivalent capacitance C_e is finite and DCVM is entered for a sufficiently large load current I_{out}.

5.3 Converters with a Floating Load

The synthesis procedure described in Chapter 4 encompassed only converters with a common input and output (ground) terminal. Without attempting to generate all possible converters with a floating load, we shall consider the case when two basic converters are combined to form a class of *bridge* PWM converters. In a bridge converter, the load is connected between outputs of two PWM converters as illustrated in Fig. 5.8(a). Similarly, an inverse bridge in Fig. 5.8(b) is obtained by connecting the source between the inputs of the two PWM converters. The DC conversion ratio of the bridge is $M(D) = M_1(D) - M_2(D)$, while $M(D) = 1/(1/M_1(D) - 1/M_2(D))$ for the inverse bridge. If $M(D)$ changes sign with D, PWM converters in the bridge must be current bidirectional.

In general, any two PWM converters can be used in the bridge connection. However, if the conversion ratios of the converters 1 and 2 are identical, the converters have to be operated at different duty ratios. The simplest and most commonly applied scheme is to use complementary control signals for the two converters so that $M_2(D) = M_1(1 - D)$.

One reason that bridge converters are used in practice is that voltage and/or current stresses are shared among switching devices. Thus, more devices with lower ratings can be used to process the same amount of power. Another reason is that bridge converters

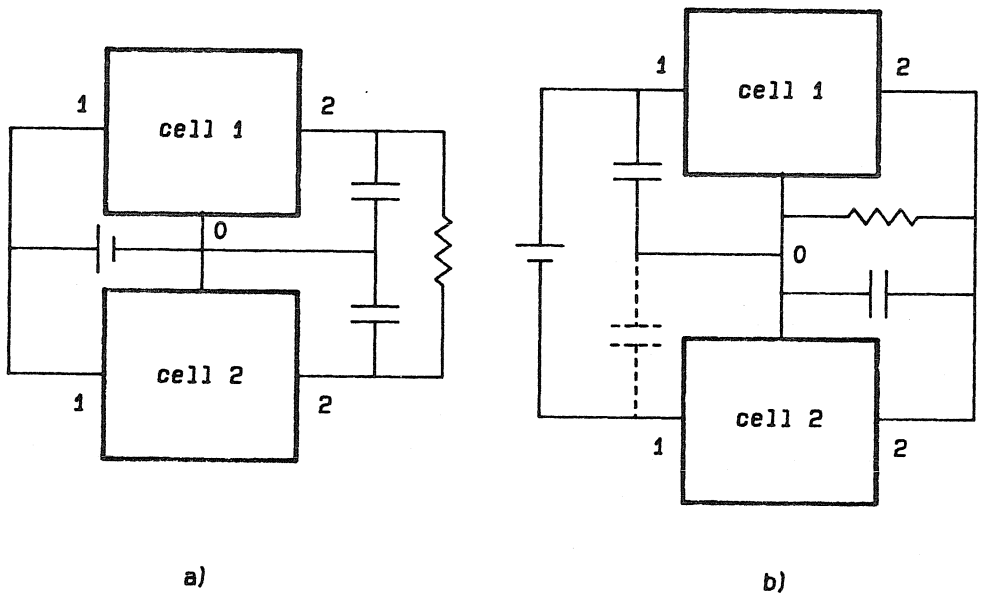


Figure 5.8: Bridge (a) and inverse bridge (b) converters.

can have a DC conversion ratio suitable for DC-to-AC inversion. For example, if two buck converters are connected in a bridge, $M(D) = 2D - 1$, and output voltage of either polarity can be generated.

5.4 Output Capacitor Transformation

The assumption that load R is in a loop with a single capacitor is a special case of the requirement that R is in a loop with capacitors and possibly V_g. In every PWM converter having the structure of Fig. 4.1, at least one output capacitor transformation is possible – capacitor C_1 can be placed between terminals 1 and 2 of the converter cell instead of being in parallel with the load R. Clearly, DC conversion properties of the converter are not affected by the transformation. However, it is possible that a more favorable distribution of currents can be obtained. Consider, for example, the buck-boost converter and the transformed converter (single-inductor Ćuk converter [26]) in Fig. 5.9. Input current is pulsating in the original buck-boost converter, while in the transformed

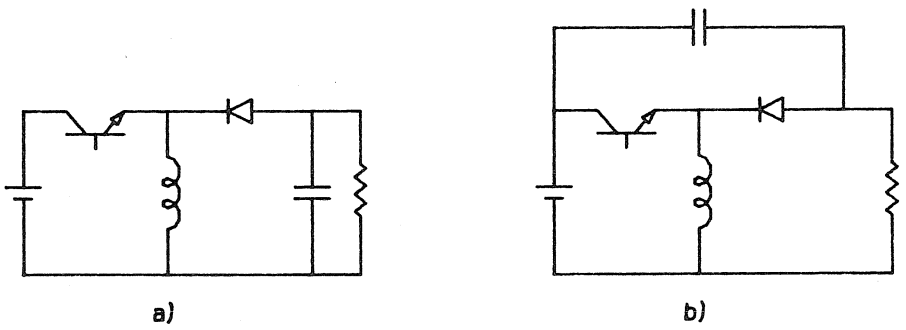


Figure 5.9: An example that illustrates how input current becomes continuous as a result of the output capacitor transformation.

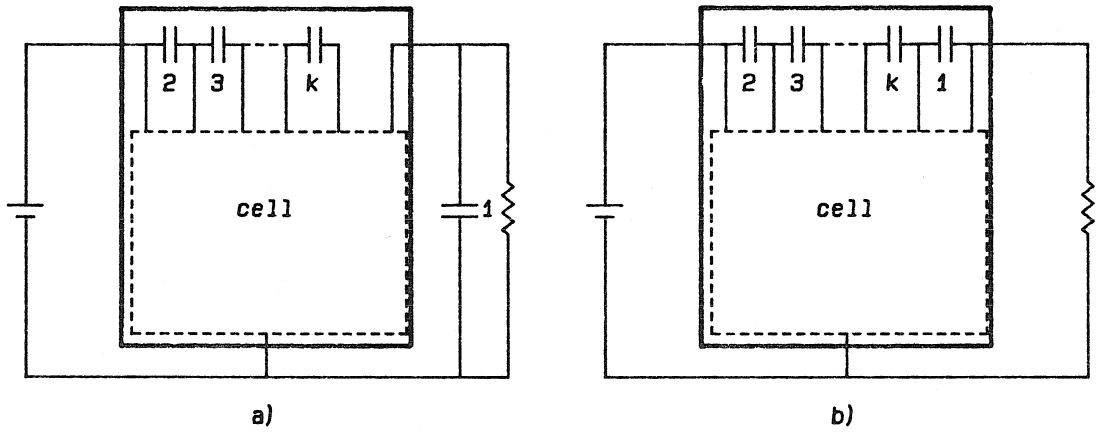


Figure 5.10: Output capacitor transformation.

converter it is continuous, with benefits of reduced conduction losses in the parasitic resistance of the input source. In addition, lower switching noise is generated toward the source. One disadvantage of the transformed buck-boost is that insertion of an isolation transformer is no longer feasible.

In general, the output capacitor transformation can involve any path consisting of elements in $\mathcal{C} \cup \{V_g\}$, as illustrated in Fig. 5.10.

Chapter 6

Synthesis of Quasi-Resonant DC-to-DC Converters

A straightforward approach in the continuous quest for smaller and lighter power converters is to reduce the size and weight of energy storage and filtering components by increasing the switching frequency. However, a substantial part of the total power loss in a power converter is proportional to the switching frequency. The trade-off between efficiency and size/weight puts an upper limit on the range of switching frequencies utilized in practical designs. Quasi-Resonant (QR) topologies were introduced as a means of reducing the frequency-dependent part of the losses associated with non-idealities of semiconductor switches. Corresponding savings in size and weight are based on the assumption that efficiency can be maintained while increasing the switching frequency.

Section 6.1 contains a brief introduction to the realm of Quasi-Resonant DC-to-DC power conversion.

In Section 6.2, a method for systematic synthesis of Quasi-Resonant converters is presented. The method is based on a definition that links QR to PWM converter networks. Any QR converter is constructed by adding two or more resonant elements to a given parent PWM converter network. Thus, general topological and conversion properties of PWM networks from Chapters 3 through 5 can be carried over and applied to synthesis and analysis of QR converters.

Six classes of QR converters with two resonant elements are obtained by extraction of all possible positions of resonant elements within a parent PWM topology. It is interesting that two of the classes have not been identified before.

In Section 6.3, QR classes with more than two resonant elements are derived recursively, starting from one of the previously defined QR classes. By means of proper

topological definitions, all known and newly uncovered QR classes are put into order.

In Section 6.4, it is emphasized that topology alone is not sufficient for complete characterization of a QR converter. In order to encompass all possible operating modes, different switch implementations are enumerated. It is important to note that in addition to conventional implementations with a single controllable switch, options with two controllable switches should be considered as well. A possibility of practical interest, confirmed in subsequent chapters, is that control at a constant switching frequency can be achieved at the expense of increased complexity of the converter network.

Common notation, conventions and structure of unified DC analyses completed in Chapters 7 through 10 for selected QR classes and operating modes are outlined in Section 6.5.

6.1 Quasi-Resonant Converters: Motivation and Basic Properties

In this section, a brief introduction to the topic of Quasi-Resonant conversion is presented. Motivation behind the introduction of Quasi-Resonant converters is outlined and used to derive one particular Quasi-Resonant topology in an intuitive manner. Finally, some of the basic properties and issues related to Quasi-Resonant converters are pointed out.

Consider the environment for semiconductor switches in a two-switch PWM converter as shown in Fig. 6.1(a). Under the small-ripple assumption, the transistor and the diode form a cut-set with a constant current source I_{on}. The two switches form a loop with a constant voltage source V_{off}. Idealized waveforms for the transistor are shown in Fig. 6.1(b). Assume that switches are ideal except that switching transitions are not instantaneous. Simplified waveforms during switching transitions are shown in Fig. 6.1(c,d). If the diode is conducting and the transistor is turned ON, the transistor current must first ascend to I_{on} before the transistor voltage starts to decrease from V_{off} toward zero. Thus, during the transistor ON-transition, instantaneous power loss on the transistor, $p_t = v_t \times i_t$, is not zero. Transistor current and voltage waveforms are interchanged during the turn-OFF transition, but the effect is the same – some power is lost on the switching device during the transition interval.

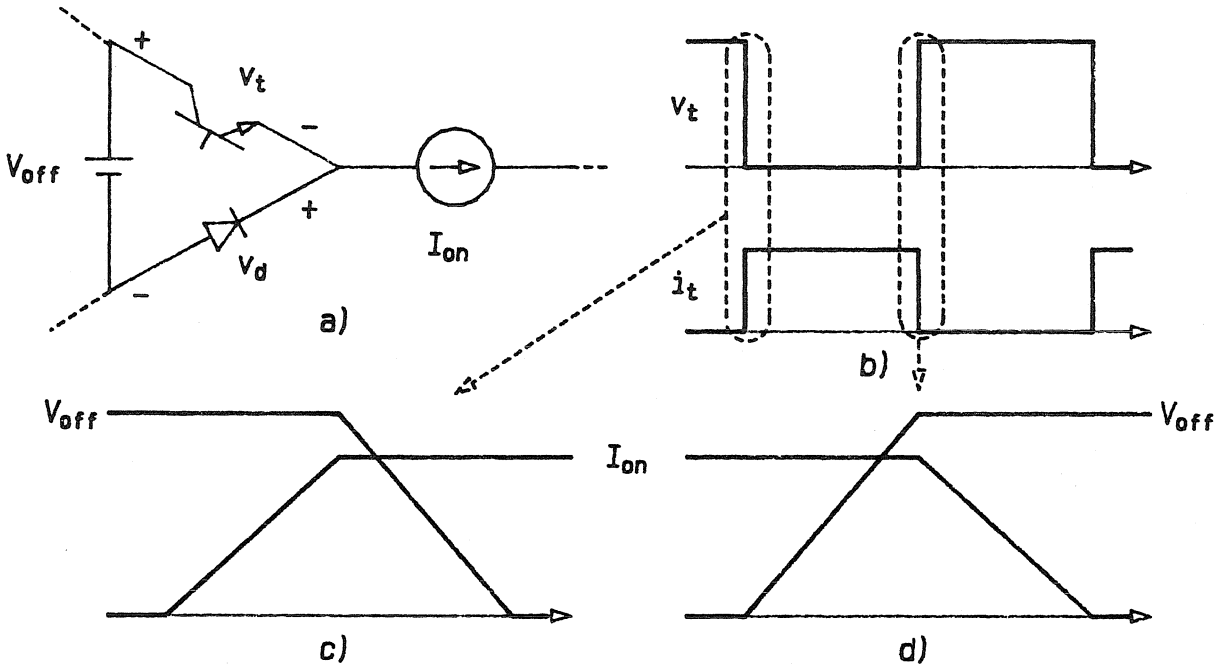


*Figure 6.1: Semiconoductor switches in a two-switch PWM converter (a), idealized transistor waveforms (b) and details of the transistor turn-*ON *(c) and turn-*OFF *(d).*

The power loss during the transistor turn-ON can be attributed to the fact that non-zero voltage and current waveforms overlap. The voltage transition is apparently lagging behind the current transition. One may attempt to decrease or eliminate the overlap by inserting an inductor in series with the transistor as shown in Fig. 6.2. Indeed, if the added inductance is sufficiently large and if the inductor current is initially zero, the transistor voltage is allowed to collapse to zero *before* the current attains a significant value. Losses attributed to the turn-ON transition can be significantly reduced, as is evident from the waveforms in Fig. 6.2. Consider, however, the transistor turn-OFF transition. The inductor in series with the transistor tends to delay the change in the transistor current with respect to the change in the transistor voltage. In the original PWM circuit, the transition in current is already delayed with respect to the transition in voltage, so that the power loss during the transistor turn-OFF becomes even larger. Another detrimental effect caused by attempting an abrupt change in the inductor current is that voltage across the transistor switch becomes much larger than V_{off}. The net effect is that all energy stored in the inductor is effectively lost during the turn-OFF

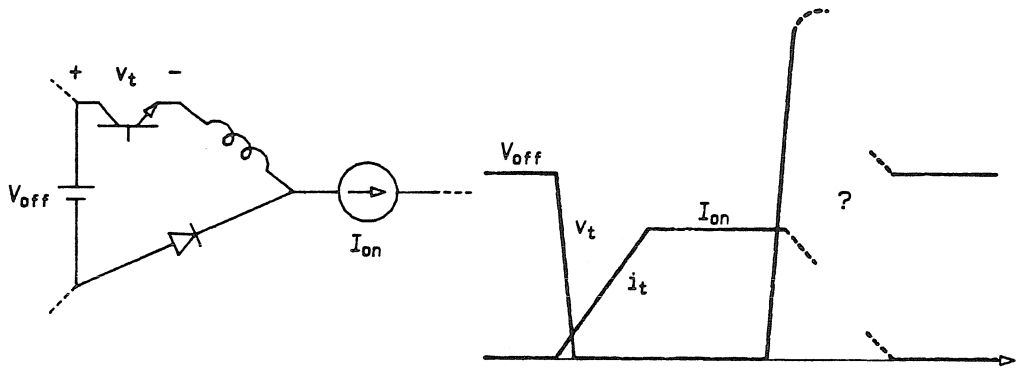


Figure 6.2: An attempt to reduce the switching losses by adding an inductor in series with the transistor in a PWM converter.

transition, thus completely compromising the lossless turn-ON transition. One may conclude that reduction in power loss will be achieved if, somehow, the inductor current is equal to zero during the turn-OFF transition. However, since the inductor current is not identically zero and since it should be zero at two points in the response of a LTI network driven by a DC source, the LTI network must necessarily contain a capacitor that *resonates* with the inductor.

In the circuit of Fig. 6.3, a capacitor is placed across the diode. Whenever the diode is OFF and the transistor is ON, the capacitor is allowed to resonate with the inductor, resulting in a sinusoidal waveform for the inductor current. The inductor current starts from zero and returns to zero again. Therefore, the transistor switch can be turned ON and OFF at *zero current* so that all switching losses are eliminated. Note that after passing through zero the inductor current continues to resonate and changes polarity. An "antiparallel" diode is added to the transistor switch to provide a path for the inductor current. Thus, after the capacitor and inductor are added to the PWM network, the transistor switch needs to be converted to a current-*bidirectional* switch. In fact, the transistor need not be turned OFF exactly at zero inductor current. If it is turned OFF at any instant while the antiparellel diode is conducting, the waveforms and operation of the circuit are not affected. One immediate consequence should be noted – the transistor turn-OFF is no longer a controllable transition since it is dictated by the circuit waveforms

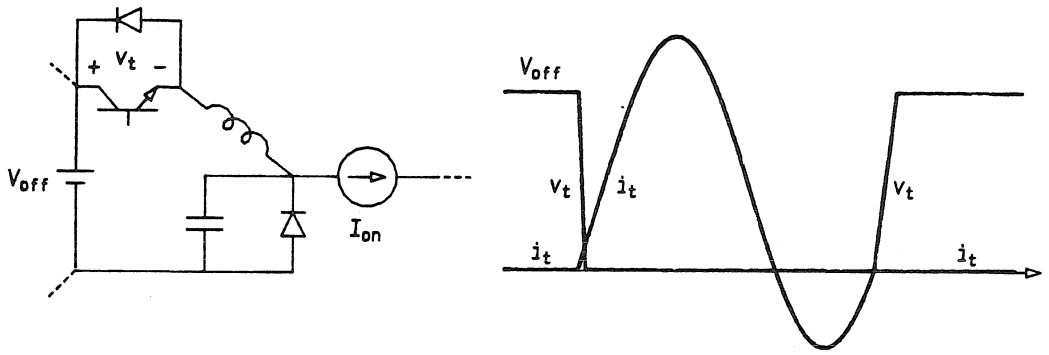


Figure 6.3: A Zero-Current, Quasi-Resonant converter.

rather than by some external control.

The circuit in Fig. 6.3 is a representative of *Zero-Current* converters operating in the *full-wave mode* [12,13]. If the transistor is converted to a voltage-bidirectional switch, the negative portion of the inductor current waveform disappears, but zero-current switching is still possible. The resulting operating mode is called the *half-wave mode*. It is somewhat surprising that although the change in waveforms may look relatively insignificant, behavior of converters in the two modes is immensely different [20]. This indicates the importance of *switch implementations* and *operating modes* in addition to the topology of a QR converter.

Non-instantaneous switching is not the only cause of switching losses in PWM converters. Loss mechanisms also arise from the fact that each semiconductor device has its junction capacitance(s). If the switch voltage is equal to V_{off} before the ON-transition, as in the circuits of Figs. 6.1 through 6.3, energy stored in the junction capacitance is dissipated in the junction itself. Since the energy stored in the junction capacitance is dissipated in every switching cycle, the power loss is again proportional to the switching frequency.

In the circuit of Fig. 6.3, one may note that the resonant capacitor coincides with the position of the diode junction capacitance. Because of the resonance with the added inductor, voltage across the diode starts from zero, resonates in a sinusoidal manner, and then drops to zero gradually. The diode turns ON and OFF at *zero voltage*, and

losses associated with charge and discharge of its junction capacitance are completely eliminated. On the contrary, losses associated with the transistor junction capacitance are not eliminated.

In addition to junction capacitances, parasitic inductance in the loop with switches is present unintentionally in any PWM converter. Part of the energy stored in the inductance is dissipated in each cycle, just as in the case of the circuit in Fig. 6.2. In the Zero-Current circuit, however, the parasitic inductance in the loop with switches can be absorbed by the added resonant inductor. This reveals another important feature of Quasi-Resonant converters – *insensitivity to major parasitic reactances.* For example, a Zero-Current converter is insensitive to the junction capacitance of the diode and to the parasitic inductance in the loop with the switches but not to the junction capacitance of the transistor.

The complete quantitative estimation of switching losses in a power converter is a complex problem since effects described so far are not independent, and many second-order effects were completely neglected. Nevertheless, it is sufficient to note that switching losses in a PWM converter are results of the inevitable circuit parasitic reactances and finite switching speed of semiconductor devices. Introduction of Quasi-Resonant converters is motivated by possible elimination of some or all major loss mechanisms by appropriately shaping the switch voltage and/or current waveforms and by incorporating parasitics into the resonant network.

Various classes of QR converters were introduced mainly as intuitively justified circuit modifications of the PWM converters. The derivation was strongly motivated by the goals of eliminating some or all switching-loss mechanisms.

In the systematic synthesis of QR converters pursued in this chapter, the original motivation is temporarily set aside. A QR converter is *defined* as the network generated from a PWM network by addition of two or more resonant elements. Then, all eligible positions of resonant elements are extracted by use of simple topological properties of the original PWM parent network. Once distinct classes of QR converters are formally defined, we turn back to the original motivation and examine operating modes with all transitions at zero voltage or at zero current for different switch implementations.

6.2 Synthesis of Quasi-Resonant Converters with Two Resonant Elements

Consider a PWM converter network N with two switches – S and $\hat{S}$, a set of capacitors $\mathcal{C}$ and a set of inductors $\mathcal{L}$. A Quasi-Resonant converter is defined as follows:

Definition 6.1 *Starting from a two-switch PWM converter network N for which the small-ripple assumption is satisfied and for which there exists a unique steady-state solution, construct a new network N_r by adding a single resonant capacitor C_r and a single resonant inductor L_r. The network N_r is a Quasi-Resonant DC-to-DC converter if*

B1: each resonant element forms a loop with elements in N or a cut-set with an element in N;

B2: $N_r = N$ at DC.

Since the small-ripple assumption is imposed on the parent PWM converter, PWM capacitors and inductors are clearly distinguished from added resonant elements. Furthermore, we may assume that $L_r << L_i \in \mathcal{L}$ and $C_r << C_i \in \mathcal{C}$.

Assumption B1 guarantees that N_r has a non-separable graph so that both resonant elements participate in the operation of a QR converter. Assumption B2 ties DC conversion properties of a QR converter to conversion properties of its PWM parent. The two networks should be identical if all inductors are shorted and all capacitors are removed. If there is a unique solution for average switch voltages and currents in N_r, a unique solution is guaranteed for all states and for the DC conversion ratio of the QR converter. It is important to note that by definition, the unifying analysis method outlined in Section 3.6 is applicable to all QR converters derived from two-switch PWM parents.

We now examine all possible positions of the resonant elements C_r and L_r.

Case 1: C_r is in a cut-set with an element in N.

If the resonant capacitor is placed in series with V_g or R, in series with a switch, or in series with an inductor in $\mathcal{L}$, Assumption B2 of Definition 6.1 is violated. In fact, it can be shown that in these cases the network N_r is not a valid DC-to-DC converter. If C_r is placed in a cut-set with a capacitor C_i in $\mathcal{C}$, the switch waveforms are not affected unless

C_i is also in $\mathcal{C}_{off}$. Thus, the only eligible position of C_r is in a cut-set with a capacitor in $\mathcal{C}_{off}$. However, since every capacitor in $\mathcal{C}_{off}$ forms a cut-set with a switch and a non-empty set of inductors in $\mathcal{L}$, possible positions of C_r with respect to the switches are:

CcS : C_r is in a cut-set with the S-switch and a non-empty set of inductors in $\mathcal{L}$;

$Cc\hat{S}$: C_r is in a cut-set with the $\hat{S}$-switch and a non-empty set of inductors in $\mathcal{L}$.

Case 2: C_r is in a loop with elements in N.

In this case, Assumption B2 is satisfied for every position of the resonant capacitor. If, however, C_r forms a loop with elements in $\{V_g\}\cup\mathcal{C}$ only, the voltage across C_r is constant, and addition of the resonant element does not affect the switch waveforms. All other positions of the resonant capacitor with respect to the switches are encompassed by the following two:

ClS : C_r is in a loop with the S-switch and a possibly empty set of elements in $\{V_g\}\cup\mathcal{C}$;

$Cl\hat{S}$: C_r is in a loop with the $\hat{S}$-switch and a possibly empty set of elements in $\{V_g\}\cup\mathcal{C}$.

Case 3: L_r is in a loop with elements in N.

By the arguments dual to the arguments in Case 1, L_r can form a loop only with inductors in $\mathcal{L}_{on}$. The following two cases encompass all possible positions with respect to the switches:

LlS : L_r is in a loop with the S-switch and a non-empty set of elements in $\{V_g\}\cup\mathcal{C}$;

$Ll\hat{S}$: L_r is in a loop with the $\hat{S}$-switch and a non-empty set of elements in $\{V_g\}\cup\mathcal{C}$.

Case 4: L_r is in a cut-set with an element in N.

Eligible positions of L_r with respect to the switches are dual to the positions of the resonant capacitor in Case 2:

LcS : L_r is in a cut-set with the S-switch and a possibly empty set of inductors in $\mathcal{L}$;

$Lc\hat{S}$: L_r is in a cut-set with the $\hat{S}$-switch and a possibly empty set of inductors in $\mathcal{L}$.

<table>
<tr><th></th><th>LcS</th><th>$Lc\hat{S}$</th><th>LlS</th><th>$Ll\hat{S}$</th></tr>
<tr><td>ClS</td><td>×</td><td>ZV</td><td colspan="2" rowspan="2">ZV-QSW</td></tr>
<tr><td>$Cl\hat{S}$</td><td>ZC</td><td>×</td></tr>
<tr><td>CcS</td><td colspan="2" rowspan="2">ZC-QSW</td><td>×</td><td>Q_n-PWM</td></tr>
<tr><td>$Cc\hat{S}$</td><td>Q_f-PWM</td><td>×</td></tr>
</table>

Table 6.1: Classes of two-switch, Quasi-Resonant converters with two resonant elements.

There are at most sixteen classes of QR converters corresponding to all possible combinations of positions of resonant elements. However, not all combinations are feasible, and some combinations are equivalent.

Suppose that the resonant capacitor is in the ClS position. Then, every cut-set that includes S but does not include any of the elements in $\{V_g\} \cup \mathcal{C}$ must include C_r. Hence, combination $ClS - LcS$ is not realizable. By the same or by dual arguments, combinations $Cl\hat{S} - Lc\hat{S}$, $CcS - LlS$ and $Cc\hat{S} - Ll\hat{S}$ are not feasible.

Suppose that the resonant capacitor is in the ClS position. By Proposition 3.7, the S-switch and the $\hat{S}$-switch form a loop with elements in $\{V_g\} \cup \mathcal{C}$. Provided that the resonant inductor is in a loop with inductors in $\mathcal{L}$, it follows that C_r is also in the $Cl\hat{S}$ position. Therefore, combinations $ClS - LlS$, $Cl\hat{S} - LlS$, $ClS - Ll\hat{S}$ and $Cl\hat{S} - Ll\hat{S}$ are equivalent. By a dual argument it follows that combinations $CcS - LcS$, $CcS - Lc\hat{S}$, $Cc\hat{S} - LcS$ and $Cc\hat{S} - Lc\hat{S}$ are equivalent.

The complete set of classes of Quasi-Resonant converters with two resonant elements has six members, defined in Table 6.1.

A note about terminology is in order. The name for each class of Quasi-Resonant converters (except for two Q-PWM classes) is adopted from the reference where con-

verters in compliance with the definition appeared – [12] for *Zero-Current* (ZC), [14] for *Zero-Voltage* (ZV) and [18] for *Zero-Voltage, Quasi-Square-Wave* (ZV-QSW) and *Zero-Current, Quasi-Square-Wave* classes. ZV-QSW and ZC-QSW converters were introduced in [17], but no particular name was suggested. None of converters in *On-Resonant Quasi-PWM* (Q_n-PWM) and *Off-Resonant Quasi-PWM* (Q_f-PWM) classes have appeared in the literature known to the author.

For illustration of loops and cut-sets in the definitions of QR converters, circuit examples derived from the SUSD(9) (inverse Sepic) PWM converter are shown in Fig. 6.4. An inductor in $\mathcal{L}$ (PWM inductor) can always be removed from parallel combination with the resonant inductor L_r. Similarly, a capacitor in $\mathcal{C}$ (PWM capacitor) in series with the resonant capacitor C_r can be absorbed. Consequently, the circuits of the two Q-PWM converters have exactly the same topology as the original PWM converter. Therefore, Q-PWM converters can be viewed as PWM converters operating in both discontinuous modes, DICM and DCVM, simultaneously. In the same manner, QSW converters can be considered as PWM converters in DICM or DCVM to which a *single* resonant element is added. In the sense of this interpretation, only ZV and ZC classes would represent "true" Quasi-Resonant converters with two resonant elements.

6.3 Synthesis of More Complex Quasi-Resonant Converters

Quasi-Resonant converters may have more than two resonant elements. We can take advantage of the fact that all QR classes with two resonant elements are now known. More complex QR converters can be defined recursively – in Definition 6.1, PWM network N is replaced by one of the previously defined Quasi-Resonant networks N_r and a single resonant element L_{r1} or C_{r1} is added so that Assumptions B1 and B2 are satisfied.

For example, if parent networks are taken from the ZV class, six classes of QR converters with three resonant elements can be identified – with an additional resonant inductor in the LcS, LlS or $Ll\hat{S}$ position, or with an additional resonant capacitor in the CcS, $Cc\hat{S}$ or $Cl\hat{S}$ position. It is easy to recognize that ZV $+Cl\hat{S}$ and ZV $+LcS$ formally define converters introduced as *Zero-Voltage, Multi-Resonant* (ZV-MR) and *Zero-Current, Multi-Resonant* (ZC-MR) in [16], while other classes have not been identified before.

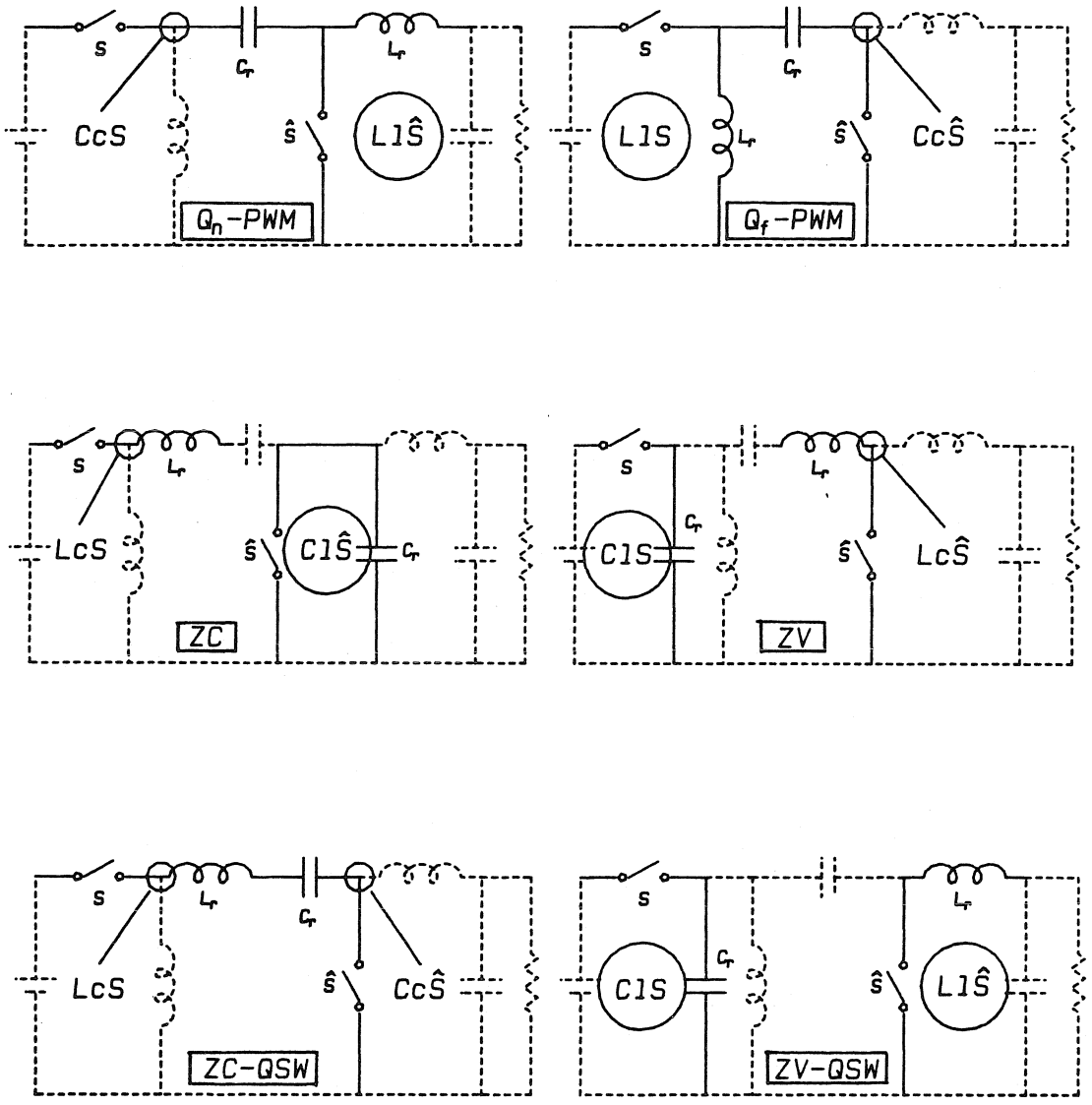


Figure 6.4: Circuit examples that illustrate loops and cut-sets in the topological definitions of QR converters with two resonant elements. Six Quasi-Resonant converters are derived from the Inverse Sepic (SUSD(9)) PWM converter.

At this point, it should be noted that, in general, simplicity of the converter network is beneficial from the standpoints of size, weight and cost trade-offs. Also, analysis and consequently design of more complex QR converters are inevitably more involved. Introduction and utilization of more complex resonant networks need to be well motivated and justified. Among QR converters defined from the ZV class, ZV-MR converters are particularly interesting since the positions of all major parasitic reactances in the converter circuit are consistent with the positions of the resonant elements. Furthermore, operating modes with all transitions at zero voltage can be found. Thus, at least theoretically, the ZV-MR class offers complete elimination of switching losses associated with non-idealities of semiconductor switching devices.

It is interesting to note that converters in classes ZV $+Ll\hat{S}$ and ZV $+CcS$ can be viewed as Zero-Voltage converters that operate in DICM and DCVM, respectively.

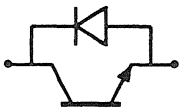
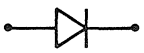
6.4 Operating Modes of Quasi-Resonant Converters

For PWM converters, topology alone is sufficient for complete understanding of the circuit operation under the small-ripple assumption. In two-switch PWM converters, either one of the switches is ON at any time. All waveforms in the circuit are either DC or square-wave and they can be usually inferred by inspection of the converter topology. On the contrary, operation of a Quasi-Resonant converter cannot be deduced from the topology alone. In general, in addition to the operating states ON-ON and OFF-OFF, two more states are possible: the state when both switches are ON and the state when both switches are OFF. Waveforms and conversion properties depend on the operating mode defined by the succession of the four operating states inside a switching cycle. Operating modes for which all transitions are at zero current or at zero voltage are of major practical interest.

6.4.1 Switch Implementations

Complete characterization of QR converters is further complicated by the fact that operating modes depend on the implementation of switches. Possible switch implemen-

tations are the following:

switch S or $\hat{S}$: { controllable { current-bidirectional,  ; voltage-bidirectional,  } ; uncontrollable (diode).  }

(6.1)

A total of five distinct combinations of switch implementations can be inferred from the diagram above:

CD: current-bidirectional + diode,

VD: voltage-bidirectional + diode,

CC: current-bidirectional + current-bidirectional,

VV: voltage-bidirectional + voltage-bidirectional,

CV: current-bidirectional + voltage-bidirectional.

In PWM converters, both turn-ON and turn-OFF transitions can be controlled by an external signal. Hence, constant-frequency control can be applied. With the exception of two Q-PWM classes, only one switching transition is subject to external control in operating modes of QR converters with a single controllable switch (implementations CD or VD). Remaining transitions are determined by zero-crossing of the switch voltage or current waveforms. Therefore, variable-frequency control must be employed in order to regulate the output DC voltage. Two controllable transitions and therefore constant-frequency control can be restored if *both* switches are implemented as controllable (implementations CC, VV and CV).

As discussed in the example of a Zero-Current converter, because of the losses associated with parasitic junction capacitances, zero-voltage switching is more favorable than zero-current switching. Zero-voltage switching of a voltage-bidirectional switch is not feasible in practice. This is because the diode in series with the transistor prevents

quantity	base
voltage	V_{off}
current	V_{off}/R_o
time	$1/\omega_r$
frequency	f_r

Table 6.2: Base quantities for normalization.

resonant discharge of the transistor junction capacitance. The transistor voltage at turn-ON is essentially equal to the peak voltage across the voltage-bidirectional switch and losses that are due to discharge of the junction capacitance are inevitable. In Chapters 7 through 10, only operating modes for switch implementations CD and CC are studied in detail.

6.5 DC analysis of QR converters

A study of selected classes of QR converters is undertaken in Chapters 7 through 11. Notation, conventions and structure of the analyses are outlined in this section.

In order to obtain results that are generic with respect to specific values of circuit parameters, it is useful to introduce normalized electrical and time parameters.

Define:

$$\omega_r \equiv 2\pi f_r \equiv \frac{1}{\sqrt{L_r C_r}} \quad \text{and} \quad R_o \equiv \sqrt{\frac{L_r}{C_r}}\,. \tag{6.2}$$

A quantity X normalized with respect to Y is denoted as $\{X\}_Y$. The base Y is given in Table 6.2 for all quantities of interest. For brevity, the notation in Table 6.3 will be used in the analyses of QR converters.

Possible operating states are denoted as ON-ON, ON-OFF, OFF-ON and OFF-OFF, indicating the states of the switches S and $\hat{S}$.

By definition, a QR converter and its PWM parent have the same DC network, so that the unified analysis approach outlined in Section 3.6 is applicable. Since

$$\delta \equiv \{I_{on}\}_{V_{off}/R_o} = \{I_{out}\}_{V_g/R_o}\,, \tag{6.3}$$

parameter δ can be regarded as a normalized output current.

ON current	$i_{on}(t)$	$\{i_{on}(t)\}_{V_{off}/R_o} \equiv i_{on}$
OFF voltage	$v_{off}(t)$	$\{v_{off}(t)\}_{V_{off}} \equiv v_{off}$
S-switch voltage	$v_t(t)$	$\{v_t(t)\}_{V_{off}} \equiv v_t$
S-switch current	$i_t(t)$	$\{i_t(t)\}_{V_{off}/R_o} \equiv i_t$
$\hat{S}$-switch voltage	$v_d(t)$	$\{v_d(t)\}_{V_{off}} \equiv v_d$
$\hat{S}$-switch current	$i_d(t)$	$\{i_d(t)\}_{V_{off}/R_o} \equiv i_d$
average ON current	I_{on}	$\{I_{on}\}_{V_{off}/R_o} \equiv \delta$
average OFF voltage	V_{off}	$\{V_{off}\}_{V_{off}} = 1$
average $\hat{S}$-switch voltage	$\overline{v}_d$	$\{\overline{v}_d\}_{V_{off}} \equiv m$
average S-switch current	$\overline{i}_t$	$\{\overline{i}_t\}_{V_{off}/R_o} = \delta m$
time	t	$\{t\}_{1/\omega_r} \equiv \theta$
switching frequency	f_s	$\{f_s\}_{f_r} \equiv f$
switching period	T_p	$\{T_p\}_{1/\omega_r} \equiv \theta_p$

Table 6.3: Notation for the analysis of QR converters.

DC analysis is reduced to establishing the equivalent duty ratio m as a function of the normalized current δ and the control variable that dictates the timing of controllable transitions. Once m is known, DC conversion ratio for any specific topology is equal to $M(m)$, where function $M(\cdot)$ is inherited from the parent PWM converter.

Overall structure for each of the analyses is the same:

1. Based on the topological definition of the QR class under study, state variables are chosen so that description of the four operating states is valid for any converter in the class (any topological variation) and any PWM parent topology.

2. Operating modes with all transitions at zero voltage or zero current are identified for switch implementations with one and two current-bidirectional, controllable switches (CD and CC). Operating modes are denoted by Roman numbers with subscripts that indicate the number of controllable switches. A *state transition diagram* used for the study of possible operating modes is a graph in which nodes represent the operating states and oriented edges represent transitions. An edge is a solid line if the transition is at zero voltage or at zero current, a dashed line

otherwise. The sign © is used to denote controllable transitions. Operating modes in which the periodic sequence includes more than four states are not considered.

3. For each of the selected modes, the equivalent duty ratio m is found as a function of the normalized load current δ and the appropriate control variable. If only one transition in the operating mode is controllable, the control variable is the switching frequency f. If two transitions are controllable, the control variable is the length of the interval between the controllable transitions relative to the switching period, θ_c/θ_p. In all cases, DC analysis is performed in two steps:

   – a steady-state solution is found for the state variables by equating initial conditions at the beginning and end of a switching cycle;

   – the solution for the state variables is used to compute the average switch voltage or current and finally, the equivalent duty ratio m.

   Lengths of the operating states are denoted by θ_i. The same subscript is used to denote voltages and currents at the *end* of the i^{th} operating state.

4. Conditions for operation in the selected operating mode are established and translated into the load-to-output (δ–m) plane. Part of the plane where the conditions are satisfied and the mode is possible is called the *operating region.*

5. DC characteristics are found in both load-to-output and control-to-output planes.

6. Existence of selected modes and corresponding DC characteristics are verified experimentally. Experimental verification is necessary since in the analysis two idealizing assumptions are made: the small-ripple assumption and the assumption that there are no losses in the converter circuit.

Detailed study is performed for classes Q_n-PWM, ZV, ZV-QSW, and ZV-MR, which exhibit more favorable sets of switching transitions (except for Q_n-PWM for which the selection is arbitrary). Results for dual classes follow directly from duality relations.

Chapter 7

On-Resonant, Quasi-PWM Converters

This chapter is devoted to a study of On-Resonant, Quasi-PWM (Q_n-PWM) converters defined in Chapter 6.

An operating mode (I_1) with all switching transitions at zero current or at zero voltage is found in Section 7.1. The transistor turn-ON and the diode turn-OFF are at zero current, while the transistor turn-OFF and diode turn-ON are at zero voltage. It is interesting that in contrast to other QR classes, constant-frequency, duty-ratio control is possible although only one switch is controllable.

For mode I_1, DC analysis is carried out in Section 7.2. A closed-form solution is found for the equivalent duty ratio m as a function of load current and switching frequency.

Operation in mode I_1 is possible in a bounded portion of the load-to-output plane. The operating region does not include the zero-load axis so that the attainable load range is limited. Normalized switching frequency is a design parameter that can be selected to optimize the load range for a given conversion ratio.

Existence of the operating mode I_1 and results of the DC analysis are confirmed by experimental verification of Section 7.3.

7.1 Operating States and Operating Modes

By definition, in a Q_n-PWM converter, resonant capacitor C_r is in series with a PWM capacitor $C_i \in \mathcal{C}$, while resonant inductor L_r is in parallel with a PWM inductor $L_i \in \mathcal{L}$. Hence,

$$v_{off} = V_{off} + v_{C_r}, \tag{7.1}$$

$$i_{on} = I_{on} + i_{L_r}. \tag{7.2}$$

Kirchhoff's current law for the cut-set CsS, which contains C_r, the S-switch and a non-empty set of PWM inductors, yields

$$\frac{dv_{off}}{d\theta} + i_t = m\delta \,. \tag{7.3}$$

Similarly, by applying Kirchhoff's voltage law for the loop $Ll\hat{S}$, which contains L_r, the $\hat{S}$-switch and a non-empty set of PWM capacitors, we obtain

$$\frac{di_{on}}{d\theta} + m = v_d \,. \tag{7.4}$$

Finally, by Proposition 3.7 it follows that the switches (S and $\hat{S}$) are in a loop with C_r and elements in $\mathcal{C}_{off}$. Also, S and $\hat{S}$ are in a cut-set with L_r and elements in $\mathcal{L}_{on}$. Therefore,

$$v_t + v_d = v_{off} \,, \tag{7.5}$$

$$i_t + i_d = i_{on} \,. \tag{7.6}$$

Operating States

From Eqs. (7.3) through (7.6), equations and solutions for the four operating states of a Q_n-PWM converter are found in terms of the state variables v_{off} and i_{on}:

ON-ON state: $v_t = v_d = 0$.

Equations:

$$\frac{di_{on}}{d\theta} = -m \,,\; i_{on}(0) = I_{nn} \,. \tag{7.7}$$

Solution:

$$v_{off} = 0 \,, \tag{7.8}$$

$$i_{on} = I_{nn} - m\theta \,. \tag{7.9}$$

ON-OFF state: $v_t = 0$, $i_d = 0$.

Equations:

$$\frac{dv_{off}}{d\theta} + i_{on} = m\delta \;,\; v_{off}(0) = V_{nf} \,, \tag{7.10}$$

$$\frac{di_{on}}{d\theta} + m = v_{off} \;,\; i_{on}(0) = I_{nf} \,. \tag{7.11}$$

Solution:

$$v_{off} = m + (V_{nf} - m)\cos\theta + (m\delta - I_{nf})\sin\theta \,, \tag{7.12}$$

$$i_{on} = m\delta + (I_{nf} - m\delta)\cos\theta + (V_{nf} - m)\sin\theta \,. \tag{7.13}$$

OFF-ON state: $i_t = 0$, $v_d = 0$.

Equations:

$$\frac{dv_{off}}{d\theta} = m\delta \;,\; v_{off}(0) = V_{fn} \,, \tag{7.14}$$

$$\frac{di_{on}}{d\theta} = -m \;,\; i_{on}(0) = I_{fn} \,. \tag{7.15}$$

Solution:

$$v_{off} = V_{fn} + m\delta\theta \,, \tag{7.16}$$

$$i_{on} = I_{fn} - m\theta \,. \tag{7.17}$$

OFF-OFF state: $i_t = i_d = 0$.

Equations:

$$\frac{dv_{off}}{d\theta} = m\delta \;,\; v_{off}(0) = V_{ff} \,. \tag{7.18}$$

Solution:

$$v_{off} = V_{ff} + m\delta\theta \,, \tag{7.19}$$

$$i_{on} = 0 \,. \tag{7.20}$$

An Operating Mode with All Zero-Voltage and/or Zero-Current Transitions

Assume that switch implementation is conventional: the S-switch is a transistor (not necessarily bidirectional), while the $\hat{S}$-switch is a diode. Possible operating modes in

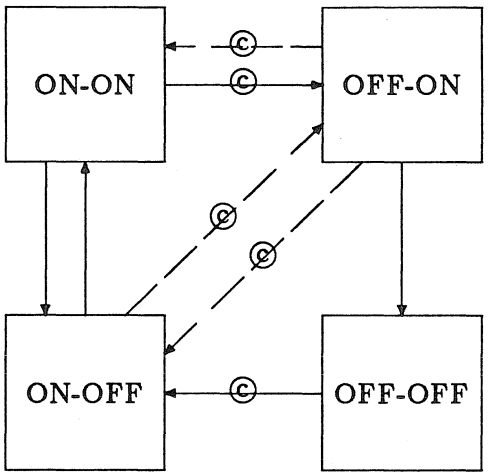


Figure 7.1: State transition diagram for a Q_n-PWM converter.

a Q_n-PWM converter can be inferred conveniently from the state transition diagram of Fig. 7.1. Dashed transitions are lossy; i.e., they occur at non-zero voltage *and* non-zero current. For example, transitions ON-OFF $\leftrightarrow$ OFF-ON are the same as transitions in a PWM converter. A transition OFF-ON $\rightarrow$ ON-ON is possible if $i_{on} > m\delta$, but the transistor switch turns ON at non-zero current and non-zero voltage. This leaves the periodic sequence of states

$$\text{Mode } I\text{: } \cdots \rightarrow \boxed{\text{ON-OFF}} \rightarrow \boxed{\text{ON-ON}} \rightarrow \boxed{\text{OFF-ON}} \rightarrow \boxed{\text{OFF-OFF}} \rightarrow \cdots \tag{7.21}$$

as the only operating mode for which switching losses are minimized, as all switching transitions can be realized at zero voltage or at zero current. The mode is denoted as mode I_1 with the subscript used to indicate that only the S-switch is controllable.

Once the sequence of states is established, one can qualitatively describe operation of a Q_n-PWM converter. Assume that initially the converter is in the OFF-OFF state. Transition to the ON-OFF state is achieved by turning the transistor switch ON. Initial conditions for the ON-OFF state are: $I_{nf} = 0$ and $V_{nf} = v_4$. The transistor turn-ON is at *zero current*. The ON-OFF state is the resonant state. It lasts until voltage v_{off} drops to zero at $\theta = \theta_1$. The diode starts to conduct at *zero voltage* and the ON-ON state is entered. The initial condition for the ON-ON state is $I_{nn} = i_1$. During the ON-ON state, voltage v_{off} is clamped to zero while current i_{on} decays linearly from i_1 to zero. After the transistor is turned OFF at *zero voltage* at $\theta = \theta_2$, the ON-ON state is terminated and

the OFF-ON state commences. Initial conditions for the OFF-ON state are $V_{fn} = 0$ and $I_{fn} = i_1 - m\theta_2$. Voltage v_{off} now starts to increase linearly. Current i_{on} continues to decay linearly to zero when the diode switch is turned OFF at *zero current* at $\theta = \theta_3$. The initial condition for the OFF-OFF state is $V_{ff} = m\delta\theta_3$. At the end of the switching period, for $\theta = \theta_4$, v_{off} reaches the value v_4 and the next switching cycle is initiated by turning the transistor ON again.

Typical waveforms in a Q_n-PWM converter are shown in Fig. 7.2. Waveform p_t indicates the state of the transistor switch. Two transitions are controllable in mode I_1 and consequently, both variable-frequency and constant-frequency control strategies are applicable. Only the constant-frequency option will be studied in detail.

Control duty ratio D_c is defined in the same manner as for PWM converters – as the ratio of the transistor ON-time relative to the switching period,

$$D_c = \frac{\theta_1 + \theta_2}{\theta_p}. \tag{7.22}$$

7.2 DC Analysis

From the solutions for the OFF-ON and OFF-OFF states, it follows that voltage v_{off} at the end of a switching cycle is

$$v_4 = (\theta_3 + \theta_4)m\delta = (1 - D_c)m\delta\theta_p. \tag{7.23}$$

After substituting $V_{nf} = v_4$ and $I_{nf} = 0$ as initial conditions for the ON-OFF state, the equation $v_{off}(\theta_1) = 0$ can be solved for θ_1. Assuming that the solution exists, θ_1 and consequently, i_1/m, are given by

$$\theta_1 = \pi - \arctan\frac{(1 - D_c)\delta\theta_p - 1}{\delta} + \arctan\frac{1}{\sqrt{((1 - D_c)\delta\theta_p - 1)^2 + \delta^2}}, \tag{7.24}$$

$$\frac{i_1}{m} = \delta + \sqrt{((1 - D_c)\delta\theta_p - 1)^2 + \delta^2 - 1}. \tag{7.25}$$

Length of the ON-ON state is determined by the control variable D_c,

$$\theta_2 = D_c\theta_p - \theta_1. \tag{7.26}$$

Current i_{on} at the and of the ON-ON state is

$$i_2 = i_1 - m\theta_2. \tag{7.27}$$

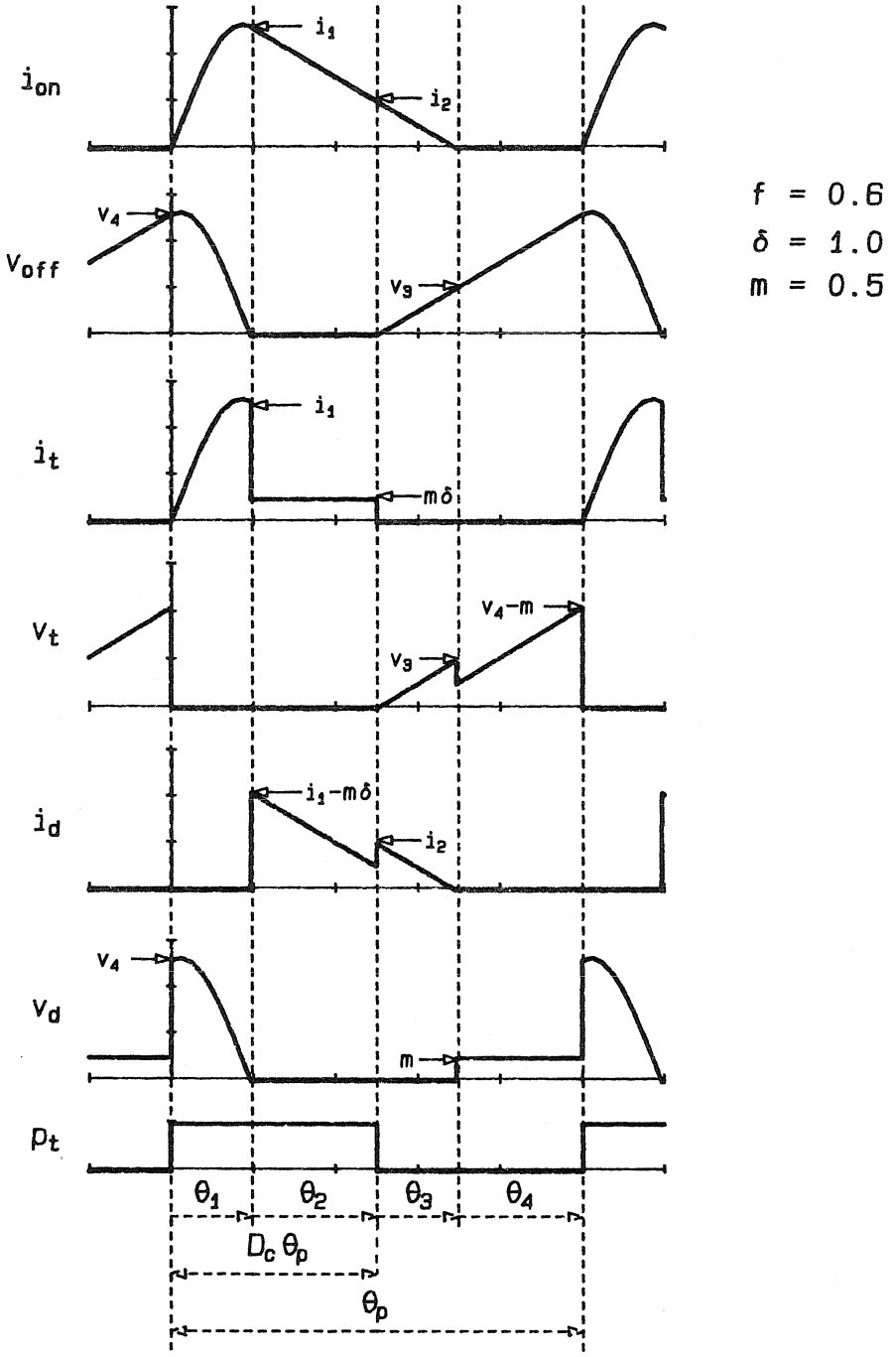


Figure 7.2: Typical waveforms in a Q_n-PWM converter.

Duration of the OFF-ON state is

$$\theta_3 = i_1/m - \theta_2 \,. \tag{7.28}$$

Finally, the OFF-OFF state lasts until the end of the switching period,

$$\theta_4 = \theta_p - \theta_1 - \theta_2 - \theta_3 = \theta_p - \theta_1 - i_1/m \,. \tag{7.29}$$

The equivalent duty ratio is found by equating the average of voltage v_{off} over one cycle to 1. The result,

$$m = \frac{\theta_p}{\theta_1 + \delta + \sqrt{((1-D_c)\delta\theta_p - 1)^2 + \delta^2 - 1} + \frac{1}{2}(1-D_c)^2\theta_p^2\delta} \,, \tag{7.30}$$

together with expression (7.24) for θ_1, gives the equivalent duty ratio m as an explicit function of normalized load current δ, switching frequency f and control variable D_c.

7.2.1 Conditions for Operation in Mode I_1

DC analysis equations are valid iff the converter operates in mode I_1 described by the sequence of operating states (7.21). Conditions for operation in mode I_1 are discussed in this section.

Transition from ON-OFF to ON-ON is possible iff there exists $\theta_1 > 0$ such that $v_{off}(\theta_1) = 0$ in the ON-ON state; i.e.,

$$\sqrt{((1-D_c)\delta\theta_p - 1)^2 + \delta^2} \geq 1 \,. \tag{7.31}$$

If this condition is not satisfied, voltage v_{off} does not reach zero and the diode turn-ON at zero voltage is not possible.

The transistor can be turned OFF at zero voltage iff duration of the ON-ON state is non-negative,

$$D_c\theta_p \geq \theta_1 \,. \tag{7.32}$$

In the ON-ON state, the diode ceases to conduct if i_{on} drops to $m\delta$ before the transistor is turned OFF. If this is the case, the circuit enters the ON-OFF state, which is not a viable path in the state transition diagram of Fig. 7.1. This gives rise to the condition $i_{on}(\theta_2) \geq m\delta$, which after substitution of results from DC analysis becomes

$$\sqrt{((1-D_c)\delta\theta_p - 1)^2 + \delta^2 - 1} \geq D_c\theta_p - \theta_1 \,. \tag{7.33}$$

At the transition from the OFF-ON state to the OFF-OFF state, v_{off} must be greater than m. Otherwise, the S-switch would be reverse-biased and, unless the switch is implemented as voltage-bidirectional, the ON-OFF state would be entered again. This condition can be expressed as $m\delta\theta_3 \geq m$, which can be translated into

$$\sqrt{((1-D_c)\delta\theta_p - 1)^2 + \delta^2 - 1} \geq D_c\theta_p - \theta_1 + \frac{1}{\delta} - \delta\,. \tag{7.34}$$

Finally, OFF-ON to OFF-OFF transition must occur before the transistor is turned ON again. Condition $\theta_4 \geq 0$ yields

$$\sqrt{((1-D_c)\delta\theta_p - 1)^2 + \delta^2 - 1} \leq \theta_p - \theta_1 - \delta\,. \tag{7.35}$$

For a given set of parameters δ, θ_p, D_c, a Q_n-PWM converter operates in mode I_1 if all five conditions are satisfied. However, it is easy to verify that for $\delta < 1$, conditions (7.31) and (7.33) are implied by condition (7.34) and that condition (7.35) is implied by condition (7.32). Similarly, for $\delta > 1$, conditions (7.31) and (7.34) are implied by (7.33), while condition (7.32) is implied by (7.35). For $\delta = 1$, conditions (7.33) and (7.34) and likewise (7.32) and (7.35) are equivalent so that (7.31) is again superfluous. Therefore, for any set of parameters, only two conditions need to be checked.

Operating regions for mode I_1 in the load-to-output plane are shown in Fig. 7.3 for switching frequency f as a varying parameter. A procedure for computation of boundary curves is outlined in Appendix B.1. The operating region is a closed portion of the load-to-output plane, resulting in a limited load range and a limited range of attainable conversion ratios. Normalized switching frequency f is a free parameter, which can be selected to optimize the load range, the range of attainable conversion ratios or switch current/voltage stresses. As an example, the choice of switching frequency that maximizes the load range for a given conversion ratio is discussed in the next section.

7.2.2 Maximum Load Range for a Given DC Conversion Ratio

Assuming that parent PWM topology is known, the equivalent duty ratio m can be easily determined from the DC conversion ratio M. For a given normalized frequency f, a minimum load (δ_1) and a maximum load (δ_2) can be found at intersections of the $m = const.$ line with boundary curves for the operating region in mode I_1. Load range

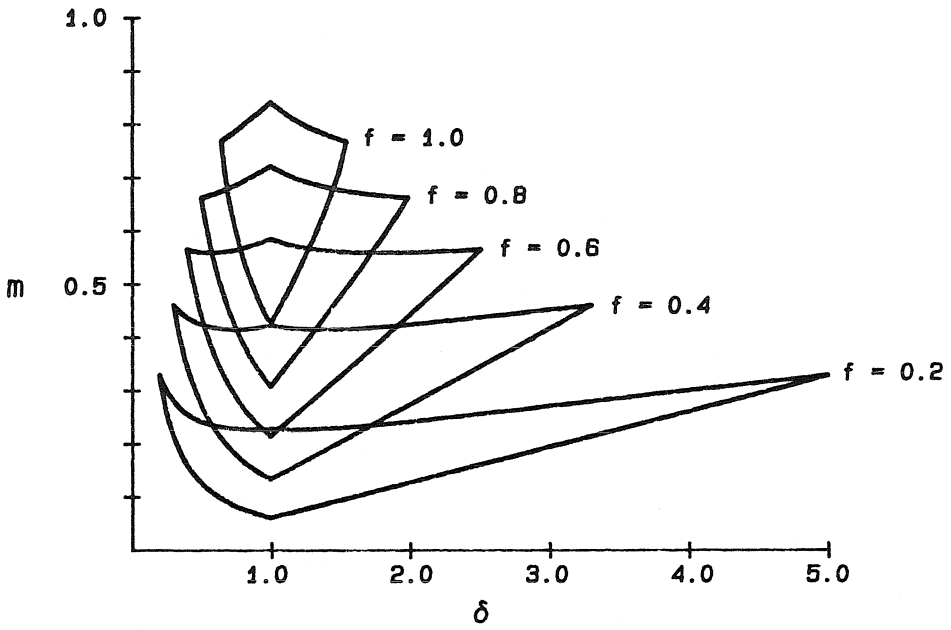


Figure 7.3: Operating region for mode I_1 in the load-to-output plane for switching frequency f as a varying parameter.

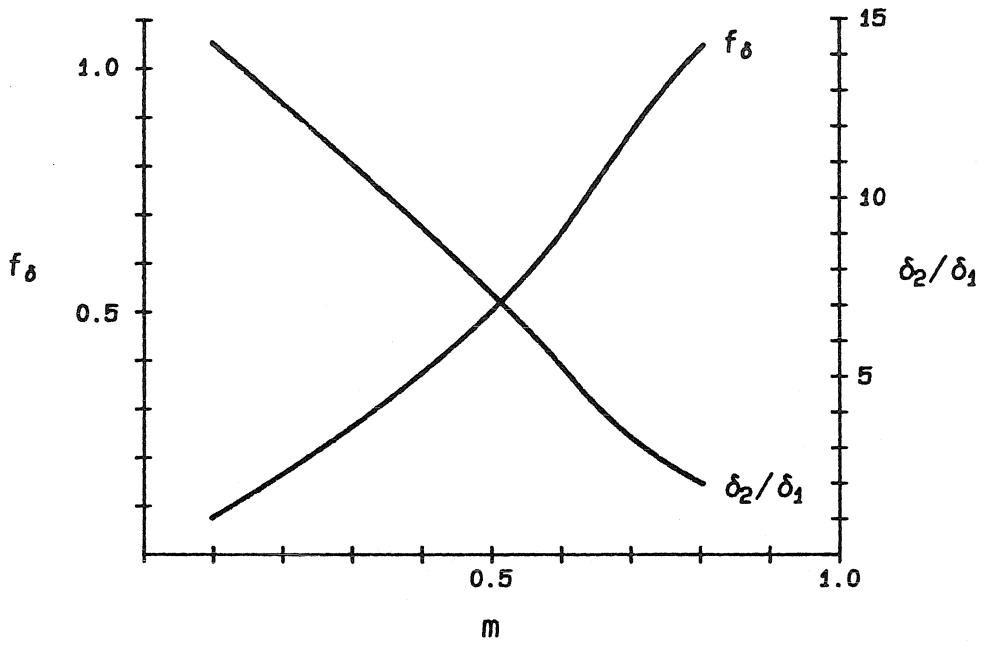
δ_2/δ_1 is then regarded as a function of frequency f. Switching frequency $f_\delta(m)$ for which the load range is largest is found numerically and is plotted in Fig. 7.4(a) as a function of the equivalent duty ratio m. Computational aspects are discussed in Appendix B.1. In the same plot, the maximum achievable load range for $f = f_\delta(m)$ is shown as a decreasing function of the equivalent duty ratio m. The minimum and the maximum load are plotted in Fig. 7.4(b).

7.2.3 DC conversion characteristics

DC conversion characteristics of a Q_n-PWM converter operating in mode I_1 are shown in Figs. 7.5 and 7.6. In contrast to DC characteristics of PWM converters, the characteristics of Q_n-PWM converters are strongly load-dependent.

7.3 Experimental Verification

An experimental Q_n-PWM converter is shown in Fig. 7.7. Parent PWM topology for the experimental circuit is the buck converter with an input filter (converter SD(1)



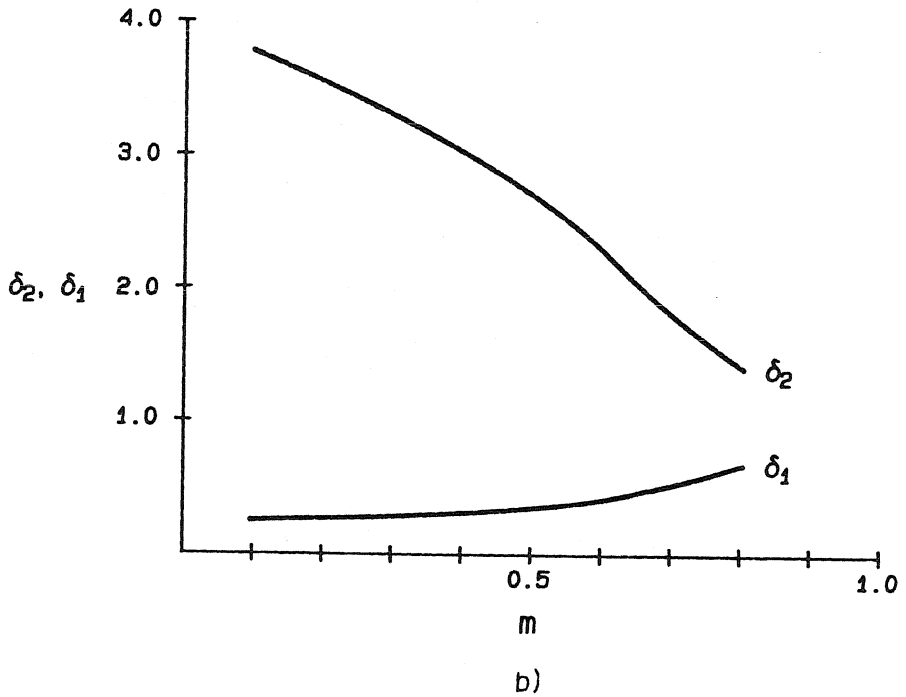


Figure 7.4: Frequency f_δ for which the load range is maximized together with the maximum load range δ_2/δ_1 (a); the minimum load (δ_1) and the maximum load (δ_2) (b).

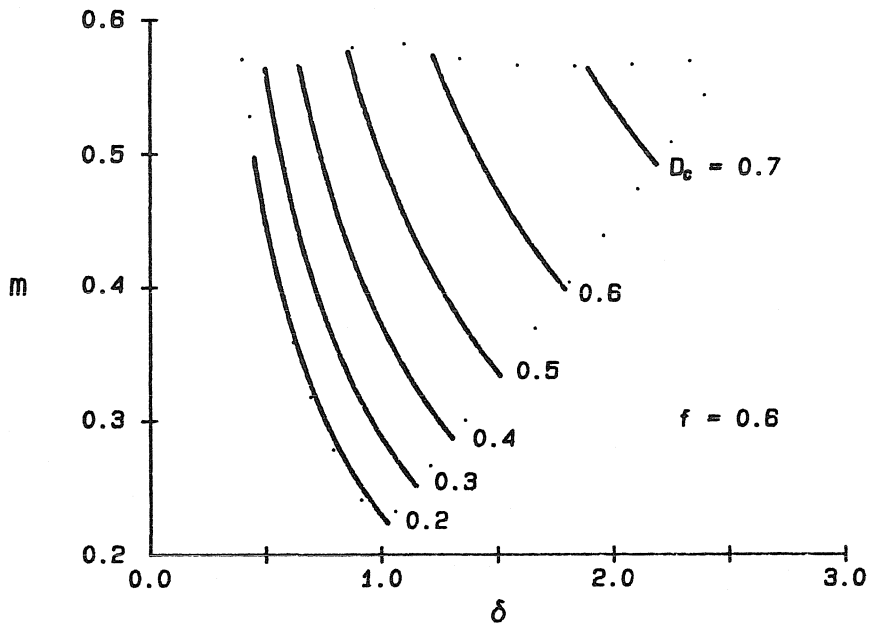


Figure 7.5: Load-to-output characteristics for a Q_n-PWM converter operating in mode I_1.

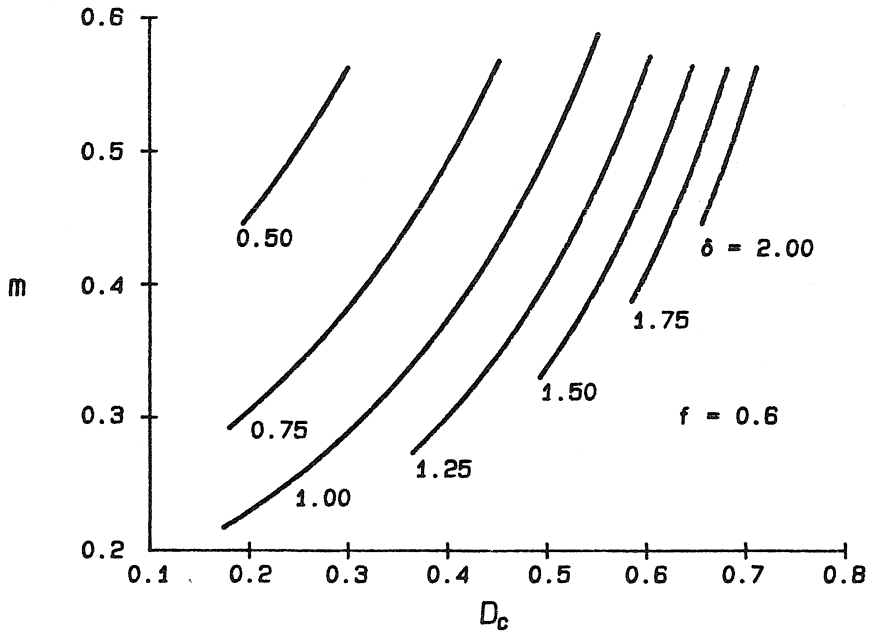


Figure 7.6: Control-to-output characteristics for a Q_n-PWM converter operating in mode I_1.

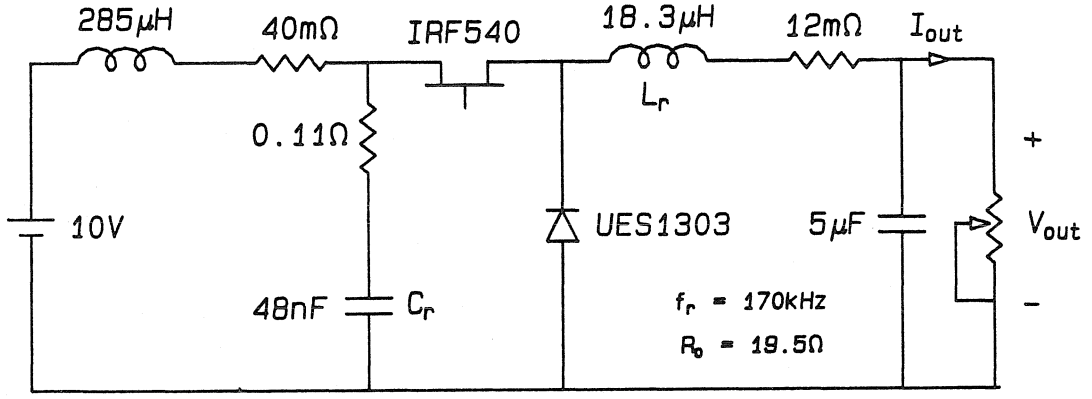
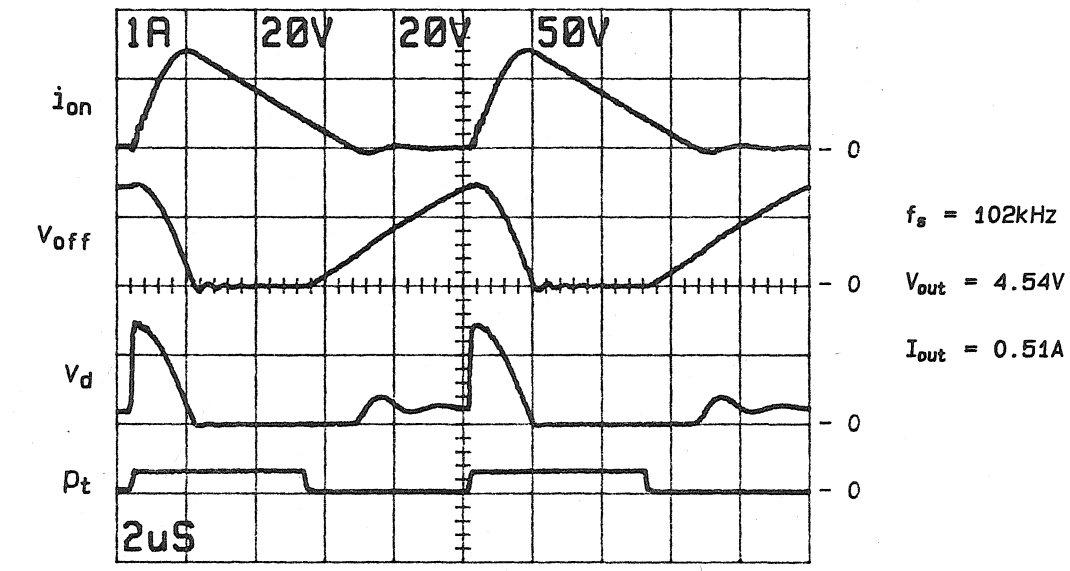


Figure 7.7: An experimental Q_n-PWM buck converter.

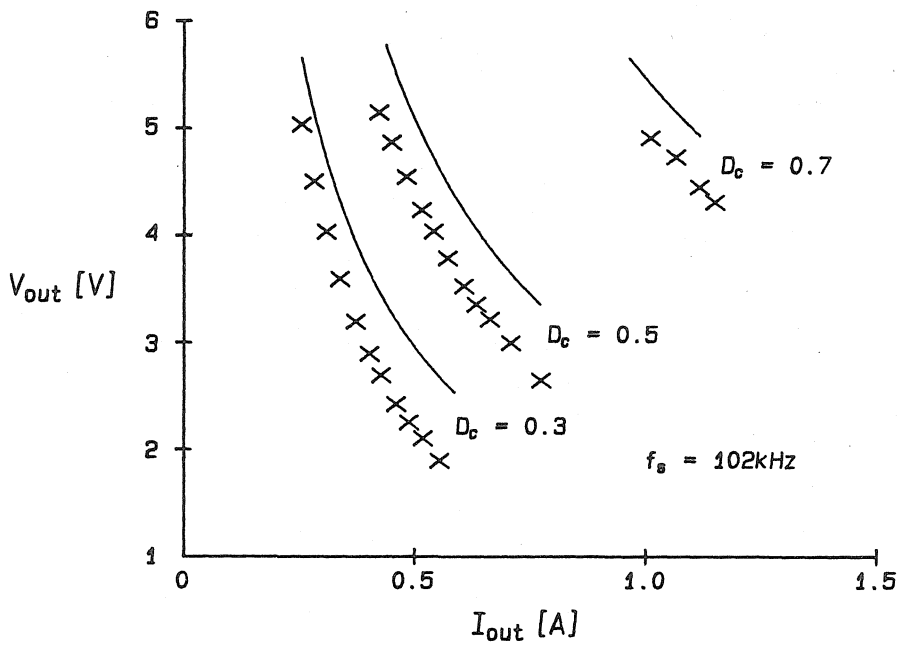
in Fig. 4.13). The DC conversion ratio of the parent converter is $M(D) = D$. Resonant capacitor C_r is placed in series with the capacitor C_2 and then C_2 is absorbed in C_r, using the fact that $C_2 >> C_r$. Similarly, output PWM inductor L_2 is replaced by L_r, which is in the loop with the diode and the output capacitor C_1. Since C_2 and L_2 are the only elements that contribute to V_{off} and I_{on}, respectively, the Q_n-PWM topology is unique.

Waveforms in Fig. 7.8 (a) are recorded under approximately the same operating conditions as for the ideal waveforms of Fig. 7.2 (a). Comparison of waveforms confirms that the circuit indeed operates in mode I_1. The largest discrepancy is observed in the diode voltage v_d. A smooth, damped, resonant response is observed instead of the sharp voltage step during the turn-OFF transition of the diode. The observed resonance is between the resonant inductor L_r and the parasitic capacitances of the semiconductor switches. The parasitic capacitances were not accounted for in the analysis. Peak-to-peak current ripple in the input inductor ($285\mu H$), taken as zero in the analysis, was approximately $80mA$ in the actual circuit.

Discrepancies between measured and predicted DC characteristics in Fig. 7.8 (b) can be ascribed to losses in the experimental circuit and to observed distortion in the diode voltage waveform. Both effects were neglected in the analysis.



a)



b)

Figure 7.8: Recorded waveforms (a) and measured and predicted DC characteristics (b) for the experimental Q_n-PWM buck converter operating in mode I_1.

The transistor switch is driven by constant-frequency pulses p_t. The DC conversion ratio is controlled by varying the duty ratio of p_t.

Chapter 8

Zero-Voltage Converters

A study of Zero-Voltage (ZV) converters is undertaken in this chapter.

In the implementation with one controllable, current-bidirectional switch, an operating mode (I_1) with all transitions at zero voltage or at zero current is unique. In this mode, which is known as the half-wave mode [14], output voltage can be controlled only by varying the switching frequency. DC analysis for ZV converters operating in mode I_1 is presented in Section 8.3 for completeness. It is in agreement with results obtained in [20].

Original results are obtained for two operating modes, I_2 and II_2, with all transitions at zero voltage or at zero current and the implementation with two controllable, current-bidirectional switches. Most importantly, constant-frequency control is applicable in both modes, and closed-form analytical solutions for DC characteristics are found in Section 8.4. The operating region for mode I_2 is very restricted – only a very limited range of equivalent duty ratios is accessible. The operating region for mode II_2 is much broader. It is bounded in the load direction but it includes the zero-load axis.

Existence of operating modes and results of DC analysis are verified experimentally in Section 8.5.

8.1 Operating States

By definition of the ZV class, resonant capacitor C_r, the S-switch and possibly elements of $\mathcal{C} \cup \{V_g\}$ form a loop. Since elements of $\mathcal{C} \cup \{V_g\}$ carry DC voltages only,

$$\frac{dv_t}{d\theta} = \frac{dv_{C_r}}{d\theta}. \tag{8.1}$$

Furthermore, every cut-set that contains the S-switch must contain at least one element from $\mathcal{C} \cup \{V_g\} \cup \{C_r\}$. In particular, the cut-set of Proposition 3.7 contains no elements

in $\mathcal{C} \cup \{V_g\}$, so that it must contain C_r. Therefore,

$$i_t + i_d + \frac{dv_t}{d\theta} = \delta \,. \tag{8.2}$$

By dual arguments, it follows that

$$\frac{di_d}{d\theta} + \frac{di_{L_r}}{d\theta} = 0 \,. \tag{8.3}$$

Consequently,

$$v_t + v_d - \frac{di_d}{d\theta} = 1 \,. \tag{8.4}$$

Starting from Eqs. (8.2) and (8.4), equations and solutions for possible operating states are written in terms of state variables v_t and i_d as follows:

ON-ON state: $v_t = 0$, $v_d = 0$.

Equations:

$$\frac{di_d}{d\theta} = -1 \,,\; i_d(0) = I_{nn} \,. \tag{8.5}$$

Solution:

$$v_t = 0 \,, \tag{8.6}$$

$$i_d = I_{nn} - \theta \,. \tag{8.7}$$

ON-OFF state: $v_t = 0$, $i_d = 0$. This is simultaneously the solution for this state.

OFF-ON state: $i_t = 0$, $v_d = 0$.

Equations:

$$\frac{di_d}{d\theta} = v_t - 1 \,,\; i_d(0) = I_{fn} \,, \tag{8.8}$$

$$\frac{dv_t}{d\theta} = -i_d + \delta \,,\; v_t(0) = V_{fn} \,. \tag{8.9}$$

Solution:

$$v_t = 1 + (V_{fn} - 1)\cos\theta + (\delta - I_{fn})\sin\theta \,, \tag{8.10}$$

$$i_d = \delta + (I_{fn} - \delta)\cos\theta + (V_{fn} - 1)\sin\theta \,. \tag{8.11}$$

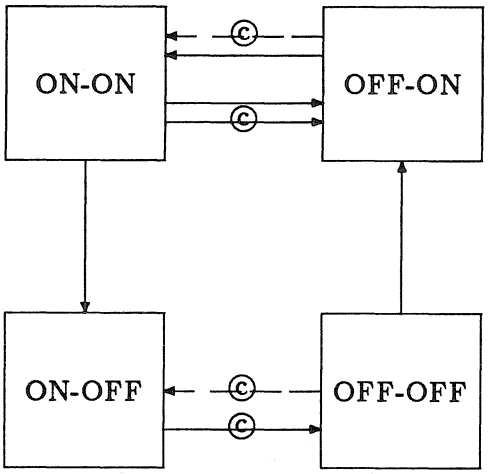


Figure 8.1: State transition diagram for ZV converters with a single, controllable, current-bidirectional switch.

OFF-OFF state: $i_t = i_d = 0$.

Equations:

$$\frac{dv_t}{d\theta} = \delta \ , \ v_t(0) = V_{ff} \, . \tag{8.12}$$

Solution:

$$v_t = V_{ff} + \delta\theta \, , \tag{8.13}$$

$$i_d = 0 \, . \tag{8.14}$$

8.2 Operating Modes

Implementations with a single controllable switch and with two controllable switches are studied separately.

8.2.1 Implementation with a Single Controllable Switch

If the S-switch is a controllable, current-bidirectional switch and the $\hat{S}$-switch is a diode, the state transition diagram of a ZV converter is shown in Fig. 8.1. The S-switch turn-OFF transitions are controllable and occur at zero voltage. Controllable turn-ON transitions are necessarily at non-zero voltage. The diode switch turns OFF at zero current and ON at zero voltage and zero current but, of course, none of the transitions is controllable.

The periodic sequence,

$$\text{Mode } I\text{: } \cdots \rightarrow \boxed{\text{OFF-OFF}} \rightarrow \boxed{\text{OFF-ON}} \rightarrow \boxed{\text{ON-ON}} \rightarrow \boxed{\text{ON-OFF}} \rightarrow \cdots \tag{8.15}$$

defines the only operating mode for which all transitions are at zero voltage and/or at zero current so that switching losses are minimized. Only one transition (transistor turn-OFF) in the sequence is controllable. Therefore, only variable-frequency control can be applied.

Assume that initially the converter is in the ON-OFF state. Both state variables are equal to zero. The OFF-OFF state is entered by turning the S-switch OFF. In the OFF-OFF state, v_t ascends linearly until the diode-switch voltage drops to zero and the diode starts to conduct at $\theta = \theta_1$. Initial conditions for the OFF-ON state are $I_{ff} = 0$ and $V_{fn} = v_{t1} = 1$. The resonant (OFF-ON) state is completed when the S-switch voltage drops to zero at $\theta = \theta_2$ and the antiparallel diode in the S-switch starts to conduct. The initial condition for the succeeding ON-ON state is $I_{nn} = i_{d2}$. In the ON-ON state, the diode current descends linearly until it reaches zero at $\theta = \theta_3$. The converter remains in the ON-OFF state until the S-switch is turned OFF again and the switching cycle is completed at $\theta = \theta_4$.

Waveforms typical for a variable-frequency ZV converter operating in mode I_1 are shown in Fig. 8.2. The hatched portion of the control signal p_t for the transistor in the S-switch denotes the interval when the state of the transistor is irrelevant since the antiparallel diode is conducting. Thus, the transistor can be turned ON at zero voltage during the entire hatched interval.

8.2.2 Implementation with Two Controllable Switches

If both S and $\hat{S}$ are implemented as controllable, current-bidirectional switches, the augmented state transition diagram is shown in Fig. 8.3. In addition to the sequence of mode I, there is another periodic sequence,

$$\text{Mode } II\text{: } \cdots \rightarrow \boxed{\text{ON-OFF}} \rightarrow \boxed{\text{ON-ON}} \rightarrow \boxed{\text{OFF-ON}} \rightarrow \boxed{\text{ON-ON}} \rightarrow \cdots, \tag{8.16}$$

with all zero-voltage or zero-current transitions, two of which are controllable.

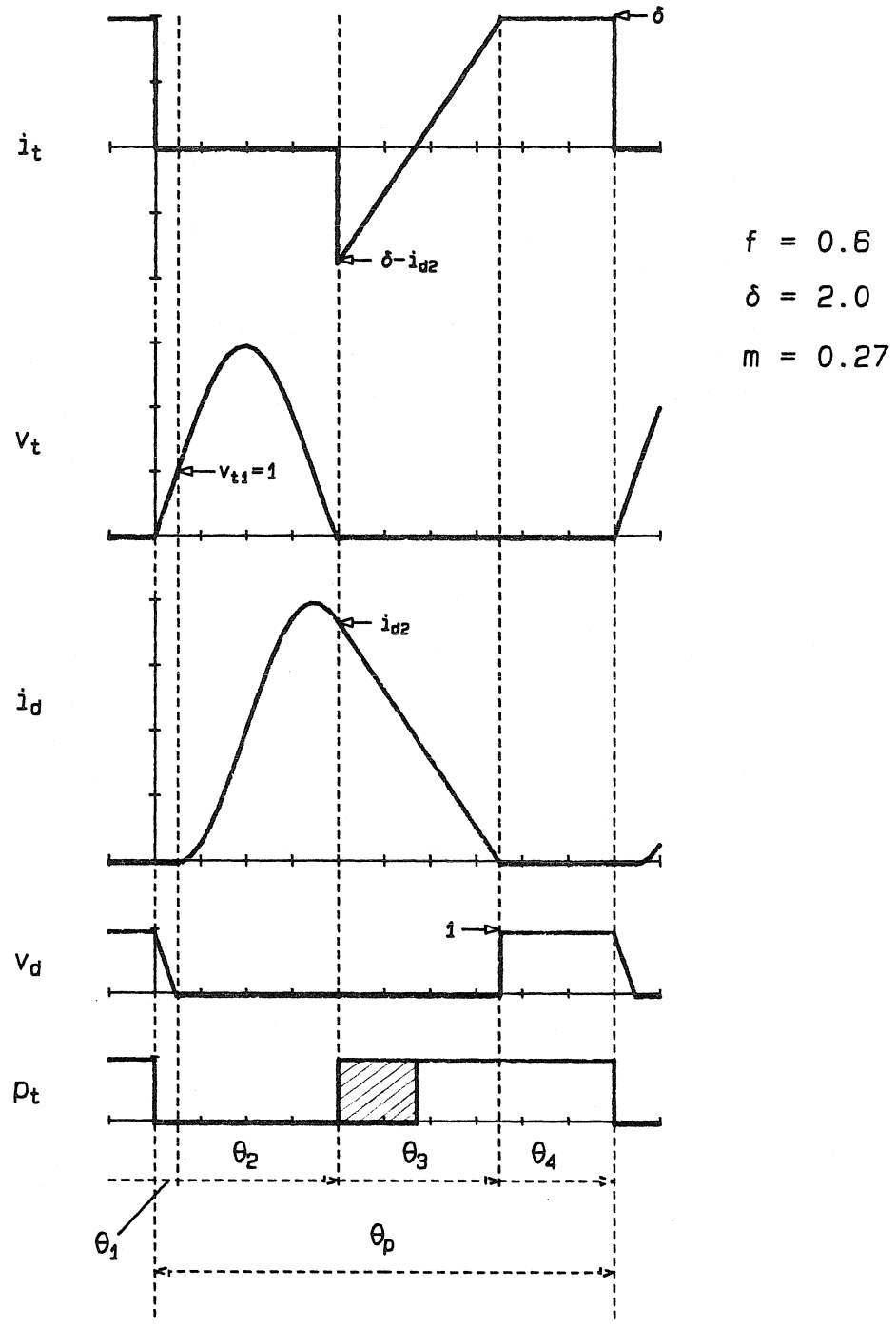


Figure 8.2: Typical waveforms in a ZV converter operating in mode I_1.

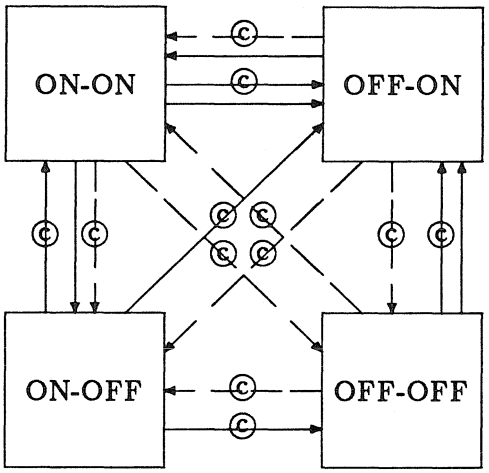


Figure 8.3: State transition diagram for ZV converters with two controllable, current-bidirectional switches.

Operation in mode I_2 is quite similar to operation of converters with a single controllable switch in mode I_1. The only difference is that the $\hat{S}$-switch can be turned ON at non-zero voltage (but still at zero current) so that the initial condition for the OFF-ON state is $V_{fn} = v_{t1} < 1$.

Control duty ratio D_{c1} for mode I_2 is defined as the interval between the S-switch turn-OFF and the $\hat{S}$-switch turn-ON, relative to the switching period,

$$D_{c1} \equiv \theta_1/\theta_p\,. \tag{8.17}$$

In the operating mode II_2, the ON-ON state is entered twice inside a single switching cycle. Transition from the ON-OFF to the ON-ON state is controllable by the $\hat{S}$-switch turn-ON, while transition from the OFF-ON to the ON-ON state is determined by the circuit waveforms. Assume that initially the converter is in the ON-OFF state and that the $\hat{S}$-switch is turned ON at the beginning of the switching cycle, at *zero current*. In the ON-ON state, i_d descends linearly until the S-switch is turned OFF at $\theta = \theta_1$, at *zero voltage*. The resonant OFF-ON state terminates when the S-switch voltage reaches zero again and the ON-ON state is re-entered. It is assumed that the transistor in the $\hat{S}$-switch is turned OFF while i_d is positive. Thus, when i_d reaches zero at $\theta = \theta_3$, the antiparallel diode in $\hat{S}$ turns OFF at *zero current* so that the final ON-OFF state is entered. The transistor in the S-switch has to be turned ON before i_t becomes positive. The cycle is completed when the $\hat{S}$-switch is turned ON again at $\theta = \theta_4$.

Control duty ratio D_{c2} for mode II_2 is defined as the interval between the $\hat{S}$-switch turn-ON and the S-switch turn-OFF, relative to the switching period,

$$D_{c2} \equiv \theta_1/\theta_p\,. \tag{8.18}$$

It should be noted that for $D_{c1} = D_{c2} = 0$, both operating modes reduce to the periodic sequence

$$\cdots \rightarrow \boxed{\text{ON-OFF}} \rightarrow \boxed{\text{OFF-ON}} \rightarrow \boxed{\text{ON-ON}} \rightarrow \cdots\,. \tag{8.19}$$

Thus, a unique control-variable D_c for both modes can be defined by

$$D_c \equiv \begin{cases} -D_{c1} & \text{in mode } I_2\,, \\ D_{c2} & \text{in mode } II_2\,. \end{cases} \tag{8.20}$$

Typical waveforms for a ZV converter with two controllable switches operating in modes I_2 and II_2 are shown in Fig. 8.4. p_t and p_d denote control waveforms for the transistor in the S-switch and for the transistor in the $\hat{S}$-switch, respectively. Hatched areas in the control waveforms indicate intervals where the state of the corresponding transistor is irrelevant for operation of the circuit.

8.3 Variable-Frequency Control: DC Analysis

Assume that a ZV converter operates in mode I_1 and that transition from the ON-OFF to the OFF-OFF state is at the beginning of a switching cycle. Initial conditions for the OFF-OFF state are $I_{ff} = 0$ and $V_{ff} = 0$. At $\theta = \theta_1$, transistor voltage v_t reaches 1 and the diode starts to conduct. For the OFF-OFF state, $v_t(\theta_1) = 1$ is solved for θ_1,

$$\theta_1 = \frac{1}{\delta}\,. \tag{8.21}$$

During the OFF-ON state, the S-switch voltage and the diode current are shaped by the resonance between elements L_r and C_r. Initial conditions for the state are $V_{fn} = 1$ and $I_{fn} = 0$. Transition to the ON-ON state occurs when the S-switch voltage drops to zero, and its antiparallel diode starts to conduct. Assuming that it is possible to solve the equation $v_t(\theta_2) = 0$ for θ_2, the solution is given by

$$\theta_2 = \pi + \arctan\frac{1}{\sqrt{\delta^2 - 1}}\,, \tag{8.22}$$

$$i_{d2} = \delta + \sqrt{\delta^2 - 1}\,. \tag{8.23}$$

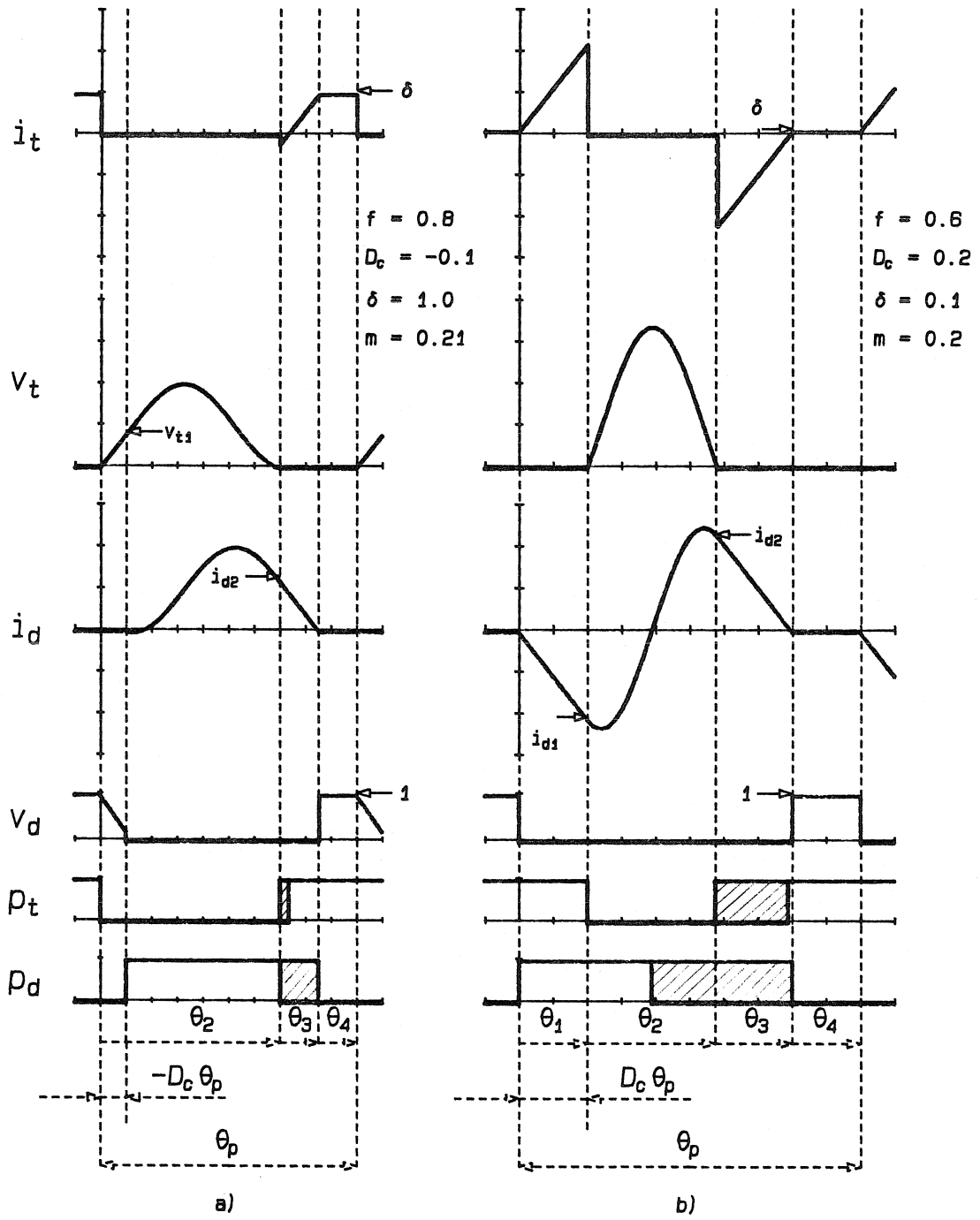


Figure 8.4: Typical waveforms in a ZV converter operating in modes I_2 (a) or II_2 (b).

During the ON-ON state, i_d drops linearly from i_{d2} to zero at $\theta = \theta_3$, when the ON-OFF state is entered. Thus,

$$\theta_3 = i_{d2}\,. \tag{8.24}$$

Finally, the ON-OFF state lasts until the S-switch is turned OFF again at $\theta = \theta_4$.

The equivalent duty ratio m for frequency-controlled ZV converters can be found by averaging the transistor voltage over one switching cycle and substituting for θ_1 and θ_2 from Eqs. (8.21) and (8.22). The final result is:

$$m = 1 - \frac{f}{2\pi}\left[\pi + \frac{1}{2\delta} + \arctan\frac{1}{\sqrt{\delta^2-1}} + \delta + \sqrt{\delta^2-1}\right] = 1 - G_1(\delta)f\,. \tag{8.25}$$

8.3.1 Conditions for Operation in Mode I_1

Results of the DC analysis are valid if the converter operates in mode I_1. Conditions for operation in this mode are discussed in this section.

Solution (8.22) for θ_2 exists iff

$$\delta \geq 1\,. \tag{8.26}$$

Thus, for operation in mode I_1, normalized load current must be greater than one. This excludes frequency-controlled ZV converters from applications where operation at zero load is required.

The upper limit on the switching frequency f is determined by the fact that θ_1 must be non-negative. Using the results of the DC analysis, this condition is translated into the minimum achievable m for any given load $\delta \geq 1$,

$$m \geq m_{min} = \frac{\frac{1}{2\delta}}{\pi + \frac{1}{\delta} + \arctan\frac{1}{\sqrt{\delta^2-1}} + \delta + \sqrt{\delta^2-1}}\,. \tag{8.27}$$

Together with $m \leq 1$, which must be satisfied by definition, conditions (8.26) and (8.27) are necessary and sufficient for operation in mode I_1. The operating region for mode I_1 is depicted in Fig. 8.5.

8.3.2 DC conversion characteristics

The equivalent duty ratio is found in the form $m = 1 - G_1(\delta)f$, where effects of load variations on m are exposed through the function $G_1(\delta)$ shown in Fig. 8.6. It is

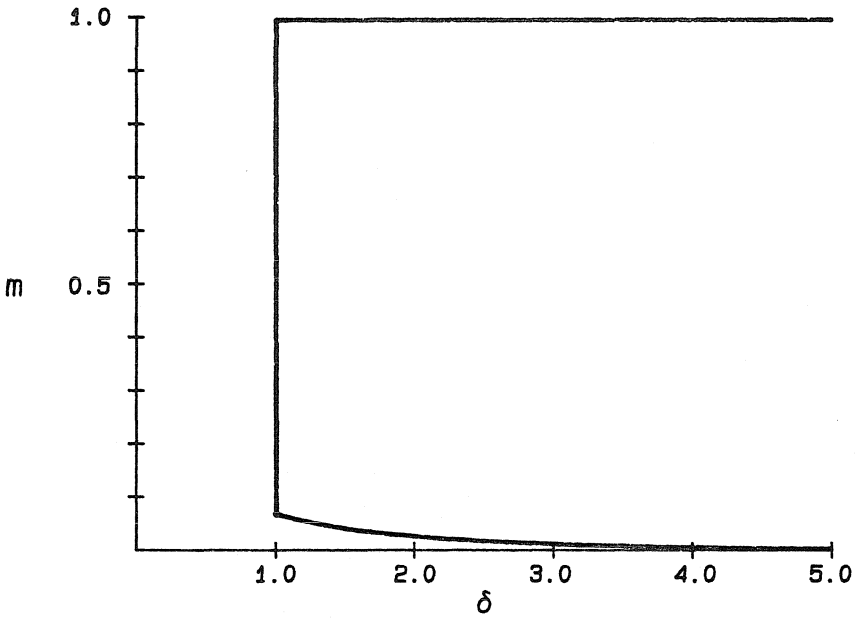


Figure 8.5: Operating region for ZV converters in mode I_1.

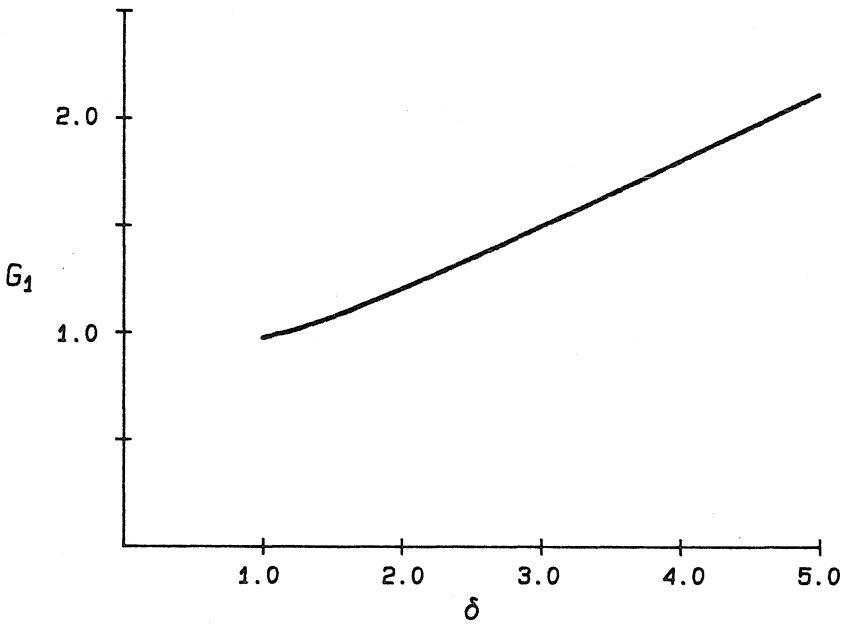


Figure 8.6: Function G_1 for ZV converters operating in mode I_1.

tempting to examine how close G_1 is to its large-δ asymptote, $(0.5 + \delta/\pi)$. Relative error is largest (17%) for $\delta = 1$, and it drops below 10% for $\delta > 1.5$. For all practical purposes this is sufficient to approximate the equivalent duty ratio m with a family of linear characteristics,

$$m \approx 1 - 0.5f - \frac{1}{\pi}\delta f\,, \tag{8.28}$$

in the load-to-output and control-to-output planes.

8.4 Constant-Frequency Control: DC Analysis

8.4.1 Operating Mode I_2

In the operating mode I_2, the same sequence of states is traversed as in I_1. However, duration of the OFF-OFF state is now controllable,

$$\theta_1 = \theta_c = -D_c\theta_p\,, \tag{8.29}$$

and the S-switch voltage at the end of the OFF-OFF state is

$$v_{t1} = \delta\theta_c\,. \tag{8.30}$$

With initial conditions $I_{fn} = 0$ and $V_{fn} = v_{t1}$, the solution for the OFF-ON state is

$$\theta_2 = \pi + \arctan\frac{1 - v_{t1}}{\delta} + \arctan\frac{1}{\sqrt{(1 - v_{t1})^2 + \delta^2 - 1}}\,, \tag{8.31}$$

$$i_{d2} = \sqrt{(1 - v_{t1})^2 + \delta^2 - 1} + \delta\,, \tag{8.32}$$

if existence conditions are satisfied. Duration of the ON-ON state is the same as before $(\theta_3 = i_{d2})$, and duration of the ON-OFF state is determined from the constant-frequency condition

$$\theta_4 = \theta_p - \theta_c - \theta_2 - \theta_3\,. \tag{8.33}$$

Finally, the expression for the equivalent duty ratio m is obtained by equating the average of the S-switch voltage over one switching cycle to $1 - m$,

$$\begin{aligned} m = 1 - \frac{f}{2\pi}\Bigg[&\frac{\delta\theta_c^2}{2} + \pi + \arctan\frac{1 - \delta\theta_c}{\delta} + \\ &+ \arctan\frac{1}{\sqrt{(1 - \delta\theta_c)^2 + \delta - 1}} + \sqrt{(1 - \delta\theta_c)^2 + \delta - 1} + \delta\Bigg]\,, \end{aligned} \tag{8.34}$$

or

$$m = 1 - G_2(\delta, \theta_c) f \,. \tag{8.35}$$

It is easy to see that for $\delta\theta_c = 1$, this result reduces to result (8.25) found for frequency-controlled converters.

Conditions for Operation in Mode I_2

If the $\hat{S}$-switch is not turned-ON before the $\hat{S}$-switch voltage drops to zero in the OFF-ON state, the converter operates in mode I_1, i.e., with only one controllable transition. Thus, for operation in mode I_2, it is necessary that

$$\delta\theta_c \leq 1 \,. \tag{8.36}$$

The solution for θ_2 exists iff $\delta^2 + (1 - \delta\theta_c)^2 \geq 1$, or

$$\delta\theta_c \leq 1 - \sqrt{1 - \delta^2}, \quad \text{if } 0 \leq \delta < 1 \,. \tag{8.37}$$

Another condition is that duration of the ON-ON state is non-negative,

$$\theta_4 \geq 0 \,. \tag{8.38}$$

Assume that switching frequency is chosen so that the last condition is always satisfied. The function $G_2(\delta, \theta_c)$ attains its minimum value, G_{2min}, for $\theta_c = 0$ and its maximum value, G_{2max}, for θ_c that satisfies equality in Eq. (8.36) for $\delta \geq 1$ or in Eq. (8.37) for $0 \leq \delta < 1$. G_{2min} and G_{2max} are evaluated and plotted in Fig. 8.7 as functions of the load current δ. It is evident that the available control range in mode I_2 is severely limited for any normalized switching frequency f.

8.4.2 Operating Mode II_2

Assume that transition from the ON-OFF state to the ON-ON state is at the beginning of a switching cycle. The initial condition for the first ON-ON state is $I_{nn} = 0$. The state is terminated after the S-switch is turned OFF at $\theta = \theta_c = D_c\theta_p$. At the end of the ON-ON state, the $\hat{S}$-switch current is

$$i_{d1} = -\theta_c \,. \tag{8.39}$$

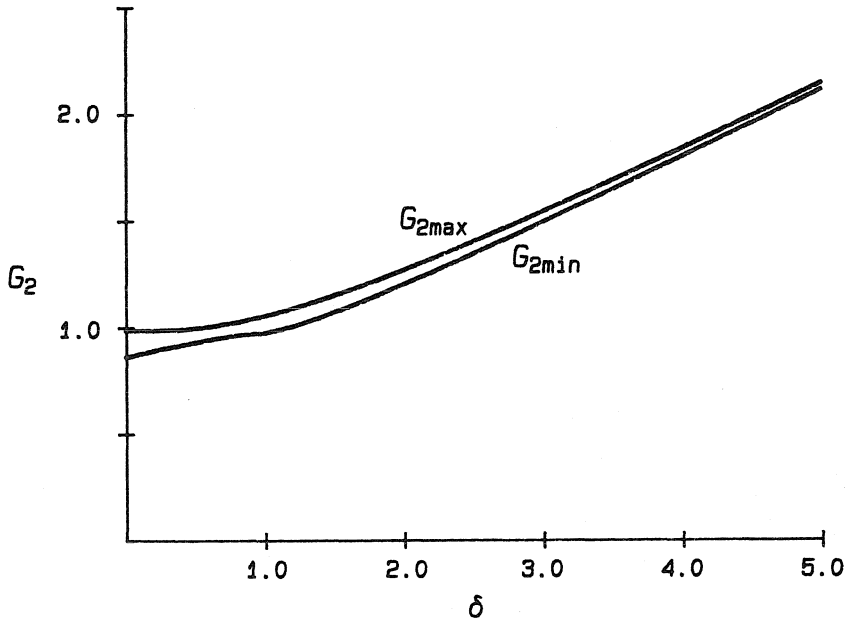


Figure 8.7: Extreme values of the function $G_2(\delta, \theta_c)$ for ZV converters operating in mode I_2.

The OFF-ON state, which is the resonant state, starts with $V_{fn} = 0$ and $I_{fn} = i_1$ and ends after the S-switch voltage returns to zero at $\theta = \theta_2$. If the solution to $v_t(\theta_2) = 0$ exists, it is given by

$$\theta_2 = 2\pi - 2\arctan(\delta + \theta_c) \tag{8.40}$$

$$i_{d2} = \theta_c + 2\delta\,. \tag{8.41}$$

In the second ON-ON state, current i_d decreases linearly from $I_{nn} = i_{d2}$ to zero at $\theta = \theta_3$. Hence,

$$\theta_3 = i_{d2}\,. \tag{8.42}$$

Finally, the ON-OFF state lasts until the end of the switching period:

$$\theta_4 = \theta_p - \theta_1 - \theta_2 - \theta_3\,. \tag{8.43}$$

By taking the average of voltage v_t over one switching cycle, the equivalent duty ratio m is obtained in closed form,

$$m = 1 - \frac{f}{\pi}\left[\pi - \arctan(\delta + \theta_c) + \delta + \theta_c\right] = 1 - G_3(\delta, \theta_c) f = 1 - G_3'(\delta + \theta_c) f\,. \tag{8.44}$$

Conditions for Operation in Mode II_2

Since $\delta \geq 0$ and $\theta_2 \geq 0$ by assumption, the equation $v_t(\theta_2) = 0$ in the OFF-ON state can be solved for θ_2 always. Except for the implicitly assumed condition $0 \leq m \leq 1$, the only further requirement for operation in mode II_2 is that the length of the ON-OFF is non-negative,

$$\theta_4 \geq 0\,, \tag{8.45}$$

but it is equivalent to $m \leq 1$.

From Eq. (8.44), it follows that the maximum possible m for a ZV converter operating in mode II_2 is

$$m_{max} = 1 - f\,. \tag{8.46}$$

The maximum m is attained for $D_c = \theta_c/\theta_p = 0$ and zero load. On the other hand, the equivalent duty ratio collapses to zero for load and control variables that satisfy

$$\delta + \theta_c = G_3'^{-1}(\frac{1}{f})\,. \tag{8.47}$$

Here, $G_3'^{-1}(\cdot)$ denotes the inverse of the function $G_3'(\cdot)$.

DC conversion characteristics

The equivalent duty ratio m in Eq. (8.44) is a function of the sum of the load current δ and the control variable $\theta_c = D_c\theta_p$. The function $G'(\delta + \theta_c)$ is plotted in Fig. 8.8.

8.5 Experimental Verification

In this section, existence of operating modes I_1 and II_2 and predicted DC characteristics are verified using an experimental ZV converter of Fig. 8.9. Parent PWM topology is the second-order buck converter with $M(D) = D$. Switch $\hat{S}$ is implemented as a diode (1) or as a MOS transistor (2). The resonant capacitor C_r is placed in parallel with the S-switch, which is a MOS transistor in both cases. The resonant inductor L_r forms a cut-set with $\hat{S}$ and the output inductor ($285\mu H$). A resistor (390Ω) is added in parallel with the resonant inductor to damp undesirable resonance with a parasitic capacitor of the $\hat{S}$-switch.

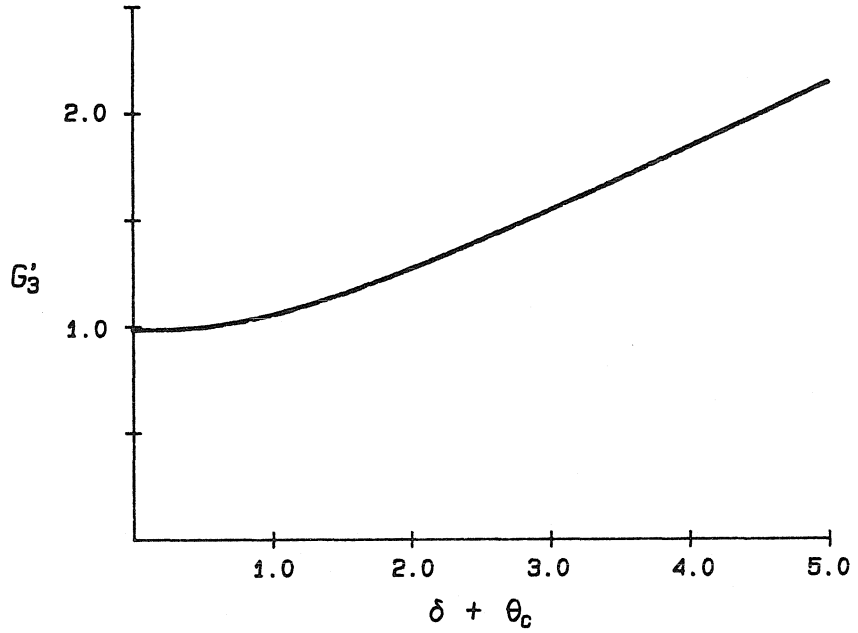


Figure 8.8: Function $G_3'(\delta + \theta_c)$ for ZV converters operating in mode II_2.

Evidently, the ZV converter constructed from the buck PWM parent is not unique. Nevertheless, experimental results for DC characteristics are within marginal errors identical for several variations of the ZV buck topology corresponding to different positions of C_r and L_r. With $\hat{S}$ implemented as a diode, waveforms in Fig. 8.10 (a) are recorded for approximately the same operating conditions as ideal waveforms of Fig. 8.2. The comparison confirms that the circuit operates in mode I_1, which is already well documented [14]. Without the damping resistor, the diode voltage exhibits weakly damped oscillations in place of the sharp transition in ideal waveforms. Otherwise, waveforms are in excellent agreement with the prediction.

Slight discrepancies between measured and predicted DC characteristics in the load-to-output plane of Fig. 8.10 (b) are due to the fact that all losses were ignored in the idealized DC analysis.

When the ZV converter operates in mode I_1, control circuitry provides variable-frequency, constant-pause pulses (p_t) to drive the transistor switch.

With the $\hat{S}$-switch implemented as a MOS transistor, mode II_2 is verified by comparison of recorded waveforms in Fig. 8.11 (a) and ideal waveforms of Fig. 8.4 (b). Again, the

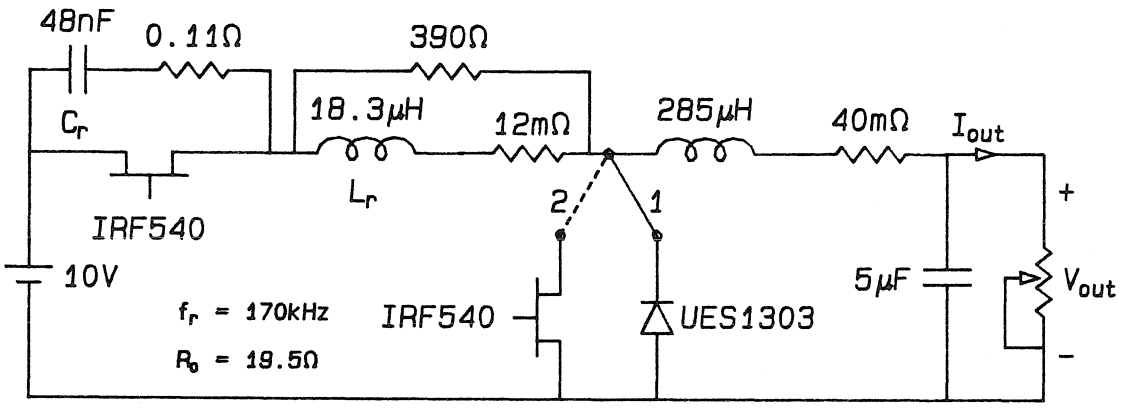
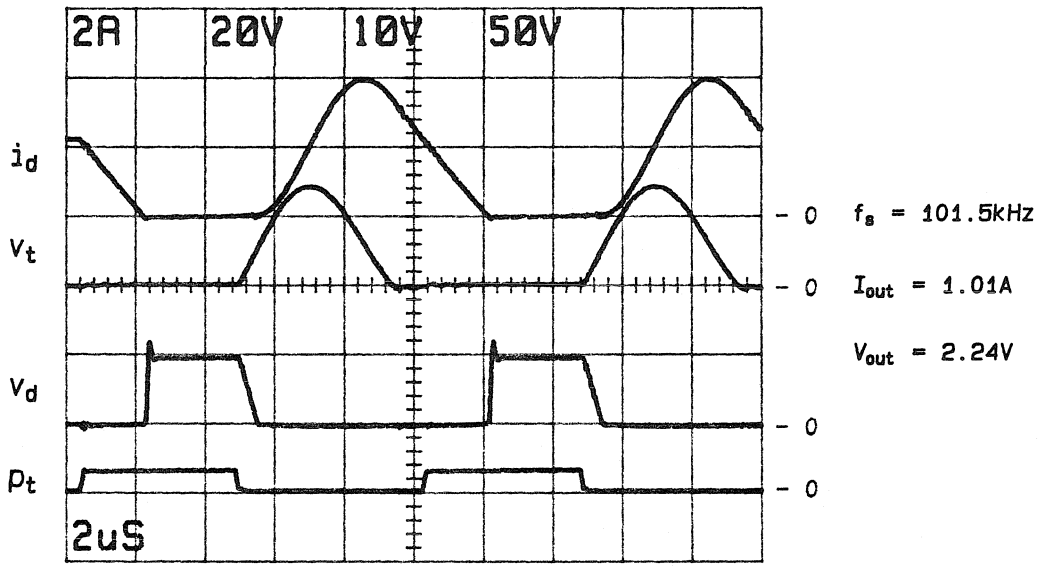


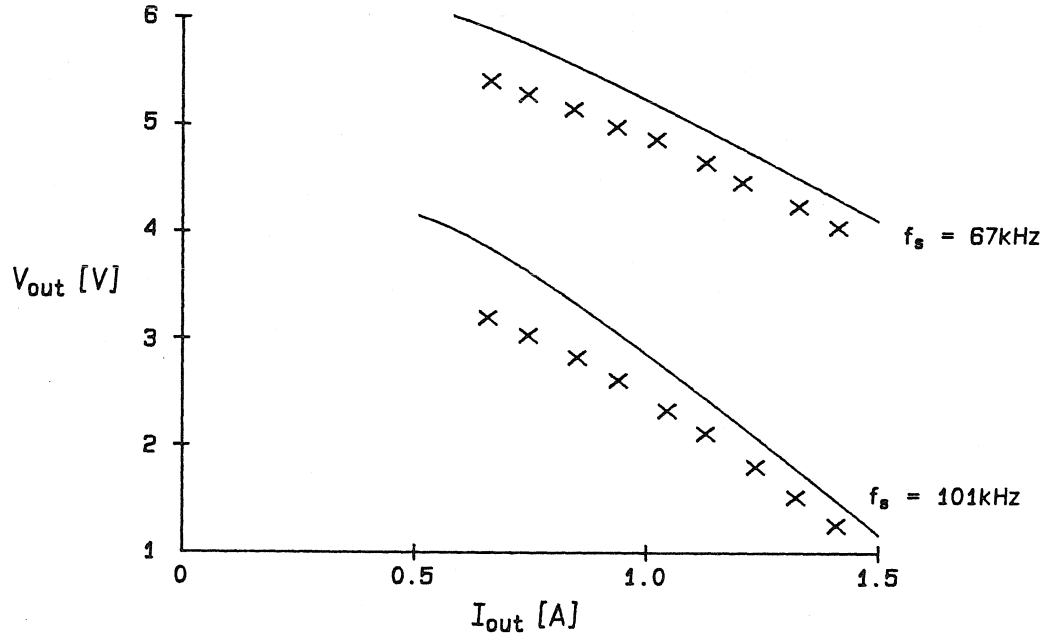
Figure 8.9: An experimental ZV buck converter.

only observable difference is in the diode voltage waveform. It should be noted that the employed MOS transistor has a larger parasitic capacitance than the diode used in mode I_1 so that parasitic oscillations are less damped and more energy is lost in mode II_2. Nevertheless, a satisfactory agreement between measured and ideal DC characteristics is demonstrated in Fig. 8.11 (b).

Control circuitry for the converter in mode II_2 provides constant-frequency, constant-pause pulses (p_t) to drive the S-switch transistor and constant-frequency, variable-duty-ratio pulses (p_d) to drive the $\hat{S}$-switch transistor. The falling edge of p_d and the raising edge of p_t are synchronized.



a)



b)

Figure 8.10: Recorded waveforms (a) and measured and predicted DC characteristics (b) for the experimental ZV buck converter operating in mode I_1.

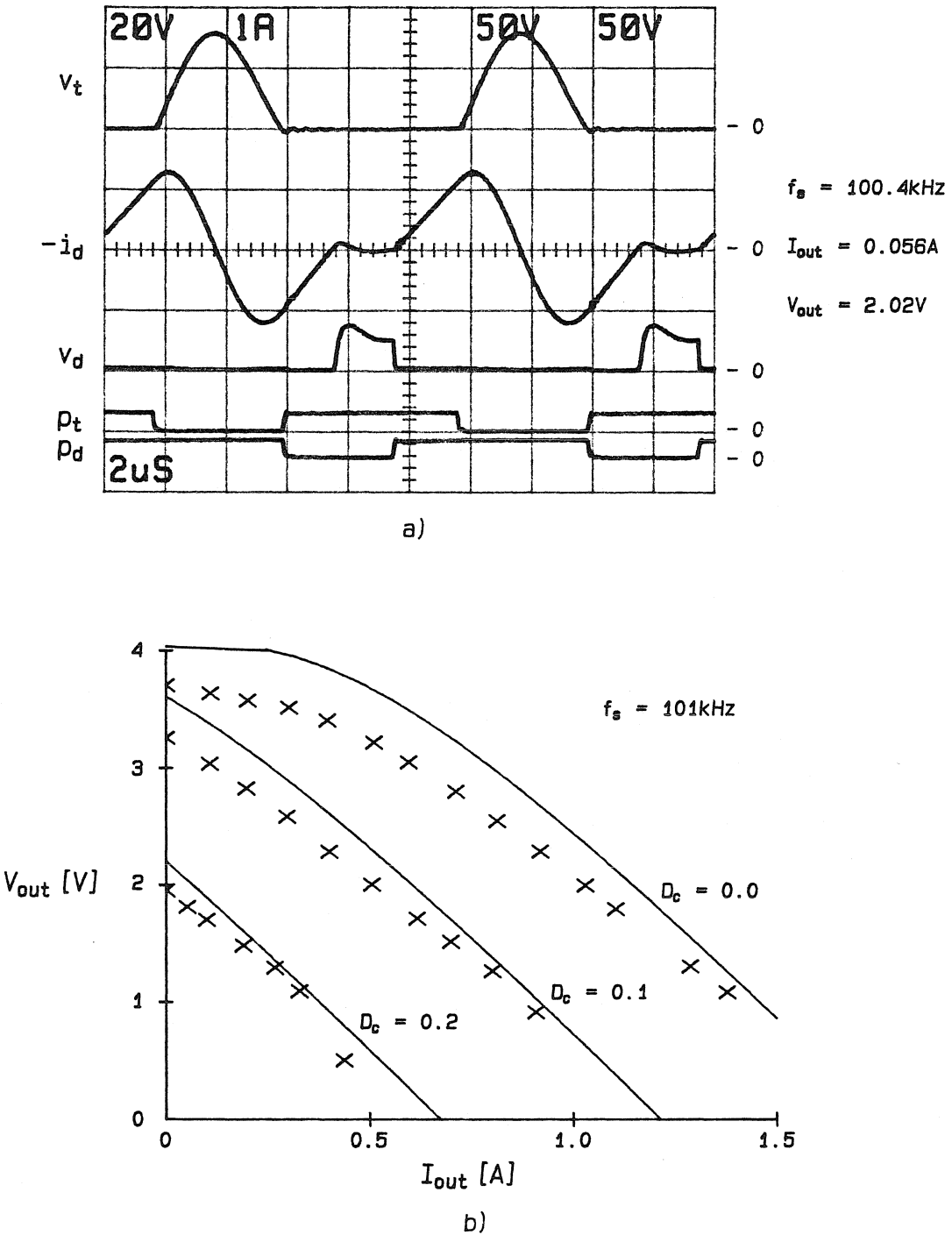


Figure 8.11: Recorded waveforms (a) and measured and predicted DC characteristics (b) for the experimental ZV buck converter operating in mode II_2.

Chapter 9

Zero-Voltage, Quasi-Square-Wave Converters

Zero-Voltage, Quasi-Square-Wave (ZV-QSW) converters are studied in this chapter.

A unique operating mode with all transitions at zero voltage is found for implementations with one (mode I_1) and two (mode I_2) controllable, current-bidirectional switches.

In mode I_1, for which the unified DC analysis is carried out in Section 9.3, only variable-frequency control is applicable. Provided that no lower limit is imposed on the switching frequency, the operating region in mode I_1 is open in the load direction. The operating region also includes the zero load axis. However, equivalent duty ratios $0 < m < 0.5$ are not accessible.

In mode I_2, for which DC analysis is completed in Section 9.4, constant-frequency control can be utilized to regulate the DC conversion ratio. Equivalent duty ratios above and below $m = 0.5$ are equally accessible. The operating region is now bounded in the load direction, but the zero-load axis is included. It is interesting to note that distinctions between mode I_2 and the continuous conduction mode of the PWM parent gradually disappear as the normalized switching frequency tends to zero.

In Section 9.5, experimental verification of existence of operating modes and results of DC analyses completes the study of ZV-QSW converters.

9.1 Operating States

By definition of ZV-QSW converters, none of the loops in the the parent PWM topology is disturbed. In particular, for the loop of Proposition 3.7, which contains two switches and elements that contribute to V_{off}, we have

$$v_t + v_d = 1\,. \tag{9.1}$$

By the argument identical to the one of Section 8.1 for ZV converters, the cut-set of Proposition 3.7 now must include C_r. Since by definition $v_d = v_{C_r} + V$, where V is some DC voltage, it follows that

$$i_t + i_d = i_{on} + \frac{dv_d}{d\theta} . \tag{9.2}$$

Finally, L_r is in parallel with an inductor in $\mathcal{L}_{on}$ so that $i_{on} = I_{on} + i_{L_r}$ and, therefore,

$$\frac{di_{on}}{d\theta} + m = v_d . \tag{9.3}$$

The ON-ON state is not feasible in a ZV-QSW converter because the condition $v_t = v_d = 0$ contradicts Eq. (9.1).

In terms of the state variables v_d and i_{on}, equations and solutions for three possible states are summarized as follows:

ON-OFF state: $v_t = 0$, $i_d = 0$.

Equations:

$$\frac{di_{on}}{d\theta} = v_d - m \, , \; i_{on}(0) = I_{nf} . \tag{9.4}$$

Solution:

$$v_d = 1 , \tag{9.5}$$

$$i_{on} = I_{nf} + (1 - m)\theta . \tag{9.6}$$

OFF-ON state: $i_t = 0$, $v_d = 0$.

Equations:

$$\frac{di_{on}}{d\theta} = -m \, , \; i_{on}(0) = I_{fn} . \tag{9.7}$$

Solution:

$$v_d = 0 , \tag{9.8}$$

$$i_{on} = I_{fn} - m\theta . \tag{9.9}$$

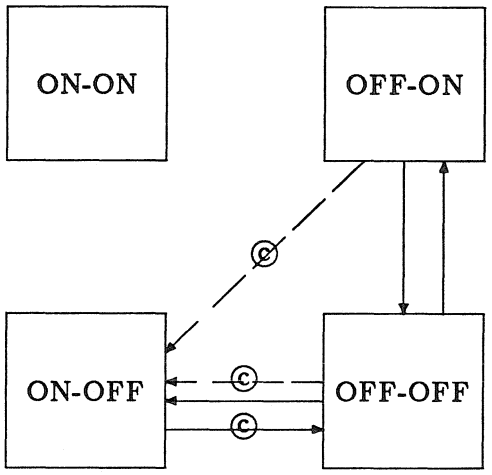


Figure 9.1: State transition diagram for the ZV-QSW converters with a single, controllable, current-bidirectional switch.

OFF-OFF state: $i_t = i_d = 0$.

Equations:

$$\frac{dv_d}{d\theta} = -i_{on}\,,\; v_d(0) = V_{ff}\,, \tag{9.10}$$

$$\frac{di_{on}}{d\theta} = v_d - m\,,\; i_{on}(0) = I_{ff}\,. \tag{9.11}$$

Solution:

$$v_d = m + (V_{ff} - m)\cos\theta - I_{ff}\sin\theta\,, \tag{9.12}$$

$$i_{on} = I_{ff}\cos\theta + (V_{ff} - m)\sin\theta\,. \tag{9.13}$$

9.2 Operating Modes

9.2.1 Implementation with a Single Controllable Switch

If S is a controllable, current-bidirectional switch and $\hat{S}$ is a diode, the state transition diagram for a ZV-QSW converter is shown in Fig. 9.1. Since S and $\hat{S}$ form a loop with V_{off}, a lossy transition OFF-ON $\rightarrow$ ON-OFF is possible as in a PWM converter. The periodic sequence

$$\text{mode } I_1\text{: } \cdots \rightarrow \boxed{\text{OFF-OFF}} \rightarrow \boxed{\text{ON-OFF}} \rightarrow \boxed{\text{OFF-OFF}} \rightarrow \boxed{\text{OFF-ON}} \rightarrow \cdots \tag{9.14}$$

defines the only operating mode for which switching losses are minimized, since all switching transitions can be realized at zero voltage. Only one transition (the $\hat{S}$-switch turn-OFF) in the sequence is controllable, so that only variable-frequency control is applicable.

Assume that the converter is initially in the OFF-ON state. Current i_{on} decreases linearly until the $\hat{S}$-switch turns OFF. In the succeeding OFF-OFF (resonant) state, the S-switch voltage decreases in a sinusoidal manner until it crosses zero, and the antiparallel diode starts to conduct at $\theta = \theta_1$. The succeeding ON-OFF state lasts until the S-switch is turned OFF at $\theta = \theta_2$, initiating the second OFF-OFF state. Now, diode voltage descends in a sinusoidal manner until it drops to zero and the diode starts to conduct at $\theta = \theta_3$. The converter is in the OFF-ON state until the diode current reaches zero at $\theta = \theta_4$, and the switching cycle is completed.

Typical waveforms in a ZV-QSW converter operating in mode I_1 are shown in Fig. 9.2. The hatched area in the control signal p_t for the S-switch transistor corresponds to the interval when $i_t < 0$. In this interval, the S-switch antiparallel diode is conducting and the state of the transistor is irrelevant.

9.2.2 Implementation with Two Controllable Switches

If both switches are controllable current-bidirectional, the modified state transition diagram is shown in Fig. 9.3. The $\hat{S}$-switch turn-OFF is now controllable so that control at constant switching frequency is possible. Operation in mode I_2 is quite similar to the operation in mode I_1. The only difference is that i_{on} at the end of the OFF-ON state can be less than zero in mode I_2.

Waveforms illustrating operation of a ZV-QSW converter in mode I_2 are shown in Fig. 9.4. Control signals p_t and p_d for transistors in switches S and $\hat{S}$ can assume any value during the hatched intervals without affecting other converter waveforms. Control duty ratio D_c is defined as the interval between the $\hat{S}$-switch turn-OFF and the S-switch turn-OFF relative to the switching period,

$$D_c \equiv \frac{\theta_1 + \theta_2}{\theta_p}. \tag{9.15}$$

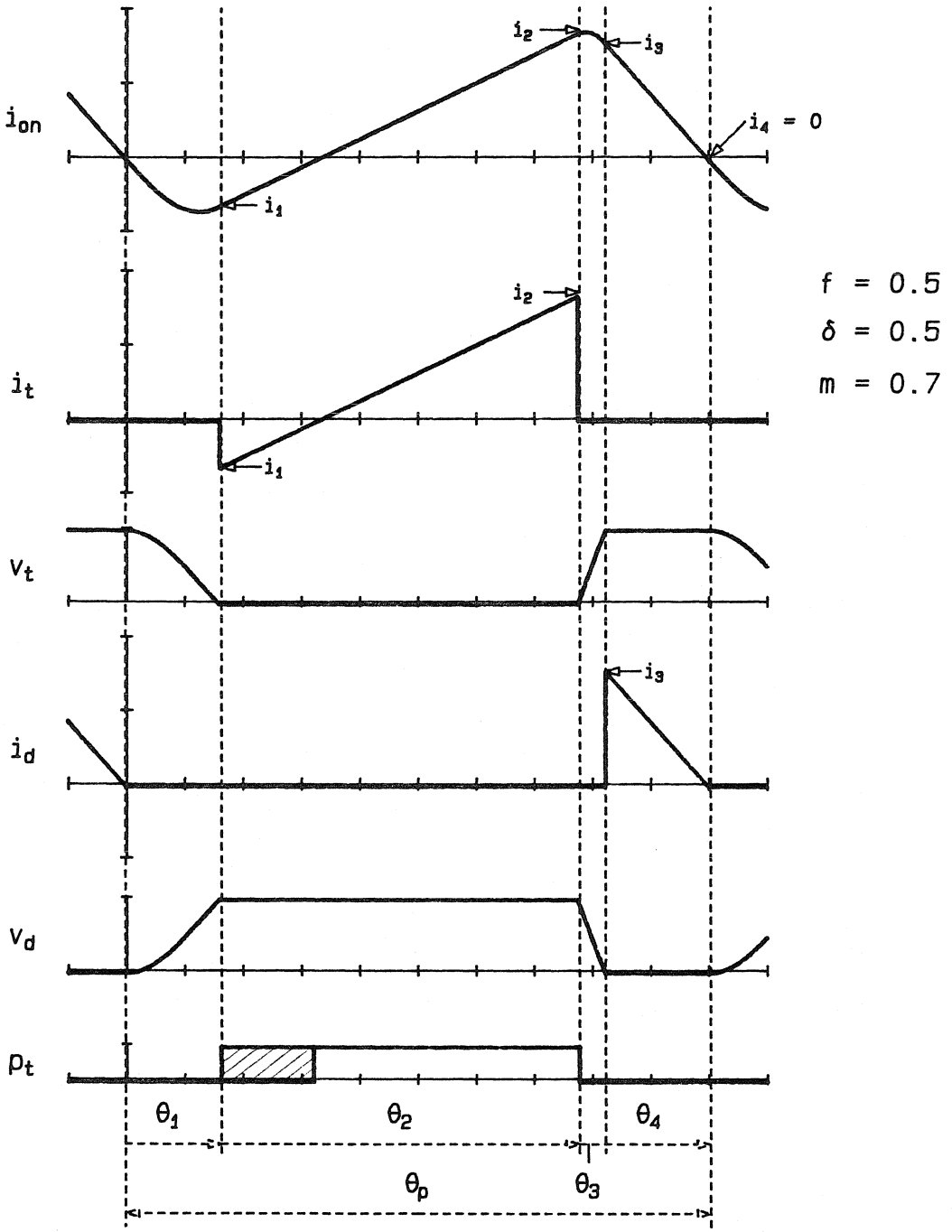


Figure 9.2: Typical waveforms in a ZV-QSW converter operating in mode I_1.

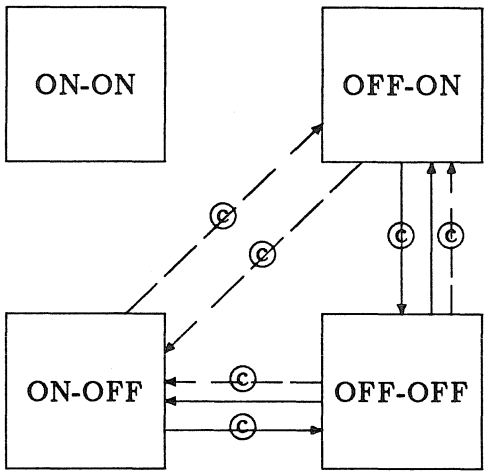


Figure 9.8: State transition diagram for a ZV-QSW converter with two controllable, current-bidirectional switches.

9.3 Variable-Frequency Control: DC Analysis

A set of steady-state equations can be derived from the general solutions of state equations for each operating state. Assume that transition from the OFF-ON to the OFF-OFF state is at the beginning of a switching cycle. Initial conditions for the OFF-OFF state are known: $I_{ff} = 0$ and $V_{ff} = 0$. At $\theta = \theta_1$, diode voltage reaches $v_d = 1$, so that the current-bidirectional switch S is forced to conduct current $I_{nf} = i_1 < 0$. Assuming that equation $v_d(\theta_1) = 1$ can be solved, the solution for θ_1 and i_1 is given by

$$\theta_1 = \pi - \arctan \frac{\sqrt{2m-1}}{1-m}, \tag{9.16}$$

$$i_1 = -\sqrt{2m-1}\,. \tag{9.17}$$

In the ON-OFF state, current i_{on} ramps up linearly. The transistor in the S-switch has to be turned ON before i_{on} crosses zero. A connection between the initial current i_1 and the final current i_2 at the end of the ON-OFF state is given by

$$i_2 = i_1 + (1-m)\theta_2\,. \tag{9.18}$$

Since transition from the ON-OFF state is initiated by an external control signal and not by the internal circuit waveforms (provided that $i_2 \geq 0$), duration of the ON-OFF state, θ_2, can be regarded as a free parameter.

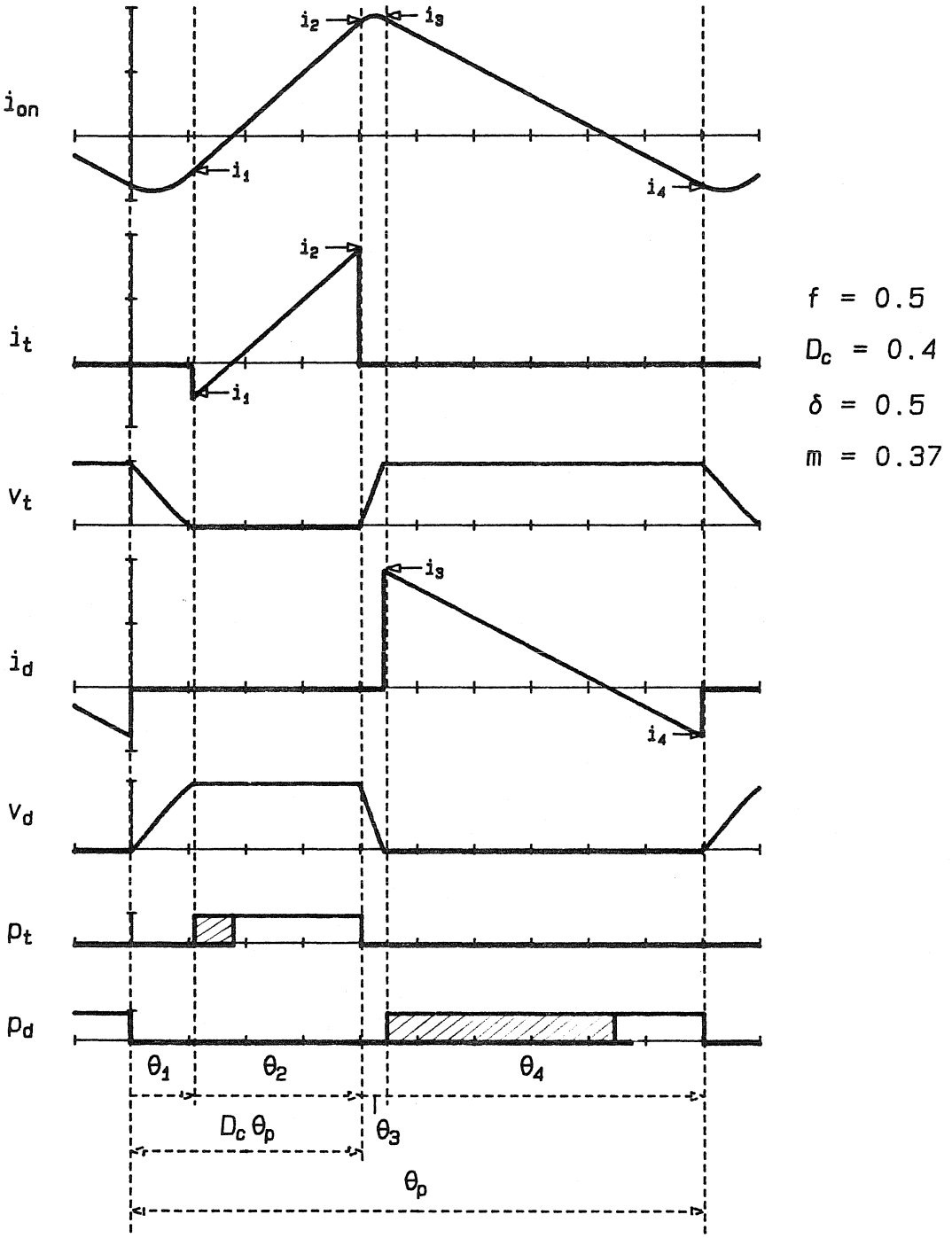


Figure 9.4: Typical waveforms in a ZV-QSW converter operating in mode I_2.

From the ON-OFF state the converter enters the OFF-OFF state again. With initial conditions $I_{ff} = i_2$ and $V_{ff} = 1$, the solution to $v_d(\theta_3) = 0$, if it exists, is given by:

$$\theta_3 = \frac{\pi}{2} + \arctan\frac{1-m}{i_2} - \arctan\frac{\sqrt{1-2m+i_2^2}}{m}, \tag{9.19}$$

$$i_3 = \sqrt{1-2m+i_2^2}. \tag{9.20}$$

In the OFF-ON state, current i_{on} decreases linearly. This state and the switching cycle are completed at $\theta = \theta_4$ when $i_{on}(\theta_4) = i_4 = 0$ and the diode turns OFF. Duration of the last state is given by

$$\theta_4 = i_3/m. \tag{9.21}$$

Expressions for the average S-switch and $\hat{S}$-switch currents,

$$\bar{i}_t = m\delta = \frac{i_1+i_2}{2}\frac{\theta_2}{\theta_p}, \tag{9.22}$$

$$\bar{i}_d = (1-m)\delta = \frac{i_3}{2}\frac{\theta_4}{\theta_p}, \tag{9.23}$$

provide the necessary link between the equivalent duty ratio m and normalized load δ. Although it is not possible to solve the system of steady-state equations in a closed form of the type $F(m, \delta, f) = 0$, switching frequency $f(m, \theta_2)$ and load $\delta(m, \theta_2)$ can be found easily from Eqs. (9.16) through (9.23) for any given equivalent duty ratio m and parameter θ_2. For $m = const.$, $f(m, \theta_2)$ is monotonously decreasing and $\delta(m, \theta_2)$ is monotonously increasing with θ_2. All operating points in mode I_1 can be traversed by sweeping m and θ_2.

Operation at Zero Load

If a ZV-QSW converter is unloaded, it follows that $i_2 = -i_1$ and that both i_3 and θ_4 are equal to zero. The closed form solution for zero load can be found for the control variable f as a function of the equivalent duty ratio m,

$$f(\delta = 0) = \frac{\pi}{\pi - \arctan\frac{\sqrt{2m-1}}{1-m} + \frac{\sqrt{2m-1}}{1-m}}. \tag{9.24}$$

9.3.1 Conditions for Operation in Mode I_1

DC analysis of the preceding section is valid if the converter operates in mode I_1. The solution for θ_1 in Eq. (9.16) exists iff

$$1 > m \geq 0.5\,. \tag{9.25}$$

If this condition is satisfied, the solution for θ_3 exists provided that

$$i_2 \geq \sqrt{2m-1}\,. \tag{9.26}$$

It should be noted that the last condition implies that $i_2 \geq 0$, so that controllable transition from ON-OFF to OFF-OFF state is guaranteed. Assume that $m \geq 0.5$ and that $i_2 = \sqrt{2m-1}$. Then, from Eqs. (9.17) and (9.22), load current δ is necessarily equal to zero. On the other hand, since $\delta(m, \theta_2)$ is an unbounded, monotonously increasing function of θ_2 for any fixed $m \geq 0.5$, and since no condition imposes an upper bound on θ_2, operation in mode I_1 is possible for any $m \geq 0.5$ and any $\delta \geq 0$. Note, however, that since

$$\delta \to \infty \quad \Rightarrow \quad f \to 0\,, \tag{9.27}$$

the operating region is effectively bounded in the load direction by a lower bound on the switching frequency. Such a bound is imposed in all practical designs.

The lower bound on θ_2, which corresponds to operation at zero load, is given by

$$\theta_{2min} = 2\frac{\sqrt{2m-1}}{1-m}\,. \tag{9.28}$$

9.3.2 DC conversion characteristics

Load-to-output and control-to-output DC characteristics are shown in Figs. 9.5 and 9.6, respectively. Computation of curves is described in Appendix B.2.

9.4 Constant-Frequency Control: DC Analysis

In ZV-QSW converters with two controllable switches, turn-OFF transitions of both switches are controllable. This means that current i_{on} at the end of the OFF-ON state can be less than or equal to zero. Therefore, the initial condition for the first OFF-OFF state

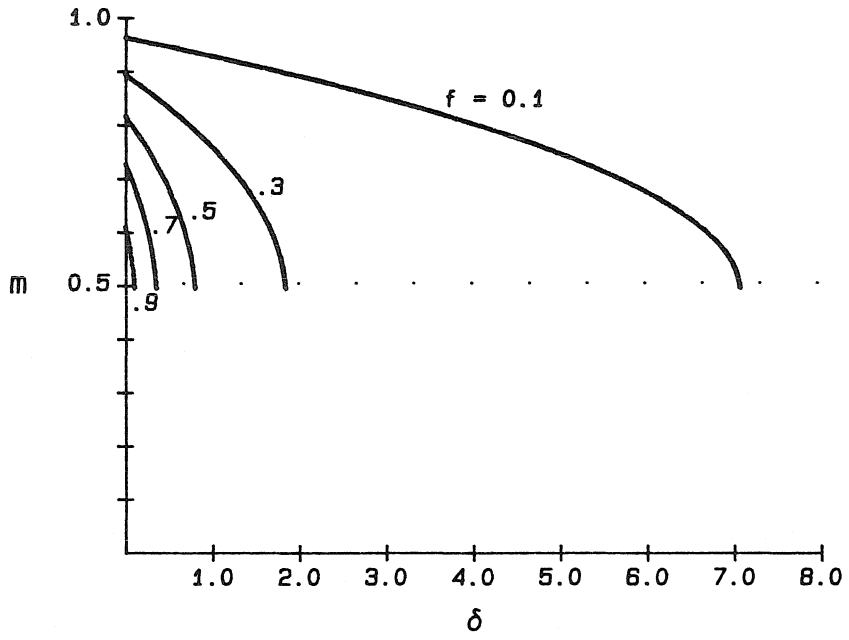


Figure 9.5: Load-to-output characteristics of a ZV-QSW converter operating in mode I_1

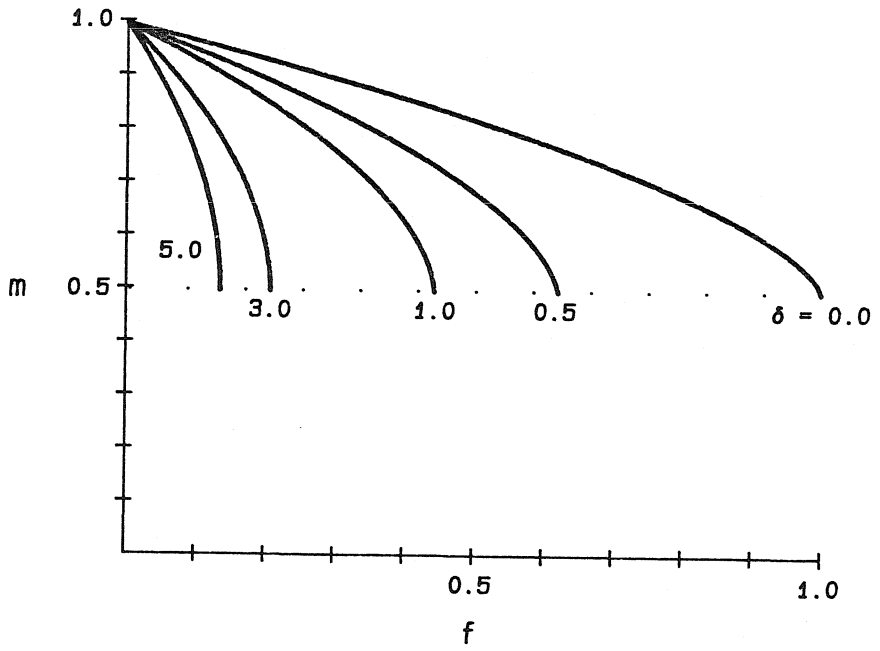


Figure 9.6: Control-to-output characteristics of a ZV-QSW converter operating in mode I_1

is $I_{ff} = i_4 \leq 0$, and the steady-state equations and solutions are changed accordingly. Instead of Eqs. (9.16) and (9.17), we have

$$\theta_1 = \frac{\pi}{2} + \arctan\frac{m}{|i_4|} - \arctan\frac{\sqrt{2m-1+i_4^2}}{1-m}, \tag{9.29}$$

$$i_1 = -\sqrt{2m-1+i_4^2}. \tag{9.30}$$

Equations (9.18) through (9.20) for the ON-OFF state and the second OFF-OFF state are still valid. However, θ_2 is now determined by the control duty ratio,

$$\theta_2 = D_c\theta_p - \theta_1. \tag{9.31}$$

For the final OFF-ON state, one can write

$$\theta_4 = \theta_p - \theta_1 - \theta_2 - \theta_3, \tag{9.32}$$

$$i_4 = i_3 - m\theta_4. \tag{9.33}$$

The average S-switch current is the same as before, and only the expression for the average $\hat{S}$-switch current needs to be changed to allow possibly non-zero current i_4,

$$\bar{i}_d = (1-m)\delta = \frac{i_3 + i_4}{2}\frac{\theta_4}{\theta_p}. \tag{9.34}$$

9.4.1 Conditions for Operation in Mode I_2

In this section, conditions for operation in mode I_2 are established. Solutions (9.29) and (9.30) for i_1 and θ_1 in terms of m and i_4 can be found if

$$i_4 \leq \begin{cases} -\sqrt{1-2m}, & 0 < m < 0.5, \\ 0, & 0.5 \leq m < 1.0. \end{cases} \tag{9.35}$$

The fact that i_4 must be less than zero is taken into account. The same argument for solutions (9.20) and (9.21) translates into

$$i_2 \geq \begin{cases} 0, & 0 < m < 0.5, \\ \sqrt{2m-1}, & 0.5 \leq m < 1.0. \end{cases} \tag{9.36}$$

Finally, duration of all states must be non-negative,

$$\theta_2, \theta_4 \geq 0. \tag{9.37}$$

The above conditions are difficult to apply because they involve unknown quantities such as instantaneous values of current i_{on}. It is of practical interest to translate the conditions for operation in mode I_2 into the load-to-output plane.

Assume first that $1 > m \geq 0.5$. Boundary conditions, $\theta_4 = 0$ and $i_2 = \sqrt{2m-1}$, imply that $\delta = 0$. Thus, operation at zero load is possible. Boundary condition $i_4 = 0$ gives the maximum possible load δ for a given equivalent duty ratio m. But, for $i_4 = 0$, the converter operates in mode I_1. This implies that the boundary of the operating region in mode I_2 coincides with the load-to-output DC characteristic in mode I_1 for the same normalized frequency f.

Assume now that $0 < m < 0.5$. Boundary conditions $\theta_2 = 0$, $i_2 = 0$ again imply that $\delta = 0$. The maximum possible load is determined by the boundary condition for i_4. Pick a point (m', δ') at the boundary curve found for $m > 0.5$ earlier and denote all quantities at that point with prime ($'$). One can verify that for $m = 1 - m'$, boundary condition $i_4 = -\sqrt{1-2m}$ corresponds to the solution $\theta_1 = \theta_1'$, $\theta_2 = \theta_4'$, $\theta_3 = \theta_3'$, $\theta_4 = \theta_2'$ and $\delta = \delta'$. Thus, for each point on the boundary curve for $m > 0.5$, there is a point for $m < 0.5$ symmetrical around $m = 0.5$.

Boundaries of the operating region for mode I_2 are shown in Fig. 9.7 for switching frequency f as a varying parameter. As discussed above, boundary curves are symmetrical around $m = 0.5$. It should be noted that the ZV-QSW converter with two controllable, current-bidirectional switches is current-bidirectional by itself. Thus, the operating region in mode I_2 extends symmetrically for $\delta < 0$.

In contrast to mode I_1, equivalent duty ratios above and below 0.5 are equally attainable. Operating mode I_2 is limited to a bounded portion of the load-to-output plane, but since $\delta = 0$ is inside the operating region, the available load range is infinitely large. The operating region in mode I_2 expands with decreasing normalized frequency f. This can be justified by a qualitative argument that for a lower switching frequency, relative lengths of the resonant OFF-OFF states diminish, and the distinction between mode I_2 and the continuous conduction mode described by the sequence ON-OFF $\leftrightarrow$ OFF-ON disappears.

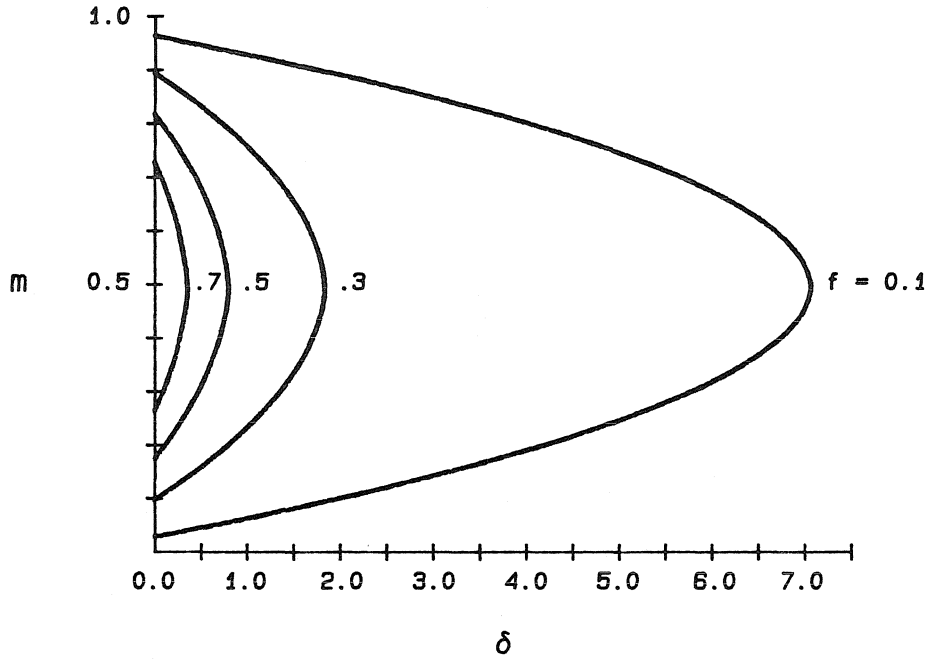


Figure 9.7: Operating regions for a ZV-QSW converter in mode I_2 for normalized frequency f as a varying parameter.

9.4.2 DC conversion characteristics

For a particular switching frequency, DC conversion characteristics can be computed numerically, as detailed in Appendix B.2. Results are presented in two planes – load-to-output (Fig. 9.8) and control-to-output (Fig. 9.9).

Within boundaries of the operating region in mode I_2, characteristics are similar to ideal PWM characteristics – the equivalent duty ratio and, therefore, DC conversion ratio are weakly dependent on the load current while control-to-output characteristics are almost straight lines. As the switching frequency is lowered, DC characteristics of a ZV-QSW converter further approach the characteristics of PWM converters. Indeed, if $f << 1$, $\theta_2 \approx D_c\theta_p$ and $(i_1 + i_2)/2 \approx \delta$. From Eq. (9.22) it follows that $m \approx D_c$ for any load δ. Particular examples of ZV-QSW converters with two controllable switches appeared in [19] with an analysis based on the low-frequency approximation.

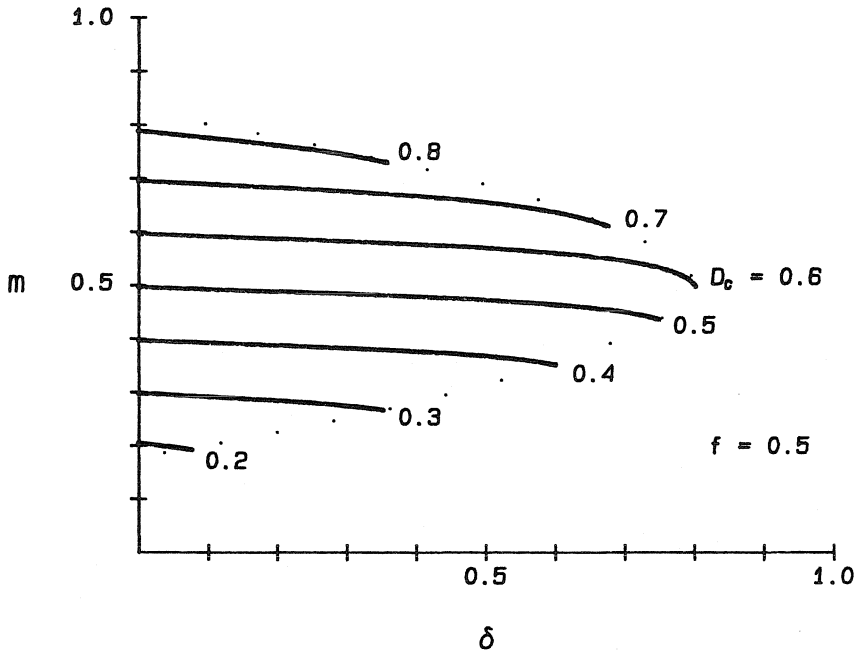


Figure 9.8: Load-to-output characteristics for a ZV-QSW converter operating in mode I_2.

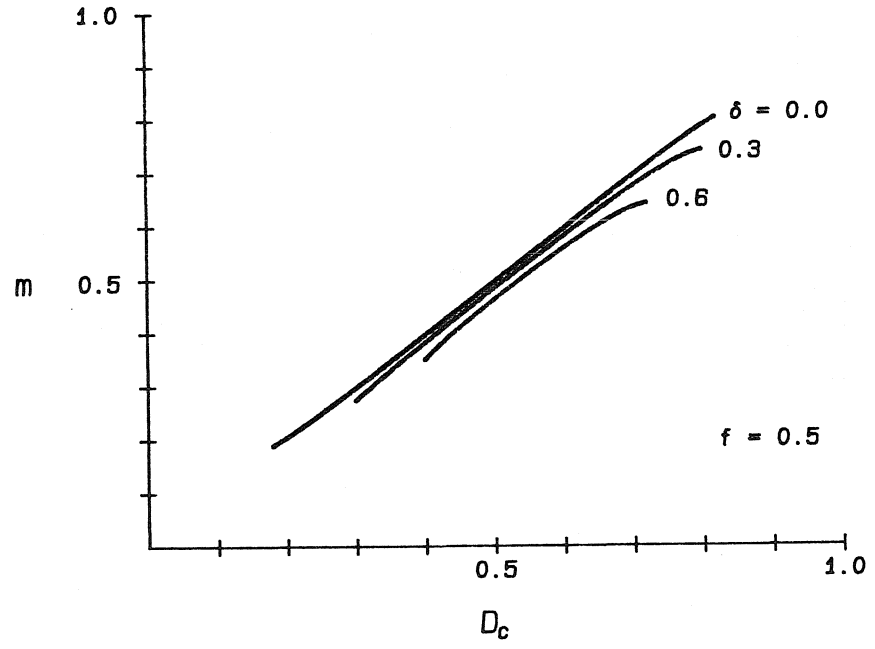


Figure 9.9: Control-to-output characteristics for a ZV-QSW converter operating in mode I_2.

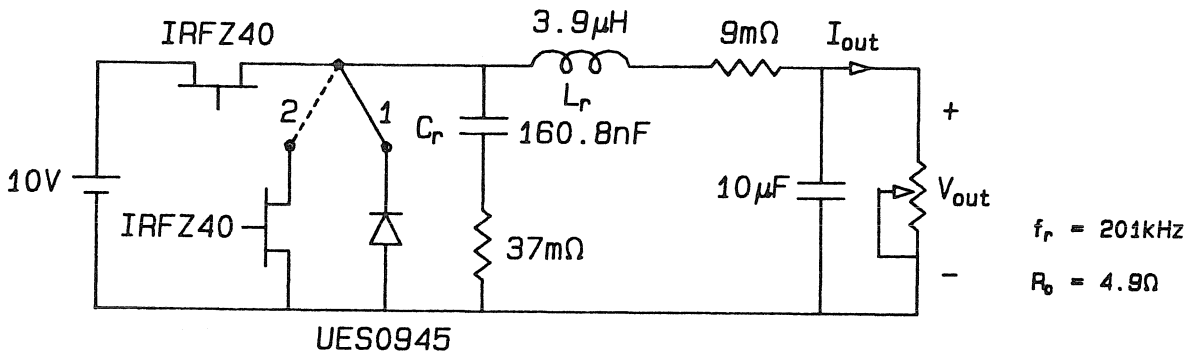


Figure 9.10: An experimental ZV-QSW buck converter.

9.5 Experimental Verification

In this section, existence of operating modes I_1 and I_2 and predicted DC characteristics are verified using an experimental ZV-QSW converter of Fig. 9.10. Parent PWM topology is the second order buck converter with $M(D) = D$. The $\hat{S}$-switch is implemented as a diode (1) or as a MOS transistor (2). Resonant capacitor C_r is placed in parallel with the $\hat{S}$-switch. Resonant inductor L_r forms a loop with $\hat{S}$ and the output capacitor. In fact, according to defining position $Ll\hat{S}$, the resonant inductor is placed in parallel with the output inductor L of the buck converter. Then, L is absorbed in L_r. Position of the resonant inductor is unique, while the resonant capacitor can also be placed in parallel with the S-switch or in parallel with L_r without affecting DC conversion properties of the converter.

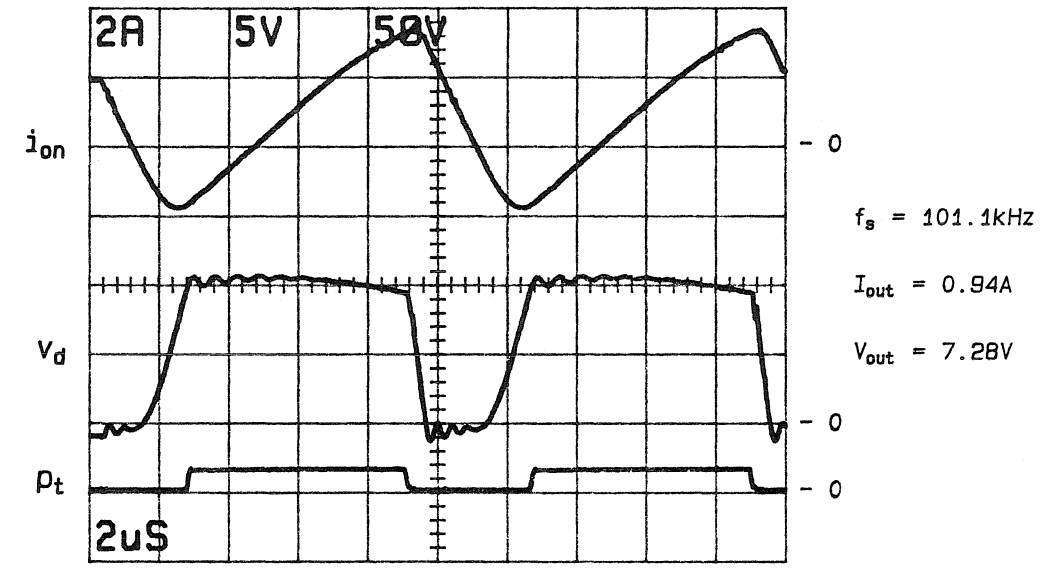
With $\hat{S}$ implemented as a diode, waveforms in Fig. 9.11 (a) compare favorably with ideal waveforms of Fig. 9.2, confirming operation in mode I_1. Spurious oscillations observable in the diode voltage waveform are due to resonance between C_r and parasitic inductance in the loop with the switches.

Control circuitry drives the S-switch with variable-frequency, constant-pause pulses p_t.

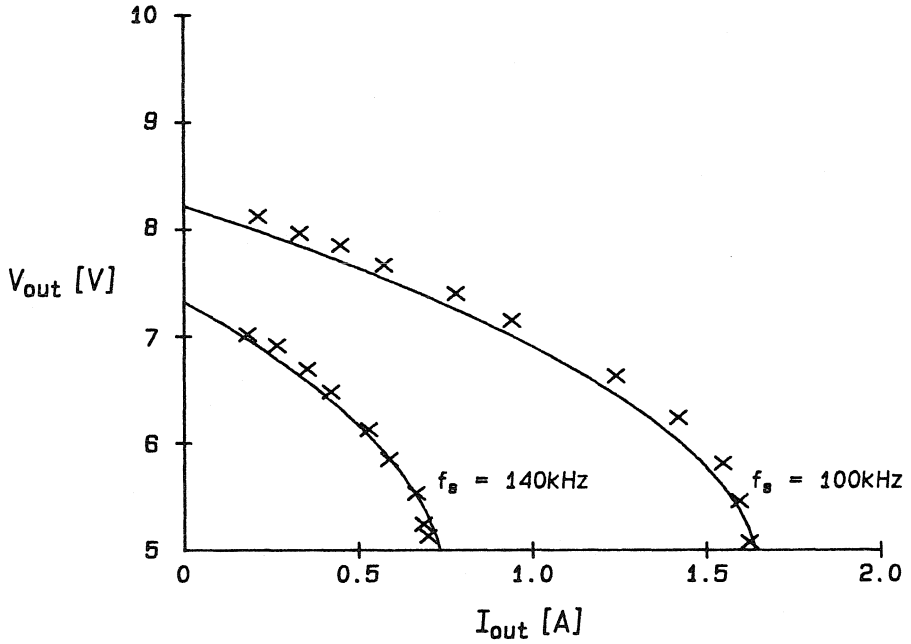
Measured DC characteristics (Fig. 9.11 (b)) are in excellent agreement with prediction. Compared to Q_n-PWM and ZV experimental circuits, the circuit in Fig. 9.10 has a lower number of elements, and their parasitic series resistances are lower. In particular, since voltage stresses in ZV-QSW converters are low (just as in PWM converters), a $50V$ device (IRFZ40 MOS transistor with a rated ON-resistance of $28m\Omega$) is used instead of a $100V$ device (IRF540 with an ON-resistance of $85m\Omega$). Thus, a closer match between measurement and prediction is obtained compared to experimental results for Q_n-PWM and ZV converters.

With the $\hat{S}$-switch implemented as a MOS transistor, mode I_2 can be verified by comparison of recorded waveforms in Fig. 9.12 (a) and ideal waveforms of Fig. 9.4 (b).

Control circuitry provides constant-frequency signals (p_t and p_d) to drive the S-switch and $\hat{S}$-switch transistors. Control over the conversion ratio is accomplished by varying the duty ratio of the signals p_t and p_d. An excellent agreement between measured and predicted DC characteristics is demonstrated in Fig. 9.12 (b).

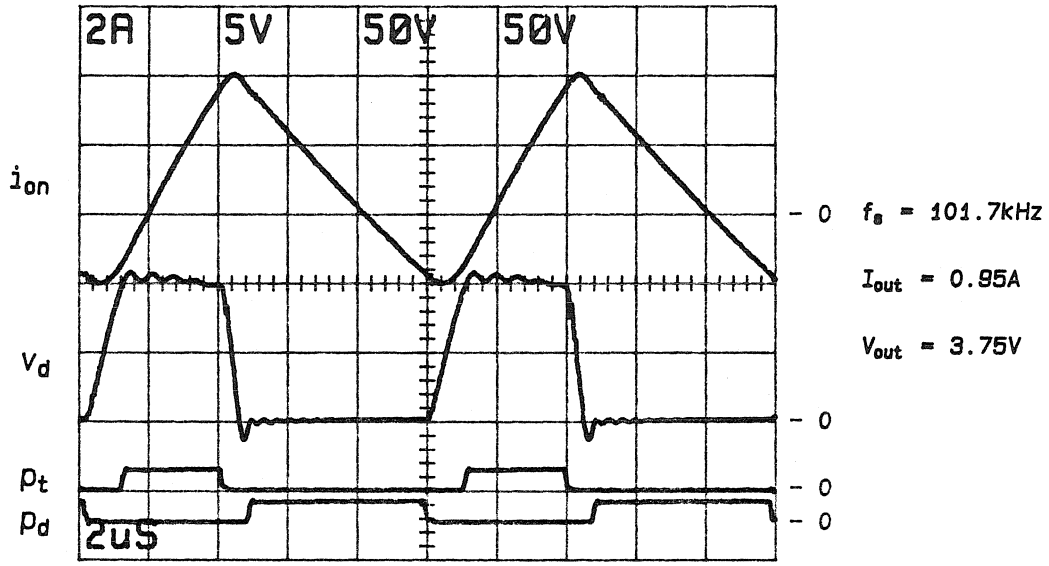


a)

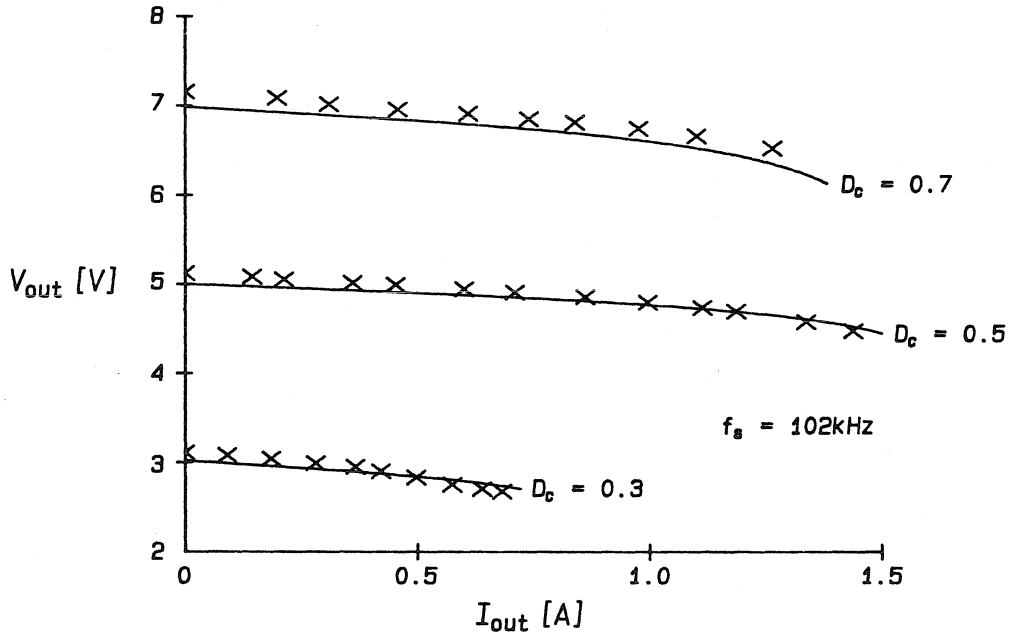


b)

Figure 9.11: Recorded waveforms (a) and measured and predicted DC characteristics (b) for the experimental ZV-QSW buck converter operating in mode I_1.



a)



b)

Figure 9.12: Recorded waveforms (a) and measured and predicted DC characteristics (b) for the experimental ZV-QSW buck converter operating in mode I_2.

Chapter 10

Zero-Voltage, Multi-Resonant Converters

In this chapter, a study of Zero-Voltage, Multi-Resonant (ZV-MR) converters is presented.

In Section 10.2 it is shown that an operating mode with all zero-voltage transitions is not unique. Three such modes, $(I, II, III)_1$, are found for the implementation with one controllable, current-bidirectional switch. In addition, there are four operating modes with all zero-voltage transitions, $(I, II, III, IV)_2$, if both switches are controllable.

Variable-frequency control is applicable in modes $(I, II, III)_1$. DC analysis of Section 10.3 reveals that a closed form solution for the equivalent duty ratio does not exist. Thus, DC characteristics and boundaries of the operating regions are computed numerically. The combined operating region for modes $(I, II, III)_1$ is bounded, but it includes the zero-load axis. Analitical results are found for the DC characteristic at zero load, minimum equivalent duty ratio attainable at zero load and maximum normalized frequency f.

If both switches are implemented as controllable current-bidirectional, control at a constant switching frequency is possible. DC analysis for all four operating modes is carried out in Section 10.4. The combined operating region for modes $(I, II, III)_2$ includes the zero-load axis, and up to some maximum normalized load, all equivalent duty ratios $0 \leq m \leq 1$ are accessible. In mode IV_2, the range of attainable equivalent duty ratios is more restricted.

Existence of operating modes with all zero-voltage transitions and corresponding DC characteristics are verified experimentally in Section 10.5.

10.1 Operating States

In a ZV-MR converter, there are three resonant elements: a resonant inductor L_r, a resonant capacitor C_r (in the $C\!lS$ position – in a loop with the S-switch and possibly elements of $\mathcal{C} \cup \{V_g\}$) and a resonant capacitor C_{r1} (in the $C\!l\hat{S}$ position – in a loop with the $\hat{S}$-switch and possibly elements of $\mathcal{C} \cup \{V_g\}$). Define the parameter x as a ratio of the two resonant capacitance values,

$$x \equiv \frac{C_{r1}}{C_r} . \tag{10.1}$$

By the same argument as for ZV converters, L_r is in a loop with both switches and DC voltage V_{off}, so that

$$v_t + v_d + \frac{di_{L_r}}{d\theta} = 1 . \tag{10.2}$$

The cut-set of Proposition 3.7 must now include both C_r and C_{r1}. Kirchhoff's voltage law for the loops that include a resonant capacitor and a switch yields

$$v_t = v_{C_r} + V_0 \quad \text{and} \quad v_d = v_{C_{r1}} + V_1 . \tag{10.3}$$

Here, V_0 and V_1 are some DC voltages. Therefore,

$$i_t + \frac{dv_t}{d\theta} + i_d - x\frac{dv_d}{d\theta} = \delta . \tag{10.4}$$

Finally, since L_r in a ZV converter forms a cut-set with the $\hat{S}$-switch and possibly elements of $\mathcal{L}$, this cut-set must also include C_{r1} in a ZV-MR converter. But then, there must be a cut-set that includes the resonant inductor L_r, the S-switch, the resonant capacitor C_r and possibly elements of $\mathcal{L}$. For this cut-set, we have

$$i_t + dv_t/d\theta = i_{L_r} + I , \tag{10.5}$$

where I is some DC current. State variables selected for description of operating states of a ZV-MR converter are the S-switch voltage v_t, the $\hat{S}$-switch voltage v_d and current i_r, defined by

$$i_r \equiv i_t + \frac{dv_t}{d\theta} . \tag{10.6}$$

In terms of the state variables, Eqs. (10.2) and (10.4) become

$$v_t + v_d + \frac{di_r}{d\theta} = 1\,, \tag{10.7}$$

$$i_r + i_d - x\frac{dv_d}{d\theta} = \delta\,. \tag{10.8}$$

Now, description of the operating states follows in a straightforward manner:

ON-ON state: $v_t = 0$, $v_d = 0$.

Equations:

$$\frac{di_r}{d\theta} = 1\,,\ i_r(0) = I_{nn}\,. \tag{10.9}$$

Solution:

$$i_r = I_{nn} + \theta\,. \tag{10.10}$$

ON-OFF state: $v_t = 0$, $i_d = 0$.

Equations:

$$\frac{di_r}{d\theta} = 1 - v_d\,,\ i_r(0) = I_{nf}\,, \tag{10.11}$$

$$\frac{dv_d}{d\theta} = -\frac{\delta}{x} + \frac{i_r}{x}\,,\ v_d(0) = V'_{nf}\,. \tag{10.12}$$

Solution:

$$i_r = \delta + (I_{nf} - \delta)\cos\frac{\theta}{\sqrt{x}} + \sqrt{x}(1 - V'_{nf})\sin\frac{\theta}{\sqrt{x}}\,, \tag{10.13}$$

$$v_d = 1 + (V'_{nf} - 1)\cos\frac{\theta}{\sqrt{x}} + \frac{1}{\sqrt{x}}(I_{nf} - \delta)\sin\frac{\theta}{\sqrt{x}}\,. \tag{10.14}$$

OFF-ON state: $i_t = 0$, $v_d = 0$.

Equations:

$$\frac{di_r}{d\theta} = 1 - v_t\,,\ i_r(0) = I_{fn}\,, \tag{10.15}$$

$$\frac{dv_t}{d\theta} = i_r\,,\ v_t(0) = V_{fn}\,. \tag{10.16}$$

Solution:

$$i_r = I_{fn}\cos\theta + (1 - V_{fn})\sin\theta\,, \tag{10.17}$$

$$v_t = 1 + (V_{fn} - 1)\cos\theta + I_{fn}\sin\theta\,. \tag{10.18}$$

OFF-OFF state: $i_t = 0, i_d = 0$.

Equations:

$$\frac{di_r}{d\theta} = 1 - v_t - v_d \,,\; i_r(0) = I_{ff} \,, \tag{10.19}$$

$$\frac{dv_t}{d\theta} = i_r \,,\; v_t(0) = V_{ff} \,, \tag{10.20}$$

$$\frac{dv_d}{d\theta} = -\frac{\delta}{x} + \frac{i_r}{x} \,,\; v_d(0) = V'_{ff} \,. \tag{10.21}$$

Solution:

$$\begin{aligned} v_t &= \frac{x}{1+x}(1 + \frac{1}{x}V_{ff} - V'_{ff}) + \frac{\delta}{1+x}\theta + \\ &+ \frac{x}{1+x}(V_{ff} + V'_{ff} - 1)\cos\sqrt{\frac{1+x}{x}}\theta + \\ &+ \sqrt{\frac{x}{1+x}}(I_{ff} - \frac{\delta}{1+x})\sin\sqrt{\frac{1+x}{x}}\theta \,, \end{aligned} \tag{10.22}$$

$$\begin{aligned} v_d &= \frac{1}{1+x}(1 - V_{ff} + xV'_{ff}) - \frac{\delta}{1+x}\theta + \\ &+ \frac{1}{1+x}(V_{ff} + V'_{ff} - 1)\cos\sqrt{\frac{1+x}{x}}\theta + \\ &+ \frac{1}{\sqrt{x(1+x)}}(I_{ff} - \frac{\delta}{1+x})\sin\sqrt{\frac{1+x}{x}}\theta \,, \end{aligned} \tag{10.23}$$

$$\begin{aligned} i_r &= \frac{\delta}{1+x} + (I_{ff} - \frac{\delta}{1+x})\cos\sqrt{\frac{1+x}{x}}\theta + \\ &+ \sqrt{\frac{x}{1+x}}(1 - V_{ff} - V'_{ff})\sin\sqrt{\frac{1+x}{x}}\theta \,. \end{aligned} \tag{10.24}$$

10.2 Operating Modes

As for other QR converters, operating modes with lossless transitions are studied for two distinct implementations of the switches S and $\hat{S}$.

10.2.1 Implementation with a Single Controllable Switch

Assume that S is a controllable, current-bidirectional switch and that the $\hat{S}$-switch is a diode. Since both switches are in loops with resonant capacitors, every turn-OFF transition is at zero voltage. By assumption, the S-switch turn-OFF transitions are controllable as long as $i_t \geq 0$, while the diode turn-OFF transitions occur when current i_d drops to zero. Every controllable turn-ON transition is necessarily at non-zero voltage.

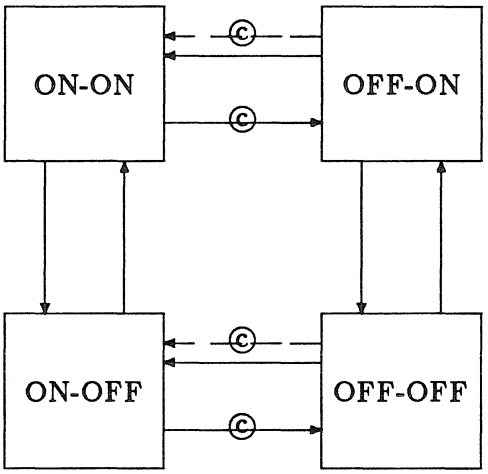


Figure 10.1: State transition diagram for ZV-MR converters with a single, controllable, current-bidirectional switch.

From the state transition diagram shown in Fig. 10.1, it appears that a large number of operating modes with all lossless transitions are possible. However, it can be shown that a viable operating mode cannot include the following two sequences of states:

$$\rightarrow \boxed{\text{OFF-ON}} \rightarrow \boxed{\text{OFF-OFF}} \rightarrow \boxed{\text{ON-OFF}} \rightarrow \tag{10.25}$$

and

$$\rightarrow \boxed{\text{ON-ON}} \rightarrow \boxed{\text{ON-OFF}} \rightarrow \boxed{\text{ON-ON}} \rightarrow . \tag{10.26}$$

If the OFF-OFF state is entered from the OFF-ON state, the initial conditions are: $I_{ff} = \delta$, $V_{ff} > 0$ and $V'_{ff} = 0$. In the OFF-OFF state with these initial conditions, the relation

$$v_t = \delta\theta + xv_d + V_{ff} \tag{10.27}$$

can be obtained from Eqs. (10.22) and (10.23). If sequence (10.25) is possible, then for some $\theta > 0$, the S-switch and diode voltages are $v_t = 0$ and $v_d > 0$, respectively. This is in contradiction to Eq. (10.27), so that the first part of the assertion is proved.

If the ON-OFF state is entered from the ON-ON state, the initial conditions are $I_{nf} = \delta$ and $V'_{nf} = 0$. By eliminating the time variable from Eqs. (10.13) and (10.14), it follows that

$$x(v_d - 1)^2 + (i_r - \delta)^2 = x\,. \tag{10.28}$$

The only point where v_d is zero is for $i_r = \delta$ or, equivalently, for $i_d = 0$. Thus, once the ON-OFF state is entered from the ON-ON state, the periodic sequence

$$\cdots \rightarrow \boxed{\text{ON-OFF}} \rightarrow \boxed{\text{ON-ON}} \rightarrow \cdots \tag{10.29}$$

can be interrupted only by turning the controllable switch OFF, which brings the converter to the OFF-OFF state. In conclusion, (10.29) is the only periodic sequence of states in which the sequence (10.26) is traversed. Since the S-switch is ON forever, this is not a valid operating mode and the second part of the assertion is proved.

By exclusion of sequences (10.25) and (10.26), possible operating modes with lossless transitions are reduced to the following three:

$$\begin{aligned}
&\text{mode } I\text{: } \cdots \rightarrow \boxed{\text{ON-ON}} \rightarrow \boxed{\text{ON-OFF}} \rightarrow \boxed{\text{OFF-OFF}} \rightarrow \boxed{\text{OFF-ON}} \rightarrow \cdots, \\
&\text{mode } II\text{: } \cdots \rightarrow \boxed{\text{ON-ON}} \rightarrow \boxed{\text{ON-OFF}} \rightarrow \boxed{\text{OFF-OFF}} \rightarrow \boxed{\text{ON-OFF}} \rightarrow \cdots, \\
&\text{mode } III\text{: } \cdots \rightarrow \boxed{\text{ON-ON}} \rightarrow \boxed{\text{OFF-ON}} \rightarrow \boxed{\text{OFF-OFF}} \rightarrow \boxed{\text{OFF-ON}} \rightarrow \cdots.
\end{aligned} \tag{10.30}$$

In each of these three modes, only one transition (the S-switch turn-OFF) is controllable and, consequently, only variable-frequency control can be applied.

One can now qualitatively describe the operation in modes I_1 and II_1. Assume that initially a ZV-MR converter is in the ON-ON state. Current i_r ramps up linearly until it reaches δ at $\theta = \theta_1$, when the diode switch turns OFF. The subsequent ON-OFF state lasts until the S-switch is turned OFF at $\theta = \theta_2$. This transition is controllable and it transfers the converter to the OFF-OFF state. Subject to initial conditions for the OFF-OFF state, the next state can be either OFF-ON, if the diode voltage reaches zero before the S-switch voltage does, or ON-OFF, if the S-switch voltage drops to zero first. In the first case, the switching cycle is completed when the S-switch voltage drops to zero at $\theta = \theta_4$ and the ON-ON state is entered again. In the second case, the ON-OFF state terminates when the diode voltage drops to zero. These two cases correspond to operating modes I_1 and II_1, respectively.

For a description of operation in mode III_1, assume again that the initial state is ON-ON. Transition to the OFF-ON state is achieved by turning the S-switch OFF at $\theta = \theta_1$, before the diode switch ceases to conduct. The converter stays in the OFF-ON state until the diode switch turns OFF at $\theta = \theta_2$ and the next state, OFF-OFF, is entered. With the

initial conditions $I_{ff} = \delta$, $V_{ff} > 0$ and $V'_{ff} = 0$, the OFF-OFF state is followed by the OFF-ON state. The OFF-ON state is entered at $\theta = \theta_3$ when the diode voltage drops to zero and the diode switch turns ON again. The cycle is completed at $\theta = \theta_4$ when the S-switch voltage drops to zero and the ON-ON state is re-entered.

Typical waveforms illustrating operation of a ZV-MR converter in each of the three operating modes are shown in Fig. 10.2. While the S-switch current is negative, the state of its transistor is irrelevant, as indicated by the hatched area in the waveform of the transistor control signal p_t.

10.2.2 Implementation with Two Controllable Switches

If both switches are implemented as controllable current-bidirectional, the augmented state-transition diagram is shown in Fig. 10.3. Sequence (10.25) cannot be part of a valid operating mode by the same argument as before. However, since i_{r1} can now be greater than δ, sequence (10.26) cannot be excluded. This enables an additional operating mode with all transitions at zero voltage,

$$\text{mode } IV\text{: } \cdots \rightarrow \boxed{\text{ON-ON}} \rightarrow \boxed{\text{OFF-ON}} \rightarrow \boxed{\text{ON-ON}} \rightarrow \boxed{\text{ON-OFF}} \rightarrow \cdots . \qquad (10.31)$$

In all four operating modes, there are two controllable transitions so that control at constant switching frequency is possible.

Operation in modes I_2, II_2 and III_2 is essentially the same as in modes I_1, II_1 and III_1, respectively. The only difference stems from the fact that now the $\hat{S}$-switch can be turned OFF at any current $i_d \leq 0$.

In mode IV_2, one can assume that initially both switches are ON so that current i_r ramps up linearly. The next state, OFF-ON, is entered by turning the S-switch OFF at $\theta = \theta_1$. In the OFF-ON state, the $\hat{S}$-switch is held ON until the S-switch voltage returns to zero at $\theta = \theta_2$. The second ON-ON state is terminated by turning the $\hat{S}$-switch OFF at $\theta = \theta_3$ so that the ON-OFF state is entered. Finally, the converter returns to the initial ON-ON state at $\theta = \theta_4$ when the S-switch voltage reaches zero and the switching cycle is completed.

For any of the four operating modes, part of the switching cycle between two controllable (turn-OFF) transitions (relative to the switching period) can be defined as the

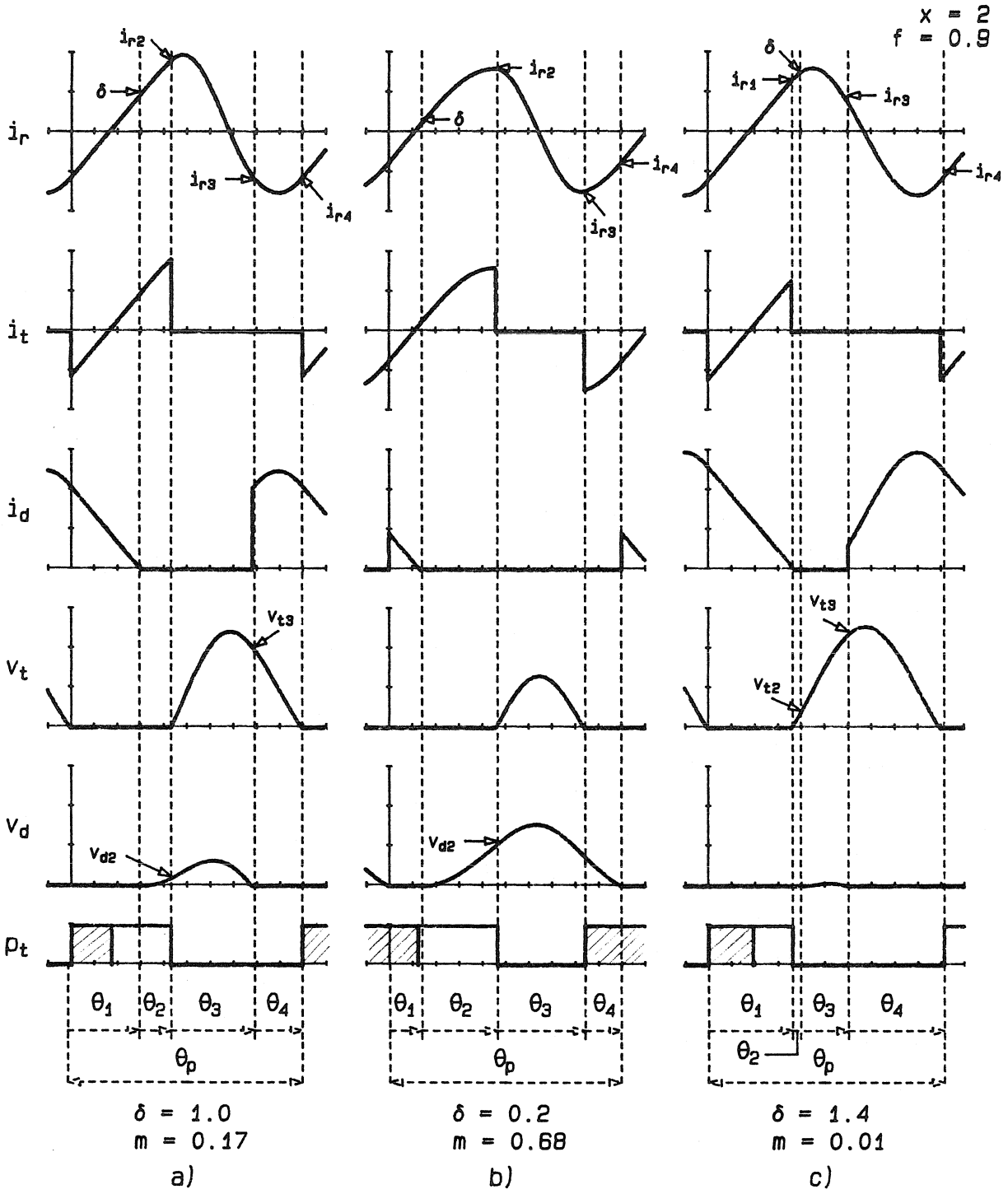


Figure 10.2: Typical waveforms for a ZV-MR converter operating in modes I_1 (a), II_1 (b) or III_1 (c).

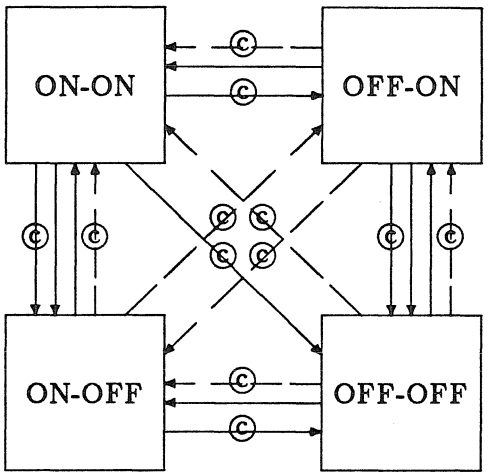


Figure 10.3: State transition diagram for ZV-MR converters with two controllable, current-bidirectional switches.

control variable D_c:

$$D_c = \begin{cases} \theta_2/\theta_p\,, & \text{in modes } I_2 \text{ and } II_2, \\ -\theta_2/\theta_p\,, & \text{in mode } III_2, \\ (\theta_2+\theta_3)/\theta_p\,, & \text{in mode } IV_2. \end{cases} \tag{10.32}$$

Typical waveforms in a ZV-MR converter are shown in Fig. 10.4 for modes I_2, II_2 and III_2 and in Fig. 10.5 for mode IV_2. In each case, hatched areas in waveforms of transistor control signals, p_t or p_d, label intervals when the state of the transistor in a current-bidirectional switch is arbitrary because the antiparallel diode of the switch is ON.

10.3 Variable-Frequency Control: DC Analysis

DC analysis of ZV-MR converters is complicated by the fact that the operating mode with all transitions at zero voltage is not unique.

Assume that a ZV-MR converter operates in mode I_1 or in mode II_1. At the end of the ON-ON state, the initial conditions for the next ON-OFF state are known: $I_{nf} = \delta$, $V'_{nf} = 0$. Since transition from the ON-OFF to the OFF-OFF state is controllable, θ_2 can be treated as a known parameter. Given θ_2, the initial conditions $I_{ff} = i_r(\theta_2) = i_{r2}$, $V'_{ff} = v_d(\theta_2) = v_{d2}$ for the OFF-OFF state are found by direct substitution in Eqs. (10.13) and (10.14). A closed form solution is not possible for the equations $v_d(\theta_3) = 0$ (mode

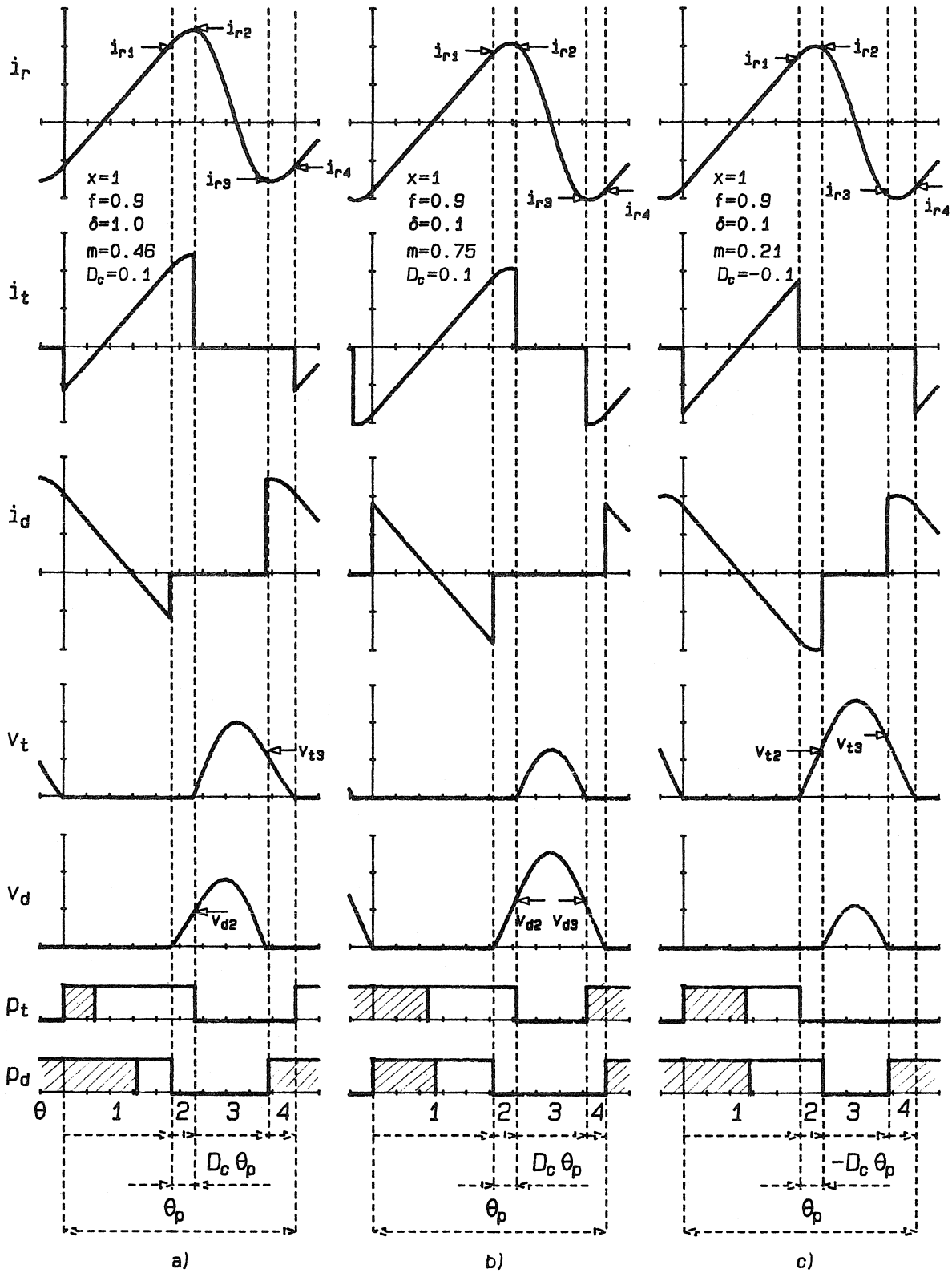


Figure 10.4: Typical waveforms in a ZV-MR converter operating in modes I_2 (a), II_2 (b) or III_2 (c).

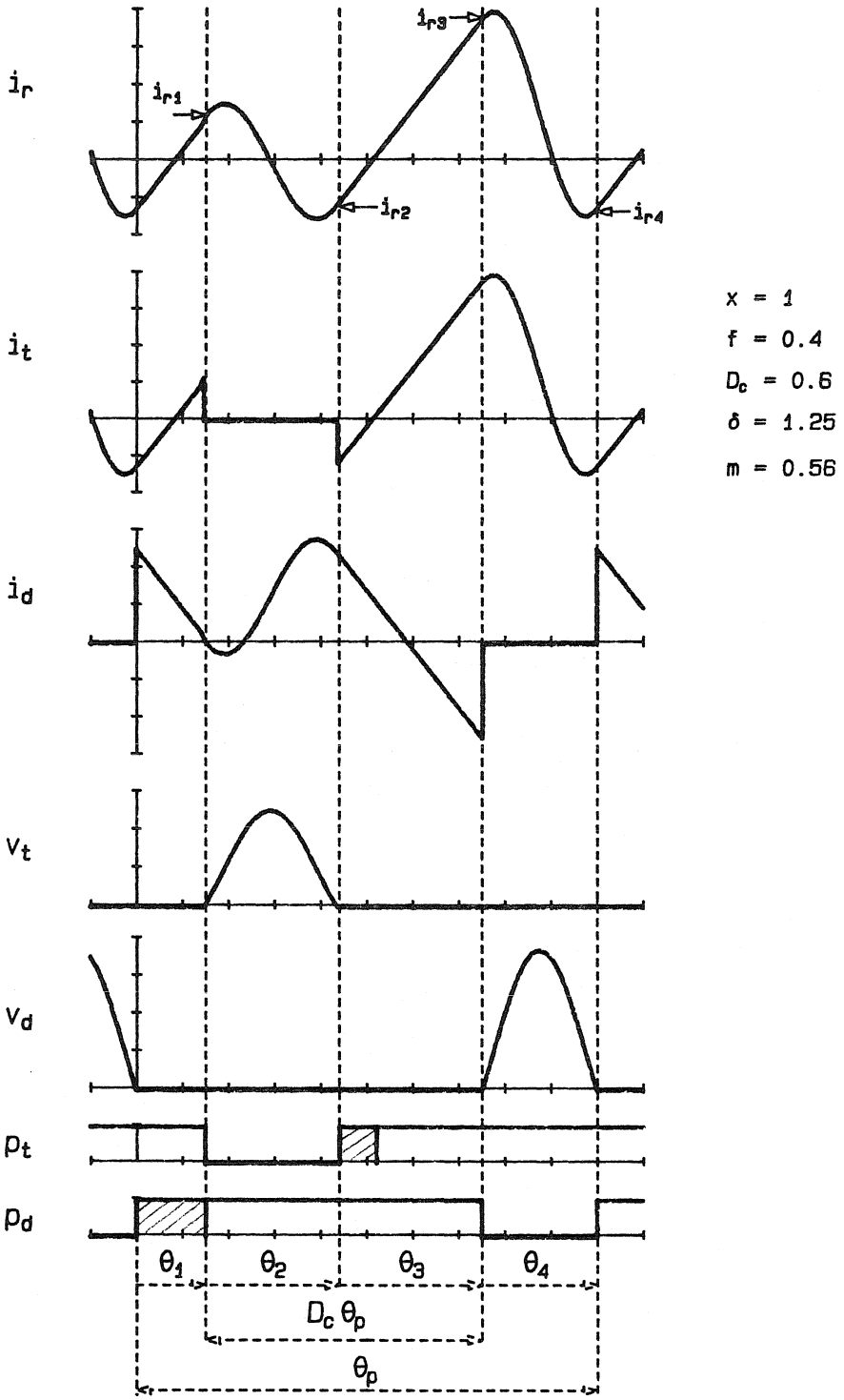


Figure 10.5: Typical waveforms in a ZV-MR converter operating in mode IV_2.

I_1) or $v_t(\theta_3) = 0$ (mode II_1) in the OFF-OFF state. For a given set of parameters, the solution has to be found numerically, and details of a numerical procedure are given in Appendix B.3. Once the solution for θ_3 is found, initial conditions for the following state are known.

Suppose that in the OFF-OFF state the diode voltage drops to zero at $\theta = \theta_3$, while $v_{t3} = v_t(\theta_3) > 0$. The converter operates in mode I_1. The succeeding OFF-ON state lasts until the S-switch voltage reaches zero at $\theta = \theta_4$. With known initial conditions, $I_{fn} = i_{r3}$ and $V_{fn} = v_{t3}$, the solutions for θ_4 and i_{r4}, if they exist, are given by

$$\theta_4 = \arctan \frac{1}{\sqrt{i_{r3}^2 + (1 - v_{t3})^2 - 1}} + \arctan \frac{1 - v_{t3}}{i_{r3}} + \begin{cases} \pi & \text{if } i_{r3} > 0 \\ 0 & \text{if } i_{r3} < 0 \end{cases}, \quad (10.33)$$

$$i_{r4} = -\sqrt{i_{r3}^2 + (1 - v_{t3})^2 - 1}\,. \quad (10.34)$$

If the converter operates in mode II_1, the OFF-OFF state is followed by the ON-OFF state. If the solution to the equation $v_d(\theta_4) = 0$ in the ON-OFF state exists, it is given by

$$\theta_4 = \sqrt{x}\left(\arctan \frac{1}{\sqrt{(i_{r3} - \delta)^2 + x(v_{d3} - 1)^2 - x}} + \arctan \frac{1 - v_{d3}}{i_{r3} - \delta}\right), \quad (10.35)$$

$$i_{r4} = \delta - \sqrt{(i_{r3} - \delta)^2 + x(v_{d3} - 1)^2 - x}\,. \quad (10.36)$$

With the initial condition $I_{nn} = i_{r4}$, duration of the ON-ON state is

$$\theta_1 = \delta - i_{r4}\,. \quad (10.37)$$

Assuming that θ_2 is a given parameter, all other state durations and initial conditions can be determined. Finally, the equivalent duty ratio m can be found by averaging the diode current over one switching period. For mode I_1,

$$m = 1 - \frac{1}{2\delta}\frac{\theta_1^2}{\theta_p}, \quad (10.38)$$

while for mode II_1,

$$m = 1 - \frac{1}{2\delta}\frac{\theta_1^2 + 2\delta\theta_4 + 2i_{r3}}{\theta_p}. \quad (10.39)$$

No-load operation

Under the no-load condition ($\delta = 0$), it is possible to solve the OFF-OFF equations explicitly. For $\delta = 0$ in the OFF-OFF state we have $v_d = v_t + v_{d2}/x$. Since $v_{d2} > 0$, the

S-switch voltage (v_t) drops to zero before $v_d = 0$ and therefore, the converter operates in mode II_1. In this case, closed form results can be obtained for f and m as functions of the parameter θ_2,

$$f(\delta = 0) = \frac{2\pi}{2\theta_2 + \theta_3}, \tag{10.40}$$

$$m(\delta = 0) = 1 - 2\frac{\sqrt{x}\sin\frac{\theta_2}{\sqrt{x}} + \frac{\theta_3}{2}\cos\frac{\theta_2}{\sqrt{x}}}{2\theta_2 + \theta_3}\frac{x}{1+x}, \tag{10.41}$$

where

$$\theta_3 = 2\sqrt{\frac{1+x}{x}}\left[\pi - \arctan\left(\sqrt{1+x}\tan\frac{\theta_2}{\sqrt{x}}\right)\right]. \tag{10.42}$$

The minimum possible equivalent duty ratio at zero load, given by

$$m_{min}(\delta = 0) = \frac{1}{1+x}, \tag{10.43}$$

is attained for $\theta_2 = 0$. The switching frequency resulting in $m(\delta = 0) = m_{min}(\delta = 0)$,

$$f_{max} = \sqrt{\frac{1+x}{x}}, \tag{10.44}$$

is the maximum normalized frequency for the entire combined operating region for modes I_1 and II_1.

Conditions for operation in modes I_1 and II_1

In the ON-OFF state with $I_{nf} = \delta$ and $V_{nf} = 0$, $v_d \geq 0$ for all θ. Thus, duration of the ON-OFF state, $\theta_2 \geq 0$, can be determined externally by controlling the S-switch turn-OFF. Choice of θ_2 affects the resulting frequency f and the equivalent duty ratio m. The effect that can be easily comprehended is that increasing θ_2 contributes to lower f and larger m, just because the S-switch ON-time is longer. Thus, one would expect that both m and f are monotonous functions of θ_2, and that m is a monotonously decreasing function of normalized frequency f for $\delta = const.$ However, the effects of θ_2 on m and f through altered initial conditions for the next state are not as obvious and may result in a quite opposite trend. Indeed, it has been found by simulations of a ZV-MR converter [16] that control-to-output DC characteristics may become non-monotone as the switching frequency is decreased.

For $\delta = const.$, the equivalent duty ratio increases monotonously as the switching frequency is decreased down to some minimum switching frequency, f_m. The minimum switching frequency (f_m) is determined by one of the following events:

1. $m(f = f_m) = 1$;
2. some condition for operation in modes I_1 and II_1 is not satisfied so that lossless transitions are not possible for $f < f_m$; or
3. m starts to decrease with decreasing f below f_m.

In the first two cases, the operating point is at the boundary of the operating region. The third case is not encountered in QR converters with two resonant elements. Although it is inside the operating region with all zero-voltage transitions, the non-monotone part of the control-to-output DC characteristic is not acceptable in practice. Positive and negative slopes in the control-to-output characteristic render impossible closing a stable feedback loop. Therefore, the valid operating region for ZV-MR converters in modes I_1 and II_1 is taken as part of the operating region in which characteristics are monotone.

The OFF-OFF state terminates with $v_d(\theta_3) = 0$ or with $v_t(\theta_3) = 0$ for any viable set of initial conditions and parameters. Thus, the only condition for operation in modes I_1 and II_1 emerges from the succeeding OFF-ON or ON-OFF state. For mode I_1, solution (10.33) exists if

$$i_{r3}^2 + (1 - v_{t3})^2 \geq 1\,. \tag{10.45}$$

Furthermore, the OFF-OFF state must not be re-entered before $\theta = \theta_4$, or

$$i_r \leq \delta \quad \text{for} \quad 0 < \theta < \theta_4\,. \tag{10.46}$$

For mode II_1, solution (10.35) exists if

$$(i_{r3} - \delta)^2 + x(1 - v_{t3})^2 \geq x\,. \tag{10.47}$$

This is also sufficient to guarantee transition to the ON-ON state since initial condition i_{r3} has to be less than zero, and the S-switch can be turned ON to prevent possible transition back to the OFF-OFF state if $i_{r3} = 0$ for some $\theta < \theta_3$. Finally, i_{r4} found from (10.33) or (10.35) is always less than δ so that θ_4 is necessarily non-negative.

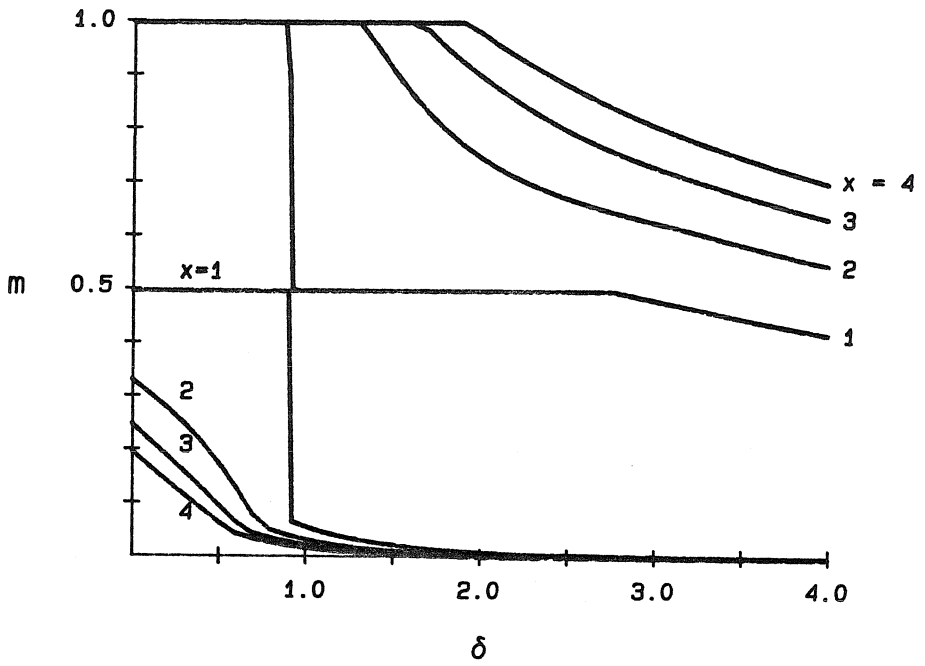


Figure 10.6: Combined operating regions for a ZV-MR converter in modes $(I, II)_1$ with x as a varying parameter.

Using the results of DC analysis, conditions for operation in modes I_1 or II_1 can be verified for any given δ and θ_2.

Boundaries of the combined operating region for modes I_1 and II_1 with monotone control-to-output characteristics are shown in Fig. 10.6 for different values of the parameter x. The available operating region in the load-to-output plane widens as x is increased. Also, the minimum possible value for the equivalent duty ratio at no load decreases with x as predicted by Eq. (10.43).

Operating Mode III_1

For operation in mode III_1, it is necessary that $i_{r1} \leq \delta$. The maximum possible value for the equivalent duty ratio in mode III_1 is on the boundary curve that separates operating regions of modes III_1 and II_1. It can be shown that the maximum does not exceed $m = 0.1$ for any value of the parameter x. Since this is a very restricted region in the load-to-output plane, mode III_1 can be ignored for all practical purposes.

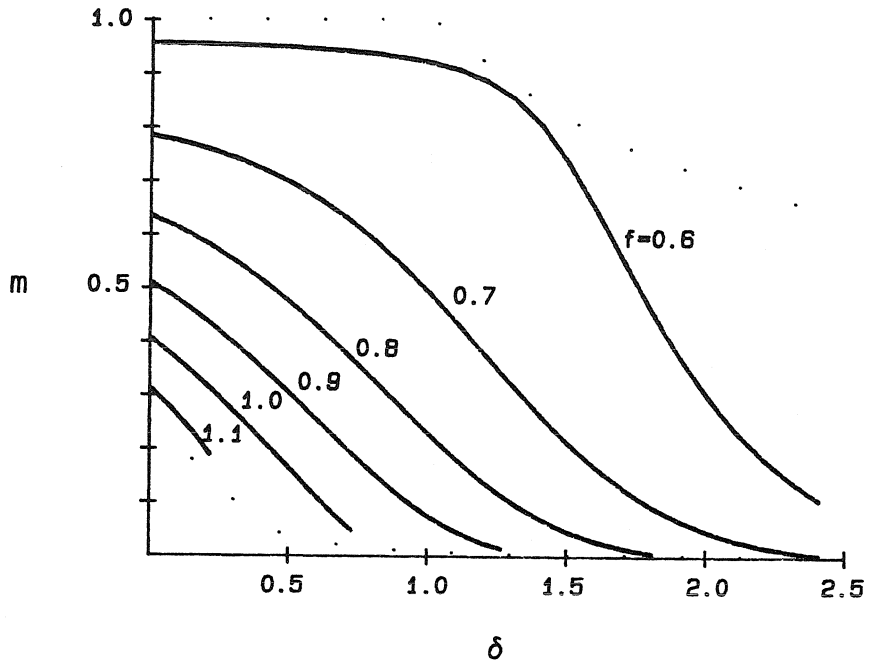


Figure 10.7: Load-to-output DC characteristics of a ZV-MR converter operating in modes $(I, II)_1$.

DC characteristics

DC characteristics of frequency-controlled ZV-MR converters are shown in Figs 10.7 and 10.8 for $x = 3$.

10.4 Constant-Frequency Control: DC Analysis

10.4.1 Operating Modes I_2 and II_2

DC analysis equations of Section 10.3 for ZV-MR converters in modes I_1 and II_1 are directly applicable here with three adjustments:

1. the initial condition for current i_r at the beginning of the ON-OFF state is set to $i_{r1} \geq \delta$,

2. duration of the ON-OFF state is determined by the control variable, $\theta_2 = D_c\theta_p$, $\theta_p = 2\pi/f = const.$,

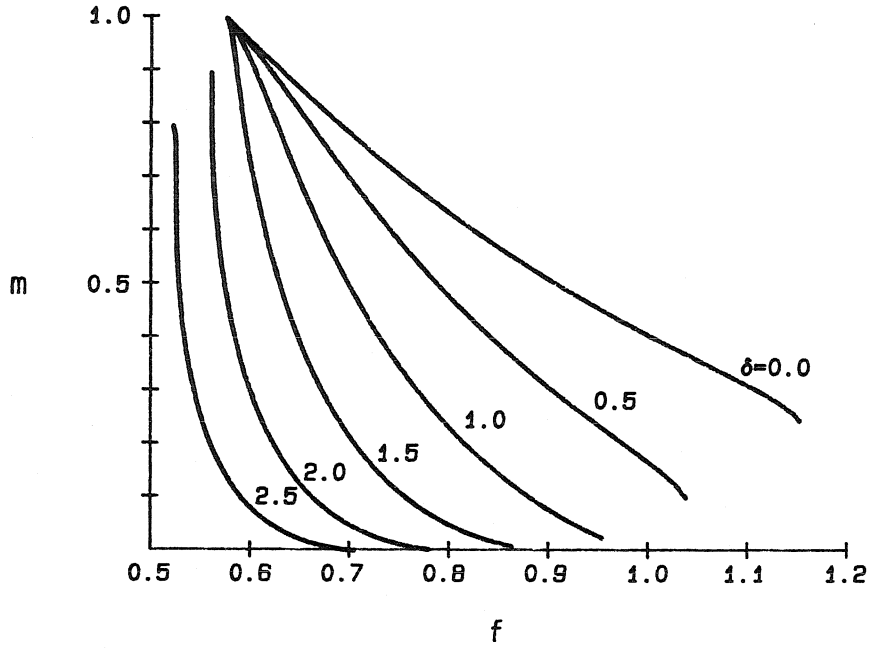


Figure 10.8: Control-to-output DC characteristics of a ZV-MR converter operating in modes $(I, II)_1$.

3. duration of the initial ON-ON state is determined so that switching frequency is constant. Therefore,

$$\theta_1 = \theta_p - \theta_2 - \theta_3 - \theta_4 , \tag{10.48}$$

$$i_1 = i_4 + \theta_1 . \tag{10.49}$$

An expression for m is obtained by averaging the S-switch or the $\hat{S}$-switch current over one switching cycle:

$$m = \frac{\delta\theta_2 + x(\delta - i_{r2}) + \frac{1}{2}\theta_1(i_{r1} + i_{r4})}{\theta_p \delta} \tag{10.50}$$

and

$$m = 1.0 - \frac{\delta - \frac{1}{2}(i_{r1} + i_{r4})}{\theta_p \delta}\theta_1 \tag{10.51}$$

in modes I_2 and II_2, respectively.

Conditions for Operation in Modes I_2 and II_2

The S-switch turn-OFF is effective if $i_t \geq 0$. Similarly, the $\hat{S}$-switch turn-OFF prompts the state transition if $i_d \leq 0$. In terms of current i_r, these two conditions become

$$i_{r1} \geq \delta , \tag{10.52}$$

$$i_{r2} \geq 0 . \tag{10.53}$$

Since period θ_p is fixed, one must check to see if duration of the ON-ON state is non-negative,

$$\theta_1 \geq 0 . \tag{10.54}$$

The remaining conditions, (10.45) and (10.46) for mode I_2 and (10.47) for mode II_2, are carried over from the analysis of ZV-MR converters in modes I_1 and II_1.

10.4.2 Operating Mode III_2

In mode III_2, the S-switch is turned OFF before the $\hat{S}$-switch. The OFF-ON state is entered with the initial condition $I_{fn} = i_{r1}$ and its duration is determined by the control variable,

$$\theta_2 = -D_c \theta_p . \tag{10.55}$$

Initial conditions for the succeeding OFF-OFF state are found by direct substitution of θ_2 in Eqs. (10.15) and (10.16). Steady-state equations for the rest of the switching period are exactly the same as corresponding equations for mode I_2.

The equivalent duty ratio m in mode III_2 is found by averaging the S-switch current over one cycle,

$$m = \frac{1}{2} \frac{i_{r1} + i_{r4}}{\theta_p \delta} \theta_1 . \tag{10.56}$$

Conditions for Operation in Mode III_2

If the S-switch current is negative at $\theta = \theta_2$ when the S-switch is turned OFF, the state transition does not occur. Hence, for operation in mode III_2, it is necessary that

$$i_{t1} = i_{r1} \geq 0 . \tag{10.57}$$

In the OFF-ON state, the $\hat{S}$-switch must be turned OFF before v_t reaches zero and the diode must not cease to conduct before $\theta = \theta_2$. The conditions are given by

$$\theta_2 < 2(\pi - \arctan i_{r1}), \tag{10.58}$$

$$i_{r2} > \delta. \tag{10.59}$$

The succeeding OFF-OFF state is necessarily followed by the second OFF-ON state in which the S-switch voltage must drop to zero for some $\theta = \theta_4 \geq 0$. This is possible if

$$i_{r3}^2 + (1 - v_{t3})^2 > 1. \tag{10.60}$$

As in modes I_2 and II_2, duration of the final ON-ON state must be non-negative,

$$\theta_1 \geq 0. \tag{10.61}$$

10.4.3 Combined Operating Region and DC Characteristics in Modes I_2, II_2 and III_2

Operating regions and DC characteristics for modes $(I, II, III)_2$ are combined together. Two design parameters affect the extent of the combined operating region – normalized switching frequency (f) and the ratio of resonant capacitance values (x). Let us first examine the extreme values of the equivalent duty ratio, $m = 0$ and $m = 1$.

In a ZV-MR converter with two controllable switches, $m = 0$ is always attainable simply by holding the $\hat{S}$-switch ON indefinitely. The question is whether $m = 0$ can be attained while simultaneously operating in one of modes I_2, II_2 or III_2, for some control duty ratio D_c. To achieve $m = 0$, the converter must operate in mode III_2 with $D_c < 0$ adjusted so that duration of the OFF-OFF state is zero. Mode III_2 is effectively reduced to the periodic sequence

$$\cdots \rightarrow \boxed{\text{ON-ON}} \rightarrow \boxed{\text{OFF-ON}} \rightarrow \cdots, \tag{10.62}$$

where duration of the ON-ON state is θ_1 and duration of the OFF-ON state is $\theta_2 + \theta_4$. If this periodic sequence is possible with all lossless transitions, θ_1 must satisfy

$$\theta_1 = 2\pi\left(\frac{1}{f} - 1\right) + 2\arctan\frac{\theta_1}{2}. \tag{10.63}$$

A non-negative solution for θ_1 exists iff

$$f \leq 1. \tag{10.64}$$

In conclusion, $m = 0$ axis is a boundary curve for operation in mode III_2 if the normalized frequency f is less than or equal to 1.

The other extreme, $m = 1$, is attained in mode II_2 with $\theta_3 = 0$. Mode II_2 reduces to the periodic sequence

$$\cdots \rightarrow \boxed{\text{ON-ON}} \rightarrow \boxed{\text{ON-OFF}} \rightarrow \cdots . \tag{10.65}$$

Duration of the ON-ON state, θ_1, must satisfy

$$\theta_1 = 2\pi\left(\frac{1}{f} - \sqrt{x}\right) + 2\sqrt{x}\arctan\frac{\theta_1}{2}. \tag{10.66}$$

The equation can be solved for non-negative θ_1 iff

$$f \leq \frac{1}{\sqrt{x}}. \tag{10.67}$$

Thus, if normalized frequency f and parameter x satisfy the last condition, $m = 1$ is part of the boundary curve for mode II_2.

In the δ direction, boundaries of the combined operating region for modes $(I, II, II)_2$ are found numerically.

The plots in Figs. 10.9 and 10.10 reveal the roles of parameters x and f with respect to boundaries of the operating region. In all cases, the combined operating region for modes $(I, II, III)_2$ encloses the no load axis and spans full range of equivalent duty ratios up to some maximum load δ_{max}. In general, δ_{max} is higher for lower frequency as illustrated by the plots in Fig. 10.9. It is interesting that δ_{max} is smaller and that the operating region shrinks for larger x, contrary to the trend found in the study of operating regions for modes $(I, II)_1$.

DC Characteristics

DC characteristics in the load-to-output and control-to-output planes for $x = 1$ and $f = 0.9$ are shown in Figs. 10.11 and 10.12. Numerical procedures used to compute DC characteristics are discussed in Appendix B.3.

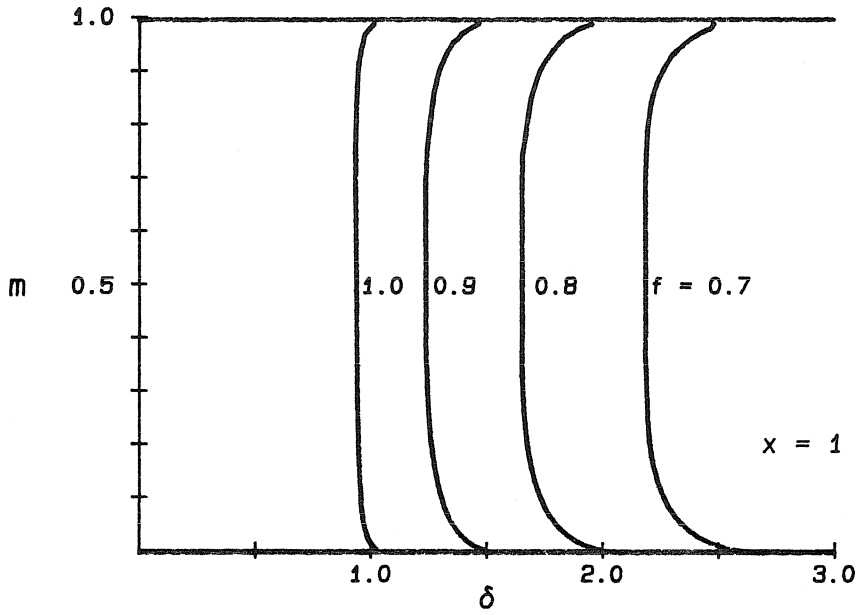


Figure 10.9: Boundaries of the combined operating regions for modes $(I, II, III)_2$ with normalized frequency f as a varying parameter.

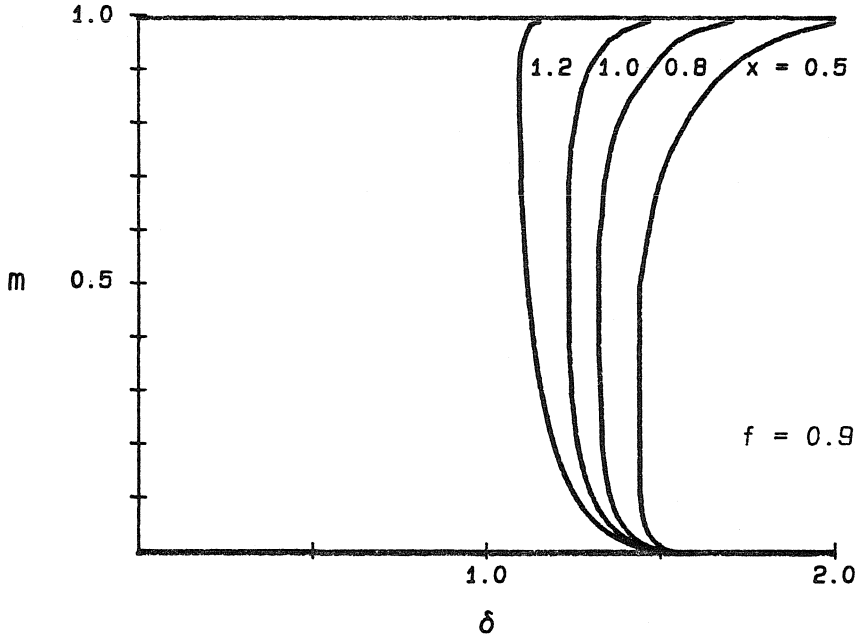


Figure 10.10: Boundaries of the combined operating regions for modes $(I, II, III)_2$ with the ratio of resonant capacitors x as a varying parameter.

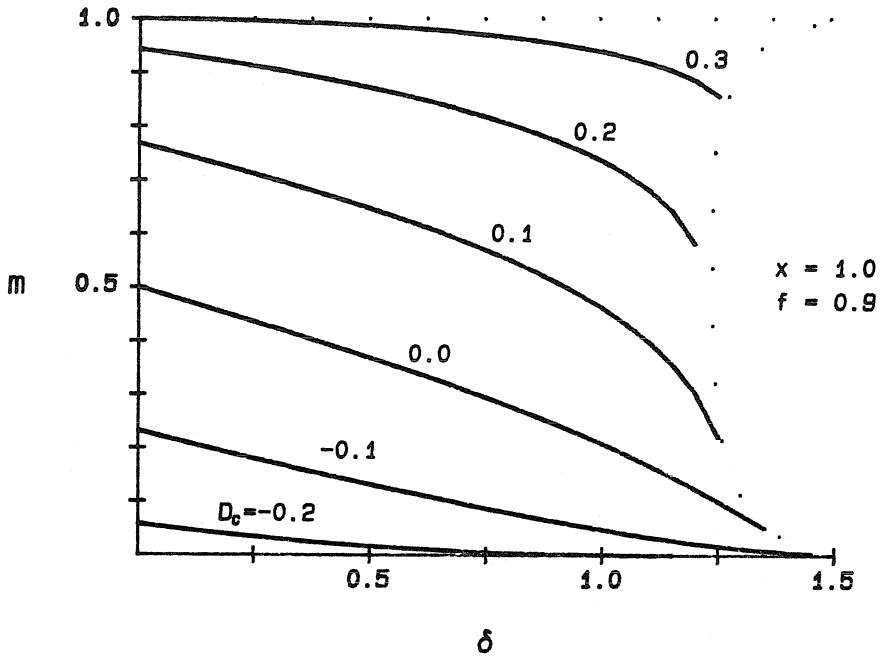


Figure 10.11: Load-to-output DC characteristics of a ZV-MR converter operating in modes $(I, II, III)_2$.

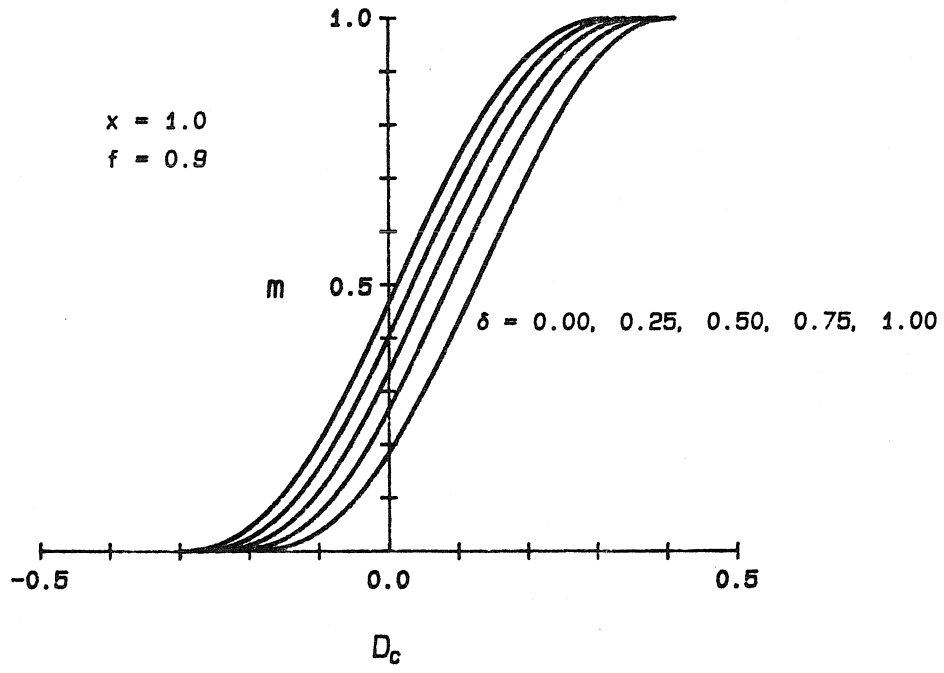


Figure 10.12: Control-to-output DC characteristics of ZV-MR converters in modes $(I, II, III)_2$.

10.4.4 Operating Mode IV_2

The operating region for mode IV_2 overlaps in part with operating regions for the other three modes. In contrast to modes $(I, II, III)_2$, the controllable period $D_c\theta_p$ extends over two adjacent states, OFF-ON and ON-ON. Inevitably, compared to the other three modes, implementation of the control signals is quite different. Furthermore, the OFF-OFF state is never entered in mode IV_2. These are the reasons that mode IV_2 is considered apart from operation in the other three modes.

Suppose, as before, that current i_r is equal to i_{r1} at the end of the first ON-ON interval. With the initial conditions $I_{fn} = i_{r1}$ and $V_{fn} = 0$, the equation $v_t(\theta_2) = 0$ in the succeeding OFF-ON state can be solved for θ_2 and i_{r2}:

$$\theta_2 = 2(\pi - \arctan i_{r1}), \tag{10.68}$$

$$i_{r2} = -i_{r1}. \tag{10.69}$$

The next ON-ON period is entered with the initial conditions $I_{fn} = i_{r2}$ and $V_{fn} = 0$. Duration of the state is determined by the control variable $\theta_c = D_c\theta_p$:

$$\theta_3 = \theta_c - \theta_2, \tag{10.70}$$

$$i_{r3} = i_{r2} + \theta_c - \theta_2. \tag{10.71}$$

With the initial conditions $I_{nf} = i_{r3}$ and $V_{nf} = 0$, the solution to $v_d(\theta_4) = 0$ in the ON-OFF state is given by

$$\theta_4 = 2\sqrt{x}(\pi - \arctan \frac{i_{r3} - \delta}{\sqrt{x}}), \tag{10.72}$$

$$i_{r4} = 2\delta - i_{r3}. \tag{10.73}$$

Finally, the ON-ON state lasts until the end of the switching period so that

$$\theta_1 = \theta_p - \theta_c - \theta_4, \tag{10.74}$$

$$i_{r1} = i_{r4} + \theta_p - \theta_c - \theta_4. \tag{10.75}$$

If conditions for existence of all solutions for state durations θ_i and currents i_{ri} are satisfied and furthermore, if the system of Eqs. (10.68) through (10.75) has a solution,

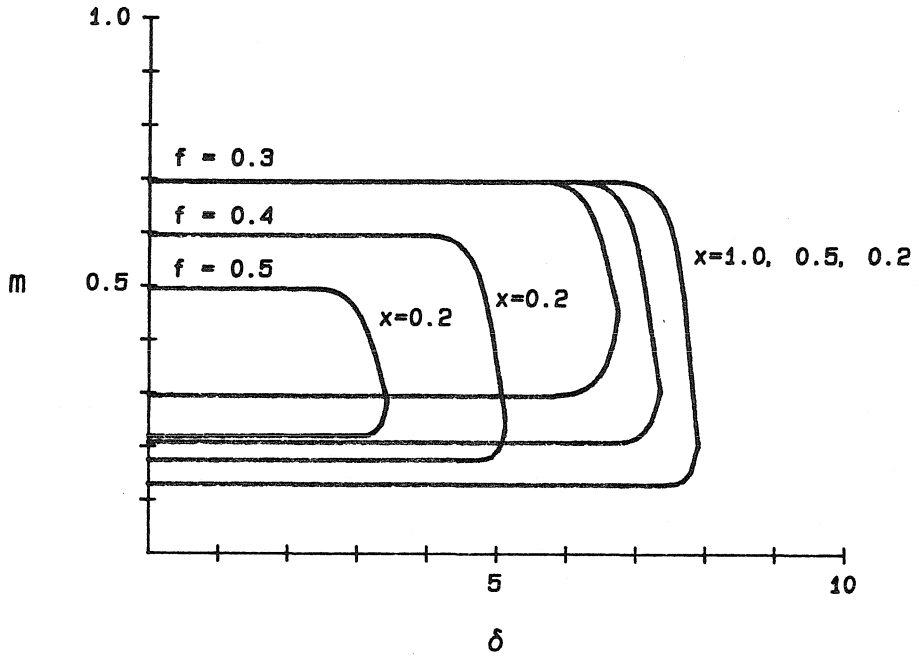


Figure 10.13: Operating regions for a ZV-MR converter in mode IV_2 for various values of the parameters f and x.

Again, δ_2 is larger for lower f and smaller x.

The operating regions for mode IV_2 in the load-to-output plane for different values of the parameters x and f are shown in Fig. 10.13. It is interesting that the operating regions collapse abruptly for loads exceeding δ_1 and δ_2.

DC Characteristics

As an example, DC characteristics are found numerically for one particular pair of values for parameters x and f, both in control-to-output and load-to-output planes. The characteristics are shown in Figs. 10.14 and 10.15. Numerical procedures used in the analysis of mode IV_2 are outlined in Appendix B.3.

10.5 Experimental Verification

An experimental ZV-MR converter is shown in Fig. 10.16. Parent PWM topology is the second-order buck converter with $M(D) = D$. Resonant capacitors C_r and xC_r are placed directly in parallel with semiconductor switches, while L_r is placed so that

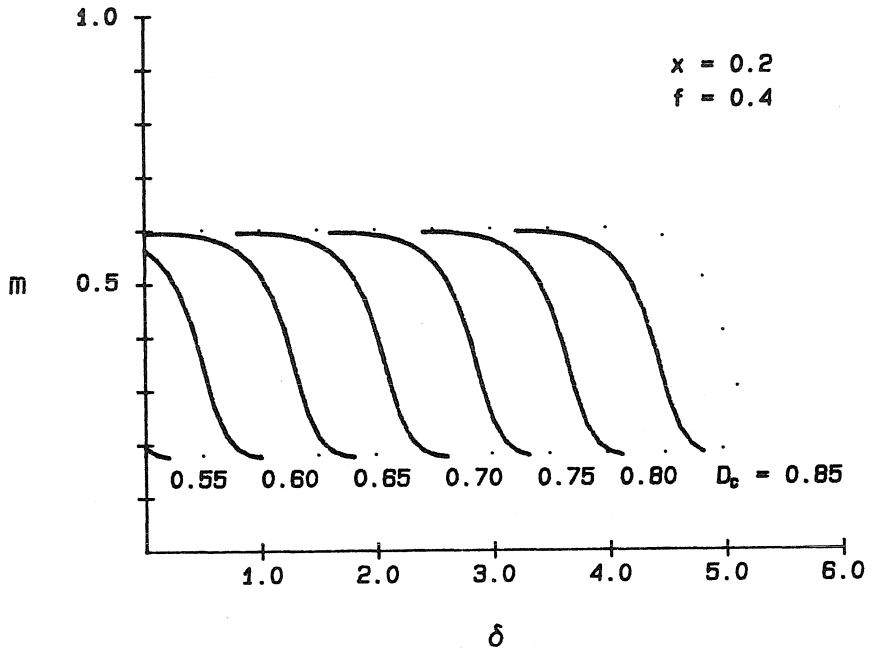


Figure 10.14: Load-to-output DC characteristics of a ZV-MR converter in mode IV_2.

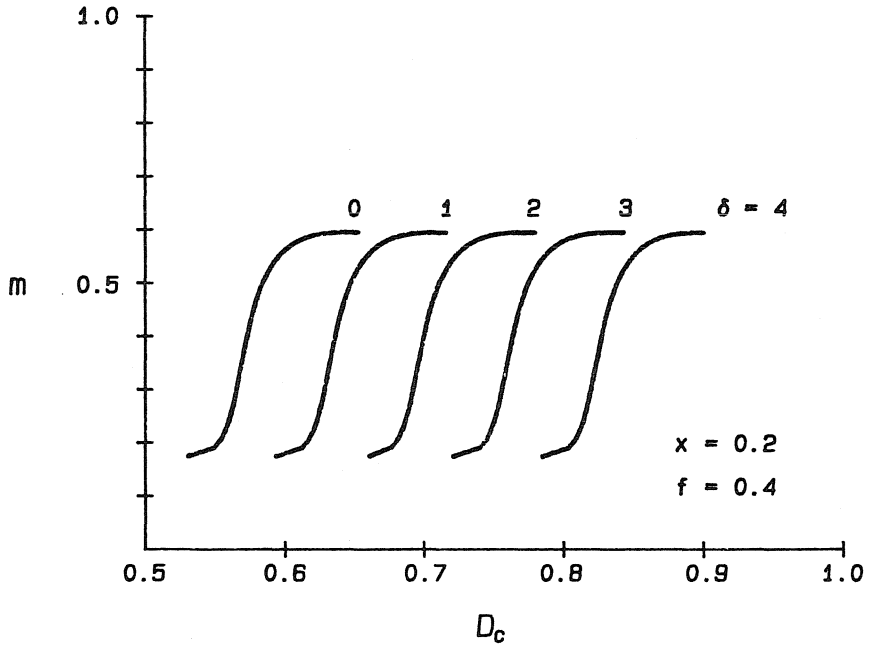


Figure 10.15: Control-to-output DC characteristics of a ZV-MR converter in mode IV_2.

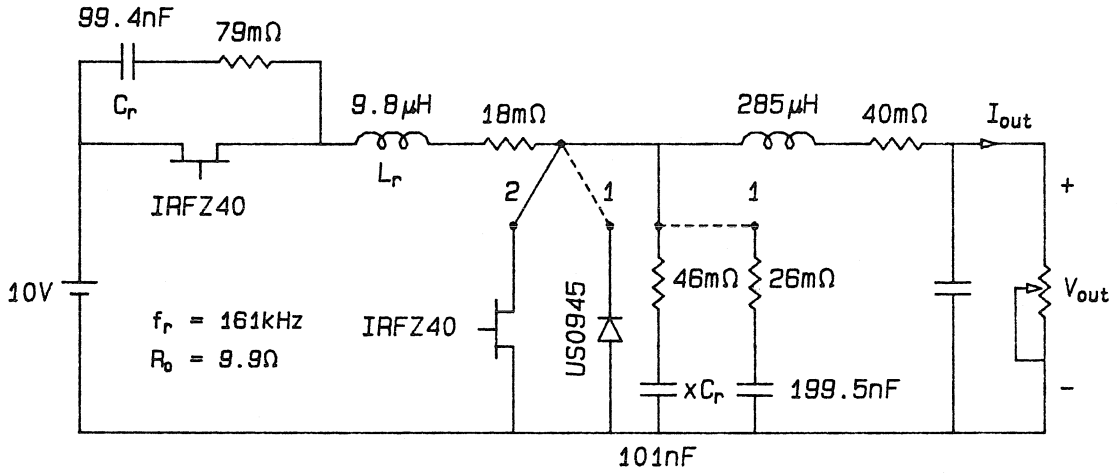


Figure 10.16: An experimental ZV-MR buck converter.

$i_r = i_{L_r}$. For implementation with a single controllable switch (position 1), $x \approx 3$, while for implementation with two controllable switches (position 2), $x \approx 1$.

Recorded waveforms that illustrate operation in modes I_1 and II_1 are shown in Figs. 10.17 (a) and (b). They can be compared to idealized waveforms of Fig. 10.2 since both sets of waveforms are found for approximately equal operating conditions. There are no significant discrepancies between ideal and measured waveforms because all major parasitic reactances are effectively absorbed by the resonant elements. The agreement between predicted and measured DC characteristics in Fig. 10.18 is also satisfactory. It is interesting, however, that for lower loads, measured output voltage is higher than predicted. In order to verify if the error can be ascribed to losses in parasitic series resistances of resonant elements, measurements are repeated with a resistor of 0.1Ω placed in series with C_r, xC_r or L_r. In all cases the output voltage was higher with the resistor than without the resistor. For example, dots in Fig. 10.18 denote the results of the measurement with 0.1Ω in series with C_r. This experimental verification shows that the commonly accepted perception that higher losses necessarily imply lower output voltage is not true in general.

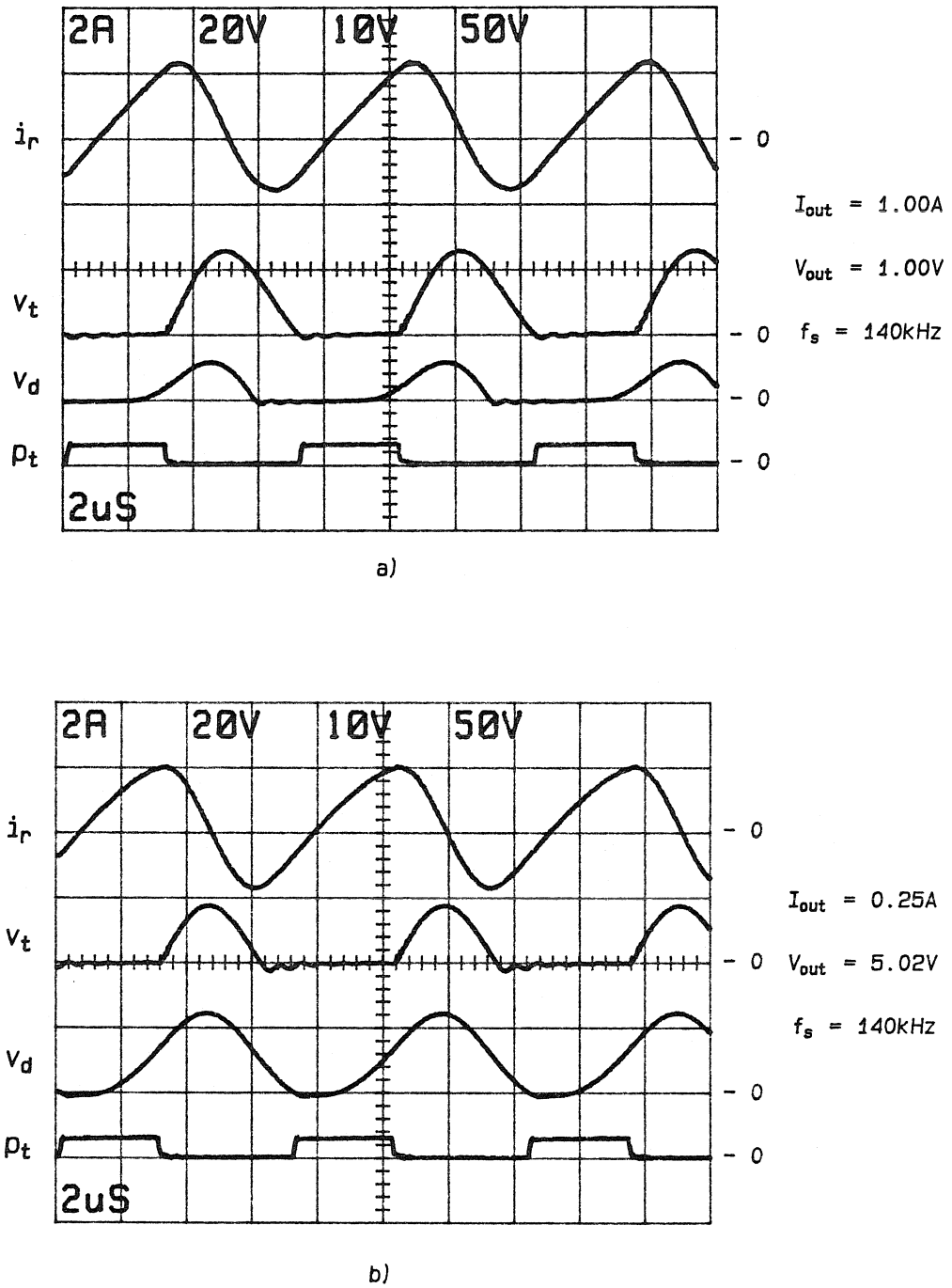


Figure 10.17: Waveforms recorded in the experimental ZV-MR buck converter operating in mode I_1 (a) or II_1 (b).

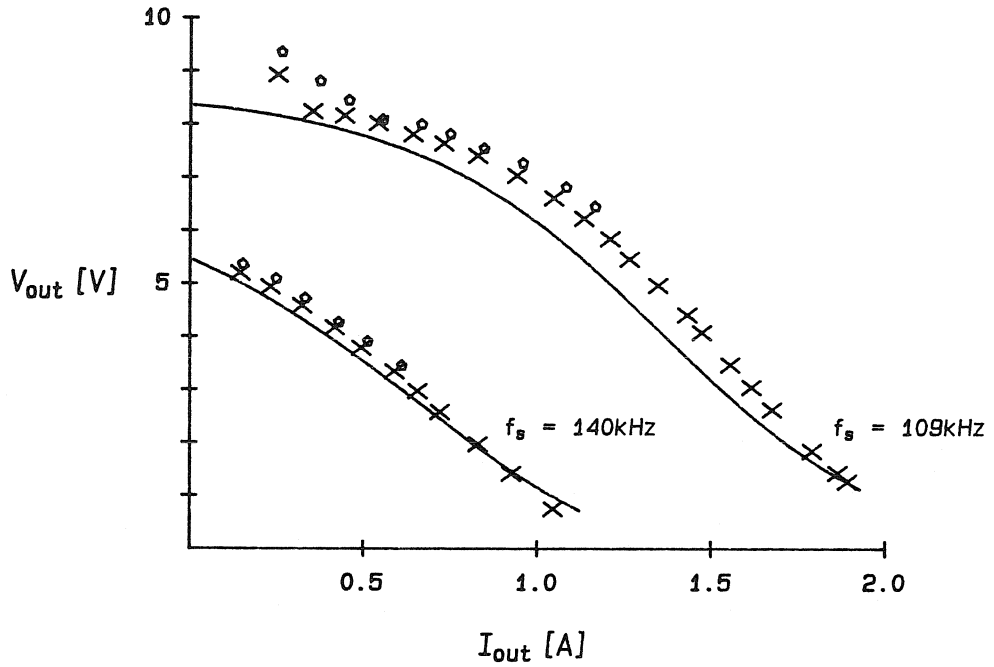


Figure 10.18: Measured and predicted DC characteristics for the experimental ZV-MR buck converter operating in modes I_1 or II_1.

Operation in modes I_2, II_2 and III_2 is confirmed by comparison of ideal waveforms in Fig. 10.4, with experimental waveforms shown in Figs. 10.19, 10.20 and 10.21.

p_t and p_d are constant-frequency, variable-duty-ratio signals used to drive the transistors in the controllable, current-bidirectional switches S and $\hat{S}$, respectively. Control signals are synchronized on the raising edge. By adjusting the two duty ratios, the control variable D_c is set to a desired value. In practice, one switch can be operated at a fixed duty ratio, while control over DC conversion ratio can be achieved by varying the duty ratio of the other switch. As shown in Fig. 10.22, DC characteristics predicted for operation in modes $(I, II, III)_2$ are close to measured characteristics.

Existence of mode IV_2 and corresponding DC characteristics in the load-to-output plane are verified in Fig. 10.23. Waveforms p_t and p_d are constant-frequency, constant-pause signals. Control over the conversion ratio is accomplished by varying the phase shift between p_t and p_d.

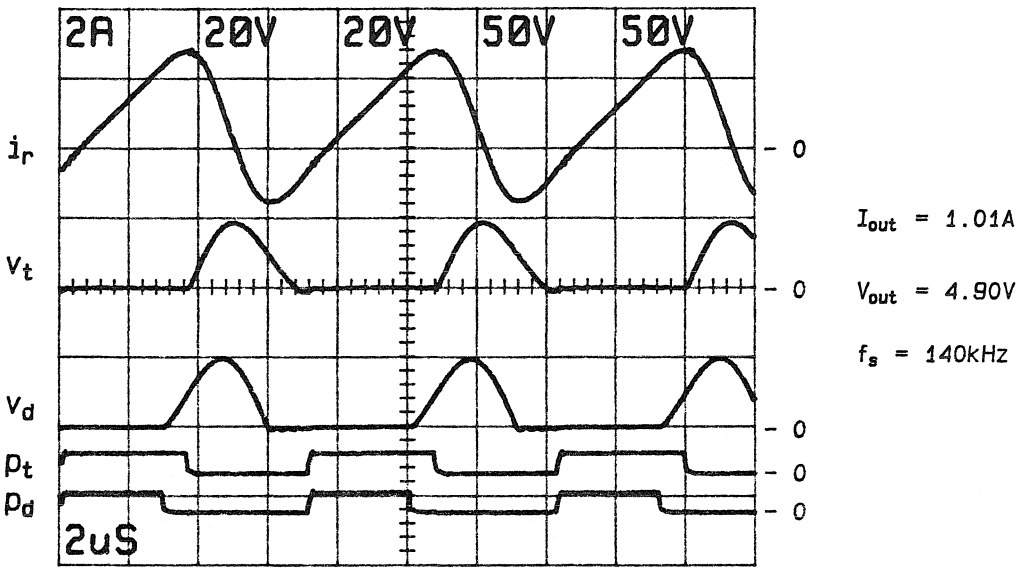


Figure 10.19: Waveforms in the experimental ZV-MR buck converter operating in mode I_2.

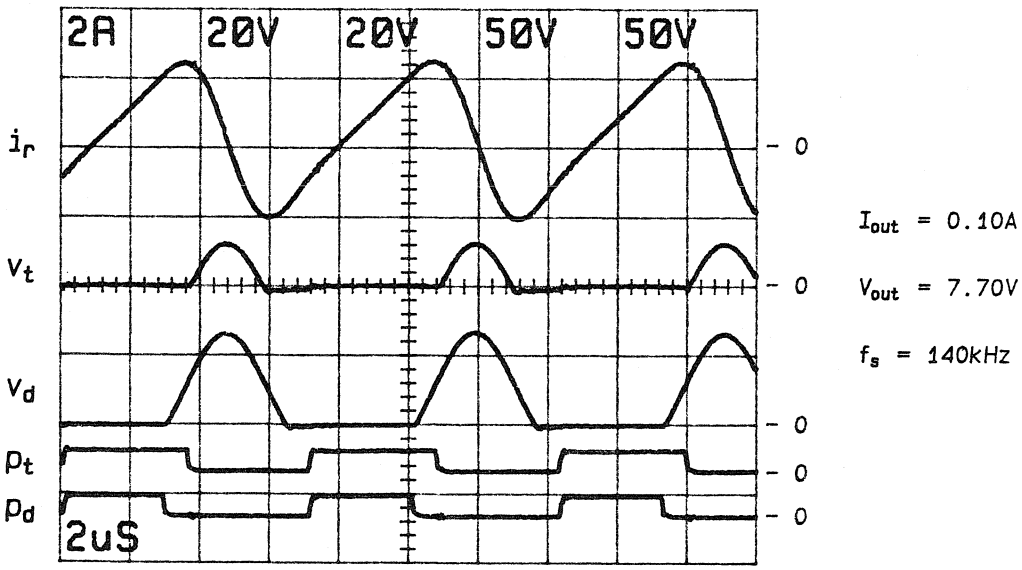


Figure 10.20: Waveforms in the experimental ZV-MR buck converter operating in mode II_2.

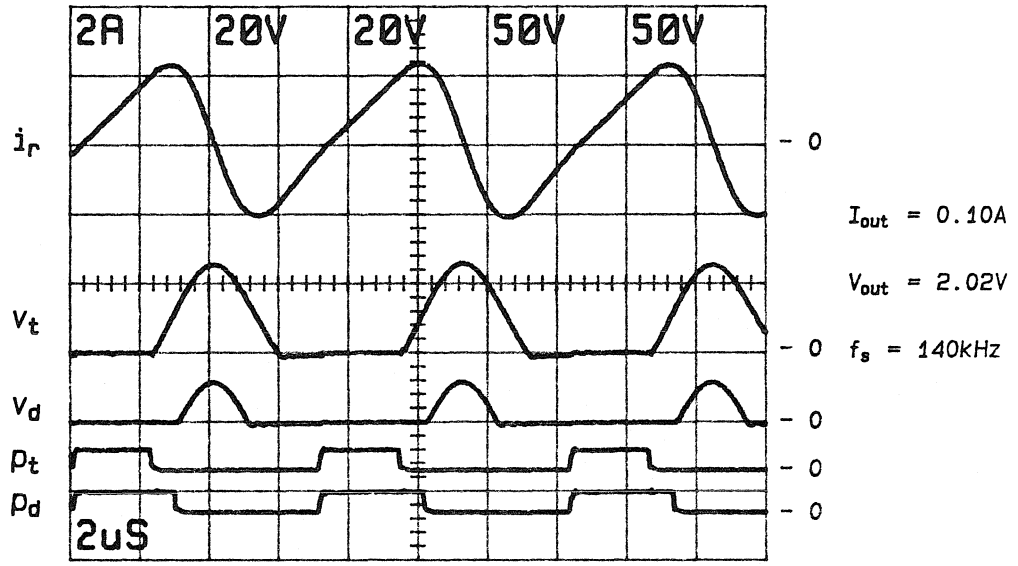


Figure 10.21: Waveforms in the experimental ZV-MR buck converter operating in mode III_2.

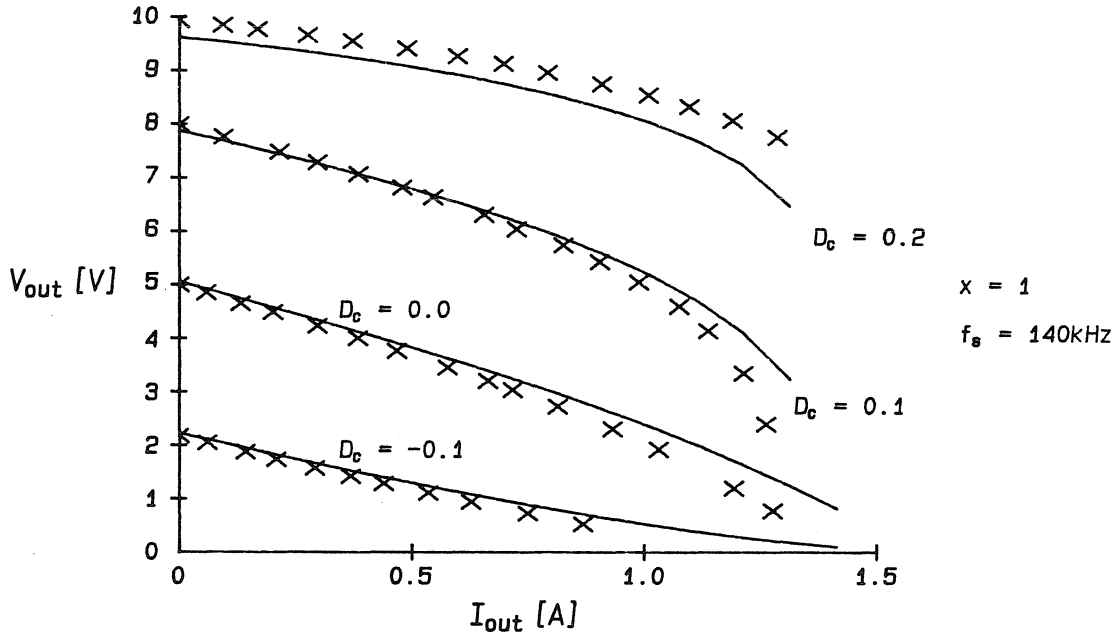


Figure 10.22: Measured and predicted DC characteristics for the ZV-MR buck converter operating in modes $(I, II, III)_2$.

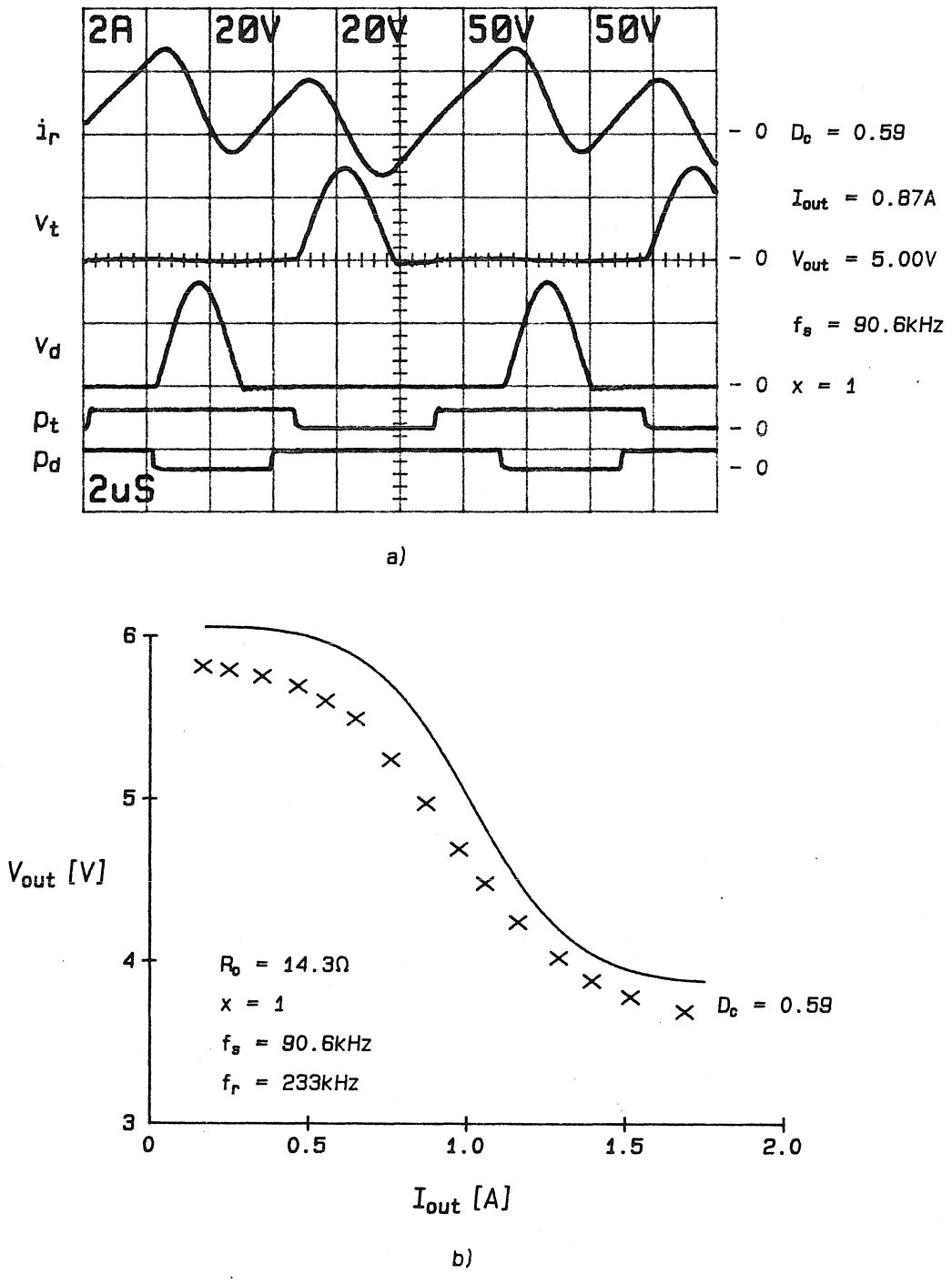


Figure 10.23: Recorded waveforms (a) and measured and predicted DC characteristics (b) for the experimental ZV-MR buck converter operating in mode IV_2.

Chapter 11

A Comparison of Quasi-Resonant Converters

Existence of numerous QR converters generated by the synthesis method of Chapter 6 poses a problem of how to select and design the most appropriate topology with respect to a given set of requirements. The problem is augmented by the fact that for each QR topology there are many operating modes with substantially different DC characteristics, possible control strategies, stresses on switching devices, dynamic responses, etc. Without attempting to encompass all relevant issues, this chapter is aimed toward a better understanding of trade-offs encountered in comparison and design of QR converters.

A qualitative comparison of QR topologies with respect to switching losses is presented in Section 11.1. Only one of the QR classes, namely, ZV-MR, provides, at least ideally, elimination of all major loss mechanisms that plague PWM converters. Other QR topologies offer partial reduction of switching losses.

In Section 11.2 we turn to the design of QR converters, i.e., to the problem of how to select the values of resonant elements. Based on results from Chapters 7 through 10, we consider properties of QR converters affected by the choice of resonant elements – available operating region, frequency range and switch stresses. Main practical contributions of this section are analytical and numerical results as well as guidelines that could be used by a prospective designer to compare various topologies, select and finally design the one best suited for a given application. A simple design example is used to illustrate implementation of the analysis results in comparison of various QR topologies.

11.1 Switching Losses

A qualitative comparison of QR topologies with respect to switching losses is summarized in Table 11.1. Entries zv and zc denote switching transitions at zero voltage and

QR Topology	Switching Transition				Topology Insensitive to:		
	S-switch		$\hat{S}$-switch				
	ON→OFF	OFF→ON	ON→OFF	OFF→ON	L_p	C_t	C_d
Q_n-PWM	zc	zv	zv	zc	–	–	–
Q_f-PWM	zc	zv	zv	zc	–	–	–
ZV	zv	zv	zc	zc	√	√	–
ZC	zc	zc	zv	zv	√	–	√
ZV-QSW	zv	zv	zv	zv	–	√	√
ZC-QSW	zc	zc	zc	zc	√	–	–
ZV-MR	zv	zv	zv	zv	√	√	√
ZC-MR	zc	zc	zc	zc	√	–	–

Table 11.1: Comparison of QR converters with respect to type of switching transitions and sensitivity to major parasitic elements.

zero current, respectively. All QR classes studied in Chapters 7 through 10 together with dual classes are included in the comparison. By the duality principle applied to switching transitions, one can conclude that if a switch turns ON at zero voltage in a converter, the same switch turns OFF at zero current in a dual converter. Thus, transitions for converters in Q_n-PWM and Q_f-PWM classes are identical, while the S-switch and the $\hat{S}$-switch have interchanged types of transitions in ZV and ZC classes. Finally, ZV-QSW and ZC-QSW and likewise ZV-MR and ZC-MR have complementary sets of transitions.

Table 11.1 also summarizes sensitivity of QR topologies to major circuit parasitic reactances that cause a substantial part of switching losses in a PWM converter: the S-switch junction capacitance C_t, the $\hat{S}$-switch junction capacitance C_d and the parasitic inductance L_p distributed in the loop with the switches. A topology is insensitive to a parasitic element if the position of the element agrees with the position of the like resonant element. If a topology is insensitive to a parasitic element, switching loss mechanisms associated with the element are effectively eliminated. The parasitic element can be absorbed by the resonant element or even used alone as the resonant element.

If a switch undergoes a transition at zero current but at non-zero voltage, the topology is necessarily sensitive to the parasitic junction capacitance of the switch, since the energy

stored in the capacitance is lost in every switching cycle. Therefore, transitions at zero current are less favorable than transitions at zero voltage.

With respect to transitions and sensitivity to parasitics, ZV-MR topologies are clearly superior to other QR converters. ZV-QSW topologies also exhibit all zero-voltage transitions, but switching losses associated with the parasitic inductance L_p in the loop with the switches are not eliminated. In converters with an isolation transformer, leakage inductance of the transformer appears in the position of L_p so that the ZV-QSW class and other classes sensitive to L_p may be suitable for very high-frequency operation only in applications where a transformer is not utilized.

11.2 Operation Region, Frequency Range and Switch Stresses

The most widespread application of DC-to-DC converters is in DC voltage regulators. Typical design specifications for a voltage regulator include the output voltage, the range of input voltages and the range of output currents. In the normalized load-to-output plane, these specifications can be translated into

$$m^*_{min} \leq m \leq m^*_{max} \tag{11.1}$$

and

$$\frac{\delta_{max}}{\delta_{min}} = \gamma^* , \tag{11.2}$$

where m^*_{min} (m^*_{max}) is the required equivalent duty ratio for maximum (minimum) input voltage and minimum (maximum) load, while γ^* is the required load range.

Since the choice of the absolute switching frequency f_s is not related to the selection of resonant components, we may assume that f_s is also given. For the design of frequency-controlled converters, we assume that the maximum switching frequency is given.

The first design consideration is that the *required* operating region, defined by conditions (11.1) and (11.2), must fit into the *available* operating region for the selected QR class and operating mode.

Since in the load direction only the load range γ^* is specified, the position of the required region within the available region may not be unique. In particular, if the

available operating region includes the zero-load axis, δ_{max} can be chosen arbitrarily as long as it is within boundaries of the available region.

The design problem of selecting values for resonant elements is equivalent to the problem of selecting or computing parameters f and δ_{max}. An exception is the class of ZV-MR converters where there are two resonant capacitors, so that an additional parameter is the ratio x of the capacitor values. Once the parameters f and δ_{max} are determined, values of the resonant elements are given by

$$C_r = \frac{f}{2\pi f_s} \frac{(I_{out})_{max}}{(V_g)_{min}} \frac{1}{\delta_{max}}, \tag{11.3}$$

$$L_r = \frac{f}{2\pi f_s} \frac{(V_g)_{min}}{(I_{out})_{max}} \delta_{max}. \tag{11.4}$$

Here, it is understood that the normalized frequency f and the absolute frequency f_s correspond to each other. If the converter is controlled by varying the switching frequency, the maximum value for f_s is usually specified, so that the maximum value for f should be determined and used to compute C_r and L_r.

Although importance of different criteria for selection of design parameters may depend on the particular application, in general, minimum switch voltage/current stresses and minimum frequency range are of major concern. Voltage and current stresses dictate the choice of semiconductor components with obvious implications with respect to cost and availability. A large frequency range for frequency-controlled converters is undesirable primarily because of difficulties in handling the generated noise and because of the problems related to filtering the variable-frequency ripple.

Voltage stress (V_{peak}) is defined as the maximum of the peak instantaneous switch voltage over all operating points in the operating region. Voltage stress is normalized to V_{off}, which is ideally equal to the voltage stress in the PWM parent converter. Thus, not only a common ground is established for comparison of QR converters but also, the comparison is made with respect to the parent PWM converter. It is important to note that the comparison does not depend on what particular PWM parent topology is used, as long as it is the same for all QR converters under consideration. The same conclusions extend to the comparison of current stresses if the maximum peak current I_{peak} is re-normalized to the maximum load δ_{max}. Again, current stress I_{peak}/δ_{max} can be compared

directly to the current stress of the PWM parent converter, where it is ideally equal to one. Current stress is important not only for the proper choice of switching devices but also as an indication of the amount of conduction losses in the converter circuit.

In succeeding sections, various design trade-offs involving the operating region, switch stresses and/or frequency range are discussed and compared for QR classes and operating modes of Chapters 7 through 10.

A Design Example

For various QR topologies and operating modes, design trade-offs are illustrated using the same design example in each case. Assume that the specified output voltage, input voltage range and load range result in the requirements

$$m^*_{min} = 0.4, \tag{11.5}$$

$$m^*_{max} = 0.6, \tag{11.6}$$

$$\gamma^* = 5. \tag{11.7}$$

The first design concern is to select parameters so that the required operating region fits into the available operating region. Then, in order to equalize conditions for comparison, the remaining free parameters are selected so that the stress product $(V \times I)$, defined by

$$(V \times I) \equiv V_{peak} \frac{I_{peak}}{\delta_{max}}, \tag{11.8}$$

is minimized whenever possible. Results of the comparison are summarized in Table 11.4, at the end of this section.

11.2.1 Q_n-PWM Converters: Mode I_1

Operating Region

Q_n-PWM converters have the most restricted available operating region among all studied QR topologies. If the load range is critical, the best possible design approach is to choose the normalized frequency f so that the load range is maximized for $m = m^*_{max}$. This frequency,

$$f = f_\delta(m^*_{max}), \tag{11.9}$$

f	V_{tpeak}	I_{tpeak}/δ_{max}	V_{dpeak}	I_{dpeak}/δ_{max}
0.2	8.3	2.0	8.5	2.0
0.4	5.1	1.9	5.3	1.9
0.6	3.6	1.9	3.9	1.9
0.8	2.6	1.8	3.0	1.8
1.0	1.9	1.8	2.4	1.7

Table 11.2: Switch voltage and current stresses in a Q_n-PWM converter operating in mode I_1.

can be found from plots in Fig. 7.4.

Switch Voltage and Current Stresses

For a given frequency f, switch stresses are found at the operating point corresponding to the maximum normalized load δ (at the right-hand corner of the available operating region). Values found numerically for several normalized frequencies are shown in Table 11.2. Voltage stresses increase rapidly with decreasing frequency f. Taking into account the positions of the available operating regions, this implies that Q_n-PWM converters are not practical for applications where low equivalent duty ratios are required.

Design example: the maximum possible load range for $m = m^*_{max} = 0.6$, corresponding frequency $f_\delta(0.6)$ and δ_{max} can be found from plots in Fig. 7.4. At $m = 0.6$, the available load range is approximately equal to the required range $\gamma^* = 5$. However, for lower m, the available range diminishes, and at $m = 0.4$ it is only 2.5. Voltage and current stresses displayed in Table 11.4 are found numerically for $\delta = \delta_{max}$.

11.2.2 ZV Converters: Mode I_1

Operating Region

The minimum normalized load for ZV converters operating in mode I_1 is equal to 1.

Switch Voltage and Current Stresses

The S-switch peak current is equal to δ_{max}, so that its current stress is equal to 1, just as in PWM converters. The diode current stress is equal to 2. This can be easily inferred from the solution for current i_d in the OFF-ON state. The diode voltage stress is ideally equal to 1. However, the S-switch voltage stress, reached in the OFF-ON state for a maximum load, amounts to

$$V_{tpeak} = 1 + \delta_{max} . \tag{11.10}$$

Frequency Range

The required frequency range can be computed from the analytical expression found for the equivalent duty ratio ($m = 1 - G_1(\delta)f$). Minimum frequency corresponds to the maximum load and maximum m, while maximum frequency corresponds to the minimum load and minimum m. Thus, the frequency range is given by

$$\frac{f_{max}}{f_{min}} = \frac{1 - m^*_{min}}{G_1^{-1}(1)} \frac{G_1^{-1}(\gamma^*)}{1 - m^*_{max}} . \tag{11.11}$$

Design Considerations

Since $\delta_{min} \geq 1$ and since both the S-switch voltage stress and the frequency range increase with δ_{max}, design of ZV converters in mode I_1 reduces to

$$\delta_{max} = \gamma^* . \tag{11.12}$$

Design example: maximum load is $\delta_{max} = 5$ and all entries in Table 11.4 follow from the results of this section.

11.2.3 ZV Converters: Mode II_2

Operating Region

From the results of Section 8.4, the required operating region can be encircled by the available operating region if f and δ_{max} are chosen such that

$$1 - fG_3'(\delta_{max}) = m^*_{max} , \tag{11.13}$$

$$1 - fG_3'(\max(\delta + \theta_c)) = m^*_{min} . \tag{11.14}$$

Switch Voltage and Current Stresses

From the conditions stated above, voltage and current stresses can be computed for the required operating region. From the solution for the state trajectories in the OFF-ON state, one can determine the transistor peak voltage. Then, the S-switch voltage stress is found at the operating point with minimum m and maximum value of the sum $\delta + \theta_c$,

$$V_{tpeak} = 1 + \sqrt{1 + \left[G_3'^{-1}\left(\frac{1 - m^*_{min}}{f}\right)\right]^2}. \tag{11.15}$$

As in mode I_1, the $\hat{S}$-switch voltage stress is ideally equal to 1.

Peak current for the S-switch is attained in the ON-ON state, while peak current for the $\hat{S}$-switch is attained in the OFF-ON state. Both switches experience current stresses for maximum load and minimum equivalent duty ratio. It follows that

$$\frac{I_{tpeak}}{\delta_{max}} = \frac{G_3'^{-1}\left(\frac{1-m^*_{min}}{f}\right)}{G_3'^{-1}\left(\frac{1-m^*_{max}}{f}\right)}, \tag{11.16}$$

and

$$\frac{I_{dpeak}}{\delta_{max}} = 1 + \frac{\sqrt{1 + \left[G_3'^{-1}\left(\frac{1-m^*_{min}}{f}\right)\right]^2}}{G_3'^{-1}\left(\frac{1-m^*_{max}}{f}\right)}. \tag{11.17}$$

Design Considerations

Except for the constraint

$$f < 1 - m^*_{max}, \tag{11.18}$$

normalized switching frequency is a free parameter. The minimum possible S-switch voltage stress is obtained for $f \to 1 - m^*_{max}$. However, current stresses become infinitely large as f approaches the limit. If, on the other hand, $f \to 0$, current stresses tend to lower limits, but the S-switch voltage stress blows up. Thus, within the limits, it is possible to make a trade-off between voltage and current stresses by varying parameter f.

Design example: Using expressions found for switch stresses, switching frequency f is determined so that $V_{tpeak} I_{tpeak}/\delta_{max}$ is minimized. The inverse of $G_3'(\cdot)$ is computed numerically. The results are displayed in Table 11.4.

11.2.4 ZV-QSW Converters: Mode I_1

Operating Region

The available operating region in mode I_1 is unlimited in the load direction and it includes the zero-load axis. Therefore, for a given load range, δ_{max} can be treated as a free parameter. In the m direction, however, the operating region is limited to equivalent duty ratios $0.5 \leq m < 1$.

Switch Voltage and Current Stresses

With respect to voltage stresses, ZV-QSW converters are unique among QR topologies. As in ideal PWM converters, voltage stress is equal to 1 for both switches and for all operating points in the available operating region.

The S-switch peak current is equal to the current $i_{on} = i_2$ at the transition from the ON-ON to the OFF-ON state. If a lower bound is imposed on normalized frequency f, current stresses for the S-switch and the diode occur at the operating point where $f = f_{min}$, $m = 0.5$ and $\delta = \delta_{max}$. From DC analysis equations of Section 9.3, it follows that the S-switch current stress is given by

$$\frac{I_{tpeak}}{\delta_{max}} = 1 + \sqrt{1 + \frac{3\pi}{4\delta_{max}}}, \tag{11.19}$$

where δ_{max} is related to the minimum switching frequency through

$$f_{min} = \frac{\pi}{\frac{3\pi}{4} + 2\delta_{max}\left[1 + \sqrt{1 + \frac{3\pi}{4\delta_{max}}}\right]}. \tag{11.20}$$

It can be inferred that current stress decreases with increasing δ_{max} or, equivalently, with decreasing the lower bound on f.

The diode peak current is given by

$$I_{dpeak} = \sqrt{1 - 2m + I_{tpeak}^2}. \tag{11.21}$$

The diode current stress is the same as the S-switch current stress, and it occurs at the same operating point.

Frequency Range

Minimum (maximum) frequency is attained at the operating point with maximum (minimum) m and maximum (minimum) load. The required frequency range can be depicted directly from the load-to-output characteristics or computed numerically from

$$\frac{f_{max}}{f_{min}} = \frac{f(\delta_{min}, m^*_{min})}{f(\delta_{max}, m^*_{max})}. \tag{11.22}$$

It increases with increasing δ_{max} or, equivalently, with decreasing the lower limit on f.

Design Considerations

For a given load range and limits on conversion ratio, the design parameter δ_{max} can be varied to reach a favorable trade-off between current stresses and the frequency range. It should be noted that increasing δ_{max} results not only in an increased frequency range, but also in relatively shorter OFF-OFF states which, in turn, may diminish the benefits of zero-voltage switching if duration of the transition states become comparable to switching times of employed switching devices.

Design example: Since optimization of the stress product would lead to an infinitely large frequency range and PWM-like transitions, instead, δ_{max} is selected with respect to the current stress vs frequency-range trade-off. Since operation below $m = 0.5$ is not possible, parameters in Table 11.4 are computed for $m^*_{min} = 0.5$ and $m^*_{max} = 0.7$.

11.2.5 ZV-QSW Converters: Mode I_2

Operating Region

In mode I_2, the operating region is a bounded portion of the load-to-output plane, symmetrical around $m = 0.5$. The maximum possible load δ_{max} corresponds to $m = 0.5$ and can be found from Eq. (11.20) with f_{min} replaced by the selected frequency f. However, assuming that limits on the conversion ratio are given, intersections of $m = m^*_{max}$ and $m = m^*_{min}$ with boundary curves of the operating region determine the actual maximum possible load, lower than δ_{max}.

Switch Voltage and Current Stresses

As in mode I_1, voltage stress is equal to 1 for both switches. The S-switch current stress is attained at the upper-right corner of the required operating region, for maximum load and maximum m. Similarly, the $\hat{S}$-switch current stress is attained at the lower-right corner, for maximum load and minimum m. Upper bounds for stresses can be found from Eqs. (11.19) through (11.21) by replacing f_{min} with f.

Design Considerations

As in mode I_1, current stresses are lower for higher δ_{max} or, equivalently, for lower f. Once f is chosen, a corner point of the required operating region,

$$(\delta_{max}, m^*_{min}) \text{ or } (\delta_{max}, m^*_{max}), \tag{11.23}$$

has to be placed on the boundary curve of the available operating region in order to minimize the current stresses. Since the absolute switching frequency is given, the only relevant trade-off is between too short transition times and too high current stresses. Lower f contributes to lower current stresses but possibly higher switching losses as transitions get shorter. Both conclusions are in agreement with the notion that, as frequency f is decreasing, mode I_2 approaches the ideal continuous conduction mode of the PWM parent converter.

Design example: Normally, the choice of f would depend on the speed of utilized devices and the desired absolute frequency f_s. Since no specific assumptions were made, the design example is used to illustrate how stresses in mode I_2 can be quite comparable to stresses in mode I_1. Selected frequency f is between the limiting values determined for mode I_1.

11.2.6 ZV-MR Converters: Modes I_1 and II_1

Operating Region

The available operating region for ZV-MR converters in modes $(I, II)_1$ depends only on parameter x. For $x = 1$, the region splits into two regions, one for $m > 0.5$ and $\delta < 1$

and the other for $m < 0.5$ and $\delta > 1$. By increasing x, the operating region expands, as illustrated in Fig. 10.6.

Switch Voltage and Current Stresses

In order to find voltage and current stresses for switching devices, we assume that $\delta = \delta_{max} = const.$ and seek the maximum of the peak voltage or current as frequency is varied.

The S-switch voltage, v_t, assumes its peak value in the OFF-OFF state of mode I_1. Since current i_r is equal to the derivative of v_t in this state, time θ, for which peak voltage is attained, can be found as a minimum positive solution of $i_r(\theta) = 0$. Then, equations for the OFF-OFF and the preceding ON-OFF state are solved for the peak S-switch voltage as a function of θ_2, which is the duration of the ON-OFF state. An exact analytical solution can be found for the maximum of the peak S-switch voltage. The solution yields the S-switch voltage stress as a function of maximum load δ_{max} and parameter x,

$$V_{tpeak} = \sqrt{x} + \frac{\delta_{max}}{1+x}\left[\pi - \arctan\sqrt{x^2-1} + \sqrt{x(x-1)}\right] = \sqrt{x} + \mu(x)\delta_{max}\,. \qquad (11.24)$$

Function $\mu(x)$ is equal to $\pi/2$ at $x = 1$ and decays rapidly toward 1 with increasing x. If $\mu(x) \approx 1$ is taken, the error in calculated V_{tpeak} is less than 10% for $x \geq 2$ and $0 < \delta < 3$, or for $x \geq 3$ and all $\delta > 0$. Since for $x < 2$ the available operating region becomes fairly restricted, a simple expression,

$$V_{tpeak} \approx \sqrt{x} + \delta_{max}\,, \qquad (11.25)$$

can be taken in most practical designs.

The diode voltage stress,

$$V_{dpeak} = 2\,, \qquad (11.26)$$

can be found by inspection of the solutions for the state trajectories in the ON-OFF state.

The S-switch current stress,

$$\frac{I_{tpeak}}{\delta_{max}} = 1 + \frac{\sqrt{x}}{\delta_{max}}\,, \qquad (11.27)$$

is found at the operating point for which current i_r at the end of the ON-OFF state attains its maximum value.

The diode current stress occurs in the OFF-ON state, in mode I_1. Assuming that the S-switch peak voltage occurs at the same time as the OFF-OFF to OFF-ON transition and by taking V_{tpeak} as the maximum possible S-switch voltage, an approximation for the diode current stress is determined:

$$\frac{I_{dpeak}}{\delta_{max}} \approx 2 + \frac{\sqrt{x} - 1}{\delta_{max}}. \tag{11.28}$$

Within practically negligible errors, the result for the diode current stress is in agreement with results obtained numerically from DC analysis equations.

Frequency Range

Maximum frequency (at minimum load and minimum m) and minimum frequency (at maximum load and maximum m) can be computed numerically from DC analysis equations or, better, inferred directly from the load-to-output DC characteristics.

Design Considerations

All peak voltage and current stresses (except V_{dpeak}, which is constant) increase with parameter x. On the other hand, the operating region expands with x. Therefore, minimum x for which required operating region can be fully encompassed by the available operating region should be selected in the design.

Since the zero-load axis is included in the available region (except if conversion ratios less than $m_{min}(\delta = 0)$ are required), δ_{max} is a free parameter. Value of the parameter δ_{max} affects trade-offs among the voltage stresses, the current stresses and the frequency range. Higher δ_{max} results in lower current stresses but in higher voltage stresses. For a given load range γ^*, the frequency range increases with δ_{max}, as is evident from the load-to-output DC characteristics for frequency-controlled ZV-MR converters.

Design example: parameter x is set to 2. From Eqs. (11.25) and (11.27), it can be shown that $\delta_{max} = \sqrt{x}$ minimizes the S-switch stress product $V_{tpeak} I_{tpeak} / \delta_{max}$. Only the S-switch (transistor) stresses are taken into account since $V_{dpeak} = const.$, and the diode peak current is usually of less concern than the transistor peak current. All values in Table 11.4 are computed using the results of this section except that the exact frequency range is found numerically. It should be noted that the available operating region exceeds

the required operating region. Stresses computed for the available operating region can be regarded as upper bounds for stresses in the required operating region.

11.2.7 ZV-MR Converters: Modes $(I, II, III)_2$

Operating Region

For loads up to some maximum value $\delta_{max}(f)$, the available operating region covers all possible equivalent duty ratios provided that

$$f < \min(1, \frac{1}{\sqrt{x}}) . \tag{11.29}$$

The maximum load $\delta_{max}(f)$ increases with decreasing f while for f increasing above 1, the operating region diminishes quickly. For x decreasing below $x = 1$, only a modest expansion of the operating region is obtained with a penalty of increased voltage stress on the $\hat{S}$-switch. One can also note that in a transformerless ZV-MR converter, $x = 1$ is the most convenient choice since identical transistors (with presumably equal parasitic capacitances) can be used for both switches. Henceforth, it is assumed that $x = 1$.

Switch Voltage and Current Stresses

For $x = 1$, voltage and current stresses for switches S and $\hat{S}$ are the same although they do not occur at the same operating point. The fact that both switches have the same stresses for $x = 1$ follows intuitively from symmetry of switches in a ZV-MR converter circuit or from symmetry of state equations and solutions for the switch voltages v_t and v_d. Thus, assuming that $x = 1$, we can consider only one switch. An analogous analysis of stresses for the other switch would lead to the same results.

A plausible assumption for estimation of the S-switch voltage stress is that maximum of the average (DC) voltage and maximum of the peak voltage occur simultaneously (at the same operating point). In a loop consisting of L_r, two switches and V_{off}, the S-switch supports the maximum possible DC voltage (equal to V_{off}) for $m = 0$. The peak voltage calculated under this condition can be taken as an approximation for the S-switch voltage stress. For $m = 0$, duration of the ON-ON state must satisfy

$$\theta_1 = 2\pi \left(\frac{1}{f} - 1 \right) + 2 \arctan \frac{\theta_1}{2} . \tag{11.30}$$

f	$V_{tpeak}(m=0)$	V_{tpeak}	δ_{max}	$\frac{I_{tpeak}}{\delta_{max}}$
0.6	4.5	4.5	2.9	1.6
0.7	3.7	3.8	2.2	1.7
0.8	3.1	3.2	1.7	1.9
0.9	2.6	2.7	1.3	2.1
1.0	2.0	2.3	1.0	2.4

Table 11.3: Switch voltage and current stresses in a ZV-MR converter operating in modes $(I, II, III)_2$ *for* $x = 1$.

For any $f < 1$, a solution for θ_1 can be obtained by simple iteration of Eq. (11.30). Then, peak voltage,

$$V_{tpeak}(m=0) = 1 + \sqrt{1 + \left(\frac{\theta_1}{2}\right)^2}, \tag{11.31}$$

is taken as an estimate for the voltage stress V_{tpeak}. The exact values for the S-switch voltage stress are computed numerically for various frequencies f. Surprisingly, it is found that the S-switch voltage stress occurs always for *zero load* and close to, but not exactly at, $m = 0$. Nevertheless, discrepancies between the estimate $V_{tpeak}(m=0)$ and the numerically computed values are marginal (except for f close to 1), and entirely negligible for $f < 0.7$. For $f \geq 0.6$, comparison of $V_{tpeak}(m=0)$ with numerically computed results is shown in Table 11.3, together with numerically computed values for the maximum load $\delta_{max}(f)$ and the S-switch current stress.

Design Considerations

Voltage stress decreases, while current stress increases with increasing frequency f. The full range of equivalent duty ratios ($0 < m < 1$) can be obtained if $f < 1$.

Design example: Parameter x is set to 1. From results in Table 11.3, a minimum stress product is obtained for $f = 1$. However, since for $f > 1$ the available operating region collapses, $f = 0.9$ is chosen to provide a safety margin with respect to component tolerances. Since the available operating region exceeds the required operating region, stresses displayed in Table 11.4 are upper bounds for stresses in the required operating region.

11.2.8 ZV-MR Converters: Mode IV_2

Operating Region

For ZV-MR converters operating in mode IV_2, limits for the equivalent duty ratio are

$$m_{min}(x,f) = \sqrt{x}f\,, \tag{11.32}$$

$$m_{max}(x,f) = 1-f\,. \tag{11.33}$$

The available load range is from zero to some maximum load $\delta_{max}(x,f,m)$. Of practical interest is the maximum load for which the limits m_{min} and m_{max} are attainable. Thus, we can take

$$\delta_{max}(x,f) = \min(\delta_1\ \delta_2)\,, \tag{11.34}$$

where δ_1 and δ_2 are found from Eqs. (10.79) and (10.81), respectively.

Switch Voltage and Current Stresses

In the operating region for mode IV_2, the S-switch voltage stress is attained for $m = m_{min}$ and maximum load, while the $\hat{S}$-switch voltage stress is found at the operating point where $m = m_{max}$ and $\delta = \delta_{max}$. Voltage stresses are given by

$$V_{tpeak} = 1+\sqrt{1+\delta_{max}^2}\,, \tag{11.35}$$

$$V_{dpeak} = 1+\sqrt{1+\frac{\delta_{max}^2}{x}}\,. \tag{11.36}$$

Switch current stresses,

$$\frac{I_{tpeak}}{\delta_{max}} = 1+\frac{\sqrt{\delta_{max}^2+x}}{\delta_{max}}\,, \tag{11.37}$$

$$\frac{I_{dpeak}}{\delta_{max}} = 1+\frac{\sqrt{\delta_{max}^2+1}}{\delta_{max}}\,, \tag{11.38}$$

are found from solutions for the state trajectories in the ON-OFF state (for the S-switch) and in the OFF-ON state (for the $\hat{S}$-switch), at the operating point where $m = m_{max}$ and $\delta = \delta_{max}$.

Design Considerations

Parameters f and x can be chosen to fit the required operating region into the available operating region in mode IV_2. By lowering the normalized switching frequency, the available operating region extends in both m and δ directions. However, voltage stresses increase accordingly. Parameter x can be lowered to decrease the lower limit on m. However, the $\hat{S}$-switch voltage stress increases at the same time. Lowest current stresses are achieved if the available operating region matches the required region as closely as possible.

Design example: Parameters f and x are set to 0.4 and 1, respectively, in order to enclose but not exceed the required operating region. Then, $\delta_{max} = \delta_1 = \delta_2$ is calculated from Eq. (10.79), and stresses in Table 11.4 follow from the results of this section.

11.2.9 Converters with a Single Controllable Switch Versus Converters with Two Controllable Switches

Introduction of QR converters with two controllable switches is motivated by the possibility of constant-frequency control. Increased complexity of the converter circuit is an evident disadvantage. At this point, it is appropriate to note that the idea of using controllable switches as rectifiers is not new. However, it was proposed in a completely different context. The technique of *synchronous rectification* in PWM converters is offered as a means of reducing conduction losses on rectifiers [34,35]. The concept is becoming more viable with the introduction of MOS switching transistors with extremely low ON-resistance. Conduction losses on rectifier diodes are particularly detrimental in low-voltage ($V_{out} = 5V$) power supplies for digital electronics. Since standards requiring even lower voltages are being introduced, the efficiency of switching power supplies can be maintained only if lower-voltage-drop rectifiers are used instead of currently available diodes. Thus, if increased complexity is justified by possible reduction in conduction losses, the advantage of operating QR converters at a fixed frequency can be regarded as an important additional benefit.

As shown in Table 11.4, where switch stresses are computed for one particular design example, a converter with two controllable switches may exhibit higher voltage and/or

#	Topology	Mode	Parameters
1	PWM	CCM	–
2	Q_n-PWM	I_1	$f = 0.68$, $\delta_{max} = 2.3$
3	ZV	I_1	$f_{max} = 0.61$, $\delta_{max} = 5.0$
4	ZV	II_2	$f = 0.32$, $\delta_{max} = 1.9$
5	ZV-QSW	I_1	$f_{max} = 0.7$, $\delta_{max} = 1.8$
6	ZV-QSW	I_2	$f = 0.33$, $\delta_{max} = 1.5$
7	ZV-MR	$(I, II)_1$	$f_{max} = 1.00$, $\delta_{max} = 1.4$
8	ZV-MR	$(I, II, III)_2$	$f = 0.90$, $\delta_{max} = 1.3$
9	ZV-MR	IV_2	$f = 0.40$, $\delta_{max} = 2.8$

#	V_{tpeak}	$\frac{I_{tpeak}}{\delta_{max}}$	$(V \times I)_t$	V_{dpeak}	$\frac{I_{dpeak}}{\delta_{max}}$	$(V \times I)_d$	$\frac{f_{max}}{f_{min}}$
1	1.0	1.0	1.0	1.0	1.0	1.0	1.0
2	3.2	1.8	5.8	3.5	1.8	6.3	1.0
3	6.0	1.0	6.0	1.0	2.0	2.0	3.2
4	5.2	2.2	11.4	1.0	3.3	3.3	1.0
5	1.0	2.5	2.5	1.0	2.4	2.4	2.9
6	1.0	2.5	2.5	1.0	2.5	2.5	1.0
7	2.8	2.0	5.6	2.0	2.3	4.6	1.4
8	2.7	2.1	5.7	2.7	2.1	5.7	1.0
9	4.0	2.1	8.4	4.0	2.1	8.4	1.0

Table 11.4: Design example: a comparison of QR converters.

current stresses. ZV converters operating in mode II_2 and ZV-MR converters in mode IV_2 have substantially higher stresses than their variable-frequency counterparts operating in modes I_1 and $(I, II)_1$, respectively. On the other hand, ZV-QSW converters in modes I_1 and I_2 and likewise ZV-MR converters in modes $(I, II)_1$ and $(I, II, III)_2$ exhibit quite comparable switch stresses. In addition to possible operation at constant switching frequency, ZV-QSW converters in mode I_2 and ZV-MR converters in modes $(I, II, III)_2$ feature significantly extended operating regions in the m direction. Finally, we note that (just as in current-bidirectional PWM converters) operation at zero load and bidirectional power flow are possible in QR topologies with two controllable, current-bidirectional switches.

11.2.10 QR Versus PWM Converters

Compared to PWM converters, all QR topologies exhibit considerably higher voltage or current stresses (or both) with several detrimental consequences. Using the same switching devices, a PWM converter is capable of processing power that is usually an order of magnitude higher than the power that can be processed by a derived QR converter. Conversely, if the same power is processed, switching devices with substantially higher voltage and/or current ratings are necessary in the QR topology. Moreover, higher current stresses indicate that conduction losses are inevitably higher in QR topologies, not only on switches but also on other converter components that carry resonant currents. Since efficiency is of prime concern in power converters, the choice between PWM and QR topologies in a specific application is reduced to a trade-off between conduction losses and voltage stresses on one side and switching losses on the other side. Either experimental comparison (as in [27], for example) or a study based on detailed quantitative estimation of circuit parasitics and power losses [28] has to be made in order to decide whether a PWM or a QR converter topology is better for a given set of design constraints and requirements.

Chapter 12

Conclusions

Synthesis of DC-to-DC converters in the two largest families – PWM and Quasi-Resonant – is undertaken in this thesis. Generation of converter topologies is based on formal definitions of the converter networks and on the recognition of underlying topological properties derived from defining assumptions. Thus, rather then rely on intuition or various circuit manipulation techniques, one is able not only to construct complete classes of converters, but also to examine pertinent properties systematically. Once all possible topologies with features for comparison are exposed, the problem of selecting the one best suited for a given application becomes well defined. Original contributions of the thesis are summarized as follows:

1. General properties of PWM converter networks:

Based on the rigorous definition of PWM converter networks in Chapter 3, several interesting properties of PWM networks are uncovered. The properties interrelate the network complexity and attainable DC conversion ratios. Thus, a PWM (voltage-to-voltage) converter must have an even number of switches (Proposition 3.2) and the same number of inductors and capacitors (Proposition 3.3), if, in addition, there exists a unique solution to DC model equations. The DC conversion ratio $M(D)$ is a ratio of polynomials in duty ratio D. Degree of the polynomials cannot be grater than the number of inductors/capacitors or half the number of switches in the converter network (Proposition 3.4). Both the possibility of coupling inductors and the property of continuous terminal currents imply lower upper bounds on the degree of polynomials in $M(D)$ (Propositions 3.5 and 3.6). The constraints imposed on the PWM networks are used to justify the choices for the number of elements that need to be considered by the synthesis procedure constructed in Chapter 4.

PWM converters with two switches come with a particularly interesting property:

voltage and current stresses on switches are the same for converters that share the same conversion ratio $|M(D)|$. Moreover, the stresses can be found directly from the known denominator of $M(D)$ (Proposition 3.9).

2. Synthesis procedure for generation of complete classes of PWM converters:
The synthesis procedure constructed in Chapter 4 guarantees that *complete* classes of converters that satisfy a set of prescribed requirements are generated. The procedure is developed in detail and is executed via a computer program in order to generate all second-order and fourth-order topologies. The input requirements include the DC conversion ratio, continuous terminal currents, possible coupling of inductors and the number of switches. In particular, the number of switches implemented as transistors can be specified. Outputs of the procedure are complete converter networks that include switches and switch implementations.

3. Generalization of a unified approach to analysis of converters derived from two-switch PWM converters:
An immediate consequence of Proposition 3.9, given by Eq. (3.48), can be used to devise a simple unified analysis method[1] for two-switch, PWM-derived converters. The only prerequisite for application of the method is that the converter under study and a two-switch PWM converter share the same DC network. Generality of the method is fully utilized in the unified DC analysis of PWM converters in discontinuous modes (Section 5.2), and in the unified DC analyses of various classes of Quasi-Resonant converters (Chapters 7 through 11).

4. A systematic approach to synthesis and topological characterization of Quasi-Resonant converters:
Synthesis of Quasi-Resonant converters in Chapter 6 is based on the proper definition which, in this case, simply formalizes the fact that a Quasi-Resonant converter is a two-switch PWM converter with added resonant elements. Thus, topological properties, DC conversion properties and the unifying analysis method are carried over from well-known and well-understood PWM converters into much less comprehended QR arena.

After all possible topological positions are examined, six classes (in dual pairs) of QR

[1]The relation (3.48) was conjectured and the analysis approach was first proposed in [20].

converters with a single resonant capacitor and a single resonant inductor are uncovered, two of which have not been identified before. QR converters with more than two resonant elements can be generated recursively, by adding a resonant element to an existing QR topology.

Most importantly, the synthesis method puts into order and properly defines all known and newly uncovered QR topologies. The topological definitions of QR classes are instrumental for the application of the unifying analysis method.

5. Results of immediate practical interest:

– Novel, single-transistor PWM converters are found with conversion ratios suitable for applications requiring large step-down, large range of input voltages and/or large range of output voltages. In particular, two single-transistor topologies with $M(D) = D^2$ and three with $|M(D)| = D^2/1 - D$ are uncovered.

– PWM converters generated by the synthesis procedure are compared with respect to conduction losses on converter elements. The comparison tables can be utilized in the process of selecting the most appropriate topology for a given application.

– Two new classes (named Quasi-PWM) of QR converters with two resonant elements are uncovered. In Q-PWM converters, transistor turn-ON and diode turn-OFF are at zero current, while transistor turn-OFF and diode turn-ON are at zero voltage. Control at constant switching frequency is possible with a conventional (single-transistor, single-diode) implementation of switches. A major deficiency of Q-PWM converters is that the operating region in the operating mode with all zero-voltage/zero-current transitions is very restricted. Q-PWM converters can also be viewed as PWM converters operating in the discontinuous inductor current mode and the discontinuous capacitor voltage mode simultaneously.

– Converters in all QR classes can be controlled at constant switching frequency if both switches are controllable. For each QR class under study in Chapters 7 through 10, this option is examined in detail. Converters with two controllable, current-bidirectional switches in ZV-QSW and ZV-MR classes are particularly interesting since they exhibit similar switch stresses as their single-transistor counterparts, but in addition to constant-frequency control, they feature significantly extended operating regions in modes with all

zero-voltage transitions. Finally, it should be noted that if the technique of synchronous rectification is used in order to reduce the conduction losses, additional benefits of having a controllable rectifier in a QR converter come virtually without penalty.

– A number of new analytical and numerical results are derived for classes of QR converters and operating modes of most practical interest. The results that can be used for comprehensive comparison, selection and design of QR converters include DC characteristics, boundaries of operating regions, switch stresses and a discussion of pertinent design trade-offs.

Appendix A

2L1C Converter Cells

A 2L1C converter cell is shown in Fig. A.1 as a three-terminal device. DC conversion ratios for six possible input and output terminal designations are listed in Table A.1. All converter cells with a single capacitor, two inductors and four switches are listed in

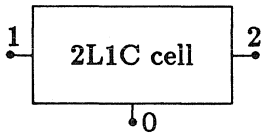


Figure A.1: 2L1C converter cell

input	1 – 0	2 – 0	2 – 1	0 – 1	1 – 2	0 – 2
output	2 – 0	1 – 0	0 – 1	2 – 1	0 – 2	1 – 2
conversion ratio	$M(D)$	$\frac{1}{M(D)}$	$\frac{1}{1-M(D)}$	$1-M(D)$	$\frac{M(D)}{M(D)-1}$	$\frac{M(D)-1}{M(D)}$

Table A.1: DC Conversion ratios for six possible terminal designations of a converter cell

Table A.2. The list is an output of the computer program that implements the synthesis procedure described in Chapter 4. Entries in Table A.2 have the following format:

$$\#\ i_1j_1k_1\text{–}i_2j_2k_2.s\ \ p_2\ p_1\ p_0/\ q_2\ q_1\ q_0\ \ \mathrm{I\ O\ C}\ . \tag{A.1}$$

Assuming that input is between terminals 1 and 0, while output is between terminals 2 and 0, $(i_1j_1k_1, i_2j_2k_2.s)$ is the pair used to represent positions of elements in the cell and

$$M(D) = \frac{P(D)}{Q(D)} = \frac{p_2D^2 + p_1D + p_0}{q_2D^2 + q_1D + q_0} \tag{A.2}$$

is the conversion ratio. Entries I and O denote continuous (c) or pulsating (p) input or output current, while C denotes possible (y) or not possible (n) coupling of inductors.

1	114-142.1	0	0	-1/	-1	2	-1	p	p	n	46	116-152.4	0	-1	0/	-1	1	0	c	c	y
2	114-146.1	0	-1	0/	1	-2	1	p	p	n	47	116-153.4	-1	1	-1/	-1	1	0	p	c	n
3	114-152.3	0	-1	0/	1	-2	1	c	p	n	48	116-153.8	1	-3	1/	1	-1	0	p	c	n
4	114-152.7	0	-1	0/	-1	2	-1	c	p	n	49	116-154.3	-1	0	0/	0	-1	1	c	p	n
5	114-152.8	0	-1	0/	1	-2	1	c	p	n	50	116-154.8	-1	0	0/	0	1	-1	c	p	n
6	114-156.3	-1	0	0/	-1	2	-1	c	p	n	51	116-155.3	0	-2	1/	0	-1	1	p	p	y
7	114-156.4	1	-2	0/	1	-2	1	c	p	n	52	116-156.1	1	-2	0/	1	-1	0	p	c	n
8	114-156.8	-1	0	0/	-1	2	-1	c	p	n	53	116-156.7	1	-2	0/	1	-1	0	c	c	y
9	114-166.1	0	-1	0/	0	-1	1	p	p	y	54	116-243.6	-1	1	-1/	-1	1	0	p	c	n
10	114-252.7	0	0	-1/	-1	2	-1	p	p	n	55	116-243.8	1	-1	-1/	1	-1	0	p	c	n
11	114-253.8	1	-2	0/	1	-2	1	p	p	n	56	116-246.1	0	-2	1/	1	-1	0	p	c	n
12	114-256.8	-1	1	-1/	-1	2	-1	p	p	n	57	116-252.8	0	0	-1/	1	-1	0	p	c	n
13	114-261.7	1	-1	-1/	0	1	-1	p	p	n	58	116-255.8	0	-1	0/	0	1	-1	p	p	y
14	114-342.5	0	0	-1/	1	-1	0	p	p	n	59	116-256.1	1	-3	1/	1	-1	0	p	c	n
15	114-342.7	0	0	-1/	-1	1	0	p	p	n	60	116-256.3	-1	1	-1/	-1	1	0	p	c	n
16	114-344.1	0	-1	0/	0	1	-1	p	p	y	61	116-256.7	1	-1	-1/	1	-1	0	p	c	n
17	114-351.7	1	-3	1/	0	-1	1	p	p	n	62	116-346.1	0	-1	0/	1	0	-1	p	p	n
18	114-353.7	-1	1	-1/	-1	1	0	p	p	n	63	116-356.3	-1	0	0/	-1	0	1	c	p	n
19	114-354.3	-1	0	0/	0	-1	1	c	p	n	64	116-356.7	1	-2	0/	1	-2	1	c	p	n
20	114-354.7	1	-2	0/	0	-1	1	c	p	n	65	116-356.8	-1	0	0/	-1	2	-1	c	p	n
21	114-354.8	-1	0	0/	0	-1	1	c	p	n	66	116-366.1	0	-1	0/	0	1	-1	p	p	y
22	114-355.8	0	-2	1/	0	-1	1	p	p	y	67	134-155.1	0	2	-1/	0	1	0	p	p	y
23	114-364.1	0	-1	0/	-1	2	-1	p	p	n	68	134-156.1	1	0	0/	1	-1	1	c	p	n
24	115-143.1	-1	1	-1/	-1	2	-1	p	p	n	69	134-254.1	1	-1	1/	0	1	0	p	p	n
25	115-146.1	0	-2	1/	1	-2	1	p	p	n	70	134-264.3	0	2	-1/	1	0	0	p	c	n
26	115-146.2	0	0	-1/	-1	2	-1	p	p	n	71	135-144.1	0	0	1/	0	1	0	p	p	y
27	115-152.8	0	-2	1/	1	-2	1	p	p	n	72	135-145.1	-1	2	0/	0	1	0	p	p	n
28	115-153.3	1	-2	0/	1	-2	1	c	p	n	73	135-145.3	1	0	0/	0	1	0	p	p	n
29	115-153.7	-1	0	0/	-1	2	-1	c	p	n	74	135-154.1	1	-1	1/	0	1	0	p	p	n
30	115-156.3	-1	1	-1/	-1	2	-1	p	p	n	75	135-164.3	0	2	-1/	1	0	0	p	c	n
31	115-161.8	-1	1	-1/	0	1	-1	p	p	n	76	135-164.4	0	0	1/	-1	2	0	p	c	n
32	115-165.1	-1	0	0/	-1	1	0	p	p	n	77	135-164.8	0	0	1/	1	0	0	p	c	n
33	115-165.3	1	-2	0/	1	-1	0	p	p	n	78	135-255.1	0	0	1/	0	1	0	p	p	y
34	115-343.5	1	-1	-1/	1	-1	0	p	p	n	79	135-265.3	1	1	-1/	1	0	0	p	c	n
35	115-343.7	-1	1	-1/	-1	1	0	p	p	n	80	135-265.8	1	-1	1/	1	0	0	p	c	n
36	115-345.1	-1	0	0/	0	1	-1	p	p	n	81	135-355.1	0	1	0/	0	2	-1	c	p	y
37	115-346.6	0	0	-1/	1	-1	0	p	p	n	82	135-365.3	1	0	0/	1	-1	1	p	p	n
38	115-351.8	-1	0	0/	0	-1	1	c	p	n	83	135-366.8	0	0	1/	0	1	0	p	p	y
39	115-352.7	0	-2	1/	-1	1	0	p	p	n	84	145-156.1	1	-2	0/	1	-1	0	p	p	n
40	115-356.8	-1	-1	1/	-1	1	0	p	p	n	85	145-164.1	0	-1	0/	-1	1	0	p	p	n
41	115-365.1	-1	0	0/	-1	2	-1	p	p	n	86	145-165.3	1	-2	0/	1	-1	0	c	p	n
42	116-143.2	1	-2	0/	1	-1	0	p	c	y	87	145-246.1	0	-1	0/	1	-1	0	p	p	n
43	116-144.1	0	-1	0/	0	1	-1	p	p	y	88	145-265.1	-1	0	0/	-1	1	0	p	p	n
44	116-145.1	-1	1	-1/	0	1	-1	p	p	n	89	156-246.1	0	1	0/	1	0	0	p	c	y
45	116-146.3	0	-1	0/	-1	1	0	p	c	n											

Table A.2: All 2L1C converter cells

Appendix B

DC Analyses of Quasi-Resonant Converters: Numerical Procedures

Numerical procedures used in DC analyses of Quasi-Resonant converters in Chapters 7, 9 and 10 are outlined in this appendix.

In most cases, the problem is reduced to solving an equation of the form $\eta(\xi) = 0$, where $\eta(\xi)$ is a continuous function of ξ, defined on some interval (ξ_a, ξ_b). If there exist ξ' and ξ'' in (ξ_a, ξ_b) such that $\eta(\xi')\eta(\xi'') < 0$, there is at least one $\xi_x \in (\xi', \xi'')$ such that $\eta(\xi_x) = 0$. If ξ_x is unique, it can be found numerically by the bisection method. In each iteration, η is evaluated at $\bar{\xi} = (\xi' + \xi'')/2$, and then ξ' or ξ'' is set to $\bar{\xi}$, depending on the sign of $\eta(\bar{\xi})$. Thus, the interval is halved in each iteration and the procedure is terminated when the desired accuracy is achieved. The bisection method was chosen for its simplicity of implementation and also since computational time was of no concern.

B.1 On-Resonant, Quasi-PWM Converters

Boundary Curves of the Operating Region for Mode I_1

Suppose that normalized switching frequency (f) is given. According to conditions derived in Section 7.2.1, the operating region for mode I_1 is given by

$$m_{f1}(\delta) \leq m \leq m_{f2}(\delta)\,, \tag{B.1}$$

$$\delta_{f1} \leq \delta \leq \delta_{f2}\,. \tag{B.2}$$

Curves m_{f1} and m_{f2} intersect at $\delta = \delta_{f1} \leq 1$ and at $\delta = \delta_{f2} \geq 1$. For $\delta_{f1} = \delta_{f2} = \delta^* = 1$, the operating region for mode I_1 shrinks to a single point. At that point all conditions of Section 7.2.1 become equalities, so that corresponding frequency f^* and the equivalent

duty ratio m^* follow from the results of DC analysis in Section 7.2,

$$f^* = \frac{4\pi}{2+3\pi} \approx 1.1\,, \tag{B.3}$$

$$m^* = \frac{3\pi+1}{3\pi+3} \approx 0.84\,. \tag{B.4}$$

At $\delta = \delta_{f1}$, conditions (7.32) and (7.34) become equalities. Together with results of DC analysis, this implies that δ_{f1} is a solution of

$$\eta_1(\delta) = \pi - \arctan\frac{\sqrt{1-\delta^2}}{\delta^2} + \arctan\frac{\delta}{1-\delta^2} - \theta_p + \frac{1}{\delta} + \frac{\sqrt{1-\delta^2}}{\delta^2} = 0\,. \tag{B.5}$$

$\eta_1(\delta)$ is a monotonously decreasing function of δ. Furthermore, since $\eta_1(\delta \to 0) \to +\infty$ and $\eta_1(1) = 3\pi/2 + 1 - \theta_p < 0$, for $f < f^*$, a unique δ_{f1} can be found by the bisection method.

At $\delta = \delta_{f2}$, conditions (7.33) and (7.35) become equalities. It follows that δ_{f2} is a solution of

$$\eta_2(\delta) = \pi - \arctan\frac{\delta^2-1}{\delta} + \arctan\frac{1}{\delta\sqrt{\delta^2-1}} - \theta_p + \delta + \delta\sqrt{\delta^2-1} = 0\,. \tag{B.6}$$

By comparison of $\eta_1(\delta)$ and $\eta_2(\delta)$, one finds that

$$\delta_{f2} = \frac{1}{\delta_{f1}}\,. \tag{B.7}$$

For $\delta \in (\delta_{f1}, 1)$, $m_{f1}(\delta)$ and $m_{f2}(\delta)$ are found from Eqs. (7.24) and (7.30), using the fact that conditions (7.32) and (7.34), respectively, become equalities. Since it can be shown that $m_{f1}(\delta) = m_{f1}(1/\delta)$ and $m_{f2}(\delta) = m_{f2}(1/\delta)$, boundary curves are computed simultaneously for $\delta \in (1, \delta_{f2})$.

Switching Frequency for Maximum Load Range

For a given normalized frequency, $f < f^*$, the available load range, δ_2/δ_1 varies with m. If $f = const.$, the equivalent duty ratio for which the maximum load range is attained is equal to the minimum of $m_{f2}(\delta)$ over $(\delta_{f1}, \delta_{f2})$. Since $m_{f'1} > m_{f''1}$ for $f' > f''$, the converse is also true; i.e., the frequency f for which $m = \min(m_{f2})$ is the frequency that maximizes the load range for this particular m. Thus, the inverse of the optimum frequency $f_\delta(m)$ is found as the minimum of m_{f2}, while the minimum and maximum

loads are found as intersections of $m_{f1}(\delta)$ with $\min(m_{f2})$. In particular, the minimum load, $\delta_1 < 1$, is found from

$$m_{f1}(\delta) - \min(m_{f2}) = 0\,, \tag{B.8}$$

using the bisection method, while the maximum load, $\delta_2 > 1$, is equal to $1/\delta_1$.

B.2 Zero-Voltage, Quasi-Square-Wave Converters

Variable-Frequency Control: mode I_1

The first step in computation of load-to-output characteristics for $f = const.$ is to determine the maximum equivalent duty ratio, $m_{fmax} = m(\delta = 0)$. θ_2 is set to θ_{2min} and m is varied so that $f(\delta = 0)$ matches f. It is easy to verify that $f(\delta = 0)$ in Eq. (9.24) is a monotone function of m. Furthermore, since $f(\delta = 0) \to 0$ for $m \to 1$ and $f(\delta = 0) = 1$ for $m = 0.5$, equation

$$f(\delta = 0) - f = 0 \tag{B.9}$$

can be solved for m_{fmax} by the bisection method for any given frequency $f \in (0, 1)$. Once m_{fmax} is determined, m is swept from $m_{min} = 0.5$ to m_{fmax}. At each point, θ_2 is adjusted so that the normalized frequency is kept constant. Again, the bisection method is used to solve for θ_2, given m and f.

The starting point for computation of control-to-output characteristics for each $\delta = const.$ is $m = 1$, $f = 0$. Then, m is swept from 1 to 0.5, while at each point δ is regarded as a function of θ_2 and the bisection method is used to find θ_2 that results in the predetermined load current δ. Existence and uniqueness of the solution can be established easily.

Constant-Frequency Control: Mode I_2

Assume that the normalized switching frequency $f = const.$ is given. The upper part (for $m \geq 0.5$) of the maximum-load boundary curve for mode I_2 coincides with the $f = const.$, load-to-output characteristic for mode I_1. The lower part (for $m < 0.5$) is symmetrical around $m = 0.5$.

In order to compute a load-to-output characteristic for a given control D_c, maximum, $m_{max}(D_c)$, and minimum, $m_{min}(D_c)$ are found as points on the boundary curves with $(\theta_1+\theta_2)/\theta_p = D_c$. This is possible if $D_{c1} \leq D_c \leq D_{c2}$, where D_{c1} and D_{c2} are maximum and minimum control duty ratios on boundary curves. Then, $m_{max}(D_c)$, $m_{min}(D_c)$ are found using the bisection method with m as an independent variable along the boundary curves.

Points on load to output characteristic are computed by sweeping m between the limits. At each point, the minimum current, i_2', and the maximum current, i_2'', are found such that all conditions for operation in mode I_2 are satisfied for $i_2' \leq i_2 \leq i_2''$. Denote by $i_{2new}(i_2)$ a function that maps current i_2 from the beginning of a cycle to current i_2 at the end of the cycle. For $i_2 \in (i_2', i_2'')$, the function is well defined by use of DC analysis equations of Section 9.4. Using the bisection method, equation

$$\eta(i_2) = i_{2new}(i_2) - i_2 = 0 \tag{B.10}$$

can be solved for i_2 provided that

$$\eta(i_2')\eta(i_2'') < 0\,. \tag{B.11}$$

Since m is between m_{min} and m_{max}, all points are inside the operating region for mode I_2 and existence of a solution is guaranteed. Uniqueness follows from the fact that $\eta(i_2)$ is a monotone function of i_2. With known initial condition for i_2, a steady-state solution for all states and all θ_i follows directly from the DC analysis equations. Finally, δ is determined from Eq. (9.34).

For a control-to-output characteristic, limits for the equivalent duty ratio, $m_{min}(\delta)$ and $m_{max}(\delta)$, are found at intersections of boundary curves with a $\delta = const.$ line. This is possible if the maximum load for $m = 0.5$ is greater than the given δ. Since $m_{min}(\delta) = 1 - m_{max}(\delta)$, the solution for one intersection is sufficient and it is found using the bisection method.

Points on control-to-output characteristics are computed by sweeping m from the lower to the upper limit and by adjusting D_c so that at each point the resulting load current coincides with given δ. The bisection method is applied with D_c as an independent variable. The upper and lower limit for D_c are determined as control duty ratios

found at limiting points for m. At each value of m and D_c, a steady-state solution is computed as described above in the case of load-to-output characteristics. Existence of the solution is guaranteed by the fact that each point on the curve is in the operating region of mode I_2.

B.3 Zero-Voltage, Multi-Resonant Converters

OFF-OFF State: Numerical Solution

In general, the solution for the OFF-OFF state is the minimum angle variable $\theta^* > 0$ such that either $v_d(\theta^*) = 0$ or $v_t(\theta^*) = 0$, or both. Since $v_d(\theta \to \infty) \to -\infty$, it follows that θ^* always exists. Except for particular values of initial conditions, it is not possible to solve for θ^* analytically. A numerical procedure is described in this section.

Zero crossing of voltage $v(\theta)$ (v_t or v_d) is necessarily between angles θ' and θ''. Here, θ' is equal to zero, or it is a point where $v(\theta)$ attains a local maximum, while θ'' is a point where $v(\theta)$ attains its local minimum. Since $dv_t/d\theta = i_r$ and $dv_d/d\theta = i_r - \delta$, points where extrema are attained can be found as zeros of $i_r(\theta) = 0$ and $i_r(\theta) - \delta = 0$, respectively. From Eq. (10.24), zeros can be found analytically for any set of initial conditions.

Assume that, as explained above, two points closest to zero, θ' and θ'' are identified such that

$$v(\theta')v(\theta'') < 0\,. \tag{B.12}$$

Then, equation $v(\theta) = 0$ can be solved by the bisection method and uniqueness of the solution follows trivially.

It may happen that $v_t(\theta) = 0$ cannot be solved. If this is the case, θ^* is the solution of $v_d(\theta) = 0$. Otherwise, θ^* is assigned to smaller of the two solutions.

Variable-Frequency Control: Modes $(I, II)_1$

Control-to-output DC characteristics for $\delta = const.$ are computed by sweeping θ_2 from θ_{2min} to a maximum value θ_{2max}. Angle θ_{2min} is determined as minimum θ_2 for which all necessary conditions for operation in modes I_1 or II_2 are satisfied. $\theta_2 =$

θ_{2max} corresponds to the minimum frequency $f_{min}(\delta)$ as discussed in the DC analysis of Section 10.3. Both θ_{2max} and θ_{2min} are found by applying the bisection method with a criterion that is not a sign of the function but is a flag that indicates whether or not all operating conditions are satisfied. Maximum frequency, $f_{max}(\delta)$, and minimum frequency $f_{min}(\delta)$, corresponding to $\theta_2 = \theta_{2min}$ and θ_{2max} are tabulated as functions of δ. Moreover, equivalent duty ratios determined at limiting values of θ_2 are used to generate boundary curves $m_{min}(\delta)$ and $m_{max}(\delta)$ shown in Fig. 10.6.

Control-to-output characteristics are computed by sweeping θ_2 between θ_{2min} and θ_{2max} in DC analysis equations.

Computation of load-to-output DC characteristics is more involved since frequency f is a predetermined constant. Intersections of $f = const.$ with tabulated functions $f_{min}(\delta)$ and $f_{max}(\delta)$ yield minimum, $\delta_{min}(f)$, and maximum, $\delta_{max}(f)$, load currents for which operation in modes I_1 or II_1 is possible. If $f_{min}(0) < f$, $\delta_{min}(f) = 0$, unless $f_{max}(0) < f$, so that operation at the given f is not at all possible. At each point $\delta \in (\delta_{min}(f), \delta_{max}(f))$, frequency f is regarded as a function of independent variable θ_2. The bisection method is used to solve for θ_2 that results in a frequency equal to f. Finally, the equivalent duty ratio is calculated using Eq. (10.38) or Eq. (10.39), as appropriate.

Constant-Frequency Control: Modes $(I, II, III)_2$

Steady-State Solution

Suppose that parameters x, f, δ and D_c are given. The problem is to find a steady-state solution for i_r, v_t, v_d, and θ_i. At the end of ON-ON state, the initial conditions for voltages are known: $v_{t1} = 0$, and $v_{d1} = 0$, while $i_{r1} > 0$ can be regarded as an independent variable. DC analysis equations of Section 10.4 can be used to find current i_{r1} at the end of the switching cycle. Denote by $i_{r1new}(i_{r1})$ the function that maps current i_{r1} from the beginning of a cycle to current i_{r1} at the end of the cycle. Function $i_{r1new}(i_{r1})$ is defined on interval (i'_{r1}, i''_{r1}), assuming that necessary conditions for operation in mode I_2, II_2 or III_2 are satisfied for each $i_{r1} \in (i'_{r1}, i''_{r1})$. Equation

$$\eta(i_{r1}) = i_{r1new}(i_{r1}) - i_{r1} = 0 \tag{B.13}$$

can be solved for i_{r1} by the bisection method, if $\eta(i'_{r1})\eta(i''_{r2}) < 0$. Uniqueness of the solution is confirmed for all sets of input parameters used to obtain the boundary curves and DC characteristics of Section 10.4. However, uniqueness of the solution in general is taken without proof. Once a steady-state solution for i_{r1} is found, all other states and the equivalent duty ratio follow from the results of the DC analysis in Section 10.4.

DC Characteristics

Control-to-output DC characteristics are found for given x, f and δ by varying D_c from D_{cmin} to D_{cmax}. For all D_c within the limits, there exists a steady-state solution.

Load-to-output DC characteristics are computed for given x, f and D_c by varying δ from zero to some maximum value δ_{max}, where a steady-state solution ceases to exist. δ_{max} and m computed at $\delta = \delta_{max}$ define points on the boundary curves shown in Fig. 10.9.

Constant-Frequency Control: Mode IV_2

Suppose that x, f, δ and D_c are given, and consider current i_{r4} as an independent variable. Assume that for $i_{r4} \in (i'_{r4}, i''_{r4})$, conditions (10.77) necessary for operation in mode IV_2 are satisfied. Denote by $i_{r4new}(i_{r4})$ the function that maps the current at the beginning of a switching cycle to the current at the end of the switching cycle. It can be verified that $\eta(i_{r4}) = i_{r4new}(i_{r4}) - i_{r4}$, defined for $i'_{r4} \leq i_{r4} \leq i''_{r4}$, is a monotonously decreasing function of i_{r4}. Therefore, assuming that i'_{r4} and i''_{r4} can be found, $\eta(i_{r4}) = 0$ can be solved for i_{r4}, provided that

$$\eta(i'_{r4})\eta(i''_{r4}) < 0\,. \tag{B.14}$$

Once current i_{r4} in steady state is found, all states and the equivalent duty ratio follow from the DC analysis of Section 10.4.4. DC characteristics are computed in the same manner as for modes I_2, II_2 or III_2.

References

[1] D. H. Wolaver, "Fundamental Study of DC to DC Conversion Systems," Ph.D. Thesis, Massachusetts Institute of Technology, 1969.

[2] H. Matsuo and K. Harada, "The Cascade Connection of Switching Regulators," IEEE Trans. on Industry Applications, vol. IA-3, No. 2, March/April 1976.

[3] B. P. Israelsen, J. R. Martin, C. R. Reeve, V. S. Scown, "A 2.5kV High-Reliability TWT Power Supply: Design Techniques for High Efficiency and Low Ripple," IEEE Power Electronics Specialists Conference, 1977 Record, pp. 109-130 (IEEE Publication 77CH1213-8 AES).

[4] R. P. Massey and E. C. Snyder, "High Voltage Single-Ended Dc-Dc Converter," IEEE Power Electronics Specialists Conference, 1977 Record, pp. 156-159 (IEEE Publication 77CH1213-8 AES).

[5] S. Ćuk and R. D. Middlebrook, "A New Optimum Topology Switching DC-to-DC Converter," IEEE Power Electronics Specialists Conference, 1977 Record, pp. 160-179 (IEEE Publication 77CH1213-8 AES).

[6] Slobodan Ćuk and R. W. Erickson, "A Conceptually New High-Frequency Switched-Mode Amplifier Technique Eliminates Current Ripple," Proc. Fifth National Solid-State Power Conversion Conference, pp. G3.1-G3.22, 1978.

[7] R. D. Middlebrook, Slobodan Ćuk, and Bill Behen, "A New Battery Charger/Discharger Converter," IEEE Power Electronics Specialists Conference, 1978 Record, pp. 251-255.

[8] E. E. Landsman, "A Unifying Derivation of Switching Regulator Topologies," IEEE

Power Electronics Specialists Conference, 1979 Record, pp. 239-243 (IEEE Publication 79CH1461-3).

[9] R. P. E. Tymerski and Vatche Vorperian, "Generation, Classification and Analysis of Switched-Mode Dc-to-Dc Converters by the Use of Converter Cells," IEEE International Telecommunications Energy Conference, 1986 Proceedings, pp. 181–195 (IEEE Publication 86CH2328-3).

[10] R. W. Erickson, "Synthesis of Switched-Mode Converters," IEEE Power Electronics Specialists Conference, 1983 Record, pp. 9-22 (IEEE Publication 83CH1977-0).

[11] R. D. Middlebrook, "Transformerless DC-to-DC Converters with Large Conversion Ratios," Proc. IEEE INTELEC Conference, 1984.

[12] K-H. Liu and F. C. Lee, "Resonant Switches—A Unified Approach to Improve Performances of Switching Converters," IEEE International Telecommunications Energy Conference, 1984 Proceedings, pp. 344–351 (IEEE Publication 84-CH-2073-5).

[13] K-H. Liu, R. Oruganti, and F. C. Lee, "Resonant Switches—Topologies and Characteristics," IEEE Power Electronic Specialists Conference, 1985 Record, pp. 106–116 (IEEE Publication 85CH2117-0).

[14] K-H. Liu and F. C. Lee, "Zero-Voltage Switching Technique in Dc/Dc Converters," IEEE Power Electronics Specialists Conference, 1986 Record, pp. 58–70 (IEEE Publication 86CH2310-1).

[15] T. Zeng, D. Y. Chen, and F. C. Lee, "Variations of Quasi-Resonant Dc-Dc Converter Topologies," IEEE Power Electronics Specialists Conference, 1986 Record, pp. 381–392 (IEEE Publication 86CH2310-1).

[16] W. A. Tabisz and F. C. Lee, "Zero-Voltage-Switching Multi-Resonant Techique - A Novel Approach to Improve Performance of High-Frequency Quasi-Resonant Converters," IEEE Power Electronics Specialists Conference, 1988 Record, pp. 9-17.

[17] Khai D. T. Ngo, "Generalization of Resonant Switches and Quasi-Resonant DC-DC Converters," IEEE Power Electronics Specialists Conference, 1987 Record, pp. 395-403.

[18] Vatche Vorperian, "Quasi-Square-Wave Converters: Topologies and Analysis," Virginia Power Electronics Center Conference, 1987 Proceedings, pp. 72-80.

[19] C. P. Henze, H. C. Martin, D. W. Parsley, "Zero-Voltage Switching in High Frequency Power Converters Using Pulse Width Modulation," Proc. IEEE Applied Power Electronic Conference, 1988., pp. 33-40.

[20] Stephen D. Freeland, "I. A Unified Analysis of Converters with Resonant Switches II. Input-Current Shaping for Single-Phase AC-DC Power Converters," Ph.D. Thesis, California Institute of Technology, June 1988.

[21] Slobodan Ćuk, "Modelling, Analysis and Design of Switching Converters," Ph.D. Thesis, California Institute of Technology, November 1976.

[22] R. D. Middlebrook and Slobodan Ćuk, "A General Unified Approach to Modelling Switching Converter Power Stages," IEEE Power Electronics Specialists Conference, 1976 Record, pp. 18–34 (IEEE Publication 76CH1084-3 AES); also International J. of Electronics, vol. 42, no. 6, pp. 521–550, June 1977.

[23] S. Ćuk and R. D. Middlebrook, "A General Unified Approach to Modelling Switching Dc-to-Dc Converters in Discontinuous Conduction Mode," IEEE Power Electronics Specialists Conference, 1977 Record, pp. 36–57 (IEEE Publication 77CH-1213-8 AES).

[24] S. Seshu and M. B. Reed, *Linear Graphs and Electrical Networks.* Addison-Wesley: Reading, Mass., 1961.

[25] Billy B. Y. Lau, "Small-Signal Frequency Response Theory for Ideal Dc-Dc Converter Systems," Ph.D. Thesis, California Institute of Technology, June 1986.

[26] S. Ćuk, "General Topological Properties of Switching Structures," IEEE Power Electronics Specialists Conference, 1979 Record, pp. 109–130 (IEEE Publication

79CH-1461-3 AES).

[27] Slobodan Ćuk and Dragan Maksimović, "Integrated-Magnetics, Quasi-Resonant Ćuk DC-to-DC Converter," in *Recent Developement in Resonant Power Conversion*, edited by K. Kit Sum, Intertec Communications, Inc., 1988.

[28] M. F. Schlecht and L. F. Casey, "A Comparison of the Square-Wave and Quasi-Resonant Topologies," IEEE Applied Power Electronics Conference, 1987 Record, pp. 124-134.

[29] Zhe Zhang, "Coupled-Inductor Magnetics in Power Electronics," Ph.D. Thesis, California Institute of Technology, October 1986.

[30] Slobodan Ćuk, "Integrated Magnetics Versus Conventional Power Filtering," INTELEC 87 Conference, 1987.

[31] C. A. Desoer and E. S. Kuh, *Basic Circuit Theory*. McGraw-Hill: New York, 1969.

[32] B. Peikari, *Fundamentals of Network Analysis and Synthesis*. Prentice-Hall: Englewood Cliffs, N.J., 1974.

[33] M. Vidyasagar, *Nonlinear System Analysis*. Prentice-Hall: Englewood Cliffs, N.J., 1978.

[34] R. Blanchard and P. E. Thibodeau, "The Design of a High Efficiency, Low Voltage Power Supply Using MOSFET Synchronous Rectification and Current Mode Control," IEEE Power Electronics Specialists Conference, 1985 Record, pp. 355-366.

[35] C. S. Korman et al. , "A Synchronous Rectifier for High-Density Power Supplies," Proc. High-Frequency Power Conversion Conference, 1988., pp. 128-139.