OPTIMIZATION AND MINIATURIZATION OF MICROPROCESSOR POWER SUPPLIES

Thesis by
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To my family

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Abstract

This thesis is motivated by the power demands of the modern Intel microprocessors. These microprocessors require a very stable and tightly controlled core supply voltage in order to reliably operate at their correct clock frequency. The core supply voltage has to remain within the prescribed window during normal operation, as well as during power-up and power-down when the processor current can change from almost zero to 16A or more in 200-300ns. Maintaining tight processor voltage regulation during these current transients can be difficult. In addition to stringent load transient specifications, a microprocessor power supply has to meet efficiency requirements, as well as size and cost requirements. Size requirements become especially important in portable computer systems where space is at a premium.

The work presented in this thesis deals with the optimization of the microprocessor power supply for performance, size and cost, with the emphasis on size. Every aspect of the power supply is carefully analyzed and optimized through the size prism: the topology, the control algorithm, and the components. Design and optimization tools are developed, and the theoretical calculations are verified in hardware. The result of the optimization is a microprocessor power supply that meets Intel Pentium III electrical performance specs in approximately one-fifth of the specified volume, resulting in a power density of roughly $40W/in^3$.

Contents

Chapter 1

Introduction

Today, we live in an increasingly "electronic" world dominated by computers, mobile phones, and pagers. Having instant access to information anywhere and everywhere is becoming essential. And, as the world strives for global connectivity, it leaves it up to the discipline of power electronics to provide the power the world needs to achieve its goal.

Power electronics, in general, deals with the conversion of electric power from one form to another. Since electric power can be either dc-power or ac-power, only four power conversion possibilities exist; namely, dc-to-dc, dc-to-ac, ac-to-dc, and ac-to-ac.

Electronic equipment such as computers and other types of consumer electronic devices operate from dc-power. However, the commonly available power sources are the ac-power from the utility grid and dc-power from batteries. Neither of these power sources can readily power a typical electronic device. Instead, this power has to be conditioned before it can be used. In case of the utility grid, the ac-power needs to be converted to dc-power; in case of a battery source, the dc battery voltage usually needs to be converted to different value of dc voltage.

An example of the utility ac-power being converted to dc-power is a desktop computer. The computer power supply, commonly referred to as the "silver box," takes the ac-power input and converts it to several dc-power outputs required for the proper operation of the computer system. In the past, dc-power provided by the silver box was good enough to guarantee proper operation of the microprocessor and the entire system. However, constant advances in silicon processing enabled the processor manufacturers to increase the number of devices per unit area of a silicon wafer. As the device density per unit area increased, more and more computational power could be packed in the same silicon area. But, as the number of devices increased, so did the power requirements of the processor. Fueling more and more complex processors with higher and higher clock rates became a rather difficult problem for several reasons. First, in an effort to reduce the power dissipated by the processor, CPU manufacturers started lowering the operational voltage of their chips. As a result, maintaining the logic level accuracy became harder simply due to less available voltage headroom. This immediately translated into severe restrictions on the variation of the processor supply voltage, and thus, into very tight power supply output voltage regulation requirements.

Second, the increased number of devices per unit of silicon area of the processor increase the current consumption of the part. The power supply has to be able to deliver the current required by the processor both during normal operation and during "wake up" and "power down" sequences while maintaining a tight output voltage regulation. The "wake up" and "power down" sequences are particularly taxing for the power supply. In these modes of operation the current consumption of the processor can change from maximum to minimum in a matter of nanoseconds. Yet, the power supply has to meet

the processor current demands and keep the processor supply voltage variation within the prescribed limits to insure normal, reliable, high-speed operation of the system.

In light of the development trends in the microprocessor industry, it became clear the silver box was no longer able to adequately fuel the modern "megaprocessor". The conventional power distribution scheme in which the silver box supplied power to a connector at one end of the motherboard had to be changed. The long power traces from the motherboard power connector to the processor introduced too much parasitic inductance and resistance into the supply line. These parasitics were the cause of unacceptable processor supply voltage variations under normal operating conditions. The only way to eliminate the effect of the parasitics associated with the power supply traces was to make them as short as possible. Hence, a new power distribution philosophy was born. The dc voltage provided by the silver box had to be stabilized at a location physically close to the load, the microprocessor. The dc-to-dc converter used to achieve this goal became known as the Voltage Regulator Module (VRM) or the Point-of-Load module. The VRM's job was to tightly control the microprocessor supply voltage and provide the required current on demand. Due to the proximity of the VRM to the processor, the parasitics between the processor and the VRM output were minimized and limited to the resistance and inductance of a short supply trace and the processor package leadframe. Now, the processor supply voltage could be tightly controlled providing that the VRM had good load transient response. In addition to good transient response, the VRM had to meet additional requirements. The VRM had to be efficient, small, and low cost. VRM efficiency was important because of the cooling and heat removal issues around the processor that dissipates power by itself. In addition, the efficiency of the

VRM is crucial for battery life in laptop computers. Keeping the size of the VRM small was important due to the limited amount of space available on the motherboard. Finally, the low cost requirement was obviously of a purely economic nature and in line with trying the keep the overall cost of the computer system at an absolute minimum. Clearly, the VRM has to satisfy a number of conflicting conditions. The optimization of a VRM is the focus of this thesis.

As it was demonstrated on an example of a desktop computer, ac-power has to first be converted to dc-power, and then processed again by a dc-to-dc converter before it can be used to power a modern microprocessor. On the other hand, when the supply is a dc battery source instead of the utility ac-grid, the ac to dc power conversion is eliminated, but the dc-to-dc conversion still has to take place. Various examples of this type of conversion are found in mobile phones, pagers, and all kinds of other hand-held and portable equipment. While these devices require much less power than a microprocessor of a desktop computer, the VRM and the power supply of a mobile phone share several common characteristics: high efficiency, small size, and low cost. In battery powered applications, the efficiency of the power supply is of utmost importance. Since the power source is limited, the less power is wasted in the power supply, the longer will the device be able to operate before the battery is fully discharged. The size and weight of the power supply are equally important in portable equipment. In order to make a portable device convenient and portable, it has to be small and light. Keeping the size and the weight of the power supply at a minimum contributes to the reduction of the size and the weight of the overall system making it more convenient, portable, and more attractive to

the consumer. Finally, the last, but no less important, concern is to maintain the low cost of the power supply in order not to drive up the cost of the portable device.

In light of these developments in the computer and portable electronic device industries, the dc-to-dc converter, and its designer, are facing never before encountered challenges in dc-to-dc power conversion. The only presently known way to reduce the size of a switching dc-to-dc power supply is to increase its switching frequency. Unfortunately, the efficiency of the power supply is heavily dependent on the switching frequency. Therefore, a reduction in size of the power supply is inevitably accompanied by the degradation of its efficiency. Furthermore, maintaining a tightly regulated processor supply voltage under a zero to full load current transient requires, in a conventional design, a significant amount of capacitance at the output of the power supply. Providing an adequate amount of capacitance to meet the transient specifications results in an increase of the size of the power supply and contradicts the goal to keep the power supply small. Ways to reconcile these conflicting requirements and optimize the dc-to-dc power supply for computer and mobile applications are addressed in this thesis.

The analysis presented in this thesis was motivated by VRM specifications. However, developed concepts and optimization tools are general, and can readily be applied in other arenas where high efficiency and small size are of particular interest.

VRMs are designed to use the voltages provided by the silver box (3.3V, 5V, 12V) and convert them into an appropriate processor supply voltage requested by a five bit voltage identification code supplied by the processor to the VRM. The switched mode power supply best suited for VRM applications is a step-down buck converter. There are two possible implementations of a buck converter: regular buck and synchronous buck.

Chapter 5 compares the efficiency of these two implementations of the buck converter. The efficiency is studied as a function of the switching frequency and of the load current. This analysis is aimed at exploring the feasibility of reducing the size of the power supply by increasing the switching frequency while maintaining a high efficiency. The loss distribution is used to identify areas in which improvements can be made.

The advantages and weaknesses of both implementations of a low voltage, buck converter operating at a high switching frequency were clearly exposed in Chapter 5. The examination of the loss distribution in the synchronous buck converter revealed that the switch timing is critical for efficient operation at moderately high switching frequencies. Chapter 6 addresses the switch timing issues in the synchronous buck converter and proposes a switch driver that significantly improves the efficiency of the synchronous buck VRM.

Unlike Chapters 5 and 6 which primarily deal with the efficiency of the VRM, Chapter 7 is devoted to its load transient response. Chapter 7 defines the optimum transient response and discusses the proper ways to close the voltage mode control loop in order to achieve the desired transient response.

Chapter 2

From the Silver Box to the VRM

The demand for faster, more powerful computers keeps pushing the microprocessor manufacturers to pack more computational power and more features into each new generation of microprocessors. As a result, the power requirements of the microprocessor have steadily been increasing. Under the circumstances, thermal management became a significant concern. Adequate cooling of the processor, and the entire system, became increasingly difficult. To alleviate the problem, CPU designers lowered the supply voltage required by the core logic of the processor. A lower operating voltage of the processor core logic results in lower processor power requirements providing the clock frequency remains unchanged. Or, looking at it in another way, for a given power dissipation, a processor with a lower core logic operating voltage can run at a higher clock frequency. Hence, it is quite clear that as microprocessors become more powerful, they will continue to migrate to lower voltages and higher operating currents making power distribution and delivery an important aspect of the overall system architecture.

In November of 1995, Intel published the power supply guidelines for the Pentium® Pro processor [17]. Selected electrical specifications for a 150MHz, 256-Kbyte L2 Cache

Pentium Pro® are presented in Table 2.1. Most of the specifications contained in Table 2.1 are common in dc-to-dc converter data sheets: input voltage, output voltage, peak load current, and maximum output voltage ripple. The only processor power supply specific requirement is the unusually demanding load transient response spec. According to Table 1.1, the output voltage of the converter has to stay within ±5% of the nominal voltage under all normal operating conditions, including a sudden I_{min} to I_{peak} output current transient.

Parameter	Value
Output voltage	3.1V
Output voltage ripple and noise	±1%
Output voltage variation with load	±2%
Transient output voltage tolerance	±5%
I_{min}	0.3A
I_{max}	9.9A
I_{peak}(several μs of overshoot)	11A
Slew rate (I_{min} to I_{peak})	30A/μs at converter pins
Load toggle rate	100Hz to 100kHz

Table 2.1: Pentium Pro power supply specifications

The specified tight output voltage regulation is essential for proper operation of the processor. Overshooting the voltage specification can cause certain signals to violate the

Minimum Valid Delay timing specifications. This timing violation will lead to system instability and failure. Furthermore, excessive and sustained overshooting can cause hot electron related effects that can compromise the reliability and the life of the processor.

Undershooting the voltage specification, on the other hand, degrades the performance of the processor, and can lead to timing related failures. The processor will not function properly at its correct clock frequency. The effects of undershooting are further aggravated by improper cooling mechanisms.

2.1 Conventional Power Distribution Architecture

In the previous section we described some of the mechanisms that cause unreliable system operation and system failure when the processor supply voltage deviates more than ±5% from nominal. Hence, the processor voltage has to be tightly controlled to ensure proper, reliable high speed operation. The question is, how can this voltage regulation be achieved.

Let's start off with the conventional, centralized power distribution scheme shown in Fig. 2.1. This power distribution architecture is standard in desktop systems. In this

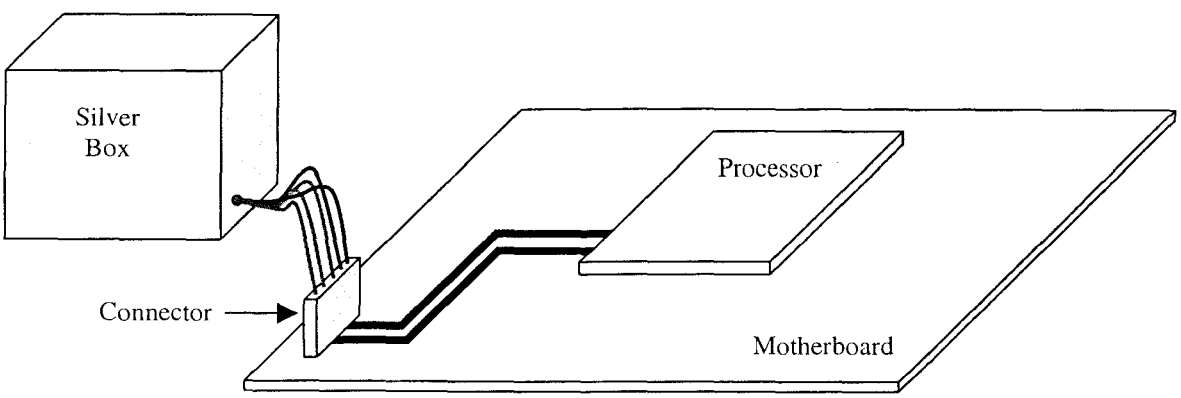


Figure 2.1: Conventional desktop computer power distribution scheme

approach, an off-board power supply (the silver box) converts the AC voltage from the supply line into several DC voltages needed by the processor and other peripheral devices. The appropriate output of the silver box is connected to a connector located at the edge of the motherboard using a number of wires approximately 6 to 8 inches long. From the motherboard connector, the supply voltage is routed to the processor using heavy copper traces on the motherboard.

In an effort to evaluate whether this conventional approach is adequate for powering Pentium® Pro processors, a lumped circuit model of the conventional power distribution architecture was developed. As Fig. 2.2 shows, the output of the silver box is modeled by an ideal voltage source; the wiring, the motherboard connector, and the PCB traces are modeled by their respective series resistance and inductance; the supply and the return paths are modeled separately. The model of Fig. 2.2 can be used to calculate the voltage at the processor pins during both steady state operation and sudden processor current transients.

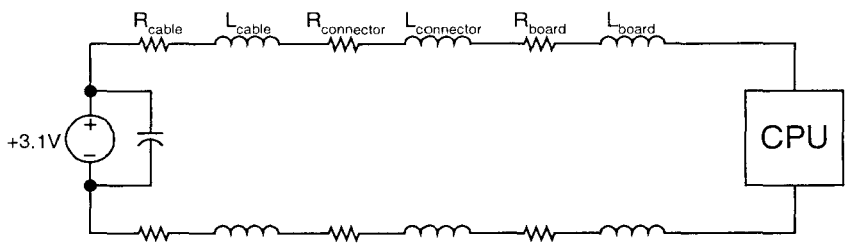
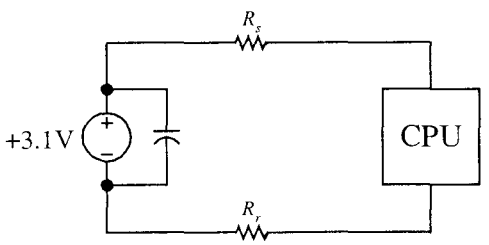


Figure 2.2: Model of the conventional power distribution scheme

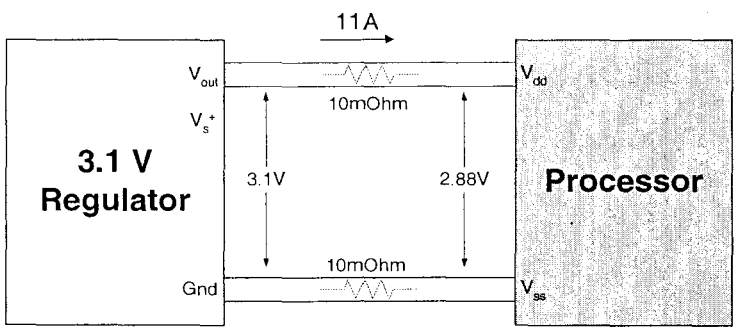
2.1.1 Effects of the Parasitic Resistance of the Supply Path on the Processor Voltage

The effects of the supply path resistance will be studied under the assumption that the processor is constantly drawing its maximum rated current from the power supply.

Under this assumption, I_{out}=11A=const. Consequently, $dI_{out}/dt = 0$ resulting in a zero voltage drop across all the inductances in Fig. 2.2. Therefore, all the inductances can, for the moment, be neglected. After neglecting all the inductances and collecting all the resistances in the supply path into a single resistor R_s, and all the resistances in the return



a)



b)

Figure 2.3: a) Simplified model of the conventional power distribution scheme; b) Voltage drops observed in the system

path into R_r, we arrive at a simplified, steady state model of the conventional power distribution scheme. This simplified model is shown in Fig. 2.3a.

If we assume that the total resistance in the supply path, denoted by R_s in Fig. 2.3a, is only 10mΩ, and is equal to the total resistance in the return path, R_r, we can easily calculate the voltage at the processor pins. The results of the voltage calculations are

given in Fig. 2.3b. Fig. 2.3b shows the voltage across the processor pins to be only 2.88V at the rated processor current because of the voltage drop caused by the resistance of the supply and the return path.

According to Table 2.1, the maximum allowed supply voltage variation with load is ±2% of 3.1V, or ±62mV. Thus, the minimum processor supply voltage is 3.1-0.062=3.038V. Fig. 2.3b shows assuming even a minimal supply trace resistance of 10mΩ, the conventional power distribution architecture cannot meet the Pentium® Pro specs during steady state operation. In fact, just to meet steady state specs, the total resistance of the supply path together with the return path would have to be less than 14mΩ. Since the 14mΩ has to include approximately 16 inches of wire, the motherboard connector, and PCB traces, it is clear that this architecture cannot meet the processor's power requirements.

2.1.1.A Remote Sensing

The voltage droop caused by the large processor current across a small parasitic resistance of the supply path, R_s, can be remedied by the use of a regulator that supports remote sensing. Remote sensing is a technique that uses extra connections to sense and regulate the voltage at the point of use. The voltage sense leads carry almost no current and are, therefore, unaffected by the resistance in their path. Consequently, the voltage is accurately regulated at the sense points. Fig. 2.4 shows a system that offers remote sensing in the supply path. The regulator now regulates the voltage at the processor supply pins with respect to the regulator ground (Gnd). Consequently, as Fig. 2.4 shows, the regulator raises the voltage at its output pins in order to compensate for the voltage drop in the supply line. The regulator does not, however, compensate for the drop in the

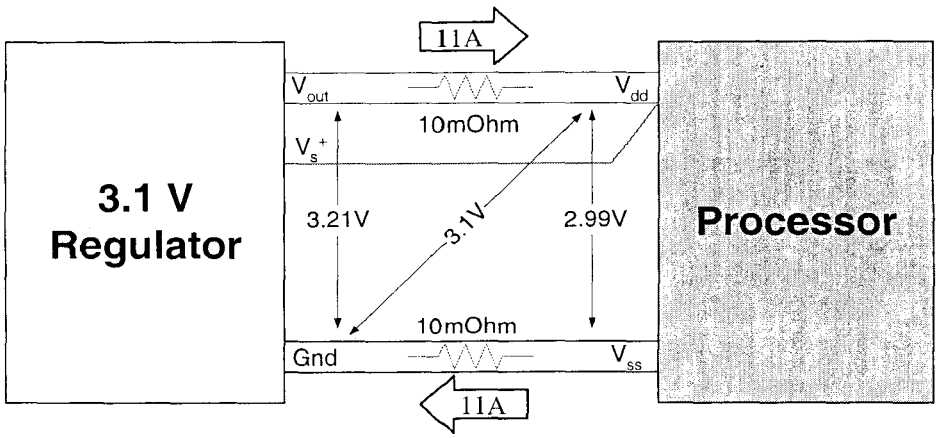


Figure 2.4: Conventional desktop computer power distribution scheme with remote sensing in the supply path.

return path. There are two possible solutions to this problem. The first is to minimize the resistance in the return path by using heavy ground planes and multiple processor connections. The other possibility is to use a regulator that offers remote sensing in both the supply and the return paths. However, the addition of the return path sense considerably complicates regulator design, and most off-the-shelf regulators do not offer it.

2.1.2 Effects of the Parasitic Inductance of the Supply Path on the Processor Voltage

Due to the high specified processor current slew rate, the parasitic inductance of the power supply lines presents an even greater problem than its parasitic resistance. In order to fully appreciate the magnitude of the problem, consider the following: 1cm of round wire in air exhibits approximately 10nH of inductance. The voltage drop across this piece of wire can be calculated according to

$$\Delta V = L\frac{di(t)}{dt} \tag{2.1}$$

Substituting for $di(t)/dt$ in (2.1) the specified load current slew rate of $0.03\frac{A}{ns}$ gives us a voltage drop of 300mV! So, only 1cm of wire between the source and the processor pins is enough to push the voltage at the processor pins out of spec regardless of the behavior of the source. To illustrate this, consider the circuit in Fig. 2.5 obtained from the circuit of Fig. 2.2 by setting all the resistances zero and replacing the CPU with a time varying current source. Even though V_1 is assumed to be an ideal voltage source, the voltage across the current source (CPU) will experience a constant droop equal to

$$\Delta V = 2L\frac{di(t)}{dt} = 600\text{mV} \tag{2.2}$$

during the 360ns it takes the processor current to ramp up to its maximum value. In other words, the ability of a power supply to respond to the kind of load current change specified in Table 2.1 is no longer dominated exclusively by the speed of the control loop. Instead, the inductance of the supply determines how quickly can current be delivered to the load. In fact, unless this inductance can be made low enough, even an ideal voltage source cannot meet processor supply voltage tolerances.

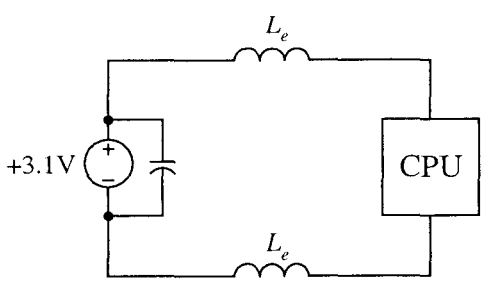


Figure 2.5: Simplified model of the computer power distribution architecture during the load transient

The previous example shows that as little as 10nH of inductance in the supply path drives the voltage at the processor pins way outside the specifications. In the conventional power distribution architecture, a typical supply path includes, as shown in Fig. 2.1, approximately 16 inches of wire, a motherboard connector, and PCB traces. Thus, the total inductance in the supply path is far greater than 10nH. This parasitic inductance of the supply path makes it impossible for any off-board power supply, with or without a remote sense, to meet the specifications outlined in Table 2.1.

In the preceding discussion, the output of the silver box had been modeled by an ideal voltage source to illustrate the effect of supply line inductance on the voltage at the processor pins. In reality, however, the silver box is a switched mode power supply whose output voltage is regulated by a feedback loop. A typical switching frequency of the converter inside a silver box is around 100kHz. Thus, the duty cycle of this power supply is updated every 10μs. By comparison, the processor current ramps up in only 360ns. Clearly, the power supply cannot respond to this change in its load current until the beginning of the next switching cycle. This inherent inability to react faster causes the output voltage of the power supply to droop. As a result, the initial fast spike at the processor supply pins caused by the voltage drop across the supply line inductance is followed by a slow voltage droop caused by the droop of the supply's output voltage. This droop is the difference between the response of an ideal voltage source and a real life power supply to the load current change specified in Table 2.1.

2.1.2.A Capacitive Bypassing

The only way to quickly deliver current to the load is to place a source physically close to the load. This is accomplished through proper use of bypass capacitors. Bypass

capacitors are placed close to the processor in order to minimize the inductance and the resistance of the trace that connects them to the processor supply pins. As a result, the stability of the processor voltage can be improved.

As it was pointed out in the preceding section, a power supply needs time to respond to a sudden change in its load current. Placing bypass capacitors close to the processor allows them to supply the processor current and maintain the voltage at the processor pins within transient limits until the power supply responds. As a result, the number and the quality of the bypass capacitors exclusively determine the initial response to a fast current transient.

Theoretically, the centralized power distribution scheme of Fig. 2.1 could meet the Pentium Pro specifications with the use of remote sensing and enough bypass capacitance. However, due to the inductance of the wiring that connects the output of the silver box to the bypass capacitor bank, the required number of bypass capacitors would be very large. These capacitors would add to the overall cost of the system and occupy valuable motherboard real-estate. Furthermore, with increasing power demands, this system would become increasingly cumbersome, expensive and, therefore, impractical.

2.2 Distributed Power Architecture

In light of the challenges posed by the parasitic inductance and resistance of the conventional supply path, a logical, new distributed power delivery architecture, shown in Fig. 2.6, was adopted. The idea behind the new architecture was to minimize the physical distance between the output of a fast supply with tight regulation, named Voltage Regulator Module (VRM), and the load (CPU). In this way, the voltage is tightly regulated at the point of use, and supplied to the processor supply pins using only

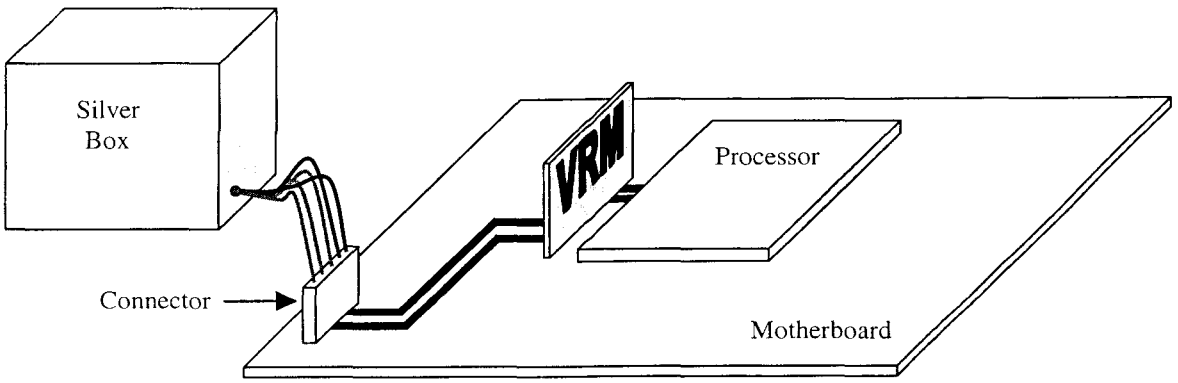


Figure 2.6: Distributed desktop computer power distribution scheme

a short, low inductance, low resistance PCB trace. So, while the length of the supply path hasn't really changed in comparison with the conventional power distribution architecture, "re-regulation" of the silver box voltage close to the processor eliminates the effects of the parasitic inductance and resistance of the lengthy supply path on the voltage at the processor supply pins. Furthermore, good transient performance of the VRM, and its proximity to the point of use make it possible to significantly reduce the amount of required bypass capacitance in comparison with the conventional centralized power distribution scheme.

2.2.1 The VRM

In addition to good transient performance, the VRM has to satisfy several other conditions. First, the VRM needs to be as efficient as possible to minimize the power it dissipates inside the system. An efficient VRM will keep its contribution to the temperature rise inside the system at a minimum, and thus, facilitate the overall thermal design of the system. Second, the VRM has to be small to allow it to be placed as close to the point of use as possible without taking up more valuable space than it is absolutely

necessary. And finally, the VRM should be inexpensive in order not to increase the price of the entire system.

2.2.1.A VRM Candidate Topologies

According to the specifications in Table 2.1, the task at hand is to design a DC-DC converter with a 5V input and an output of 3.1V; no isolation is required.

A buck converter shown in Fig. 2.7 is the simplest, and the most cost-effective, way to achieve non-isolated voltage step-down in the specified voltage range. Furthermore, the buck topology has no internal capacitive energy storage-the output is directly connected to the input during the on-time of the main switch (S_1). Therefore, a buck converter is well suited to respond to sudden load current changes, an absolute must in VRM applications.

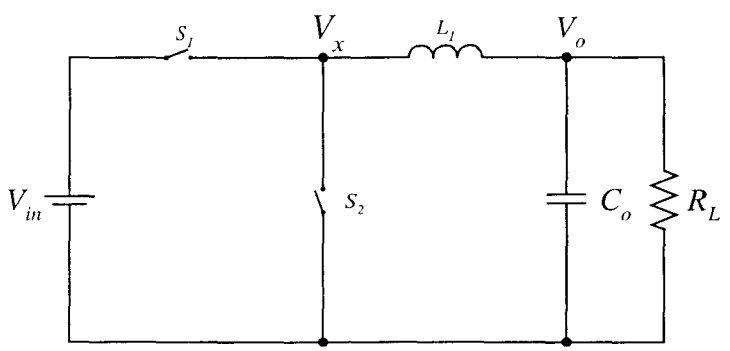


Figure 2.7: Basic buck converter

While the buck topology clearly stood out as the most-likely-to-succeed VRM candidate, it was less than obvious which buck topology implementation, regular or synchronous, would be the best choice. This question will be addressed in detail in Chapter 5.

Chapter 3

Overview of the Buck Converter Load Transient Response

A Pentium Pro VRM has to meet or exceed a number of electrical and mechanical specifications. Per Table 2.1, the two most challenging electrical specifications are the required tight output voltage regulation of ±5% during a fast zero to full load output current transient and the required high efficiency at full load. Still, meeting these specifications by themselves would not be particularly hard What makes VRM design rather difficult is meeting these electrical specifications in absolutely the smallest volume possible.

The first thing a VRM has to satisfy are the transient response specifications. If they are not met, the module cannot perform its function, and is useless. Thus, meeting the transient response specs has to be chosen as the starting point in VRM design. The constraints imposed by the transient response largely determine the direction that the design will take.

In Chapter 2, the buck topology has been identified as a topology suitable for VRM applications. Since the load transient response has been identified as a starting point in

VRM design, the load transient response of the chosen topology has to be thoroughly analyzed and well understood in order to insure an optimum overall design.

3.1 Overview of the Buck Converter Load Transient Response

The chosen VRM topology, a buck converter, was given in Fig. 2.7, and is reproduced here, in Fig. 3.1, for convenience. Per Table 2.1 the load current transient occurs in approximately 360ns. By today's standards, a rather high power supply switching frequency might be around 500kHz, resulting in a switching period of 2μs. Thus, even if the converter is switching with a rather high switching frequency, the load current transient still occurs in about a sixth of the regulator's switching period.

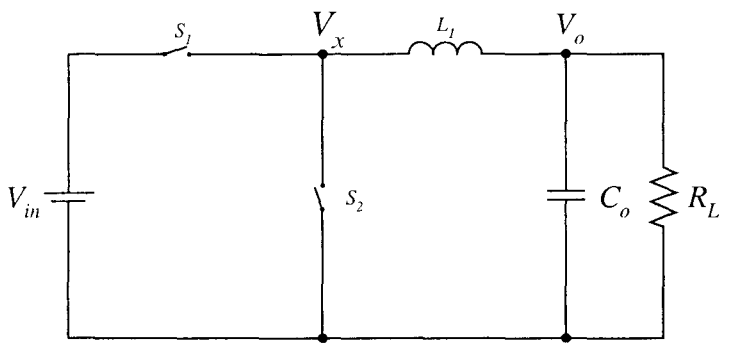


Figure 3.1: Basic buck converter

A typical regulator response to an almost zero to full-load load current change occurring within a fraction of the regulator's switching period (see Fig. 3.2a) is sketched in Fig. 3.2b. After a load current transient, the converter will need a number of switching cycles to reach a new steady-state. During the transition to the new steady state, four distinct response intervals, I_1 through I_4, can be identified as shown in Fig. 3.2b. The first interval, I_1, coincides with the rise-time of the load current; I_2 represents the response delay inherent to switching converters; I_3 is the time it takes the average inductor current

to become equal to the load current, and I_4 is the interval during which the output voltage recovers to its nominal value after reaching its minimum value at $t=t_3$.

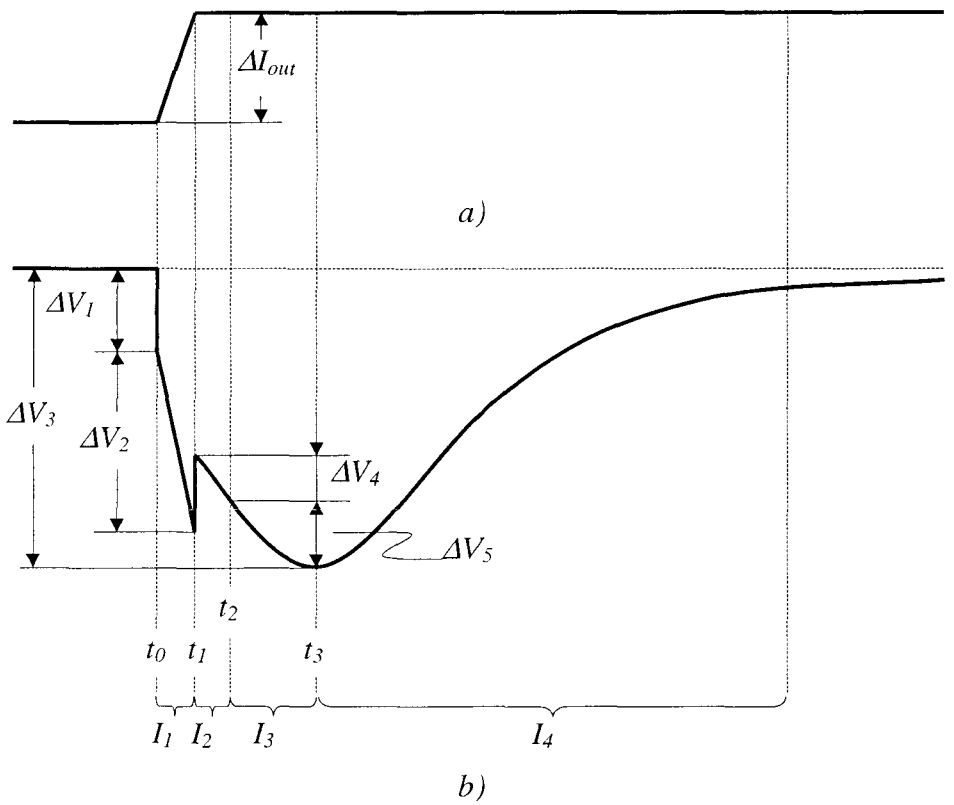


Figure 3.2: Typical load transient response of a buck converter: a) load current step, and b) output voltage

3.1.1 Interval I_1

A switching converter is effectively a discrete-time system whose duty cycle gets updated once during each switching period. Every switching converter is in a sense a discrete-time system because the duty cycle is updated only once during each switching period. Since the load current transient occurs in a fraction of the switching period, an inherent delay will exist between the time when the load current transient occurs and the

time when the duty cycle gets updated at the beginning of the new switching period. During this interval there is no control action, and the converter is responding essentially in an open loop fashion. Consequently, the output of the converter of Fig. 3.1 can be modeled as shown in Fig. 3.3.

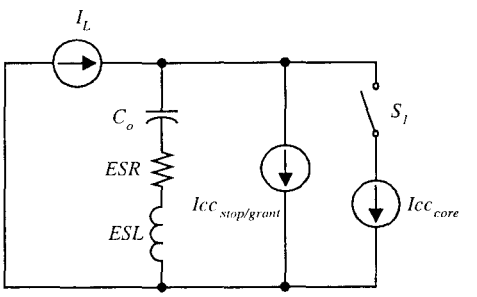


Figure 3.3: Converter output model during the intervals I_1 and I_2

Because the load current transition is much shorter than the switching period of the converter, the output impedance of the converter is simply the impedance of the output capacitors. Therefore, the peak output voltage deviation during I_1 can be expressed as:

$$\Delta V_{o1} = \Delta V_1 + \Delta V_2 = ESL\frac{dI_o}{dt} + ESR \cdot \Delta I_o + \frac{1}{2}\frac{\Delta I_o^{\,2}}{C_o \frac{dI_o}{dt}} \tag{3.1}$$

Hence, the peak output voltage deviation during I_1 depends on the load current slew rate, and the *ESR* and *ESL* of the output capacitors. The magnitude of the spike observed during I_1 is independent of the control loop bandwidth and the chosen switching frequency. Clearly, the only way to reduce the magnitude of this spike is to place a sufficient number of very high quality (low *ESR* and *ESL*) capacitors in parallel at the converter output.

3.1.2 Interval I_2

Because of the high load current slew rate, the load current will have reached its final value long before the controller can respond to this change in the operating point. Consequently, there will be no control action present during I_2, and the converter will continue to respond in an open loop fashion to the sudden load current change that had occurred. Thus, the model of Fig. 3.3 remains valid, and can be used to calculate the peak voltage deviation during I_2.

Since the control loop cannot respond fast enough to the load current change, once the load current reaches its final value at t_1, it will continue to discharge the output capacitors until the controller turns the main switch (S_1) on at t_2. The resulting output voltage drop is:

$$\Delta V_4 = \frac{I_o}{C_o} \cdot D' \cdot T_s = \frac{I_o}{f_s \cdot C_o} \cdot \left(1 - \frac{V_o}{V_{in}}\right) \tag{3.2}$$

where f_s is the switching frequency of the converter, and D' is the duty factor of the switch S_2.

Equation (3.2) shows that the peak voltage drop during I_2 is inversely proportional to the switching frequency and the output capacitance. Thus, keeping ΔV_4 small requires either a large output capacitor or a high switching frequency.

In order to get a quantitative feel for how the size of the output capacitor depends on the chosen switching frequency, (3.2) can be rewritten in the following way:

$$C_o = \frac{I_o}{f_s \cdot \Delta V_4} \cdot \left(1 - \frac{V_o}{V_{in}}\right) \tag{3.3}$$

From (3.3) we can calculate the amount of output capacitance needed to achieve a particular maximum voltage deviation ΔV_4. The value for ΔV_4 is obtained from

preliminary voltage deviation budgeting. Namely, the peak transient voltage drop specified in Table 2.1 is 150mV. This is the total voltage deviation budget for intervals I_2 and I_3. As a starting point, let us allot 50mV to I_2 and 100mV to I_3. Therefore, ΔV_4=50mV can be substituted into (3.3) along with I_o=10A, V_{in}=5V, and V_o=3V.

Using (3.3) the amount of output capacitance required to achieve ΔV_4=50mV for a load current step of 10A is plotted as a function of the switching frequency in Fig. 3.4. Fig. 3.4 shows that at a switching frequency of 500kHz, more than 160μF of capacitance is needed to achieve a voltage drop of less than 50mV during I_2.

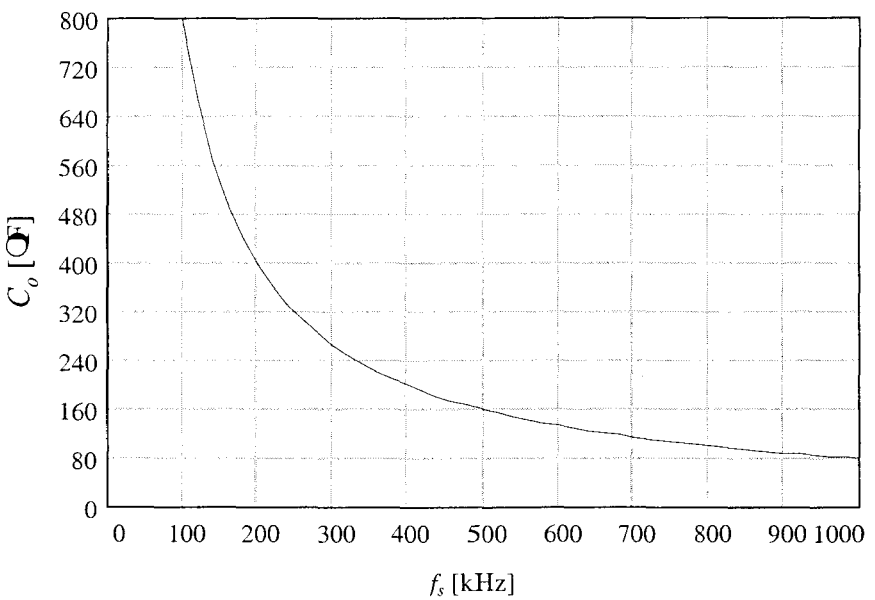


Figure 3.4: Output capacitance required to achieve a maximum voltage drop of 50mV during the interval I_2 as a function of the switching frequency

The question now becomes how to implement 160μF of output capacitance. It would be desirable if only low profile ceramic capacitors in a 1206 package could be used. However, low profile ceramic capacitors in a 1206 package with an X7R dielectric are currently only available with a maximum value of 4.7μF. Placing 35 of these capacitors

on the board might not be acceptable from the required board area and the cost standpoints.

Another possibility to implement the 160μF output capacitance would be to sacrifice the low board profile that could be achieved with ceramic chip capacitors and use either expensive tantalum capacitors or less expensive electrolytic capacitors. In order to keep the board cost in check, one might opt to use 100μF OSCON electrolytic capacitors (10SA100M). Two of these capacitors will provide 25% more capacitance than it is needed to make ΔV_4=50mV. However, the *ESR* of these capacitors is 30mΩ and the *ESL* is about 13nH. Substituting these numbers back into (3.1) yields a drop of approximately 378mV during I_1! Thus, in order to now bring ΔV_{o1} within specs, we would need to use five 10SA100M OSCON capacitors in parallel instead of two that would have been more than enough to meet the 50mV maximum deviation during I_2.

The main disadvantage of using electrolytic capacitors is the significant increase in board height and volume. For example, if only ceramic chip capacitors are used, the component height is only 60 mills. If, on the other hand, electrolytic capacitors are chosen, component height increases significantly. In fact, if 10SA100M OSCON capacitors used in the previous example are chosen, the component height increases to 413 mills. Thus, if the transient response specs can cost effectively be met without electrolytic capacitors at the output, the volume of the module could be reduced 6.8 times! The tremendous height and volume reduction is obviously a huge incentive to avoid placing electrolytic capacitors on the board.

3.1.3 Interval I_3

At $t=t_2$, S_1 is turned on by the control circuit, and the converter starts to respond to the disturbance. For simplicity, we will assume that once the controller turns S_1 on, it will remain on until the average inductor current becomes equal to the load current. In this case, the circuit of Fig. 3.1 can be modeled as shown in Fig. 3.5. From the model, we can write an expression for the output voltage for $t>t_2$:

$$V_o(t) = i_c \cdot ESR + \frac{1}{C_o} \cdot \int_0^t i_c \cdot dt \tag{3.4}$$

where i_c is the capacitor current. Applying Kirchoff's current law we get:

$$i_c = i_L - I_o \tag{3.5}$$

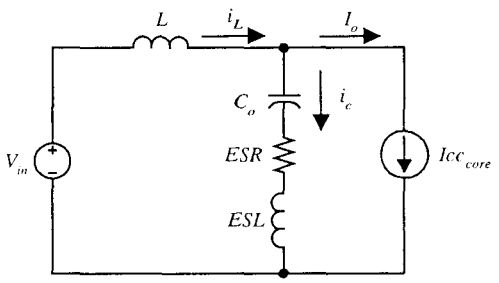


Figure 3.5: Simplified model of the converter output during the interval I_3

From Fig. 3.5, the inductor current can be expressed as:

$$i_L = \frac{V_{in} - V_o}{L} \cdot t = S \cdot t \tag{3.6}$$

where S is the slope of the inductor current. After substituting (3.5) and (3.6) into (3.4) and evaluating the integral we get:

$$V_o = (S \cdot t - I_o) \cdot ESR + \frac{S \cdot t^2}{2 \cdot C_o} - \frac{I_o \cdot t}{C_o} \tag{3.7}$$

Equation (3.7) can now be used to calculate the peak output voltage deviation during the interval I_3. The time when the output voltage reaches its minimum value can be calculated by taking the derivative of (3.7) and setting it to zero. Solving for t yields:

$$t_m = \frac{I_o}{S} - C_o \cdot ESR \tag{3.8}$$

In some cases, t_m might turn out to be negative indicating that the voltage drop across the ESR is dominant. In such cases a value of zero should be used for t in (3.7). Otherwise (3.8) can be substituted into (3.7) to calculate the peak output voltage deviation during the interval I_3:

$$\Delta V_5 = \frac{I_o^2}{2 \cdot C_o \cdot S} + \frac{1}{2} \cdot S \cdot C_o \cdot ESR^2 = \Delta V_5' + \Delta V_5'' \tag{3.9}$$

From (3.9), $\Delta V_5'$ can be expressed as:

$$\Delta V_5' = \left(\frac{I_o}{S} \right)^2 \cdot \frac{S}{2C_o} \tag{3.10}$$

Similarly, $\Delta V_5''$ can be written as:

$$\Delta V_5'' = (ESR \cdot C_o)^2 \cdot \frac{S}{2C_o} \tag{3.11}$$

Keeping in mind that (3.9) holds if t_m>0 from (3.8) we get:

$$\frac{I_o}{S} > ESR \cdot C_o \tag{3.12}$$

From (3.10), (3.11), and (3.12) it is clear that (3.9) holds *iff*:

$$\Delta V_5' > \Delta V_5'' \tag{3.13}$$

From (3.9) we can calculate how much output capacitance will be needed to insure that ΔV_5 does not exceed the chosen maximum value at the selected switching frequency.

Substituting $S = \frac{V_{in} - V_o}{L}$ into (3.9) yields:

$$\Delta V_5 = \frac{L \cdot I_o^2}{2 \cdot C_o \cdot (V_{in} - V_o)} + \frac{1}{2} \cdot \frac{(V_{in} - V_o)}{L} \cdot C_o \cdot ESR^2 = \Delta V_5' + \Delta V_5'' \qquad (3.14)$$

Equation (3.14) gives the peak voltage deviation during I_3. This result is a bit counter intuitive. Namely, one would expect ΔV_5 to be proportional to the size of the inductor and inversely proportional to the size of the output capacitor. This dependence is, indeed, present in the first term in (3.14). However, the second term is actually, unexpectedly, proportional to the size of the output capacitor and inversely proportional to the size of the inductor. This would tend to indicate that at one point the second term in ΔV_5 could become dominant and ΔV_5 would start to increase as the value of the output capacitor is increased. However, this cannot happen because of the condition given by (3.13). Thus, despite the second term in (3.14), ΔV_5 can be minimized by increasing output capacitance or decreasing the size of the inductor.

The size of the inductor is closely related to the switching frequency. Since

$$\Delta I_L = \frac{V_{in} - V_o}{L} \cdot D \cdot T_s \qquad (3.15)$$

we get:

$$L = \frac{V_{in} - V_o}{\Delta I_L} \cdot D \cdot T_s \qquad (3.16)$$

where ΔI_L is the peak to peak inductor current ripple, D is the duty cycle of the main switch (S_1), and T_s is the switching period. Substituting (3.16) into (3.14) and rearranging, we get:

$$\Delta V_5 = \frac{\frac{V_o}{V_{in}} \cdot I_o^2}{2 \cdot C_o \cdot \Delta I_L \cdot f_s} + \frac{1}{2} \cdot \frac{\Delta I_L}{\frac{V_o}{V_{in}}} \cdot f_s \cdot C_o \cdot ESR^2 \tag{3.17}$$

Assuming further that

$$\Delta I_L = k \cdot I_o \tag{3.18}$$

where k would typically have a value between 0.1 and 0.4 (for an inductor current ripple of 10% to 40% of the maximum load current), (3.17) becomes:

$$\Delta V_5 = \frac{\frac{V_o}{V_{in}} \cdot I_o}{2 \cdot C_o \cdot k \cdot f_s} + \frac{1}{2} \cdot \frac{k \cdot I_o}{\frac{V_o}{V_{in}}} \cdot f_s \cdot C_o \cdot ESR^2 \tag{3.19}$$

Equation (3.19) gives an expression for ΔV_5 as a function of the switching frequency and the output capacitance. In order for (3.19) to be valid, inequality (3.12) still has to be satisfied. Given the form of (3.19), it is more convenient to rewrite (3.12) in the following way:

$$f_s \cdot C_o < \frac{1}{ESR \cdot \frac{V_o}{V_{in}} \cdot k} \cdot \tag{3.20}$$

From (3.19) the amount of output capacitance required to achieve a prescribed maximum drop during I_3 can be expressed as a function of the switching frequency with the inductor current ripple as a parameter. So, choosing the maximum allowable deviation for ΔV_5 and solving for C_o, we get:

$$C_o = \frac{\Delta V_5 - \sqrt{\Delta V_5^2 - I_o^2 \cdot ESR^2}}{I_o \cdot k \cdot f_s \cdot ESR^2} \cdot \frac{V_{in}}{V_o} \tag{3.21}$$

Equation (3.21) is, of course, valid if:

$$C_o < \frac{1}{ESR \cdot \frac{V_o}{V_{in}} \cdot k \cdot f_s} \cdot \tag{3.22}$$

Equation (3.21) was used to create Fig. 3.6 which shows the output capacitance required to achieve ΔV_5=100mV as a function of the switching frequency with the inductor current ripple as a parameter.

Fig. 3.6 shows that at 500kHz achieving 100mV of voltage drop during I_3 requires between 150μF and 650μF of output capacitance, depending on the size of the buck inductor. Recalling for the moment that because of intervals I_1 and I_2 we already have 500μF on the board, we could safely choose a k of 0.2 at f_s=500kHz.

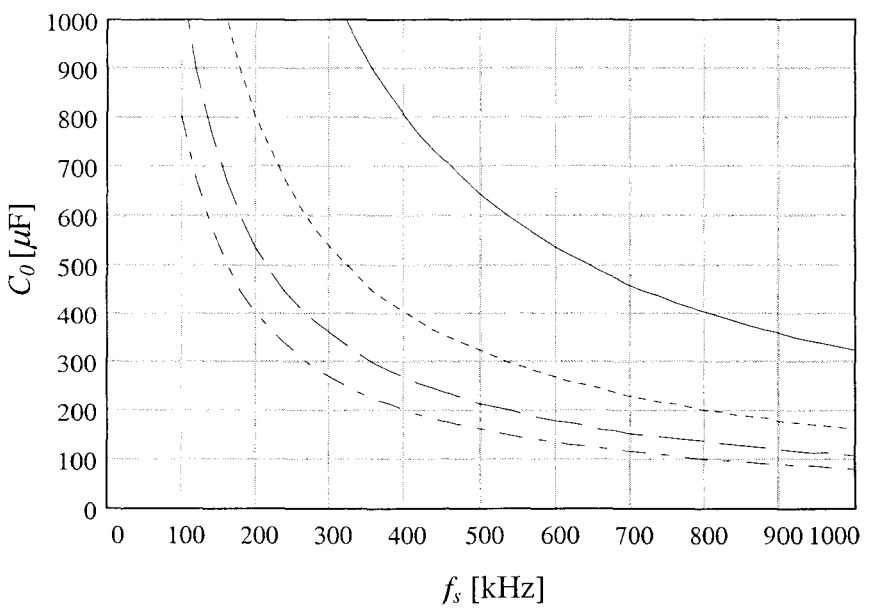


Figure 3.6: Output capacitance required to achieve ΔV_5=100mV for four different inductor current ripple magnitudes (k=0.1 to 0.4)

3.1.4 Interval I_4

During I_4 the duty cycle is no longer saturated, and the converter resumes its normal switching pattern. The integral action of the control loop returns the output voltage to its nominal set-point. Since we are currently interested solely in the peak output voltage deviation during a load current transient, circuit behavior during this interval will be discussed in Chapter 7.

3.2 Optimizing Voltage Budgeting

In Section 3.1.2 a preliminary voltage budget was made for the transient response. Under that voltage budget, out of the 150mV of available deviation, 50mV was allotted to the interval I_3, leaving 100mV for the interval I_4. However, the real concern is the total voltage deviation after a transient. In other words, how the voltage drop is distributed between the response intervals is not as critical, as long as the specs are met with the least amount of output capacitance.

In order to optimize the voltage budgeting, the voltage drops during I_2 and I_3 need to be taken into account concurrently. Combining (3.2) and (3.19) we get:

$$\frac{I_o}{f_s \cdot C_o} \cdot \left(1 - \frac{V_o}{V_{in}}\right) + \frac{\frac{V_o}{V_{in}} \cdot I_o}{2 \cdot C_o \cdot k \cdot f_s} + \frac{1}{2} \cdot \frac{k \cdot I_o}{\frac{V_o}{V_{in}}} \cdot f_s \cdot C_o \cdot ESR^2 = \Delta V_4 + \Delta V_5 \qquad (3.23)$$

Solving for C_o as a function of the maximum voltage deviation ΔV_4+ΔV_5 and the switching frequency yields:

$$C_o = \frac{\Delta V_4 + \Delta V_5 - \sqrt{(\Delta V_4 + \Delta V_5)^2 - I_o^2 \cdot ESR^2 \cdot (1 + 2 \cdot k) + 2 \cdot I_o \cdot k \cdot ESR^2 \cdot \frac{V_{in}}{V_o}}}{I_o \cdot k \cdot f_s \cdot ESR^2} \cdot \frac{V_{in}}{V_o} \qquad (3.24)$$

A plot of the output capacitance needed to achieve a combined voltage drop of 150mV during the intervals I_2 and I_3 is shown in Fig. 3.7 as a function of the switching frequency with the inductor current ripple as a parameter.

Fig. 3.7 shows that with better voltage budgeting during the intervals I_2 and I_3, the total output capacitance can be significantly reduced. In fact, at f_s=500kHz, less than 300μF would be enough to keep the output voltage within specs with k=0.2. However,

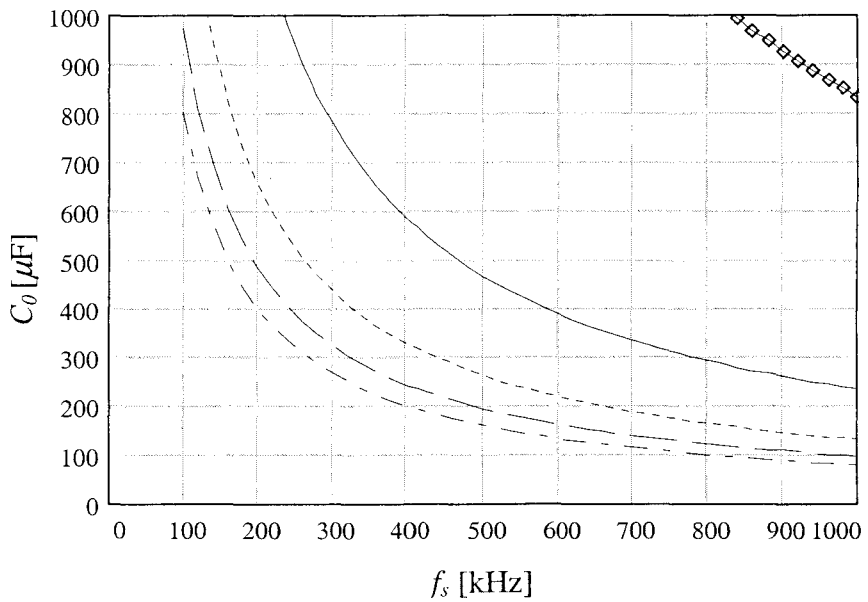


Figure 3.7: Output capacitance required to achieve $\Delta V_4+\Delta V_5$=150mV for four different inductor current ripple magnitudes (k=0.1 to 0.4)

the output capacitance cannot be reduced below 500μF because of the *ESR* and the *ESL* of the chosen capacitors. The overkill in capacitance required to make the *ESR* and the *ESL* sufficiently small to meet specs during I_1 can be used to lower the switching frequency and still meet transient specs during I_2 and I_3. Fig. 3.7 shows that with k=0.2, the switching frequency can be lowered to 300kHz without jeopardizing transient

performance. This reduction in the switching frequency would increase the overall efficiency of the circuit. Hence, the size penalty resulting from the *ESR* and the *ESL* of the chosen capacitors is somewhat compensated by the overall efficiency improvement.

3.3 Approaching the VRM Design Problem

Equations (3.1), (3.2), and (3.19) describe the peak output voltage drops during the three intervals of the buck converter transient response. These three equations are reproduced here for convenience.

$$\Delta V_{o1} = \Delta V_1 + \Delta V_2 = ESL\frac{dI_o}{dt} + ESR \cdot \Delta I_o + \frac{1}{2}\frac{\Delta I_o^{\,2}}{C_o \frac{dI_o}{dt}} \tag{3.25}$$

$$\Delta V_4 = \frac{I_o}{C_o} \cdot D' \cdot T_s = \frac{I_o}{f_s \cdot C_o} \cdot \left(1 - \frac{V_o}{V_{in}}\right) \tag{3.26}$$

$$\Delta V_5 = \frac{\frac{V_o}{V_{in}} \cdot I_o}{2 \cdot C_o \cdot k \cdot f_s} + \frac{1}{2} \cdot \frac{k \cdot I_o}{\frac{V_o}{V_{in}}} \cdot f_s \cdot C_o \cdot ESR^2 \tag{3.3}$$

Obviously, minimizing all three voltage drops yields the best overall transient response. However, the question is how to get the best overall transient response in the smallest volume, with the lowest cost, and with the highest overall efficiency.

From (3.25) it is clear that ΔV_{o1} depends only on the *ESR* and the *ESL* of the output capacitors, and is unaffected by any other circuit parameters like the switching frequency or the control loop bandwidth. Thus, the only way to reduce ΔV_{o1} is to choose high quality capacitors and place a number of them in parallel. Here again the issue of electrolytic capacitors versus ceramic chip capacitors arises. If ceramic chip capacitors are used, ΔV_{o1} will be very small because there will be a large number of low *ESR* and

low *ESL* capacitors at the output. However, meeting transient specs during I_1 may not insure adequate performance during I_2 and I_3 as well. As a result, the number and type of capacitors that will need to be placed at the output will also depend on what happens during the intervals I_2 and I_3. On the other hand, if electrolytic capacitors are to be used, because of their rather high *ESR* and *ESL* a number of them will have to be placed in parallel in order to maintain ΔV_{o1} small. In this case, the *ESR* and the *ESL* determine how many capacitors will have to be used. Typically, however, the amount of output capacitance dictated by ΔV_{o1} will far exceed the capacitance requirements imposed by the intervals I_2 and I_3.

The peak voltage drop during the intervals I_2 and I_3 is given by equations (3.26) and (3.27), respectively. These equations show that good transient response requires either a large output capacitor or a high switching frequency. The optimal solution finds the right balance between VRM size (dictated by the number and the size of the output capacitors) and efficiency (dictated by the switching frequency). For example, from Fig. 3.7 we can see that the total output voltage drop of 150mV during I_2 and I_3 can be achieved with 270μF of output capacitance at a switching frequency of 500kHz. However, meeting the 150mV specification with 270μF of capacitance requires $k \geq 0.2$ (see Fig. 3.7).

It should by now be clear that there are two design paths that can be taken. One possibility is to keep the switching frequency low and rely on the output capacitors to keep the output voltage within specs. There are several problems with this approach. First, bulky electrolytic capacitors required at the output dramatically increase the volume of the module and prevent its use in laptop applications. For now, however, such solutions are still finding their place in the desktop market (where the space is not as

limited) due their low cost. Second, this approach suffers from the lack of scalability. Namely, the trend in the processor industry has been to demand higher core currents with higher slew rates to be provided by the VRM for every new generation of processors. As a result, relying extensively on the output capacitors to do all the work will quickly become a totally unacceptable solution even in the desktop market because of size issues. Therefore, the low frequency, large output capacitor approach is at best a short-term solution and will not be considered here.

The other VRM design path is based on minimizing the role of the output capacitors in keeping the output voltage within specs. Instead, it is desirable to have a fast, high bandwidth control loop do the bulk of the work in keeping the output voltage within the prescribed limits after a fast load current transient. This is achieved by opting to operate the converter at a higher than usual switching frequency. The high frequency, low output capacitance approach advocated in the rest of this thesis produces a scalable, high power density, low volume solution that will be able to efficiently meet future processor power demands.

3.3.1 Merits of the High Switching Frequency

The obvious benefit of a higher switching frequency is the reduction of the physical size of the buck inductor. A smaller inductor helps to reduce the size of the converter. In addition, having a smaller inductor allows the inductor current to be changed faster. This allows the circuit to reach a new steady state sooner. Consequently, transient specs can be met with less output capacitance, which further reduces size of the converter.

Another benefit of high frequency operation is that it shortens the maximum response delay time (interval I_2). Consequently, a high switching frequency results in a smaller

peak voltage drop during I_2. Again, this helps in reducing the size of the output capacitor, and thus, the size of the whole module.

Operating at a high switching frequency makes it possible for the feedback loop to have a high bandwidth. The benefits of a high bandwidth control loop and a small inductor, both results of operating at a high switching frequency, are felt during the interval I_3 where both help to minimize ΔV_5 (see (3.14) and (3.27)).

In short, a higher switching frequency allows the designer to reduce the size of both the buck inductor and the output capacitors and increase the bandwidth of the control loop. As a result, the overall size of the VRM is significantly reduced. On the down side, however, operating at a high switching frequency will lower the efficiency of the converter and require advanced packaging techniques.

3.4 VRM Design Philosophy

Based on the discussion in this chapter, a new VRM design philosophy will be adopted here. The central idea is to make the module as small and compact as possible. Thus, we want to minimize the board area and achieve a low module profile by eliminating electrolytic capacitors (or any other through-hole parts) from the design. In addition, the goal is to keep the cost of the module as low as possible.

In light of the outlined goals, the switching frequency will be pushed as high as the efficiency specs will allow in order to minimize the size of the module. In order to keep the cost at a minimum, a simple hard-switching buck topology with voltage mode control will be used. Every subsystem will be optimized for maximum performance at high frequency. Alternate topologies and more complicated control schemes will not be used unless the specs absolutely cannot be met with the simplest topology and control method.

Clearly, VRM design philosophy is to push simple topologies and algorithms to their technological limit. Therefore, the chosen buck topology and the chosen voltage mode control algorithm have to be carefully analyzed in order to identify efficiency bottlenecks and find a way to squeeze every bit of efficiency out of the circuit. In order to do this, the losses in the buck topology are carefully analyzed in Chapter 4 as a function of the load current and the switching frequency. Loss equations derived in Chapter 4 are used in Chapter 5 to choose the right topology for VRM boards operating from a 5V input. The conclusions drawn in Chapter 5 are then used in Chapter 6 to optimize the operation and efficiency of a synchronous buck topology designed to operate from a 12V input. The optimization of the transient response of a voltage mode controlled buck converter is undertaken in Chapter 7.

Chapter 4

Overview of Loss Mechanisms in the Buck Topology in Continuous Conduction Mode

In line with the adopted VRM design philosophy, it is important to accurately predict all the losses in the buck topology as a function of the switching frequency and the load current. An accurate loss analysis can be used to optimize the VRM module.

The accuracy of loss calculations will depend on the ability to identify all loss mechanisms in the circuit and model them correctly. Because of high frequency operation, this task needs to be approached with great care so that no high frequency parasitics get overlooked.

4.1 Overview of Various Loss Mechanisms in the Regular Buck Topology

The regular buck topology including loss-causing parasitics is shown in Fig. 4.1. As shown in Fig. 4.1, the following loss mechanisms can be identified in the regular buck topology:

- Main Switch (Q_1)
  - Conduction Loss
  - Switching Loss
  - Drain to Source Capacitance Loss

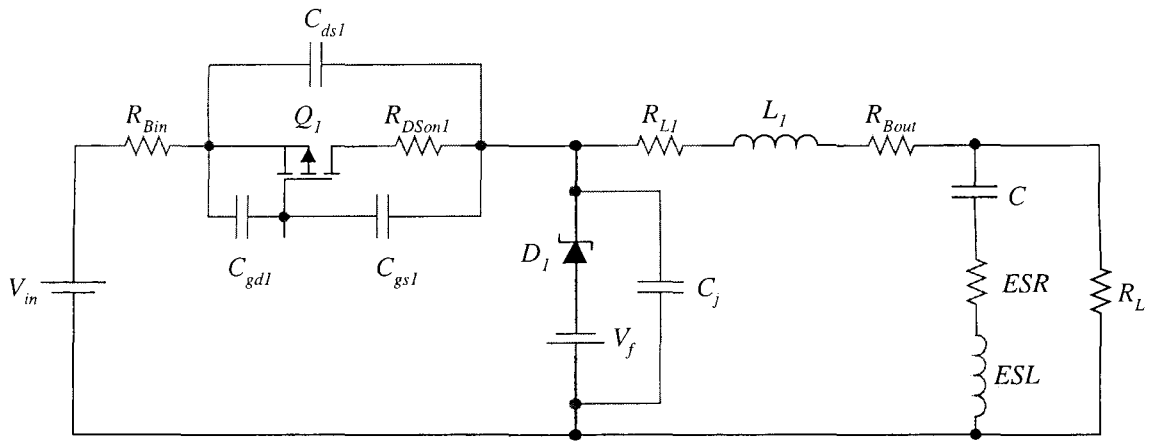


Figure 4.1: Regular buck converter including parasitics

- Gate Drive Loss

- Schottky Diode (D_1)
  - Conduction Loss
  - Reverse Bias Leakage Loss
  - Junction Capacitance Loss
- Inductor
  - Copper Loss
  - Core Loss
- Resistive Losses on the Circuit Board
  - Input Trace
  - Output Trace
  - Other Traces

4.1.1 Losses in the main switch (S_1)

As it was pointed out, the main switch will suffer from conduction loss, switching loss, drain-to-source capacitance loss, and gate drive loss. Conduction loss in the main switch, P_{c1}, can be expressed as:

$$P_{c1} = \frac{R_{DSon1}(T)}{N_{m1}} \cdot I_{Lrms}^2 \cdot D \tag{4.1}$$

where R_{DSon1} is the drain to source on resistance of the main switch, N_{m1} is the number of MOSFETs used in parallel, I_{Lrms} is the inductor rms current, and D is the duty cycle. The inductor *rms* current can be calculated using the following formula:

$$I_{Lrms} = \sqrt{I_o^2 + \frac{(\Delta I_L)^2}{12}} \tag{4.2}$$

The switching loss, sometimes called the overlap loss, is caused by the nonideality of the MOSFET. If there are no soft-switching techniques being applied, which is the assumption here, the MOSFET will, both turn-on and turn-off, briefly conduct the full on-current while the voltage across the drain and source terminals is still the full off-voltage of the switch (see Fig. 4.2). This produces significant switching (overlap) losses whenever the MOSFET turns on or off, especially at high switching frequencies.

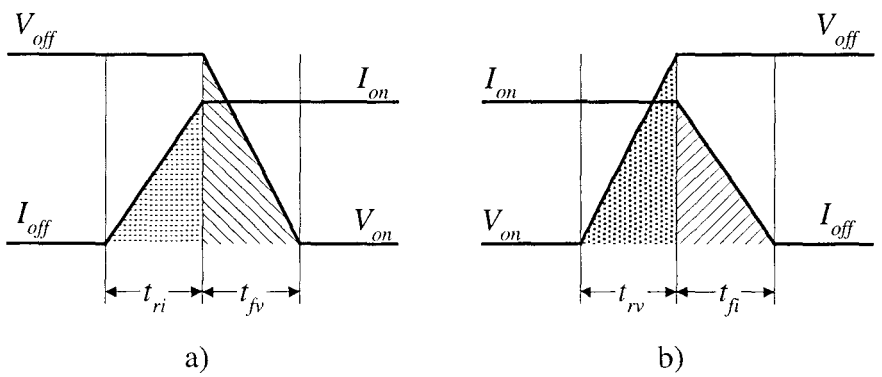


Figure 4.2: Switch voltage and current waveforms at a) turn-on, b) turn-off

From Fig. 4.2 we can derive expressions for the turn-on switching loss, P_{son1}, and turn-off switching, P_{soff1}. The turn-on switching loss is given by:

$$P_{son1} = \tfrac{1}{2} \cdot V_{in} \cdot \left(I_{out} - \frac{\Delta I_{out}}{2} \right) \cdot \left(t_{fv1} + t_{ri1} \right) \cdot f_s \tag{4.3}$$

while the turn-off switching loss is given by:

$$P_{soff1} = \tfrac{1}{2} \cdot V_{in} \cdot \left(I_{out} + \frac{\Delta I_{out}}{2} \right) \cdot \left(t_{rv1} + t_{fi1} \right) \cdot f_s \tag{4.4}$$

where f_s is the switching frequency, ΔI_{out} is the inductor current ripple, t_{rv1} and t_{fv1} are the switch voltage rise and fall times, respectively, and t_{ri1} and t_{fi1} and the switch current rise and fall times, respectively. The total switching loss, Ps1, is then:

$$P_{s1} = P_{soff1} + P_{son1} \tag{4.5}$$

Each time the MOSFET switch is turned on, the voltage across the drain and source terminals drops from V_{off} to V_{on} (see Fig. 4.2). Thus, the drain-to-source capacitance of the MOSFET is discharged in a lossy manner through its R_{DSon}. This lossy discharge of the drain-to-source capacitance has been termed drain-to-source capacitance loss, P_{DSc1}, and can be approximated using the following formula:

$$P_{DSc1} = \frac{1}{2} \cdot C_{DS1} \cdot V_{in}^2 \cdot f_s \cdot N_{m1} \tag{4.6}$$

where C_{DS1} is the drain-to-source capacitance of the main switch.

The gate drive loss is caused by the charging and discharging of C_{GS1} and C_{GD1} (see Fig. 4.1) each time the MOSFET is turned on or off. While the gate drive loss can be calculated using C_{GS1} and C_{GD1}, it is much easier to use the total gate charge needed to turn the FET on provided in the manufacturer's data sheet. In this case the gate drive loss can be expressed as:

$$P_{G1} = V_{GS1} \cdot Q_{G1} \cdot f_s \cdot N_{m1} \tag{4.7}$$

where V_{GS1} is the applied gate-to-source voltage, and Q_{G1} is the total gate charge that needs to be supplied by the gate driver in order to make the gate-to-source voltage equal to V_{GS1}.

The total loss in the main switch of the regular buck topology can be expressed as:

$$P_{Q1} = P_{c1} + P_{s1} + P_{DSc1} + P_{G1} \tag{4.8}$$

The expression for each of these loss components is given by (4.1) through (4.7).

4.1.2 Loss Mechanisms in the Schottky Diode

The chief loss mechanisms in the Schottky are the conduction loss, the loss due to the reverse bias leakage current, and the loss due to the charging and discharging of the junction capacitance. The conduction loss is given by:

$$P_{cdr} = V_{fr}(T) \cdot I_{out} \cdot D' \tag{4.9}$$

where V_{fr} is the forward voltage drop on the Schottky diode. The loss due to the reverse bias leakage current is:

$$P_{ldr} = V_{in} \cdot I_{sr}(T) \cdot D \cdot N_d \tag{4.10}$$

where I_{sr} is the reverse bias leakage current of the Schottky, and N_d is the number of diodes used in parallel. The loss due to the junction capacitance can be expressed as:

$$P_{Cj} = \frac{1}{2} \cdot C_j \cdot V_{in}^2 \cdot f_s \tag{4.11}$$

where C_j is the Schottky diode junction capacitance. The total loss in the Schottky diode is now:

$$P_{Sd} = P_{cdr} + P_{ldr} + P_{Cj} \tag{4.12}$$

4.2 Overview of the Losses in the Synchronous Buck Topology

The synchronous buck topology including loss-causing parasitics is shown in Fig. 4.3.

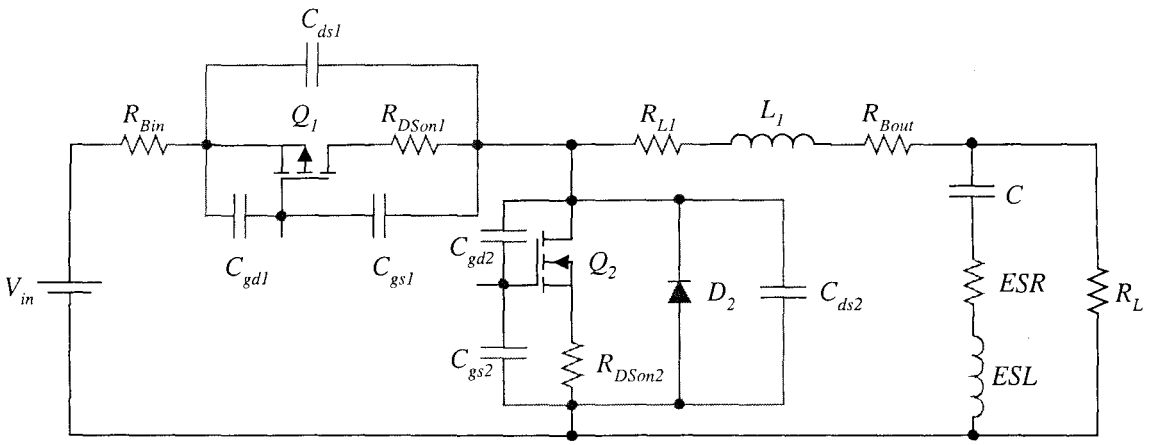


Figure 4.3: Synchronous buck topology including parasitics

As shown in Fig. 4.3, the following loss mechanisms can be identified in the synchronous buck topology:

- Main Switch (Q_1)
  - Conduction Loss
  - Switching Loss
  - Drain to Source Capacitance Loss
  - Gate Drive Loss
- Synchronous Rectifier (Q_2)
  - Conduction Loss
  - Switching Loss
  - Body Diode Loss
    - Conduction Loss
    - Reverse Recovery Loss
  - Gate Drive Loss
- Inductor

- Copper Loss
- Core Loss

- Resistive Losses on the Circuit Board
  - Input Trace
  - Output Trace
  - Other Traces

4.2.1 Loss Mechanisms in the Main Switch

The losses in the main switch can, in the first approximation, be assumed to be identical to those in the main switch of the regular buck. Thus, (4.1) through (4.8) can readily be applied, and will not be repeated here. Certain fine points concerning the difference in losses in the main switch of the regular and the synchronous buck will be discussed in more detail in later sections.

4.2.2 Loss Mechanisms in a Synchronous Switch

In order to accurately evaluate the losses in the synchronous rectifier as a function of frequency, we must take into account conduction loss, switching loss, gate drive loss, body diode conduction (dead time) loss, and the body diode reverse recovery loss. Conduction loss is given by:

$$P_{c2} = \frac{R_{DSon2}(T)}{N_{m2}} \cdot I_{Lrms}^2 \cdot D' \tag{4.13}$$

where R_{DSon2} is the drain to source on resistance of the synchronous switch, and N_{m2} is the number of MOSFETs used in parallel. The switching loss consists of the switching loss at Q_2 turn on:

$$P_{son2} = \tfrac{1}{2} \cdot V_f \cdot \left(I_{out} + \frac{\Delta I_{out}}{2} \right) \cdot \left(t_{fv2} + t_{ri2} \right) \cdot f_s \tag{4.14}$$

and at Q_2 turn off:

$$P_{soff2} = \tfrac{1}{2} \cdot V_f \cdot \left(I_{out} - \frac{\Delta I_{out}}{2} \right) \cdot \left(t_{rv2} + t_{fi2} \right) \cdot f_s \tag{4.15}$$

where V_f is the forward voltage drop of the body diode, f_s is the switching frequency, ΔI_{out} is the inductor current ripple, t_{rv2} and t_{fv2} are the switch voltage rise and fall times, respectively, and t_{ri2} and t_{fi2} and the switch current rise and fall times, respectively. Hence, the total switching loss is given by:

$$P_{s2} = P_{son2} + P_{soff2} \tag{4.16}$$

The gate drive loss can be estimated from the following equation:

$$P_{G2} = V_{GS2} \cdot Q_{G2} \cdot f_s \cdot N_{m2} \tag{4.17}$$

where V_{GS2} is the drive voltage, and Q_{G2} is the total gate charge that needs to be supplied in order to turn the synchronous FET on. Next, we need to consider the losses associated with the body diode. Namely, the body diode will conduct during the dead time between the turn off of one MOSFET and the turn on of the other. The loss before Q_1 turns on is given by:

$$P_{cbd1} = V_f \cdot \left(I_{out} - \frac{\Delta I_{out}}{2} \right) \cdot \frac{t_{d1}}{T_s} \tag{4.18}$$

while the loss before Q_2 turn on is given by:

$$P_{cbd2} = V_f \cdot \left(I_{out} + \frac{\Delta I_{out}}{2} \right) \cdot \frac{t_{d2}}{T_s} \tag{4.19}$$

where t_{d1} and t_{d2} are the dead time intervals before Q_1 and Q_2 turn on, respectively, and T_s is the switching period. Finally, the loss due to the reverse recovery of the body diode is:

$$P_{rr} = \frac{1}{2} \cdot I_{rr\max} \cdot t_b \cdot V_{in} \cdot f_s \tag{4.20}$$

where I_{rrmax} is the peak reverse recovery current, and t_b is the reverse recovery time. Hence, the total loss in the synchronous rectifier is obtained by summing all the losses characterized above.

$$P_{Q2} = P_{c2} + P_{s2} + P_{G2} + P_{cbd} + P_{rr} \tag{4.21}$$

Chapter 5

Synchronous Rectifiers Vs. Schottky Diodes in a Buck Topology for VRM Applications

5.1 Efficiency Considerations

The reasons for operating a VRM DC-DC converter at a high switching frequency were thoroughly explained in previous sections. However, since most losses in a switching power supply are directly proportional to the switching frequency, increasing the switching frequency results in a lower overall module efficiency. But, by now it is clear that some efficiency will have to be sacrificed in order to meet the transient response requirements in the smallest volume.

The regular and the synchronous buck topologies, shown in Figs. 5.1(a) and 5.1(b), respectively, are identical in every respect except in the implementation of the slave switch. A low voltage regular buck uses a Schottky diode (D) as a slave switch. In a synchronous buck, the Schottky diode is replaced by an active switch, a low on-resistance (R_{Dson}) MOSFET, commonly referred to as a synchronous rectifier (SR).

In conventional low frequency power supply designs, the low R_{DSon} of the MOSFET yields a considerable reduction in the conduction loss in comparison with the fixed voltage drop across any diode, even a low voltage Schottky. Thus, MOSFETs are

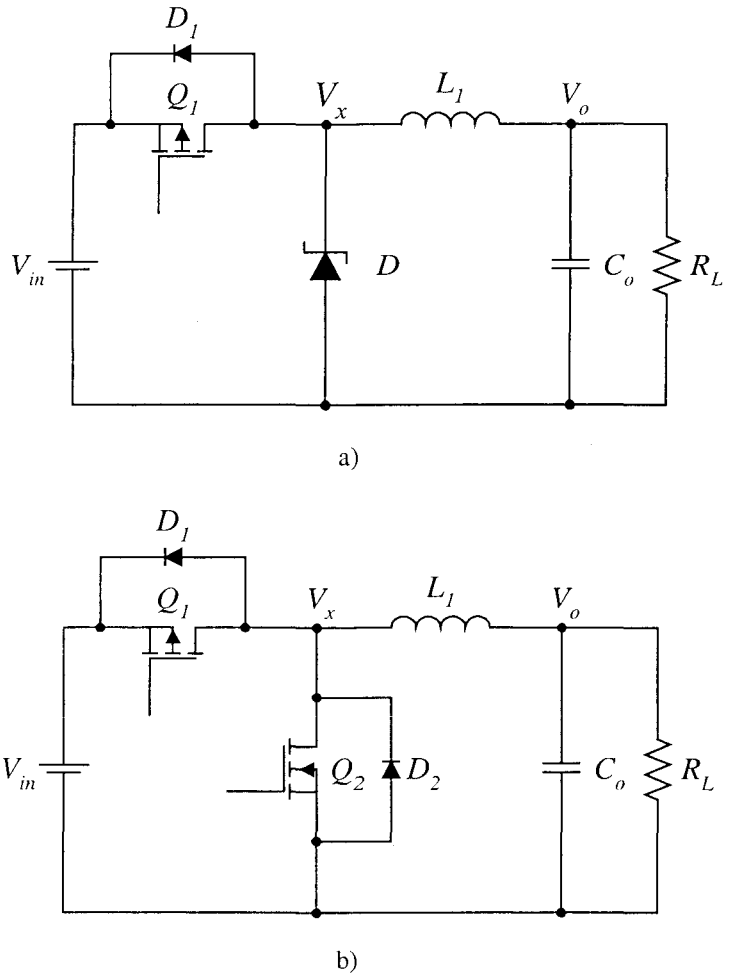


Figure 5.1: a) Regular buck; b) Synchronous buck

commonly used in place of diodes in order to improve the efficiency of switching converters. However, as it was explained earlier, the nature of the application these topologies are being considered for dictates moderately high switching frequencies.

As the switching frequency is raised, the benefit of the SR's low R_{DSon} is diminished by the increase in its frequency dependent switching loss, gate drive loss, and body diode loss. In fact, it becomes conceivable that using synchronous rectifiers might not be beneficial at all due to the mentioned frequency dependent loss components.

Consequently, unusually demanding VRM specifications require the conventional wisdom to be reexamined on a case by case basis in order to arrive at an optimum design.

Since the regular and the synchronous buck are almost identical in size, optimizing the VRM in the two-dimensional size-efficiency plane means choosing the more efficient of the two topologies for a particular input voltage, output voltage, load current, and a chosen switching frequency. However, in order to choose the right topology, the efficiency of both the regular buck and the synchronous buck topology has to be accurately calculated over a wide range of load currents and switching frequencies. The results of efficiency calculations can then be compared and the more efficient topology can be chosen.

An accurate calculation of the overall circuit efficiency of both topologies is important in several ways: first, it determines which topology should be used in a particular application; second, it becomes a powerful design tool that can be used to optimize future VRMs ahead of time, thus eliminating much of the guesswork and many unnecessary redesign attempts; and third, it provides an accurate component level loss distribution that allows the designer to immediately identify the dominant loss mechanisms.

During the design process, the component level loss distribution is as important as the overall efficiency information. The component level loss distribution provides the information needed to properly design all the components and avoid exceeding the rated maximum power dissipation for a particular device package. In order to illustrate the importance of the last point, let us consider the following situation: A VRM needs to be designed for the following specifications:

- V_{in}=5V
- V_{out}=2.0V
- I_{out}=16A
- f_s=500kHz

Looking at these requirements, it is impossible to say how many SRs, in say an SO-8 package, will be needed in order not to exceed the typical maximum rated dissipation for the chosen package (1W). The component level loss distribution obtained from the efficiency calculations can answer this question by providing an estimate of the power dissipation in the SR. Based on this estimate, we can determine the number of devices that need to be paralleled in order to achieve a reasonable design. This information, in turn, leads to a better system level efficiency prediction because the frequency dependent SR losses can be accurately taken into account for the proper number of devices. As a result, a fair comparison with the competing regular buck topology can be achieved.

5.1.1 Overview of Previously Published Work

Numerous attempts have been made in literature to compare the performance of synchronous rectifiers and Schottky diodes, primarily in the forward topology. The efficiency of Schottky diodes as opposed to synchronous rectifiers in various forward topologies has been discussed as a function of the output current and temperature [1], [2], and as a function of the input voltage [3] at frequencies below 500 kHz. Some authors examined the benefits of replacing Schottky diodes with resonant synchronous rectifiers at frequencies up to 20MHz [4].

By comparison, very few authors have weighed the advantages and the disadvantages of using a synchronous rectifier instead of a Schottky diode in a compact, high

performance, high efficiency, high power density, and high current buck converter. An effort was made to address this issue in [5]. In [5], the author compares the performance of an HDTMOS MOSFET used as a SR and a Schottky diode in a 5V to 3.3V buck converter. However, this discussion is limited to output currents below 3A and a single operating frequency (not mentioned). Therefore, [5] fails to address the both the load current range and the frequency dependent module size issues present in VRM design.

5.1.2 Schottky Diode Vs. Synchronous Rectifier

The focus of this chapter is a VRM candidate buck topology with a 5V input and a 3.1V output (@10-12A) capable of responding to output current steps with a slew rate faster than 35A/μs while maintaining a tight output voltage regulation of ±5% (see Table 2.1). Fast transient response, low cost, and small size requirements dictate a moderately high frequency operation in the megahertz range, while still maintaining high efficiency at full load. Obviously, the tradeoff between the performance, the size, and the cost has to be considered in order to achieve an optimized design.

The performance comparison between a Schottky diode and an SR was motivated by the Pentium® Pro specs given in Table 2.1. However, anticipating future processor core voltage reduction, the analysis in this chapter is extended beyond the current specs, and seeks to offer a comprehensive analysis of buck regulators operating from a 5V input. Therefore, the performance of a Schottky is compared to the performance of an SR for output voltages between 1.8V and 3.3V and load currents up to 12A.

Since the regular and the synchronous buck are identical in every respect except for the bottom switch (when operated in the continuous conduction mode, CCM), any difference in the overall circuit efficiency must be caused by bottom switch. Therefore,

in order to determine which topology is more efficient, it is sufficient to accurately account for all the losses in the switches as a function of the switching frequency and the output current and compare the results. Still, it is beneficial to go one step further and accurately account for all the losses in the circuit in order to estimate the overall circuit efficiency and make sure that the module can meet efficiency specs.

The following assumptions were made in the loss calculations:

- V_{in}=5V.
- V_{out}=1.8-3.3V.
- The top switch (Q_1) is a P-channel MOSFET identical in both the regular and the synchronous buck topology (R_{DSon}=29mΩ and Q_g=22.5nC @ V_{gs}=5V).
- The bottom switch in the regular buck (D) is a low voltage Schottky diode (V_f=0.3V @ 3.0Apk T_j=75°C, $I_{F(AV)max}$=3A).
- The synchronous rectifier (Q_2) is an N-channel MOSFET (R_{DSon}=18mΩ and Q_g=22.5nC).
- The output filter is same in both topologies.
- Switching times for the P-channel MOSFET are t_r=20ns, t_f=30ns; switching times for the N-channel MOSFET are t_r=15ns, t_f=30ns (based on previous experience and MOSFET data sheets).
- The dead-time in the synchronous buck is 60ns (from the IC controller data sheet).
- The ratio between the average current and the rated current for the MOSFETs and the Schottky diode was greater than 0.5 and 0.6, respectively.

5.1.2.A Loss Evaluation in the Switches

As previously discussed, the total loss in the top switch, Q_1, is virtually the same in both topologies, and is given by (4.8). The total loss in the Schottky diode and the SR is given by (4.12) and (4.21), respectively. Combining (4.8) and (4.12) yields an expression for the combined loss in the regular buck switches, P_r:

$$P_r = P_{Q_1} + P_{Sd} \tag{5.1}$$

Similarly, from (4.8) and (4.21) the combined loss in the synchronous buck switches, P_s, can be written as:

$$P_s = P_{Q_1} + P_{Q_2} \tag{5.2}$$

Equations (5.1) and (5.2) were used to plot P_r and P_s as a function of the switching frequency with the load current as a parameter. The results are shown in Fig. 5.2. Note that in Figs. 5.2-5.4, the first subscript (i) denotes the switching frequency, the second subscript (j) denotes the output current, and the third subscript (k) denotes the number of paralleled MOSFETs for both the main switch and the synchronous rectifier.

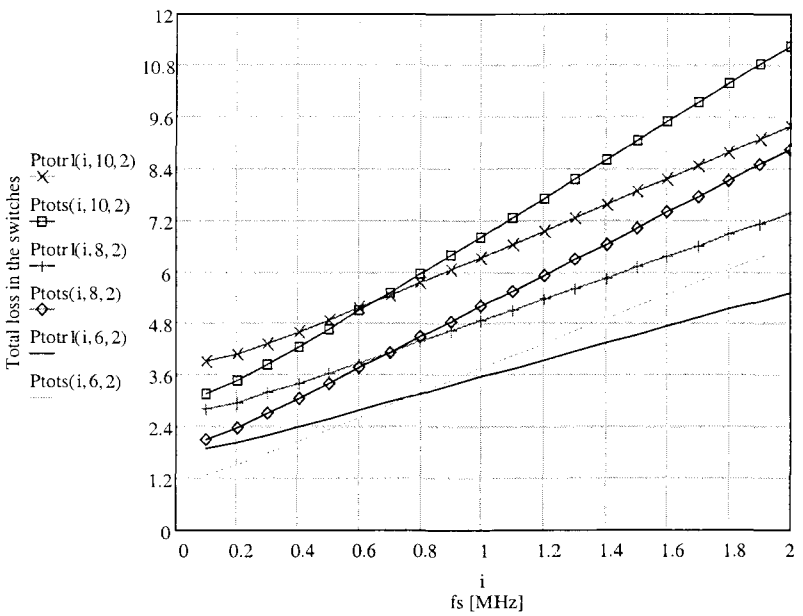


Figure 5.2: Combined loss in the switches for the regular and the synchronous buck topologies as a function of the switching frequency for I_{out}=10A, 8A, and 6A (V_{in}=5.0V, V_{out}=3.0)

As one can see from Fig. 5.2, the synchronous rectifier cannot compete with the Schottky diode at higher load currents (I_o=10A) and switching frequencies above

700kHz. However, at I_o=6A, the synchronous rectifier will have superior performance at frequencies below 800kHz. Therefore, the Schottky--synchronous rectifier break-even point exhibits only a weak dependence on the load current due to a relatively high duty ratio and low on-resistance of Q_1. Still, Fig. 5.2 clearly shows that the Schottky diode will have lower losses than the synchronous rectifier in low voltage (3V), high current, high frequency applications.

5.1.2.B Overall Efficiency Calculation

The next step is to determine what kind of efficiency we can expect. The overall efficiency is calculated by taking into account, in addition to loss in the switches, all parasitic resistances in the circuit (copper traces and inductor windings) and the loss in the magnetics. The output inductor, L, is adjusted to maintain a constant output current ripple equal to 20% of the maximum load current at all frequencies. The overall efficiency of the circuit is plotted as a function of the switching frequency, f_s=0.1MHz-2MHz, for I_{out}=10A and 6A in Fig. 5.3.

Since all the losses except for the loss in the switches are, in the first approximation, the same, it is not surprising that Fig. 5.3 reinforces the conclusions drawn from Fig. 5.2. In addition, Fig. 5.3 shows that with a regular buck we can expect an efficiency better than 76% for I_{out}=10A and f_s=2MHz. This is about 3% better than what we can get with a synchronous rectifier and with additional cost for another active switch and a more complex controller.

The next step is to examine how these two topologies would behave over the full range of the output current for three different switching frequencies. The overall circuit efficiency is plotted as a function of the output current for f_s=1.5MHz, 0.9MHz, and

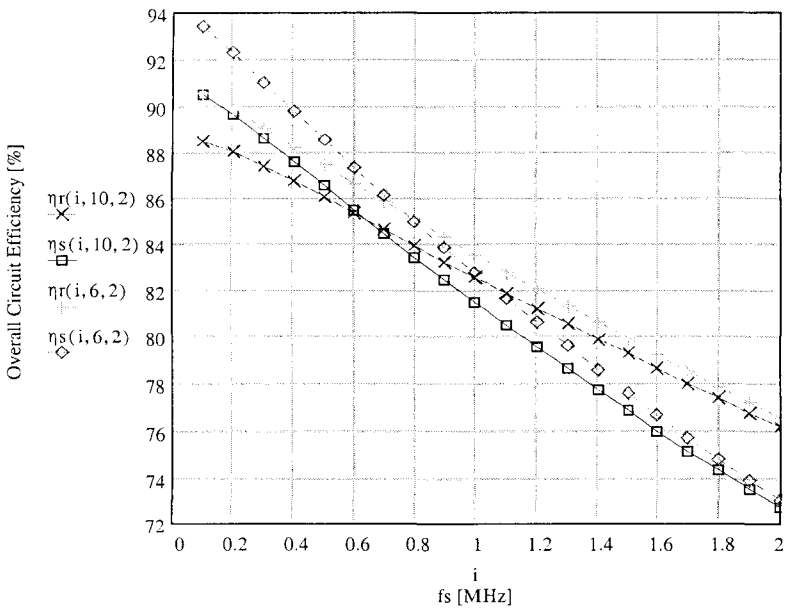


Figure 5.3: Overall efficiency of the circuits from Fig. 5.1 as a function of the switching frequency for I_{out}=10A and 6A (V_{in}=5V, V_{out}=3.0V).

500kHz in Fig. 5.4. At f_s=1.5MHz, the synchronous buck is less efficient than the regular buck, regardless of the load current. At I_o=10A, the regular buck has almost a 3% higher overall efficiency than the synchronous buck. And, even at f_s=600kHz, the regular buck will have a higher efficiency in applications requiring I_o≥9A.

Figs. 5.2 – 5.4 can be used to pick the more efficient 5V to 3.3V topology. Still, based on Figs. 5.2 – 5.4 one cannot outright say which topology will have a higher efficiency when the output voltage or the peak load current are changed. This ultimately depends on the particular choice of the input voltage, the output voltage, the output current, and component parameters. The results of this study do, however, show that for *any switching frequency* there is an output current for which the regular buck is the preferred topology. Similarly, for a particular current level, there is a switching frequency above which synchronous rectification would not be beneficial. For a 5V input

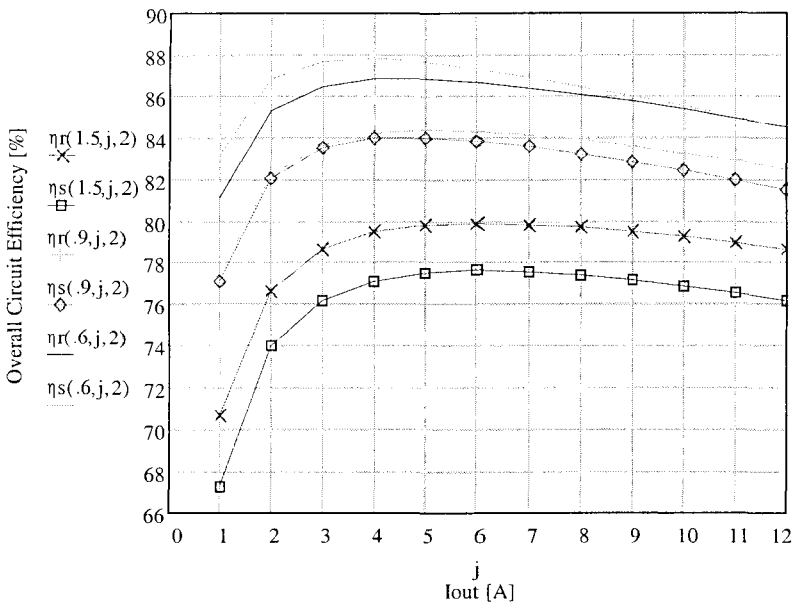


Figure 5.4: Overall efficiency of the circuit as a function of the load current for f_s=1.5MHz, 0.9MHz, and 0.5MHz at V_{in}=5V, V_{out}=3.0V

and a 3V output, the regular buck would definitely be the topology of choice if current levels above 6-8A are required.

5.1.2.C Loss Distribution

Figures 5.2-5.4 provide very useful system level efficiency trend information. However, the equations used to generate these plots can be used to calculate losses at the component level. This detailed loss distribution analysis allows us to detect the dominant loss mechanism in each circuit. Once the trouble spots have been pinpointed, steps can be undertaken to improve the overall efficiency of the circuit.

In order to gain further insight into the loss distribution as a function of the load current and the switching frequency, we generated Tables 5.1-5.6 which provide a detailed breakdown of the losses for the regular and the synchronous buck topology. The tables were created assuming that the input voltage is 5V, and that the output voltage is

2.5V. Two representative load current levels, 5A and 10A, and two representative switching frequencies, 440kHz and 850kHz, were chosen as the comparison basis.

Tables 5.1 – 5.3 show a breakdown of the losses for the regular buck. For convenience and easy comparison, the loss distribution for the synchronous buck, under identical operating conditions, is given in Tables 5.4 – 5.6.

Table 5.1 contains the loss breakdown for Q_1 of the regular buck. One can immediately observe that the switching loss, P_{sq1}, dominates even at 440kHz. In a hard-switched converter, P_{sq1} is directly proportional to the FET turn-on and turn-off times. These times are a function of the gate charge of the FET and the current capability of the gate driver. Thus, a better driver and a faster FET can significantly improve the overall efficiency of both topologies.

The loss distribution for the Schottky diode (D) is shown in Table 5.2. As is to be expected, the forward conduction loss, P_{cd}, is dominant. This loss depends on the duty ratio and the V_f of the diode. Since 0.3V Schottky diodes were used, no improvement can be achieved with the presently available device technology.

Table 5.3 compares the loss in Q_1 and D_1 with the total resistive loss (in the copper traces and the inductor series resistance), P_{res}, in the buck topology. It turns out that the resistive loss is almost 1W, and represents an unacceptably high percentage of the total loss. The resistive loss can be reduced by lowering the resistance of the board traces and the inductor windings. This will allow us to gain 1% - 2% in the overall efficiency. However, both topologies will benefit equally, so their relative performance will not be changed.

Table 5.4 shows the losses in Q_1 of the synchronous buck. Obviously, due to the reverse recovery of the body diode of Q_2, the losses in Q_1 of the synchronous buck will be slightly higher than those of the Q_1 of the regular buck (shown in Table 5.1). Otherwise, the discussion accompanying Table 5.1 readily applies.

Table 5.5 shows the loss distribution for the synchronous rectifier Q_2. It is interesting to note that the dominant losses in Q_2 are the conduction loss, P_{cq2}, and the body diode loss, P_{db} (includes reverse recovery and forward conduction losses). Table 5.5 points out that even at 440kHz, P_{db} is comparable, if not the larger of the two. The body diode losses become especially important at high frequency and high current (see f_s=850kHz, I_o=10A in Table 5.5).

Though presently available devices offer a very low R_{DSon}, we can only take advantage of it at lower frequencies and load currents. At higher operating frequencies, the required brief conduction of the body diode poses a serious limitation to application of synchronous rectifiers. Table 5.5 also shows that a FET with a lower body diode forward drop and a controller with a shorter dead time would extend the competitiveness of the synchronous rectifier to somewhat higher frequencies and load currents. However, the body (pn) diode reverse recovery will still be a major limitation. One could try to prevent the body diode from conducting appreciable current by placing a small Schottky in parallel with the synchronous rectifier. But, then, why use a synchronous rectifier at all? At frequencies and load currents of interest, for example, using three Schottky diodes instead of two synchronous rectifiers and a Schottky will be cheaper, more efficient, and the circuit will be less complex.

Finally, in Table 5.6 we have the loss distribution for the synchronous buck topology. One will notice that in Tables 5.3 and 5.6 the core loss has been omitted. Since both topologies are operating in the CCM, and with a small inductor current ripple, the core loss will be negligible in comparison with other losses, and can be omitted.

5.2 Experimental Verification

The experimental data was collected on a prototype buck converter. The prototype was designed so that it could be configured either as a regular buck or as a synchronous buck by simply replacing the Schottky diode with a MOSFET. In this way, both topologies are tested using the same board and the same devices, except for the bottom switch. Thus, a completely fair efficiency comparison between the two topologies is guaranteed.

The accuracy of our efficiency predictions was verified on the developed prototype operating at 440kHz and 850kHz for both topologies. The main switch (Q_1) was implemented using two P-channel MOSFETs with R_{DSon}=29mΩ and Q_g=22.5nC. For the regular buck diode we used three 3A Schottky diodes with a forward voltage drop of 0.3V. The synchronous rectifier was implemented using two N-channel MOSFETs with R_{DSon}=18mΩ and Q_g=22.5nC. The ratio between the average current and the rated current for the MOSFETs and the Schottky diode was greater than 0.5 and 0.6, respectively. Therefore, the performance comparison between the Schottky diode and the SR is absolutely fair.

Loss in Q_1 [W]	f_s=440kHz		f_s=850kHz	
	I_o=5A	I_o=10A	I_o=5A	I_o=10A
P_{cq1}	0.142	0.695	0.160	0.899
P_{sq1}	0.568	1.435	1.036	2.681
P_{gq1}	0.113	0.113	0.213	0.213
P_{q1} (tot)	0.823	2.243	1.408	3.792

Table 5.1: Loss distribution in Q_1 of the regular buck for V_o=2.5V

Loss in D_1 [W]	f_s=440kHz		f_s=850kHz	
	I_o=5A	I_o=10A	I_o=5A	I_o=10A
P_{cd}	0.548	1.159	0.501	1.043
P_{ld}	0.160	0.165	0.171	0.177
P_{cj}	$\sim 10^{-8}$	$\sim 10^{-8}$	$\sim 10^{-8}$	$\sim 10^{-8}$
P_d (tot)	0.708	1.324	0.672	1.220

Table 5.2: Loss distribution in D_1 of the regular buck for V_o=2.5V

Loss in regular Buck [W]	f_s=440kHz		f_s=850kHz	
	I_o=5A	I_o=10A	I_o=5A	I_o=10A
P_{q1}	0.445	0.450	1.408	3.792
P_d	0.708	1.324	0.672	1.220
P_{res}	0.237	0.961	0.237	0.961
P_{totr}	1.768	4.528	2.317	5.973

Table 5.3: Loss distribution in the regular buck for V_o=2.5V

Loss in Q_1 [W]	f_s=440kHz		f_s=850kHz	
	I_o=5A	I_o=10A	I_o=5A	I_o=10A
P_{cq1}	0.215	0.830	0.285	1.106
P_{sq1}	0.570	1.437	1.038	2.678
P_{gq1}	0.113	0.113	0.213	0.213
P_{q1} (tot)	0.898	2.380	1.536	3.997

Table 5.4: Loss distribution in Q_1 of the synchronous buck for V_o=2.5V

Loss in Q_2 [W]	f_s=440kHz		f_s=850kHz	
	I_o=5A	I_o=10A	I_o=5A	I_o=10A
P_{cq2}	0.096	0.416	0.100	0.489
P_{sq2}	0.033	0.118	0.060	0.220
P_{gq2}	0.113	0.113	0.213	0.213
P_{db}	0.135	0.297	0.255	0.561
P_{q2} (tot)	0.377	0.944	0.628	1.483

Table 5.5: Loss distribution in D_1 of the synchronous buck for V_o=2.5V

Loss in Sync. Buck [W]	f_s=440kHz		f_s=850kHz	
	I_o=5A	I_o=10A	I_o=5A	I_o=10A
P_{q1} (tot)	0.898	2.380	1.536	1.860
P_{q2} (tot)	0.377	0.944	0.628	1.483
P_r (tot)	0.235	0.952	0.235	0.952
P_{tots}	1.492	4.276	2.399	6.432

Table 5.6: Loss distribution in the synchronous buck for V_o=2.5V

In order to verify the accuracy of efficiency predictions, experimental efficiency data was collected for three values of the output voltage at two different switching

frequencies. The input voltage was kept at 5V, per Pentium® Pro spec; the three output voltages were chosen according to the current and anticipated future Pentium® Pro specs to be 3.0V, 2.5V, and 2.0V. Because of the VRM size requirements, two moderately high switching frequencies of 440kHz and 850kHz were chosen.

The predicted and the measured efficiency of the regular buck operating at 440kHz and 850kHz are shown in Figs. 5.5 and 5.6, respectively. The same information for the synchronous buck is presented in Figs. 5.7 and 5.8, respectively. Figs. 5.5 through 5.8 include the efficiency data for all three chosen input/output voltage combinations.

An excellent agreement between the calculated and the measured overall efficiency was obtained for load currents above 4A, which was the primary region of interest. At lower load currents, a rather large discrepancy of up to 5% can be observed between the predicted and the measured efficiency curve. It should be noted that the largest discrepancy occurs at the lowest output power level. At this low power level, a small absolute difference, on the order of a few tens of milliwatts, between the calculated and the measured loss, translates into a large relative error (on the order of several percent) in efficiency. While the discrepancy at the light load is larger than desired, it is encouraging that the efficiency has consistently been underestimated.

The experimental results presented in Figs. 5.5 through 5.8 clearly prove that the efficiency calculations accurately predict the circuit efficiency over a wide range of load currents and switching frequencies. The best accuracy is, at all frequencies, achieved in the medium to full load range (4A to 10A). At the light load (0A-4A), the efficiency prediction is overly pessimistic. Consequently, the formulas used to calculate the circuit

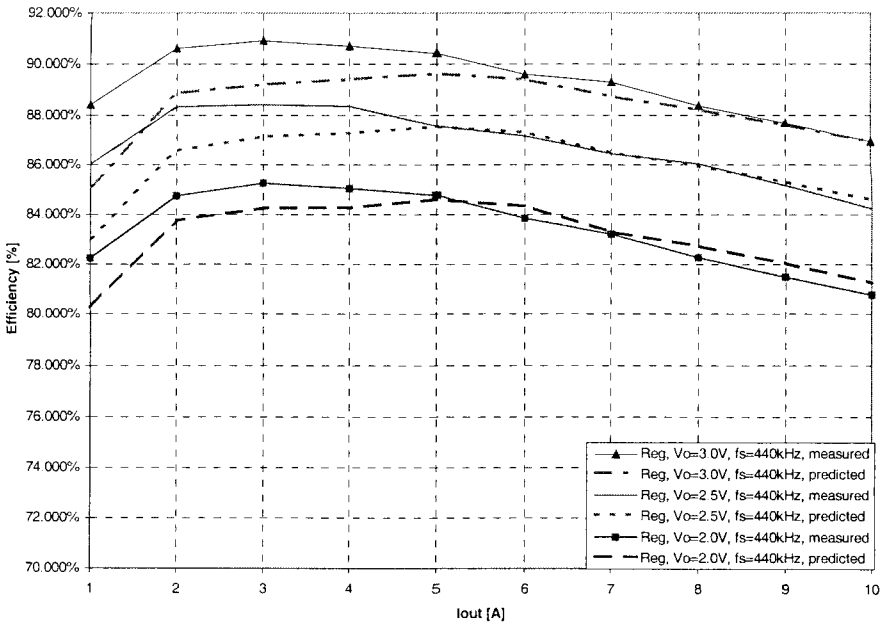


Figure 5.5: The predicted and the measured efficiency of the regular buck for V_{in}=5.0V, V_o=3.0V, 2.5V, and 2.0V, f_s=440kHz

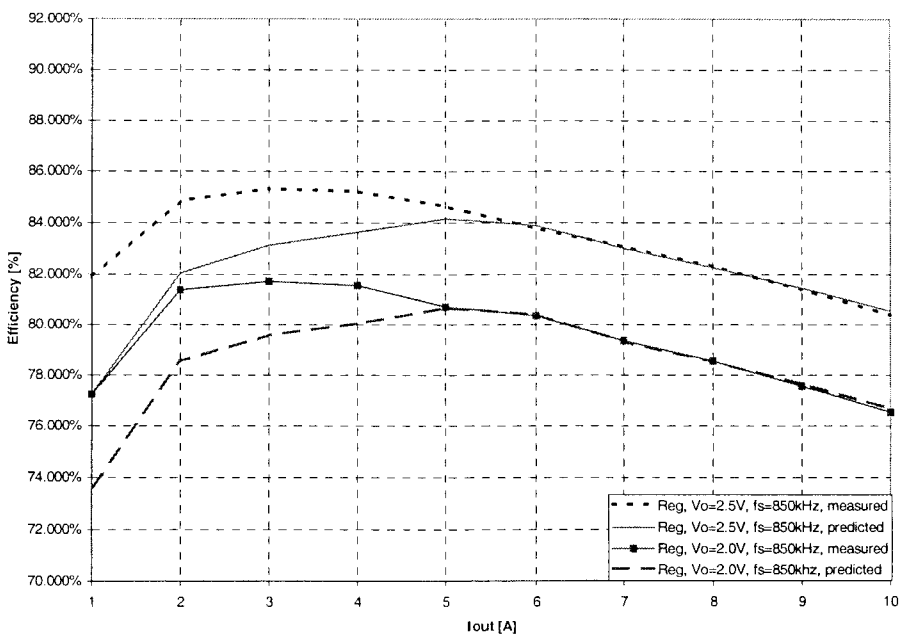


Figure 5.6: Predicted and measured efficiency of a regular buck for V_{in}=5.0V, V_o=2.5V, and 2.0V, f_s=850kHz

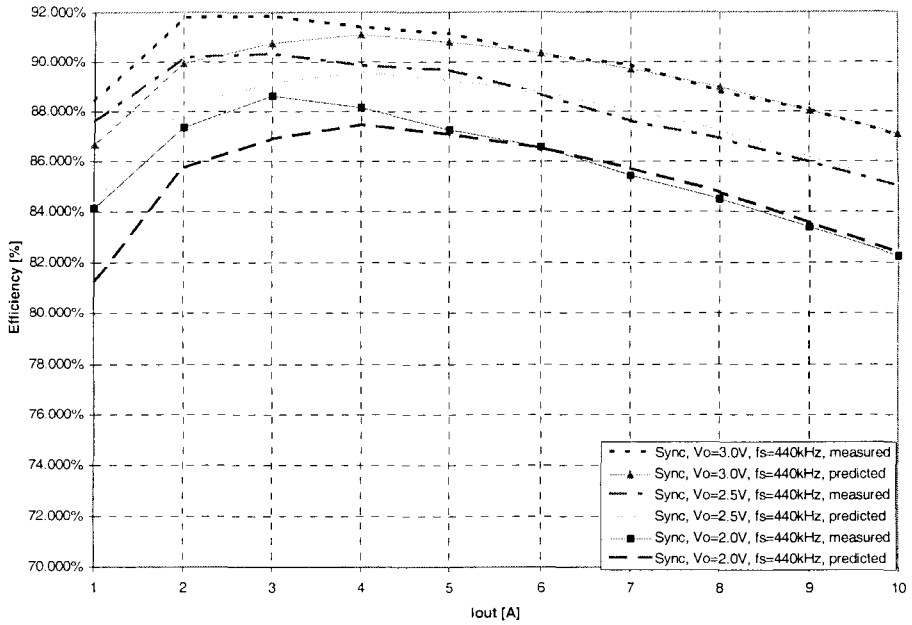


Figure 5.7: Predicted and measured efficiency of a synchronous buck for V_{in}=5.0V, V_o=3.0V, 2.5V, and 2.0V, f_s=440kHz

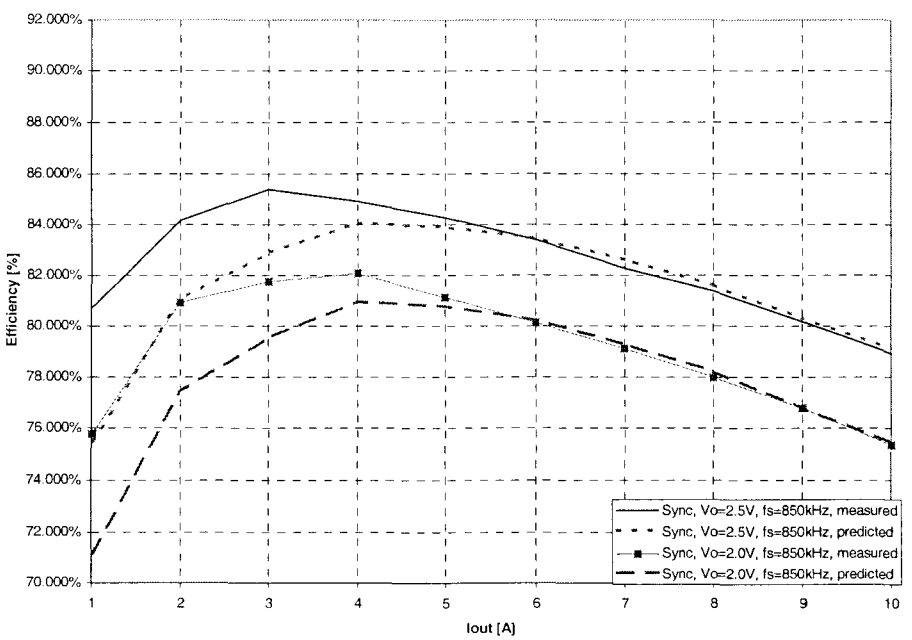


Figure 5.8: The predicted and the measured efficiency of a synchronous buck for V_{in}=5.0V, V_o=2.5V, and 2.0V, f_s=850kHz

efficiency can fully be trusted to accurately predict the circuit efficiency in future designs. As a result, these equations become a powerful optimization tool that should be used during the design process to optimize the VRM. Optimizing the circuit parameters ahead of time shortens the design-to-market time by eliminating unnecessary design iterations.

As it was pointed out in the preceding paragraphs, the first objective to create a trustworthy design tool has been accomplished. Now the attention can be turned back to the VRM at hand. The question which topology is best suited for the Pentium Pro application still hasn't been answered. However, all the information needed to answer this question has already been presented in Figs. 5.5 through 5.8. All that remains to be done is to slightly rearrange this information and draw appropriate conclusions.

Previously collected experimental efficiency data for the regular buck and the synchronous buck for V_{in}=5.0V, V_o=3.0V operating at 440kHz and 850kHz is combined in Fig. 5.9. The same information is presented for V_o=2.5V and V_o=2.0V in Figs. 5.10 and 5.11, respectively. Figs. 5.9 through 5.11 allow a clear and immediate efficiency comparison between the two topologies.

With the output voltage set at 3V (see Fig. 5.9), the duty ratio is above 60%. Since the second switch (D_1 or Q_2) conducts less then 40% of the time, the advantage of using a low on-resistance synchronous rectifier is negated by switching and gate drive losses even at 440kHz (see Fig. 5.9). Already at 850 kHz, the regular buck has over 2% higher efficiency at I_o=10A. Hence, the increased control circuit complexity and the overall cost of the synchronous buck topology cannot be justified for this input/output voltage

combination. In fact, based on Fig. 5.9, it is clear that the use of the synchronous rectifier cannot be justified for any output voltage above 3V.

Figure 5.10 shows the efficiency comparison between a regular buck and a synchronous for V_o=2.5V. As the output voltage migrates to lower levels, the on-time of the second switch increases, and it may make more sense to use the low on-resistance synchronous rectifier in place of a Schottky diode. However, at V_o=2.5V and f_s=440kHz, the synchronous solution still offers less than 1% higher efficiency at the maximum load current (see Fig. 5.10). The decision then has to be made whether the added circuit complexity and the higher cost are a price worth paying for a slight efficiency improvement. On the other hand, at the 2.5V output voltage setting and 850kHz switching frequency, the regular buck is still more efficient at the full load.

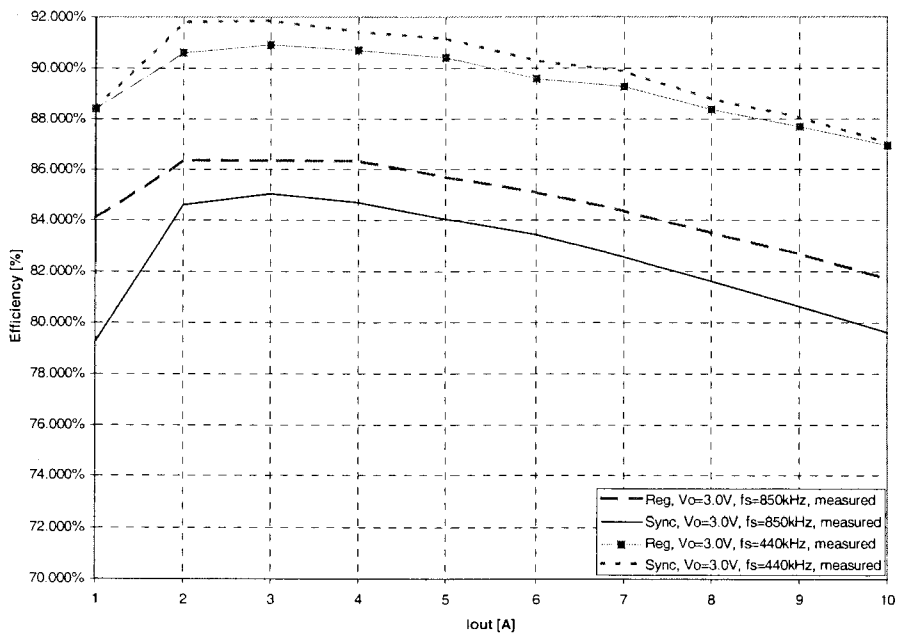


Figure 5.9: Efficiency comparison between a regular and a synchronous buck for V_{in}=5.0V, V_o=3.0V for f_s=440kHz and 850kHz

Figure 5.11 shows the efficiency comparison between a regular buck and a synchronous for V_o=2.0V. In this case, due to the small duty ratio of the main switch (about 40%), the synchronous topology is more efficient both at 440kHz, and at 850kHz. However, at frequencies above 850 kHz or at higher load currents, the regular buck will have a higher efficiency.

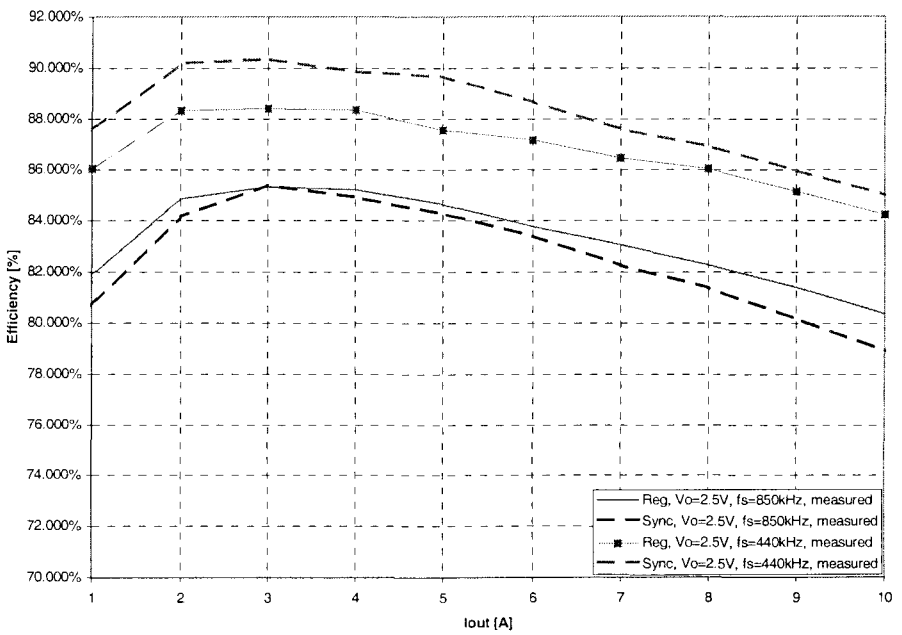


Figure 5.10: Efficiency comparison between a regular and a synchronous buck for V_{in}=5.0V, V_o=2.5V for f_s=440kHz and 850kHz

5.3 On the Accuracy of the Component Level Distribution

While Figs. 5.5–5.8 show that the overall circuit efficiency of both topologies has been accurate, no experimental evidence has as yet been presented to verify that the actual component level loss distribution can be trusted. Indeed, it would be very hard to separately accurately measure each loss component in the circuit. Part of the reason for this is that in order to make the measurement, sense resistor or current probes would have

to be inserted in the circuit. Insertion of either of these measurement aids would significantly alter the circuit, and void the validity of the measurement. Thus, direct experimental evidence of the component level distribution cannot be offered. However, the results in Figs. 5.5-5.8 offer indirect proof that the component level distribution given in Table 5.1-5.6 is, indeed, valid. Namely, it is conceivable that, for a given input voltage, output voltage, and switching frequency, certain losses in the circuit could have been overestimated, while others have been underestimated resulting in the correct overall circuit efficiency, but in an incorrect component level loss distribution. However, if this were the case, once the operating point was changed, this error would show up, and the overall circuit efficiency prediction would no longer closely match the measurement. Yet, Figs. 5.5-5.8 show that the overall circuit efficiency was accurately predicted over a wide range of load currents, for three different output voltages, and for two different switching frequencies. Thus, since the accuracy of the overall circuit efficiency was unaffected by the change in the operating point, Figs. 5.5 through 5.8 indirectly prove that the component level loss distribution given in Tables 5.1-5.6 must be accurate.

5.4 Conclusion

We have analyzed a regular and a synchronous buck topology for low voltage, high current applications. The analysis, and subsequent experimental verification, showed that, for a given input and output voltage, the regular buck always had higher efficiency for a certain combination of output current and switching frequency. However, it may not always be practical to operate at frequencies at which a diode will offer higher efficiency. It turns out that for a 5V input, with presently available device technology, it makes sense to use the regular buck for I_{out}>6A, f_s>850kHz, and D>0.5. Of course, as we

decrease D, the efficiency break-even point will move to higher frequency and/or current. For example, for D=0.4, the one would use a regular buck above 1.1MHz at 6A.

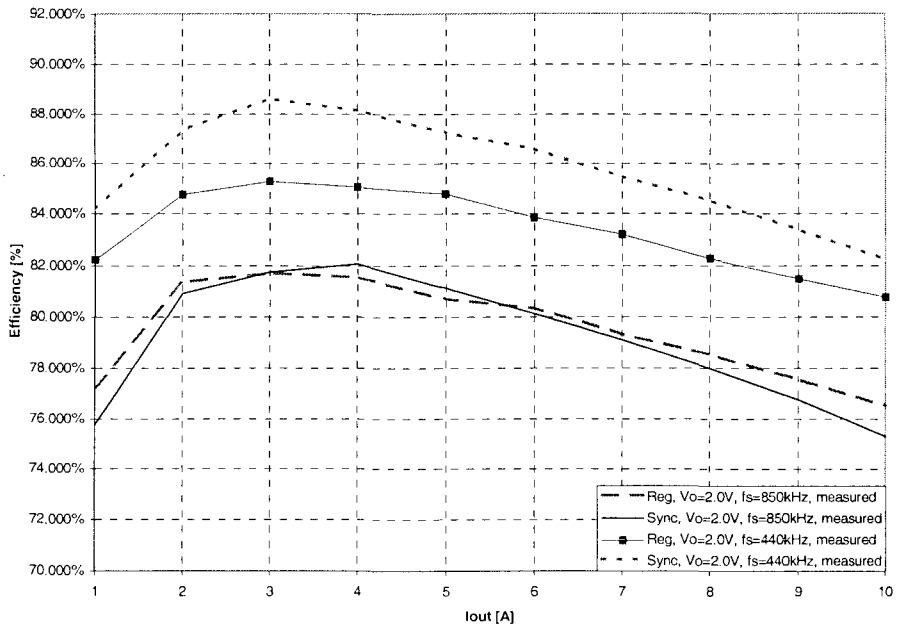


Figure 5.11: Efficiency comparison between a regular and a synchronous buck for V_{in}=5.0V, V_o=2.0V for f_s=440kHz and 850kHz

In the future, improved synchronous rectifiers could extend their competitiveness to higher frequencies and load currents. However, they face two inherent drawbacks when it comes to high frequency, high current operation: (pn) body diode and required dead time. These factors will ultimately impose a limit on the use of synchronous rectifiers at high frequencies and currents.

On the other hand, should the breakdown capability of the 15V Schottky diodes (unnecessary for 5V applications) be traded for somewhat lower forward drop, we could see the application of the regular buck shift to lower frequency and lower load current.

With present technology, higher efficiency and lower overall cost make the regular buck the topology of choice in 5V input, 1.8V-3.3V output voltage applications requiring high current, fast transient response, and small size.

Chapter 6

High Frequency Synchronous Buck VRM

In conventional low frequency designs, MOSFETs have been used in place of diodes in order to improve the efficiency of switching converters. However, small size requirements, encountered in computer systems and portable devices, call for higher switching frequencies. As the switching frequency is raised, the benefit of the low MOSFET on resistance (R_{DSon}) is diminished by the increase in the switching loss, the gate drive loss, and the body diode loss. In fact, as it was illustrated in Chapter 5, using synchronous rectifiers might not be beneficial at all. With this in mind, "Why bother with the synchronous buck at all?" becomes a legitimate question.

The answer to this question was already offered in Chapter 5. In Chapter 5, it was pointed out that a combination of four factors (the input voltage, the output voltage, the switching frequency, and the maximum load current) determines which topology, the regular or the synchronous buck, will be more efficient. Or, in other words, which topology will be more efficient depends on the duty cycle, the load current, and the switching frequency.

In Chapter 5 it was found that if the duty cycle is relatively high (greater than 60%), the regular buck is more efficient; if, on the other hand, the duty cycle is relatively low

(less than 40%), the synchronous buck tends to be more efficient. Since in some applications the VRM has to operate from a relatively high input voltage (12V) and produce a relatively low output voltage (1.8V to 3.3V), the synchronous buck VRM deserves to be carefully analyzed and optimized.

An optimized VRM is efficient, compact, inexpensive, and has good load transient response. The size and the load transient response requirements dictate a moderately high switching frequency. On the other hand, a high switching frequency inevitably reduces the overall circuit efficiency. Thus, a compromise between the size, the load transient response, and the efficiency needs to be found.

6.1 Overview of Previously Published Work

The obvious way to operate a converter efficiently at a high switching frequency is to minimize the losses proportional to the switching frequency by any means available. Examples of such attempts are found in literature. For instance, in order to deal with the switching loss in a buck topology operating at a high switching frequency, some authors have proposed an adaptive dead time control algorithm [6], variable frequency operation [7], and hybrid control [8]. All three proposed algorithms share a common shortcoming in the context of the VRM—they require fairly complex additional hardware, and thereby increase the overall size and cost of the converter. In addition, all three works concentrate on optimizing the dead time and the converter efficiency for load currents (I_{out}≤4A) three times smaller than required by the Pentium® Pro spec (I_{out}≤12A) given in Table 2.1.

6.2 Overview of the Proposed Approach

The philosophy advocated in this chapter is diametrically opposite to what was presented in the referenced works. Instead of *a priori* using cumbersome and expensive additional hardware and complicated control methods, we have chosen to use a simple, cost effective control algorithm and push it to the limit. Only when it is proven that this algorithm cannot meet the specifications with the presently available technology, only then does it become warranted for it to be discarded in favor of more complicated and more expensive algorithms.

The basic approach that will be used throughout this chapter is to use a very simple voltage mode control algorithm and push it to the limit. Therefore, we have chosen to operate with a fixed switching frequency in the megahertz range to maintain a small size while preserving high efficiency at full load. Furthermore, we have chosen to perform hard switching and keep dead time delays fixed. In order to minimize losses in the switches under these conditions, the gate drive circuit should reduce the body diode conduction time to a minimum while still avoiding cross conduction and achieving the fastest possible switching speed.

6.3 Existing Controllers

Based on component data sheets and the observed circuit operation, the loss distribution in a synchronous buck converter was accurately calculated in Chapter 5. The goal was to identify dominant loss mechanisms in order to understand what can be done to improve the design and optimize the synchronous buck topology for high frequency operation. The results of the loss distribution analysis were reported in Tables 5.3 through 5.6. Of particular interest at this time is Table 5.5 (reprinted here for

convenience as Table 6.1) which gives the loss distribution in the SR itself for the following circuit parameters and test conditions:

- V_{in}=5V.
- V_{out}=2.5V.
- The Top switch (Q_1) is a P-channel MOSFET (R_{DSon}=29mΩ and Q_g=22.5nC @ V_{gs}=5V).
- The synchronous rectifier (Q_2) is an N-channel MOSFET (R_{DSon}=18mΩ and Q_g=22.5nC @ V_{gs}=5V).
- Dead time for synchronous buck is 60ns (observed on the actual circuit).

Loss in Q_2 [W]	f_s=440kHz		f_s=850kHz	
	I_o=5A	I_o=10A	I_o=5A	I_o=10
P_{cq2}	0.096	0.416	0.100	0.489
P_{sq2}	0.033	0.118	0.060	0.220
P_{gq2}	0.113	0.113	0.213	0.213
P_{db}	0.135	0.297	0.255	0.561
P_{q2} (total)	0.377	0.944	0.628	1.483

Table 6.1: Loss distribution in Q_2 of the synchronous buck for V_{in}=5.0V, V_o=2.5V

From Table 6.1 we can immediately notice that body diode loss dominates at higher frequencies. In order to emphasize this point, the equations used to create Table 6.1 were used to plot the total loss in the SR, along with all of its loss components and the total loss in the Schottky diode Fig. 6.1 as a function of the load current for a switching frequency of 850kHz. In Fig. 6.2, we have plotted the SR loss distribution as a function of the switching frequency for a load current of 10A. In both cases, the loss in the body diode significantly contributes to the overall loss. Therefore, reducing body diode losses could significantly improve the overall circuit efficiency.

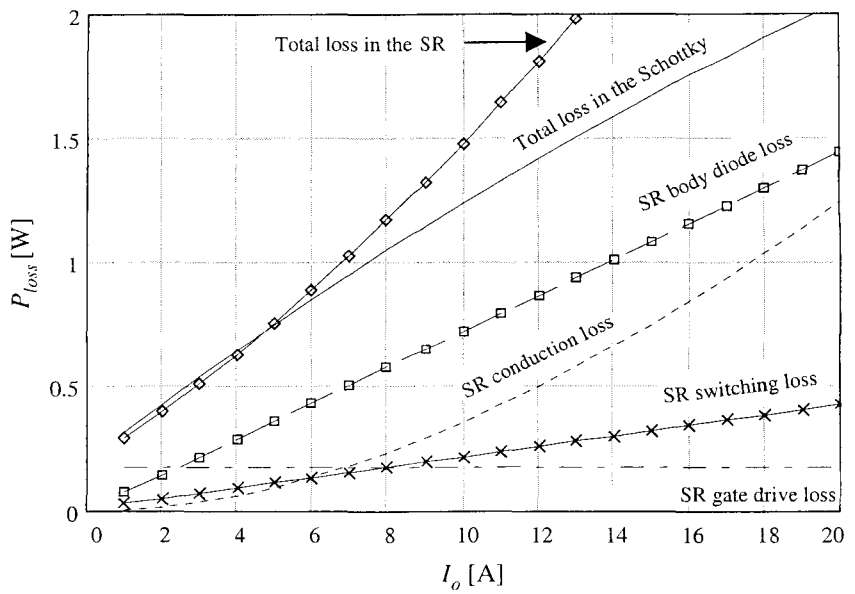


Figure 6.1: Loss distribution in the SR as a function of the load current for f_s=850kHz

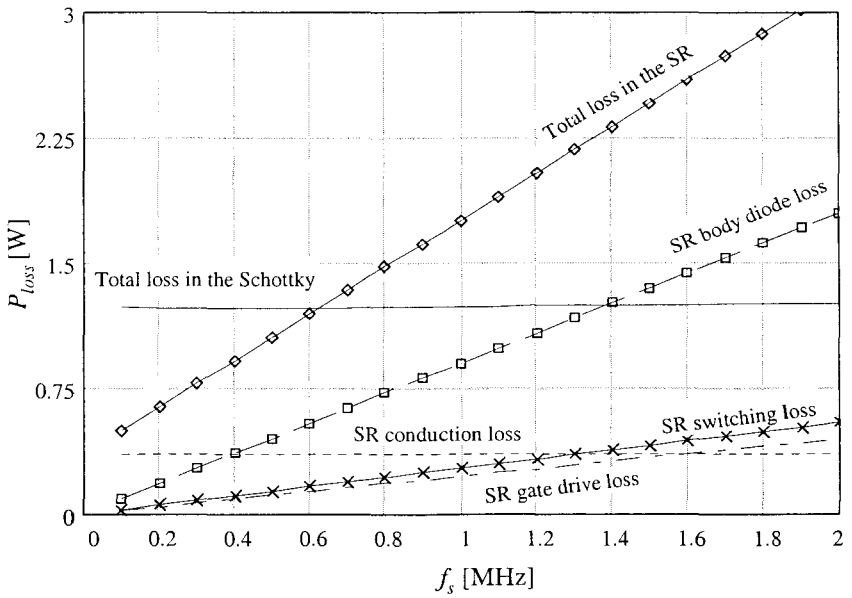


Figure 6.2: Loss distribution in the SR as a function of the switching frequency for I_o=10A

Extensive body diode losses encountered on the existing prototype called for a closer scrutiny of the gate drive signals being provided by the Siliconix Si9140 control IC being used. The Si9140 was chosen because of its performance characteristics, its ability to operate at switching frequencies above 1MHz, and its availability in the low profile, TSSOP-16, surface mount package.

Typical synchronous buck waveforms when operating at f_s=0.85MHz are presented in Figs. 6.3-6.5. The upper trace in Fig. 6.3 is the phase node voltage, while the lower two traces are the FET gate voltages. Looking at the phase node voltage (top trace in Fig. 6.3) we can immediately notice rather long body diode conduction periods (circled).

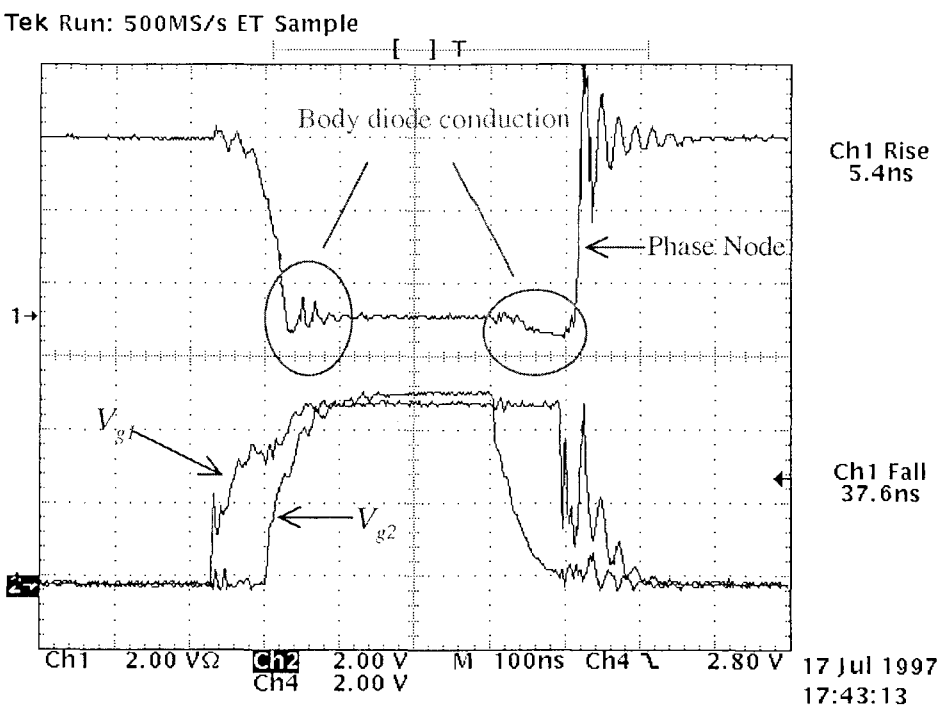


Figure 6.3: Typical Si9140DB waveforms (top to bottom): phase node, V_{g1}, and V_{g2}

Furthermore, displayed waveforms show that it takes ~37ns to turn off the main switch.

In order to examine these waveforms in more detail, we expanded the time scale of Fig. 6.3 to show the turn on and turn off transitions of Q_1 in Figs. 6.4 and 6.5, respectively. In Fig. 6.4, a 60ns dead time is clearly visible before the main switch turns on. Fig. 6.5 shows that the turn off time of Q_1 is ~40ns -- too slow for high frequency operation. It is also interesting to note that while the controller maintains a 70ns delay

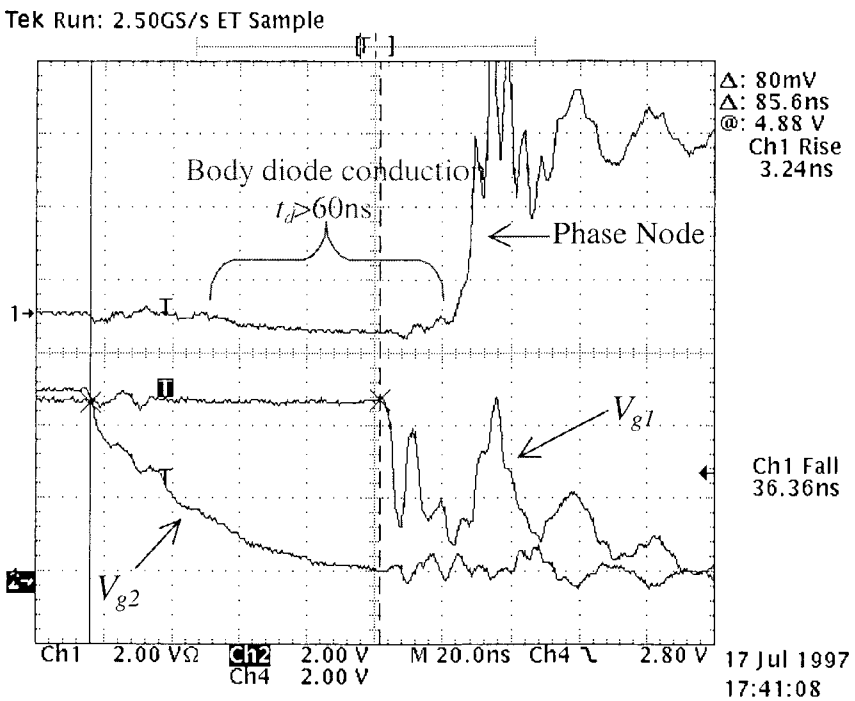


Figure 6.4: Si9140DB dead time before the main switch turns on; waveforms shown (top to bottom): phase node, V_{g1}, and V_{g2}

between initiating the turn off of Q_1 and initiating the turn on of Q_2 (see Fig. 6.4), this large dead time cannot be observed in the phase node waveform due to the very slow rise of V_{g1}. However, these waveforms were taken during light load operation to qualitatively demonstrate some of the salient features of circuit operation. At or near full load the circuit achieves the following:

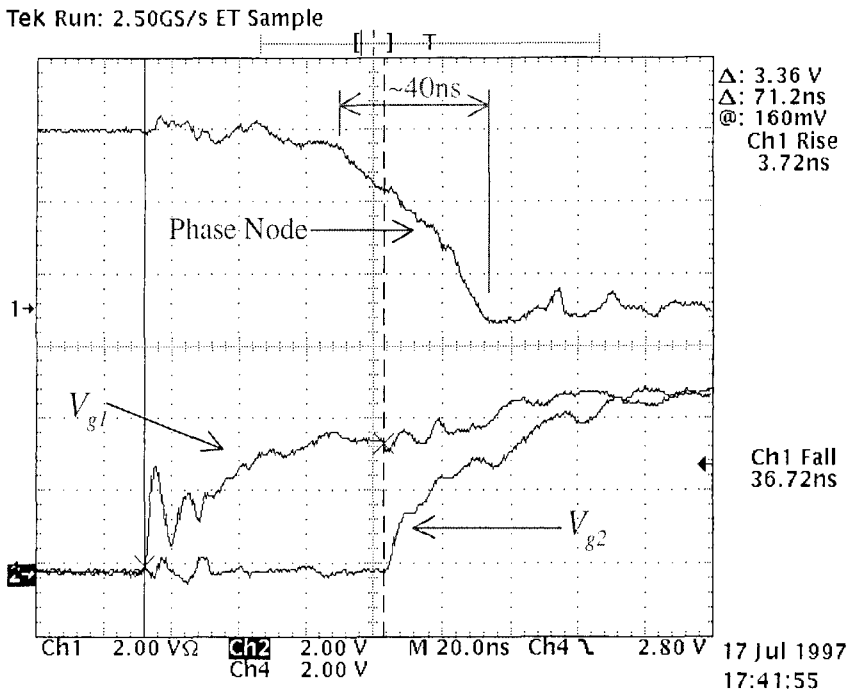


Figure 6.5: Si9140DB dead time before the SR turns on; waveforms shown (top to bottom): phase node, V_{g1}, and V_{g2}

- Switching times for Q_1 (P-channel MOSFET) are t_r=20ns, t_f=30ns.
- Switching times for Q_2 (N-channel MOSFET) are t_r=15ns, t_f=30ns.
- Dead time for synchronous buck is 60ns at phase node transitions.

Based on the waveforms presented in Figs. 6.3-6.5, it is clear that there are several modifications that can be made in order to improve overall circuit efficiency when the converter is operated with a fixed switching frequency:

1. Replace the P-channel main switch with a lower on resistance, faster N-channel MOSFET.
2. Improve the switching speed.
3. Reduce body diode conduction to a minimum.

If we can achieve a very fast switching time and very short (ideally zero) body diode conduction, we will have done the best we could with a fixed frequency, hard switched synchronous buck topology. Thus, we set out to calculate what is the best efficiency we could expect from a fully optimized, hard switched buck topology with a fixed dead time.

Because of the demand for VRM with a 12V input, in this chapter we will calculate the overall circuit efficiency of a synchronous buck converter shown in Fig. 6.6 as a function of the load current and the switching frequency with dead time as a parameter.

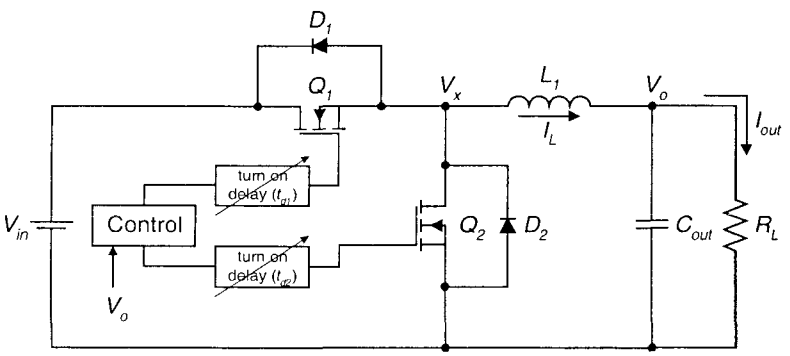


Figure 6.6: Synchronous buck converter with independent dead time control for both switches

The output voltage range of interest is between 1.8 and 3.3V, and the maximum load current is 12A. The goal is to predict the overall efficiency degradation due to the conduction of the synchronous rectifier (SR) body diode D_2, and calculate the maximum achievable overall circuit efficiency if these losses can be eliminated. Therefore, the SR losses are reviewed in Section 6.4, and various loss components and mechanisms are identified. Sections 6.5 and 6.6 discuss the efficiency degradation due to the SR body diode conduction before the main switch turns on for two possible modes of converter operation. The efficiency degradation due to the SR body diode conduction after the

main switch turns off is calculated in Section 6.7. Results from Sections 6.5, 6.6, and 6.7 are combined in Section 6.8 to show the full effect of the SR body diode conduction on the efficiency of a synchronous buck converter. Experimental results and conclusions are given in Sections 6.8 and 6.9, respectively.

6.4 Overview of the Synchronous Rectifier Loss

The loss in the synchronous rectifier can be expressed as:

$$P_{sr} = P_c + P_s + P_g + P_{BD} \tag{6.1}$$

where P_c is the conduction loss, P_s is the switching loss, P_g is the gate drive loss, and P_{BD} is the body diode loss. In (6.1), only P_{BD} is a function of the dead time. Since our goal is to determine the effect of dead time delays on the efficiency of a synchronous buck converter, we will concentrate on this loss component.

The gate drive, the inductor current, and the SR body diode current waveforms for the circuit in Fig. 6.6 are shown in Fig. 6.7. In every switching period, there are two dead time intervals, t_{d1} and t_{d2}. The first interval, t_{d1}, occurs at t_1 (see Fig. 6.7), when the SR turns off. Since the SR is a current bi-directional switch, the inductor current at t_1 can be either positive or negative with respect to the reference direction shown in Fig. 6.6 (see Figs. 6.7b and 6.7d). If $I_{out} \geq \frac{\Delta I_L}{2}$ the inductor current at t_1 will be positive (Fig. 6.7b), and the diode will turn on to provide a return path for the inductor current. We will call this mode of operation *mode 1*. If, on the other hand, $I_{out} < \frac{\Delta I_L}{2}$, the inductor current at t_1 will be negative (see Fig. 6.7d) and the diode will not turn on. Instead, the inductor current will charge and discharge the drain to source capacitance of the SR and the main switch, respectively, until the main switch turns on at t_2. We will call this mode of operation

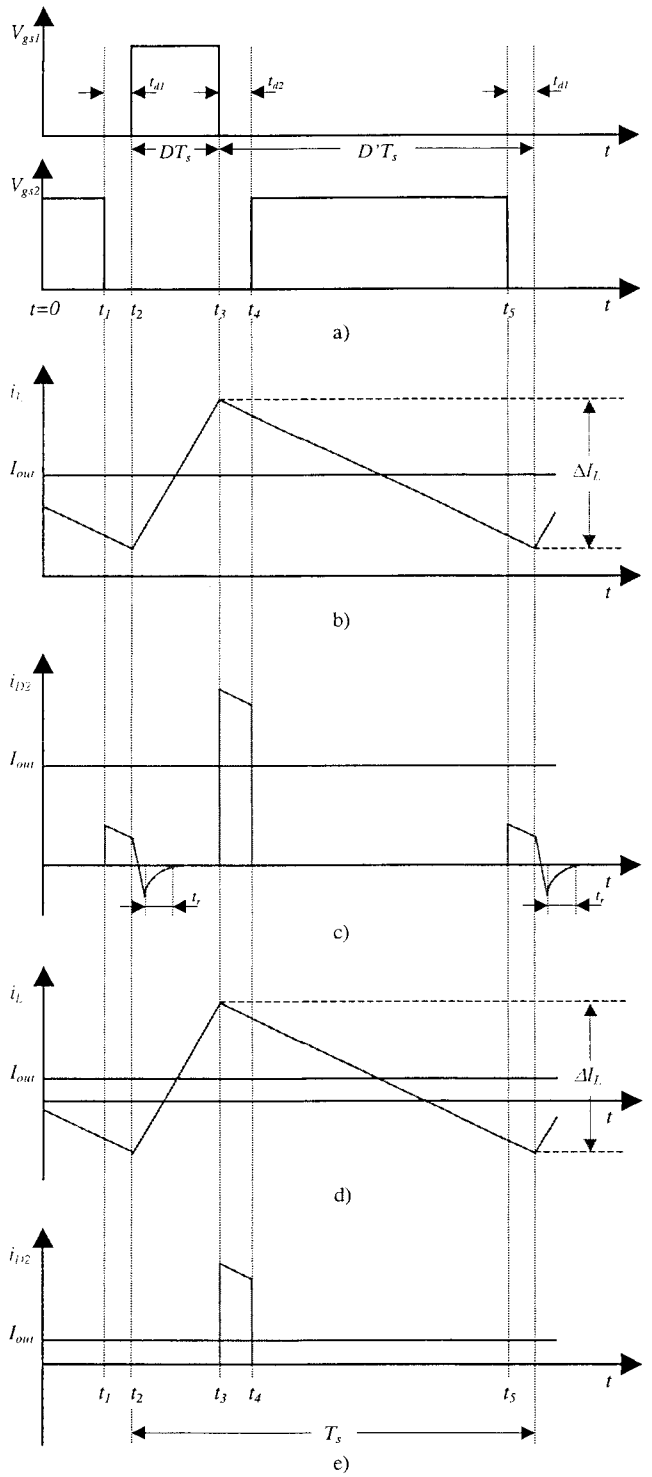


Figure 6.7: Synchronous buck converter waveforms: a) gate drive signals for Q_1 and Q_2, b) inductor current in mode 1, c) SR body diode current in mode 1, d) inductor current in mode 2, and e) SR body diode current in mode 2

mode 2. Although a synchronous buck converter always operates in the continuous conduction mode (CCM), as the waveforms in Fig. 6.7 indicate, mode 1 and mode 2 are very different from the efficiency standpoint and merit separate careful investigation.

The second dead time interval, t_{d2}, occurs at a time t_3. At t_3, the main switch turns off and allows the diode D_2 (the body diode of the SR or an external Schottky diode) to conduct until the SR turns on at t_4 (see Fig. 6.7).

The SR body diode will produce losses during the two dead time intervals, t_{d1} and t_{d2}. Therefore, we can express P_{BD} as:

$$P_{BD} = P_{td1} + P_{td2} \tag{6.2}$$

where P_{td1} is the total body diode loss during t_{d1}, and P_{td2} is the total body diode loss during t_{d2}.

6.5 Effect of t_{d1} on the Synchronous Buck Efficiency in Mode 1

At $t=t_1$, the SR is turned off and the SR body diode D_2 turns on to provide a return path for the inductor current (see Figs. 6.7b and 6.7c). When Q_1 turns on at t_2, the forward biased body diode sees a reverse voltage equal to the input voltage. Since the SR body diode is a regular p-n diode, it cannot turn off instantaneously due to the stored minority carrier charge. The reverse recovery current spike caused by the removal of the stored charge can be quite large. It can, therefore, be a source of a significant additional loss in both the SR and the main switch. Thus, P_{td1} is given by:

$$P_{td1} = P_{cd1} + P_{rr} \tag{6.3}$$

where P_{cd1} is the body diode conduction loss during t_{d1}, and P_{rr} is the loss caused by the body diode reverse recovery at the end of t_{d1}.

6.5.1 Overall Efficiency Degradation Due to the Body Diode Conduction During t_{d1} (mode 1)

After the SR turns off at t_1, the body diode will conduct for a time t_{d1} before the main switch turns on at t_2. During this time, the diode conducts the full inductor current equal to $I_{out} - \frac{\Delta I_L}{2}$. Hence, the body diode conduction loss can be expressed as:

$$P_{cd1} = V_f \cdot \left(I_{out} - \frac{\Delta I_L}{2} \right) \cdot t_{d1} \cdot f_s \tag{6.4}$$

where V_f is the diode forward voltage drop, ΔI_L is the inductor current ripple, and f_s is the switching frequency. Clearly, in order to minimize P_{cd1}, we must minimize t_{d1}. The next step is to determine the impact of P_{cd1} on the overall converter efficiency. Therefore, we will define the efficiency degradation due to the body diode conduction during t_{d1}, $\Delta\eta_{cd1}$, in the following way:

$$\Delta\eta_{cd1} = \frac{P_{cd1}}{P_{in}} \tag{6.5}$$

where P_{in} is the input power of the converter. In order to calculate $\Delta\eta_{cd1}$ we made the following assumptions:

- V_{in}=12V.
- V_{out}=3.3V.
- ΔI_L=7.6A.
- f_s=1MHz.
- The top switch (Q_1) is an N-channel MOSFET (R_{DSon}=20mΩ and Q_g=15nC @ V_{gs}=5V).
- The synchronous rectifier (Q_2) is an N-channel MOSFET (R_{DSon}=16mΩ and Q_g=18nC @ V_{gs}=5V).

- Switching times for Q_1 are t_{on}<8ns, t_{off}<9ns; switching times for the SR are t_{on}<8ns, t_{off}<6ns (based on previous experience and MOSFET data sheets).

In Fig. 6.8 we plotted $\Delta\eta_{cd1}$ as a function of the load current with t_{d1} as a parameter (t_{d2}=const.=10ns). Fig. 6.8 shows that by reducing t_{d1} from 60ns down to 10ns (while keeping t_{d2} constant) we can increase the overall converter efficiency by over 0.6% at full

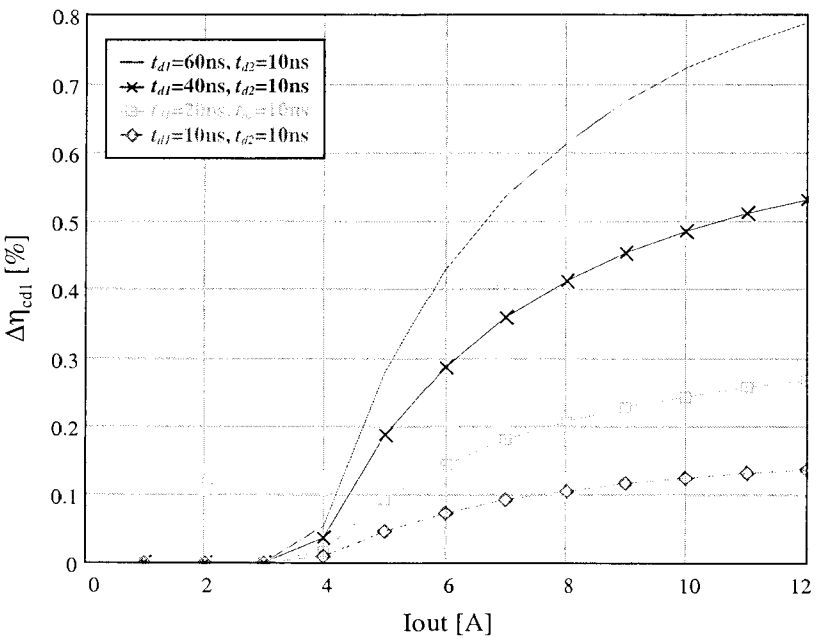


Figure 6.8: The overall efficiency degradation due to the conduction of D_2 as a function of the load current for t_{d1}=10ns-60ns (V_{in}=12V, V_{out}=3.3V, f_s=1MHz, t_{d2}=10ns)

load (12A). Hence, in mode 1, t_{d1} should be as short as possible in order to minimize $\Delta\eta_{cd1}$, and, in turn, maximize the efficiency of a synchronous buck converter.

6.5.2 Overall Efficiency Degradation Due to the Body Diode Reverse Recovery During t_{d1} (mode 1)

Assuming the converter operates in mode 1, the body diode will turn on and conduct during the interval t_{d1} (see Fig. 6.7c). When the SR body diode turns off at t_2, two kinds

of losses associated with its reverse recovery can be identified: the loss in the diode itself, and the loss in the main switch due to the reverse recovery spike. The additional loss in the main switch will only be present if the parasitic inductance of the loop formed by V_{in}, Q_1, and Q_2 (see Fig. 6.6) is small enough to allow the reverse recovery current to reach its peak before the voltage across Q_1 has dropped. In this case, the turn on switching loss of the main FET will increase significantly. If, on the other hand, the parasitic inductance of the V_{in}-Q_1-Q_2 loop is large enough, Q_1 will be able to turn on before any appreciable reverse recovery current can build up. Hence, the loss in the main switch will be unaffected by the reverse recovery of the body diode.

Regardless of whether the loss in the main switch is increased or not, the loss in the body diode due to its reverse recovery will always be present. Since the typical turn on time of the FET, t_{on}, is much shorter than the typical recovery time of the diode, t_r (see Fig. 6.7c), the FET will turn on while the peak reverse recovery current is flowing through the diode. Thus, the reverse recovery loss in the body diode can be approximated by:

$$P_{rr} = \tfrac{1}{2} \cdot V_{in} \cdot I_{rr} \cdot t_r \cdot f_s \tag{6.6}$$

where I_{rr} is the peak reverse recovery current, and t_r is the recovery time of the body diode (see Fig. 6.7c). We can now define the total efficiency degradation due to the reverse recovery of the body diode, $\Delta\eta_{rr}$, in the following way:

$$\Delta\eta_{rr} = \frac{P_{rr} + \Delta P_{SQ1}}{P_{in}} \tag{6.7}$$

where ΔP_{SQ1} is the increase in the switching loss of the main FET due to the reverse recovery spike.

Based on our measurements and the assumptions made in Section 6.4, we calculated $\Delta\eta_{rr}$ and plotted it as a function of the load current with t_{d1} as a parameter (t_{d2}=const.=10ns) in Fig. 6.9. It is important to notice that, for a fixed load current, the magnitude of the peak reverse recovery current decreases as the dead time is decreased. In fact, at t_{d1}=10ns, we were unable to measure any significant reverse recovery current. This reduction in the reverse recovery current can be explained by the extremely short time (<60ns) during which the diode is allowed to conduct. Since the diode cannot reach a steady state that fast, the excess minority carrier concentration is much smaller than in

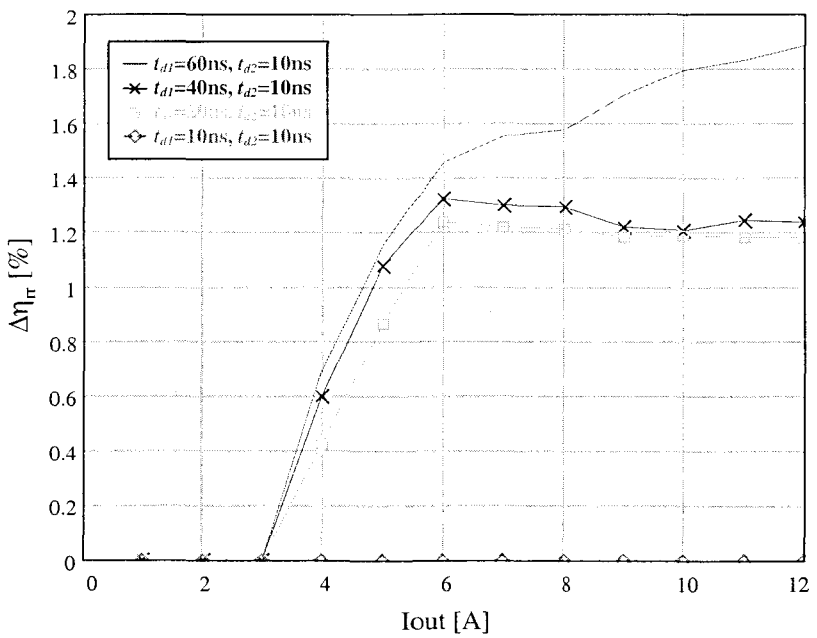


Figure 6.9: The overall efficiency degradation due to the reverse recovery of D_2 as a function of the load current for t_{d1}=10ns-60ns (V_{in}=12V, V_{out}=3.3V, f_s=1MHz, t_{d2}=10ns)

the steady state. Thus, when the diode turns off, less charge needs to be removed resulting in a reduced reverse recovery spike and a reduced power loss. Therefore, it is important to minimize the body diode conduction time in order to reduce the reverse

recovery loss. In fact, the efficiency of a synchronous buck converter can be improved by over 1.5% when a portion of the reverse recovery loss is eliminated by reducing t_{d1} from 60ns to 10ns.

6.5.3 Overall Efficiency Degradation Due to the Body Diode Conduction and Reverse Recovery During t_{d1} (mode 1)

In the preceding two sections, we have separately examined the two loss components associated with t_{d1} in mode 1: body diode conduction and body diode reverse recovery. Comparing the efficiency degradation due to these effects (see Figs. 6.8 and 6.9), one can conclude that the latter is more significant for the chosen inductor current ripple. The full effect of t_{d1} on the converter efficiency is, however, obtained when these two effects are combined. Hence, we will define the total efficiency degradation due to t_{d1}, $\Delta\eta_{td1}$, in the following way:

$$\Delta\eta_{td1} = \Delta\eta_{cd1} + \Delta\eta_{rr} \tag{6.8}$$

Fig. 6.10 shows a plot of $\Delta\eta_{td1}$ as a function of the load current with t_{d1} as a parameter (t_{d2}=const=10ns). Since both $\Delta\eta_{cd1}$ and $\Delta\eta_{rr}$ are reduced by shortening t_{d1}, it follows from (6.8) that $\Delta\eta_{td1}$ is also reduced by minimizing t_{d1}. The reduction of t_{d1} from 60ns to 10ns yields an overall synchronous buck efficiency improvement of approximately 2.5%

6.6 Effect of t_{d1} on the Synchronous Buck Efficiency in mode 2

If the converter operates in mode 2, the inductor current has reversed its direction when the SR turns off at t_1 (see Figs. 6.2d and 6.2e). Consequently, the body diode cannot turn on. Instead, the inductor current simultaneously charges the parasitic drain to source capacitance of the SR and discharges the drain to source capacitance of the main switch. Thus, the phase node voltage V_x (see Fig. 6.6) increases during t_{d1} even though

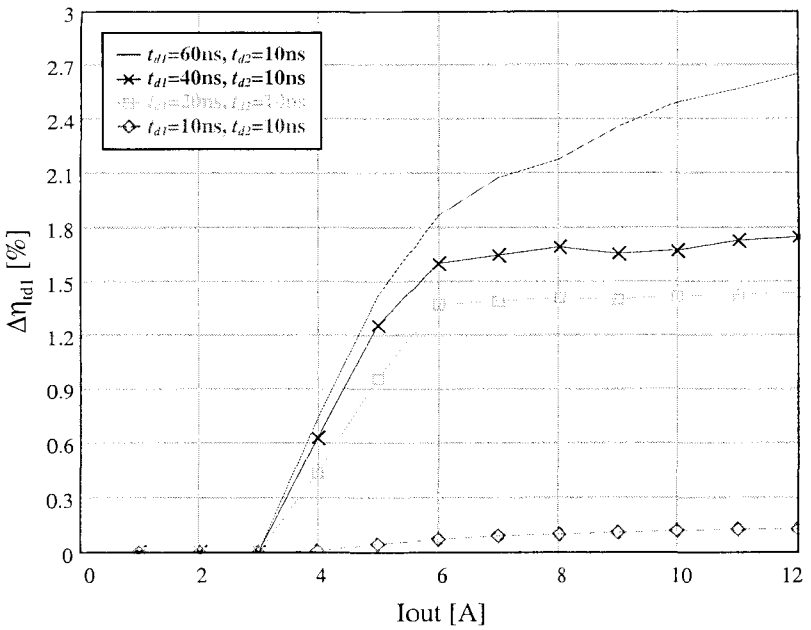


Figure 6.10: The overall efficiency degradation due to the conduction and the reverse recovery of D_2 as a function of the load current for t_{d1}=10ns-60ns (V_{in}=12V, V_{out}=3.3V, f_s=1MHz, t_{d2}=10ns)

Q_1 remains turned off. Ideally, we would like Q_1 to turn on exactly when V_x reaches the input voltage. Unfortunately, the minimum possible dead time that is optimum in mode 1 will not be sufficient to achieve full soft turn on of Q_1.

Since the body diode does not turn on during t_{d1} in mode 2, it cannot produce any losses during this interval. Therefore,

$$P_{td1} = 0 \tag{6.9}$$

as shown in Figs. 6.8, 6.9, and 6.10 (for I_{out}<4A).

Since P_{td1} is zero in mode 2, we can increase t_{d1} to achieve full soft turn on of the main switch, thereby increasing the efficiency of the converter. However, if we increase the dead time too much, V_x can exceed V_{in} during t_{d1} and the body diode of the main FET

turns on. In this situation, the benefit of the soft turn on of Q_1 is reduced by the conduction loss of D_1.

Having a fixed t_{d1}, we cannot simultaneously optimize the converter for operation in both mode 1 and mode 2. However, our analysis has shown that the efficiency degradation at full load due to the unnecessarily long t_{d1} is far greater than the efficiency improvement achieved due to the soft switching at light load. Therefore, the best overall synchronous buck efficiency over the entire load range is achieved with the minimum possible t_{d1}.

6.7 Effect of t_{d2} on the Synchronous Buck Efficiency

During the interval t_{d1}, the reverse recovery of the SR body diode was the dominant loss mechanism. On the other hand, during t_{d2}, the reverse recovery will not be a problem. When the SR turns on at t_4, it softly takes over the current from the body diode. The voltage across the body diode remains positive, but smaller than the diode forward voltage. Thus, the diode is forced to turn off. However, since no reverse voltage is applied across the diode, it turns off without any reverse recovery taking place. Therefore, the only loss associated with the dead time interval t_{d2} is the body diode conduction loss. We can write:

$$P_{td2} = P_{cd2} \tag{6.10}$$

where P_{td2} is the total body diode loss during t_{d2}, and P_{cd2} is the body diode conduction loss during t_{d2}. P_{cd2} can now be expressed as:

$$P_{cd2} = V_f \cdot \left(I_{out} + \frac{\Delta I_L}{2} \right) \cdot t_{d2} \cdot f_s \tag{6.11}$$

As we can see from (6.11), P_{cd2} is directly proportional to the output current and the output current ripple. Clearly, the larger the output current and the larger the ripple, the more critical it becomes to keep t_{d2} as small as possible. Although there is no reverse recovery loss during t_{d2}, the effect of P_{cd2} on the overall converter efficiency is quite detrimental since the diode has to conduct the output current plus half the ripple current (see Fig. 6.7). In order to quantify this effect, we will define the overall efficiency degradation due to t_{d2}, $\Delta\eta_{td2}$, in the following way:

$$\Delta\eta_{td2} = \frac{P_{td2}}{P_{in}} \tag{6.12}$$

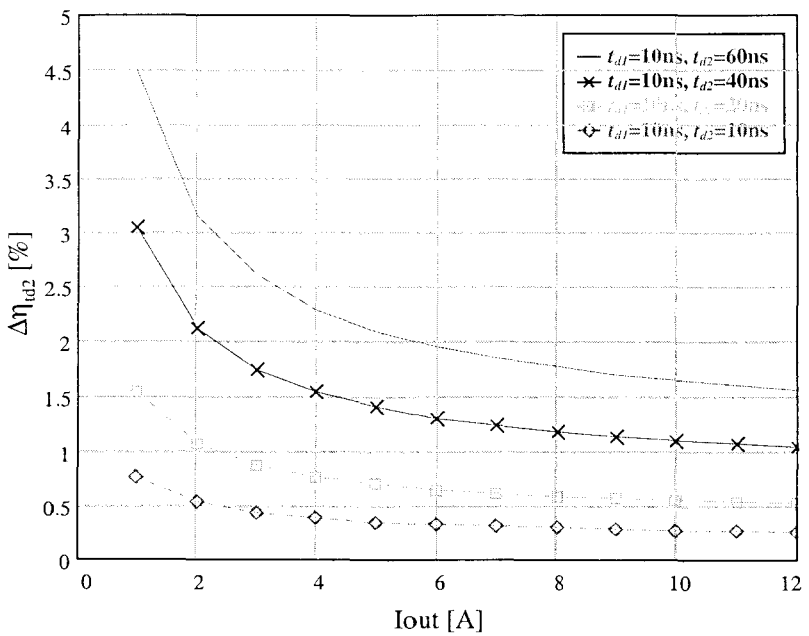


Figure 6.11: The overall efficiency degradation due to the conduction of D_2 as a function of the load current for t_{d2}=10ns-60ns (V_{in}=12V, V_{out}=3.3V, f_s=1MHz, t_{d1}=10ns)

Under the assumptions made in Section 6.4, the maximum load current is 12A, and the inductor current ripple is 7.6A. At full load, the dominant factor in (6.11) is the output current. However, at light load, P_{cd2} is dominated by the ripple current. In Fig. 6.11, $\Delta\eta_{td2}$ is plotted as a function of the load current with t_{d2} as a parameter (t_{d1}=const.=10ns). Fig. 6.11 shows that while it is important to keep t_{d2} small over the entire load current range of a fixed frequency, hard-switched converter, it is critical to keep it as small as possible at a very light load. If we can reduce t_{d2} from 60ns down to 10ns, we will improve the overall synchronous buck efficiency by over 3.5% at light load (1A) and by over 1.2% at full load (12A).

6.8 Effect of t_{d1} and t_{d2} on the Synchronous Buck Efficiency

Based on our previous discussion, we can combine the efficiency degradation effects of t_{d1} and t_{d2}. Therefore, we will define $\Delta\eta_{td}$, the overall converter efficiency degradation due to both dead time intervals, in the following way:

$$\Delta\eta_{td} = \Delta\eta_{td1} + \Delta\eta_{td2} \tag{6.13}$$

We can now get the complete picture of efficiency degradation for any combination of t_{d1} and t_{d2}.

First, we can keep t_{d2}=10ns (constant) and increase t_{d1} from 10ns to 60ns. For this combination of t_{d1} and t_{d2}, $\Delta\eta_{td}$ is plotted as a function of the load current in Fig. 6.12. When the converter is operating in mode 2, which in this particular case happens for I_{out}<4A, P_{td1} is zero. Hence, any efficiency degradation in this region is due to P_{td2}. However, since t_{d2} is only 10ns, this degradation will be rather small. On the other hand, once the converter enters mode 1, P_{td1} starts to increase (see Fig. 6.10) and quickly becomes the dominant factor (see Figs. 6.10, 6.11, and 6.12).

The effect of increasing t_{d2} while t_{d1} is kept constant is shown in Fig. 6.13. Since t_{d1} is very small, the efficiency degradation it introduces in this case can be neglected. Therefore, efficiency degradation over the entire load current range is due to t_{d2}. Comparing the efficiency degradation curves in Figs. 6.12 and 6.13, we can immediately note that it is equally important to minimize both t_{d1} and t_{d2} in a fixed frequency, hard-switched synchronous buck converter.

In our calculations and subsequent experimental verification, we were able to change t_{d1} and t_{d2} independently. However, a commercial controller does not provide this luxury. The break-before-make times, t_{d1} and t_{d2}, are internally set, and are equal. Consequently,

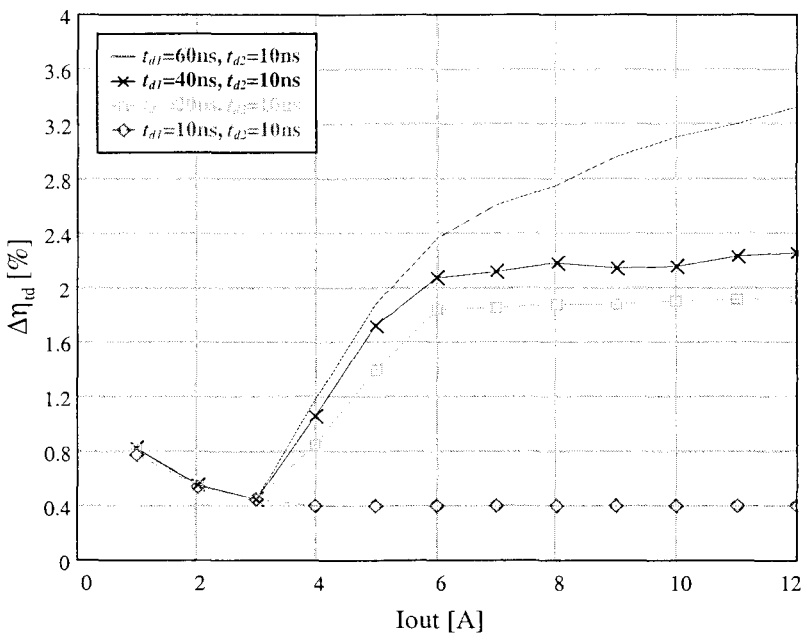


Figure 6.12: The overall efficiency degradation as a function of the load current for t_{d1}=10ns-60ns, t_{d2}=10ns, (V_{in}=12V, V_{out}=3.3V, f_s=1MHz)

the price you pay for a long dead time is even worse than what Figs. 6.12 and 6.13 predict. The overall efficiency degradation as a function of the load current for t_{d1}=t_{d2}

varied from 10ns to 60ns is given in Fig. 6.14 (V_{in}=12V, V_{out}=3.3V, f_s=1MHz). Fig. 6.14 shows that by reducing t_{d1} and t_{d2} from 60ns to 10ns in a fixed frequency, hard-switched, synchronous buck converter, we can improve both the full load (12A) and the light load (1A) efficiency by approximately 4%.

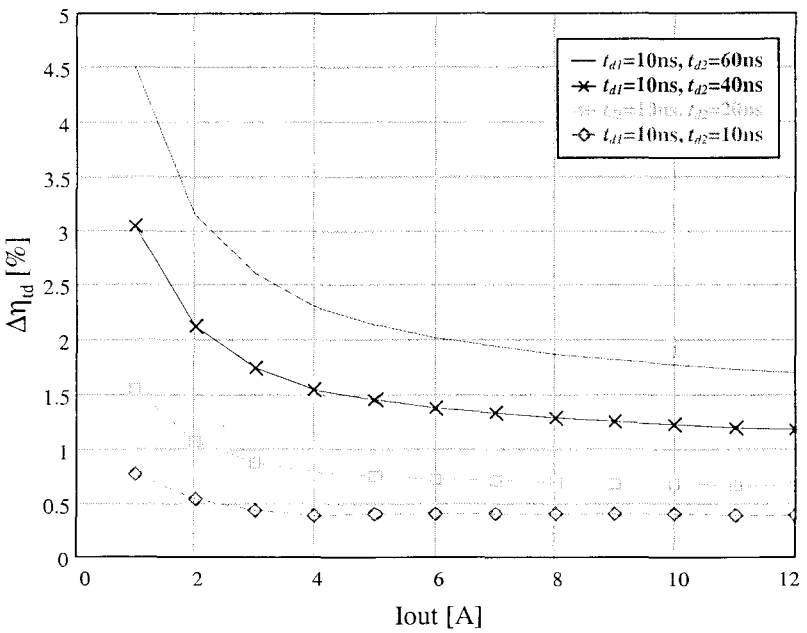


Figure 6.13: The overall efficiency degradation as a function of the load current for t_{d2}=10ns-60ns, t_{d1}=10ns, V_{in}=12V, V_{out}=3.3V, f_s=1MHz

If we compare the results in Figs. 6.8 and 6.11, we will notice that the loss due to the body diode conduction during t_{d2} is much larger than during t_{d1}. This ratio will, however, depend on the size of the inductor current ripple. Namely, when the ripple is increased, P_{cd2} becomes larger and P_{cd1} becomes smaller. The total body diode conduction loss due to t_{d1} and t_{d2}, P_{cd}, can be expressed by:

$$P_{cd} = V_f \cdot f_s \cdot \left[I_{out} \cdot (t_{d1} + t_{d2}) + \frac{\Delta I_L}{2} \cdot (t_{d2} - t_{d1}) \right] \tag{6.14}$$

If $t_{d1}=t_{d2}$, as is usually the case, P_{cd} will be independent of the inductor current ripple. This should be taken into account when choosing the value of the inductor current ripple.

The results presented in Fig. 6.14 demonstrate that by precise gate drive timing the overall circuit efficiency can be improved by 4%. However, even after an extensive data sheet search, it turned out that a standard control IC which combines enough drive

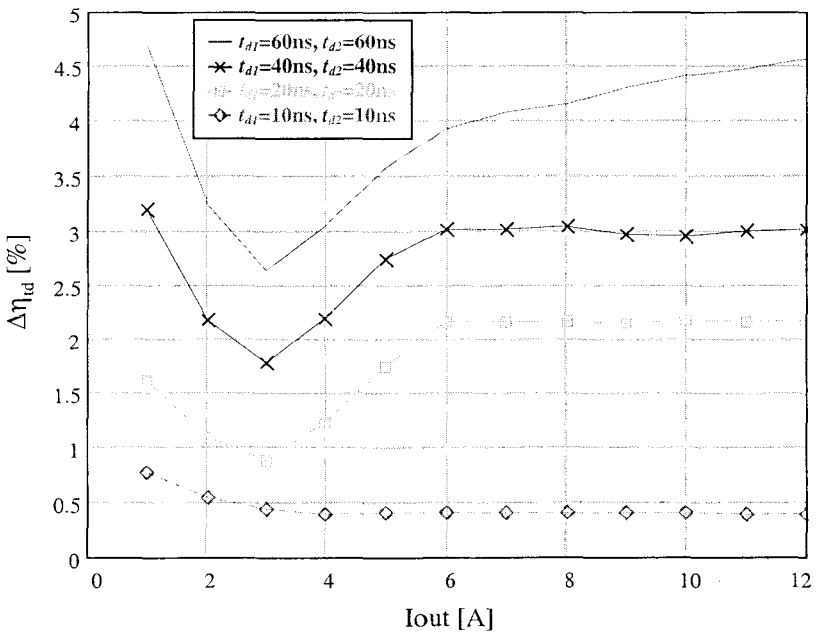


Figure 6.14: The overall efficiency degradation due to $t_{d1}=t_{d2}$ varied from 10ns to 60ns as a function of the load current ($V_{in}=12V$, $V_{out}=3.3V$, $f_s=1MHz$)

capability with a minimum dead time of less than about 50-60ns is not commercially available. Thus, in order to optimize the synchronous buck for high frequency operation, it was necessary to develop a gate drive circuit that will achieve 10ns dead times and have adequate drive capability for sub 10ns switching times.

6.9 New High Performance Gate Drive Circuit

The lack of a standard IC suitable for use in high frequency, high power density applications prompted us to develop a new gate drive circuit that provides a much shorter dead time. In order to study the effects of each dead time delay on the converter efficiency, we made it possible to independently adjust the turn on delay for each FET. This feature allowed us to experimentally verify theoretical predictions and investigate what is the highest efficiency we can achieve with a fixed frequency and a fixed dead time synchronous buck converter at high frequency.

The new drive circuit, shown in Fig. 6.15, was used to control a high efficiency prototype buck converter shown in Fig. 6.6. Feedback from the power MOSFET gate V_{g1} to the input of the NOR_2 logic gate provides shoot-through protection at SR turn on. If this feedback is not enough to insure that no cross-conduction occurs, the delay network R_{d1}-C_{d1} can be used to introduce an additional delay before Q_1 turns on. The delay network can be used to precisely set the dead time.

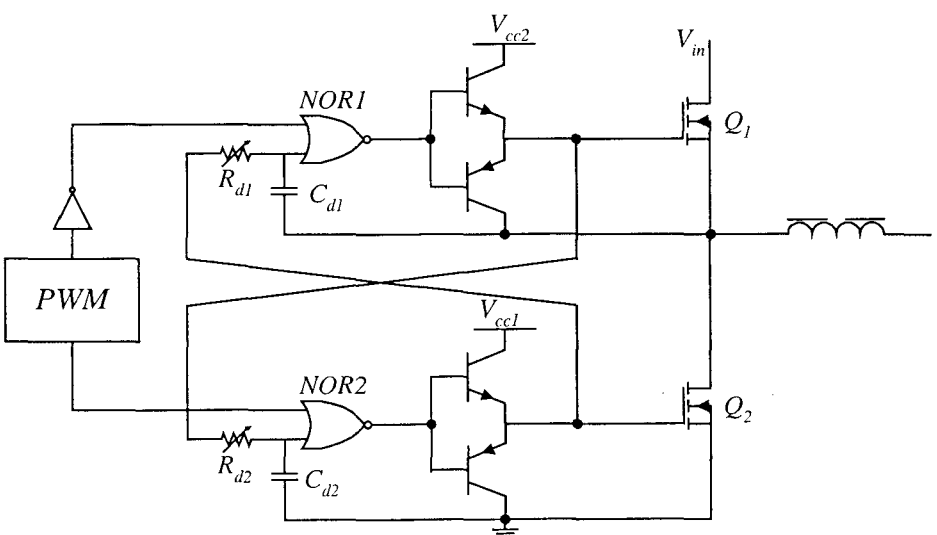


Figure 6.15: High performance gate drive with independently adjustable dead times

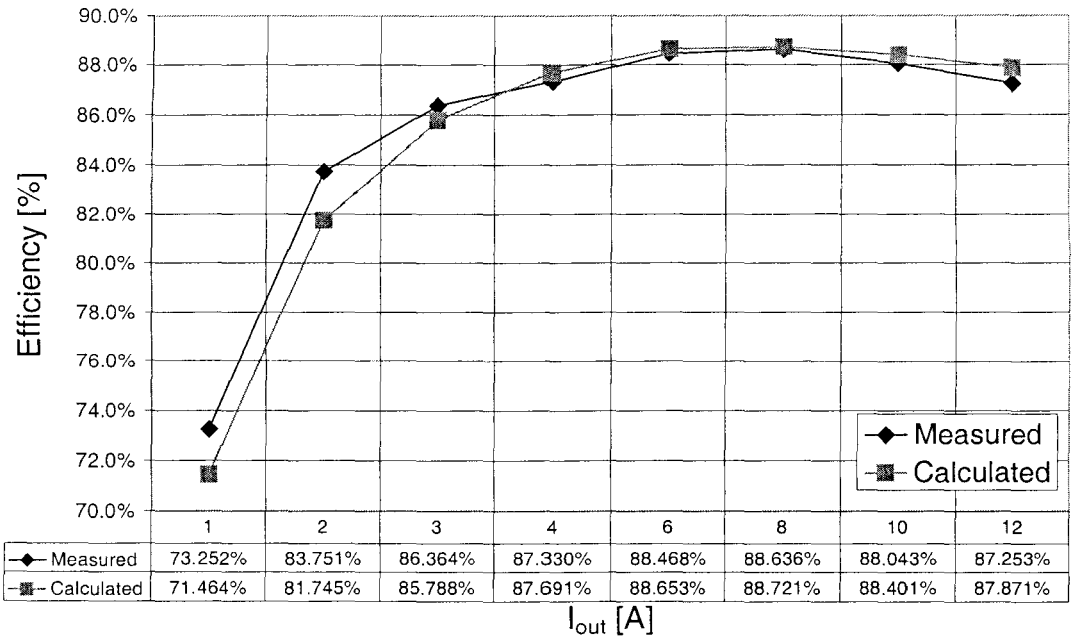
As in the case of SR turn on, feedback from the power MOSFET gate V_{g2} to the input of the NOR_1 logic gate provides shoot-through protection at S_1 turn on. Similarly, the delay network R_{d2}-C_{d2} allows us to adjust the delay before Q_2 turns on. Hence, with this circuit, we have achieved independent dead time control down to less than 10ns. The key to achieving t_d~10ns was the fast logic (*NOR1*, *NOR2*). Independent control of the delay before each switch turns on allows us to optimize each delay separately to achieve maximum efficiency. Adequate drive capability for sub 10ns switching is provided by the high current capability bipolar output stage.

The prototype achieves a minimum dead time of 10ns and adequate switching speed for 1MHz operation. The converter is operated with a 12V input voltage, a 3.3V output voltage, and with a load current of up to 12A.

6.10 Experimental Verification

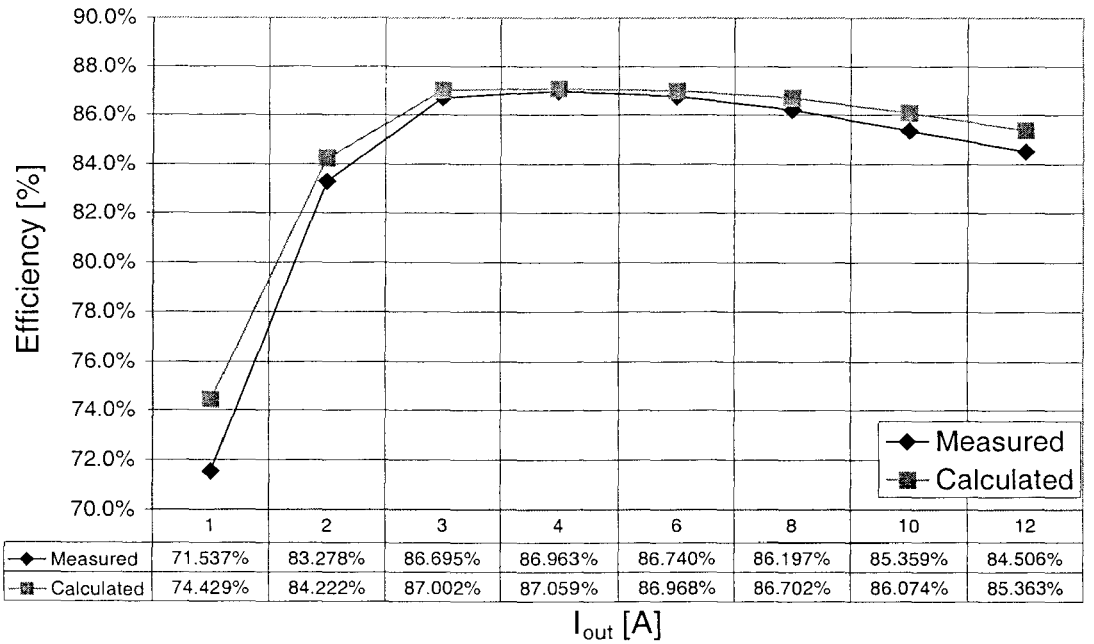
In order to verify our calculations and predictions, we built a synchronous buck converter using surface mount components, and operated it according to the assumptions given in Section 6.4.

The predicted and the measured synchronous buck efficiency, as a function of the load current for two values of t_{d1} (10ns and 60ns) with t_{d2}=const.=10ns (V_{in}=12V, V_{out}=3.3V, f_s=1MHz), are shown in Figs. 6.16 and 6.17, respectively. Figs. 6.16 and 6.17 show the excellent agreement between the measured and the calculated results over the entire load current range.



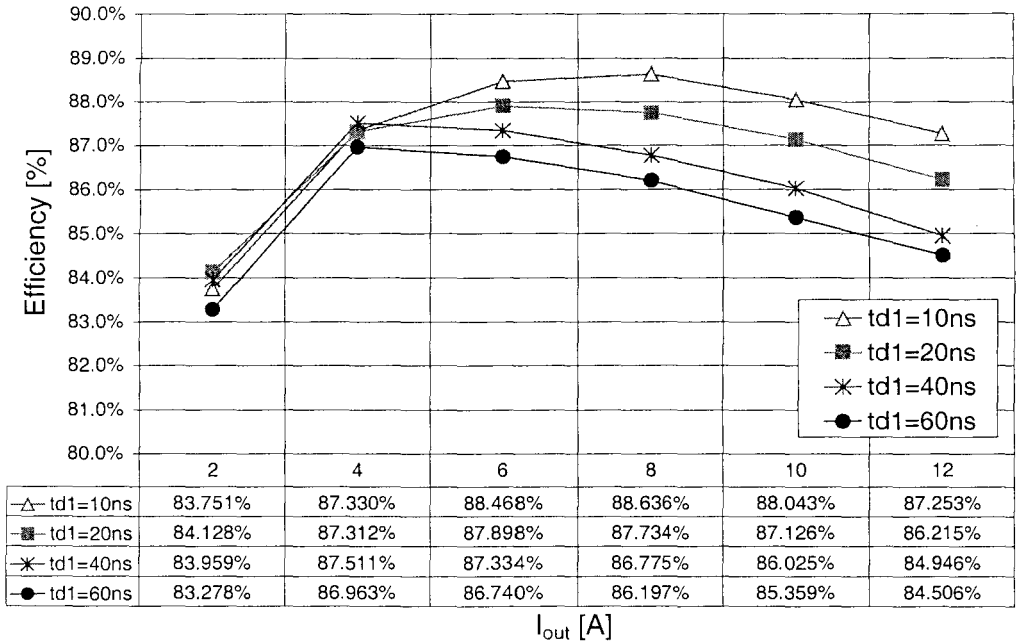
	1	2	3	4	6	8	10	12
Measured	73.252%	83.751%	86.364%	87.330%	88.468%	88.636%	88.043%	87.253%
Calculated	71.464%	81.745%	85.788%	87.691%	88.653%	88.721%	88.401%	87.871%

Figure 6.16: Measured and calculated overall synchronous buck efficiency for $t_{d1}=t_{d2}=10ns$ ($V_{in}=12V$, $V_{out}=3.3V$, $f_s=1MHz$)



	1	2	3	4	6	8	10	12
Measured	71.537%	83.278%	86.695%	86.963%	86.740%	86.197%	85.359%	84.506%
Calculated	74.429%	84.222%	87.002%	87.059%	86.968%	86.702%	86.074%	85.363%

Figure 6.17: Measured and calculated overall synchronous buck efficiency for $t_{d1}=60ns$, $t_{d2}=10ns$ ($V_{in}=12V$, $V_{out}=3.3V$, $f_s=1MHz$)



	2	4	6	8	10	12
td1=10ns	83.751%	87.330%	88.468%	88.636%	88.043%	87.253%
td1=20ns	84.128%	87.312%	87.898%	87.734%	87.126%	86.215%
td1=40ns	83.959%	87.511%	87.334%	86.775%	86.025%	84.946%
td1=60ns	83.278%	86.963%	86.740%	86.197%	85.359%	84.506%

Figure 6.18: The measured overall synchronous buck efficiency for t_{d1}=10-60ns, t_{d2}=10ns (V_{in}=12V, V_{out}=3.3V, f_s=1MHz)

Fig. 6.18 shows measured efficiency data for several values of t_{d1} combined in one plot to clearly show the effects we discussed in previous sections. First, we notice the efficiency degradation at full load due to the increase of t_{d1}. The efficiency degradation is evident throughout mode 1 operation (I_{out}>4A). However, as we enter mode 2 (I_{out}<4A) the efficiency increases slightly as t_{d1} is increased due to the soft turn on of Q_1. When the dead time becomes too long (t_{d1}=60ns), the benefit of the soft switching is offset by the conduction loss of the diode D_1.

6.11 Conclusion

We have analyzed the effect of two dead time intervals, t_{d1} and t_{d2}, on the synchronous buck efficiency. It was found that each interval contributes approximately half of the efficiency degradation. However, the loss mechanisms are different. During t_{d1}, the dominant loss component is the reverse recovery of the SR body diode. The loss

due to the conduction of the body diode is, in this case, small because the diode carries the inductor current minus one-half of the inductor ripple current. On the other hand, during t_{d2}, the SR body diode carries the load current plus one-half of the inductor current ripple. Therefore, the conduction loss is significant during this interval. Our calculations have shown that it is important to minimize t_{d1} to reduce the body diode reverse recovery loss, and that it is important to minimize t_{d2} to reduce the body diode conduction loss. Consequently, the best overall efficiency is achieved when both t_{d1} and t_{d2} are minimized.

The SR body diode conduction loss during both intervals depends on the magnitude of the inductor current ripple. When the ripple is increased, P_{cd2} increases and P_{cd1} decreases. Interestingly enough, if $t_{d1}=t_{d2}$, their sum remains constant. However, the overall efficiency degradation due to the SR body diode conduction is *not* independent of the inductor current ripple. Namely, the loss due to the body diode reverserecovery, dominant during t_{d1}, will depend on the magnitude of the ripple current. The larger the ripple, the smaller the forward current through the diode D_2 will be when it starts to turn off at t_2. Consequently, less minority carrier charge will be stored, the reverse recovery spike will be smaller, and the overall efficiency degradation will be reduced. Therefore, the efficiency degradation due to the SR body diode conduction decreases when the inductor current ripple increases. Unfortunately, a large inductor current ripple will increase losses in other parts of the circuit. This trade-off needs to be taken into consideration.

The efficiency calculations predicted that synchronous buck efficiency could be improved by over 3.5% by eliminating unnecessary body diode conduction. On the basis of this analysis, a highly efficient, fixed frequency, 1MHz synchronous buck converter

has been realized by implementing a gate drive that allows less than 10ns dead time and achieves fast switching speed. Theoretical predictions have been fully verified on the developed prototype. The overall efficiency of over 87.2% for V_{in}=12V and V_o=3.3V has been achieved at I_{out}=12A and f_s=1MHz.

Chapter 7

Optimizing the Voltage Mode Control Loop of a Buck Converter for Point-of-Load Microprocessor Applications

7.1 Introduction

The demand for faster, more powerful computers keeps pushing microprocessor manufacturers to pack more computational power and more features into each new generation of microprocessors. As a result, the power requirements of a microprocessor, as well as the on-chip power dissipation, have steadily been increasing. As this trend continued, adequate cooling of the processor, and the entire system, became an issue. In order to deal with the on-chip power dissipation, the processor core logic supply voltage had to be lowered. A lower core logic operating voltage reduces the processor power requirements providing the clock frequency remains unchanged. In other words, for a given power dissipation, a processor with a lower core logic operating voltage can run at a higher clock frequency. Hence, it is quite clear that future high performance microprocessors will continue to migrate to lower core supply voltages and higher operating currents making power distribution and delivery increasingly difficult.

As the processor core logic supply voltage is reduced, more precise signal voltage levels are required to insure error-free operation. Under the circumstances, microprocessor manufacturers have had to impose very stringent requirements on both the static and the transient output voltage regulation of the point-of-load modules powering the CPU. A portion of the latest Pentium III VRM electrical specifications is given in Table 7.1 [11]. Meeting these specs requires careful optimization of both the power stage and the control loop. This paper will focus on the design and optimization of the voltage mode control loop. An optimized control loop can save microfarads of output capacitance, thus reducing the size and the cost of the point-of-load module.

One way to approach the loop design of a point-of-load module is to use SPICE to simulate the entire circuit. However, this process is time consuming, and yields little insight into which circuit parameters need to be changed to improve the transient response of the converter. An alternative to "brute force" simulation, as it was pointed out in [12], [13] and [14], is the design oriented approach that uses the output impedance of the converter to predict its transient response. This approach was used in [14] to optimize the load transient response of a synchronous buck converter designed to meet the Pentium II VRM specifications.

In [14] the authors propose the use of constant off-time current mode control. This control method inherently offers attractive features like the relative ease of closing the loop and the information about the load current that can be used to achieve the ideal load transient response by offsetting the nominal output voltage depending on the load current. Another control method suitable for microprocessor power applications is summing mode control proposed in [15]. Summing mode control is similar to typical current mode

control methods, but is claimed to have a much higher bandwidth, and thus a better transient response. While current mode control schemes advocated in [12], [14] and [15] demonstrate good transient response, it comes at the expense of reduced efficiency. A 7mΩ current sensing resistor will reduce the efficiency of the module by 2-3% depending on the output voltage.

Symbol	Parameter	μP frequency (MHz)	Min	Typ	Max	Unit
Vcc_{core}	Vcc for μP core			2.0		V
	Static tolerance at VRM pins on system board	(K) 450-500	-0.060		0.070	V
	Transient tolerance at VRM pins on system board		-0.130		0.130	V
Icc_{core}	Current for Vcc_{core}	(K) 450 (K) 500			14.5 16.1	A
Icc_{sgnt}	*Icc* for Stop-Grant Vcc_{core}				0.8	A
$\frac{dIcc_{core}}{dt}$	*Icc* slew rate				20	A/μs

Table 7.1: Voltage and current specifications for 2.0V Pentium III (k) processors

In this chapter, we will demonstrate how to use the closed loop output impedance of a buck converter to design and optimize a voltage mode control loop that will achieve a transient response similar to the ones reported in [14] and [15] without sacrificing efficiency. This loop design method eliminates the need for time-consuming simulation of the entire circuit and offers direct insight into where the compensation poles and zeros need to be placed to achieve the desired transient response. In addition, we will be able to derive a simple formula that accurately predicts the peak output voltage deviation due

to a load current transient as a function of the output capacitance and the loop gain crossover frequency.

The voltage mode control loop will be optimized for a 12V to 2.0V synchronous buck converter intended to meet the specifications set forth in [11]. An overview of the buck converter transient response in given in Section 7.2. Section 7.3 examines the conventional voltage mode loop design. Section 7.4 introduces the concept of optimum transient response, and Section 7.5 explains how to achieve it with voltage mode control. Sections 7.6 and 7.7 are devoted to transient response simulation and peak output voltage determination, respectively. Experimental results are presented in Section 7.8, and conclusions in Section 7.9.

7.2 Buck Converter Load Transient Response Revisited

A closed loop buck regulator with voltage mode control is shown in Fig. 7.1. The output of the regulator is connected to a dynamic (microprocessor) load. The load's current requirements can change from almost zero to 16A in a fraction of the regulator's

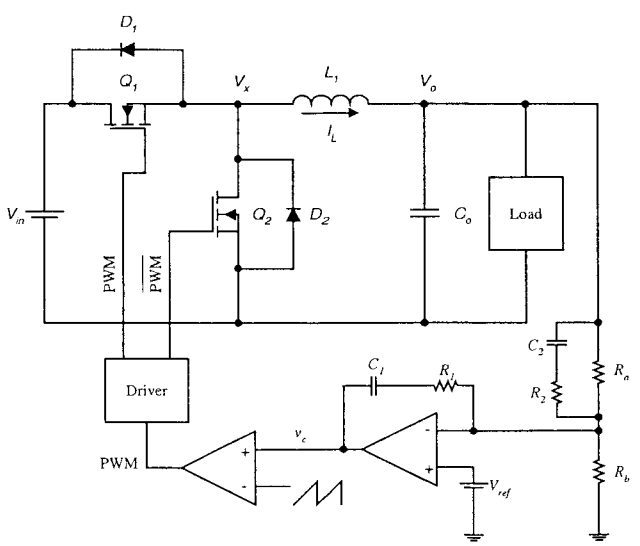


Figure 7.1: Closed loop buck regulator with voltage mode control

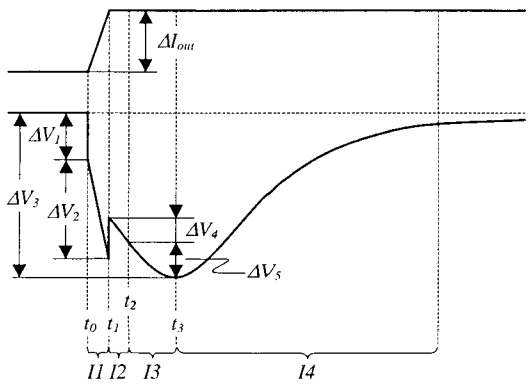


Figure 7.2: Typical transient response of a synchronous buck converter to a load current step occurring at $t=t_0$

switching period. A typical regulator response to a load current change with a slew rate of 20A/μs (Fig. 7.2a) occurring at $t=t_0$ is sketched in Fig. 7.2b. Fig. 7.2b shows that after a load current transient, the output voltage begins to droop because of the power supply's inherent inability to instantly change its operating point. The controller senses the output voltage error and attempts to correct it. Eventually, integral action of the control loop eliminates any steady state error in the output voltage and returns it to its nominal value, as shown in Fig. 7.2b. Between the time when the load current transient occurs and when the regulator output voltage returns to its nominal value, four distinct response intervals, I_1 through I_4, can be identified.

The first interval, I_1, coincides with the rise-time of the load current; I_2 represents the time needed by the control loop to react to the disturbance; I_3 is the time it takes the average inductor current to become equal to the load current, and I_4 is the interval during which the output voltage recovers to its nominal value after reaching its minimum value at $t=t_3$.

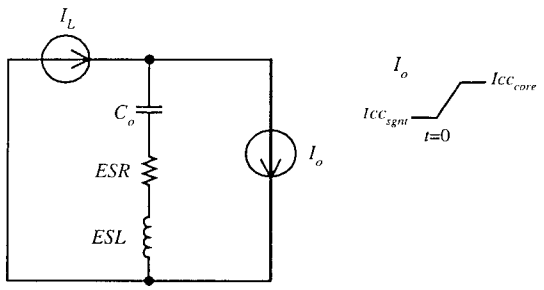


Figure 7.3: Equivalent model of the buck regulator output during I_1

7.2.1 Interval I_1

Since $\Delta t_1=t_1-t_0$ is much shorter than the switching period, the control loop cannot immediately react to this disturbance. Thus, the converter initially responds to the sudden change in the load current in an open loop fashion. As a result, during I_1, the control loop can simply be omitted, and the circuit of Fig. 7.1 can be modeled as shown in Fig. 7.3. In Fig. 7.3, the buck inductor is modeled by a constant current source; the equivalent series resistance and the equivalent series inductance of the output capacitors (*ESR* and *ESL*, respectively) have also been included, as they contribute to the output voltage deviation.

The output voltage deviation during Δt_1, ΔV_{o1}, can be calculated using the following expression:

$$\Delta V_{o1} = Z_o \cdot I_o, \tag{7.1}$$

where Z_o is the open loop output impedance of the converter, and I_o is the ramping load current.

From Fig. 7.3, it can, by inspection, be determined that Z_o is the impedance of the output capacitors. At the frequency of the load current slew rate, Z_o is dominated by the *ESR* and *ESL* of the output capacitors, but the discharge of the output capacitor has been

included for completeness. Consequently, the resulting peak output voltage drop during I_1 can be calculated using (7.2).

$$\Delta V_{o1} = \Delta V_1 + \Delta V_2 = ESL\frac{dI_o}{dt} + ESR \cdot \Delta I_o + \frac{1}{2}\frac{\Delta I_o^{\,2}}{C_o \frac{dI_o}{dt}} \tag{7.2}$$

From (7.2), it is clear that ΔV_{01} depends on the number and the quality of output capacitors, and the magnitude and the slew rate of the load current step; ΔV_{01} *does not* depend on any feedback loop parameters.

7.2.2 Interval I_2

At $t=t_1$ the load current had ramped up to its final value, and the controller still had not had time to respond. Since we are primarily interested in the maximum output voltage deviation, let us assume that the controller turns the main switch (Q_1) on at $t=t_2$, after the worst case delay, t_d, given by:

$$t_d = D'T_s + t_p = t_2 - t_1 = \Delta t_2, \tag{7.3}$$

where D' is the duty ratio of the synchronous rectifier, T_s is the switching period, and t_p is the propagation delay through the PWM comparator and the MOSFET driver. During Δt_2, the full load current discharges the output capacitors causing the worst case output voltage drop to be:

$$\Delta V_4 = \frac{\Delta I_o}{C_o}\Delta t_2, \tag{7.4}$$

where C_o is the total output capacitance. Equation (7.4) shows that ΔV_4 is determined by the value of the output capacitor, the magnitude of the load current step, and the worst case delay, t_d, which, in turn, depends on the switching frequency, and the duty cycle, D;

again, like ΔV_{01}, ΔV_4 *does not* depend on any feedback loop parameters since the loop has not had enough time to respond to the disturbance.

7.2.3 Interval I_3

At $t=t_2$, the controller finally turns Q_1 on, and the feedback loop attempts to correct the output voltage to its nominal value. During the ensuing time interval, $\Delta t_3 = t_3 - t_2$, the inductor current starts to ramp up, but the output voltage continues to decrease until the average inductor current becomes equal to the load current at $t=t_3$.

During I_3, the duty cycle (D) may or may not saturate (keep Q_1 on for more than one whole switching period). If D saturates, the formula derived in Chapter 2 can be used to calculate ΔV_5. This formula can be used in cases when the buck inductor is too large to change its state within one switching cycle and the feedback has enough gain to command a unity duty cycle based on the disturbance until the inductor current becomes equal to the load current. If, on the other hand, the duty cycle does not saturate either because the inductor can change its state quickly or because the loop doesn't have enough gain to command a unity duty cycle, the formula given in Chapter 2 will not apply. Instead, a formula that takes into account the dynamics of the control loop should be used to calculate ΔV_5. Such a formula will be derived in Section 7.7.

If the duty cycle does not saturate during I_3, the converter of Fig. 7.1 can be modeled by its Thevenin equivalent circuit shown in Fig. 7.4. The Thevenin equivalent model takes into account the action of the control loop which results in the regulation of the output voltage and a modification of the open loop output impedance of the converter. Thus, the Thevenin voltage source, V_{TH}, is the regulated output voltage; the Thevenin

impedance, Z_{TH}, is equal to the closed loop output impedance of the converter, Z_{of}. The closed loop output impedance can be expressed as:

$$Z_{TH} = Z_{of} = \frac{Z_o}{1+T}, \tag{7.5}$$

where Z_o is the open loop output impedance of the converter, and T is the loop gain, both of which can easily be calculated using standard small signal modeling methods.

7.2.4 Interval I_4

At $t=t_3$, the average inductor current becomes equal to the load current. Consequently, after $t=t_3$ the output capacitors will start to recharge to their nominal voltage.

During I_4 the converter remains in the normal mode of operation dictated by the control loop. Therefore, the Thevenin equivalent model used to model the converter during I_3 remains valid during I_4.

7.3 Conventional Loop Compensation

In the previous section it was pointed out that the designer's ability to influence the shape of the load transient response using the control loop is limited to intervals I_3 and I_4. Thus, these two intervals will be the focus of the remainder of this work.

In a typical power supply application, the primary goal of a design is to tightly regulate the output voltage. In addition, the regulator will most likely be required to respond to relatively infrequent changes in the load current that certainly do not have the dynamics or the magnitude required by Pentium microprocessors [11]. Consequently, transient response is frequently a secondary concern. Under the circumstances, the voltage feedback loop is usually compensated in such a way to achieve a dominant low-

frequency pole, single slope, loop gain characteristic. Closing the loop in this manner insures a tight output voltage regulation due to a high DC gain, and a reasonably good transient response depending on the achieved bandwidth.

The load transient response of a buck converter with a conventional voltage loop can be examined with the help of the Thevenin equivalent model of Fig. 7.4. When the switch S_1 is closed, it produces a step change in the load current. From Fig. 7.4 we can by inspection write an expression for the output voltage, V_o:

$$V_o(s) = \frac{V_{th}}{s} - Z_{th}(s) \cdot \frac{I_o}{s} \tag{7.6}$$

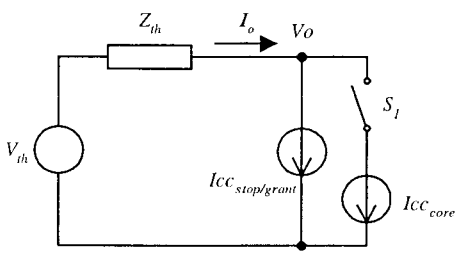


Figure 7.4: The Thevenin equivalent model of a buck regulator output during I_3 and I_4

It should, however, be pointed out that (7.6) is valid only if the duty cycle does not saturate after the step change in the load current. In this case, even though $I_o(t)$ is not a small signal perturbation, the mode of operation of the converter does not change. As a result, small signal models used to derive (7.6) are still valid, despite the temporary increase of the duty cycle.

In order to calculate the transient response using (7.6), $Z_{TH}(s)$ needs to be calculated. As it turns out, $Z_{TH}(s)$ can easily be determined graphically. First, $|Z_o|$ is sketched, as shown in Fig. 7.5a. Since the common single slope loop gain characteristic is assumed,

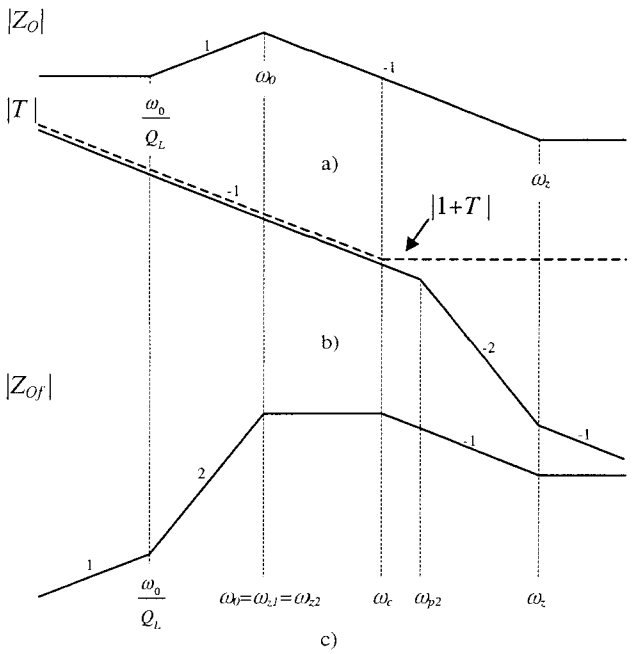


Figure 7.5: a) Typical open loop output impedance of a buck converter, b) Single slope loop gain, c) Closed loop output impedance

$|T|$ and $|1+T|$ can easily be plotted as shown in Fig. 7.5b; $|Z_{TH}|$, given in Fig. 7.5c, is obtained by simply "doing the algebra on the graph," i.e. graphically adding $|Z_o(s)|$ and $|1+T|$. From Fig. 7.5c, an expression for $Z_{TH}(s)$ can be written by inspection. Substituting this expression back into (7.6) results in a frequency-domain expression for the output voltage.

Fig. 7.5c shows that with single slope loop gain, the output impedance starts to quickly decrease below ω_0, and becomes vanishingly small at low frequencies. When this result is substituted in (7.6), it becomes clear why the output voltage quickly returns to its nominal value after any kind of disturbance. Consequently, the peak to peak voltage deviation due to a loading transient followed by an unloading transient is approximately equal to twice the peak output voltage deviation due to a loading transient

alone. If, on the other hand, the output voltage were to stay at, or close to, the lowest level it had reached after the loading transient, extra headroom would be available for the unloading transient; the peak to peak output voltage deviation could approximately be reduced in half.

7.4 Optimum Load Transient Response

It is by now apparent that the single slope loop gain is not the best way to close the loop in Pentium power supply applications. Instead, the system behavior during intervals I_3 an I_4 needs to be influenced by the control loop to minimize ΔV_5 (see Fig. 7.2) and control the output voltage recovery during I_4. Therefore, once the power stage components and the switching frequency have been chosen based on (7.1)-(7.3), optimum control loop design can be undertaken. If ΔV_3 (see Fig. 7.2) can be brought within static tolerances, the loop should be designed to minimize ΔV_5 and realize the response shown with a dashed line in Fig. 7.6. Otherwise, as will most likely be the case, the loop should still minimize ΔV_5, but will, in this case, have to achieve the response shown with a solid line in Fig. 7.6, and allow the output voltage to return to within the static tolerance limit.

7.5 Achieving Optimum Transient Response With Voltage Mode Control

With voltage mode control the information about the value of the average inductor current is not available. Hence, it is not possible to offset the output voltage based on the value of the inductor current. Instead, the desired transient response shown in Fig. 7.6 needs to be achieved by clever loop design.

The problem with conventional single slope loop gain in the context of the optimum transient response in microprocessor applications was clearly outlined by (7.6) and Fig.

7.5c. The rapid decrease of $|Z_{of}|$ below ω_0 is undesirable, and should be eliminated through more suitable loop compensation.

An examination of Fig. 7.4 in conjunction with (7.6) leads to a conclusion that the dashed-line response in Fig. 7.6 requires:

$$Z_{TH}=R_{TH}=const. \tag{7.7}$$

Similarly, the solid line response shown in Fig. 7.4 could be realized with:

$$Z_{TH} = \begin{cases} R_1 = const., f \geq f_m \\ R_2 < R_1 = const., f \leq f_m \end{cases} \tag{7.8}$$

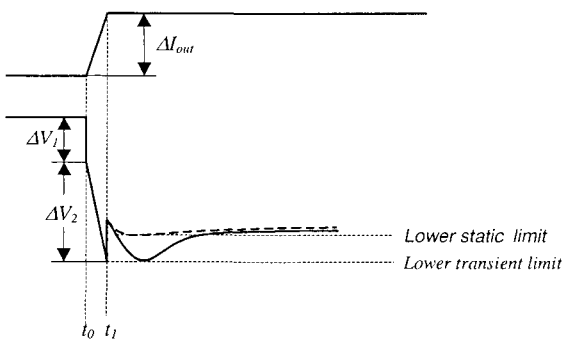


Figure 7.6: Optimum transient response of a synchronous buck converter to a load current step occurring at $t=t_0$

where $1/f_m$ must be less than or equal to the time during which the output voltage can be outside the static limits [1]. Since the general shape of Z_o of a buck converter is predetermined, equations (7.7) and (7.8) define the shape of the loop gain that needs to be achieved.

A typical open loop output impedance of a synchronous buck converter is shown in Fig. 7.7a. In Fig. 7.7 $\omega_0 = 1/\sqrt{LC_o}$ is the filter corner frequency, $Q_L = R_0/R_l$ is the Q factor associated with the series resistance of the inductor, R_l, $R_0 = \sqrt{L/C_o}$ is the characteristic

impedance, and $\omega_z = 1/(ESR \cdot C_o)$ is a zero due to the *ESR* of the output capacitors. The loop gain required to achieve Z_{TH} described by equations (7.7) and (7.8) is given in Fig. 7.7b by the dashed and the solid line, respectively. In Fig. 7.7b ω_{z1}, ω_{z2}, and ω_{p1}, ω_{p2} are the two compensation zeros and the two compensation poles, respectively, and ω_c is the loop gain crossover frequency.

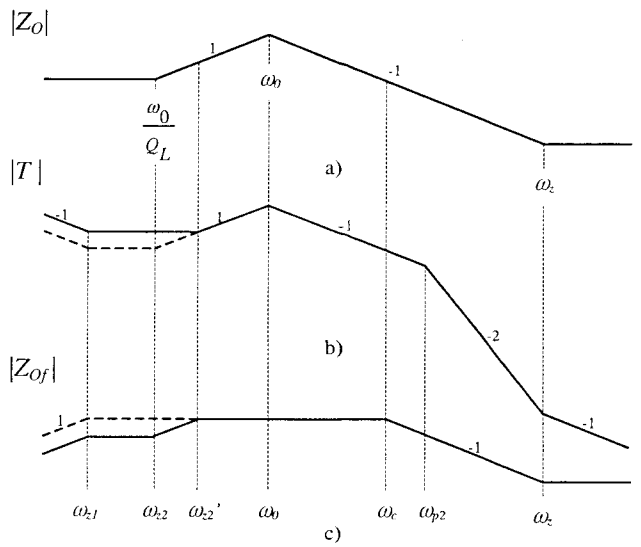


Figure 7.7: a) A typical open loop output impedance of a buck converter, b) Targeted loop gain, c) Optimum closed loop output impedance

Shaping the loop as shown in Fig. 7.7b results in a closed loop output impedance presented in Fig. 7.7c. Figures 7b and 7c demonstrate that only the location of the compensation zero ω_{z2} determines whether Z_{of} approximates equation (7.7) or (7.8). If ω_{z2} is placed at $\frac{\omega_0}{Q_L}$, Z_{of} approximates (7.7) (see the dashed line in Figs.7b and 7c) and results in the dashed transient response in Fig. 7.6. On the other hand, if ω_{z2} is placed between $\frac{\omega_0}{Q_L}$ and ω_0, Z_{of} approximates (7.8) (see the solid line in Figs. 7.7b and 7.7c) and yields a transient response shown with a solid line in Fig. 7.6.

Further examination of Fig. 7.7 reveals that the compensation zero ω_{z1} and its associated pole (assumed to be at zero frequency and not shown), ω_{p1}, actually hurt the transient response by reducing Z_{of} at low frequencies. In fact, without this pole-zero pair, Z_{of} would have the exact shape needed to achieve the ideal transient responses shown in Fig. 7.6. Unfortunately, if this pole-zero pair were omitted from the compensation, the integral action of the control would be eliminated, and the required tight static voltage regulation could not be achieved. Therefore, some transient performance has to be traded for static voltage regulation.

Since ω_{z1} and ω_{p1} cannot be omitted from the compensation, their location has to be chosen carefully to minimize their effect on the transient performance. Namely, in Z_{of} ω_{z1} becomes a dominant low frequency pole. The location of this pole determines the rate of the output voltage recovery after a load transient. As it turns out, [1] specifies a load toggle rate of 100Hz to 100kHz. Therefore, placing the dominant low frequency pole (compensation zero ω_{z1}) in Z_{of} far below 100Hz insures that the output voltage will not significantly recover before the worst case unloading transient (100Hz) happens, thus providing the needed additional headroom for the transient response. The pole ω_{p1} can be placed anywhere from a decade below ω_{z1} all the way to zero frequency, depending on the static voltage regulation requirements. Placing ω_{p1} above zero frequency results in a finite closed loop output impedance at DC, and thus, in a finite output voltage offset (steady state error).

7.6 Analysis and Simulation

Once the shape of the closed loop output impedance has been determined by "doing the algebra on the graph," we can by inspection write the expression for Z_{of}. If $\frac{\omega_0}{Q_L} < \omega_{z2} < \omega_0 = 1/\sqrt{LC_o}$, Z_{of} is drawn with a solid line in Fig. 7.7c, and can be expressed as:

$$Z_{of}(s) = ESR \frac{\left(1+\frac{\omega_z}{s}\right)\left(1+\frac{\omega_0/Q_L}{s}\right)}{\left(1+\frac{\omega_c}{s}\right)\left(1+\frac{\omega_{z1}}{s}\right)\left(1+\frac{\omega_{z2}}{s}\right)}. \tag{7.9}$$

In a special case, when $\omega_{z2} = \omega_0 = 1/\sqrt{LC_o}$, Z_{of} takes the shape shown with the dashed line in Fig. 7.7c, and (7.9) reduces to:

$$Z_{of}(s) = ESR \frac{\left(1+\frac{\omega_z}{s}\right)}{\left(1+\frac{\omega_c}{s}\right)\left(1+\frac{\omega_{z1}}{s}\right)}. \tag{7.10}$$

Substituting (7.9) and (7.10) into (7.6), respectively, and rearranging, we get:

$$V_o(s) = \frac{V_{th}}{s} - \Delta I_o \cdot ESR \frac{(s+\omega_z)(s+\omega_0/Q_L)}{(s+\omega_c)(s+\omega_{z1})(s+\omega_{z2})} \tag{7.11}$$

$$V_o(s) = \frac{V_{th}}{s} - \Delta I_o \cdot ESR \frac{(s+\omega_z)}{(s+\omega_c)(s+\omega_{z1})} \tag{7.12}$$

Equations (7.11) and (7.12) are frequency domain expressions for the converter output voltage during I_3 and I_4. The Mathematica™ software package can be used to calculate the inverse Laplace transform of (7.11) and (7.12) and plot the resulting time-domain converter output voltage behavior during I_3 and I_4. Simulation results for two compensation networks designed to approximate (7.7) and (7.8) are given in Fig. 7.8 by the dashed and the solid line, respectively.

Using Mathematica's built-in inverse Laplace function, predicting and plotting the load transient response of the converter takes only a few seconds compared to several minutes required for a SPICE simulation on a Pentium II 450MHz workstation.

Mathematica is an efficient tool for calculation and plotting of the time-domain transient response. However, doing the task analytically yields significant additional design insight.

Taking the inverse Laplace transform of (7.11) and (7.12) yields time-domain equations for the converter output voltage given by (7.13) and (7.14), respectively.

$$V_o(t) = V_{TH} - \Delta I_o \cdot ESR \cdot (A_1 e^{-\omega_c t} + A_2 e^{-\omega_{z1} t} + A_3 e^{-\omega_{z2} t}) \tag{7.13}$$

$$V_o(t) = V_{TH} - \Delta I_o \cdot ESR \cdot (A_1 e^{-\omega_c t} + A_2 e^{-\omega_{z1} t}) \tag{7.14}$$

where A_1, A_2, and A_3, are constants. Equations (7.13) and (7.14) show that the converter response during I_3 is a function of the loop gain crossover frequency, ω_c, and the compensation zeros, ω_{z1} and ω_{z2}. Furthermore, since $\Delta V_o(t)$ in both (7.13) and (7.14) is a sum of decaying exponential terms, the shape of the transient response can be controlled

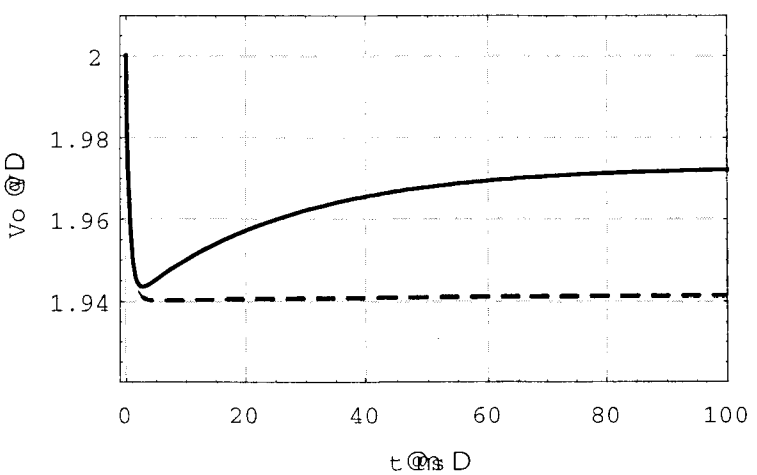


Figure 7.8: Simulated converter transient response during I_3 and I_4

by appropriately adjusting the time constant of each of the exponential terms. In other words, if ω_c, ω_{z1} and ω_{z2} are properly chosen, the transient response can be made to resemble the waveforms in Fig. 7.6. This is actually a mathematical restatement of Fig. 7.7; choosing appropriate time constants is equivalent to shaping the closed output impedance according to (7.7) and (7.8). The added value of (7.13) and (7.14) lies in the opportunity to examine the contribution of each exponential term to the overall transient response and derive closed form expressions for peak voltage deviation.

7.7 Calculating the Peak Voltage Deviation

Equation (7.14) is particularly suitable for obtaining a closed form expression for the peak output voltage deviation during I_3. Finding the peak voltage deviation in this case is equivalent to finding the maximum of the expression to the right of the minus sign in (7.14). Taking the first derivative of this expression, setting it equal to zero, and solving for t yields the time t_{min} at which the output voltage reaches its lowest level:

$$t_{\min} = \frac{1}{\omega_c - \omega_{z1}} \ln\left(-\frac{A_1 \cdot \omega_c}{A_2 \cdot \omega_{z1}} \right). \tag{7.15}$$

Substituting t_{min} back into (7.14), and making the appropriate approximations, we get an expression for the peak output voltage deviation during I_3:

$$\Delta V_5 \approx \frac{\Delta I_o}{\omega_c C_o} \left(\frac{\omega_{z1}}{\omega_c} \right)^{\frac{\omega_{z1}}{\omega_c}} \tag{7.16}$$

7.8 Experimental Verification

Theoretical results were verified on a prototype synchronous buck converter. The input voltage was chosen to be 12V, and the nominal output voltage was 2.0V. A voltage mode feedback loop was designed based on (7.7), (7.8) and Fig. 7.7, and implemented as

shown in Fig. 7.1. The loop was designed for f_{z1}=20Hz, $f_{z2}=\frac{f_0}{Q_L}$=2.7kHz, and f_c=250kHz; the measured crossover frequency was 290kHz. The transient response was measured for a load current step from 0.1 to 15A with a slew rate of 60A/μs and a frequency of 100Hz. A plot of the converter output voltage is shown in Fig. 7.9 on a 50mV/division scale.

Fig. 7.9 shows the worst case peak to peak output voltage deviation due to a 15A load transient to be only 160mV. This deviation is in fact within the static voltage tolerance specified in [11] with only 160μF of output capacitance. The experimental results also verified the validity of (7.16): peak measured deviation during I_3 was 56mV versus 60mV predicted by (7.16) and demonstrated in Fig. 7.8.

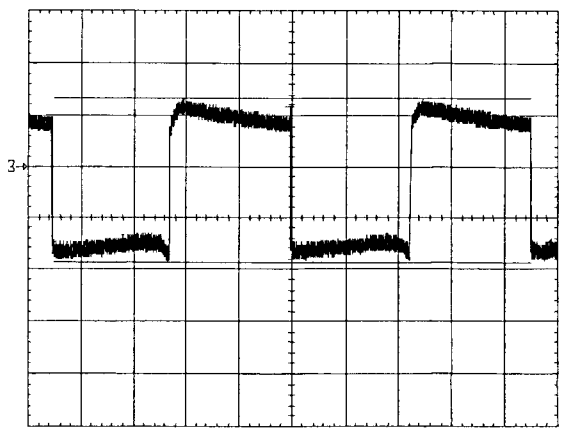


Figure 7.9: The output voltage of the point-of-load module under the worst case transient conditions (load frequency = 100Hz)

7.9 Conclusion

In this paper we have shown how to correlate the desired time domain converter response to a step load current change with the shape of its closed loop output impedance. The closed loop output impedance is then used to determine the optimum shape of the loop gain and thus, the optimum location of the compensation poles and zeros. Since all

relevant equations can be written by inspection, this design-oriented approach doesn't require any lengthy derivations, and offers immediate insight into how each compensation pole and zero affects the transient response of the converter. Thus, the proposed method insures that the desired load transient response can be achieved without time-consuming trial and error loop design using a circuit simulation tool.

The validity of the voltage mode loop design based on the closed loop output impedance was experimentally verified on a prototype buck converter built using exclusively surface mount parts. Tight static voltage regulation and the desired shape of the converter transient response were achieved by proper feedback loop design. A transient response typically available with current mode control schemes was realized with pure voltage mode control. Hence, by eliminating the current sensing resistor the overall efficiency of the module was improved by 2-3% without degrading the transient response.

Chapter 8

Practical VRM Design Example

In this chapter it will be demonstrated how to design an optimized VRM board using the tools developed in the preceding chapters.

8.1 Board Specifications

In this example the following parameters will be assumed:

V_{in}=12V

V_{out}=3V

I_{min}=0.8A

I_{max}=16A

Efficiency at full load: 85%

Load current slew rate = 60A/μs

Peak output voltage deviation: ±90mV

Target Size (L x W x H): 2.6" x 1.5" x 0.3"

8.2 Introductory Remarks

The starting point for the design is the size spec, and the height spec in particular. The specified height immediately rules out the use of electrolytic capacitors at the output.

Therefore, the switching frequency will have to be sufficiently high to allow the transient specs to be met with a limited amount of output capacitance that can be achieved using ceramic chip capacitors.

Furthermore, because of the height limitations, the value of the inductor might have to be limited. As a result, a higher than usual switching frequency might have to be chosen in order to keep the inductor current ripple reasonable.

From the transient response point of view, operating with a high switching frequency and having a small inductor is beneficial because the specs can be met with less output capacitance. In fact, it might be desirable to operate with as high switching frequency as the efficiency specs will allow.

8.3 Power Stage Design

The first in the design process is to perform the preliminary voltage budgeting and check how much output capacitance is needed to achieve transient specs as a function of the switching frequency.

Since the decision has been made to use only ceramic chip capacitors, the voltage spike during the interval I_1 (see Chapter 2) will not be the determining factor in the design because a large number of low ESR and low ESL capacitors will be placed in parallel. Hence, the effective ESR and ESL of the output capacitor bank will be very low, and the voltage drop ΔV_{o1} will not be the limiting factor in the design. Instead, the voltage drop during the intervals I_2 and I_3 will determine how much output capacitance will be needed to meet transient specs.

The peak to peak output voltage deviation due to a worst case load current transient is specified to be 180mV. Obviously, the transient response will be shaped as described in

Chapter 6. Therefore, the peak output voltage deviation during the loading transient can safely be chosen to be 160mV, allowing 20mV of extra headroom. Out of the 160mV, let's allot 80mV to the interval I_2 and 80mV to the interval I_3. Using (3.3) we can plot the capacitance required to achieve ΔV_4=80mV as a function of the switching frequency. The results are shown in Fig. 8.1.

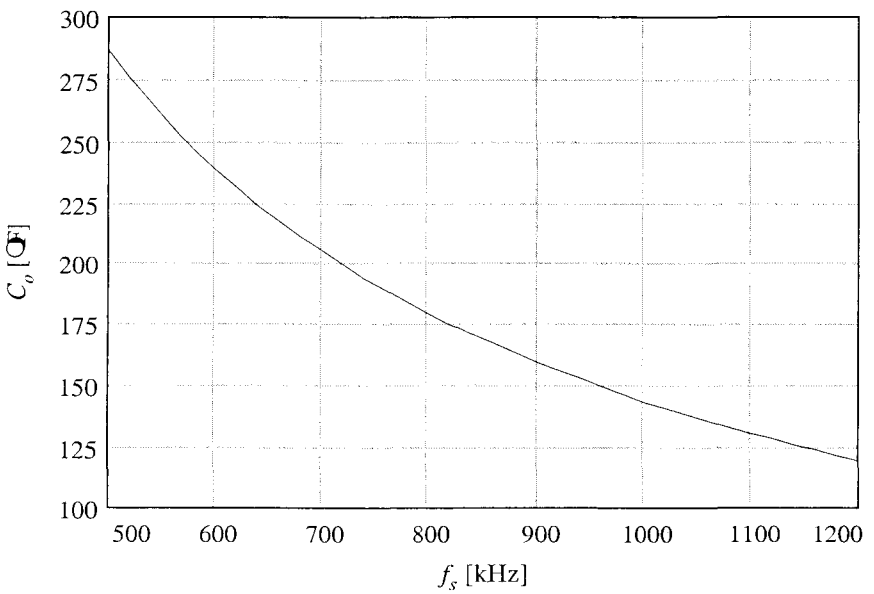


Figure 8.1: Output capacitance required to achieve ΔV_4=80mV as a function of the switching frequency

Similarly, using (3.19) we can plot the capacitance required to achieve ΔV_5=80mV as a function of the switching frequency. The results are given in Fig. 8.2.

The results in Figs. 8.1 and 8.2 show that the voltage drop during the interval I_2 is dominant for this combination of input voltage and output voltage. This is not surprising since the duty cycle is on the order of 25-30%. A load current transient occurring right after the main switch turns off will draw its current from the output capacitors for 70-75% of the switching period causing a significant drop in the output voltage.

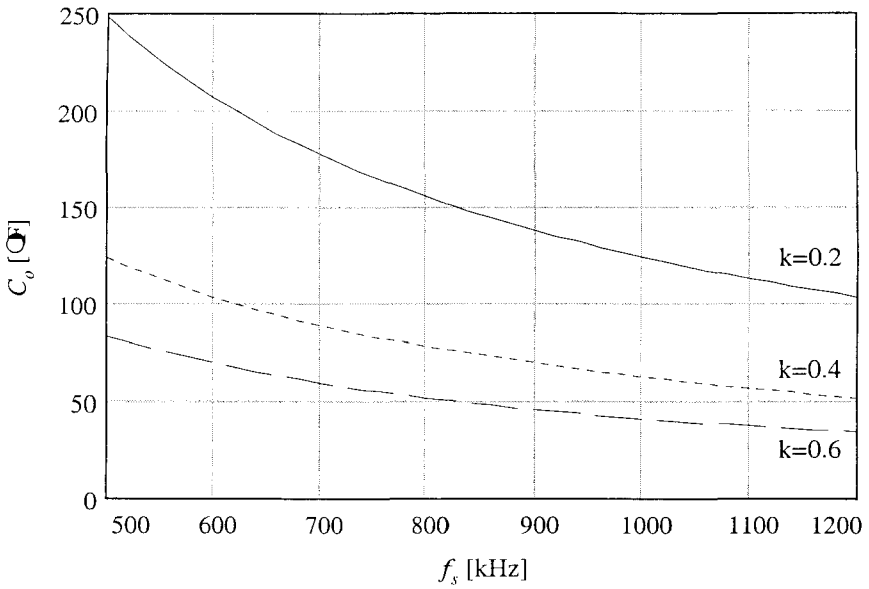


Figure 8.2: Output capacitance required to achieve ΔV_5=80mV as a function of the switching frequency with the inductor current ripple as a parameter

The optimum value of the output capacitance needed to insure that $\Delta V_4+\Delta V_5<160$mV as a function of the switching frequency can be calculated using (3.22). The results are shown in Fig. 8.3.

From Fig. 8.3 it can be seen that the acceptable switching frequency range, in terms of the number of 4.7μF output capacitors that will be needed, is between 800kHz and 1MHz. However, it still remains to be seen whether the efficiency specs can be met at this switching frequency.

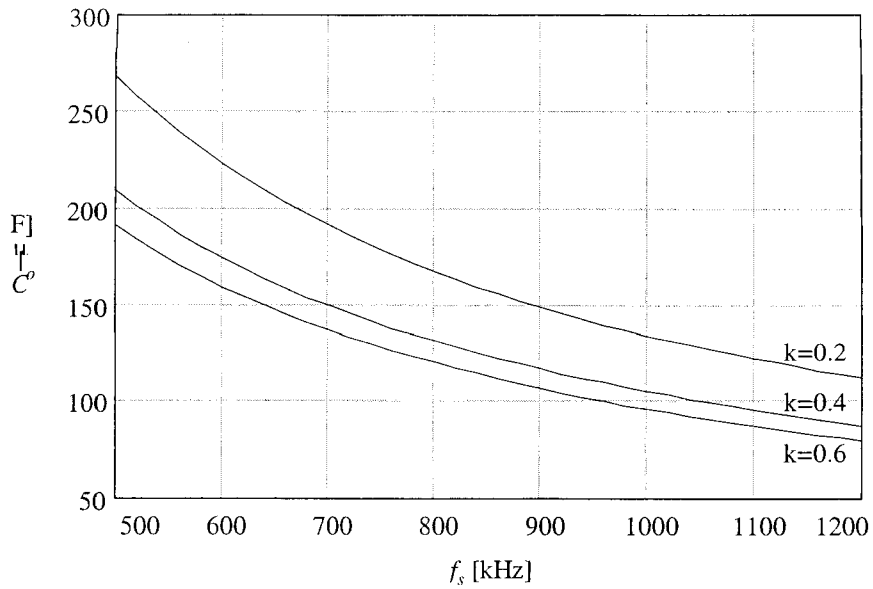


Figure 8.3: Optimum output capacitance required to achieve $\Delta V4+\Delta V5=160mV$ as a function of the switching frequency with the inductor current ripple as a parameter

8.3.1 Choosing the Inductor

The value of the buck inductor has to be small enough to allow a fast transient response and large enough to maintain the inductor current ripple within acceptable limits. A small inductor with a large current ripple is desirable from the transient response point of view. However, a large inductor current ripple increases the *rms* current and increases the current stress on the switches.

For good transient response, it is desirable to have an inductor that will be able to change its steady state current within one switching cycle of the converter. In this case, the load current step is 15.2A. Let's say that we want the inductor to be able to change its load current within 50% of the switching cycle. Then, the value of the inductor has to be less than:

$$L \leq \frac{V_{in} - V_o}{\Delta I_L} \cdot 0.5 \cdot T_s \tag{8.1}$$

Choosing a switching frequency of 900kHz yields a maximum inductor value of 0.32μH. This inductor value results in a peak to peak inductor current ripple of 7.8A, or 49% of the maximum load current.

Having chosen the value of the inductor, we can refer back to Fig. 8.3 to find the amount of output capacitance required to meet transient specs. A value of 120μF is obtained from Fig. 8.3 for $0.4<k<0.6$ and f_s=900kHz. It should, however, be pointed out that 120μF will be enough to meet transient specs in case of an ideal controller that keeps the duty cycle saturated until the output voltage reaches its minimum value. However, this might not be the case. Hence, the capacitance value might have to be adjusted depending on the performance of the control loop.

8.3.2 Switch Implementation

The preliminary design from the transient response point of view has been completed. It now remains to be seen whether efficiency specs can be met with the chosen circuit parameters.

From experience, it would be expected that for the specified input, output voltage, maximum load current, and the chosen switching frequency range, a synchronous buck topology would be more efficient. Nevertheless, this supposition should be verified.

8.3.2.A Choosing the Switches

In order to meet the efficiency specs, the switches have to be chosen very carefully. Since the converter is going to be operated with a switching frequency around 900kHz,

chosen devices have to be state of the art high frequency devices with a low gate charge and a low R_{DSon}.

Given the low duty cycle that the converter will be operated with, the main switch will be on for approximately 30% of the switching period. As a result, the dominant losses in this device will be the gate drive loss and the switching loss. Under the circumstance, it is desirable for this device to be optimized for very low gate charge rather than R_{DSon}. The resulting slightly higher R_{DSon} can in this case be tolerated because the switch is not on for a very long time. On the other hand, a low gate charge reduces the gate drive loss and allows the FET to be turned on faster. If the FET is turned on faster, the voltage-current overlap time at turn on and turn off is reduced (see Fig. 4.2). A reduced overlap time significantly reduces the dominant switching loss. Hence, a FET with the following parameters was chosen for the main switch:

Channel on resistance:	R_{DSon}=20mΩ
Gate charge:	Q_g=15nC @ V_{GS}=5V
Turn on time:	t_{fv1}=6.5ns
Turn off time:	t_{rv1}=7ns
Drain to source capacitance:	C_{DS}=1nF
Package:	SO-8

Unlike the main switch (S_1), the synchronous rectifier (SR) is on for approximately 70% of the switching period. In addition, unlike S1 which has the full input voltage across it at turn on and turn off, the SR has only the body diode forward voltage across it at turn on and turn off. Consequently, the switching losses in the SR are almost negligible. Thus, the turn on and turn off times are not as critical as in the case of S_1. As

a result, it is desirable for this device to be optimized for a low R_{DSon} at the expense of a slightly higher gate charge. A low R_{DSon} will reduce the dominant conduction loss in this device and yield a better overall circuit performance. Thus, a device with the following characteristics has been chosen as the SR:

Channel on resistance:	R_{DSon}=16mΩ
Gate charge:	Q_g=18nC @ V_{GS}=5V
Turn on time:	t_{fvl}=8ns
Turn off time:	t_{rvl}=5ns
Drain to source capacitance:	C_{DS}=1nF
Package:	SO-8

For efficiency comparison purposes, a low voltage Schottky diode with the following characteristics has been selected for the regular buck topology:

Forward voltage drop:	V_f=0.3V at T_j=75°C
Peak forward current:	I_{fmax}=3A
Junction capacitance:	C_j=1.12nF
Reverse leakage current:	I_{leak}=4mA at T_j=25°C; I_{leak}=50mA at T_j=125°C
Package:	SMC

8.3.2.B Switch Efficiency Comparison

Having specified the switches that will be used in the design, we can proceed to compare which switch implementation will give better overall circuit efficiency. Using the formulas given in Chapter 4, we can plot the combined loss in the switches for both topologies as a function of the load current with the switching frequency as a parameter. The results are given in Fig. 8.4.

Previous experience taught us that the power dissipation in the switches would certainly be too high for a single device to handle. As a result, Fig. 8.4 was created based on the assumption that both S_1 and S_2 are implemented either using two devices in parallel (two FETs or two Schottky diodes, depending on the topology) or three devices in parallel. However, the per package dissipation along with size and cost issues will finally determine how many devices will be used.

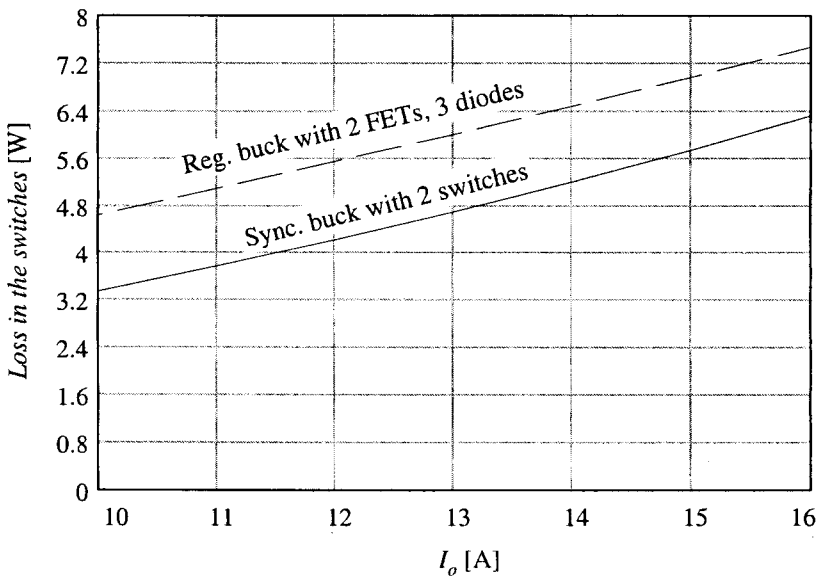


Figure 8.4: Total loss in the switches of the regular and the synchronous buck as a function of the load current

Fig. 8.4 proves that the initial supposition that the losses in the SR would be lower than in the Schottky diode for the specified operating conditions. Furthermore, in order to use the chosen Schottky diode, at least three, and maybe four of these devices will have to be used in parallel, compared to only two SRs. Hence, a regular buck, in this case, is neither a cost-effective nor a size-effective solution. Therefore, a synchronous buck topology is chosen for this application.

8.3.2.C Choosing the Number of Switches

As it was pointed out, Fig. 8.4 was created under the assumption that each switch is implemented using two devices in parallel. Table 8.1 gives the per FET power dissipation depending on the number of devices in parallel for both S_1 and S_2.

	Per FET power Dissipation	
# of Devices in parallel	Q_1	Q_2
1	4.55	4.57
2	1.8	1.35
3	1.11	0.74

Table 8.1: Power loss in the FETs depending on the number of devices in parallel

From Table 8.1 it is clear that, as predicted, it would have been impossible to dissipate 4.5W out of a single SO-8 package. So, a single device is out of the question. Placing two devices in parallel yields more reasonable dissipation numbers. However, it is unlikely that it would be possible to dissipate 1.8W out of an SO-8 package without a heatsink and some airflow.

From the data in Table 8.1, using two devices in parallel might be doable. Using three devices in parallel is safe, but more expensive, and uses more board space. Thus, an attempt will be made to survive with only two devices in parallel for each switch.

8.3.3 Overall Circuit Efficiency

Having almost completed the design of the power stage, we can proceed to check the overall circuit efficiency based on the assumptions we have made so far. Overall circuit

efficiency is shown as a function of the load current in Fig. 8.5. The number of paralleled devices is used as a parameter.

Fig. 8.5 shows that three devices in parallel for each switch will improve the overall circuit efficiency by about 1% at full load compared to the two paralleled devices case. This minor efficiency improvement does not warrant the increase in the size and the cost of the board. Therefore, three devices will not be used in parallel unless it becomes necessary to reduce the per package dissipation.

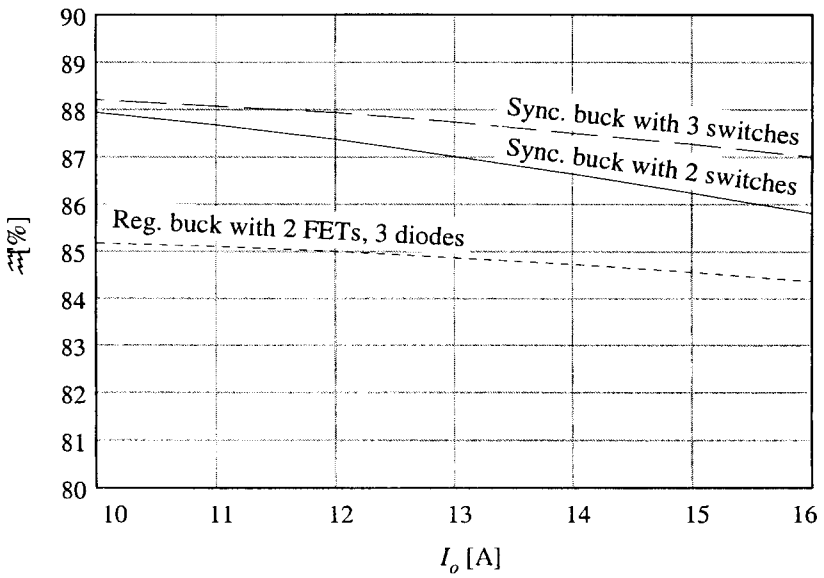


Figure 8.5: Efficiency comparison between the regular and the synchronous buck topology for V_{in}=12V, V_o=3V, f_s=900kHz

8.4 Control Loop Design

The control loop design is going to be based on the ideas outlined in Chapter 6. Therefore, voltage mode control will be used, and the loopgain will be shaped to achieve the optimum load transient response.

Keeping in mind that we had chosen L=0.32μH and C_o=120μF, a double pole will exist in the loopgain at a frequency f_o given by:

$$f_o = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C_o}} = 25.7\text{kHz} \tag{8.2}$$

Since the maximum possible control loop bandwidth is desired, the loopgain crossover frequency, f_c, can be chosen to be 250kHz. It, however, remains to be seen whether this high bandwidth can be achieved with an adequate phase margin.

The control to output transfer function of the buck converter is given by:

$$\frac{\hat{v}_o}{\hat{v}_c} = \frac{V_o}{D} \cdot \frac{1}{1 + \frac{1}{Q} \cdot \frac{s}{\omega_o} + \left(\frac{s}{\omega_o}\right)^2} \tag{8.3}$$

where

$$R_0 = \sqrt{\frac{L}{C_o}} \tag{8.4}$$

$$Q_L = \frac{R_0}{R_l} \tag{8.5}$$

the gain in the forward path is equal to $\frac{V_o}{D}$, or approximately equal to V_{in}. Since V_{in}=12V, the gain in the forward path is 21.6dB. A plot of the control-to-output transfer function is given in Fig. 8.6a.

Based on the discussions in Chapter 6, the loop compensation should be implemented as shown in Fig. 8.6b, resulting in the overall loopgain shown in Fig. 8.6c.

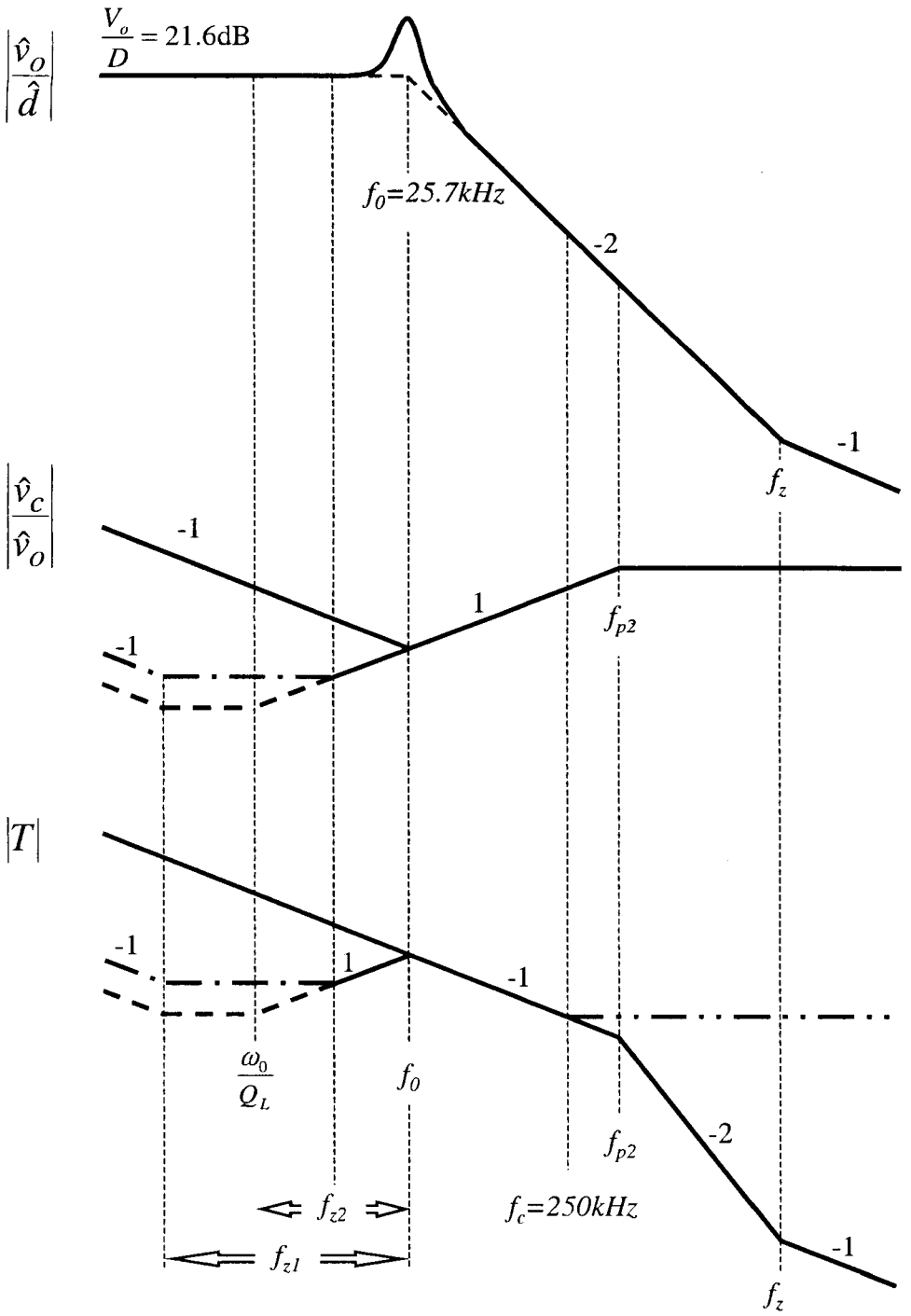


Figure 8.6: Closing the voltage loop: a) duty ratio to output transfer function, b) compensation possibilities, and c) resulting loopgain

8.4.1 Placing Compensation Poles and Zeros

The loopgain crossover frequency has already been chosen to be 250kHz. Given the control-to-output transfer function, the gain in the forward path at f_0 is already 21.6dB. Thus, a full decade in the frequency domain is needed to dump all this gain with a single slope characteristic that we would like to have above f_0. Thus, if f_c=250kHz, the compensation gain at f_0 should be:

$$A_{f=f_0} = \frac{1 \cdot f_c}{12 \cdot f_0} = 0.81 \tag{8.6}$$

A crossover frequency of 250kHz was chosen as a good loop design starting point based on previous experience. Increasing the gain in the compensation path at f_0 beyond 0.81 would lead to a higher crossover frequency and lower closed loop output impedance, both of which would be very desirable from the load transient response standpoint. Unfortunately, however, increasing the gain at f_0, while theoretically possible, cannot be done in practice in this particular case. The reason for this is pretty clear after an examination of Fig. 8.6b. Namely, the gain in the compensation increases with a single slope in the frequency domain from f_0 until f_{p2}. In order to insure a damped transient response, f_{p2} has to be placed far enough above the loopgain crossover frequency. However, in this case, f_{p2} also has to be placed reasonably close to f_c in order to limit the high frequency gain in the compensation. A good tradeoff between these two conditions would be to place f_{p2} at 320kHz. Even so, the gain in the compensation above 320kHz will be 14.3 if the gain at f_0 is one. Thus, all the frequencies above 320kHz, including the switching frequency, will be amplified with a very high gain of 14.3. As a result, the error amplifier will face an output voltage ripple amplified 14.3 times!

The controller chip being used for this application has a triangular ramp with a peak to peak amplitude of 1V. Since the chip uses a triangular ramp instead of a sawtooth, both edges of the ramp can be modulated, somewhat decreasing the response time after a load current transient. On the down side, however, the main switch is not necessarily forced to turn on at the beginning of each cycle. Instead, if the voltage at the comparator input is below the ramp, the main switch never turns on. In addition, because of the propagation delay time through the comparator (~100ns), the comparator will not turn the main switch on even if the signal applied to its input is not below the ramp, but catches the very bottom of the ramp.

Given the low duty cycle, and the amplitude of the signal at the comparator input (14.3 times the output voltage ripple), it is foreseeable that the controller can start to skip pulses and enter subharmonic oscillation at one-half of the switching frequency. In order to remedy the situation, an additional pole might have to be placed at or above one-half of the switching frequency in order to reduce the high frequency gain. However, this pole will reduce the overall phase margin.

Because of the described limitations, the gain in the compensation has to be limited to one at f_0. This limitation imposes a further limitation on the position of f_{z2}, and thus, as explained in Chapter 6, on the shape of the transient response. Namely, since Q=10.8, for ideal load transient response, f_{z2} should be placed at

$$f_{z2} = \frac{f_0}{Q} \approx 2\text{kHz}. \tag{8.7}$$

However, placing f_{z2} at 2kHz would result in an unacceptable loop gain of 1.1 at that frequency. Given the preferred shape of the loopgain shown in Fig. 8.6c, it is clear that with unavoidable component tolerances the loop crossover frequency might end up being

well below 100Hz. This, of course, is contrary to the desire to have a very high bandwidth loop. Hence, f_{z2} has to be above one-sixth of f_0, resulting in a nearly optimum transient response, as described in Chapter 6.

The only thing that is still left to design in the compensation is the location of f_{z1}. Since the minimum load transient frequency is 100Hz, f_{z1} has to be placed far below this frequency to insure that the output voltage doesn't recover to its set point even under these load toggle conditions. Therefore, f_{z1} should be placed around 20Hz.

8.4.2 Circuit Implementation

The compensation designed in the preceding section can be implemented using a very typical compensation circuit shown in Fig. 8.7. Compensation zero and pole frequencies are given by (8.6) through (8.8).

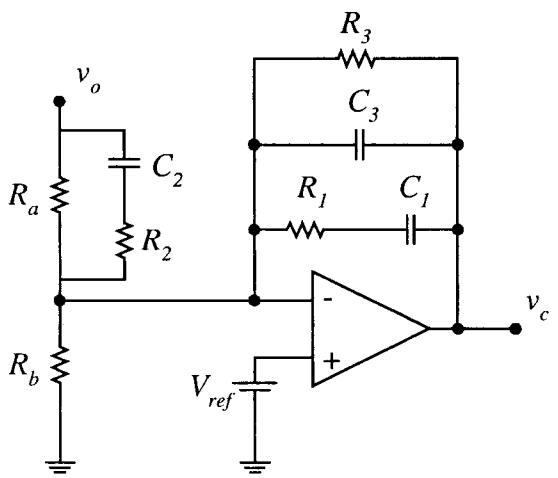


Figure 8.7: Compensation circuit

$$\omega_{z1} = \frac{1}{R_1 C_1} \tag{8.8}$$

$$\omega_{z2} = \frac{1}{R_a C_2} \tag{8.9}$$

$$\omega_{p1} = \frac{1}{R_3 C_1} \tag{8.10}$$

$$\omega_{p2} = \frac{1}{R_2 C_2} \tag{8.11}$$

$$\omega_{p3} = \frac{1}{R_1 C_3} \tag{8.12}$$

The capacitor C_3 and the resistor R_3 are optional, and can be omitted from the circuit. C_3 introduces a pole at f_{p3} that is used to roll off the high frequency gain if the need arises to limit the amplitude of the signal being applied to the comparator input. This pole should be placed at or above one-half of the switching frequency.

The resistor R_3 is used to limit the DC gain. As it was already pointed out, the optimum shape of the loopgain cannot be achieved because of practical limitations. To make up for this, the DC gain can be limited to introduce a slight steady state error and provide a bit of extra headroom for the transient. If it becomes necessary to limit the DC gain, R_3 can be included in the circuit; otherwise, it can be omitted from the compensation all together.

8.4.3 Circuit Simulation

The circuit schematic has been completed. But before proceeding with the PCB design, it is prudent to verify that the loop will be stable and that the desired transient response can indeed be achieved.

8.4.3.A Loopgain Calculation

Loop design is easily verified using the SCAMP program. Fig. 8.8 shows the results of the loopgain calculation using SCAMP. The magnitude plot shows that a loop bandwidth of 199kHz has been achieved; the phase plot shows that a very safe phase margin of 67 degrees has been accomplished. The actual pole and zero locations are given in Table 8.2. Hence, the use of SCAMP allowed us to validate the control loop design and to verify the loop stability.

Pole (Frequency)	Pole (Q)	Zero (Frequency)	Zero (Q)
.26424341E+06	real	.12541761E+02	real
.25764549E+05	.18638449E+01	.58809704E+04	real
.25764549E+05	.18638449E+01	.99471834E+06	real
.16668221E+00	real		

Table 8.2: Compensation pole and zero locations obtained from SCAMP

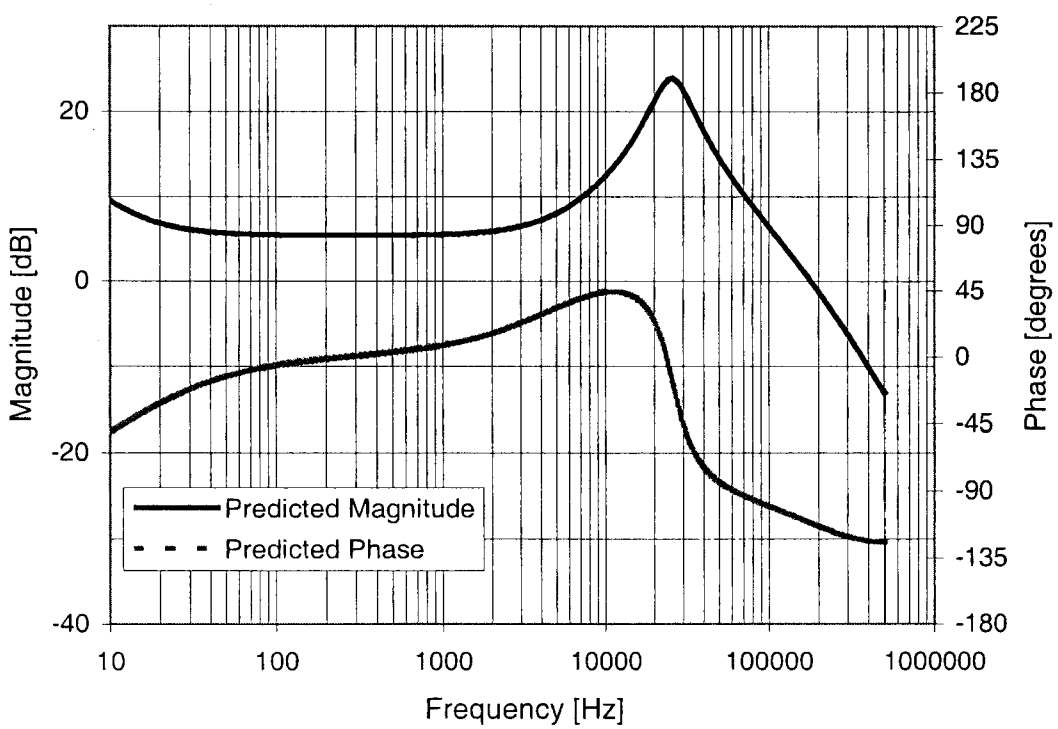


Figure 8.8: Loopgain prediction

8.4.3.B Load Transient Response Simulation

Having completed the loop design, the load transient response can be simulated using MATHEMATICA, as it was described in Chapter 6. Load transient response simulation results are presented in Fig. 8.9.

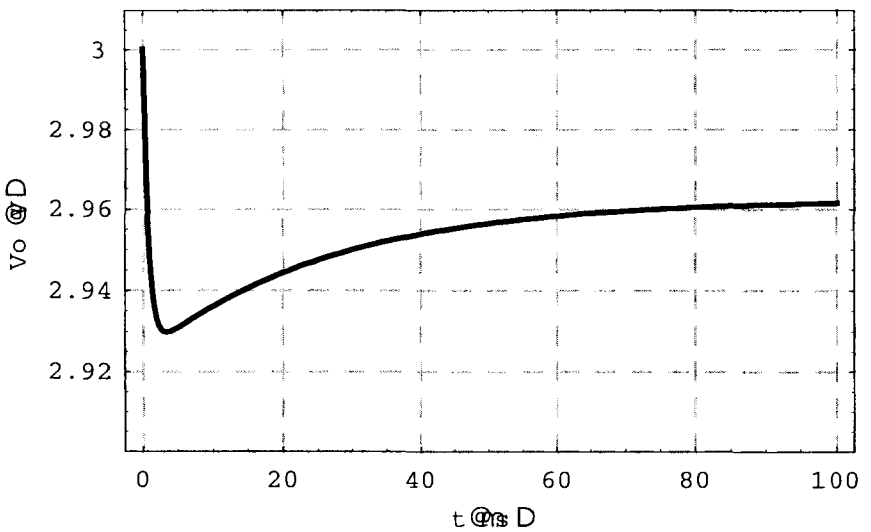


Figure 8.9: Simulated load transient response

Fig. 8.9 shows that with the achieved loop bandwidth, the peak output voltage deviation during I_3 is 70.2mV. This leaves only 90mV of voltage drop available for I_2. From Fig. 8.1 we know that 160μF is required to achieve a maximum voltage drop of 80mV during I_2. Therefore, the chosen output capacitance of 120μF will not be enough to meet transient specs. In other words, the duty cycle will not saturate after the load transient and the formulas derived in Chapter 3 for the voltage drop during I_3 cannot be used to calculate the required amount of output capacitance. Instead Fig. 8.1 should be used in conjunction with Fig. 8.9 to determine the proper value of the output capacitor. From Figs. 8.1 and 8.9 it can be concluded that 160μF of output capacitance will be

enough to meet transient specs. Therefore, the value of the output capacitor has to be increased from 120μF to 160μF.

8.5 Experimental Results

The above paper design was implemented on a four-layer PCB measuring 2.6" by 1.5"; 2oz copper thickness was used on the board. The design rules were 10mill traces with 10mill spacing trace to trace, trace to pad and pad to pad. This board was used to verify that all the design specs have been adequately met.

8.5.1 Circuit Waveforms

After the initial power-up, the first order of business was to check all the waveforms to make sure that the converter is operating properly. The load current was set to 10.5A and the output voltage was measured to be 2.997V. A plot of the inductor current, phase node, and the output voltage is given in Fig. 8.10. The top trace in Fig. 8.10 is the inductor current displayed on a 5A/div scale. The actual inductor current ripple is 9.8A. The middle trace is the output voltage displayed on a 10mV/div scale. The output voltage waveform indicates that the output voltage ripple is 14mV, well within the specified tolerance. The bottom trace in Fig. 8.10 is the phase node on a 10V/div scale. This trace shows a bit more ringing than it would be desirable after the main FET turns on indicating that the board layout could be improved.

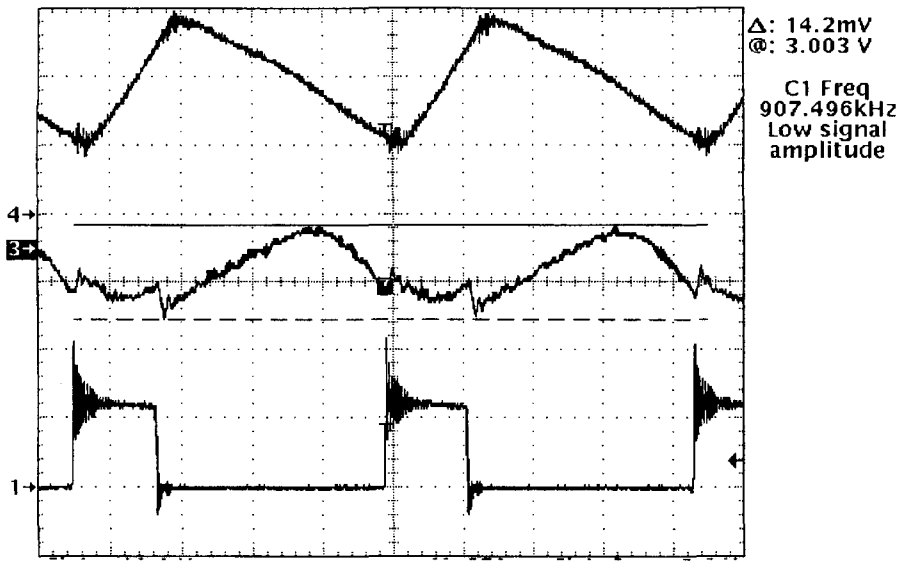


Figure 8.10: Circuit waveforms (Io=10A): inductor current (top), output voltage (middle), phase node (bottom)

Since precise gate drive timing is essential in achieving a high module efficiency, it is very important to insure that the best possible timing has indeed been achieved. In other words, it is important to verify that there is no cross-conduction on one extreme, and that the body diode does not conduct longer than absolutely necessary on the other extreme. The easiest way to check for prolonged body diode conduction is to look at the magnified phase node waveform. A dip in the phase node waveform right after the SR turns off (see Fig. 8.11) or before it turns on (see Fig. 8.12) indicates body diode conduction. No such dips can be identified in Figs. 8.11 and 8.12. Thus, the body diode is not conducting longer than necessary, and the losses associated with the body diode are being kept at bay.

While we know from the phase node waveform in Fig. 8.11 that the body diode conduction is not excessive, we cannot verify that there is no cross-conduction. The best

way to determine whether cross-conduction occurs is to look at the SR current. However, this is not possible on a highly populated surface mount board. One way to measure the SR current would be to add a wire for the current probe. However, this adds a significant amount of inductance and changes the characteristics of the whole circuit. Therefore, this kind of measurement is not valid. Another possibility would be to use a current sensing resistor, but this would again involve altering the board in some way and is, therefore, undesirable. Under the circumstances, we can only look at the gate drive waveforms in conjunction with the phase node waveform in order to determine the performance of the gate drive and determine whether cross-conduction occurs or not.

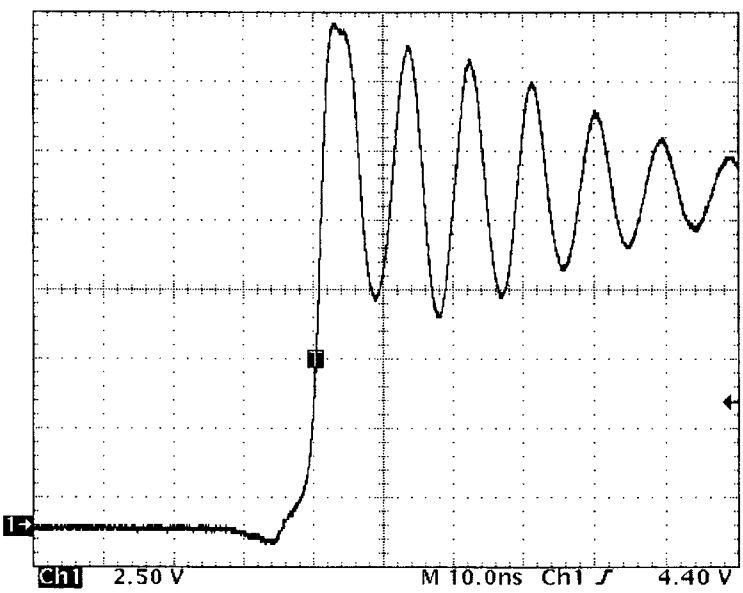


Figure 8.11: Phase node waveform (I_o=10A): detail of the SR turn-off – S_1 turn-on transition

Gate drive waveforms at SR turn off – S_1 turn on transition are shown in Fig. 8.13, along with the phase node waveform (bottom). The scale for all waveforms is 5V/div. Fig. 8.13 reveals that the gate drive timing for this transition as almost perfect, and does

not need to be trimmed in any way because there is no cross-conduction. In fact, the dead time measured from the threshold of the SR to the threshold of S_1 (V_{GS2}=1V to V_{GS1}=1V) is roughly 10ns, which is what the driver design was meant to achieve.

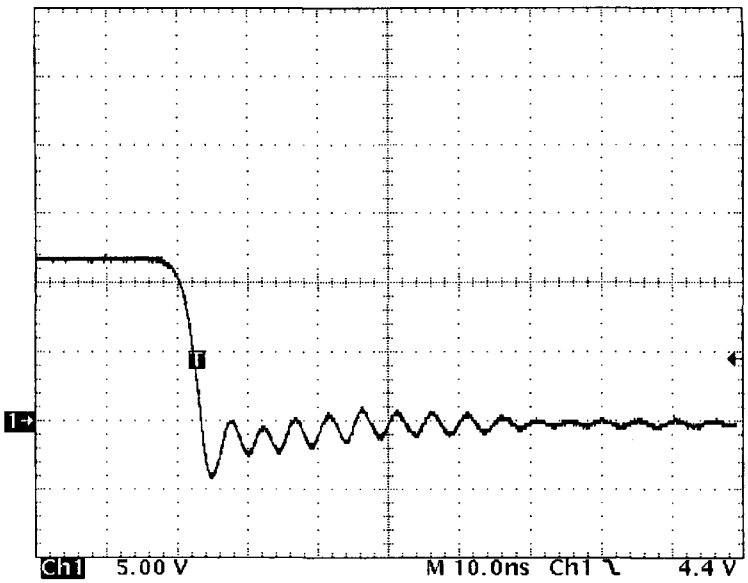


Figure 8.12: Phase node waveform (I_o=10A): detail of the S_1 turn-off – SR turn-on transition

Another critical issue from the efficiency standpoint is how fast S_1 turns on since this affects the dominant switching loss in the device. Fig. 8.13 shows that S_1 turns on in about 8ns at the full load current, which is adequate even for 900kHz operation.

Gate drive waveforms at S_1 turn off – SR turn on transition are shown in Fig. 8.14, along with the phase node waveform (top). The scale for all waveforms is 5V/div. Fig. 8.14 shows that excellent timing is achieved at this transition as well. No cross-conduction occurs, and the dead time is approximately 10ns; the main switch turns off in 7ns. Hence, the gate drive is functioning properly, and no trimming is necessary.

Figs. 8.13 and 8.14 show that the gate drive is truly optimized for high frequency operation. It would be nearly impossible to achieve better timing and still avoid cross-

conduction. The switching times are also very fast, and only slight improvements might be possible by increasing the current capability of the driver. However, increased driver current capability comes with an increased price tag.

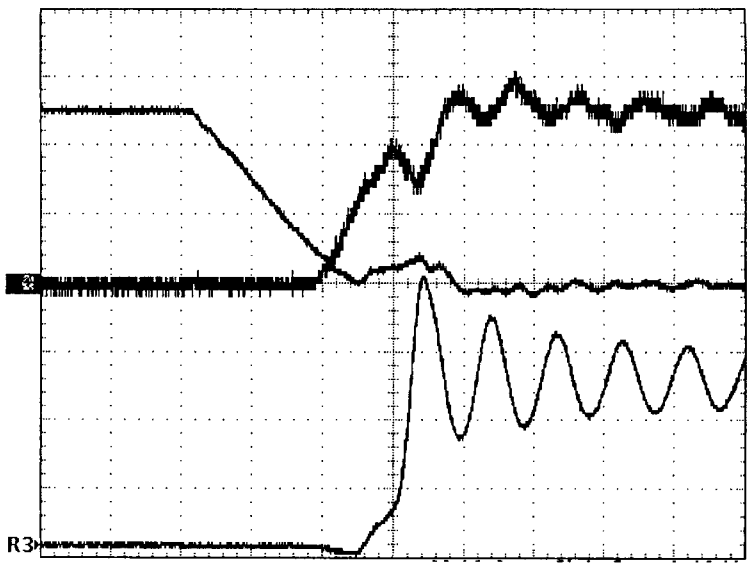


Figure 8.13: Gate drive waveforms (top) for the SR turn-off –S_1 turn-on transition, and phase node waveform (bottom)

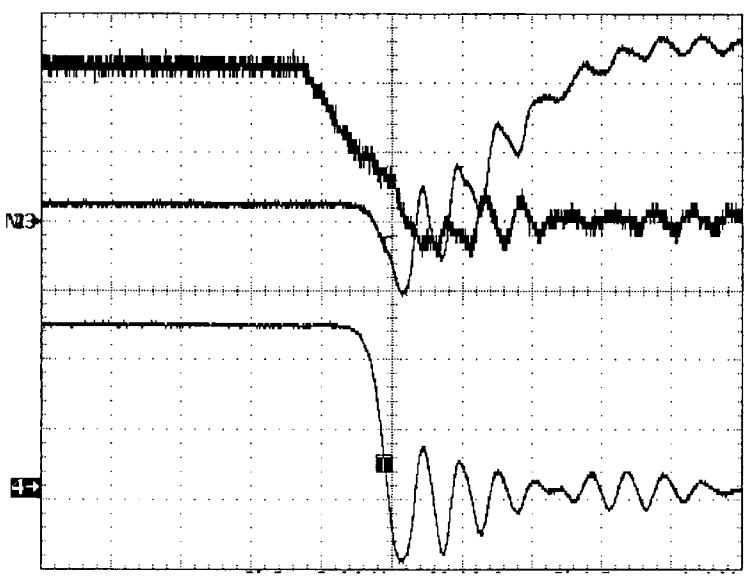


Figure 8.14: Gate drive waveforms (top) for the S_1 turn-off –SR turn-on transition, and phase node waveform (bottom)

8.5.2 Loopgain Measurement

Though it has already been demonstrated that the circuit is stable and working properly, it would be interesting to compare the loopgain prediction with the actual measurement.

Loopgain measurement was performed using an injection transformer to inject a signal into the loop at the output of the converter. While this is not an ideal injection point, it is the only accessible point in the circuit where the signal could be injected into the loop; the preferred injection point, in input of the modulator, is inside the control IC, and is not accessible.

The results of the loopgain measurement are shown in Fig. 8.15. The top trace in Fig. 8.15 is the magnitude, and the bottom trace is the phase. The actual loopgain cross-over frequency is 185kHz; the actual phase margin is 70 degrees.

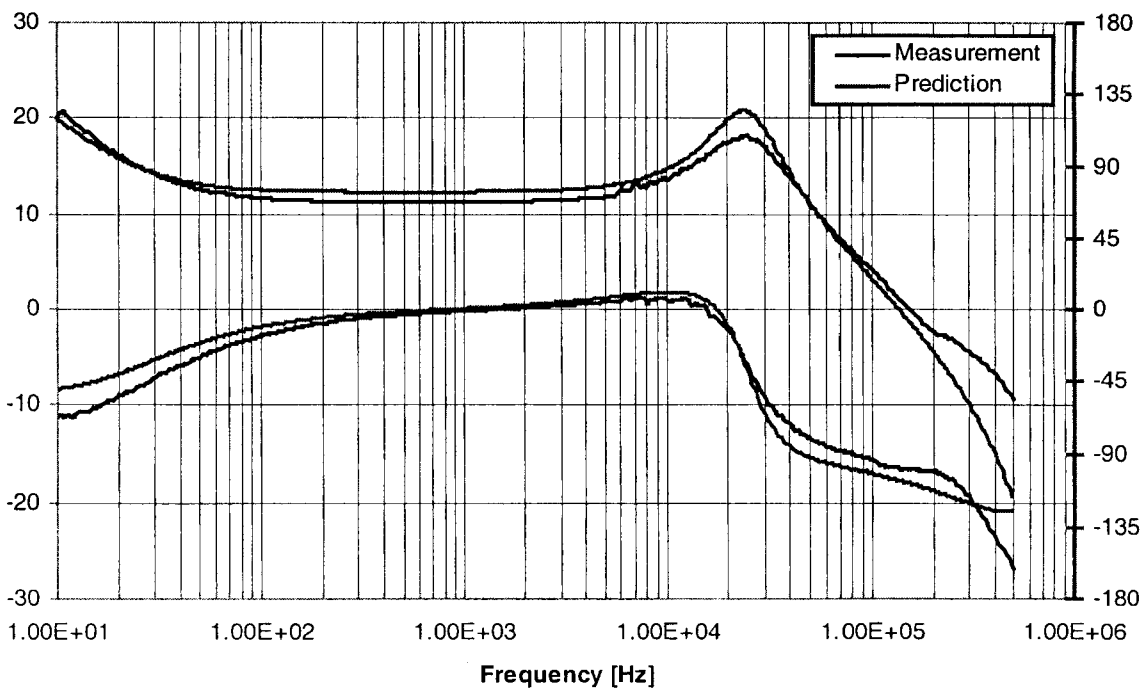


Figure 8.15: Predicted and measured loopgain

Fig. 8.15 shows a remarkably good correspondence between the measured and the calculated loopgain characteristic. Therefore, it is to be expected that the module will perform as predicted by the load transient simulations presented earlier in this chapter. In other words, the module should be able to meet the load transient specifications.

8.5.3 Load Transient Response

In order to test the load transient response, the module was mounted onto an evaluation board using a standard 50-pin AMP connector. The evaluation board was designed to simulate a microprocessor load; the load is switched from 0.8A to 16.1A with a slew rate greater than 60A/μs. The load frequency can be varied from 100Hz to 100kHz.

The board was tested for the entire range of load frequencies. The output voltage for load frequencies of 100Hz, 10kHz, and 100kHz measured at the connector pins is shown in Figs. 8.16, 8.17, and 8.18, respectively.

Fig. 8.16 shows that for the worst case load toggle rate (100Hz), the peak to peak output voltage deviation is 149mV, and is within the specs. When the load toggle rate is increased to 10kHz, the peak to peak output voltage deviation is reduced to 143mV. Finally, at the maximum load toggle frequency, the peak to peak output voltage deviation is 161mV.

Figs. 8.16 through 8.18 show that the module meets or exceeds load transient specs in the entire specified load toggle frequency range.

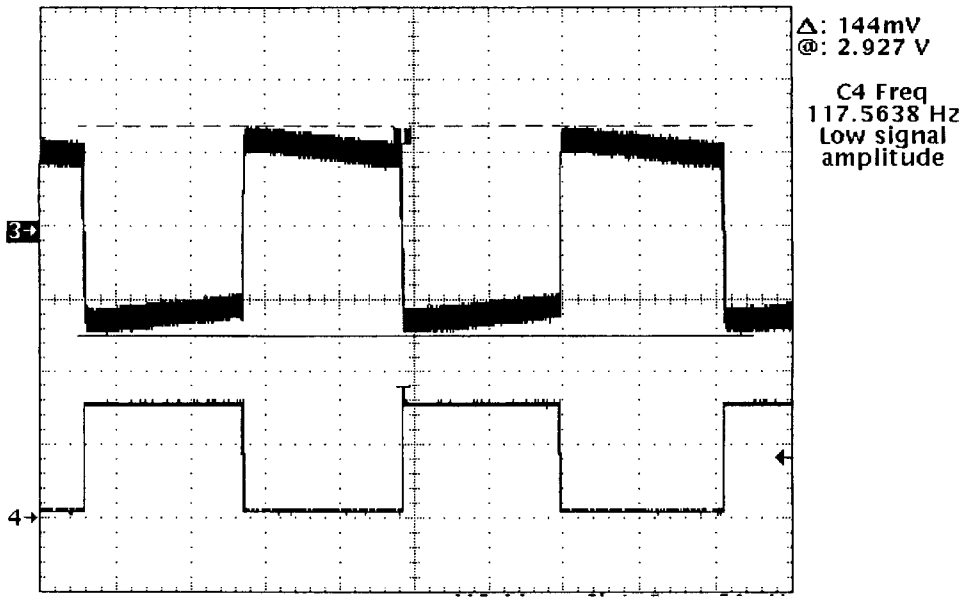


Figure 8.16: Load transient response to a 15.1A current step with a slew rate of 60A/μs: output voltage (top) and load current (bottom)

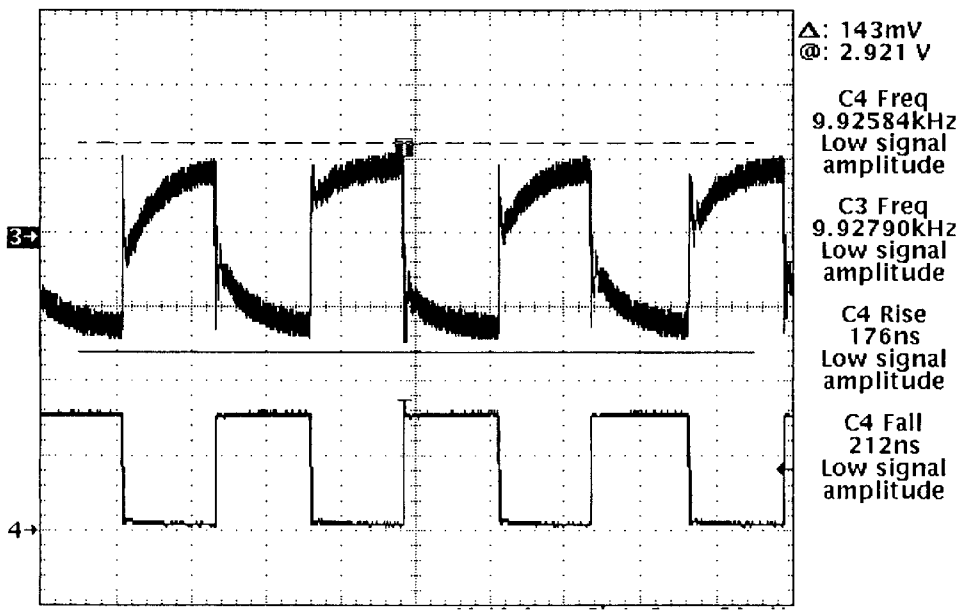


Figure 8.17: Load transient response to a 15.1A current step with a slew rate of 60A/μs and a frequency of 10kHz: output voltage (top) and load current (bottom)

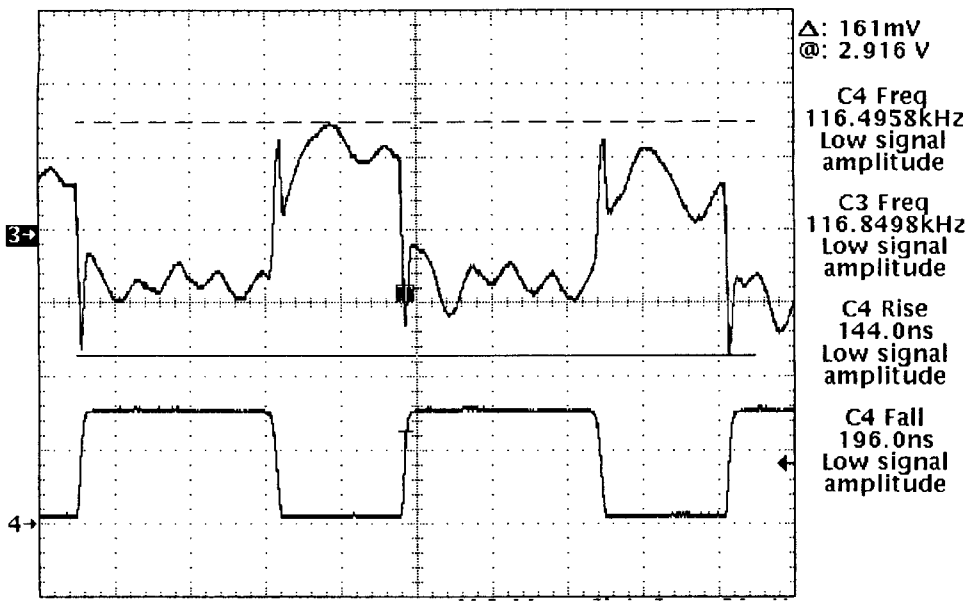


Figure 8.18: Load transient response to a 15.1A current step with a slew rate of 60A/μs and a frequency of 10kHz: output voltage (top) and load current (bottom)

8.5.4 Efficiency Measurements

The efficiency of the module was measured with the board mounted onto the evaluation board. The efficiency was measured for V_{in}=12V, V_{out}=3V, f_s=900kHz. Since the drive circuitry was powered from a separate 5V power supply, gate drive losses have been measured separately. In this way, efficiency measurements yield both the power stage efficiency as well as the overall circuit efficiency that includes the drive losses. Power stage efficiency and the overall circuit efficiency including drive losses are given in Fig. 8.19.

Fig. 8.19 shows that the power stage efficiency at the lightest load (0.8A) is 66.1%, and the overall circuit efficiency is 59.9%. At minimum load, the 380mW of total drive

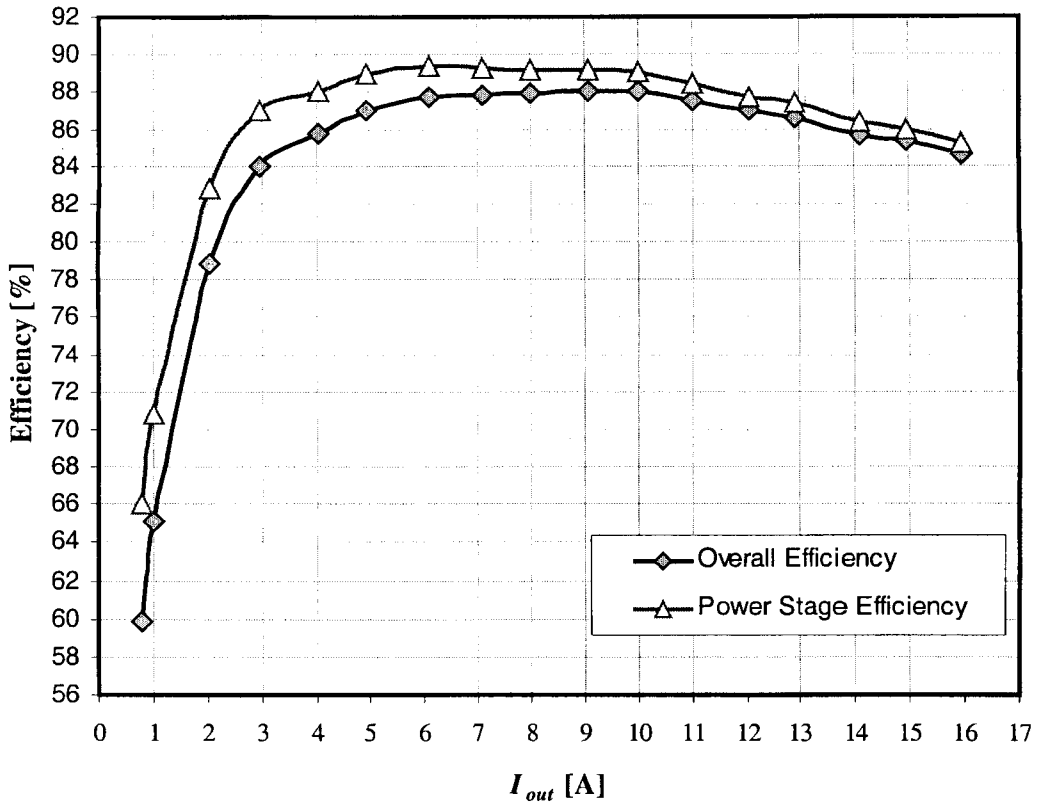


Figure 8.19: Measured VRM module efficiency

loss degrades the efficiency by approximately 6%. However, the overall circuit efficiency is well within the specified efficiency at minimum load (40%).

Measured power stage efficiency at full load (16A) is 85.2%, while the overall circuit efficiency is 84.6%. Thus, the efficiency at full load just misses the spec (85%). However, minor adjustments and switching frequency trimming can easily bring the efficiency at full load within specs.

The measured overall efficiency at full load is 1.1% lower than predicted by Fig. 8.5. Overall, however, the efficiency prediction was quite accurate. The numbers used in the prediction were based on previous experience and an educated guess about the actual

parasitic board trace resistance. A slightly higher parasitic resistance can easily account for the efficiency calculation error.

8.5.5 Physical Dimensions

As it has been shown in preceding sections, the optimized module meets all electrical specifications. The real story, however, is in the achieved dimensions. The achieved dimensions and the specs are given in Table 8.3.

	Intel Specifications [inches]	Optimized Board Size [inches]
Length	3.1	2.6
Width	1.5	1.5
Height	1.1	0.3

Table 8.3: Specified and actual board dimensions

From Table 8.3 we notice that the length of the board is 1.2 times smaller than what was specified. Similarly, the height of the board is 3.66 times smaller than the spec. Hence, the optimized board meets all electrical specs in a 4.4 times smaller volume than specified! The resulting power density exceeds $40W/in^3$.

8.6 Concluding Remarks

Optimization methods developed throughout this thesis have been utilized in this chapter to demonstrate how to design a synchronous buck VRM optimized for the smallest volume. Significant size reduction in comparison with the specs is achieved by choosing right topology, using an optimized gate drive circuit, and designing an optimized, high bandwidth control loop. The result is a VRM shown in Figs. 8.20 and

8.21. Fig. 8.20 shows the dimensions of the module, and Fig. 8.21 demonstrates the module mounted onto the evaluation board.

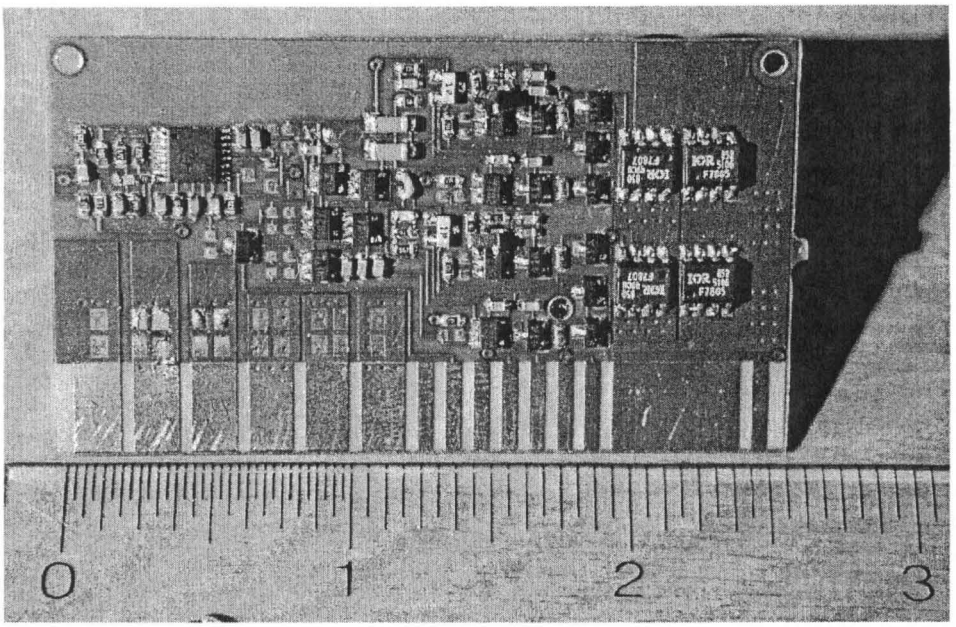


Figure 8.20: Optimized VRM module

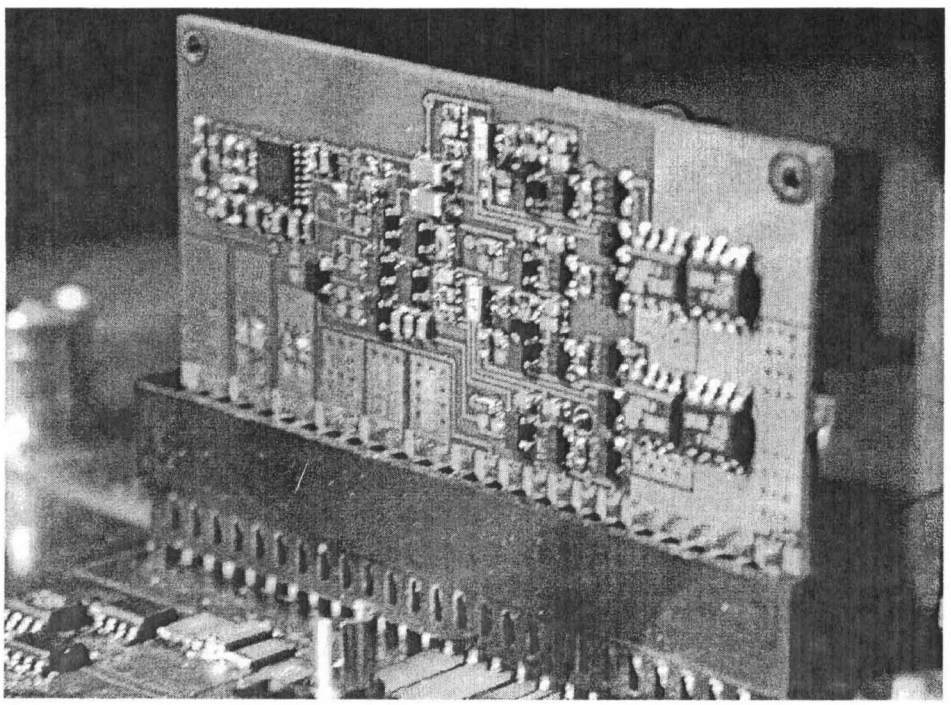


Figure 8.21: VRM mounted onto the evaluation board

Through careful optimization, the module in this example has a peak to peak transient output voltage deviation of less than 160mV, an efficiency of 85% at full load, a volume 4.4 times smaller than the Intel spec, and a power density that exceeds $40W/in^3$.

Chapter 9

Conclusion

This thesis deals with the optimization of Intel Pentium microprocessor power supplies for performance, size and cost, with the emphasis on size. Pentium microprocessors require a very stable and tightly controlled core supply voltage in order to reliably operate at their correct clock frequency. The core supply voltage has to remain within the prescribed window during normal operation, as well as during power-up and power-down when the processor current can change from almost zero to 16A or more in 200-300ns. Maintaining tight processor voltage regulation during these current transients can be difficult to accomplish in a very small volume because the amount of capacitance that can be placed on the output of the power supply to keep the processor supply voltage within specs is limited.

Since the size of the power supply is a major concern, a new approach to meeting the transient response specs in a smaller volume is introduced. Namely, instead of relying on bulky output capacitors to do the majority of the work in keeping the output voltage within specs after a load current transient, the idea is to make the converter and its high bandwidth control loop respond quickly to the processor's rapidly changing current demands. The way to achieve this goal is to efficiently operate at a high switching

frequency. A high switching frequency allows the reduction of both the physical size and the value of the magnetic components. A smaller value of the inductor, in turn, contributes to faster transient response, thus allowing the size of the output capacitors to be reduced. Hence, operating at a high switching frequency can lead to excellent transient response being achieved in a small volume. The only drawback of operating at a high switching frequency is the reduced efficiency of the power supply and more difficult thermal management.

Given the size reduction possibilities offered by a high switching frequency, an effort was made to minimize the efficiency penalty. The losses in a buck topology were carefully calculated in order to find the best switch implementation in each case. It turned out that in systems with a 5V bus, the regular buck proved to be a better solution. However, in systems with a 12V bus, the synchronous buck was the better choice. Efficiency calculations were successfully experimentally verified. Once the validity of the equations was proven, they became a valuable design tool for future modules.

The loss distribution in a buck topology obtained during the efficiency calculations proved to be helpful in two ways: First, it provided an accurate component level power dissipation that is very helpful in designing the package size and the number of devices that will need to be used. Second, the loss distribution pointed out all the efficiency bottlenecks.

The component level loss distribution identified the body diode of the synchronous FET in the buck topology as a major loss mechanism at high frequency. Having become aware of the severity of the problem, a new gate drive circuit was developed to reduce the

loss in the body diode. The new driver successfully eliminated most of the losses associated with the SR body diode through very precise gate signal timing.

Finally, a new way to close the voltage mode loop was proposed in order to be able to meet transient specs with less output capacitance. The unusual compensation method yields a transient response typically available with current mode control schemes without the efficiency penalty introduced by the current sensing resistor.

In short, every aspect of the power supply has carefully been analyzed and optimized through the size prism: the topology, the control algorithm, the drive circuitry, and the components. Design and optimization tools were developed, and theoretical calculations were verified in hardware. The result of the optimization is a microprocessor power supply that meets Intel Pentium III electrical performance specs in approximately one-fifth of the specified volume, resulting in a power density of roughly $40W/in^3$.

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