New Developments in Single Phase Power Factor Correction

Thesis by

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To my family

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Abstract

Power Factor Correction (PFC) is a necessary feature of many AC/DC Power Electronics products. The issues of increasing the value of the Power Factor (PF) and increasing efficiency of transferring the power in such applications motivated this thesis.

Input rectification is needed for the most topologies in AC/DC applications for these topologies to perform however, it is pretty much one of the main causes of distortions and power losses. Diode bridge is also one the hottest components of PFC, which is an important issue in terms of thermal management.

New approach for Power Factor Correction is introduced in the first part. Topologies with bipolar gain characteristics are proposed to be used, naturally providing constant DC output from non-rectified AC input. Practical design of such converter is presented and analyzed, theoretical predictions are confirmed by experimental data; proposed idea of Power Factor Correction is verified.

Another new general approach of Power Factor Correction improvement is introduced in second part. Idea of shifting input line rectification to switching elements of the power stage is proposed for certain topologies and verified on practical example. Key features are analyzed and illustrated by experimental data. This class of converters presents an opportunity for accurate comparison with related conventional topologies, which is included to show the advantages of the new approach.

General advantages and improvements of Power Factor value in bridge-less topologies in comparison to conventional converters are analyzed and illustrated experimentally in the third part of the thesis.

Contents

Part 1

New Power Factor Correctors, Topologies with Bipolar Gain

Chapter 1

1 Introduction

Modern power transfer from AC line to DC output includes having input characteristics that satisfy certain standards. *Power Factor Correction* (PFC) is important and often necessary for such applications. Same time, designers try to implement these circuits with as high efficiency as possible, satisfying other specified parameters.

High value of the *Power Factor* (PF) and low value of *Total Harmonic Distortions* (THD) are important since introduced noise from power supplies can affect operation of other power consumers, and even electronic devices that are not collected to the power line. The general problem is called *Electro Magnetic Interference* (EMI), which includes conducted and radiated interference. Shielding, proper grounding and elimination of EMI at its origins are standard ways to deal with radiated component; filtering and Power Factor Correction are used to decrease conducted EMI.

Power Factor Correction is also important from efficiency point of view. It will be shown below that if input current of the power supply has different harmonics in its spectrum that are not related to spectrum of input voltage, then it leads to power dissipation which occurs in conducting wires and parasitic resistances of the components of power distribution system.

The following chapters will introduce necessary definitions and conventional methods for power factor correction.

Related standards for the acceptable distortions are developed and enforced, making power factor correction pretty much a standard feature in AC applications. This thesis

presents new developments in this area. Part 1 introduces a new approach of PFC on the basis of so called topologies with bipolar gain characteristics, which allows eliminating standard feature of conventional circuits - input rectification.

From the point of view of two main design objectives (PFC and efficiency): input diode bridge is quite undesirable. Input rectification is needed for the most topologies in AC/DC applications for those topologies to perform however, it is pretty much one of the causes of distortions and power losses.

Circuits without input rectification have been developed [4-8]. Different classes of such circuits can be synthesized. There are circuits that implement an idea of having two parts of the circuit, or sometimes two whole converters, with each of them dedicated to working during either positive or negative halves of line period. This approach obviously affects the complexity and cost [7,8]. Our objective is therefore to look for those schematics that accomplish the same objectives with minimum increase in cost and number of components.

One approach is to incorporate line rectification directly into converter (on its primary if isolation is present) by appropriate circuit modification or developing a topology with rectifying features built in. For example, circuit illustrated in [6] shows high efficiency and good performance. However, the output voltage has to be at least twice the voltage used in conventional topology, which is considered a main disadvantage.

Another approach is to modify the existing converters by incorporating the rectification on the secondary side. In that case the diodes on the secondary perform both high frequency as well as line frequency (60Hz) rectification. These circuits usually require four quadrant switches and some topological modifications. Flyback derived

circuit in [5] was only computer simulated and had extra diodes on the low voltage – high current side in comparison to traditional topology, which will definitely decrease the efficiency. Related general idea with better results and new Power Factor Corrector will be illustrated in Part II of this thesis.

Other class of AC/DC circuits is presented in Part I. The basic idea is that in order to get DC output (for example positive) from non rectified AC input, topologies with specific gain characteristics can be considered. If some topology has positive and negative parts of gain characteristics (i.e., it can produce positive or negative output voltage from just positive input): then it can produce strictly positive output voltage from any (positive or negative) input. Such topologies will be called Topologies with Bipolar Gain characteristics (TBG), as proposed by the author in [9]. If suitable control is found, then such topology can implement PFC as well, and therefore produce positive DC output from non rectified AC input.

It is necessary to point out that although some particular example will be analyzed in this part of the thesis, and experimental results will be presented for that circuit in greater detail, the idea is general and other topologies and control circuits can be used and will be discussed.

Chapter 2

General Definitions

This chapter reviews the main quantities and definitions that are used in Power Electronics area, especially related to Power Factor Correction. These terms and quantities will be often used in the following text, analysis and derivations of new expressions and parameters, so it is important to provide a quick reference in case one is needed.

Function *f(t)* is defined as *periodic function* with a period (time interval) T if it satisfies the following equation:

$$f(t) = f(t+T) \tag{2.1}$$

The *average of function f(t)* on the time interval T is defined as

$$< f(t) >= \frac{1}{T}\int_0^T f(t)dt \tag{2.2}$$

Periodic function *f(t)* can be expressed in *Fourier series*:

$$f(t) = a_0 + \sqrt{2}\sum_{n=1}^{\infty}\left[a_n \cos(n\varpi t) + b_n \sin(n\varpi t)\right] \tag{2.2}$$

where

$$a_0 = \frac{1}{T}\int_0^T f(t)dt \tag{2.4}$$

$$a_n = \frac{1}{T}\int_0^T f(t)\cos(n\varpi t)dt \tag{2.5}$$

$$b_n = \frac{1}{T}\int_0^T f(t)\sin(n\varpi t)dt \tag{2.6}$$

Another (alternative) form of *Fourier series* expansion is often used:

$$f(t) = c_0 + \sqrt{2}\sum_{n=1}^{\infty}\left[c_n \sin(n\varpi t + \varphi_n)\right] \tag{2.7}$$

where

$$c_0 = \frac{1}{T}\int_0^T f(t)dt \tag{2.8}$$

$$c_n = |k_n| \tag{2.9}$$

$$\varphi_n = \arg(k_n) \tag{2.10}$$

$$k_n = \frac{1}{T}\int_0^T f(t)e^{-jn\varpi t}dt \tag{2.11}$$

There is a relation between coefficients in both versions of the Fourier expansion

$$c_0 = a_0 \tag{2.12}$$

$$k_n = ja_n + b_n \tag{2.13}$$

Fourier expansion in (2.7) form is convenient because it has a single term for each frequency and they are called "harmonics"; term with n=1 is called fundamental and has particular importance. Coefficients c_n have a meaning of rms value for each component, the definition of "rms value" follows.

Root-mean-square (rms) value of the periodic function *f(t)* is defined as

$$F_{rms} = \sqrt{\frac{1}{T}\int_0^T f^2(t)dt} \tag{2.14}$$

It can be shown that rms value F_{rms} of the periodic function *f(t)* relates to coefficients in Fourier expansion of that function by *Parseval's theorem* (2.15).

$$F_{rms} = \sqrt{\sum_{n=0}^{\infty} c_n^{\,2}} \tag{2.15}$$

AC voltage in power line is never ideal sine wave it usually has some kind of distortions. Current can also be distorted and its waveform can differ from the shape of voltage waveform depending on the load characteristics. It can be stated though that when application circuits reach steady state (in other words, the transient is over) - waveforms are periodical (although might be non sinusoidal), so the following expressions are correct for rms values of voltage and current:

$$V_{rms} = \sqrt{\sum_{n=0}^{\infty} V_n^{\,2}} \tag{2.16}$$

$$I_{rms} = \sqrt{\sum_{n=0}^{\infty} I_n^{\,2}} \tag{2.17}$$

V_n and I_n terms have a practical meaning, they present information about rms components of the waveforms at different harmonics. It will be shown in the next chapter that this information is very useful for understanding how to improve the Power Factor, which is the quantity of how efficient the energy is transferred to the load.

Chapter 3

Introduction of the Power Factor

Consider an arbitrary voltage source in Fig. 2.1, which supplies current to the arbitrary load. There is a quantity to describe the energy transfer.

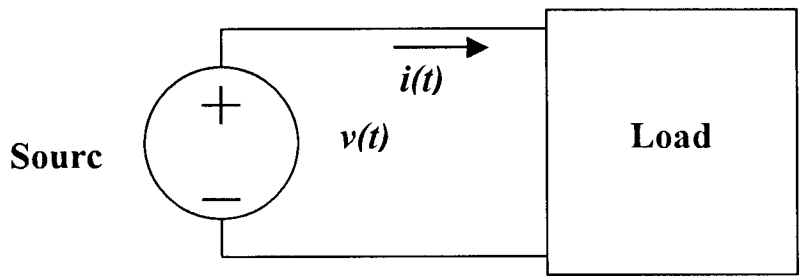

Figure 3.1: Energy transfer from the source to the load

Power Factor (PF) is a parameter that shows how effectively energy is transmitted to the load. The energy transfer is understood to be under arrangement in Fig. 2.1. PF is defined formally as:

$$PF = \frac{< P >}{V_{rms} I_{rms}} \tag{3.1}$$

where <P> is an *average power*; also called *real, true, or active power*.

$$< P >= \frac{1}{T}\int_0^T v(t)i(t)dt \tag{3.2}$$

Sometimes the product $V_{rms}I_{rms}$ is called *apparent power S,* or Volt-Amperes (VA). It can be shown that PF is always in the interval between zero and one.

The average power can be derived in more details. First, express the voltage *v(t)* and current *i(t)* in Fourier series:

$$< P >= \frac{1}{T}\int_0^T v(t)i(t)dt \tag{3.3}$$

$$v(t) = V_0 + \sqrt{2}\sum_{n=1}^{\infty}[V_n \sin(n\varpi t + \varphi_n)] \tag{3.4}$$

$$i(t) = I_0 + \sqrt{2}\sum_{n=1}^{\infty}[I_n \sin(n\varpi t + \theta_n)] \tag{3.5}$$

The following expression will be used for further derivation:

$$\int_0^T V_n \sin(n\varpi t + \varphi_n) I_m \sin(m\varpi t + \theta_m) = \begin{cases} 0, & if \quad n \neq m \\ \frac{V_n I_n}{2}\cos(\varphi_n - \theta_n) & if \quad n = m \end{cases} \tag{3.6}$$

the average power can then be derived as following:

$$< P >= \frac{1}{T}\int_0^T v(t)i(t)dt = V_0 I_0 + \sum_{n=1}^{\infty} V_n I_n \cos(\varphi_n - \theta_n) \tag{3.7}$$

Two important particular cases that have practical importance will now be considered: first one is when voltage has an arbitrary waveform and load is linear resistive; second case is when voltage has sine wave waveform, nonlinear dynamic load.

When load is linear resistive R, the current harmonics are in phase with, and proportional to, the voltage harmonics. Magnitudes and phases of current harmonics are

$$I_n = \frac{V_n}{R} \tag{3.8}$$

$$\theta_n = \varphi_n \tag{3.9}$$

where θ_n is a phase of nth current harmonic, and φ_n is a phase of nth voltage harmonic.

Then it can be concluded that

$$I_{rms} = \sqrt{\sum_{n=0}^{\infty} I_n^{\,2}} = \sqrt{\sum_{n=0}^{\infty} \frac{V_n}{R}} = \frac{V_{rms}}{R} \tag{3.10}$$

The average power from (3.2) is then

$$< P >= V_0 I_0 + \sum_{n=0}^{\infty} V_n I_n \cos(\varphi_n - \theta_n) = \frac{V_{rms}^{\ 2}}{R} \tag{3.11}$$

This result can be used in equation for the power factor, and it shows that PF=1 (the maximum) in case of arbitrary voltage waveform and linear resistive load.

In case of sine-wave voltage waveform ($V_{rms}=V_1$) and nonlinear dynamic load, it can be noticed that

$$< P >= V_1 I_1 \cos(\varphi_1 - \theta_1) \tag{3.12}$$

The result is logical, since only one (first) harmonic is present in voltage waveform.

The following result is valid if the voltage waveform is sinusoidal, as well as current waveform. Assume that voltage sine wave has 0 phase, then phase of the current sine φ will be exactly the phase difference between voltage and current sinusoids to simplify the picture; see example in Fig. 3.2 and Fig. 3.3. Fig. 3.2 shows example of such circuit.

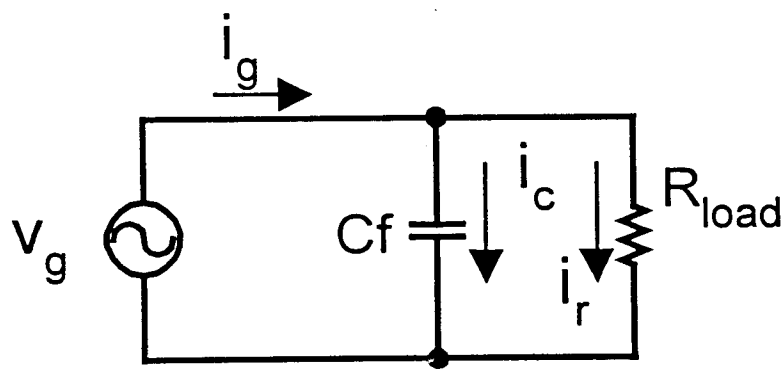

Figure 3.2: Schematic example for the case of the load with reactive component

Current from the voltage source $i_g(t)$ has two components: resistive $i_r(t)$ which is in phase with applied voltage $v_g(t)$, and reactive $i_c(t)$ which has +90 degrees phase shift in

the reference to applied voltage, Fig. 3.3. As a result, the current $i_g(t)$ has a phase φ and only fundamental component.

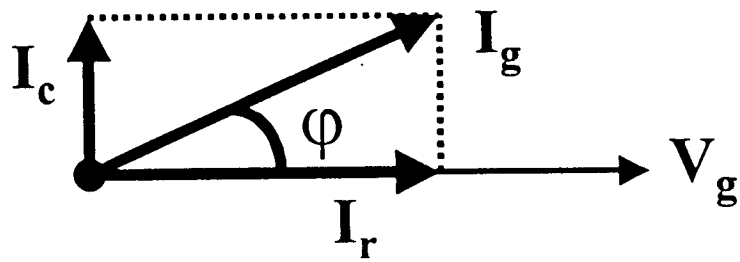

Figure 3.3: The phase diagram of the currents for the circuit in Fig.3.2

Average power is then

$$< P >= V_1 I_1 \cos\varphi \tag{3.13}$$

and since $V_{rms}=V_1$ and $I_{rms}=I_1$ - power factor is found from 3.1 as

$$PF = \cos\varphi \tag{3.14}$$

Clearly, the power factor will reach unity if the load current has zero phase difference from the phase of voltage sine wave.

More generally - current does not have to have only one fundamental harmonic but can be expressed as $I_{rms} = \sqrt{\sum_{n=0}^{\infty} I_n^2}$. It is clear that harmonics do increase the rms value of the current, but do not contribute to the power transfer to the load (from equation (3.12)). However, any series resistive elements (parasitics) will cause additional losses due to every harmonic that is present in current waveform, as well as first (fundamental) one.

Power factor can be then written as (3.15)

$$PF = \frac{< P >}{V_{rms} I_{rms}} = \frac{I_1}{I_{rms}} \cos(\varphi_1 - \theta_1) \tag{3.15}$$

The term $\cos(\varphi_1 - \theta_1)$ is usually called *displacement factor*; it represents the phase difference between fundamental components of the voltage and current. AC voltage is close to sinusoidal in most practical cases, distortions are to be minimized, so it practically means that power factor can be increased if fundamental component of the current is as much in phase with the voltage as possible.

The term $\frac{I_1}{I_{rms}}$ is called *distortion factor*. It shows how big the difference is between fundamental component of the current and actual current waveform.

Parameter of *Total Harmonic Distortion* (THD) is often used; it is defined as the ratio of the rms value of the waveform not including the fundamental, to the rms of the fundamental component.

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} I_n^{\,2}}}{I_1} \tag{3.16}$$

Distortion factor can be related to THD in a following way:

$$DF = \frac{I_1}{I_{rms}} = \frac{1}{\sqrt{1 + (THD)^2}} \tag{3.17}$$

The power factor can be written as a product of distortion factor and displacement factor:

$$PF = \frac{< P >}{V_{rms} I_{rms}} = \frac{I_1}{I_{rms}} \cos(\varphi_1 - \theta_1) = \frac{1}{\sqrt{1 + (THD)^2}} \cos(\varphi_1 - \theta_1) \tag{3.18}$$

where $(\varphi_1 - \theta_1)$ is a phase difference between fundamental (first) components of voltage and current. Often the voltage fundamental component is used as a reference, so it has a zero phase to simplify the equations.

It is clear that to decrease the distortion factor - the current harmonics other than fundamental should be eliminated (decreased as much as possible).

Furthermore, as it was shown, in case of sinusoidal voltage waveform – current waveform should have only fundamental component (affecting the distortion factor) with the same phase as the voltage (making the displacement factor to be equal to one) to achieve a unity power factor.

These conditions are met in case of the resistive load, and it has a practical meaning since AC voltage sources usually have low distortion, so assumption of sine wave voltage waveform is valid. It was also shown earlier that power factor will reach unity even in case of arbitrary voltage waveform if the load is linear resistive.

These conclusions represent the objectives of power factor correction.

Chapter 4

Power Factor Correction

As it was shown in a previous chapter, to achieve unity power factor: first, the load current should not have any extra harmonics that are not present in voltage waveform, and second, present current harmonics should be proportional to related voltage harmonics and be in phase with them. In other words, the resistor is ideal load with unity power factor for any voltage waveform. Therefore, even when the load is not a resistor, it should emulate resistive behavior.

4.1 Introduction to the Switching Converters

Modern energy transfer implies the usage of switching topologies because they can provide high efficiency in comparison, for example, to linear regulators. Consider the simple step-up topology – boost in Fig. 4.1.1. First, the DC voltage is supplied at the input of the converter.

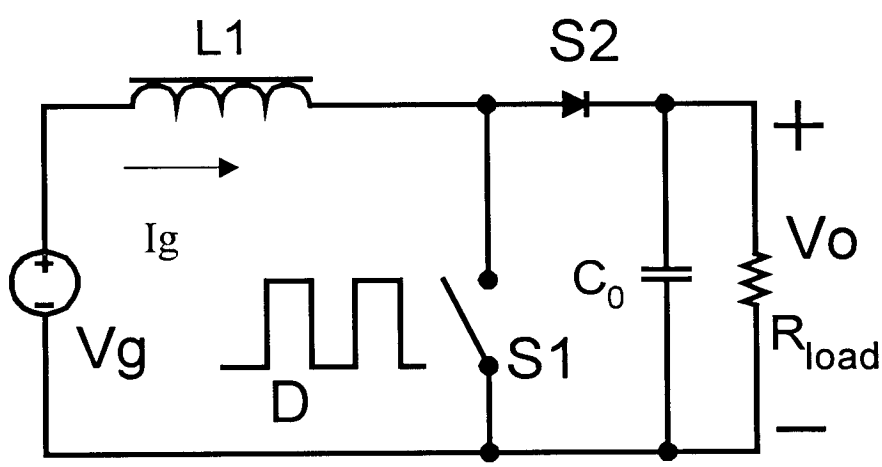

Figure 4.1.1: Boost DC/DC converter

Switch *S1* is usually a transistor, switch *S2* is a passive switch in this topology. The control waveform is shown in Fig. 4.1.2.

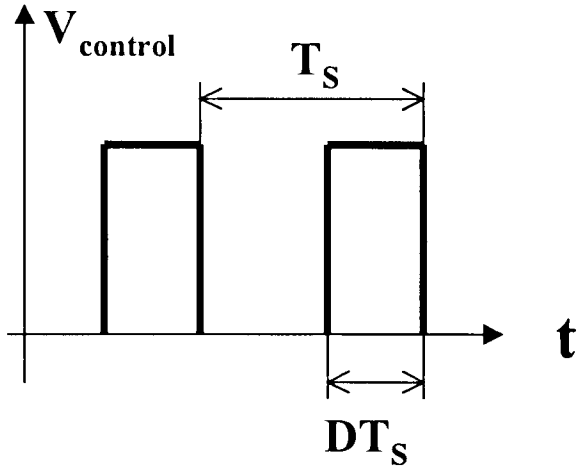

Figure 4.1.2: Control waveform for Boost DC/DC converter in Fig.4.1

It can be easily shown that described boost converter ideally has a voltage gain characteristic *M(D)* as (4.1.1), if parasitic elements are assumed to be negligible.

$$M(D) = \frac{V_0}{V_g} = \frac{1}{1-D} \tag{4.1.1}$$

This characteristic is plotted in Fig. 4.1.3.

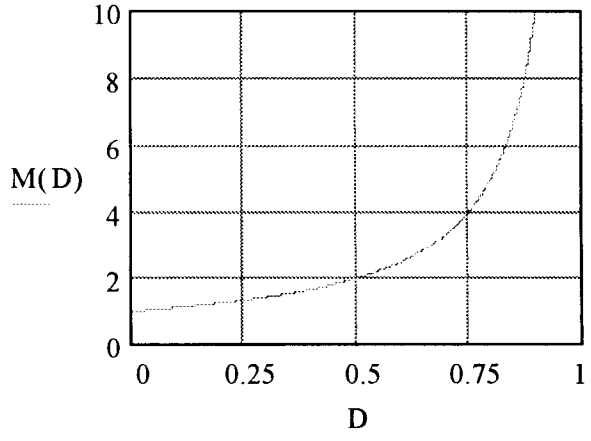

Figure 4.1.3: Voltage gain characteristic M(D) of the ideal boost converter

Output voltage will change according to $V_g M(D)$ as duty ratio D is changed. This control method is called *Pulse Width Modulation* (PWM). Therefore, by introducing the feedback into PWM, it is possible to achieve and regulate desired output voltage V_0 even with some changes in V_g. Recalling objectives of achieving unity power factor – the input filer is needed, since inductor current has harmonics of switching frequency (typically in 50KHz – 500KHz range) that should be eliminated since they are not present in input voltage waveform.

Now consider the AC input voltage with necessary rectification, Fig. 4.1.4. Practically, the input filter should also be included to eliminate harmonics of switching frequency in input current $i_g(t)$.

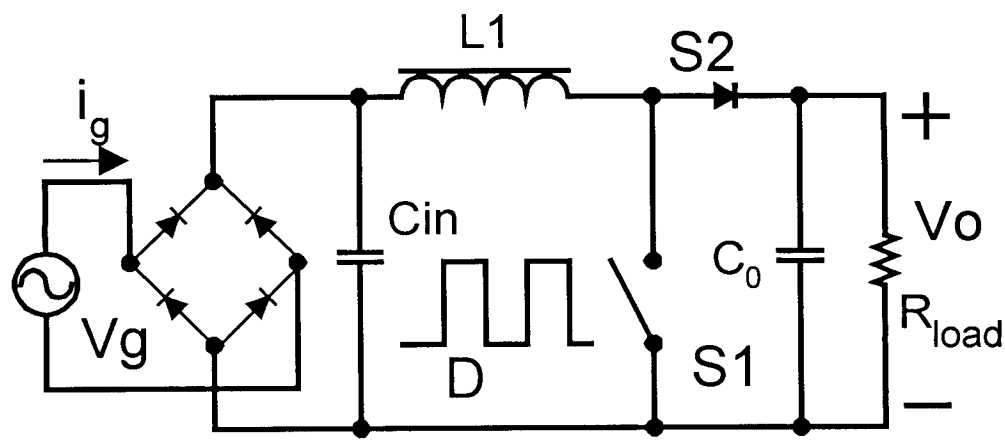

Figure 4.1.4: Boost converter with AC input voltage

First, consider the situation when the input capacitor Cin is sufficiently big, so it's voltage is almost DC.

4.2 Rectification by the Diode Bridge

The following boost implements DC-to-DC operation with almost constant duty ratio *D* and provides necessary value of output voltage. Rectification of AC to DC is provided by diode bridge and capacitor *Cin*. The equivalent circuit is shown in Fig. 4.2.1 where $R_{eff}=M^2(D)R_{load}$. The main problem of such rectifier is that input current is heavily distorted. Since voltage on the *Cin* drops very slightly – then diodes conduct only at small region of line cycle when input voltage is at its highest.

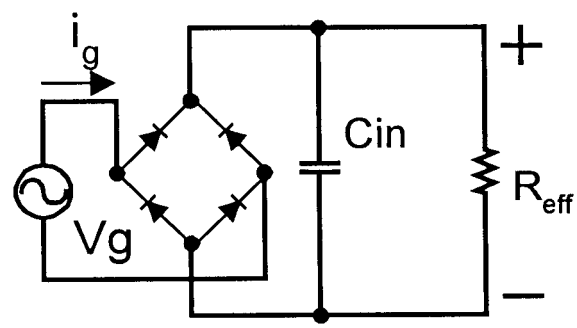

Figure 4.2.1: Equivalent circuit for Boost converter with AC input voltage in Fig.4.1.4

The typical current waveform is shown in Fig. 4.2.2. Illustration is made by PSPICE computer simulation, but this result is well known practically in such application [14]. The following parameters were used: *Cin*=900uF, *Reff*=500Ohm, *Vg*=100V. The harmonic content of this waveform is illustrated in Fig. 4.2.3 and clearly has more than just one fundamental component (60Hz).

Low power applications can be implemented this way however, most the consumer and industrial applications would introduce so much noise to other power consumers and so much reactive power that it is out of the question.

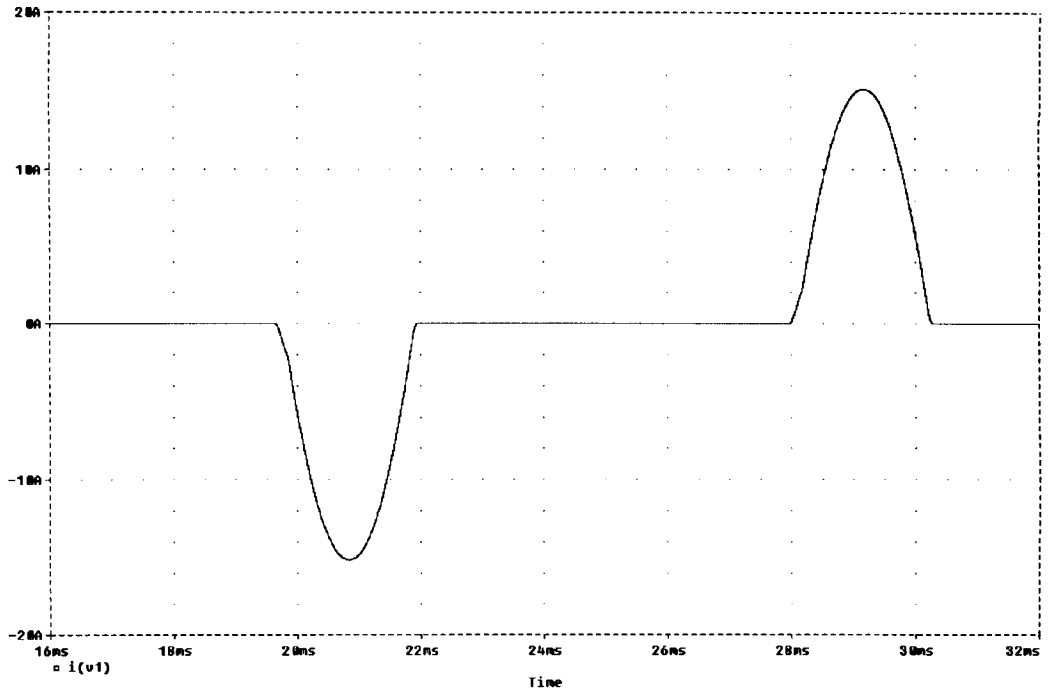

Figure 4.2.2: Input current waveform for the boost with "big" Cin

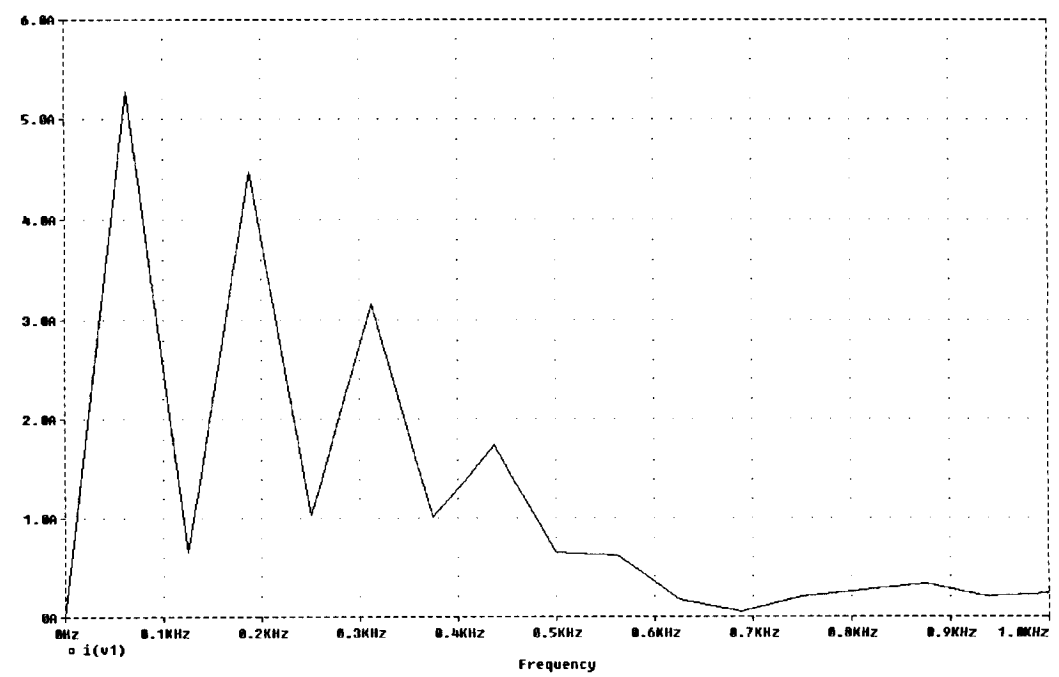

Figure 4.2.3: Harmonic content of the waveform in Fig.4.6

Waveform in Fig.4.2.2 is clearly distorted and is far from ideal sine wave. Fourier analysis in Fig.4.2.3 confirms that this waveform has extra harmonics with relatively high amplitudes. The need for power factor correction is therefore established.

4.3 Conventional Methods for Power Factor Correction

One approach to correct the waveform in Fig. 4.2.2 is to use passive filters [15]. This approach is limited though, because eliminating extra harmonics with such high amplitude will require a lot of attenuation, and while the filter is designed for more and more attenuation, it will start influencing the power factor by introducing bigger and bigger phase shift and distortion at low frequencies. The improvement is therefore limited.

The other possibility is to have the value of *Cin* sufficiently small, so it absorbs the current ripple at switching frequency, but does not interfere with AC input voltage. In other words, the value of *Cin* is such that it is discharged by R_{eff} at much faster rate than time scale of line frequency. Voltage on the capacitor *Cin* is close to the original waveform and is just rectified to be only one polarity.

Consider operation of the boost converter with PWM in such conditions. The constant duty ratio (PWM control) will provide necessary output voltage, as before; however, the input current of the converter will still differ in shape from ideal sine wave of voltage at the input. The example of input current is shown in Fig. 4.3.1, and related harmonic content of this waveform is sketched in Fig. 4.3.2. Illustrations were done by PSPICE computer simulation.

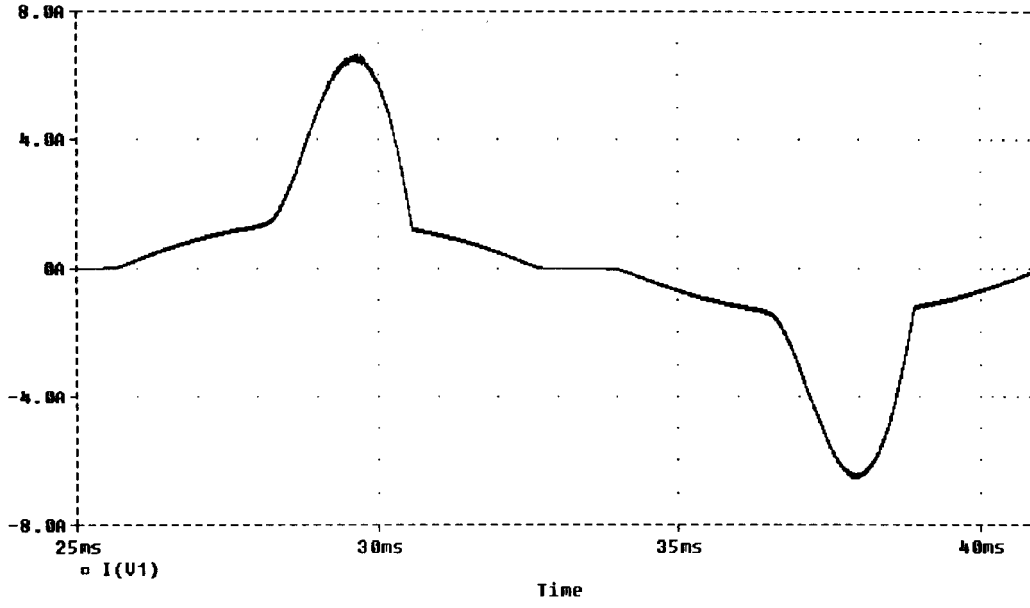

Figure 4.3.1: Input current for the boost with "small" Cin and constant duty ratio

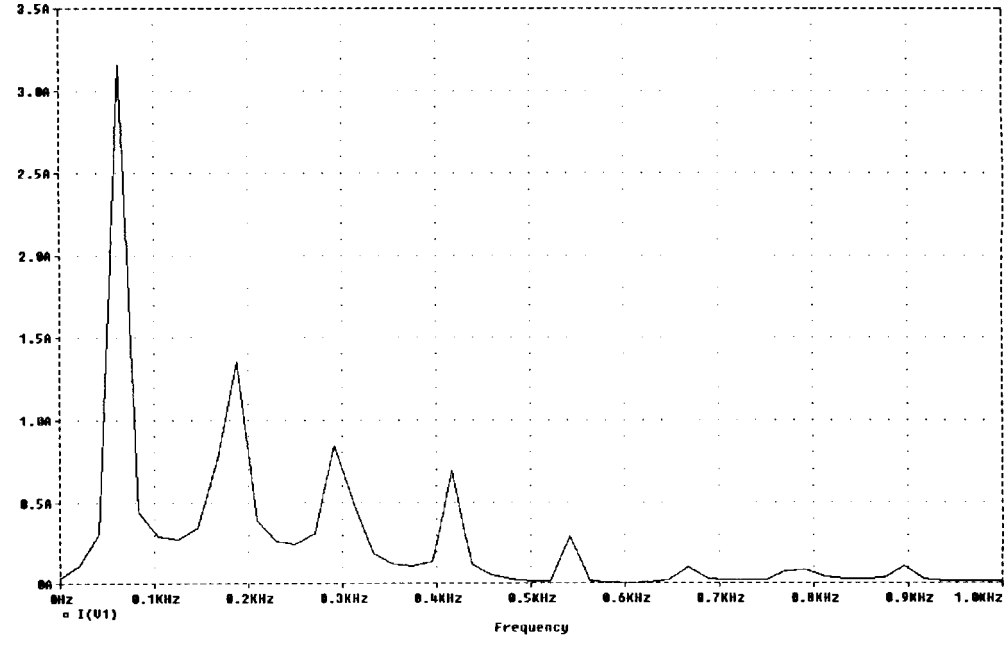

Figure 4.3.2: Harmonic content of the waveform in Fig.4.3.1

Noticeable "plateau" and then spike of the current in Fig. 4.3.1 is explained by the change of converter operation in this example: boost operates in DCM at low input voltages and then enters *Continuous Conduction Mode* (CCM) at high voltage region.

Clearly, the power factor of such waveforms is not unity and extra steps in control should be taken to improve it, although the situation is somewhat better than one in section 4.2 where AC was rectified to DC by diodes and big capacitor; see Fig. 4.2.2 and 4.2.3. There are many methods to make input current of the converter to follow the input voltage. Some are more general than others, and some depend on the type of the converter and even a type of its operation. One way to make the boost current to be proportional to input AC voltage is to preserve PWM operation for on-time of the switch but change off-time in such a way that inductor current starts to ramp up from zero value when switch is turned on. This method is illustrated in Fig.4.3.3 (switching frequency is not in a right scale to displayed half of line period). The converter operation is as discussed next.

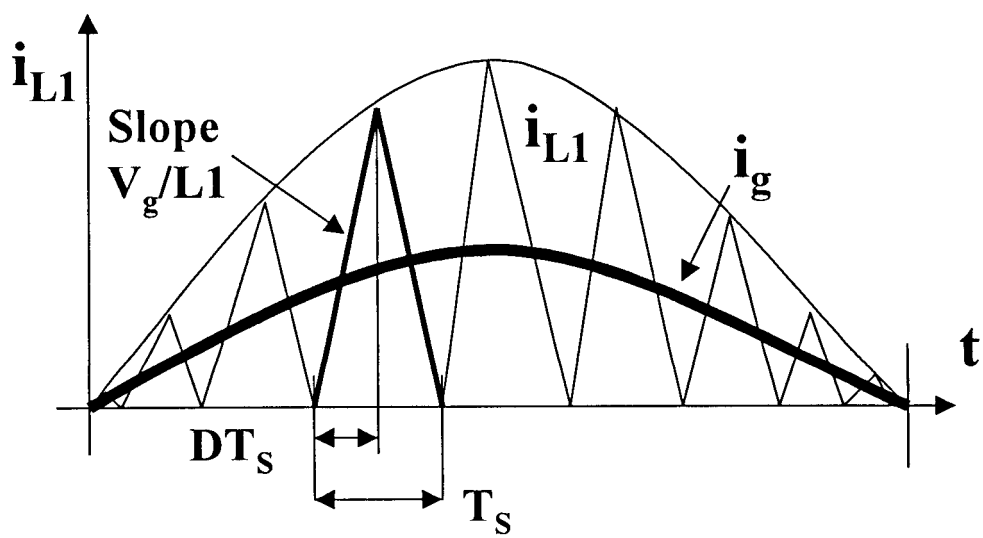

Figure 4.3.3: Boost inductor current during operation at the boundary of DCM

DT_S time is kept constant (slope of inductor current is *Vg/L1*), then switch *S1* (schematic in Fig. 4.1.4) is turned off and current ramps down with the slope *(Vg-Vo)/L1*, which is clearly dependent not only on input voltage. At some point the inductor current reaches zero value and switch *S1* turns on.

This method of control leads to the condition when switch *S1* always turns on at zero inductor current. Since the slope of the raising current is *Vg/L1*, then the reached peak value I_{L1_peak} will also be proportional to input voltage *Vg*; see (4.3.1).

$$I_{L1\_peak} = \frac{Vg}{L1} DT_S \tag{4.3.1}$$

Current waveform has therefore triangular shape each switching cycle with peak current proportional to *Vg*. Average current of such waveform is 0.5 of the peak value, (4.3.2).

$$< I_{L1} >= \frac{Vg}{2L1} DT_S \propto Vg \tag{4.3.2}$$

Therefore, when input filter eliminates harmonics of the switching frequency – the averaged input current $i_g(t)$ is proportional to input voltage and power factor reaches unity value.

There are techniques that allow much smaller current ripple, for example average current control. Switching frequency is usually constant in such applications, but duty ratio changes to make average inductor current to follow the input voltage waveform. Many of such topologies and control methods are developed; these circuits usually have relatively complicated control to achieve output voltage regulation and Power Factor Correction at the same time.

There is also a class of circuits called automatic current shapers, the example is a buck-boost converter in *Discontinuos Conduction Mode* (DCM), shown in Fig. 4.3.4. The corresponding waveforms are shown in Fig. 4.3.5.

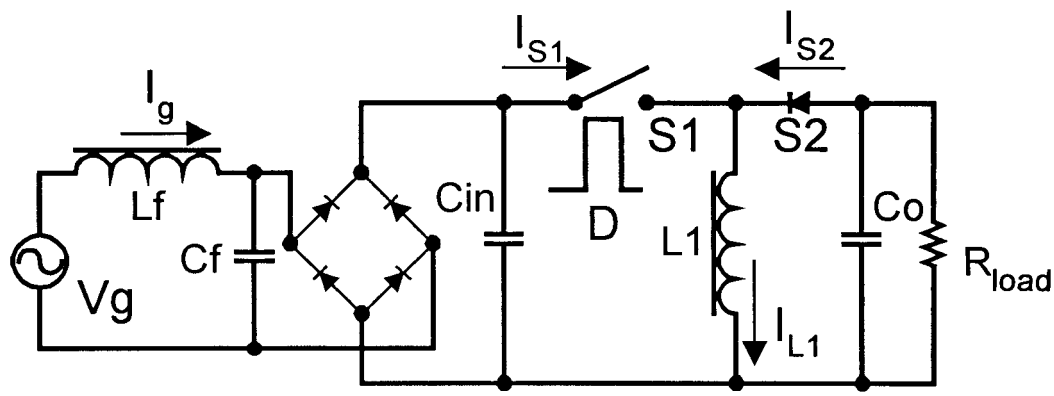

Figure 4.3.4: Power factor correction with buck-boost converter

The buck-boost is operating in DCM, so inductor current starts ramping up from zero value every switching cycle (duty ratio is constant and is adjusted by feedback for the appropriate output voltage, as in usual PWM operation). Similar to the previously discussed case, the peak value of the current I_{L1_peak} is proportional to Vg, since the slope of the current waveform is $Vg/L1$; and part of the current during DT_S time interval is proportional to input voltage. Notice that only this part of inductor current contributes to input current I_{S1}. Since duty ratio does not change, the average current during the whole switching period T_S is proportional to Vg as well, (4.3.3).

$$< I_{L1} >= \frac{Vg}{2L1} D^2 T_s \propto Vg \qquad (4.3.3)$$

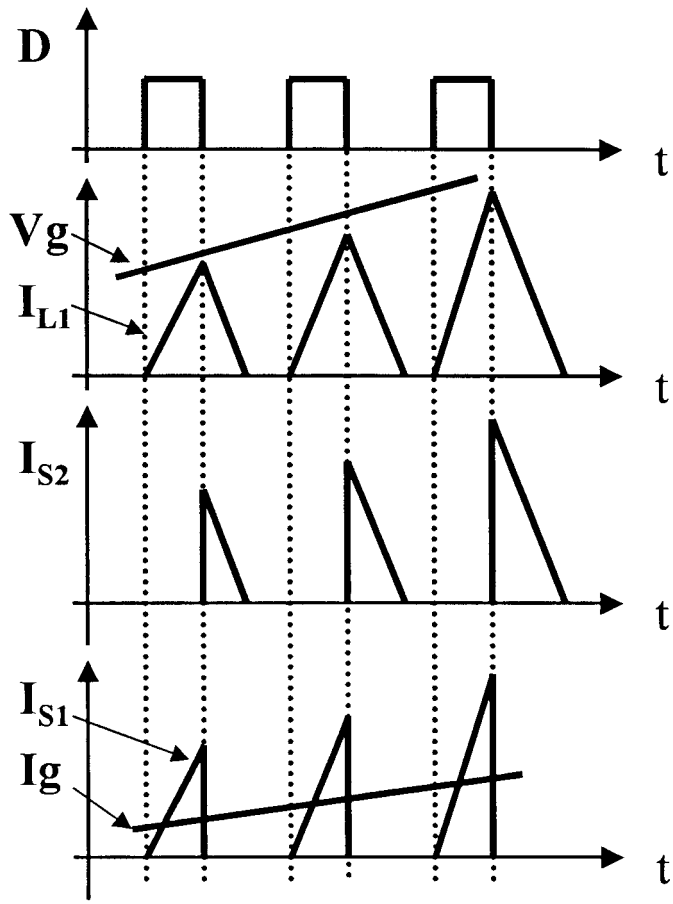

Figure 4.3.5: Waveforms for buck-boost PFC in DCM in Fig.4.3.4

Therefore, the average current of *S1* is proportional to *Vg*, and once harmonics of the switching frequency are eliminated by input filter, the waveform of input current Ig has the same shape as the voltage waveform. Unity value of the power factor is therefore achieved.

There are several converters that can be classified as automatic current shapers, practically - they all have to be in DCM for such operation. This is a clear disadvantage, because DCM represents high current stress on all components and very high rms current values that lead to increased losses in all parasitic resistances of the converter. Fig. 4.3.5 shows the current I_{S1} that corresponds to input current of the power stage. This current

clearly has very high ripple and big rms value, which decreases efficiency. DCM also results in a bigger input filter to eliminate harmonics of such waveform, even in comparison to high ripple waveform on the boundary of CCM and DCM in Fig. 4.3.3.

Advantage of automatic current shapers is that they allow much simpler control, usually simple PWM.

To understand more about the need for specific control (usually more complicated than PMW) in case of PFC converter; the described earlier boost example is considered. This power stage has better efficiency and better shape of input current in comparison to buck-boost converter, it is simple and often used. Consider boost topology in Fig. 4.1.4 operating in DCM. Corresponding shape of inductor current is shown in Fig. 4.3.6.

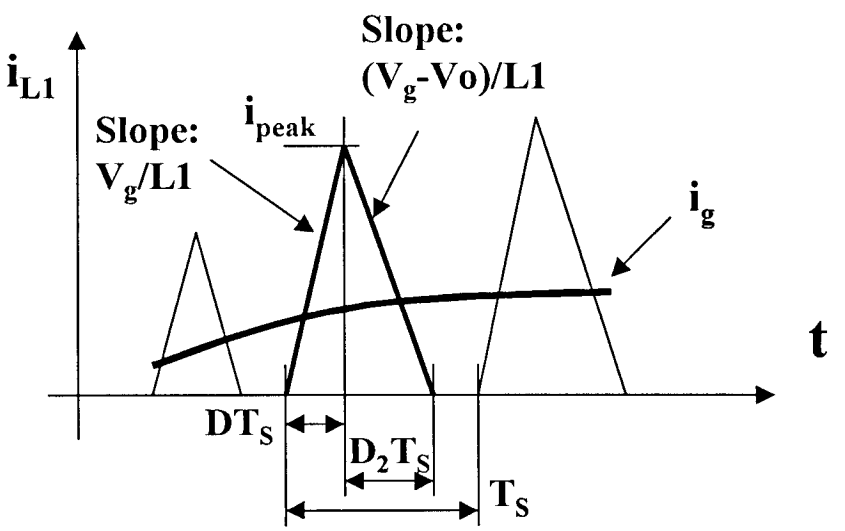

Figure 4.3.6: Waveforms for boost PFC in DCM

The i_g current in Fig.4.3.6 corresponds to input current of the PFC; it is effectively inductor current with eliminated harmonics or, in other words, averaged by the input filter.

From the waveform in Fig. 4.3.6 it can be concluded that average inductor current during arbitrary switching period T_S is found as (4.3.4).

$$< I_{L1} >= i_g = \int_0^{T_S} i_{L1}(t)dt = \frac{1}{2} i_{peak} D + \frac{1}{2} i_{peak} D_2 \qquad (4.3.4)$$

Parameter D_2 can be found from expressing the value of i_{peak} with D and D_2 same time; see (4.3.5). Notice that $V_o > V_g$ for the boost topology.

$$i_{peak} = \frac{V_g}{L1} D T_S = \frac{-V_g + V_o}{L1} D_2 T_S \qquad (4.3.5)$$

Then the D_2 parameter can be found as (4.3.6) and substituted into (4.3.4).

$$D_2 = \frac{V_g}{V_o - V_g} D \qquad (4.3.6)$$

Finally, the input current i_g (inductor current, averaged during switching period) is found as (4.3.7).

$$i_g = < I_{L1} >= \frac{1}{2} i_{peak}(D + D_2) = \frac{V_g}{2L1}\left(1 + \frac{V_g}{V_o - V_g}\right) D^2 T_S \qquad (4.3.7)$$

Notice that boost input current i_g does not have exact $i_g \propto Vg$ dependence, which is needed for the unity power factor. The mathematically calculated waveforms are shown in Fig. 4.3.7. The sinusoidal input voltage is shown as rectified after the diode bridge; the related input current of the boost i_g has known "bell-shape." The difference of shapes for voltage and current waveform lead to power factor less than unity, or in other words: current waveform has extra harmonics that do not contribute to power transfer, cause losses in parasitic resistance of the power line and introduce noise for other power consumers. Non linear loads also cause the distortion of voltage waveform itself, so line

voltage often has a flat part around the peak value – the result of disproportional load current in that region.

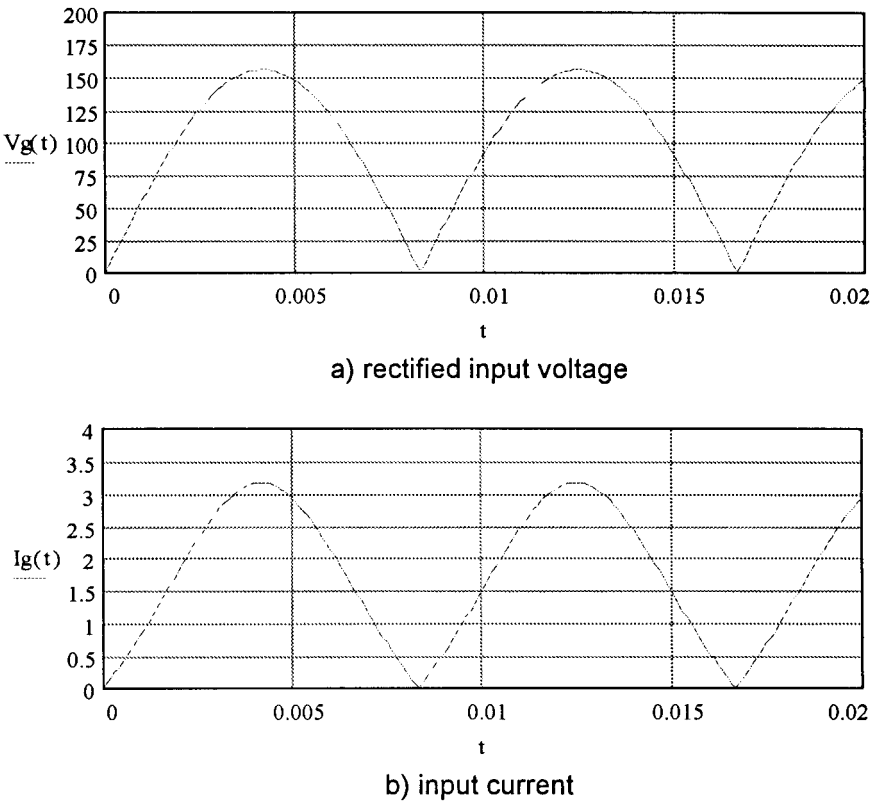

Figure 4.3.7: Calculated waveforms for boost PFC in DCM: input a) voltage b) current

Notice that boost operation in DCM can be changed to CCM if for example load current, value of $L1$ or switching frequency is sufficiently increased. The converter can therefore be in CCM partially or during the whole line cycle. Exact $i_g \propto Vg$ proportionality will be still violated.

As it was mentioned, the boost is not included into limited class of automatic current shapers and needs specific control to achieve unity power factor.

There is some common issue for most of the topologies associated with power factor correction. Majority of the conventional topologies share the same feature: they all have a diode bridge at the input (as in Fig. 4.1.4, and 4.3.4), so voltage is rectified into pulsing DC and can be then processed to DC by the power stage. This input rectification is probably the most common feature in modern power factor correctors, and so are the associated problems.

Chapter 5

Disadvantages of Input Rectification

Input rectification introduces power losses and waveform distortion in power factor correction (PFC) circuits. Losses in diode rectifier must be investigated to evaluate the problem. Option of synchronous rectifier will be also considered and comparison will be presented. Usually much less critical issue of the waveform distortion and noise associated with input rectification becomes important in some applications and will be considered as well.

5.1 Losses in the Diode Rectifier

Fig. 5.1 represents equivalent circuit for loss calculation, where V_d is a voltage drop on the diode. Relative losses in the input rectifier as a ratio of losses in a diode bridge P_{br} to the total power delivered by the voltage source P_{in} will be calculated as in (5.1.1).

$$\frac{P_{bridge}}{P_{in}} = \frac{2V_d I_g}{V_g I_g} 100\% = \frac{2V_d}{V_g} 100\% \qquad (5.1.1)$$

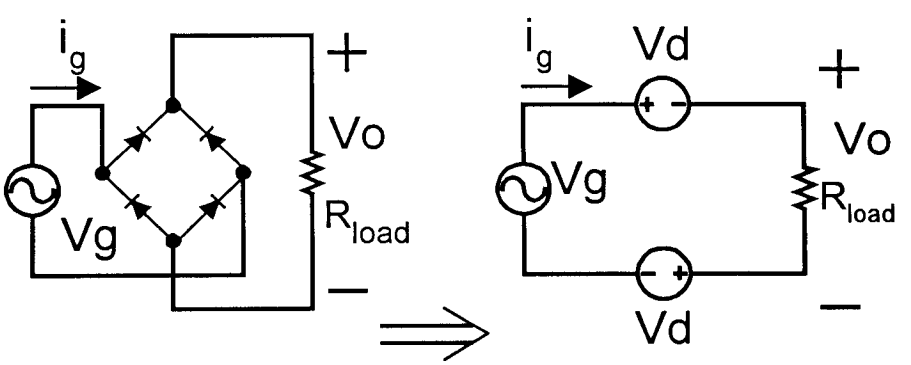

Figure 5.1: Equivalent circuit for calculation of losses in input rectifier

First, assume that this voltage drop does not depend on current $i_g(t)$, then choosing a realistic value of 1V for V_d the estimated losses can be easily plotted as a function of input voltage V_g, Fig. 5.2. Clearly, there will be no dependence on input current or power dissipated in the load, Fig. 5.3.

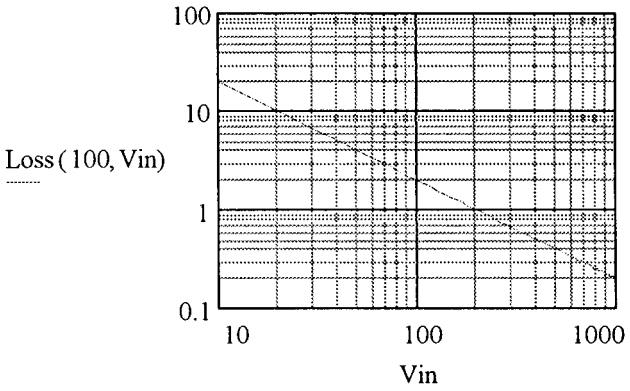

Figure 5.2: Rectifier loss [%] calculation (5.1.1) as a function of input voltage Vin for 100 W input power

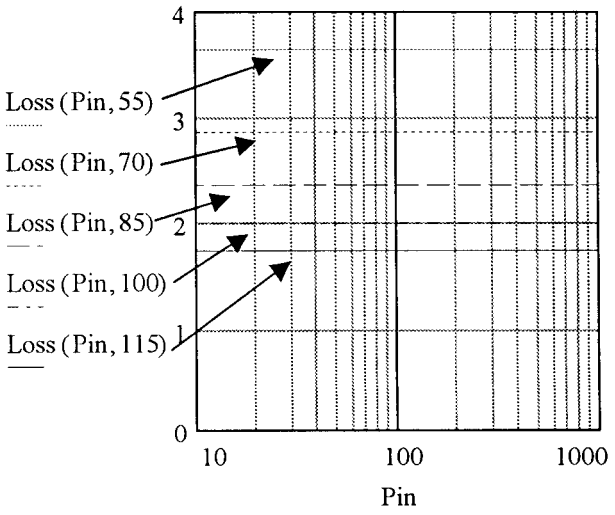

Figure 5.3: Rectifier loss [%] calculation (5.1.1) as a function of input power Pin for input voltages 55-115 V

Considered estimation shows that diode bridge will have 2-2.5 V voltage drop under high input currents, which results to about 1.5-2% loss of input power for standard 115 VAC input. Specifications, however, always include 85 VAC as a lower boundary of converter operation, and it would be certainly an objective to make operation range of input voltage even wider, so converters can operate reliably and with high efficiency even at lower voltages.

Assumption of the constant voltage drop across the diode resulted in realistic estimation of power losses, now the exact calculation will be done. The following chapters will show topologies without such losses, so it is important to understand exact trade-off.

Define diode characteristic by (5.1.2), where I_D=Ig and V_D are diode current and voltage respectively, and I_0 and V_B are parameters of the particular diode.

$$I_D = I_0\left(e^{\frac{V_D}{V_B}} - 1\right) \tag{5.1.2}$$

then the relative losses in a diode bridge can be found as (5.1.3)

$$\frac{P_{bridge}}{P_{in}} = \frac{2V_B \ln\left(1+\frac{I_g}{I_o}\right)}{V_g}100\% = \frac{2V_B \ln\left(1+\frac{Pin}{V_g I_o}\right)}{V_g}100\% \tag{5.1.3}$$

where V_g is the input voltage and Pin is input power (power taken from the source) of the converter.

Table 5.1 shows examples of diode parameters I_0 and V_B for (5.1.2), found to fit manufacturer's data sheets. Examples were chosen as practical and popular rectifiers, used in industry.

Parameters are mainly shown for 25°C temperature; notice that conditions of actual

operation are usually different. Notice that fast components, called by manufacturer's switching diodes, ultra fast diodes, etc., would have substantially higher voltage drop under the same conditions. The reason is that minimizing the voltage drop and increasing current and voltage ratings are the only parameters in the case of line rectification. Switching/fast diodes, from other hand, have the reverse recovery time as dominating parameter. Notice also that two components will be needed in case of only two diodes in one package (MURB1660CT or MUR3060).

Diode Rectifier	**Manufacturer**	I_0 **[A]**	$V_{forward}$ **at** $I_{forward}$	V_B **[V]**
2KBB60 (bridge)	Int. Rectifier	0.00001	1.1 @ 1.9A	0.090
100JB60L (bridge)	Int. Rectifier	0.00001	1.3 @ 10A	0.094
MURB1660CT (double)	Motorola	0.00001	1.5V @ 8A	0.11
MUR3060 (double)	Motorola	0.00001	1.7V @ 15A	0.12
D10XB60H (bridge)	Shindengen	0.00001	1.05V @ 5A	0.084
D25XB800 (bridge)	Shindengen	0.00001	1.05V @ 12.5A	0.078

Table 5.1: Parameters of the diode rectifiers.

Calculation of losses in the diode bridge rectifier is not connected to voltage/current ratings of particular devices, so attention will be paid mainly to actual electrical parameters. Notice that all diodes have the same parameter I_0=10μA as maximum reverse current at highest reverse voltage. It is clear then that rectifiers with smallest values of V_B parameter will have the lowest voltage drop and therefore the lowest losses.

The following calculations will be made for the best of shown examples - D25XB800 from Shindengen, and for the worst one – MUR3060 from Motorola. This way some practical range of characteristics will be outlined.

Equation (5.1.3) predicts relative power losses as a function of input power *Pin* and input voltage *Vg*. The dependence of rectifier losses on input power *Pin* for different values of input voltage *Vg* is shown in Fig. 5.4 and 5.5 for D25XB800 and MUR3060 respectively.

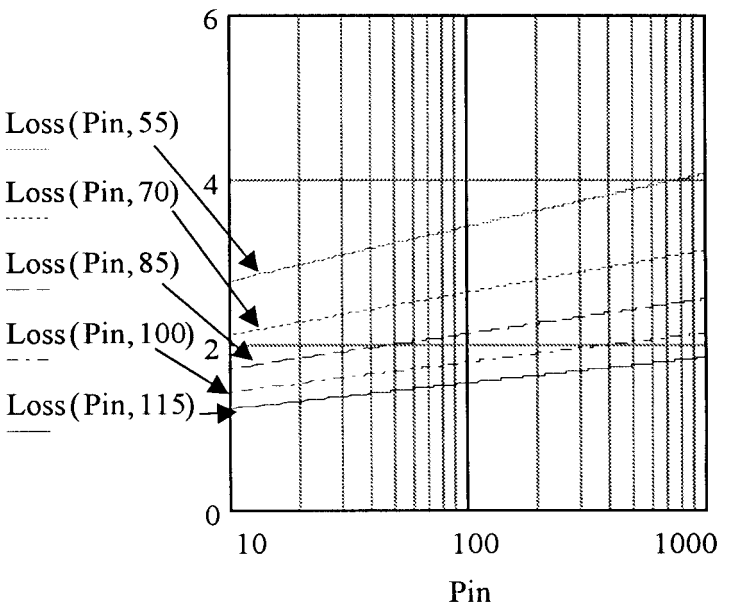

Figure 5.4: Rectifier loss [%] from (5.3) as a function of input power Pin for D25XB800 for input voltages 55-115 V

The actual data shows that, for example, at 85V input voltage and 100W input power the relative losses in input rectifier will range from 2% to 3.5%. Increasing the power will lead to some increasing in losses, because the voltage across the diodes will increase

with the current. More dramatic though is the increase of losses as input voltage decreases.

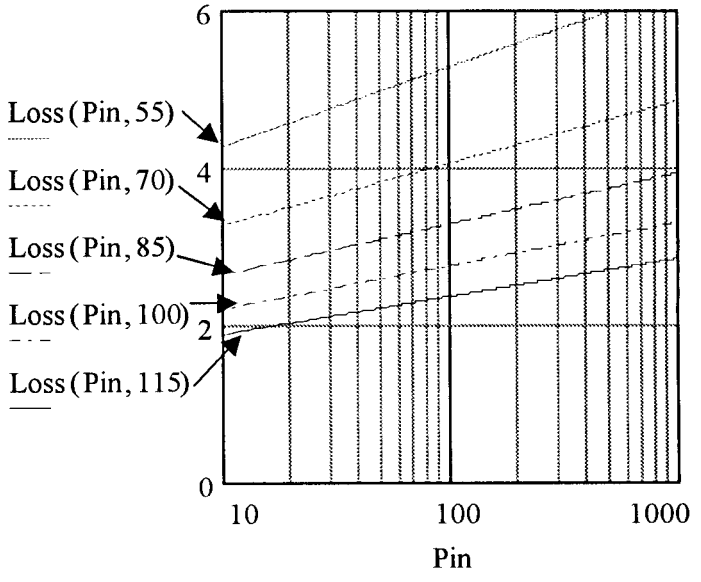

Figure 5.5: Rectifier loss [%] from (5.3) as a function of input power Pin for MUR3060 for input voltages 55-115 V

Voltage on the diodes becomes bigger and bigger fraction of decreasing input voltage *Vg* and since same power in the load should be supported – the input current is increasing proportionally to decreasing of *Vg*, so the voltage drop on the diodes is even increasing further with the current. Fig. 5.6 shows relative losses in D25XB800 rectifier as a function of input voltage *Vg* for two values of input power 1KW and 100W. Fig. 5.7 displays the same characteristics for MUR3060.

One important comment should be made about those losses. The practical value for efficiency in modern power factor correctors is above 90% at low input voltage. The point of lowest input voltage in the specification range is the most critical, since it is the

point where converter takes the maximum current to support some constant output power, so losses are maximized and efficiency is therefore the worst. The most competitive power factor correctors have efficiency in the range of 92-94% at 85V input voltage and output power of several hundred Watts. The relative losses of 2-3.5% are therefore very significant, since they represent 25-58% of total losses in that region of operation.

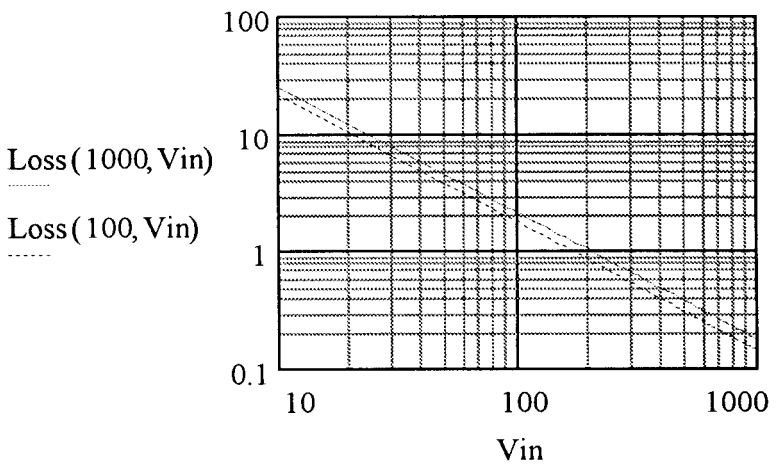

Figure 5.6: Rectifier losses [%] from (5.1.3) as a function of input Vg for D25XB800, 100 W (bottom trace) & 1KW (top trace) input power

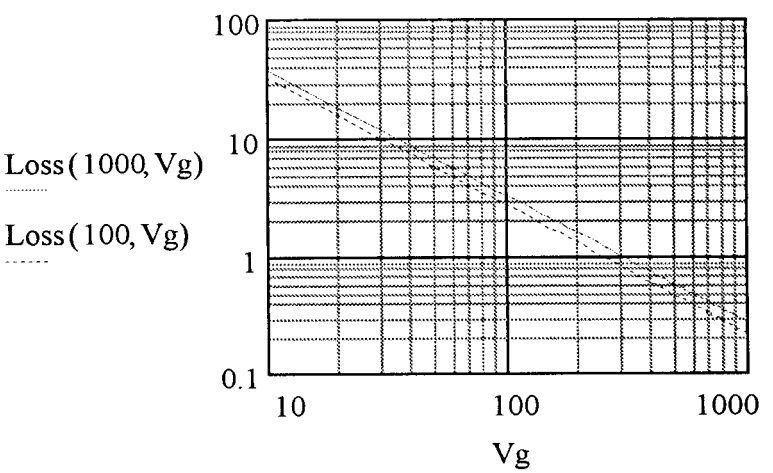

Figure 5.7: Rectifier losses [%] from (5.1.3) as a function of input Vg for MUR3060, 100 W (bottom trace) & 1KW (top trace) input power

The point of 85V is a standard low boundary for most input voltage specifications; if even lower input voltage is considered, the losses in input rectifier become not just dominating, but a catastrophe.

It has been shown that input rectifier losses degrade the overall efficiency and performance of power factor corrector; however, there is an additional issue about it. The diode bridge is one of the hottest components in off-line applications. The power dissipation there is significant and creates additional complications for thermal management and heat sinking. Fig. 5.8 shows the power dissipated in D25XB800 as a function of input power *Pin* for different input voltages *Vg*.

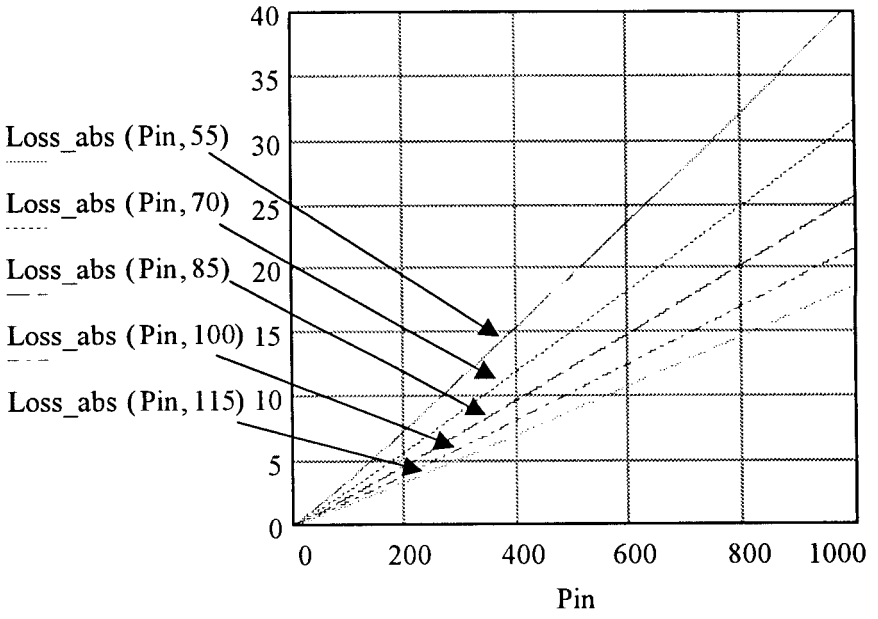

Figure 5.8: Rectifier loss [W] from (5.1.3) as a function of input power Pin for D25XB800, input voltages 55-115 V

Related loss characteristics for MUR3060 are shown in Fig. 5.9. Notice that at a standard critical point of 85V input voltage, the modern several hundred watt power

modules from Lambda, Lucent Technologies, Vicor and others have rectifier losses in 12-20W range at input power about 500W.

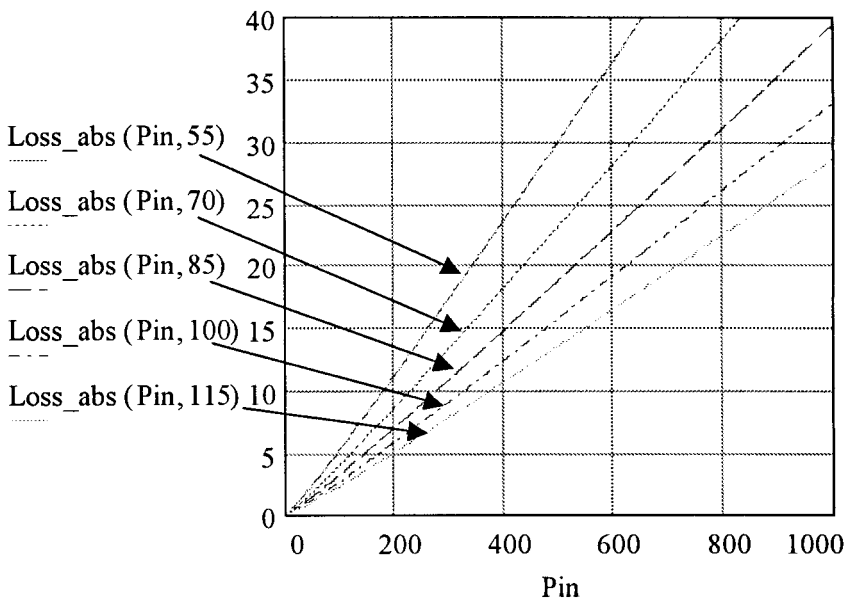

Figure 5.9: Rectifier loss [W] from (5.1.3) as a function of input power Pin for MUR3060, input voltages 55-115 V

It is important, since related standard small packages for the similar off-line power factor correctors can practically dissipate only about 40W of total losses without forced heat sinking.

5.2 Diode Rectifier vs. Synchronous Rectifier

One option could be to use synchronous rectification with low impedance MOSFETs to decrease the losses at the input of converter. This approach clearly involves control

complications, increase in size and cost, without eliminating the problem completely. What is even more important: there is always a current where the voltage drop across the on resistance of the MOSFET will be higher than related voltage drop across the diode, so diode bridge will be even more effective than proposed active switches.

Table 5.2 shows parameters of popular MOSFET devices. Notice that the temperature of the junction *Tj* would be definitely higher than room temperature of 25°C, especially in modern tight package with other heat dissipating components of PFC while operating under high input current condition. The temperature dependence is approximated as liner with good accuracy of several percent. The coefficient of 1.8 is valid for change in R_{on} while temperature changes from 25°C to 100°C according to manufacturer's data, so parameter K_T=0.010666 [Ohm/°C] defines the effective R_{on} to be used in calculations. The R_{on} can then be expressed as (5.2.1).

$$R_{on}(T^0C) = R_{on}(25^0C)\cdot\left(1 + K_T\cdot(T^0C - 25^0C\right) \tag{5.2.1}$$

Temperature of 70°C is chosen as a realistic operation condition for loss derivations. The calculated values of R_{on} are also shown in Table 5.2.

The losses in synchronous rectifier P_{s_bridge} can be expressed as losses in two MOSFETs, conducting the input current I_g. As before, the relative losses will be expressed as the ratio of losses in synchronous rectifier P_{s_bridge} and total power consumed from the source P_{in} via parameters V_g (input voltage) and P_{in} (input power), (5.2.2).

$$\frac{P_{s\_bridge}}{P_{in}} = \frac{2R_{on}I_g^2}{P_{in}}100\% = \frac{2R_{on}P_{in}}{V_g^2}100\% \tag{5.2.2}$$

MOSFET	Manufacturer	R_{on} [Ohm] at Tj=25°C/100°C	R_{on} [Ohm] at Tj=70°C (calculated)
IRF840	Int. Rectifier	0.85/1.45	1.26
IRFP450	Int. Rectifier	0.40/0.72	0.59
IRF340	Harris	0.30/0.53	0.44
IRF740	Harris	0.55/0.94	0.81
MTV16N50	Motorola	0.40/0.60	0.57
MTV25N50	Motorola	0.20/0.35	0.30

Table 5.2: Parameters of some popular MOSFETs.

The losses in synchronous rectifier will be illustrated on two boundary examples from the Table 5.2. However, necessary comment should be made about practical usage of these and similar MOSFETs.

The IRF840 MOSFET has the highest R_{on} among considered examples, but in fact it is 8A rated popular transistor. This rating would make IRF840 a possible choice in a rectifier for several hundred Watt converter which is operating under low input voltage conditions. Other transistors from Table 5.2 are therefore more expensive choices to gain efficiency at any cost.

Figure 5.10 represents relative losses in synchronous rectifier based on IRF840 as a function of input power for different input voltages. Related characteristics for MTV25N50 are shown in Fig. 5.11.

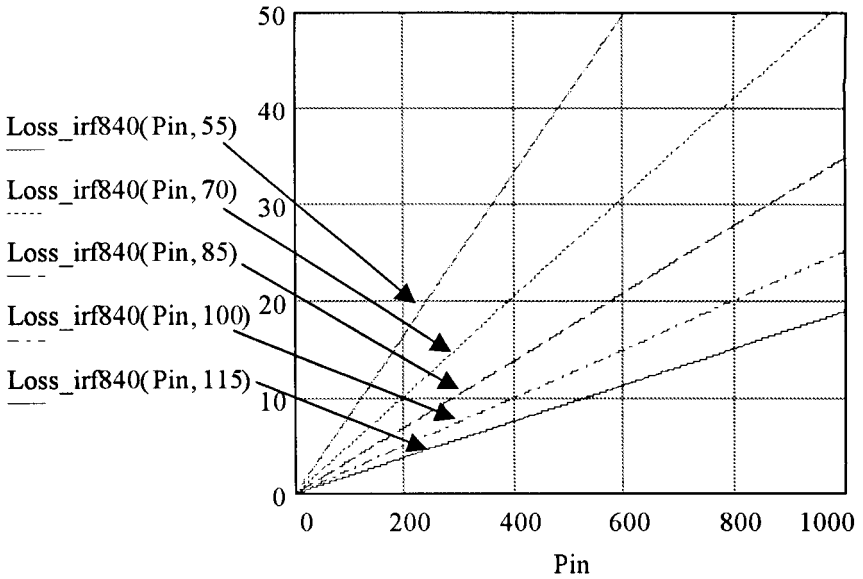

Figure 5.10: Rectifier loss [%] from (5.5) as a function of input power for IRF840, for input voltages 55-115 V

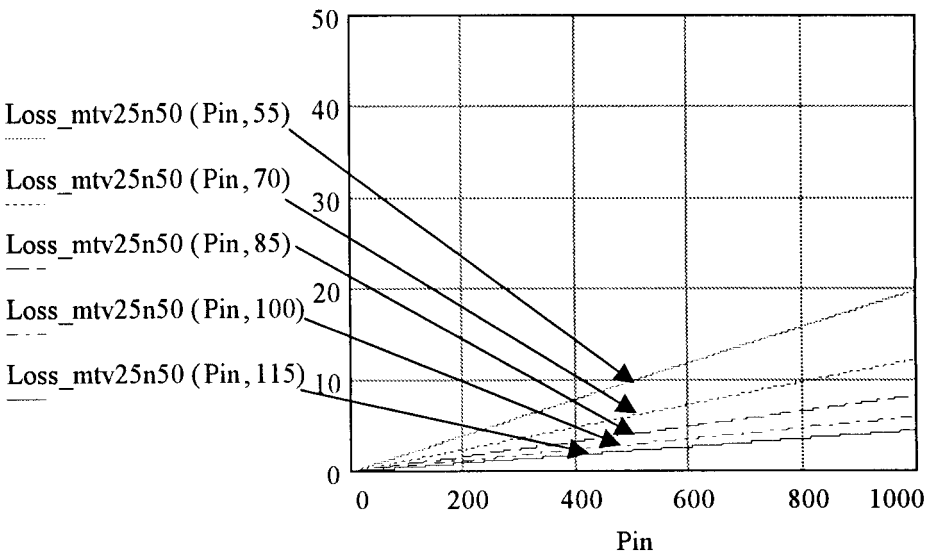

Figure 5.11: Rectifier loss [%] from (5.5) as a function of input power for MTV25N50, for input voltages 55-115 V

Notice the strong dependence of relative losses on *Vg* in (5.2.2). Relative losses in synchronous rectifier as a function of *Vg* are shown in Fig.5.12 and 5.13 for IRF840 and MTV25N50 respectively.

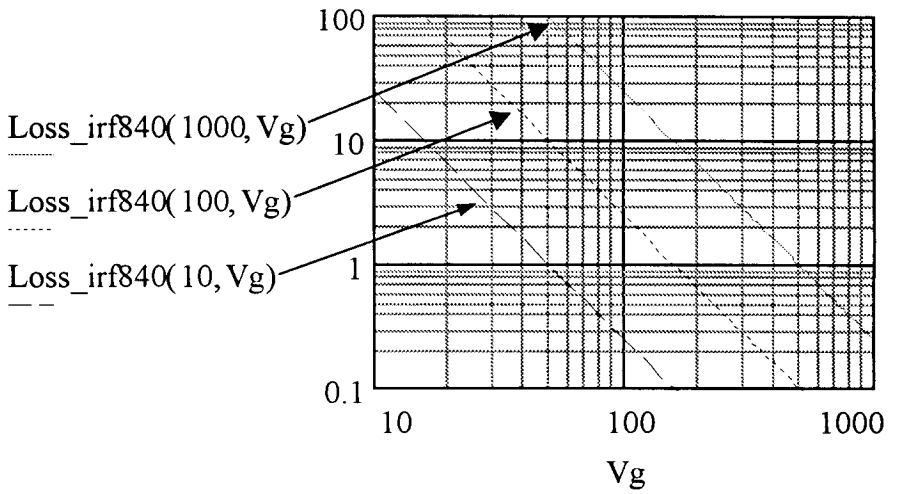

Figure 5.12: Rectifier loss [%] from (5.2.2) as a function of input voltage for IRF840, power levels 10, 100 and 1000 W

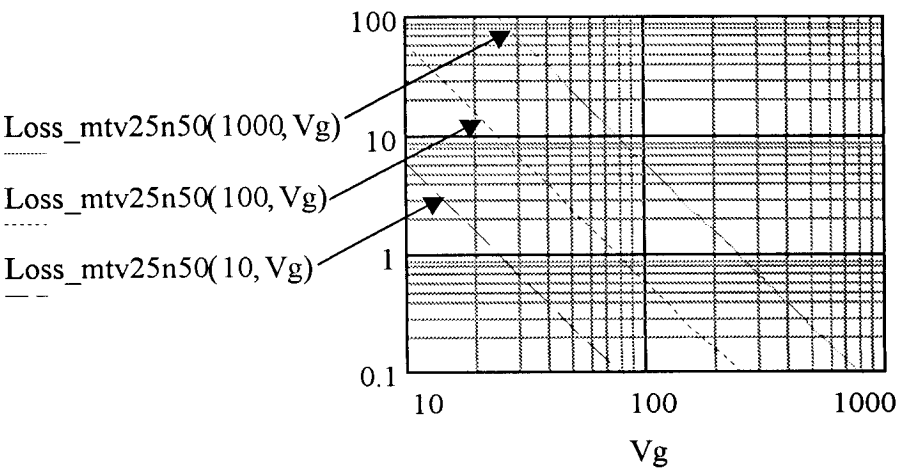

Figure 5.13: Rectifier loss [%] from (5.2.2) as a function of input power for MTV25N50, power levels 10, 100 and 1000 W

As input power increases, so does the input current which increases the losses in rectifier in general. Same time, converter represents effective load resistance that drops in value proportionally to the power increase; therefore, it provides higher voltage on MOSFETs and relative losses increase as well, degrading the efficiency.

It is now possible to compare the diode rectifiers and synchronous (MOSFET) rectifiers. Notice that it does not make any sense to compare worst performance diodes and best performance MOSFETs, because even high performance diode rectifiers would represent only small fraction of the cost invested into four high performance active switches and their control. The temperature increase would affect the voltage across the diode linearly, so the change from 25°C to 70°C will result in 1.15 times lower voltage.

Fig. 5.14 represents relative losses in input rectifiers based on IRF840 and MUR3060, moderate performance transistor and diode from the Tables 5.2 and 5.1 respectively, with correction to the same temperature 70°C.

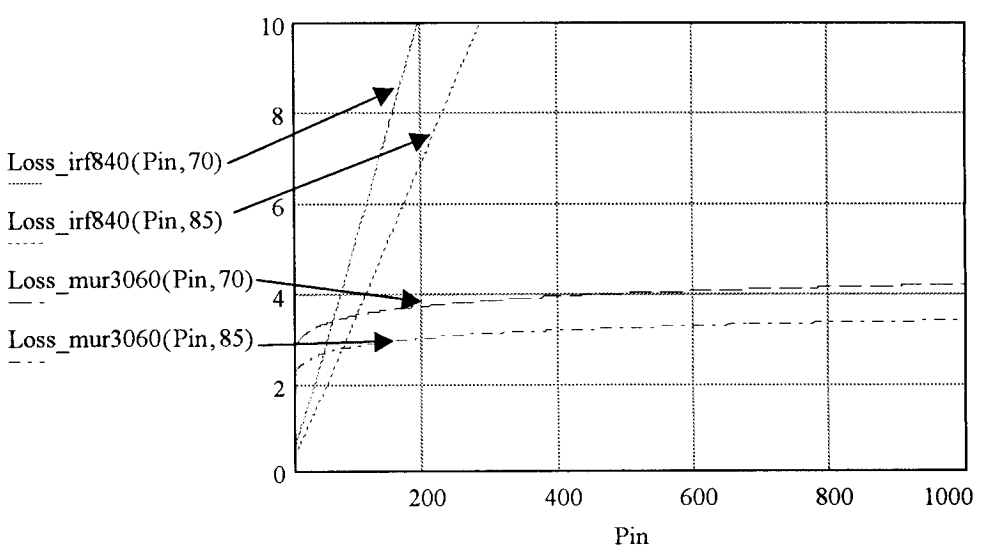

Figure 5.14: Losses [%] for input rectifiers based on IRF840 and MUR3060

Relative losses are plotted as a function of input power *Pin* – for critical input voltage 85V and for lower voltage of 70V to show the change of characteristics when input voltage drops even further. The same characteristics are plotted for high performance transistors MTV25N50 and diode bridge 25XB800 in Fig. 5.15.

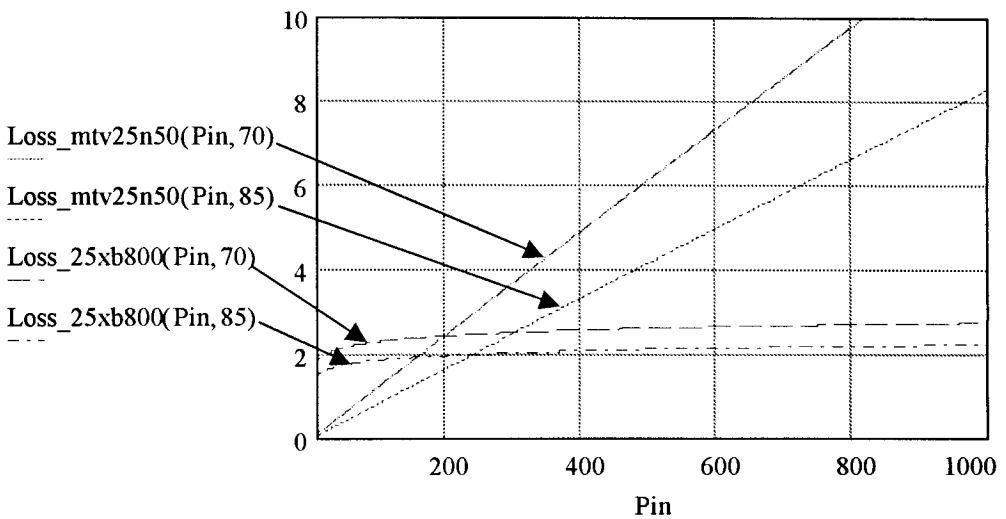

Figure 5.15: Losses [%] for input rectifiers based on MTV25N50 and 25XB800

There is clearly a region where MOSFETs dissipate lower power than diodes. However, it is a very limited region and with increase of input power *Pin* or decrease of input voltage *Vg*, the losses in synchronous rectifier become dramatically higher. In other words, increase of input current (by any reason) causes much smaller increase in voltage drop across the diode than proportional to current increase of voltage drop across on resistance of the MOSFET. The crossover point, or boundary where diode rectifier becomes more efficient, also moves to lower power region as input voltage decreases.

Fig. 5.16 illustrates the change in the crossover point with change in input voltage in detail for high performance components MTV25N50 and 25XB800.

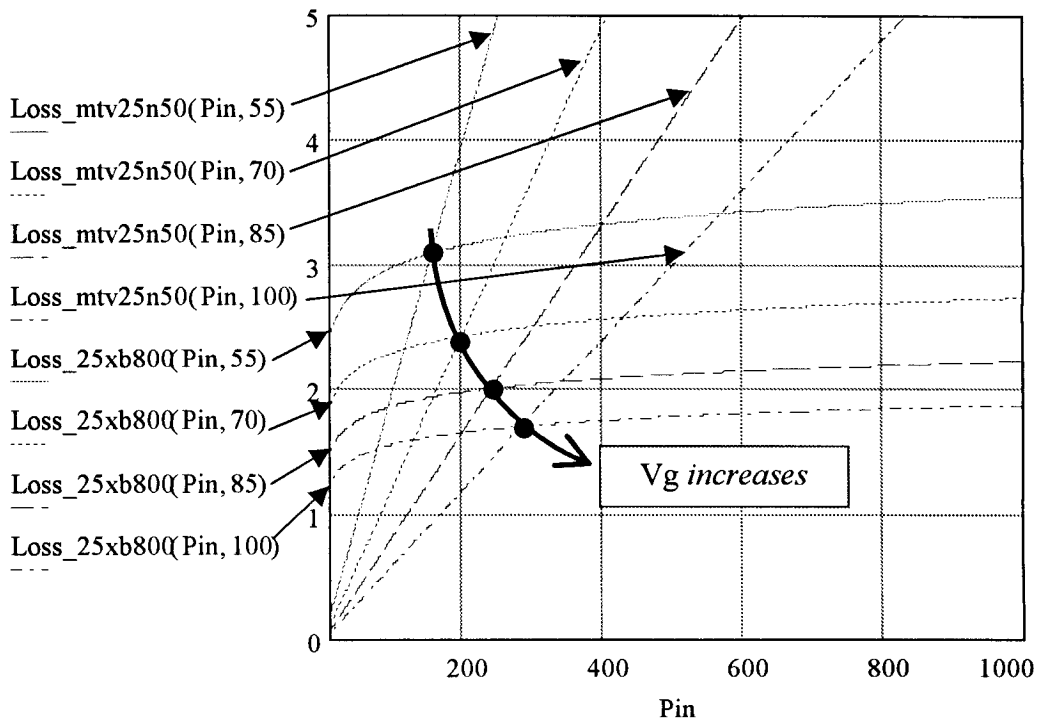

Figure 5.16: Losses [%] for input rectifiers based on MTV25N50 and 25XB800 as a function of power level, detailed. Input voltages 55, 70, 85 and 100 V

Investing into more expensive MOSFETs with better performance and their control therefore represents approach of gaining efficiency at any coast. Still, the advantage of such high performance synchronous rectifier will be limited, and the most critical area of converter operation, high input current (when input voltage is low, or/and load current is increased) is clearly the area of MOSFETs disadvantage.

5.3 Distortion and Noise

Another fact to consider is that any rectifier is a switching network, introducing corresponding EMI noise. Clearly, full wave diode rectifier will need an input voltage about $2V_d$=1.5V to start conducting. This fact leads to distortion of the current waveform even in case of pure resistive load after the rectifier – with no capacitor at all.

The worst distortion will be at lowest input voltage because the value of $2V_d$ to V_g ratio is the biggest in this case, and also because the current has the highest value under such condition, so noise harmonics will have the most significant amplitude for all region of converter operation. Fig. 5.17 shows the waveforms of input voltage, given by (5.3.1), and related current of diode rectifier with pure resistive load.

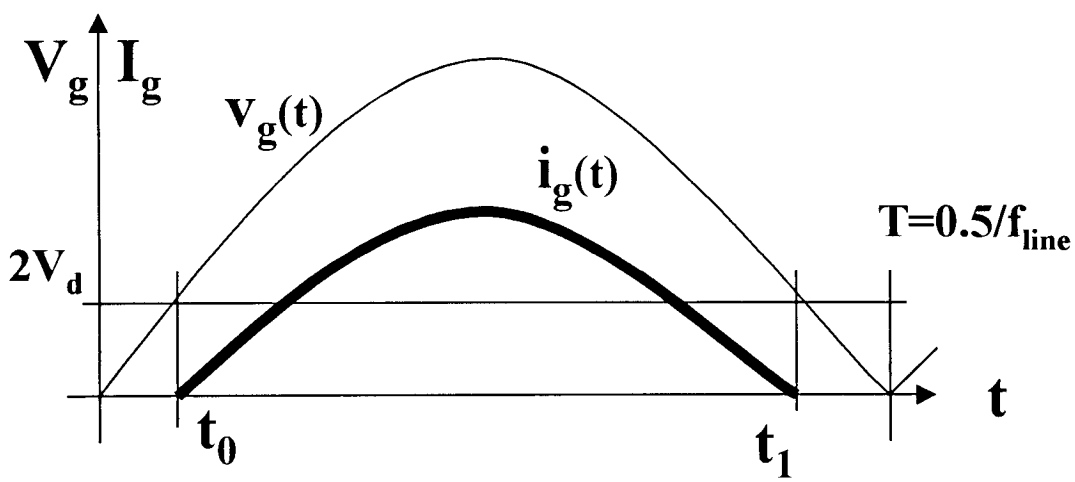

Figure 5.17: Waveforms for diode rectifier with pure resistive load

$$v_g(t) = \sqrt{2}V_{rms}\cos(\varpi t) \tag{5.3.1}$$

The time t_0 when input voltage reaches $2V_d$ and diodes start conducting is found by

(5.3.2)

$$t_0 = \frac{\cos^{-1}\left(\frac{2V_d}{\sqrt{2}V_{rms}}\right)}{2\pi f} \tag{5.3.2}$$

Same way, the time t1 when input voltage becomes lower than $2V_d$ can be found as (5.3.3), where T is a period of rectified input voltage which is related to twice of the line frequency f_{line} (60Hz)

$$t_1 = T - t_0 = \frac{1}{2f_{line}} - t_0 \tag{5.3.3}$$

The distorted waveform is illustrated in Fig. 5.18, where current of the rectifier clearly has a flat part at zero crossing. Input voltage was lower than critical 85 V to exaggerate the picture.

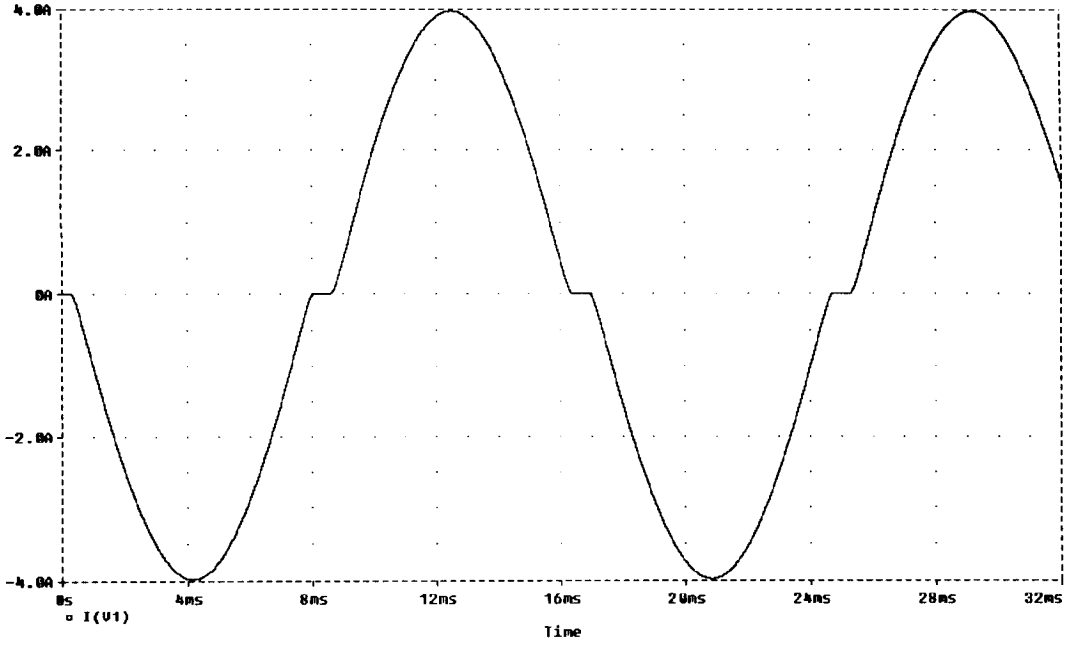

Figure 5.18: Distorted current waveform of the diode full wave rectifier

Harmonic content of the waveform in Fig. 5.18 is presented in Fig. 5.19 on the linear scale and in Fig. 5.20 on the logarithmic scale.

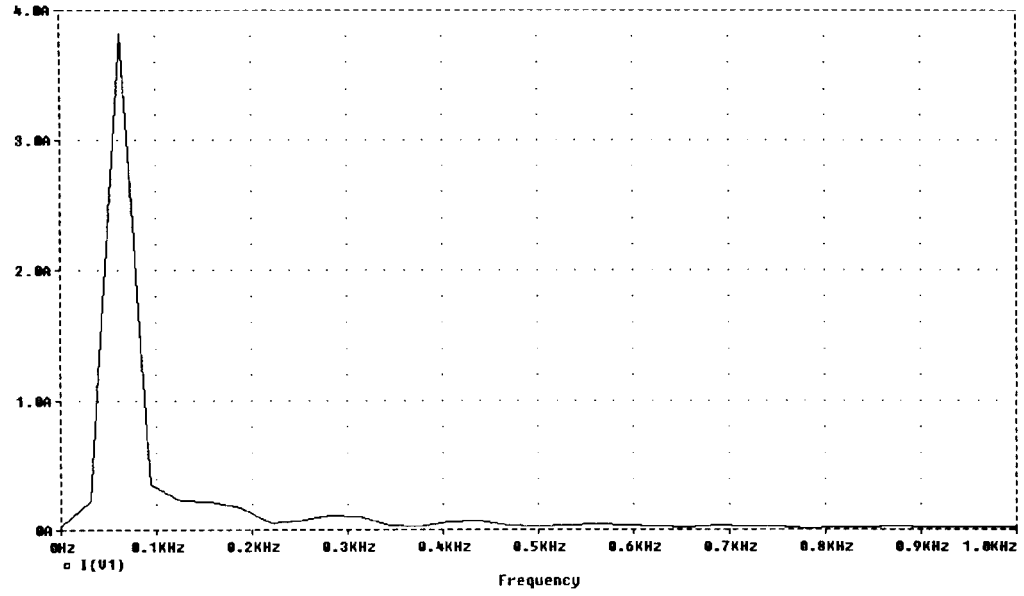

Figure 5.19: Harmonic content of the current waveform in Fig.5.18, linear scale

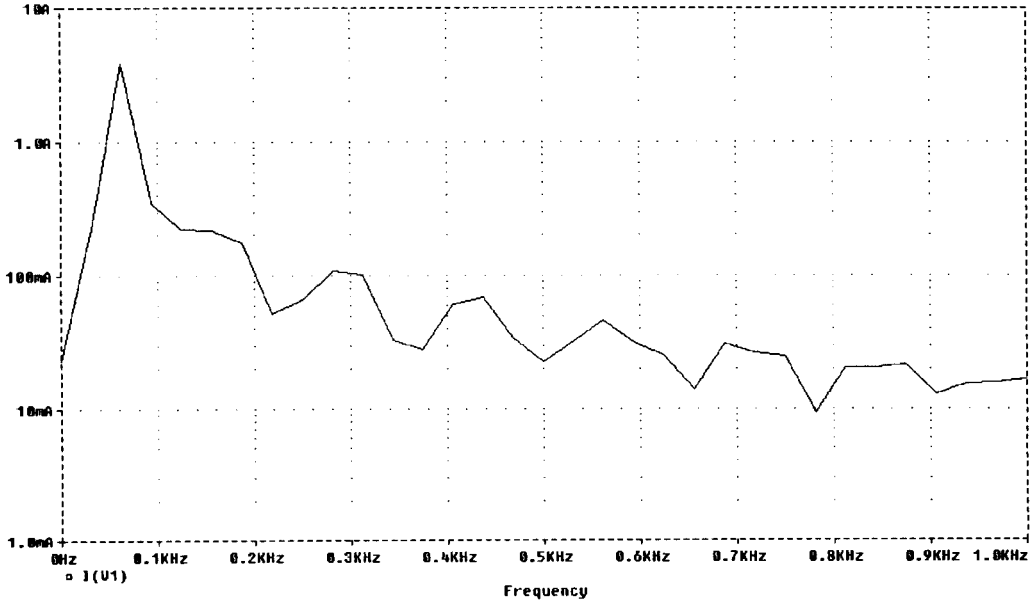

Figure 5.20: Harmonic content of the current waveform in Fig.5.18, logarithmic scale

The distortion occurs at low voltage region, where input current is also low. This fact leads to low relative amplitude of harmonics that have frequencies higher than fundamental. This problem is therefore of a less importance in comparison to distortions and power factor degrading considered in previous sections. This distortion is also decreased because of the presence of input filter, which is a usual part of PFC to filter switching frequency ripple and harmonics at higher frequencies.

However, this distortion and associated noise can become important in some applications, such as radio receiving. Such applications imply very high sensitivity of equipment and received power of the signal can be very low so additional efforts are done to minimize the rectifier noise. Extra capacitors can be used for this objective, as shown in Fig. 5.21.

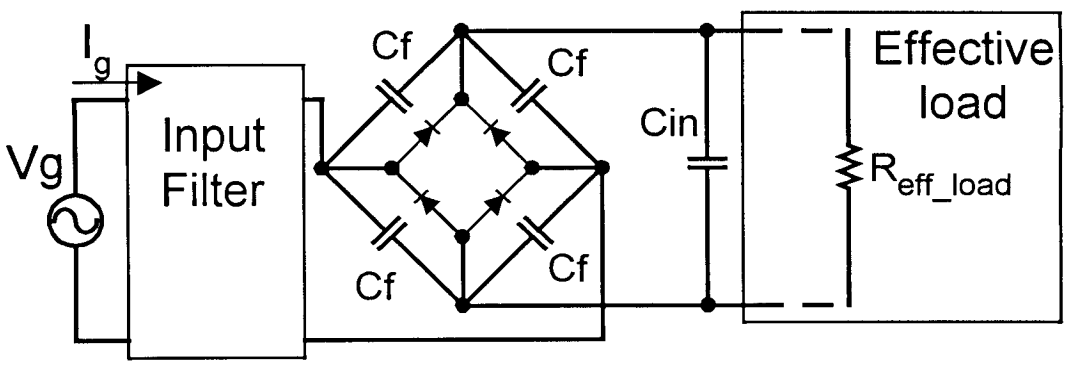

Figure 5.21: Usage of extra capacitors Cf to decrease rectifier noise

5.4 Input Rectification: Conclusions

It was established that input diode bridge introduces substantial losses in modern power factor correctors. These losses degrade the overall efficiency, which is one of the

most critical parameters in power transfer. These losses also cause concerns for thermal management, especially because it directly affects constant trend of minimizing the size of the equipment. Losses in the input diodes are hardly controllable by designers and can be minimized only in a small fraction by using high performance devices with lowest voltage drop at rated current, which basically implies using more of semiconductor material to improve current characteristics. This approach is extremely limited and leads to increase in cost.

The usage of active rectifier will always be more expensive and becomes totally inappropriate when voltage drop on the on-resistance of the active switches is higher than voltage drop on the diodes (which happens under high enough current). This is a most possible case when input voltage is low, so input current is high to provide necessary load power. This region of low input voltages is already critical from the point of view of overall converter efficiency, and the fact that rectifier has the worst performance in that region also amplifies the problem. The conclusion is that usage of synchronous rectifiers is really limited.

Fig. 5.22 illustrates graphically how losses are approximately distributed in the modern Power Factor Correctors. First, the input power of the converter is introduced on the left. Clearly, part of it is delivered to the load as output power, and other part is dissipated in the converter as losses. Modern PFCs have efficiency of 91-93% under normal conditions, so losses take about 7-9% of input power. As it was shown earlier in the section 5.1, the losses in diode rectifier can be of 2-4% order of input power, and reach much higher values if, for example, input voltage is decreased. These numbers

show that losses in input rectifier can be in 20%-57% range of the total losses in the converter. This is a very significant number.

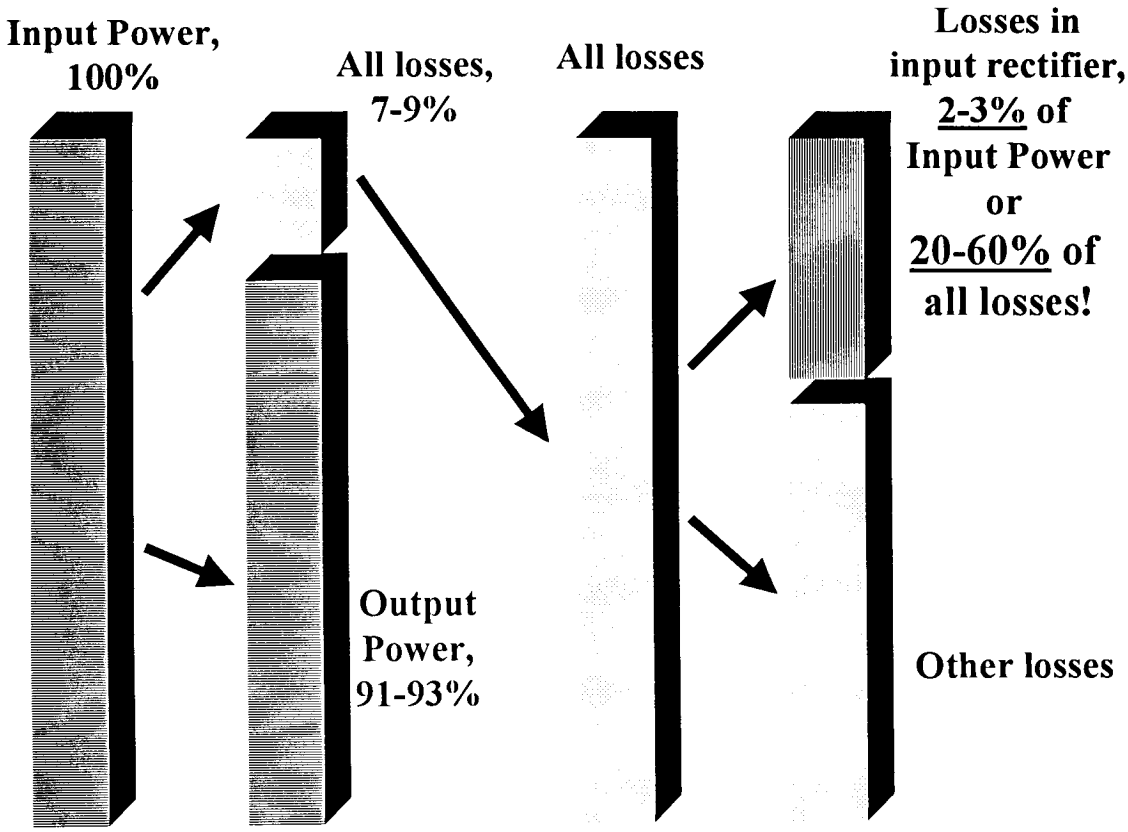

Figure 5.22: Illustration of losses in modern Power Factor Correctors

Input rectification also introduces a noise and distortion at the input of converter, which is usually not critical because of noise frequencies and amplitudes of the harmonics (and performance of input filter to deal with switching frequency ripple); however, it can become important in some applications.

Diode rectifier has four devices with high ratings for voltage and current, which leads to significant usage of the available space. Mentioned above heat sinking problem can even lead to additional space, weight and cost expenses because of the heatsinks for the

diodes. Synchronous rectifier only adds more space usage for control circuitry and affects the cost issue even further.

The elimination of input rectification is therefore an attractive goal because of many concerns.

Chapter 6

Novel Approach of Power Factor Correction

The purpose and reasons for eliminating of input rectification in power factor correctors were previously established. One possible general approach for such designs will be introduced in this chapter. First, general comments will be made about expectations from such topologies, including advantages and drawbacks. Then the new idea will be presented and some related issues will be considered. Finally, some suitable topologies and schematics will be discussed in more detail.

6.1 Expected Advantages of PFC without Input Rectification

Topology without input rectification would potentially have the following advantages in AC/DC application:

1) Such topology would not have uncontrollable losses in input rectifier bridge, which leads to efficiency improvement.
2) Heat management would be improved since substantial power dissipation, concentrated in small volume of input rectifier, would be eliminated.
3) Bridgeless schematics would not have 4 high-power elements: diodes rated for high voltage and currents or even more expensive combination of high performance MOSFETs and control for these active switches. This issue potentially affects a cost and size of the considered converters.
4) Such circuits would have less nonlinear elements: simpler design and analysis, better performance in terms of EMI, input filter excitation, control.

5) The new approach also introduces simplified input filter considerations, which also affects cost and size of the designed equipment.
6) It will be also shown that the absence of input rectifier enables some unique features to improve the power factor by including the input filter into operation of power factor correctors. It also allows to sense the input voltage right on the voltage source, at the very input of all schematic, which provides much better noise immunity and supplies PFC chips with exact waveform of input voltage, not affected by performance of input filter, switching frequency ripple or loading effects.

On the other hand, topology without input rectification would have to have some special features and this fact introduces the following general expected drawbacks:

1) Such schematics would introduce less freedom in choosing power stage. It will be shown that special voltage gain characteristics are needed, so only specific topologies could be used in this new approach of Power Factor Correction.
2) Special types of control algorithms are expected to be necessary. New topologies imply some specific control methods; they also imply possible complications in schematics of voltage and current sensing, compared to conventional circuits.

6.2 Introduction of the New Approach for PFC

New class of the converters arises easily out of the problem consideration. When there is no input rectification, then input voltage of the converter changes polarity, while output voltage has to be constant. This leads to consideration of the converters with specific gain characteristics. If some topology has positive and negative parts of gain characteristics (i.e., it can produce positive or negative output voltage from just positive

input), then it can produce strictly positive output voltage from any (positive or negative) input. Such topologies will be called topologies with bipolar gain characteristics. If suitable control is found, then such topology can implement PFC as well, and therefore produce positive DC output from non-rectified AC input.

It is necessary to point out that although some particular examples will be analyzed in this thesis, and some experimental results will be presented, the idea is general and other topologies and control circuits can be used.

Consider some conventional PFC topology in Fig. 6.1. Output voltage V_0 is kept at necessary value by the feedback that defines steady state duty ratio D_0, according to particular voltage gain characteristic $M(D)$ of the power stage (6.2.1), where Vg is rms value of input voltage. Practically, duty ratio D is varied in some region of D_0 by some control method to provide power factor correction $D=D_0+d$.

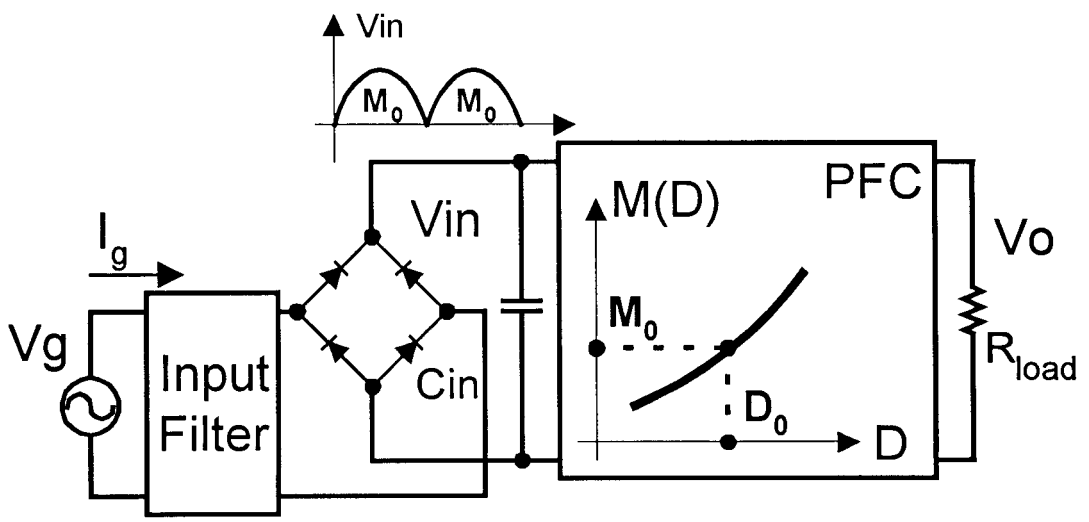

Figure 6.1: Conventional PFC schematic

$$D_0 = f\left(M = \frac{Vo}{Vg}\right) \tag{6.2.1}$$

Related waveforms are shown in Fig. 6.2. Input voltage V_g is rectified so converter operates in exactly the same way with steady state voltage gain M_0 every half of the line cycle.

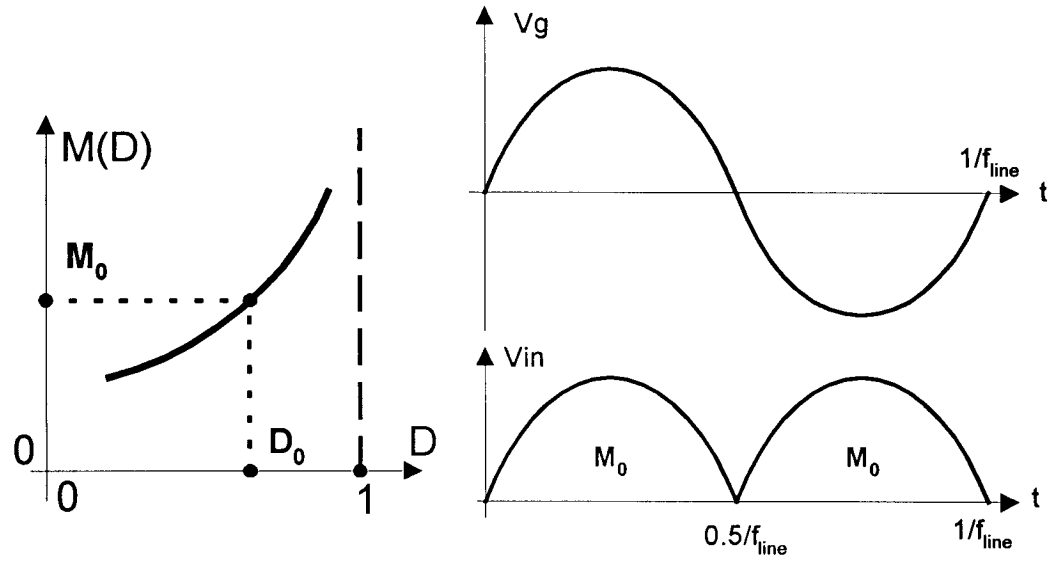

Figure 6.2: Waveforms for conventional PFC schematic in Fig.6.1

Assume that some topology has positive and negative branches of voltage gain characteristic. Then it is possible to operate power stage in area of M_+ of the positive branch of gain characteristic when V_g is positive, and in the area of M_- of the negative branch when input voltage becomes negative, Fig. 6.3. Related waveforms are shown in Fig. 6.4. M_+ and M_- are steady state values of the voltage gain for positive and negative branch respectively. Clearly, the feedback should provide such values for the D_+ and D_- that $M_+ = M_- = M_0$ to support necessary output voltage.

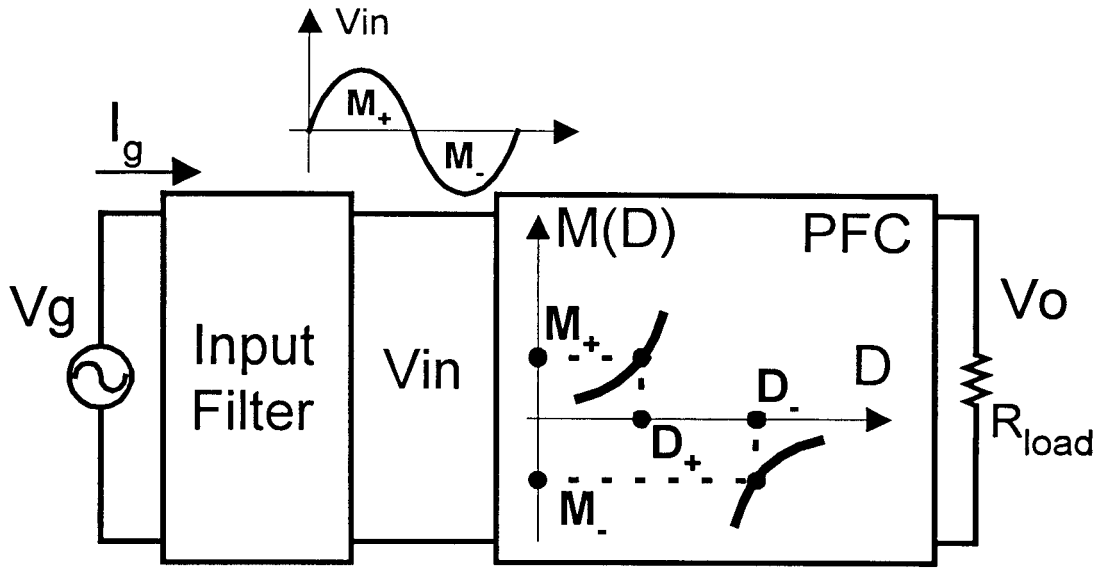

Figure 6.3: Schematic of the proposed PFC

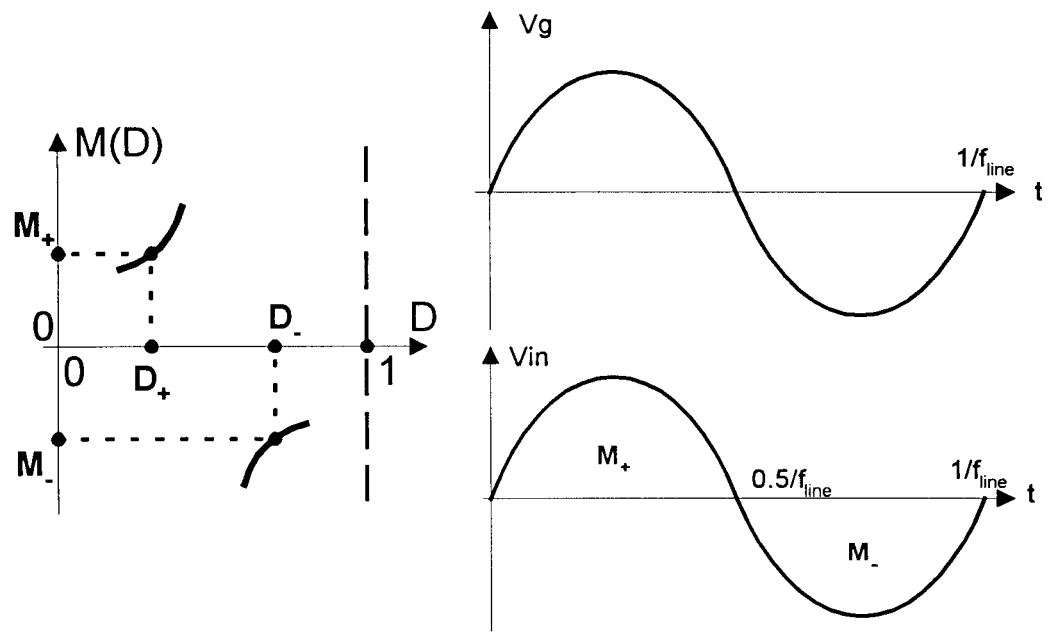

Figure 6.4: Waveforms for the proposed PFC schematic in Fig.6.3

Power factor correctors based on the new approach allow realizing advantages commented in previous section 6.1. Quite a few topologies with appropriate characteristics can be found or derived, but it turned out that special characteristics of the switches are needed in some cases when it comes to practical implementation.

6.3 Four Quadrant Switches

Diode represents passive switch and transistor (usually MOSFET) represents active (controlled) switch. However, there is more general classification in terms of conducting the current and blocking the voltage. Fig.6.5 shows directions of the current *Ic* that diode and MOSFET can conduct and polarity of voltage *Vb* that these switches can block.

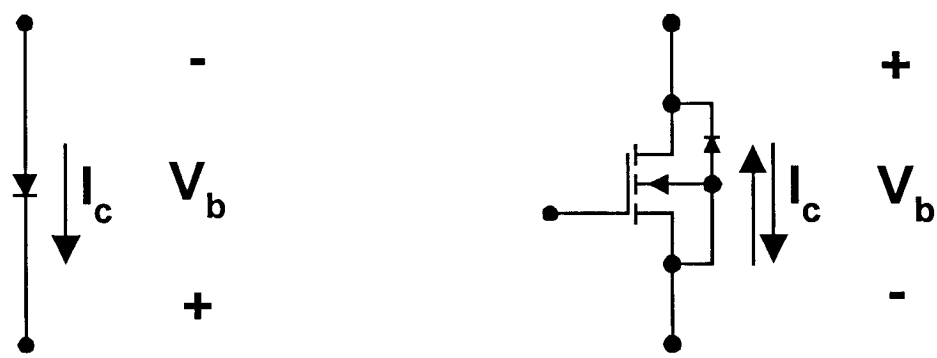

Figure 6.5: Diode and MOSFET conducting currents and blocked voltages

Notice that MOSFET has a so-called body diode as part of the package and can therefore conduct current in both directions, so these transistors can be called current bi-directional switches. Body diode of the MOSFET is a somewhat parasitic product. External diode with better performance is often connected parallel to MOSFET, although all manufacturers try to improve DC and dynamic characteristics of the body diodes.

There is a special issue how to make sure that this external diode conducts and effect of the body diode with significantly longer reverse recovery time is minimized.

Example of voltage bi-directional switch is shown in Fig. 6.6. This switch can block voltage of both directions and conduct current only in one.

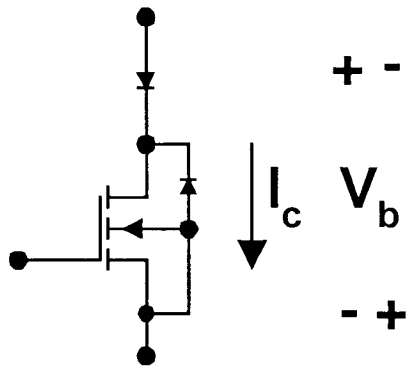

Figure 6.6: Voltage bi-directional switch

The classification becomes clear when voltage/current plane is considered, Fig. 6.7. Diode can conduct current in one direction and block voltage of one direction, so diodes occupy first quadrant I on V/I plane.

Similarly, voltage and current bi-directional switches are displayed, occupying I&II and I&IV quadrants respectively. The ideal switch, which is similar to mechanical connection/disconnection of two conductors, should conduct current in any direction and block the voltage of any polarity, so it is called four quadrant switch and would occupy all four quadrants in Fig. 6.7.

Some of applications considered further require the implementation of four quadrant switches, so this topic will be investigated. Four quadrant switches can be designed by

connection of two current bi-directional or two voltage bi-directional switches, Fig. 6.8 a) and b) respectively.

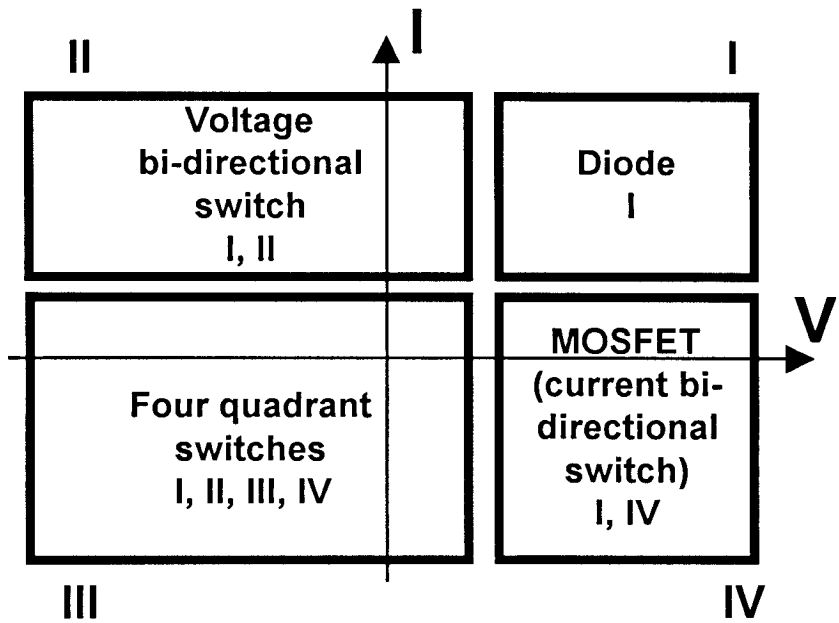

Figure 6.7: Switch classification

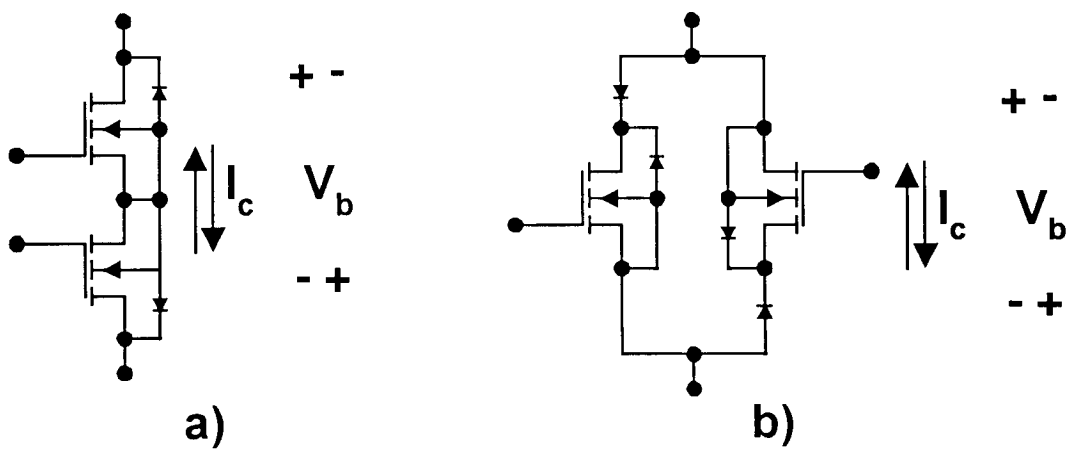

Figure 6.8: Possible four quadrant switch implementations

Switch in Fig. 6.8 can be modified by changing one n-channel MOSFET to p-channel so better drive option is available, Fig. 6.9 a). However, the p-channel MOSFETs are known for much worse performance – they have much higher on resistance in comparison to compatible n-channel MOSFETs of the same voltage rating. Fig. 6.9 b) presents yet another possibility to implement a four quadrant switch – with only one active element. However, the losses in such configuration are definitely the highest among all presented four quadrant switches so far because is has on resistance of the MOSFET and two diodes in series connection as a path for the current.

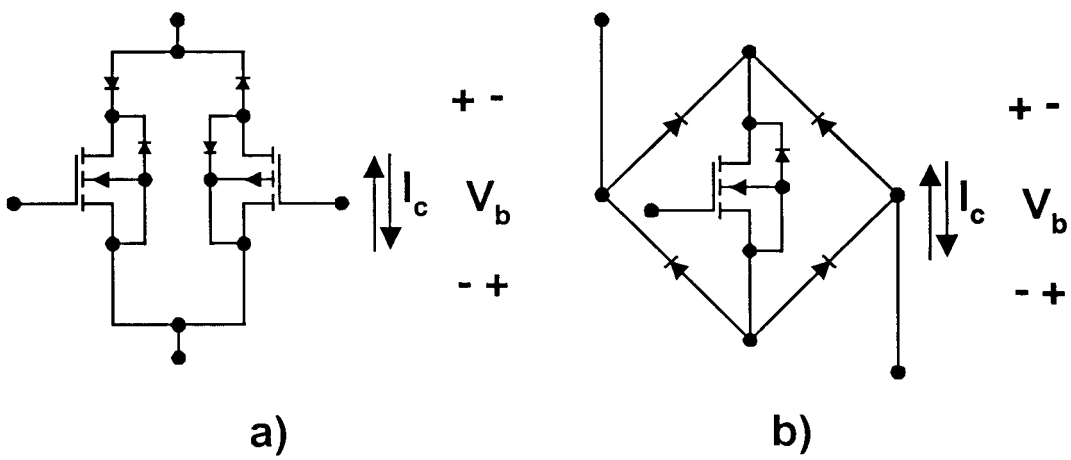

Figure 6.9: Other possible four quadrant switch implementations

The optimal choice is the connection of two current bi-directional switches as in Fig. 6.8 a), modified for simpler driving, see Fig. 6.10. The losses in this switch are associated with on resistance of only one MOSFET and a parallel connection of the diode and on resistance of other MOSFET – when voltage of any polarity is applied.

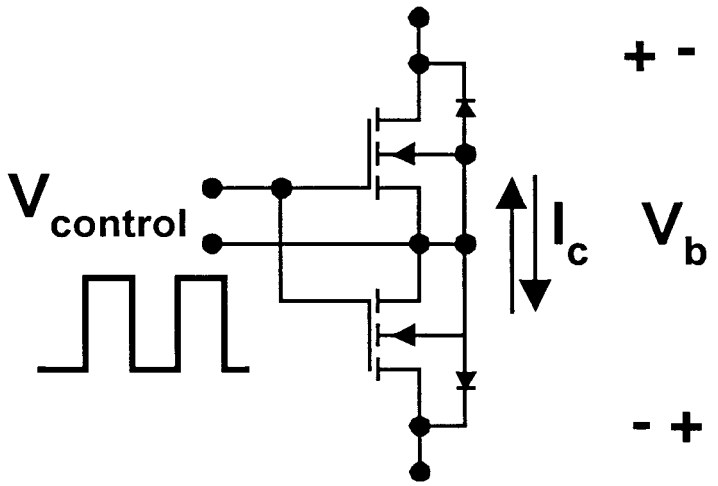

Figure 6.10: The optimal four quadrant switch

Clearly, isolated drive is needed for such configuration. Notice that the n-channel MOSFET that has minus on drain node and plus on the source node can not have this voltage higher than voltage drop of its body diode, so although MOSFET behaves in a usual way under such inverse polarity of voltage, no Miller effect is present. This leads to the fact that this reverse biased transistor turns on easily and without consuming high current at the gate.

On the other hand, MOSFETS share the current and therefore turn on and off at the same time. This fact leads to the situation that body diodes of neither MOSFETs have a problem of reverse recovery time affecting the circuit. In fact, the only possibility for one body diode to conduct is if current through the switch is so high that voltage drop on the on resistance of the related MOSFET would be higher than voltage drop across the body diode. This can be avoided if necessary by using a MOSFET with lower on resistance. Notice that even in case the body diode starts conducting, the MOSFET

channel would still take at least part of the current, which equals to V_d/R_{on}, where V_d is a drain to source voltage on the MOSFET, limited to voltage across conducting body diode, and R_{on} is on resistance of the device.

Described configuration has only one port with two nodes for control signal, which is another advantage in comparison to some other presented topologies. Also notice that gates and sources of both the MOSFETs are connected in parallel, which can potentially offer some additional simplifications in circuit layout or even device packaging.

The four quadrant switches can conduct the current in any direction and block the voltage of any polarity, so potentially they can be used in any switching power stage with arbitrary switch requirements. However, very often more simple switches can be chosen to perform; the actual design depends on properties of particular topology and careful analysis of all its possible modes of operation under condition of non-rectified AC input voltage.

6.4 Different Topologies with Bipolar Gain Characteristics

Many topologies with bipolar gain characteristics exist. It is important to clarify the classification of step-up and step-down topologies in such case when there are clearly two parts of gain characteristic – positive and negative. If positive and negative characteristics of the topology have the regions of voltage gain values from "1" to "0" and from "0" to "–1" respectively: such topologies will be called step-down topologies. If positive and negative characteristics of the topology have the regions of voltage gain values from "1" and up and from "–1" to more negative values respectively: such topologies will be called step-up topologies.

Example of the topology with bipolar voltage gain characteristic is shown in Fig. 6.11. This is a derivation from one of the eight circuits from the complete set of DC/DC topologies, employing one transistor and one diode, generated in [15]. Implementation of such circuit in AC/DC condition will require extra analysis and changes in switch realization, so simplest version of the topology is presented for now.

The following equations are valid if assumption that this circuit has steady state is correct:

$$\frac{1}{L1}(Vg - Vc)DT_s + \frac{1}{L1}(Vg - V_0)D'T_s = 0 \tag{6.4.1}$$

$$\frac{1}{L2}(-Vo)DT_s + \frac{1}{L2}(-Vc)D'T_s = 0 \tag{6.4.2}$$

$$\frac{1}{C1}IgDT_s - \frac{1}{C1}I'D'T_s = 0 \tag{6.4.3}$$

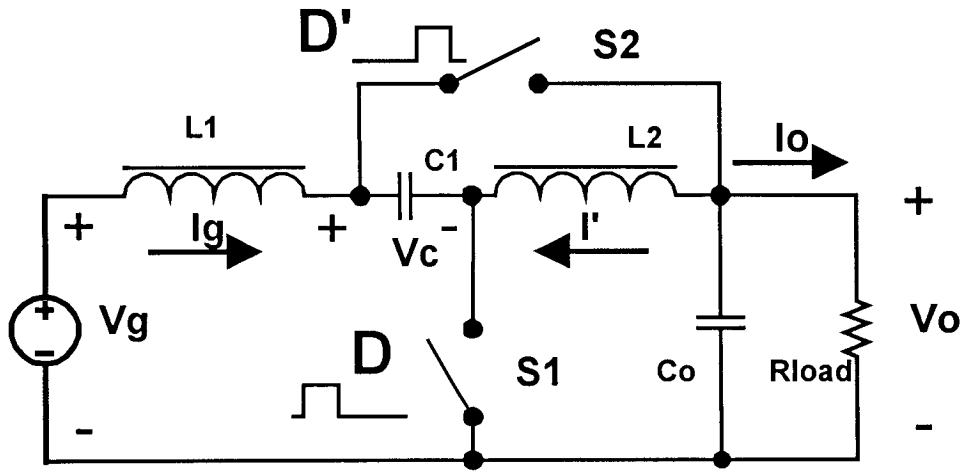

Figure 6.11: Example of the topology with bipolar voltage gain

Circuit has three reactive elements: *L1*, *L2* and *C1* (*Co* is assumed to have a big value, which is a realistic situation to avoid ripple of output voltage, so output voltage does not change much. Three variables have to be found to describe the steady state of the circuit: inductor currents *Ig* and *I'* and capacitor voltage *Vc*. Solution will confirm the assumption that this topology does have a steady state.

The system of equations can be solved for *M(D)=Vo/Vg*. First, the (6.4.3) can be simplified to (6.4.4); then (6.4.5) can be written by inspection, considering the components of the output current *Io* and the way that switches *S1* and *S2* operate.

$$IgD - I'D' = 0 \tag{6.4.4}$$

$$IgD' - I'D = Io \tag{6.4.5}$$

The voltage gain of the power stage can be finally expressed as (6.4.6), same time finding relation (6.4.7) from (6.4.4) and (6.4.5)

$$M(D) = \frac{Vo}{Vg} = \frac{1-D}{1-2D} \tag{6.4.6}$$

$$\frac{Io}{Ig} = \frac{1-2D}{1-D} = \frac{1}{M(D)} \tag{6.4.7}$$

Derived voltage gain *M(D)* (6.4.5) is plotted in Fig. 6.12. The implementation of switches is omitted for now, but it will be shown later than under condition of strictly positive output voltage with higher value than the peak of *Vg* – simple MOSFETs can be used as switches, without implementing four quadrant configurations.

This gain characteristic shows that topology in Fig. 6.11 can be classified as step–up topology, in other words – given some input voltage *Vg* the output voltage can be set to

value of any polarity with the amplitude higher than input voltage. The full classification is therefore "step-up topology with bipolar voltage gain."

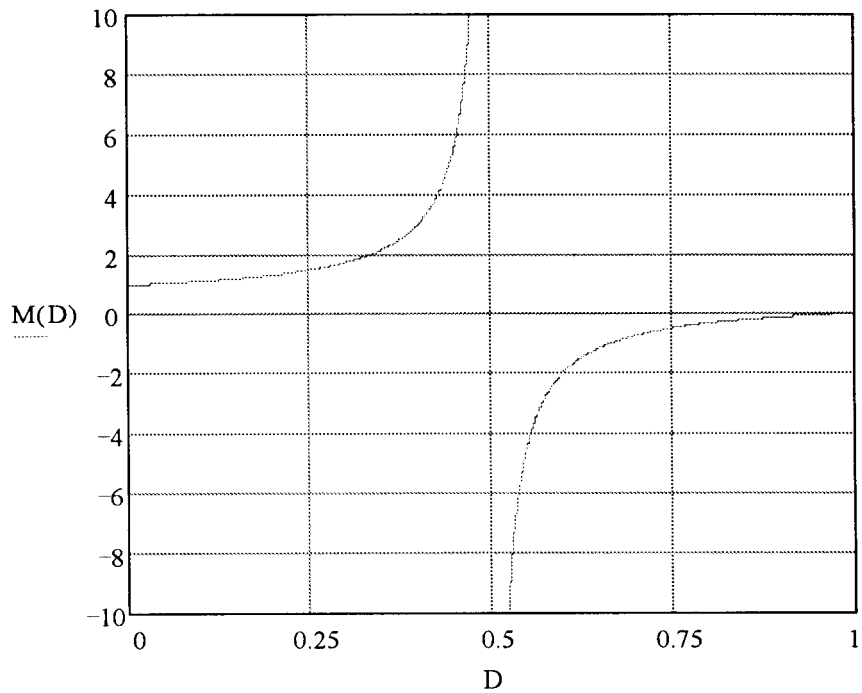

Figure 6.12: Ideal gain characteristic M(D)=(1-D)/(1-2D)

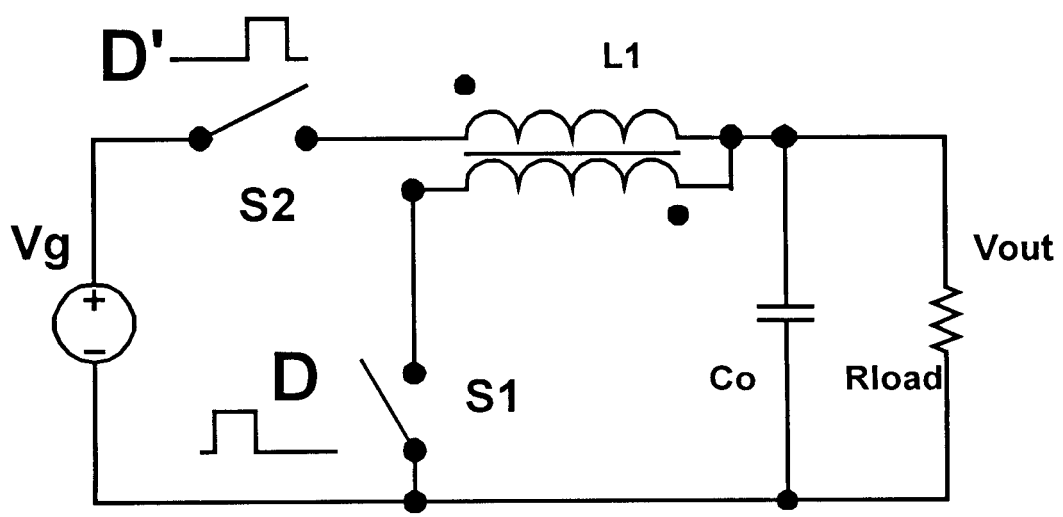

Figure 6.13: Buck derived topology with bipolar voltage gain M(D)=(1-D)/(1-2D)

Another topology is presented in Fig. 6.13. The gain characteristic of this buck derived topology can also be found as (6.4.6).

Step-down topologies, related to step-up circuits in Fig. 6.11 and Fig. 6.13, exist; see Fig. 6.14 and Fig. 6.15 respectively.

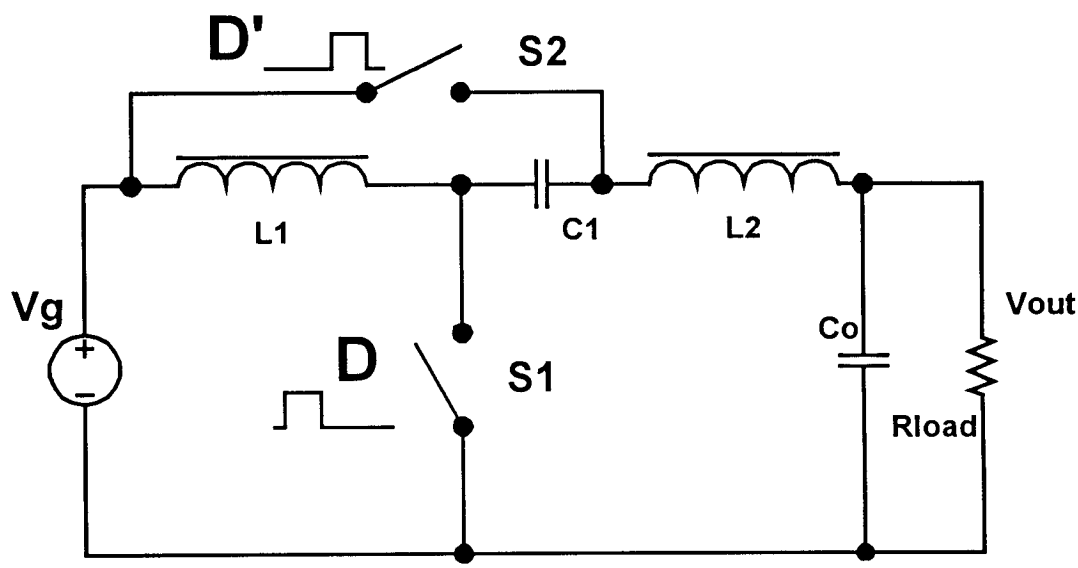

Figure 6.14: Step-down topology with bipolar voltage gain M(D)=(1-2D)/(1-D)

The voltage gain *M(D)=(1-2D)/(1-D)*, see (6.4.8), is plotted in Fig. 6.16 and corresponds to ideal characteristics of topologies in Fig. 6.14 and Fig. 6.15. Notice that these topologies can produce output voltage of any polarity with amplitude lower than absolute value of input voltage. These topologies can be therefore classified as "step-down topologies with bipolar voltage gain."

$$M(D) = \frac{Vo}{Vg} = \frac{1-2D}{1-D} \tag{6.4.8}$$

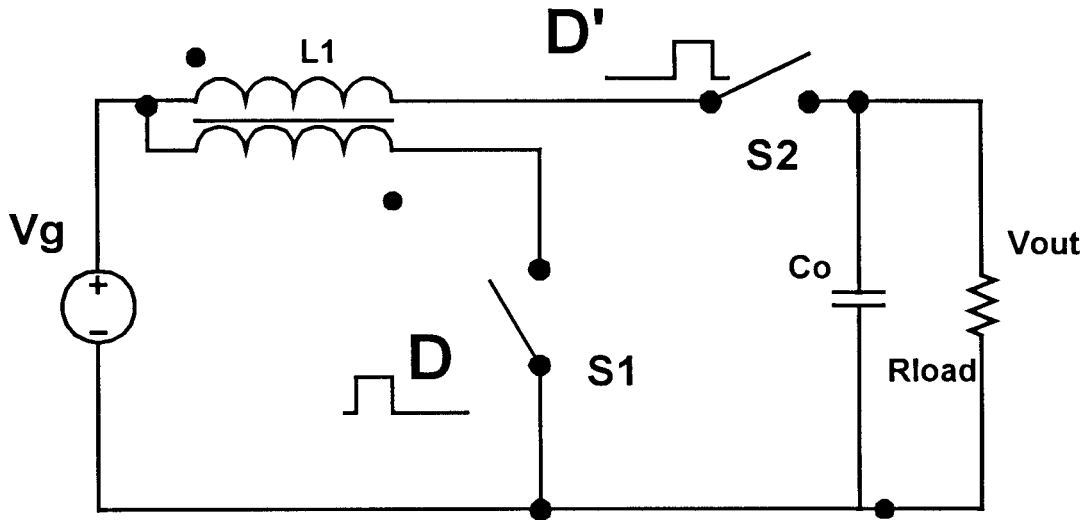

Figure 6.15: Boost derived topology with bipolar voltage gain M(D)=(1-2D)/(1-D)

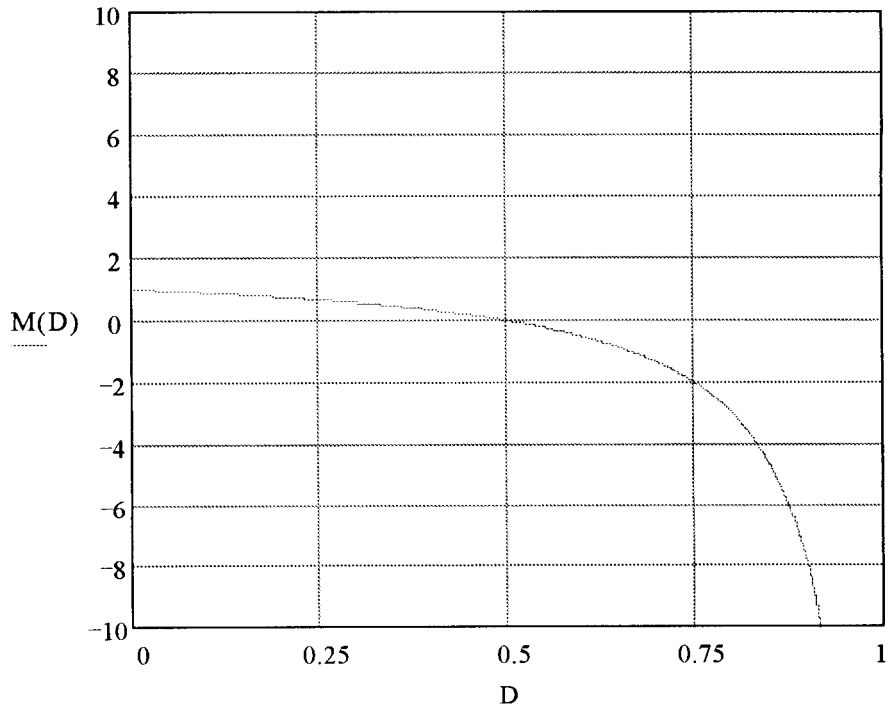

Figure 6.16: Ideal gain characteristic M(D)=(1-2D)/(1-D)

Some other topologies with bipolar gain characteristic will be reviewed briefly. Inverted Watkins-Johnson converter, shown in Fig. 6.17, has step-up voltage gain characteristic $M(D)=(1-D)/(1-2D)$; its cousin in Fig. 6.18 has step down characteristic as $M(D)=(1-2D)/(1-D)$.

Ideal gain characteristics of all topologies with bipolar gain are being considered, unless otherwise noted. Introduction of parasitic elements and associated losses will change ideal gain characteristics closer to realistic ones. This more detailed consideration will be conducted when some topologies will be considered in more detail.

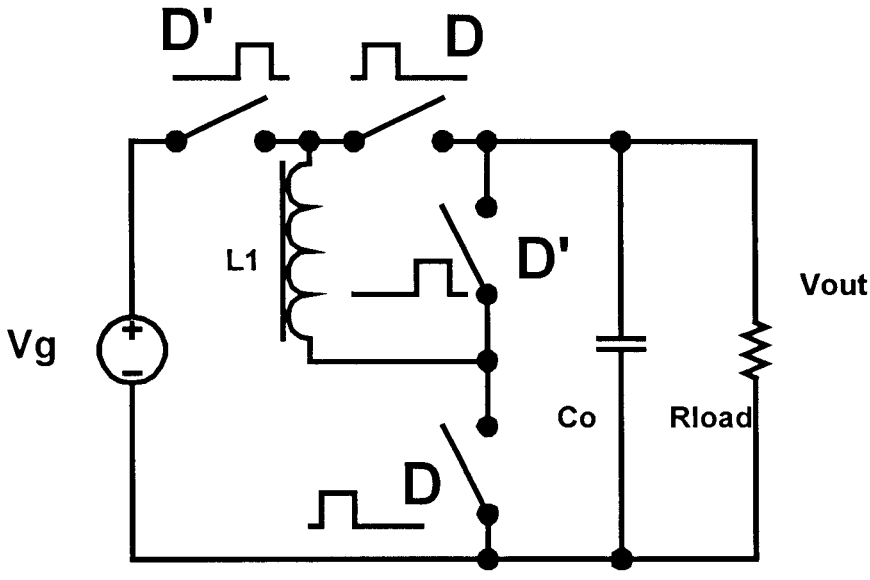

Figure 6.17: Inverted Watkins-Johnson converter with M(D)=(1-D)/(1-2D)

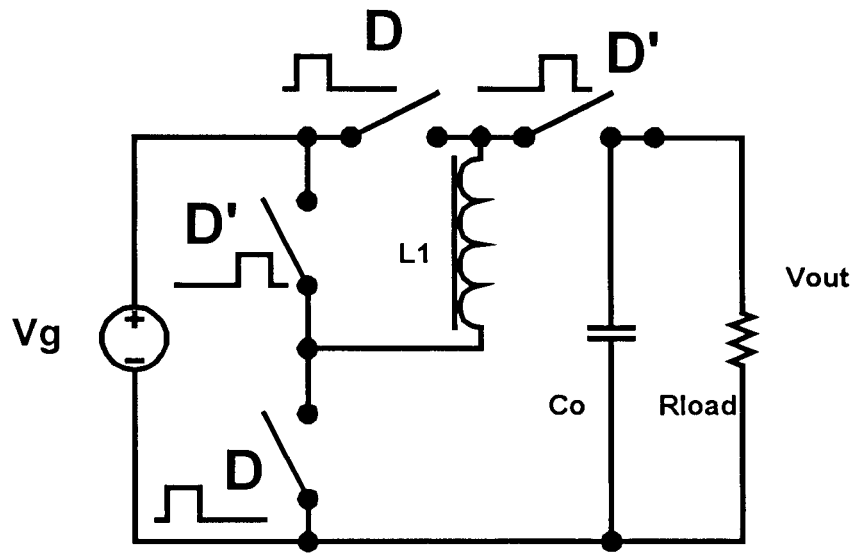

Figure 6.18: Step-down WJ converter with bipolar characteristic M(D)=(1-2D)/(1-D)

The reviewed topologies so far had voltage gain characteristics shown in Fig. 6.12 or 6.16. There are also topologies with other bipolar gain characteristics. Fig. 6.19 illustrates current fed full bridge with voltage gain (6.4.9), plotted in Fig. 6.20.

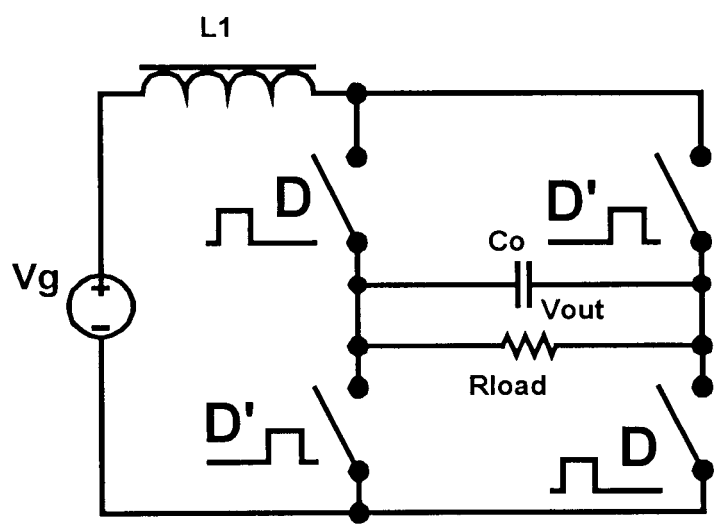

Figure 6.19: Current fed full bridge with voltage gain M(D)=1/(2D-1)

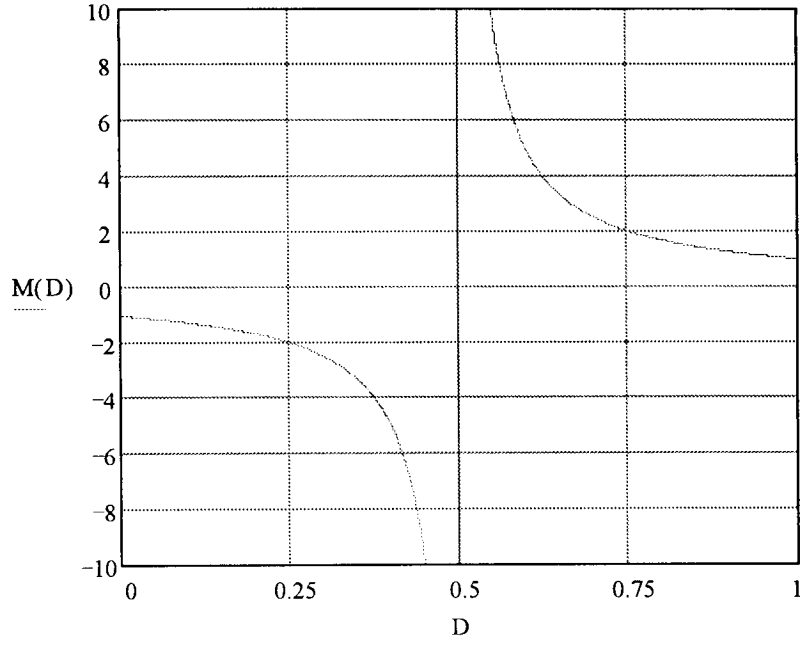

Figure 6.20: Gain characteristic M(D)=1/(2D-1) for current fed full bridge in Fig. 6.19

The characteristic *M(D)=2D-1*, plotted in Fig. 6.20 classifies current fed full bridge as step-up topology.

$$M(D) = \frac{Vo}{Vg} = \frac{1}{(2D-1)} \tag{6.4.9}$$

Full bridge in Fig. 6.21 has voltage gain characteristic as (6.4.10), which is plotted in Fig. 6.22. This characteristic classifies the circuit as step-down topology. The full bridge circuit is quite symmetric; notice the symmetry of characteristics in Fig. 6.20 and Fig. 6.22.

$$M(D) = \frac{Vo}{Vg} = (2D-1) \tag{6.4.10}$$

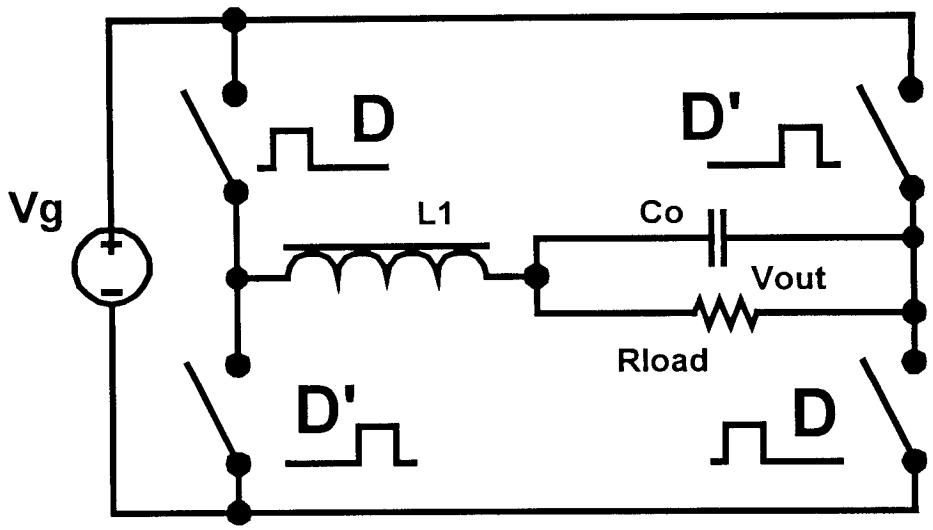

Figure 6.21: Full bridge topology with voltage gain M(D)=(2D-1)

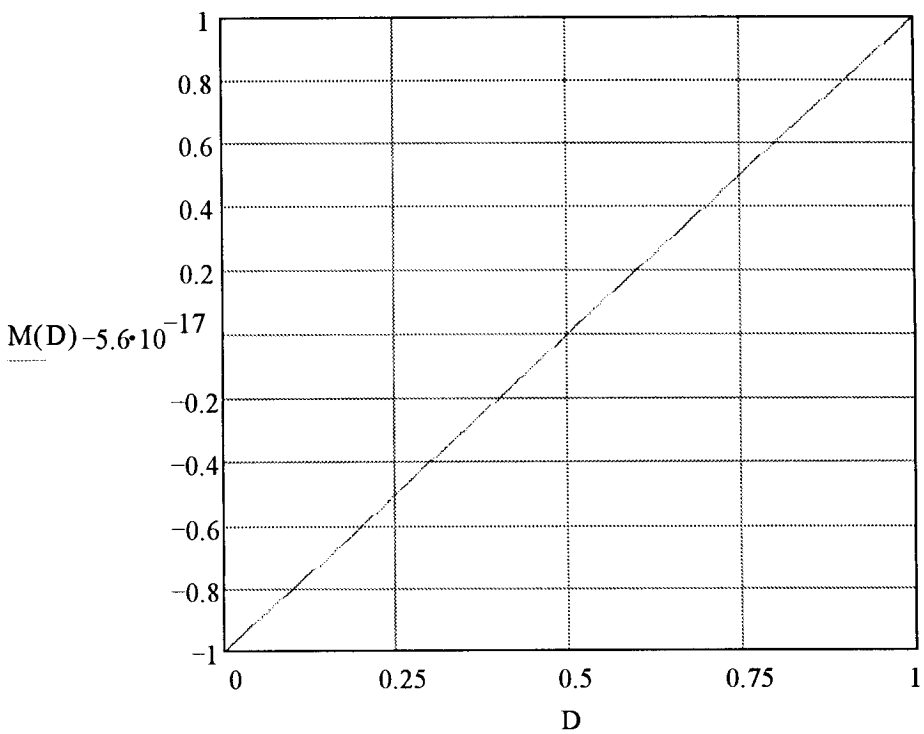

Figure 6.22: Gain characteristic M(D)=(2D-1) for full bridge in Fig. 6.21

It is necessary to point out, that well known general differential schematic in Fig. 6.23 could also be considered as a topology with bipolar gain characteristic. Output voltage can be expressed as (6.4.11) and can be any polarity.

$$Vo = Vg\left(M(D) - M(D')\right) \tag{6.4.11}$$

However, schematic in Fig. 6.23 is a specific connection of two basic power stages, and therefore it does not represent a single topology. It also has load connected differentially, which is often a disadvantage.

Described differential topology is mainly used for specific applications, such as audio power amplifiers, etc.

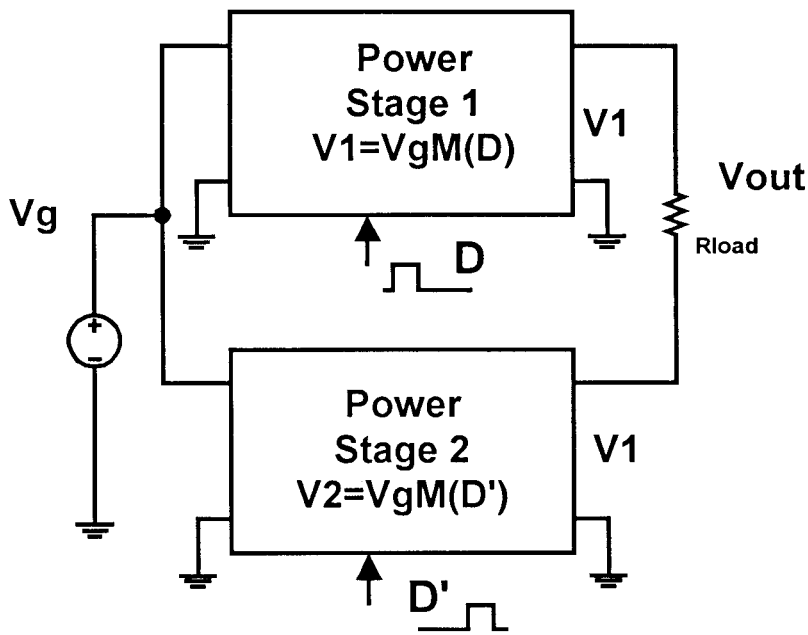

Figure 6.23: Differential load connection to two power stages

Another circuit is shown in Fig. 6.24. Inverters of such kind can also produce output voltage of any polarity, and such configurations also could be considered as topologies with bipolar gain characteristic.

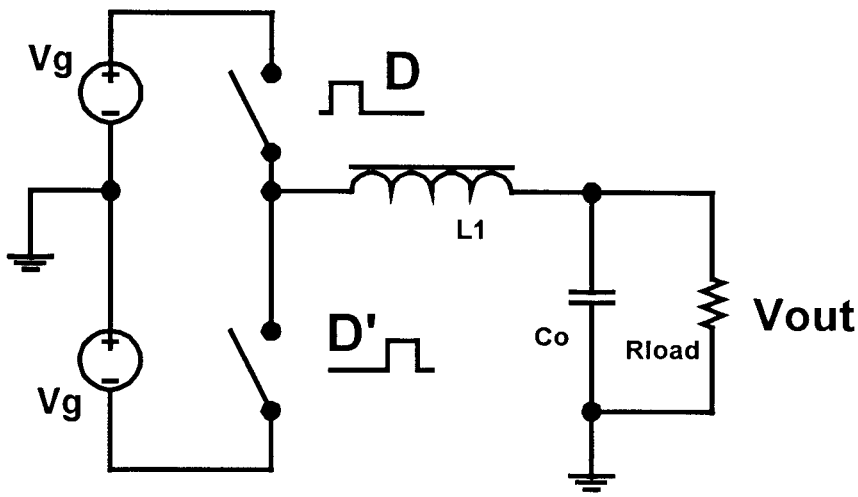

Figure 6.24: Inverter with voltage gain M(D)=2D-1

The gain expression is equivalent to (6.4.10). This circuit, however, implies two input voltage sources to be able to function, and represents certain special case, not suitable for power factor correction where by definition there is only one input voltage source.

6.5 Switch Implementation in Topologies with Bipolar Gain

The implementation of the switches in these topologies needs to be addressed. This issue is important, because it will affect switch losses and overall converter efficiency as well as control, therefore influencing the choice of the topology.

The general procedure is outlined, for example, in [14]. Conducting currents and blocked voltages are found for all switches of the topology, as illustrated in section 6.3, then these combinations will show what kind of switch is needed in each case. In fact, formal rule can be used: if voltage and current are in related direction (conducting current flowing during on time flows from positive node to negative node of blocked voltage during off time), then the product of current and voltage is positive and MOSFET should be chosen. If the product of conducting current and blocked voltage is negative in that notation: diode should be used. Notice that in PFC application without input rectification, the procedure should be done for positive and negative voltage separately, to insure proper operation. Several examples of the switch implementation will be shown.

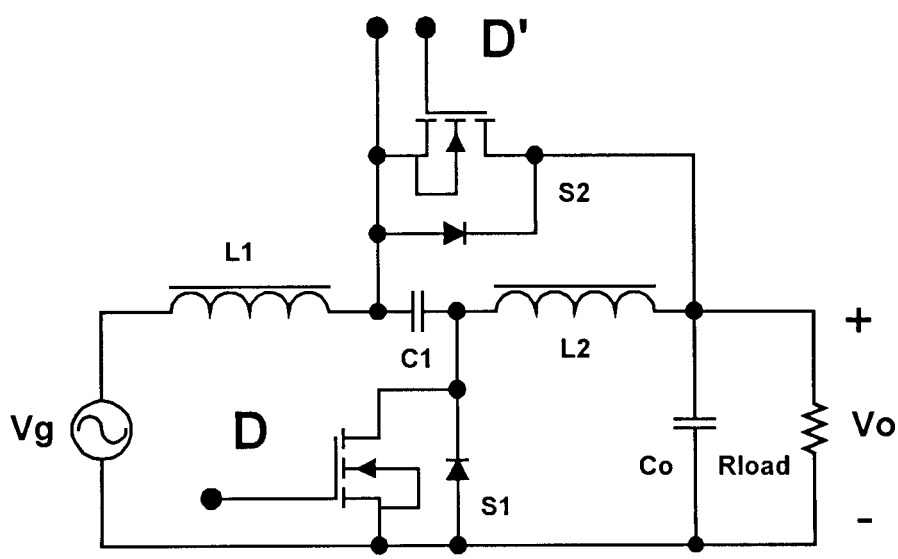

Figure 6.25: Switch implementation for topology from Fig.6.11; M(D)=(1-D)/(1-2D)

Fig. 6.25 and 6.26 show switch implementation for step-up converters with voltage gain *M(D)=(1-D)/(1-2D)* from Fig. 6.11 and Fig. 6.13 respectively.

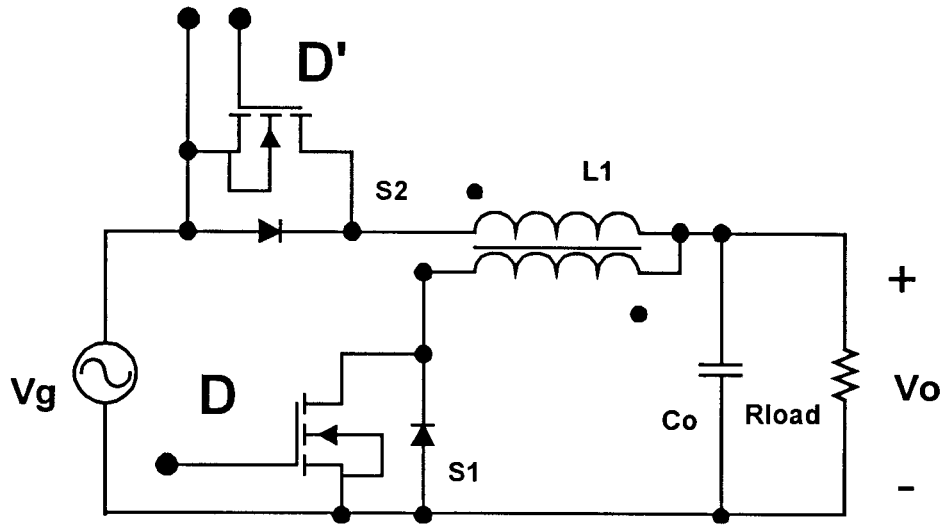

Figure 6.26: Switch implementation for topology from Fig.6.13; M(D)=(1-D)/(1-2D)

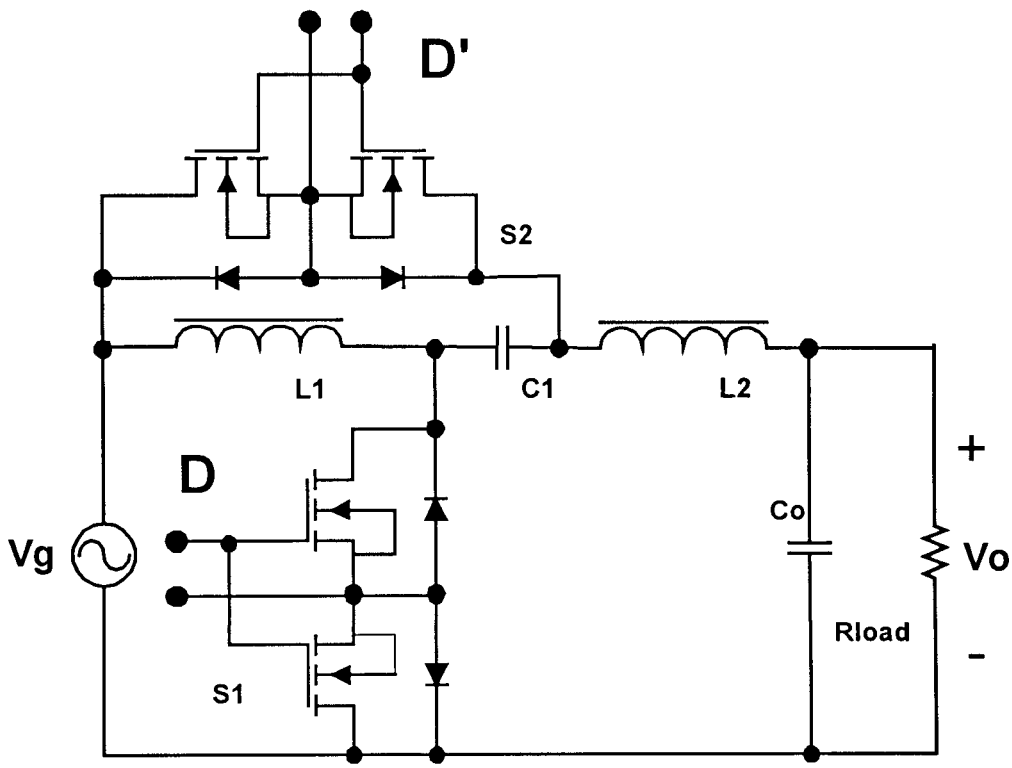

Figure 6.27: Switch implementation for topology from Fig.6.14; M(D)=(1-2D)/(1-D)

Fig. 6.27 and 6.28 show switch implementation for step-up converters with voltage gain *M(D)=(1-2D)/(1-D)* from Fig 6.14 and Fig. 6.15 respectively.

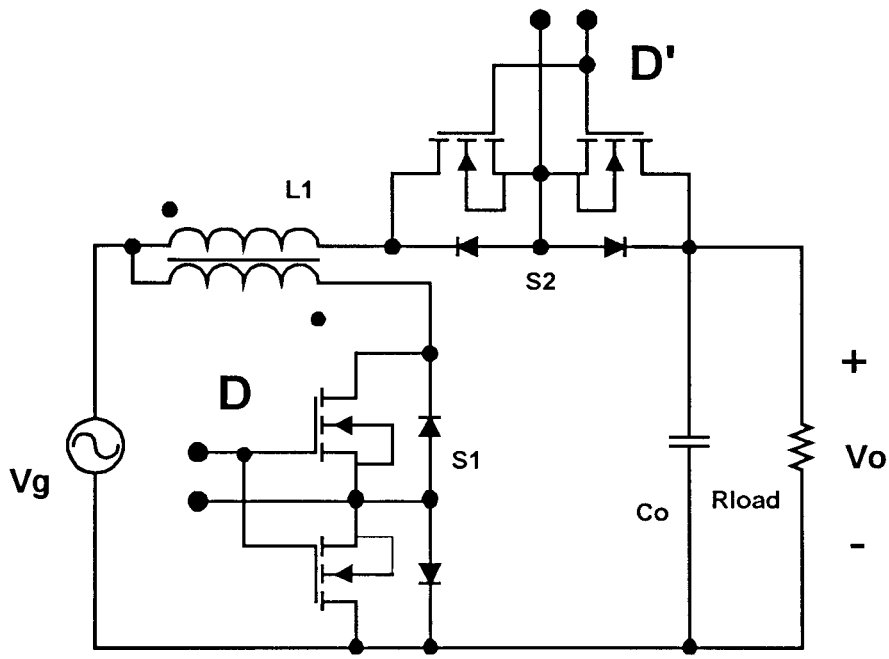

Figure 6.28: Switch implementation for topology from Fig.6.15; M(D)=(1-2D)/(1-D)

Notice that for step up topologies in Fig. 6.25 and Fig. 6.26 the output voltage is always higher that input voltage – for any polarity of input voltage. This condition leads to the fact that switches have to block voltages of the same polarities during positive or negative halves of the line cycle, which results to simple realization of the switches. Simple MOSFETs are possible to be used even without external diodes. Current bi-directional switches are needed in this case and body diodes of the MOSFETs can provide conducting current in extra direction unless better performance is needed.

Situation is different for the step-down topologies in Fig. 6.27 and Fig. 6.28. The input voltage is lower than output at some part of the line cycle, and higher at other time intervals. This leads to condition of blocking voltages of both polarities, as well as conduction currents in both directions, so four quadrant switches are necessary.

Clearly, topologies with step-up characteristic in Fig. 6.25 and Fig. 6.26 are completely suitable for PFC because they can provide $Vout>Vg$ for input of any polarity. Topologies with characteristic in Fig. 6.27 and Fig. 6.28 could be used to get $Vout<Vg$; however, distortion will occur at the area of line circle when input voltage drops below output voltage value. Similar effects occur when topologies like buck are used for off-line applications.

In the next chapter suitable topology for power factor correction will be chosen, analyzed in detail and experimentally achieved results will be shown to confirm the theory and analysis.

Chapter 7

New Power Factor Corrector without Input Rectification

The choice will be made for the experimental PFC realizing new approach of power factor correction. Topology will be analyzed analytically and basic equations will be used to compare predictions with experimental data. Novel control scheme will be discussed in detail and experimental waveforms will be presented. Detailed calculations of fundamental losses will be evaluated and compared with measurements.

7.1 Analytic Analysis of the Chosen Topology

The topology in Fig. 6.25 was chosen for PFC implementation because of the following considerations:

1) Step-up gain characteristic: usual and convenient for PFC, no distortion in input current.
2) *L1* and *L2* have continuous currents and they don't exchange energy during converter operation: there is no problem with leakage inductance associated with voltage overshoot and losses.
3) *L1* and *L2* are in different branches but share the same current waveforms. This fact leads to opportunity to integrate *L1* and *L2* to one magnetic structure, which is an important technological benefit.
4) Only two switches of simple construction (MOSFETs) in the whole converter.
5) Continuous waveform of the input current: ideal for filtering and input PFC characteristics.

The drawbacks of this topology can be outlined as:

1) Switches conduct currents from both inductors same time, so current rating of MOSFETs is somewhat high and extra losses can be expected.
2) Switches have to be rated at least for *2Vout*, which is a clear price issue in terms of the MOSFETs. High voltage across the MOSFET turning on also means increased dynamic losses.

Basic derivation of ideal gain characteristic of the topology in Fig. 6.25 was conducted in chapter 6. To have more realistic understanding of this topology operation, parasitic elements are introduced in Fig. 7.1.

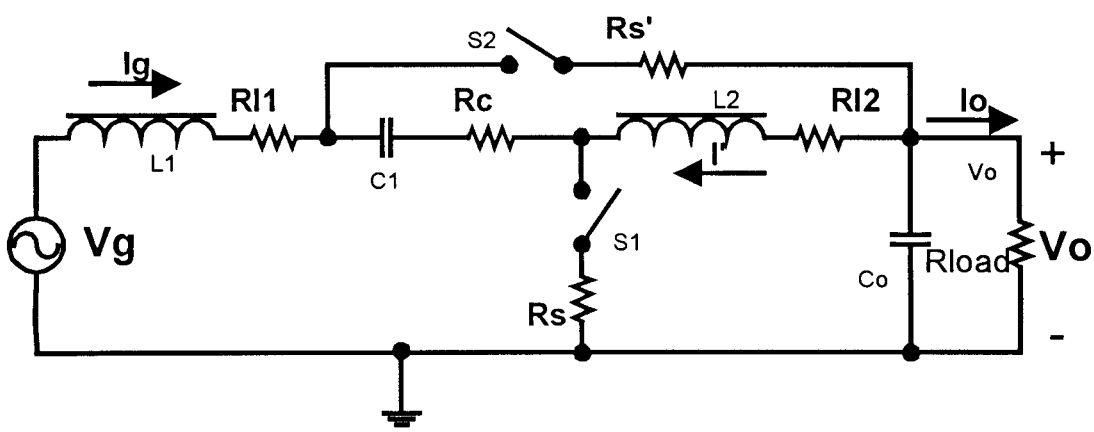

Figure 7.1: Power stage with parasitic elements

The following notations are used for new elements: *Rl1* is a series resistance of the inductor *L1* and the similar parasitic resistance of the filter inductance (not shown) is included for better accuracy. *Rl2* is a series resistance of the inductor *L2*. *Rc* is *ESR* (equivalent series resistance) of switching cap *C1* in Fig. 7.1. *Rs* and *Rs'* are on switch

resistances, since same MOSFETs are used and we assume about the same temperature on the switches: $Rs=Rs'$.

Notice that equations (6.4.1) and (6.4.2) are not valid anymore because of voltage drops on parasitic resistances. Equation (6.4.3) is still valid though, because no new paths for the current were created.

Equation (6.4.3) is then simplified to $IgD - I'D' = 0$ (6.4.4). Using $IgD' - I'D = Io$ (6.4.5) it can be also noticed that: input and output currents of the power stage are still related (7.1.1) via ideal voltage gain formula (6.4.6); although the real voltage gain does not satisfy that equation anymore.

$$\frac{Io}{Ig} = \frac{1-2D}{1-D} = \frac{1}{M(D)} \tag{7.1.1}$$

where M(D) is an ideal voltage gain $M(D)=(1-D)/1-2D)$ (6.4.6)

The efficiency of power stage is introduced in (7.1.2) and farther expressed using (7.1.1), where $M_R(D)$ is real voltage gain of the power stage with parasitic elements. Finding efficiency will then provide the equation for the real voltage gain.

$$\eta = \frac{Pout}{Pout + Ploss} = \frac{Pout}{Pin} = \frac{VoIo}{V_g I_g} = \frac{M_R(D)}{M(D)} \tag{7.1.2}$$

Only *Ploss* is needed to calculate the efficiency in (7.1.2). Losses in particular parasitic element *Ri* can be expressed as a product of parasitic resistance and square of rms current through it, (7.1.3)

$$P_i = Irms_i^2 R_i \tag{7.1.3}$$

According to (2.14), the following expression is valid for the value of the losses in *Ri* element, (7.1.4):

$$P_i = \frac{R_i}{T}\int_0^T i_i^{\,2}(t)dt \qquad (7.1.4)$$

Values of *Ri* are given parameters, so only $Irms_i$ have to be determined by the analysis of the circuit.

Rms current in *Rl1* (Fig. 7.1) is clearly *Ig*, so losses in this component are easy to find by inspection.

$$P_{L1} = (Ig)^2 Rl1 \qquad (7.1.5)$$

Ic, current in *Rc*, is illustrated in Fig. 7.2. Assuming small ripple, the current during *DTs* time interval can be approximated as *Ig*, and the current during *D'Ts* time interval can be approximated as *I'* (Fig. 7.1).

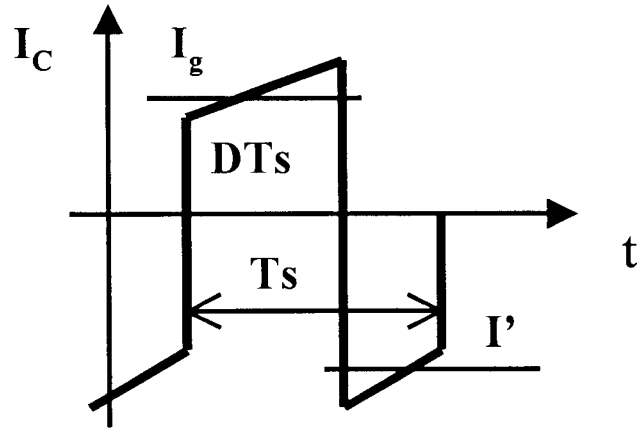

Figure 7.2: Current waveform Ic

Then (7.1.4) yields (7.1.6) for losses in *Rc*.

$$P_C = (Ig^2 D + (I')^2(1-D))R_C \qquad (7.1.6)$$

Switches *S1* and *S2* both conduct currents *Ig* and *I'* when they are on, at *DTs* and *D'Ts* time intervals respectively. Equations (7.1.7) and (7.1.8) then represent losses in *S1* and S2 respectively.

$$P_{S1} = (Ig + I')^2 DR_{S1} \tag{7.1.7}$$

$$P_{S2} = (Ig + I')^2 (1 - D) R_{S2} \tag{7.1.8}$$

Finally, in assumed abbreviations, the current in *Rl2* is clearly *I'*, Fig.7.1, so the copper losses in second inductor can be simply expressed as (7.1.9)

$$P_{S1} = (I')^2 Rl2 \tag{7.1.9}$$

Equation (7.1.10) represents total considered (so-called DC) losses in the power stage and does not include switching losses, dynamic losses, core losses, etc.

$$\begin{aligned} Ploss = Ig^2 Rl1 + \left(Ig^2 D + (I')^2 (1 - D)\right) Rc + \left((Ig + I')^2 D\right) Rs + \\ + \left((Ig + I')^2 (1 - D)\right) Rs' + (I')^2 Rl2 \end{aligned} \tag{7.1.10}$$

These losses can be further expressed via I_0 and therefore: V_0 and *Rload* (7.1.11)

$$Ploss = \left(\frac{Vo}{(1 - 2D) Rload} \right)^2 ((1 - D)^2 Rl1 + + D(1 - D) Rc + DRs + (1 - D) Rs' + D^2 Rl) \tag{7.1.11}$$

Finally, efficiency η can be expressed as (7.1.12) (*Pload* is the power dissipated in the load and is equal $Vo^2/Rload$)

$$\eta = \frac{Pload}{Pload + Ploss} = \frac{1}{1 + \frac{Ploss}{Vo^2} Rload} = \frac{1}{1 + \beta(D)} \tag{7.1.12}$$

where term $\beta(D)$ is expressed as (7.1.13)

$$\beta(D) = \frac{(1 - D)^2 Rl1 + D(1 - D) Rc + DRs + (1 - D) Rs' + D^2 Rl2}{(1 - 2D)^2 Rload} \tag{7.1.13}$$

Notice that efficiency is always lower than 100%. The critical point is when D=0.5 because equation predicts 0% efficiency at that point. Also notice that every single parasitic element separately would cause this effect.

The following parameters were used for calculations: $Rl1$=$Rl2$=0.1 Ohm; R_S=R_S=0.6 Ohm, Rc=0.1 Ohm. Breadboard also included sense resistor and input filter, so respectively 0.25 Ohm and 0.2 Ohm were added to $Rl1$ to improve the prediction. 80 W output power was assumed, Vg=115 V, Vo=200 V. The 200 V value of output voltage was chosen to be able to step down in input voltage and have data to analyze in a range of low input voltages. This calculation includes only DC losses, but it allows derivation of the analytic expressions for efficiency and voltage gain as the functions of duty ratio D. Analytical expressions in a compact form are very illustrative to describe the general behavior of the power stage. Efficiency prediction is shown in Fig. 7.3.

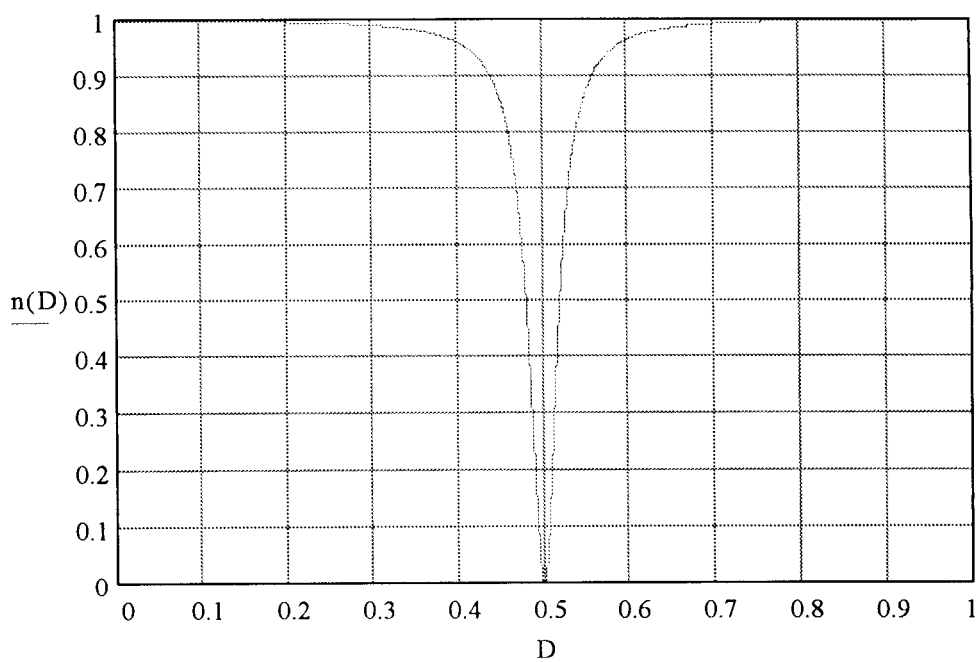

Figure 7.3: Efficiency prediction from the (7.1.3) as a function of D

As expected, efficiency decreases around point D=0.5, which corresponds to infinite ideal voltage gain, which is never reached practically as it will be shown shortly. It is seen from equation (7.1.12) that any parasitic element would make efficiency less than

100% in general and provide 0% value of efficiency at D=0.5 point. Looking at (7.1.13), it can be concluded that higher value of *Rload* would provide lower relative losses, in other words: to achive high efficiency – the values of parasitic elements should be values much less than load resistance *Rload*. Notice that at D=0.5 efficiency would still be zero, no matter how small the values of parasitic elements might be.

Now it is possible to predict real voltage gain $M_R(D)$ using equation (7.1.2):

$$Mpr(D) = M(D)\eta(D) \tag{7.1.14}$$

Fig. 7.4 shows the predicted value of the voltage gain *Mpr(D)*. Notice that voltage gain is limited and even crosses zero value at D=0.5 – the point where ideal gain would reach infinity.

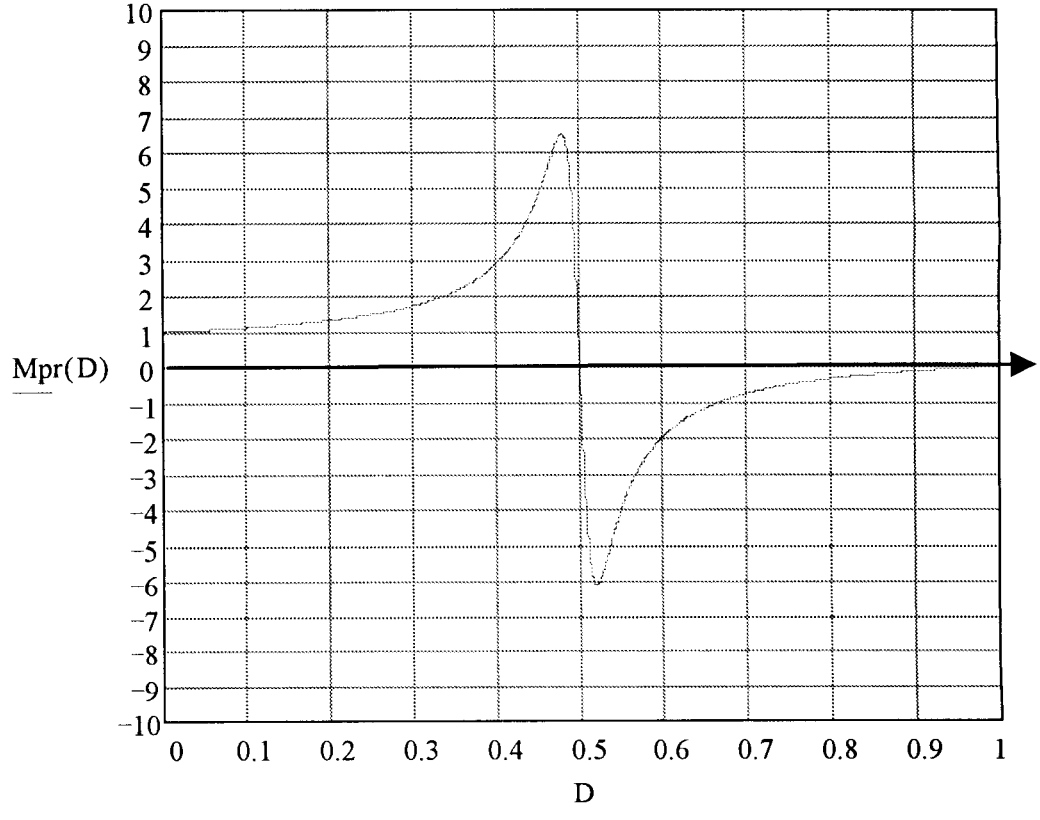

Figure 7.4: Predicted voltage gain Mpr(D) from (7.1.14)

As it was established, the reason is that at that region converter has poor efficiency and losses in parasitic elements limit the maximum voltage gain that could be reached. Analytic expressions (7.1.12) and (7.1.13) give a clear picture about effect of losses and values of parasitics. Not all losses were included in this derivation though, so some discrepancy is expected.

Now predictions can be compared with experimental data. Fig. 7.5 shows measured voltage gain *Mexp*, the ideal voltage gain *M(D)* (from equation (6.4.6)), and predicted voltage gain *Mpr(D)* (from equation (7.1.14)).

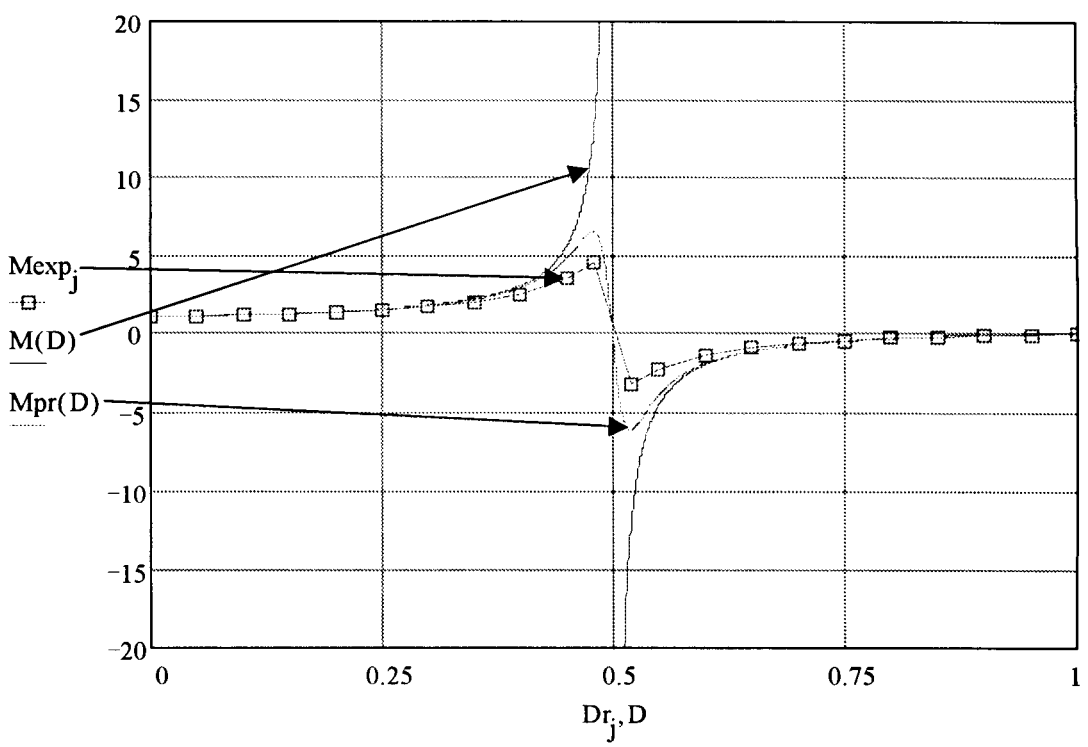

Fig. 7.4: Measured gain Mexp(D), ideal gain M(D) and predicted gain Mpr(D)

As it was mentioned: any one parasitic element would bring efficiency value to 0% at D=0.5, so looking at (7.1.14) it can be expected that real voltage gain will not blow up to infinity at that point. *Mpr(D)* in Fig. 7.5 shows expected behavior. Experimental data (*Mexp* in Fig.7.5) shows good agreement with prediction.

Some difference between predicted gain *Mpr(D)* and measured gain *Mexp(D)* in area around D=0.5 can be explained by the fact that only DC losses were used for prediction. Core losses, switching losses and dynamic losses should be also considered for more accurate calculations.

7.2 Control Scheme and Practical Implementation

The control circuit had to be designed for the power stage to implement the power factor correction. Notice that usual feedback as "low output voltage causes duty ratio to increase" would not work in this case, because of bipolar gain characteristic of the power stage. Usual conventional control integrated circuits are therefore not suitable for this application, at least without modifications. Hysteresis current control was implemented with discrete components. The main control idea is shown in Fig. 7.6, and corresponding control signals are illustrated in Fig. 7.7.

The circuit operates as following. Two frame signals for the input current are generated: *Vin-UP* and *Vin-DN*. These signals are proportional to input waveform *Vg* to achieve high power factor value at the input of the converter. Input current is sensed using the resistor *Rsense* and generated voltage is compared with two frame signals. Notice that switching *S1* in Fig. 7.6 on and *S2* off will provide positive slope of the input current for any polarity of input voltage. Negative slope of input current occurs when *S1*

is off and *S2* is on: during *D'Ts* time interval. So as soon as voltage proportional to input current reaches lower frame *Vin-DN*, the flip-flop triggers into *D* state, and when upper frame *Vin-UP* is reached, the flip flop triggers into *D'* state, Fig.7.7.

This control method makes average input current to be proportional to input voltage even during one switching circle. Therefore, it provides unity power factor.

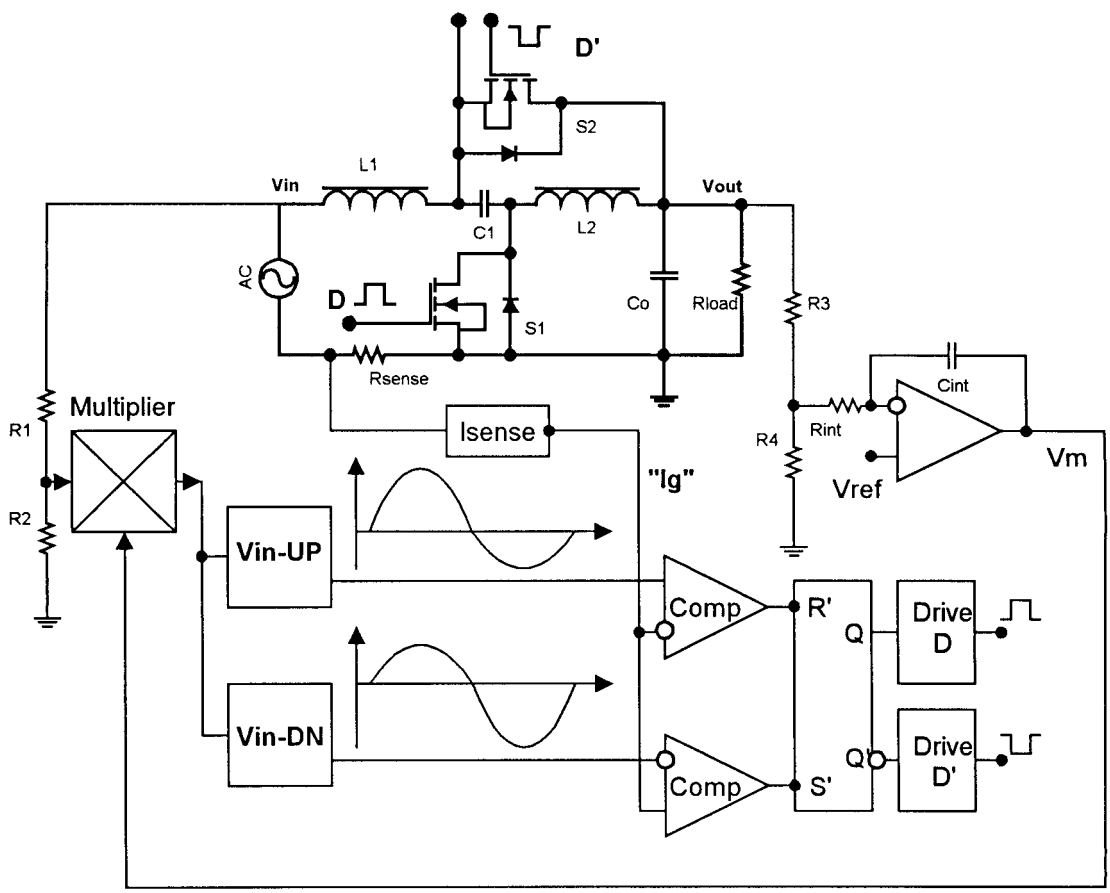

Figure 7.6: General control schematic for PFC

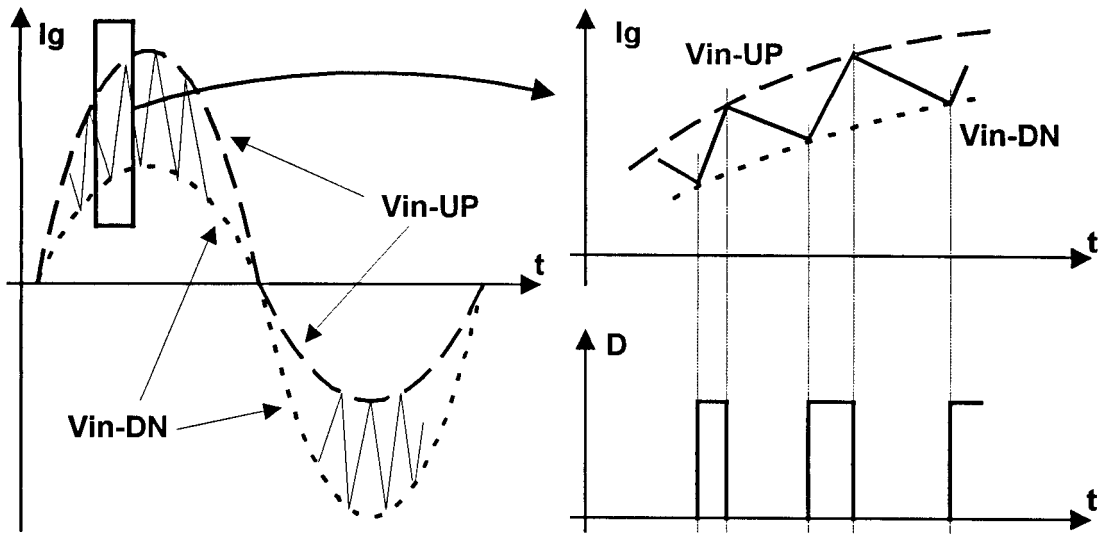

Figure 7.7: Main control waveforms for the circuit in Fig.7.6

This control method has a disadvantage, however, of being noise sensitive. The actual current waveform is used for control, so noise from power stage can easily cause false triggering of the comparators, and circuit can become unstable. Circuitry generating blanking pulses was introduced to avoid this problem, Fig. 7.8. The illustrating waveforms are shown in Fig. 7.9 and Fig. 7.10.

This part of the circuit provides regulated noise immunity and work as following: when input current waveform reaches one of the current frame signals and switching from one state to another occurs: the opposite current frame is shifted away from the current signal for the short period of time. Possible noise spike will not therefore reach it and cause false triggering. Notice the noise spike on the current waveform in Fig. 7.10. Damping network *Cd-Rd* was also included to damp parasitic resonance effects in power stage.

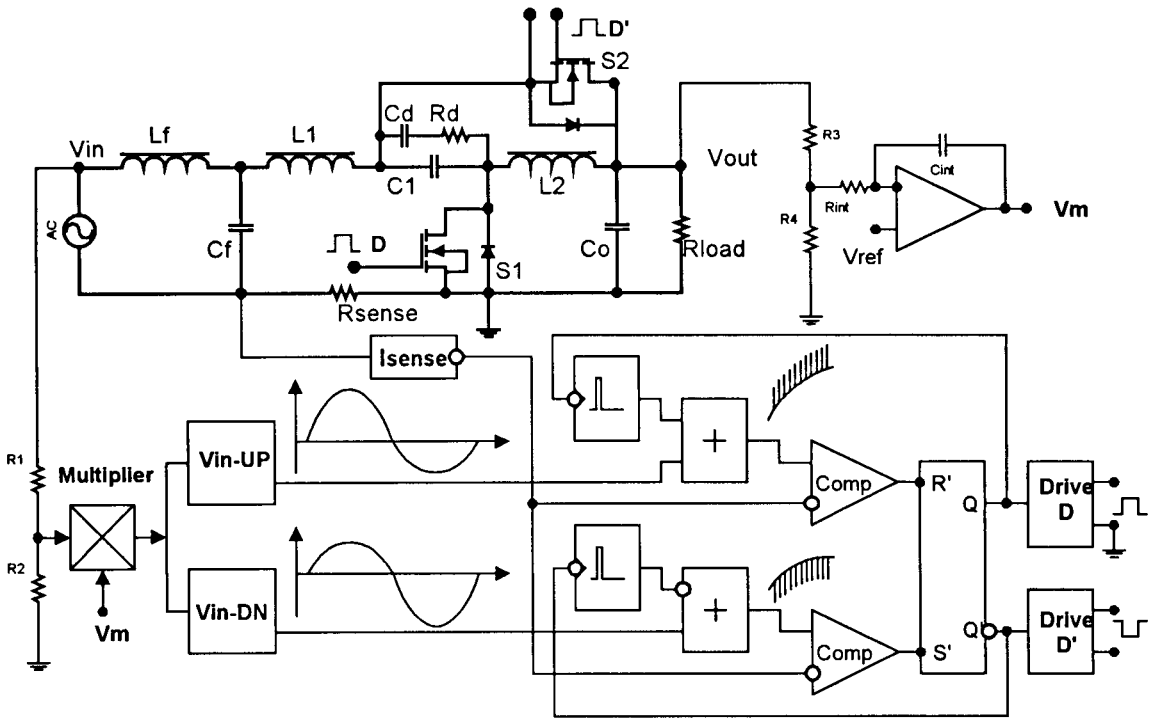

Figure 7.8: Detailed schematic of the PFC

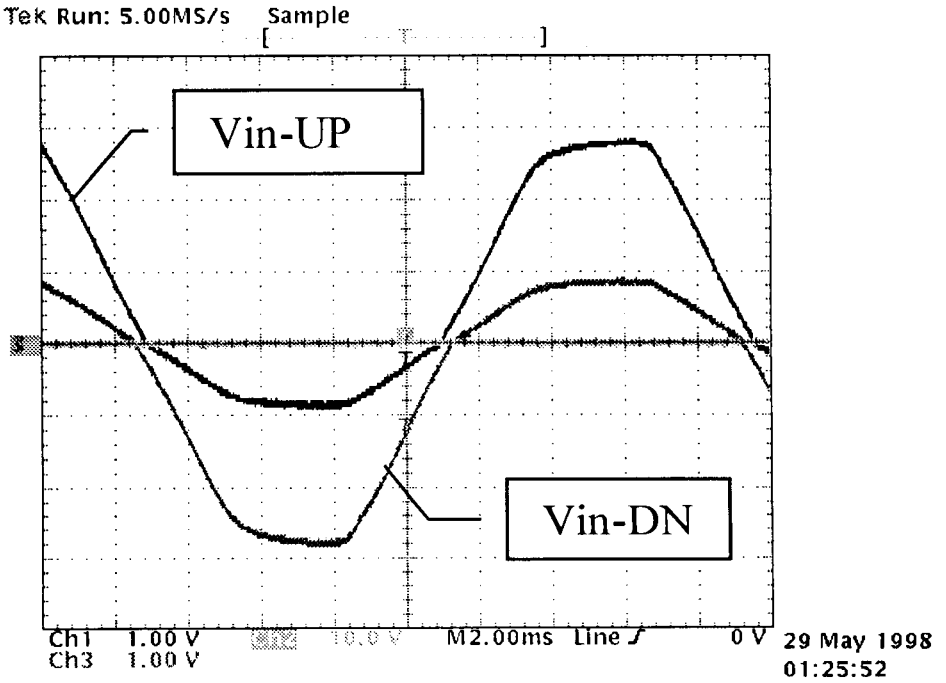

Figure 7.9: Current frame signals Vin-UP and Vin-DN

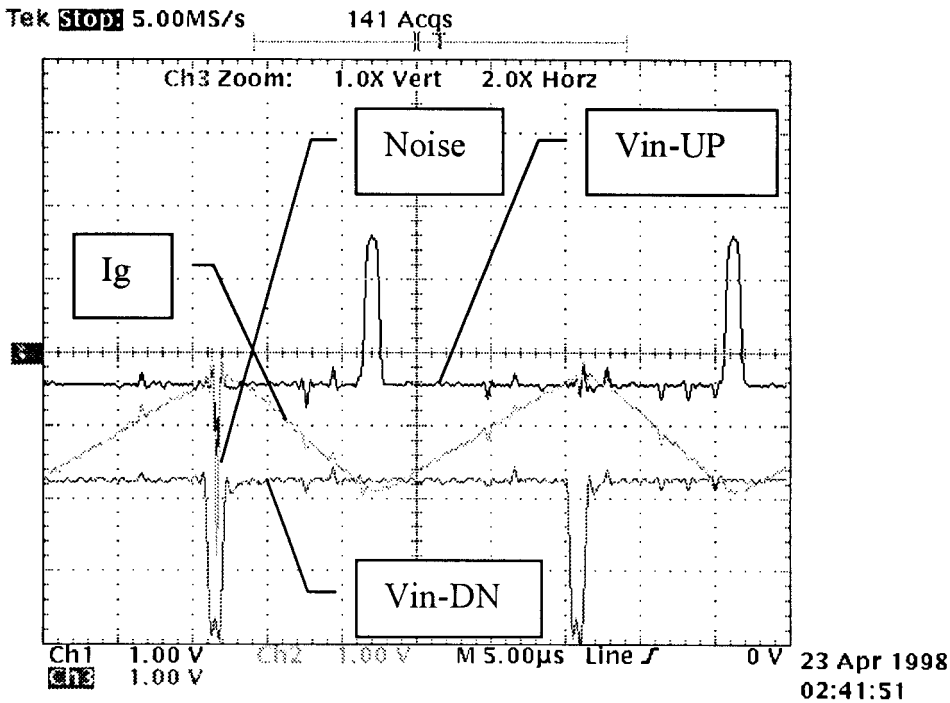

Figure 7.10: Vin-UP and Vin-DN with blanking pulses

Prototype was assembled with the following components of the power stage (Fig. 7.8): $L1$=$L2$=0.5mH, Lf=2mH, Cf=1µF, $C1$=4µF, Cd=5µF, Rd=20Ω, Co=680µF.

The input waveforms of the circuit are shown in Fig. 7.11 and correspond to 85 Vrms input voltage, 200V DC output with 1% output ripple, 80W output power, 86.7% efficiency.

Power factor achieved higher than 0.998 value, even though input voltage was not ideal sin wave, Fig. 7.11. Circuit proved the concept of using topologies with bipolar gain for power factor correction without input rectification.

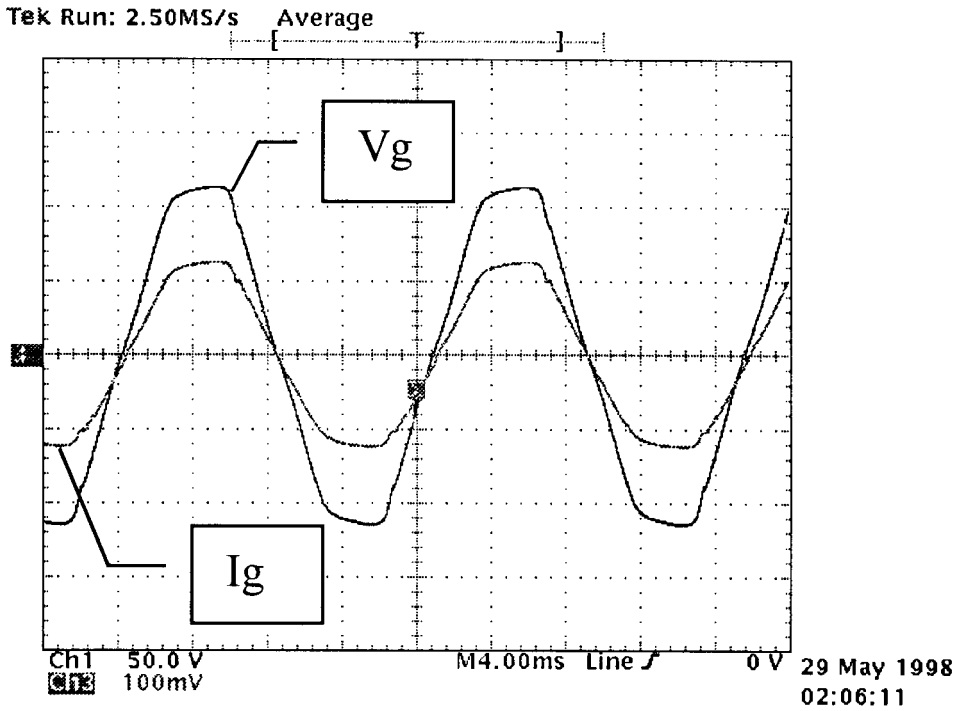

Figure 7.11: Input voltage Vg and current Ig waveforms of PFC 85 Vrms input voltage, 200V DC output with 1% output ripple, 80W output power, 86.7% efficiency

The power stage has a bipolar gain characteristic with singularity at D=0.5 point. The shape of input current is forced to follow input voltage waveform and can get out of limits only because of the noise problem or control failure. However, it would be illustrative to plot actual change of duty ratio during the complete line cycle and therefore judge the behavior of the circuit according to the $M(D)$ characteristic. As it was also shown, the D=0.5 point is associated with degradation of efficiency so it is important to check if power stage operates at this point at some moments.

The following data in Fig. 7.12-7.14 is illustrating the behavior of the power stage during the change of input voltage along complete 60 Hz line cycle.

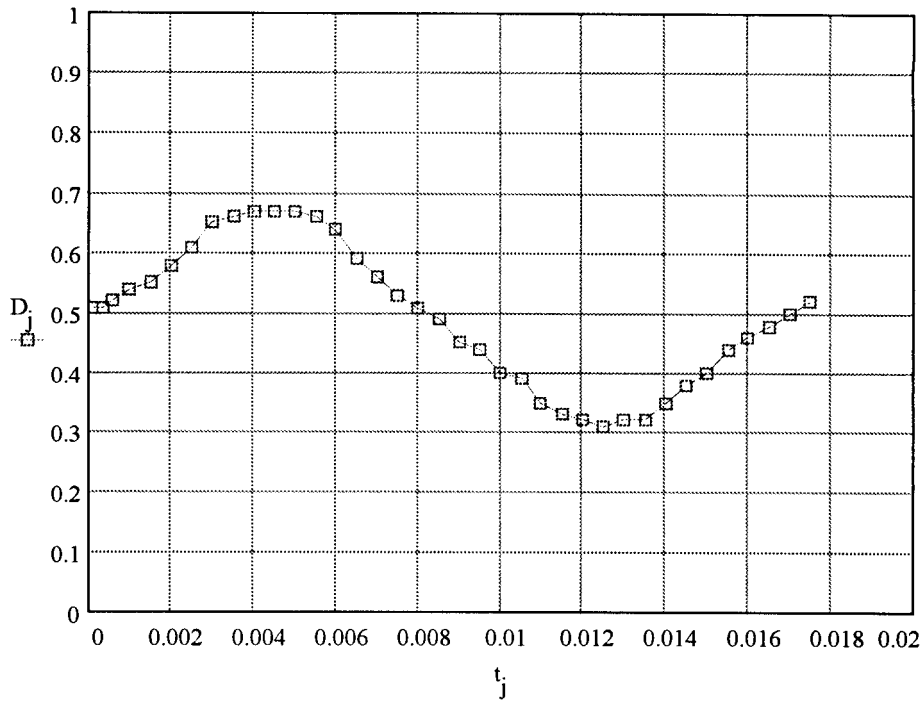

Figure 7.12: Experiment values of the duty ratio D during a line cycle

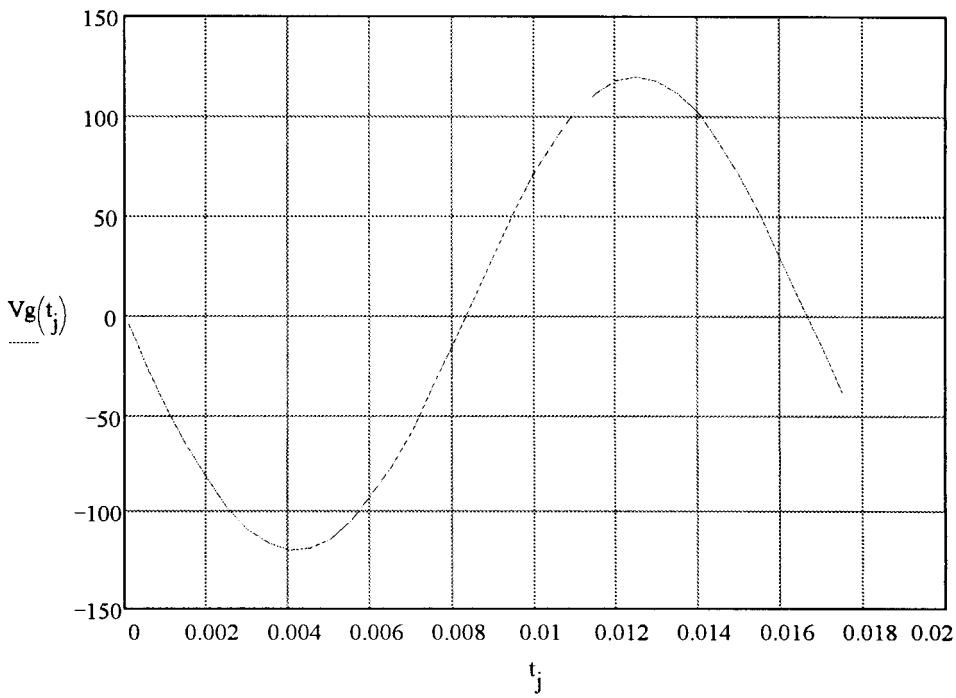

Figure 7.13: Sketch of input voltage waveform corresponding to Fig.7.12

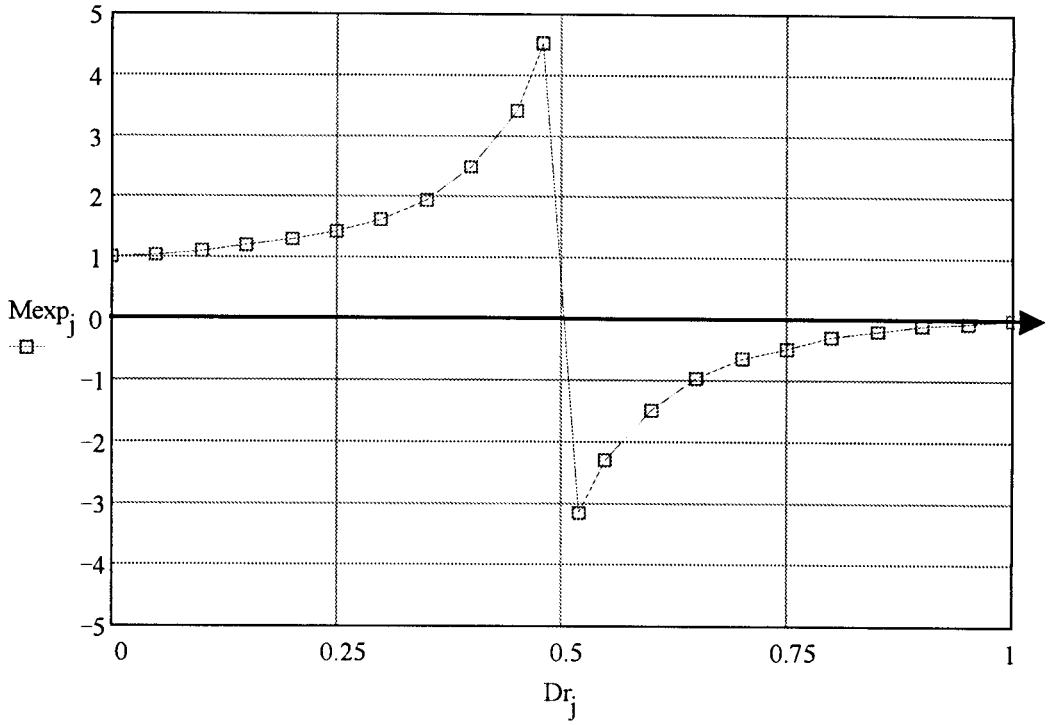

Figure 7.14: Experimental values of the power stage gain Mexp(D)

Fig. 7.12 shows experimental values of the duty ratio D during the one line cycle, and Fig. 7.13 shows corresponding input voltage waveform. Bipolar gain characteristics were shown in Fig. 7.4, and experimental values of the power stage gain are shown in detail in Fig. 7.14. According to Fig. 7.12, the value of duty ratio crosses the D=0.5 point; however, it happens when input voltage is at zero value and therefore it does not cause the overload of the circuit or critical degradation of the efficiency. Notice that duty ratio changes in the region D>0.5 when input voltage is negative and in the region D<0.5 when input voltage is positive, Fig. 7.12 and Fig. 7.13. It corresponds to Fig. 7.14, since negative gain of the power stage is expected at Vg<0 time period and positive gain is needed respectively at Vg>0 time period.

7.3 Experimental Verification and Data

Understanding of the key factors that influence efficiency, especially at low input voltage, is particularly important. MATHCAD file was created to predict efficiency characteristic. Calculations were based on assumption that voltages on the capacitors are constants ("big" values of the caps). The usual way of calculating efficiency is to find rms values of voltages and currents for the half of the line circle. Since this circuit utilizes non rectified AC and behaves differently at positive and negative halves of the line circle: calculations were done separately for these halves of the period. Overall efficiency is clearly the average of efficiencies during positive and negative half periods.

The following parameters were used in calculations and then used in taking experimental data: out voltage Vo=200V, switching frequency Fs=50KHz, load resistance $Rload$=500Ohm. The values of parasitic elements are based on measurements and data sheets, and will be introduced step by step with related loss calculations.

Many of accounted losses I^2R depend on value and waveform of the current, which goes through the element. Therefore, the estimate of the duty ratio is needed to derive necessary value.

Fig. 7.15 shows the value of steady state duty ratio D, (7.3.1), derived from equation of ideal gain $M(D)$, (6.4.6). Input voltage Vg changes polarity, so two branches are shown in Fig. 7.15.

$$D = \frac{Vg - Vo}{Vg - 2Vo} \tag{7.3.1}$$

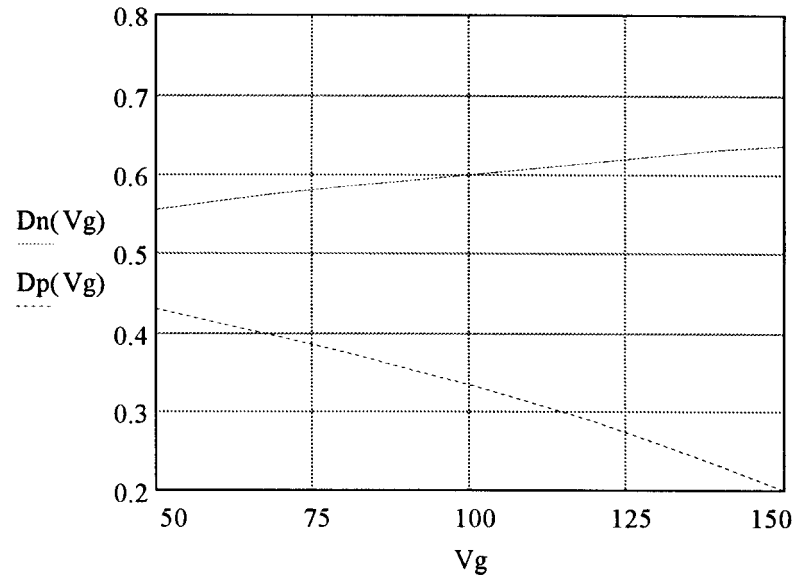

Figure 7.15: Steady state value of D for negative Dn and positive Dp halves of the line cycle

Of course, practical duty ratio would differ from the one derived with assumption that gain is ideal and no losses are present in the power stage. However, the difference between ideal and real values of duty ratio is not substantial.

As expected, steady state duty ratio has values less than 0.5 for positive half wave of input voltage, and values above 0.5 for the negative part.

DC losses were already analyzed in simplified calculation (7.1.12), (7.1.13). The rms currents will be different during positive and negative parts of the circle, but general calculation does not change. Losses in parasitic *ESRs* of input filter and output capacitors were added in similar way. All losses in parasitic resistances are calculated as I^2R.

Losses are calculated to account for many effects; some losses are added together to illustrate total losses in particular elements. For example, switching losses, DC losses in on resistance of the MOSFET and dynamic losses would give an estimate of total losses

in the active switch.

First, the losses in input filter *Pf* are calculated, (7.3.2). *Plf* represents loss in parasitic resistance of filter inductor, *Pfc* is associated with loss in *ESR* of the filter capacitor; see schematic in Fig. 7.8.

$$Pf = Plf + Pcf \tag{7.3.2}$$

Notice that input current is the same for positive and negative halves of the 60Hz line cycle. Therefore, filter losses in inductor are the same as well. The losses in ESR of the capacitor are different though because switching frequency depends on the sign of input voltage. Values 0.2 Ohm and 0.1 Ohm were used for resistance of the filter inductor and *ESR* of the filter capacitor respectively. Fig. 7.16 shows related losses. Fig. 7.17 illustrates total input filter losses (7.3.2).

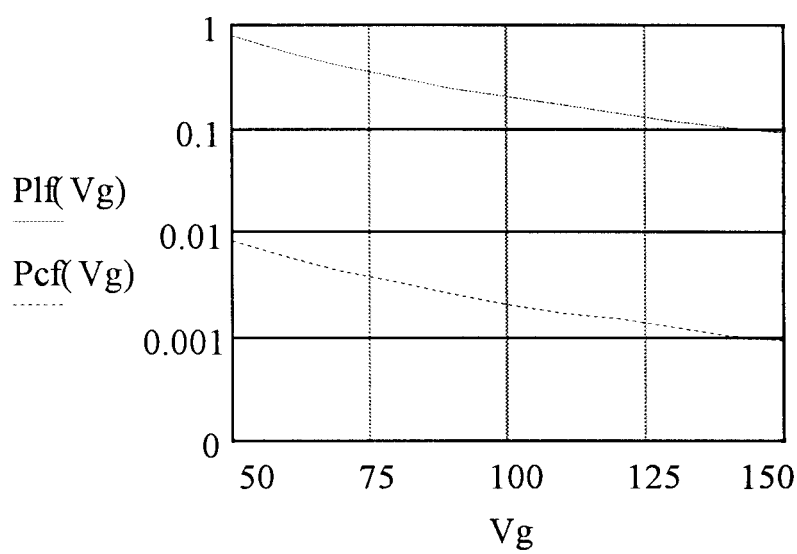

Figure 7.16: Losses in filter inductor Plf(Vg) and filter capacitor Pcf(Vg)

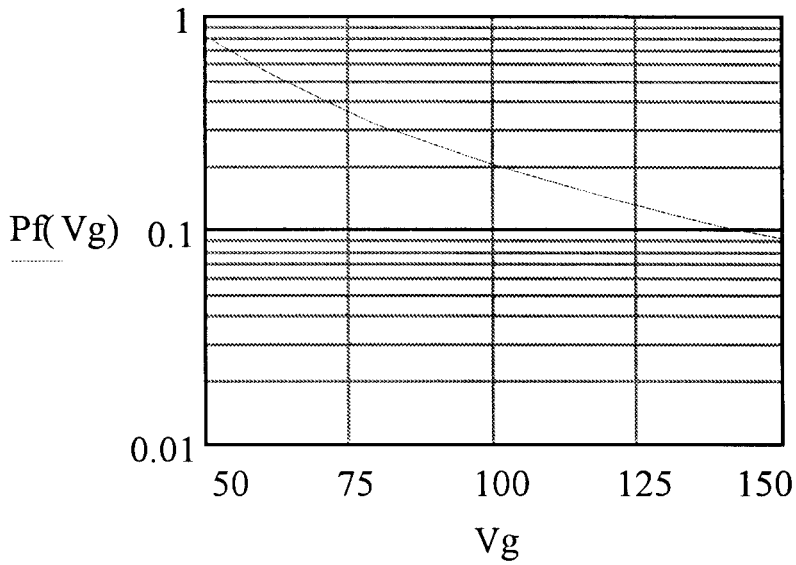

Figure 7.17: Total input filter losses Pf(Vg)

Current in inductor *L1* corresponds to input current of topology and has similar waveform for both halves of the line cycle. Therefore, losses in parasitic resistance of the inductor are the same, see Fig. 7.18.

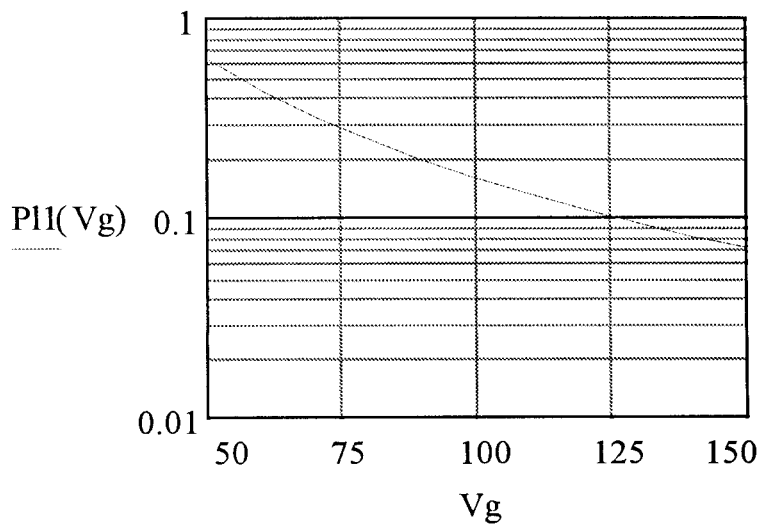

Figure 7.18: Losses in inductor L1 Pl1(Vg)

Current waveform changes significantly in *L2*, depending on the polarity of input voltage; losses in parasitic resistance of *L2* are plotted in Fig. 7.19.

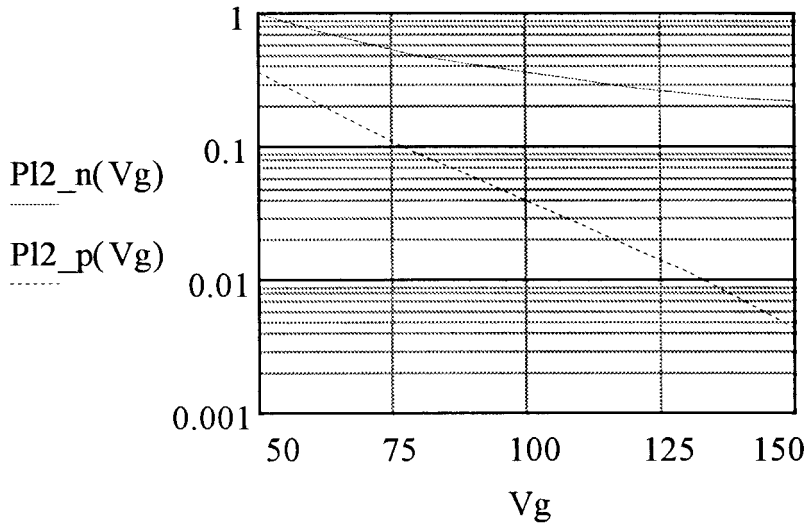

Figure 7.19: Losses in L2 for negative Pl2_n and positive Pl2_p halves of the line circle

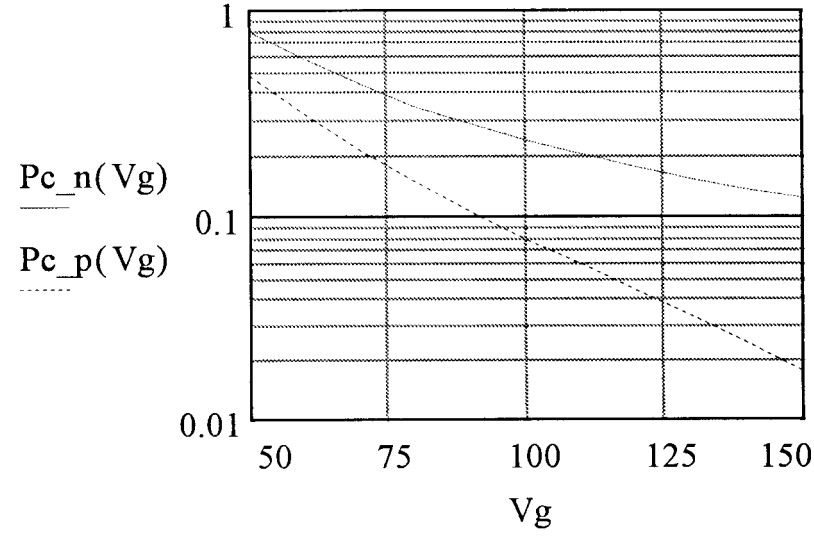

Figure 7.20: Losses in C1 for negative Pc_n and positive Pc_p halves of the line circle

Switching capacitor *C1* in Fig. 7.7 was approximated to have *ESR* of 0.1 Ohm. Associated losses are shown in Fig. 7.20, for positive and negative halves of the 60Hz line cycle.

Irms of the switches are different for positive and negative halves of the line circle. Calculations show that negative half of the circle introduces higher current stress on both switches Fig. 7.21 and Fig. 7.22. It was expected because of non-symmetrical gain characteristic of the power stage, Fig. 7.4.

Fig. 7.21 represents DC losses in *S* switch in Fig. 7.7, for the negative and positive half periods. Fig. 7.22 represents the same DC losses for the switch *S'* in Fig. 7.7. It is clearly seen that lower input voltage causes higher rms currents and therefore higher DC losses. Similar considerations are correct for DC losses in parasitic resistances of inductors *L1* and *L2*.

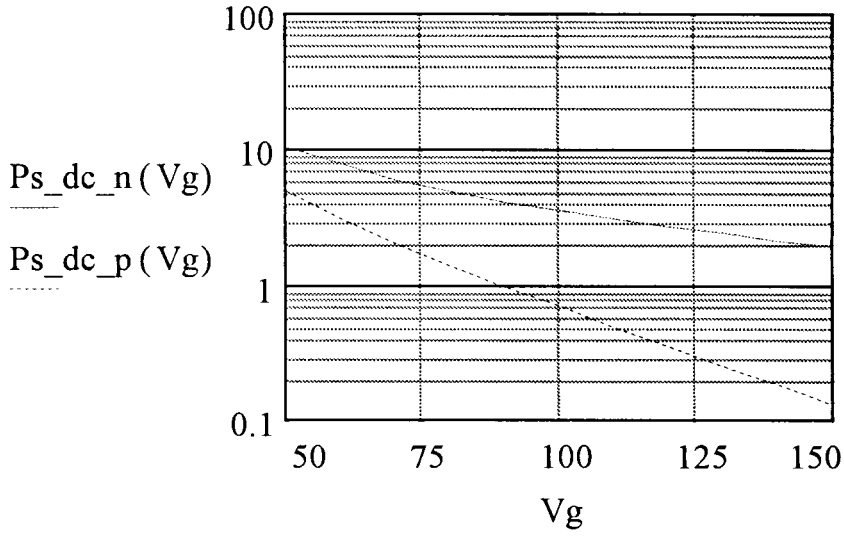

Figure 7.21: DC losses in the switch S: negative and positive halves of the line circle

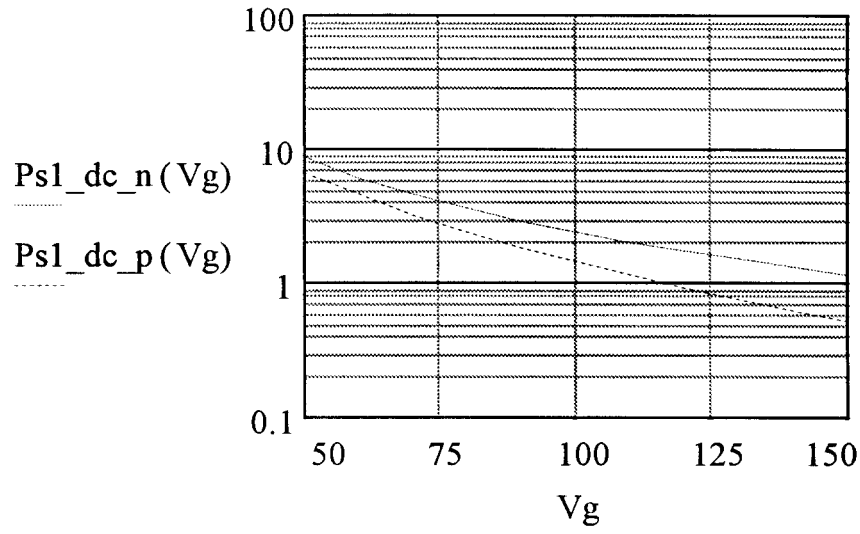

Figure 7.22: DC losses in switch S': negative and positive halves of the line circle

Dynamic losses will now be considered: both switches have a voltage of *2Vout* when they are not conducting. So the parasitic capacitance is discharged from that voltage every time when switch turns on, with total losses in each separate switch shown in (7.3.3), where *Cs* is a parasitic capacitance across the switch (0.6nF value was used), and *Fs* is a switching frequency.

$$Pdynamic = (2Vout)^2 \frac{Cs}{2} Fs \qquad (7.3.3)$$

Switching frequency *Fs* is not constant in a case of implemented control. Practically, the average switching frequency is about 55 KHz, ranging down to 40 KHz and up to 70 KHz at positive and negative halves of the line period respectively. This effect is associated with the fact that voltages applied to inductances are different in these cases, which leads to different slopes of the inductor currents. The latter leads to different on and off times of the switches and therefore change of switching frequency.

Switching waveforms were assumed as a worst case for switching losses, as shown in Fig. 7.23. Equation (7.3.4) shows the resulting formula for switching losses.

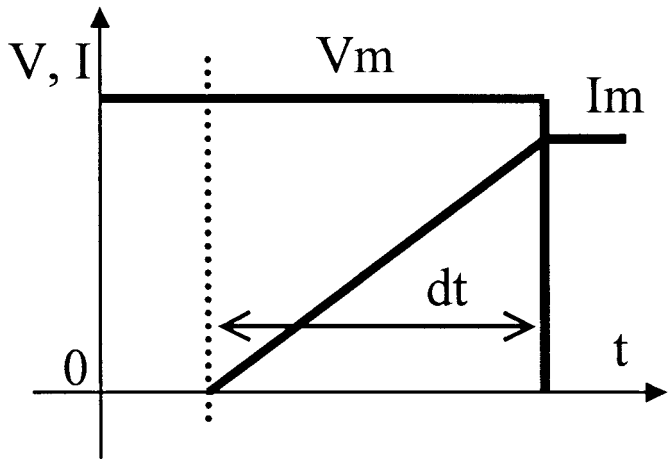

Figure 7.23: Assumed switch current and voltage waveforms.

The peak current *Im* in Fig. 7.20 and (7.3.4) is a current through the switch at *DTs* time interval, found as *Irms/D*. *Vm* is *2Vout*. The steady state value *Do* will be used for substituting to *D*, different at positive and negative parts of the switching cycle.

$$Pswitching = Vm\frac{\mathrm{Im}}{2}dt \cdot Fs = Vout \cdot \frac{Irms}{Do} \cdot dt \cdot Fs \qquad (7.3.4)$$

Switching losses for the switches S and S' are presented in Fig. 7.24 and Fig. 7.25 respectively.

As before, rms currents increase when input voltage becomes negative, also: the switching frequency increases. Both of these effects cause switching losses to increase at the negative half of the line circle.

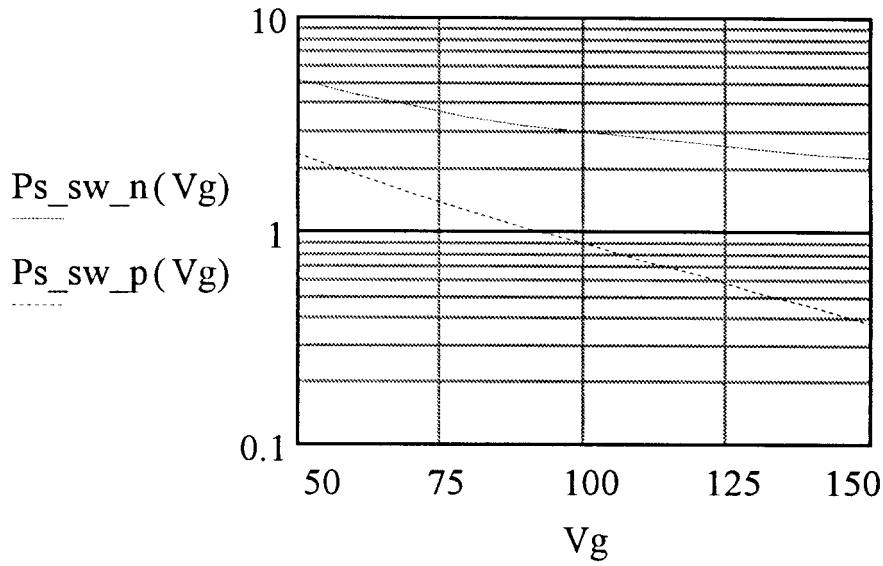

Figure 7.24: Switching losses for the switch S, negative and positive halves of the line cycle

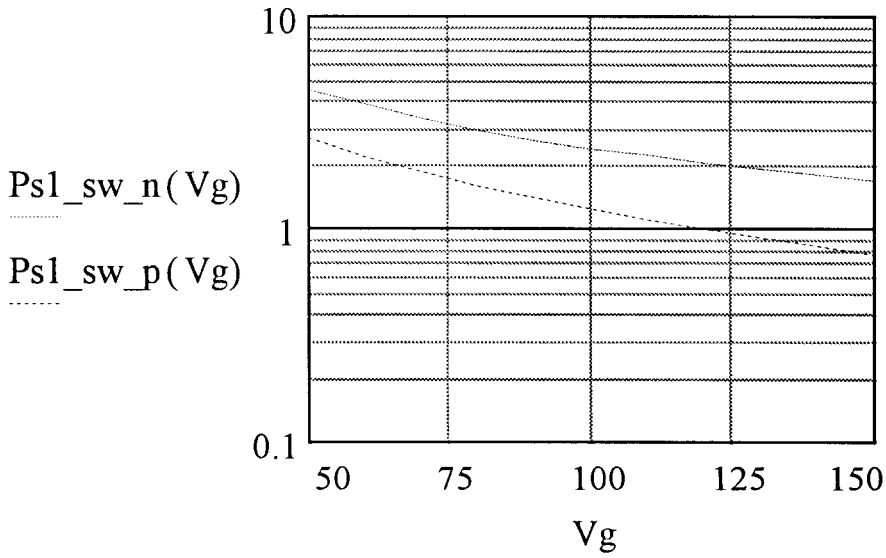

Figure 7.25. Switching losses for the switch S', negative and positive halves of the line circle

There is a particular interest to see total switch losses, expressed as a sum of DC losses *Ps_dc*, switching losses *Ps_sw* and dynamic losses *Pdynamic*, (7.3.5)

$$Ps = Ps\_dc + Ps\_sw + Pdynamic \tag{7.3.5}$$

Fig. 7.26 and Fig. 7.27 show total losses in the switch *S* and *S'* respectively for negative and positive parts of the line circle.

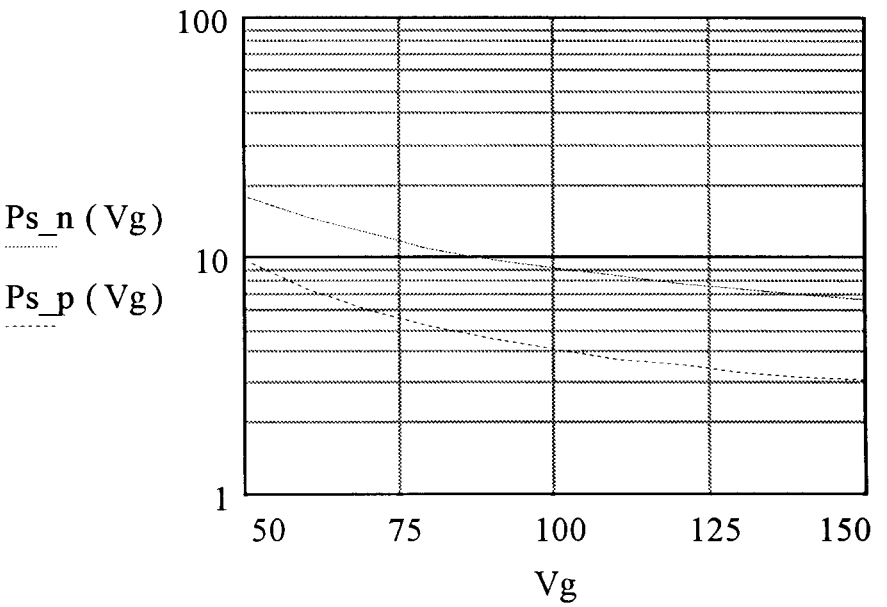

Figure 7.26: Total losses in the switch S for negative and positive parts of the line circle

Ripple currents in the *C1*, see Fig. 7.7, and output capacitor *Co* also increase at negative input voltage, and it affects power losses. The calculated power losses in the *C1* and output capacitor are presented in Fig. 7.28 and Fig. 7.29 respectively.

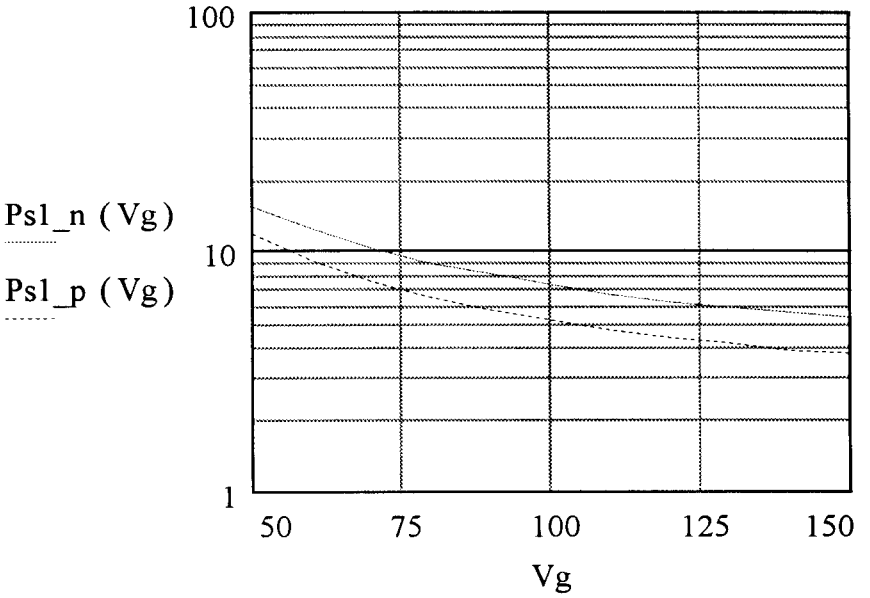

Figure 7.27: Total losses in the switch S' for negative and positive parts of the line circle

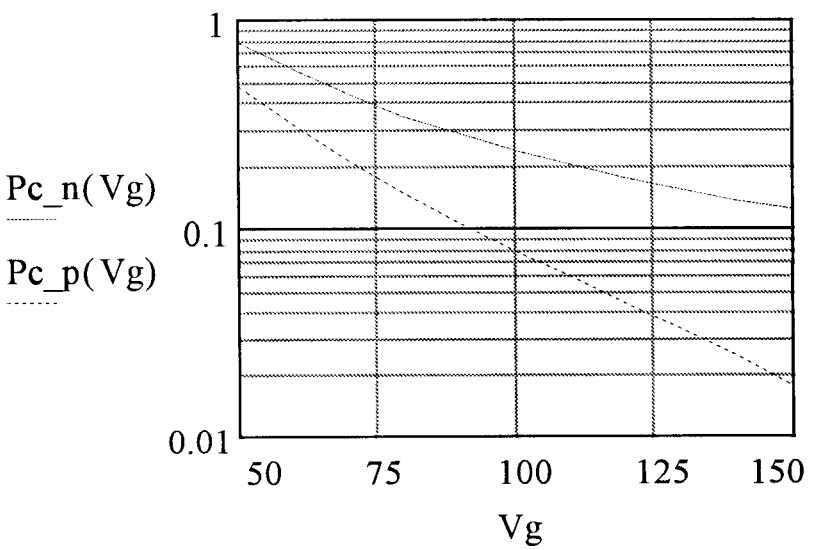

Figure 7.28: Losses in ESR of the C1 capacitor as a function of input voltage for negative and positive parts of the line circle

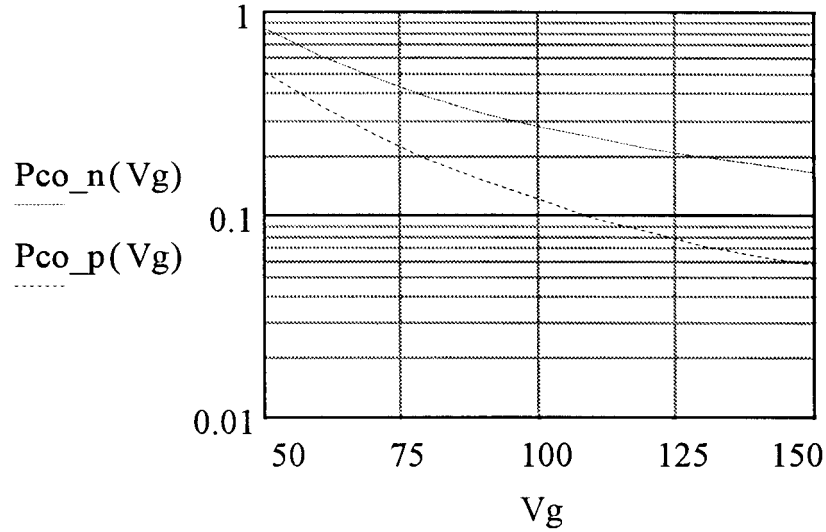

Figure 7.29: Losses in ESR of the output capacitor Co for negative and positive parts of the line circle

Finally, the total losses are found as a sum of filter losses *Pf*, DC losses in inductor parasitics *Pl1* and *Pl2*, losses in switches *S* and *S'* - *Ps* and *Ps'* respectively, and losses in switching capacitor, *Pc*, and output capacitor *Pco*. All losses are found separately for positive and negative halves of the line circle (7.3.6).

$$Plosses = Pf + PL1 + PL2 + Ps + Ps' + Pc + Pco \qquad (7.3.6)$$

Efficiency is then calculated using equation (7.3.7): for both positive and negative line half periods, and plotted in Fig. 7.30.

$$\eta(Vg) = \frac{Pout}{Pout + Ploss(Vg)} \cdot 100\% \qquad (7.3.6)$$

Pout is defined as *Vo/Rload*, and was equal to 80W in considered case.

Efficiency of the converter is clearly lower when input voltage is negative. Most of the accounted losses had higher values under that condition.

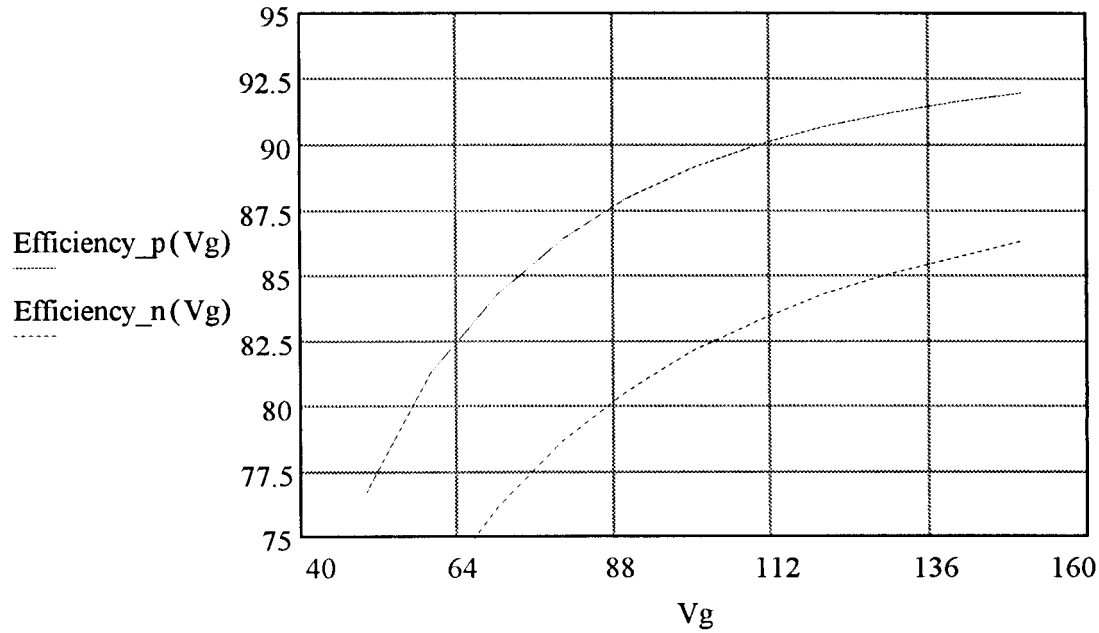

Figure 7.30: Calculated efficiency % for positive and negative line half periods

Formally, the currents in parasitic elements have higher rms values, but there is also another way to look at it.

Consider the non-symmetric gain of the power stage in Fig. 7.4. If duty ratio is zero D=0 (no switching happens), the voltage gain is 1 and power is still delivered to the load. If circuit is in another non-switching state, corresponding to D=1, then voltage gain is zero and so is the output voltage. Therefore, for the same absolute value of voltage gain, power is delivered to output completely by the switching operation when input voltage is negative and it represents harder conditions for stepping up the voltage.

Resulting efficiency of PFC is the average of efficiencies during halves of the line period. The total calculated efficiency is shown in Fig. 7.31, together with measured values (boxes).

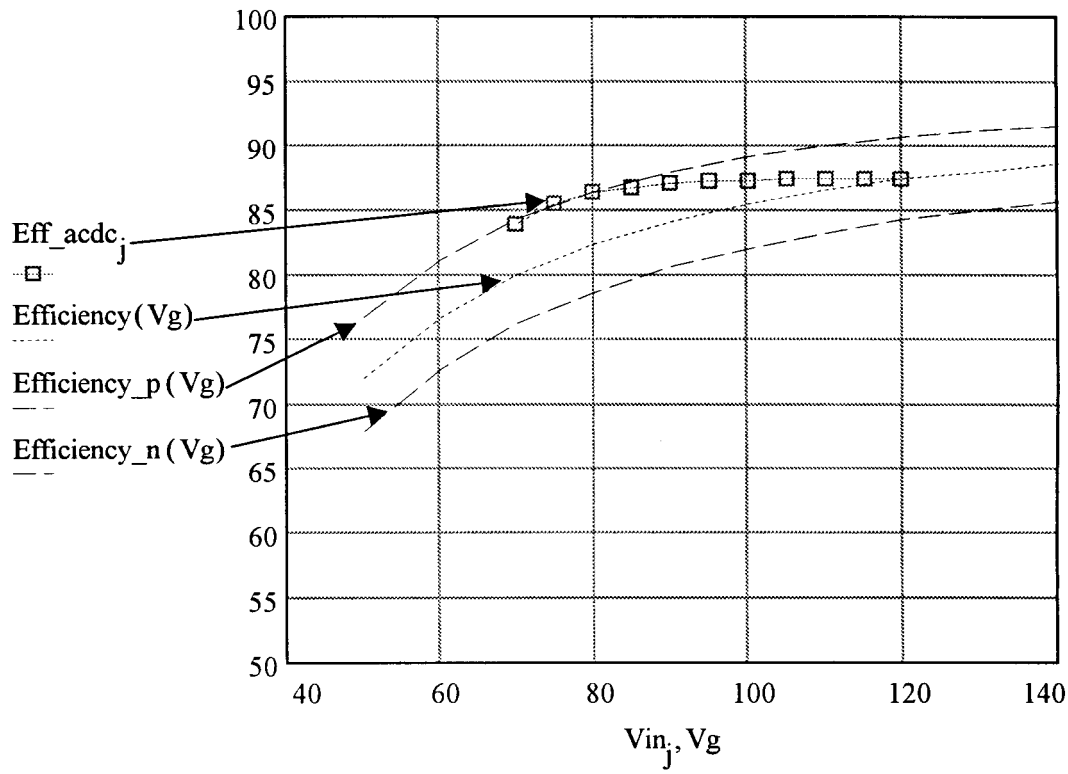

Figure 7.31: Measured efficiency Eff_acdc, calculated efficiency Efficiency(Vg), efficiency for positive and negative halves of the line circle Efficiency_p(Vg) and Efficiency_n(Vg)

Results are in a good agreement with prediction, although some assumption were used for calculations and some effects were not taken into account (core losses, etc.). Effects such as change in switching frequency for positive and negative part on the input voltage cycle were approximated as well.

Partial distortion in input current waveform was appearing during experiments when input voltage reached the region of higher values. It caused the increased current ripple and therefore higher losses which is indicated by the flat part of the measured efficiency

characteristic (at the higher input voltage region). This issue was more of the control noise sensitivity problem, still experimental data generally match theoretical prediction.

Chapter 8

Conclusion

The new idea of the power factor correctors was established, concepts of topologies with bipolar gain were considered and the number of such topologies discussed.

Novel approach of power factor correction was confirmed by practical example, chosen topology was analyzed in detail, prototype was built and experimental data were compared to predictions. Agreement was established between theoretical derivations and experimental results.

New approach of the power factor correction is valid and possible to use. Some comments can be made in general.

Topologies with bipolar gain characteristics tend to have a common feature: high rms currents. The origin of it can be explained as the following.

Fig. 8.1 shows the main currents in the topology used as example. Current waveforms in question are shown in Fig. 8.2. Output current I_O corresponds to current I_C after filtering the ripple in Co. The current I_C is clearly $I_{S'}$ minus I_{L2}, Fig. 8.2. $I_{S'}$ corresponds to I_{L1} during $D'Ts$ time interval. The origination of bipolar characteristic is the fact that by changing duty ratio the positive $I_{S'}$ and negative I_{L2} parts of the current I_C change, so the resulting output current I_O can be positive or negative.

This waveform of I_C in Fig. 8.2 clearly has high rms value in comparison, for example, to related waveform of the boost power stage, Fig. 8.4. DC waveform has the lowest rms value (which is equal to DC value and average value of DC waveform), the waveforms with the same average current and "ripple" waveform present higher rms values.

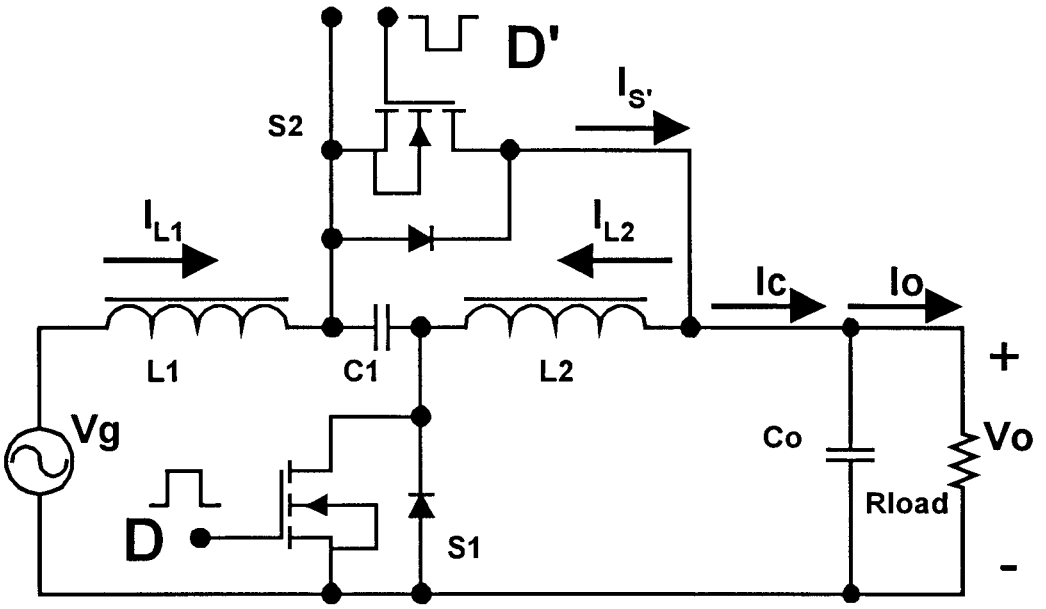

Figure 8.1: Example topology with main currents shown

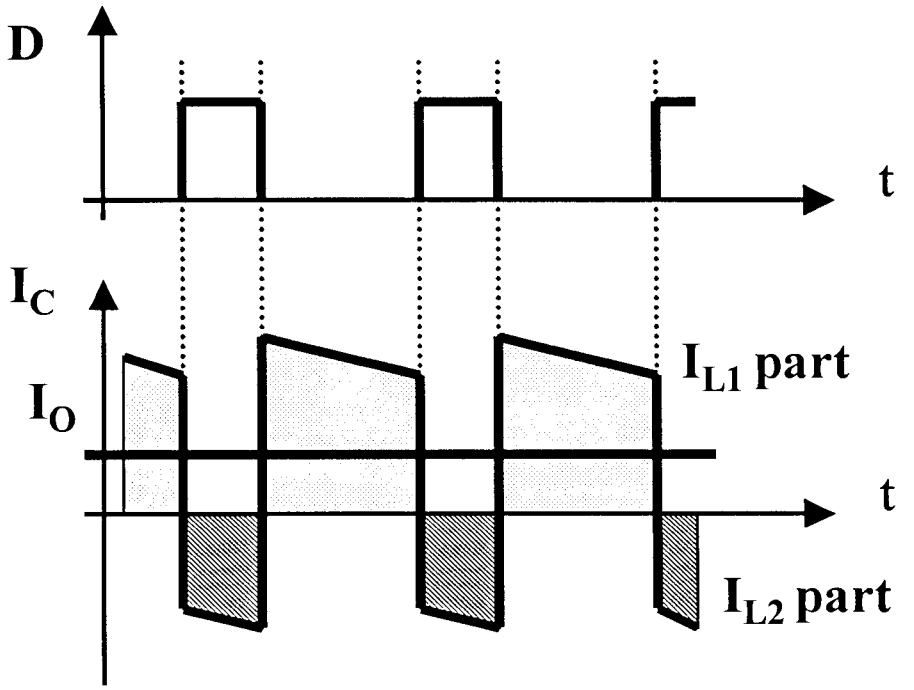

Figure 8.2: Main current waveforms for topology in Fig. 8.1

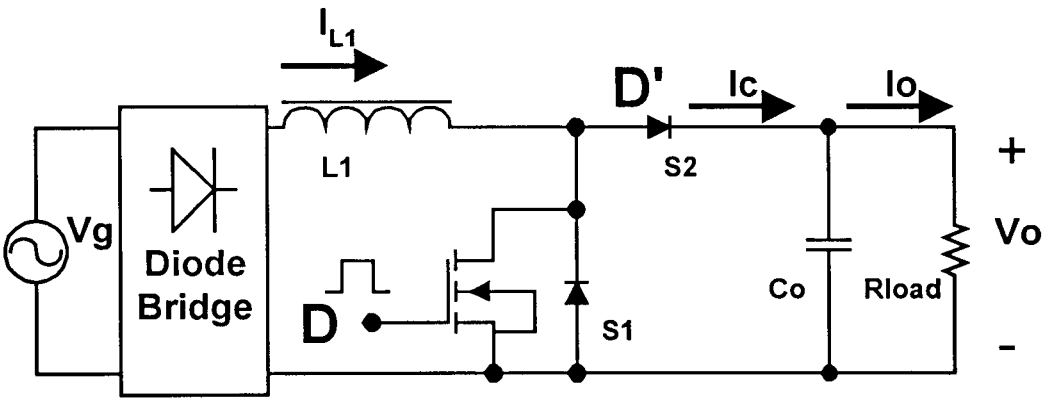

Figure 8.3: Comparison with boost topology

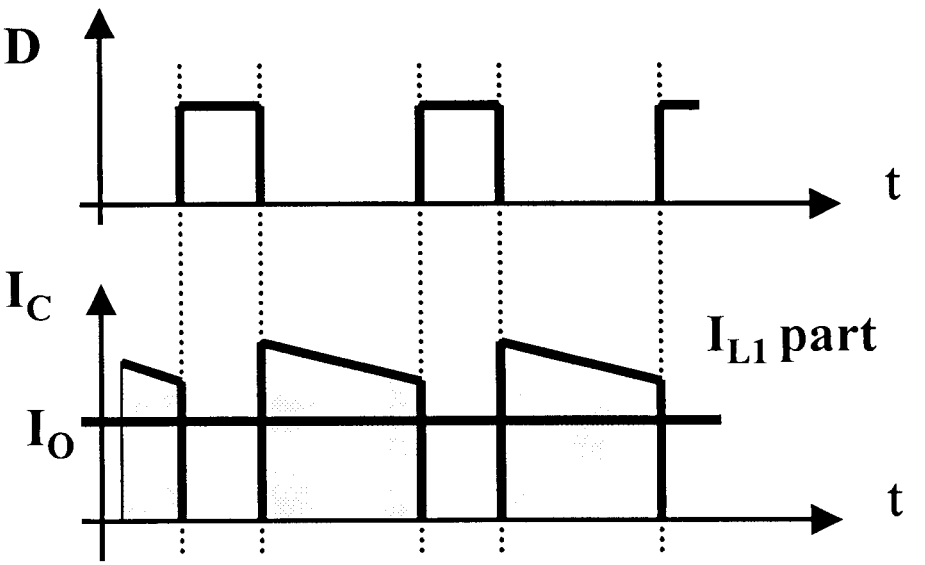

Figure 8.4: Current waveform example for traditional boost topology

For the same average current, current waveform with only positive (or only negative) part will have smaller rms value than waveform that includes parts of both polarities. Example of such only positive waveform is shown in Fig. 8.4; this particular waveform can be observed in a boost converter with input rectification. Certainly, even waveform of one polarity can have arbitrarily high rms, but practical consideration of conventional

topologies allows us to make some assumptions and comparison that confirm discussed considerations.

High rms values of circulating currents increase the losses and therefore affect efficiency of the converter.

It is hard to argue about such general comparison of different topologies; however, the following comments can be made. The losses in input diode bridge are less critical at higher input voltage, and therefore traditional topologies are probably more efficient in that area. As input voltage decreases: the efficiency of traditional topologies goes to zero as input voltage approaches the value of the voltage drop on input diodes. New PFCs, on the other hand, will reach zero efficiency value at zero input voltage. These considerations are illustrated in Fig. 8.5.

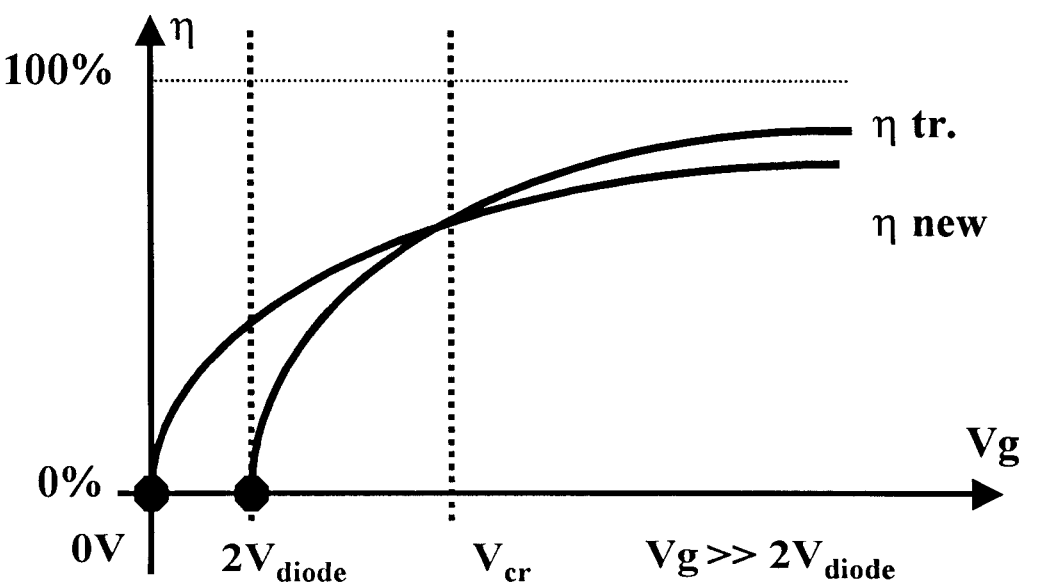

Figure 8.4: Efficiency considerations for traditional and new PFCs

It is clear that there is some voltage *Vcr* below which the new PFCs will show better efficiency. Notice that improving overall converter efficiency will move critical point

Vcr to higher voltage value. Related improvement in efficiency of conventional topology would only slightly suppress this fact, because the main difference in between new and conventional topologies is the losses in input diode bridge. These losses are hardly controllable and will relate to bigger relative part of losses if other losses are decreased

New family of PFCs promises improved efficiency in a range of low input voltages in comparison to traditional topologies with input rectification.

The absence of input diode bridge allows us to include input filter into power factor corrector operation and therefore improve Power Factor. This approach also allows more freedom in input filter design. The fact that in new topologies common point of the power stage and control does not oscillate with the line frequency but is connected to one of the power lines opens some additional options for input filter design, EMI suppressing, etc. These issues will be investigated in a separate chapter, because these advantages are associated with all power factor correctors without input rectification, not only topologies with bipolar gain characteristics.

Part 2

New PF Correctors with Shifted Line (60Hz) Rectification

Chapter 9

Introduction

New general idea of eliminating input rectification was presented previously in this thesis. Topologies with bipolar gain offer options for improvement of efficiency (especially at low input voltage) and power factor. It was shown though that these topologies have a feature of relatively high rms currents. The effect is associated with the fact that output current of these topologies has positive and negative components during one duty cycle, which allows achieving bipolar gain characteristics.

Logically, topologies with currents that do not have positive and negative components during one switching cycle are subject of interest. Providing that such topologies can still operate from AC input and provide DC output – such topologies are expected to have further efficiency improvement in comparison with topologies with bipolar gain.

Traditional topologies used in power factor correction would satisfy the criteria of having only unidirectional currents (and therefore low rms value of such currents). However, they can not function without input rectification under condition of AC input.

This section will present a general approach of modifying some existing conventional topologies to operate with AC input and still provide DC output. General idea will be presented and illustrated on particular example with analysis and experimental data.

Chapter 10

Previously Developed Schematics

There are some topologies developed that have a conventional stage as basis. Conventional in such context means that traditional DC to DC stages were used, not topologies with bipolar gain characteristics. Such topologies were then modified to perform PFC under non rectified AC input condition. Different topologies were reported; they all perform rectification to achieve DC output from AC input but the rectification happens due to operation of the topology, not due to input diode bridge.

Fig. 10.1 shows topology described in [8]. Important fact for the current discussion is that rectification happens due to separate operation of the primary branches during positive and negative semi cycle.

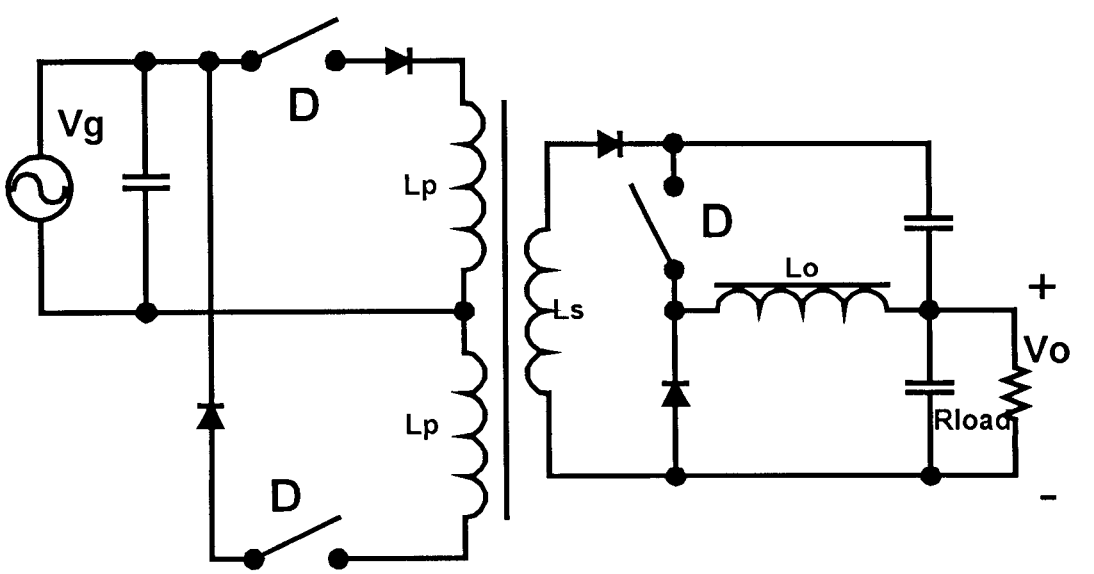

Figure 10.1: General schematic of PFC developed in [8]

Fig. 10.2 and Fig. 10.3 show converter operation at positive and negative semi cycles of input voltage respectively.

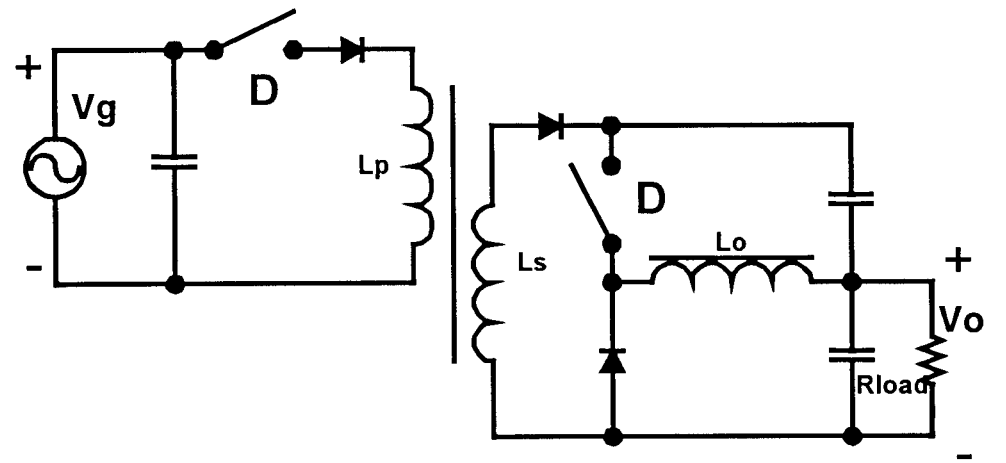

Figure 10.2: Operation of PFC in Fig. 10.1 during positive line semi cycle

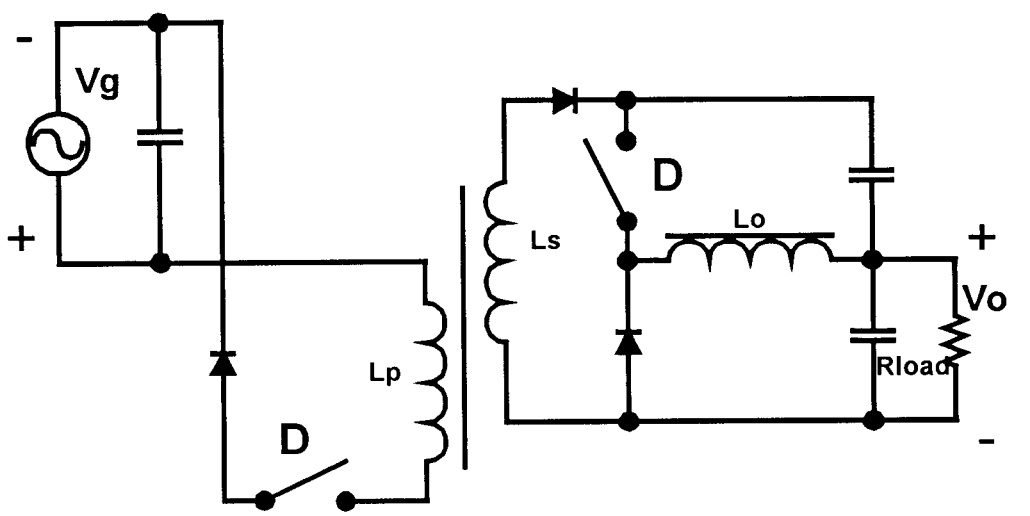

Figure 10.3: Operation of PFC in Fig. 10.1 during negative line semi cycle

Notice that converter has two branches on the primary side, operating separately for positive and negative input voltage. This duplication is a disadvantage in terms of size and cost of the circuit. In addition to that, efficiency benefits in comparison to conventional topology are doubtful because of the fact that diodes are present in these branches to insure operation at the proper polarity.

Circuit with high efficiency was analyzed in [6], Fig. 10.4. The PFC shows good performance, high efficiency and low component count. However, it has a disadvantage that output voltage has to be higher than twice the peak of input voltage for proper boost operation. This fact implies extremely high voltage stress on active and passive components, increase in dynamic losses. It also represents similar complications for the following circuitry (which is conventionally DC to DC stage with isolation).

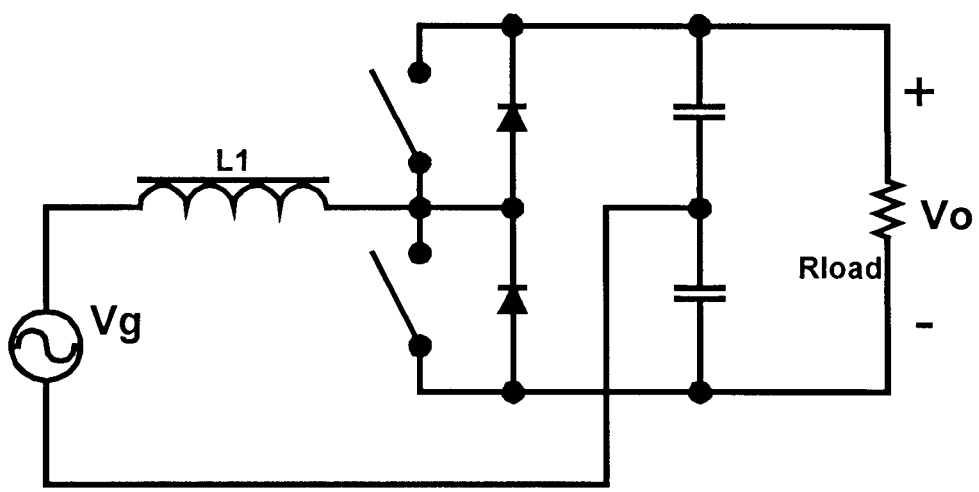

Figure 10.4: PFC based on Half Bridge Boost Topology [6]

Another PFC without input rectification was presented in [4], Fig. 10.5. Circuit has resonant elements *Lr* and *Cr*, which improves the switching but does not change the main idea of operation.

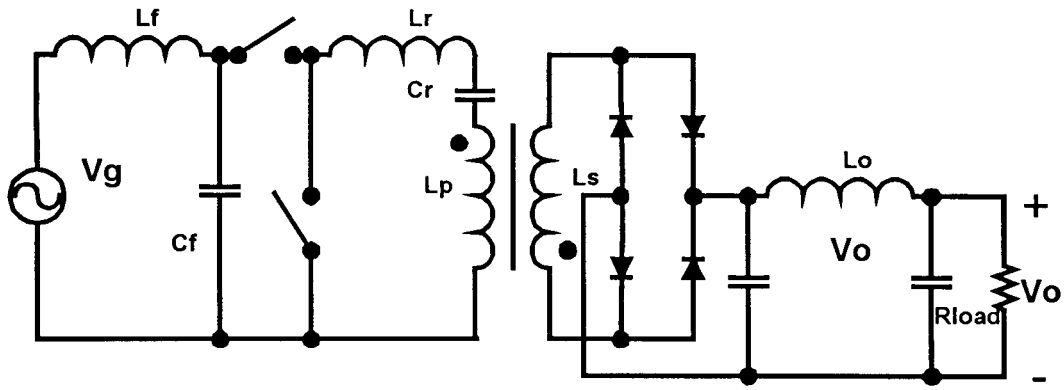

Figure 10.5: Series resonant AC to DC rectifier [4]

The AC input is chopped with high frequency and then rectified on the secondary side, where diode bridge has a function of high frequency switching and line rectification as well.

As a similar solution for rectification, very simple power stage for PFC was computer simulated in [5]. The circuit is based on traditional flyback topology. Single switch on the primary side is implemented as a four quadrant switch and rectification happens on the secondary side.

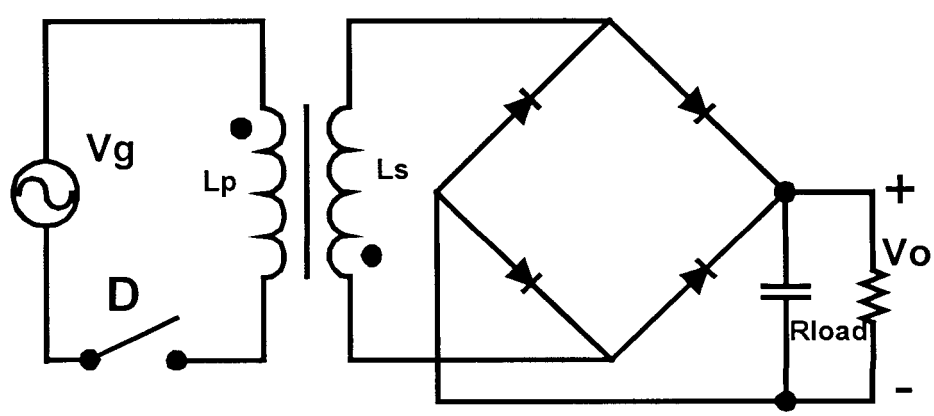

Figure 10.6: PFC based on the flyback topology [5]

Such PFC has simplicity and low cost of the flyback converter, it also has associated low efficiency and big voltage overshoots on the main switch due to problem of the leakage inductance in the transformer. The important disadvantage of such PFC is effective transfer of the diode bridge from the primary (high voltage side) to the secondary (low voltage side). Stepping down applications, such as battery charger described in mentioned paper, will therefore have low efficiency.

Described examples of PFCs without input rectification are based on topologies with no bipolar gain characteristics (and associated high rms currents). However, they have different disadvantages such as excessive number of diodes on the secondary side (and therefore degraded efficiency) [5], extremely high output voltage [6] or excessive number of components on the primary side [8], etc.

The question of finding topology (or general method for creating ones) which has low rms currents of conventional power stage, but can operate at AC input and have no disadvantages commented above, should be definitely addressed.

Chapter 11

Proposed New General Approach for Shifting of Input Rectification

The concept of eliminating of input rectification in power factor correctors based on some conventional topologies (elimination of the diode bridge at the input) will be introduced in this chapter. It will be shown that taking advantage of already existing elements of the topology allows achieving necessary performance of the circuit with AC input without complicating the schematics. Efficiency improvement can be expected without increase in the number of components, size and cost, as it was the case in previously illustrated references.

11.1 Combining Switching at High Frequency and Line Rectification

The general idea can be best illustrated in Fig. 11.1, where typical isolation section of the switching converter is shown. The two diodes operate at the switching frequency and generate rectified (DC) voltage regardless of the polarity of the voltage applied to the primary side. In this way, the diodes can perform the double-duty: high frequency switching and rectification as well as at the same time the rectification of the low (60 Hz) line frequency. In other words, the secondary of the converter can operate (at switching frequency) in traditional way when input voltage of the primary is positive, and then just inverse the order of switching and operate in a similar mode when input voltage of the primary changes polarity. Magnetic component is used efficiently since it operates at

high switching frequency, yet the 60 Hz line modulation is transferred to the secondary of the transformer and rectified there.

Using diodes as rectifiers for both, switching at high frequency and low frequency rectification, would allow to improve efficiency of the converter with less expenses in comparison to circuits overviewed in chapter 10.

Typical converters may have primary side with either simple winding (such as flyback converter) or tapped (two windings) primary side (such as in push-pull and bridge-type converters). Thus, the next section will give examples of both general cases.

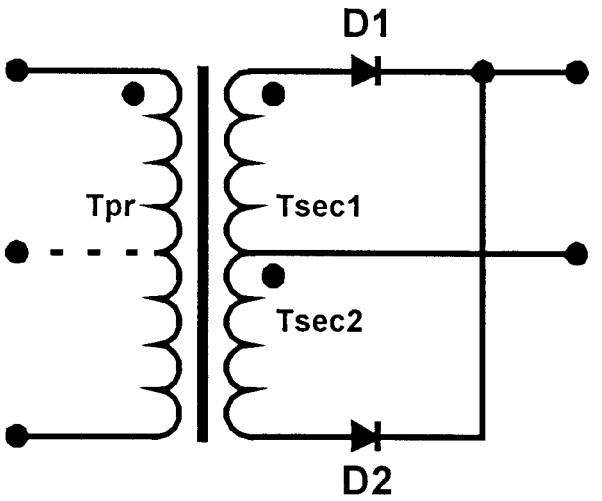

Figure 11.1: General isolation transformer with two secondaries and following rectifiers

Some topologies with isolation transformer have only single secondary winding (for example flyback topology). Sometimes it is possible to add another secondary and create schematic in Fig. 11.1 without violating the operation of the converter. Then same idea of line rectification can be applied.

Using non rectified input voltage at primary side of the converter would normally lead to the need to implement four quadrant (ideal) switches. Such switches have to conduct current in any direction and block voltage of any polarity since the input voltage is not rectified any more. Possible implementation of such switches was considered in chapter 6.3.

Examples of modified topologies are considered in the following section.

11.2 Some Topologies for Implementing of the Proposed Approach

Fig. 11.2 shows flyback derived topology (input EMI filter is not shown). It implements the general presented idea of line rectification on the secondary of isolation transformer and has less losses and smaller component count than topology described in Chapter 10; see Fig. 10.6, [5].

The operation is illustrated in Fig. 11.3 and Fig. 11.4. Fig. 11.3 shows positive input voltage period of time: input current *Ig* flows on the primary side at DT_S time interval, diode D1 conducts current on the secondary side during $D'T_S$ time interval. Circuit resembles operation of conventional flyback converter.

When input voltage is negative, Fig. 11.4, input current *Ig* flows in opposite direction during DT_S time interval so flux in the core of transformer is exercised in different direction and other diode, *D2*, conducts during $D'T_S$ time interval. Again, operation of conventional flyback topology is resembled at negative semi cycle of input voltage.

Turns ration of the transformer should be such that diodes remain off during DT_S time interval. This latter condition is easily met.

Control and operation of such converter is pretty much similar to traditional case of flyback power factor corrector. Isolated drive is needed for the four quadrant switch, and some modifications are possibly needed for voltage/current sensing of the modified converter.

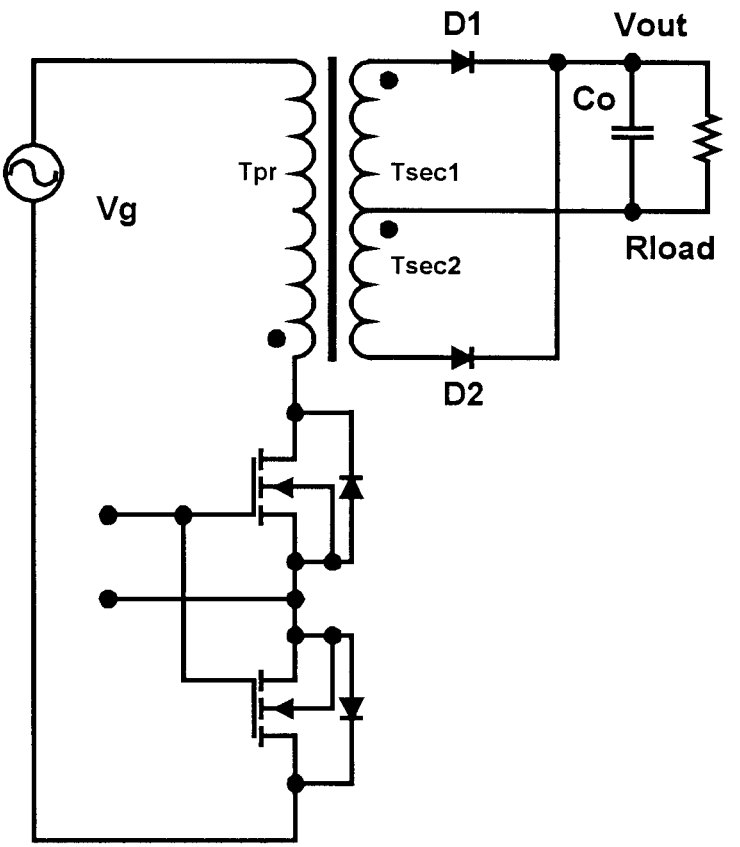

Figure 11.2: Proposed flyback derived topology

New converter inherits the advantages of the flyback original topology: it is simple and chip and it has a property of an automatic current shaper in DCM. However, it also has flyback disadvantages: chopped input and output currents, low efficiency and problems associated with leakage inductance of the transformer.

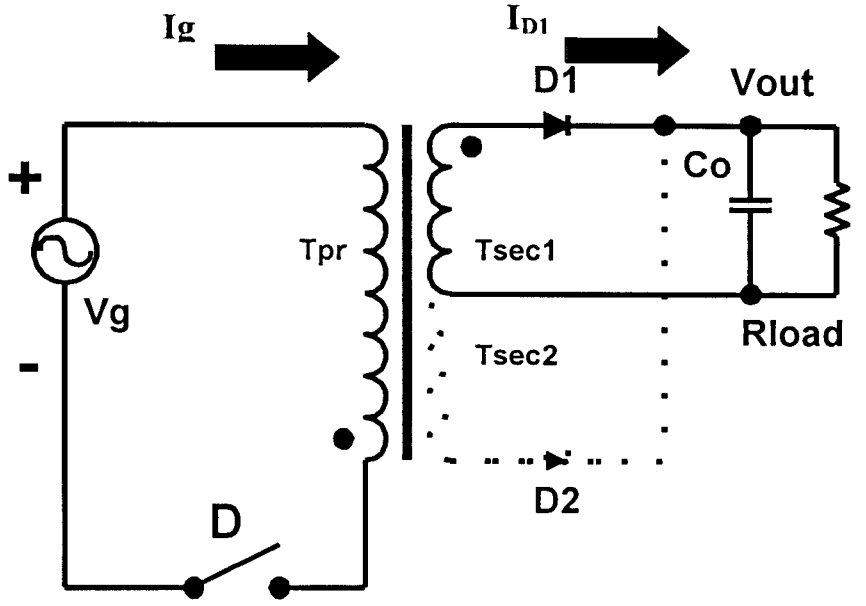

Figure 11.3: Operation of the new topology at positive input voltage semi cycle

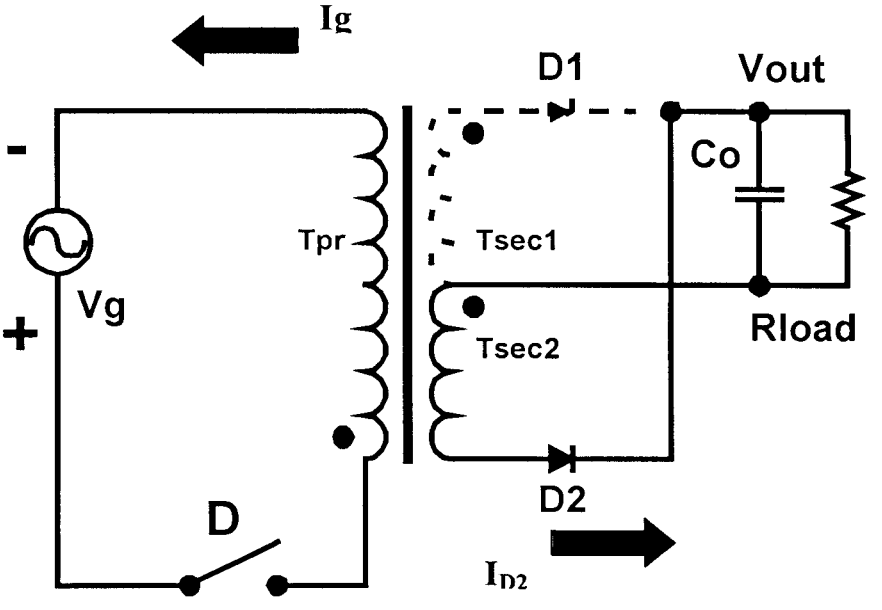

Figure 11.4: Operation of the new topology at negative input voltage semi cycle

Push-pull and bridge type converters are certainly suitable for the new approach. These converters typically have a transformer with secondary side illustrated in Fig. 11.1. The new concept will be further illustrated on the basis of current fed push-pull, which is also called isolated boost or Clarke converter, Fig.11.5.

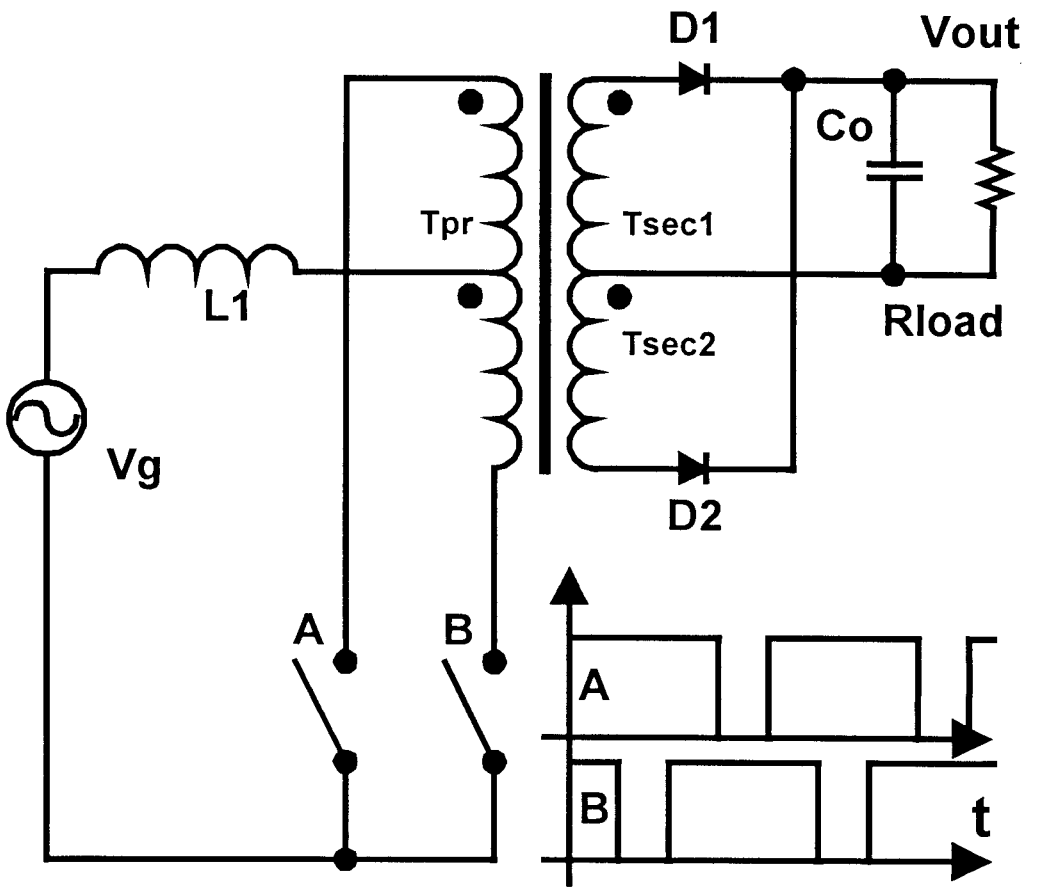

Figure 11.5: Clarke converter as power factor corrector without separate input rectification unit

Switches *A* and *B* are driven with overlaps, and overlapping part of the switching period corresponds to on time of the switch in parent boost converter. Operation and waveforms are therefore similar to the simple boost case.

The implementation of the isolated boost as power factor corrector was discussed, for example, in [11], but with the conventional diode bridge rectification stage. Our approach though, outlined in this chapter, is to eliminate the diode bridge stage all together and still achieve power factor correction. This is possible in this topology as described earlier, thanks to integration of rectification at high switching frequency and low frequency (60 Hz AC) in the same switching devices of the original basic DC/DC isolated topology. Basic converter has to be appropriately modified, for example, the original primary side switches *A* and *B* (Fig. 11.5) must be replaced with four quadrant switches.

Consider the operation of the converter. First assume that voltage is positive at one half of line period, Fig. 11.6. When both switches *A* and *B* are on (control signals are overlapped), the currents in the primaries of the transformer cancel each other, this time interval corresponds to DT_S time interval in conventional boost stage.

When only one switch is on, current appears on the secondary side via related diode. Switch *A* causes diode *D2* to conduct, and switch *B* relates to the diode *D1*, Fig. 11.6. This part of operation resembles operation of conventional isolated boost with rectified input voltage.

At the moment when input voltage becomes negative, Fig. 11.6, current in main inductor *L1* still ramps up when both switches are on although in different direction. But now when single switch *A* is on, current flows via diode *D1* (not *D2*), and single operation of the switch *B* is now resulting in conduction of the diode *D2* (not *D1*).

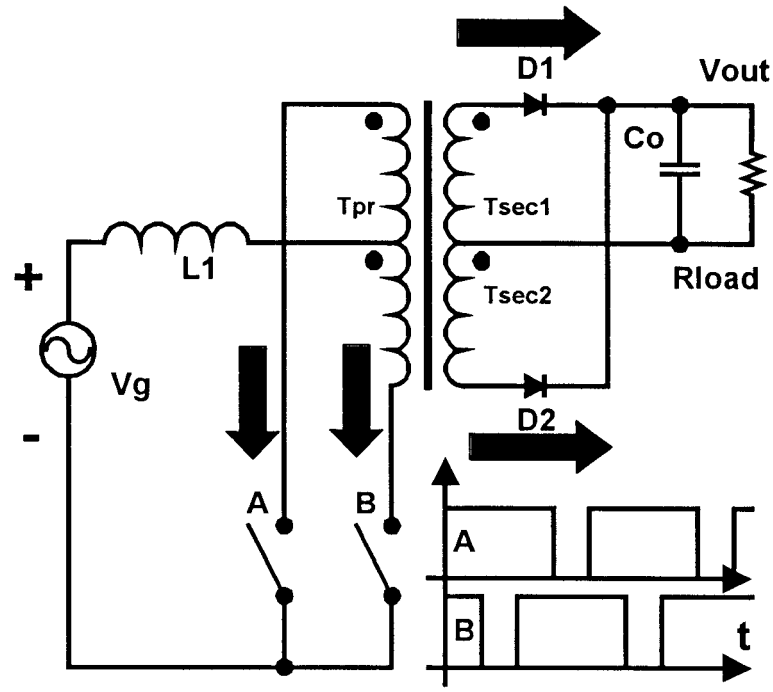

Figure 11.6: Operation of the Clarke based converter at positive voltage half period

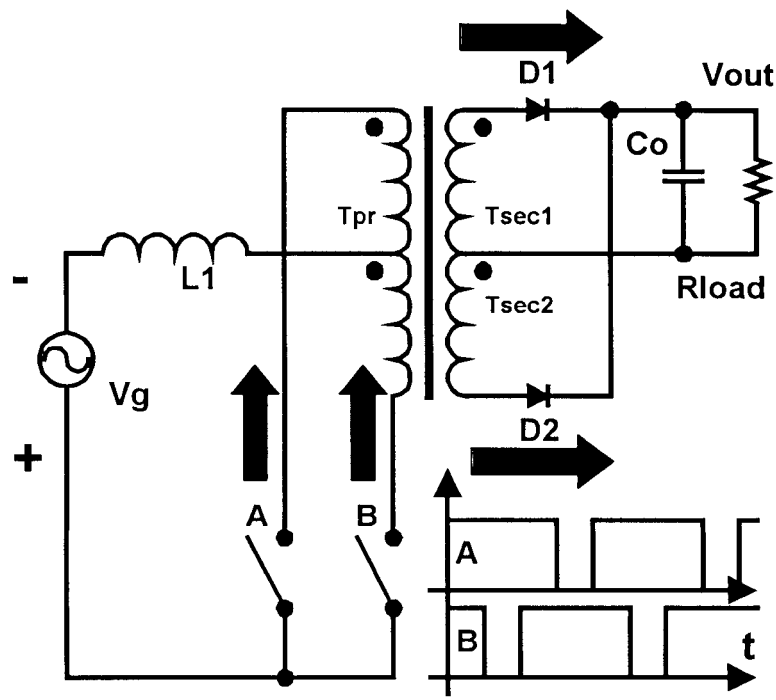

Figure 11.6: Operation of the Clarke based converter at negative voltage half period

The proposed concept would work for a number of converters including flyback, push-pull and different bridge type power stages. One example will be considered in detail in the following chapter to show and verify the analysis, confirm theory with experiment and illustrate the operation with real waveforms.

Chapter 12

Implementing of the Proposed Method on the Basis of Clarke Converter

The concept of combining high frequency switching and low frequency line rectification will be illustrated in this chapter on particular example. Analysis will be conducted and experimental data shown. New converter will be compared with conventional prototype and related conclusions will be presented.

12.1 Analysis of the PFC Based on Clarke Converter

The isolated boost or Clarke converter was chosen for practical implementation with the new approach. Chosen prototype offers front end PFC with isolation same time; it has similar to simple boost stage operation. Operation of the new circuit would be easy to compare to operation of original prototype so advantages and possible disadvantages of the new concept would be easy to outline.

Operation of the chosen topology is very close to one of the boost, with similar gain characteristics and dynamics. By time interval *DTs* we will understand overlap time interval when both switches *A* and *B* are on.

Ideal gain *M(D)* is then easily derived as shown in (12.1.1) and plotted in Fig. 12.1, where *N*=1.5 is a transformer turns ratio. *Vo* and *Io* will stand for output voltage and current respectively, and *Vg* and *Ig* are input voltage and current.

$$M(D) = \frac{Vo}{Vg} = \frac{N}{1-D} \tag{12.1.1}$$

If we assume no losses in ideal case, then (12.1.2) is valid.

$$Pin = VgIg = Pout = VoIo \tag{12.1.2}$$

Then (12.1.3) can be easily derived.

$$M(D) = \frac{Vo}{Vg} = \frac{Ig}{Io} \tag{12.1.3}$$

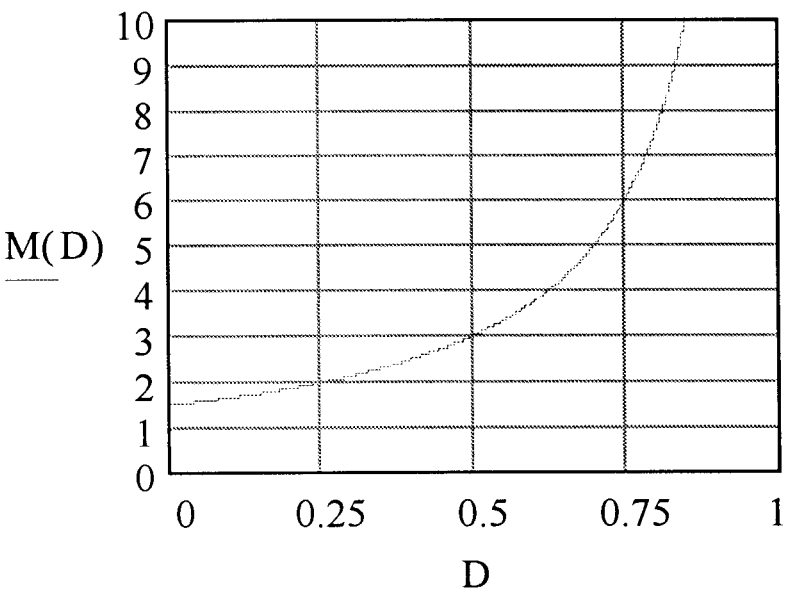

Figure12.1: Ideal gain M(D) for the isolated boost

Let's now introduce parasitic element to represent losses in the components of the converter, Fig. 12.2. Simple assumptions are made, for example assuming low ripple in input current; not all losses are taken into account. *Rl* represents resistance of the inductor, *Rs* is on resistance of the switch plus resistance of the transformer winding, *Vd* is a voltage drop across the diode.

Efficiency of the converter can be therefore expressed as (12.1.4), where *Pout* is output power and *Ploss* represents losses. Equation (12.1.5) is another possible

expression of efficiency. It is clear that $Ig/Io=M(D)$, since no additional paths for current were created (where $M(D)$ is an ideal voltage gain from (12.1.1)). $M_R(D)$ here represents real voltage gain of the converter, which is different from ideal gain M(D) because of the losses.

$$\eta = \frac{Pout}{Pout + Ploss} \tag{12.1.4}$$

$$\eta = \frac{VoIo}{V_g I_g} = \frac{M_R(D)}{M(D)} \tag{12.1.5}$$

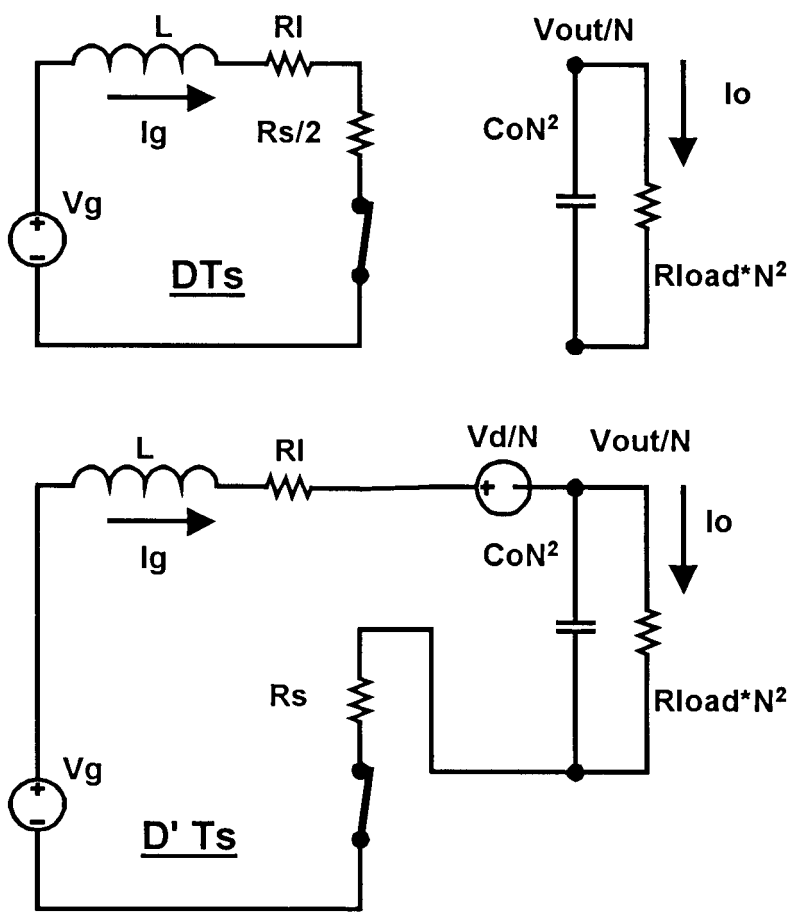

Figure 12.2: Equivalent circuit with parasitics for DTs and D'Ts time intervals

Expressing losses in parasitic resistances and diode by rms currents and then by output voltage and load resistance, final equation is achieved for losses in the converter *Ploss* (12.1.6). Notice that not all losses are accounted for; however, used method allows convenient analytical expression.

$$Ploss=\left(\frac{VoN}{(1-D)Rload}\right)^2 Rl+\left(\frac{VoN}{(1-D)Rload}\right)^2\left(1-\frac{D}{2}\right)^2 Rs+\frac{Vd}{N}\frac{Vo}{Rload\sqrt{1-D}} \qquad (12.1.6)$$

Finally, from (12.1.4), efficiency can be expressed as (12.1.7).

$$\eta=\frac{1}{1+\beta(D)} \qquad (12.1.7)$$

where $\beta(D)$ is represented by (12.1.8)

$$\beta(D)=\frac{N^2Rl+N^2(1-\frac{D}{2})Rs+DRs+\frac{Vd}{Vo}\frac{(1-D)^{3/2}}{N}}{(1-D)^2Rload} \qquad (12.1.8)$$

Predicted efficiency as a function of duty ratio for isolated boost is shown in Fig. 12.3. As expected, efficiency degrades close to D=1 point, where ideal gain of the power stage would approach infinity.

Predicted voltage gain *Mr(D)*, as a function of duty ratio D, can be expressed from (12.1.5) via efficiency and ideal gain and is plotted, Fig. 12.4. Value 1.5 was used for N.

Derived characteristics are similar to ones of the conventional boost converter, as expected.

Operation of the boost is a common knowledge. The isolated boost or current fed push pull can be analyzed similarly. The main interest is therefore in the difference of new modified isolated boost in terms of losses or efficiency.

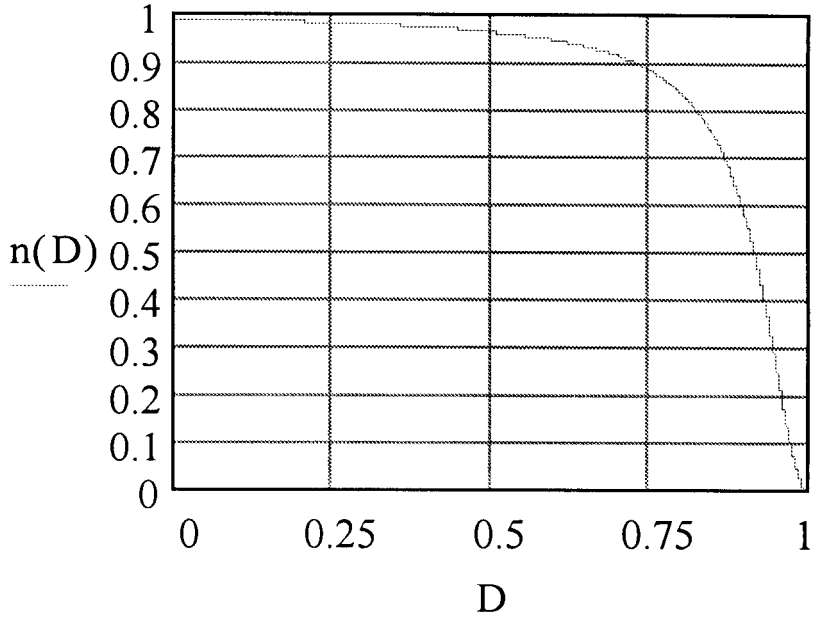

Figure 12.3: Predicted efficiency as a function of duty ratio for isolated boost

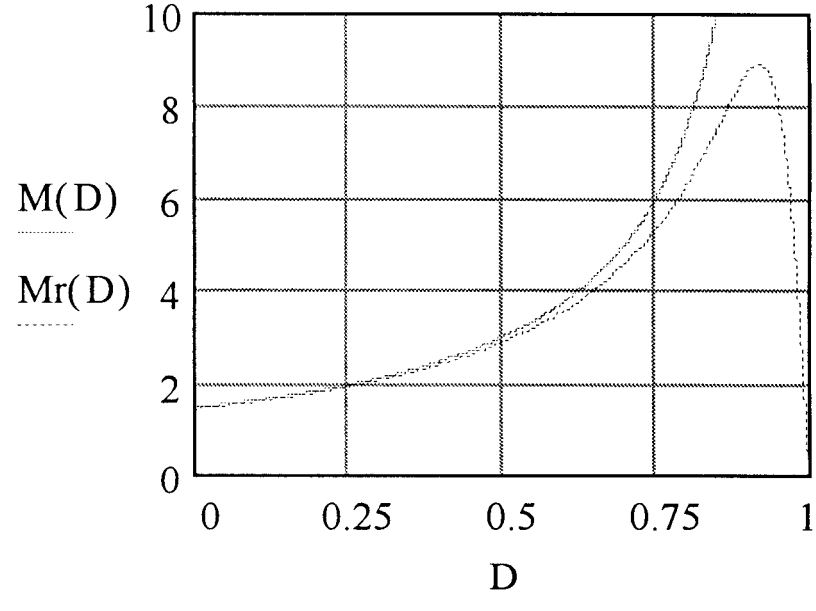

Figure 12.4: Ideal voltage gain M(D) and predicted voltage gain Mr(D)

Eliminating of input diode bridge eliminates losses discussed in chapter 5. However, it is not the only difference from traditional PFC with input rectification. Implementing four quadrant switches, see section 6.3, creates additional conduction losses. Clearly, expected overall benefit in efficiency is a difference between losses in the diode bridge and losses in additional MOSFET of each "ideal" switch in bridge-less converter.

Trade off should be more dramatic at low input voltages because of one more reason. Since input current approaches infinity when input voltage *Vg* approaches 2 diode voltage drops in case of traditional PFC, and 0V in case of new configuration: more benefit in efficiency for the new PFC is expected at low input voltages.

This circuit was logical to compare with traditional isolated boost with usual single MOSFET switches and diode bridge, so discussed trade-offs would be clearly illustrated. Data is presented in the next section.

12.2 Experimental Verification and Data. Comparison with Traditional PFC

The general boost topology can be controlled in many ways, especially popular are PWM with zero current sense (UC3852 from Unitrode) and average current control (UC3854). These integrated circuits could be used with additional circuitry to produce overlapping signals *A* and *B* in Fig.11.5; however, another integrated circuit UCC3857 (average current control) is specifically well suited for isolated boost. Switch *D* is added to improve the converter performance and decrease DC losses.

There is no difference in converter operation at positive or negative halves of the line cycle, but control IC needs certain polarities of input signals to function properly.

Additional circuitry was therefore used to ensure such polarity for input voltage and input current senses, as shown in simplified schematic in Fig. 12.5.

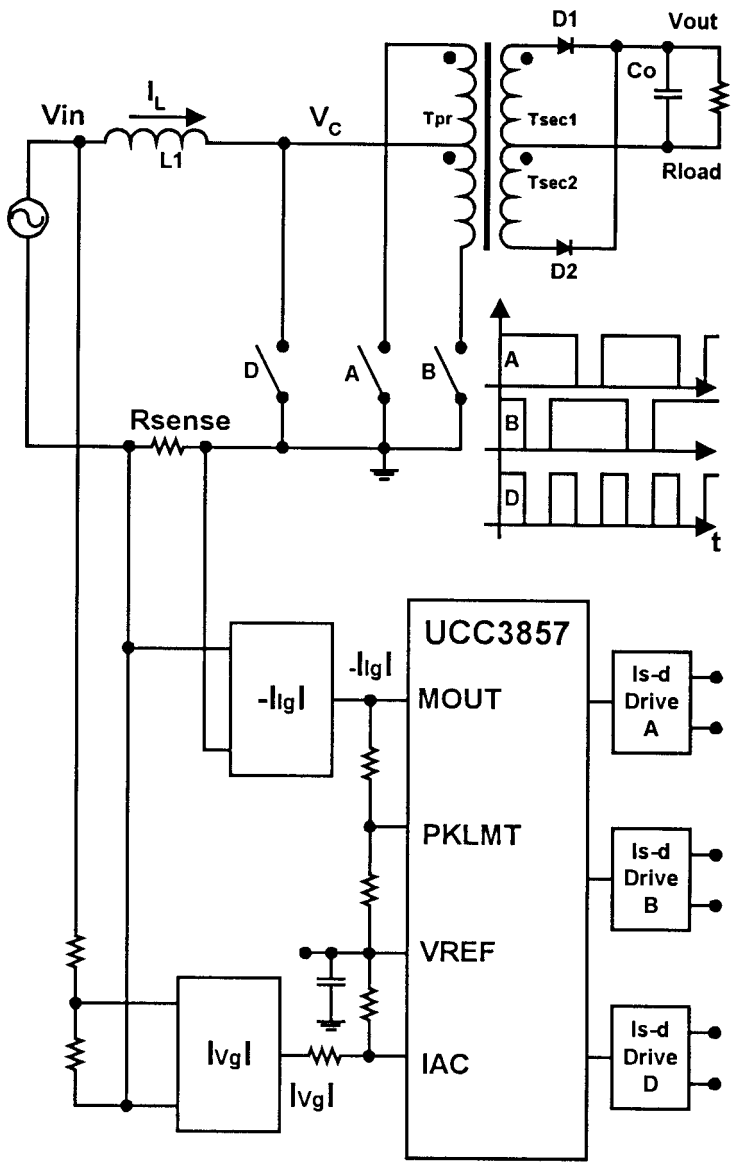

Figure12.5: General schematic of new Power Factor Corrector without input rectification

There are two absolute value circuits, one for current sense and one for input voltage sense. Detailed schematic is shown in Fig. 12.6.

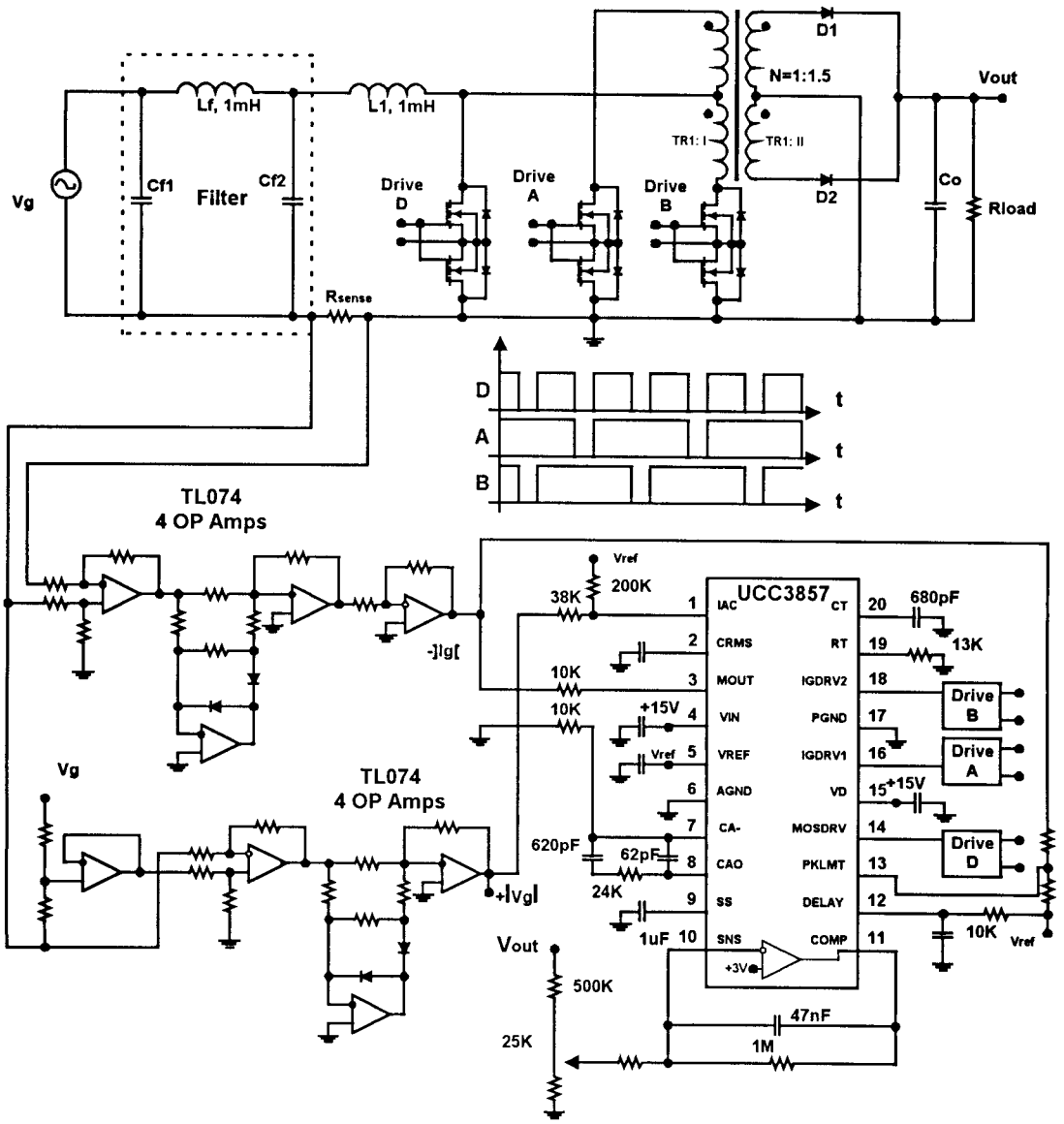

Figure 12.6: Detailed schematic of the new Power Factor Corrector

It was found that input called *IAC*, which senses input voltage and effectively sets the value of average current, is a current sink with some constant voltage potential. Stepping input voltage down for absolute value circuit and using respectively scaled down resistor

at *IAC* input can therefore result in significant distortion of current waveform, unless bias to *Vref* is used.

Isolated drives were implemented to drive four quadrant switches. Output voltage can be any value because of isolation transformer. It was chosen to be 160 V, so 500 Ohm load would provide 50 W output power and allow a range of low input voltages.

Chosen voltage also insures a proper operation of boost derived stage for input voltages up to 75V, considering 1.5 turns ratio of the transformer. This range was chosen because low input voltages were of the main interest since it is the most critical area of operation for the PFCs and the advantages of the new approach are most illustrative in that region.

Exactly the same circuit was used to measure performance of traditional isolated boost with input rectification. It is important to point out, that in latter case original single MOSFET switches were used to provide fair comparison with new topology (versus four quadrant switches in the new topology). The main interest is the difference in efficiency of these two similar topologies (they both offer power factor correction and galvanic isolation in a single stage; similar average current control was used in both cases).

Waveforms for traditional and new topologies are shown in Fig. 12.7 and Fig. 12.8 respectively. Upper trace is a voltage right before input inductor *Vin*, lower trace is inductor current I_L, and voltage of the middle point of the transformer primary V_D (voltage across switch D in Fig. 12.5) is shown at the bottom, the same way for both topologies.

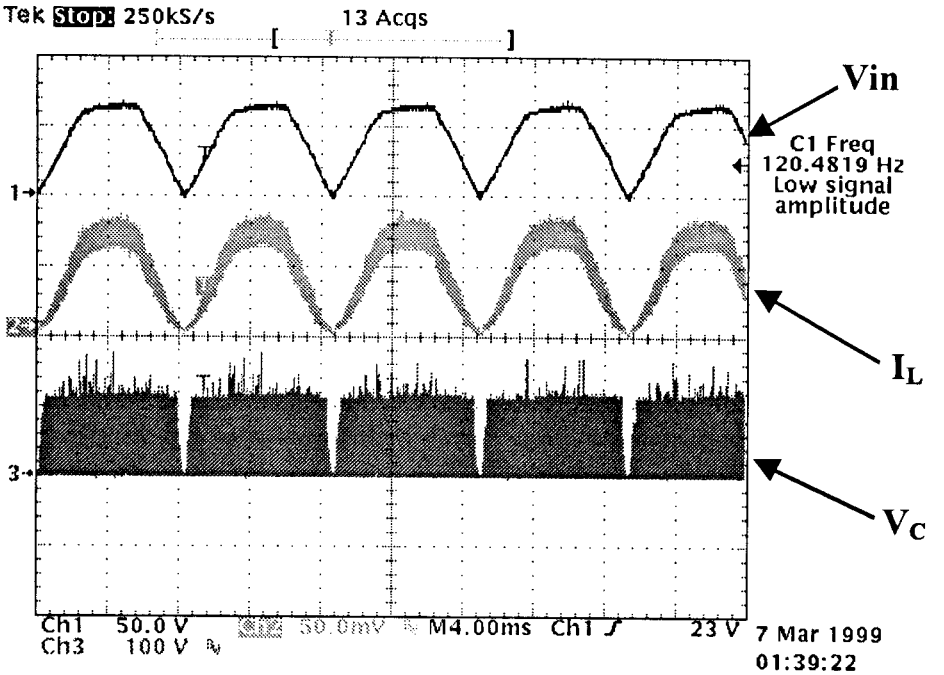

Figure 12.7: Waveforms for the traditional isolated boost topology (with input rectifier).

Vg=50Vrms, Pout=50W

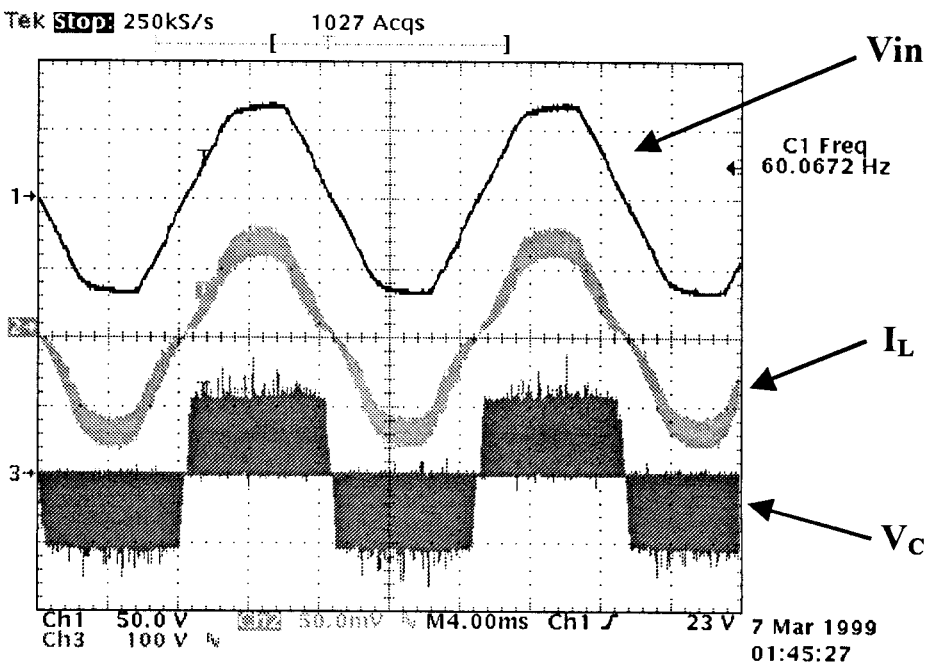

Figure12.8: Waveforms for the new topology.

Vg=50Vrms, Pout=50W

Fig. 12.9 shows measured efficiency for new (top trace) and traditional (bottom trace) topologies for output power 50 W. New circuit clearly has better efficiency; the difference between two sets of measurements is shown in Fig. 12.10.

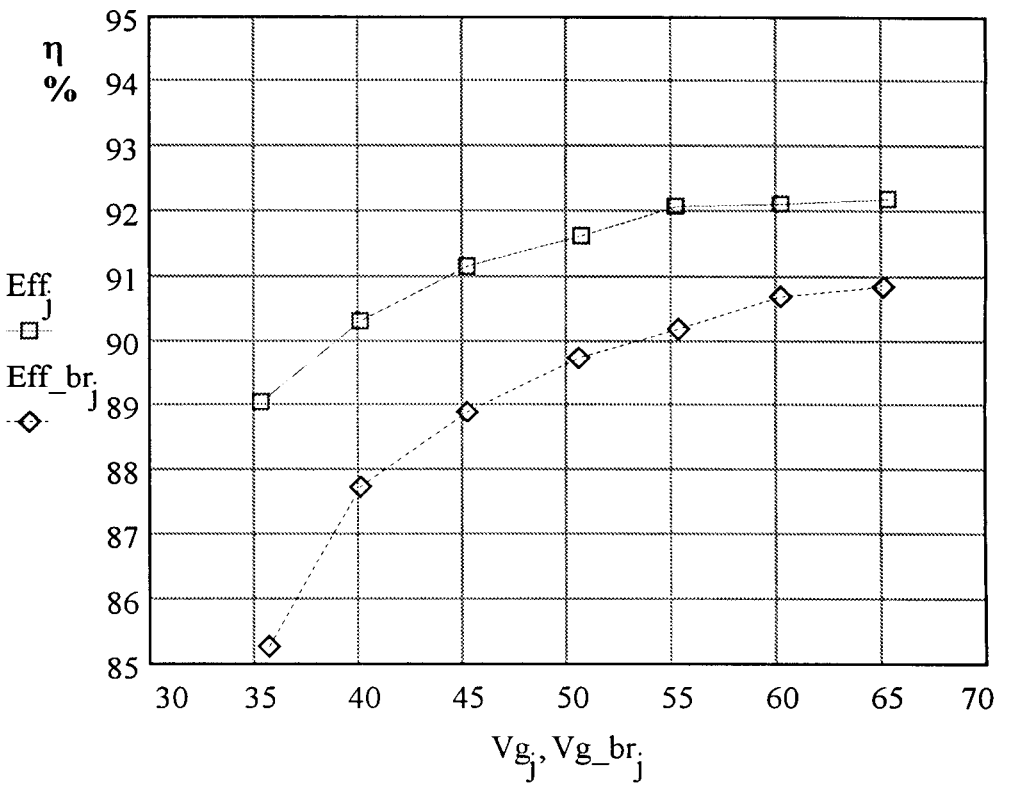

Fig.12.9: Efficiency measurements % vs. Vg. Top trace: new topology. Bottom trace: traditional isolated boost

The advantage can be explained by the fact that losses in input rectifier bridge (chapter 5) were completely eliminated. Some additional losses in four quadrant switches turned out to be non-significant. The difference between conventional MOSFET switch and four quadrant switch is a second MOSFET in a latter, which drain and source terminals are connected "backwards," see Fig. 6.10. This additional element is associated with body diode of the MOSFET, which is even shorted by the small on

resistance (drain and source are functionally interchangeable nodes, only body diode makes a difference in applications).

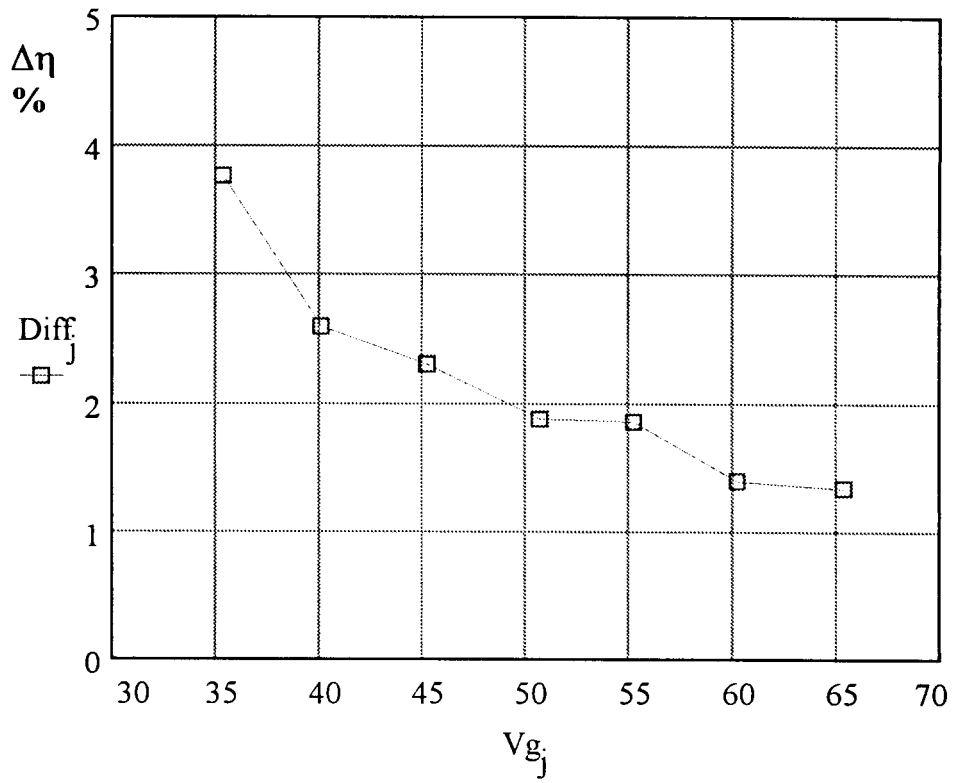

Fig.12.10: Efficiency advantage of the new topology, %, as a function of input voltage Vg (Difference of efficiency values shown in Fig.12.9)

The losses in a four quadrant switch are therefore not dramatically higher than in a single MOSFET, and in fact much less than losses in input diode bridge. Another point is that it is always possible to easily upgrade the MOSFETs to ones with less on resistance, while changing the diode bridge would hardly decrease the losses.

Fig. 12.10 clearly illustrates the advantage of the new approach. The efficiency improvement corresponds to the shape of loss curves described in chapter 5, when losses in input rectifier were investigated. New method has more significant improvement at

low input voltage, where power factor correctors operate in the most critical conditions. At this region the input current is the highest to provide constant output power of the converter and therefore converter operates at high voltage gain. Having lowest efficiency under this condition leads to increased losses and overheating. Improvement of efficiency in this critical region is therefore a very important issue.

Chapter 13

Shifted Line Rectification: Conclusion

New approach of implementing Power Factor Correction circuits was presented. Some conventional topologies with isolation can be modified in such a way that primary side of the converter operates under AC input condition (which often requires implementation of the four quadrant switches). Secondary side of such topologies would have a function of low frequency line rectification in addition to the function of conventional high frequency switching. This double function of the switching elements is shown to be effective.

Example circuit was analyzed, control for new schematic was designed and prototype was built. Measured characteristics were presented and compared to characteristics of the conventional topology. New circuit showed higher efficiency in comparison to parent topology with input rectification.

New family of PFCs promises improved efficiency in all input voltage range, especially significant at low input voltages, in comparison to traditional topologies with input rectification. The advantage of the new topologies in comparison with conventional origins will depend on used components for four quadrant switches. Ideally, the eliminated losses in input rectifier will represent the efficiency improvement, practically though some losses in additional components of four quadrant switches will somewhat decrease the advantage. Using MOSFETs with low on resistance makes these additional losses non-significant and efficiency advantage close to the maximum possible.

The absence of input rectifier also allows including input filter into power factor

corrector operation and therefore improving Power Factor. New approach also allows more freedom in design of input filter.

New topologies also introduce some additional options for input filter design, EMI suppressing, etc., because of well defined connection of the power stage to power lines. These issues will be addressed in the following chapters.

Part 3

Advantage of Bridgeless PFCs: Power Factor Improvement

Chapter 14

Introduction

Input filter is a necessary part in modern switching converters. Although modern circuits usually have power factor correction and provide high power factor values - all such converters introduce ripple of input current at switching frequency and related harmonics of this ripple, which need to be filtered. Different standards apply, and necessary filter has to be implemented to attenuate noise signals according to these standards and amount of introduced harmonics and noise. Practically, filters have different topologies with inductors in series and capacitors in parallel to attenuate Differential Mode (DM) and Common Mode (CM) noise. These reactive elements introduce phase shift in voltages and currents of the circuit. This effect certainly degrades the value of power factor, since unity power factor suggests zero phase shift between source voltage and load current.

Input filters are designed with objective to have necessary attenuation and lowest possible influence on the power factor value, latter condition restricts the possible design options and there is always some influence on the power factor value from the input filter. This effect also changes with the load current.

The degradation of power factor, associated with input filter, will be discussed in this part of the thesis. The unique features of converters without input rectification will be outlined, related to power factor improvement. Possible schematic improvements include increasing the noise immunity of the control by sensing the input voltage right on the voltage source, where converter noise is filtered. Complete integration of input filter into operation of power factor corrector is also possible because of the absence of rectifier

between power factor corrector and the filter. General comparison of implementing the filter "before" and "after" the diode bridge rectifier is shown in [15], so the absence of the rectifier enables the best conditions for input filter design. Analysis of different input filter and control circuitry connections will be shown and experimental data will be discussed and compared with predictions.

Chapter 15

Effect of Input Filter on Power Factor Value

Usually input filter is designed to have minimal influence at 60Hz line frequency; however, there is always some degradation of power factor value that properly controlled power stage would otherwise provide without this effect from input filter.

Another issue is that although necessary attenuation mainly defines the values of the input filter, designers usually prefer to increase the values of capacitors and decrease the values of inductors from technological point of view. Inductors have to be rated at certain current to avoid saturation. Winding of the inductor is much less technological than capacitor production. There are always design issues of core losses, preserving the correct gap in inductor, etc. Natural trend to use more and more capacitance than inductance in input filter is in opposition to design of input filter with as small a power factor degradation as possible.

New converters without input rectification open beneficial opportunity to include input filter into power factor correction. Just eliminating the diode bridge allows to unite two usual capacitors "before" and "after" the rectifier, *Cf* and *Cin* in Fig. 15.1. Capacitor *Cf* is a part of the input filter, and such connection provides better filter performance. Capacitor *Cin* is usually needed for circuit control to function properly and especially needed when, for example, input inductor operates on the boundary of DCM or in DCM.

It will also be shown that converters without input rectification allow to correct power factor right before the input filter, not after as in conventional topologies, therefore improving overall performance. This feature also significantly lowers discussed

restriction on increasing capacitance value and decreasing the value of inductance in the input filter.

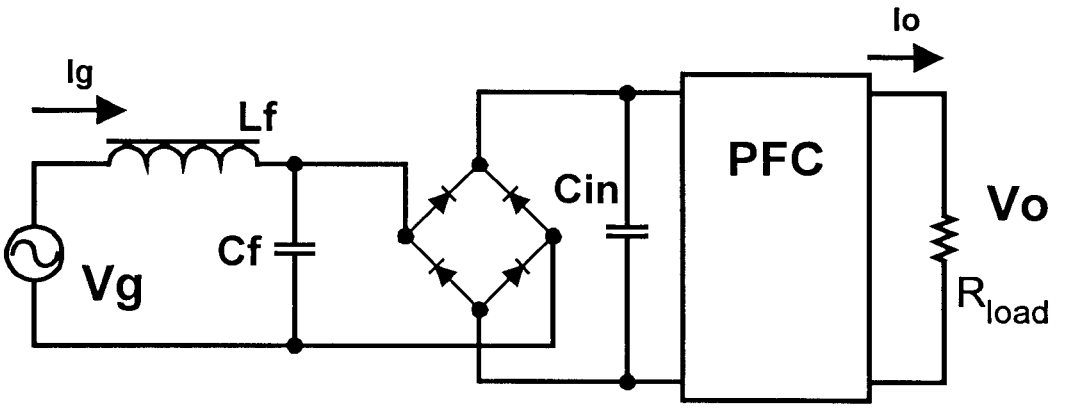

Figure 15.1: Simplified schematic of conventional PFC with input filter

First, equivalent circuit for the power factor corrector needs to be established. Notice that the area of interest is 60Hz and some frequencies just above, since line voltage can be slightly distorted by other consumers and have extra harmonics. Only at these frequencies the proportionality between input voltage and current is critical to achieve unity power factor or, in other words, power factor corrector can be represented as a resistor with some effective value.

Feedback to regulate output voltage is usually closed at frequencies below 1Hz to maintain necessary output voltage but avoid interference with Power Factor Correction. This means that feedback defines lower boundary for the region where Power Factor Corrector can be represented as resistor loading input voltage source. On the other hand, at frequencies much higher than 60 Hz, the behavior of the filter could cause a difference in a voltage amplitude and phase at the input of PFC and cause feedback to react and effectively change the value of effective resistor. PFC also can not be considered as

resistor at switching frequency and higher. Another issue is that parasitic elements can also change the assumed behavior of the circuit at high frequencies.

These considerations lead to certain range of frequencies where assumption of resistive behavior of PFC is valid. Derivations will be made generally on the basis of such assumption, but then only neighborhood of 60Hz will be considered for evaluating of the power factor. This is a perfectly practical condition, since line frequency is an accurate standard and conclusions are needed only in this region of frequencies.

Consider the equivalent circuit in Fig. 15.2. Assumption is made that in the frequency range of interest the PFC behaves as a resistor.

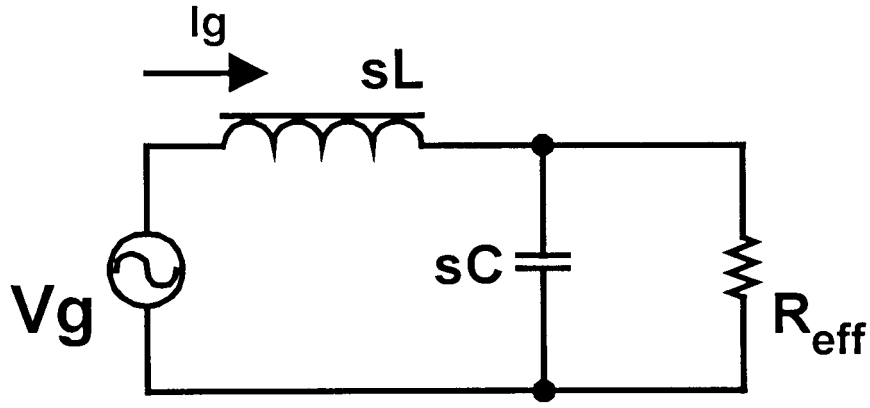

Figure 15.2: Equivalent schematic of PFC with input filter

Using (15.1) and (6.4.7) the effective resistance of the PFC R_{eff} can be expressed as (15.2) and then as (15.3), where η is efficiency, *Rload* is load resistance of PFC in Fig. 15.1 and *M(D)* is an ideal voltage gain of the converter.

$$\eta = \frac{Pout}{Pin} = \frac{VoIo}{VgIg} \tag{15.1}$$

$$R_{eff} = \frac{Vg}{Ig} = \frac{VoIo}{\eta Ig^2} \tag{15.2}$$

$$R_{eff} = \frac{1}{\eta}\frac{VoIo^2}{IoIg^2} = \frac{Rload}{\eta}\frac{1}{M(D)^2} \tag{15.3}$$

Reff, see Fig. 15.2, will be substituted by R for convenience. The input current of the circuit can then be found in complex form (15.4), and then written in usual qualities (15.5), where $\varpi_Z = 1/RC$, $\varpi_O = 1/\sqrt{LC}$, $Q = R/\sqrt{L/C}$. Related frequencies [Hz] are $f_Z = \varpi_Z / 2\pi$ and $f_O = \varpi_O / 2\pi$.

$$i_g(s) = \frac{Vg}{R}\frac{1+RCs}{1+\frac{L}{R}s+LCs^2} \tag{15.4}$$

$$i_g(s) = Ig\frac{1+\frac{s}{\varpi_Z}}{1+\frac{1}{Q}\frac{s}{\varpi_O}+\left(\frac{s}{\varpi_O}\right)^2} \tag{15.5}$$

Vg is a sine wave and constitutes as zero phase reference. The phase of the current *Ig* will therefore reflect the phase difference between input voltage and current, and power factor can be found as cosine of this phase (3.14). Power Factor can then be expressed as (15.6), for the case when quadratic term in denominator of (15.5) represents double pole.

$$PF = \cos\left(\arctan\left(\frac{f}{f_Z}\right) - \arctan\left(\frac{\frac{1}{Q}\frac{f}{f_O}}{1-\left(\frac{f}{f_O}\right)^2}\right)\right) \tag{15.6}$$

Assume the initial conditions shown in Table 15.1. Notice that these values are typical for filter which is used together with power factor correction circuit, so the

situation is very different from that described in chapter 4 where no Power Factor Correction was used.

L	*C*	*Vg*	*Pin*
1 mH	0.5 μF	100 V	100 W

Table 15.1: Initial conditions for the circuit in Fig. 15.2.

Since Vg=100 V, Pin=100 W then effective resistance R equals 100 Ohm in the area of interest. Resulting parameters are summarized in Table 15.2.

fz	*fo*	*Q*	*PF*
3.18 KHz	7.12 KHz	2.24	0.9998

Table 15.2: Parameters of the circuit in Fig. 15.2.

This estimation gives practical sense for the behavior of input current. The general case amplitude and phase of input current (15.5) are shown in Fig. 15.3. Notice that since Q>0.5, it means imaginary roots for denominator in (15.5) and related resonance characteristic in Fig. 15.3.

Practically, the capacitance of about 0.5 μF is a value used in popular power factor correctors, and will only be increased for better filtering and especially in case of higher load power, therefore only increasing the parameter Q; see Fig.15.4. Considering this, the parameter Q will still be higher than 0.5 even if L is increased up to 20mH (see Fig. 15.5), which is unusually high value for the filter inductance. Therefore, it can be

concluded, that quadratic term in denominator will have two imaginary roots, which constitutes to double pole, and is not likely split into two real poles.

Critical point corresponds to Q=0.5 condition, and double pole will just start splitting into two poles if power is increased to higher than 400 W (Fig. 15.6), or input voltage is decreased lower than 50 V (Fig. 15.7), while other conditions are kept constant.

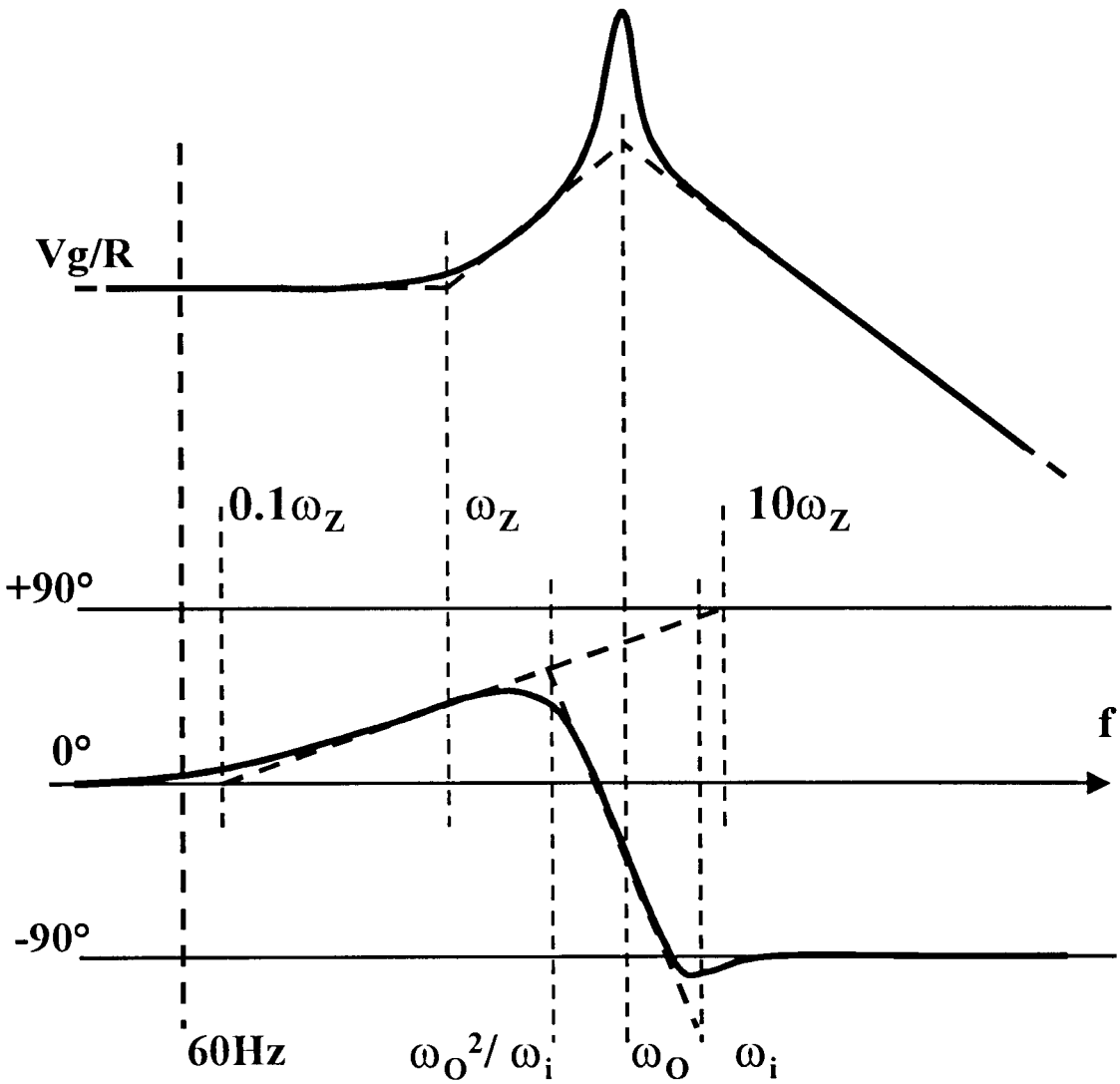

Figure 15.3: Amplitude and phase of input current Ig for circuit in Fig.15.2

Fig. 15.3 shows that double pole from quadratic term in denominator of (15.5) has no significant effect on the phase of current *Ig* at frequency 60 Hz, if it represents double pole, not two single poles. Therefore, only zero, numerator term in (15.5), defines the PF.

It is important then to check conditions under which double pole does not split to two poles and therefore starts affecting the phase at 60Hz. This condition is equal to Q=0.5 boundary. It is also logical to expect that denominator term in (15.5) will have more effect on phase of the current and therefore PF, as Q decreases towards 0.5 value. Fig. 15.5 shows that Q stays above 0.5 value for L values up to 20mH.

Change of the Q parameter with the change of input power is illustrated in Fig. 15.6. It shows that increase in power up to above 400 W will not cause a double pole to separate.

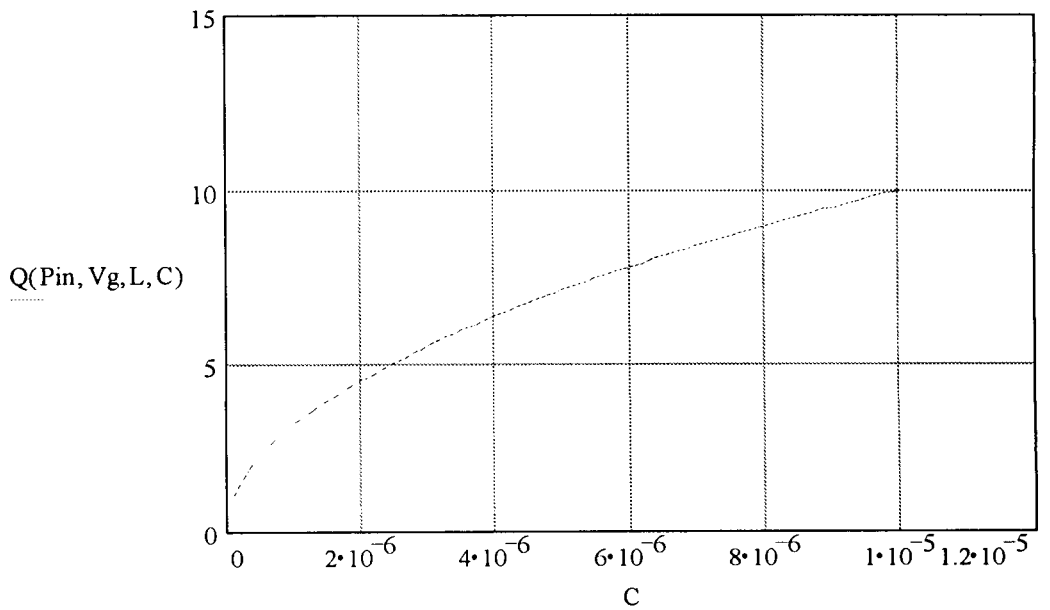

Figure 15.4: Parameter Q from (15.5) as a function of C

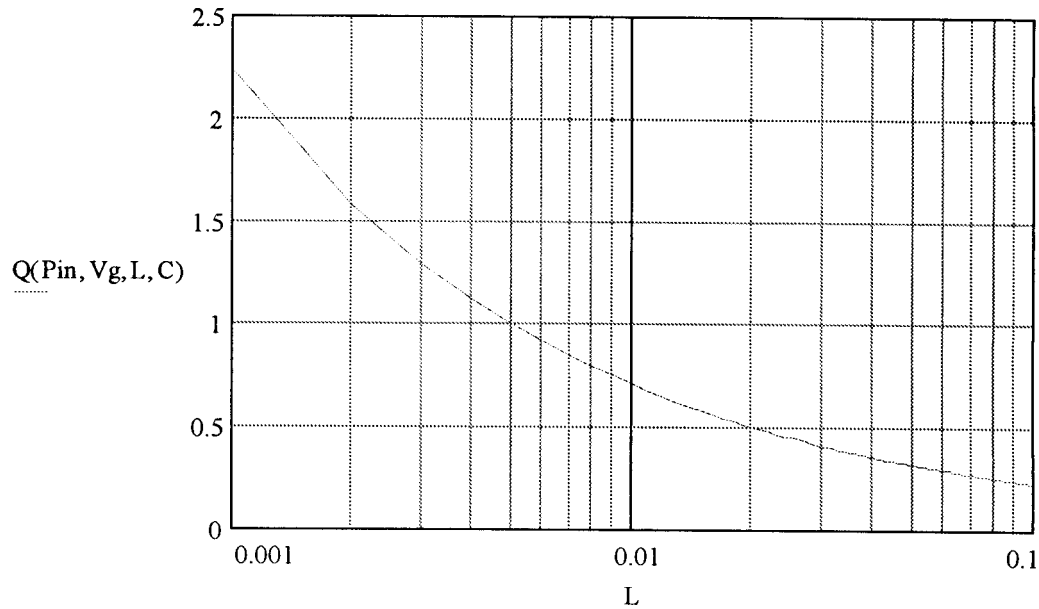

Figure 15.5: Parameter Q from (15.5) as a function of L

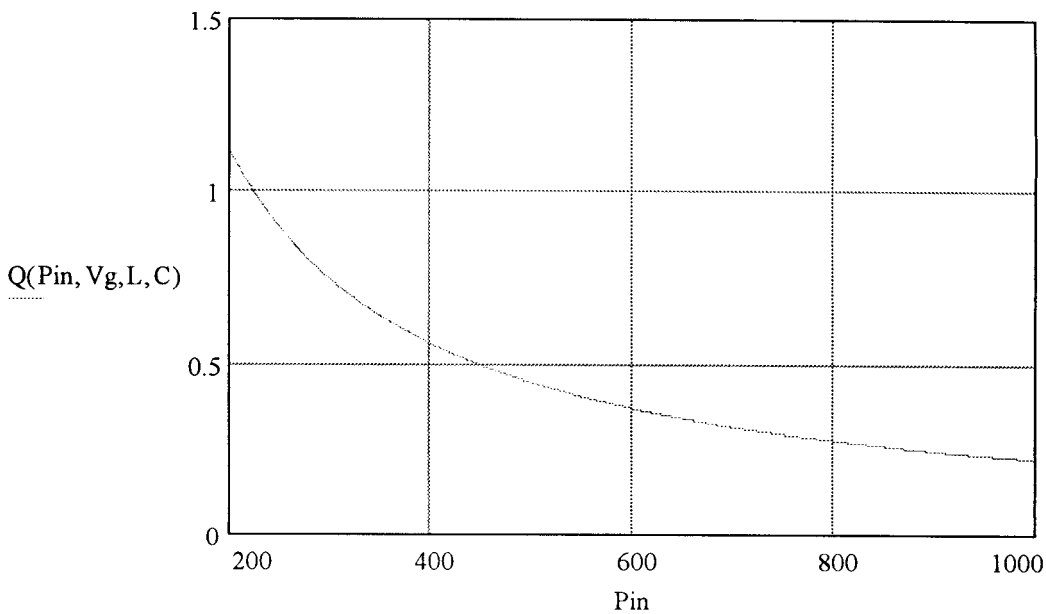

Figure 15.6: Parameter Q from (15.5) as a function of input power Pin

Decreasing Vg and therefore decreasing effective R for constant load power (100 W) will affect Q, but still keep it above 0.5 value even when input voltage drops below 50 V, Fig. 15.7.

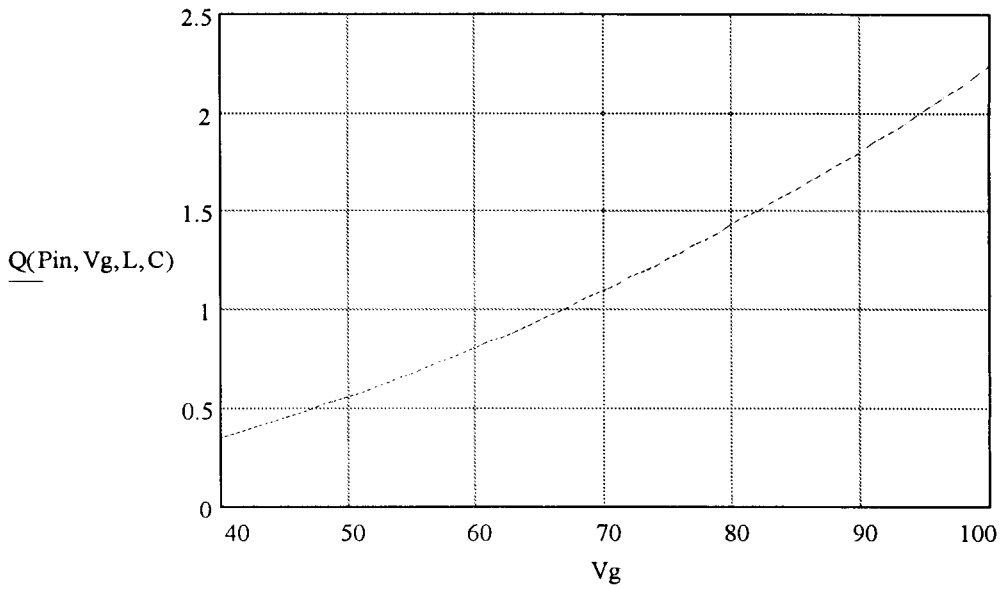

Figure 15.7: Parameter Q from (15.5) as a function of input voltage Vg

In majority of cases, when Q>>0.5, we can therefore account only phase contribution from zero in (15.5) at f=60Hz and express power factor as (15.7)

$$PF = \cos\left(\arctan\left(\frac{f}{f_z}\right)\right) = \cos(\arctan(2\pi RCf)) \qquad (15.7)$$

Now it is possible to investigate how power factor depends on circuit parameters. The convenient estimate (15.7) will be plotted together with exact expression (15.6). This approach becomes not valid when Q parameter reaches the value 0.5 so it will be indicated on the graphs.

Clearly, (15.7) does not depend on L, so as long as Q parameter is much bigger than 0.5, there is no concern about filter inductance influencing the power factor. The plot of

exact equation (15.6) is close to estimate (15.7) in Fig. 15.8 at high Q values (small L). Then it differs as L increases, so phase from double pole compensates phase of the zero, then phase of double pole dominates up to the about 20mH value of L, where Q approaches 0.5 value (see Fig. 15.5) and other equations should be used.

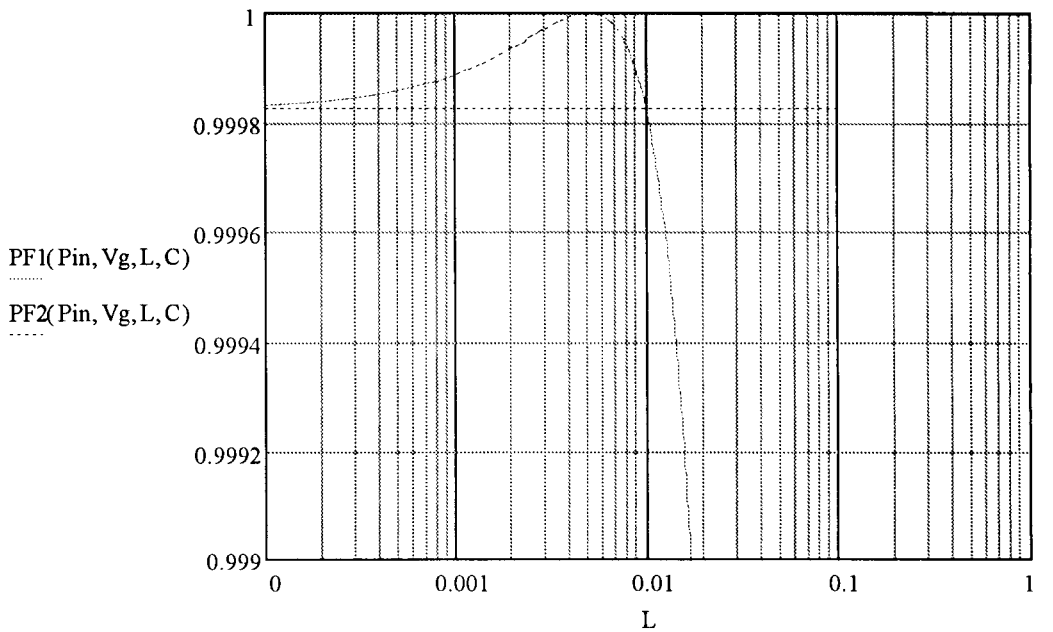

Figure 15.8: Power factor PF1 (15.6) and PF2 (15.7) as a function of L

Plot in Fig. 15.8 can be commented as low dependence of PF on L in the region of consideration. Capacitance, from the other hand, affects PF strongly, Fig. 15.9. Notice how close exact (15.6) and estimate (15.7) expressions are; it is a result of high Q values in that region of capacitance.

Since *Vg* and *Pin* change effective R, these parameters affect PF as well; see Fig. 15.10 and Fig. 15.11 respectively. Considered *Vg* range represents high values of Q (see Fig. 15.7), so in the same way as in the case of PF dependence on C, there is very close agreement between exact and estimate expressions, Fig. 15.10.

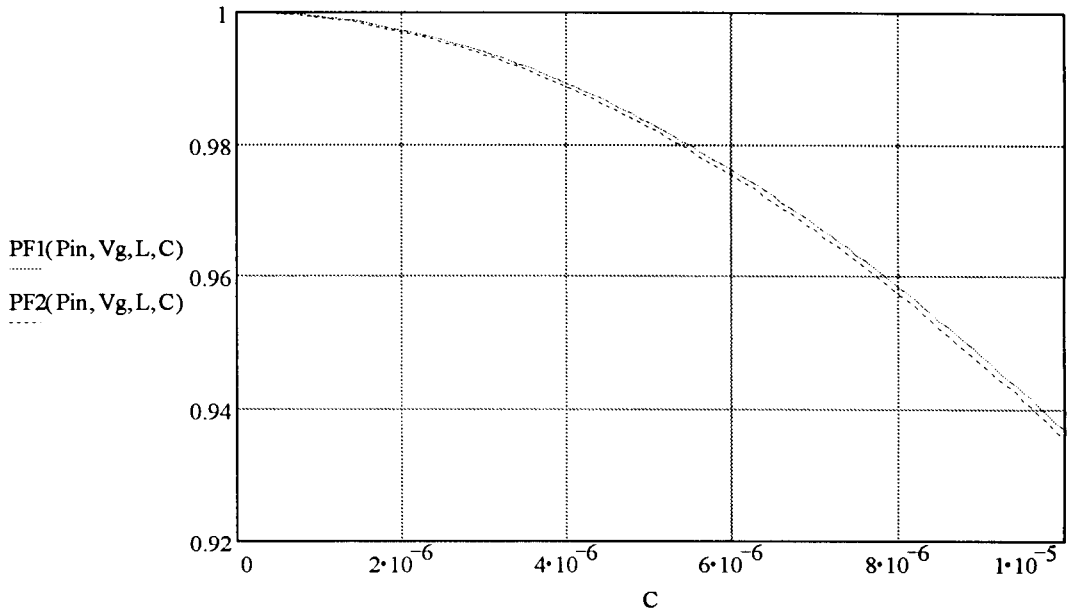

Figure 15.9: Power factor PF1 (15.6) and PF2 (15.7) as a function of C

Situation with *Pin* dependence is different, because Q value approaches 0.5 at about 450 W level. Fig. 15.11 shows that at low power (high Q) region estimate is very close to exact equation, then phase from double pole compensates phase from zero and finally dominates. At about 450 W mark the equations become not valid, since double pole splits into two single poles.

Looking at practical ranges of *Vg, Pin* and *C*, it can be concluded that the most sensitive factor that affects power factor is capacitance. This conclusion introduces a contradiction to technological preference of decreasing inductance value of the filter and related increasing of the capacitance.

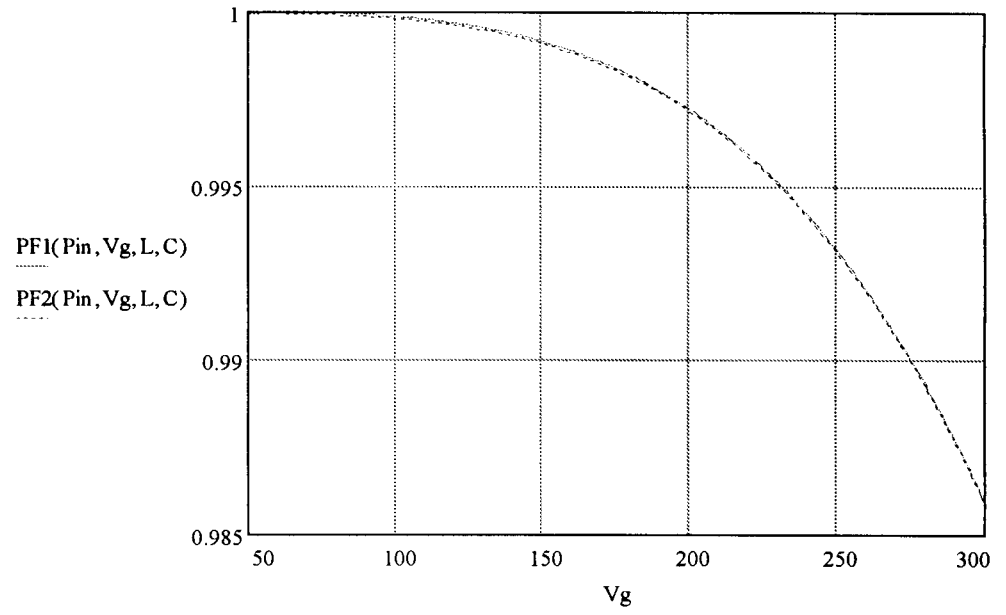

Figure 15.10: Power factor PF1 (15.6) and PF2 (15.7) as a function of Vg

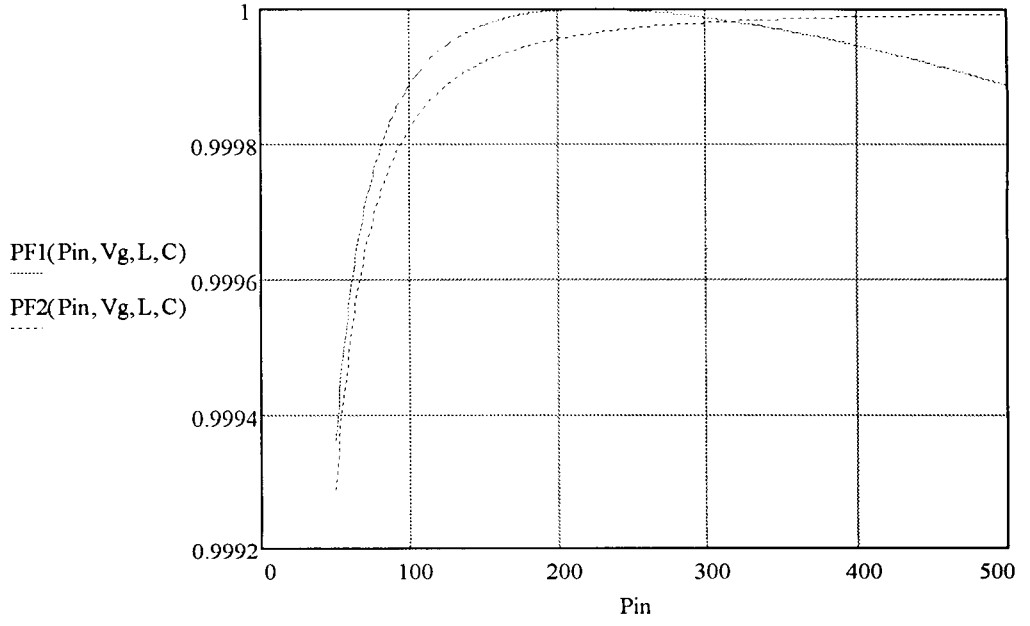

Figure 15.11: Power factor PF1 (15.6) and PF2 (15.7) as a function of Pin

Now the less likely case when $Q<0.5$ will be considered. From previous analysis it is known that to decrease Q: L value should be increased, C value and effective resistance value R decreased. Latter means decreasing Vg and increasing input power Pin of the circuit. The following initial conditions, similar to the approach presented in Table 15.1, are presented in Table 15.3.

L	*C*	*Vg*	*Pin*
5 mH	0.5 μF	85 V	500 W

Table 15.3: New initial conditions for the circuit in Fig.15.2.

These initial conditions lead to circuit parameters shown in Table 15.4. Increased power level resulted into low value of effective resistance, which pushed the zero corner frequency f_Z to much higher range. Two pole corner frequencies appeared, f_1 and f_2 instead of double pole frequency f_O. Q value is below 0.5 as expected. The value of PF is clearly defined by the closest pole at f_1.

f_Z	F_1	f_2	*Q*	*PF*
22.0 KHz	149.6 Hz	6.86 KHz	0.144	0.929

Table 15.4: New parameters of the circuit in Fig.15.2.

Equation (15.5) has two real roots in denominator now and can be interpreted as (15.8) (under condition that $Q<0.5$)

$$i_g(s) = Ig \frac{1 + \frac{s}{\varpi_Z} s}{\left(1 + \frac{s}{\varpi_1}\right)\left(1 + \frac{s}{\varpi_2}\right)} \tag{15.8}$$

Two separate poles are described with ϖ_1 and ϖ_2, or f_1 and f_2; see (15.9) and (15.10) respectively.

$$f_1 = \frac{f_O}{2Q}\left(1 - \sqrt{1 - 4Q^2}\right) \tag{15.9}$$

$$f_2 = \frac{f_O}{2Q}\left(1 + \sqrt{1 - 4Q^2}\right) \tag{15.10}$$

If Q<<0.5, then further simplification can be done as (15.11) and (15.12), where $f_O = \varpi_O / 2\pi = 1/\left(2\pi\sqrt{LC}\right)$.

$$f_1 \approx f_O Q \tag{15.11}$$

$$f_2 \approx \frac{f_O}{Q} \tag{15.12}$$

Intuitively, now the new pole with lower corner frequency f_1 will have influence at 60Hz. The other pole at higher frequency f_2 will not contribute anything. Power factor is then found as (15.13), or expressed in initial circuit parameters as (15.14).

$$PF = \cos\left(\arctan\left(\frac{f}{f_Z}\right) - \arctan\left(\frac{f}{f_1}\right)\right) \tag{15.13}$$

$$PF = \cos\left(\arctan(2\pi RCf) - \arctan\left(\frac{f}{\frac{f_O}{2Q}\left(1 - \sqrt{1 - 4Q^2}\right)}\right)\right) \tag{15.14}$$

Now evaluation of PF at $Q<0.5$ condition will be done. Notice that mentioned condition has to be checked to validate the used equations.

Fig. 15.12 shows that under conditions in Table 15.3 the Q value stays lower than 0.5 up to the point when capacitance is increased to about 6 μF. PF dependence on the value of C is illustrated in Fig. 15.13.

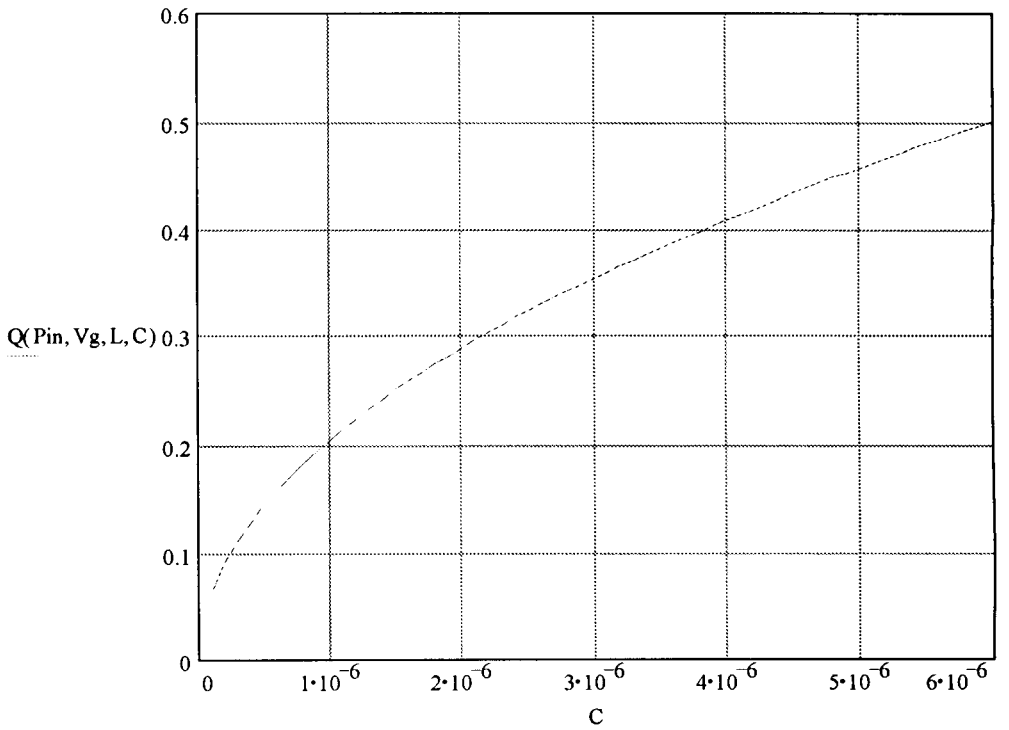

Figure 15.12: Parameter Q from (15.5) as a function of C

Not expected at first sight increasing of PF with increasing of C, Fig. 15.13, can be explained as follows: the dominating factor in (15.13) is contribution from pole at f_1. As capacitor value increases, this pole moves to higher frequencies, lowering the phase shift at 60Hz and therefore increasing the PF value. Although pole at f_Z moves to lower frequencies at the same time, it is too far away from 60Hz and does not have significant effect.

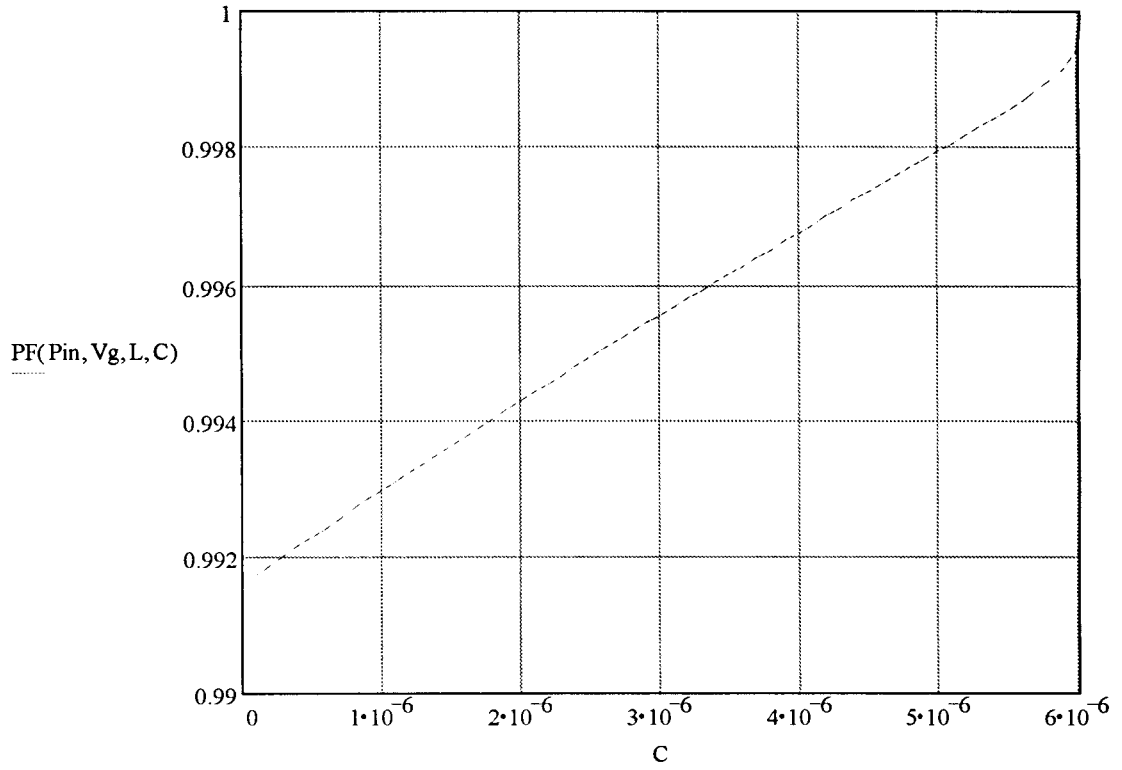

Figure 15.13: Power factor PF (15.13) as a function of C

Fig. 15.14 shows that zero *Fz* stays at high frequencies (away from 60Hz) as *C* changes, so does the second pole *F2*. The contribution from first (low frequency) pole *F1* dominates the phase, and this pole shifts to higher frequency as C increases, improving PF value on the contrary to intuitive expectations. Notice that (15.15) can be derived from (15.9) and (15.10).

$$f_o^{\,2} = f_1 f_2 \tag{15.15}$$

Fig. 15.14 illustrates how (15.15) holds and how f_1 and f_2 collapse together into f_o as parameter Q reaches 0.5 value at about 6 μF value, Fig. 15.13.

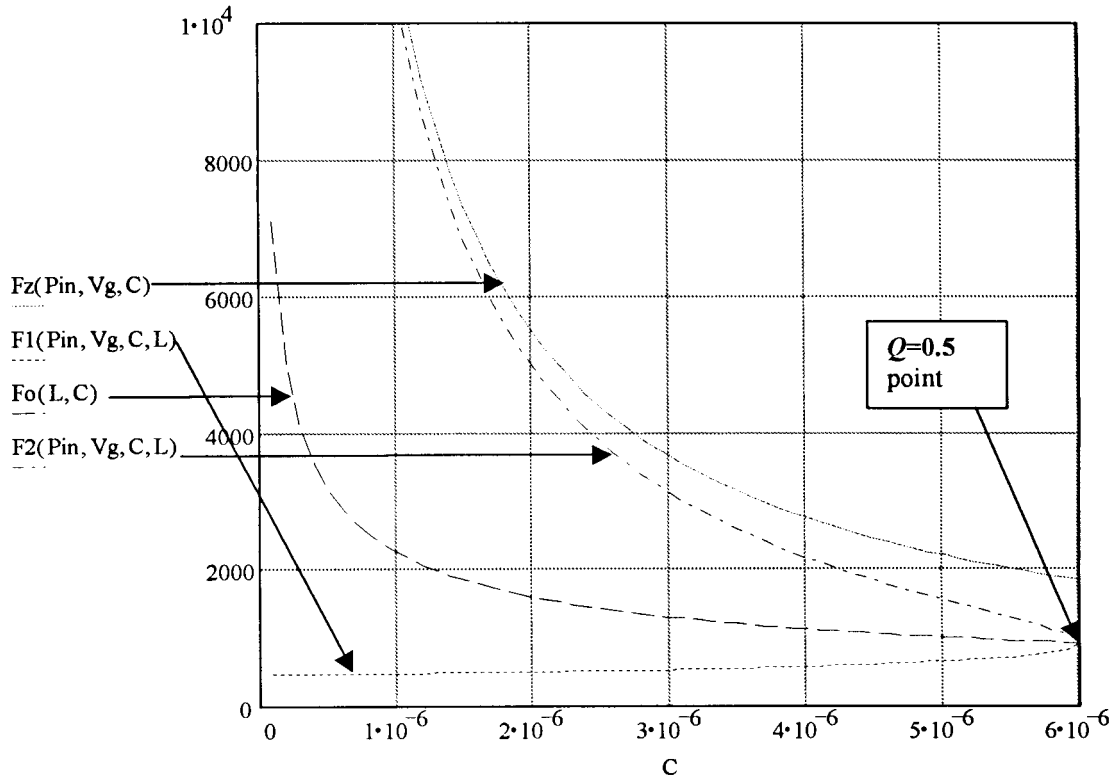

Figure 15.14: Frequencies of zero Fz, 1st pole F1, 2nd pole F2, and frequency Fo

It can be expected that L will have significant effect on PF as well. Fig. 15.15 shows that condition Q<0.5 is satisfied for L values as low as 0.4mH and other parameters as in Table 15.3.

Fig. 15.16 demonstrates that increasing L degrades PF value strongly, and the reason is that most important pole (with frequency closest to 60 Hz) at f_1 moves to lower frequencies as L increases.

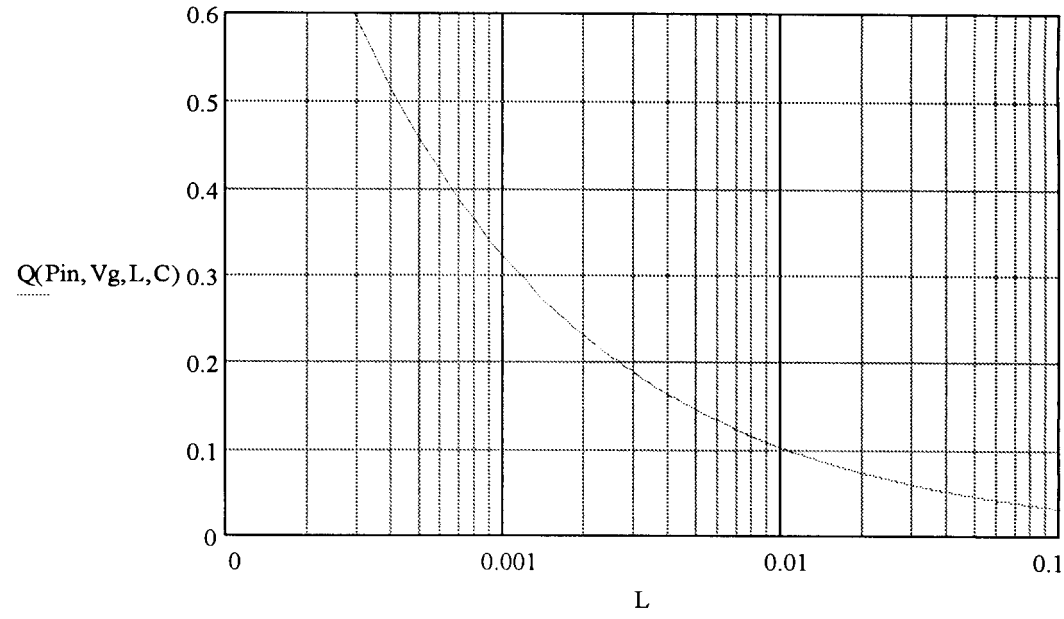

Figure 15.15: Parameter Q from (15.5) as a function of L

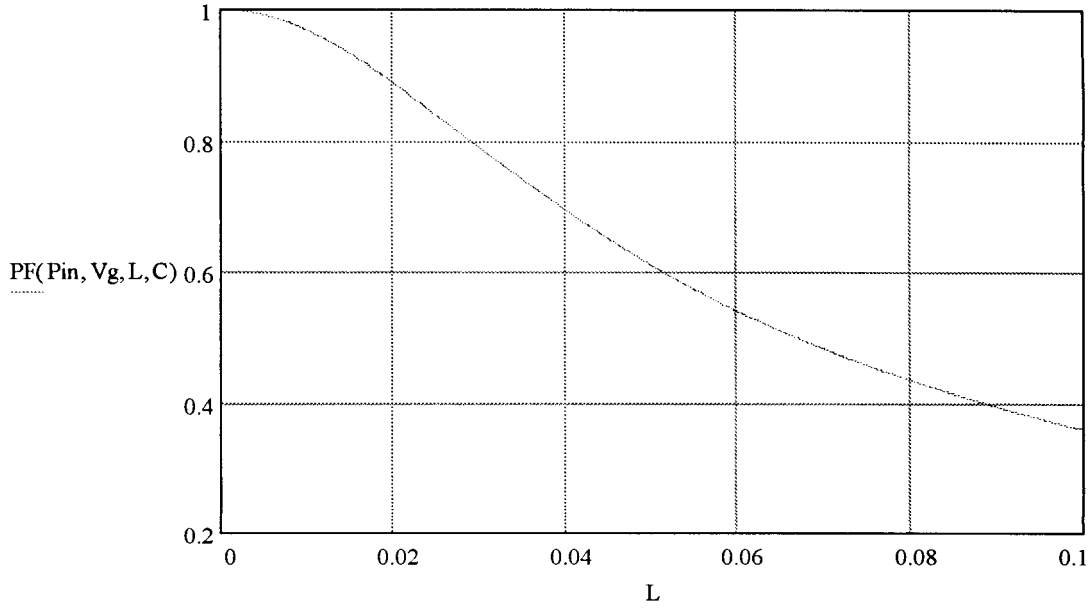

Figure 15.16: Power factor PF (15.13) as a function of L

Changing Vg will result in change of the value of effective resistance R, which will affect pole at f_1 and therefore PF, especially at low Vg where change will be most significant. Fig. 15.17 shows that voltage can go up to about 160 V to still have $Q<0.5$. Fig. 15.18 displays the related PF value.

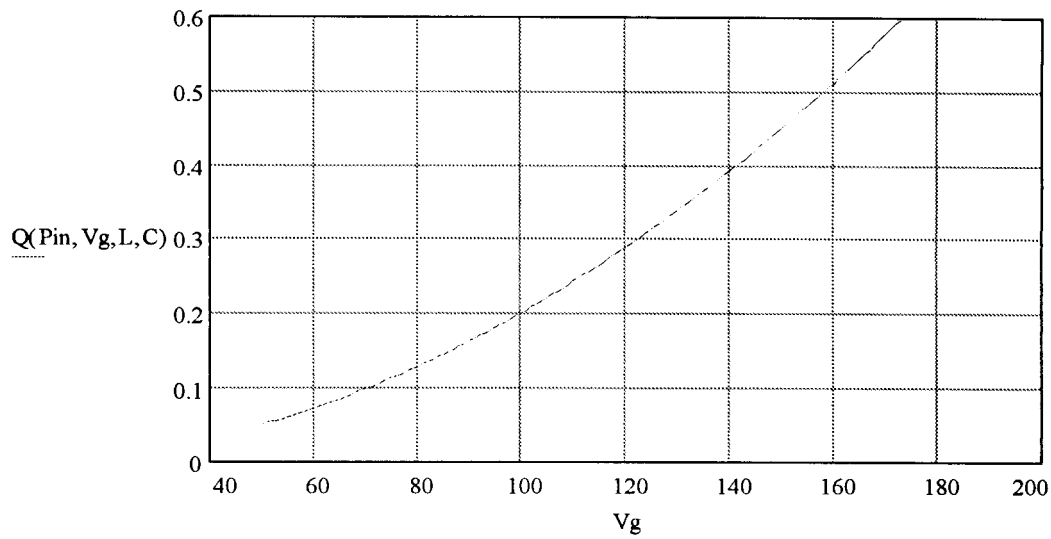

Figure 15.17: Parameter Q from (15.5) as a function of Vg

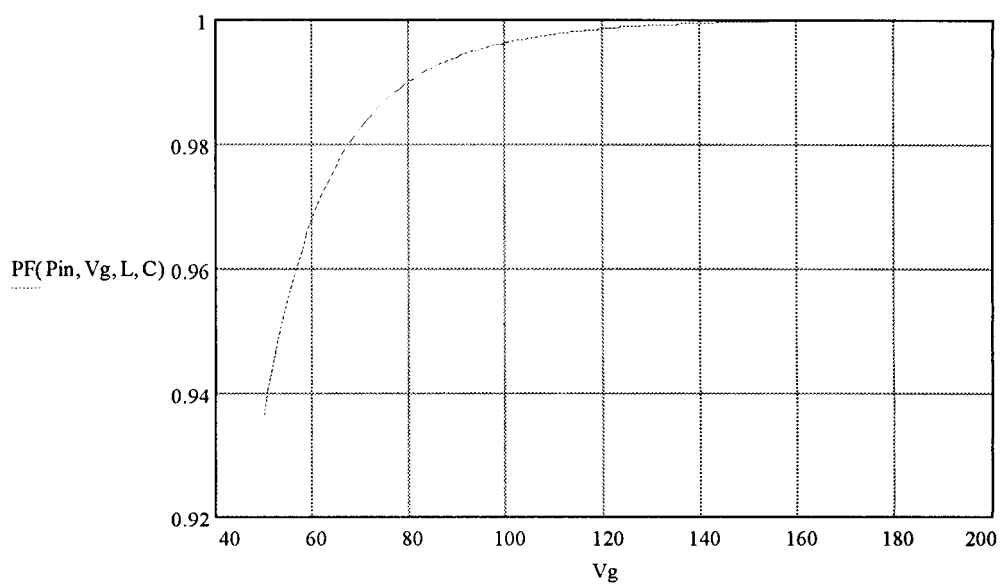

Figure 15.18: Power factor PF (15.13) as a function of Vg

As *Vg* increases f_1 goes up, see Fig. 15.19, and therefore PF increases. Fig. 15.19 explains increasing of PF value as *Vg* increases since the critical pole at low frequency f_1 moves up, similar to the discussed case when *C* was increased.

Changing *Pin* also causes the value of effective resistance *R* to change as *Vg* does. The parameter *Q* stays below 0.5 value with power dropping to about 150 W level, Fig.15.20.

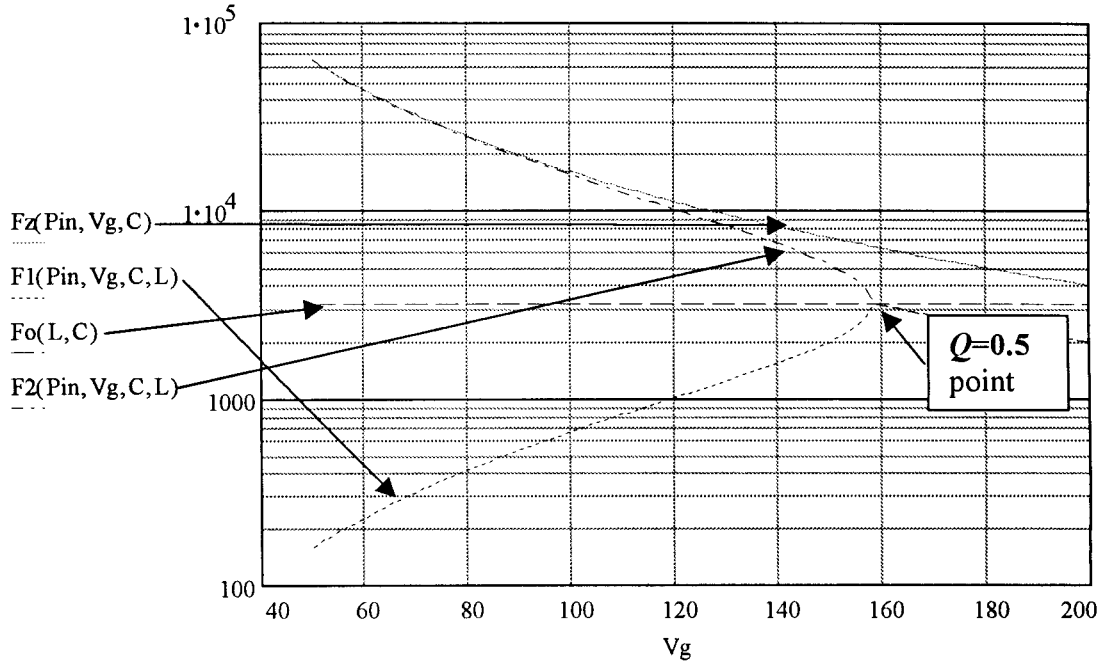

Figure 15.19: Frequencies of zero Fz, 1st pole F1, second pole F2, and frequency Fo

Fig.15.21 shows that PF degrades as *Pin* is increased, which is expected because effective *R* decreases. This effect is similar to decreasing of *Vg*, which was discussed above.

Notice that power of several hundred watts is rather usual range for power products and Fig.15.21 shows that PF degrades significantly. However, the other parameters have uncommon values as it was stated for this case of low *Q* values. There is no guarantee

though that by some reasons the value of Q would not decrease to below 0.5 in real circuitry under some conditions.

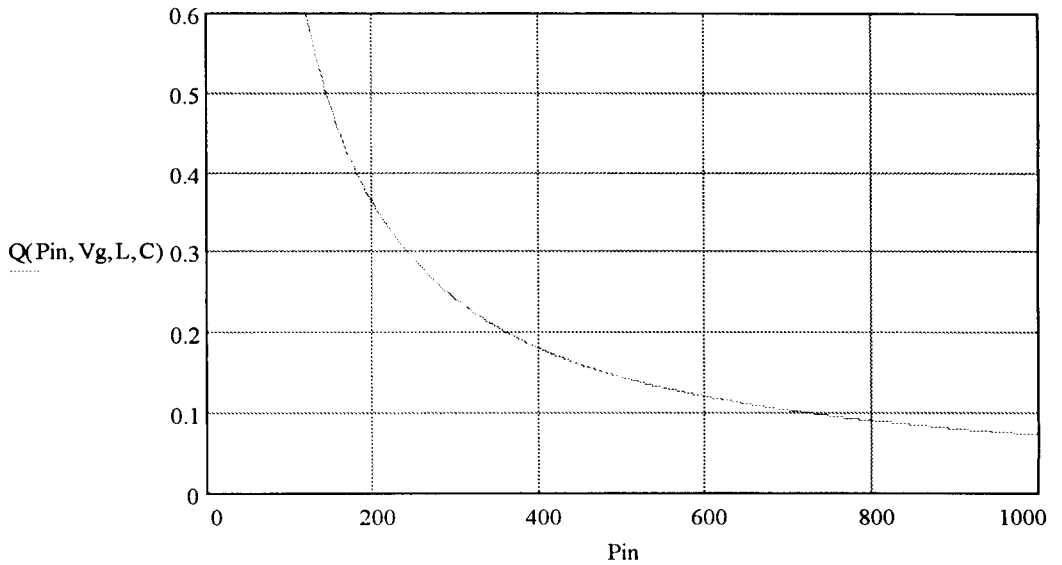

Figure 15.20: Parameter Q from (15.5) as a function of Pin

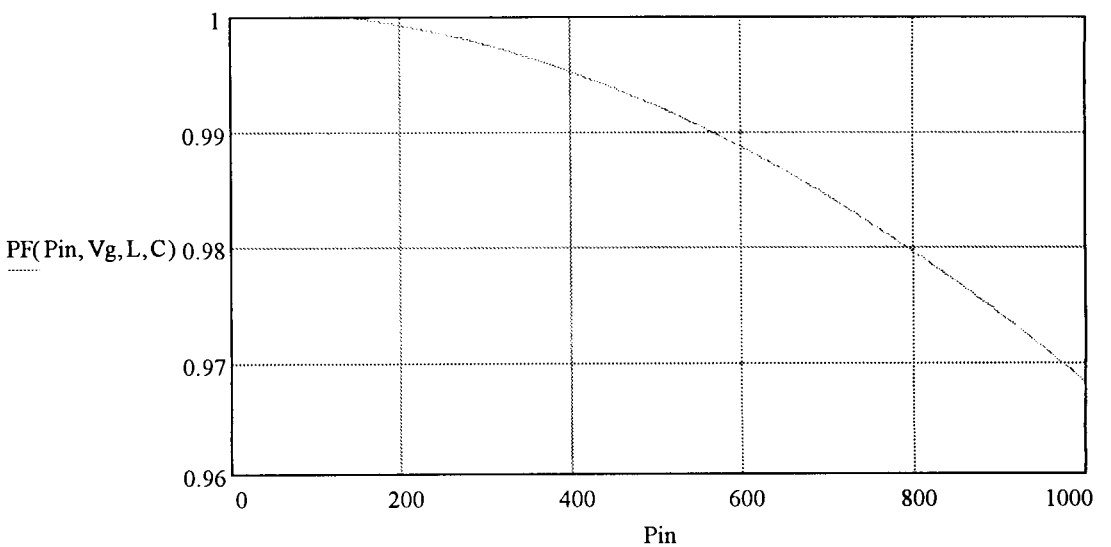

Figure 15.21: Power factor PF (15.13) as a function of Pin

After considerations of PF dependence on different circuit parameters, the following general comments can be made. The most common case is when input current characteristic has a zero and a double pole - in this case zero is more critical to the power factor value. This zero is defined by value of the filter capacitance and effective resistance.

Considering trend to increase the value of the capacitance (and decrease the inductance value), Q parameter is likely to increase even further which leads to preserving a double pole in the input current characteristic.

Most sensitive parameter for the PF is capacitor value C; see Fig.15.9. Input voltage and load power also affect the PF since they affect the effective resistance value and therefore position of the zero. The dependence on *Pin* is more important if circuit parameters lead to splitting of the double into two separate poles. Increasing inductance lead exactly to the mentioned condition (opposite effect in comparison to increasing of the capacitance). Relatively big values of inductance degrade PF significantly, see Fig. 15.15. However, these values are not practical and are less likely to be chosen for the filter inductance.

Having established the undesirable effects of the input filter on the PF value, it is now possible to investigate the options of PF improvement, which are enabled by the absence of the input rectification. The considerations will be shown in the following chapter.

Chapter 16

Including Input Filter into PFC Operation in Bridge-less Converters

New converters without input rectification enable beneficial opportunities to include input filter into power factor correction. It will be shown that these converters allow to correct power factor right before the input filter, not after as in conventional topologies, therefore improving overall performance. This feature also significantly lowers discussed restriction on increasing capacitance value and decreasing the value of inductance in the input filter.

16.1 Equivalent Schematics and Analysis

Two issues need to be considered independently. First, the input voltage sense for the control circuitry can be implemented directly on input voltage source avoiding any influence of input filter. Second, the controlled current, which has to follow input voltage waveform for Power Factor Correction, can be now chosen not as input current of the power stage, but rather as input current of the PFC including the input filter. In other words, the controlled current can be chosen as the current from input voltage source directly.

These issues will be considered separately, although practical implementation can include any variations of connections and control methods.

Consider the connection of the input voltage sense as in Fig. 16.1. The loaded power stage is now approximated not as just equivalent resistance, but as voltage dependent

current source, controlled by V_C in a form of $\frac{\alpha V_C}{R}$. Notice that if sense terminals of this source are shorted to current source itself, it will be exactly the case of two terminal resistive element that was used the case in previous chapter.

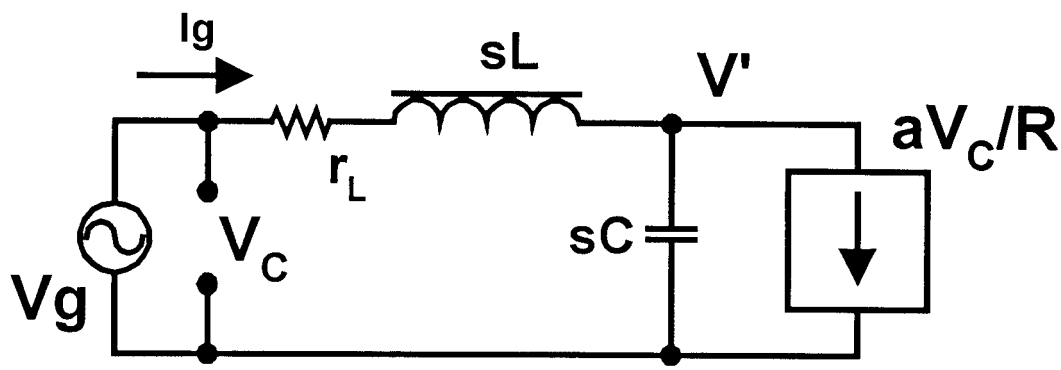

Figure 16.1: Simplified schematic of input voltage sense connection in new PFC

All general comments and assumption used above are used here as well. The characteristics will be derived in somewhat wide frequency range; however, only f=60Hz is the point of interest and used models will not be valid at higher frequencies as it was discussed in chapter 15. Resistance r_L is introduced for the reason, which will be clear later. This relatively small resistance is always present as parasitic element in filter inductance. The ratio $r_L << R$ can be established, where R is an effective resistance of the loaded power stage.

The following equations can be written for the circuit in Fig. 16.1:

$$i_g = \frac{v_g - v'}{sL + r_L} \tag{16.1}$$

$$i_g = \frac{v'}{1/sC} + \frac{\alpha v_g}{R} \tag{16.2}$$

Notice that the current of dependent current source is expressed as $\frac{\alpha v_g}{R}$. Basically, it introduces the same equivalent resistance R as in previous chapter, and it establishes that phase of that current is exactly as the phase of input voltage v_g is. The coefficient α represents the fact that effective resistance R depends on magnitude of the voltage v' (and load power), not v_g. Practically, this coefficient is very close to 1, at least because it does not make any sense to use an input filter that decreases the input voltage so power stage has to work in unusual conditions. This would be very bad in terms of efficiency, in terms of the phase shift introduced by the filter, and in terms of vary big values and therefore size of the filter components. Assumption of parameter α being close to 1 is therefore a very valid one.

(16.1) and (16.2) can be solved for input current i_g in a complex form, and the result is shown as (16.3). The result is then written in usual qualities (16.4), where $Ig = \frac{\alpha Vg}{R}$, $\varpi_Z = \alpha / RC$, $\varpi_O = 1/\sqrt{LC}$, $Q = \sqrt{L/C}/r_L$. Related frequencies [Hz] are $f_Z = \varpi_Z / 2\pi$ and $f_O = \varpi_O / 2\pi$.

$$i_g(s) = \frac{\alpha Vg}{R} \frac{1 + \frac{RC}{\alpha} s}{1 + r_L Cs + LCs^2} \tag{16.3}$$

$$i_g(s) = Ig \frac{1 + \frac{s}{\varpi_Z}}{1 + \frac{1}{Q}\frac{s}{\varpi_O} + \left(\frac{s}{\varpi_O}\right)^2} \tag{16.4}$$

As before, Vg is a sine wave and constitutes as zero phase reference. The phase of the current i_g will therefore reflect the phase difference between input voltage and current, and power factor equals the cosine of that value.

The general result (16.4) is identical to previous case (15.5). Notice that "plateau" current Ig in (16.4) differs from the same quantity in (15.5) by the factor of α. This fact, connected to amplitude difference between v_g and v', is nothing else but the accounting of the extra voltage drop across r_L, which should be small. New frequency of zero f_Z is also different from previous case, but very slightly, since parameter α is close to 1.

The general equation (16.4) is the same as (15.5) in previous case, and parameters Ig, ϖ_Z and ϖ_O are very close to ones in (15.5) or the same. Parameter Q is quite different, though it is $Q = \sqrt{L/C}/r_L$ instead of $Q = R/\sqrt{L/C}$. In the previous case it could be observed that practically the effective load resistance R has usually higher value than characteristic resistance of the second order system $R_O = \sqrt{L/C}$. The values of Q were plotted for detailed analysis. In the current case it can be expected that since r_L is a parasitic element, which is kept as low as possible, the ratio $\sqrt{L/C}/r_L$ is expected to be higher than 0.5 in practical conditions, in fact much higher.

Assumptions for initial values for the circuit elements in Fig. 16.2 are shown in Table 16.1. The value of L is chosen 0.5 mH instead of 1mH, because the trend of decreasing L and increasing C will be explored later and capacitance value will be pushed very high for the experiment purposes. Resulting parameters of the circuit in Fig.16.1 are shown in Table 16.2. The value of r_L was accounted as 0.08 Ohm, which is the parasitic resistance of the filter inductance, but 0.25 Ohm was added, which includes the value of current

sensing resistor. The choice of the r_L value depends on connection of the current sensing resistor and capacitor and will be considered later. Two related values of Q are shown.

L	R_L	*C*	*Vg*	*Pin*
0.5 mH	0.08/0.33 Ohm	0.5 μF	100	100

Table 16.1: Initial conditions for the circuit in Fig.16.1.

F_Z	f_O	*Q*	*PF*
3.18 KHz	7.12 KHz	395/96	0.9998

Table 16.2: Parameters of the circuit in Fig.16.1 under conditions from Table16.1.

Notice the very high value of Q in both cases of r_L values. Now, the dependence of the parameter Q on the values of new circuit elements can be investigated.

Basically, the case of voltage sense "before" the filter is very close to the case of voltage sense "after" the filter, considered in chapter 15. Frequencies and amplitudes differ not significantly in (15.5) and (16.4) except the values of Q parameter. This implies that splitting of the double pole in denominator of (16.4) to two single poles is even less likely than in (15.5).

Fig. 16.2 shows dependence of Q on the value of the capacitance C. The value stays way above 0.5 for r_L=0.08 Ohm (*Q1* curve) as well as for r_L=0.33 Ohm (*Q2* curve).

Prediction of the power factor is shown in Fig.16.3 and is calculated as (15.6) since the (16.4) has the same general structure as (15.5).

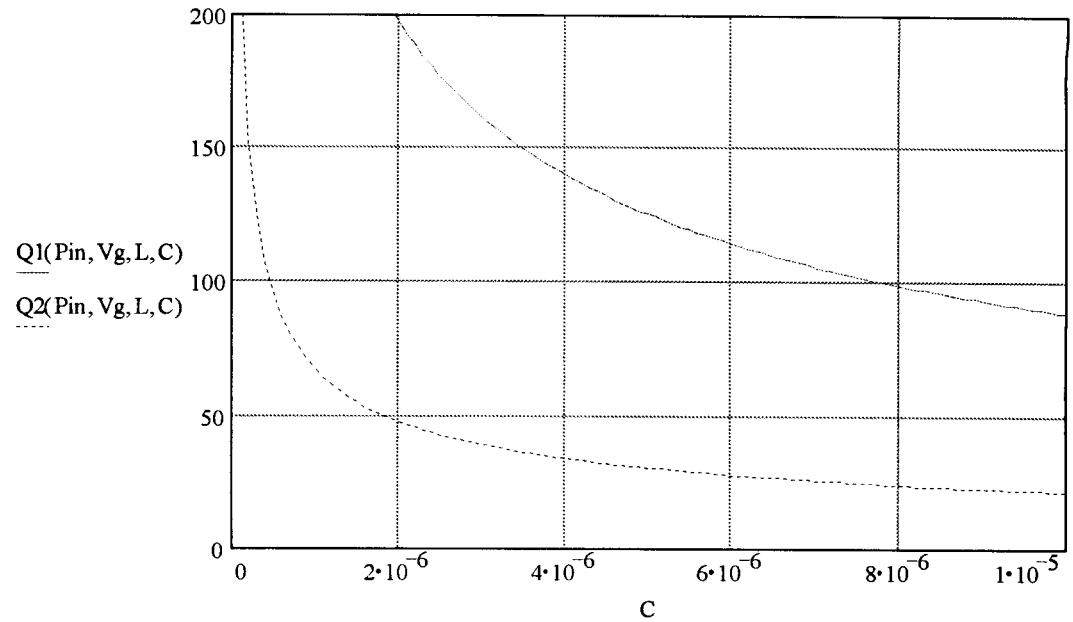

Figure 16.2: Parameter Q from (16.4) as a function of C: Q1(r_L=0.08), Q2(r_L=0.33)

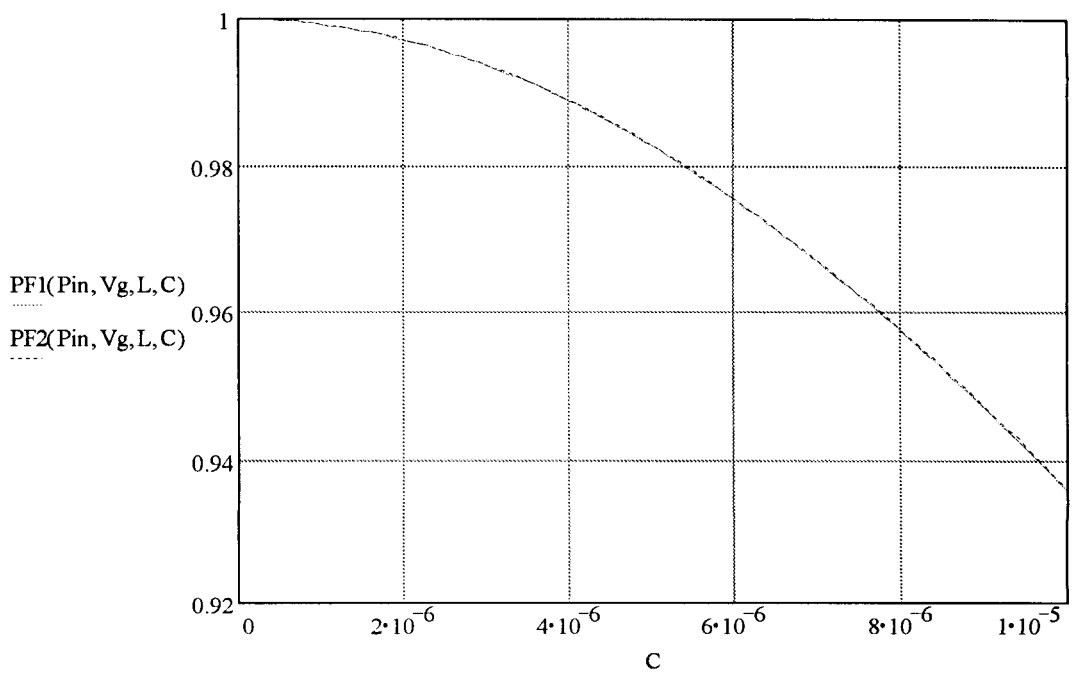

Figure 16.3: Power factor (15.6) as a function of C: PF1(r_L=0.08), PF2(r_L=0.33)

The value of Q parameter does not influence the zero in denominator of (16.4), so power factor does not depend on Q value as long as it stays above 0.5, and therefore the choice of r_L is also unimportant for PF value.

Changing L in a wide range keeps the value of Q well above 0.5, and since L does not affect the frequency of zero $f_Z = \varpi_Z / 2\pi$, the power factor does not depend on L in this case.

Increasing the input power will decrease the value of effective resistance R and therefore move zero at $f_Z = \varpi_Z / 2\pi$ up, increasing the power factor value, Fig.16.3. This result is expected.

Input voltage Vg has related effect – increasing Vg would increase effective R and therefore decrease the value of power factor, Fig. 16.4.

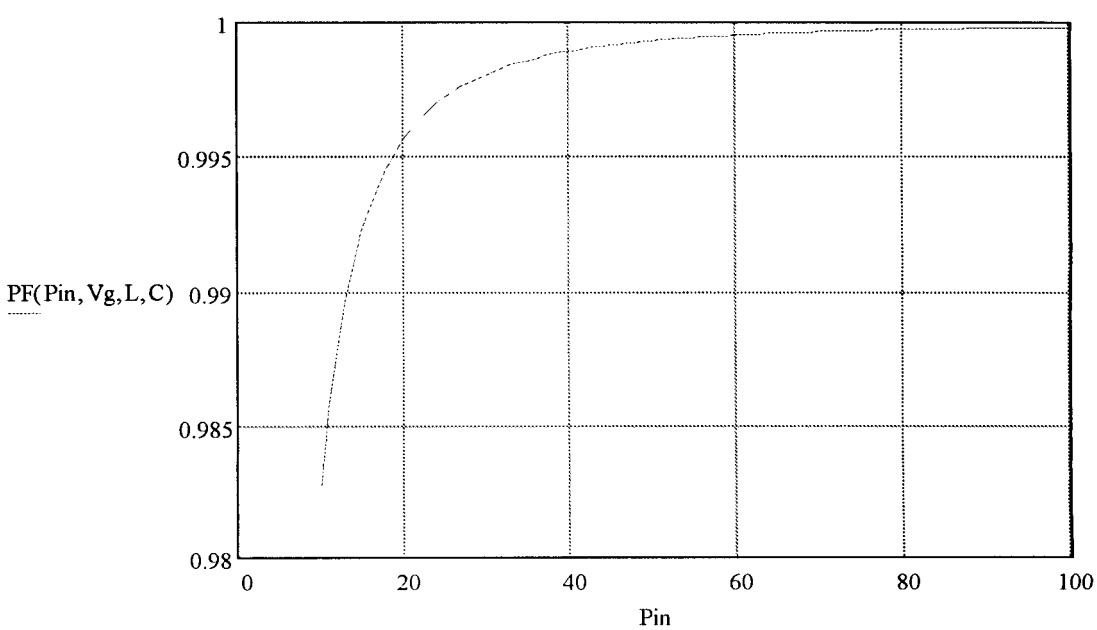

Figure 16.3: Power factor (15.6) as a function of Pin

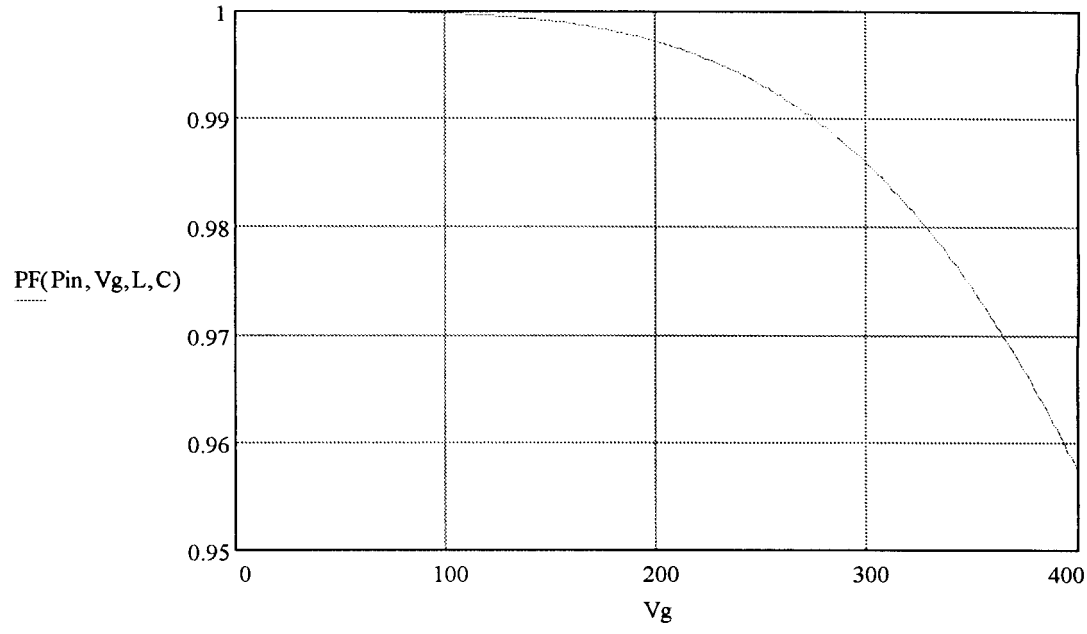

Figure 16.4: Power factor (15.6) as a function of Vg

The most interesting is a plot of power factor as a function of C. It was established previously that power factor is sensitive to capacitance value, and technological trend is such that this value tends to be increased decreasing used filter inductance.

16.2 Experimental Verification and Data

Fig.16.5 shows the experimental data for the power factor *PFconv* when voltage sense is implemented after the filter, experimental data *Pfnew* when input voltage is sensed before the filter (right on the voltage source), and theoretical fit *PFpr*.

The ideal prediction of PF as (15.6) differs from the data; however, the following consideration was done.

Effective value of R was used for assumptions and calculations. However, the power stage is not a resistor, but a rather complex system with a feedback. Control chip always

has some finite accuracy and an offset, delays, etc. Even sense of input voltage has *RC* filter, which therefore leads to some delay in the control circuit. This delay is designed to be negligible or not critical for power factor correction. However, all these factors lead to some extra phase in input current, which can be approximated by some constant θ and power factor is then represented as (16.5).

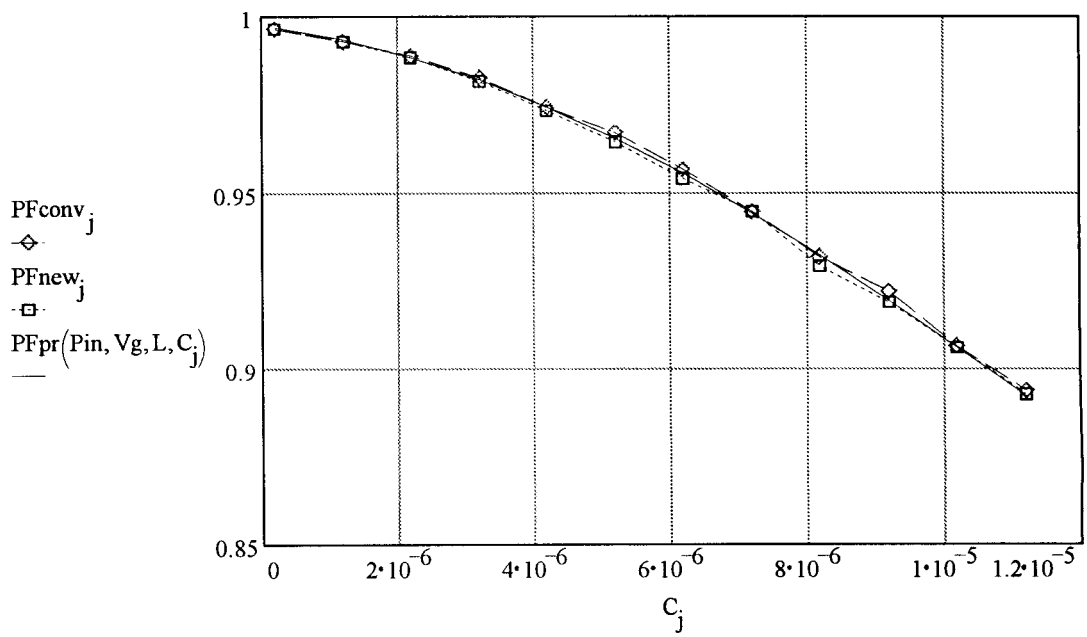

Figure 16.5: Power factor as a function of C

$$PF = \cos\left(\arctan\left(\frac{f}{f_z}\right) - \arctan\left(\frac{\frac{1}{Q}\frac{f}{f_o}}{1-\left(\frac{f}{f_o}\right)^2}\right) + \theta\right) \tag{16.5}$$

Main factor is a zero $f_Z = \varpi_Z / 2\pi$ in the denominator of (16.4). Practically, the constant θ allows very accurate correction of ideal equation. The value 0.07 for the θ parameter allows a perfect fit in Fig. 16.5.

Fig. 16.5 shows that in fact there is no improvement of power factor under normal practical conditions if voltage sense is moved from "after" the filter to the very voltage source. Only noise sensitivity can be gained this way, not the power factor value. This somewhat unexpected result can be explained by the fact that voltage at the input of the power stage (after the filter - v' in Fig. 16.1) does not have any significant phase shift in comparison to the voltage in the input source v_g. So the current of the power stage will follow necessary shape in any way of connection of the voltage sense. In this case additional current through input filter capacitance, which has definite phase shift from applied voltage, degrades power factor.

Consider now controlling the input current right from the voltage source – before the input filter, Fig. 16.6. Power factor correction then includes any currents that might be in the filter capacitors and therefore highest possible power factor is achieved. Only control issues and characteristics of used integrated circuits limit the value of PF in such arrangement.

The PF dependence on the capacitance is definitely the most interesting. However, L and C now introduce a double pole (with high Q) for the current sense, Fig. 16.6. Extra phase can make control unstable, and therefore values up to 10 μF as in Fig. 16.5 could not be repeated without extra compensation. Values of 10 μF order are not realistic though, so data taken in 1 μF range can be considered practical.

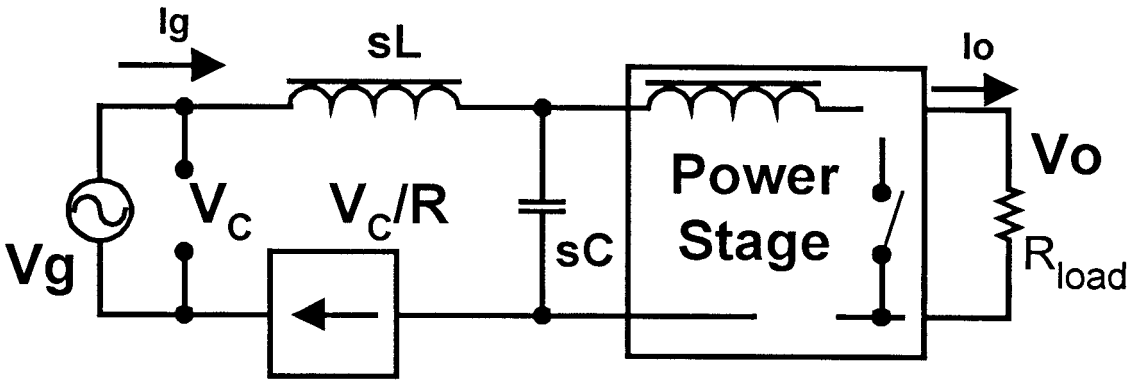

Figure 16.6: Including input filter into PF correction in new PFC

Table 16.3 shows initial conditions for the circuit in Fig. 16.6.

L	R_L	*C*	*Vg*	*Pin*
0.5 mH	0.08/0.33 Ohm	0.2-1.3 μF	85	80

Table 16.3: Initial conditions for the circuit in Fig.16.6.

Fig. 16.7 shows the detailed schematic of the experiment. Capacitors C_{f1} and C_{f2} were set at 0.1 μF initially to have the circuit operational. Then capacitor C_{f1} was increased in steps to take measurements for conventional case, and second set of data was achieved by measurements of PF while C_{f2} was increased in steps. Data sets therefore both start from 0.2 μF value.

Fig. 16.8 shows the experimental data for the power factor *PFnew* when power factor correction is implemented before the filter (as in Fig. 16.6), experimental data *PFconv* when power factor correction is implemented in traditional way (after the input filter), and theoretical fit *PFpr* for the traditional case.

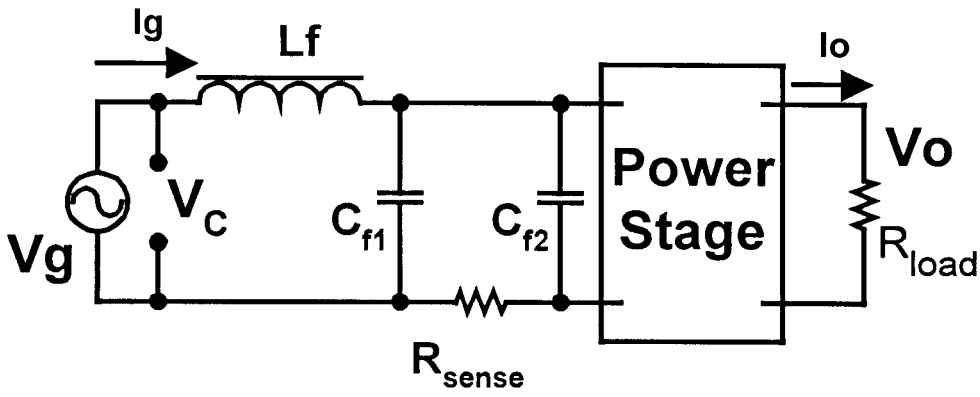

Figure 16.7: Experimental schematic for different connection of the filter

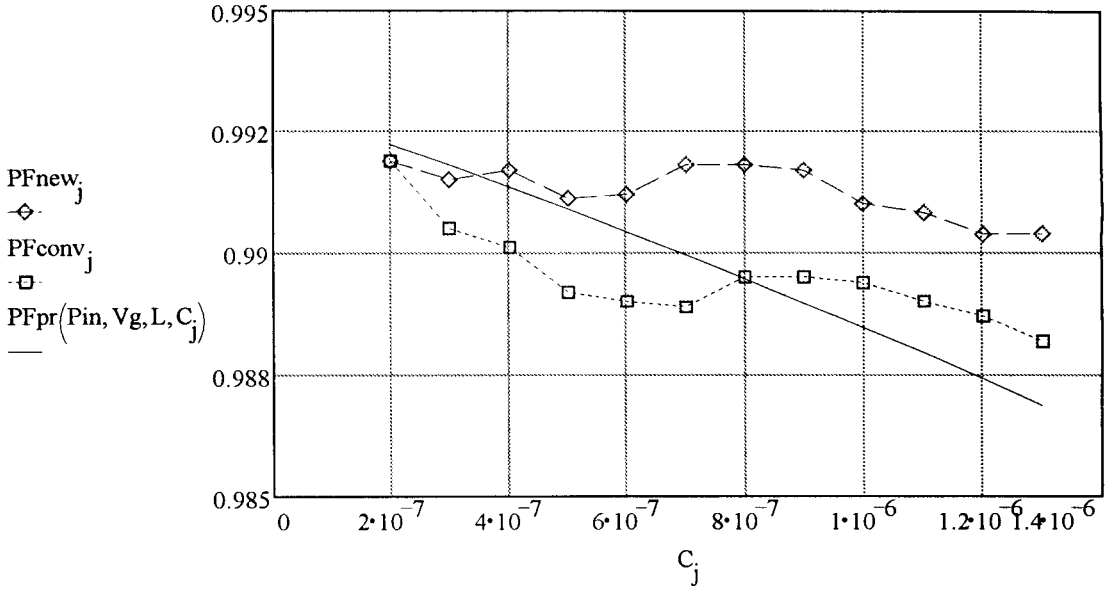

Figure 16.8: Power factor as a function of C, new approach Pfnew, conventional approach Pfconv and theoretical fit PFpr

PF value turns out to be sensitive to change in input and output voltage, so data in Fig. 16.8 clearly has some error margins in it. The data shows, though, that PF value is

improved when input filter is included into PF correction. As capacitance of the filter is increased, the PF value hardly changes in the new schematic, while it starts to degrade in conventional case.

Developing appropriate frequency compensation for current sense (amplifier) in control circuits would further increase the range for the filter capacitance. The point of improvement in power factor value by the new approach, however, has been already illustrated.

New approach is therefore beneficial and promises improvements in general performance of the circuits (better power factor, increased efficiency, better heat management and smaller size) as well as better options in input filter design.

Chapter 17

Advantage of Bridge-less Converters for Active Filter Implementation

Issues associated with traditional passive filters applied to new bridge-less power factor correctors were discussed in previous chapters. Calculations and predictions were done for simple case – second order filter, which can be expanded to the filters of higher order with similar results. There is a different feature that appears in the new topologies; it is some advantage in case active filters are used.

Some theoretical work in area of active filters in related applications was done in [21] and [22]. New practical circuits were developed by author and described in [23] and [24]. All these circuits can be considered as feedback systems, or description of enhancement of the passive reactive element value can be also used. Such enhancement is done by the active elements in the circuit, which requires local supply source.

Fig. 17.1 shows basic block diagram for the active filter in three wire (one phase) system: line, neutral and ground. Conventional PFC is shown in this illustration.

New converters also enable including the input filter into power factor correction in case input filter is active. In addition to that, some practical issues of active filters have better and easier solutions, for example local power supply.

Fig. 17.1 shows that additional efforts have to be made to build the supply for active filter, which is located before the input diode bridge. On the other hand, local supplies are usual in PFCs because control always needs one. It is not possible to use already existing local control power supply from PFC in conventional topology. However, it is possible in the new bridge-less converters, Fig. 17.2.

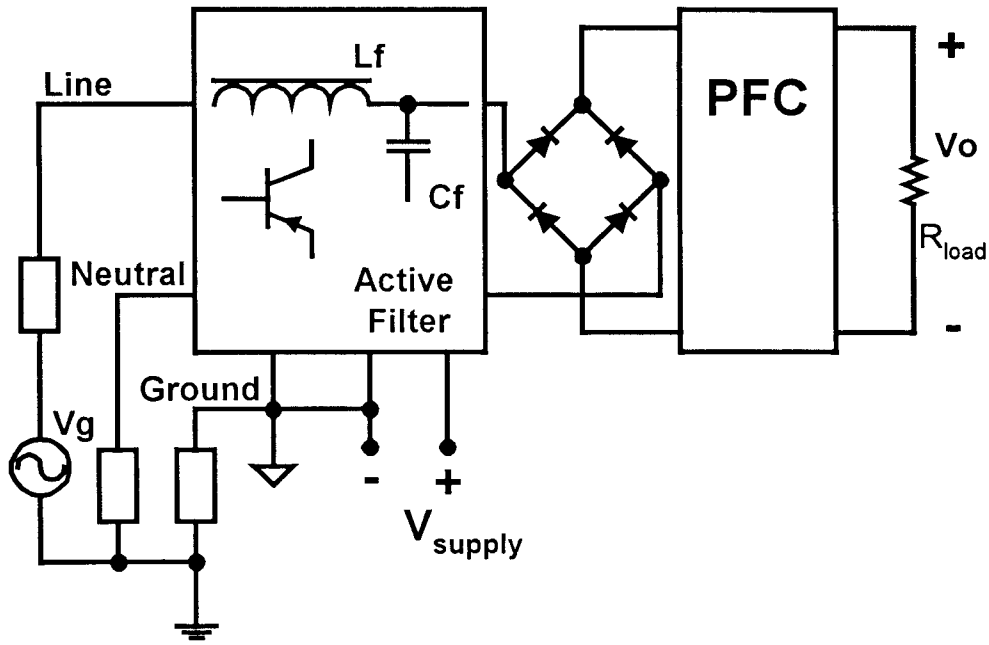

Figure 17.1: Block diagram of conventional PFC with active filter in three wire system

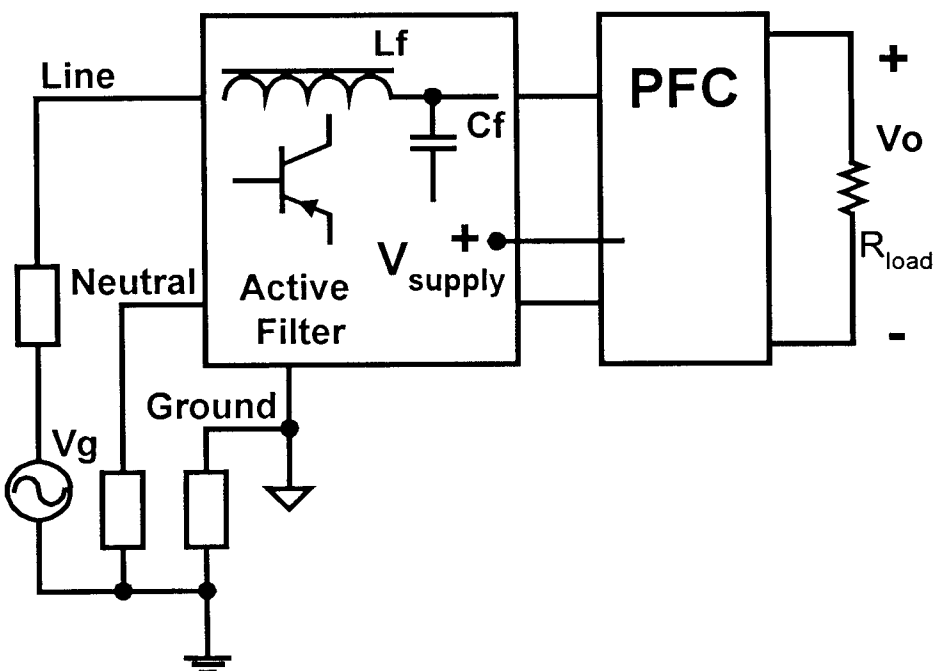

Figure 17.2: Block diagram of bridge-less PFC with active filter in three wire system

Bridge-less converters therefore show additional advantages over conventional topologies.

Further considerations in terms of active filters and new topologies are possible; however, they are outside of the main topic of this thesis.

Chapter 18

Advantage of Bridge-less PFCs: Conclusion

This thesis presented two new families of power factor correctors. PFCs on the basis of topologies with bipolar gain were introduced in the first part, then converters with shifted rectification were presented. These families of the converters, in addition to some existing topologies, share the absence of the input rectifier bridge.

Elimination of input rectification offers improved efficiency of the power factor correctors, especially in critical region of low input voltages. Also, this unique feature allows beneficial opportunities to include input filter into power factor correction and therefore to correct power factor right before the input filter, not after as in conventional topologies.

New topologies also allow more freedom in design of the input filter by weakening the condition of not affecting the value of PF by filter components. This feature leads to decreasing the cost and size of the filter.

Detailed analysis of the effects how input filter influences the value of power factor was conducted. New opportunities associated with bridge-less PFCs were investigated and findings were confirmed experimentally.

Introduced new families of the topologies for power factor correction also simplify some design issues in the area of active filter applications.

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