Si Microwire-Array Solar Cells

Thesis by
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Dedication

I proudly dedicate this thesis to my family.

They have made me the person who I am today.

Acknowledgements

The work presented in this thesis would not be possible without the numerous contributions and lessons learned from all of the wonderful people with whom I have had the chance to interact while at Caltech.

First and foremost, I must acknowledge my advisor, Harry Atwater, who welcomed me into his group five years ago. I did not fully appreciate at the time what a great privilege and opportunity this was. The Atwater group is full of people who are truly passionate about the possibility for their research to make a meaningful difference in the world around them. Have no doubts, this is a direct reflection of Harry. In particular, I would like to thank Harry for beginning to teach me the value of patience.

Nate Lewis has served as an unofficial co-advisor in many ways throughout my time here at Caltech. In this role Nate has offered forth his extensive knowledge of electrochemistry and the English language. Equally importantly, Nate has helped me to realize that while one can dedicate themselves to saving the world, it is best not to sacrifice oneself to it. His love of his Mazda RX-7, windsurfing, and his rumored love of the coral reefs in Hawaii have all been subtle reminders of this to me.

Like many successful Ph.D. projects, the Si microwire-array solar cell project has grown from work started by a single graduate student (Brendan Kayes in 2003) and blossomed into a project that merits the efforts of a number of graduate students and postdoctoral scholars. Members of the Si microwire-array solar cell project, in chronological order include: Brendan Kayes; James Maiolo; Josh Spurgeon; Michael Kelzenberg; Morgan Putnam; Dr. Michael Filler; Dan Turner-Evans; Dr. Kate Plass; Emily Warren; Jan Petykiewicz; Dr. Shannon Boettcher; Joseph Beardslee; Dr. Michael Walter; Dr. Adele Tamboli; Dr. Matthew Bierman; Dr. Nick Strandwitz; Dr. Ron Grimm; Liz Santori; Claire Baek; Emily Kosten; and Manav Malhotra. Each and everyone of these members has made their own (or is beginning to make their own) contributions to the project, and the success of my research has been largely dependent upon contributions from many of these individuals. It has and continues to be a truly great group of people with whom to work.

In particular, I would like to thank Michael Kelzenberg for showing me again and again, despite my protests to the contrary, the cadence of science. (The list of lessons that I could thank Mike for is actually quite a bit longer.) Brendan Kayes for demonstrating to me that those who know the most don't always speak the most. Shannon Boettcher for inspiring me to think like a chemist. Daniel Turner-Evans for reminding me how to be thoughtful when working as part of a team, and Michael Filler for teaching me how to write a scientific manuscript. I would also be remiss if I didn't thank Yunbin Guan for displaying true patience.

In addition to my research, I spent a good part of a year at Caltech working with Mike Kelzenberg to organize the student-installation of a 14 kW solar array on the roof of the Thomas J. Watson Laboratories of Applied Physics. A number of people were critical to the success of this project and in particular I would like to thank John Onderdonk, Jim Cowell, Alta Fang, Andrew Gong, and Heidrun Mumper-Drumm.

There is also a cohort of people who have helped me to maintain a sense of self and to help me grow as a person during my time here. Dalziel Wilson, Yonathan and Maayan Schwarzkopf, Mary Laura Lind, Nathan Lamarre-Vincent, Emily Rosene, John McKeen, David Pekarek, John Delacruz, Emily Warren, Michael Deceglie, Michael and Jessica Kelzenberg, Dan Turner-Evans, Shannon Boettcher, Imogen Pryce, Ryan Briggs, Kenneth Diest, Matthew Dicken, Melissa Archer, Adele Tamboli, Deirdre OCarrol, Marina Leite, Krista Langeland, Sean Pang, Erik Schomburg, Julian Romero, Alex Romero, Lise Lahourcade, Alice Robie, Alex Gagnon, Leo d'Espaux, and of course the Atwater group.

Morgan Putnam

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Abstract

By allowing for the fabrication of flexible crystalline-Si (c-Si) solar cells that employ $\sim 1/100^{th}$ the Si of a traditional wafer-based c-Si solar cell, while maintaining high photovoltaic efficiencies, vertically aligned arrays of c-Si microwires provide a novel photovoltaic geometry that has the potential to dramatically reduce the cost of solar electricity. In this thesis we report on 1) the growth of Si microwire arrays, 2) the chemical and electrical characterization of Si microwire arrays, and 3) the fabrication of Si microwire-array solar cells.

Using the vapor-liquid-solid (VLS) growth mechanism in combination with photolithographic patterning, vertically aligned arrays of Si microwires, with nominally identical heights and diameters, were fabricated over areas > 1 cm^2. Chemical characterization of the Si wires was then performed using secondary ion mass spectrometry to measure the incorporation of the Au VLS-catalyst into the Si wire. The incorporation of the VLS-catalyst into the Si wires at its thermodynamic equilibrium concentration suggested that the use of Cu as a VLS-catalyst was less likely to limit the photovoltaic performance of Si microwire-array solar cells. Switching to the Cu-catalyzed growth of Si wires, in-situ doping with BCl_3 was used to demonstrate control of the electrically active dopant concentration from 8×10^{15} to 4×10^{19} dopants cm^{-3}. Scanning photocurrent measurements were then made to measure the minority-carrier diffusion length. The observation of 10 μm minority-carrier diffusion lengths indicated that solar cells with efficiencies of 17.5% should be possible. With the knowledge that highly efficient solar cells were possible, methods for the fabrication of a p-n junction and a transparent top contact in a solid-state solar cell were developed. This culminated in the demonstration of Si microwire-array solar cells with Air Mass 1.5 Global photovoltaic conversion efficiencies of up to $\eta = 7.9\%$. Through improved device processing and the use of an amorphous Si passivation layer at the top contact, $\sim$15% efficient solar cells should be possible.

Contents

List of Figures

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List of Publications

Portions of this thesis have been drawn from the following publications:

Si Microwire-Array Solar Cells. M. C. Putnam, S. W. Boettcher, M. D. Kelzenberg, D. B. Turner-Evans, J. M. Spurgeon, E. L. Warren, R. M. Briggs, N. S. Lewis, and H. A. Atwater, Energy and Environmental Science, In press (2010).

10 μm Minority-Carrier Diffusion Lengths in Si Wires Synthesized by Cu-Catalyzed Vapor-Liquid-Solid Growth. M. C. Putnam, D. B. Turner-Evans, M. D. Kelzenberg, S. W. Boettcher, N. S. Lewis, and H. A. Atwater, Applied Physics Letters, **95**, 163116 (2009).

Secondary Ion Mass Spectrometry of Vapor-Liquid-Solid-Grown, Au-Catalyzed, Si Wires. M. C. Putnam, M. A. Filler, B. M. Kayes, M. D. Kelzenberg, Y. Guan, N. S. Lewis, J. M. Eiler and H. A. Atwater, Nano Letters, **8**, 3109 (2008).

Growth of Vertically Aligned Si Wire Arrays over Large Areas (>1 cm^2) with Au and Cu Catalysts. B. M. Kayes, M. A. Filler, M. C. Putnam, M. D. Kelzenberg, N. S. Lewis, and H. A. Atwater, Applied Physics Letters, **91**, 103110 (2007).

Chapter 1

Introduction

1.1 The Promise of Solar Energy

Solar energy is abundant, globally distributed, and free. Take a moment to consider the implications of this statement: energy, the single resource that has been most fundamental to improved standards of living, distributed equitably to all.

To place the abundance of solar energy in perspective, 90,000 terawatts (TW) of solar power continuously strikes the earth's surface.[1] Humanity's global power demand is a mere 14 TW.[2] Additionally, solar energy is the only energy resource that humanity could chose to use, not for the next 100 years, 10,000 years, or 1,000,000 years, but rather, for the next 5,000,000,000 years.

However the challenges to humanity's use of solar energy are not without merit. Like the facts above, it is also no secret that we desire to use energy when the sun does not shine. Additionally, we have developed technologies (airplanes and automobiles) that require areal power densities that can not be directly met by solar energy. Finally, humanity is largely able to function through capitalistic economies, which may or may not have correctly assessed the cost of solar energy, in its present form, to be unaffordable.

Consequently, for those who would desire to increase the use of solar energy, we must develop technologies that allow our global society to collect and store solar energy for as low a cost as possible.

1.2 Photovoltaics

Photovoltaic devices, or more commonly solar cells, are devices that upon exposure to electromagnetic radiation (photo) produce an electrical potential (volt). Though not the only means for harvesting solar energy[†], photovoltaics are particularly interesting because of their ability to produce electricity, which is the largest and fastest growing form of energy used in the United States.[4]

1.2.1 Market

Photovoltaics are currently experiencing rapid global growth, with 10-year and 5-year compound annual growth rates of 46% and 56%, respectively.[5] This tremendous rate of growth was initially driven by the restructuring of Germany's Renewable Energy Sources Act in 2000.[6] This act is a feed-in tariff, which guarantees to pay a price for photovoltaic electricity that will ensure that a well designed and operated photovoltaic system can realize between a 5 and 10% rate of return.

As the photovoltaics industry has grown, it has continued to exhibit a 80% progress ratio, which has led to significant cost reductions.[7, 8] A progress ratio reflects the cost reductions that are achieved as economies of scale are realized. Today the industry appears to be between 6 and 10 years from grid-parity without technological breakthroughs.[9] Grid-parity is the point at which the end-user pays the same price for photovoltaic electricity as they would to purchase electricity from the electrical grid.

However, if photovoltaics are to move beyond simply providing electricity during the day, the cost of photovoltaic electricity must be reduced below the point

[†]Photosynthesis, concentrated solar power, and passive solar energy are also important methods for harvesting solar energy. Though it receives little press, passive solar energy (the capture, storage and use of solar energy through building elements such as windows, Trombe walls, sunrooms, thermal chimneys, green roofs, roof ponds, thermal masses, day lighting and solar water heaters) is a form of particular interest for reducing the 39% of U.S. annual energy consumption that is attributed to buildings, of which 19.8% goes to space heating, 12.7% to space cooling and 17.7% to lighting.[3]

of grid-parity. To this end the need for technological breakthroughs in the field of photovoltaics still exists.

1.2.2 Technology

A number of photovoltaic technologies exist in the market today, e.g. crystalline-silicon (c-Si), multi-crystalline silicon (mc-Si), cadmium telluride (CdTe), copper indium gallium selenium (CIGS), amorphous-Si (a-Si), gallium arsenide (GaAs), and multi-junction solar cells, among others. Broadly, these technologies can be grouped into three groups. Thin-film technologies (CdTe, CIGS, *a*-Si) that are low-efficiency (7-10%) and low-cost (< \$1 per Watt peak), c-Si and mc-Si solar cells that are mid-efficiency (13-22%) and mid-cost (\$2.50-3.50 per Watt peak), and multi-junction solar cells that are high-efficiency (35-40%) and high-cost (many \$100's per Watt peak). Historically, crystalline-silicon (c-Si) and multi-crystalline (mc-Si) solar cells have been responsible for > 90% of the photovoltaics market. But in recent years this fraction has dropped to ∼85% as thin-film technologies (specifically First Solar's CdTe technology) have reduced costs low enough to enable significant market penetration despite their low efficiencies.

The low costs of thin-film technologies center around their reduced material usage and the ability to manufacture solar cells with a minimal number of processing steps. All three thin-film technologies achieve reduced materials usage (as compared to c-Si and mc-Si) through the use of semiconductors with direct bandgaps that strongly absorb incident sunlight. These materials need only be a few μm-thick to ensure complete absorption of incident sunlight as compared to ∼200 μm-thick c-Si and mc-Si wafers. Perhaps more importantly is the small number of processing steps that are needed to fabricate thin-film solar cells. By developing manufacturing processes that allow for processing of the photovoltaic material on its final support structure, thin-film solar cells have a significantly smaller number of processing steps than wafer-based photovoltaic technologies. Additionally, the deposition of the photovoltaic material onto the final support structure in thin-film technologies is often accomplished thru a low-cost solution or vapor deposition method.

Despite these recent advances in thin-film technologies, c-Si and mc-Si photovoltaics are still quite competitive with thin-film technologies because of their higher efficiencies. Though higher cell efficiencies are not enough to offset the low materials and manufacturing cost of thin-film cells at the module level, the higher cell efficiencies of c-Si and mc-Si cells becomes economically significant at the systems level, where higher efficiencies allow for significant reductions in the installation and balance of systems (support structure, copper wiring, etc.) costs.

As follows below, we will present a technology that combines the reduced materials utilization (and possibly the fewer number of processing steps) of thin-film technologies with the efficiencies of c-Si and mc-Si technologies.

1.3 Si Microwire-Array Solar Cells

1.3.1 Initial Motivation

For a typical photovoltaic installation, the solar panels comprise between 33% and 50% of the total installed cost.[9] In turn, for c-Si panels, the initial Si feedstock comprises between 14% and 28% of the panel cost.[10, 11] The large raw material cost of Si is determined by the purity of the Si required to produce efficient photovoltaic devices. Consequently, reducing the amount of Si feedstock required and/or the purity of the Si feedstock required[‡] has a significant impact upon the cost of c-Si solar panels and installed photovoltaic systems.

In order to reduce the Si purity required in a traditional wafer-based solar cell, one must decrease the distance that minority-carriers must travel before being collected at the p-n junction. However, because c-Si is a relatively weak absorber, the distance that minority-carriers must travel to the p-n junction is pre-determined by the wafer thickness required to absorb the incident illumination ($\sim$200 μm). One design that circumvents this challenge is the use of radial p-n junctions in wire-array solar cells.[13]

[‡]Metallurgical grade Si ($\sim$98% pure) can be purchased for $\sim$\$2/kg,.[12] while semiconductor/solar grade Si (99.9999% pure) costs $\sim$\$60/kg.[9]

As seen in Figure 1.1, the use of a radial p-n junction orthogonalizes the minority-carrier extraction direction from the light absorption direction. Si wires with length to diameter ratios on the order of 100:1 allow for solar cells that are optically thick, yet require minority-carrier diffusion lengths of only 1-2 μm, thereby significantly reducing the purity of the Si required.

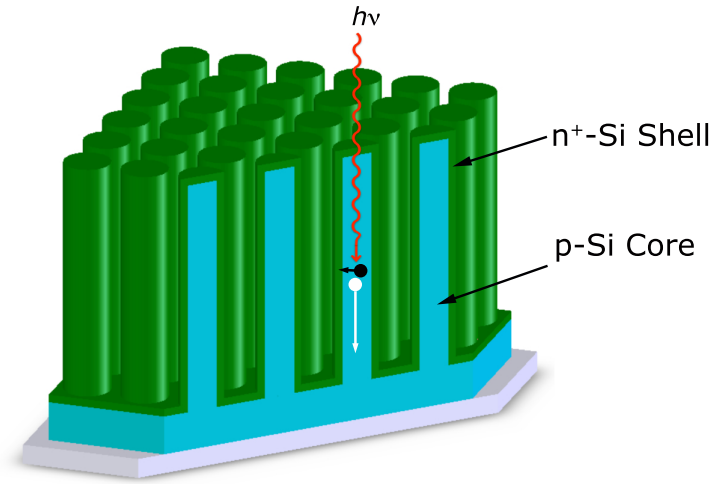


Figure 1.1. Schematic of a radial p-n junction, wire-array solar cell. Incident illumination is absorbed along the axial wire direction, while photogenerated minority-carriers (black dot) are collected radially.

Figure 1.2 provides a comparison of the calculated solar cell efficiencies for (a) a traditional planar cell and (b) a wire-array solar cell, as predicted by numerical modeling.[13] Whereas the traditional wafer-based solar cell exhibits a significant decay in efficiency as the minority-carrier diffusion length (L_n) is reduced, the wire-array solar cell remains capable of efficiencies $> 10\%$ for diffusion lengths as short as 100 nm. For minority-carrier diffusion lengths between 1 and 10 μm, wire-array solar cell efficiencies range from 12 to 15%. These efficiencies are quite comparable to the efficiencies of multi-crystalline Si solar cells and are meaningfully higher than the 10% efficiency of First Solar's CdTe solar cells (both mc-Si and First Solar's CdTe technologies are currently doing very well in the photovoltaics market).

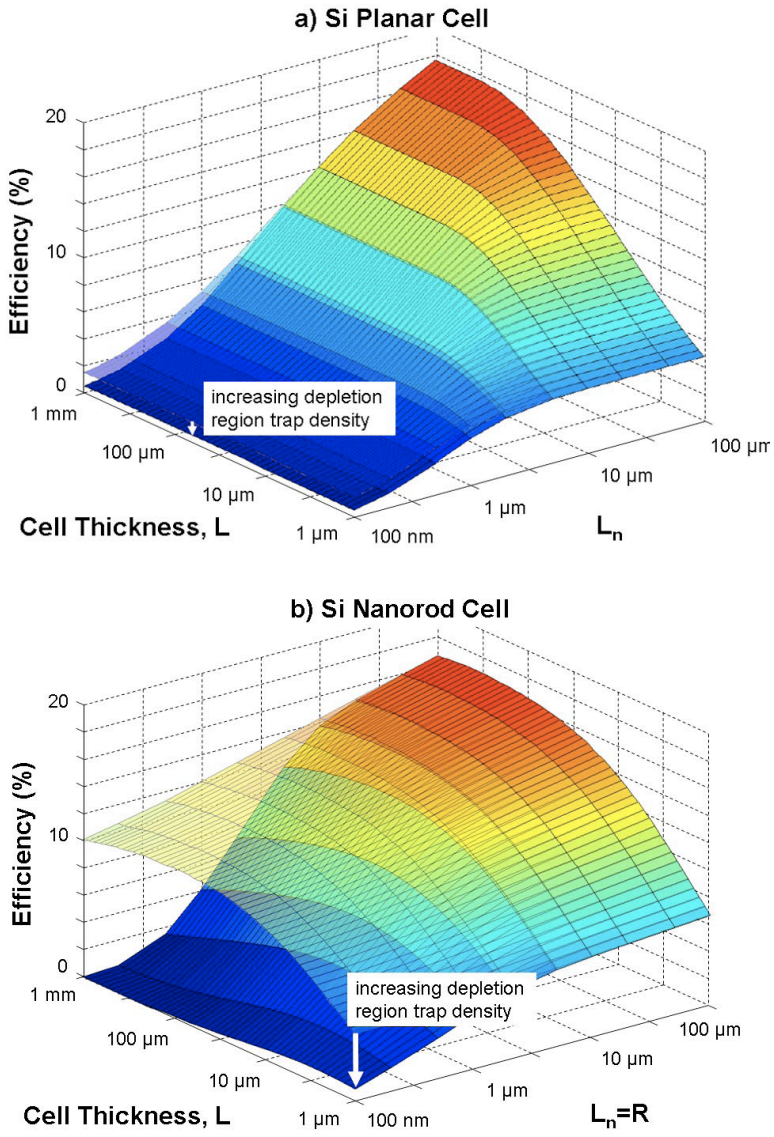


Figure 1.2. Calculated cell efficiency as a function of minority-carrier diffusion length (L_n) and cell thickness for (a) a traditional wafer-based solar cell and (b) a wire-array solar cell. In (b) the wire radius for the modeled solar cell has been set equal to the minority-carrier diffusion length.[13]

1.3.2 Flexible c-Si

Finding the predicted efficiencies of wire-array solar cells to be sufficiently high to merit further investigation, we began fabricating the proposed device structure. As will be detailed in Chapter 2, the fabrication of Si wire arrays is possible. However, we would like to point out that having fabricated Si wire arrays a fundamentally new type of material can be obtained by embedding the Si wire arrays in a flexible polymer.

As can be seen in Figure 1.3, Si wires embedded in polydimethylsiloxane (PDMS) polymer are a flexible form of c-Si.[14] We have shown that this material can absorb $> 85\%$ of the above bandgap solar illumination using a volume of Si equivalent to a 2.8 μm-thick Si film.[15] Thus, wire-array solar cells not only offer the possibility to reduce the cost of solar cells through the use of lower purity Si, but more importantly, wire-array solar cells offer the potential to use $1/100^{th}$ the Si of a traditional wafer-based solar cell. Furthermore, the flexibility of this material is especially exciting. In addition to allowing for the fabrication of flexible solar panels with efficiencies $> 10\%$, it may also result in reduced module manufacturing costs through the adoption of quasi roll-to-roll fabrication processes.

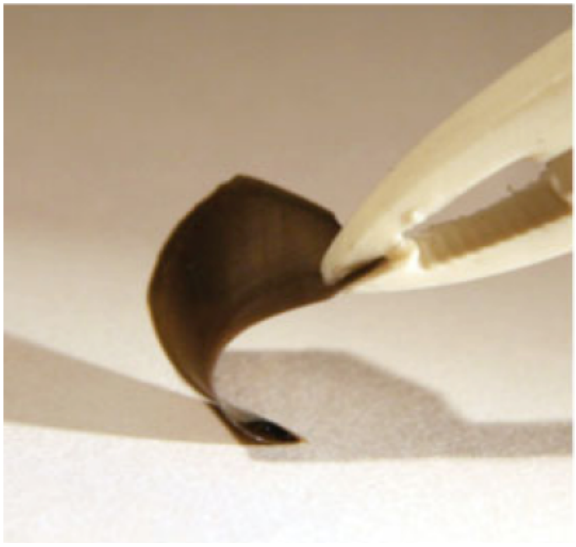


Figure 1.3. Optical image of a Si microwire array embedded in polydimethylsiloxane polymer.[14]

1.4 Thesis Outline

This thesis will detail key steps in the fabrication and characterization of Si microwire-array solar cells. Chapter 2 will detail how the vapor-liquid-solid (VLS) growth mechanism can be used to grow arrays of nominally identical, vertically aligned, Si microwires over areas > 1 cm^2. In Chapter 3, Si microwires are chemically characterized to understand if incorporation of the metal VLS-catalyst into the Si microwires might limit the microwire solar cell efficiencies. Chapter 4 details how in-situ doping was incorporated during the VLS-growth process to control the electrical properties of the microwires. Chapter 5 presents photocurrent measurements used to demonstrate that the minority-carrier diffusion length in the Si microwires was sufficiently large for the fabrication of efficient solar cells. In Chapter 6, Si microwire-array solar cells are fabricated and characterized. Finally, Chapter 7 provides an outlook for further progress towards the fabrication of $\sim$15% efficient, flexible, Si microwire-array solar cells.

Chapter 2

Vertically Aligned Si Microwire Arrays

2.1 Introduction

In this chapter we will discuss the development of a process for the fabrication of large-area arrays of vertically aligned, nominally identical, Si microwires. There are three major reasons that a homogeneous medium of Si microwires was felt to be important for the characterization and fabrication of Si microwire arrays as a potential photovoltaic material. First, control of the wire height and diameter allows for the fabrication of wires with diameters and heights that are optimized for photovoltaic performance based upon the measured photovoltaic properties of the wires. Second, fabrication steps, such as the definition of a p-n junction, the growth of a surface passivation layer, and the deposition of a transparent top contact, are much more straightforward (as will be seen in Chapter 6) for a uniform array of wires. Third, a large distribution of wire heights and diameters will lead to a distribution in each wire's voltage at its maximum power point.[16] As the wires will be connected in parallel in a wire-array solar cell and as the wire-array solar cell must operate at a single voltage, a distribution in the wire height and diameter will result in a fraction of wires that operate away from their maximum power point. Thus, a wire-array solar cell with a large variation in wire heights and diameters will be inherently inefficient.

The fabrication of nominally identical, vertically aligned, Si microwires was accomplished through the use of the vapor-liquid-solid (VLS) growth mechanism. Photolithography was used to pattern an array of VLS-catalysts (Au, Cu or Ni) onto a Si(111) wafer. VLS-growth using $SiCl_4$ as a Si precursor at 1000 °C was then used to grow Si microwires roughly 2 μm in diameter and 75 μm in length. The use of a

thermally grown silicon oxide was found to be critical to prevent catalyst diffusion and loss of pattern fidelity during the pre-growth anneal at 1000 °C.

2.2 Vapor-Liquid-Solid Growth

2.2.1 Mechanism

The vapor-liquid-solid (VLS) growth mechanism was discovered in 1964 by Wagner and Ellis.[17] As depicted in Figure 2.1, the VLS growth mechanism involves the incorporation of Si from a gaseous Si precursor into a VLS-catalyst/Si alloy (liquid), followed by the precipitation of solid Si from the VLS-catalyst/Si alloy. Under the appropriate growth conditions, the VLS-catalyst (most commonly Au) enhances the local deposition rate ∼100-fold, resulting in the creation of a one-dimensional Si wire.

Figure 2.1b provides the Au-Si phase diagram. Prior to the introduction of the Si precursor, Si from the growth wafer alloys with the Au catalyst (and Au from the catalyst diffuses into the wafer) as the sample is brought to the growth temperature. This annealing process results in a Au-Si alloy lying on the right liquidus line (as indicated by the small circle). With the addition of a gaseous Si precursor, the Au-Si alloy incorporates additional Si and begins to precipitate solid Si.

Studying the VLS-growth mechanism in some depth, Wagner and Ellis showed that a number of metals could be used as VLS-catalysts (e.g, Au, Pt, Ag, Pd, Cu, Ni, Gd, Mg and Os).[17, 19] Importantly, Wagner also showed that wires grown by the VLS-growth mechanism were single-crystals and grew in the <111> growth direction.[20] The observation of single-crystal wire growth is significant, as it indicates that the wires have the potential to exhibit very good photovoltaic properties.

2.2.2 Growth Conditions

For the fabrication of Si wires, the early work of Wagner focused on the use of $SiCl_4$ as the Si precursor.[17, 18, 19, 20] In contrast the recent literature has focused on the use of SiH_4 or Si_2H_6 as a Si precursor.[21, 22, 23] VLS-growth conditions using SiH_4

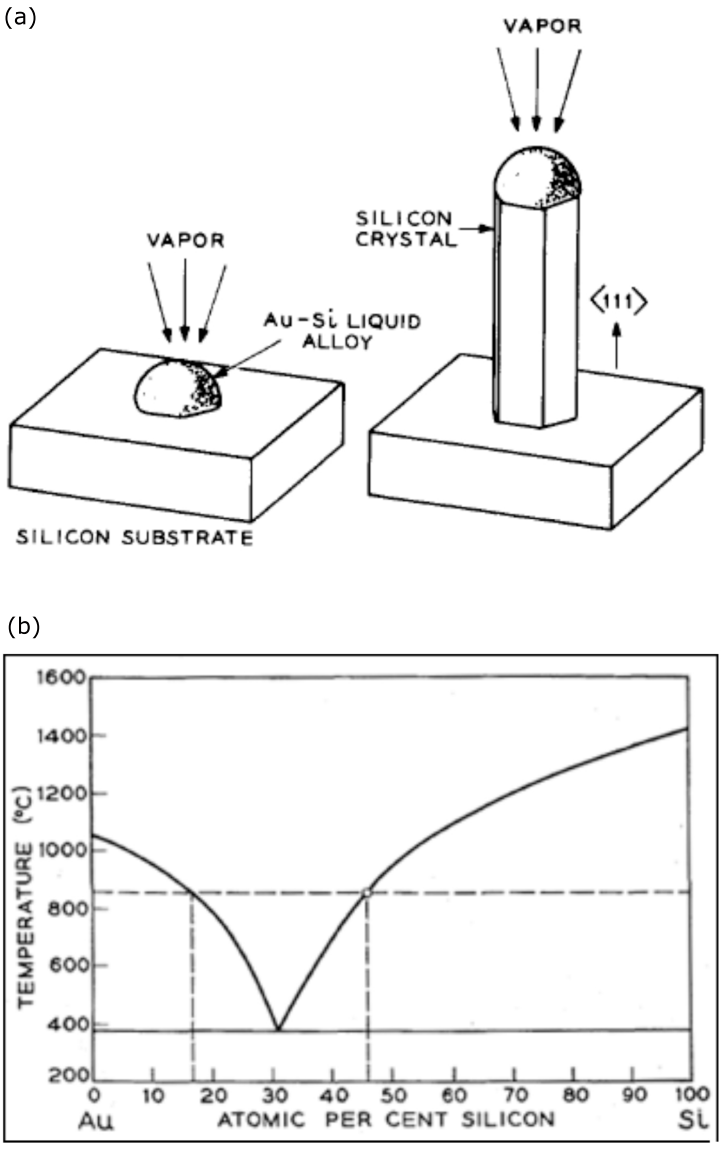


Figure 2.1. (a) Schematic of the vapor-liquid-solid (VLS) growth mechanism.[17] (b) The Au-Si phase diagram.[18]

typically range from 350-600°C and have a typical SiH_4 partial pressure between 0.01 and 5 Torr. $SiCl_4$ growth conditions use temperatures between 800°C and 1000°C and operate close to atmospheric pressure with a $SiCl_4$ to H_2 ratio of 1:50.

In addition to the different temperature and pressure regimes, a key difference between the use of SiH_4 and $SiCl_4$ as a Si precursor is the presence of an etching reaction when using $SiCl_4$ as a Si precursor. The decomposition of SiH_4 as shown in Eqn. 2.1 is an exothermic, irreversible reaction, limited only by kinetic decomposition.[24] In comparison $SiCl_4$ can be used to either etch or deposit Si depending upon the pressure, temperature, and the ratio of $SiCl_4$ to H_2 in the gas phase.[25] This is because the decomposition of $SiCl_4$ as shown in Eqn. 2.2 results in the production of HCl(g), which is known to etch Si.

$$SiH_4(g) \rightarrow Si(s) + 2H_2(g) \tag{2.1}$$

$$SiCl_4(g) + 2H_2(g) \rightleftharpoons Si(s) + 4HCl(g) \tag{2.2}$$

In our work we have used both SiH_4 and $SiCl_4$ as Si precursors. For SiH_4 growths, a hot wall reactor was used as shown in Figure 2.2, while for $SiCl_4$ growths a tube furnace reactor was used as shown in Figure 2.3. Using SiH_4, Brendan Kayes found the optimal growth temperature to be between 500 and 550 °C and the optimal growth pressure to be 1 Torr with a 100 sccm flow of SiH_4 (5% in H_2.)[26]. Using $SiCl_4$ we found the optimal growth temperature to be 1000 °C at atmospheric pressure with a 500:10 sccm H_2:$SiCl_4$ reactant flow.[27].

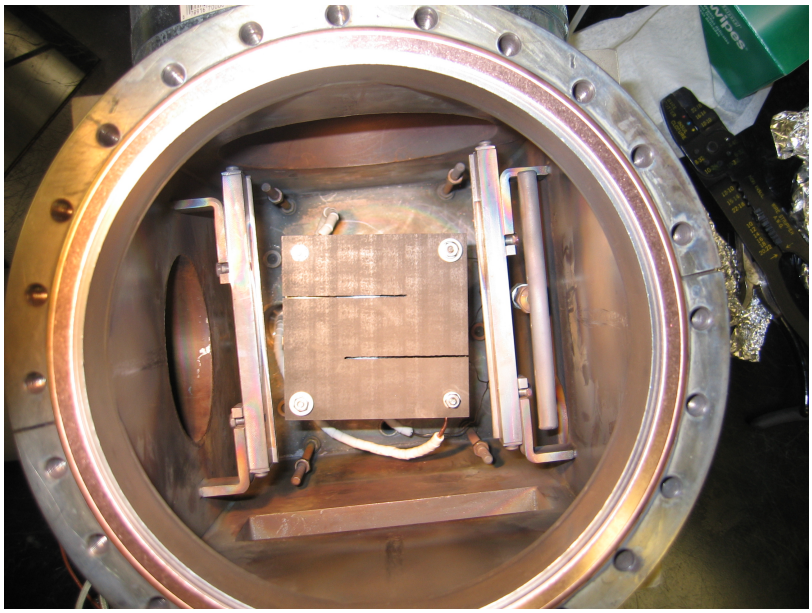


Figure 2.2. SiH_4 VLS growth reactor located in Watson 247. The gas inlet is the thin cylinder on the far right of the chamber, while the gas outlet is the visible opening on the left hand side of the chamber. The sample is placed in the center of the chamber, above the internal heating element (not used during VLS growths) visible at the center of the reactor and ∼0.5 in. below the external heating element of the reactor, which is located in a recessed well that is part of the top of the reactor (not shown here.)

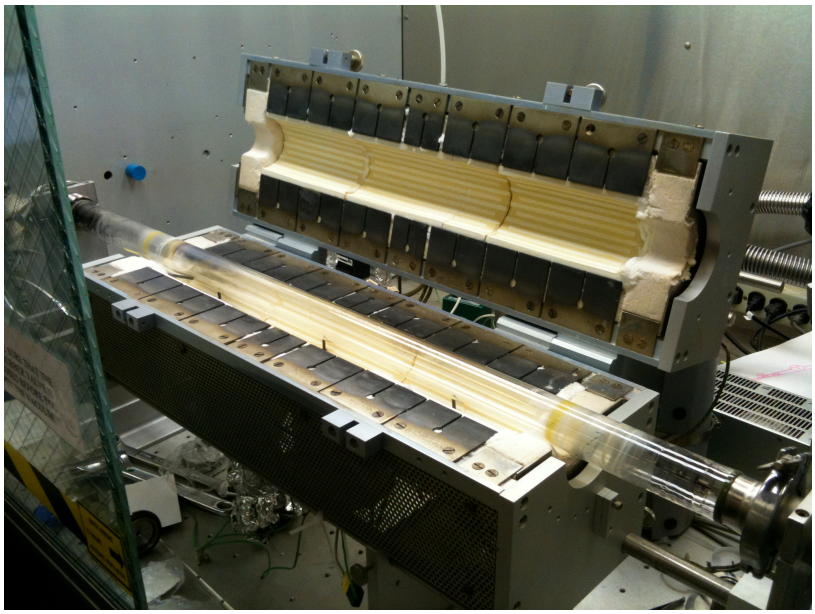


Figure 2.3. $SiCl_4$ VLS growth reactor located in Watson 251. Gases enter the tube furnace from the left and are exhausted to a NaOH scrubber (not shown) on the right hand side. For a more detailed description and a schematic of the reactor layout, see Appendix A.

2.3 Catalyst Deposition

2.3.1 Blanket Deposition

Initial efforts in our group to obtain Si wire arrays for solar cells focused on the blanket deposition (thermal evaporation) of Au catalyst, followed by the optimization of wire-growth conditions (catalyst, temperature and pressure) using SiH_4 as the Si precursor.[28] In this process, the blanket deposited Au would break up into smaller droplets from which the Si wires would grow, as schematically depicted and shown (for a 6 nm-thick Au layer) in Figure 2.4. It is clear from Figure 2.4c that the size of the Au-Si alloy at the onset of wire-growth was varied and that Si wire growth did not begin uniformly across the wafer.

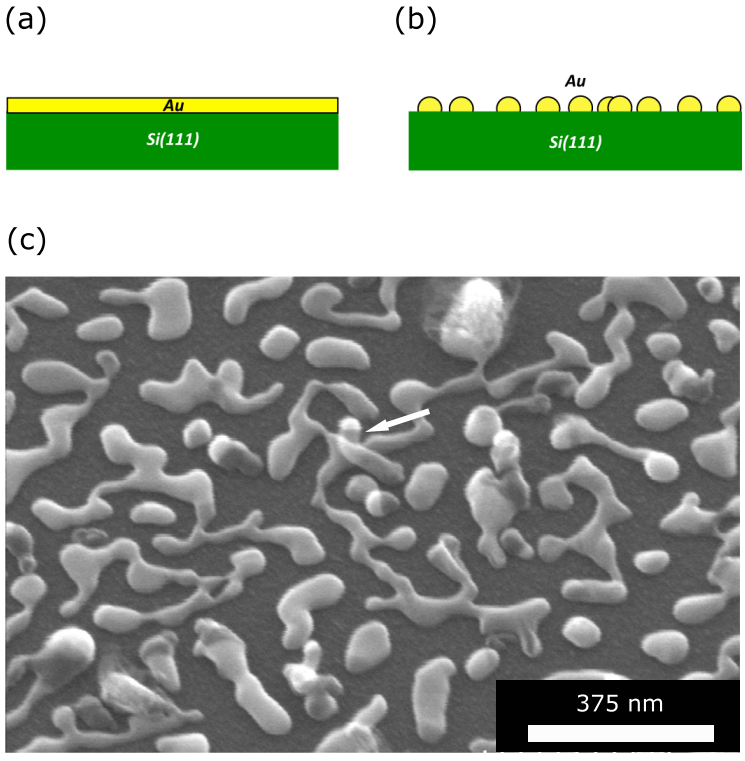


Figure 2.4. SEM image of the onset of VLS-growth. The white arrow denotes a wire that has begun to grow.

After three hours of growth, wire arrays exhibiting a roughly 75% fraction of vertically oriented wires were obtained, as shown in 2.5. The Si wires were ∼200 nm in diameter and on the order of 10 μm in length. In Fig. 2.5a, the short bright lines are the vertically oriented wires.

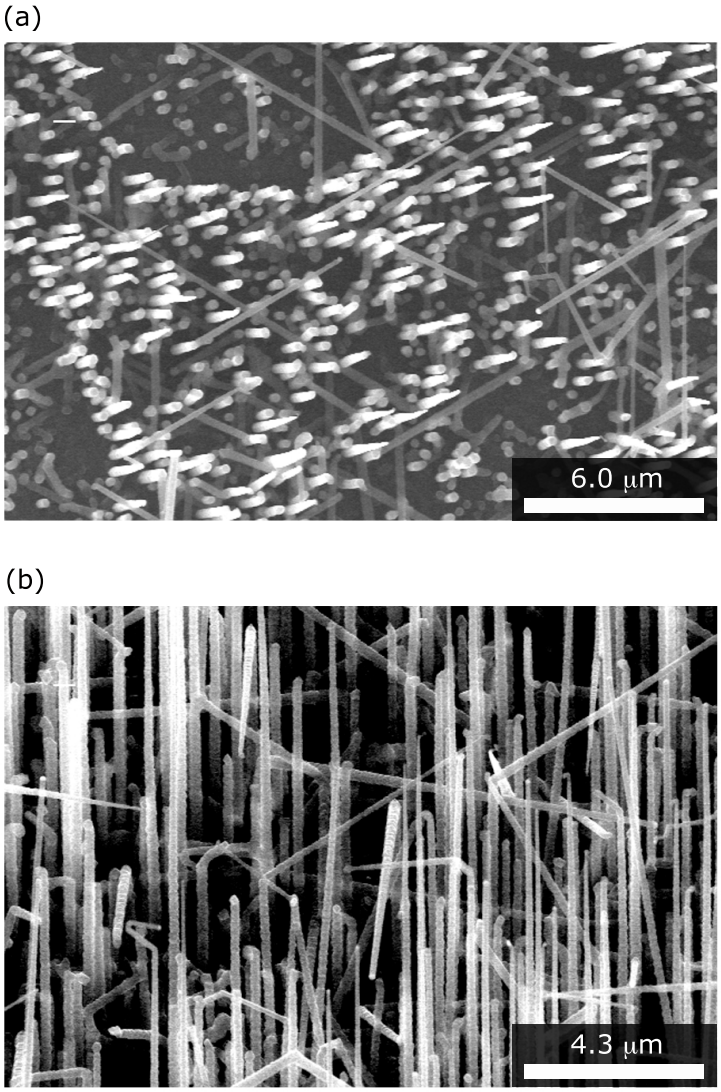


Figure 2.5. (a) Top-down and (b) tilted SEM images of a Si wire array grown from a 20 nm-thick Au film using SiH_4 as the Si precursor.

2.3.2 Photolithographic Patterning

Hoping to realize a more uniform array of Si wires, efforts were undertaken to pattern the Au catalyst prior to wire growth. Two photolithographic patterning processes were developed. The first process produced a square-array of 3 μm diameter Au pads on a 7 μm pitch on a Si(111) wafer (Fig 2.6a). The second process patterned the same array of Au pads, except that these pads were patterned onto the Si wafer through openings in a thermal oxide (SiO_2) with the inverse pattern (Fig. 2.6b). Figures 2.6c,d provide optical and SEM images, respectively, of a catalyst array deposited onto a Si wafer through openings in a thermal oxide (the second process.) The right hand side of Fig. 2.6c is a region of the wafer with incomplete lift-off of the 1813 photoresist after blanket Au deposition. Though incomplete lift-off was not typical, it has been included here to provide a sense of the lift-off process.

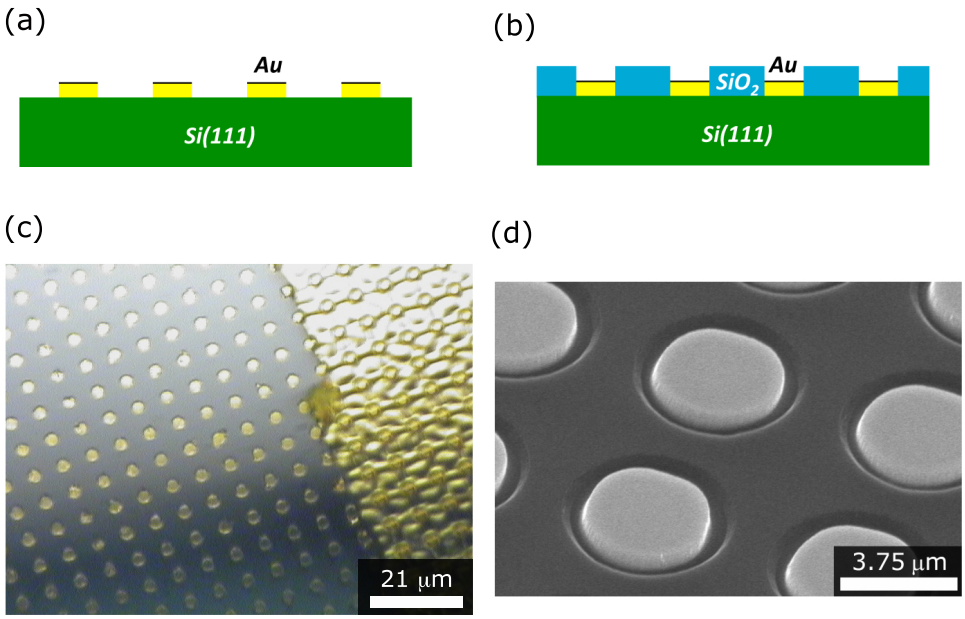


Figure 2.6. Cross-sectional schematic of a patterned Au array (a) on a Si(111) substrate and (b) into holes in a thermal oxide on a Si(111) substrate. (c) Optical and (d) SEM images of 300 nm-thick Au pads surrounded by a thermal oxide on a Si(111) substrate.

Our initial thought in developing the second patterning process was that the etched oxide might guide initial wire growth in the vertical direction. However, given that SiO_2 is etched isotropically by hydrofluoric acid (aq.) and that the deposited catalyst thickness was comparable to the oxide thickness (typically 300 nm), it is unlikely that the patterned oxide conferred a significant physical barrier to wire kinking at the onset of growth. But, as can be seen in Figure 2.7, it was discovered that the presence of the thermal oxide between the patterned Au pads was critical to preventing Au diffusion during the pre-growth anneal at 1000 °C when using $SiCl_4$ as the Si precursor.[27]

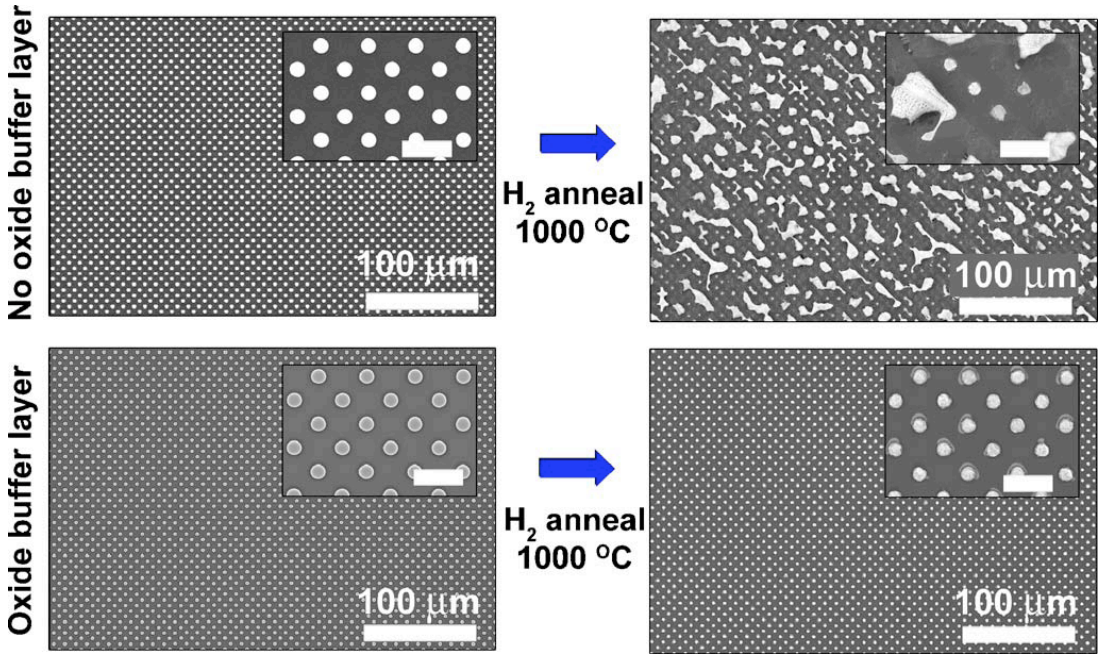


Figure 2.7. SEM images of patterned Au catalyst arrays before (left) and after (right) a pre-growth anneal in H_2 (740 Torr) at 1000 °C. The top row is a catalyst array without the thermal oxide, and the bottom row is a catalyst array with the thermal oxide. *Insets*, the scale bars are 10 μm.[27]

2.4 Array Growth

As can be seen in Figure 2.8, use of the patterned catalyst arrays (no oxide present) in the SiH_4 growth system resulted in the desired isolation of wire growth to areas of the substrate initially patterned with catalyst (as expected from the VLS-growth mechanism.) Encouragingly, the density of wires and the fraction of vertically oriented wires was now uniform over the growth area, which was a marked improvement from the varying density of wires and varying fraction of vertically aligned wires obtained using the blanket deposition of catalyst (Fig. 2.5.)

However, the nucleation of multiple wires per patterned catalyst area and the presence of wire kinking during growth meant that the synthesized wire arrays were still not uniform enough for use in solar cells. The nucleation of multiple wires per Au pad is attributed to breakup of the catalyst droplet. Considering the large ratio of the catalyst diameter, 3000 nm, to the catalyst thickness, 1 nm, breakup of the catalyst droplet seems plausible. Furthermore, nucleation of multiple wires per Au pad was successfully eliminated by increasing the catalyst thickness to 300-500 nm. Figure 2.9 provides a higher magnification image of the kinking observed during wire growth.

While I had been working on the development of photolithographically patterned catalyst arrays, Brendan Kayes and Dr. Michael Filler had been building a reactor for VLS-growth using $SiCl_4$. $SiCl_4$ had recently been shown to yield a very high fraction of vertically aligned Si wires,[28] and it was hoped that by combining the use of patterned catalyst arrays with a $SiCl_4$ precursor we would be able to obtain homogeneous wire arrays over large areas.

Indeed, as shown in Figure 2.10, the fabrication of nominally identical, vertically aligned, Si microwires over areas > 1 cm^2 was possible.[27] Though it was not known to us at the time, the selective placement and growth of vertically aligned wires over very small areas (100 wires on a 60μ pitch) had previously been shown using a similar process.[29] After a 30 min growth, the wires were 75 μm in length and 2 μm in diameter. The difference between the patterned catalyst diameter of 3 μm and the

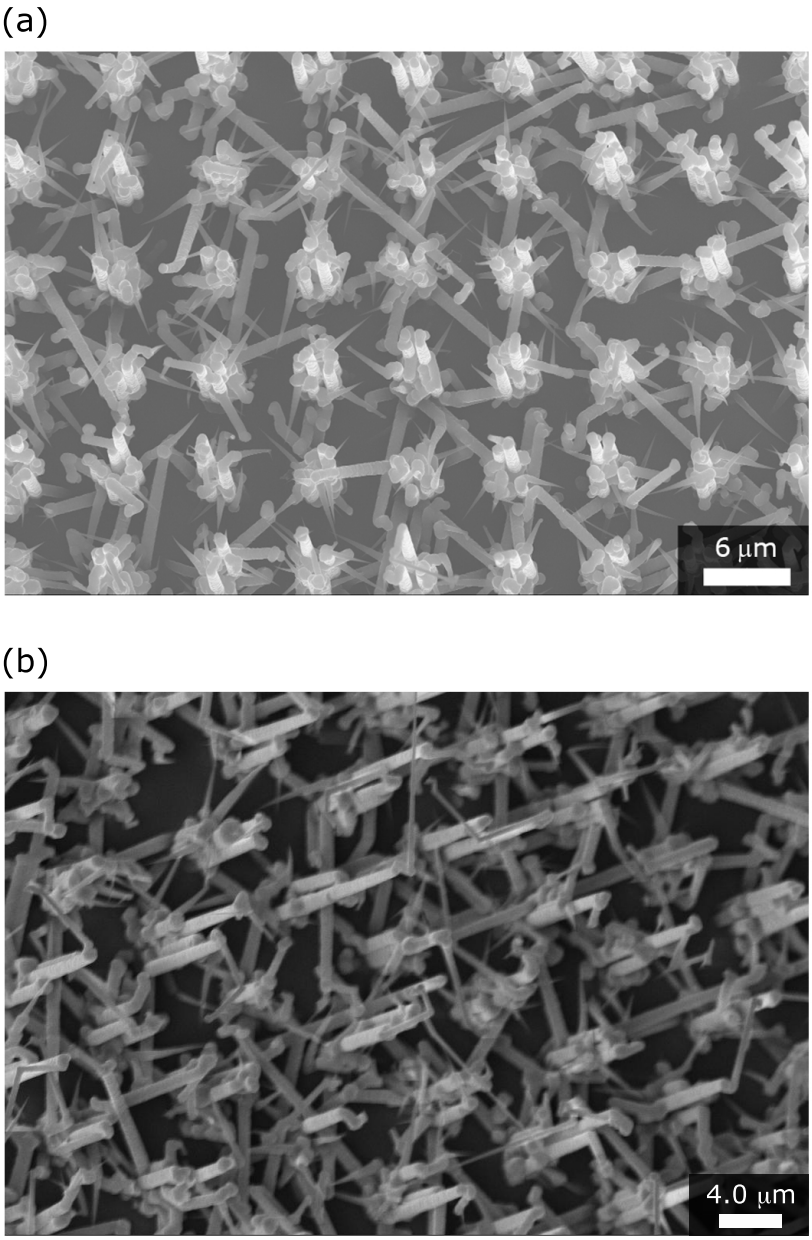


Figure 2.8. (a) Top-down and (b) tilted SEM images of a Si wire array grown from a photolithographically patterned, 1 nm-thick, Au array (thermal oxide not present), using SiH_4 as the Si precursor.

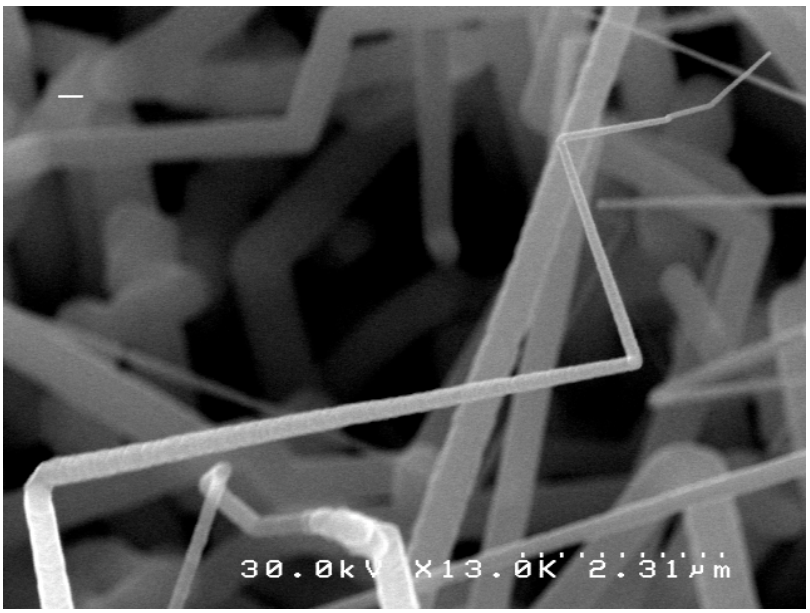


Figure 2.9. SEM image of a wire that has kinked multiple times during VLS-growth using SiH_4 as a Si precursor.

observed wire diameter of 2 μm is attributed to the change in the catalyst shape as it transitions from the solid state to the liquid state when alloyed with Si at the growth temperature.

In addition to the growth of the Si wire arrays using Au as the VLS catalyst, we have demonstrated that structurally identical wire arrays can be grown using Cu or Ni as the VLS-catalyst under identical growth conditions, as seen in Figure 2.11. The Si wire growth rate using Cu and Ni catalysts was $\sim$5 μm/min, roughly twice the 2-3 μm/min growth rate observed for Au-catalyzed Si wires. Ni and Cu-catalyzed Si wires also exhibited slightly smaller diameters for a given catalyst thickness, likely due to a change in the contact angle of the catalyst alloy with the growing Si wire and/or greater incorporation of the catalyst into the growth wafer.

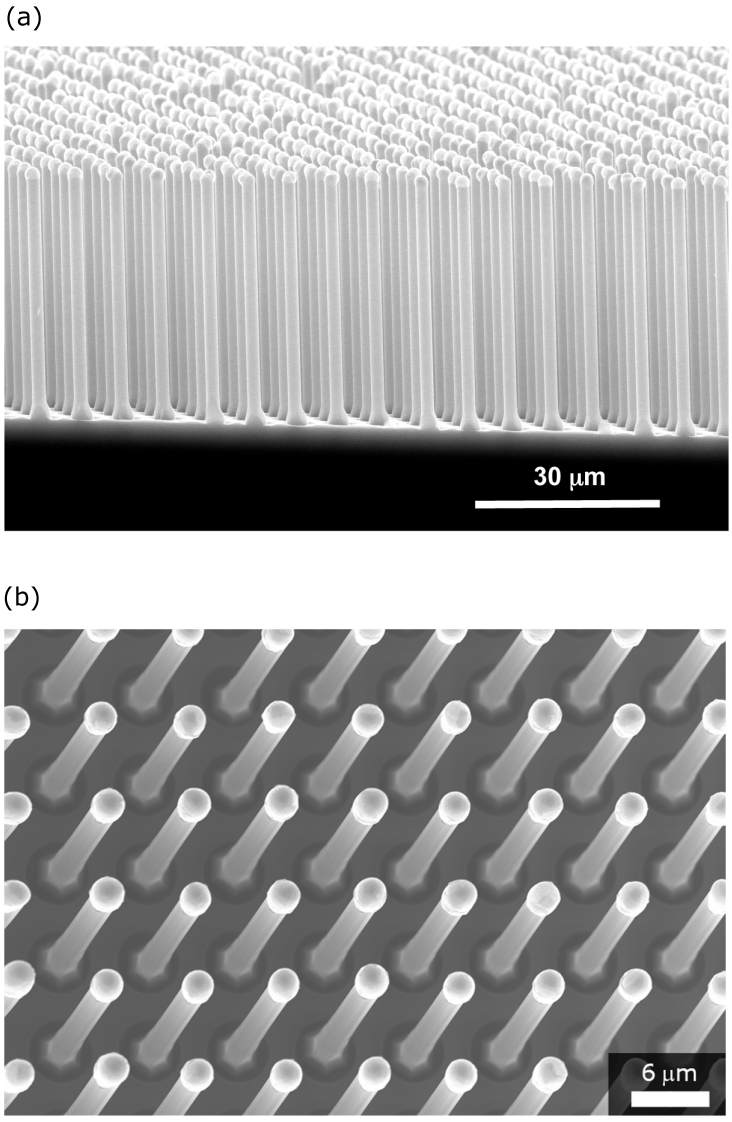


Figure 2.10. (a) Cross-sectional and (b) top-down SEM images of a Si wire array grown in the $SiCl_4$ reactor using a 500 nm-thick Au catalyst array.[27]

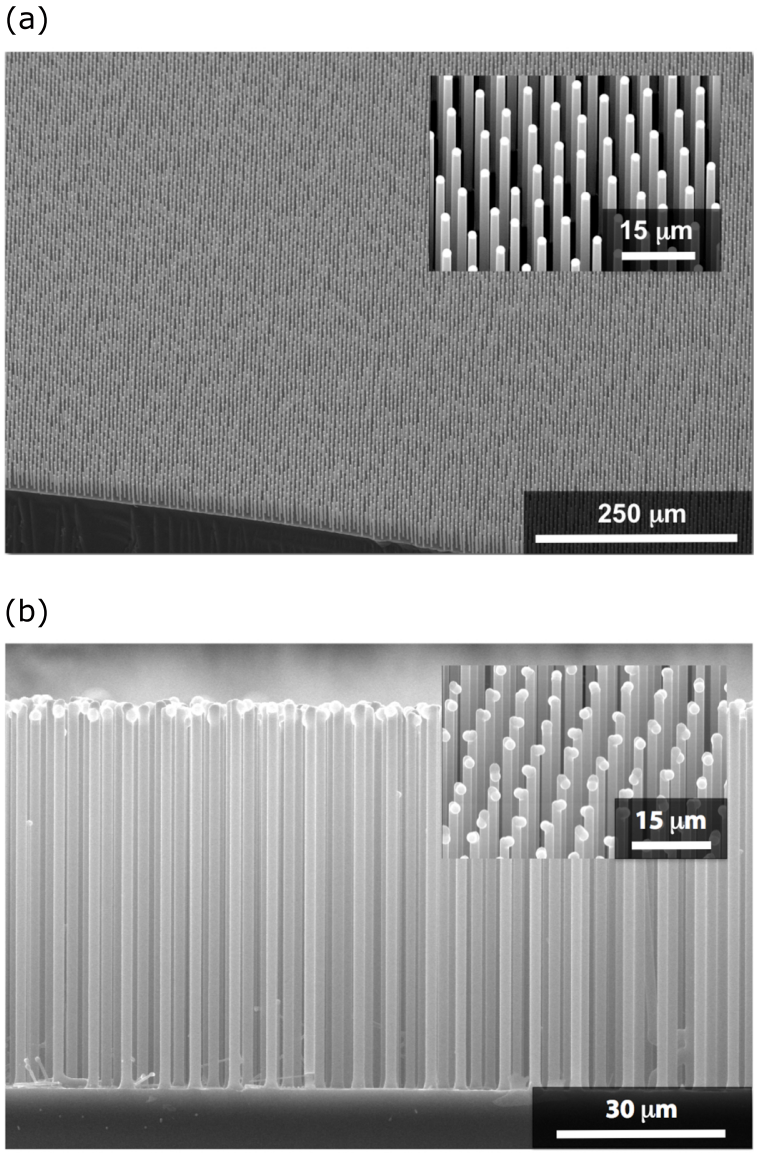


Figure 2.11. (a) Cu-catalyzed wire array growth (b) Ni-catalyzed wire array growth.[27]

2.5 Discussion

2.5.1 Si Precursor

Though our high-fidelity wire arrays were grown using $SiCl_4$, it is not clear that similar arrays could not also be grown using SiH_4 as the Si precursor. However, the presence of an etching reaction during $SiCl_4$ growth should facilitate the removal of high-energy surface defects that may lead to kinking during wire growth. Indirect evidence for the dependence of kinked wire growth on surface defects exists in the literature. Using SiH_4 as the Si precursor, Westwater showed that wire kinking decreased with increasing growth temperature and decreased with decreasing SiH_4 partial pressure.[21] Higher growth temperatures and lower SiH_4 pressures should both result in greater Si surface diffusion, the later as a result of a greater number of unoccupied surface sites. Thus, Westwater's observations support the hypothesis surface defects may lead to kinked wire growth.

Additional indirect evidence relating wire kinking to surface defects is provided by two separate observations. First, Si wires grown from Si_2H_6 at a pressure of 1×10^{-6} Torr and temperature of 600 °C (using an ultra-high vacuum growth system) exhibited minimal kinking, while wires grown under the same conditions with the addition of 2×10^{-7} Torr O_2 exhibited significant wire kinking.[30] Second, O_2 is known to prevent the sintering of Si particles (performed at T > 1000 °C), which is largely a surface diffusion driven process.[31] Thus, we again conclude that decreased surface diffusion and a probable increase in the number of defect states at the Si surface is likely related to kinked wire growth.

2.5.2 Photolithography

Though photolithography is a simple and relatively inexpensive patterning method at the research scale, the use of photolithography in the manufacturing of commercial solar cells would likely be prohibitively expensive. While other patterning techniques, such as the use of ink-jets, could be used in place of photolithography, Josh Spurgeon

in the Lewis group has demonstrated a promising method to re-use the growth substrates without additional patterning, as seen in Figure 2.12.[32] After peel-off of the PDMS-embedded Si wire array,[14] the growth substrate retains the patterned thermal oxide as well as a small fraction of the wire bases and the PDMS (Fig. 2.12a). The wire bases and the PDMS are then removed through wet chemical etching, while leaving the patterned thermal oxide intact (Fig. 2.12b). The desired array of Au catalyst pads was then created through the electrodeposition of Au, taking advantage oxide's dielectric properties (Fig. 2.12c). Thus, another Si wire array was grown on a previously used growth substrate without the use of additional patterning methods (Fig. 2.12d).

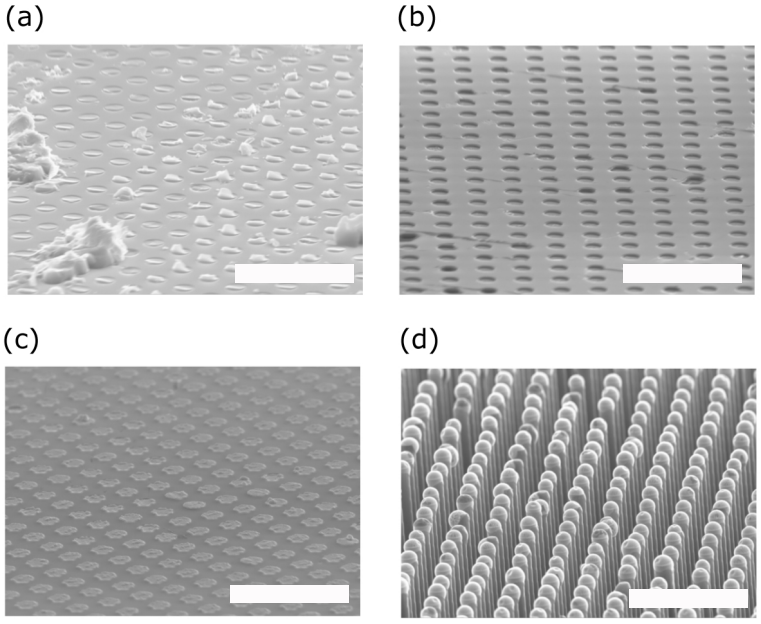


Figure 2.12. SEM images detailing the re-use of the growth substrate without additional patterning steps. (a) Si substrate after peel-off of the PDMS-embedded wire array. (b) Chemical etching is performed to remove the remaining PDMS and the bases of the Si wires. (c) Electrodeposition of the VLS-catalyst onto the Si substrate (but not onto the thermal oxide.) (d) Growth of a Si wire array from a Au array electrodeposited onto a previously used growth substrate. Scale bars are 20 μm.

2.6 Conclusion

Vapor-liquid-solid growth using $SiCl_4$ as a Si precursor and photolithographically patterned arrays of a Au, Cu, or Ni catalyst were used to produce vertically aligned, Si microwire arrays over areas > 1 cm^2. The narrow distribution of wire heights and diameters obtained with the described growth method is critical to the fabrication of efficient wire-array solar cells. As such, the Si wire arrays fabricated in this chapter represent the key building block upon which the subsequent work in this thesis is built.

Chapter 3

Si Microwire Chemical Composition

3.1 Introduction

Having demonstrated the ability to fabricate arrays of vertically aligned Si microwires using the vapor-liquid-solid (VLS) growth mechanism in Chapter 2, we turned our focus to the characterization of the wires' chemical composition. Quantitative measurement of the concentration of both impurity (e.g., VLS catalyst) and dopant species in Si microwires allows one to understand the limits on photovoltaic efficiency imposed by the VLS growth mechanism and the pn-junction fabrication process. In this chapter we use secondary ion mass spectrometry to characterize the Au catalyst concentration within individual, VLS-grown, Si wires. For Si wires grown by chemical vapor deposition from $SiCl_4$ at 1000 °C, an upper limit on the bulk Au concentration was observed to be 1.7×10^{16} atoms cm^{-3}, similar to the thermodynamic equilibrium concentration of Au in Si at the growth temperature. Additionally, we demonstrate the ability to measure B and P concentrations $> 5 \times 10^{17}$ atoms cm^{-3}. Finally, we discuss the motivation for switching to Cu-catalyzed wire growth.

3.2 Background

Efforts to determine Au incorporation in VLS-grown, Si wires have been limited to date, as a result of the sub-micron spatial resolution and better than part per million chemical sensitivity required to analyze individual wires. In an attempt to meet these stringent requirements, localized electrode atom probe (LEAP) tomography has been used to probe the concentration of Au in 100 nm diameter Si wires grown by chemical

vapor deposition (CVD) at 550 °C using SiH_4 as the Si precursor.[33] However, using LEAP tomography Perea et al. were unable to detect Au in the Si wires and were limited to setting an upper limit on the Au concentration between 5×10^{17} and 1.5×10^{18} atoms cm^{-3}.[34] More recently, high-angle annular dark-field (HAADF) scanning transmission electron microscopy (STEM) has been used to spatially localize single Au atoms within 15 nm diameter Si wires grown by CVD at 450 °C,[34] as well as ∼30 nm diameter Si wires grown by molecular beam epitaxy (MBE) at 500 °C.[35] SiH_4 was used as the Si precursor in both reports. These HAADF STEM results suggested that for both the CVD and MBE grown Si wires the bulk Au concentration is considerably greater than the thermodynamic equilibrium concentration of Au in Si at the growth temperature. Estimates of the bulk Au concentration from the HAADF STEM results were limited by the small volume of Si sampled (only a couple Au atoms were detected) and the correspondingly poor counting statistics.

3.3 Sample Preparation

As described in Chapter 2 and shown in Figure 3.1, high-fidelity arrays of well-aligned Si wires were grown from patterned Au catalysts on a Si(111) wafer.[27] These wires were then analyzed in both the axial and radial directions. To analyze the wires radially, the wire arrays were sonicated in isopropanol to obtain a suspension of Si wires in isopropanol. This suspension was then drop-cast onto a Ge(111) wafer to obtain wires lying on their side. For axial analysis, wires were measured in their as-grown vertical orientation on the growth substrate.

All axially profiled wires and some radially profiled wires were etched to remove Au (in a manner similar to Woodruff *et al.*[36] and detailed in Appendix B) prior to SIMS analysis (Fig. 3.1c). After treatment, Au was not detectable on the sidewalls or tips of the wires by electron beam energy dispersive spectroscopy (EDS). Ellipsometry measurements on a silicon on insulator wafer revealed that the Au etching procedure did not etch Si.

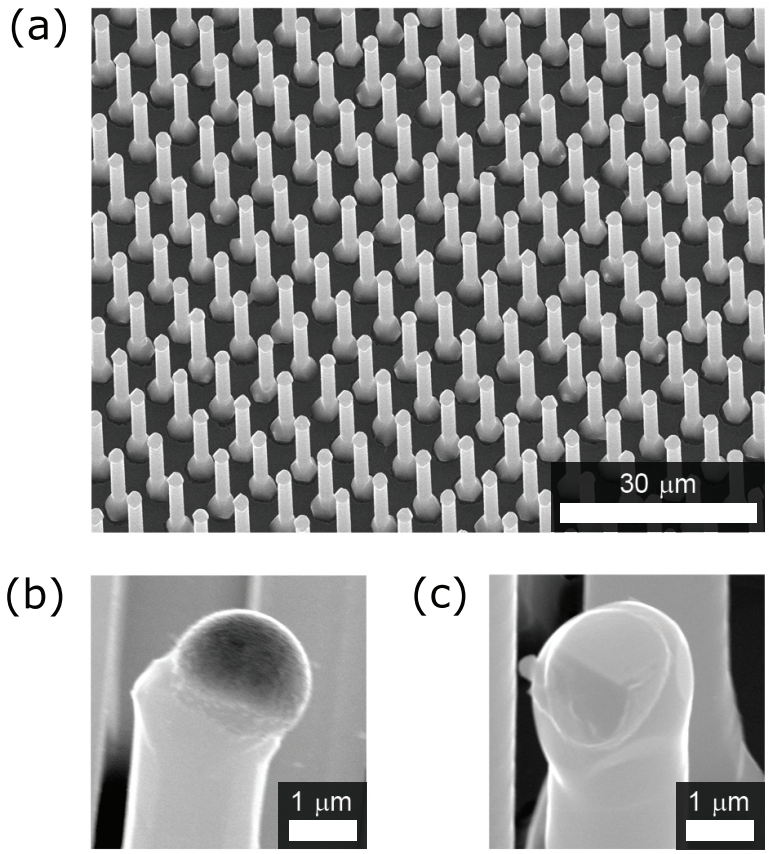


Figure 3.1. VLS-grown, Au-catalyzed, Si wire arrays were grown on a Si(111) substrate from Au catalyst that had been lithographically patterned and confined by a thermal oxide. Wires were tens of micrometers in length and 2 μm in diameter and grew in the <111> direction. (a) Tilted SEM image of a Au-etched wire array. (b) Tilted SEM image of a single Si wire tip, prior to Au removal. (c) Tilted SEM image of a single Si wire tip, after Au removal.

3.4 Secondary Ion Mass Spectrometry

3.4.1 General Principles

In secondary ion mass spectrometry (SIMS), a primary ion beam is used to ionize and sputter surface atoms from the sample, as depicted in Figure 3.2. The sputtered, ionized surface atoms (secondary ions) are then collected and analyzed in a mass spectrometer. To obtain accurate results, secondary ions are only collected from the center of the area over which the primary ion beam is rastered through the process of electronic gating (Fig 3.2a). Because it will be relevant to the discussion of the Au surface concentration later, it is worth noting that the process of sputtering produces an amorphized, well-mixed layer at the sample surface (Fig. 3.2b). In this work, a Cameca NanoSIMS-50L was used for secondary ion mass spectrometry (SIMS) analysis. The NanoSIMS-50L is a relatively new type of SIMS instrument (designed for use in the field of geology), which has the unique ability of being able to provide sub-micron spatial resolution.

To obtain an elements concentration (e.g., Au) from the secondary ion count rates, a relative sensitivity factor (RSF) is required, see Eqn. (3.1).

$$Au\ Concentration = RSF(atoms\ cm^{-3})\frac{^{197}Au\ count\ rate}{^{30}Si\ count\ rate} \tag{3.1}$$

The RSF is a function of the impurity and matrix secondary ion species sampled. To calculate the RSF, Au, B, and P standards (Charles Evans and Associates) with known Au, B, and P implant doses and depth profiles were used. A discussion of the calculated RSFs is presented in Appendix B.

3.4.2 Analysis Conditions

As a result of the complex ion optics necessary to achieve sub-micron spatial resolution in the NanoSIMS-50L, it was difficult to obtain similar beam conditions between successive sessions on the NanoSIMS. Optimal analysis conditions used a 1 μm^2 rastered area to predominantly confine the sputtered area within the wire, as seen for a ra-

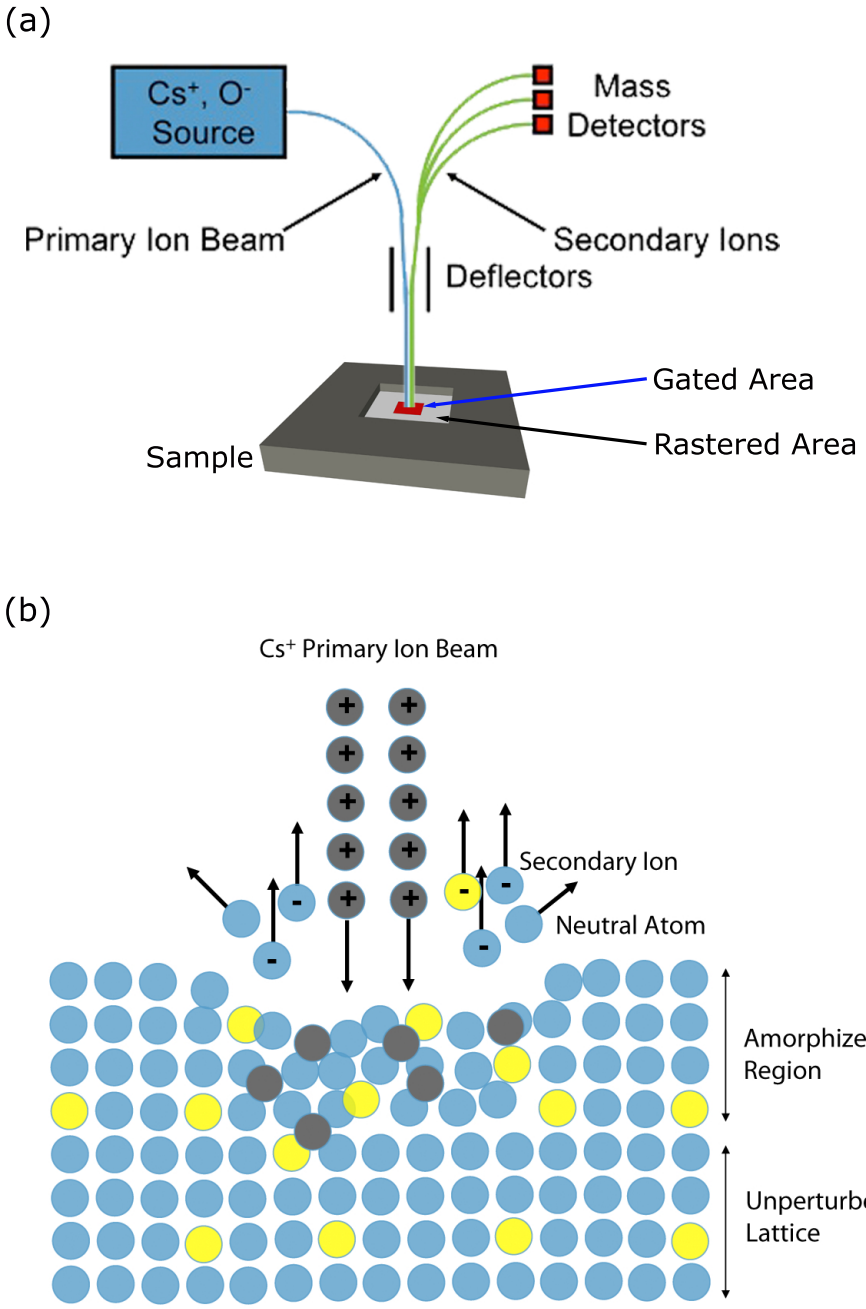


Figure 3.2. (a) Schematic of secondary ion mass spectrometry (SIMS) analysis technique. (b) Schematic of the sputtering process induced by the primary ion beam.

dially profiled wire in Figure 3.3. Electronic gating of the secondary ions was used to further limit the area sampled to the center 0.25 μm^2 of rastered area. However, because the beam diameter has a finite size (on the order of a couple hundred nm) some secondary ions will be collected from outside of the electronically gated area. A discussion of the beam currents used and the resulting sample sputtering rates as well as the differences in analysis conditions can be found in Appendix B. For all measurements, wires were analyzed at normal incidence with a 16 keV Cs+ primary ion beam.

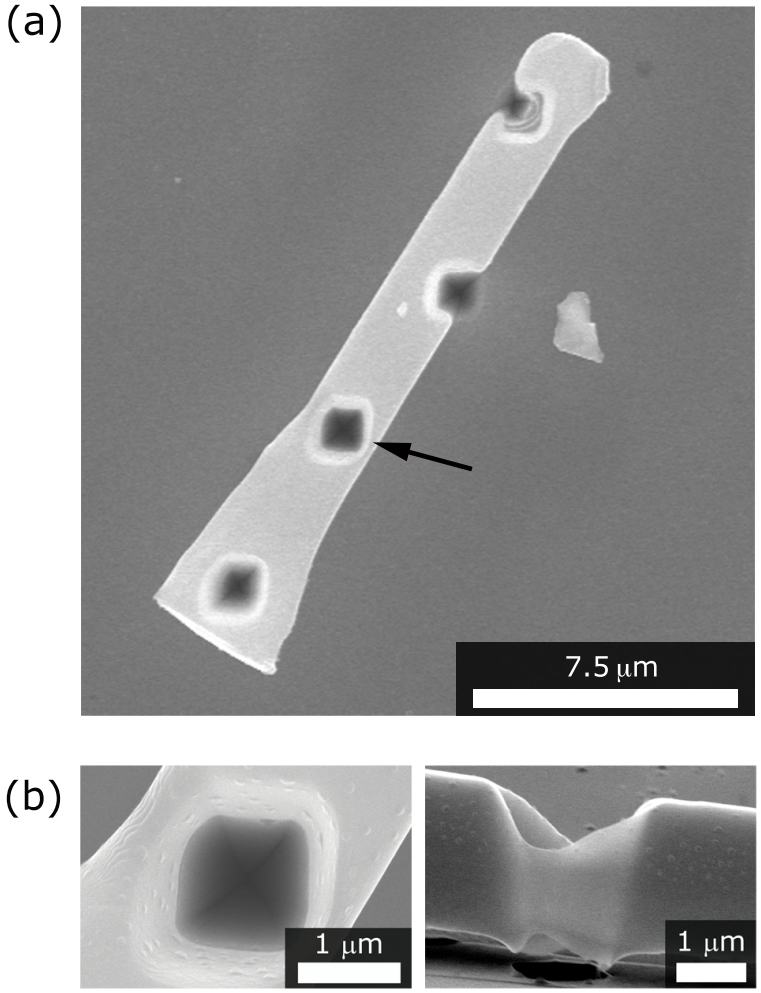


Figure 3.3. SEM images of a radially profiled wire. (a) Top-down image of an analyzed wire. (b) Top-down and side-view images of the analysis area indicated by the black arrow in (a).

3.5 Secondary Ion Count Rates

The measured count rates of ^{30}Si, ^{74}Ge, and ^{197}Au secondary ions versus depth for a Au-etched Si wire analyzed in the radial direction are displayed in Figure 3.4. The point at which the sputtered depth reached the back surface of the wire was clearly visible from the sharp rise in the ^{74}Ge count rate and the sharp fall in the ^{30}Si count rate. The ^{197}Au count rates within the bulk of the wires were often only a few counts per second (cps), but even a 1 cps ^{197}Au count rate is still significant compared to the average background ^{197}Au count rate of ~0.01 cps.

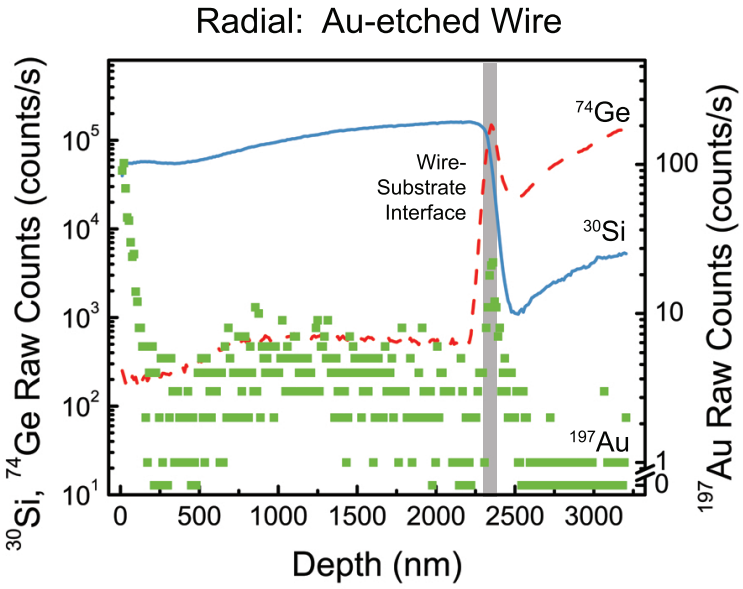


Figure 3.4. ^{30}Si, ^{74}Ge, and ^{197}Au secondary ion count rates for a radially profiled VLS-grown, Si wire. The vertical, grey band corresponds to the Si wire / Ge substrate interface, defined as the transition region from 16% to 84% of the maximum counts for either ^{30}Si or ^{74}Ge. The ^{30}Si and ^{74}Ge count rates are referred to the left-hand y-axis, while the ^{197}Au count rate is referred to the right-hand y-axis.

Two possible effects from the large sputtered depth to rastered length ratio were observed (in traditional SIMS this ratio would be ~1:100, whereas our analysis conditions are ~3:1). First, the measured ^{197}Au count rate was larger at the front surface

than the back surface of the wires. This difference in the ^{197}Au count rate produced the observed difference in the front and back surface Au concentrations, see below. While the origin of the lower ^{197}Au count rate at the back surface is unknown, we suspect that the large aspect ratio of the sputtered crater when sampling the back surface leads to a decreased secondary ion extraction efficiency. At the same time, the sidewalls of the sputtered volume are likely to contribute a greater number of secondary ions as the sputtered depth increases. Thus the measured Au concentration at the back surface is likely to have contributions from both the back surface of the wire and the bulk of the wire. However, the difference in the ^{197}Au count rate (and Au concentration) at the back surface may also be related to the discontinuous crystalline interface between the Si wire and the Ge substrate.

The second possible effect of the large sputtered depth to rastered length ratio was the roughly two-fold increase in the measured ^{30}Si counts as the wire was profiled in the radial direction. The increase in ^{30}Si counts is not well understood but may be related to the effective increase in sputtering area as the sputtered depth increased. Remember that the finite width and Gaussian profile of the primary ion beam will result in the collection of some counts from outside of the electronically gated area, and thus allow for an increase in the effective sputtering area to be observed.

3.6 Surface Au Concentration

Figure 3.5 displays the Au concentration profiles for un-etched and Au-etched, radially profiled wires. In both cases, the Au concentration is larger near the surface than in the bulk (center) of the wires. Comparing the un-etched and the Au-etched wires, a large difference in both the near-surface and bulk Au concentrations was observed. As the Au removal does not appreciably etch Si, the differences between the two Au concentration profiles are ascribed to a difference in the amount of Au present at the surface of the wires before and after the Au etch.

As a result of the amorphization and mixing at the sample surface during SIMS analysis (see Fig. 3.2),[37] a Au layer residing on the sidewalls of the wires is expected

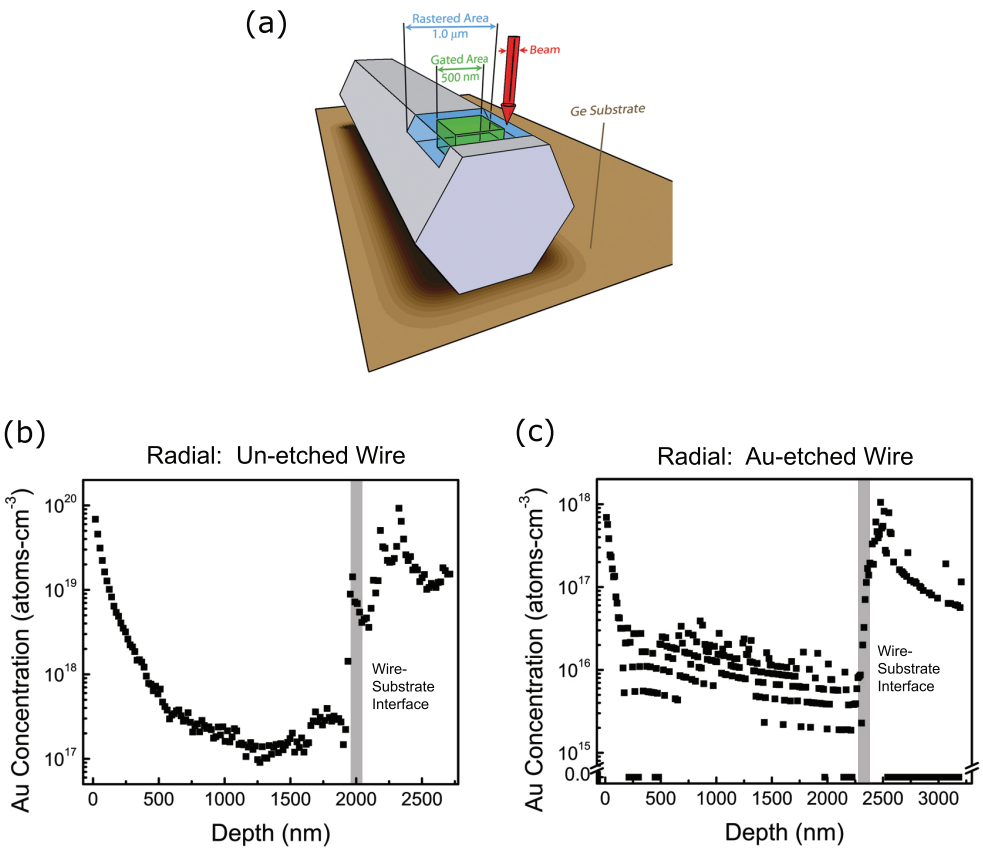


Figure 3.5. (a) Schematic of the radial-analysis geometry. (b) Radial Au concentration profile of an un-etched, VLS-grown, Si wire. (c) Radial Au concentration profile of a Au-etched, VLS-grown, Si wire. The apparent lines in the Au concentration profile, for the Au-etched wire, reflect the fact that integer counts per cycle time period were observed. In b and c, the vertical, grey band corresponds to the Si wire / Ge substrate interface.

to produce an exponential decay in the observed Au concentration profile. This is observed for the Au-etched wires, though a single exponential decay is less obvious for the un-etched wires. The perturbation from a single exponential decay for the un-etched wires is thought to arise from the use of a more diffuse primary ion beam during analysis of the un-etched wires (confer Appendix B).

Given the evidence for the observed near-surface Au concentration arising from Au on the sidewalls of the wires and a mechanism by which Au could be mixed to a greater depth within the wire, it is reasonable to estimate the surface Au concentration by integrating the Au concentration profile for the un-etched Si wire over the depth of the near-surface region (Fig. 3.5b). Integrating from 0 to 400 nm yields an estimate for the surface Au concentration on the order of 1 monolayer.

Further examining the observed surface Au concentration, one finds that it is larger at the front surface than at the back surface of the wires. This difference in the surface Au concentration seems unreasonable, given the radial symmetry of the wires. As discussed in Section 3.5, the high-aspect ratio of the sputtered volume when sampling the back surface of the wire may be producing this asymmetry in the surface Au concentration. It is important to note that the elevated Au concentration observed within the Ge wafer, seen for both un-etched and Au-etched wires, is an artifact of the decreased ^{30}Si count rate when sputtering the Ge wafer.

3.7 Bulk Au Concentration

3.7.1 Un-etched and Au-etched Wires

Comparing the observed bulk Au concentrations for the un-etched and Au-etched Si wires, one notes an order of magnitude higher Au concentration for the un-etched Si wire (Fig. 3.5b,c). Since the Au concentration profile for the un-etched wire exhibits a nearly constant value ($\sim 2 \times 10^{17}$ atoms cm^{-3}) between 500 and 2000 nm, the larger bulk Au concentration observed for this wire is unlikely to be due to Au from the sidewall of the wire that was mixed to a greater depth. Rather, it is likely that

a small fraction of secondary ions are being collected from outside of the rastered area. Given the high surface Au concentration, the collection of only one secondary ion in 200 from outside of the rastered area would produce the observed bulk Au concentration for the un-etched wire.

To obtain an estimate for the bulk Au concentration, the observed Au concentration was averaged over the first half of the Au-etched wires (not including the near-surface region), where the effects of the high-aspect ratio sputtered area should be smallest. For the five, Au-etched, radial profiles obtained, the average Au concentration within the bulk of the wire was $1.7 \pm 0.7 \times 10^{16}$ atoms cm^{-3}. The internal error of the measurement is estimated to be $< 15\%$.[†] Given the high surface Au concentration still present for the Au-etched wires and the potential to collect counts from the sidewalls of the wires, the average bulk Au concentration is best viewed as an upper limit.

3.7.2 Removing the Surface Au

As seen in Figure 3.6, an increased Au concentration at the surface of the wire is not observed with the addition of a KOH etch after the Au-etch to remove ∼20 nm of the surface Si. For the two KOH-etched wires, the average bulk Au concentrations were 1.2×10^{16} atoms cm^{-3} and 0.9×10^{16} atoms cm^{-3}, demonstrating that the bulk Au concentration is $\sim 1 \times 10^{16}$ atoms cm^{-3}. As before, the average was performed over the first half of the wire. However, the un-rastered analysis conditions (Appendix B) used to measure the KOH-etched wires resulted in a larger internal error for the bulk Au concentration. Therefore, we believe that the Au-etched data reflects the most conservative upper bound on the bulk Au concentration.

[†]The total internal error is found by taking the root of the sum of the squares of the internal errors. The two dominant internal errors arise from the counting statistics for the ^{197}Au secondary ions and the measurement of the average sputtered depth on the standard.

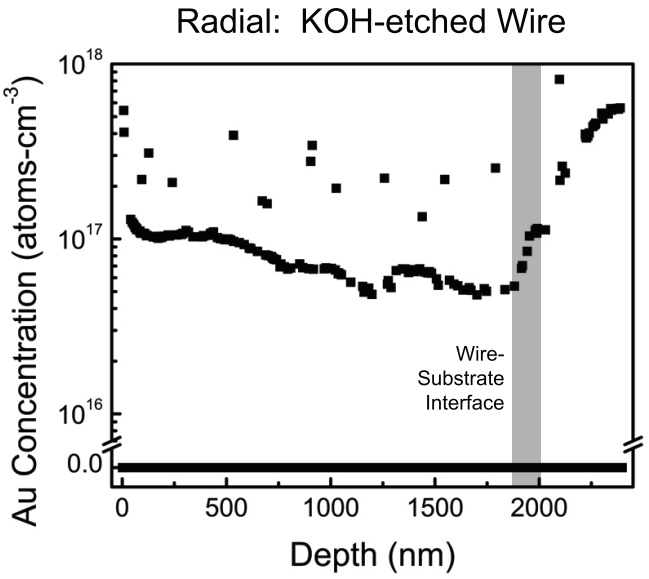


Figure 3.6. Radial Au concentration profile for a KOH-etched, Au-etched, VLS-grown Si wire. Note the observed zero Au concentration values in the Au concentration profile. The vertical, grey band corresponds to the Si wire / Ge substrate interface, defined as the transition region from 16% to 84% of the maximum counts for either ^{28}Si or ^{74}Ge.

3.8 Axial Au Concentration Profile

Figure 3.7 depicts the Au concentration profile observed when a Au-etched, Si wire was axially profiled. For the wire shown, the observed Au concentration decreased exponentially from 6×10^{18} atoms cm^{-3} at the surface to an average of 2.4×10^{16} atoms cm^{-3} within the bulk of the wire, while a second axially profiled wire exhibited a surface Au concentration of 8×10^{18} atoms cm^{-3} and an average bulk Au concentration of 5×10^{16} atoms cm^{-3}. As compared to the Au-etched, radially profiled wires, the observed surface Au concentrations for the Au-etched, axially profiled wires are a factor of 7 larger. This difference is reasonable given that the rapid cooling of the Au-Si alloy at the wire tip produces a Au-Si region that is difficult to etch (images not shown). In contrast, the average bulk Au concentration is expected to be simi-

lar for both the axially and the radially profiled wires. Though the axially profiled wires exhibited a few-fold higher bulk Au concentration, the sputtering of the wire sidewall that occurred in the axial geometry, shown in Figure 3.7c, would be capable of producing this difference.

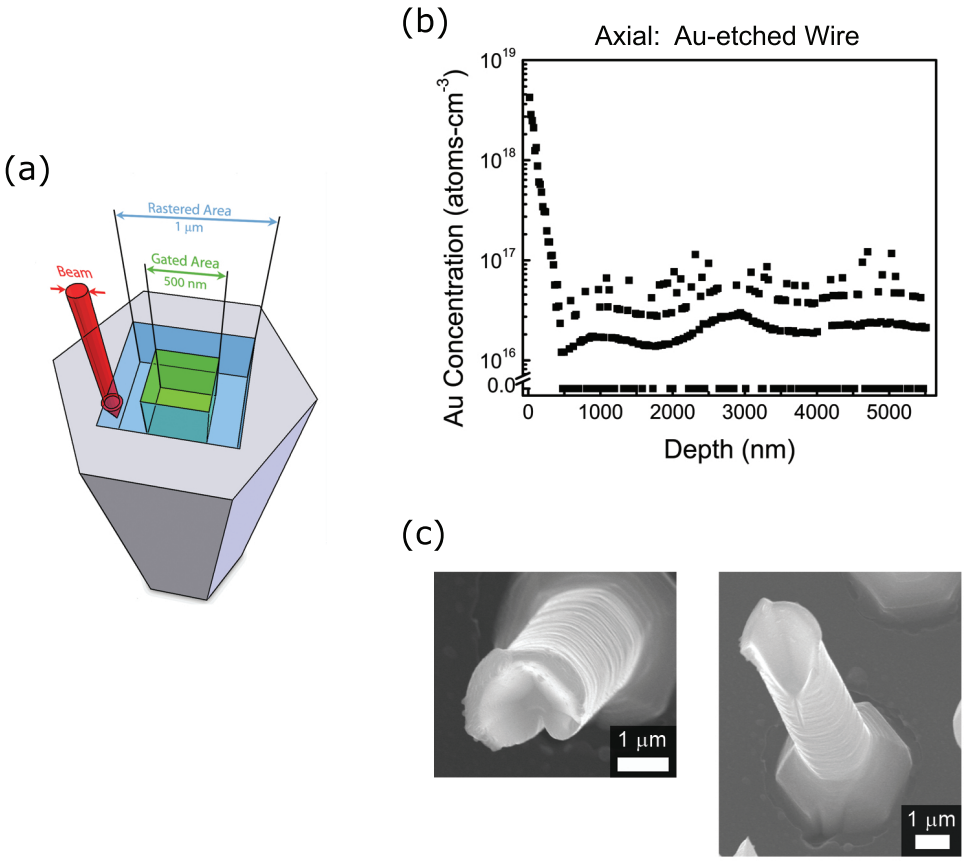


Figure 3.7. (a) Schematic of the axial-analysis geometry. (b) Axial Au concentration profile of a Au-etched, VLS-grown, Si wire. The apparent lines in the Au concentration profile reflect the fact that the detection limit was approached under our analysis conditions and that integer counts per cycle time period must be obtained. (c) Top-down and tilted SEM images of an axially profiled wire.

3.9 Discussion

3.9.1 Au Surface Phase

The increased Au concentration on the sidewalls of the wires may be a result of a Au-Si phase that is present during growth. The existence of a Au-Si phase on the sidewalls of VLS-grown, Au-catalyzed, Si wires during growth has been suggested previously for Si wires grown with Si_2H_6 as the Si precursor,[38] and Au clusters, possibly indicators of the existence of a Au-Si surface phase, have also been found on the surface of Si wires grown with SiH_4.[39, 40] Moreover, HAADF STEM results also revealed an increased Au concentration near the sidewalls of the wires for the MBE grown wires, though not for the CVD grown wires.[34, 35] In our work, for the two un-etched wires measured, the integrated amount of Au over the surface region was on the order of 1 monolayer, which would be consistent with the existence of a Au-Si surface phase.[41]

3.9.2 Bulk Au Concentration

Our observed upper limit on the bulk Au concentration of 1.7×10^{16} atoms cm^{-3} is comparable to the 1×10^{16} atoms cm^{-3} thermodynamic equilibrium concentration of Au in Si at the growth temperature of 1000 °C.[42] The observed upper limit represents a chemical sensitivity to Au in Si of ∼400 ppb. For the VLS growth method, the Au-Si phase diagram should determine the bulk Au concentration within the Si wire provided that the diffusion kinetics are sufficiently rapid to enable the establishment of the thermodynamic equilibrium Au concentration within the wire. Thus, we expect the bulk Au concentration within our 2 μm diameter Si wires to be representative of the bulk Au concentrations for Si wires ranging from tens of nm to many μm in diameter, as long as the Au-Si phase diagram is similar across the range of diameters and the wires are grown under our growth conditions.

In contrast, HAADF STEM results indicate a bulk Au concentration much greater than the thermodynamic equilibrium concentration of Au in Si for Au-catalyzed, Si

wires grown by CVD and MBE at temperatures of 450 °C and 500 °C, respectively, using SiH_4 as a Si precursor.[34, 35] While these differences can not yet be fully explained, it is possible that they are related to changes in the growth temperature and/or the Au-Si phase diagram between the various growth conditions and wire diameters. In particular, the much higher temperature of our growth conditions should prevent kinetic effects from controlling the incorporation of the VLS-catalyst into the Si wire at concentrations other than the thermodynamic equilibrium concentration.

3.9.3 Implications for Solar Cells - Catalyst Choice

A bulk Au concentration of 1.7×10^{16} atoms cm^{-3} in Si is expected to yield a minority-carrier recombination lifetime of 3 ns, for either electrons or holes as minority carriers.[42] In a radial-junction photovoltaic cell, with dopant concentrations of 10^{18} dopants cm^{-3} for both the n- and p-type regions, a 3 ns minority-carrier recombination lifetime would lead to minority-carrier diffusion lengths of 1 μm for both electrons and holes,[43] which agrees reasonably well with the 2 μm effective hole diffusion length that has recently been observed by scanning photocurrent microscopy on similar VLS-grown, Au-catalyzed, Si wires with $N_D = 10^{18}$ atoms cm^{-3}.[44] As shown in Figure 3.8, theoretical modeling predicts that solar cells with efficiencies of 13.4% should be possible with minority-carrier diffusion lengths of 2 μm. However, if other VLS-catalysts are also incorporated at their thermodynamic equilibrium concentration in Si using our growth conditions, then the use of Cu as a catalyst should result in minority-carrier diffusion lengths of at least 10 μm,[45] enabling the possibility for 17.5% efficient solar cells.

3.10 Measuring B and P Concentrations

In addition to quantifying the Au concentration in VLS-grown, Si microwires, SIMS measurements were made on Si microwires to demonstrate the ability to characterize radial p-n junctions. These radial p-n junctions were fabricated by performing a P thermal diffusion, followed by a thermal drive-in (to ensure a uniform P concentration

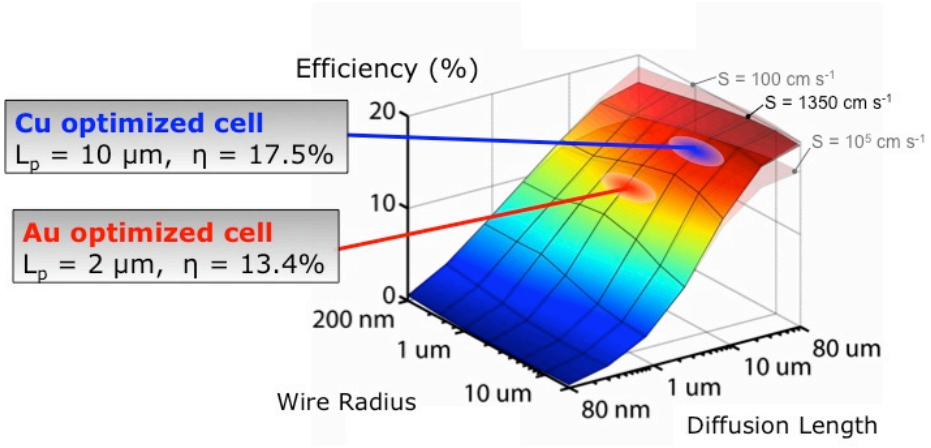


Figure 3.8. Theoretically modeled solar cell efficiencies as a function of wire radius and diffusion length. Cells with the expected minority-carrier diffusion length for Cu-catalyzed and Au-catalyzed microwires are highlighted, assuming that the catalyst is incorporated at its thermodynamic equilibrium concentration in Si at the growth temperature.

in the radial direction), and completed with a B thermal diffusion (to form a heavily doped emitter).[26] As seen in Figure 3.9, the P concentration is quite uniform in the radial direction with an average concentration of $\sim 8 \times 10^{17}$ atoms cm^{-3}. The observed uniformity indicates that the thermal drive-in step is effective, and the average P concentration is close to the desired P concentration based upon theoretical modeling.[16] The measured B concentration is greater than the P concentration near the front surface of the wire and well below the P concentration in the wire bulk, indicating that the B thermal diffusion is effective. Similar to the radial Au concentration profile, the measured B concentration at the back surface of the wire is lower than the measured B concentration at the front surface of the wire. In summary, these results indicate that p-n junction profiles should be resolvable using the NanoSIMS for B and P concentrations $> 5 \times 10^{17}$ atoms cm^{-3}.

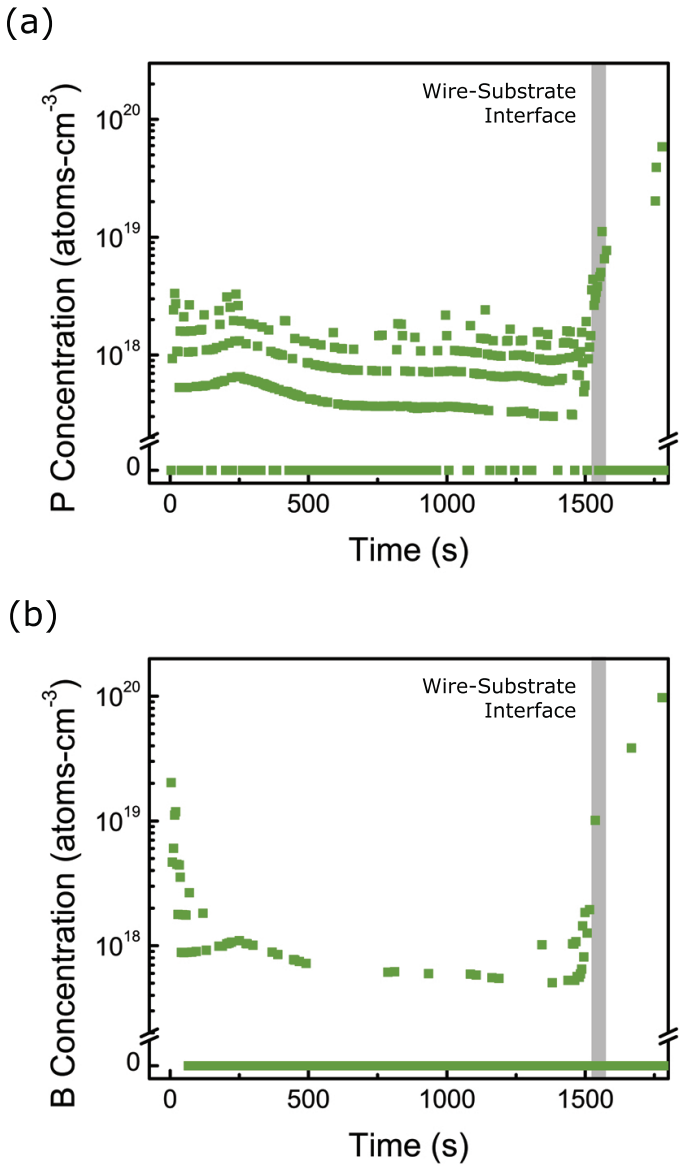


Figure 3.9. (a) Radial P concentration profile in a Si microwire after a thermal P diffusion and drive-in. (b) Radial B concentration profile in a Si microwire after a thermal B diffusion.

3.11 Conclusion

In this chapter we have shown that secondary ion mass spectrometry can be used to quantitatively measure the bulk Au concentration in VLS-grown Si wires. The measured bulk Au concentration is found to be in good agreement with the thermodynamic equilibrium concentration of Au in Si at the growth temperature. Solar cells with efficiencies of 13.4% should be possible using Au as the VLS-catalyst, and solar cells with markedly higher efficiencies of 17.5% should be possible using Cu as the VLS-catalyst, assuming that Cu is also incorporated at its thermodynamic equilibrium concentration in Si at the growth temperature. We have also shown that a simple Au-etch was not sufficient to remove all of the surface Au, but that a KOH-etch to remove $\sim$20 nm of the surface Si leads to a Au-free Si surface. Lastly, it was shown that the NanoSIMS should be able to characterize p-n junctions with B and P concentrations $> 5 \times 10^{17}$ atoms cm^{-3}.

Chapter 4

Doping of Si Microwires

4.1 Introduction

This chapter discusses the use of thermal diffusion and in-situ doping to control the electrically active dopant concentrations in Si wire devices. Thermal dopant diffusion was found to work well for producing a large dopant concentration ($\sim 10^{19}$ cm^{-3}) at the wire surface, while in-situ doping with BCl_3 allowed for the electrically active dopant concentration to be varied from 8×10^{15} cm^{-3} to 4×10^{19} cm^{-3} in the as-grown wire. In-situ doping was critical for the study of minority-carrier diffusion lengths (Ch. 5.), and both in-situ doping and thermal dopant diffusion were essential for the fabrication of efficient Si microwire-arrays solar cells (Ch 6.).

4.2 Background

4.2.1 Optimal Base Doping

Control of the base (wire core) electrically active dopant concentration is of particular importance when trying to fabricate microwire solar cells with radial p-n junctions. As shown in Figure 4.1, optimal doping of the wire base is required to avoid parasitic recombination in the wire base. If the base doping is too low (Fig. 4.1a), the heavy doping of the emitter (wire shell) will deplete the entire core of the wire. Because recombination in the depletion region is higher than in the quasi-neutral region (un-depleted regions of emitter and base), majority-carriers are now likely to recombine before being collected at the contact at the base of the wire. (Remember that the

wires have large wire length to wire diameter ratios, ∼1/100.) However, if the base doping is too high (Fig. 4.1c), it can lead to a reduction of the minority-carrier diffusion length to the point where photo-generated minority-carriers recombine before reaching the p-n junction. In the case of degenerate (very high, $> 10^{19}$ cm^{-3}) base doping, a tunnel-junction may form between the base and emitter, eliminating the rectifying properties of the p-n junction. Thus, precise control of the base doping is critical for ensuring an optimal base doping (Fig. 4.1b) so that undue recombination of the photo-excited carriers does not occur.

4.2.2 Literature

Thermal diffusion doping, in-situ doping, and ion-implantation have been used to dope Si wires.[22, 46, 47] In particular, in-situ doping has been studied using p-type (trimethylboron and diborane) and n-type (phosphine) dopants in Si wires grown using SiH_4.[22, 48, 49] However, to the best of our knowledge, no comprehensive doping studies have been undertaken for Si wires grown using a $SiCl_4$ precursor.

4.3 Thermal Dopant Diffusion

Initial attempts to control the electrically active dopant concentrations in the Si wires were made using thermal dopant diffusion. As depicted in Figure 4.2, either B or P source wafers were placed in close proximity to Si wire arrays and then heated in a tube furnace to a temperature between 850-950 °C under a stream of N_2.

During the thermal diffusion, either boric oxides or phosphorous oxides were transferred to the Si wires. Upon adsorption to the Si, the boric or phosphorous oxide decomposes, resulting in the formation of free B and P atoms and a SiO_x layer. As was shown in Figure 3.8a, this produced a thin region of doping at the wire surface. As will be shown in Chapter 6, the creation of a n^+-Si emitter through a thermal phosphorous diffusion helped lead to the fabrication of efficient solar cells.

To create a uniform base doping, a thermal drive-in of the dopant species is required. For B doping this requires heating the Si microwires for 5 hrs at 1100 °C

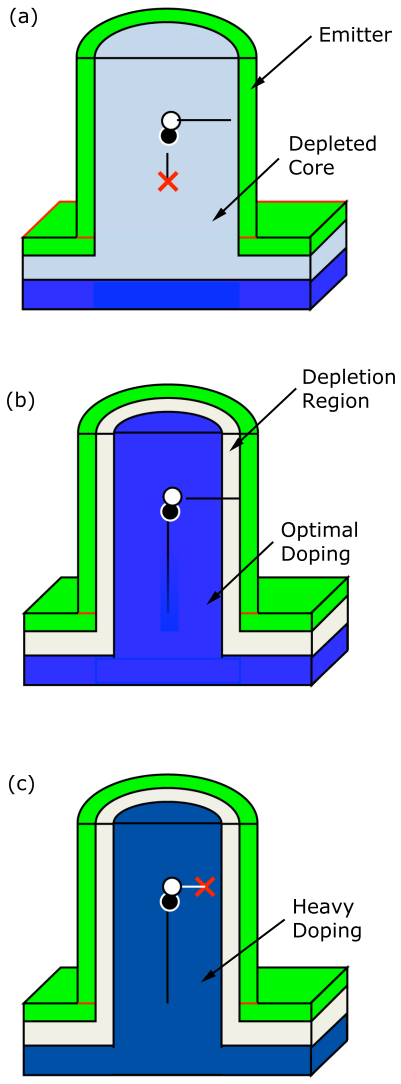


Figure 4.1. Cross-sectional schematic of carrier collection/recombination in wires with radial p-n junction where (a) the base doping is too small, (b) the base doping is optimal, and (c) the base doping is too large.

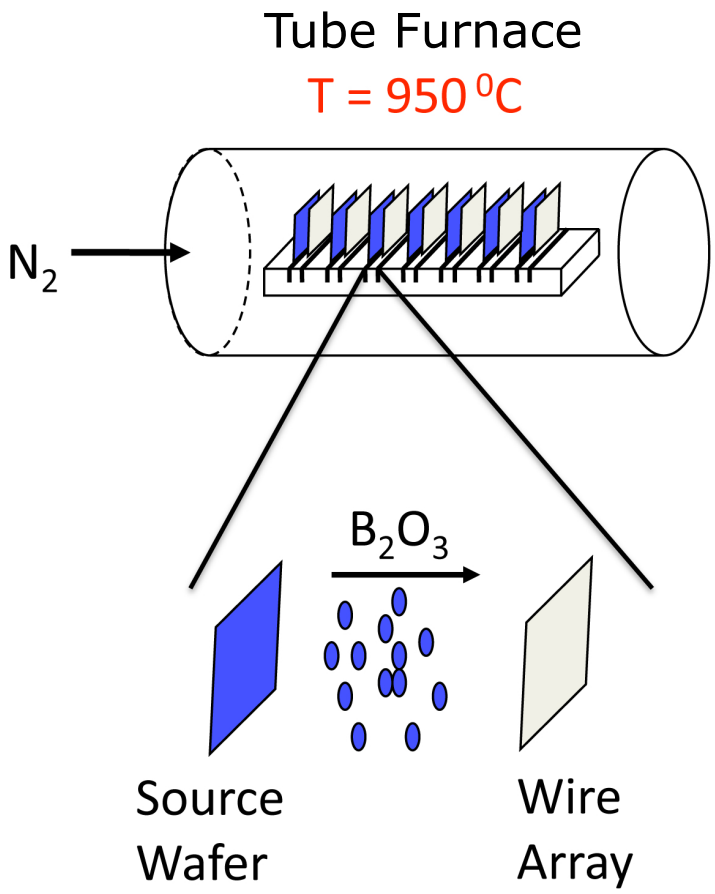


Figure 4.2. Schematic of B thermal dopant diffusion.

to ensure complete diffusion of the B atoms across the radius of the wire (or 3 hrs at 1100 °C for P species.) Though not desirable in a commercial process because of the costs associated with processing steps that require high-temperatures, a thermal drive-in is an effective method for producing a uniform base doping as was shown in Figure 3.9a.

Finally, a schematic for the formation of a radial p-n junction via thermal diffusion is shown below in Figure 4.3. After wire growth, the base thermal diffusion is performed, followed by the base drive-in and then finally an emitter thermal diffusion. Thus, it is clear that two high-temperature processing steps could be removed, if in-situ doping during growth could be used to create a uniform base profile.

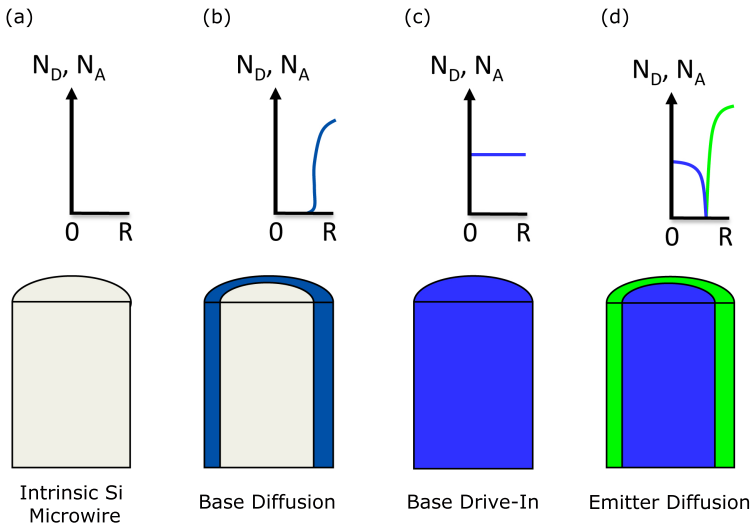


Figure 4.3. Schematic of the radial p-n junction fabrication process using thermal dopant diffusion. Top, graphs of the net electrically active dopant concentration.

4.4 In-Situ Doping

To evaluate the possibility of in-situ doping, BCl_3 was added to the $SiCl_4$ and H_2 gas stream during the VLS-growth of the Si microwires. Upon the addition of BCl_3 no change in wire morphology or array fidelity was observed, as seen in Figure 4.4.

By removing the wires from the growth substrate and depositing them onto a Si wafer with an insulating Si_3N_4 coating,[44] photolithographic patterning could be used to deposit Al contacts on individual Si microwires for both 2 and 4-point current-voltage measurements, as shown in Figure 4.5.

Initial current-voltage measurements on the Si microwires grown in the presence of BCl_3 were made in a back-gated field effect transistor geometry as shown in Figure 4.6. By applying a negative bias to the n^+-Si substrate, a negative charge is introduced at the n^+-Si/Si_3N_4 interface and a positive charge is induced at the bottom surface of the Si microwire. For p-type Si microwires, this positive charge at the bottom surface of the wire results in an accumulation layer of majority-carriers, thereby resulting in a slightly decreased wire resistivity. However, when a positive bias is applied to the

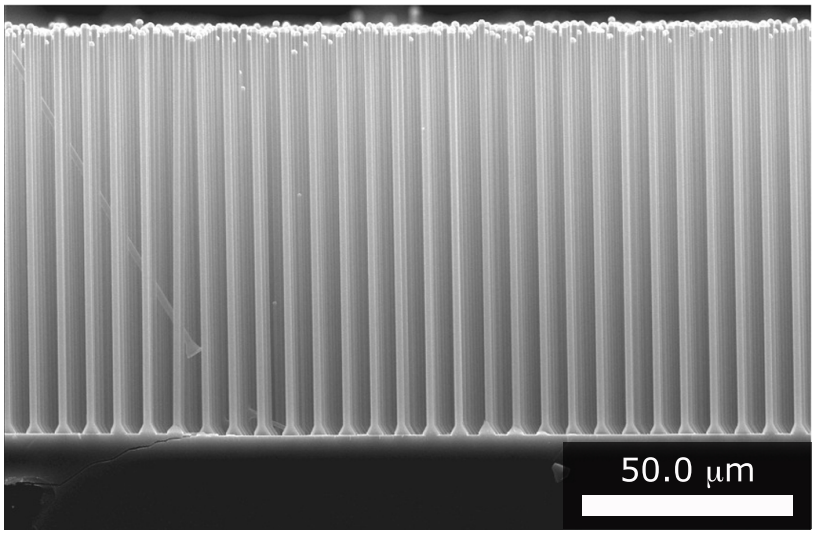


Figure 4.4. SEM image of a wire array grown with in-situ BCl_3 doping.

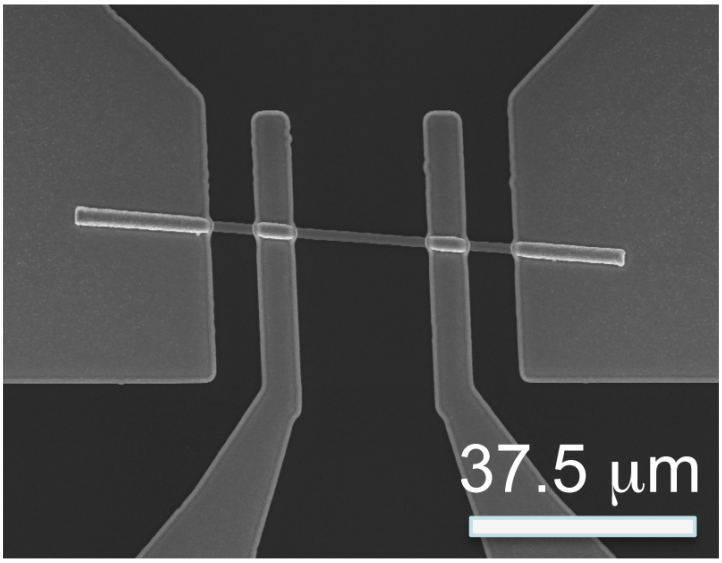


Figure 4.5. SEM image of a Si microwire with four Al contacts.

n^+-Si substrate, a negative charge is induced at the bottom surface of the wire. This negative charge will produce a depletion layer in p-type Si microwires and result in a slightly increased wire resistivity. As seen in Figure 4.7, this is exactly the type of behavior we observe for Si microwires grown in the presence of BCl_3.

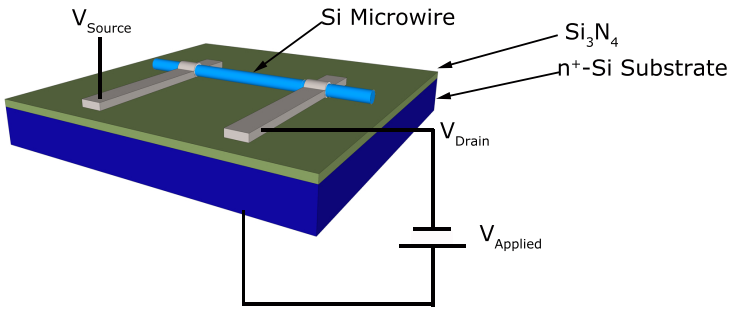


Figure 4.6. Schematic of back-gated field effect transistor measurement.

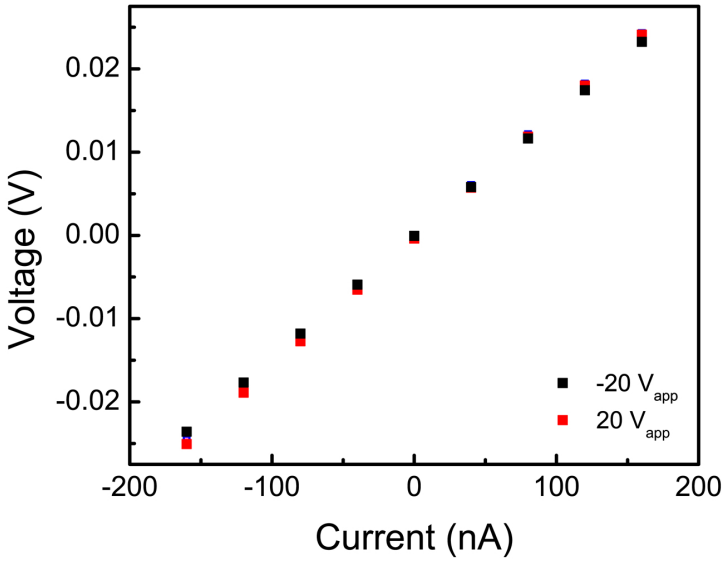


Figure 4.7. Voltage-current behavior of a Si microwire grown with BCl_3 in-situ doping.

Having demonstrated that the addition of BCl_3 to the reactant stream resulted in

the expected p-type behavior, four-point I-V measurements were used to measure the wire resistance as a function of the BCl_3 concentration in the gas phase. Four-point I-V measurements, as opposed to two-point I-V measurements, were made so that the contact resistance could be eliminated from the measured wire resistance. From the measured wire resistance and cross-sectional area (as measured by SEM), a wire resistivity was calculated. The wire resistivity was then used to infer the electrically active dopant concentration.[50]

Figure 4.8 plots the electrically active dopant concentration as a function of the BCl_3 concentration in the gas phase. By varying the gas phase concentration from 0.5 to 200 ppm, the electrically active dopant concentration could be varied from 8×10^{15} cm^{-3} to 4×10^{19} cm^{-3}. Cu-catalyzed, microwires grown without the presence of BCl_3 were not observed to pass current under reasonable biases, implying that any electrically active dopants were present in concentrations $<< 10^{14}$ cm^{-3}.

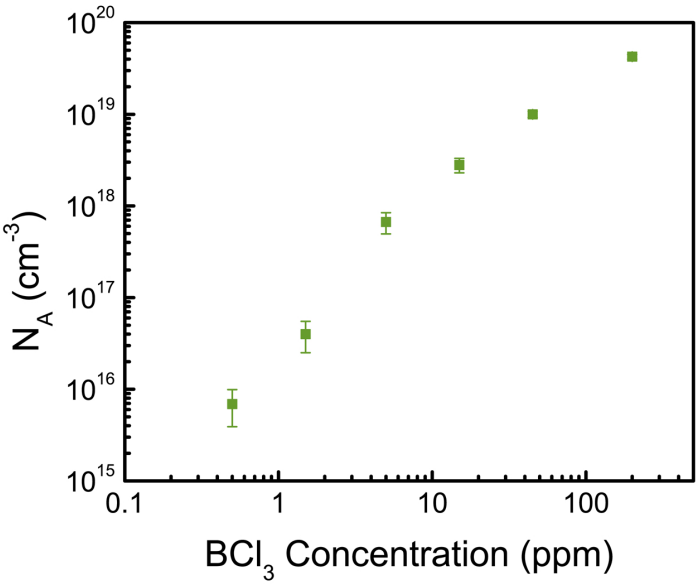


Figure 4.8. Electrically active doping concentration as a function of BCl_3 concentration in the gas phase. Error bars are the standard error.

4.5 Total Dopant Concentration and Electrically Active Dopant Fraction

In addition to control of the electrically active dopant concentration, the demonstration of a high electrically active dopant fraction (electrically active dopant concentration / total dopant concentration) is desirable. A low (< 0.1) electrically active dopant fraction is undesirable as it will lead to increased carrier recombination without providing the desired electrical properties.

Initial attempts to measure the *total* dopant concentration were made using both secondary ion mass spectrometry (SIMS) and inductively coupled plasma mass spectrometry (ICP-MS). Using SIMS an attempt was made to measure the B concentration for two different doping concentrations. However, the analysis conditions chosen (an O^- primary ion beam was used instead of the Cs^+ primary ion beam in an attempt to measure the Cu concentration in Cu-catalyzed wires) did not result in the generation of enough secondary ions to quantitatively measure the B concentration.

As SIMS measurements on the Cameca NanoSIMS-50L were quite time intensive, ICP-MS was explored as a potentially quicker method for measuring the total dopant concentration in the wires. The challenge with ICP-MS is that it requires $\sim$1 mg of sample material. While the mass of a single wire is $<<$ 1 mg, the mass of a wire array is $\sim$1 mg. Because of the homogenous nature of the wire arrays, we felt comfortable that the average total dopant concentration in the wire array would be quite close to the total dopant concentration in a given wire. Table 4.5 reports our initial ICP-MS findings. (The concentration of the species of interest can be calculated in one of two ways using ICP-MS.) In agreement with the measured electrically active B concentration, the total B concentration was observed to increase from samples 598 to 601. Additionally, the order of magnitude agreement between the measured total B concentration and the electrically active B concentration suggests that the electrically active dopant fraction is on the order of 1. While these results demonstrate the promise of ICP-MS, the fact that the measured total B concentration was at times lower than the measured electrically active B concentration is likely indicative of error

in the ICP-MS measurement, and further development of ICP-MS sample preparation and data collection is necessary to obtain quantitative results.

Table 4.1. Boron concentration measured by ICP-MS.

	598	**599**	**600**	**601**
[B] calculated from semi-quantitative analysis (cm^{-3})	5.0×10^{16}	1.5×10^{17}	4.0×10^{17}	1.3×10^{18}
[B] calculated from concentration standards and sample mass (cm^{-3})	2.2×10^{17}	5.0×10^{17}	1.3×10^{18}	4.0×10^{18}
N_A (cm^{-3})	4.0×10^{16}	6.7×10^{17}	2.8×10^{18}	1.0×10^{19}

4.6 Electrically Active B Concentration in Ni-Catalyzed Wires

The use of BCl_3 as an in-situ dopant was also studied for Si wires grown from a Ni-catalyst.[51] The Ni-catalyzed, Si wires were grown under the same growth conditions as the Cu-catalyzed, Si wires, and the preparation of single wire devices for electrical characterization (wire placement onto a Si wafer with an insulating coating, followed by photolithography, contact deposition and contact annealing) was also the same. However, unlike for the Cu-catalyzed wires, four point current-voltage measurements were only linear (and therefore meaningful) for the most heavily doped wires. For the most heavily doped, Ni-catalyzed wire an electrically active B concentration of 4×10^{17} cm^{-3} was inferred.

The non-linearity of the of four-point current-voltage measurements for the more lightly doped Ni-catalyzed wires suggests that the contact resistance to these wires was quite high. As seen in Figure 4.9, two point current-voltage measurements were roughly linear but exhibited no trend with increasing dopant concentration (except

for the Ni-catalyzed wires grown under the highest BCl_3 concentration, which exhibited a significantly decreased resistance as expected), suggesting that the contact resistance was large and that it dominated the measured resistance. Modifications to the contact fabrication procedure (chemical etching prior to metal deposition, contact anneals of increased temperature and time) were made in an attempt to reduce the contact resistance, but no appreciable change in the measured resistances was observed. Though we do not know for sure, we suspect that the observed large contact resistances arose from a low electrically active B concentration in the wires (it can be quite difficult to obtain low resistance contacts to lightly doped, $< 10^{15}$ cm^{-3}, Si). If so this poses the curious question as to why the electrically active B concentration increased so dramatically between 10 and 45 ppm of BCl_3 in the gas phase. One possible explanation is that the Ni-Si alloy (the catalyst phase may actually be a Ni-silicide) acts as a B sink. Thus, the B concentration in the wire remains low/negligible until the B sink is saturated, at which point B enters the wire as expected. If so, this would indicate that it could be quite difficult to control the electrically active B concentration in Ni-catalyzed Si wires below $\sim 4 \times 10^{17}$ cm^{-3}.

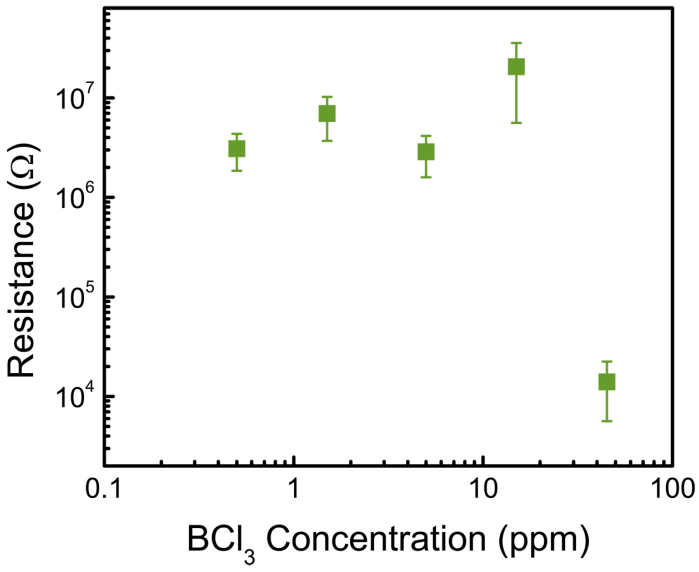


Figure 4.9. Resistance of Ni-catalyzed Si wires as a function of the BCl_3 concentration in the gas phase. Error bars are the standard error.

4.7 Conclusion

In this chapter we have demonstrated the ability to controllably dope Si wires. Thru the combination of BCl_3 in-situ doping to moderately dope the as grown Si wires and a post-growth thermal phosphorous diffusion to create a heavily doped wire shell, the fabrication of radial p-n junctions is now possible.

Chapter 5

Minority-Carrier Diffusion Lengths in Cu-Catalyzed Si Wires

5.1 Introduction

With the ability to control the active doping concentration in Cu-catalyzed, Si microwires (Ch. 4), we turned our attention to the fabrication of devices that would allow us to study the minority-carrier diffusion length. As alluded to in section 3.9.2, the minority-carrier diffusion length is a critical indicator of material quality and plays a significant role in determining photovoltaic performance. To measure the minority-carrier diffusion length, scanning photocurrent microscopy measurements were made on single wire devices exhibiting rectifying behavior. In dark, ambient conditions, the effective minority-carrier diffusion length ($L_{n,eff}$) was limited by surface recombination to a value of ≤ 0.7 μm. However, a value of $L_{n,eff} = 10.5 \pm 1$ μm was measured under broad area illumination (low-level injection conditions). The minority-carrier diffusion length observed under broad-area illumination is consistent with filling of the surface states of the Si wires by photogenerated carriers and has important implications for the design of high-efficiency solar cells from arrays of Si wires synthesized by the VLS-growth method.

5.2 Background

Kelzenberg et al. measured minority-carrier diffusion lengths from 2 μm to 4 μm in 900 nm diameter, Au-catalyzed, Si wires.[44] These values are considerably smaller

than the diffusion length in high-purity bulk Si. However, they are in good agreement with the minority-carrier diffusion length expected for Si with a Au concentration of 1.7×10^{16} cm^{-3}, the measured Au concentration in the Si wires, see Chapter 3. (Au is a highly effective recombination center in bulk Si.) As discussed in Chapter 3, the measured Au concentration in the Si wires is in good agreement with the thermodynamic equilibrium concentration of Au in Si at the growth temperature of 1000 °C. Assuming that the Cu concentration in the Si wire is also at its thermodynamic equilibrium concentration in Si at the growth temperature, Cu-catalyzed Si wires would be expected to exhibit bulk minority-carrier diffusion lengths of ∼20 μm.[45] Thus, by switching from the use of a Au VLS-catalyst to a Cu VLS-catalyst, we hope to see a significant enhancement in the bulk minority-carrier diffusion length.

5.3 Scanning Photocurrent Microscopy

As depicted in Figure 5.1, scanning photocurrent microscopy (SPCM) produces a map of a wire's local photocurrent response by scanning the wire beneath a focused illumination source while the photocurrent is measured. For wires with a rectifying junction and sufficiently high doping, such that the minority-carrier transport is dominated by carrier diffusion and not carrier drift, the minority-carrier diffusion length can be extracted using Eqn. (5.1), where (x_{Jxn}-x) is the distance between the rectifying contact and the laser illumination.[50]

$$J_{ph} \propto e^{\frac{-(x_{Jxn}-x)}{L_{n,eff}}} \tag{5.1}$$

5.4 Diode Fabrication

Having demonstrated the ability to selectively place metal contacts on the Si wires,[44] we felt that the most direct route to obtaining Si microwires with rectifying behavior would be to form one Ohmic metal contact and one rectifying metal contact through the use of a two-step photolithography process. Though the scientific literature sug-

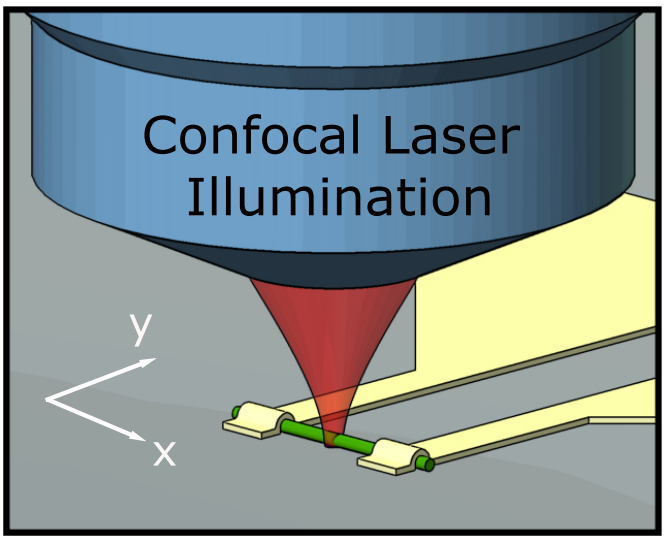


Figure 5.1. In scanning photocurrent microscopy, the short-circuit current is measured as the sample (the wire) is rastered beneath a confocally focused laser beam.

gests that a few metals (Ca, Cr, Mg, and Ti) should exhibit barrier-heights > 0.6 eV to p-Si,[50] the fabrication of good rectifying devices proved difficult in practice. However, thoroughly scanning the literature revealed the use of Al metal-insulator-silicon (MIS) contacts as rectifying junctions in silicon solar cells.[52] In these solar cells, the use of a thin layer (3-9 nm) of SiO_2 (either native or thermally grown) between p-Si and Al resulted in rectifying contacts with ideality factors of 1.4.

As described in Ch. 2 and Ch. 4, Cu-catalyzed Si wires were grown at 1000 °C and 1 atm from a 500:10 sccm gaseous H_2:$SiCl_4$ stream using BCl_3 to in-situ dope the wires. Four-point probe measurements of the wires studied in this chapter indicated that the wires were p-type with a resistivity of 0.19 ± 0.02 Ω cm. This value corresponds to an acceptor concentration, N_A, of (1.05 ± 0.15) × 10^{17} cm^{-3}, assuming a bulk hole mobility (3.1 × 10^2 cm^2 V^{-1} s^{-1}) for Si. Prior to SPCM characterization, a 5:1:1 (by volume) mixture of deionized H_2O (18 MΩ cm resistivity):NH_4OH(29%):H_2O_2(30%) (RCA1) was used to remove any organic con-

tamination, and a 6:1:1 (by volume) mixture of deionized H_2O:HCl(37%):H_2O_2 (RCA2) was used to remove residual Cu. The chemical/native oxide was then removed by etching the wires for 15 s in Buffer HF Improved (Transene Inc.). A native oxide was then grown on the wires by exposing them to atmosphere for 3.5 days.

The Si wires were then removed from the growth substrate and dispersed onto a Si_3N_4-coated Si(100) wafer. A two-step photolithography process was used to pattern an Ohmic and a rectifying contact onto individual Si wires. Rectifying contacts were formed by sputtering Al onto the native oxide of the p-Si wires. Ohmic contacts were formed by sputtering Al (with 1% Si) onto the p-Si wires, after a 15 s etch in Buffer HF Improved, to remove the native oxide. After contact deposition, a contact anneal was performed at 300 °C for 10 min in forming gas (5% H_2 in N_2).

Figure 5.2 illustrates the observed rectifying behavior for a device with an ideality factor of 1.8 and an effective barrier height of 0.6 eV. Ideality factors ranged from 1.4 to 3.1, and the effective barrier height ranged from 0.4 to 0.7 eV. The inset of Fig. 5.2 displays an optical microscope image of the device. The bright spot near the center of the wire corresponds to the area illuminated by the laser. The other two spots are artifacts that arose from reflections in the microscope optics.

5.5 Minority-Carrier Diffusion Lengths

5.5.1 Measurement Conditions

SPCM measurements were made using a WiTec scanning near-field optical microscope (SNOM) in confocal mode. Local illumination was provided by a 650 nm laser that was chopped at 30 Hz to allow for the use of a lock-in amplifier and focused through a 20x objective to produce a diffraction-limited spot-size of 0.4 μm. Broad-area illumination was provided by the microscope light (color temperature = 3200 K). By using a photodiode to measure the illumination power density, the carrier generation density for both illumination sources was calculated to be a factor of 40 less than the equilibrium hole concentration of 1.0×10^{17} cm^{-3}, thus satisfying the requirement for

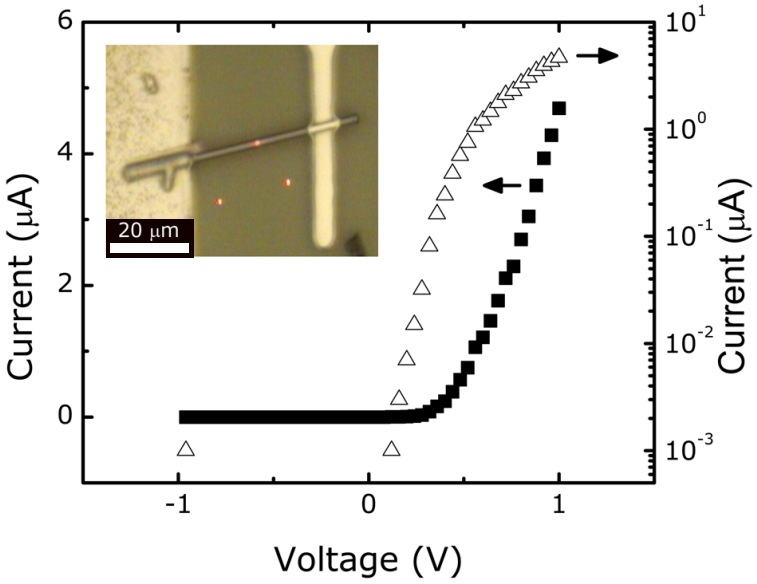


Figure 5.2. Current-voltage sweep of a 2.0 μm diameter Si wire device. Inset, optical microscope image of the measured device; the Ohmic contact is on the left and the Al MIS contact is on the right. The laser illumination spot can be seen in the center of the wire.

low-level-injection (LLI) illumination conditions (see Appendix C). The photocurrent from the MIS rectifying contact was detected by a pre-amplifier connected to a lock-in amplifier.[44] For measurements at an applied bias, the Ohmic contact was connected to a DC voltage source.

5.5.2 Photocurrent Response

Figure 5.3 provides (a) an SEM image of and (b-d) zero-bias SPCM images for the devices from 5.2. In the dark (Fig. 5.3b), a small photocurrent (note respective scale-bars) was observed along the wire, as well as on the MIS rectifying contact in the regions immediately above and below the wire. The photocurrent above and below the wire on the MIS contact is believed to arise from an optically thin coating of Al along the sidewall of the wire that formed as a result of the directional nature of sputtering and the large ratio of the wire diameter to the thickness of the contact. Under broad-area illumination (Fig. 5.3c), a much larger signal, that extended

greater than half the length of the device, was observed. Interestingly, a photocurrent response comparable to the one observed under broad-area illumination was observed for dark measurements made immediately after exposure to broad-area illumination (Fig. 5.3d).

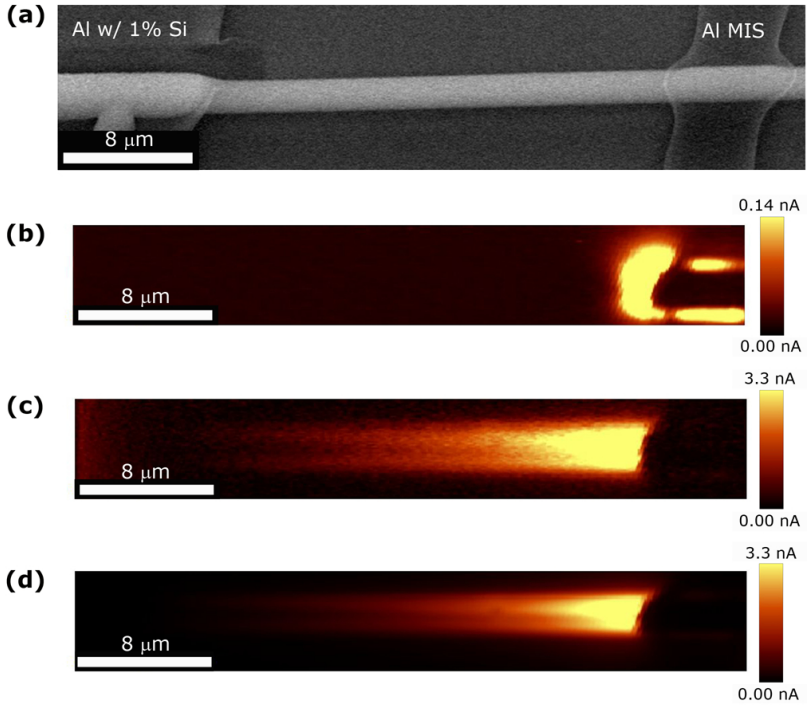


Figure 5.3. (a) SEM image of the device of Fig.5.2. (b) Scanning photocurrent microscopy (SPCM) image of the device measured in the dark. (c) SPCM image of the device measured under low-level-injection, broad-area illumination. (d) SPCM image of the device measured in the dark for a measurement started ∼5 s after exposure to broad-area illumination.

To further characterize the observed transient surface passivation of Figure 5.3d, photocurrent measurements were made in the dark 0 min, 10 min, 20 min and 65 min after exposure to the broad-area illumination, as shown in Figure 5.4. Note that in Fig. 5.4 the scale bars are all the same, unlike in Fig. 5.3. The time-dependent decay in the dark photocurrent response was clearly evident. Similarly, the observed increase in photocurrent-response with broad-area illumination is not instantaneous

(data not shown.) The measurement time for a single SPCM image was 4 min and 14 s.

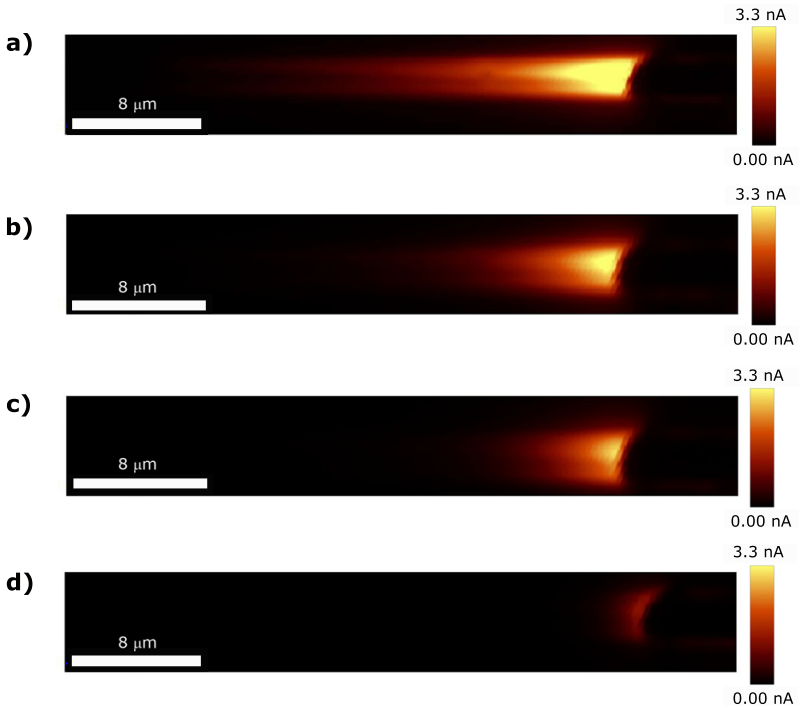


Figure 5.4. Dark SPCM images (a) 0 min (b) 10 min (c) 20 min and (d) 65 min after exposure to broad-area illumination. Note that (d) is shifted to the right as a result of imperfect attempts to center the device after a slow stage drift. Also note that the photocurrent scale bars are the same, unlike in Fig. 5.3.

The larger amplitude of the photocurrent and the increased distance over which photocurrent was observed are indicative of a larger effective electron minority-carrier diffusion length, $L_{n,eff}$, under broad-area illumination than in the dark. Because of the observed long time decay in $L_{n,eff}$ (time scale of minutes) after removal of the broad-area illumination, we assume that an improvement in surface passivation produces the observed increase in $L_{n,eff}$ with broad-area illumination. An increase in $L_{n,eff}$, as a result of an increase in the bulk lifetime, would be expected to decay on the time scale of the minority-carrier lifetime (10100 ns.) A proposed mechanism for

the observed surface passivation under broad-area illumination is presented in section 5.6.

5.5.3 Extracted Minority-Carrier Diffusion Lengths

Figure 5.5 displays photocurrent cross-sections of the SPCM images along the length of the wire, as a function of the bias voltage applied to the Ohmic contact. These data allowed calculation of values of $L_{n,eff}$ based upon the expected relationship for diffusion-limited minority-carrier transport in the quasi-neutral region, as detailed in Eqn. (5.1). Under broad area illumination, the best-performing individual device exhibited a value of $L_{n,eff} = 9.5 \pm 0.2$ μm for photocurrent cross-sections along the center of the wire and a value of $L_{n,eff} = 11.5 \pm 0.2$ μm for photocurrent cross-sections along the sidewall of the wire (Fig 5.3c, see Appendix C), producing an average $L_{n,eff}$ of 10.5 ± 1 μm for this sample. Measurements in the dark yielded $L_{n,eff} \leq 0.7$ μm. The value of $L_{n,eff}$ measured in the dark is an upper bound for the actual value of $L_{n,eff}$ under these conditions, because the photocurrent variation produced by the Gaussian profile of the laser beam is significant for such small diffusion lengths. Four other devices yielded $L_{n,eff}$ values under illumination of 4, 5, 6 and >7 μm, with the latter value limited by the contact-to-contact spacing in the devices under study. The observed variation of $L_{n,eff}$ is not surprising based on the proposed surface passivation mechanism. The highest measured value of 10.5 μm can thus be taken as a lower bound on the true bulk minority-carrier diffusion length of such wires. Measurements made at both forward and reverse bias, as well as zero-bias photovoltaic collection conditions, confirmed that the measured effective minority-carrier diffusion lengths were independent of bias, and thus rule out significant contributions from drift current to the $L_{n,eff}$ measurements.

5.6 Proposed Surface Passivation Mechanism

The photo-injection of electrons into the oxide (oxide trapped charge)[53] could produce a decrease in the surface recombination velocity, S, and is consistent with the long

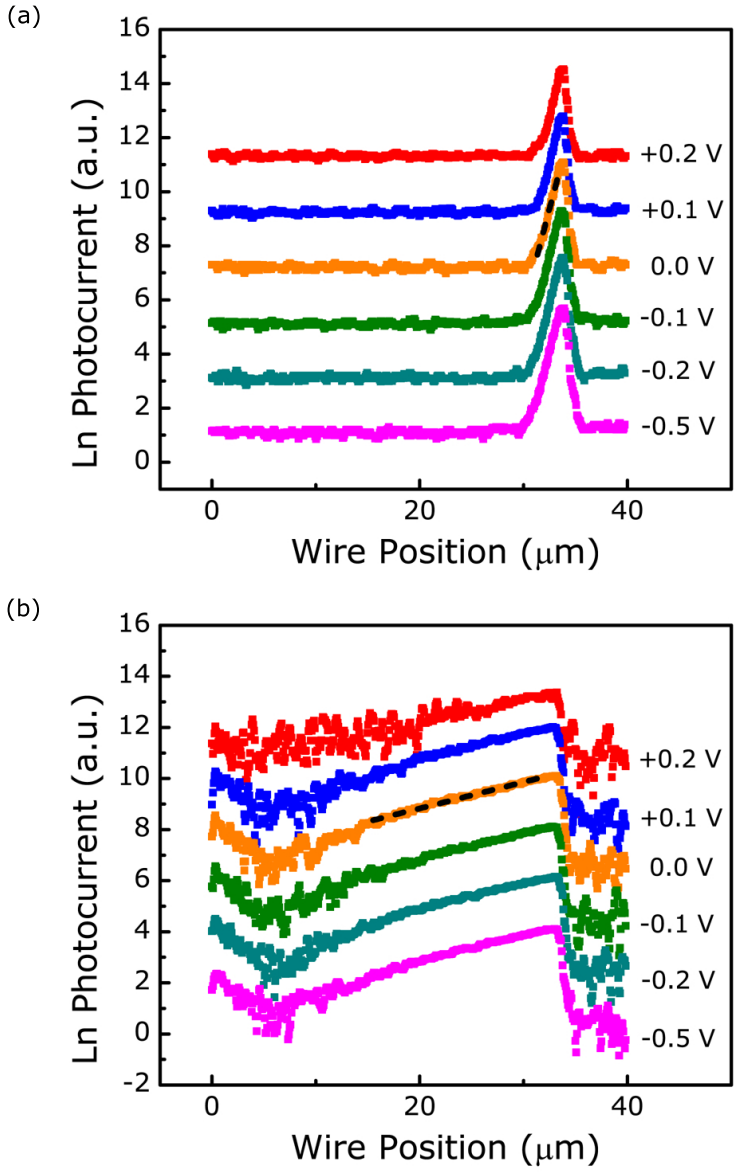


Figure 5.5. Photocurrent cross-sections along the length of the wire, as a function of the bias voltage applied to the Ohmic contact. (a) Measured in the dark, (b) and measured under low-level-injection, broad-area illumination. In both (a) and (b) the zero-bias fit is shown as a dashed black line and is used to calculate effective electron minority-carrier diffusion lengths, $L_{n,eff}$, of < 0.7 μm and 9.7 μm, respectively.

time decay in $L_{n,eff}$. Figure 5.6a depicts the expected band structure for p-Si coated with a native oxide that contains positive fixed oxide charge. The presence of positive fixed oxide charge, which is well known to exist in SiO_2,[54, 55] will introduce negative surface band bending. This band-bending will result in a large minority-carrier surface concentration and hence produce a high surface-recombination velocity. However, the photo-injection of electrons into the oxide could balance the positive fixed oxide charge, thereby reducing the negative surface band bending and decreasing S. (Fig. 5.6b). A long time scale (time scale of minutes) for electrons to tunnel out of an oxide[56] is consistent with observed the long time decay in $L_{n,eff}$ under the proposed surface passivation mechanism.

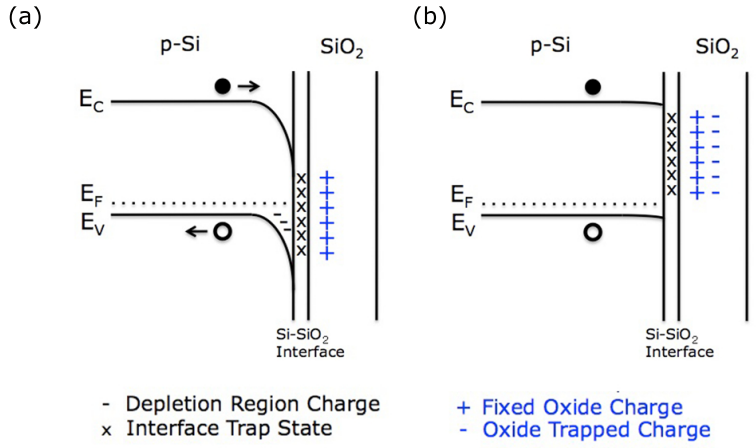


Figure 5.6. (a) Schematic illustration of the proposed band-diagram in the dark. (b) Schematic diagram of the proposed band-diagram under broad-area illumination.

5.7 Surface Recombination Velocity

The $L_{n,eff}$ in a cylindrical geometry can be calculated as a function of the surface recombination velocity (SRV) and bulk minority-carrier diffusion length using the method reported by Allen and developed by Daiminger.[34, 57] Figure 5.7 displays the calculated $L_{n,eff}$ for a 2.0 μm diameter, p-Si wire with an active doping concentration

of 1.0×10^{17} cm^{-3}, as a function of SRV and bulk minority-carrier diffusion length. $L_{n,eff}$ is observed to depend sensitively on the SRV for 2.0 μm diameter Si wires with bulk minority-carrier diffusion lengths > 10 μm.

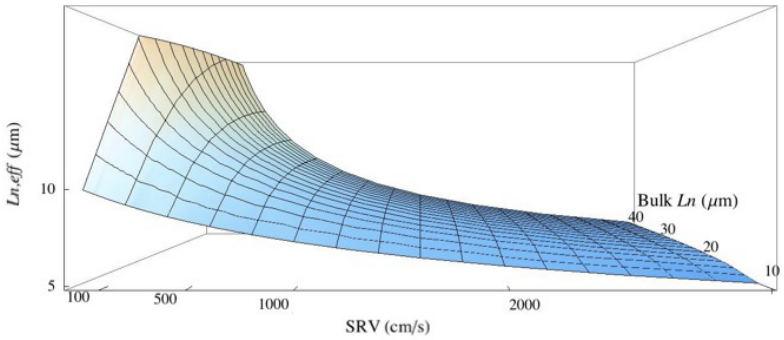


Figure 5.7. Calculated $L_{n,eff}$ in 2.0 μm diameter p-Si wires with a doping of 1.0×10^{17} cm^{-3} plotted against the surface recombination velocity (SRV) and the bulk minority-carrier diffusion length, L_n.

As can be seen from Table 5.7, bounds of S $\leq 9 \times 10^2$ cm s^{-1} under broad-area illumination and S $\geq 3 \times 10^5$ cm s^{-1} in the dark can be estimated from the measured values of $L_{n,eff}$ for the best-performing device, assuming a bulk diffusion length of 20 μm.[34, 58]

5.8 Discussion

5.8.1 Bulk Minority-Carrier Diffusion Length

The bulk minority-carrier electron diffusion length is 20 μm for p-Si that contains the thermodynamic equilibrium concentration (10^{17} atoms cm^{-3}) for Cu in Si at 1000°C.[45] Hence, the $L_{n,eff}$ measured for our Cu-catalyzed Si wires may still be limited by surface recombination and/or by the presence of other impurities in the bulk of the Si wires.

Since the time of this work, we have shown that $L_{n,eff} >> 30$ μm (and correspondingly the bulk minority-carrier diffusion length $>> 30$ μm) are possible using

Table 5.1. Calculated $L_{n,eff}$ in 2.0 μm diameter p-Si wires with a doping of 1.0 $\times$ 10^{17} cm^{-3} for values of the surface recombination velocity (SRV) from 10 to 10^6 cm s^{-1} assuming a 20 μm bulk minority-carrier diffusion length, L_n.

SRV (cm/s)	Bulk L_n (μm)	$L_{n,eff}$ (μm)	SRV (cm/s)	Bulk L_n (μm)	$L_{n,eff}$ (μm)
10	20	20	10000	20	3.3
25	20	19	25000	20	2.1
100	20	17	50000	20	1.5
250	20	14	100000	20	1.1
500	20	12	250000	20	0.76
1000	20	9.3	500000	20	0.60
2500	20	6.3	1000000	20	0.51

an a-SiN$_x$:H layer to passivate the surface of the wires.[59]

5.8.2 Interface Trap Density

From the value of S measured in the dark, the Si-SiO$_2$ interface trap density can be estimated to exceed 3 $\times$ 10^{13} cm^{-2}, assuming reasonable values of the thermal velocity (ν_{th} = 10^7 cm s^{-1}) and of the trap capture cross-section (σ =10^{-15} cm^2) (D$_{it}$ = 1/(S σ ν_{th})). This is a large interface trap density, but is comparable with previous results[34] and is much smaller than the surface density of Si atoms.

5.8.3 Implications for Solar Cells Catalyst Choice

Achievement of $L_{n,eff}$ = 10.5 μm in Si microwires grown from a low-cost Si precursor is a significant result for Si wire array photovoltaics. Semiconductor device transport models suggest that single-wire solar cells with a Si wire diameter of 5.8 μm, a wire length of 103 μm, and a base doping concentration of 6 $\times$ 10^{17} cm^{-3} should be able to produce Air Mass 1.5 efficiencies of η =17.5%.[16] As a means for comparison, the optimized design parameters for a single-wire solar cell with an $L_{n,eff}$ = 2 μm are a

wire diameter of 1.7 μm, a wire length of 46 μm, and a base doping concentration of 10^{18} cm^{-3}, yielding a cell with a predicted efficiency of η =13.4%.[16]

Additionally, concurrent to the work presented in this chapter, we have used Cu-catalyzed, Si wire arrays (in-situ doped with BCl_3) to demonstrate internal quantum yields of at least 0.7 in a photoelectrochemical cell.[60] Internal quantum yields ¿ 0.7 further demonstrate the possibility to fabricate an efficient Si microwire-array solar cell.

5.9 Conclusion

In this chapter we have demonstrated that Cu-catalyzed, Si microwires, in-situ doped with BCl_3, can exhibit effective minority-carrier diffusion lengths of 10.5 μm. This result indicates that solar cells with efficiencies of at least 17.5% should be possible. With this knowledge, we can now turn our attention to the fabrication steps necessary to realize a solid-state, Si microwire-array solar cell.

Chapter 6

Si Microwire-Array Solar Cells

6.1 Introduction

The work presented in this chapter is the culmination of work by myself and others to develop an efficient Si microwire-array solar cell. In particular, I would like to acknowledge work by Michael Kelzenberg that demonstrated the use of light-trapping elements for enhanced optical absorption in Si microwire arrays,[15] which guided the development of solid-state Si microwire-array solar cells of an advanced design, as presented in this chapter.

In this chapter we will discuss the design, fabrication, and characterization of Si microwire-array solar cells with Air Mass 1.5 Global conversion efficiencies of up to $\eta = 7.9\%$. These solar cells exhibited open-circuit voltages of 500 mV, short-circuit current densities (J_{sc}) of up to 24 mA cm^{-2}, and fill factors $> 65\%$, and had Al_2O_3 dielectric particles that scattered light incident in the space between the wires, a Ag back reflector that prevented the escape of incident illumination from the back surface of the solar cell, and an a-SiN$_x$:H passivation/antireflection layer. Wire-array solar cells without some or all of these design features were also fabricated to demonstrate the importance of the light-trapping elements in achieving a high J_{sc}. Scanning photocurrent microscopy images of the microwire-array solar cells revealed that the higher J_{sc} of the most advanced cell design resulted from an increased absorption of light incident in the space between the wires. Spectral response measurements further revealed that solar cells with light-trapping elements exhibited improved red and infrared response as compared to solar cells without light-trapping elements.

6.2 Background

Wire solar cells have been fabricated using c-Si,[26, 44, 61, 62, 63, 64, 65, 66, 67, 68, 69] amorphous-Si,[70] GaAs,[71] III-Nitrides,[72] and InP,[73] via a variety of growth techniques, including VLS growth,[26, 44, 61, 62, 63, 64, 65, 66, 69] metal-catalyzed chemical etching,[67, 70] molecular beam epitaxy,[71] metal-organic chemical vapor deposition,[72, 73] and deep reactive-ion-etching.[68] In particular, the VLS growth method offers a materials-efficient and scalable route for the synthesis of semiconducting wires. However, the efficiencies of VLS-grown, c-Si, single-wire[44, 64, 66] and wire-array[26, 61, 62, 63, 65, 69] solar cells, up to 3.4%[64] and 1.8%[65] respectively, have fallen short of the ∼15% photovoltaic efficiency predicted from simple considerations.[13, 57] In particular these solar cells have failed to demonstrate open-circuit voltages (V_{oc}) in excess of 300 mV, possibly indicative of significant recombination within the depletion region and/or at the surfaces of the cells.[13, 63, 74]

6.3 Device Design

6.3.1 p-n Junction Design

Before delving into the process of device fabrication, there are two points with regards to device design that are worth mentioning. The first point relates to the design of the p-n junction. Figure 6.1 depicts the most straightforward p-n junction design: a continuous emitter that extends throughout the length of the wire and across the growth substrate. This type of junction could be readily achieved through a single thermal diffusion doping of the p-Si wire arrays. However, given the long ($>> 30\ \mu$m) minority-carrier diffusion lengths reported in passivated Si microwires,[59] it is likely that the simplicity of this design will impose a larger p-n junction area than the p-n junction area necessary to ensure the complete collection of the photoexcited carriers. Because the dark saturation current (J_o) scales with junction area and because the V_{oc} logarithmically decreases with increasing J_o, see Eqn. (6.1), the effect of the additional junction area will be to reduce the V_{oc}.

$$V_{oc} = \frac{kT}{q} ln \frac{J_L}{J_o} \tag{6.1}$$

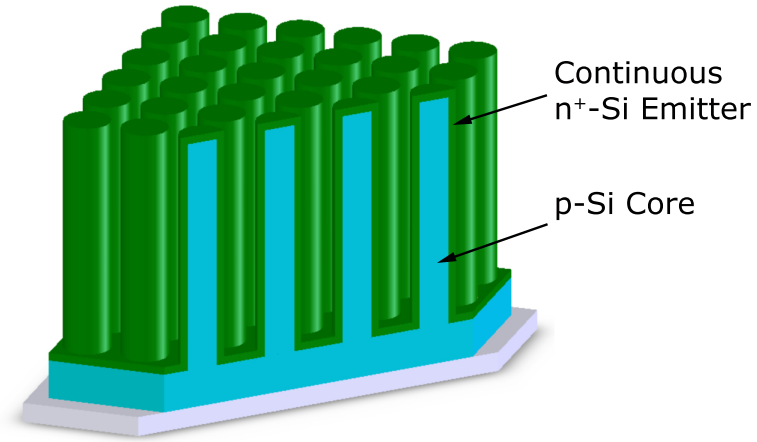


Figure 6.1. Continuous emitter geometry in a wire-array solar cell.

While a decreased V_{oc} is not optimal, a larger concern with the continuous emitter design arises when one considers the fabrication of Si wire-array solar cells that have been removed from the growth substrate. For wire-arrays with continuous emitters, both the p and n regions of the solar cell will be exposed at the base of the wire-array. Consequently, making a back contact without shorting the p-n junction will be difficult. (The back contact would have to make an Ohmic contact to the p-region, while making a rectifying contact to the n-region under 0.5-0.6 V forward-bias.)

Thus, to avoid a reduced V_{oc} and the possibility for a short at the back contact, we developed a photolithography-free process for the fabrication of p-n junctions extending across an arbitrary length of the wires, as will be discussed in section 6.4.3.

6.3.2 Contacting Strategies

The second design point worth mentioning is the fabrication of a contact to the n^+-Si emitter. Two separate designs were considered for contacting the n^+-Si emitter. The first design employed a transparent conducting oxide (TCO) to electrically contact

each wire, as shown in Figure 6.2a. The second design utilized an Al film to electrically contact each wire and serve as a back reflector, as shown in Figure 6.2b. In addition to serving as a back reflector, the embedded Al contact is promising because of its potential for reduced shadowing loses. In comparison, a TCO layer is only expected to transmit ∼90% of the solar spectrum and would require a metallic top contact grid covering ∼5% of the cell area (not shown in Fig. 6.2a) to keep the cell series resistance below an acceptable level (∼0.5 Ω cm^2.) Though good progress was made towards realizing the embedded Al contact (Appendix D), the more straightforward TCO design was demonstrated first and used to explore the more fundamental challenges for the fabrication of efficient Si microwire-array solar cells, namely the incorporation of light-trapping elements in a solid-state device.

6.4 Device Fabrication

6.4.1 As-Grown, Scatterer, and PRS Cell Types

Three different types of Si microwire solar cells were fabricated. The *As-Grown* cell contained no light trapping elements or surface passivation. The *Scatterer* cell incorporated light-scattering Al_2O_3 particles (nominally 80 nm in diameter) in-between the wires. The *PRS* cell utilized an *a*-SiN_x:H passivation layer to minimize surface recombination and serve as an anti-reflection coating, a Ag back reflector to prevent the loss of incident illumination into the growth substrate, and Al_2O_3 particles to scatter light incident between the Si microwires.

The As-Grown cell was fabricated in the following manner: growth of wire arrays (section 6.4.2); definition of the p-n junction (section 6.4.3); dielectric infill of the wire arrays (section 6.4.7); and deposition of a transparent conducting oxide (section 6.4.8). For the Scatterer solar cell, the same process was followed, except that inclusion of Al_2O_3 particles (section 6.4.4) occurred prior to the dielectric infill of the wire arrays (section 6.4.7). For the PRS cell, the deposition of an *a*-SiNx:H layer (section 6.4.5), followed by the fabrication of a Ag back reflector (section 6.4.6) was performed prior

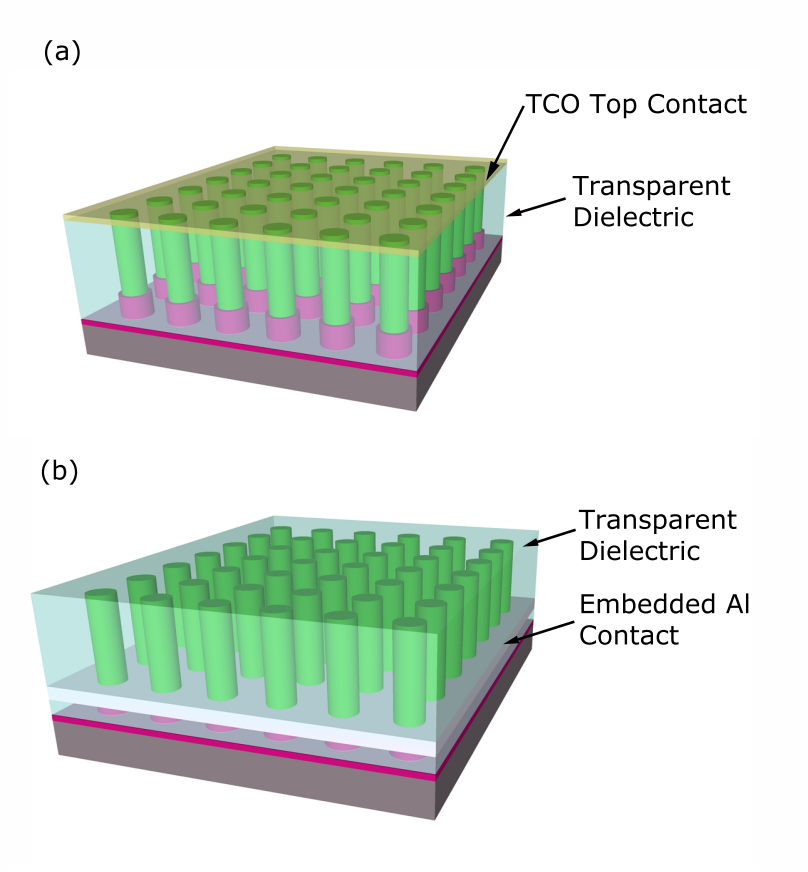


Figure 6.2. (a) Schematic of a wire array solar cell employing a transparent conductive oxide (TCO) as a transparent top contact. (b) Schematic of a wire array solar cell employing an Al film embedded near the base of the wire array, which functions as both a contact to the n^+-Si emitter and as a back reflector.

to the inclusion of the Al_2O_3 particles (section 6.4.4). The details of these fabrication steps can be found in Appendix D.

6.4.2 Starting Material

Square-tiled arrays of vertically aligned Si microwires (2-3 μm in diameter on a 7 μm pitch) were grown on p^{++} (resistivity, ρ, < 0.001 Ω cm) Si(111) wafers using the VLS growth method, as described previously.[27] P-type doping of the Si microwires was achieved during growth using BCl_3 as a gaseous dopant source.[75] Four-point electrical measurements performed on individual Si wires from arrays grown under

nominally identical growth conditions indicated that the wires were p-type with $\rho =$ 0.05 Ω cm, which corresponds to an electrically active dopant concentration (N_A) of 7×10^{17} cm^{-3}, assuming a bulk hole mobility of 1.8×10^2 cm^2 V^{-1} s^{-1} for Si.

6.4.3 p-n Junction

As illustrated in Figure 6.3, a simple and photolithography-free p-n junction fabrication process was developed that allowed for p-n junctions to extend across an arbitrary length of the wires. First, the as-grown wire arrays (Fig. 6.3a) were chemically etched to remove the Cu-catalyst and to remove a thin layer (∼50 nm) of surface Si. A 200 nm-thick thermal oxide was then grown, which was followed by the deposition of a polydimethylsiloxane (PDMS) layer at the bases of the microwires (Fig. 6.3b). The thermal oxide was then selectively removed in a hydrofluoric acid (HF) solution (aq.) using the PDMS layer as an etch barrier for the thermal oxide located at the bases of the microwires (Fig. 6.3c). After removal of the PDMS,[76] radial p-n junctions were formed in the upper region of the Si microwires during a thermal phosphorous diffusion, while the thermal oxide functioned as a phosphorous diffusion barrier for the lower region of the wires (Fig. 6.3d).

Figure 6.4 displays cross-sectional scanning electron microscope (SEM) images of a wire array after p-n junction formation. As seen in Figure 6.4a, the height of the thermal oxide (and thus the extent of the radial p-n junction) was uniform across the wire array. Figure 6.4b demonstrates the abrupt removal of the thermal oxide that can be obtained with this junction fabrication method. Spreading resistance analysis of planar controls revealed the phosphorous diffusion depth to be ∼80 nm, as shown in Figure 6.5.

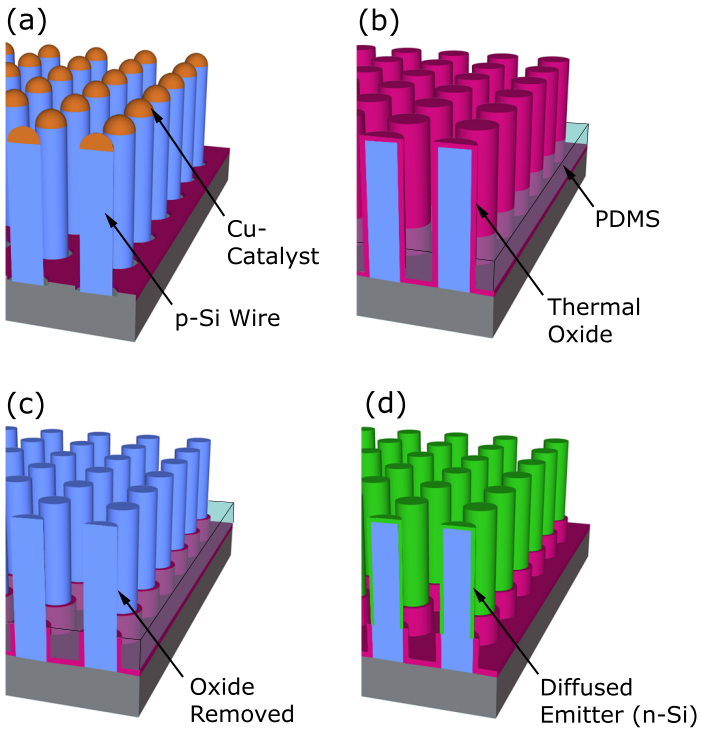


Figure 6.3. Schematic of the radial p-n junction fabrication process. (a) VLS-grown, p-Si microwire array. (b) Microwire array after catalyst removal, growth of a thermal oxide and deposition of a PDMS layer. (c) Removal of the unprotected thermal oxide. (d) Removal of the PDMS and subsequent phosphorous diffusion to complete the fabrication of a radial p-n junction.

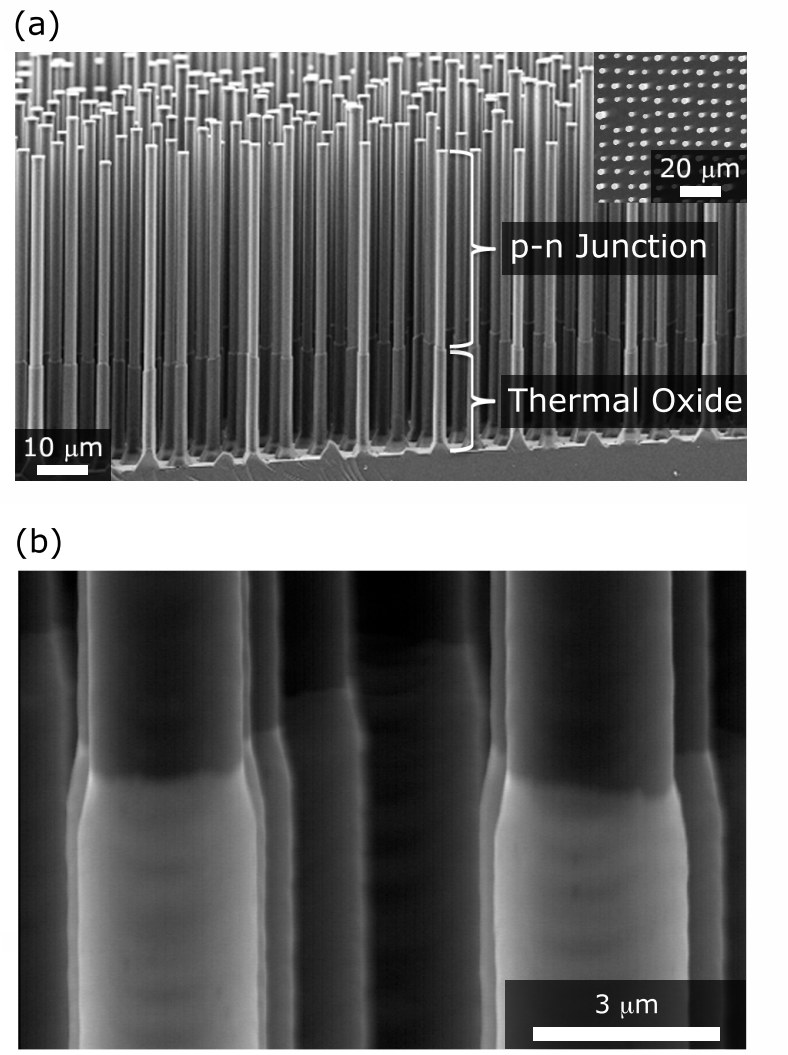


Figure 6.4. Cross-sectional SEM images of a Si microwire array after radial p-n junction formation. (a) Low-magnification SEM image. Inset, top-down SEM image of the same Si microwire array. (b) High-magnification SEM image of the region where the thermal oxide ends and the radial p-n junction begins.

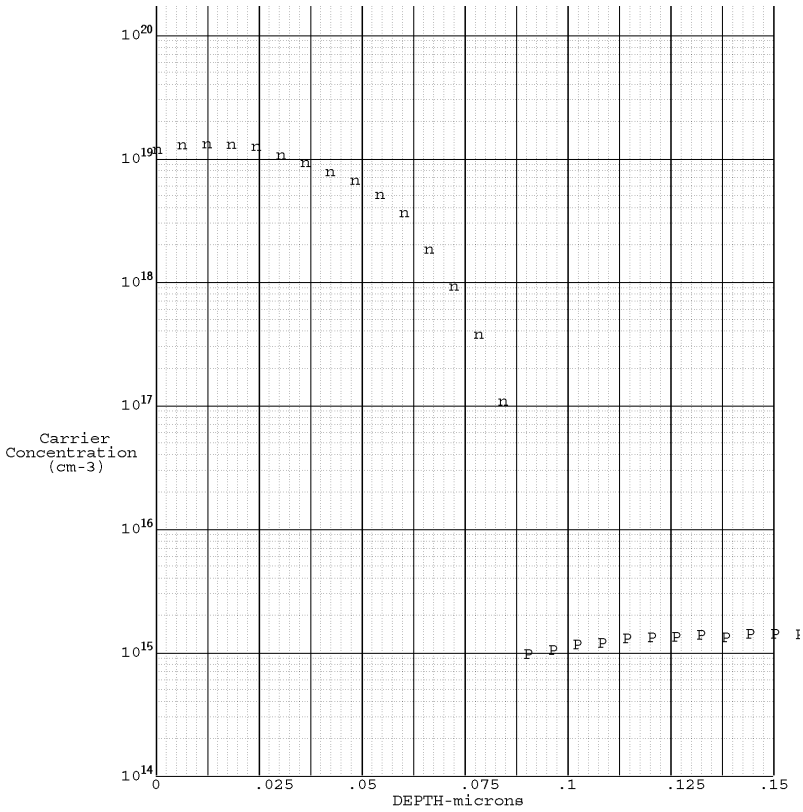


Figure 6.5. Phosphorous diffusion profile for a 10 min diffusion at 850°C as measured by spreading resistance analysis on a planar sample.

6.4.4 Al_2O_3 Scattering Particles

For the Scatterer and PRS solar cells, Al_2O_3 scattering particles were incorporated by centrifuging a dispersion of Al_2O_3 particles in ethanol onto a wire array, as depicted in Figure 6.6a. Al_2O_3 scattering particles accumulated primarily at the base of the wire array, however some also collected along the wire sidewalls and at the wire tips (Fig. 6.6b.)

6.4.5 *a*-SiN_x:H Passivation/Antireflection

For the PRS solar cells, the thermal oxide was completely removed after the phosphorous diffusion. An *a*-SiN_x:H passivation/antireflection layer was then deposited using

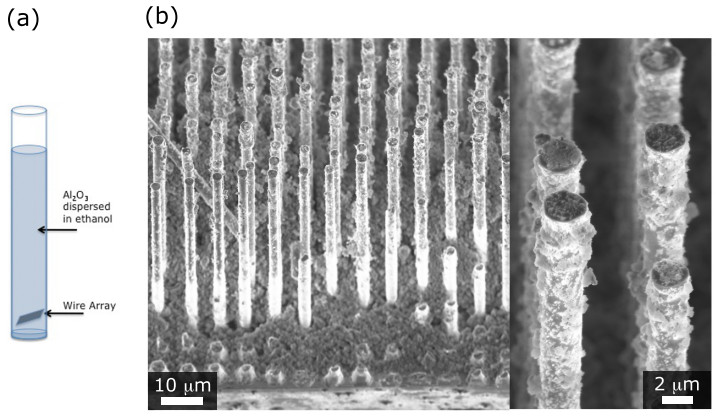


Figure 6.6. (a) Schematic of Al_2O_3 particle incorporation. (b) SEM image of a wire array after incorporation of Al_2O_3 scattering particles. Inset, high magnification SEM image of wire tips.

plasma enhanced chemical vapor deposition (PECVD), as described previously.[15] The *a*-SiN_x:H layer conformally coated the wires and substrate prior to selective removal of the *a*-SiN_x:H from the tips of the wires using hydrofluoric acid (HF) aq., as shown in Fig. 6.7. The bright tip is the c-Si wire, while the darker base is the *a*-SiN_x:H-coated c-Si wire. The difference in the extent of the exposed tip relates to variations in the wire height and variations in the height of the mounting wax etch barrier (removed prior to imaging.) Removal of the *a*-SiN_x:H allowed for the transparent conducting oxide to form an Ohmic contact the n-Si emitter.

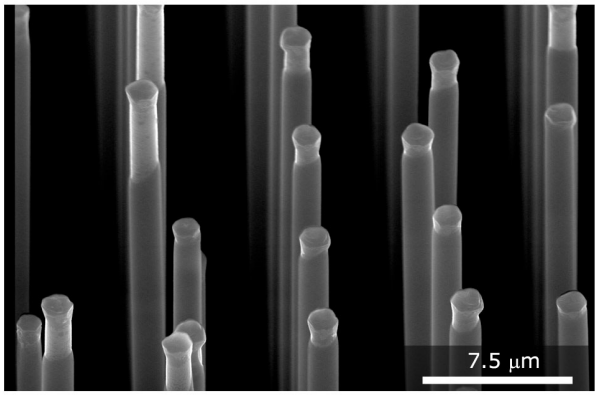


Figure 6.7. SEM image of a wire array after selective removal of *a*-SiN_x:H from the wire tips.

6.4.6 Ag Back Reflector Fabrication

Figure 6.8 provides SEM images that document the fabrication of the Ag back reflector in the PRS solar cell after *a*-SiN_x:H deposition, but prior to Al_2O_3 incorporation. Following two 500 nm Ag evaporations, Ag uniformly coated the substrate and the wire sidewalls (Fig. 6.8a). PDMS was then deposited and continuously coated the Ag-coated substrate (Fig. 6.8a,b). (Because the SEM images shown are from the edge of a wire array, the PDMS is thinner than in the center of the wire array and there exists a small area at the immediate wafer edge where no PDMS coating exists.) A Ag etch was then used to remove any Ag that was not protected by the PDMS film at the base of the wire array (Fig. 6.8b). After PRS cell fabrication, the PDMS-protected Ag back reflector was revealed by cell cross sectioning (Fig. 6.8c).

6.4.7 Transparent Dielectric

Four different materials were considered for use as a dielectric infill and structural support. As the selection of a dielectric infill provided considerable insight into the future design of Si microwire-array solar cells, especially the design of flexible Si microwire-array solar cells, a discussion of the different materials examined is provided in Appendix D. Ultimately mounting wax (a transparent, non-conducting, thermoplastic polymer) was selected for its ability to provide a sufficiently firm surface as to prevent fracture of the transparent conducting oxide during contact with an electrical probe tip. By melting mounting wax into the wire array, a uniform infill of mounting wax at the height of the wire tips could be obtained, as seen in Figure 6.9. The one minor issue with mounting wax was that it cracked upon cooling (Fig. 6.9 inset), (These cracks closely resembled the cracks found in dried mud.) By reducing the cooling rate the density of cracks could be sufficiently reduced to the point where fabricated cells did not contain cracks. Prior to TCO deposition, an O_2 plasma was used to remove 5-15 μm of wax to ensure that all of the wire tips were exposed and free of wax (Fig. 6.9b).

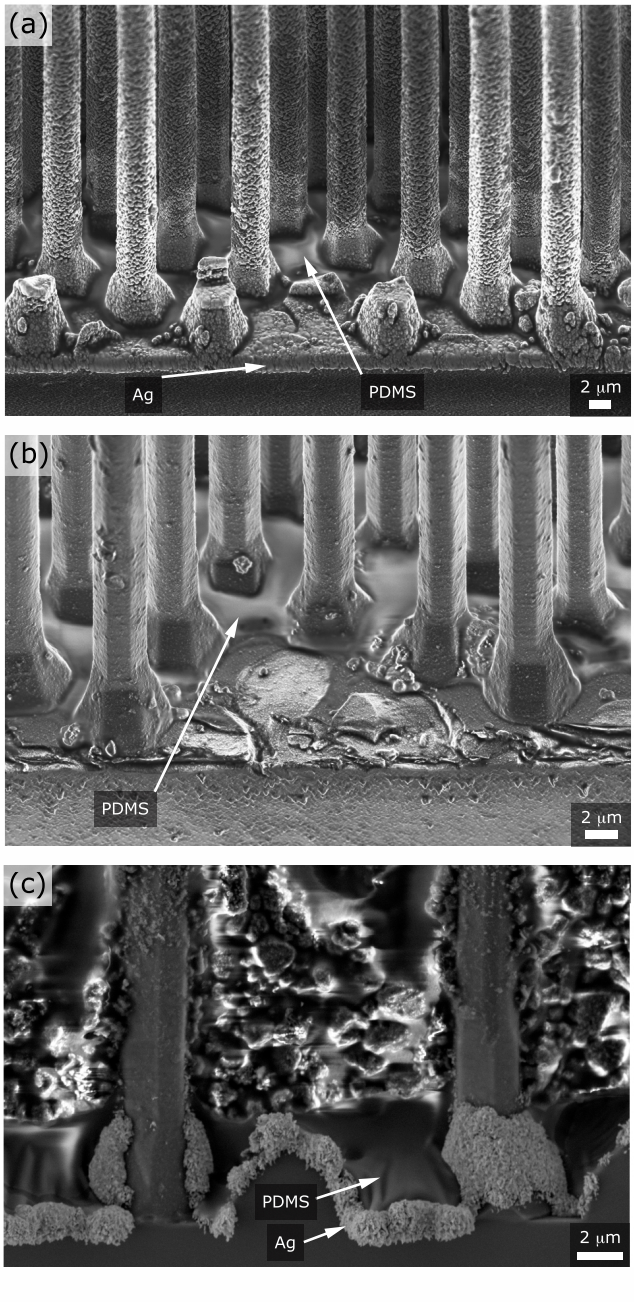


Figure 6.8. Tilted scanning electron microscope (SEM) images illustrating the fabrication of a Ag back reflector. (a) SEM image post Ag and protective polydimethylsiloxane (PDMS) deposition. (b) SEM image of the wire array from (a) after a Ag-etch. (c) Cross-sectional SEM image of a PRS microwire solar cell.

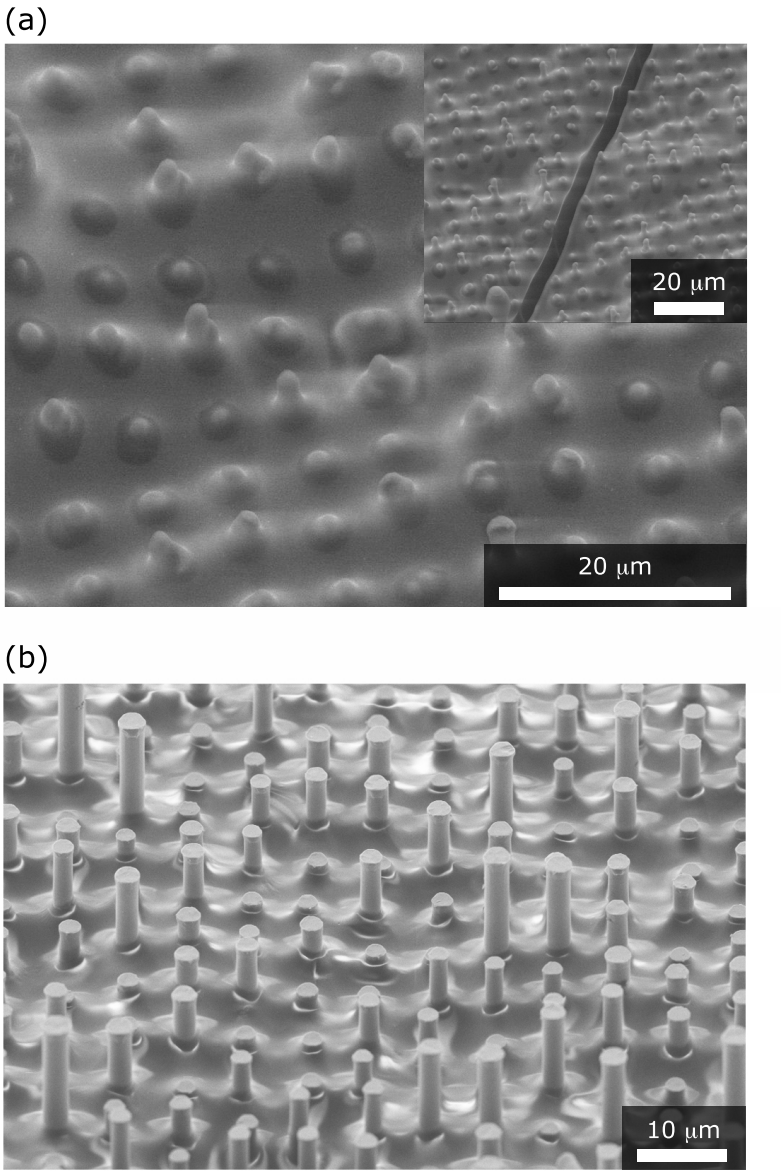


Figure 6.9. (a) SEM image of a wire array infilled with mounting wax. Inset, a small density of cracks in the mounting wax was observed. (b) SEM image of a wire array after removing a few microns of mounting wax with an O_2 plasma.

6.4.8 Transparent Conducting Oxide

Indium tin oxide (ITO) was chosen as the transparent conducting oxide to contact the n^+-Si emitter because of its excellent optical transmission and electrical conductivity. A 120-150 nm-thick ITO layer ($\rho \sim 7 \times 10^{-4}$ Ω cm) was sputtered through square openings in a shadow mask (270 μm on a side) to form a top contact and to define the area of the solar cells, as shown in Figure 6.10.

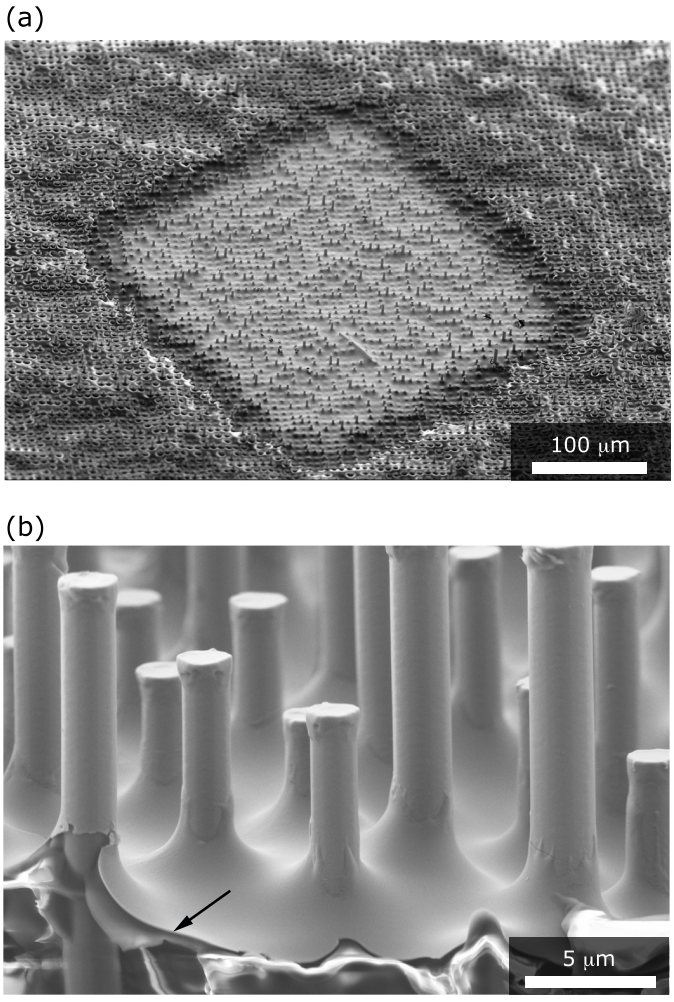


Figure 6.10. (a) SEM image of a wire array infilled with mounting wax and coated with a 150 nm-thick ITO layer. (b) Cross-sectional SEM image revealing the ITO layer on top of the mounting wax, as indicated by the black arrow.

Figure 6.11 plots the transmission as a function of wavelength for a glass coverslip with a 150 nm-thick indium tin oxide (ITO) layer. For wavelengths > 700 nm, strong oscillations in transmission were observed. Nearly identical oscillations in the transmission as function of wavelength were observed for a glass coverslip without an ITO coating. Thus, the oscillations are attributed to Fabry-Pérot interferences that arise from the thin nature of the glass coverslip. Applying a 5 nm running average, transmission through the ITO was found to be $> 80\%$ for wavelengths > 500 nm, and monotonically increasing from 65% to 80% between 400 and 500 nm.

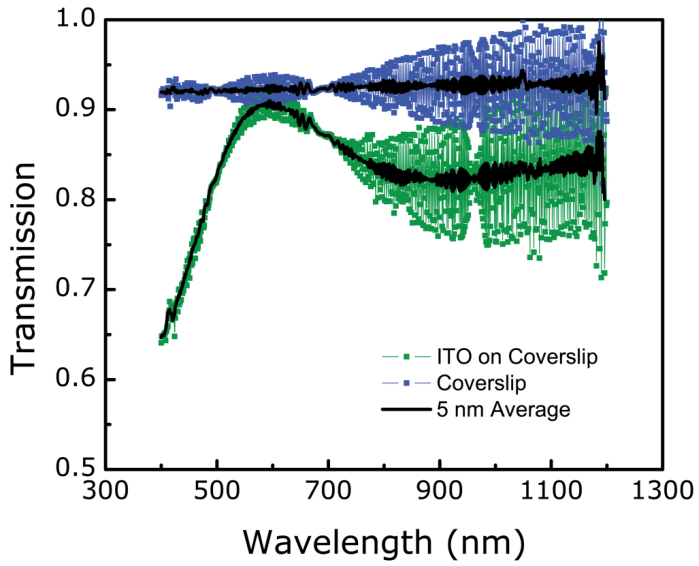


Figure 6.11. Transmission as a function of wavelength for a glass coverslip with and without a 150 nm-thick indium tin oxide coating. The black lines are 5 nm running averages.

6.4.9 Completed Cells

Figure 6.12 displays cross-sectional scanning electron microscope (SEM) images for (a) As-Grown, (b) Scatterer, and (c) PRS microwire-array solar cells. Wire heights ranged from 57-63 μm, 71-78 μm, and 43-49 μm for the As-Grown, Scatterer, and PRS microwire solar cells, respectively. The thermal oxide in the finished cells covered

the lower 27-32 μm of the wires for the As-Grown and Scatterer solar cells. For both the Scatterer and PRS solar cells, the 80 nm Al_2O_3 particles were observed to form micron-sized agglomerates that were located near the base of the wires, as evidenced by the granular texture of the mounting wax near the bottom of the wire array (Fig. 6.12b,c) and at the wire tips and sidewalls (Fig. 6.12b,c inset.) In the PRS solar cells, the 1000 nm-thick Ag back reflector covered the growth substrate and the tapered base of the wires (Fig. 6.12c and Fig. 6.8). The a-SiN_x:H anti-reflection/passivation layer is not visible in Fig. 6.12c. For all devices, the mounting wax uniformly infilled the wire array, and the ITO conformally coated the mounting wax and the wire tips, thereby providing a continuous top contact despite the highly textured surface.

Figure 6.13 provides optical images of the fabricated solar cells. Contact to the p-type core of the Si microwires was established through the p^+-Si substrate by scribing a Ga/In eutectic onto the back side of the growth wafer. The growth wafer was then placed on Cu tape and mounted onto a glass slide for ease of handling. Figure 6.13b is an optical microscope image of an electrical probe tip contacting a single microwire solar cell. The bright stripes down the centers of the solar cells are Au contact fingers (not found on the cells discussed below) that were placed on initial solar cells in an attempt to improve the ease of obtaining a low resistance electrical contact between the electrical probe tip and the ITO layer.

6.5 Characterization

6.5.1 Cell Area

In total, 15 As-Grown microwire solar cells, 12 Scatterer microwire solar cells, and 24 PRS microwire solar cells were fabricated. The area of the fabricated cells spanned a range from 0.12 to 0.21 mm^2, as a result of variations in the gap between the top of the microwire arrays and the shadow mask during the deposition of the ITO. To accurately determine the cell area, scanning photocurrent microscopy (SPCM) was used to image the perimeter of 2-3 cells from each cell type, as schematically depicted

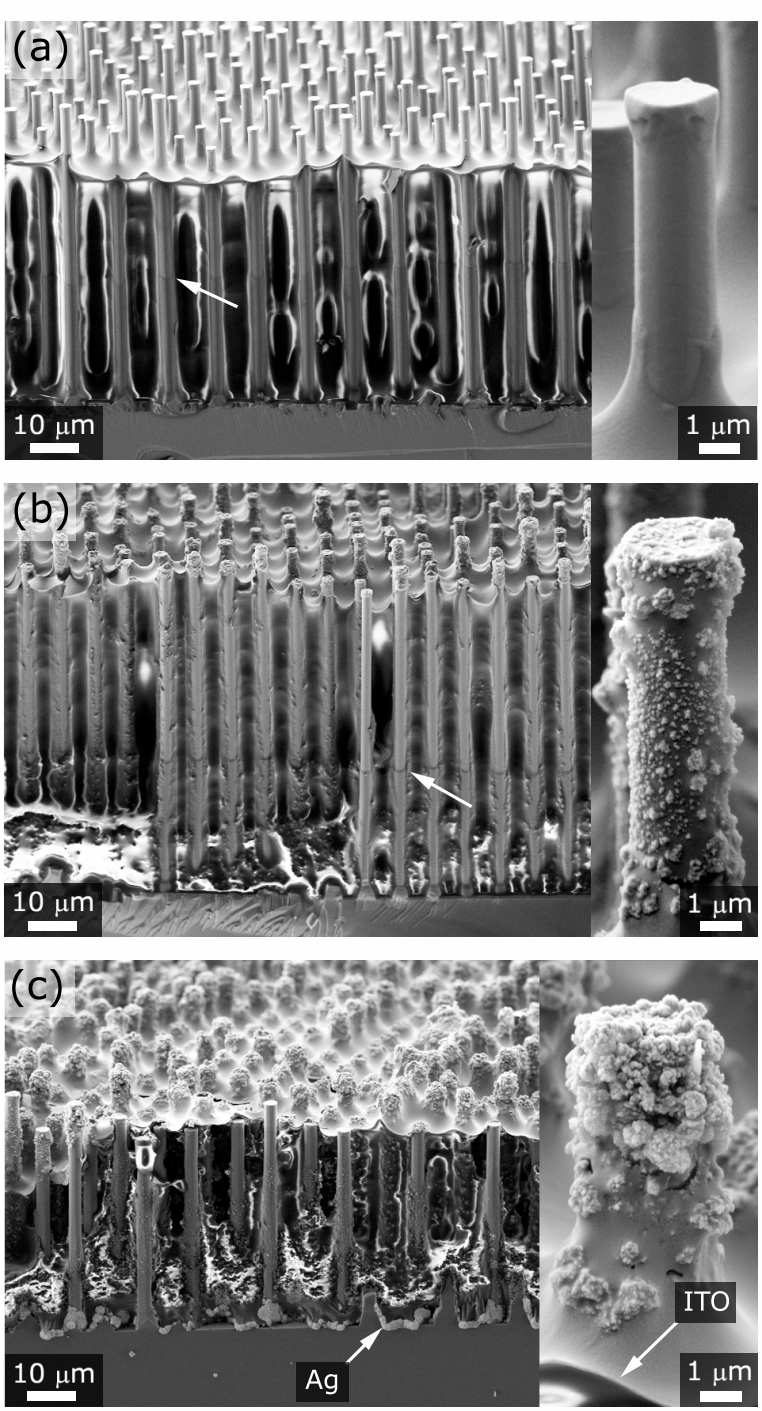
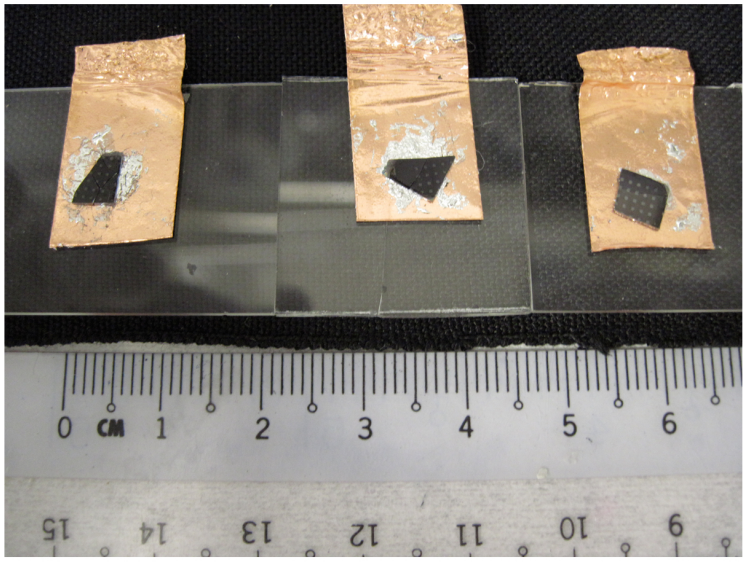


Figure 6.12. Si microwire-array solar cell device geometry. Cross-sectional SEM image of (a) an As-Grown solar cell, (b) a Scatterer solar cell, and (c) a PRS solar cell. Insets, higher magnification SEM images of the wire tips d. For (a)-(b) the white arrow denotes the height of the thermal oxide.

(a)



(b)

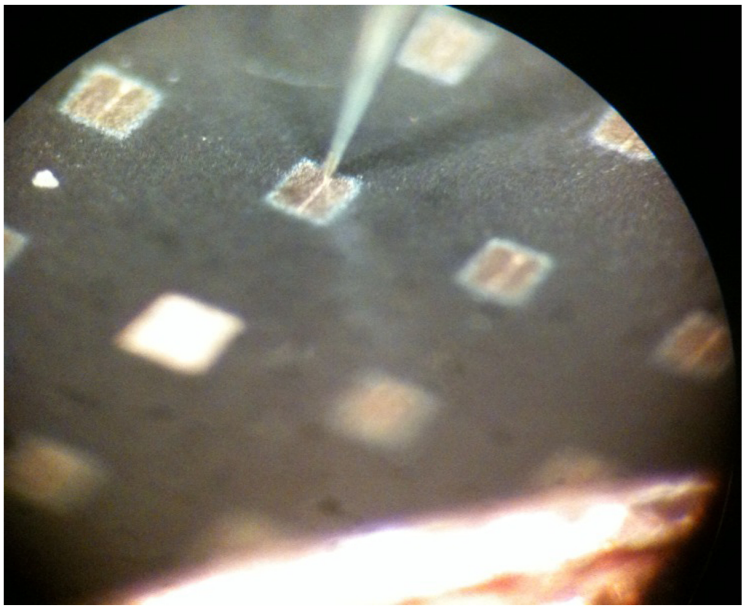


Figure 6.13. Si microwire-array solar cells. (a) Optical image of As-Grown, Scatterer, and PRS cells (from left to right.) (b) Optical microscope image of a probe tip contacting an individual solar cell. Each pad is $\sim$ 300 μm on a side.

in Figure 6.14.

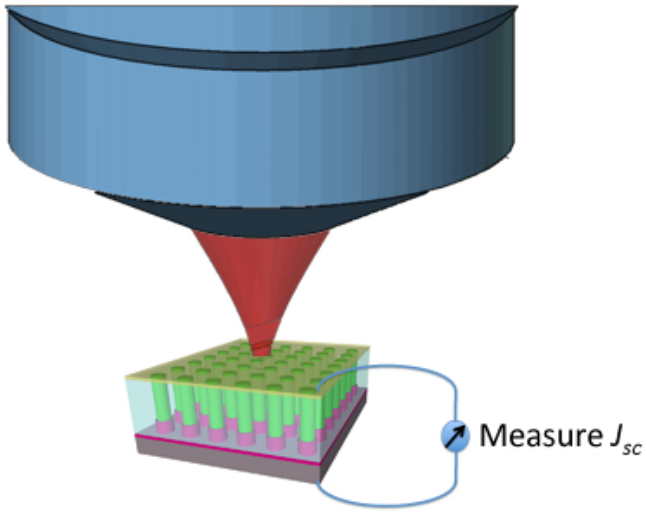


Figure 6.14. Schematic of the scanning photocurrent measurement. Confocal laser illumination is focused onto the Si microwire-array solar cell. The solar cell sits on top of a piezoelectric stage and is rastered beneath the focused laser illumination while the short-circuit current is measured.

Scanning photocurrent microscopy images (90 μm x 90 μm, Fig. 6.15a) were stitched together to produce a photocurrent map of the cell perimeter (Fig. 6.15b), which was then analyzed to calculate the cell area (Fig. 6.15c). Area analysis was performed using the thresholding feature in Image J. Thresholding was done in such a way that all of the wires within the cell perimeter (defined by the photoactive wires) were selected. The indent on the left side of the cell resulted from contact shadowing and an appropriate correction to the cell area was made (not shown.) A small photocurrent signal was present outside of the cell perimeter (Fig. 6.15a) and is presumed to arise from light that was scattered/reflected into the active area. Though this additional collection area was accounted for during the thresholding process, no correction should have been necessary given that an equivalent amount of light would have also been scattered/reflected out of the cell.

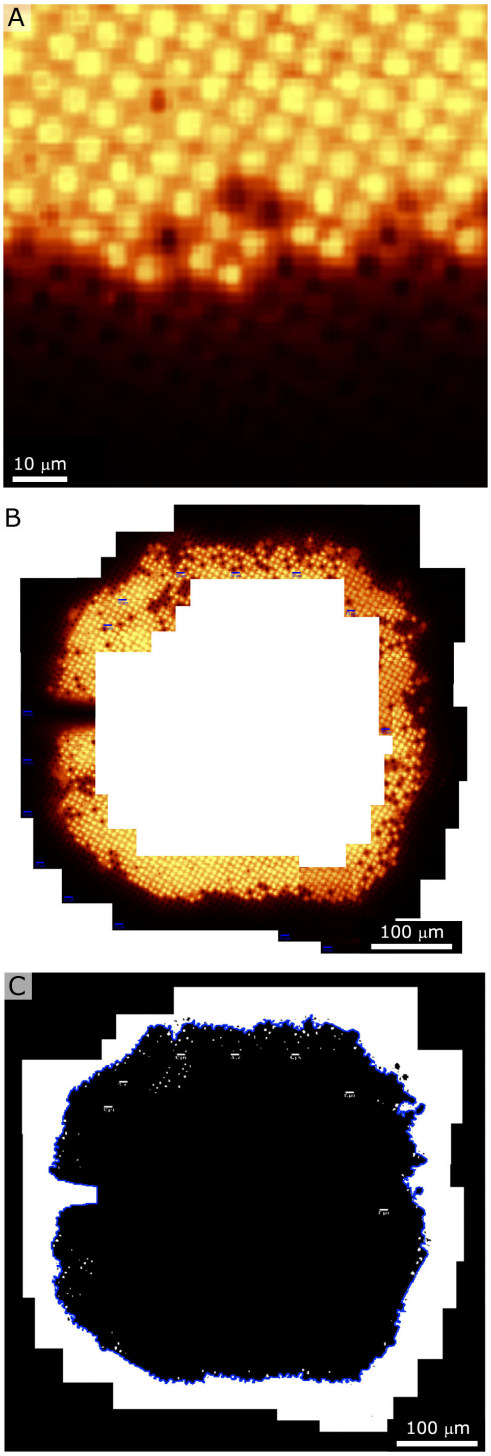


Figure 6.15. Measuring PRS C4R5s active area. (a) 90 μm x 90 μm scanning photocurrent microscopy (SPCM) image along the cell perimeter. (b) Twenty-six SPCM images over-laid to map out the cell perimeter. (c) Image of (b) after thresholding. The blue line is the cell perimeter from which the cell area was calculated.

6.5.2 Dark J-V

Figure 6.16a plots the measured current density as a function of voltage for the champion microwire solar cell of each cell type in the dark. The microwire solar cells exhibited rectifying behavior with diode ideality factors between 1.7 and 2.2. The roll-off in the current density near 0.5 V in forward-bias resulted from the series resistance of the solar cells, which ranged from 300 to 3000 Ω (Figure 6.16b) and was dependent upon the quality of the contact between the electrical probe and the ITO.

6.5.3 Light J-V and Photovoltaic Performance

Under simulated AM 1.5G illumination, the champion PRS solar cell exhibited markedly higher photovoltaic performance than the champion Scatterer and As-Grown solar cells, as a result of a significant increase in the short-circuit current density, as seen in Figure 6.17. Table 6.1 displays the open-circuit voltage (V_{oc}), the short-circuit current density (J_{sc}), the fill factor (FF), and the efficiency (η) for all microwire solar cells, whose cell areas were measured by SPCM. V_{oc} of $\sim$ 500 mV and $FF > 65\%$ was observed for all three cell types. (For each cell type, the majority of the cells were found to exhibit similar V_{oc} and FF, see Appendix D.) The champion PRS solar cell produced a V_{oc} of 498 mV, J_{sc} of 24.3 mA cm^{-2}, and FF of 65.4%, for an η = 7.92%. The champion Scatterer and As-Grown solar cells exhibited $\eta = 5.64\%$ and $\eta = 3.81\%$, respectively, with similar V_{oc} and FF but lower J_{sc}. For PRS and Scatterer cells the differences in η within a cell type largely resulted from differences in J_{sc}, which may result from either variations in the incorporation of the Al_2O_3 scattering particles or the fraction of electrically contacted wires (see Fig. figCellarea and Fig. 6.18b,c) between cells of the same type. We estimate the internal error in the measurement of the cell area to be 5% and the internal error in the AM 1.5G illumination intensity to be 5%, yielding a $\sim$ 7% internal error in the measurement of the J_{sc} and η.

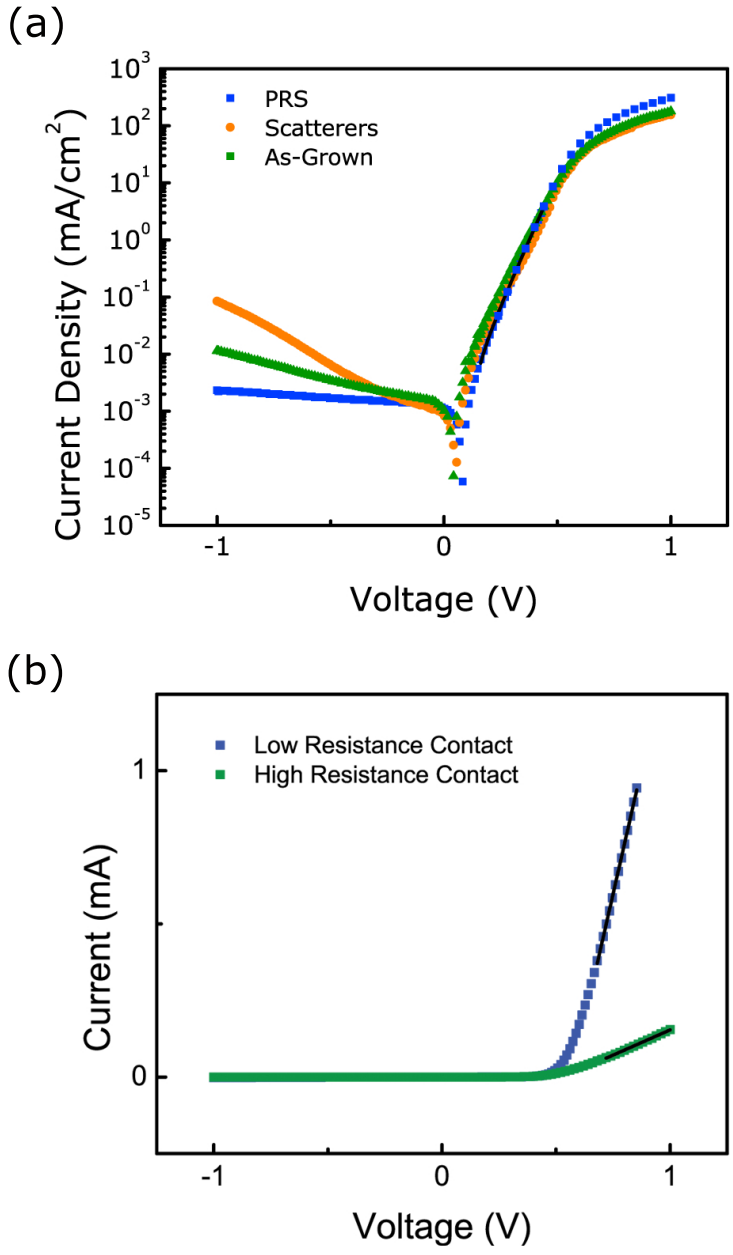


Figure 6.16. (a) Current density as a function of voltage for the champion microwire solar cell of each cell type in the dark. The black line in is an exponential fit to the dark J-V curve of the PRS solar cell and is used to extract an ideality factor of 1.8. (b) Current as a function of voltage on a linear scale for two microwire solar cells in the dark. The black lines are linear fits to the dark I-V curves and yield series resistances of 300 and 3000 Ω.

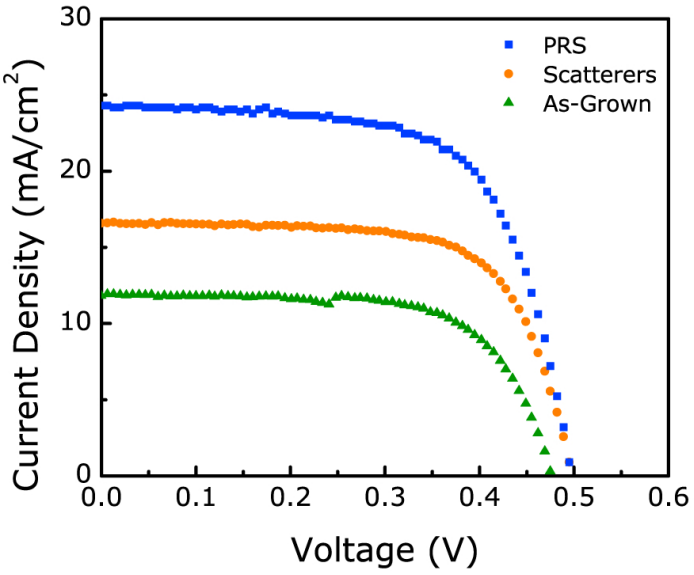


Figure 6.17. Current density as a function of voltage for the champion microwire solar cell of each cell type under simulated AM 1.5G illumination.

Table 6.1. Photovoltaic performance under simulated AM 1.5G illumination. The champion solar cell from each cell type is bolded.

Sample	V_{oc}**(mV)**	J_{sc}**(mA cm^{-2})**	FF**(%)**	η**(%)**
As-Grown C2R3	482	11.2	69.4	3.75
As-Grown C4R6	**482**	**11.8**	**67.5**	**3.81**
Scatterer C2R4	**499**	**16.6**	**68.0**	**5.64**
Scatterer C2R3	504	15.2	68.8	5.28
PRS C2R5	503	22.2	66.1	7.38
PRS C3R5	500	22.8	67.2	7.65
PRS C4R5	**498**	**24.3**	**65.4**	**7.92**

6.5.4 Photocurrent Mapping

To better understand the differences in J_{sc} between the PRS, Scatterer, and As-Grown solar cells, scanning photocurrent microscopy was used to map the photocurrent produced by the wire-array solar cells as a function of localized laser illumination ($\lambda =$ 650 nm, $\sim$1.0 μm beam waist), as seen in Figure 6.18. To facilitate comparison between the different types of cells, each scanning photocurrent image was normalized to its maximum photocurrent. The measured photocurrent was maximized when the laser illumination was centered on a wire and was minimized when the illumination was centered between four adjacent wires. The photocurrent cross-sections shown below each scanning photocurrent image indicated that the relative magnitude of the decay in photocurrent as the laser moved from a peak (centered on a wire) to a valley (between two adjacent wires) decreased from the As-Grown cell (Fig. 6.18a) to the Scatterer cell (Fig. 6.18b) and from the Scatterer cell to the PRS cell (Fig. 6.18c). In particular, the PRS solar cell exhibited nearly uniform absorption across the array, demonstrating that the Ag back reflector and Al_2O_3 dielectric scattering particles allowed for the effective collection of light incident between the wires.

The spots of greatly reduced photocurrent in the Scatterer and PRS solar cells arose from wires that were not electrically contacted by the ITO (wire vacancies would be expected to produce a photocurrent similar to the valley photocurrent, whereas, uncontacted wires parasitically absorb incident illumination.) Comparing Fig. 6.15b with Fig. 6.18c, the fraction of electrically inactive wires was higher near the cell perimeter (2-20%) than at the cell center ($\sim$2%), which is not unexpected given the decreased ITO thickness at the device edge. The small fraction of electrically inactive wires, at the cell center, seen for the PRS and Scatterer cells may result from the presence of Al_2O_3 scattering particles at the wire tips preventing the fabrication of a good electrical contact between the n-Si emitter and the ITO.

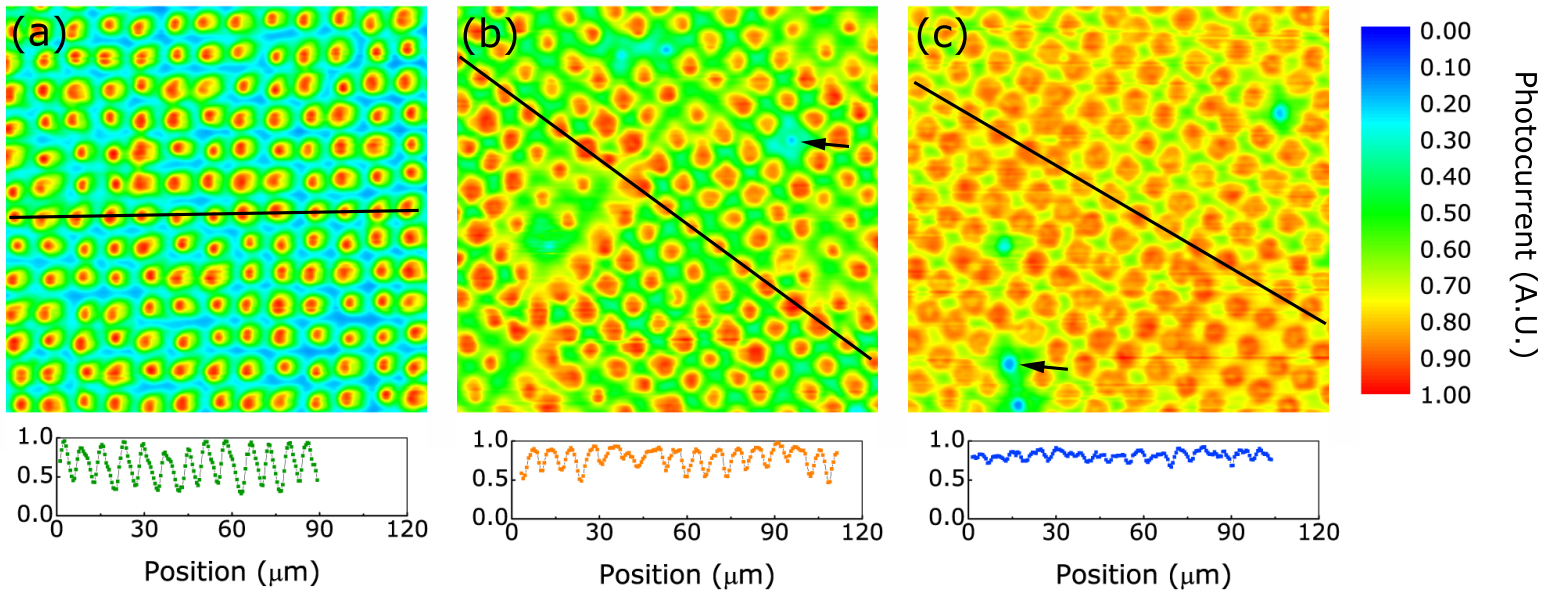


Figure 6.18. Scanning photocurrent microscopy (SPCM) images and associated photocurrent line profiles from the center of (a) an As-Grown solar cell, (b) a Scatterer solar cell, and (c) a PRS solar cell. The SPCM images are 90 μm x 90 μm and normalized to the maximum measured photocurrent of each image. The black lines on each SPCM image denote the cross-section used to produce the associated photocurrent line profiles. The black arrows denote spots of greatly reduced photocurrent.

6.5.5 Spectral Response

As seen in Figure 6.19, the As-Grown and Scatterer solar cells exhibited similarly shaped spectral response curves (though different in absolute magnitude), both exhibiting a decline in the external quantum yield (EQY) at wavelengths > 550 nm. By comparison, the PRS solar cell exhibited nearly constant EQY between 500 nm and 800 nm. The increased red and infrared response of the PRS cell presumably arose from light incident between the wires that was scattered multiple times from the Al_2O_3 scattering particles and the Ag back reflector. Integration of the observed EQY with the AM 1.5G solar spectrum predicted J_{sc} values of 13.3 mA cm^{-2}, 18.0 mA cm^{-2}, and 23.3 mA cm^{-2} for the As-Grown, Scatterer, and PRS solar cells, respectively, in good agreement with the measured J_{sc} values.

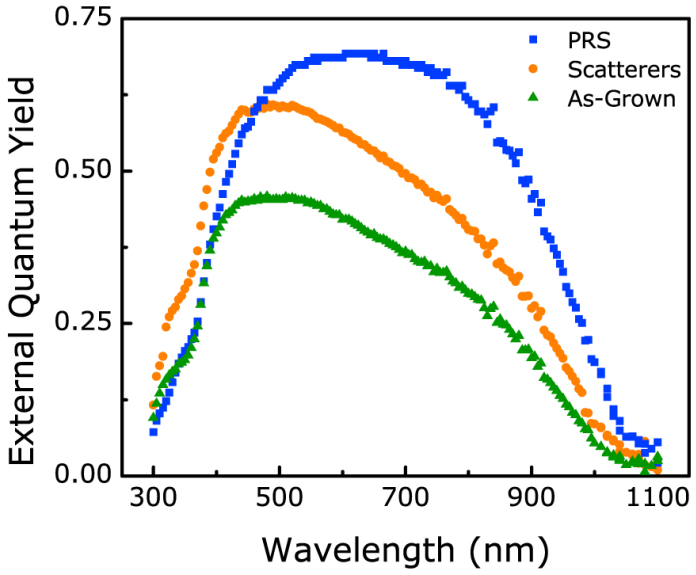


Figure 6.19. Spectral response of the champion Si microwire solar cell of each cell type.

6.6 Discussion

6.6.1 Photocurrent Response from the Growth Substrate

An important consideration for measurements of the photovoltaic performance of wire-array solar cells is the contribution to the observed photocurrent from the growth substrate. Though the fabrication of an appropriate control cell is not straightforward (even if the emitter doping compensated the substrate doping, the n^+ emitter and p^{++} substrate would form a tunnel junction) significant photocurrent from the substrate can be ruled out in our microwire-array solar cells. For the As-Grown and Scatterer solar cells, scanning photocurrent microscopy measurements indicated a $<$ 0.5 μm effective minority-carrier diffusion length for electrons in the thermal oxide coated bases of the wires.[59] Consequently, neither the growth substrate nor the lower 27-32 μm of the wires contributed significantly to the observed photocurrent of the As-Grown and Scatterer solar cells. For the PRS microwire solar cells, the removal of the thermal oxide, followed by the deposition of the a-SiN_x:H passivation layer, produced an effective electron minority-carrier diffusion length $>>$ 30 μm in the p-type bases of the wires.[59] Taken together, these results suggest that the bulk minority carrier diffusion length is $>>$ 30 μm throughout the wire but that the thermal oxide coated bases of the wires, for the Scatterer and As-Grown cells, exhibited very high surface recombination velocities, limiting the effective diffusion length in the oxide-coated wire bases to $<$ 0.5 μm. Hence, a photovoltaic response from the entire length of the wires was possible for the PRS solar cells. However, the photovoltaic contribution from the substrate for the PRS cells should be negligibly small. The optically thick Ag back reflector coated the entire substrate except for where the wires had grown, ensuring that only the light guided through the Si microwires was able to reach the substrate. Consequently, 95% of the illumination $\leq$ 800 nm should be absorbed over the 43-49 μm length of the wires, by a simple Beer-Lambert law analysis. The remaining illumination entered the p^{++} Si substrate ($\rho < 0.001$ Ω cm), which has been shown to exhibit an external quantum yield $<$ 0.05 for 800 nm -1100 nm illumination.[59, 60]

6.6.2 Comparing Between Cell Types

The three types of microwire solar cells were fabricated to facilitate a comparison between the cell types. However, three differences between the cells are worth noting. First, the wire length and thermal oxide heights translated to active wire lengths of 27-33 μm, 41-48 μm, and 43-49 μm for the As-Grown, Scatterer and PRS solar cells, respectively. Assuming no reflection losses and single-pass absorption, the theoretical increase in J_{sc} from a 30 μm-thick Si wafer to a 45 μm-thick Si wafer is 1.75 mA cm^{-2}, a 5.3% increase. Applying a 5.3% increase to the 11.8 mA cm^{-2} J_{sc} of the As-Grown champion solar cell yields a J_{sc} of 12.4 mA cm^{-2}, well short of the observed 16.6 mA cm^{-2} J_{sc} for the Scatterer champion solar cell. Thus, the additional active wire length alone cannot explain the increase in J_{sc} from the As-Grown solar cells to the Scatterer solar cells. Second, the Al_2O_3 scattering particles were largely located adjacent to the photo-inactive, thermal oxide coated, bases of the wires in the Scatterer solar cells. Consequently, the full effect of the Al_2O_3 scattering particles is unlikely to have been seen in the Scatterer solar cells. Third, for the PRS and Scatterer cell types, $\sim$2% of the wires in the center of the cell (Fig. 18b,c) and 2-20% of the wires near the perimeter of the cell (Fig. 15b) were not electrically active. Thus, with improved contacting, the PRS and Scatterer cell types would be expected to produce a still higher J_{sc} and η.

6.7 15% Efficient Solar Cells

The fabrication of Si microwire-array solar cells with efficiencies of $\sim$15%, as compared to the simple theoretical expectation of 17%, should be possible by increasing the short-circuit current density to 32 mA cm^{-2}, increasing the fill factor to 80%, and increasing the open-circuit voltage to 600 mV, as detailed below.

6.7.1 Short-Circuit Current Density (J_{sc})

Previously, we have shown that wire-array photoelectrochemical cells can exhibit near-unity internal quantum yields.[15] We have also shown that Si microwire arrays can absorb 96% of the visible solar spectrum and exhibit day-integrated absorption > 85% of the above bandgap solar spectrum.[15] Consequently, near-unity external quantum yields resulting in a J_{sc} of 35.9 mA cm^{-2} (not accounting for contact shading) should be possible through improved light trapping in microwire-array solar cells.

Lower than unity external quantum yields in the microwire-arrays solar cells reported can be attributed to three factors. First, a significant fraction of Al_2O_3 particles collected at the wire tips. The presence of dielectric scatterers at the top of the solar cell is expected to increase reflection losses. Additionally, the presence of Al_2O_3 particles at the wire tips likely led to the observed fraction (a few percent) of uncontacted wires. Second, the Si microwires in the PRS cell were only between 45 and 49 μm in length, as compared to 67 μm in the absorption study. Ideal wire lengths for microwire-array solar cells are thought to fall between 80 and 100 μm. Third, the indium tin oxide (ITO) layer was 150 nm-thick. If the ITO thickness could be reduced to 80 nm, there would be lower reflection losses and roughly half the parasitic absorption losses. Incorporating these improvements (the growth of longer wires and a more ideal incorporation of the Al_2O_3 scattering particles at the base of the wire-array have already been shown), short-circuit current densities of 32 mA cm^{-2} should be possible (accounting for contact shading).

6.7.2 Fill Factor (FF)

Single-wire solar cells have exhibited open-circuit voltages up to 600 mV and fill factors up to 82%.[59] The lower fill factors of 65-70% observed in the microwire-array solar cells are related, at least in part, to the cell series resistance, which is typically between 0.45 and 4.5 Ω cm^2, and thus expected to partially degrade the fill factor.[77] The addition of a metallic top contact grid (shadowing losses are accounted for in the short-circuit current density quoted above), should significantly reduce the

series resistance of the solar cells and lead to noticeable gains in the fill factor.

6.7.3 Open-Circuit Voltage (V_{oc})

The difference in open-circuit voltage between the best single-wire solar cells (600 mV) and the microwire arrays can be partly attributed to the use of an amorphous Si layer between the Si wire and the Al contacts in single-wire solar cells with high V_{oc}.[59] Furthermore, the microwire-array solar cells have a much larger contact area (as a fraction of the total wire area), than the single-wire solar cells as a result of our current fabrication methods. This additional contact area leads to increased recombination (ohmic contacts are essentially perfect recombination sources for carriers) and consequently an increased dark saturation current and decreased open-circuit voltage.[77]

6.8 Conclusion

In this chapter we have demonstrated that microwire-array solar cells fabricated from arrays of VLS-grown Si microwires can exhibit significant performance with $V_{oc} >$ 500 mV, $J_{sc} > 24$ mA cm^{-2}, FF approaching 70%, and $\eta = 7.9\%$. We have also demonstrated that optical light-trapping elements, such as a back reflector and/or dielectric scattering particles, are important for realizing high short-circuit current densities in wire-array solar cells through the capture of illumination incident between wires and the collection of red and infrared illumination.

Chapter 7

Outlook

7.1 The Potential of Si Microwire-Array Solar Cells

As detailed at the end of Chapter 6, the fabrication of Si microwire-array solar cells with efficiencies of ∼15% should be possible without significant technological advances. These efficiencies, in combination with the ability to grow arrays of Si microwires over large areas (> 1 cm^2),[27] to peel the wire arrays from the growth substrate in a flexible polymer,[14] and to re-use the growth substrate,[32] indicate that the fabrication of flexible, high efficiency c-Si solar cells should be possible.[13, 57] If realized, these solar cells would possess a clear efficiency advantage over First Solar's market leading cadmium tellurium (CdTe) technology, while hopefully offering a similar, or even lower, cost per watt.

Two recent results in our lab further demonstrate the potential for Si microwire-array solar cells to be (1) flexible and (2) high efficiency. First, using a thin metallic film as a back-contact to a peeled wire array, Josh Spurgeon has shown that wire-array cells exhibit nearly identical photoelectrochemical performance to on-wafer wire-array cells.[78] Second, as shown in Figure 7.1, Michael Kelzenberg and Dan Turner-Evans have shown that single-wire solar cells can exhibit efficiencies of 17.4% when operating at the per wire short-circuit current (calculated from optical and device physics modeling) for a wire-array solar cell with optimal light-trapping.[59]

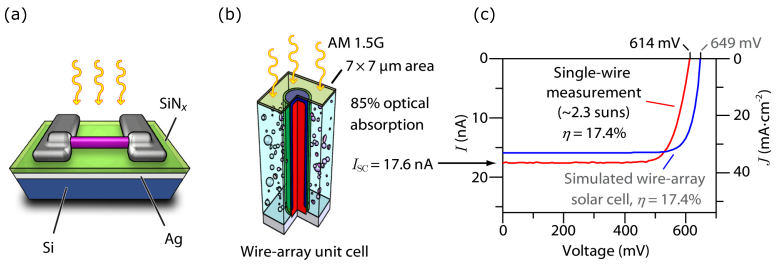


Figure 7.1. (a) Schematic of the single-wire solar cell measurement geometry. (b) Cartoon of the wire-array unit cell used in optical and device physics modeling. (c) Photovoltaic performance of a single-wire solar cell operating at the per wire short-circuit current of a wire-array solar cell with optimal light absorption.[59]

7.2 Advanced Device Design

The growth of a p-n junction in-situ would allow for a significant reduction in the number of processing steps (growth of a thermal oxide, PDMS deposition, selective oxide removal, PDMS removal, and emitter diffusion) and thus represent an additional advance in the development of Si microwire-array solar cells. One method for creating an in-situ junction would be through dopant modulation during growth to produce an axial p-n junction. The use of an axial p-n junction would require minority-carrier diffusion lengths on the order of the wire length, $\sim$90 μm. However, recent work has shown that Si microwires passivated with an a-SiN$_x$:H layer exhibit minority-carrier diffusion lengths >> 30 μm.[59] Thus, the minority-carrier diffusion length may already be sufficiently long for the use of an axial p-n junction. An additional benefit of the axial p-n junction is that it reduces the area of the p-n junction. As compared to a radial p-n junction that covers the top 60 μm of a 2 μm diameter wire, an axial p-n junction in the same wire would have $< 1/100^{th}$ the junction area. Assuming a diode ideality factor of 1, this translates to an expected increase in the open-circuit voltage of 120 mV.[50]

One potential challenge to the implementation of an in-situ, axial p-n junction is the abruptness of the p-n junction that can be created through dopant modulation.

The Cu/Si alloy is a reservoir for the dopant species and even an abrupt modulation of the gas composition is not sufficient to produce an abrupt modulation of the dopant species within the grown wire.[79] Consequently, the dopant modulation will need to be optimized to create as abrupt a p-n junction as possible to minimize unnecessary loses in the open-circuit voltage.[80]

Other means of creating a p-n junction with fewer processing steps would be a thermal diffusion or the deposition of an amorphous Si heterojunction immediately after wire growth. Both of these options would produce a radial junction that extended over the length of the wire. As noted in section 6.3.1, this structure is likely to result in a shunt between the p and n regions (or Si and amorphous Si regions, in the case of the heterojunction) at the back contact. However, selective etching methods may allow for sufficient removal of the diffused or deposited layer that a dielectric infill could then be deposited and used to isolate the p and n regions prior to the deposition of a back contact.

7.3 Future Technologies

In addition to showing great promise as single-junction solar cells, arrays of Si microwires appear to be a promising platform for the development of multi-junction solar cells and water-splitting devices.[81, 82] Multi-junction solar cells often suffer from material defects incurred as a result of the lattice mismatch between different semiconductors. Consequently, semiconductors that are closely latticed-matched must be chosen. But, the choice of latticed-matched semiconductors limits the number of junctions that can be used and often results in a less than ideal combination of bandgaps.

As shown in Figure 7.2, the advantage of the wire geometry for multi-junction solar cells is that defects induced at the interface between lattice-mismatched semiconductors will propagate out of the wire in the radial direction. Additionally, the small length scale in the radial direction of the wire will limit the amount of strain that can accumulate before the unconstrained wire surface is reached, thereby min-

imizing the number of defects that are created. As a result, only a small region of the cell volume will be photoinactive. By limiting the photoinactive region to a small region of the wire near the interface(s) between the different semiconductors (where a photoinactive tunnel junction is already required) wire-array solar cells should allow for the selection of semiconductors with optimal bandgap spacings. Not surprisingly, recent work in the field has investigated the various combinations of axial semiconductor heterostructures that can be grown using the VLS-growth method.[83]

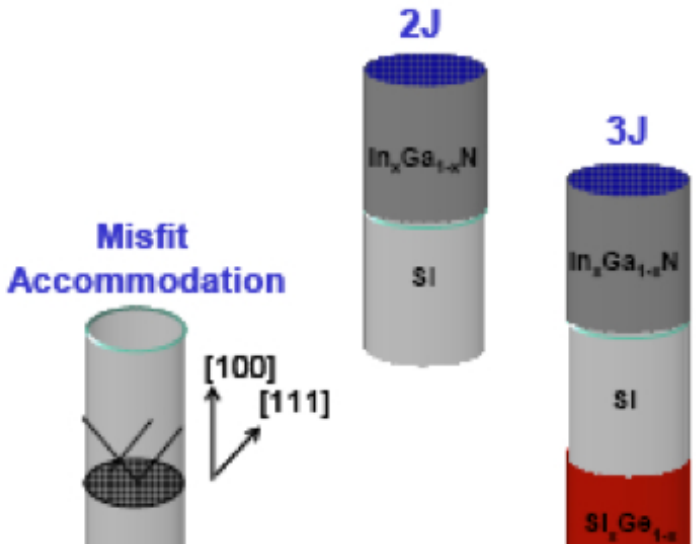


Figure 7.2. Schematic of multi-junction wire solar cells and defect accommodation in the radial direction.

As shown in Figure 7.3, wire-arrays also offer an exciting geometry for water-splitting applications. One of the main challenges water-splitting devices face is the discovery of low-cost, earth-abundant catalysts with turnover rates that are sufficiently high to harvest the photon flux of the solar spectrum. Catalysts, such as Pt, have sufficiently high turnover rates, but are not earth-abundant or cost-effective enough to be used on a global scale. As an alternative to the discovery of earth-abundant catalysts with high turnover rates, semiconductor wire arrays can provide a 10-fold increase in the semiconductor surface area over which water-splitting catalysts can be deposited. By increasing the potential for catalyst loading 10-fold, semiconductor wire arrays may facilitate the development of water-splitting devices

for use on the global scale through the use of less costly and more earth abundant catalysts.

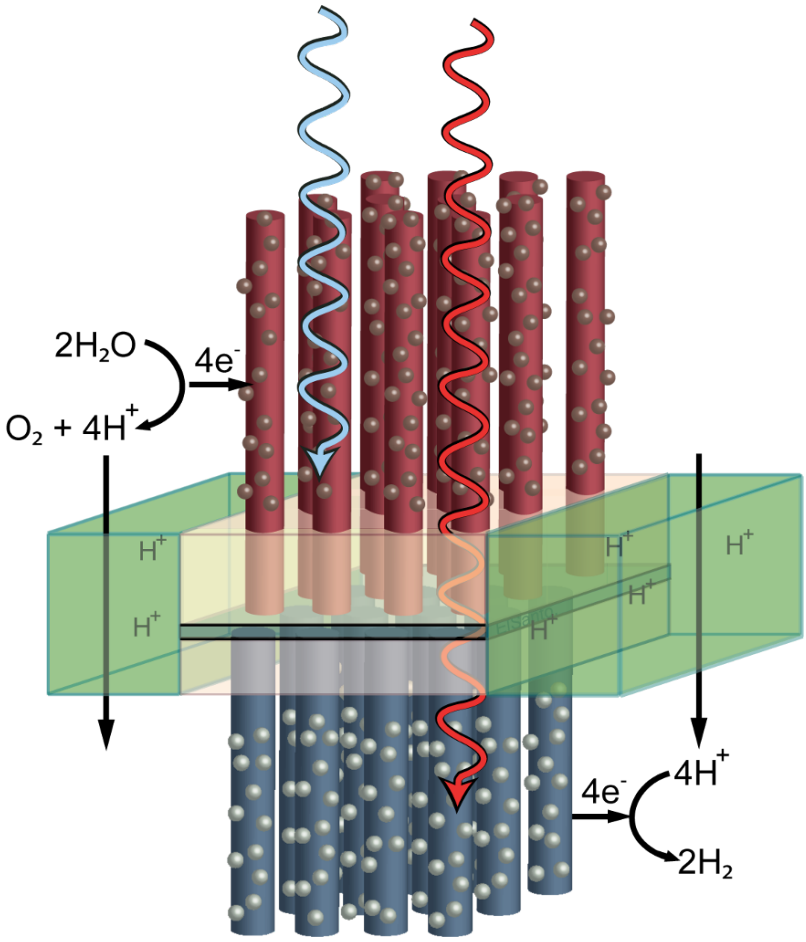


Figure 7.3. Schematic of a wire-array water-splitting device. The increased surface area of the cell may allow for the use of earth-abundant catalysts with lower turnover rates than expensive and rare catalysts like Pt.

7.4 Conclusions

This thesis has detailed the fabrication and characterization of Si wire-arrays for use as solar cells. In Chapter 2, we used the vapor-liquid-solid (VLS) growth method to fabricate arrays of vertically aligned, Si microwires with nominally identical wire heights and diameters. These structures have proved immensely useful for characterizing and understanding the inherent photovoltaic properties of wire-array solar cells. In Chapter 3, we used secondary ion mass spectrometry to study the Au concentration in Au-catalyzed, Si wires. Our measurements led us to the conclusion that VLS-catalysts are likely incorporated at their thermodynamic equilibrium concentration under our growth conditions. This finding motivated a switch to the use of Cu as the VLS-catalyst. In Chapter 4, we demonstrated that in situ doping using BCl_3 could be used to modulate the electrically active dopant concentration from 8×10^{15} cm^{-3} to 4×10^{19} cm^{-3} in p-Si microwires, which was critical to the fabrication of efficient solar cells in the radial p-n junction geometry. In Chapter 5, it was shown that Cu-catalyzed wires exhibited long (10 μm) minority-carrier diffusion lengths, as expected from our measurement of the VLS-catalyst incorporation in Chapter 3. These minority-carrier diffusion lengths indicated that the fabrication of efficient microwire solar cells should be possible. In Chapter 6, we constructed Si microwire-array solar cells with open-circuit voltages up to 500 mV, short-circuit current densities up to 24.3 mA cm^{-2}, and fill factors $> 65\%$, achieving an Air Mass 1.5 Global solar conversion efficiency of 7.9%. These solar cells used multiple light-trapping features (Al_2O_3 particles, a Ag back reflector, and an a-SiN_x:H antireflection layer) to ensure the efficient collection of light incident on both the wires and the area between wires. Finally, in Chapter 7, we discussed the potential for further improvements in Si microwire-array solar cells and for their use as multi-junction solar cells and in water-splitting devices. Taking the results of this thesis and our previous work, we believe that Si microwire-array solar cells have the strong potential to reduce the costs of solar electricity and solar fuels.

Appendix A

Array and Solar Cell Fabrication

Catalyst Patterning

1. The growth substrates were boron-doped p^{++}-Si (111) wafers, having a resistivity, $\rho < 0.001\ \Omega$ cm, that were coated with 450 nm of thermal oxide (Silicon Quest International).

2. Place the wafer on the spinner and turn on the vacuum. Blow off any dust particles from the wafer surface with a N_2 gun. Coat the wafer surface with MCC Primer 80/20 (Microchem), wait for 10 s, and then spin dry for 30 s at 3000 rpm (acceleration index ACL=100).

3. Coat the wafer with S1813 photoresist (Microchem), and then spin at 3000 rpm for 1 min (acceleration index ACL=100).

4. Cure on a hotplate at 115 °C for 2 mins.

5. Photolithographically pattern the resist using the Karl Suss MA 6 mask aligner. Expose for ∼10s (exact time will vary with bulb age and should be recalibrated from time to time) in 'Hard Contact' mode. *For the wire-array solar cells of Chapter 6, an array of 4-μm-diameter circular holes, on a square lattice with a 7 μm pitch, was defined in the oxide. This was done by using a photomask with an array of 3-μm-diameter circular holes, on a square lattice with a 7 μm pitch, and slightly over-exposing the resist.*

6. Place the sample in MF-319 developer (Microchem) for 60s. Check with the optical microscope that the pattern has come out correctly, and if not adjust the exposure time accordingly for subsequent patterns.

7. Cure on a hotplate at 115 °C for 15 min.

8. After development of the pattern, the oxide within the patterned holes can be removed by immersion of the samples for 3 mins in buffered HF (Transene). The BHF etches the oxide at ∼2 nm/s.

9. Thermally evaporate either Au (Electronic Space Products International, 3N5 purity), Cu (EPSI Metals, 6N purity) or Ni (Electronic Space Products International, 4N5 purity). The evaporator settings for each metal are: Au: density = 19.30 g cm^{-3}, z-ratio = 0.381 Cu: density = 8.93 g cm^{-3}, z-ratio = 0.437 Ni: density = 8.85 g cm^{-3}, z-ratio = 0.331 and we use tooling factor = 148%. (Note that the liquid nitrogen cooled stage is required for best results with Ni. Start LN_2 cooling 10 mins before starting to heat the metal to ensure the samples reach a low enough temp. Note also that with the cooled stage and a tooling factor of 148%, the quartz crystal monitor overestimates the thickness of the deposited metal film by roughly a factor of 3). *For the wire-array solar cells of Chapter 6, 600 nm of Cu was deposited.*

10. Lift off the resist and excess catalyst by submerging the sample in acetone and (if necessary) leaving overnight and/or (if necessary) sonication. Rinse sample in acetone, isopropanol, methanol, and finally DI water before drying with nitrogen.

Wire Array Growth

1. Cleave the patterned samples to the desired size and transfer to the $SiCl_4$ reactor. *For the wire-array solar cells of Chapter 6, 600 nm of Cu was deposited, the samples were approximately 1.5 cm × 1.5 cm in dimension*

2. Anneal the samples at 1000 °C for 20 mins under 1 atm of H_2 at a flow rate of 500 sccm.

3. Wire growth was performed by the introduction of $SiCl_4$ (Strem, 99.9999+%), BCl_3 (Matheson, 0.25% in H_2), and H_2 (Matheson, research grade) at flow rates of 10, 1.0, and 500 sccm, respectively, for 30 min. Growth rate varies depending upon catalyst, ∼2-3 μm / min for gold, ∼2-7 μm / min for Cu and Ni. *Directions for operation of the $SiCl_4$ reactor are provided below.*

4. Following growth, the tube was purged with N_2 at 200 sccm and was allowed cool to ∼ 650 °C over the course of ∼30 min.

A few minor differences are worth noting from our previously published work.[27] First, removable 1" diameter quartz tubes, dedicated to the individual growth catalysts (Au, Cu and Ni), have been inserted into the 1.5" diameter reactor tube to reduce catalyst cross-contamination. As a result the reactant flow rates were reduced by half from 1000 to 500 sccm (H_2) and from 20 to 10 sccm ($SiCl_4$) to obtain optimal growth. This reduction in the reactant flow rate is directly proportional to the decrease in the cross-sectional area of the reactor. Secondly, the grown samples are cooled in the reactor to a temperature of 750 °C over ∼ 10 min prior to removing the samples from the reactor. This slow cooling step has been added to mitigate any negative effects on the electrical properties of the wire associated with rapid cooling from 1000 °C.

p-n Junction Definition

1. Following growth the Cu catalyst was removed from the wire arrays by etching in 5% HF(aq) for 30 s, 6:1:1 by volume H_2O:H_2O_2(30% in H_2O):conc. HCl (aq.) at 75 °C for 15 min, and 20 wt % KOH (aq.) at 20 °C for 60 s.

2. A conformal SiO_2 diffusion-barrier that was 200 nm in thickness was grown via dry thermal oxidation at 1100 °C for 2 h.

3. The wire array samples were then coated with a solution that contained 4.4 g hexamethycyclotrisiloxane (Sigma-Aldrich), 1 g PDMS (Sylgard 184, Dow

Corning), and 0.10 g of curing agent in 5 ml of dicholoromethane; spun at 1000 RPM for 30 s; and cured at 150 °C for 30 min, to produce a 10-20 μm thick PDMS layer selectively at the base of the wire array.[14]

4. After a quick etch ($\sim$2 s) in a 1:1 mixture of 1.0 M tetrabutylammonium fluoride in tetrahydrofuran (Sigma-Aldrich) and dimethylformamide (PDMS etch)[76] and a DI rinse, these partially infilled arrays were immersed for 5 min in BHF, to remove the exposed diffusion-barrier oxide.

5. The PDMS was then completely removed by etching for 30 min in PDMS etch. A 10 min piranha etch (3:1 aq. conc. H_2SO_4:H_2O_2) was performed to remove residual organic contamination.

6. After etching the wires for 5 s in 10% HF (aq), thermal P diffusion was performed using solid source CeP_5O_{14} wafers (Saint-Gobain, PH-900 PDS) at 850 °C for 10 min (As-Grown and Scatterer) or 15 min (PRS) under an N_2 ambient, to yield a radial p-n junction in the wire regions unprotected by the thermal oxide.

7. A 30 s etch in BHF was used to remove the surface dopant glass.

Device Fabrication and Contacting

The As-Grown cell was fabricated as follows:

1. After p-n junction fabrication, the wire array was heated to 150 °C on a hot plate, and mounting wax (Quickstick 135, South Bay Tech.) was melted into the array.

2. Excess wax was removed from the array using a glass coverslip.

3. The mounting wax was then etched in an O_2 plasma (400 W, 300 mTorr) until the wire tips were sufficiently exposed for electrical contacting (30-90 min).

4. After etching with BHF for 30 s, 150 nm of indium tin oxide [0.0007 Ω cm] was sputtered (48 W, 3 mTorr, 20:0.75 sccm Ar:10% O_2 in Ar) through a shadow mask, to serve as a transparent contact to the n-type shell of the Si microwires, thereby defining the area of the microwire solar cells.

5. Contact to the p-type core of the Si microwires was established through the p^{++}-Si substrate by scribing a Ga/In eutectic onto the back side of the growth wafer. The backside of the p^{++}-Si substrate was then placed onto a piece of Cu tape, which was mounted to a glass microscope slide for structural support. An alligator clip was then used to make electrical contact to the Cu tape, and thus the base of the wire array during electrical measurements.

Fabrication of the Scatterer cell was performed identically to that of the As-Grown cell, except that prior to infilling with wax, Al_2O_3 light-scattering particles (0.08 μm nominal-diameter, South Bay Technology) were added to the wire array.

1. The wire-array was placed face-up in a flat-bottomed glass centrifuge tube and $\sim$ 3 mL of an ethanolic dispersion of the particles ($\sim$0.3 mg/ml) were added. Centrifugation ($\sim$3000 RPM) for 5 min was used to drive the particles to the base of the wire-array.

Fabrication of the PRS cell was performed identically to that for the Scatterer cell, except that prior to the addition of the Al_2O_3 particles, an a-SiN_x:H passivating layer and a Ag back reflector were added to the cell.

1. After p-n junction fabrication, the wire arrays were etched for 5 min in BHF, to completely remove the remaining oxide diffusion barrier.

2. A standard clean was then performed (10 min in 5:1:1 by volume H_2O:H_2O_2(30%

in H_2O): NH_4OH(15% in H_2O) at 75 °C, 30 s in BHF, 10 min in 6:1:1 by volume H_2O:H_2O_2(30% in H_2O):conc. HCl (aq.) at 75 °C, 30 s in BHF).

3. An *a*-SiN_x:H layer (∼140 nm thick at the wire tip and ∼60 nm thick at the wire base) was then deposited using plasma-enhanced chemical vapor deposition, as described previously.[15]

4. The *a*-SiN_x:H was etched for 15 s in BHF, prior to the deposition of a total of 1 μm planar-equivalent of Ag via thermal evaporation (two successive 500 nm evaporations at two different specimen-tilt angles (± ∼5 degrees) with sample rotation, to ensure continuous coverage of the growth substrate). The array was then infilled with ∼5 μm of PDMS using a process similar to the one described above. This PDMS etch barrier allowed the Ag at the wire tips and sidewalls to be selectively removed by etching for 6.5 min in 8:1:1 methanol: NH_4OH(15% in H_2O): 30 wt.% aq. H_2O_2. A thin layer (∼40 nm) of SiO_2 was then sputtered to improve the incorporation of the Al_2O_3 particles. The Al_2O_3 scattering elements, mounting wax, and ITO were then added as described above.

$SiCl_4$ CVD System Operating Instructions

These instructions are not intended to be a substitute for being trained by an experienced user. If there are any problems or questions, please contact Morgan Putnam (x3657 or 612-703-5201 (cell)) or Daniel Turner-Evans (x2380 or 203-671-1338 (cell)).

Reactor Location: 251 Thomas J. Watson Laboratories of Applied Physics, California Institute of Technology

1. Check the temperature readings on the Eurotherm controllers.

   (a) If no one has been using the system, zones 1, 3, and 5 should be at 0 °C. These three control the left, center, and right segments of the tube furnace, respectively. If you need to change the tube liner for your material,

do so now (see end for instructions). Set them to your process temperature (typically 1000 °C). Do not set the tube temperature above 1100 °C the furnace was originally designed for MOCVD processes and may be damaged by very high temperature settings.

(b) Zones 2 and 4 should be 90 °C at all times. They control the heating tape on the tubing leading from the $SiCl_4$ bubbler to the tube furnace, and the heating tape on the $SiCl_4$ MFC, respectively. The tubing needs to be at 90 °C to prevent condensation, and the MFC needs to be at 120 °C to prevent condensation.

(c) Zone 6 is a second readout of the temperature of the tubing, just upstream of the quartz tube. It doesnt control anything and therefore does not need to be set.

(d) Zone 7 controls the temperature of the $SiCl_4$ bubbler. It should be at 50 °C if the reactor is not being used. Set zone 7 to 80 °C for growth.

(e) Give the system at least 30 mins to reach a stable operating temperature.

2. Check that the liquid level in the NaOH scrubber is between 10 and 14 gallons if not, contact the current guru and wait until the problem is rectified before continuing. Plug in the scrubber pump and ensure that it is functioning (it should be audible).

3. Note the base pressure in the furnace tube. Close the vacuum line (top valve).

4. After the reactor has reached your desired temperature, vent the system with N_2. Monitor the pressure reading. When it reaches about 730 Torr (which takes about 5 mins), open the clamp on the quick flange (QF) connection at the end of the steel three way connection.

5. Remove the quartz boat, load your sample into it, and push the boat back into the furnace.

6. Replace the QF cap and tighten the clamp.

7. Open the process line (bottom valve), and monitor the pressure (ensure that the pressure stays constant at ∼735 Torr).

8. Turn off the N_2, turn on the H_2 (500 sccm at the current time).

9. Wait for 20 mins for the sample and boat to reach a uniform temperature. During this time adjust the $SiCl_4$ and BCl_3 setpoints to your desired values. (10 sccm for $SiCl_4$ at the current time)

10. When ready to begin growth, switch on the $SiCl_4$ and BCl_3, wait 10 s and then open the blue valves downstream of the $SiCl_4$ and BCl_3 MFCs. Ensure that the $SiCl_4$ and BCl_3 flow rates reach the desired set points.

11. Wait for the desired growth time.

12. Turn off the H_2, $SiCl_4$ and BCl_3. Close the blue valves just downstream of the $SiCl_4$ and BCl_3 MFCs.

13. Close the process line (bottom valve).

14. ENSURE THAT THE PROCESS LINE IS CLOSED (bottom valve). (Always ensure that the process line is closed before opening the vacuum line to prevent a closed loop between the vacuum pumps inlet and outlet which could result in a small H_2 explosion.)

15. Open the vacuum line (top valve), slowly, monitoring the pressure. If the pressure does not drop, close the vacuum line again and make sure that the process line is fully closed. If you wish, you may leave the N_2 flowing for 30 sec to a few minutes to fully purge the system.

16. Lower the reactor temperature set-points (Zones 1, 3 and 5) to 750 °C. (A slow cooling to 750 °C was chosen to ensure reproducible results and to allow for possible outdiffusion of impurities.

17. Wait for 1-2 mins, the pressure should be within a few tenths of a Torr of the initial vacuum pressure. Close the vacuum line (top valve).

18. Switch on the N_2 and bring the tube back to atmospheric pressure. When the pressure reaches about 730 Torr (which takes about 5 mins), open the tube.

19. BE SURE NOT TO MELT THE PYREX WHEN REMOVING YOUR SAMPLE. (The quartz tube gives way to pyrex before connecting to the steel QF connections at either ends). Use the quartz rod to pull the boat all the way into the steel three-way connection. Note the boat may overhang the quartz tube liner slightly but should not be touching the steel. Finally, after waiting at least 2 minutes, draw the quartz boat onto the quartz boat holder.

20. Replace the QF cap and tighten the clamp.

21. Turn off the N_2. Open the vacuum line (top valve) to pump down the system. Ensure the pressure returns to a value similar to the initial base pressure.

22. Set the temperatures back to their idle set points (zones 1, 3, and 5 at 0 °C, and zone 7 at 50 °C).

23. Update the excel spreadsheet.

24. Unplug the NaOH scrubber pump.

Changing the tube liner:

1. Close the vacuum line (top valve).

2. Vent the system with N_2. Monitor the pressure reading. When it reaches about 730 Torr (which takes about 5 mins), open the clamp on the quick flange (QF) connection at the end of the steel three way connection.

3. Take out the old tube liner, slide it into the appropriately labeled bag, and store it on the back of the reactor. Obtain the tube liner necessary for your conditions and insert it into the furnace.

4. Replace the QF cap and tighten the clamp.

5. Turn off the N_2

6. Open the vacuum line (top valve), slowly, monitoring the pressure. If the pressure does not drop, close the vacuum line again and make sure that the process line is fully closed.

A.1

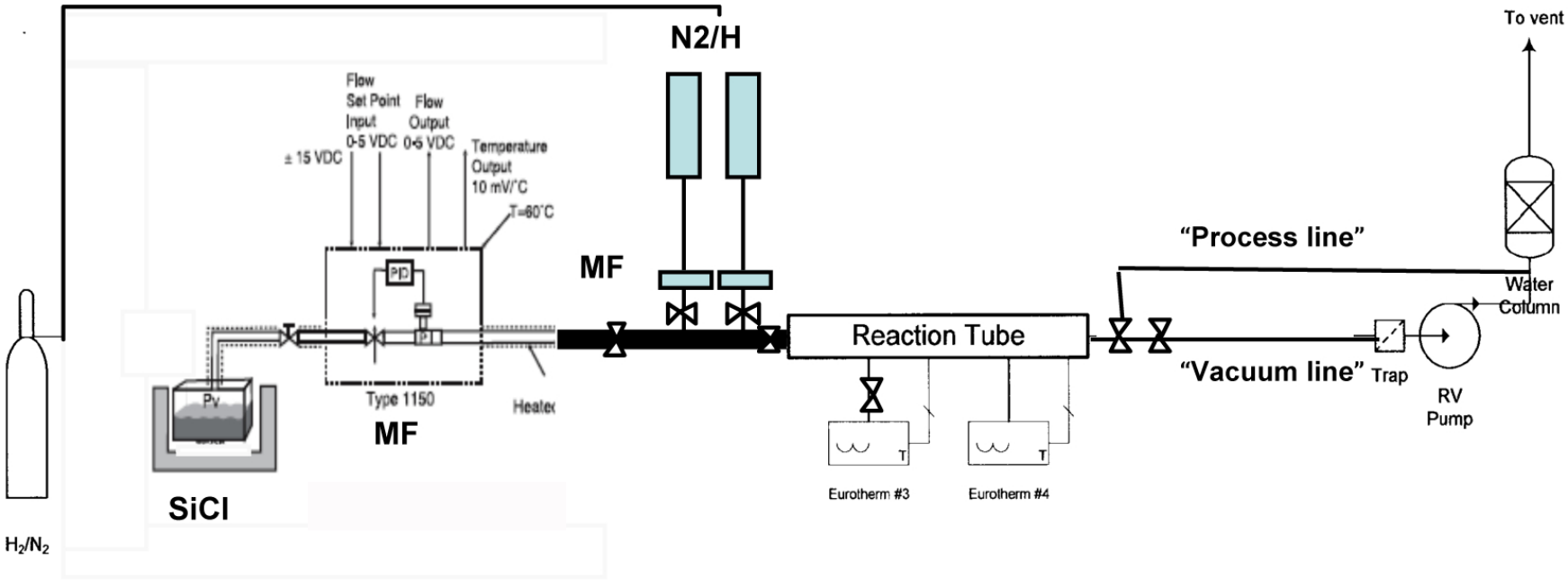


Figure A.1. Schematic of the $SiCl_4$ reactor

Appendix B

Secondary Ion Mass Spectrometry

Secondary Ion Mass Spectrometry Analysis

General Notes:

First and foremost, for any one interested in using secondary ion mass spectrometry (SIMS), I highly recommend reading Secondary Ion Mass Spectrometry by Wilson, Stevie and Magee.[37] It is an excellent introduction to SIMS, covering in detail the optimization of analysis conditions, sources of experimental error, and the quantification of data, as well as discussing number of specific applications. Additionally, it serves as a wonderful reference guide with an abundance of useful appendices.

Secondly, the Cameca NanoSIMS 50-L is a highly complex instrument, which can only be conquered through a detailed understanding of instrument operation and the patience of a zen master. Though I can not claim to fully posses either of these, Yunbin Guan who runs Caltech's Center for Microanalysis does. For a typical SIMS session, Yunbin would first optimize the primary and secondary ion beams for my samples. Optimization of the ion beams is the most challenging aspect of obtaining good data when working with the NanoSIMS. After the ion beams had been optimized, I would take over and start collecting data. However, I did learn a fair bit of ion beam optimization and instrument trouble shooting, both of which were required during data collection to maintain optimal analysis conditions. While some notes on these procedures can be found in my notebooks, Alex Gagnon has complied a detailed list of user instructions for working with the Cameca NanoSIMS 50-L, which can be found here: `http://caltechnanosims.pbworks.com/nanoSIMS50L-Instructions-Main`.

Sample Preparation: The Si-wire-coated Ge wafers and the Cu and B,P standards were mounted on Al disks B.1, which were then mounted into the NanoSIMS sample holder.

Figure B.1. Optical image of Si-wire-coated Ge wafers (6 perimeter samples) and of Cu and B,P standards (two center samples) mounted onto an Al disk.

Good sample preparation required two things. First and most importantly, the samples must be positioned level (± 250 μm) with each other and with the height of the NanoSIMS sample holder. The samples must be positioned level with each other because the secondary ion extraction efficiencies (and thus the RSFs) are sensitively dependent on the ion extraction distance (the distance between the sample and the secondary ion extraction optics, typically 300-400 μm) Variations in the sample height can be accounted for by adjusting the position of the NanoSIMS holder in the NanoSIMS, but to minimize the amount of secondary ion beam tuning between samples, it was best to keep variations in the sample height as small as possible. The samples must be positioned level with the height of the NanoSIMS sample holder as the NanoSIMS sample holder has a limited translation range of 800 μm.

To ensure that the wafers were level and flush with the surface of the SIMS sample

holder (not shown, but into which the Al disk was loaded), two different depths were milled into the Al disk. Two depths were necessary to accommodate the difference in wafer thickness between the Ge wafers and the Cu and B,P standards.

To ensure that the samples were as level with each other and with the surface of the NanoSIMS sample holder as possible, I measured the wafer thickness and the thickness of compressed carbon tape with calipers to determine the depth to which to mill the Al disk. As seen in B.1, two depths were necessary to accommodate the difference in wafer thickness between the Ge wafers and the Cu and B,P standards.

The second component of good sample preparation was the production of samples with minimal out-gassing, so that the the 10^{-10} Torr pressure range required for sample analysis could be reached. As a result, carbon tape could be used for sample mounting, while Ag paste could not.

Sample Analysis:

The following are a few brief notes on sample analysis:

1. Reducing the primary ion beam current will lead to improved spatial resolution (reduced beam diameter). However, reducing the primary ion beam current also reduces the sample sputtering rate and correspondingly the secondary ion count rates. Under our analysis conditions (where we were operating near the detection limit), one thus had to carefully consider the trade-off between improved spatial resolution and reduced secondary ion count rates. *In general, the best practice was to spend at lesat one day optimizing the primary and secondary ion beams before attempting to collect data.*

2. Our best analysis conditions allowed us to produce well-defined sputtered volumes, with a cross-sectional area quite close to the 1 μm $\times$ 1 μm rastered area, as seen in Figure B.2. It is estimated that under these conditions, a Cs^+ primary ion beam with a 14 pA beam current had a $\sim$200-300 nm beam diameter.

3. Wires for analysis were centered beneath the primary ion beam by using a light

pre-sputter to generate Si^- secondary ions which could then be visualized using the real-time-imaging software.

4. When trying to align single wires beneath the primary ion beam two challenges arose.

   (a) First, the NanoSIMS (which has down to 30 nm spatial resolution) has a sample stage that moves in 1 μm increments. Thus, centering a 2 μm diameter wire directly beneath the primary ion beam often required was not straightforward. In order to achieve stage translations < 1 μm, multiple 1 μm stage translations were made in quick succession to take advantage of motor hysteresis to produce stage translations of a fraction of a micron.

   (b) Secondly, centering the wire based upon the Si^- secondary ion image from the real-time-imaging (RTI) software, often led to slightly off-center profiling. Thus, it was often necessary to determine the offset of the RTI image and correct for this offset when aligning. (It was easy to tell during SIMS analysis whether the primary ion beam was centered on the wire by monitoring the Si and Ge counts during a run. If the wire was slightly off-center, the Ge counts would begin to rise and the Si counts would begin to fall in a gradual manner before the time necessary to sputter to the back surface of the wire had elapsed.

Measuring the Cu Concentration: Attempts were made to measure the Cu concentration in Cu-catalyzed Si microwires. However, even on the planar control standards the secondary ion count rates for Cu, P and B using the O^- primary ion beam were too low for quantitative analysis. This was surprising as the Si secondary ion count rates were sufficiently high that based upon the literature RSFs for Cu, P, and B in Si[37], we would have expected to have sufficiently high secondary ion

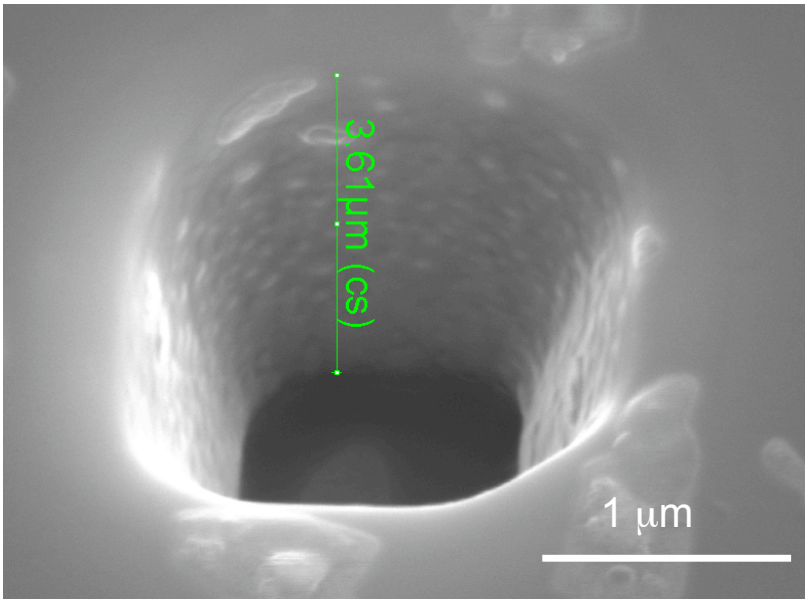


Figure B.2. Sputtered volume produced by an optimally focused Cs^+ primary ion beam with a 14 pA beam current, using a 1 μm × 1 μm rastered area

count rates. (The literature RSF's used an O_2^+ primary ion beam , but I have been told by Steve Smith at EAG Labs that the type of O primary ion beam should not drastically alter the RSFs.)

Data Analysis:

Relative Sensitivity Factor: The calculated RSFs are either the $^{197}Au^-$ in $^{28}Si^-$ RSF or the $^{197}Au^-$ in $^{30}Si^-$ RSF depending upon the Si ion species measured. To report the calculated RSFs in the same basis, we have chosen to report the $^{197}Au^-$ in Si RSF, which can be obtained by taking the calculated $^{197}Au^-$ in $^{28}Si^-$ RSF or the $^{197}Au^-$ in $^{30}Si^-$ RSF and dividing by the isotopic abundance of the Si isotope. The relative sensitivity factor (RSF) for $^{197}Au^-$ in Si was determined to be 1.8×10^{22} atoms cm^{-3} for the un-etched wires, 1.0×10^{22} atoms cm^{-3} and 0.75×10^{22} atoms cm^{-3} for the Au-etched wires, and 0.5×10^{22} atoms cm^{-3} for the KOH-etched, Au-etched wires (un-rastered analysis conditions, see below). The literature value of the RSF for Au in Si is reported to be 1.0×10^{22} atoms cm^{-3}.[37] Although the

difference in the RSFs for the un-etched and KOH-etched, Au-etched wires are large, they are within reason given that the ion extraction efficiency (and hence the RSF) can depend sensitively on the sample height in the Cameca NanoSIMS-50L, due to its very short extraction distance $\sim 0.4 \pm 0.05$ mm. Additionally, error is introduced into the calculation of the RSF through the measurement of the depth of the sputtered area. The error in this measurement was greatest for the un-etched wires and the KOH-etched, Au-etched wires, due to the more diffuse primary beam and un-rastered analysis conditions, respectively.

Analysis Conditions: Rastered Analysis Conditions: Using a 16 keV Cs^+ primary ion beam and a 1 μm^2 rastered area, a 10 pA beam current produced a sputter rate of 0.9 nm/s for the radially profiled, un-etched wires. A slightly larger beam current of 14 pA was used for the radially profiled, Au-etched wires and produced sputter rates of 2.7 nm/s. The three-fold increase in the sputter rate from the un-etched to the Au-etched radial analyses is a combination of the increased primary ion beam current and a reduction in the sputtered area. The reduction in the sputtered area was a result of the realization of a more optimum beam focus for the Au-etched analyses. For the Au-etched, axially profiled wires the sputter rate was 5 nm/s. The two-fold increase in the sputter rate from the radially profiled to the axially profiled, Au-etched wires may be related to the sputtering of the sidewall of the axially profiled wires, as shown in Figure 3.7c. Elimination of the sidewall of the wire would mean that atoms could be sputtered from the wire laterally, thereby increasing the sputtering rate.

Un-Rastered Analysis Conditions: For the KOH-etched wires (Fig. 3.6 and Fig. B.4c) the 16 keV Cs^+ primary ion beam was not rastered and the sputtered secondary ions were not electronically gated. A beam current of 2.9 pA was used, which resulted in a sample sputtering rate of 1.1 nm/s and a sputtered area of 0.5 μm^2. Finally, the ^{28}Si secondary ion was measured instead of the ^{30}Si secondary ion.

Exponential Decay: A simple model produces a decay in the Au concentration similar to the decay observed for the un-etched wires. The primary ion beam was more diffuse for the un-etched wires than for the Au-etched wires. This resulted in

a sputtered volume with more rounded edges than the sputtered volume shown in the paper. An approximation for this sputtered volume can be obtained by defining a sputtering region with a high sputtering rate, sputtering region 1 (SR1), and a sputtering region with a low sputtering rate, sputtering region 2 (SR2), as shown in Figure B.3a. By setting the exponential decay length for the ^{197}Au count rate equal to 60 nm for both SR1 and SR2 and choosing the sputtering rate and sputtering area of SR1 to be 10 times greater than the sputtering rate and sputtering area for SR2, a decay in the ^{197}Au count rate which is similar to that observed for the un-etched wires is calculated (Figure B.3b). The exponential decay length for SR2 appears greater than 60 nm because the ^{197}Au count rate is graphed against the depth of SR1. Note that the 60 nm exponential decay length used in this model is the average of the observed exponential decay lengths for the Au-etched wires.

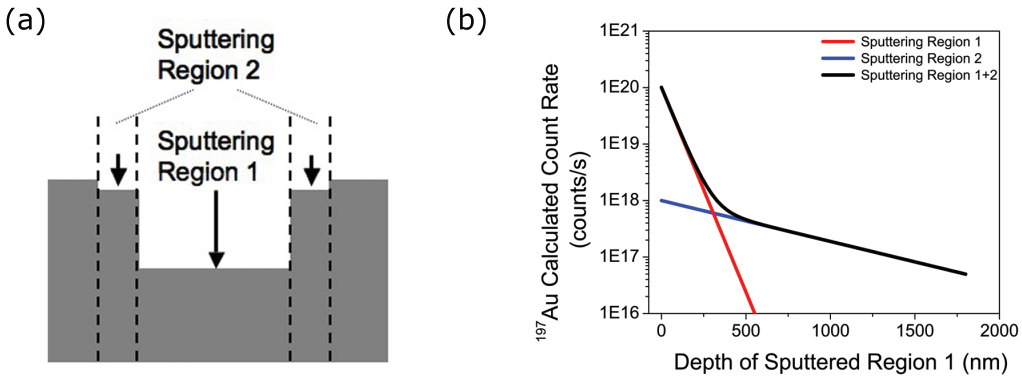


Figure B.3. (a) Cross-sectional sketch of the sputtered volume. (b) Au concentration versus depth for Sputtering Region 1, Sputtering Region 2, and the summation of Sputtering Regions 1 and 2.

Au-Etch: In our procedure, the wire arrays were exposed to Buffer HF Improved (Transene Inc.) for 30 s, rinsed in 18 MΩ cm resistivity deionized (DI) water, immersed in a 9:1 gold etchant TFA (an aqueous solution of I_2 and KI; Transene Inc.):HCl (37%, aq) mixture for 20 min, and rinsed in a 1 M HCl (aq) solution. Arrays were then washed in 18 MΩ cm resistivity DI water and dried in a stream of N_2.

KOH Etch: A KOH etch was performed after the Au-etch to remove Si from the surface of the wire. Arrays were placed in Buffered HF Improved (Transene Inc.) for 10 s to remove the native oxide and then dipped in a 50 wt.% KOH solution at 55°C for 2-3 s to etch the Si. Ellipsometry was done on a silicon(100) on insulator wafer to estimate that $\sim$ 20 nm of Si had been removed during the KOH etch. After etching, a few of the measured wires still exhibited an increased Au concentration near the surface of the wire. We attribute this to a lack of uniform etching across the array. It should be noted that the Au etch was performed for 45 min instead of 20 min (as for the Au-etched wires). However, the increased surface Au concentration was still present after the 45 min Au etch.

Secondary Ion Count Rates: Figure B.4 provides the secondary ion count rates as a function of depth for the Au-etched, radially and axially profiled wires and for the KOH-etched, radially profiled wires. A comparison between the Au-etched, radially and axially profiled wires, reveals the ^{30}Si count rate was almost an order of magnitude greater for the radially profiled wires. This difference in ^{30}Si count rates is suspected to result from a difference in sample height and a corresponding change in the ion extraction efficiency. As mentioned in the RSF section above, the RSF may be affected by a change in ion extraction efficiency. Thus the axial results, whose ^{30}Si count rate differed from the Au standards ^{30}Si count rate, should be understood to have a larger uncertainty than the radial results whose ^{30}Si count rate was quite similar to the Au standards ^{30}Si count rate.

When comparing Fig. B.4a and Fig. B.4c, note that Fig. B.4a reports a count rate for ^{30}Si secondary ions, while Fig. B.4c reports a count rate for ^{28}Si secondary ions. Because the ^{28}Si to ^{30}Si ratio is $\sim$ 30, similar count rates for ^{28}Si and ^{30}Si secondary ions represent a large difference in the amount of Si sampled. This explains why a 1 cps ^{197}Au count rate produces a Au concentration of $\sim 5 \times 10^{15}$ atoms cm^{-3} from the secondary ion count rates in Figure B.4a, and the same 1 cps ^{197}Au count rate produces a Au concentration of $\sim 1 \times 10^{17}$ atoms cm^{-3} from the secondary ion count rates in Figure B.4c.

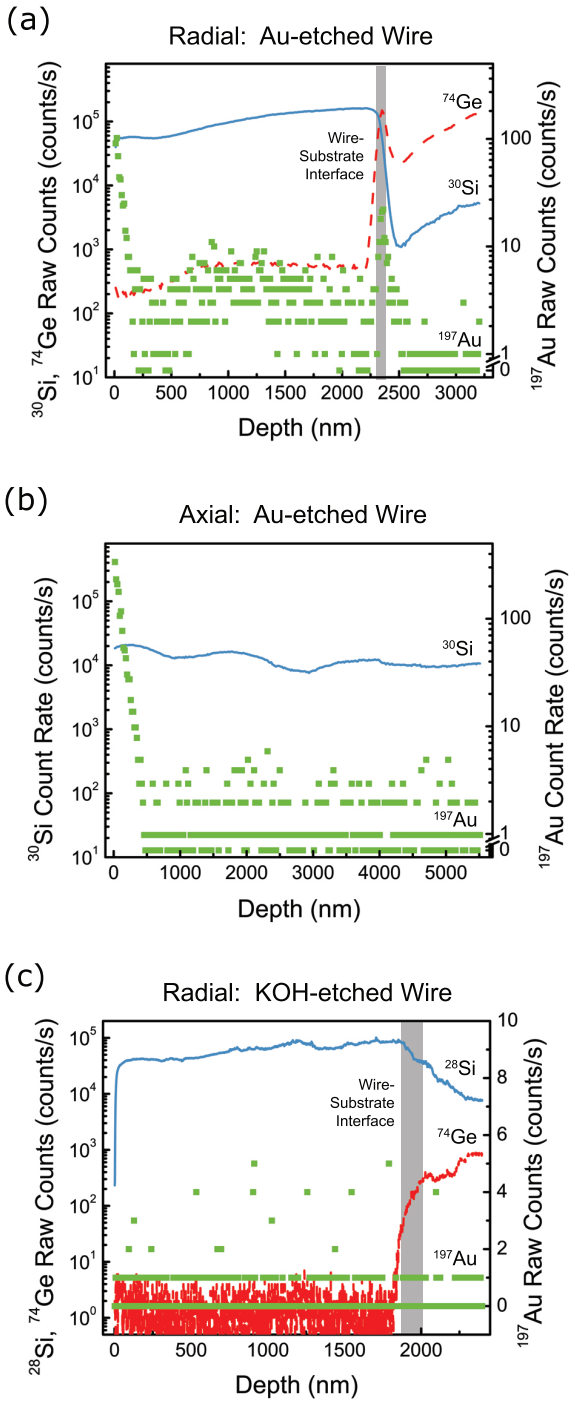


Figure B.4. Secondary ion count rates for (a) a radially profiled VLS-grown, Si wire, (b) an axially profiled VLS-grown, Si wire, and (c) a radially profiled, KOH-etched, Au-etched, VLS-grown, Si wire. In a and c, the vertical, grey band corresponds to the Si wire / Ge substrate interface. The ^{28}Si (^{30}Si) and ^{74}Ge count rates are referred to the left-hand y-axis, while the ^{197}Au count rate is referred to the right-hand y-axis.

Appendix C

Scanning Photocurrent Microscopy

Contact Deposition: The contact deposited first (the ohmic Al w/ 1% Si contact with the exception of one device) was ~ 1.5 μm thick such that wires would remain attached to the substrate during resist lift-off, while the contact deposited second (the rectifying MIS contact with the exception of one device) was ~ 0.3 μm thick to ensure conformal coverage of the wire surface.

LLI estimation:

Measured Photocurrent: The maximum measured photocurrent of the Si wire device is in good agreement with the measured photocurrent of the laser. The maximum photocurrent measured during a SPCM scan of a typical Si wire device was 2.9 nA. Accounting for the 0.60 external quantum yield of the photodiode at 650 nm (the laser wavelength), the measured photocurrent of the laser was 12 nA. Thus we find a maximum external quantum yield of 0.24, which is reasonable for our Si wire devices.

Variation of the Extracted Effective Minority-Carrier Diffusion Length: Examining the transverse photocurrent intensity in Fig. 5.3c, the photocurrent intensity is found to be larger along the wire sidewalls than in the wire center. This variation in the photocurrent intensity is thought to arise from greater optical incoupling of the laser illumination at the wire sidewall. Since the effective minority-carrier diffusion length, $L_{n,eff}$, is dependent upon the broad-area illumination intensity, the increased optical incoupling of the laser illumination may be producing the observed difference in the $L_{n,eff}$ extracted from photocurrent cross-sections between the wire center and the wire sidewall if a fraction of the laser illumination is incoupled into a

Table C.1. Calculation of the optical carrier generation density under laser illumination.

Laser (λ = 650 nm)	
Measured I_{sc} (A)	1.2×10^{-8}
Illuminated Area (cm^{-2})	7.9×10^{-9}
J_{sc} (A cm^{-2})	1.5×10^{0}
$I_o = J_{sc}/q$ (photons cm^{-2} s^{-1})	9.4×10^{18}
α (cm^{-1})	3.1×10^{3}
G_L= -dI/dz = $\alpha I_o e^{-\alpha z}$ (photons cm^{-3} s^{-1})	2.9×10^{22}
$L_{n,eff}$ (cm)	1.1×10^{-3}
D_n (cm^2 s^{-1})	1.9×10^{1}
Lifetime (s)	5.7×10^{-8}
n'=p'=G_L τ_{eff} (cm^{-3})	$\mathbf{1.7 \times 10^{15}}$
Wire Doping (cm^{-3})	$\mathbf{1 \times 10^{17}}$

guided wave mode within the Si wire. The existence of guided wave modes within the Si wires is known[50] and not unexpected given the similarity in structure between a Si wire in air and an optical fiber.

Table C.2. Calculation of the optical carrier generation density under broad-area illumination.

Broad-Area Illumination	
Measured I_{sc} (A)	8.7×10^{-5}
Illuminated Area (cm^{-2})	6.4×10^{-5}
J_{sc} (A cm^{-2})	1.4×10^{0}
$I_o = J_{sc}/q$ (photons cm^{-2} s^{-1})	8.6×10^{18}

Partitioning white light (T = 3200 K) into seven bins

λ (nm)	966	732	599	441	377	343	297
Fraction of Spectrum	0.595	0.298	0.088	0.016	0.0015	0.0015	0.0002
α (cm^{-1})	760	1.7×10^3	5.7×10^3	4.9×10^4	3.7×10^5	1.1×10^6	1.9×10^6

G_L= -dI/dz = $\alpha I_o e^{-\alpha z}$ (photons cm^{-3} s^{-1})	4.1×10^{22}
$L_{n,eff}$ (cm)	1.1×10^{-3}
D_n (cm^2 s^{-1})	1.9×10^{1}
Lifetime (s)	5.7×10^{-8}
n'=p'=G_L τ_{eff} (cm^{-3})	**2.3×10^{15}**
Wire Doping (cm^{-3})	**1×10^{17}**

Appendix D

Si Microwire-Array Solar Cells

Characterization: Dark and light current-voltage measurements were performed on a probe station with a 4-point source-measure unit (Keithley 238). Contact to the ITO top contact was made with a micromanipulator-controlled Au-coated tungsten probe tip. Simulated solar illumination was provided by a 1000 W Xe arc lamp with air mass (AM 1.5G) filters (Oriel), calibrated to 1-sun illumination by an NREL-traceable Si reference cell (PV Measurements, Inc.). Spectral response measurements were performed in an overfilled geometry using chopped (30 Hz) illumination from a 300 W Xe arc lamp coupled to a 0.25 m monochromator (Oriel) that provided ∼2 nm spectral resolution. The specimen photocurrent was normalized (by area) to that of a 3 mm-diameter calibrated photodiode, to determine the external quantum yield. The signals were measured with independent lock-in detection of the sample and calibration channels. Scanning photocurrent microscopy measurements were performed using a confocal microscope (WiTEC) in a light-beam-induced current (LBIC) configuration described previously.[44] Scanning photocurrent microscopy (SPCM) images were formed by rastering each device beneath a ∼1.0 μm-diameter laser spot (λ = 650 nm) while recording the short-circuit current (0 V bias) under otherwise dark conditions. Multiple 90 μm x 90 μm SPCM images were manually stitched together and post-processed to determine the active cell area using image processing software (Image J).

***V_{oc}* and *FF*:** Tables D.1, D.2 and D.3 provide the V_{oc} and *FF* for *all* of the fabricated As-Grown, Scatterer, and PRS solar cells. (These tables include the V_{oc} and *FF* for solar cells whose area was not measured by SPCM.) As seen in Table D.3 below, the V_{oc} and *FF* were remarkably consistent for the PRS solar cells. The V_{oc}

and FF were also consistent between the best Scatterer (Tbl. D.2) and As-Grown (Tbl. D.1) solar cells, however some cells with lower V_{oc} and FF were observed. For the As-Grown solar cells, obvious fabrication defects (cracking of the mounting wax prior to ITO deposition) may have resulted in the larger variation in cell performance. Between cells with similar performance (within each respective cell type), we attribute much of the variation in FF to the observed variations in the probe tip to ITO contact resistance.

Table D.1. As-Grown Cells (V_{oc} and FF)

Sample	$\boldsymbol{V_{oc}}$**(mV)**	$\boldsymbol{FF}$**(%)**
C4R2	401	59.3
C4R3	209	44.9
C4R4	452	61.4
C4R5	257	42.2
C4R6	478	59.1
C3R2	419	43.0
C3R3	339	52.0
C3R4	474	66.2
C3R5	453	65.8
C3R6	485	68.4
C2R3	482	69.4
C2R4	492	70.1
C2R5	484	71.6
C2R6	429	59.1
C1R6	463	54.4

Table D.2. Scatterer Cells (V_{oc} and FF)

Sample	$\boldsymbol{V_{oc}}$**(mV)**	$\boldsymbol{FF}$**(%)**
C1R1	477	61.7
C2R1	429	54.8
C3R1	387	53.5
C4R1	475	61.4
C1R2	498	67.5
C2R2	503	68.6
C3R2	481	54.3
C4R2	475	65.1
C1R3	497	64.9
C2R3	486	60.4
C3R3	505	68.8
C2R4	499	68.0

Table D.3. PRS Cells (V_{oc} and FF)

Sample	$\boldsymbol{V_{oc}}$**(mV)**	$\boldsymbol{FF}$**(%)**
C2R1	491	59.3
C3R1	487	61.2
C4R1	488	59.7
C5R1	485	61.9
C2R2	497	61.0
C3R2	493	60.8
C4R2	495	61.1
C5R2	489	60.0
C2R3	499	63.3
C3R3	497	63.0
C4R3	495	62.9
C5R3	493	61.5
C2R4	504	62.6
C3R4	494	64.5
C4R4	502	62.5
C5R4	501	61.5
C2R5	503	66.1
C3R5	500	67.2
C4R5	498	65.4
C5R5	497	62.6
C2R6	502	63.4
C3R6	499	63.3
C4R6	489	61.0
C5R6	485	64.3

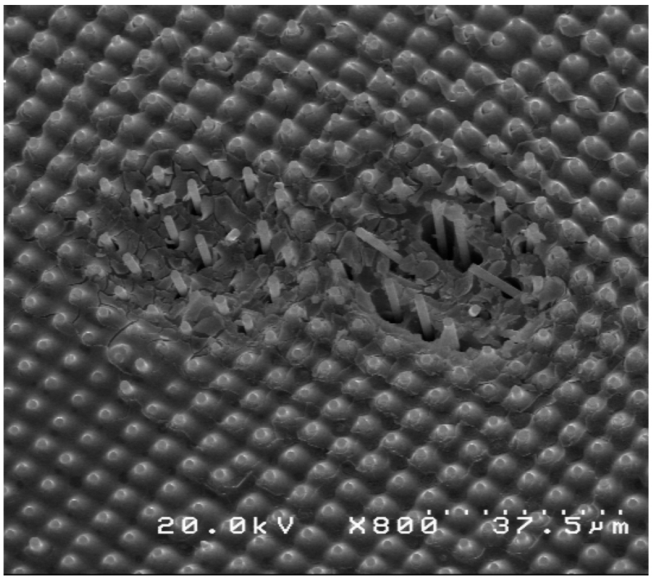
Transparent Dielectric: Ideally, a flexible, transparent, dielectric would have been used in the Si microwire-array solar cells fabricated in Ch. 6. Three such materials were considered for use: polydimethylsiloxane (PDMS); polyethylenevinylacetate (PEVA); and hot glue (a mixture of PEVA and wax). Though these materials were not successfully implemented in a wire-array solar cell, knowledge was gained towards the future fabrication of flexible wire-array solar cells.

Given our previous work with PDMS infilled Si microwire arrays[14] and their use as photoelectrochemical cells,[78] PDMS was the first dielectric infill we examined for use in a solid-state solar cell. One immediate difficulty with the choice of PDMS as an infill was the removal of excess PDMS from the top of the wire arrays (not necessary for the photoelectrochemical cell, as it was only partially infilled with PDMS). A dry-etch selective for PDMS over Si is not know to exist, and selective wet chemical etches proved difficult to control. However, as a result of the variation in the wire height across an array, regions with near optimal infill of PDMS could be obtained (not shown.)

An equally important challenge to the use of PDMS as a dielectric infill (and likely many flexible infills) was obtaining an electrical contact to the TCO once deposited on the PDMS. As can be seen in Figure D.1a, attempts to place an electrical probe onto the TCO resulted in compression of the PDMS layer beneath the TCO and fracture of the TCO. Consequently, it was not possible to obtain a good electrical contact to the TCO. A metal contact pad ($\sim 1\mu$m-thick) was evaporated on top of the TCO in an attempt to prevent the fracture of the TCO during the contacting process (not shown), but no improvement in the electrical contact was observed. The TCO also appears to have fractured in areas that had not been probed, as seen in Figure D.1b. It is not known whether this second type of fracturing prevented the TCO from functioning as a continuous contact layer.

Seeking to use a less mechanically elastic (but still flexible) polymer than PDMS and a polymer that could be etched without etching Si, we examined ethylenevinylacetate (EVA). EVA is already used in commercial solar cell production as a transparent encapsulant and exhibits no photo-degrading over the 25-year warranty of a commer-

(a)



(b)

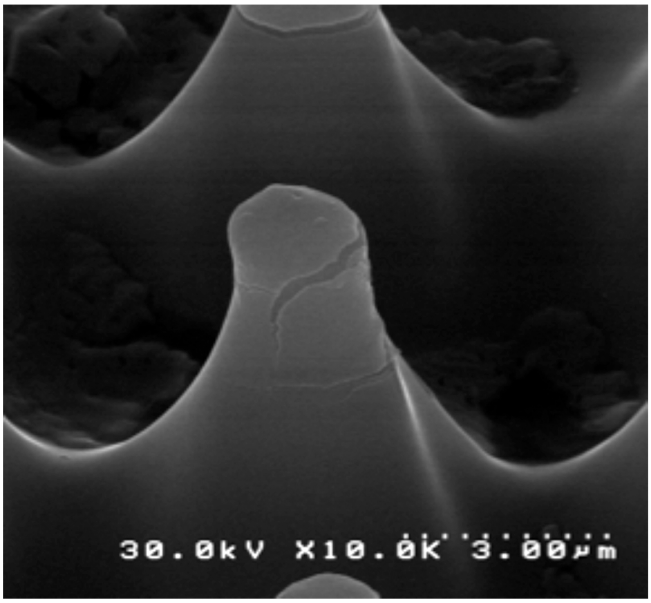


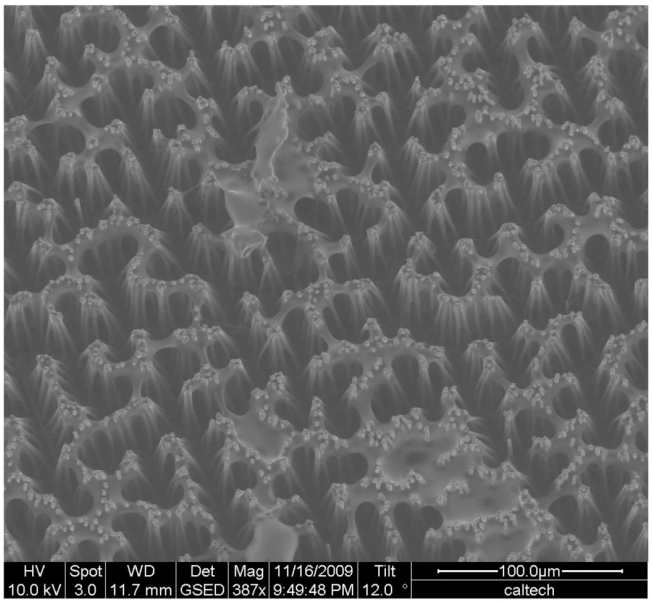
Figure D.1. SEM images of a wire array infilled with PDMS and coated with ITO. (a) Indentations in the PDMS and cracking of the ITO layer after attempts at establishing an electrical contact with a metallic probe tip. (b) High magnification SEM image of a wire tip exhibiting cracks in the ITO.

cial solar module. However unlike PDMS, EVA did not lend itself to the spin-coating deposition process. As seen in Figure D.2, surface tension led to the formation of regions filled to the wire tips with EVA and regions devoid of EVA. Increasing the concentration of EVA in the solvent (dicholoromethane) clearly led to a more uniformly infilled wire array, however the solution used in Figure D.2b was near the solubility limit.

Concurrent to my work with PDMS and PEVA, Dr. Michael Walter had shown that hot glue (a mixture of PEVA and wax) could be used to infill the wire arrays, as can be seen in Figure D.3. The hot glue yielded a less uniform infill than the mounting wax (Fig. D.3, Fig. 6.9), though in some areas the uniformity of the hot glue was comparable with uniformity of the mounting wax (not shown.)

Solar cells fabricated using hot glue as the transparent dielectric infill had a high V_{oc}, but exhibited a low FF and inconsistent J_{sc}, likely due to failure of the TCO layer under mechanical pressure from the electrical probe tip. However, the ability to make an electrical contact to TCO deposited on hot glue and the ability to peel-off wire arrays using hot glue, suggest that hot glue be strongly considered as the dielectric infill in flexible solar cells.

(a)



(b)

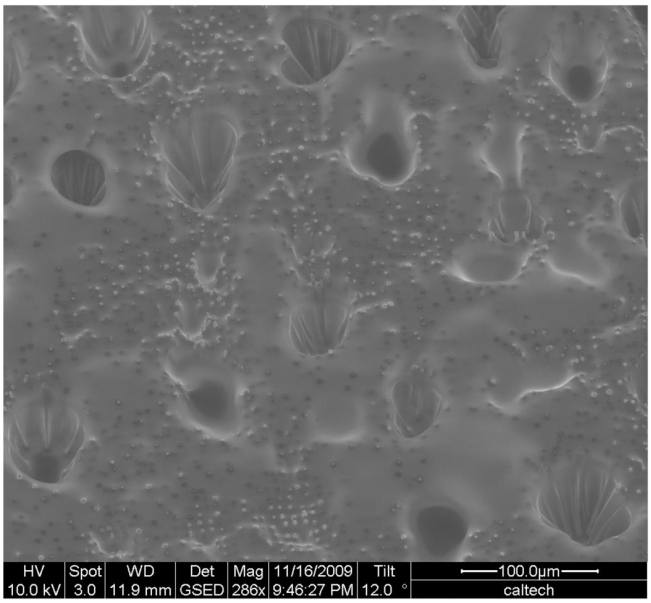


Figure D.2. SEM images of wire-arrays infilled with ethylenevinylacetate (EVA.) (a) 0.6 g 70% VA EVA dissolved in 4 mL dicholoromethane and spin-coated at 2000 rpm for 60s (b) 0.6 g 70% VA EVA dissolved in 2 mL dicholoromethane and spin-coated at 2000 rpm for 60s.

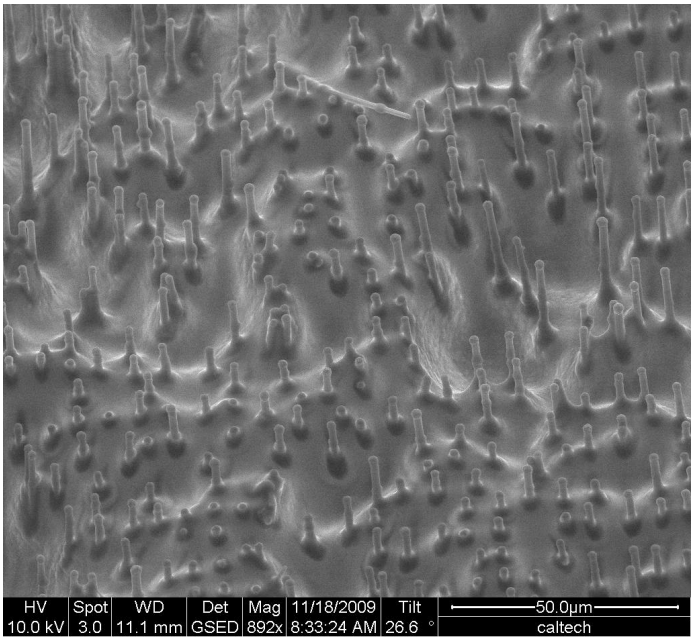


Figure D.3. SEM image of a wire array infilled with hot glue.

Bibliography

[1] NASA. Climate and earth's energy budget, 2010. 1

[2] N. S. Lewis. Powering the planet, 2006. 1

[3] US Department of Energy. Buildings energy data book, October, 2009 2009. 2

[4] US Energy Information Administration. Annual energy review 2008: Energy perspectives, 2010. 2

[5] National Renewable Energy Laboratories. 2008 solar technologies market report, 2010. 2

[6] Wikipedia. Feed-in tariff, 2010. 2

[7] SunPower. Solar photovoltaic electricity, 2010. 2

[8] R. M. Margoils. Photovoltaic technology experience curves and markets, 2003. 2

[9] Stephen O'Rourke. Pv status and pathways, 2009. 2, 4

[10] C. del Canizo, G. del Coso, and W. C. Sinke. Crystalline silicon solar module technology: Towards the 1 euro per watt-peak goal. *Progress in Photovoltaics*, 17(3):199–209, 2009. 4

[11] V. Shah. Discovering "second" thin film solar in a poly supply glut environment, 2009. 4

[12] USGS. Mineral commodity summaries, 2010. 4

[13] B. M. Kayes, H. A. Atwater, and N. S. Lewis. Comparison of the device physics principles of planar and radial p-n junction nanorod solar cells. *Journal of Applied Physics*, 97(11):114302–11, 2005. 4, 5, 6, 72, 101

[14] K. E. Plass, M. A. Filler, J. M. Spurgeon, B. M. Kayes, S. Maldonado, B. S. Brunschwig, H. A. Atwater, and N. S. Lewis. Flexible polymer-embedded si wire arrays. *Advanced Materials*, 21(3):325–328, 2009. 7, 25, 101, 110, 137

[15] M. D. Kelzenberg, S. W. Boettcher, J. A. Petykiewicz, D. B. Turner-Evans, M. C. Putnam, E. L. Warren, J. M. Spurgeon, R. M. Briggs, N. S. Lewis, and H. A. Atwater. Enhanced absorption and carrier collection in si wire arrays for photovoltaic applications. *Nature Materials*, 9:239–244, 2010. 7, 71, 80, 99, 112

[16] M. D. Kelzenberg, D. B. Turner-Evans, B. M. Kayes, M. A. Filler, M. C. Putnam, N. S. Lewis, and H. A. Atwater. Single-nanowire si solar cells. *33rd IEEE Photovoltaic Specialists Conference, Vols 1-4*, pages 144–149, 2008. 9, 42, 68, 69

[17] R. S. Wagner and W. C. Ellis. Vapor-liquid-solid mechanism of single crystal growth (new method growth catalysis from impurity whisker epitaxial + large crystals si e). *Applied Physics Letters*, 4(5):89, 1964. 10, 11

[18] R. S. Wagner and W. C. Ellis. Vapor-liquid-solid mechanism of crystal growth and its application to silicon. *Transactions of the Metallurgical Society of Aime*, 233(6):1053, 1965. 10, 11

[19] R. S. Wagner, W. C. Ellis, S. M. Arnold, and K. A. Jackson. Study of filamentary growth of silicon crystals from vapor. *Journal of Applied Physics*, 35(10):2993, 1964. 10

[20] R. S. Wagner. Defects in silicon crystals grown by vls technique. *Journal of Applied Physics*, 38(4):1554, 1967. 10

[21] J. Westwater, D. P. Gosain, S. Tomiya, S. Usui, and H. Ruda. Growth of silicon nanowires via gold/silane vapor-liquid-solid reaction. *Journal of Vacuum Science and Technology B*, 15(3):554–557, 1997. 10, 24

[22] L. J. Lauhon, M. S. Gudiksen, C. L. Wang, and C. M. Lieber. Epitaxial core-shell and core-multishell nanowire heterostructures. *Nature*, 420(6911):57–61, 2002. 10, 46

[23] F. M. Ross, J. Tersoff, and M. C. Reuter. Sawtooth faceting in silicon nanowires. *Physical Review Letters*, 95(14), 2005. 10

[24] J. M. Jasinski and S. M. Gates. Silicon chemical vapor-deposition one-step at a time - fundamental-studies of silicon hydride chemistry. *Accounts of Chemical Research*, 24(1):9–15, JAN 1991. ISSN 0001-4842. 12

[25] E. G. Bylander. Kinetics of silicon crystal growth from sicl4 decomposition. *Journal of the Electrochemical Society*, 109(12):1171–1175 ISI:A1962WG28200013, 1962. 12

[26] B. M. Kayes. *Radial pn Junction Wire Array Solar Cells*. PhD thesis, California Institute of Technology, 2009. 12, 42, 72

[27] B. M. Kayes, M. A. Filler, M. C. Putnam, M. D. Kelzenberg, N. S. Lewis, and H. A. Atwater. Growth of vertically aligned Si wire arrays over large areas (> 1 cm^2) with Au and Cu catalysts. *Applied Physics Letters*, 91(10):103110–3, 2007. 12, 18, 19, 22, 23, 28, 75, 101, 109

[28] A. I. Hochbaum, R. Fan, R. R. He, and P. D. Yang. Controlled growth of si nanowire arrays for device integration. *Nano Letters*, 5(3):457–460, 2005. 15, 19

[29] Y. Okajima, M. Amemiya, K. Kato, and S. Asai. VLS growth of silicon whiskers on a patterned silicon-on-insulator (soi) wafer. *Journal of Crystal Growth*, 165 (1-2):37–41, 1996. 19

[30] S. Kodambaka, J. B. Hannon, R. M. Tromp, and F. M. Ross. Control of si nanowire growth by oxygen. *Nano Letters*, 6(6):1292–1296, 2006. 24

[31] M. M. Lunden. *Sintering of Aerosol Agglomerates*. PhD thesis, California Institute of Technology, 1995. 24

[32] J. M. Spurgeon, K. E. Plass, B. M. Kayes, B. S. Brunschwig, H. A. Atwater, and N. S. Lewis. Repeated epitaxial growth and transfer of arrays of patterned, vertically aligned, crystalline si wires from a single si(111) substrate. *Applied Physics Letters*, 93(3), 2008. 25, 101

[33] D. E. Perea, J. L. Lensch, S. J. May, B. W. Wessels, and L. J. Lauhon. Composition analysis of single semiconductor nanowires using pulsed-laser atom probe tomography. *Applied Physics a-Materials Science and Processing*, 85(3):271–275, 2006. 28

[34] J. E. Allen, E. R. Hemesath, D. E. Perea, J. L. Lensch-Falk, Z.Y. Li, Feng Yin, M. H. Gass, Peng Wang, A. L. Bleloch, R.E. Palmer, and L. J. Lauhon. High-resolution detection of au catalyst atoms in si nanowires. *Nature Nanotechnology*, 3:168–173, 2008. 28, 40, 41, 66, 67, 68

[35] S.H Oh, K. Benthem, S.I. Molina, A. Y. Borisevich, W. Luo, P. Werner, N. D. Zakharov, D. Kumar, S. T. Pantelides, and S. J. Pennycook. Point defect configurations of supersaturated au atoms inside si nanowires. *Nano Letters*, 8(4): 1016–1019, 2008. 28, 40, 41

[36] J. H. Woodruff, J. B. Ratchford, I. A. Goldthorpe, P. C. McIntyre, and C. E. D. Chidsey. Vertically oriented germanium nanowires grown from gold colloids on silicon substrates and subsequent gold removal. *Nano Letters*, 7(6):1637–1642, 2007. 28

[37] R. G. Wilson, F. A. Stevie, and C. W. Magee. *Secondary Ion Mass Spectroscopy*. John Wiley and Sons, New York, 1989. 34, 119, 122, 123

[38] J. B. Hannon, S. Kodambaka, F. M. Ross, and R. M. Tromp. The influence of the surface migration of gold on the growth of silicon nanowires. *Nature*, 440 (7080):69–71, 2006. 40

[39] F. Dhalluin, P. J. Desre, M. I. den Hertog, J. L. Rouviere, P. Ferret, P. Gentile, and T. Baron. Critical condition for growth of silicon nanowires. *Journal of Ap-*

plied Physics, 102(9), NOV 1 2007. ISSN 0021-8979. doi: {10.1063/1.2811935}. 40

[40] M. I. Hertog, J. L. Rouviere, F. Dhalluin, P. J. Desre, P. Gentile, P. Ferret, F. Oehler, and T. Baron. Control of gold surface diffusion on si nanowires. *Nano Letters*, 8(5):1544–1550, 2008. 40

[41] J. Slezak, M. Ondrejcek, Z. Chvoj, V. Chab, H. Conrad, S. Heun, T. Schmidt, B. Ressel, and K. C. Prince. Surface diffusion of au on si(111): A microscopic study. *Physical Review B*, 61(23):16121–16128, 2000. 40

[42] W. M. Bullis. Properties of gold in silicon. *Solid-State Electronics*, 9(2):143–168, 1966. 40, 41

[43] Robert F. Pierret. *Advanced Semiconductor Fundamentals*, volume VI of *Modular Series on Solid State Devices*. Prentice Hall, Upper Saddle River, NJ, 2003. 41

[44] M. D. Kelzenberg, D. B. Turner-Evans, B. M. Kayes, M. A. Filler, M. C. Putnam, N. S. Lewis, and H. A. Atwater. Photovoltaic measurements in single-nanowire silicon solar cells. *Nano Letters*, 8(2):710–714, 2008. 41, 49, 57, 58, 61, 72, 133

[45] R. Sachdeva, A. A. Istratov, and E. R. Weber. Recombination activity of copper in silicon. *Applied Physics Letters*, 79(18):2937–2939, 2001. 41, 58, 67

[46] O. Hayden, M. T. Bjork, H. Schmid, H. Riel, U. Drechsler, S. F. Karg, E. Lortscher, and W. Riess. Fully depleted nanowire field-effect transistor in inversion mode. *Small*, 3(2):230–234, 2007. 46

[47] J. Y. Yu, S. W. Chung, and J. R. Heath. Silicon nanowires: Preparation, device fabrication, and transport properties. *Journal of Physical Chemistry B*, 104(50): 11864–11870, 2000. 46

[48] Sarah M. Eichfeld, Tsung-Ta Ho, Chad M. Eichfeld, Alexana Cranmer, Suzanne E. Mohney, Theresa S. Mayer, and Joan M. Redwing. Resistivity

measurements of intentionally and unintentionally template-grown doped silicon nanowire arrays. *Nanotechnology*, 18(31), AUG 8 2007. ISSN 0957-4484. doi: {10.1088/0957-4484/18/31/315201}. 46

[49] I. Kimukin, M. S. Islam, and R. S. Williams. Surface depletion thickness of p-doped silicon nanowires grown using metal-catalysed chemical vapour deposition. *Nanotechnology*, 17(11):S240–S245, 2006. 46

[50] S. M. Sze. *Physics of Semiconductor Devices*. Wiley-Interscience, New York, 1981. 52, 58, 59, 102, 130

[51] A. M. Lapides, M. C. Putnam, and H. A. Atwater. Electronic measurements of vapor-liquid-solid grown, Ni-catalyzed, Si wires. SURF report, California Institute of Technology, 2009. 54

[52] E. J. Charlson and J. C. Lien. Al p-silicon mos photovoltaic cell. *Journal of Applied Physics*, 46(9):3982–3987, 1975. 59

[53] Abraham Many, Yehuda Goldstein, and Norman B. Grover. *Semiconductor surfaces*. North-Holland Pub. Co. ; Interscience Publishers [distributor], Amsterdam New York, 1965. 64

[54] K. I. Seo, S. Sharma, A. A. Yasseri, D. R. Stewart, and T. I. Kamins. Surface charge density of unpassivated and passivated metal-catalyzed silicon nanowires. *Electrochemical and Solid State Letters*, 9(3):G69–G72, 2006. 66

[55] Dieter K. Schroder. *Semiconductor material and device characterization*. Wiley-Interscience, 3rd edition, 2006. 66

[56] T. Hanrath and B. A. Korgel. Influence of surface states on electron transport through intrinsic ge nanowires. *Journal of Physical Chemistry B*, 109(12):5518–5524, 2005. 66

[57] M. D. Kelzenberg, M. C. Putnam, D. B. Turner-Evans, N. S. Lewis, and H. A. Atwater. Predicted efficiency of si wire array solar cells, 2009. 66, 72, 101

[58] F. Daiminger, A. Schmidt, F. Faller, and Forchel A. Picosecond time-resolved investigations of carrier lifetime and carrier capture ingaas/gaas quantum dots. *Proceedings of the SPIE*, 2139, 1994. 67

[59] M. D. Kelzenberg, D. B. Turner-Evans, M. C. Putnam, S. W. Boettcher, R. M. Briggs, C. M. Baek, N. S. Lewis, and H. A. Atwater. Crystalline si microwires for high-efficiency thin-film photovoltaics, 2010. 68, 72, 97, 99, 100, 101, 102

[60] S. W. Boettcher, J. M. Spurgeon, M. C. Putnam, E. L. Warren, D. B. Turner-Evans, M. D. Kelzenberg, J. R. Maiolo, H. A. Atwater, and N. S. Lewis. Energy-conversion properties of vapor-liquid-solid-grown silicon wire-array photocathodes. *Science*, 327(5962):185–187, 2010. 69, 97

[61] J. R. Maiolo, B. M. Kayes, M. A. Filler, M. C. Putnam, M. D. Kelzenberg, H. A. Atwater, and N. S. Lewis. High aspect ratio silicon wire array photoelectrochemical cells. *Journal of the American Chemical Society*, 129(41):12346–12347, 2007. 72

[62] A. P. Goodey, S. M. Eichfeld, K. K. Lew, J. M. Redwing, and T. E. Mallouk. Silicon nanowire array photoelectrochemical cells. *Journal of the American Chemical Society*, 129(41):12344–12345, 2007. 72

[63] L. Tsakalakos, J. Balch, J. Fronheiser, B. A. Korevaar, O. Sulima, and J. Rand. Silicon nanowire solar cells. *Applied Physics Letters*, 91(23), 2007. 72

[64] B. Z. Tian, X. L. Zheng, T. J. Kempa, Y. Fang, N. F. Yu, G. H. Yu, J. L. Huang, and C. M. Lieber. Coaxial silicon nanowires as solar cells and nanoelectronic power sources. *Nature*, 449(7164):885–889, 2007. 72

[65] O. Gunawan and S. Guha. Characteristics of vapor-liquid-solid grown silicon nanowire solar cells. *Solar Energy Materials and Solar Cells*, 93(8):1388–1393, 2009. 72

[66] T. J. Kempa, B. Z. Tian, D. R. Kim, J. S. Hu, X. L. Zheng, and C. M. Lieber.

Single and tandem axial p-i-n nanowire photovoltaic devices. *Nano Letters*, 8 (10):3456–3460, 2008. 72

[67] K. Q. Peng, Y. Xu, Y. Wu, Y. J. Yan, S. T. Lee, and J. Zhu. Aligned single-crystalline si nanowire arrays for photovoltaic applications. *Small*, 1(11):1062–1067, 2005. 72

[68] E. C. Garnett and P. Yang. Light trapping in silicon nanowire solar cells. *Nano Letters*, 2010. 72

[69] T. Stelzner, M. Pietsch, G. Andra, F. Falk, E. Ose, and S. Christiansen. Silicon nanowire-based solar cells. *Nanotechnology*, 19(29), 2008. 72

[70] E. C. Garnett and P. D. Yang. Silicon nanowire radial p-n junction solar cells. *Journal of the American Chemical Society*, 130(29):9224–9225, 2008. 72

[71] C. Colombo, M. Heiss, M. Gratzel, and A. F. I. Morral. Gallium arsenide p-i-n radial structures for photovoltaic applications. *Applied Physics Letters*, 94(17), 2009. 72

[72] Y. J. Dong, B. Z. Tian, T. J. Kempa, and C. M. Lieber. Coaxial group iii-nitride nanowire photovoltaics. *Nano Letters*, 9(5):2183–2187, 2009. 72

[73] H. Goto, K. Nosaki, K. Tomioka, S. Hara, K. Hiruma, J. Motohisa, and T. Fukui. Growth of core-shell inp nanowires for photovoltaic application by selective-area metal organic vapor phase epitaxy. *Applied Physics Express*, 2(3), 2009. 72

[74] M. C. Putnam, M. A. Filler, B. M. Kayes, M. D. Kelzenberg, Y. B. Guan, N. S. Lewis, J. M. Eiler, and H. A. Atwater. Secondary ion mass spectrometry of vapor-liquid-solid grown, au-catalyzed, si wires. *Nano Letters*, 8(10):3109–3113, 2008. 72

[75] M. C. Putnam, D. B. Turner-Evans, M. D. Kelzenberg, S. W. Boettcher, N. S. Lewis, and H. A. Atwater. 10 μm minority-carrier diffusion lengths in si wires

synthesized by cu-catalyzed vapor-liquid-solid growth. *Applied Physics Letters*, 95(16):163116, 2009. 75

[76] B. Balakrisnan, S. Patil, and E. Smela. Patterning PDMS using a combination of wet and dry etching. *Journal of Micromechanics and Microengineering*, 19(4), 2009. 76, 110

[77] Alan L. Fahrenbruch and Richard H. Bube. *Fundamentals of Solar Cells*. Academic Press, 1983. 99, 100

[78] J. M. Spurgeon, S. W. Boettcher, M. D. Kelzenberg, B. S. Brunschwig, H. A. Atwater, and N. S. Lewis. Flexible, polymer-supported, si wire array photoelectrodes. *Advanced Materials*, 2010. 101, 137

[79] N. Li, T. Y. Tan, and U. Gosele. Transition region width of nanowire hetero- and pn-junctions grown using vapor-liquid-solid processes. *Applied Physics a-Materials Science and Processing*, 90(4):591–596, 2008. 103

[80] Gerold W. Neudeck. *The PN junction diode*. Modular series on solid state devices ;. Addison-Wesley, Reading, Mass., 2nd edition, 1989. 103

[81] Nathan S. Lewis and Daniel G. Nocera. Powering the planet: Chemical challenges in solar energy utilization. *Proceedings of the National Academy of Sciences of the United States of America*, 103(43):15729–15735, OCT 24 2006. ISSN 0027-8424. doi: {10.1073/pnas.0603395103}. 103

[82] A.C. Tamboli, M. Malhotra, D. B. Turner-Evans, M. D. Kelzenberg, and H. A. Atwater. Growth of conformal gap layers on si wire arrays for solar growth of conformal gap layers on si wire arrays for solar growth of conformal gap layers on si wire arrays for solar growth of conformal gap layers on si wire arrays for solar energy applications. 2010. 103

[83] Kimberly A. Dick, Suneel Kodambaka, Mark C. Reuter, Knut Deppert, Lars Samuelson, Werner Seifert, L. Reine Wallenberg, and Frances M. Ross. The

morphology of axial and branched nanowire heterostructures. *NANO LETTERS*, 7(6):1817–1822, JUN 2007. ISSN 1530-6984. doi: {10.1021/nl0705900}. 104