Silicon Integrated Optics: Fabrication and Characterization

Thesis by
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Abstract

For decades, the microelectronics industry has sought integration and miniaturization as canonized in Moore's Law, and has continued doubling transistor density about every two years. However, further miniaturization of circuit elements is creating a bandwidth problem as chip interconnect wires shrink as well. A potential solution is the creation of an on-chip optical network with low delays that would be impossible to achieve using metal buses. However, this technology requires integrating optics with silicon microelectronics. The lack of efficient silicon optical sources has stymied efforts of an all-Si optical platform. Instead, the integration of efficient emitter materials, such as III-V semiconductors, with Si photonic structures is a low-cost, CMOS-compatible alternative platform.

This thesis focuses on making and measuring on-chip photonic structures suitable for on-chip optical networking. The first part of the thesis assesses processing techniques of silicon and other semiconductor materials. Plasmas for etching and surface modification are described and used to make bonded, hybrid Si/III-V structures. Additionally, a novel masking method using gallium implantation into silicon for pattern definition is characterized. The second part of the thesis focuses on demonstrations of fabricated optical structures. A dense array of silicon devices is measured, consisting of fully-etched grating couplers, low-loss waveguides and ring resonators. Finally, recent progress in the Si/III-V hybrid system is discussed. Supermode control of devices is described, which uses changing Si waveguide width to control modal overlap with the gain material. Hybrid Si/III-V, Fabry-Perot evanescent lasers are demonstrated, utilizing a CMOS-compatible process suitable for integration on in electronics platforms. Future prospects and ultimate limits of Si devices and the hybrid Si/III-V system are also considered.

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Chapter 1

Introduction

Few materials are as integral to modern society as silicon. It is difficult to imagine microelectronics without the crystalline silicon wafer, or telecommunications without silicon dioxide optical fibers. While silicon is widely used in both industries, the driving forces in each have been very different. The microelectronics industry has sought integration and miniaturization as canonized in Moore's Law [1], and has continued doubling transistor density about every two years. The telecommunications industry has not had the same versatile platform of the silicon chip; instead, it has developed a variety of materials and technologies to achieve long-range, high-bandwidth data transmission. Today, both industries are facing problems to their further development that are a direct product of these development methodologies. In microelectronics, the further miniaturization of circuit elements is creating a bandwidth problem as chip interconnect wires are forced to shrink as well. The problem arises from the increased RC time constant for charging or discharging the line, which is quickly becoming a limiting factor in chip design.[1] For example, at the 1 μm technology node, the switching delay of a MOSFET was 20 times longer than the RC delay of the benchmark 1.0-mm-long Al interconnect (20 ps to 1 ps). However, by the 100 nm technology node, the situation has completely reversed; MOSFETs are 100 times *faster* than the same generation interconnects (2.5 ps to 250 ps) [3]. This problem will continue to get worse as interconnects are shrunk with each smaller technology node, and may eventually prevent further miniaturization due to excessive power dissipation [4]. In telecommunications, the lack of a unified optical platform has kept

[1] The RC time constant scales roughly as K^2, where K is the scaling factor (linear dimensions shrink by $\frac{1}{K}$). For a full discussion of this scaling, see the chapter by Gaburro[2]

cost per component high and limited growth. These seemingly disparate problems can be addressed by integrating optics with silicon microelectronics. A silicon photonic chip would solve the interconnect bandwidth problem by using optical buses with low delays that would be impossible to achieve using metal buses. Likewise, the same technology used for these buses enables an integrated optical transceiver, extending the same economies of scale to formerly expensive multi-component systems [5].

1.1 Scope of this thesis

Before discussing experimental results in detail, it is important to understand one of the key processing tools used to fabricate these devices: the inductively coupled plasma reactive ion etcher (ICP-RIE). Plasma processing techniques are integral to modern semiconductor fabrication because of their high radical density, high selectivity, and anisotropic etch profiles at low temperatures and mild voltages. This gentle processing environment prevents unwanted diffusion and degradation of materials due to heat and lattice damage from ion bombardment. Plasma treatments have a minimal effect on existing wafer structure, which is a key requirement for large scale integration schemes such as CMOS, such as those discussed in Chapter 5. In this chapter, we will cover the applications of plasmas to etching and bonding materials appropriate for photonic integration, which rely on ICP-RIE capabilities.

Chapter 2 describes plasma applications of etching and surface modification to semiconductor materials, with special attention to processing techniques suitible for low-loss photonic structures and wafer bonding.

Chapter 3 examines a novel masking method using gallium implantation into silicon for pattern definition, characterizing the processing and discussing possible applications of the technique.

Chapter 4 describes compact silicon devices fabricated on 220nm/2um SOI, analyzing a fully-etched grating coupler for interfacing with optical fiber, low-loss waveguides and ring resonators. Characterization of the grating coupler and cavity quality factor (Q) are determined using an automated test system.

Chapter 5 discusses recent progress in the Si/III-V hybrid system, which was performed with members of the Atwater and Yariv groups. Supermode control of devices is described, which uses changing Si waveguide width to control modal overlap with the gain material. Hybrid Si/III-V, Fabry-Perot evanescent lasers are demonstrated, utilizing InGaAsP gain material. Finally, promising results of the supermode lasers over evanscent lasers are presented.

1.2 Silicon Photonics

Before we discuss fabrication techniques for making optical structures, we will introduce the basic concepts and some useful relationships used later in the thesis. More comprehensive treatments are found in several books and theses on the subject [6, 7, 8].

1.2.1 Simulation of Electromagnetic Modes

While many semianalytic methods [9, 10, 11] exist for determining the distribution of electromagnetic energy in dielectric structures, numerical methods for determining the fields are frequently needed to account for the complexity of realistic waveguide designs. To that end, recasting Maxwell's equations in a form amenable to numerical simulation is possible. We start with Maxwell's equations in the absence of free charge or currents:

$$\nabla \cdot \mathbf{D} = 0 \tag{1.1}$$

$$\nabla \cdot \mathbf{B} = 0 \tag{1.2}$$

$$\nabla \times \mathbf{E} = -\frac{\partial \mathbf{B}}{\partial t} \tag{1.3}$$

$$\nabla \times \mathbf{H} = \frac{\partial \mathbf{D}}{\partial t}, \tag{1.4}$$

with constitutive relations $\mathbf{D} = \epsilon\mathbf{E}$ and $\mathbf{B} = \mu_0\mathbf{H}$. Combining the constitutive relations with equations 1.3 and 1.4 yields:

$$\nabla \times \mathbf{E} + \mu\frac{\partial \mathbf{H}}{\partial t} = 0 \tag{1.5}$$

$$\nabla \times \mathbf{H} - \epsilon\frac{\partial \mathbf{E}}{\partial t} = 0. \tag{1.6}$$

Now, if we separate the time and express the fields in the time-harmonic basis

$$\mathbf{E}(\mathbf{r}, t) = \mathbf{E}(\mathbf{r})e^{i\omega t} \tag{1.7}$$

$$\mathbf{H}(\mathbf{r}, t) = \mathbf{H}(\mathbf{r})e^{i\omega t}, \tag{1.8}$$

we can rewrite equations 1.5 and 1.6 as an eigenvalue problem for $\mathbf{E}(\mathbf{r})$ or $\mathbf{H}(\mathbf{r})$:

$$\nabla \times \left(\frac{1}{\mu}\nabla \times \mathbf{E}(\mathbf{r})\right) = \omega^2\epsilon\mathbf{E}(\mathbf{r}) \tag{1.9}$$

$$\nabla \times \left(\frac{1}{\epsilon}\nabla \times \mathbf{H}(\mathbf{r})\right) = \omega^2\mu\mathbf{H}(\mathbf{r}). \tag{1.10}$$

These forms of Maxwell's equations are frequently used in the finite element method (FEM) [12]. An example of an FEM simulation is shown in figure 1.1, which shows the waveguide structure discussed in Chapter 4. Simulation of these structures allows us to quickly determine salient characteristics of the given dielectric structure, and ensures that we do not approximate away any important details of the structure.

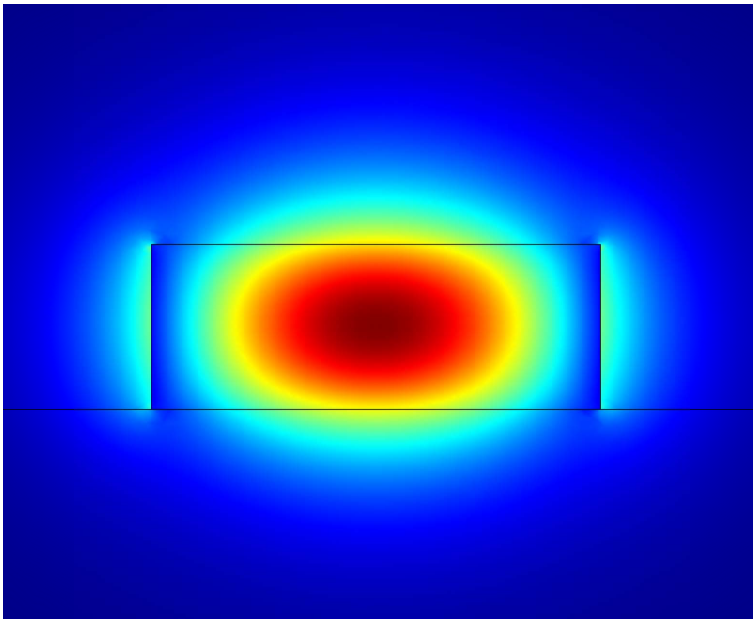


Figure 1.1. Plot of the electric field intensity profile $|E_x|^2$ of a 220 nm $\times$ 500 nm Si waveguide on SiO_2, showing the fundamental TE mode, calculated by FEM simulation in COMSOL

1.2.2 Photonic Structure Characteristics

A frequently quoted figure of merit is the quality factor, Q, which is defined by [6]:

$$\begin{aligned} Q &\equiv 2\pi \frac{\text{stored energy}}{\text{energy loss per cycle}} \\ &= 2\pi \left(\frac{\text{cycles}}{\text{second}}\right) \cdot \frac{\text{stored energy}}{\text{energy loss per second}} \\ &= \omega \frac{U_{stored}}{P_{loss}} \qquad (1.11) \\ &= \frac{\nu}{\delta\nu} \qquad (1.12) \end{aligned}$$

Equation 1.11 is useful when running simulations of electromagnetic modes, where U_{stored} and P_{loss} can be calculated directly. In an experimental context, equation 1.12 is more useful since both terms can be determined directly from a transmission measurement. Frequently, measurements are taken with respect to wavelength rather than frequency; using $c = \nu\lambda$, we can rewrite $\Delta\nu$ as

$$\delta\nu = \frac{c}{\lambda_1} - \frac{c}{\lambda_2} \approx \frac{c\delta\lambda}{\lambda^2}, \lambda \equiv \frac{\lambda_1 + \lambda_2}{2} \tag{1.13}$$

and thus equation 1.12 becomes

$$\begin{aligned} Q &= \frac{\nu}{\delta\nu} \\ &\approx \frac{c}{\lambda} \cdot \frac{\lambda^2}{c\delta\lambda} \\ &= \frac{\lambda}{\delta\lambda}. \end{aligned} \tag{1.14}$$

This approximation holds for $Q \gg 1$.

Finally, in Chapter 5, we will look at maximizing the gain in a hybrid system. In order to do this, it is important to maximize the confinement factor, Γ, in the gain region. This is the fraction of the mode that exists in the gain material, and can be calculated with the FEM using

$$\Gamma = \frac{\int_{dV} n^2(\mathbf{r}) \left|\mathbf{E}(\mathbf{r})\right|^2 dV}{\int_V n^2(\mathbf{r}) \left|\mathbf{E}(\mathbf{r})\right|^2 dV} \tag{1.15}$$

where dV is taken over the gain region. This can be used to understand trends in other laser performance characteristics like the threshold voltage and current.

Chapter 2

Plasma Etching and Wafer Bonding Techniques

2.1 Introduction

Before discussing experimental results in detail, it is important to understand one of the key processing tools used to fabricate these devices: the inductively coupled plasma reactive ion etcher (ICP-RIE). Plasma processing techniques are integral to modern semiconductor fabrication because of their high radical density, high selectivity, and anisotropic etch profiles at low temperatures and mild voltages. This gentle processing environment prevents unwanted diffusion and degradation of materials due to heat and lattice damage from ion bombardment. Plasma treatments have a minimal effect on existing wafer structure, which is a key requirement for large scale integration schemes such as CMOS, such as those discussed in Chapter 5. In this chapter, we will cover the applications of plasmas to etching and bonding materials appropriate for photonic integration, which rely on ICP-RIE capabilities. [1]

2.2 Plasmas in Electronics Processing

Plasmas are found in a wide range of industrial applications, including ashing, sputtering, etching, and chemical vapor deposition. However, the types of plasmas used in each process vary greatly. In this section, we will describe the important parame-

[1] Portions of this chapter are adapted from a publication with M. David Henry and Xiankai Sun [13].

ters of plasmas for understanding ICP-RIE etching and deposition, and establish how they relate to our desired processing results.

2.2.1 Figures of Merit

Central to semiconductor processing is the high fidelity transfer of a pattern onto a substrate through addition, modification, or removal of material. In order to quantify the ability to accomplish this selective processing, it is useful to have a few figures of merit to describe the process, namely:

- *Etch rate* - controllable and robust to small deviation in processing conditions. Depending on the application, one may want a higher etch rate for increased throughput or a lower etch rate for precision.
- *Uniformity* - both at each feature and across the wafer
- *Selectivity* - the ability to etch only the desired material, relative to the etching of mask and other substrate materials
- *Anisotropy* - The verticality of the etch profile. Also, the nanostructure of this vertical surface is important in many applications, particularly waveguides.
- *Damage* - Any surface or substrate damage acquired from the processing technique.

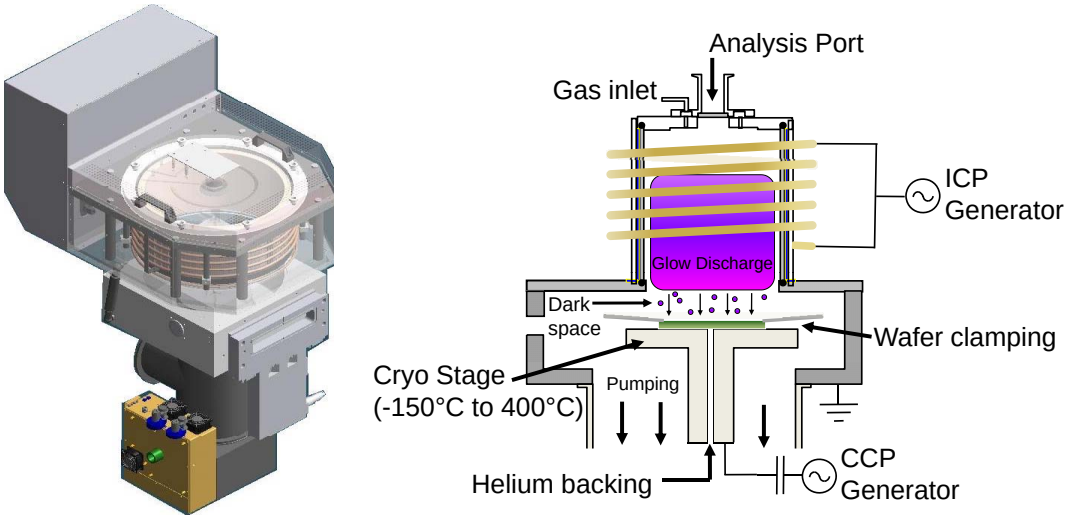
In addition, the environment in which the process occurs is important. Some conditions will have a deleterious effect on existing wafer structure. Chief among these is the temperature of processing. Heating (and cooling) can cause many problems, including thin film delamination due to thermal expansion coefficient mismatch, unwanted dopant diffusion, and other negative effects [14]. In the CMOS industry, the wafers tolerance to temperature fluctuations is often captured as a thermal budget [15], which means that minimizing use during one process step can give more latitude in other steps.

2.2.2 Plasma Characteristics

Plasma is a partially ionized gas with a combination of free electrons, ions, radicals, and neutral species. To create and sustain a plasma in the laboratory, it requires some energy input. Different coupling methods generate plasmas of different characteristics. Most useful to RIE are those generated by glow discharge plasmas (GDP), capacitive coupled plasma (CCP), inductively coupled plasma (ICP), or some combination thereof.

In a GDP process, electromagnetic energy is delivered as a voltage applied between two conducting plates, known as the cathode and the anode. The applied voltage is usually DC or in the low frequency regime, such that the characteristic time of field variation is longer than the response time of the system. The voltage generates an electric field across the gases in the chamber. Plasma initiation occurs when a small initial population of charged species is accelerated through the electric field and collides with other molecules, causing them to ionize. A relatively high voltage is required to initiate and sustain the plasma, which is a severe processing drawback. High voltage will cause the resultant energy of incident ions on the cathode to be high, favoring rough, physical processes (sputtering) over smooth, chemical processes (surface reactions). This will lower the selectivity to masking materials and cause sidewall roughening due to mask erosion. For these reasons, GDP sources are often used to sputter materials rather than etch anisotropically [16].

In a CCP process, energy is again supplied as a voltage across an anode and a cathode plate, but in a time-varying fashion. An RF voltage is applied to the plates at a frequency of 13.56 MHz. In this time-varying field, electrons in the plasma tend to oscillate, traveling between the anode and the cathode plates. Collisions of rapidly moving electrons with the slowly moving ions cause further ionizations. However, massive ions are less mobile and cannot track the rapidly oscillating electric field changes. By placing a capacitor between the anode plate and the RF supply, negative charge accumulates on the plate (typically referred to as the table). The resulting potential difference between the plasma and the negatively charged plate is



(a) Isometric (b) Cross-sectional

Figure 2.1. Views of an Oxford Instruments ICP-RIE.

called the self-bias V_b. The electric field due to V_b drives the positive ions in plasma towards the negatively charged table. This is the basis for traditional reactive ion etching (RIE).

In an ICP process, the excitation is again a time-varying RF source, but is delivered inductively, instead of capacitively, resulting in a changing magnetic field. This changing magnetic field, through the Maxwell-Faraday equation, induces an electric field that tends to circulate the plasma in the plane parallel to the CCP plates. Similarly to a CCP, collisions of the rapidly moving electrons with the slowly moving ions cause further ionizations. Loss of electrons from the plasma through the grounded chamber walls tends to create a static voltage, deemed the plasma voltage V_{plasma}. This is distinct from the self bias V_b, as will be examined later. Inductive coupling is generally realized through a large 4 to 5 turn coil encircling the plasma chamber. In the typical geometry, this means that one is able to change ion density and other plasma parameters without significantly perturbing the incident energy of the ions.

The results discussed in this chapter are realized on Oxford Systems Plasma Lab 100 ICP-RIE 380 systems, which utilize a CCP and an ICP power source, as seen in Figure 2.1. This dual plasma powering affords the greatest flexibility in altering plasma characteristics such as ion density and bias voltage independently of each

other. These systems have been extensively studied, particularly for silicon etching [17].

2.2.3 Processing Parameters

There are a few important features of an ICP-RIE plasma that have an effect on etching. Most noticeable during operation is the region of glow discharge, where visible light emission occurs from a cloud of energetic ions and electrons. The emission is caused by inelastic collisions of gas particles, exciting bound electrons into an excited state which results in a photon. The color of the plasma is characteristic of the excited gas species, because the photon energy is a function of the electronic structure of the gas molecules and their interactions with surrounding molecules [18]. This can be a good diagnostic for incorrect plasma striking conditions or other adverse changes in your plasma. For example, in a multiple gas recipe, sometimes the emission looks like only one of your gas species, instead of the average of the colors. This happens when the other species are not being ionized, and thus will cause the process to take on a completely different character from a calibrated recipe.

Beneath the glow discharge region is a dark space, where the depletion of electrons means that atoms are no longer excited into emitting photons. This dark space is also the part of the plasma that most directly affects the paths of incoming ions that will accomplish the etching. Neutral atoms and other ions will tend to scatter the otherwise straight path of the ions from the edge of the glow discharge to the cathode.

The spread in the ion energy and trajectory is characterized by ion angular distribution function (IADF) and the ion energy distribution function (IEDF) [17]. These distributions, depicted in Figure 2.2, describe the likelihood that an incident ion has a particular energy and trajectory. IADF strongly affects the sidewall profile, as a wider IADF corresponds to a higher flux of ions reaching the sidewall. Similarly, the IEDF controls the types of processes in which the ions can be engaged when they reach the surface; removal of passivating species, overcoming activation energies for reactions to occur, and sputtering yield are all consequences of the IEDF. These are all central to making an etch with desired performance characteristics, so understand-

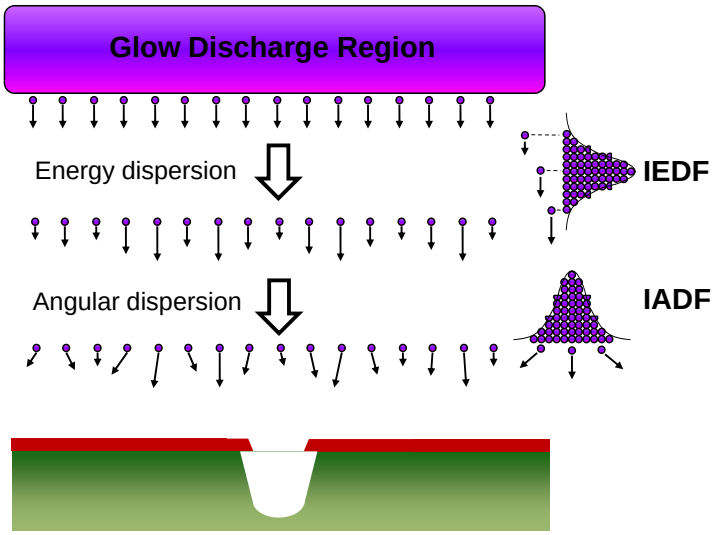


Figure 2.2. The action of the ion angular and ion energy distribution functions is to spread the kinetic energy and angle of incidence of etch species, resulting in etched profile distortion. Changes of each distribution function shown separately for clarity.

ing these effects and recognizing limitation due to them are paramount to optimizing a recipe. Parameters controlling the IADF and IEDF include the bias voltage V_b , the ion density, gas composition, and the mean free path (which also depends on the aforementioned parameters).

2.2.4 Etch Reaction Dynamics

In wet chemical processes, etching is accomplished through physical dissolution or reaction specific dissolution [19]. This takes place at any exposed surface and thus results in isotropic etching, although the etch rate can vary along different crystalline orientations due to the bonding state variation of the surfaces. A good example of crystalline anisotropy in Si wet processing is potassium hydroxide (KOH) etching, which is widely used for making MEMS structures that capitalize on the direction-dependent etch rate of KOH [20]. However, in a myriad of planar processes that are utilized in the semiconductor industry, an anisotropic etching profile with sidewalls perpendicular to the wafer surface is frequently required for effective pattern transfer.

In order to prevent the isotropic or crystalline anisotropic behavior of our processing gases, the sidewalls must be protected from further etching. This is accomplished by forming a passivating or inhibiting layer on the sidewall, in one of the following ways:

- Surface passivation
  - inserting gases in the plasma which react with wafer materials and form involatile compounds [21]
  - freezing volatile reaction products at the structures walls using, e.g., cryogenic wafer cooling [22]
- Inhibitor deposition
  - using polymer precursor gases to form physical barrier layers (e.g., C_4F_8) [23]
  - eroding and redepositing inert mask materials

All of these processes are important to consider when evaluating an etch, as there may be problems with the etch profile related to the deleterious effect of one of these regimes. We use both surface passivation and inhibitor deposition techniques in the following etch descriptions.

2.2.5 Time-Dependent Processes

In addition to the previously discussed processing parameters, one additional variable is at our disposal: time. A notable example of using time as an etching parameter is the Bosch silicon etch process, which occurs in a time-multiplexed manner, or *pulsed mode*, using an etching plasma followed immediately by a deposition plasma. Alternatively, a plasma that contains properly balanced etching and deposition gases can yield the desired etch profile. This is called a *mixed mode* process. Finally, the process conditions can be changed continuously over time in response to the changing surface condition of our wafer, or to compensate for a negative effect due to the initial conditions of the wafer.

2.2.6 Summary

When making and refining an etching recipe, it is important to have an understanding of all of the aforementioned plasma variables. The diversity of processing conditions accounts for both the sensitivity and flexibility of ICP-RIE plasmas. By having basic knowledge of the underlying physical processes, diagnosing problems in a particular etch recipe becomes more intuitive and makes refinement much easier. In the following sections, we will refer to many of the concepts covered here to explain results and understand the rationale for a given recipe.

2.3 Deep Silicon Etching

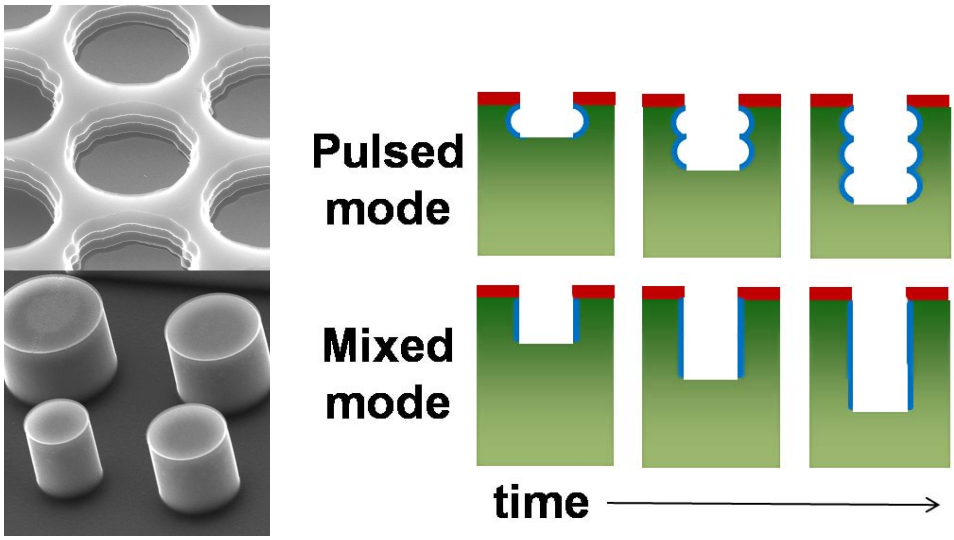
Before examining some of the more exotic etching recipes, it is best to examine two of the canonical silicon etching recipes frequently used in industrial settings: the Bosch process [24] and the cryogenic silicon etch [25]. The Bosch process[2] is a pulsed mode etch which uses gas chopping to alternatively etch silicon and deposit inhibitor to protect feature sidewalls. Inherent in the discreteness of the etching is notching on the sidewalls that occurs every step. The duty cycle between steps controls the etch angle and the total length of the combined steps controls the depth of the notching. In contrast, the cryogenic silicon etch[3] is a mixed mode etch that uses a different gas chemistry and chamber conditions to form passivating compounds at the sidewalls at the same time as etching, in effect combining the etch and passivation steps into a single step. By using cryogenic temperatures from $-80°C$ to $-140°C$, improvements in etch mask selectivity and passivation effects are enabled. These two processes are illustrated diagrammatically in Figure 2.3.

2.3.1 Gas Chemistries

The Bosch process utilizes sulfur hexafluoride (SF_6) as the etching gas and octafluorocyclobutane (C_4F_8) as the passivation gas. When the SF_6 is injected into the

[2]Recipe is found in the appendix, A.2.1

[3]Recipe is found in the appendix, A.2.3



(a) Example etches (b) Characteristic cross-sections of pulsed and mixed mode etches

Figure 2.3. Comparison of the Bosch process to cryogenic silicon etching.

chamber, the plasma ionizes and radicalizes the gas molecules to create a mixture of SF_x and F_y ions and neutrals, where x and y range from 0 to 6 and 1 to 2, respectively [26]. The potential established between the plasma and the substrate, due in part to the ICP and the CCP power, causes the electric field that drives the ions down to the substrate. The unmasked silicon then bonds to the fluorine atoms to create the volatile tetrafluorosilane (SiF_4) etch product which is then pumped away from the chamber. This is the predominant etching mechanism, and results in an isotropic etch profile. After a few seconds of etch time, the SF_6 flow is rapidly terminated and the C_4F_8 gas is then injected into the chamber for the passivation step. During this step, the C_4F_8 fragments into smaller CF_x ions which act as fluorocarbon film precursors [27]. This chemically-resistant film forms on both the vertical and horizontal surfaces of the wafer. The thickness of the protective layer is controlled by the length of the passivation step. Once the deposition is complete the subsequent etch step begins. No silicon etching occurs initially because of the previously deposited layer. However, the fluorocarbon film is milled due to ion bombardment. The bias voltage causes the ions to preferentially remove film from horizontal surfaces (cf. 2.2);

once the film is removed, isotropic etching continues on the exposed silicon surface. The discrete nature of these steps results in the scalloping characteristic of the Bosch process.

The cryogenic silicon etch also utilizes the SF_6 chemistry similar to that of the chopping Bosch. However, by lowering the substrate temperature, and by simultaneously injecting SF_6 and oxygen gas, O_2, a passivation layer is created simultaneously as the silicon is etched. The current understanding of the chemical process is that oxygen ions combine with the fluorine bonded to the silicon surface prior to the silicons removal and forms a SiO_xF_y layer. The exact composition of this layer is a topic of current research [28]. In a manner similar to the chopping Bosch passivation, the SiO_xF_y passivation layer protects the exposed vertical silicon while the unmasked horizontal silicon is etched way. To make this passivation process as energetically favorable as the chemical reaction of making SiF_4, the substrate temperature is required to be cooler than approximately $-80°C$. When the silicon is warmed back up to room temperature, the SiO_xF_y becomes volatile and leaves the sample [29].

2.3.2 Mask Selection

The ultimate test of a mask is the fidelity of pattern transfer into the silicon over the entire etching period. Since the mask interacts with the etching process parameters, it is vital to understand which masks to use for different etches. As stated earlier, if the selectivity is too low a thicker mask is required to achieve the desired etch depths. Furthermore, as the edge of the mask erodes it will impart undesired slope or features to the sidewalls of the etched structure, often referred to as mask-induced roughness. For these reasons, deep silicon etching requires higher selectivity masks. Conventional silicon etch masks are metal, oxides, and resist.

Metal masks, such as chrome, offer the advantage of high selectivity as high as thousands to one. This is primarily due to their lack of chemical reactivity with the etch gas molecules and their mechanical strength. However, metal masks typically induce detrimental effects such as notching at the top of the etched structures, due to image charge forces, and unwanted masking due to redeposited metal introduced

by ion sputtering. A particular problem with chrome during the cryogenic etch is that oxygen radicals appear to be locally consumed around the mask reducing the adjacent silicon passivation layer [17]. Silicon dioxide masks typically offer high selectivity (150:1 for Bosch and 200:1 for cryogenic etching) with the added cost of more complicated patterning. The oxide layer must be grown or deposited, followed by pattern transfer from another material or resist into the oxide mask. Increasing the number of processing steps increases the effort needed for accurate pattern transfer as well as the potential for reduction in mask fidelity. Resist masks offer the simplicity of a single processing step along with good selectivity (approximately 75:1 for Bosch and 100:1 for cryogenic etching). These selectivity values highly depend on process conditions and are seen to widely vary.

2.3.3 ICP Power

For both the Bosch process and the cryogenic silicon etch, etch rate is a primary consideration. In order to optimize this, radical density is increased while minimizing decreases in uniformity. The primary method of achieving high radical density is with ICP power; as the ICP power is increased, more energy is available to excite plasma constituents generated, causing the chemical etch rate to increase. However, this can lead to negative consequences of increased milling, reduced selectivity, and reduced passivation due sidewall bombardment. However, the two chemistries display slightly different responses to ICP power increases.

For the Bosch process, the ICP power for the etch and passivations steps is decoupled. By increasing the ICP power for the passivation step, passivation layer thickness can be increased independently of etch rate for a given passivation time, ignoring second order effects such as the C:F ratio in the resultant film due to gas species fractionation [27]. For the etch step, ICP power increases etch rate by increasing the F radical density. Finally, for both steps increasing the ICP power also slightly increases the bias between the plasma and the electrode. For the Bosch etch, this increase is generally negligible (a few volts) since the bias from CCP power is much larger (tens of volts).

For the cryogenic etch, applying more ICP power can significantly increase the amount of milling due to an increased bias voltage, as well increasing the substrate temperature. It is estimated that the exothermic formation of SiF_4 releases 2 W/cm^2 for an 8 µm/min etch rate. For an unmasked 6 inch Si wafer, this results in approximately 360 W of exothermic heating. Without proper cooling, the wafer temperature would increase at a rate of ≥10 °C/second [30, 31].

2.3.4 CCP Power

Increasing the CCP power establishes a larger electric field between the plasma and the table electrode. By imparting more momentum to the ions, the silicon milling rate increases. This typically increases the vertical etch rate (sputtering/milling), reduces the selectivity (faster mask erosion), increases lateral etching slightly (IADF broadening), and raises wafer temperature (higher incident ion energy).

The Bosch process is relatively robust to changes in CCP power; etching proceeds as soon as the passivation is removed, and is predominantly chemical. The Bosch etch is typically insensitive to temperature effects, while the cryogenic etch is extremely responsive to any temperature changes. Since the Bosch etch is performed at 15–20 °C, the polymer passivation layer is far from both the melting and freezing regimes.

The cryogenic etch, however, is very sensitive to CCP power changes. Heating by as little as 5 °C during the cryogenic etch reduces the passivation rate and changes sidewall angle dramatically. Passivation during the cryogenic etch roughly begins to occur around -85 °C. However, if the wafer is too cold, SF_x etch gases and SiF_x product gases can freeze on the sample sidewalls, adding to the SiO_xF_y passivation layer. Variations in table temperature by 5 °C due to oscillations in the table temperature controller have been seen to change the profile of deep etches adding a sinusoidal curvature to the sidewalls. Temperature is typically controlled by cooling the stage with liquid nitrogen or water and thermally connecting the wafer to the table by flowing helium between them.

2.3.5 Pattern Dependence and Chamber Hysteresis

Changing the amount of exposed silicon on a pattern can significantly alter the etch rate by moving the process into a reactant-limited regime. This is further complicated for the cryogenic etch, as a more exposed pattern leads to higher substrate heating and reduced passivation. This can be partially remedied by maintaining a large silicon loading through the use of carrier wafers. By attaching a smaller sample to a large carrier wafer, slight changes in sample mask patterning will be reduced by the relative area. However, this technique is impractical for high throughput applications. A more cost effective solution is calibration to a particular mask set in order to maximize the die area etched per process.

Cleanliness of the chamber can also change the effects of etches. Since the plasma interacts with the sidewalls as well as the substrate, residual molecules from previous etches can be redeposited on the etched surface, causing micromasking, or can chemically react with the etch gas. This is particularly true for the narrow process window of the cryogenic etch, where etch rate can easily be slowed by 50% in a unconditioned chamber.

2.4 Nanoscale Silicon Etching

The Pseudobosch process[4] is a mixed mode etching suitable for photonic and other nanoscale structures. It combines the gas chemistry of the Bosch process with the cryogenic etching strategy of simultaneous passivation and etching. Unlike deep silicon etching, nanoscale etching requires neither extraordinary selectivity nor large etch rates. On the contrary, moderate selectivity of 5:1 is acceptable and slower etch rates are more useful for accuracy of etch depths. Furthermore, Bosch etching and cryogenic etching prove to be unsuitable for very small structures due to the notching and lateral etching of the two chemistries, respectively. In exchange for the lower etch rate, pattern fidelity is improved because of highly controllable sidewalls and low undercutting effects.

[4]Recipe is found in the appendix, A.2.2

2.4.1 Gas Chemistries

For Pseudobosch, SF_6 is used as an etch gas while C_4F_8 is used to passivate simultaneously. Plasma parameters are similar to those used in the cryogenic etch, which has a lower ICP power and CCP power. Since incoming ions must constantly mill the continuously deposited fluorocarbon polymer layer, the etch rate is only 200–300 nm/min; this is a significant drop from a comparable Bosch process. The advantage of using C_4F_8 as the passivation gas in mixed mode enables processing at room temperature.

2.4.2 Mask Selection

Typical masks for nanoscale etches are based on the difficult patterning requirements. To define structures down to 20 nm, e-beam resists such as polymethylmethacrylate (PMMA) are employed with film thicknesses ranging from 500 nm down to 30 nm. The advantage of using this as the etch mask is the simplicity in pattern transfer: once the e-beam patterning is complete, the resist can be developed leaving the patterned etch mask. The disadvantage is that typical selectivity values range from 3:1 to 0.5:1. High resolution features require thinner resists; this can often limit the maximum etch depth due to low selectivity. Another polymer-based resist, ZEP-520A, offers the lithographic advantages of PMMA while offering a much higher selectivity ($\geq$4:1) to F-based etches like the Pseudobosch.[5].

A novel etch mask for silicon nanostructures is implanted gallium [32, 33]. With this method, Ga ions are implanted in the silicon substrate using a focused ion beam. Typical threshold dosages are about 10^{16} ions/cm^2 or 2000 μC/cm^2. For comparison, typical resist sensitivities range from 200–1200 μC/cm^2 when exposed on a 100 kV electron beam lithography system. An example of this mask is shown in figure 2.4 This masking technique is explored in further detail in Chapter 3.

[5]ZEP resist is partly halogenated PMMA, with a chlorine substituting for one of the hydrogens (compare ZEP's monomer formula $C_5H_7ClO_2$ to PMMA's $C_5H_8O_2$)

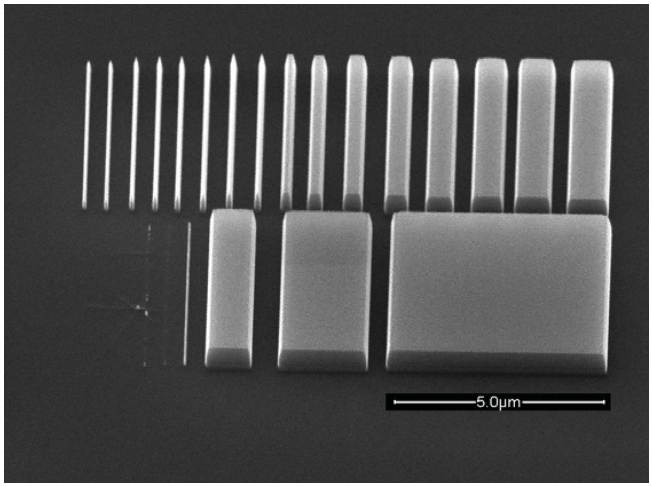


Figure 2.4. Pseudobosch etch of a Ga etch mask. Etch depth is 700 nm.

2.4.3 Etching Conditions and Optimization

By changing the ratio of the etch gas to passivation gas, SF_6:C_4F_8, the sidewall profile can be controlled. A typical ratio is 1:3 with the absolute gas flow rates dependent upon chamber volume, as sufficient flow is required to establish a chamber pressure of 10 mTorr; a good starting point is roughly 30 and 90 sccm respectively. Increasing the ratio improves the etch rate, reduces the selectivity, and drives the sidewall to be reentrant. Typical ICP power is around 1200 W combined with a slightly higher CCP power than that of the cryogenic etch of around 20 W. Increasing the CCP power again reduces the selectivity with a slight improvement in etching rates. Unlike cryogenic mixed mode, this etch is typically performed at room temperature or 15–20 °C.

2.5 Nanoscale Indium Phosphide Etching

In contrast to the previously discussed fluorine-based etch recipes, many III-V materials (GaAs, InP, etc.) require the use of chlorine-based chemistries. This is due to the difference in chemical properties of the etch products. As seen in the previous section, Ga implantation can serve as a mask in fluorine-based plasma. The proposed

mechanism for this masking capability is the formation of involatile GaF_x compounds that prevent further etching. Thus, for etching of Ga and other similar compounds, we expect that a Cl_2-based etch will result in faster etching rate and smoother sidewalls from the readily removed etch products. In this section, we will discuss an InP etch[6] that uses a hybrid gas mixture of Cl_2, CH_4, and H_2, used for etching waveguide structures in Chapter 5.

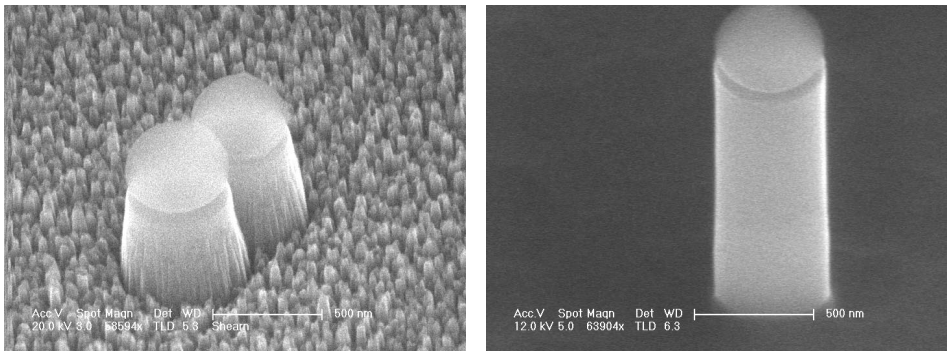
2.5.1 Gas Chemistries

The gas composition of this etching recipe is a hybrid between two established InP recipes. Specifically, high etch rate recipes with Cl_2- and Cl_2/Ar-based plasmas are well known but suffer from sidewall roughness and require high processing temperatures to volatilize $InCl_x$ species [34], as illustrated in Figure 2.5. Smooth etch recipes with CH_4/H_2 plasmas have also been studied but have prohibitively slow etch rates. In this case, the smoothness is a result of two factors. Firstly, the dominant etching mechanism of InP is the evolution of volatile products PH3 and $In(CH_3)_3$, which can be controlled by adjusting the gas flow rates [35]. Secondly, the deposition of CH films from the source gases serves to protect the sidewalls [36]. In our etch, we utilize a precise ratio of source gases that balances all these properties and takes interactions into account, such as removal of H and Cl ions by formation of HCl.

2.5.2 Mask Selection

Appropriate masks for the InP etch are metals and dielectrics. This is due to the high rate of mask erosion inherent in the etching conditions. The forward bias and thus bias voltage that drive ions toward the wafer surface are much higher than those found in the SF_6-based silicon etches in previous sections. This will make the etch more milling, and will help to maintain the same etch characteristics in other stoichiometries of interest, such as InGaAsP compounds. We utilized masks of silicon dioxide spheres and evaporated Au layers in the etching experiments. The selectivity

[6]Recipe is found in the appendix, A.2.4



(a) Low ICP (b) Sufficient ICP

Figure 2.5. InP etching temperature sensitivity. (a) Micromasking due to insufficient heating. (b) By increasing ICP power and thus raising sample temperature, micromasking is removed.

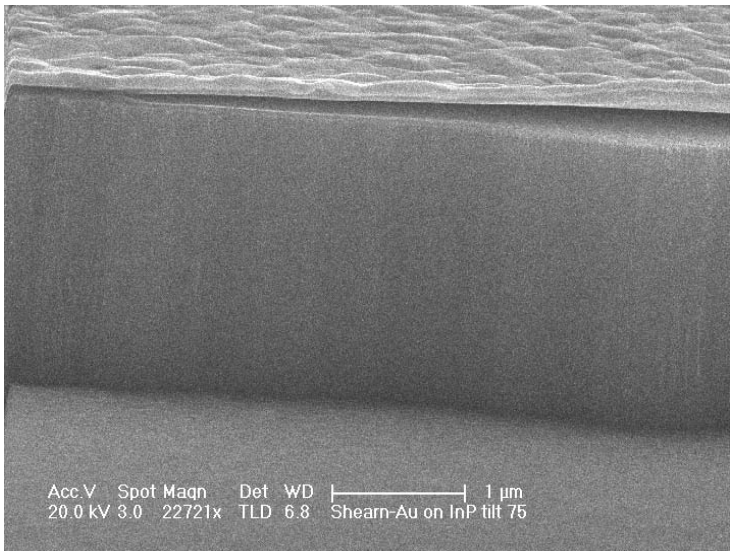
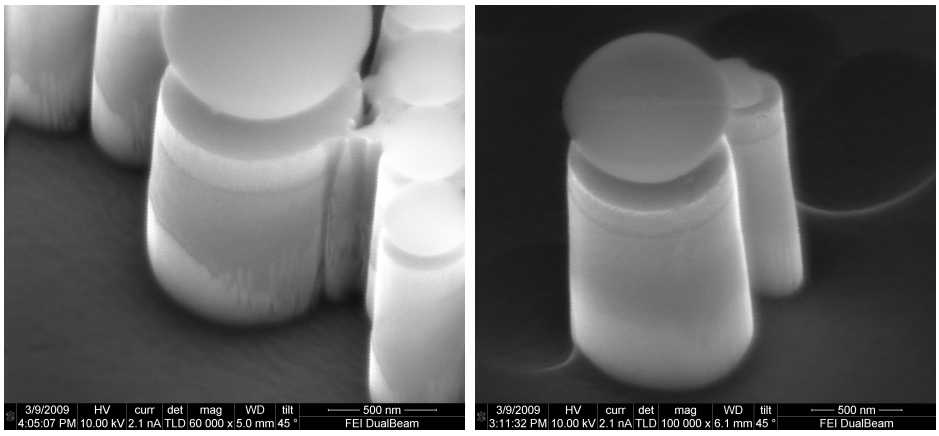


Figure 2.6. Anisotropic InP etch using a metal hardmask. Smoothness is only limited by mask irregularities

of oxide was approximately 10:1; however, faceting occurred before the mask was completely eroded, limiting the useful selectivity to a more modest 4:1. In deeper nanoscale etching applications, a silicon nitride or metal mask is preferred as it has high selectivity and does not suffer from faceting as readily as oxide. As seen in Figure 2.6, the metal hardmask has eliminated most pattern-induced roughness seen in figure 2.5.



(a) High CCP (b) Adequate CCP

Figure 2.7. CCP power dependence of InGaAsP on InP etching: (a) excessive CCP power and (b) adequate CCP power. The features at the bottom of the pillar are due to faceting and redeposition of mask materials

2.5.3 Etching Conditions and Optimization

Our etch had Cl_2:H_2:CH_4 ratio of 8:7:4 with actual gas flows of 32 sccm Cl_2, 28 sccm H_2, and 16 sccm CH_4 and a chamber pressure of 4 mTorr. The table was heated to 60°C to reduce polymer deposition, and no helium backing was applied in order to have the plasma heat the sample. This heating is key to proper etch characteristics, as too little heat will cause micromasking due to involatile gas products such as $InCl_x$. The CCP power was 180 W, found experimentally by varying until an anisotropic profile was achieved without excessive mask erosion. This resulted in a cathode bias of approximately 200 V. ICP power was 2200 W, also found experimentally by monitoring the transition of black InP to smooth InP due to the cessation of micromasking during etching. The etch rate of pure InP was measured to be 1.2 μm/min.

During some etches with identical conditions, a roughening of the bottom surface was noticed due to chamber cleanliness. The sensitivity of this etch to chamber condition is not as high as the cryogenic Si etch described earlier, but reproducible results require a regular cleaning schedule to return the chamber to a known clean

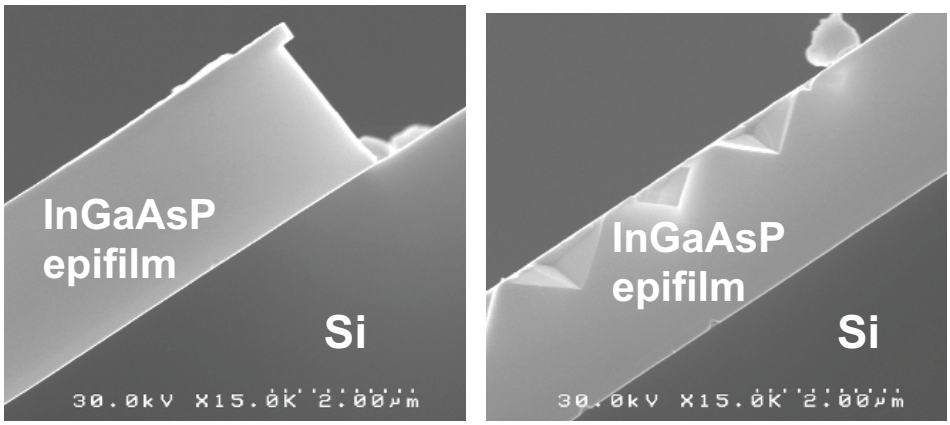
state. This is best implemented by running a short, minute-long SF_6 cleaning plasma just before etching to remove any contaminants that are readily incorporated into the plasma. For long term cleanliness, periodic hour-long SF_6/O_2 plasma is run. The frequency depends on what other etches have been performed previously, but is typically one hour of cleaning per three to four hours of etching. In an industrial setting, this could be done in shorter periods between each wafer to maintain a constant chamber state.

2.6 Plasma-Assisted Wafer Bonding

In order to best utilize the capabilities of the patterned Si-based materials and InP-based III-V materials described above, we require a way to combine them onto the same platform. As an alternative to epitaxial growth, direct wafer bonding provides a way to join together two flat and clean semiconductor surfaces at room temperature without the restriction of matching lattice constants. The intermolecular and interatomic forces bring the two wafers together and the bonds form at the interface. By introducing a superlattice defect-blocking layer, dopants and defects are prevented from migrating from the bonding interface to the active region so that the luminescence from the multiple quantum well structure can be preserved [37]. To increase the bond strength, a high-temperature post-bonding annealing step is usually required. However, this high-temperature annealing step induces material degradation and is incompatible with backend Si CMOS processing. For this purpose, many efforts have been put into reducing the annealing temperature while keeping a strong bonding [38, 39, 40]. The technique is integral to the III-V hybrid structures described in Chapter 5.

2.6.1 Direct Wafer Bonding

For Si-to-InP wafer bonding, a pre-bonding oxygen plasma treatment for both wafer surfaces has been demonstrated to yield a very spontaneous bonding at room temperature [41]. Similar to previously discussed etching plasmas, the pre-bonding plasma



(a) Edge (b) Center

Figure 2.8. SEM cross-sectional view of InGaAsP epifilm on Si by wafer bonding after the step of InP substrate removal. The InGaAsP epifilm consists of an InGaAs contact layer at the top, a p-InP upper cladding layer at middle followed by an InGaAsP active layer and then an n-InP lower cladding layer at the bottom. (a) Zoom at one end of the epifilm. The top InGaAs layer is protrusive at the end due to its different composition from the p-InP layer below. (b) Pyramids at the top of p-InP layer are results of HCl wet etching during InP substrate removal due to the damaged outer InGaAs layer.

aims to have a high density of chemically active species arrive at the surface with a low incident power to minimize surface damages, such as dislocations, that work against bond formation. The post-bonding annealing temperature can be below 200 °C while the interface strength can be as high as the bulk fracture energy of InP. The oxygen plasma is used to remove hydrocarbon and water molecules so as to reduce the probability of the formation of interfacial bubbles and voids during post-bonding annealing. Additionally, the plasma treatment generates a very smooth and reactive thin oxide layer which helps in the bonding process.

2.6.2 Bonding Procedure

In this work, an SOI wafer and an InP wafer with InGaAsP epitaxial film were bonded together. The bonding procedure begins with solvent cleaning of both the Si wafer and an InP wafer surfaces. Depending on application, an 10-nm-thick oxide layer can be grown on top of the Si wafer to enhance the bonding strength or omitted if the current wafer structure cannot withstand a high temperature oxidation step. Then the surfaces of the two wafers are activated through exposure to oxygen plasma[7], and bonded together under a pressure of 0.1 MPa at 150 °C for 2 h. Following the bonding process, the InP substrate is removed by HCl wet etching. Figure 2.8 clearly shows the cross-sectional structure consisting of the remaining InGaAsP epifilm bonded onto the Si substrate. The bonding interface between the epifilm and Si is thin and smooth. In Figure 2.8(a), the top InGaAs layer has been undercut due to its different composition from the p-InP layer below. In Figure 2.8(b) focuses on a middle part of the epifilm. The pyramids at the top of p-InP layer are results of HCl wet etching during InP substrate removal due to the damaged outer InGaAs layer.

2.7 Conclusion

In this chapter, we have described plasma applications of etching and surface modification to semiconductor materials. The process latitude available in modern ICP-RIE systems has enabled these novel processes. This is a direct consequence of the multitude of changes one can effect on a plasma by changing the pressure, driving fields, gases, temperature, and other parameters as discussed in the introduction. In particular, temperature-controlled stages capable of cryogenic cooling have given process engineers the ability to tune the types and rates of chemical reactions that occur on their samples. This was strongly illustrated in our discussion of cryogenic silicon etching, but a similar scheme could be imagined for other materials, given appropriate gas selection. We demonstrated both deep Si etching appropriate for MEMS as well as nanoscale Si etching, and discussed the difference in processing details between these

[7]Recipe is found in the appendix, A.2.6

two regimes. By using a plasma treatment of both surfaces, we were able to join together two dissimilar semiconductors because this method is not affected by lattice constant mismatch. This bonding technique showed room temperature spontaneous bonding which can be annealed at 200 °C or less while keeping a high interfacial strength. By combining all of these techniques, integrated photonic structures are possible.

Chapter 3

Ga Beam Lithography for Silicon Nanostructures

3.1 Introduction

In this chapter, we examine a novel masking method using gallium implantation into silicon for pattern definition. By using a fluorine etch chemistry that displays high preferential etching of silicon over that of gallium (Ga), we show resist-free fabrication of high aspect ratio nano- and microstructures in silicon using a Focused Ion Beam (FIB) and an inductively coupled plasma reactive ion etcher (ICP-RIE). Silicon etch masks are patterned via Ga ion implantation in a FIB and then anisotropic etched in an ICP-RIE using fluorinated etch chemistries. We determine the critical areal density of the implanted Ga layer in silicon required to achieve a desired etch depth for both a Pseudobosch (SF_6/C_4F_8) and cryogenic fluorine (SF_6/O_2) silicon etch. High fidelity nanoscale structures down to 30 nm and high aspect ratio structures of 17:1 are demonstrated. Since etch masks may be patterned on uneven surfaces, we utilize this lithography to create multilayer structures in silicon. The linear selectivity versus implanted Ga density enables grayscale lithography. Limits on the ultimate resolution and selectivity of Ga lithography are also discussed, along with a brief analysis of this masking technique for photonic applications.[1]

[1]Portions of this chapter are adapted from a publication with M. David Henry and Bophan Chhim [33].

3.2 Observations of Ga masking

A cornerstone of silicon fabrication is the ability to pattern a structure on a planar silicon surface and subsequently use this pattern as a mask to etch the structure in the silicon. There are a variety of ways of defining this pattern in resist, including ultraviolet, electron beam, or nanoimprint lithography [42, 43]. Alternatively, direct removal of silicon via sputtering by focused ion beam (FIB) can circumvent the need for resist at the expense of low throughput as well as aspect ratio and minimum feature size limitations [44, 45]. However, FIB implantation of gallium into silicon can be used to define nanoscale structures directly without resist at any stage of the fabrication, achieving both high throughput and high aspect ratio structures.

One of the first observations of high selectivity Ga masking was in preferential wet etching of the silicon over Ga-doped silicon [46]. The hypothesized masking mechanism was the bonding of oxygen to Ga, forming GaO_x layer that is chemically resistant to the KOH wet etch and acts as a mask for the silicon from the hydroxide chemical attack. However, not only is this mask resilient against wet chemical etching, it is also effective for masking fluorinated reactive ion etching [47]. Further demonstrations of Ga-based masking in plasma etching showed that deep reactive ion etching (DRIE) with time-multiplexed etch chemistries can produce micron scale features with nanometer scale etch depths [48]. This work was significantly improved upon when a cryogenic SF_6/O_2 silicon etch was used with an implanted Ga mask [32]. What allowed for the improvement was the fact that the mixed mode cryogenic silicon etch dramatically reduced the mechanical milling aspect, which is proportional to the bias voltage, with an increase in chemical etching thereby increasing the etch mask selectivity [49]. Since the cryogenic etching employs the use of sidewall passivation, the cryogenic silicon etch can achieve deep etches similar to the chopping etch chemistries while reducing the etch mask damage. However, when this etch chemistry is applied to nanometer scale structures, incomplete passivation and inherent etch recipe limitations resulted in severe undercutting. The low pattern fidelity of the nanoscale structures is problematic for establishing a realistic minimum feature

size figure of merit.

Due to properties of the etching plasma, there is a trade off between selectivity and anisotropy. By operating at different points of this trade off, we have developed etch conditions appropriate for different applications. For minimum feature size etching, we employ a mixed-mode SF_6/C_4F_8 plasma that has moderate selectivity and high anisotropy, referred to here as Pseudobosch [50], and describe feature size and etch depth dependence on implantation dose. For higher aspect ratio structures at the expense of mask notching and lower anisotropy, we use a cryogenic SF_6/O_2 plasma [50]. Finally, at the limit of maximum selectivity and complete isotropy, we employ a cryogenic SF_6 plasma appropriate for release of Ga implantation defined membrane. By understanding this selectivity to anisotropy trade off, we extend previous work by moving out of the undercut-limited regime of the cryogenic etch.

3.3 Mask Patterning Using FIB

Patterning of the Ga etch mask was accomplished using the dual beam Nova FIB/SEM by FEI. A cleaned silicon sample is placed at the eucentric height and rotated such that the ion beam strikes perpendicular to the substrate surface. For a selected beam current, the Ga beam is focused at the edge of the substrate. Automated write programs specifying the pattern and dwell times are then executed to raster the ion beam. In a manner analogous to a scanning electron microscope, the FIB accelerates the Ga ions to the surface of the silicon substrate using various accelerating beam voltages. The magnitude of the beam voltage controls both the implantation depth and the thickness of the Ga layer.

To estimate the effect of the beam voltage on the thickness of the implantation layer and implantation depth, simulations using Stopping and Range of Ions in Matter (SRIM/TRIM) were performed for implanting Ga ions into Silicon [51]. The results are summarized in figure 3.1; here we take the vertical straggle length of the implantation to approximate the thickness of the Ga-implanted layer for the purpose of effective selectivity calculations. All implantations performed are with a 30 kV

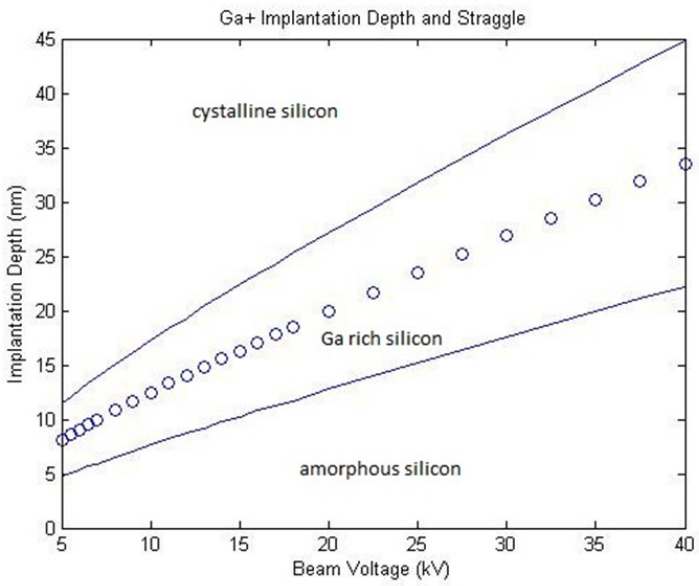


Figure 3.1. Ga implantation depth for varying FIB beam voltages as simulated using TRIM. The etch mask thickness is approximated twice the straggle length.

beam voltage. From the implantation simulations of 30 kV beams, we approximate the implantation damage to the top 15 nm of silicon, creating amorphous silicon, and the next 20 nm below as a Ga rich amorphous silicon layer, consistent with TEM measurements [52].

To investigate patterning over the entire nanometer length scale, three sets of patterns were generated. To measure the nanometer range, we patterned squares starting at 500 nm and ending at 50 nm stepped in 50 nm increments. The dose columns began at 5.3×10^{15} ions·cm^{-2} and ended in 1.96×10^{17} ions·cm^{-2} with the dose stepped in approximately 1×10^{16} ions·cm^{-2} increments. To determine sub 200 nm resolution, we again patterned squares starting at 200 nm and ending at 20 nm stepped in 20 nm increments. The third pattern arrays were circles starting at 100 nm in diameter and ending at 10 nm in diameter stepped in 10 nm increments. Both the second and third pattern arrays, the dose column began with 1.25×10^{16} ions·cm^{-2} and ended in 1.25×10^{17} ions·cm^{-2} with the dose stepped in approximately 1.25×10^{16} ions·cm^{-2} increments using a measured 6.87 pA beam.

For the micron scaled structures we created dose arrays of 5 micron by 5 micron

(a) Etch 1

Etch Parameters		
Gas	SF_6	33 sccm
	C_4F_8	**50 sccm**
	Pressure	10 mT
Plasma	CCP	**10 W**
	ICP	1200 W
	Voltage	54 V
Wafer	Temperature	15 °C
	He backing	10 T
	Stage height	20 mm

(b) Etch 2 & 3

Etch Parameters		
Gas	SF_6	33 sccm
	C_4F_8	**68 sccm**
	Pressure	10 mT
Plasma	CCP	**15 W**
	ICP	1200 W
	Voltage	61 V
Wafer	Temperature	15 °C
	He backing	10 T
	Stage height	20 mm

Table 3.1. Recipes for the two dose array etches. Changed parameters shown in bold.

squares separated by approximately 10 microns. Each square dose was varied by incrementing the write time 2 second. With the beam current at 100 pA, this provided a dose step of 5×10^{16} ions·cm^{-2}. The dose array began at 1×10^{16} ions·cm^{-2} and stopped at 5×10^{16} ions·cm^{-2}. After implantation, verification of the patterning can be seen using a scanning electron microscope (SEM). Inset of Figure 3.2 is a SEM of the dose array for the micron scales features.

3.4 Pseudobosch Silicon Etching

Patterned Ga implanted silicon samples were anisotropically etched in an Oxford Instruments PlasmaLab 100 inductively coupled plasma reactive ion etcher (ICP-RIE) 380. The Si samples, N-doped ($\langle 100\rangle$, ρ =1-10 ohm·cm) and P-doped ($\langle 100\rangle$, $\rho = 0.005$ ohm·cm), were placed on a 6 inch silicon carrier wafer using Fomblin oil as an adhesive and thermal conductor. The etch chemistry utilized was a mixed mode etch using SF_6 as the etch gas and C_4F_8 as a modified form of the Pseudobosch silicon etch.[2]

The first dose array etch was performed under the conditions summarized in Table 3.0(a). In this case, the CCP power was lowered from a nominal value of 20 W to 10 W and the C_4F_8 gas flow was a lower from 68 sccm to 50 sccm. Conditions

[2]Original recipe is found in the appendix, A.2.2

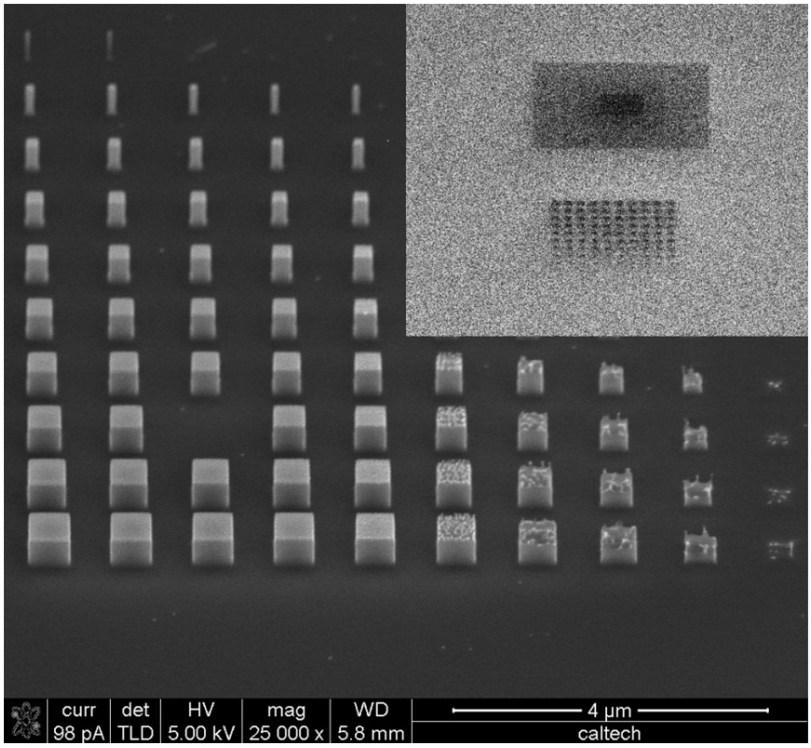


Figure 3.2. SEM image of a dose array for nanoscale SF_6/C_4F_8 etch. Etch depth was 460 nm with the squares ranging from 500 nm down to 50 nm in 50 nm increments. Inset is a SEM image of Ga implanted nanoscale dose array in silicon below a large square implanted while focusing.

for the second and third dose arrays were summarized in table 3.0(b). CCP power was increased to 15 W and the C_4F_8 gas was returned to 68 sccm; this modification improved pattern fidelity for sub 100 nm structures. Upon completion of etching, the Fomblin was removed using Isopropyl Alcohol (IPA) and the sample imaged by SEM. Figure 3.2 shows the results of this process.

3.4.1 Determination of Threshold Dose and Selectivity

Dose arrays of 50 nm to 500 nm squares were etched for different times so that etch rate, minimum dose for a required depth, the critical dose, and minimum structure size could be ascertained. Samples were inspected in SEM to determine the time and height of each structure. The results of these measurements are shown in figure 3.3.

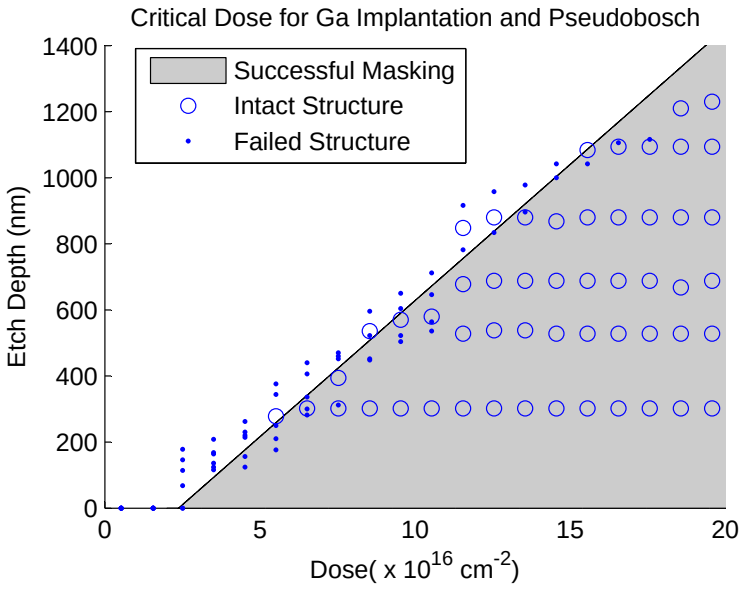


Figure 3.3. Required dose for a given etch depth for the Pseudobosch etch. The shaded area indicates acceptable dose for achieving a desired etch depth.

Two features of this graph are important to notice. First, no measurable masking occurs below a particular dose, termed here as the threshold dose. Next, the height of failure displays an approximately linear relationship with the areal dose.

Motivated by this apparent structure, we attempted to fit the data with the following equation:

$$h_{critical} = \frac{k_{etch}}{k_{erosion}} \cdot (d_{critical} - d_{threshold}) \tag{3.1}$$

where $h_{critical}$ is the height of the etched structure at failure, k_{etch} is the experimentally measured etch rate, $d_{critical}$ is the measured dose from FIB implantation of the failed structure, and $k_{erosion}$ and $d_{threshold}$ are the effective erosion rate of the mask and the threshold dose treated as free parameters to be determined by a least squares fit to the data. The etch rate, k_{etch} was determined to be 186 nm/min for the P-doped silicon samples. For the Pseudobosch data, the fit yields the following fit parameters:

$$h_{critical} = \frac{0.186[\frac{\mu m}{min}]}{2.45 \times 10^{16}[\frac{ions \cdot cm^{-2}}{min}]} \cdot (d_{critical} - 1.85 \times 10^{16}[ions \cdot cm^{-2}]) \tag{3.2}$$

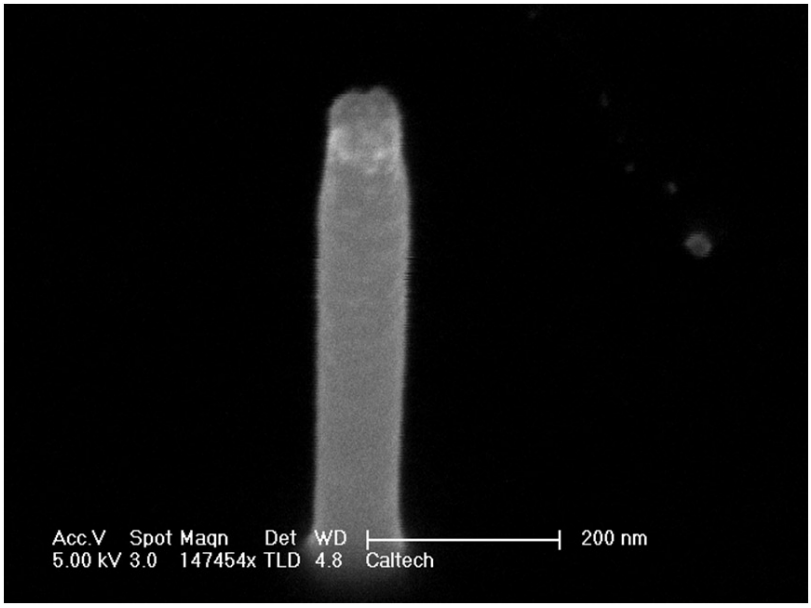


Figure 3.4. SEM image of a silicon nanopillar, 72 nm in diameter and 800 nm tall.

Since the implantation thickness was approximated as 20 nm, the selectivity of mask improves as the areal dose increases (increasing the density of the Ga mask) and is also described using equation 3.2 by dividing the etch height by the mask thickness of 20 nm. Although the etch damage is approximated to be the 15 nm of amorphous silicon on the top of the etch mask, we note that surface remains notably smooth. The first dose array demonstrates that this masking technique can create, at the minimum write pattern of 50 nm, a 72 nm diameter nanopillars and 800 nm tall with sidewall and roughness of less than 5 nm, figure 3.4. Although the patterned size was originally 50 nm, the increase in size to 72 nm is consistent to SEM resolution and SRIM calculations of having a lateral straggle length of 7.2 nm. Other contributions to the mask size increase can be attributed to several factors including approximation of the beam as Gaussian and the ion beam being slightly defocused. We approximate the lateral straggle as being the most significant of all the contributions at this beam voltage. Resolution and characterization of the Ga beam width will be discussed later in this chapter [53, 54, 44, 45].

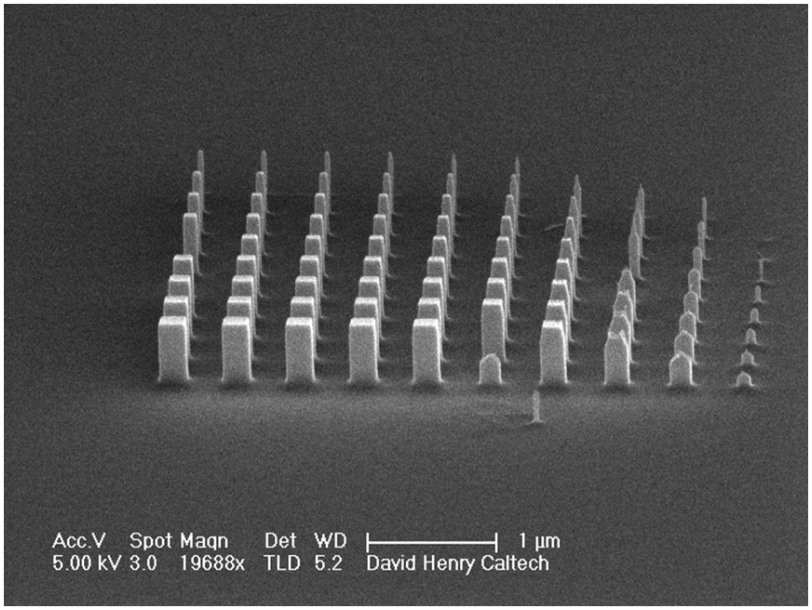


Figure 3.5. SEM image of second dose array for nanoscale SF_6/C_4F_8 etch. Etch depth was 448 nm with the squares ranging from 200 nm down to 20 nm in 20 nm increments.

3.4.2 Determination of Minimum Feature Size

To investigate the minimum structure size, we employed the second and third dose array. The second dose array consisted of squares etched 448 nm tall, figure 3.5. The minimum pattern etched was a 43 nm square with an aspect ratio of 10:1. Although a 20 nm square was implanted, the SEM shows only a mound where the pattern began to etch but ultimately failed, possibly due to a lower Ga concentration caused by imperfect focusing. It is also clear that the minimum dose of 1.25×10^{16} ions·cm^{-2}was not sufficient to protect the silicon much greater than 70 nm. The third dose array patterns were circles for vertical silicon nanowire fabrication and were etched simultaneously with the second dose array pattern. The minimum pattern etched was the 31 nm diameter pillar, figure 3.6. The etch was reentrant at 89.15 degrees causing the base of the pillar to be at an 18 nm diameter. Although it is clear that some masking occurred for the 20 nm pattern, the reentrant angle did not permit the structure to withstand the etch. Important to note is the higher fidelity of this patterning as compared to previous demonstrations.

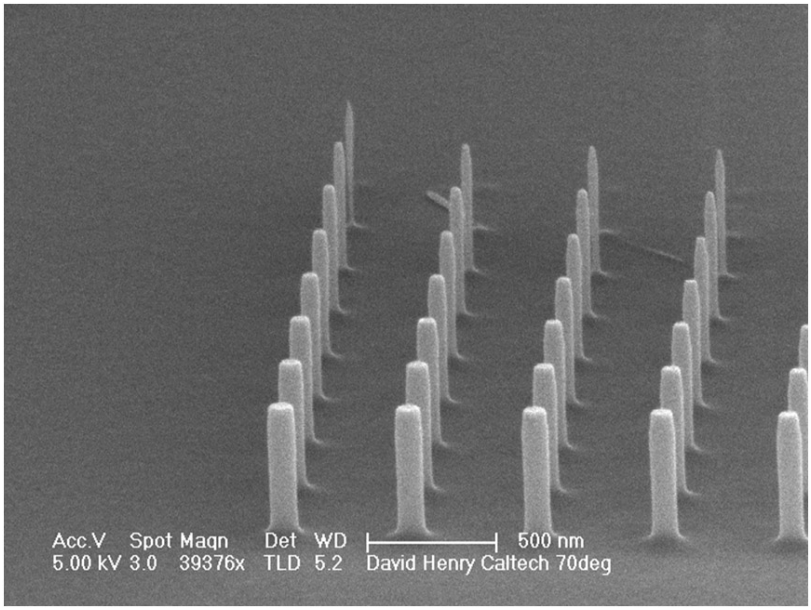


Figure 3.6. SEM image of third dose array for nanoscale SF_6/C_4F_8 etch. Etch depth was 448 nm with the pillars ranging from 100 nm down to 10 nm diameters in 10 nm increments.

This etch attained a very high selectivity with no oxygen in the etch chemistry. This is contrary to the masking mechanism of GaO_x forming at the surface proposed elsewhere [47]. Formation of a GaO_x layer during sample exposure to ambient air is also excluded due to the 28nm implantation depth. This leads us to hypothesize another masking mechanism. Fluorine can bond with the Ga to create an involatile GaF_x mask, which may also contribute to further physical sputtering resistance. This is consistent with previous results using reactive ion etching with SF_6 which relies on F ions for etching [47, 48, 32].

3.5 Cryogenic Silicon Etching

Using the same etching system and mounting techniques as the nanoscale etch, micron sized features were also etched to determine the etch rate and threshold dose for a required depth. The etch chemistry employed for this scale was a mixed mode cryogenic silicon etch, with conditions shown in Table 3.2.

Etch Parameters		
Gas	SF_6	70 sccm
	C_4F_8	**6.5 sccm**
	Pressure	10 mT
Plasma	CCP	**10W**
	ICP	900W
	Voltage	54V
Wafer	Temperature	**-130 °C**
	He backing	10 T
	Stage height	20mm

Table 3.2. Recipes for the cryogenic dose array etches. Changed parameters shown in bold.

3.5.1 Determination of Threshold Dose and Selectivity

The cryogenic dose array, described earlier, was etched for process times of 1, 3, 10, 20 and 40 minutes with a measured etch rate, k_{etch}, of 1.03 μm/minute; the results are detailed in figure 3.7. The etch depth dependence on dose for the cryogenic etch was least squares fit and is described by equation 3.3:

$$h_{critical} = \frac{1.03[\frac{\mu m}{min}]}{0.06736 \times 10^{16}[\frac{ions \cdot cm^{-2}}{min}]} \cdot (d_{critical} - 2.2 \times 10^{16}[ions \cdot cm^{-2}]) \qquad (3.3)$$

The CCP power, and subsequently the bias voltage, was intentionally set to match that of the Pseudobosch etch while other were left unchanged. Although the ICP and gas chemistry changes the plasma density, matching the bias voltages allows for the milling aspect of the two etch chemistries to be more closely compared.

Interestingly, $d_{threshold}$ is nearly the same for both etch chemistries (2.2×10^{16} ions·cm^{-2} as compared to 1.85×10^{16} ions·cm^{-2}), while $k_{erosion}$ for the cryogenic etch is nearly two orders of magnitude lower than for Pseudobosch. This threshold dose, etched with 10 W of CCP power, is consistent with other experiments with 2-3 W of CCP power and with an etch rate approximately twice as large as our reported value [32]. To compare the fidelity of the Pseudobosch etch to that of the cryogenic, a smaller feature size Pseudobosch dose array pattern was cryogenically etched for 1 minute

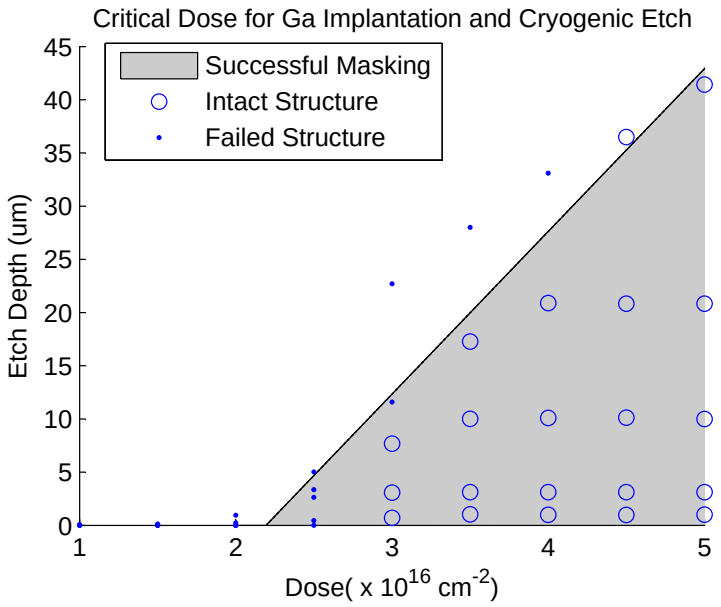


Figure 3.7. Required dose for a given etch depth for the Cryogenic silicon etch. The shaded area indicates acceptable dose for achieving a desired etch depth.

(approximately 1 μm). The minimum resolvable feature was a 350 nm square mask with the pillar body 200 nm at its widest spot, figure 3.8.

3.6 Multilevel and Grayscale Etch Masking

One of the most significant advantages of using Ga implanted etch masks is that unlike photolithography, which requires a planar surface for effective spin coating and exposure, the FIB can pattern non-planar structures. A second advantage of Ga masking is the linear relationship of etch depth to dose beyond the threshold dose. Utilizing these two advantages, we demonstrate the feasibility of three dimensional structures in silicon using multi-exposure and grayscale etch masking.

3.6.1 Multilevel Masking

Since the Ga beam does not require a polymer resist in which to define a pattern, one may perform multiple implantations for etch masking regardless of sample surface to-

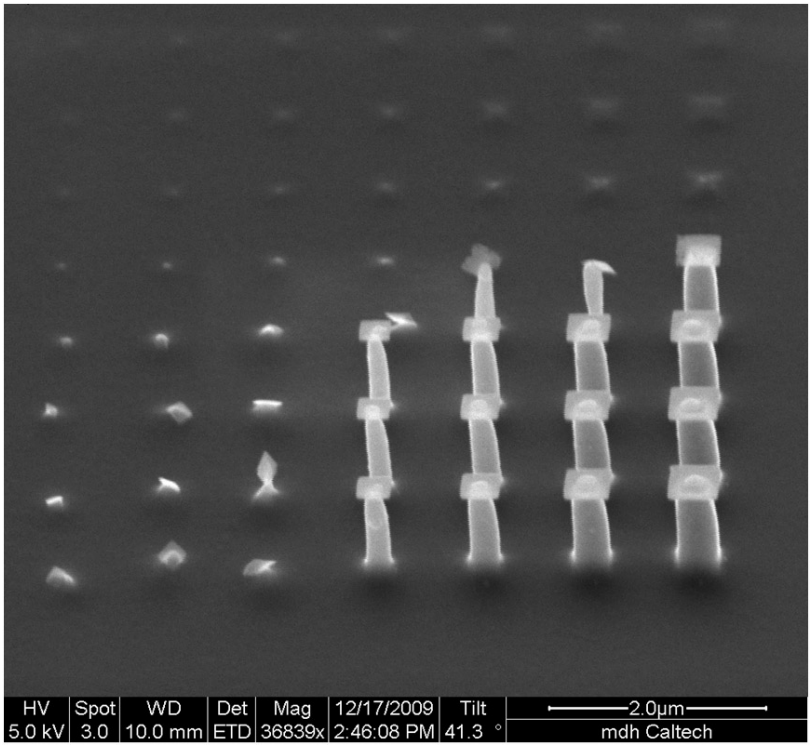


Figure 3.8. SEM image of Ga masked silicon squares, cryogenically etched to 1 µm tall, to quantify the mask undercut associated with cryogenic etching. The pattern etched is identical to that used for the Pseudobosch dose array.

pography. Experimentally, this fabrication procedure proceeds as follows: implant initial mask, etch the silicon, implant second pattern, and etch the silicon. This repeating sequence can continue for as long at the Ga etch mask remains. Re-implantation of previous structures can also extend the critical height for these structures.

We demonstrated this technique using both the Pseudobosch and the cryogenic etch to create a suspended silicon nanowire connected to two pads. First, two 10 µm diameter circles separated by 10 µm were Ga implanted at a dose of 2×10^{17} ions·cm^{-2}. The structure was then etched to a height of 0.5 µm using the Pseudobosch etch. A Ga mask was then implanted in the shape of a rectangle connecting the two pillars with the same dose as the circles. A mask undercutting cryogenic etch was then performed for an etch height of 5 µm; this step utilized the undercut to remove all unmasked silicon below the rectangle. The resulting structure was an 80 nm by 20 nm

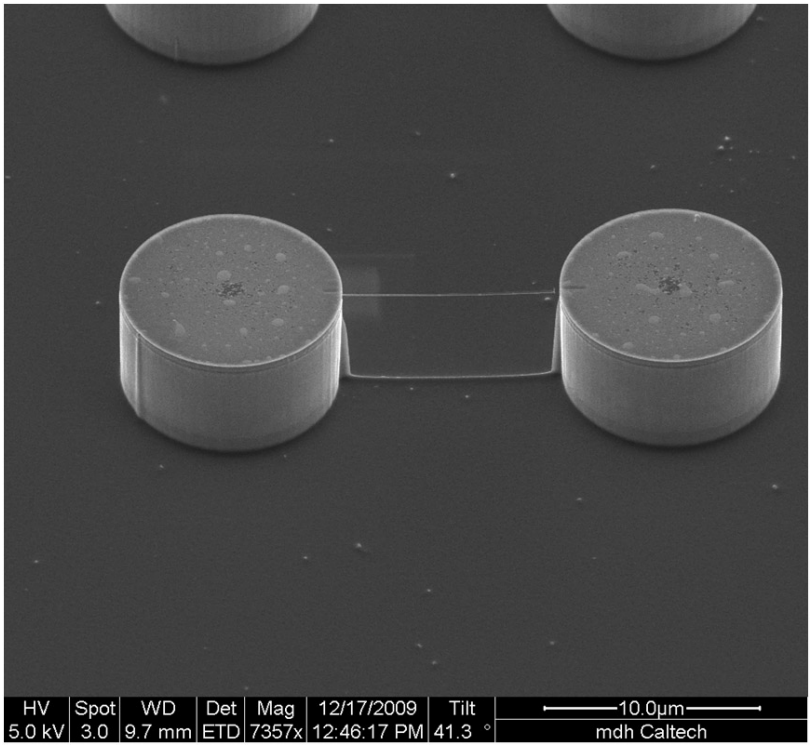


Figure 3.9. SEM image of 10 µm diameter silicon pillars, etched 5 µm tall, with an 80 by 20 nm silicon nanowire suspended in between. The wire is connected 500 nm below the tops of the pillars.

silicon nanowire suspended between two 10 µm diameter pillars etched 5 µm tall with the nanowire connected half a micron below the pillar tops, figure 3.9. This technique utilized the advantages of each etch, the high pattern fidelity of the Pseudobosch etch and the inherent undercutting and high selectivity of the cryogenic etch.

3.6.2 Grayscale Masking

A second applicable technique is the creation of graded structures which utilizes the observation of the etch depth's linear dependence on the critical dose. Here, the structures are dosed to different critical doses and etched to the desired height. At the heights corresponding to their critical dose, the structures will then start to etch at the same rate as the substrate, in a manner similar in principle to grayscale lithography [55, 56]. These implanted structures can then be etched to create sloped features such as blazed gratings and optical lenses. This idea was demonstrated using

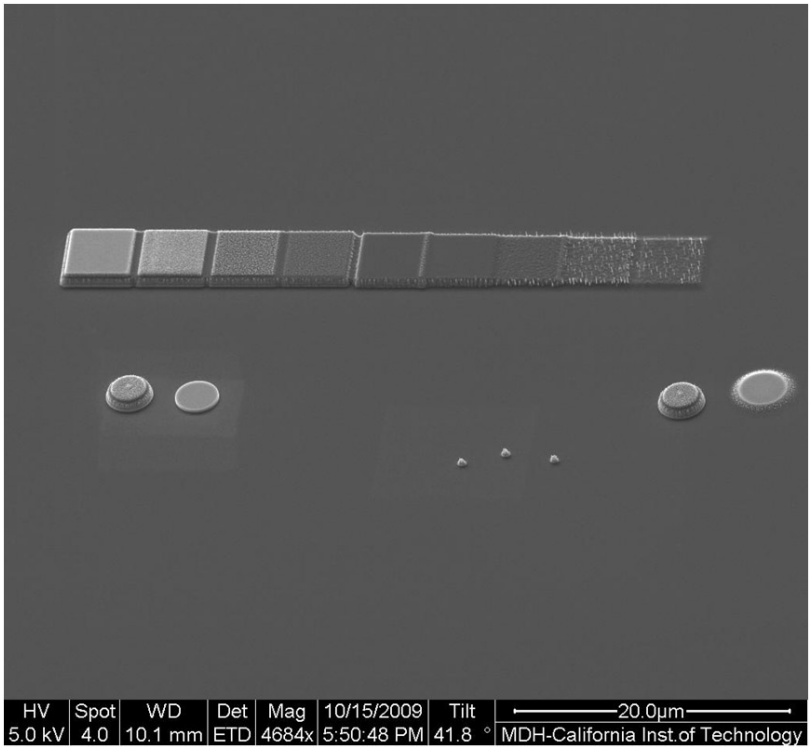


Figure 3.10. SEM image of 5 µm squares with varied doses. When the etch depth increases over the critical dose depth, the structure begins to etch but maintains its relative height to its neighbor.

nine 5 µm squares arranged in a row. Each square's dose was increased approximately 2.5×10^{16} ions·cm^{-2} more than the neighboring square for a dose ranging from 2.5–22.5 $\times10^{16}$ ions·cm^{-2} and etched using the Pseudobosch etch. This created the stair step set of platforms shown figure 3.10.

3.7 Resolution limitations and masking mechanism

3.7.1 Resolution limit

The theoretical limit to the highest resolution structures is highly dependent on the beam spot size and the accelerating beam voltage. These two parameters define the effective implantation masking area, as the spot size establishes the kernel to be convolved with the desired dose profile and the accelerating voltage determines the further spread of ions after interacting with the silicon. For our system, a theoretical

resolution limit can be estimated by summing these dimensions in quadrature[44]:

$$(d_{system})^2 = (d_{spot})^2 + (d_{ion})^2 \tag{3.4}$$

For our minimum spot size $d_{spot} = 5$ nm and lateral ion spread at 5kV $d_{ion} = 3.2$ nm + 1.8 nm (1-σ straggle), resulting is $d_{system} = 7.07$ nm. For our experiments at 30kV, $d_{ion} = 9.9$ nm + 5.6 nm, resulting in $d_{system} = 16.2$ nm, as compared to our minimum realized structure of 43 nm. This analysis does not take into account any excess resolution loss from deflection error, exposure scheme (amount of overlap between shots was 50%), defocus, or other experimental parameters which may account for our measured minimum [57, 58].

3.7.2 Maximum Implanted Dose

To achieve the greatest etch depths, and hence highest selectivity, we would like to maximize the amount of Ga present in the top layer. However, further exposure of the beam past a certain dwell time leads to a steady state where the influx of Ga is balanced by the sputtered Ga. Displayed in figure 3.11 is the areal concentration of implanted Ga in the silicon sample as a function of total ion flux for a 30kV beam. This is approximated by the total flux of Ga atoms minus the sputtered Ga atoms, using the composition-dependent sputter yield computed by Monte Carlo simulation [59].

As expected, for low doses the areal dose implanted is linear with total flux, as the sputtered material has a low concentration of Ga relative to the amount implanted. However, as the sputtered depth approaches the mean implantation depth of 27 nm, the total concentration of Ga in the sputtered material increases. By 28.4 nm we are at an areal concentration of 10^{17} Ga ions·cm^{-2}, which is lower than total incident flux by 16%. The Ga sputter yield rapidly increases from this point, requiring an enormous amount of incident flux to increase the implanted concentration. As an example, doubling the target concentration from 10^{17} to 2×10^{17} Ga ions·cm^{-2} requires more than five times the incident flux, which sputter 144 nm of Si below attaining the

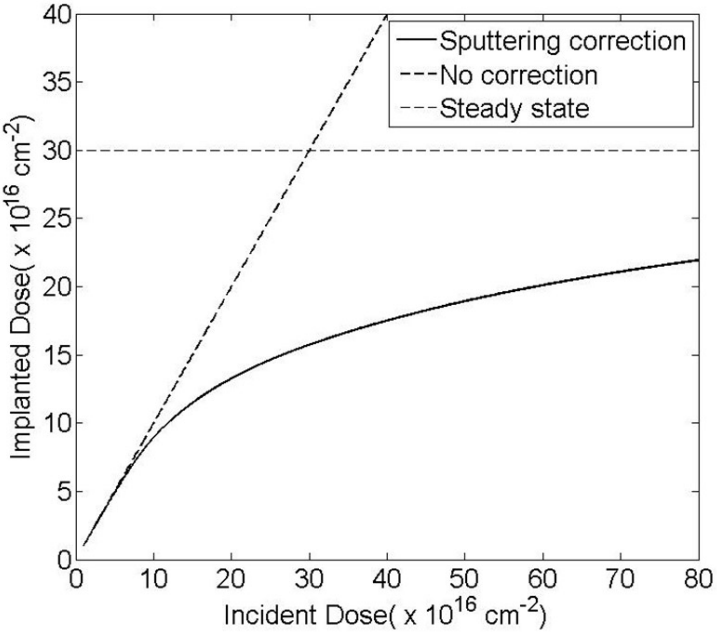


Figure 3.11. Plot of implanted dose as a function of incident dose, with limiting value of 3×10^{17} Ga ions·cm^{-2}.

desired concentration. The maximum implanted value at steady state, calculated to be 3×10^{17} Ga ions·cm^{-2}, is dependent on the ratio of the mean implantation depth and the sputter yield. For our two etch chemistries, this leads to a theoretical maximum etch depth of 3406 nm for the Pseudobosch chemistry and 425 μm for the cryogenic etch chemistry and a maximum effective selectivity of 85 and 10625 respectively assuming a 40 nm mask layer. However, practically achievable figures will be lower, as determined by fidelity requirement and the point of diminishing returns in implantation, where the selectivity increase is less than the amount milled by the Ga beam.

3.7.3 Possible Origin of the threshold dose

Based on SRIM simulations, the 1-σ average density of Ga assuming no phase segregation or preferential removal of silicon is approximately 14% of the density of a pure Ga layer. However, silicon's low solubility in Ga is well known [60], so the assumption of complete segregation of the implanted Ga combined with measured Ga lattice

constants leads to a figure of 5.11–8.66 equivalent monolayers of Ga present at the threshold dose [61]. This leads the authors to speculate that the etch masking mechanism is the formation of a contiguous Ga layer that forms involatile compounds in fluorine-based chemistries and fails once the layer is breached via physical sputtering of the mask.

3.8 Suitability of Ga lithography for photonics

Based on the loss figure of $\sim 0.07 \frac{dB}{\mu m \cdot 10^{16} \frac{Ga}{cm^2}}$ in 10 μm wide, 220 nm thick Si waveguides [62], it is clear that using Ga masking for defining low-loss photonic structures is out of the question. However, their use in making gratings for localized, partially etched structures is more promising. For the grating coupler design discussed in the next chapter (Section 4.3), the additional loss introduced by using Ga lithography is

$$\begin{aligned}
\frac{\text{loss}}{\text{coupler}} &= \frac{\text{loss}}{\text{length} \cdot \text{dose}} \cdot \frac{\text{length}}{\text{coupler}} \cdot \text{grating duty cycle} \cdot \text{dose} \\
&= 0.07 \frac{dB}{\mu m \cdot 10^{16} \frac{Ga}{cm^2}} \cdot \frac{14 \mu m}{\text{coupler}} \cdot 0.5 \cdot 5 \times 10^{16} \frac{Ga}{cm^2} \\
&= 2.45 \frac{\text{dB}}{\text{coupler}} \\
&= 57\% \ \frac{\text{relative efficiency}}{\text{coupler}}.
\end{aligned}$$

Alternatively, a partial etch can be accomplished that would avoid even this excess loss with the following processing flow:

Pattern definition	Use any technique to make a mask that exposes both fully and partially etched structures
Ga Implantation	Implant couplers or other area that should be partially etched
Etch (Ga Selective)	Use one of the F-based etches described to fully etch the uncovered, unimplanted regions
Etch (Ga Unselective)	Use etching conditions that are not selective to Ga to break through mask and partially etch implanted regions (use a higher bias voltage and/or different gas chemistry, e.g. Cl_2-based Si etches)

In this way, the additional loss from the amorphized, Ga-rich layer could be eliminated, as the material is removed for etches greater than 30 nm for a 30 kV implantation voltage.

3.9 Conclusion

This work has demonstrated the use of FIB patterned Ga implanted etch masks for two different mixed mode silicon ICP-RIE chemistries with the objective of achieving nanoscale structures. Mask writing with the FIB is used here as a completely dry lithographic process for patterning of silicon for fluorinated plasma etching. This work measured the critical dose, the minimum areal Ga dose needed to achieve a given etched depth, for both the Pseudobosch and cryogenic silicon etch under similar plasma conditions. Under identical bias voltages in the same reactor, the etch chemistries each displayed markedly different linear dependencies on the critical dose, with the cryogenic etch showing more than 200 times the masking potential of the Pseudobosch for identical implantation dose. The threshold dose for masking, in contrast, was relatively insensitive to changes in both the implantation voltage and the etch chemistry. The milling aspect of both etches was similar due to comparable bias voltages. However, the addition of oxygen in the cryogenic etch may have contributed

to the increased mask resilience.

Despite the lower selectivity Pseudobosch etch as compared to the cryogenic etch, the slower etch rate is more precise and yields less undercut, enabling a smaller minimum feature size. Although each of the two etch chemistries were optimized for maximum pattern fidelity, the minimum feature size for the two etches was drastically different. The best a 1 μm deep cryogenic etch could achieve was a severely undercut 350 nm square pattern. Conversely, the Pseudobosch was demonstrated to faithfully mask a 30 nm Ga pattern with high anisotropy. Additionally, applications of Ga masks to grayscale and multilevel etching show promise as a way to achieve otherwise impractical geometries.

Although this work was limited to nanoscale patterning of silicon, the principle of using an implanted ion to act as an etch mask can be expanded to other ions and materials for other etch chemistries. Fundamentally, this technique can be generalized to using a focused ion beam to implant a pattern in a target material, so long as the implanted ion is not rapidly etched by ions in the plasma.

Chapter 4

Characterization of Silicon Waveguides and Resonators using Grating Couplers

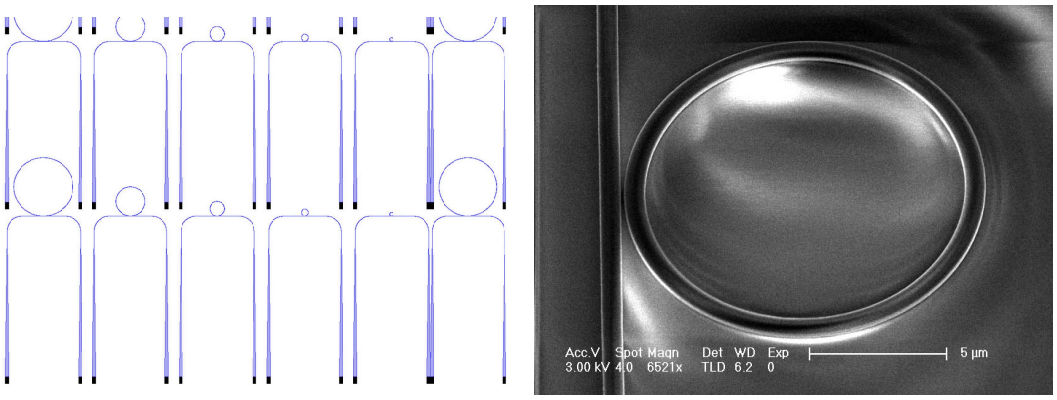
4.1 Introduction

In this chapter, we study compact silicon devices fabricated on SOI. These devices are suitable for passive optical elements or for incorporation in hybrid systems like those discussed in Chapter 5. The fabrication techniques discussed in earlier chapters are used to minimize loss in the structures. A compact, fully-etched grating coupler for that interfaces with optical fiber is demonstrated. This couple is used for dense arrays of low loss passive waveguides and ring resonators. Characterization of the grating coupler and cavity quality factor (Q) are determined using an automated test system.

4.2 Fabrication

We studied an array of bus waveguides with and without coupled microrings resonators. A typical layout motif was a 5×10 array of silicon microrings (Figure 4.1) with diameters of 12, 24, 50, 100, and 200 μm and a coupling gap between ring and bus waveguide ranging from 50nm to 500nm.

This motif can then be repeated in order to have multiple copies of a given coupling gap and ring diameter for statistical analysis of a given device geometry. We coupled to the bus waveguides using a fiber array polished at 8° from normal and controlled using an automated test setup that can move to different devices, maximize trans-



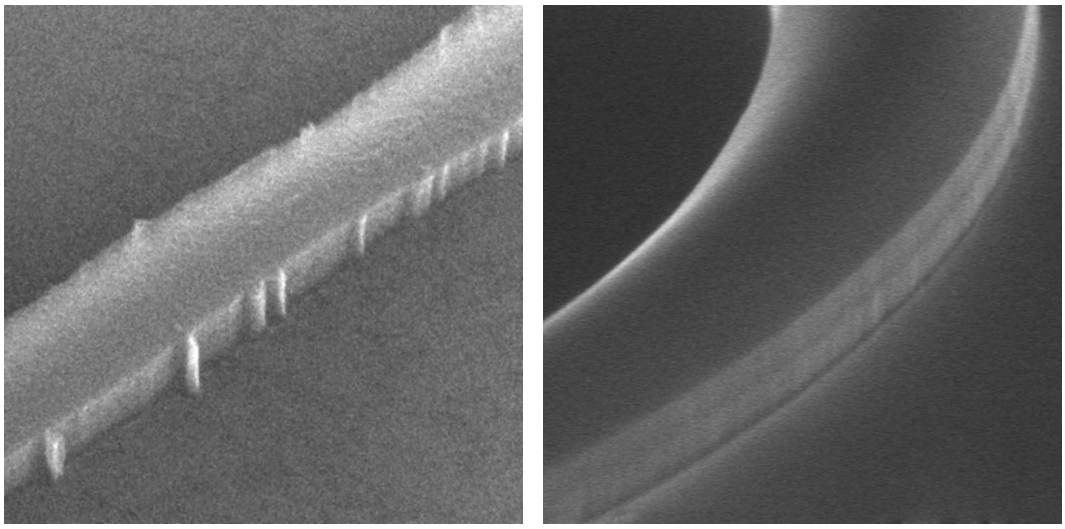
(a) Device Layout (b) SEM of Device

Figure 4.1. Typical Si ring-bus geometry. (a) Detail of ring resonator test devices consisting of a bus waveguide, ring resonator, and grating couplers. Largest ring is 200 µm in diameter. (b) Si ring-bus geometry after reflow and etching. Despite pattern swelling due to reflow, coupling gaps below 100nm are still possible.

mission, and obtain a device spectrum. Typical testing times were approximately 30 devices/hour.[1] The microrings were fabricated from silicon-on-insulator with a 220 nm device layer ($\langle 100 \rangle$, p-type, ρ =14-20 Ω·cm) and a 2 µm SiO_2 buried oxide layer (BOX). The resonators were defined using electron-beam lithography and resist reflow (recipe A.1.1), and C_4F_8:SF_6 ICP-RIE etch (recipe A.2.2). After initial measurement, the silicon surfaces were hydrogen passivated using repeated Piranha/HF treatments[64]. Immediately afterwards, a thin oxide layer was grown for 8 minutes in O_2 at 1000 °C followed by a 3-hour anneal in N_2 at 1000 °C, followed by a 1.5-hour slow cool down in N_2 from 1000 °C to 550 °C.

Despite the small minimum feature size of modern resists, the stochastic nature of the exposure and development process can lead to electrical device degradation through line edge roughness [65]. This nanometer-scale resist roughness is also a problem for photonic structures. First, roughness tends to be magnified during dry etching by projecting these detects into the waveguide sidewall a vertical striations, as pictured in figure 4.2(a). Because of the small size and high index contrast of Si

[1] See Guangxi Wang's thesis[63] for further details

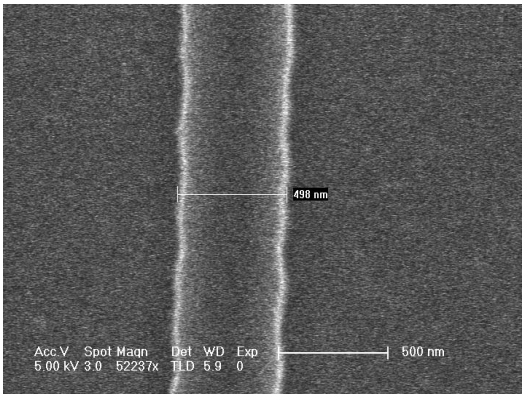


(a) No reflow (b) Reflow

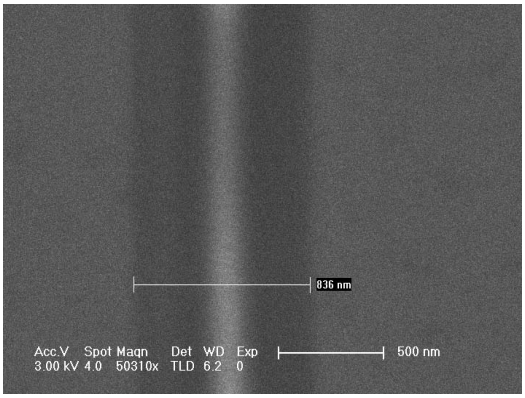
Figure 4.2. Reflow smoothing of an Si waveguide. Identical lithographically defined patterns show different amounts of roughness before and after reflow. Reflow results in improved performance due to lower scattering loss.

waveguides, a significant portion of the optical energy is concentrated at the sidewalls; the optical mode is thus highly sensitive to edge roughness. These surface problems can frequently be the limiting factor in the fabrication of high-Q devices [66].

In order to minimize this loss, patterns can be reflowed to allow surface tension to reduce the pattern roughness. Differences in the edge roughness are shown in figure 4.2. The etch is nearly identical to that used in earlier sections (3.3), ruling out etch-induced roughness as a possible cause instead of problems from the pattern. The reflow process does add the complication of increasing the sizes of patterns in the resist, as shown in figure 4.3. Compensation for reflow swelling was performed by uniformly shrinking the written pattern. For this design and reflow, a bias of -50 nm was found to produce the best grating performance. Further shrinking resulted in higher loss and increased Fabry-Perot-like modulation of the transmission spectra due to high reflection at the couplers. An SEM image of the reflowed gratings after etching is shown in figure 4.4.

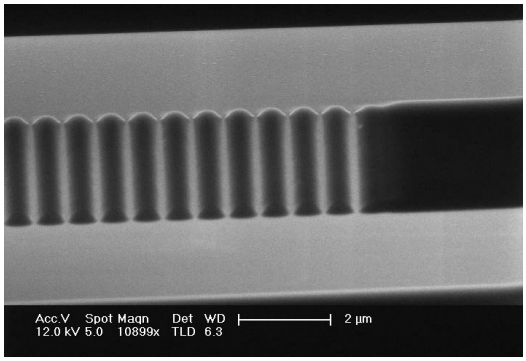


(a) No reflow, $w = 500$ nm

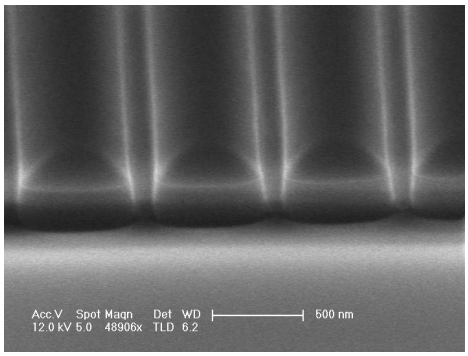


(b) Reflow, $w = 840$ nm

Figure 4.3. Pattern swelling due to reflow. A nominal 500nm pattern can swell more than 40% in relative size to 840 nm. Lithographic compensation is possible by defining a thinner initial pattern.



(a) Grating pattern in resist



(b) Transferred pattern

Figure 4.4. Pattern transfer of a grating using reflowed resist. Due to the thinned resist layer at pattern edges, the resultant Si etch profile is slightly angled due to erosion.

4.3 Grating Couplers

A key capability in building and characterizing silicon photonic devices is the ability to couple light into and out these devices from available testing equipment. As already noted, no technologically mature light source on silicon is available. Instead, optical fiber from the telecommunications industry is the prefer platform for getting light to these chips. However, the mode from these fibers is not well matched to Si waveguide dimensions, with a typical mode diameter of around 12 μm. Current coupling strategies include using inverse tapers [67], tapered fibers [68], and grating couplers [69]. Each of these approaches has different limitations. Inverse tapers require butt coupling to chip edge and therefore limit the device density due to routing of input and output waveguides or the inclusion of optical vias. Tapered fibers frequently suffer from poor phase matching to the Si waveguide mode, limiting the maximum power transfer. Grating couplers on SOI tend to be highly reflective and suffer from high substrate loss without bottom reflectors. Importantly, gratings can couple light in and out from anywhere on the chip. For this reason, we chose to use gratings to couple into and out of the bus waveguides.

Several designs exist for compact grating couplers on SOI that transform the confined Si mode into to a fiber mode with a Gaussian-like profile. However, highly efficient couplers are usually more processing intensive. These include partially-etched, nonuniform structures [70] and nonuniform depth gratings utilizing feature-size dependent ICP-RIE etching [71]. For ease of fabrication, we chose a fully-etched design with a simulated maximum efficiency of 49% at $\lambda_0 = 1550\ nm$ [72]. This design has a relatively simple geometry, as pictured in figure 4.5. It is essentially a 701 nm period, 50% duty cycle grating with a half period structure at the ends of the coupler to reduce reflectivity. The size of the grating structure (14 μm ×12 μm) is chosen to best match the fiber mode size. Additionally, the uniform pattern width improves pattern fidelity; the constant resist dimensions between gaps avoids any complications due to size-dependent swelling during reflow.

For the wafers tested here, the buried oxide layer thickness is not optimized for

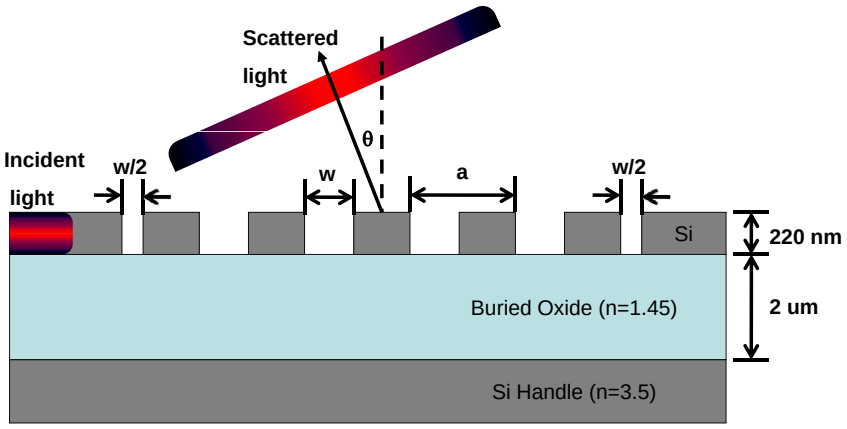
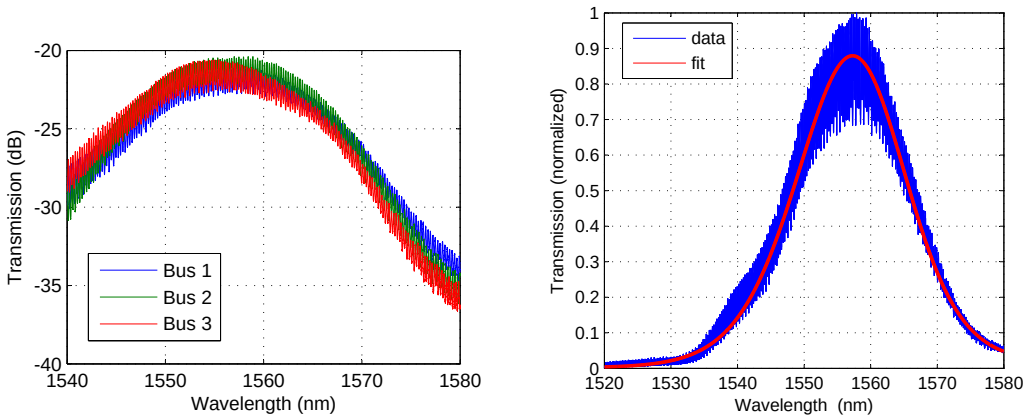


Figure 4.5. Grating Coupler Schematic. Incident light is scattered back toward the source at an angle θ away from the surface normal. Grating has a period a and gap width w as pictured. Original design has $a = 701$ nm, $w = 350$ nm, $\theta = 8°$, and 20 periods ($N = 20, L_{grating} \equiv Na = 14.02\ \mu m$). After [72]

this design. This reduces transmission by half of the optimized efficiency to 24.5%. This could be easily remedied by purchasing wafers with the appropriate oxide thickness. However, it does bring up an important design issue common to most grating couplers: sensitivity to the buried oxide thickness. The abrupt index change at the bottom SiO_2/Si interface causes a reflection, which can interfere constructively or destructively with the incident wave at the coupler. This can affect both the overall efficiency as well as the maximum useful bandwidth since this resonance condition is dependent on wavelength. Generally, the SiO_2 thickness is not a free parameter, but is chosen to maximize electrical device performance. Future off-chip couplers insensitive to this thickness are needed.

4.3.1 Grating Transmission

Wavelength scans from 1480 nm to 1580 nm were performed on an array of 30 bus waveguides in order to characterize the average performance of this design. Shown in figure 4.6 is the transmission spectrum of three bus waveguides, consisting of two



(a) Raw Data (b) Fit and Normalized

Figure 4.6. Bus waveguide transmission spectra. Broadness of data is due to Fabry-Perot resonance at grating couplers.

grating couplers on a bus waveguide of length $L_{total} = 1307$ µm.[2] The transmission spectrum has two main features: a slow grating response function modulated by a 1-2 dB rapid oscillation. This small oscillation appears noisy, is in fact due to a resonance in the transmission spectra of each device that is discussed shortly.

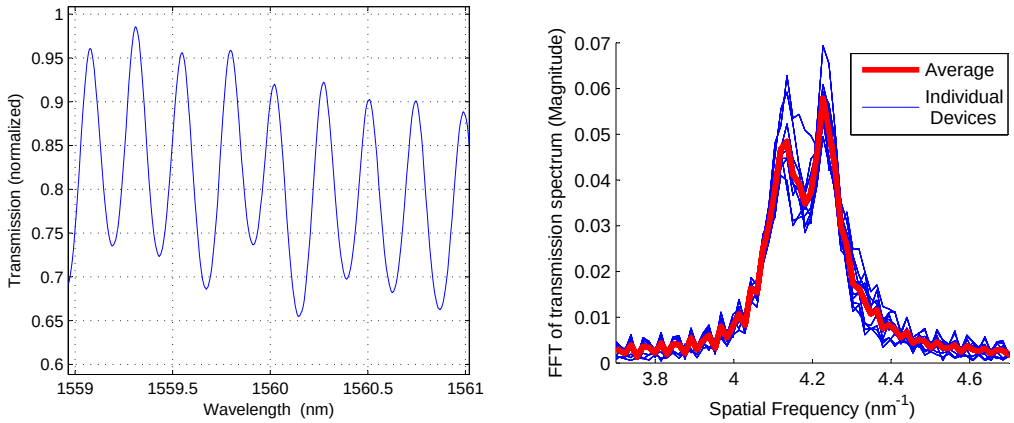
Data analysis was performed to fit the slowly-changing wavelength dependence of transmission and determine the device bandwidth. This data is summarized in table 4.1. These fitted curves were then subtracted from the original data to observe the rapidly-varying components of the spectra. Figure 4.7 shows the renormalized data, with the Fabry-Perot resonance made more apparent. The Fourier transform of this data shows resonance at $\Delta\lambda_{FSR} = 0.24\,nm$. Following the treatment of Sakai [73], we express n_{eff} as:

$$n_{eff} = \frac{\lambda^2}{2L_{total}\Delta\lambda} = 3.83 \tag{4.1}$$

$$n_{eff} \equiv n_{mode} + n_{dispersion} = n_{mode} - \lambda\frac{\partial n_{mode}}{\partial\lambda} \tag{4.2}$$

Equation 4.2 can be evaluated numerically via FEM simulations. Since the waveguide

[2]The bus consists of two linear tapers that go from 12 µm to 500 nm in width, and a 500nm width waveguide region: $L_{taper} = 500\ \mu m, L_{wg} = 307\ \mu m, L_{total} = 2L_{taper} + L_{wg} = 1307\ \mu m$



(a) Typical F-P Resonance

(b) FFT of Spectrum

Figure 4.7. Detail of a bus waveguide transmission spectrum showing the Fabry-Perot resonance. FFT of spectrum shows resonance occurs at $\frac{1}{\Delta\lambda_{FSR}} \sim 4.2\ nm^{-1}$

changes sizes along the length of the cavity, both n_{mode} and $\frac{\partial n_{mode}}{\partial \lambda}$ vary with position. Rather than try to rigorously calculate along the varying geometry, we can bound the possible values of n_{eff}. The largest possible value occurs at n_{eq} large (slab mode $n_{eq} = 2.87$) and $n_{dispersion}$ large (waveguide mode $\frac{\partial n_{mode}}{\partial \lambda} = -8.9 \times 10^{-4}\ nm^{-1}$). Similarly, the smallest possible value is at n_{eq} small (waveguide mode $n_{eq} = 2.49$) and $n_{dispersion}$ small (slab mode $\frac{\partial n_{mode}}{\partial \lambda} = -4.4 \times 10^{-4}\ nm^{-1}$). Thus the terms in equation 4.2 are

$$2.49 \leq n_{mode} \leq 2.87$$

$$0.69 \leq n_{dispersion} \leq 1.39$$

$$3.18 \leq n_{eff} \leq 4.28$$

the value calculated independently via equation 4.1 sits in between these values of n_{eff}. If you instead approximate the cavity as 1000 μm of the slab mode and 307 μm of the waveguide mode, we find $n_{eff} = 3.63$, which is close to the value calculated from the spectrum of $n_{eff} = 3.83$. We see that this underestimated value makes

sense, as we are neglecting the increasing $n_{dispersion}$ along the taper. Note that these values of n_{eff} exceed the bulk value for Si (n =3.481 at λ =1550nm), underscoring the highly dispersive nature of this waveguide.

4.3.2 Grating Reflectivity

The next cavity parameter of interest is the reflectivity, R. Assuming low loss, the cavity transmission is given by

$$\frac{I_{transmitted}}{I_{incident}} = \frac{(1-R)^2}{(1-R)^2 + 4R\,sin^2\,(\delta/2)}, \delta \equiv 2kL \tag{4.3}$$

The ratio of the maximum and minimum transmission is thus

$$\frac{I_{min}}{I_{max}} = \frac{(1-R)^2}{(1-R)^2 + 4R} = \frac{(1-R)^2}{(1+R)^2} \tag{4.4}$$

which can be rewritten as

$$R = \frac{1 - \sqrt{\frac{I_{min}}{I_{max}}}}{1 + \sqrt{\frac{I_{min}}{I_{max}}}} \tag{4.5}$$

Based on the observed extinction of 1.5–2dB, equation 4.5 predicts the reflectivity of the gratings to be R =0.08–0.12. These values are consistent with the simulated reflection coefficients of $R \leq 0.1$ ($R \leq 0.3$) for gratings with (without) the half period slot at the beginning [72].

Finally, we can use

$$\alpha = -\frac{1}{L} \ln \left(\frac{1}{R} \cdot \frac{\sqrt{I_{max}/I_{min}} - 1}{\sqrt{I_{max}/I_{min}} + 1} \right) \tag{4.6}$$

to estimate the loss. Using the the simulated value of $R \leq 0.1$ yields $\alpha_{bus} \leq$ 3.5 dB/cm. It is important to note that this α_{bus} is distinct from α_{ring}, since the bus includes the taper structure as well. However, we expect these values to be comparable.

	Simulated	Measured
Grating Characteristics		
Period (a)	701 nm	701 nm
Width (w)	350 nm	495 nm
Coupling Angle	10°	8°
Grating Performance		
Loss per coupler	-6 dB	$\leq$ -10 dB
3 dB Bandwidth	35 nm	(20$\pm$1.1) nm
1 dB Bandwidth	20 nm	(11$\pm$1.3) nm

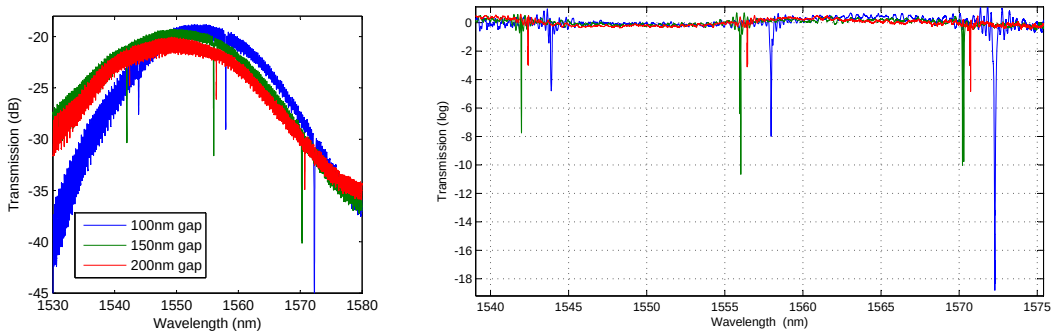
Table 4.1. Summary of measured grating coupler performance as compared to simulated values quoted in [72].

4.3.3 Grating Summary

Table 4.1 summarizes the observed grating performance as compared to quoted simulated values. Overall, the measured values are similar though significantly less efficient than expected. However, limitations of the setup prevented coupling at the correct angle, which may account for some of the discrepancy. Based on the calculated efficiencies in the paper, most of the excess loss relative to the ideal coupler could be explained by the narrower slots present in our fabricated sample. Unexplained then is the observation that wider slots produced more lossy grating. Further tests at the correct angle and using a more finely spaced paramber slot of the slot size is required fully characterize the fidelity of the simulations.

4.4 Ring Resonators

After characterizing the grating response, we moved on to look at the array of coupled ring-bus devices. Shown in figure 4.8(a) is the unmodified transmission. The nonuniform response of the bus waveguides makes determining the cavity Q difficult. As described earlier, the wavelength-dependent behavior of the grating coupler is removed first, followed the rapid oscillation which are removed by applying a notch



(a) Raw Data (b) Fit and Normalized

Figure 4.8. Combined Ring-bus waveguide transmission spectra for a ring with R=6 μm. Fit data in (a) show $\Delta\lambda_{FSR}$ =14nm, and thus n_eff =4.62

filter at the expected Fabry-Perot frequency. As shown in figure 4.8(b), this data processing is not enough to remove all of the unwanted structure of the transmission spectra. However, the resonances are usually distinct enough for numerical fitting routines to successfully identify and provide an estimate of the loaded quality factor Q_l.

4.4.1 Determining Q

Because of the remaining fluctuations in the spectra, a large number of resonances were measured in order to minimize any artificial changes in the measured Q_l. As shown in figure 4.9, the line shape fits are not perfect because of the remaining fluctuations from the bus waveguide. However, by measuring several resonances on copies of the same ring for different coupling gaps, we can minimize this fluctuation. Figure 4.10 summarizes these measurements of the loaded Q. As expected, the quality factor increases with increasing coupling gap. Based on the overall trend and the observation of several $Q_l \geq 10^5$ resonances at weak coupling, it is safe to assume that $Q_i \geq 10^5$. Based on this value, the waveguide loss can be estimated as $\alpha \leq \frac{\omega}{Qv_g} =$ 0.8 cm^{-1} = 1.84 dB/cm. This is still an order of magnitude higher than previously observed structures on a similar substrate [68]; however, the mode is much more

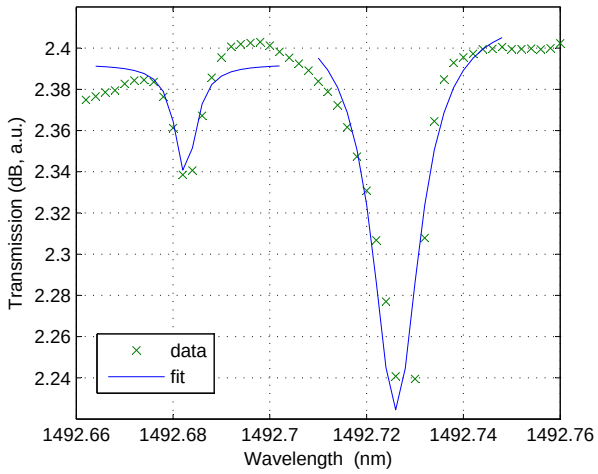


Figure 4.9. Example of Q fit to the noisy data. The quality factors of the left and right resonances were $Q = 1.4 \times 10^5$ and $Q_{sin} = 0.67 \times 10^5$, respectively The doublet splitting due to coherent backscattering is $\Delta\lambda = 44$ pm or $\Delta\nu = 5.5$ GHz. Ring radius of R=12 μm.

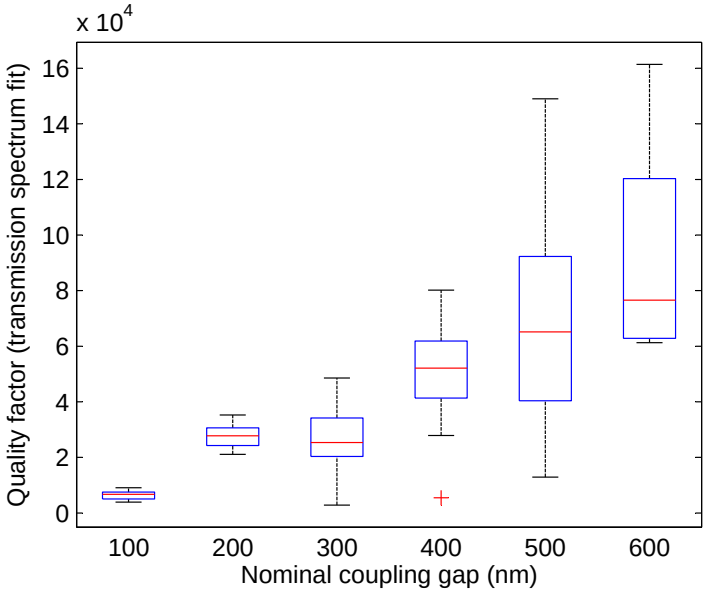


Figure 4.10. Ring resonator loaded quality factor for various coupling gaps. Box plot generated from fits to multiple transmission spectrum resonances.

strongly confined and overlaps with the lossy surfaces much more.

4.5 Summary

In this chapter, we investigated compact silicon devices fabricated on SOI. Fully etched grating couplers with losses $\leq$ -10 dB/couplers were shown, and the resonance structure of the bus waveguides was described. Resonators with $Q_i \geq 10^5$ and $\alpha \leq$ 1.84 dB/cm were also demonstrated. The ability to make these low loss Si structures is necessary for integration with III-V materials, which are discussed next.

Chapter 5

Hybrid Silicon Devices

5.1 Introduction

In this chapter we look at a promising geometry for active optical devices on silicon: the Si/III-V hybrid system. The preceding chapters demonstrated the feasibility of patterning Si with high quality that is suitable for monolithic integration. Here we examine InP based direct bandgap materials directly bonded on Si substrates. Supermode control of devices is described, which uses changing Si waveguide width to control modal overlap with the gain material. Hybrid Si/III-V, Fabry-Perot evanescent lasers are demonstrated, utilizing InGaAsP gain material. The lasing threshold current of 300-μm-long devices was as low as 24 mA, with a maximal single facet output power of 4.2 mW at 15°C, with single facet output power as high as 12.7 mW in longer devices. Finally, promising results of the supermode lasers over evanscent lasers are presented.

[1]

5.2 Supermode Device Geometry

The hybrid Si/III-V structure consists of an Si waveguide on SOI bonded to an InGaAsP wafer with mesa structures and metallization [75]. The modal overlap is controlled by the waveguide along the length of the device. Fixed width devices are termed evanescent hybrid structures [75], while variable width devices are termed su-

[1] Portions of this chapter are based on work done with Xiankai Sun, Avi Zadok, Ken Diest, Ali Ghaffari, and Marina Leite[74]

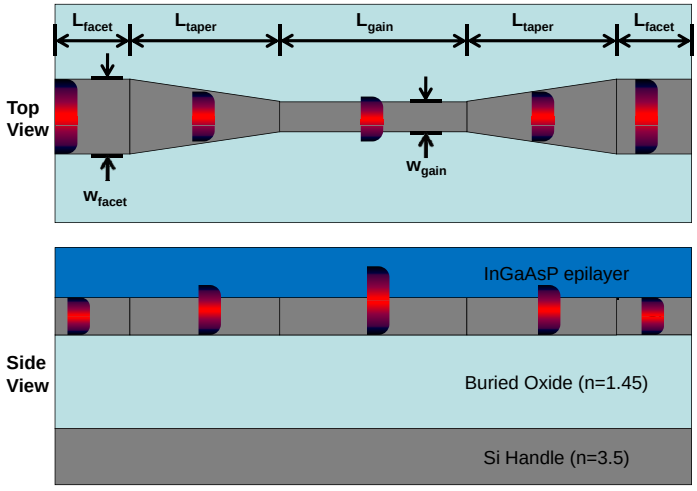


Figure 5.1. Schematic of supermode evolution

permode hybrid structures after the coupled mode formalism introduce by Yariv [7]. Changing the Si waveguide width causes the mode to couple from the Si waveguide into the III-V waveguide as the propagation constant of the Si structure is changed [76]. Figure 5.1 shows the a schematic of the Si waveguiding structure for our tested devices. In purely evanescent devices, $w_{facet} = w_{gain} \in [0.8\mu m, 1.5\mu m]$. Supermode devices have values of $w_{facet} \in [1.2\mu m, 1.5\mu m]$ and $w_{gain} \in [0.5\mu m, 0.9\mu m]$, with section lengths of L_{facet}=350 μm, L_{taper}=200 μm, and L_{gain}=400 μm.

5.3 Fabrication

5.3.1 Pattern Definition

In order to efficiently test and compare evanescent to supermode [76] structures, a parameter sweep of Si waveguides were written. Variations in the mask were generated via L-Edit code[2]. Corresponding mask sets were generated for the various ion implantation, mesa formation, and metallization steps done after the Si waveguiding etching and wafer bonding. The masks were design so that different versions of the mask could be used interchangeably. Finally, each photomask contained appropriate

[2] An example of this code is found in Appendix B

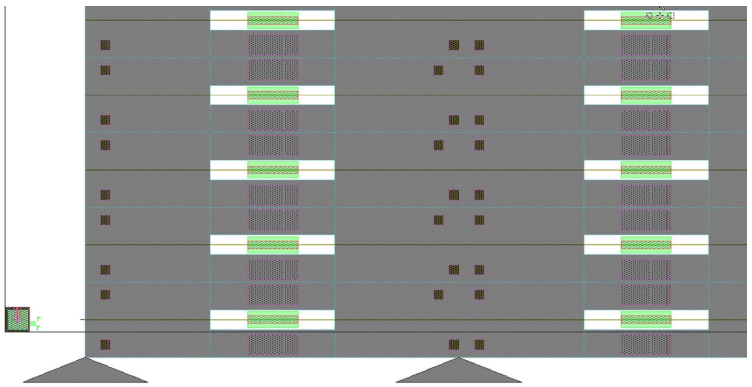


Figure 5.2. Portion of a typical a 2×5 array of devices. Cleave marks (triangles) on the Si layer separate individual copies of each device, while different parameters are changed in the orthogonal direction.

structures for secondary alignment in the electron beam lithography system, so that a speculative design could be tried without having a separate mask made for the layer.

Finally, to minimize the likelihood of missing devices due to a bonding epilayer failure or other localized defect, the parameter sweep design was kept small enough to repeat the pattern several times on a typical 1 cm × 1 cm wafer. This also minimized any bias in wafer location when making performance comparsions. Any systematic changes in the quality of the bonding or other parameters is likely to be slowly varying with location, as a abruptly changing one would probably lead to device failure.

5.3.2 Si Waveguides

Waveguide patterns were defined on silicon-on-insulator wafers with an Si layer thickness of 900 nm on top of a 2 sμm buried oxide layer using electron beam lithography without reflow(recipe A.1.1), and a C_4F_8:SF_6 ICP-RIE etch (recipe A.2.2). An example of these waveguides is found in figure 5.3. The waveguides were partially etched so that a thin layer of ∼100 nm of Si remained. This was done to improve device yield during the bonding step. The applied force during wafer bonding caused cracking at the waveguide Si/SiO_2 interface using a fully etched design. This modification does not significantly alter the the properties of the hybrid optical mode due to the small thickness remaining, but is enough to provide mechanical stability to the waveguide

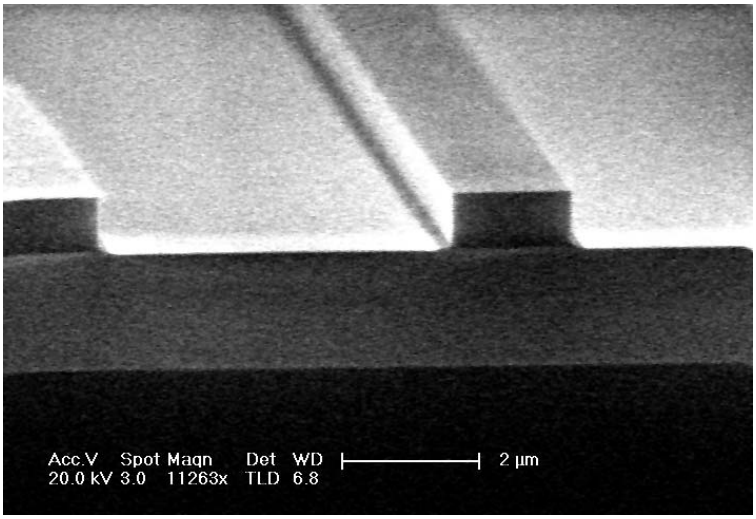


Figure 5.3. Isometric view of the cleaved facet of a fully etched Si Waveguide. A small foot is visible at the edge of the waveguide due to a slightly slower etch rate at that sidewalls.

ridges.

5.3.3 Bonding

The complete bonding procedure is described in detail in section 2.6.2. For earlier designs, we used a 10-nm-thick oxide bonding interface layer grown on the patterned SOI to enhance the bonding strength. As we improved our bonding process, we moved to direct bonding with O_2 plasma activation. Our procedure included cleaning in a 3:1 H_2SO_4:H_2O_2 mixture (10 min at 170 °C) that can aid in surface passivation [64].

5.3.4 InGaAsP Waveguides

Evanescent devices and some hybrid design do not require a III-V guiding structure to be formed; gain guiding and the high index of the Si waveguide is enough to form a hybrid mode. However, further modal confinement can be accomplished by forming a ridge waveguide in the III-V. This can also improve current characteristics of the device by shortening the length to the bottom-side contact in the thin n-side contact layer. Although the dimensions of the III-V waveguide are achievable using photolithography, this step requires a second electron beam lithograph step in

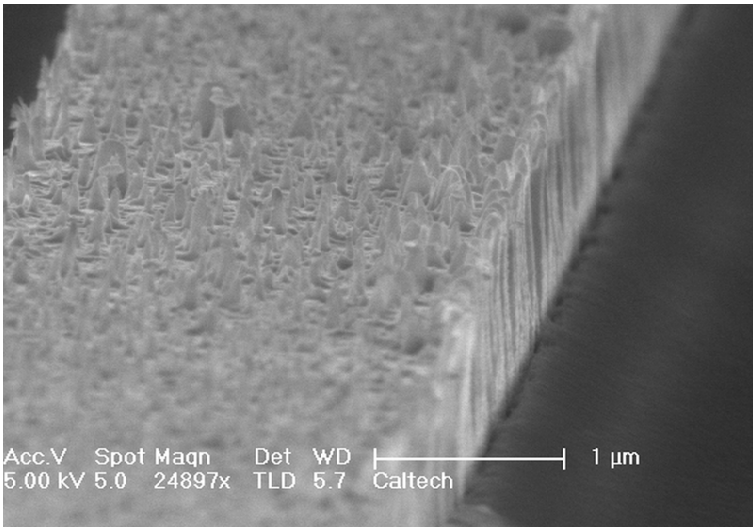


Figure 5.4. View along etched sidewall of III-V waveguide. The spikes in the metal mask are caused by partial mask failure during the etch.

order satisfy the narrower alignment tolerances. Alignment was done using etched structures on the exposed Si surface outside of the bonding area defined at the same times as the Si waveguide. A bilayer PMMA process (recipe A.1.5) was used as a liftoff layer for mask metallization. For etching the ridge waveguide, we used a mixed mode $CH_4/H_2/Cl_2$ etch for optimized for InP/InGaAsP materials (recipe A.2.4). A metal mask is preferred for this etch for its high selectivity. The bias voltage is must higher than in the silicon mixed mode SF_6:C_4F_8 etch, so a tough mask is required to minimize erosion that can lead to roughness and thus scattering. For the metal, we choose to use the same Cr/AuZn/Au metallization that is used for the broad area contact, making it a self aligned procedure. Figure 5.4 shows a III-V waveguide etched using this procedure.

5.3.5 Planarization

In order to make contacts on the narrow III-V waveguide, planarization was required (recipe A.1.6). We used PI-2562, a curable polyimide material used in other III-V laser structures that did not cause significant loss [77]. The lower degree of planarization of this material required 2-3 coatings of polyimide to achieve coverage of the III-V

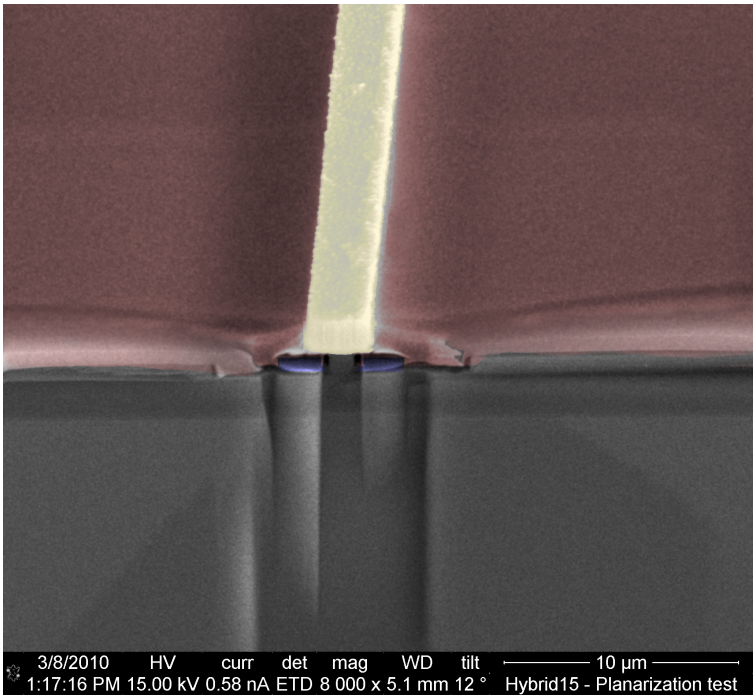


Figure 5.5. Cross sectional view of planarization of a hybrid waveguide. The contact (gold), PI-2562 (red), and failed 110 nm n-InP layer (blue) are visible on the SOI substrate (uncolored).

ridge and ensure that not shorting would occur at an incompletely covered area. Once covered, the structure was etched back (recipe A.2.5) to expose the metal contact for second metallization. Shown in figure 5.5 is a cross section of the bonded waveguide after etch back. In the figure, we see the exposed contact surrounded by cured PI-2562. However, the 110 nm n-InP layer has failed during the planarization process, and remain in the void left by the etched trenches on either side of the Si waveguide. It is unclear when the failure occurred, but a likely point in the process is during the curing bake, when any thermal expansion mismatch between the materials could cause the thin membrane to be breached. An alternative structure, simulated in COMSOL, is pictured in figure 5.6. This would add to the mechanical support of the III-V membrane while minimizing negative effects to the modal structure.

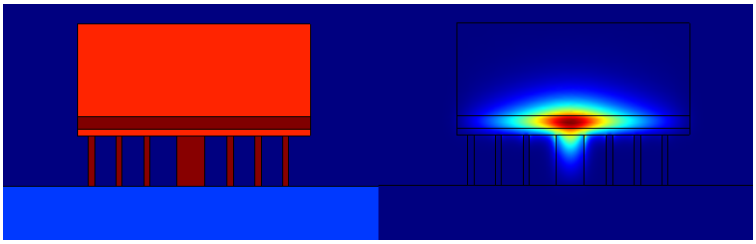


Figure 5.6. FEM simulation of a mechanical support structure for the III-V membrane. The mode is not influenced by the adjacent narrow silicon veins.

5.3.6 Contacts and Wet Etching

In the results discussed below, we used a simpler III-V processing flow. First, following the bonding, the InP substrate was removed by HCl wet etching. Then, a 80-μm-wide mesa structure was formed in the InGaAsP layers, centered above the Si waveguide, through photolithography and three-phase wet etching, down to the n-InP contact layer (see table 5.1). The etching solutions were (a) 1:1:10 mixture of H_2SO_4:H_2O_2:H_2O (p-InGaAs layer, 60 s), (b) 2:1 mixture of HCl:H_2O (p-InP layer, 30 s), and (c) 1:1:10 mixture of H_2SO_4:H_2O_2:H_2O (quaternary layers, 4 min). Before depositing metal contact, proton implantation was performed to limit the current flow laterally to a 5-μm-wide channel directly above the Si waveguide. The implantation dosage and proton energy were 5×10^{14} cm^2 and 170 keV, respectively. After implantation, metal contacts were deposited. We evaporated alloys of Cr/AuZn/Au (top, p-InGaAs layer) and Cr/AuGe/Au (bottom, n-InP layer) for these contacts. Finally, the Si substrate was lapped down to a thickness of 50 μm, and device bars were cleaved and annealed at 410°C for 10 s to assists in the diffusion of Zn from the p-side metal contact into the p-side layers. Figure 5.7 shows a scanning electron microscope image of the device's cross section.

Layer	Material	Thickness (nm)	Bandgap (eV)	Doping (cm^{-3})
p-side contact layer	p-$In_{0.53}Ga_{0.47}As$	200	0.77	$p > 10^{19}$
Upper cladding layer	p-InP	1500	1.34	$p = 10^{18} \rightarrow 5 \times 10^{17}$
Separate confinement layers	InGaAsP	40	1.08	undoped
	InGaAsP	40	0.99	undoped
Quantum wells (1% compressive strain)	InGaAsP (×5)	7	0.83	undoped
Barriers (0.3% tensile strain)	InGaAsP (×4)	10	0.99	undoped
Separate confinement layers	InGaAsP	40	0.99	undoped
	InGaAsP	40	1.08	undoped
n-side contact layer	n-InP	110	1.34	$n = 10^{18}$
Superlattice	n-InGaAsP (×2)	7.5	1.13	$n = 10^{18}$
	n-InP (×2)	7.5	1.34	$n = 10^{18}$
Bonding layer	n-InP	10	1.34	$n = 10^{18}$

Table 5.1. InGaAsP Wafer Epilayer Structure

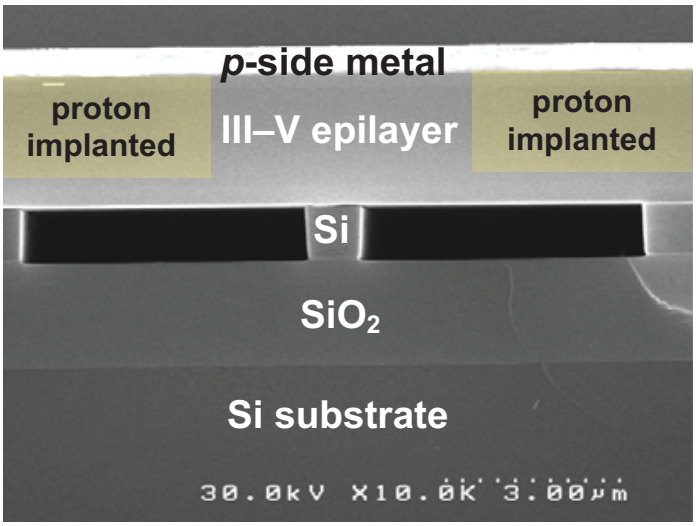
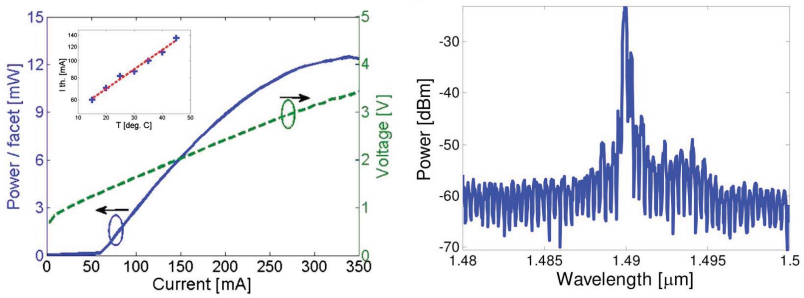


Figure 5.7. SEM view of a cleaved end facet of a fabricated hybrid Si/III-V laser. This is a close-up at the center Si waveguide region. Approximate proton implanted regions are superimposed on the image for illustration.



(a) L-I-V Curve (b) Spectrum

Figure 5.8. L-I-V curve and spectrum of a 960-μm-long laser operating in CW mode at 15 °C. Courtesy of Xiankai Sun.

5.4 Measurements

5.4.1 Electrically pumped evanescent hybrid lasers

Using the above fabrication procedure, we were able to make hybrid lasers capable of continuous wave operation. Figure 5.8(a) shows the output power and device voltage versus current of a 960-μm long device, mounted on a thermoelectric cooler at 15°C. The turn-on voltage was 0.8 V, and the lasing threshold voltage V_{th} was 1.3 V. The threshold current I_{th} was 60 mA, corresponding to a threshold current density J_{th} of 1.25 kA/cm^2. The maximum power output P_{max} from a single facet was 12.5 mW, and the differential slope efficiency η_{diff} for a single facet was 8.4%. The inset of Fig. 5.8(a) shows I_{th} as a function of temperature. Figure 5.8(b) shows the laser spectrum, whose central wavelength was 1490 nm. The measured values of η_{diff} and α_i correspond to an internal quantum efficiency of 0.54. J_{th} of 1-1.5 kA/cm^2 were obtained for numerous devices, having lengths between 300 and 1500 μm. I_{th} of the 300-μm-long devices was 24 mA at 15 °C, with P_{max} of 4.2 mW. J_{th} and V_{th} of the devices are about 35% lower than those of previously reported F-P hybrid Si/AlGaInAs lasers [78]. At the same time, the devices' P_{max} is 70% higher, and their η_{diff} is 30% higher.

Si waveguide type	w_{facet} (μm)	w_{gain} (μm)	Γ_{QW}^{eff}	V_{th} (V)	J_{th} (kA·cm^{-2})	η_{ex}
Supermode	1.2	0.6	0.0388	3.0	1.47	1.06%
Supermode	1.2	0.7	0.0264	4.0	2.20	1.88%
Supermode	1.2	0.8	0.0189	5.0	3.85	2.31%
Supermode	1.2	0.9	0.0155	9.0	11.7	1.50%
Evanescent	1.2	1.2	0.0123	11.0	11.9	0.36%

Table 5.2. Test results of supermode and evanescent lasers. Courtesy of Xiankai Sun.

5.4.2 Comparison of supermode hybrid lasers to evanescent hybrid lasers

While supermode device were made along with the evanescent structures in the previous section, their characteristics were worse than the evanscent counterparts, partially due to design and fabrication issues. In future runs, we had problems reproducing the same device quality, but were able to try a wider range of the device parameters in order to find more optimal supermode designs. While the result in this section are not for continuous wave operation, they point to an improve in device characteristic when using supermode designs. Table 5.2 summarizes test results comparing supermode to traditional evanescent lasers. The threshold behavior of the hybrid lasers is expected: a higher concentration in the quantum well region (Γ_{QW}^{eff}) results in a lower threshold current density (J_{th}) and voltage (V_{th}), as expected from the threshold gain condition [7]. The behavior of the slope efficiency, η_{ex}, is unexpected; rather than decreasing monotonic with increased threshold, a local maximum is attained. Further analysis of this behaviour with respect to the modal profile suggests that there is additional loss at the bonded interface, pointing to the need for further characterization and possible improvement of the bonding process.

5.5 Conclusion

In this chapter we investigated Si/III-V hybrid structure, which is a strong candidate for integration into existing microelectronics platforms. While the results are promising, further work into maximizing the output from these devices must be done in order to achieve the required efficiency and size constrains of a realistic optic source for on-chip interconnects. However, processing techniques for integrating these materials and making these structures continue to rapidly improve, making the likelihood that Gordon Moore's idea of "cramming more components onto integrated circuits" will extend to optical components in the near future.

Appendix A
Fabrication Recipes

A.1 Resist and Planarization

A.1.1 ZEP-520A Resist Process

Used for waveguide and other nanostructure definition for plasma etching. Not suitable for liftoff.

Pre-spin Oxide removal	Buffered HF dip for 10s, Rinse in DI water 3x; helps with resist adhesion
Dehydration Bake	Hotplate at 180 °C for ≥1min
Spin Coating	static dispense, hold for ∼15s, spin at 5000rpm for 60s
Pre-bake	Hotplate at 180 °C for 3min
Exposure	$\sim 190 \frac{\mu C}{cm^2}$ on EBPG-5000+ at 100kV, typical beam current of 1nA
Develop	ZED-N50 (n-Amyl Acetate) for 3min
Rinse	ZMD-D (MIBK) for 10s
Reflow Bake	Oven bake, 165 °C for 3mins on a glass slide/dish for thermal insulation
Etch	Dry plasma etch as detailed in A.2
Solvent Removal	PG-Remover (NMP) soak in a covered dish at 50 °C for ≥10min; Rinse IPA, Acetone, IPA
Acid Removal	Piranha clean, see recipe A.3.1
Ga-doped resist removal	O_2 plasma descum for 15min or until clean

A.1.2 Shipley 1813 Resist Process

Used for metal liftoff for large contacts on Si/III-V hybrid structures.

Dehydration Bake	Hotplate at 95 °C for ≥5min
Spin Coating	Static dispense, spin at 4000rpm for 90s
Pre-bake	Hotplate at 95 °C for 6min
Exposure	8s on Karl Suss MA-6
Develop	MF319 for 45s
Rinse	IPA, followed by N_2 dry
Descum	O_2 plasma descum for 1min (optional)
Evaporation	Desired material for contact
Liftoff	Acetone soak in a covered dish; Rinse IPA, Acetone, IPA

A.1.3 AZ 5214 Resist Process

Used as an etch mask for Si_3N_4 ICP-RIE etching.

Dehydration Bake	Hotplate at 95 °C for ≥5min
Spin Coating	Static dispense, spin at 5000rpm for 40s
Pre-bake	Hotplate at 95 °C for 90s
Exposure	5s on Karl Suss MA-6
Develop	MIF300 for 90s
Rinse	Water, followed by N_2 dry
Hard bake	Hotplate at 115 °C for ≥90s
Descum	O_2 plasma descum for 1min (optional)

A.1.4 nLOF 2070 Resist Process

Used for metal liftoff of thick indium contacts for bonding.

Solvent Clean	Acetone, IPA, O_2 plasma descum for 1min
Dehydration Bake	Hotplate at 115 °C for ≥2min
Spin Coating	Static dispense, spin at 1000rpm for 30s, 500rpm/s ramp
Pre-bake	Hotplate at 110 °C for 2min
Exposure	0.8s on Karl Suss MA-6 (25mW/cm^2, 405nm)
Post Exposure Bake	Hotplate at 115 °C for 2min
Develop	MIF300 for approximately 4min 15s
Rinse	Water, followed by N_2 dry
Hard bake	Hotplate at 115 °C for 2min
Evaporate	Indium
Liftoff	Microstrip 2001 at 80 °C for ≥1 hour
Rinse	IPA, followed by N_2 dry
Prebond cleaning	4:1 H_2O:HCl for 1min

A.1.5 Bilayer PMMA Resist Process

Used for metal liftoff for small contacts and the metal mesa mask for Si/III-V hybrid structures.

Dehydration Bake	Hotplate at 170 °C for ≥3min
First Coating	Use 495k/A11 PMMA, spin at 4500rpm for 60s
Pre-bake 1	Hotplate at 170 °C for 5min
Second Coating	Use 950k/C2 (or A2) PMMA, spin at 2500rpm for 60s
Pre-bake 2	Hotplate at 170 °C for 5min
Exposure	$\sim 1700 \frac{\mu C}{cm^2}$ on EBPG-5000+ at 100kV, typical beam current of 10nA
Develop	1:3 MIBK:IPA for 45s
Rinse	IPA for 30s, followed by N_2 dry
Descum	O_2 plasma descum for 1min
Evaporation	Desired material for contact
Liftoff	Acetone soak in a covered dish; Rinse IPA, Acetone, IPA

A.1.6 PI-2562 Planarization Process

Used for metal liftoff for small contacts and the metal mesa mask for Si/III-V hybrid structures.

Dehydration Bake	Hotplate at 95 °C for ≥5min
Spin Coating	Static dispense PI-2562, spin at 500rpm for 3s, followed by 30s at final spin
Spin Thickness	2krpm = 3.1μm, 3krpm = 2.5μm, 4krpm = 1.8μm, degree of planarization = 55%
Pre-bake	Hotplate at 120 °C for 6min
Cure	Ramp up to 200 °C, rate of 4 °C/min Hold 200 °C, 120min Ramp down to room temperature, rate of 2.5 °C/min

A.2 Plasma Etching

All recipes are specified for an Oxford PlasmaLab 380 with 6 inch tooling. Tranferring to another system would require rescaling of parameters to account for differences in chamber size (gases) and electrode/inductor size (CCP/ICP powers).

A.2.1 Pulse-mode SF_6/C_4F_8 etch for silicon (Bosch process)

Used for deep Si etching and MEMs structures.

Etch Parameters		
Etch Rate	Si	3.6μm/min
Wafer	Temperature	15 °C
	He backing	10 T
	Stage height	20 mm
Etching Step		
Gas	SF_6	160 sccm
	C_4F_8	0 sccm
	Chamber pressure	20 mT
Plasma	CCP	30 W
	ICP	1750 W
	Time	15 s
Deposition Step		
Gas	SF_6	0 sccm
	C_4F_8	140 sccm
	Chamber pressure	20 mT
Plasma	CCP	30 W
	ICP	1750 W
	Time	10 s

A.2.2 Mixed-mode SF_6/C_4F_8 etch for silicon (Pseudobosch)

Used for etching Si waveguides and nanostructures.

Etch Parameters		
Etch Rate	Si	260-300nm/min
Gas	SF_6	33 sccm
	C_4F_8	67 sccm
	Pressure	10 mT
Plasma	CCP	10-20 W
	ICP	1200 W
	Voltage	5-75 V
Wafer	Temperature	15 °C
	He backing	10 T
	Stage height	20 mm

A.2.3 Cryogenic SF_6/O_2 etch for silicon

Used for high aspect ratio Si micro- and nanostructures. Good thermal stability is required for proper execution. Longer etches require hold steps with no plasma in order to keep wafer from warming up and having passivation fail.

Etch Parameters		
Etch Rate	Si	1.1μm/min
Gas	SF_6	70 sccm
	O_2	5 sccm
	Chamber pressure	10 mT
Plasma	CCP	5-10 W
	ICP	900 W
	Voltage	15-60 V
Wafer	Temperature	-120 °C
	He backing	10 T
	Stage height	20 mm

A.2.4 Mixed-mode $CH_4/H_2/Cl_2$ etch for InP/InGaAsP materials

Used for III-V bonded wafer after wet chemical etch to remove handle wafer. A metal mask was used both for its high selectivity and because it allows for a self aligned process with later steps. For other applications, a nitride mask is preferred over an oxide mask in order to reduce mask erosion defects and faceting.

Etch Parameters		
	intrinsic InP	1200nm/min
Etch rate	p-InP/InGaAsP	550nm/min
Gas	CH_4	16 sccm
	H_2	28 sccm
	Cl_2	32 sccm
	Chamber pressure	4 mT
Plasma	CCP	180 W
	ICP	2200 W
	Voltage	180-200 V
Wafer	Temperature	60 °C
	He backing	0 T (off)
	Stage height	20 mm

Occasionally, a pre-cleaning is necessary if the etched area appears rough or grassy. A brief cleaning plasma can be employed immediately before the etch.

Pre-clean Parameters		
Time		1 min
Gas	SF_6	50 sccm
	Chamber pressure	10 mT
Plasma	CCP	50 W
	ICP	1000 W
Wafer	Temperature	60 °C
	He backing	0 T (off)
	Stage height	20 mm

A.2.5 Polyimide Etch

Used for etching PI-2562 to expose contacts.

Etch Parameters		
Etch Rate	PI-2562	540-560nm/min
Gas	SF_6	5 sccm
	O_2	30 sccm
	Strike pressure	20 mT
	Chamber pressure	5 mT
Plasma	CCP	40 W
	ICP	1000 W
	Voltage	10 V
Wafer	Temperature	15 °C
	He backing	10 T
	Stage height	20 mm

A.2.6 Oxygen Plasma Activation

Used prior to wafer bonding Si/III-V hybrid structures.

Etch Parameters		
Duration		5 minutes
Gas	O_2	60 sccm
	Chamber pressure	50 mT
Plasma	CCP	8 W
	ICP	1000 W
	Voltage	55 V
Wafer	Temperature	20 °C
	He backing	20 T
	Stage height	20 mm

A.2.7 Typical Etch Chemistries

List of etch chemistry for various materials of interest. Drawn from personal etch recipes and Oxford Plasma Technologies datasheets.

Material	Gases	Typical reaction products
Si	SF_6, C_4F_8 SF_6, O_2 HBr, Cl_2, HI	SiF_4 SiF_4, SiO_xF_y $SiCl_4$, $SiBr_4$, SiI_4
SiO_2	C_4F_8, O_2	SiF_4, CO, CO_2
InGaAsP	CH_4, H_2 Cl_2, BCl_3	$In(CH_3)_3$, PH_3 Ga_2Cl_6, $AsCl_3$, HCl
Polymer (PMMA/ZEP)	O_2, C_4F_8, CF_4	H_2, H_2O, HF, CO, CO_2

A.3 Wet Etching

A.3.1 Piranha clean for surface passivation/bonding

Used prior to wafer bonding Si/III-V hybrid structures or growing a passivating oxide layer on Si devices. Substitution: Nanostrip if separate sulfuric acid and hydrogen peroxide is unavailable.

Solvent Clean	NMP soak, IPA, Acetone, IPA
Pre-heat Acid	Place 30mL of H_2SO_4 (97%) in a glass beaker on a hotplate at 165 °C for 10 minutes
Add Peroxide	Add 10mL of H_2O_2 (30%) to acid beaker slowly to minimize violent reaction
Introduce Sample	Place piece mounted on Teflon holder into beaker. Hold 10mins. (Use this step for Si sample only)
Water Rinse	Rinse sample 3x in DI water beakers for 30s each
Oxide Removal	Place sample in 10:1 HF for 10s; rinse sample 3x in DI water beakers for 30s each.
Plasma Activation	Use a commercial O_2 plasma at ambient pressure; alternatively, use an ICP-RIE plasma (A.2.6).

A.3.2 KOH and HCl etching for Si/Indium

KOH used prior to release silicon nitride membranes for wet cell project. The indium gaskets are also etched in KOH, but at a much slower rate than the Si wafer. Lower temperature seems to have better selectivity. Brief HCl dip is used to remove InO_x before bonding.

Etch Parameters		
KOH (30%, 55 °C) Etch Rate	In	75-80nm/hr
	Si	1300nm/hr
HCl (10%, 15 °C) Etch Rate	In	75-80nm/hr

Appendix B
L-Edit Code for Layout Generation

This is an example program for generating the hybrid III-V/Si waveguide structures with all necessary mask layers.

```
module hybrid01_code
{
#include <stdlib.h>
#include <math.h>
#include <string.h>
#include <stdio.h>
#include "ldata.h"

/* This sets the resolution of the taper */
#define TMAX 800
#define TMAX2 1600
/* number of alignment marks */
#define ALIGN_SIZE 4
#define MARK_DIM 200
/* Bounding box parameters */
#define BOX_H 10000
#define BOX_W 10000
#define BOX_T 500
#define MARGIN 800
#define XPERIOD 1600
#define YPERIOD 300

/* proton mask parameters */
#define W_PROTON          5
#define W_PROTON_WINDOW 30
#define W_PROTON_EDGE     0

/* Si waveguide parameters */
#define W_SI_PASSIVE     1.8
#define D_W_SI_PASSIVE -0.2
#define W_SI_ACTIVE      1.8
#define D_W_SI_ACTIVE  -0.2
#define L_SI_PASSIVE     450
```

```
#define L_SI_ACTIVE      200
#define L_TAPER          200
#define NUMWG              7

/* III-V parameters */
#define W_MESA           80
#define L_MESA          500
#define W_P_CONTACT      30
#define W_N_CONTACT      80
#define CONTACT_OFFSET   20

/* Draw parameters */
#define DRAW_P           1
#define DRAW_N           1
#define DRAW_MESA        1
#define DRAW_ION         1
#define DRAW_OPTO        1
#define DRAW_OPTOALIGN   1


 /* TODO: Put local functions here. */
LPoint MyPoint_Set( double x, double y ) {
 return LPoint_Set( LC_Microns(x), LC_Microns(y));
}

LObject MyBox_New( LCell cell, LLayer layer, LPoint *Box) {
 return LBox_New(cell, layer, Box[0].x,Box[0].y,Box[1].x,Box
     [1].y);
}

void BoundingBox( LCell cell, LLayer layer, double height,
   double width, double thickness) {

 LPoint Box[2], Corners[4], Align[4], Align_offset[4], offset
     ;
 Box[0]=MyPoint_Set(-1000,-1000);
 Box[1]=MyPoint_Set(thickness,height);
 Box[1]=LPoint_Add(Box[0],Box[1]);
 LBox_New(cell, layer, Box[0].x,Box[0].y,Box[1].x,Box[1].y);

 offset=MyPoint_Set(0,0);
 Corners[0]=LPoint_Add(Box[0],offset);
 Corners[1]=Corners[0]; Corners[2]=Corners[0]; Corners[3]=
     Corners[0];
 offset=MyPoint_Set(-MARGIN,-MARGIN);
```

```
Corners[0]=LPoint_Add(Box[0],offset);
offset=MyPoint_Set(-MARGIN,height+MARGIN);
Corners[1]=LPoint_Add(Box[0],offset);
offset=MyPoint_Set(width+MARGIN,height+MARGIN);
Corners[2]=LPoint_Add(Box[0],offset);
offset=MyPoint_Set(width+MARGIN,-MARGIN);
Corners[3]=LPoint_Add(Box[0],offset);

Box[0]=MyPoint_Set(-1000,-1000-thickness);
Box[1]=MyPoint_Set(width,thickness);
Box[1]=LPoint_Add(Box[0],Box[1]);
LBox_New(cell, layer, Box[0].x,Box[0].y,Box[1].x,Box[1].y);

Box[0]=MyPoint_Set(width-1000,-1000-thickness);
Box[1]=MyPoint_Set(thickness,height);
Box[1]=LPoint_Add(Box[0],Box[1]);
LBox_New(cell, layer, Box[0].x,Box[0].y,Box[1].x,Box[1].y);

Box[0]=MyPoint_Set(-1000+thickness,height-1000-thickness);
Box[1]=MyPoint_Set(width,thickness);
Box[1]=LPoint_Add(Box[0],Box[1]);
LBox_New(cell, layer, Box[0].x,Box[0].y,Box[1].x,Box[1].y);

 //Alignment marks

 //Define Corners
 double xsize, ysize, xsize_offset;
 xsize=width;
 xsize_offset=1000;
 ysize=height;

 //define Mark
 Align[0]=MyPoint_Set(MARK_DIM,MARK_DIM);
 Align[1]=MyPoint_Set(MARK_DIM,-MARK_DIM);
 Align[2]=MyPoint_Set(-MARK_DIM,-MARK_DIM);
 Align[3]=MyPoint_Set(-MARK_DIM,MARK_DIM);

 // put in code for all layer alignment marks
 //Offset mark 4x
 int c,d;
 for(d=0; d<4; d++) {
  for(c=0; c<ALIGN_SIZE; c++) {
   Align_offset[c] = LPoint_Add(Corners[d],Align[c]);
  }
```

```
    LPolygon_New(cell, layer, Align_offset, ALIGN_SIZE);
  }

 return;
}



 /* Main function */
 void hybrid01_main(void)
 {
  /* Begin DO NOT EDIT SECTION generated by L-Edit */
  LCell           cellCurrent    = (LCell)LMacro_GetNewTCell()
     ;
  LLayer          Layer1         = (LLayer)LCell_GetParameter(
     cellCurrent, "Layer1");
  LLayer          Layer2         = (LLayer)LCell_GetParameter(
     cellCurrent, "Layer2");
  LLayer          Layer3         = (LLayer)LCell_GetParameter(
     cellCurrent, "Layer3");
  LLayer          Layer4         = (LLayer)LCell_GetParameter(
     cellCurrent, "Layer4");
  LLayer          Layer5         = (LLayer)LCell_GetParameter(
     cellCurrent, "Layer5");
  LLayer          Layer6         = (LLayer)LCell_GetParameter(
     cellCurrent, "Layer6");
  /* End DO NOT EDIT SECTION generated by L-Edit */


  /* TODO: Put local variables here. */

  LPoint Box_1[2];
  LPoint Taper[TMAX2];
  LPoint Box_2[2];
  LPoint Align[ALIGN_SIZE];
  LPoint Align_offset[ALIGN_SIZE];
  LPoint Corners[4];
  LPoint currPos, currPoint, currOrigin;
  LLayer MyLayers[6], layerCurrent;

  //init MyLayers
  MyLayers[0]=Layer1;
  MyLayers[1]=Layer2;
  MyLayers[2]=Layer3;
  MyLayers[3]=Layer4;
```

```
MyLayers[4]=Layer5;
MyLayers[5]=Layer6;


int c,d,n;
double xtemp, ytemp;
//parameter in exponential taper
double tau_inv = (log(W_SI_ACTIVE/W_SI_PASSIVE)) * L_TAPER;
double xsize, ysize, xsize_offset,arb_offset;

/* TODO: Begin custom generator code.*/

//initialize
currPoint     = MyPoint_Set(0,0);  //work coordinate in the
    current cell ref frame
currPos       = MyPoint_Set(0,0);  //work coordinate in the
   absolute ref frame
currOrigin    = MyPoint_Set(0,0);  //origin of current cell
    in abs ref frame

for(n=0; n<NUM_WG; n++) {
currOrigin = MyPoint_Set(0,n*YPERIOD);  //origin of current
    cell in abs ref frame
currPos = currOrigin;
tau_inv = (log( (W_SI_ACTIVE+n*D_W_SI_ACTIVE) / (
   W_SI_PASSIVE+n*D_W_SI_PASSIVE) ))/ L_TAPER;


//Si waveguide definition

//Alignment marks

 //Define Corners
 xsize=L_SI_PASSIVE+L_TAPER+L_SI_ACTIVE+L_SI_PASSIVE+
    L_TAPER;
 xsize_offset=-80;
 ysize=YPERIOD-100;
 arb_offset=60;
 Corners[0]    = MyPoint_Set(-xsize_offset,ysize/2);
 Corners[1]    = MyPoint_Set(-xsize_offset,-ysize/2);
 Corners[2]    = MyPoint_Set(xsize+xsize_offset,ysize/2);
 Corners[3]    = MyPoint_Set(xsize+xsize_offset+arb_offset
    ,-ysize/2);
 for(d=0; d<4; d++) {
```

```
  Corners[d] = LPoint_Add(Corners[d] ,currOrigin); //move
      to the next section
 }

 //define Mark
 Align[0]=MyPoint_Set(20,20);
 Align[1]=MyPoint_Set(20,-20);
 Align[2]=MyPoint_Set(-20,-20);
 Align[3]=MyPoint_Set(-20,20);

 // put in code for all layer alignment marks
 layerCurrent=MyLayers[0];
 //Offset mark 4x
 for(d=0; d<4; d++) {
  for(c=0; c<ALIGN_SIZE; c++) {
   Align_offset[c] = LPoint_Add(Corners[d],Align[c]);
  }
   if(DRAW_OPTOALIGN) { LPolygon_New(cellCurrent,
      layerCurrent, Align_offset, ALIGN_SIZE);}
 }


//generate section "a"
 Box_1[0]      = MyPoint_Set(0 ,-(W_SI_PASSIVE+n*
    D_W_SI_PASSIVE)/2.);     //lower left corner
 Box_1[0]      = LPoint_Add(Box_1[0],currPos);    //offset
 Box_1[1]      = MyPoint_Set(L_SI_PASSIVE, (W_SI_PASSIVE+n*
    D_W_SI_PASSIVE)/2.);     //upper right corner
 Box_1[1]      = LPoint_Add(Box_1[1],currPos);    //offset

 if(DRAW_OPTO) { MyBox_New(cellCurrent, layerCurrent, Box_1
    );}

 currPoint     = MyPoint_Set(L_SI_PASSIVE,0);
 currPos       = LPoint_Add(currPos,currPoint);  //move to
    the next section


//generate taper array
 for(c=0; c<TMAX; c++) {
  xtemp     = L_TAPER*c/(TMAX-1);
  currPoint     = MyPoint_Set(xtemp,(W_SI_PASSIVE+n*
     D_W_SI_PASSIVE)/2.*exp(xtemp*tau_inv));
  Taper[c]     = LPoint_Add(currPoint, currPos);
```

```
  currPoint      = MyPoint_Set(xtemp,-(W_SI_PASSIVE+n*
     D_W_SI_PASSIVE)/2.*exp(xtemp*tau_inv));
  Taper[TMAX2-1-c]  = LPoint_Add(currPoint, currPos);
 }

 if(DRAW_OPTO) { LPolygon_New(cellCurrent, layerCurrent,
    Taper, TMAX2); }

 currPoint      = MyPoint_Set(L_TAPER,0);
 currPos      = LPoint_Add(currPos,currPoint);  //move to
    the next section

//generate section "b"
 Box_2[0]      = MyPoint_Set(0 ,-(W_SI_ACTIVE+n*
    D_W_SI_ACTIVE)/2.);      //lower left corner
 Box_2[0]      = LPoint_Add(Box_2[0],currPos);   //offset
 Box_2[1]      = MyPoint_Set(L_SI_ACTIVE, (W_SI_ACTIVE+n*
    D_W_SI_ACTIVE)/2.);      //upper right corner
 Box_2[1]      = LPoint_Add(Box_2[1],currPos);   //offset

 if(DRAW_OPTO) { LBox_New(cellCurrent, layerCurrent, Box_2
    [0].x,Box_2[0].y,Box_2[1].x,Box_2[1].y); }

 currPoint      = MyPoint_Set(L_SI_ACTIVE,0);
 currPos      = LPoint_Add(currPos,currPoint); //move to the
     next section

//generate taper array
 for(c=0; c<TMAX; c++) {
  xtemp     = L_TAPER*c/(TMAX-1);
  currPoint      = MyPoint_Set(L_TAPER*(1-xtemp/L_TAPER),(
     W_SI_PASSIVE+n*D_W_SI_PASSIVE)/2.*exp(xtemp*tau_inv));
  Taper[c]      = LPoint_Add(currPoint, currPos);
  currPoint      = MyPoint_Set(L_TAPER*(1-xtemp/L_TAPER),-(
     W_SI_PASSIVE+n*D_W_SI_PASSIVE)/2.*exp(xtemp*tau_inv));
  Taper[TMAX2-1-c]  = LPoint_Add(currPoint, currPos);
 }
 if(DRAW_OPTO) { LPolygon_New(cellCurrent, layerCurrent,
    Taper, TMAX2);}

 currPoint      = MyPoint_Set(L_TAPER,0);
 currPos      = LPoint_Add(currPos,currPoint);  //move to
    the next section

//generate section "a"
```

```
 Box_1[0]      = MyPoint_Set(0 ,-(W_SI_PASSIVE+n*
    D_W_SI_PASSIVE)/2.);     //lower left corner
 Box_1[0]      = LPoint_Add(Box_1[0],currPos);    //offset
 Box_1[1]      = MyPoint_Set(L_SI_PASSIVE, (W_SI_PASSIVE+n*
    D_W_SI_PASSIVE)/2.);     //upper right corner
 Box_1[1]      = LPoint_Add(Box_1[1],currPos);    //offset

 if(DRAW_OPTO) { MyBox_New(cellCurrent, layerCurrent, Box_1
    );}


 currPos       = currOrigin;     //reset to origin

//Proton mask
layerCurrent=MyLayers[1];
for(d=0; d<4; d++) {
  for(c=0; c<ALIGN_SIZE; c++) {
   Align_offset[c]  = LPoint_Add(Corners[d],Align[c]);
  }
   if(DRAW_ION) { LPolygon_New(cellCurrent, layerCurrent,
      Align_offset, ALIGN_SIZE);}
 }

BoundingBox( cellCurrent, layerCurrent, BOX_H,BOX_W,BOX_T);

 Box_1[0]      = MyPoint_Set(L_SI_PASSIVE+L_TAPER-
    W_PROTON_EDGE ,W_PROTON/2.);    //lower left corner
 Box_1[0]      = LPoint_Add(Box_1[0],currPos);    //offset
 Box_1[1]      = MyPoint_Set(L_SI_PASSIVE+L_TAPER+
    L_SI_ACTIVE+W_PROTON_EDGE , W_PROTON/2.+W_PROTON_WINDOW
    );  //upper right corner
 Box_1[1]      = LPoint_Add(Box_1[1],currPos);    //offset
 if(DRAW_ION) { MyBox_New(cellCurrent, layerCurrent, Box_1)
    ;}


 Box_1[0]      = MyPoint_Set(L_SI_PASSIVE+L_TAPER-
    W_PROTON_EDGE ,-W_PROTON/2.);    //lower left corner
 Box_1[0]      = LPoint_Add(Box_1[0],currPos);    //offset
 Box_1[1]      = MyPoint_Set(L_SI_PASSIVE+L_TAPER+
    L_SI_ACTIVE+W_PROTON_EDGE, -(W_PROTON/2.+
    W_PROTON_WINDOW));  //upper right corner
 Box_1[1]      = LPoint_Add(Box_1[1],currPos);    //offset
 if(DRAW_OPTO) { MyBox_New(cellCurrent, layerCurrent, Box_1
    );}
```

```
  //Mesa mask
  layerCurrent=MyLayers[2];
   for(d=0; d<4; d++) {
    for(c=0; c<ALIGN_SIZE; c++) {
     Align_offset[c]  = LPoint_Add(Corners[d],Align[c]);
    }
     if(DRAW_MESA) { LPolygon_New(cellCurrent, layerCurrent,
        Align_offset, ALIGN_SIZE);}
   }
  BoundingBox( cellCurrent, layerCurrent, BOX_H,BOX_W,BOX_T);
/*
  //Center part
   Box_1[0]      = MyPoint_Set(L_SI_PASSIVE+L_TAPER ,-W_MESA
      /2.);   //lower left corner
   Box_1[0]      = LPoint_Add(Box_1[0],currPos);   //offset
   Box_1[1]      = MyPoint_Set(L_SI_PASSIVE+L_TAPER+
      L_SI_ACTIVE, -YPERIOD/2); //upper right corner
   Box_1[1]      = LPoint_Add(Box_1[1],currPos);   //offset

   Box_2[0]      = MyPoint_Set(L_SI_PASSIVE+L_TAPER ,W_MESA
      /2.);   //lower left corner
   Box_2[0]      = LPoint_Add(Box_2[0],currPos);   //offset
   Box_2[1]      = MyPoint_Set(L_SI_PASSIVE+L_TAPER+
      L_SI_ACTIVE, YPERIOD/2);  //upper right corner
   Box_2[1]      = LPoint_Add(Box_2[1],currPos);   //offset

   if(DRAW_MESA) { MyBox_New(cellCurrent, layerCurrent, Box_1
      );}
   if(DRAW_MESA) { MyBox_New(cellCurrent, layerCurrent, Box_2
      );}

  //Side boxes
   Box_1[0]      = MyPoint_Set(0 ,-YPERIOD/2);   //lower left
      corner
   Box_1[0]      = LPoint_Add(Box_1[0],currPos);   //offset
   Box_1[1]      = MyPoint_Set(L_SI_PASSIVE+L_TAPER, YPERIOD
      /2); //upper right corner
   Box_1[1]      = LPoint_Add(Box_1[1],currPos);   //offset

   Box_2[0]      = MyPoint_Set(L_SI_PASSIVE+L_TAPER+
      L_SI_ACTIVE , -YPERIOD/2);   //lower left corner
   Box_2[0]      = LPoint_Add(Box_2[0],currPos);   //offset
```

```
    Box_2[1]      = MyPoint_Set(xsize, YPERIOD/2);   //upper
       right corner
    Box_2[1]      = LPoint_Add(Box_2[1],currPos);    //offset

    if(DRAW_MESA) { MyBox_New(cellCurrent, layerCurrent, Box_1
       );}
    if(DRAW_MESA) { MyBox_New(cellCurrent, layerCurrent, Box_2
       );}
*/

  //Center part
    Box_1[0]      = MyPoint_Set(xsize/2.-L_MESA/2. ,-W_MESA/2.)
       ;   //lower left corner
    Box_1[0]      = LPoint_Add(Box_1[0],currPos);    //offset
    Box_1[1]      = MyPoint_Set(xsize/2.+L_MESA/2., -YPERIOD/2)
       ; //upper right corner
    Box_1[1]      = LPoint_Add(Box_1[1],currPos);    //offset

    Box_2[0]      = MyPoint_Set(xsize/2.-L_MESA/2. ,W_MESA/2.);
         //lower left corner
    Box_2[0]      = LPoint_Add(Box_2[0],currPos);    //offset
    Box_2[1]      = MyPoint_Set(xsize/2.+L_MESA/2., YPERIOD/2);
        //upper right corner
    Box_2[1]      = LPoint_Add(Box_2[1],currPos);    //offset

    if(DRAW_MESA) { MyBox_New(cellCurrent, layerCurrent, Box_1
       );}
    if(DRAW_MESA) { MyBox_New(cellCurrent, layerCurrent, Box_2
       );}

  //Side boxes
    Box_1[0]      = MyPoint_Set(0 ,-YPERIOD/2);    //lower left
       corner
    Box_1[0]      = LPoint_Add(Box_1[0],currPos);    //offset
    Box_1[1]      = MyPoint_Set(xsize/2.-L_MESA/2., YPERIOD/2);
        //upper right corner
    Box_1[1]      = LPoint_Add(Box_1[1],currPos);    //offset

    Box_2[0]      = MyPoint_Set(xsize/2.+L_MESA/2., -YPERIOD/2)
       ;   //lower left corner
    Box_2[0]      = LPoint_Add(Box_2[0],currPos);    //offset
    Box_2[1]      = MyPoint_Set(xsize, YPERIOD/2);   //upper
       right corner
    Box_2[1]      = LPoint_Add(Box_2[1],currPos);    //offset
```

```
 if(DRAW_MESA) { MyBox_New(cellCurrent, layerCurrent, Box_1
    );}
 if(DRAW_MESA) { MyBox_New(cellCurrent, layerCurrent, Box_2
    );}


//P contact
layerCurrent=MyLayers[3];
for(d=0; d<4; d++) {
  for(c=0; c<ALIGN_SIZE; c++) {
   Align_offset[c]  = LPoint_Add(Corners[d],Align[c]);
  }
   if(DRAW_P) { LPolygon_New(cellCurrent, layerCurrent,
      Align_offset, ALIGN_SIZE);}
 }

BoundingBox( cellCurrent, layerCurrent, BOX_H,BOX_W,BOX_T);
 //This goes on top of the Mesa
 Box_1[0]      = MyPoint_Set(L_SI_PASSIVE+L_TAPER,-
    W_P_CONTACT/2.);   //lower left corner
 Box_1[0]      = LPoint_Add(Box_1[0],currPos);   //offset
 Box_1[1]      = MyPoint_Set(L_SI_PASSIVE+L_TAPER+
    L_SI_ACTIVE, W_P_CONTACT/2.); //upper right corner
 Box_1[1]      = LPoint_Add(Box_1[1],currPos);   //offset

 //layerCurrent=MyLayers[];
 if(DRAW_P) { MyBox_New(cellCurrent, layerCurrent, Box_1);}

//N contact
layerCurrent=MyLayers[4];
for(d=0; d<4; d++) {
  for(c=0; c<ALIGN_SIZE; c++) {
   Align_offset[c]  = LPoint_Add(Corners[d],Align[c]);
  }
   if(DRAW_N) { LPolygon_New(cellCurrent, layerCurrent,
      Align_offset, ALIGN_SIZE);}
 }

BoundingBox( cellCurrent, layerCurrent, BOX_H,BOX_W,BOX_T);
 //This goes to either side of the Mesa
 Box_1[0]      = MyPoint_Set(L_SI_PASSIVE+L_TAPER,W_MESA/2.+
    CONTACT_OFFSET);   //lower left corner
 Box_1[0]      = LPoint_Add(Box_1[0],currPos);        //
    offset
```

```
    Box_1[1]      = MyPoint_Set(L_SI_PASSIVE+L_TAPER+
       L_SI_ACTIVE, W_MESA/2.+CONTACT_OFFSET+W_N_CONTACT);   //
       upper right corner
    Box_1[1]      = LPoint_Add(Box_1[1],currPos);          //
       offset

    Box_2[0]      = MyPoint_Set(L_SI_PASSIVE+L_TAPER ,-W_MESA
       /2.-CONTACT_OFFSET-W_N_CONTACT);    //lower left corner
    Box_2[0]      = LPoint_Add(Box_2[0],currPos);          //
       offset
    Box_2[1]      = MyPoint_Set(L_SI_PASSIVE+L_TAPER+
       L_SI_ACTIVE, -W_MESA/2.-CONTACT_OFFSET);   //upper right
        corner
    Box_2[1]      = LPoint_Add(Box_2[1],currPos);          //
       offset


    //layerCurrent=MyLayers[];
    if(DRAWN) { MyBox_New(cellCurrent, layerCurrent, Box_1);}
    if(DRAWN) { MyBox_New(cellCurrent, layerCurrent, Box_2);}

    currPoint      = MyPoint_Set(0,L_SI_PASSIVE);
    currPos        = LPoint_Add(currPos,currPoint);   //move to
       the next section




   /* End custom generator code.*/
   }
  }
}
hybrid01_main();
```

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