UHF and X-Band Class-E Amplifiers

Thesis by

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To my Parents,

For their Love and Patience

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UHF and X-Band Class-E Amplifiers

Abstract

A Class-E amplifier consists of a single transistor which is driven as a switch and a passive output load network. The output load network is a tuned resonant circuit and is designed to minimize the voltage and current waveforms overlapping, thus minimize the power dissipation in the transistor. The Class-E amplifier is for high efficiency operation with a theoretical maximum efficiency of 100%, and in practice about 80%–90%. Design approaches for Class-E amplifiers are described. Designs and experimental results for one 440 MHz and two X-band Class-E amplifiers are presented in detail. The 440 MHz Class-E amplifier is implemented using lumped components and the active transistor is the Motorola MRF183 n-channel lateral MOSFET. It delivers an output power of 15 W, drain efficiency of 77%, power-added efficiency (PAE) of 70% with an input power of 1.4 W. For the two X-band Class-E amplifiers, one uses Fujitsu FHX35X HEMT as the active device and has an output power of 30 mW, drain efficiency of 80% and PAE of 64% at 11.2 GHz. The other one uses Fujitsu FLR056XV MESFET and achieves an output power of 190 mW, drain efficiency of 72% and PAE of 56% at 9 GHz. The two X-band Class-E amplifiers are implemented using microstrip transmission lines.

Contents

Chapter 1

Introduction

Achieving high efficiency in amplifiers is very important because it allows high output power and reduces heat dissipation. Reduction of the DC input power required to produce the same output power allows reduction in the size of the power supply or batteries. This is important in both portable transmitters and fixed high power transmitters. High efficiency also means low power dissipation, making it possible to greatly reduce the size and the weight of the heat sink. The low power dissipation also permits a reduction in the device junction temperature, and a subsequent improvement in reliability.

The Class-E amplifier [1]–[3] operates in a switch mode to achieve a high efficiency. It was first demonstrated by Gerald Ewing in 1964 [1], and developed and patented by Nathan and Alan Sokal in 1975 [2][3]. In the Class-E amplifier, a single transistor is employed to be driven as a switch. The the output load network is designed so that the voltage and current waveshapes have minimal overlapping and the power dissipation in the transistor is minimized.

Class-E amplifiers can be used in CW, FM, and AM transmitters. CW signals require only two carrier amplitudes: on and off. FM signals (as well as phase-modulated and frequency-shift-keyed signals) have a carrier with a constant amplitude. Although an AM signal requires a carrier signal with a time-varying amplitude, the amplitude variation can be modulated on the drain bias voltage since the output power is proportional to the DC power for Class-E amplifiers. Gaussian Minimum Shift Keying (GMSK) [4] used as the modulation

scheme in the European standard for mobile communications (GSM), is an example of constant envelope modulation. On the other hand, the North American Digital Cellular (NADC) standard uses $\pi/4$-shift Differential Quadrature Phase Shift Keying ($\pi/4$-DQPSK) [5], which yields nonconstant carrier envelope once it is filtered. In this case, if a high efficiency power amplifier, such as Class-E amplifier, is used, the signal spectrum will be degraded due to nonlinearities in the amplifier and the high efficiency amplifiers must be linearized with techniques such as Envelope Elimination and Restoration [6]. Industrial applications of electric process heating utilize electrical energy at frequencies from 50 Hz to 2.5 GHz and power levels from 100 W to over 100 MW. Class-E amplifiers are useful in these applications, and a 100-W, 3.3-MHz Class-E amplifier for industrial cap sealing applications is demonstrated in [7].

In the following, we will introduce various classes of amplifiers for different applications. We will also discuss the background, progress of Class-E amplifiers, as well as the design and development of the amplifiers at Caltech.

Although we will focus on Class-E amplifiers, it is worthwhile to note that oscillators [8][9] and multipliers [10][11] operating in Class-E mode have also been developed.

1.1 Classification of Power Amplifiers

There are numerous classes of amplifiers such as class A, B, C, D, E, F, etc., for different applications. Refs. [12] and [13] give a review of all these classes of amplifications. Class A and Class B modes operate in the active region of a transistor which results in maximum gain and linearity at the expense of efficiency. Class C, D, E, F operate in switch mode. This results in maximum efficiency at the expense of gain and linearity. The ideal maximum efficiency of Class A amplifier is 50%. For Class B amplifier, the most common configuration is the push-pull transformer-coupled circuit. Two devices are driven 180° out of phase so that each device is active half of the cycle and cut off during the other half of

the cycle. The ideal maximum efficiency is 78.5%.

The increased efficiency of amplifiers results from techniques that reduce the average drain voltage-current product, i.e., power dissipation. In switching mode power amplifiers, such as Class D and E, this is accomplished by employing the active devices as switches. The ideal efficiency for Class D and E amplifiers is 100%.

1.1.1 Class A Amplifier

Class A amplifiers produce outputs with little distortion because the transistors are biased and driven so that they are always active. However, when a transistor is active, the voltage and current are large simultaneously, causing large power dissipation and low efficiency. The amplifier dissipates power even when there is no output. For this reason, Class A amplifiers are most commonly used as low-level driver amplifiers. In these applications, the power consumed by the Class A amplifier is a relatively small portion of the total transmission power. The theoretical maximum efficiency of Class A amplifier is 50%, while in practice the efficiency is around 30%.

1.1.2 Class B Amplifier

The most common configuration of Class B amplifier is the push-pull circuit. In a push-pull amplifier, there are two transistors and they are driven 180° out-of-phase and each transistor is active for half of the cycle. Class B operation is more efficient than Class A for linear RF amplification. The maximum theoretical efficiency is 78.5% and in practice it is around 60%. Class B is almost universal in medium and high power linear amplifiers.

1.1.3 Class C Amplifier

Class C amplifier is a nonlinear amplifier and the transistor operates in switch mode. It is typically driven hard enough to cause the transistor to enter

the saturation during a portion of each RF cycle. The output amplitude depends primarily on the drain supply voltage and is largely insensitive to variations of the amplitude of the driving signal. The efficiency is typically 75%. It is often used in FM transmitters and may be used in broadcast AM by varying the supply voltage.

1.1.4 Class D Amplifier

The Class D amplifier employs a pair of transistors and a tuned output circuit. The two transistors are driven as switches. The devices are driven to act as a two-pole switch that defines either a rectangular voltage or rectangular current waveform. The output circuit is tuned to the switching frequency and prevents DC and harmonic currents from reaching the load, resulting in a sinusoidal output. The main advantage of Class D amplifiers is the square-wave voltage across the device so that the peak voltage is low. The efficiency for an idealized Class D amplifier is 100% but in practice capacitive discharge losses limit the efficiency to near Class C levels.

1.1.5 Class F Amplifier

Class D amplifiers give a square-wave voltage that is attractive because it keeps the peak voltage low. On the other hand, Class C amplifiers use only one transistor and hence are simpler. The Class F amplifier uses a single transistor as switch like Class C, but uses a 3rd-harmonic trap filter to produce a flattened voltage like Class D. The efficiency of Class F amplifier is typically higher than Class C but lower than Class E.

1.2 Fundamentals of Class-E Amplifiers

The Class-E amplifier operates in switch mode. It employs a single transistor driven to act as a switch and connected to a passive load network. Figure 1.1 shows the simplest Class-E amplifier configuration. The output load network is

a tuned resonant circuit and the resonant frequency of L and C is set somewhat below the operating frequency. The active device acts as a switch, and the surrounding circuitry needs to be properly designed to minimize the heat loss by having minimal overlap between voltage and current across the transistor. The ideal switch voltage and current waveforms are shown in Figure 1.2. When the transistor turns off, the current flows into the resonant load network, and there

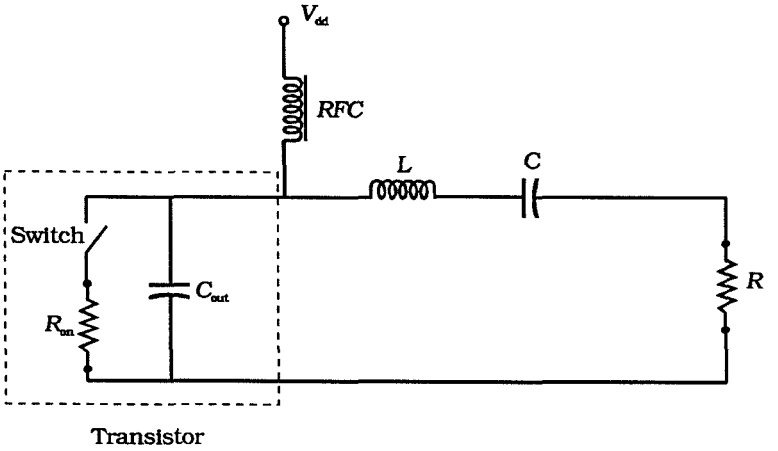

Figure 1.1 The Class-E amplifier configuration.

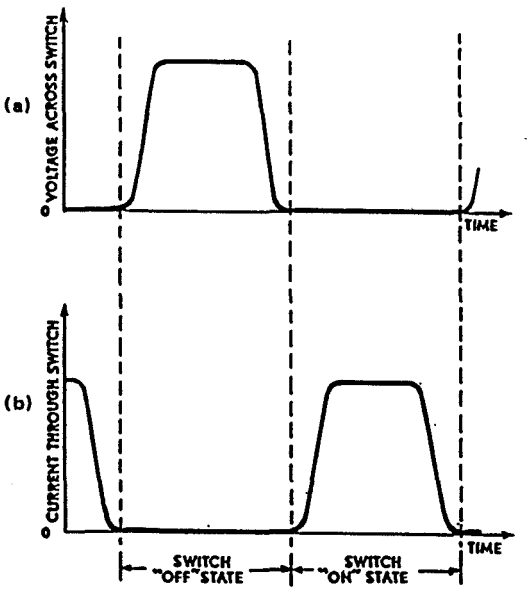

Figure 1.2 Ideal Class-E voltage and current waveforms.

is a transient voltage that rises and falls. With a properly designed load network, the voltage returns to zero smoothly with zero slope. The transistor voltage at turn-on is zero, so that the transistor does not discharge the output capacitance, thus avoiding dissipating the capacitive stored energy. When the slope of the transistor voltage waveform is zero, the current injected into the transistor at turn-on by the load network rises smoothly from zero at a controlled moderate rate, resulting in low power dissipation during the turn-on transition. When the transistor turns on, current rises smoothly until it switches off again. The transistor switches on when both the voltage and current are small, thus keeping losses low.

In the Class-E amplifier, the driving signal causes the switching of the transistor, but there is no relationship between the amplitude of the driving signal and the output signal. The output power is proportional to the DC power. Class-E amplifiers are the most efficient amplifiers known, about 90% in practice. The disadvantage is that the peak voltages across the transistor are even higher than for Class D and F amplifiers.

1.3 Class-E Amplifier Design Approaches

The Class-E amplifier design approaches can be categorized into two types: one is the analytical approach and the other is the Computer Aided Design approach.

1.3.1 Analytical Approach

Since the introduction of the Class-E amplifier, several papers have developed equations to analyze and design the Class-E amplifier [14]–[23]. In [14], Raab derived a set of equations to describe the idealized operation of the Class-E amplifier. In his analysis, he made five assumptions: (1) the RF choke allows only DC current and has no series resistance; (2) Q of the series-tuned output circuit is high enough that the output current is essentially a sinusoid at the fun-

damental frequency; (3) the switching action of the transistor is instantaneous and lossless (except when discharging the shunt capacitor); (4) the transistor has zero saturation voltage, zero on-resistance, and infinite off-resistance; (5) the total shunt capacitance is independent of the collector or drain voltage. These assumptions simplify the analysis. Based on [14], several papers analyze the Class-E amplifier by taking the nonideal conditions of the circuit into account. Since real amplifiers are made from nonideal components and are subject to non-ideal loads, it is necessary to determine the effects of deviation from the ideal. In [15], Raab shows the effects of variations in component values determined from the equations derived in [14]. In [16], Raab and Sokal analyze the performance of the Class-E amplifier in respect of the transistor power loss. Refs. [17] and [18] show that it is not possible to achieve both nonzero output power and 100% efficiency. In switching-mode circuits, it is not possible to eliminate both the transistor turn-on switching loss and the transistor turn-off switching loss while obtaining nonzero output power. At least one of the switching losses must be nonzero at nonzero output power. In other words, at least one discontinuity in switch voltage or switch current is necessary for nonzero output power of such a circuit. This imposes a lower bound on the power dissipation. Because the capacitive discharge loss at the transistor turn-on dominates, it is best to constrain the discontinuity to appear across the switch current. In the idealized Class-E high efficiency amplifier analysis, the collector current fall time is assumed to be zero. In [19], the effect of the non-zero collector current fall time during the on-to-off transition is described. Ref. [20] presents a detailed analysis of a Class-E amplifier at any load quality factor Q_L and any on switch duty cycle D, with component values chosen for optimum circuit operation. A complete analysis of the Class-E amplifier with finite DC feed inductance of the RF choke is given in [21]. The minimum value of the shunt capacitance of a Class-E amplifier is derived in [22]. If the shunt capacitance is selected to be smaller than the minimum

value, the output power of the amplifier cannot reach the desired level. To obtain the desired output power of the Class-E amplifier for optimum performance, the shunt capacitance must be selected to be equal to or greater than the minimum value. In [23], an analysis is performed to use the finite DC choke inductor to compensate the high intrinsic output capacitance of the active power device to extend the operation frequency.

1.3.2 Computer Aided Design Approach

In the Computer Aided Design approach, a commercial software package is used to design the output load network. The advantage of this is that it is not necessary to make so many assumption as in the analytical approach and it can handle all kinds of situations in the circuit. Two commercial softwares have been used in our design. One is PSpice [24][25] by MicroSim Corporation and the other is MDS (Microwave Design System) [26] by Hewlett Packard. When the large signal nonlinear model of the device is not available, the device can be modelled as a switch in parallel with the output capacitance of the device. With this simple model in PSpice, the output load network can be designed and the output power and drain efficiency can be simulated. Drain efficiency is defined as

$$\eta_{\mathrm{D}} = \frac{P_{\mathrm{out}}}{P_{\mathrm{dc}}}, \tag{1.1}$$

where P_{out} is the RF output power and P_{dc} is the DC power. When the nonlinear model of device is available, it can be used in MDS for the design of the output load network and simulation of the output power, gain, drain efficiency and power-added efficiency (PAE). Power-added efficiency is defined as

$$\mathrm{PAE} = \frac{P_{\mathrm{out}} - P_{\mathrm{in}}}{P_{\mathrm{dc}}}, \tag{1.2}$$

where P_{out} is the RF output power, P_{in} is the RF input power, and P_{dc} is the DC power. PAE is commonly used at microwave frequencies where the gain is often

low and it takes the input power into account. Another efficiency called overall efficiency is defined as

$$\eta = \frac{P_{\text{out}}}{P_{\text{dc}} + P_{\text{in}}}. \tag{1.3}$$

It is used at lower frequencies and gives a good indication of heating. Comparing these two methods, it can be seen that the MDS simulation using nonlinear model of device gives more information on the Class-E amplifier but it needs the nonlinear model of the device which is often not available. In the PSpice simulation, the device model is simple, the output load network of the Class-E amplifier can be designed, and the output power, the drain efficiency and harmonics can be predicted. But the switching model cannot be used to design the input match of a Class-E amplifier and it does not allow the prediction of gain and power-added efficiency. For the 440-MHz amplifier described in Chapter 2, the two methods have been used and the simulated component values for the output load network are very close. For the X-band Class-E amplifiers described in Chapter 3, since the nonlinear model of the transistor is not available, the device is modelled as a switch in parallel with the output capacitance of the device and the simulation is performed in PSpice.

1.4 The Progress of Class-E Amplifiers

Since the introduction of Class-E amplifiers [1]–[3], several Class-E amplifiers have been developed at different frequencies. Sokal [27] gives a review of the Class-E amplifiers from HF to microwave frequencies. In [1], Ewing showed a 20-W Class-E amplifier of 94% collector efficiency at 500 KHz. At low MHz frequencies, the Sokals [2] demonstrated a Class-E amplifier with efficiency as high as 96% and output power of 26 W at 3.9 MHz from a pair of Motorola 2N3735 TO-5 transistors. Since then, several Class-E circuits have been demonstrated at higher frequencies. In [28], a 450-MHz, 5-W output Class-E power amplifier was designed and constructed. It provided a collector efficiency of 89% and

5 W output power. Then four identical Class-E amplifiers and a travelling-wave power divider/combiner were combined to achieve a higher output power and high efficiency amplifier with 15 W output, 90% collector efficiency. A Class-E power amplifier with low supply voltage for wireless transmitter application is presented in [29]. This amplifier is designed at 835 MHz and it delivers an output power of 251 mW and power-added efficiency of greater than 50% at the supply voltage of 2.5 V. Tom Mader [30] demonstrated Class-E amplifiers at 0.5, 1, 2, and 5 GHz and the 5-GHz Class-E amplifier is integrated into an active antenna and demonstrated on a 2 × 2 power-combining array. At 0.5 GHz, 83% drain efficiency and 80% power-added efficiency are measured with output power of 0.55 W using Siemens CLY5 MESFET device. At 5 GHz, 81% drain efficiency and 72% power-added efficiency are measured with an output power of 0.61 W using the Fujitsu FLK052WG MESFET device. For the 2x2 power-combing Class-E amplifier array, at 5.05 GHz, it delivers a total of 2.4 W of output power with a DC-RF conversion efficiency of 74% and a power-added efficiency of 64%.

1.5 Class-E High Efficiency Amplifiers Developed at Caltech

Our group at Caltech started to develop Class-E high efficiency amplifiers three years ago. Joyce Wong [31] built a 300-W Class-E amplifier at 7 MHz using International Rectifier IRF840 MOSFET, achieving a drain efficiency of 89%. Eileen Lau *et al.* [32] developed a 500-W Class-E amplifier at 7 MHz with 90% drain efficiency. The transistor is the International Rectifier IRFP450 and the amplifier is driven by a QRP transceiver, a NorCal 40A modified for greater power output. John F. Davis *et al.* [33] developed a 400-W Class-E amplifier for industrial applications. The amplifier operates at 13.56 MHz and uses the International Rectifier IRFP440 Power MOSFET. The transistor is driven by 10 W input power and the amplifier achieves a drain efficiency of 91% and an overall efficiency of 87%.

Prof. Herbert Zirath, Chalmers University, Sweden, developed a 144-MHz

Class-E amplifier [34] using Motorola MRF183 MOSFET. The schematic diagram of the circuit is shown in Figure 1.3. An external shunt capacitance is added between the drain and source of the transistor. An inductance in series with a capacitance form the tuned circuit at the output to prevent DC and harmonic current from flowing through the load. At the output, a shunt capacitance in parallel with the 50 Ω load transforms the 50 Ω load to the desired load level for the Class-E amplifier. The output series inductance is a tuning inductor and Prof. Zirath has applied for a patent for it. The input matching circuit uses a 4:1 turn ratio transformer to transform 50 Ω to the impedance at the gate. The transformer has an inductance of 12 nH which happens to be needed in the matching circuit. The output load network is designed using the MDS simulation and the nonlinear Root model for the Motorola MRF183 MOSFET is used. The circuit is built on a $3\times4\frac{1}{8}$ -inch heat sink, and the device is mounted on the heat sink.

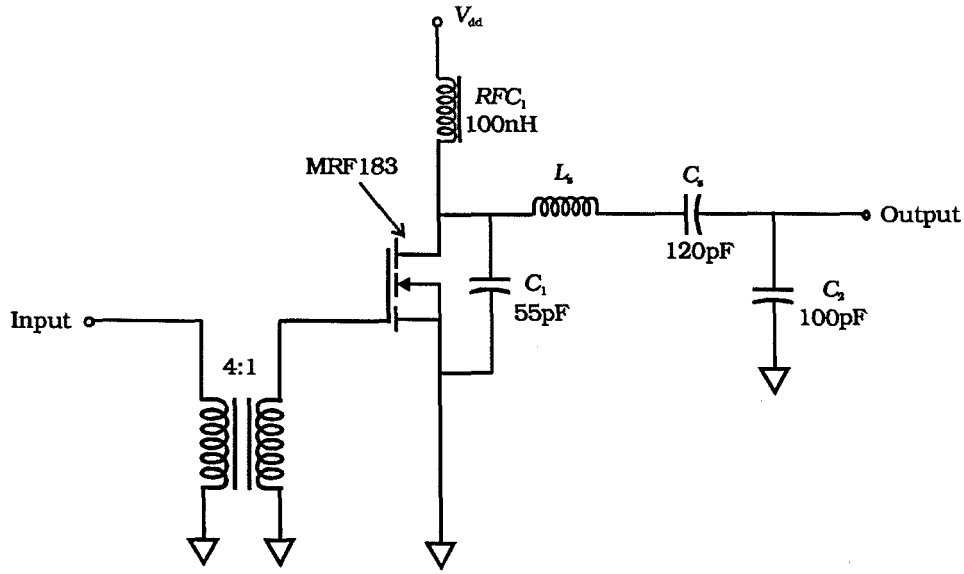

Figure 1.3 The schematic circuit diagram of the 144-MHz Class-E amplifier developed by Prof. Herbert Zirath.

Figures 1.4, 1.5, and 1.6 show the measurement results at 144 MHz. In the measurement shown in Figure 1.4, the input power is fixed at 5 W, the drain-source bias voltage is 20 V, and the output series inductance is tuned to get different output power and thus the corresponding efficiency. When the output power is adjusted to 54 W, the corresponding drain efficiency is 70% and PAE is 64%.

In Figure 1.5, with the input power fixed to be 5 W, it shows the output power versus the drain-source DC bias voltage while the output series inductance is tuned so that the output power achieves maximum. It shows that the output power increases with the drain-source bias voltage. When the drain-source DC bias voltage is 24 V, the output power gets to 61 W, and the corresponding drain efficiency and PAE are 59% and 54% respectively.

In Figure 1.6, with drain-source DC bias voltage fixed at 20 V, it shows

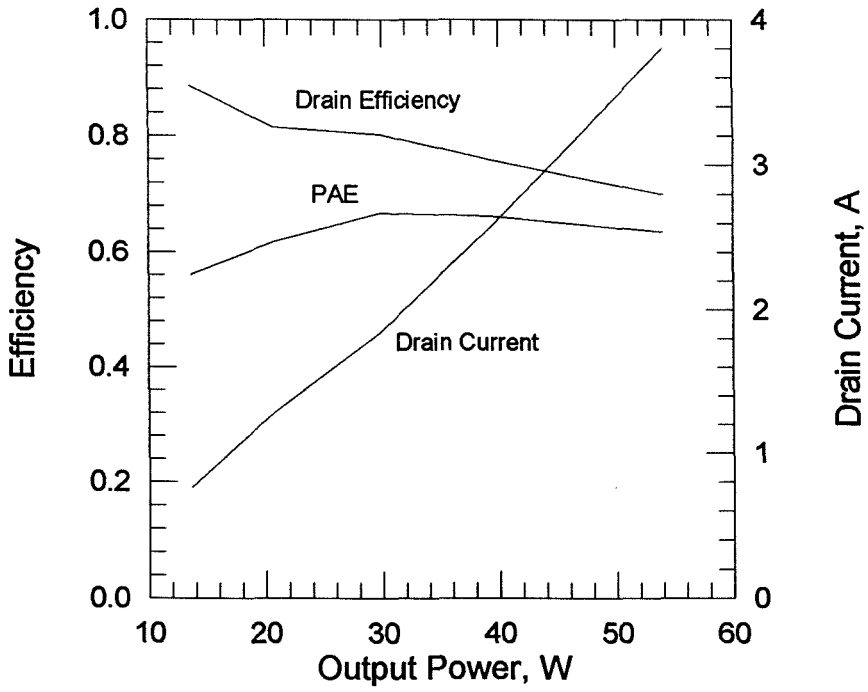

Figure 1.4 The 144-MHz Class-E amplifier measurement result of the efficiency versus the output power while tuning the output series inductance with input power of 5 W, the drain-source bias voltage of 20 V. Courtesy of Prof. Herbert Zirath.

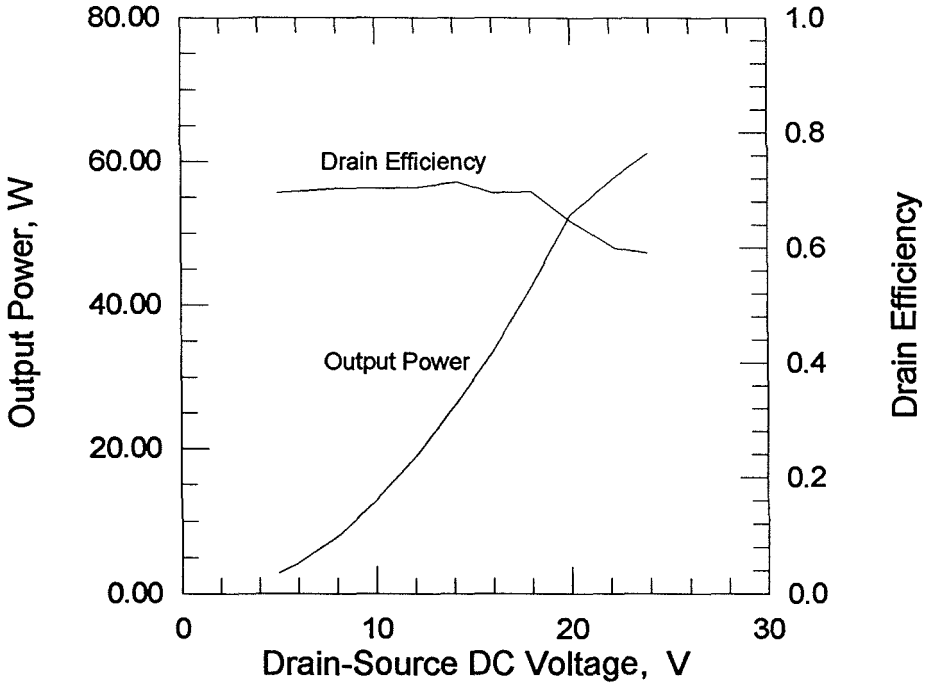

Figure 1.5 The 144-MHz Class-E amplifier measurement result of the efficiency and output power versus the drain-source bias voltage while tuning the output series inductance for maximum RF output power with input power of 5 W. Courtesy of Prof. Herbert Zirath.

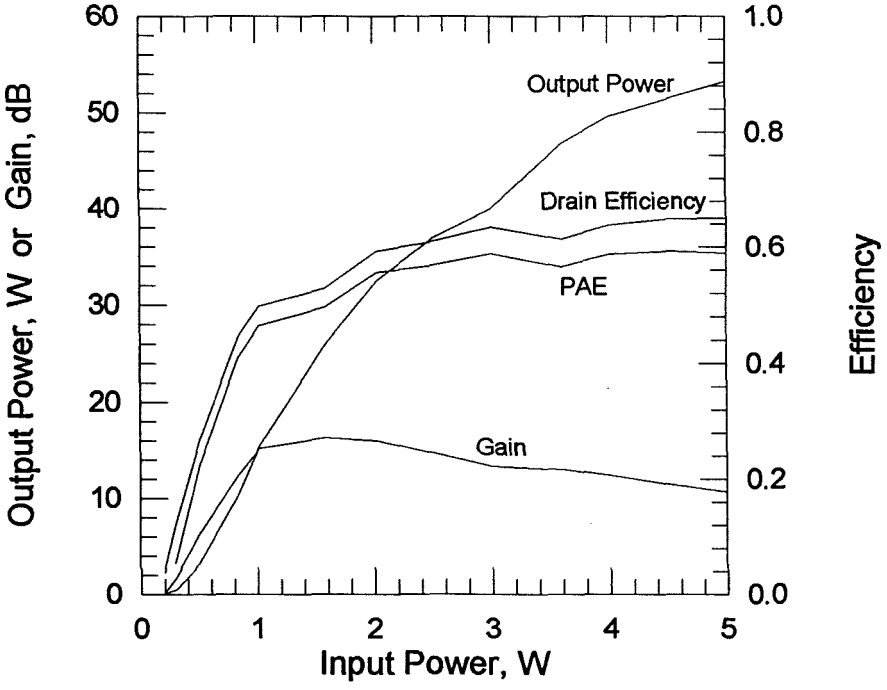

Figure 1.6 The 144-MHz Class-E amplifier measurement result of the efficiency and output power versus the input power while tuning the output series inductance for maximum RF output power with drain-source bias voltage of 20 V. Courtesy of Prof. Herbert Zirath.

the output power and efficiency versus the input power while the output series inductance is tuned so that the output power achieves maximum. When the input power is low, the efficiency is low because the on-resistance of the transistor is big. As the input power increases, the drain efficiency increases. As the input power continues to increase, the efficiency becomes flat.

In all the measurements only the output series inductance is tuned. The other circuit components are selected according to the MDS simulation result.

1.6 Outline of the Thesis

In Chapter 2, a UHF Class-E amplifier at 440 MHz is designed and developed. The Motorola MRF183 MOSFET operates as a switch in the amplifier. MRF183 MOSFET is an n-channel enhancement mode MOSFET. It is turned off when there is no voltage across the gate-source. This makes it suitable for our Class-E amplifier. Only a single power supply is necessary since we do not need to bias the gate. The output power is 16 W with drain efficiency of 77% and PAE of 70%. Two approaches are used in the amplifier design. One approach models the device as a switch in parallel with the output capacitance of the device and the model is used in PSpice to design the output load network. The other approach uses the nonlinear Root model downloaded from Motorola website and then uses MDS to design both the output load network and the input matching circuit.

Chapter 3 introduces the design and development of two X-band Class-E amplifiers. The first one uses the Fujitsu FHX35X HEMT, and achieves an output power of 30 mW, drain efficiency of 80% and PAE of 64%. The second one uses the Fujitsu FLR056 MESFET and delivers an output power of 190 mW, drain efficiency of 72% and PAE of 56%. In the amplifier design, the transistor is modelled as a switch in parallel with the output capacitance of the device. The output capacitance was measured and found to be linear. PSpice is used to design the output load network to produce the Class-E voltage and current

waveshapes. For the input matching, the manufacturer's S parameters are used with S_{21} attenuated by 3 dB to simulate the saturation of the device. These two Class-E amplifiers use transmission lines for the output load network and input matching.

Chapter 4 describes an X-band grid-oscillator beam-steering array which can scan from $-6.5°$ to $5°$. In a beam-steering array, beam-steering is achieved by setting the constant phase difference between adjacent elements. In a traditional phased array, the constant phase difference is set by phase shifters. However, phase shifters are expensive at microwave and millimeter wave frequencies. So in the grid-oscillator beam-steering array, no phase-shifters are used. The constant phase progression is established by detuning the end elements in the array. The planar line-grid oscillator is used as the radiating element.

The final chapter gives suggestions for future work.

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Chapter 2

440-MHz Class-E High Efficiency Amplifier

In this chapter, a 440-MHz Class-E high efficiency amplifier is presented. The Motorola MRF183 MOSFET [1] is the active device in the 440-MHz Class-E amplifier. Two Class-E amplifier design methods are introduced: one method uses PSpice [2][3] and models the transistor as a switch in parallel with the output capacitance of the transistor; the other uses Hewlett-Packard Microwave Design System (MDS) [4] and the proprietary nonlinear Root model of the transistor [5] given by Motorola. The Root model is a data based model and is generated by taking DC and S-parameter measurements over the entire operating range of the device. It can accurately capture device specific nonlinearities. The advantage of PSpice simulation is that we can introduce our own models for the device, and here it is only a switch model. But the MDS simulation will give a more complete design of the amplifier when the nonlinear model is available. The output capacitance of the MRF183 MOSFET is nonlinear and it depends on the drain-source voltage. The methods of modelling the nonlinear capacitance in PSpice are introduced. In the 440-MHz Class-E amplifier no external capacitor is added in parallel with the transistor at the drain.

The MDS simulation for the Class-E amplifier was first started by Professor Herbert Zirath, Univ. of Chalmers, Sweden. He developed a 144-MHz Class-E amplifier using MDS and the results are shown in Chapter 1. He also came up with the unique idea of tuning the output series inductance in the 440-MHz Class-E amplifier.

The 440-MHz Class-E amplifier is built on a Duroid substrate with dielectric constant of 2.2 and thickness of 10 mil. The substrate is copper plated on both sides. The substrate is mounted on a $3\times4\frac{1}{8}$ inch heat sink. A 1.5 mm deep and 6 mm wide slot is milled in the heat sink. The device is mounted in the slot with two 2-56 screws. Metal patterns are cut on the top of the substrate board for soldering the components. All the components used in the amplifier are lumped elements.

At 440 MHz the Class-E amplifier achieves a drain efficiency of 77%, a power-added efficiency of 70%, a gain of 10 dB, and an output power of 15 W.

2.1 Motorola MRF183 MOSFET

MOSFET stands for Metal-Oxide-Semiconductor Field-Effect Transistor. There are p-channel and n-channel devices, and they may be used as normally-ON (depletion-mode) devices, or as normally-OFF (enhancement-mode) devices. Figure 2.1 shows the cross section of an n-channel enhancement-mode LDMOS. In an enhancement-mode device the path between the source and drain takes the form of two back-to-back series diodes. Consequently the current is negligible for zero gate voltage. Application of a positive gate voltage, exceeding a certain threshold value, attracts sufficient number of negative carriers to the surface of the semiconductor to form an inversion layer. The resulting surface layer behaves

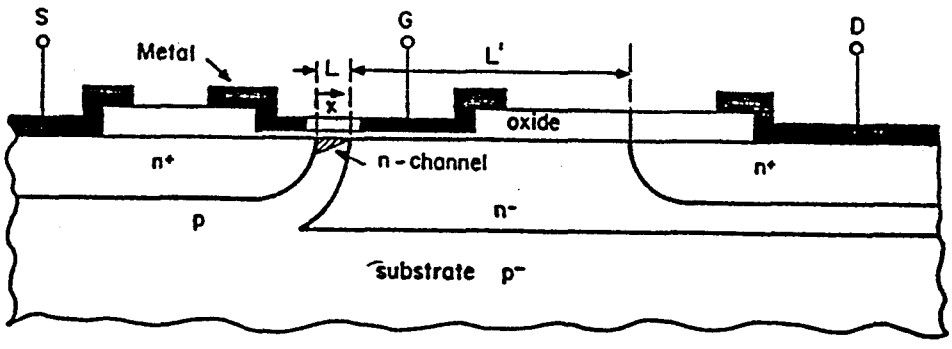

Figure 2.1 The cross section of an n-channel LDMOS [6].

as a piece of n-type material and forms a conducting bridge or channel between the source and drain. There are several reasons for the use of the n-channel enhancement-mode device for the Class-E amplifier application. Firstly, the conductivity is due to electrons, which have a higher degree of mobility than holes. Therefore, for given dimensions, the channel resistance is lower and the carrier transit time is shorter in an n-channel device. Secondly, as an enhancement-mode device, it draws negligible current and hence dissipates virtually no power in its normal OFF state. Because no gate bias is needed, the Class-E amplifier circuit is simpler. When no RF input is applied, there is no DC current and no DC power dissipation.

LDMOS [6] is developed for high frequency, high power applications. "L" means lateral and "D" indicates the double diffusion process. Figure 2.1 shows the cross section of an LDMOS device. The LDMOS has the advantage of short channel length, low feedback capacitance, high breakdown voltage, and scattering-limited drift velocity. What makes LDMOS different from a conventional MOSFET is that it contains a lowly doped n-region of length L' between the channel p-region and the highly n-doped drain contact region. LDMOS has high voltage capacity due to that the channel-drain depletion layer extends mostly to the lowly doped drain region. This aspect allows independent design of channel length and breakdown voltage. In order for the MOSFET to work at high frequency, the channel length should be small. The double-diffusion process makes it possible to achieve extremely narrow channels with conventional fabrication techniques and corresponding yields. With the channel length reduced, the MOSFET's can be expected to work to 10 GHz or higher.

The Motorola MRF183 is an n-channel enhancement-mode lateral MOSFET. It is designed for broadband commercial and industrial applications at frequencies to 1.0 GHz. According to the Motorola specification sheet [1], at 945 MHz, with a supply voltage of 28 V, the output power is 45 W PEP, the power

gain is 11.5 dB, and efficiency is 33%. The gate threshold voltage is typically 4 V when $V_{ds} = 10\,V$, and $I_d = 75\,mA$.

The output capacitance of MRF183 is nonlinear and it changes with the drain-source voltage. The output capacitance versus the drain-source voltage is given in the data sheet and is shown by a solid line in Figure 2.2. We use an equation to describe the relationship between the capacitance and the drain-source voltage. The dash line in Figure 2.2 is the fitted curve with the corresponding equation

$$C_{\text{nonlinear}} = \frac{C_0}{\sqrt[3]{1 + \frac{V}{V_0}}}, \tag{2.1}$$

where $C_0 = 117\,pF$ and $V_0 = 0.857\,V$. The best fit to the data yields an exponent of $-1/3$.

The on-resistance of the device between drain and source versus the gate-

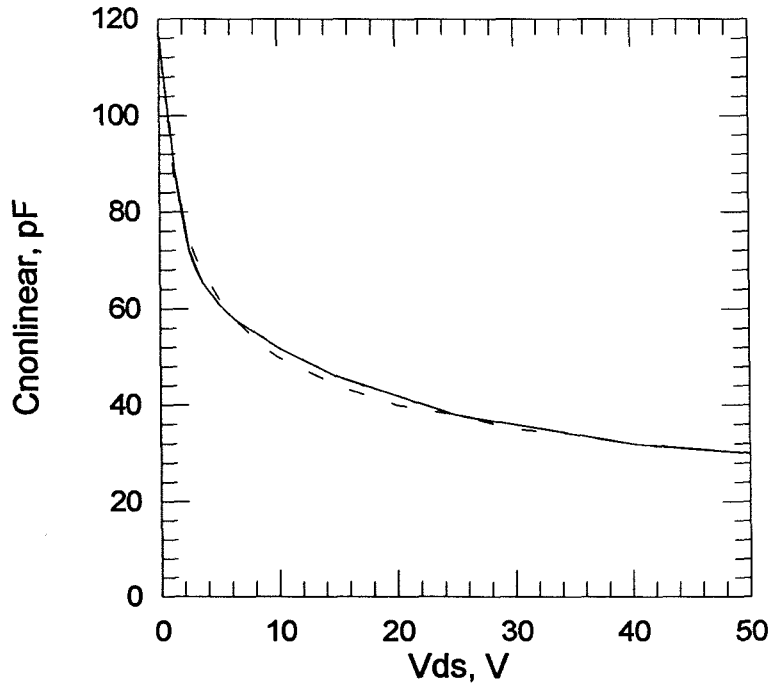

Figure 2.2 The MRF183 MOSFET output capacitance versus the drain-source voltage. — Manufacturer's data for the output capacitance. ---: $C_{\text{nonlinear}} = \frac{117}{\sqrt[3]{1+\frac{V_{ds}(V)}{0.857}}}(pF)$.

source voltage has been measured on a curve tracer and it is shown in Figure 2.3. When the gate voltage is 10 V, the on-resistance is measured to be 0.23 Ω.

2.2 Class-E Amplifier Design Using PSpice

In the PSpice simulation, the device is modelled as a switch in parallel with the output capacitance $C_{\text{nonlinear}}$ of the device as shown in Figure 2.4. The output capacitance is nonlinear and varies with the drain-source voltage as shown in Figure 2.2. R_{on} is the on-resistance of the transistor and its value is 0.23 Ω.

Given the output capacitance and the drain-source on-resistance for the device MRF183, the output load network is designed using PSpice. Since the output capacitance is nonlinear, a PSpice model for the nonlinear capacitance needs to be developed. We have tried two approaches to model the nonlinear capacitor. One uses a voltage-controlled current source and the other uses a

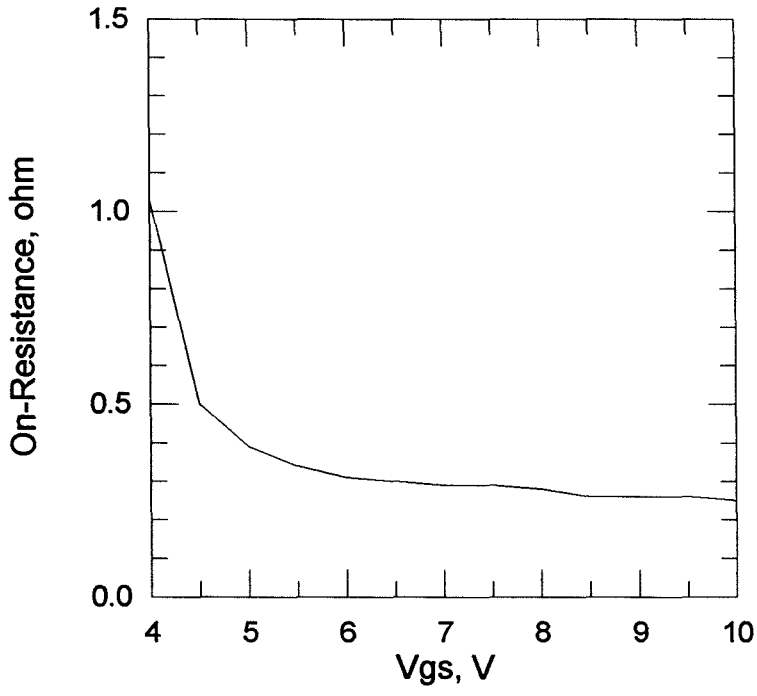

Figure 2.3 The curve tracer measurement of Motorola MRF183 MOSFET drain-source on-resistance versus gate-source voltage.

voltage-controlled voltage source in series with a linear capacitor. The capacitance of a linear capacitor does not vary with the voltage across it. The two approaches give the same simulation results and are equivalent.

2.2.1 A Parallel Model for the Nonlinear Capacitor in PSpice

The charge and current formulas for a linear capacitor C are:

$$Q = C \cdot V, \tag{2.2}$$

and

$$I = C \cdot dV(t)/dt, \tag{2.3}$$

where Q is the charge, V is the voltage across the capacitor, and I is the current through the capacitor. For a nonlinear(voltage-dependent) time-independent capacitor, these formulas become:

$$Q = \int_0^{V(t)} C(V') \cdot dV', \tag{2.4}$$

and

$$I = \frac{dQ}{dt} = C(V) \cdot \frac{dV(t)}{dt}. \tag{2.5}$$

The nonlinear capacitance can be modelled by a voltage-controlled current source G whose current is defined by Equation (2.5). The time derivative dV/dt is measured by applying a copy of the voltage across the voltage-controlled current source, G, to a known linear capacitance, C_{ref}, and monitoring its current, as

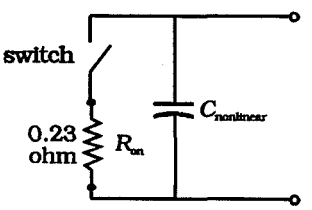

Figure 2.4 The MRF183 MOSFET model used in PSpice simulation. $C_{\text{nonlinear}}$ is the output capacitance of the transistor and R_{on} is the on-resistance.

shown in Figure 2.5. E is a voltage-controlled voltage source and its value is V. The current flowing through C_{ref} is

$$I = C_{\text{ref}} \frac{dV}{dt}. \tag{2.6}$$

From Equation (2.6), we get $\frac{dV}{dt}$, which is

$$\frac{dV}{dt} = \frac{I}{C_{\text{ref}}}. \tag{2.7}$$

In principle C_{ref} can have any value, but the PSpice simulation often gives an error when it is bigger than 0.01 F. For the voltage-controlled current source G, according to Equation (2.5), it is

$$\begin{aligned} G(V) &= C(V)\frac{dV(t)}{dt} \\ &= \frac{117\,(\text{pF})}{\sqrt[3]{1+\frac{V}{0.857}}} \cdot I \cdot C_{\text{ref}}. \end{aligned} \tag{2.8}$$

In this way, the nonlinear capacitor can be replaced by a voltage-controlled voltage source in PSpice simulation.

2.2.2 A Series Model for the Nonlinear Capacitor in PSpice

From circuit theory it is known that if two circuits are equivalent, the currents and voltages of the two circuits must be equal. Based on this, the nonlinear capacitor can be modelled using a linear capacitor in series with a voltage-controlled voltage source.

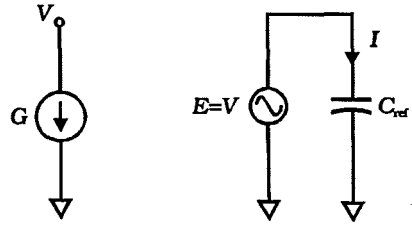

Figure 2.5 The parallel nonlinear capacitance model in PSpice.

There are two circuits in Figure 2.6. Assume they are equivalent. $C_{\text{nonlinear}}$ is a nonlinear capacitor that needs to be modelled and its capacitance varies with the voltage V across it. C_{linear} is a linear capacitor and its capacitance value can be chosen at one's convenience. V_1 is the voltage across C_{linear} and E is a voltage-controlled voltage source that is controlled by the voltage V_1. Once the dependence of E on V_1 is figured out, the nonlinear capacitor $C_{\text{nonlinear}}$ can be replaced by the linear capacitor C_{linear} in series with the voltage controlled voltage source E. For the MRF183 MOSFET device, the output capacitance is

$$C_{\text{nonlinear}} = \frac{C_0}{\sqrt[3]{1+\frac{V}{V_0}}}, \tag{2.1}$$

where $C_0 = 117\,\text{pF}$ and $V_0 = 0.857\,\text{V}$. Assume the charge on the capacitor $C_{\text{nonlinear}}$ is Q, then

$$C_{\text{nonlinear}} = \frac{dQ}{dV}. \tag{2.9}$$

Integrating the above equation gives

$$Q = \frac{3}{2}C_0V_0\left[\left(1+\frac{V}{V_0}\right)^{\frac{2}{3}} + A\right], \tag{2.10}$$

where A is a constant to be determined. Assume $Q = 0|_{V=0}$, solving for A in Equation (2.10),

$$A = -1,$$

which leads to

$$Q = \frac{3}{2}C_0V_0\left[\left(1+\frac{V}{V_0}\right)^{\frac{2}{3}} - 1\right]. \tag{2.11}$$

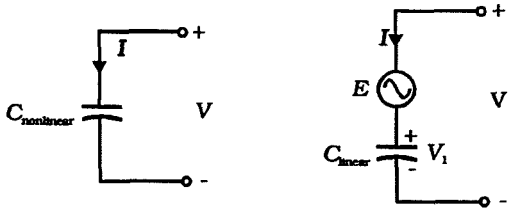

Figure 2.6 The series nonlinear capacitance model in PSpice.

Since the two circuits in Figure 2.6 are equivalent, the charge on C_{linear} is equal to that on $C_{\text{nonlinear}}$. For the linear capacitor,

$$Q = C_{\text{linear}} V_1. \tag{2.12}$$

Since C_{linear} is a linear capacitor and it can be any value, we can set

$$C_{\text{linear}} = \frac{3}{2} C_0. \tag{2.13}$$

Plugging this in the Equation (2.12),

$$Q = \frac{3}{2} C_0 V_0. \tag{2.14}$$

From Equations (2.11) and (2.14),

$$V_0 \left[\left(1 + \frac{V}{V_0} \right)^{\frac{2}{3}} - 1 \right] = V_1. \tag{2.15}$$

Solve the above equation for V,

$$V = V_0 \left[\left(1 + \frac{V_1}{V_0} \right)^{\frac{3}{2}} - 1 \right]. \tag{2.16}$$

And then

$$\begin{aligned} E &= V - V_1 \\ &= V_0 \left[\left(1 + \frac{V_1}{V_0} \right)^{\frac{3}{2}} - 1 \right] - V_1. \end{aligned} \tag{2.17}$$

In this way the nonlinear capacitor is modelled by a linear capacitor in series with a voltage controlled voltage source as shown in Figure 2.6.

2.3 PSpice Simulation

After the modelling of the output capacitance of the transistor, the output load network can be designed using PSpice. The PSpice model for the 440-MHz Class-E amplifier is shown in Figure 2.7. In the simulation, all the capacitors and

inductors are ideal, without loss. The MRF183 MOSFET transistor is modelled as a switch in parallel with a nonlinear capacitor. The switch has an on-resistance of 0.23 Ω. V_{dd} is the DC drain supply voltage. *RFC* is an RF choke that blocks the RF signal and the current flowing through it is a constant DC current. The output load network consists of a series inductor and capacitor resonant circuit loaded with a resistor. The values of R, L and C are chosen so that they produce the current and voltage waveshapes needed for the Class-E amplifier. With an R of 1.6 Ω, L of 5.5 nH, and C of 29 pF, the waveforms of the current through the switch and the voltage across the switch are shown in Figure 2.8. When V_{dd} is 15 V, the peak drain voltage is 50 V which is smaller than the device breakdown voltage 65 V specified in the data sheet, and the peak current through the transistor is 9.22 A. The simulated drain efficiency is 83%, and the output power is 36 W. The PSpice simulation of the output power spectrum is shown in Figure 2.9. The output power of the 2nd harmonic is 23 dB below the fundamental.

Varying L or C can tune the output power and efficiency. The PSpice simulation in Figure 2.10 shows the output power and drain efficiency versus L with C and R fixed when L varies from 4.5 nH to 7.0 nH. The plot shows that the peak output power and peak drain efficiency do not appear at the same

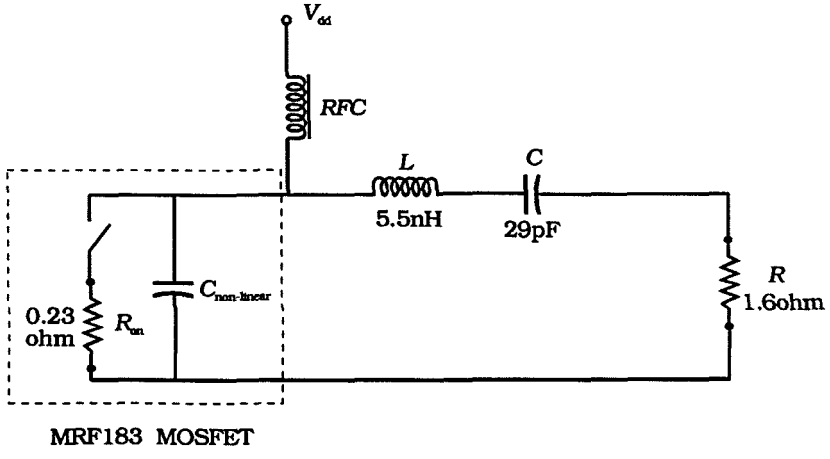

Figure 2.7 The 440-MHz Class-E amplifier PSpice model.

inductance and there is a trade-off between the output power and the drain efficiency. When L is 5 nH, the output power peaks at 44 W and the drain efficiency is about 72%. When L is 6.3 nH, the drain efficiency peaks at 92% but the output power drops to 14 W. Also note that when L is between 5 nH and 6.3 nH, higher output power is at the expense of lower drain efficiency and vice versa. The output power is sensitive to the value of L. The plot shows that when L increases from 5.5 nH to 6.25 nH, the output power decrease from

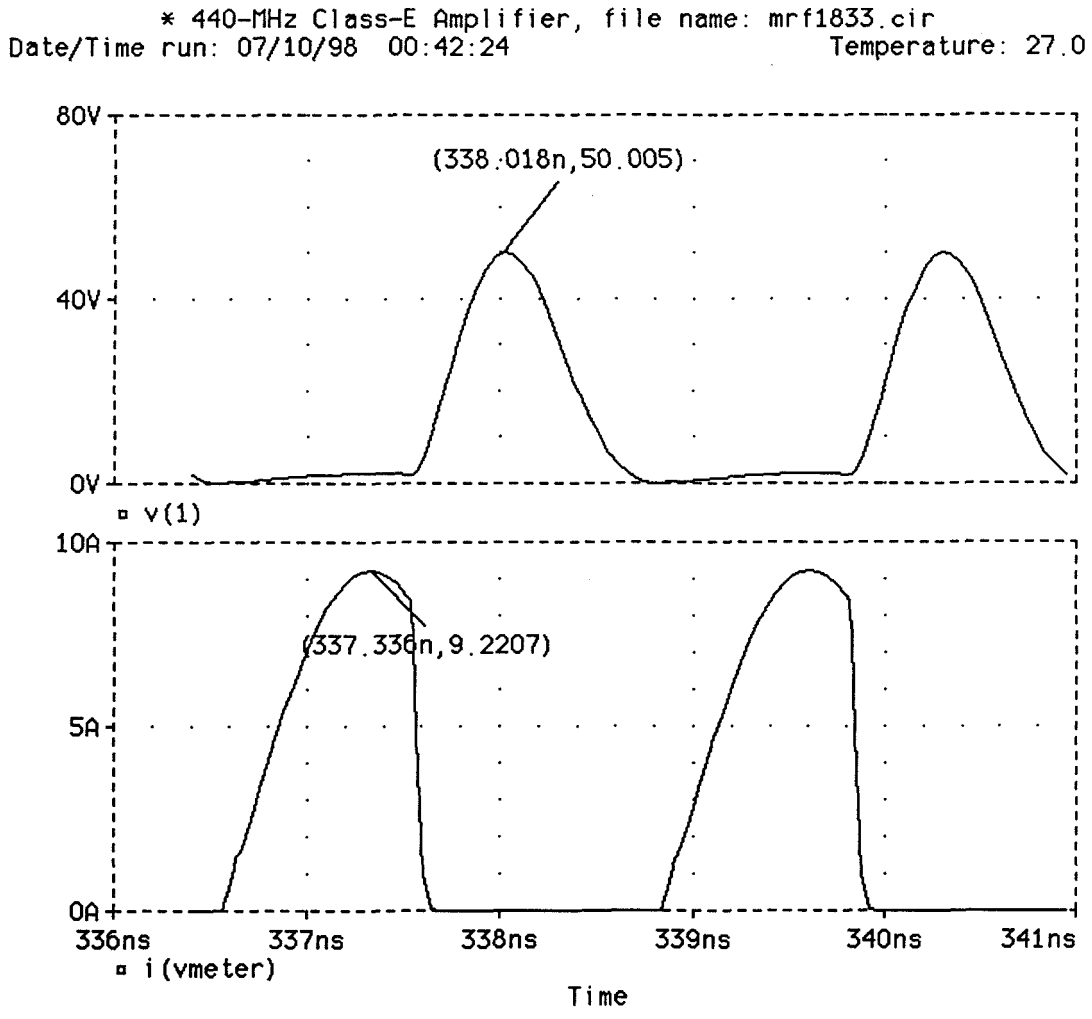

Figure 2.8 The 440-MHz Class-E amplifier PSpice simulation of switch voltage and current waveforms with device MRF183 MOSFET, $L = 5.5\,\text{nH}$, $C = 29\,\text{pF}$, $R = 1.6\,\Omega$.

36 W to 15 W, which is more than 4 dB. The reason why the output power is so sensitive to the value of L is that Q of the output load network is high. Q is defined as

$$Q = \frac{2\pi f L}{R}, \tag{2.18}$$

where f is the operating frequency. For the Class-E amplifier, $f = 440\,\text{MHz}$, $L = 5.5\,\text{nH}$, and $R = 1.6\,\Omega$. Plugging them in the above equation gives $Q = 10$ which is high. If the Q is lowered by half, the output power will not be that sensitive to L and it will be much easier to tune the circuit.

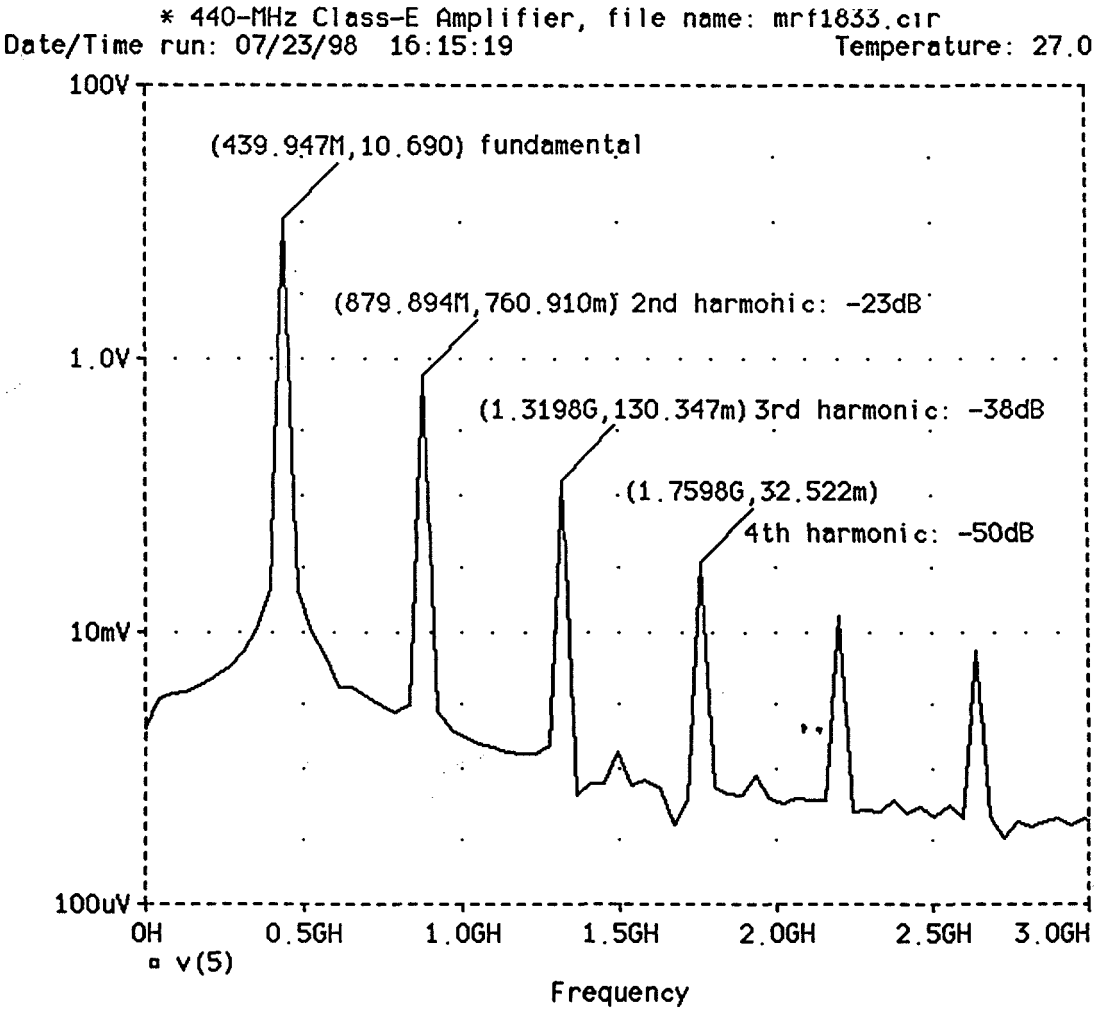

Figure 2.9 The 440-MHz Class-E amplifier PSpice simulation of the output power spectrum.

The output series capacitance C can tune the output power and the drain efficiency too. In Figure 2.11, PSpice simulates the output power and drain efficiency versus the series capacitance C with L and R fixed. Again the output power and efficiency do not peak at the same capacitance. When $C = 27\,\text{pF}$, the output power has a maximum value of 43 W and the corresponding drain efficiency is 71%. When $C = 35\,\text{pF}$, the drain efficiency peaks at 93% and the output power is 15 W. When C increases from 29 pF to 35 pF, the drain efficiency increases from 83% to 93%, but the output power drops from 44 W to 16 W.

In the Class-E amplifier, when the circuit components are fixed, the output power is determined by the drain-source bias voltage and it is proportional to the drain-source bias voltage squared. In Figure 2.12 the simulated output power in solid line can be represented by the following formula

$$P_{\text{out}} = V_{\text{dd}}^2/6.1\,\Omega, \tag{2.19}$$

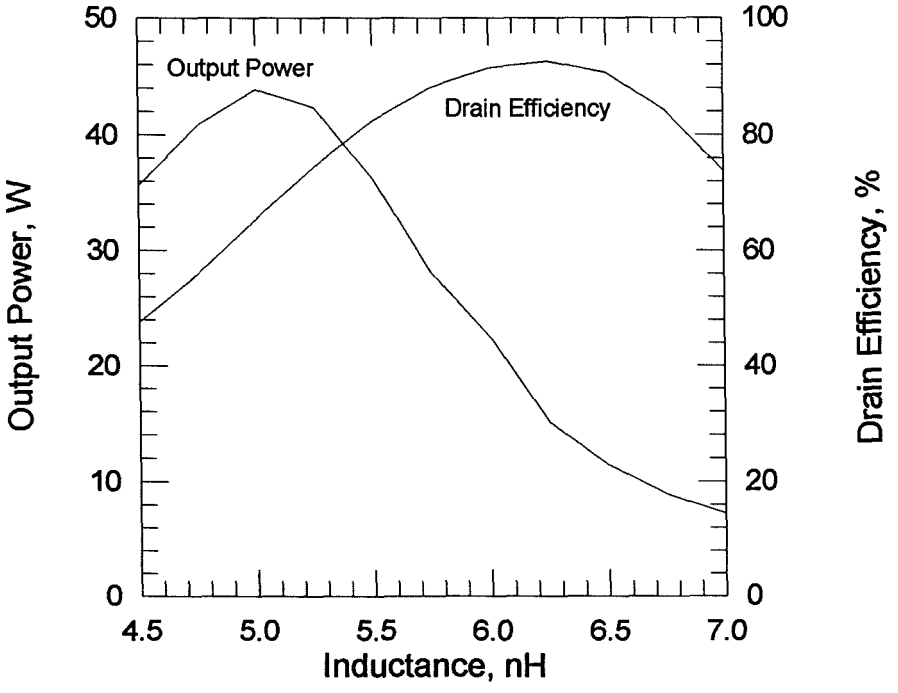

Figure 2.10 The 440-MHz Class-E amplifier PSpice simulation of the output power and drain efficiency versus the output series inductance L with $C = 29\,\text{pF}$, $R = 1.6\,\Omega$.

where P_{out} is the RF output power and V_{dd} is the drain-source bias voltage. The fitting curve with Equation (2.19) is shown by the dash line. Equation (2.19) shows that the output power is proportional to the drain-source bias voltage squared, i.e. the DC power. At the same time, the drain efficiency is not sensitive to the drain-source bias voltage. It is shown in Figure 2.12 that when the drain-source bias voltage increases from 5 V to 20 V, the output power increases from 3.6 W to 67 W, but the drain efficiency only decreases about 5% from 86% to 81%.

The bandwidth of the amplifier is affected by the quality factor Q and it is inverse proportional to Q. This is also true for the Class-E amplifier. The effect of the output load network Q on the bandwidth of the Class-E amplifier can be shown in PSpice simulation. In the PSpice simulation, two values of Q are selected, one is 5 and the other is 10. The bandwidths for these two cases

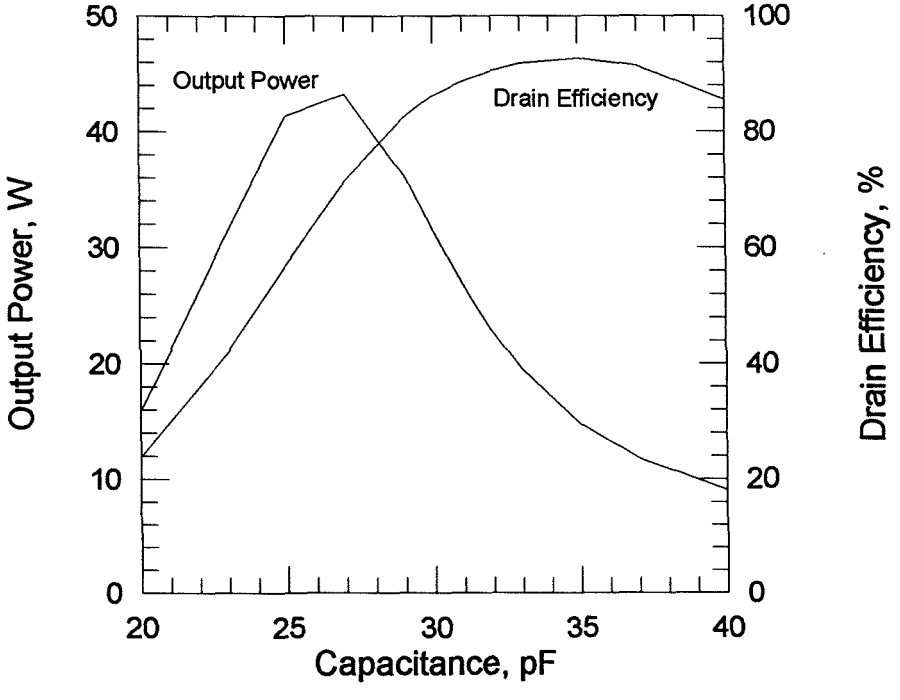

Figure 2.11 The 440-MHz Class-E amplifier PSpice simulation of the output power and drain efficiency versus the output series capacitance C with $L = 5.5\,\text{pF}$, $R = 1.6\,\Omega$.

are compared. Figure 2.13 shows the output power and drain efficiency with Q of 5 and 10. When Q is 5, the 3-dB bandwidth is about 200 MHz. When Q is 10, the 3-dB bandwidth is 90 MHz which is about half the bandwidth with Q of 5. When Q is low, it is easier to tune the output load network. But if it is too low, there will be large harmonic currents flowing through the load and filters will be needed. When Q is high, the harmonic current through the load is low but it is harder to tune the output load network.

Once L, R and C are determined, a network is needed to transform the 50 Ω load to the desired load R of 1.5 Ω. The simplest network is a shunt capacitor for the transformation. Figure 2.14 shows a parallel circuit and a series circuit. Assume the two circuits are equivalent at a specified frequency. Define the quality

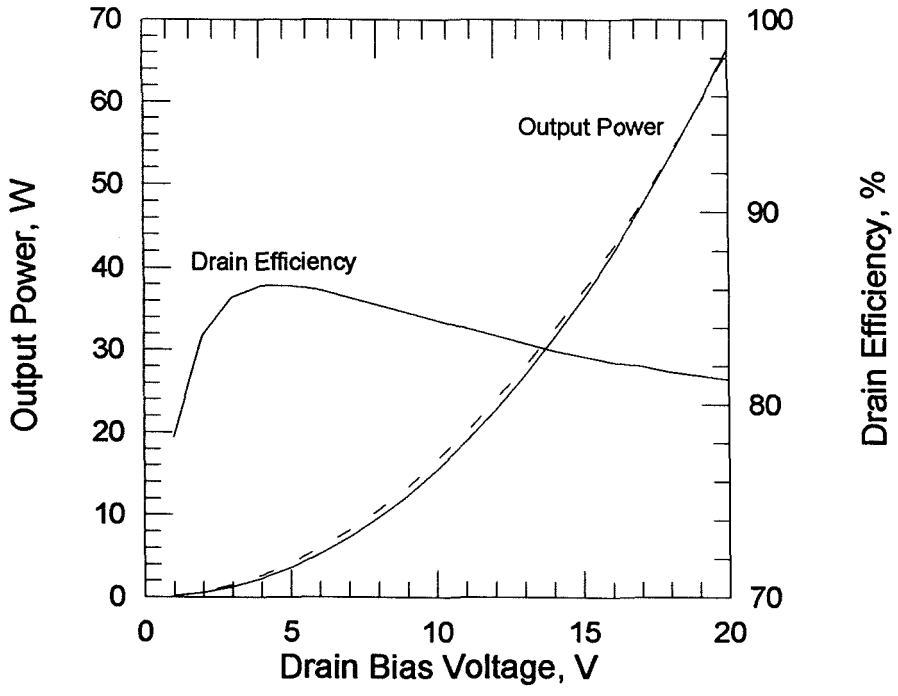

Figure 2.12 The 440-MHz Class-E amplifier PSpice simulation of the output power and drain efficiency versus the drain-source voltage, $L = 5.5\,\text{nH}$, $C = 29\,\text{pF}$, and $R = 1.6\,\Omega$. ---: $P_{\text{out}} = V_{\text{dd}}^2/6.1\,\Omega$.

factor of the parallel circuit as

$$Q_{\mathrm{p}} = \frac{R_{\mathrm{p}}}{X_{\mathrm{p}}}, \tag{2.20}$$

and the quality factor of the series circuit as

$$Q_{\mathrm{s}} = \frac{X_{\mathrm{s}}}{R_{\mathrm{s}}}. \tag{2.21}$$

R_{s} and R_{p} are $50\,\Omega$ and $1.6\,\Omega$ respectively. It can be shown that

$$R_{\mathrm{s}} = \frac{R_{\mathrm{p}}}{Q_{\mathrm{p}}^2 + 1}, \tag{2.22}$$

then

$$Q_{\mathrm{p}} = \sqrt{\frac{R_{\mathrm{p}}}{R_{\mathrm{s}}} - 1}. \tag{2.23}$$

From Equation (2.20)

$$X_{\mathrm{p}} = \frac{R_{\mathrm{p}}}{Q_{\mathrm{p}}}. \tag{2.24}$$

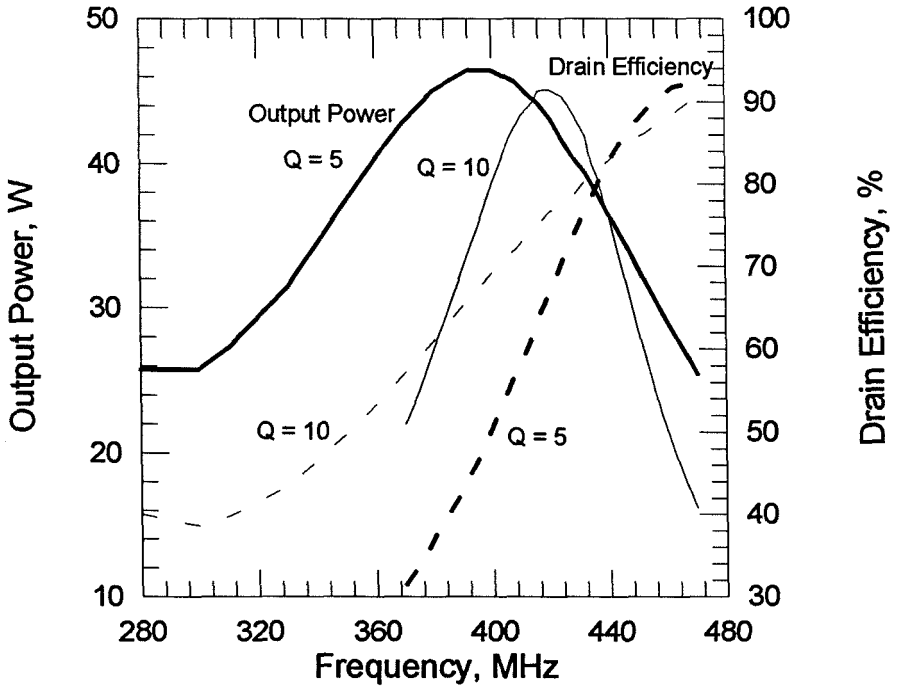

Figure 2.13 The 440-MHz Class-E amplifier PSpice simulation of frequency sweep. — output power. --- drain efficiency. Thick line: $Q = 5$. Thin line: $Q = 10$.

Substituting Q_p by Equation (2.23),

$$X_p = \frac{R_p}{\sqrt{\frac{R_p}{R_s} - 1}}. \tag{2.25}$$

Similarly,

$$X_s = \frac{X_p Q_p^2}{Q_p^2 + 1} = \sqrt{R_s(R_p - R_s)}. \tag{2.28}$$

Plugging in $R_s = 1.6\,\Omega$ and $R_p = 50\,\Omega$, the shunt capacitance is calculated to be 39.8 pF at 440 MHz.

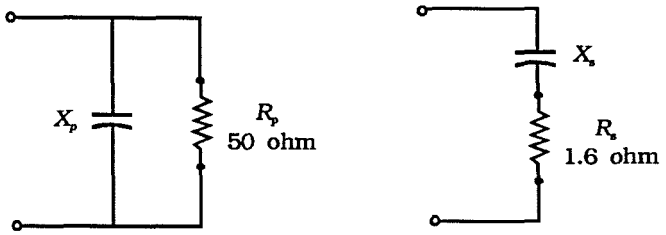

Figure 2.14 The impedance transformation network which transforms 50 Ω to 1.6 Ω.

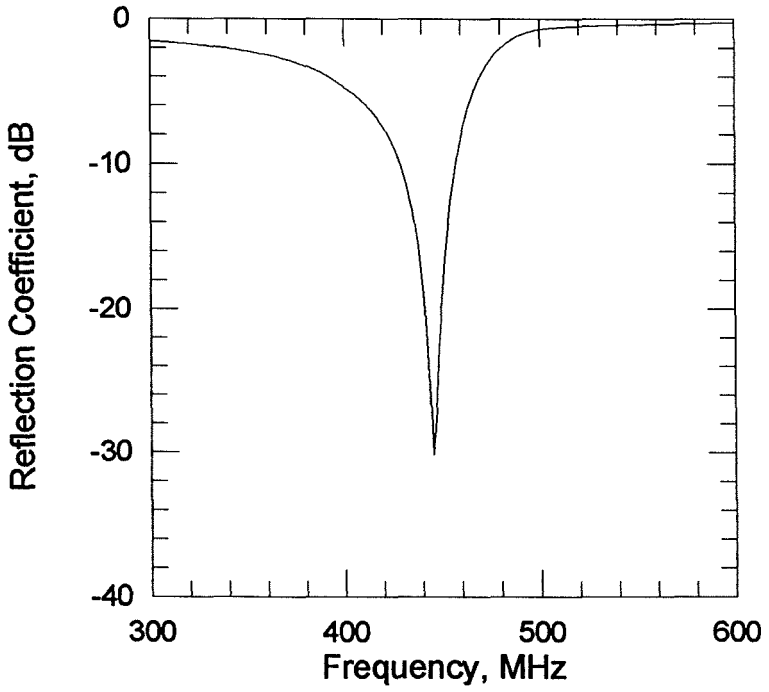

Figure 2.15 The 440-MHz Class-E amplifier input reflection coefficient simulation.

Following the output load network design is the input matching design. The small signal S-parameter given by Motorola is used as a starting point in the input matching design. The S_{21} parameter is attenuated by 3 dB to simulate the saturation of the device. The input impedance at the gate of the device with the output load network connected is simulated to be $1\,\Omega - j1.6\,\Omega$ at 440 MHz. This impedance is transformed to $50\,\Omega$ by a series inductance of 3 nH and a shunt capacitance of 51.5 pF. Figure 2.15 shows the reflection coefficient as a function of frequency in the input matching design. The plot shows that the bandwidth for the input matching circuit is very narrow. The bandwidth for the input reflection coefficient smaller than -10 dB is only 30 MHz. The Class-E amplifier circuit diagram including both the input and output is shown in Figure 2.16. At the output, C_2 transforms $50\,\Omega$ load to the desired load $1.6\,\Omega$ and together with L and C forms the output load network. At the input, L_1 and C_1 transform the input impedance at the gate to $50\,\Omega$.

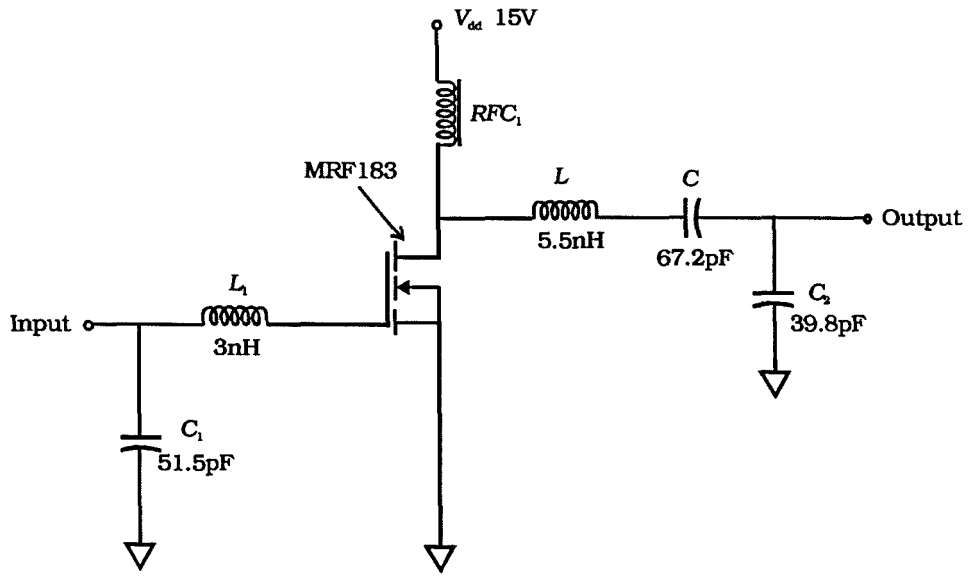

Figure 2.16 THe designed circuit of the 440-MHz Class-E amplifier. The output is designed by PSpice simulation and the input matching is designed using the S-parameter provided by Motorola.

2.4 MDS Simulation

The MDS simulation uses the proprietary nonlinear Root model for MRF183 MOSFET downloaded from the Motorola website [5]. The MDS circuit model for the 440-MHz Class-E amplifier is shown in Figure 2.17. The model includes both the output load network and the input matching circuit. The output load network is similar to that in PSpice simulation and consists of a series inductor L, a series capacitor C, and a load R. The input matching circuit includes a series inductor L_1 and a shunt capacitor C_1. RFC_1 and RFC_2 are RF chokes which block the RF signal. The gate bias voltage V_g is 0 V. In the simulation, all the capacitors and inductors are ideal, without loss.

The MDS simulation uses the component values from the PSpice simulation as the starting values and then change them for optimum design result. With the gate bias of 0 V, the drain bias of 15 V, and the input power of 3 W, L, C, and R are chosen so that they produce the drain voltage waveshape needed for

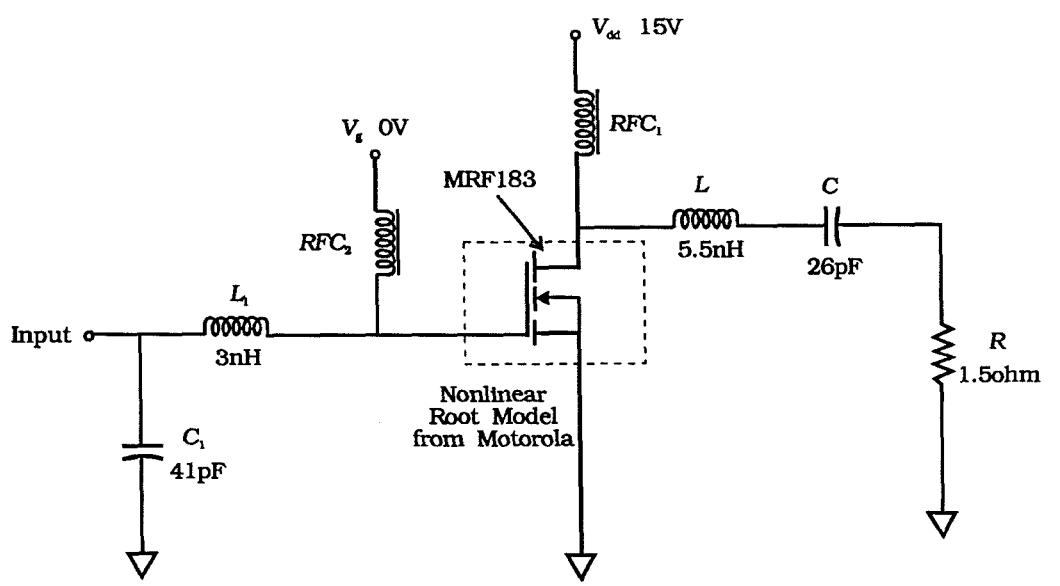

Figure 2.17 The MDS circuit model for the 440-MHz Class-E amplifier with MRF183 MOSFET.

the Class-E operation. In the PSpice simulation, both the current and voltage waveshapes can be monitored. But in the MDS simulation, since the nonlinear Root model for the device is a black box, the current waveshape through the switch cannot be monitored. The output load network is simulated to be $L = 5.5\,\text{nH}$, $C = 26\,\text{pF}$, and $R = 1.5\,\Omega$ in MDS. When the input power is 3 W, the output power is 37 W, the drain efficiency is 78%, and PAE is 72%. The drain and gate voltage waveforms are shown in Figure 2.18. The top one is the drain voltage waveform and the bottom one is the gate voltage waveform. Figure 2.19 gives the the output power spectrum in MDS simulation. The highest harmonic power is at the 2nd harmonic and it is about 25 dB lower than the operating frequency. This is the typical level that is observed in lower frequency Class-E amplifiers [7]. Table 2.1 summarizes the simulation results from both PSpice and MDS simulations. The two simulations give pretty similar results.

The PSpice simulation has shown that the output power and drain efficiency for the Class-E amplifier can be tuned by varying the output series inductance or the output series capacitance. Also PSpice simulation has shown that the output power of the Class-E amplifier is proportional to the DC power and the bandwidth is inversely proportional to Q of the output load network. Similar simulations are done in MDS. Since the MDS simulation includes both the output load network and the input matching circuit, we also simulate the output power and efficiency versus the input power.

Figure 2.20 shows how the output power, drain efficiency vary with the output series inductance. Similar to what we have in the PSpice simulation in Figure 2.10, the peak output power and peak drain efficiency do not achieve at the same output series inductance. By varying the inductance value, we can achieve the maximum output power at the expense of the drain efficiency, and vice versa. Figure 2.21 shows the output power and drain efficiency curves versus the output series capacitance in the MDS simulation. They are similar to those we get in

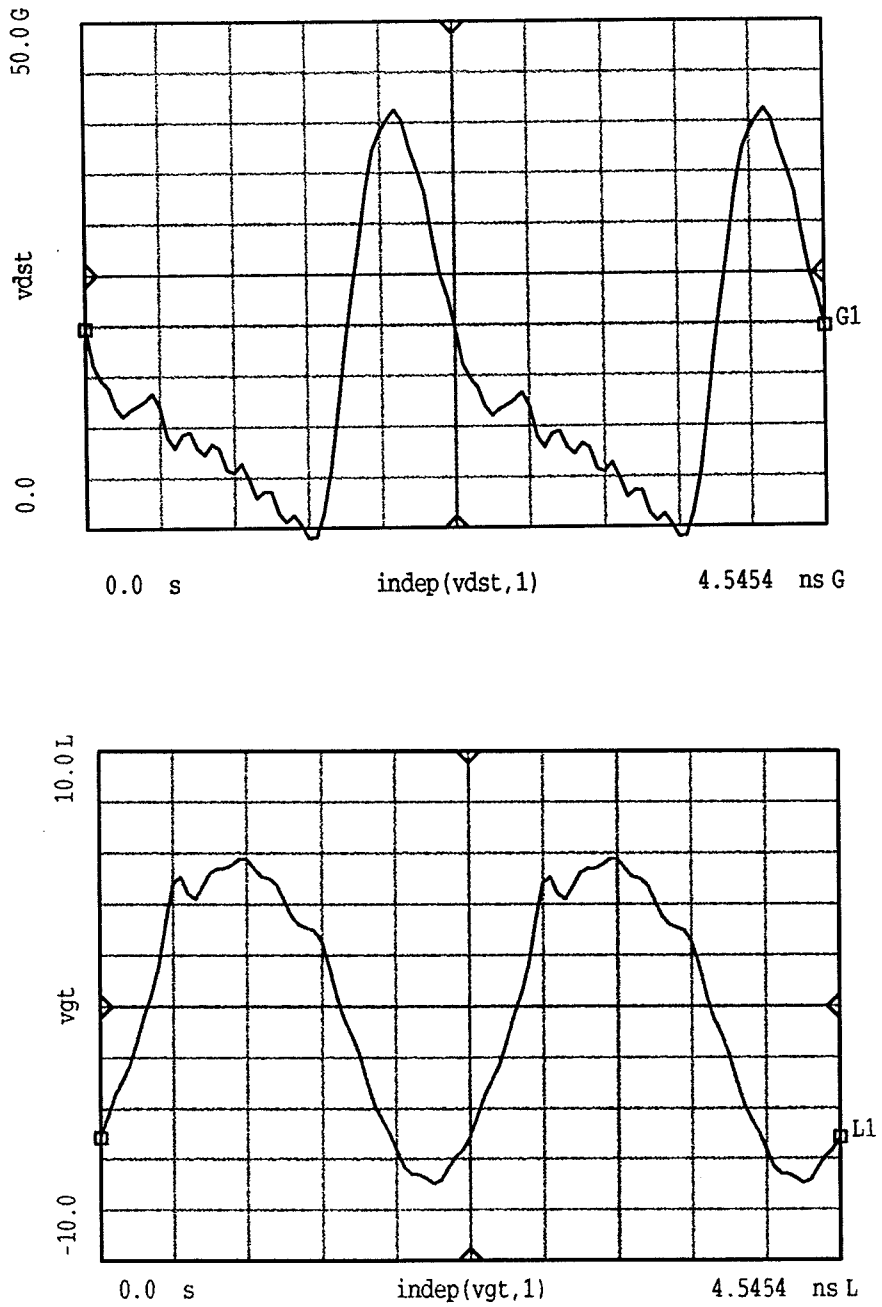

Figure 2.18 The MDS simulation of the 440-MHz Class-E amplifier drain and gate voltage waveforms. The top one is the drain voltage waveshape. The bottom one is the gate voltage waveshape.

the PSpice simulation as shown in Figure 2.11 qualitatively. Within a certain range, the smaller the series inductance is, the bigger the output power is but the lower the drain efficiency is. Again it shows that there is a trade-off between the output power and drain efficiency. Figure 2.22 shows the output power and drain efficiency versus the drain-source bias voltage. In the PSpice simulation in Figure 2.11, it has been shown that the output power is proportional to the DC power and

$$P_{\text{out}} = V_{\text{dd}}^2/6.1\,\Omega. \tag{2.19}$$

Here in Figure 2.22, similar curve fitting for the output power gives

$$P_{\text{out}} = V_{\text{dd}}^2/6.5\,\Omega. \tag{2.27}$$

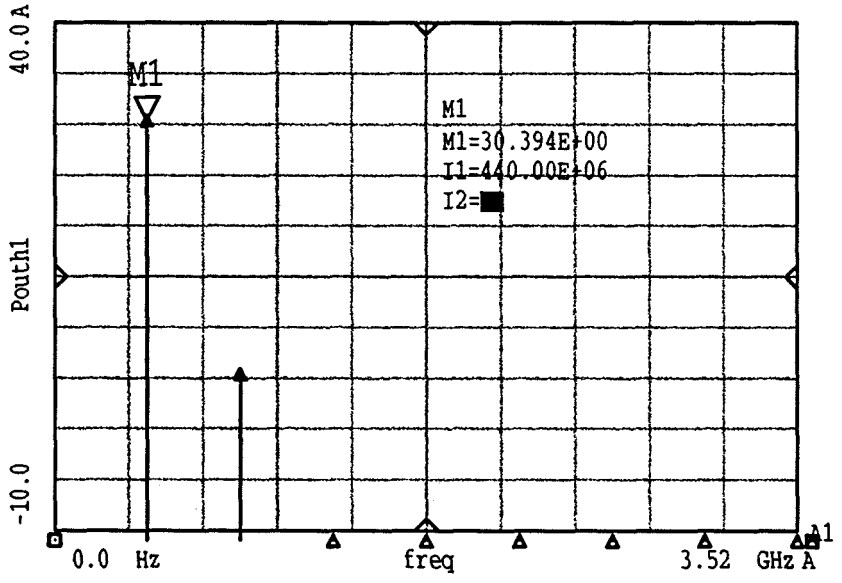

Figure 2.19 The MDS simulation of the 440-MHz Class-E amplifier output power spectrum.

	Frequency(MHz)	V_{dd}(V)	P_{in}(W)	P_{out}(W)	η_{D}(%)	PAE(%)	L(nH)	C(pF)	$R(\Omega)$
PSpice	440	15	–	36.2	82.5	–	5.5	29	1.6
MDS	440	15	3	36.7	78.3	71.9	5.5	26	1.5

Table 2.1 Comparison of PSpice and MDS simulations.

Again the output power is proportional to the drain-source bias voltage squared, i.e., the DC power. When the drain-source bias voltage increases, the output power increases, and the drain efficiency decreases only a bit.

Figure 2.23 shows the output power and drain efficiency versus the input power in the MDS simulation. When the input power is low, the drain efficiency is low because of the large on-resistance. As the input power increases, the drain efficiency increases since the on-resistance decreases. When the input power reaches 2 W, the device starts to saturate and the output drain-efficiency and the output power become flat.

A frequency sweep for the output power and drain efficiency in the MDS simulation is shown in Figure 2.24 with Q of 10 and 5. When Q is 10, the 3-dB bandwidth is 40 MHz; when Q is 5, the 3-dB bandwidth is 80 MHz. The simulated bandwidth in MDS is smaller than that in PSpice. In the PSpice simulation, the

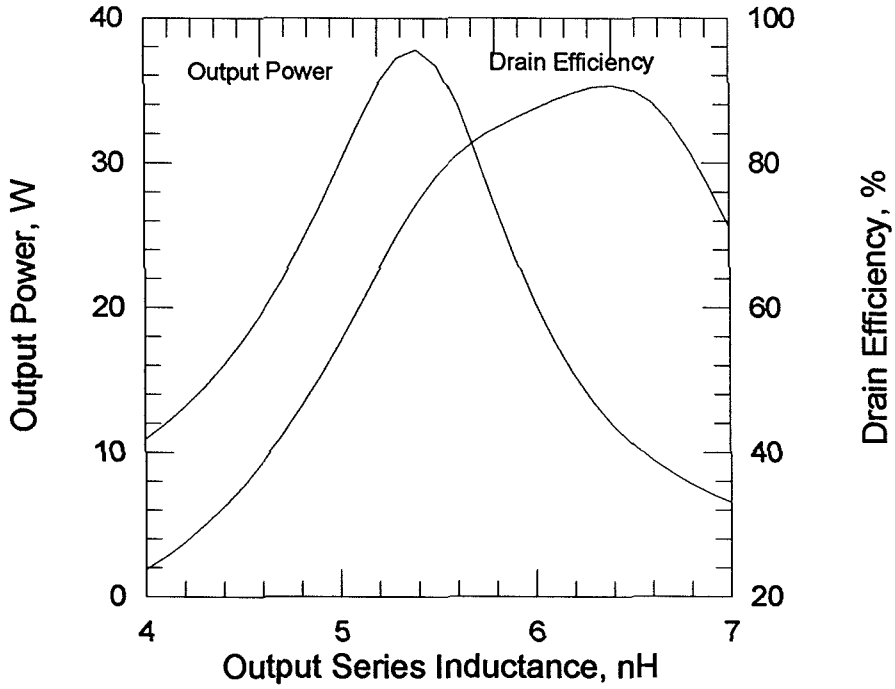

Figure 2.20 The MDS simulation of the 440-MHz Class-E amplifier output power and drain efficiency versus the output series inductance L, with $C = 26\,\text{pF}$, $R = 1.5\,\Omega$, $P_{\text{in}} = 3\,\text{W}$, $V_{\text{dd}} = 15\,\text{V}$, $V_{\text{gs}} = 0\,\text{V}$.

bandwidth is 90 MHz when Q is 10, and 200 MHz when Q is 5. The reason is that the input matching circuit is included in the MDS simulation and the input matching circuit decreases the bandwidth, while in the PSpice simulation the input matching circuit is not included.

2.5 Class-E Amplifier Construction

The picture of the 440 MHz Class-E amplifier is shown in Figure 2.25, and the amplifier circuit schematic diagram is shown in Figure 2.26. The circuit board is Duroid substrate with dielectric constant of 2.2 and thickness of 10 mil. The substrate is plated with copper on both sides. Metal patterns are cut on top of the board for soldering the components. The circuit board is mounted on a $3\times4\frac{1}{8}$-inch heat sink. A 1.5 mm deep and 6 mm wide slot is milled in the heat sink. The MRF183 MOSFET is mounted in the slot with two 2-56 screws. A few

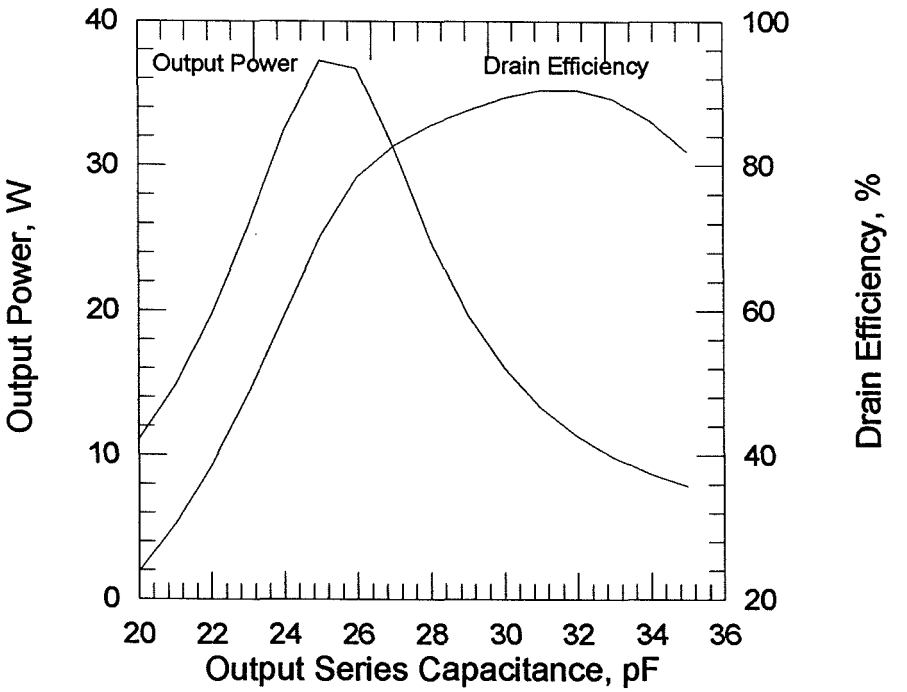

Figure 2.21 The MDS simulation of the 440-MHz Class-E amplifier output power and drain efficiency versus the output series capacitance C, with $L = 5.5\,\text{pF}$, $R = 1.5\,\Omega$, $P_{\text{in}} = 3\,\text{W}$, $V_{\text{dd}} = 15\,\text{V}$, $V_{\text{gs}} = 0\,\text{V}$.

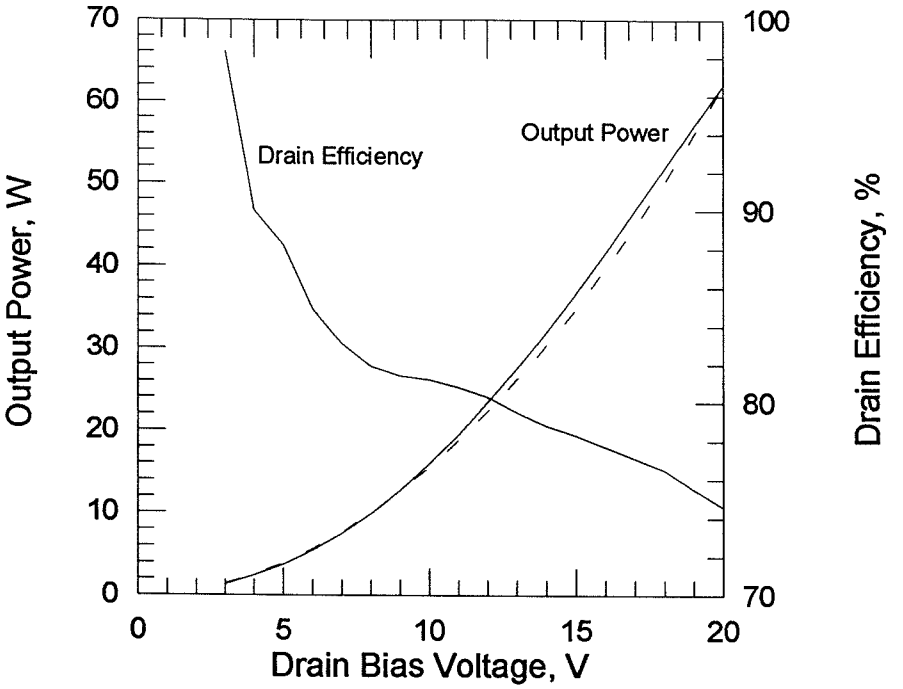

Figure 2.22 The MDS simulation of the 440-MHz Class-E amplifier output power and drain efficiency versus the drain-source supply voltage with $L = 5.5\,\text{nH}$, $C = 26\,\text{pF}$, $R = 1.5\,\Omega$, $P_{\text{in}} = 3\,\text{W}$, $V_{\text{gs}} = 0\,\text{V}$. — simulation of the output power. --- $P_{\text{out}} = V_{\text{dd}}^2/6.5\,\Omega$.

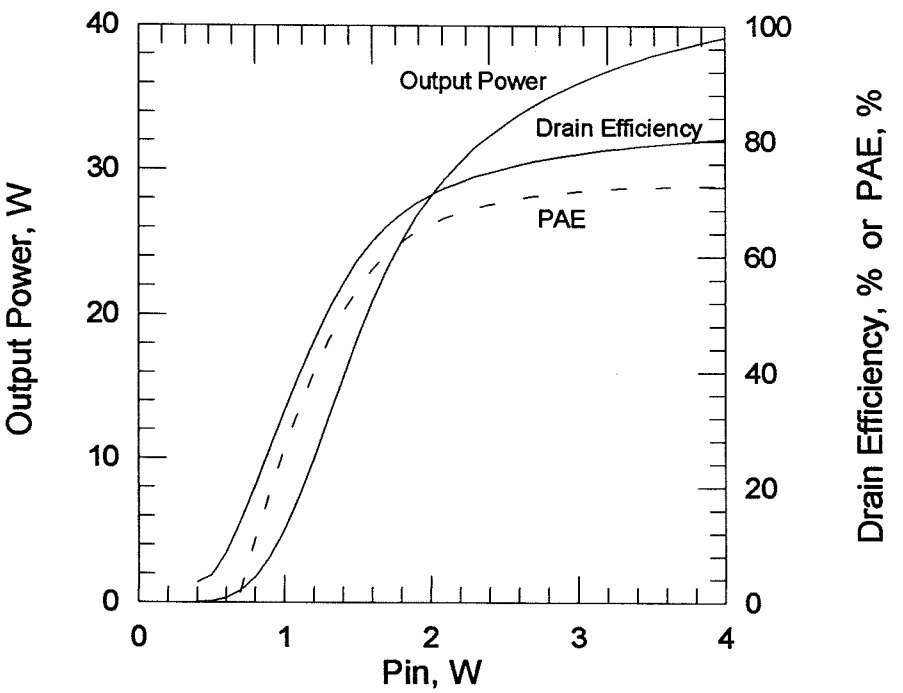

Figure 2.23 The MDS simulation of the 440-MHz Class-E amplifier input power sweep with $L = 5.5\,\text{nH}$, $C = 26\,\text{pF}$, $R = 1.5\,\Omega$, $V_{\text{gs}} = 0\,\text{V}$, and $V_{\text{dd}} = 15\,\text{V}$.

2-56 mounting holes are drilled on the circuit board and heat sink around the transistor so that there is a good connection between the source of the transistor and the ground.

Table 2.2 summarizes the components in the amplifier. RFC_1 and RFC_2 are RF chokes and made by winding gauge 18 wire on a drill bit $\frac{13}{64}$. RFC_1 blocks the RF current and contains a constant DC current. The inductance of the choke is measured to be about 100 nH at 440 MHz on the HP8510 network analyzer. C_{b1} and C_{b2} are bypass capacitors to protect the power supply from the RF signal. At the input, L_1 and the two capacitors C_1 and C_2 transform the input impedance at the gate to 50 Ω. RFC_1 and R_1 are added to help stabilize the amplifier. At the output, C_3 and C_4 transform the 50 Ω load to the load desired for the Class-E amplifier and together with L and C form the output load network. All the ATC

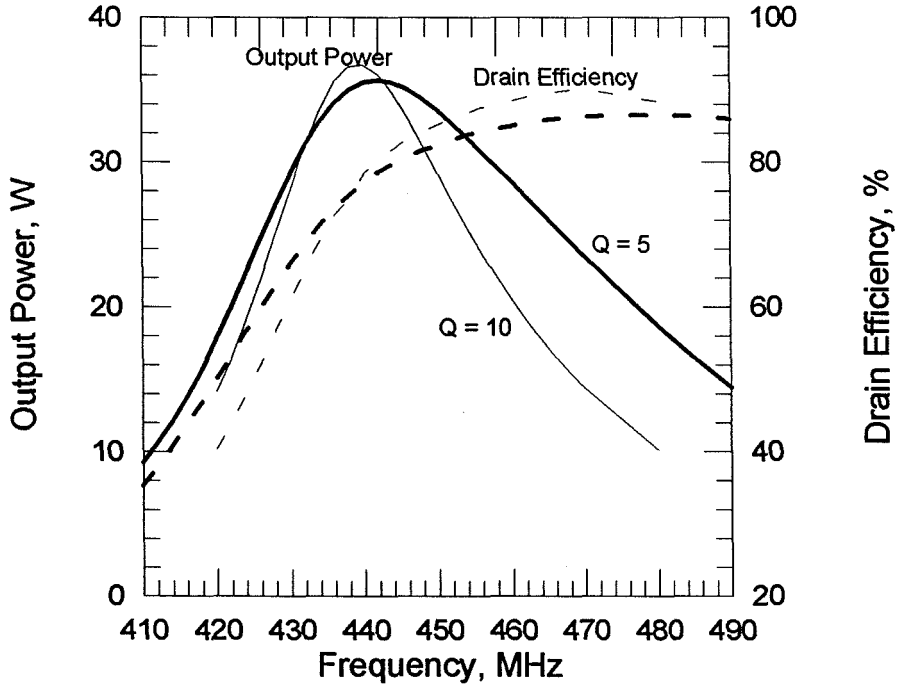

Figure 2.24 The MDS simulation of the 440-MHz Class-E amplifier frequency sweep of the output power and drain efficiency, with $L = 5.5$, $C = 26$ pF, and $R = 1.5\,\Omega$. $P_{in} = 3$ W, $V_{dd} = 15$ V, and $V_{gs} = 0$ V. — output power. --- drain efficiency. Thick line: $Q = 5$. Thin line: $Q = 10$.

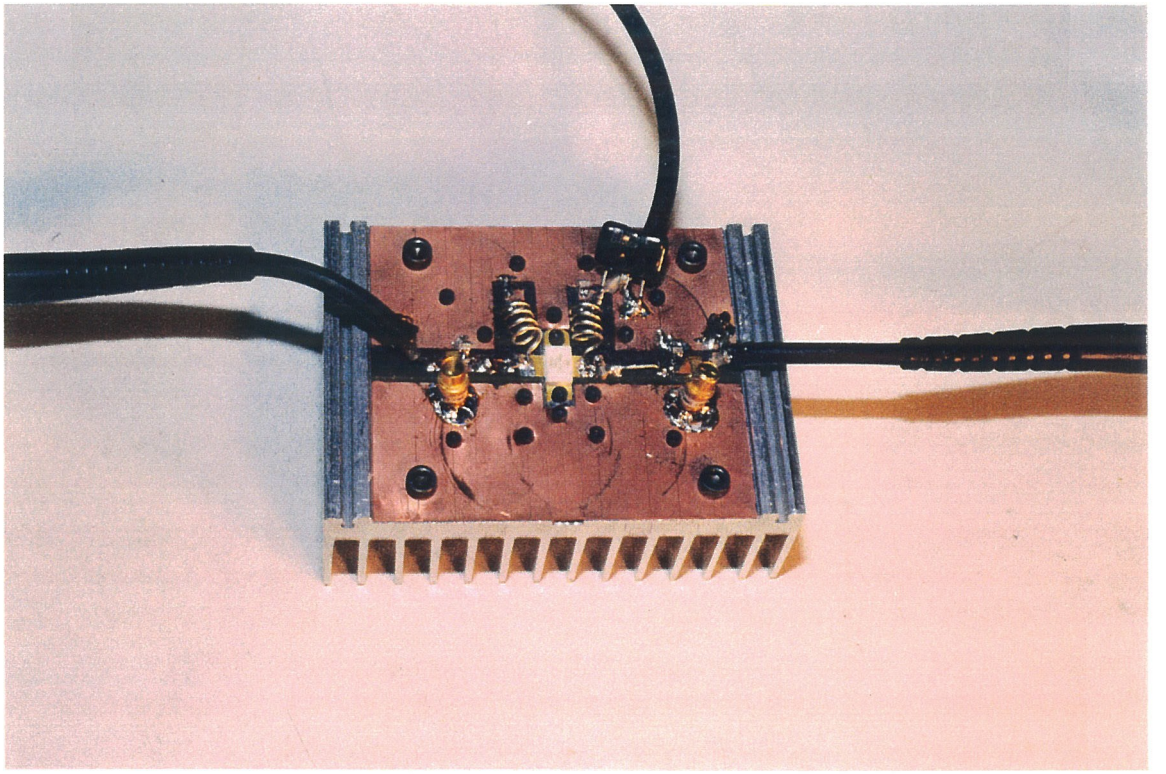

Figure 2.25 The picture of the 440-MHz Class-E amplifier.

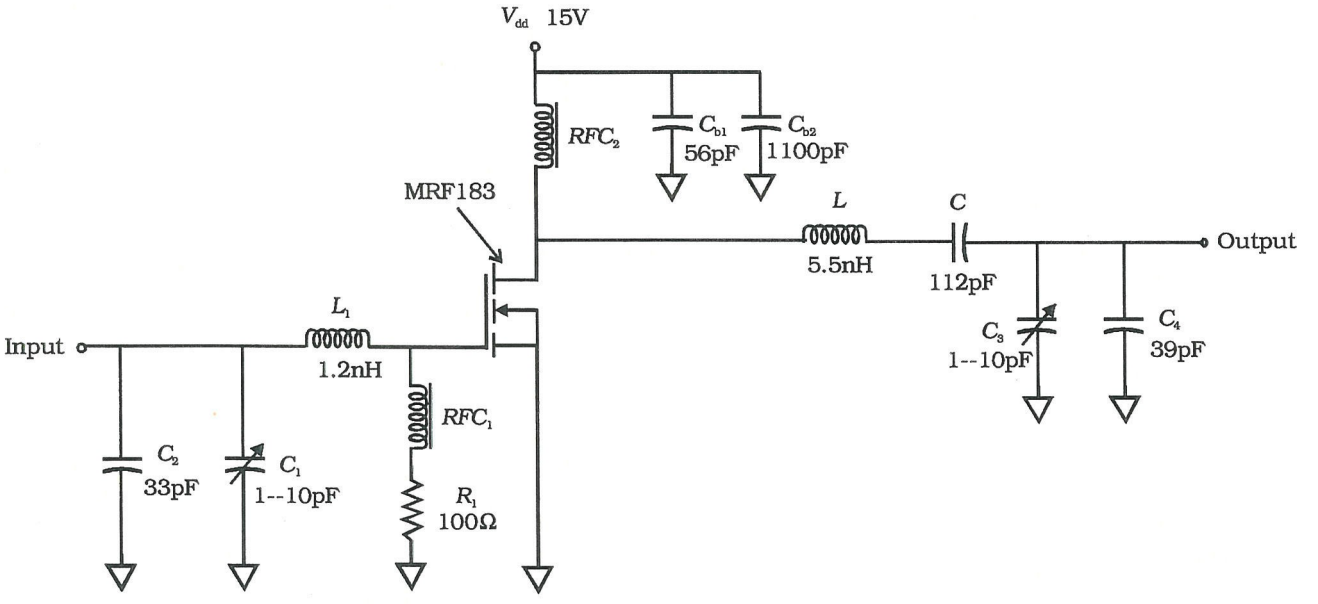

Figure 2.26 The 440-MHz Class-E amplifier circuit schematic diagram.

chip capacitors used in the circuit are 500 V capacitors. C_1 and C_3 are variable capacitors which are used to tune the input and output. L is a 10 mm long gauge 18 wire and it is 2 mm above the circuit board. Since the output power and efficiency are sensitive to the value of L, it is desirable to have a type of inductor which can be tuned easily. Professor Herbert Zirath came up with the idea of changing the inductance value by changing the height of the wire above the ground and he simulated the wire inductance [8] in MDS. Figure 2.27 shows the simulated inductance versus the height of the wire above the ground. The simulation shows that when the height is 2 mm, the inductance is about 4.1 nH.

2.6 Experimental Results

The measurement setup of the 440 MHz Class-E high efficiency amplifier is shown in Figure 2.28 and the schematic diagram of the setup is shown in

Component	Description
L_1	1.5 nH Toko chip inductor with maximum DC current of 1 A,
	$Q = 13$ @ 100 MHz and $Q = 47$ @ 800 MHz
C_1	1–10 pF Johanson 1585 tuning capacitor, $Q > 4000$ @ 195 MHz
C_2	39 pF ATC chip capacitor, $Q > 50$ @ 900 MHz
R_1	100 Ω chip resistor
RFC_1	4-turn loop by winding gauge 18 wire on drill bit $\frac{13}{64}$
L	10 mm long gauge 18 wire, 2 mm above the ground
C	two 56 pF ATC chip capacitors in parallel, $Q > 50$ @ 900 MHz
C_3	1–10 pF Johanson 1585 tuning capacitor, $Q > 4000$ @ 195 MHz
C_4	39 pF ATC chip capacitor, $Q > 50$ @ 900 MHz
RFC_2	4-turn loop by winding gauge 18 wire on drill bit $\frac{13}{64}$
C_{b1}	56 pF ATC chip capacitor, $Q > 50$ @ 900 MHz
C_{b2}	1000 pF mica capacitor

Table 2.2 The 440-MHz Class-E amplifier circuit components.

Figure 2.29. The Bird Power Meters measure the RF powers at the input and output of the amplifier. These meters have an accuracy of 5%. The YAESU transceiver is used as the driver of the amplifier. A 6 dB attenuator is connected after the YAESU transceiver to protect the transceiver from the reflected power of the amplifier during the measurement. Multimeters are used to measure the DC drain-bias voltage and the corresponding DC current. During the measurement, there is a fan blowing air to the amplifier.

At the beginning of the measurement, the 100 Ω chip resistor (R_1) and the 4-turn loop RF choke (RFC_1) are not connected at the gate of the device and an oscillation at 47 MHz is observed. Adding RFC_1 only, the oscillation still exits. Adding R_1 in series with RFC_1 kills the oscillation.

We have tried different output inductance. When the height of the 10 mm long gauge wire is 2 mm and the input power is 1.4 W, the drain efficiency is

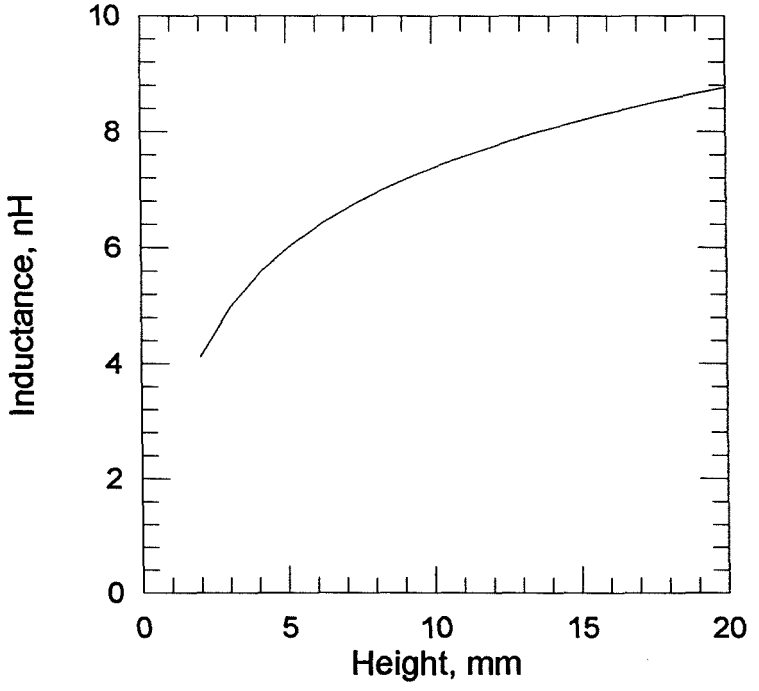

Figure 2.27 The MDS simulation of the inductance of the 10 mm long, gauge 18 wire versus the height above the substrate. Courtesy of Prof. Herbert Zirath.

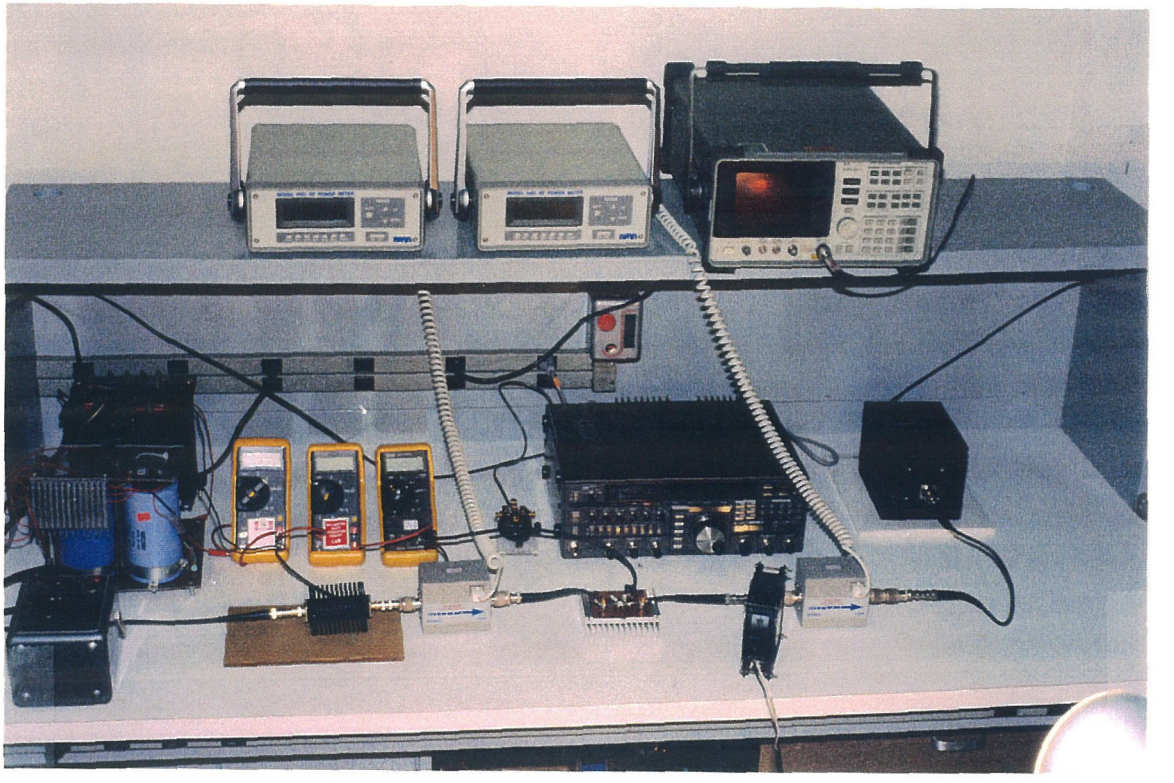

Figure 2.28 The 440 MHz Class-E amplifier measurement setup.

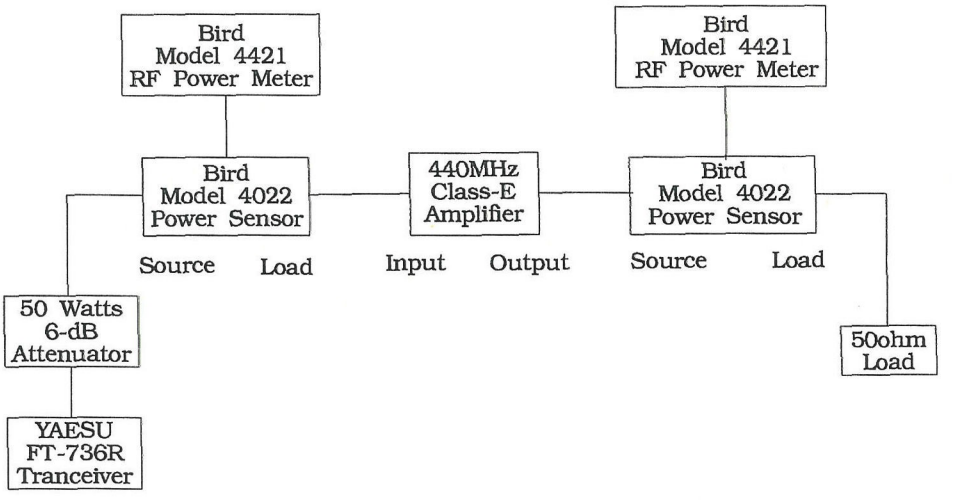

Figure 2.29 The schematic diagram of the 440-MHz Class-E amplifier measurement setup.

77%, the power-added efficiency is 70%, the output power is 15 W, and the gain is 10.3 dB. A spectrum analyzer is connected at the output of the amplifier with a 50 dB attenuator between the amplifier output and the spectrum analyzer to protect the spectrum analyzer. The measured spectrum of the amplifier is shown in Figure 2.30. The output power of the second harmonic is measured more than 35 dB below that of the fundamental frequency. Figure 2.31 shows the measurement result when the input power varies from 0.3 W to 2.2 W. Figure 2.32 shows the measurement result when the drain-source bias voltage varies from 6.5 V to 20 V with the input power of about 1.45 W. The output power is proportional to the drain-bias voltage squared and it is

$$P_{\text{out}} = V_{\text{dd}}^2/22.2\,\Omega. \tag{2.28}$$

When the output power increases, the VSWR increases with it. The drain efficiency is flat and the power added efficiency increases when the drain bias increases since the gain increases. In Figure 2.33, the frequency sweeps from

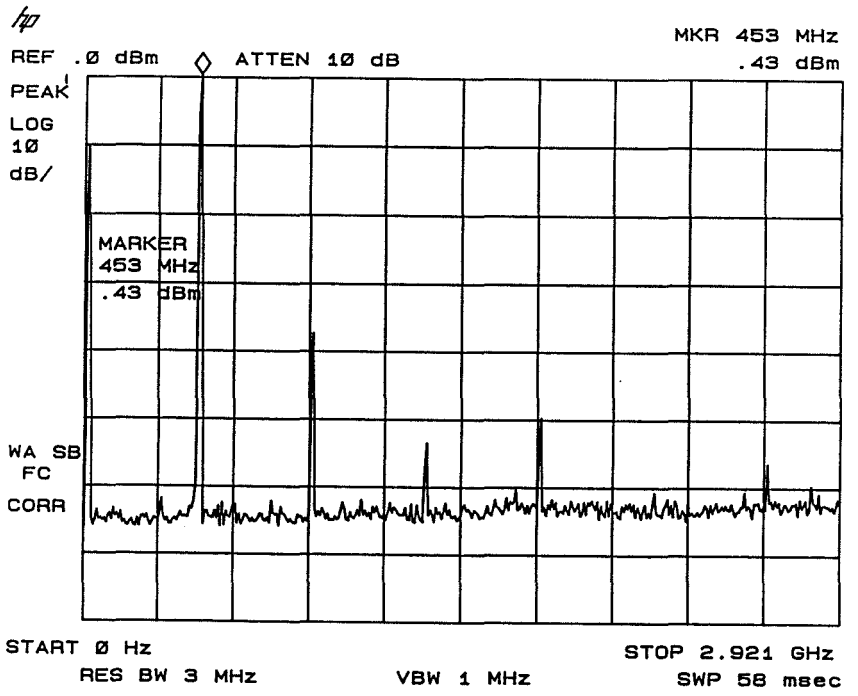

Figure 2.30 The measured spectrum of the 440 MHz Class-E amplifier circuit with MRF183 MOSFET.

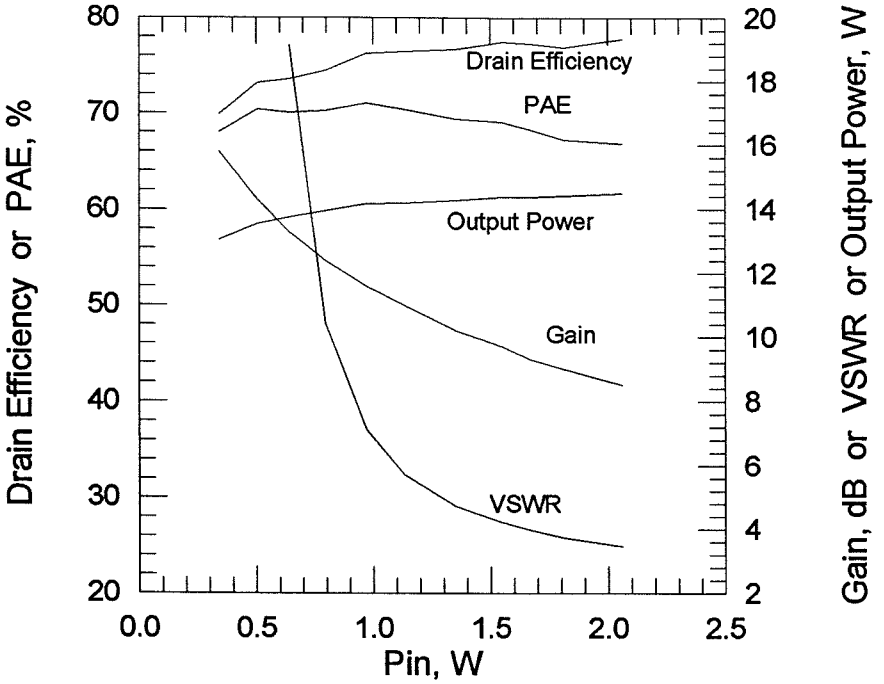

Figure 2.31 The measurement result of the input power sweep for the 440-MHz Class-E amplifier with MRF183 MOSFET, $V_{dd} = 18.3\,V$.

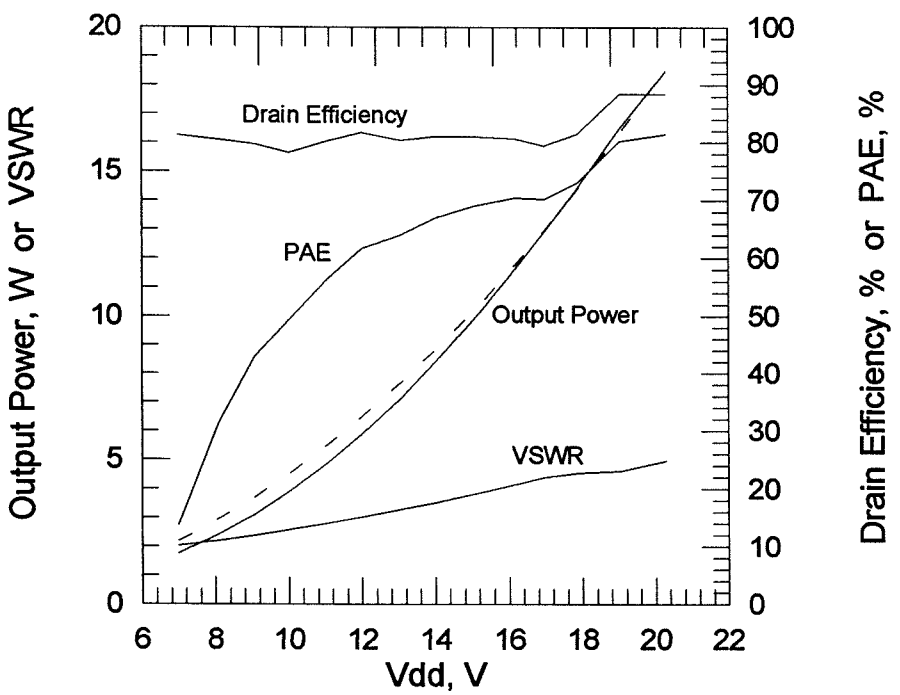

Figure 2.32 The measurement result of the drain-source supply voltage sweep for the 440-MHz Class-E amplifier with MRF183 MOSFET. The RF input power $P_{in} = 1.45\,W$. --- $P_{out} = 0.045V_{dd}^2$.

430 MHz to 450 MHz which is the frequency range of the YAESU transceiver. When the frequency increases from 430 MHz to 450 MHz, the output power decreases and the drain efficiency increases. This agrees with both PSpice and MDS simulations. The input VSWR is high when the frequency is between 430 MHz and 435 MHz.

2.7 Discussion

In this section we discuss some issues encountered in the design and measurement of the Class-E amplifier, such as the selection of Q of the output load network, the measured high VSWR at the input, comparison of the PSpice and MDS simulations.

2.7.1 Selection of Q of Output Load Network

In the beginning of the design, the output series inductance is designed to be

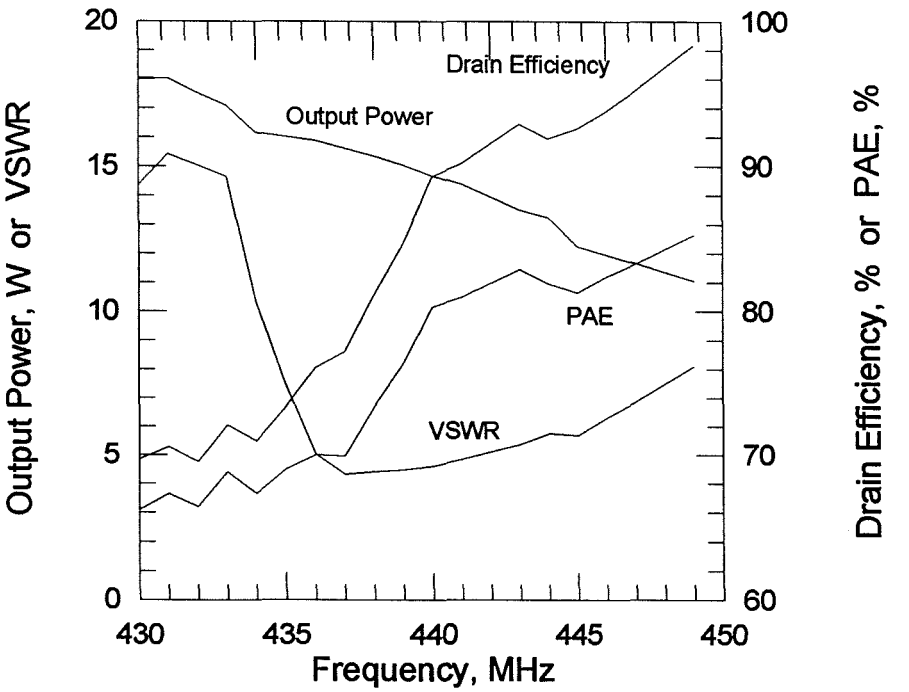

Figure 2.33 The measurement result of the frequency sweep for the 440-MHz Class-E amplifier with MRF183 MOSFET.

11 nH, the output series capacitance 12.5 pF, and the load 1.5 Ω. For $L = 11$ nH and R =1.5 Ω, Q is about 20 at 440 MHz. As a comparison, for the 13.56-MHz 400-W Class-E amplifier [9], Q is 3.7. In general the bandwidth of an amplifier is inversely proportional to Q. This is also true for the Class-E amplifier. It is hard to tune the Class-E amplifier with Q of 20. Q can be lowered by reducing the output series inductance and keeping the same load. If the output series inductance is reduced to 5.5 nH with the same load of 1.5 Ω and the corresponding series capacitance of 29 pF, Q becomes 10. In this case the PSpice simulation gives similar current and voltage waveshapes, output power and drain efficiency If Q is further reduced to 5, the resulting output series inductance becomes 2.75 nH and the output series capacitance becomes 60 pF with a load of 1.5 Ω. But when the shunt capacitance transforms the 50 Ω load to 1.5 Ω, the resulting series capacitive reactance is bigger than that of 60 pF. So in the final circuit, Q is selected to be 10 and the output series inductance is 5.5 nH.

2.7.2 High VSWR at the Input of the Class-E Amplifier

In the measurement, we found the VSWR is high at the input of the amplifier. This may happen when the output power couples back to the input through the miller capacitor between the gate and the drain. The high VSWR at the input agrees with the input matching design in the MDS simulation. When the component values for the input matching circuit are selected to match the input, the efficiency and the output power are not optimal. When the component values for the input matching circuit are taken to optimize the efficiency and the output power, the input is not matched. More work needs to be done on the input matching.

2.7.3 Comparison of PSpice and MDS Design Approaches

In the design of the Class-E amplifier, two methods are used. One is PSpice and the other is MDS. In the PSpice simulation, the device is modelled as a

	Frequency(MHz)	P_{out}(W)	η_D(%)	PAE(%)
MDS	440	16	79	72
Measurement	440	15	77	70

Table 2.3 Comparison of the MDS simulation and the measurement results of the 440-MHz Class-E amplifier with MRF183 MOSFET.

switch in parallel with the output capacitance of the device. In the MDS simulation, the nonlinear Root model of the device is used and the output load network and the input matching circuit are designed at the same time. Table 2.1 gives a comparison of the simulation results from these two methods and they are pretty close. The advantage of the PSpice simulation is that it uses a simple switch model and does not require the nonlinear model of the device. The disadvantage is that it cannot predict the gain and PAE and it cannot design the input matching circuit. For the MDS simulation, it needs the nonlinear model of the device but it can give a more complete design. It can simulate the gain and PAE besides output power and drain efficiency and it can be used to design the input matching circuit where PSpice model fails.

2.7.4 Comparison of Theory and Measurement

Table 2.3 compares the MDS simulation and the measurement results of the 440-MHz Class-E amplifier with MRF183 MOSFET. The losses of the capacitors and inductors at the output are included in the MDS simulation. In Figure 2.26, Q of the output series inductance L is simulated to be 200. According to the manufacturer, Q of the output series capacitance C is around 35, and Q of the shunt capacitance C_4 is around 200. From the table we see that the simulation agrees very well with the measurement.

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Chapter 3

X-Band Microstrip Class-E High Efficiency Amplifier

Since the introduction of Class-E high efficiency amplifiers [1]–[3], several Class-E circuits have been developed at microwave frequencies. Tom Mader [4] first developed the Class-E amplifiers at 0.5, 1, 2, and 5 GHz. He also integrated the 5-GHz Class-E amplifier and an active-antenna and demonstrated a 2×2 power-combining array [4]. At 5 GHz, 81% drain efficiency and 72% power added efficiency are measured with an output power of 0.61 W using the Fujitsu FLK052WG MESFET device [5]. At 5.05 GHz the 2x2 power-combing Class-E amplifier array delivers a total of 2.4 W of output power with a DC-RF conversion efficiency of 74% and a power added efficiency of 64%. A 5-GHz Class-E high efficiency oscillator with a maximum conversion efficiency of 59% and output power of 300 mW was presented in [6].

In this chapter we present two X-band Class-E high efficiency amplifiers. In the Class-E amplifier, the transistor is driven as a switch and connected to a passive load network. The transistor is modelled as a switch in parallel with the output capacitance of the transistor. The output capacitance is extracted by measuring the output impedance with the transistor pinched off. Subsequently the switch model of the transistor is used in the PSpice [7][8] simulation and the output load network is determined by the PSpice simulation in time domain. Two X-band microstrip Class-E high-efficiency amplifiers designed by the above approach are demonstrated. The first one uses Fujitsu FHX35X HEMT transistor [5] and achieves an output power of 30 mW, drain efficiency of 80% and

PAE (power-added efficiency) of 64%. The second one uses Fujitsu FLR056XV MESFET transistor [5] and delivers an output power of 186 mW, drain efficiency of 72% and PAE of 56%. The measurement results are compared with the data given by Fujitsu for Class-A mode operation, showing that Class-E mode operation has higher efficiency and lower gain than Class-A mode operation.

In the Class-E amplifier circuit proposed by Sokals [2], as shown in Figure 3.1, the components are lumped elements. At microwave and millimeter-wave frequencies, transmission lines are often preferred over lumped elements because the losses of the transmission lines are less. Therefore as in [4], L and C in Figure 3.1 are replaced by a series transmission line and a shunt transmission line for these two X-band amplifiers, which is shown in Figure 3.2. Transmission lines are also used for the input matching. Both amplifiers are fabricated on the Duroid substrate with dielectric constant of 2.2 and thickness of 0.254 mm. After the circuit fabrication the dimensions of the transmission lines are not adjusted.

3.1 Circuit Model for Class-E Amplifier

In the Class-E amplifier, the device can be modelled as a switch in parallel with a capacitance C_s which is the output capacitance of the device as shown in Figure 3.3. The switch has on and off-resistance and the circuit models for on and

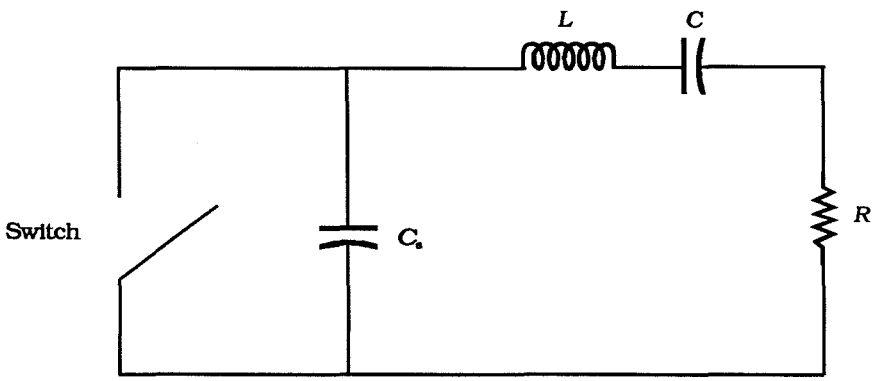


Figure 3.1 The Class-E amplifier circuit.

off states are shown in Figure 3.4. During the transistor off-state, since the off-resistance is usually big, the output looks primarily reactive and the transistor looks like a capacitor at its output port, as shown in Figure 3.4(a). During the on-state, because the on-resistance is usually in the order of a few ohms, so the transistor looks like a small resistor, as shown in Figure 3.4(b). The on-resistance can be estimated from the transistor's $I-V$ curve and the off-resistance is assumed to be big. The most important parameter to be determined is the output capacitance of the transistor, because it has big effect on the design of the output load network which determines the waveshapes of the current and voltage across the switch and directly affects the efficiency of the amplifier. The output capacitance C_s is measured by biasing the transistor at its pinched-off state. When the transistor is pinched off, the resistive part of the output circuit can be ignored and only the capacitance is left. By measuring the output impedance using a network analyzer and fitting the phase angle of the measured output impedance, the capacitance can be extracted.

After the determination of the output capacitance, the output load network can be designed. Subsequently the input matching is designed using the small

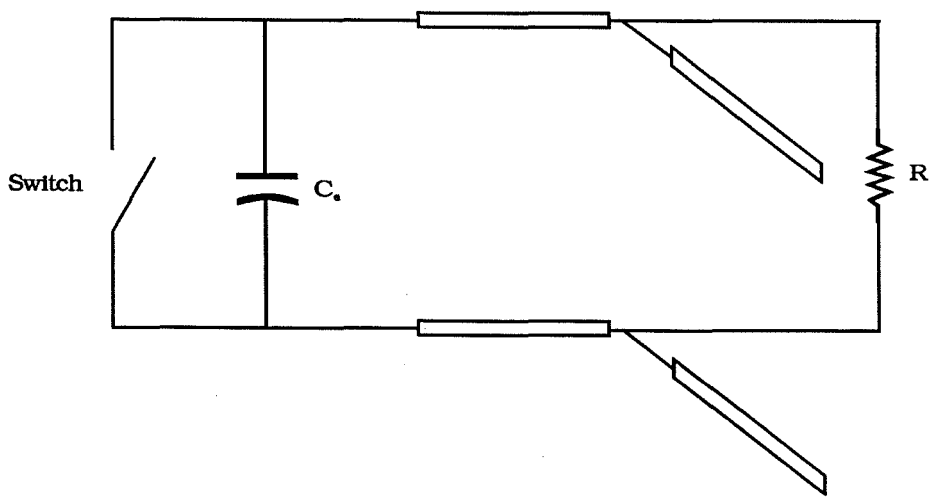


Figure 3.2 Class-E circuit with series/shunt transmission lines.

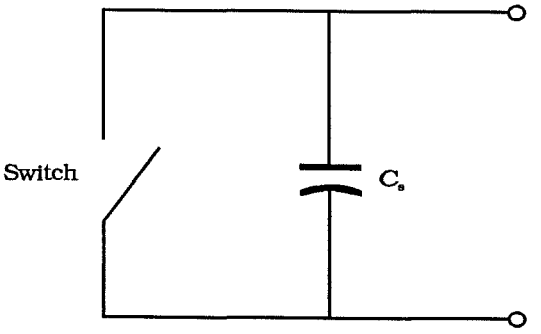


Figure 3.3 Transistor output circuit model in Class-E operation. C_s is the output capacitance of the transistor.

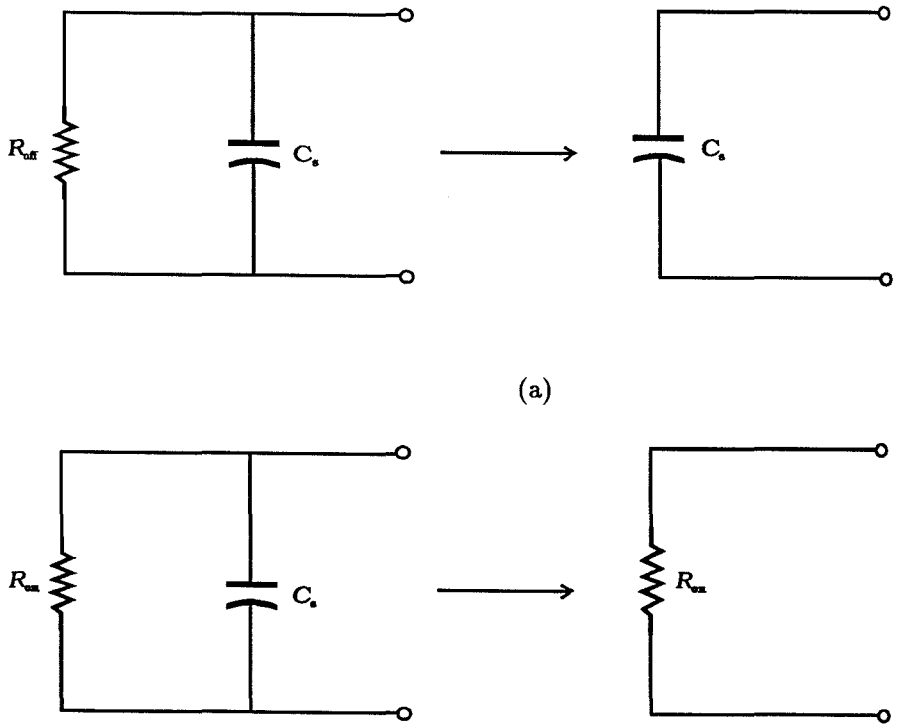


Figure 3.4 Transistor output circuit models for on and off states. (a) Off state. (b) On state.

signal S-parameter with the magnitude of the S_{21} attenuated by 3 dB in order to simulate the saturation of the transistor. This is the design procedure for Class-E high-efficiency amplifier.

3.2 30-mW FHX35X Class-E Amplifier

The first X-band Class-E amplifier is built using Fujitsu FHX35X HEMT device on a Duroid substrate with dielectric constant of 2.2 and thickness of 0.254mm. It delivers an output power of 30 mW, drain efficiency of 80% and PAE of 64%.

3.2.1 Transistor Output Capacitance Measurement

The output capacitance of the device FHX35X is measured by the HP8510 network analyzer. The circuit for the capacitance measurement is shown in Figure 3.5. The characteristic impedances of the two transmission lines in the circuit are 50 Ω. The device is put on the top of the middle metal pad. The Gate and drain are connected to the transmission lines and the source is connected to the metal pad by wire bonding. To connect the metal pad to the ground which is at the backside of the substrate, a small hole is drilled at the center of the metal pad which is filled with silver epoxy (one type of electrically conductive glue) to reduce the source inductance. The size of the substrate is cut as small as possible to minimize the effects of the substrate on the measurement. Two SMA connectors are connected to the ends of the transmission lines. Furthermore the flange of the SMA connector is trimmed as much as possible to minimize its effect on the measurement.

The method of measuring the output capacitance is as follows: first measure the phase angle of the output impedance of the transistor when the transistor is pined off, then come up with a circuit model and fit the parameters in the model such that the phase angles of the measurement and the circuit model agree with each other. Since the output of the device is connected to a section of 50 Ω

transmission line, the section of 50 Ω transmission line needs to be de-embedded. To de-embed the section of transmission line, the bonding wire of the drain is taken off and S_{22} is measured as a reference. Then the bonding wire is bonded back and S_{22} is measured again and the phase angle is normalized to that of the reference. The output capacitance of the transistor is determined by performing parameter fitting in the circuit model.

The measurement is taken at several drain bias voltages, while the gate bias voltage is -1 V to pinch off the transistor. The normalized phase angle versus frequency for several drain bias voltages is measured by fixing the gate bias and varying the drain bias voltage, as shown in Figure 3.6. The drain bias varies from 0 V to 3 V and the step is 0.5 V.

The next step is to extract the output capacitance of transistor by parame-

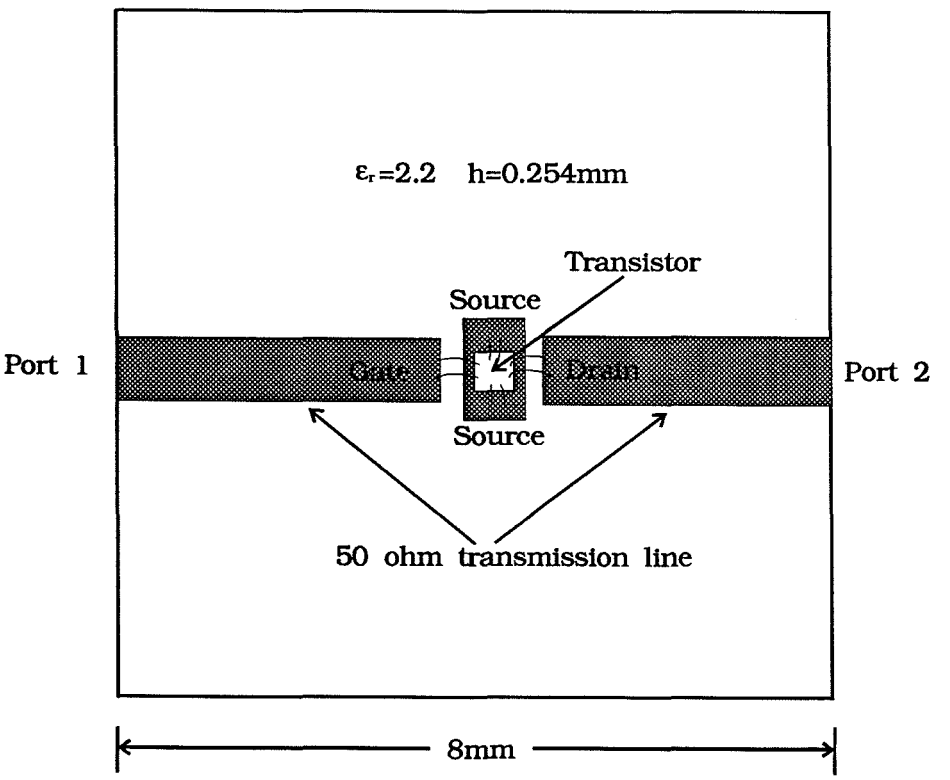


Figure 3.5 The circuit for the output capacitance measurement. The circuit is fabricated on 0.254 mm thick Duroid substrate with dielectric constant of 2.2.

ter fitting. We performed the parameter fitting for two drain bias voltages of 0 V and 3 V. Figure 3.7(a) and (b) show the equivalent circuit models for these two cases respectively. Figure 3.7(c) shows the comparison of the phase angles of the measurements and circuit models. The two solid lines represent the measurement results. The two dash lines are the results from the circuit models. The capacitance in series is the output capacitance of the device and the shunt inductance and capacitance are parasitic parameters in the circuit. The measurement results show that the capacitance doesn't change much when the drain-source DC bias varies. So the assumption that the capacitance is linear is reasonable. The average of the capacitances of these two cases is taken as the output capacitance of the device and the output circuit model used in PSpice simulation is shown in Figure 3.8. The on-resistance for the device is measured to be 9.4 Ω.

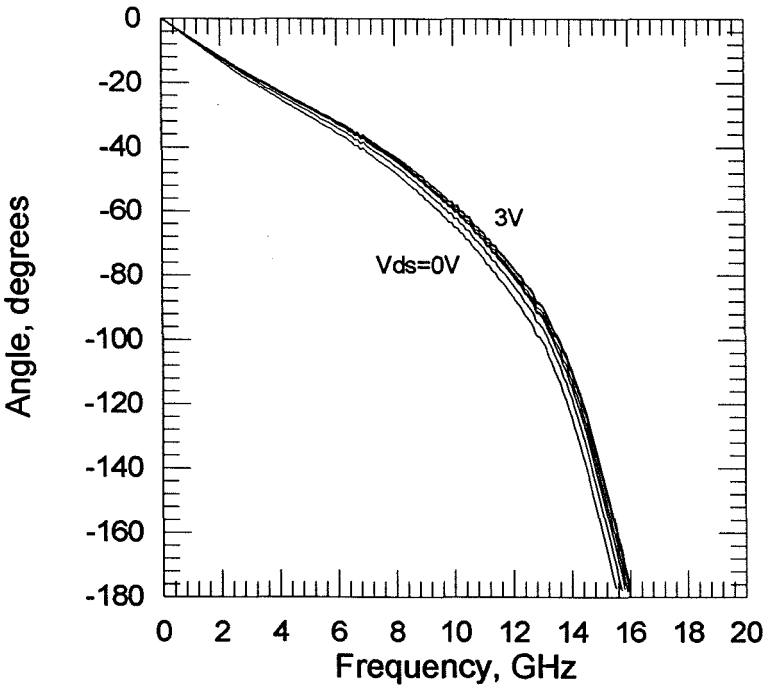
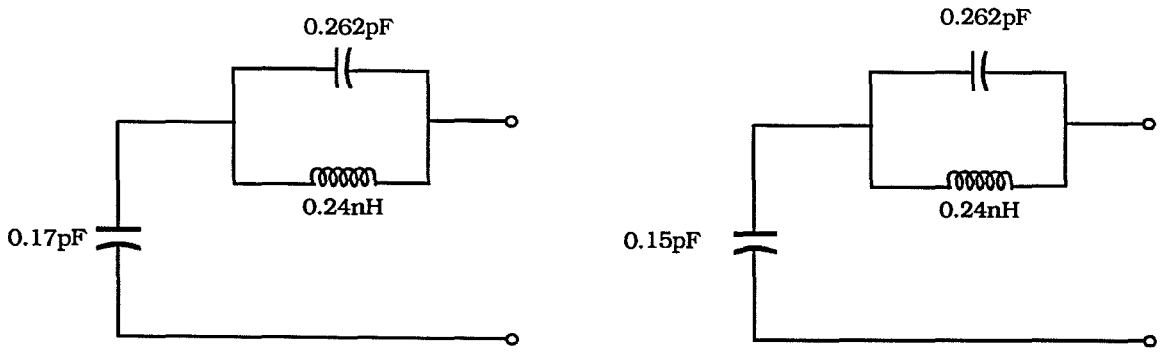


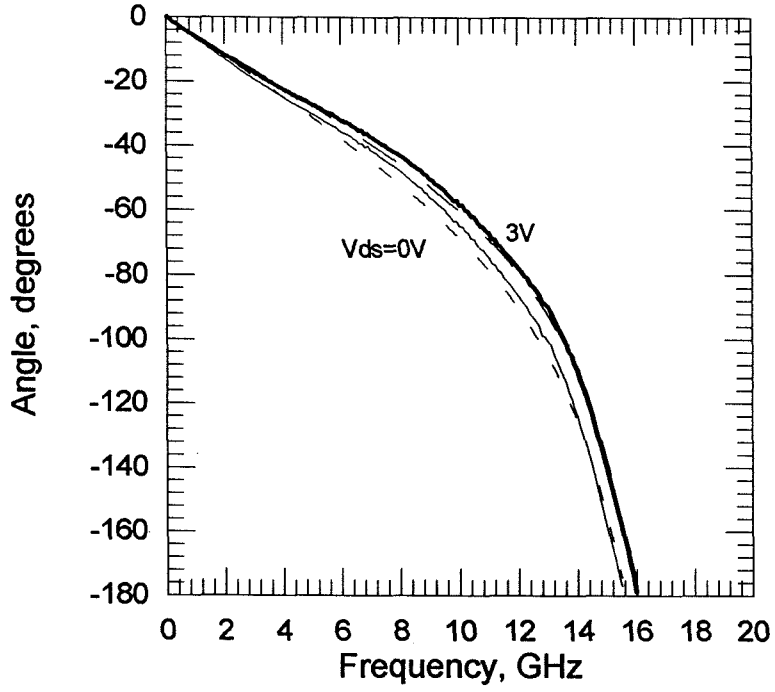
Figure 3.6 Normalized phase angle versus frequency at different drain bias voltages.

3.2.2 PSpice Simulation

Once the output capacitance of the device and the parasitic parameters in the circuit are determined, the output load network can be designed using PSpice.



(a) (b)



(c)

Figure 3.7 Output circuit model for FHX35X at gate bias of -1 V and drain bias of 0 V and 3 V respectively. (a) V_{ds}=0 V (b) V_{ds}=3 V (c) —: measurement, - - -: circuit model.

The load network is a series transmission line and a shunt transmission line with a 50 Ω load. In the simulation, the length and characteristic impedance of the transmission line are adjusted until the waveforms of voltage and current look like the Class-E operation. The PSpice simulation result for the output load network is shown in Figure 3.9. The corresponding switch voltage and current waveforms are shown in Figure 3.10. The simulated drain efficiency is 79% and the output power is 41 mW.

Following the design of the output is the input matching design. Small signal S-parameter is used in the input matching design. The S_{21} of the small signal S-parameter is attenuated by 3 dB to simulate the saturation of the device. The dimensions of the transmission lines for both the input and output are shown in Figure 3.11. The circuit is fabricated on the 0.254 mm thick Duroid substrate with dielectric constant of 2.2.

3.2.3 Efficiency and Output Power Measurement

The measurement is done by an HP8510 network analyzer. In the measurement, first set the input power at a desired level. Then perform the calibration by putting a 50 Ω transmission line in place of the Class-E amplifier. Finally the circuit is connected and S_{21} (the gain of the amplifier at the specified input power and frequency) is measured. Figure 3.12(a) shows the input power sweep

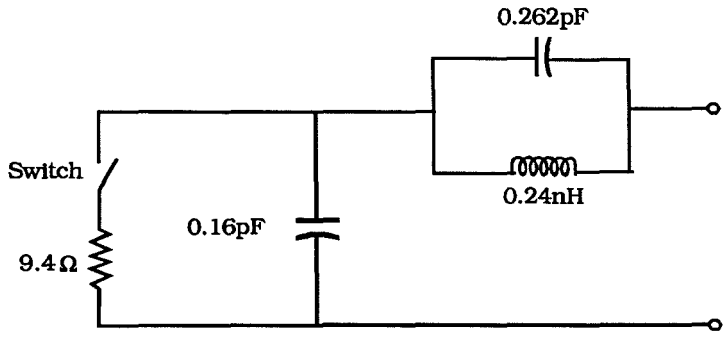


Figure 3.8 Output circuit model for FHX35X.

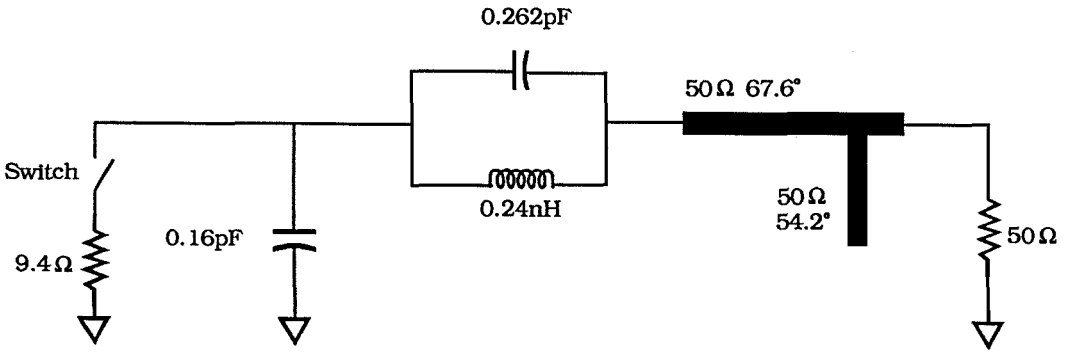


Figure 3.9 PSpice model of the output load network for Class-E amplifier with FHX35X.

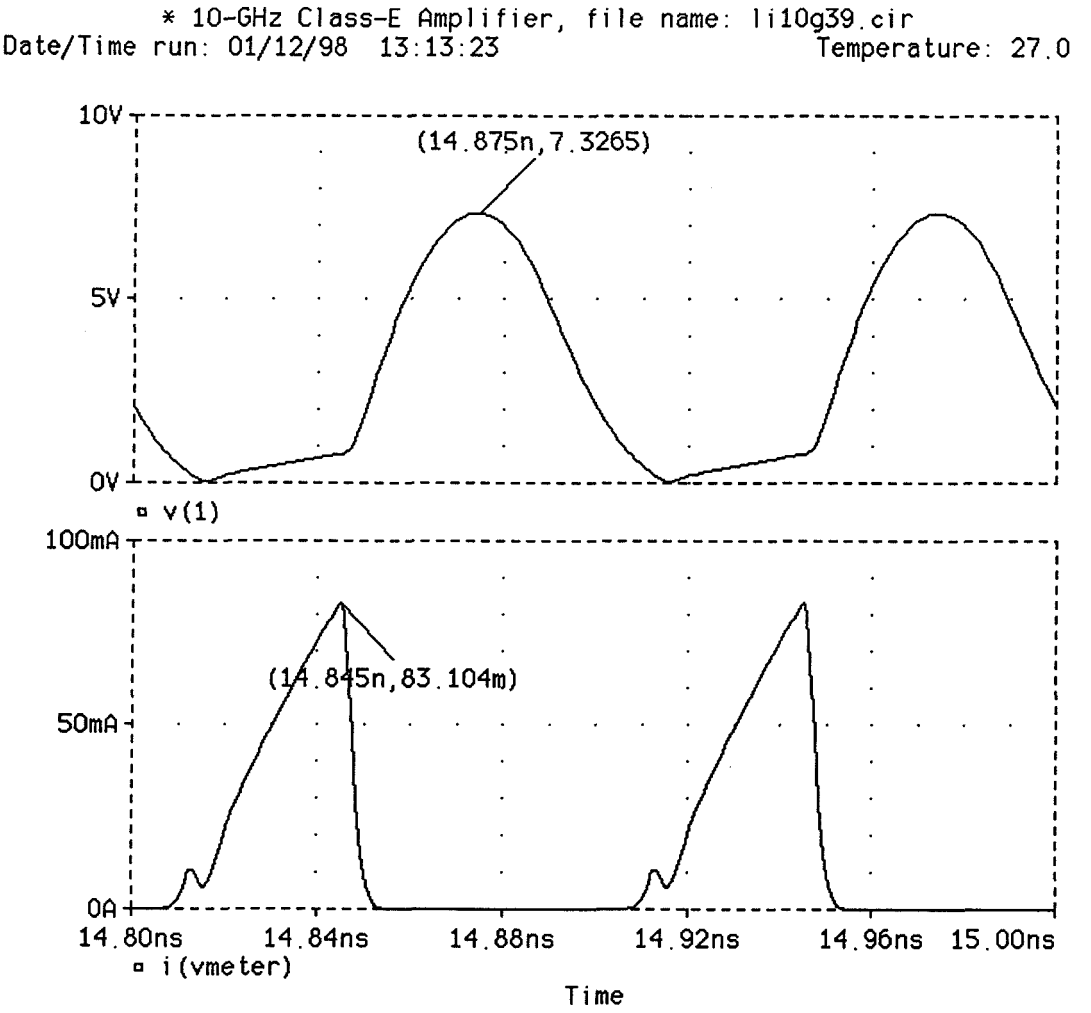


Figure 3.10 PSpice simulation of switch voltage and current waveforms with device FHX35X.

measurement result with the frequency of 11.2 GHz. When the input power is 8 dBm, the amplifier gets a maximum PAE of 64% with 80% of drain efficiency and 15 dBm of output power. Figure 3.12(b) shows the frequency sweep measurement result, with the input power fixed at 8 dBm. During the measurement the dimensions of the transmission lines in the circuit are not adjusted.

3.2.4 Comparison of Theory and Measurement

Given the PSpice circuit model for FHX35X Class-E amplifier, drain efficiency as a function of frequency is simulated and compared with the measured drain efficiency. Figure 3.13(a) shows the comparison. There is a frequency shift between the measured and simulated drain efficiency. For the simulation, the drain efficiency peaks at 10.4 GHz and the measured drain efficiency peaks at 11.2 GHz. If the frequency of the simulation is shifted from 10.4 GHz to 11.2 GHz, the result is shown in Figure 3.13(b). Figure 3.13(b) shows that the bandwidth of the measurement is narrower than that of the simulation. This is probably due to that the PSpice simulation only includes the output circuit and does not take the effect of the input matching circuit into account.

Table 3.1 compares the amplifier performance of Class-A mode and Class-E mode operations with device FHX35X HEMT. The theoretical maximum effi-

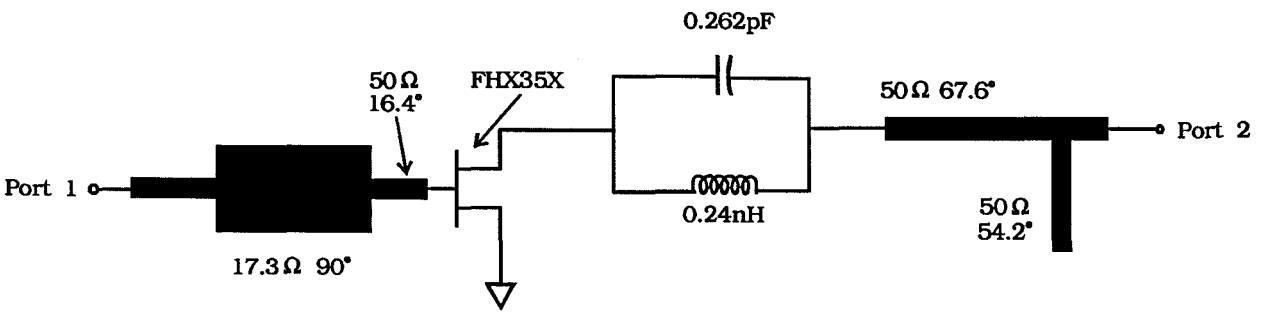
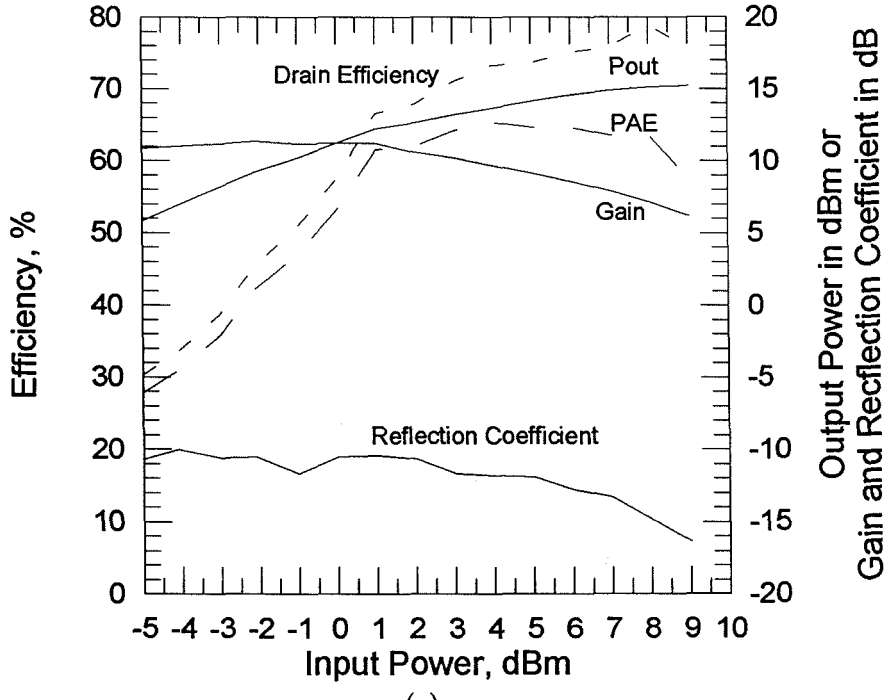
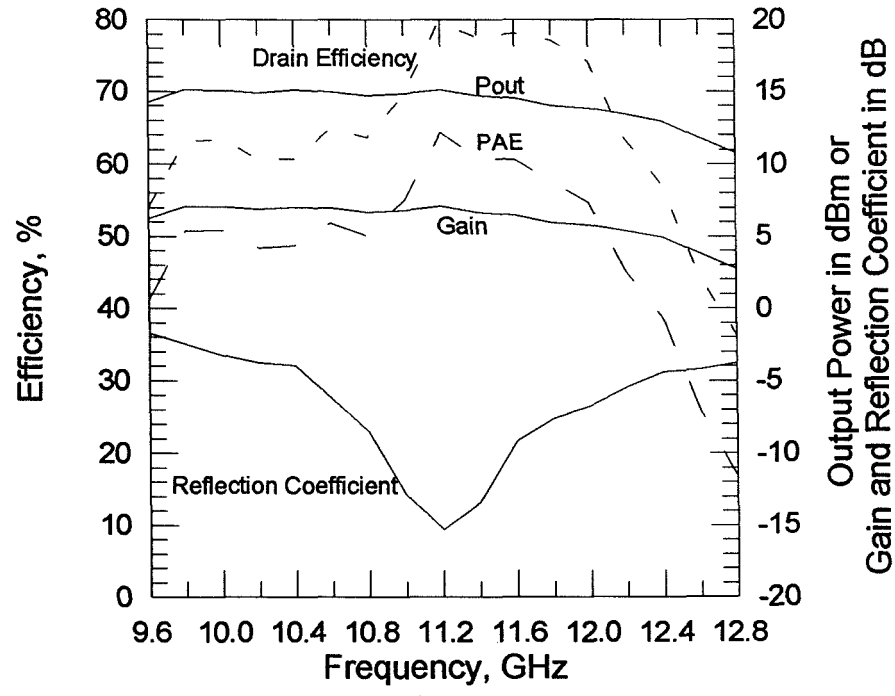


Figure 3.11 The input and output circuit dimensions for the Class-E amplifier with Fujitsu HEMT FHX35X.



(a)



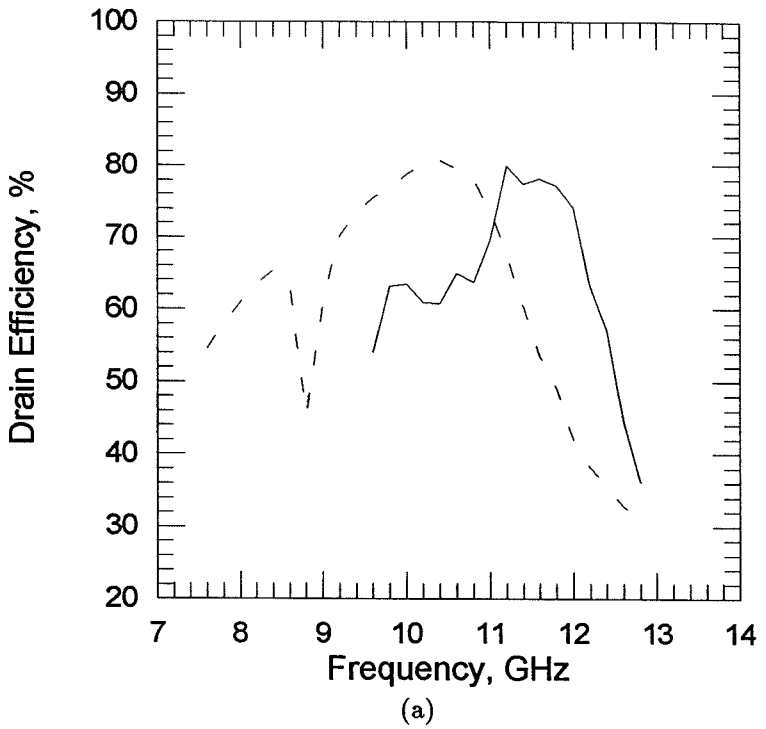
(b)

Figure 3.12 Output power and efficiency measurement results for the FHX35X Class-E amplifier. Without RF signal, the DC bias is: $V_{ds} = 3\,\text{V}$, $I_{ds} = 0.97\,\text{mA}$, $V_{gs} = -0.518\,\text{V}$. (a) Power sweep with the frequency fixed at 11.2 GHz. (b) Frequency sweep with the input power of 8 dBm.

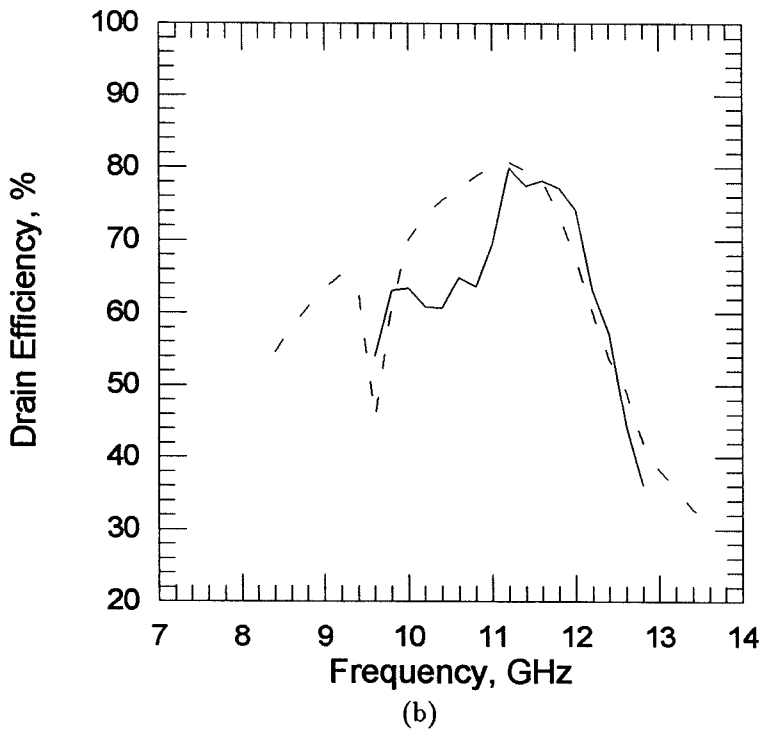
ciency for Class-E amplifier is 100%, while for Class-A, the theoretical maximum efficiency is 50%. The table shows clearly that the Class-E mode provides much higher efficiency than Class-A mode operation, though at the expense of lower gain.

3.3 190-mW FLR056XV Class-E Amplifier

It is desirable to have high output power while maintaining high efficiency. At first the Fujitsu FLK052XP chip device was selected. FLK052XP is a Ku band device. According to the Fujitsu databook [5], it has output power at 1 dB gain compression point of 27 dBm (500 mW), power gain at 1 dB gain compression point of 7 dB and power added efficiency of 32% at 14.5 GHz. But for the Class-E operation at X-band, the gain is only around 4 dB. Although the drain efficiency is 80%, the PAE is only 48% because of the low gain. Since for the Class-E operation, the device is biased to pinched-off state and is on for half of the cycle, the gain is greatly reduced compared to Class-A operation. So higher frequency device Fujitsu FLR056XV chip device is selected, and the gain of the Class-E amplifier at 9 GHz is 6.5 dB. FLR056XV is a device for 18 GHz application. According to the Fujitsu databook [5], it has output power at 1 dB gain compression point of 26 dBm (400 mW), power gain at 1 dB gain compression point of 8 dB and power-added efficiency of 29%. The design procedure for this high power amplifier is similar to that of the 30 mW one. First the output capacitance of the device is measured by fixing the gate bias voltage to be -3.018 V and sweeping the drain bias voltage from 0 V to 6 V. Next is the parameter fitting to come up with the equivalent circuit which is shown in Figure 3.14(a) and (b) for drain bias voltage at 0 V and 6 V respectively. Figure 3.14(c) shows the measured phase angle of the output circuit port at two drain bias conditions 0 V and 6 V and their equivalent circuit models. For some reason, the model doesn't agree well in the whole frequency range. Since the design frequency is 10 GHz, the parameters are adjusted so that the results agree well around 10 GHz frequency range. The



(a)



(b)

Figure 3.13 Comparison of the theoretical (—) and measured (---) drain efficiency versus frequency for the Class-E amplifier with Fujitsu FHX35X transistor. (a) the frequency of the simulation does not shift; (b) the frequency of the simulation shifts from 10.4 GHz to 11.2 GHz.

output circuit model is shown in Figure 3.15 by averaging the result of Figure 3.14(a) and (b). Again, here the output capacitance of the transistor is assumed to be linear and independent of the drain-source voltage. The average of the fitted capacitances with drain bias voltage of 0 V and 6 V respectively is taken as the output capacitance. The on-resistance of the FLR056XV is measured to be 3.6 Ω.

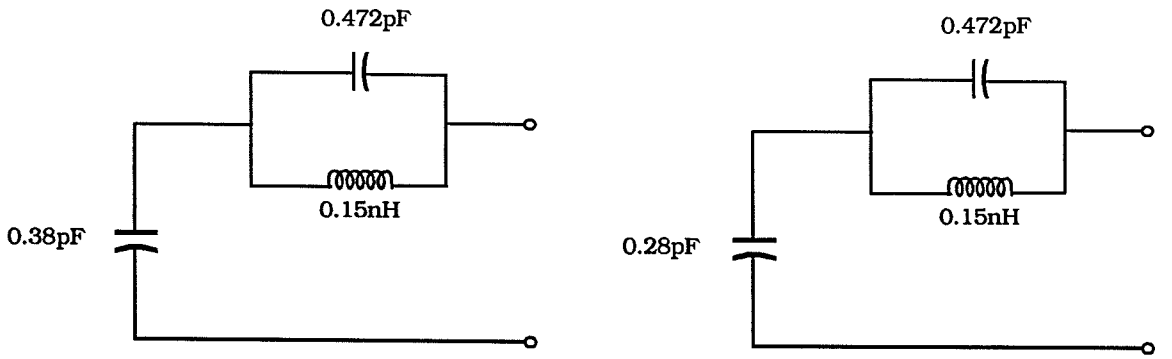
Next is the PSpice simulation for the output load network design. The transmission line dimensions obtained from the PSpice simulation are shown in Figure 3.16. The lengths and characteristic impedances of the two transmission lines are adjusted until the overlapping of the switch voltage and current waveforms is minimal such that the power consumption across the transistor is minimized. The switch voltage and current waveforms are shown in Figure 3.17. Following the output load network design is the input matching design. Again the small signal S-parameter of the device is used with the magnitude of S_{21} attenuated by 3 dB to simulate the saturation of the device. At present the whole circuit design is finished and the circuit is shown in Figure 3.18. The circuit is fabricated on the 0.254 mm Duroid substrate with dielectric constant of 2.2.

The measurement of the first Class-E amplifier with an output power of 30 mW is performed by the network analyzer HP8510C. For the second amplifier, however, since it has higher output power than the first one, it needs more input power. But the HP8510 does not have that power capacity. Therefore an HP83620A Synthesized Sweeper followed by an HP8349B Microwave Amplifier is

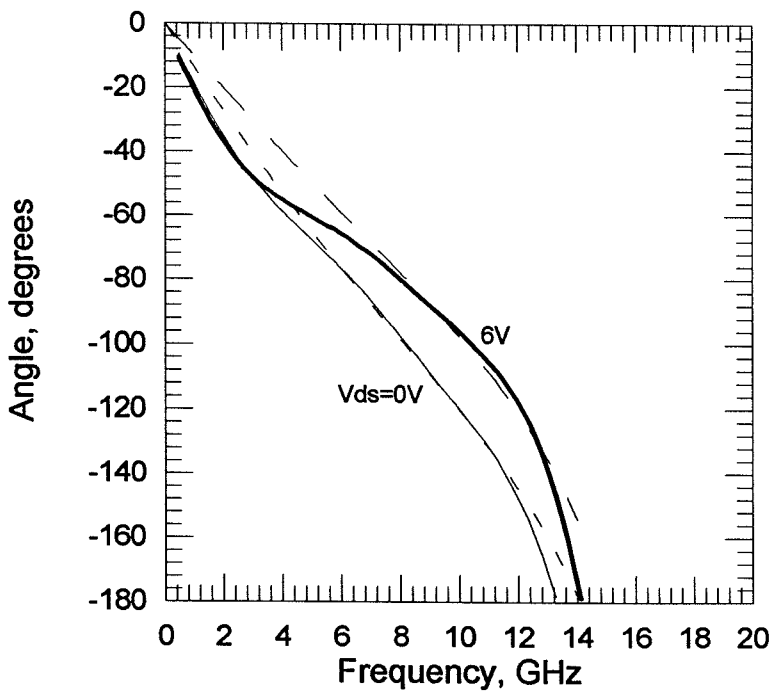
	Frequency(GHz)	Gain(dB)	Power(dBm)	η_D(%)	PAE(%)
Class-A mode(manufacturer)	12.0	10	15	35.1	31.6
Class-E mode(measurement)	11.2	7	15	80.0	64.0

Table 3.1 Comparison of amplifier performance of Class-A mode (from Fujitsu databook [5]) and Class-E mode (from measurement) operations with device FHX35X HEMT.

used as the driver of the second Class-E amplifier. The calibration is performed by putting a 50 Ω line in place of the Class-E amplifier; and the gain and the output power of the amplifier are measured. The measured efficiency and output



(a) (b)



(c)

Figure 3.14 Output circuit model for FLR056XV device at gate bias of −3.018 V and drain bias of 0 V and 6 V respectively. (a) V_{ds}=0 V (b) V_{ds}=6 V (c) — measurement, --- circuit model.

power are shown in Figure 3.19. With the frequency of 9 GHz and the input power of 16.2 dB (42 mW), the PAE peaks at 56%, the drain efficiency is 72% and the output power is 22.7 dBm (186 mW). Again the circuit dimensions are not adjusted during the measurement.

Table 3.2 compares of the measurement result of Class-E amplifier with the data of Class-A mode operation given by Fujitsu [5]. It shows again that Class-E amplifier has much higher efficiency than Class-A mode operation at the expense of lower gain.

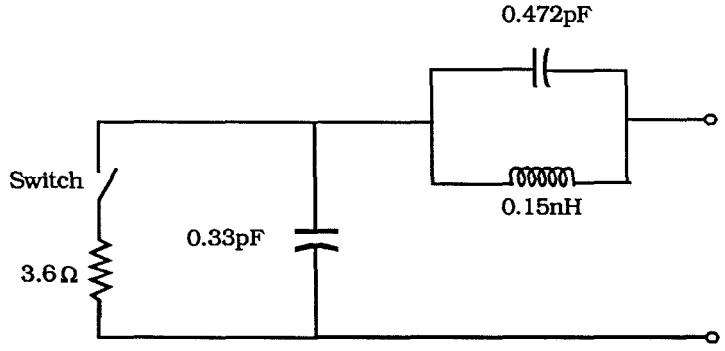


Figure 3.15 Output circuit model for FLR056XV.

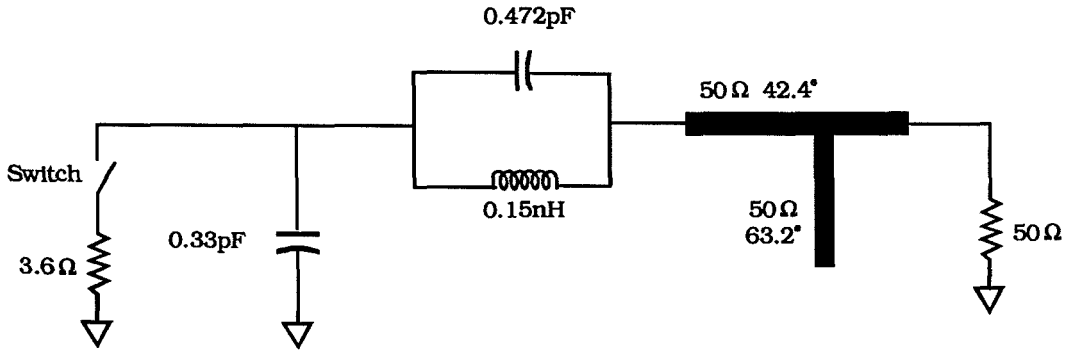


Figure 3.16 PSpice model of the output load network for Class-E amplifier with FLR056XV.

3.4 Discussion

For the 190 mW Class-E amplifier using FLR056XV MESFET, the reflection coefficient is measured around −4 dB. In the input matching circuit design, the small signal S-parameter of the device with 3 dB attenuation of S_{21} is used. At microwave frequencies, the circuit tuning is not as easy as at low frequencies because of the use of transmission lines instead of lumped components. Therefore the nonlinear model of the device is needed for the input matching circuit design.

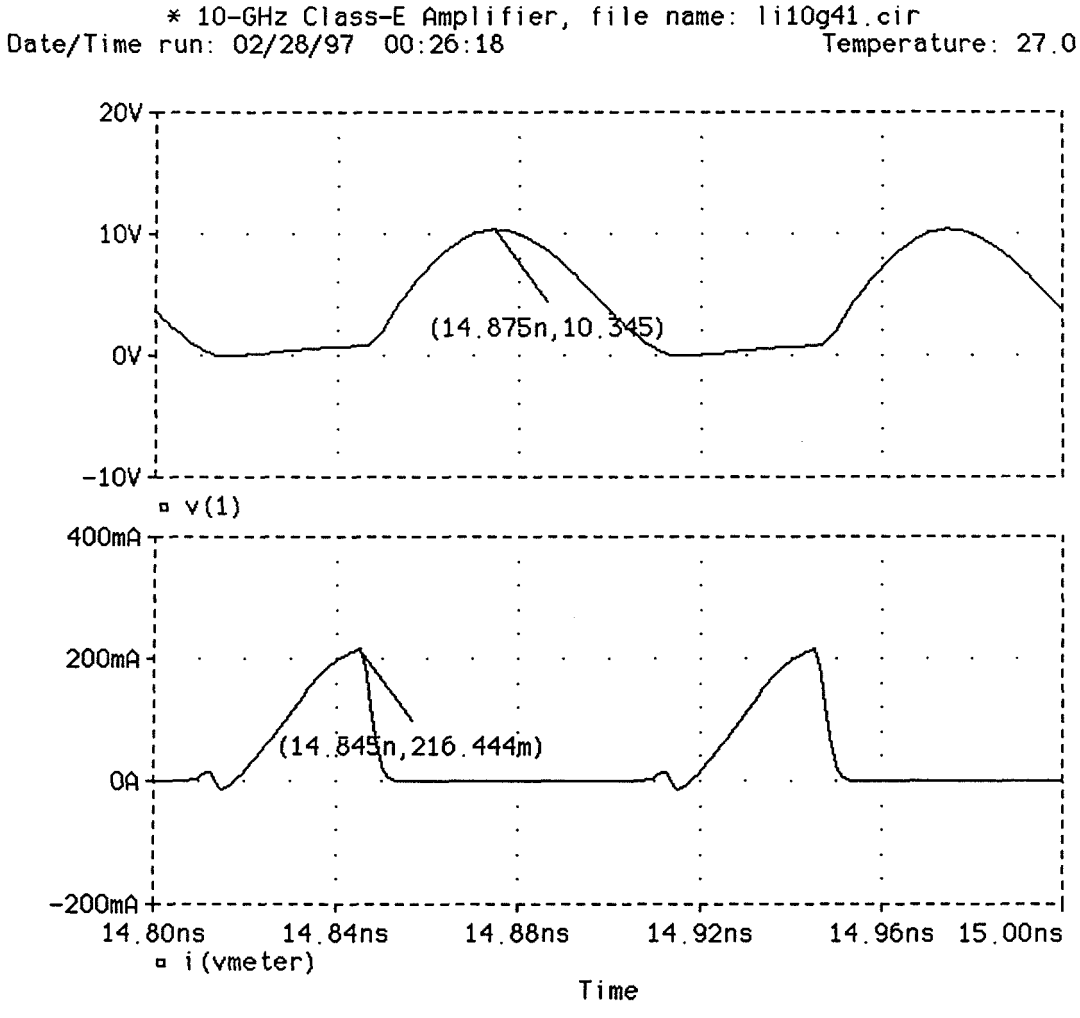


Figure 3.17 PSpice simulation of switch voltage and current waveforms across the transistor FLR056XV MESFET.

For the output load network, it has been shown in the previous chapter that the efficiency and output power are very sensitive to the output load network component values. If an accurate nonlinear model is available, we can design the

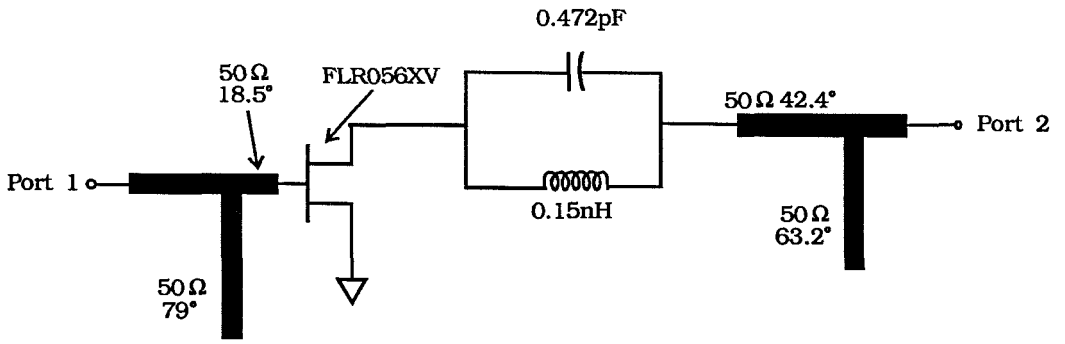


Figure 3.18 The input and output circuit dimension for Class-E amplifier with transistor FLR056XV.

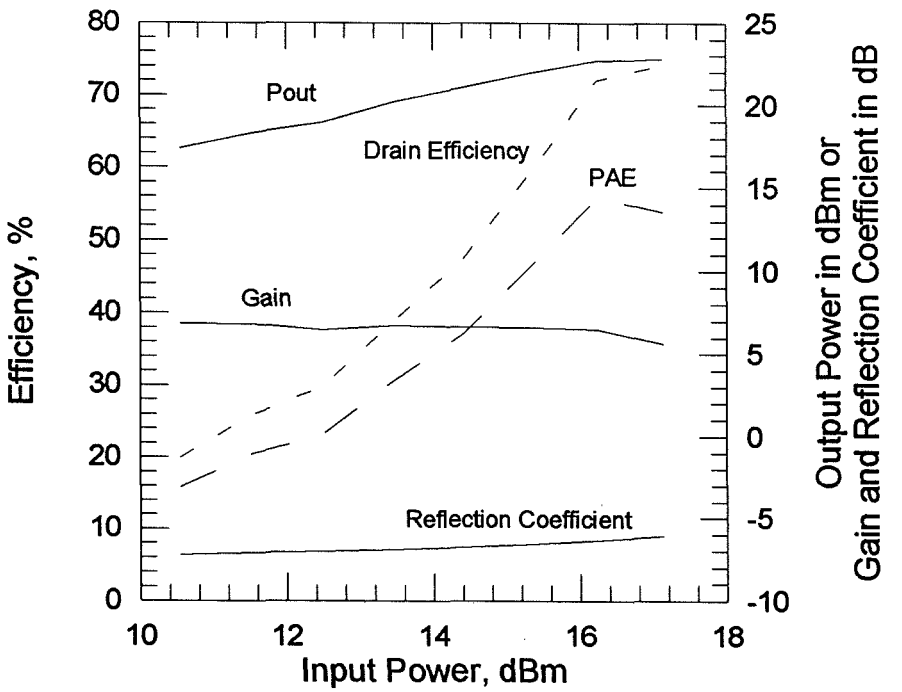


Figure 3.19 Output power and efficiency measurement results for the FLR056XV Class-E amplifier. Without RF signal, the DC bias is: $V_{ds} = 4.21\,\text{V}$, $I_{ds} = 66.1\,\text{mA}$, $V_{gs} = -2.238\,\text{V}$. Power sweep with the frequency fixed at 9 GHz.

output load network more accurately so that the amplifier can achieve optimum performance.

The amplifier is designed to operate at Class-E mode, however it is not clear whether it indeed operates at that mode since no high speed oscilloscope at X-band is available to measure the drain waveform. It is desirable to measure the drain waveform to confirm the Class-E mode when such oscilloscope becomes available in the future.

In the two X-band Class-E amplifiers, we need to apply negative gate bias to pinch off the device so that there is DC power dissipated in the device when there is no signal at the input. Consequently in the amplifier circuits, two biases are needed, one for the gate and the other for the drain. In the previous chapter, the 440 MHz Class-E amplifier uses an n-channel enhancement mode MOSFET, and does not need the gate bias since the MOSFET is at off-state when there is no signal at the gate. Only one power supply (for the drain bias) is needed, which makes the circuit simpler. For the HEMT and MESFET transistors used in X-band Class-E amplifiers, there is a large reduction in the gain of the amplifier when the negative gate bias is applied to pinch off the device completely. Therefore in the measurement the device is not pinched off completely and there is a small drain current flow. For the MOSFET device, it does not have this problem and can be turned off completely. There is a lot of progress in the development for MOSFET's. They are definitely good candidates when they are available at X-band frequencies.

	Frequency(GHz)	Gain(dB)	Power(dBm)	η_D(%)	PAD(%)
Class-A mode(manufacturer)	18	8.0	26.0	34.5	29.0
Class-E mode(measurement)	9	6.5	22.7	72.0	56.0

Table 3.2 Comparison of amplifier performance of Class-A mode (from Fujitsu databook [5]) and Class-E mode (from measurement) operations with device FLR056XV MESFET.

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Chapter 4

Grid-Oscillator Beam-Steering Array

Quasi-optical power combining techniques [1] offer a promising approach to realize compact, reliable, lightweight, and higher-power systems at millimeter and submillimeter wave frequencies. A complete structure of quasi-optical transmitter or receiver requires electronic beam-controllers for beam steering. Beam-steering can be achieved mechanically or electrically. Electronic beam-steering has a few advantages over mechanical beam-steering. Mechanical beam-steering is slow to scan an area. It is expensive to build a mechanical beam-scanning system and usually it is heavy and bulky. Electronic scanning systems are more reliable, flexible and have higher scanning-speeds. Electronic beam-steering is achieved by establishing a constant phase difference between adjacent elements in an array.

Millimeter wave systems are of great interest. However, the lack of reliable, inexpensive high power sources has been a problem. So far two types of sources have been used: tubes and solid-state devices. Tubes are high-power source and have higher frequencies than the semiconductor devices. But in many circumstances, the size, weight, and required high-voltage supplies limit their use. Compared to tube sources, solid-state devices are small, light-weight, inexpensive, and require small to moderate voltages. In order to overcome the limited power output of solid-state devices, the power combining of large numbers of solid-state devices is needed. One of the methods is planar grid oscillator power combining which is developed at Caltech [2]–[6]. In this work the planar grid

oscillator is used as the single radiating element.

Electronic beam-steering is achieved by setting constant phase progression between adjacent elements. In a traditional phased array the constant phase difference is set by phase shifters. However, the phase shifters are expensive at microwave and millimeter wave frequencies. Robert York proposed a new method of beam-steering without using any phase shifters [7]. The idea is to establish the constant phase progression by slightly detuning the end elements in the array. Liao and York demonstrate this idea using a line array of patch antennas [8]. The beam-steering presented here uses a planar line-grid oscillator as the radiating element. The planar line-grid oscillator is based on the planar grid developed by Weikle [6].

The outline of this chapter is as follows: first the introduction of the principle of the beam-steering array. Then York's beam-steering theory is introduced. From York's theory, to get the right phase shift between the active elements, the phase coupling coefficient between adjacent element needs to be determined. So the coupling coefficient measurement is discussed. Next the line-grid oscillator is presented. This line-grid oscillator is the radiating element for the beam-steering array. Finally the grid-oscillator beam-steering array is fabricated and the maximum beam-scanning angles in both direction are $-6.5°$ and $5°$ respectively.

4.1 Introduction to Beam-Steering Array

Assume we have an N-element linear array shown in Figure 4.1. In the array all of the elements are equidistant and all of the currents on each element are equal in magnitude. The array pattern can be described by the following equation

$$E \propto \frac{\sin\left[(N/2)(kd\sin\phi - \Delta\theta)\right]}{\sin\left[(1/2)(kd\sin\phi - \Delta\theta)\right]}, \tag{4.1}$$

where E is the electric field, N is the number of elements in the array, k is the propagation constant, d is the the distance between adjacent elements, ϕ is the

beam-steering angle, and $\Delta\theta$ is the phase difference between adjacent elements. For a given phase delay $\Delta\theta$, the direction of the main lobe ϕ_{m} can be determined from the following equation

$$\phi_{\mathrm{m}} = \sin^{-1}\left(\frac{\Delta\theta}{kd}\right). \tag{4.2}$$

If the phase delay can be electronically controlled, the direction of the main lobe can be scanned without physical motion of the antenna. This is important in large installation which must continually scan a large range of directions in a short period of time.

4.2 York's Beam-Steering Theory

York's theory is based on the van der Pol oscillator equation [9] and the Adler injection-locking theory [10]. For weak coupling, the oscillator amplitude is close to its free-running value, so the system is mainly represented by the phase dynamics. York accounts for the interaction between adjacent elements of a system of coupled oscillators by a complex coefficient with magnitude ϵ and phase ϕ with assumption of the reciprocity of the elements. The oscillator phases satisfy the following equation

$$\frac{d\theta}{dt} = \omega_0 + \frac{\omega_0}{2Q}\frac{A_{inj}}{A}\sin(\theta_{inj} - \theta), \tag{4.3}$$

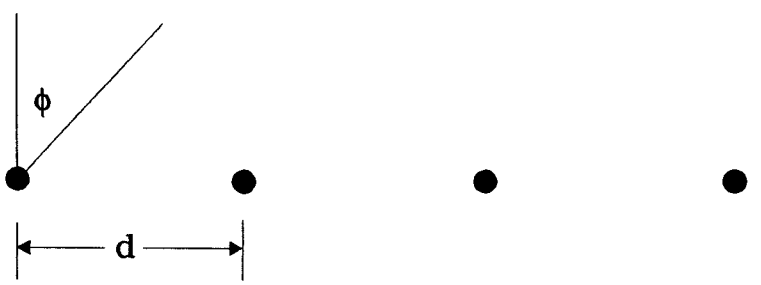


Figure 4.1 An N-element linear array.

which is a form of Adler's equation for injection-locking [10]. In Equation (4.3), A and θ are the instantaneous amplitude and phase of the oscillator respectively, A_{inj} and θ_{inj} are the instantaneous amplitude and phase of the injected signal respectively, ω_0 is the free running frequency of the oscillator, and Q is the Q-factor of the oscillator embedding circuit.

For a system of coupled oscillators, the mutual interaction between oscillators i and j can be described by a complex coupling coefficient, κ_{ij}, which is

$$\kappa_{ij} \equiv \lambda_{ij} e^{-j\Phi_{ij}}, \tag{4.4}$$

where λ_{ij} is the amplitude, and Φ_{ij} is the phase angle of κ_{ij}. In the case of weak coupling, the elements in the array interact primarily with adjacent elements. With the additional assumption that the coupling is reciprocal and the oscillators in the array are equidistant, the coupling coefficient can be expressed as

$$k_{ij} = \begin{cases} \lambda e^{-j\Phi}, & \text{if } |i-j| = 1 \\ 0, & \text{otherwise} \end{cases} \tag{4.5}$$

with λ to represent the coupling strength and Φ to represent the coupling phase angle. Then the array is described by a set of equations

$$\frac{d\theta_i}{dt} = \omega_i - \frac{\lambda\omega_i}{2Q} \sum_{\substack{j=i-1 \\ j\neq i}}^{i+1} \frac{\alpha_j}{\alpha_i} \sin(\Phi + \theta_i - \theta_j) \quad i = 1, 2, \ldots, N \tag{4.6}$$

where the subscript i represents the oscillator i in the array, α_i is the free running amplitude, ω_i is the free running frequency, $\theta_i = \omega_i t + \phi_i$ is the instantaneous phase of oscillator i, and Q is the Q-factor of the oscillator embedding circuit. Electronic beam-steering requires a constant phase progression along the array, such that $\theta_i - \theta_{i+1} = \Delta\theta$, define $\lambda' = \lambda/2Q$ and assume $\alpha_i = \alpha_j$, in the case of $\Phi = 0°$, when the oscillators synchronize to a common frequency ω_f, where

$$\frac{d\theta_i}{dt} = \omega_f \quad i = 1, 2, \ldots, N. \tag{4.7}$$

The constant phase difference $\Delta\theta$ between adjacent elements can be achieved if

$$\omega_i = \begin{cases} \omega_f \left[1 - \lambda' \sin \Delta\theta\right]^{-1} & \text{if } i = 1 \\ \omega_f & \text{if } 1 < i < N \\ \omega_f \left[1 + \lambda' \sin \Delta\theta\right]^{-1} & \text{if } i = N \end{cases} \tag{4.8}$$

A stability analysis [7] puts limits on the phase difference $\Delta\theta$. For the case of $\Phi = 0°$, the limits are $-90° < \Delta\theta < +90°$. The relationship between the phase shift and the beam-steering angle is

$$\Delta\theta = kd \sin \Psi, \tag{4.9}$$

where Ψ is the scan angle measured from broadside, d is the element separation, k is the propagation constant, and $\Delta\theta$ is the phase shift.

4.3 Line-Grid Oscillator

The grid-oscillator is a periodic array with embedded active solid-state devices. As shown in Figure 4.2, the mirror and the partial reflector form a Fabry-Perot resonator and the grid is placed in the cavity.

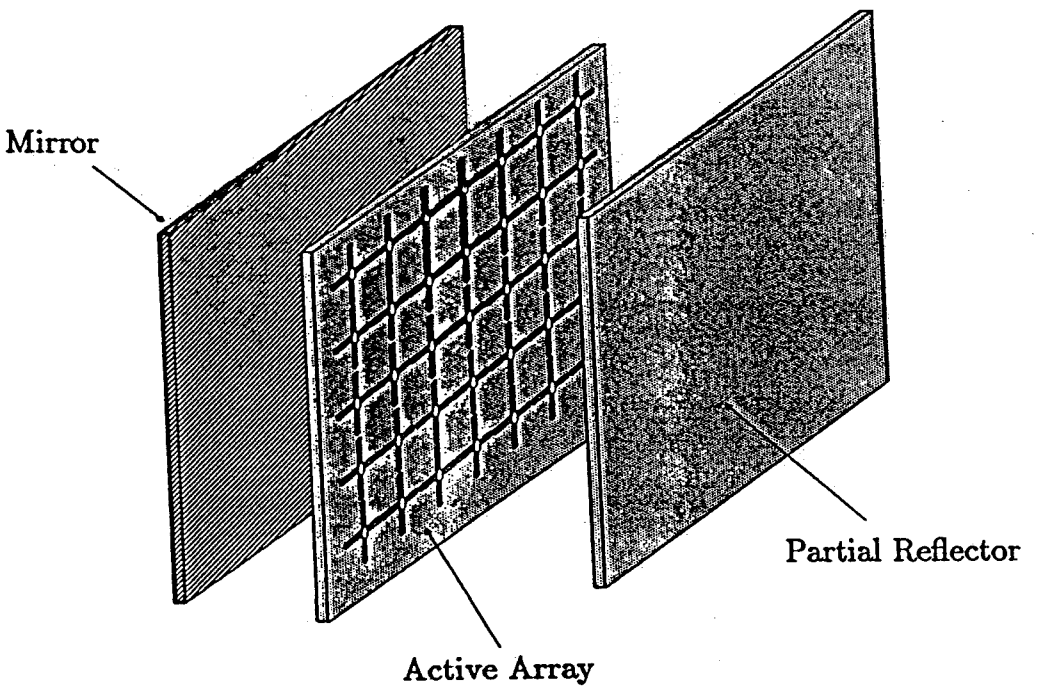


Figure 4.2 Grid-oscillator configuration, from Robert Weikle's Ph.D. thesis [6].

The elements making up an oscillator grid are not themselves free-running oscillators. Mutual interaction of all the devices in the grid is necessary for oscillation to occur. Consequently, the oscillation frequency and output power are strongly affected by the device spacing and the grid configuration. Furthermore, because the power is combined in free space, losses associated with waveguide walls and feed network are eliminated.

A planar transistor grid is shown in Figure 4.3. In the design, the transistors are placed at each node in the grid and represented by circles. The DC bias is fed along horizontal leads which extend across the grid. Adjacent rows of devices share bias lines. The radiating leads run in the vertical direction and are connected to two terminals of the transistor. The third transistor terminal is connected to the center bias line which runs along the row of the devices. In order to predict the oscillation frequency, the embedding circuit for solid-state devices needs to be determined. However, calculation of the driving point impedance

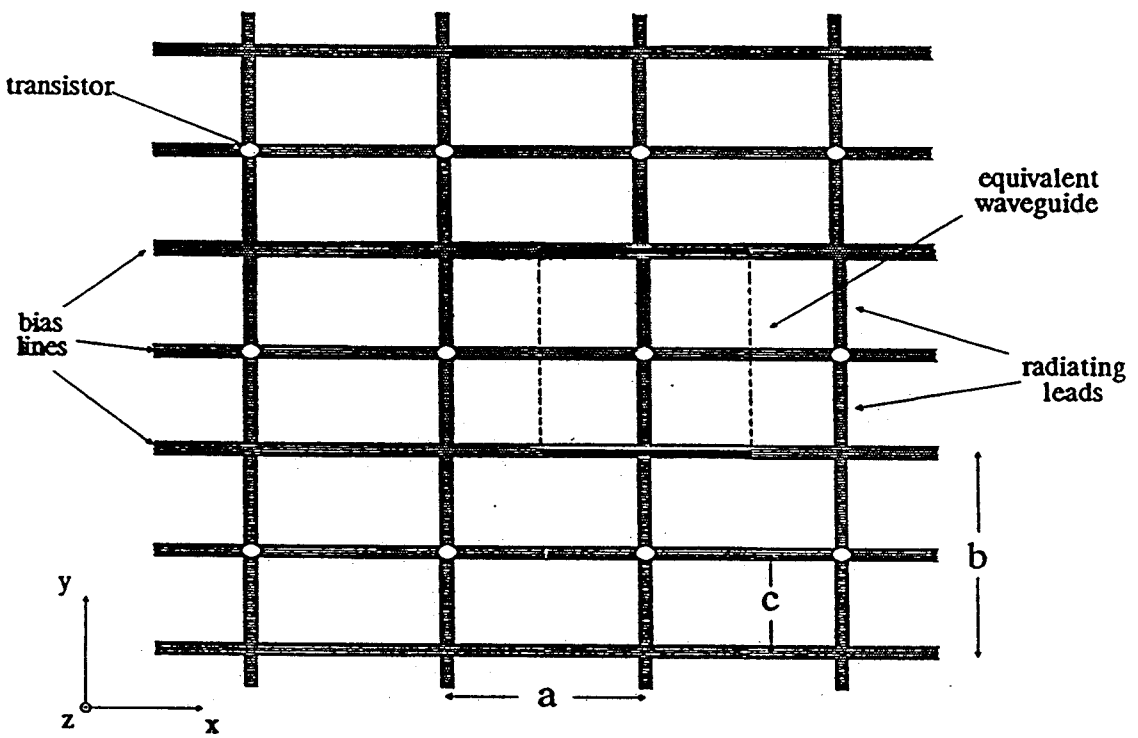


Figure 4.3 A planar transistor grid, from Robert Weikle's Ph.D. thesis [6].

for devices in a finite grid is difficult because of the unknown behavior of the field at the grid edges. Furthermore, each device in the array couples to all other devices through the radiated fields. For simplicity, it is usually assumed that the grid is infinite in extent. By the symmetry of the grid, a unit cell equivalent waveguide is defined. The top and the bottom are electric walls and the two sides are magnetic walls. With an assumption of the current distribution and the application of EMF method, an equivalent circuit model for the planar transistor grid is determined and shown in Figure 4.4.

Terminal 1 and 2 of the circuit represent connection to the vertical leads of the grid. Currents in these leads couple to the radiated field through the transformer. In addition, there is a lead inductance L associated with TE modes which are excited by currents flowing in the vertical direction. The third terminal of the transistor is connected to the horizontal lead running through the center of the unit cell. Currents on this leads are perpendicular to the radiated field and thus produce evanescent TE and TM modes which are modelled with

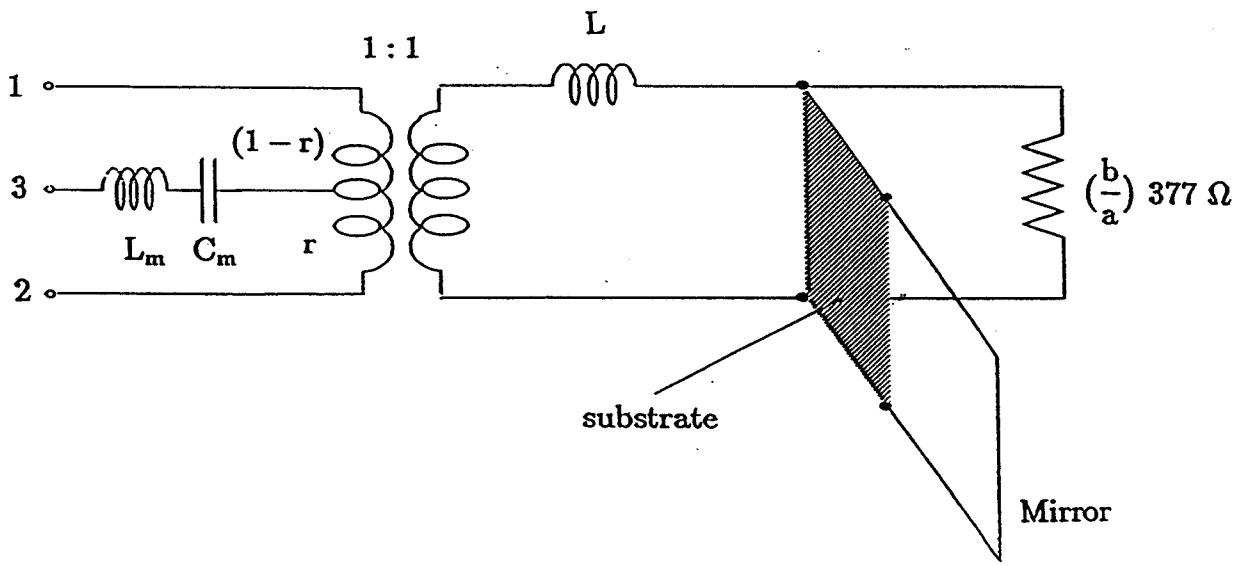


Figure 4.4 Transmission line circuit model for the planar grid-oscillator, from Robert Weikle's Ph.D. thesis [6].

reactive lumped elements. The resistance represents the free space. We design the oscillator using this equivalent circuit model and the transistor model.

In the grid-oscillator beam-steering array, the active element is the line-grid oscillator. It is a 4×1 array with Fujitsu FHX35X HEMT device. The relationship between the phase shift and the beam-scanning angle in Equation (4.9) indicates that, for a fixed phase shift angle, the smaller the spacing is, the bigger the beam-scanning angle can be achieved. Therefore there is only one row of chips in each single grid-oscillator such that the spacing between the oscillators can be as small as possible. The grid is fabricated on 15 mil thick Duroid substrate with dielectric constant of 2.33. The metal pattern of the line-grid oscillator is show in Figure 4.5. The grid is a periodic array with embedded active solid-state devices. The mirror and the partial reflector form a Fabry-Perot resonator. The design of the line-grid oscillator is based on the Robert Weikle's EMF method [6]. The transistors are placed at each node in the grid and are represented by circles.

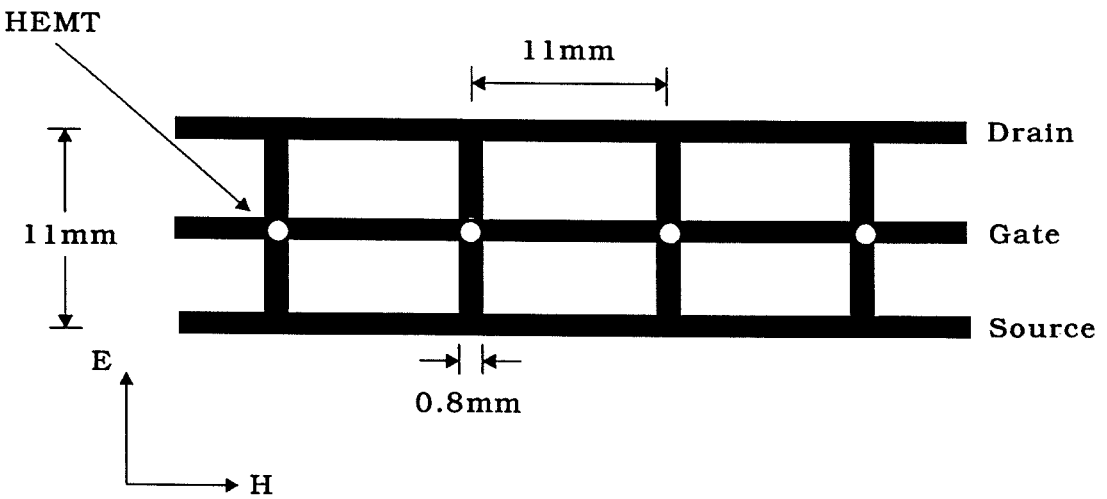


Figure 4.5 The line-grid oscillator radiating element at 11 GHz with effective radiated power of 50 mW.

The DC bias is fed along horizontal leads which extend across the grid. The radiating leads run in the vertical direction and are connected to two terminals of the transistor. A mirror behind the grid helps to lock the devices together and assures the power radiates in one direction.

After the line-grid oscillator fabrication, the radiating patterns are measured and shown in Figure 4.6. The theoretical pattern is shown in dash line. The theoretical E-plane and H-plane patterns are calculated using the configurations shown in Figure 4.7. Since there is a mirror for the oscillator circuit, the radiating element has an image. For the E-plane pattern, the electric field is

$$E \propto \sin(\frac{\pi d}{\lambda}\cos\theta)\cos\theta, \tag{4.10}$$

where $\cos\theta$ is for the element pattern by assuming each element is a small dipole. For the H-plane pattern, the electric field is

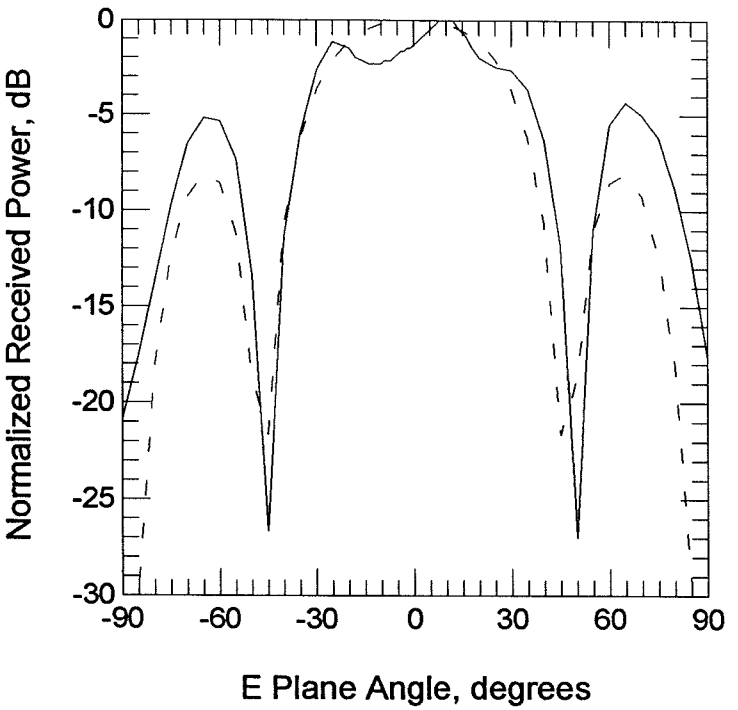
$$E \propto \frac{\sin(\frac{4\pi d_1}{\lambda})\sin\theta}{\sin(\frac{\pi d_1}{\lambda}\sin\theta)\sin(\frac{\pi d}{\lambda}\cos\theta)}. \tag{4.11}$$

The variables in Equations (4.10) and (4.11) are defined in Figure 4.7.

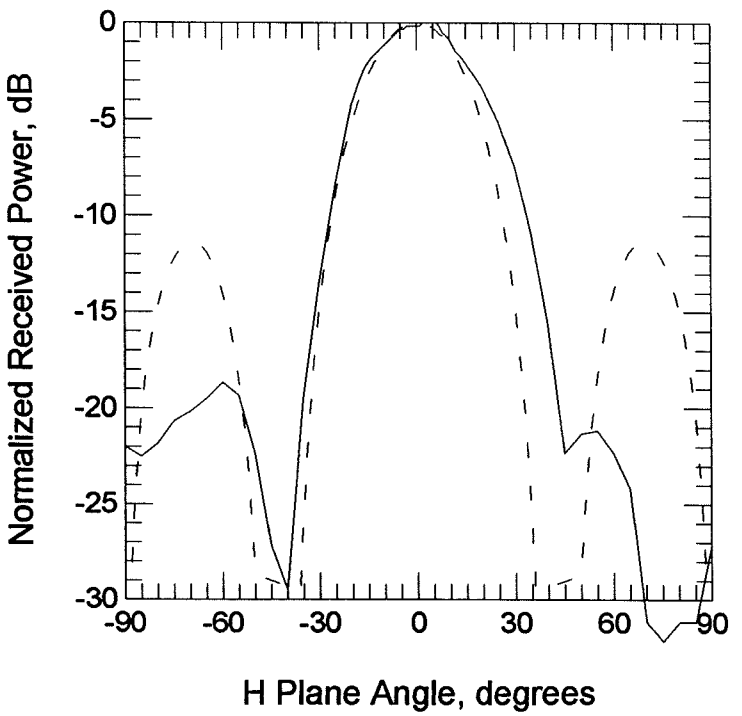
4.4 Coupling Coefficient Measurement

From York's theory, it is clear that if the coupling coefficient angle Φ is set to 0°, the constant phase difference can be formed by detuning the two end elements in the array so that the beam can be scanned. Since the spacing between the radiating elements has direct effects on the coupling coefficient, the coupling coefficient needs to be measured to determine the appropriate spacing between the adjacent elements so that the coupling phase angle $\Phi = 0°$. The measurement follows the idea of measuring the mutual impedance of the oscillators [11]. A single oscillator is imaged by a metal plane and thus simulating two identical oscillators as shown in Figure 4.8. For two identical, frequency-locked oscillators (i.e., $\omega_1 = \omega_2 \equiv \omega_0, \alpha_1 = \alpha_2$), from Equation (4.6) we can get

$$\frac{\Delta f}{f_0} = \pm\lambda'(x)\sin\Phi(x), \tag{4.12}$$



(a)



(b)

Figure 4.6 The radiation pattern for the line-grid oscillator. (a) E-plane pattern. (b) H-plane pattern. — Measurement and - - - Theory. The theory assumes that the mirror is 20 mm away from the line-grid oscillator.

where $\lambda' = \lambda/2Q$, $\Delta f = f - f_0$, and f is the output frequency. The + sign is for the H-plane coupling (i.e., $\Delta\theta = \pi$) and the − sign is for the E-plane coupling (i.e., $\Delta\theta = 0$). The coupling between the oscillator and its image is controlled by adjusting the spacing between the oscillator and the image plane. When the spacing changes, the output frequency will change also. This frequency change can be related to the coupling coefficient by Equation (4.12) and can be used to decide the oscillator spacing such that $\Phi = 0°$.

The measurement setup is shown in Figure 4.9. A HEMT grid-oscillator is fabricated on the substrate 15 mil thick with dielectric constant 2.33. The

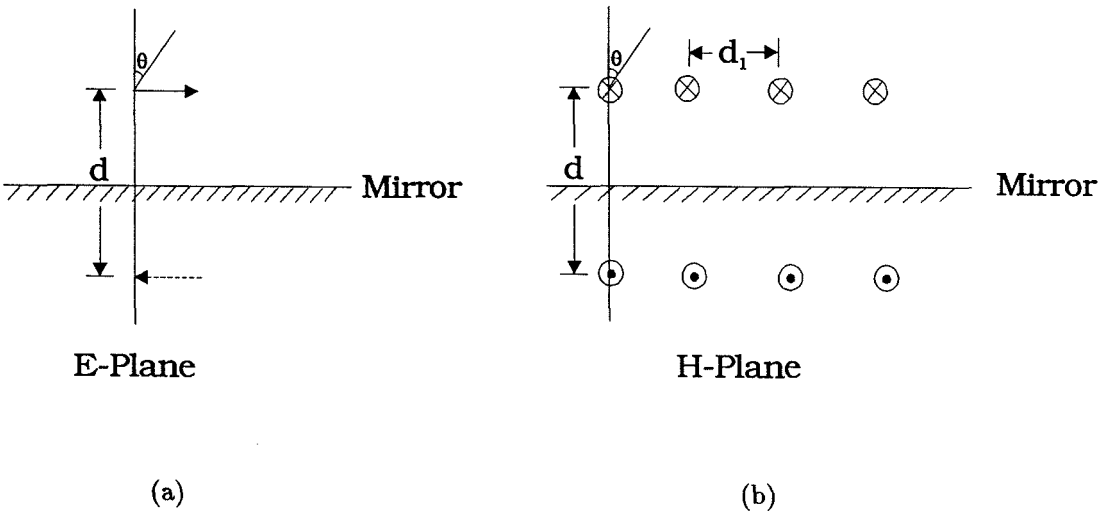


Figure 4.7 The configurations for the theoretical patterns calculations of single line-grid oscillator. (a) E-plane. (b) H-plane.

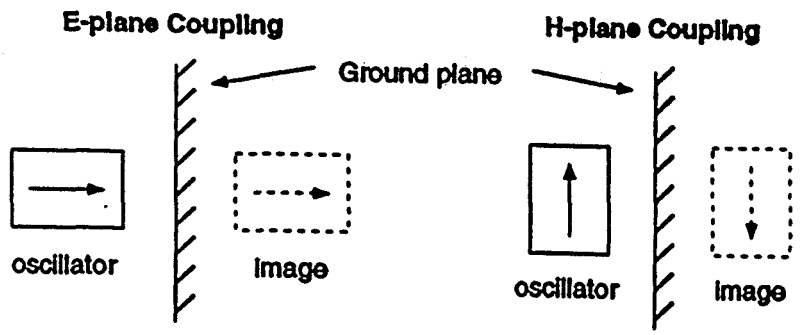


Figure 4.8 The idea of coupling coefficient measurement.

horizontal metal plate is a part of the grid-oscillator to provide the feedback necessary for oscillation. The grid-oscillator is imaged by the vertical metal plate, thus simulating two identical coupled oscillators. In order that the oscillator can be close enough to the image plane, we can either cut the substrate very close to one edge of its metal pattern or cut a slot on the vertical metal plate. The first method cannot reflect the real case of the circuit. So we use the second method. In the second method, to minimize the effect of the slot on the metal plate, the vertical metal plate is $\lambda_d/4$ thick, where λ_d is the wavelength of the dielectric substrate at the free-running frequency of the oscillator. The $\lambda_d/4$ thick metal plate with the slot is a one-quarter wavelength transmission line. It transforms the high impedance at the right side of the metal plane to the low impedance at the left side of the metal plane, such that the slot doesn't have much effect on the metal plate. Slipping the substrate back and forth, thus varying the spacing between the oscillator and its image, causes a frequency shift

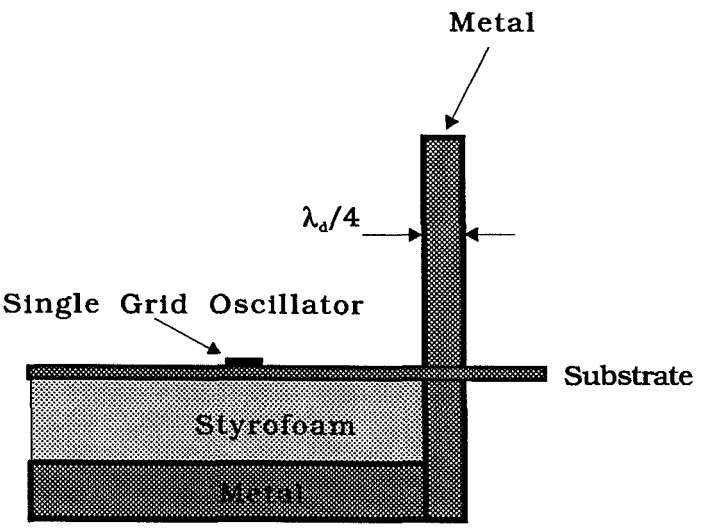


Figure 4.9 Setup for the coupling coefficient measurement. The horizontal metal plate is to provide the feedback necessary for oscillation for the grid-oscillator, and the vertical metal plate is to image the grid-oscillator.

that can be used to decide the spacing. In our measurement, the RF current direction is perpendicular to the vertical metal plane, so it is the case of E-plane coupling. From Equation (4.12) we can see that the zero-crossover with negative derivative is the desired spacing between the adjacent oscillators so that the coupling coefficient angle is 0°. The measured result is shown in Figure 4.10. When the horizontal metal plate is 18 mm away from the chips, the desired spacing between adjacent elements is 25 mm.

4.5 Grid-Oscillator Beam-Steering Array Measurement Results

The 2-element X-band HEMT grid-oscillator beam-steering array is shown in Figure 4.11. The two oscillators are with the same dimension and are built on the same piece of dielectric substrate with thickness of 15 mil and dielectric constant of 2.33. The dielectric substrate is mounted on the styrofoam with dielectric constant of approximately 1 and there is a mirror at the backside of

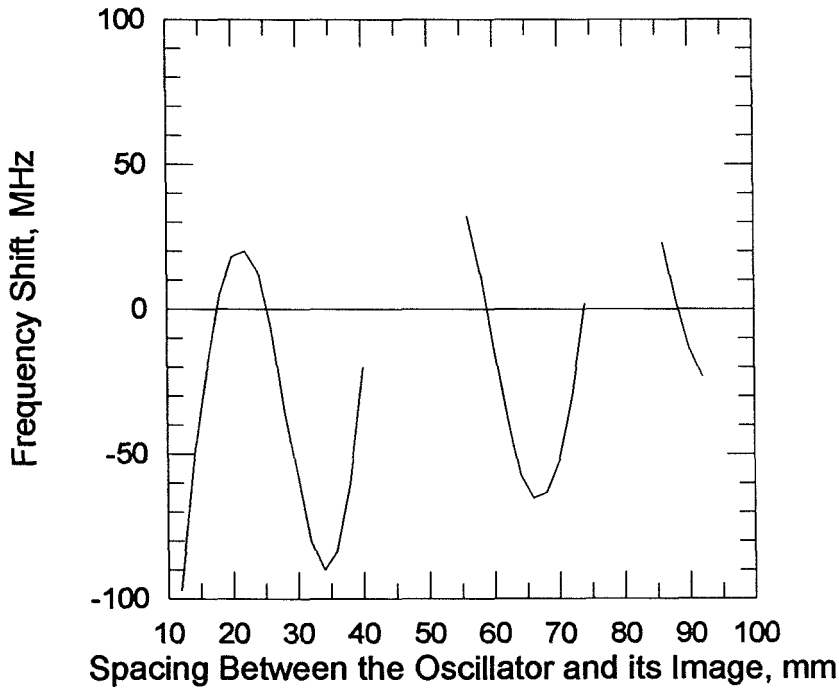


Figure 4.10 Measured frequency shift with spacing between the oscillator and its image. The horizontal plate is 18 mm away from the chips and the free running frequency is 10.87 GHz.

the chips. Given a mirror position, coupling coefficient can be measured to decide the appropriate spacing between the two elements such that the coupling phase angle $\Phi = 0°$.

From the above coupling coefficient measurement, when the mirror is 18 mm, the spacing between the adjacent oscillators is 25 mm. The two oscillators were tuned to a free running frequency of 11.013 GHz individually. When both oscillators were coupled, the received radiation pattern from these two oscillators was broadside and a phase-locked frequency of 11.02 GHz was observed. This frequency shift indicates that the coupling phase Φ was not zero.

Figure 4.12 shows the measured broadside pattern obtained from the array. A theoretical pattern is also shown for the H-plane pattern. The calculation of the theoretical H-plane pattern for the array is the same as that for the line-grid

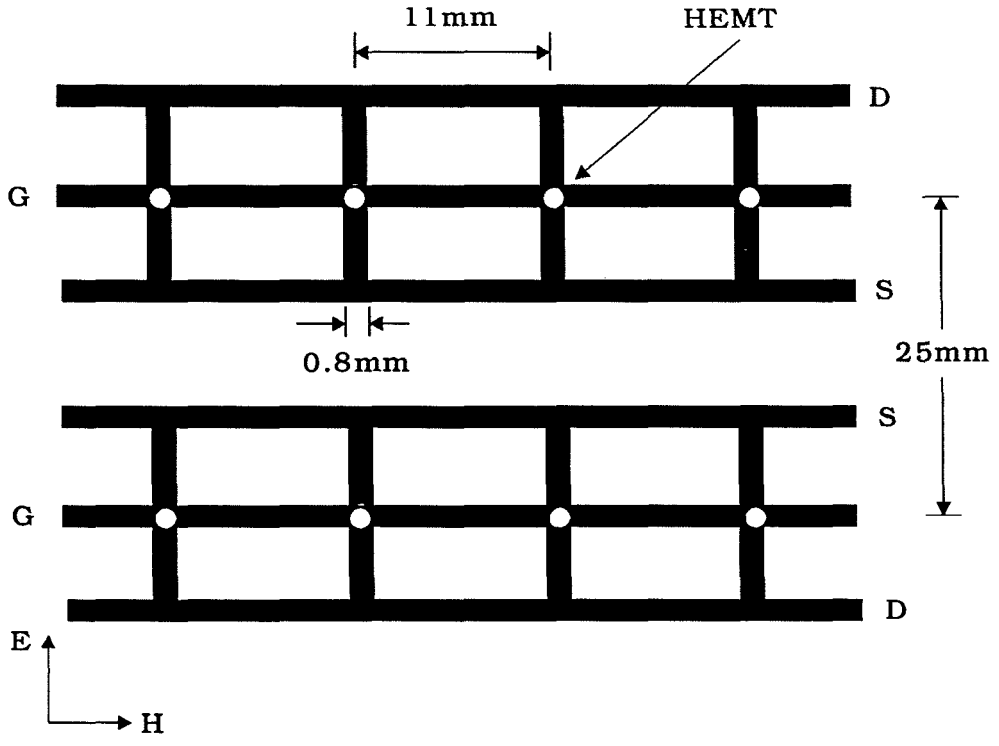


Figure 4.11 Grid-oscillator beam-steering array.

oscillator. This broadside pattern was obtained by setting all the oscillators' free running frequencies to 11.013 GHz.

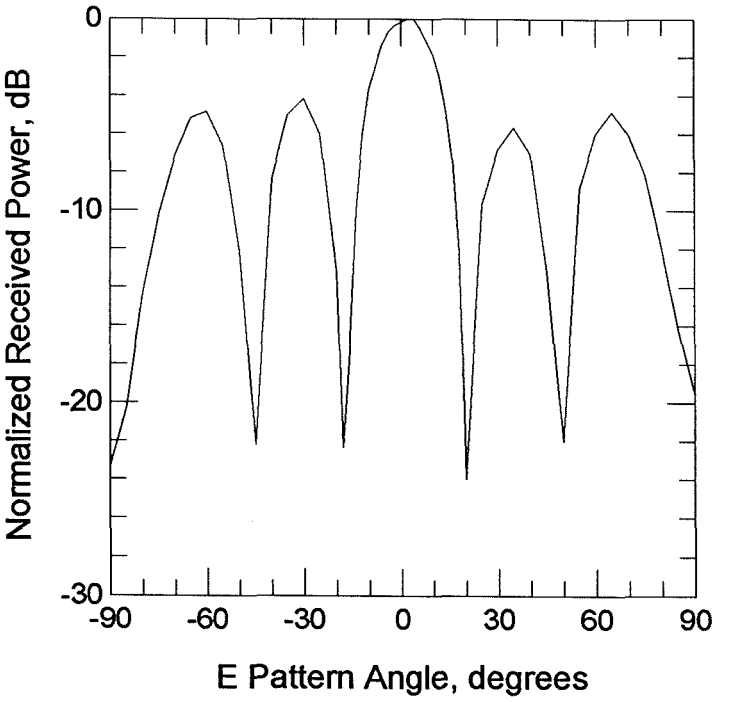
Measured radiation patterns indicating beam-steering in other directions are plotted in Figure 4.13. It was possible to continuously scan the radiation pattern from $-6.5°$ to $+5°$. When the pattern was steered to $-6.5°$, the free running frequencies of the two oscillators are 11.04 GHz and 11 GHz respectively. In the case of $+5°$ beam-steering, the free running frequencies are 10.987 GHz and 11.027 GHz respectively.

4.6 Discussion of the Measured E-Plane Pattern

In order to determine the phase shift of each element in the array, we need to find the effective distance between the elements. The broadside E-plane pattern for the two-element array shown in Figure 4.12(a) is used to determine the effective distance. The method is as follows: First the E-plane pattern for the beam-steering array is calculated by the following model which is shown in Figure 4.14. The electric field is

$$E \propto \cos(\frac{\pi d}{\lambda} \sin\theta) \sin(\frac{\pi d_2}{\lambda} \cos\theta) \cos\theta, \tag{4.13}$$

where the variables are defined in Figure 4.14, and $\cos\theta$ is for the radiating pattern of the element with the assumption that the radiating element is a dipole. Assuming the distance of d_2 is the physical separation between the two line-grid oscillators, we obtain the resulting theoretical E-plane pattern which is shown in Figure 4.15(a). Here the theory and measurement do not agree. However, if we assume the distance of d_2 to be 40 mm, we obtain the resulting theoretical E-plane pattern which is shown in Figure 4.15(b). Then the theory and measurement agree pretty well. After the effective distance is found, and if the scanning angle is known, the phase-shift can be determined using the Equation (4.2), where $\lambda = 27.27$ mm corresponding to frequency of 11 GHz, $d = 40$ mm, $\Delta\theta$ is the beam-steering angle and ϕ_m is the phase-shift to be determined. When the



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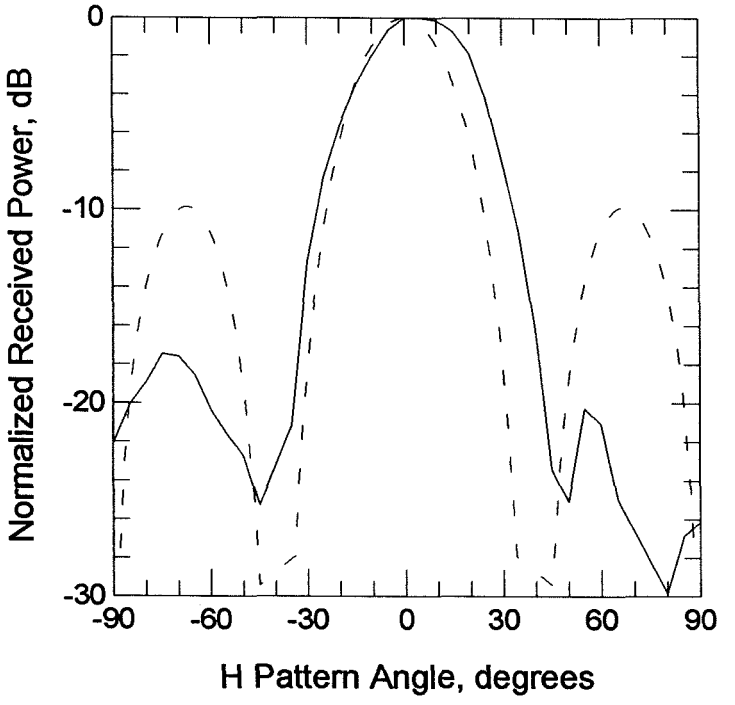


(b)

Figure 4.12 Measured and theoretical broadside patterns for the grid-oscillator beam-steering array. (a) E-plane radiation pattern. (b) H-plane radiation pattern. — measurement and - - - theory. The theory assumes that the mirror is 20 mm away from the array.

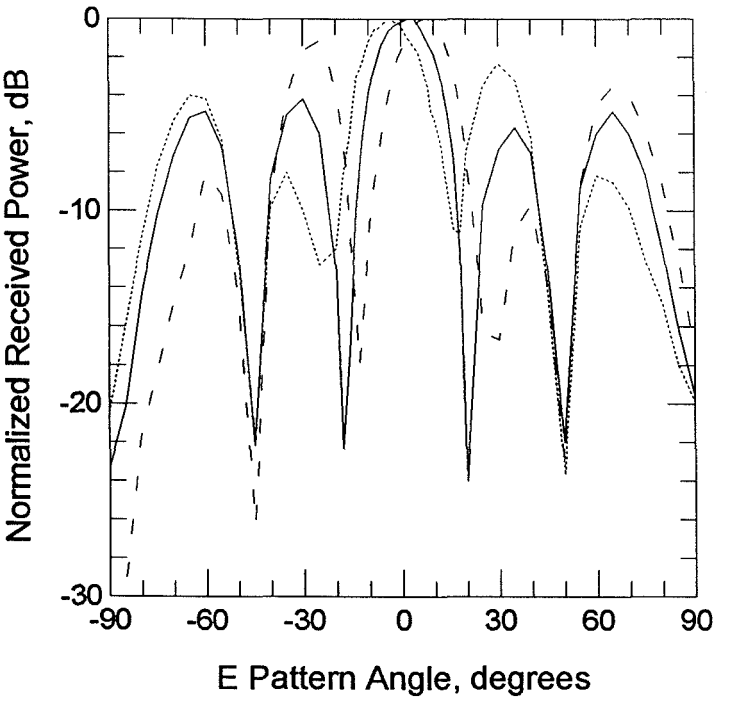


Figure 4.13 Comparison of measured E-plane radiation patterns at three different scan angles. — 0°, --- −6.5°, - - - 5°. f_1 and f_2 are the free-running frequencies of the two oscillators respectively. When the mirror is 18 mm away from the chips with the corresponding oscillator spacing of 25 mm, continuous beam-scanning was possible from −6.5° to +5° by adjusting the element frequencies.

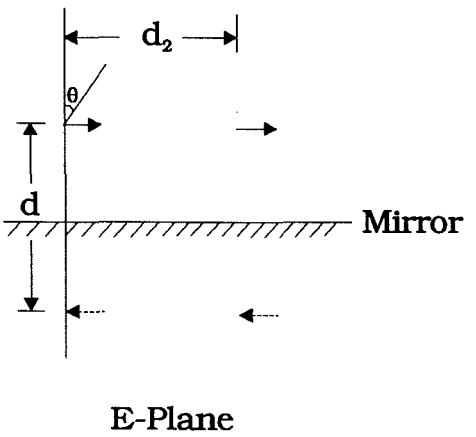
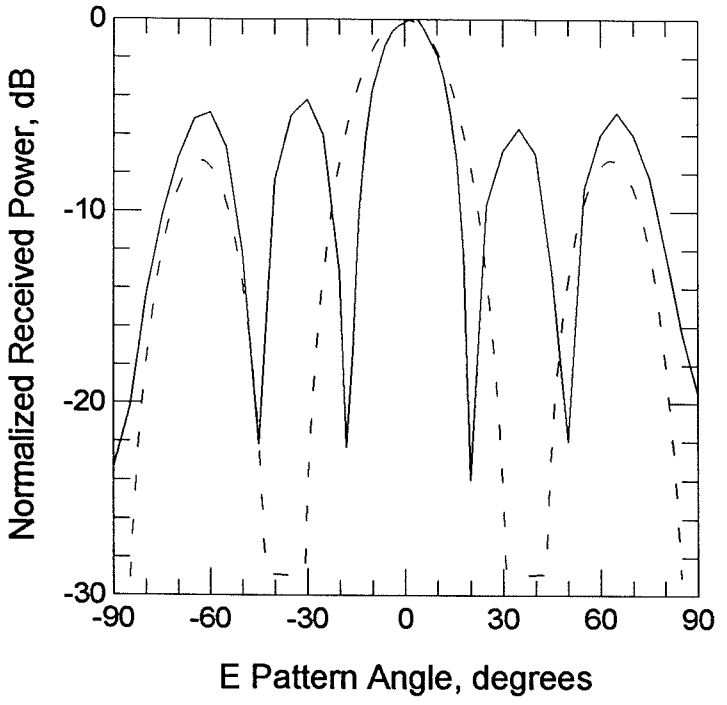


Figure 4.14 Theoretical model for the calculation of the E-plane pattern of the beam-steering array.



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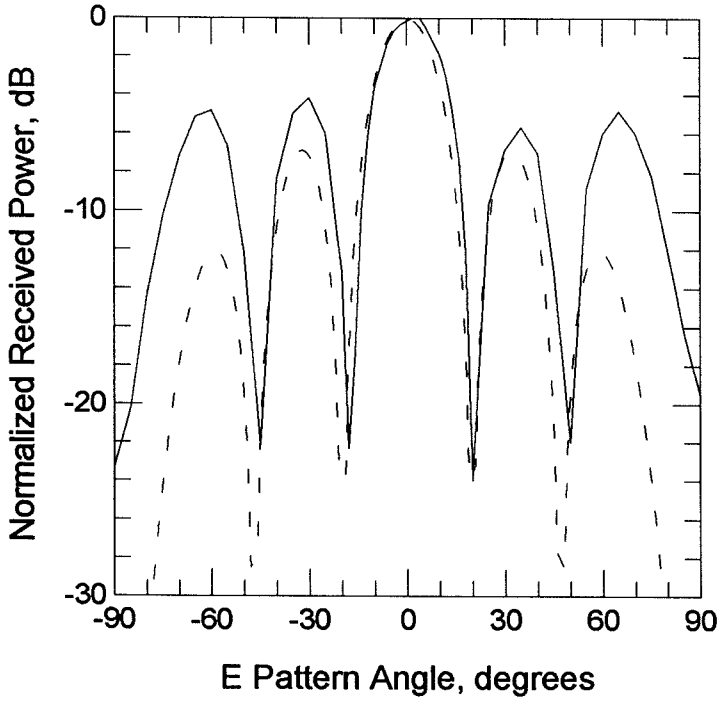

(b)

Figure 4.15 Comparison of the theoretical E-plane pattern and the measured E-plane pattern. — Measurement and - - - Theory. The mirror is assumed to be 20 mm away from the array. (a) The effective distance d_2 is assumed to be the physical distance of 25 mm. (b) The effective distance d_2 is assumed to be 40 mm.

array scans from $-6.5°$ to $5°$, the corresponding phase-shift for each element is calculated to be from $-60°$ to $46°$. The theoretical phase-shift is from $-90°$ to $90°$. As a comparison, the phase-shift for York's circuit is from $-79°$ to $66°$.

4.7 Summary

A 2-element X-band planar grid-oscillator beam-steering array without using any phase shifters has been demonstrated. For the array with the adjacent radiating element spacing of 25 mm and a mirror 18 mm away from the HEMT chips, continuous beam-steering was possible from $-6.5°$ to $+5°$ by detuning the free running frequencies of the elements in the array. This is the maximum scanning angle which can be achieved using different mirror positions. The theoretical maximum beam-scanning angle corresponding to this array is $\pm 15.8°$. It is not clear why the array is unable to achieve the theoretical maximum range. Some possible causes are that the coupling phase is not exactly $0°$, the nonuniformity of the oscillators' amplitudes, and the fact that the oscillators were not modelled exactly by the simple van der Pol equation.

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Chapter 5

Discussion and Suggestions for Future Work

In the previous chapters we have introduced the Class-E amplifier and demonstrated UHF and X-band Class-E amplifiers. The Class-E amplifiers employ the simplest output load network which is an LC series tuned circuit. They are narrow band amplifiers and the output power and efficiency is highly dependent on the frequency because the circuit is tuned to a frequency lower than the operating frequency. A more complicated configuration can be designed for broadband operation. In [1], Everard describes the techniques of broadband Class-E amplifier design and developed a 130 to 180 MHz Class-E amplifier using these techniques. In the design, the output circuit is combined with a broadband matching network and a third order bandpass filter to reduce the output power at the harmonics. The filter is based on a Chebyshev low-pass filter design and is converted to a bandpass filter. A large signal model of the device is developed and used in order to make an accurate computer simulation of the Class-E amplifier. The model is based on DC and small signal S-parameter measurements. The nonlinearities incorporated in the model include the nonlinear transconductance of the device, the reverse biased diode inherent in the MOS structure, and nonlinear feedback and output capacitors.

For the 440-MHz Class-E high efficiency amplifier described in Chapter 2, the VSWR at the input is high. It is found in the MDS design that if the input matching circuit component values are optimized for the output power and drain efficiency, the input is not matched, while if the input is matched, the output

power and drain efficiency degrade. This input matching problem needs to be solved because the driver cannot take such big reflected power in most cases.

MOSFET's are suitable for Class-E high efficiency power amplifier applications and the development of MOSFET's for high power devices at higher frequencies are very promising. Compared with bipolar transistors, RF power MOSFET's exhibit higher gain, higher input impedance, enhanced thermal stability, and low noise. MOSFET's with higher power and higher efficiency have been developed. In the 440 MHz Class-E amplifier, the Motorola MRF183 MOSFET is used. MRF183 should work well to 1 GHz. At 945 MHz, it has output power of 45 W PEP, gain of 13 dB, and efficiency of 36%. At present Motorola has MOSFET devices with even higher output power at 1 GHz. The MRF184 has output power of 60 W, gain of 15 dB at 1 GHz, and efficiency of 60%. MRF185 has output power of 85 W, gain of 14 dB, and efficiency of 55%. Also Motorola has developed MOSFET's working at higher frequency. The MRF284 works up to 2.6 GHz. It has an output power of 30 W, gain of 10.5 dB, and efficiency of 33%.

Although the power semiconductor chips are made from Silicon and GaAs today, theoretical analysis [2] shows that Silicon Carbide (SiC) has demonstrated the ability to function under extreme high-temperature, high-power, and/or high-radiation conditions. SiC is becoming to be the most attractive material for use in high-temperature, high frequency, and radiation-intensive device applications. In [3], high temperature performances of SiC and Silicon devices are measured and compared. Although the Silicon devices have shown better performance at low temperatures, the SiC devices can be useful at high temperatures (above 150°C), where Silicon devices cannot be used. Theoretical analysis has indicated that SiC power MOSFET's and diode rectifiers would operate over higher voltage and temperature ranges, have superior switching characteristics, and yet have die sizes nearly 20 times smaller than correspondingly rated Silicon-based devices [2].

These tremendous theoretical advantages have yet to be realized in experimental SiC devices. This is mainly due to the fact that SiC's relatively immature crystal growth and device fabrication technologies are not yet sufficiently developed to the degree required for reliable incorporation into electronic systems. However, prototype SiC electronic devices have been demonstrated with very good DC and RF performance. In [4], a UHF SiC power module with 400 W and an S-band SiC SIT (Static Induction Transistor) of 200 W are demonstrated. With the SiC device fabrication processes well developed, high power, high frequency, and high temperature Class-E amplifiers can be expected with the SiC MOSFET.

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