

Chapter 4

Wire Array Transfer to Polymer Films and Substrate Reuse

4.1 Introduction

The VLS growth of Si structures provides a route to fabricate vertically aligned wires of highly uniform, tunable dimensions that can be studied to determine the optimal Si wire array geometry for solar energy conversion. The wires can be grown at high growth rates under atmospheric pressure using the inexpensive gas precursor SiCl_4 .^{25, 118, 119} High-quality wire arrays are attainable with the relatively abundant catalysts Cu or Ni. These metals can be selectively placed in the patterned oxide buffer layer on the substrate using electrodeposition to minimize catalyst waste. Together these advantages of the VLS growth process are encouraging for the prospect of using this scheme to fabricate low-cost Si wire array solar cells. However, the necessary inclusion of a pure, single-crystal Si wafer to grow highly uniform wire arrays detracts from the purpose of using radial junctions to make solar cells out of inexpensive materials.

Si wire array photovoltaics cannot afford to sacrifice a single-crystal substrate with the fabrication of every array if they are to eventually become economically competitive. To

address this issue, we have developed a scheme in which the wires are transferred to a low-cost film and the substrate is recycled to grow subsequent wire arrays (Figure 4.1). The array order is preserved in a durable, transparent polymer in a flexible, processible form. The expense of the Si substrate is amortized over numerous wire array growth cycles. The polymer-embedding procedure should be applicable in a roll-to-roll processing scheme, contributing to the scalability of wire array solar cell fabrication.

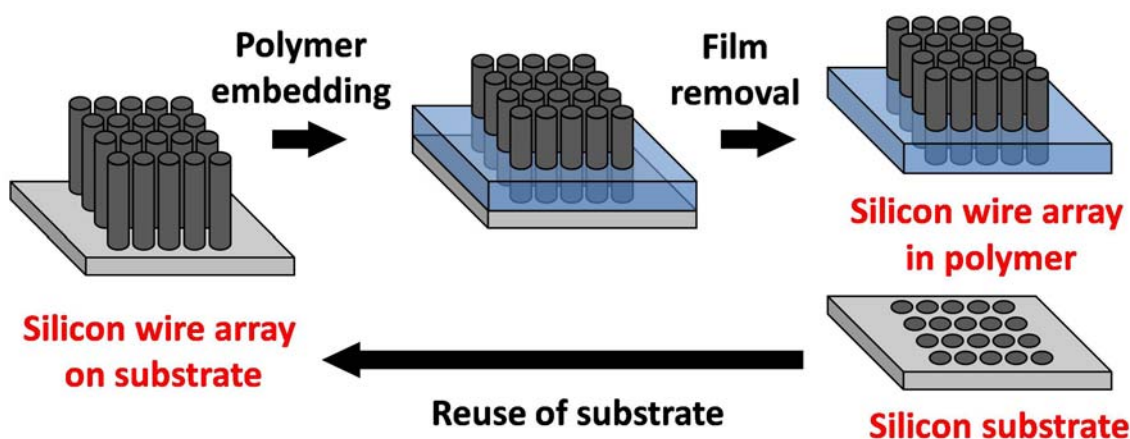


Figure 4.1. Schematic for Si wire array transfer and substrate reuse. The wire array is embedded in a low-cost, durable, transparent polymer and removed from the underlying substrate. The substrate, a single-crystal Si(111) wafer with a patterned thermal oxide surface, is recycled to grow additional Si wire arrays.

4.2 Wire Array Transfer to Polymer Films

4.2.1 Choice of Polymer and Deposition Method

The polymer to be used for wire array transfer must meet several criteria to successfully work in this application. It should be highly transparent to visible light at thicknesses of $\sim 100\ \mu\text{m}$ to prevent it from having a significant parasitic effect on the absorbance of the Si wires. The polymer should be able to conformally coat the wires and adhere to them

strongly enough to maintain their location and order when the film is removed from the substrate. It also needs to be structurally robust enough to hold together as a substrate-free film of $< 100\ \mu\text{m}$.

Chlorinated polypropylene was the first polymer investigated for this application. Polypropylene (PP) is an inexpensive polymer commonly used in plastics that is highly transparent to visible light. Initial attempts to dissolve chlorinated PP in dichloromethane (DCM) and dropcast it onto Si wire arrays resulted in clumps of PP at the tops of the wires only. However, thin films of PP of approximately uniform thickness were conformally coated on Si wire arrays (Figure 4.2a) by dissolving 0.1 g of chlorinated PP (Aldrich) in 10 mL of DCM (99.9%, Aldrich) in a scintillation vial, placing the wire array in the solution with the wires facing upward, and allowing the solution to evaporate slowly over several hours. The resulting thin plastic/Si wire array film was mechanically removed from the substrate using a razor blade. The majority of the PP film area failed to hold the Si wires in place, causing the bottom of the polymer film to be covered in loose wires and to have periodic holes consistent with the wire size and pattern (Figure 4.2b). Considering that shear forces from the razor blade procedure may have dislodged the wires from the polymer film, a sonication approach to film removal was tried. However, sonication was not powerful enough to break the wires loose from the substrate when they were embedded in the PP film.

Poly(ethylene-co-vinyl acetate) (PEVA) was also used to make Si wire/polymer composite films. Dissolving PEVA (18% vinyl acetate, Aldrich) in DCM and allowing a slow evaporation as before, however, led to a highly cracked thin film of polymer on the

wire array. Conformal coating of the wires was achieved by heating PEVA ($>190\text{ }^{\circ}\text{C}$) on a sample until it liquefied and wicked into the wire array (Figure 4.2c). Removal of these films from the substrate yielded a PEVA/Si wire composite chip that maintained the wire placement and pattern fidelity in the polymer (Figure 4.2d). With this deposition method for PEVA, however, it was difficult to control the polymer thickness over large areas, and upon cooling, the polymer was hard and brittle. Using a razor blade to remove the PEVA layer resulted in many chips of polymer/wire material rather than a single continuous film.

These issues were overcome by using polydimethylsiloxane (PDMS) as the polymer layer. PDMS has been widely studied in microfluidics applications¹²⁵⁻¹²⁸ and has been observed to be a durable material that is quite chemically stable.¹²⁹ PDMS is also highly transparent in the UV/visible regions of the solar spectrum.¹²⁸ The PDMS elastomer base and curing agent (Sylgard 184, Dow Corning) were mixed in a 10:1 w/w ratio and stirred thoroughly before spin coating onto a Si wire array at 3000 rpm for 1 min. The wafer was then heated at $120\text{ }^{\circ}\text{C}$ for $> 2\text{ h}$ to cure the PDMS. PDMS/wire composite films were carefully removed from the underlying Si growth substrate using a razor blade. The PDMS conformally covered the wires, leaving only their bases exposed from the peeled layer (Figure 4.2e). Despite the high flexibility of the PDMS film, the wires were always observed to maintain their position within the polymer matrix (Figure 4.2f), due to the large adhesive force between PDMS and SiO_2 surfaces.¹³⁰

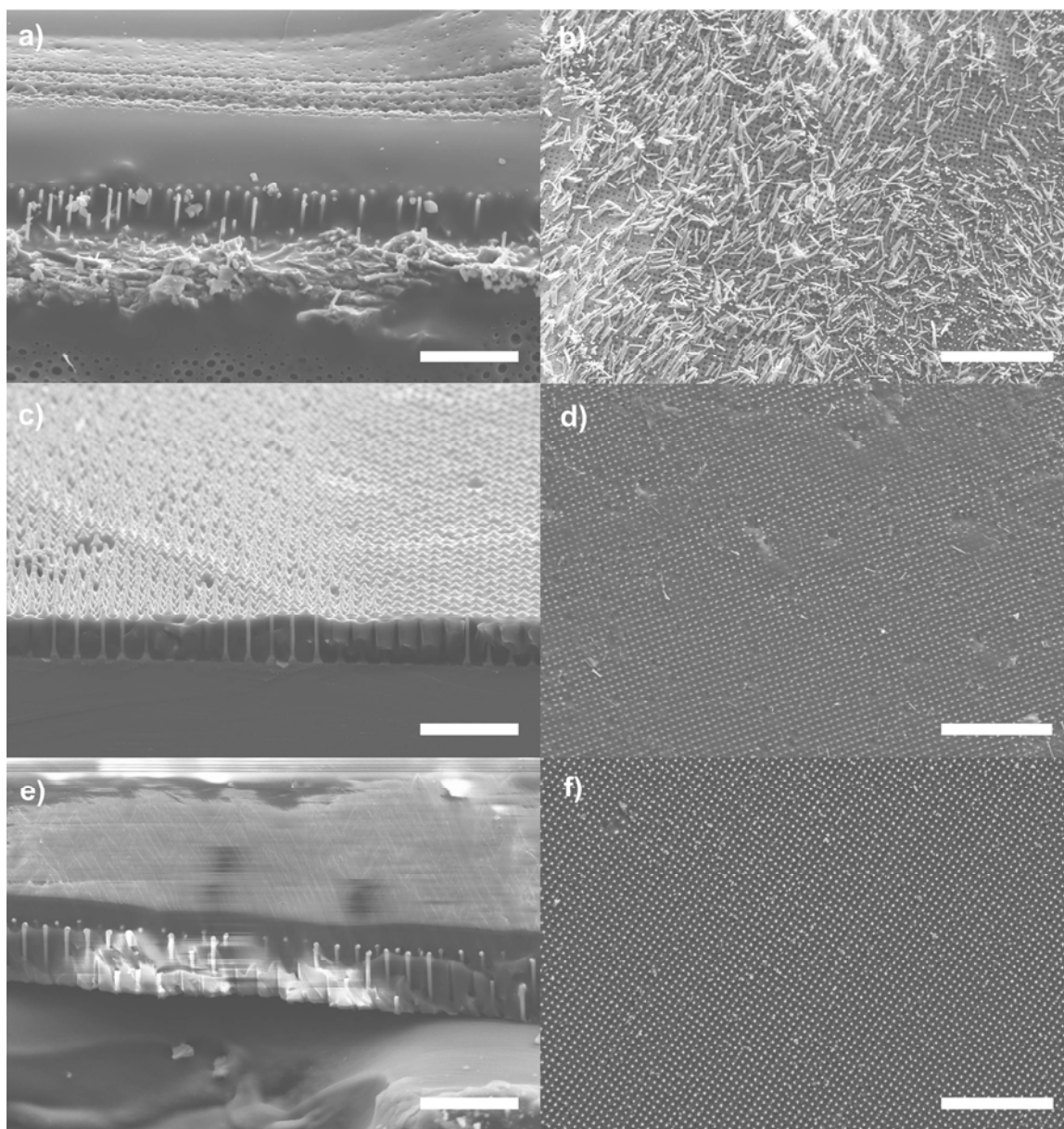


Figure 4.2. Wire array transfer to different polymer films. SEM images of Si wire arrays infiltrated with **(a,b)** chlorinated polypropylene, **(c,d)** polyethylene, 18% vinyl acetate, and **(e,f)** polydimethylsiloxane. **(a,c,e)** Cross-sectional view of the arrays and **(b,d,f)** top-down view of the bottom of the films after peeling from the substrate with a razor blade. Scale bar for **(a,c,e)** is 40 μm and for **(b,d,f)** is 100 μm .

4.2.2 Peeled, PDMS-Embedded Si Wire Arrays²

The PDMS curing and peeling process produced flexible, polymer-supported arrays of crystalline Si wires embedded within a transparent, mechanically and chemically robust, film (Figure 4.3a).¹²⁹ Si wire arrays with areas $> 1 \text{ cm}^2$ were transferred to a single polymer sheet (Figure 4.3b). The area of the wire-embedded film was limited only by the size of the initial array, which in turn was limited by the size of the reactor tube used to fabricate the Si wire arrays. Cross-sectional SEM images of the PDMS/Si wire array composite films revealed intimate contact between the wires and the polymer (Figure 4.4a). The as-removed films could be bent or rolled into cylinders having diameters as small as several millimeters without damaging or dislodging the embedded Si wires (Figure 4.4d). The polymer/wire composite also maintained the spacing, cubic unit cell, and orientation of the wires prior to casting. Diffraction of visible light was used to verify the embedded wire spacing and periodicity in the PDMS films. A 670 nm diode laser normally incident to a flat sample surface produced a cubic array of diffraction spots (Figure 4.3c) with a diffraction angle indicating an array spacing of $6.9 \pm 0.2 \text{ }\mu\text{m}$, in agreement with the photolithography mask's square arrangement with a center-to-center pitch of $7 \text{ }\mu\text{m}$. Up to 4 orders of diffraction were observed even after mechanical deformation of the films. The wire array/polymer composites were highly light absorbing and/or scattering at the angles shown (Figures 4.3a and 4.3b), despite the high transparency of PDMS in the visible region of the solar spectrum and the top-down density of Si wires being only $\sim 4\%$ of the projected area of the film. This finding is in

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agreement with the reported enhanced light absorption in wire arrays^{55, 122, 131} and suggests that these composite films may have direct application in solar energy-conversion devices.^{met}

The thickness of the PDMS film determined both the structural integrity of the composite and the extent to which the wires were exposed. PDMS/Si wire sheets were prepared in which one (Figure 4.4a) or both (Figures 4.4b-d) ends of the Si wires were exposed, allowing for subsequent formation of electrical contacts to the Si wires. Thicker layers with only the bases of the Si wires exposed from the polymer were fabricated as described above (see Section 4.2.1). To produce thinner polymer films, a low-boiling-point siloxane was added to the PDMS solution that was used to embed the wires. Hexamethylcyclotrisiloxane (HMCTS, 98%, Alfa Aesar) was dissolved in dichloromethane (until saturation, ~ 4 g HMCTS/5 mL DCM), then mixed with Sylgard 184 polydimethylsiloxane (Dow Corning) in a 4.4: 1.0: 0.1 (HMCTS: PDMS base: PDMS curing agent) w/w ratio, not including the DCM weight. This mixture was spin coated onto the wire arrays at 1000 rpm for 1 min, then heated at 150 °C for 30 min. The HMCTS evaporated rapidly at this temperature without cross-linking into the PDMS, which allowed the polymer to contract below the tips of the wires and cure conformally at the base. This left a 10 – 20 µm thick layer of PDMS at the bottoms of the Si wires, leaving the majority of the wire length exposed (Figures 4.4b-d). The wire arrays in such films were electrically conductive from top to bottom, but exhibited immeasurably high resistances laterally. This observation indicated that the embedded Si wires extended

through the polymer film and were also electrically isolated from each other by the polymer matrix.

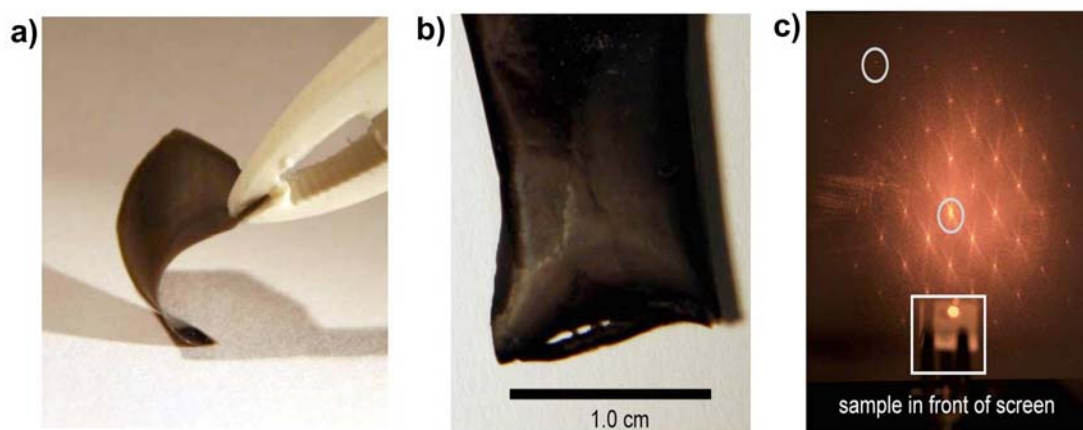


Figure 4.3. Flexible, PDMS-embedded Si wire array films. (a) Demonstration of the flexibility of a PDMS-embedded Si wire array (held by tweezers) and of the (b) large area ($> 1 \text{ cm}^2$) and nearly black color achievable in these films. (c) Optical diffraction pattern resulting from transmitted laser light, indicating the long-range order of the array. The center (zero-order diffraction) and outer (4^{th} -order diffraction) spots are circled (image credit: K.E. Plass).

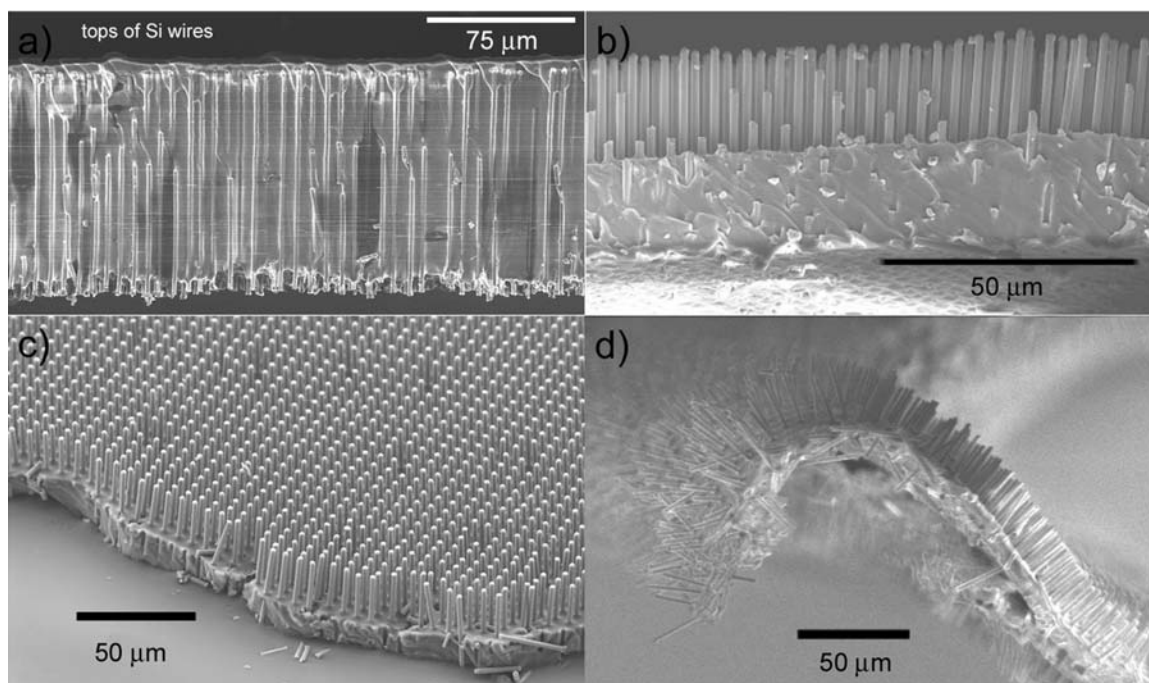


Figure 4.4. SEM images of cross-sections of embedded Si wire arrays of two different polymer thicknesses. (a) A composite film fabricated without a low-boiling point siloxane additive. Upon removal from the growth substrate, wires were exposed only at the bottom of the film. Note the conformal filling of the gaps between wires. (b-d) The thinner composite film fabricated with the addition of a low-boiling point siloxane had a significant fraction of the wire length emerging from the polymer while the array pattern was maintained. (b) The bottom of the film can be seen, demonstrating that the rods passed through the polymer. (c) The array order from the top of the film is visible. (d) The films remained flexible even while containing ordered arrays of single-crystalline wires.

4.2.3 Polymer-Embedded Wire Array Densification

The ability to transfer wire arrays from their rigid epitaxial growth substrate into a flexible organic layer opens new avenues for manipulating the array geometry. For example, chemically or thermally shrinking the polymer matrix can increase the wire density without requiring short nearest-neighbor distances during the initial growth step and represents a means of further improving the light absorption/trapping of such films. Densification of the wire array in a polymer film is therefore a potential way to increase the packing density of the wires beyond the limits imposed by the wet chemical etch patterning of the thermal oxide buffer layer during array fabrication (see Section 3.7.2).

Thermally shrinking the composite film by utilizing a polymer similar to that used in heat-shrink tubing (e.g., polyethylene, polypropylene, etc.) would seem a straightforward route to densify peeled wire array layers. However, heat-shrink plastics are typically prepared by irradiating the polymer to induce cross-linking of the chains, heating and stretching it, then slowly cooling the plastic so that it retains an extended, non-equilibrium shape. Upon annealing past a critical temperature, the plastic will relax back to its smaller state.¹³² It would be very challenging to cast these polymers on a wire array and peel them in the non-equilibrium state, which would be necessary to gain the benefit of densification from this type of thermal shrinkage.

Instead, an approach was investigated in which a volume-filling molecule was added to a cross-linked polymer during the wire array coating, then removed by a liquid extraction step after peeling the wire/polymer composite film. In this process, 5 g hexamethylcyclotrisiloxane (HMCTS, 98%, Alfa Aesar) was mixed with 1 g Sylgard 184 PDMS (Dow Corning), then heated at 150 °C and stirred to liquefy the HMCTS. A

substrate-attached wire array was immersed in a beaker full of this siloxane mixture and heated at 150 °C for ~ 30 min. The wire array sample was elevated on a metal stand ~ 1 cm from the bottom of the beaker to prevent bubbles from curing in the wire array. Although it boils at this temperature, the presence of excess HMCTS ensured that much of it remained in the beaker for a sufficient length of time to be incorporated into the cured PDMS film. The wire array sample was then cut from the cured PDMS block and peeled from the substrate using a razor blade. For the liquid extraction of the HMCTS, the polymer-embedded film was immersed in dichloromethane for > 10 h, then immersed in acetone for > 3 h, then immersed in water for > 1 h, and finally allowed to dry under air for > 2 h. An example wire/polymer composite film made from this process weighed 0.0289 g before the liquid extraction and 0.0135 g afterward.

This procedure successfully led to the densification of the Si wire array through a volume contraction of the peeled PDMS film. SEM images of the bottom of the shrunken film (Figures 4.5b and 4.5d) show wires packed noticeably denser than either the wire stubs left behind on the wafer after peeling (Figure 4.5a) or the wire array before polymer embedding (Figure 4.5c). The projected area of the Si wire array was reduced by as much as 70% from the densification process (Figure 4.5e).

Although this is an encouraging step towards increasing the packing density of wire arrays through post-growth processing, this method has key shortcomings that need to be improved for densification to be included in a final wire array solar cell fabrication scheme. Not all areas of the polymer film appeared to densify equally, with some locations maintaining approximately the same wire-to-wire pitch as before polymer embedding. Parts of the film have microscopic gaps in the PDMS layer surrounding the

wires rather than a single continuous polymer sheet (Figure 4.5f). Finally, the polymer deposition method used for densification does not allow control over the thickness of the film on the micron scale required to be able to expose both ends of the Si wires for contacting. Hexaphenylcyclotrisiloxane (Gelest, Inc.), a cyclic siloxane molecule similar to HMCTS that should not cross-link with PDMS (but with a higher boiling point, ~ 300 °C), may allow thinner films to be deposited and densified. Initial attempts to use this molecule, however, have so far met with difficulty in getting it to mix well with PDMS.

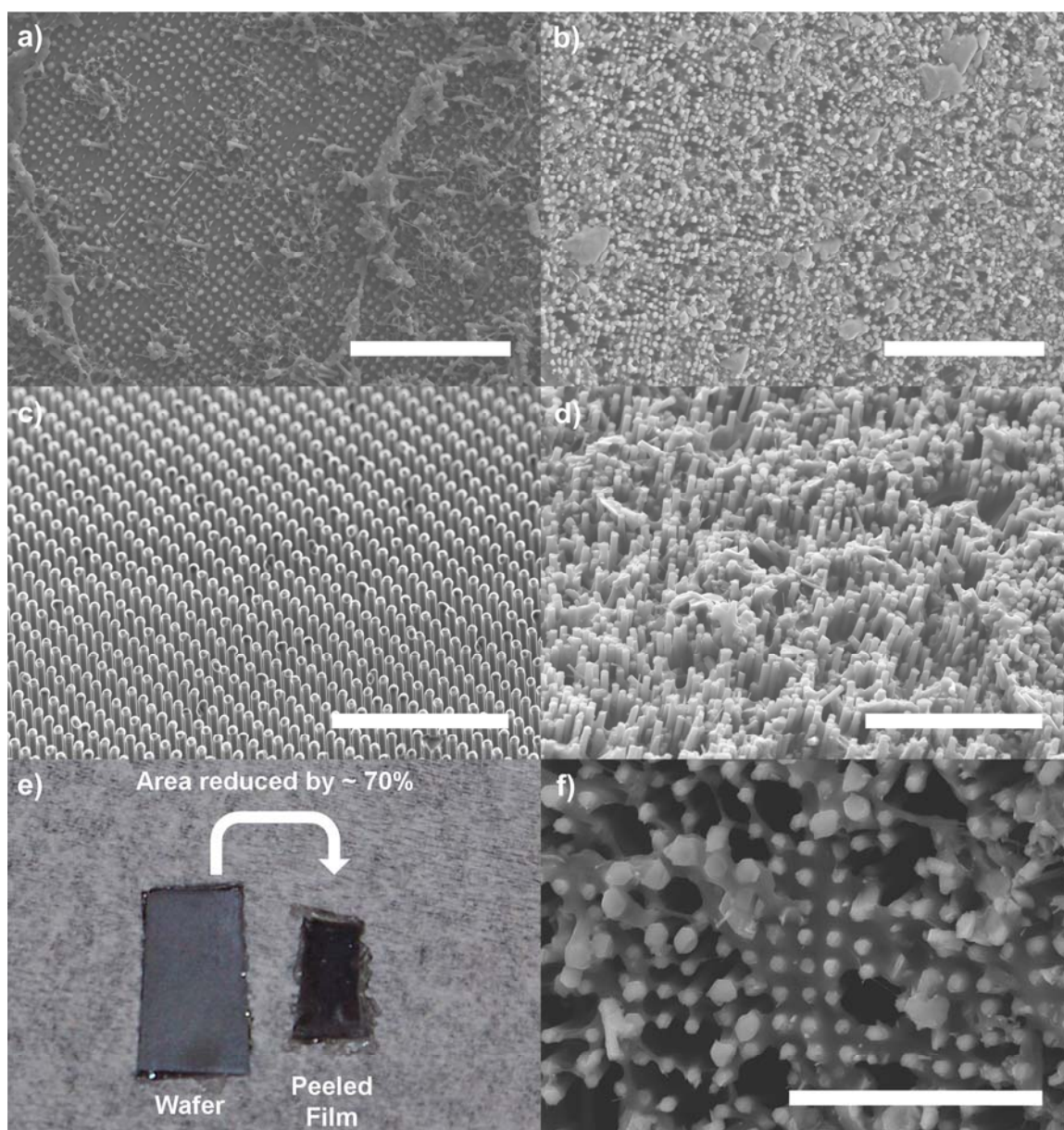


Figure 4.5. Densification of wire arrays by volume contraction of PDMS films. (a,b) Top-down view SEM images of (a) the growth substrate surface after polymer film removal and (b) the bottom of the PDMS/wire composite film after peeling from the substrate and densification. (c,d) Tilted-view SEM images of (c) a Si wire array before transfer to a polymer film and (d) the bottom of the PDMS/wire composite film after peeling from the substrate and densification. (e) After densification by liquid extraction of the volume-filling species, the projected area of the array was reduced by up to $\sim 70\%$. (f) SEM image of the bottom of a peeled film after the densification procedure displaying an area where the wire array did not significantly densify and the PDMS layer was no longer continuous. Scale bar is $100\ \mu\text{m}$ for (a,b) and $40\ \mu\text{m}$ for (b,c,f).

4.3 Reuse of the Substrate to Grow Multiple Si Wire Arrays³

4.3.1 Wire Regrowth by Regeneration of the Oxide Buffer Template

To minimize the expense associated with using a single-crystal Si wafer, a method was developed to recycle the substrate repeatedly for the production of multiple high-quality Si wire arrays. The first-generation Si wire arrays were fabricated by epitaxial VLS growth on a Si wafer by the procedure described in Section 3.5.3.¹¹⁹ Here, a highly doped Si(111) wafer (330 - 430 μm thick n-type Si, doped with Sb to a resistivity of 0.005 – 0.02 $\Omega\text{-cm}$, International Wafer Service, Inc.) with 300 nm of a thermally grown silicon oxide was used as the growth substrate. 300 nm of Au was thermally evaporated onto the photolithographic pattern, resulting in a square array of 3 μm diameter Au islands, having a center-to-center pitch of 7 μm , separated by the SiO_2 layer. Using SiCl_4 (see Section 3.5.3), highly uniform, vertically aligned, crystalline Si wires were fabricated over areas $> 1 \text{ cm}^2$ (Figure 4.6a). The wire array dimensions and pore spacing used in this work were chosen based on an available lithography mask, to facilitate comparison to previous results.¹¹⁹ Other wire diameters and center-to-center pitches could be produced by the use of other masks, to the limit of the resolution and pore-size fidelity that can be accommodated by the development and etching steps. The optimal catalyst volume is readily calculated for a given wire radius from the surface tension of the Au meniscus on the growing Si wire (see Section 3.7.2),^{100, 105} and requires a SiO_2 buffer layer with a thickness approximately equal to that of the deposited metal.

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A 10:1 w/w ratio of polydimethylsiloxane (PDMS) and a curing agent (Sylgard 184, Dow Corning) was applied to the top of the wire array by spin coating at 3000 rpm. The sample was then heated for 2 h at 120 °C to cure and solidify the polymer. Scanning electron microscopy (SEM) images confirmed that the PDMS fully infiltrated the Si wire array. The polymer film and the embedded Si wires were then removed by scraping the wafer surface with a razor blade. This transfer approach preserved the pattern fidelity and vertical alignment of the wires within the polymer matrix (Figure 4.6b).

After the removal of the PDMS layer, residual stubs of broken Si wires, 2 μm long or less, along with some polymer residue, were observable at the wafer surface (Figure 4.6c). To enable wire regrowth, the wafers were immersed for 90 s in 4.5 M KOH(aq) at 80 °C with stirring.⁹⁶ At elevated temperatures, KOH(aq) etches the Si(100) and (110) planes approximately two orders of magnitude faster than it etches the Si(111) plane. Furthermore, the etch rate for Si is significantly faster than that for SiO₂.⁹⁶ The KOH(aq) thus selectively etched the Si stubs as well as the polymer residue. After etching, the original oxide hole pattern remained, with the Si(111) substrate exposed at the bottom of each hole (Figure 4.6d). Because the KOH(aq) etch does eventually remove the oxide, however, this step must be kept as brief as possible, and it was determined empirically that 90 s was generally sufficient to remove the Si wire stubs and the PDMS residue.

Electrodeposition was then used to redeposit the VLS catalyst into the holes in the oxide. The deposition of Au catalyst was conducted by forming electrodes and using them in an electrodeposition bath as described in Section 3.7.3. Relatively low current densities (0.4 to 0.8 mA cm⁻² of exposed wafer area between the Si working electrode and the Pt gauze counter electrode) and Si wafers of high conductivity were required to

electrodeposit uniform layers of Au selectively inside the oxide pattern (Figure 4.6e). The deposition was allowed to proceed galvanostatically until 0.12 C cm^{-2} of charge had been passed, yielding Au catalyst arrays of $3 \text{ }\mu\text{m}$ diameter and approximately 300 nm thickness over areas $> 1 \text{ cm}^2$. With sufficiently deep pores, no limit has yet been observed for the thickness of Au that can be homogeneously deposited by the electroplating method. The wafer, with metal catalyst deposits in the patterned holes in the oxide layer, was then recovered from the electrode.

This substrate was placed back into the reactor for VLS-catalyzed wire growth, under the same conditions used to grow the first-generation Si wire arrays on the Si(111) substrate, including the 20 min anneal step. The regrown Si wires were between 70 and $100 \text{ }\mu\text{m}$ long, with the wires in any single growth run of a uniform height distribution. The entire process was repeated to fabricate a third and fourth generation of wires. No appreciable differences in wire length, diameter, vertical orientation, or morphology were detected between growth generations (Figure 4.6f).

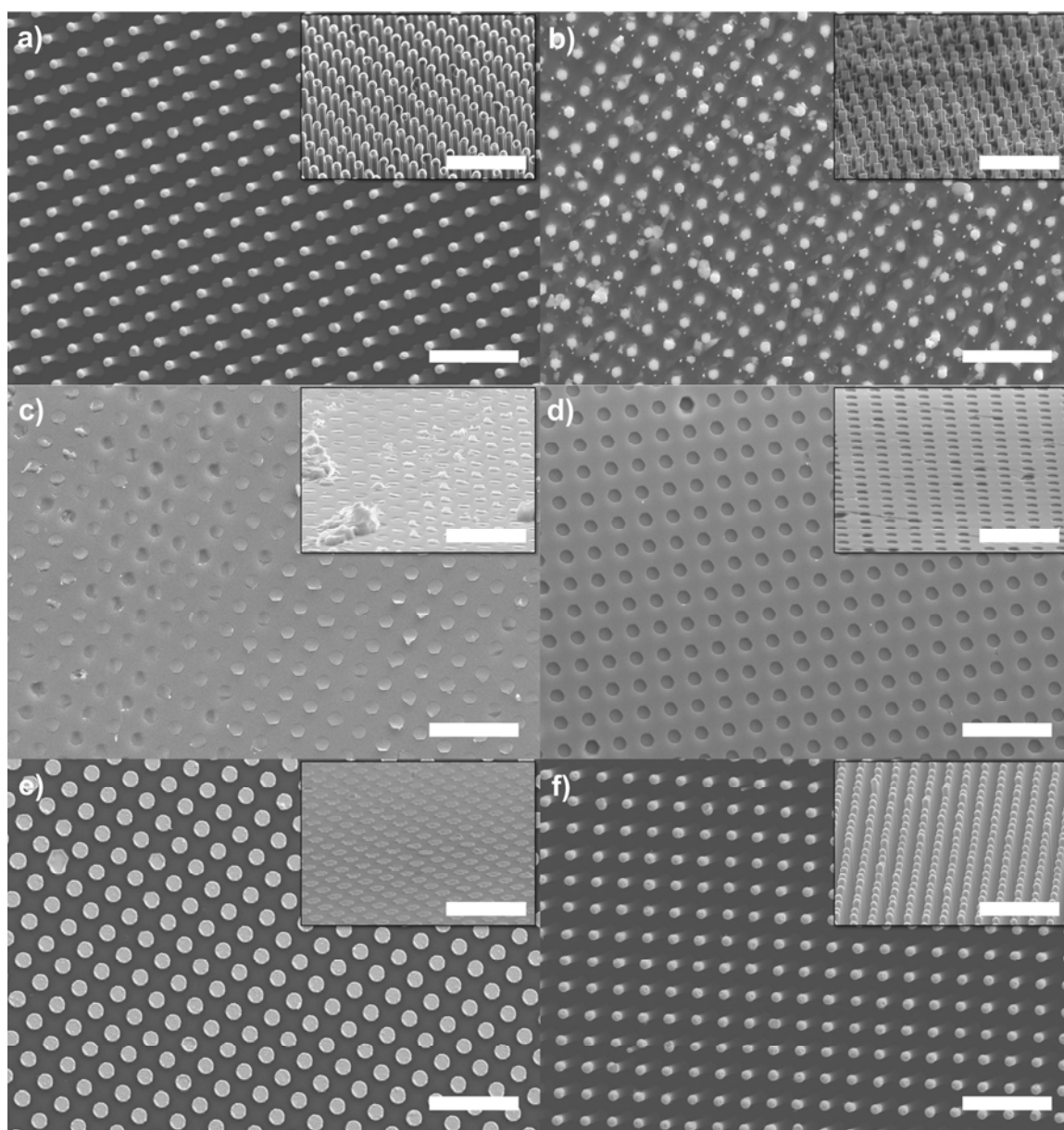


Figure 4.6. The wire array regrowth process. Top-down and 70° tilted-view (insets) SEM images. **(a)** The first-generation wire array was **(b)** peeled in PDMS, leaving behind **(c)** a wafer surface with wire stubs and polymer residue. **(d)** The oxide pattern was recovered with a KOH(aq) etch, **(e)** Au catalyst was electrodeposited into the holes, and **(f)** a new wire array was regrown from the wafer. The scale bar is 20 μm in all images.

4.3.2 Defect Accumulation in Subsequent Wire Array Generations

Defects, defined as a Si wire missing from the pattern, were evaluated using imaging software surveys of top-down SEM views of the wire arrays. Because every defect in the surface pattern was transferred to succeeding generations, the success of subsequent growths depended directly on the quality of the initial array. The oxide template served the crucial role of preserving the pattern fidelity by preventing the catalyst metal from migrating across the wafer surface during the growth reaction.¹¹⁹ Second-generation wire arrays were nearly defect-free (Figure 4.6f). However, damage to the oxide pattern, caused by the formation of HCl in the reactor,¹⁰⁶ and undercutting during the KOH etch, was observed to introduce defects in the wire array. The accumulation of defects became more prominent, although still fairly modest, in third- and fourth-generation arrays (Figure 4.7 and Table 4.1). In the fourth-generation arrays, the number of defects approached 10% of the initial wire density. With optimization of the reaction process, it is likely that the density of defects could be reduced, so that several more generations of useful wire arrays could be produced with the same oxide pattern. The use of ethylenediamine pyrocatechol instead of KOH ought to further improve the selectivity of etching Si relative to SiO₂.¹³³

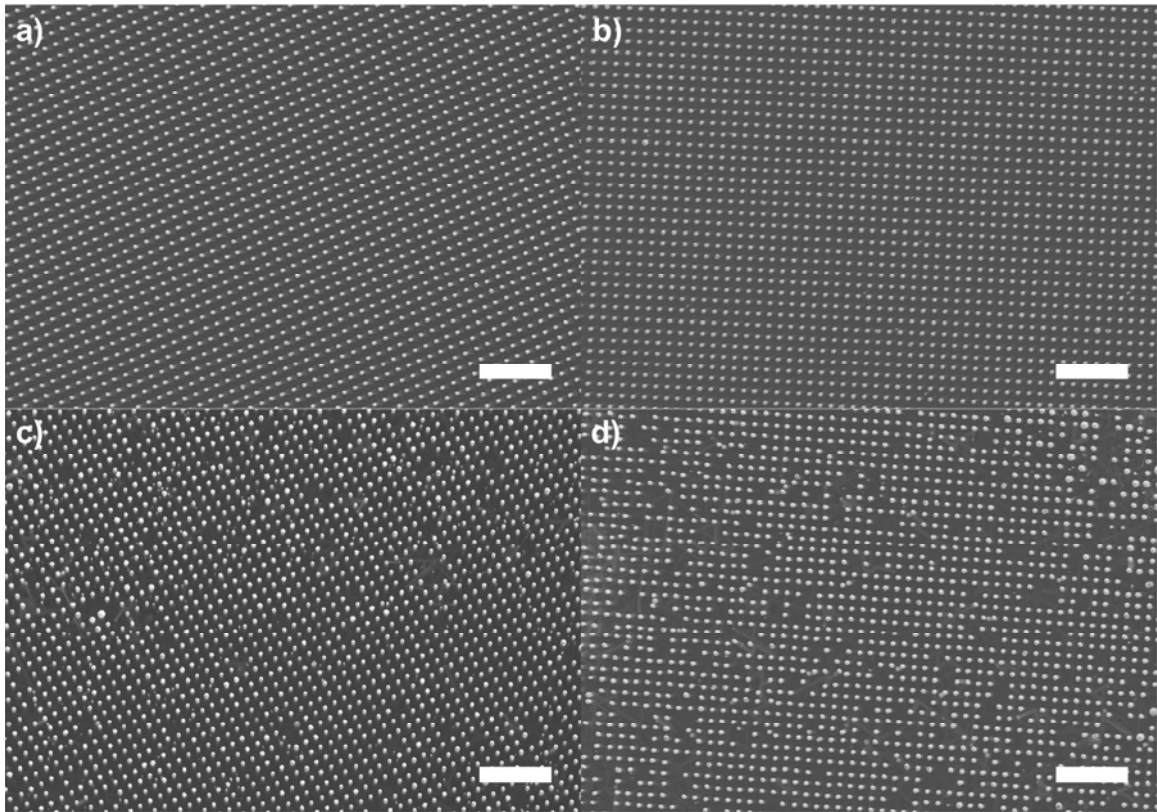


Figure 4.7. Accumulation of defects in succeeding wire array generations. Top-down SEM images for (a) first, (b) second, (c) third, and (d) fourth generation Si wire arrays, showing increasing defect density with successive generations of wire growth using a single oxide pattern on the substrate. The scale bar in each image is 40 μm .

Table 4.1. Average defect density within each generation of arrays.^a

Wire Array Generation	Defect Density (cm^{-2})	Defect Percentage (%)
First	$(7.5 \pm 5.0) \times 10^2$	0.04 ± 0.02
Second	$(2.5 \pm 1.1) \times 10^4$	1.2 ± 0.5
Third	$(1.4 \pm 0.7) \times 10^5$	6.6 ± 3.4
Fourth	$(2.2 \pm 0.8) \times 10^5$	10.0 ± 3.4

^a The data were collected using five top-down view SEM images of each generation. The averages were weighted by the area surveyed within each image.

4.3.3 Closing the Reuse Cycle by Growth of a New Thermal Oxide

Wire regrowth on a single Si(111) substrate was further extended by subjecting cycled wafers to mechanical polishing, which reduced their thickness by 10 to 20 μm , followed by thermal oxidation. To simulate rapid and inexpensive processing, the wafers were intentionally polished in a cursory manner. Because restoration of the patterned oxide overlayer required oxidation and then etching of the Si wafer, some degree of surface roughness should be tolerable. The polished Si wafers were thermally oxidized in a tube furnace under a fully hydrated atmosphere of industrial grade air at 900 $^{\circ}\text{C}$ for 8 h, resulting in a 300 – 400 nm thick surface oxide. Even with an imperfect starting surface, VLS-catalyzed wire growth yielded a vertically aligned Si wire array of comparable quality to that of the first-generation Si wire array (Figure 4.8). Furthermore, the use of a more precise industrial polishing technique such as chemomechanical polishing⁹⁶ or electropolishing¹³⁴ should significantly reduce the amount of silicon lost in this process step.

Even without further improvements, if four generations of arrays can be grown from each oxide template and only 10 μm of wafer thickness is lost in each polishing step, a single 400 μm thick wafer would be capable of producing 160 Si wire arrays (fewer, if the wafer thinness limits its manipulation). Reasonable expectations for optimization (i.e., five generations per oxide layer, and 2 μm of Si removed per polishing step) imply that the same thickness of Si substrate should be capable of producing 1000 or more Si wire arrays. Furthermore, the VLS growth catalyst can be replaced by Ni or Cu to produce Si wire arrays of nominally equivalent structure¹¹⁹ that ought to have superior electronic properties relative to those produced from the deep-trap Au VLS catalyst.

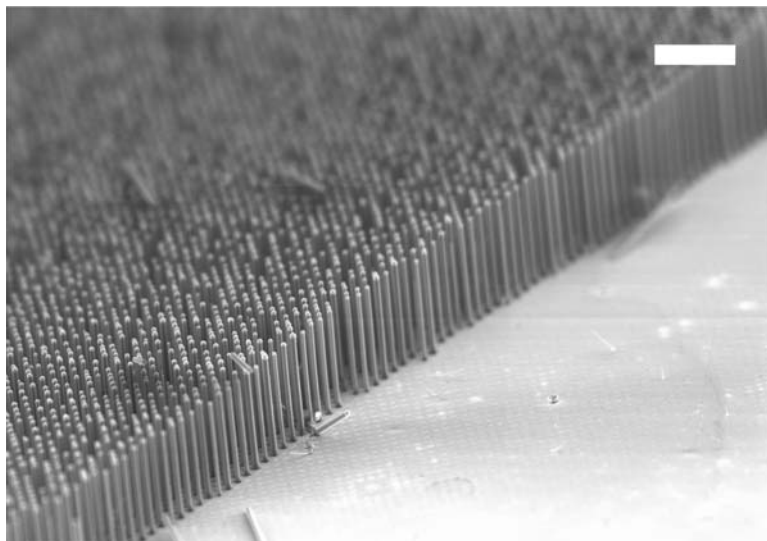


Figure 4.8. Growth after formation of a new thermal oxide layer. Tilted-view SEM image of a Si wire array grown from a Si(111) wafer that had been mechanically polished and then thermally oxidized. The scale bar is 40 μm .

4.4 Conclusion

The ability to transfer single-crystal wires in highly structured arrays to polymer films and recycle the growth substrate repeatedly is significant for minimizing the expense of high-quality Si wire array fabrication. Given the proven low cost of chlorosilane-based CVD processes,^{135, 136} the approach described herein has the potential to afford a scalably manufacturable method for the production of large areas of oriented, patterned Si wire arrays for use in solar cells, batteries, photonics, and a variety of other applications. With our technique, solar cell absorber materials with the potential to achieve high efficiency can now be prepared by high-temperature processing and then transformed into a flexible,

processable form. New avenues of research into the optical, chemical, and mechanical properties of these composites are now available. Increases in the light absorption of the film can be pursued by shrinking the polymer matrix to increase the packing density of the wires beyond the templated epitaxial growth limits. The availability of large area, freestanding Si wire array films enables the optoelectronic and electrochemical properties of VLS-grown wire arrays and the substrate to be deconvoluted. Ultimately, we envision the inclusion of such wire array structures in a variety of electronic and photonic applications, in which ordered, extended three-dimensional structures of nanoscale devices are desired on the macroscale.