Wire Array Solar Cells:

Fabrication and Photoelectrochemical Studies

Thesis by

Joshua Michael Spurgeon

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Abstract

Despite demand for clean energy to reduce our addiction to fossil fuels, the price of these technologies relative to oil and coal has prevented their widespread implementation. Solar energy has enormous potential as a carbon-free resource but is several times the cost of coal-produced electricity, largely because photovoltaics of practical efficiency require high-quality, pure semiconductor materials. To produce current in a planar junction solar cell, an electron or hole generated deep within the material must travel all the way to the junction without recombining. Radial junction, wire array solar cells, however, have the potential to decouple the directions of light absorption and charge-carrier collection so that a semiconductor with a minority-carrier diffusion length shorter than its absorption depth (i.e., a lower quality, potentially cheaper material) can effectively produce current. The axial dimension of the wires is long enough for sufficient optical absorption while the charge-carriers are collected along the shorter radial dimension in a massively parallel array. This thesis explores the wire array solar cell design by developing potentially low-cost fabrication methods and investigating the energy-conversion properties of the arrays in photoelectrochemical cells.

The concept was initially investigated with Cd(Se, Te) rod arrays; however, Si was the primary focus of wire array research because its semiconductor properties make low-quality Si an ideal candidate for improvement in a radial geometry. Fabrication routes for Si wire arrays were explored, including the vapor-liquid-solid growth of wires using $SiCl_4$. Uniform, vertically aligned Si wires were demonstrated in a process that permits control of the wire radius, length, and spacing. A technique was developed to transfer

these wire arrays into a low-cost, flexible polymer film, and grow multiple subsequent arrays using a single Si(111) substrate. Photoelectrochemical measurements on Si wire array/polymer composite films showed that their energy-conversion properties were comparable to those of an array attached to the growth substrate. High quantum efficiencies were observed relative to the packing density of the wires, particularly with illumination at high angles of incidence. The results indicate that an inexpensive, solid-state Si wire array solar cell is possible, and a plan is presented to develop one.

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Portions of this thesis have been drawn from the following publications:

Spurgeon, J. M., Boettcher, S. W., Kelzenberg, M. D., Brunschwig, B. S., Atwater, H. A., and Lewis, N. S., Photoelectrodes from arrays of crystalline Si wires embedded in a flexible polymer. Submitted, (2009).

Plass, K. E., Filler, M. A., Spurgeon, J. M., Kayes, B. M., Maldonado, S., Brunschwig, B. S., Atwater, H. A. and Lewis, N. S., Flexible polymer-embedded Si wire arrays. *Adv. Mater.* **21**, 3, 325-328 (2009).

Spurgeon, J. M., Plass, K. E., Kayes, B. M., Brunschwig, B. S., Atwater, H. A. and Lewis, N. S., Repeated epitaxial growth and transfer of arrays of patterned, vertically aligned, crystalline Si wires from a single Si(111) substrate. *Appl. Phys. Lett.* **93**, 3, 032112-1-3 (2008).

Spurgeon, J. M., Atwater, H. A. and Lewis, N. S., A comparison between the behavior of nanorod array and planar Cd(Se, Te) photoelectrodes. *J. Phys. Chem. C* **112**, 15, 6186-6193 (2008).

Chapter 1

Introduction

1.1 Energy and Climate Change

The modern world, with its lighted cities, heated homes, millions of cars, trucks, boats, planes, and even Ipods and cell phones, uses far more energy per capita than the world of our ancestors. It is difficult to fathom the magnitude of energy that we, as a planet, are consuming all the time. In 2006, our global civilization consumed 472.3 quadrillion (10^{15}) BTUs,[1] which converts to an average power of 15.8 Terawatts (TW), or 15.8 x 10^{12} W. With our current global population of approximately 6.5 billion people, that is 2,430 W each, equivalent to constantly running about 40 incandescent, 60 W light bulbs for every single person on the planet. Of course, the per capita consumption is far higher in the developed world, with the typical U. S. consumer using more than 4 times the global average. However, as the rest of the world continues to develop, the per capita consumption will climb even higher.

The energy needs of the planet are projected to continue growing in the foreseeable future, largely due to population growth and the rapid economic development of countries such as China and India. The Energy Information Administration (EIA) of the U. S. Department of Energy predicts that the mean global energy consumption will rise

44% from its 2006 value to an average rate of 22.7 TW by 2030 (Figure 1.1).[2] These numbers are a cause for alarm, not only because it will be a challenge to supply energy on this scale, but because the large majority of our energy (~ 86%)[1] is currently generated by burning fossil fuels (Figure 1.2). In addition to questions about the long-term sustainability of this dependence on non-renewable fuels, there are serious concerns about the consequences of the combustion of so much carbon.

The burning of fossil fuels creates CO_2, a known greenhouse gas that contributes to the phenomenon of global warming. While there is still ongoing debate in the media about the validity and consequences of the global warming theory, the scientific community as a whole is largely in agreement that it is real and happening. This is strongly supported by the Intergovernmental Panel on Climate Change's Fourth Assessment Report released in 2007.[3] The clearest evidence that the planet is warming includes global temperature data and worldwide observations of the shrinking of sea ice, the retreating of glaciers, the rising of ocean levels, the bleaching of coral reefs, and the increases in strong storms and floods. On its present course, unabated climate change could have severely adverse effects on ecosystems, submerge coastal cities through sea level rise, and lead to more water shortages and droughts.

There are reasons beyond the threat of climate change to strive for energy production that is less reliant on fossil fuels. Burning coal and petroleum releases gases into the atmosphere that cause pollution and lead to smog and acid rain. Mining and drilling for fossil fuels can devastate the local environment, and oil spills can cause harm to ecosystems from which they can take decades to recover. A dependence on fossil fuels

also causes many nations to be dependent on others that are rich in these natural resources, resulting in geopolitical tensions. Lastly, a growing demand for a dwindling supply of resources is clearly an unsustainable energy plan for the long-term future. These issues, along with the grave and uncertain threat of climate change, are strong motivators to replace fossil fuels with carbon-free energy sources.

In the coming decades, carbon-free energy alternatives will need to be implemented on a massive scale to avert the climate change crisis by stabilizing CO_2 levels at reasonable target values. The technical analyses of Hoffert et al. indicate that 10 – 30 TW of carbon-free primary power technology will need to be in place by 2050 to meet modest CO_2 stabilization goals.[4, 5] Thus, the majority or even the entirety of our global energy consumption will need to be supplied by the middle of this century by sources that do not emit carbon. While they are worth exploring to help ease this transition, the concepts of "clean" coal and carbon sequestration are unlikely to be able to meet this challenge in a sustainable fashion.[6-9] Nuclear fission technology is well-established and has the potential to play a partial role in meeting the "terawatt challenge." However, in addition to serious concerns about nuclear waste, nuclear weapons proliferation, long plant start-up times, and a strong "not-in-my-backyard" sentiment among the general public, energy from fission may be limited on this scale by the abundance of suitable nuclear fuel.[6, 10, 11] Nuclear fusion is a promising long-term carbon-free power source, but it has enormous technical challenges to overcome. Researchers have yet to demonstrate a fusion reactor that generates more energy output than its required energy input, and advancing the technology requires decades-long, exorbitantly expensive, multinational projects such as the International Thermonuclear Experimental Reactor

(ITER).[12] Nuclear fusion is therefore extremely unlikely to provide a significant fraction of the world's energy needs by the middle of this century.[11] To implement at least 10 TW of carbon-free energy by 2050, we will need to turn to renewable energy sources.

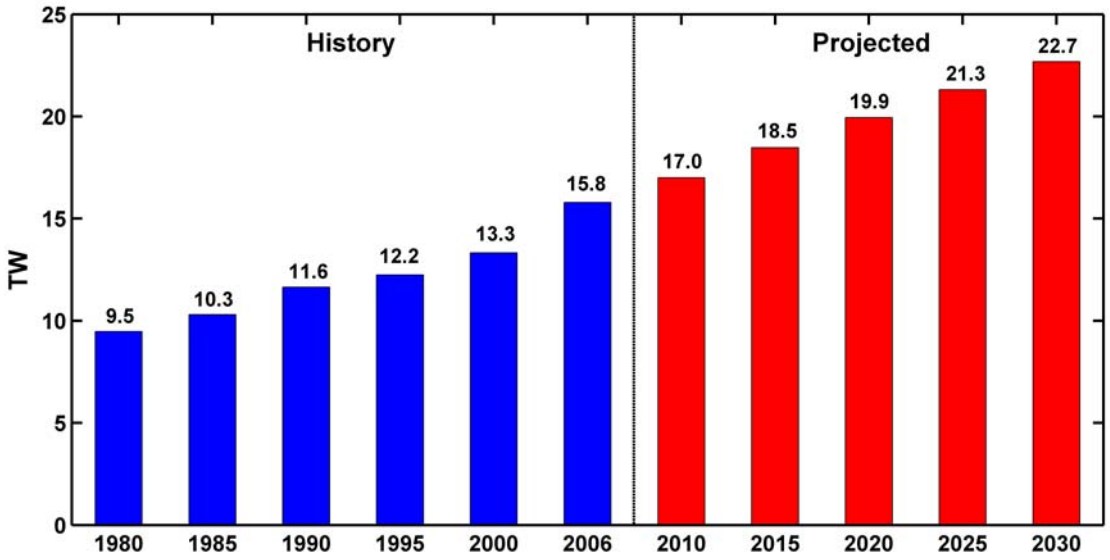

Figure 1.1. Mean global energy consumption, 1980 – 2030. Total average annual energy used by humankind, in TW (10^{12} W). Historical data for the recent past is displayed in blue, and projections up to the year 2030 are shown in red. Projections are based on the EIA's International Energy Outlook 2009.[2]

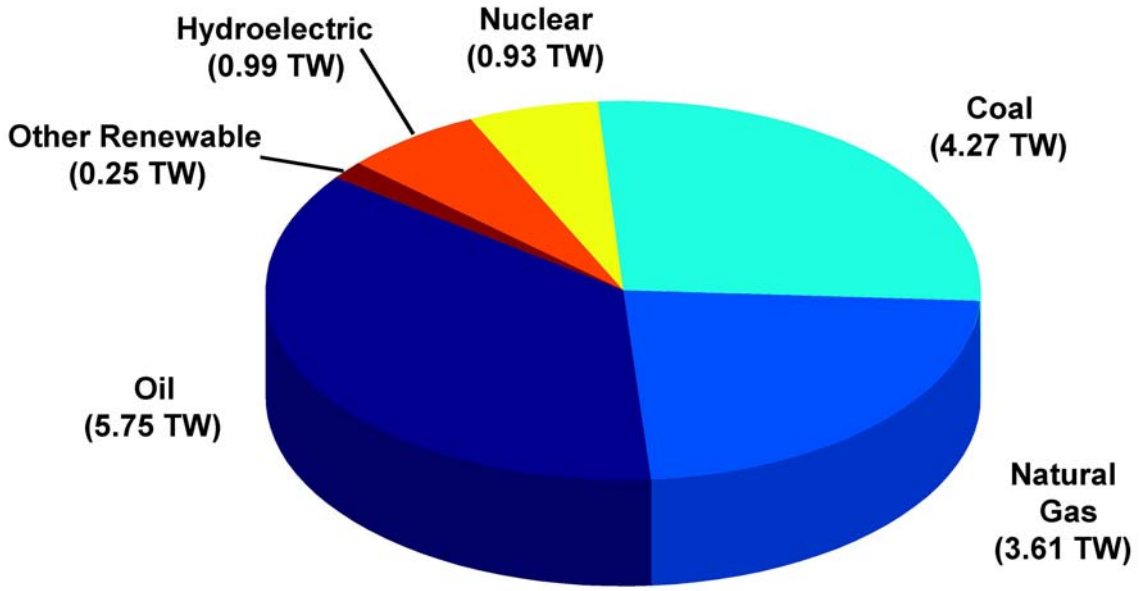

Figure 1.2. Mean global energy consumption by source, 2006. A breakdown, in TW (10^{12} W), of how humankind generated the energy it consumed in 2006. "Other Renewable" includes geothermal, solar, wind, and wood and waste. The total average power used by the world in 2006 was 15.8 TW, with ~ 86% generated by the combustion of fossil fuels. Numbers are converted from data provided by the EIA.[1]

1.2 Renewable Energy Options

Mankind has developed a number of ways to harness energy from the ongoing natural processes of our environment. These renewable sources include hydroelectricity, biomass, wind, geothermal, ocean, and solar energy. Together these resources provide a hope of meeting the terawatt challenge with carbon-free or carbon-neutral primary energy sources.

A comparison between the practical potential for power generation between these resources highlights which can be key technologies for meeting the world's future energy

needs (Figure 1.3).[13, 14] Hydroelectricity is by far the most commonly used renewable energy for electricity generation at present. The World Energy Assessment concludes that there is technical potential for ~ 1.6 TW of hydroelectricity, which does not impose restrictions for economic or environmental considerations.[13] As such, it is an overestimate of the practical limit. Considering that 0.99 TW of hydroelectricity was consumed in 2006 (Figure 1.2),[1] there is little room for this industry to contribute more towards the 10 TW carbon-free energy goal. Biomass for electricity generation and transportation fuel can be produced carbon-neutrally, but the low power density of photosynthesis (~ 0.6 W m^{-2}) is a limitation. More than 10% of the Earth's land surface, an area approximately equivalent to all agricultural land, would be needed to get 10 TW from biomass.[6] This would create competition for water supplies, drive up global food prices, and contribute to deforestation and habitat destruction. An optimistic estimate for the potential power generation of biomass is 7 TW.[14] There is theoretically potential for 50 TW of wind energy if the entire suitable land area of the Earth were used. However, a more reasonable limit of 4% land area utilization gives a practical potential of 2 TW of wind power.[13] Geothermal energy has enormous potential but is widely dispersed, and the technological ability to utilize it, rather than its available quantity, will determine how much it can contribute. One estimation for the total continental geothermal energy potential is 11.6 TW.[14] There is also a great deal of energy theoretically available from the ocean in the form of tides, waves, ocean thermal, and salt gradient energy. However, these energy resources are very diffuse and therefore difficult to collect, and the technology for harvesting energy from the ocean is not considered mature enough yet for commercialization.[13]

The most abundant renewable resource by far is supplied by the sun. There is an average 1.2 x 10^5 TW of solar energy striking the surface of the Earth,[11, 13, 14] which means that in only 69 min, the sun hits our planet with enough energy to run human society at our 2006 rate (15.8 TW) for an entire year. With the conservative restrictions of a 10% conversion efficiency and land-based sites only, there is a practical potential for 60 TW of solar energy.[13, 14] This is nearly four times the 2006 global energy consumption and represents a greater practical potential than the combination of hydroelectricity, biomass, wind, and geothermal energy (Figure 1.3). Our current energy needs could be met by covering just 0.1% of the Earth's surface with 10% efficient photovoltaics. Although there are issues with the solar resource, such as its regional variance and intermittency due to time, season, and weather conditions, its vast abundance in comparison to the other renewable options makes it clear that solar will need to play a leading role in the global energy portfolio to produce > 10 TW of carbon-free primary energy by 2050.

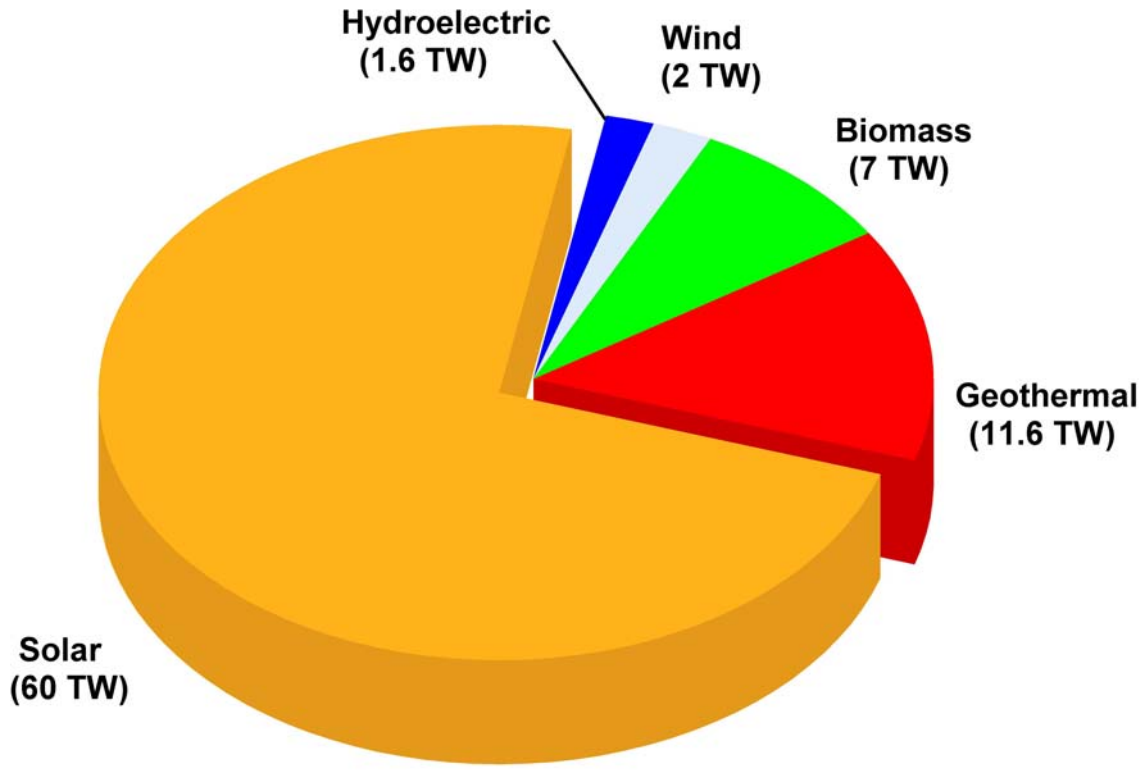

Figure 1.3. Global practical potential of renewable resources. Estimates of the technical, annual average power, in TW, available from various terrestrial renewable energy sources.[13, 14] The solar energy number assumes 10% energy conversion efficiency.

1.3 Cost of Photovoltaics

Considering the enormous abundance of the solar resource, why are we not using solar energy on a massive scale already? Sunlight falls freely on everyone, and the photovoltaic concept has been around for a long time. Becquerel discovered the photovoltaic effect in 1839,[15] and in the 170 years since that time it has only grown to comprise ~ 0.1% (or 16 GW) of the global energy consumption.[16]

Economics is the main factor limiting the implementation of photovoltaics (PV). The core problem is that solar cells cannot yet provide electricity to the consumer as cheaply as fossil fuels can. The production cost of solar photovoltaics at present is US$ 0.25 – 0.30 per kWh, compared to US$ ~ 0.03 – 0.05 per kWh for fossil fuel based utility-scale electrical power generation.[17-19] Although government subsidies and cost savings from scaling up can help this price comparison, changes in photovoltaic manufacturing are needed to drive the cost per kWh down so that it can be competitive with existing utilities.

With approximately 90% of the market share,[19-22] crystalline and polycrystalline silicon solar cells set the benchmark for photovoltaic prices. Estimates for the least expensive current retail module prices are ~ US$ 3 per peak watt (W_p), with average retail module prices closer to US$ 4.50/W_p.[20, 23] Although estimates vary substantially,[20, 24] one breakdown of the production of multicrystalline silicon solar module costs assigns 48% of the cost to materials, 13% to cell processing, 9% to module assembly, and 30% to the "balance of systems" (Figure 1.4).[22] Within the materials category, the feedstock costs refer to the expense of electronic grade polysilicon used for crystal growth, which itself is typically produced by purifying silicon dioxides (sand) to metallurgical grade silicon which is then further purified by the Siemens process to electronic grade. In this process, for each mole of Si converted to electronic grade polysilicon, 3 – 4 moles are converted to the byproduct $SiCl_4$.[25] The ingot growth expenses involve polysilicon sorting and etching, crystallization, and ingot shaping and sizing.[24] The crystallization step, through a process such as the Czochralski growth technique or block-casting, is expensive because it is energy intensive, must strictly exclude impurities, and sacrifices a large crucible for each ingot produced.[21] Wafering refers to the costs associated with

cutting the Si boules into wafers and then cleaning and polishing them. The cutting process is particularly expensive because it uses wire saws to slice the boule, with each wire consuming ~ 180 μm of silicon lost as waste and requiring the etching of another 25 μm to remove the damaged surface.[24] In all, the wire sawing process wastes up to 35% of the material as "kerf losses."[21] The cell processing costs include chemical etches, diffusion doping, antireflection coating, front and rear contact printing, and cell testing.[24] Module assembly involves connecting the cells together reliably in a circuit, encapsulation of the cells, framing the unit, and testing the module.[20, 24] The balance of systems refers to the inverter, grid connection, and installation fee that are necessary for a fully installed system.

Although photovoltaic electricity costs have been gradually declining (from over US$ 60/W_p in 1976 to ~ US$ 4/W_p in 2009), significant changes will be needed to continue the cost curve to the target US$ 1/W_p that is required to achieve grid parity so that PV can compete with large-scale utilities.[23, 26, 27] Because materials expenses are approximately half of the cost of a solar module, the ability to make solar cells out of much cheaper materials with fewer purification and wafering requirements would subtract substantially from the final price of photovoltaic electricity. Several thin film solar technologies, such as amorphous Si, CdTe, and $CuInSe_2$, are striving for this goal but have not reached it yet.[21] While promising, these technologies have had limitations including low module efficiency, toxicity, and materials scarcity issues.

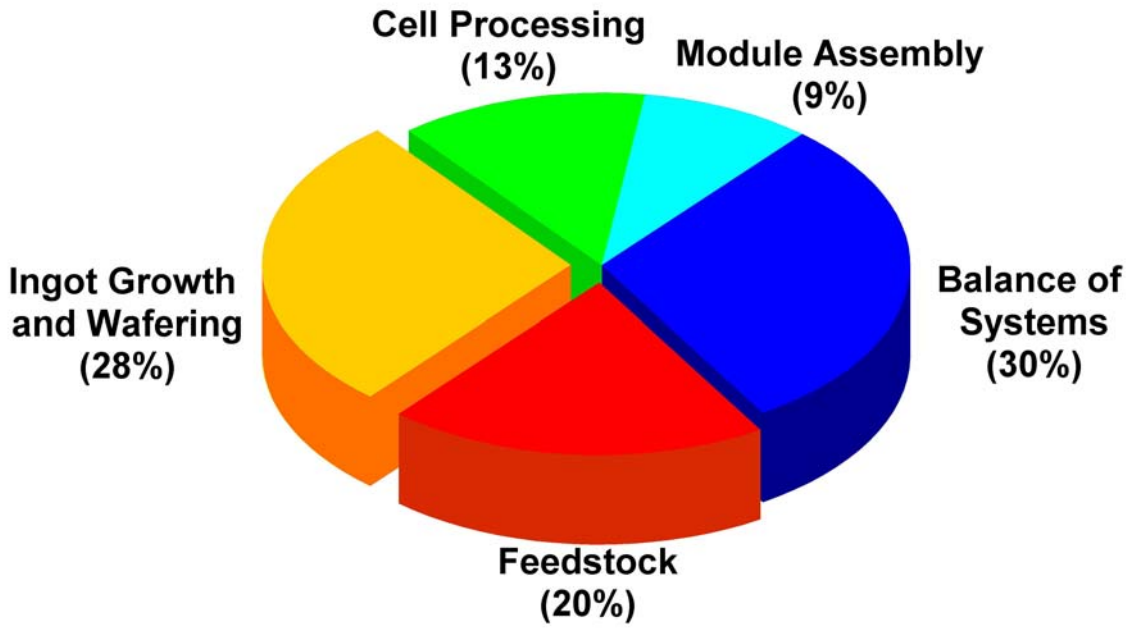

Figure 1.4. Cost breakdown of crystalline silicon solar PV modules. Percentages of the total module cost attributed to specific manufacturing processes.[22] Feedstock, ingot growth, and wafering together constitute the materials cost and total 48%.

1.4 The Radial Junction Concept

Solar cell materials are costly because they must be able to satisfy the physics necessary to produce photovoltaic electricity. In a cell, a photon of sufficient energy will create an electron-hole pair that is then separated by a built-in electric field near the junction.[28, 29] The charge-carriers that are effectively separated through the junction are collected and sent to the front and back contacts as useful electric current. The minority-carriers (holes for n-type, electrons for p-type) move across the junction, and must therefore be able to diffuse from the point of their generation to within the electric field without recombining in order to produce current.

Solar-quality semiconductor materials are expensive to manufacture primarily because they must be both pure and highly crystalline to minimize the recombination of photogenerated electron-hole pairs. Impurities and grain boundaries act as trap centers where charge-carriers can wait until encountering a carrier of opposite sign, recombining and wasting the energy as heat rather than current. Inexpensive semiconductor materials that are candidates for solar cells generally have a high impurity level and/or defect density, which causes them to have a low minority-carrier diffusion length (L_n for p-type, L_p for n-type).[30]

In a traditional, planar junction solar cell, $L_{n/p}$ must be greater than the optical absorption depth in order to efficiently collect the photogenerated charge-carriers (Figure 1.5). If $L_{n/p} < 1/\alpha$ (an average "optical thickness," related to the absorption constant $\alpha(\lambda)$ integrated over all wavelengths λ), the solar cell will be carrier-collection limited in the base region. Also, the thickness of the cell, L, must be $> 1/\alpha$ to absorb most of the incident light. Defining $1/\alpha$ to be the thickness of material required to absorb 90% of the incoming photons, Si has an optical thickness of ~ 125 μm. Thus efficient, planar junction Si solar cells must have both L and $L_{n/p} > 125$ μm. The same reasoning applies for other semiconductors and sets the lower limit for an acceptable minority-carrier diffusion length in an efficient solar cell. The effective optical thickness, and therefore the necessary L and $L_{n/p}$, can be lowered by using light-trapping techniques (i.e., antireflection coatings, back side reflectors, etc.). However, considering the limitations of the ability of light-trapping to decrease the required thickness,[31, 32] materials with minority-carrier diffusion lengths significantly less than their optical thicknesses cannot be made into high efficiency planar junction solar cells.

By switching to a different cell geometry, however, it may be possible to avoid this restriction. An answer might be found in redesigning the junction architecture to promote the separation of photon absorption and charge-carrier collection into orthogonal spatial directions. Using an array of high aspect-ratio cylindrical pillars with radial junctions, optimal light absorption could occur along the lengthier axial dimension, while charge-carrier extraction would take place over the much shorter radial dimension (Figure 1.6). This structure makes it possible to separately optimize the design for both ideal optical absorption and carrier collection by tuning the wire length and diameter independently. If inexpensive, low-diffusion-length semiconductor materials can be fabricated as a wire array structure in a cost-effective process, they could potentially produce efficient solar cells much more cheaply than the high-diffusion-length planar alternatives.

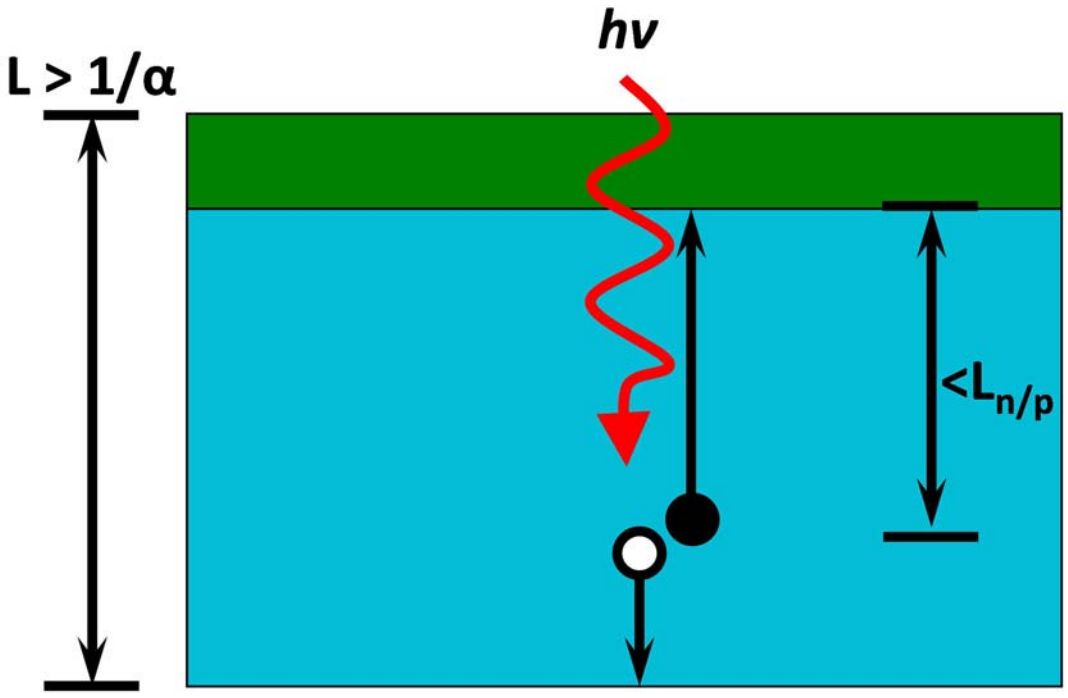

Figure 1.5. Planar junction solar cell architecture. The semiconductor slab thickness, L, must be greater than the optical thickness, 1/α, to absorb most of the light. The minority-carrier diffusion length, $L_{n/p}$ (L_n for p-type, L_p for n-type), must also be greater than 1/α or the device will be carrier-collection limited toward the base of the cell.

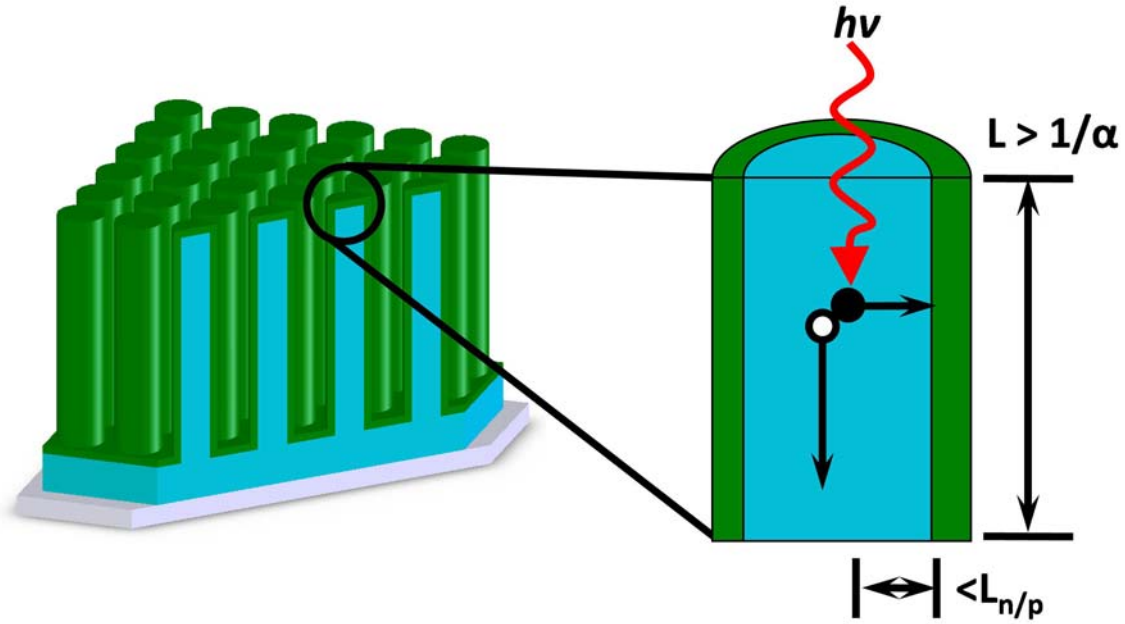

Figure 1.6. Radial junction solar cell architecture. The idealized radial junction cell consists of a densely packed array of wires of uniform dimension (image credit: M.D. Kelzenberg). The semiconductor wire length, L, should be greater than the optical thickness, $1/\alpha$, to absorb most of the light, but the minority-carrier diffusion length, $L_{n/p}$ (L_n for p-type, L_p for n-type), need only be comparable to the wire radius for the device to collect most of its photogenerated charge-carriers.

1.5 Modeling of a Radial Junction

At the outset of this project, a theoretical study was conducted by Kayes et al. to model the behavior of an inorganic radial p-n junction solar cell and compare it to a planar cell.[33] The model assumed an abrupt junction with the depletion layer approximation, included the effects of surface recombination and Shockley-Read-Hall recombination from a single-trap level at midgap, used only light normally incident on the top face of the semiconductor rod, and took carrier transport to be purely radial. A single cylinder with a radial junction was investigated, so that the model neglected the complicated

optical effects that would result from light passing through arrays of wires of varying packing density and arrangement. The simulation used both Si and GaAs rods. The key findings of the study were that optimal cells had a radius approximately equal to the minority-carrier diffusion length in the core of the rod, doping levels must be high enough that such short radii rods are not fully depleted, the short-circuit current (J_{sc}) was basically independent of radius if the radius was less than the diffusion length, open-circuit voltage (V_{oc}) decreased with decreasing rod radius, and an increasing depletion-region trap density profoundly decreased the (V_{oc}) at diffusion lengths less than ~ 5 μm. The study concluded that radial junctions offered large gains in efficiency over planar junctions if the material was carrier-collection limited in planar form and if the depletion-region recombination rate was relatively low. With higher depletion-region recombination, only modest efficiency gains were possible. For Si, regardless of depletion-region trap density, efficiencies of ~ 15% were predicted with minority-carrier diffusion lengths of 5 – 10 μm, several percent better than the planar equivalent.

This work was eventually followed by additional modeling by Kelzenberg et al. with the benefit of minority-carrier diffusion length estimates for Si wires grown by a chemical vapor deposition method.[34] This model employed the Sentaurus Device simulator software, which simultaneously solves the electron and hole continuity equations and the Poisson equation within the device. A Si p-n junction on a single wire was modeled with most of the same assumptions used in Kayes' work, with the notable exception that carrier transport was allowed to occur in both the axial and radial directions. All the same general trends were confirmed, although this work concludes that a radius equal to half the minority-carrier diffusion length is optimal. Simulated

current-voltage curves based on an experimentally measured diffusion length of 10 μm led to a wire cell efficiency of 17%, compared to 13% for a planar cell.

1.6 Routes to Wire Array Fabrication

While it will be critical to produce wire array cells that perform as well in experiment as they do in theory, it is equally essential that they be fabricated with a cost-effective method that reduces the materials and processing costs of solar cell manufacturing. If wire array fabrication is as expensive as the production of pure, crystalline planar materials, there is little reason to pursue this technology. Fortunately, a number of approaches have been developed to promote the one-dimensional growth of materials, several of which hold promise as potentially inexpensive routes to manufacture wire arrays.[35-37]

Perhaps the cheapest method is the utilization of solution-based chemistry to induce one-dimensional growth. One possible way to do this is to introduce capping agents that change the free energy of different crystal planes and favor one plane in particular.[35] With this approach, colloids in solution have been grown into nanowires and tetrapod structures.[38] Through the control of interfacial surface tension and a thermodynamic understanding of the nucleation and growth, metal oxide materials can be "purpose-built" from solution into nanowire array structures.[39, 40] Another inexpensive, scalable technique is to use nanocrystals dispersed on a substrate in a hydrothermal solution process to seed the growth of nanowires. This method has been demonstrated to

efficiently produce large-area arrays of dense ZnO wires.[41] In general, solution-based wire growth methods are limited in their application for solar cell fabrication by either the disassembled, substrate-free nature of the wires produced or by the restricted types of semiconductors that can be shaped with a particular technique.

Physical or chemical vapor deposition techniques can produce semiconductor wire arrays as well. The most widely used approach, the vapor-liquid-solid (VLS) mechanism, uses a solid catalyst droplet that liquefies upon absorption of a vaporous species until it becomes supersaturated and deposits a solid wire by growth in a particular crystal direction (see Section 3.3.2).[42] The VLS mechanism can produce aligned, highly crystalline wire arrays of a range of semiconductors, but uses potentially expensive gas phase precursors, catalysts, and substrates. The possible need for high growth temperatures and low pressures can also add to the expense of wire growth with this approach.

A straightforward route to the production of one-dimensional structures of practically any material is to use template-directed synthesis.[35] In this method, the material is deposited within the template so that its morphology is shaped by the scaffold surrounding it. The template is usually sacrificial and can be removed by a chemical etch after nanowire deposition. Research groups have demonstrated templates through the use of porous materials, biological macromolecules, surfactants, block copolymers, and nanostructures produced by another method. Porous anodic aluminum oxide membranes are particularly common templates for nanowire synthesis (see Section 2.1).[43, 44] The

drawbacks of this approach include the additional processing and complexity of using a template as well as the potential for surface contamination after template removal.

1.7 Previous Work Related to Wire Array Solar Cells

Ideas similar to the radial junction wire array solar cell have been investigated to test the concept of decoupling the directions of carrier collection and optical absorption. The first, the vertical multijunction solar cell, etched grooves into a planar base to form a vertical junction that increased the probability of minority-carriers reaching the collecting junction.[45] Later, a parallel multijunction solar cell was explored in which thin, horizontal, interpenetrating n- and p-type layers were alternately laid on top of each other.[46] While both of these designs were demonstrated with impressive efficiencies,[47, 48] research was eventually halted on them, likely because they were not cost-effective to produce. There was even one early published example of Si wires as photoconverters,[49] but it was a preliminary report and the serious study of wire array solar cells was not pursued.

Many of the fundamental properties of semiconductor nanowires are well established, however.[35, 36] The properties of single wires of semiconductors, including their carrier mobilities and lifetimes,[50] their resistivities,[51] methods to passivate their surfaces,[52] and their preparation as core-shell structures,[53] have been reported in detail. The photoluminescence,[54] reflectivity,[55] quantum-confinement effects,[56] and electrical properties[57] of arrays of semiconductor nanowires have been reported. However,

comparatively little work has been performed on the use of such nanowire arrays as absorber layers in solar cells. Nanowire arrays have been used in dye-sensitized solar cells.[58-60] In these studies, the presence of TiO_2[59] or ZnO[60] nanowires provides a direct path for dye-sensitized, injected majority-carriers to reach the back contact, instead of exploiting the nanowires for their ability to facilitate collection of minority-carriers in the radial direction. Improved minority-carrier collection has been demonstrated, however, in photoetching processes using porous electrodes. Vanmaekelbergh and Kelly observed improved photocurrent quantum efficiencies in their studies comparing planar and nanoporous photoelectrodes of SiC and GaP.[61, 62] Thus, the theory that a nanowire geometry can be effective in overcoming minority-carrier collection length limitations in a semiconducting absorber phase, as compared to the properties of that same material in a planar solar cell structure, remains of significant interest. The work presented herein continues in this context. The objective of this thesis was to develop cost-effective methods for the fabrication of semiconductor wire array solar cells and to test and improve their photovoltaic performance relative to analogous planar solar cells.

Chapter 2

A Comparison Between the Behavior of Nanorod Array and Planar Cd(Se, Te) Photoelectrodes[1]

2.1 Introduction

The II-VI semiconductors CdSe and CdTe are appropriate materials for testing the merits of the nanowire-based solar cell design. These II-VI compounds are both direct gap, highly absorbing materials having band gaps (1.7 eV for CdSe and 1.4 eV for CdTe) well-matched to the solar spectrum. Both materials can be deposited by a number of techniques.[63-65] Electrodeposition of CdTe and CdSe is well established,[66-73] and the photovoltaic or photoelectrochemical cell performance of the electrodeposited forms of these materials is usually limited by low minority-carrier diffusion lengths in the absorber material.[63, 74]

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[1] Reproduced with permission from Spurgeon, J. M., Atwater, H. A. and Lewis, N. S., *J. Phys. Chem. C* **112**, 15, 6186-6193 (2008). Copyright 2008 American Chemical Society.

When a deposition technique that does not induce one-dimensional growth is used, production of a nanorod array requires the use of a template.[35] Anodic aluminum oxide (AAO) templates have been demonstrated to facilitate the electrodeposition of arrays of II-VI semiconductor nanorods.[73, 75, 76] The pores in AAO templates are dense, relatively uniform in dimension, and highly vertically aligned (Figure 2.1). These pores can be fabricated with controllable pore aspect ratios, with pore diameters ranging from 5 nm to 200 nm, and with densities as high as 10^{11} pores cm^{-2}.[44, 77] AAO templates can be formed by anodization of Al under a bias of 10 – 100 V in an acidic solution of sulfuric acid, phosphoric acid, or oxalic acid,[78-81] or are commercially available. AAO membranes are particularly compatible with electrodeposition methods because the insulating nature of the alumina prevents material from depositing directly onto the template. After fabrication of the rods, the template can be selectively removed in an aqueous solution of sodium hydroxide, leaving behind a freestanding, vertically aligned semiconductor nanorod array.

Validation of the theoretical, radial junction nanorod predictions[33] requires a direct comparison between the performances of planar and nanorod array geometries in systems in which high-quality, conformal, rectifying contacts are made for each type of microstructure. The use of a liquid junction is advantageous for such situations. The chemistry involved with obtaining stable photoelectrochemical cells using CdSe or CdTe has been well developed.[82-87] Studies of the photoelectrochemistry of electrodeposited Cd(Se, Te) alloy layers are of particular relevance.[88] We describe herein photoelectrochemical studies of arrays of vertically aligned nanorods of Cd(Se, Te) in contact with rectifying, stable, liquid electrolytes, and compare the performance of such

electrodes to the behavior of photoelectrodes formed from analogous, planar Cd(Se, Te) materials. In addition, the spectral response of solid/liquid junctions with both planar and nanorod absorber microstructures has been obtained to elucidate the carrier collection properties as a function of the light absorption depth in the two different systems.

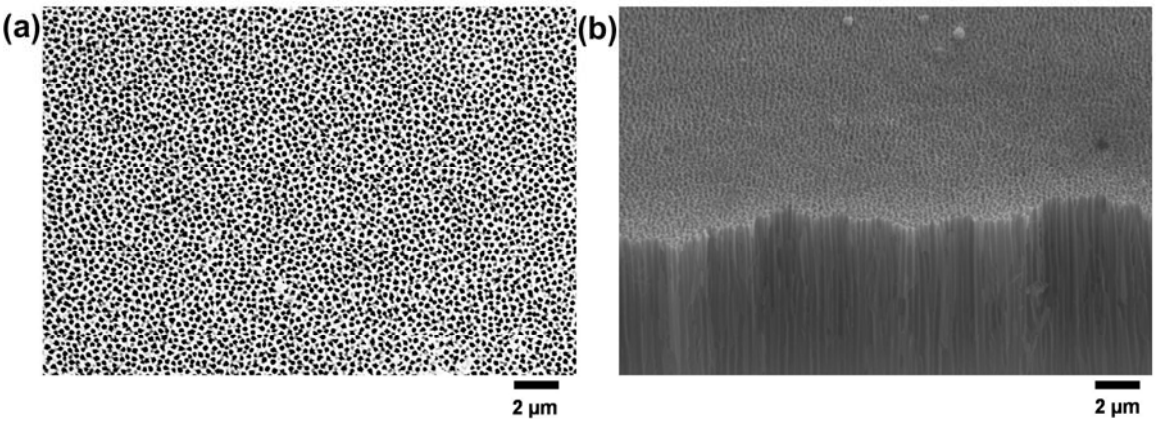

Figure 2.1. Anodic aluminum oxide (AAO) templates. (a) Top-down and **(b)** tilted cross-sectional view SEM images of 200 nm diameter pore AAO templates used to fabricate Cd(Se, Te) nanowire arrays.

2.2 Nanorod Array and Planar Electrodes

2.2.1 Electrode Fabrication

Nanorod array electrodes were fabricated using commercially available, 60 μm thick, 200 nm pore diameter, AAO membranes (Whatman Scientific) as templates. A 300 nm thick layer of CdSe was sputtered (RF magnetron sputterer, CdSe sputter target of 99.995% purity, Kurt J. Lesker Company) onto one side of the AAO to cover the bottoms of the pores. An ohmic back contact was then made by sputtering 1.5 μm of Ti (99.995% purity Ti sputter target, Kurt J. Lesker Company) onto the back of the CdSe layer. The other

side of the AAO was then covered in a layer of mounting wax to prevent deposition of metal onto the bottoms of the pores in subsequent processing steps. The template was made into a working electrode by attaching a Cu wire and applying conductive Ag paint around the edge of the membrane. The wire was encased in a glass tube, and the wire contact area was sealed with epoxy.

To provide mechanical stability and support for the nanorod array after the removal of the template, > 10 μm of Ni metal was electrodeposited onto the back of the Ti. The Ni substrate was galvanostatically electrodeposited at room temperature, under stirring, from an aqueous solution of 0.8 M nickel (II) sulfamate ($Ni(SO_3NH_2)_2$) and 0.6 M boric acid (H_3BO_3). In this process, a current density of 25 mA cm^{-2} was maintained for 1 hr between the working electrode and a Pt gauze counter electrode. The mounting wax was then thoroughly removed by several washes in acetone. $CdSe_{0.65}Te_{0.35}$ was electrodeposited into the pores using an aqueous deposition bath that contained 0.2 M $CdSO_4$, 20 mM SeO_2, and 10 mM TeO_2 in 1 M H_2SO_4. Triton X-100 was also added (0.25%) to reduce the surface tension and to improve the quality of the deposit. In addition to the Pt gauze counter, a saturated calomel electrode (SCE) reference was used with the AAO working electrode. The electrodeposition was performed potentiostatically at -650 mV versus SCE, at room temperature, without stirring, for 5 to 30 min.

After growth of the nanorods, the AAO template was removed by submersion of the electrode assembly for 20 min into 1 M NaOH(aq). The nanorod array was then thoroughly rinsed in 18 MΩ cm resistivity H_2O, dried, and detached from the Cu wire. The array was then annealed for ~ 90 min at 600 ^oC in an Ar atmosphere that contained a small percentage (~0.2%) of O_2. The nanorod array was then cut into smaller samples

(0.1 – 0.3 cm^2), and the samples were made into electrodes for use in photoelectrochemical cell measurements. Figure 2.2 provides a schematic summarizing the fabrication steps of the nanorod array photoelectrodes.

Planar Cd(Se, Te) electrodes were prepared in a nearly identical fashion. Ti foil (99.5% purity, 0.25 mm thickness) was cut into squares (0.2 – 0.4 cm^2), flattened, mechanically polished, and then made into electrodes in the same way as was done for the AAO templates. The Cd(Se, Te) layer was then electrodeposited exactly as it was for the nanorod arrays. After ~ 15 min of electrodeposition, the semiconductor deposit began to clump on the Ti substrate and easily fell off. The best-performing planar electrodes were therefore obtained by electrodeposition of the film until just before this phenomenon started. The planar electrodes were then annealed under exactly the same conditions as those used to make the nanowire array electrodes.

The morphology and dimensions of the planar and nanorod array electrodes were investigated using a LEO 1550 VP field-emission scanning electron microscope (FE-SEM). The microscope was equipped with an Oxford INCA Energy 300 X-ray energy-dispersive spectrometer (EDS) system that was used to measure the elemental composition of the samples.

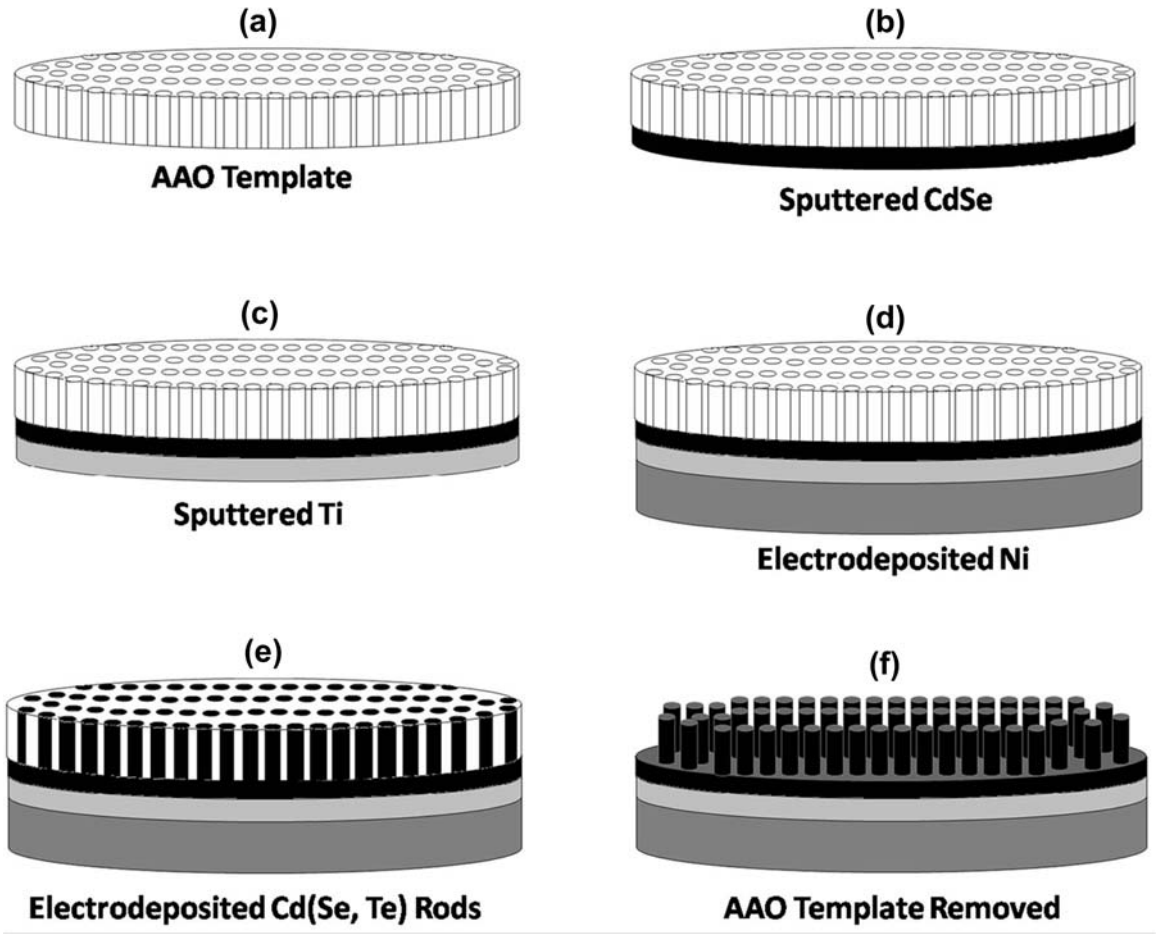

Figure 2.2. Schematic for the fabrication of nanorod array photoelectrodes. Starting with a commercially available **(a)** AAO template, a shunt-preventing layer was first applied by **(b)** sputtering a thin CdSe film on one side of the template, followed by **(c)** sputtering a Ti ohmic back contact layer. For structural stability, **(d)** Ni metal was electrodeposited on the back (note that to prevent growth of Ni inside the pores a wax layer was applied to the front of the template before electrodeposition and removed thoroughly with acetone afterwards). Nanorods were then grown by **(e)** electrodeposition of Cd(Se, Te) into the pores of the template (using wax on the back to prevent deposition in undesired areas). Finally, **(f)** the AAO template was removed with 1 M NaOH(aq), then rinsed, dried, annealed, and made into photoelectrodes.

2.2.2 Electrode Morphology and Composition

Figure 2.3 shows a cross-sectional SEM image of a Cd(Se, Te) nanorod array after the removal of the AAO template. The contrast in the substrate indicates the transition from the Ti ohmic back contact to the sputtered CdSe shunt-preventing layer. The Ni supporting layer is not visible in this image because the Ni separated from the Ti at the edges of the sample when the electrode was cut. EDS indicated that the elemental composition of the nanorods was Cd: Se: Te in the ratio 3: 2: 1, to within a few atomic percent.

Figure 2.4 displays top-view SEM images of planar and nanorod array electrodes. The planar sample exhibited an uneven morphology, as is typical of electrodeposited Cd(Se, Te) films that are not constrained within a template.[88] EDS results on the planar material indicated that the elemental composition was Cd: Se: Te in the ratio 3: 2: 1, to within a few atomic percent.

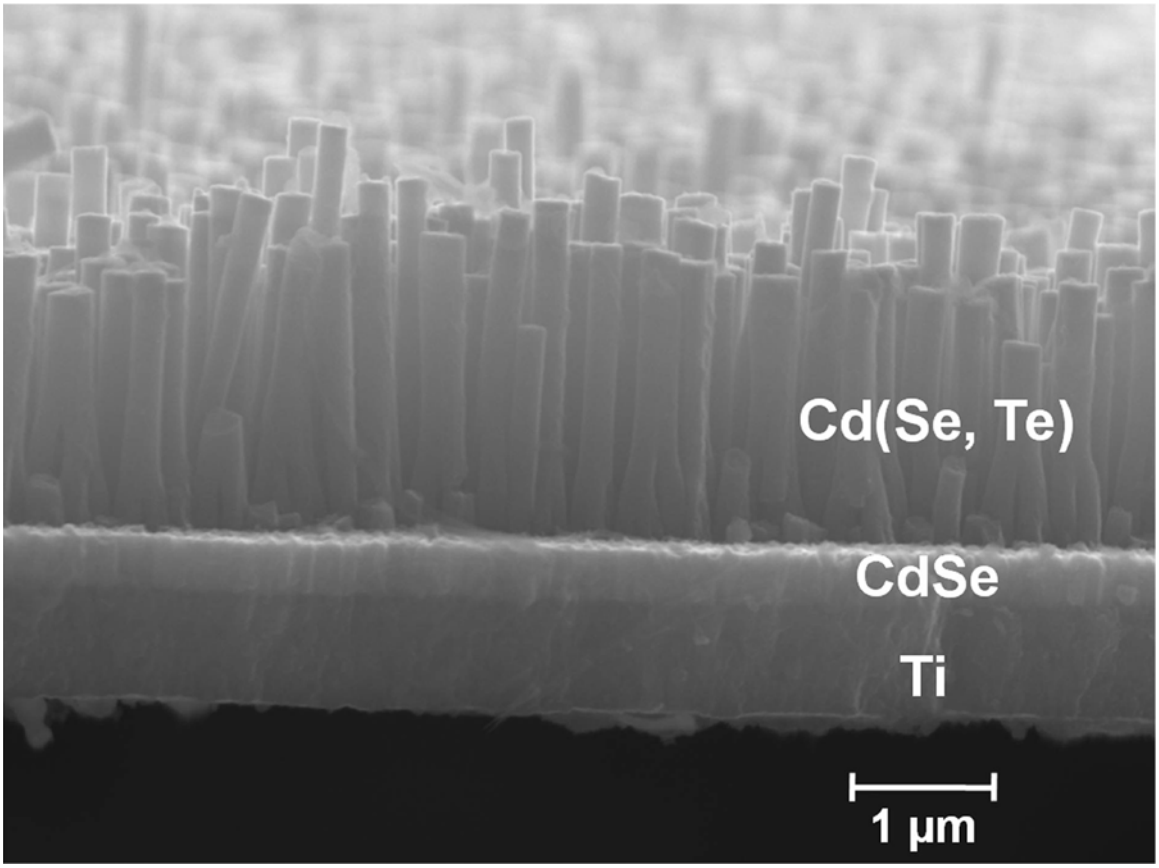

Figure 2.3. Nanorod array photoelectrode. SEM image (SE2 detector, 20 kV accelerating voltage) of a cross section of a Cd(Se, Te) nanorod array. The contrast in the substrate section indicates the shift from the Ti ohmic contact layer on the bottom to the sputtered CdSe shunt-preventing layer directly below the nanorods.

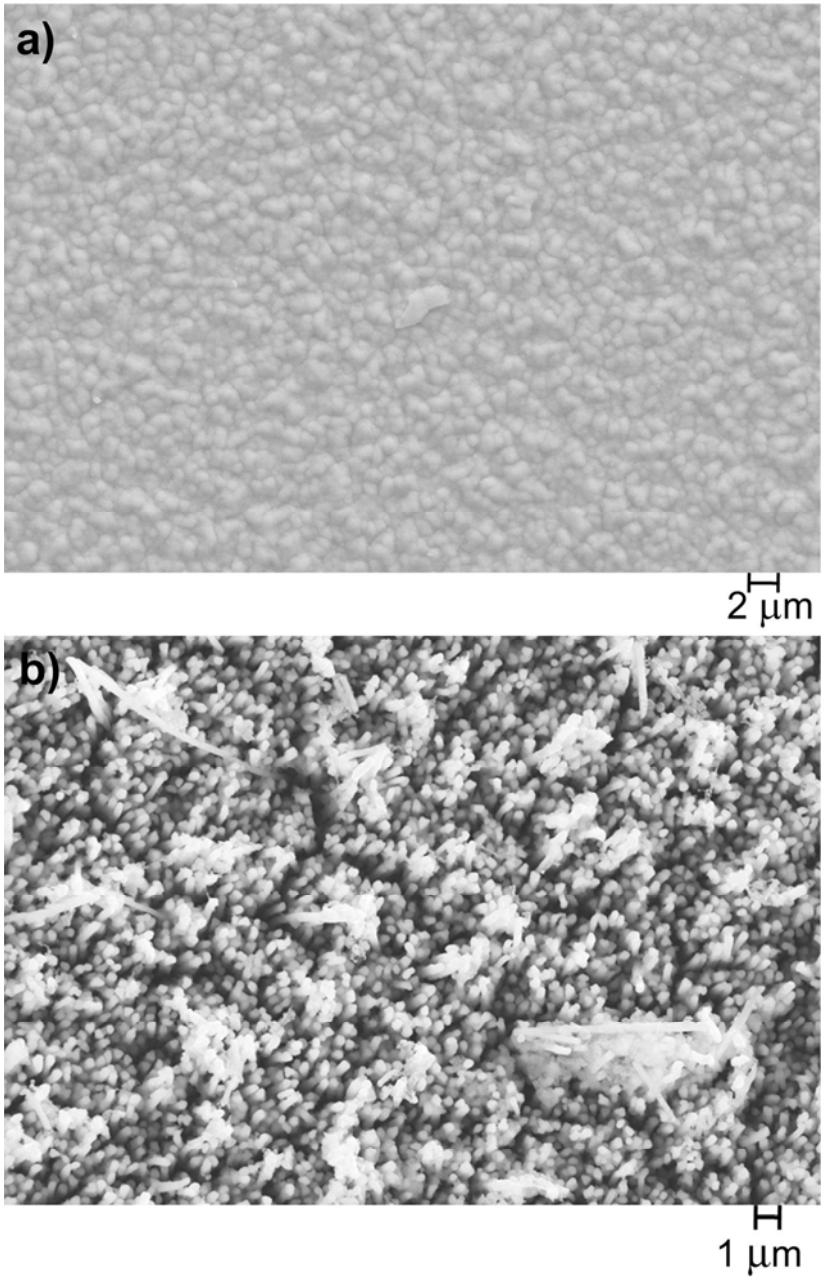

Figure 2.4. Planar vs. nanorod morphology. Top-down SEM images (SE2 detector, 20 kV accelerating voltage) of **(a)** a planar electrode showing the rough morphology characteristic of Cd(Se, Te) electrodeposition and **(b)** a nanorod array electrode displaying a typical, high density of nanorods (> 10^9 cm^{-2}) with very uniform dimensions.

2.3 Photoelectrochemistry

2.3.1 Photoelectrochemical Cell Setup

The photoelectrochemical assembly consisted of the working electrode, a Pt gauze counter electrode, a Pt wire reference, and a liquid electrolyte, all in a glass cell. The electrolyte was 1 M Na_2S and 1 M S in aqueous 1 M NaOH, maintained under an Ar ambient. The cell potential determined at the Pt reference electrode was -0.76 V vs. SCE, which corresponds to the redox potential of the solution species and is in agreement with the literature value of the Nernst potential for this electrolyte.[89] The electrolyte was deoxygenated when made, and was kept under a positive pressure of Ar through the use of a Schlenk line. To prevent evaporation of the solution, the Ar was saturated with water vapor by bubbling the gas flow through 18 MΩ cm resistivity H_2O prior to introduction of the gas into the cell.

Current density vs. potential (*J-E*) data were measured using a Solartron SI 1287 potentiostat. Light from a Sylvania ELH-type halogen projector bulb was passed through a ground-glass diffuser to provide the equivalent of 100 mW cm^{-2}, as measured using a Si photodiode that had been calibrated relative to a secondary standard, NIST traceable, Si photocell calibrated at 100 mW cm^{-2} of Air Mass (AM) 1.5 illumination. Before collection of *J-E* data, each electrode was allowed to reach equilibrium at open-circuit. *J-E* data were then measured on each electrode before and after a photoetch step. Photoetching was performed by immersing the electrode in a 90: 9.7: 0.3 H_2O: HCl: HNO_3 (v/v) solution for 10 s at short-circuit, under 100 mW cm^{-2} of ELH-type illumination.

2.3.2 Current-Potential (*J-E*) Curves

Figure 2.5 displays the *J-E* behavior of a typical planar Cd(Se, Te) electrode under 100 mW cm^{-2} of simulated AM 1.5 illumination. As expected for these electrodeposition conditions, the electrodes exhibited n-type behavior, passing cathodic current at forward bias and showing rectification towards anodic current flow in the dark.[88] For virtually every planar electrode tested, the photoetching step improved the short-circuit current density (J_{sc}), the open-circuit voltage (V_{oc}), and the fill factor, with the greatest improvement occurring in J_{sc}.[90] The annealing step was crucial for photoelectrode performance, as none of the unannealed samples, whether photoetched or not, displayed significant performance under illumination. Although an energy-conversion efficiency as high as ~ 4.1% was recorded for a planar Cd(Se, Te) electrode that had been photoetched and annealed, the majority of the photoetched and annealed planar Cd(Se, Te) electrodes exhibited energy-conversion efficiencies in the range of 1.5 – 3.0%. The thicknesses of the planar deposits were measured with SEM cross-sectional images to be between 2 – 3 μm.

Nanorod array electrodes were fabricated by electrodeposition of Cd(Se, Te) for times ranging from 5 min to 30 min. Those arrays that were measured to have the best performance under illumination had deposition times of 20 min, which corresponded to a total charge passed of 2 – 2.5 C cm^{-2} of template area. SEM images revealed that the nanorods in these arrays varied in length from ~ 3.5 – 7.0 μm. In any particular array, however, the rods were within 1 μm of each other in length. These nanorod electrodes were also tested before and after the photoetching process.

Figure 2.6 shows the *J-E* behavior of one of the best-performing nanorod array electrodes. In many cases, the photoetching step significantly improved the efficiency of the nanorod array electrodes, as it did for planar electrodes. Photoetching of the nanorod arrays always increased J_{sc}, but only sometimes improved V_{oc}. For many of the nanorod electrodes, in fact, the photoetch step significantly reduced V_{oc}. Figure 2.7 displays the *J-E* behavior of one such cell.

Figure 2.8 and Table 2.1 present a direct comparison of the *J-E* behavior of planar versus nanorod electrodes. On the whole, the open-circuit voltage and short-circuit current density of the nanorod arrays were approximately half of the corresponding values for planar electrodes. The fill factors, on the other hand, improved relative to planar electrodes.

Control experiments were performed to evaluate the effect of the sputtered CdSe layer on the performance of the nanorod array electrodes. In these experiments, each step in the fabrication process of a nanorod array was followed, except for the deposition of Cd(Se, Te) into the pores of the template. The resulting electrode thus consisted of a thin layer of annealed CdSe on a Ti/Ni substrate. This electrode had a very low efficiency, of 0.11% before photoetching and 0.03% afterwards. Several planar electrodes were also fabricated with an identical sputtered layer of CdSe between the Ti back contact and the electrodeposited Cd(Se, Te) layer. The behavior of these planar electrodes was nominally indistinguishable from those that did not have the sputtered layer, with each such control electrode exhibiting values of the open-circuit voltage, short-circuit current density, and efficiency that were within the same distribution as those measured for samples that did not have the sputtered layer.

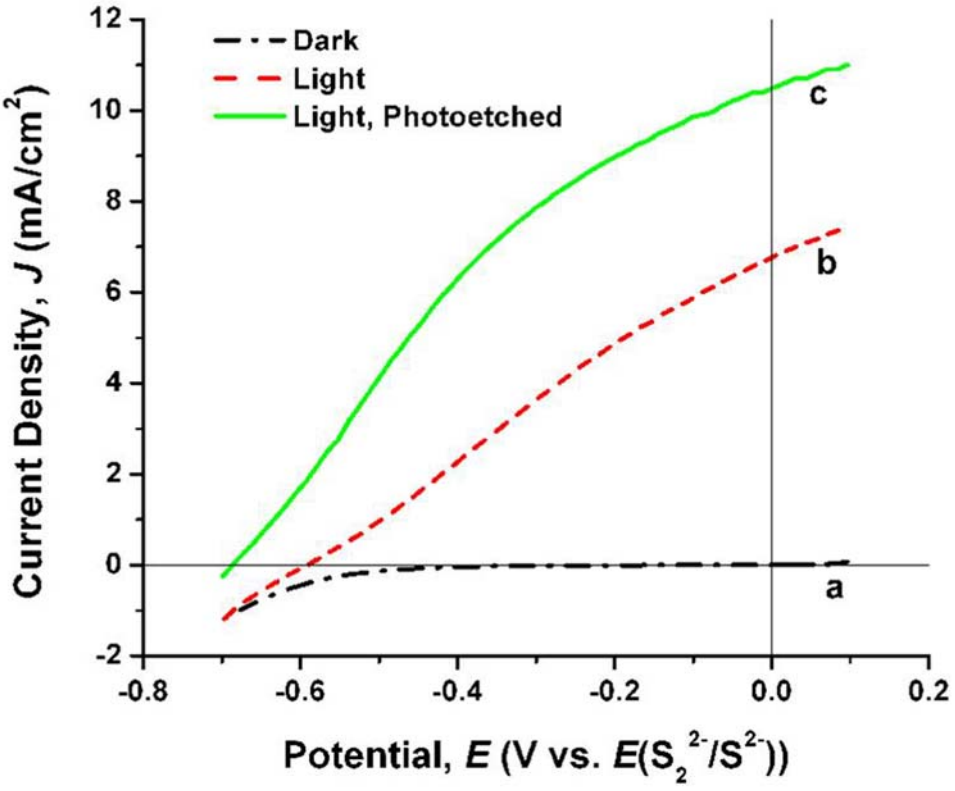

Figure 2.5. *J-E* data for a typical planar photoelectrode before and after photoetching. The black dashed-dotted line **(a)** is the behavior in the dark before photoetching (the behavior in the dark after photoetching was nominally identical, on this scale); the red dashed line **(b)** is the behavior in the light before photoetching; and the green solid line **(c)** is the behavior in the light after photoetching.

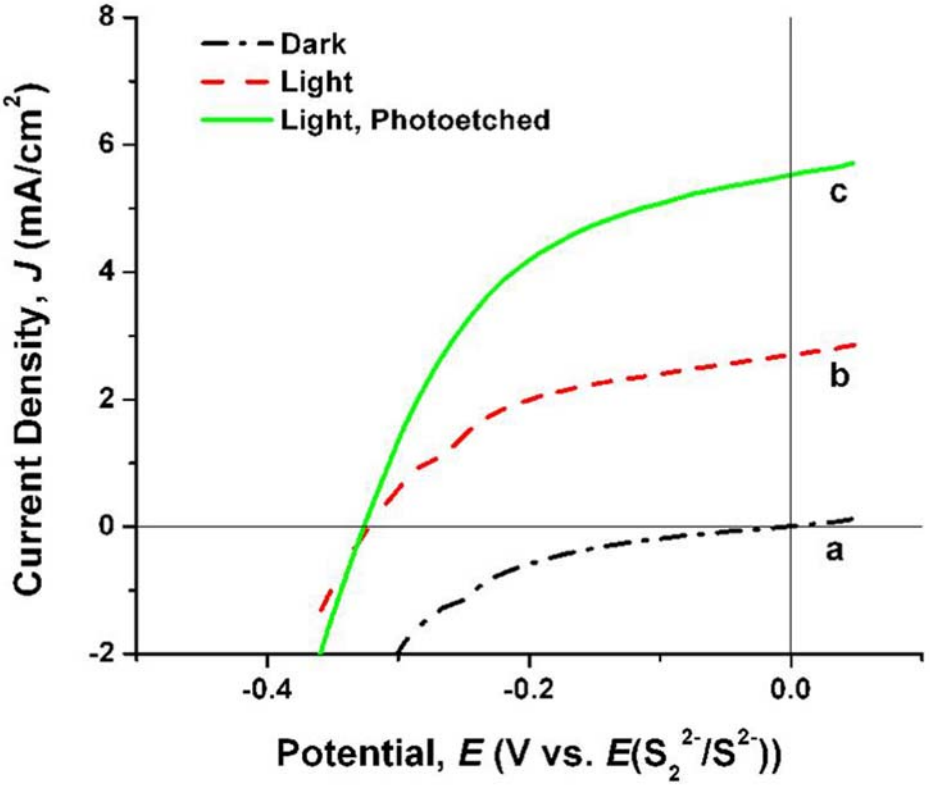

Figure 2.6. *J-E* curves of one of the best nanorod array electrodes before and after photoetching. The black dashed-dotted line **(a)** is the behavior in the dark before, or after, photoetching (no significant difference was observed between the two traces on this scale); the red dashed line **(b)** is the behavior in the light before photoetching; and the green solid line **(c)** is the behavior in the light after photoetching.

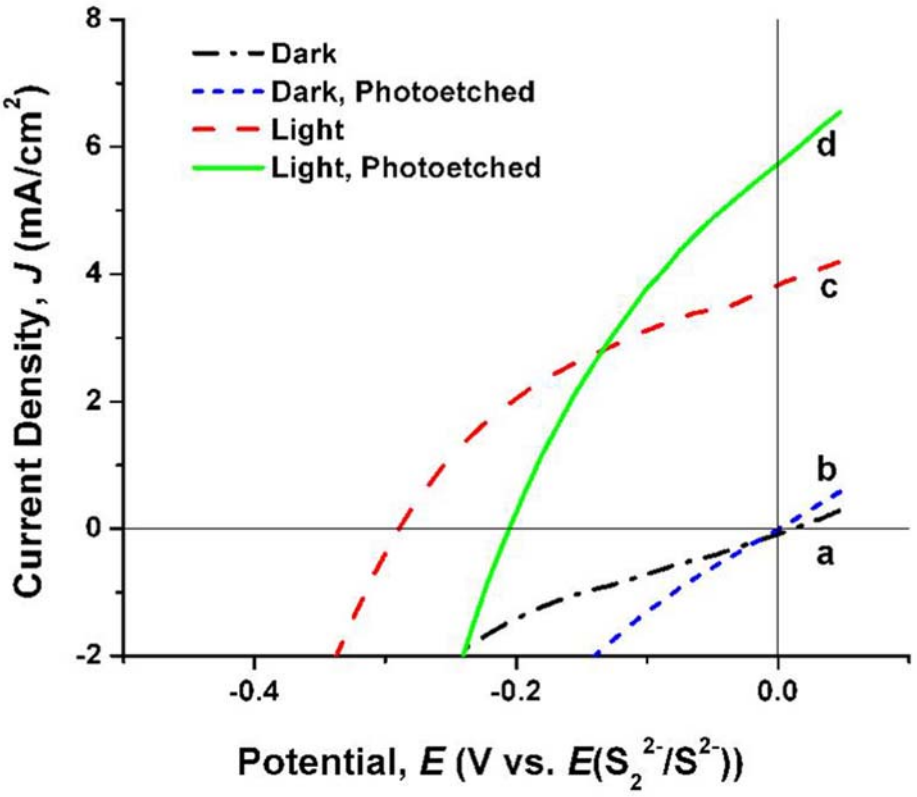

Figure 2.7. *J-E* data for a nanorod array electrode before and after photoetching. In this more common case, V_{oc} was reduced by the photoetch step. The black dashed-dotted line **(a)** is the behavior in the dark before photoetching; the blue short-dashed line **(b)** is the behavior in the dark after photoetching; the red dashed line **(c)** is the behavior in the light before photoetching; and the green solid line **(d)** is the behavior in the light after photoetching.

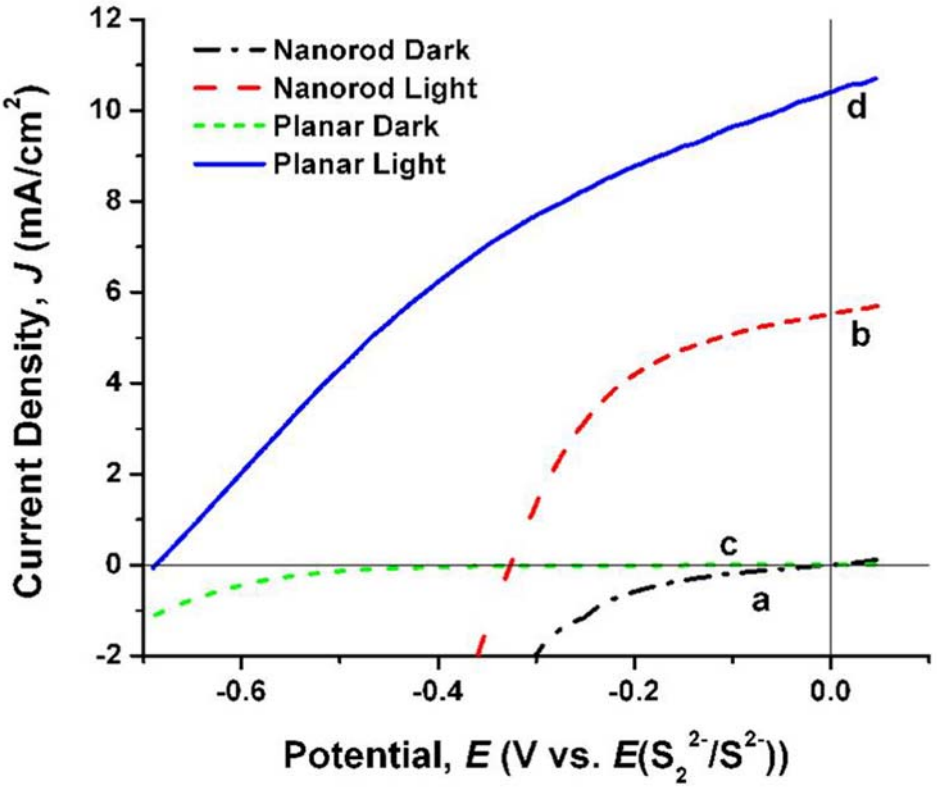

Figure 2.8. Comparison of the *J-E* curves of the planar and nanorod array cells. The responses shown are for photoetched electrodes. The black dashed-dotted line **(a)** is the behavior of the nanorod array in the dark; the red dashed line **(b)** is the behavior of the nanorod array in the light; the green short-dashed line **(c)** is the behavior of the planar electrode in the dark; and the blue solid line **(d)** is the behavior of the planar electrode in the light.

Table 2.1. Average *J-E* data for planar and nanorod array electrodes.[a]

Electrode	V_{oc} (mV)	J_{sc} (mA/cm^2)	Fill Factor	Efficiency
Planar	557 ± 66	6.1 ± 0.8	0.288 ± 0.041	0.98 ± 0.16%
Photoetched Planar	650 ± 63	10.0 ± 3.4	0.358 ± 0.025	2.35 ± 0.95%
Nanorod	274 ± 36	4.0 ± 1.2	0.428 ± 0.051	0.45 ± 0.10%
Photoetched Nanorod	260 ± 27	5.6 ± 1.2	0.433 ± 0.055	0.62 ± 0.19%

[a] The data are from 10 typical planar photoelectrodes and 7 nanorod array photoelectrodes that did not exhibit substantial reductions in open-circuit voltage with photoetching.

2.4 Spectral Response

2.4.1 System Setup

Spectral response measurements were performed immediately after each set of *J-E* data was obtained. The spectral response apparatus consisted of a 50 W Xe arc lamp, a quarter-wave monochromator equipped with 2.5 mm slits, a glass slide to direct a percentage of the beam to a reference Si photodiode, and an optical mirror to direct the remaining light onto the working electrode in the photoelectrochemical cell. The short-circuit current through the cell, and through the reference diode, was recorded simultaneously using two Princeton Applied Research Model 173 potentiostats. The absorbance of the liquid electrolyte was measured at each wavelength, using a UV-vis spectrophotometer.

2.4.2 Nanorod Array vs. Planar Normalized External Quantum Yield

As expected from the magnitude of the J_{sc} values, the planar electrode displayed a significantly higher external quantum yield than did the nanorod array electrode. A good planar electrode exhibited a maximum quantum yield of ~ 0.45 at 580 nm. In contrast, the best of the nanorod array electrodes exhibited a quantum yield of 0.29 at the same wavelength. Absorbance spectra taken on the polysulfide liquid electrolyte confirmed that the solution was highly absorbing at wavelengths, λ, < 500 nm, accounting for the decline in external quantum yield of the Cd(Se, Te) photoelectrodes at short wavelengths.

Although the external quantum yield of the planar electrode decreased with increasing wavelength, that of the nanorod array electrode stayed relatively constant until the onset of the band gap. Figure 2.9 depicts the spectral response data from two electrodes that were characteristic of the response of typical electrodes of each type. The data in Figure 2.9 have each been normalized to their respective points of highest quantum yield, so that the shapes of the spectral response data can be readily compared. The nanorod array electrodes exhibited a smaller decline in quantum yield near the band gap energy than did the planar electrodes, indicating that nanorod array samples more effectively collected minority-carriers generated from photons having longer penetration depths than planar electrodes.

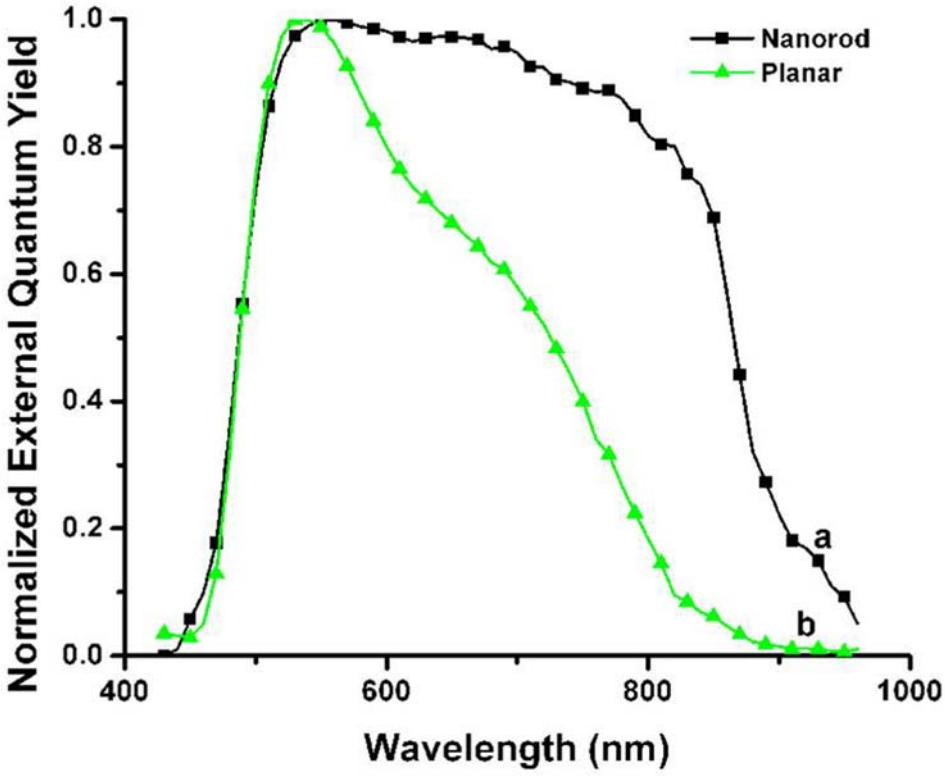

Figure 2.9. Spectral response of typical photoetched planar and nanorod array photoelectrochemical cells with the external quantum yield normalized to its highest value. The quantum yield of the nanorod array electrodes at wavelengths greater than 600 nm decreased less than that of the planar electrodes. The black solid line with squares **(a)** is the normalized spectral response of the nanorod array electrode, and the green solid line with triangles **(b)** is the normalized spectral response of the planar electrode.

2.5 Discussion of Nanorod Array vs. Planar Behavior

2.5.1 Spectral Response

The spectral response data indicate that the nanorod array electrodes behave as if they had a much longer minority-carrier collection length than planar electrodes made using nominally identical materials fabrication processes. In a planar electrode, photons of energies at or near the band gap energy penetrate deeply into the absorber, producing electron-hole pairs that are physically remote from the collecting junction. For absorbers having minority-carrier collection lengths shorter than the optical absorption depth, these remotely generated electron-hole pairs cannot be effectively collected at the junction, and such electrodes therefore suffer a loss in quantum yield at these excitation energies. CdSe, CdTe, and the Cd(Se, Te) alloys are direct band gap materials whose absorption coefficient rises relatively quickly as the photon energy is increased above the band gap energy. Hence, the monotonic increase in quantum yield for planar electrodes until very short wavelengths are approached (Figure 2.9) indicates that the minority-carrier collection length is relatively small in such samples, and the short-circuit photocurrent density and photoelectrode efficiency suffer from this materials-related deficiency.

The spectral response behavior of the nanorod electrodes affords a striking contrast to that of the planar electrodes. Photogenerated charge-carriers are effectively collected even for the deepest penetrating photons above the band gap energy. Hence, the nanorod array electrodes effectively combine long absorption depths with small minority-carrier collection lengths, offering a method for obtaining high short-circuit photocurrent densities even from low collection length materials.

Electrodeposited Cd(Se, Te) films have been reported to have a relatively low doping density. On films that were electrodeposited using nominally identical methods to those employed herein, the doping density has been estimated to be ~ 10^{15} cm^{-3}, through use of the Gärtner model to analyze the response of photocurrent produced by monochromatic illumination as a function of the reverse bias voltage.[88, 91] Such a doping level corresponds to a depletion width of ~ 1 μm, implying that the nanorods in the arrays studied herein are essentially fully depleted of majority-carriers. Hence, for the nanorods under investigation, the collection length is dominated by the width of the space-charge region, with some relatively smaller contribution from diffusive minority-carrier transport. Regardless of whether diffusion or drift determine the minority-carrier collection length, the data are in accord with expectations that the nanorod geometry allows more efficient collection of photogenerated minority-carriers over a limited collection length than does a planar structure having a thickness sufficient to obtain full optical absorption throughout the solar spectrum.

2.5.2 Short-Circuit Photocurrent Density

The nanorod array electrodes did, however, exhibit lower overall short-circuit current densities than the planar electrodes, despite the improved relative quantum efficiency vs. wavelength for the nanorod array samples (Table 2.1). This likely reflects, at least in part, the lack of a complete filling fraction of the incident optical plane of the specific nanorod electrode arrays used in this work. The filling fraction (projected area of the rods divided by the total projected area of the rods and the voids in between) of the arrays was estimated to be only 0.3. Methods to prepare higher density nanorod arrays, with less

void area between the rods, are therefore of interest. Optical scattering should partly mitigate the lack of a high optical filling fraction of the nanorod arrays, and light trapping schemes can in principle be used to enhance the optical absorption in such systems. Although the planar samples were dark gray in color, the nanorod array electrodes were jet black. Hence, to some extent, light trapping is already occurring, but not with sufficient magnitude to produce the highest quantum yields that are possible from such systems.

2.5.3 Open-Circuit Voltage

A significant difference in performance between the nanorod array electrodes and the planar electrodes is in the open-circuit voltage, V_{oc}. The nanorod array electrodes clearly yielded smaller V_{oc} values than the planar electrodes (Table 2.1). The decline in V_{oc} for nanorods can in general be related to two factors, one inherent to the nanorod array geometry, and one that can in principle be manipulated with optimized materials processing and junction formation. The inherent effect is that the nanorod array electrodes distribute the photogenerated minority-carrier flux over a larger junction collection area than is present for a planar electrode geometry. Specifically, the ratio of the junction area for a nanorod array electrode to a planar electrode is:

$$\gamma = A_{NR}/A_P = (2\pi rh\rho_{NR}A_P)/A_P = 2\pi rh\rho_{NR} \quad (2.1)$$

where A_{NR} is the junction area of the nanorod array electrode, A_P is the area of the planar electrode junction, r is the radius of a single nanorod, h is the height of the nanorods, and ρ_{NR} is the density of nanorods (number of rods per unit of planar base area). Note that this definition of γ only considers the area of the sidewalls of the rods and neglects the

area of the top of the rods and of the base between rods. For the arrays used herein, $r \sim$ 100 nm, $\rho_{NR} \sim 10^9$ nanorods cm^{-2}, and h varied from 3.5 to 7.0 μm. For a nearly optimum absorber thickness, i.e., with $h = n(1/\alpha)$, with $n \sim 2$ - 3 where α is the absorption coefficient, $\gamma \sim 19$ for the same radius and density rods. For the specific samples used herein, $\gamma \sim 22$ - 44. Hence, if the charge is collected over the entire nanorod surface and if the rate of production of photogenerated charge-carriers is the same for both samples, then the minority-carrier flux across the junction boundary will be less for each nanorod in the nanorod array electrode than is present across the same projected area for the planar junction system.

Because the open-circuit voltage is related to the photocurrent density across the junction area by the relationship:

$$V_{oc} = (nk_BT/q) \ln(J_{sc}/\gamma J_o) \quad (2.2)$$

where n is the diode quality factor, k_B is Boltzmann's constant, T is the temperature, q is the elementary charge, J_o is the reverse saturation current density over the actual junction area, and J_{sc} is the short-circuit photocurrent density per unit of projected device area, V_{oc} will be decreased in nanorod electrode arrays having $\gamma >> 1$ relative to the value of V_{oc} produced by an analogous absorber and junction in a planar electrode arrangement. Note that for $\gamma >> 1$ this inherent geometry effect will tend to bias the optimum design away from the smallest nanorod diameters, due to the resultant increased junction area of such systems. In the present case, the increased junction area per unit of projected area is a factor of ~ 30, which will produce a decrease in V_{oc} of ~ 90 mV (higher for $n > 1$) for the nanorod array electrode relative to the planar electrode, if all other parameters are equivalent. Since the J_{sc} of the nanorod array electrodes was, however, lower than that of

the planar electrodes, an even lower V_{oc} will result from the theoretical limit of Equation 2.2 for such samples. Furthermore, Equation 2.2 does not account for the exponential light absorption along the length of the rod, which would yield reduced quasi-Fermi level separation relative to the material at the front surface of the cell and further reduce V_{oc}. This, however, is a second-order correction that would require a full analytical treatment to describe properly.

Surface and/or junction recombination, which is more important in systems having a higher junction area per unit of projected area than a planar system, can also lower V_{oc} in nanorod array electrodes. The value of V_{oc} for junctions between the Cd(Se, Te) electrodes and the S_2^{2-}/ S^{2-} electrolyte is lower than the bulk recombination-diffusion limit, which is approximately 1.0 V under AM 1.5 100 mW cm^{-2} conditions according to the Shockley diode equation.[29] This indicates that the limiting process at present is related to a recombination process associated with the solid/liquid junction. In addition, the full depletion of the nanorods under study will produce a lower value of the band bending in the nanorod arrays than in the planar samples. Hence, improved fabrication methods that increase the doping of the rods, and/or lower the J_o of the solid/liquid contact are expected to produce an increase in V_{oc} for such systems, up to the value of the theoretical limit obtained from the Shockley diode equation using the junction-area-corrected relationship of Equation 2.2.

Experimental evidence that V_{oc} in these specific nanorod array systems is limited by junction-derived recombination is also provided by consideration of the effects of photoetching. The improvement in photoelectrode performance due to photoetching is believed to derive from the removal of surface recombination centers as well as a

reduction in the reflectivity of planar electrode samples by the photocorrosion of small pits in the surface.[90] The nanorod array electrodes appeared black and should inherently produce significant internal light scattering and light trapping. Nevertheless, photoetching improved the J_{sc} and external quantum yields of planar and nanorod array samples. In addition, photoetching improved the V_{oc} of some nanorod array electrodes but reduced the V_{oc} of the majority of the nanorod array electrodes. If photoetching occurs due to photocorrosion, and therefore produces a roughening of the surface,[90] surface recombination would then be increased due to the increased value of the junction surface area, thereby decreasing V_{oc}. In contrast, because charge-carriers have a propensity to remain in trap states, the photoetch step will selectively etch surface defects, thereby offering a mechanism to increase V_{oc}. The trade-off between these two competing effects could account for the observation that photoetching improved V_{oc} in some cases and lowered it in others.

2.5.4 Fill Factor

The nanorod arrays exhibited better fill factors than the planar samples investigated in this study. However, the fill factors measured here for the planar electrodes were low relative to values reported previously for electrodeposited Cd(Se, Te) in contact with the same liquid electrolyte.[88] Some cracking of the Cd(Se, Te) layer during the annealing step may have led to pinholes that could account for the lower fill factor. Nevertheless, using nominally identical electrodeposition conditions, the nanorod array electrodes consistently exhibited better fill factors than their planar counterparts. This difference is consistent with the well-documented slow interfacial hole-transfer kinetics of the S_2^{2-}/S^{2-}

electrolyte. These slow charge-transfer kinetics produce a competition for minority-carriers between collection across the interface and surface recombination, with the potential dependence of these processes determining the fill factor of the device.[92, 93] Accordingly, use of electron-transfer catalysts and/or rapid, one-electron transfer donors as redox species has been shown to improve the fill factor of n-GaAs/KOH(aq)-Se_2^{2-}-Se^{2-} junctions.[94] In such systems, increases in the surface area of the electrode can therefore tend to favor charge-transfer relative to surface recombination because, at constant light intensity, the minority-carrier flux to the junction is reduced as the internal junction area is increased. Such effects would lead to an improved fill factor for such systems, in accord with the observations reported herein.

2.5.5 Avoidance of Shunting

When a liquid junction contact is used in conjunction with a nanorod array electrode, a significant shunt conductance will be produced if the electrolyte directly contacts the back ohmic electrical contact. In this work, this issue was mitigated by sputtering a thin layer of CdSe over the bottoms of the pores of the AAO at the beginning of the electrode fabrication process. In this way, the Ti contact cannot be exposed to the liquid electrolyte. This procedure raises the question of whether the sputtered CdSe layer contributed significantly to the observed properties of the Cd(Se, Te) nanorod array photoelectrode. Control experiments were conducted using this sputtered layer alone, and the resulting performance was quite low in comparison to what was measured for nanorod arrays. Considering that only a fraction of this area could be exposed to light when the nanorods were present, the contribution of this sputtered CdSe layer to the overall performance is

therefore concluded to be minimal. Such methods therefore demonstrate that it is possible to grow nanorod array electrodes in a template, without the use of a single-crystal substrate of the material being grown to form the nanorod array, without significant shunting.

2.6 Conclusion

Nanorod arrays of Cd(Se, Te) were fabricated using porous alumina templates and their photovoltaic properties were compared with analogous, planar electrodes in a photoelectrochemical cell. Spectral response experiments on both types of electrodes showed that the nanorod arrays exhibited enhanced collection, relative to planar electrodes, of low energy photons absorbed far from the front surface of the cell. The ability of nanorod arrays to maintain relatively high quantum yields in the red is evidence that the theoretical expectation of this geometry to improve carrier collection in diffusion-limited systems is valid. Furthermore, nanorod arrays were observed to have improved fill factors relative to their planar counterparts, possibly attributable to an improved ratio of charge-transfer relative to surface recombination, as a result of increasing the internal junction area. However, open-circuit voltages for the nanorod arrays were less than half the values for planar electrodes. A combination of increased surface recombination and an inherent geometrical limitation contributed to this effect. While these results are encouraging for future nanorod solar cell designs, improvements in the fabrication of these electrodes will need to be made to take full advantage of the benefits offered by this geometry. In particular, lowering the junction recombination rate should lead to large

improvements in the nanorod solar cell. Using single-crystal rods in the array is one method by which this could be pursued. Deposition of the semiconductor with a higher doping density, so that full band bending can be achieved within each nanorod, could also lead to improvements in the performance of the cell.

Chapter 3

Strategies for the Fabrication of Silicon Wire Arrays

3.1 Introduction

Although the Cd(Se, Te) nanorod cell of Chapter 2 was a logical initial experiment to test the radial junction concept, the results of that work indicate this is not an ideal material for realizing the benefits of a radial junction, wire array solar cell. One of the key limitations of the cell was its reduced open-circuit voltage, V_{oc}, relative to the planar cell due in part to increased recombination and the fully-depleted nature of the wires. Better control over the doping, materials properties, and surface conditions will be necessary to improve the V_{oc} and produce a wire array that can meet the theoretical expectations.

Silicon seems an ideal material for making these advancements in wire array performance. Being an indirect gap absorber with a long optical absorption depth (100 – 200 μm), low-quality Si is generally minority-carrier collection limited and could potentially benefit from the radial junction architecture. As the dominant semiconductor in the PV industry, there is a wealth of knowledge about how to controllably dope Si and affect its materials properties. Even though reports of Si nanowires have shown the

possibility of one-dimensional growth, the challenge remains to assemble Si wires into a uniform, controllable array that can eventually be doped and contacted to produce a high-efficiency solar cell.

3.2 Silicon Properties

At present, Si is by far the most commonly used semiconductor in the terrestrial photovoltaics industry, accounting for ~ 90% of the PV market.[20, 21] The success of Si is due to several beneficial attributes. It has a band gap energy of 1.12 eV, well matched to the terrestrial solar spectrum.[21, 29] Si is, however, an indirect gap semiconductor and consequently requires > 100 μm of material to absorb most of the incident light. Due to its abundance, this is not an overwhelming design constraint. In fact, Si is the second most common element in the Earth's crust (Figure 3.1).[95] Considering the enormous areas that will need to be covered with photovoltaics to approach 10 TW of carbon-free energy (see Section 1.2), it will be essential that the dominant semiconductor in PV technology be extremely abundant. In contrast, the promising thin film technologies CdTe and $CuInSe_2$ (and its alloys) employ elements that may not be useable at this scale. Indium (In) and selenium (Se) are approximately as common as silver (Ag), while tellurium (Te) is only slightly more common than gold (Au) (Figure 3.1). Although these films can be made inexpensively at their present scale due to the lack of competition for materials like Te, they would likely suffer from scarcity issues upon scaling up to the TW range. Si has a further advantage over competing technologies like CdTe and GaAs in that it is nontoxic. Cd and As are both highly toxic and are known carcinogens.

Covering the land with square miles of these materials with only glass encapsulation to prevent them from leaching into the groundwater has significant potential health risks.

Silicon is also the benefactor of decades of research by the microelectronics industry. A great deal is known about the crystal structure and surface planes, isotropic and anisotropic etch techniques, controllable doping of both n- and p-types, surface passivation methods, effects of impurities, etc.[29, 96, 97] The semiconductor industry prefers Si over materials such as Ge because its oxide can be easily grown and etched and is water-stable. With all of these advantages, Si is likely to play a leading role in the PV industry for years to come.

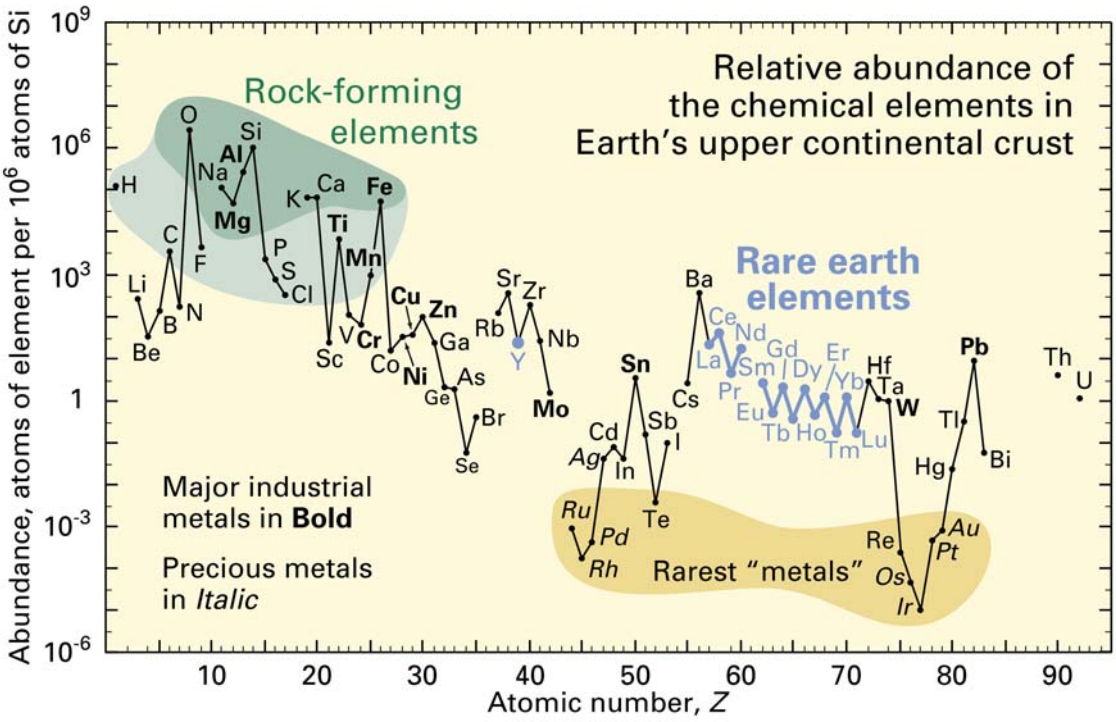

Figure 3.1. Abundance (atom fraction) of the chemical elements in Earth's upper continental crust as a function of atomic number. Many of the elements are classified into (partially overlapping) categories: (1) rock-forming elements (major elements in green field and minor elements in light green field); (2) rare earth elements (lanthanides, La-Lu, and Y; labeled in blue); (3) major industrial metals (global production ≥ 3 x 10^7 kg/year; labeled in bold); (4) precious metals (italic); and (5) the nine rarest "metals" – the six platinum group elements plus Au, Re, and Te (a metalloid). (credit: U.S. Geological Survey).[95]

3.3 Silicon Deposition Methods

3.3.1 Electrodeposition of Silicon

It is possible to fabricate silicon layers via electrodeposition from nonaqueous solvents.[98, 99] The negative electrode potential of Si would result in hydrogen emission in an aqueous medium, so its electrodeposition must be carried out in electrolytes such as

propylene carbonate or tetrahydrofuran under an inert gas. These solutions typically use silicon halide precursors (e.g., $SiCl_4$ or $SiBr_4$) and are nonconducting without the addition of a supporting electrolyte such as tetrabutylammonium chloride or lithium chloride. The electrodeposit can be doped by adding to the electrolyte bath small amounts of PCl_3 or PCl_5 for n-Si or $AlCl_3$ for p-Si.[99] All the materials must be rigorously dried to exclude water.

The electrodeposition of Si could be combined with porous anodic aluminum oxide (AAO) templates to make nanowire arrays in a nearly identical process to that described for Cd(Se, Te) in Chapter 2. Si could even be sputtered from n- or p-type targets to create a shunt-preventing layer at the base of the wires. However, to date, electrodeposited Si has had a microscopic honeycombed structure that has led to significant oxidation throughout the material. The semiconductor properties of these deposits have been quite poor and fundamental research on improving the electrodeposition process is still needed.

3.3.2 Chemical Vapor Deposition of Silicon

Silicon can also be deposited by the decomposition of gas phase precursors. Among vapor-based methods, chemical vapor deposition (CVD) through the vapor-liquid-solid (VLS) process is the most successful for producing Si wires.[42, 100] The many benefits of the VLS mechanism include its tendency to form single-crystal wires,[101] the high growth rates that are achievable (up to several μm/s),[102] the availability of in situ doping

techniques,[103] and the ability to influence the wire diameter by controlling the catalyst size.[104]

In the VLS mechanism (Figure 3.2), a solid impurity metal acts as a preferred site for the deposition of Si from a gas precursor such as SiH_4 or $SiCl_4$, allowing for a very selective growth location as well as accelerated growth rates relative to uncatalyzed deposition under similar conditions.[100] The metal alloys with the Si, forming a liquid eutectic mixture at the reaction temperature (400 – 1100 ºC). As the metal droplet continues to uptake Si from the vapor phase, the concentration increases until the droplet is supersaturated with Si. Crystalline Si then precipitates from the alloy droplet, aided by the low activation energy for nucleation at the crystal-melt interface.[105] The metal droplet rises with the Si precipitate, resulting in the one-dimensional growth of Si wires. Under most conditions, the wire grows in the <111> crystal direction with the side facets usually having a {211} orientation.[42] If the catalyst metal has a low solubility in solid Si, the wire will not taper appreciably and will have a diameter approximately equal to the metal droplet diameter. Although Au has predominantly been used for VLS Si wire growth, several metals including Cu, Ni, Pt, and others are predicted to meet the necessary catalyst criteria.[105]

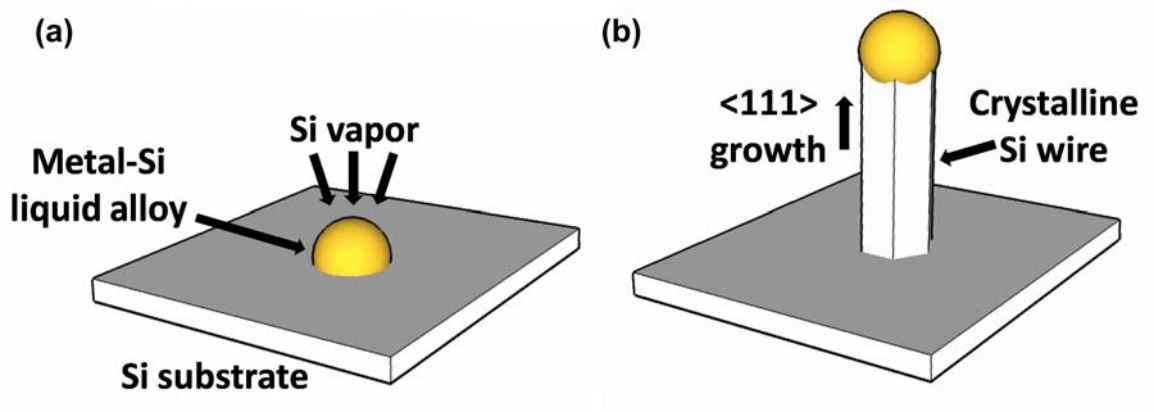

Figure 3.2. Schematic of the vapor-liquid-solid (VLS) mechanism of Si wire growth. **(a)** A solid metal catalyst forms a liquid eutectic alloy upon uptake of Si from the vapor phase. **(b)** When the metal becomes supersaturated, Si crystallizes out (typically in the <111> direction) and forms a one-dimensional wire with the catalyst droplet at the tip.

3.4 VLS-Grown Si Nanowires in Porous Alumina Templates

3.4.1 Benefits of a Template with the VLS Method

Despite the many advantages of the VLS technique for Si wire growth, it has a few key drawbacks. The growth of a high-quality Si wire array typically relies on a single-crystal Si wafer to produce aligned, crystalline wires epitaxially attached to the substrate.[106-110] The use of an expensive wafer detracts from the mission of the radial junction solar cell to be a low-cost photovoltaic. Also, it can be difficult to control the pattern and diameter uniformity of the wires due to the tendency of the catalyst metal to migrate on the substrate surface at reaction temperatures.

The use of AAO templates to guide and control the VLS process addresses both of these drawbacks. The pores should be able to confine both the catalyst metal and the Si deposition so that aligned wires of uniform dimensions are fabricated. Redwing et al.

have demonstrated that this can be done by electrodepositing metal into the pores and then exposing the template to SiH_4.[111-113] While we are not aware of any AAO-fabricated Si nanowires left as a freestanding array after the dissolution of the template, it should be possible to achieve by the deposition of a low-cost substrate onto one side of the membrane. Such a scheme would enable the fabrication of crystalline, aligned Si wires of uniform dimensions assembled into an array without the need for an expensive substrate. We report herein freestanding Si wire arrays grown with an AAO template-assisted VLS mechanism[114] and discuss the shortcomings of this approach.

3.4.2 Fabrication of Si Wire Arrays with AAO Templates

Nanowire arrays were fabricated using commercially available, 60 μm thick, 200 nm pore diameter, AAO membranes (Whatman Scientific) as templates. A 100 nm thick layer of Au was thermally evaporated onto one side of the AAO to cover the bottoms of the pores with catalyst and to make that side of the template conductive. The other side of the AAO was then covered in a layer of mounting wax to prevent deposition of metal onto the bottoms of the pores in subsequent processing steps. The template was then made into a working electrode by attaching a Cu wire and applying conductive Ag paint around the edge of the membrane. The wire was encased in a glass tube, and the wire contact area was sealed with epoxy.

To provide mechanical stability and support for the nanowire array after the removal of the template, > 10 μm of Ni metal was electrodeposited onto the back of the Au. The Ni substrate was galvanostatically electrodeposited at room temperature, under stirring,

from an aqueous solution of 0.8 M nickel (II) sulfamate ($Ni(SO_3NH_2)_2$) and 0.6 M boric acid (H_3BO_3). In this process, a current density of 25 mA cm^{-2} was maintained for 1 hr between the working electrode and a Pt gauze counter electrode. The mounting wax was then thoroughly removed by several washes in acetone. The AAO template was mechanically removed from the electrode assembly.

To grow Si wires, the AAO with a Ni substrate and Au at the bottom of the pores was inserted into a reactor at ~ 500 ºC and exposed to 5% SiH_4 in Ar at a flow rate of 100 sccm and a total pressure of 1 Torr. The reaction was allowed to proceed for 1 hr or more before removing the sample and allowing it to cool under vacuum. After growth of the nanowires, the AAO template was removed by submersing the array in 1 M NaOH(aq) for 20 min.

Figure 3.3 shows SEM images of a typical Si nanowire array that resulted from the templated VLS growth method. Si nanowires of 200 nm diameter, conforming to the AAO pore size, were regularly fabricated as freestanding arrays on the electrodeposited Ni substrate. Si wires up to ~ 5 μm long were produced after a grow time of 1 hr.

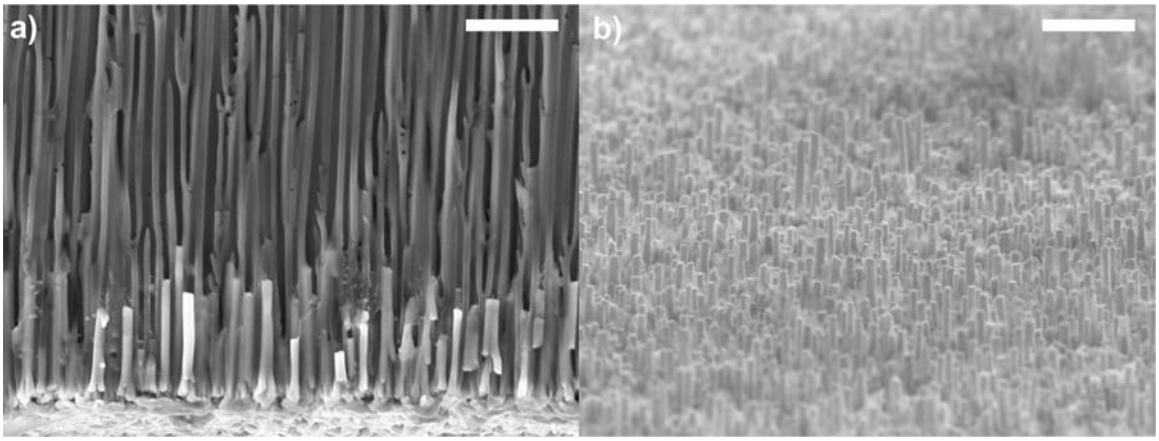

Figure 3.3. Si nanowire arrays grown with AAO templates. (a) Cross-sectional view SEM image of an AAO template with Si wires at the bottom of the pores. **(b)** Tilted-view SEM image of a freestanding Si nanowire array on a Ni substrate after the removal of the template. The scale bar for **(a,b)** is 2 μm.

3.4.3 Shortcomings of Templated VLS Growth

The gradual conformal deposition of Si onto the porous alumina template eventually accumulated until it blocked the pores on the top surface of the membrane (Figure 3.4). This conformal Si deposit made the selective chemical removal of the AAO difficult and limited the length of nanowires attainable. One approach to mitigate the conformal deposition problem would be to switch the carrier gas from Ar to H_2. By Le Chatlier's principle, the presence of excess H_2 would shift the equilibrium of the silane decomposition reaction so that less conformal Si would deposit on the template. This should promote the selectivity of the VLS-catalyzed Si deposition at the bottom of the pores. This approach was not pursued, however, as research began to focus on other Si wire growth strategies.

The difference in thermal expansion coefficients between Ni and alumina (α_{Ni} = 16.8, α_{Al2O3} = 8.8 mm/(mm ºC) x 10^6 at ~ 500 ºC)[115] presented another difficulty with this Si

nanowire array fabrication route. It was commonly observed that thermal stresses induced by heating and cooling the Ni-backed AAO template warped the sample and often resulted in pieces of the brittle alumina chipping away from the metal substrate, which could be a serious problem in any attempt to scale up this fabrication procedure. An alternative route was pursued with some success, wherein a conductive Ag layer was deposited on one side of the AAO followed by selective electrodeposition of Au catalyst at the bottom of the pores. The Ag layer was chemically removed in 8 M HNO_3, and then a thin (< 10 μm) layer of either p- or n-Si was sputtered over the bottom of the AAO to serve as a substrate. This type of sample was put in the reactor to grow Si wires, and as long as the heating and cooling steps were conducted slowly, minimal warping and no chipping were observed. After wire growth, an ohmic metal back contact followed by a thicker metal support layer was applied to the sputtered Si and then the template was removed. Technical difficulties with the silane reactor halted progress on this fabrication scheme, however, and it was not pursued further because an alternative VLS growth approach showed more promise for producing high-quality Si wire arrays.

Although it was demonstrated that vertically aligned, densely packed Si nanowire arrays of highly uniform diameters could be fabricated without expensive substrates via this technique, the limitations of the AAO-templated VLS growth of Si wires make this method less than ideal for producing parallelized radial junction Si solar cells. In addition to conformal Si deposition and AAO warping issues, templating the VLS Si growth is known to introduce polycrystallinity to the wires that is likely to result in lower quality electronic properties than if they were grown without confinement.[35, 116] Radial junction modeling[33] along with the experimental results on Cd(Se, Te) nanowire array

photoelectrodes (see Chapter 2) indicate that very high surface area electrodes will have a significantly reduced open-circuit voltage. At 200 nm, the AAO templates used in this work are already near the upper limit achievable for pore diameter size.[44] It will therefore be difficult to transition to larger diameter, and hence lower surface area, wire arrays by this technique. While the AAO template method can produce Si nanowire arrays that may be useful in other applications that require high surface areas, it is not the best route to fabricate Si wire arrays that are optimized for solar energy conversion.

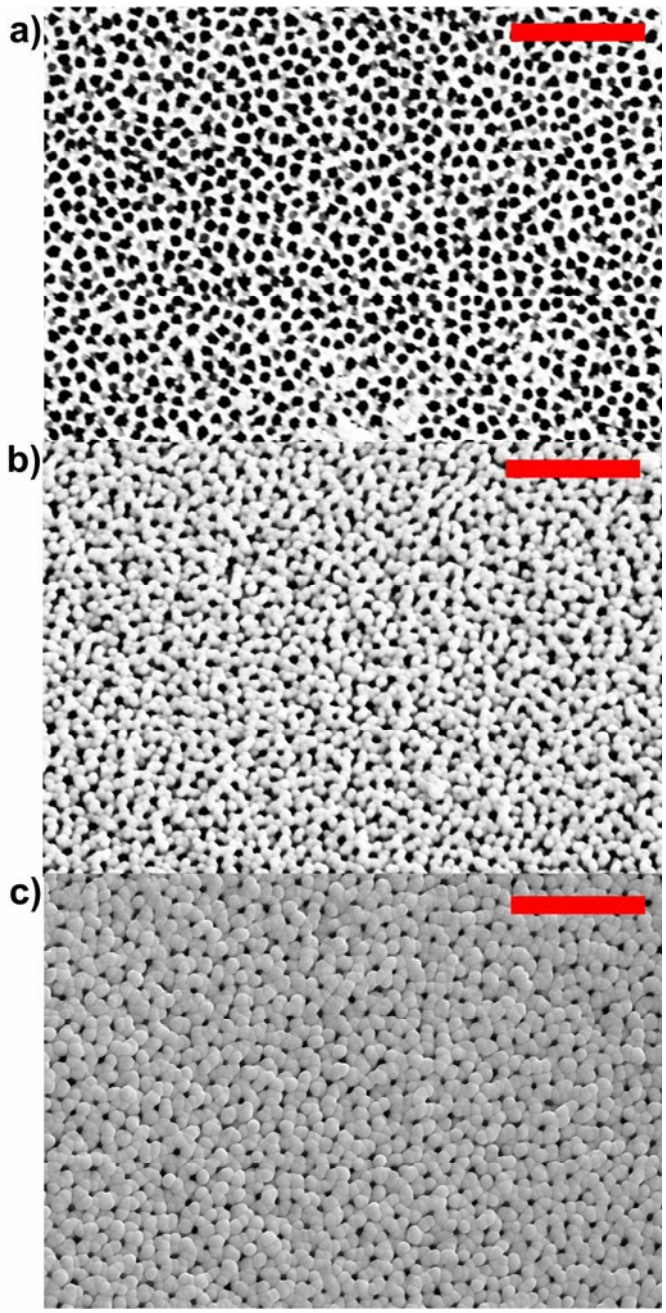

Figure 3.4. AAO template surface after SiH_4 chemical vapor deposition. Top-down view SEM images of an AAO template used to grow Si nanowires after **(a)** < 1 hr, **(b)** ~ 2 hr, and **(c)** ~ 3 hr in 5% SiH_4 in Ar at a flow rate of 100 sccm, a total pressure of 1 Torr, and a growth temperature of ~ 500 ºC . The scale bar for **(a-c)** is 2 μm.

3.5 VLS-Grown Si Microwire Arrays on Si(111) Substrates

3.5.1 Growth of Optimal Si Wire Array Geometry

The best approach for producing Si wire arrays that can be optimized for solar energy conversion is one that allows for the growth of wires with dimensions that are tunable within a wide range and also highly uniform from wire to wire. Control over the dimensions and spacing of the wires within an array is necessary to be able to individually change parameters such as radius, length, or pitch and interpret the effect that each variable has on the experimental results. As previously mentioned, theoretical modeling on radial junction Si solar cells indicates that larger diameter wires will result in a higher V_{oc} and efficiency as long as the minority-carrier collection length is at least equal to the wire radius.[33, 34] Unlike AAO-templated wires, VLS-grown Si wires on a Si wafer substrate are not prevented from having diameters > 200 nm. Therefore, if catalyst placement and growth conditions can be controlled such that uniform wire arrays can be produced, guiding VLS growth with a high-quality Si substrate may be the best way to study the optimal Si wire array geometry.

3.5.2 Growth from SiH_4

Initial attempts to grow Si wire arrays on single-crystal wafers employed a SiH_4 gas precursor. A Si(111) wafer was etched in 10% aq. HF for > 10 s immediately prior to the thermal evaporation of ~ 10 nm of Au onto the surface. The wafer was then put into a silane CVD reactor at ~ 500 ºC and exposed to 5% SiH_4 in Ar at a flow rate of 100 sccm

and a total pressure of 1 Torr to grow Si wires. Upon heating the wafer, the thin Au film broke up and agglomerated into larger pools of catalyst metal (Figure 3.5a). The resulting Si wires were arranged randomly and had widely varying diameters, mostly 100 – 2000 nm (Figure 3.5b). Even after 3 hr of growth under these reaction conditions, wire lengths were generally < 20 μm. Although straight, vertically oriented wires were sometimes achieved, wires were commonly kinked and at angles to the substrate (Figure 3.5b). Kinking occurs when the wire spontaneously switches from its initial [111] direction to one of the other equivalent {111} directions. It is known to occur in VLS growth at lower temperatures and SiH_4 partial pressures.[117] The silane reactor used in this work was not capable of reaching temperatures significantly > 500 ºC, limiting the ability to prevent kinking in this system. Greater control over catalyst size and placement, faster growth rates, and the more consistent growth of straight, aligned wires is needed to produce an ideal Si wire array.

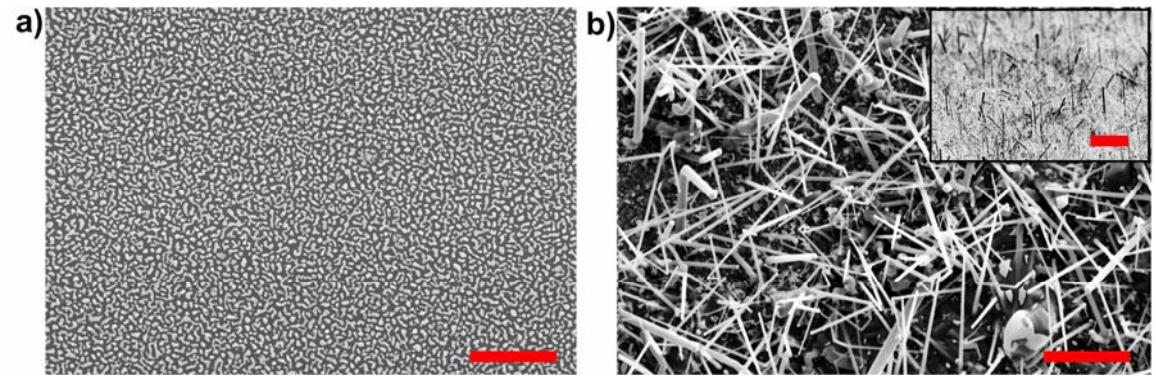

Figure 3.5. VLS Si wire growth from SiH_4 without patterning the catalyst. Top-down view SEM images of **(a)** a Si(111) wafer with ~ 10 nm of Au thermally evaporated on the surface and then annealed under vacuum at ~ 500 ºC for 5 min and **(b)** the same sample after exposure to a 100 sccm flow of 5% SiH_4 in Ar at 1 Torr total pressure and ~ 500 ºC for 3 hr. Scale bar for **(a,b)** is 2 μm. The inset shows a tilted-view SEM image of the Si wires shown in **(b)**. Scale bar for the inset is 10 μm.

3.5.3 Growth from $SiCl_4$

To pursue a better fabrication route for Si wire arrays, a reactor capable of employing $SiCl_4$ as the gas precursor at temperatures above 1000 ºC was built. $SiCl_4$ has several notable advantages over SiH_4 as the VLS gas precursor. At ~ 1000 ºC, wires can be grown at rates > 3 μm min^{-1} with no kinking, allowing the production of wires longer than the optical thickness of Si in < 1 hr. The $SiCl_4$ VLS reaction can be conducted at atmospheric pressure, decreasing the expense of the process by eliminating the need for vacuum technology. In the presence of H_2, HCl is formed in situ that can etch the native oxide from the Si growth substrate, promoting the epitaxial growth of Si wires normal to a [111] surface so that essentially all the wires are in vertical alignment.[106] Finally, as noted earlier (see Section 1.3), $SiCl_4$ is a byproduct of the current process used to produce solar grade Si.[25] In fact $SiCl_4$ is inexpensive enough that some polysilicon producers

have dumped it as a waste product.[118] These factors make $SiCl_4$ VLS growth appealing as a method to produce an ideal Si wire array architecture in a potentially cost-effective, scalable process.

To precisely form the desired wire array geometry, a method is still required to pattern the catalyst metal and control its location and size during Si wire growth. Our research group solved this problem by utilizing conventional photolithography on the Si substrate surface in combination with thermal evaporation to deposit patterns of catalyst metal islands.[119] At reaction temperatures, however, the catalyst pattern fidelity was lost due to metal migration and agglomeration on the Si(111) surface, leading to a low fidelity wire array. This issue was solved by using a thermal oxide buffer layer to confine the VLS catalyst to the patterned areas on the substrate surface. To do this, a buffered HF etch was performed before metal evaporation to remove the oxide from the exposed portion of the photoresist pattern so that the catalyst was deposited on Si but surrounded by SiO_2.

Specifically, a Si(111) wafer with 300 nm of a thermally grown silicon oxide was photolithographically patterned with S1813 photoresist (Microchem), followed by immersion for 4 min in buffered HF(aq) (Transene, Inc., 9% HF, 32% NH_4F) to remove the oxide in the holes formed by exposure of the photoresist. 300 nm of Au was then thermally evaporated onto the wafer, followed by lift-off of the remaining resist. Lithographic patterning resulted in a square array of 3 μm diameter Au islands, having a center-to-center pitch of 7 μm, separated by the SiO_2 layer (Figure 3.6a). The wafers were then annealed in a tube furnace at 1000 ^oC for 20 min under 1 atm of H_2 at a flow rate of 500 sccm, and then wire growth proceeded during a subsequent 30 min step by

addition of a flow of 10 sccm of $SiCl_4$ while maintaining the same pressure, temperature, and H_2 flow rate. This process produced highly uniform, vertically aligned, crystalline Si wires of ~ 1.5 μm diameter over large areas (Figures 3.6b and 3.6c). Uniform arrays > 1 cm^2 were produced, with the area limited only by the size of the reactor tube diameter. Equivalent wire array structures were grown under the same conditions using Cu or Ni as the VLS catalyst.

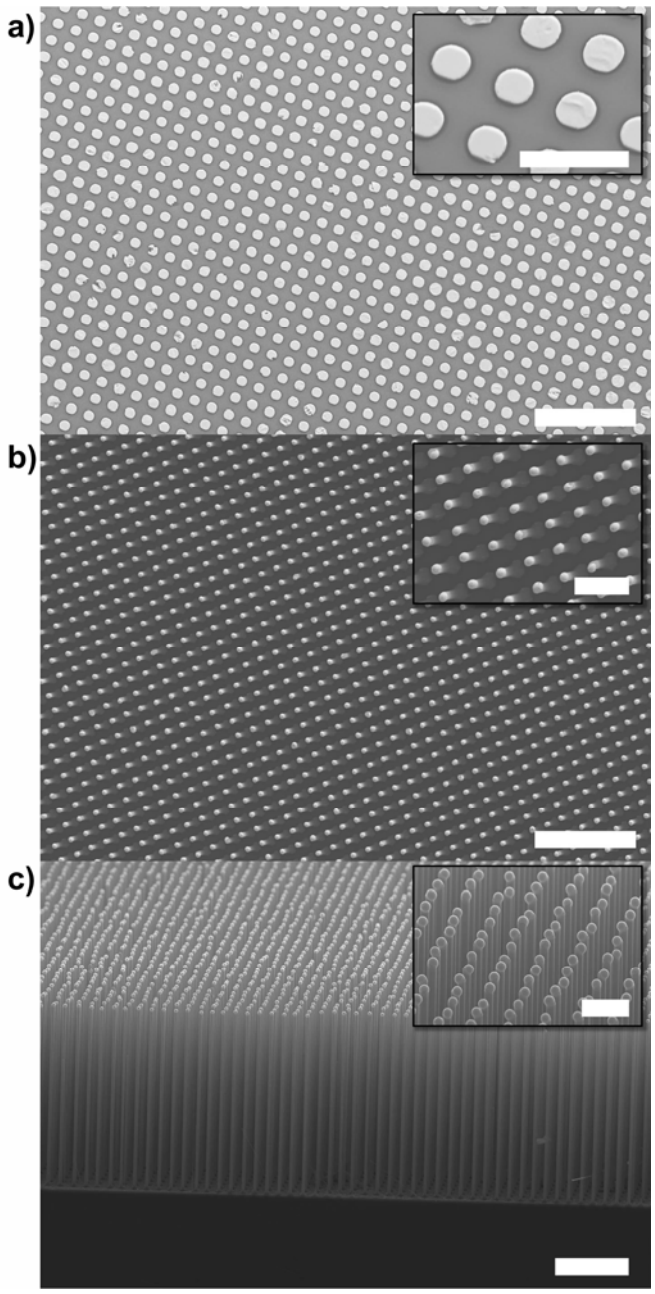

Figure 3.6. VLS Si wire growth from $SiCl_4$ with photolithographically defined catalyst. (a) Top-down view SEM image of a Si(111) wafer photolithographically patterned with 3 μm diameter Au catalyst islands in a square arrangement of 7 μm pitch. **(b)** Top-down view and **(c)** tilted-view SEM images of Si wires grown from 500:10 sccm H_2:$SiCl_4$ at 1 atm and 1000 ºC for 30 min. Scale bar is 40 μm for **(a-c)**, and 10 μm for each inset.

3.6 Effect of Substrate Surface Orientation on Wire Growth

While the primary role of the oxide buffer layer was to constrain the catalyst metal to its patterned location, there was also the possibility that the oxide side walls were helping to guide the nucleation and initial wire formation to grow normally to the substrate surface. To test this, a 300 nm thermal oxide was grown on the surface of Si substrates of (111), (110), and (100) orientation, patterned with 300 nm Au catalyst, and exposed to $SiCl_4$ under the reaction conditions described above (~ 20 min of growth time). Figure 3.7 shows cross-sectional SEM images of the resulting Si wire arrays. As expected, the wires on the Si(111) wafer grew normal to the substrate. However, the wires grew at a ~ 35 º angle to the Si(110) surface and a ~ 55 º angle to the Si(100) surface, indicating wire growth in the [111] direction despite the presence of the thermal oxide buffer layer. Therefore, a single-crystal Si(111) surface appears to be necessary in this process to fabricate vertically aligned epitaxial wire growth.

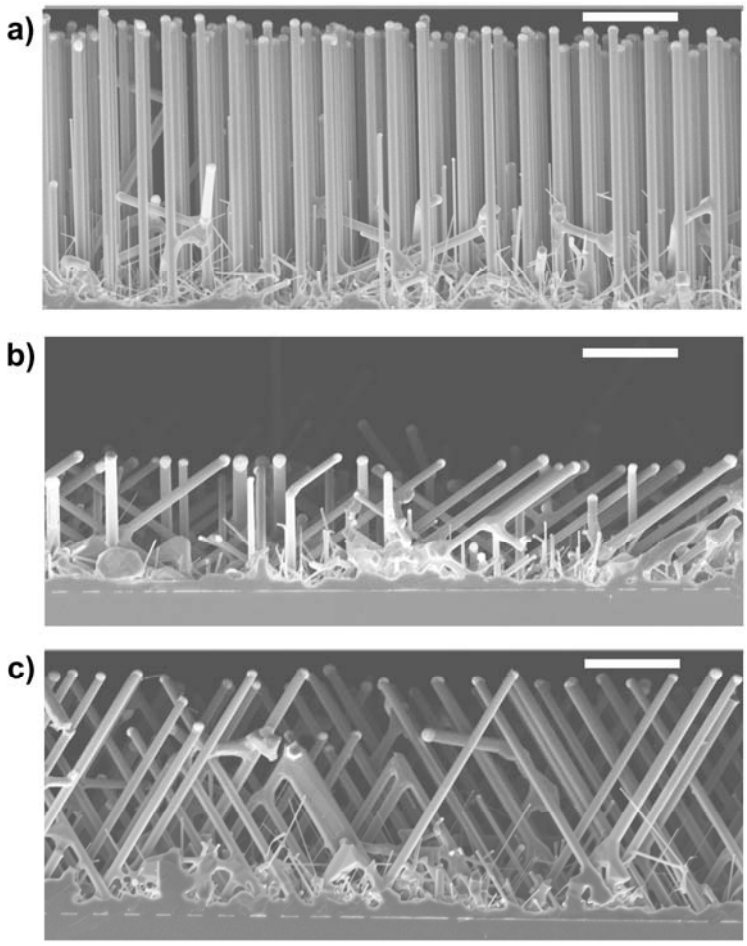

Figure 3.7. VLS Si wire growth from $SiCl_4$ on Si substrates of different crystal orientations. Cross-sectional SEM images of Si wire arrays produced after ~ 20 min of growth on a Si surface of **(a)** (111), **(b)** (110), and **(c)** (100) orientations. Scale bar for **(a-c)** is 20 μm.

3.7 Moving Toward Larger Diameter, Denser Wire Arrays

3.7.1 Motivation and Approach

According to the radial junction theory,[33] larger diameter wires will need to be grown to optimize the energy-conversion efficiency based on the minority-carrier collection length

of the Si wires. Arrays of smaller diameter wires have higher surface area, which increases overall surface recombination and lowers the V_{oc} because of the increased dark current (Equation 2.2). Therefore, without accounting for optical effects, the ideal Si wire array cell would have wires with the largest diameter that could be tolerated based on its minority-carrier collection length. Using e-beam lithography to create contacts to individual wires, four-point probe measurements to Au-catalyzed VLS-grown Si wires indicated minority-carrier diffusion lengths > 2 μm.[120] Similar studies later concluded that both Ni-catalyzed[34] and Cu-catalyzed[121] wires had minority-carrier diffusion lengths ≥ 10 μm. Optimized geometries are therefore likely to have wire diameters significantly larger than the ~ 1.5 μm initially reported.[119]

The photocurrent generated by a Si wire array cell should be optimized by maximizing the light absorption within the wires. In addition to standard industry techniques such as back reflectors and antireflection coatings that could potentially be added to a finalized array, absorption could be improved by increasing the packing density of the wires. The high-fidelity $SiCl_4$ VLS-grown wire arrays reported, with diameters of ~ 1.5 μm in a square arrangement of 7 μm pitch, have a packing fraction (percentage of the cross-sectional device area occupied by wires) of only ~ 4%.[119] Optical absorption studies conducted by our group on these wire arrays indicated that very high absorption is possible with an increased packing fraction, with even relatively sparse arrays (packing fraction ~ 10%) able to absorb nearly 80% of above band gap solar illumination.[122]

With an emphasis on larger diameter, more closely spaced wires, the ability to grow arrays with thermally evaporated catalyst metal becomes limited. As the patterned photoresist holes get closer together and the overlying metal layer gets thicker,

performing the lift-off procedure becomes increasingly difficult. It should be possible to avoid this issue by switching to electrodeposition as the method to selectively place catalyst metal in the holes of the patterned oxide buffer layer. This technique is particularly beneficial because the insulating properties of the oxide layer prevent metal from depositing on the entire surface, resulting in much less catalyst metal that must be recycled or wasted.

3.7.2 Designing for Arrays of a Specific Wire Size

To use electrodeposition to grow larger diameter wires, it should be helpful to have a decent initial estimation of the amount of charge to pass per sample area in order to deposit catalyst plugs that will result in wires of a predetermined radius. The following analysis attempts to provide that estimation. More details are available in the appendix.

The wire radius, r_w, can be related to the catalyst tip volume, V_{cattip}, by considering the contact angle, θ_c, that the specific metal forms with the silicon wire (Figure 3.8a). $\theta_c = 90° + \varphi$, where φ is the angle between the liquid-vapor interface and the direction of wire growth. From this, and assuming no tapering of the wire, it can be determined that:

$$r_w = r_{cat} \cos\varphi \tag{3.1}$$

$$V_{cattip} = \frac{4}{3}\pi r_{cat}^3 \left[1 - \frac{1}{8}\left(3\cos^2\varphi + (1-\sin\varphi)^2\right)(1-\sin\varphi)\right] \tag{3.2}$$

where r_{cat} is the radius of the spherically shaped catalyst tip. The contact angles of the relevant catalyst metals with Si{111} faces are known,[105] and Table 3.1 uses this information with Equations 3.1 and 3.2 to show V_{cattip} in terms of r_w.

The volume in Equation 3.2 is the same volume of catalyst (perhaps multiplied by a factor to account for any volumetric expansion upon saturation with Si and conversion to a eutectic alloy, which will be neglected here) that must be present on each patterned site on the substrate during growth. However, if a pure wafer is being used as the substrate, a fraction of the deposited catalyst metal will dissolve into the wafer during the annealing stage up to its solid solubility at 1000 ºC. The volume of the catalyst plug, $V_{catplug}$, that must be deposited on the substrate is therefore equal to the wire catalyst tip volume, V_{cattip}, plus the volume per plug of pure catalyst metal that is dissolved into the wafer at the reaction temperature, $V_{catwafer}$:

$$V_{catplug} = V_{cattip} + V_{catwafer} \tag{3.3}$$

The volume of metal per catalyst plug that would be dissolved into a pure Si wafer, assuming sufficient annealing time to reach saturation and a substrate with a fully patterned front surface, is:

$$V_{catwafer} = \frac{C_{s,cat} M_{cat} t_{wafer}}{N_A \rho_{cat} \rho_{elec}} \tag{3.4}$$

where $C_{s,cat}$ is the solid solubility of the catalyst metal in Si at 1000 ºC (values in Table 3.1), t_{wafer} is the thickness of the wafer (excluding oxide thickness), N_A is Avogadro's number (6.022 x 10^{23} atoms/mol), M_{cat} is the molecular weight of the catalyst metal, ρ_{cat} is the mass density of the catalyst metal, and ρ_{elec} is the number of catalyst plugs per unit of projected electrode surface area. For a square arrangement and hexagonal arrangement, respectively:

$$\rho_{elec,square} = \frac{1}{p^2} \tag{3.5}$$

$$\rho_{elec,hex} = \frac{2\sqrt{3}}{3p^2} \tag{3.6}$$

where p is the pitch, or center-to-center distance, of the catalyst particles. If the substrate is being reused for wire growth (see Section 4.3), $V_{catwafer}$ should be near zero, unless the wafer has been gettered to lower the impurity concentration. In that case, Equation 3.4 should be adjusted accordingly for the concentration of catalyst metal left in the wafer after gettering.

The thickness of the deposited catalyst plug can also be determined. The hole within the thermal oxide layer where the catalyst is deposited is actually a truncated cone (Figure 3.8b) rather than a cylindrical shape because buffered HF etches SiO_2 isotropically and thus undercuts the photoresist at approximately the same rate it etches downward.[96] Note that this means the center-to-center pitch must be greater than twice the oxide thickness plus the patterned hole diameter or else the holes will begin to etch into each other. The minimum pitch could possibly be changed in a future processing scheme by using an anisotropic dry etch such as reactive ion etching, in which case a cylindrical hole should be used instead. The radius of the oxide holes, r_h, is set by the photolithography mask but can be made larger by extended etching. When designing a mask, r_h should be > r_w, and most likely $r_h \geq r_{cat}$. It is unclear what minimum oxide thickness is necessary to confine the catalyst metal on the Si surface during the reaction. However, an oxide thickness, $t_{ox} \geq t_{cat}$, where t_{cat} is the deposited catalyst thickness, should prevent the catalyst from migrating and lowering the pattern fidelity. Assuming then that the deposited catalyst layer is not thicker than the oxide, and that the oxide etch

is well calibrated so that the bottom of the hole is the expected size, the volume of catalyst in the patterned hole is:

$$V_{catplug} = \frac{1}{3}\pi\left[t_{cat}^3 + 3t_{cat}^2 r_h + 3t_{cat} r_h^2\right] \tag{3.7}$$

Knowing r_h and determining $V_{catplug}$ from Equations 3.2 – 3.4 and Table 3.1, t_{cat} may be calculated to estimate the necessary t_{ox} for a given wire radius.

The total charge that must be passed in an electrodeposition process can be determined from the volume of each catalyst plug along with the pattern arrangement and pitch:

$$Q = \frac{nF\rho_{cat} V_{catplug} A_{elec} \rho_{elec}}{M_{cat}} \tag{3.8}$$

where Q is the total charge passed, n is the number of electrons required to deposit one atom of catalyst metal, F is Faraday's constant, A_{elec} is the projected surface area of the electrode exposed to electrodeposition conditions, and the other variables have the meanings defined above.

The preceding analysis does not account for volume expansion or contact angle differences due to changes in the surface tension when the catalyst droplet is saturated with Si at reaction temperatures. However, these formulas should enable a reasonable first estimate to be made for the total charge that must be passed to electrodeposit the proper amount of catalyst that will yield a desired Si wire diameter. Correction factors could be determined by experiment.

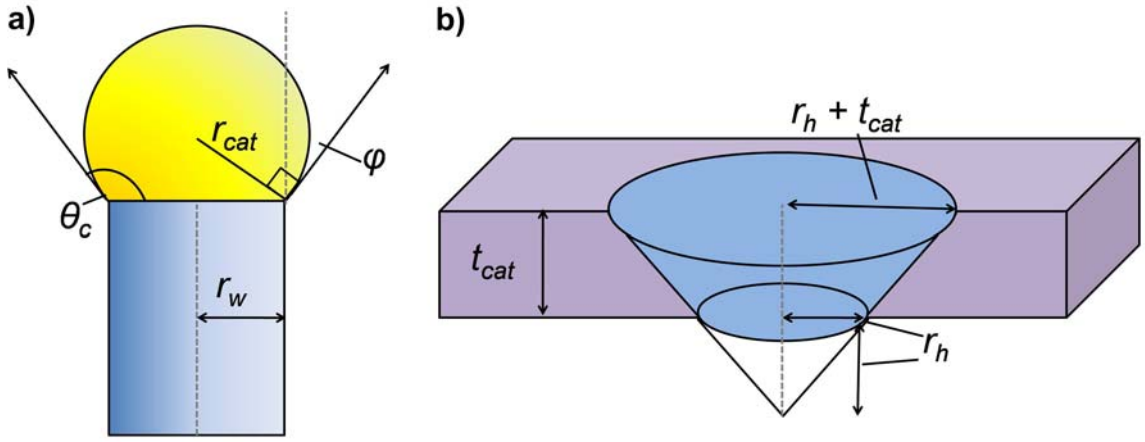

Figure 3.8. Schematics for relating wire size to catalyst deposition. **(a)** Schematic of a Si wire tip showing the relation between wire radius, r_w, catalyst tip radius, r_{cat}, and the contact angle between the catalyst metal and the Si(111) surface, θ_c, where $\theta_c = 90° + \varphi$. **(b)** Schematic of the truncated-cone-shaped hole that results from etching the oxide surface with buffered HF. The radius of any circle through the cone is equal to the hole radius at the bottom, r_h, plus the height of the circle from the bottom, so that a deposited catalyst plug has a top surface radius of $r_h + t_{cat}$ as long as it is not thicker than the oxide.

Table 3.1. VLS catalyst properties.

Catalyst	Au	Cu	Ni
θ_c (°)[105]	110	135	120
φ (°)	20	45	30
r_{cat}	$1.06r_w$	$1.41r_w$	$1.15r_w$
V_{cattip}	$1.20\pi r_w^3$	$3.55\pi r_w^3$	$1.73\pi r_w^3$
$C_{s,cat}$ (atoms cm^{-3})[123, 124]	~ 8 x 10^{15}	~ 3 x 10^{17}	~ 1 x 10^{17}
M_{cat} (g/mol)	196.97	63.55	58.69
ρ_{cat} (g/cm^3)	19.32	8.96	8.91

3.7.3 Hexagonally Packed, 3 – 4 μm Diameter Wire Arrays

Au was used to demonstrate the premise of growing larger diameter, more densely packed wires through the electrodeposition of catalyst metal. A Si(111) wafer (330 - 430 μm thick n-type Si, doped with Sb to a resistivity of 0.005 – 0.02 Ω-cm, International Wafer Service, Inc.) was heated at 1000 ºC under a flow of fully hydrated O_2 at 1 atm for 3.5 h, resulting in a thermal oxide surface layer of ~ 900 nm thickness as verified by ellipsometry. The wafer was photolithographically patterned with S1813 photoresist (Microchem) using a mask with circles of 5 μm diameter hexagonally packed with a pitch of 7 μm, followed by immersion for 10 min in buffered HF(aq) (Transene, Inc., 9% HF, 32% NH_4F) to remove the oxide in the holes formed by exposure of the photoresist (Figures 3.9a-c). The photoresist was subsequently removed with acetone.

Electrodeposition was then used to deposit the Au VLS catalyst into the holes in the oxide. The oxide was removed from the back surface of the Si by etching the back for > 10 min with buffered HF(aq), and care was taken during this step to avoid any contact of the HF(aq) with the front surface of the wafer. A piece of two-sided, conductive Cu tape was then attached to the back of the wafer, and the assembly was made into an electrode by connecting the other side of the Cu tape to a Cu wire that was sealed in a glass tube. Mounting wax was used to seal the tube and cover the wafer, so that only the patterned oxide on the front of the wafer was exposed. This electrode was then dipped in 10% (by volume) HF(aq) for 10 s to remove the native oxide at the bottom of the patterned holes. The electrode was rinsed thoroughly in H_2O and then immediately transferred to a Au electrodeposition bath (Orotemp 24 from Technic Inc.). Relatively low current densities (0.4 to 0.8 mA cm^{-2} of exposed wafer area between the Si working electrode and the Pt

gauze counter electrode) and Si wafers of high conductivity were required to electrodeposit uniform layers of Au selectively inside the oxide pattern (Figure 3.9d). The deposition was allowed to proceed galvanostatically until 0.2 – 0.4 C cm^{-2} of charge had been passed. The wafer, with metal catalyst deposits in the patterned holes in the oxide layer, was then recovered from the electrode by thoroughly dissolving the mounting wax in acetone. The patterned sample was then put into the CVD reactor, and Si wires were grown using the conditions described in Section 3.5.3 with 30 min of growth time.

The resulting Si wire array was significantly denser than the previously published array.[119] The earlier array, with 1.5 μm diameter wires in a square arrangement of 7 μm pitch, had a packing fraction of only ~ 4%, while the hexagonally packed arrays had wire diameters of 3 – 4 μm with a 7 μm pitch, resulting in packing fractions of ~ 17 – 30% (Figure 3.10). The fidelity was high for these electrodeposited arrays but became poor if wire diameters > 4 μm were attempted with this pattern and oxide thickness. After 30 min of growth, these wires were ~ 60 μm long. In the earlier square arrangement array, the wires were ~ 100 μm long after the same growth period. The slower growth of the larger diameter, more densely packed array under the same conditions suggests that the growth rate may have been limited by the flux of $SiCl_4$ to the sample. The successful fabrication of larger diameter wires of fairly high packing density using electrodeposition of the catalyst demonstrates that arrays of optimal geometry can be produced using a low-cost metal deposition technique.

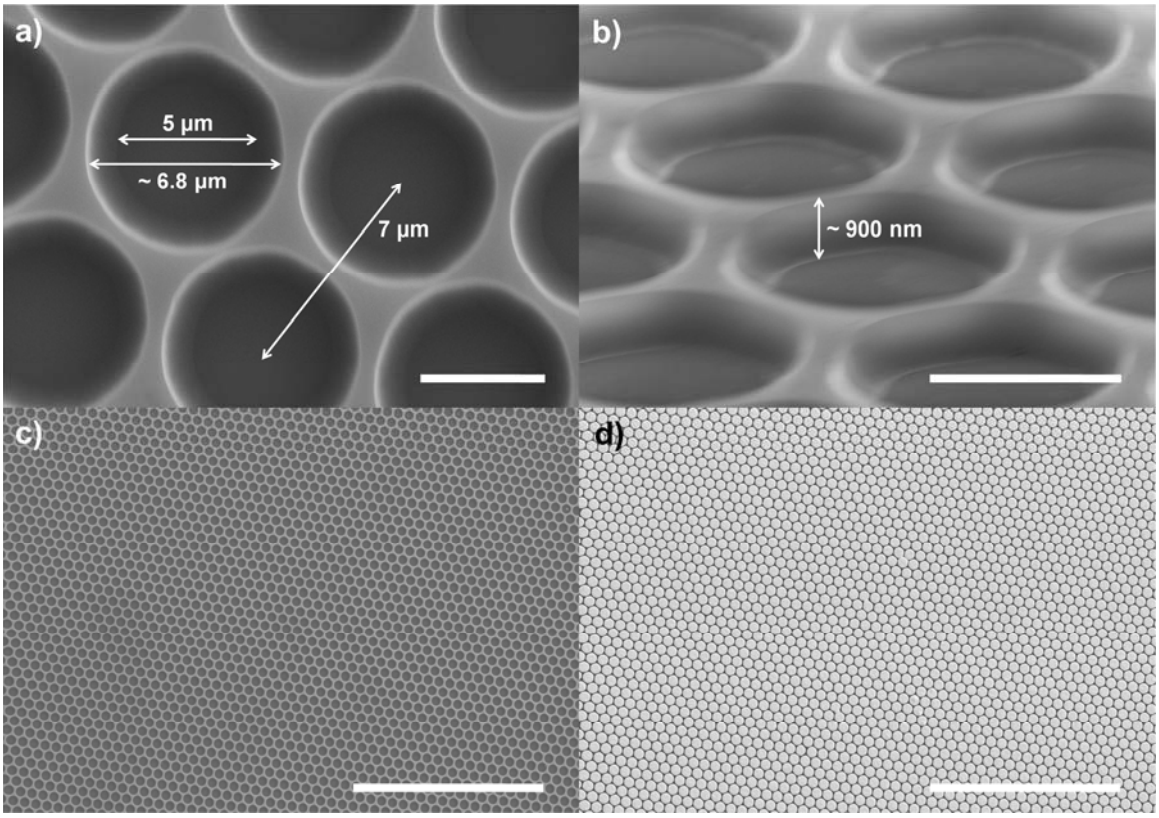

Figure 3.9. Oxide patterning and electrodeposition of a hexagonally packed array. **(a)** Top-down view and **(b)** tilted-view SEM images of a 5 µm hole diameter, 7 µm pitch pattern etched into a ~ 900 nm thick thermal oxide on Si(111). Scale bar for **(a,b)** is 4 µm. Top-down view SEM images of the hexagonally packed pattern **(c)** before and **(d)** after electrodeposition of Au catalyst. Scale bar for **(c,d)** is 100 µm.

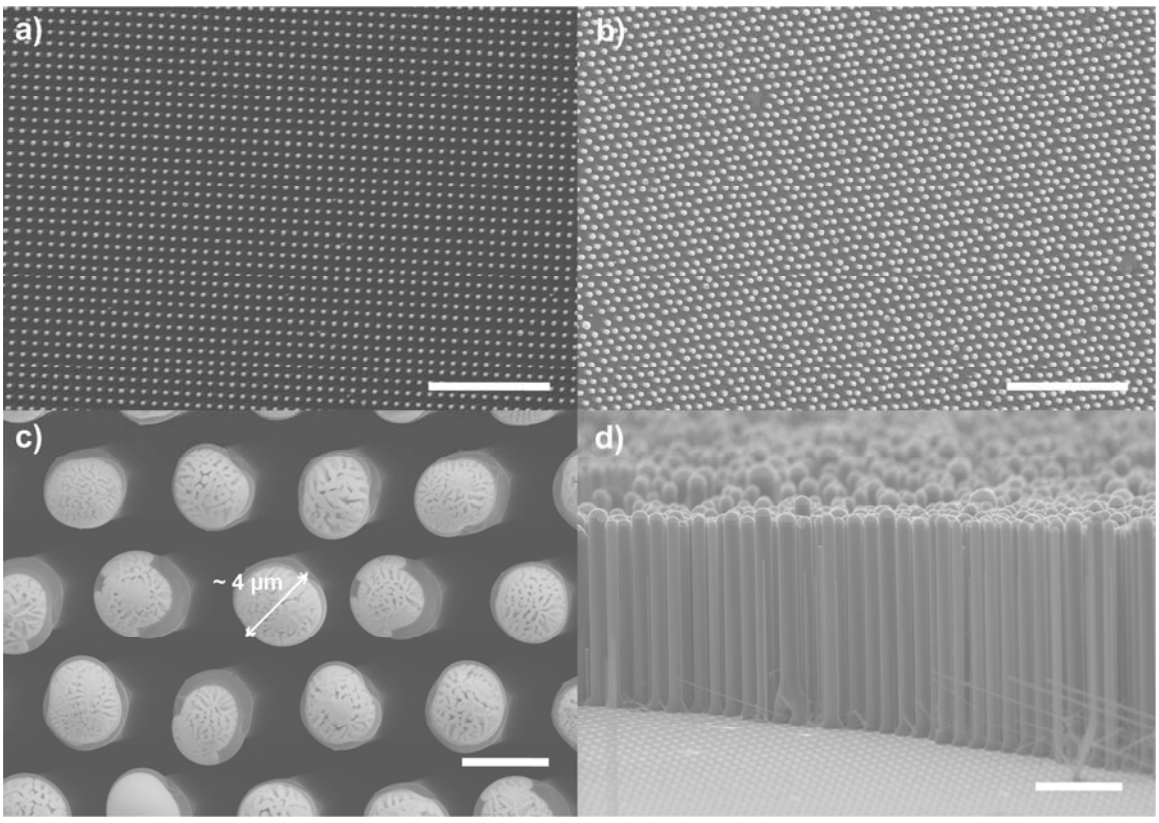

Figure 3.10. Hexagonally packed wire array grown from electrodeposited Au. Top-down view SEM images of **(a)** the original 3 µm diameter hole, 7 µm pitch, square packed wire array and **(b)** the 5 µm diameter hole, 7 µm pitch, hexagonally packed wire array. Scale bar in **(a,b)** is 50 µm. SEM images of the hexagonally packed array from the **(c)** top-down view, showing wires with diameters up to ~ 4 µm, and **(d)** tilted-view, showing wires ~ 60 µm long. Scale bar is 4 µm for **(c)** and 20 µm for **(d)**.

3.8 Conclusion

Si, as the predominant semiconductor of the photovoltaics industry and an indirect gap absorber easily limited by its minority-carrier diffusion length, is a logical material to be applied in the radial junction architecture. The vapor-liquid-solid mechanism is a convenient route to the fabrication of one-dimensional Si structures that, when guided by patterned catalysts, can produce highly uniform wire arrays of tunable dimensions.

Electrodeposition, rather than thermal evaporation, of catalyst allows larger diameter, more densely packed wire arrays to be produced while minimizing wasted metal. These techniques should permit the fabrication of uniform Si wire arrays of nearly any diameter, length, or spacing within the regime of interest, which makes possible the careful study of the solar energy-conversion properties of Si using radial junctions.

Chapter 4

Wire Array Transfer to Polymer Films and Substrate Reuse

4.1 Introduction

The VLS growth of Si structures provides a route to fabricate vertically aligned wires of highly uniform, tunable dimensions that can be studied to determine the optimal Si wire array geometry for solar energy conversion. The wires can be grown at high growth rates under atmospheric pressure using the inexpensive gas precursor $SiCl_4$.[25, 118, 119] High-quality wire arrays are attainable with the relatively abundant catalysts Cu or Ni. These metals can be selectively placed in the patterned oxide buffer layer on the substrate using electrodeposition to minimize catalyst waste. Together these advantages of the VLS growth process are encouraging for the prospect of using this scheme to fabricate low-cost Si wire array solar cells. However, the necessary inclusion of a pure, single-crystal Si wafer to grow highly uniform wire arrays detracts from the purpose of using radial junctions to make solar cells out of inexpensive materials.

Si wire array photovoltaics cannot afford to sacrifice a single-crystal substrate with the fabrication of every array if they are to eventually become economically competitive. To

address this issue, we have developed a scheme in which the wires are transferred to a low-cost film and the substrate is recycled to grow subsequent wire arrays (Figure 4.1). The array order is preserved in a durable, transparent polymer in a flexible, processible form. The expense of the Si substrate is amortized over numerous wire array growth cycles. The polymer-embedding procedure should be applicable in a roll-to-roll processing scheme, contributing to the scalability of wire array solar cell fabrication.

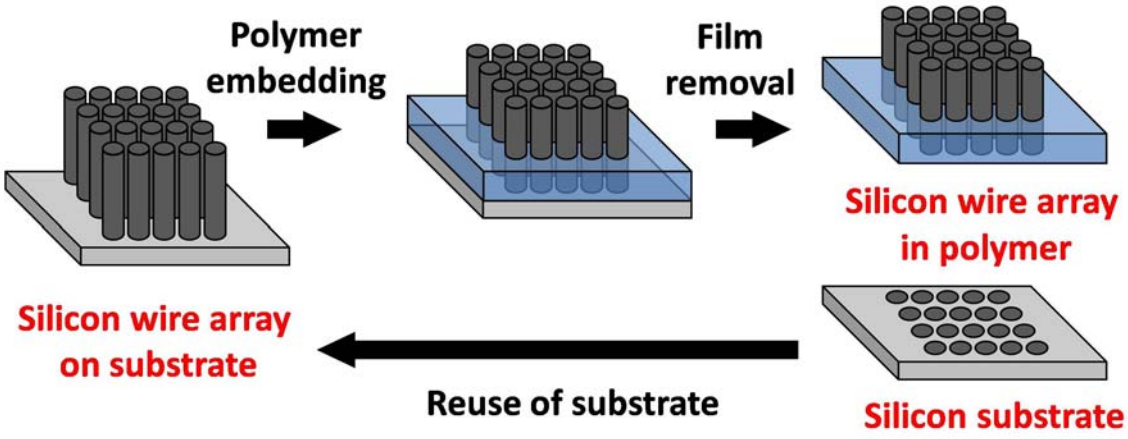

Figure 4.1. Schematic for Si wire array transfer and substrate reuse. The wire array is embedded in a low-cost, durable, transparent polymer and removed from the underlying substrate. The substrate, a single-crystal Si(111) wafer with a patterned thermal oxide surface, is recycled to grow additional Si wire arrays.

4.2 Wire Array Transfer to Polymer Films

4.2.1 Choice of Polymer and Deposition Method

The polymer to be used for wire array transfer must meet several criteria to successfully work in this application. It should be highly transparent to visible light at thicknesses of ~ 100 μm to prevent it from having a significant parasitic effect on the absorbance of the Si wires. The polymer should be able to conformally coat the wires and adhere to them

strongly enough to maintain their location and order when the film is removed from the substrate. It also needs to be structurally robust enough to hold together as a substrate-free film of < 100 μm.

Chlorinated polypropylene was the first polymer investigated for this application. Polypropylene (PP) is an inexpensive polymer commonly used in plastics that is highly transparent to visible light. Initial attempts to dissolve chlorinated PP in dichloromethane (DCM) and dropcast it onto Si wire arrays resulted in clumps of PP at the tops of the wires only. However, thin films of PP of approximately uniform thickness were conformally coated on Si wire arrays (Figure 4.2a) by dissolving 0.1 g of chlorinated PP (Aldrich) in 10 mL of DCM (99.9%, Aldrich) in a scintillation vial, placing the wire array in the solution with the wires facing upward, and allowing the solution to evaporate slowly over several hours. The resulting thin plastic/Si wire array film was mechanically removed from the substrate using a razor blade. The majority of the PP film area failed to hold the Si wires in place, causing the bottom of the polymer film to be covered in loose wires and to have periodic holes consistent with the wire size and pattern (Figure 4.2b). Considering that shear forces from the razor blade procedure may have dislodged the wires from the polymer film, a sonication approach to film removal was tried. However, sonication was not powerful enough to break the wires loose from the substrate when they were embedded in the PP film.

Poly(ethylene-co-vinyl acetate) (PEVA) was also used to make Si wire/polymer composite films. Dissolving PEVA (18% vinyl acetate, Aldrich) in DCM and allowing a slow evaporation as before, however, led to a highly cracked thin film of polymer on the

wire array. Conformal coating of the wires was achieved by heating PEVA (>190 ºC) on a sample until it liquefied and wicked into the wire array (Figure 4.2c). Removal of these films from the substrate yielded a PEVA/Si wire composite chip that maintained the wire placement and pattern fidelity in the polymer (Figure 4.2d). With this deposition method for PEVA, however, it was difficult to control the polymer thickness over large areas, and upon cooling, the polymer was hard and brittle. Using a razor blade to remove the PEVA layer resulted in many chips of polymer/wire material rather than a single continuous film.

These issues were overcome by using polydimethylsiloxane (PDMS) as the polymer layer. PDMS has been widely studied in microfluidics applications[125-128] and has been observed to be a durable material that is quite chemically stable.[129] PDMS is also highly transparent in the UV/visible regions of the solar spectrum.[128] The PDMS elastomer base and curing agent (Sylgard 184, Dow Corning) were mixed in a 10:1 w/w ratio and stirred thoroughly before spin coating onto a Si wire array at 3000 rpm for 1 min. The wafer was then heated at 120 ºC for > 2 h to cure the PDMS. PDMS/wire composite films were carefully removed from the underlying Si growth substrate using a razor blade. The PDMS conformally covered the wires, leaving only their bases exposed from the peeled layer (Figure 4.2e). Despite the high flexibility of the PDMS film, the wires were always observed to maintain their position within the polymer matrix (Figure 4.2f), due to the large adhesive force between PDMS and SiO_2 surfaces.[130]

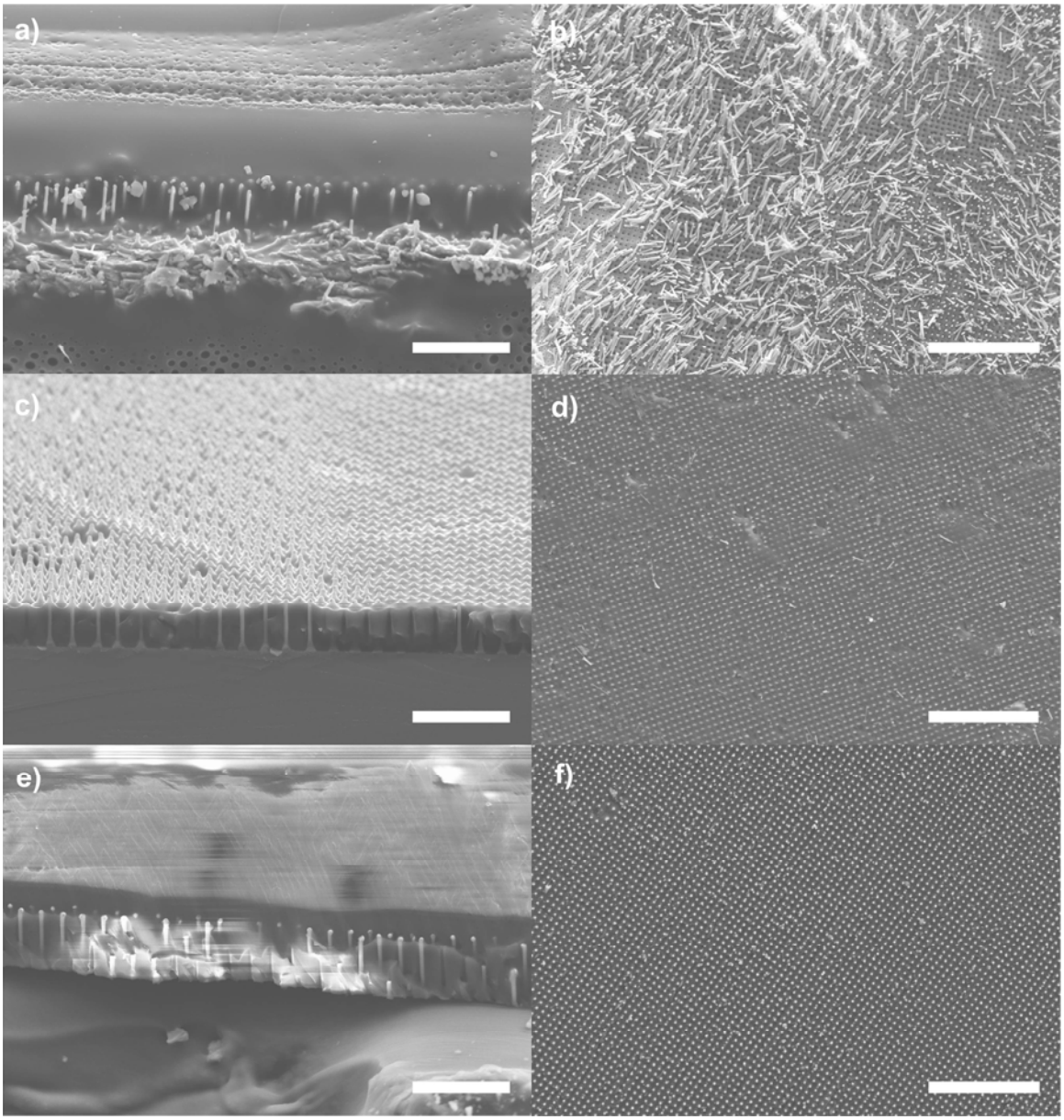

Figure 4.2. Wire array transfer to different polymer films. SEM images of Si wire arrays infiltrated with **(a,b)** chlorinated polypropylene, **(c,d)** polyethylene, 18% vinyl acetate, and **(e,f)** polydimethylsiloxane. **(a,c,e)** Cross-sectional view of the arrays and **(b,d,f)** top-down view of the bottom of the films after peeling from the substrate with a razor blade. Scale bar for **(a,c,e)** is 40 μm and for **(b,d,f)** is 100 μm.

4.2.2 Peeled, PDMS-Embedded Si Wire Arrays[2]

The PDMS curing and peeling process produced flexible, polymer-supported arrays of crystalline Si wires embedded within a transparent, mechanically and chemically robust, film (Figure 4.3a).[129] Si wire arrays with areas > 1 cm^2 were transferred to a single polymer sheet (Figure 4.3b). The area of the wire-embedded film was limited only by the size of the initial array, which in turn was limited by the size of the reactor tube used to fabricate the Si wire arrays. Cross-sectional SEM images of the PDMS/Si wire array composite films revealed intimate contact between the wires and the polymer (Figure 4.4a). The as-removed films could be bent or rolled into cylinders having diameters as small as several millimeters without damaging or dislodging the embedded Si wires (Figure 4.4d). The polymer/wire composite also maintained the spacing, cubic unit cell, and orientation of the wires prior to casting. Diffraction of visible light was used to verify the embedded wire spacing and periodicity in the PDMS films. A 670 nm diode laser normally incident to a flat sample surface produced a cubic array of diffraction spots (Figure 4.3c) with a diffraction angle indicating an array spacing of 6.9 ± 0.2 μm, in agreement with the photolithography mask's square arrangement with a center-to-center pitch of 7 μm. Up to 4 orders of diffraction were observed even after mechanical deformation of the films. The wire array/polymer composites were highly light absorbing and/or scattering at the angles shown (Figures 4.3a and 4.3b), despite the high transparency of PDMS in the visible region of the solar spectrum and the top-down density of Si wires being only ~ 4% of the projected area of the film. This finding is in

[2] Reprinted with permission from Plass, K. E., Filler, M. A., Spurgeon, J. M., Kayes, B. M., Maldonado, S., Brunschwig, B. S., Atwater, H. A. and Lewis, N. S., *Adv. Mater.* **21**, 3, 325 – 328 (2009). Copyright 2009 Wiley-VCH GmbH & Co. KGaA.

agreement with the reported enhanced light absorption in wire arrays[55, 122, 131] and suggests that these composite films may have direct application in solar energy-conversion devices.met

The thickness of the PDMS film determined both the structural integrity of the composite and the extent to which the wires were exposed. PDMS/Si wire sheets were prepared in which one (Figure 4.4a) or both (Figures 4.4b-d) ends of the Si wires were exposed, allowing for subsequent formation of electrical contacts to the Si wires. Thicker layers with only the bases of the Si wires exposed from the polymer were fabricated as described above (see Section 4.2.1). To produce thinner polymer films, a low-boiling-point siloxane was added to the PDMS solution that was used to embed the wires. Hexamethylcyclotrisiloxane (HMCTS, 98%, Alfa Aesar) was dissolved in dichloromethane (until saturation, ~ 4 g HMCTS/5 mL DCM), then mixed with Sylgard 184 polydimethylsiloxane (Dow Corning) in a 4.4: 1.0: 0.1 (HMCTS: PDMS base: PDMS curing agent) w/w ratio, not including the DCM weight. This mixture was spin coated onto the wire arrays at 1000 rpm for 1 min, then heated at 150 °C for 30 min. The HMCTS evaporated rapidly at this temperature without cross-linking into the PDMS, which allowed the polymer to contract below the tips of the wires and cure conformally at the base. This left a 10 – 20 μm thick layer of PDMS at the bottoms of the Si wires, leaving the majority of the wire length exposed (Figures 4.4b-d). The wire arrays in such films were electrically conductive from top to bottom, but exhibited immeasurably high resistances laterally. This observation indicated that the embedded Si wires extended

through the polymer film and were also electrically isolated from each other by the polymer matrix.

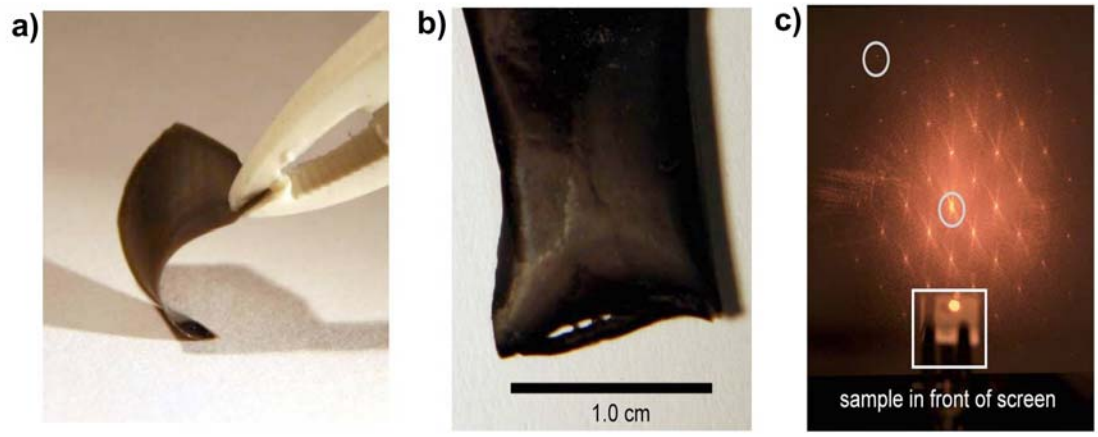

Figure 4.3. Flexible, PDMS-embedded Si wire array films. (a) Demonstration of the flexibility of a PDMS-embedded Si wire array (held by tweezers) and of the **(b)** large area (> 1 cm^2) and nearly black color achievable in these films. **(c)** Optical diffraction pattern resulting from transmitted laser light, indicating the long-range order of the array. The center (zero-order diffraction) and outer (4^{th}-order diffraction) spots are circled (image credit: K.E. Plass).

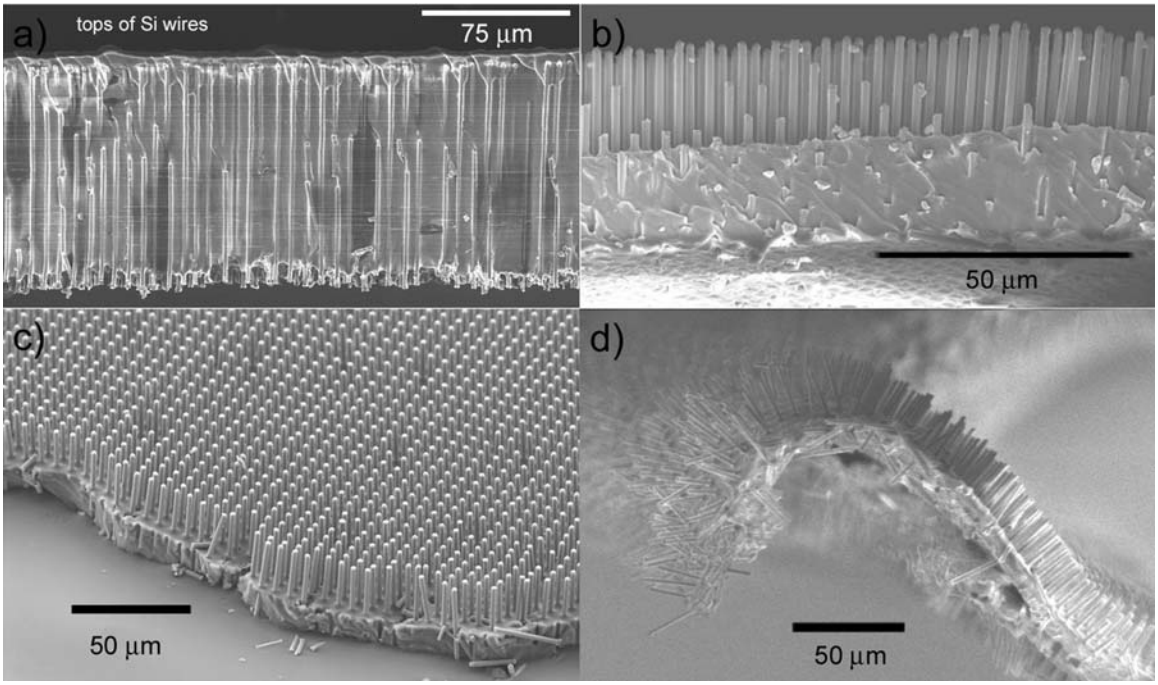

Figure 4.4. SEM images of cross-sections of embedded Si wire arrays of two different polymer thicknesses. **(a)** A composite film fabricated without a low-boiling point siloxane additive. Upon removal from the growth substrate, wires were exposed only at the bottom of the film. Note the conformal filling of the gaps between wires. **(b-d)** The thinner composite film fabricated with the addition of a low-boiling point siloxane had a significant fraction of the wire length emerging from the polymer while the array pattern was maintained. **(b)** The bottom of the film can be seen, demonstrating that the rods passed through the polymer. **(c)** The array order from the top of the film is visible. **(d)** The films remained flexible even while containing ordered arrays of single-crystalline wires.

4.2.3 Polymer-Embedded Wire Array Densification

The ability to transfer wire arrays from their rigid epitaxial growth substrate into a flexible organic layer opens new avenues for manipulating the array geometry. For example, chemically or thermally shrinking the polymer matrix can increase the wire density without requiring short nearest-neighbor distances during the initial growth step and represents a means of further improving the light absorption/trapping of such films. Densification of the wire array in a polymer film is therefore a potential way to increase the packing density of the wires beyond the limits imposed by the wet chemical etch patterning of the thermal oxide buffer layer during array fabrication (see Section 3.7.2).

Thermally shrinking the composite film by utilizing a polymer similar to that used in heat-shrink tubing (e.g., polyethylene, polypropylene, etc.) would seem a straightforward route to densify peeled wire array layers. However, heat-shrink plastics are typically prepared by irradiating the polymer to induce cross-linking of the chains, heating and stretching it, then slowly cooling the plastic so that it retains an extended, non-equilibrium shape. Upon annealing past a critical temperature, the plastic will relax back to its smaller state.[132] It would be very challenging to cast these polymers on a wire array and peel them in the non-equilibrium state, which would be necessary to gain the benefit of densification from this type of thermal shrinkage.

Instead, an approach was investigated in which a volume-filling molecule was added to a cross-linked polymer during the wire array coating, then removed by a liquid extraction step after peeling the wire/polymer composite film. In this process, 5 g hexamethylcyclotrisiloxane (HMCTS, 98%, Alfa Aesar) was mixed with 1 g Sylgard 184 PDMS (Dow Corning), then heated at 150 ºC and stirred to liquefy the HMCTS. A

substrate-attached wire array was immersed in a beaker full of this siloxane mixture and heated at 150 ºC for ~ 30 min. The wire array sample was elevated on a metal stand ~ 1 cm from the bottom of the beaker to prevent bubbles from curing in the wire array. Although it boils at this temperature, the presence of excess HMCTS ensured that much of it remained in the beaker for a sufficient length of time to be incorporated into the cured PDMS film. The wire array sample was then cut from the cured PDMS block and peeled from the substrate using a razor blade. For the liquid extraction of the HMCTS, the polymer-embedded film was immersed in dichloromethane for > 10 h, then immersed in acetone for > 3 h, then immersed in water for > 1 h, and finally allowed to dry under air for > 2 h. An example wire/polymer composite film made from this process weighed 0.0289 g before the liquid extraction and 0.0135 g afterward.

This procedure successfully led to the densification of the Si wire array through a volume contraction of the peeled PDMS film. SEM images of the bottom of the shrunken film (Figures 4.5b and 4.5d) show wires packed noticeably denser than either the wire stubs left behind on the wafer after peeling (Figure 4.5a) or the wire array before polymer embedding (Figure 4.5c). The projected area of the Si wire array was reduced by as much as 70% from the densification process (Figure 4.5e).

Although this is an encouraging step towards increasing the packing density of wire arrays through post-growth processing, this method has key shortcomings that need to be improved for densification to be included in a final wire array solar cell fabrication scheme. Not all areas of the polymer film appeared to densify equally, with some locations maintaining approximately the same wire-to-wire pitch as before polymer embedding. Parts of the film have microscopic gaps in the PDMS layer surrounding the

wires rather than a single continuous polymer sheet (Figure 4.5f). Finally, the polymer deposition method used for densification does not allow control over the thickness of the film on the micron scale required to be able to expose both ends of the Si wires for contacting. Hexaphenylcyclotrisiloxane (Gelest, Inc.), a cyclic siloxane molecule similar to HMCTS that should not cross-link with PDMS (but with a higher boiling point, ~ 300 ºC), may allow thinner films to be deposited and densified. Initial attempts to use this molecule, however, have so far met with difficulty in getting it to mix well with PDMS.

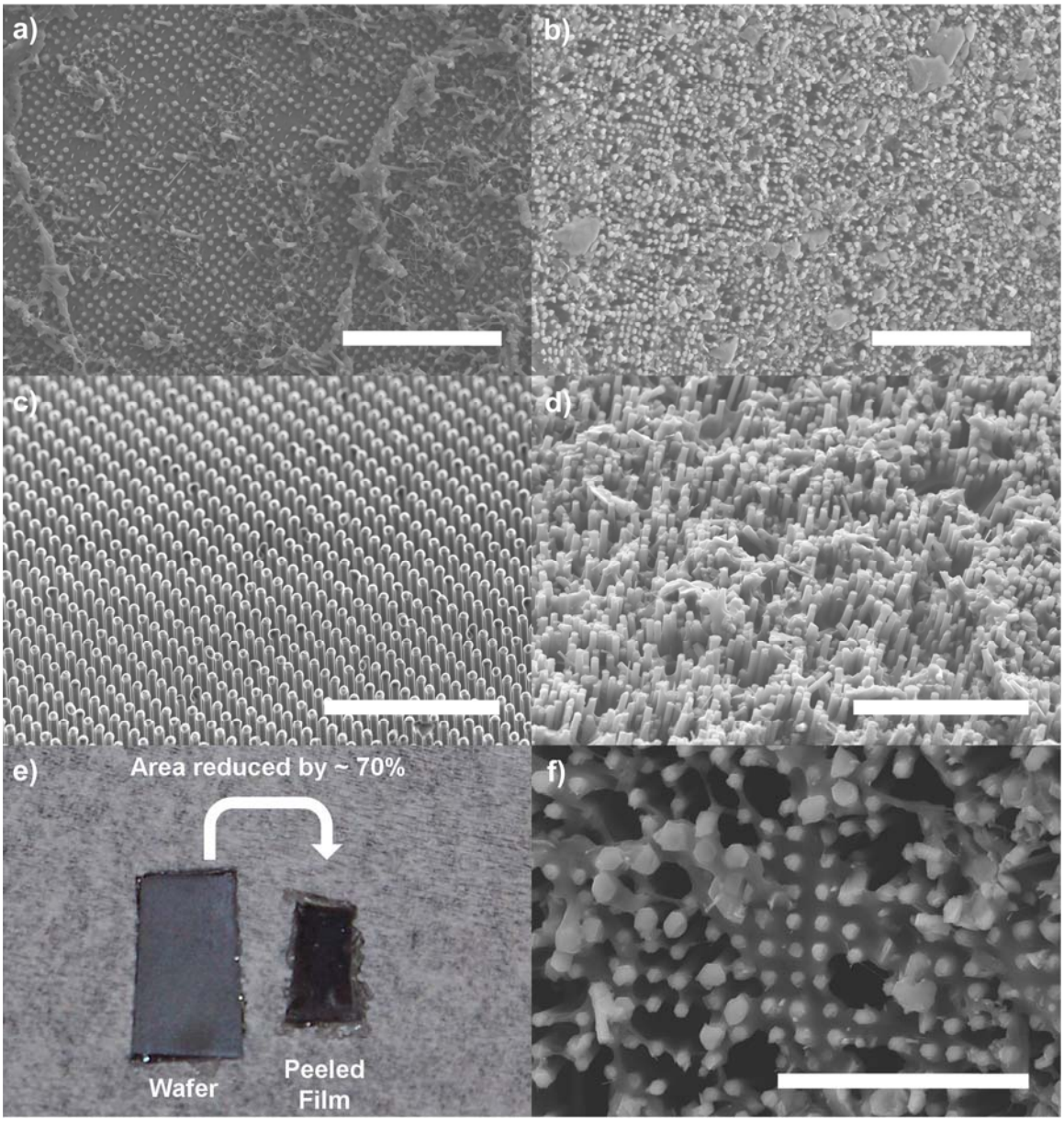

Figure 4.5. Densification of wire arrays by volume contraction of PDMS films. (a,b) Top-down view SEM images of **(a)** the growth substrate surface after polymer film removal and **(b)** the bottom of the PDMS/wire composite film after peeling from the substrate and densification. **(c,d)** Tilted-view SEM images of **(c)** a Si wire array before transfer to a polymer film and **(d)** the bottom of the PDMS/wire composite film after peeling from the substrate and densification. **(e)** After densification by liquid extraction of the volume-filling species, the projected area of the array was reduced by up to ~ 70%. **(f)** SEM image of the bottom of a peeled film after the densification procedure displaying an area where the wire array did not significantly densify and the PDMS layer was no longer continuous. Scale bar is 100 μm for **(a,b)** and 40 μm for **(b,c,f)**.

4.3 Reuse of the Substrate to Grow Multiple Si Wire Arrays[3]

4.3.1 Wire Regrowth by Regeneration of the Oxide Buffer Template

To minimize the expense associated with using a single-crystal Si wafer, a method was developed to recycle the substrate repeatedly for the production of multiple high-quality Si wire arrays. The first-generation Si wire arrays were fabricated by epitaxial VLS growth on a Si wafer by the procedure described in Section 3.5.3.[119] Here, a highly doped Si(111) wafer (330 - 430 μm thick n-type Si, doped with Sb to a resistivity of 0.005 – 0.02 Ω-cm, International Wafer Service, Inc.) with 300 nm of a thermally grown silicon oxide was used as the growth substrate. 300 nm of Au was thermally evaporated onto the photolithographic pattern, resulting in a square array of 3 μm diameter Au islands, having a center-to-center pitch of 7 μm, separated by the SiO_2 layer. Using $SiCl_4$ (see Section 3.5.3), highly uniform, vertically aligned, crystalline Si wires were fabricated over areas > 1 cm^2 (Figure 4.6a). The wire array dimensions and pore spacing used in this work were chosen based on an available lithography mask, to facilitate comparison to previous results.[119] Other wire diameters and center-to-center pitches could be produced by the use of other masks, to the limit of the resolution and pore-size fidelity that can be accommodated by the development and etching steps. The optimal catalyst volume is readily calculated for a given wire radius from the surface tension of the Au meniscus on the growing Si wire (see Section 3.7.2),[100, 105] and requires a SiO_2 buffer layer with a thickness approximately equal to that of the deposited metal.

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[3] Reprinted with permission from Spurgeon, J. M., Plass, K. E., Kayes, B. M., Brunschwig, B. S., Atwater, H. A. and Lewis, N. S., *Appl. Phys. Lett.* **93**, 3, 032112-1-3 (2008). Copyright 2008 American Institute of Physics.

A 10:1 w/w ratio of polydimethylsiloxane (PDMS) and a curing agent (Sylgard 184, Dow Corning) was applied to the top of the wire array by spin coating at 3000 rpm. The sample was then heated for 2 h at 120 ºC to cure and solidify the polymer. Scanning electron microscopy (SEM) images confirmed that the PDMS fully infiltrated the Si wire array. The polymer film and the embedded Si wires were then removed by scraping the wafer surface with a razor blade. This transfer approach preserved the pattern fidelity and vertical alignment of the wires within the polymer matrix (Figure 4.6b).

After the removal of the PDMS layer, residual stubs of broken Si wires, 2 μm long or less, along with some polymer residue, were observable at the wafer surface (Figure 4.6c). To enable wire regrowth, the wafers were immersed for 90 s in 4.5 M KOH(aq) at 80 ºC with stirring.[96] At elevated temperatures, KOH(aq) etches the Si(100) and (110) planes approximately two orders of magnitude faster than it etches the Si(111) plane. Furthermore, the etch rate for Si is significantly faster than that for SiO_2.[96] The KOH(aq) thus selectively etched the Si stubs as well as the polymer residue. After etching, the original oxide hole pattern remained, with the Si(111) substrate exposed at the bottom of each hole (Figure 4.6d). Because the KOH(aq) etch does eventually remove the oxide, however, this step must be kept as brief as possible, and it was determined empirically that 90 s was generally sufficient to remove the Si wire stubs and the PDMS residue.

Electrodeposition was then used to redeposit the VLS catalyst into the holes in the oxide. The deposition of Au catalyst was conducted by forming electrodes and using them in an electrodeposition bath as described in Section 3.7.3. Relatively low current densities (0.4 to 0.8 mA cm^{-2} of exposed wafer area between the Si working electrode and the Pt gauze counter electrode) and Si wafers of high conductivity were required to

electrodeposit uniform layers of Au selectively inside the oxide pattern (Figure 4.6e). The deposition was allowed to proceed galvanostatically until 0.12 C cm^{-2} of charge had been passed, yielding Au catalyst arrays of 3 μm diameter and approximately 300 nm thickness over areas > 1 cm^2. With sufficiently deep pores, no limit has yet been observed for the thickness of Au that can be homogeneously deposited by the electroplating method. The wafer, with metal catalyst deposits in the patterned holes in the oxide layer, was then recovered from the electrode.

This substrate was placed back into the reactor for VLS-catalyzed wire growth, under the same conditions used to grow the first-generation Si wire arrays on the Si(111) substrate, including the 20 min anneal step. The regrown Si wires were between 70 and 100 μm long, with the wires in any single growth run of a uniform height distribution. The entire process was repeated to fabricate a third and fourth generation of wires. No appreciable differences in wire length, diameter, vertical orientation, or morphology were detected between growth generations (Figure 4.6f).

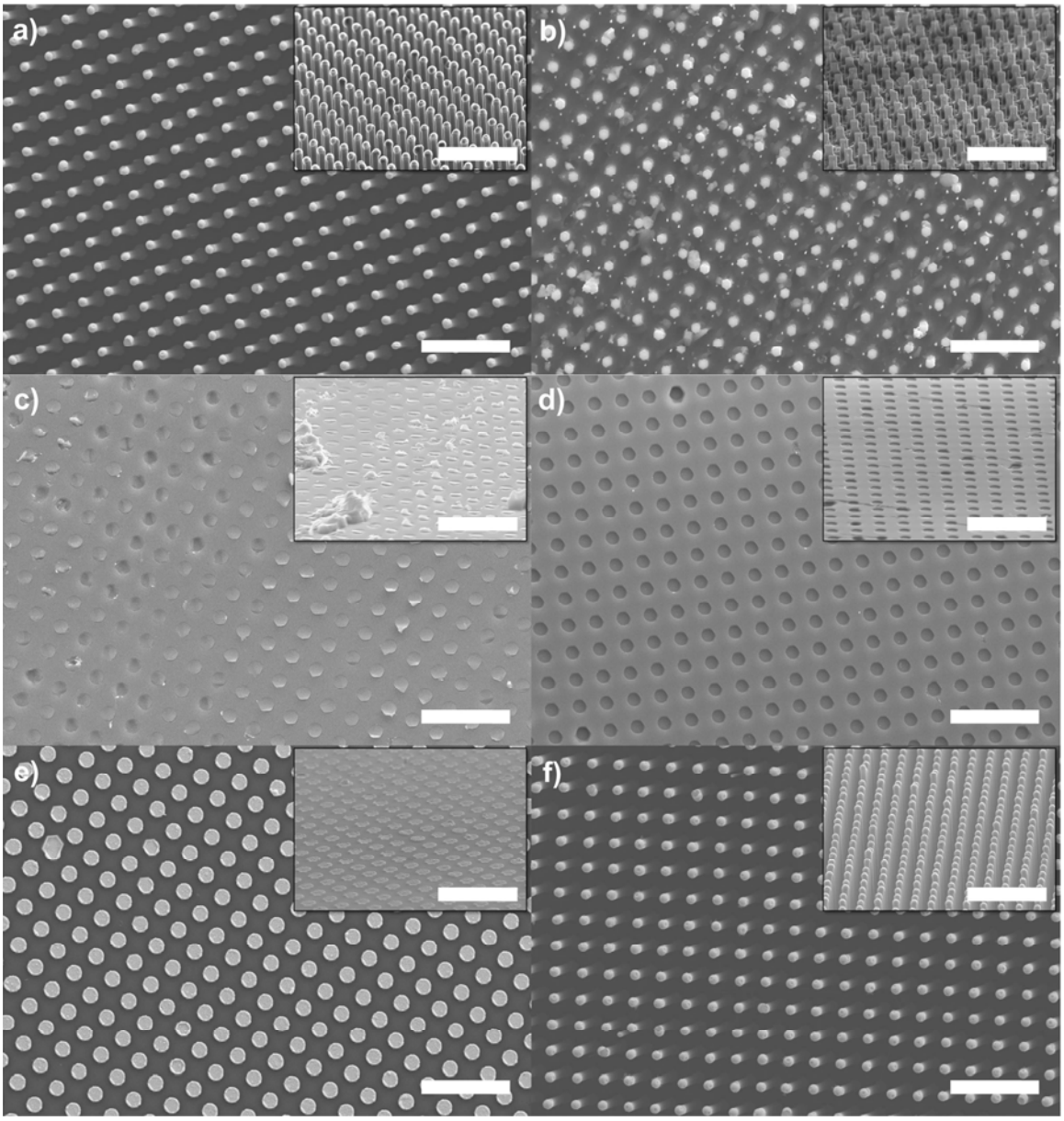

Figure 4.6. The wire array regrowth process. Top-down and 70º tilted-view (insets) SEM images. **(a)** The first-generation wire array was **(b)** peeled in PDMS, leaving behind **(c)** a wafer surface with wire stubs and polymer residue. **(d)** The oxide pattern was recovered with a KOH(aq) etch, **(e)** Au catalyst was electrodeposited into the holes, and **(f)** a new wire array was regrown from the wafer. The scale bar is 20 μm in all images.

4.3.2 Defect Accumulation in Subsequent Wire Array Generations

Defects, defined as a Si wire missing from the pattern, were evaluated using imaging software surveys of top-down SEM views of the wire arrays. Because every defect in the surface pattern was transferred to succeeding generations, the success of subsequent growths depended directly on the quality of the initial array. The oxide template served the crucial role of preserving the pattern fidelity by preventing the catalyst metal from migrating across the wafer surface during the growth reaction.[119] Second-generation wire arrays were nearly defect-free (Figure 4.6f). However, damage to the oxide pattern, caused by the formation of HCl in the reactor,[106] and undercutting during the KOH etch, was observed to introduce defects in the wire array. The accumulation of defects became more prominent, although still fairly modest, in third- and fourth-generation arrays (Figure 4.7 and Table 4.1). In the fourth-generation arrays, the number of defects approached 10% of the initial wire density. With optimization of the reaction process, it is likely that the density of defects could be reduced, so that several more generations of useful wire arrays could be produced with the same oxide pattern. The use of ethylenediamine pyrocatechol instead of KOH ought to further improve the selectivity of etching Si relative to SiO_2.[133]

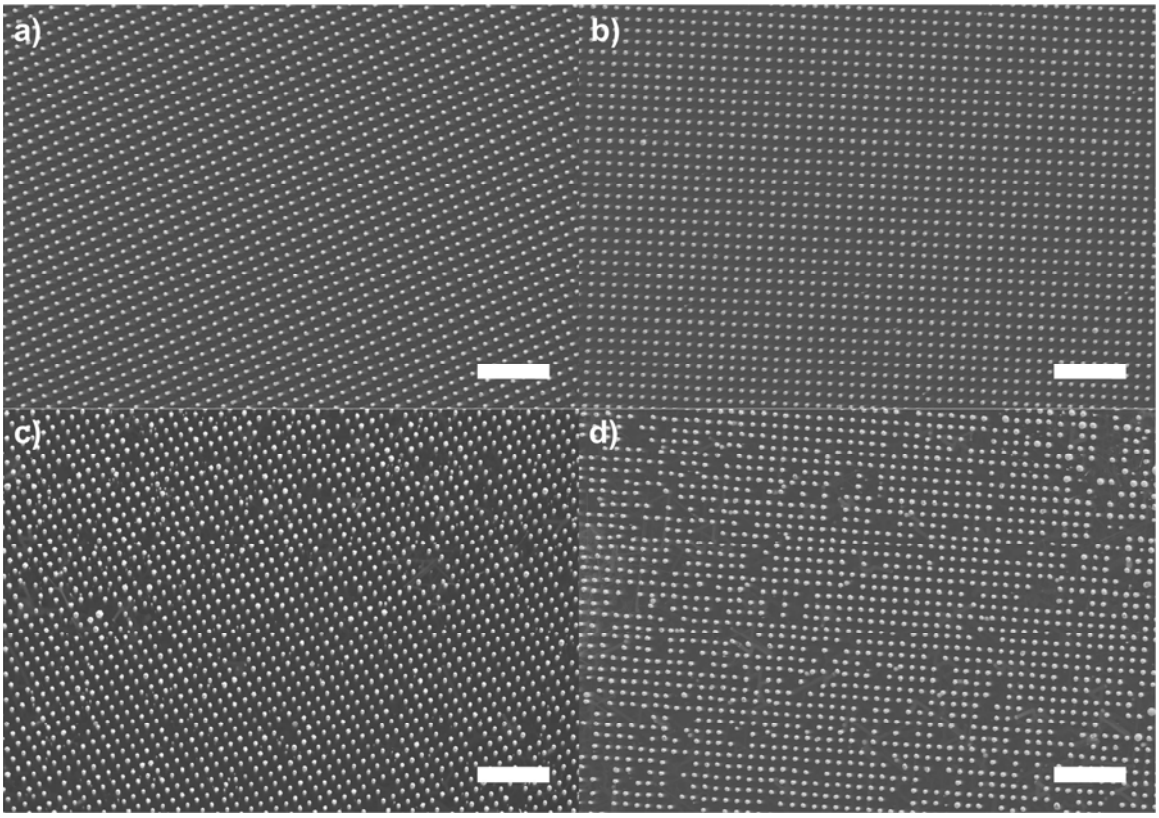

Figure 4.7. Accumulation of defects in succeeding wire array generations. Top-down SEM images for **(a)** first, **(b)** second, **(c)** third, and **(d)** fourth generation Si wire arrays, showing increasing defect density with successive generations of wire growth using a single oxide pattern on the substrate. The scale bar in each image is 40 μm.

Table 4.1. Average defect density within each generation of arrays.[a]

Wire Array Generation	Defect Density (cm^{-2})	Defect Percentage (%)
First	$(7.5 \pm 5.0) \times 10^2$	0.04 ± 0.02
Second	$(2.5 \pm 1.1) \times 10^4$	1.2 ± 0.5
Third	$(1.4 \pm 0.7) \times 10^5$	6.6 ± 3.4
Fourth	$(2.2 \pm 0.8) \times 10^5$	10.0 ± 3.4

[a] The data were collected using five top-down view SEM images of each generation. The averages were weighted by the area surveyed within each image.

4.3.3 Closing the Reuse Cycle by Growth of a New Thermal Oxide

Wire regrowth on a single Si(111) substrate was further extended by subjecting cycled wafers to mechanical polishing, which reduced their thickness by 10 to 20 μm, followed by thermal oxidation. To simulate rapid and inexpensive processing, the wafers were intentionally polished in a cursory manner. Because restoration of the patterned oxide overlayer required oxidation and then etching of the Si wafer, some degree of surface roughness should be tolerable. The polished Si wafers were thermally oxidized in a tube furnace under a fully hydrated atmosphere of industrial grade air at 900 ºC for 8 h, resulting in a 300 – 400 nm thick surface oxide. Even with an imperfect starting surface, VLS-catalyzed wire growth yielded a vertically aligned Si wire array of comparable quality to that of the first-generation Si wire array (Figure 4.8). Furthermore, the use of a more precise industrial polishing technique such as chemomechanical polishing[96] or electropolishing[134] should significantly reduce the amount of silicon lost in this process step.

Even without further improvements, if four generations of arrays can be grown from each oxide template and only 10 μm of wafer thickness is lost in each polishing step, a single 400 μm thick wafer would be capable of producing 160 Si wire arrays (fewer, if the wafer thinness limits its manipulation). Reasonable expectations for optimization (i.e., five generations per oxide layer, and 2 μm of Si removed per polishing step) imply that the same thickness of Si substrate should be capable of producing 1000 or more Si wire arrays. Furthermore, the VLS growth catalyst can be replaced by Ni or Cu to produce Si wire arrays of nominally equivalent structure[119] that ought to have superior electronic properties relative to those produced from the deep-trap Au VLS catalyst.

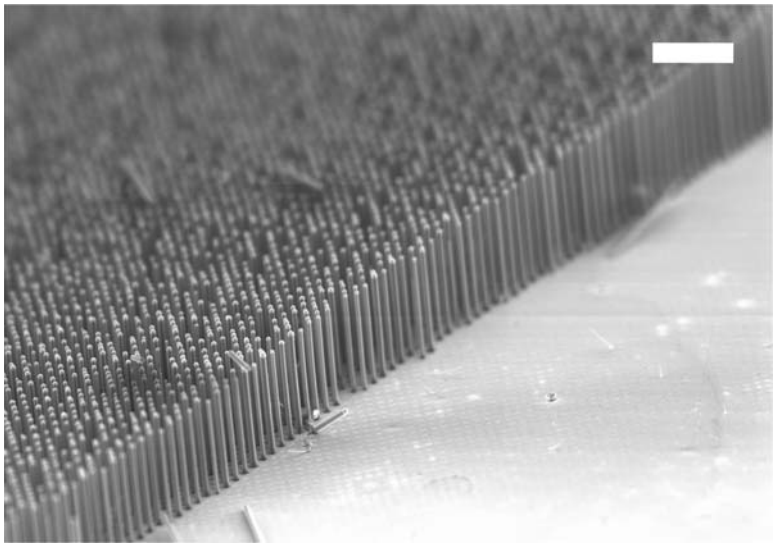

Figure 4.8. Growth after formation of a new thermal oxide layer. Tilted-view SEM image of a Si wire array grown from a Si(111) wafer that had been mechanically polished and then thermally oxidized. The scale bar is 40 μm.

4.4 Conclusion

The ability to transfer single-crystal wires in highly structured arrays to polymer films and recycle the growth substrate repeatedly is significant for minimizing the expense of high-quality Si wire array fabrication. Given the proven low cost of chlorosilane-based CVD processes,[135, 136] the approach described herein has the potential to afford a scalably manufacturable method for the production of large areas of oriented, patterned Si wire arrays for use in solar cells, batteries, photonics, and a variety of other applications. With our technique, solar cell absorber materials with the potential to achieve high efficiency can now be prepared by high-temperature processing and then transformed into a flexible,

processible form. New avenues of research into the optical, chemical, and mechanical properties of these composites are now available. Increases in the light absorption of the film can be pursued by shrinking the polymer matrix to increase the packing density of the wires beyond the templated epitaxial growth limits. The availability of large area, freestanding Si wire array films enables the optoelectronic and electrochemical properties of VLS-grown wire arrays and the substrate to be deconvoluted. Ultimately, we envision the inclusion of such wire array structures in a variety of electronic and photonic applications, in which ordered, extended three-dimensional structures of nanoscale devices are desired on the macroscale.

Chapter 5

Energy-Conversion Properties of Substrate-Attached vs. Freestanding Polymer-Supported Si Wire Array Photoelectrodes

5.1 Introduction

While current silicon solar cells require ultrahigh purity silicon, device physics modeling shows that silicon wires with radial junctions can achieve high energy-conversion efficiencies using lower purity material that has a low ratio of its minority-carrier collection length to its optical absorption depth.[33, 34] To date, however, device efficiencies for radial junction Si photovoltaics fabricated using potentially inexpensive techniques, such as the vapor-liquid-solid (VLS) growth process,[42] have been low. Single-wire Si cells grown this way have demonstrated efficiencies up to 3.4% with a low open-circuit voltage (V_{oc}) of 260 mV,[137] while modeling on a Si wire predicts efficiencies over 17% and V_{oc} ~ 600 mV based on measured diffusion lengths.[34] Several groups have also studied solar cells using an array of Si wires.[138-142] Top-down approaches such as etching wire arrays from a high-quality, single-crystal wafer have produced efficiencies

around 0.5% and V_{oc} of 290 mV,[139] while the more economically relevant scenario of using bottom-up VLS-grown Si wire arrays has so far been limited to efficiencies of ~ 0.1% and V_{oc} < 390 mV.[141, 142] These reports, while promising, leave much room for improvement.

The best Si wire arrays, those with the most controllable and uniform dimensions and best vertical alignment, have used single-crystal growth substrates.[106, 119, 143] Because VLS-grown Si wires proceed in the <111> direction,[42] using a Si(111) substrate promotes vertical orientation of the array. However, the benefit of using a wire array is undermined unless there is a way of reusing the expensive Si substrate. We have developed a technique to transfer the wire array into a film of polydimethylsiloxane (PDMS), a low-cost, transparent, flexible polymer, with both ends of the wires exposed for contacts,[144] and a scheme to recycle the growth substrate repeatedly so that it is a minor expense in the overall fabrication process (see Chapter 4).[145] Proving that these flexible, inorganic Si wire/polymer composite films can function as efficient photoelectrodes is an important step towards the production of a scalable, affordable wire array solar cell.

The VLS-grown Si wire array electrodes in liquid-junction photoelectrochemical cells reported herein yielded higher external quantum efficiencies and open-circuit voltages than previously reported wire array cells.[138-142] Substrate-free, polymer-supported Si wire array photoelectrodes exhibited current-potential behavior similar to that of the wires epitaxially attached to the growth substrate. Furthermore, the quantum efficiency of the wire arrays as a function of wavelength and angle of incidence indicated that the devices

produced more photocurrent than expected based solely on their geometric packing fraction.

5.2 Si Wire Array Photoelectrodes

5.2.1 Wire Array Properties

Figures 5.1a and 5.1b show representative scanning electron microscope (SEM) images of substrate-attached and peeled, polymer-supported Si wire arrays, respectively. The wires were grown by the vapor-liquid-solid (VLS) method from a Cu catalyst that was deposited in lithographically defined holes in a Si oxide buffer layer on the surface of a Si growth substrate.[119] Cu was chosen instead of the more commonly used Au as the growth catalyst, due to the higher abundance of Cu in the Earth's crust as well as the less deleterious effect of Cu as an impurity in p-Si based solar cells.[97] An etch was used to remove the Cu catalyst tips from the wires prior to their use as photoelectrodes (see Section 5.2.2). Consistently, > 10 μm minority-carrier collection lengths have been measured on individual Si microwires grown by this method.[34, 121] The ~ 1.5 μm radius of the Si microwires should thus enable efficient radial minority-carrier collection while the 100 μm length of the wires is comparable to the necessary planar thickness for efficient absorption of incident photons with energies greater than the 1.1 eV indirect band gap of Si. The wire arrays were partially embedded in polydimethylsiloxane (PDMS) and peeled off the growth substrate, yielding a flexible, processible material that consisted of ordered arrays of crystalline Si wires with their bases embedded in, but most

of their length projecting out from, the PDMS film (Figures 5.1b and 5.1c). An ohmic contact to the wires was made by evaporating ~ 300 nm of Au onto the back side of the PDMS film. Although the polymer/wire composite films were subsequently attached to a Ti foil to facilitate their use as photoelectrodes, replacement of this foil with a bendable current collector would yield a fully flexible device. Current-voltage measurements using a microprobe station on the polymer-supported cells showed that essentially all of the wires were contacted using this method (see Section 5.2.3). The photoelectrochemical energy-conversion properties of these polymer-supported wire arrays were then compared to those of a photoactive, planar crystalline Si bulk electrode as well as an array of nominally identical VLS-grown Si wires that were produced on, and still physically attached to, a photoinactive, p^+-Si substrate.

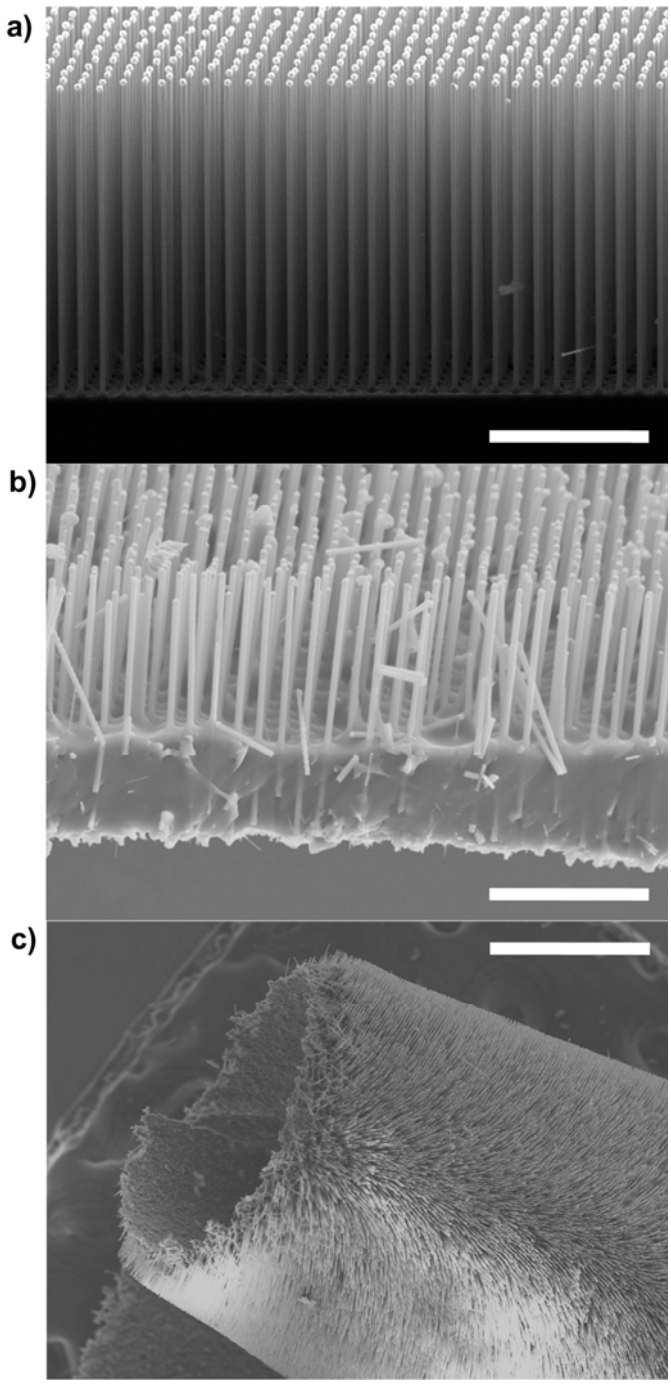

Figure 5.1. Si wire array photoelectrodes. Cross-sectional view SEM images of **(a)** a substrate-attached wire array (with the Cu catalyst tips still present) and **(b)** a peeled, polymer-supported wire array. The PDMS layer in **(b)** was deliberately made thicker than was typically used, to facilitate SEM imaging of the structure. The scale bar for **(a,b)** is 50 μm. **(c)** SEM image of a peeled, polymer-supported wire array demonstrating the flexibility of these films. Scale bar for **(c)** is 200 μm.

5.2.2 Electrode Fabrication and Processing

The Si wire array growth process has been described in detail elsewhere (see Section 3.5.3).[119] In this work, 300 nm of thermally evaporated Cu (99.9999%, ESPI) was used as the catalyst in all growths. The substrates were < 0.001 Ω-cm p^+-Si(111) wafers that were coated with a 300 nm thick thermal oxide (Silicon Quest International). The gas flow composition during wire growth was 500 sccm H_2, 10 sccm $SiCl_4$, 1 sccm dopant (0.25% BCl_3 in H_2) at 1 atm total pressure. The wire growth was allowed to proceed for 30 min, so that the wires were ~ 1.5 – 1.7 μm in diameter and 90 ± 15 μm long, with little length variation within a particular sample. The wires were formed on the substrate in a square arrangement having a 7 μm pitch. Following growth at 1000 ºC, the reactor tube was purged with N_2(g), and over the course of ~ 30 min was allowed to cool to ~ 750 °C before the sample was removed. A doping concentration in the wires of 10^{17} cm^{-3} was determined by a series of lithographically defined 4-point probe measurements on individual wires.[121] A LEO 1550 VP field-emission SEM at a 20 keV accelerating voltage was used to characterize the arrays.

Prior to being made into an electrode, each Si sample was etched for 10 s in 10% aq. HF, 10 min in 6: 1: 1 H_2O: 30% H_2O_2: concentrated HCl (v/v) at 70 °C (RCA2 clean), 10 s in 10% aq. HF, and then 2 min in 20% aq. KOH. The samples were thoroughly rinsed in 18 MΩ-cm resistivity H_2O and dried with N_2(g) between each step. This process removed the Cu catalyst tip and the top surface layer of the wires, but left the thermal oxide on the growth substrate intact.

The wire arrays were embedded in polymer and stripped from the underlying wafer using a procedure that closely followed our published methods (see Section 4.2).[144] In this process, 4.4 g of hexamethylcyclotrisiloxane (HMCTS, 98%, Alfa Aesar) was dissolved in ~ 5 mL methylene chloride, then mixed with 1.1 g of Sylgard 184 polydimethylsiloxane (Dow Corning, 1.0 g PDMS base, 0.1 g PDMS curing agent). This mixture was spin-coated onto the wire arrays at 1000 rpm for 1 min, then heated at 150 °C for 30 min. The HMCTS boiled off at this temperature without cross-linking into the PDMS, allowing the polymer to contract below the tips of the wires and cure conformally at the bases of the wires. This procedure produced a 10 – 20 μm thick layer of PDMS at the bottoms of the Si wires. The polymer-supported wire arrays were then mechanically removed from the underlying Si substrate using a razor blade.

Planar Si photoelectrodes were made from 1–2 Ω-cm p-Si(111) wafers. Ohmic back contacts were made to the substrate-attached wire array and to the planar electrodes by rubbing a Ga/In eutectic mixture onto the back side of the Si wafer. To make back contacts to the polymer-supported films, the polymer samples were carefully unrolled, taped down to a glass slide, and then ~ 300 nm Au was thermally evaporated onto the film. The polymer/wire films were then carefully painted onto squares of Ti foil using conductive silver paint to facilitate their use as photoelectrodes. Both types of wire arrays were silver-painted to a coiled Cu wire. The wire was placed in a glass tube and the electrode edges were sealed in Hysol 9460 epoxy.

Immediately prior to use in the photoelectrochemical cell, the polymer-supported electrodes were subjected to an oxygen plasma to remove any residual PDMS adhered to

the exposed Si wires and to convert the PDMS surface from hydrophobic to hydrophilic so that the aqueous liquid electrolyte could effectively penetrate the array. For each electrode, the plasma generator (March PX-500) was run for 180 s at 600 W with 330 mTorr O_2. Before photoelectrochemical measurements, all of the electrodes were etched in 10% aq. HF for 10 s to remove the surface oxide.

5.2.3 Microprobe Station Measurements

To investigate the effectiveness of the back contact to the polymer-supported wire arrays, a Signatone H100 Series Probe Station was used to make contact to the tops of Si wires and, in combination with a Keithley 237 Source-Measure Unit, bias them to -1 V and measure the resulting current. A total of 50 points were measured on 4 different samples for substrate-attached wire arrays along with another 50 points on 4 different samples for peeled, polymer-supported wire arrays. At -1 V, the average current measured was 0.11 ± 0.05 mA for the substrate-attached samples and 0.08 ± 0.04 mA for the freestanding, polymer-supported samples. The error in the measurements was due to the variation in the number of wires contacted each time, which was difficult to control on such a fine scale using this probe station. However, all probed points gave a reasonable current, demonstrating that there were no large dead areas on the peeled array films.

5.3 Photoelectrochemistry

5.3.1 Methyl Viologen Electrolyte

The use of a liquid-junction photoelectrochemical cell (Figure 5.2) allowed for the evaluation of the energy-conversion performance of the wire arrays without the challenges associated with producing high-quality radial solid-state junctions, transparent conductors, or metallic grid emitter contacts. Although published Si wire array photoelectrochemical cells to date have demonstrated low efficiencies (around 0.1%),[141, 142] we have recently shown that with controlled p-type doping by the in situ addition of BCl_3 during the array growth, Cu-catalyzed p-Si wire arrays attached to the Si substrate in contact with aqueous methyl viologen electrolyte yield drastically improved performance.[146] The aqueous solution containing methyl viologen (MV^{2+}/MV^{+}) as the redox species permeated the full length of the wire array to form a highly rectifying, conformal contact with p-type Si,[147, 148] yielding a high barrier height, along with open-circuit voltages (V_{oc}) > 550 mV and near the bulk diffusion/recombination limit on planar, crystalline Si samples under illumination conditions that produced short-circuit photocurrent densities (J_{sc}) of 25 mA cm^{-2}. The MV^{+} radical cation is highly absorbing across much of the visible (350 – 750 nm) spectrum,[149] which gives the test electrolyte an intense, violet color. To minimize confounding effects due to solution absorbance, 808 nm laser light was used to excite the Si photoelectrodes in all of the comparisons reported herein. A calibrated photodiode was placed in the solution at the height of the wire array electrode to monitor the in situ illumination intensity.

5.3.2 Photoelectrochemical Cell Setup

For electrochemical measurements, a flat-bottomed glass cell was filled with 50 mL of aqueous 0.05 M methyl viologen dichloride (MV^{2+}, Aldrich 98%), 0.5 M K_2SO_4, and buffered at pH = 2.9 using 0.1 M potassium hydrogen phthalate and sulfuric acid. The cell was constantly purged with H_2O-saturated Ar. The cell contained a standard calomel reference electrode (SCE), a Pt mesh counter electrode separated from the main compartment by a medium porosity glass frit, a large carbon cloth electrode, a small carbon cloth electrode, a face-down Si working electrode (wire array or planar), and a calibrated Si photodiode (Thorlabs) that was carefully positioned at the same height as the Si working electrode surface (Figure 5.2). To minimize mass-transport limitations, a stir bar was placed next to the Si electrode and stirred as vigorously as possible without causing vortexing, by using a magnet attached to an electric motor (NWSL 12270-9) that was controlled by a DC power supply (Rail Power 1370).

Both the oxidized and reduced form of the redox couple must be present for a cell to have a well-defined potential. As mixed, only the MV^{2+} form was present in any appreciable quantity, so the solution was electrolyzed before each measurement to produce the MV^{+} radical species. The solution was electrolyzed to -0.6 V vs. SCE using the large carbon cloth as working electrode, the Pt mesh as counter electrode, and the SCE as reference. This process produced ~ 3 mM MV^{+} and turned the solution a dark violet color ($E^{o'}(MV^{2+/+})$ = -0.67 V vs. SCE). The solution potential was monitored and adjusted periodically to maintain a value of -0.6 V vs. SCE. Current-potential data were obtained using the Si as the working electrode, the large carbon cloth as the counter

electrode, and the small carbon cloth (poised at the solution potential) as the reference. A 1 W, 808 nm diode laser (Thorlabs L808P1WJ) was used to minimize the solution absorbance. The power output of the laser was adjustable, and the calibrated photodiode was used to determine the light intensity incident on the Si working electrode. A Princeton Applied Research model 273 potentiostat was used to collect the current-potential data.

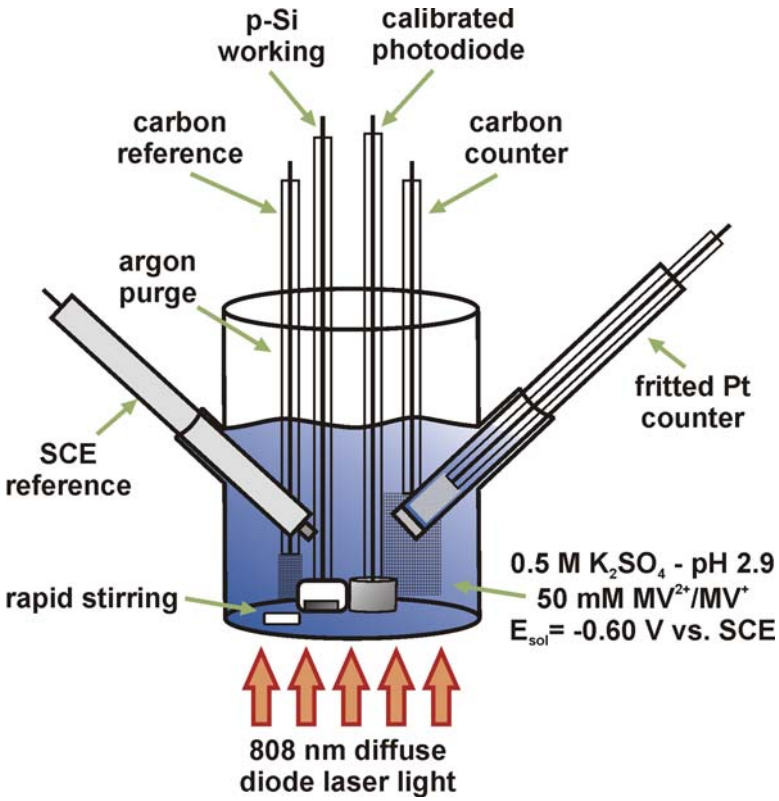

Figure 5.2. Diagram of the cell setup used for photoelectrochemical measurements. Monochromatic 808 nm illumination was used to minimize solution absorbance. A calibrated photodiode was kept in solution at the height of the Si working electrode to monitor the in situ illumination intensity (image credit: S.W. Boettcher).

5.4 Photoelectrochemical Energy-Conversion Properties

5.4.1 External Quantum Efficiency vs. Potential Behavior

Figures 5.3, 5.4, and 5.5 compare the current density vs. potential (*J-E*) behavior of a planar p-Si wafer, a substrate-attached wire array, and a peeled, polymer-supported Si wire array, respectively. The *J-E* data at various light intensities have been displayed on a common graph by presenting the data in terms of the measured external quantum efficiency, which is directly proportional to the observed photocurrent density.

When using a monochromatic illumination source, it is more meaningful to describe the current in terms of the quantum efficiency. A given photon will have an energy dependent upon its wavelength. However, a photon above the band gap can only excite one electron to the conduction band of a semiconductor to be collected as current (in the absence of multi-exciton generation), with the additional energy being wasted as heat as the electron thermalizes to the conduction band energy. Therefore, different wavelengths of light with the same input illumination intensity will result in different currents in a solar cell. The external quantum efficiency (Φ_{ext}) is the fraction of photons incident on the solar cell that produce a charge-carrier collected as current. The equation to convert current to Φ_{ext} is then:

$$\Phi_{ext} = \frac{\text{electrons}}{\text{incident photon}} = \frac{i\frac{1}{q}}{P\frac{\lambda}{hc}} = \frac{i \text{ x } 1240\frac{\text{mW nm}}{\text{mA}}}{P \text{ x } 808 \text{ nm}} \qquad (5.1)$$

where i is the current in mA, q is the electronic charge, P is the power incident on the cell in mW, λ is the wavelength in nm (808 nm in this work), h is Planck's constant, and c is the speed of light.

5.4.2 Planar Electrodes

As shown in Figure 5.3, at light intensities ≤ 40 mW cm^{-2}, the planar p-Si photoelectrode exhibited $\Phi_{ext} \sim 0.7$, in accord with the value expected for specularly reflective, high-quality bulk Si samples.[150] The decline in the short-circuit external quantum yield ($\Phi_{ext,sc}$) at higher light intensities resulted from mass-transport effects in the solution, while the increase in open-circuit voltage with illumination intensity occurred because the value of V_{oc} depends logarithmically on the photocurrent. The high Φ_{ext}, along with $V_{oc} \sim 530 – 570$ mV, demonstrated that the methyl viologen liquid electrolyte effectively formed a high barrier-height junction with the p-Si surface.

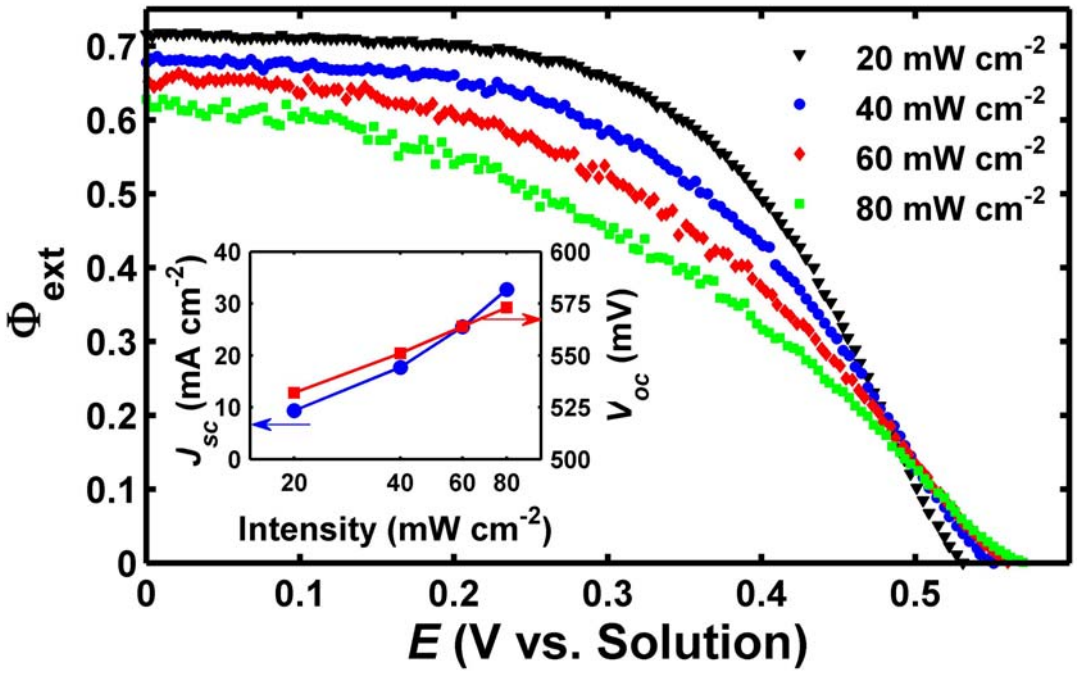

Figure 5.3. Effect of intensity on planar photoelectrode performance. Plot of external quantum efficiency (Φ_{ext}) vs. potential (E) for different illumination intensities using a planar photoelectrode. Inset shows semilogarithmic (lin-log) plots of J_{sc} and V_{oc} vs. intensity.

5.4.3 Wire Array Electrodes

Figures 5.4 and 5.5 depict the *J-E* behavior of substrate-attached and freestanding polymer-supported wire array photoelectrodes, respectively. The photoelectrochemical response observed from the substrate-attached wire arrays arose primarily from the Si wires, because as established previously, the presence of the thermal oxide, combined with the use of degenerately doped p-Si substrates, minimized the photoelectrochemical response from the Si substrate.[146] The *J-E* behavior of the polymer-supported wire arrays

was very similar to that of the wire array on the growth substrate (Table 5.1, Figures 5.4, 5.5, and 5.6). The most noticeable difference was in the fill factor, which improved after casting the PDMS into the Si wires (even if the array was not then peeled from the substrate), consistent with the presence of shunts through the base of the substrate-attached wire arrays. However, the fill factor of photoelectrodes made from substrate-attached wire arrays that were not embedded in PDMS (Figure 5.4) improved significantly when a surface etch was performed immediately prior to measurement of the *J-E* behavior,[146] suggesting that a Cu-rich surface layer might still be present on the wires despite the use of a Cu etch prior to electrode fabrication. However, this etch caused irreversible damage to the polymer-supported electrodes (see Section 5.5.2), precluding a direct comparison of the array performance under these more optimal conditions.

The $\Phi_{ext,sc}$ values observed for the polymer-supported wire array photoelectrodes were slightly lower than those observed for the substrate-attached wire arrays without PDMS (Table 5.1, Figure 5.6). This difference is expected because the PDMS covered the bottom 10 – 20 μm of the Si wires, preventing those regions from directly exchanging current with the electrolyte. The observed $\Phi_{ext,sc} = 0.2 – 0.3$ is significant, especially considering that the packing fraction (percentage of the cross-sectional device area occupied by wires) of the array was ~ 4%. Without enhanced photon capture, a 4% packing fraction would result in a $\Phi_{ext,sc}$ of ≤ 0.04.

The V_{oc} values measured for wire array photoelectrodes, although ~ 150 mV lower than the planar electrode, are higher than those previously measured on Si nanowire arrays.[137, 139-142] The decrease in V_{oc} is attributed to an increase in dark current from the

increased junction area of the wire array relative to the planar electrode, as well as from the increased effects of surface recombination (see Section 2.5.3).[151] A decrease in wire size from the ~ 1.5 μm radius investigated herein would thus result in a lower V_{oc} without a concomitant increase in J_{sc}, in accord with the lower photovoltages observed for photoelectrodes formed using Si nanowires.[137, 139, 140]

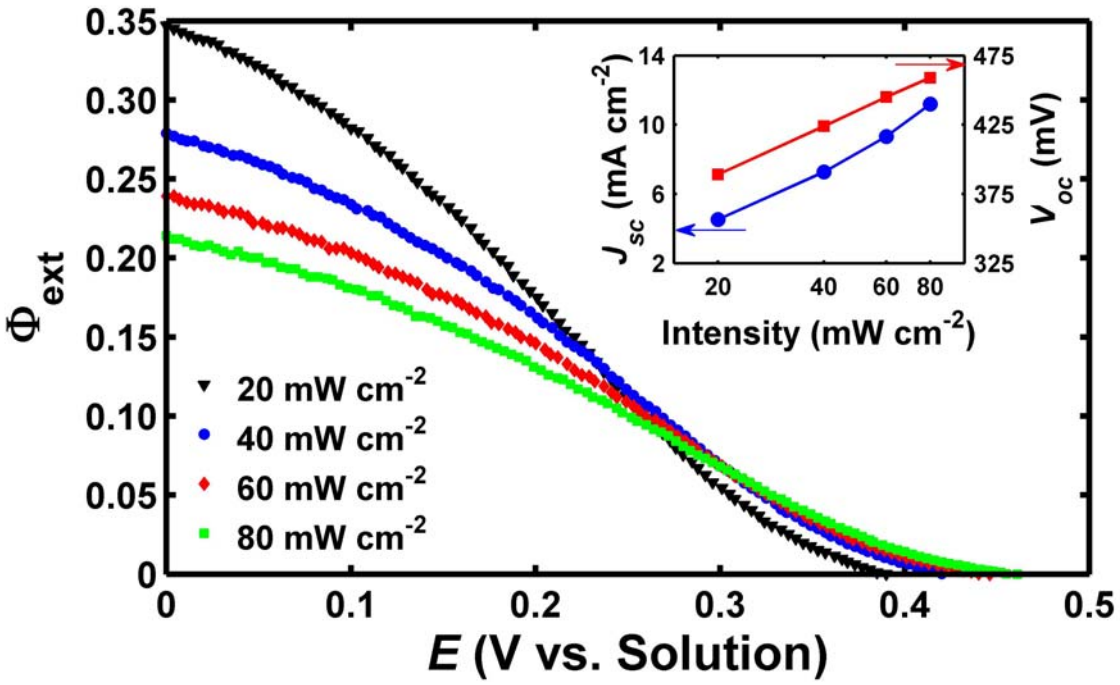

Figure 5.4. Effect of intensity on substrate-attached wire array photoelectrode performance. Plot of external quantum efficiency (Φ_{ext}) vs. potential (E) for different illumination intensities using a substrate-attached wire array without PDMS. Inset shows semilogarithmic (lin-log) plots of J_{sc} and V_{oc} vs. intensity.

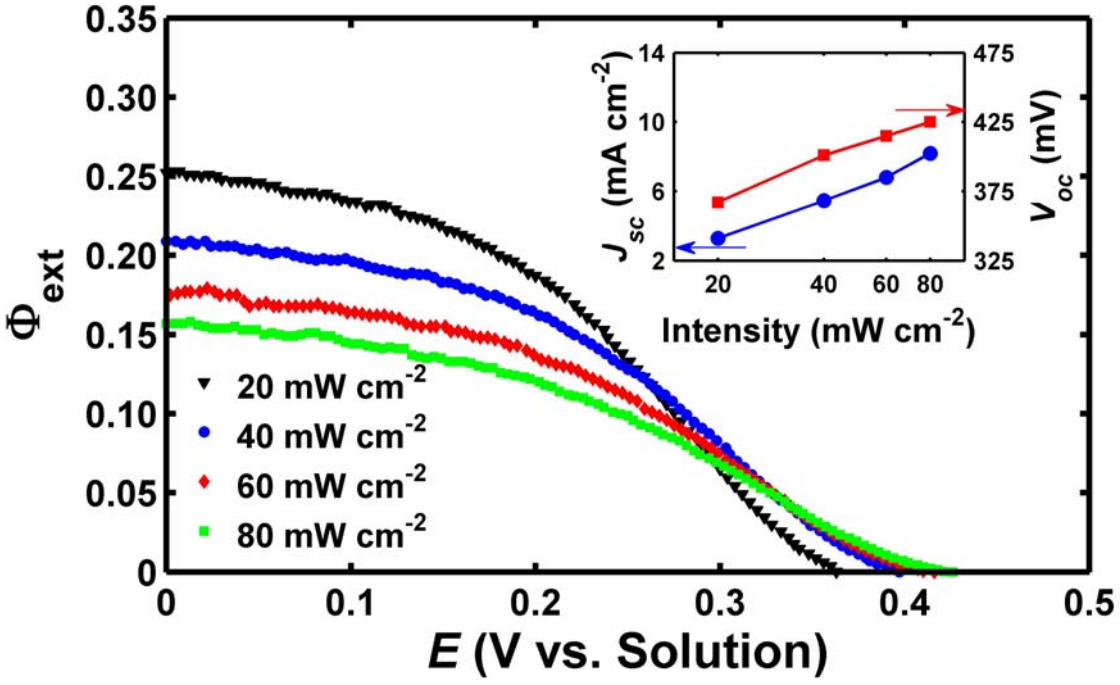

Figure 5.5. Effect of intensity on peeled, polymer-supported wire array photoelectrode performance. Plot of external quantum efficiency (Φ_{ext}) vs. potential (E) for different illumination intensities using a peeled, polymer-supported wire array without PDMS. Inset shows semilogarithmic (lin-log) plots of J_{sc} and V_{oc} vs. intensity.

Table 5.1. Wire array photoelectrochemical cell performance data.[a]

	Substrate-attached			
Intensity (mW cm^{-2})	20	40	60	80
$\Phi_{ext,sc}$	0.36 ± 0.06	0.29 ± 0.05	0.25 ± 0.05	0.22 ± 0.04
J_{sc} (mA cm^{-2})	4.6 ± 0.7	7.4 ± 1.3	9.8 ± 1.8	11.6 ± 2.1
V_{oc} (mV)	356 ± 21	398 ± 16	422 ± 16	437 ± 17
FF	0.26 ± 0.03	0.27 ± 0.02	0.27 ± 0.03	0.28 ± 0.03
η_{808} (%)[b]	2.2 ± 0.6	2.0 ± 0.6	1.9 ± 0.5	1.8 ± 0.5
$\eta_{808,corr}$ (%)[c]	3.1 ± 0.8	3.0 ± 0.8	2.8 ± 0.8	2.7 ± 0.8
	Peeled, polymer-supported			
Intensity (mW cm^{-2})	20	40	60	80
$\Phi_{ext,sc}$	0.27 ± 0.04	0.23 ± 0.04	0.20 ± 0.03	0.18 ± 0.03
J_{sc} (mA cm^{-2})	3.5 ± 0.5	6.0 ± 0.9	7.9 ± 1.3	9.6 ± 1.6
V_{oc} (mV)	339 ± 29	373 ± 29	390 ± 30	402 ± 31
FF	0.36 ± 0.05	0.36 ± 0.04	0.35 ± 0.05	0.35 ± 0.04
η_{808} (%)[b]	2.1 ± 0.3	2.0 ± 0.3	1.8 ± 0.2	1.6 ± 0.2
$\eta_{808,corr}$ (%)[c]	2.8 ± 0.4	2.8 ± 0.4	2.6 ± 0.4	2.4 ± 0.4

[a]Averages and standard errors were calculated using 10 different samples of both substrate-attached and peeled, polymer-supported wire arrays.

[b]This efficiency is for monochromatic 808 nm illumination.

[c]This efficiency is for monochromatic 808 nm illumination after correcting for concentration overpotential and uncompensated resistance losses.

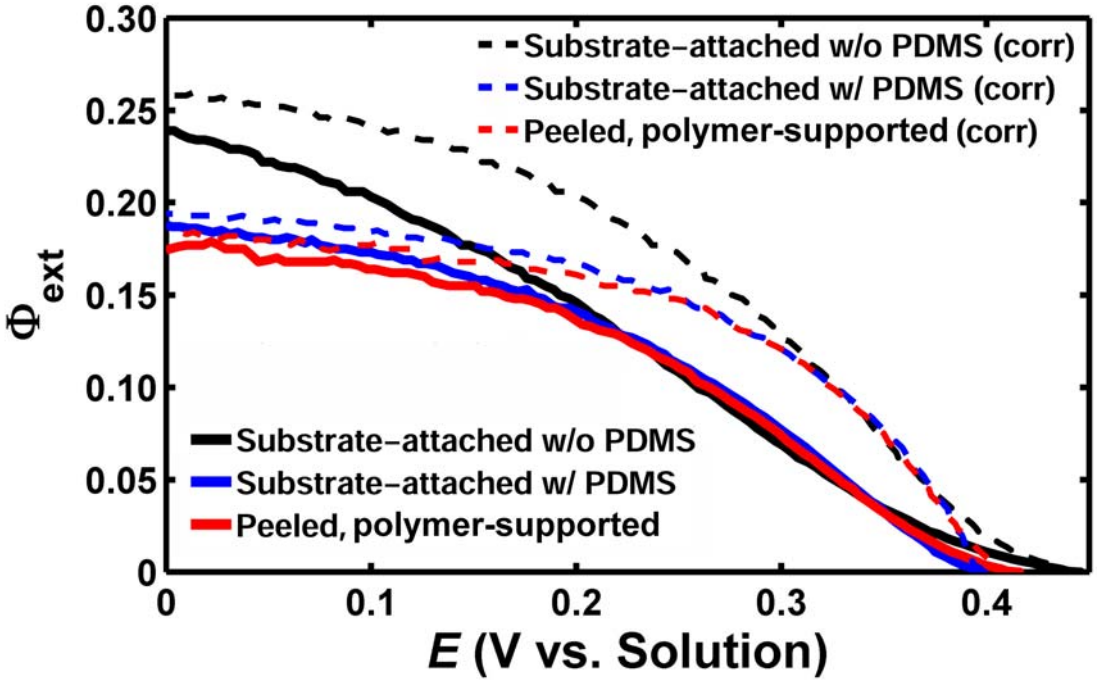

Figure 5.6. Effect of PDMS layer on photoelectrochemical behavior. Plot comparing the external quantum efficiency (Φ_{ext}) vs. potential (E) behavior of a substrate-attached wire array without PDMS, a substrate-attached wire array with PDMS cast on it, and a peeled, polymer-supported wire array electrode under 60 mW cm^{-2} of 808 nm illumination. Dashed lines are the photoelectrode behavior corrected for concentration overpotential and solution resistance losses. All three electrodes came from the same Si wire array sample.

5.4.4 Corrections for Concentration Overpotential and Uncompensated Series Resistance

Assessing the inherent energy-conversion behavior of the wire array electrodes requires correction for any concentration overpotential and uncompensated resistance losses that arise from the use of this unoptimized test electrolyte. The corrected Φ_{ext} vs. E behavior (Figure 5.6, dashed lines) reveals the performance of the photoelectrodes that would be obtained in a thin-layer cell that had minimal concentration overpotential and solution resistance losses, with the corrected efficiency values for each type of wire array photoelectrode summarized in Table 5.1. The concentration overpotential is the voltage that is necessary to create a concentration gradient and drive the charge-transferring redox species in solution to the electrode surface. The solution resistance refers to the ohmic series resistance of the liquid electrolyte. Equations have been derived to account for these losses.[152, 153] The overpotential depends on the limiting anodic and cathodic currents, which depend on the concentrations of the two forms of the redox couple. The equation for correcting the potential is:

$$E_{corr} = E - iR_{cell} - \eta_{conc} \tag{5.2}$$

$$\eta_{conc} = \left(\frac{k_B T}{nq}\right)\left\{\ln\left(\frac{J_{l,a}}{-J_{l,c}}\right) - \ln\left(\frac{J_{l,a} - J}{J - J_{l,c}}\right)\right\} \tag{5.3}$$

Where E_{corr} is the corrected potential, E is the measured potential, i is the measured current, R_{cell} is the cell solution resistance, η_{conc} is the concentration overpotential, J is the current density, and $J_{l,a}$ and $J_{l,c}$ are the mass-transport-limited anodic and cathodic current

densities. $J_{l,a}$ and $J_{l,c}$ were estimated from the limiting current measured for the specific electrode of interest in forward bias and from measurements made on a glassy carbon electrode in the same cell configuration, respectively. The uncompensated cell solution resistance, $R_{cell} \sim 20\ \Omega$, was extracted from the inverse slope of the *J-E* curve collected using the glassy carbon working electrode, after correction for the concentration overpotential using Equation 5.3.

5.5 Effect of Cu Impurities

5.5.1 Planar Electrodes

The effect of the Cu catalyst used for wire growth on the electronic properties of the arrays is of significant interest in this work. Based on the VLS growth mechanism,[42] it is expected that the Si wires produced will be saturated with the catalyst metal to the solubility limit at the growth temperature. However, it has been shown that the high diffusivity of Cu in p-Si at room temperature allows most of the metal to out-diffuse to the surface and/or defect sites, suggesting that the bulk concentration most likely approaches the room temperature solubility limit.[154] To investigate the effect of this Cu saturation, we annealed planar Si samples of the same doping as the wires with Cu metal and compared them to pure planar electrodes.

Planar photoelectrodes used 1 – 2 Ω-cm p-Si(111) wafers (Silicon Quest International). To prepare Cu-saturated samples, the wafers were etched for 2 min in 10% aq. HF immediately prior to having a 300 nm Cu layer (99.9999%, ESPI) thermally evaporated

onto the front surface. They were then annealed at 1000 ºC under 500 sccm H_2 at atmospheric pressure for 30 min in the same reactor used to grow Si wire arrays. The reactor tube was purged with N_2 and allowed to cool to ~ 750 °C over the course of ~ 30 min before the sample was removed. Cu annealed wafers underwent the same etch treatment as the wire arrays before being made into electrodes. Back contact was made to both types of planar samples using Ga/In eutectic. Both types of planar electrodes were tested in the same aqueous methyl viologen electrolyte used to measure wire array photoelectrodes.

Figure 5.7 shows the resulting photoelectrochemical behavior at 60 mW cm^{-2}. The pure, unannealed planar Si exhibited good solar cell properties, as shown in Figure 5.3. After being annealed with Cu, however, the fill factor of the Φ_{ext} curve dropped from 0.47 to 0.28, which is close to that observed for substrate-attached Si wire arrays (Table 5.1). We speculate that a Cu-rich surface layer causes this loss. Even though the Si surface was etched with 20% aq. KOH before being made into an electrode, more Cu could out-diffuse to the surface in the time between the etch and the photoelectrochemical measurement (a day or more). After conducting a 2 min etch in 20% aq. KOH at room temperature immediately before the measurement, the fill factor improved back to 0.49. Excepting some loss in V_{oc}, the KOH-etched, Cu-annealed planar electrode behavior was nearly as good as the pure planar Si, indicating that the level of Cu present does not affect the bulk Si electronic properties too adversely.

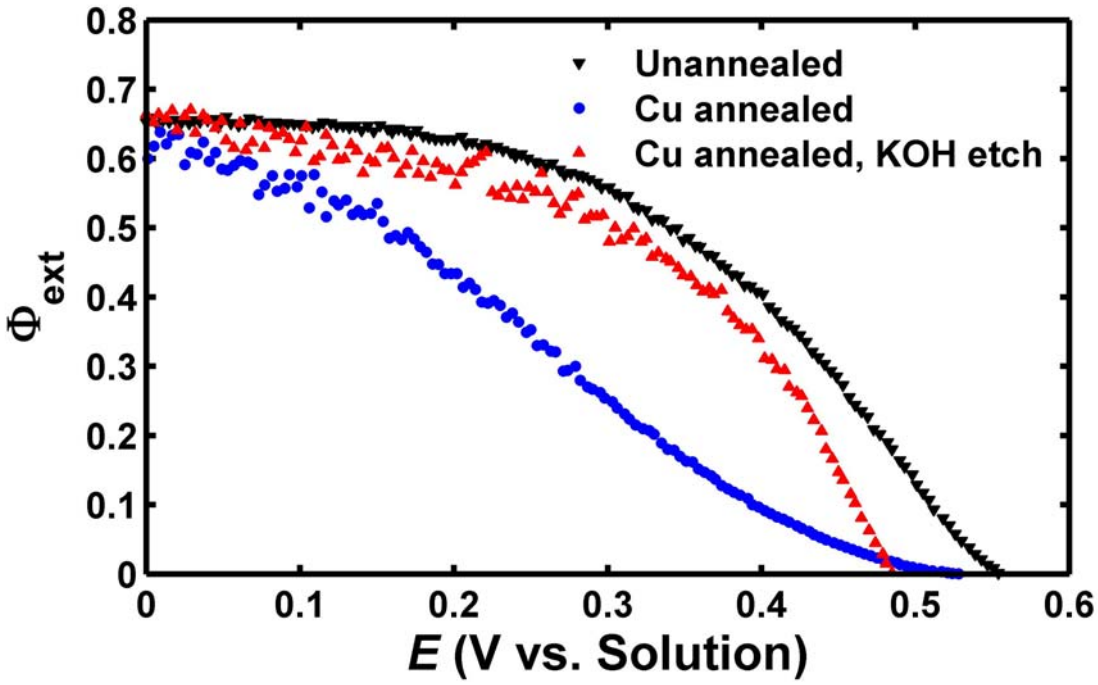

Figure 5.7. Effect of Cu impurities on planar photoelectrodes. Plot of the external quantum efficiency (Φ_{ext}) vs. potential (E) of planar p-Si before and after annealing in the presence of Cu. Annealed performance is shown with and without a KOH surface etch immediately prior to the measurement. Illumination intensity was 60 mW cm^{-2} at 808 nm.

5.5.2 Wire Array Electrodes

As with Cu-annealed planar electrodes, the fill factor of substrate-attached wire arrays was observed to improve markedly with a 1 – 2 min 20% aq. KOH etch immediately before taking measurements (Figure 5.8). Again we propose that this enhancement is due to the removal of a Cu-rich surface layer from the wires. The optimized substrate-attached Si wire array performance has been reported elsewhere.[146] Unfortunately, this surface etch proved deleterious to polymer-supported wire array electrodes, making a direct comparison with this method impractical (Figure 5.8a). Although it is not entirely

clear what effect the KOH had on these electrodes, we believe damage was occurring to the back contacts. The same behavior for both types of electrodes was observed even if the initial KOH etch prior to electrode fabrication was allowed to run longer. While it would have been ideal to conduct the surface etch before applying the polymer, the need to cast PDMS, peel the film, evaporate a metallic back contact, and prepare the surface with a plasma etch to produce a polymer-supported wire array electrode took too long for the benefit of the KOH etch to be noticeable. When measured one day after a KOH etch, the substrate-attached wire array electrode returned to its reduced fill factor state, demonstrating that the benefit of this surface treatment is temporary (Figure 5.8b). Cu is known to preferentially diffuse to p^+ over p-Si areas,[154] indicating that the Cu concentration in the growth substrate should be significantly higher than the wires. The diffusion of additional Cu from the substrate to the wires after the KOH surface etch could account for the energy-conversion properties reverting back to their pre-etch behavior. Future improvement of the peeled, polymer-supported wire array energy-conversion properties could therefore be pursued by a new surface etch that does not damage the delicate electrode or by thoroughly gettering Cu impurities out of the wires and growth substrate before applying PDMS (i.e., leaving the substrate-attached arrays in $FeCl_3$ for an extended period of time to siphon out Cu).

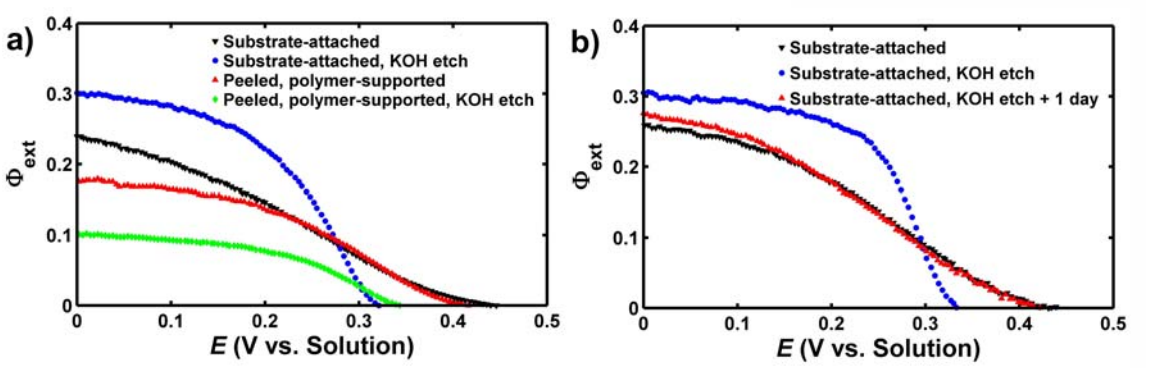

Figure 5.8. Effect of KOH etch on wire arrays. (a) Plot of the external quantum efficiency (Φ_{ext}) vs. potential (E) for substrate-attached and peeled, polymer-supported wire array electrodes with and without a KOH surface etch immediately prior to the measurement. Both of these electrodes came from the same Si wire array. **(b)** Plot of the external quantum efficiency (Φ_{ext}) vs. potential (E) for a different substrate-attached wire array electrode before a KOH surface etch, immediately after the KOH etch, and one day after the KOH etch. Illumination intensity was 60 mW cm^{-2} at 808 nm.

5.6 Spectral Response

5.6.1 Substrate-Attached vs. Peeled, Polymer-Supported Wire Arrays

The spectral response properties of the wire array photoelectrodes were evaluated in aqueous methyl viologen as a function of the angle of incidence (Figure 5.9).[122] The $\Phi_{ext,sc}$ values observed at 808 nm were in good agreement with those measured at low light intensity using the 808 nm laser. As observed previously, the quantum efficiency of the wire array photoelectrode was highly dependent on the angle of incidence.[122, 146] At angles significantly off normal, the optical path length through the substrate-attached wires increased, less light passed completely in the regions between wires, and $\Phi_{ext,sc} >$ 0.6 (Figure 5.9a). The peeled, polymer-supported wire array spectral response also

showed an increase in $\Phi_{ext,sc}$ at higher angles, with a maximum of $\Phi_{ext,sc} \sim 0.45$ (Figure 5.9b).

The angular dependence of $\Phi_{ext,sc}$ suggests that more disorder was present in the peeled wire array electrodes than in the substrate-attached array electrodes, resulting in additional scattering that reduced the dependence of $\Phi_{ext,sc}$ on the angle of incidence. SEM images of the substrate-attached wires showed a well-defined array with a uniform wire geometry (Figure 5.10a). Such structures also produced a distinct, square optical diffraction image when illuminated with a 633 nm He-Ne laser beam (Figure 5.10b). Embedding the wires in PDMS (and leaving the wires on the substrate) made the diffraction pattern less distinct (Figure 5.10d), even though the SEM image still showed an ordered structure (Figure 5.10c), presumably because the polymer surface induced some optical scattering. Peeling the polymer-supported array and silver-painting it to a metal foil to make an electrode (see Section 5.2.2), produced distinct domains in the surface of the array, as revealed by SEM images (Figure 5.10e), and the loss of the ordered optical diffraction pattern (Figure 5.10f). The enhanced scattering due to this disorder is consistent with the reduced dependence of $\Phi_{ext,sc}$ on the incidence angle for the peeled, polymer-supported wire arrays.

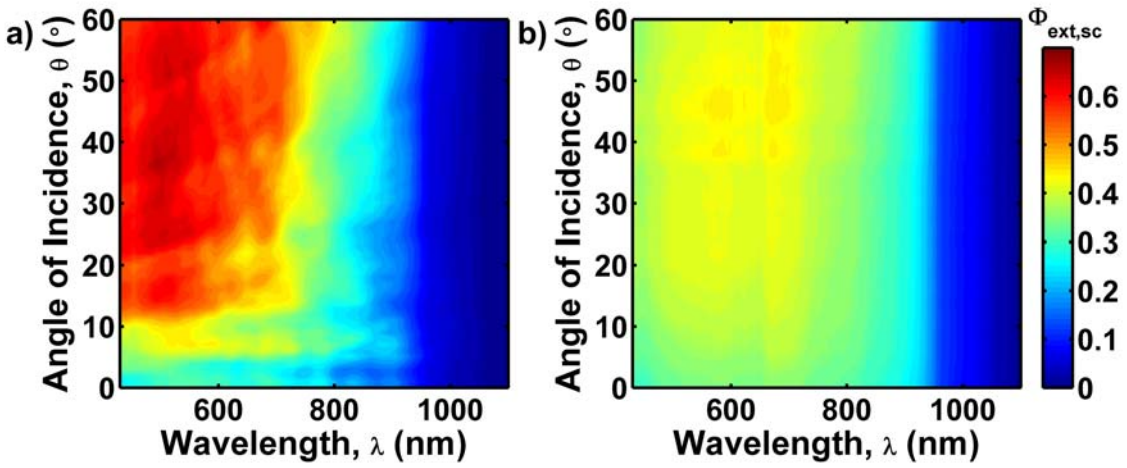

Figure 5.9. Si wire array spectral response. 2-dimensional color maps depicting the short-circuit quantum yield, $\Phi_{ext,sc}$ at low intensity as a function of wavelength and angle of incidence for **(a)** a substrate-attached wire array without PDMS and **(b)** a peeled, polymer-supported wire array.

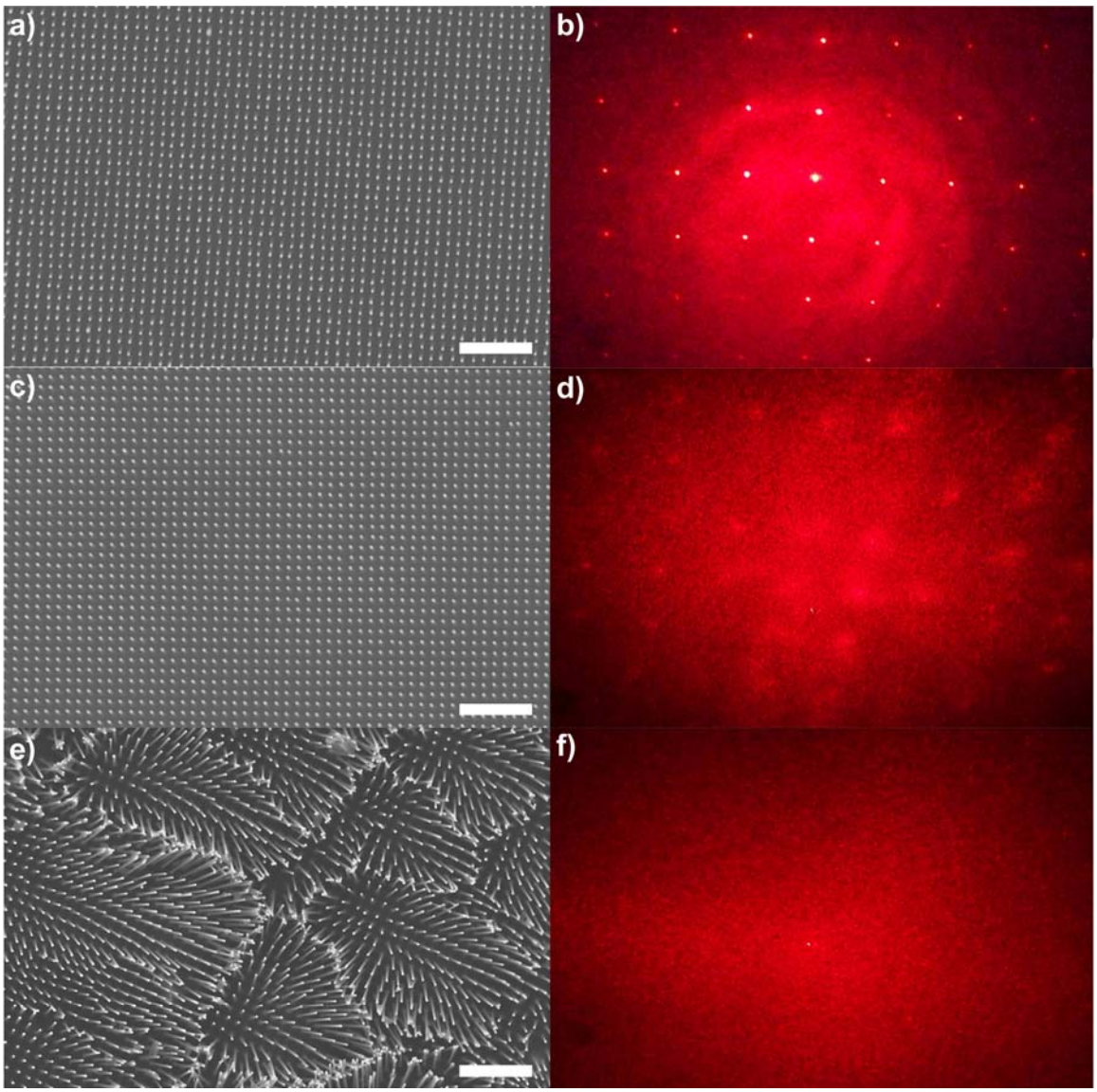

Figure 5.10. Increased scattering in peeled, polymer-supported wire array electrodes. (a,c,e) Top-down SEM images of **(a)** a substrate-attached wire array, **(c)** a substrate-attached wire array with PDMS cast on the base, and **(e)** a peeled, polymer-supported wire array silver-painted to a Ti substrate in the manner used to prepare photoelectrodes. The silver-painting process produced clearly distinguishable contours in the thin film. The scale bar for **(a,c,e)** is 50 μm. **(b,d,f)** Diffraction patterns resulting from the reflection of a 633 nm He-Ne laser off of **(b)** a substrate-attached wire array, **(d)** a substrate-attached wire array with PDMS cast on the base, and **(f)** a peeled, polymer-supported wire array silver-painted to a Ti substrate. While the periodic, square arrangement of the wires is clearly evident in the diffraction pattern of **(b)**, the scattering introduced by the PDMS layer made the pattern less crisp in **(d)**, and the loss of strict periodicity in **(e)** caused enough disorder that no discernible pattern was evident in **(f)**.

5.6.2 Spectral Response and Diffraction Image Setup

The apparatus used for spectral response measurements has been described in detail elsewhere.[122] The same aqueous methyl viologen electrolyte was used, with stirring, as for photoelectrochemical measurements. A glass box cell with an open top was used, to allow for the rotation of the working electrode. Using a Pt coil counter electrode and a Ag/AgCl reference electrode, the photoresponse of the wire arrays were measured at -400 mV vs. the reference, with the bias chosen to position the photoelectrochemical cell near short-circuit conditions based on the cell's observed current-potential behavior. Absolute V_{oc} values were not necessary and hence optically transparent electrolyte solutions were used ($[MV^{2+}]/[MV^{+}]>>1$), allowing measurements across the full visible spectrum. A custom-built, motorized stage enabled computerized control of the illumination incidence angle by adjusting the position of the working electrode. Normal incidence was set by directing the laser approximately perpendicular to the wire array surface and then minimizing the photoresponse. A tunable, collimated light source was achieved by coupling a supercontinuum laser (Fianium) to a monochromator along with a chopper and lock-in amplifier. Data were collected in 2 nm increments. $\Phi_{ext,sc}$ was determined by relating the photoresponse of the wire arrays to a calibrated photodiode that had been placed in nominally the same location within the cell.

To produce diffraction images, a 633 nm He-Ne laser source of spot size ~ 1 mm^2 was passed through a small hole in a vertical plate to strike the wire array electrodes at approximately normal incidence. The resulting diffraction pattern was reflected back

onto the vertical plate. Images were taken in the absence of room light, using a digital camera mounted on a tripod.

5.7 Conclusion

The behavior of the peeled, polymer-supported Si wire film relative to the unpeeled, substrate-attached wire array electrode demonstrates that Si wires can be transferred into inexpensive, flexible films without sacrificing their solar energy-conversion performance. The single-wavelength Φ_{ext} and V_{oc} values reported herein are large compared to those reported for previous Si nanowire array solar cells, and the spectral response data showed high $\Phi_{ext,sc}$ across the entire visible spectrum. The peeled wire/polymer composite photoelectrode had $\Phi_{ext,sc}$ values that ranged from 0.28 (approximately 7 times the packing fraction, ~ 4%) at normal incidence to 0.45 at high angles of incidence (~ 50º). By increasing the packing fraction and exploring designs that lengthen the path of light through the wires, quantum efficiencies approaching that of planar bulk Si should be attainable from the peeled wire array photoelectrodes. If optical absorption by the redox species can be minimized, improving the J_{sc} to 35 mA cm^{-2} indicates that energy-conversion efficiencies > 5% are possible under AM 1.5 illumination even without improving the other uncorrected characteristics of these polymer-supported wire array photoelectrodes.[155] The overpotential-corrected data demonstrate that better performance is achievable in optimized liquid-junction or solid-state cell configurations. The results indicate that a flexible, Si wire array solar cell with a competitive efficiency is possible based on wire array architectures without the need for a supporting crystalline Si wafer.

Chapter 6

Future Directions and Outlook for Radial Junction Wire Arrays

6.1 An Inexpensive, Flexible, Efficient Solid-State Si Wire Array Solar Cell

6.1.1 Efficiency Projections

Now that the radial junction project has successfully demonstrated the controlled fabrication of highly uniform Si wire arrays from abundant materials in a potentially low-cost, scalable process and shown that the inherent energy-conversion properties of such arrays should enable them to make efficient photovoltaic devices, the next logical direction of this research is to construct a solid-state wire array solar cell and optimize its efficiency. Kayes, et al. from our research group made an initial attempt to produce and test a solid-state wire array solar cell fabricated with Si wires from our VLS growth process.[156] While efficiencies up to 0.87% were observed, this cell did not incorporate numerous advances we have made since that time, including high-quality, in situ p-type doping and larger diameter wires.

Based on modeling,[34] single-wire measurements,[121] absorption studies,[122] and wire array photoelectrochemical measurements (see Chapter 5)[146] on our current Si wires, we expect a well-constructed solid-state cell to have a significantly better performance, with an efficiency > 10% within reach. Solar cell efficiency, η, is determined by:

$$\eta = \frac{J_{sc} V_{oc} f}{P_{in}} \tag{6.1}$$

where J_{sc} is the short-circuit photocurrent density, V_{oc} is the open-circuit voltage, f is the fill factor, and P_{in} is the power density of the incident illumination. The relevant solar cell efficiency is that occurring under the white light of the solar flux at the Earth's surface. This is approximately 100 mW cm^{-2} for AM 1.5 illumination, which has a very similar photon flux to a 60 mW cm^{-2} intensity of 808 nm illumination. Therefore, the uncorrected values from Table 5.1 for a peeled, polymer-supported wire array photoelectrochemical cell at 60 mW cm^{-2} 808 nm illumination can be used in Equation 6.1 with a P_{in} of 100 mW cm^{-2} to estimate an efficiency under white light of ~ 1.1%. This efficiency, though a promising start, could be greatly increased by incorporating improvements achieved in the laboratory on various aspects of the wire array cell design. Increasing the J_{sc} in the cell to 35 mA cm^{-2} by effectively trapping light within the Si wires ($\Phi_{ext} \sim 0.9$) would result in $\eta \sim 5.2\%$.[155] This is a realistic projection considering that up to 96% absorption has been measured at normal incidence with this wire array geometry by including a Lambertian back reflector and an antireflection coating on the wire surfaces. Wires with a clean surface free of catalyst impurities, i.e., from a KOH etch (Figure 5.8) or effective gettering procedure, have demonstrated uncorrected fill

factors ~ 0.55. Combined with effective light trapping, this results in η ~ 8.2%. If the same improvements are made in a solid-state device, such that concentration overpotential and solution resistance losses are eliminated, the fill factor can be corrected to ~ 0.7, leading to η ~ 10.5%. Finally, if this device incorporates good p-n junctions with passivated surfaces, for which single-wire measurements have demonstrated V_{oc} ~ 580 mV, the efficiency could be ~ 14.2% or higher. These projections are reasonable and based on results that have already been achieved through laboratory experiments on these Si wires.

6.1.2 Envisioned Fabrication Process

We have devised a realistic plan for the fabrication of an efficient solid-state wire array photovoltaic device. Figure 6.1 shows a schematic of the envisioned process. As we have previously demonstrated,[119] a Si(111) wafer with a thermally grown SiO_2 buffer layer with patterned islands of Cu catalyst (Figure 6.1a) is used as a substrate to epitaxially grow vertically aligned p-Si wires of controlled length, diameter, spacing and arrangement (Figure 6.1b) from gaseous $SiCl_4$ via the VLS growth mechanism. The Cu catalyst tips are then chemically removed (as in Section 5.2.2), metal impurities are removed by gettering to the feasible limit (possibly by extended immersion in $FeCl_3$ or another Cu etchant), and a thin thermal oxide, ~ 200 – 300 nm, is grown on the surface of the Si wires (Figure 6.1c). The array is infiltrated with a ~ 10 μm thick layer of PDMS at the base of the wires (Figure 6.1d), with the same method used to produce peeled, polymer-supported Si wire arrays (see Section 5.2.2). The oxide shell is then removed

from the exposed wire areas using buffered HF. The PDMS, which masks the underlying oxide from the HF etch, is subsequently removed by > 20 min in a 3:1 dimethylformamide: tetrabutylammonium fluoride etch,[157] leaving the SiO_2 layer intact (Figure 6.1e). This process has been experimentally demonstrated, yielding highly uniform p-Si wire arrays with an oxide sheath on the bottom ~ 10 μm of the wire (Figure 6.2). By casting additional layers of PDMS before the buffered HF etch, the length of this oxide shell can be tuned from 10 μm to the full length of the array.

The surface of the wires is next doped n-type to a depth of ~ 200 nm using a diffusion doping procedure (Figure 6.1f). This has been experimentally achieved by heating Si wire arrays to 850 ºC in the presence of n-type doping wafers (a phosphorus source) under carefully controlled conditions for 10 min. The oxide at the base of the array acts as a diffusion barrier, preventing the bottom of the wires from developing an n-type shell. The thin oxide barrier is therefore critical to enabling a back contact to the p-Si wire cores that does not form shunts through the n-Si shells. The doping process leaves a thin glass phase of high P concentration at the surface of the wires that must be removed. A surface etch and oxide etch treatment is used to remove < 50 nm of the wire surface as well as the oxide shell at the base of the rods (Figure 6.1g). Passivation of the Si wire surfaces could be included at this stage of the fabrication procedure as well. Surface recombination could be mitigated by methyl termination of the Si surface[52, 158] or by the conformal deposition of a thin amorphous Si layer.[21]

With the preparation of the absorber and emitter elements of the Si wires complete, the array is next embedded in a supporting matrix of transparent PDMS (Figure 6.1h).

The PDMS infill allows the wire array to be transferred from the single-crystal growth substrate to a flexible film, permitting the substrate to be recycled for the production of subsequent wire arrays (see Sections 4.2.2 and 4.3). Ideally, the thickness of the PDMS matrix should be precisely controlled and expose only the tips of the wires for an eventual front contact. This can be achieved by depositing the polymer in multiple thin layers (see Section 5.2.2) until the desired thickness is reached. However, uniformly exposing only the tip of the wire from the polymer layer requires that the wires be of identical length across the entire area. In practice, the wires tend to be longer near the edges of a sample and of a more uniform height across the interior area of the substrate. Producing polymer-embedded arrays with only the wire tips exposed could possibly be achieved by growing large areas of Si wire arrays in each growth run (i.e., an entire patterned Si wafer). Alternatively, if height variation across wire arrays is problematic, a planarization step could be added to the process between catalyst removal and growth of the thermal oxide on the wires by an infill with spin-on glass followed by chemomechanical polishing and then a wet chemical etch to remove the spin-on glass.[159] The PDMS infill could additionally be utilized to improve light absorption within the array by including scattering elements within the matrix during polymer deposition. Experiments with well-dispersed particles of alumina of ~ 1 μm diameter in the PDMS layer have shown promise as a way to increase absorption.

After the transfer of the wire array from the growth substrate to a PDMS film, front and back contacts must be applied to complete the solar cell (Figure 6.1i). The back contact should make an ohmic electrical connection between each p-Si core while reflecting light from between the wires back into the array. For the polymer-supported

wire array photoelectrodes of Chapter 5, this was accomplished by thermally evaporating Au onto the back of a freshly peeled film. For scalability and economic viability, the use of rare metals should be minimized (see Figure 3.1). If, however, a metal such as Au is deemed to be necessary for the formation of an ohmic contact on this structure, the amount required could be greatly reduced by plating it on the bottom of the wires by electroless deposition and then interconnecting the wires by evaporation of another more common metal. Ideally though, an Al layer would be evaporated on the back and the film heated at low temperature (< 200 ºC) to form a reflective, ohmic back contact with a single, earth-abundant material.[29] The back surface should be rough enough that the metal acts like a Lambertian reflector, which has been demonstrated to maximize the absorbance in Si wire arrays.[122] The top contact, on the other hand, needs to electrically connect the highly doped n-type emitter shells while being as transparent as possible. A sputtered indium tin oxide (ITO) layer could serve this function, but another transparent conducting oxide with more abundant elements, such as fluorine-doped tin oxide (FTO) or aluminum zinc oxide (AZO), would make the cell more scalable. Unfortunately, these oxides are fairly brittle and would likely crack significantly in a flexible device. If made highly conducting and thin enough, a conductive polymer (i.e., PEDOT: PSS) could potentially be a flexible, transparent top contact to the n^+-Si shell. PDMS has been made conductive (10^{-2} Ω-cm) by the incorporation of Ag nanoparticles into the matrix.[160] By replacement of the Ag with well-dispersed ITO nanoparticles or nanowires,[161] a flexible, transparent, conductive PDMS top contact may be possible. Alternatively, a nontransparent metal could interconnect the n-Si shells at the base of the emitter layer, leaving the majority of the wire length uncovered to absorb light (Figure 6.3). This

contacting scheme could be accomplished by deposition of the metal after embedding the array in a layer of PDMS just thicker than the p-Si wire base, then casting an additional thin PDMS layer, etching any excess metal off the exposed wires, and then fully embedding the rest of the array in supportive polymer before peeling the film and adding a back contact.

The final device would be an inexpensive, flexible, efficient solid-state Si wire array solar cell (Figure 6.4). Once the fabrication of the device is realized, its efficiency would be improved by optimizing the wire diameter and spacing. The optimal geometry would be one that gets the most voltage and photocurrent with the least amount of Si. Further efficiency gains would be sought by improvements in surface passivation and contacting methods.

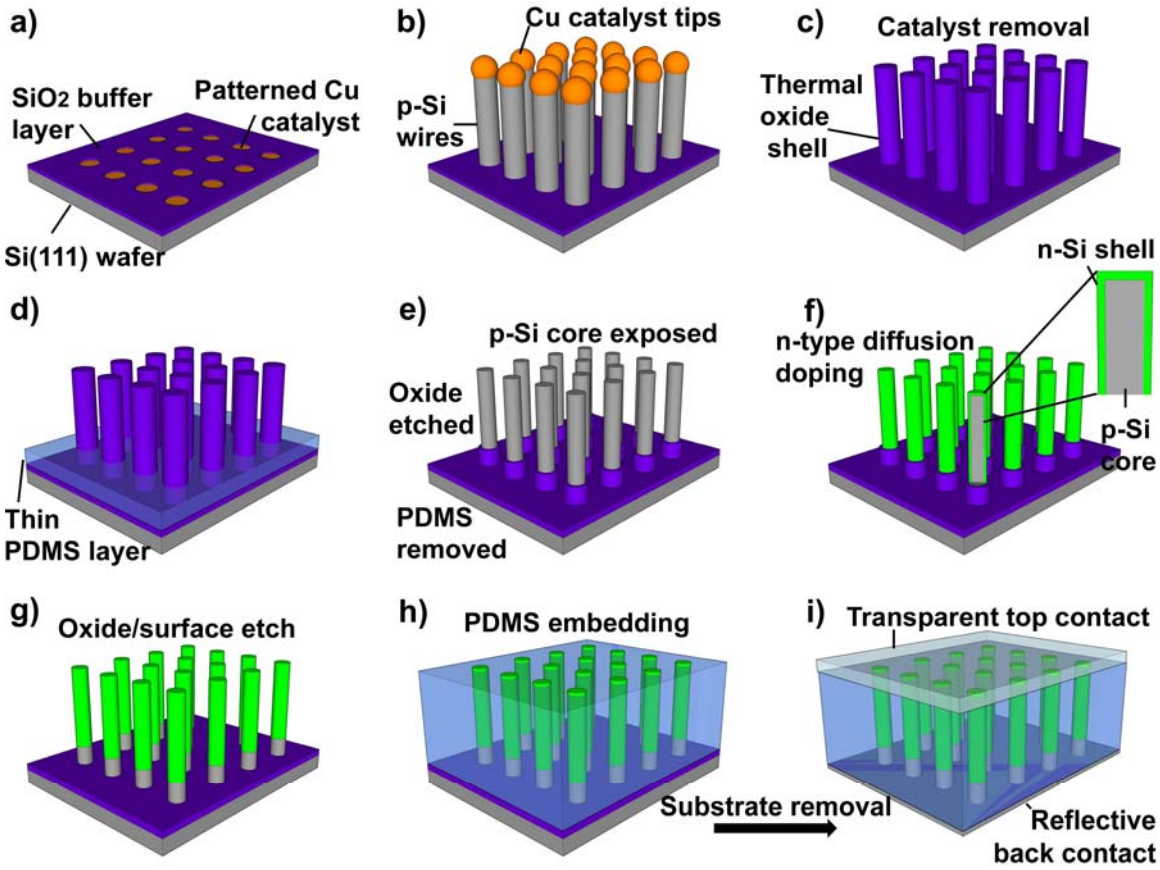

Figure 6.1. Schematic of the envisioned process for producing solid-state Si wire array solar cells. **(a)** A Si(111) wafer with patterned Cu catalyst in a buffered oxide template is used to grow **(b)** vertically aligned, p-Si wires, as previously demonstrated. **(c)** The catalyst tips are chemically removed and then a thermal oxide is grown on the wires. **(d)** A thin PDMS layer is cured at the base of the wires followed by **(e)** an oxide etch step and subsequent chemical removal of the PDMS, leaving an oxide shell at the base of the wires to act as a diffusion barrier. **(f)** A diffusion doping procedure is used to make an n-Si shell on the wire array above the oxide-covered base, and then **(g)** another etch is used to remove the surface layer. **(h)** The wire array is embedded in PDMS, leaving the tops of the wires exposed. **(i)** The PDMS/wire array composite film is removed from the substrate followed by the deposition of a reflective back contact and a transparent top contact.

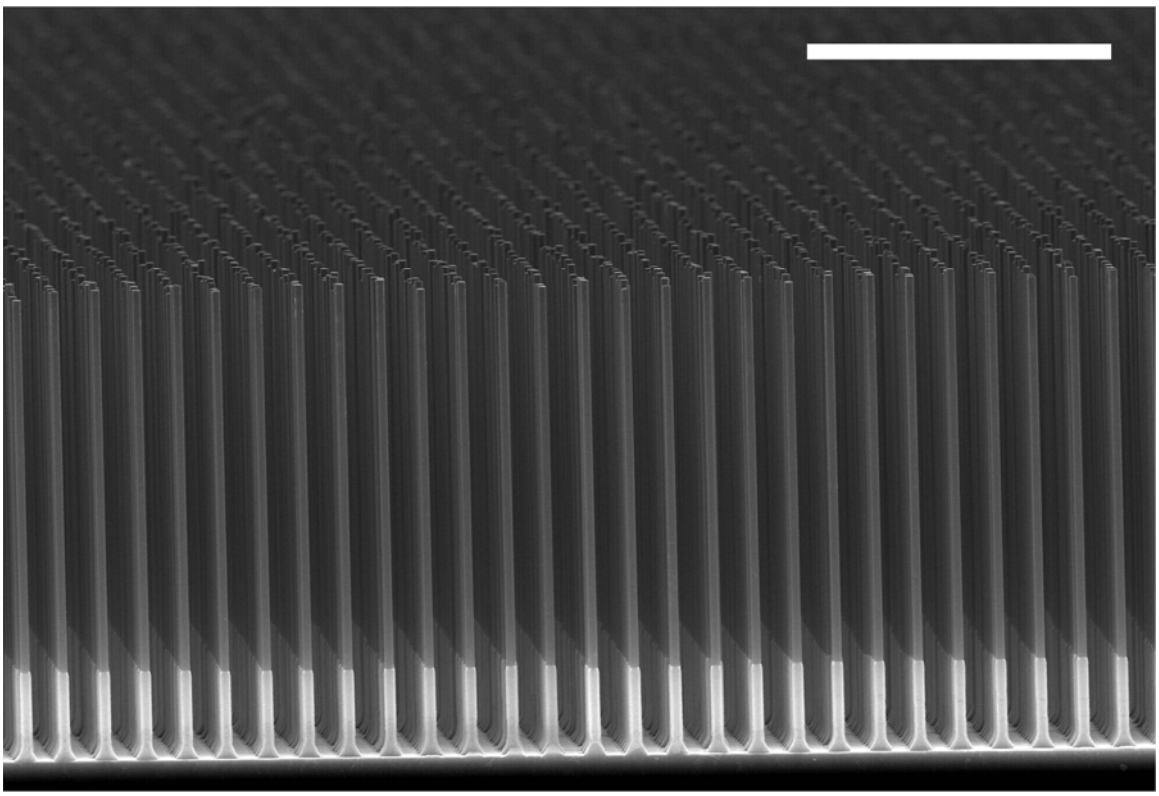

Figure 6.2. Si wire array with an oxide shell on the bases of the wires. Cross-sectional SEM image of an array that had a ~ 300 nm oxide shell thermally grown on the wires, followed by embedding in ~ 10 μm PDMS. The oxide above the PDMS film was etched away in buffered HF, and the PDMS was etched away in 3:1 dimethylformamide: tetrabutylammonium fluoride. Scale bar is 50 μm (image credit: S.W. Boettcher).

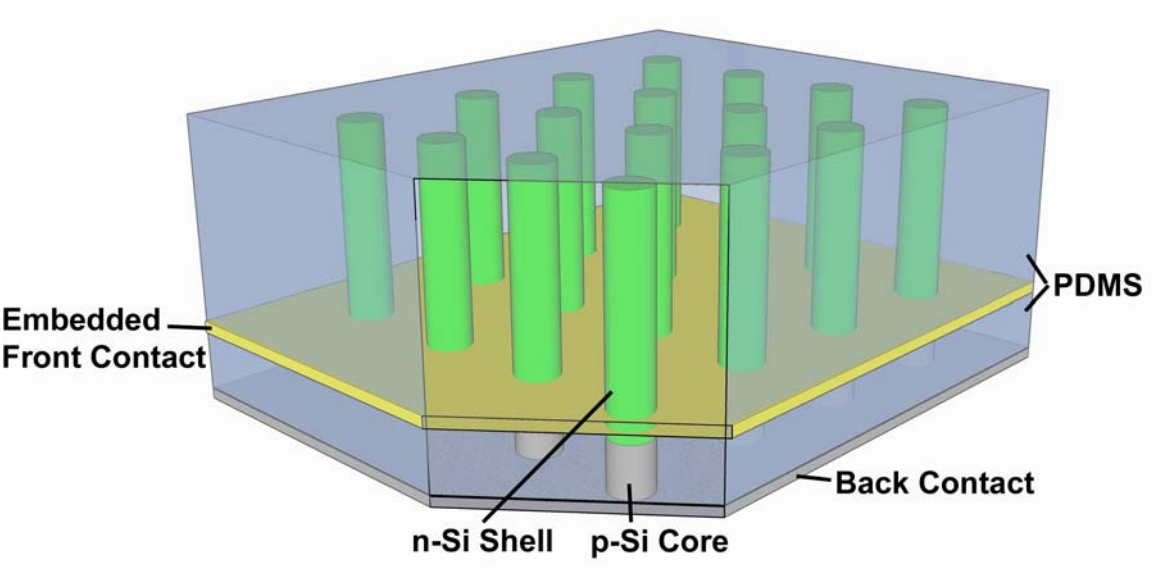

Figure 6.3. Embedded front contact scheme for a solid-state Si wire array solar cell. To avoid the need for a flexible, transparent front contact, a reflective metal could be placed at the bottom of the n-Si emitter layer instead.

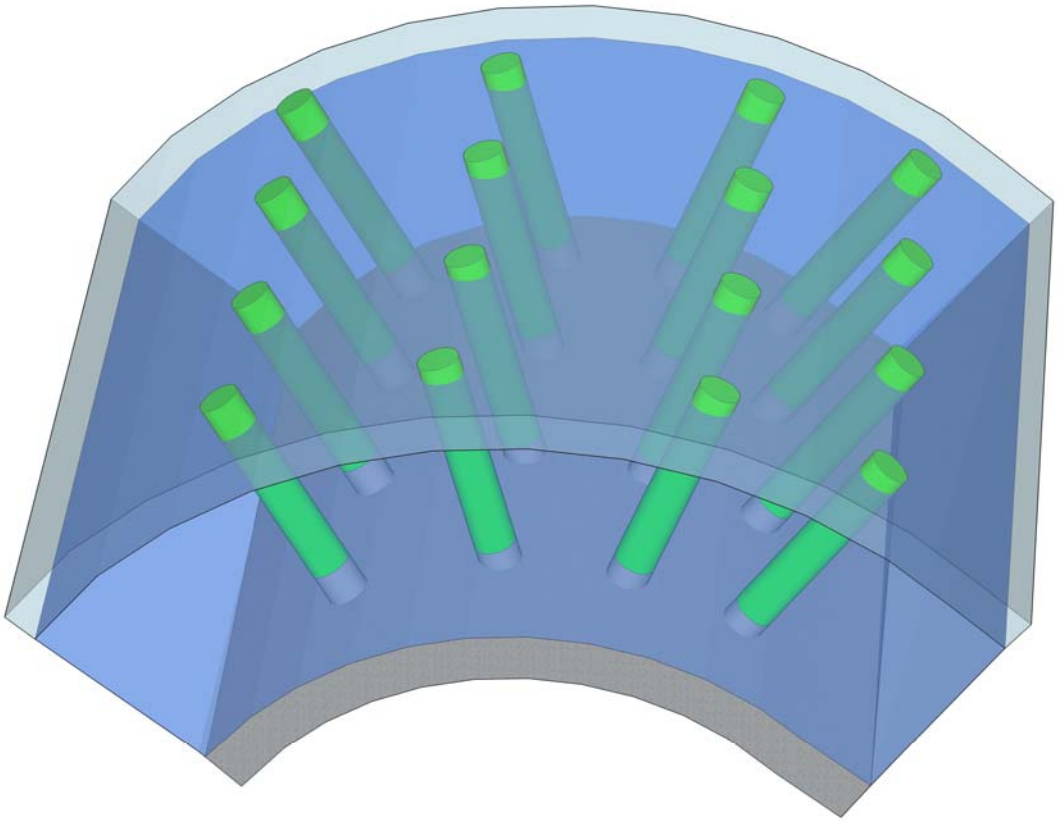

Figure 6.4. Flexible, solid-state Si wire array solar cell. Schematic of a core-shell pn-junction wire array embedded in transparent PDMS with a transparent top contact and reflective back contact. The composite film would have the benefits of a single-crystal inorganic semiconductor and a flexible organic material while using a fraction of the Si required in a planar arrangement.

6.1.3 Cost Comparison to Planar Si

While a thorough cost analysis is beyond the scope of this work and perhaps premature until a definite fabrication route is selected, some speculation of the manufacturing cost of the wire array solar cell compared to current planar Si technology can be made. Referring back to Figure 1.4, it is likely that the Si wire array solar cell could see significant cost savings in the areas of feedstock, ingot growth, and wafering. The primary feedstock for the wire array process is $SiCl_4$, an inexpensive chlorosilane that is

currently an unwanted byproduct. Rather than the growth of high-purity ingots, these wire arrays are grown with Cu catalyst, a fairly abundant metal, at atmospheric pressure without rigorous purification steps. The growth process is still fairly high temperature, but growth rates are high, too. Moreover, wafering expenses should be dramatically reduced as there are no kerf losses and a significantly lower volume of Si is required per cell area for wire array photovoltaics. It is unclear how cell processing costs would compare, as the wire array cell still involves high temperature doping and the integration of top and bottom contacts. The PDMS embedding steps should be low-cost because they involve an inexpensive polymer that could be applied in a roll-to-roll process. The substrate recycling procedure, although it adds some complexity, should greatly reduce the expense associated with using a single-crystal wafer. Module assembly costs would likely be comparable, except that as a flexible photovoltaic that could be rolled out, the wire array cell would not need expensive framing or glass. Finally, the balance-of-systems costs would likely be reduced as well. Although some increase in expense is possible in the wire array case because these cells would probably be somewhat lower in efficiency and would therefore need to cover a larger area to produce the same amount of energy, that cost would be offset by the significantly easier process required to install a system of lightweight, flexible wire array cells relative to a heavy, brittle crystalline system. Overall, the wire array solar cell design has the potential to substantially reduce the cost of manufacturing Si-based photovoltaics.

6.2 A Solar Water-Splitting Membrane Using Earth-Abundant Semiconductors in Radial Junctions

6.2.1 Water-Splitting Membrane Concept

Even if a revolution in the manufacture of photovoltaics successfully reduces the cost of solar electricity to a level that is economically competitive with fossil fuels, the widespread implementation of solar as a primary energy source will require the ability to overcome the diurnal variation of sunlight in a given region. In order to have energy from the sun at night, a cost-effective storage mechanism is needed. The use of batteries to store electricity could work in principle, but all current battery technologies are too expensive. Mechanical storage methods, such as pumping water uphill or compressing gases, are a possibility, but this approach would require enormous reservoirs to be filled and emptied everyday (i.e., a pumping capacity of > 5000 Hoover Dams to meet U.S. energy demand).[11] The ideal solution would be to store solar energy in the form of chemical bonds – to convert sunlight into an energy-dense fuel. Nature utilizes this approach through the mechanism of photosynthesis. However, the energy conversion and storage efficiency of even the most rapidly growing plant is < 0.5%.[11] Higher efficiencies should be possible in an artificial photosynthesis device that does not divert energy to rebuild complicated biological systems as a plant must do. For instance, solar photoelectrolysis has been demonstrated at conversion efficiencies up to 18.3% using AlGaAs/Si bipolar band gap cells with RuO_2 and Pt catalysts.[162, 163] Unfortunately, this cell is far too expensive to be a practical energy storage solution. Combining electrolyzers directly with photovoltaics has not been cost-effective on a large scale either

due to the need for wires and expensive catalysts. Instead, a scalably manufacturable device using only earth-abundant elements is needed that is significantly more efficient than plants at generating fuel from sunlight.

We have developed a credible scheme to accomplish this goal by building a water-splitting membrane that uses the advantages of radial junctions. Figure 6.5 demonstrates how this membrane would work. The electrolysis of water into hydrogen and oxygen thermodynamically requires 1.23 V, with overpotential losses driving the necessary potential even higher. To split water directly from the photovoltage of a semiconductor, there is an additional requirement that the conduction and valence band energy levels must straddle the oxidation and reduction potentials of the electrolysis reaction. Meeting these requirements while simultaneously being efficient, stable, and earth-abundant is a lot to expect from a single material. No known semiconductor currently satisfies all of these criteria effectively. The proposed membrane would therefore use two separate materials in series to build the photovoltage needed to split water. Rather than relying on one very wide band gap material that could only use UV light, the device would make more efficient use of the solar spectrum by employing a wider band gap photoanode material that would absorb higher energy light while transmitting lower energy light to be absorbed by a narrower band gap photocathode material. The two semiconductors would be electrically connected to each other through an ion exchange membrane that would be impermeable to hydrogen and oxygen gases while allowing the transfer of protons. The ion exchange function is necessary to prevent the buildup of a pH gradient. Both semiconductors would be in the form of wire arrays, with the radius tuned to the minority-carrier collection length of the material and the length adjusted for optimal light

absorption. The spacing of the wires would be optimized for the tradeoff between optical absorption and mass transport (i.e., bubble formation and the removal of gaseous products from the array). The wire surfaces would be decorated with bonded multi-electron transfer catalysts to drive the oxidation and reduction reactions at low overpotentials. By shaping the semiconductors as wire arrays, lower-purity materials can be used and spaces are created for ion transfer across the membrane. Furthermore, charge-carriers will be distributed over a larger area, reducing the turnover frequency at catalyst sites and lowering the necessary activity of those catalysts. This will allow more earth-abundant materials to be candidates for the catalysis of the reaction. The product gases would be collected, with oxygen vented to the atmosphere and hydrogen collected for use as a fuel.

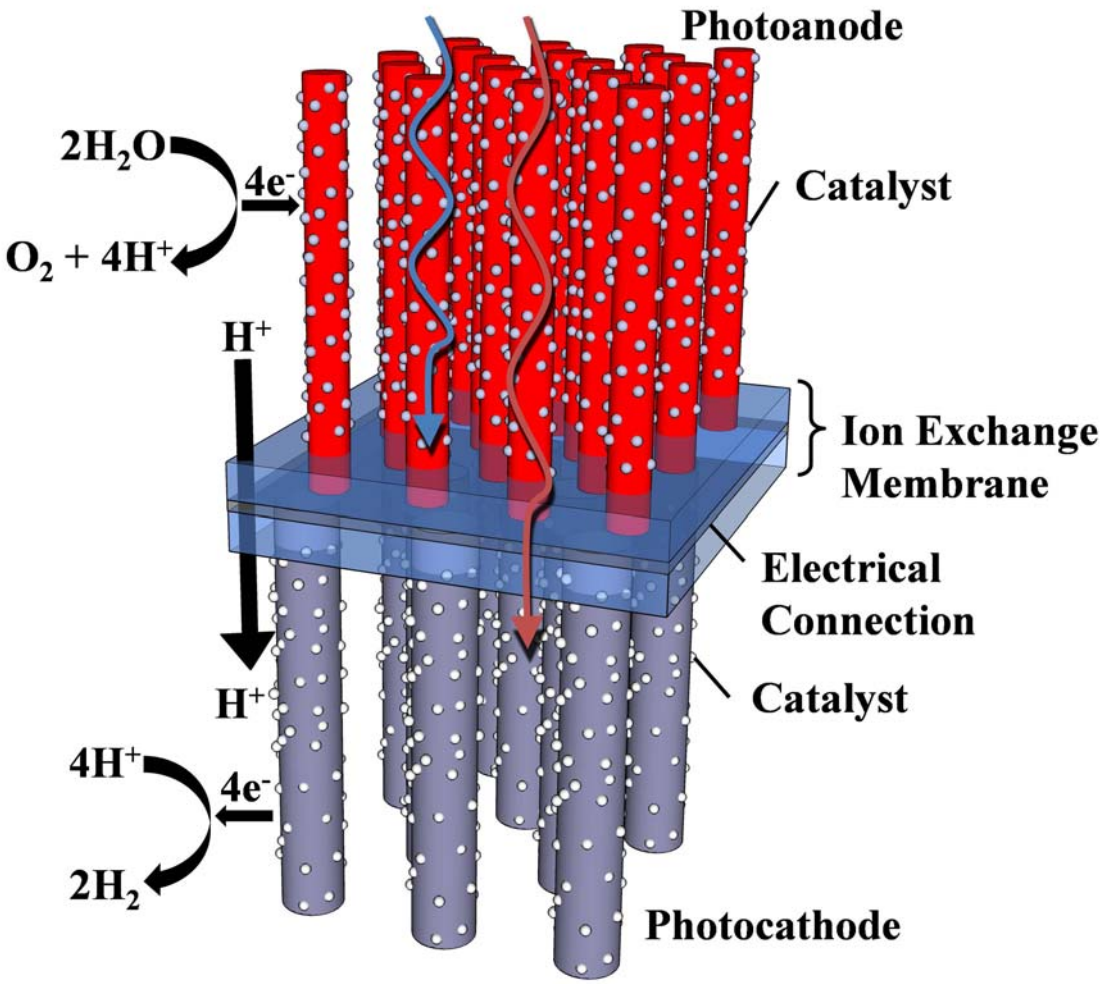

Figure 6.5. Schematic of a water-splitting device to generate fuel from sunlight. The device uses two different semiconductors, a wider band gap anode material and a narrower band gap cathode material, to produce the > 1.23 V necessary to electrolyze water. The anode material absorbs higher energy light, allowing lower energy light to be absorbed by the cathode. The two semiconductors are electrically connected in a transparent membrane that is impermeable to H_2 and O_2 but allows proton transfer. The semiconductors are radial junction arrays in order to utilize lower-purity materials, to distribute charge-carriers over a larger area so that the catalyst turnover requirement is lower, and to allow proton transfer across the membrane. H_2 is collected on the cathode side and O_2 is vented to the atmosphere from the anode side. The image is not to scale.

6.2.2 Photocathode

The photocathode material must be stable under the reducing environment on its side of the cell and have a conduction band edge energy sufficiently negative of the formal potential to produce hydrogen from water in order to make the reaction energetically favorable. One material that could fulfill this role is p-type Si, which is cathodically stable under illumination in aqueous conditions,[164] has its conduction band edge well-positioned relative to the reduction potential to produce hydrogen, and can be coupled to effective catalysts. The work report herein on Si wire arrays (Chapters 3-5) is thus directly applicable to producing a photocathode for this solar fuel generating membrane. Although Pt is the most active catalyst for H_2 production currently known, other earth-abundant metals such as Ni or Co may be effective on these arrays due to the lower flux of charge-carriers through a given area relative to a planar surface. These metals have already been demonstrated as catalysts for hydrogen evolution in conjunction with p-Si.[165]

6.2.3 Photoanode

The photoanode material must be stable under the oxidizing environment on its side of the cell and have a valence band edge energy sufficiently positive of the water oxidation potential to make the reaction energetically favorable. With these criteria, metal oxide semiconductors are favorable because their valence band edges are normally quite positive of the water oxidation potential and because the metal atoms are already in their highest oxidation state. The drawback of many metal oxides is that their band gaps are

too large (> 3 eV) to make efficient use of the solar spectrum and their minority-carrier diffusion lengths are too low for efficient charge-carrier collection.

Although the search for a metal oxide of ideal properties is ongoing, WO_3 is a promising candidate to meet the requirements of the photoanode material. It has a band gap that can absorb much of the visible spectrum (E_g = 2.6 eV)[65] and can be tuned lower by the addition of other metals such as Mo.[166, 167] The minority-carrier diffusion length of WO_3 (up to 10^{-6} m),[168] though short, is longer than most other metal oxide candidate materials for the photoanode. By utilizing WO_3 in a radial junction structure, efficient charge-carrier collection should be possible.

Nanostructured WO_3 for the photoanode could be fabricated by several routes. The most straightforward method to produce wire arrays would be to employ templating techniques, such as the AAO approach described earlier (see Section 2.2.1). W metal could be cathodically electrodeposited and oxidized after removal of the template, or WO_3 (with a Mo fraction) could be electrodeposited into the template directly.[166, 167] In the latter case, a wet chemical etch would be needed that would selectively dissolve the alumina template but not the metal oxide semiconductor rods. Alternatively, a porous film of WO_3, the inverse of a wire array, would accomplish the same task provided that it allowed for sufficient mass transport and transmittance of light to the photocathode (Figure 6.6). Porous WO_3 can be made from the anodization of tungsten foil in a process similar to the fabrication of AAO templates.[169]

Whether the photoanode is a wire array or a porous film, it will need to be decorated with oxygen-evolving catalyst. Finding an earth-abundant catalyst that drives the oxidation of water at low overpotential is one of the largest challenges inherent in the

water-splitting membrane design. Initial research would focus on Co_3O_4 colloids, which are known to be fairly active and stable water oxidation electrocatalysts.[170]

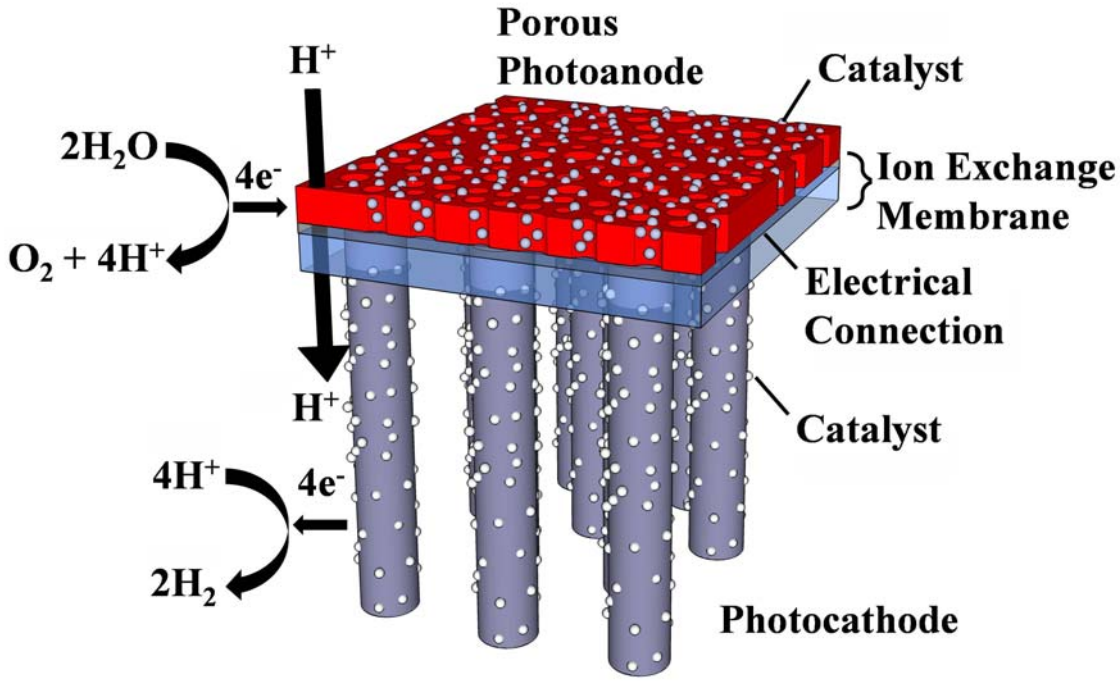

Figure 6.6. Schematic of a water-splitting device using a porous film as a photoanode. While the initial photocathode candidate material, p-Si, can now readily be fabricated into wire arrays of tunable dimensions, the initial photoanode material, WO_3, has not been explored as heavily. Porous anodic WO_3 films could be used as an alternative to metal oxide wires provided that they could be readily incorporated into the membrane device in a way that allowed for sufficient mass transport and transmittance of light to the photocathode.

6.2.4 Membrane and Device Assembly

The membrane layer between the two semiconductor electrodes must fulfill a number of important functions for the device to split water sustainably. It must simultaneously provide structural support for the wire arrays, separate the gaseous hydrogen and oxygen products, enable an ohmic conduction path for electrons between the anode and cathode,

and act as an ion-exchange medium for the protons involved in the electrochemical reaction, all while being optically transparent enough to ensure that light is effectively absorbed by both semiconductor assemblies. There are several approaches that will be explored to meet this daunting challenge.

In its essential functions, the envisioned water-splitting membrane acts as a proton exchange membrane (PEM) fuel cell operating in reverse. The membrane of PEM fuel cells must also be impermeable to hydrogen and oxygen gases while allowing efficient proton exchange. The material most commonly used in these membranes is perfluorosulphonic acid polytetrafluoroethylene copolymer, known as Nafion.[171] Fortunately, Nafion is commercially available and highly transparent when cast from solution. To test the possibility of using Nafion directly as the ion-exchange membrane for the water-splitting device, it was spin-coated from a solution (5% w/w Nafion/alcohol mixture, Alfa Aesar) onto a Si wire array, left to dry for > 2 hr, and then peeled from the substrate using a razor blade. Figure 6.7 shows the resulting Si wire array/Nafion composite film. Although the casting and peeling procedure with Nafion is still unoptimized, a Si wire array with the majority of the wire length exposed can be peeled in a structurally supportive thin film. The thin Nafion layer is not as robust as equivalent PDMS films, but the Nafion does appear to make intimate contact with the wires (Figure 6.7d). To make the full device, each wire array would be peeled in a Nafion film, thin layers of an appropriate metal would be electrolessly deposited on the back of the wire bases to establish an ohmic contact, and the two sides of the membrane would be carefully sealed together using a third, electrically conducting Nafion layer. The middle layer of Nafion would be made conducting by the addition of conjugated polymer chains

or Ag nanoparticles to the extent permitted without substantial degradation of the transparency or ion-exchange capability of this thin film. Well-dispersed nanoparticles may even be beneficial as light scatterers. Alternatively, Nafion or a similar ion-exchange material could be applied by layer-by-layer deposition methods, utilizing the capabilities of that technology to make the material connecting the wire arrays conductive.[172]

In the event that a single material to accomplish the membrane's functions becomes infeasible, a combination of several materials could be used instead (Figure 6.8). In this multi-component membrane, the wires would be peeled from their growth substrates in a structurally supportive polymer to make the water-splitting device mechanically robust. PDMS, as it has already been demonstrated with Si wires (see Section 4.2.2), would be ideal to fulfill this role, although the surface would need to be functionalized to make it hydrophilic and thus permit the aqueous medium to penetrate the array. The two peeled wire arrays would be connected by a layer of conductive polymer (i.e., PEDOT, polypyrrole, etc.), thin enough to be transparent and polymerized or cured between the PDMS layers to adhere them together. Finally, the ion-exchange capability would be provided by Nafion or a similar polymer interspersed throughout the membrane as proton-conducting channels. This structure could possibly be fabricated by selectively removing areas of the membrane with reactive ion etching through a shadow mask, followed by polymer deposition into the resulting pores.

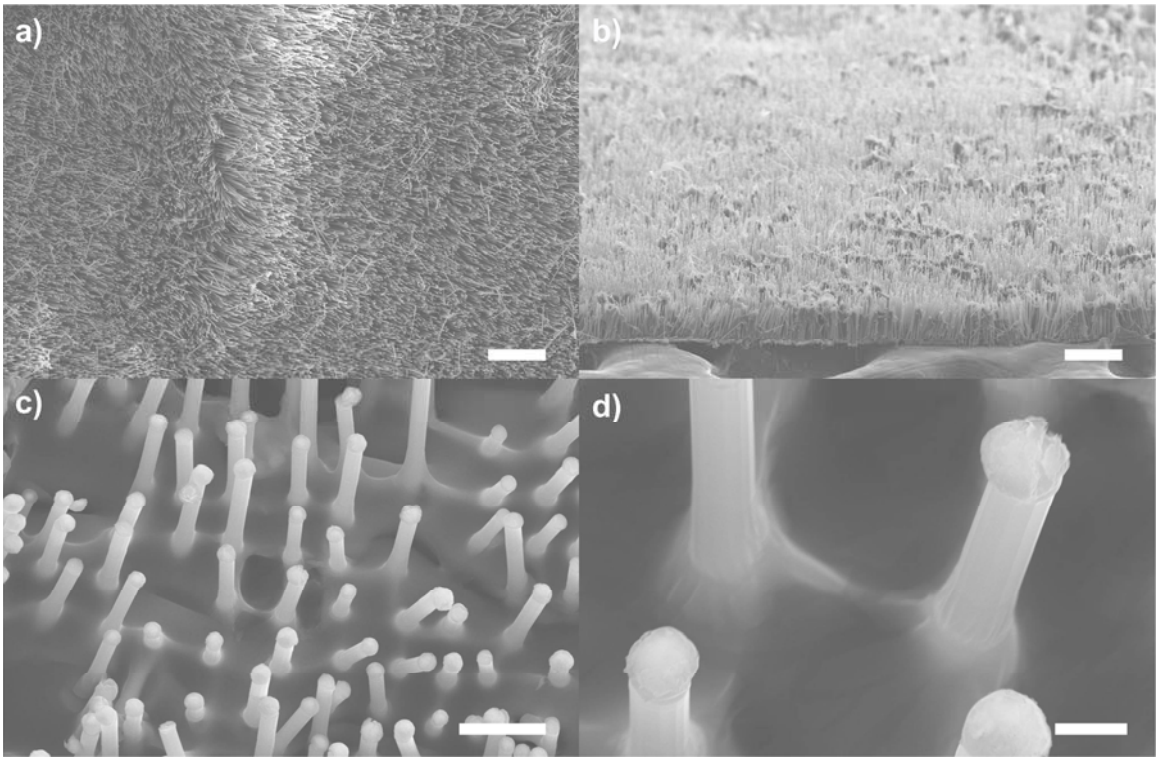

Figure 6.7. Si wire arrays embedded in thin Nafion films. The array **(a)** was uniform over a large area, **(b)** could be peeled from the substrate in a thin polymer film, **(c)** had most of the wire length exposed from the Nafion, and **(d)** made intimate contact with the polymer. Scale bar is 100 μm for **(a,b)**, 20 μm for **(c)**, and 2 μm for **(d)**.

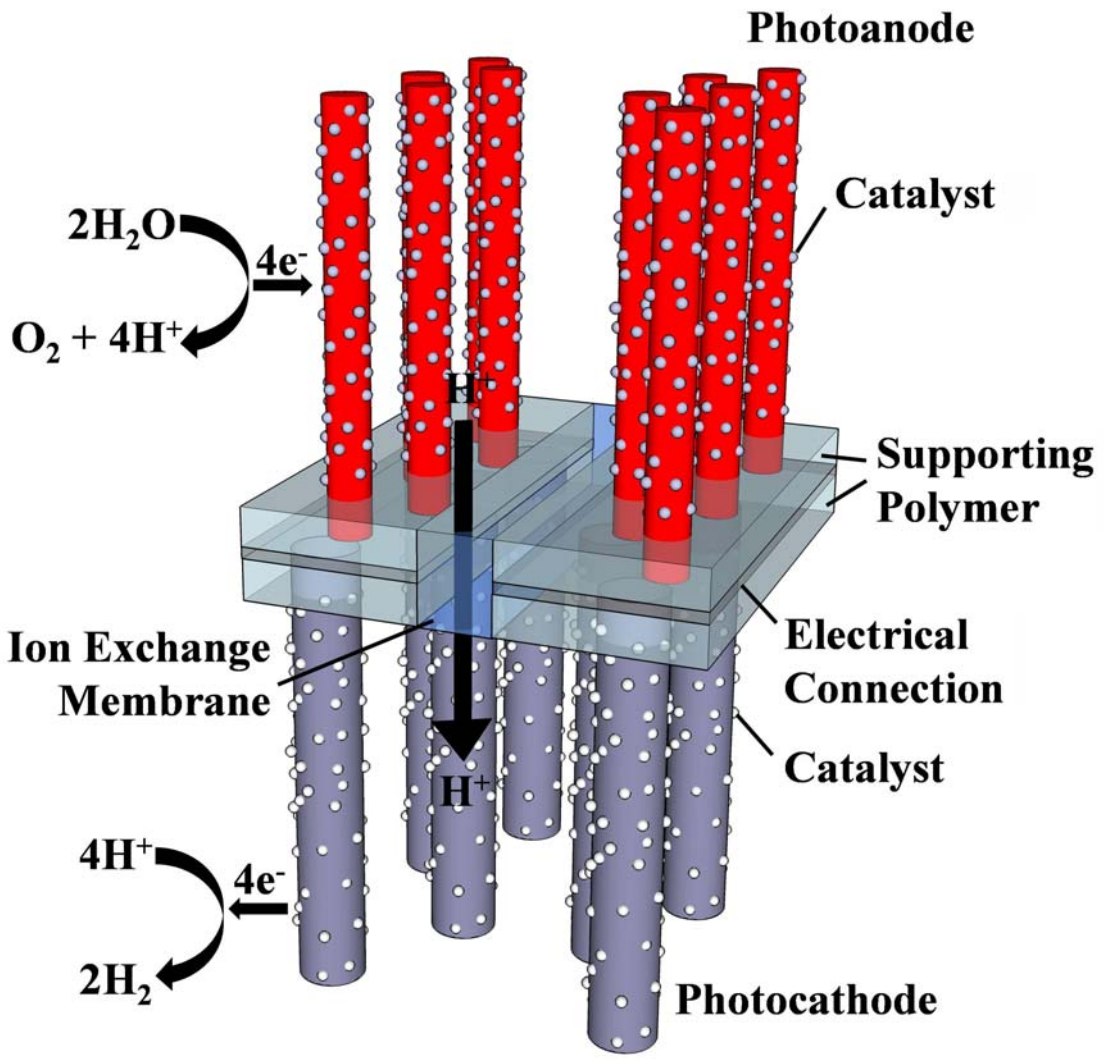

Figure 6.8. Schematic of a water-splitting device using a multi-component membrane. In this version of the device, the membrane is composed of three separate polymers serving three different functions. A structurally supportive polymer at the base of the semiconductor wires gives the device mechanical stability while a conducting polymer provides the electrical connection between the electrodes. A third polymer, interspersed in regions throughout the membrane, allows ion-exchange to occur.

6.2.5 Design Modularity

One of the greatest advantages of the design of this device, from a developmental point of view, is its modularity. Individual components, such as the anode, cathode, membrane, and catalysts, can be studied and improved independently of each other. This added degree of freedom allows multiple researchers to work on different aspects of the device simultaneously, greatly accelerating its development. While the final design of the device may change as improvements and discoveries are made, we expect that the end water-splitting membrane will resemble the image shown in Figure 6.9. The success of this device, which would store sunlight as a chemical fuel, would be a large step towards making solar a viable primary energy source.

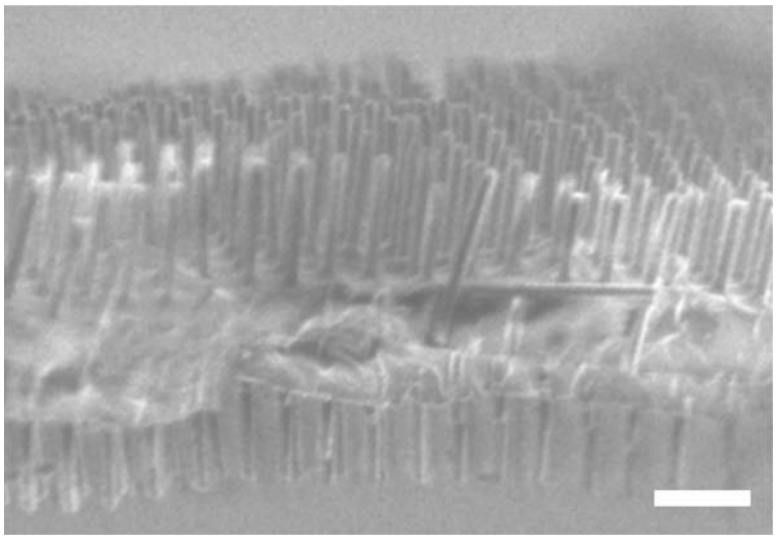

Figure 6.9. Back-to-back polymer-supported semiconductor wire arrays for a sunlight-driven fuel-generating system. Cross-sectional SEM image of two PDMS-supported Si wire arrays adhered to each other. A final water-splitting device with two semiconductor wire arrays in an ion-exchange membrane may resemble this structure. Scale bar is 20 μm.

6.3 Thesis Summary

This thesis has summarized our findings over the last several years fabricating and studying wire array solar cells. The radial junction project has progressed a long way since its inception. Based on our experience and successes to date, we believe it can go much further still.

In the introductory chapter, we explored the global energy situation and how it relates to the ongoing climate change threat. We then evaluated the available carbon-free energy sources and concluded that solar energy must play a vital role in displacing fossil fuels. A cost breakdown of the dominant photovoltaic technology was provided, followed by an explanation of the radial junction concept and how it could potentially lead to less expensive solar cells primarily by reducing feedstock and materials costs. We also discussed the results of modeling on radial junctions, as well as potential ways to fabricate such semiconductor structures and an overview of work that has already been reported on them.

In Chapter 2, we demonstrated the fabrication of Cd(Se, Te) nanorod arrays and compared their photoelectrochemical behavior to analogously produced planar cells. Among the key findings was that the nanorod array open-circuit voltage was significantly lower than that of the planar electrode due to the increased junction area of the device and the increased effects of surface recombination. Nanorod arrays exhibited reduced short-circuit current density as a result of a lower optical filling fraction but generally displayed better fill factors than the planar electrodes. Importantly, spectral response studies demonstrated that nanorod arrays were able to maintain their carrier-collection efficiency

better than planar cells at lower energy, more deeply penetrating wavelengths of light. This observation indicated that the radial junction was allowing better charge-carrier collection at a low minority-carrier diffusion length.

In Chapter 3, we explained why Si would be an ideal candidate for improvement through an architecture employing radial junctions. We discussed the evolution of our approach for the fabrication of controllable, uniform Si wire arrays. Attempts were made to control the dimensions of Si wires by confining them within porous alumina templates during growth. As the need for larger diameter wires became more apparent, wires were increasingly grown by the VLS method without confinement on an epitaxial growth substrate. Better control and growth rates were eventually achieved by switching from SiH_4 to a $SiCl_4$ gas precursor at higher temperatures in conjunction with a lithographically patterned thermal oxide buffer layer on the substrate surface. We demonstrated that uniform Si wire arrays of tunable diameter, length, and spacing could be grown this way from several different catalyst metals. We also demonstrated a general approach using the electrodeposition of catalyst to produce larger diameter, more densely packed wire arrays.

In Chapter 4, we addressed the paradox of using single-crystal growth wafers to fabricate lower-purity Si wire arrays. A scheme was demonstrated to transfer the wire arrays to low-cost polymer films and then recycle the growth substrate for the production of subsequent wire arrays. PDMS-embedded Si wire films maintained the long-range order and alignment of the array while being both durable and flexible. Initial

experimental attempts to densify the wire pattern within the polymer after its removal from the substrate resulted in some success but still require further development.

In Chapter 5, we studied the photoelectrochemical energy-conversion properties of peeled, polymer-supported p-Si wire arrays and compared them to p-Si wire arrays still epitaxially attached to the growth substrate as well as to p-Si planar wafers. The performance of polymer-supported wire arrays was found to be comparable to substrate-attached arrays, both of which displayed better energy-conversion properties than previously reported Si wire array solar cells. Compared to substrate-attached arrays, polymer-supported arrays had similar open-circuit voltages, better fill factors, and slightly lower external quantum efficiencies due to the partial coverage of the wire surface with polymer. All Si wire arrays measured had external quantum efficiencies several times higher than their packing fraction, indicating light trapping and optical concentration within the wires in agreement with previous absorption studies. Furthermore, we showed that high currents within wire arrays should be possible by increasing light absorption, as evidenced by increased external quantum efficiencies (> 0.6) at high angles of incidence.

In this concluding chapter, we discussed two major directions of future research for semiconductors with wire array geometries. The first is to produce an efficient solid-state Si wire array solar cell, which is a logical extension of the work on Si wire arrays presented herein. We described in detail a plan for the fabrication of a solid-state solar cell that should be flexible and reasonably efficient and discussed how the cost of its manufacture would likely compare to current planar Si technology. Because of

significant savings over planar Si in the areas of feedstock, ingot growth, and wafering, this solar cell, if efficient enough, has the potential to be significantly less expensive. We continued by discussing the application for semiconductor wire arrays in a sunlight-driven, water-splitting membrane for the production of chemical fuel. Wire arrays, at both the anode and cathode of this device, would enable the use of low minority-carrier diffusion length materials and possibly allow earth-abundant catalysts by spreading the charge-carriers over a larger area, thereby lowering the activity requirement at catalyst sites. The successful, sustainable operation of a solar fuel-generating membrane would provide an energy-dense storage mechanism for sunlight, which is critical to deploying the solar resource as a primary energy source for the planet.

This thesis has demonstrated that it is possible to fabricate semiconductor wire arrays in a potentially high-throughput, low-cost method that results in an inorganic material in a flexible film form without sacrificing the electronic quality of the material. The primary future direction of this research is to integrate these Si wire array/PDMS composite films into a solid-state solar cell and optimize its efficiency. Advancements in the device will be possible through improving contacts, increasing the voltage by using larger diameter wires with passivated surfaces, ensuring high fill factors by eliminating surface impurities and shunts, and maximizing light absorption with an optimal packing density, a back reflector, and an antireflection layer. If experimental efficiencies in the range of theoretical predictions can be achieved, this technology could have an enormous impact on the photovoltaics market.

Appendix

Derivation of Equations 3.1, 3.2, and 3.7

The catalyst tip at the top of a VLS-grown wire shown schematically in Figure 3.8a is isolated below in Figure A.1.

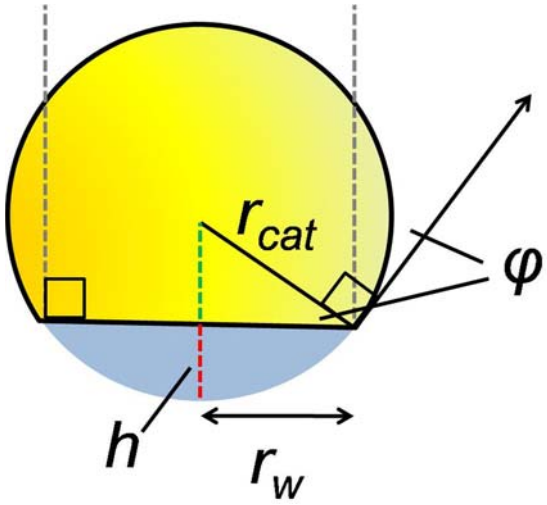

Figure A.1. Schematic of the catalyst tip on a VLS-grown wire.

As Figure A.1 shows, the angle, φ, between the liquid-vapor interface and the direction of wire growth is the same as the angle between r_{cat} (as drawn) and r_w, leading to the relation:

$$r_w = r_{cat} \cos\varphi \tag{A.1}$$

which is Equation 3.1 relating the wire radius to the catalyst tip radius. The volume of the catalyst tip, V_{cat}, can be determined by recognizing that the ball is a truncated sphere. The missing section of the sphere, shown in blue in Figure A.1, is a spherical cap. The

formula for the volume of a spherical cap is known and is (using the variables in Figure A.1):

$$V_{spherecap} = \frac{\pi}{6}\left(3r_w^2 + h^2\right)h \tag{A.2}$$

Where $V_{spherecap}$ is the volume of the spherical cap, h is the height of the cap, and r_w is the radius of the cap (equal to the VLS-grown wire radius in this case). Recognizing that:

$$\sin\varphi = \frac{r_{cat} - h}{r_{cat}} \tag{A.3}$$

and rearranging gives:

$$h = r_{cat}\left(1 - \sin\varphi\right) \tag{A.4}$$

The catalyst tip volume is the volume of the entire sphere minus the spherical cap:

$$V_{cat} = \frac{4}{3}\pi r_{cat}^3 - \frac{\pi}{6}\left(3r_w^2 + h^2\right)h \tag{A.5}$$

Substituting into Equation A.5 with Equations A.1 and A.4 yields:

$$V_{cat} = \frac{4}{3}\pi r_{cat}^3 - \left[\frac{\pi}{6}\left(3r_{cat}^2\cos^2\varphi + r_{cat}^2\left(1-\sin\varphi\right)^2\right)r_{cat}\left(1-\sin\varphi\right)\right] \tag{A.6}$$

which simplifies to Equation 3.2:

$$V_{cat} = \frac{4}{3}\pi r_{cat}^3\left[1 - \frac{1}{8}\left(3\cos^2\varphi + \left(1-\sin\varphi\right)^2\right)\left(1-\sin\varphi\right)\right] \tag{A.7}$$

The truncated-cone shape of Figure 3.8b that is etched into the oxide buffer layer of the substrate is shown again in Figure A.2. Because the buffered HF etches SiO_2 isotropically, it etches to the side at the same rates it etches downward. This gives the sloping edge a 45° angle and makes the height of the cone equal to its radius. The

volume of the truncated cone that will be occupied by catalyst is equal to the entire cone minus the imaginary extended cone tip that would project beyond the oxide layer:

$$V_{cat} = \frac{1}{3}\pi\left(t_{cat} + r_h\right)^3 - \frac{1}{3}\pi r_h^3 \tag{A.8}$$

which simplifies to Equation 3.7:

$$V_{cat} = \frac{1}{3}\pi\left[t_{cat}^3 + 3t_{cat}^2 r_h + 3t_{cat} r_h^2\right] \tag{A.9}$$

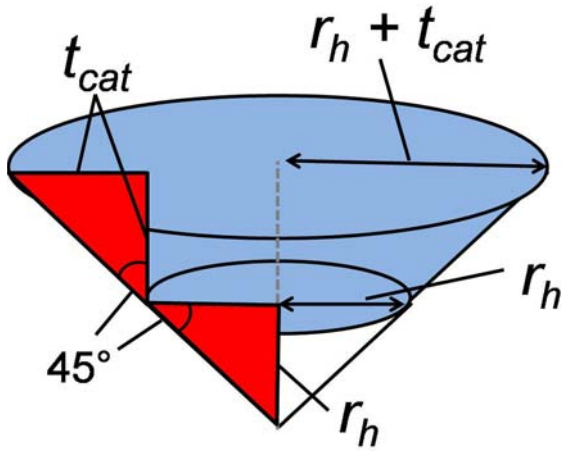

Figure A.2. Schematic of the truncated-cone hole etched into the buffered oxide layer.

References

1. Energy Information Administration, U. S. Department of Energy, *World Energy Consumption of Primary Energy by Energy Type and Selected Country Groups, 1980 - 2006*, (2008).
2. Energy Information Administration, U. S. Department of Energy, *International Energy Outlook 2009*, (2009).
3. Bernstein, L., et al., Climate Change 2007: Synthesis Report. Technical report, Intergovernmental Panel on Climate Change. (2007).
4. Hoffert, M. I., Caldeira, K., Jain, A. K., Haites, E. F., Harvey, L. D. D., Potter, S. D., Schlesinger, M. E., Schneider, S. H., Watts, R. G., Wigley, T. M. L. and Wuebbles, D. J., Energy implications of future stabilization of atmospheric CO_2 content. *Nature* **395**, 6705, 881-884 (1998).
5. Caldeira, K., Jain, A. K. and Hoffert, M. I., Climate sensitivity uncertainty and the need for energy without CO_2 emission. *Science* **299**, 5615, 2052-2054 (2003).
6. Hoffert, M. I., Caldeira, K., Benford, G., Criswell, D. R., Green, C., Herzog, H., Jain, A. K., Kheshgi, H. S., Lackner, K. S., Lewis, J. S., Lightfoot, H. D., Manheimer, W., Mankins, J. C., Mauel, M. E., Perkins, L. J., Schlesinger, M. E., Volk, T. and Wigley, T. M. L., Advanced technology paths to global climate stability: Energy for a greenhouse planet. *Science* **298**, 5595, 981-987 (2002).
7. Cox, P. M., Betts, R. A., Jones, C. D., Spall, S. A. and Totterdell, I. J., Acceleration of global warming due to carbon-cycle feedbacks in a coupled climate model. *Nature* **408**, 6809, 184-187 (2000).
8. Herzog, H., Eliasson, B. and Kaarstad, O., Capturing greenhouse gases. *Sci.Am.* **282**, 2, 72-79 (2000).
9. Kheshgi, H. S., Flannery, B. P., Hoffert, M. I. and Lapenis, A. G., The effectiveness of marine CO_2 disposal. *Energy* **19**, 9, 967-974 (1994).
10. Sailor, W. C., Bodansky, D., Braun, C., Fetter, S. and van der Zwaan, B., Policy forum - Nuclear power - A nuclear solution to climate change? *Science* **288**, 5469, 1177-1178 (2000).
11. Lewis, N. S. and Nocera, D. G., Powering the planet: Chemical challenges in solar energy utilization. *Proc. Natl. Acad. Sci. U. S. A.* **103**, 43, 15729-15735 (2006).
12. Tomabechi, K., Gilleland, J. R., Sokolov, Y. A. and Toschi, R., ITER conceptual design. *Nucl. Fusion* **31**, 6, 1135-1224 (1991).
13. *World Energy Assessment, 2000*, (ed. Goldemberg, J.) (United Nations Development Programme, New York, 2000).
14. Lewis, N. S., *Powering the Planet*, (2005) (http://nsl.caltech.edu/energy.html).
15. Becquerel, A.E., Mémoire sur les effets électriques produits sous l'influence des rayons solaires. *Comt. Rend. Acad. Sci.* **9**, 561-567 (1839).
16. REN21, *Renewables Global Status Report: 2009 Update*, (REN21, Renewable Energy Policy Network for the 21st Century, Paris, 2009) (http://www.ren21.net/pdf/RE_GSR_2009_Update.pdf).

17. *World Energy Assessment Overview, 2004 Update*, (ed. Goldemberg, J.) (United Nations Development Programme, New York, 2004).
18. Lewis, N. S., Toward cost-effective solar energy use. *Science* **315**, 5813, 798-801 (2007).
19. Gratzel, M., Photovoltaic and photoelectrochemical conversion of solar energy. *Philos. Trans. R. Soc. A-Math. Phys. Eng. Sci.* **365**, 1853, 993-1005 (2007).
20. del Canizo, C., del Coso, G. and Sinke, W. C., Crystalline silicon solar module technology: Towards the 1 EUR per watt-peak goal. *Prog. Photovoltaics* **17**, 3, 199-209 (2009).
21. Goetzberger, A., Hebling, C. and Schock, H. W., Photovoltaic materials, history, status and outlook. *Mater. Sci. Eng. R-Rep.* **40**, 1, 1-46 (2003).
22. Muller, A., Ghosh, M., Sonnenschein, R. and Woditsch, P., Silicon for photovoltaic applications. *Mater. Sci. Eng. B-Solid State Mater. Adv. Technol.* **134**, 2-3, 257-262 (2006).
23. Solarbuzz, *Solar Module Price Highlights: August 2009*, (2009) (http://www.solarbuzz.com/Moduleprices.htm).
24. Jester, T. L., Crystalline silicon manufacturing progress. *Prog. Photovoltaics* **10**, 2, 99-106 (2002).
25. *Handbook of Photovoltaic Science and Engineering*, (eds. Luque, A. & Hegedus, S.) (John Wiley & Sons, 2003).
26. Nemet, G., *Learning Curves for Photovoltaics*, (International Energy Agency, 2007) (http://www.iea.org/textbase/work/2007/learning/Nemet_PV.pdf).
27. Swanson, R. M., A vision for crystalline silicon photovoltaics. *Prog. Photovoltaics* **14**, 5, 443-453 (2006).
28. Tan, M. X., Laibinis, P. E., Nguyen, S. T., Kesselman, J. M., Stanton, C. E. and Lewis, N. S., Principles and applications of semiconductor photoelectrochemistry, in *Progress in Inorganic Chemistry, Vol 41* 21-144 (1994).
29. Sze, S.M., *Physics of Semiconductor Devices*, 2nd edition (John Wiley & Sons, Inc., 1981).
30. Schlosser, V., Limiting factors for the application of crystalline upgraded metallurgical grade silicon. *IEEE Trans. Electron Devices* **31**, 5, 610-613 (1984).
31. Green, M. A., Lambertian light trapping in textured solar cells and light-emitting diodes: Analytical solutions. *Prog. Photovoltaics* **10**, 4, 235-241 (2002).
32. Thorp, D. and Wenham, S. R., Ray-tracing of arbitrary surface textures for light-trapping in thin silicon solar cells. *Sol. Energy Mater. Sol. Cells* **48**, 1-4, 295-301 (1997).
33. Kayes, B. M., Atwater, H. A. and Lewis, N. S., Comparison of the device physics principles of planar and radial p-n junction nanorod solar cells. *J. Appl. Phys.* **97**, 11, (2005).
34. Kelzenberg, M. D., Turner-Evans, D. B., Kayes, B. M., Filler, M. A., Putnam, M. C., Lewis, N. S. and Atwater, H. A., Single-nanowire Si solar cells, in *Proc. 33rd IEEE Photovoltaics Spec. Conf.*, 1-6 (2008).
35. Xia, Y., Yang, P., Sun, Y., Wu, Y., Mayers, B., Gates, B., Yin, Y., Kim, F. and Yan, H., One-dimensional nanostructures: Synthesis, characterization, and applications. *Adv. Mater.* **15**, 5, 353-389 (2003).

36. Law, M., Goldberger, J. and Yang, P., Semiconductor nanowires and nanotubes. *Annu. Rev. Mater. Res.* **34**, 83-122 (2004).
37. Duan, X. and Lieber, C. M., General synthesis of compound semiconductor nanowires. *Adv. Mater.* **12**, 4, 298-302 (2000).
38. Milliron, D. J., Hughes, S. M., Cui, Y., Manna, L., Li, J. B., Wang, L. W. and Alivisatos, A. P., Colloidal nanocrystal heterostructures with linear and branched topology. *Nature* **430**, 6996, 190-195 (2004).
39. Vayssieres, L., Hagfeldt, A. and Lindquist, S., Purpose-built metal oxide nanomaterials. The emergence of a new generation of smart materials. *Pure Appl. Chem.* **72**, 1, 47-52 (2000).
40. Vayssieres, L., Beermann, N., Lindquist, S. and Hagfeldt, A., Controlled aqueous chemical growth of oriented three-dimensional crystalline nanorod arrays: Application to iron(III) oxides. *Chem. Mater.* **13**, 2, 233-235 (2001).
41. Greene, L. E., Law, M., Goldberger, J., Kim, F., Johnson, J. C., Zhang, Y. F., Saykally, R. J. and Yang, P. D., Low-temperature wafer-scale production of ZnO nanowire arrays. *Angew. Chem.-Int. Edit.* **42**, 26, 3031-3034 (2003).
42. Wagner, R. S. and Ellis, W. C., Vapor-Liquid-Solid Mechanism of Single Crystal Growth. *Appl. Phys. Lett.* **4**, 5, 89-90 (1964).
43. Almawlawi, D., Liu, C. Z. and Moskovits, M., Nanowires formed in anodic oxide nanotemplates. *J. Mater. Res.* **9**, 4, 1014-1018 (1994).
44. Hulteen, J. C. and Martin, C. R., A general template-based method for the preparation of nanomaterials. *J. Mater. Chem.* **7**, 7, 1075-1087 (1997).
45. Rahilly, W. P., Vertical multijunction solar cells, in *Proceedings of the 9th IEEE Photovoltaic Specialists Conference*, 44-52 (1972).
46. Green, M. A. and Wenham, S. R., Novel parallel multijunction solar cell. *Appl. Phys. Lett.* **65**, 23, 2907-2909 (1994).
47. Wohlgemuth, J. and Scheinine, A., New developments in vertical junction silicon solar cells, in *Proceedings of the 14th IEEE Photovoltaic Specialists Conference*, 151-155 (1980).
48. Keevers, M. J., Fabrication and characterisation of parallel multijunction thin film silicon solar cells. *Sol. Energy Mater. Sol. Cells* **65**, 1-4, 363-368 (2001).
49. Shchetinin, A. A., Drozhzhin, A. I., Sedykh, N. K. and Novokreshchenova, E. P., Photo-converters based on silicon-crystal whiskers. *Meas. Tech.* **21**, 4, 502-504 (1978).
50. Gu, Y., Romankiewicz, J. P., David, J. K., Lensch, J. L. and Lauhon, L. J., Quantitative measurement of the electron and hole mobility-lifetime products in semiconductor nanowires. *Nano Lett.* **6**, 5, 948-952 (2006).
51. Yu, J. Y., Chung, S. W. and Heath, J. R., Silicon nanowires: Preparation, device fabrication, and transport properties. *J. Phys. Chem. B* **104**, 50, 11864-11870 (2000).
52. Haick, H., Hurley, P. T., Hochbaum, A. I., Yang, P. and Lewis, N. S., Electrical characteristics and chemical stability of non-oxidized, methyl-terminated silicon nanowires. *J. Am. Chem. Soc.* **128**, 8990-8991 (2006).
53. Lauhon, L. J., Gudiksen, M. S., Wang, D. and Lieber, C. M., Epitaxial core-shell and core-multishell nanowire heterostructures. *Nature* **420**, 6911, 57-61 (2002).

54. Lyons, D., Ryan, K., Morris, M. and Holmes, J., Tailoring the optical properties of silicon nanowire arrays through strain. *Nano Lett.* **2**, 8, 811-816 (2002).
55. Tsakalakos, L., Balch, J., Fronheiser, J., Shih, M.-Y., LeBoeuf, S. F., Pietrzykowski, M., Codella, P. J., Korevaar, B. A., Sulima, O., Rand, J., Davuluru, A. and Rapol, U., Strong broadband optical absorption in silicon nanowire films. *J. Nanophotonics* **1**, 013552 (2007).
56. Vayssieres, L., Sathe, C., Butorin, S. M., Shuh, D. K., Nordgren, J. and Guo, J., One-dimensional quantum-confinement effect in α-Fe_2O_3 ultrafine nanorod arrays. *Adv. Mater.* **17**, 2320-2323 (2005).
57. Dilts, S. M., Mohmmad, A., Lew, K. K., Redwing, J. M. and Mohney, S. E., B.S. thesis, *Fabrication and electrical characterization of silicon nanowire arrays*, Pennsylvania State University, State College, PA, 2005.
58. Beermann, N., Vayssieres, L., Lindquist, S. and Hagfeldt, A., Photoelectrochemical studies of oriented nanorod thin films of hematite. *J. Electrochem. Soc.* **147**, 7, 2456-2461 (2000).
59. Tan, B. and Wu, Y., Dye-sensitized solar cells based on anatase TiO_2 nanoparticle/nanowire composites. *J. Phys. Chem. B* **110**, 15932-15938 (2006).
60. Law, M., Greene, L. E., Johnson, J. C., Saykally, R. and Yang, P. D., Nanowire dye-sensitized solar cells. *Nature Materials* **4**, 6, 455-459 (2005).
61. Kelly, J. J. and Vanmaekelbergh, D., Charge carrier dynamics in nanoporous photoelectrodes. *Electrochim. Acta* **43**, 19-20, 2773-2780 (1998).
62. vandeLagemaat, J., Plakman, M., Vanmaekelbergh, D. and Kelly, J. J., Enhancement of the light-to-current conversion efficiency in an n-SiC/solution diode by porous etching. *Appl. Phys. Lett.* **69**, 15, 2246-2248 (1996).
63. McCandless, B. and Sites, J., Cadmium Telluride Solar Cells, in *Handbook of Photovoltaic Science and Engineering* (eds. Luque, A. & Hegedus, S.) 617-657 (John Wiley & Sons, Chichester, England, 2003).
64. Jenny, D. and Bube, R., Semiconducting cadmium telluride. *Phys. Rev.* **96**, 5, 1190-1191 (1954).
65. Harris, L. A. and Wilson, R. H., Semiconductors for photoelectrolysis. *Annu. Rev. Mater. Sci.* **8**, 99-134 (1978).
66. Basol, B. M., High-efficiency electroplated heterojunction solar cell. *J. Appl. Phys.* **55**, 2, 601-603 (1984).
67. Fulop, G., Doty, M., Meyers, P., Betz, J. and Liu, C. H., High-efficiency electrodeposited cadmium telluride solar cells. *Appl. Phys. Lett.* **40**, 4, 327-328 (1982).
68. Bhattacharya, R. N. and Rajeshwar, K., Electrodeposition of CdTe thin films. *J. Electrochem. Soc.* **131**, 9, 2032-2037 (1984).
69. Paulson, P. D. and Mathew, X., Spectroscopic ellipsometry investigation of optical and interface properties of CdTe films deposited on metal foils. *Sol. Energy Mater. Sol. Cells* **82**, 1-2, 279-290 (2004).
70. Lepiller, C. and Lincot, D., New facets of CdTe electrodeposition in acidic solutions with higher tellurium concentrations. *J. Electrochem. Soc.* **151**, 5, C348-C357 (2004).

71. Kressin, A. M., Doan, V. V., Klein, J. D. and Sailor, M. J., Synthesis of stoichiometric cadmium selenide films via sequential monolayer electrodeposition. *Chem. Mater.* **3**, 6, 1015-1020 (1991).
72. Basol, B., Thin film CdTe solar cells - A review, in *Proceedings of the 21st IEEE Photovoltaic Specalists Conference*, 588-594 (1990).
73. Klein, J. D., Herrick, R. D., Palmer, D., Sailor, M. J., Brumlik, C. J. and Martin, C. R., Electrochemical fabrication of cadmium chalcogenide microdiode arrays. *Chem. Mater.* **5**, 7, 902-904 (1993).
74. Basol, B., Tseng, E. and Rod, R., Ultra-thin electrodeposited CdS/CdTe heterojunction with 8% efficiency. *Proceedings of the IEEE Photovoltaic Specialists Conference*, 805-808 (1982).
75. Routkevitch, D., Bigioni, T., Moskovits, M. and Xu, J. M., Electrochemical fabrication of CdS nanowire arrays in porous anodic aluminum oxide templates. *J. Phys. Chem.* **100**, 33, 14037-14047 (1996).
76. Kang, Y. M., Park, N. G. and Kim, D., Hybrid solar cells with vertically aligned CdTe nanorods and a conjugated polymer. *Appl. Phys. Lett.* **86**, 11, (2005).
77. Toh, C. S., Kayes, B. M., Nemanick, E. J. and Lewis, N. S., Fabrication of free-standing nanoscale alumina membranes with controllable pore aspect ratios. *Nano Lett.* **4**, 5, 767-770 (2004).
78. Keller, F., Hunter, M. S. and Robinson, D. L., Structural features of oxide coatings on aluminum. *J. Electrochem. Soc.* **100**, 9, 411-419 (1953).
79. Hunter, M. S. and Fowle, P., Determination of barrier layer thickness of anodic oxide coatings. *J. Electrochem. Soc.* **101**, 9, 481-485 (1954).
80. Diggle, J. W., Downie, T. C. and Goulding, C. W., Anodic oxide films on aluminum. *Chem. Rev.* **69**, 3, 365-& (1969).
81. Goad, D. G. W. and Moskovits, M., Colloidal metal in aluminum-oxide. *J. Appl. Phys.* **49**, 5, 2929-2934 (1978).
82. Ellis, A. B., Kaiser, S. W. and Wrighton, M. S., Optical to electrical energy-conversion. Characterization of cadmium sulfide and cadmium selenide based photoelectrochemical cells. *J. Am. Chem. Soc.* **98**, 22, 6855-6866 (1976).
83. Ellis, A. B., Kaiser, S. W., Bolts, J. M. and Wrighton, M. S., Study of n-type semiconducting cadmium chalcogenide-based photoelectrochemical cells employing polychalcogenide electrolytes. *J. Am. Chem. Soc.* **99**, 9, 2839-2848 (1977).
84. Cahen, D., Hodes, G. and Manassen, J., S/Se substitution in polycrystalline CdSe photoelectrodes. Photoelectrochemical energy-conversion. *J. Electrochem. Soc.* **125**, 10, 1623-1628 (1978).
85. Hodes, G., Manassen, J. and Cahen, D., Effect of photoelectrode crystal-structure on output stability of Cd(Se, Te)-polysulfide photoelectrochemical cells. *J. Am. Chem. Soc.* **102**, 18, 5962-5964 (1980).
86. Licht, S., Hodes, G., Tenne, R. and Manassen, J., A light-variation insensitive high efficiency solar cell. *Nature* **326**, 6116, 863-864 (1987).
87. Licht, S., Tenne, R., Dagan, G., Hodes, G., Manassen, J., Cahen, D., Triboulet, R., Rioux, J. and Levyclement, C., High efficiency n-Cd(Se, Te)/S^{2-}

photoelectrochemical cell resulting from solution chemistry control. *Appl. Phys. Lett.* **46**, 6, 608-610 (1985).

88. Hodes, G., Manassen, J., Neagu, S., Cahen, D. and Mirovsky, Y., Electroplated cadmium chalcogenide layers: Characterization and use in photoelectrochemical solar cells. *Thin Solid Films* **90**, 4, 433-438 (1982).
89. Bard, A., Parsons, R. and Jordan, J., *Standard Potentials in Aqueous Solution*, (IUPAC, Marcel Dekker, New York, 1985).
90. Tenne, R. and Hodes, G., Improved efficiency of CdSe photoanodes by photoelectrochemical etching. *Appl. Phys. Lett.* **37**, 4, 428-430 (1980).
91. Mirovsky, Y., Cahen, D., Hodes, G., Tenne, R. and Giriat, W., Photoelectrochemistry of the the $CuInS_2/S_n^{2-}$ system. *Sol. Energy Mater.* **4**, 2, 169-177 (1981).
92. Tufts, B. J., Abrahams, I. L., Casagrande, L. G. and Lewis, N. S., Studies of the n-GaAs/KOH-Se_2^{2-}-Se^{2-} semiconductor/liquid junction. *J. Phys. Chem.* **93**, 8, 3260-3269 (1989).
93. Lewis, N. S., Mechanistic studies of light-induced charge separation at semiconductor/liquid interfaces. *Acc. Chem. Res.* **23**, 6, 176-183 (1990).
94. Tufts, B. J., Abrahams, I. L., Santangelo, P. G., Ryba, G. N., Casagrande, L. G. and Lewis, N. S., Chemical modification of n-GaAs electrodes with Os^{3+} gives a 15% efficient solar cell. *Nature* **326**, 6116, 861-863 (1987).
95. Haxel, G. B., Hedrick, J. B. and Orris, G. J., *Rare earth elements - Critical resources for high technology: US Geological Survey fact sheet 087-02*, (US Geological Survey, 2002) (http://pubs.usgs.gov/fs/2002/fs087-02/).
96. Lehman, V., *Electrochemistry of Silicon*, (WILEY-VCH, Weinheim, Germany, 2002).
97. Davis, J. R., Rohatgi, A., Hopkins, R. H., Blais, P. D., Raichoudhury, P., McCormick, J. R. and Mollenkopf, H. C., Impurities in silicon solar cells. *IEEE Trans. Electron Devices* **27**, 4, 677-687 (1980).
98. Elwell, D. and Feigelson, R. S., Electrodeposition of solar silicon. *Sol. Energy Mater.* **6**, 2, 123-145 (1982).
99. Nicholson, J., Electrodeposition of silicon from nonaqueous solvents. *J. Electrochem. Soc.* **152**, 12, C795-C802 (2005).
100. Wagner, R. S. and Ellis, W. C., The vapor-liquid-solid mechanism of crystal growth and its application to silicon. *T. Metall. Soc. AIME* **233**, 1053-1064 (1964).
101. Wagner, R. S., Defects in silicon crystals grown by VLS technique. *J. Appl. Phys.* **38**, 4, 1554-& (1967).
102. Givargizov, E. I., Fundamental aspects of VLS growth. *J. Crystal Growth* **31**, DEC, 20-30 (1975).
103. Cui, Y., Duan, X. F., Hu, J. T. and Lieber, C. M., Doping and electrical transport in silicon nanowires. *J. Phys. Chem. B* **104**, 22, 5213-5216 (2000).
104. Wagner, R. S. and Doherty, C. J., Controlled vapor-liquid-solid growth of silicon crystals. *J. Electrochem. Soc.* **113**, 12, 1300-& (1966).
105. Nebol'sin, V. A. and Shchetinin, A. A., Role of surface energy in the vapor-liquid-solid growth of silicon. *Inorganic materials* **39**, 9, 899-903 (2003).

106. Hochbaum, A. I., Fan, R., He, R. R. and Yang, P. D., Controlled growth of Si nanowire arrays for device integration. *Nano Lett.* **5**, 3, 457-460 (2005).
107. Jagannathan, H., Nishi, Y., Reuter, M., Copel, M., Tutuc, E., Guha, S. and Pezzi, R. P., Effect of oxide overlayer formation on the growth of gold catalyzed epitaxial silicon nanowires. *Appl. Phys. Lett.* **88**, 10, 103113 (2006).
108. Hannon, J., Kodambaka, S., Ross, F. and Tromp, R., The influence of the surface migration of gold on the growth of silicon nanowires. *Nature* **440**, 69-71 (2006).
109. Kodambaka, S., Tersoff, J., Reuter, M. C. and Ross, F. M., Diameter-independent kinetics in the vapor-liquid-solid growth of Si nanowires. *Phys. Rev. Lett.* **96**, 9, (2006).
110. Wang, Y. W., Schmidt, V., Senz, S. and Gosele, U., Epitaxial growth of silicon nanowires using an aluminium catalyst. *Nature Nanotechnology* **1**, 3, 186-189 (2006).
111. Lew, K. and Redwing, J., Growth characteristics of silicon nanowires synthesized by vapor-liquid-solid growth in nanoporous alumina templates. *J. Crystal Growth* **254**, 1-2, 14-22 (2003).
112. Bogart, T., Dey, S., Lew, K. K., Mohney, S. and Redwing, J., Diameter-controlled synthesis of silicon nanowires using nanoporous alumina membranes. *Adv. Mater.* **17**, 1, 114-117 (2005).
113. Lew, K. K., Reuther, C., Carim, A. H., Redwing, J. M. and Martin, B. R., Template-directed vapor-liquid-solid growth of silicon nanowires. *J. Vac. Sci. Technol. B* **20**, 1, 389-392 (2002).
114. Kayes, B. M., Spurgeon, J. M., Sadler, T. C., Lewis, N. S. and Atwater, H. A., Synthesis and characterization of silicon nanorod arrays for solar cell applications, in *Proc. 4th IEEE WCPEC*, 221-224 (2006).
115. Shackelford, J. F., *Introduction to Materials Science for Engineers*, 6th edition (Pearson Prentice Hall, Upper Saddle River, NJ, 2005).
116. Carim, A. H., Lew, K. K. and Redwing, J. M., Bicrystalline silicon nanowires. *Adv. Mater.* **13**, 19, 1489-1491 (2001).
117. Westwater, J., Gosain, D. P., Tomiya, S., Usui, S. and Ruda, H., Growth of silicon nanowires via gold/silane vapor-liquid-solid reaction. *J. Vac. Sci. Technol. B* **15**, 3, 554-557 (1997).
118. Cha, A.E., Solar energy firms leave waste behind in China. *Washington Post*, (9 March 2008).
119. Kayes, B. M., Filler, M. A., Putnam, M. C., Kelzenberg, M. D., Lewis, N. S. and Atwater, H. A., Growth of vertically aligned Si wire arrays over large areas (> 1 cm^2) with Au and Cu catalysts. *Appl. Phys. Lett.* **91**, 10, (2007).
120. Kelzenberg, M. D., Turner-Evans, D. B., Kayes, B. M., Filler, M. A., Putnam, M. C., Lewis, N. S. and Atwater, H. A., Photovoltaic measurements in single-nanowire silicon solar cells. *Nano Lett.* **8**, 2, 710-714 (2008).
121. Putnam, M. C., Turner-Evans, D. B., Kelzenberg, M. D., Boettcher, S. W., Lewis, N. S. and Atwater, H. A., 10 μm minority-carrier diffusion lengths in Si wires synthesized by Cu-catalyzed vapor-liquid-solid growth. *Appl. Phys. Lett.*, Submitted, (2009).

122. Kelzenberg, M. D., Boettcher, S. W., Petykiewicz, J. A., Turner-Evans, D. B., Putnam, M. C., Warren, E. L., Spurgeon, J. M., Lewis, N. S. and Atwater, H. A., Absorption enhancement in Si wire arrays for photovoltaic applications. Submitted, (2009).
123. Struthers, J. D., Solubility and diffusivity of gold, iron, and copper in silicon. *J. Appl. Phys.* **27**, 12, 1560-1560 (1956).
124. Aalberts, J. H. and Verheijke, M. L., The solid solubility of nickel in silicon determined by neutron activation analysis. *Appl. Phys. Lett.* **1**, 1, 19-20 (1962).
125. Quake, S. R. and Scherer, A., From micro- to nanofabrication with soft materials. *Science* **290**, 5496, 1536-1540 (2000).
126. Unger, M. A., Chou, H. P., Thorsen, T., Scherer, A. and Quake, S. R., Monolithic microfabricated valves and pumps by multilayer soft lithography. *Science* **288**, 5463, 113-116 (2000).
127. Whitesides, G. M. and Stroock, A. D., Flexible methods for microfluidics. *Phys. Today* **54**, 6, 42-48 (2001).
128. McDonald, J. C. and Whitesides, G. M., Poly(dimethylsiloxane) as a material for fabricating microfluidic devices. *Acc. Chem. Res.* **35**, 7, 491-499 (2002).
129. Lee, J. N., Park, C. and Whitesides, G. M., Solvent compatibility of poly(dimethylsiloxane)-based microfluidic devices. *Anal. Chem.* **75**, 23, 6544-6554 (2003).
130. Ulman, A., Choi, G. Y., Shnidman, Y. and Zurawsky, W., Adhesion studies using contact mechanics. *Isr. J. Chem.* **40**, 2, 107-121 (2000).
131. Yang, Z. P., Ci, L. J., Bur, J. A., Lin, S. Y. and Ajayan, P. M., Experimental observation of an extremely dark material made by a low-density nanotube array. *Nano Lett.* **8**, 2, 446-451 (2008).
132. Li, H. L., Ujihira, Y., Shukushima, S. and Ueno, K., Variation of size, numerical concentration and size distribution of free volume of heat shrink polyethylene prepared by electron irradiation cross-linkage with temperature probed by positron annihilation technique. *Polymer* **41**, 1, 93-99 (2000).
133. Wu, X. P., Wu, Q. H. and Ko, W. H., A study on deep etching of silicon using ethylenediamine-pyrocatechol-water. *Sens. Actuators* **9**, 4, 333-343 (1986).
134. Turner, D. R., Electropolishing silicon in hydrofluoric acid solutions. *J. Electrochem. Soc.* **105**, 7, 402-408 (1958).
135. Ismail, H. and Hashim, U., Hydrogen gas production for electronic-grade polycrystalline silicon growth. *Proc. IEEE ICSE*, 53-56 (2002).
136. Chu, T. L., Stokes, E. D. and Abderrassoul, R. A., Large area polycyrstalline silicon solar cells on unidirectionally solidified acid-treated metallurgical grade silicon. *Proc. IEEE Southeastcon*, 1436-1441 (1989).
137. Tian, B. Z., Zheng, X. L., Kempa, T. J., Fang, Y., Yu, N. F., Yu, G. H., Huang, J. L. and Lieber, C. M., Coaxial silicon nanowires as solar cells and nanoelectronic power sources. *Nature* **449**, 7164, 885-889 (2007).
138. Kayes, B. M., Filler, M. A., Henry, M. D., Maiolo, J. R., Kelzenberg, M. D., Putnam, M. C., Spurgeon, J. M., Plass, K. E., Scherer, A., Lewis, N. S. and Atwater, H. A., Radial pn junction, wire array solar cells, in *Proc. 33rd IEEE Photovoltaics Specs Conf.*, 1-5 (2008).

139. Garnett, E. C. and Yang, P. D., Silicon nanowire radial p-n junction solar cells. *J. Am. Chem. Soc.* **130**, 29, 9224-9225 (2008).
140. Tsakalakos, L., Balch, J., Fronheiser, J., Korevaar, B. A., Sulima, O. and Rand, J., Silicon nanowire solar cells. *Appl. Phys. Lett.* **91**, 23, (2007).
141. Maiolo, J. R., Kayes, B. M., Filler, M. A., Putnam, M. C., Kelzenberg, M. D., Atwater, H. A. and Lewis, N. S., High aspect ratio silicon wire array photoelectrochemical cells. *J. Am. Chem. Soc.* **129**, 41, 12346-12347 (2007).
142. Goodey, A. P., Eichfeld, S. M., Lew, K. K., Redwing, J. M. and Mallouk, T. E., Silicon nanowire array photoelectrochemical cells. *J. Am. Chem. Soc.* **129**, 41, 12344-12345 (2007).
143. Lombardi, I., Hochbaum, A., Yang, P., Carraro, C. and Maboudian, R., Synthesis of high density, size-controlled Si nanowire arrays via porous alumina mask. *Chem. Mater.* **18**, 4, 988-991 (2006).
144. Plass, K. E., Filler, M. A., Spurgeon, J. M., Kayes, B. M., Maldonado, S., Brunschwig, B. S., Atwater, H. A. and Lewis, N. S., Flexible polymer-embedded Si wire arrays. *Adv. Mater.* **21**, 3, 325-328 (2009).
145. Spurgeon, J. M., Plass, K. E., Kayes, B. M., Brunschwig, B. S., Atwater, H. A. and Lewis, N. S., Repeated epitaxial growth and transfer of arrays of patterned, vertically aligned, crystalline Si wires from a single Si(111) substrate. *Appl. Phys. Lett.* **93**, 3, 032112-1-3 (2008).
146. Boettcher, S. W., Spurgeon, J. M., Putnam, M. C., Warren, E. L., Turner-Evans, D. B., Kelzenberg, M. D., Maiolo, J. R., Atwater, H. A. and Lewis, N. S., Energy conversion properties of silicon wire-array photocathodes. Submitted, (2009).
147. Bookbinder, D. C., Lewis, N. S., Bradley, M. G., Bocarsly, A. B. and Wrighton, M. S., Photoelectrochemical reduction of N,N'-dimethyl-4,4'-bipyridinium in aqueous-media at p-type silicon - Sustained photogeneration of a species capable of evolving hydrogen. *J. Am. Chem. Soc.* **101**, 26, 7721-7723 (1979).
148. Kooij, E. S., Despo, R. W., Mulders, F. P. J. and Kelly, J. J., Electrochemistry of porous and crystalline silicon electrodes in methylviologen solutions. *J. Electroanal. Chem.* **406**, 1-2, 139-146 (1996).
149. Stargardt, J. F. and Hawkridge, F. M., Computer decomposition of the ultraviolet-visible absorption spectrum of the methyl viologen cation radical and its dimer in solution. *Anal. Chim. Acta* **146**, FEB, 1-8 (1983).
150. Philipp, H. R. and Taft, E. A., Optical constants of silicon in the region 1 to 10 eV. *Phys. Rev.* **120**, 1, 37-38 (1960).
151. Spurgeon, J. M., Atwater, H. A. and Lewis, N. S., A comparison between the behavior of nanorod array and planar Cd(Se, Te) photoelectrodes. *J. Phys. Chem. C* **112**, 15, 6186-6193 (2008).
152. Bard, A. J. and Faulkner, L. R., *Electrochemical Methods: Fundamentals and Applications*, 2nd edition (John Wiley & Sons, 2001).
153. Hamann, T. W., Gstrein, F., Brunschwig, B. S. and Lewis, N. S., Measurement of the free-energy dependence of interfacial charge-transfer rate constants using ZnO/H_2O semiconductor/liquid contacts. *J. Am. Chem. Soc.* **127**, 21, 7815-7824 (2005).

154. Istratov, A. A. and Weber, E. R., Physics of copper in silicon. *J. Electrochem. Soc.* **149**, 1, G21-G30 (2002).
155. The efficiency is determined by $\eta = (J_{sc})(V_{oc})(FF)/P$ where P = 100 mW cm^{-2} and J_{sc} is assumed to be 35 mA cm^{-2}. From Table 5.1 for a polymer-supported wire array at 60 mW cm^{-2} of 808 nm illumination (approximately the same photon flux as 100 mW cm^{-2} AM 1.5), the uncorrected FF = 0.35. Because $V_{oc} = (kT/q)\ln(J_{sc}/J_o)$, increasing J_{sc} from 7.9 to 35 mA cm^{-2} would increase the V_{oc} by 38 mV to V_{oc} = 428 mV. The result is η = 5.2%.
156. Kayes, B. M., Ph.D. thesis, *Radial pn Junction, Wire Array Solar Cells*, California Institute of Technology, Pasadena, California, 2008.
157. Takayama, S., Ostuni, E., Qian, X. P., McDonald, J. C., Jiang, X. Y., LeDuc, P., Wu, M. H., Ingber, D. E. and Whitesides, G. M., Topographical micropatterning of poly(dimethylsiloxane) using laminar flows of liquids in capillaries. *Adv. Mater.* **13**, 8, 570-574 (2001).
158. Bansal, A., Li, X. L., Yi, S. I., Weinberg, W. H. and Lewis, N. S., Spectroscopic studies of the modification of crystalline Si(111) surfaces with covalently-attached alkyl chains using a chlorination/alkylation method. *J. Phys. Chem. B* **105**, 42, 10266-10277 (2001).
159. Perraud, S., Poncet, S., Noel, S., Levis, M., Faucherand, P., Rouviere, E., Thony, P., Jaussaud, C. and Delsol, R., Full process for integrating silicon nanowire arrays into solar cells. *Sol. Energy Mater. Sol. Cells* **93**, 9, 1568-1571 (2009).
160. Cong, H. L. and Pan, T. R., Photopatternable conductive PDMS materials for microfabrication. *Adv. Funct. Mater.* **18**, 13, 1912-1921 (2008).
161. Song, J. E., Lee, D. K., Kim, H. W., Kim, Y. I. and Kang, Y. S., Preparation and characterization of monodispersed indium-tin oxide nanoparticles. *Colloid Surf. A-Physicochem. Eng. Asp.* **257-58**, 539-542 (2005).
162. Licht, S., Wang, B., Mukerji, S., Soga, T., Umeno, M. and Tributsch, H., Efficient solar water splitting, exemplified by RuO_2-catalyzed AlGaAs/Si photoelectrolysis. *J. Phys. Chem. B* **104**, 38, 8920-8924 (2000).
163. Licht, S., Multiple band gap semiconductor/electrolyte solar energy conversion. *J. Phys. Chem. B* **105**, 27, 6281-6294 (2001).
164. Heller, A., Lewerenz, H. J. and Miller, B., Silicon photocathode behavior in acidic V(II) - V(III) solutions. *J. Am. Chem. Soc.* **103**, 1, 200-201 (1981).
165. Szklarczyk, M. and Ombockris, J., Photoelectrocatalysis and electrocatalysis on p-silicon. *J. Phys. Chem.* **88**, 9, 1808-1815 (1984).
166. May, R. A., Kondrachova, L., Hahn, B. P. and Stevenson, K. J., Optical constants of electrodeposited mixed molybdenum-tungsten oxide films determined by variable-angle spectroscopic ellipsometry. *J. Phys. Chem. C* **111**, 49, 18251-18257 (2007).
167. Kondrachova, L., Hahn, B. P., Vijayaraghavan, G., Williams, R. D. and Stevenson, K. J., Cathodic electrodeposition of mixed molybdenum tungsten oxides from peroxo-polymolybdotungstate solutions. *Langmuir* **22**, 25, 10490-10498 (2006).
168. Wang, H. L., Lindgren, T., He, J. J., Hagfeldt, A. and Lindquist, S. E., Photolelectrochemistry of nanostructured WO_3 thin film electrodes for water

oxidation: Mechanism of electron transport. *J. Phys. Chem. B* **104**, 24, 5686-5696 (2000).

169. Watcharenwong, A., Chanmanee, W., de Tacconi, N. R., Chenthamarakshan, C. R., Kajitvichyanukul, P. and Rajeshwar, K., Anodic growth of nanoporous WO_3 films: Morphology, photoelectrochemical response and photocatalytic activity for methylene blue and hexavalent chrome conversion. *J. Electroanal. Chem.* **612**, 1, 112-120 (2008).
170. Hitoki, G., Takata, T., Ikeda, S., Hara, M., Kondo, J. N., Kakihana, M. and Domen, K., Mechano-catalytic overall water splitting on some mixed oxides. *Catal. Today* **63**, 2-4, 175-181 (2000).
171. Larminie, J. and Dicks, A., *Fuel Cell Systems Explained*, 2nd edition (John Wiley & Sons, West Sussex, England, 2003).
172. Farhat, T. R. and Hammond, P. T., Designing a new generation of proton-exchange membranes using layer-by-layer deposition of polyelectrolytes. *Adv. Funct. Mater.* **15**, 6, 945-954 (2005).