Chapter 7

The plasMOStor: A Metal/Oxide/Si Field Effect Plasmonic Modulator

7.1 Introduction

In this part of the thesis, we discuss using doped silicon layers and transparent conducting oxides as the active layers in MIM waveguides. With these devices, modulation of the optical signal is based on changing the carrier density distribution within the active region. An added benefit of using silicon as the active region is that this material forms the basis for much of the semiconductor industry. Besides being one of the most extensively studied material in existence, silicon already forms the basis for complementary metal-oxide- semiconductor (CMOS) processes. Using silicon also allows plasmonic devices to be easily integrated into current fabrication processes when the focus is on designing chip-based all-optical and optoelectronic computational networks. Designing plasmonic-based circuits will require ultracompact Si-compatible modulators, ideally comprising dimensions, materials, and functionality similar to electronic complementary metal-oxide-semiconductor (CMOS) components. Here we demonstrate such a modulator, based on field-effect modulation of plasmon waveguide modes in a MOS geometry. Near-infrared transmission between an optical source and drain is controlled by a gate voltage that drives the MOS into accumulation. Using the gate oxide as an optical channel, electro-optic modulation is achieved in device volumes of half of a cubic wavelength with femtojoule switching energies and the potential for gigahertz modulation frequencies. [1]

7.2 CMOS and the Emergence of Plasmonics

The integrated circuits ubiquitous in modern technology were critically enabled by the invention of the metal-oxide-semiconductor field effect transistor (MOSFET) - a three-terminal device that

[1] This chapter is based on work done with Dr. Luke Sweatlock and Dr. Jennifer Dionne [34].

modulates current flow between a source and drain via an applied electric field. Since the first successful demonstration of MOSFETs in the 1960s, silicon devices and circuits have continuously scaled according to Moore's law, which predicts that the density of electronic circuits within a chip of a given size will double every 18 - 24 months. This has been done by increasing both the integration density and bandwidth of complementary metal-oxide-semiconductor (CMOS) networks. At present, microprocessors contain over 800 million transistors clocked at 3 GHz, with transistor gate lengths as small as 35 nm [20, 53]. Unfortunately, as gate lengths approach the single-nanometer scale, following Moore's Law becomes increasingly difficult. MOS scaling is accompanied by increased circuit delay and higher electronic power dissipation - a substantial hurdle to Moore's law often referred to as the interconnect bottleneck.

To circumvent the electrical and thermal parasitics associated with MOS scaling, new interconnect technologies are being considered. Particular attention has been given to optical technologies, which could achieve high integration densities without significant electrical limitations [73, 113, 119]. On-chip optical components would offer a substantially higher bandwidth, a lower latency, and a reduced power dissipation compared with electronic components [73, 83, 119]. Unfortunately, the size of these optical components is diffraction limited as discussed in Chapter 1.

Here, we present an experimental demonstration of a field effect Si modulator based on multimode interferometry in a plasmonic waveguide. Like the Si-based modulators implemented by Lipson and colleagues [124], this device utilizes high optical mode confinement to enhance electro-optical nonlinearities in Si. Moreover, like the Si optical modulator of Liu and colleagues [68], this device exploits the fast modulation of accumulation conditions in a metal-oxide-semiconductor (MOS) capacitor. In contrast with these and related structures [69], our plasmonic modulator can achieve modulation of nearly 10 dB in device volumes of half a cubic wavelength. In particular, our device illustrates that conventional scaled MOSFETs can operate as optical modulators, by transforming the channel oxide into a plasmon slot waveguide.

7.3 Design and Fabrication of the plasMOStor

To fabricate the plasmostor, we start with an silicon-on-insulator (SOI) wafer having a doped device layer (n-type) with carrier concentrations of $9 \times 10^{16}\ cm^{-3}$ and an initial thickness of 1.5 μm, Figure 7.1(a). The wafer is initially covered in a chemically resistant Logitech chemical mechanical polishing wax. The entire sample is covered with the exception of an etch window that is left

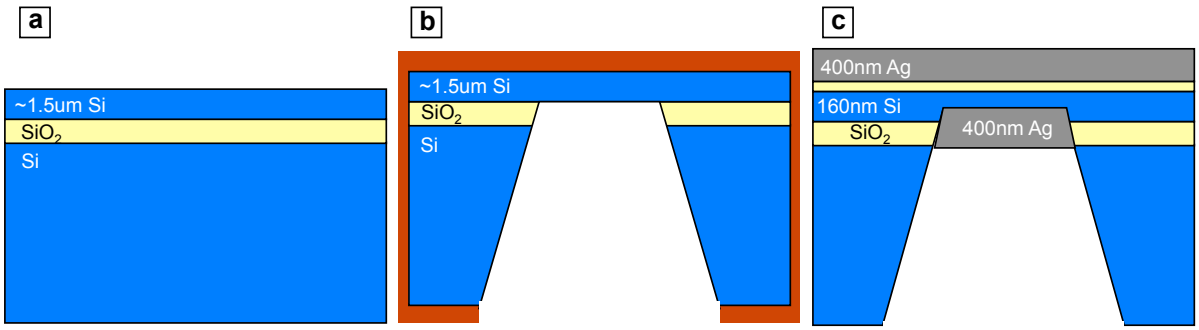


Figure 7.1. Etching and oxidation steps involved in the plasmostor fabrication.

exposed on the bottom, handle substrate, Figure 7.1(b). A mixture of 5:1 nitric to hydrofluoric acid is constantly stirred while the waxed sample is placed in the etch bath. After $\sim$ 60 minutes, a region within the etch window will reach the buried oxide layer of the SOI wafer and the etch window will change color from black to white. The sample is then removed from the etch and placed in buffered oxide etch (BOE) until the buried oxide layer is removed ($\sim$ 2 nm/sec), Figure 7.1(b). The wax layer is then removed by soaking in acetone over night.

At this point, the silicon device layer exists as a free-standing, single crystal silicon membrane. The thickness of this membrane was determined using spectroscopic ellipsometry which is discussed in detail in Appendix C. To thin the membrane, wet oxidation was performed and the oxidation time was calculated using Reference [24]. The membranes were thinned to the desired thickness, and then a 10nm oxide layer was grown on the top surface. After oxidation, 400 nm of silver was evaporated on the top and bottom surfaces of the membrane. A schematic of the final structure is shown in Figure 7.1(c).

It should be noted that, while we do not currently believe that strain within the membranes significantly contributes to the overall performance of the device, both Raman and x-ray diffraction measurements of the membranes at varying thicknesses indicated that the membranes were in a state of tensile stress. For the critical thickness used in these studies, both measurement techniques indicated that the silicon was under $\sim$ 500 MPa of tensile stress. This effect was considered when determining the effective electron mass for the Drude model. This is shown in Figure 7.2. The pannel on the left shows Raman peak shifting as a function of silicon membrane thickness. The pannel on the right shows rocking curve x-ray diffraction measurements of thick and thin SOI and silicon membranes. The peak splitting shown in the thinned membrane pannel indicates that the

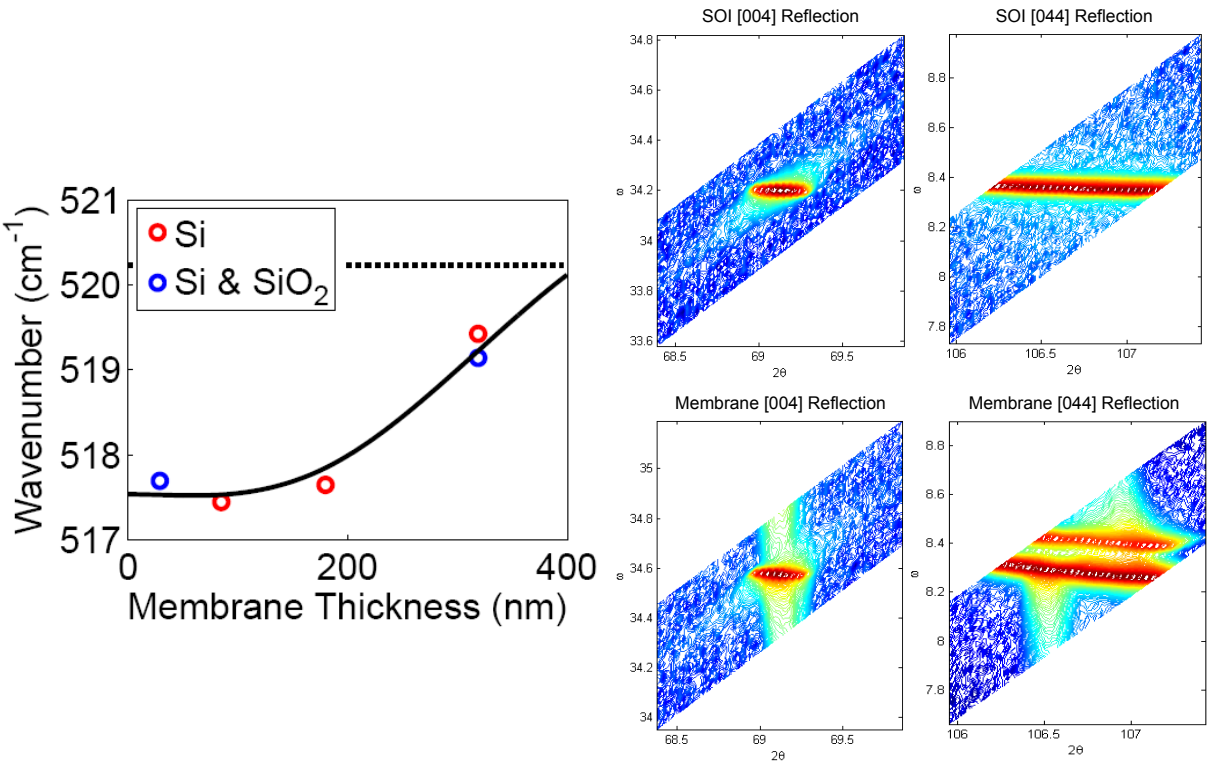


Figure 7.2. Raman peak shifting as a function of silicon membrane thickness (left pannel). Rocking curve x-ray diffraction measurements of thick and thin SOI and silicon membranes (right pannel).

tensile stress in the thinned membranes has distorted the lattice to the point that two separate lattice constants are present in the out-of-plane direction and the in-plane direction.

Sub-wavelength input and output slits were milled into the top and bottom of the membrane, respectively, Figure 7.3. Light was coupled into and out of the plasmostor via subwavelength slits etched into the top and bottom cladding layers (Figure 7.3(b)). This double-sided coupling configuration provides for a dark-field imaging configuration with minimal background signal, though end-fire excitation could also be used. Note that in this geometry, the slits function as the optical source (input) and drain (output) of the plasmostor. As seen in Figure 7.3(b), the input slits are defined to a length of approximately 4 μm, which determines the lateral extent of waveguided modes [35]. To map transmission as a function of device length, the input-output slit separation was varied from approximately 1 - 8 μm in 50 nm increments. An overview of the entire device is shown in Figure 7.4. Here each of the dark spots on the membrane represent a different device. All the devices were spaced such that there was no cross-talk between them.

At λ = 1550nm, in the absence of an applied electric field, dispersion calculations for the

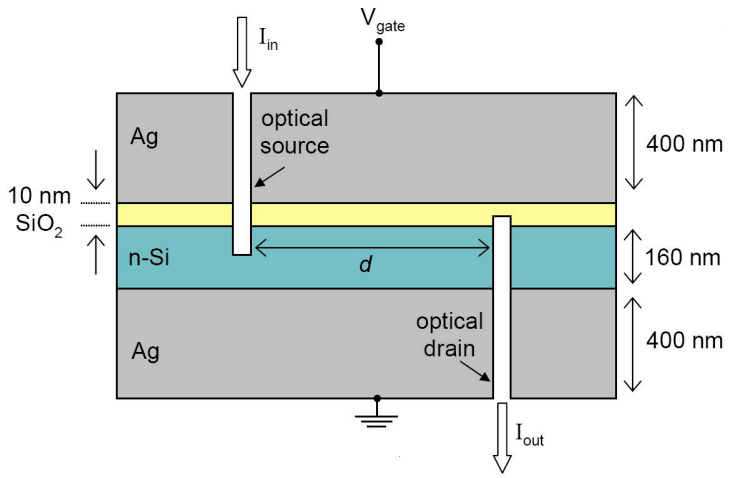


Figure 7.3. Cross-sectional schematic of the Si field effect plasmonic modulator.

plasmostor show the existance of two optical modes: a photonic mode lying to the left of the Si and SiO_2 light lines, and a plasmonic mode lying to the right of the Si light line. Both modes will be generated at the plasmostor source and can interfere either constructively or destructively at the drain, depending on the source-drain separation, Figure 7.5(a). The nearly-flat dispersion of the photonic mode around $\lambda = 1.55\ \mu m$ suggests that this mode will be extremely sensitive to changes in the Si complex index. For example, modifying the Si index through free-carrier absorption will push this mode into cutoff, such that the dispersion curve intercepts the energy axis just above $\lambda = 1.55\ \mu m$. The remaining plasmonic mode will then propagate through the plasmostor without interference from the photonic mode. Dispersion calculations confirm that upon application of an electric field, the plasmonic mode remains mostly unchanged, while the photonic mode is pushed into cutoff, Figure 7.5(b). As a comparison, looking at 7.5(a) and (b) for devices operated at $\lambda =$ 685 nm, the dispersion diagrams show negligible changes between the on state and the off state.

Modal properties were calculated via a numerical solution of Maxwell's equations and assume uniform coupling across the waveguide stack. For reference, the dispersion diagram also includes the light lines in Si and SiO_2, corresponding to light propagation through bulk media with refractive index $n = n_{Si}$ or n_{SiO_2}.

Looking explicitly at the mode profiles, Figure 7.6 shows that in the absence of an applied field at the gate, the plasmostor is fully depleted and light can be guided from the source to the drain through both the Si and SiO_2 layers. As seen in Figure 7.6(b), the photonic mode (red) is characterized by an electric field localized predominately in the Si core and a mode index of $n =$ 0.375. In contrast, the plasmonic mode (blue) exhibits maximal field intensities within the SiO_2

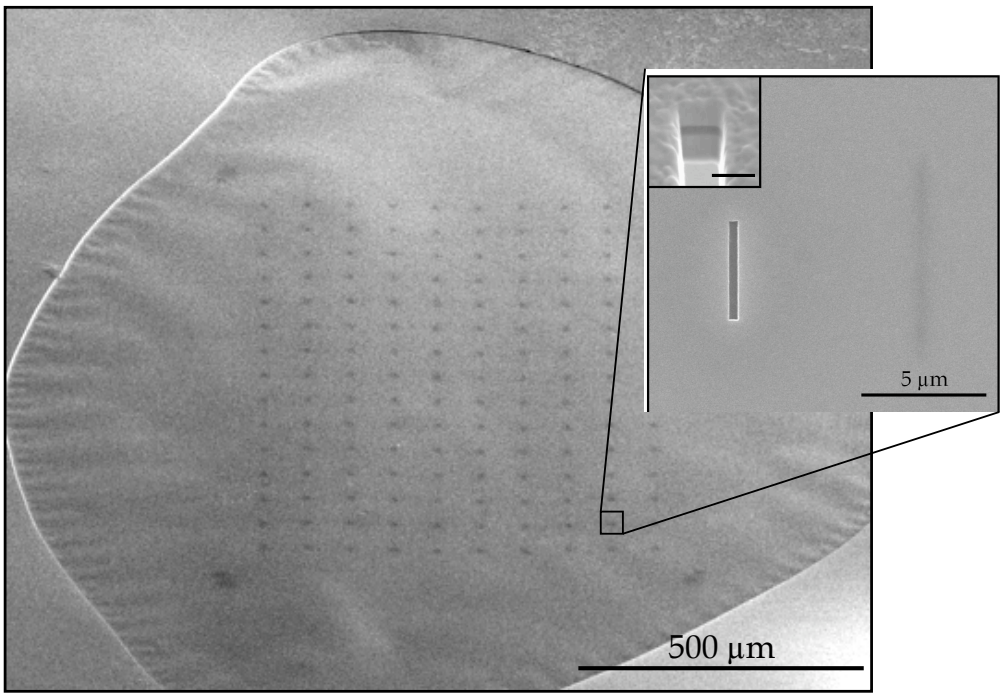


Figure 7.4. An overview of an entire plasmostor membrane. In the large inset, the input slit is visible on top of the membrane. Using high energy imaging in the SEM, we can see through the membrane and also image the output slit. The small inset shows a cross-sectional cut through the 4-layer plasmostor waveguide (scale bar is 500 nm).

channel and a mode index of n = 3.641. While the high plasmonic mode index arises from mode overlap with the Ag and Si layers, propagation losses remain relatively low. At $\lambda = 1.55\ \mu m$, losses of the plasmonic and photonic modes are 0.207 dB/μm and 2.37 dB/μm, respectively. For both modes, fields in the metal cladding decay within approximately 20 nm of the Ag-Si and Ag-SiO_2 interfaces.

For devices that were fabricated using n-type silicon, the changes just described are induced by applying a positive bias to the gate. For drive voltages above the flat-band voltage, electrons in the n-type Si form an accumulation layer characterized by a peak carrier concentration at the Si/SiO_2 interface and a spatial extent given by the Debye length. Figure 7.6 tabulates the theoretical change of mode index and propagation length with the onset of accumulation. To represent the spatially-varying charge distribution predicted by Poisson's equation, the accumulation layer is modeled as five discrete Drude layers with an average plasma frequency of 7.94×10^{14} Hz and a Debye decay length of 14 nm. The parameters used for the five-layer stack are listed in Table 7.1.

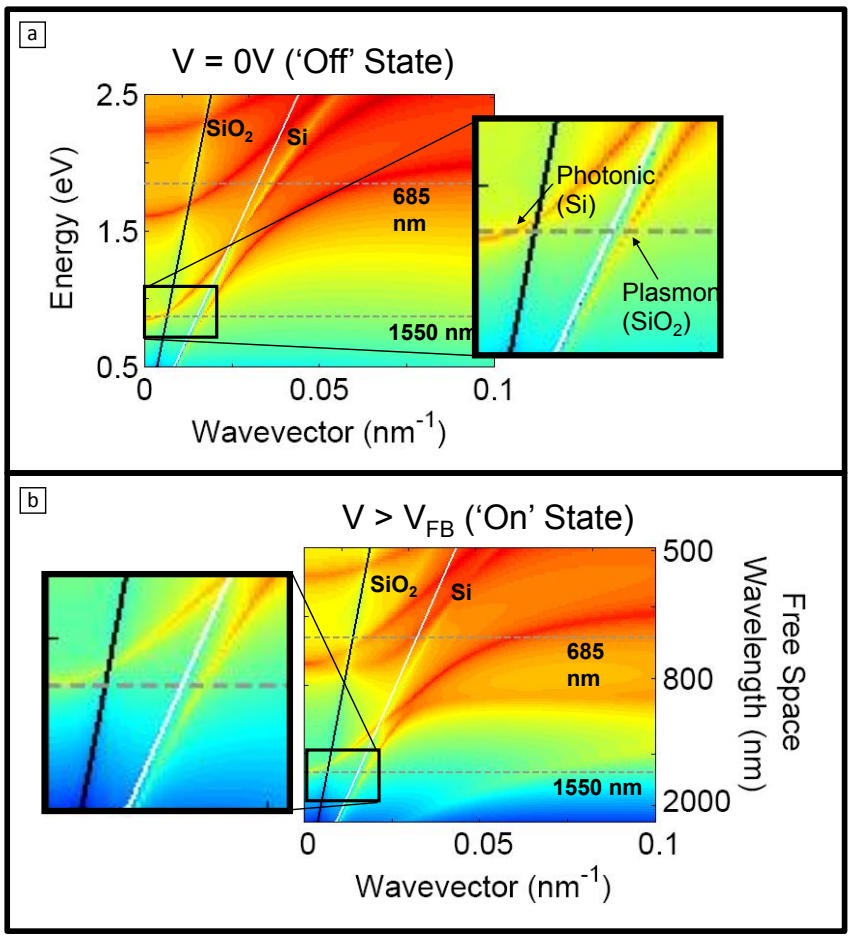


Figure 7.5. Plasmostor dispersion relation with and without and applied electric field. With no applied electric field, both the plasmonic and photonic modes contribute to device behavior. With an applied field, the photonic mode is pushed into cutoff and all that remains is the plasmonic mode.

Note that both the Drude model and the Debye approximation were used for simplicity. As expected, the effective index and losses of the plasmonic mode exhibit very little change between the voltage-off (depletion) and voltage-on (accumulation) states. In particular, the plasmonic mode index varies from the off state by $\Delta n = 0.008$, and losses are only slightly increased to 0.228 dB/μm. However, the photonic mode is pushed into cutoff, as indicated by the near-zero mode index and the fact that the losses increase by an order of magnitued (i.e., the photonic mode becomes evanescent and can no longer propagate power through the device). Therefore, in the accumulation state, the plasmostor will guide near-infrared light almost exclusively through the SiO_2 channel [61], solely via the plasmonic mode.

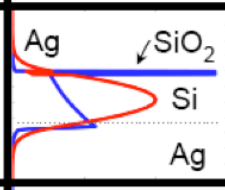
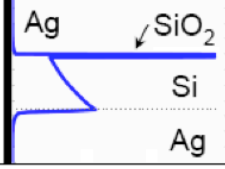
λ=1.55μm	|E| mode profile	Mode Index	Loss (dB/μm)
Off state (V=0) *depletion*		3.641	0.207
		0.375	2.37
On state (V>0.7V) *accumulation*		3.649	0.228
		0.033	28.14

Figure 7.6. Tabulated mode properties of the plasmostor with and without an applied electric field.

Table 7.1. 5-layer stack used in plasMOStor modeling.

Thickness (nm)	Carrier Concentration $\left(\mathrm{cm}^{-3}\right)$	Conductivity $\left(\mathrm{S/cm}^{3}\right)$
5	7×10^{19}	2.17×10^{6}
12	3×10^{19}	9.30×10^{5}
33	8×10^{18}	2.48×10^{5}
50	5×10^{17}	1.55×10^{4}
73	1×10^{16}	3.098×10^{2}

7.4 Switching Behavior

Modulation of the electric field distribution and out-coupled power is illustrated in the finite difference time domain simulations of Figure 7.7 and 7.8. In these simulations, the plasmostor is illuminated through the optical source with a gaussian beam of wavelength $\lambda = 1.55\ \mu m$ or $\lambda = 685$ nm, and the source-drain separation is set to d $= 2\ \mu m$. As seen in the left column of Figure 7.7, in the absence of an applied field, plasmostor transmission at $\lambda = 1.55\ \mu m$ is distributed throughout the Si core with sparse regions of high electric field in the oxide slot. However, with the onset of accumulation, the field transmitted within the Si core is notably decreased. As seen in the right column of Figure 7.7, plasmostor fields are localized predominately within the 10 nm-thick oxide layer,

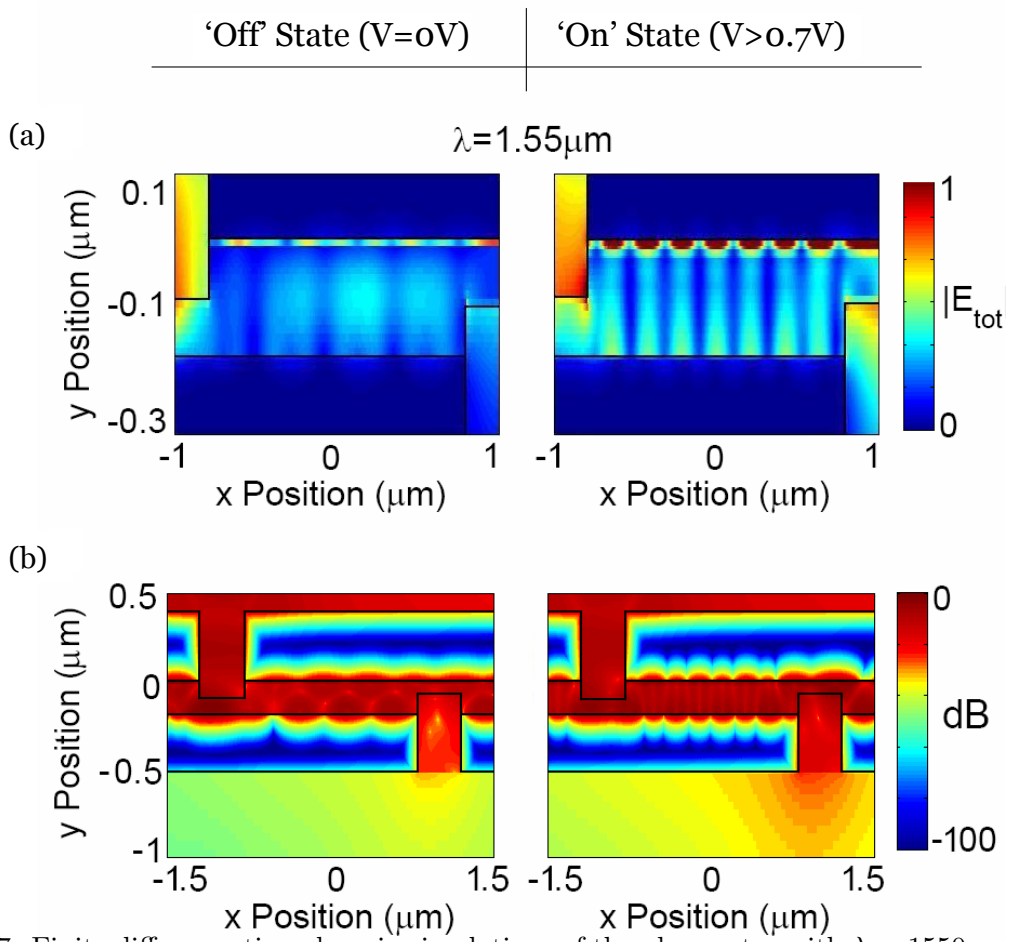


Figure 7.7. Finite difference time domain simulations of the plasmostor with $\lambda = 1550$ nm, showing the total electric field and the transmitted power for a 2-μm-long optical source-drain separation.

which acts as a channel between the optical source and optical drain. Within the slot, pronounced maxima and minima within the resonator can be observed with a wavelength of approximately 225 nm.

By choosing the source-drain separation to correspond to a condition of destructive interference between the photonic and plasmonic modes, plasmostor transmission can be substantially increased by inducing accumulation. Figure 7.7(b) plots the total power transmitted through the plasmostor at $\lambda = 1.55\ \mu m$, with d = 2 μm. Comparing intensities at the optical drain between the voltage-off and voltage-on states, simulated modulation ratios exceeding +10 dB can be observed.

For comparison, at $\lambda = 685$ nm, the unbiased plasmostor exhibits three modes with effective indices of n = 5.36, 3.40, and 2.28. An applied field shifts these indices to n = 5.35, 3.34, and 2.15. Such multimode behavior is readily visualized in the simulated images of Figures 7.8(a)

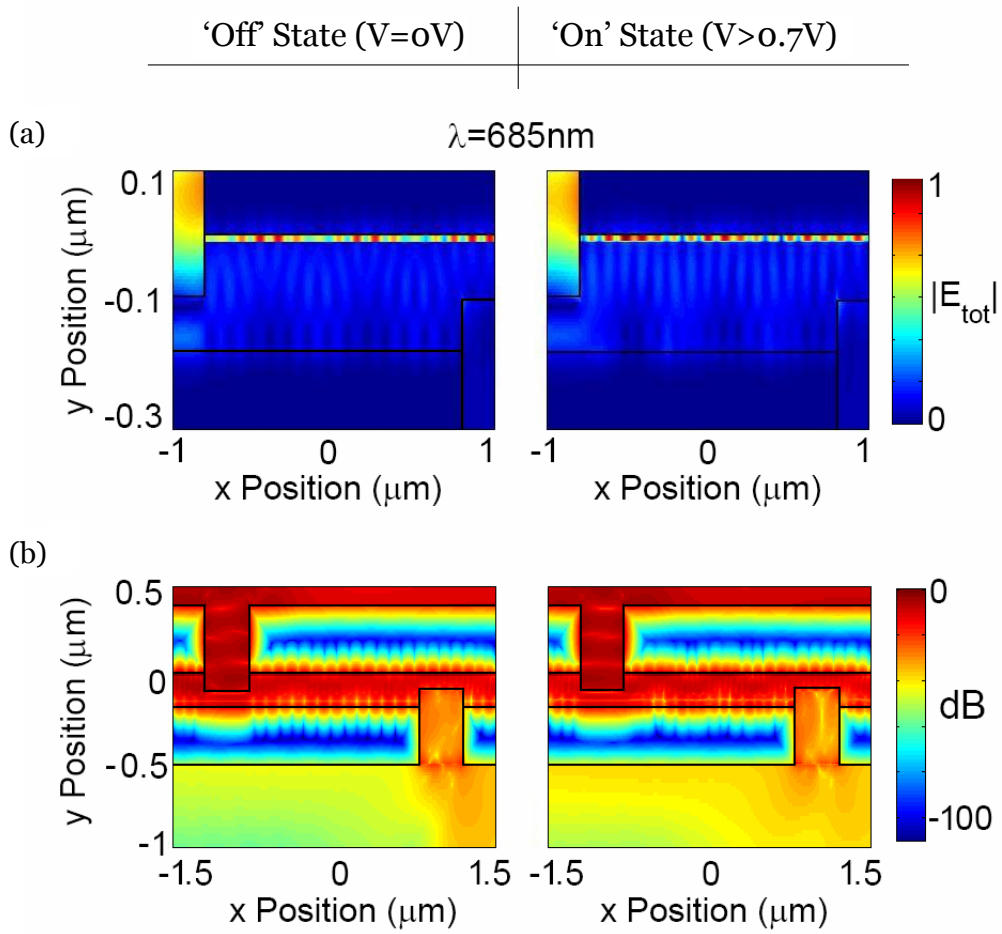


Figure 7.8. Finite difference time domain simulations of the plasmostor with $\lambda = 685$ nm, showing the total electric field and the transmitted power for a 2-μm-long optical source-drain separation.

and (b). However, because Si is more absorbing in the visible, the propagation lengths of these modes do not exceed 3 μm. The accumulation layer induces higher losses in the structure, and modulation between the voltage-on and voltage-off states results almost exclusively from absorption of all modes. The higher absorption and multi-mode behavior at visible wavelengths suggest that when the plasmostor is designed using silicon with the thicknesses reported, the device is ideally suited for near-infrared operation.

Experimental capacitance-voltage (CV) curves were used to characterize the electrical response of our fabricated plasmostor. Figure 7.9(a) shows a high-frequency CV curve obtained with a driving frequency of 100 kHz, measured over an area of approximately 100 μm $\times 100 \mu m$. As the figure reveals, the plasmostor is in a state of inversion for negative biases, depletion for biases between 0 and 0.7 V, and accumulation for biases greater than 0.7 V. The flat-band voltage, where the Si

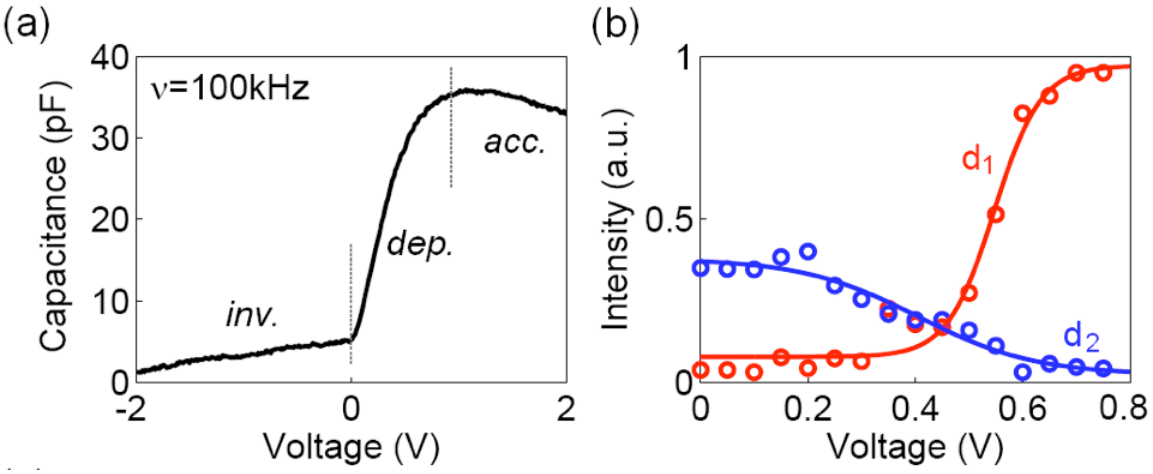


Figure 7.9. (a) High-frequency (100 kHz) capacitance-voltage curve of the modulator over a ∼100 $\times 100\mu m^2$ area. (b) Optical drain intensity as a function of gate bias for two source-drain separations ($d_1 = 2.2\ \mu m$ and $d_2 = 7.0\ \mu m$) at $\lambda = 1.55\ \mu m$.

layer is charge neutral, occurs around 0.5 V. From the total observed accumulation capacitance (35 pF) of this sample region A_{meas}, we infer the capacitance of a typical plasmostor with areal dimensions $A_{plasmostor} = 4\ \mu m^2$ as $C_{plasmostor} = C_{meas}(A_{plasmostor}/A_{meas}) = 14$ fF.

To characterize the optical response, the out-coupled intensity from the plasmostor was monitored as a function of gate bias. An infrared laser source ($\lambda = 1.55\ \mu m$) was focused onto a single device and transmission through the optical drain was imaged using a 50x microscope objective coupled to a Ge detector. Depending on the source-drain separation - and hence the interference condition of the photonic and plasmonic modes in the depleted state - transmitted intensity could increase or decrease with applied bias. As seen in Figure 7.9(b), a modulator of length $d_1 = 2.2\ \mu m$ exhibits a pronounced intensity increase with increasing positive bias for $\lambda = 1.55\ \mu m$. Consistent with the capacitance-voltage curves, modulation saturates around 0.7 V, corresponding to the onset of accumulation. In contrast, a modulator of length $d_2 = 7.0\ \mu m$ exhibits a 30% decrease in transmitted intensity for $\lambda = 1.55\ \mu m$.

This measurement was then repeated for every device shown in Figure 7.4. Full experimental optical characterization was achieved by varying the source-drain separation and the illumination wavelength, both with and without an applied bias. Figure 7.10 shows plasmostor transmission as a function of resonator length for source wavelengths of 685 nm and 1.55 μm, respectively. As

seen in the top pane of Figure 7.10, at a wavelength of 685 nm, negligible modulation is observed for TM-polarized light between the voltage on and off states of the modulator. For shorter cavity lengths, transmission predominately decreases with applied bias. Cavities longer than 2.5 μm are dominated by extinction, consistent with mode propagation lengths derived from calculations.

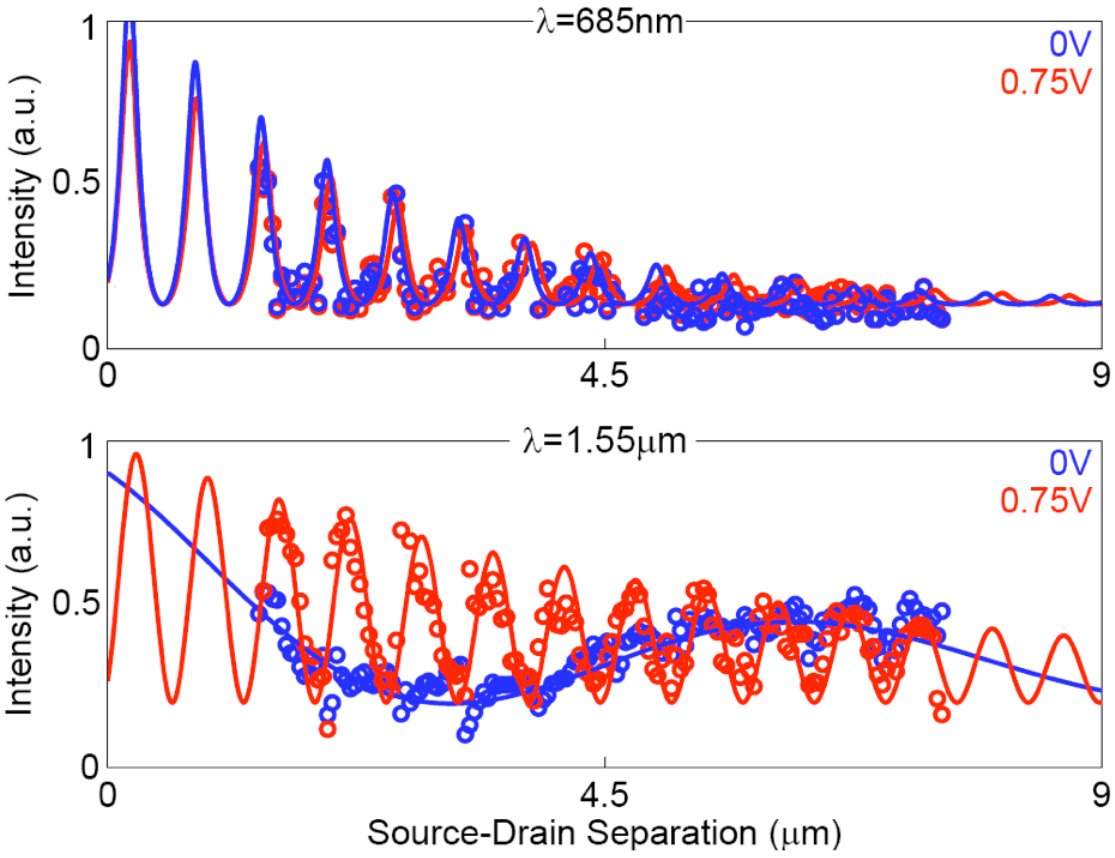


Figure 7.10. Optical drain intensity as a function of source-drain separation for the voltage-off state (blue, V = 0) and the voltage-on states (red, V = 0.75 V) at $\lambda = 685$ nm and $\lambda = 1.55$ μm.

In contrast, the plasmostor exhibits pronounced modulation for near-infrared sources. As seen in the bottom pane of Figure 7.10, with no applied bias, plasmostor transmission at $\lambda = 1.55$ μm is characterized by an output signal comprised of both high and low frequency components. As illustrated by the dispersion diagram of Figure 7.5, these components correspond to the plasmonic and photonic waveguide modes, respectively. An applied bias of 0.75 V forces the photonic mode

into cut-off, leaving only a single, high-frequency mode in the waveguide. Experimentally, the observed propagation length of this mode is in fair agreement the plasmonic mode losses predicted from calculations. The observed mode index is about half the calculated plasmon index, likely due to aliasing effects arising from the chosen optical source-drain separation step-size. Still, source-drain separations of approximately 2 μm exhibit amplitude modulation ratios as high as $+11.2 \pm 0.6$ dB. Such observations are consistent with the simulations of Figure 7.7. To our knowledge, this plasmostor yields one of the highest reported near-infrared Si modulation depths in the smallest reported volume, with device volumes as small as one half of a cubic wavelength.

Plasmostor modulation depths remain high for wavelengths spanning from 1.48 μm to 1.58 μm (the range of our infrared source), where changes in the complex refractive index of Si induce cut-off of the photonic mode. For these wavelengths, significant modulation is preferentially observed in shorter resonator lengths ($d < 3$ μm), which in the depleted state produce destructive interference between the photonic and plasmonic modes. Previous Si modulators based on MOS capacitors, in contrast, require device dimensions on the order of millimeters [68]. Interestingly, the internal waveguide propagation losses of the plasmostor are not significantly higher than 1 dB (for a source-drain separation of d = 2.2 μm, the plasmonic mode has a propagation loss of 0.5 dB). Thus, despite the higher losses generally associated with plasmonic components, the plasmostor exhibits propagation losses that are comparable with traditional Si- or dielectric-based modulators [68, 69, 124].

We note that the prototype plasmostor reported here incurs additional losses from mode insertion and extraction through the "source" and "drain" slits employed in our device. Using full field electromagnetic simulations, we calculate an insertion loss of -12.8 $\pm$ 0.1 dB and an extraction loss of -3 $\pm$ 1 dB. Combined with the waveguide propagation losses, then, this prototype plasmostor exhibits a total on-chip loss of approximately -17 dB, in rough accord with the total experimentally-determined loss of approximately -20 dB. However, we do not consider these high coupling losses intrinsic to device operation, since slit coupling is not fundamental to plasmostor modulation. In fact, our simulations indicate that by modifying the coupling geometry to simple, non-optimized end-fire excitation from a Si-waveguide, an increased coupling efficiency of 36% (coupling losses of 4.4 dB) can be achieved. Moreover, as reported by Veronis and Fan [118], optimization techniques have been proposed to achieve $> 90\%$ incoupling efficiencies into plasmonic waveguides, corresponding to coupling losses as low as 0.3 dB. Thus, future plasmostors with a device length of approximately 2 microns and more optimal incoupling could achieve overall "on" state losses as

low as 1.1 dB.

7.5 Time Response Analysis

The frequency response of the plasmostor was characterized by applying a 4 V, 100 kHz pulse train to the modulator with a rise-time of 10 ns. Plasmostor switching was determined to be at least as fast as 10 ns, which was limited by the frequency response of our pulse generator. We note, however, that modulation speeds of a plasmostor are likely to be fundamentally limited by the speed of formation of the MOS accumulation layer, as is true in a conventional small-geometry MOSFET; accordingly, plasmostor operation should be compatible with GHz modulation frequencies. This device could potentially respond even faster than traditional MOSFETs because of the fact that this device is based on forming an accumulation layer with majority carriers within the device, rather than minority carriers which are often manipulated using MOSFETs.

To explore the potential for GHz modulation in more detail, we conducted circuit simulations of our plasmostor driven into accumulation by optical means. For example, a photodiode connected to the plasmostor gate could provide sufficient power to modulate the channel properties [80]. Provided the photodiode could produce gate voltages exceeding 0.7 V, this coupled plasmostor-photodiode system could form the basis for all-optical MOS-based modulation. Figure 7.11 proposes such a scheme for all-optical modulation. As seen, a Ge p-i-n photodiode is connected to the plasmostor in parallel with a dielectric (a resistor). Here, the plasmostor is modelled using the experimentally-inferred capacticance (14 fF) of a typical 4 μm^2 device. Similarly, the photodiode is modelled using circuit parameters from state-of-the-art small photodiodes [57] exhibiting quantum efficiencies of 10% under 6 mW optical illumination. Using a photodiode with an active area of 75 μm^2 and an $\sim$ 40 GHz bandwidth [57], circuit simulation indicates coupled plasmostor-photodiode bandwidths of 3 GHz (Fig. 5a). Scaling the photodiode active area to 4 μm^2 (and thereby increasing the photodiode bandwidth [57]), coupled plasmostor-photodiode bandwidths increase to 15 GHz. Further improvements could be achieved by varying the oxide thickness or the plasmostor gate length. Moreover, by tuning the magnitude of the optical carrier (λ_1) and signal (λ_2) sources, this coupled photodiode-plasmostor system could exhibit signal gain at the plasmostor drain [80]. This three-terminal, integrated optical device requires no electronic conditioning and can be fabricated from SOI waveguide technology, using, for instance, local oxidation of silicon (LOCOS) processing. Such processing would facilitate CMOS compatibility while minimizing optical insertion losses.

7.6 Conclusion

In this chapter we have shown that the plasmostor offers a unique opportunity for compact, Si-based field effect optical modulation using scaled electronic MOSFET technology. The empirically determined switching voltage (0.7 V) and capacitance (14 fF) yield a required switching energy of $E = CV^2 = 6.8$ fJ for a typical 4 μm^2 plasmostor device, commensurate with existing CMOS and optical logic gates [69]. To our knowledge, the plasmostor achieves the first electrical amplitude modulation of light in a plasmon waveguide. Furthermore, by modulating optical signals with a photodiode coupled to the gate, the plasmostor promises potential for opto-electronic and perhaps even all-optical Si-based modulation.

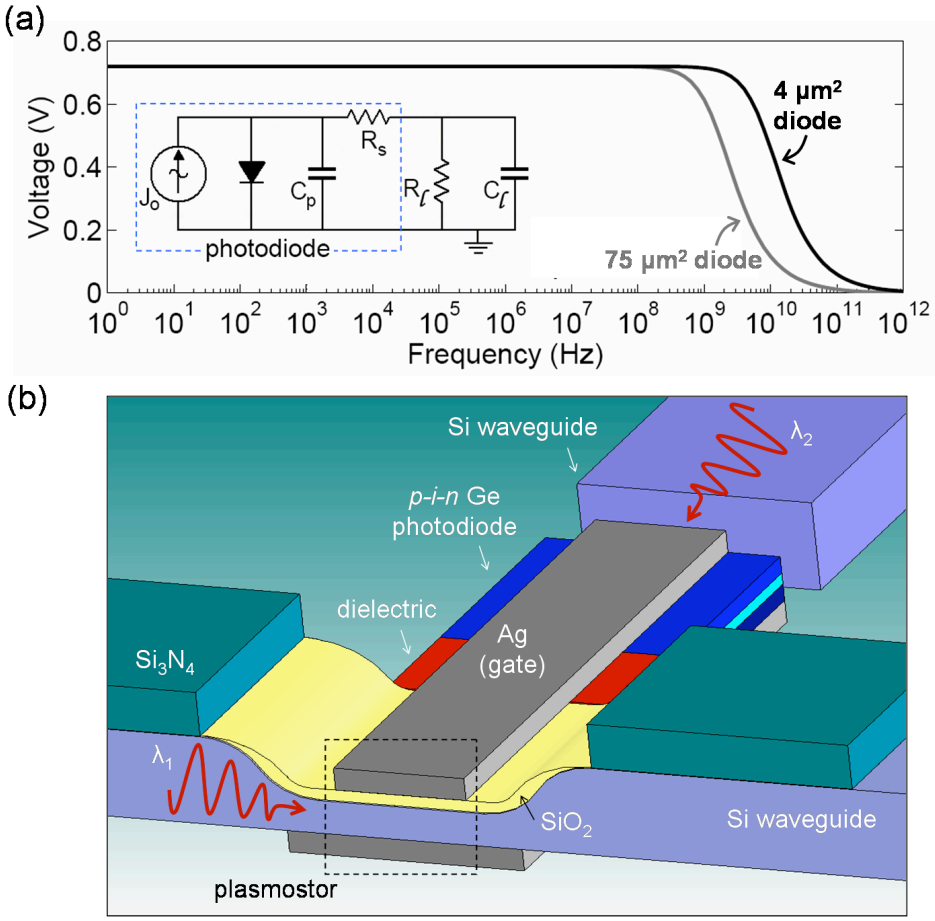


Figure 7.11. Circuit analysis of the coupled photodiode-plasmostor system, modelling the photodiode after reference [57] and the plasmostor as a MOS capacitor with a capacitance of 14 fF. (a). Schematic of an SOI-based all-optical plasmostor (b).