

# Monolithic Grid Amplifiers

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To My Parents,  
For Their Love and Patience

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# Monolithic Grid Amplifiers

## Abstract

A grid amplifier is a quasi-optical power-combining device which amplifies a microwave beam and spatially combines the outputs of many transistors, making it possible to greatly increase power. This thesis will discuss gain and stability models for Heterojunction-Bipolar-Transistor (HBT) grid amplifiers. A transmission-line equivalent-circuit model for gain analysis will be discussed. Hybrid HBT grid amplifiers, fabricated with high-dielectric substrates, have been demonstrated with gains of 11 dB at 10 GHz and 6 dB at 16 GHz. A stability model for common-mode oscillations will be presented and stabilizing techniques will be discussed. With stabilizing capacitors, a highly stable grid amplifier has been achieved at 10 GHz. Based on the models, a 36-element monolithic HBT grid amplifier is designed, fabricated and tested. The result is a highly stable monolithic grid amplifier with a peak gain of 5 dB and 3-dB bandwidth of 1.8 GHz. This monolithic HBT grid amplifier has a maximum saturated output power of 670 mW at 40 GHz. The far-field approach was employed to measure the gain and power of the grid amplifiers. Theoretical discussions on aperture efficiencies of grids and thermal modelling for a two-layer structure of a grid with a carrier will be discussed.



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- [2] C.-M. Liu, E.A. Sovero, D.B. Rutledge, "40-GHz Monolithic Grid Amplifier," *Dig. 53rd Device Research Conf.*, 1995, session IVA-8.
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- [5] M.P. De Lisio, C.-M. Liu, "Chapter 9: Grid Amplifiers," to be published in *Active and Quasi-Optical Arrays*, R.A. York and Z.B. Popović eds., John Wiley & Sons, Inc., New York, 1996.

## Contents

<b>Acknowledgements</b> .....	iii
<b>Abstract</b> .....	iv
<b>Chapter 1. Introduction</b> .....	1
1.1. Quasi-Optical Amplifiers .....	2
1.2. Grid Amplifiers .....	3
1.3. Thesis Organization .....	5
<b>Chapter 2. Hybrid HBT Grid Amplifiers</b> .....	12
2.1. Introduction .....	12
2.2. Grid-Amplifier Gain Model .....	13
2.3. Construction of 10-GHz Grid Amplifiers .....	19
2.3.1 Unit Cell .....	19
2.3.2 Hairpin Bias Lines .....	21
2.4. Measurements .....	24
2.4.1. Gain Measurements .....	25
2.4.2. Tuning Measurements .....	28
2.5. 16-GHz Grid Amplifier .....	31
<b>Chapter 3. Grid-Amplifier Stability Model</b> .....	38
3.1. Origin—Common-Mode Oscillation .....	38
3.2. Stability Model .....	42
3.3. Stabilizing the Grid Amplifiers .....	45
3.4. Measurements .....	49
<b>Chapter 4. Monolithic 40-GHz HBT Grid Amplifier</b> .....	53
4.1. Introduction .....	53
4.2. Design .....	55
4.2.1. Unit Cell .....	55
4.2.2. Stability Analysis .....	61

4.3. Fabrication .....	63
4.4. Gain Measurements .....	64
4.4.1. Frequency Response .....	65
4.4.2. Tuning Curves .....	69
4.4.3. Radiation Patterns .....	72
4.5. Power Measurements .....	72
4.6. Tiling Issue .....	74
<b>Chapter 5. Far-Field Measurements .....</b>	<b>85</b>
5.1. Calibration Measurements .....	85
5.2. Power Gain Measurements .....	88
5.3. Validation Measurements .....	89
5.4. Computation Models for Aperture Efficiency Analysis .....	91
5.5. Simulations for Grid Aperture Efficiencies .....	96
5.5.1 Aperture Efficiency versus Unit-Cell Period .....	96
5.5.2 Aperture Efficiency versus Mirror Distance .....	97
5.5.3 Aperture Efficiency versus Array Size .....	102
<b>Chapter 6. High-Power Millimeter-Wave Amplifiers .....</b>	<b>104</b>
6.1: Thermal Examination .....	105
6.1.1. Thermal Modelling .....	106
6.1.2. Thermal Simulations for a 20-W 16×16 Tiled Grid .....	108
6.2. Approach to a High-Power Amplifier .....	111
6.2.1. Improving Power Capability .....	111
6.2.2. Improving Thermal Performance .....	112
6.2.3. Tiling Technology .....	113
6.3. A Cascade Quasi-Optical Amplifier System .....	113

# Chapter 1

## Introduction

The applications of millimeter-wave technologies have been growing in recent years, particularly in the commercial area [1]. These applications include satellite communications, Wireless Local Area Networks (WLAN's), a vehicle-crash-avoidance system, and an airplane landing image camera. The demand for low-cost and reliable components is growing. However, at millimeter-wave frequencies, the output power of solid-state devices is limited. Quasi-optical power combining technology is a promising approach to the satisfaction of these high-frequency applications.

Quasi-optical devices combine the output powers of many solid-state transistors/diodes in free space without the conduction losses associated with a conventional microstrip feed network. In 1983, Lothar Wandering and Vahakn Nalbandian demonstrated a millimeter-wave power combiner using two InP Gunn oscillators within a quasi-optical resonator [2]. In 1986, James Mink proposed the concept of quasi-optical power combining—an efficient approach to solid-state millimeter-wave sources by using quasi-optical resonators and monolithic source arrays [3]. Following this concept, significant progresses have been made by various groups. Review articles on the development of quasi-optical technology have been published [4,5]. Very recently, a book devoted to quasi-optical technology has been submitted for publication [6].

Nowadays, much of the quasi-optics research has been shifting to amplifiers [7–30]. Quasi-optical amplifiers, using hybrid technology, have demonstrated

output power levels up to 3.7 W at 9 GHz [11]. These hybrid quasi-optical amplifiers were fabricated by mounting transistors on printed-circuit boards with embedded antennas. Hybrid technology offers the researchers flexibility and convenience in investigating the performance of quasi-optical amplifiers, including detailed comparison between theoretical prediction and measurement. Nevertheless, at millimeter wavelengths, the small dimensions and parasitic effects make construction difficult. Monolithic technology, integrating all components on a GaAs substrate, is a solution for the millimeter-wave amplifiers. Quasi-optical amplifiers are planar structures that are quite suitable for monolithic fabrication. Several groups have competed to construct a monolithic millimeter-wave amplifier with gain. Two attempts for monolithic quasi-optical amplifiers have been reported with 0-dB gains [31,32]. We have demonstrated the first successful monolithic quasi-optical amplifier with a peak gain of 5 dB and a maximum output power of 670 mW at 40 GHz [13–15]. This was soon followed by two successful amplifiers using pHEMT's [16,33]. High-power monolithic quasi-optical amplifiers are now being pursued by several groups. These high-power quasi-optical amplifiers are now the subject of a major ARPA initiative.

### 1.1 QUASI-OPTICAL AMPLIFIERS

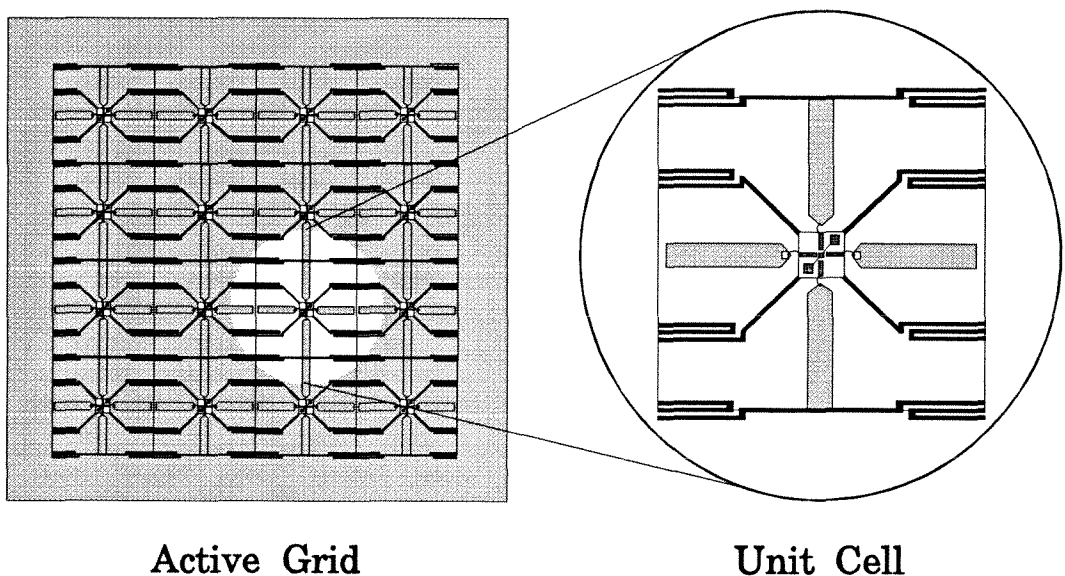
A quasi-optical amplifier receives an input beam from free space and re-radiates an amplified output beam into free space. Because of the interaction with beams in free space, quasi-optical amplifiers eliminate the conduction losses associated with conventional feeding networks—waveguides or transmission lines. In addition, it is straightforward in principle to increase the power simply by increasing the area of the amplifier, either with a larger chip or by tiling chips. This also allows us to use many low-power transistors to produce a high-power beam. This quasi-optical power combining technology is a promising approach to high-power amplifiers for millimeter wavelengths.

In the past few years, various quasi-optical amplifiers have been devel-

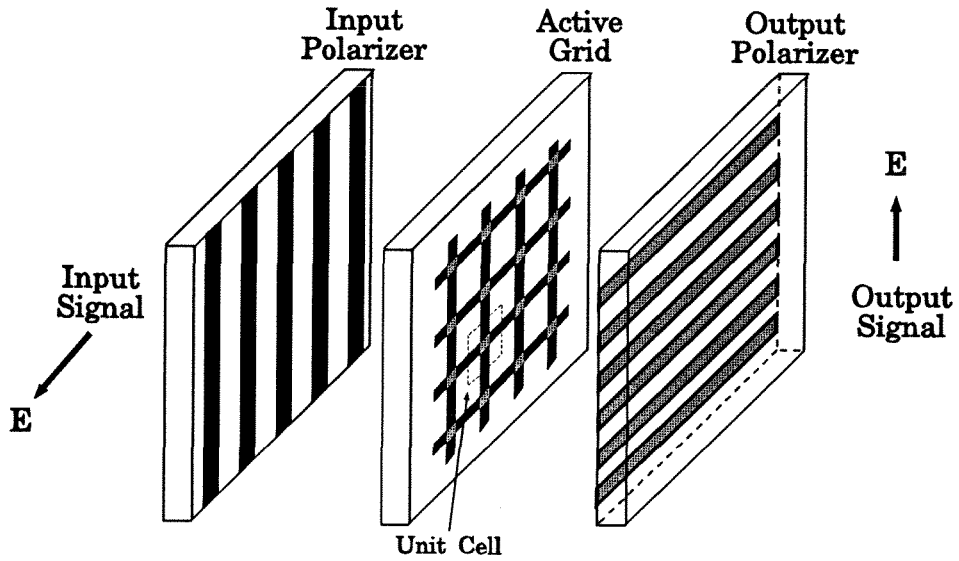
oped [7–33]. The first quasi-optical amplifier was a  $5 \times 5$  MESFET grid amplifier [7]. Following the first success, the grid-amplifier approach has been successfully applied at X band [8–12], and Ku band (Sec. 2.5). Very soon, monolithic grid amplifiers demonstrated appreciable gains at Ka band [13–15] and U band [16]. Other approaches have been demonstrated by using back-to-back horn antennas [17,18], probe antennas [19], patch antennas [20–27], and slot antennas [28–30]. Very recently, monolithic quasi-optical amplifiers, using slot and patch antennas, have been demonstrated by Emilio Sovero at Rockwell Science Center [31,33]. High-power and high-frequency quasi-optical amplifiers, using monolithic technology, are being pursued.

## 1.2 GRID AMPLIFIERS

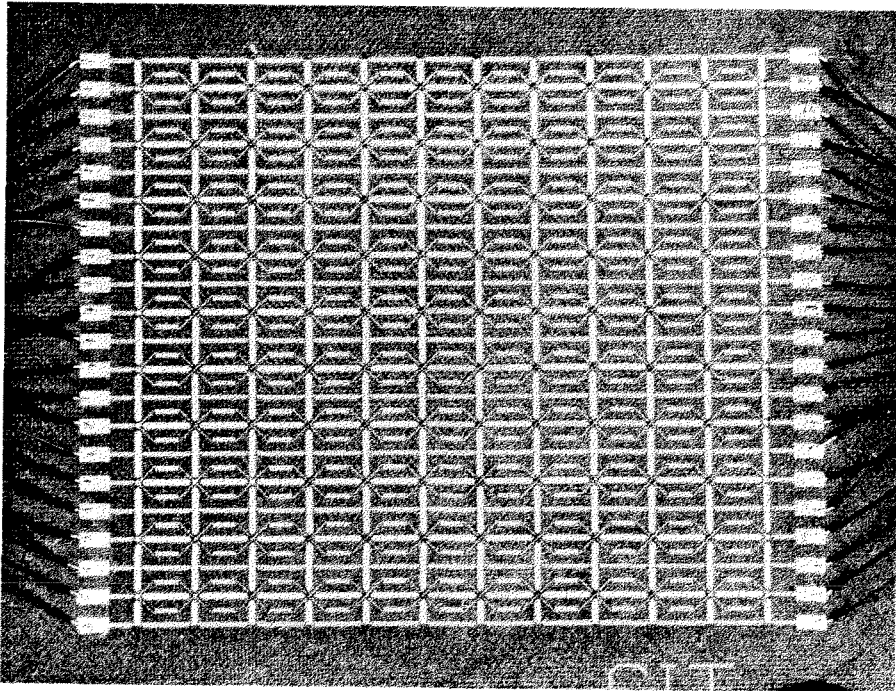
Figure 1.1 shows a typical  $4 \times 4$  active grid, with 16 unit cells periodically distributed on a substrate. Essentially, a grid amplifier is composed of an active grid and two polarizers, as shown in Fig. 1.2. The input beam is fed from the left with horizontal polarization. The output beam is measured on the right with



**Fig. 1.1.** An active grid is composed of many unit cells periodically distributed on a substrate.



**Fig. 1.2.** A grid amplifier is composed of an active grid, an input polarizer, and an output polarizer. Matching conditions are determined by polarizers' positions.



**Fig. 1.3.** Photo of the 100-element HBT grid amplifier developed by Dr. M. Kim [10].

vertical polarization. The active grid interacts with the input and output beams and contributes the amplification. Two polarizers are to confine the signal flow to transmission direction and tune the amplifier.

The first grid amplifier, also the first quasi-optical amplifier, has been demonstrated by Moonil Kim in 1991 [7]. The first grid, using MESFET transistors, had a peak gain of 11 dB at 3.3 GHz. Very soon, successful 10-GHz grid amplifiers, using HBT differential pairs [34], were also demonstrated by Dr. Kim [8–10]. Figure 1.3 shows the full-size 10×10 HBT amplifier grid. This grid has a peak gain of 10 dB and a saturated output power of 450 mW at 10 GHz. Accompanied with the modelling development, a 10×10 pHEMT grid amplifier was demonstrated by Michael De Lisio [11]. This pHEMT grid amplifier has a peak gain of 12 dB and a saturated output power of 3.7 W at 9 GHz. In the meanwhile, 4×4 HBT grids, fabricated with high-dielectric substrates, were reported with gain and stability models [12]. These grids were fabricated by hybrid technology with

Freq. (GHz)	Array	Devices	Type	Substrate $\epsilon_r$	Gain (dB)	$P_{out}$ (mW)	Eff. %	Reference
3.3	5×5	MESFET	Hybrid	2.2	11	—	—	[7]
10	10×10	HBT	Hybrid	2.2	10	450	5	[10]
9	10×10	pHEMT	Hybrid	2.2	12	3700	12	[11]
10	4×4	HBT	Hybrid	10.8	11	—	—	[12]
16	4×4	HBT	Hybrid	10.8	5.7	—	—	Sec. 2.5
40	6×6	HBT	Monolithic	12.8	5	670	4	[15]
44–60	6×6	pHEMT	Monolithic	12.8	2.5–6.5	—	—	[16]

Table 1.1 Summary of grid amplifiers. Tabulated characteristics are: operating frequency, array format, active devices, fabrication technology, substrate dielectric constant, peak gain, output power, power-added efficiency, and reference.

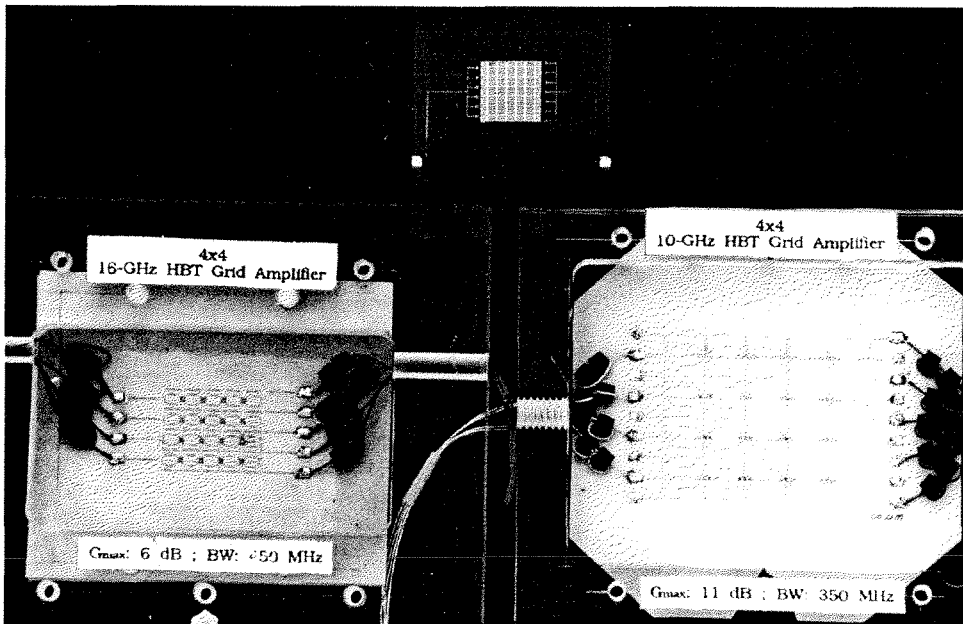


transistor chips mounted on printed-circuit boards. With a planar structure, the grid amplifier is very attractive for monolithic fabrication. Very recently, based on the developments of the hybrid grids, two successful monolithic grid amplifiers have been reported [13–16]. The salient characteristics and performances of the grid amplifiers are summarized in Table 1.1.

### 1.3. THESIS ORGANIZATION

This thesis discusses gain and stability models for the HBT grid amplifiers. Three HBT grid amplifiers, for 10 GHz, 16 GHz, and 40 GHz, are demonstrated. Figure 1.4 shows a photo of three HBT active grids.

In Chapter 2, a gain model for the HBT grid amplifier is discussed. A transmission-line equivalent-circuit model is presented. Analysis and modelling of the hairpin bias line are also discussed. Two 10-GHz hybrid grids, fabricated with high-dielectric substrates, are reported. Moreover, gain and tuning mea-



**Fig. 1.4.** Photo of three HBT grid amplifiers, 10-GHz hybrid grid (right bottom), 16-GHz hybrid grid (left bottom), and 40-GHz monolithic grid (top).

measurements are compared with theory. A 16-GHz grid amplifier, with a peak gain of 5.7 dB, is also demonstrated.

Chapter 3 investigates the stability of the grid amplifier and discusses the stabilizing techniques. Based on the analysis of oscillation patterns, an equivalent-circuit model for the common-mode oscillations is presented. Resistive and reactive approaches to grid stabilization are discussed. A highly stable grid amplifier, with stabilizing capacitors, is reported.

The subject of Chapter 4 is the design and performance of a 36-element monolithic HBT grid amplifier. This grid, the first successful monolithic quasi-optical amplifier, has a peak gain of 5 dB at 40 GHz and a 3-dB bandwidth of 1.8 GHz (4.5%). The maximum output power is 670 mW at 40 GHz. Gain, radiation patterns, tuning, and power measurements are demonstrated. Measurements of the tiled monolithic grids are also reported.

Chapter 5 describes the setups and calibration procedures for the power measurements of the grid amplifier. Two validation measurements are also demonstrated. The computational models for the aperture efficiencies of grids are discussed. The simulation results can be treated as a validation for the assumption that the antenna aperture of the grid is equal to its geometric area. Mirror effects to the aperture efficiencies are demonstrated.

The plan for the second-generation monolithic power grid is discussed in Chapter 6. The future work is to modify the design to improve the power capability and thermal performance of the monolithic grid. The thermal model for a two-layer structure is used to examine the thermal performance of the power grid. Simulations for the proposed 20-W  $16 \times 16$  power grid amplifier are discussed. A 35-GHz cascade quasi-optical amplifier system with a predicted 20-W output power is described.

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## Chapter 2

# Hybrid HBT Grid Amplifiers

Recently, a variety of hybrid quasi-optical power-combining amplifiers have been explored by various groups [1–16]. These amplifiers were fabricated by hybrid technology—that is, mounting transistors on a printed-circuit board with embedded antenna structures. Without special assembly techniques, hybrid quasi-optical amplifiers can be fabricated with commercial devices. Hybrid technology offers the researchers flexibility and convenience in investigating the gain and stability performance of quasi-optical amplifiers.

This chapter discusses the development of hybrid HBT grid amplifiers. A gain model for HBT grid amplifiers is presented. A hairpin bias line is discussed and used in a 10-GHz grid amplifier. Grid amplifiers were fabricated with Duroid substrates of relative dielectric constants of 10.8. The active devices are Heterojunction-Bipolar-Transistor (HBT) differential pairs, designed and fabricated by the Rockwell Science Center. A 16-element hybrid grid amplifier, using stabilizing capacitors, has a peak gain of 11 dB at 10 GHz and a 3-dB bandwidth of 350 MHz. Measured gain responses and tuning curves are compared with theory. Furthermore, a 16-element hybrid HBT grid amplifier, with a peak gain of 5.7 dB at 16 GHz, is demonstrated.

### 2.1 INTRODUCTION

Quasi-optical amplifiers combine the output powers of solid-state devices and thereby can greatly increase the power capability. Moreover, combining

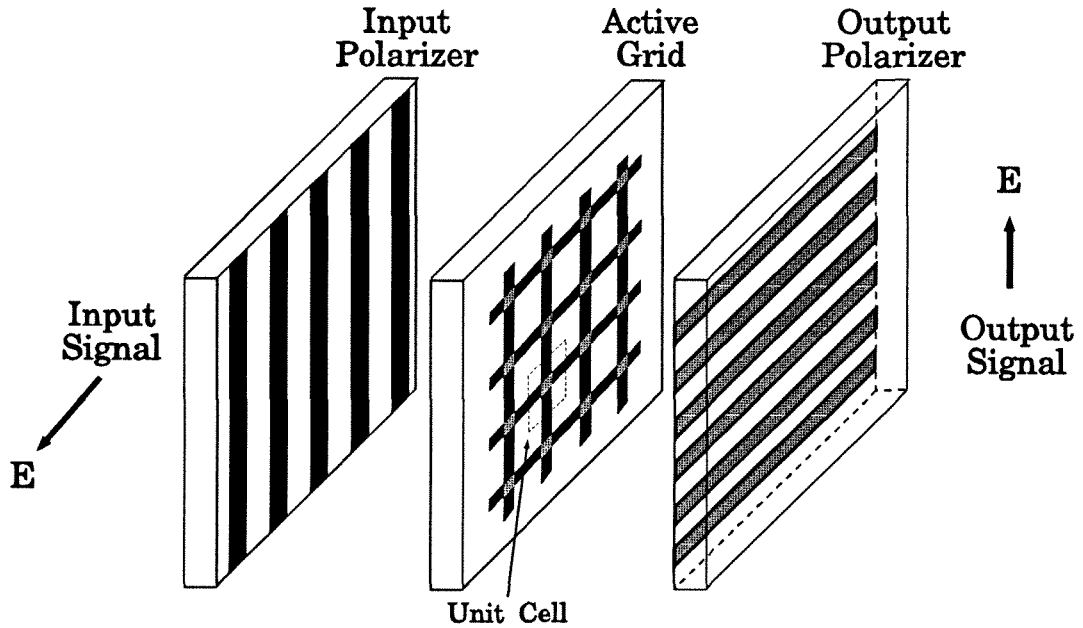
power in free space also eliminates losses associated with waveguide walls and feed networks. Dr. Moonil Kim has demonstrated the first successful quasi-optical amplifier—a 25-element MESFET grid amplifier at C-band [13]. This pioneering grid has a two-layer structure with RF components on front side and bias networks on back side. The second successful grid amplifier was a 100-element HBT grid, also developed by Dr. Kim [14]. This HBT grid, with planar structure, had a peak gain of 10 dB and an output power of 450 mW at 10 GHz. However, these grids were designed empirically. Recently, Dr. Michael DeLisio has demonstrated a 100-element pHEMT grid with a 12-dB peak gain and a 3.7-W output power at 9 GHz [15]. Very recently, monolithic quasi-optical amplifiers have demonstrated further successes at millimeter-wave frequencies [17–20]. This chapter will discuss the gain model for the HBT grid amplifiers and demonstrate the performance of grids at 10 and 16 GHz.

## 2.2 GRID-AMPLIFIER GAIN MODEL

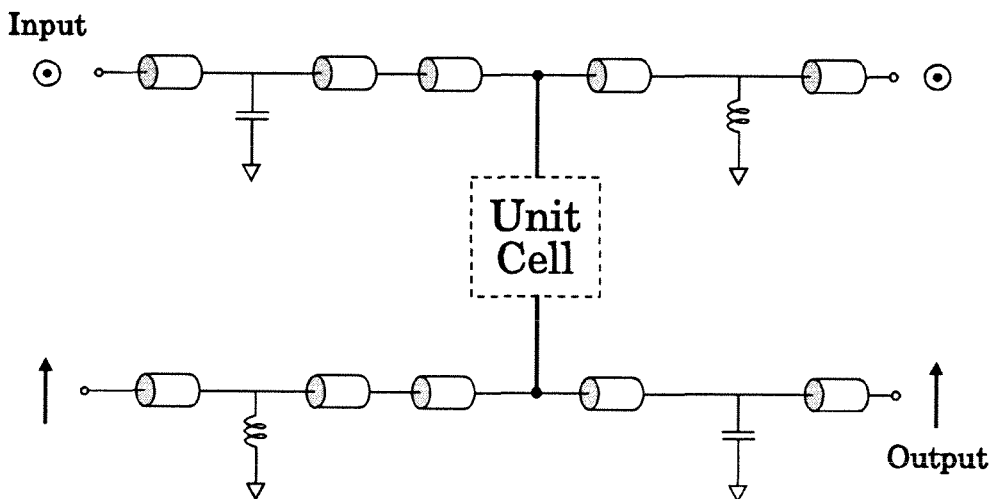
Figure 2.1 shows a conceptual grid amplifier. A basic grid amplifier is composed of an active grid, an input polarizer, and an output polarizer. An input is fed from the left with horizontal polarization, and is received and amplified by the active grid. The active grid radiates the amplified output to the right with vertical polarization. Two polarizers are to confine the signal flow from the left to the right and tune the matching conditions.

The basic grid amplifier can be modelled by a transmission-line equivalent-circuit model, as shown in Fig. 2.2 [16]. In this model, dielectric layers and air spacings of the grid amplifier are represented by transmission lines. The upper portion of the equivalent circuit is for the horizontal polarization—the input. Similarly, the lower portion is for the vertical polarization—the output. The unit cell links input and output, and contributes to the amplification. Polarizers are modelled by inductors and capacitors depending on the metal-stripe orientations [21,22]. These two polarizers, with low inductive impedances and high

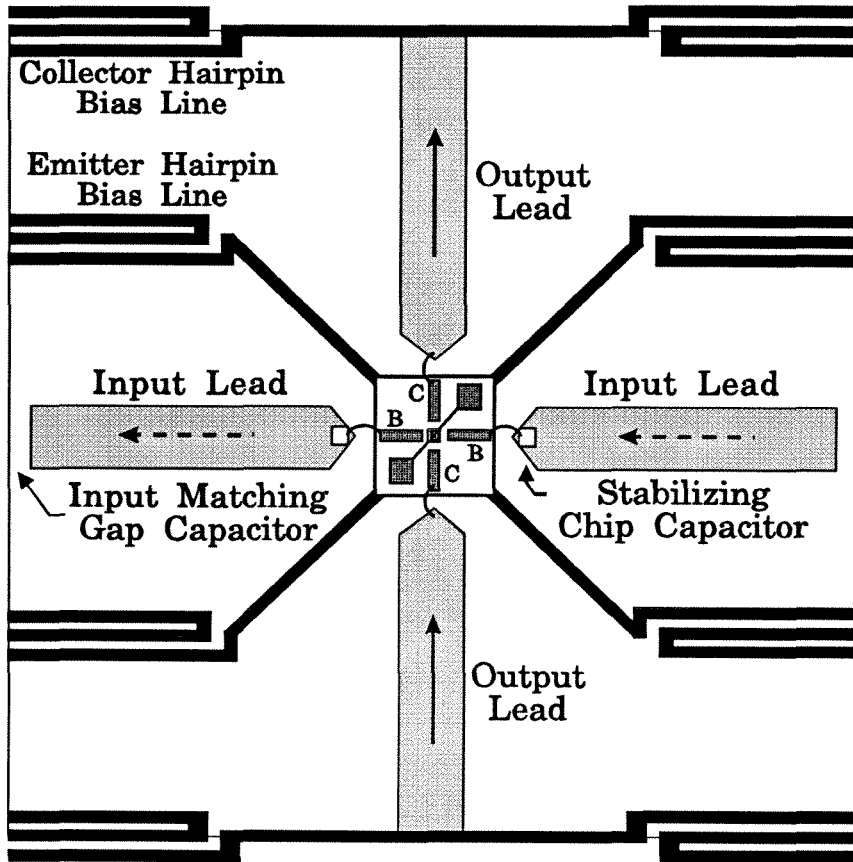




**Fig. 2.1.** A grid amplifier. Essentially, a grid amplifier is composed of an active grid, input and output polarizers. The input is fed from the left, with horizontal polarization. The output is received on the right, with vertical polarization.



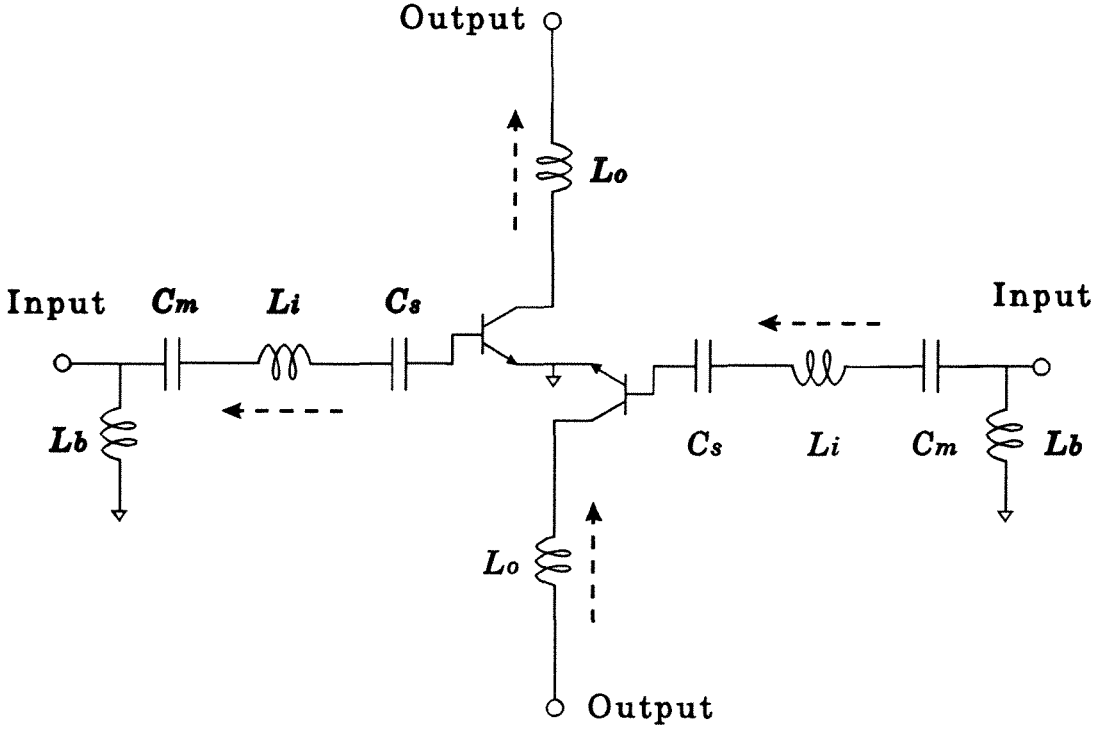
**Fig. 2.2** Transmission-line equivalent-circuit model. The upper portion of the circuit is for the horizontal polarization, the input. The lower portion of the circuit is for the vertical polarization, the output. The unit cell links the input and output.



**Fig. 2.3** A unit cell. Input leads receive the horizontally polarized input and output leads radiate the vertically polarized output. Transistors are biased through hairpin bias lines.

capacitive impedances, confine the signal flow to the desired direction—the left, horizontally-polarized input, to the right, vertically-polarized output.

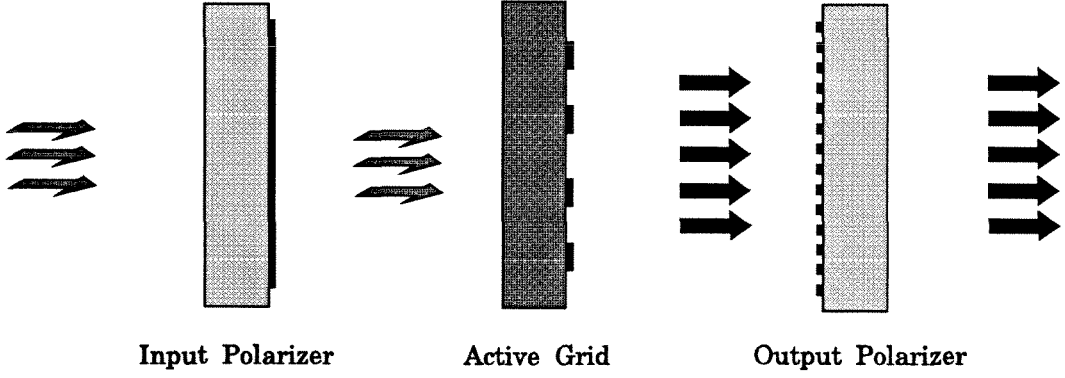
An active grid is composed of many unit cells periodically distributed on a dielectric substrate. The behavior of the active grid is, therefore, characterized by the unit cell. A unit cell of the 10-GHz active grid is shown in Fig. 2.3. In the unit cell, an HBT differential pair is located in the center and biased by horizontal bias lines. The horizontally polarized input is received by the input leads and induces RF currents, driving the transistor pair in differential mode. The RF currents are amplified by the transistors and reradiated through the vertical



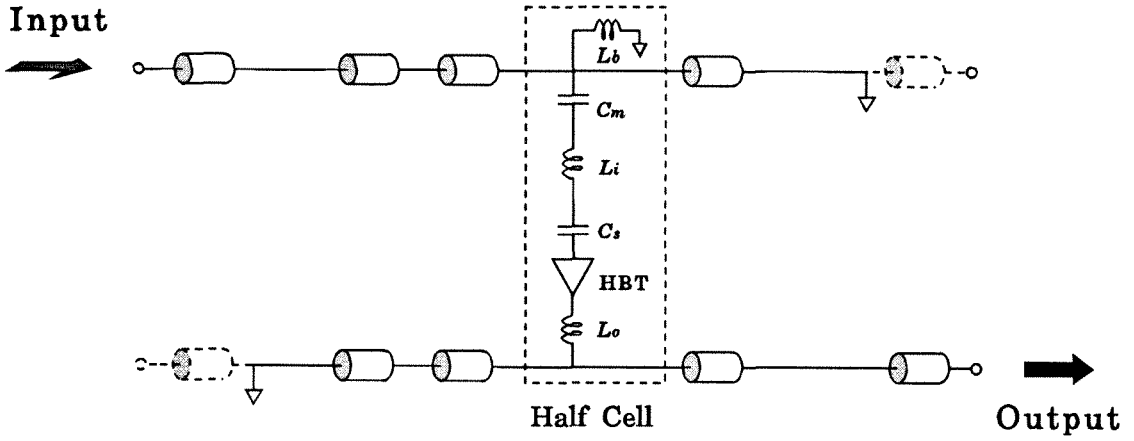
**Fig. 2.4** Equivalent circuit of the unit cell. Input and output leads are represented by inductors. Input matching gap capacitor is to compensate the input lead inductance. The function of the stabilizing capacitor is to improve the amplifier stability. A virtual ground results from the differential operation of the transistors.

output leads as the output, with vertical polarization. The perpendicularity of input and output leads results in cross-polarization of input and output thus establishing the isolation.

Figure 2.4 shows the model for the unit cell. For the unit cell, the input and output leads are modelled by inductors,  $L_i$  and  $L_o$ . The input matching gap capacitor,  $C_m$ , is to match the inductive impedance of the input lead. The stabilizing capacitor,  $C_s$ , improves the stability of the grid amplifier [16], as discussed in Chapter 3. The bias lines are mainly directed horizontally and are represented by an inductor,  $L_b$ .



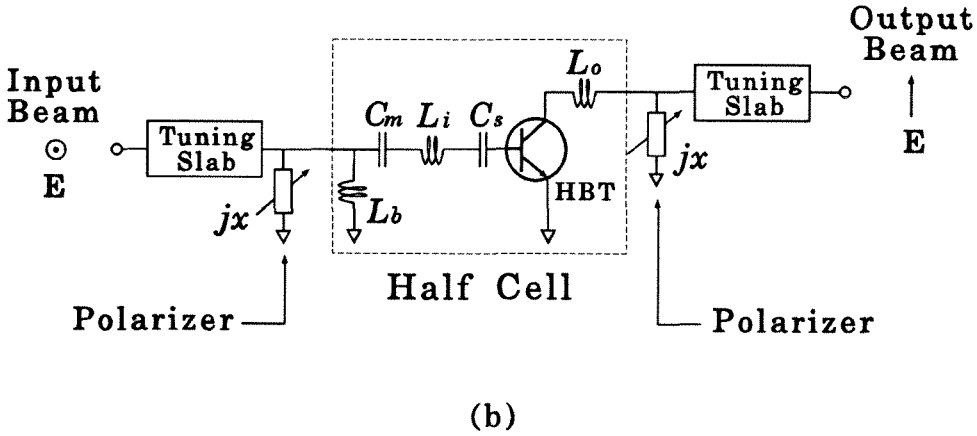
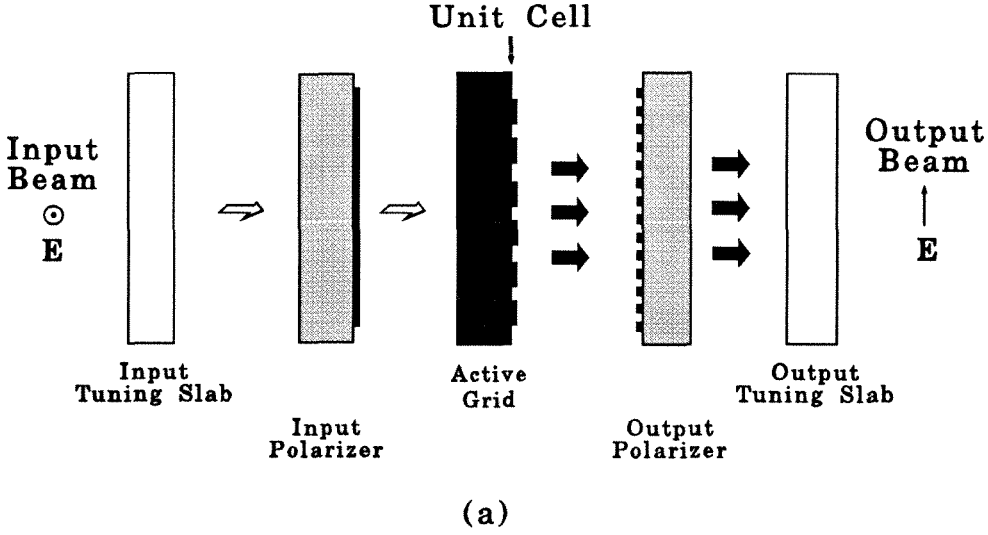
(a)



(b)

**Fig. 2.5** (a) Sideview of a grid amplifier. (b) Transmission-line equivalent-circuit model. Due to the differential-operation mode, the characteristic impedances of transmission lines are half of their dielectric impedances, and the input and output are linked by half cell.

Because of the RF differential currents, a virtual ground can be introduced into the unit cell and the rest of the grid. Therefore, the behavior of the grid amplifier is determined by the half cell [14,15]. Based on the analysis of the half cell, a grid amplifier (Fig. 2.5(a)) can be modelled as Fig. 2.5(b). The character-



**Fig. 2.6** (a) Sideview of a grid amplifier with both input and output tuning slabs. (b) Simplified equivalent-circuit model. The active grid is tuned reactively by the polarizers and resistively by the tuning slabs.

istic impedances of the transmission lines are half of the dielectric impedances,  $\sqrt{\epsilon/\mu}$ .

To improve the matching conditions, tuning slabs were used at input and/or output ends [14–16]. A tuning slab is a dielectric layer and is represented by transmission lines in the model. Qualitatively speaking, the input of the active grid is tuned reactively by the output polarizer and resistively by the input tuning

slab. On the other hand, the output of the active grid is tuned reactively by the input polarizer and resistively by the output tuning slab. Figure 2.6 shows a grid amplifier with input and output tuning slabs and a simplified equivalent-circuit model.

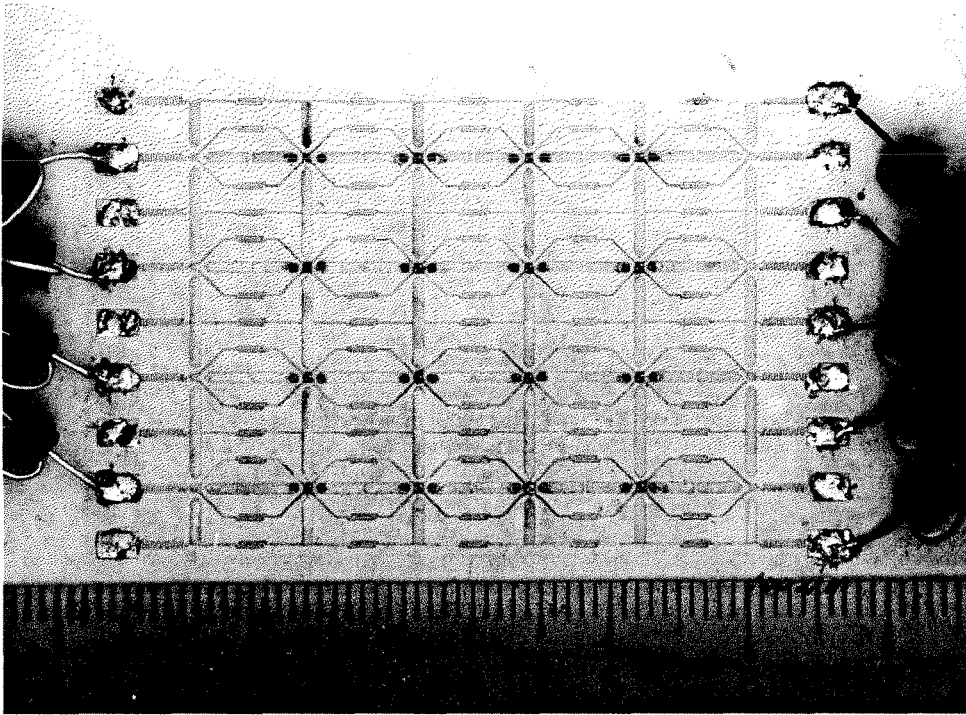
### 2.3 CONSTRUCTION OF A 10-GHZ GRID AMPLIFIER

Two 16-element active grids were fabricated on a Duroid substrate. Figure 7 shows a photo of one of the grids with hairpin bias lines. The Duroid substrate is 50-mil thick with a relative dielectric constant of 10.8. This is the first grid amplifier fabricated with a substrate of high dielectric constant. The active devices were AlGaAs/GaAs HBT's fabricated by Dr. Sovero at Rockwell Science Center.

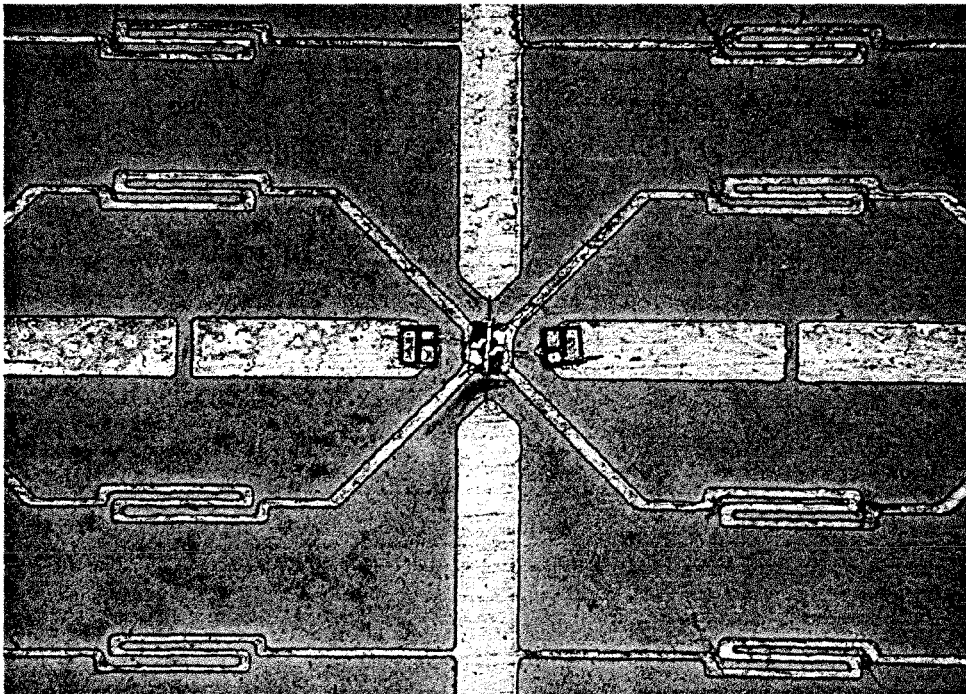
#### 2.3.1 UNIT CELL

The unit cell has 8 mm on a side, as shown in Fig. 2.8. The input and output leads are 0.8 mm wide. Based on a method-of-moment calculation [22], the inductances of the input and output leads are 1.7 nH. The input matching gap is 2 mm with a capacitance of 0.27 pF, derived from Hewlett-Packard High-frequency-Structure-Simulation (HFSS) [23]. The stabilizing capacitor is a binary-valued chip capacitor with capacitances of 0.18, 0.36, and 0.7 pF. This binary-valued capacitor was used to test the stability of the grid.

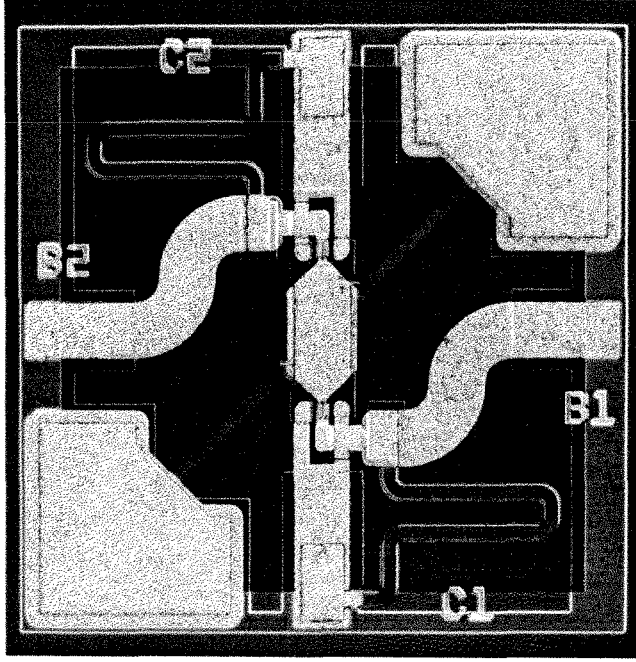
Figure 2.9 shows a photo of the HBT differential-pair chip. The chip dimensions are 600  $\mu\text{m}$  on a side [24]. The HBT transistor has a 40  $\mu\text{m}^2$  effective area. The transistor, with common-emitter configuration, is self-biased by a 2 k $\Omega$  resistor. Only one DC supply is required to bias the transistor. This self-bias configuration simplifies the bias network of the active grid and makes it possible to have a completely planar structure—an attractive structure for monolithic technology. Two 750- $\Omega$  emitter resistors are to reduce the common-mode gain of the transistor and should not affect the RF performance.



**Fig. 2.7** A 10-GHz hybrid HBT active grid with hairpin bias lines. There are four elements on a side. The grid is biased by horizontally directed hairpin lines.



**Fig. 2.8** A unit cell of the 10-GHz HBT active grid. The unit cell has 8 mm on a side.



**Fig. 2.9** HBT differential-pair chip. The chip dimensions are  $600\ \mu\text{m}$  on a side [24].

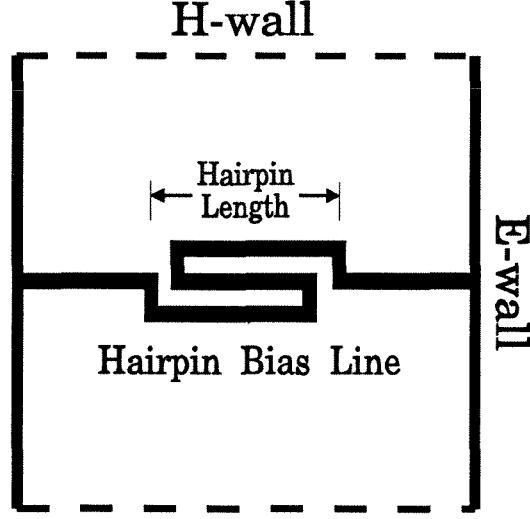
The HBT transistor with common-emitter configuration has a maximum available gain of 18 dB at 10 GHz. The small-signal model and details of the HBT transistor are shown in Sec. 4.2.

### 2.3.2 HAIR-PIN BIAS LINES

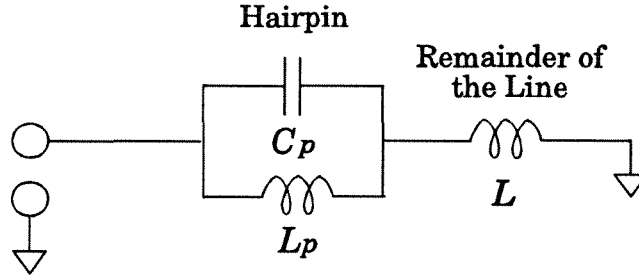
Conventionally, meandering metallization lines are employed to bias the transistors. However, the bias lines, parallel to the input leads, act as a low-impedance inductance at the input end,  $L_b$ , as shown in Fig. 2.5. For meandering lines, the bias-line inductance,  $L_b$ , is about one third of the straight-line inductance. To avoid shorting out the input, the bias-line impedance should be made highly reactive thus increasing the input-lead inductance. High bias-line inductance will limit the unit cell to a large dimension.

The hairpin bias lines are designed to have high impedance at the design frequency, as shown in Fig. 2.10.(a). The preliminary length of the hairpin was





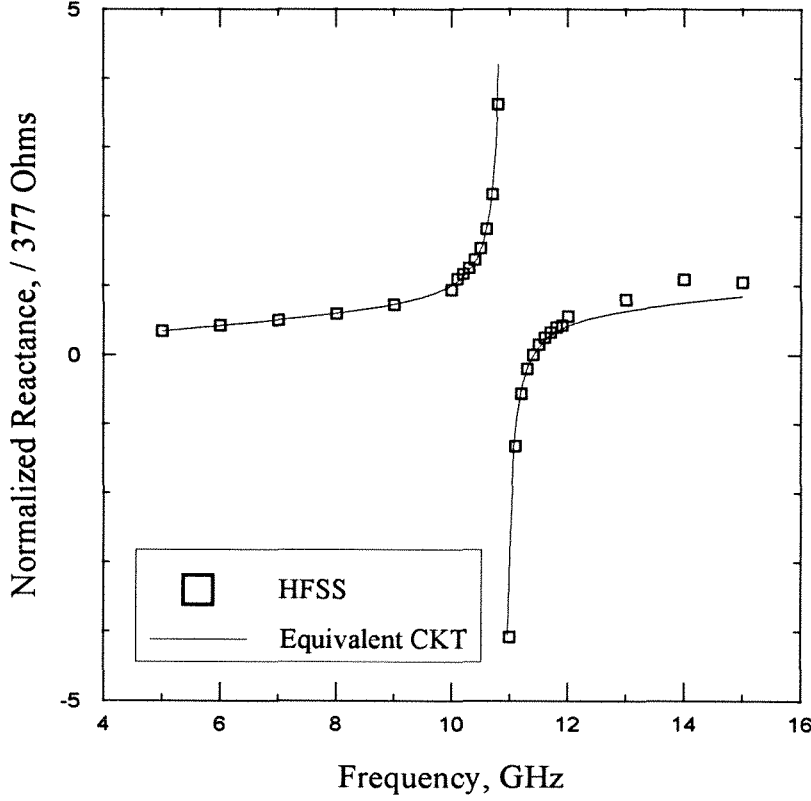
(a)



(b)

**Fig. 2.10** (a) A unit cell for the hairpin bias line. (b) Lumped-element equivalent circuit. The hairpin is represented by a parallel resonator and the remainder of the line is represented by an inductor.

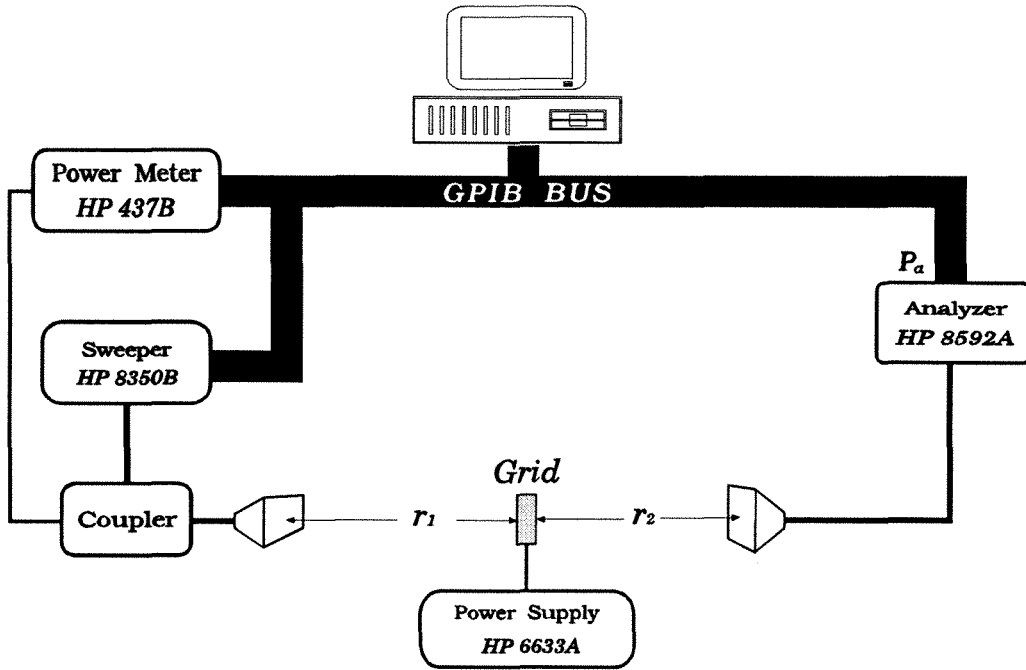
a quarter of wavelength for a material with the mean dielectric constant of the substrate and air at the design frequency. Figure 2.10(b) shows the equivalent-circuit model for the hairpin bias line. In the model, the hairpin is represented by a parallel resonator. For the parallel resonator, the inductance,  $L_p$ , is mainly determined by the horizontal length of the hairpin, and the capacitance,  $C_p$ , is determined by the vertical spacing between lines of the hairpin. The remainder of



**Fig. 2.11** Reactance response of the hairpin bias line with a hairpin length of 2.1 mm. The series resonant frequency is 11.4 GHz and the parallel frequency is 10.9 GHz.

the line is represented by an inductor,  $L$ . The preliminary structure has a hairpin length of 3.1 mm and a line width of 0.1 mm. Based on the HP HFSS simulation results, the parallel resonant frequency of this structure is 7.2 GHz. By scaling the hairpin length, the resonant frequency can be shifted close to the design frequency. In fabrication, the hairpin length is 2.1 mm. The reactance response of the scaled structure is shown in Fig. 2.11. The parallel resonant frequency is shifted to 10.9 GHz. The solid line shows the result of the equivalent-circuit model with fitted parameters,  $L_p = 0.36$  nH,  $C_p = 0.6$  pF, and  $L = 3.8$  nH.

An advantage of the hairpin bias line is that a hairpin line can be made to have shorter length than a comparable meandering line. This reduction of bias-line length can reduce the conduction resistance of the bias network and reduce

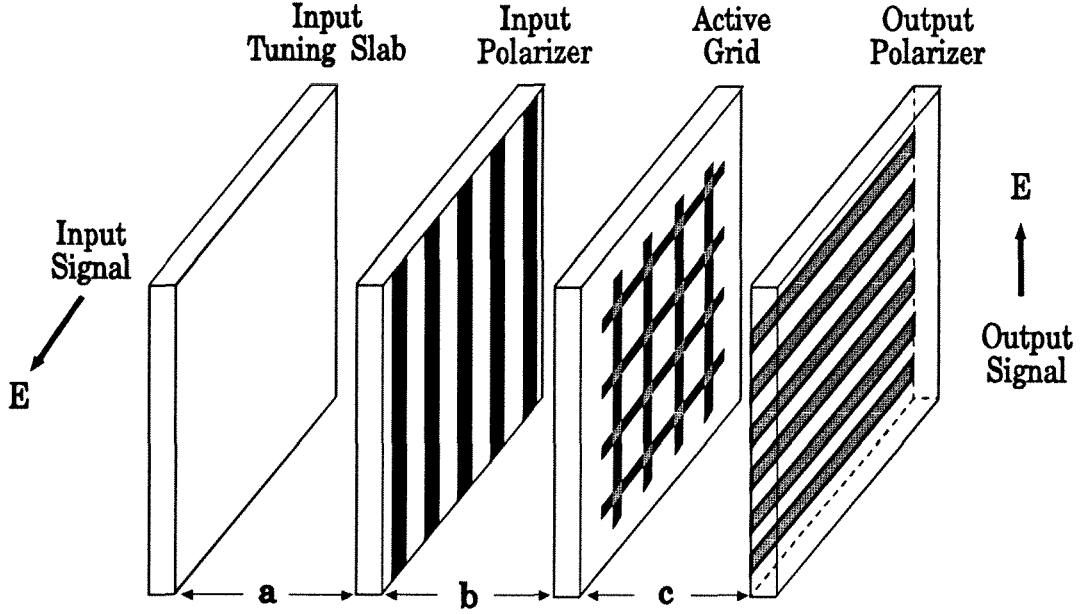


**Fig. 2.12** Far-field measurement setup for 10-GHz grids amplifiers. Instrumental control and data acquisition were performed by a computer.

DC dissipation of the grid. Less DC dissipation will result in higher efficiency of the grid, especially for monolithic grids as suggested in Sec. 6.2.2.

## 2.4 MEASUREMENTS

The gain was measured in the far-field [14]. Figure 2.12 shows the measurement setup. A similar setup is discussed in Chapter 5. An HP8350B sweeper was used as the RF source. The output power of the sweeper was monitored by an HP437B power meter through a 10-dB directional coupler. The receiver was an HP8592A spectrum analyzer. The transmitting and receiving antennas were AEL H-1498 horn antennas with 11 dB gain at 10 GHz. The complete measurement setup was controlled by a computer.

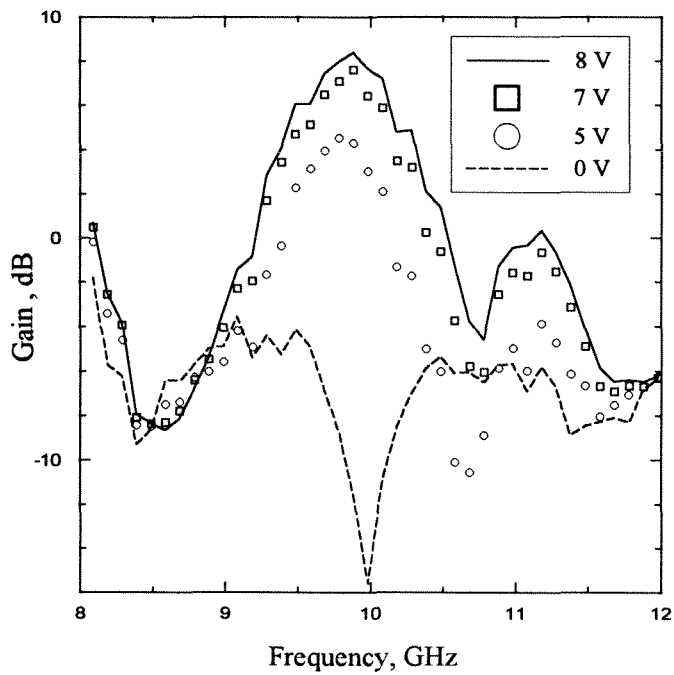


**Fig. 2.13** Assembled 10-GHz grid amplifier. The input tuning slab,  $\epsilon_r = 10.2$ , is employed to improve the input matching condition. The tuning procedure is to optimize the gain at 10 GHz by changing the air spacings,  $a$ ,  $b$ , and  $c$ .

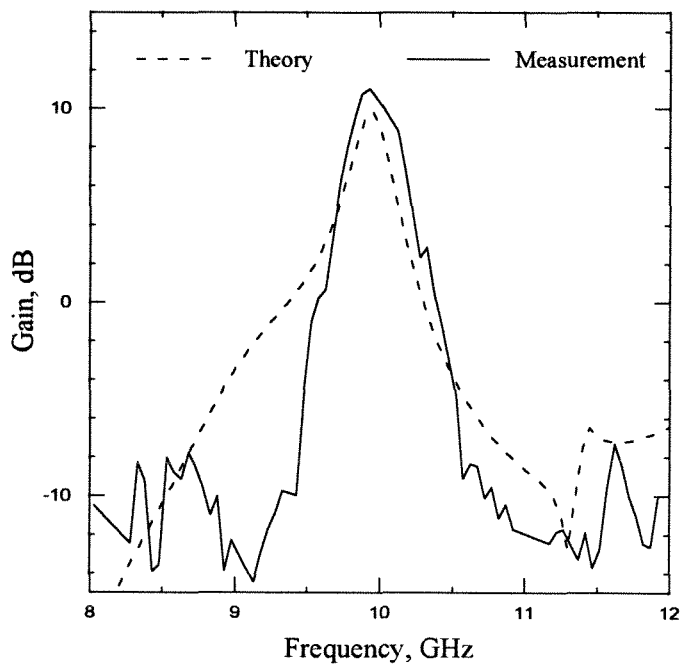
#### 2.4.1 GAIN MEASUREMENTS

Figure 2.13 shows the complete grid amplifier in the measurements. By changing the air spacings, the amplifier can be tuned to achieve the optimal gain at 10 GHz. An input tuning slab, with a relative dielectric constant of 10.2, was used to improve the input matching. The input and output polarizers were implemented by many 1 mm wide metal strips with spacings of 1 mm on a Duroid substrate with a relative dielectric constant of 2.2. Based on a method-of-moment simulation [22], at 10 GHz, the polarizer has an impedance of  $j2\ \Omega$  for signals with polarization parallel to the strips and an impedance of  $-j3000\ \Omega$  for signals with polarization orthogonal to the strips.

The first grid was fabricated without stabilizing capacitors and using HBT transistors with maximum stable gains of 16 dB at 10 GHz. Figure 2.14 shows



**Fig. 2.14** Gain response of the 10-GHz grid amplifier without stabilizing components. The peak gain is 8.5 dB at 9.9 GHz at a transistor current of 4 mA (8 V). The 3-dB bandwidth is 700 MHz (7%).



**Fig. 2.15** Gain response of the 10-GHz grid amplifier with 0.18-pF stabilizing capacitors. The peak gain is 11 dB at 9.9 GHz with a transistor current of 5 mA. The 3-dB bandwidth is 350 MHz (3.5%).

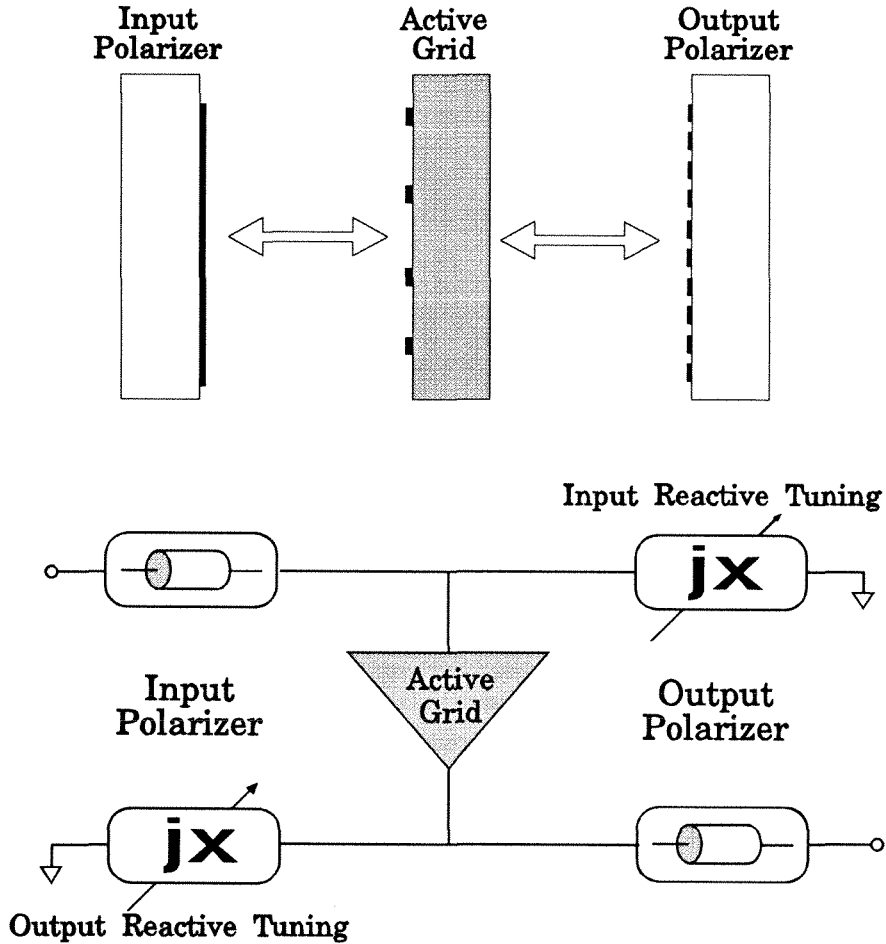
Layer	$\epsilon_r$	Dimension (mm)	Elec. Length ( $^\circ$ @10 GHz)
Substrate	10.8	1.27	50
Polarizer	2.2	3.18	57
Tuning Slab	10.2	2.54	97
Air Spacing $a$	1	4.8	58
Air Spacing $b$	1	19	228
Air Spacing $c$	1	26	312

**Table 2.1** Physical parameters of dielectric layers and air spacings for the measurement setup, as shown in Fig. 2.13.

the gain responses at four bias currents. At a transistor current of 4 mA, the grid has a peak gain of 8.5 dB at 9.9 GHz and a 3-dB bandwidth of 700 MHz (7%). The difference between the biased and zero-biased gains, i.e., the on-off ratio, is 23 dB at 10 GHz. When the bias current was increased above 4 mA, the grid started to oscillate at 7.8 GHz.

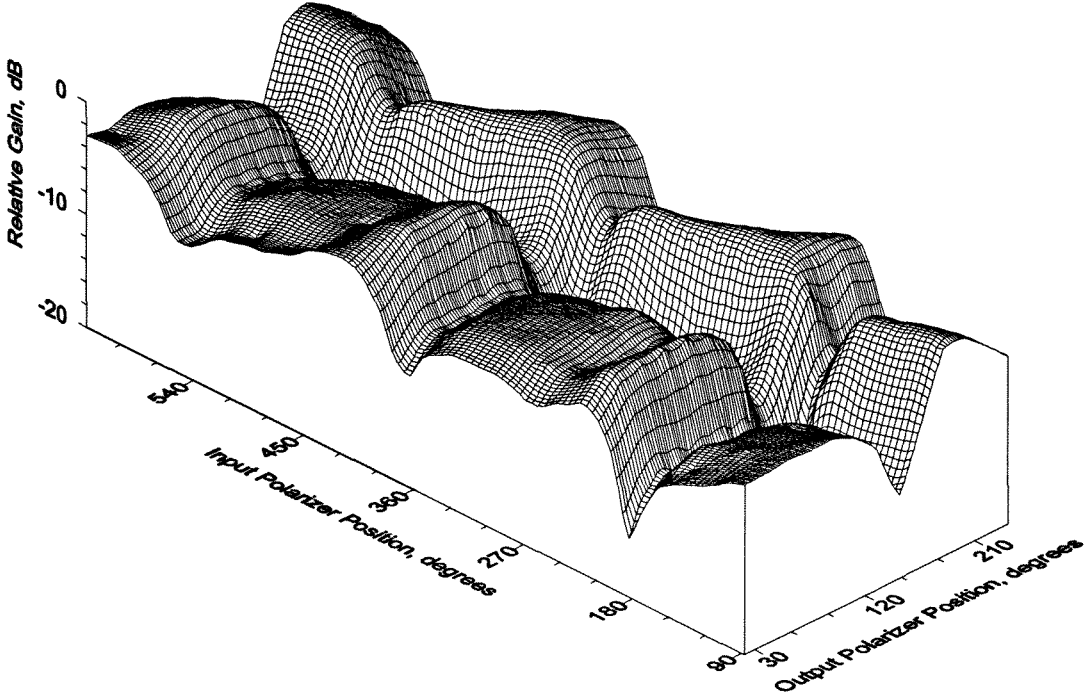
The second grid was fabricated with the 0.18-pF stabilizing capacitors. The HBT transistor used in this grid has a higher maximum available gain than the previous grid. Because of the higher inherent gain of the HBT transistor, without the stabilizing capacitors, the grid started oscillation at 7.8 GHz at a bias current of 2.4 mA per transistor. With the 0.18-pF stabilizing capacitors, the grid was stable as the bias current was less than 6 mA per transistor. A gain response was measured at a transistor current of 5 mA, as shown in Fig. 2.15. The maximum gain is 11 dB at 9.9 GHz and the 3-dB bandwidth is 350 MHz (3.5%). The 3-dB bandwidth is narrower than the previous grid (7%); however, due to the stabilizing capacitor, higher stability results in higher bias currents thus increasing the peak gain of the grid amplifier. A highly stable 10-GHz grid amplifier is discussed in Sec. 3.4.

Table 2.1 shows the relative dielectric constants and thicknesses of the Duroid dielectrics and the air spacings in the measurement. The theoretical gain plot,



**Fig. 2.16** Mechanically tuning the grid amplifier. The output of the active grid is mainly tuned by the input polarizer, and the input of the active grid is mainly tuned by the output polarizer.

derived from the transmission-line equivalent-circuit model, is also shown in Fig. 2.15 (dashed line). At an optimal current of 20 mA, the HBT transistor has a maximum available gain of 18 dB at 10 GHz. The theoretical gain is simulated exactly based on the scattering parameters measured at a transistor current of 5 mA. The peak gain difference of theory and the measurement is about 1 dB.



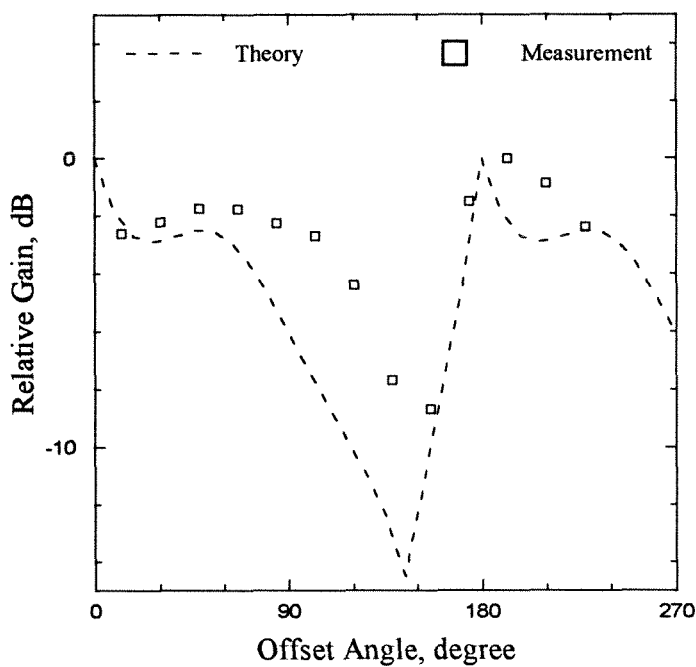
**Fig. 2.17** Measured tuning curve. Relative gain is measured versus input and output polarized positions.

#### 2.4.2 TUNING MEASUREMENTS

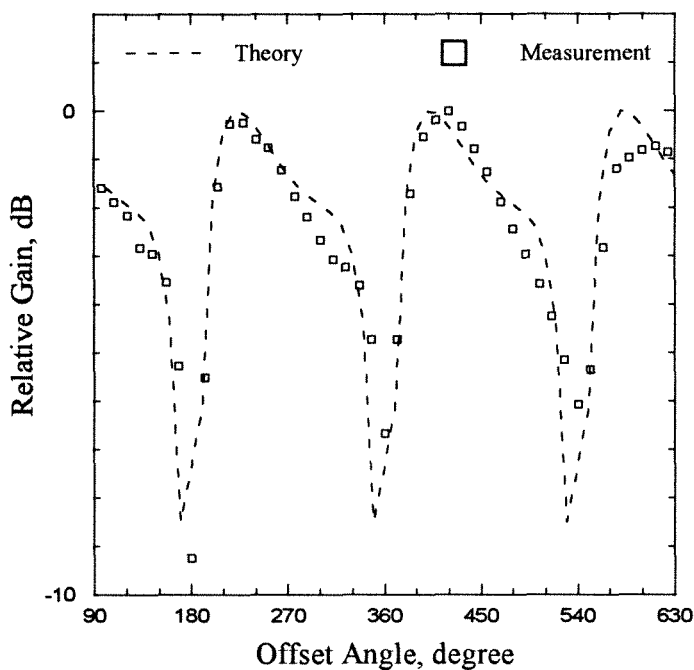
In the gain measurements, the gain was optimized by changing the positions of the input and output polarizers. Mechanical movements of the input and output polarizers are equivalent to electrical tuning on output and input of the active grid, respectively. Figure 2.16 shows this equivalent circuit, where the polarizers are assumed to be perfect—short and open circuits with respect to the two polarizations. Changing the input polarizer position reactively tunes the output of the active grid; and, changing the output polarizer position reactively tunes the input of the active grid.

In the tuning measurements, gains were measured at a fixed frequency by moving one polarizer and fixing the other polarizer. No tuning slabs were used. Figure 2.17 shows a two-dimensional tuning curve at 10 GHz versus input and output polarizer positions,  $\theta_i$  and  $\theta_o$ . The gain is repeated with periods of  $180^\circ$ .



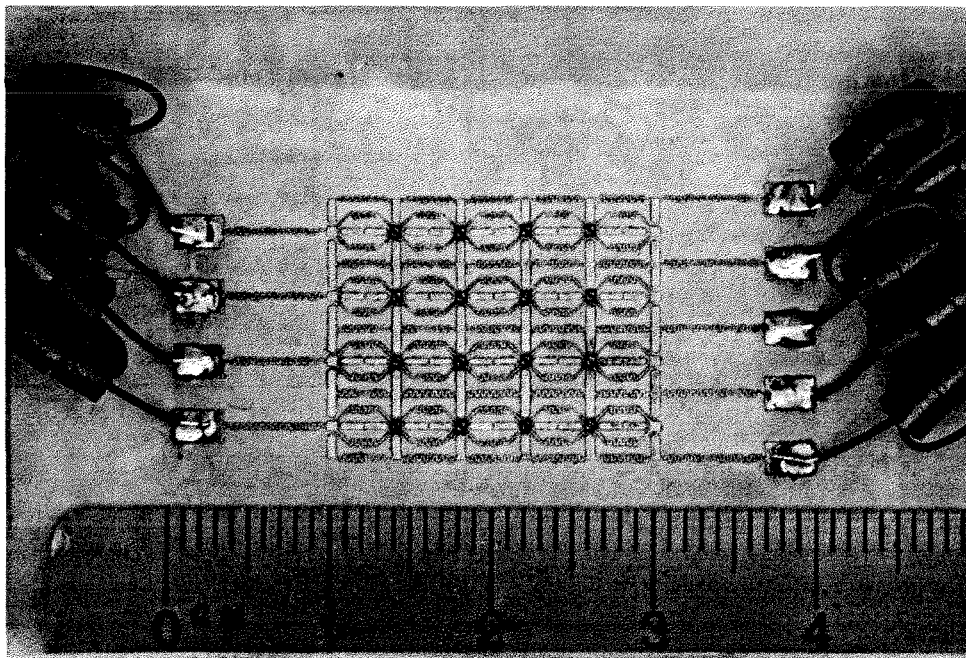


(a)



(b)

**Fig. 2.18** (a) Input tuning curve at 10 GHz. The input tuning curve is the relative gain obtained by moving the output polarizer and fixing the input polarizer. (b) Output tuning curve at 10 GHz. The output tuning curve is the relative gain obtained by moving the input polarizer and fixing the output polarizer.



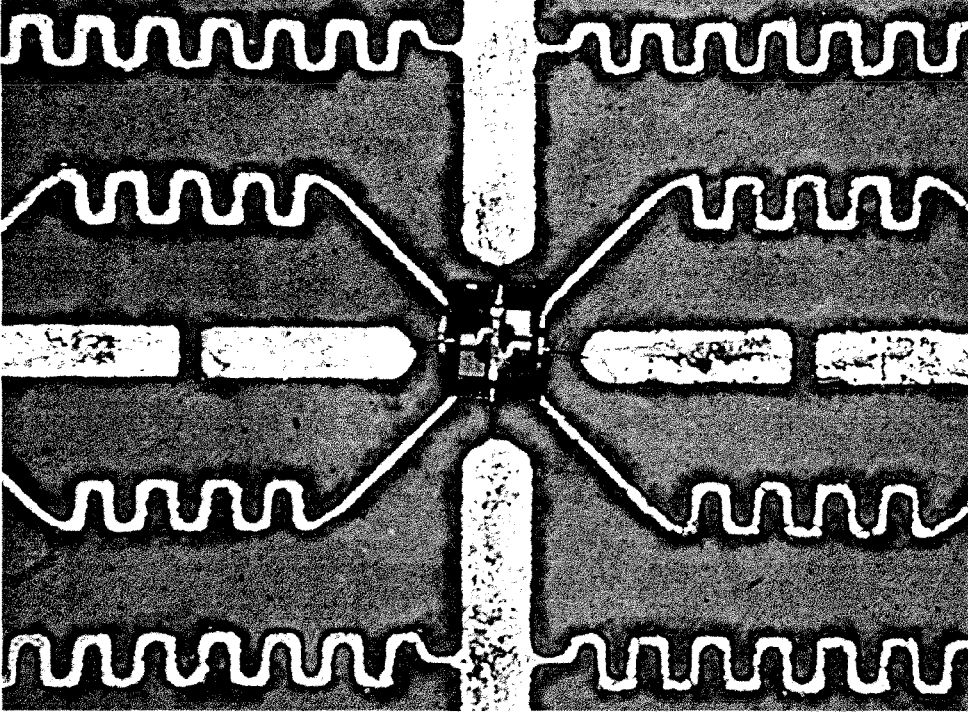
**Fig. 2.19** Photo of the 16-element 16-GHz active grid. The substrate is a 50-mil Duroid with a relative dielectric constant of 10.8.

The peak gain occurs at  $\theta_i = 424^\circ$  and  $\theta_o = 192^\circ$ . For further comparisons, two cuts on the peak gain are plotted in Fig. 2.18(a,b). In these two plots, measurements show reasonable agreement with the theory.

Polarizer positions determine the reactive matching conditions of the grid amplifiers. To accomplish resistive tuning, tuning slabs with suitable thickness and dielectric constant can be used at the input and/or output ends. Tuning ability gives more flexibility in compensating the mismatch between modelling and fabrication.

## 2.5 A 16-GHz HYBRID GRID AMPLIFIER

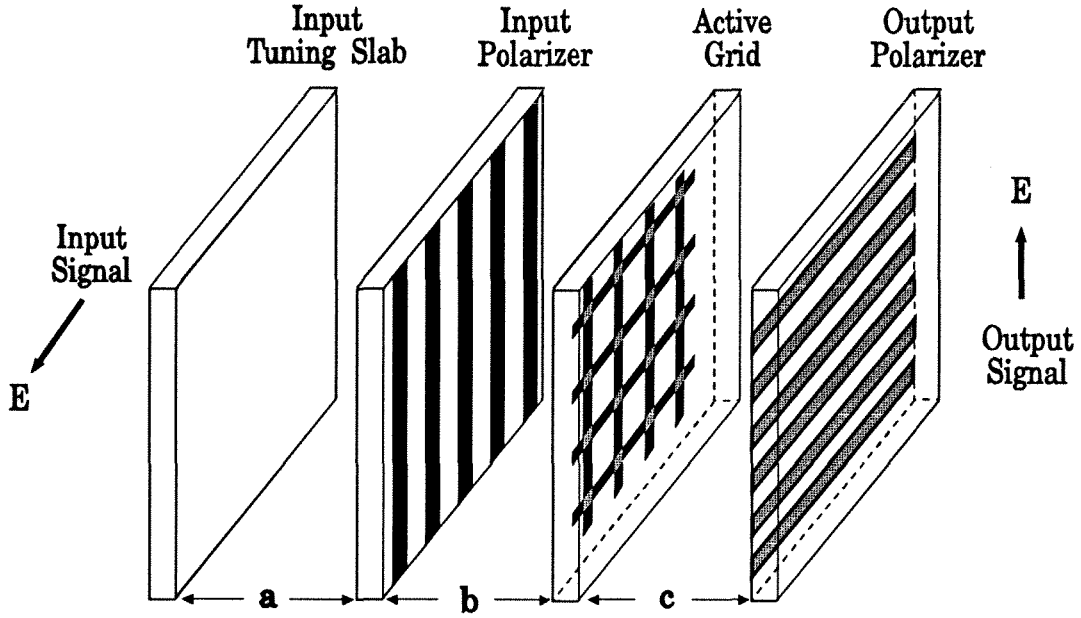
A 16-element hybrid HBT grid amplifier was designed and fabricated on a 50-mil Duroid substrate with a relative dielectric constant of 10.8, as shown in Fig. 2.19. This grid used the same HBT differential-pair chips as the 10-GHz



**Fig. 2.20** Photo of a unit cell of the 16-GHz active grid. The unit cell is 4 mm on a side. Input leads are 0.4 mm wide and output leads are 0.5 mm wide. Input matching gap is 0.2 mm.

grids. The photo of the unit cell is shown in Fig. 2.20. The unit-cell dimensions are 4 mm on a side, half of the 10-GHz grid's cell. The input lead is 0.4 mm wide and the output lead is 0.5 mm. Based on the method-of-moment simulation [22], the impedances of the input and output leads are  $j82\Omega$  and  $j73\Omega$  at 16 GHz. The input matching gap capacitor is 83 fF. Transistors are biased by the meandering bias lines.

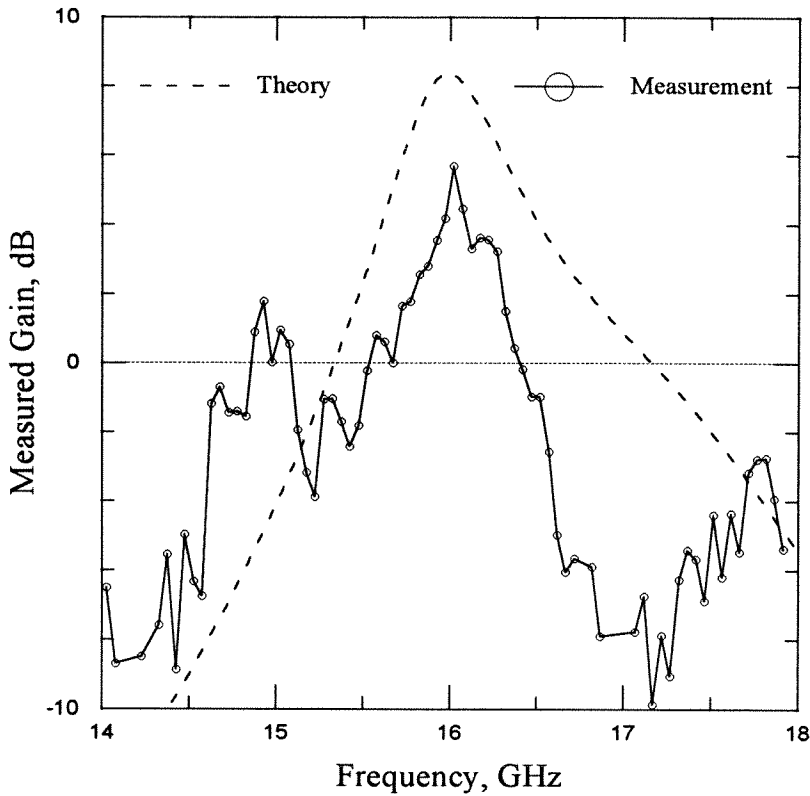
Figure 2.21 shows the assembled 16-GHz grid amplifier including the active grid, input and output polarizers, and an input tuning slab. Table 2.2 shows the physical parameters of the grid amplifier. The gain was measured in the far field with a setup similar to the 10-GHz gain measurement. Figure 2.22 shows the gain response of the 16-GHz grid at a bias current of 4.5 mA per transistor. The grid



**Fig. 2.21** Assembled 16-GHz grid amplifier. The input tuning slab,  $\epsilon_r = 2.2$ , is to improve the input matching condition. Tuning procedure is to optimize the gain at 16 GHz by changing the air spacings,  $a$ ,  $b$ , and  $c$ .

Layer	$\epsilon_r$	Dimension (mm)	Elec. Length ( $^\circ$ @16 GHz)
Substrate	10.8	1.27	80
Polarizer	2.2	3.18	90
Tuning Slab	2.2	3.18	90
Air Spacing $a$	1	17	326
Air Spacing $b$	1	14.5	278
Air Spacing $c$	1	10.5	202

**Table 2.2** Physical parameters of dielectric layers and air spacings for the 16 GHz measurement setup, as shown in Fig. 2.21.



**Fig. 2.22** Gain response of the 16-GHz grid amplifier. The peak gain is 5.7 dB at 16 GHz with a transistor current of 4.5 mA. The 3-dB bandwidth is 500 MHz(3.1%).

has a peak gain of 5.7 dB at 16 GHz and a 3-dB bandwidth of 500 MHz (3.1%). The theoretical gain, derived from the transmission-line equivalent-circuit model as in Sec. 2.4, is also plotted in Fig. 2.22. The grid has no stabilizing components and suffered from spurious oscillations around 15 GHz when biased at a transistor current of more than 5 mA.

The on-off ratio is about 7 dB. The poor on-off ratio may be caused by scattering from the bias wires and the plastic frame holding the grid. Another difficulty encountered in the measurement was the weakness of the signal due to the small area of the grid. Noise will become significant if the grid area is not roughly equal to the area of the antenna horn as described in [25].

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## Chapter 3

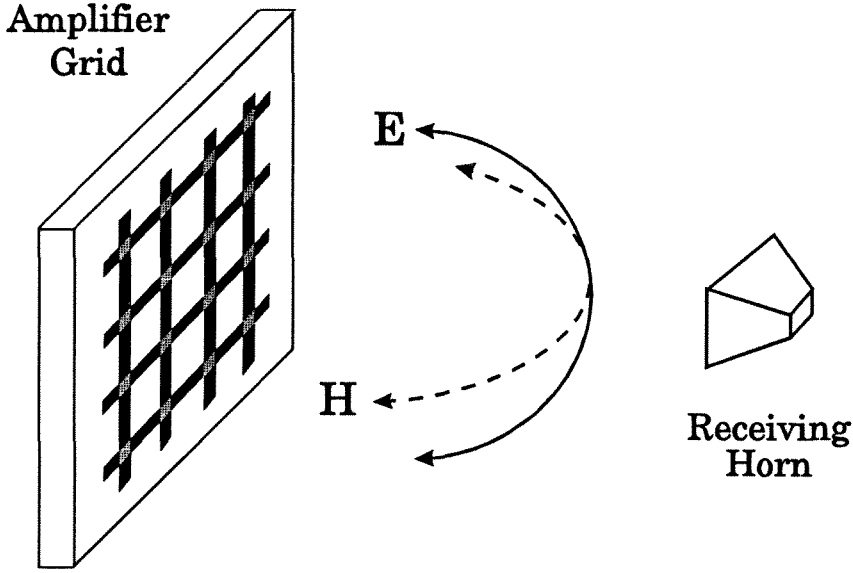
# Grid-Amplifier Stability Model

In this chapter, grid-amplifier stability and stabilizing techniques are discussed. Without stabilizing components, spurious oscillations were observed in the development of hybrid grid amplifiers[1,2]. The oscillation frequencies were in the range from 7 to 9 GHz. These instabilities limited the grid amplifiers to operating at low bias currents thereby limiting gain and power performances. Hence, stability is another important issue in the design. Based on the investigation of the spurious oscillations, a stability model is presented. Two stabilizing approaches (resistive and reactive) are discussed. A highly stable grid amplifier, with stabilizing capacitors, is also demonstrated [3].

### 3.1 ORIGIN—COMMON-MODE OSCILLATION

In the development of the X-band grid amplifiers, without the stabilizing capacitor, the grid oscillated at 7.8 GHz as the bias current was increased to 3 mA per transistor. This bias current is much lower than the optimal bias current, 20 mA per transistor. The peak gain of the grid amplifier was less than 4 dB at this low bias current.

To analyze the spurious oscillation, we tried some perturbations on the grid amplifier. When we changed the polarizer positions or added extra dielectric layers to the substrate, the oscillations did not have significant variations in magnitude and frequency. However, when we shorted out the input matching gap capacitors with bond wires, the oscillation frequency shifted to 4.8 GHz. A

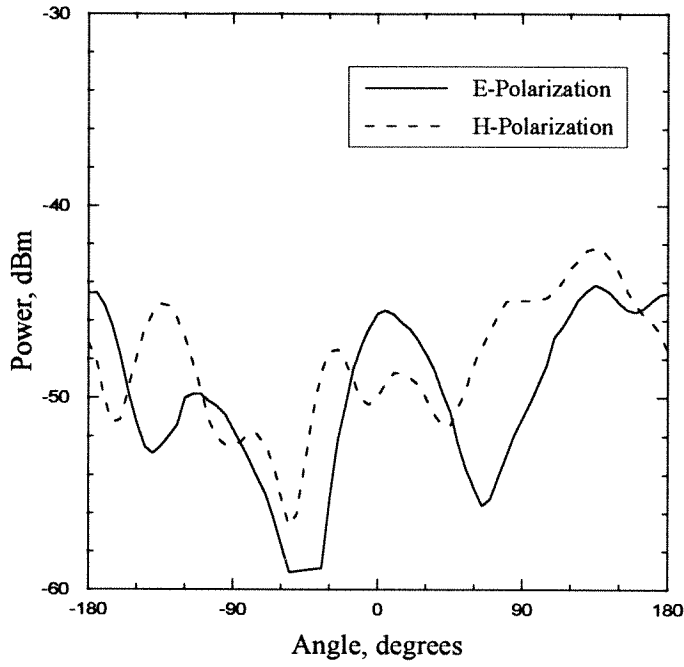


**Fig. 3.1.** Oscillation-pattern measurement setup. E-plane is parallel to the output leads of the grid.

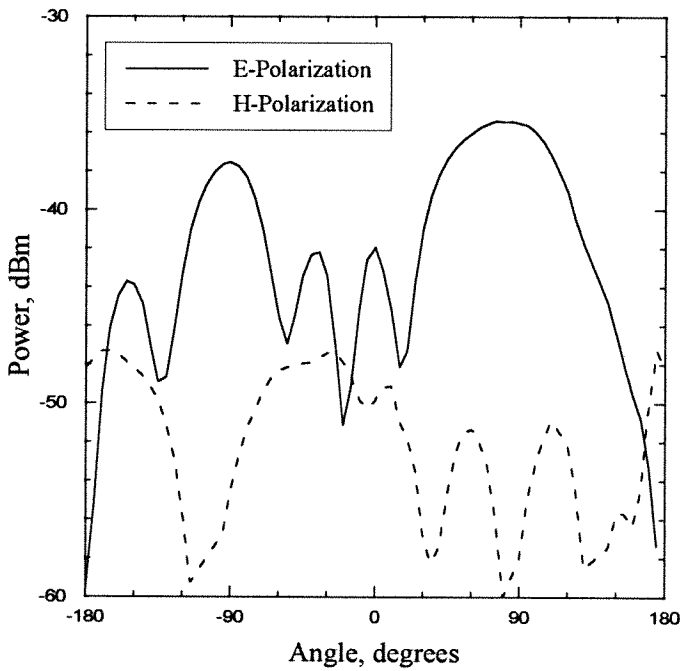
frequency shift was also observed by changing the lengths of the bond wires. These phenomena showed that the oscillations were sensitive to the transverse components on the unit cell, but not sensitive to the longitudinal components, the substrate and polarizers.

Further analysis has been performed by measuring far-field radiation patterns of the spurious oscillation. The oscillation patterns were measured in both E plane and H plane, as shown in Fig 3.1. The oscillation patterns of two polarizations in H plane and E plane are shown in Fig. 3.2.(a) and Fig. 3.2.(b). The patterns show that the oscillation has two peaks of power density at the bias ends with E polarization. A further measurement was the azimuth pattern in the plane of the grid, as shown in Fig. 3.3.(a). The measured azimuth pattern is shown in Fig. 3.3.(b). The greatest power density is exactly from the emitter-bias end.

This significant peak characterizes the oscillation as a common-mode source

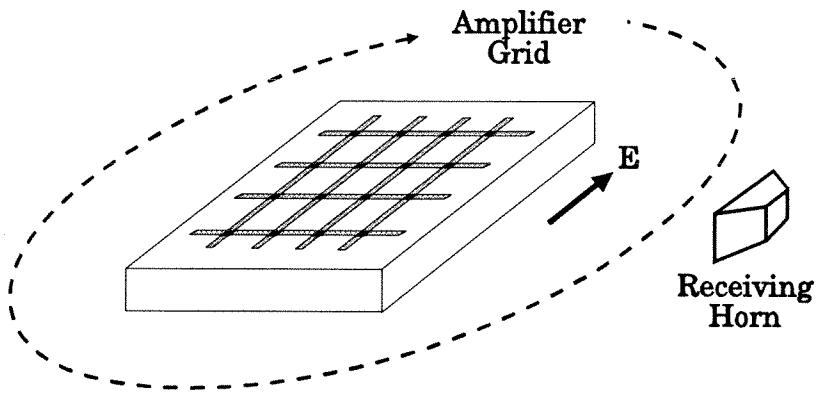


(a)

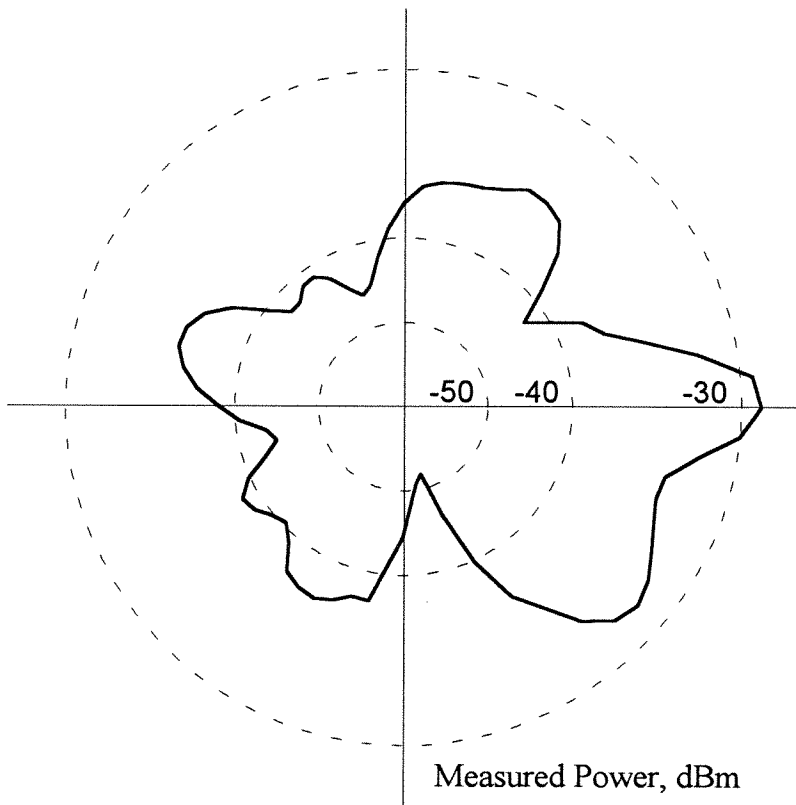


(b)

**Fig. 3.2.** (a) E-plane oscillation patterns for both polarizations. (b) H-plane patterns. The peak power density occurs at  $90^\circ$ , emitter-bias end, with E-plane polarization.



(a)



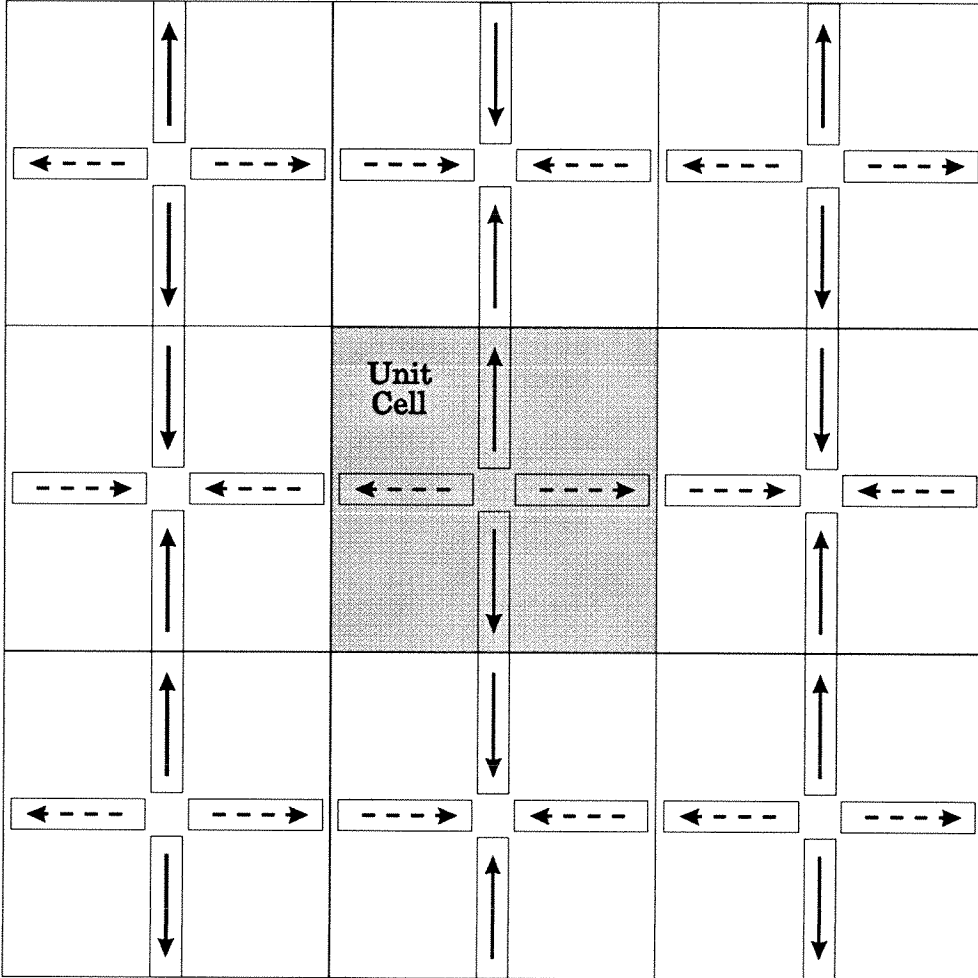
(b)

**Fig. 3.3.** (a) Azimuth pattern measurement. (b) Azimuth oscillation pattern measured in the plane of the grid with polarization parallel to the grid. The peak power density came from the emitter-bias end.

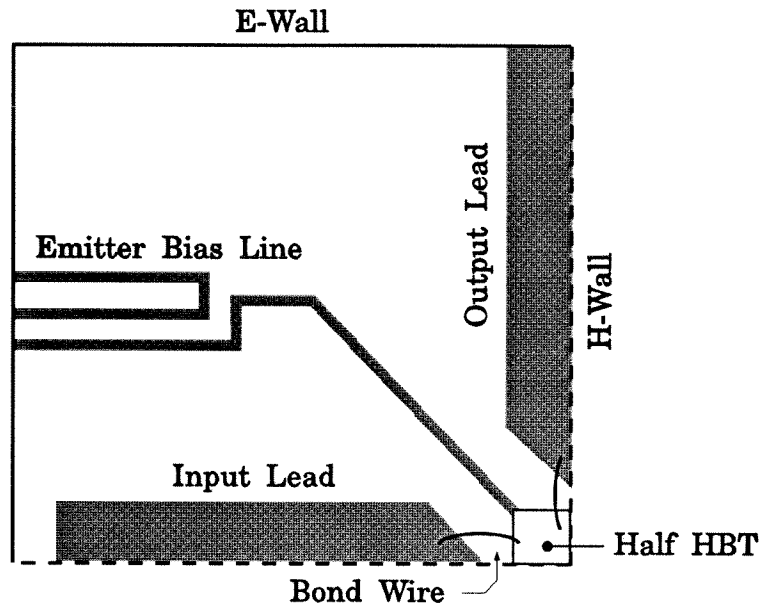
excited by vertically distributed currents, the collector currents. The current distribution of the common-mode oscillation is shown in Fig. 3.4. The RF power is excited by the common-mode currents, coupled to and propagated in the substrate, and radiated to the free space at the end of the substrate.

### 3.2 STABILITY MODEL

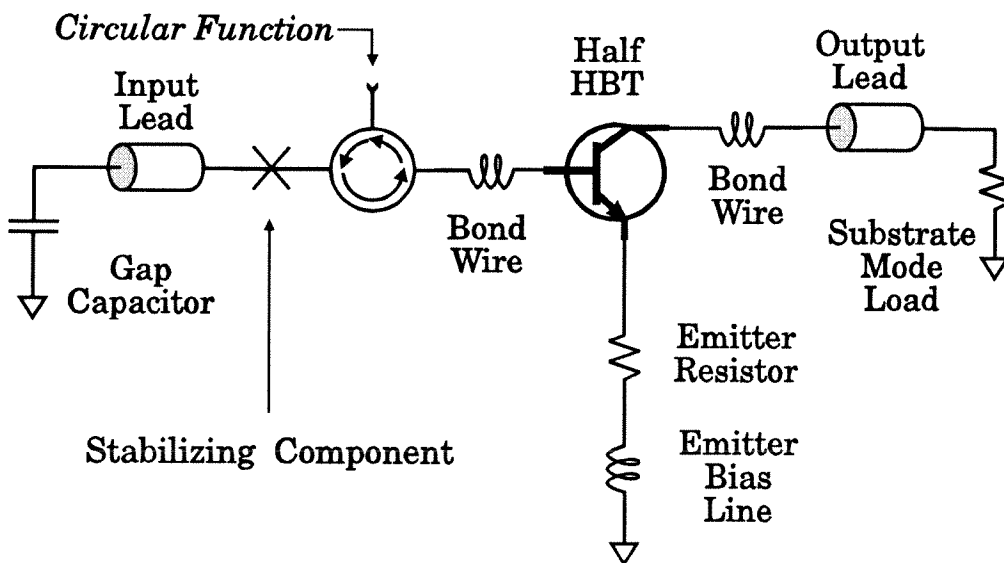
Due to the common-mode operation of the transistor pair, we can use the quarter cell, as shown in Fig. 3.5.(a), to analyze the stability of a grid ampli-



**Fig. 3.4.** Stimulus-current direction for the common-mode oscillation. Anti-symmetry of currents result in an E-wall boundary condition for the unit cell.



(a)



(b)

**Fig. 3.5.** (a) A quarter cell. Boundary conditions are imposed by symmetry. (b) Equivalent-circuit model for the quarter cell. The circular function is the reflection coefficient of the circulator port.

fier. For the quarter cell, boundary conditions are imposed by symmetry. Figure 3.5.(b) shows the equivalent-circuit model for the quarter cell. Because we analyze the circuit in the transverse direction, the input and output leads are represented by transmission lines, rather than inductors in the gain model. Bond wires are represented by inductors with values [4]:

$$L = 4 \times 10^{-4} l \left[ \ln \frac{4l}{d} + 0.5 \frac{d}{l} - 0.75 \right]. \quad (3.1)$$

The emitter bias line is represented by an inductor. The substrate-mode resistor is for the power delivered into the substrate and is assumed zero in the analysis. The active device is half of the transistor because we analyze a quarter of the unit cell. The scattering parameters of half an HBT transistor can be derived from half the admittance parameters. The transformations are [5]:

$$Y_{11} = \frac{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}}, \quad (3.2.a)$$

$$Y_{12} = \frac{-2S_{12}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}}, \quad (3.2.b)$$

$$Y_{21} = \frac{-2S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}}, \quad (3.2.c)$$

$$Y_{22} = \frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}}, \quad (3.2.d)$$

where  $Y_{ij}$  and  $S_{ij}$  are the admittance and scattering parameters of an individual HBT transistor. Then, the scattering parameters of half an HBT transistor,  $S'_{ij}$ , can be derived as:

$$S'_{11} = \frac{(2 - Y_{11})(2 + Y_{22}) + Y_{12}Y_{21}}{(2 + Y_{11})(2 + Y_{22}) - Y_{12}Y_{21}}, \quad (3.3.a)$$

$$S'_{12} = \frac{-4Y_{12}}{(2 + Y_{11})(2 + Y_{22}) - Y_{12}Y_{21}}, \quad (3.3.b)$$

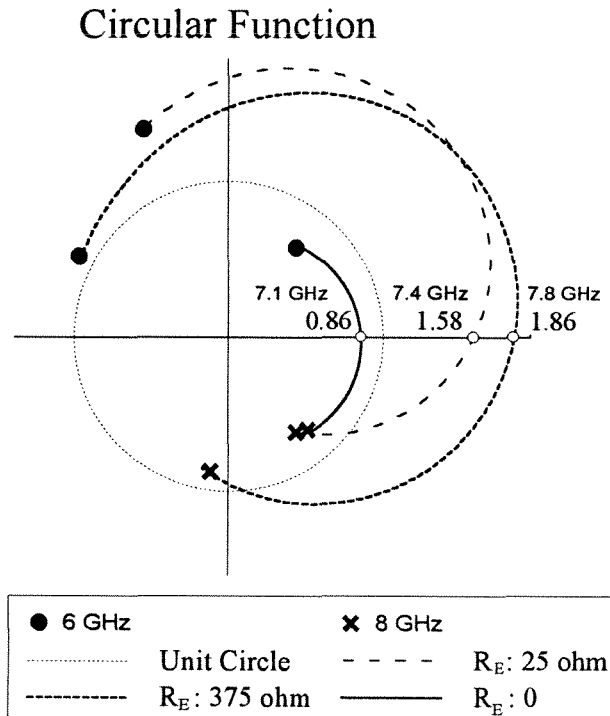
$$S'_{21} = \frac{-4Y_{21}}{(2 + Y_{11})(2 + Y_{22}) - Y_{12}Y_{21}}, \quad (3.3.c)$$

$$S'_{22} = \frac{(2 + Y_{11})(2 - Y_{22}) + Y_{12}Y_{21}}{(2 + Y_{11})(2 + Y_{22}) - Y_{12}Y_{21}}. \quad (3.3.d)$$

A circulator is inserted at the base end and the reflection coefficient of the circulator port, circular function, is used to analyze the stability[6]. Based on Martinez-Compton theory, for small signal analysis, the circuit has the potential to oscillate at the frequency where the phase of the circular function is zero and the magnitude of the circular function exceeds unity. The circular function can be thought of as a measure of the open-loop gain of the circuit. The zero-phase magnitude of the circular function is the criterion of circuit stability.

### 3.3 STABILIZING THE GRID AMPLIFIERS

To stabilize the grid, the circular function needs to move to a locus with a zero-phase magnitude less than unity by adding stabilizing components to the grid. There are two approaches to stabilize the grid—resistive and reactive. These two approaches have orthogonal effects on the phase and magnitude of the

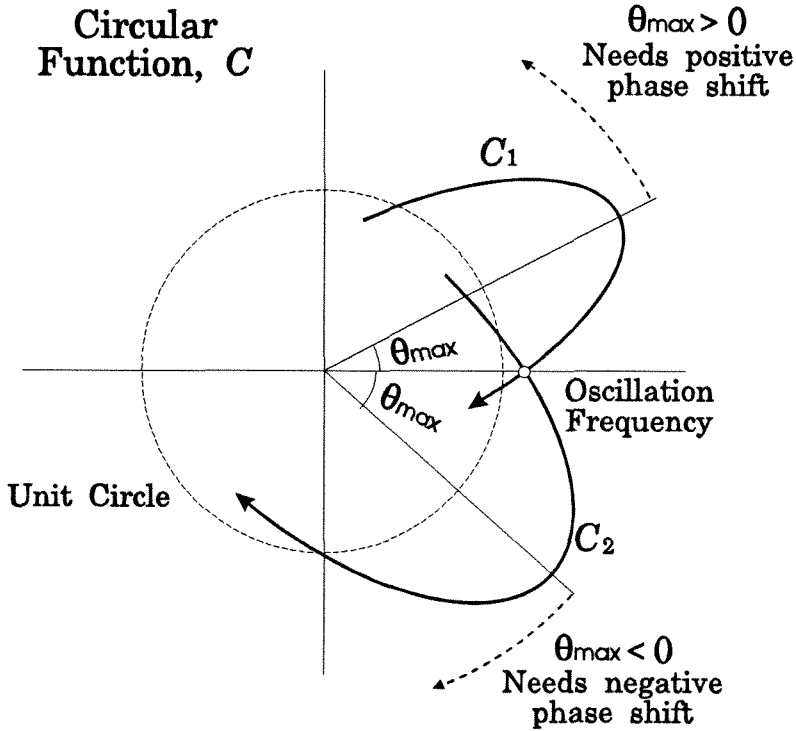


**Fig. 3.6.** Circular functions with and without emitter resistors,  $R_E$ 's. The grid with smaller emitter resistors should have higher stability.



circular function.

Resistive approaches employ resistors as stabilizing components to reduce the magnitude of the circular function. A successful result has been achieved by Michael De Lisio at Caltech [2]. Stabilizing resistors, 50- $\Omega$  chip resistors, were placed in the radiating gate leads to suppress the oscillations. Nevertheless, this approach reduces the magnitude of the circular function at the expense of lowering peak gain and increasing the noise figure of the grid. Another resistive approach is to reduce the emitter (source) resistors of the differential transistor pair. Figure 3.6 shows the circular functions with and without the 375- $\Omega$  emitter resistors. Simulations show that lower emitter resistors result in higher stability.



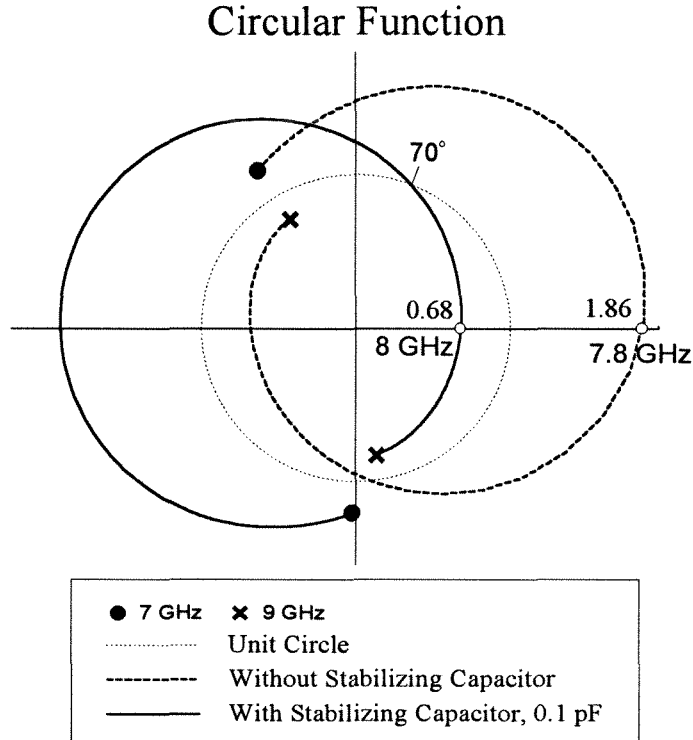
**Fig. 3.7.** Analysis of circular functions. With  $\theta_{max} > 0$ , a positive phase shift is required to reduce the zero-phase magnitude—a capacitor is the stabilizing component. With  $\theta_{max} < 0$ , a negative phase shift is required to reduce the zero-phase magnitude—an inductor is the stabilizing component.

Reducing the emitter resistors can also improve the efficiency of the grid amplifier. This approach has been experimentally demonstrated by Alina Moussessian at Caltech.

Reactive approaches are to exploit reactive components, capacitors or inductors. Reactive stabilizing components can contribute a proper phase shift to the circular function thus reducing the zero-phase magnitude. The selection of capacitors or inductors to serve as stabilizing components is determined by the phase of the maximum magnitude of the circular function,  $\theta_{max}$ , as shown in Fig. 3.7. When  $\theta_{max}$  is positive, capacitors are the stabilizing components [3,7]. The stabilizing capacitors offer a positive phase shift to the circular function and reduce the zero-phase magnitude. On the other hand, if the circular function has negative  $\theta_{max}$ , a negative phase shift is necessary to stabilize the circuit. Therefore, inductors are the stabilizing components. These reactive stabilizing components should not affect the peak gain of the grid amplifier. However, they will increase the quality factor of the grid thus increasing the tuning difficulties and reducing the gain bandwidth.

Figure 3.8 shows the circular functions of the X-band hybrid HBT grid amplifier (Chapter 2). In the stability simulations, the impedances of the transmission lines were chosen to give an oscillation frequency identical to the observed oscillation frequency. In simulations, the transmission lines for the input and output lead are  $106\ \Omega$  with  $104^\circ$  electrical length at 10 GHz. Without any stabilizing component, the circular function has a zero-phase magnitude of 5.4 dB at 7.8 GHz. A potential spurious oscillation is predicted at 7.8 GHz. For the circular function, the maximum-magnitude phase,  $\theta_{max}$ , is  $26^\circ$  at 7.75 GHz. Therefore, capacitors, offering positive phase shift, are used as stabilizing components to improve the stability of the amplifier grid.

Stabilizing capacitors of 0.1 pF are added at the base ends of the HBT's. In the stability model, a 50-fF capacitor is located at the node marked with



**Fig. 3.8.** Circular functions with and without stabilizing capacitors,  $C_s$ 's. The stabilizing capacitors offer a positive phase shift of  $153^\circ$  to the circular function and stabilizing the grid.

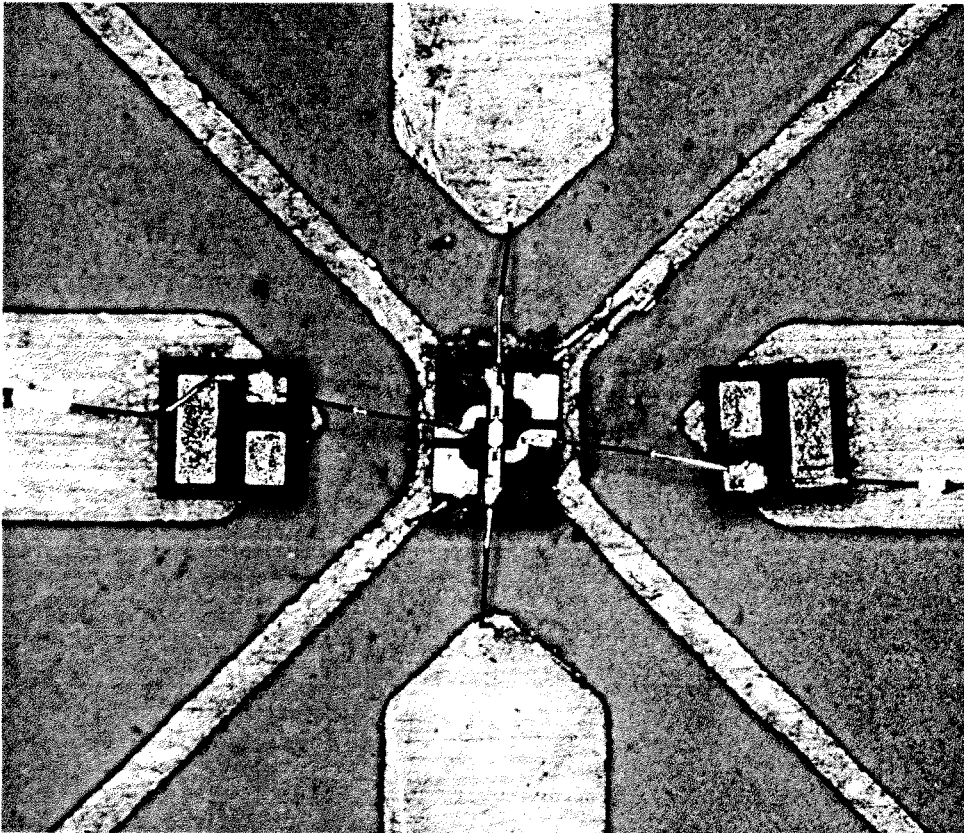
an  $\times$ , as shown in Fig. 3.5(b). The circular function with the 0.1-pF stabilizing capacitor is also shown in Fig. 3.8. This stabilizing capacitor offers a  $153^\circ$  phase shift to the circular function and reduce the zero-phase magnitude to 0.68. The circuit is stable with a phase margin of  $70^\circ$  and a gain margin of 3.4 dB. Based on the analysis, more gain and phase margin can be achieved by using smaller stabilizing capacitors.

In the stability analysis, the gain and phase margins are relative estimates of stability for the specified circuit. A different location of the circulator will result in a different circular function and margin. Figure 3.5(b) is a convenient circuit for stability analysis because it has only reactive components on the left of the circulator. This makes an obvious observation on the phase shift contributed by reactive stabilizing components.

### 3.4 MEASUREMENTS

We used chip capacitors with binary values to investigate the stability of the amplifier grid, as shown in Fig. 3.9. The capacitances of 0.18, 0.36, and 0.7 pF were chosen by bonding the wires on the capacitors. The result is that the grid amplifier with smaller stabilizing capacitance has higher stability. This is consistent with the stability analysis—the smaller capacitance gives more positive phase shift and higher margins.

To further test the stability model, another grid was fabricated with the stabilizing capacitors of 0.1 pF. The 0.1-pF stabilizing capacitors successfully stabilized the amplifier grid without any spurious oscillation. Table 3.1 shows a

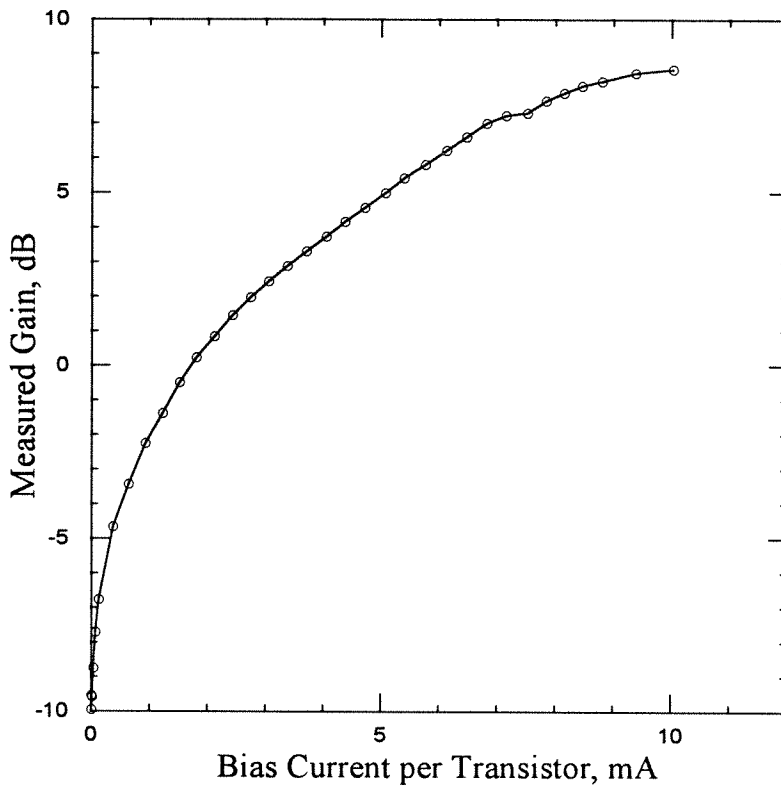


**Fig. 3.9.** Close-up of the unit-cell center. The capacitance of the binary-valued chip capacitor is determined by the bond wire.

Stabilizing Cap. (pF)	Phase Shift (°)	Gain Margin (dB)	Onset Current (mA)
None	0	-5.4	2.4
0.7	33	-3.9	3
0.36	66	-1.5	4
0.18	114	1.9	6
0.1	153	3.4	> 10

Table 3.1 Comparison of phase shifts, gain margins, and onset oscillation currents for the amplifier grid without and with stabilizing capacitors.

comparison of the phase shifts, gain margins, and onset oscillation currents for the grid without and with stabilizing capacitors. The plot of gain versus bias current is shown in Fig. 3.10. No oscillation was observed in the measurement. When biased above 10 mA, the grid became hot and may cause some thermal damage. In the measurement, the maximum gain is 8.5 dB at the bias current of 10 mA per transistor. This bias current is twice as high as the bias current of the previous grid. The stabilizing capacitors reduced the gain by 2.5 dB. However, the higher bias current should give the grid higher maximum output power.



**Fig. 3.10.** Gain versus bias current at 10 GHz. The grid amplifier, with 0.1-pF stabilizing capacitors, has a peak gain of 8.5 dB at a transistor current of 10 mA.

## References

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## Chapter 4

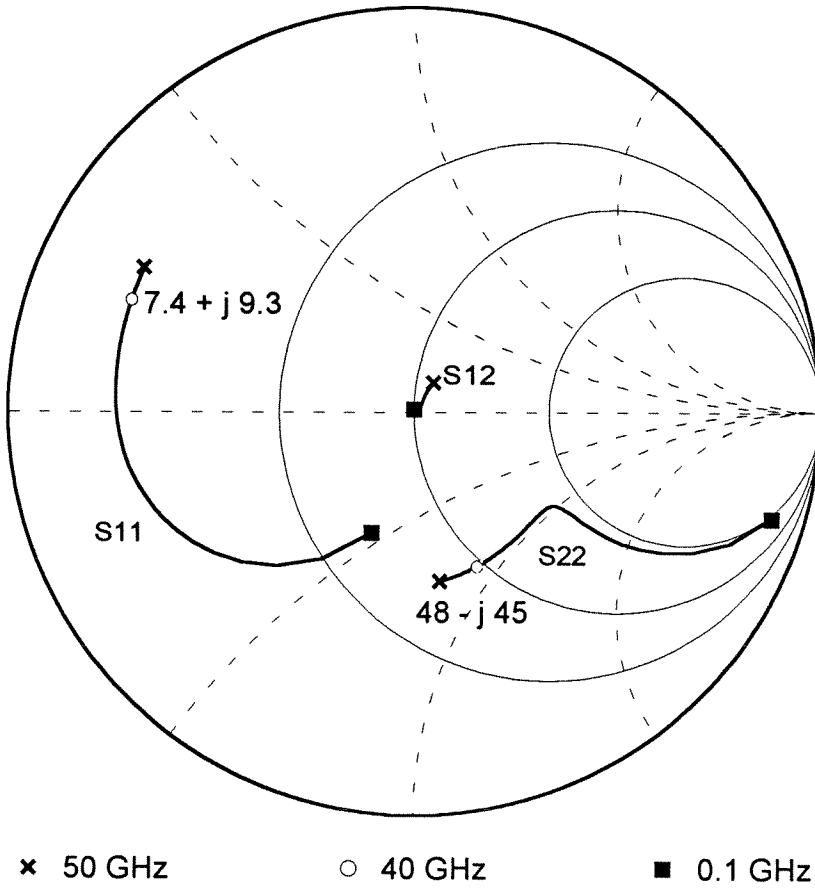
# Monolithic 40-GHz HBT Grid Amplifier

This chapter discusses a 36-element monolithic HBT grid amplifier. The monolithic amplifier grid was fabricated with the HBT process established at Rockwell Science Center. The monolithic grid, with base stabilizing capacitors, is highly stable. The peak gain is 5 dB at 40 GHz and the 3-dB bandwidth is 1.8 GHz (4.5%). The maximum output power is 670 mW at 40 GHz with a gain of 2.5 dB. The power-added efficiency is 4% for the whole grid, and is 13.5% for the HBT transistor without counting the DC dissipation in the bias network. This is the first monolithic quasi-optical amplifier with power measurement report. Tiling technology is also discussed in this chapter.

### 4.1 INTRODUCTION

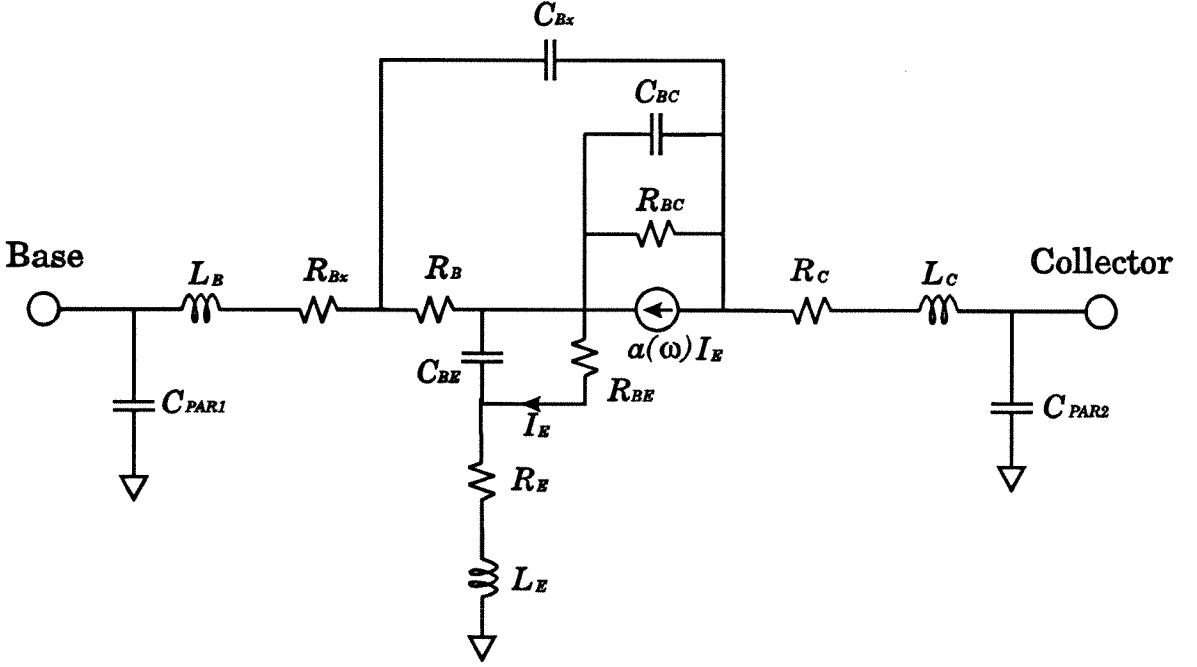
Several quasi-optical amplifiers have been demonstrated, as described in Chapter 1. John Hubert *et al.* demonstrated a quasi-optical millimeter-wave amplifier using slot antennas, with a flange-to-flange gain of 6 dB at 29 GHz [1]. However, these quasi-optical amplifiers were fabricated by hybrid technology. Recently, Emilio Sovero and Aiden Higgins have reported two monolithic quasi-optical plane-wave amplifiers, using HBT's [2] and pHEMT's [3]. The pHEMT plane-wave amplifier, using slot and/or patch antennas, has a peak gain of 3 dB with a 3-dB bandwidth of 6%. Using monolithic technology, grid components have been demonstrated, including multipliers [4–6], phase shifters [7], beam steerers [8], and oscillators [9]. The grid-amplifier structure can be com-





**Fig. 4.1.** Scattering parameters for the HBT transistor with common-emitter configuration. The unilateral input impedance is  $7.4 + j9.3 \Omega$  at 40 GHz.

pletely planar with all the devices on one side, making this approach attractive to monolithic fabrication. Very recently, Michael De Lisio has demonstrated a successful monolithic pHEMT grid amplifier with peak gains of 6.5 dB at 44 GHz and 2.5 dB at 60 GHz [10]. This chapter will discuss the monolithic approach for the HBT grid amplifier. The first reports of gain and power measurements for a successful monolithic quasi-optical amplifier are demonstrated in this chapter [11–13]. Moreover, an attempt to provide higher output power, tiling technology, is also discussed.



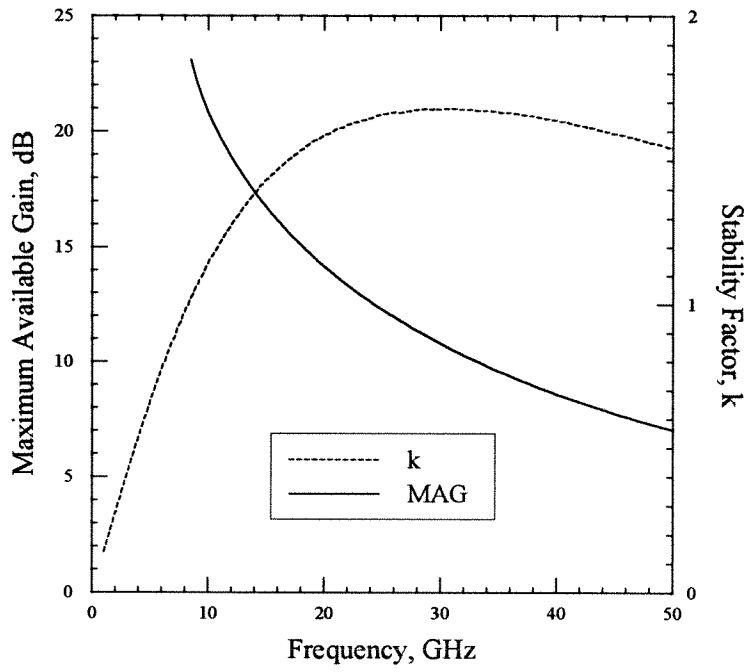
**Fig. 4.2.** Small-signal equivalent circuit for the HBT with common-emitter configuration.

## 4.2 DESIGN

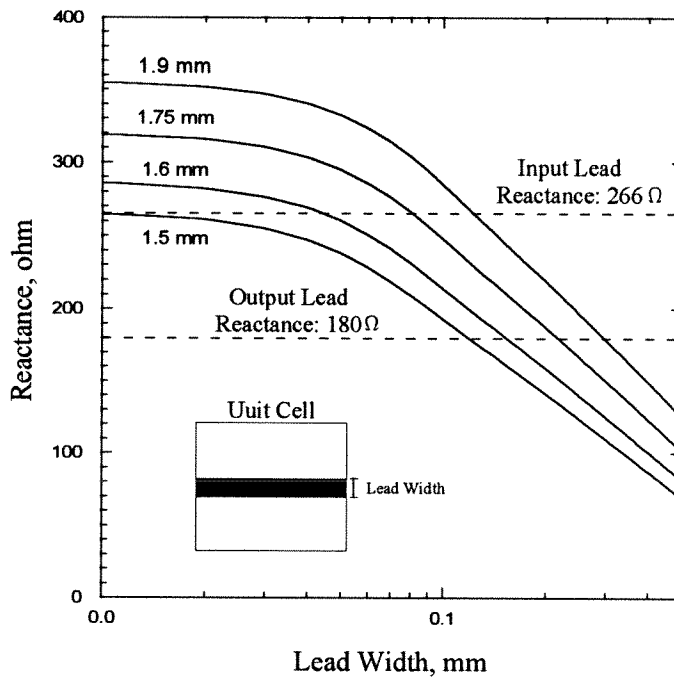
The active device used in the monolithic amplifier grid is an HBT transistor. The HBT under optimum bias current (20 mA per transistor) has a maximum oscillation frequency,  $f_{max}$ , of 100 GHz and a unity-current-gain frequency,  $f_t$ , of 60 GHz. Figure 4.1 shows the measured scattering parameters of an individual HBT transistor with common-emitter configuration. The measured frequency was swept from 0.1 GHz to 40 GHz. A small-signal model, derived by Dr. Sovero from fitted parameters as shown in Fig. 4.2, was utilized to extrapolate the scattering parameters up to 50 GHz. The stability factor,  $k$ , and the maximum available gain are shown in Fig. 4.3. At 40 GHz, the HBT transistor is inherently stable and has a maximum available gain of 9 dB.

### 4.2.1 UNIT CELL

In the preliminary simulation, the optimal lead reactances are  $j266 \Omega$  for



**Fig. 4.3.** Maximum available gain (MAG), and stability factor ( $k$ ).



**Fig. 4.4.** Lead reactance versus lead width for four unit-cell periods.

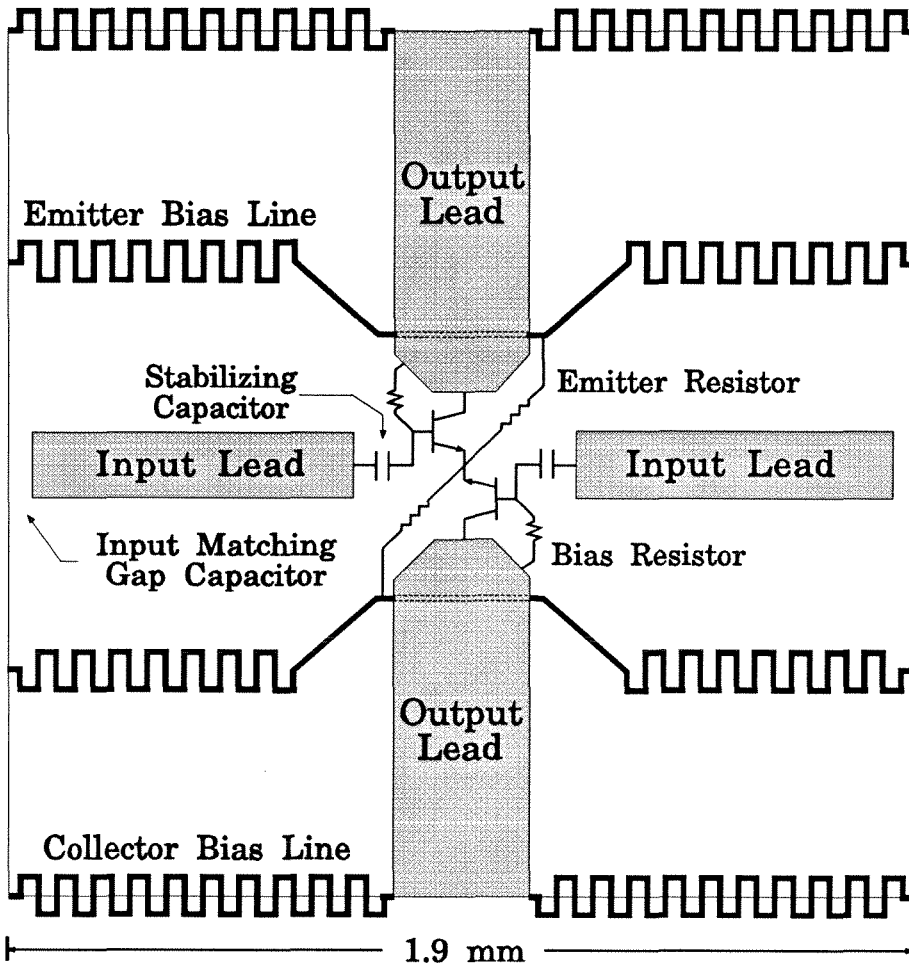
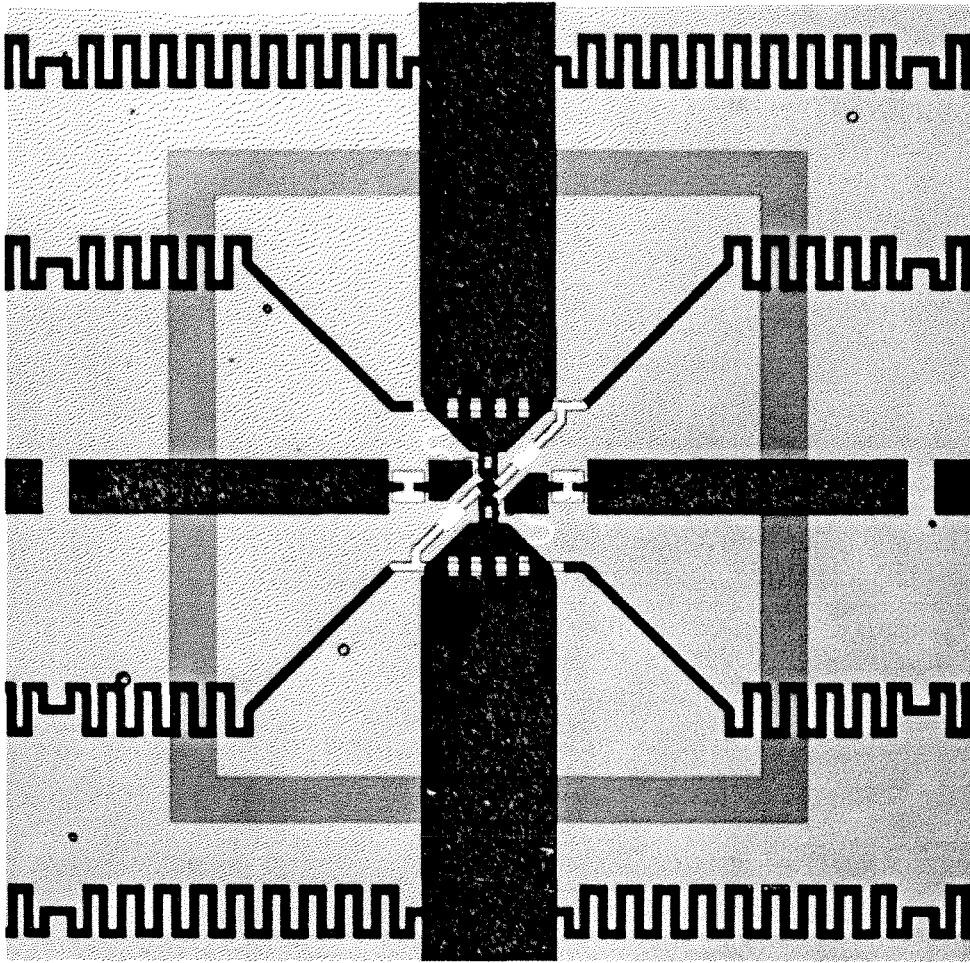


Fig. 4.5. Symbolic unit cell for the monolithic amplifier grid.

input leads and  $j180\ \Omega$  for output leads. Figure 4.4 shows lead reactances versus lead width for four unit-cell periods. These reactance curves were derived based on an EMF calculation developed by Robert Weikle at Caltech [14]. In the development of hybrid grids, the lead widths are about one tenth of the unit cell period. For the monolithic grid, 1.9 mm is chosen as the period of the unit cell. Correspondingly, the input lead width is  $120\ \mu\text{m}$  and the output lead is  $300\ \mu\text{m}$ .

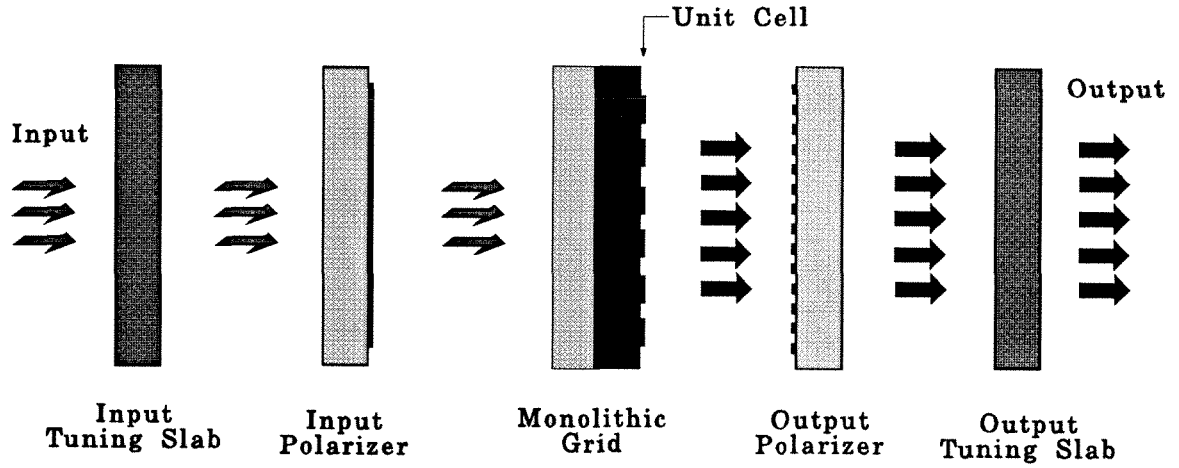
Figure 4.5 shows the symbolic plot for the unit cell. The input matching gap capacitor,  $30\text{-}\mu\text{m}$  wide, cancels the inductive reactance of the input lead. From HFSS simulation results, the capacitance of the input matching gap is 62 fF. The



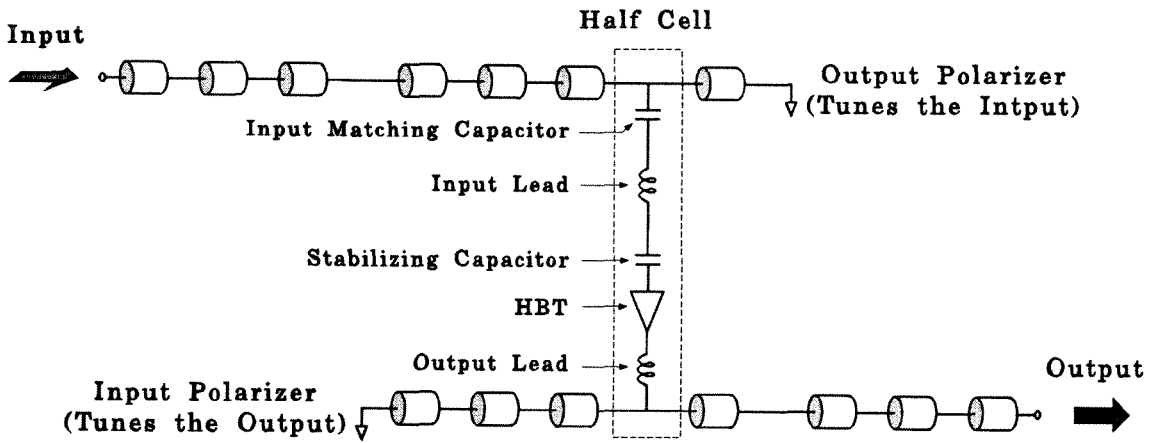
**Fig. 4.6.** Photo of the unit cell of the monolithic amplifier grid.

stabilizing capacitor prevents the common-mode oscillations of the grid amplifier. The two  $300\text{-}\Omega$  emitter resistors are to reduce the common-mode gain of the transistors. The  $4\text{-k}\Omega$  bias resistor provides a self-biasing configuration. The transistors are biased by the meandering lines. The width of the meandering line is  $20\text{ }\mu\text{m}$ .

A photo of the unit cell is shown in Fig.4.6. In the center of the unit cell, two transistors are located as close as possible to avoid the inductance of the connection between emitters. The emitter bias lines were connected underneath the output leads.



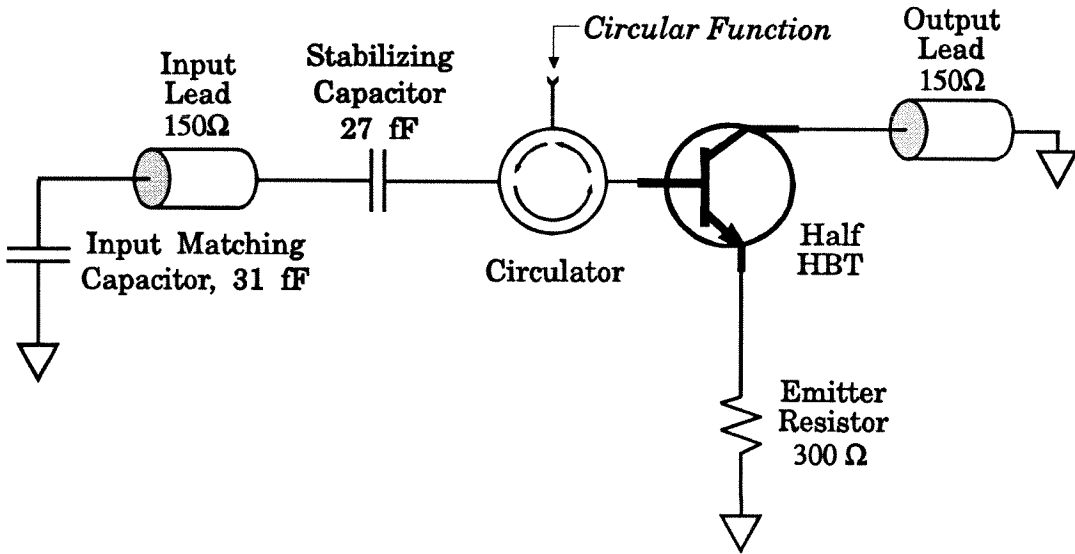
(a)



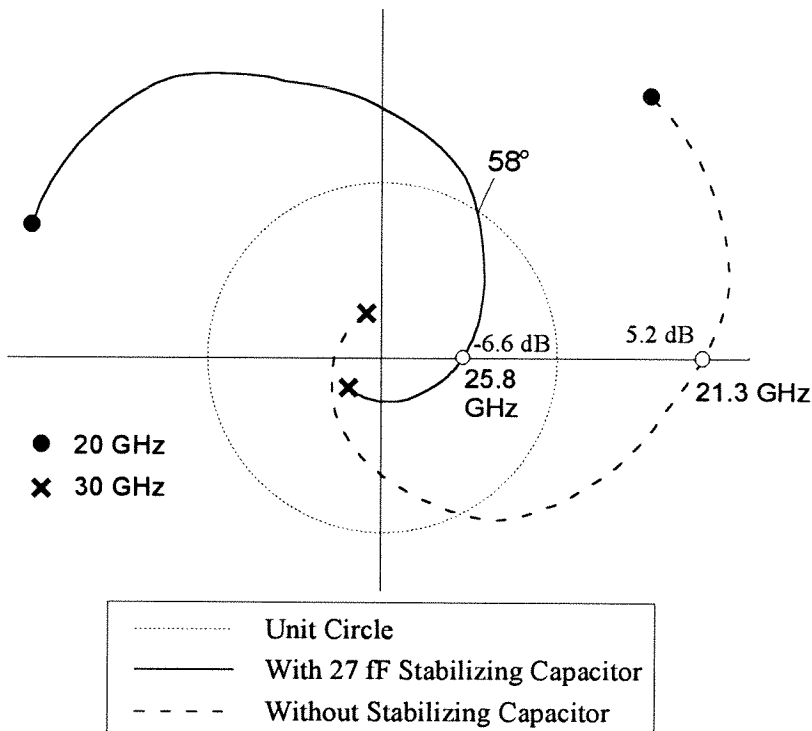
(b)

**Fig. 4.7.** (a) Side view of the monolithic grid amplifier. (b) The corresponding transmission-line equivalent circuit.

Based on the analysis in Sec. 2.2, the monolithic grid amplifier (Fig. 4.7.(a)) can be represented by an equivalent-circuit model (Fig. 4.7.(b)). Dielectric layers and air gaps in the measurement setup are represented by transmission lines. The unit cell links the input and output. The polarizers confine the signal path from the left, input with horizontal polarization, to the right, output with vertical polarization. The matching conditions are determined reactively by the



**Fig. 4.8.** Stability model. A stabilizing capacitor is employed at the base end.



**Fig. 4.9.** Circular function loci for stability analysis. The stabilizing capacitor offers a positive phase shift and reduces the zero-phase magnitude to  $-6.6$  dB. The grid amplifier is predicted stable with a gain margin of  $6.6$  dB and a phase margin of  $58^\circ$ .

polarizers and resistively by the tuning slabs.

At the design frequency of 40 GHz, the input impedance for the maximum available gain is  $4.8 + j9.1 \Omega$ . It is important to match the input because the resistive part of the corresponding input impedance is much lower than half of the free-space impedance,  $188.5 \Omega$ . To match the input, the GaAs substrate, of  $565\text{-}\mu\text{m}$  thickness, serves as a quarter-wavelength transformer and accomplishes the resistive matching condition. Nevertheless, the quarter-wavelength GaAs substrate will increase the quality factor,  $Q$ , of the grid amplifier and result in narrower bandwidth.

#### 4.2.2 STABILITY ANALYSIS

In previous hybrid grid amplifiers, common-mode oscillations were observed (Chapter 3). These spurious oscillations limited the gain and power performance of the grid amplifiers. To improve the stability, stabilizing capacitors were used in the monolithic amplifier grid.

The stability model, shown in Fig. 4.8, is used to analyze the common-mode oscillation of the grid amplifier, as described in Chapter 3. The input and output leads are represented by transmission lines, the characteristic impedance and electric length of which are derived based on a material with the mean dielectric constant of the substrate and air. A Metal-Insulator-Metal (MIM) capacitor of  $54\text{ fF}$  was located at the base end to stabilize the grid. Figure 4.9 shows the plot of the circular functions for the stability analysis. Without the stabilizing capacitors, the grid is predicted to oscillate at 21.3 GHz, where the zero-phase magnitude is larger than unity. The stabilizing capacitor gives a  $121^\circ$  phase shift to the circular function thus stabilizing the grid. Based on the stability analysis, with the stabilizing capacitors, the grid is stable with a phase margin of  $58^\circ$  and a gain margin of 6.6 dB.



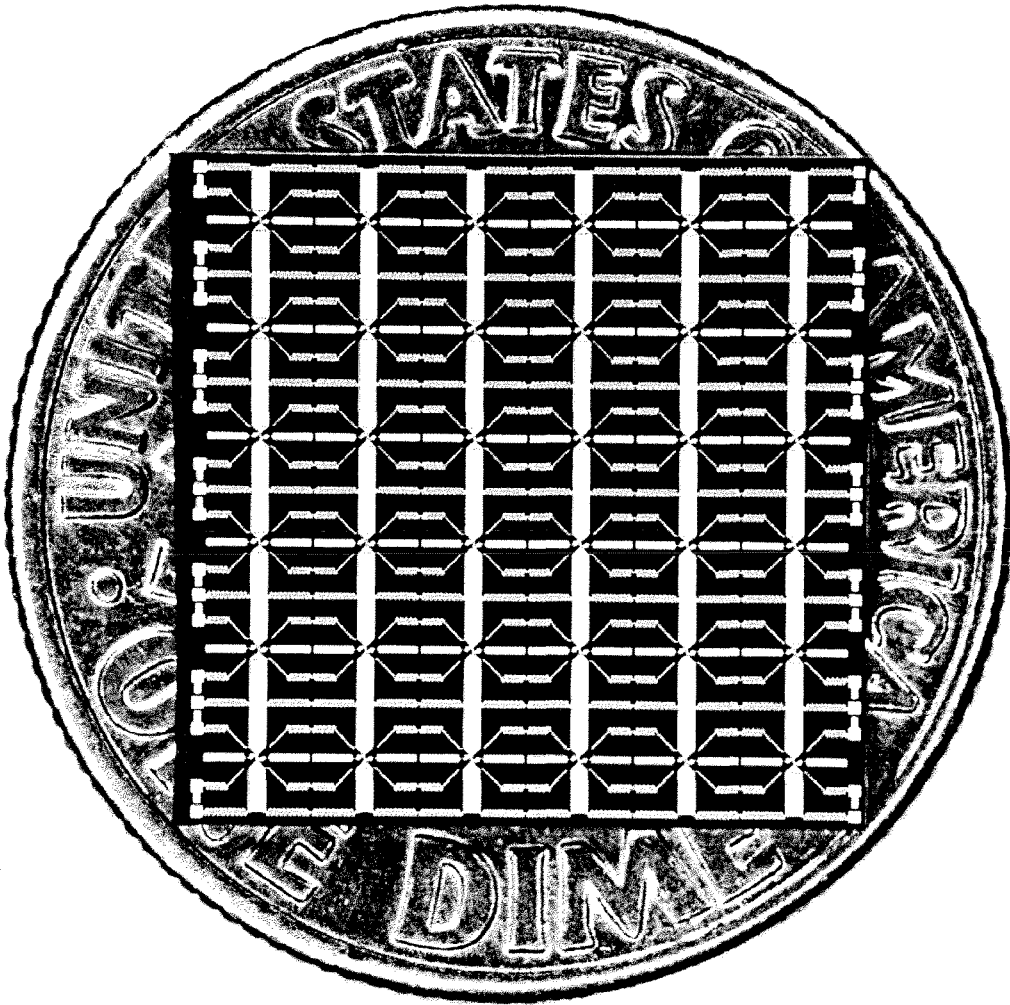
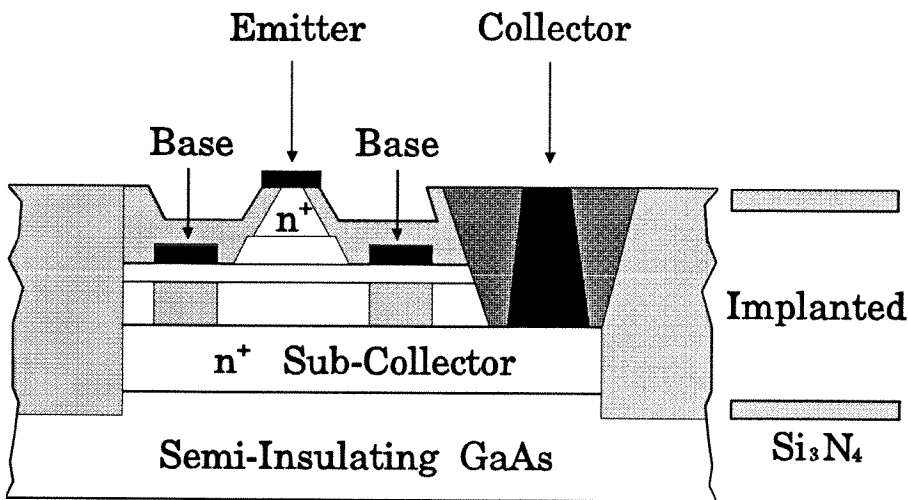


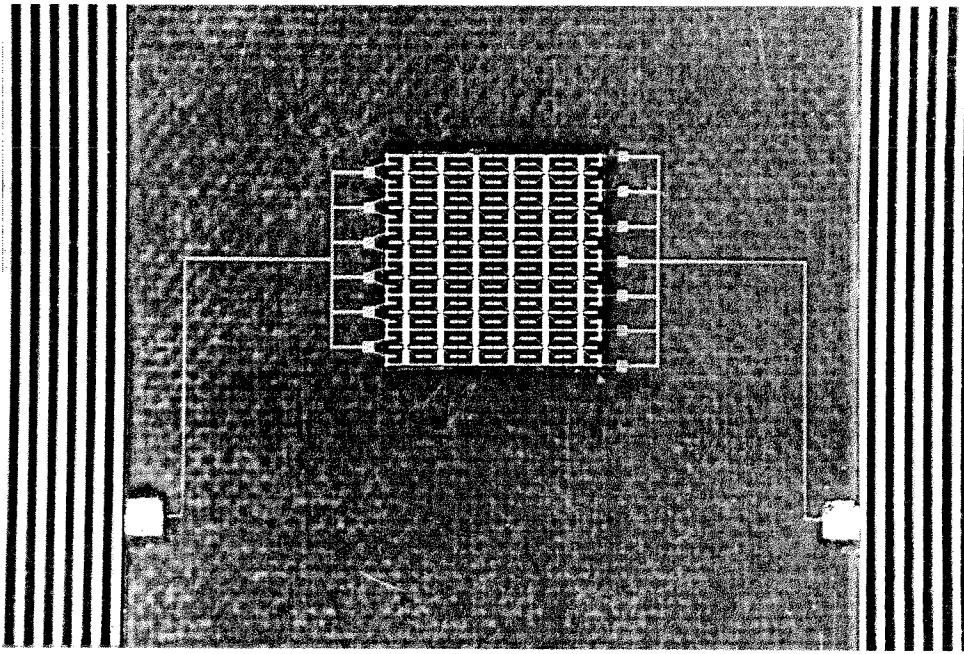
Fig. 4.10. Photo of a monolithic amplifier grid compared with a dime.

### 4.3 FABRICATION

The monolithic amplifier grid, shown in Fig. 4.10, is composed of 36 unit cells periodically distributed on a 565- $\mu\text{m}$  thick GaAs substrate. A self-aligned and self-passivated Rockwell HBT process was used to fabricate the grid. A typical device cross section is shown in Fig. 4.11. In this process, the emitter base self-alignment and edge passivation were processed using a single photolithography step. The emitter GaAs cap was selectively etched down to the AlGaAs emitter layer using reactive ion etch with the proper undercut control. A thin photo-enhanced CVD  $\text{Si}_3\text{N}_4$  layer was then deposited and etched away with  $\text{Si}_3\text{N}_4$  left only on the sidewalls and undercut regions of the emitter. The remaining  $\text{Si}_3\text{N}_4$  protects the AlGaAs in the GaAs undercut region from the subsequent AlGaAs etch and was used to passivate the emitter periphery. To expose the base layer for making the base metal contact, the exposed AlGaAs was subsequently etched away anisotropically. The collector in this extrinsic base region was metal and another  $\text{Si}_3\text{N}_4$  layer was deposited and lifted off at the same time. This process preserves the self-aligned emitter base structure to enhance the device RF performance and leaves a depleted AlGaAs layer(0.3- $\mu\text{m}$  width) to suppress the



**Fig. 4.11.** Representative self-aligned, self-passivated  $\text{AlGaAs}/\text{GaAs}$  HBT device cross section.



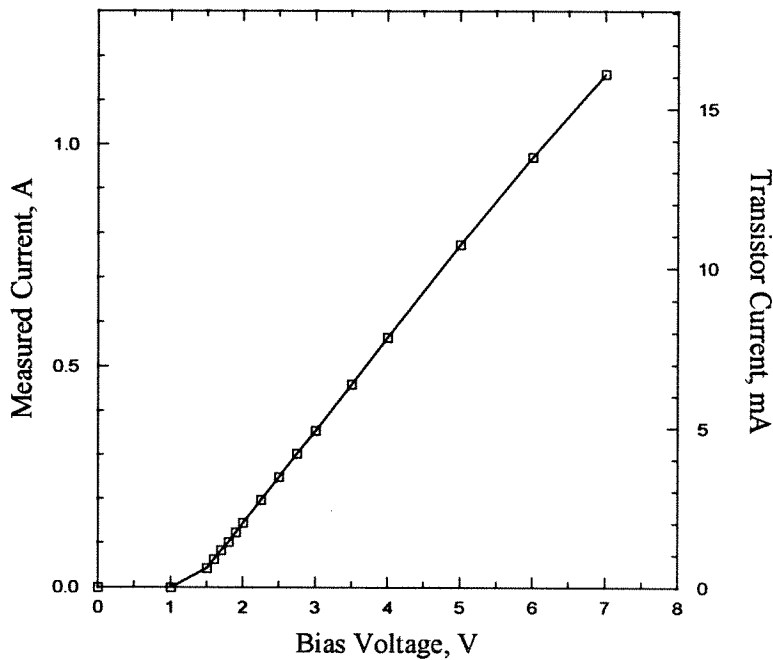
**Fig. 4.12.** Photo of a monolithic amplifier grid attached on a Duroid substrate. The grid was biased laterally, the right for the collectors ( $V_{cc}$ ) and the left for emitters (Ground).

surface recombination in the emitter periphery, thus achieving high DC current gain. The processing uniformity, device yield, and the device performance were reported in [15,16].

Figure 4.12 shows a photo of a monolithic amplifier grid attached on a 62-mil Duroid holder, with a relative dielectric constant of 2.2. The grid is biased laterally—the left is for emitter bias (ground) and the right is for collector bias ( $V_{cc}$ ). To avoid parasitic oscillations at very low frequencies, a low-pass filter was implemented at each bias end of the monolithic grid.

#### 4.4 GAIN MEASUREMENTS

In the measurements, no oscillation has been observed—the grid is highly stable. Each HBT transistor was proved sound by individual-row DC measurements and infrared-viewer inspection. The typical DC characteristic curve of the self-biased transistor is shown in Fig. 4.13. To avoid electrical and thermal



**Fig. 4.13.** DC characteristic curve for the entire 36-element grid.

damage, the grid was tested with bias voltages of less than 7 V.

#### 4.4.1 FREQUENCY RESPONSE

The gain is measured in the far field (Chapter 5), as shown in Fig. 4.14. At the maximum bias voltage, 7 V, the DC current of the entire grid was about 1.2 A. A considerable DC dissipation resulted from bias-line resistance, emitter resistance, and inefficiency of the HBT transistors. Because of large DC dissipation power, each measurement was taken in a time period of 0.6 second to avoid thermal damage to the grid. At 7 V, two sequential measurements were separated by a time period of 3 minutes to ensure that the transistors were completely cooled down. The pulse-mode measurements were controlled by a computer.

In the beginning, the grid was measured in a configuration shown in Fig. 4.7. The input tuning slab is a 50-mil Duroid layer with a relative dielectric constant of 10.8. The output tuning slab is a 30-mil thick AlN layer. The gain response, from 37 to 43 GHz, is shown in Fig. 4.15. The maximum gain is 5 dB at 40.8 GHz

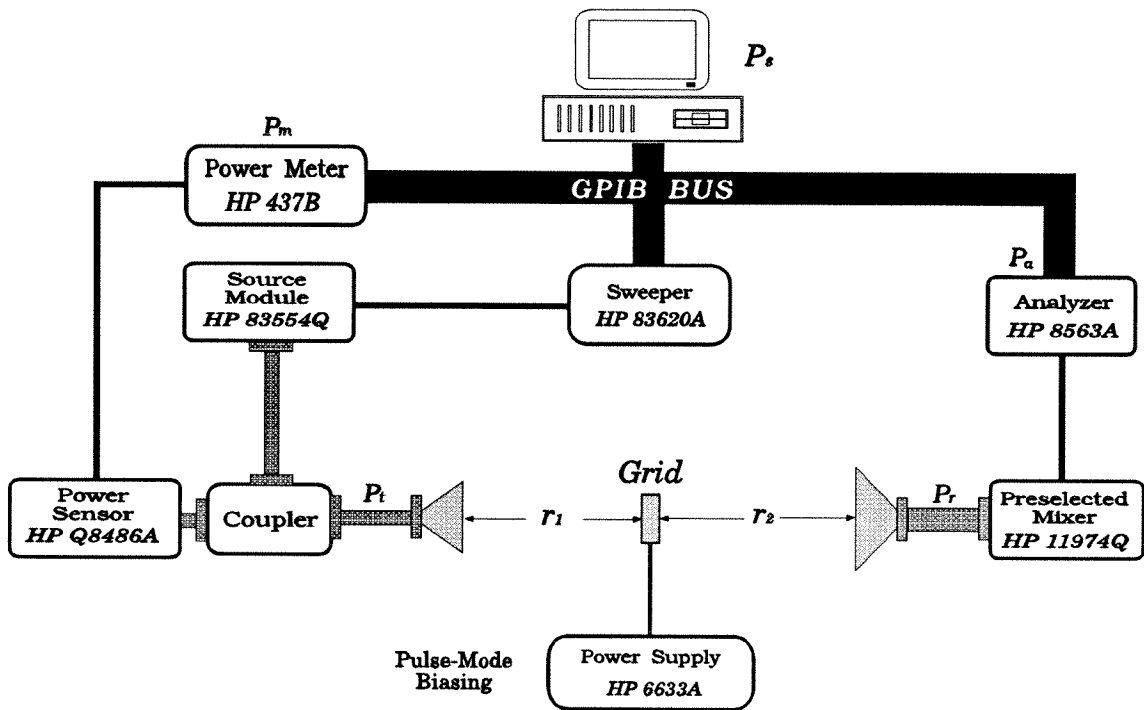


Fig. 4.14. Measurement setup for gain response.

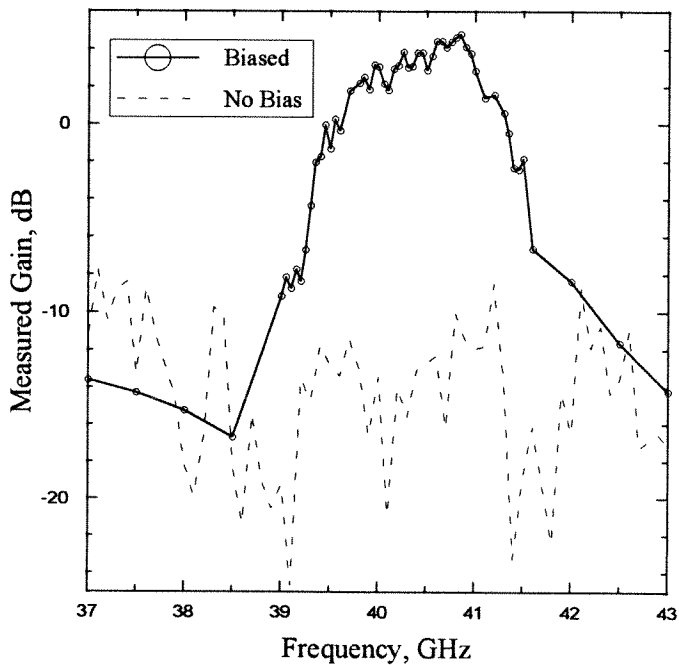
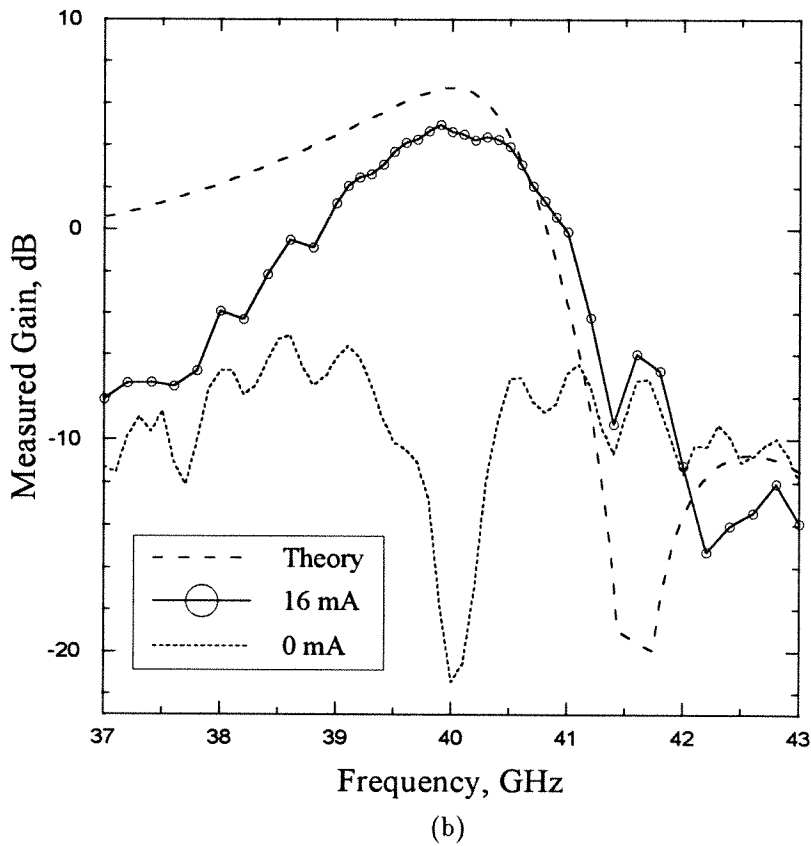
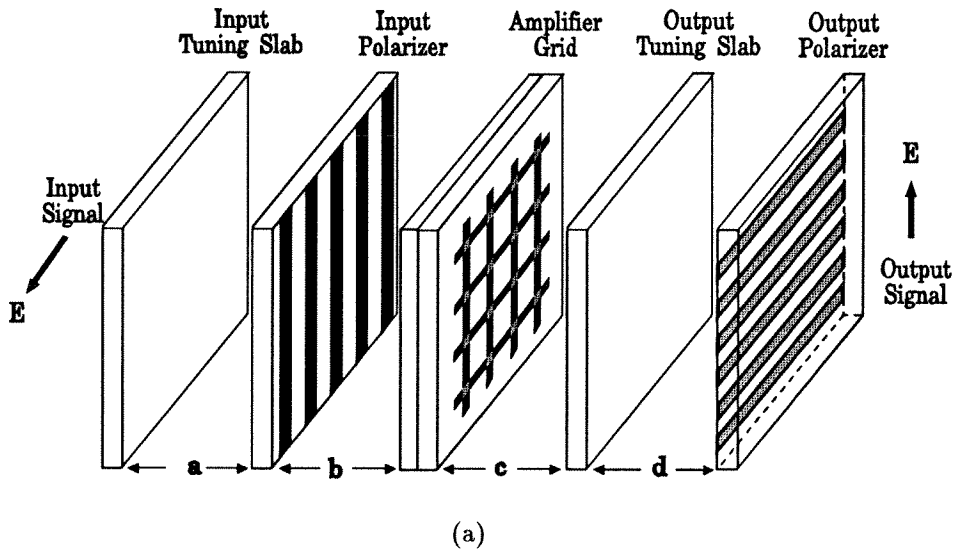


Fig. 4.15. Gain response measured with the configuration of Fig. 4.7. The peak gain is 5 dB at 40.8 GHz and the 3-dB bandwidth is 1.4 GHz, 3.5%.



**Fig. 4.16.** (a) Alternative configuration of the monolithic grid amplifier. The output polarizer is between the amplifier grid and the output polarizer. (b) This configuration has a peak gain of 5 dB at 40 GHz and a 3-dB bandwidth of 1.8 GHz, 4.5%.

Layer	$\epsilon_r$	Dimension (mm)	Elec. Length (° @40 GHz)
Substrate	12.8	0.56	96
Polarizer	2.2	0.38	27
Input Tuning Slab	2.2	0.64	45
Output Tuning Slab	10.8	0.64	100
Air Spacing $a$	1	1.3	60
Air Spacing $b$	1	1.7	82
Air Spacing $c$	1	4.1	198
Air Spacing $d$	1	3.9	189

**Table 4.1.** Physical parameters of the grid amplifier(Fig. 4.16(a)).

and the 3-dB bandwidth is 1.4 GHz (3.5%). The narrow bandwidth may be a result of the critical matching condition at the input end. The stabilizing capacitor and the quarter-wavelength GaAs substrate also increase the  $Q$  factor of the grid. The difference between the biased and zero-biased gains (on-off ratio) is 29 dB at the tuned frequency of 40.5 GHz.

An alternative configuration of polarizers and tuning slabs was used to obtain wider bandwidth, as shown in Fig.4.16(a). The gain response, from 37 to 43 GHz as shown in Fig.4.16(b), has a peak of 5 dB at 40 GHz and a 3-dB bandwidth of 1.8 GHz(4.5%). The bandwidth is wider than the previous measurement. This improvement of gain bandwidth was achieved empirically. The physical parameters for the complete grid amplifier is shown in Table 4.1.

At high frequencies, due to the skin effect, surface resistivity,  $R_s$ , may cause a considerable conduction loss for the RF signal [17]. At a frequency of  $f$ , the calculated surface resistivity of gold is:

$$R_s \doteq 3.1 \times 10^{-7} \times \sqrt{f} \quad \Omega/\text{square}. \quad (4.1)$$

For the monolithic grid, at 40 GHz, the calculated surface resistance is about  $0.5 \Omega$  for the input lead (950  $\mu\text{m}$  long and 120  $\mu\text{m}$  wide) and  $0.2 \Omega$  for the output

lead ( $950\text{ }\mu\text{m}$  long and  $300\text{ }\mu\text{m}$  wide). Figure 4.17 shows the predicted gain drop as a function of the input-lead surface resistance at 40 GHz. There is a 0.5 dB drop resulting from this surface resistance. The theoretical gain derived from the transmission-line equivalent-circuit model, with the surface resistances, is also shown in Fig. 4.16.(b). The gain difference between measurement and theory is about 2 dB at 40 GHz.

Figure 4.18 shows the gain versus the bias current at 40 GHz. The gain increases monotonically from  $-22\text{ dB}$  to  $5\text{ dB}$  as the bias current increases from 0 to 16 mA per transistor. The on-off ratio is 27 dB at 40 GHz.

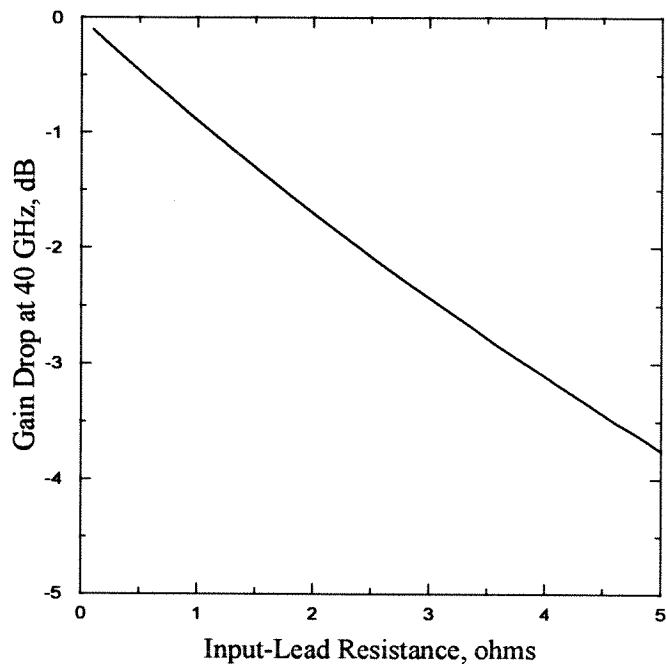
#### 4.4.2 TUNING CURVES

In the tuning measurements, relative gains were measured versus polarizer positions, as described in Sec. 2.4.2. Figure 4.19(a) shows the input tuning curve at 40 GHz. The minimums of measured gains are periodic with a period of  $180^\circ$ . A theoretical curve is also plotted and compared.

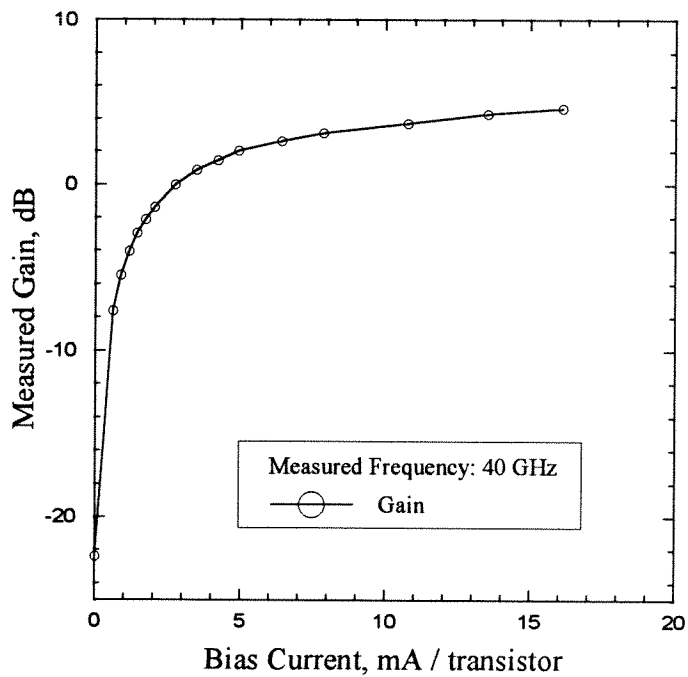
The measured input-tuning curve is different from the theoretical prediction. The peak-gain positions of the measurement and theory differ by 30 degrees. This may be due to the critical matching condition at the input. At 40 GHz, with the maximum gain, the optimal input impedance of the unit cell has a very small resistance and inductance. To match the input, the output polarizer needs to act as a capacitive tuner to cancel this small inductance. From theory, the matched position of the output polarizer is  $175^\circ$  from the amplifier grid. However, the peak of the radiation pattern will be steered away from the center as the polarizer moves close to positions with multiples of  $\lambda/2$  from the grid. The difference of peak-gain positions may be interpreted as a trade-off between electrical tuning and radiation steering.

Figure 4.19(b) shows the measured and theoretical output tuning curves at 40 GHz. The measurement shows reasonable agreement with the theory.

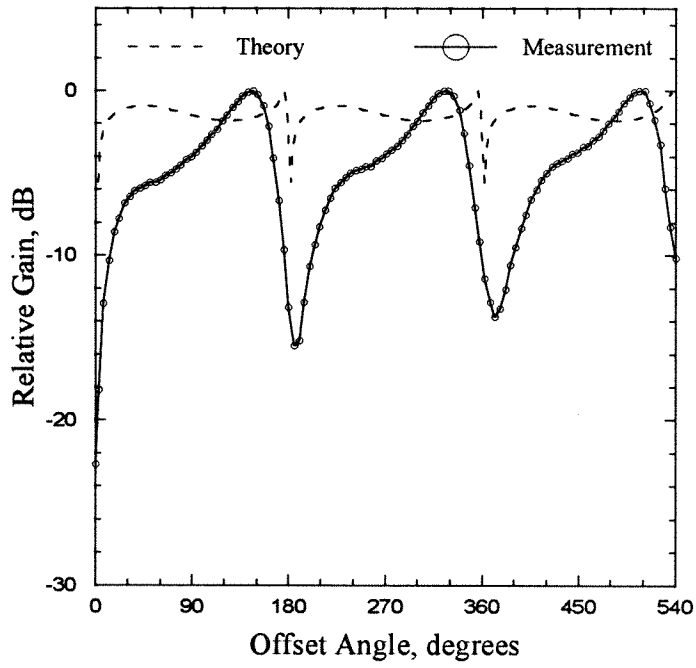




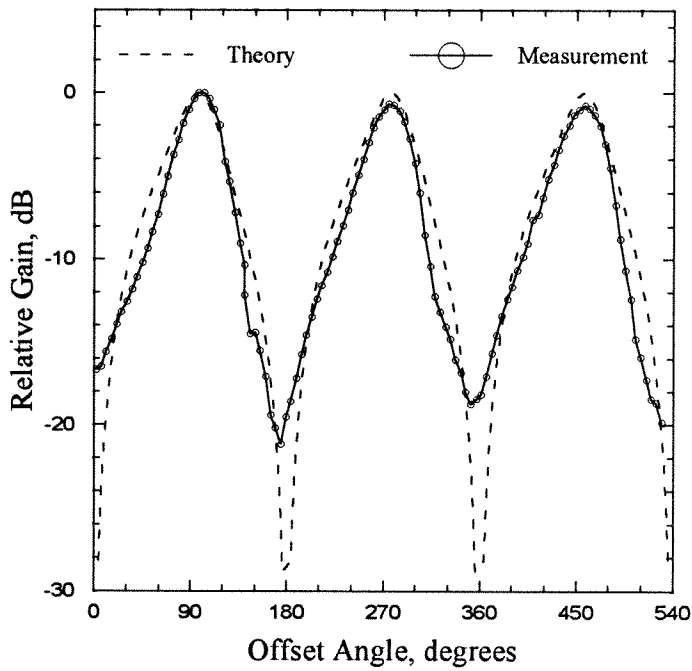
**Fig. 4.17.** Gain drop versus input-lead surface resistance at 40 GHz.



**Fig. 4.18.** Gain versus bias current at 40 GHz. The gain increases monotonically as the bias current increases.



(a)



(b)

**Fig. 4.19.** (a) Input tuning curve—relative gain curve as a function of output polarizer position.  
 (b) Output tuning curve—relative gain curve as a function of input polarizer position.

#### 4.4.3 RADIATION PATTERNS

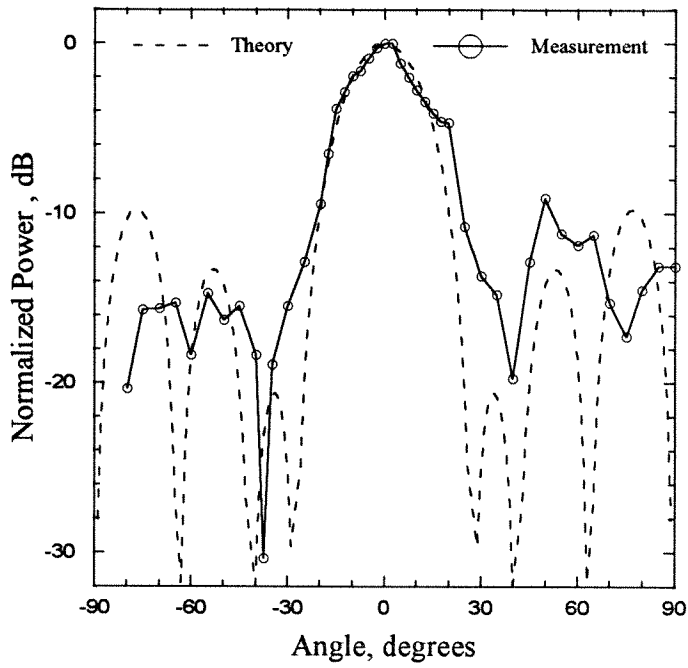
To avoid thermal damage, the radiation patterns were measured at a transistor current of 5 mA. The output H-plane radiation pattern is shown in Fig. 4.20(a). This pattern is measured by fixing the grid amplifier and the input antenna, and rotating the output antenna. The theoretical pattern of six elementary dipoles with a mirror 8.5-mm behind is also shown in Fig. 4.20(a). The measurement shows reasonable match to the theory in the main lobe. The measured side lobes were lower than the peak by more than 10 dB. No significant substrate-mode power was observed.

Figure 4.20(b) shows the input pattern, measured by fixing the grid and output antenna, and rotating the input antenna. The theoretical pattern of six elementary dipoles with a mirror 8.7-mm behind is also shown in Fig. 4.20(b). Similarly, side lobes were at least 10-dB lower than the main-lobe peak. The discrepancy between measurement and theory may be due to more layers at the input end and damage of transistors. This was the last measurement and the grid had degraded due to overheating in the power measurements.

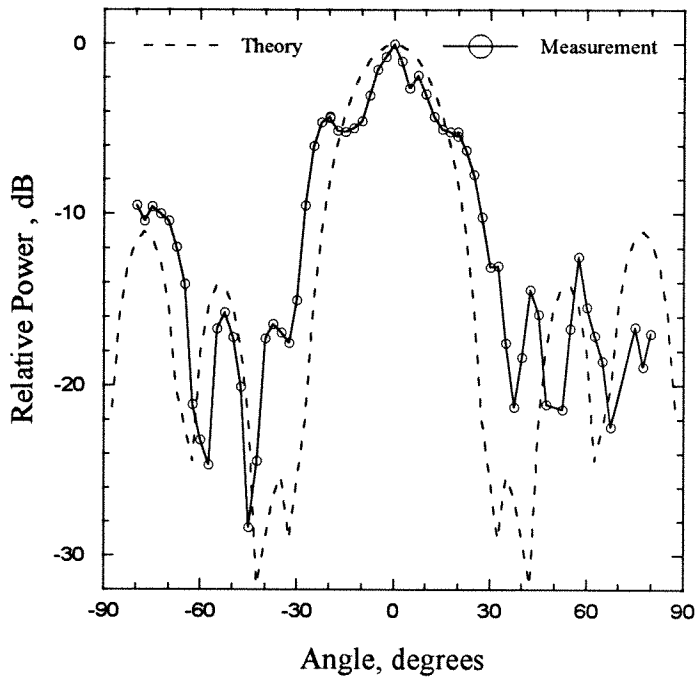
#### 4.5 POWER MEASUREMENTS

The power was also measured in the far field at 40 GHz. A Hughes 8010H 10-W Ka-band Traveling-Wave-Tube amplifier was used as a millimeter-wave source. The details of calibration and power-gain measurements are discussed in Chapter 5. In the power measurements, the input power on the monolithic grid was swept from 32 mW to 400 mW.

The HBT transistor has an active area of  $40 \mu\text{m}^2$  and is predicted to generate 20 mW at the optimal bias current of 20 mA. Figure 4.21 shows the output power versus the input power of the grid amplifier at three bias levels. The peak output power is 670 mW at 7 V with a bias current of 16 mA per transistor. Figure 4.22 shows the measured gain versus the input power at three biases, 3, 4, and 7 V.



(a)



(b)

**Fig. 4.20.** (a) Output radiation pattern. The theoretical pattern is calculated with six elementary dipoles with a mirror 8.5-mm behind. (b) Input radiation pattern. The theoretical pattern is calculated with six elementary dipoles with a mirror 8.7-mm behind.

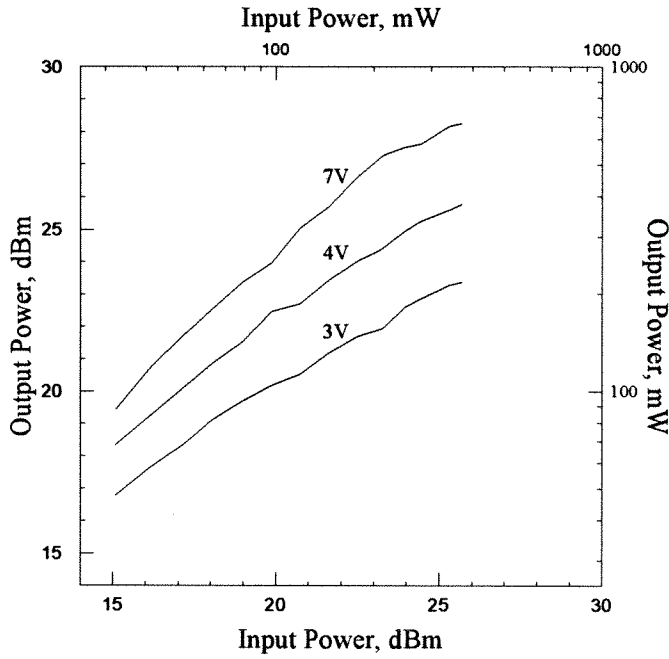
For 3 and 4 V, the output powers were saturated over the entire measured range of the input power. The 1-dB compression point at 7 V is 250 mW with an output of 500 mW. The gain drops to 2.5 dB at the maximum output power of 670 mW.

Figure 4.23 shows the output power versus bias voltage at four input power levels. Output power increases monotonically with increasing bias voltage. Figure 4.24 shows the grid gain versus bias voltage at four input power levels.

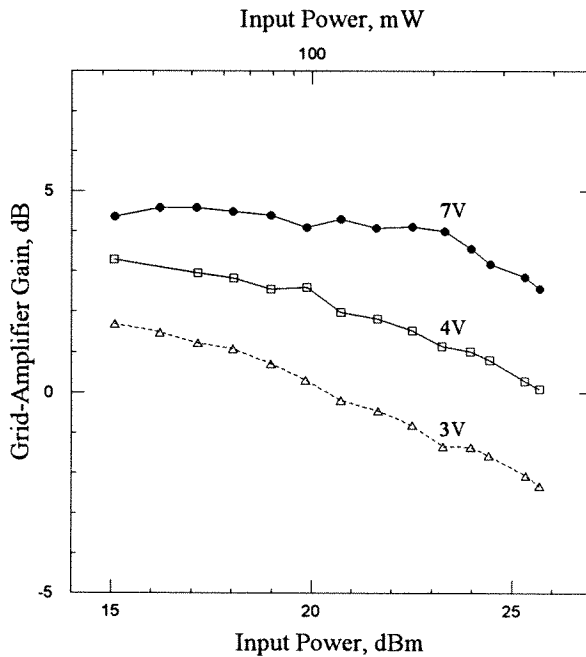
The power-added efficiency of the grid at 4 V and 7 V is shown in Fig. 4.25(a). The peak efficiency is 4% at 7 V. From the DC measurement, the meandering bias line had DC resistance of about  $15\ \Omega$  per row. The bias-line resistance results from the very narrow and long second metallization. The DC power dissipation of the meandering bias lines was 3.1 W, 38% of the supply power. Another contribution to the DC power dissipation was associated with the emitter resistors. The entire grid had a dissipation of 2.8 W on the seventy-two  $150\text{-}\Omega$  emitter resistors. Totally, we have about 73% of the supply power dissipated in the bias network, the meandering bias lines and emitter resistors. By discounting the DC dissipation of the bias network, the power-added efficiency of the HBT transistors is about three times as high as the power-added efficiency of the grid, as shown in Fig. 4.25(a). The peak power-added efficiency of the HBT transistor is 13%. Figure 4.25(b) shows the power-added efficiency versus the output power for the grid and the HBT transistor.

#### 4.6 TILING ISSUE

Essentially, the power capability of a grid is proportional to its size. In fabrication, the yield rate of a monolithic chip is mainly limited by the chip size. Tiling many monolithic grids together on a substrate seems to be a sound approach to accomplish high output power.



**Fig. 4.21.** Output power versus input power. At 7 V, the monolithic grid amplifier has a maximum output power of 670 mW at an input power of 380 mW.



**Fig. 4.22.** Gain versus input power. At 7 V, the grid has a small-signal gain of 4.5 dB and the gain drops to 2.5 dB with a maximum output power of 670 mW.

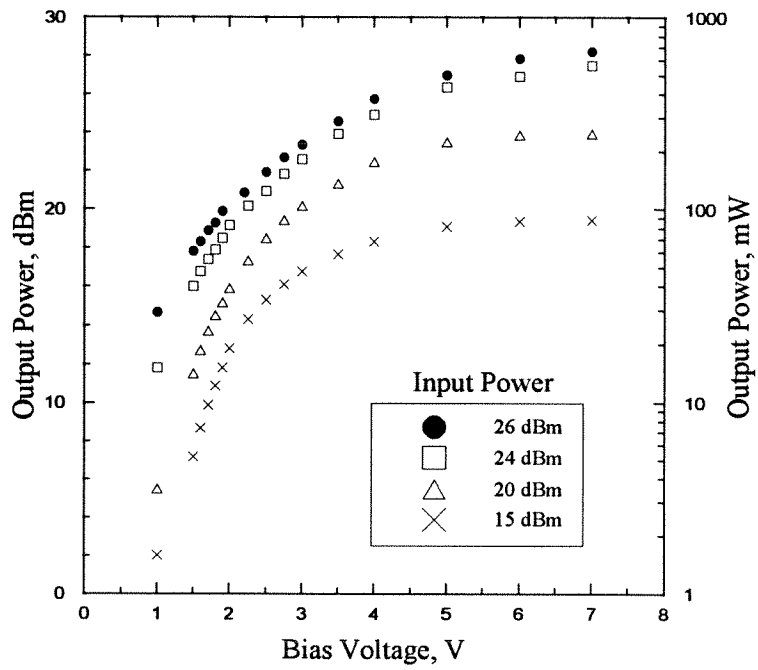


Fig. 4.23. Output power versus bias voltage.

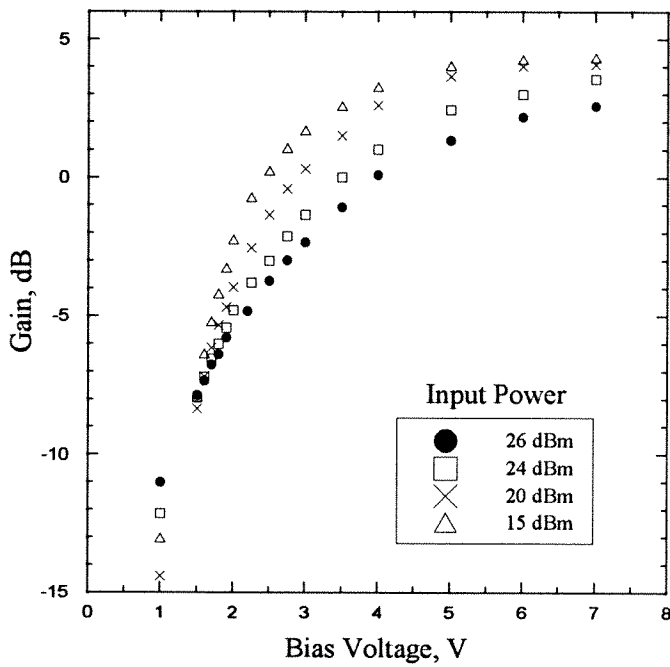
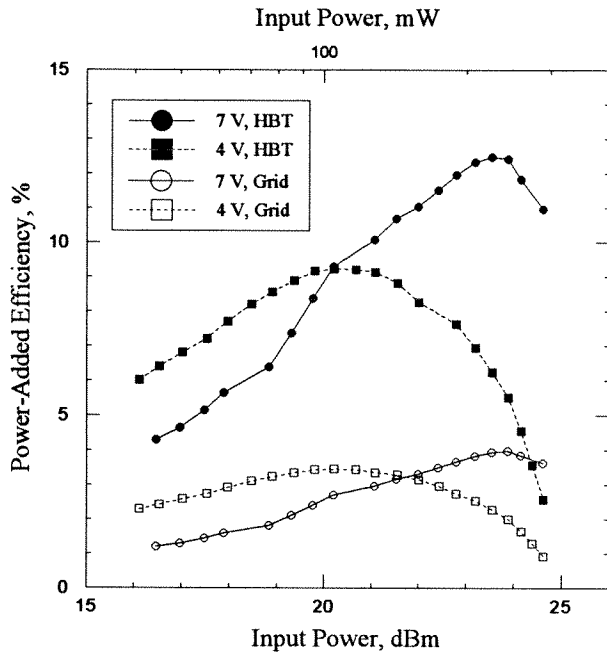
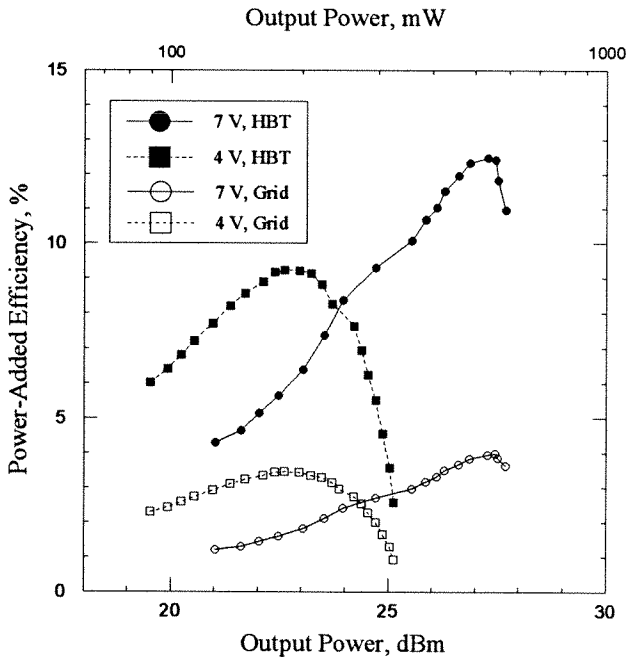


Fig. 4.24. Gain versus bias voltage.



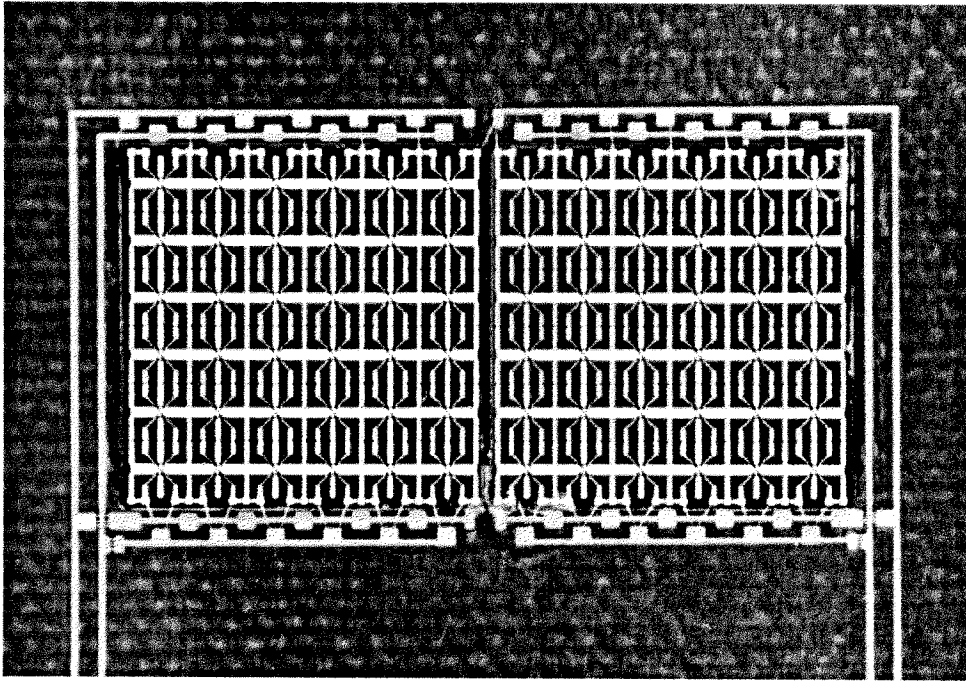
(a)



(b)

**Fig. 4.25.** (a) Power-added efficiency versus input power. The peak efficiency is 4% at 7 V at an input power of 250 mW. Discounting the DC dissipation in the bias network, the efficiency of the HBT transistors is plotted with solid symbols. The HBT transistor has a peak power-added efficiency of 12.5%. (b) Power-added efficiency versus output power.

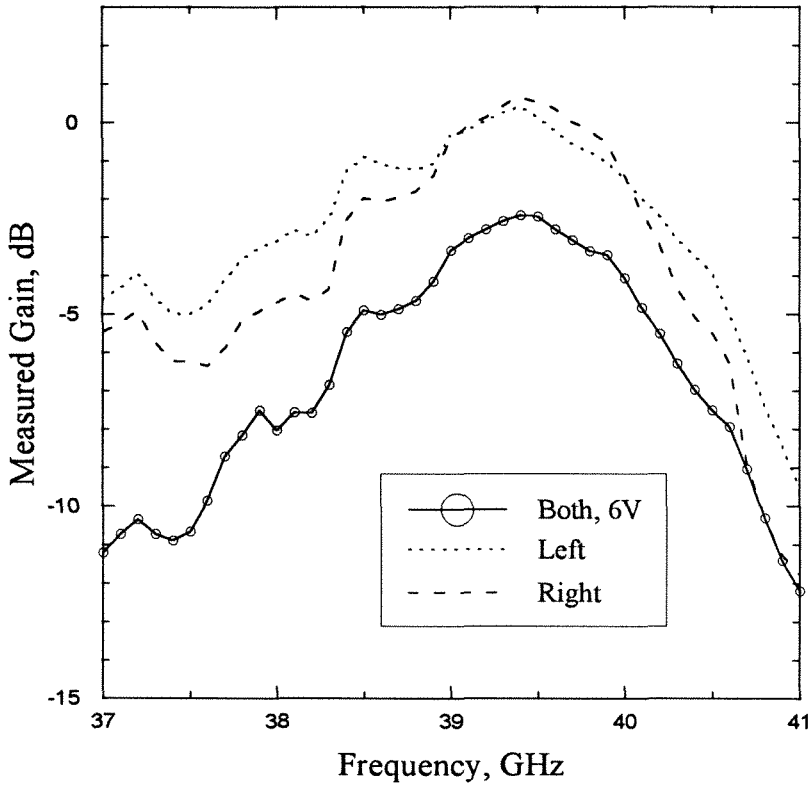




**Fig. 4.26.** Photo of the tiled grids in a  $2 \times 1$  format. The holder is a 62-mil Duroid substrate with a relative dielectric constant of 2.2.

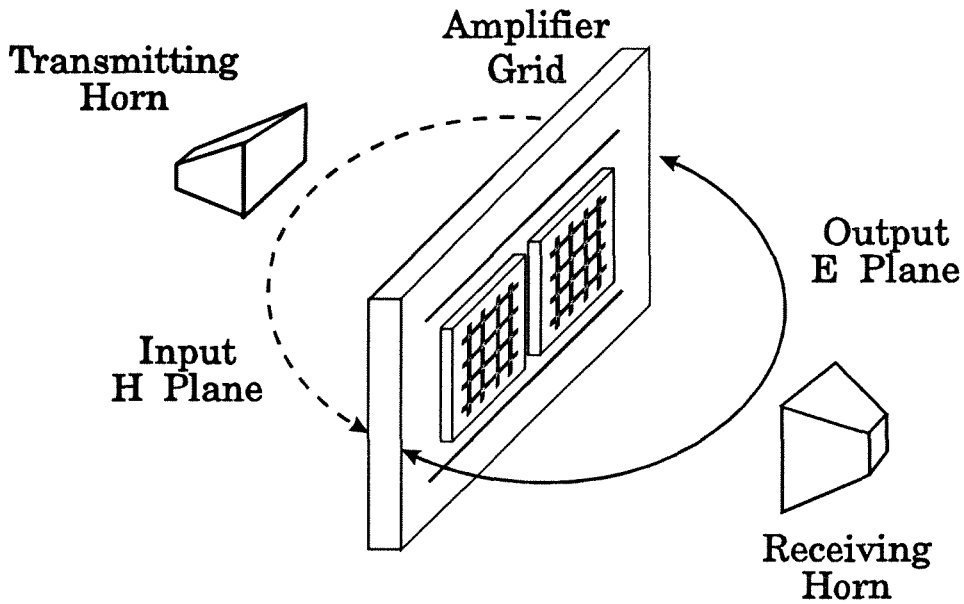
Figure 4.26 shows the photo of the tiled monolithic grids in a 2-by-1 format. Each grid was biased from top and bottom by an independent power supply. The measurement setup is similar to Fig. 4.14 and two power supplies were controlled individually by a computer. Only polarizers were used to tune the grids. The amplifier was tuned to maximize the tiled-grid gain rather than individual grid gain. The gain response is shown in Fig. 4.27. The peak gain of the tiled grids is  $-2.5$  dB at 39.4 GHz. Gains of two individual grids were also measured, as shown in Fig. 4.27. Each individual grid has a peak gain of about 0.5 dB at 39.4 GHz. Apparently, the peak gain of the tiled grids is less than the gain of individual grid by 3 dB. The gain mismatch suggests that the power combination is nonlinear. In other word, the power is not proportional to the number of the tiled grid.

For further insight, input and output radiation patterns in the plane with twelve elements were measured, as shown in Fig. 4.28. The patterns of individual



**Fig. 4.27.** Gain responses of the tiled and individual grids.

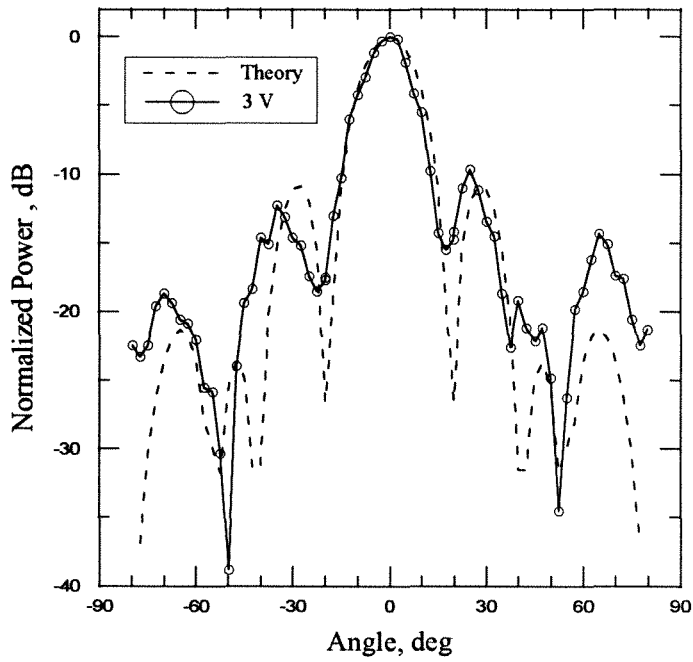
grids were also measured by turning the other grid off. Figure 4.29(a) shows the input H-plane pattern for the 12-by-6 tiled grids. The theoretical pattern is derived from seventy-two elementary dipoles in a 12-by-6 array format with a mirror 6.5-mm behind. The measurement shows good agreement with the theory. Two input-H-plane patterns of individual grids are shown in Fig. 4.29(b). Unlike the tiled grid, individual grids have obviously different patterns from the theoretical prediction. The main lobes are narrower than the theory and the maxima of the main lobes are not in the center. The output E-plane patterns of the tiled grids are shown in Fig. 4.30(a). The theoretical pattern is derived from seventy-two elementary dipoles in a 12-by-6 array format with a mirror located 10.1-mm behind. The measurement shows good agreement with the theory. Two output-E-plane patterns of individual grids are shown in Fig. 4.30(b). Similarly, individual grids have obviously different patterns from the theoretical prediction.



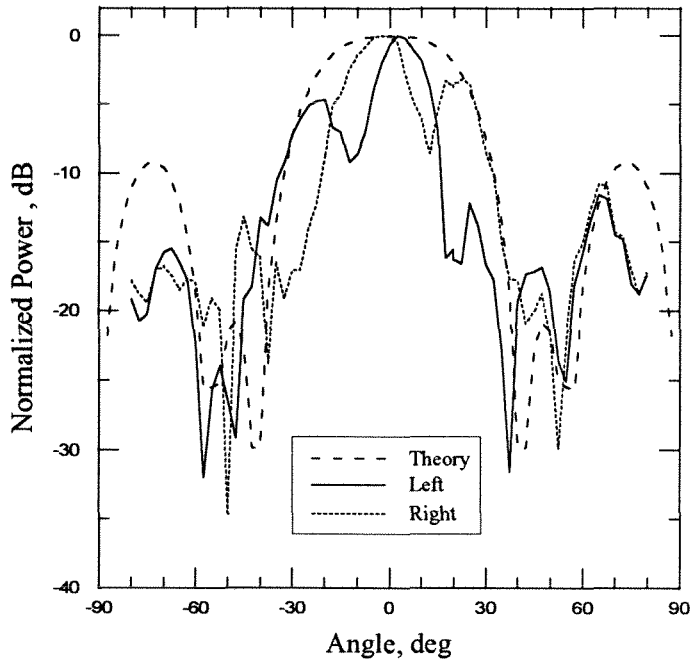
**Fig. 4.28.** Pattern measurement setup for the tiled grids. The horizontal plane is H plane for the input and E plane for the output. Polarizers are not plotted.

The mismatch of individual radiation patterns shows that the grid was perturbed by the other unbiased grid. However, the radiation patterns of the tiled grids show good agreement with the theory. Discontinuity of the grid substrate did not effect the tiled-grid radiation patterns.

This mismatch of gains can be due to the critical matching conditions of the grids. In the measurements, only an input polarizer and an output polarizer were used to tune the tiled grids. The individual grid is sensitive to the matching conditions. Dissimilarities in matching conditions of individual grids can cause difficulties in optimizing both grids for maximum gain.

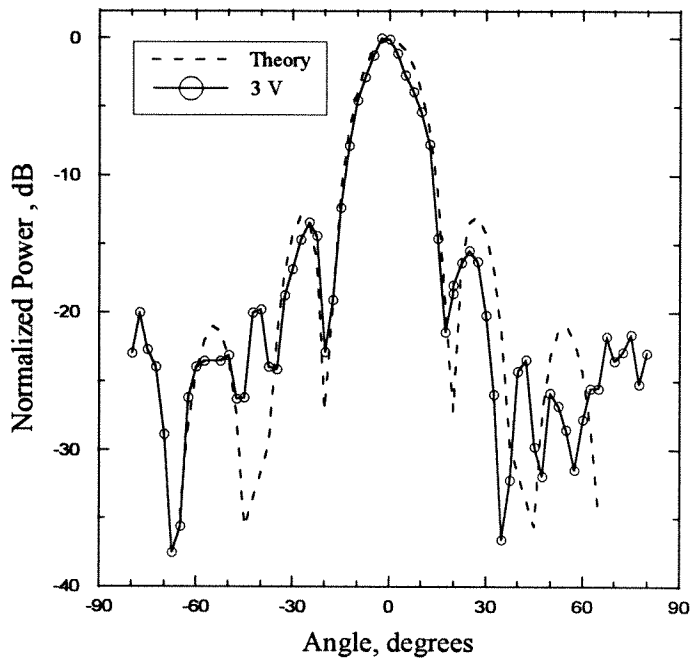


(a)

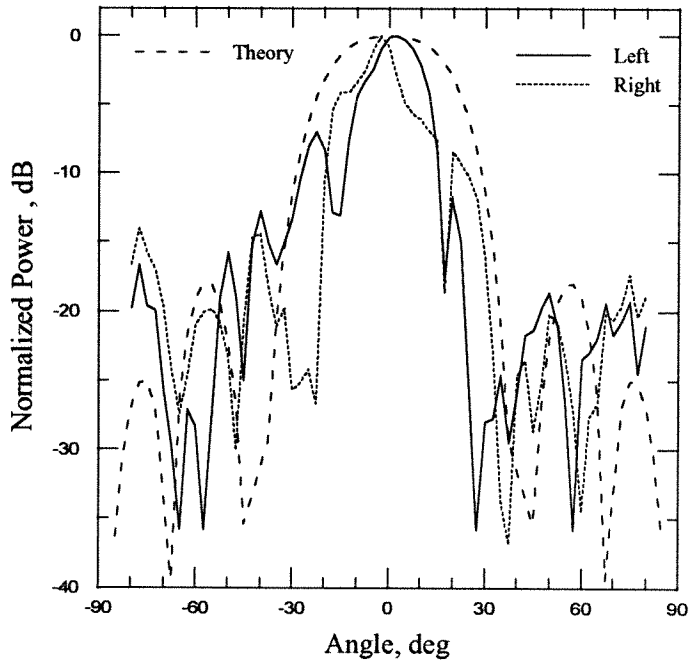


(b)

**Fig. 4.29.** (a) Input H-plane pattern of the tiled grid. The theoretical pattern is calculated with  $12 \times 6$  elementary dipoles with a mirror 6.5-mm behind. (b) Input H-plane patterns for the individual grids.



(a)



(b)

**Fig. 4.30.** (a) Output E-plane pattern of the tiled grid. The theoretical pattern is calculated with  $12 \times 6$  elementary dipoles with a mirror 10.1-mm behind. (b) Output E-plane patterns for the individual grids.

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## Chapter 5

### Far-Field Measurements

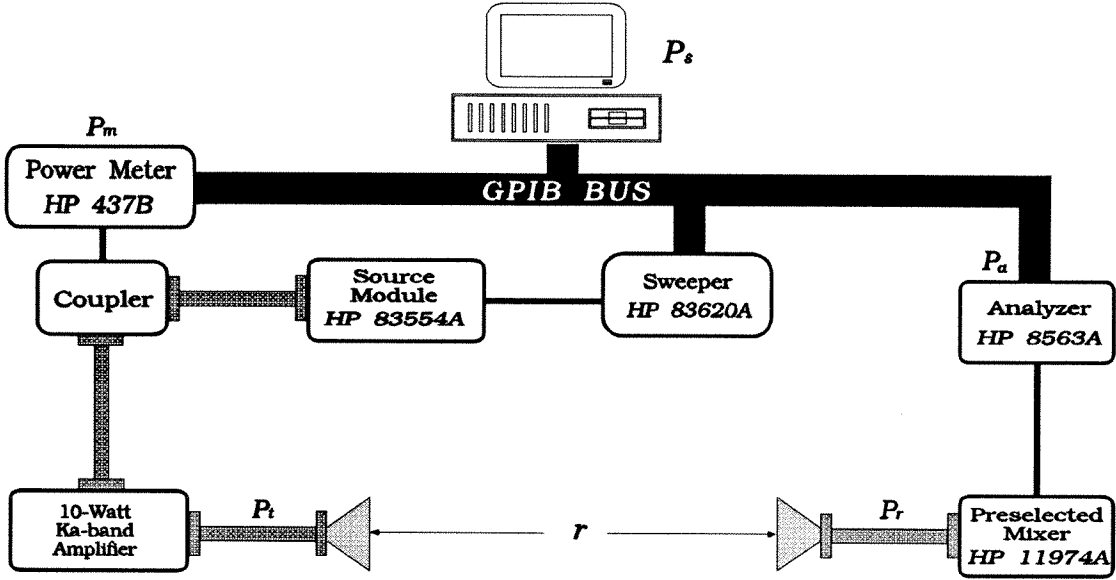
Far-field and lens-focus approaches have been used in the quasi-optical amplifier measurements [1]. Moonil Kim has demonstrated almost identical results of the 100-element HBT grid using both far-field and lens-focus approaches. The far-field approach is simpler and were used to measure the gain and power for the HBT grid amplifiers. This chapter discusses the setup and measurement techniques for the far-field approach used in the power measurements of the monolithic grid amplifier. Two validations of the far-field measurements are demonstrated. Grid aperture efficiencies are discussed.

#### 5.1 CALIBRATION MEASUREMENTS

The calibration set-up is shown in Fig. 5.1. The fundamental-band RF source was generated by an HP 83620A synthesizer. An HP 83554A source module was fed by the synthesizer to generate a 40-GHz RF signal. The output power level of the source module was controlled over the range of  $-15$  to  $0$  dBm and was monitored by an HP 437B power meter through a 10-dB coupler and an HP Q8486A power sensor. The RF signal was amplified by a Hughes 8010H 10-W Ka-band TWT(Traveling-Wave-Tube) amplifier. The amplified power level on the transmitting horn was 300 mW to 10 W.

At the receiving end, a horn antenna was used to receive the output signal from free space. The output spectrum was displayed on an HP 8563A spectrum analyzer following an HP 11974 preselected mixer. The gain measurement was





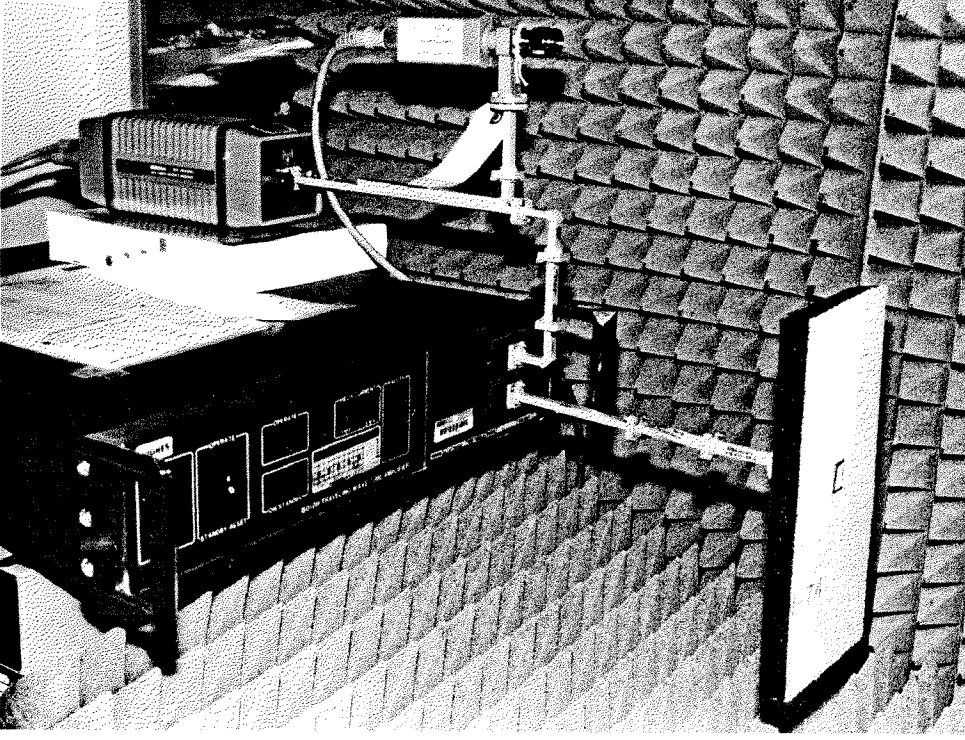
**Fig. 5.1.** Calibration setup for co-polarized measurements.

done in pulse mode rather than continuous-wave mode. Hence, we used a spectrum analyzer instead of a power meter to measure the output power because a power meter needs a few seconds for steady-state reading. In the power measurements, the power was measured in a time period of less than 1 second.

We require the calibrations of three instruments: the preselected mixer, the antenna horns, and the TWT power amplifier.

The first calibration is to measure the conversion loss of the preselected mixer. In this measurement, the coupler output was directly connected to the input of the pre-selected mixer. The conversion loss was the difference between the source module output,  $P_s$ , and the analyzer reading,  $P_a$ . In the following measurements, the conversion loss was valid only when the received power level was within the sweep range of the source power in this measurement.

The second calibration is to measure the effective area of the horn antennas. The transmitting and receiving horns are identical and have the same effective



**Fig. 5.2.** Photo of the connection among the 10-W TWT amplifier, the coupler, and the transmitting horn.

area. In this calibration, two horns were oriented in the same polarization with a separation distance of  $r$ . Based on the conversion loss of the first calibration, we can derive the ratio of transmitted power over received power,  $P_t/P_r$ . Hence, the effective area of the horns,  $A_{horn}$ , can be calculated by the Friis' transmission formula:

$$\frac{P_r}{P_t} = \frac{A_{horn}^2}{r^2 \lambda^2}, \quad (5.1)$$

and

$$A_{horn} = \left[ r^2 \lambda^2 \cdot \frac{P_r}{P_t} \right]^{1/2}. \quad (5.2)$$

The third calibration is to measure the power gain of the TWT power amplifier. The TWT power amplifier was added between the coupler output and the transmitting horn. A photo of the connection is shown in Fig. 5.2. By measuring

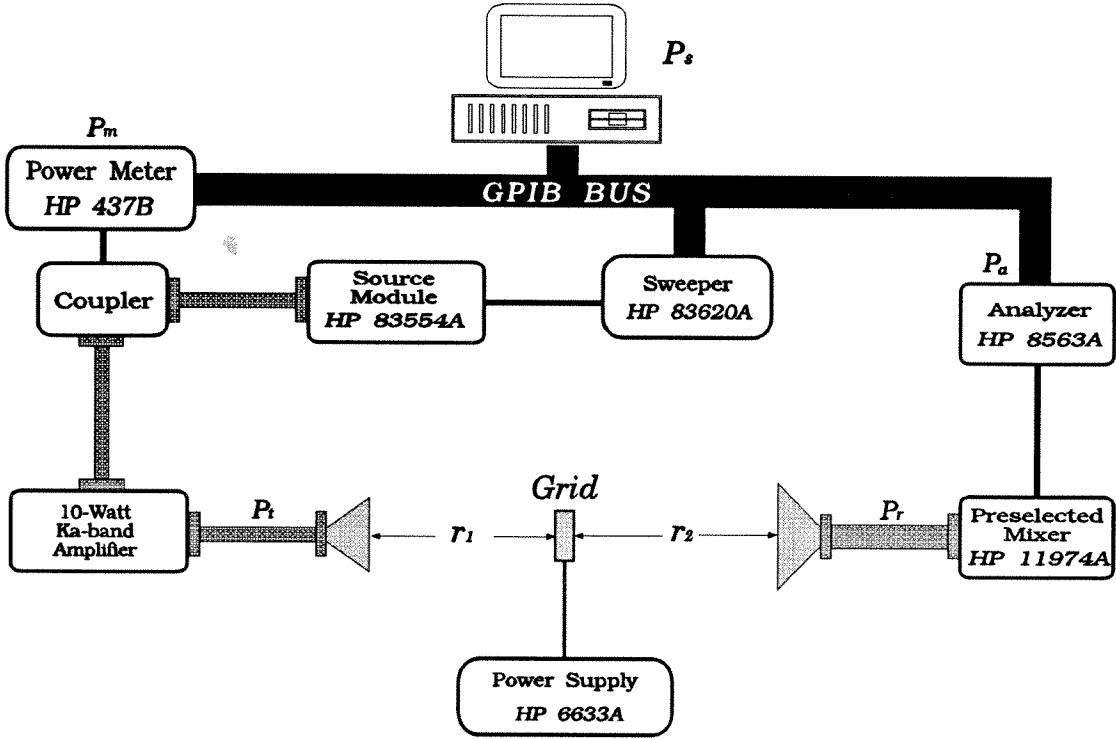


Fig. 5.3. Power gain measurement setup for cross-polarized measurements.

the received power, we can derive the gain of the power amplifier,  $G_{TWT}$ :

$$G_{TWT} = \frac{r^2 \lambda^2}{A_{horn}^2} \times \frac{P_r}{P_s}, \quad (5.3)$$

where  $P_s$  is the source power controller by the computer. In this measurement, the distance,  $r$ , was properly adjusted to ensure that the received power,  $P_r$ , was in the valid scope of the analyzer conversion loss. To have enough attenuation of the received power, the distance should be longer than the one in the second calibration measurement.

## 5.2 POWER GAIN MEASUREMENTS

After the calibrations, the grid was located between the horns and biased by an HP 6633A power supply, as shown in Fig. 5.3. The receiving horn was rotated

by  $90^\circ$  for the cross-polarized measurement. The power incident on the grid,  $P_{in,Grid}$ , is:

$$P_{in,Grid} = \frac{A_g A_{horn}}{r_1^2 \lambda^2} \times G_{TWT} \times P_s, \quad (5.4)$$

where  $A_g$  is the geometric area of the grid. Here, we assume the grid has an effective antenna area the same as its geometric area. Details of grid aperture efficiencies are discussed in Sec. 5.5. Similarly, the output power of the grid,  $P_{out,Grid}$ , is:

$$P_{out,Grid} = \frac{r_2^2 \lambda^2}{A_g A_{horn}} \times P_r. \quad (5.5)$$

Hence, the gain of the grid is:

$$G_g \equiv \frac{P_{out,Grid}}{P_{in,Grid}} = \frac{r_1^2 r_2^2 \lambda^4}{A_{horn}^2 A_g^2 G_{TWT}} \times \frac{P_r}{P_s}. \quad (5.6)$$

In the far-field gain measurements, as discussed in Sec. 2.4 and Sec. 4.4, without the TWT amplifier, (5.6) can be simplified to

$$G_g = \frac{r_1^2 r_2^2}{r^2} \cdot \frac{\lambda^2}{A_g^2} \times \frac{P_r}{P_c}, \quad (5.7)$$

where  $P_c$  is the received power in the calibration measurement and  $P_r$  is the received power in the gain measurement.

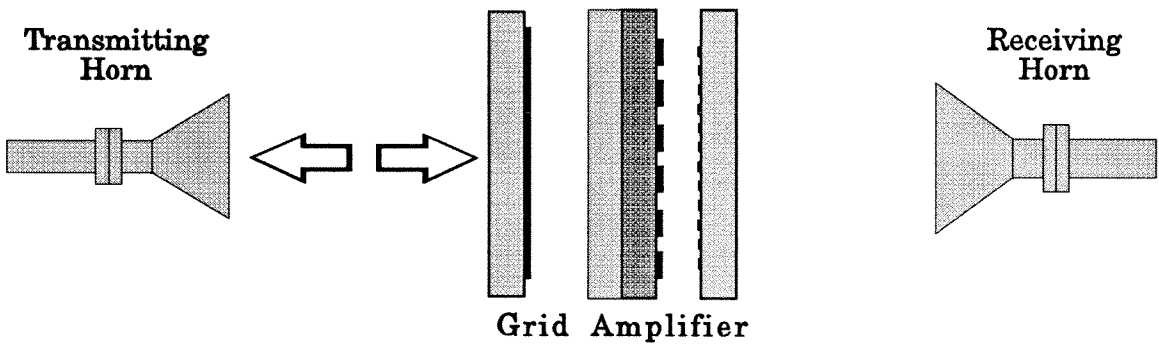
### 5.3 VALIDATION MEASUREMENTS

In the power measurement, the grid was located close to the transmitting horn to derive high input power on the grid. The boundary between near-field and far-field is [2]:

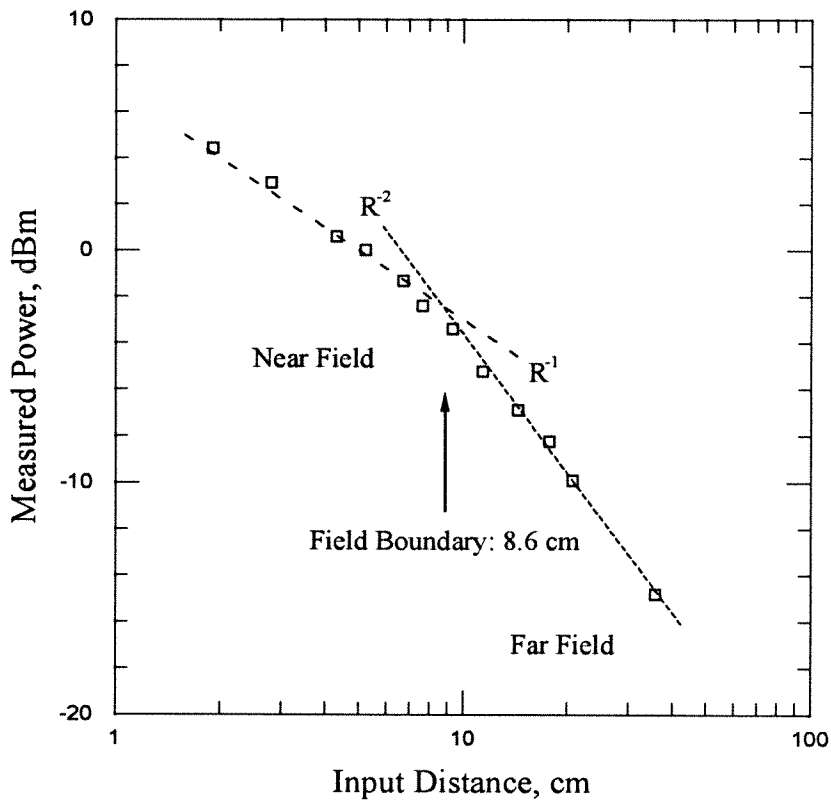
$$R_{ff} = \frac{2D^2}{\lambda}, \quad (5.8)$$

where  $D$  is the longest dimension of the grid or horn antenna. For the measurement,  $D$  is the longer side of the horn antenna with a length of 18 mm. The calculated  $R_{ff}$  is 86.4 mm.

Figure 5.4.(a) shows a simple measurement to verify the far-field boundary. The grid output power was measured at different input distances around the

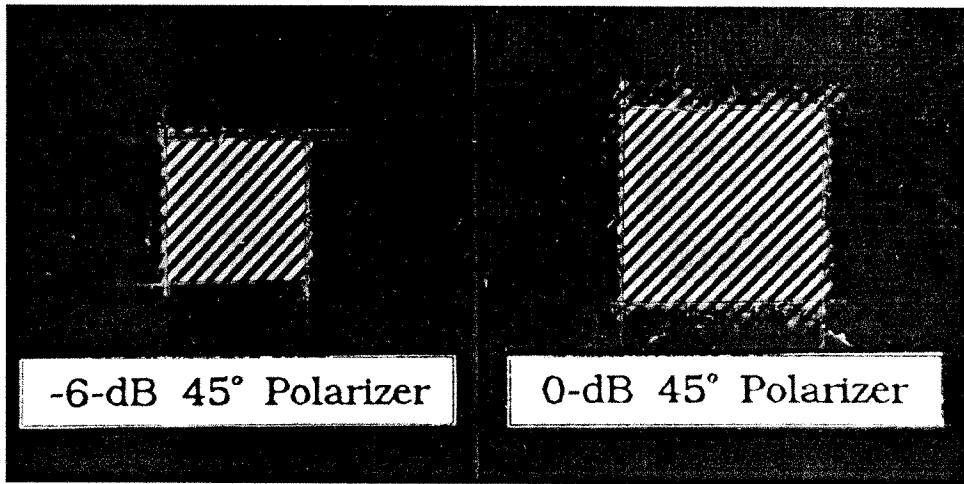


(a)

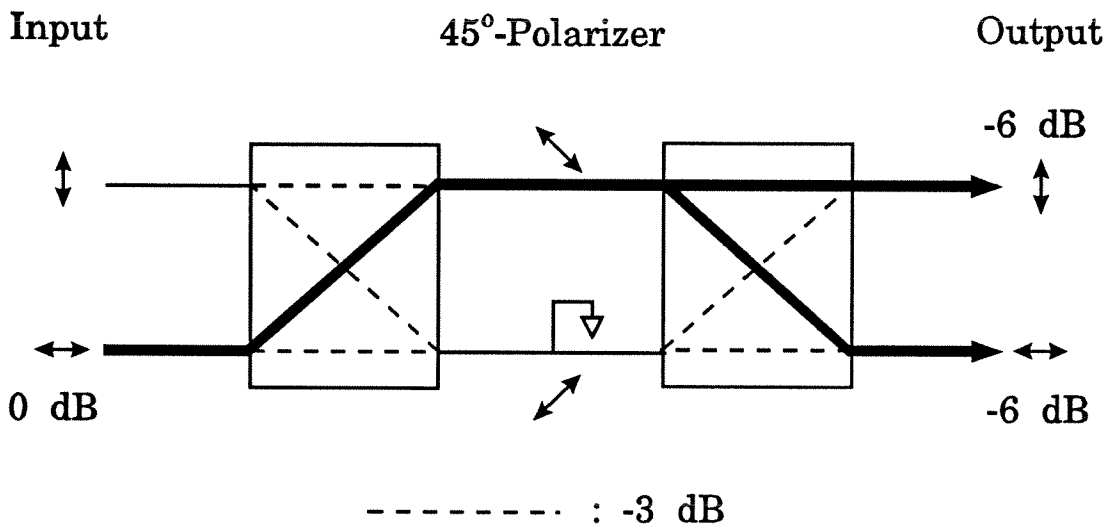


(b)

**Fig. 5.4.** (a) Setup for the far-field boundary measurement. Cross-polarized power is measured by changing the transmitting horn position. (b) Measured power versus input distance. The far-field boundary, 8.6 cm, is nearly identical to the calculation.

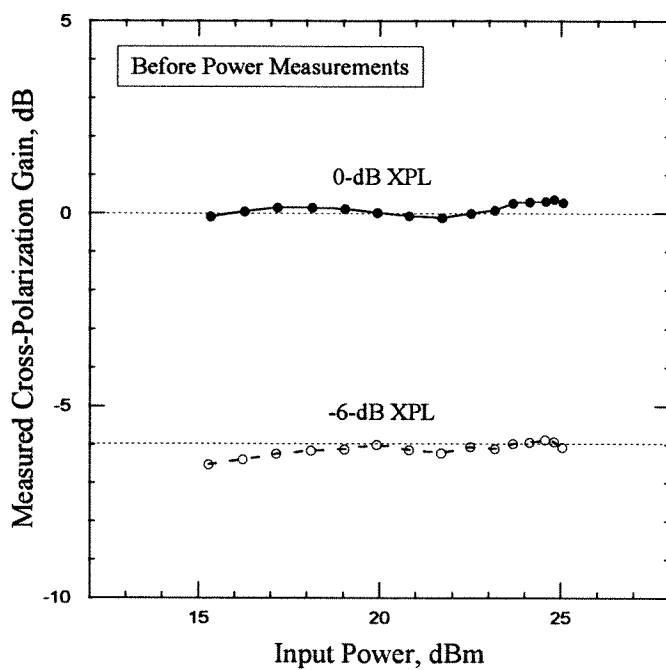


(a)

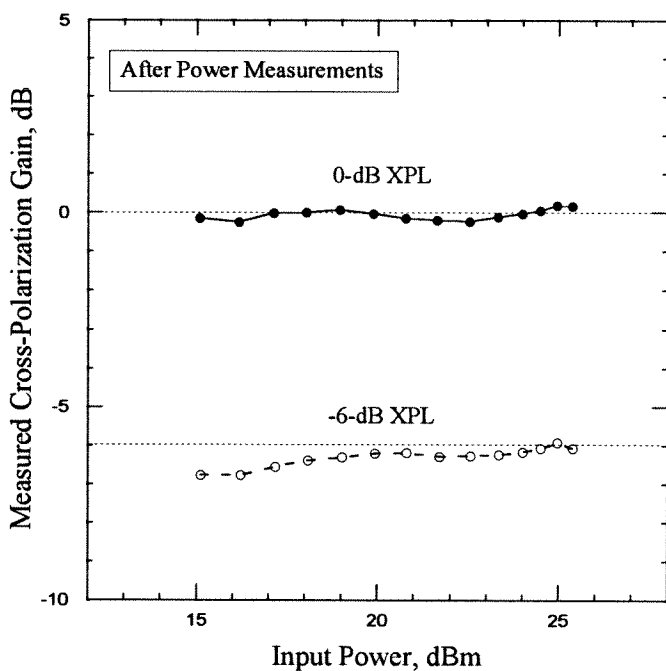


(b)

**Fig. 5.5.** (a) Photo of two 45°-polarizers. 0-dB 45°-polarizer has 16 mm on a side and the -6-dB 45°-polarizer has 11 mm on a side. The Duroid substrate has a relative dielectric constant of 2.2 and a thickness of 15 mil. (b) Signal flow for the polarization decomposition.



(a)



(b)

**Fig. 5.6.** (a) Gains versus input power for the 45°-polarizers before the power measurements.  
 (b) Gains versus input power after the power measurements.

calculated  $R_{ff}$ , as shown in Fig. 5.4.(b). As  $r_1 > R_{ff}$ , the output power is proportional to  $1/r_1^2$ . As  $r_1 < R_{ff}$ , the output power is proportional to  $1/r_1$ . The measurement agrees well with the prediction.

A further validation was provide by cross-polarized gain measurements of 45°-polarizers. A 45°-polarizer is a collection of many 45°-tilted metal strips in a square, as shown in Fig. 5.5.(a). Figure 5.5.(b) shows the signal flow for the polarization decomposition. A 0-dB horizontally polarized input is equally decomposed into a right-tilted and left-tilted 45° polarizations. Only right-tilted polarization signal passes the 45°-polarizer and results in two -6-dB outputs of vertical and horizontal polarizations. This 45° polarizer can be thought of as a -6-dB polarization divider.

From (5.6), the gain of the 45°-polarizer,  $G_{xPL}$ , is proportional to its area square, that is:

$$G_{xPL} \propto A_{xPL}^2, \quad (5.9)$$

where  $A_{xPL}$  is the area of the 45°-polarizer. A -6-dB 45° polarizer, with the same area of the grid, was measured before and after the power measurements, as shown in Fig. 5.6(a,b). A 0-dB 45°-polarizer, with twice of the grid area, was also measured as a reference. The results show that the gain errors were less than 0.5 dB for the 0-dB reference and less than 1 dB for the -6-dB reference.

#### 5.4 COMPUTATION MODELS FOR APERTURE EFFICIENCY ANALYSIS

In this section, the grid aperture efficiency is modelled and analyzed. In the far-field measurements, we assume that a grid has an effective antenna area the same as its geometric area. Aperture efficiency analysis is a validation of this assumption. The analysis is also valid for oscillator grids and other array devices with similar current distributions.

In the far-field zone, the available power density is [3]:

$$P_a = \left[ \frac{k}{4\pi} \right]^2 \times \left[ |F_\phi|^2 + |F_\theta|^2 \right] \times J_o^2 \eta_o, \quad (5.10)$$



where  $k$  and  $\eta_o$  are the free-space wave number and impedance, and  $J_o$  is the reference current of the source. The source factors,  $F_\phi$  and  $F_\theta$ , in the far-field zone are:

$$F_\phi = -\sin \phi F_x + \cos \phi F_y, \quad (5.11)$$

$$F_\theta = \cos \theta \left[ -\cos \phi F_x + \sin \phi F_y \right] - \sin \theta F_z, \quad (5.12)$$

and

$$F_\xi = \int_{-\infty}^{\infty} J_{e,\xi}(x', y', z') \cdot e^{j(k_x x' + k_y y' + k_z z')} dx' dy' dz', \quad (5.13)$$

where  $\xi = x, y$ , and  $z$ , and  $J_{e,\xi}$  is the  $\xi$ -direction normalized current with respect to  $J_o$ .

In the analysis, we assume that the currents are only in the  $y$  direction. The array factor in the  $y$  direction,  $F_y$ , can be decomposed into three array factors,  $AF_x$ ,  $AF_y$ , and  $AF_z$ . These array factors are the spatial Fourier transforms of the  $y$ -direction current components in  $x, y$ , and  $z$ , that is:

$$AF_\xi = \int_{-\infty}^{\infty} J_{e,y}(\xi) \cdot e^{jk_\xi \xi} d\xi \quad \text{with } \xi = x, y, \text{ and } z. \quad (5.14)$$

Figure 5.7 shows two models for analysis. The arrays have  $N_x$  and  $N_y$  elements along  $x$  and  $y$  directions. The periods of the unit cells are  $d_x$  and  $d_y$ . Two current distributions are discussed: uniform distribution and discrete-uniform distribution. The array factors for the uniform distribution are:

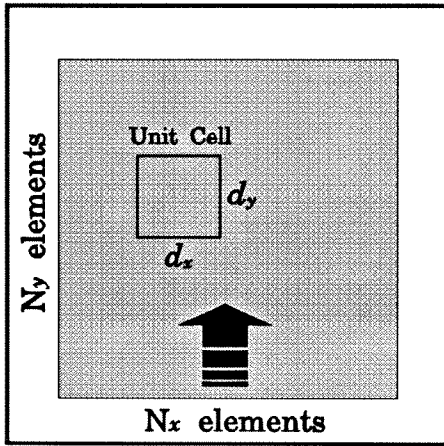
$$AF_x = \text{Sinc} \left( \frac{N_x d_x k_x}{2} \right) \quad (5.15)$$

and

$$AF_y = \text{Sinc} \left( \frac{N_y d_y k_y}{2} \right). \quad (5.16)$$

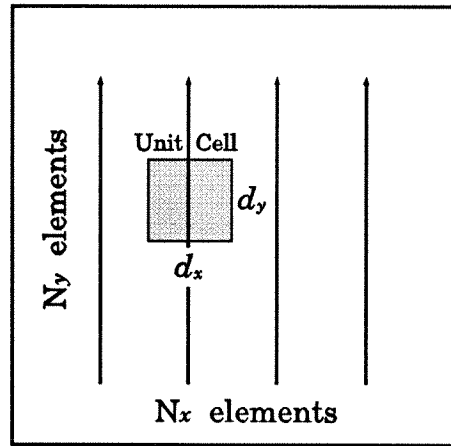
For the discrete-uniform distribution, the array factors are:

$$AF_x = \frac{1}{N_x} \frac{\sin(N_x k_x d_x / 2)}{\sin(k_x d_x / 2)} \quad (5.17)$$



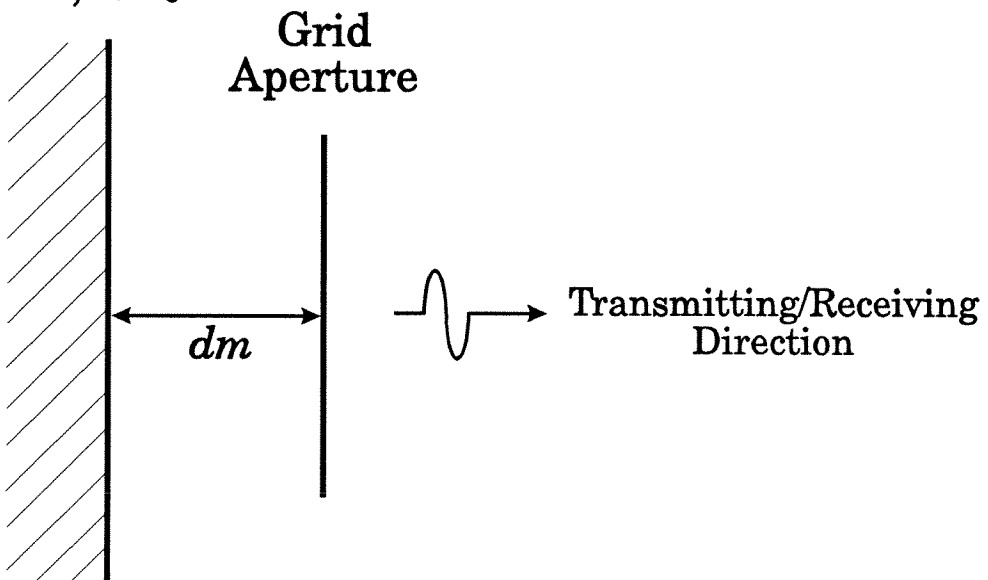
Uniform Distribution

(a)



Discrete-Uniform Distribution

(b)

Mirror,  $z=0$ 

(c)

**Fig. 5.7.** (a) Aperture with uniformly distributed current. (b) Aperture with discrete distribution along  $x$  direction and uniform distribution along  $y$  direction. (c) Sideview of the model. A mirror is  $d_m$  behind the grid aperture.

and  $AF_y$  is the same as (5.16). In the analysis, we use image currents, with opposite direction, to emulate the mirror. Hence, the  $z$ -direction array factor,  $AF_z$ , is:

$$AF_z = 2j \sin(k_z d_m), \quad (5.18)$$

where  $d_m$  is the mirror distance between the array and the mirror.

The available power density can be rewritten as:

$$P_a = \left[ \frac{k}{4\pi} \right]^2 J_o^2 \eta_o (1 - \sin^2 \phi \sin^2 \theta) |AF_x AF_y AF_z|^2. \quad (5.19)$$

The total radiation power in the far field is:

$$P_t = \int_0^{\frac{\pi}{2}} \int_0^{2\pi} P_a(\phi, \theta) \sin \theta \, d\phi \, d\theta. \quad (5.20)$$

The aperture efficiency is the ratio of effective area over geometric area of the antenna, that is:

$$\eta = \frac{A_{eff}}{A_g}. \quad (5.21)$$

The effective area can be derived from the knowledge of the available power density,  $P_a$ :

$$A_{eff} = \lambda^2 \times \frac{P_a(\theta = 0)}{P_t}. \quad (5.22)$$

## 5.5 SIMULATIONS FOR GRID APERTURE EFFICIENCIES

In the simulations, the unit cell is assumed to be a square and the grid has equal numbers of elements along  $x$  and  $y$  directions. Four arrays— $4 \times 4$ ,  $6 \times 6$ ,  $10 \times 10$ , and  $100 \times 100$ —are investigated. The results of the  $100 \times 100$  array can be good approximation for an infinite array.

### 5.5.1 APERTURE EFFICIENCY VERSUS UNIT-CELL PERIOD

Figure 5.8 shows the aperture efficiency versus unit-cell period for the uniform current distribution. The mirror distance is a quarter of the wavelength.

A grid with smaller unit cells will have higher aperture efficiency. Not surprisingly, a point source, a grid with infinitesimal unit cells, has zero geometric area resulting in an infinite aperture efficiency.

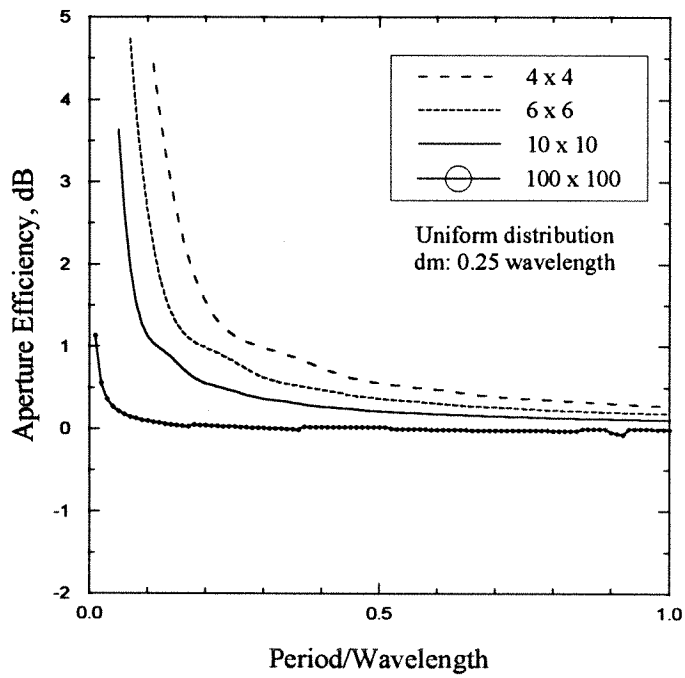
Figure 5.9 shows the aperture efficiency versus unit-cell period for the discrete-uniform current distribution. Similarly, a grid with smaller unit cells will have higher aperture efficiency. Unlike the uniform-distribution aperture, the aperture efficiency in this case rolls below 0 dB because more significant side lobes enter visible range of angles as unit cells get larger.

Figure 5.10(a,b) show the aperture efficiencies of both current distributions with a mirror distance of 0.625 wavelength. Rippled variations of aperture efficiencies result from the mirror. The aperture efficiencies have considerable peaks of 4 dB at larger periods.

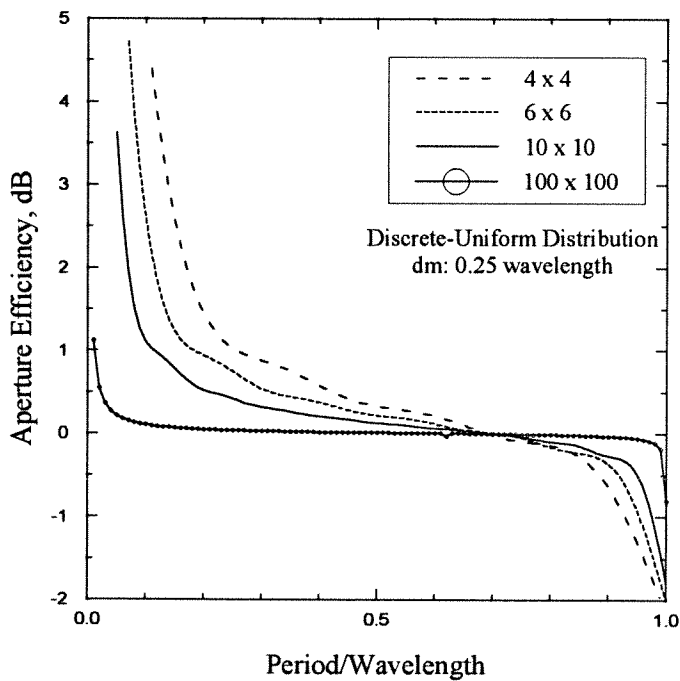
### 5.5.2 APERTURE EFFICIENCY VERSUS MIRROR DISTANCE

The monolithic grid discussed in Chapter 4 has a unit-cell period of 1.9 mm. The aperture efficiencies for this unit cell are plotted with four grid sizes, as shown in Fig. 5.11. The mirror modulates the radiation pattern and results in repeatable fin-shape curve with a period of half wavelength. Figure 5.12(a,b) show four H-plane radiation patterns at mirror positions of 0.1, 0.6, 1.1, and 1.6 wavelengths. The corresponding aperture efficiencies are 1.1, 1.8, 2.8, and 2.4 dB, and are not periodical.

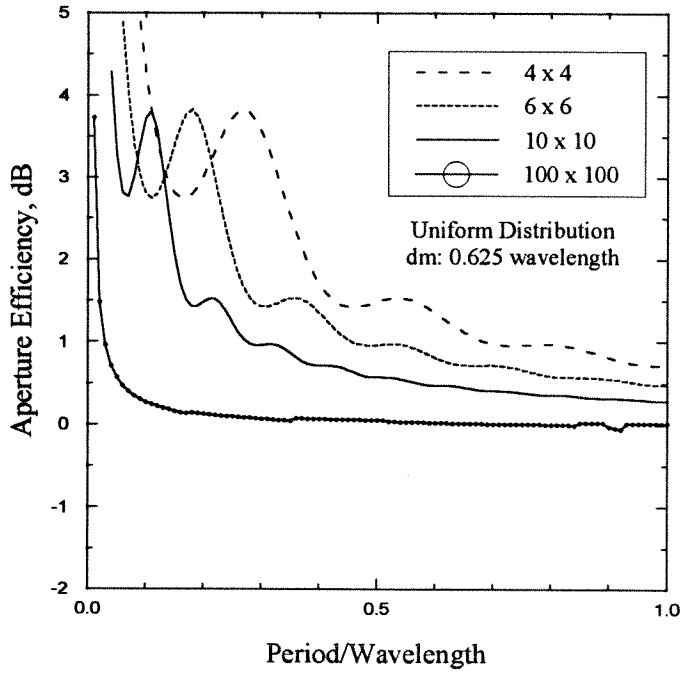
The input and output aperture efficiencies of the grids discussed in Chapter 2 and 4 are illustrated in Table 5.1. The input mirror distance is determined by the output polarizer position and by the dielectric layer(s) between output polarizer and the amplifier grid (Fig. 2.5). Similarly, the output mirror distance is determined by the input polarizer position and by the dielectric layer(s) and air spacings between output polarizer and the grid. Total aperture efficiency is the product of the input and output efficiencies. For the 10-GHz hybrid grid, the total aperture efficiency is 0.9 dB. That is, we overestimate the gain by 0.9 dB.



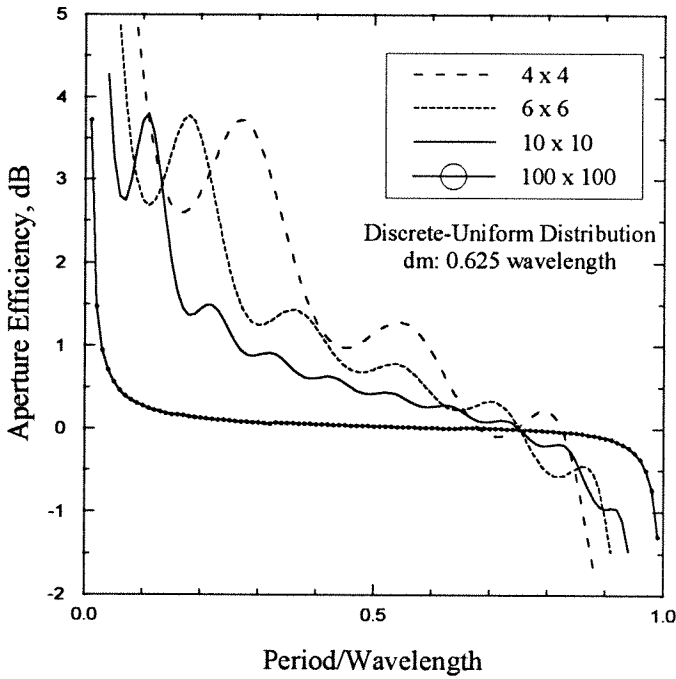
**Fig. 5.8.** Aperture efficiency versus unit-cell period for the uniform aperture with a mirror distance of  $0.25\lambda$ .



**Fig. 5.9.** Aperture efficiency versus unit-cell period for the discrete-uniform aperture with a mirror distance of  $0.25\lambda$ .



(a)



(b)

**Fig. 5.10.** (a) Aperture efficiency versus unit-cell period for the uniform aperture with a mirror distance of  $0.625 \lambda$ . (b) Aperture efficiency versus unit-cell period for the discrete-uniform aperture with a mirror distance of  $0.625 \lambda$ .

	Hybrid Grid	Monolithic Grid
Grid Size	4×4	6×6
Operating Frequency	10 GHz	40 GHz
Unit Cell Period	8 mm	1.9 mm
Input Mirror Distance	$0.87 \lambda_o$	$0.85 \lambda_o$
Input Aperture Efficiency	1.7 dB	−0.5 dB
Output Mirror Distance	$0.77 \lambda_o$	$0.81 \lambda_o$
Output Aperture Efficiency	−0.8 dB	0.2 dB
Total Aperture Efficiency	0.9 dB	−0.3 dB

Table 5.1. Aperture efficiencies for the hybrid and monolithic grid amplifiers.

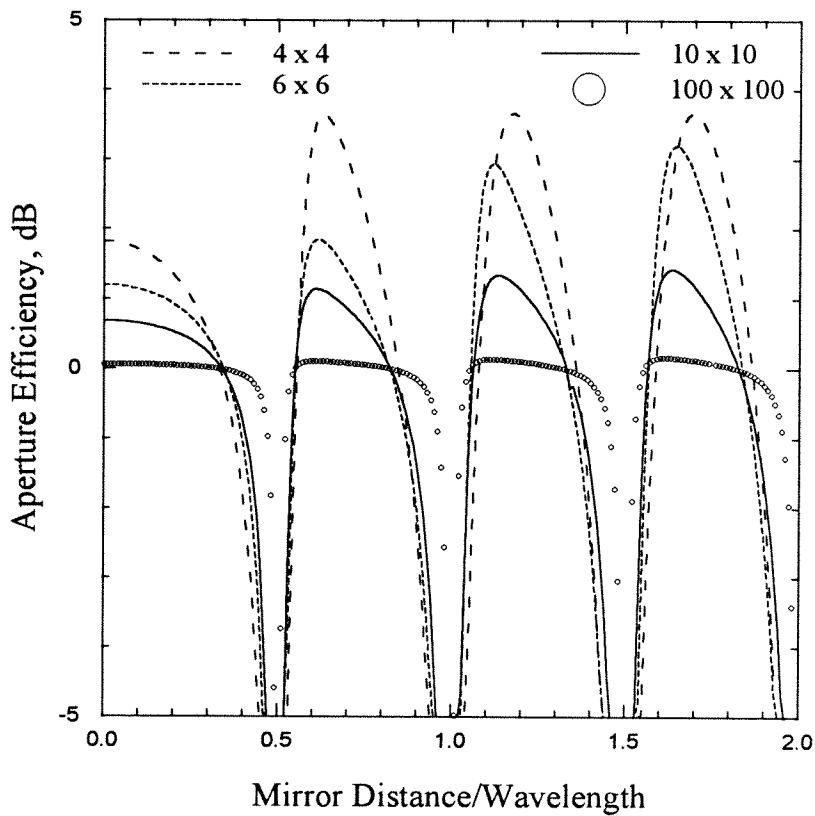
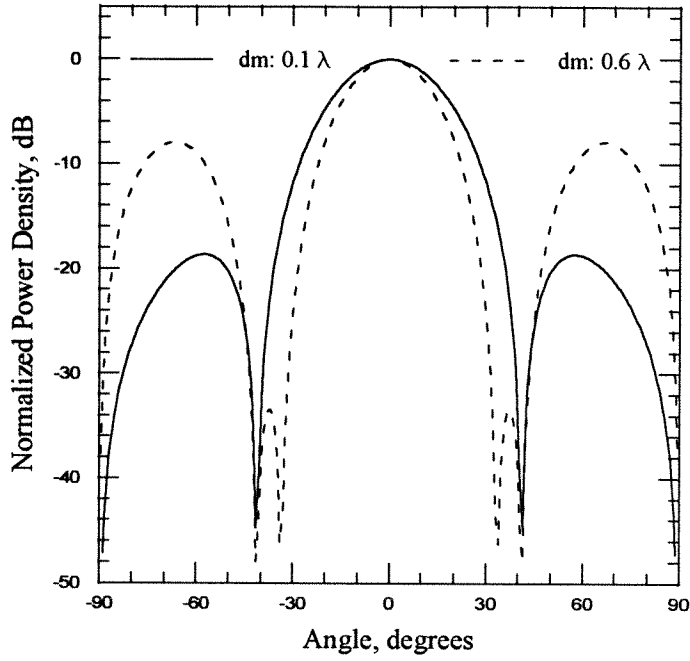
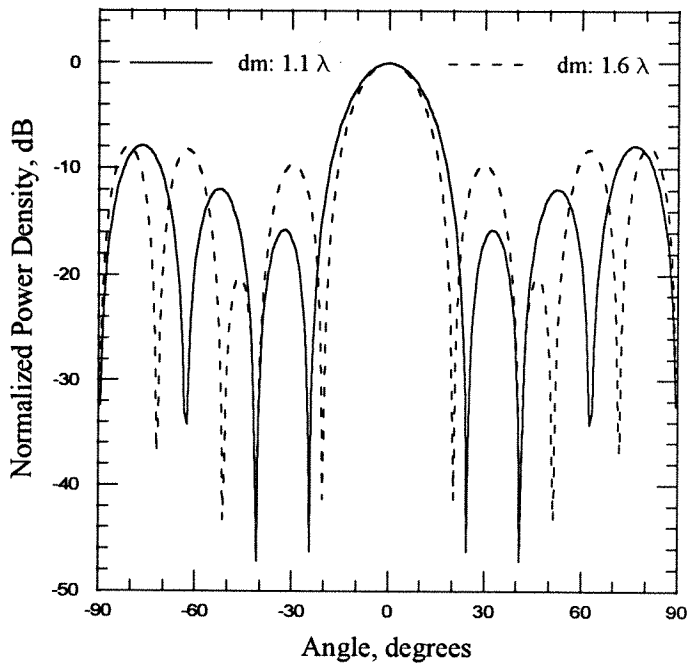


Fig. 5.11 Aperture efficiency versus mirror distance for the discrete-uniform aperture with a unit-cell period of  $0.25 \lambda$ , the cell size of the monolithic grid amplifier.



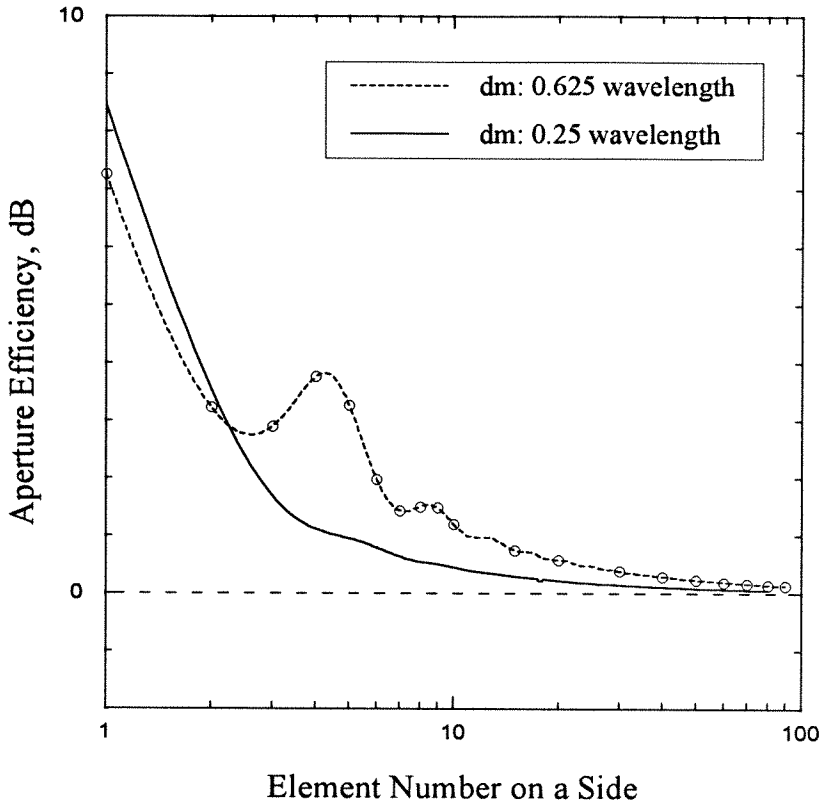
(a)



(b)

**Fig. 5.12.** H-plane radiation patterns at mirror distances of  $0.1 \lambda$  (a, solid),  $0.6 \lambda$  (a, dashed),  $1.1 \lambda$  (b, solid), and  $1.6 \lambda$  (b, dashed).





**Fig. 5.13.** Aperture efficiency versus array size for the uniform aperture with a unit-cell period of  $0.25 \lambda$ .

For the 40-GHz monolithic grid, the total aperture efficiency is  $-0.3$  dB. That is, we underestimate the gain by  $0.3$  dB.

These simulation results are based on a simple current distribution, the discrete-uniform distribution. More sophisticated and precise predictions of grid current distribution may be derived from HFSS simulation [4]. Table 5.1 can be treated as a preliminary validation of the assumption that a grid has an effective antenna area the same as its geometric areas.

### 5.5.3 APERTURE EFFICIENCY VERSUS ARRAY SIZE

Figure 5.13 shows the aperture efficiency at 40 GHz as a function of array size for the grid with unit-cell period of  $1.9$  mm. For a small array, the mirror distance significantly affects the aperture efficiency.

## References

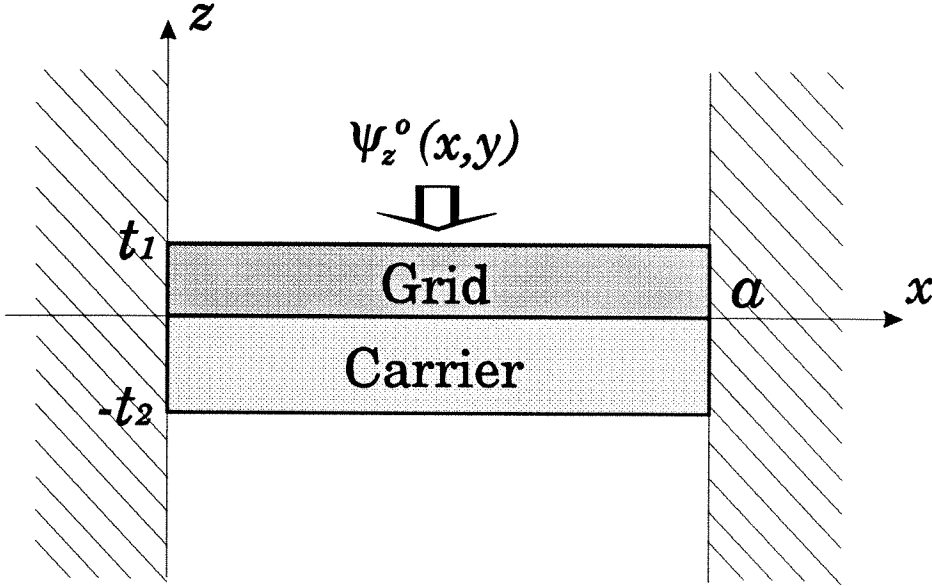
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- [2] J.D. Kraus, *Antennas*, second ed., McGraw-Hill Book Co., New York, 1988, pp. 48–61.
- [3] R.E. Collin, "Chapter 4: Aperture-Type Antennas," *Antennas and Radiowave Propagation*, McGraw-Hill Book Co., New York, 1985.
- [4] "HP 85180A High Frequency Structure Simulator," Hewlett-Packard, Networks Measurements Division, Santa Rosa, CA.

## Chapter 6

# High-Power Millimeter-Wave Amplifiers

In 1991, Moonil Kim demonstrated the first quasi-optical amplifier—a 25-element MESFET grid amplifier [1]. Two full-size 100-element grids, using HBT's and pHEMT's, soon followed [2,3]. Gain and stability models for grid amplifiers have been presented and experimentally verified, using hybrid technology [3,4]. Recently, two successful monolithic grid amplifiers have been reported [5,6]. These efforts show that the grid-amplifier approach, using monolithic technology, is possible at millimeter waves.

Very recently, ARPA has announced a major new initiative for high-power millimeter-wave amplifiers. The monolithic quasi-optical amplifier is a very promising approach to this target. A new project, a cascade quasi-optical amplifier system, has been initiated by Emilio Sovero and Aiden Higgins at Rockwell Science Center. The future work is to optimize the design to improve the efficiency and to drive a monolithic grid amplifier with a power density of 5 W per square centimeter. By tiling four grids on a bulk carrier, we can achieve a 20-W grid amplifier. The critical issue for the high-power amplifier is the thermal issue. This chapter examines thermal performance of the high-power grid amplifier. Suggestions to improve the existing monolithic grid amplifier and approaches to develop a quasi-optical amplifier system are also discussed.



**Fig. 6.1.** Two-layer configuration for thermal analysis. The top layer is the grid substrate and bottom layer is the carrier.

## 6.1 THERMAL EXAMINATION

Overheating problems have been encountered in the measurements of power grids [3,7]. In the measurements of monolithic grids, small area and high DC dissipation result in considerable temperature rise on the transistors. The thermal issue turns to be a critical issue in designing high-power millimeter-wave amplifiers. A carrier with high thermal conductivity can solve the overheating problem [8]. This section uses a thermal model with a two-layer structure to examine the possible temperature rise for the amplifiers. This thermal model is similar to the one in [8], but in addition it takes into account the finite thermal conductivity of the carrier.

### 6.1.1 THERMAL MODELLING

The steady-state temperature distribution  $T(x, y, z)$  in the substrate must satisfy Laplace's equation [9]:

$$\nabla^2 T(x, y, z) = 0. \quad (6.1)$$

The vector heat flux  $\vec{\psi}(x, y, z)$  is related to this temperature distribution by the material's thermal conductivity,  $k$ , by:

$$\vec{\psi}(x, y, z) = -k \nabla T(x, y, z). \quad (6.2)$$

Figure 6.1 shows the configuration for the analysis. The grid has a thickness of  $t_1$  and a thermal conductivity of  $k_1$  and is mounted on a dielectric carrier, with a thickness of  $t_2$  and a conductivity of  $k_2$ . The dimensions of the cross section are  $a$  and  $b$  in the  $x$  and  $y$  directions, respectively. The heat is generated by the DC dissipation on the surface of the grid. Presumably, the heat is conducted through the carrier to the lateral heat sink. Boundary conditions are imposed by the zero normal heat flux on the carrier back ( $z = -t_2$ ) and zero temperature rise on the heat sink. The following expressions are solutions of (6.1) and satisfy the specified boundary conditions, for the grid substrate, i.e.,  $z > 0$ :

$$T_1(x, y, z) = \sum_{m=1}^{\infty} \sum_{n=1}^{\infty} T_{1,mn} \sin(\alpha_m x) \sin(\beta_n y) [e^{\gamma_{mn} z} + A_{mn} e^{-\gamma_{mn} z}], \quad (6.3)$$

where:

$$\alpha_m = \frac{m\pi}{a}, \quad \beta_n = \frac{n\pi}{b}, \quad \text{and} \quad \gamma_{mn} = \sqrt{\alpha_m^2 + \beta_n^2}. \quad (6.4)$$

For the carrier,  $z \leq 0$ :

$$T_2(x, y, z) = \sum_{m=1}^{\infty} \sum_{n=1}^{\infty} T_{2,mn} \sin(\alpha_m x) \sin(\beta_n y) \frac{\cosh(\gamma_{mn}(z + t_2))}{\sinh(\gamma_{mn} t_2)}. \quad (6.5)$$

The boundary condition at the interface,  $z = 0$ , is:

$$k_1 \frac{\partial T_1}{\partial z} \Big|_{z=0} = k_2 \frac{\partial T_2}{\partial z} \Big|_{z=0} = \frac{(T_1 - T_2)}{R_{th}} \Big|_{z=0}, \quad (6.6)$$

where  $R_{th}$  is the thermal resistance for the junction. Solving for  $A_{mn}$  and  $T_{2,mn}$ , we have:

$$A_{mn} = \frac{F - 1}{F + 1} \quad \text{with} \quad F = \frac{k_1}{k_2} [ R_{th} k_2 \gamma_{mn} + \coth(\gamma_{mn} t_2) ], \quad (6.7)$$

and

$$T_{2,mn} = \frac{k_1}{k_2} (1 - A_{mn}) T_{1,mn}. \quad (6.8)$$

The excitation is characterized by the power dissipation on the front surface. The heat flux at the surface,  $z = t_1$ , is the power density of DC dissipation. In the thermal model, the heat flux is:

$$\psi_z^o(x, y) = k_1 \left. \frac{\partial T_1}{\partial z} \right|_{z=t_1},$$

that is,

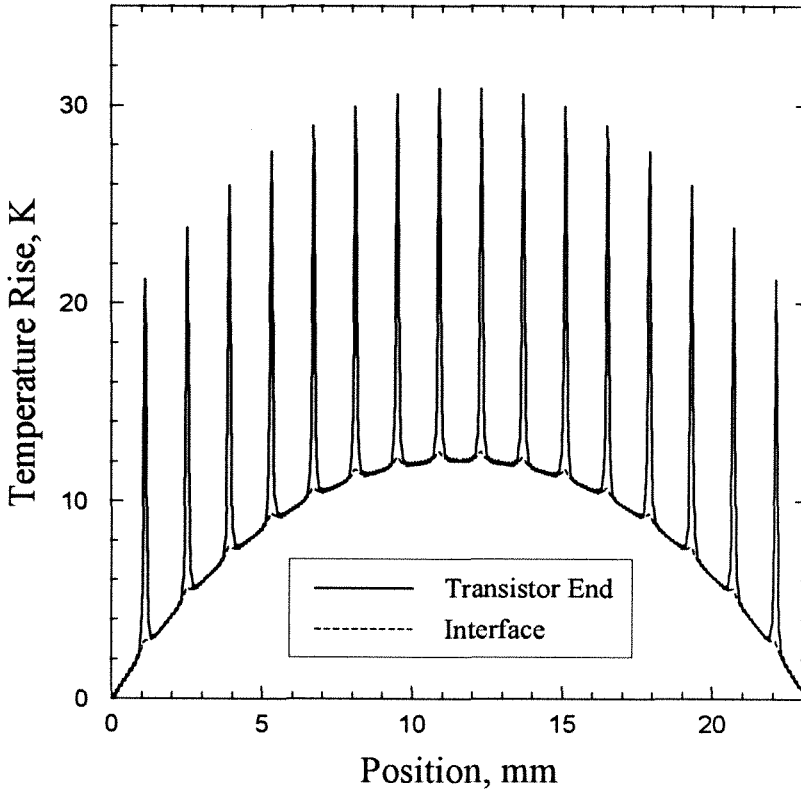
$$\psi_z^o(x, y) = k_1 \sum_{m=1}^{\infty} \sum_{n=1}^{\infty} T_{1,mn} \gamma_{mn} \sin(\alpha_m x) \sin(\beta_n y) (e^{\gamma_{mn} t_1} - A_{mn} e^{-\gamma_{mn} t_1}). \quad (6.9)$$

Solving for  $T_{1,mn}$ , we get:

$$T_{1,mn} = \frac{4}{k_1 a b \gamma_{mn} (e^{\gamma_{mn} t_1} - A_{mn} e^{-\gamma_{mn} t_1})} \times \int_0^a \int_0^b \psi_z^o(x, y) \sin(\alpha_m x) \sin(\beta_n y) dx dy. \quad (6.10)$$

	Thermal Cond. (W/m/°K)	Peak Temp. Rise (°K)
Diamond	1000 [10]	31
Aluminum Nitride	170 [11]	87
Gallium Arsenide	46 [12]	235
Duroid	0.4 [13]	1057

**Table 6.1** Peak temperature rises of diamond, AlN, GaAs, and Duroid as a carrier for the 20-W power grid.

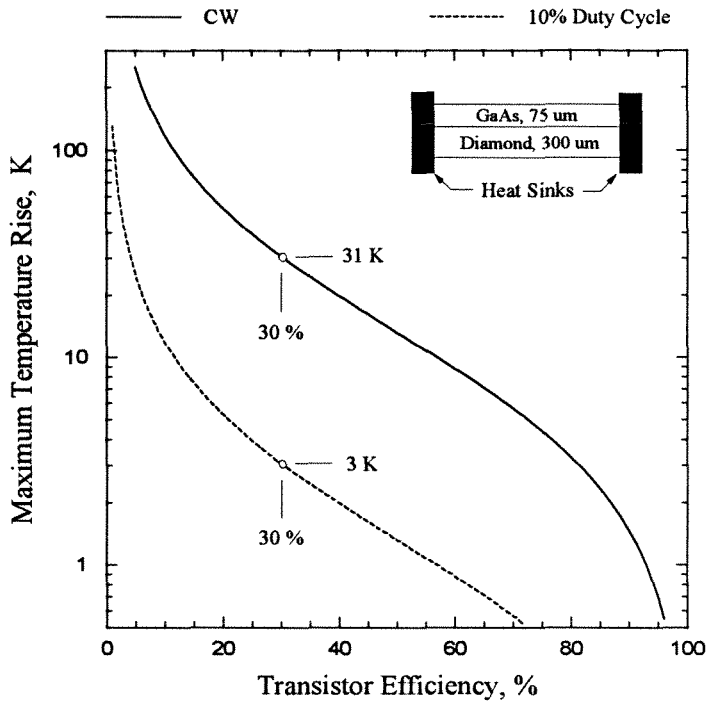


**Fig. 6.2.** Profile of temperature rise on the center row of the grid.

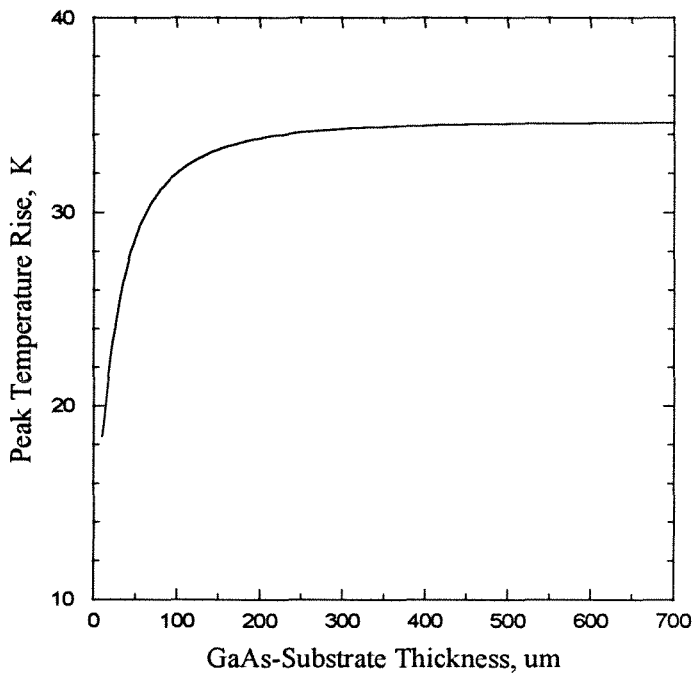
#### 6.1.2 THERMAL SIMULATIONS FOR A 20-W $16 \times 16$ TILED GRID

The second-generation monolithic grid amplifier suggested in Sec.6.2 has a 20-W output with a transistor efficiency of 30%. Totally, we have 46.7 W DC dissipation for the whole grid. The corresponding heat flux is modelled by 256 periodic sources of 182 mW on a square with  $100 \mu\text{m}$  on a side. In the simulation, the GaAs-substrate is  $75 \mu\text{m}$  thick and attached on a  $300\text{-}\mu\text{m}$  carrier. The thermal resistance of the attachment,  $R_{th}$ , is assumed zero.

Table 6.1 shows a comparison of peak temperature rises of four carriers—diamond, AlN, GaAs, and Duroid. Diamond, with a peak temperature rise of  $31^\circ\text{K}$ , is a good candidate for the carrier. Based on the thermal simulation, the maximum temperature rise per DC dissipation power is  $23.4^\circ\text{K/W}$  without the carrier and  $0.66^\circ\text{K/W}$  with the diamond carrier. Figure 6.2 shows the tempera-

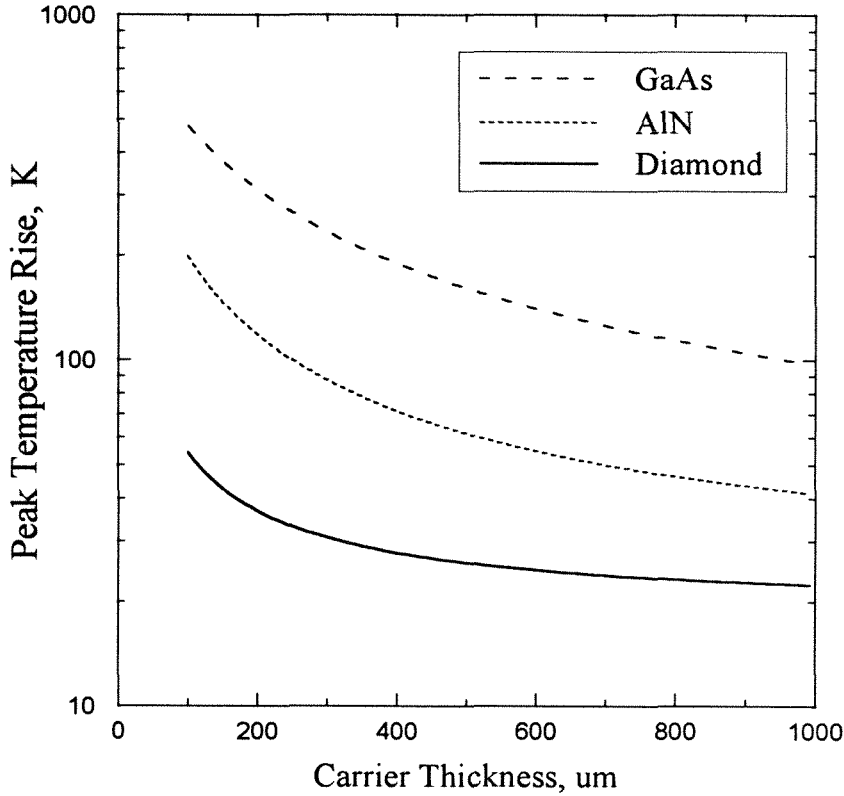


**Fig. 6.3.** Peak temperature rise versus transistor efficiency. The solid line is for the continuous-wave operation and the dashed line is for the pulse-mode operation with a duty cycle of 10%.



**Fig. 6.4.** Peak temperature rise versus GaAs thickness.





**Fig. 6.5.** Peak temperature rise versus carrier thickness for GaAs, AlN, and diamond carriers.

ture rise on the center rows of the grid and the attachment junction. Reasonably, the peak temperature rises occur at the center transistors. In this simulation, about 99% of the heat flux is conducted through the diamond carrier to the heat sink on the sides.

The peak temperature rise as a function of transistor efficiency is plotted in Fig. 6.3. Even with a diamond carrier, poor transistor efficiency still results in an intolerable temperature rise.

Figure 6.4 shows the peak temperature rise versus the thickness of GaAs substrate. This plot offers a reference to determine the thickness of the GaAs substrate. The temperature rise is lower for a thinner GaAs substrate. However, it will be difficult to manipulate an amplifier grid with a very thin substrate.

The electrical effect of the carrier and GaAs substrate should be compensated by tuning components.

Figure 6.5 shows the peak temperature rises versus the thickness of the carrier for the diamond, AlN, and GaAs. For the thick carrier, with  $t_2 = 1$  mm, AlN has a peak temperature rise of 41°K and diamond has a peak of 22°K. Both of them can be good candidates for the carrier. However, for the thin carrier, with  $t_2 = 100$   $\mu$ m, AlN has a considerable peak rise of 200°K. Hence, diamond, with a peak rise of only 54°K, appears to be the only choice for the 100- $\mu$ m carrier.

For the monolithic grid discussed in Chapter 4, poor efficiency and lack of a heat removal mechanism limit the power performance and caused difficulties in the measurements. Because of high power dissipation and small area, the thermal performance plays an important role for quasi-optical power amplifiers. Choosing an appropriate thermal carrier, determining the proper thicknesses of the GaAs substrate and the carrier, and a reliable estimating transistor efficiency turn out to be important issues in designing the second-generation monolithic power grid amplifier.

## 6.2 APPROACH TO A HIGH-POWER AMPLIFIER

The existing HBT grid has an output power of 670 mW and does not suffer from parasitic oscillation. However, the power-added efficiency is only 4% and this limits the output power, and forces us to operate the amplifier in a pulse of 0.6 second. To achieve higher power capability in the second-generation grid, three approaches are suggested to improve power capability and thermal performance of the existing monolithic grid.

### 6.2.1 IMPROVING POWER CAPABILITY

Higher power capability can be achieved by two modifications on the existing grid. The first modification is to shrink the unit cell. A smaller unit cell results

in higher power density, that is, higher power for a fixed area. A monolithic grid amplifier with smaller unit-cell period has been proven possible [6]. The existing  $6 \times 6$  grid has a unit cell of 1.9 mm on a side. A unit cell of 1.4 mm is suggested and can improve the output power of the grid by 2.5 dB. The new grid will have 8 elements on a side.

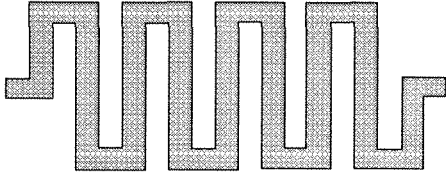
The second modification is to use 100-mW pHEMT's as active devices. The active devices of the existing grid are 20-mW HBT's with maximum available gain of 10 dB at 35 GHz. The substitute pHEMT can greatly increase the output power. Moreover, the new grid is expected to have higher gain because of the higher inherent gain of the pHEMT's. The new pHEMT grid will need two individual biases. This makes it possible to optimize the transistor efficiency.

### 6.2.2 IMPROVING THERMAL PERFORMANCE

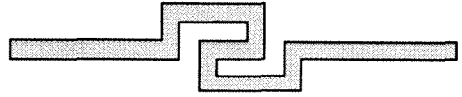
Two approaches can solve the thermal problem of the high-power amplifier. The first approach is to reduce the heat by improving the efficiency of the grid amplifier. For the existing monolithic grid, 73% of the DC power is dissipated in the bias circuit, including the bias lines (38%) and emitter resistors (35%). In the existing grid, the bias-line resistance is 15  $\Omega$ . Bias-line resistance can be reduced by making a thicker second metallization. A further improvement is to replace the meandering lines by hairpin bias lines (Sec. 2.3.2). The hairpin lines will reduce the effective lengths of the bias lines by a factor of three thus reducing the bias-line resistance. The comparison is shown in Fig. 6.6. On the other hand, the large emitter resistor also limits the efficiency of the monolithic grid amplifier. We believe we can reduce the emitter resistance from 150  $\Omega$  to 25  $\Omega$ . Stability simulations predict the grid will be still stable with the smaller emitter resistance.

The second approach to solve the thermal problem is to provide the grid with a good heat sink. The heat sink should not affect the RF behavior of the grid. This could be achieved by attaching the grid to a carrier with high thermal

## Meandering Line



## Hairpin Line



**Fig. 6.6.** Comparison of meandering and hairpin bias lines.

conductivity. Diamond is a good candidate for the carrier. Based on the thermal simulation in Sec. 6.1, the peak temperature rise with a diamond carrier is only 2.8% of the peak temperature rise without any carrier. A peak temperature rise of 31°K is predicted for the 20-W 16×16 tiled grid with transistor efficiency of 30%.

### 6.2.3 TILING TECHNOLOGY

The power capability of the grid amplifier is proportional to the number of unit cells. It is possible to enhance grid power capability by tiling several monolithic grids in an array format. The pHEMT grid will have higher input impedance and less sensitivity to the matching conditions. This makes it possible to achieve higher power using tiling technology. A quasi-optical amplifier with 20-W output power can be achieved by tiling four 5-W grids on a bulk carrier in a 2-by-2 array format. Table 6.2 shows the comparison of the existing and suggested grid amplifiers.

### 6.3 A CASCADE QUASI-OPTICAL AMPLIFIER SYSTEM

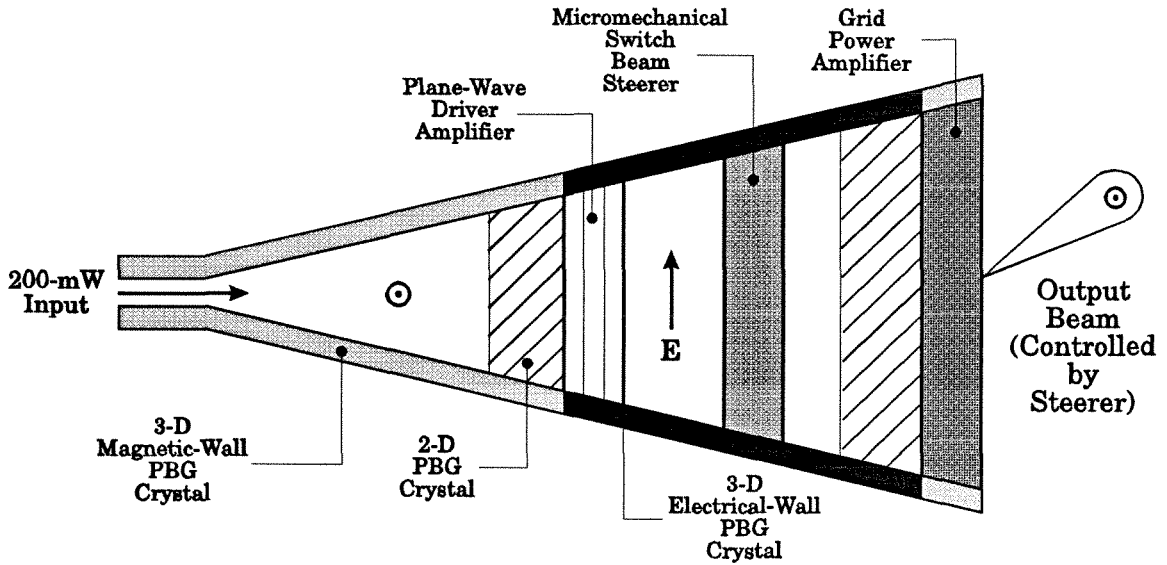
Figure 6.7 shows the cascade amplifier system with beam steering capability. A 200-mW input with horizontal polarization is fed from the waveguide. A steered 20-W output with the same horizontal polarization is radiated into free space. The first stage is the driver amplifier, a plane-wave amplifier [14,15]. The

	Current HBT Grid	Proposed pHEMT Grid
Operating Frequency	40 GHz	35 GHz
Number of Unit Cells	36	256
Cell Dimension	1.9 mm	1.4 mm
Peak Gain	5 dB	$\geq 6$ dB
Output Power	670 mW	20 W
Max. Temperature Rise	$> 100^\circ\text{K}$	$31^\circ\text{K}$
Heat Sink	None	Diamond
Substrate Thickness	$560\ \mu\text{m}$	$75\ \mu\text{m}$
Bias Line Type	Meandering	Hairpin
2nd Metal Thickness	$3\ \mu\text{m}$	$10\ \mu\text{m}$
Bias Resistance	$150\ \Omega$	$25\ \Omega$
Transistor Efficiency	27 %	$\geq 30$ %
Transistor Current	15 mA	$\geq 20$ mA
Operation Mode	Pulse	CW

Table 6.2. Comparison of the existing HBT and suggested pHEMT grid amplifiers.

driver amplifier has a power gain of 14 dB. The intermediate stage is a micromechanical switch beam steerer. An electrically controlled multi-layer beam steerer can create a  $360^\circ$  phase shift for steering purposes [16]. A 2-dB loss is predicted for the beam steerer stage. The last stage is the power amplifier with a power gain of 8 dB and an output power of 20 W. The 20-W power amplifier can be achieved by tiling four  $8 \times 8$  5-W grid amplifiers.

Recently, Ivonov and Mortazawi have demonstrated a two-stage spatial amplifier with hard horn antennas [17]. The hard horn has a dielectric lining on the two sidewalls that gives the effect of a magnetic wall. A nearly uniform power distribution across the guide improved the power gain by about 5 dB. An alternative approach to a magnetic wall, the photonic-band-gap crystal [18,19], will be also used in the amplifier system.



**Fig. 6.7.** A cascade amplifier system. The input power is 200 mW with horizontal polarization. The output power is 20-W and steered electrically by the beam steerer. The system is surrounded by Photonic-Band-Gap (PBG) crystals with the proper orientations.

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