INVESTIGATIONS ON SCHOTTKY BARRIER STRUCTURES IN COMPOUND SEMICONDUCTORS:

I. HgTe on CdTe: A Lattice-Matched Schottky Barrier
II. Au-Cd Barriers to CdTe
III. Au Barriers on $In_xGa_{1-x}P$

Thesis by

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TO MY PARENTS

TO DEE

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ABSTRACT

i) The Au Schottky barrier height to n - $In_xGa_{1-x}P$ was measured as a function of alloy composition. The Au barrier, ϕ_p, to p-$In_xGa_{1-x}P$ was found to be independent of composition. The barrier, ϕ_p, was determined by the relation $\phi_p + \phi_n = \phi_g$ where ϕ_g is the band gap energy and ϕ_n is the measured barrier height to n-$In_xGa_{1-x}P$. It has been observed that the Au barrier height to p-type material for most compound semiconductors is determined by the anion. This dependence on the anion of the compound has now been seen to extend to the alloy system $In_xGa_{1-x}P$ measured here.

ii) The Schottky barrier height of Cd, Au, and Au-Cd alloys was determined on vacuum cleaved surfaces of n-CdTe. A large barrier of 0.92 eV was found in the case of the Au-Cd alloy contacts. Contacts made with elemental Cd or Au gave barrier heights of 0.45 and 0.65 eV, respectively. The increased barrier height found on Au-Cd alloy contacts may be related to recent UHV observations on Schottky barrier formation where crystal defects play a role in determining the observed barrier height.

iii) HgTe-CdTe lattice matched heterojunctions were formed by the epitaxial growth of HgTe on CdTe substrates using a new low temperature metal organic chemical vapor deposition (MOCVD) technique. These heterojunctions combine features of the Schottky barrier structure, due to the high carrier concentrations found in the semi-

metallic HgTe, with the structural perfection present in a lattice matched heterojunction. The measured Schottky barrier height varied from 0.65 to 0.90 eV depending on the details of the HgTe growth procedure used. Two models of the HgTe-CdTe heterojunction are presented which account for the observed variation in barrier height.

Parts of this thesis have been previously presented in the following publications:

1. "Compositional Dependence of Schottky Barrier Heights for Au on Chemically Etched $In_xGa_{1-x}P$ Surfaces", T. F. Kuech and J. O. McCaldin, J. Vac. Sci. Technol. (1980), 17, p. 891; also presented at the Seventh Conference on the Physics of Compound Semiconductor Interfaces, Estes Park, Colorado, January, 1980.

2. "Low-Temperature CVD Growth of Epitaxial HgTe on CdTe", T. F. Kuech and J. O. McCaldin, to be published J. Electrochemical Society; also presented at the Electronic Materials Conference, Cornell University, Ithaca, New York, June, 1980.

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PREFACE

The field of metal semiconductor interfaces and semiconductor heterojunctions is rich in physical phenomena. This thesis represents what the author hopes will be a contribution to the understanding of such phenomena. Of the work undertaken during the author's stay at Caltech, it is this work that is most fitting for a thesis presentation. Other research efforts undertaken during the four-year residence have been focused on the development of techniques for crystal growth on amorphous or inert substrates. These techniques involve the fabrication and use of thin liquid films which serve as the crystal growth medium. This work, while in an early stage of development, shows promise as a method of producing single crystal or controlled polycrystalline large grain semiconductor materials. This work to date has been presented in the two publications listed below.

"Confining Substrates for Micron-Thick Liquid Films", T. F. Kuech and J. O. McCaldin, Applied Physics Letters, (1980), 37, p. 44.

"Stability and Pinning Points in Substrate Confined Liquids", J. O. McCaldin and T. F. Kuech, to be published, J. Applied Physics.

The author has also studied, in collaboration with M. Maenpaa, S. S. Lau, and M. A. Nicolet the heteroepitaxial growth of Ge on Si

substrate by use of vacuum deposition and CVD techniques. This work is currently in progress (2/81).

CHAPTER 1

INTRODUCTION AND REVIEW OF FUNDAMENTALS

A. INTRODUCTION

The interface between a metal and semiconductor is one of great technological importance in the fabrication of electronic semiconductor devices. The metal-semiconductor structure can serve as the electrical contact to a device as in an ohmic contact or as part of the active device itself as in metal-insulator field effect transistors and Schottky barrier devices. Devices based on Schottky barrier structures perform in a wide variety of applications. Schottky barriers are used in metal semiconductor field effect transistors (MESFETS), power diodes, clamped TTL logic, and solar cells, to name only a few of their uses.

Schottky barriers have been the subject of many theoretical and experimental investigations. Despite the magnitude of the research effort expended in the area of Schottky barriers, there is still a lack of understanding concerning the physics of Schottky barrier formation. It is to a better understanding of Schottky barriers on compound semiconductors that this thesis is directed.

The thesis consists of three experimental studies. The first study concerns itself with the compositional dependence of Au Schottky barriers on chemically prepared surfaces of $In_xGa_{1-x}P$. The second work deals with the use of Au-Cd alloys to achieve higher barrier heights on CdTe. The third work investigates the Schottky barrier-like structure formed by the epitaxial growth

of the semimetal HgTe on the semiconductor CdTe.

B. SCHOTTKY BARRIERS: Simple Models and Experimental Observation

The first published observation of a rectifying metal-semiconductor junction was recorded by Braun in 1874 [1]. It was not until 1938, however, that the first theoretical attempts at explaining the phenomena were made by Schottky [2] and Mott [3]. The Schottky-Mott theory explains the presence of the electrostatic barrier which causes the rectifying behavior as resulting from the difference in the electron affinity of the two materials.

The formation of a Schottky barrier in the Schottky-Mott theory can be illustrated by the following "gedanken" experiment. The metal and semiconductor, when considered separately, are characterized by a work function, ϕ, and electron affinity, χ, as shown in Fig. 1.1. The common case of an n-type semiconductor whose workfunction ϕ_{sc} is less than the metal workfunction is illustrated here. Other possible situations leading to ohmic and rectifying contacts are shown in Fig.1.2.

Thermodynamic equilibrium is achieved when the Fermi level of the metal and semiconductor coincide. This is accomplished by allowing electrons to be transferred between the two materials by, perhaps, a wire connecting the two materials. As the two materials are then brought together, electrons in the conduction band of the semiconductor are transferred to the lower energy states in the metal. The transfer

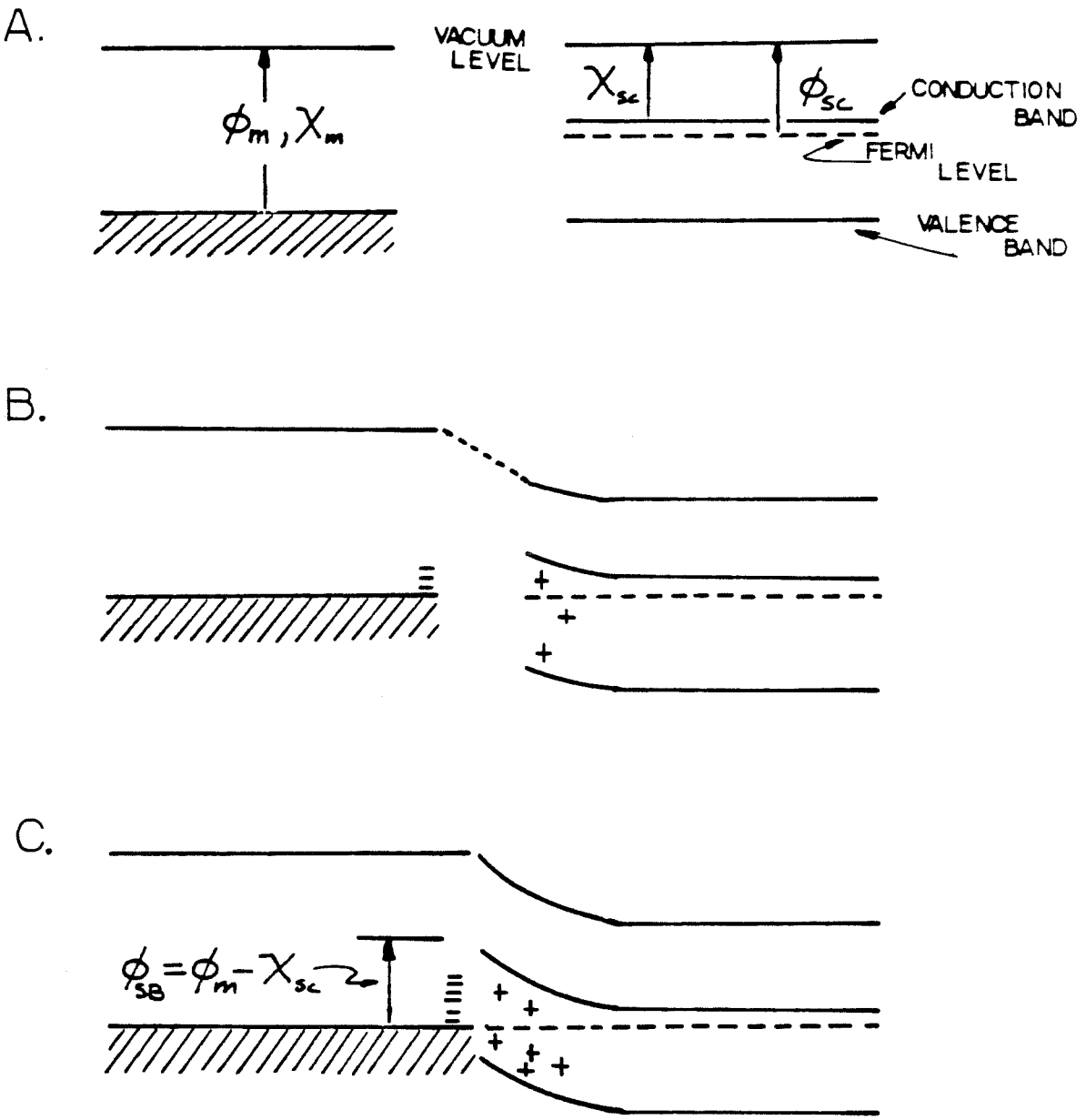

Figure 1.1. The Schottky-Mott theory of barrier formation. The metal and semiconductor are each characterized by a workfunction ., ϕ, and an electron affinity, χ, (A). At thermodynamic equilibrium the Fermi level of the electrons must be constant (B). This necessitates the formation of a space charge region to accommodate the difference in workfunctions of the two materials. A fully formed Schottky barrier (C) has a barrier height equal to the difference in the electron affinities.

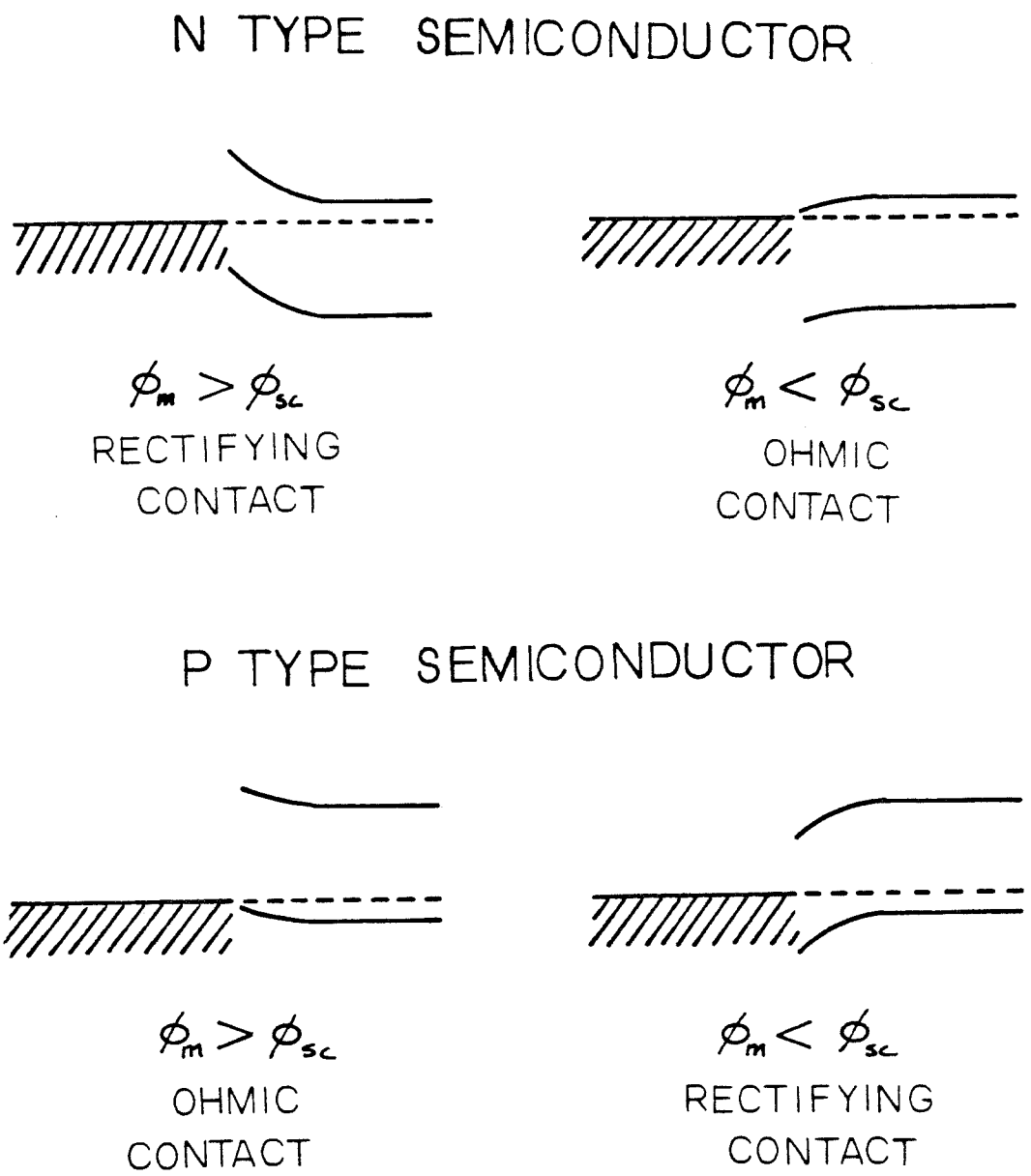

Figure 1.2. The Schottky-Mott theory predicts a range of electrical behavior at a metal semiconductor contact depending on the relative values of the workfunctions of the two materials.

of charge results in an electric field and potential difference between the two materials. The excess charge in the metal is confined to a narrow region on the metal surface whose width is on the order of the Fermi-Thomas screening distance in the metal (~ 0.5 Å).

Since the conduction electron density in the semiconductor is several orders of magnitude less than that of the metal, the screening length (Debye length) is much larger in the semiconductor than the metal. The electric field is subsequently pushed into the semiconductor creating a positive space charge region with the resulting band bending.

The positive charge in the semiconductor is provided by the depletion of electrons from a region near the surface leaving the ionized donor atoms exposed. As the distance between the metal and semiconductor is diminished to zero the electric field which has formed is pushed further into the semiconductor, resulting in the observed electrostatic barrier to be formed. From the diagram we find that the resultant barrier height is simply the difference in electron affinities in the two materials:

$$\phi_{SB} = \phi_{metal} - \chi_{sc} \quad . \qquad (1.1)$$

The Schottky-Mott theory predicts then that the barrier height is directly proportional to the metal workfunction.

While this theory has the attraction of being conceptually simple,

it is found to apply only in a few cases. Earlier investigations by Kurtin et al[4] and Cowley [5] found that in most cases the relationship between the Schottky barrier height and the metal work function was of the form

$$\phi_{SB} = S * \phi_m - \phi_o \qquad (1.2)$$

where ϕ_o is a constant and $S = \frac{\Delta\phi_{SB}}{\Delta\phi_m}$, usually referred to as the index of interfacial behavior. The Schottky-Mott theory corresponds to the S = 1 case.

Most semiconductors have an empirically derived value of S less than 1 and in many cases $S \sim 0$. The covalent semiconductors, such as Si, GaAs, and InP, have barrier heights which show very little dependence on metal workfunction for a variety of surface preparations. Ionic materials, such as ZnS, SiO_2, and ZnO, have a value of $S \sim 1$. Many of the II - VI semiconductors were found to have intermediate values of S. Both CdTe and CdSe have values of $S \sim 0.3$ [6]. Subsequent investigations [7-15], however, have demonstrated a more complex dependence on metal and surface preparation, particularly with recent sensitive surface techniques at ultra high vacuum (UHV).

The insensitivity of the barrier height to the metal workfunction is usually explained in terms of high density of localized electronic states which pins the Fermi level at the interface. Surface or interface states in the energy gap of the semiconductor are attributed to

a variety of causes. Dangling bonds, crystal defects [16], and states induced by chemical bonding [17] between the metal and semiconductor, among other effects, have been listed as sources of pinning states at the interface. A change in metal workfunction results in a change in occupation of the surface states and if the density of surface states is great enough, the Fermi level moves very little. The difference in workfunctions between the semiconductor and the metal is accommodated in a dipole layer at the interface made up of charged surface states and the metal surface charge layer. The dependence of S on the surface state density in this case has been derived by several authors [5,18].

While the exact origins of the pinning states in covalent semiconductors is still unknown, investigations on Schottky barrier formations have lead to a number of observations and empirical rules. The most common observation made is that the barrier heights to p and n material for a given metal, ϕ_p and ϕ_n, respectively, sum to the band gap of the semiconductor;

$$\phi_p + \phi_n = E_{gap} \tag{1.3}$$

This relationship has been seen to be valid to within the experimental uncertainty of most of the determinations of ϕ_p and ϕ_n. This result implies that the states responsible for pinning the Fermi level in both n and p material are located at the same energy within the gap of

the semiconductor. If the same state is responsible for the barrier height on n and p material, this state must be able to charge both positive and negative. The state must therefore be able to be both an acceptor and a donor, depending on its charge state. Recent investigations, however, have found some exceptions to Equation 1.3. Studies made on GaAs and other III - V materials under very controlled UHV conditions indicate that the Fermi level position at the interface is different on p and n materials [19]. Measurements made during the initial stages of barrier formation, using submonolayer metal coverages, find that the band gap exceeds the sum of the two barriers, $\phi_n + \phi_p < E_{gap}$. For the case of Al on GaAs (<110>), the band gap exceeds the sum of the barriers by 0.3 eV. This result may mean that under these experimental conditions there may be two types of pinning states; one acceptor-like and one donor-like, located at different energy positions in the gap responsible for determining a different barrier height on p and n material.

Another observation made, sometimes referred to as the "common anion" rule [20], states that the barrier heights produced by Au contacts are usually a function of the anion of the semiconductor substrate but not the cation [21]. This dependence was reported to occur as well as for the vacuum semiconductor interface [22] where the ionization potential is a function of anion only. The Au barrier height to a p type compound semiconductor was found to be dependent

only on the anion such that the Au barriers to p - InP and p - GaP are the same; about 0.76 eV in this case. This trend in Au barriers is illustrated in Fig. 1.3, obtained from Ref. 21. The Au barrier to p-type material is also seen to increase with increasing anion electronegativity.

Other observations made under UHV conditions have been important in understanding Schottky barrier formation. Several authors have shown that clean surfaces of III - V and some II - VI compounds possess no states in the gap of the semiconductor [23,24]. In the absence of these intrinsic surface states, the Fermi level at the surface and in the bulk semiconductor resides at the same position in the gap and no band bending is evident at the surface. The addition of metal adatoms to the surface of the semiconductor moves the Fermi level to the observed barrier height at submonolayer coverages [14]. The absorption of oxygen or chlorine onto a vacuum cleaved surface also results in the Fermi level being pinned at the interface near the same position in the bandgap that is observed with the absorption of metal adatoms. The insensitivity of the barrier height to the chemical nature of the metal overlayer has lead some authors to propose that crystal defects residing on or near the semiconductor surface introduce states in the gap. These defects could be induced by the condensation of metal atoms on the surface. States derived from these defects then serve to pin the Fermi level and yield the

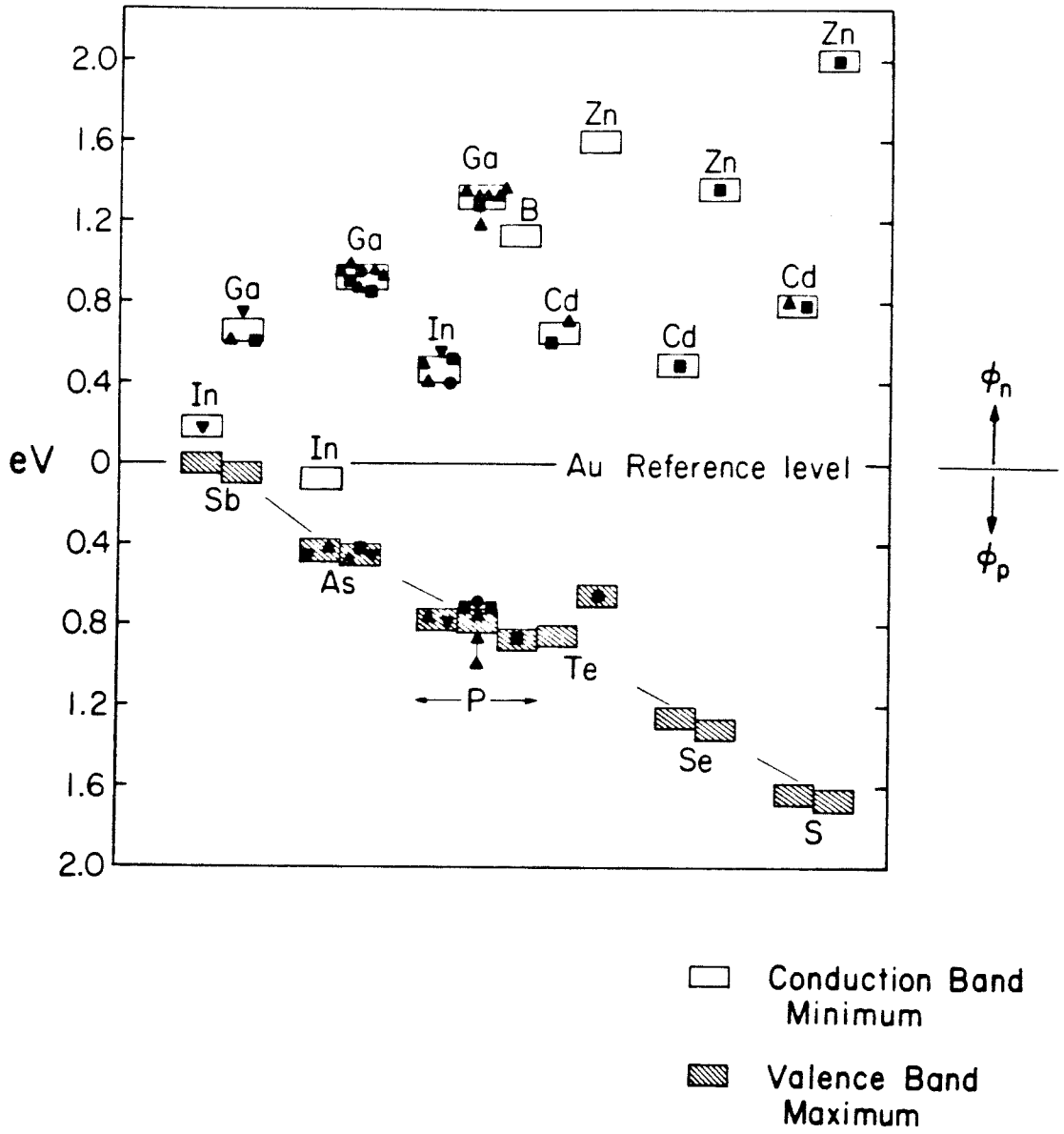

Figure 1.3.Schottky barrier height produced by Au on some II - VI and III - V semiconductors. The barrier height to the p-type materials, ϕ_p, is determined by the anion of the material. The semiconductors are ordered by anion electronegativity which increases from left to right.

observed band bending. The dependence of the Au barrier height on the anion suggests that an anion related defect, such as an arsenic vacancy in the case of GaAs, provides the necessary states. Calculations by Daw and Smith [25,26] have shown that neutral surface anion vacancies do provide a state in the gap near the observed barrier height. Such neutral vacancies can charge both positive and negative by the removal or addition of an electron. These defect-related states could fix the barrier height on both p and n material. While such a model is attractive, the actual situation at the metal semiconductor interface is probably more complex.

Observations made on Schottky barriers with submonolayer metal surface coverages, however, may not be directly applicable to contacts made with thicker metal layers. Physical and chemical reactions between the metal layer and the semiconductor substrate have been noted in several cases [8]. Dissolution of the substrate into the metal layer has often been observed. Both semiconductor constituents of InP and GaAs are found throughout Au overlayers [24]. Deposition of Au on GaSb causes the compound to decompose with Sb segregating to the surface of the Au. Many of these reactions proceed rapidly at room temperature [28]. All such reactions serve to increase the structural complexities of the metal-semiconductor interface.

These considerations all indicate the complicated nature of the metal-semiconductor interface making a complete understanding of

Schottky barrier formation difficult. The defect model of Schottky barrier formation has served as a useful framework to unify many of the past observations on III - V semiconductors, but further work is necessary in order to verify the existence and nature of these defects.

C. Au ON $In_xGa_{1-x}P$

In view of the considerations just discussed, a test of the dependence of the Au Schottky barrier height on the semiconductor anion can be made by studying the compositional dependence of the barrier height in a semiconductor alloy system. This chapter will investigate the extension of the common anion rule to the ternary system $In_xGa_{1-x}P$. For the two end points, x = 0 and x = 1, the barrier height to p-type material, ϕ_p, is known to be $\sim$0.76 eV. In this study we wished to determine whether ϕ_p remains constant for intermediate compositions. An analogous study of the corresponding arsenide ternary, $In_{1-x}Ga_xAs$, showed ϕ_p to be independent of composition, as expected from the common anion rule [29]. A contrary result has been obtained, however, in the case of ternaries involving Al. In the alloy system n - $Ga_xAl_{1-x}As$,

$$\phi_p = E_{gap} - \phi_n \tag{1.4}$$

was found to increase linearly with aluminum content [20].

D. Au - Cd ALLOY CONTACTS ON CdTe

This study investigates the use of Au-Cd alloys to achieve a higher barrier height on CdTe than possible with the use of a single metal. It is found that metal contacts consisting of an alloy of Au and Cd can produce a barrier height of 0.92 eV on vacuum cleaved surfaces of CdTe while contacts consisting of only Au and Cd produce a barrier of 0.65 and 0.45 eV, respectively, on vacuum cleaved surfaces. This increased barrier height found with Au-Cd alloy contacts may be consistent with current observations on Schottky barrier formation where crystal defects determine the measured barrier height.

E. HgTe - CdTe LATTICE MATCHED SCHOTTKY BARRIERS

Heterojunctions formed by the growth of an Hg chalcogenide on the corresponding Cd chalcogenide are unique structures which combine features present in Schottky barriers with those found in lattice matched heterojunctions. HgTe, HgSe, and β - HgS are all semimetals possessing a zincblende crystal structure and a lattice constant close to that of its cadmium counterpart [30]. The lattice mismatch of HgTe and CdTe is only 0.3%, (a_{HgTe} = 6.46 Å and a_{CdTe} = 6.48 Å) [31]. The close lattice match in this case makes possible the growth of a semiconductor heterojunction free of misfit dislocations and other strain related defects.

The heterojunction consisting of HgTe on CdTe is of particular interest due to a number of possible applications. Superlattices

consisting of thin alternating layers of CdTe and HgTe, each layer having a thickness of a few atomic layers, have been shown to have desirable optical and electrical properties [32]. Schottky barrier structures formed from a single heterojunction could exhibit a larger barrier height than can be achieved from the use of an elemental metal. Information derived from these structures may be useful in understanding the electrical properties in devices made from the solid solution of HgTe and CdTe; $Hg_xCd_{1-x}Te$. The devices are particularly important in infrared sensing applications.

There have been several estimates of the Schottky barrier height exhibited on the Hg X/Cd X heterojunction, where X is S, Se, or Te. A simple model of heterojunctions predicts that the valence band discontinuity at the heterojunction interface is equal to the difference in the ionization potentials of the semiconductors. The discontinuity in the conduction bands is then equal to the difference in electron affinities [33]. This is illustrated in Fig.1.4. The common anion rule states that the ionization potential of the semiconductor is determined by the anion of the material. The ionization potential of ZnTe, CdTe, and HgTe, using the common anion rule, are therefore the same. Since HgTe is a zero band gap semiconductor, or semimetal, the Fermi level lies near or at the valence band maximum of the material. The valence bands of HgTe and CdTe should in this case lie close in energy at the heterojunction interface. For a HgTe/n - CdTe heterojunction,

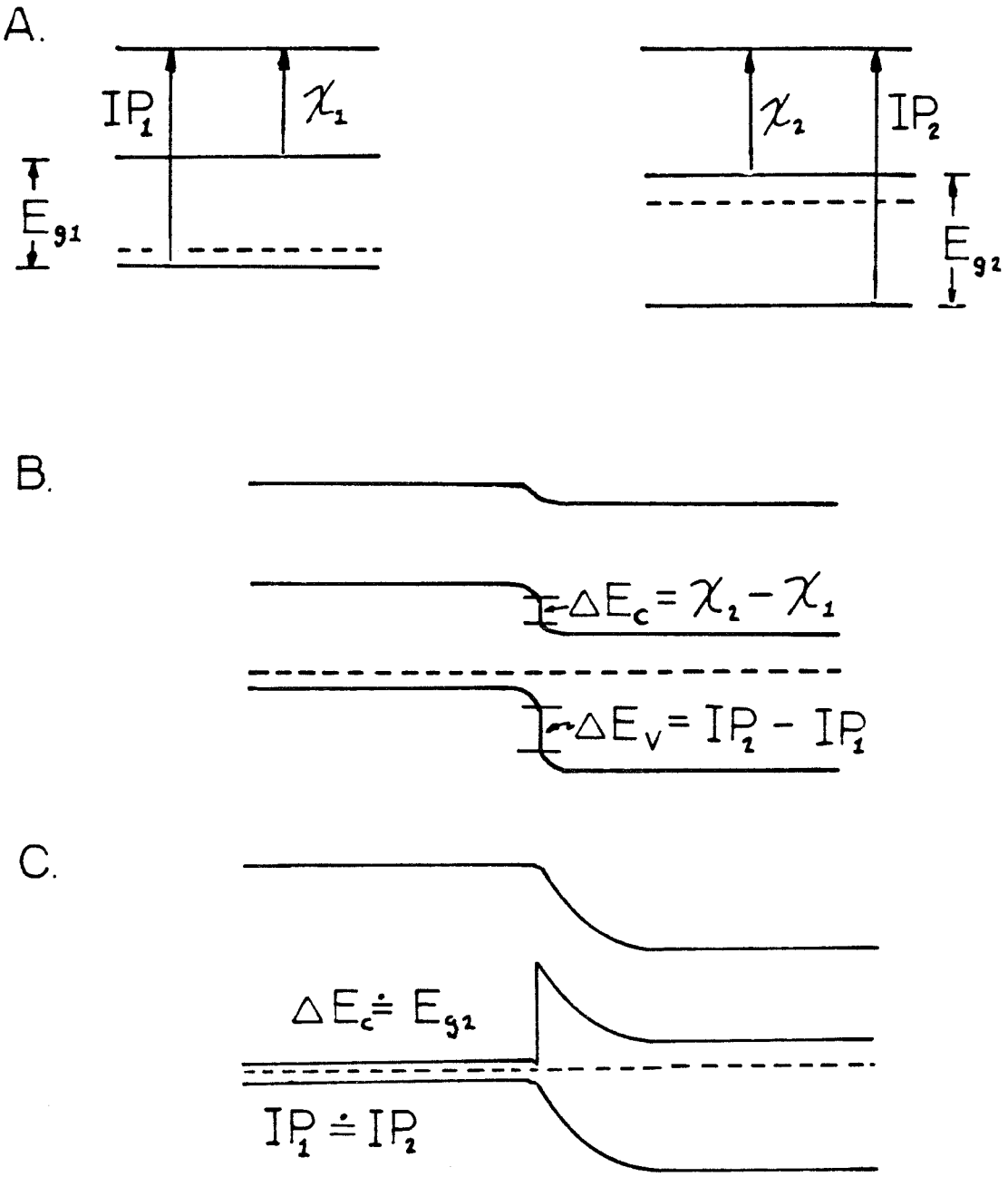

Figure 1.4. The band diagram for a semiconductor heterojunction can be constructed using assumptions similar to the Schottky-Mott theory. The separate semiconductors (A) are characterized by an electron affinity, χ, an ionization potential, IP, and a band gap, E_g. The resulting p - n heterojunction is shown in B. A heterojunction similar to that predicted for HgTe on CdTe by this model is illustrated in C.

the predicted barrier height almost equals the band gap of the CdTe, about 1.5 eV. The barrier height of HgTe on p - CdTe would be quite small, yielding perhaps, an ohmic contact. The barrier height of Au on n - CdTe is equal to 0.65 eV; thus the HgTe contact should represent a substantial increase in the range of obtainable barrier heights on CdTe.

The valence band discontinuity present in the HgTe/CdTe heterojunction can also be predicted by a method developed by Harrison [34]. A relative valence band maximum is assigned each material by a simplified tight binding approach. The valence band discontinuity present at a given heterojunction is then obtained by the subtraction of the two assigned values of the valence band maxima. The method successfully predicts the proper band discontinuities in a number of heterojunction systems such as Ge on GaAs and InP on CdS [34]. This method predicts valence band discontinuity of less than 0.1 eV in the case of both HgTe on CdTe and HgSe on CdSe. The measured valence band discontinuity in the HgSe on n - CdSe system, however, is $\sim$1.0 eV [35]. The failure of Harrison's method in the HgSe/CdSe case may possibly be attributed to the fact that CdSe cannot be made P type. Compensating defects are thought to be created in the material as the Fermi level is pushed to the lower half of the gap. This may prevent the formation of a Schottky barrier height greater than half the band gap in CdSe [36]. This complication does not arise in the case of CdTe

which can be made both p and n type. A HgTe on n - CdTe Schottky barrier height, which is approximately equal to the band gap of CdTe, is therefore also predicted by this model.

Heterojunctions consisting of epitaxial HgTe on n - CdTe substrates were fabricated in this study by a low temperature chemical vapor deposition technique (CVD). The barrier height determined on these structures is less than the predicted values of 1.5 eV. The barrier height was found to range from 0.65 eV to 0.85 eV depending on the HgTe growth conditions. The discrepancy between the predicted and observed values of the band discontinuities along with the dependence of the barrier height on the growth conditions will be discussed in this chapter.

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CHAPTER 2

REVIEW OF EXPERIMENTAL TECHNIQUES

A. INTRODUCTION

There are three main methods by which the Schottky barrier height is usually determined; current-voltage measurements, internal photoemission or photoresponse measurements, and capacitance-voltage measurements. Since these same methods were used in all three experimental works reported here, a brief review of each of these methods will be presented. Particular aspects of each of the measurement techniques pertinent to the experimental works later discussed will also be described.

B. CURRENT - VOLTAGE MEASUREMENTS

The measurement of the current-voltage characteristic is usually the fastest and easiest method by which the Schottky barrier height may be obtained. In these measurements, the current-voltage characteristic determined from a Schottky barrier device is typically fitted to an equation of the form

$$J = J_o(e^{qv/nk_BT} - 1) \quad , \tag{2.1}$$

where J is the measured current density at a given applied voltage V and n is the quality factor of the diode. If n is close to unity and J_o is independent of the applied voltage, the current transport over the electrostatic barrier can be interpreted in terms of Bethe's thermionic emission theory [1]. The reverse saturation current of the diode J_o is given by the thermionic emission theory as

$$J_o = A^{**} T^2 e^{-q\phi / k_B T} \qquad (2.2)$$

where A^{**} is the modified Richardson constant, T is the absolute temperature, and ϕ is the Schottky barrier height. The constant A^{**} is given as $A^{**} = 120 \left(\frac{m_e^*}{m_o}\right)$ in amps per cm^2 where m_e^* and m_o are the effective mass and mass of the free electron, respectively. The barrier height is usually determined by measuring the forward bias current characteristic at a given temperature or less frequently by the variation of the reverse bias saturation current with temperature. The barrier height determined from current-voltage measurements must be corrected for the image force lowering effect. This lowering of the electrostatic barrier is due to the attractive potential seen by the electron as it approaches the metal layer due to its image charge present in the metal. The change in barrier height $\Delta \phi$ is given by

$$\Delta\phi = \frac{1}{\varepsilon\varepsilon_o} \left\{ \frac{q\phi}{2\pi} C(0) \right\}^{\frac{1}{2}} \qquad (2.3)$$

where ϕ is the barrier height, C(0) is the zero bias capacitance per unit area, $\varepsilon\varepsilon_o$ is the permitivity of the substrate, and ϕ is the barrier height. In practice, the determination of ϕ from the reverse bias characteristic is more difficult due to the diode leakage currents and edge effects present in actual contacts [2]. In the studies presented here, only forward bias current measurements were made on the fabricated diodes.

The presence of other current transport mechanisms, in parallel with the thermionic emission current, results in an increase in the value of the diode quality factor from n = 1. These additional currents can arise from generation and recombination currents present in and near the depletion region, tunneling currents, and edge effects among other sources [1]. The determination of the barrier height when n deviates significantly from 1 is difficult due to the complicated dependence of the current on the bias voltage in these latter cases. The results of thermionic theory are usually taken to apply in diodes which have a quality factor $n \leq 1.2$.

An additional complexity can also arise due to the presence of a highly doped region near the metal-semiconductor interface [3,4]. This highly doped region can be intentionally produced by the use of ion implantation or result from chemical surface treatment implemented prior to the metal deposition. In certain cases such as Al Schottky barriers on silicon, a highly doped region is made by the doping of the semiconductor by the metal atoms themselves; a process accelerated by the heat treatment of the metal-semiconductor structure. The barrier height deduced from current-voltage measurements can differ substantially from actual barrier height measured at the interface. If the doping is of the same type as the background doping of the semiconductor, there can be a rapid band bending near the interface, as seen in Fig. 2.1. Electrons approaching this region of rapid band

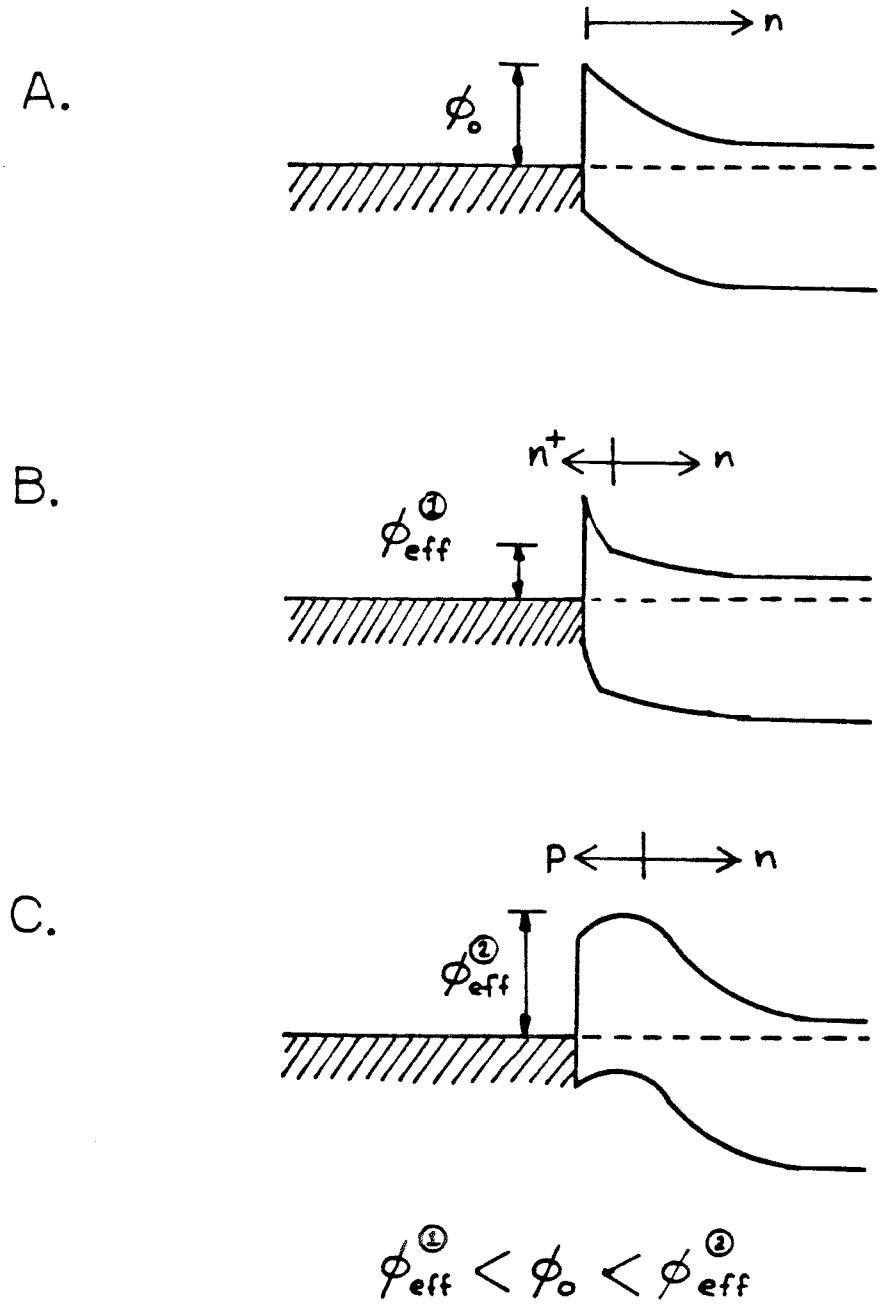

Figure 2.1. The barrier height of a Schottky barrier device can be affected by the non-uniformities in the semiconductor near the interface. In A, the semiconductor doping is uniform. The presence of a highly doped region of the same type as the bulk semiconductor, in B, causes sharp band bending through which the electrons may easily tunnel, decreasing the effective barrier height. Doping of the opposite type increases the effective barrier height by the partial formation of a p - n junction.

bending can tunnel through this narrow potential region. The effective barrier height to current is then lower than the actual barrier height at the interface. If the near-surface doping is of the opposite type than the semiconductor background doping, the measured barrier height may be greater than the actual barrier height at the interface due to the partial formation of a p-n junction. This is also illustrated in Fig. 2.1.

C. PHOTORESPONSE MEASUREMENTS

The theory for the photoemission of electrons from a metal was developed by Fowler in 1931 [5]. In his work, the photocurrent per incident photon J was found to have a dependence on photon energy given by $J \alpha(h\nu - \phi_{WF})^2$ where ϕ_{WF} is the metal work function. A simplified derivation of this result is given in reference 12. The photoemission of electrons from a metal into a semiconductor follows a similar dependence with the metal work function being replaced by the Schottky barrier height. The range of photon energies useful in the measurement depends on the experimental arrangement as shown in Fig. 2.2. The zero response intercept on a plot of the square root of the photoresponse with photon energy yields the Schottky barrier height, again uncorrected for the image force lowering effect.

Similarly, the photoemission from a semiconductor into a vacuum follows a power law dependence:

$$J \alpha(h\nu - \phi_{VB})^{\beta} \quad , \qquad (2.4)$$

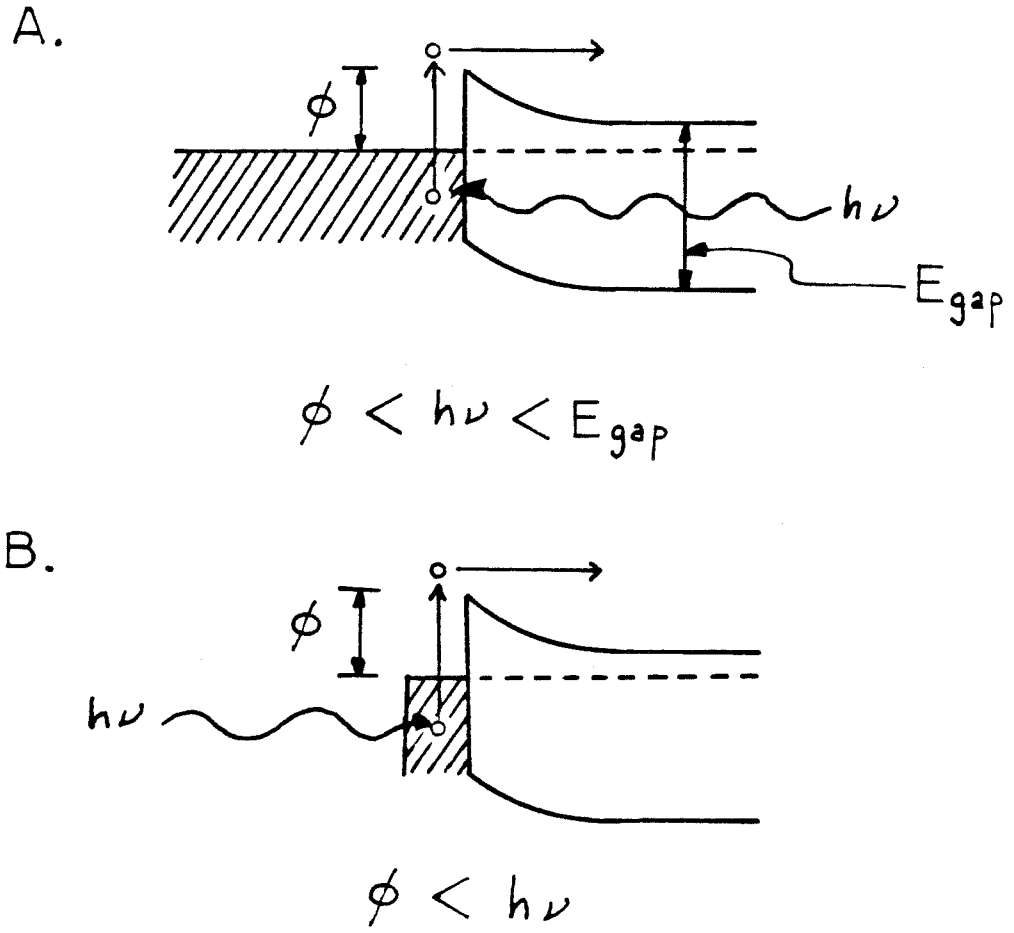

Figure 2.2. In the photoresponse measurement, an incident photon excites an electron from the metal over the electrostatic barrier. Since the electron mean free path in the metal is very short, only electrons excited near the interface may reach and surmount the barrier. The range of usable photon energies, $h\nu$, depends on whether the metal near the interface is illuminated through the semiconductor (A) or through a thin (<100 A) transparent metal layer (B).

where ϕ_{VB} is the semiconductor electron affinity plus the band gap, or ionization potential. The appropriate value of β depends on the details of the emission process and the nature of the semiconductor [6]. In lattice matched Schottky barrier structures where the metal overlayer has been replaced by a zero band gap semiconductor, the conduction band discontinuity, less the image force lowering, replaces ϕ_{VB}. A previous study on HgSe/CdSe heterojunctions has found the photoresponse to follow an $\beta = 3$ dependence [7].

The photoresponse measurement is usually considered the most reliable of the three barrier height measurements discussed here.

D. CAPACITANCE MEASUREMENTS.

The variation of the capacitance of a Schottky diode with voltage can provide a substantial amount of information on the nature of the near surface region of the semiconductor. The capacitance characteristic of an ideal Schottky diode is similar to that of a one-sided p - n junction where the metal takes the place of the heavily doped region of the p - n junction. The capacitance per unit area, at a given reverse bias, is given by

$$C = \frac{\varepsilon\varepsilon_o}{W} \quad , \qquad (2.5)$$

where $\varepsilon\varepsilon_o$ is the permitivity of the semiconductor and W is the depletion region width. The width of the depletion region increases with reverse

bias applied to the structure. In the simplest case of a constant doping in the semiconductor, the depletion region varies as

$$W = \sqrt{\frac{2\varepsilon\varepsilon_o}{qN_D}(V_{bi}-V)} \quad , \tag{2.6}$$

where N_D is the dopant concentration, and V_{bi} and V are the built-in and applied voltages, respectively [8].

Results of capacitance measurements are typically given in graphs of C^{-2} as a function of reverse bias. The slope of the curve at given reverse bias is related to the value of N_D at the depletion region edge by

$$\frac{dC^{-2}}{dV} = \frac{2}{\varepsilon\varepsilon_o q}\ \frac{1}{N_D} \quad . \tag{2.7}$$

Depth profiling of the dopant concentration may be accomplished this way. If the curve is a straight line, it may be extrapolated to infinite capacitance ($C^{-2} = 0$) yielding the value for the built-in voltage. The Schottky barrier height is obtained from the V_{bi} in voltage by

$$\phi = V_{bi} + \delta + \frac{K_B T}{q} \tag{2.8}$$

where δ is the energy difference between the Fermi level and the band edge (conduction band for n-type and valence band for p-type) in the

bulk semiconductor, given by

$$\delta = \frac{K_B T}{q} \ln \left(\frac{N_{DS}}{N_D}\right) \quad , \tag{2.9}$$

where N_{DS} is the density of states in the majority carrier band, and $\frac{K_B T}{q}$ in Eqn. 2.8 is a finite temperature correction to the depletion approximation.

The presence of deep levels in the semiconductor in addition to the shallow dopant complicates the interpretation of the capacitance measurement. Studies have found that the effect of deep levels on the measured capacitance depends sensitively on the method by which the capacitance is measured [9,10]. The capacitance is typically measured by applying a small high frequency ($\sim$1 MHz) test voltage on the diode in addition to the DC applied reverse bias. If the test voltage frequency is higher than the emission or capture rates of the deep level, the test voltage affects only the shallow dopant levels at the edge of the depletion region. As the test frequency becomes comparable to the emission and capture rates of the deep level, the test voltage affects the occupation of both deep and shallow levels causing the measured capacitance to change from its high frequency value. The measured capacitance is found to be not only a function of the test voltage frequency but also of temperature, through temperature dependence of the emission and capture rates of the deep level. The study of this dependence of the capacitance on test frequency and

the emission/capture rates of the deep level has given rise to experimental techniques such as Deep Level Transient Spectroscopy (DLTS) used in deep trap analysis [11].

Capacitance measurements performed on materials which have deep levels must therefore be interpreted carefully. It is impossible to discern between capacitance characteristics which are due to spatial varying shallow dopant concentration or those taken on materials with a deep level present without supplementary measurements being made on the material. An example of such a case is given in Appendix 1.

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CHAPTER 3

COMPOSITIONAL DEPENDENCE OF Au SCHOTTKY BARRIERS ON $In_{1-x}Ga_xP$

A. INTRODUCTION

As discussed in Chapter 1, the compositional dependence of the Au Schottky barrier height has been measured in only two semiconductor alloy systems. Measurements on $In_{1-x}Ga_xAs$ have found that the Au Schottky height to p-type material, ϕ_p, is independent of composition[1]. A similar study on $Ga_{1-x}Al_xAs$ has found that $\phi_p = E_{gap} - \phi_n$ is not constant, but increases linearly with Al content [2]. The $In_{1-x}Ga_xP$ system, like the $In_{1-x}Ga_xAs$ alloy system, has end point compositions ($x = 0$ and $x = 1$) which have the same Au barrier, ϕ_p, thus following the common anion rule. This present study was undertaken in order to determine if the common anion rule can be extended to intermediate compositions in $In_{1-x}Ga_xP$.

Schottky barrier structures on $In_{1-x}Ga_xP$ may have applications in optical devices. $In_{1-x}Ga_xP$ and the quadternary formed by As addition has been investigated as a potential semiconductor laser material for use in fiber optics communication. The use of quaternary alloys permits the choice of both the direct energy gap and lattice parameter over a wide range of values. Lasers made with $In_{1-x}Ga_xP$ offer the possibility of obtaining low wavelength lasers which are lattice-matched to conventional substrates. High quality $In_{1-x}Ga_xP$ epitaxial layers have been grown by LPE (liquid phase epitaxy) techniques on both GaAs and $GaAs_{1-x}P_x$ substrates [3]. The bandgap of $In_{1-x}Ga_xP$ varies with composition from the direct gap of InP which has a value

of 1.35 eV (0.92 μm) to the indirect gap of GaP at 2.24 eV (0.55 μm). The alloy system undergoes a direct to indirect transition at a composition of 74% GaP [4].

B. SAMPLE PREPARATION AND EXPERIMENTAL PROCEDURE

The Au Schottky barrier height was measured on 1-2 μm films of n-$In_{1-x}Ga_xP$ of various compositions epitaxially grown by LPE on <100> n-GaAs substrates. The samples were obtained from the RCA laboratories. Bulk samples of n-InP were also used in the subsequent measurements. All the specimens were first cleaned in a series of organic solvents (TCE, acetone, and methanol) and then chemically etched in a warm solution of $5H_2SO_4:1H_2O:H_2O_2$ ($T = 40^oC$) for 90 sec. After etching, the samples were rinsed in distilled water and dried in purified N_2. The etching rate of the acid solution was found to be 200 - 500 Å/min. Ohmic contacts were made to the GaAs substrate before etching by evaporating a Au-Ge eutectic and annealing in forming gas ($5\%H_2$ - 95% N_2) at 380^oC for 90 sec. The etched samples were then placed in an oil free ion pumped vacuum system. Gold evaporated through a stainless steel mask formed 160 μm diameter dots on the sample surface. The vacuum system pressure was less than 10^{-6} Torr as measured at the ion pump during evaporation. Samples of n-InP were also prepared by cleaving in air prior to the Au evaporation. In the case of n-InP, samples were prepared by these two methods produced similar barrier heights.

The chemical composition of the epitaxial layers was determined by photoluminescence, electron microprobe, and Rutherford $^4He^+$ backscattering measurements. The electron microprobe beam energy was 15 keV and the data were reduced by the Bence and Albee technique [5]. The three methods agreed well. Estimated error bars are shown in Fig.3.3.

Electrical and photoresponse measurements were then carried out on the resulting structures. Reverse bias capacitance-voltage and forward bias current-voltage characteristics were both measured.

C. EXPERIMENTAL RESULTS AND DISCUSSION

The forward bias I-V characteristics were measured over many decades of current and were fitted to Equation (1) of Chapter 2. Typical I-V characteristics of samples of various alloy compositions are shown in Fig.3.1. Only diodes having a quality factor $n \leq 1.1$ were used in the subsequent analysis except where noted.

The photoresponse measurements were performed by illuminating the metal-semiconductor interface through the GaAs substrate with monochromatic light. A broad spectrum tungsten lamp and a Gaertner monochromator were used as a light source [16]. The photoresponse as a function of incident photon energy at various alloy compositions is shown in Fig.3.2. The photocurrent was found to be of the form $J \alpha (h\nu - \phi_n)^2$ as expected for emission from the metal into vacuum or semiconductor.

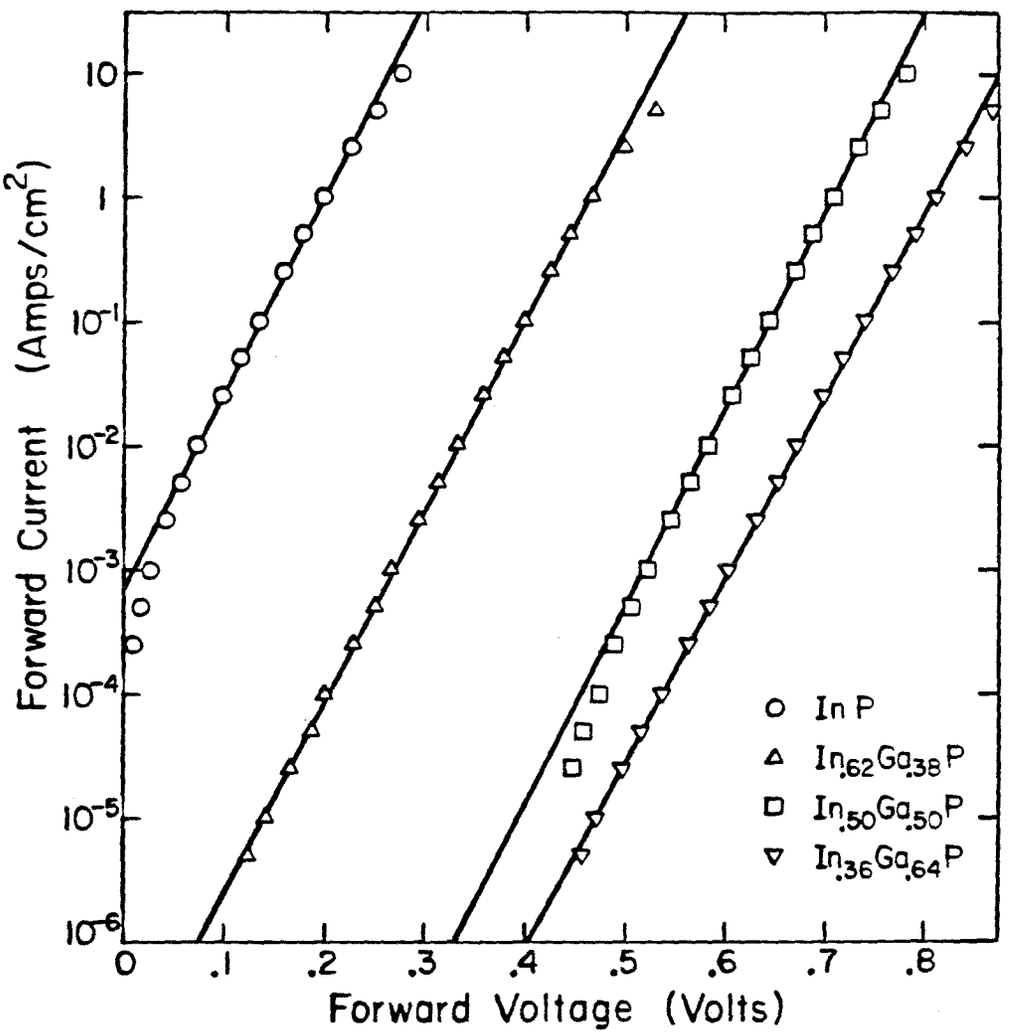

Figure 3.1. The forward bias current-voltage characteristics of Au on $In_xGa_{1-x}P$ Schottky barriers. The approximate area of the Au dots was $2 \times 10^{-4} cm^2$. All measurements were conducted at room temperature.

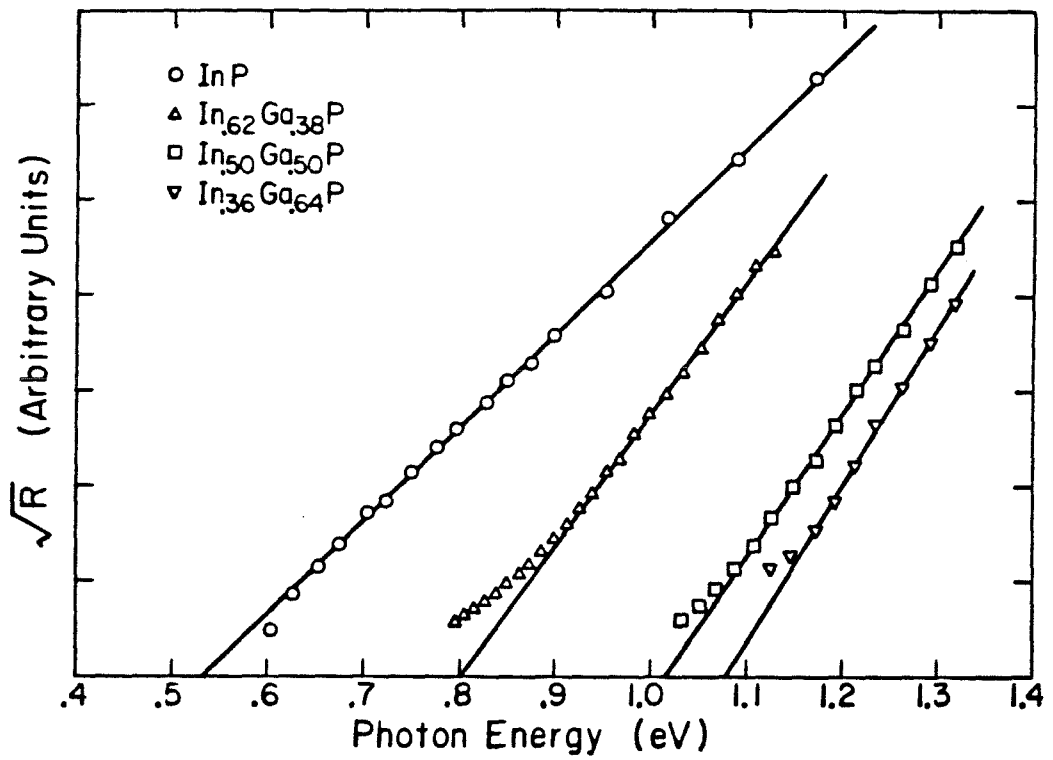

Figure 3.2. The photoresponse as a function of incident photon energy at various alloy compositions for Au Schottky barriers on n-$In_xGa_{1-x}P$. These measurements were made at room temperature.

The barrier height as determined by I-V and photoresponse methods is shown in Fig.3.3as a function of composition. The estimated error in the barrier height is indicated by error bars. The barrier heights shown here have not been corrected for the Schottky lowering effect. Since the sample doping is of the order 10^{16} - 10^{17} per cm^3, the decrease in barrier height would be 20 - 50 meV. The bandgap of $In_{1-x}Ga_xP$ is also indicated on this figure by a solid line. All barrier height measurements were done on direct gap material.

Barrier heights deduced from I-V and photoresponse methods were found to be in good agreement while the C-V measurement was found to be unreliable in determining the barrier height. $In_{1-x}Ga_xP$ is lattice matched to GaAs at x = .51. The capacitance method may be affected by bulk crystal defects in the epitaxial layer induced by the lattice mismatch of the epitaxial material to the GaAs substrate making the results difficult to interpret. High dislocation densities have been reported in $In_{1-x}Ga_xP$ grown on GaAs at compositions away from the lattice matched value [6]. Good agreement between barrier heights as deduced from the capacitance method and the other two methods was found only near the lattice matched composition.

An increased deviation from ideal thermionic behavior (n = 1) in the I-V characteristic was also observed as the sample composition was shifted away from the lattice matched composition. This is illustrated in Fig.3.4where the quality factor, n, increases with lattice mismatch,

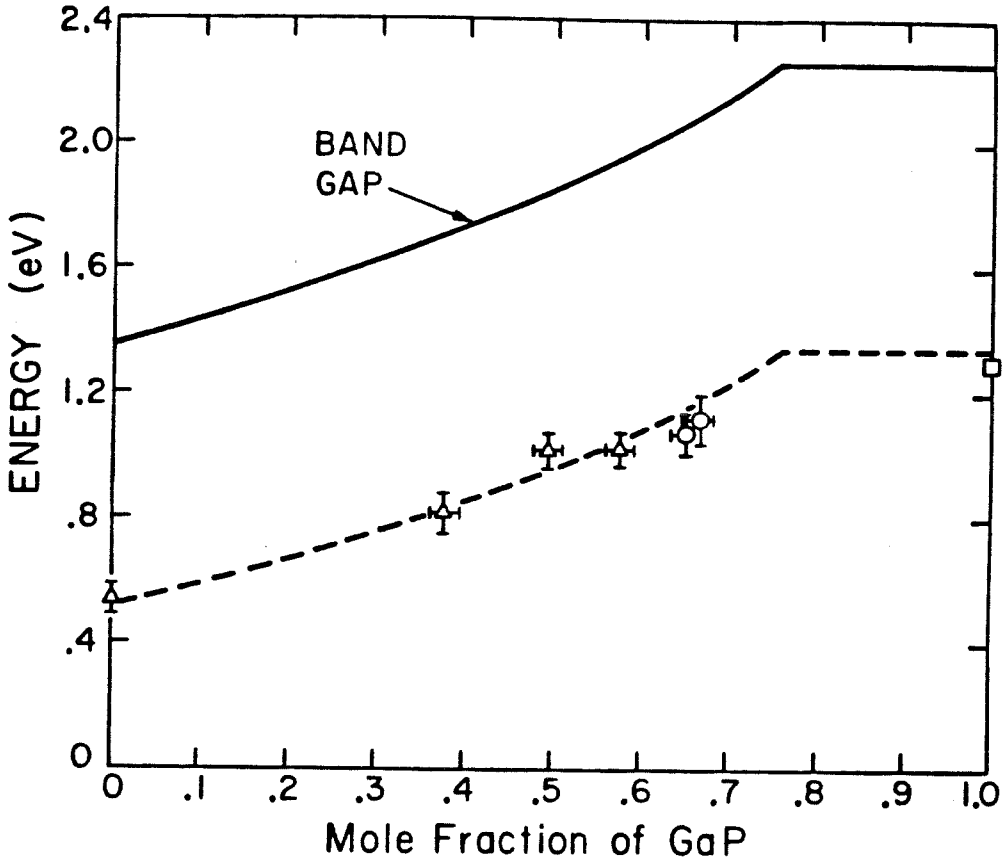

Figure 3.3. Measured Au Schottky barrier heights as a function of mole fraction of GaP, x in $In_{1-x}Ga_xP$. Δ indicates barrier heights obtained from diodes having a quality factor $n < 1.1$, O indicates diodes with $n \leq 1.2$. and □ is the Au on GaP barrier height reported by Mead (15). Dashed line is band gap -0.76 eV, i.e., barrier height expected by the "common anion" rule.

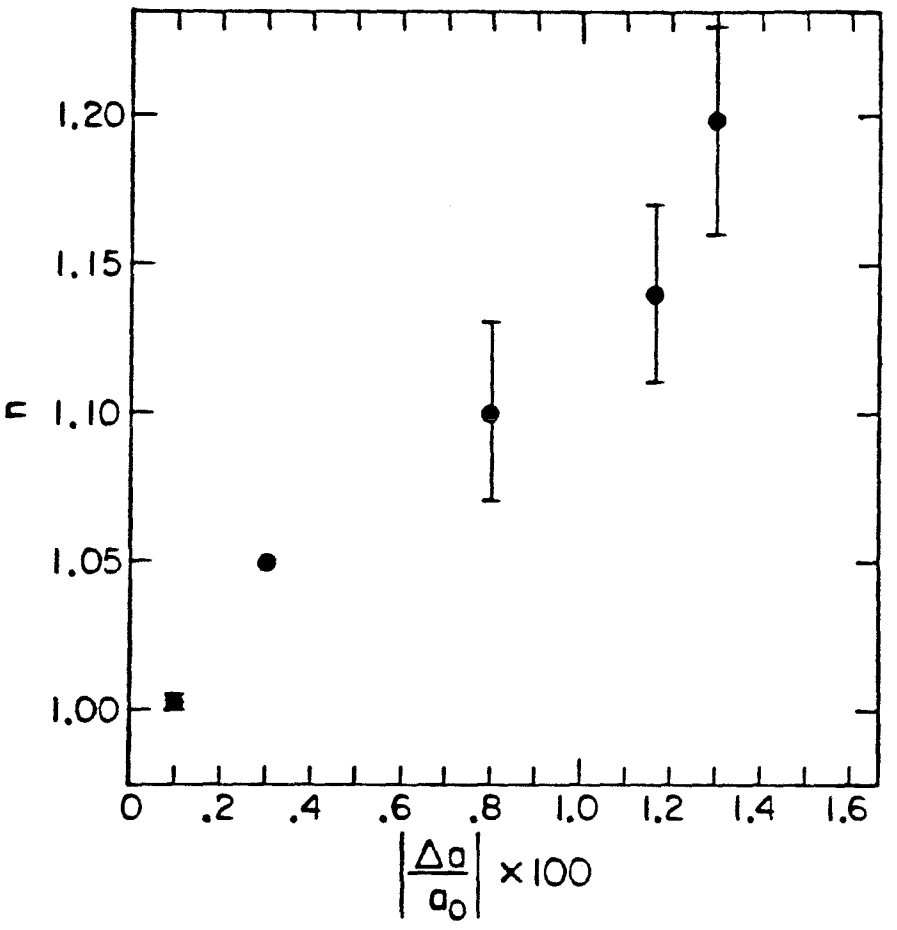

Figure 3.4.The quality factor, n, determined by fitting the measured current density to the Equation $J = AT^2e^{qV/nK_BT}$, is plotted as a function of lattice mismatch between the $In_xGa_{1-x}P$ epilayer and GaAs substrate. The lattice parameter was calculated using Vegard's law.

$$\frac{a_{epi} - a_{sub}}{a_{sub}} \quad , \qquad (3\text{-}1)$$

where a_{epi} and a_{sub} are the lattice parameters of the epitaxial and substrate materials, respectively. The value of a_{epi} was calculated using Vegard's law [7]. In heterojunctions, edge dislocations caused by lattice mismatch are thought to be very active recombination centers at the interface [8]. In the case considered here, misfit dislocations originating at the $In_{1-x}Ga_xP/GaAs$ interface propagate through the epilayer to the metal semiconductor interface where they may serve as such generation and recombination centers. The effect of such centers on the I-V characteristic would be evident in the deviation of the quality factor from n = 1. Diodes where the recombination/generation current is the dominant current transport mechanism exhibits a quality factor of n = 2 [9].

While acid etched samples gave reproducible barrier heights with nearly ideal diode characteristics, Schottky diodes fabricated on samples of $In_{1-x}Ga_xP$ which had been cleaned only by organic solvents often resulted in anomalous behavior. Barrier heights of such diodes were found at times to give higher barriers than the acid etched samples while other such samples yielded very low or zero barriers. Such results were usually nonreproducible, thus requiring the use of the acid etch.

According to the "common anion" rule, ϕ_p, being equal to the energy difference between the bandgap and ϕ_n which was measured here,

should be a constant. This is the case for $In_{1-x}Ga_xP$ where the barrier to n-type material is fixed relative to the conduction band minimum. This is indicated by the dashed line in Fig. 3.3. Deviations from ideal thermionic behavior ($n > 1$) seen at the larger values of lattice mismatch tend to give slightly lower values for the barrier height as calculated from the I-V characteristic than in the ideal thermionic case. This may give rise to the apparent slight deviation from the "common anion" rule found at the gallium rich alloy composition.

Recent calculations by Daw and Smith have attempted to explain the compositional independence on the Au barrier height in terms of a crystal defect related surface state. The energy level of a neutral anion vacancy located on or near the semiconductor surface shows a similar compositional independence in the $In_xGa_{1-x}P$ [10] system and linear dependence on Al content in the $Ga_{1-x}Al_xAs$ [11]. The energy level of these vacancy states are located near the Fermi level pinning position observed in Schottky barrier measurements. The authors, Daw and Smith, do point out that the correlation of the calculated anion vacancy energy level with the measured barrier height will probably be maintained by other defect levels formed from cation dangling bonds, as is the anion vacancy [11]. While the exact mechanism of the Fermi level pinning is unknown, it is suggestive from these calculations that the measured barrier height in $In_xGa_{1-x}P$ could be due to a defect surface state.

In summary, it has then been found that if the "common anion" rule applies to two compound semiconductors, such as InP and GaP, then the rule can be extended to an alloy mixture of those two compounds. This has been seen in both $In_{1-x}Ga_xP$ and $In_{1-x}Ga_xAs$. It is expected that $In_{1-x}Ga_xSb$ will also follow these "common anion" trends. The compounds or alloys which contain Al, for example AlAs or $Ga_{1-x}Al_xAs$, are found not to follow the rule. The extension of this work to quaternary system p-$In_{1-x}Ga_xAs_{1-y}P_y$ has also shown that the Au barrier height is dependent only on the anion ratio [12].

It has been suggested that information derived from these and other Schottky barrier measurements could also prove useful in estimating band edge discontinuities in heterostructures [13].

Since the valence band position relative to the Au Fermi level has been observed to be determined by the anion of the semiconductor compounds, the valence band discontinuity, ΔE_v, of compound semiconductor heterostructures composed of alloys or compounds following the "common anion" rule may be independent of the respective cations. Thus, one might expect the valence band discontinuity, ΔE_v, of $In_{1-x}Ga_xP_{1-y}As_y$-InP heterostructure to be independent of x. Using a linear interpolation for an estimate of the valence band position with respect to Au of $In_{1-x}Ga_xP_{.71}As_{.13}$, one would expect that $\Delta E_v \simeq 70$ meV. Recent experiments [14] in this system indicate $\Delta E_v \simeq 80$ meV.

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CHAPTER 4

Au-Cd ALLOY SCHOTTKY BARRIERS ON CdTe

A. INTRODUCTION

Schottky barriers fabricated on CdTe have been used for the past 10-15 years in nuclear detector applications and as a potential solar cell material. In these applications a large barrier height is desired in order to improve the device properties [1]. The barrier height on CdTe has been investigated both on chemically etched [2-4] and cleaved surfaces [5-8] with a range of metal overlayers. The barrier height on chemically etched specimens has been found to be independent of the nature of the metal overlayer. Measurements on both air cleaved and vacuum cleaved surfaces indicate a small dependence of the barrier height on the metal work function [5], although there is some disagreement among reported values for a given metal overlayer. Typically the largest barriers attained with elemental metals, 0.65 eV, is reported for Au or Pt contacts on CdTe although large barriers may be possible with the use of highly electronegative materials such as $(SN)_x$ or HgSe [9,10]. For most applications, however, the ease of fabrication and the reproducibility achieved by the use of common metals is highly desirable.

This study investigates the use of Au-Cd alloys to achieve a higher barrier height on CdTe than possible with the use of a single metal. It is found that metal contacts consisting of an alloy of Au and Cd can produce a barrier height of 0.92 eV on vacuum cleaved surfaces of CdTe while contacts consisting of only Au or Cd produce a barrier of 0.65 and 0.45 eV, respectively, on vacuum cleaved surfaces.

Since the defect structure and electrical properties of CdTe change with Cd activity, the increased barrier height found with Au-Cd alloy contacts may be related to current observations on Schottky barrier formation where crystal defects determine the measured barrier height.

B. EXPERIMENTAL PROCEDURE

Samples of both Indium doped and nominally undoped n-CdTe were used in the measurements. Square rods of undoped CdTe 2 mm on a side were first annealed at 750°C in a Cd pressure of about 650 Torr in order to decrease the bulk resistivity to $\sim$0.8 Ω cm. Both Au and Cd Schottky barrier structures were formed by cleaving bulk samples of CdTe in an ion pumped vacuum system at a pressure of $\leq 10^{-6}$ Torr as measured at a pump flange. In order to minimize contamination of the cleaved surface by the residual gases in the vacuum system, the crystal was cleaved under a stream of rapidly evaporating metal. The cleaved crystal with either an Au or Cd overlayer was then removed from the vacuum system. Circular contacts, 1 to 2 x 10^{-4} cm^2 in area, were defined in the metal layer by photolithography. The Cd metal layer was then etched in dilute HNO_3 (<1% HNO_3 in H_2O) solution. The Au overlayers were etched in a 1% Br in methanol solution. Since Hg can dissolve an appreciable amount of Au, the Au on the field regions between the photoresist dots was also removed by dissolution into a Hg drop rolled across the sample surface.

Schottky barrier structures utilizing an Au-Cd alloy were formed in a similar fashion. Samples of bulk CdTe were cleaved in vacuum and coated with a thin ($\leq$200 Å) layer of Cd. The cleaved crystal was then immediately placed in a second ion pumped vacuum system where Au dots (1 to 2 x 10^{-4} cm^2) were evaporated onto the Cd overlayer. The Au dots served as an etchant mask for the removal of Cd from the field region between the Au dots. After fabrication of the Au/Cd metallization, several of these structures were annealed at low temperature (160° C) for up to 1 hr. The forward bias current-voltage characteristic was measured over 4 to 5 decades of current. The results were fitted to Equation 1 of Chapter 2. All the data were taken at room temperature except where otherwise noted. Since only diodes having a quality factor less than n $\leq$1.2 were investigated further in this study, the results of thermionic emission theory are valid. The electron effective mass, m_e^*, taken to be $m_e^* = 0.10\ m_o$ for CdTe in the determination of the barrier height from the I-V characteristic. Typical I-V characteristics are shown in Fig. 4.1.

Photoresponse measurements were performed on the Au and Au-Cd structures by illuminating the metal-semiconductor interface through the CdTe substrate with monochromatic light. Photoresponse measurements on Cd Schottky barriers were not possible due to the low barrier height and subsequent poor diode behavior at room temperature. The measured photoresponse as a function of incident photon energy is shown in Fig. 4.2. The photocurrent was found to be of the form

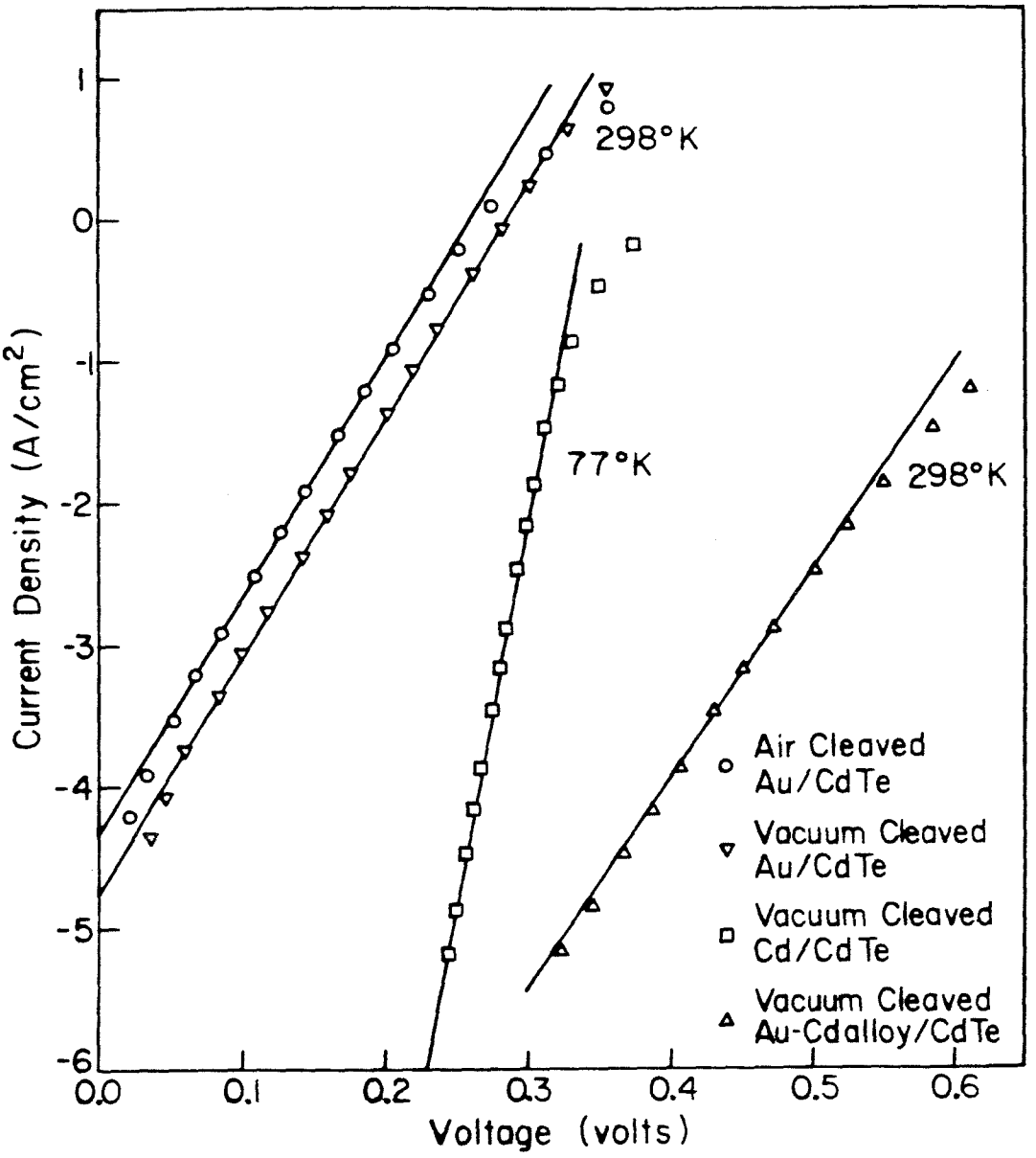

Figure 4.1.The forward bias current-voltage characteristics of Schottky barrier structures measured here. All the measurements were taken at room temperature except for the Cd on CdTe structure which was measured at 77°K.

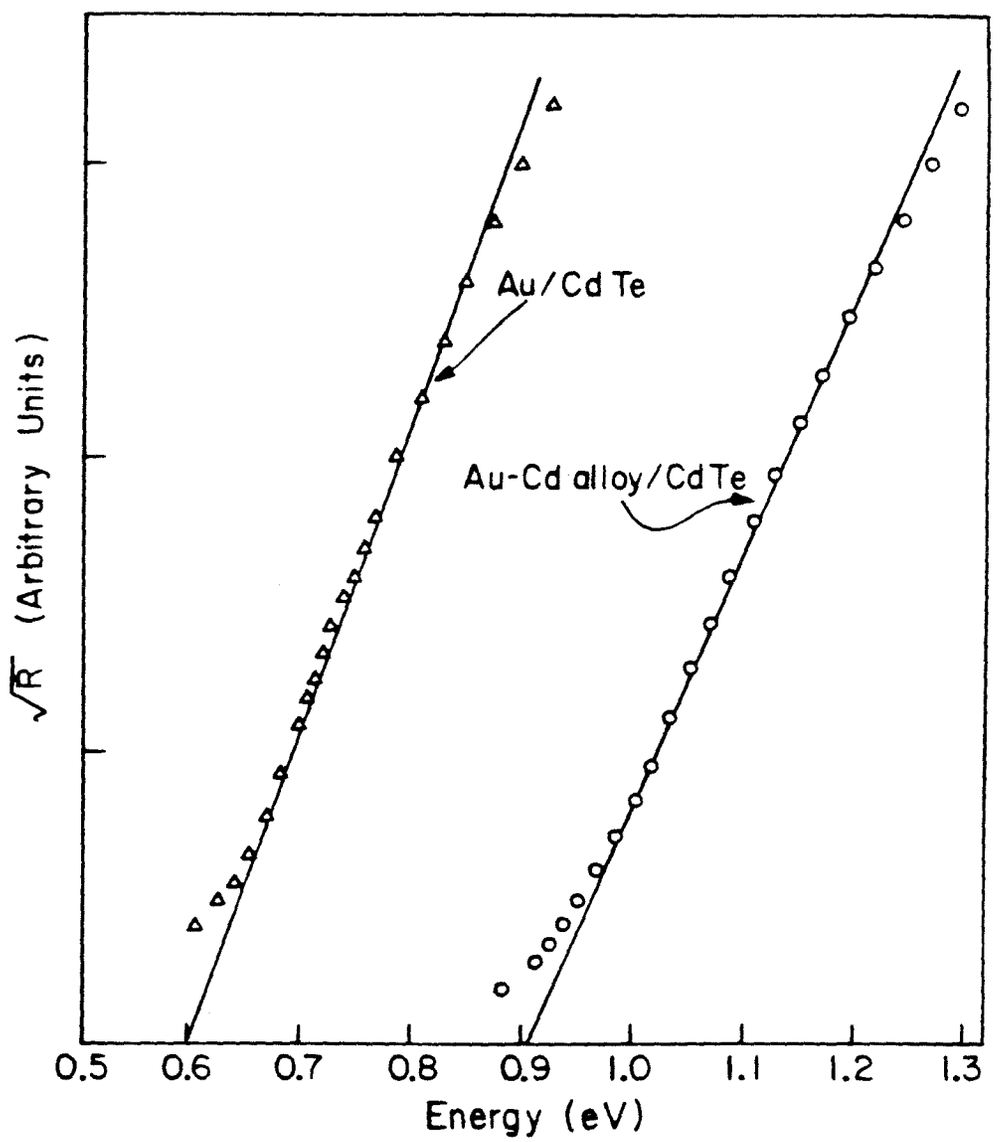

Figure 4.2. The photoresponse, R, as a function of incident photon energy. Barrier heights obtained from this measurement must be corrected for the image force lowering effect. The photoresponse was measured at room temperature.

$J \alpha (h\nu - \phi)^2$ as expected for emission from a metal into a semiconductor.

Reverse bias capacitance measures on the diode structures were made using a Boonton capacitance meter. The barrier height and carrier concentration were deduced using the conventional model for a Schottky barrier structure as described in Chapter 2.

C. RESULTS

A summary of the measured barrier heights is given in Table 4.1. Excellent agreement was found between barrier heights as determined by current voltage and photoresponse techniques while the capacitance-voltage measurement typically gave slightly higher values. The reported barrier heights have been corrected for the image force lowering effect. The carrier concentration was typically 10^{14} to 10^{15} electrons per cm^3, yielding an image force lowering of 10 to 30 meV. There was no measurable difference between heights measured in In doped or undoped CdTe. The small increase in barrier height for Au on air cleaved samples has been observed previously on CdTe [5].

The Schottky barrier height for Cd on CdTe, of 0.4 to 0.5 eV, was found to be lower than the barrier height for Au on CdTe contacts. The low barrier height of this structure and the resulting poor room temperature diode characteristic complicated the room temperature measurements making a more accurate determination of the barrier height impossible. The low barrier height of Cd on CdTe does agree with

Metal	Surface Preparation	ϕ(eV)
Au	air cleaved	0.71 ± .02
Au	vacuum cleaved	0.65 ± .02
Cd	vacuum cleaved	0.45 ± .05
Au-Cd	vacuum cleaved	0.92 ± .02

TABLE 4.1. Measured Schottky Barrier Height for Various Metal Overlayers on n-CdTe.

previous trends on CdTe where metals having a lower electronegativity tend to give a lower barrier height than Au.

The contacts formed by the deposition of a Au overlayer on a thin Cd layer gave two different barrier heights. A low barrier equal to that of the Cd on CdTe barrier height was found on samples where the Au and Cd layers had not formed an alloy or interdiffused appreciably. A larger barrier was found on samples in which the Au and Cd had formed an alloy or solid solution. The formation of the alloy occurred either during the deposition or by annealing the sample after the Au deposition. The surface of the CdTe may become heated during the Au deposition due to proximity to the hot filament used in the Au evaporation. The bulk diffusion coefficient for Au in Cd at a temperature of 200°C is approximately $10^{-12} cm^2/sec$ [11]. If the sample surface attained this temperature during a typical 20 - 30 second deposition, an interdiffusion region of 500 Å would be expected. Since the Cd layer thickness is about 100 Å, the Au and Cd should form a relatively homogeneous solid solution near the substrate surface. Gold has a high solubility for Cd at low temperatures; 18 atom.% at 200°C [12]. The Cd may also diffuse into the CdTe substrate itself. Using extrapolated bulk values of the tracer diffusion coefficient of Cd in CdTe, the diffusion distance of Cd is approximately 60 Å [13].

Structures in which the Au and Cd did not appreciably interdiffuse during the Au deposition possessed the low Cd on CdTe barrier height. The low barrier height could be converted to the higher barrier by

annealing the metal layers at low temperatures (<200^{o}C) in an inert atmosphere. Further heat treatments on the alloyed contacts did not provide any additional increase in barrier height as determined by the I-V measurement. Such additional heat treatments did result in a slow degradation in the diode characteristic, increasing the diode quality factor from $n < 1.1$ to $n \geq 1.5$.

D. DISCUSSION

A possible cause of the increased barrier height achieved by the use of Au-Cd alloys is suggested by recent studies which indicate that chemical activity and surface stoichiometry may play an important role in Schottky barrier formation. These studies are reviewed and discussed in Chapters 1 and 3. The physics of Schottky barrier formation has been studied predominantly on Si and III - V materials. In comparison, there has been little work done on II - VI materials. It is not surprising that the formation of Schottky barriers on CdTe and other II - VI materials is not as well understood as on III - V materials. A large number of bulk crystal defects have been observed in CdTe [14] as in all of the II - VI compound semiconductors, a fact that has long complicated the understanding and use of II - VI materials. These defects can be made to dominate the electrical properties in CdTe by appropriate annealing treatments.

Annealing treatments, for example, done under a low Cd activity (vapor pressure) produce compensation in In doped material. This is

believed to be due to the introduction of Cd vacancies, which are acceptors. These Cd vacancies can form complexes with the In dopant atoms producing compensation [15]. In CdTe, defects characteristic of the metal excess side of the phase stability region tend to make the material n type, while material which has an anion excess is usually p type. At any point, however, the defect structure and concentration of bulk CdTe is determined by the temperature, impurities, and the chemical activities of Cd and Te through the laws of mass action and the electroneutrality condition [16].

In this study, the presence of Cd in the Au overlayer changes the nature of the surface reactions and defects normally present at the Au-CdTe interface. There is a difference in chemical environment at the interface from the high Cd activity present in the Au-Cd alloy contact to the lower Cd activity found at the pure Au contact. As mentioned above, bulk CdTe exhibits wide variations in defect structure with temperature and Cd activity. Similar or analogous variations in defect structure at and near the interface could be expected with the difference in Cd activity in the three structures studied here; Cd, Au and Au-Cd alloys. The model proposed here does assume the formation of a Au-Cd solid solution after annealing. The formation of a Au-Cd intermetallic compound, however, cannot be ruled out. Other investigations on thin film reactions, particularly in the metal-silicon systems [18], have found that the thin film structure and composition may

not always be predicted from bulk phase diagrams, as was done in this study. Such compound formation would complicate the physical situation present at this metal-semiconductor interface and perhaps account for the observed change in barrier height. While these are only qualitative observations, much additional work would be needed in order to verify if this is indeed the case.

The use of alloy contacts may increase the range of obtainable barrier heights on a variety of semiconducting materials. Such contacts where the activity of the substrate material is fixed in the metal overlayer should prove to be more stable with respect to time and temperature than elemental metal contacts. A similar situation occurs with Al contacts to Si where the addition of Si to the Al metallization inhibits the reaction of the Al with the Si substrate [17]. Further studies on alloy contacts in a more controlled environment will be helpful in understanding the basic mechanism of Schottky barrier formation.

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CHAPTER 5

HgTe/CdTe LATTICE MATCHED SCHOTTKY BARRIERS

A. INTRODUCTION

The study of HgTe/CdTe heterojunctions is of both technological and scientific interest. The information obtained from these structures is useful in understanding the properties of $Hg_xCd_{1-x}Te$, an important material for use in infrared detectors and imaging arrays. The bandgap of the material may be varied with composition over a wide spectral range from the visible ($x \lesssim 0$) to over 30 μm ($x > 0.80$) [1]. Since the lattice parameters of HgTe and CdTe are nearly equal ($\frac{\Delta a}{a} = 0.003$), lattice matched epitaxial growth of $Hg_xCd_{1-x}Te$ for all values of x may be obtained on CdTe substrates.

This heterojunction along with the other HgX/CdX heterojunctions, where X = S or Se, form unique structures; combining features of the Schottky barrier structure, due to the high carrier concentrations present in the semi-metallic Hg chalcogenides, with the structural perfection present in lattice matched heterojunctions. Calculations on superlattices of alternating HgTe and CdTe layers suggest desirable optical and electrical properties [2]. The realization of these properties depends, however, on the existence of a small valence band discontinuity between HgTe and CdTe.

There have been two predictions of the valence band discontinuity between these two materials, as discussed in Chapter 1. The "common anion" rule predicts that the valence band discontinuity should be approximately zero. The method of Harrison for predicting heterojunction

band lineup also indicates no appreciable valence band discontinuity. The resulting heterojunction between HgTe and n-CdTe should exhibit a large barrier height, almost equal to the band gap of CdTe. A junction made with p-CdTe would have a small barrier, thus affording an ohmic contact.

Similar predictions of a negligible valence discontinuity have been made in the case of the lattice matched heterojunction formed by the growth of HgSe on CdSe. Best and McCaldin have grown this heterojunction by a H_2 transport CVD technique [3]. Measurements on this structure indicate a valence band discontinuity, ΔE_V, of approximately $\Delta E_V \simeq 1$ eV. As pointed out in Chapter 1, there may be limitations set on the Schottky barrier height attainable on CdSe due to self compensation in the material. It should also be noted that the electrical characteristics of the HgSe/CdSe heterojunction also depended on the growth procedure. Prior to the HgSe growth, the CdTe substrate was annealed in either a H_2 or Ar ambient in order to remove any damage and surface impurities on the growth surface. Heterojunctions fabricated on Ar annealled substrates yielded rectifying contacts with the above-mentioned band discontinuity ($\Delta E_V \simeq 1$ eV). Contacts formed by the growth of HgSe on H_2 annealled CdSe yielded an ohmic characteristic. In this case, the extreme reducing atmosphere was thought to make the surface region of the CdSe highly n type by the introduction of native donor defects such as Cd interstitials and Se vacancies [4]. This highly doped region would reduce the effective barrier height to below

a value where rectification is achieved at room temperature. This effect is described in greater detail in Chapter 2.

The work on HgSe/CdSe heterojunctions has proved to be an exception to the results derived from the simple models for estimating the valence band discontinuity at the heterojunction interface. This work has also shown that variations in the growth procedure may change the electrical properties of the near surface region by the introduction of electrically active defects, which in turn can change the observed Schottky barrier height.

The limitation on the Schottky barrier height in CdSe, due to self-compensation effects, should not be present in CdTe. Bulk samples of both p and n type CdTe have been prepared and are commercially available. The electrical characteristics of CdTe depend not only on the dopant atoms but also on the crystal defects present in the substrate as pointed out in Chapter 3. With this limitation on the barrier height due to self-compensation absent in CdTe, the Schottky barrier of the HgTe/CdTe heterojunction should follow the common anion rule yielding a barrier height equal to the band gap of CdTe, $\phi \simeq 1.5$ eV.

B. GROWTH TECHNIQUE CONSIDERATIONS

The epitaxial layers of HgTe were grown on CdTe substrates in this study by a new metal organic chemical vapor deposition (MOCVD) technique. Epitaxial layers of HgTe, or more commonly $Hg_{1-x}Cd_xTe$, have been formed

by a variety of methods including vacuum deposition [5], sputter deposition [6], ion implantation [7], vapor deposition [8-9], close-spaced transport [10], and liquid-phase epitaxy (LPE) [11-13]. Overall, LPE has proved to be the most useful of these methods. Epitaxial layers have been grown by LPE from both Hg and Te solutions. Most $Hg_{1-x}Cd_xTe$ used in infrared detectors is grown by LPE using a Te solvent. The relatively high temperatures used in Te solution LPE growth does, however, lead to the interdiffusion of the growing layer with the underlying substrate causing a vertical compositional grading in the $Hg_xCd_{1-x}Te$ layer. The extent of the interdiffusion increases rapidly with temperature making a low temperature growth technique desirable. The use of chemical vapor deposition techniques has not previously been reported for the growth of HgTe or $Hg_{1-x}Cd_xTe$.

Epitaxial layers of HgTe were formed by the reaction of Hg vapor and the organic compound dimethyl telluride (DMT) according to the reaction:

$$Hg + (CH_3)_2Te + H_2 \rightleftarrows HgTe + 2CH_4 \quad . \qquad (5.1)$$

Dimethyl telluride has been used previously, together with other metal-organic compounds, in the formation of CdTe, ZnTe and a variety IV-VI compounds [14-15]. DMT has been used instead of H_2Te, which is a preferred source of Te. H_2Te is commercially unavailable probably due to its unstable nature. The use of DMT may introduce

carbon as an impurity into the growing films. This technique was developed in this study in order to provide a low temperature growth method.

The development of a low temperature growth technique in this study was required from both materials and device structure considerations. The remainder of this section will discuss the effects of these considerations on the choice of a CVD growth technique. Limitations on the CVD growth parameters such as temperature, vapor phase composition, and growth rate will be presented in reference to the growth of HgTe on CdTe. Since this section represents a detailed materials oriented discussion, the reader may choose to proceed to the next section without a great loss in continuity.

The most easily controlled growth parameter in a CVD system is the growth temperature. The range of growth temperatures which may be used in a specific CVD growth technique is limited not only by the kinetics of the chemical reaction utilized in the deposition but also by material properties and final desired device structure. These considerations set both upper and lower bounds on the processing and growth temperatures which may be used.

The first consideration of the growth temperature is set by the kinetics of the chemical reaction used in the growth. The lower bound on the growth temperature in this case is determined by the temperature where the reaction kinetics are too slow to deposit the

necessary material in a reasonable length of time. The lower range of useable temperatures may be extended by the use of a plasma-assisted or photo-assisted CVD [16] system. Plasma vapor deposition has been very successful in the production of amorphous silicon films [17-18]. An upper temperature limit in a CVD system is derived from the need to confine the reaction to the substrate material. If the gas phase temperature becomes too high, the chemical reaction can take place in the vapor phase. These undesirable gas phase reactions can deplete the growth nutrients from the vapor phase and interfere with the material growth on the substrate. Such reactions may be suppressed by use of a low pressure CVD technique and through the use of a cold wall CVD reactor. In a cold wall reactor only the sample substrate is heated, usually by r-f induction, leaving the gas phase cool until it reaches the hot substrate where the chemical reaction can easily occur. Many metal organic compounds react easily at low temperatures, a fact which has necessitated the use of a cold wall reactor for metal organic CVD growth. This gas phase reaction usually sets the upper limit on growth temperatures in a hot wall reactor. In a hot wall reactor, the growth reactor is typically situated in a tube furnace. The gas phase, not just sample substrate, is heated prior to the deposition. A hot wall reactor was utilized in this study.

The range of growth temperatures used in this study was relatively narrow. HgTe grown at temperatures greater than 350 °C

yielded poor results. A factor contributing to this poor growth was the reaction of Hg and DMT vapors in the gas phase at elevated temperatures (>350°C). The lower limit on the growth temperature was found to be 300° - 325°C. At temperatures below 300°C, the reaction between Hg and DMT is very slow leading to little or no HgTe growth.

A second set of considerations which affect the growth method is determined by the material properties of the growing layer and the substrate. These are generally divided into the conditions for stability of the growing layer and surface mobility considerations.

Thermodynamic equilibrium and stability of the HgTe layer is maintained when the chemical activities of Hg and Te are fixed at appropriate values at the HgTe surface. This is achieved by fixing the vapor pressures of Hg and Te in the growth environment at values determined by the temperature and free energy of the HgTe. The equilibrium vapor pressure of Hg and Te are related by the law of mass action. The equilibrium of HgTe with its vapor phase components can be described by the reaction:

$$Hg(v) + \frac{1}{2}Te_2(v) \rightleftarrows HgTe(s); \quad \Delta G \tag{5.2}$$

where ΔG is the Gibb's free energy of the reaction. The law of mass action when applied to this reaction relates the vapor pressures of Hg, P_{Hg}, and Te, P_{Te_2}, through the relation:

$$P_{Hg}\, P^{\frac{1}{2}}_{Te_2} = e^{-\Delta G/RT} \quad . \qquad (5.3)$$

The upper and lower limits on the Hg and Te vapor pressures can be found at both the metal saturated and anion saturated sides of the HgTe phase stability region. On the metal rich side, the Hg pressure in equilibrium with HgTe is almost equal to the vapor pressure of elemental Hg at that same temperature. A similar situation exists at the anion rich side of the phase stability region where the Te vapor pressure in equilibrium with the HgTe is essentially that of elemental Te. In the absence of the required equilibrium vapor pressures, the HgTe will decompose in an effort to provide the requisite vapor pressure. This has been observed in HgTe heated to low temperatures (<300°C) in vacuum. In these studies, Hg readily evaporates from the HgTe surface, creating a pure Te layer on the surface which grows in time [19].

The CVD growth of both HgTe and $Hg_xCd_{1-x}Te$ is difficult due to the large vapor pressures of the constituent elements, in particular Hg, required to be present to prevent thermal decomposition of the growing layer. In the case of pure HgTe at 500°C, the vapor pressure of Hg must remain between 0.16 and 7.0 atm. to prevent decomposition or two-phase formation [20]. The high Hg pressures required at these temperatures (500°C) for the growth and stability of the deposited layer have prevented the use of conventional open tube CVD reactors

which operate at pressures less than or equal to 1 atm. If the substrate temperature is lowered, however, the required Hg pressures also decrease such that growth of HgTe at 325°C requires the Hg pressure to remain between $5x10^{-4}$ and 0.6 atm. [21] These pressures can be easily maintained by a source consisting of elemental Hg held at an appropriate temperature. However, the use of elemental Hg as a source does require the use of a hot wall reactor to prevent Hg condensation.

A final material consideration which restricts the growth temperature is the surface mobility of the absorbed Hg and Te atoms on the growth surface. The absorbed atoms must have sufficient mobility and time to move on the surface to an appropriate crystal site before being immobilized or trapped by the subsequent deposition of additional atoms. Low surface mobilities and high deposition rates tend to yield poor epitaxial growth. Extremely low surface mobilities can lead to deposition of amorphous material, as in the plasma deposition of silicon. Surface mobility, as with bulk diffusion, typically has an exponential dependence on the reciprocal temperature, characteristic of activated processes ($\alpha e^{-\beta/T}$). High quality epitaxial layers were obtained in this study, indicating sufficient surface mobility at the growth temperatures used here.

The effects of the various growth parameters and the resulting device structure must also be considered. An ideal heterojunction

in this study would possess a perfectly abrupt interface between the CdTe and HgTe. The degree of abruptness present at the HgTe - CdTe interface is determined by the extent of the interdiffusion which takes place between the two materials. HgTe and CdTe are completely miscible, forming a solid solution at all compositions of $Hg_{1-x}Cd_xTe$. Interdiffusion between HgTe and CdTe has been found to be quite rapid at low temperatures [22]. Interdiffusion at the heterojunction interface can lead to a reduction in the heterojunction Schottky barrier height. If there is a slow compositional grading between the two materials, the built-in potential, which results from the difference in electron affinities between HgTe and CdTe, is screened by the mobile charge carriers in the CdTe.

The grading of the electron affinity present in an interdiffused heterojunction is analogous to a graded p-n junction. In a graded p-n junction, the built-in potential, which is derived from the difference in work functions of the p and n regions (Fermi level position in the energy gap), is reduced from the value found in abrupt junction. The slow change in work function over the graded region is screened by mobile carriers. The reduction in built-in voltage from that found in the perfectly abrupt junction is dependent on the impurity gradient at the junction [23].

The band bending in a heterojunction, resulting from the electron affinity difference, will be reduced from that present in an abrupt junction when the interdiffusion distance is on the order of

the Debye screening length of the material. The interdiffusion distance, x, is given by $x = \sqrt{Dt}$, where D is the chemical diffusion coefficient of the HgTe - CdTe system and t is the growth time in this case. Oldham and Milnes [24] have shown that for rectification to occur in a n-n heterojunction the interdiffusion distance must satisfy

$$\sqrt{Dt} < L_D \left(\frac{\Delta\chi}{6\sqrt{3}\, k_B T} \right)^{\frac{1}{2}} \qquad (5.4)$$

where $\Delta\chi$ is the difference in electron affinities, T is the absolute temperature, and L_D is the Debye screening length. The Debye length is given by

$$L_D = \left(\frac{k_B T\, \varepsilon\, \varepsilon_o}{q^2 N_D} \right)^{\frac{1}{2}} , \qquad (5.5)$$

where $\varepsilon\, \varepsilon_o$ is the permittivity of the semiconductor and N_D is the donor dopant concentration. The Debye length of CdTe is approximately 800 Å for a doping concentration of $N_D = 10^{15}$ to $10^{16} cm^{-3}$. The diffusion length must be less than 1400 Å for rectification to occur using a $\Delta\chi$ obtained in this study of $\Delta\chi \simeq 0.8$ eV. The interdiffusion distance of HgTe and CdTe must be confined to a tenth of this distance for a negligible decrease in the observed barrier height. The

interdiffusion rate was measured by Almasi and Smith [22] at elevated temperatures, 450° and 630° C. The extrapolated interdiffusion data yield an interdiffusion distance of 100 Å for a typical growth temperature of 325°C and growth period of 20 minutes. This short interdiffusion distance ensures that the compositional grading should have a minor effect on the measured barrier height.

The need to minimize the interdiffusion of HgTe and CdTe was one of the main motivations for finding a low temperature growth technique in this study. The temperatures typically encountered in the LPE growth of $Hg_{1-x}Cd_xTe$ using a Te solvent are 500° - 600°C [13]. A growth period of 10 minutes would lead to an interdiffusion distance of over 7000 Å, clearly exceeding the limit for a rectifying junction for similar doping and $\Delta\chi$ considered in this study.

C. METAL ORGANIC CVD GROWTH OF HgTe

The crystal growth was undertaken in a horizontal silica hot wall reactor 3 cm in diameter, heated in a two-zone resistance furnace. This is shown schematically in Fig. 5.1. The left-zone of the furnace was used to control the temperature of a boat of elemental Hg (triple distilled) which served as the source of Hg vapor. The Hg vapor pressure in the reactor was regulated by controlling the Hg source temperature. The left zone was also used to heat the source of Cd vapor utilized in the annealing procedure to be described below. The Cd source was elemental Cd (6-9's purity) which

$$(CH_3)_2\,Te + Hg + H_2 \rightarrow HgTe + 2CH_4$$

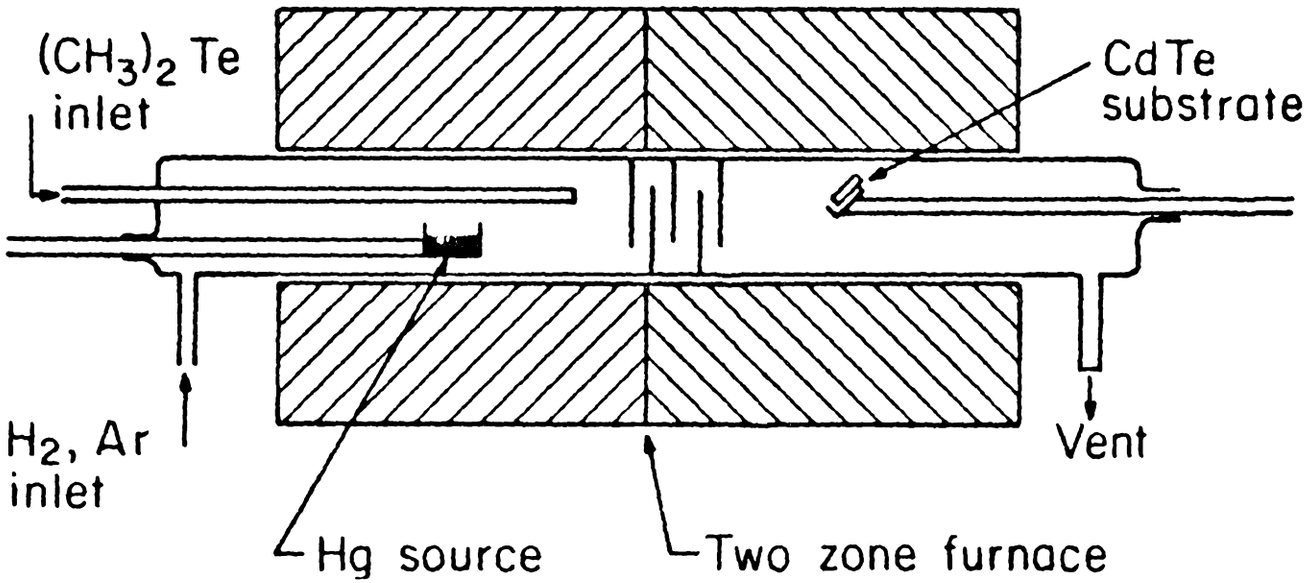

Figure 5.1. A schematic diagram of the CVD reactor used in this study. The mercury source and substrate holder may be moved inside the reactor.

had been etched in dilute HNO_3 (<10% HNO_3 in distilled H_2O) in order to clean the Cd surface. The right zone controlled the substrate temperature.

The Hg and Cd source boats and the substrate holder were mounted on quartz rods which could be moved into and out of the furnace. The rods were fed through close fitting teflon bushings in the end-caps of the reactor, minimizing the diffusion of oxygen into the reactor during growth.

DMT vapor was supplied by bubbling hydrogen through liquid DMT held at room temperature. The DMT vapor was introduced downstream from the mercury source to prevent surface contamination of the Hg. Typical H_2 flow rates through the DMT were 10-40 cc/min during the growth period. Quartz baffles were installed in the reactor to ensure good mixing of the Hg and DMT vapors prior to reaction. The hydrogen used as a carrier gas was purified in a Pd-purifier and passed through a liquid nitrogen cold trap before entering the reactor. The apparatus operated at atmospheric pressure with total hydrogen flow rates of 0.4 - 0.6 ℓ/min. The hydrogen had less than 0.5 ppm of H_2O which prevented any oxidation of the Hg and Cd source from the carrier gas and could reduce oxides which may be present initially on the sample surface.

Substrates of <110> CdTe were prepared by cleaving bulk single-crystals of CdTe in air. The <110> CdTe substrate was used in most

of this study due to the ease of sample preparation. However, substrates of <111> A CdTe etched in 1% bromine in methanol were also used. Most of the measurements were made on n - CdTe substrates doped with 10^{17}-10^{18} In. Substrates of undoped CdTe were also used. All substrates were obtained from the Eagle Picher Corp. The undoped substrates were cut into square rods 2 mm on a side, then annealed at 750°C for 8 hours under a Cd pressure of about 650 torr. This treatment reduced the bulk resistivity to $\simeq$0.8 Ω-cm.

After preparing the sample surface by air cleaving or etching, the substrate was immediately placed into the CVD reactor. The CdTe substrate was annealed in the reactor under a H_2 atmosphere for 30 - 180 minutes at typically 325 - 350°C prior to the HgTe growth. An alternate annealing procedure consisted of annealing the substrate under a H_2 atmosphere containing Cd vapor. The Cd vapor was supplied by the metal Cd source. The Cd source was always held at temperatures greater than 325° to ensure a molten Cd source, but 2° - 5° C lower than the substrate temperature. An annealing step was found necessary to ensure good epitaxial growth of the HgTe. Sample substrates which had been chemically etched required a longer annealing time than the air cleaved samples in order to achieve epitaxial growth of the HgTe.

After the annealing treatment the growth of the HgTe was initiated by heating the Hg source to 270° - 300°C followed by the

introduction of DMT into the growth reactor. The Cd source was removed after the introduction of DMT into the reactor. Cd vapor and DMT react readily to form CdTe. Failure to remove the Cd source resulted in the quenching of DMT from the carrier gas and subsequently no growth of HgTe occurred on the sample substrate. The substrate temperature was typically 325 - 350°C during the growth period which lasted 10-120 min. This procedure gave growth rates of 0.3 to 0.6 μ/hr. After the growth period, the sample was quickly pulled from the furnace hot zone to prevent thermal decomposition of the HgTe layer. The growth procedure used here should not be considered to be optimal without further experimentation. Higher growth rates may be possible.

The growth of the alloy $Hg_{1-x}Cd_xTe$ was also attempted unsuccessfully in this reactor by the introduction of Dimethyl Cadmium, $(CH_3)_2Cd$, into the reactor during the growth period. The reaction of DMT and Dimethyl Cadmium proceeds rapidly at low temperatures, preventing the use of a hot wall reactor. The use of elemental Hg as a source of Hg vapor requires a hot wall reactor arrangement to prevent Hg condensation in the reactor. Dimethyl mercury could serve as an alternative source of Hg for use in a cold wall reactor in the growth of $Hg_{1-x}Cd_xTe$.

D. CHARACTERIZATION OF THE HgTe LAYERS

The HgTe layers grown in this study were examined by helium back-scattering and channeling measurements and glancing angle x-ray diffraction. The growth morphology of the HgTe layers was examined by scanning electron microscopy (SEM).

A variety of growth morphologies were observed, depending on the substrate crystal orientation, substrate crystal quality, and growth conditions. A typical HgTe growth on a <110> cleaved surface is shown in Fig.5.2. Figure 5.2 (a) shows a HgTe layer grown over a tilt boundary in the CdTe substrate. This is evident in the surface morphology of the HgTe layer. Small terraces on the HgTe surface are found to be oriented along specific crystal directions in the substrate. Figure 5.2 (b) shows an enlarged view of the HgTe surface. This reveals the faceting which occurs on the growing layer. This faceting may imply that the cleaved crystal face may not be the preferred growth direction. In LPE studies, the <111> A CdTe surface has been found to be the optimal surface for growth of $Hg_xCd_{1-x}Te$ [9], while previous vapor phase growth studies found the highest growth rate on the <111> B CdTe surface [8].

Smoother growth morphologies than shown in Figure 5.2 were achieved on the <110> cleaved surface as seen in Figure 5.3. The HgTe layer, shown growing over a cleavage step on the substrate

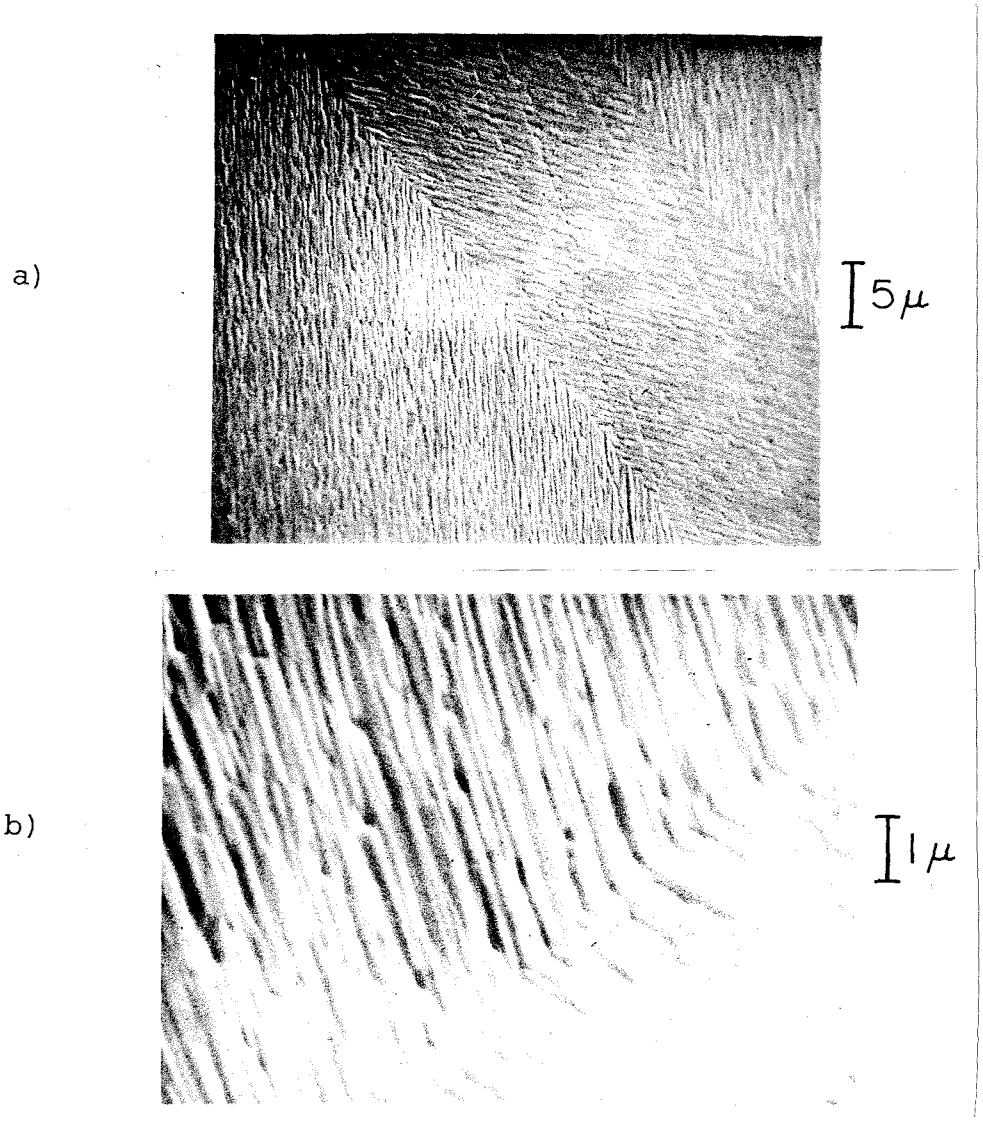

Figure 5.2. HgTe layer grown on a <110> cleaved CdTe surface.
(a) HgTe layer grown over a tilt boundary in the substrate.
(b) A higher magnification view reveals the faceting which occurs on the growing layer. The small terraces are orientated along specific crystal directions in the substrate. The SEM views are inclined 60° from the normal.

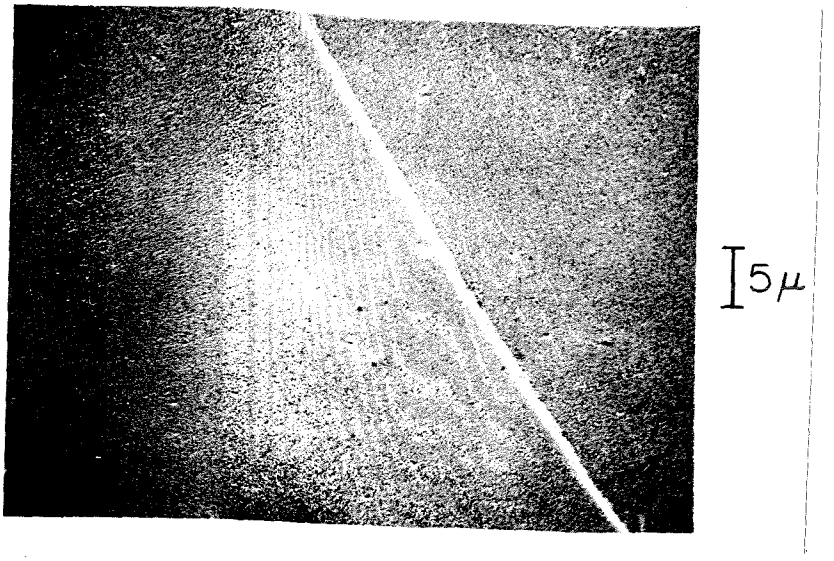

Figure 5.3. Hg Te layer on a <110> CdTe substrate possessing a smooth growth morphology. This layer was grown over a cleavage step in the substrate surface. Growth morphology was found to be partly dependent on substrate quality.

surface, is very smooth with little or no surface relief. The occurrence of different growth morphologies was found to be partly dependent on the quality of the substrate material. Rough surface morphologies were usually found on substrates of poor crystalline perfection.

The growth morphology on the <111> A surface of the CdTe is shown in Figure 5.4. On this surface, the HgTe exhibits a triangular relief, characteristic of the symmetry of the underlying substrate. The <111> B face was not investigated.

Since the growth morphology indicated epitaxy growth, Rutherford helium backscattering measurements were made to determine the degree of crystalline perfection present in the epitaxial layer. In the helium backscattering experiment, a beam of 1.5 MeV helium ions, $^4He^+$, impinges on the substrate and the energy distribution of the backscattered particles is measured at an angle of 170° from the direction of the incident beam. A typical backscattering spectrum of HgTe layer is shown in Figure 5.5. The curve labeled random corresponds to the case where the substrate is randomly aligned with respect to the ion beam. The high energy peak in the spectrum is due to scattering off the HgTe layer while the broad low energy part of the spectrum corresponds to scattering off the CdTe substrate. The thickness of the HgTe layer is easily obtained from the energy width of the HgTe peak [25]. The curve labeled

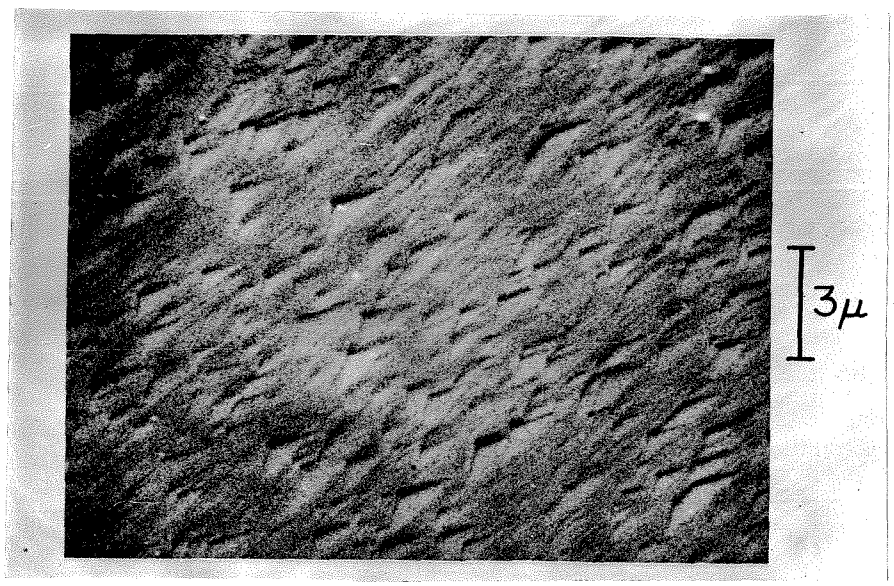

Figure 5.4. The HgTe layer grown on a <111> A CdTe substrate. The growing layer exhibits a triangular relief, characteristic of the underlying substrate. The polarity of the substrate was determined by chemical etching techniques [27].

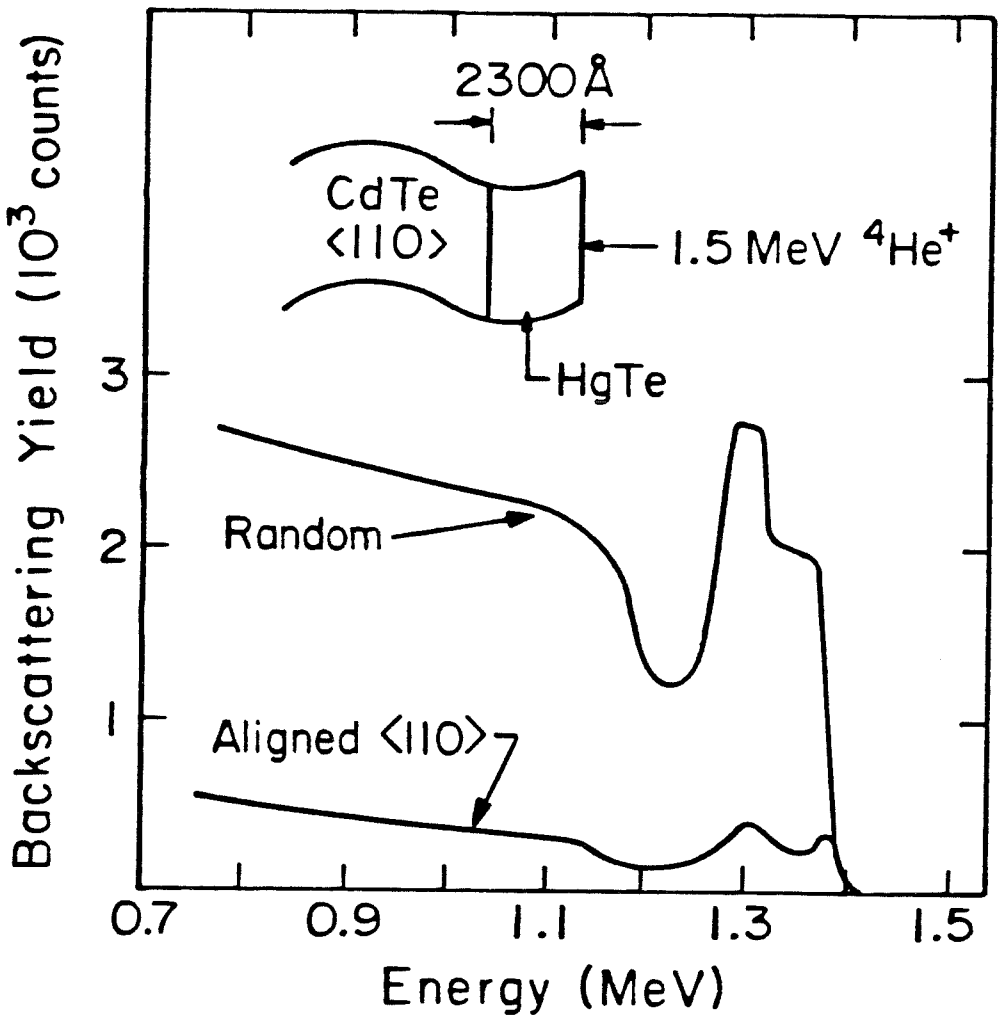

Figure 5.5. The 1.5 MeV $^4He^+$ backscattering spectra of epitaxial HgTe layers. The random spectrum was used to determine the thickness of the HgTe layer. The aligned <110> spectrum indicates good epitaxial growth.

"aligned <110> " in Figure 5.5 is the channeling spectrum of the HgTe layer. In this case, the ion beam is aligned along the <110> axis of the CdTe substrate. The yield of backscattered particles is reduced, since the helium ions are channeled between the rows of atoms in the crystal. The ratio of the height of the HgTe peak in the channeled spectrum to random spectrum (χ_{min}) gives an indication of the crystal perfection of the HgTe layer which in this case is very good with χ_{min} = 10 - 15% and indicates good expitaxial growth.

The thickness and hence the growth rate of the epilayer can be monitored by this technique. In Figure 5.6, the HgTe peak from the random spectrum taken on two different growths is shown. The thicker film was grown with twice the vapor pressure of DMT in the reactor than in the case of the thinner layer. The growth rate was found to be proportional to the DMT pressure under the growth conditions used here. The variation of Hg pressure, obtained by changing the Hg source temperature, did not change the growth rate of the HgTe for a given DMT pressure. The Hg source temperature was varied from 250° - 300°C. This corresponds to a range in Hg vapor pressure from 73 torr to 240 torr.

E. ELECTRICAL MEASUREMENTS -- METHODS AND RESULTS

The samples were first prepared for the electrical measurements by making ohmic contact to the CdTe substrate with In-Ag solder

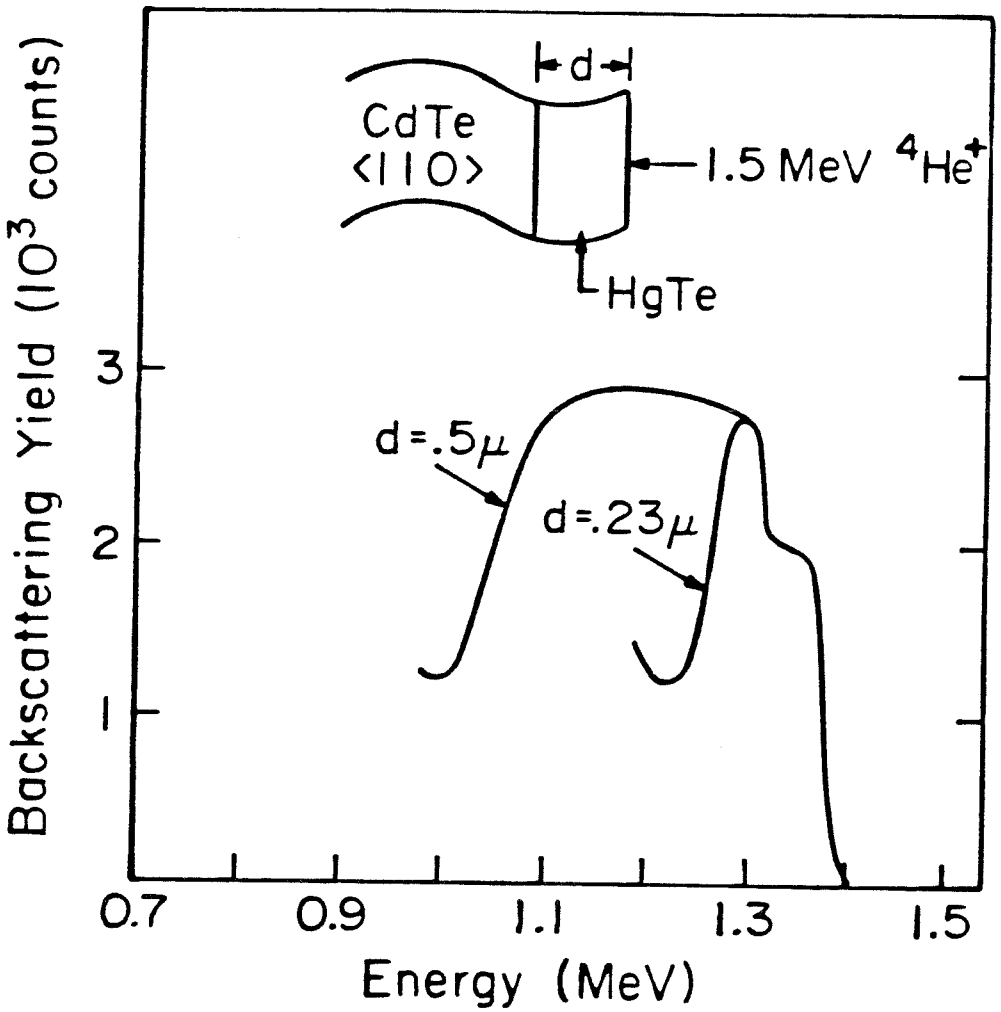

Figure 5.6. The HgTe peak of the random backscattering spectrum taken on two different growths. The growth rate was obtained from the energy width of the HgTe peak.

(90% In: 10% Ag.). Circular areas were defined on the HgTe surface by conventional photolithography techniques. Mesas were then formed by etching the HgTe layer in 1% Br in methanol. This procedure gave circular diode structures having an area between 1.4 - $2.0 \times 10^{-4} cm^2$. Contact was made to the HgTe layer by a Au pressure contact.

These structures were then used in the subsequent room temperature measurement of the forward bias current voltage characteristic, the reverse bias capacitance voltage characteristic, and the diode photoresponse.

The forward bias current voltage characteristic was measured over 3 - 4 decades of current. The measured characteristic was fitted to equation 2.1. Two typical measurements are shown in Figure 5.7. The data labeled "H_2 anneal" were taken on a diode where the CdTe substrate was annealed at 335°C for 30 minutes in a pure H_2 ambient prior to the growth of the HgTe layer. The data marked "H_2 and Cd vapor anneal" corresponds to a structure grown on a CdTe substrate which had a pre-growth anneal of 5 - 10 minutes at 338°C in H_2 gas which had flowed over a molten Cd source held at 337°C. Substrates receiving a shorter anneal time than 30 minutes in pure H_2 yielded characteristics which would lie between the two curves shown. Only diodes with a quality factor less than $n \leq 1.2$ were investigated further. The photoresponse was measured

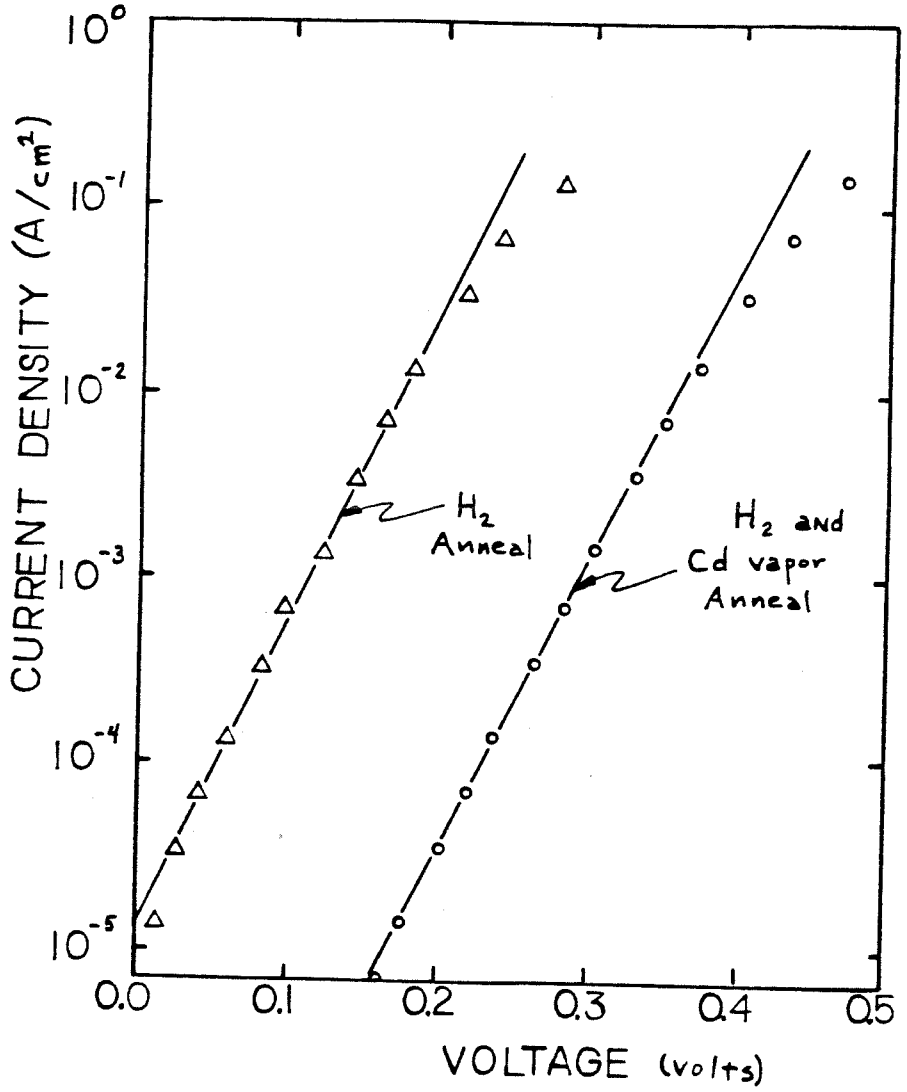

Figure 5.7. The forward bias current-voltage characteristics of the HgTe-CdTe heterojunctions studied here. The current characteristic and the deduced barrier height was dependent on the substrate annealing treatment performed prior to the growth of HgTe.

on these structures by illuminating the HgTe - CdTe interface through the CdTe substrate. The cube root of the photoresponse per incident photon is shown as a function of photon energy in Figure 5.8. The cubic dependence of the photoresponse has been observed for the emission of electrons from a semiconductor into vacuum [26]; $\beta = 3$ in Equation 2.4. The data shown in Figure 5.8 were taken on the structures used in Figure 5.7. The barrier heights derived from the photoresponse measurements agree well with values deduced from the current voltage measurement. These measurements also indicate an increased barrier height found in samples annealed in H_2 containing Cd vapor.

Capacitance measurements were made on the diode structures as a function of reverse bias voltage using a Boonton capacitance meter. The capacitance data, taken on the structures used in Figures 5.7 and 5.8, are shown in Figure 5.9. The data shown exhibit a deviation from the expected result for a Schottky structure. In a Schottky barrier diode with uniform substrate doping, the capacitance characteristic would be given by a straight line on Figure 5.9. While these measurements cannot be used to determine a barrier height, the capacitance measurement does indicate that there are changes in the electrical properties of the CdTe substrate with depth which probably develops during the annealing and possibly during the HgTe growth itself.

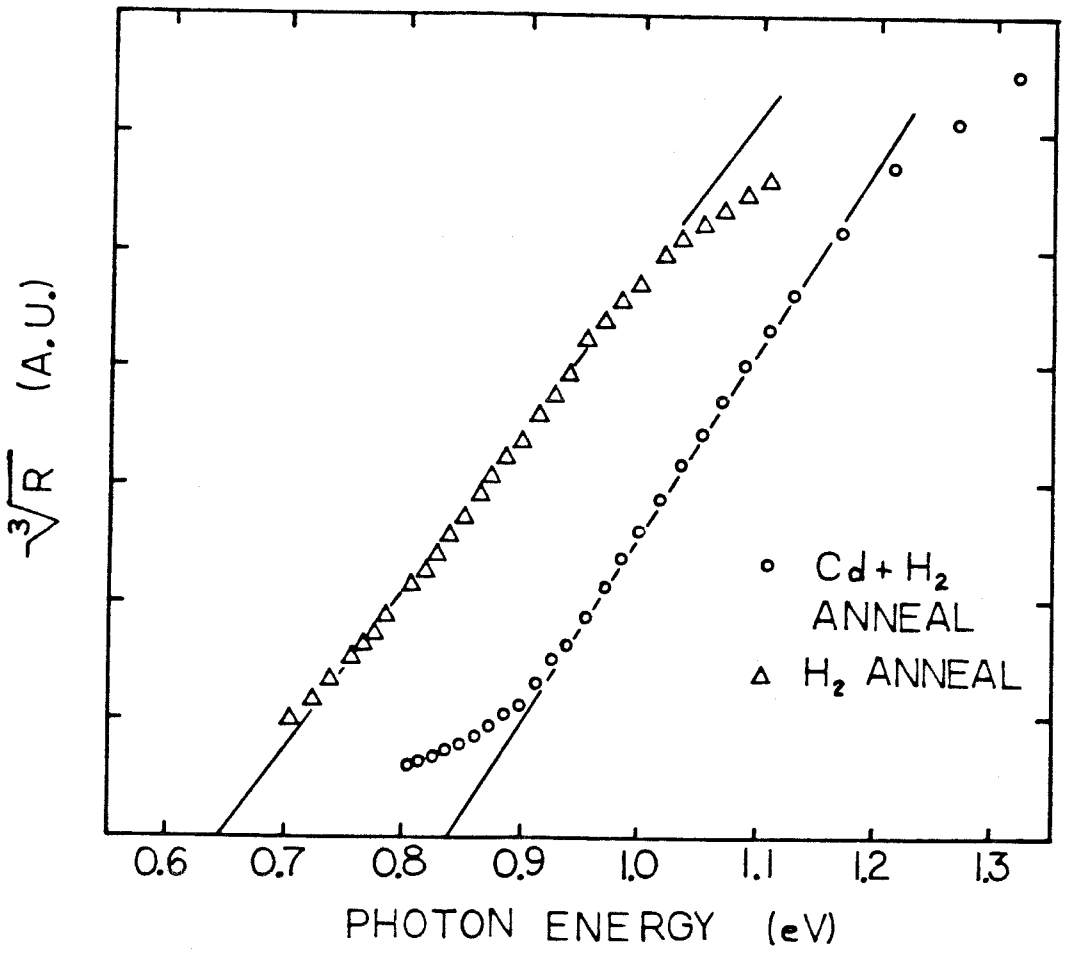

Figure 5.8. The photoresponse, R, as a function of incident photon energy measured on HgTe-CdTe heterojunctions.

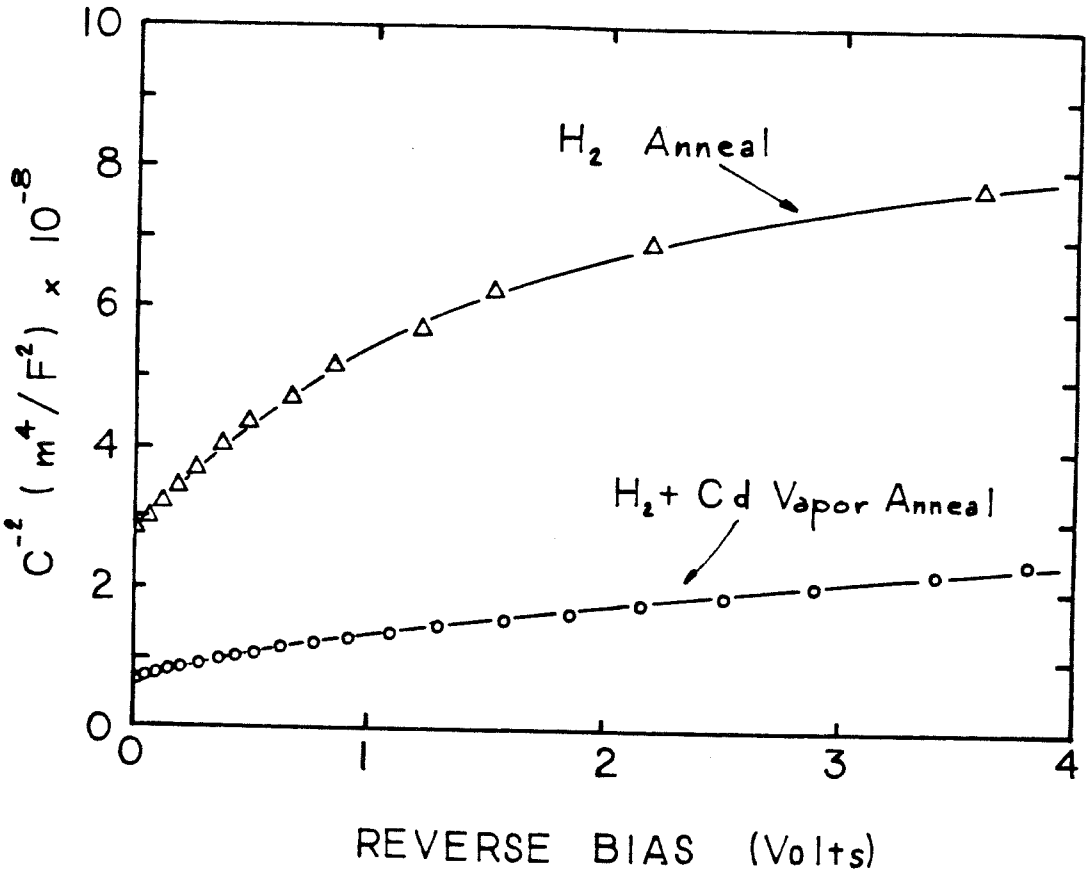

Figure 5.9. The measured capacitance as a function of reverse bias voltage. The use of a H_2 annealing ambient appears to produce compensation in the CdTe substrate. The addition of Cd vapor into the annealing atmosphere reduces the amount of compensation present.

Systematic trends evident in the measured capacitance characteristics can be correlated with changes in the substrate annealing conditions. As the annealing conditions are changed from the H_2 plus Cd vapor ambient to a pure H_2 ambient, and as the duration of the H_2 only anneal increases, the capacitance of the structures at zero applied decreases. This effect is accompanied by a decrease in the space charge concentration deduced from the slope of the curve at zero bias, using Equation 2.7. The space charge on donor concentration decreases from the pre-annealed value of 10^{17} to 10^{18} per cm^3 to less than 10^{15} per cm^3. There is also noted an increase curvature in the data shown in Figure 5.9 with the above sequence of annealing conditions.

The dependence of barrier height on the carrier concentration, deduced from the capacitance characteristic at zero bias is shown in Figure 5.10. The Cd vapor annealed substrates yielded the larger barriers and higher deduced carrier concentration.

Other Schottky barrier structures on CdTe substrates were also investigated in order to further study the effects of the annealing procedure on the CdTe substrates without the complications due to the subsequent growth and interdiffusion of the HgTe.

Au Schottky barrier structures were formed on substrates of In doped CdTe (10^{17} - $10^{18}/cm^3$) which had been air cleaved and then annealed in pure H_2 for varying lengths of time at the HgTe growth

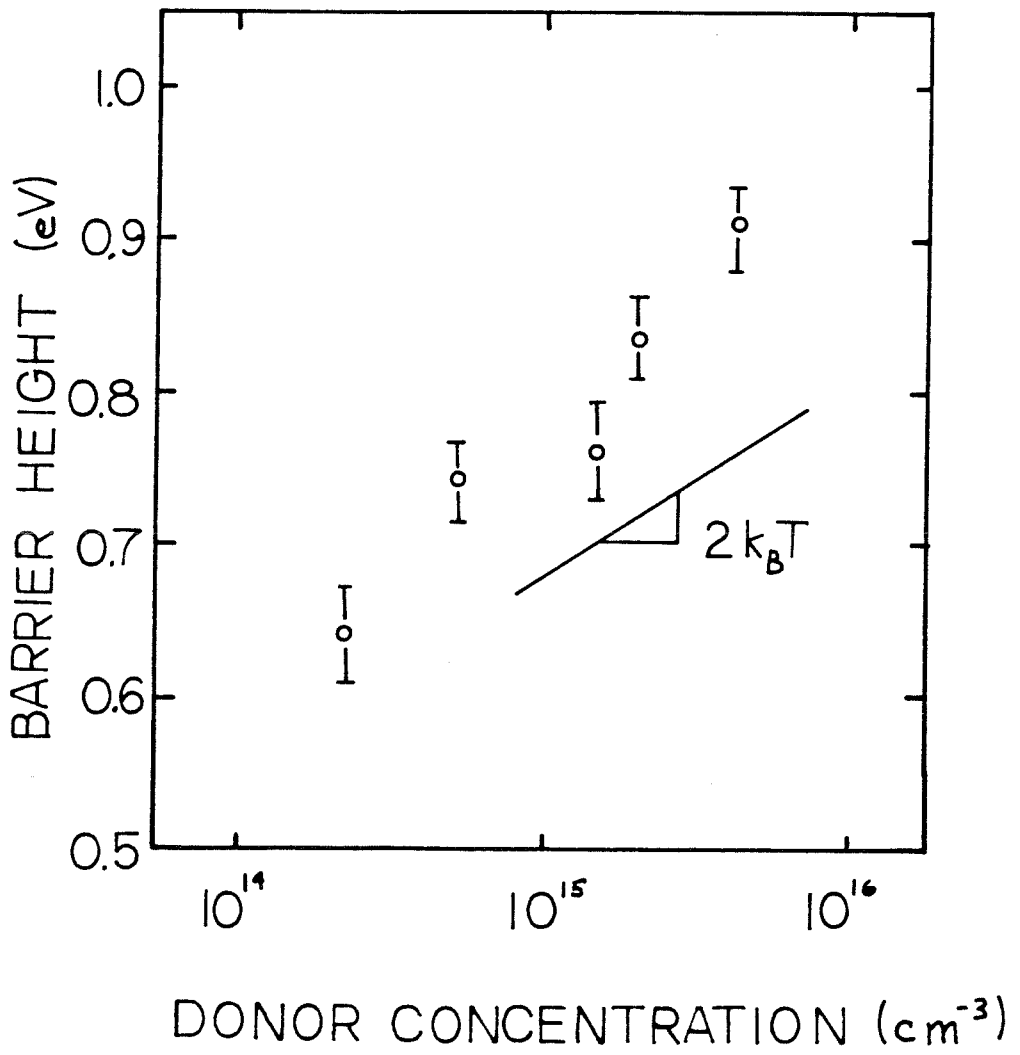

Figure 5.10. The barrier height deduced from the I-V and photoresponse measurements was found to increase with the effective donor concentration. An effective donor concentration in the sample was assigned from the value of the slope of the measured capacitance characteristic at zero bias.

temperature ($\sim$ 330°C). These structures were made by evaporating Au dots onto the annealed CdTe surface in an ion pumped vacuum system. The I - V and capacitance characteristic of the structures was then measured. Changes in the electrical properties of the near surface region of the CdTe resulting from the annealing treatment could be seen in these measurements. No change in the Au barrier height with annealling condition was noted within experimental error. Changes shown in these capacitance measurements with annealling treatment, similar to the trends found in the HgTe - CdTe structures can be noted in Figure 5.11. There is again a decrease in both the zero bias capacitance and donor concentration with the longer annealing times in pure H_2. The Au Schottky barrier structures do however have a deduced carrier concentration greater than that observed in the HgTe - CdTe structures for identical CdTe substrate annealing conditions. This may indicate that additional compensation in the CdTe substrate may be occurring during the epilayer growth.

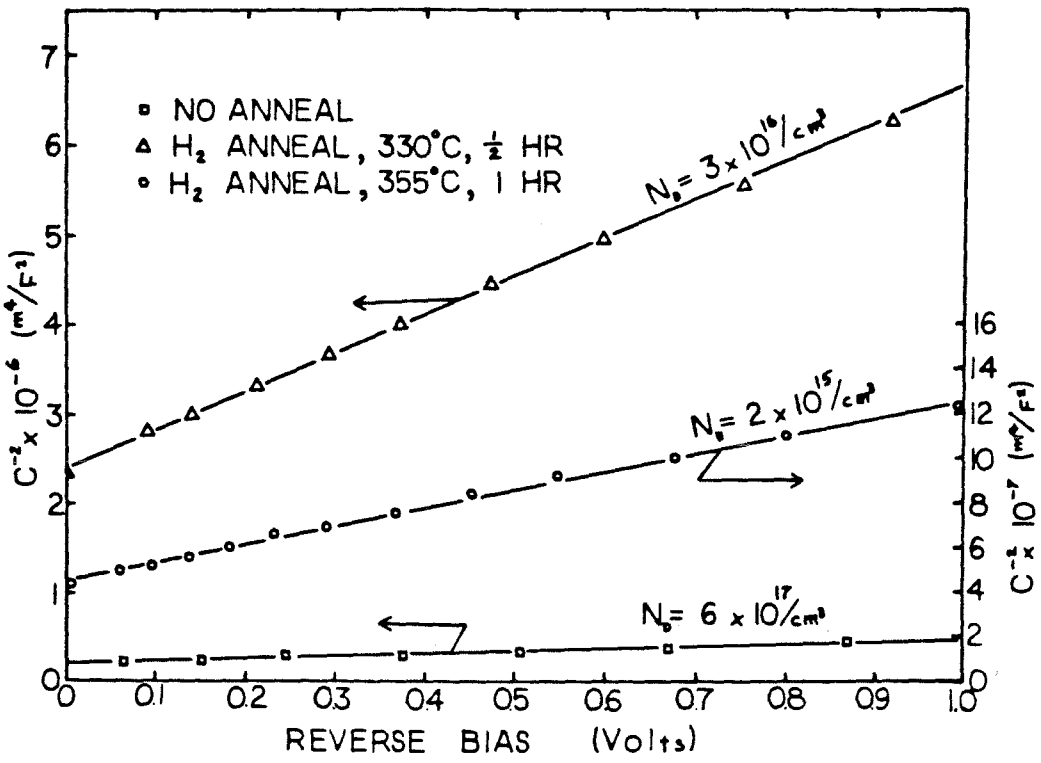

Figure 5.11. Capacitance characteristics measured on Au Schottky barriers formed on H_2 annealled CdTe substrates. A decrease in the measured donor concentration, N_D, is found in substrates annealed at the HgTe growth temperature (325-350°C).

F. TWO MODELS OF THE HgTe-CdTe HETEROJUNCTION

The barrier height measured on the HgTe-CdTe heterojunctions indicate a barrier height which can vary from 0.65 to .92 eV depending on the annealling conditions utilized prior to the HgTe growth. The highest barrier height obtained in this heterojunction appears to be substantially less than that expected for this structure from the models and observations noted in the introduction to this chapter. It is therefore important, not only to understand the deviations from the simple predictions made of the HgTe-CdTe heterojunction but also the dependence of the barrier height on annealing conditions. It would then be hoped that further increases in the barrier height may be possible by additional changes in the growth technique.

This section will first discuss the changes in the electrical properties of the CdTe substrates due to the annealling conditions. Two models of heterojunction behavior will then be presented which are consistent with the measurements made here.

i. Annealling effects in CdTe

In the discussion of Chapter 4 it was pointed out that annealling treatments on CdTe carried out under conditions of low Cd activity can produce compensation in both In and undoped n-type material. This observed compensation is attributed to the introduction of Cd vacancies, which are known acceptors. These Cd vacancies can be complex with In or native defect donors reducing the carrier concen-

tration [28-29]. The equilibrium carrier concentration is determined by the Cd activity (vapor pressure) and temperature.

The growth technique used here, utilizing a pure H_2 ambient during the anneal, leaves the Cd activity undefined due to the total absence of Cd in the H_2 atmosphere. The CdTe will experience a loss of Cd under such conditions in an effort to provide the minimum Cd pressure required for the phase stability of the compound at the given temperature. It is this loss of Cd from the substrate which results in the diffusion of Cd vacancies into the substrates. The inclusion of Cd vapor into the annealing atmosphere fixes the Cd activity over the CdTe substrate. The presence of Cd activity inhibits the Cd loss from the substrate resulting in less compensation with a resulting higher measured carrier concentration in the near-surface region.

The Cd vacancy is one type of defect which is being created as a result of the annealing treatment. Other defects, both acceptors and donors may be and probably are generated during the anneal. These additional defects may form deep levels in the energy gap of the semiconductor [31]. These deep levels can affect the electrical behavior of the CdTe.

The possible defect related changes in annealed CdTe can affect the measurement of the Schottky barrier height. Two separate models of the HgTe-CdTe heterojunction which incorporate the influence of these defects are found to be consistent with the observations in this study. The first model to be discussed considers the effect of deep

levels introduced into the CdTe on the Schottky barrier while the second model will consider the effect of this defect-induced compensation and minority carriers on a heterojunction possessing large Schottky barrier heights.

ii) Deep Levels and Schottky Barrier Formation

A model of Schottky barrier formation, mentioned previously, postulates that deep levels derived from crystal defects, which may be introduced in the annealing process, serve to pin the Fermi level at the HgTe-CdTe interface. In order to accommodate the difference in electron affinities correctly, these states would have to be deep donor levels.

As described in Chapter 2 and Appendix 1, these deep levels can produce curvature in the measured capacitance with reverse bias similar to that seen in Figure 5.7. The degree of curvature is dependent on the details of the measuring process. The change in annealing procedure could alter the defect structure of the near-surface region of the CdTe which may in turn change the concentration and even the type of deep level present. A different measured barrier height reflects this change in deep level structure. The presence of more than one deep level, which possesses broad energy distributions, could explain the continuous change in barrier height with annealing conditions seen in Figure 5.11.

The complicated dependence of capacitance on the physical properties

and spatial distribution of the deep levels require additional measurements in order to substantiate this model. Recent measurements, employing DLTS (Deep Level Transient Spectroscopy), on Au Schottky barrier formed on H_2 annealed CdTe indicate the presence of a deep donor level located approximately 0.7 eV below the conduction band edge [32]. This level is near the Fermi level position found in the HgTe-CdTe heterojunction made using similarly annealed substrates. It is possible that this state could determine the barrier height here.

iii) The Effect of Minority Carriers on Large Schottky Barrier Heights

An alternative view of the HgTe-CdTe heterojunction which is consistent with the observations and measurements of this study requires a more detailed examination of the information obtained in a particular measurement process. Estimates of the valence band discontinuity present at the HgTe-CdTe heterojunction predict a large barrier height. The model discussed in this section will assume that these simple predictions are correct and that there is only a small valence band discontinuity. Since large Schottky barrier heights are uncommon, there has been little experimental and theoretical work done on these structures. This section will discuss the modification of the simple theory of Schottky barriers necessary when interpreting measurements made on large Schottky barrier height structures.

In a Schottky barrier structure which has a barrier height close to the energy gap of the semiconductor ($\phi \simeq E_{gap}$), there are the additional complications in the interpretation of the electrical measurements due to the presence of minority carriers near the interface [33]. The effect of minority carriers becomes more evident as the Schottky barrier increases and the Fermi level is pushed closer to the valence band. The formation of an inversion layer may become possible in this case depending on the bulk donor concentration and actual barrier height.

The presence of an inversion layer will substantially change the band bending in the semiconductor from that predicted from the simple model of a Schottky barrier. The band bending in the case considered here is found by solving Poisson's equation:

$$\frac{d^2\phi}{dx^2} = -\frac{q}{\varepsilon\varepsilon_o}(N_D + p - n) \qquad (5.6)$$

where N_D is the background donor doping and p and n are the hole and electron concentrations, respectively. The simple model of the Schottky barrier commonly discussed excludes the effect of electrons and holes in the above equation. The solution of this equation is given in Appendix 2 for the case of an abrupt junction and uniform doping profile in the semiconductor.

The effect of minority carriers on the band bending profile is easily seen in Figure 5.12. The band profile given by the simple

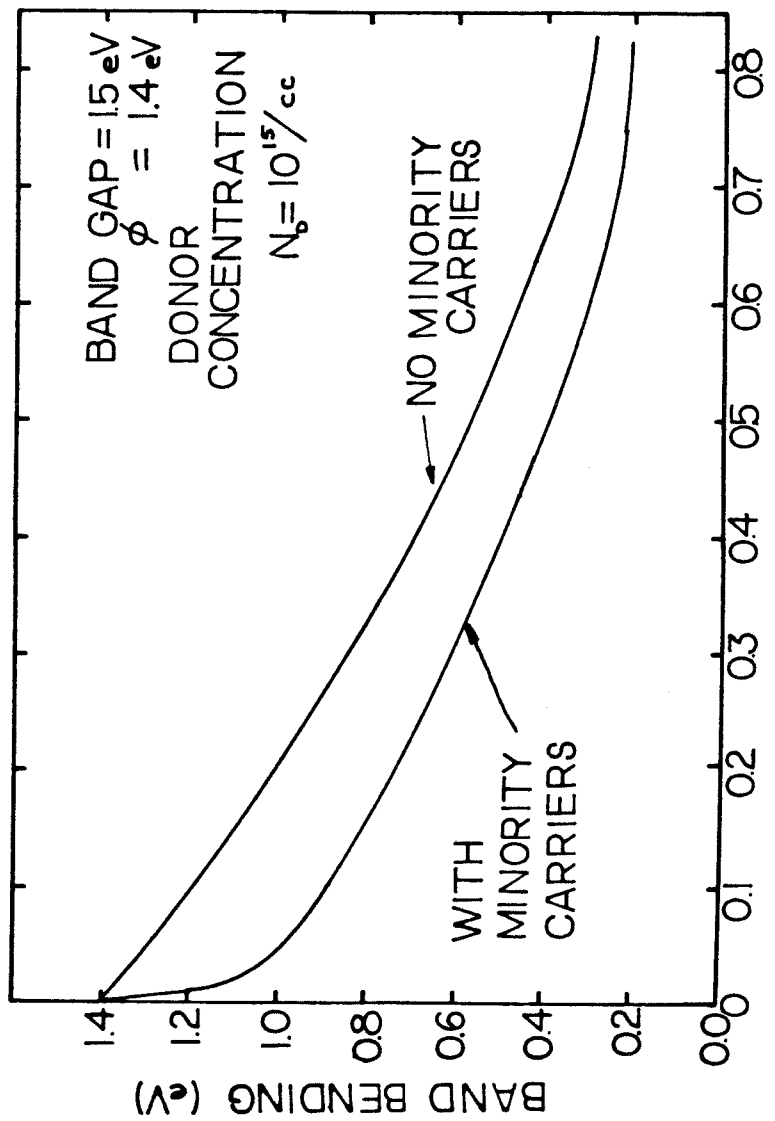

Figure 5.12. The calculated band bending profile in a large Schottky barrier height structure. The inclusion of the minority carriers into the calculated profile can alter the band profile from that predicted from the simple Schottky model (Equations 2.5-2.7).

Schottky model and that given by Equation 5.7 illustrated there. The zero of energy is taken to be the metal Fermi level and only the semiconductor conduction band is shown. Since the Fermi level is near the valence band edge ($\phi \simeq E_{gap}$), a high concentration of holes is then found near the interface. These holes cause a rapid band bending over narrow region in much the same way a high concentration of donor atoms would as illustrated in Figure 2.1.

The influence of the inversion layer on the band bending profile depends strongly on the semiconductor doping. The effect of minority carriers becomes more evident as the ratio of the fixed donor concentration to the valence band density of states decreases. An analogous situation is found in the MIS (metal-insulator-semiconductor) structure. The onset of inversion in the MIS structure approximately occurs when the applied bias pushed the Fermi level to a position ϕ_{INV} in the energy gap defined by:

$$\phi_{INV} = E_{gap} - 2k_B T \ln[N_C/N_D] \qquad (5.7)$$

where E_{gap} is the energy band gap, N_C is the conduction band density of states, and N_D is the fixed donor concentration [34]. In the Schottky barrier structure, the formation of an inversion layer is expected when the barrier height ϕ exceeds ϕ_{INV} ($\phi > \phi_{INV}$). The voltage, V_{EX}, given by $V_{EX} = \phi - \phi_{INV}$ is then primarily accommodated in the voltage drop occurring over the inversion layer of the semiconductor.

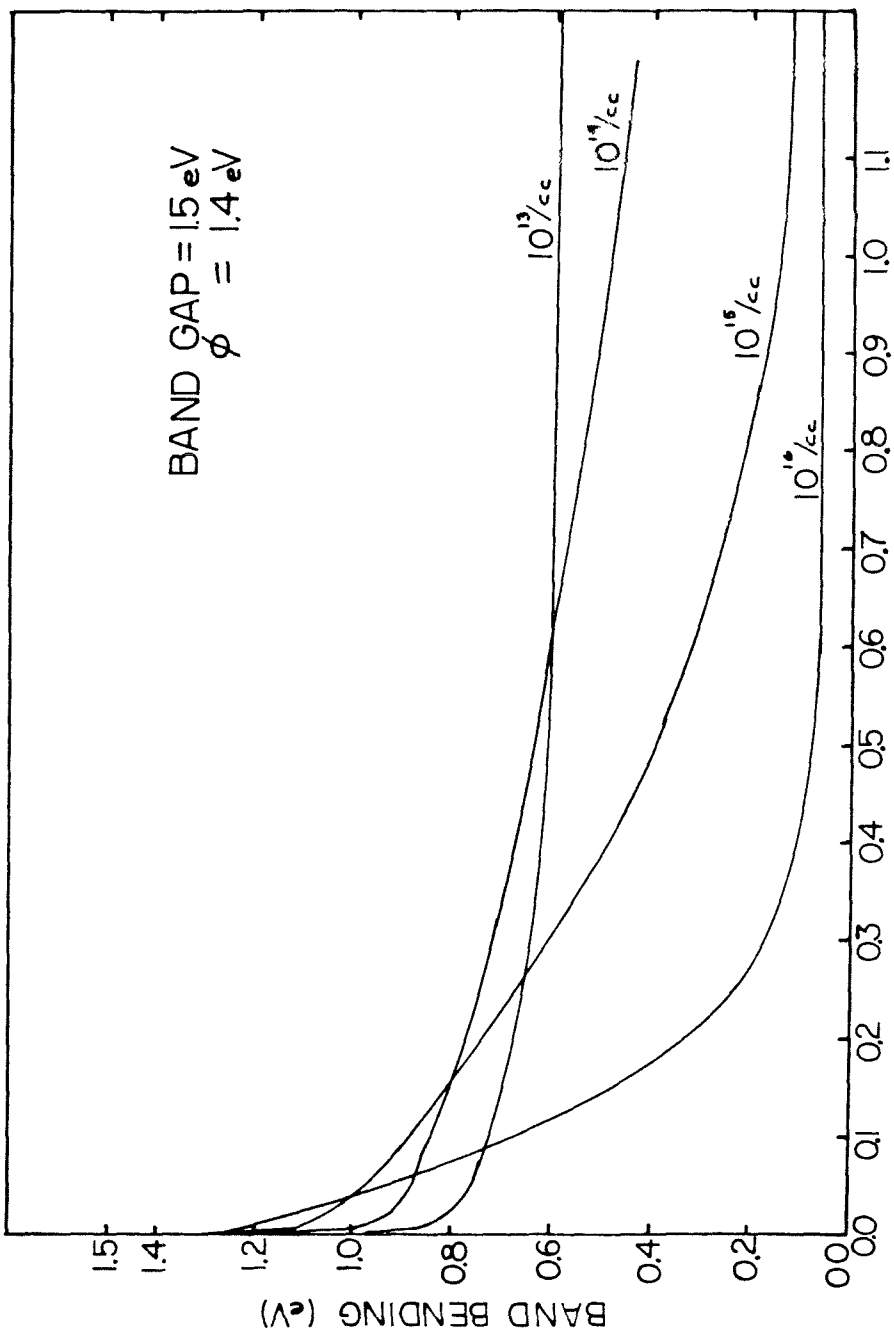

Figure 5.13. The band bending profile calculated from Equation 5.7 at various values of the substrate donor concentration. The effect of minority carriers becomes more pronounced in substrates containing a low impurity concentration.

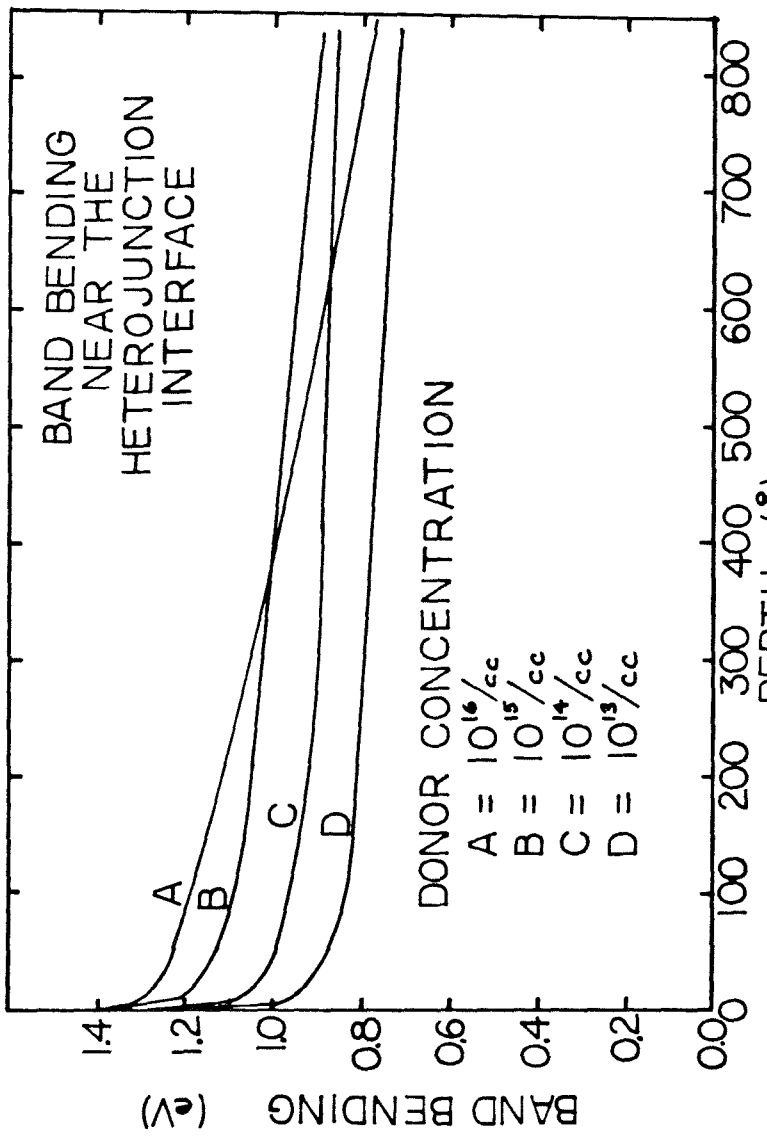

Figure 5.14. The band bending profile near an abrupt heterojunction interface. The barrier height and the energy band gap were taken to be 1.4 and 1.5 eV, respectively. The compositional grading occurring in actual heterojunctions will further reduce the measured barrier height of the structure.

The effect of the bulk donor concentration on the resulting band bending profile is illustrated in Figures 5.13 and 5.14. The band profile at zero bias was calculated from Equation 5.5. The zero of energy is again the metal Fermi level. It is seen in these figures that as the carrier concentration decreases a larger fraction of the barrier height voltage is supported by the inversion layer, as expected from Equation 5.7.

The rapid band bending occurring in a narrow region near the interface presents a potential spike through which electrons can easily tunnel in the electrical transport measurements. The barrier height measured in the I-V and photoresponse technique will then be lower than the actual barrier height present due to this tunneling effect. This again is similar to the case shown in Figure 2.1. The deviation of the measured barrier height from the actual barrier increases with the reduction in the donor concentration. This dependence is seen in Figure 5.11. If one assumes that the measured barrier height is proportional to ϕ given by Equation 5.5, the slope of the curve in Figure 5.11 should be equal to $2k_BT \ln 10$. This is indicated in that figure.

The compositional grading present across the HgTe-CdTe interface will affect the barrier height measured in the heterojunction by enhancing the effect of the minority carriers in the interdiffusion region. The grading in the band gap would then lead to further decreases in the measured barrier height.

The capacitance characteristic found in a large Schottky barrier height diode also exhibits deviations from the expression given for the simple Schottky diode in Equations 2.5 - 2.7. The capacitance characteristic in the model considered here shows a non-linear behavior similar to that found in Figure 5.8. It is difficult, however, to distinguish the capacitance curve deduced from the model presented in this section from that predicted for a structure with a spatially varying deep levels.

The effect of annealing the substrate on the measured barrier height can be understood in this model in terms of the compensation which occurs in the CdTe. The lowering of the carrier concentration due to Cd loss during annealing enhances the effect of the minority carriers at the junction producing a lower measured barrier height.

G. DISCUSSION AND SUMMARY

The two models discussed in the previous section relate changes in heterojunction fabrication procedure to the measured barrier height and capacitance. The basic difference between these two views can be seen by noting the Fermi level position at the interface as the growth procedure is altered. In the deep level model, the Fermi level position at the interface is changing with annealing conditions. The production of a new dominant deep level would yield a different Schottky barrier height. The second model states that while the

barrier height is large and independent of the annealing conditions, it is our ability to measure the actual barrier height that is impaired by defect related changes in the substrate material. The large barrier height postulated in this second model would however make this heterojunction attractive for use in a superlattice structure.

As pointed out, these two models would yield similar results in the electrical measurements available for this study, making a definitive determination of the actual physical situation present in the heterojunction impossible here. Other experiments on these structures may be able to discern between the two cases. The change in electron transmission rates through the thin tunnelling barrier should be evident in a sensitive photoresponse experiment. An accurate understanding of the internal photoemission data would require a more complete knowledge of the physical structure of the HgTe-CdTe interface and the resulting band bending profile [35]. The attainment of barrier heights higher than found in this study will require a greater control over the activities of all the chemical constituents present during the epilayer growth. This study has found that the substrate experiences a decrease in carrier concentration not only during the annealing but during the HgTe growth itself. This is seen by comparison to Au Schottky barriers on appropriate annealed CdTe substrates. If this donor compensation can be at-

tributed to a Cd loss from the substrate, the compensation occurring during the epilayer growth could be prevented by the growth of $Hg_{1-x}Cd_xTe$ instead of pure HgTe. The growth of $Hg_{1-x}Cd_xTe$ fixes the Cd activity in the epilayer, thus inhibiting the defect related effects from occurring during the epilayer growth. $Hg_{1-x}Cd_xTe$ remains a zero or negative band gap semiconductor for values of $x \leq 0.17$. The qualitative features of the lattice matched Schottky barrier structure should be present in such structures.

The use of a lower temperature growth technique will also suppress the production and diffusion of defects during the fabrication of the heterojunction. The formation of HgTe-CdTe heterojunctions by use of MBE (Molecular Beam Epitaxy) may permit crystal growth at temperatures below those used in the present CVD technique. MBE has provided a great degree of control over the physical structure of the growing crystal layer using the III-V semiconducting compounds (for example, see Ref. 36). This technique may allow a more definitive study to be made on this system.

In summary, this study has provided the first measurements of the electrical properties of an abrupt HgTe-CdTe heterojunction. The lattice matched Schottky barrier structure was grown by a new metal organic CVD technique which allows the epitaxial growth of HgTe on CdTe at low temperatures. The barrier height measured in these structures was found to be dependent on the details of growth

procedure utilized. Two models of the HgTe-CdTe heterojunction are proposed which relate changes in growth environment with the observed barrier height.

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APPENDIX 1

THE EFFECTS OF DEEP LEVELS ON THE MEASURED CAPACITANCE OF A SCHOTTKY BARRIER

It was noted in Chapter 1 that the presence of deep levels may affect changes in the capacitance measurements. While these effects have been utilized in probing the physical nature of deep levels by the use of admittance spectroscopy [1] and DLTS (Deep Level Transient Spectroscopy) [2-4], deep levels can complicate the interpretation of capacitance measurements which are used in determining the Schottky barrier height. The purpose of this appendix is to present a simple calculation of the capacitance characteristic for a Schottky barrier structure possessing a deep donor located at the Fermi level pinning position at the metal semiconductor interface. It will be shown that curvature in the capacitance characteristic similar to that seen in Figure 5.9 may be found in Schottky barriers possessing a deep donor level.

The depletion region of a Schottky diode which possesses both a deep and a shallow donor level can be divided into two regions. The region near the metal semiconductor interface contains a positive space charge which consists of both ionized deep levels and ionized shallow donors. Near the depletion region edge a second region is found where the space charge is due to only ionized shallow donors.

The built-in and applied voltage, V_{bi} and V, respectively, are related to the concentration of deep levels, N_t, and shallow im-

purities, N_D through the solution of Poisson's equation. This relation can be expressed by

$$V_{bi} - V = \frac{q}{2\varepsilon\varepsilon_o} [N_D w^2 + N_t (w-\lambda)^2] \quad , \qquad \text{(A1.1)}$$

where $\varepsilon\varepsilon_o$ is the semiconductor permittivity, w is the depletion region width, and λ is a constant given by

$$\lambda = \left(\frac{2\varepsilon\varepsilon_o}{N_D} |E_f - E_t|_{bulk} \right)^{\frac{1}{2}} \quad . \qquad \text{(A1.2)}$$

The quantity of $|E_f - E_t|_{bulk}$ is the energy difference between the Fermi level and the deep level position in the gap within the bulk semiconductor. These relations are derived in detail in Chapter 4 of Reference 5. The voltage, V, in Equation (A1.1) is assumed to be a DC or low frequency bias, where the frequency is much less than the emission or capture rates of the deep level.

In a typical capacitance measurement, a small high frequency (1 - 20 MHz) test voltage, V_s, is superimposed onto the bias voltage. Due to the high frequency of the test voltage the measured differential capacitance will only reflect the change in space charge due to the shallow donor levels. The capacitance is given by:

$$C = qN_d \frac{\partial w}{\partial V_s} \quad . \qquad \text{(A1.3)}$$

From Equation (A1.1), the required derivative in (A1.3) is found to be

$$\frac{\partial w}{\partial V_s} = \frac{\varepsilon\varepsilon_o}{qN_d w} \tag{A1.4}$$

and the width of the depletion region is found to be

$$w = \frac{\varepsilon\varepsilon_o}{C} \quad . \tag{A1.5}$$

The measured capacitance as a function of DC bias voltage can then be found by substituting w from Equation (A1.5) into Equation (A1.1).

Model characteristics can be used for comparison to the capacitance measured on the heterojunction in Chapter 4. The case of interest would locate the deep level at an energy below the conduction band in the semiconductor equal to the measured Schottky barrier height. The calculated capacitance is shown in Figure (A1.1) for a constant shallow donor concentration of $N_D = 10^{15}/cm^3$ and at a variety of deep level concentrations, N_t. The location of the deep level below the conduction band and the barrier height in this case was taken to be 0.7 eV. CdTe was used as the semiconductor.

The effect of the deep level on the measured capacitance is seen only when the deep level concentration is equal to or greater than shallow dopant concentration. The presence of two or more deep levels,

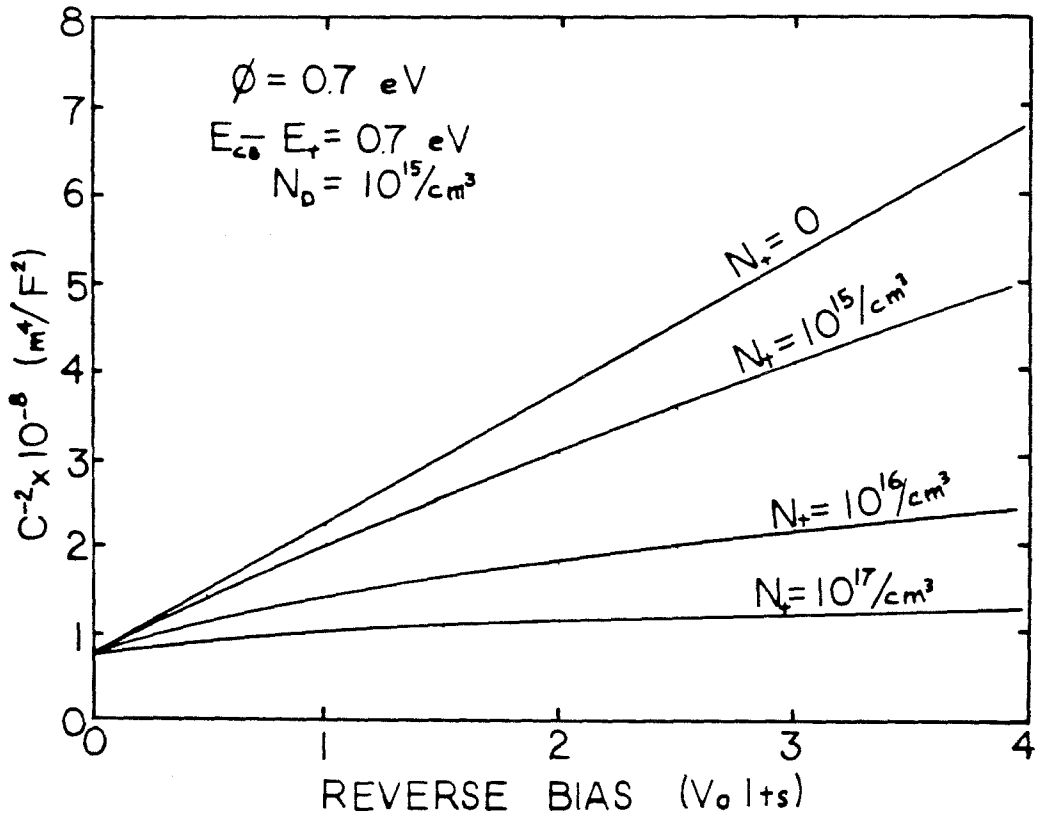

Figure A1.1. The calculated capacitance characteristic of a Schottky barrier diode possessing a spatially uniform deep level. The deep level is located 0.7 eV below the conduction band edge. A barrier height of 0.7 eV to n-CdTe was assumed. The shallow donor concentration, N_D, was fixed at $N_D = 10^{15}/cm^3$ while the deep level concentration, N_t, was allowed to vary.

which may be spatially varying, can complicate the capacitance characteristic further. Such situations require additional information in order to understand the measured capacitance.

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APPENDIX 2

EFFECT OF MINORITY CARRIERS ON THE HETEROJUNCTION BAND BENDING PROFILE

The band bending profile in a Schottky diode, which possesses a barrier height, ϕ_{SB}, approximately equal to the band gap of the semiconductor, requires the solution of Poisson's equation:

$$\frac{d^2\phi}{dz^2} = \frac{-q}{\varepsilon\varepsilon_o}(N_D - n + p) \qquad (A2.1)$$

for the potential, ϕ in the junction region, where N_D is the impurity concentration and n and p are the electron and hole concentration, respectively.

The electron and hole populations are spatially varying and depend strongly on the potential. The electron and hole concentrations can be expressed as

$$n = N_c \exp\left(\frac{-q}{k_B T}(\phi - V)\right) \qquad (A2.2)$$

and

$$p = N_v \exp\left(\frac{-q}{k_B T}(E_{gap} - \phi)\right) \qquad (A2.3)$$

where N_c and N_v are the conduction and valence band density of states,

E_{gap} is the band gap of the semiconductor, and V is the applied voltage. These expressions assume that the hole quasi-Fermi level is equal to the metal Fermi level at the interface and is independent of applied bias. The solution to Equation (A2.1) can be achieved in integral form. The distance, X, into the semiconductor at which the potential has a value ϕ is given by

$$X = -\sqrt{\frac{\varepsilon\varepsilon_o}{2N_D k_B T}} \int_{\phi}^{\phi_{SB}} \frac{dz}{F^{\frac{1}{2}}(z)} \qquad \text{(A2.4)}$$

where

$$F(z) = \frac{q}{k_B T}(z - \phi_e - v) - \left(1 - \exp\left(\frac{-q}{k_B T}(z - \phi_e - v)\right)\right)$$

$$+ \frac{N_c N_v}{N_D^2}\left[\exp\left(\frac{-q}{k_B T}(E_{gap} - \phi_e - z)\right) - \exp\left(\frac{-q}{k_B T}(E_{gap} - 2\phi_e - v)\right)\right]$$

where ϕ_e is the Fermi level position below the conduction band edge in the bulk semiconductor (Equation 2.9). This solution follows the treatment of Schwartz and Walsh [1]; however, the case considered in that reference equates N_c, N_v, and N_D in order to simplify the solution. Such an assumption, however, will substantially underestimate the contribution of minority carriers to the resultant band bending in CdTe. Equation (A2.4) was used to calculate the profiles shown in

Figures 5.13 and 5.14.

The case of a semiconductor heterojunction, in which compositional grading occurs, differs from the model presented above. The compositional grading, which results from interdiffusion, can reduce the barrier height measured in a heterojunction. Oldham and Milnes[2] have shown that in the case of a graded heterojunction equation (A2.1) must be replaced by

$$\frac{d^2E_c}{dz^2} = \frac{q}{\varepsilon\varepsilon_o}(N_D - n + p) - \frac{d^2\chi}{dz^2} \qquad \text{(A2.5)}$$

where $E_c(z)$ is the voltage difference between the conduction band edge and the Fermi level and $\chi(z)$ is the electron affinity of the material. The Equation (A2.2) and (A2.3) are further modified by allowing N_c, N_v, and E_{gap} to spatially vary.

The band gap and electron affinity in a HgTe - CdTe heterojunction, when a zero valence band discontinuity is assumed, can be related by

$$\frac{d^2E_{gap}}{dz^2} = -\frac{d^2\chi}{dz^2} \qquad \text{(A2.6)}$$

The position dependence of the band gap can be determined from the diffusion profile. The band bending using a realistic composition

profile requires the numerical solution of Equation (A2.5). Suitable boundary conditions necessary for solution are found by requiring E_c assume bulk values far from the heterojunction interface.

REFERENCES

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