SWITCHING CONVERTERS WITH MAGNETIC AMPLIFIERS AS CONTROLLABLE SWITCHES

I: Soft-Switching Converters

II: Input Current Shaping

Thesis by

Milivoje Slobodan Brkovic

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to my parents Slobodan and Dragica

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Abstract

Part I

Novel soft-switching converters combine the functions of loss-less soft-switching for all switches and secondary side output voltage regulation at constant switching frequency. This was made possible by using magnetic amplifiers in series with the rectifier diodes in the symmetrical topologies. The primary side switches are driven at constant frequency and near 50% duty ratio with small dead-time and the output voltage is regulated by pulse width modulation (PWM) control on the secondary side.

All three soft-switching topologies, half-bridge, full-bridge and push-pull, are analyzed. It was found that the multiple-output extension of these converter do not have some serious adverse effects inherent to their parent PWM converters with magnetic amplifier post-regulators.

Experimental results obtained on two different prototypes confirm the key advantages of the proposed soft-switching converters.

Part II

Two classes of automatic current shapers are analyzed, with external and internal capacitive energy storage.

The Ćuk converter with Integrated Magnetics when operated in DICM with external energy storage exhibits advantages over other automatic current shaper topologies. Unity power factor is provided automatically and by using "ripple steering" mechanism essentially zero input and output current ripples are obtained for all operating conditions. Consequently, the size of the magnetics can be significantly reduced even at very modest switching frequencies.

The requirement for fast output regulation implies that low-frequency energy is stored

internally in the input current shaper. A new AC-to-DC converter which combines the functions of automatic current shaping, fast output voltage regulation, and loss-less soft-switching in a single converter is proposed. This was made possible through internal energy storage and discovery of the new modes of operation, which together, effectively decoupled the input boost-like part of the Ćuk converter from its buck-like output. In order to keep the voltage stress on the switches low, the variable frequency control is required in addition to PWM control.

Another novel class of single stage AC-to-DC converters with unity power factor and fast output regulation is also proposed. These converters use a magnetic amplifier for the input current shaping, while the active switch is used for fast output regulation. By using core material for magnetic amplifiers with high saturated permeability, and operating the input stage of the converter in DICM, the linear input inductance can be replaced by the saturated inductance of the magnetic amplifier. Thus, the magnetic amplifier combines the functions of a controllable switch and a linear inductor into a single device.

The proposed method of current shaping with magnetic amplifiers is extended to the full-bridge topologies with their input, boost-like stage operated in continuous conduction mode.

Experimental results obtained on different prototypes confirm advantages of the proposed topologies.

Contents

Part I

Soft-Switching Converters

Chapter 1

Introduction

With increased demand for faster response and reduced size and weight, the switching frequency of power converters is increasing toward the megahertz range. By increasing switching frequency of the converters, designers face different kinds of problems. The most serious problems related to the high switching frequency are switching losses which drastically degrade overall converter efficiency.

Over several years, the interest in high-frequency power conversion has stimulated the conception of many different converter circuits. Plenty of them are available for every application, and each year several more are going to be introduced. Every one of these topologies offers some particular combination of the following features: low-current stresses, low-voltage stresses, additional control, wide range of conversion ratio, low cost, and simplicity. There is no single topology which is superior in all these areas, so the choice of topology is left to the designer.

While faster power transistors have mitigated overlap loss, the reverse-recovery time of the power diodes as well as voltage spikes and discharging current of the parasitic capacitances start to be a limiting factor in PWM converters. Resonant converters [13, 14, 15] and their derivatives quasi-resonant [17, 18, 19, 20, 21] and multi-resonant converters [22] having continuous waveforms were introduced as a solution for switching loss elimination and higher power density than PWM converters. It turned out that due to increased conduction losses and complex control, resonant converters are only used in very specific applications. Soft-switching converters, recently introduced, combine advantages of both PWM and resonant converters and are becoming a very promising solution for highly efficient and high power density conversion.

Resonant elements in the soft-switching converters are not used for energy transfer but only during switching intervals to provide either zero current (ZCS) or zero voltage

(ZVS) switching. During the rest of the switching period, the converter behaves like the PWM converter. Resonant frequency is well above the switching frequency, and the resonant voltage is "clamped" by a rectifier or second switch after the transition is completed. The waveforms between transitions look very much like those in PWM converters. In this thesis *soft-switching* converters are classified as the converters which use a switching technique that combines PWM control at constant switching frequency, and resonant behavior only during the switching transitions.

Different soft-switching mechanisms have been proposed in the past several years [24, 25, 26, 27, 33, 34, 36]. These solutions have some common disadvantages such as increased current stresses on the switches, increased losses in the magnetics, limited range of soft-switching, and complex control circuitry. In order to achieve zero-voltage switching for all operating conditions, these topologies use an additional active or passive components.

The field of magnetic amplifier regulators is another area in power electronics which has received much attention during the past few years. This becomes more obvious when the operating frequency of the converters increases and switching losses in semiconductor devices start becoming the limiting factor. Due to its non-linear characteristic and very simple control, a magnetic amplifier, or *magamp* for short, can be used very efficiently as a controllable switch in a large variety of applications.

With the development of new amorphous materials with square-loop characteristics [29, 30, 31] which improve efficiency at higher switching frequency, it seems that magamps are going to play an important role in design of switched-mode power converters. It is gratifying to see that as the operating frequencies of modern power converters increase, the magamp is *not* a critical component. Their capability to work nicely at 1MHz and above has already been proven [6]. The magamp regulators are a dominant force in multiple-output converters [5, 11].

In the thesis magamps are studied as controllable voltage-bidirectional switches which provide two essential functions for any switched-mode regulator: a) soft-switching and b) the output voltage regulation. A novel soft-switching mechanism with magamps [32] is described and applied to all three symmetrical topologies, half-bridge, full-bridge and

push-pull converters.

Chapter 2 gives an overview of saturable inductors and magamps. Different reset methods of the magamp are discussed and the most common application of magamps as post-regulators in the multiple-output converters are reviewed. The limitations of the magamp as a controllable voltage-bidirectional switch are also discussed.

A survey of the soft-switching converters is given in Chapter 3. After the switching loss mechanisms in PWM converters are explained, the existing different solutions to switching loss elimination are briefly reviewed. The basic soft-switching mechanism is explained in the buck converter [25]. Widely used zero-voltage switching phase-shifted full-bridge converter [33, 36] is also discussed.

In Chapter 4, a novel soft-switching half-bridge converter with magamps is described. The proposed soft-switching mechanism uses reflected load current for zero-voltage switching of the primary side switches while the soft turn-off of the rectifier diodes is provided by the non-linear characteristic of magamps. Experimental results obtained on the prototype are presented to confirm these features.

The proposed soft-switching mechanism is then extended to the full-bridge and push-pull topologies in Chapter 5. The novel soft-switching full-bridge converter is compared with zero-voltage switching phase-shifted full-bridge converter, and experimental results are presented.

Multiple-output extension of the novel soft-switching converters with magamps is given in Chapter 6. It is shown that these converters do not have adverse effects inherent to their parent PWM converters with magamp post-regulators. The novel soft-switching converters are well suited for independent regulation of the multiple outputs.

Chapter 7 summarizes the advantages of the proposed soft-switching converters.

Chapter 2

Review of Saturable Inductors and Magnetic Amplifiers

Saturable inductors and magamps play an important role in the design of modern switched mode power supplies. This becomes more obvious when the operating frequency of the converters increases, and switching loss in semiconductor devices start to become the limiting factor. Due to its non-linear characteristic and very simple control, the magamp can be used very efficiently as a controllable switch with a wide range of applications.

This chapter gives an overview of saturable inductors and magamps, beginning with a piecewise-linear model for magnetics in Section 2.1. Section 2.2 describes the principle of operation of saturable inductor, while the controllable saturable inductor or magamp is outlined in Section 2.3. In Section 2.4, the multiple output converter which uses magamps for tight regulation of the auxiliary outputs is reviewed. The chapter concludes with a discussion of magamp limitations in Section 2.5.

2.1 A Piecewise-Linear Model for Magnetics

In this section the "integration procedure" (actually a scale factor change) is applied to a collection of magnetic properties that are defined analytically in order to obtain a piecewise-linear model useful for the designer [1].

There are four physical properties of magnetic material which are identifiable components of a magnetization curve, and each of them is modelled in the simplest way. These four components – high permeability, saturation, hysteresis, and dynamic loss – are then collected into a *piecewise-linear model.* The model has two forms, magnetic and electric, which differ in whether the integration procedure has been applied.

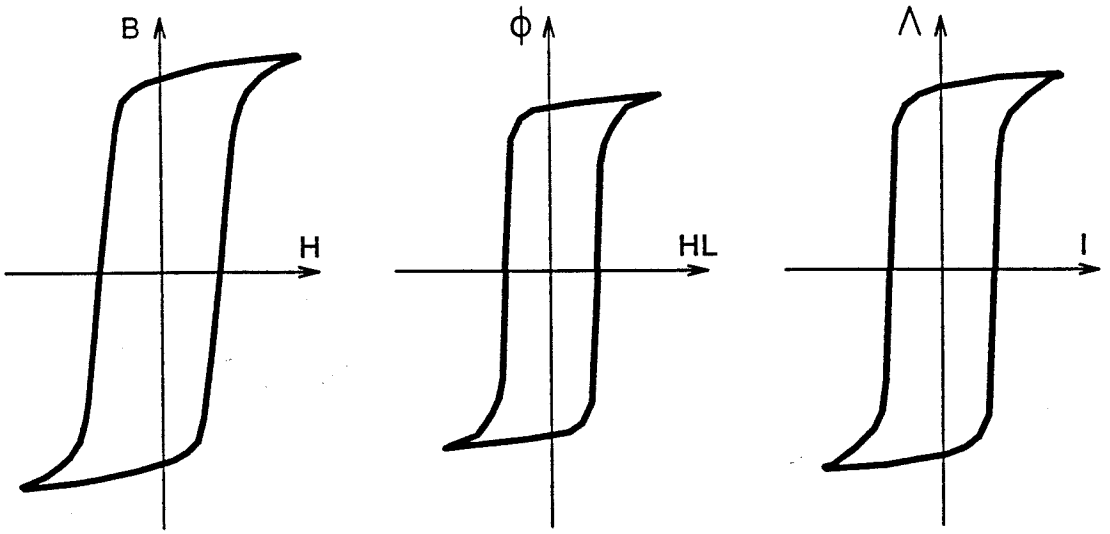


Figure 2.1: An illustration of design mechanics: from material to device properties. Bulk property of material is translated into device property by scaling both axes with geometrical parameters of the particular core.

2.1.1 Relating Material Properties to Device Characteristics

Our goal is to quantitatively translate magnetic material properties of core material (B-H characteristic) to the more useful design volt-ampere characteristic of the device. An illustration of design mechanics is shown in Fig. 2.1. The original curve $(B - H)$ which describes the property of the core material is shown in Fig. 2.1 (a). The slope of the curve, μ, is the permeability of the magnetic material, and B_s is saturation flux density.

In this procedure homogeneous flux distribution and flux path are assumed. By scaling-up (multiplying) the ordinate axis with core cross-sectional area S, and the abscissa with the total magnetic path length l, the new curve with changed scales, F versus Φ, is obtained in Fig. 2.1 (b). It describes the property of the *magnetic circuit (core)* combining the extrinsic design choice of the specific core geometry with the choice of intrinsic material properties specified by the $B - H$ curve. The slope of the $\Phi - F$ curve has the dimensions of permeance $P = \mu S/l$.

The final design step is the specification of the number of turns of wire, N to be

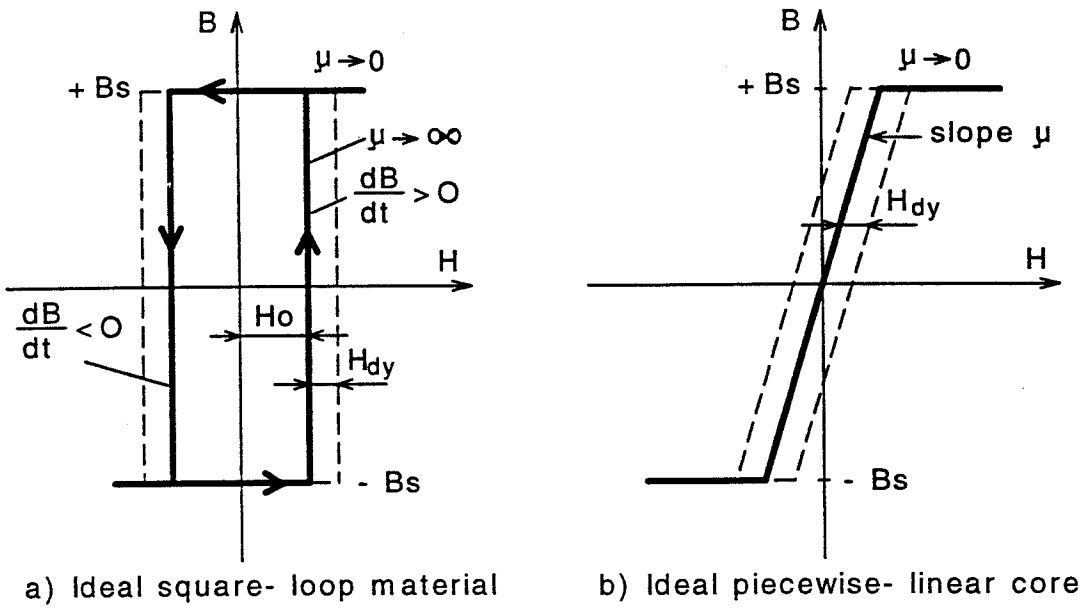


Figure 2.2: A piecewice-linear model for magnetic material combines four essential features of magnetic material: slope μ, saturation flux density B_s, static hysteresis width H_o, and dynamic hysteresis H_{dy}.

wound upon the core. By multiplying the ordinate axis and dividing the abscissa axis with N, the final result in Fig. 2.1 (c) is represented in purely electrical units. The slope of the curve in Fig. 2.1 (c) has the dimension of inductance $L = \int vdt/I = N^2P$.

It should be emphasized that all three graphs in Fig. 2.1 have the same shape, but with a different scale.

2.1.2 The Magnetic Model

The first essential feature of magnetic material, *high permeability* μ, is the ability of magnetic material to produce a larger effect (B_i, hence larger flux) with smaller means (H, hence smaller current). It is translated into the slope of the magnetizing curve in which B is proportional to H as shown in Fig. 2.2 (b).

The second component of the model is the *saturation* value B_s which models saturation of intrinsic flux density B_i. The physical meaning of saturation is that all the elementary magnetic moments that constitute the intrinsic induction of the material are

completely aligned so that any further increase of H does not contribute to change in flux density. The region between saturation levels, $+B_s$ and $-B_s$, is called the *linear region.* Magnetic circuits, such as transformers and linear inductors, are usually designed to operate in linear region of $B-H$ curve and are prevented from running into saturation. On the other hand, saturable inductors are normally designed to have flux density moving between the linear region and saturation.

The $B-H$ curve of magnetic materials possesses a *hysteresis* property which is manifested as a double-valued curve in the H-direction. The parameter of interest is the *"static width"* of the hysteresis loop, which is modelled in Fig 2.2 (a) as a square-loop parameter H_o. The total width of a square-loop material is $2H_o$, which in the ideal case is constant and independent of B for any $|B| < B_s$.

The fourth component of the piecewise-linear model represents *dynamic loss.* The area inside a $B-H$ curve is dimensionally equivalent to core loss purely due to hysteresis and associated width H_o. The excess loss in the core due to eddy current are modelled by the dynamic component of hysteresis loop width $H_{dy} = g_e dB/dt$ shown by dashed lines in Fig. 2.2.

In the linear region, the magnetic model can be expressed by the following equation in H [1]:

$$H = H_o(sgn\frac{dB}{dt}) + \frac{1}{\mu}B + g_e\frac{dB}{dt}, \quad for\ |B| < B_s. \tag{2.1}$$

The first term in Eq. (2.1) describes hysteresis. The second and third terms are the slope and the dynamic width components of H, respectively.

2.1.3 The Electrical Model

With the magnetic model given by Eq. (2.1) the electrical model is obtained by using design mechanics described in Section 2.1.1. The final result is equation in inductor current I [1]:

$$I = I_o(sgnv) + \frac{1}{L}\int vdt + G_e v, \quad for\ |\Phi| < \Phi_S. \tag{2.2}$$

The corresponding piecewise-linear electrical model for a core with N turns is shown in Fig. 2.3. The four circuit elements – inductance L, ideal switch S, reversible current source I_o, and conductance G_e – are related to the four intrinsic material properties –

slope μ, saturation B_S, static width H_o, and dynamic width H_{dy}. The ideal switch S is a "saturation switch" which is flux controlled. It is open for normal functioning of the other elements, i.e., when $|\Phi| < \Phi_S$ and closed when core is in saturation, i.e., when $|\Phi| > \Phi_S$.

Once the saturation of the core occurs, the switch S is closed and consequently shorts all elements, causing $v = 0$ regardless of the current level. By recalling that $v = 0$ is equivalent to $\frac{d\Phi}{dt} = 0$, it means that zero voltage is a condition of constant flux in saturation.

The constant current source I_o represents magnetizing current of the core and is a measure of the static width of a hysteresis loop. The associated ideal diode network, simulating *sgnv*, provides that the current direction is controlled by the polarity of the input voltage. The reversal network provides a short-circuit across the input terminal if $|I| < I_o$. When the input current exceeds I_o, two diagonal diodes conduct and allow existence of the input voltage which causes excess circuit $(I - I_o)$ through the inductance L and/or conductance G_e.

2.2 Principle of Operation of Saturable Inductor

It follows from Faraday's law that total or linkage flux, $\Lambda = N\Phi$, is the volt-seconds integral of the voltage across the inductor, i.e.,

$$\Lambda = \int v dt. \tag{2.3}$$

From Eq. (2.3) follows a very important fact that the state of the core is determined by the volt-seconds integral. Consequently we can say that the inductor is *"volt-second integral"* since it converts voltage applied during a certain interval of time into change of total flux in the core. This fact is used in understanding how a saturable inductor operates and how it can be used as a switch, which is described next.

Consider the inductor L in the electrical circuit of Fig. 2.4 (a) with ideal square-loop $\Lambda - I$ characteristic shown in Fig. 2.4 (b). The inductor is designed to saturate in both positive and negative half-cycle of source voltage.

Salient waveforms are shown in Fig. 2.5. At $t = 0$, the source voltage switches from $-V_g$ to $+V_g$. Since before $t = 0$, the inductor was in saturation (point G in Fig. 2.5 (b)),

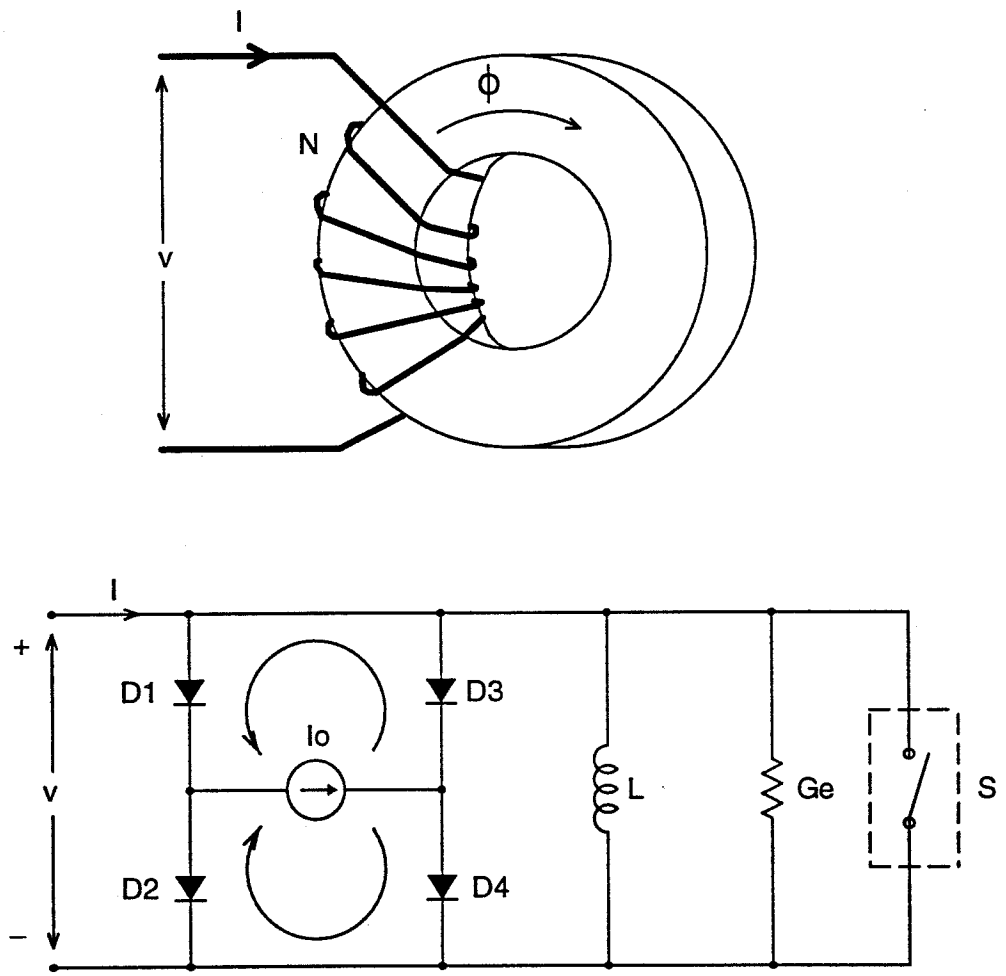


Figure 2.3: Piecewise-linear electrical model of the core of the inductor.

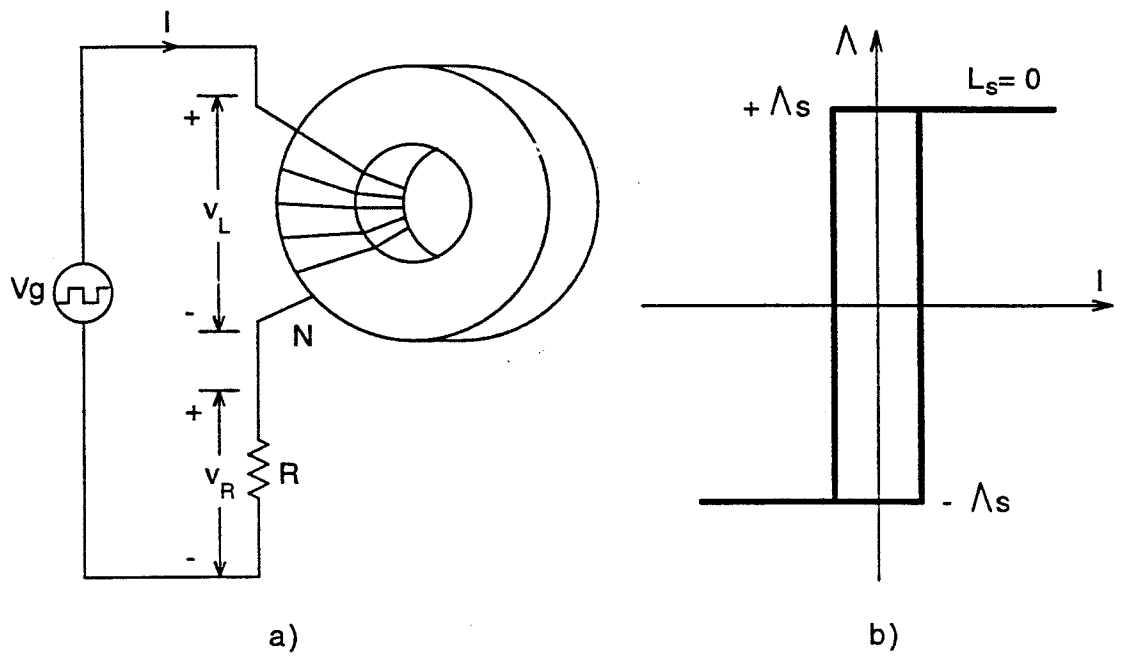


Figure 2.4: Principle of operation of the saturable inductor is explained in the simple circuit using the inductor L with ideal square-loop $\Lambda - I$ characteristic resistor R.

$v_L = 0$ and input voltage $-V_g$ was applied across resistance R. Inductor current I_L was negative and limited only by resistance R. Due to the applied positive voltage V_g, current I_L drops to zero and reverses direction. The flux in the the inductor moves from point G to point H almost instantaneously (Fig. 2.4 (b)). The inductor runs out of saturation at small current $i = I_o$ (point H) and blocks source voltage V_g. The flux linearly increases from $-\Lambda_s$ until it reaches $+\Lambda_s$ after time interval θ_1 (point C) and remains constant until source voltage again switches at $T_s/2$. As the core saturates after time θ_1, the inductor represents short-circuit ($v_L = 0$) and source voltage V_g appears across the load resistance R (Fig. 2.5 (e)).

The process repeats during negative half-cycle of source voltage when the flux in the core moves from $+\Lambda_s$ to $-\Lambda_s$ following path $D \rightarrow C \rightarrow E \rightarrow F \rightarrow G$ on the $\Lambda - I$ characteristic in Fig. 2.5 (b)). At $t = T_s/2$, the source voltage changes polarity from $+V_g$

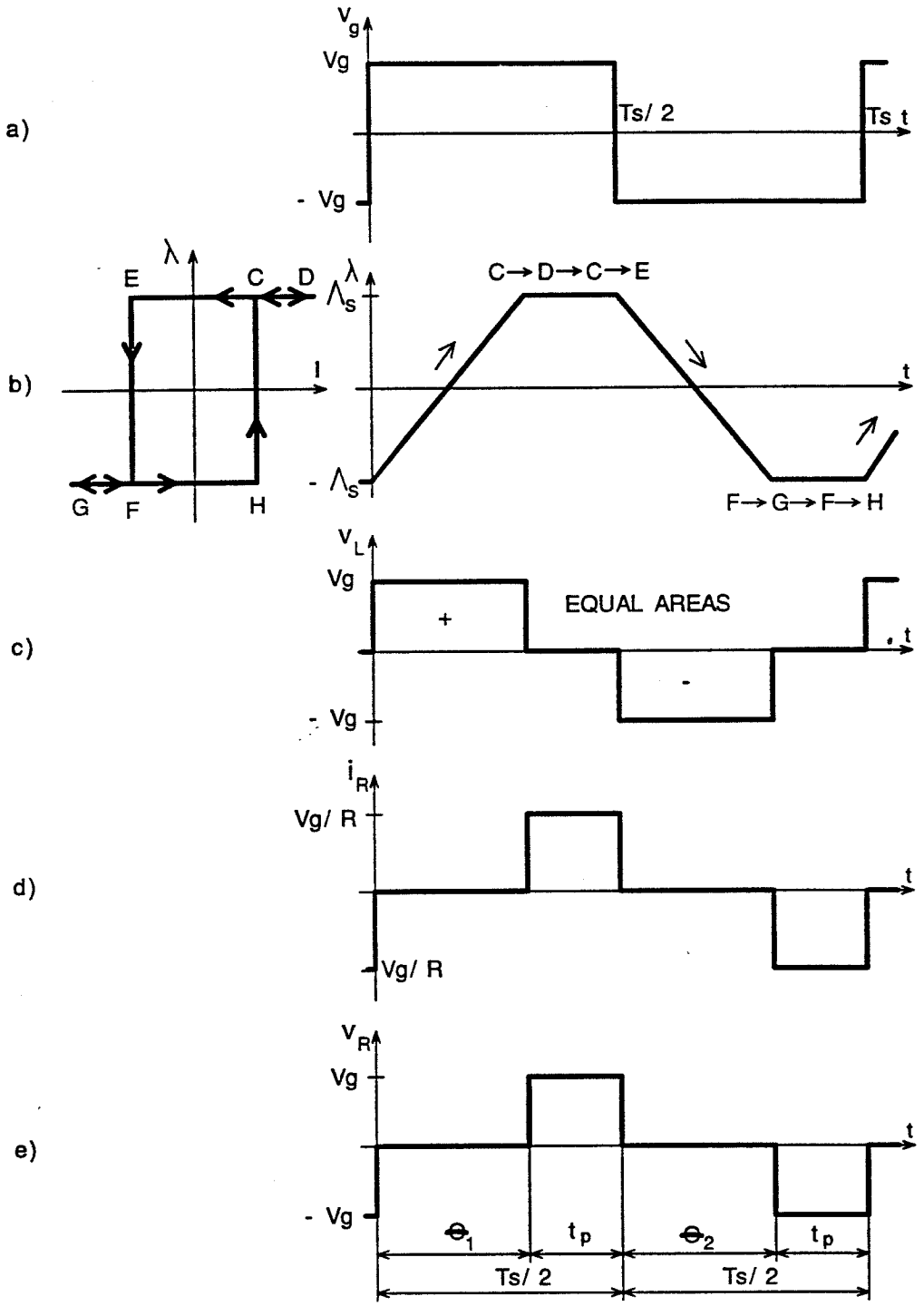


Figure 2.5: Salient waveforms in the circuit with saturable inductor: a) source voltage v_g, b) flux λ, c) inductor voltage v_L, d) resistor current i_R, and e) resistor voltage v_R.

to $-V_g$ causing the inductor to run out of saturation when $I_L = -I_o$ (point E). The inductor supports negative voltage $-V_g$ during the blocking time interval θ_2 (Fig. 2.5 (c)). At $t = \theta_2 + T_s/2$ (point F), the inductor runs into negative saturation, $v_L = 0$, and consequently source voltage $-V_g$ appears across load resistance R.

The durations of the blocked parts of incoming positive $(+V_g)$ and negative $(-V_g)$ pulses of source voltage, θ_1 and θ_2, respectively, are the same and denoted as θ. The blocking interval, θ, is the time delay between the voltage pulse applied to the load and source voltage waveform. It is given by

$$\theta = \frac{\Delta\Lambda}{V_g} = \frac{2\Lambda_s}{V_g}. \tag{2.4}$$

The duration of the voltage pulse on the resistance R is given by (Fig. 2.5 (c))

$$t_p = D_{eff}T_s = \frac{T_s}{2} - \theta, \tag{2.5}$$

where, D_{eff} is effective duty ratio defined as

$$D_{eff} = \frac{t_p}{T_s}. \tag{2.6}$$

The average voltage on the resistor, $< v_R >$, is given by

$$< v_R >= D_{eff}V_g = (1 - \frac{2\theta}{T_s})V_g. \tag{2.7}$$

The blocking capability of the saturable inductor, $2\Lambda_s$, is the maximum volt-seconds product that the core can withstand. It depends on the number of turns N, core cross-sectional area S and saturation flux density B_s. The blocking interval given by Eq. (2.4), is the maximum blocking interval for given source voltage and inductor and cannot be continuously controlled in the circuit from Fig. 2.4 (a).

2.3 Magamp

A *magamp*, also called a transductor, is a controlled magnetic impedance located in series with a unidirectional current switch and load, and connected to an alternating supply voltage. It utilizes the saturable inductor described in Section 2.2 with a controllable blocking time to control the output voltage. Thus, a magamp establishes an OFF-ON type of load control. It is also known as the reactor-rectifier [2].

The increased demand for more compact and reliable switched-mode power supplies has aroused a renewed interest in a well-founded control technique – the magamp. In multiple-output power supplies magamps are adopted as post-regulators required for independent regulation of the output voltages including features such as overcurrent and short circuit protection. In recent years, magamps have received growing interest, and a large number of papers both from the industry and universities have been published [3]-[9].

2.3.1 A Magamp Control

The basic circuit of a magamp is shown in Fig. 2.6 (a). Two main differences between this circuit and the circuit in Fig. 2.4 (a) are:

a) Diode $D1$ is added in series with saturable inductor

b) Voltage source V_c is used to control the magamp. Resistance R_c represents control source series resistance, while diode D_c blocks the positive voltage appearing across the control voltage source V_c.

Diode $D1$ is forward biased during the positive half-cycle of source voltage, usually called *forward* or *gate* cycle, and reverse biased during negative half-cycle of source voltage, also called *reset* cycle. During the forward cycle, part of the positive source voltage pulse is blocked for a time determined by the volt-seconds stored in the inductor during the preceeding reset cycle. During the reset cycle the negative voltage applied across the inductor is determined by the control voltage V_c which opposes the negative source voltage V_g.

The number of turns N, is chosen so that $2\Lambda_s$ just exceeds the source voltage maximum half-cycle area $V_g T_s/2$. This gives the core the capability of absorbing V_g over an entire half-cycle, for instance, during overload or short circuit conditions.

Salient waveforms for dc or steady-state operation during a switching period are shown together with the square-loop $\Lambda - I$ characteristic of the saturable inductor in Fig. 2.7.

There are two methods to control or reset magamp: a) *voltage reset*, and b) *current reset*. The basic principle is the same and is based on equality of volt-seconds stored,

during reset, and volt-seconds blocked, during forward cycle. In the *voltage reset* method ($R_c = 0$), constant reset voltage is applied across the inductor during the reset cycle. On the other hand, in the *current reset* method ($R_c \neq 0$) a *constant current* is applied to drive the flux away from $+B_s$. This method is also known as magneto-motive force control (*mmf* control).

2.3.2 Voltage Reset Method

During the reset cycle, voltage $-(V_g - V_c)$ is applied across the inductor (dashed area in Fig. 2.7 (c)) causing flux in the core to move from $+\Lambda_s$ down to $-\Lambda_c$ following path $D \rightarrow C \rightarrow E \rightarrow A$ in the $\Lambda - I$ characteristic (Fig. 2.7 (b)). Therefore, the control voltage V_c controls the negative volt-seconds stored during the reset of the core ($\Delta\Lambda = \Lambda_s - \Lambda_c$), and sets up equal positive volt-seconds blocking ($V_g\theta_c$) for the following forward cycle. As shown in Fig. 2.7 (b), flux transverses close path $A \rightarrow B \rightarrow C \rightarrow D \rightarrow C \rightarrow E \rightarrow A$ during one switching period T_s and core only saturates in the positive direction in contrast to path $G \rightarrow F \rightarrow H \rightarrow C \rightarrow D \rightarrow C \rightarrow E \rightarrow F \rightarrow G \rightarrow$ in Fig. 2.5 (b).

The flux swing, $\Delta\Lambda$, is calculated from volt-second balance on inductor as:

$$\Delta\Lambda = (V_g - V_c)\frac{T_s}{2} = V_g\theta_c. \tag{2.8}$$

The blocking time, θ_c, where subscript c denotes blocking time due to the control voltage, can be expressed from Eq.(2.8) as:

$$\theta_c = (1 - \frac{V_c}{V_g})\frac{T_s}{2}. \tag{2.9}$$

The duration of the voltage pulse passed to the load, t_p, is calculated from Fig. 2.7 (b) as

$$t_p = D_{eff}T_s = \frac{V_c}{V_g}\frac{T_s}{2}. \tag{2.10}$$

The average output voltage,$< v_R >$, is given by

$$< v_R >= D_{eff}V_g = \frac{V_c}{2}. \tag{2.11}$$

Equation (2.11) suggests perfect line rejection with voltage reset, i.e., that the load or output voltage of the magamp v_R, is independent of the source voltage V_g. However

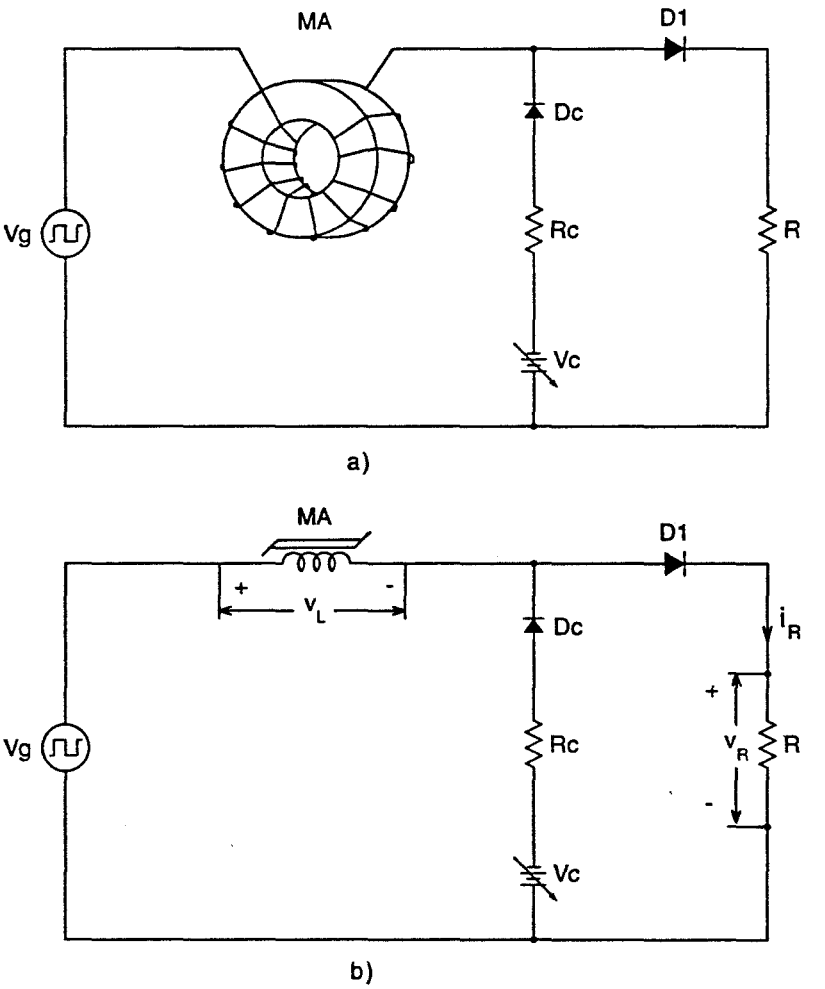


Figure 2.6: The basic circuit of the magamp.

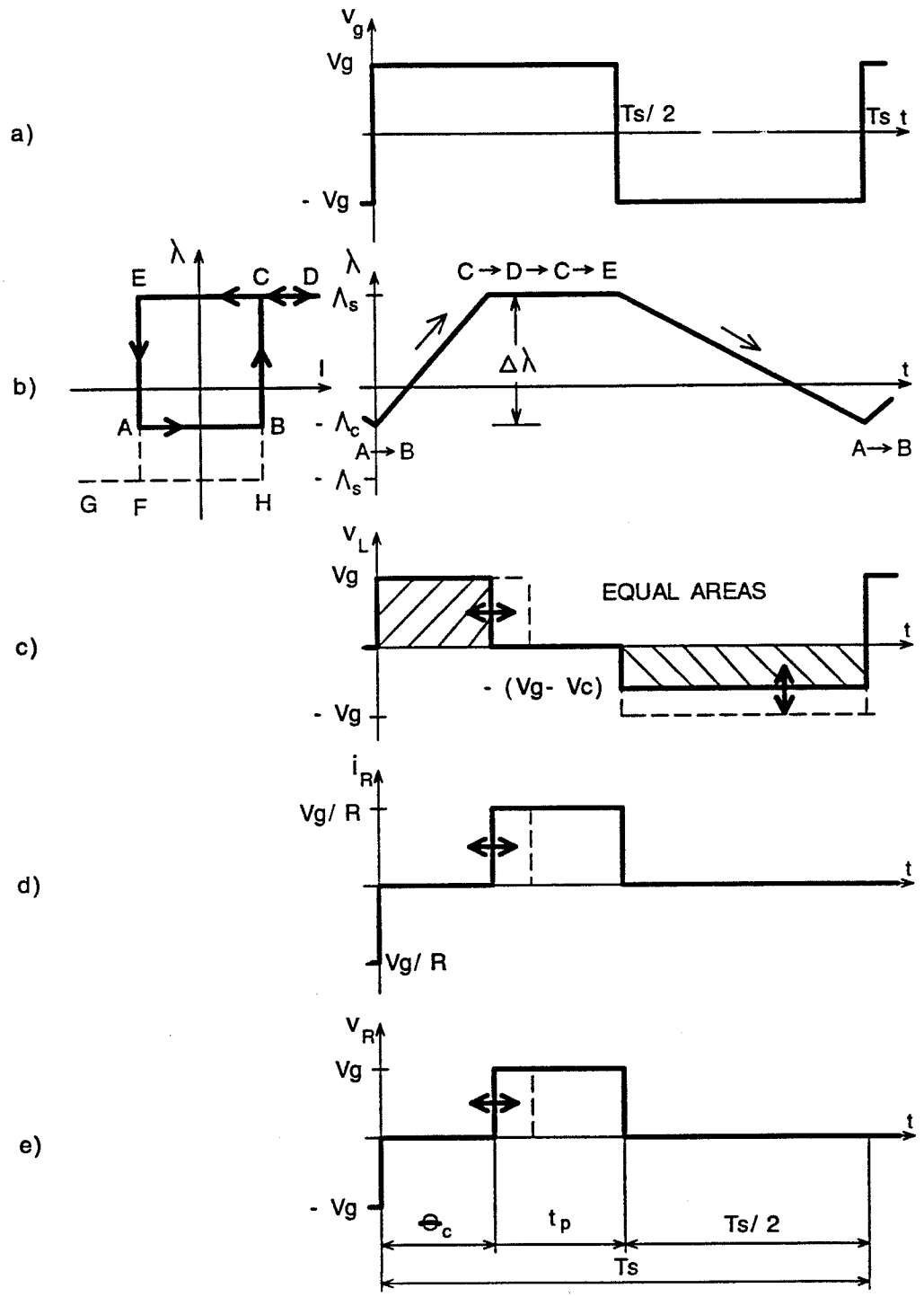


Figure 2.7: Salient waveforms in the circuit with magamp: a) source voltage v_g, b) flux λ, c) inductor voltage v_L, d) resistor current i_R, and e) resistor voltage v_R.

this is an oversimplification because in Eq. (2.8) the delay between source voltages V_g on the left and right side of the equation is neglected. The correct result including the time delays was derived in [8] and found to be a function of frequency as follows:

$$< v_R > \simeq \pi D_{eff} \frac{f}{f_s} V_g, \tag{2.12}$$

where, f is the modulating frequency of the control voltage and f_s is switching frequency.

It can be seen from Eq. (2.9) that when $V_c = 0$ (no control) the blocking time is equal to $T_s/2$, which means it is possible to block source voltage V_g over an entire half-cycle. This feature allows overload and short circuit protection.

2.3.3 Current Reset Method

In the current reset method, a constant current is used to control flux reset in the core. Control or reset current I_c determines magnetic field H (through core geometry and number of turns) which through the permeability μ determines flux density B and finally, through cross-sectional area and number of turns, total flux Λ_c. In other words, unsaturated inductance of the magamp, L, converts reset current into the linkage flux, i.e., volt-seconds stored during the reset period.

Total magnetizing current of the inductor is equal to the control current I_c and consists of three components:

$$I_c = I_o + \frac{1}{R_e}\frac{d\Lambda}{dt} + \frac{\Lambda}{L}. \tag{2.13}$$

Only the last component in Eq.(2.13), Λ/L contributes to the dc component of flux reset Λ_c.

A serious disadvantage of the current reset is that the volt-seconds stored, and therefore, the blocking capability are both dependent on the unsaturated inductance of the magamp. It may have wide variations from sample to sample, over temperature, or at different points on the $B - H$ loop. In contrast, the voltage reset does not have that problem because the gain of the reset stage is unity, independent of core characteristics. In addition, the voltage reset provides inherently feed-forward line rejection thus, allowing simple design of the regulator's loop [10].

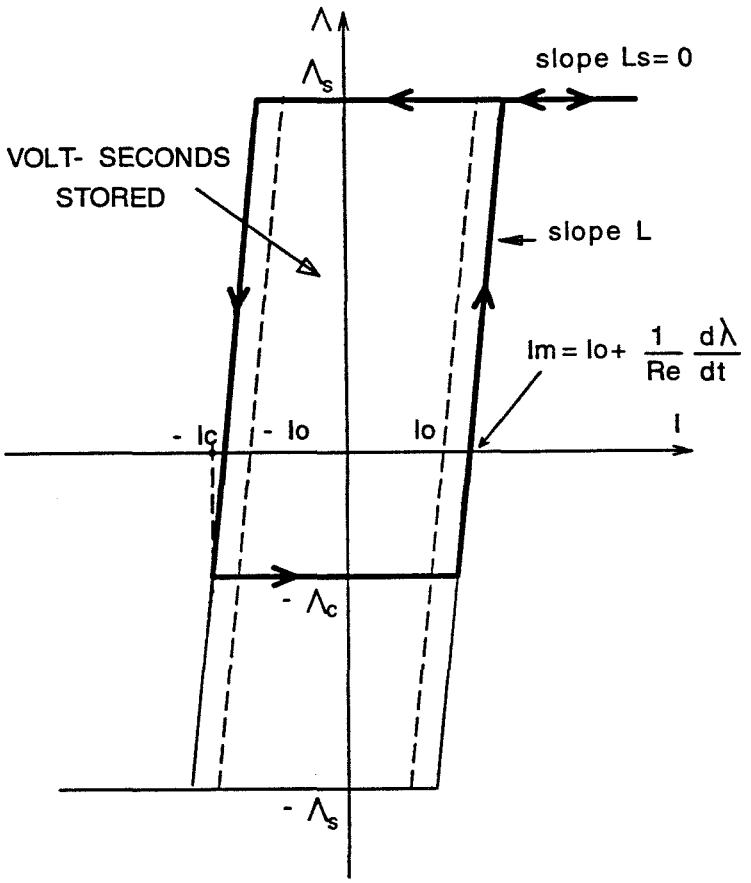


Figure 2.8: In the current reset method, control current, I_c, drives core out of saturation and determines value of the reset flux Λ_c.

In summary, a magamp can be used as a *controllable voltage bi-directional switch* consisting of saturation switch S in series with diode D as shown in Fig. 2.9 (d). Controlled variable is volt-seconds stored or flux reset. Saturation switch S is closed when inductor is saturated and open otherwise.

2.4 Magamp as a Post-Regulator

A block diagram of typical multiple-output switched-mode power supply is shown in Fig. 2.10. Since all outputs share the same inverter stage, only one output, called the *main output*, is fully regulated against load and line voltage variations by pulsewidth

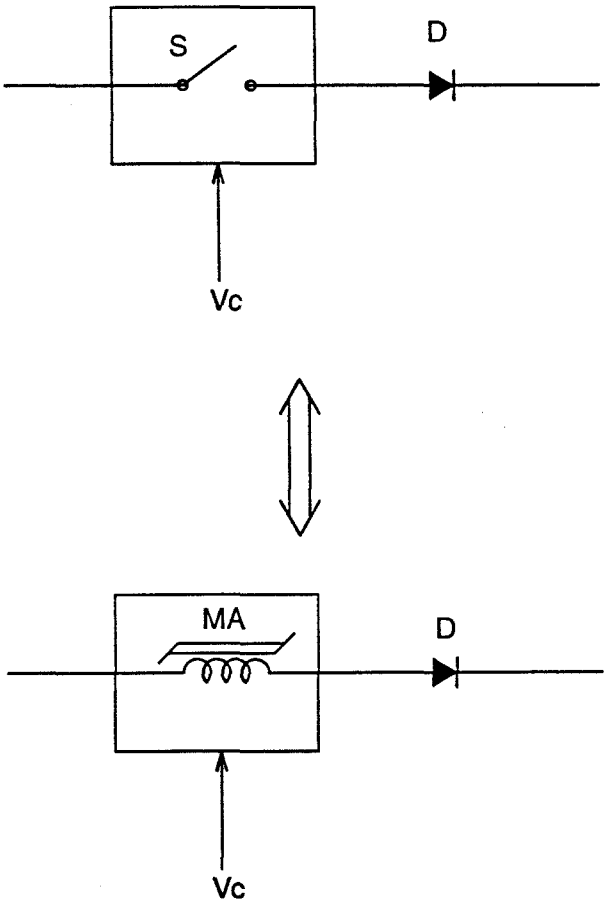


Figure 2.9: Magamp can be used as a voltage bi-directional switch consisting of saturation switch S and diode D.

modulation of the switches in the inverter stage. Additional post-regulators are required for independent regulation of auxiliary outputs against load variations.

The magamp is very attractive as a post-regulator due to its benefits,when compared to other post-regulator techinques [11], such as: lower parts count, more rugged, more efficient, considerable smaller EMI, and lower stress on the main inverter power switches. The recent development of low-cost, high frequency, square-loop amorphous materials has made the magamp regulator a preferred solution to many multiple output applications for operating frequencies over 100kHz [11, 12].

A forward converter using a magamp is shown, as an example, in Fig. 2.11, while the

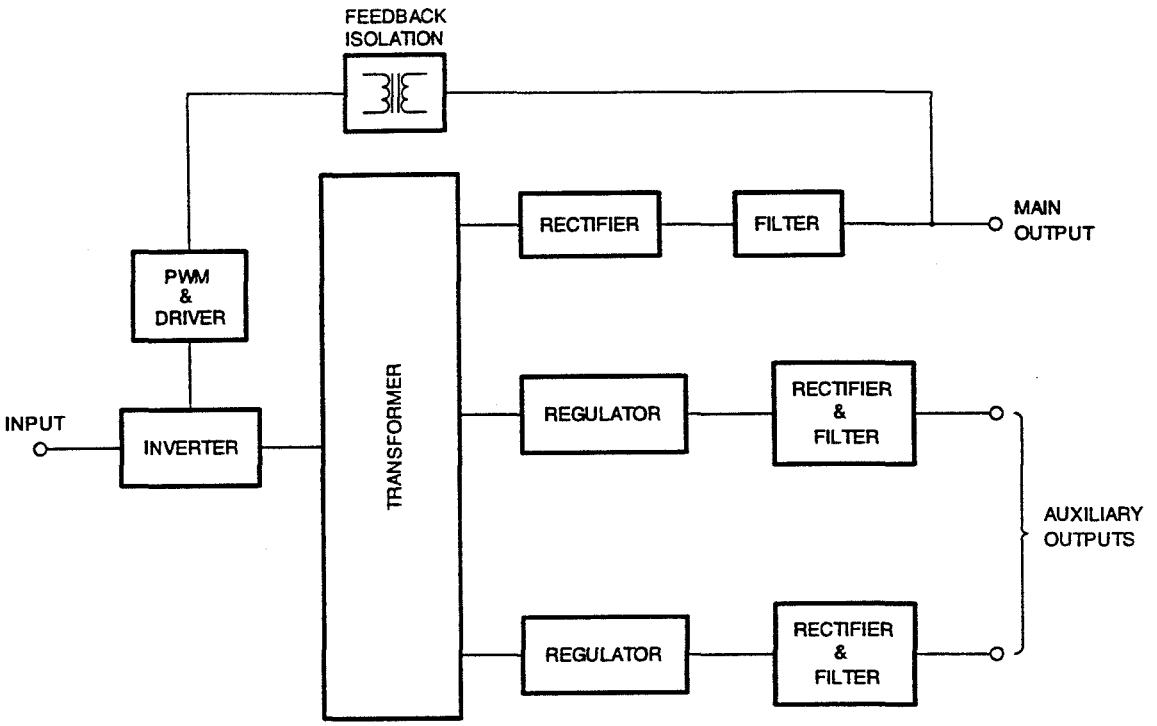


Figure 2.10: Block diagram of a multiple-output switched-mode power supply. Only one output can be regulated by PWM of the inverter stage while the auxiliary outputs require additional post-regulators.

salient waveforms are shown in Fig. 2.12. The technique can also be used in the flyback converter and the symmetrical topologies with full-wave rectification such as push-pull, half-bridge and full-bridge converters. The main switch on the primary side is controlled by a pulsewidth modulator (PWM). Voltage on the main output, usually 5V, is compared with a reference and an amplified error signal is feed into the modulator to adjust the conduction interval (t_{on}) of the main switch. In this way the volt-seconds product, which appears at all secondaries, is adjusted only against input voltage, while the 5V output is in addition, regulated against load variations.

Without magamp MA1, the auxiliary output is "semi-regulated", since the primary control loop provides only regulation against line voltage variation. Thus, an additional post-regulator, realized with a magamp, is used to tightly regulate the auxiliary output.

In order to regulate the auxiliary output voltage at 12V, the average value of the

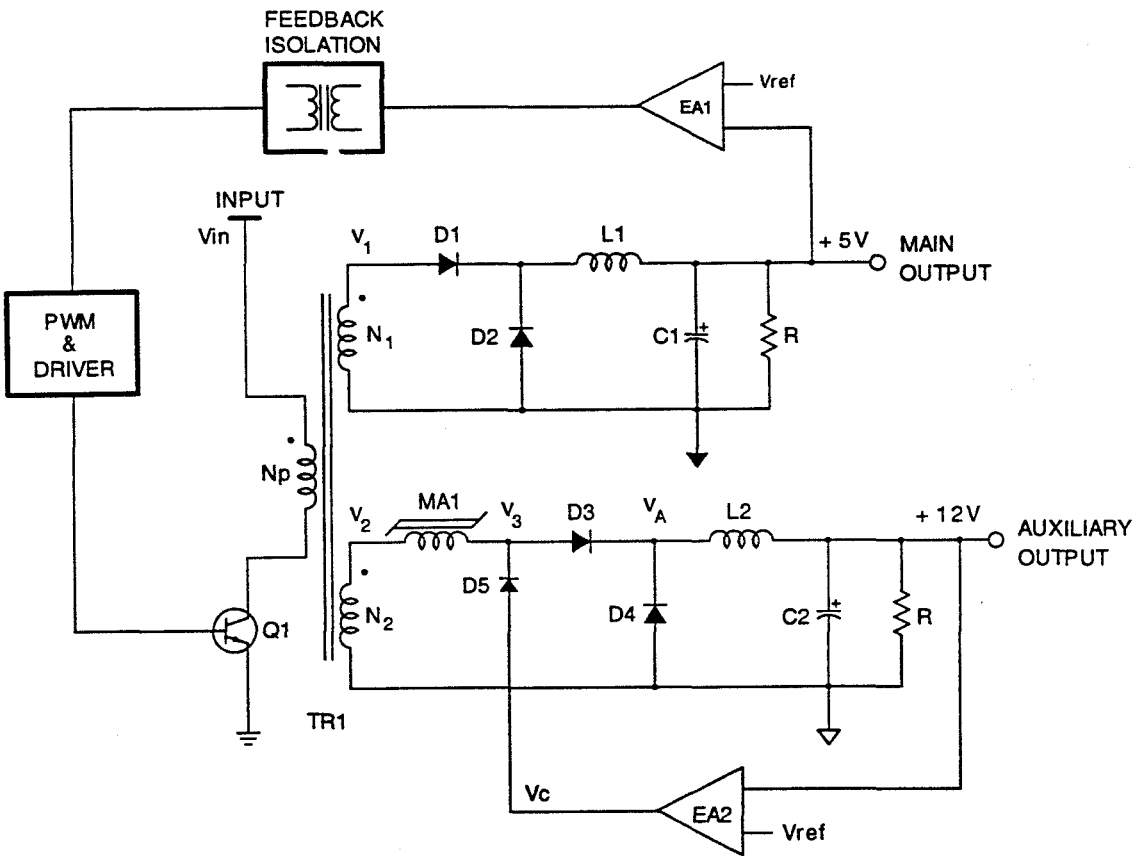


Figure 2.11: Schematic of a multiple-output forward converter using magamp as post-regulator.

rectified waveform applied to the output filter L_2C_2 (V_A in Fig. 2.11) must be constant and equal 12V. It means that the volt-seconds product at point A, must be regulated.

Since the magnitude of the secondary voltage v_2 is determined by the input voltage (V_{in}) and the transformer's turns ratio (N_2/N_p), only the pulse width of the voltage v_A, t_p, can be controlled. This is provided with magamp which delays the leading edge of the positive pulse by the appropriate time θ as shown in Fig. 2.12. The blocking interval θ is controlled by the error amplifier $EA2$ which compares the output voltage to a reference and accordingly adjusts the reseting of the core during the OFF interval of the main switch $Q1$.

The primary current increases when the core of magamp saturates and begins to

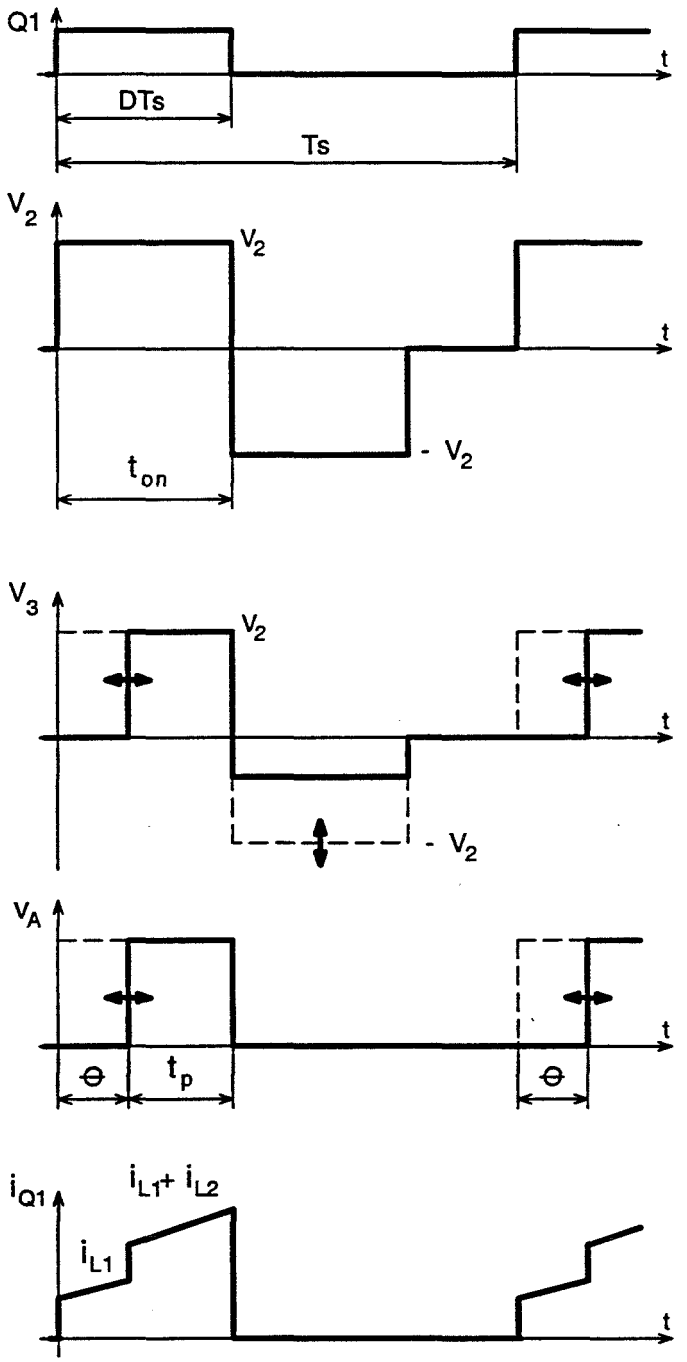


Figure 2.12: Salient waveforms in a multiple output forward converter describing principle of operation of the magamp as a regulator.

deliver current to the auxiliary output. This has an incidental bonus: the primary switching transistor has already turned on and hence, the auxiliary output does not contribute to turn on loss in the transistor.

2.5 Limitations of the Magamp as a Switch

Limitations of the magamp owe to the non-ideal characteristics of the magnetic material. More realistic $B-H$ characteristic for the square-loop magnetic material, widely used for saturable inductors, is translated to the volt-seconds-magnetizing or the $\Lambda - I$ characteristic in Fig. 2.13. There are five essential non-idealities of the magnetic material which cause three different kind of undesirable effects. They are explained next.

FINITE MAGAMP CURRENT IN BLOCKING STATE

The first effect is due to *finite unsaturated permeability* μ which produces finite unsaturated inductance L. The saturable inductor, therefore, does not represent open circuit when it is operated out of saturation because of the non-zero inductor current. In other words, there is a leakage current inversely proportional to the unsaturated inductance L when the switch (saturable inductor) is turned-OFF. Another consequence of the finite slope is increased control current and consequently increased loss in the control circuit. Cores with steeper slopes require lower number of turns and therefore have lower conduction loss.

CORE LOSSES

The existence of the *hysteresis loop* produces core loss. The hysteresis consists of static width, and two dynamic width components due to eddy currents and the re-entry characteristic of the core [7]. Re-entry current occurs as a consequence of increased hysteresis width due to high load current driving the core material far into saturation . It has been shown in [7] that the width of the $B-H$ loop for $H > 0$ is independent of the load current $B > B_s$ whereas on the left side $H < 0$ (during reset) the width increases with increasing load current. This re-entry current is more noticeable in amorphous materials. In the $\Lambda - I$ characteristic of Fig. 2.13 the dynamic width due to the re-entrant characteristic is omitted and only components due to static width and eddy currents are shown. The later is the difference between the zero-flux magnetizing current I_m and the

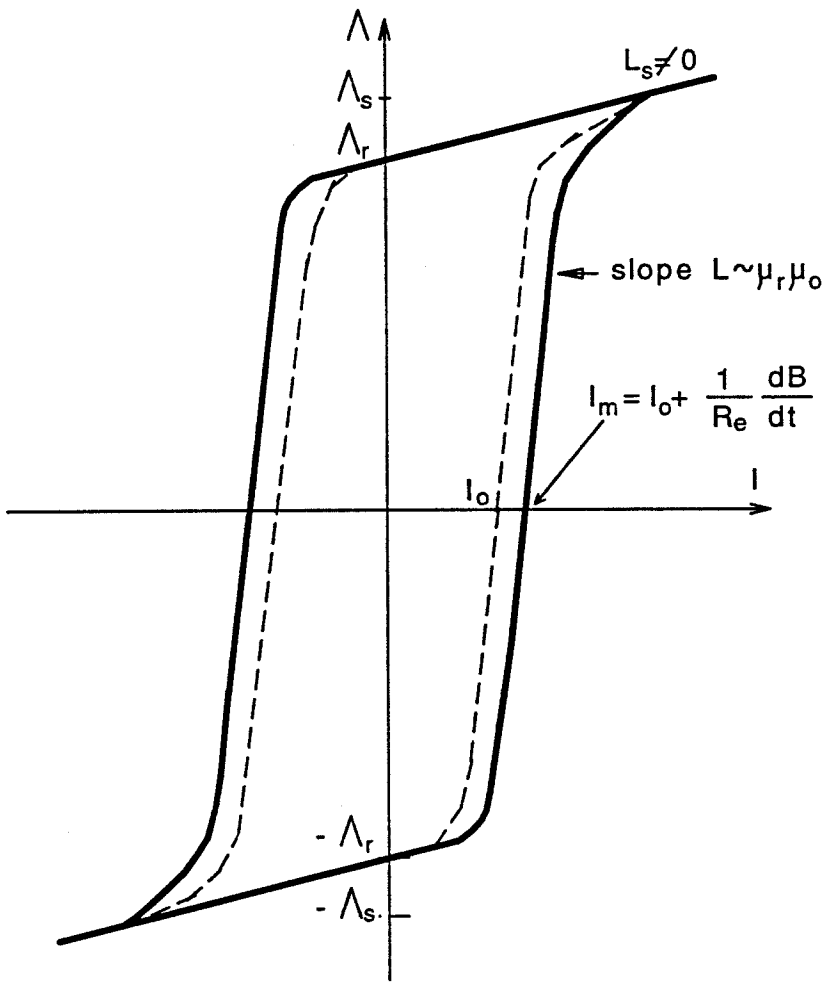


Figure 2.13: More realistic the $\Lambda - I$ characteristic of saturable inductor including essential non-linearities of core material.

static value I_o, and increases in proportion to the winding voltage $v_L = d\Lambda/dt$, or

$$I_e = I_m - Io = \frac{1}{R_e}\frac{d\lambda}{dt} \tag{2.14}$$

where, $R_e = 1/G_e$ is core resistance which describes eddy current loss.

MINIMUM BLOCKING CAPABILITY

Core squareness, defined as ratio between residual (zero-excitation) and saturation flux density B_r/B_s causes a delay as the magamp switches into saturation. This delay (ideally zero) decreases the maximum available volt-seconds which can be applied to the output filter. As a consequence, the minimum input voltage required to maintain output regulation, is increased. This overhead is in addition to the diode voltage drop and voltage drop on the resistances normally included in the design.

Core squareness causes automatic reset of the core with $\Delta\Lambda = \Lambda_s - \Lambda_r$ when the secondary voltage switches from $+V_2$ to $-V_2$, even though no reset voltage was applied ($V_c = 0$ in Fig. 2.11. The reason for this is that the current in the saturable inductor, I_2, quickly falls down to zero when the negative voltage $-V_2$ is applied. At the same time, freewheeling diode $D4$ starts to conduct the difference between I_2 and I_{L_2} and shorts point A to the ground. When the current in the saturable inductor reaches zero, which corresponds to flux Λ_r, forward diode $D3$ turns-off and the entire negative voltage $-V_2$ appears across it. Consequently, the voltage on the saturable inductor is zero (V_c=0) and the flux in the core remains at Λ_r during the entire reset cycle. This $\Delta\Lambda$ must be traversed during the forward blocking period and corresponds to the minimum volt-seconds blocking of

$$V_g\theta_{sq} = \Lambda_s - \Lambda_r \tag{2.15}$$

which must be accounted for in the average applied voltage.

Saturated inductance also delays the positive voltage pulse at the output filter L_2C_2 (point A in Fig. 2.11), and therefore, reduces the effective duty ratio of the regulator. As the core enters saturation, the current in the saturable inductor I_2 starts to increase from zero toward the output inductor current I_{L_2}. Voltage $V_A = 0$ until I_2 reaches I_{L_2} at which time the freewheeling diode $D4$ turns-off and the secondary voltage appears at

the output filter. This additional blocking is given by:

$$V_g\theta_{si} = L_s I_{L_2} \tag{2.16}$$

where, L_s is the saturated inductance given by

$$L_s = \frac{\mu_s S N^2}{l}. \tag{2.17}$$

The saturated permeability, μ_s, is not a specified data sheet parameter and is usually determined experimentally by measuring L_s in the circuit and then calculating it from Eq. (2.17). In [9], μ_s is measured for different sizes of square permalloy 80 material and was found in range from $10\mu_o$ to $36\mu_o$. It was suggested to increase these values by 30% to account for the added delay during transition at the $B - H$ loop knee.

In summary, a magamp can be used in a very efficient way as a controllable voltage bidirectional switch. By knowing its limitations, it will be possible to analyze how it affects the operation of the magamp as a controllable switch in any particular circuit. Being a *time dependent* device, it combines *switching* and *modulator* functions into a single power device which can be very easily controlled using analog circuitry in contrast to other semiconductor devices.

Chapter 3

A Survey of Soft-Switching Converters

The purpose of this chapter is to review the main problems associated with switching losses and the different solutions proposed for their elimination. In Section 3.1, switching loss mechanisms due to reverse-recovery time of the power diodes and parasitic reactances are described. Different approaches to switching loss elimination are given in Section 3.2, while in Section 3.3 two different soft-switching mechanisms, widely used in practice, are briefly described.

3.1 Switching Loss Mechanisms in PWM Converters

The semiconductor device in a switching converter is subjected to simultaneous high voltage and high current during switching instants, *turn- on* and *turn-off*, which results in high switching stress. With increased demand for faster response and reduced size and weight, switching frequency is increasing toward the megahertz region where switching losses in conventional PWM converters become intolerably high.

The buck converter is shown in Fig. 3.1 (a) and typical waveforms for a continuous conduction mode of operation (CCM) are shown, as an example, in Fig. 3.1 (b). As in any other PWM converter, semiconductor switching devices exhibit *capacitive turn-on* and *inductive turn-off* switching. The problems of voltage spikes and discharging parasitic capacitances are both consequences of the discontinuity of the waveforms of PWM converters as shown in Fig. 3.1 (b).

The switching losses depend on different factors and are directly proportional to the switching frequency. It is therefore, necessary to analyze and understand the contribution of each of these factors to the total switching losses and to provide a mechanism for their reduction.

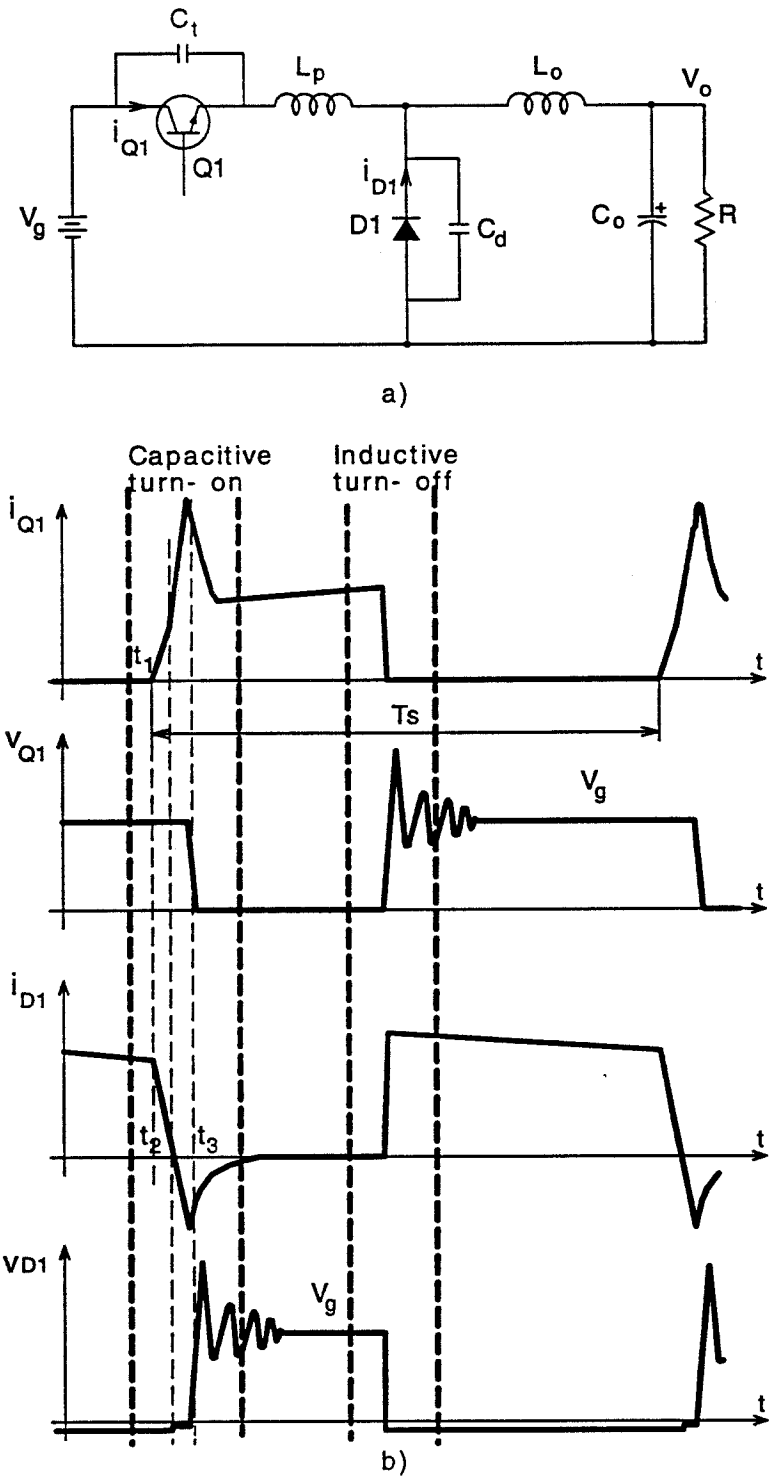


Figure 3.1: a) Basic buck converter and b) Salient waveforms during two switching transitions.

The switching frequency of PWM converters was able to increase along with the speed of available switching devices so long as the loss due to voltage/current overlap was the dominant limit on switching frequency. With very fast transistors, overlap loss is less important than the reverse recovery time of the diode and the problems of voltage spikes and discharging of the parasitic capacitance. These three loss mechanisms are briefly described next.

3.1.1 Switching Losses Due to Diode's Reverse Recovery Time

During the transistor's turn-on transition, shown in Fig. 3.1 (b), the diode $D1$ is still forward biased causing delay in voltage transition with respect to current transition. Once the diode $D1$ is turned off, voltage on the transistor $Q1$ decreases toward zero with a rate determined by the transistor itself.

Reverse-recovery current, which exists during the diode's turn-off, becomes a very serious problem at higher power levels and increased switching frequency. Switching waveforms during the transistor's turn-on transition (diode's turn-off) are shown in Fig. 3.2.

At instant $t = t_1$, the transistor $Q1$ is turned-on so the diode's current starts to decrease with slope $-di_F/dt$ (Fig. 3.2 (b)), limited by the leakage inductance L_p. The diode's current reaches zero at instant t_2 and continues in the negative direction. During the interval $t_s = t_3 - t_2$, called *storage time*, the diode $D1$ is still forward biased so the losses are low. On the other hand, the negative diode current appears as the transistor's turn-on current in addition to the load current, which as a consequence also increases losses in the transistor.

At the end of the storage time ($t = t_3$) the diode's negative current reaches its maximum, the diode becomes reverse biased and the input voltage appears across the diode (Fig 3.2 (d)). During recovery time, $t_{rec} = t_4 - t_3$, current through diode decreases exponentially toward zero. Since the diode is subjected to simultaneous high voltage and high current, power loss is relatively high during the recovery time. Switching losses, caused by the diodes reverse-recovery current, can be reduced by using a faster diode, and by limiting both magnitude and slope of the negative diode's current.

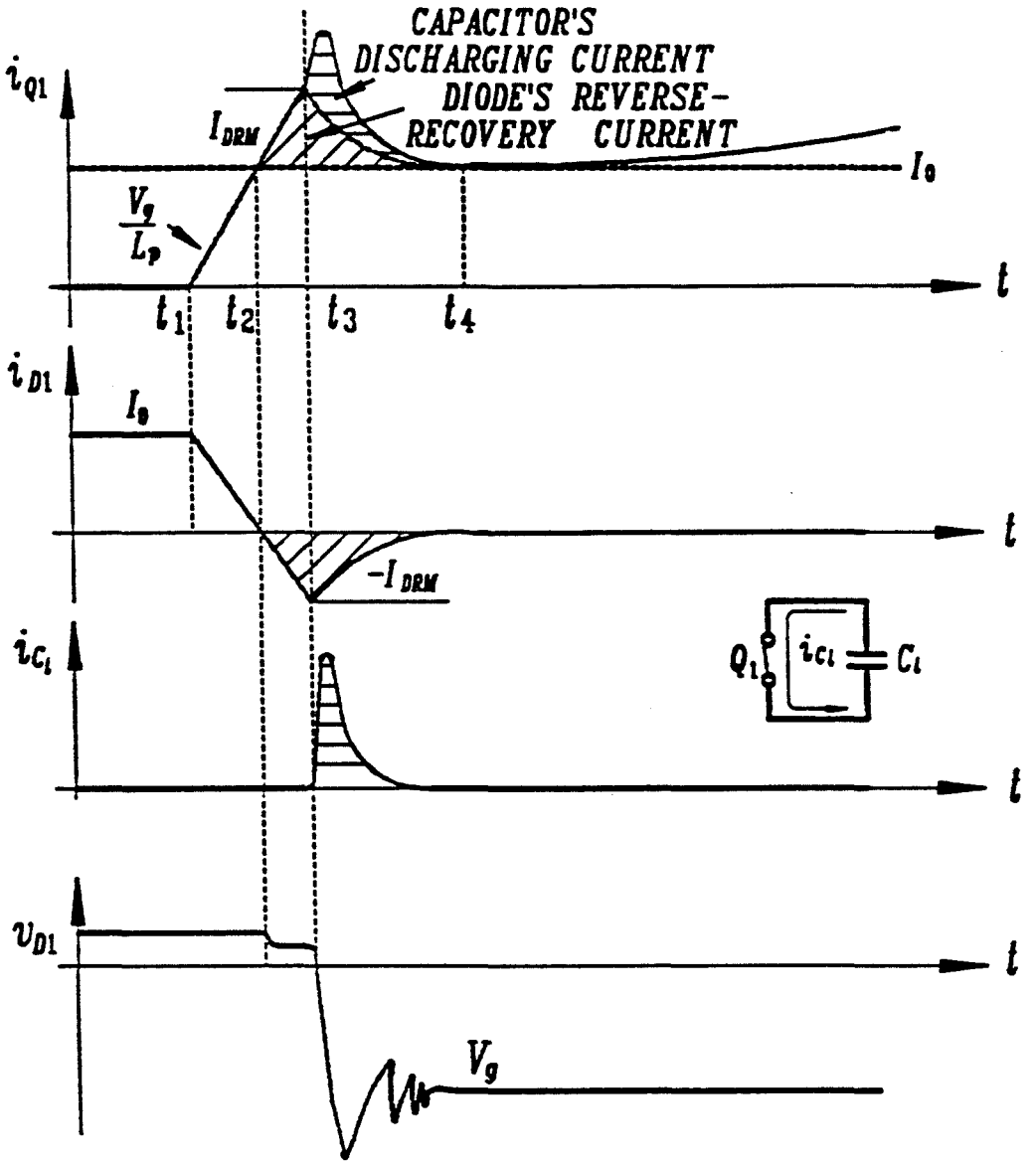


Figure 3.2: Switching waveform during the transistor's turn-on transition showing switching loss mechanisms due to reverse recovery of the diode and parasitic capacitance and inductance.

3.1.2 Switching Loss Mechanism Due to Parasitic Capacitance

The presence of the parasitic capacitance causes the power device to operate in capacitive turn-on. The parasitic capacitance which contributes the most to the power dissipation is the device's output junction capacitance. In every switching cycle, charge stored during the turn-off transition in the junction capacitance is dumped into the transistor during the turn-on transition.

Discharging current is only limited by the transistor's switching speed, which results in high di/dt and high current magnitude as shown in Fig. 3.2 (c). Furthermore, turn-on at high voltage levels induces a severe switching noise known as the Miller effect which is coupled into the drive circuit, leading to significant noise and instability. The parasitic capacitance across the switch is, on the other hand, helpful during the turn-off transition because it reduces dv/dt on the switch and consequently reduces voltage/current overlap time.

The junction capacitance is a non-linear function of the applied voltage and can be approximated by

$$C_t \approx C_{to}\sqrt{\frac{V_{off}}{v_t}} \tag{3.1}$$

where, C_{to} is nominal capacitance, V_{off} is transistor's off voltage, and v_t is applied voltage to the transistor. Energy stored in the junction capacitance is given by

$$E_c \approx \int_0^{V_{off}} C_t v_t \, dv_t = \frac{2}{3} C_{to} V_{off}^2 f_s \tag{3.2}$$

while the power lost during the turn-on transition is

$$P_c \approx E_c f_s. \tag{3.3}$$

While not severe at lower switching frequencies, the capacitive turn-on losses become the dominating factor when the switching frequency is raised to the megahertz range. For example, a junction capacitance of 100pF when switched from 300V at 1MHz will induce a turn-on loss of 4.5W.

Therefore, the capacitive turn-on is undesirable because it is dissipative and increases EMI noise.

3.1.3 Switching Loss Mechanism Due to Parasitic Inductance

In general, parasitic inductance can be due to the circuit layout as well as device packaging, the transformer's leakage inductance, and equivalent series inductance (ESL) of capacitors and voltage source. Transistor's turn-on losses can be reduced if the parasitic inductance L_p is in series with the switches (inductance L_p in Fig. 3.1 (b)). The inductance L_p slows down the rate of the rise of the transistor's current, and therefore, reduces turn-on losses caused by the diode's reverse recovery current.

On the other hand, the parasitic inductance produces voltage spikes and oscillation on both switching devices during their turn-off transitions. The abrupt change of the current in the parasitic inductance (the diode's turn-off transition is shown as an example in Figs. 3.2 (b) and (c)), induces voltage spikes with high dv/dt, and magnitude proportional to the rate of the current change (di/dt) and the inductance L_p. In addition, the parasitic inductance L_p and the parasitic junction capacitance C_t, generate high-frequency oscillations and EMI noise. The energy stored in the parasitic inductance L_p during the conduction interval of the switch is given by

$$E_l = \frac{1}{2} L_p I_p^2 \tag{3.4}$$

where, I_p is the peak current in the parasitic inductance at the beginning of the turn-off transition. The power dissipated due to the stored energy E_l is

$$P_l = E_l f_s. \tag{3.5}$$

As can be seen from Eqs. (3.4)-(3.5), power loss due to parasitic inductance becomes very high at higher current levels and high switching frequency. For example, when a current of 4A is switched at 1MHz in a leakage inductance of only $1\mu H$, the corresponding power loss will be 8W! Therefore, inductive turn-off is undesirable and should be avoided if the switching frequency is high.

In summary, even though the switching speed of semiconductor devices was drastically increased in the past decade, conventional PWM converters cannot be operated at a high switching frequency without significant degradation in overall efficiency. The main reasons for this are the diode's reverse recovery time and parasitic capacitances and inductances. The problems of voltage spikes and discharging of parasitic capacitance are

both consequences of the *discontinuity* of the (ideal) waveforms of PWM converters. If the current and voltage are smooth and slowly varying, the parasitic inductance and parasitic capacitance can be charged and discharged gracefully without losses. For the semiconductor devices it is preferable to have *inductive turn-on* and *capacitive turn-off*.

3.2 Different Approaches to Switching Loss Elimination

Different approaches have been proposed to prevent voltage and current waveforms from being discontinuous, i.e., make the converter insensitive to parasitic components – inductance and capacitance. Some of them are briefly reviewed in the rest of the chapter.

3.2.1 Resonant Converters

A *resonant converter* is defined as a power converter in which one or more switching waveforms, either voltage or current, contain pieces of sinusoidal, ringing waveforms [13]. This means that a switching waveform is a continuous, large-ripple voltage or current that starts from and returns to zero (Fig. 3.3). As a result, switching losses caused by voltage/current overlap as well as parasitic reactances can be effectively eliminated thus, allowing the switching frequency to be increased.

Without going into detail on how these waveforms are achieved, it can be stated that, in general, a resonant converter usually contains a resonant circuit in the classical sense: a series or parallel $L-C$ circuit with high Q factor produces quasi-sinusoidal waveforms when driven.

Switching loss due to voltage/current overlap is eliminated by having either the switch voltage or current waveforms continuous. In both cases, one of the switching transitions, the turn-off for *zero-current* switching (ZCS) or turn-on for *zero-voltage* switching (ZVS), are uncontrollable and determined by the resonant circuit itself.

Resonant waveforms also eliminate switching losses due to parasitic reactances and overcome problems associated with these parasitics. Having current waveform with sufficiently low di/dt, the voltage spike with magnitude Ldi/dt, generated in parasitic inductance, is no longer dangerous and parasitic oscillations are eliminated. In addition, energy stored in the parasitic inductance can be recovered instead of being dissipated in

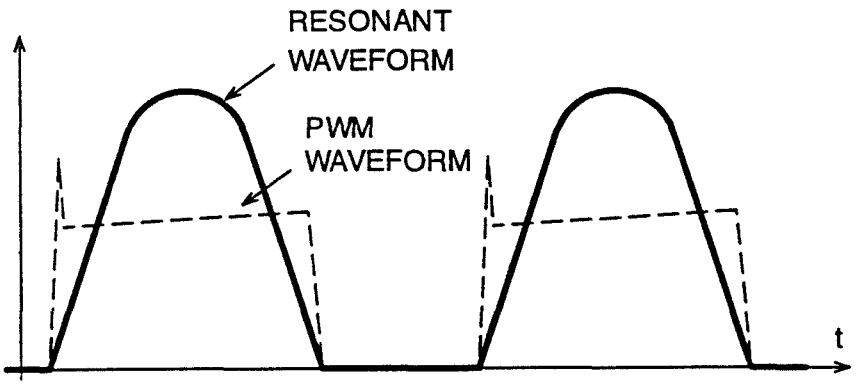


Figure 3.3: Typical waveforms in resonant converter.

snubber circuits and switches.

A continuous switch voltage waveform with low dv/dt prevents the loss due to discharging parasitic capacitance through the transistor. The parasitic capacitance is gracefully discharged and its energy is recovered rather then lost. Parasitic reactances can be constructively *used* in some cases to help in generating the large-ripple resonant waveforms as a part of the resonant circuit. Insensitivity of the resonant converter to parasitic inductance is very helpful in practical design when the transformer must satisfy "creepage" requirement or needs to be wide and flat due to packaging requirements.

Resonant switching waveforms solve the noise problem due to voltage spikes, high frequency parasitic oscillations and "snappy" reverse-recovery of the rectifiers. On the other hand, as a consequence of increased switching frequency, a resonant converter may, in order to meet harmonic limit such as for MIL-STD-461B, require nearly as large a filter as a PWM converter operated at lower frequency.

Resonant converters have some serious drawbacks which limit their wide mass production. These drawbacks are: increased component stresses, large circulating reactive energy, restricted operating region, difficult analysis, variable switching frequency, and

complex control.

Resonant waveform in Fig. 3.3 (solid line) has higher peak and r.m.s. values than rectangular waveform of PWM converter (dashed line) for the same average value. Consequently, the resonant converter suffers from higher peak stresses and poorer form factors than its PWM counterpart. The higher stresses imply poorer utilization of the power switches, while the higher r.m.s. current increases the conduction losses in magnetic windings and switch ON-resistance. In general, at least one of the switch waveforms, voltage or current, will have higher peak and r.m.s. values than in corresponding PWM converter, and the extra stresses usually propagate to other components in the converter.

In most cases, the variable-frequency control must be used for output voltage/current regulation. The variable-frequency control has several drawbacks: magnetic components have to be designed for full range of the operating frequency, and noise control becomes more complicated. Also there is possibility of entrainment. When the variable-frequency control is used, the noise generated by the converter can move constantly over a wide frequency range so the filter design is made much more difficult. Entrainment is an effect in which the switching frequency of a converter with variable-frequency control locks onto some noise source. Both of these problems are very often dominant arguments for not using resonant converters.

The constant frequency control of resonant converters is possible by using multiple switches [14, 15], electrically variable or saturable magnetic elements [16], and variable capacitances. The latter two methods change the resonant frequency and hence the conversion characteristics of the converter.

The existence of multiple operating modes together with wide variation of the load and switching frequency presents problems for control circuits. A control circuit optimized for a particular mode of operation can be unappropriate or even unacceptable for another mode forced in by change in the load. Therefore, in many cases, converter can be designed for limited range of the load and input voltage variations.

Over several years, the interest in high-frequency power conversion has stimulated the conception of many resonant converter circuits. Plenty of them are available for every application, and each year several more are going to be introduced. Every one of

these topologies offers some particular combination of the following features: low-current stresses, low-voltage stresses, additional control, wide range of conversion ratio, low cost, and simplicity. There is no single topology which is superior in all these areas, so the choise of topology is left to the designer.

Quasi-Resonant Converters represent a different approach to resonant power conversion [17]-[19]. They are derived from conventional PWM converters by adding a few components (or utilize equivalent parasitic reactances) to implement resonant switching. These converters share certain features of their PWM parent converters, but they have all the advantages of resonant switching waveforms. Introduction of the resonant switch [17, 18], obtained by adding resonant elements to the ideal switch, has provided derivation of quasi-resonant converters from their PWM parent converters. The new family was given the name "quasi-resonant" to distinguish them from continuously-resonating converters.

The important fact is that all quasi-resonant topologies are *insensitive* to transformer leakage inductance. In addition, ZCS and ZVS topologies are insensitive to the parasitic capacitance of the main rectifier and transistor, respectively. Quasi-resonant converters provide different kind of zero-switching for the transistor and rectifier. The generalized synthesis procedure of quasi-resonant and multi-resonant converters is given in [20].

The main advantages of quasi-resonant converters are resonant, loss-less switching, low component count and relatively simple analysis and operation. On the other hand, the main drawbacks are very large current stresses and r.m.s. current in ZCS topologies and the voltage stresses in ZVS topologies if the load is allowed to vary widely, variable-frequency control like all single-ended resonant converters. By replacing rectifier diode with controllable switch (MOSFET) [21], the quasi-resonant converter can operate at constant switching frequency.

Quasi-resonant converters, introduced at the beginning, featured different kinds of switching for the transistor and for the main rectifier. Recently, a new class of quasi-resonant converters called *multi-resonant* converters, which features the same kind of switching (ZCS or ZVS) for both the transistor and rectifier, has been introduced. The converter contains, for ZVS case, two resonant capacitances and one resonant inductor

[22, 23]. The resonant frequency varies from one switched network to the next as one capacitor or the other is shorted. A ZVS multi-resonant converter also offers lower voltage stresses and wider load range than a ZVS quasi-resonant converter.

3.2.2 Soft-Switching Converters

Taking into account the pros and cons for both PWM and resonant converter topologies, the "ideal" topology would combine the best features of both families. This includes low switching losses, constant frequency operation, reactive components with moderate stresses and a wide control and load range.

Resonant elements in these converters are not used for energy transfer but they are used only during switching intervals to provide either ZCS or ZVS. During the rest of the switching period the converter behaves like the PWM converter. Resonant frequency is well above the switching frequency, and the resonant voltage is clamped by a rectifier or second switch after transition is completed. The waveforms between transitions look very much those in PWM converters.

There is a large variety of converters which belong to the class of soft-switching converters such as the "pseudo-resonant" full-bridge converter [24], the zero-voltage resonant transition (ZVRT) converters [25], phase-shifted full-bridge converter [33, 34, 36], soft-switching half-bridge converter with asymmetrical drives [26], saturable-reactor assisted soft-switching converters [27] and recently proposed soft-switching converters with magnetic amplifiers [32].

The "pseudo-resonant" full-bridge resonant converter is obtained from the full-bridge PWM converter by adding two "resonant pole" circuits which consist of an LC circuit used for ZVS of each bridge leg [24]. The converter is operated at constant switching frequency and the switch voltage stress is clamped to the input voltage while the current stress of the switches is increased.

The ZVRT converters differ from some of the ZVS quasi-square-wave converters only in rectifier circuit which employes a synchronous rectifier (realized by MOSFET in practice) as a second, controllable switch [25]. Due to the addition of the second controllable switch, constant-frequency control is allowed and both switches have ZVS.

The soft-switching converters are more promising for high-frequency applications than resonant converters and some of them will be briefly described in the next section.

3.3 Different Approaches to Soft-Switching in PWM Converters

3.3.1 Basic Principle of Soft-Switching Mechanism

Soft-switching mechanism is explained in the buck converter. In order to obtain zero-voltage switching at constant switching frequency, the active switch $Q1$ and rectifier diode $D1$ in the conventional buck converter from Fig. 3.4 (a) are replaced with composite, current bi-directional switches $S1$ and $S2$ (realized with MOSFET transistors in practice) as shown in Fig. 3.4 (b). Capacitors across both switches are included in order to model either device parasitic capacitance or the externally added capacitor. Loss-less, soft transition (zero-voltage switching) in switches $S1$ and $S2$ occurs during the time intervals when both switches are turned-off, and charge between their capacitors is exchanged in the resonant fashion.

While the soft transition from the top switch $S1$ to the bottom switch $S2$ is inherently provided by the positive inductor current, transition from the bottom switch $S2$ to the top switch $S1$ requires negative current source to oppose the positive load current flowing through the bottom switch. The simplest solution is to design already existing output inductor L such that its current is bi-directional with peak-to-peak magnitude greater than twice the DC load current, for all operating conditions of interest [25].

Inductor current waveform during switching period and equivalent circuits of the converter during two different transition intervals are shown in Fig. 3.5. Duration of the transition intervals is assumed to be short compared to the switching period T_s. The inductor current is constant during these intervals as represented by constant DC current sources in the equivalent circuits in Fig. 3.5 (b)-(c).

Transition from the top to the bottom switch (interval t_{t1} in Fig. 3.5 (a)) is initiated by turning-off the top switch. The constant, positive inductor current $I_{L_p} = I_L - I_o$ (Fig. 3.5 (b)) linearly charges the capacitor across the top switch, C_{S1}, toward positive voltage and discharges the capacitor across the bottom switch, C_{S2}, toward negative voltage simultaneously, as shown by the dashed lines in the switch voltage waveforms.

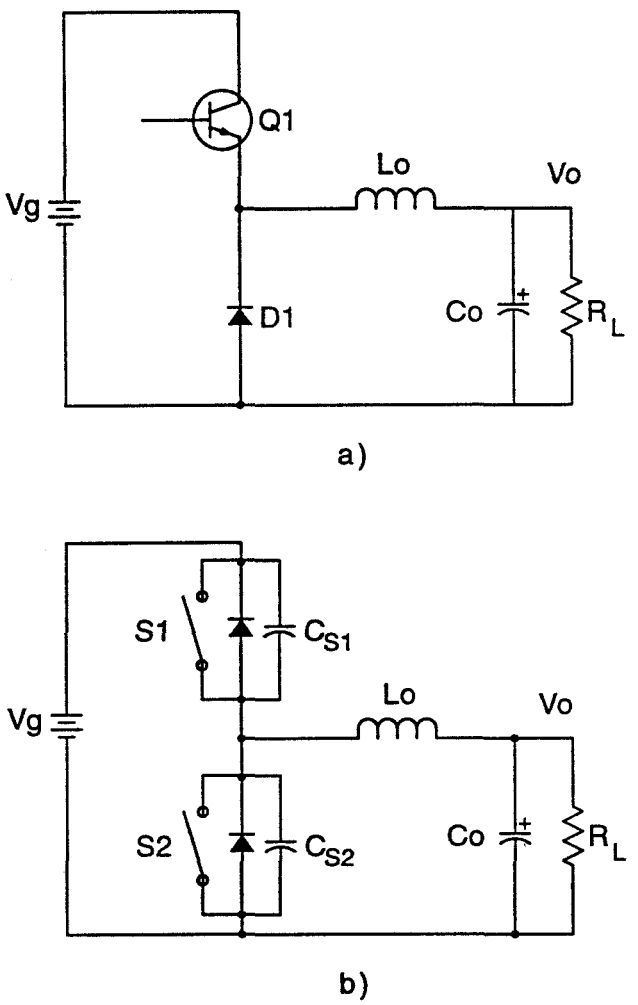


Figure 3.4: : a) Basic buck converter, and b) Soft-switching buck converter obtained by using composite switches S1 and S2.

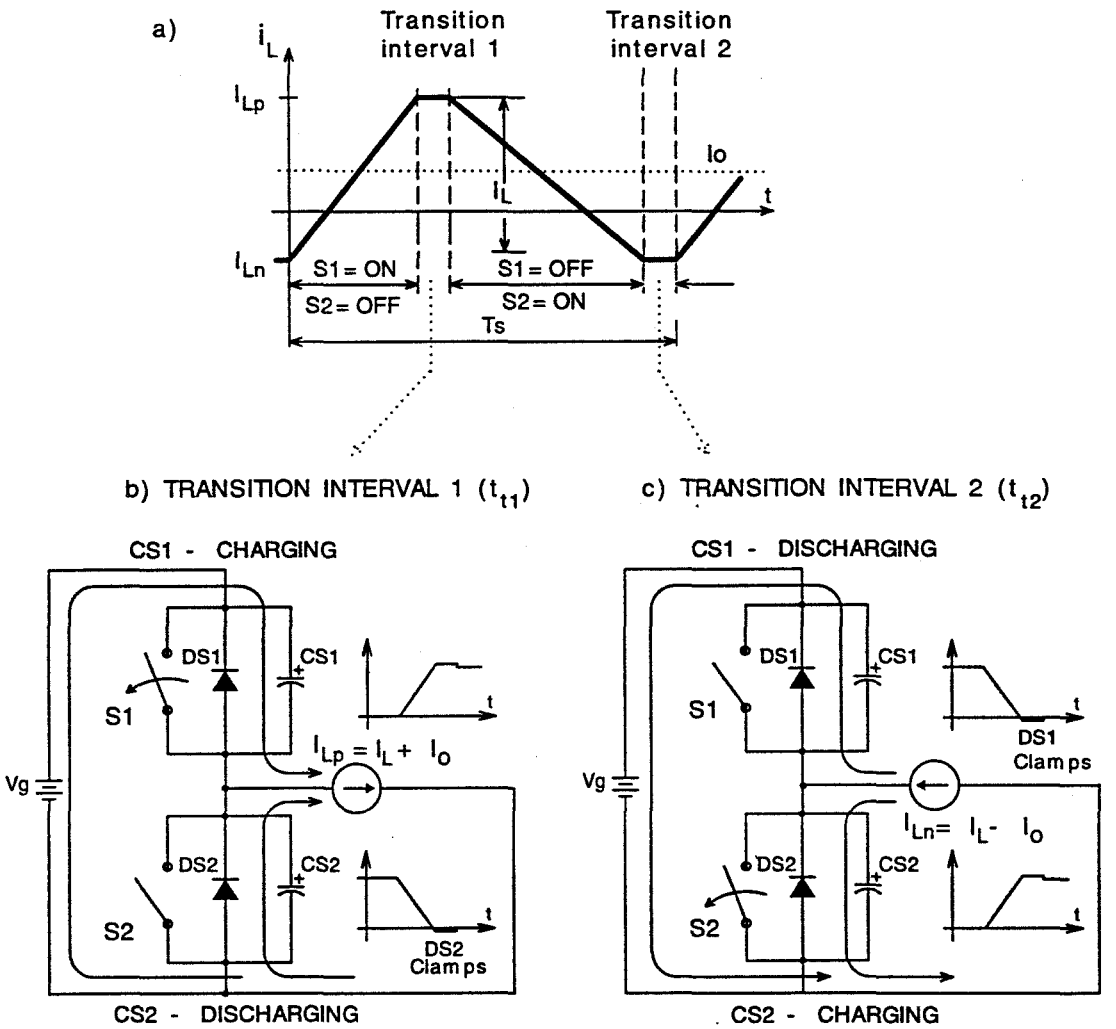


Figure 3.5: Soft-switching, provided by the bi-directional current source, is explained using equivalent circuits for two transition intervals.

Once the voltage on the bottom switch reaches zero, its diode D_{S2} becomes forward biased and clamps the bottom switch voltage to zero, and consequently clamps the top switch voltage at bus voltage V_g. The bottom switch can now be turned-on to zero voltage in a loss-less manner, which completes the first transition interval.

Transition from the bottom to the top switch (interval t_{t2}) starts by turning-off the bottom switch S2 carrying negative inductor current $I_{L_n} = I_L - I_o$ (Fig. 3.5 (a) which provides the opposite charge exchange between the switch capacitors. The bottom switch capacitor C_{S2} charges toward positive voltage and the top switch capacitor discharges toward negative voltage as shown by the dashed lines in Fig. 3.5 (c). Once the voltage on the top switch reached the bus voltage V_g, its diode D_{S1} becomes forward biased and clamps top switch voltage at zero and consequently the bottom switch voltage at V_g. The top switch ($S1$) can now be turned-on at zero-voltage in a loss-less manner, which completes the second transition interval t_{t2}.

Due to different inductor current levels I_{L_p} and I_{L_n}, transition from the top to the bottom switch is always shorter than the opposite transition from the bottom to the top switch particularly at high load currents. The amplitude of the inductor current, I_L has to be at least three to four times greater than the maximum load current in order to achieve soft-switching for all operating conditions, particularly at high switching frequency [25]. It results in increased conduction losses, increased core losses in the inductor, and requirement for additional output voltage filtering. The described soft-switching mechanism is inefficient at high load currents as well as at light loads, even though the loss-less switching can be achieved in a very simple manner and voltage stresses on the switches are the same as in the parent PWM converter.

The proposed soft-switching mechanism can be applied to any basic DC-to DC converter by [25]: a) replacing both transistor and rectifier diode with a composite switch (current-bidirectional switch in parallel with capacitor) realized by MOSFET in practice, b) driving both switches with small and well controlled dead-time, and c) designing the commutating inductor (can be either the output inductor or an additional inductor) such that zero-voltage switching can be achieved for any operating condition.

3.3.2 Soft-Switching Phase Shifted Full-Bridge Converter

The phase-shifted full-bridge converter is attractive because it utilizes all parasitics and can achieve ZVS of the primary side switches with a constant switching frequency [33]-[37]. The converter is controlled by phase-shifted (four-state) PWM control, as opposed to the parent circuit, the full-bridge converter with traditional (three state) PWM control.

The converter schematic and ideal waveforms are shown in Fig. 3.6 and Fig. 3.7, respectively. Primary side switches, $S1 - S4$, are composite switches realized with MOSFET transistors in practice. The inductance L_l represents either leakage inductance of the transformer or externally added inductance required for one transition interval. Capacitances $C_{S1} - C_{S4}$ represent parasitic capacitances of the composite switches $S1 - S4$, respectively.

Two switches in the same leg of the bridge, $S1 - S2$ and $S3 - S4$, are driven out of phase at 50% duty ratio with small dead-time t_a and t_b, respectively (Fig. 3.7). Drive signals for switches $S1$ and $S2$ are used as a reference. Their diagonal switches, $S4$ and $S3$, are driven with delay or phase shift θ as shown in Fig. 3.7 instead of in phase as in a conventional full-bridge converter. Output voltage is regulated by varying phase shift θ.

The state in which two diagonal switches are simultaneously conducting is called the *active state*, while the state in which two switches on the same side of the power bus are simultaneously conducting is called the *passive state*. During the passive state both rectifiers, $D1$ and $D2$, conduct simultaneously and short the transformer. Power is delivered to the load only during active state. Between active and passive states there are transition intervals, t_a and t_b, during which capacitances are charged and discharged simultaneously. In the following analysis transition intervals, t_a and t_b, are assumed short compared to switching period T_s.

The two legs of the bridge switch under different scenarios. The right leg switch, $S3$ or $S4$ in Fig. 3.6, is turned on after the freewheeling interval (passive state) to initiate the power delivery interval (active state). The right leg is also called the *leading* leg, because the power delivery leads in the power conversion process. The left leg switch, $S1$ or $S2$ (Fig. 3.6), is turned off to terminate the power delivery interval. Therefore, the

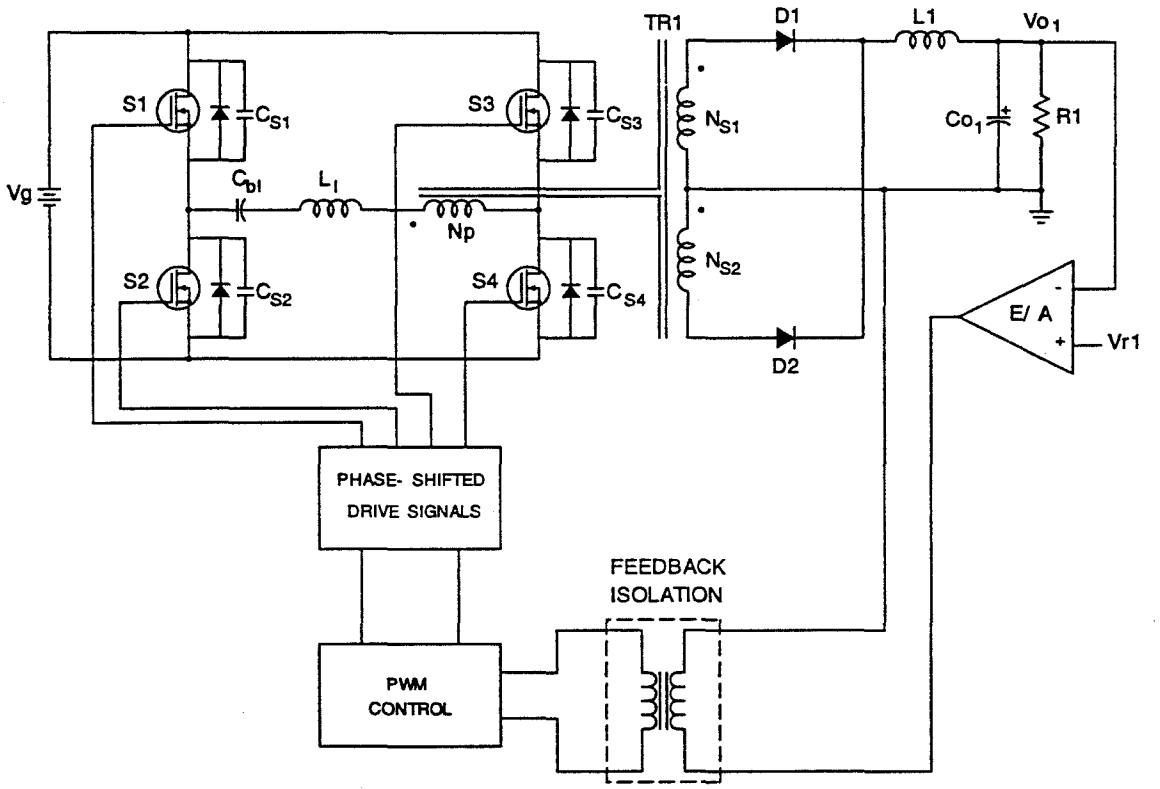


Figure 3.6: Phase-shifted full-bridge converter.

left leg is also called the *trailing* leg. The source of energy that displaces the charge of the parasitic capacitances $C_{S1} - C_{S4}$ is different for two legs.

In an ideal case without leakage and the magnetizing inductance, ZVS is possible only for the left leg switches while the right leg switches exhibit hard switching. During transition from active to passive state (t_a), the output inductor current is reflected to the primary and provides energy for charge displacement in capacitances C_{S1} and C_{S2}. The soft-switching mechanism is identical to the one described for the soft-switching buck converter in Section 3.3.1.

On the other hand, during transition from passive to active state (the right leg transition), t_b, transformer $TR1$ is shorted due to simultaneous conduction of both rectifiers ($D1$ and $D2$), primary current is zero and there is no available energy for charg-

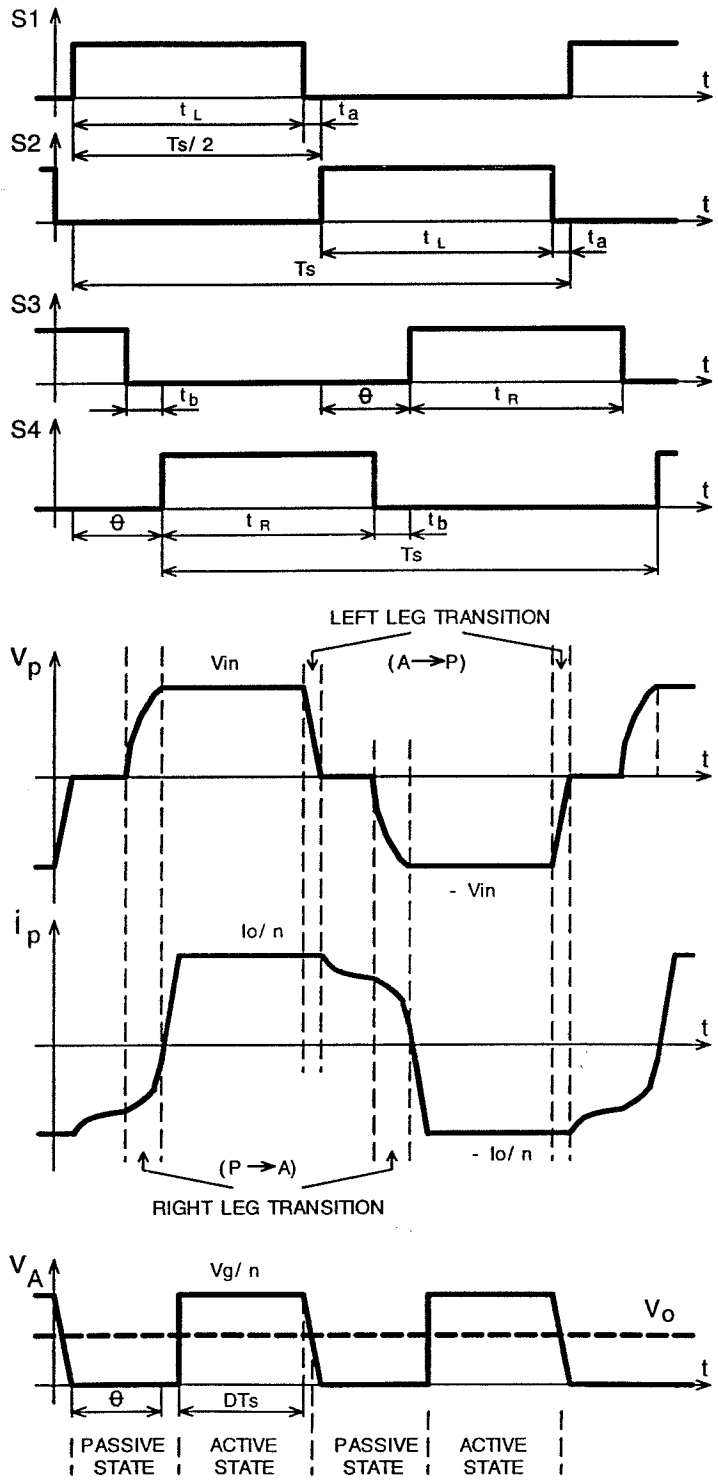


Figure 3.7: Ideal waveforms in phase-shifted full-bridge converter.

ing/discharging capacitances C_{S3} and C_{S4} in resonant fashion. Therefore, in order to provide ZVS in the right leg it is necessary to have inductance in series with the transformer (the inductance L_l in Fig. 3.6).

In summary, soft-transition from active to passive state is natural and provided by the reflected load current to the primary while transition from passive to active state is hard-transition and needs some additional source of energy–leakage inductance.

During active state the output inductor current is reflected to the primary, and energy $L_l I_p^2/2$ is stored in leakage inductance L_l. Leakage inductance is practically shorted, by the switches on the same side of the power bus during freewheeling state. Its current remains almost unchanged and circulates through the primary circuit. The right leg transition is then provided by the partial resonance between leakage inductance L_l and parallel combination of capacitances C_{S3} and C_{S4}. Achieving ZVS requires that energy stored in leakage inductance is large enough to provide maximum voltage on C_{S4} at least equal to bus voltage V_{in}. Also, maximum dead-time t_b is limited to one quarter of the resonant period $T_r = 2\pi\sqrt{L_l(C_{S3}\|C_{S4})}$ [37].

The difference in the left and right leg ZVS mechanisms is, therefore, the magnitude of reflected output inductance $L_{ref} = L/N^2$ and primary leakage inductance L_l. The reflected inductance L_{ref} is large enough to keep the primary current essentially constant during transition so voltage at the middle point of the right leg, P_L, changes linearly and very quickly. Consequently, dead-time in drive signals for the left leg switches, t_a, is short. On the other hand, since leakage inductance L_l is much smaller than L_{ref}, the voltage over L_l changes with charging/discharging of C_{S3} and C_{S4}. Voltage at the middle point of the right leg, P_R, changes in a sinusoidal fashion and thus, is slower than at the left leg's midpoint P_L. Dead-time in the driving signals for the right leg switches, t_b, therefore, depends on the resonant period T_r, the initial current in L_l (just before $S1$ or $S2$ are turned-off and bus voltage V_{in}. Therefore, zero-voltage switching is more difficult to achieve in the right leg (leading) than in the left leg (trailing).

In practice, the primary current decays exponentially during freewheeling interval as shown in Fig. 3.8 which further reduces available energy for the left leg transition. The time constant of the exponential decay is determined by the ratio R/L_l, where R is

the sum of all the resistances in the circulating current path (MOSFETs ON resistances, primary winding resistance). Increasing the leakage inductance will decrease the decay in primary current and increase the energy available for displacing charge on capacitances C_{S3} and C_{S4}, thus extending the soft-switching range. With this approach, the minimum leakage can be specified to achieve ZVS over a very wide range of input voltage and load [37].

High leakage inductance, however, can reduce overall converter efficiency. The leakage field in the transformer produces high eddy current losses in the windings. A high leakage inductance also limits di/dt and increases rise time of the primary current (Fig. 3.8). A consequence is that the crossover conduction time of the output rectifiers is increased which results in reduction of the effective duty ratio D_{eff} [37]. Compensating for the reduced duty ratio with a lower turns ratio in the transformer increases primary conduction losses and puts greater voltage stress on the output rectifiers.

The optimum leakage inductance is calculated in [38], and for a converter operating at frequencies up to several hundred kilohertz is relatively small. While the conduction losses are minimized because the resulting circulating current decays rapidly, there is a limited range of soft-switching, and the converter achieves ZVS at only full load. If the converter operates with soft-switching only for a very limited range of its desired operating range, it is unclear if any EMI filter volume reduction is possible.

In summary, the leakage inductance determines the efficiency and the range of soft-switching.

Extended ZVS Range

In order to extend ZVS operating range a saturable inductor is used in [39] as a resonant element instead of leakage inductance L_l. As a result, extended ZVS range with minimum circulating energy is obtained and the effective duty cycle of the converter is increased and parasitic oscillations between the diode junction capacitance and the resonant inductor are reduced. The switching frequency of the converter is limited to several hundred kiloherz, which is mainly determined by the core losses in the saturable inductor which operate with full flux capability, i.e., from positive to negative saturation. This mechanism is further extended by using non-controlled saturable inductors in series

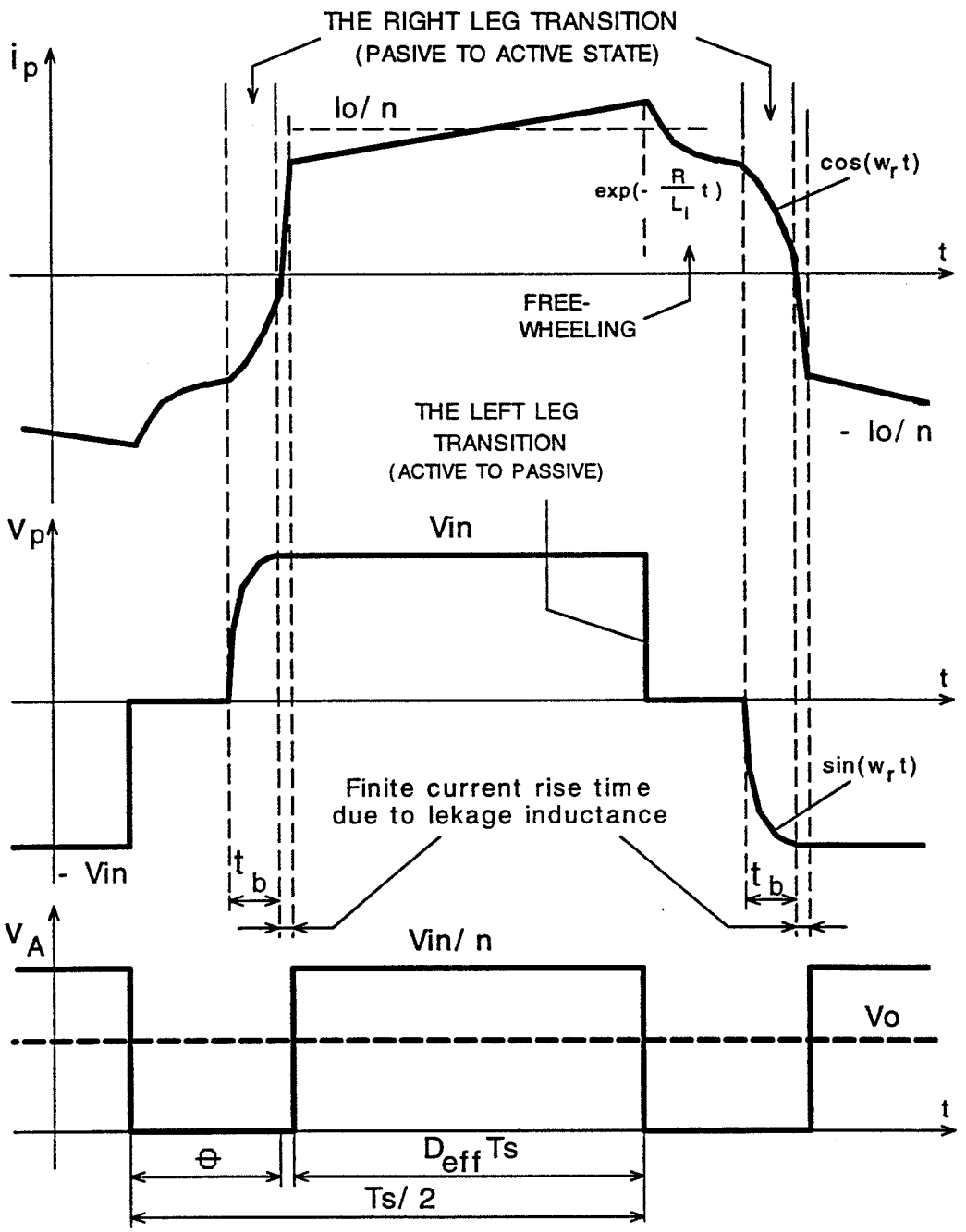


Figure 3.8: Detailed waveforms during the right leg transition when leakage inductance L_l is small.

with the rectifiers as also proposed in [41]. The core losses are significantly reduced since saturable inductors operate with flux swing only in the first quadrant.

A new method is described in [40] that uses magnetic amplifiers in series with the output rectifiers to adaptively adjust the converter's circulating current. The method regulates the minimum circulating current required to achieve ZVS while the output voltage unaffected. Thus, the output voltage is still controlled by phase-shifted modulation on the primary side. Magnetic amplifiers also act as snubbers for the output rectifiers and reduce EMI noise generated during the turn-off of the rectifiers.

Soft-switching of the Rectifiers

In addition to the above mentioned disadvantages, there is also a very serious disadvantage related to the reverse-recovery problem of the rectifiers. Phase-shifted full-bridge topology, however, does not provide any means of absorbing the parasitic capacitances of the rectifier diodes. The interaction of rectifier capacitances with large leakage inductance of the transformer (required for extended ZVS range) causes severe voltage overshoot and ringing across the rectifiers. The use of dissipative RC snubber in the secondary is impractical particularly at high switching frequencies and in high-voltage, high-power applications, where the reverse recovery time of the rectifiers is excessive.

Several solutions to this problem have been suggested. Using clamp circuit across the rectifiers, as suggested in [35], is the simplest solution but not effective in reducing parasitic ringing and improving efficiency. Another approach which uses a low-leakage power transformer with a separate inductor and two clamp diodes in the primary circuit is suggested in [36]. This additional circuit essentially eliminates the dynamic losses and the overshoot and ringing of junction capacitances. It also helps in the right leg transition without requiring excessive magnetizing current in the transformer. An active snubber, consisting of a capacitor in series with composite switch (MOSFET), is connected across the rectifiers in [42]. Voltage overshoot and ringing are essentially eliminated in a nondissipative manner which makes this circuit very efficient particularly in high-voltage, high-power applications. The disadvantage of the proposed active snubber is the need for an additional active switch.

To summarize, the soft-switching phase-shifted full-bridge converter utilizes all par-

asitics and is widely used for high power applications above a few hundred of watts. However, its main drawbacks are: a) additional components are needed to achieve an extended range of ZVS, b) additional components are needed for the soft turn-off of the rectifier diodes, c) the control circuitry is complex, and d) there is a need for the feedback isolation.

Chapter 4

A Novel Soft-Switching Half-Bridge Converter With Magamps

A novel half-bridge DC-to-DC converter combines the functions of loss-less, soft-switching and secondary side output voltage regulation at constant switching frequency. This was made possible by using magamps in series with the rectifier diodes [32]. The primary side switches are driven at constant frequency and 50% duty ratio with small dead-time and the output voltage is regulated by PWM control of the magamps on the secondary side.

In Section 4.1, a conventional half-bridge converter is briefly reviewed. Section 4.2 describes a novel soft-switching half-bridge converter. The proposed soft-switching mechanism is compared with other solutions in Section 4.3. The output voltage regulation is explained in Section 4.4, while different realizations of the voltage bidirectional switches on the secondary side are discussed in Section 4.5. Extended range of soft-switching and simple solution for reduction of the circulating current are given in Sections 4.6 and 4.7. Experimental results obtained on 250W-48V prototype operated at 200kHz are given in Section 4.8.

4.1 Conventional Half-Bridge Converter

A conventional half-bridge converter and idealized waveforms are shown in Fig. 4.1 and Fig. 4.2, respectively. Two equal capacitors $C1$ and $C2$ are connected in series across the DC power supply V_g to enable an artificial mid-point P_M to be created. The primary side switches $S1$ and $S2$ are driven alternatively during each switching period with duty ratio $D = \tau/T_s$. Full-wave rectification on the secondary side is provided by center-tapped secondary winding and rectifier diodes $D1$ and $D2$. The output voltage

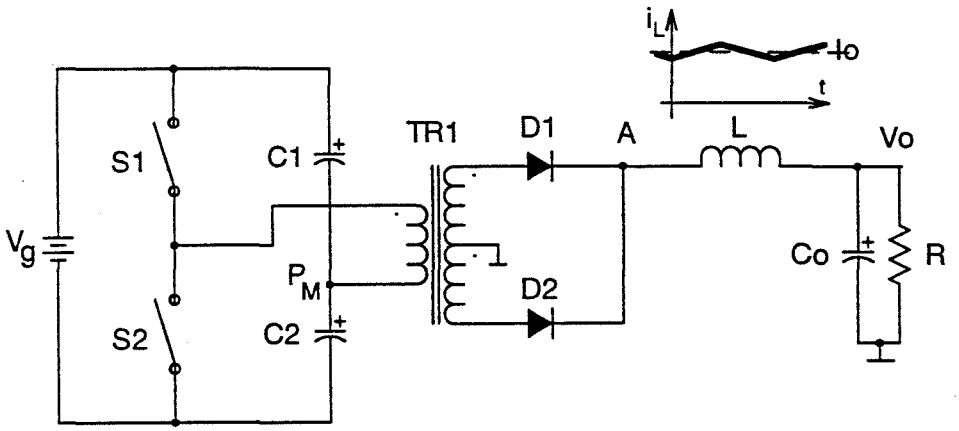


Figure 4.1: A conventional half-bridge converter.

V_o is regulated by varying duty ratio D. The transformer's turns ratio is assumed to be $N = 1$.

One can distinguish two successive operating states, active and passive during each half of the switching period T_s (Fig. 4.2). During active state τ, the corresponding pair of the primary switch and rectifier diode ($S1 - D1$ or $S2 - D2$) conduct simultaneously so the primary voltage and current have the same polarity and the power is delivered from the source to the load. Positive voltage of magnitude $V_g/2$ is applied at the point A and energy is stored in the output inductor L. Contrary, during passive state t_d, the both primary side switches are OFF but the rectifier diodes ($D1$ and $D2$) conduct inductor current simultaneously and short the transformer. As a consequence of that both the primary voltage and current are zero and no power is delivered from the source to the load. Energy stored in the output inductor during active state is now released into the load through the rectifier diodes. This operating state is also called freewheeling state due to the nature of energy transfer.

Soft-switching is not possible because the transformer is shorted by the rectifier diodes just after one of the primary side switches ($S1$ or $S2$) is turned-OFF so both switches, $S1$ and $S2$ are connected instantaneously to the mid-point P_M at voltage $V_g/2$ and stay there during dead-time t_d. Capacitors across the primary switches, charged at the $V_g/2$

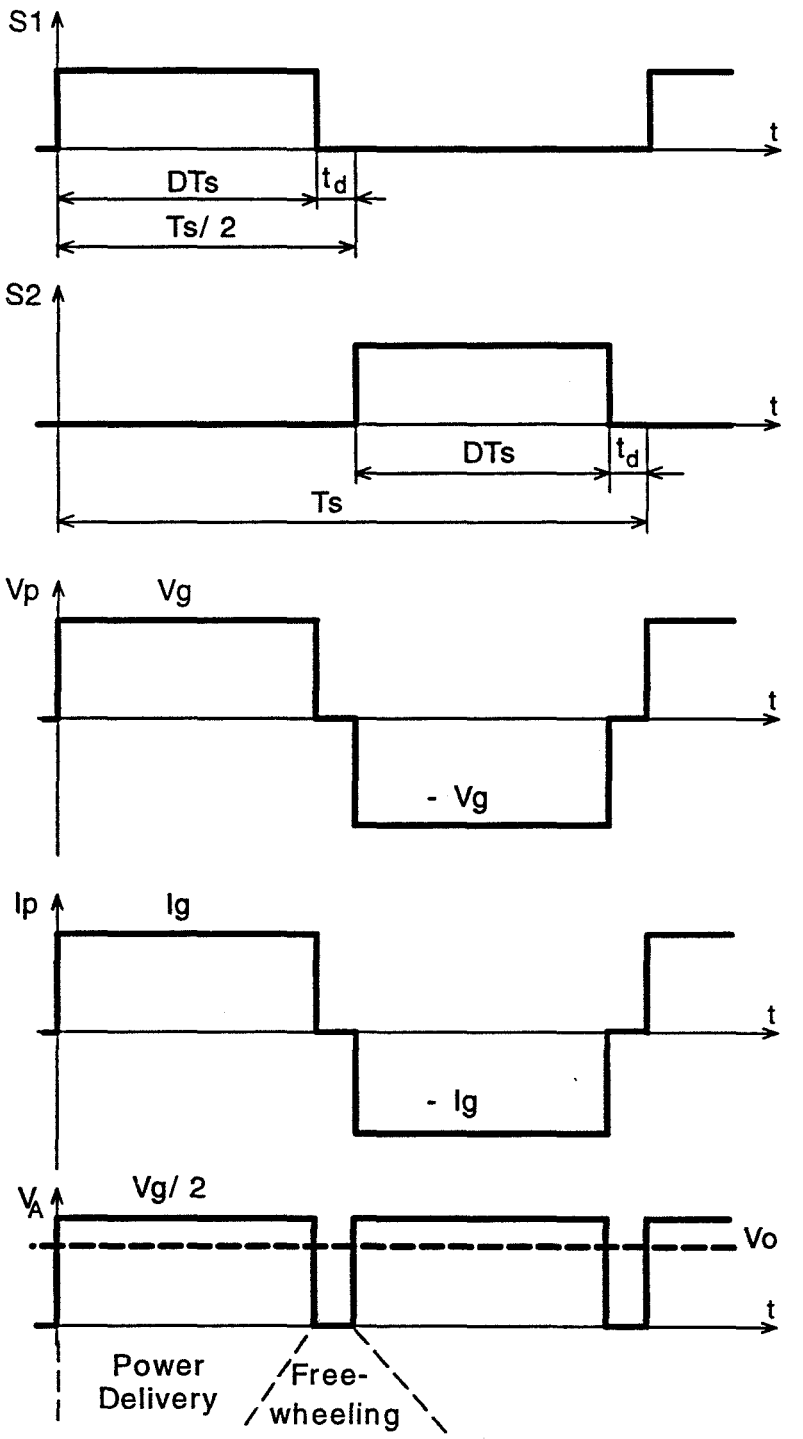


Figure 4.2: Idealized waveforms in the conventional half-bridge converter.

during t_d are discharged through the switches in lossy manner. It is, therefore, necessary to prevent shorting of the transformer during freewheeling states.

Different mechanisms for soft-switching in half-bridge have been proposed recently [23], [26], [27] and [43]. In this chapter a novel soft-switching half-bridge converter is proposed [32] and is described next.

4.2 A Novel Soft-Switching Half-Bridge Converter

4.2.1 Circuit Description

A novel soft-switching half-bridge converter is shown in Fig. 4.3. There are four main differences between proposed topology and the conventional half-bridge converter from Fig.4.1:

1. The primary side switches $S1$ and $S2$ are composite, current bi-directional switches (MOSFETs in practice)

2. The primary side switches are driven alternatively at fixed duty ratio close to 50% with small dead-time t_d (Fig. 4.4)

3. Rectifier diodes $D1$ and $D2$ are replaced with controllable, voltage bi-directional switches $S3$ and $S4$, respectively

4. Output voltage is PWM regulated by controlling the secondary side switches instead of the primary side switches

Both soft-switching of the primary side switches $S1$ and $S2$, and output voltage regulation are obtained by using voltage bi-directional switches $S3$ and $S4$ with appropriate drives.

4.2.2 Soft-Switching Mechanism

Idealized waveforms during a switching period and equivalent circuits of the converter during two transition intervals are shown in Fig. 4.4 and Fig. 4.5, respectively. The output inductor L (Fig. 4.3) is assumed to be infinitely large so it is replaced with constant dc current source I_o in the equivalent circuits in Fig. 4.5.

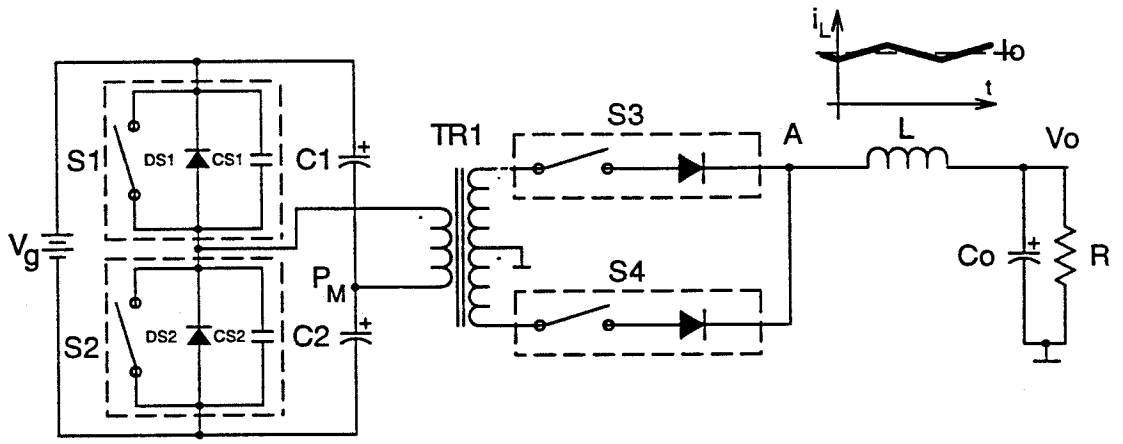


Figure 4.3: A novel soft-switching half-bridge converter.

The primary side switches, $S1$ and $S2$, are driven alternately at fixed duty ratio close to 50% with small dead-time t_d, while the secondary side switches are driven alternately at exactly 50% duty ratio as shown in Fig. 4.4. During the first transition interval both primary switches are open but only one of the secondary side switches is forced to conduct the load current ($S3$ closed and $S4$ open as in Fig. 4.5 (a)). The transformer is, therefore, never shorted. The primary current is maintained in the same direction during dead-time as it was before the primary switch is turned-OFF (dashed area in the primary current waveform in Fig. 4.4), so the soft-transition of the primary side switches is naturally provided as shown in Fig. 4.5 (a).

The primary current, being reflected DC load current I_o, naturally changes polarity between two transition intervals. Thus, soft-switching is also naturally provided during the second transition interval when $S3$ is open and $S4$ is closed as in Fig. 4.5(b).

Transition between the primary side switches is under the same scenario as described for the soft-switching buck converter in Section 3.3.1 with the only difference in the commutating current. Since in this case, the commutating current is reflected load current to the primary, both transitions are natural and equal (Fig. 4.4).

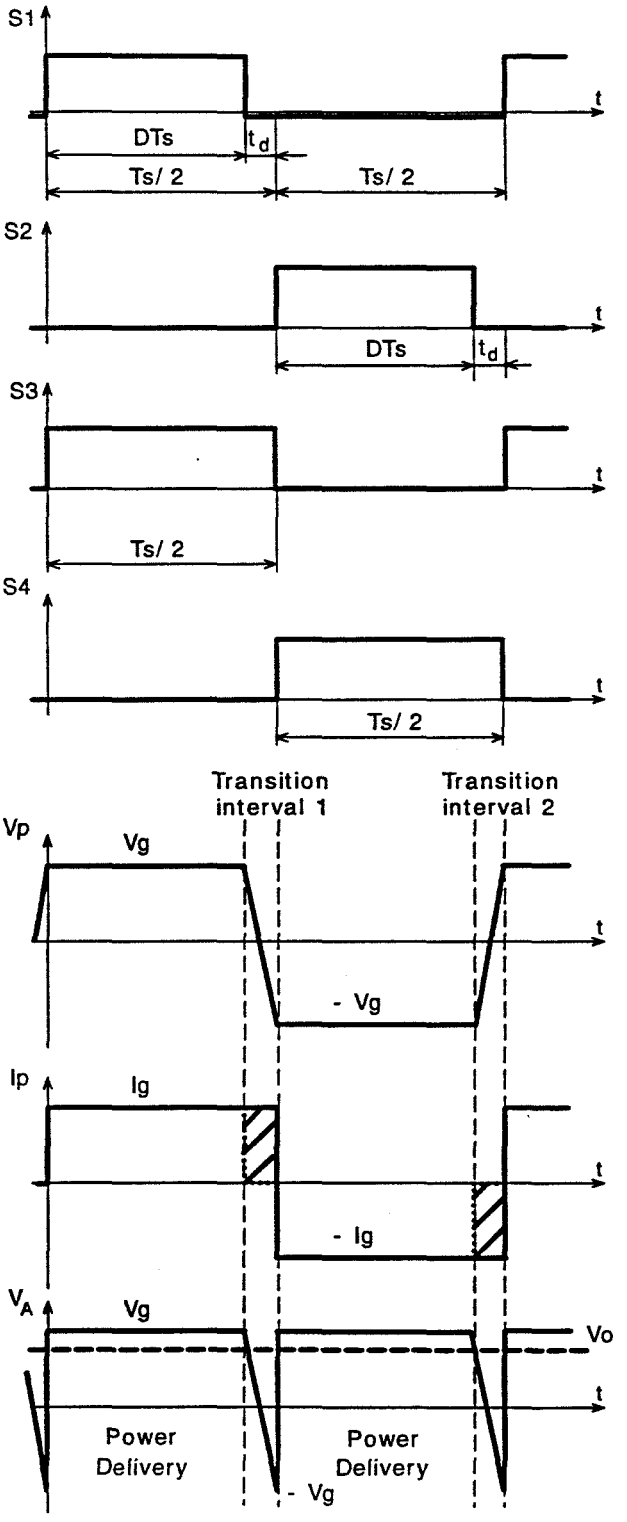


Figure 4.4: Soft-switching in the novel half-bridge converter is obtained by driving the primary side switches $S1$ and $S2$ at 50% duty ratio with small and well controlled dead-time t_d, and the secondary side switches $S3$ and $S4$ at exactly 50% duty ratio.

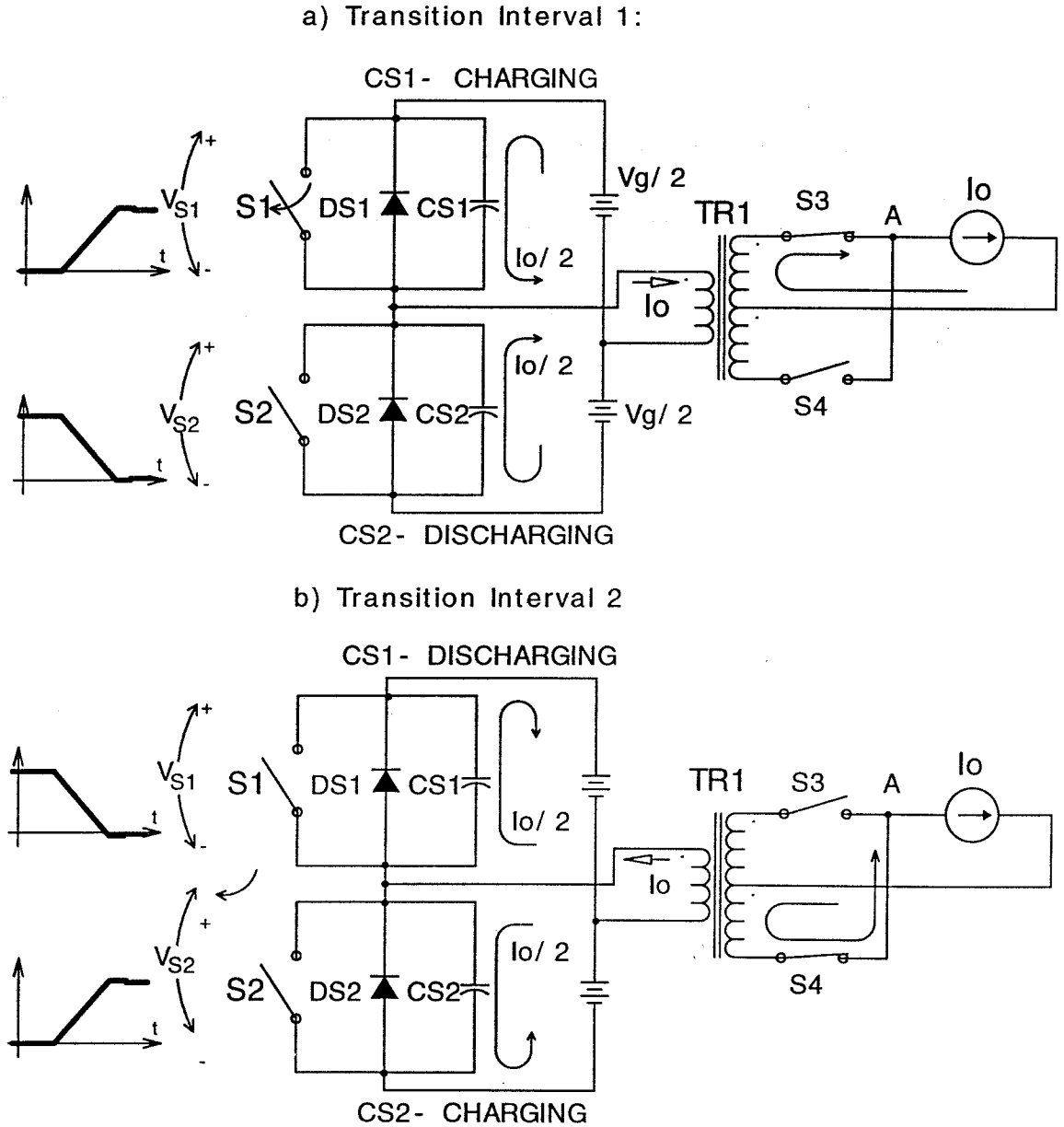


Figure 4.5: Equivalent circuits of the novel soft-switching half-bridge converter during two transition intervals. Output inductor is replaced by the constant current source for simplicity.

4.3 Comparison of Soft-Switching Mechanisms

The main, and very important difference between proposed soft-switching mechanisms and one described for buck converter in Section 3.3.1 is in the commutating current. Soft-switching mechanism in the half-bridge converter, even though similar to that in the buck converter, user transformer's inherently bi-directional primary current (reflected DC load current) (Fig. 4.4) instead of the bipolar triangular inductor current with large ripple (Fig. 3.5). As a consequence of that, conduction losses in the switches, copper losses in the windings, and core losses in the output inductor, having (almost) DC current, are also reduced compared to the soft-switching buck converter.

Moreover, duration of the transition intervals are the same compared to other solutions in which turn-ON and turn-OFF transitions can differ an order of magnitude due to different soft-switching mechanism during transition intervals, unless some additional circuitry is added.

Proposed soft-switching mechanism is also different from that suggested in [23] which uses the transformer's magnetizing current for soft-switching. The main disadvantages of this solution are: a) magnetizing current needs to be relatively large to keep transition intervals short, b) freewheeling diode is essential for the soft-switching. Note that the proposed soft-switching half-bridge converter operates without need for freewheeling diode.

Soft-switching half-bridge converter with asymmetrical drives is proposed in [26] and this approach is then extended to the whole family of saturable reactor assisted soft-switching converters [27]. The main disadvantages of these converters are: a) large magnetizing current of the transformer and b) output voltage is regulated by PWM modulation of the primary side switches so there is need for the feedback isolation.

In [43] soft-switching half-bridge converter which uses auxiliary active switch in series with output is proposed. Output inductor is moved to the primary side and together with magnetizing inductance provides soft-switching transitions. The main disadvantages of this solution are : a) high current stresses, b) need for additional switch which has to carry load current and c) auxiliary switch needs to be synchronized with the primary side switches.

The proposed novel soft-switching half-bridge converter with magnetically controlled amplifiers eliminates the key disadvantages of the other solutions while keeping the simplicity of original pulse-width-modulated (PWM) converter as described next.

4.4 Output Voltage Regulation

The main drawback of the described soft-switching half-bridge converter from Fig. 4.3 is that there is no output voltage regulation if the secondary side switches are driven as shown in Fig. 4.4. In order to provide the output voltage regulation it is necessary to vary duration of the interval during which voltage v_A is negative, which occurs when the primary voltage and current are out of phase. The secondary side switches $S3$ and $S4$ are still driven out of phase with fixed 50% duty ratio but their drive signals are delayed by variable time θ (Fig. 4.6 (c)) with respect to original drive waveforms (Fig. 4.6 (b)).

In addition to active and passive state in the conventional converter (Fig. 4.1) there is soft-transition state t_d in the new converter (Fig. 4.3). The soft-transition always occurs when the converter moves from active to passive state, as shown in Fig. 4.7, and consequently is natural transition. While the active states in the new converter are the same as in the conventional half-bridge converter, the behavior of the new converter is completely different during passive (freewheeling) state.

During active state τ , the corresponding pair of the primary and secondary switches ($S1$-$S3$ or $S2$-$S4$) conduct simultaneously providing power deliver from source to the load. Contrary, during passive state θ, the primary side switch conducts simultaneously with opposite secondary side switch ($S1$-$S4$ or $S2$-$S3$) making transformer's voltages and currents out of phase. As a consequence, the load current circulates through the primary circuit and negative voltage is applied on the output filter LC_o (point A in Fig. 4.3). Soft-transition state exist only between active and passive state, while transition from passive to active state is instantaneous.

The output voltage regulation is therefore, achieved by varying duration of the passive states which corresponds to delay time θ in drive signals of the secondary side switches $S3$ and $S4$ (Fig. 4.7). Duty ratio of the converter is defined as a portion of the switching period during which both voltages and currents in the transformer windings have the

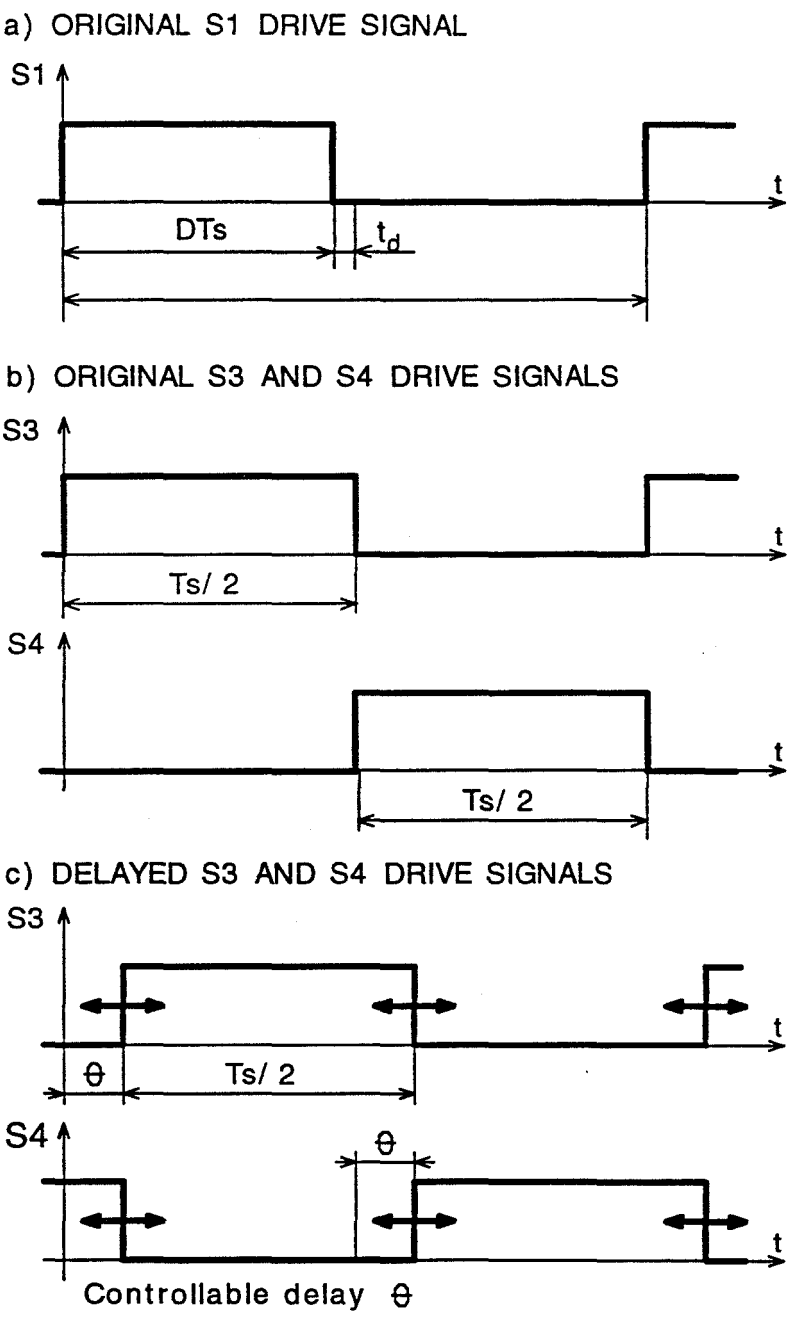


Figure 4.6: Output voltage regulation is provided by delaying the drive signals for the secondary side switches S3 and S4, in respect to the drive signal for S1.

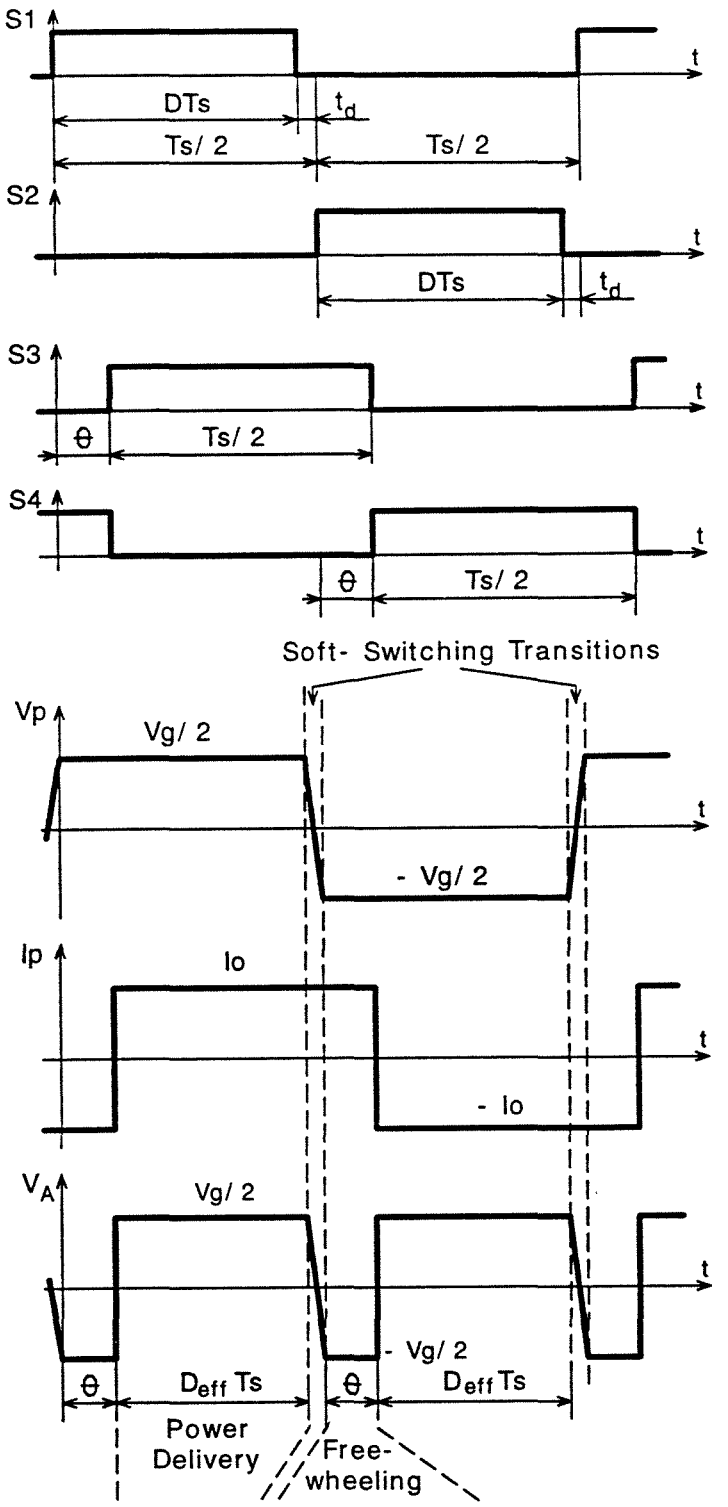


Figure 4.7: Idealized waveforms in the novel half-bridge converter explaining output voltage regulation.

same polarity. By neglecting transition interval, duty ratio is given by:

$$D = 2\frac{\tau - \theta}{T_s}. \tag{4.1}$$

The output voltage is average value of the voltage v_A at the input A and in continuous conduction mode of operation (CCM) is given by:

$$V_o = V_A(2D - 1) = V_g(D - .5). \tag{4.2}$$

Equation (4.2 suggests that duty ratio is limited to the values $.5 < D < 1$. As a consequence, the secondary voltage needs to be higher than in the conventional half-bridge converter.

4.5 Switch Realization

The primary side current bi-directional switches, $S1$ and $S2$, are realized, in practice, by the MOSFET transistors. The output capacitance of the MOSFET is usually not large enough so the external capacitance is added across each MOSFET in order to reduce dv/dt on the transistors.

Three possible practical realizations of the secondary side, voltage bi-directional switches $S3$ and $S4$ are shown in Fig. 4.8.

Realization of the voltage bi-directional switch with the bipolar transistor (BPT) and the diode D in series (Fig. 4.8 (a)) could be more advantageous than other two realizations only in the high voltage, low current applications. The base drive circuit could be simplified and low voltage drop of the saturated transistor will be an advantage.

By using MOSFET instead of bipolar transistor (Fig. 4.8 (b)) complexity of the base drive circuit is significantly reduced. In low voltage, high current applications the conduction losses could be significantly reduced when the low-resistance MOSFET (for instance 60V, 8mΩ device) is used.

The common, serious drawback for these two solutions is *reverse recovery* current of the series diode D.

Realization with the saturable inductor SR in series with the diode D, shown in Fig. 4.8 (c), solves the reverse recovery problem of the diode. This realization is chosen

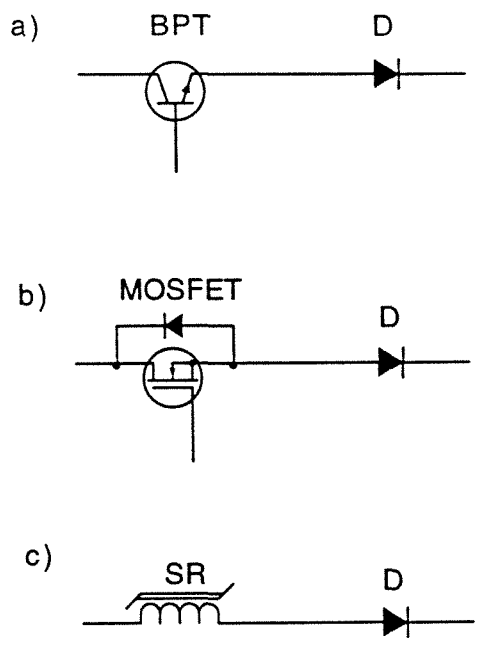


Figure 4.8: Three possible practical realizations of the voltage bi-directional switch: a) Bipolar transistor in series with diode, b) MOSFET in series with diode and c) Saturable inductor in series with diode.

due to several advantages such as: a) there is no reverse-recovery problem during the diode's turn-OFF, so the parasitic oscillations and voltage spikes in the diode voltage are significantly reduced, b) *EMI* noise generation is reduced and the overall converter efficiency is improved , c) control of the saturable reactor is very simple and requires neither synchronization with the primary side switches nor the complex control and drive circuits, and d) the conduction losses in the winding resistance of the saturable inductor can be kept reasonably low even at higher current levels.

It should be noticed that it is also possible to use MOSFET instead of the diode in series with the saturable inductor. In this case the MOSFET is turned on during the conduction interval of the diode in order to reduce the conduction losses.

4.6 Extended Range of Soft-Switching

The common limitation for all zero-voltage switching topologies is the minimum load current at which zero-voltage switching is lost. Different techniques have been proposed

for extending the range of zero-voltage switching but they require an additional resonant inductor [45], or even the active circuit [46].

The proposed converter can provide zero-voltage switching even at no-load condition simply by increasing the dead-time t_d in the drive signals of the primary side switches $S1$ and $S2$, and with the proper design of the magnetizing inductance . The magnetizing inductance, L_m is designed such that at light loads and no-load conditions there will be enough stored energy, $L_m I^2/2$, to displace the charge in the capacitances of the primary side switches during the increased dead-time. It is clear that the maximum dead-time is less than $T_s/2$.

Duration of the transition intervals is load dependent, as used to be in any zero-voltage switching converter. At nominal load, the transitions are usually short and voltages on the transistors $Q1$ and $Q2$ change linearly during the soft-transitions (Fig. 4.5). Soft-switching is also provided at light loads, when the converter is operating in DCM, but the voltage transitions are more resonant than linear.

In order to provide soft-switching, dead-time needs to be increased thus reducing effective duty ratio of the converter. Since, at light loads, converter operates in DCM, reduction in the effective duty ratio due to increase in dead-time will not affect output voltage regulation. Moreover, reset current and flux swing in the core of the saturable inductors are simultaneously reduced due to reduction of the effective duty ratio. As a consequence of that, power consumed by the control circuit and core losses in the saturable inductors are reduced. Therefore, total efficiency of the converter will be improved at light loads.

4.7 Reduction of Circulating Current

Circulating current in the primary circuit during the freewheeling period θ (Fig. 4.7) results in the higher conduction losses and should be minimized. By inserting the freewheeling diode DFW in series with the small non-controllable saturable inductor $SRFW$ (Fig. 4.9), it is possible to reduce the circulating current in the primary circuit as well as in the secondary windings (Fig. 4.10). The function of the saturable inductor $SRFW$ is twofold and is explained next.

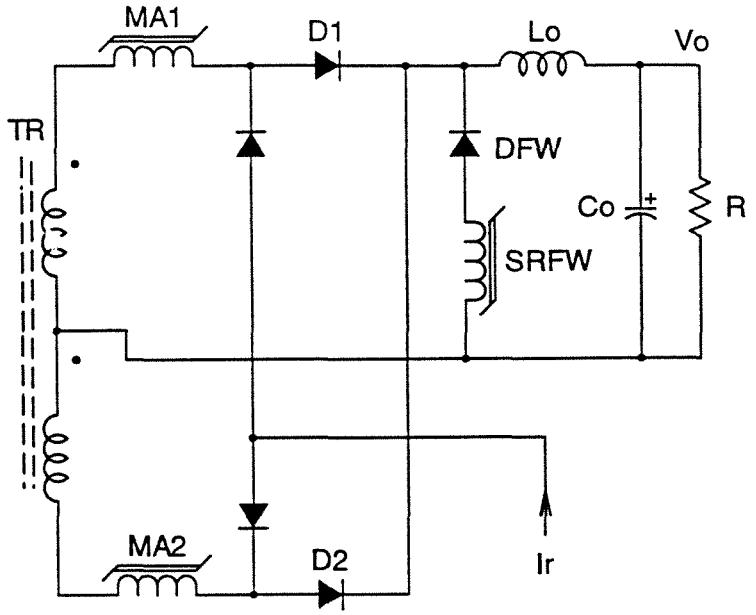


Figure 4.9: Circulating current is reduced during the freewheeling state by inserting the diode DFW in series with the non-controllable saturated inductor $SRFW$.

Conduction of the diode DFW is delayed by the blocking action of the saturable inductor $SRFW$. The saturable inductor is designed such that it runs into saturation after the soft-transition is finished as shown in Fig. 4.10. In this way, the load current is reflected to the primary until $SRFW$ saturates. The diode DFW takes, in an ideal case, the load current and thus providing zero circulating current during the freewheeling state, θ, after the transition has been finished. In this manner, the circulating current flows in the primary circuit only during the transition interval t_d.

The freewheeling diode has a lower current rating than the other two diodes, $D1$ and $D2$. As a consequence of the short transition intervals, the blocking capability of the saturable inductor is relatively small so the small saturable core can be used. This solution improves overall converter efficiency with small price paid for the additional diode and small saturable inductor.

It should be noticed that the freewheeling diode DFW, is not essential for the soft-switching operation of the converter but is rather added to improve overall converter efficiency.

Voltage at point A (Fig. 4.9) is clamped to zero by diode DFW during the freewheel-

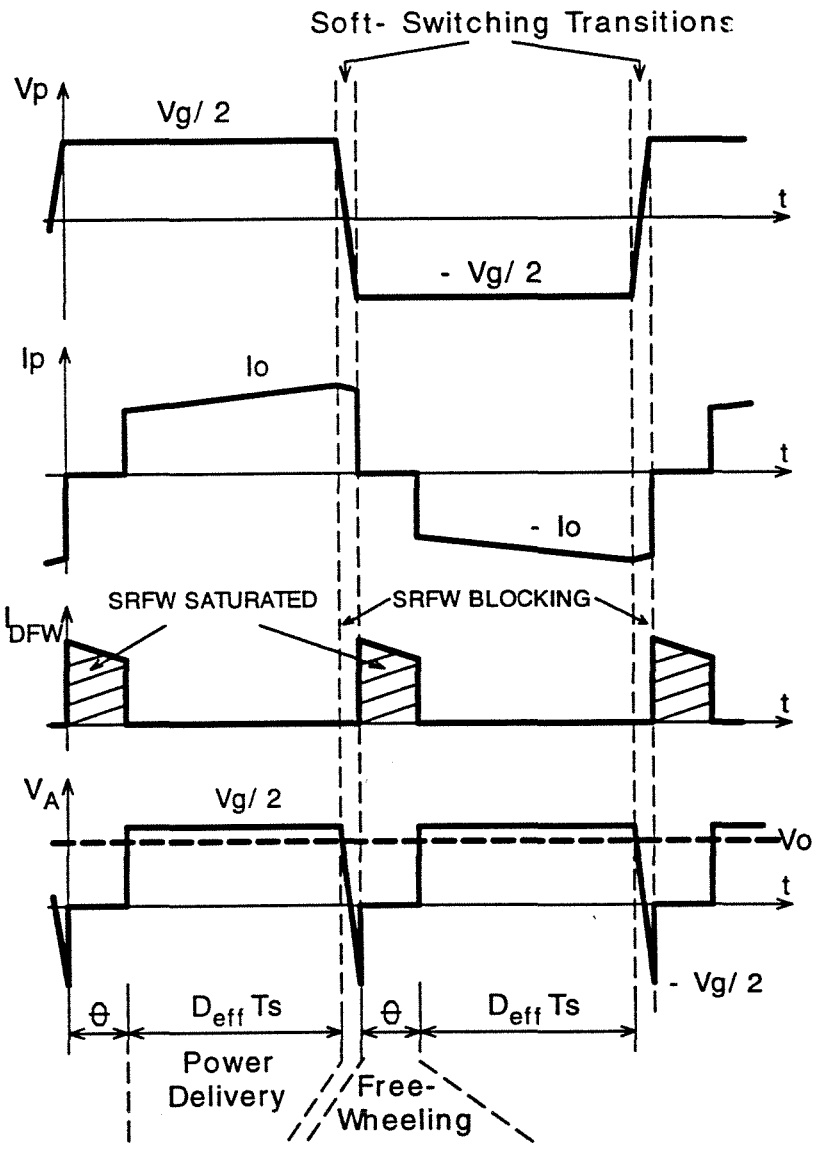


Figure 4.10: Diode DFW conducts load current during the freewheeling state θ thus, providing zero circulating current in the primary circuit.

ing state (Fig. 4.10), instead of at secondary voltage $-V_g/2$ (Fig. 4.7) before the diode was inserted. As a consequence of that, DC conversion ratio will be the same as in the conventional half-bridge converter. The output voltage is given now by:

$$V_o = V_A D = \frac{V_g}{2} D. \tag{4.3}$$

In Fig. 4.11 conversion ratio $M = V_o/V_g$ is plotted as a function of the duty ratio for the converter without the freewheeling diode (Eq. (4.2)) and with the diode (Eq. (4.3)). As one can see, conversion ratio is always larger with the freewheeling diode than without it. Consequently, for the same input voltage, the duty ratio is smaller and secondary voltage could be reduced when the freewheeling diode is added. In other words, for the same transformer's turns ratio converter with the freewheeling diode has wider dynamic range.

In practice, if the DC input voltage is already pre-regulated, for instance by the input current shaper, it is possible to minimize duration of the freewheeling state. The converter could still have high efficiency without the freewheeling diode particularly at full load. It should be expected that improvement in efficiency, due to reduced circulating current, will be more noticeable for power levels bellow 50% of the nominal power. This can be explained by the fact that the freewheeling state increases with decrease of the output power and, therefore, reduction of the circulating current becomes more efficient.

4.8 Experimental Results

In this section experimental results obtained on a 250W, 48V prototype are presented. The converter was operated at 200kHz from the 150VDC. Schematic of the is shown in Fig. 4.12. Circuit description is given in Section 4.8.1 and experimental waveforms are shown in Section 4.8.2.

4.8.1 Circuit Description

POWER STAGE

The primary side switches are realized with MOSFET transistors, $Q1$ and $Q2$, while the secondary side, voltage bi-directional switches, are realized with magamps $MA1$ and $MA2$ in series with rectifier diodes $D1$ and $D2$, respectively (Fig. 4.12).

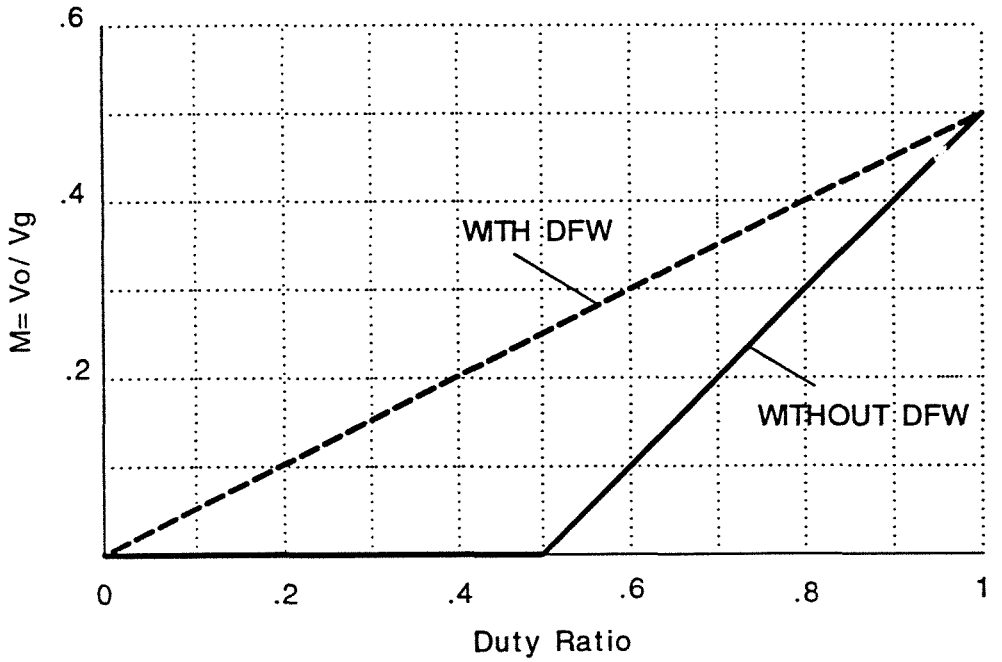


Figure 4.11: Conversion ratio $M = V_o/V_g$ as a function of the duty ratio for the half-bridge converter without and with the freewheeling diode.

The isolation transformer TR is designed with the magnetizing inductance small enough to provide zero-voltage switching at light loads, or even no-load condition as described in Section 4.6. There is no limitation for the leakage inductance as in the parent PWM converter, which together with small magnetizing inductance simplify the transformer design. The leakage inductance, of course, should be minimized particularly at higher switching frequencies (above 150kHz) because it reduces the effective duty ratio due to increased rise time of the switched current.

The output inductor is designed with usually 20-30% current ripple as in the conventional PWM converter.

Diode $D5$ and the non-controllable saturable inductor $SR3$, shown in dashed box in Fig. 4.12 are added for reduction of the circulating current in the primary circuit after the soft-transition is completed (described in Section 4.7).

CONTROL CIRCUIT

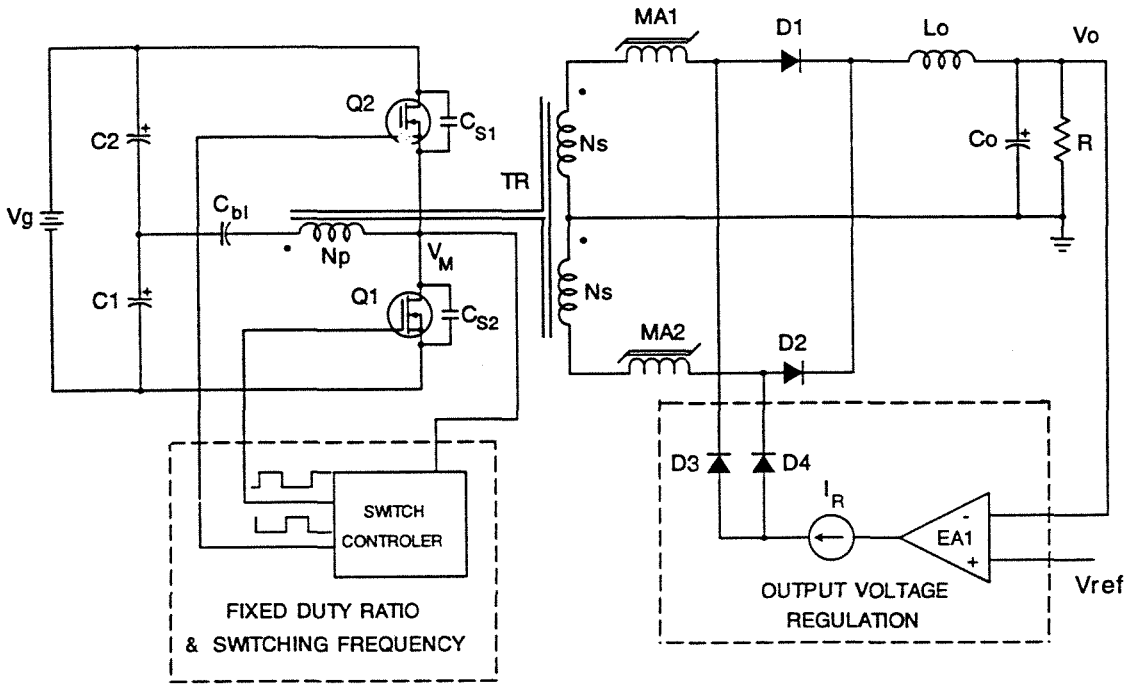


Figure 4.12: Schematic of the novel soft-switching half-bridge converter with the magamps. The primary switches Q1 and Q2 are complementary driven with fixed duty ratio close to 50% at constant switching frequency. The output voltage is PWM regulated with the magamps MA1 and MA2.

Control circuit on the primary side is realized with PWM chip with complementary outputs so the MOSFETs, $Q1$ and $Q2$ are driven at constant switching frequency and almost 50% duty ratio with the small dead-time. Voltages on the both transistors are sensed in order to delay turn on of the transistor if the soft-transition is not completed during the dead-time. In this way, the dead-time is increased at light loads, and soft-switching is provided for no-load to full load conditions.

Control circuit for the magamps is very simple and consists of an error amplifier and voltage controlled current source. Output voltage is compared with the reference V_{ref} in the error amplifier EA. Output of the EA controls the reset current for the magamps, and consequently their blocking capability. The very important advantage of the secondary side control is that there is no need for isolation of the voltage feedback

signal.

Components used in the prototype are listed bellow:

Transistors: $Q1$, $Q2$=IRF640

Diodes: $D1 - D2$=16CFP20; $D3 - D4$=1N914

$IC1$=UC3846;

Magnetic amplifiers: $MA1, MA2$ - 30T 8 x AWG30 wire on the core MB18X12X4.5 (Toshiba);

Saturable inductor: $SR3$ - 5 turns on the core SA 10X6X4.5 (Toshiba);

Capacitors: $C1, C2 = 470\mu F$, $C_{bl} = 2.2\mu F$; $C_o = 2X220\mu F$ $C_{S1}, C_{S2} = 680pF$.

Output inductor: $L = 42\mu H$

Isolation transformer: core - LP 32/13 (TDK); Turn ratio n=Np/Ns=2.

4.8.2 Experimental Waveforms

In this section experimental waveforms obtained in the prototype are shown to demonstrate the features of the proposed soft-switching half-bridge converter.

Transistor voltage and the primary current are shown in Fig. 4.13 for load current of $4A$. As can be seen the transistor's voltage is trapezoidal and free of the spikes and the parasitic oscillations. The primary current is reflected load current and delayed in respect to the voltage by approximately $500ns$. Both waveforms are in good agreement with idealized waveforms shown in Fig. 4.4.

In Fig. 4.14 the secondary voltage, the primary current and the voltage V_A waveforms, taken for load current of $4A$, are shown to verify the predicted waveforms from Fig. 4.7. As can be seen, during the freewheeling state the current waveform is delayed in respect to the voltage waveform, voltage $V_A = -75V$ and the inductor current linearly decays. During active state, the transformer's voltage and current are in phase, voltage $V_A = 75V$ and the inductor current linearly rises.

Waveforms in Fig. 4.15 confirm the proper operation of the magamps. For the simplicity only the voltage waveform of the magamp in one secondary is shown together with the secondary voltage and the current waveforms in both secondaries. The magamp blocks the secondary voltage during 500ns (bottom trace) and the diode in the

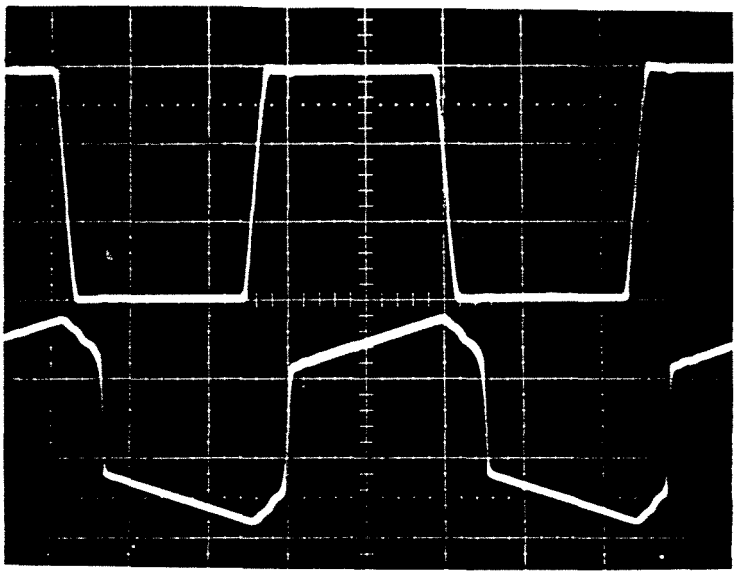


Figure 4.13: Drain-to-source voltage of the MOSFET (top trace: 50V/div.) and the primary current waveforms (bottom trace: 2A/div.) at load current 4A. Time scale: 1μs/div.

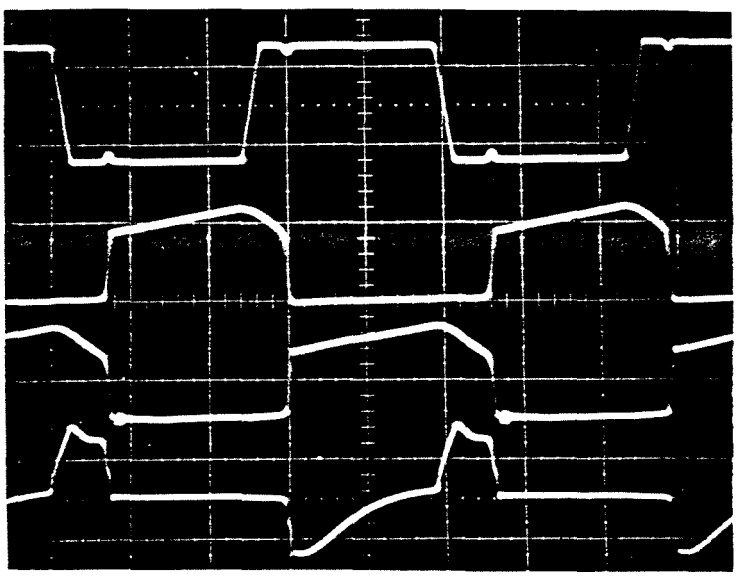


Figure 4.14: The secondary winding voltage (top trace: 100V/div.), the primary current (middle trace: 4A/div.) and voltage V_A (bottom trace: 100V/div.) waveforms at load current 4A. Time scale: 1μs/div..

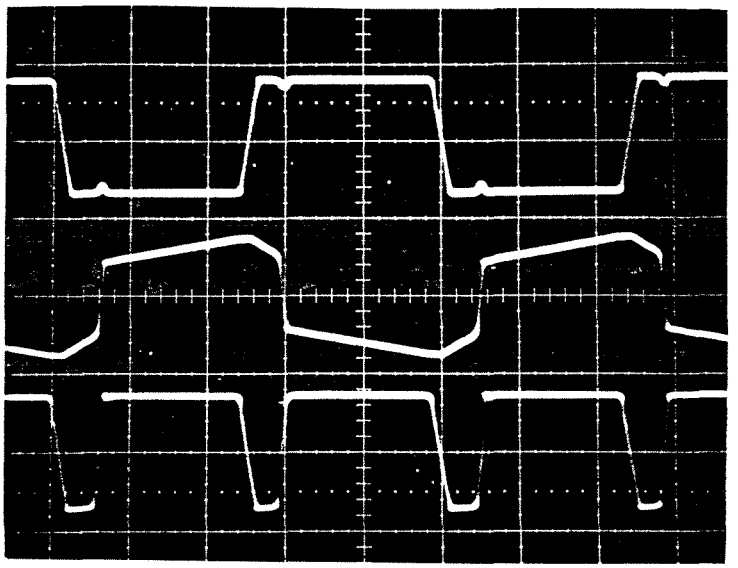


Figure 4.15: The secondary voltage V_{S1} (top trace: 100V/div.), the secondary current I_{S1} (trace 2: 4A/div.), current in the opposite secondary I_{S2} (trace 3: 4A/div.) and voltage on the magamp V_{MA1} (bottom trace: 100V/div.) waveforms at load current 4A. Time scale: 1μs/div..

opposite secondary is still conducting load current (trace 3). Once the magamp is saturated, its corresponding diode conducts the load current (trace 2) and the diode in the opposite secondary is turned off. The magamp is reset during the active state of the diode in the opposite secondary. Very clean, spike-free current waveforms in the both secondaries confirm soft-switching of the rectifier diodes by action of the magamps.

Salient waveforms in the converter at only 2% load current (.1A) are shown in Fig. 4.16. The secondary voltage waveform (top trace) confirms that soft-switching is still preserved. As one can seen from the current waveform in the common lead of the both secondaries (trace 3), the converter is operated in DCM. The asymmetry in the current pulses as well as in the voltage V_A waveforms (bottom trace) is due to different turn off characteristic of the rectifier diodes and the magamps. The primary current (trace 2) is dominated by the magnetizing current of the isolation transformer. The dead-time is increased to 1μs thus allowing the completion of the resonant transition between the magnetizing inductance and the MOSFETs capacitances before the MOSFET is turned on.

For comparison, the transistor's voltage and the primary current waveforms taken at

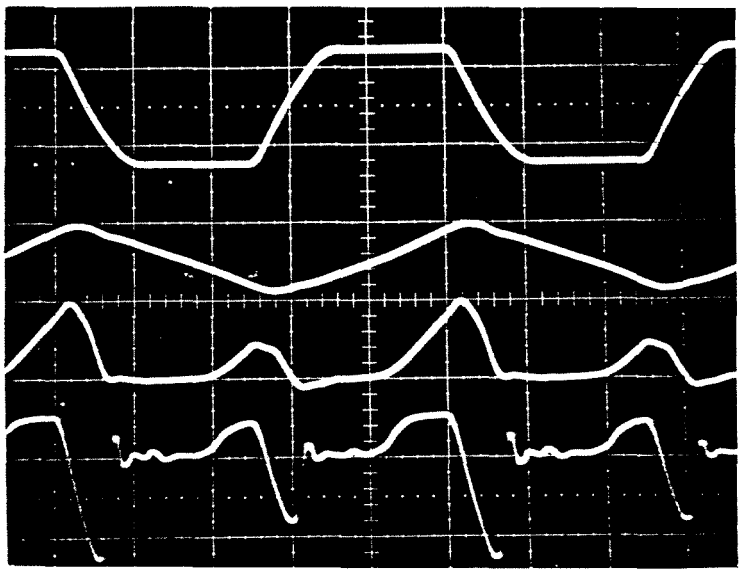


Figure 4.16: The secondary voltage (top trace: 100V/div.), the primary current (trace 2: 1A/div.), current in the common lead of the both secondaries (trace 3: .5A/div.) and voltage V_A (bottom trace: 100V/div.) waveforms at 2% load current (.1A). Time scale: 1μs/div..

2% load current and without adjustment of the dead-time are shown in Fig. 4.17. The resonant transition is longer than the dead time and hard switching occurred at approximately 70% of the transistor's nominal voltage. In addition, the parasitic oscillations are evident in both voltage and current waveforms.

In order to verify reduction of the circulating current salient waveforms are taken at nominal load (4A) before and after the freewheeling diode $D5$ and the saturable inductor $SR3$ are added and shown in Fig. 4.18 (a) and (b), respectively. Experimental waveforms are in good agreement with idealized waveforms in Fig. 4.10. The primary current (trace 2) , as well as the secondary current (trace), drop to zero after the soft-transition is completed (top trace) (Fig. 4.18 (b)), instead of circulating through the primary circuit (Fig. 4.18 (a)). Voltage V_A is clamped by the freewheeling diode at zero during the freewheeling state (Fig. 4.18 (b)) instead of at $-V_s$ (Fig. 4.18 (a)). It can be also seen that the duty ratio is also reduced when the freewheeling diode is added.

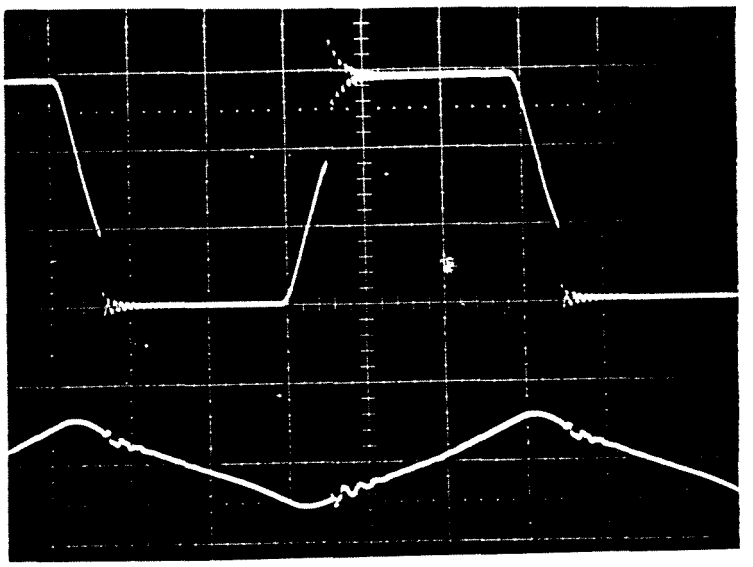


Figure 4.17: Transistor voltage (top trace: 50V/div.) and the primary current (bottom trace: 1A/div.) waveforms with fixed dead-time, t_d, at 2% load current (.1A). Time scale: 1μs/div..

4.8.3 Efficiency Measurement

Efficiency is measured on the prototype without and with the freewheeling diode operated at 172kHz and input voltage 150VDC. The output voltage is measured using a digital multimeter and both currents are measured with shunt resistors. Power stage efficiency is plotted as a function of the load current for both cases in Fig. 4.19 .

By adding the diode $D5$ and the saturable inductor $SR3$, the maximum increase in efficiency of 3% was measured at 50% load current.

Power consumption of both the primary and the secondary control circuits was fairly constant and was measured .98W, which is only .4% of the nominal power 250W.

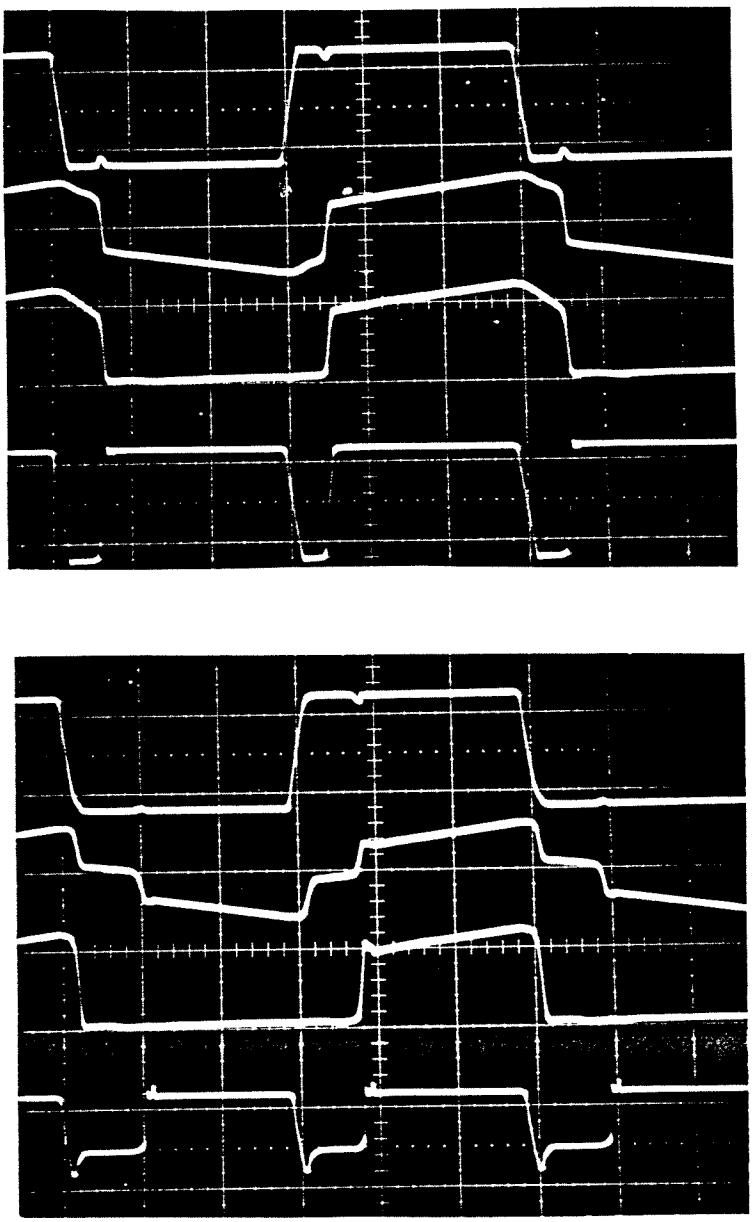


Figure 4.18: The secondary voltage V_{S1} (top trace: 100V/div.), the primary current (trace 2: 4A/div.), the secondary current I_{S1} (trace 3: 4A/div.) and voltage V_A (bottom trace: 100V/div.) waveforms at nominal load current 4A for the converter: a) without and b) with D5 and SR3. Time scale: 1μs/div..

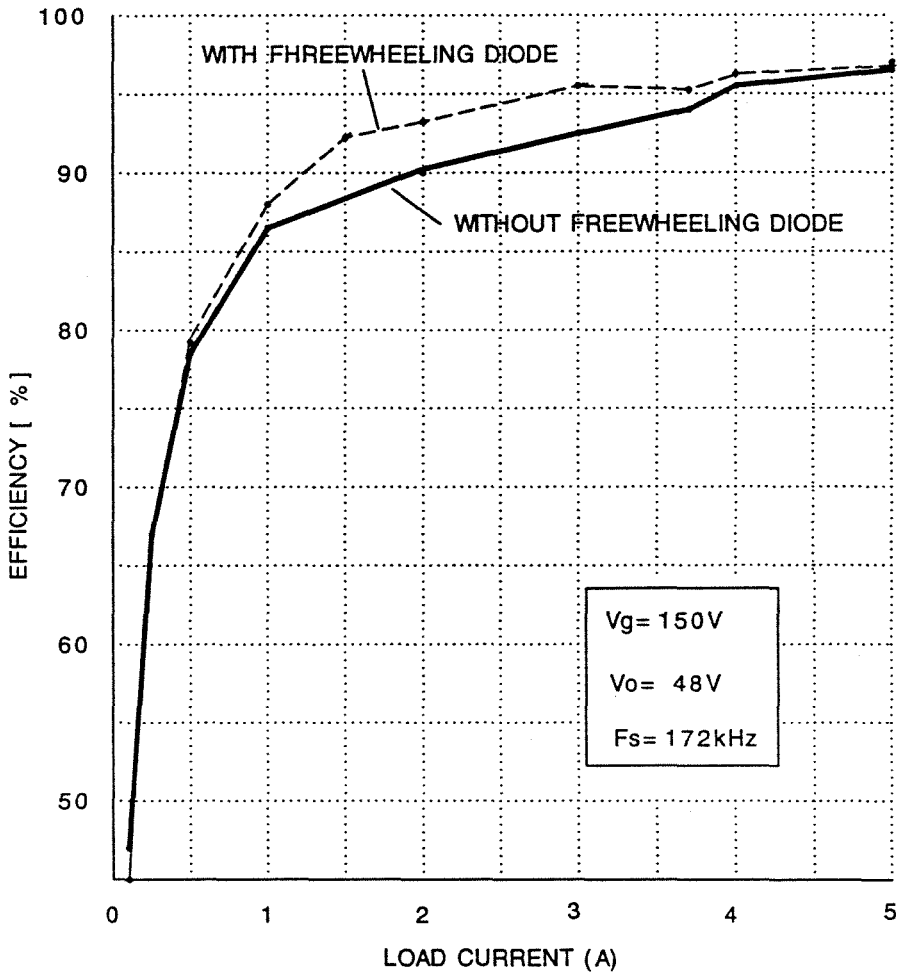


Figure 4.19: Power stage efficiency as a function of the load current.

Chapter 5

Extension of Novel Soft-Switching Mechanism to Other Symmetrical Topologies

The novel soft-switching mechanism, described in the previous chapter, can also be used in other symmetrical converter topologies, such as full-bridge and push-pull. The only difference between these three converter topologies is in their input power stages, while the secondary circuits as well as the primary side control circuits are the same.

The soft-switching full-bridge converter is described in Section 5.1 and compared with a widely used soft-switching phase-shifted, full-bridge converter. Section 5.2 reveals the soft-switching push-pull converter. Experimental waveforms are given in Section 5.3.

5.1 Soft-Switching Full-Bridge Converter with Magamps

5.1.1 Circuit Description

A novel soft-switching full-bridge converter with magamps is shown in Fig. 5.1. All four switches of the bridge, $Q1$ through $Q4$, are current bidirectional switches and preferably implemented with the $MOSFET$ devices in practice as shown in Fig. 5.1. Capacitances C_1 through C_4 represent the junction capacitances of the $MOSFET$s or externally added capacitances. The secondary side voltage bidirectional switches are realized with the magamps $MA1$ and $MA2$ in series with the rectifier diodes $D1$ and $D2$, respectively.

Switch controller on the primary side generates drive signals for $MOSFET$s $Q1$ through $Q4$ at constant switching frequency. The secondary side control circuit is identical to that described for the soft-switching half-bridge converter in Section 4.8. Zero-voltage switching of the primary side $MOSFET$s and soft turn-off of the rectifier diodes as well as the output voltage regulation are obtained by the same mechanism described

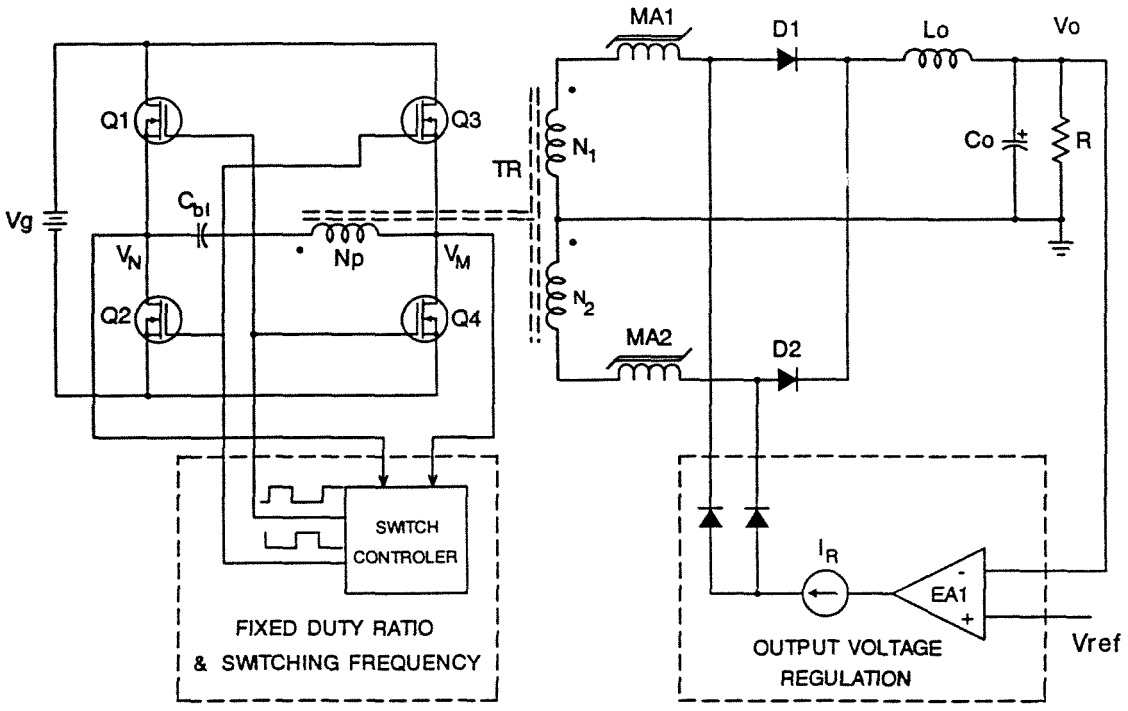


Figure 5.1: A novel soft-switching full-bridge converter.

in Chapter 4. The voltages at the midpoint of each leg of the bridge, V_N and V_M, are sensed and fed back into the switch controller. Thus, the dead time in the drive signals is adjusted such that zero-voltage switching is provided for all operating conditions.

Idealized waveforms during a switching period are shown in Fig. 5.2 . Two diagonal switches of the bridge $Q1$, $Q4$ and $Q2$, $Q3$ are driven simultaneously with a fixed, near 50% duty ratio and with small dead time t_d between the turning on of one pair and turning off of the other pair (Fig. 5.2). Thus, two switches on the same side of the rail *never* conduct simultaneously even during the soft-transitions.

The magamps on the secondary side operates at the fixed 50% duty cycle but out of phase. Turn on of the rectifier diodes is delayed in respect to the corresponding pairs of the primary side switches by the magamps ($D1$ and $Q1, Q4$, $D2$ and $Q2$, $Q3$). Thus, the primary current is delayed (or phase shifted) in respect to the voltage as shown in Fig. 5.2. Each magamp blocks for the time θ and regulates the output voltage by

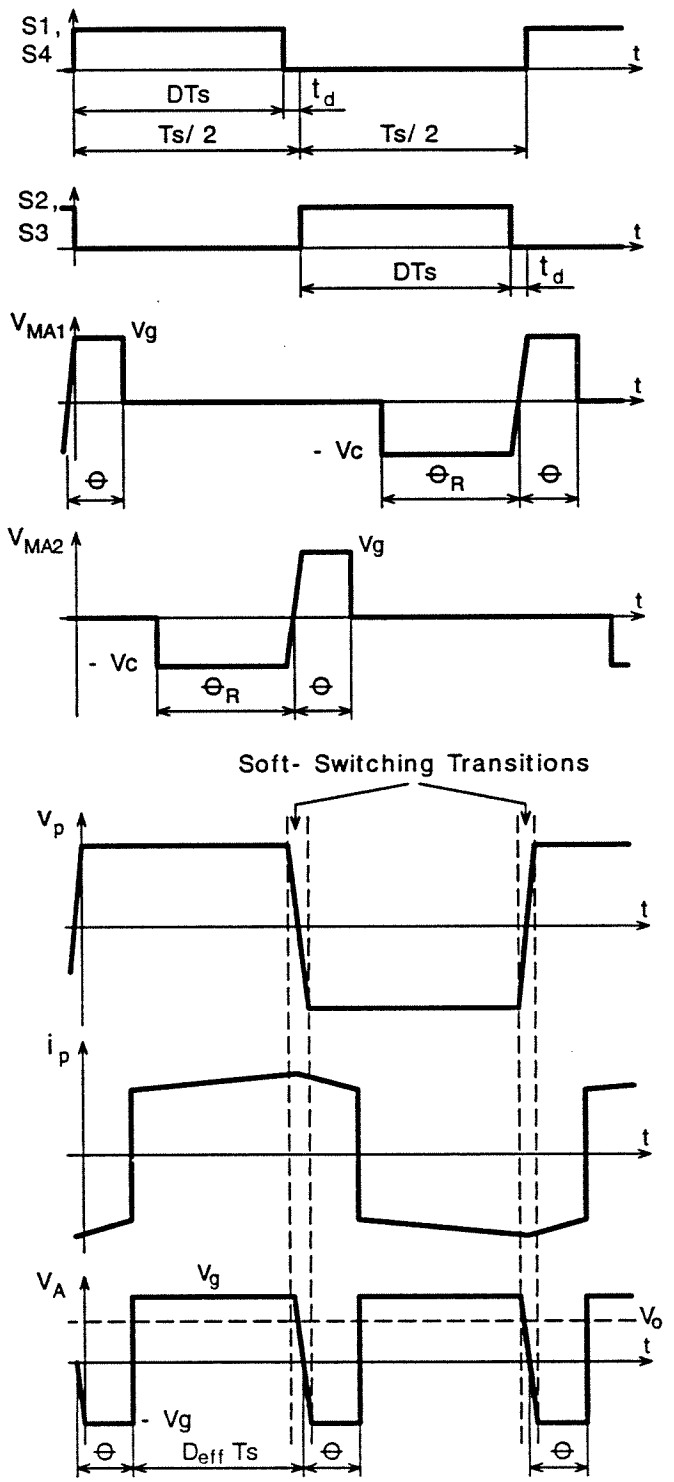


Figure 5.2: Idealized waveforms in a novel full-bridge converter during a switching period.

adjusting duration of the active state, $DT_s - \theta$.

The transformer is *never* shorted neither during the transitions t_d nor during the passive states θ. Therefore, the reflected DC load current is used for charge displacement in the transistors' junction capacitances. The soft-transition between the primary side switches is under the same scenario as described for the soft-switching half-bridge converter in Section 4.2.2.

5.1.2 Comparison Between a Novel Soft-Switching Full-Bridge and Soft-Switching Phase-Shifted Full-Bridge Converter

Described soft-switching full-bridge converter with magamps (SSFBMA) has completely different soft-switching mechanism compared to the soft-switching phase-shifted full-bridge converter (SSPSFB) described in Section 3.3.2 even though it may look the same. The purpose of this section is to clarify the main differences and advantages of the proposed SSFBMA.

The main difference between switching mechanisms in these two converters is the commutating current, i.e., source of energy used for charge displacement in the $MOSFET$s' capacitances. They are a consequence of the basic principle of the operation.

In the SSPSFB converter (Fig. 3.6), two legs of the bridge switches under different conditions due to different commutating currents leading to different duration of the transitions intervals (Fig.3.7). Only the transition from active to passive state is natural and provided by the reflected load current, while the transition from passive to active state, during which the transformer is shorted, requires an additional source of energy– leakage inductance. Thus, the large leakage inductance is *essential* for the soft-transition from passive to active state (Fig 3.8), and thus, strongly affects the overall performance of the converter.

In contrast to that, two legs of the bridge in the $SSFBMA$ converter switches only to terminate the power delivery thus, during the transition from active to passive state. Since this transition is *natural* and provided by the reflected load current to the primary, both legs of the bridge switches under the *same* conditions. Power delivery (switching from passive to active state) is initiated by the *secondary side switches* (for example

$MA1$ and $D1$ in Fig. 5.1) after two diagonal switches in the bridge ($Q1$ and $Q4$) have already been turned on.

It now becomes obvious that the soft-switching mechanism in the SSFBMA offers several advantages compared to the soft-switching mechanism in SSPSFB converter, such as:

1. Extended range of soft-switching is *naturally* provided for all operating conditions.
2. No need for large leakage inductance
3. Soft-switching of the rectifier diodes is inherently provided by the magamps.
4. Simple primary side control with fixed, near 50% duty ratio.
5. Output voltage regulation is provided on the secondary side.
6. No need for the feedback isolation.
7. Independent control of the multiple outputs.

Operation of the primary side switches at fixed duty ratio can at first seems as a big disadvantage of the novel soft-switching converters with magamps. It is true that the magamp regulators have to provide regulation against the source voltage variations in addition to load variations. On the other hand, in most of the applications the source voltage is utility. In order to improve the power quality and harmonic current pollution of the utility line, an additional pre-regulator with unity power factor (input current shaper) is added to interface dc load and utility line. Such a pre-regulator, as described in Chapter 10, in addition to a unity power factor, provides regulated dc voltage on its output. Therefore, requirement for input voltage rejection is eliminated from the dc to dc converter supplying load.

Another point which has to be made is that at light loads, the duty ratio of the primary side switches is automatically reduced by increasing the dead time required for zero-voltage switching. Thus, ac flux in the transformer is also reduced at light loads leading to high efficiency even for a wide range of the load current variations.

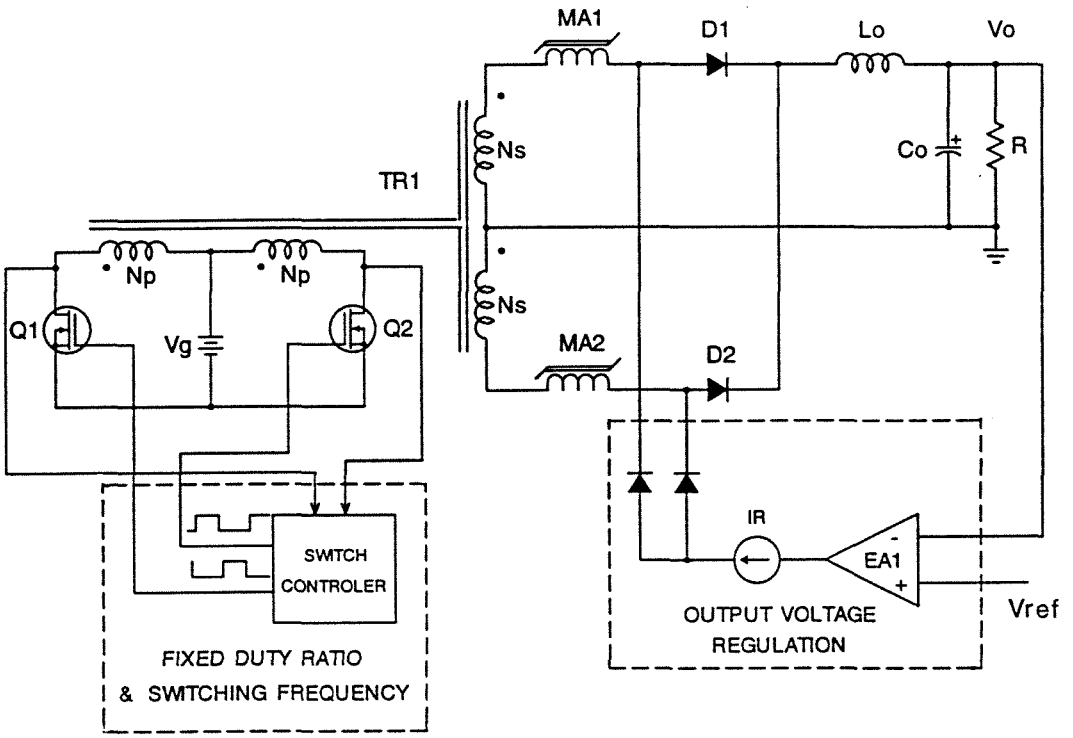


Figure 5.3: A novel soft-switching push-pull converter.

5.2 Soft-Switching Push-Pull Converter with Magamps

Soft-switching push-pull converter with magamps is shown in Fig. 5.3. The main topological difference between the push-pull converter and both half-bridge and full-bridge topologies is in the power transformer. The push-pull converter has center-tapped primary consisting of two windings with the same number of turns $N_{P1} = N_{P2} = N_P$ compared to a single primary winding in other two topologies. Due to this, it may not be so obvious that the proposed soft-switching mechanism can also be used in the push-pull converter. This is described next.

Two primary side switches are current bidirectional switches ($MOSFET$ devices), with their parallel capacitances C_1 and C_2. The secondary circuit is the same as in other two topologies.

Idealized waveforms during a switching period are shown in Fig. 5.4. Transistors $Q1$ and $Q2$ are driven at a fixed, near 50% duty cycle with the dead time t_d, but out of

phase. Two primary windings are wound such that their voltages are out of phase. Each of these two windings takes part in energy transfer during only one half of the switching period. Turn on of the rectifier diode is delayed by its magamp which introduces the phase-shift between the primary winding's current and voltage. Energy is transfer only during the time intervals when both voltage and current in the same primary winding are in phase.

During the first transition interval, initiated by turning off the previously conducting transistor, for example $Q1$, reflected load current I_o splits between two primary windings simultaneously charging C_1 and discharging C_2. At the moment when voltage on the $Q2$ drops to zero, its body diode becomes forward biased and clamps voltage at zero, and consequently voltage on the $Q1$ at $2V_g$. Transistor $Q2$ can now be turned on at zero voltage. Voltages on the primary windings change polarity so the voltage on the winding N_{P2} becomes positive. The reflected load current which is circulating through the $Q2$ and primary winding N_{P2} is negative as shown in Fig. 5.4. The current changes polarity when the magamp $MA2$ saturates and the rectifier diode $D2$ becomes forward biased which causes turn off of the diode $D1$. This initiates the power delivery (active state).

The second transition interval is initiated by turning off the transistor $Q2$. The reflected load current again splits between two primary windings and provides the soft-transition as shown in Fig. 5.4.

In the second half of the switching period the transistor $Q1$ is conducting. The current in the winding N_{P1} changes polarity when the magamp $MA1$ saturates (Fig. 5.4). The described process repeats each switching period.

The above analysis shows that both soft-transitions are the same and provided by reflected load current to the primary as in the half-bridge and the full-bridge converters.

5.3 Experimental Results

In this section experimental results obtained on a 300W, 48V prototype of the full-bridge converter are presented. The converter was operated at 200kHz switching frequency from the 300Vdc input . The schematic of the prototype is given in Fig. 5.1. Both the primary and secondary control circuits are identical to these used in the soft-

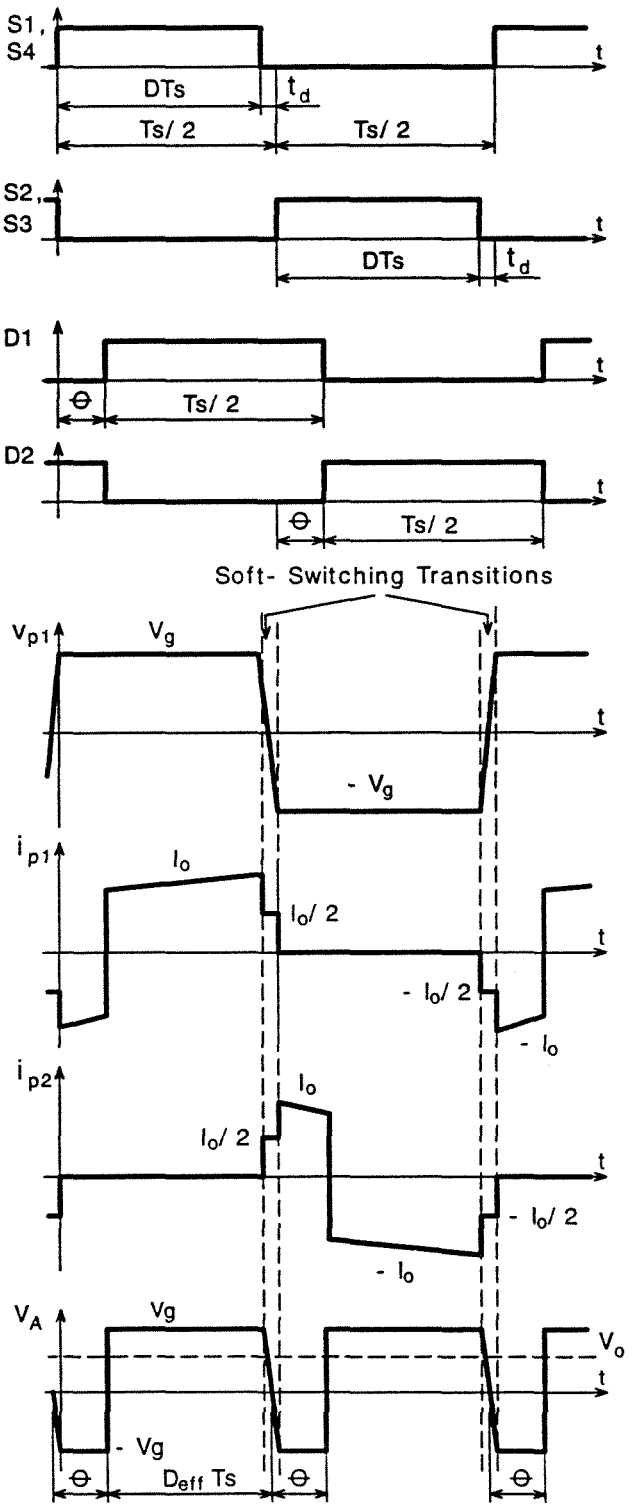


Figure 5.4: Idealized waveforms in a novel push-pull converter during a switching period.

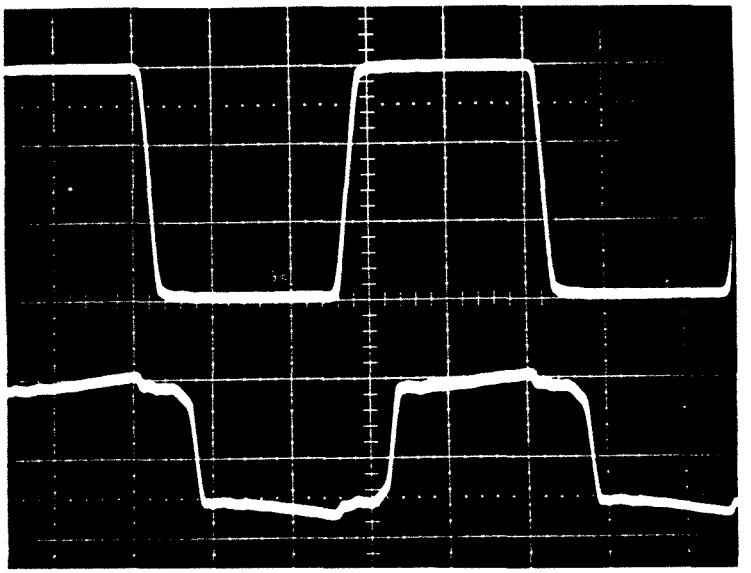


Figure 5.5: Drain-to source voltage of the MOSFET (top trace: 100V/div.) and the primary current waveforms (bottom trace: 2A/div.) at load current 6A. Time scale: 1μs/div.

switching half-bridge converter (Section 4.8.1). The components used in the prototype are listed below:

Transistors: $Q1$ - $Q4$=IRF640

Diodes: $D1 - D2$=16CFP20

$IC1$=UC3846;

Magnetic amplifiers: $MA1, MA2$ - 30T 8 X AWG30 wire on the core 50B45-1E (Magnetics)

Capacitors: $C_1 - C_4 = 470nF$, $C_{bl} = 2.2\mu F$; $C_o = 2X220\mu F$

Output inductor: $L = 42\mu H$

Isolation transformer: core - LP 32/13 (TDK) ; Turns ratio: n=Np/Ns=4.

Transistor voltage and the primary current of the isolation transformer are shown in Fig. 5.5 for load current of $6A$. As can be seen the transistor's voltage is trapezoidal and free of spike and the parasitic oscillations. The primary current is reflected load current and delayed in respect to the voltage by approximately $600ns$, thus providing soft-switching of the MOSFETs. Both waveforms are in good agreement with idealized waveforms in Fig. 5.2.

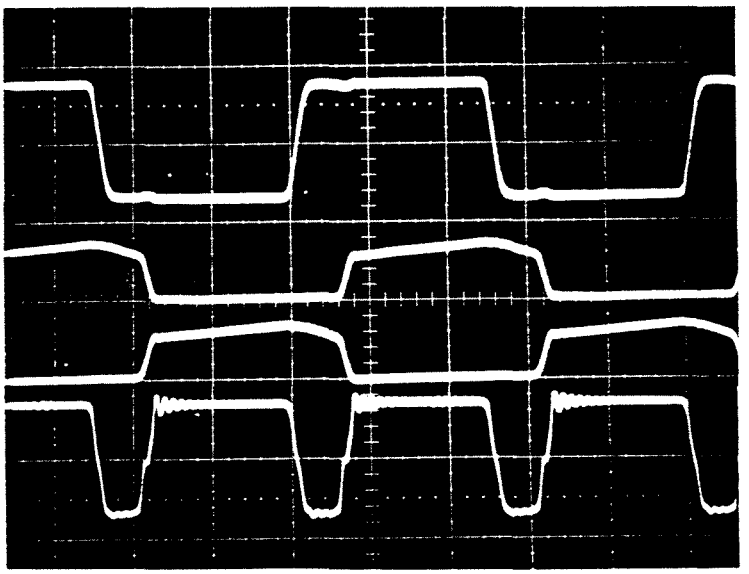


Figure 5.6: The secondary voltage V_{S1} (top trace: 100V/div.), current in the diode $D1$ (trace 2: 10A/div.), current in the diode $D2$ (trace 3: 10A/div.) and the voltage V_A (bottom trace: 100V/div.) waveforms at load current $6A$. Time scale: $1\mu s$/div..

In Fig. 5.6, the secondary voltage, the current in both rectifier diodes and the voltage V_A waveforms, taken for load current of $6A$, are shown to verify soft-switching of the rectifier diodes. As can be seen, the diodes' currents are very smooth and without either positive or negative spikes which confirms the soft turn-off of the diodes. Also the voltage V_A, is clean and without spike.

Chapter 6

Multiple-Output Extension

Many applications require a power system which can provide more than one tightly regulated output voltage. One solution, called distributed power systems, is to use a DC-to-DC converter for each output voltage. Converters are then connected to the common bus voltage and are usually placed at the same board with the load they supply. Such converters are called point of load (POL) converters. The advantages of this solution are: a) each output is independently regulated and protected, b) on shelf converters can be used for building such power system, and c) each converter can be optimized for its particular load. On the other hand, application of distributed power is limited due to their high cost and complexity.

Another approach, which offers less complexity and increases power density of the power supply, is to use a converter with a single power stage with multiple windings on the power transformer. In such a converter all outputs share the same inverter stage. Only one output, called the main output, can be fully regulated by pulse width modulation of the inverter stage, located on the primary side. Such a solution then requires feedback isolation, and additional post-regulators are required for independent regulation of the auxiliary outputs against load variation. While such converters provide a cost effective solution, their main drawback is that voltage regulation on the auxiliary outputs depends on loading of the main output.

One prior art method uses magamps as post-regulators due to some benefits as compared to other post-regulation techniques, such as [48]:

1. Lower parts count.

2. Ruggedness and reliably.

3. High efficiency.

4. Reduced EMI noise.

5. Lower current stress on the main inverter power switches.

In Section 1.1, adverse effects of magamp post regulators in symmetrical topologies are addressed. The multiple output extensions of the novel soft-switching converters, described in Chapter 4 and Chapter 5, are presented in Section 1.2 and their advantages over the conventional converters with magamp post regulators are discussed.

6.1 Adverse Effects of Magamp Post-Regulators in Symmetrical Topologies

A widely used topology which utilizes magamp post-regulators is a forward converter which requires only one magamp per output (Section 2.4). The magamp in a forward converter is reset during the flyback interval of the power transformer. Most of the magnetizing current remains in the primary during the flyback interval of the transformer, and only a small portion is diverted to the secondary for reset of the magamp. In practice, usually up to four magamps can be put in a typical forward converter with no adverse effect upon reset of the power transformer.

In symmetrical topologies (half-bridge, full-bridge and push-pull) unlike the forward converter, two magamps are required per output and the transformer's magnetizing current is not used for reset of the magamps. In a half-bridge converter, for an example, there is no flyback interval of the transformer, and each magamp is reset during alternate pulses. The magnetizing current shifts to the secondary where it causes a series of problems which make a conventional half-bridge magamp converter less versatile than the forward converter. As a consequence of that, almost all half-bridge and other symmetrical topologies with magamp post-regulators require a freewheeling diode, DF, as shown in Fig. 1.1.

Without the freewheeling diode DF, the currents in the main output's secondary windings, I_1 and I_2 (Fig. 1.1), can be severely unbalanced right after the main switch is turned off as explained in detail in [49]. This is a consequence of the simultaneous conduction of both rectifier diodes $D1$ and $D2$ in the main output's secondary, which

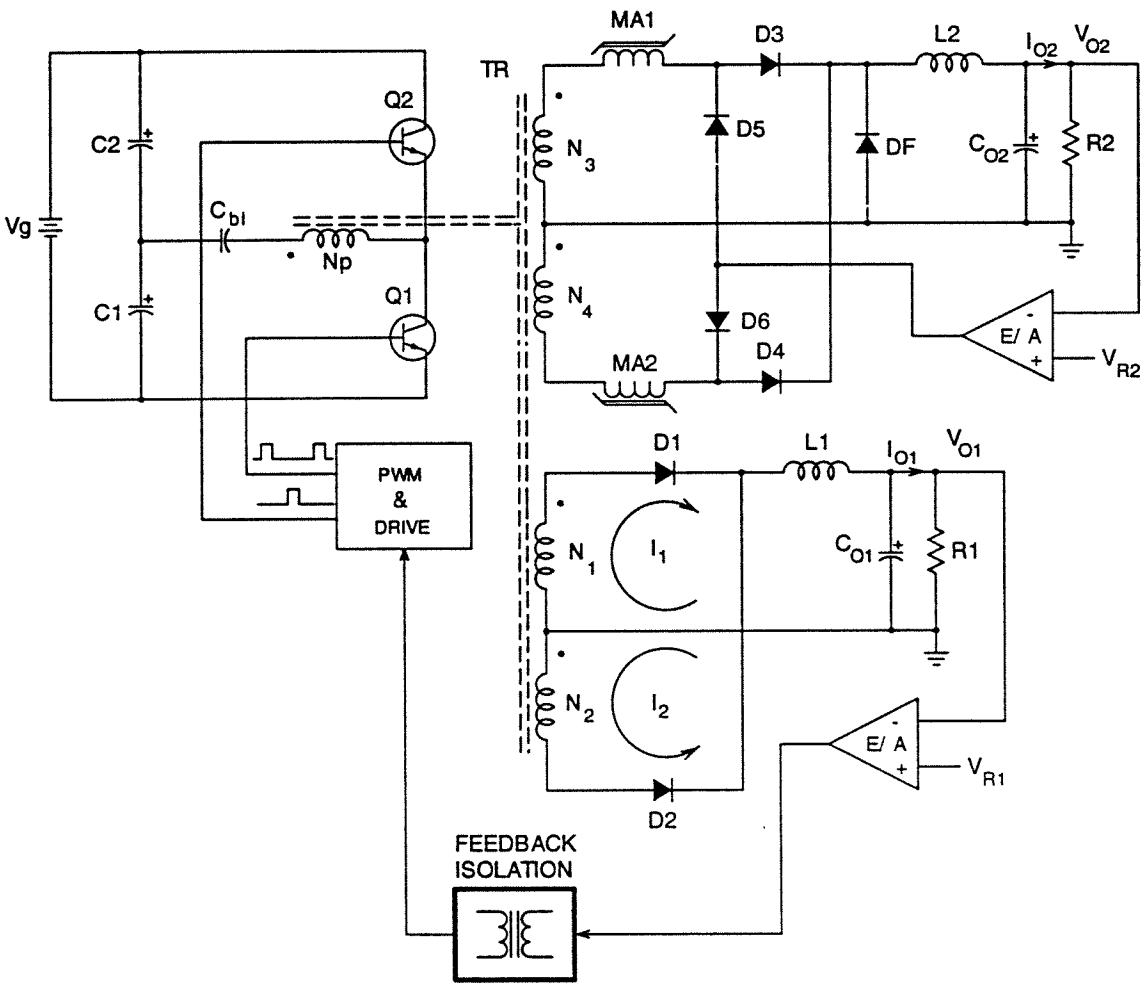


Figure 6.1: Two output conventional half bridge converter with magamp post regulators. The freewheeling diode, DF, is required *in the output with magamp post regulator.*

short the transformer during freewheeling interval. The situation is different when the main output is lightly loaded. The output inductor, L_2, actually supplies power to both the main output and its own load and to the primary of the converter. Therefore, in any practical design of the conventional half-bridge converter (or any other symmetrical topology), the freewheeling diode DF is *essential* for the proper mode of operation of the converter.

The freewheeling diode DF will keep only load current of the auxiliary output, I_{o2}, of the total imbalance from being shifted to the main output. The imbalance due to magnetizing current of the transformer still remains. In order to maintain continuous current in the main output inductor, $L1$, which is required for preventing the auxiliary output (V_{o2}) from sag, it is necessary to provide a path for the magnetizing current. This can be done by (a) increasing minimum load on the main output or (b) providing a shunt path for the excess current. Both approaches reduce converter efficiency and increase converter complexity particularly when the auxiliary output is used for supplying disk-drives and fans in computers.

Another undesirable effect is related to the energy stored in the magamp's saturated inductance which is dumped back into the transformer at the end of each pulse [50]. If this current, translated by the turns ratio, is greater than the main output's inductor current, the extra pulse will cause the main control loop to shrink the pulse width as shown in Fig. 6.2. As a consequence of that, the magamp's input pulse may be inadequate and output voltage will drop.

These adverse effects seem to be the more dominant factors in using the forward converter with magamp post regulators instead of the symmetrical topologies, particularly the half-bridge converter, for the medium power levels (a few hundreds of watts). It is shown in the next section that the novel soft switching converter topologies overcome the key disadvantages of the conventional, multiple-output symmetrical topologies with magamp regulators. In addition, soft-switching of the primary side switches is provided with the simplicity of the conventional PWM converters.

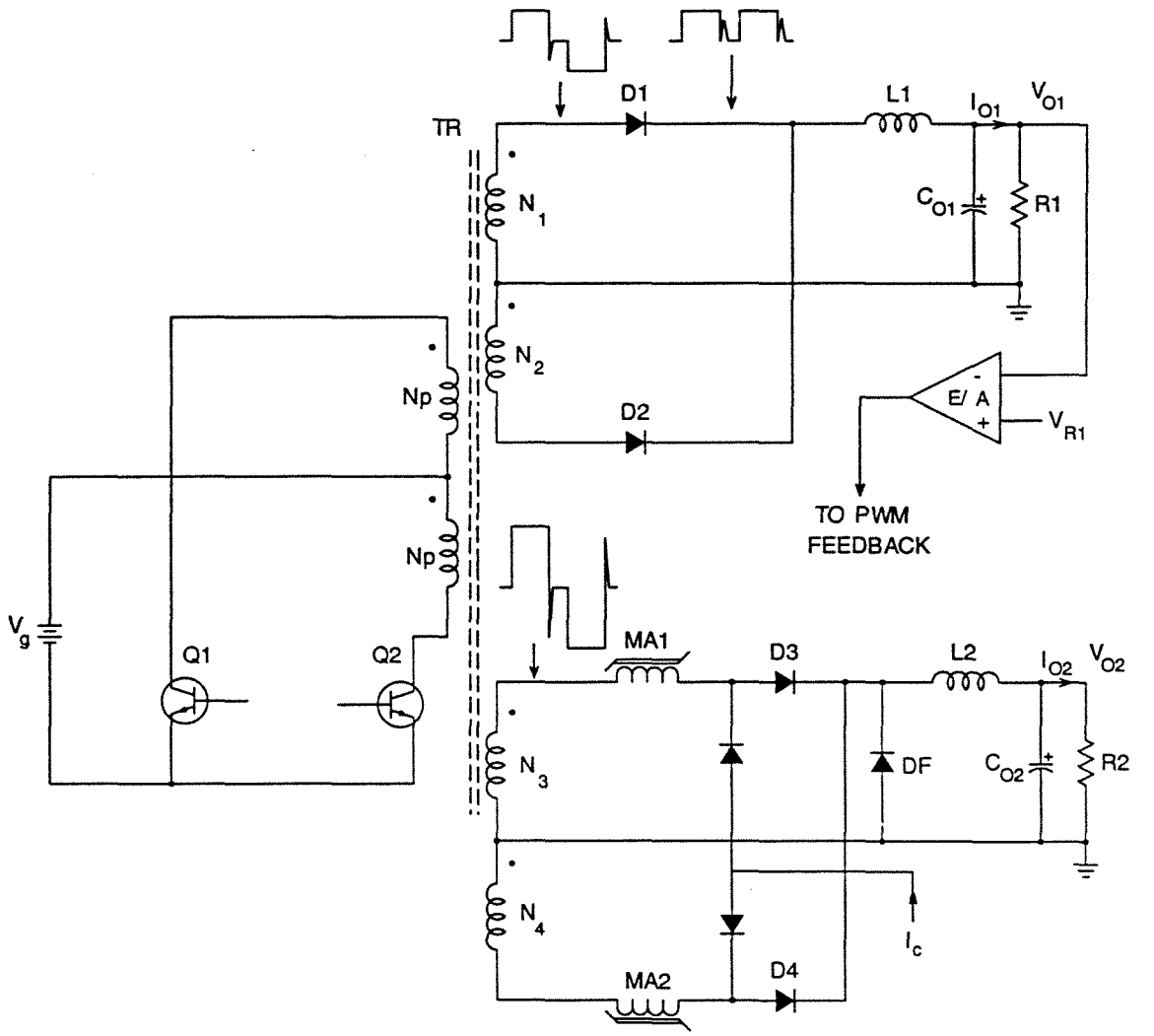


Figure 6.2: Energy stored in the magamp's saturated inductance is dumped back into the transformer at the end of each pulse, and can cause the main control loop to shrink pulse width erroneously.

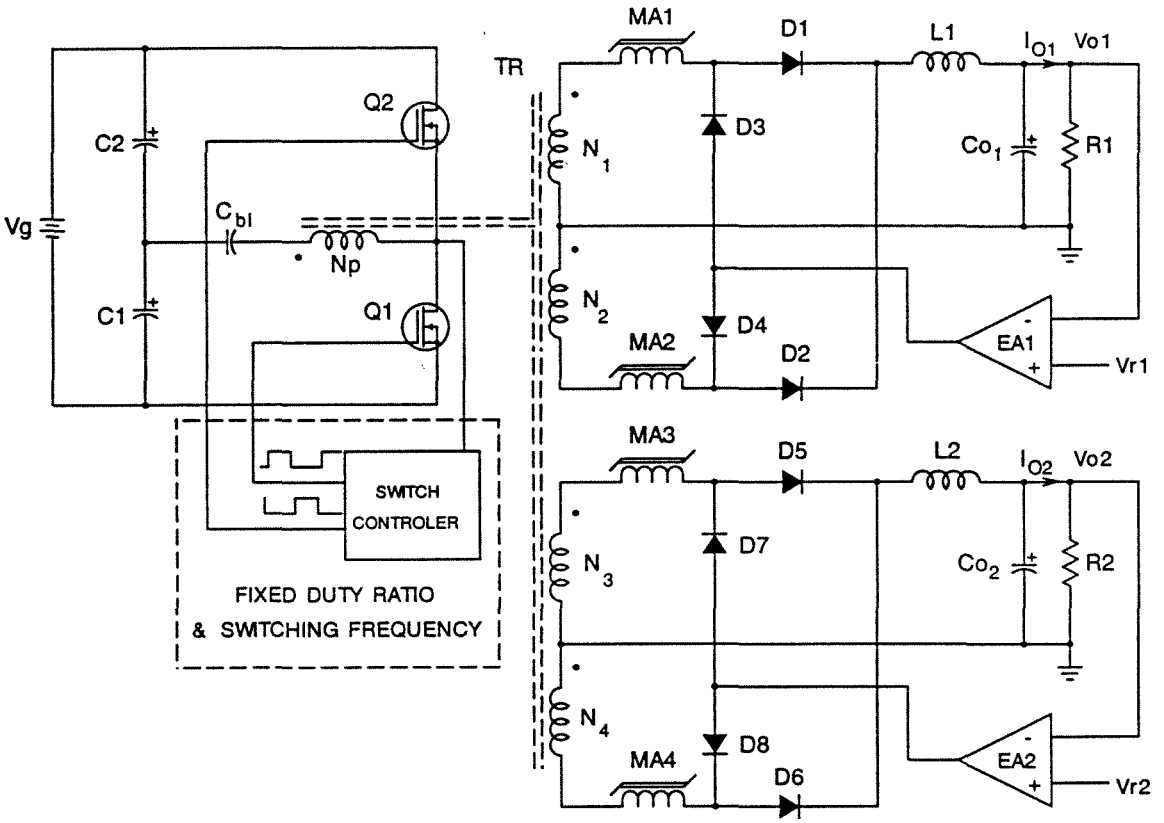


Figure 6.3: A novel soft-switching half-bridge converter with two independently controlled outputs with magamps.

6.2 Novel Multiple-Output Soft-Switching Converters with Magamp Regulators

All three novel soft-switching converter topologies, half-bridge converter (Chapter 4), full-bridge and push-pull (Chapter 5), are well suited for multiple-output extension. As an example, the novel soft switching half bridge converter with two outputs is shown in Fig. 6.3, but arbitrary number of the outputs can also be used.

The main differences between the novel soft-switching (Fig. 6.3) and the conventional half-bridge converter (Fig. 6.1) both with magamp regulators are:

1. The primary-side transistors, $Q1$ and $Q2$, are driven at fixed, near 50% duty cycle.

2. Each output is independently regulated by the full-wave magamp regulator without affecting the regulation of another output.

3. Soft-switching is provided for both primary side transistors and all rectifier diodes.

4. There is no need for feedback isolation.

5. There is no need for freewheeling diode in any of two outputs.

6. There is no limitation on the number of the regulated outputs.

By operating the primary side switches at fixed and near 50% duty cycle the simplicity of the primary control circuit is preserved as in the single output converter (Chapter 4). The problems inherent to the conventional multiple-output converters with magamp post-regulators, such as minimum load on the main output, undesirable voltage spikes on the main output due to energy stored in the magamp saturated inductances, and difficulty with using the current mode programming in the half-bridge converter [48, 49], are all eliminated since the power transformer, TR, is never shorted. Due to this, the magnetizing current of the transformer does not take part in resetting magamps, and consequently, does not limit the number of the regulated outputs as in the forward converter.

Chapter 7

Conclusion

A novel half-bridge Dc-to-Dc converter with magamps is presented which exhibits soft-switching in all switches and secondary side PWM output voltage regulation at constant switching frequency. Both soft-switching and the output voltage regulation are obtained by using voltage bi-directional switches on the secondary side realized with magamps in series with the rectifier diodes.

The proposed converter uses soft-switching mechanism different from the one used in the buck converter which provides soft-switching from no-load to full load even with small output inductor ripple current and features symmetrical transition intervals.

The Primary side switches, realized by MOSFET transistors, are alternatively driven at constant frequency and 50% duty ratio with small dead-time, while the secondary side switches are alternately driven at exactly 50% duty ratio with the variable delay with respect to the primary switches.

Zero-voltage switching in the MOSFET transistors is naturally provided by the reflected DC load current to the primary side which maintains the primary current in the same direction as before the MOSFET was turned-OFF. Zero-current switching of the rectifier diodes is provided by the action of the magamps due to their non-linear, square loop magnetic characteristic. The output voltage regulation is achieved by varying the blocking interval of the magamps using control circuit on the secondary side, which eliminated the need for isolation of the feedback signal and resulted in a simple non-isolated control circuit.

The proposed novel soft-switching mechanism with magamps, has been also successfully used in the full-bridge and the push-pull topologies.

By operating primary side switches at fixed and near 50% duty cycle, the simplicity of the primary control circuit is preserved as in the single output converter. The problems

inherent to the conventional multiple-output converters with magamp post-regulators, such as minimum load on the main output, undesirable voltage spikes on the main outputs due to energy stored in the magamp saturated inductances, and difficulty with using the current mode programing in the half-bridge converter are all eliminated since the power transformer, TR, is never shorted. Due to this, the magnetizing current of the transformer does not take part in resetting the magamps, and consequently, does not limit the number of the regulated outputs as in the forward converter.

The proposed novel soft-switching converters with magamps eliminate the key disadvantages of the conventional soft-switching converter topologies while keeping the simplicity of original pulse width-modulated (PWM) converters.

Part II

Automatic Input Current Shaping

Chapter 8

Introduction

Recent international regulations governing the power quality and harmonic current pollution of the utility placed an increased emphasis on the problem of interfacing electronic DC loads to the utility line via power circuits. This power circuit is called an AC-to-DC converter. The conventional technique of doing this is to use the bridge rectifier with capacitor-input filter followed by a post-regulator (DC-to-DC converter) [63].

The bridge rectifier converts AC voltage to DC voltage while the capacitor forces the DC voltage to have small ripple. The post-regulator provides a regulated DC voltage to the load. The main problem associated with a capacitor-input filter is the narrow-pulse, high peak current which produces high harmonic components in the line current [51]. These large harmonic currents are undesirable because they produce distortion of the line voltage, and both conducted and radiated noise.

Only the components of input current which are of the same frequency and in phase with input voltage deliver active power to the load. For ideal, sine-wave line voltage higher order harmonic currents do not contribute to the power delivery, but only generate the increased rms current in the transmission lines and therefore, produce additional losses. When the line current is made proportional to the line voltage, the maximum active power is delivered, and ideal, unity power factor is achieved. The increasing number of electronic loads connected to the line and their sensitivity to the quality of the line voltage, require from the designer and user of a utility to consider the quality of the input current as well as of the output voltage.

The following two issues are closely related but not identical: achieving unity power factor or minimization of harmonic current content. In the special case of ideal sine-wave line voltage these two objectives are identical. However, the line voltage contamination with harmonic currents is the more severe problem which is now also regulated by inter-

national regulations such as IEC 555-2 which is coming in effect in December 1994.

Close regulation of the output voltage is essential when AC-to-DC converter is to supply sensitive loads. In applications where a multiple output converter is required or in distributed power supply systems, a good solution is to have front-end input current shaper with a single isolated output (DC bus voltage), and then have one or more downstream post regulators (DC-to-DC converters) to provide close regulation on each output. This approach has several advantages: isolation and safety requirements are done only once in the current shaper, the regulation of DC bus voltage does not have to be very tight nor have fast response.

The use of active methods for input current shaping based on switching DC-to-DC converters is the best way to get high input power factor. There are numerous papers describing application of DC-to-DC converter in current shaping applications. One of the most often utilized is the boost converter [51]-[55], but also the flyback [56, 58] and the Sepic [60] converters are proposed for current shaping, although other topologies can be used [51]. Usually all above converters operate in continuous conduction mode (CCM) and widely used control circuits are based on programming input current to be proportional to the line voltage by closing input current feedback loop.

Using DC-to-DC converters in discontinuous inductor current mode of operation (DICM) in current shaping applications is very attractive for low power levels because very simple control circuits can be used [56]. When a converter operates at constant switching frequency and constant duty cycle, current shaping is obtained automatically. On the other hand, the high switching current ripple is present with magnitude at least twice the average value of the input current for variable switching frequency or even higher if the switching frequency is kept constant. High switching frequency and additional filtering are required to reduce harmonic distortion and therefore to get high input power factor. Neither of these approaches are optimal, since they reduce overall efficiency of the current shaper and increase size, weight, and number of magnetic components.

Automatic input current shaper based on the integrated magnetics Ćuk converter [59], is described in Chapter 11. This converter when operated in DICM provides unity power factor automatically like the flyback and the Sepic converters, and a voltage follower ap-

proach with simple control circuit can be used. It is shown that essentially zero switching input current ripple can be obtained without increasing switching frequency, inductance or using additional filter when coupled-inductors or integrated magnetic extension of the converter is used. This unique feature *inherent* to the Ćuk converter enables that size of magnetics can be kept small even at very modest switching frequency of 40kHz and high input power factor can be achieved without any additional filtering. Experimental results which confirm predicted behavior and performance are given at the end of the chapter.

The main drawback of the input current shapers with external energy storage is slow output regulation. An additional down-stream converter is usually added in order to provide fast output regulation. The power is processed twice, and complexity of such utility-to-DC, harmonic-free interface is increased. While this approach is widely used for the power levels above few hundred watts, it is not clear whether or not this approach is also a cost-effective solution for the low power levels.

In Chapter 12, a new single stage AC-to-DC converter is proposed which combines the functions of automatic current shaping, fast output regulation, and lossless soft-switching. This was made possible through internal energy storage and discovery of the new modes of operation, which together, effectively decoupled the input boost-like part of the Ćuk converter from its buck-like output. In order to keep the voltage stress on the switches low, the variable frequency control is required in addition to PWM control. Experimental results obtained on 50W, 12V prototype which confirm the fast output regulation (30kHz bandwidth for 100kHz switching frequency) simultaneously with the low-harmonic line current waveforms are given at the end of the chapter.

Another novel class of single stage AC-to-DC converters with unity power factor and fast output regulation is proposed in Chapter 13. These converters use a magamp for the input current shaping, while the active switch is used for fast output regulation. By using core material for the magamp with high saturated permeability, and operating the input stage of the converter in DICM, the linear input inductance can be replaced by the saturated inductance of the magamp. Thus, the magamp combines the functions of a controllable switch and a linear inductor into a single device. The proposed method of

current shaping with magamp is extended to the full-bridge topologies with their input, boost-like stage operated in continuous conduction mode. Experimental results obtained on different prototypes confirm advantages of the proposed topologies.

Conclusions are summarized in Chapter 14.

Chapter 9

Input Current Shaping

This chapter briefly describes the input current problem in a single phase AC-to-DC conversion system. Section 9.1 explains why the input current shaping is needed, while in Section 9.2, the most common measure of the quality of input current waveform, *power factor*, is defined. Functions and limitations of the current shaper are outlined in Sections 9.3-9.5.

9.1 The Need for Input Current Shaping

Recent international regulations governing the power quality and harmonic current pollution of the utility placed an increased emphasis on the problem of interfacing electronic DC loads to the utility line via power circuits. Such a power circuit is called an AC-to-DC converter and the conventional technique of doing this is to use the bridge rectifier with a capacitor-input filter followed by a post-regulator (DC-to-DC converter) as shown in Fig. 9.1.

The bridge rectifier converts AC voltage to DC while the capacitor forces the DC voltage to have a small ripple. The post-regulator provides a regulated DC voltage to the load. The main problem associated with a capacitor-input filter are narrow-pulse, high peak currents which produce high harmonic currents on the utility line, as shown in Fig. 9.2.

These large harmonic currents are the source of noise and interference to other electronic loads on the same utility line. Low power factor in the 0.5 - 0.7 range limits the maximum power available to the user.

Therefore, input current shaping is required for two reasons: efficiency and noise. Only those harmonic components of the input current that match those of the line

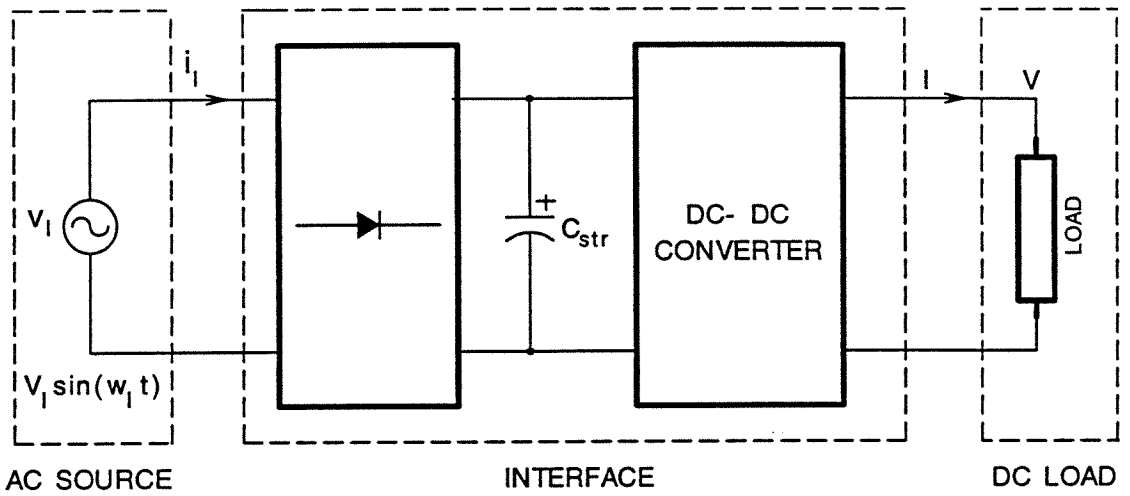


Figure 9.1: Conventional AC-to-DC power conversion scheme.

voltage waveform deliver power from source to the load, but all current components contribute to the rms value of the current, and hence to the lost power. For a maximum power delivery, every current component must be related to its corresponding voltage component by a common real scalar, i.e.:

$$i_l = K v_l. \tag{9.1}$$

Both radiated and conducted noise is generated whenever the input current and the voltage do not have the same waveform. In AC-to-DC converters, noise currents are those of frequencies other than the line frequency: reflected load current; AC current caused by switching action; harmonics of the line frequency and sidebands generated by the switching and line frequency.

9.2 Power Factor

Power factor is probably the most common parameter describing the way a load utilizes the utility line. It is defined as the ratio of real (average, true or active) power, P, to total apparent power (volt-amperes VA), i.e.,

$$Power factor\ (PF) = \frac{P}{VI} \tag{9.2}$$

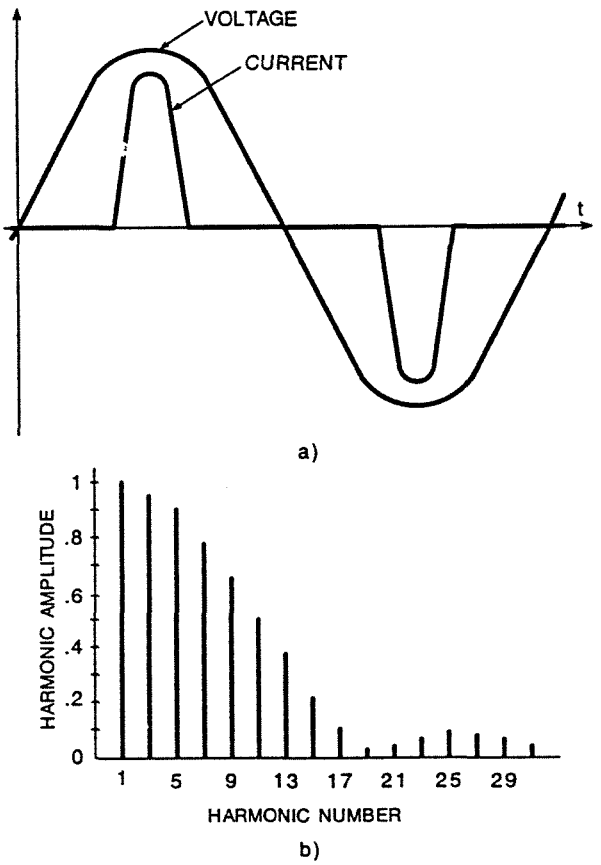


Figure 9.2: a)Line voltage and current waveforms and b) line current harmonics content, for the capacitive input filter.

where, V and I are rms values of the input voltage and current, respectively. For the sinusoidal input voltage, power factor can be expressed as:

$$PF = \frac{I_f}{I_t} cos\phi \tag{9.3}$$

where, I_f is the rms value of the fundamental of the input current, I_t is the rms value of the total input current, and ϕ is the angle between the fundamental component of the current and the voltage.

From Eq. (9.3) one can see that when the input current contains only the fundamental component in phase with input voltage, such as for resistive load, for example, the power factor is the highest and equal to one. Hence, the design objective is to make the

input current proportional to the input voltages. The important point is that drawing a proportional current from the power line is beneficial not only to the load, which achieves unity power factor, but also to the power line. Therefore, to provide high quality of the input current waveform, the device perforate for that task must act as a resistor emulator.

For ideal (sine-wave) line voltage, higher order harmonic currents do not contribute to load power but only generate the increased rms currents in the transmission lines and therefore, produce additional losses. When line current is made proportional to the line voltage, maximum active power is delivered and unity power factor is achieved. The increasing number of electronic loads connected to the line and their sensitivity to the quality of the line voltage require from the designer and user of a utility to consider the quality of the input current as well as of the output voltage.

The following two issues are closely related but not identical: achieving unity power factor and minimization of harmonic current content. In the special case of ideal sine-wave line voltage these two objectives are identical. However, the line voltage contamination with harmonic currents is the more severe problem which is now also regulated by international regulations such as IEC 555-2 [67], which is coming into effect in December 1994.

9.3 Functions and Limitations of the Input Current Shaper

The process of improving the input current waveform of an AC-to-DC converter, with the goal of alleviating problems of noise, line voltage distortion, and poor utilization voltage (in other words, improving the power factor) is called input current shaping, and the device which can perform it is called the input current shaper.

The functions required from the input current shaper are:

1. To shape the input current waveform.

2. To "balance" the difference between input and output power.

3. Output voltage regulation.

4. Isolation between line and load.

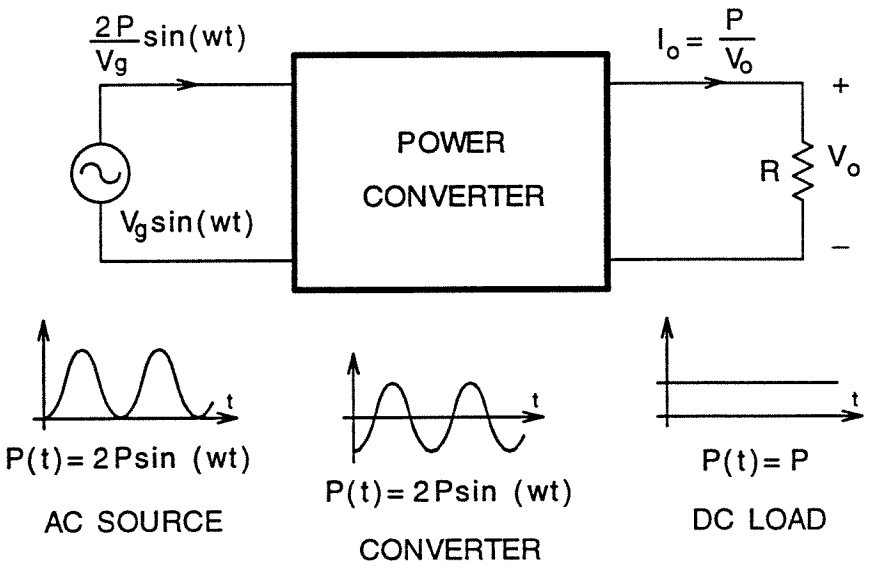


Figure 9.3: AC-to-DC power converter and corresponding power waveforms.

There are passive and active methods of input current shaping. We limit our consideration to active methods because of the advantages in power level range over passive methods of up to several kilowatts. These advantages include: smaller size and weight, achieving PF close to one, input-output isolation and output voltage regulation. The latter allows us to optimize design of the downstream DC-to-DC converter.

It is important to note that input current shapers do not follow the "rule" that by increasing the switching frequency, the problems of weight and response speed will also be solved. An AC-to-DC power converter with input current shaping is shown in Fig. 9.3 together with corresponding power waveforms for sinusoidal in-phase current. The difference between the constant load power and the time varying input power sets two fundamental restrictions on current shapers: *stored energy* and *speed response.*

9.4 Minimum Stored Energy

Absorbing the difference between the varying input power and constant load power requires a minimum amount of energy being stored in the power processor. Minimum

stored energy is limited by the line frequency and the load power level regardless of internal switching frequency. From Fig. 9.3 one can find that the change in the stored energy is given by the expression:

$$U(t) = -P \int cos(2\omega_l t)dt = -P\frac{sin(2\omega_l t}{2\omega_l} + U_0. \tag{9.4}$$

The peak stored energy is found from the constraint that $U(t) > 0$, is given by:

$$U_{peak} \geq \frac{P}{\omega_l} \tag{9.5}$$

and does not depend on switching frequency. As the line frequency is constant, the minimum stored energy is proportional to the load power.

9.5 Output Voltage Regulation

Close regulation of the output voltage is essential when the AC-to-DC converter is to supply sensitive loads. In applications where a multi-output converter is required, a good solution is to have a front-end input current shaper (AC-to-DC converter) with a single isolated output (DC bus voltage) and then have down-stream post-regulators (DC-to-DC converters) to provide close regulation on each DC output. This approach has several advantages, of which the two main ones are: isolation and safety requirements are done only once in the current shaper, and the regulation of DC bus voltage does not have to be very tight nor have a fast response.

In the current shapers with a single control, it is still possible to perform both current shaping and voltage regulation. There is a trade- off between the requirements for good current shaping and close regulation. The main reason for the trade off is the requirement for the minimum stored energy in a current shaping power converter. To obtain good regulation, the voltage loop should be fast to compensate for the changes in output load and input voltage. However, the input current shaping requires the power transferred to the output capacitor to be $P(t) = -cos(2\omega t)$. This implies that the voltage loop must be much slower than the line frequency in order not to interfere with the operation of the current shaping. Therefore, the control of the input current waveform is a high-frequency function, and the regulation of the output voltage is a low-frequency function.

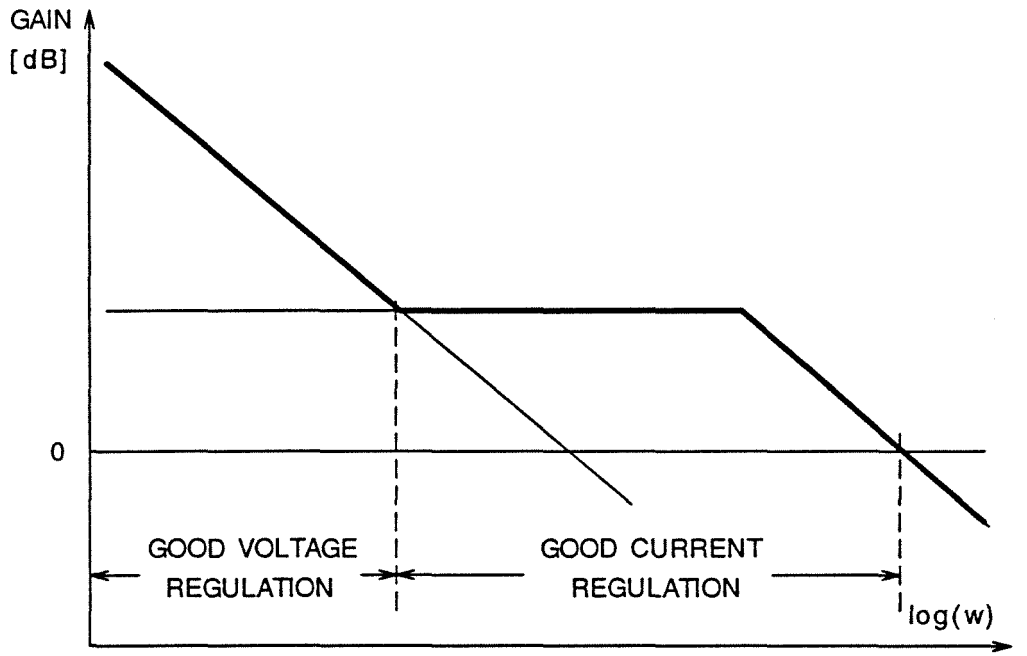


Figure 9.4: Typical loop gain magnitudes for a current shaper with both output voltage and input-current feedback.

The typical loop-gain magnitude for a current shaper with both output-voltage and input-current feedback is shown in Fig. 9.4.

Chapter 10

DC-to-DC Converters in Current Shaping Applications

By using DC-to-DC converters for active input current shaping, it is possible to get unity power factor on the line. Different topologies can be used but all of them share the same fundamental principles inherent to a single-phase AC-to-DC conversion. According to the position of the energy storage element in the converter, active current shapers can be classified as:

a) Current shapers with external energy storage.

b) Current shapers with internal energy storage.

Another classification, according to the control technique used for input current shaping, distinguishes the following:

a) Current shapers with input current feedback.

b) Automatic current shapers.

The purpose of this chapter is to give a general review of the different approaches for active input current shaping. Section 10.1 describes specific operating conditions of DC-to-DC converter when used in a current shaping application. Both external and internal energy storage methods are discussed. The basic principle of operation of the shaper with input current feedback is given in Section 10.3. Another approach which does not require input current feedback and provides current shaping automatically, is examined in Section 10.4. Two main non-idealities which contribute to distortion of the input current waveform, the "lag" effect and switching ripple, are discussed in Section 10.5. The start-up inrush current problem is analyzed for different topologies and simulation results are presented in Section 10.6

10.1 Environment of a Current Shaping Converter

When a DC-to-DC converter is used as an input current shaper it operates under specific conditions. Therefore, it is important to understand the main differences between the operation of a converter in a current shaping environment and that in a DC-to-DC application in order to be able to use the same analysis tools or even results from analysis of basic DC- to-DC converters.

In a DC-to-DC application, the steady-state implies that all currents and voltages in the converter have constant average DC values over each switching period, regardless of the mode of operation. This fact implies that all inductances are volt-second balanced and all capacitances are ampere-second balanced over each switching period. The terms volt-second and ampere-second balance, if not specified otherwise, will refer to the switching period from here on.

In a current shaping application, the operating point of the converter varies throughout the line period due to input-output power imbalance. The switching frequency of the converter, ω_s, is usually well above the line frequency, ω_l. Thus, the line voltage, $V_l sin(\omega_l t)$, can be considered as constant during the switching period with magnitude as a function of the position of the switching period in the line period. With such an assumption of a quasi- static operation, the same procedure as for a DC-to-DC operation can now be used for analysis in a current shaping environment with the input voltage $V_l|sin(\omega_l t)|$. The only difference is that all quantities are now expressed as a function of the position of the switching period in the line period. This means that the converter is in a steady-state of operation during half of the line period.

Due to the difference between time varying input power and constant DC output power, some energy storing element for input-output power balance is required. The behavior of the converter as well as determination of the trajectory of its operating point depends on how and where the low frequency energy is stored. Both capacitive and inductive energy storage methods can be used. Since the capacitive storage is more efficient in terms of the energy density than the inductive storage, only the former will be considered in the remainder of this thesis. According to the location of the energy storage element (capacitor) relative to the converter, one can distinguish between:

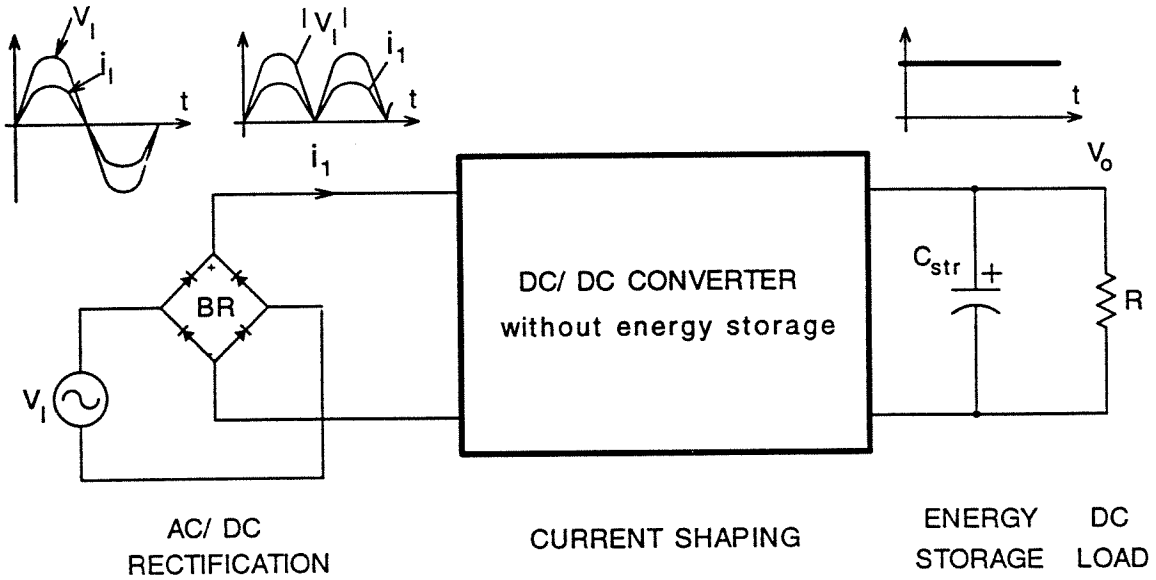


Figure 10.1: Current shaper with external capacitive energy storage. Energy storage capacitance, C_{str}, supplies constant dc voltage to the load R.

a) *External energy storage*, where the energy storage element is not part of the converter but is an external component connected directly to the DC load.

b) *Internal energy storage*, where the energy storage element is part of the converter connected to the DC load by the controllable switch.

Both methods are briefly described in the next two sections.

10.1.1 Current Shapers with External Energy Storage

Figure 10.1 shows the situation found in shapers with external energy storage. The energy storage takes places outside of the converter and energy storage element, the capacitor C_{str}, is connected in parallel with the DC load. The current shaper is considered as a combination of an external circuit (AC-to-DC rectifier, energy storage capacitance C_{str}, and DC load) and internal circuit (DC-to-DC converter without energy storage).

With the capacitor C_{str} removed, the DC-to-DC converter stores insignificant amount of energy, meaning that its reactances are high frequency components designed according to the switching frequency, not to the line frequency. The DC-to-DC converter, being a

resistor emulator, draws input current averaged over the switching period proportional to the rectified line voltage and delivers averaged current, $\bar{i}_2$, to the energy storage capacitor C_{str}.

It is useful to define the *apparent* (or operating point) conversion ratio of the DC-to-DC converter as [52]:

$$M' \equiv \frac{v_o}{v_l} = \frac{V_o}{V_l|sin(\omega_l t)|}. \tag{10.1}$$

The conversion ratio of the entire shaper is defined as:

$$M \equiv \frac{V_o}{V_l}. \tag{10.2}$$

Since the output voltage is constant, the conversion ratio of the shaper, M, is a fixed, DC quantity. By substituting Eq. (10.2) into Eq. (10.1), the expression for the apparent conversion ratio is:

$$M' = \frac{M}{|sin(\omega_l t)|}. \tag{10.3}$$

From Eq. (10.3) it follows that a DC-to-DC converter has a variable DC voltage conversion ratio which constantly varies from a finite value, M (at the peak of the rectified line voltage), to infinity (at zero crossing of the line voltage) throughout half of the line period (π). Since the converter stores insignificant energy, the current conversion ratio, $\bar{i}_1/\bar{i}_2$, is also equal to M'.

The *apparent load* of the DC-to-DC converter is designated R', and is defined as:

$$R' \equiv \frac{\bar{v}_o}{\bar{i}_2} = \frac{V_o}{\bar{i}_2}. \tag{10.4}$$

Both the apparent conversion ratio M', and the apparent load R', are instantaneous values of the position of the switching period in the line period. The meaning of these two quantities, M' and R', is that the operating point (the state variables and control inputs) of the converter operating in a current shaper with instantaneous apparent load, R', and apparent conversion ratio, M', is the same as when the converter operates as a DC-to-DC converter with steady-state DC load R' and conversion ratio M'. Once the variations of M' and R' are determined in a current shaping application, one can determine the range of control inputs from the dependence of M' on load and control when the converter is performing DC-to-DC conversion.

The apparent load, R', is calculated from the power balance between the time varying input power and power delivered to the energy storage capacitor, C_{str}, since the DC-to-DC converter stores insignificant energy. The input power is given by:

$$P_{in}(\omega_l t) = 2Psin^2(\omega_l t) \tag{10.5}$$

where, P is the output DC power of the load. The output current of the converter, which is charging current of the C_{str}, varies as:

$$\bar{i}_2(\omega_l t) = \frac{P_{in}(\omega_l t)}{V_o} = 2I_o sin^2(\omega_l t) \tag{10.6}$$

and the apparent resistance is

$$R'(\omega_l t) = \frac{R}{2sin^2(\omega_l t)}. \tag{10.7}$$

The apparent resistance of a converter constantly varies between infinity (at zero crossing of the line voltage), and one half the DC load resistance (at peak of the line voltage).

The main drawback of the current shapers with external energy storage (Fig. 10.1) is slow output voltage/current regulation as a consequence of the size of the energy storage capacitor across the load and a single control which cannot provide simultaneous input current shaping and fast output regulation. An additional down-stream converter is usually added to provide fast output regulation as shown in Fig. 10.2 (a). The power is processed twice, and the complexity of such utility to DC, harmonic-free interface is increased. While this approach is widely used for power levels above a few hundred watts, it is not clear whether or not this approach is also a cost-effective solution for the low power levels.

10.2 Current Shapers with Internal Energy Storage

When the low frequency energy is stored internally, then the energy storage capacitor, C_{str}, becomes part of the DC-to-DC converter as shown in Fig. 10.2 (b). In such a shaper, the energy storage capacitor is connected to the load by the controllable switch inside the converter [53]. Three main reasons why the internal low-frequency energy storage is a desirable feature of such a network are as follows:

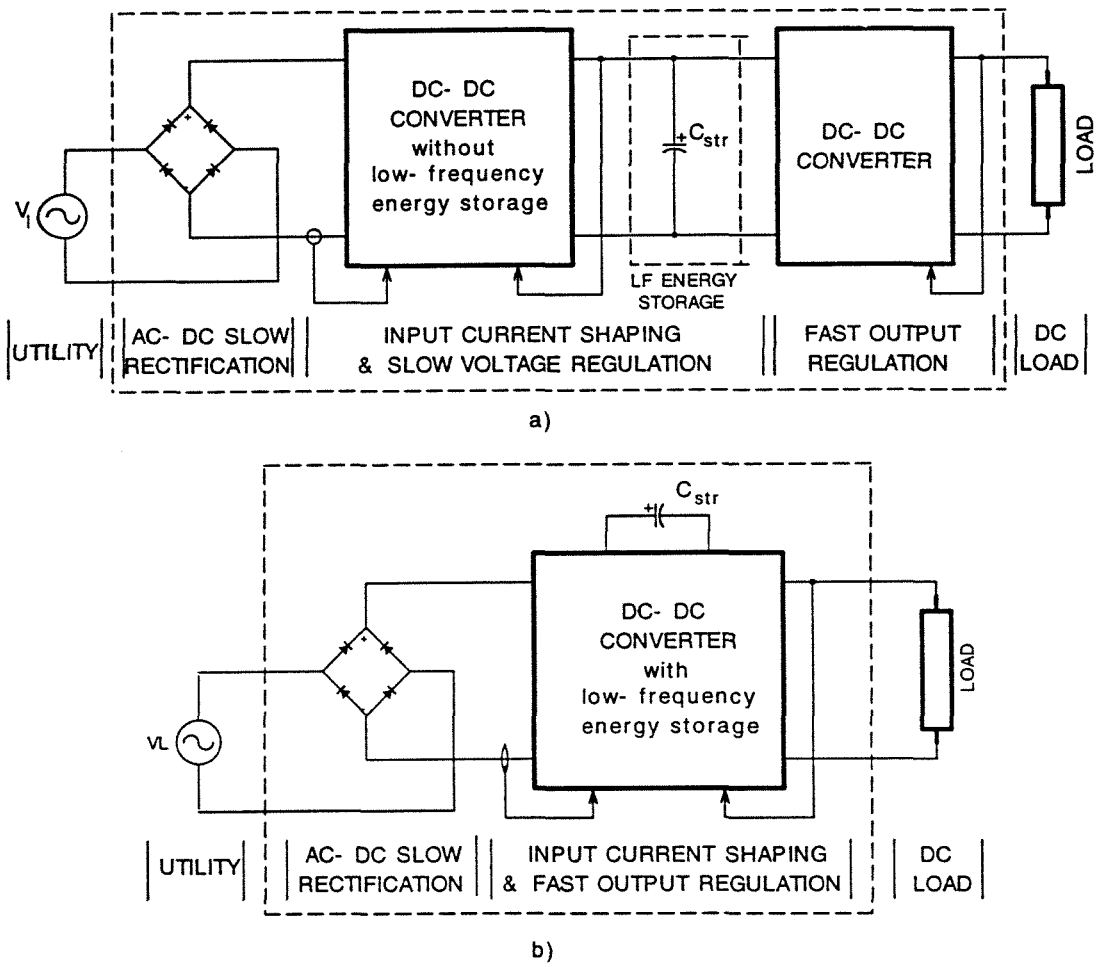


Figure 10.2: a) When energy is stored externally, fast output voltage regulation requires an additional DC-to-DC converter. b) Contrary, when energy is stored internally, both input current shaping and fast output regulation are provided in one converter.

1. Fast output voltage regulation is possible in addition to the input current shaping.
2. Overload and short circuit protection functions are inherently provided due to insertion of the active switch between the load and the energy storage capacitor.
3. Significant reduction in volume of the energy storage capacitor and size of the overall power stage can be achieved, particularly for low output voltages since the energy storage capacitor's voltage can be chosen independently of the output voltage.

Fast output regulation is, in general, obtained by connecting the low-frequency energy storage element to the load in a controllable manner by the active switch. This means that only a high frequency filter without the capability of storing low-frequency energy is required at the output.

By inserting an active switch in the loop consisting of the load and energy storage capacitor, overload as well as short circuit protection functions are inherently provided. The energy storage capacitor, therefore, will not uncontrollably discharge through the load if either overload or short circuit condition occurs. By action of the active switch, the load current can be limited in either of these two situations.

The size of the energy storage capacitor plays an important role in the overall size of the shaper. The capacitive energy storage is efficient in terms of density when the capacitor voltage is relatively high. It is shown in [54] that the volume of the energy storage capacitor is inversely proportional to the capacitor voltage to the .87 power, for any family of electrolytic capacitors. In practice, total volume of the energy storage capacitor is minimized if only one capacitor is used instead of a few of them in parallel, which means that current rating of the capacitor should be minimized. Therefore, for the same power level, the magnitude of the capacitor's low frequency current (at twice the line frequency) is lower if the capacitor voltage is higher and consequently current rating of the capacitor is lower. Furthermore, to supply low voltage loads (e.g., under 12V) directly from the energy storage capacitor, a relatively high volume capacitor with a high current rating must be used. Very often in practice, to satisfy hold up requirement for power supply, the large amount of energy must be stored in order to provide power to the load during utility power outages or brownouts.

10.3 Current Shapers with Current Feedback

Input current in these converters is programmed to follow the line voltage by closing the input current feedback loop as shown in Fig. 10.3. The converters are usually operated in continuous conduction mode (CCM), but this control technique can also be used in discontinuous conduction mode (DCM). This control technique is very often called *multiplier approach* and is described next.

There are two feedback loops in the control circuit (Fig. 10.3):

1. High bandwidth input current feedback loop.

2. Low bandwidth energy storage capacitor's voltage regulation loop.

Pulse width modulated (PWM) drive signal for the converter, $d(\omega t)$, is controlled by two inputs in the switch controller: current reference, $I_{ref}(\omega t)$, and input current, $I_g(\omega t)$.

Current reference, $I_{ref}|sin(\omega t)$, is produced by multiplying the attenuated rectified line voltage, $K_l V_l|sin(\omega t)$, with the output voltage v_c of the error amplifier EA_1, used for the voltage regulation. Voltage on energy storage capacitor, $V_{C_{str}}$, is compared with reference voltage, V_{ref}, in the low bandwidth error amplifier EA_1. In this way, amplitude of the current reference, $I_{ref}(\omega t)$, is adjusted for given line and load conditions.

The input current, $I_l|sin(\omega t)|$, is sensed either with resistor or the current transformer and compared with reference $I_{ref}(\omega t)$ in the switch controller. The switch controller is based on the current mode controller. Both peak current mode and average current mode control are used in practice.

The boost shaper is widely used as input current shaper and is shown as an example for explaining the multiplier approach in Fig. 10.4.

In the peak current mode control, the actual inductor (or the transistor) current waveform is directly compared to the current reference (set by the low bandwidth outer voltage loop) at the two inputs of the PWM comparator as shown in Fig. 10.5.

A serious problem associated with peak current mode control in current shaper circuit is the error between peak and average value since it causes distortion of the input current waveform. This error becomes much worse at lower current levels, especially when the

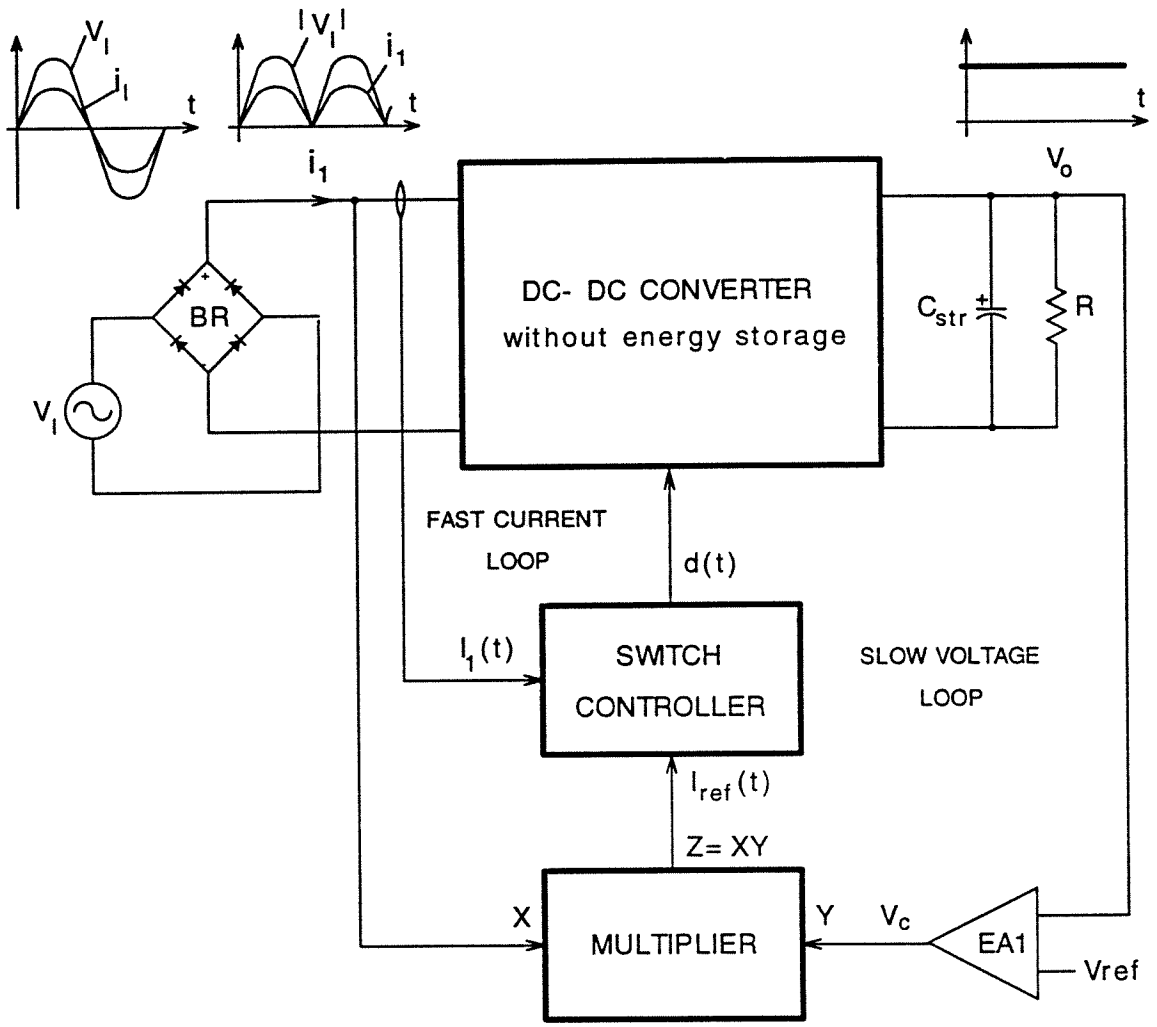


Figure 10.3: Block diagram of the shaper with input current feedback loop. Converter is usually operated in CCM.

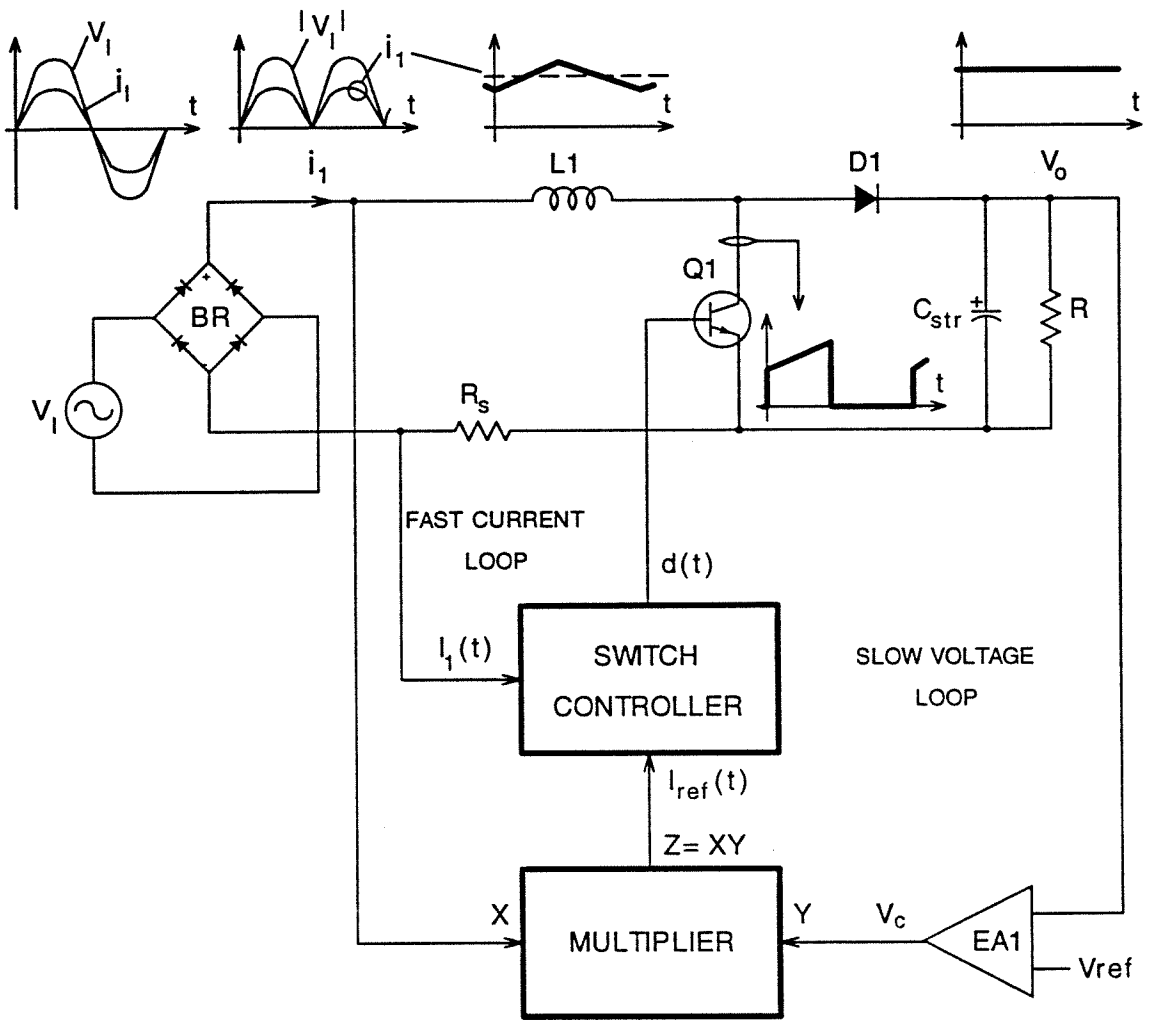


Figure 10.4: The boost shaper is used for explanation of the multiplier approach. Both input inductor current or transistor current can be programmed.

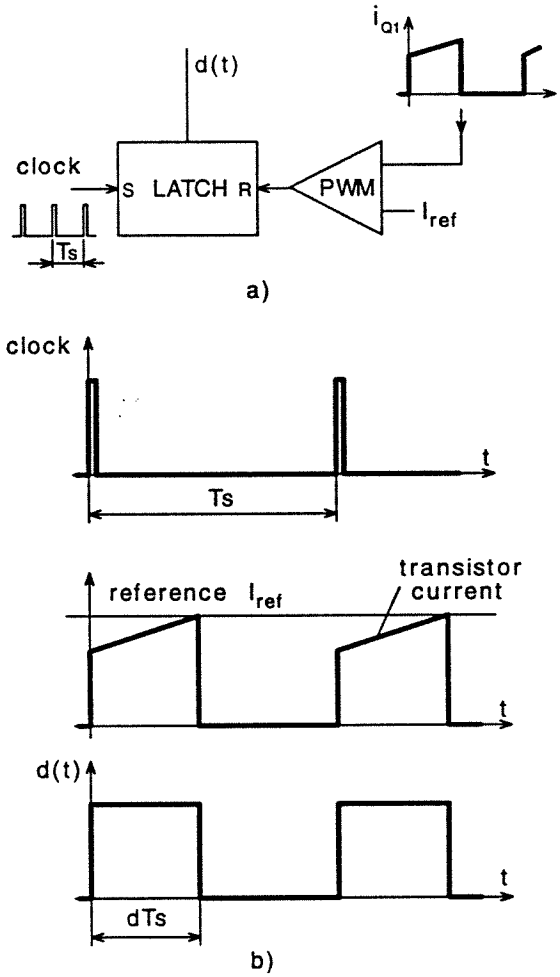


Figure 10.5: a) Simplified schematic of the peak current mode control and b) salient waveforms.

inductor current becomes discontinuous at the cusps every half cycle. To overcome this, a fairly large inductor is required to reduce the ripple current. The resulting shallow inductor ramp makes the already poor noise immunity even worse. The large inductor also introduces additional distortion in input current because of the increased "lag" at cusps of the input voltage.

The average current mode control technique overcomes the above problems by introducing a high gain current error amplifier (CA) into the current loop as shown in Fig. 10.6 [55, 56]. The difference between the current reference, I_{ref}, and the voltage drop on the sensing resistor R_s, V_{sen}, is amplified in the current amplifier CA. Amplified error signal, v_c, is then compared with a large amplitude sawtooth (oscillator ramp)

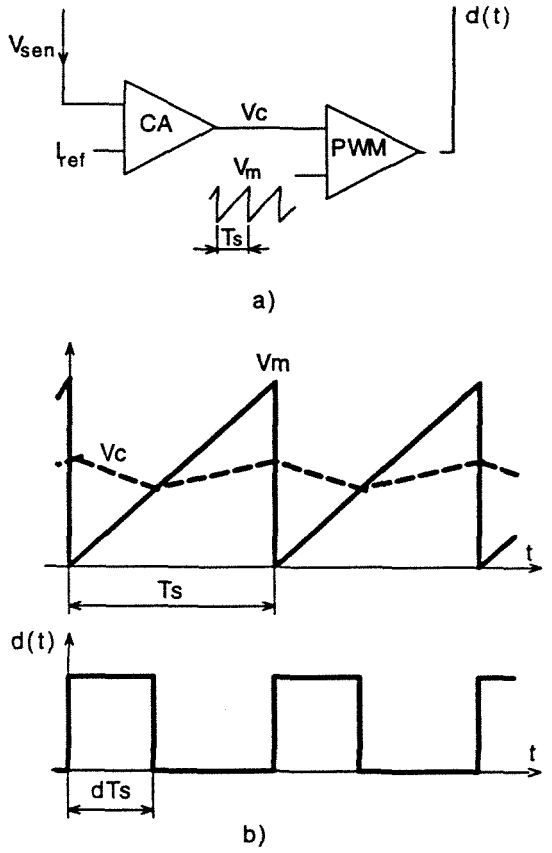


Figure 10.6: a) Switch controller with average current mode control used in the boost shaper and b) Salient waveforms.

waveform, V_m, in the PWM comparator which generates pulse width modulated drive signal d.

The advantages of the average current mode control over the peak current mode control technique are [55]:

a) High degree of accuracy is easy to achieve in both continuous and discontinuous conduction modes of operation.

b) Slope compensation is not required for stability.

c) Excellent noise immunity.

d) Smaller inductor value can be used.

The bandwidth of the error amplifier, EA_1, is usually limited below 10Hz in practice,

if the required total harmonic distortion (THD) of the input current has to be only a few percent.

The multiplier approach can, in general, provide unity power factor only in the topologies having step up capability. Thus, the buck converter and its extensions (forward converter, half-bridge and full- bridge topologies) cannot provide unity power factor even though the input current feedback loop is closed. The buck topology cannot draw any input current pulses when the rectified input voltage is less than the output voltage V_o.

10.4 Automatic Current Shaping

It has been shown in the past that when the converter is operated in DCM at constant switching frequency and duty ratio, the input current follows the input voltage automatically [57]. This approach is very attractive, particularly for low power levels, due to its simplicity, high efficiency, no interaction between the line impedance and the input current loop, and low cost.

The control circuit is very simple since the input current feedback is not required and only slow output voltage feedback loop needs to be used, as shown in Fig. 10.7. Thus, automatic current shaping is also called the *voltage follower* approach.

The output voltage is compared with reference voltage, V_{ref}, and the amplified error signal, v_c, is compared with the sawtooth ramp, V_m, in the PWM comparator which generates drive signal d for the power transistor. To keep output voltage constant against the line voltage and the load variations, duty ratio, d, is modulated by the v_c. By modulating duty ratio, the input current and consequently input power drawn from the line can be varied. The bandwidth of the voltage loop is limited to the frequency well below 120Hz in order to keep distortion in the input current at a low level. In this manner automatic current shaping and slow voltage regulation can be obtained with simple control. It should be pointed out that standard PWM integrated circuits, used for DC-to-DC converters, can also be used in automatic shapers without any additional circuitry.

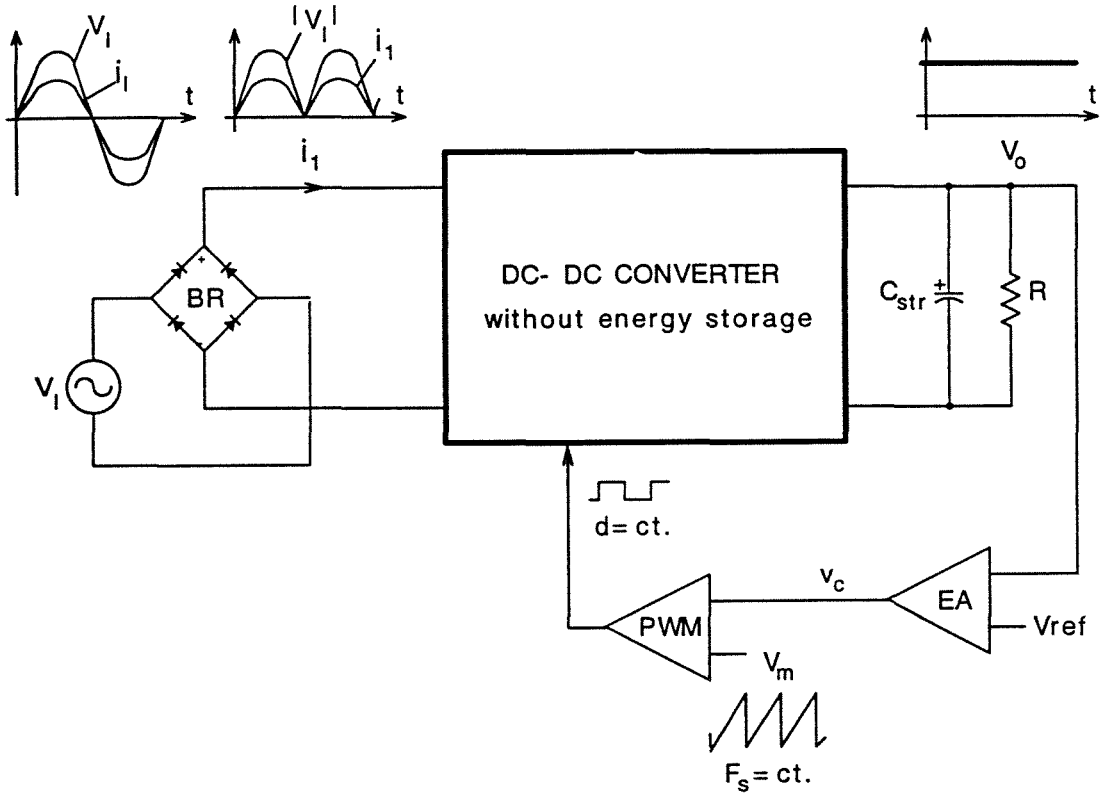


Figure 10.7: Block diagram of the automatic current shaper (voltage follower approach). Only the low bandwidth output voltage regulation loop is required in this case.

10.4.1 DCM Boost Shaper

The boost converter operated in DCM is very often used as an automatic current shaper for low power applications where isolation between line and load is not required (Fig. 10.8). The input inductor current averaged over a switching period (Fig. 10.8) is given by:

$$< i_1(\theta) >= \frac{|v_l(\theta)|}{2L_1} d^2 T_s [1 + \frac{d_2(\theta)}{d}] = \frac{|v_l(\theta)|}{R_{em}} [1 + f(\theta)] \tag{10.8}$$

where,

$$R_{em} = \frac{2L_1}{T_s d^2} \tag{10.9}$$

is the emulated resistance of the shaper, and $f(\theta)$ is nonlinear function which causes input current waveform distortion. When duty ratio and switching frequency are kept

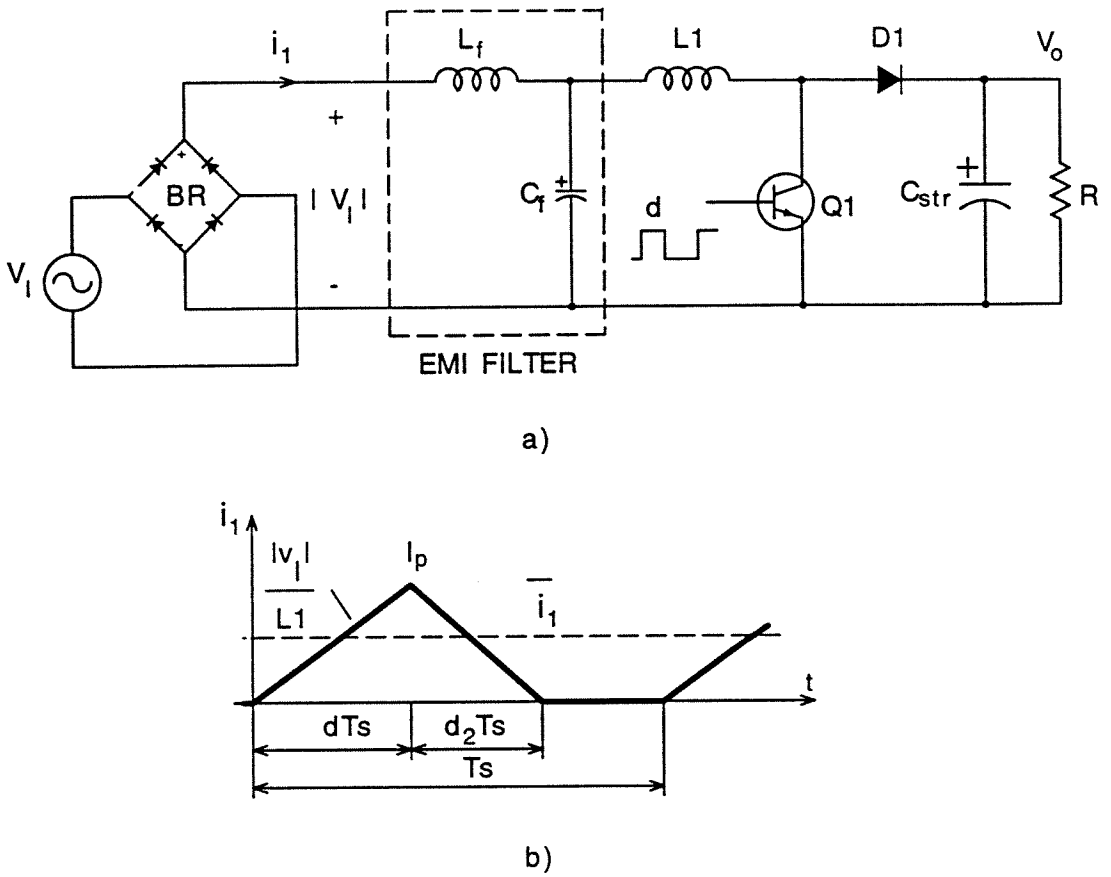


Figure 10.8: a) Automatic current shaper using the boost converter operated in DCM and b) input current waveform during the switching period T_s.

constant, the input current will, according to Eq. (10.8), follow the input voltage. The quality of the input current will be better when function $f(\theta)$, given by

$$f(\theta) = \frac{|v_l(\theta)|}{|v_l(\theta)| - V_{C1}} = \frac{|sin\theta|}{|sin\theta| - M} \tag{10.10}$$

is minimized. This can be achieved for large values of the conversion ratio M.

The power factor, PF, and total harmonic distortion, THD, are plotted as a function of M in Fig. 10.9. The input power factor greater than .97 is theoretically possible for conversion ratio $M > 1.5$. For example, the power factor greater than .992, and THD less than 13% can be theoretically achieved for M greater than 2.

An alternative method is to operate at the boundary of CCM and DICM but it

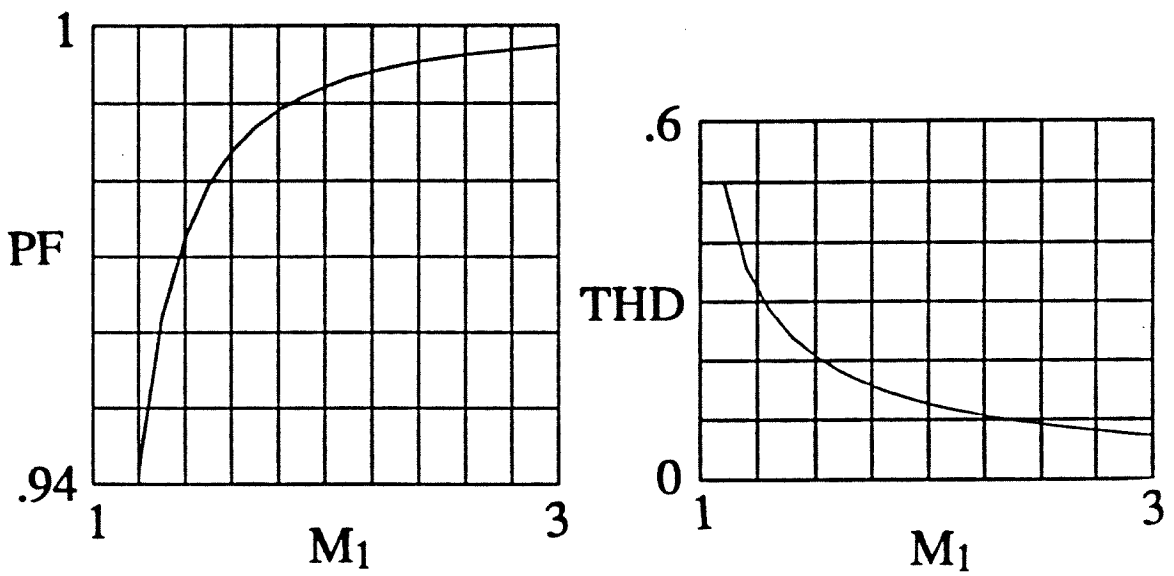


Figure 10.9: a)Power factor, and b) THD for the boost automatic current shaper as a function of the input stage conversion ratio $M = V_o/V_i$.

requires variable switching frequency and complex control circuit with multiplier [58]. The disadvantage of this control method is that switching frequency varies over a wide range with load and line voltage, which in many applications is unacceptable. Although a current shaper using DCM boost converter is very simple and popular it has some very serious practical drawbacks, such as:

1. Output voltage is always higher than the peak input voltage.
2. Isolation cannot be easily implemented.
3. High inrush current exists during startup and there is no overload protection because there is no active switch between input and output.

4. Near unity power factor can be provided only with high conversion ratio.

To effectively solve the above problems, an additional active switch and its control circuit need to be used.

10.4.2 DCM Buck Converter

The buck converter operated in DCM as an automatic current shaper is shown together with the input current pulse waveform in Fig. 10.10. The input current averaged over a switching period can be calculated from Fig. 10.10 (b) as:

$$\bar{i}_1(t) = \frac{D^2 T_s}{2L_1}(v_l(t) - V_o). \tag{10.11}$$

This topology does not provide unity power factor for two reasons. The first reason, as mentioned in Section 10.3, is that the input current remains zero until the rectified line voltage exceeds the output voltage. The second reason is that the input current pulse does not depend only on the input voltage but also on the output voltage. Due to this, the input current averaged over a switching period is a nonlinear function of the rectified input voltage.

The buck topology achieves its maximum power factor at very small conversion ratios and significantly drops with increase of conversion ratios. Therefore, the power factor is high over a smaller range of conversion ratios than in the boost.

10.4.3 DCM Flyback Shaper

The flyback converter is very popular when operated in DICM since the average input current exactly follows input voltage if switching frequency and duty ratio are kept constant, [57, 52, 59]. Automatic current shaper using the flyback converter is shown together with the input current pulse in Fig. 10.11.

This topology provides unity power factor as can be seen very easily from the input current pulse waveform shown in Fig 10.11 (b). The input current averaged over a switching period is given by:

$$\bar{i}_1(t) = \frac{1}{2} I_p d = \frac{1}{2} \frac{d^2 T_s}{L} v_l(t). \tag{10.12}$$

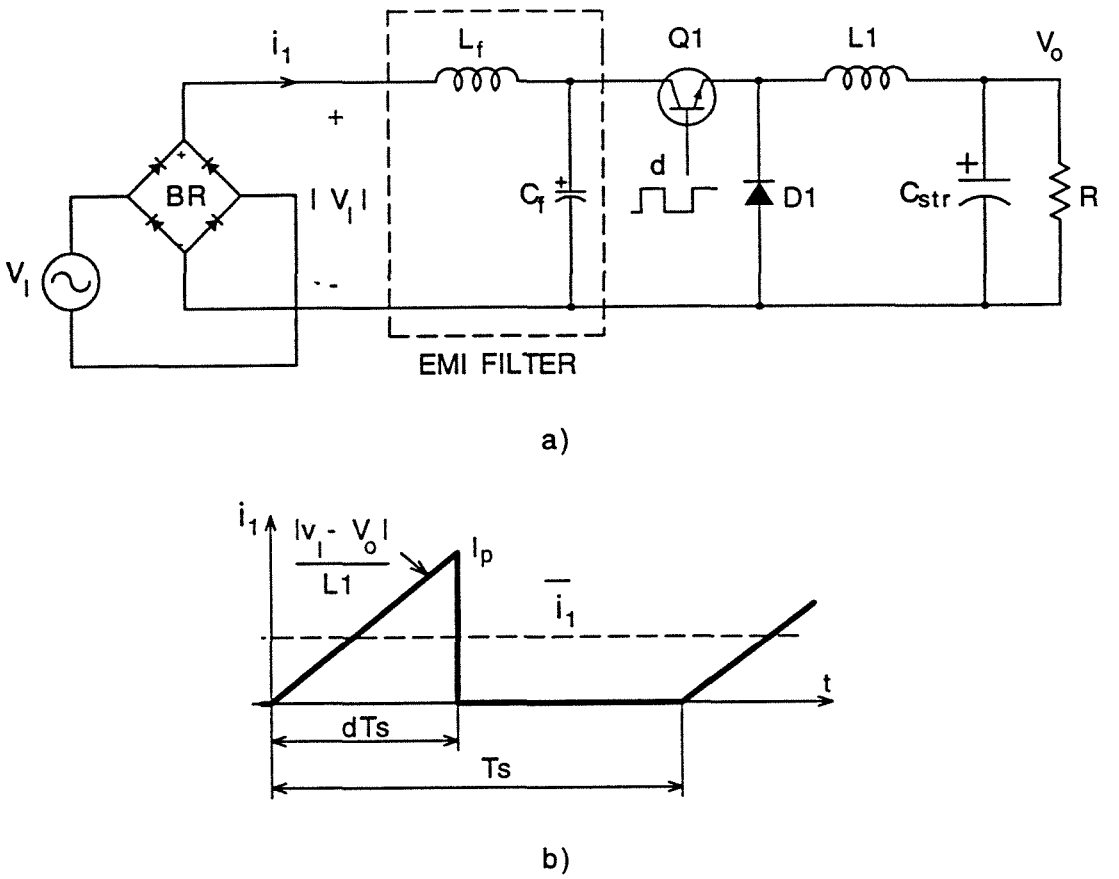


Figure 10.10: a) Automatic current shaper using the buck converter operated in DCM and b) input current waveform during the switching period T_s.

If duty cycle and switching frequency are both kept constant, the average input current, $\bar{i_1}(t)$ is a linear function of the input voltage $v_l(t)$. Notice that input voltage $v_l(t)$ can be an arbitrary waveform. If we define emulated resistance as in Eq. (10.9), then Eq. (10.12) can be rewritten as:

$$\bar{i_1}(t) = \frac{v_l(t)}{R_{em}} \tag{10.13}$$

from which one can see that the DCM flyback converter emulates resistance for all operating conditions with no control. This unusual feature is proposed in [57] and a detailed analysis for other converters is outlined systematically in [52].

DCM flyback topology achieves unity power factor automatically regardless of the conversion ratio. In addition, it overcomes all disadvantages of the DCM boost shaper

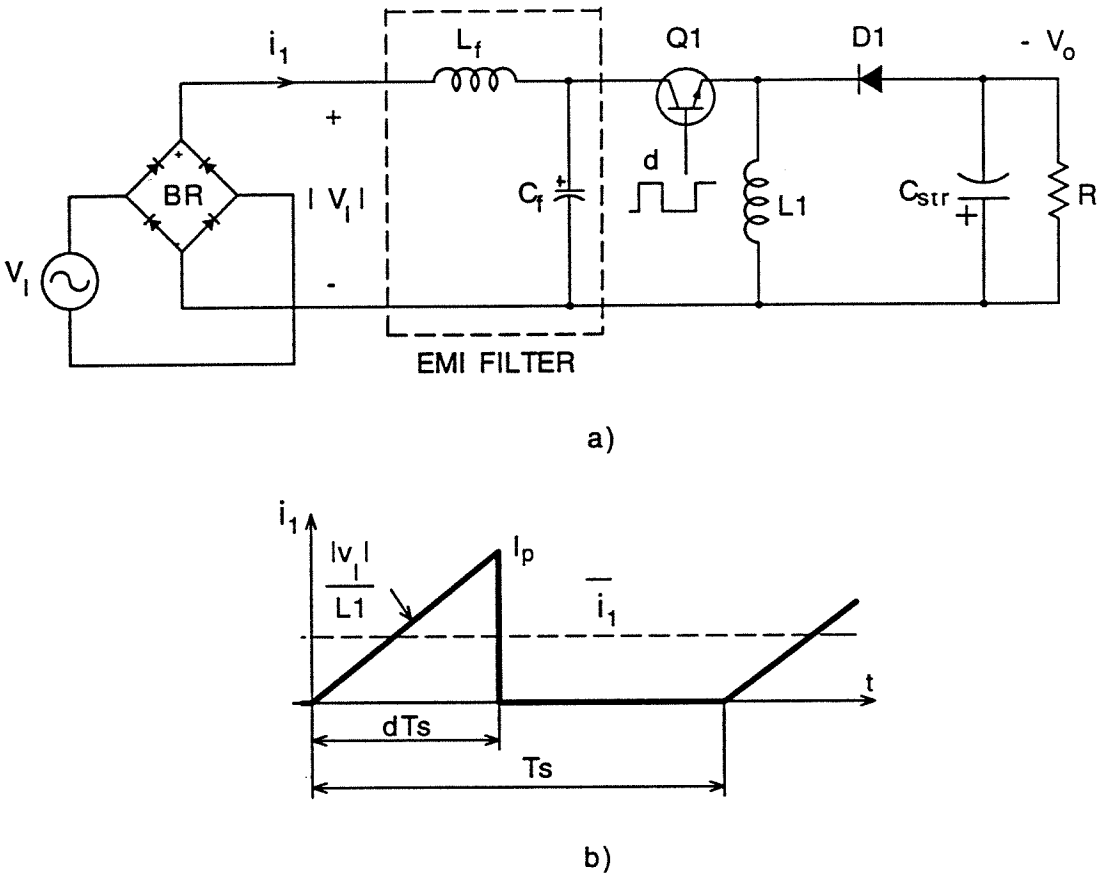


Figure 10.11: a) Flyback converter as a current shaper and b) input current waveform during the switching period T_s.

except one which is high input current switching ripple which is discussed in the next section.

10.5 Input Current Waveform Distortion

Two main non-idealities, inherent to any topology used in AC-to-DC applications which produce the input current waveform distortion and reduce the power factor are [52]:

a) "Lag" effect in the initial current at cusp of the input voltage.

b) Switching current ripple.

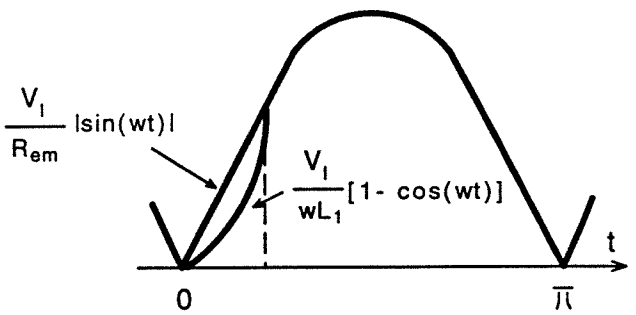


Figure 10.12: Illustration of the "lag" effect in the input current near the cusps of the line voltage.

Both effects are consequence of the finite inductance. Distortion of the boost input current waveform near the cusp of the rectified line voltage is shown in Fig. 10.12. Due to the finite value of the input inductance, L_1 in Fig. 10.4, the input current cannot follow the input voltage near the cusp even if the transistor $Q1$ is continuously held ON. The input current, i_l, is given by:

$$i_l(\theta) = \frac{1}{L_1}\int_0^{\theta} V_l sin\theta' d\theta' = \frac{V_l}{\omega_l L_1}(1 - cos\theta). \tag{10.14}$$

As can be seen from Eq. 10.14 the input current delays the line voltage for small values of θ and becomes equal to the current reference at $\theta = 2\gamma$. The angle γ is given [52] as:

$$tg\gamma \equiv \pi K_e \tag{10.15}$$

where,

$$K_e \equiv \frac{\omega_l L_1}{\pi R_{em}} \tag{10.16}$$

is the conduction parameter which involves the emulated resistance R_{em}, and line frequency ω_l.

This "lag" effect in the initial inductor current affects the power factor and in order to reduce the "lag" effect, the input inductance needs to be reduced. A more detailed analysis is given in [52].

The switching ripple in the input current waveform is also a consequence of the finite inductance and switching frequency. While the "lag" effect can be reduced by using

small inductance, which is the case in DCM shaper, the switching current ripple can, in general, be reduced by increasing either switching frequency and/or inductance or with additional filtering (shown in dashed box in Fig. 10.8, Fig. 10.10 and Fig. 10.11).

Distortion of the input current waveform due to switching ripple is more serious when the converter is operated in DCM than in CCM. Since the inductance has to be small in order to operate the converter in DCM, the switching frequency is the only means that can be used to reduce additional filtering components. Since the transistor's peak current and the AC flux in the magnetic cores are relatively high in DCM, high switching frequency will consequently reduce the efficiency of the shaper.

Therefore, an alternative method to reduce switching ripple current without increasing switching frequency is clearly desired and is explained in the next chapter.

10.6 Inrush Current Problem and Short Circuit Protection

One of the most serious drawbacks in the boost shaper (Fig. 10.8) is the high inrush current when power is initially turned on. In addition, overload as well as short circuit protection are not available without adding some additional circuitry, usually the active switch.

As one can see from Fig. 10.8, the energy storage capacitor, C_{str}, forms a loop with the line voltage through the rectifier diodes, BR and $D1$, and the input inductor $L1$. The capacitor C_{str}, being designed to provide input-output power balance, is relatively large. Low frequency voltage ripple as well as hold-up time requirements during blackouts or brownouts of the line voltage further increase the size of the C_{str}. Since the transistor, $Q1$, is not connected between the line and the capacitor C_{str}, it has no function in limiting input current during either initial startup or overload conditions.

The worst case occurs when power is turned on at the peak of the line voltage, the capacitor C_{str} is completely discharged, and the load, R, disconnected. Input inductor, $L1$, being a high frequency inductor, will very quickly saturate in a few switching periods after power is turned on. Equivalent circuit of the boost shaper during the startup is shown in Fig. 10.13.

Line voltage, $V_l sin(\omega_l t)$, and the bridge rectifier, BR, from Fig. 10.8 are replaced with

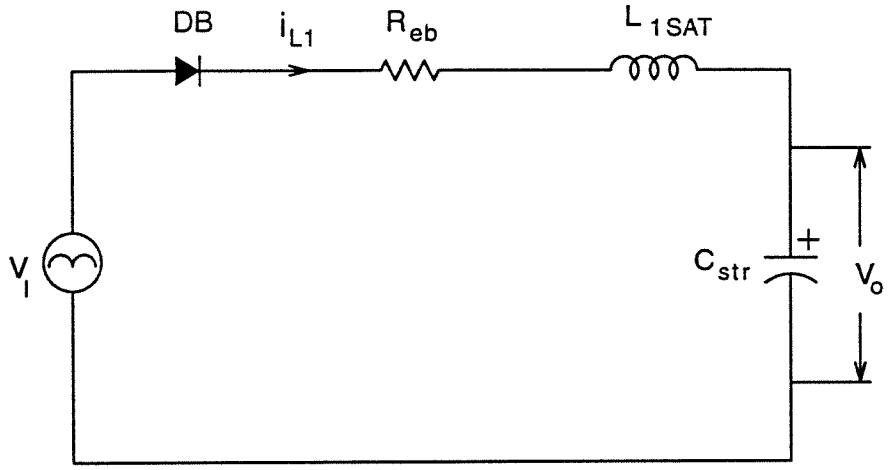


Figure 10.13: Equivalent circuit of the boost shaper during the power startup.

the voltage source $V_I|sin(\omega_l t)|$ and the diode DB, respectively. Equivalent resistance, R_{eb}, is the sum of all the resistances in the input current loop: dynamic resistance of the rectifier diodes (BR and $D1$), winding resistance of the input inductor, and ESR (equivalent series resistance) of the capacitor C_{str}. The inductance L_{1sat}, models saturated inductance of the input inductor, L_1.

The magnitude of the input current pulse is determined by the sum of the characteristic resistance, $R_{ob} = \sqrt{L_{1sat}/C_{str}}$, and series equivalent resistance R_{eb}. Overvoltage on the capacitor C_{str}, due to resonant charging, is determined by the Q factor, $Q = R_{ob}/R_{eb}$. The duration of the current pulse is determined by the natural frequency $\omega_{ob} = 1/\sqrt{L_{1sat}C_{str}}$, and the Q factor. It is, therefore, natural to expect that due to small saturated inductance L_{1sat} (usually tens of microhenries), and large capacitance C_{str} (usually μF/watt and larger), the peak current will be high, duration of the current pulse long, and voltage overshoot on the C_{str} very small. Also, due to a large value of the capacitance C_{str}, as compared to the L_{1sat}, the nature of the input current pulse will be dominated by the C_{str}.

Equivalent circuit in Fig.10.13 is used for simulation of the inrush current in the PSPICE program [51]. The simulation results are shown together with component values

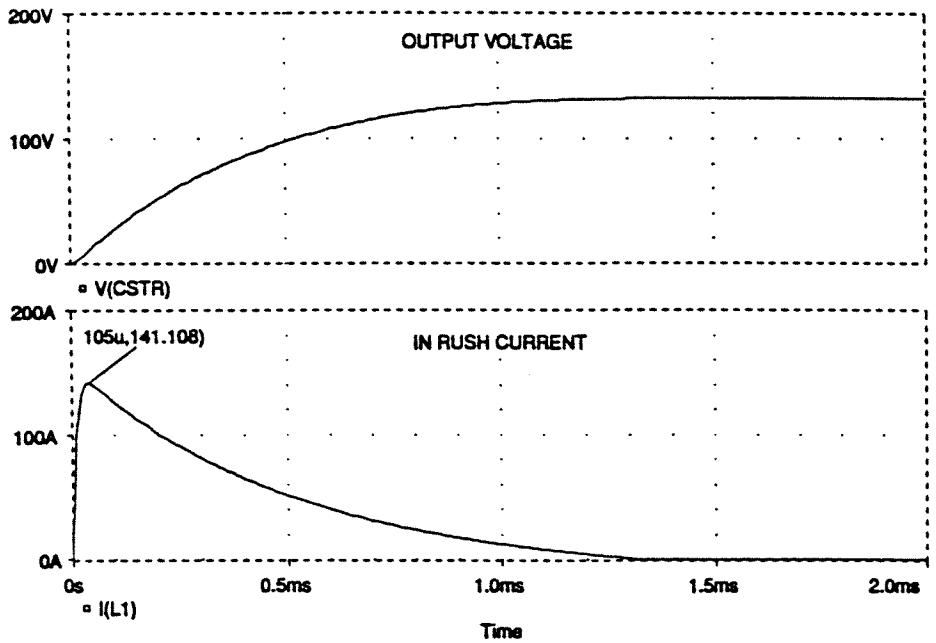


Figure 10.14: Inrush current and output voltage in the boost shaper for the following component values: $V_l = 150V$, $L_{1sat} = 10\mu H$, $R_{eb} = 1\Omega$ *and* $C_{str} = 470\mu F$.

used in simulation in Fig. 10.14.

Even though in the flyback shaper (Fig. 10.11) and the buck shaper (Fig. 10.10) the active switch (transistor $Q1$) disconnects energy storage capacitor C_{str} from the utility, the inrush current is not completely eliminated due to the high frequency input filter, $L_f C_f$. The filter capacitance, C_f, is usually at least two orders of magnitude smaller than the C_{str}, and saturated inductance of the filter inductor, L_{fsat}, is approximately of the same order of magnitude as L_{1sat} in the boost shaper. Thus, there will be significant reduction in both magnitude and pulse width of the in rush current pulse.

On the other hand, due to small input filter capacitance, C_f, a relatively large characteristic resistance of the input filter, $R_{of} = \sqrt{L_f/C_f}$, will result in resonant charging of the capacitor C_f above the line voltage. The maximum voltage on the C_f is twice the input voltage.

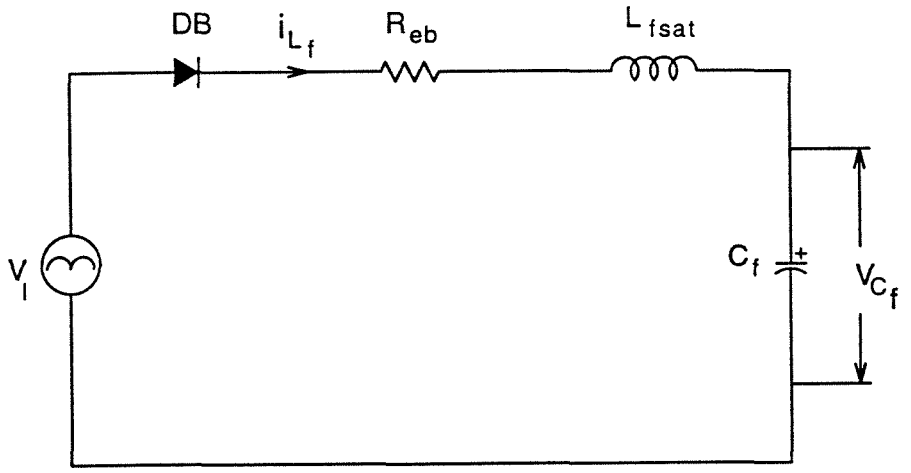


Figure 10.15: Equivalent circuit of the flyback shaper with input filter during the power startup.

Equivalent circuit during startup is shown in Fig. 10.15 while the simulation results are shown in Fig. 10.15.

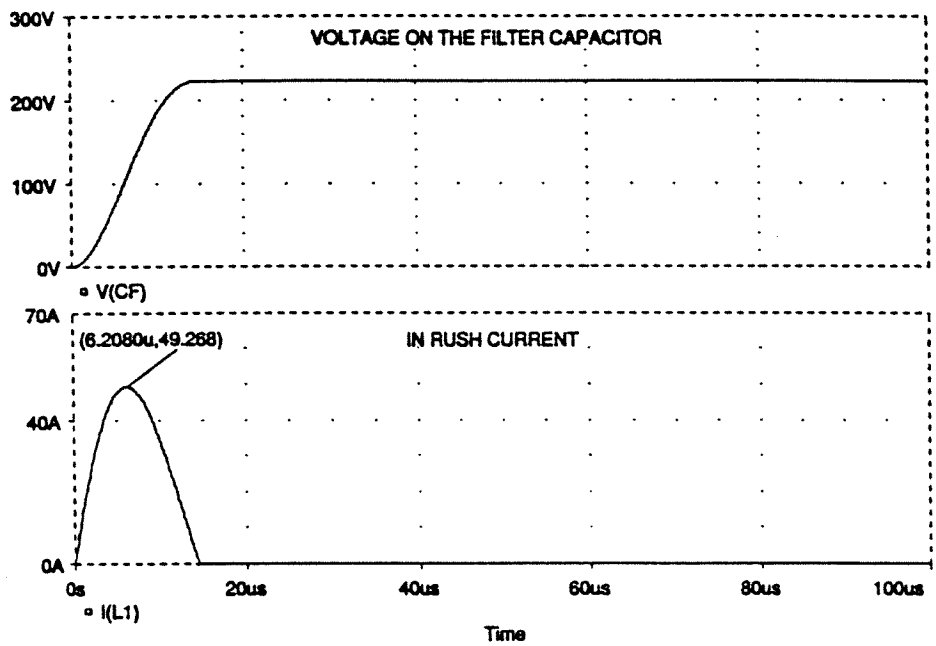


Figure 10.16: Inrush current and filter capacitor's voltage in the flyback shaper with input filter for the following component values: $V_l = 150V$, $L_{1sat} = 10\mu H$, $R_{eb} = 1\Omega$ *and* $C_f = 2\mu F$.

Chapter 11

Automatic Current Shaper Using Ćuk Converter

Automatic current shaper based on the Ćuk converter operating in DICM [60] is described in this chapter. In Section 11.3, it is shown that the input port of the converter *indeed* behaves as a resistor without additional current feedback even though it does not seem obvious from the input current waveform. Section 11.2 reveals that the Ćuk converter, due to inherent continuous input current even when operated in DICM, requires only small capacitive input filter in contrast to the other basic topologies. In Section 11.3, it is shown that essentially zero switching input current ripple can be obtained. Isolated version of the Ćuk converter with integrated-magnetics enables further improvement in performance as described in Section 11.4. Coupled inductors and integrated magnetics extensions of the converter provide additional reduction in inrush current as shown in Section 11.5. Experimental results which confirms predicted behavior and performance are shown in Section 11.6. The simple control, minimum size of the magnetics even at a very modest switching frequency of 35kHz, high input power factor, and high overall conversion efficiency suggest operation in DICM for low power level.

11.1 Input Current Shaper Using Ćuk Converter in DICM

Ćuk converter operating in DICM provides unity power factor automatically, even though it may, at first, appear not to be the case. The main reason for this is unusual behavior of the converter in DICM as described in [62].

The basic Ćuk converter with separate inductors is shown in Fig. 11.1 and three switched networks together with salient waveforms, used for the analysis, are shown in Fig 11.2 (a) and (b), respectively. If the switching frequency is much higher than the line

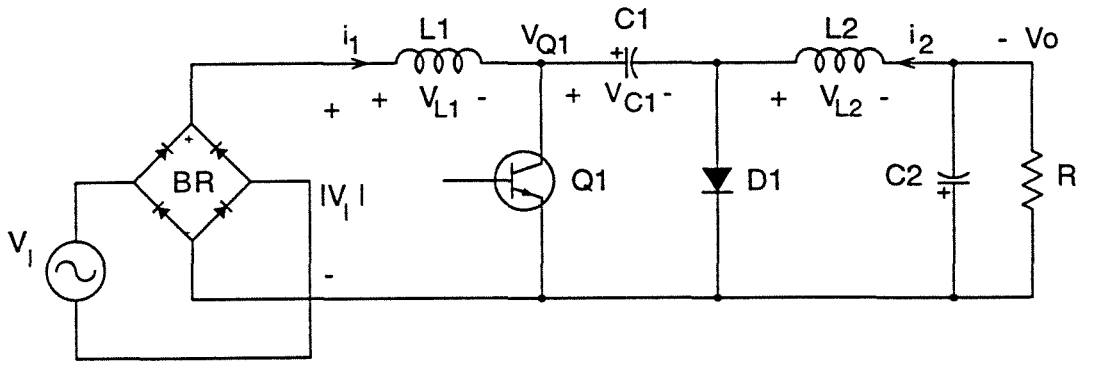


Figure 11.1: The basic Ćuk converter with separate inductors.

frequency then, the waveforms averaged over the switching period T_s can be used in the following steady-state analysis [52]. Also we will assume that efficiency of the converter is 100% so the input power equals the output power.

From the volt-seconds balance on the inductors, L_1 and L_2, we can write (Fig 11.2 (b)):

$$\frac{v_o}{v_l} = \frac{d}{d_2} \tag{11.1}$$

and from the power balance (100% efficiency):

$$\frac{\bar{i}_1}{\bar{i}_2} = \frac{d}{d_2}. \tag{11.2}$$

Note that the onset of DICM in the Ćuk converter occurs when the diode current, which is the sum of input and output inductor currents becomes zero. This leads to the existence of the constant current level i which exists in both inductors (when the diode is turned off) [62], and the third switched network (both transistor and diode off) is created. Using results from [62] and referring to the waveforms in Fig 11.2 (b), the following expression for the input current averaged over a switching period can be written

$$\bar{i}_1 = \frac{v_l}{2L_1} dT_s(d + d_2) + i. \tag{11.3}$$

From Eq. (11.3) it follows that average input current $\bar{i}_1$ is not proportional to $v_l(t)$ for constant duty cycle d, since both d_2 and i are also strong functions of $v_l(t)$. The

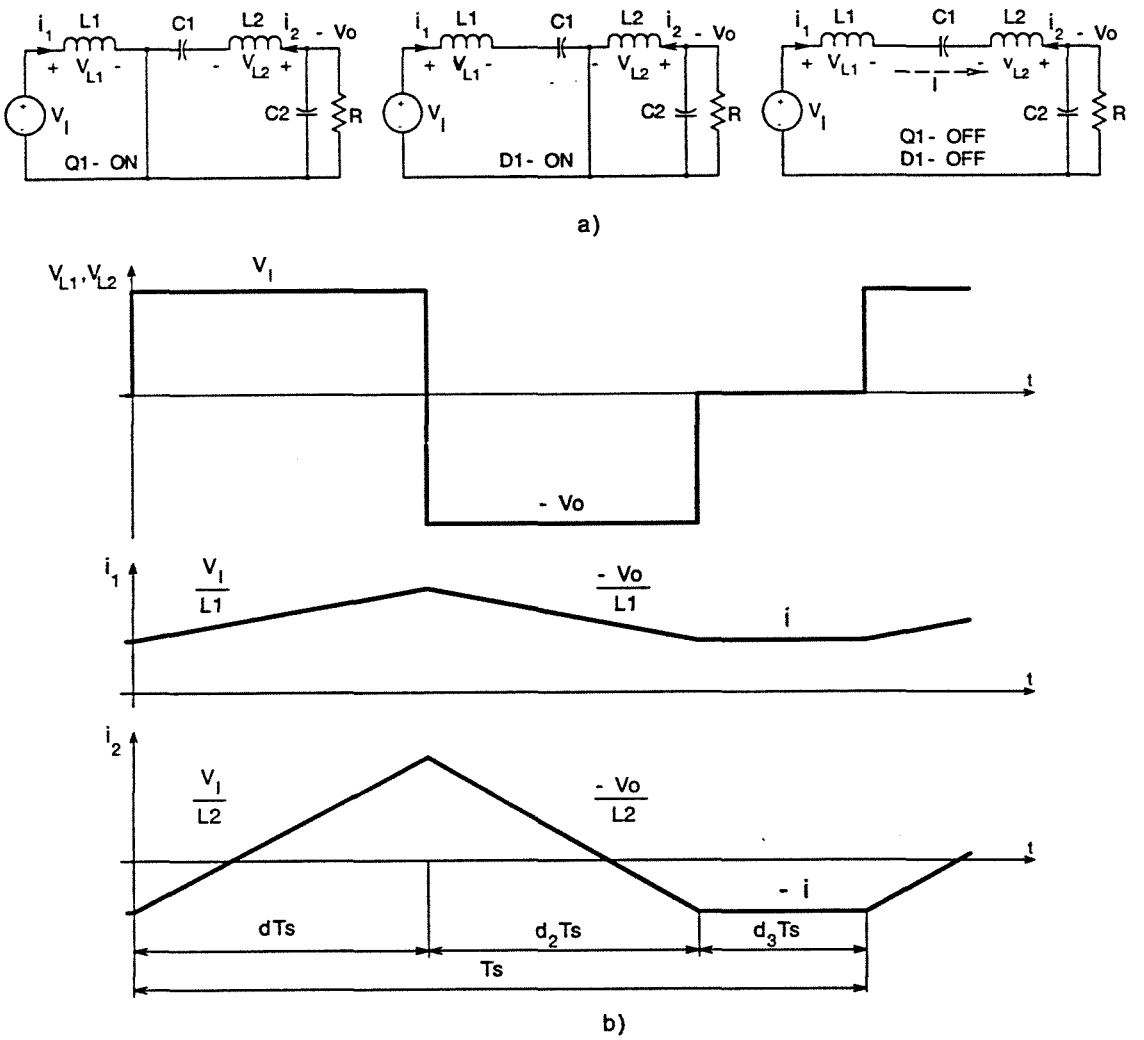


Figure 11.2: a)Three switched networks for the Ćuk converter in DICM, b) Waveforms used for determination of the steady-state in DICM.

following derivation, however, proves that i_1 is indeed linearly dependent on $v_l(t)$. From Fig 11.2 (b) the average output inductor current is:

$$\bar{i}_2 = \frac{v_l}{2L_2} dt_s(d + d_2) - i. \tag{11.4}$$

The sum of input and output currents gives:

$$\bar{i}_1 + \bar{i}_2 = \frac{1}{2}\frac{v_l}{L_e} dT_s(d + d_2) \tag{11.5}$$

$$L_e = L_1 \parallel L_2 = \frac{L_1 L_2}{L_1 + L_2} \tag{11.6}$$

where, L_e is effective inductance of the converter. By substitution of Eq. (11.2) into Eq. (11.5) we get:

$$\bar{i}_1(1 + \frac{d_2}{d}) = \frac{1}{2}\frac{v_l}{L_e} dT_s(1 + \frac{d_2}{d})d \tag{11.7}$$

which after cancellation of terms in brackets results in:

$$\bar{i}_1 = \frac{1}{2}\frac{d^2 T_s}{L_e} v_l(t). \tag{11.8}$$

Note that a rather surprising result is obtained: Eq. (11.8) has the same form as Eq. (10.12) for the flyback converter. The only difference is that in Eq. (11.8) equivalent inductance, L_e from Eq. (11.6), is used instead of the input inductance L_1. If we define, as for the flyback converter, emulated resistance as:

$$R_{em} = \frac{2L_e}{T_s d^2} \tag{11.9}$$

then Eq. (11.8) is exactly the same as Eq. (10.13). By keeping duty cycle and switching frequency constant the average input current in Ćuk converter operating in DICM also follows the input voltage exactly. Notice that input voltage is not specified in this analysis and hence can be arbitrary waveform.

Therefore, Ćuk converter provides unity power factor automatically with no control when operated in DICM.

The schematic of the shaper is shown in Fig. 11.5.

Conversion ratio for the automatic shaper the Ćuk converter is given by:

$$M = \frac{V_o}{V_l} = \frac{d}{2\sqrt{K_e}} \tag{11.10}$$

where,

$$K_e = \frac{2L_e}{RT_s} \tag{11.11}$$

is the conduction parameter of the converter.

The output voltage regulation is provided by closing the feedback loop in the usual manner as shown in Fig. 11.5. The output voltage is compared with the reference, V_{ref}, and amplified error signal, v_c, is compared with sawtooth ramp, V_s, generating drive signal d for the power transistor $Q1$. In order to keep the output voltage constant, duty ratio is modulated by controlling signal v_c. By modulating duty ratio d, the emulated resistance, R_{em} in Eq. (11.9), is also modulated thus, controlling the input power drawn from the line.

Therefore, with the output voltage feedback closed, duty ratio d, and consequently the emulating resistance R_{em}, will be function of the control voltage v_c. The bandwidth of the voltage loop is limited to the frequency well below twice the line frequency in order to keep distortion in the input current at low level. In this manner automatic current shaping and slow voltage regulation can be obtained with simple control.

The current shaper will operate in DICM when [60]:

$$K_{e,max} < \frac{1}{(M_{max}+1)^2} \tag{11.12}$$

where,

$$K_{e,max} = \frac{2L_e}{R_{min}T_s} \tag{11.13}$$

is maximum value of the conduction parameter K_e, which occurs at maximum output power level (minimum load resistance), and M_{max} occurs at minimum of the line voltage. From Eqs. (11.12)-(11.13) one can determine minimum value of the equivalent inductance required for DICM of operation as:

$$L_{e,min} < \frac{R_{min}T_s}{2(1+M_{max})^2}. \tag{11.14}$$

11.2 Current Waveform Distortion Due to Switching Ripple

The input current waveforms for the boost, flyback and Ćuk converter operating in DICM are shown in Fig. 11.3. As one can see, the input current in the Ćuk converter

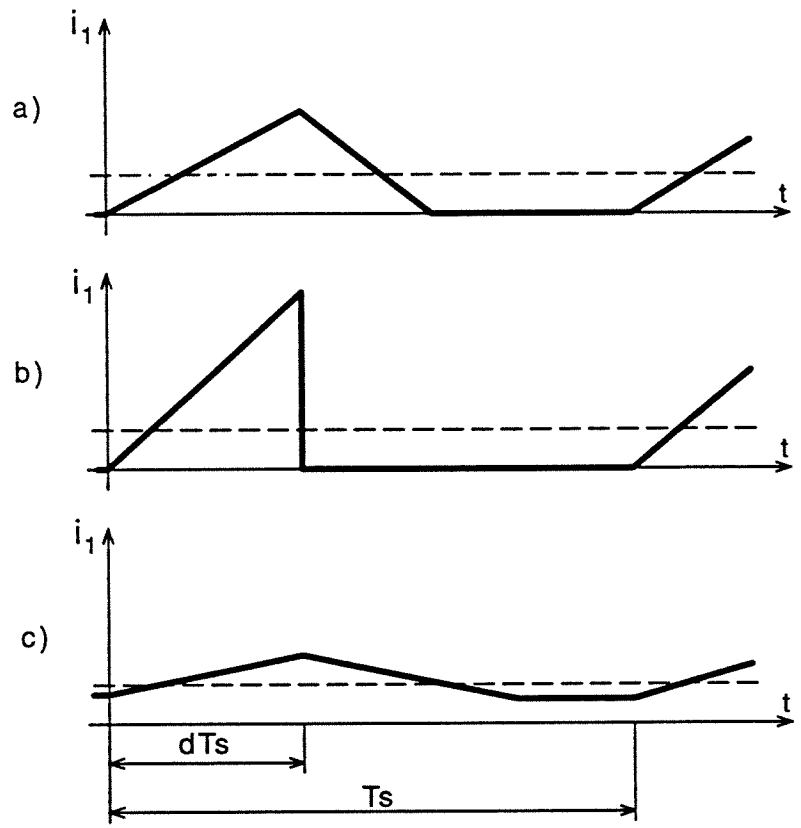


Figure 11.3: Input current waveforms for the a) boost; b) flyback: and c) Ćuk converter all operated in DICM.

contains smaller switching ripple than the boost or the flyback converter because the input current does not go to zero after the diode stops conducting. Hence, the input current in the Ćuk converter will be filtered more easily. It should be noticed that the DICM Sepic converter has the same input current waveform as the Ćuk converter.

In order to eliminate high frequency switching in the line current it is necessary to use high frequency filter at the converter's input. Both the boost and the flyback converter require $L-C$ input filter (shown in dashed box in Figs. 10.8 and 10.11). Size of the input filter can be reduced by increasing the switching frequency of the converter. Since both the transistor's peak current, and the ac flux swing in the magnetic core are relatively high in DICM, high switching frequency very often results in degradation of the converter

efficiency.

Since the input current in the Ćuk converter is continuous even the converter is operated in DICM (Fig. 11.3 (c)) only a small capacitor, C_f, on the ac side of the rectifier bridge, BR, is required as shown in Fig. 11.1. The reactive component of the line current flowing into the filter capacitor, C_f, introduces phase shift in the input current and thus reduces power factor. This phase shift becomes more dominant at lower power levels since the reactive current of the filter capacitor is independent of the output power.

Hence, an alternative method to reduce ripple current without increasing the switching frequency is clearly desired. To obtain an "ideal" current shaping, we therefore, require small size of the magnetics, moderate switching frequency, no need for additional filtering and isolation between the line and load. All these requirements are satisfied in the coupled-inductors extension of the Ćuk converter (Section 11.3), or integrated magnetics topology (Section 11.4).

11.3 Coupled-Inductor Extension

In applications where isolation between the line and the load is required, the high frequency transformer can be added as shown in Fig. 11.4. In this case, even though the transformer is ungapped and very small at high frequencies, still three separate magnetic structures need to be used.

The concept of coupled-inductors [63, 64, 65] has been proven in design of Ćuk converter for various applications. It is shown in this and the next section that it can also be used for input current shaping. The switching ripple current is eliminated from the input inductor, L_1, and "steered" into the output inductor, L_2. This unique feature becomes very useful since, even when converter operates in DICM the input current is continuous and ripple free. The price paid for this is in the output inductor current ripple which remains the same as before coupling.

Using the coupled-inductors structure, both the size and weight are reduced simultaneously with the increase of efficiency and the performance improvement. Since the actual (measured) inductance of the input inductor is smaller than it was before coupling, the "lag" effect in the input current is reduced, and since its effective value is an

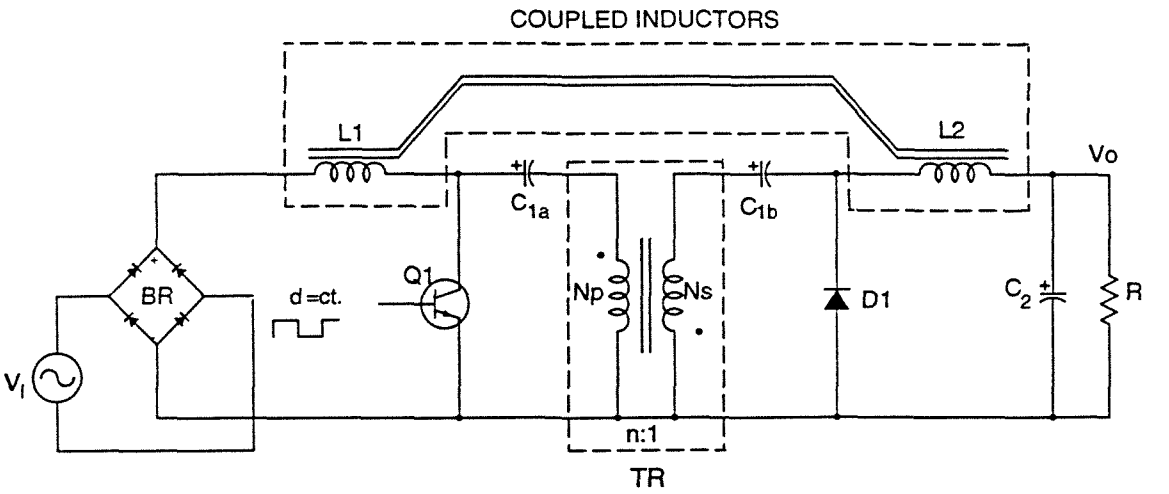


Figure 11.4: Isolated version of the Ćuk converter. The isolation transformer being high frequency component is small. Input and output inductors can be coupled onto a single magnetic core as shown with dashed lines.

order of magnitude larger than measured value, significant reduction in the switching current ripple is obtained. Therefore, by using coupled-inductors input power factor will be improved. This feature becomes very useful since even for DICM of operation neither additional filtering of the input current nor high switching frequency are necessary to obtain high input power factor, as is needed for boost, flyback or buck converter.

It should be pointed out that the steady-state analysis given in Section 11.1 for the automatic current shaper based on the Ćuk converter with the separate inductors is also valid for the coupled-inductors extension. The only difference is that the effective inductance L_e (Eq. (11.6)) used for definition of the conduction parameter K_e (Eq. (11.11) in case of the coupled-inductors becomes:

$$L_e = L_2 \tag{11.15}$$

since the switching current ripple is determined only by the output inductor L_2.

In applications where isolation between the line and load is required, a high frequency isolation transformer can be used. Even though the input and output inductors are integrated onto one magnetic core, still separate magnetics are needed for the transformer. Also, large switching ripple in the output current is present. In such applications the

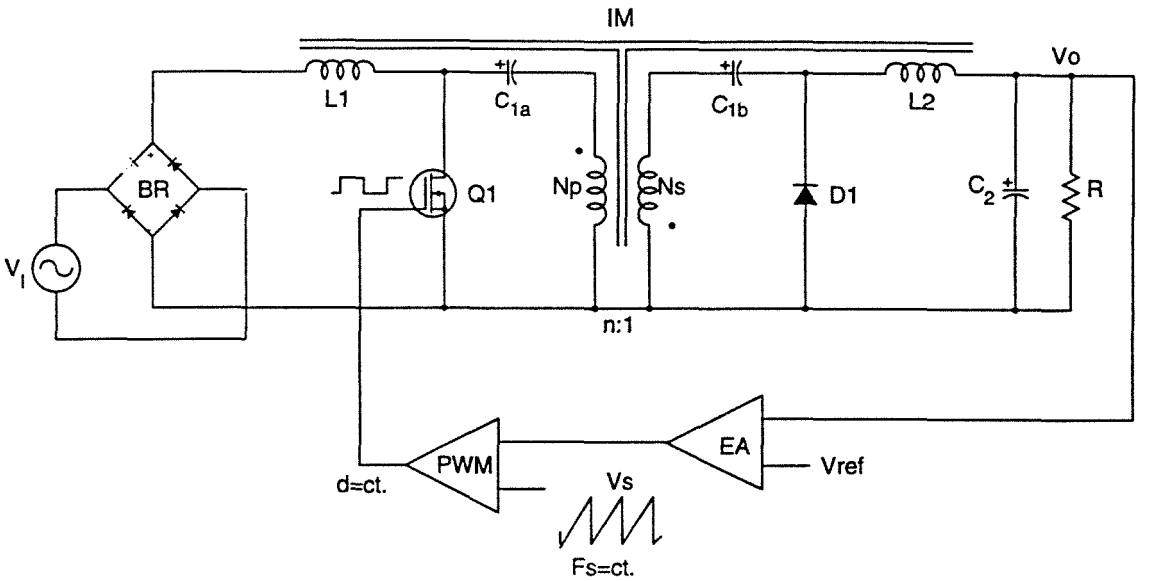


Figure 11.5: Input current in the IM Ćuk converter when operated in DICM at constant duty ratio automatically follows the line voltage. Only the DC output feedback loop is needed.

concept of integrated magnetics is preferable as described in the next section.

11.4 Integrated Magnetics Topology

Further improvement in the input current shaping can be done using isolated version of the Ćuk converter with integrated magnetics (IM) [63, 65], as shown in Fig. 11.5. The input and output inductors and isolation transformer are integrated onto one magnetic structure. Switching current ripple from the input and the output inductors is "steered" into the transformer windings where ac current (magnetizing current) inherently exists. This unique feature inherent to the Ćuk converter enables that the size of magnetics can be kept small even at very modest switching frequency of 40kHz and a high input power factor can be achieved without additional filtering.

Detailed analysis and design procedure for IM structures are given in [65]. What structure of the magnetic core will be used for IM design depends on a few factors: cost of the design, size and weight, sensitivity of the design and residual ripple. Sensitivity of

the structure is actually the sensitivity of the ripple current to changes in the turns ratio and in the air-gap size. Residual ripple is the ripple current generated due to mismatch in the drive voltage waveforms on the windings of the IM, caused by the second-order effects in the IM and in the converter circuit. Both sensitivity and residual ripple can be reduced by increasing the effective leakage inductance seen by the error voltage, or in other words IM needs to be designed with as high as possible leakage inductance [65]. The standard EE core with spacer can be used as a compromise between cost and the performance.

Analysis given in Section 11.1 is still valid for Integrated magnetics extension. The difference is only in the effective inductance which is now magnetizing inductance of the transformer since the switching current ripple appears only in the transformer.

The full advantages of this solution are:

1. Zero switching current ripple in both input and output inductors.
2. Isolation between line and load.
3. Wide range of the output voltage.
4. Overload and start-up current protection.
5. Minimum size of the magnetics at modest switching frequency and higher converter efficiency.

11.5 Inrush Current and Overload Protection

Since the input part of the Ćuk converter, is boost-like, one can erroneously conclude that the Ćuk shaper exhibits the same inrush current and overload protection problem as the boost shaper. This is not the case for two reasons:

a) Size of the primary side energy transferring capacitance in the Ćuk converter, C_1 in Fig. 11.1, is typically two to three order of magnitudes smaller than the energy storage capacitance C_{str} connected across the load.

b) The load is connected in parallel with the rectifier diode $D1$ instead of the input as in the boost shaper.

By assuming the same saturated input inductance, L_{1sat}, which is usually the case, one can immediately see that reduction in both magnitude and width of the inrush current pulse are at least an order of magnitude or even more. The size of the energy transferring capacitor C_1 is determined by magnitude of the switching voltage ripple which can be tolerated. The size of this capacitor should be as small as possible to minimize its physical size and to provide better dynamics. In practical design, the energy transferring capacitor is chosen such that switching voltage ripple on it is about 20% of the DC voltage value and therefore, it is almost three order of magnitudes smaller than the output capacitor C_o. The energy transferring capacitor, C_1, is of the same order of magnitude as the capacitance C_f in the input filter used with the flyback or the boost shaper (Section 10.6). Thus, inrush current in the basic Ćuk converter *is not* worse than in the flyback or the buck shapers with the input filter.

Another very important difference between the Ćuk and the boost shaper is that the Ćuk converter has inherently built in both overload as well as short circuit protection, which is not the case in the boost shaper. Even though transistor $Q1$ has the same location in these two topologies, the main difference is in the connection of the load to the input. While in the boost converter the load forms loop with the input through the diode $D1$ (Fig. 10.8), the load in the Ćuk converter is connected to the input through the small energy transferring capacitor C_1 (Fig. 11.1). By keeping transistor $Q1$ off, there is no current flowing from the input to the load once the capacitor $C1$ was charged, and therefore, the load is protected.

Further reduction of inrush current in the Ćuk shaper is achieved when either coupled inductors or integrated magnetics extension are used. The input inductor is, in both cases, designed to have large leakage inductance which turns out to be a very useful during the startup. Namely, the leakage inductance, being distributed in the air around the core, will not be affected by the saturation of the magnetic core. Therefore, the large leakage inductance simultaneously reduces magnitude and lengthens pulse width of the inrush current.

Simulation on the PSPICE is repeated using equivalent circuit in Fig. 10.15 but with different value for the inductance. The results of the simulation are shown together with

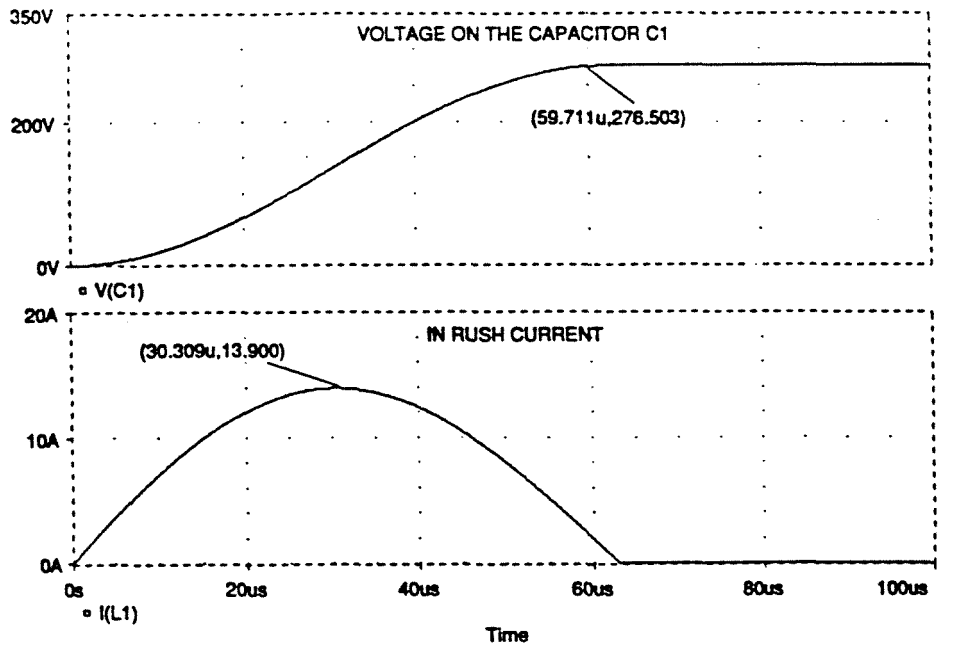


Figure 11.6: Inrush current and output voltage in the Ćuk shaper with coupled-inductors. The components used in simulation are: $V_l = 150V$, $L_{lkg} = 200\mu H$, $R_{eb} = 1\Omega$ and $C_1 = 2.2\mu F$.

component values used in simulation in Fig. 11.6.

As a comparison, the simulation results of inrush current in both the boost and the Ćuk converter are shown in Fig. 11.7. From the above analysis and results obtained from the simulation, it is evident that inrush current in the Ćuk shaper with coupled-inductors or integrated magnetics is drastically reduced compared to the boost shaper (Fig. 10.14). It is also reduced compared to the flyback or the buck shaper with the input filter (Fig. 10.16). Due to this, no additional components are needed to limit inrush current.

The problem associated with the voltage overshoot on the capacitance $C1$ and consequently on the transistor $Q1$ is not serious. The simple circuit, consisting of the zener diode $ZD1$ and diode $D2$, could be connected across the $C1$ in order to clamp voltage on the transistor $Q1$. The zener diode, $ZD1$, clamps voltage on the capacitance C_1 and dissipates excessive energy stored in the leakage inductance, which would be normally discharged into the C_1.

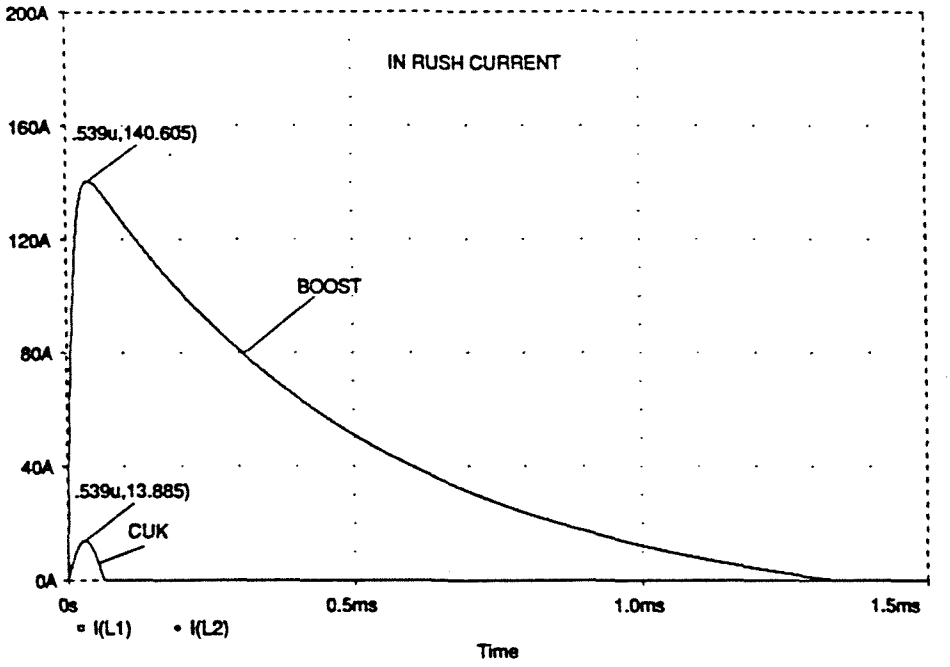


Figure 11.7: Inrush current and output voltage in the boost and the coupled-inductors Ćuk shaper. The components used in simulation are: $V_l = 150V$, $L_{lkg} = 200\mu H$, $R_{eb} = 1\Omega$, $C_1 = 2.2\mu F$ *and* $C_{str} = 470\mu F$.

11.6 Experimental Results

To demonstrate high performance of the current shaper based on the Ćuk converter with integrated magnetics operating in DICM, a 200W prototype was designed to operate from 120VAC line voltage. Output voltage of 50VDC and switching frequency of 35kHz were selected.

In order to demonstrate advantages of using integrated magnetics, first consider the use of separate inductors. The component values referring to Fig. 11.1 are: $L_1 = 720\mu H$, $L_2 = 15\mu H$, $C_1 = 1.25\mu F$, $C_o = 22mF$, $R = 25\Omega$, $Q1 = IRF740$, and $D1 = SES5403$.

Line voltage and current waveforms are plotted for output power of 100W in Fig. 11.8 (a). The input current follows the line voltage very well and is in phase. The input and the output currents during the switching period at the peak of the line voltage are plotted in Fig. 11.8 (b). The switching ripple of 1.2A is observed in the input current which is about 60% of its rms value. Also, the switching ripple of 11A is observed in the output inductor current which is 2.75 times bigger than the 4A peak current. To reduce the

switching ripple currents an additional filtering is needed.

Then, the Ćuk converter with integrated magnetics was tested. In order to reduce cost of the design, the standard $EE-42$ core with common was used for the IM design, even though the size and weight are not optimized. The transformer is wound on the center leg and input and output inductors are wound on the outer legs. Turns ratio of transformer was chosen to be $n = 2$. Number of turns and effective inductances are listed below together with other components (referring to Fig. 11.5): $N_1 = 93T$, $N_2 = 48T$, $N_p = 32T$, $N_s = 16T$, $L_1 = 710\mu H$, $L_2 = 180\mu H$, $L_p = 100\mu H$, $C_1 = 2.2\mu H$, $C_2 = 10\mu H$, $Q1 = IRF740$, and $D1 = 10CTF40$.

Experimental waveforms are shown in Figs. 11.9 -11.11. The input current and the line voltage are plotted at full output power of 200W in Fig. 11.9. As can be seen, the input current follows the line voltage very well and is ripple free. No filter capacitor was used in front of the bridge rectifier for additional filtering of the switching current ripple.

Input and output current waveforms during the line period are plotted in Fig. 11.10 (a). Switching current ripple is significantly reduced in both currents as can be seen from the waveforms during switching period shown in Fig. 11.10 (b). The switching ripple in the input current is 120mA at 3.3A peak value which is only 3.6% and ripple in the output current is 400mA at 8A peak value which is 5% at output power level of 200W. Both switching ripple currents are residual ripple currents and proportional to their peak currents [65]. Therefore, the percentage of the switching ripple currents in both inductors, relative to their peak values, is constant.

In Fig. 11.11, the line voltage and input current waveforms are plotted for different output power levels of 150W, 100W and 50W. In all three cases the input current is indeed proportional to line voltage and in phase, and zero input and output switching current ripple are preserved. For the output power level of 50W (25% of the full power) the input current leads the line voltage for a small angle of 6.3^o as a consequence of the energy transferring capacitor which is designed for the full power. This phase difference produces displacement factor $cos\varphi = .994$, which is acceptable. Comparing the waveforms from Fig. 11.11 (b) and Fig. 11.8 (b), the switching ripple component is 10 times smaller when IM is used instead of separate inductors even though the same effective inductance L_1 is

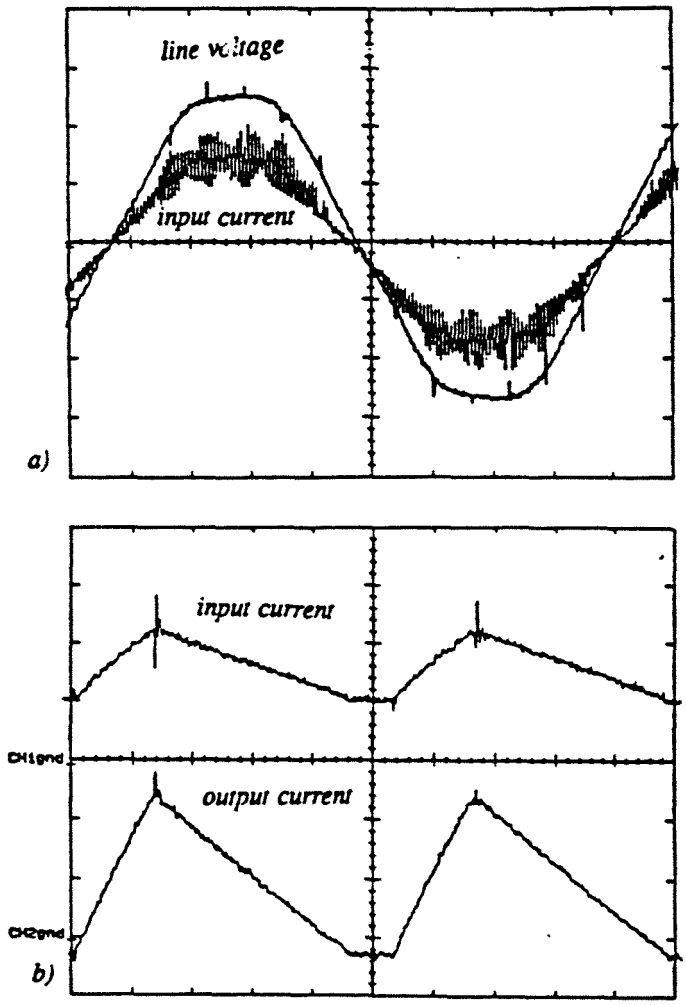


Figure 11.8: Waveforms obtained in 100W automatic current shaper based on the Ćuk converter: a) input current (1A/div.), and line voltage (50V/div.) during a line period (time scale: 2ms/div.), and b) input current (top trace: 1A/div.) and output inductor current (bottom trace: 4A/div.) during the switching period (time scale: 5μs/div.) at the peak of the line voltage.

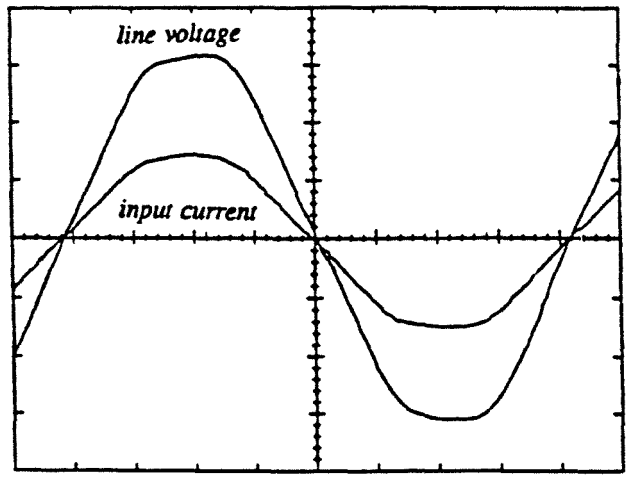


Figure 11.9: Line voltage (50V/div.) and current (2A/div.) waveforms measured at full output power of 200W. Time scale: 2ms/div.

used in both cases. Also, the switching ripple component in the output current is almost eliminated, so the improvement in the output current waveform is about two orders of magnitude.

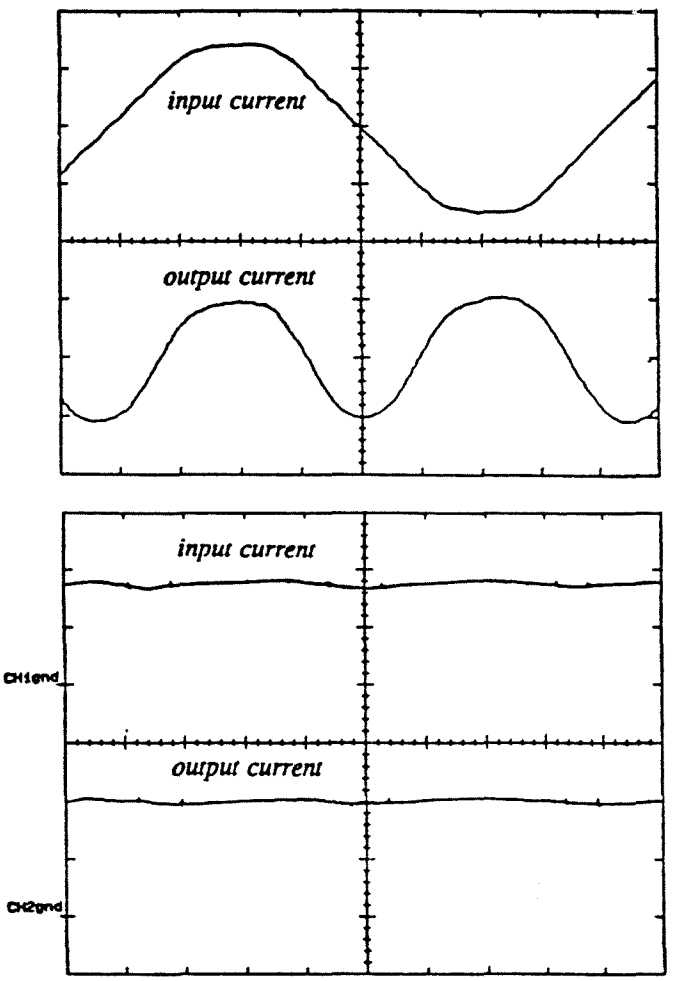


Figure 11.10: Input (top trace: 2A/div.) and output (bottom trace: 4A/div.) current waveforms at full output power of 200W: a) during a line period (time scale: 2ms/div.), b) during a switching period (time scale: 5μs/div.).

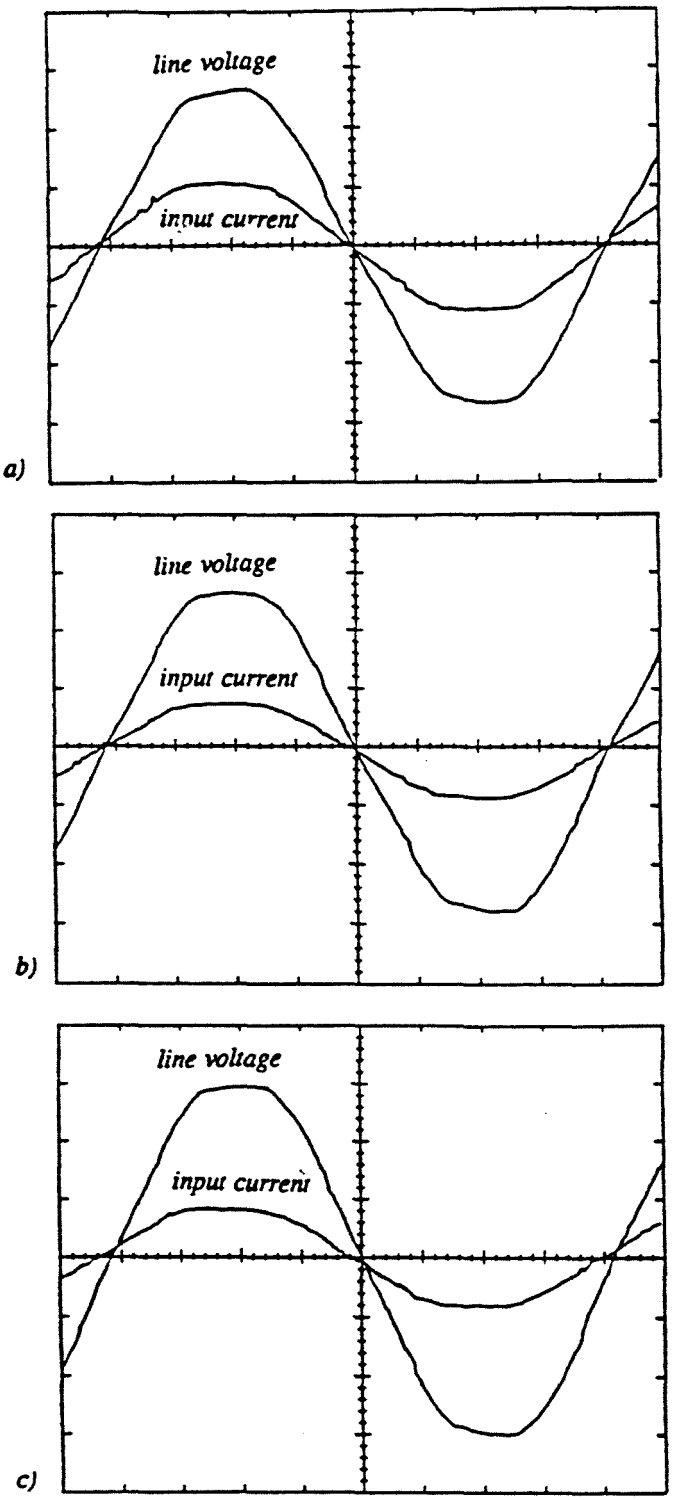


Figure 11.11: Line voltage (50V/div.) and line current waveforms measured for different output power levels. a) 150W (input current: 2A/div.); b) 100W (input current: 2A/div.), c) 50W (input current: 1A/div.). Time scale: 2ms/div.

Chapter 12

Automatic Current Shaper with Fast Output Regulation and Soft-Switching

While the solution with input current shaper followed by additional DC-to-DC converter (Fig. 10.2) is widely used for power levels above a few hundreds of watts, it is not clear whether this is also cost-effective solution for the low power levels. Since the new regulations IEC 555-2 [67] specify harmonic current limits in the line current for power levels down to 50W, it is necessary to investigate if it is possible to combine two functions together: automatic input current shaping and fast output regulation using single power stage with only one active switch as shown in Fig. 12.1.

This chapter describes a new single stage AC-to-DC converter topology which combines the functions of automatic input current shaping, fast output voltage regulation, and lossless, soft-switching [66]. This was made possible through internal energy storage and discovery of the new modes of operation, which together, effectively decoupled the input boost-like part of the Ćuk converter from its buck-like output. In Section 12.1, different modes of operation of the basic Ćuk converter are briefly reviewed, and two new modes of operation are discovered. They are caused by the presence of the rectifier in series with the source. DC analysis and criteria for different modes of operation are outlined in Section 12.2. Fast output regulation and sizing of the components are explained in Section 12.3. Soft-switching mechanism in the Ćuk converter is explained in Section 12.5. Description of the proposed circuit and experimental results obtained on 50W-12V prototype which confirm the fast output regulation (30kHz bandwidth for 100kHz switching frequency) simultaneously with the low-harmonic line current waveforms are given in Section 12.6.

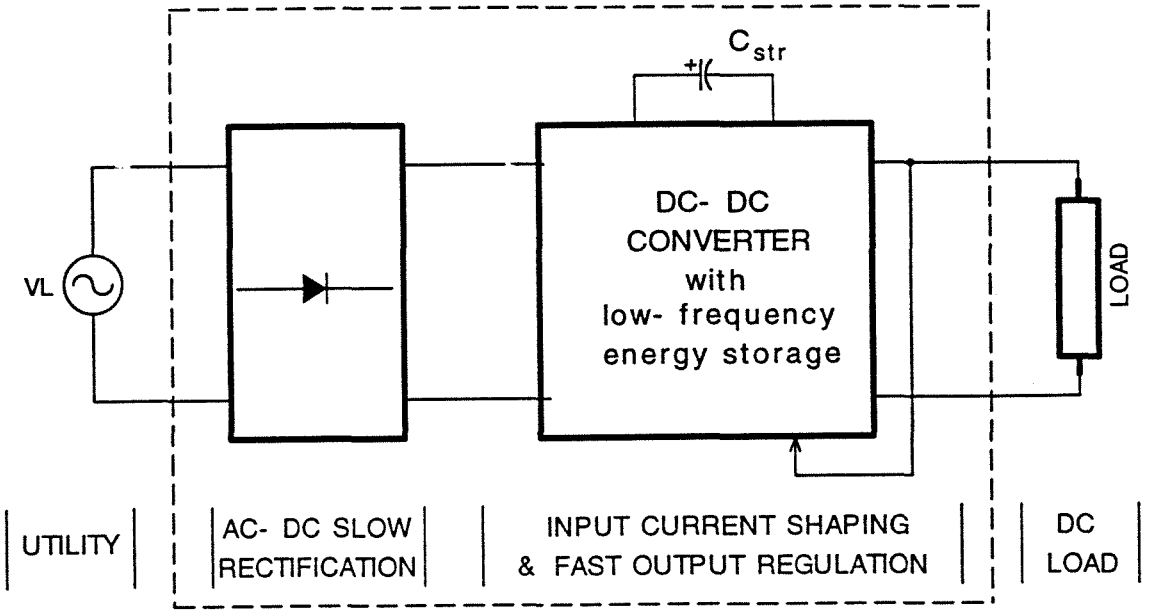


Figure 12.1: Block diagram of an automatic input current shaper with internal capacitive energy storage combined into a single power stage.

12.1 New DICM Modes in the Ćuk converter

12.1.1 Review of the DICM in the Ćuk converter

It was shown in [62] that when the Ćuk converter (Fig. 12.2) is operated in DICM both inductor currents are continuous and two different modes are possible as shown in Fig. 12.3. The onset of DICM in the Ćuk converter occurs when the diode current, which is the sum of the input and the output currents, becomes zero. This leads to the existence of the constant current level I (when the diode is turned off), and third switched network (both transistor and diode off) is created.

The presence of the constant current I in both inductors, L_1 and L_2, with opposite polarity during interval D_3T_s (Fig. 12.3) is consequence of the "coupling" between the input and the output inductors, which have the same voltage waveforms regardless of the mode of operation. Due to this, inductive energy transfer between the input and output inductors is dependent, and both inductors have the same mode of operation.

Two different discontinuous conduction modes are characterized by having unidirec-

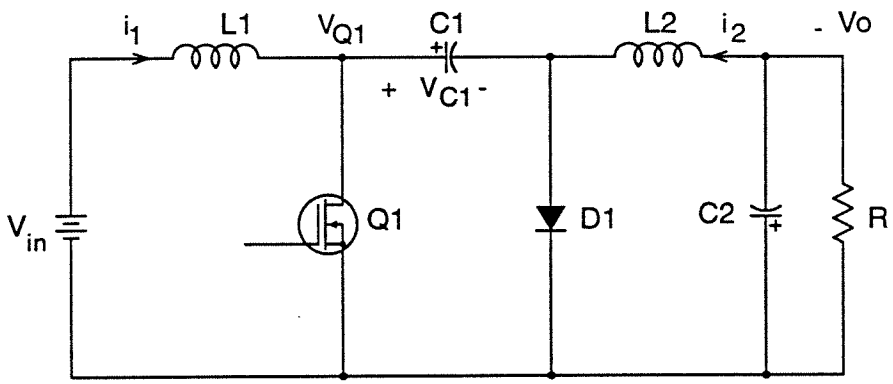


Figure 12.2: The basic Ćuk converter.

tional continuous current in one inductor and bi-directional continuous current in another inductor with their sum always non-negative. Which of these two modes will be present depends on the ratio between the input and the output inductances as shown in Fig. 12.3. DICM in the Ćuk converter (Fig. 12.2) is guaranteed when:

$$K_e \equiv \frac{2L_1 \parallel L_2}{RT_s} < (1-D)^2 \tag{12.1}$$

where, K_e is conduction parameter of the converter, D is duty ratio of the transistor $Q1$, and T_s is switching period.

The average voltage on both inductors is zero in the steady-state. Thus, the energy transferring capacitor's voltage V_{C_1} is, for any operating condition, sum of the input and the output voltages, i.e.,

$$V_{C_1} = V_{in} + V_o \tag{12.2}$$

12.1.2 Decoupling of DICM in Two New Modes

When the diode DB is added in series with the source V_{in}, as shown in Fig. 12.4, two completely new modes of operation are discovered if the basic Ćuk converter (Fig. 12.2) is designed to operate with bi-directional input inductor current (Fig. 12.3 (b)) with constraint $L_2 > ML_1$. Salient waveforms for two new modes of operation are shown

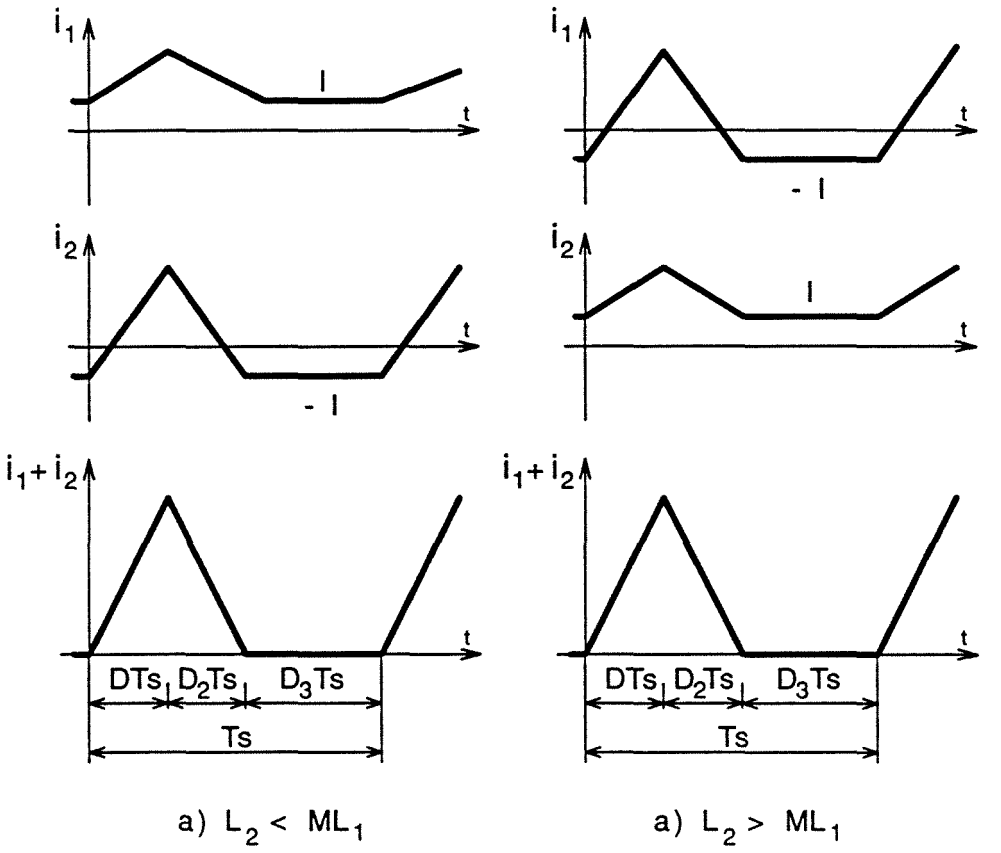


Figure 12.3: DICM in the Ćuk converter for different values of the input and the output inductances L_1, and L_2, respectively. M is DC conversion ratio defined as $M \equiv V_o/V_{in} = I_{in}/I_o$.

in Fig. 12.5. While the input inductor current is always unidirectional and discontinuous, the output inductor current is also unidirectional, but can be either discontinuous (Fig. 12.5 (a)) or continuous (Fig. 12.5 (b)). The conduction mode in the output inductor is determined by the additional constraints shown in Fig. 12.5.

By comparing waveforms from Fig. 12.5 and Fig. 12.3 (b), three main differences are evident: a) decay interval of the output current D_3T_s is always longer than decay interval of the input inductor current D_2T_s; b) the sum of the input and output inductor currents has two different slopes during decay interval and does not necessarily decays to zero, and c) the input and the output inductors do not have the same voltage waveforms. Since

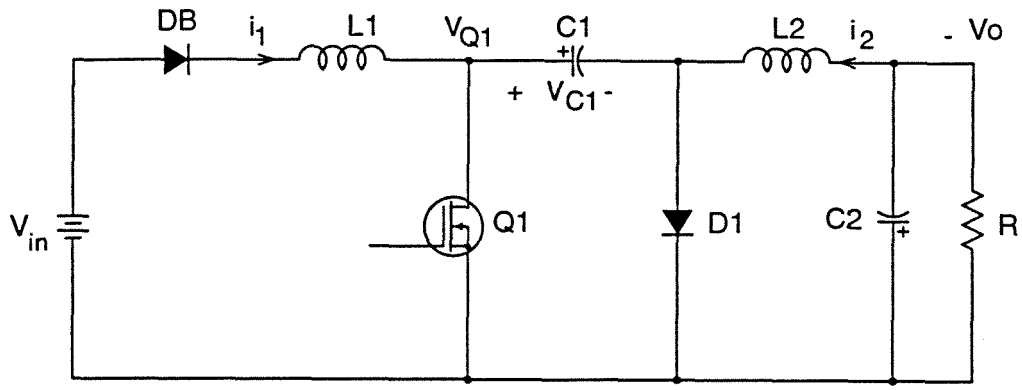


Figure 12.4: By adding the diode DB in series with the input inductor in the basic Ćuk converter, two new modes of operation are discovered.

the output diode $D1$, always conducts during the input inductor current decay interval, the very important consequence is that there is no current flowing from the input into the load during OFF interval of the transistor $Q1$. The energy transferring capacitor's voltage V_{C1}, in the converter from Fig. 12.4, is given by:

$$V_{C1} = V_{in} + V_o + v_{DB}(t) \geq V_{in} + V_o. \tag{12.3}$$

It follows from Eq. (12.3) that, the voltage V_{C1} is not necessary equal to the sum of the input and output voltages, as in the basic Ćuk converter. Equality in Eq. (12.3 holds for the case when the diode DB (Fig. 12.4) conducts during whole switching period (Fig. 12.3a). Necessary and sufficient condition for both inductors to operate in DICM (Fig. 12.5 (a)) is that the energy transferring capacitor's voltage V_{C1} is greater than the sum of the input and output voltages, i.e.,

$$V_{C1} > V_{in} + V_o. \tag{12.4}$$

The output inductor L_2 will operate in CCM (Fig. 12.5.b), whenever

$$V_{C1} > V_{in}. \tag{12.5}$$

In both cases, the voltage difference is supported by the diode DB (Fig. 12.4). Note that when the output inductor operated in CCM, voltage stresses on the transistor $Q1$

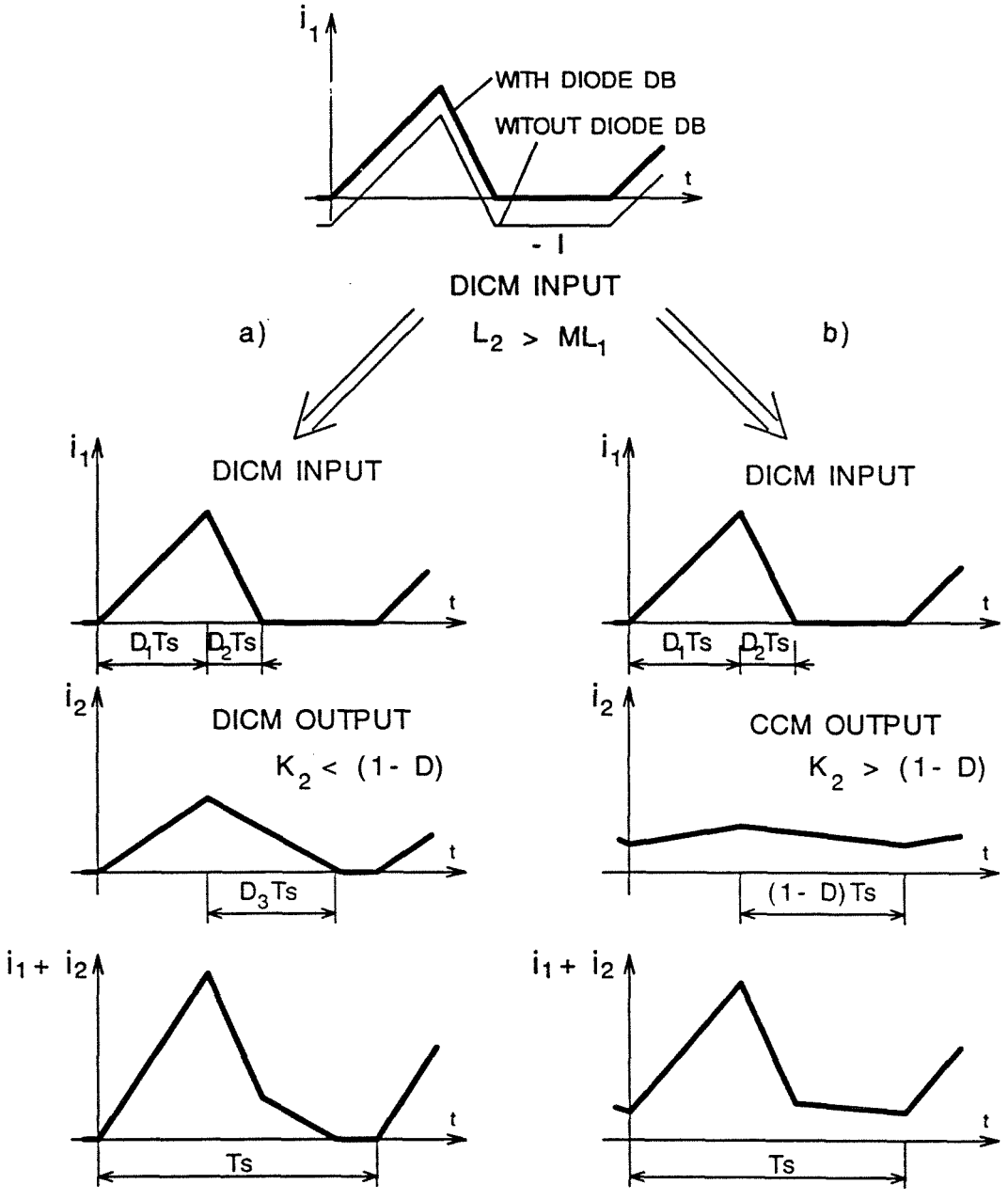


Figure 12.5: DICM in the Ćuk converter with bipolar input inductor current splits into two new modes when diode DB is added in series with the source V_{in}: a) both inductors operate in DICM, and b) while the input inductor L_1 operates in DICM, the output inductor L2 operates in CCM.

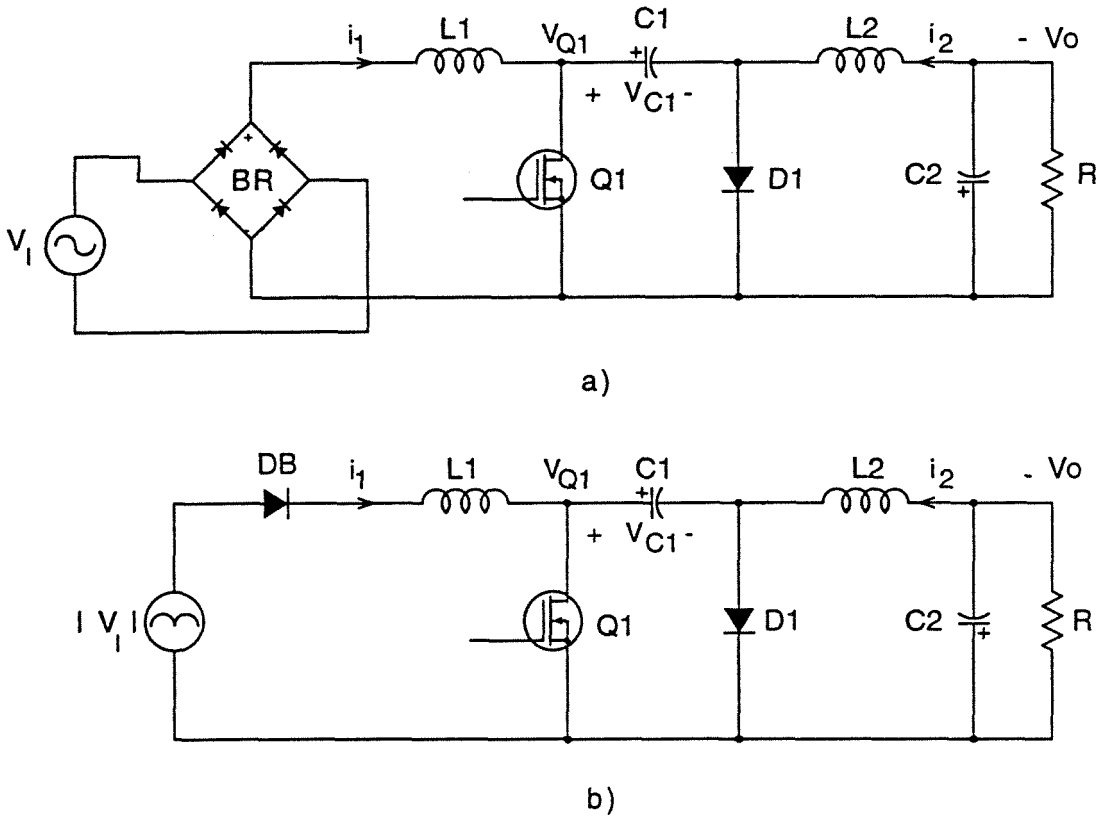


Figure 12.6: a) Input current shaper using the Ćuk converter is equivalent to b) the Ćuk converter with series input diode DB.

and diode $D1$, are lower than in the case when the output inductor is operated in DICM. In contrast, the voltage V_{C1} in the basic Ćuk converter is independent of the mode of operation and is always equal to the sum of the input and the output voltages.

In summary, by inserting the diode in series with the source, the input and the output inductors are decoupled and two new modes of operation are possible. The input and output inductors operate independently in different modes with the input inductor always operated in DICM and the output inductor operated either in DICM or CCM. The energy transferring capacitor's voltage V_{C1} is no longer uniquely determined by the input and the output voltages, and can be DC voltage, regardless of the input voltage waveform.

These two new modes of operation, shown in Fig. 12.5, are also possible when the Ćuk converter is used in input current shaping applications because of the presence of the bridge rectifier BR, as shown in Fig. 12.6. The input voltage is rectified line voltage given by:

$$|v_l| = V_l|sin(\omega_l t)| = V_l|sin\theta|. \tag{12.6}$$

Therefore, the same constraints apply on the inductors and energy transferring capacitor, when DC voltage source V_{in} in Fig. 12.4 is replaced with amplitude of the line voltage V_l in Fig. 12.6 (b). What makes these two modes of operation desirable is possibility of internal low-frequency energy storage in the energy transferring capacitor C_1. Namely, according to the above analysis, the voltage V_{C1} can be DC voltage even when the input voltage is time varying, rectified line voltage, and there will be no low-frequency current flowing from the input into the load during any portion of the switching period. This allows that output filter components, inductor L_2 and capacitor C_2, are high-frequency components. The new decoupled DICM modes now offer an attractive possibility: DICM mode of boost-like input stage can be operated as an automatic current shaper with constant duty ratio as analyzed in next section.

12.2 DC Analysis

DC analysis of the automatic current shaper from Fig. 12.6 is performed here under assumption that all switches are ideal, and the energy storage capacitor's voltage V_{C1} and output voltage V_o are DC with negligible low-frequency ripple component at twice the line frequency. The input current is calculated in Section 12.2.2. Two different modes, shown in Fig. 12.5, are considered separately. Definitions for the conversion ratios of the input and the output stage as well as overall conversion ratio of the current shaper from Fig. 12.6 are given below:

$$M_1 \equiv \frac{V_{C1}}{V_l} \tag{12.7}$$

$$M_2 \equiv \frac{V_o}{V_{C1}} \tag{12.8}$$

$$M \equiv \frac{V_o}{V_l} = M_1 M_2. \tag{12.9}$$

12.2.1 Input Current Waveform

The input inductor current averaged over a switching period (Fig. 12.5) is given by:

$$< i_1(\theta) >= \frac{|v_l(\theta)|}{2L_1} d^2 T_s [1 + \frac{d_2(\theta)}{d}] = \frac{|v_l(\theta)|}{R_{em}} \frac{|sin\theta|}{|sin\theta| - M} \tag{12.10}$$

where,

$$R_{em} = \frac{2L_1}{T_s d^2} \tag{12.11}$$

is emulated resistance of the shaper. When duty ratio and switching frequency are kept constant, the input current will, according to Eq. (10.8), follow the input voltage. The quality of the input current will depend on the conversion ratio M_1. This is the same result as for the DCM boost shaper described in Section 10.4.1. The only difference is that conversion ratio of the DCM boost shaper, M, is replaced with the conversion ratio M_1 defined in Eq. 12.7. Notice that both conversion ratios are defined as the ratio of the energy storage capacitor's voltage and the amplitude of the line voltage. In case of the boost shaper the energy storage capacitor is connected across the load while in the shaper from Fig. 12.6 there is an energy transferring capacitor.

Therefore, power factor PF, and total harmonic distortion THD, are the same as for DCM boost shaper (Fig. 10.9).

12.2.2 Input Inductor in DICM and Output Inductor in CCM

Salient waveforms for this mode of operation are given in Fig. 12.5 (b). It can be shown that conversion ratios defined in Eqs. (12.7)-(12.9) can be written as:

$$M_1^{DCM} = 1 + \frac{D}{D_2} = \frac{1 + \sqrt{1 + \frac{2}{K_1}}}{2}. \tag{12.12}$$

$$M_2^{CCM} = D \tag{12.13}$$

$$M = \frac{1 + \sqrt{1 + \frac{2}{K_1}}}{2} D \tag{12.14}$$

where,

$$K_1 = \frac{2L_1}{RT_s} \tag{12.15}$$

$$K_2 = \frac{2L_2}{RT_s} \tag{12.16}$$

are conduction parameters of the input inductor L_1, and the output inductor L_2, respectively. The super script in Eqs. (12.12) and (12.13) denotes the mode of operation of the input and the output part of the converter, respectively. The current shaper from Fig. 12.6 will operate in this mode of operation if the following inequalities are satisfied:

$$K_1 < \frac{(1-D)^2}{D} \tag{12.17}$$

$$K_2 > (1-D) \tag{12.18}$$

$$L_2 > 2ML_1. \tag{12.19}$$

By comparing results given by Eqs. (12.12)-(12.16), and in in Eqs. (12.17)-(12.18) with those obtained in [62], one can see that the shaper from Fig. 12.6 has the same DC characteristics as the cascade connection of DICM boost shaper and CCM buck converter, operated at the same duty ratio D. This is also the same result obtained in the three-switched network (3SN) Ćuk converter [69] when both active switches operated at the same duty ratio D. This should not be surprising because the diode DB, in series with input voltage, decouples the input boost-like part of the Ćuk converter from its buck-like output, so they can operate independently in DICM and CCM, respectively, under constraints (12.17)-(12.19). Note, however, that the 3SN Ćuk converter (Fig. 12.7 (b)) has already decoupled modes regardless of relative values of input and output inductors leading to elimination of the constraint (12.19).

The following important conclusions can be obtained from the above analysis:

1. Automatic current shaper using the Ćuk converter with internal energy storage (Fig. 12.6) has the same properties as the automatic boost current shaper followed by the buck converter operated in CCM.

2. Input current waveform quality depends on the energy storage capacitor's voltage $V_{C_{str}}$, and thus on the transistor's voltage stress.

3. Only a small duty ratio variation is required to regulate the output voltage against the load variations since the output buck-like stage is operated in CCM.

4. The energy storage capacitor's voltage is load dependent and cannot be controlled by varying duty ratio D.

5. By varying the switching frequency it is possible to regulate the energy storage capacitor's voltage $V_{C_{str}}$ without affecting the output voltage.

12.2.3 Both Inductors in DICM

Salient waveforms for this mode of operation are shown in Fig. 12.5 (a). The output buck-like part of the Ćuk converter will operate in DICM if:

$$K_2 < (1 - D). \tag{12.20}$$

Corresponding expressions for the conversion ratios defined in Eqs. (12.7)-(12.9) are:

$$M_1^{DCM} = 1 + \frac{D}{D_2} = \frac{1 + \sqrt{1 + \frac{D^2}{K_1}(1 + \sqrt{1 + \frac{4K_2}{D^2}})^2}}{2} \tag{12.21}$$

$$M_2^{DCM} = \frac{D}{D + D_3} = \frac{2}{1 + \sqrt{1 + \frac{4K_2}{D^2}}} \tag{12.22}$$

$$M = \frac{D(D + D_2)}{D_2(D + D_3)} = \frac{1 + \sqrt{1 + \frac{D^2}{K_1}(1 + \sqrt{1 + \frac{4K_2}{D^2}})^2}}{1 + \sqrt{1 + \frac{4K_2}{D^2}}}. \tag{12.23}$$

Again, the same result as for cascaded DICM boost shaper with DICM buck converter, or the 3SN Ćuk converter are obtained. In contrast to the mode of operation described in Section 12.2.2, where the conversion ratio M_1 was independent of duty ratio, in this mode of operation the energy storage capacitor's voltage V_{C1} and therefore, M_1 both depend on duty ratio D. This can be seen from Eqs. (12.21)-(12.23). When the load resistance R is increased, M_2 and M_1 are also increased, so in order to regulate the output voltage the duty ratio must be decreased.

The above result suggests that it could be possible, by the proper design, to regulate output voltage and keep minimum variation in the energy storage capacitor's voltage only by varying duty ratio at constant switching frequency. Even though this could be advantageous, large wide range of the load variations demands for large variation in duty ratio, which will affect input current quality. Another disadvantage of operating the output stage in DCM is that the low-frequency current can flow into the load the third interval, D_3T_s, when both transistor and diode are off. Therefore, it is still better, in practice, to operate the output buck-like stage always in CCM.

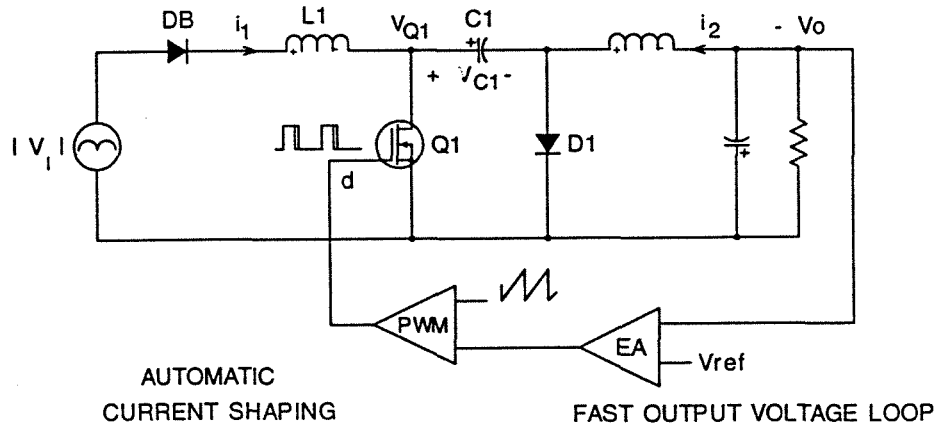
12.3 Fast Output Regulation and Automatic Current Shaping

The main feature of the current shaper with internal low-frequency energy storage shown in Fig 12.7 (a) is that fast output regulation and automatic input current shaping can be obtained simultaneously by simple duty ratio control. This feature can be explained by using a 3SN Ćuk converter [69] shown in Fig. 12.7 (b) which is equivalent to the current shaper of Fig 12.7 (a) as verified by DC analysis of Section 12.2.

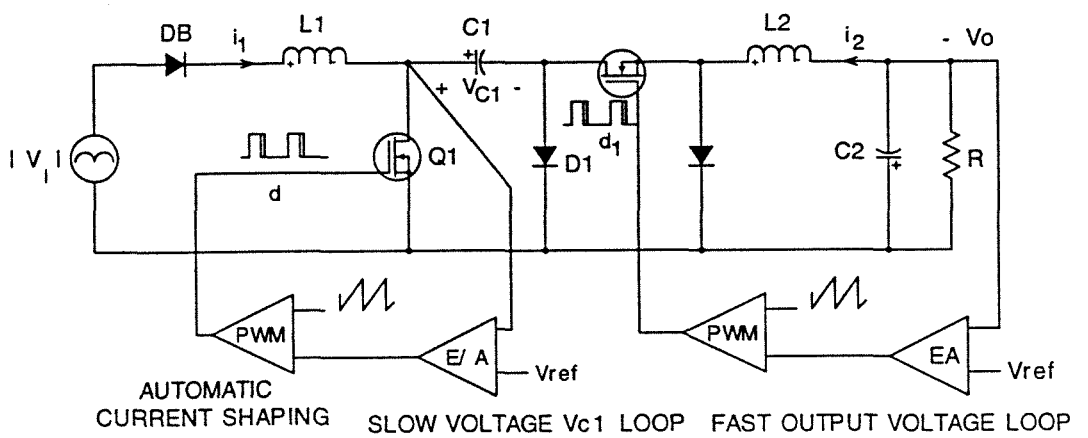
The addition of the transistor $Q2$ and diode $D2$ (Fig. 12.7 (b)) to the basic converter (Fig. 12.7 (a)) leads to the 3SN Ćuk converter, which provides another control input to the circuit [69]. The main advantage to the availability of the second control input becomes apparent in AC-to-DC applications where input current and output voltage need to be controlled independently. As shown in Fig. 12.7 (b), there are two separate control circuits which independently regulate two voltages: a) the energy storage capacitor's voltage V_{C1} by varying duty ratio d of the transistors $Q1$, and b) the output voltage V_o by varying duty ratio d_1 of the transistor $Q2$.

The slow regulation of the voltage V_{C1} is necessary in order to keep duty ratio d of the transistor $Q1$ constant during the line period and to provide the input current shaping automatically. Therefore, small variation of duty ratio d is present during the line period. On the other hand, by having an energy storage capacitor large enough to attenuate low-frequency ripple, the constant DC voltage source is provided to the CCM output buck stage. Variation in duty ratio d_1 of the transistor $Q2$, is therefore also small. Furthermore, if the output stage operated in CCM, variation in duty ratio d_1 is even smaller, and is required only to compensate voltage drop in parasitic resistances. If the output stage operated in DICM, duty ratio variation is significant for wide range of the load change. Therefore, it is preferable to operate the output stage always in CCM in order to keep duty ratio variation small, and simplify design of the output voltage feedback loop. Note that this will be automatically provided in the Soft-switching extension of the Ćuk converter described in the next section.

Since the variations in both duty ratios (d and d_1) are small, then both transistors ($Q1$ and $Q2$) can be driven at the same duty ratio, without significant degradation either in quality of the input current waveform or fast output regulation. Under this condition,



a)



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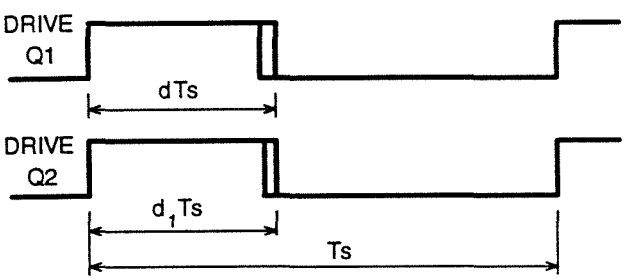

c)

Figure 12.7: Fast output regulation in: a) automatic current shaper with internal energy storage, can be explained by b) 3SN automatic current shaper, and c) the drive signal waveforms for two transistors.

the same feature of the shaper from Fig. 12.7 will be preserved when the transistor $Q2$ is shorted. By shorting the transistor $Q2$, the diode $D2$ is connected in parallel with diode $D1$, so the 3SN Ćuk shaper reduces to the Ćuk current shaper with internal energy storage as in Fig 12.7 (a). In addition to having a single active switch ($Q1$), and diode $D1$, the shaper from Fig 12.7 (a) needs only one control circuit.

12.4 Sizing of the Reactances

In the proposed shaper with internal energy storage (Fig 12.7 (a)), the only low-frequency component is the energy transferring capacitor C_{str}. All other reactances are high-frequency components. The input inductor L_1, is designed to operate always in DICM, while the output inductor L_2, is designed either to operate in DICM or CCM as described in Section 12.2. With proper design, there will be no low-frequency current flowing from the input into the load, and, therefore, the output capacitor C_2 is also high frequency component designed to suppress only the switching current ripple.

Size of the low-frequency energy storage capacitor plays an important role in overall size of the utility-to-DC interface circuit. The capacitive energy storage is efficient in terms of energy density when capacitor voltage is relatively high. Very often, in practice, to satisfy hold-up requirement for power supply, the large amount of energy must be stored in order to provide power to the load during utility power outages. This means that starting from an initial voltage V_o, the capacitor must store enough energy to maintain the output voltage above a specified minimum voltage, $V_{o,min}$, after the line voltage has been absent for a specified time t_H, often one or two full cycles of the line frequency.

In the isolated version of the shaper (Fig. 12.11), there are two additional reactances which need to be sized properly. When the magnetizing inductance L_m of the isolation transformer is infinitely large (ideal transformer), the secondary side energy transferring capacitor C_B appears in series with the energy storage capacitor C_{str}, and consequently must be a large low-frequency component, otherwise large low-frequency voltage ripple will be present at the load. On the other hand, if the magnetizing inductance of the transformer is small, high-frequency component, then the secondary side capacitor C_B can also be a small, high-frequency component as in a DC-to-DC converter.

This can be explained by considering distribution of the low-frequency current (at twice the line frequency) through the converter. Since the output voltage is constant DC, and the output filter L_2C_2 is high-frequency filter, there is no low-frequency current in the output stage of the converter. Furthermore, since the voltage on the secondary side energy storage capacitor, C_B, equals the DC output voltage, V_o, it also does not not have low-frequency current, unless it is a large low-frequency component. Therefore, low-frequency charging current of the primary side energy storage capacitor, C_{str}, must be somehow cancelled so the net current flowing into the capacitor C_B will be zero.

This can be done with proper design of the magnetizing inductance as follows. The low-frequency charging current produces low-frequency voltage ripple on the energy storage capacitor C_{str}, which laggs 90^o with respect to its current. This low-frequency voltage ripple produces low-frequency current in the magnetizing inductance which laggs 90^o in respect to the voltage. Therefore, low-frequency current in the magnetizing inductance is -180^o shifted with respect to the capacitor C_{str} charging current with magnitude inversely proportional to impedance of the magnetizing inductance at low-frequency. The magnetizing inductance is therefore, designed such that magnitude of its low-frequency current is equal to the magnitude of the capacitor C_{str} charging current. Under this condition, sum of these two currents, which is the current of the secondary side energy transferring capacitor C_B will be zero, and the capacitor C_B can indeed be small high-frequency component.

Since the low-frequency voltage ripple on the capacitor C_{str} is in practice a few percent of the DC value, the magnetizing inductance is a high-frequency component. It should be pointed out that by having the capacitors C_{str} and C_B interchanged, so that primary side energy transferring capacitor is small and secondary side capacitor is large, fast output regulation as well as overload, and short circuit protection will be lost. The reason for this is that the load is not any more connected to the energy storage capacitor by the active switch, but rather through the magnetizing inductance of the transformer..

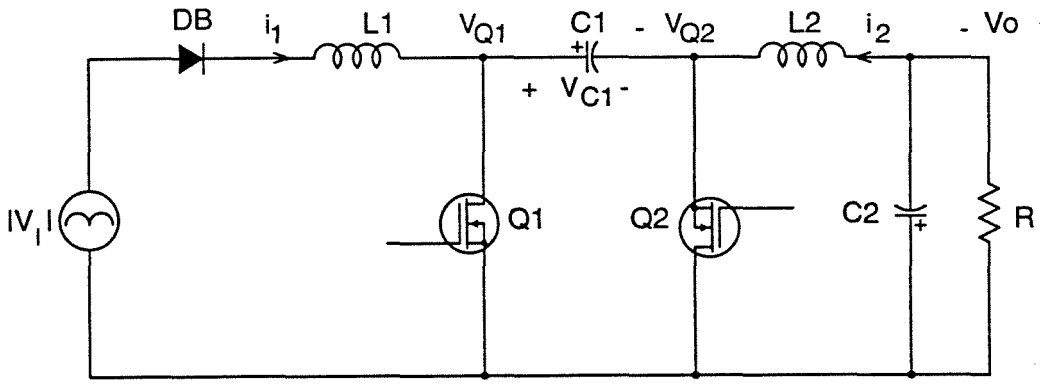

Figure 12.8: Soft-switching in the Ćuk converter is obtained by replacing the output diode with the MOSFET transistor Q2.

12.5 Zero-Voltage Switching

The power stage of the soft-switching PWM Ćuk converter is shown in Fig 12.8. In order to obtain zero voltage switching at constant switching frequency, the rectifier diode $D1$ in the circuit from Fig. 12.6 is replaced with the MOSFET $Q2$. Loss-less, soft-switching of both transistors is provided by discharging the capacitances across the MOSFET before the transistor is turned on, and charging the capacitor across the opposite MOSFET after it was turned off by the resonant circuit.

While one transition is inherently provided by the sum of the inductor currents, normally unipolar, another transition requires negative current source to oppose the positive currents through the MOSFETs. The simplest solution is to design already existing inductor such that its current will be bi-directional with the ripple amplitude greater than twice the DC load current for all operating conditions of interest as described in [25]. Therefore, one resonant component is output inductor and other two are capacitors across the MOSFETs. This technique is used in automatic current shaper with internal energy storage shown in Fig 12.8, and is described next.

The soft-switching mechanism in the Ćuk converter from Fig. 12.8 is very similar to the soft-switching mechanism in the buck converter described in Section 3.3.1. The main

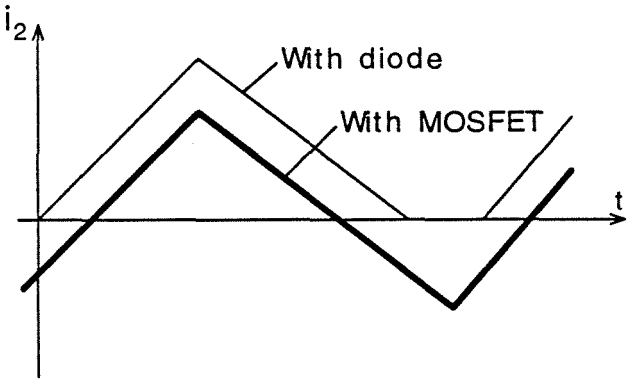

Figure 12.9: When the output diode $D1$ in the basic Ćuk converter is replaced with the MOSFET $Q2$, the discontinuous output inductor current becomes continuous and bi-directional.

difference is that in the soft-switching Ćuk converter both inductor currents take place in soft-transition instead of only the output inductor current like in the buck converter.

When the output diode $D1$ in the Ćuk converter of Fig. 12.6, designed for discontinuous output inductor current (Fig. 12.5a), is replaced with MOSFET $Q2$ as shown in Fig. 12.7, different mode of operation is obtained. The output inductor current being discontinuous and non-negative in the presence of the diode $D2$ (dashed line), now is continuous and can be negative due to the current bi-directional MOSFET (solid line) as depicted in Fig 12.9. Since the output buck stage operates in CCM, DC analysis given in Section 12.2.2 is still valid. It should be noticed that, while in the basic Ćuk converter of Fig. 12.2 the input current can also be bipolar, this is not possible in the presence of the diode DB in series with the input inductor (Fig. 12.6).

Soft-transition in MOSFETs, $Q1$ and $Q2$, occurs during the time intervals when both MOSFETs are OFF, and charge between their capacitors is exchanged in the resonant fashion. This allows the lossless, zero voltage turn on and turn off of the MOSFETs. In Fig. 12.10, waveforms of the sum of the input and output inductor currents is shown together with ac equivalent circuits of the converter from Fig 12.8 during two transition intervals. Proper design requires that the sum of the inductor currents is positive during

one transition interval, t_{t_1}, and negative during another transition interval, t_{t_2}.

Duration of the transition intervals is assumed to be short compared to a switching period, so that inductor currents remain constant during these intervals. Due to this, both inductors are replaced by the constant DC current sources in the ac equivalent circuits in Fig 12.10 (b)-(c). The equivalent circuits are obtained by replacing each MOSFET with composite switch, consisting of an ideal switch, anti parallel diode and capacitor across them, and by shorting all DC voltage sources, including energy transferring capacitor C_1. The capacitors across the switches are during transition intervals effectively connected in parallel, which corresponds to their simultaneous charging and discharging with the sum of the inductor currents.

FIRST TRANSITION INTERVAL - t_{t_1}

The first transition interval, t_{t_1}, is initiated by opening the switch $S1$, and corresponding equivalent circuit together with switch voltage waveforms is shown in Fig 12.10 (b). Both inductor currents are positive, and their sum, $I_{1p} + I_{2p}$, splits between two capacitors C_{S1} and C_{S2}. The capacitor C_{S1}, previously discharged to zero level, is charging and voltage on the switch $S1$ rises linearly toward positive value as shown by dashed line. At the same time, the capacitor C_{S2}, previously charged to positive voltage V_{C1} (DC voltage on the energy storage capacitor C_1), is discharging and voltage on the switch $S2$ decreases linearly following dashed line until it reaches zero level. At that moment, the diode D_{S2} starts to conduct and clamps voltage on the switch $S2$ to zero while voltage on switch $S1$ is clamped at V_{C1}, as shown by the solid line. Since the voltage on the switch $S2$ is clamped to zero level, it can now be turned-on with no switching losses, which completes the first transition interval. After this, converter behavior is the same as in parent PWM converter.

SECOND TRANSITION INTERVAL - t_{t_2}

The second transition interval, t_{t_2}, starts by opening the switch S2. The output inductor current is negative, and as a consequence of that the sum of the input and the output inductor currents is also negative as shown in Fig 12.10 (a). The corresponding equivalent circuit and voltage waveforms on the switches are shown in Fig 12.10 (c). The change of the current polarity provides opposite charge exchange between the capacitors,

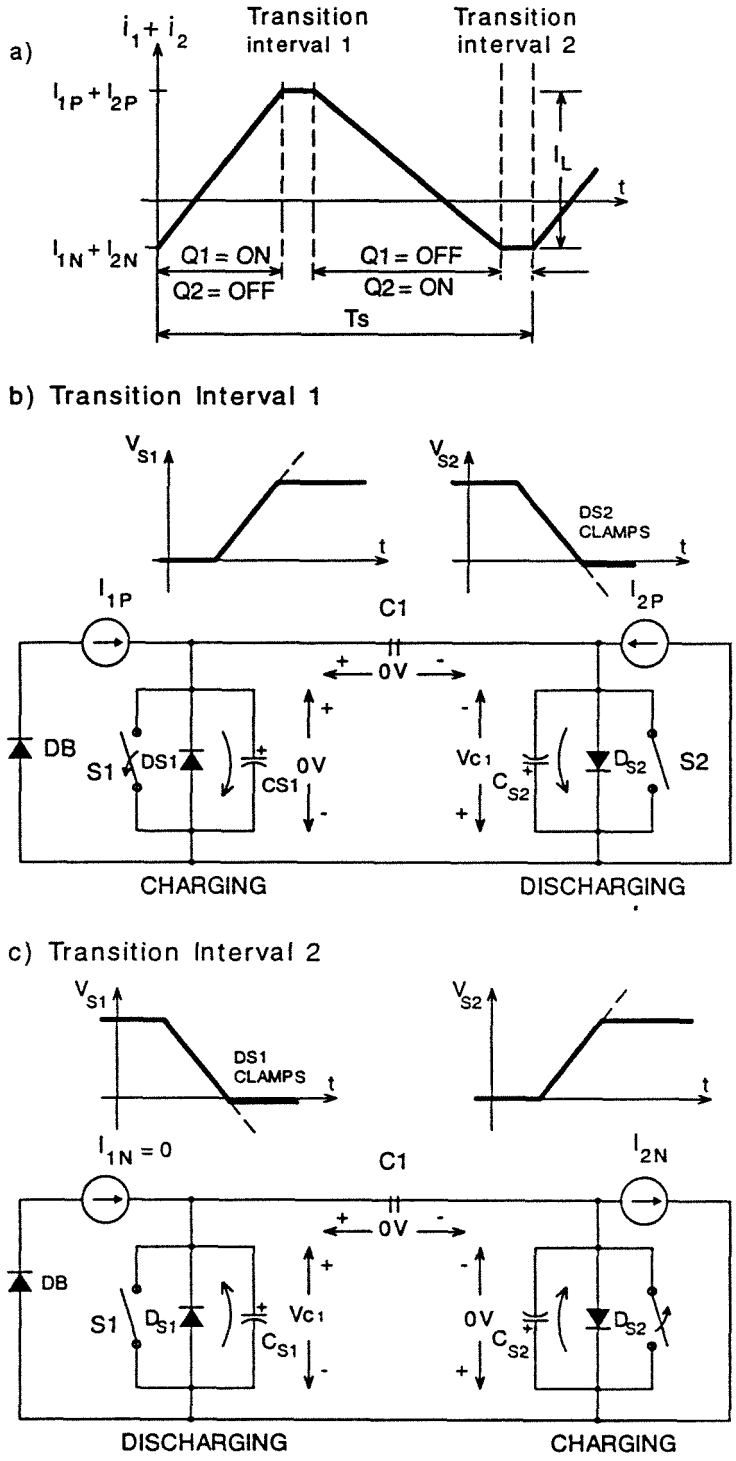

Figure 12.10: Soft-switching provided by a) bi-directional current source, is explained using equivalent circuits for two transition intervals b) t_{t_1} and c) t_{t_2}.

but now with negative current $I_{1n} + I_{2n}$. The capacitor C_{S2}, previously discharged to zero, is now charging linearly toward the positive voltage following the dashed line, and the capacitor C_{S1}, previously charged to positive voltage V_{C1}, is discharging linearly until it reaches zero level. At that moment, the diode D_{S1} starts to conduct and clamps voltage on the switch $S1$ to zero while voltage on switch $S2$ is clamped at V_{C1}, as shown by the solid lines. The switch $S1$ can now be turned on in a lossless manner, which completes the second transition interval t_{t_2}, and the converter has the same behavior as the parent PWM converter.

Due to different current levels, the transition intervals are unequal, with t_{t_1} always longer than t_{t_2}. In the automatic current shaper from Fig. 12.8 the input inductor current is always zero during second transition interval t_{t_2}, so only the negative output inductor current $-I_{2n}$ exists.

12.6 Experimental Results

In this section experimental results obtained on a 50W, 12V prototype, operated from the line voltage (80Vac-130Vac) are presented. Schematic of the automatic current shaper with fast output regulation and soft-switching is shown in Fig. 12.11. Description of the circuit is given in Section 12.6.1 and experimental waveforms and measurements are summarized in Section 12.6.2.

12.6.1 Description of the Circuit

POWER STAGE

Line voltage is rectified with slow full-bridge rectifier BR, followed by the high-frequency EMI filter, and fast diode DB. Fast diode DB is added in series with the full-bridge rectifier diodes, with EMI filter between, in order to provide proper mode of operation of the converter, and to allow that bridge rectifier diodes carry only the low-frequency current and therefore can be slow and inexpensive.

The rest of the power stage is the soft-switching PWM Ćuk converter with isolation transformer TR. The input inductor, L_1, is designed to operate always in DICM, according to analysis in Section 12.2, while the output inductor is designed to provide

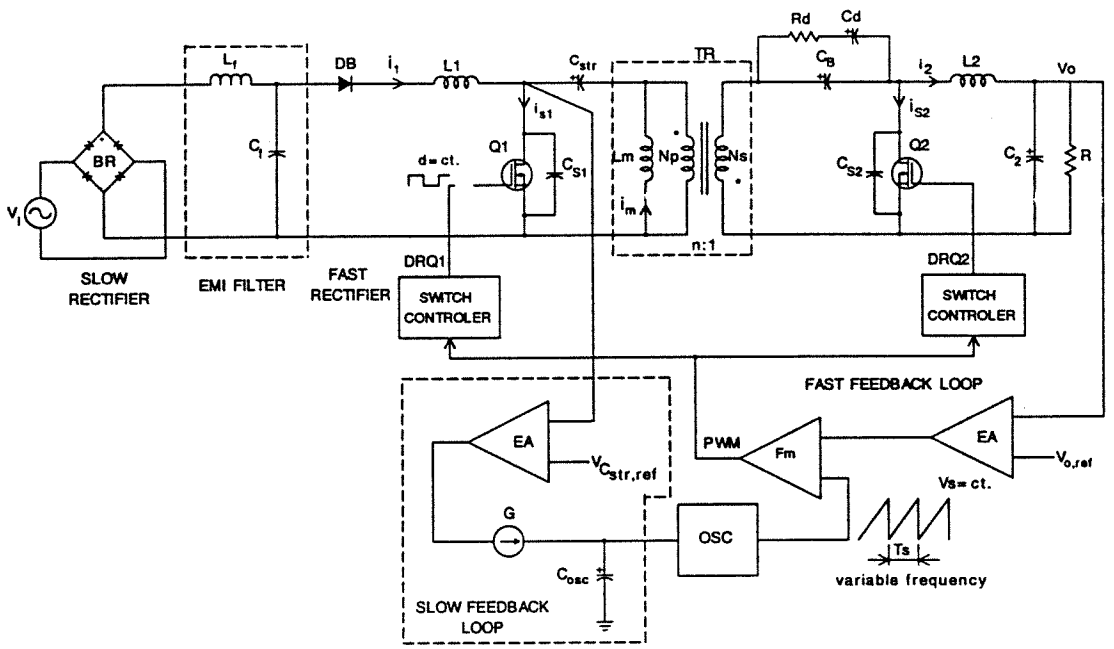

Figure 12.11: Automatic current shaper with fast output regulation, soft-switching, and galvanic isolation.

soft-switching of the MOSFETs $Q1$ and Q_2 as described in Section 12.5. Isolation transformer is designed in the same way as in DC-to-DC converter with low leakage inductance and without gap. Energy storage capacitor, C_{str}, is on the primary side of the transformer, and is sized to satisfy hold-up time requirement of 20ms. The secondary side energy transferring capacitor, C_B, is a small high frequency component as explained in Section 12.4. The output filter, L_2C_2, is a high-frequency filter, and the output capacitor is designed to bypass output inductor high-frequency currents flowing into the load. Primary side MOSFET, $Q1$, is high voltage transistor, while the MOSFET Q_2, on the secondary side, is low voltage, low ON resistance transistor. An additional damping network, R_dC_d, is added across the energy transferring capacitor C_B in order to improve converter dynamics.

CONTROL CIRCUIT

The control circuit is realized with an inexpensive PWM, duty ratio programming IC, and two switch controller circuits. The output voltage is compared to the reference voltage V_{ref} and amplified in the error amplifier EA which generates control signal V_c

on its output. This control signal is compared to the sawtooth waveform in the PWM modulator, which generates train of pulses fed into the switch controllers. The switch controllers contain delay circuits needed for proper gating, and driver circuitry for the MOSFETs.

An additional circuitry in the dashed box denoted as FM control is used for the slow regulation of the energy storage capacitor's voltage, particularly at light loads. It consists of the error amplifier AMP and voltage controlled current source G. Drain-to-source voltage of the $Q1$ is averaged and compared to the reference $V_{C1_{ref}}$, and amplified by the low bandwidth (a few Hz) error amplifier AMP, which controls the charging current of the oscillator capacitor C_{osc}.

Components used in the prototype are listed below:

$BR = VH248$, $DB = MUR850$, $Q1 = MTM750$, $Q_2 = SMP60N06$, $L_f = 125\mu H$, $L_1 = 105\mu H$, $L_m = 1.5mH$, $L_2 = 6\mu H$, $C_f = 1.25\mu F$, $C_{str} = 100\mu F$, $C_B = 50\mu F$, $C_o = 470\mu F$, $C_d = 100\mu F$, $R_d = .75\Omega$, $n = 10$.

12.6.2 Experimental Waveforms

Waveforms of the input and the output inductor currents, together with drain-to source voltages of the MOSFETs $Q1$ and Q_2, are shown during the switching period at the peak of the line voltage in Fig 12.12 . As can be seen from the waveforms, shaper operated in the proper mode of operation. The input inductor current is discontinuous (Fig 12.12 (a)) as predicted in Fig. 12.5 (a), and the output inductor current is bi-directional (Fig 12.12 (b)) with magnitude large enough to provide soft-switching of both MOSFETs, $Q1$ and Q_2, (Fig. 12.11 (c)-(d)), as explained in Section 12.5 (Fig 12.10).

Line voltage and line current waveforms, obtained at minimum line voltage (80Vac) and full load condition (50W) are shown in Fig 12.13. The line current follows the line voltage with small distortion. The measured THD was 12%, which is 3% higher than predicted 9% for $M_1 = 2.5$ from Fig. 10.9. The increased THD is primarily due to low-frequency duty ratio modulation introduced by the fast output voltage regulation loop, and partially by the modulation of the transition intervals. Measurements of the THD is repeated at high line voltage 130Vac, and slightly smaller discrepancy between

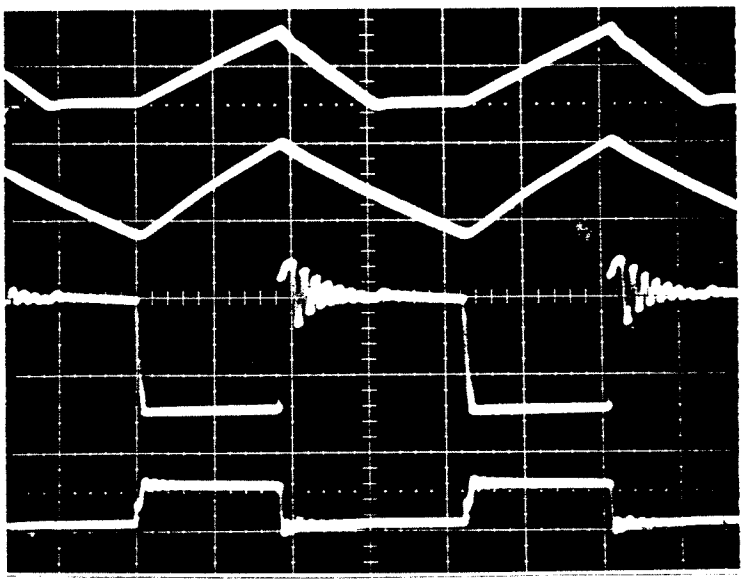

Figure 12.12: Waveforms in the novel shaper during a switching period at peak of the line voltage: a) input inductor current (top trace: 2A/div.), b) output inductor current (trace 2: 10A/div.), and voltage on MOSFETs: c) $Q1$ (trace 3: 200V/div.), and d) Q_2 (bottom trace: 50V/div.). Time scale: 1μs/div.

measured 15% and predicted 13% ($M_1 = 2$) was observed. This can be explained with reduced low-frequency voltage ripple on the energy storage capacitor, and consequently smaller duty ratio modulation.

Loop gain of the shaper measured at nominal line voltage and full load is shown in Fig 12.14. Crossover frequency is around 30 kHz with phase margin 70^o and gain margin 10dB. The resultant loop gain has single pole characteristics with flat phase up to almost half the switching frequency.

The output voltage response to step-load change of 10% to 100% is shown in Fig. 12.15. Fast and stable response with settling time 60μs, and overshoot and undershoot in the output voltage less than 1% of the nominal DC value 12V confirmed high bandwidth performance of the prototype.

DC gain of the error amplifier AMP, in the FM circuit, was chosen such that sensed voltage was regulated between 260VDC and 360VDC, which allowed variation of the switching frequency in the range 150kHz-350kHz, for line voltage variation in range

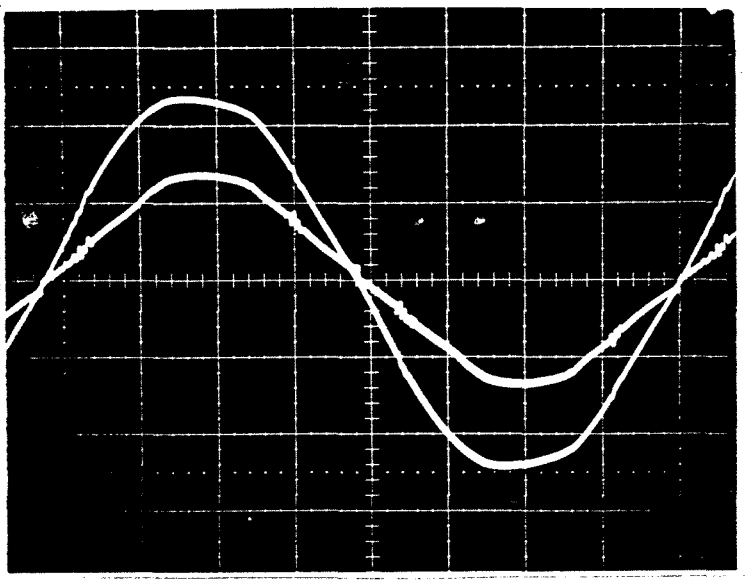

Figure 12.13: Line current (1A/div.) follows line voltage (100V/div.) automatically in the novel current shaper. Time scale: 2ms/div.

80Vac-130Vac, and no-load to full load conditions. The highest measured overall efficiency at full load, line voltage 100Vac, and switching frequency 180kHz, was 85%. The power consumption of the control circuit was measured .6W, which represented 1.2% of the maximum output power.

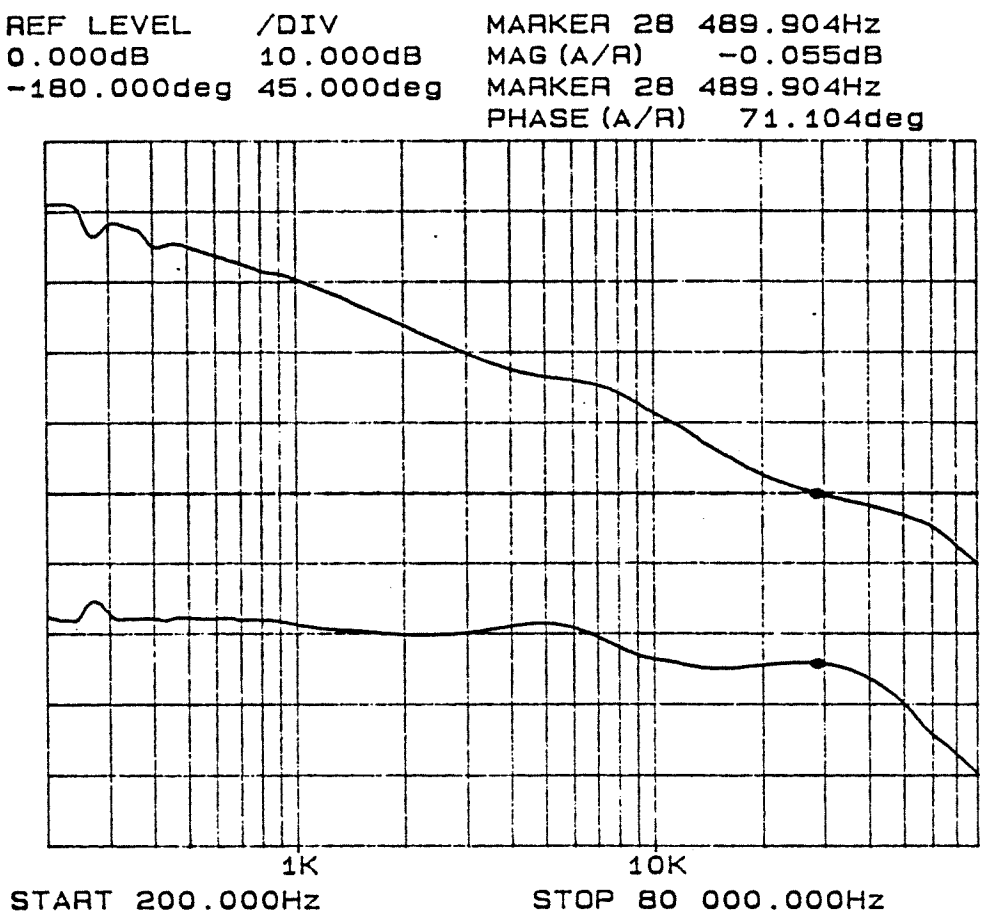

Figure 12.14: Loop gain of the automatic current shaper measured at nominal line voltage 110Vac and full load.

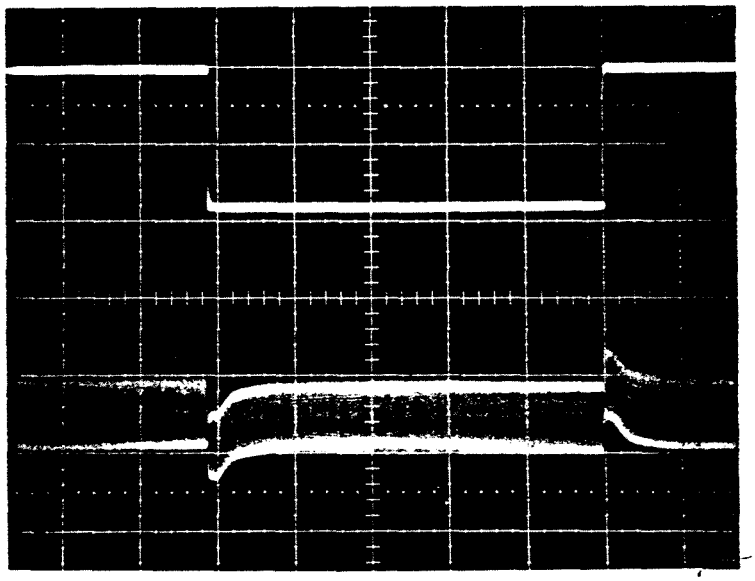

Figure 12.15: The output voltage response (bottom trace: .1V/div.) to 10% to 100% step-load variation (top trace: 2A/div.). Time scale: 500μs/div.

Chapter 13

Novel Single Stage AC-to-DC Converters Using Magamp for Input Current Shaping

In this chapter, novel single stage AC-to-DC converters with unity power factor and fast output regulation are proposed. These converters use a magamp for input current shaping, while the active switch or switches in the original converter are used for fast output regulation. The input stage of these converters operates in DICM. In addition, the input stage of the full-bridge topology can also operate in CCM.

In Section 13.1, the motivation for research into the input current shaping method with magamp is described. The principle of input current shaping with magamp is explained for the single transistor DICM shaper with internal energy storage in Section 13.2. Due to the operation of the input stage in DICM it is advantageous to have the core material for the magamp with a high saturated permeability. The saturated inductance of the magamp can be in that case used instead of the linear input inductance. The requirements for core material are given in Section 13.3. DC analysis which gives dependance of the transistor's and the magamp's duty ratios on the maximum voltage stress on the switches is given in Section 13.4. Two different control methods, voltage follower approach and multiplier approach are analyzed in Section 13.5. Different shaper topologies operating in DICM are studied in Section 13.6, while the full-bridge converter operated in CCM is studied in Section 13.7. The minimum voltage stress on the switches are obtained in both cases when the asymmetrical drives for active switches are used. Experimental results which verify principle of input current shaping with magamps are given in Section 13.8.

13.1 Problem Statement

The serious drawback of the single stage automatic current shaper with internal energy storage (ACSIS), described in Chapter 12, and the other topologies proposed in [68], is the high voltage stress on the transistor and rectifier diodes. By operating the output stage of these converters in CCM, the conversion ratio of the DICM input stage is *independent of* the transistor's duty ratio. Thus, the voltage on the energy storage capacitor and, therefore, voltage stress on the switches increase with a decrease in the load current. From the input stage conversion ratio, given by Eq. (12.12), one can see that the energy storage capacitor's voltage, $V_{C_{str}}$ (Fig. 12.6), can only be regulated in two ways: a) by varying switching frequency as suggested in [66] and b) by varying the input inductance L_1. In [68] variable frequency control is suggested only for input current shaping without voltage feedback loop for the energy storage capacitor's voltage. It is also possible to combine these two methods, but increased complexity becomes the issue since the main idea behind integration of ACSIS into a single power stage was *simplicity.*

Consider the following example as an illustration. Assume that magnitude of the rectified line voltage is in the range $120VDC-375VDC$, and the voltage $V_{C_{str}}$ is regulated at $450VDC$. Consequently, the conversion ratio of the input stage, M_1, has to vary from 1.2 to 4.5, which requires variation in controlled variable in the range 1:13 for the line voltage variations in the range 1:3.75. The situation becomes more serious when the load current varies from 0% to 100%. The controlled variable, either switching frequency or the input inductance, has to be varied in proportion with load variations. Therefore, to cover load variations from 5% to 100% and line voltage in range 1:3.75, the controlled variable must be varied in range 1:40! Such a wide dynamic range of the controlled variable is impractical when either variable frequency or variable inductance is used. If the variable frequency control is used, the converter has to operate up to one megahertz at light loads. On the other hand, the concept of variable linear inductance seems rather complex.

Assume that, somehow, the input stage of the ACSIS is controlled by the duty cycle $D_M < D$, where D is the duty ratio of the output stage. In that case the input stage

has the conversion ratio given by

$$M_1 = \frac{1+\sqrt{1+\frac{2D_M^2}{K_1}}}{2}. \tag{13.1}$$

By independent control of the input stage's duty cycle D_M, it is possible to operate ACSIS at constant switching frequency and keep voltage stress on switches at the same level as in parent DC-to-DC converter.

Automatic current shaper with internal energy storage using the Ćuk converter with additional switch $S1$ in series with the input inductor and fast diode $D1$ is shown in Fig. 13.1, together with salient waveforms. Notice that switch $S1$ and diode $D1$ form a controllable voltage bidirectional switch.

Transistor $Q1$ is driven at constant frequency and duty cycle D. The additional series switch, $S1$, is turned on with delay θ_B in respect to the transistor $Q1$ as shown in Fig. 13.1 (b). The input inductor current rises linearly during simultaneous conduction of $Q1$ and $S1$, denoted as time interval $D_M T_s$. At t=DT_s, the $Q1$ is turned off and the input inductor's current decays linearly toward zero during time interval $D_2 T_s$ as in the boost converter. In the rest of the switching period, denoted as $D_3 T_s$, the input current is zero and the switch $S1$ can be turned off. The voltage $V_{C_{str}}$ can now be regulated by controlling delay θ_B. Notice that input current shaping is preserved by adding the switch $S1$.

The natural question which arises is: Is it possible to control duty cycle of the input stage during conduction period of the transistor $Q1$ without using an additional semiconductor switch? The answer is yes, and the principle of operation of such a circuit is explained next.

13.2 Input Current Shaping with Magamp

The following assumptions are made in the analysis:

1. Input stage operates in DICM.

2. Output stage operates in CCM.

3. Voltage on the energy storage capacitance, $V_{C_{str}}$, is constant.

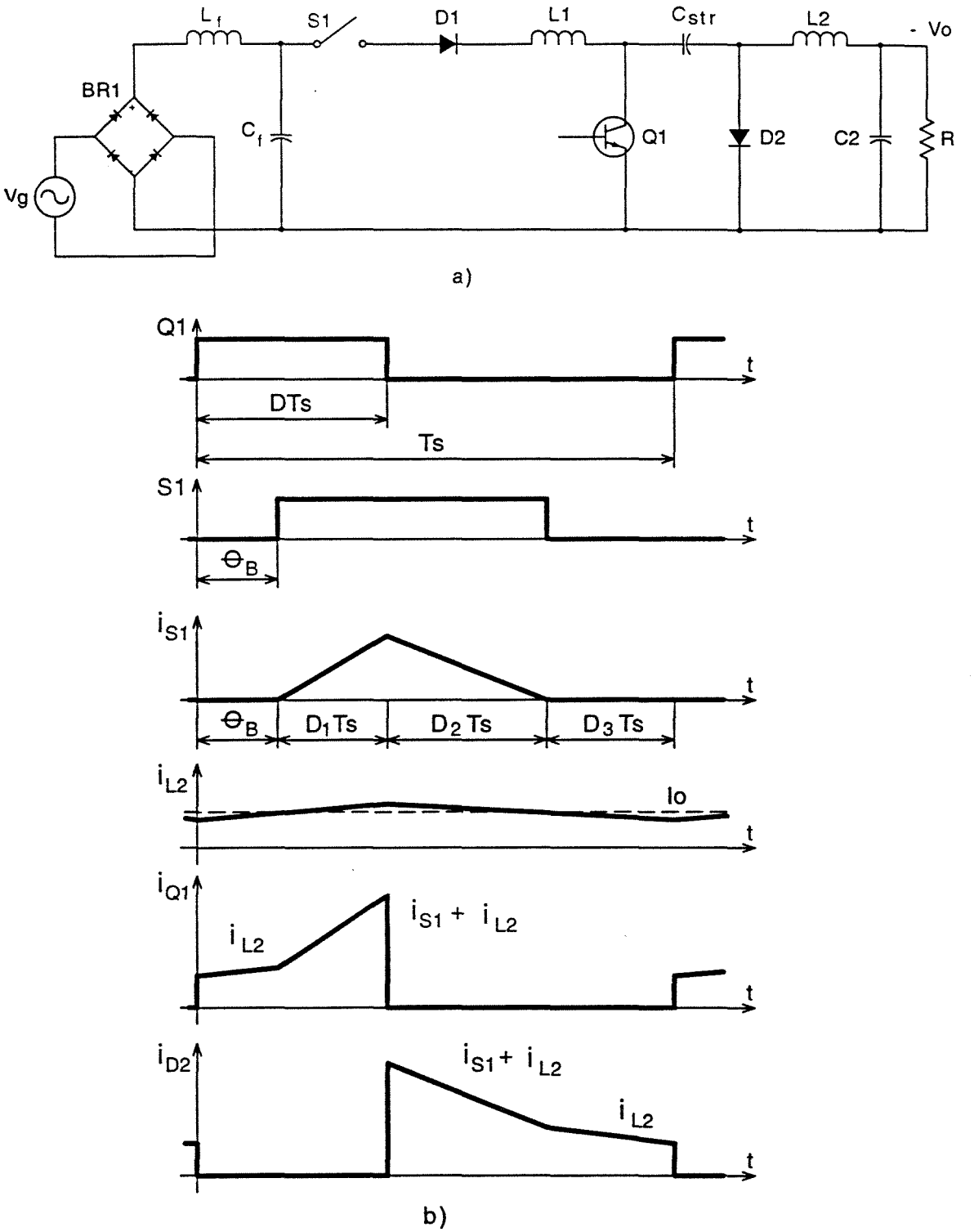

Figure 13.1: a) Automatic current shaper with internal energy storage using the Ćuk converter with additional input switch S1, and b) salient waveforms.

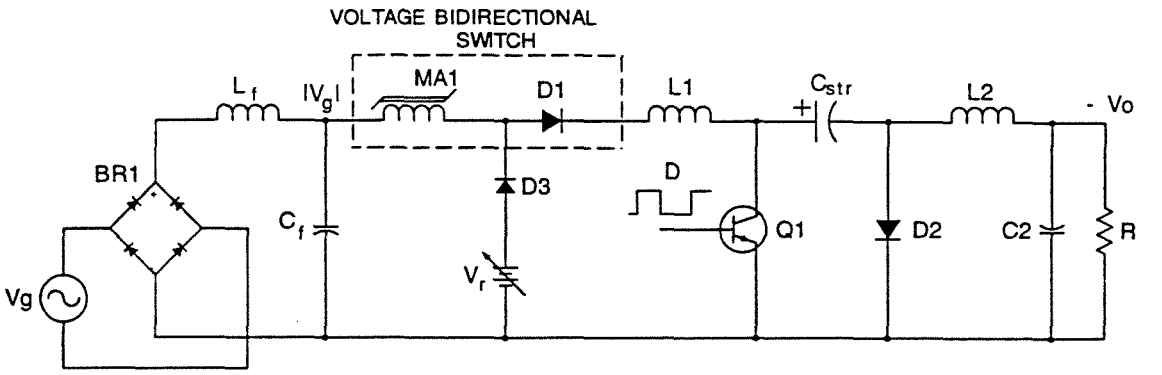

Figure 13.2: A novel single stage current shaper with internal energy storage (ACSISMA) using the magamp for input current shaping and slow regulation of the energy storage capacitor's voltage $V_{C_{str}}$. The output voltage is regulated by the transistor $Q1$.

4. Input voltage is constant during a switching period.

As a consequence of the above assumptions, it follows that the duty cycle of the transistor is constant (D=const.) regardless of the input voltage or load variations.

The practical realization of the switch $S1$ with magamp MA is shown in Fig. 13.2. The magamp MA together with diode $D1$ forms a controllable voltage bidirectional switch (as described in Chapter 2) which operates in the same manner as the ideal switch $S1$ in Fig. 13.1. Equivalent circuits for four different operating states of the circuit from Fig. 13.2 are shown in Fig. 13.3, while the salient waveforms are shown in Fig. 13.4.

During blocking state (Fig. 13.3 (a)), the magamp blocks input voltage V_g so the transistor $Q1$ only carries load current I_0 (Fig. 13.4 (d)). The magamp saturates after time θ_B (Fig. 13.3 (b)) and input current starts from zero, rising linearly during the next time interval $D_M T_s$ (Fig. 13.4 (b)).

At t=DT_s, transistor $Q1$ is turned off (Fig. 13.3 (c)), and energy previously stored in the input inductor during time $D_M T_s$ is discharged into the energy storage capacitor during time interval $D_2 T_s$. The magamp is still in saturation and the current decays linearly during this interval (Fig. 13.4 (c)). Once the input inductor current drops to zero, diode $D1$ turns off and the magamp can be reset (Fig. 13.4 (d)).

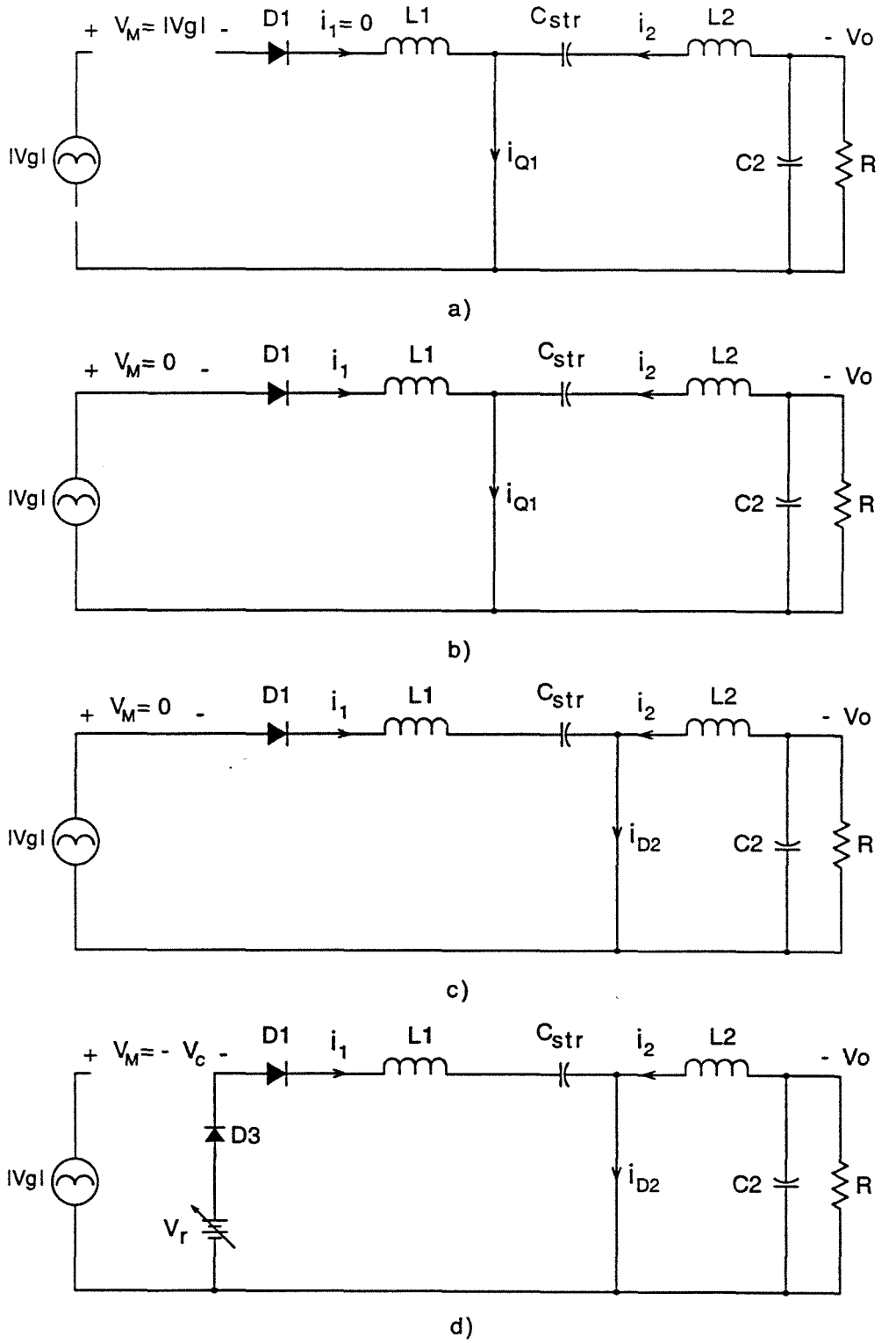

Figure 13.3: Equivalent circuits of the novel ACSISMA during four different operating states: a) magamp's blocking state, b) charging inductor state, c) discharging inductor state, and d) magamp's reset state.

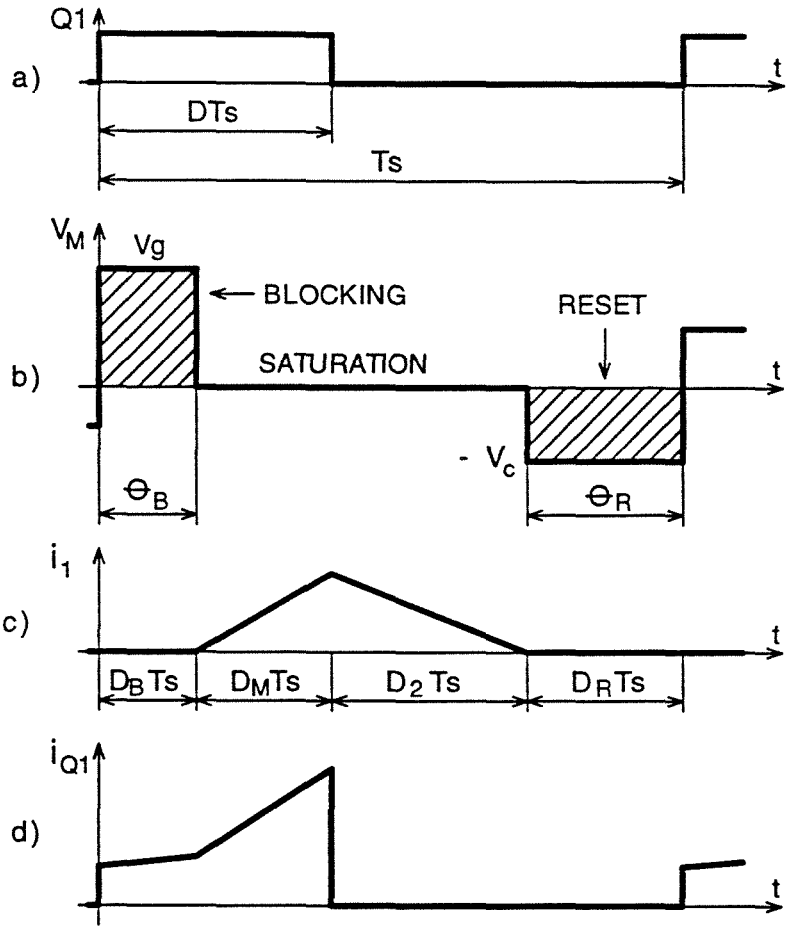

Figure 13.4: Salient waveforms in the novel ACSISMA: a) drive signal for Q1, b) voltage on the magamp, c) input current, and d) transistor current.

The blocking time θ_B, is determined by the volt-seconds stored on the magamp during the reset interval θ_R, as shown in Fig. 13.4 (b). Both voltage and current reset methods can be used for controlling the blocking time θ_B.

Therefore, it is possible to control the duty ratio of the input stage independently of the transistor's duty ratio by using the magamp in series with the input inductor. In the rest of the chapter, the proposed method is analyzed in the input current shaping applications where single stage AC-to-DC converter with harmonic-free input current and fast output regulation is of the primary interest.

13.3 Requirements for Core Material

Since the magamp $MA1$ is in series with the input inductor L_1 (Fig. 13.2), saturated inductance of magamp is useful in a current shaping application. The natural question arises immediately: Is it possible to design a magamp having a saturated inductance large enough so the input inductor L_1 can be omitted? The answer is yes, but there is a trade-off between the size of the magamp and the switching frequency, as well as a large saturated inductance and leakage current during the blocking state of the magamp.

By having core material with large saturated permeability μ_s, the linear input inductor (L_1 in Fig. 13.2) can be significantly reduced or even completely eliminated and saturated inductance of the magamp used instead, as shown in Fig. 13.5. If this is the case, then, neither a semiconductor active switch nor an additional power component have to be added to the original automatic current shaper with internal energy storage. Thus, significant improvement in the overall performance – minimized transistor and rectifier voltage stress, and improved input current quality – are obtained with the same complexity of the power stage as in the original circuit. Other advantages of using saturated inductance of the magamp instead of the linear inductor are:

a) There is no limit for the maximum current in saturated inductance as in the linear inductor.

b) Increased overload capability of the input stage.

c) Flux swing in the core is determined by the required blocking capability of the magamp and not by the current level.

d) No air gap is required in the core.

c) Lower core losses and radiated noise.

The desirable $\Lambda - I$ characteristic of the magamp used for input current shaping is shown in Fig. 13.6. Core material of the saturable inductor should have the following characteristics:

1. Square-loop characteristic.

2. High squareness.

3. High unsaturated permeability μ.

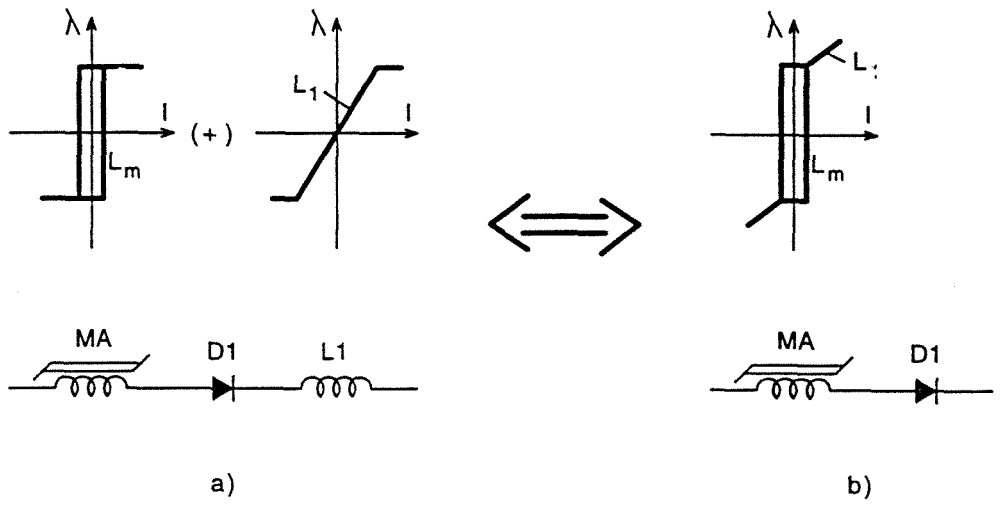

Figure 13.5: The linear input inductor L_1 could be eliminated if the magnetic core has large saturated permeability μ_s.

4. High saturated permeability μ_s.

It is impossible to satisfy all of the above requirements in a single core. The core material with the high saturated permeability μ_s has lower unsaturated permeability μ than the "ideal" square loop material. Due to this, the price which has to be paid for using core material with large μ_s is increased leakage current in the blocking state and increased reset current of magamp. The former increases required minimum load, while the latter increases losses in the control circuitry. The total effect can be quantitatively established only when a large number of parameters are included in analysis, such as core material, core geometry, number of turns, reverse-recovery characteristic of the diode in series with the magamp, switching frequency and the maximum voltage stress on transistor .

In practice, a compromise has to be made between the opposite requirements for the core material. Nevertheless, due to saturated inductance of the magamp, the size of the input inductor can be reduced, if not completely eliminated.

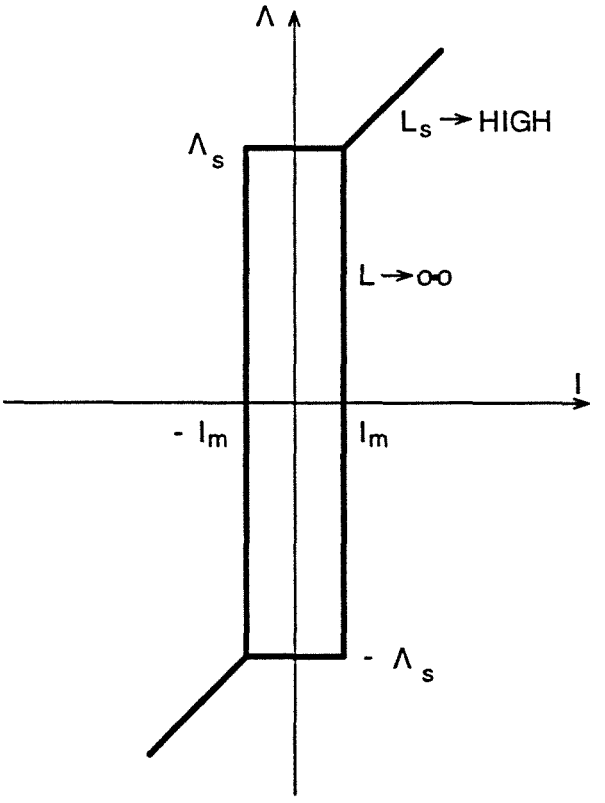

Figure 13.6: The desirable $\Lambda - I$ characteristic of the magamp used for input current shaping.

13.4 DC Analysis

In this section both the duty ratio of the transistor, D, and the duty ratio of the magamp, D_M, are calculated for the given conversion ratio of the input stage. The following assumptions are used in DC analysis of the circuit from Fig. 13.2:

1. Duty cycle of both transistor $Q1$ and magamp is constant over half of the line period, i.e., $D = ct.$ and $D_M = ct.$.

2. Voltage on the energy storage capacitor, $V_{C_{str}}$, is constant.

Let $M_{1_{min}}$ be the minimum conversion ratio of the input stage corresponding to the maximum input voltage and $M_{1_{max}}$ the maximum conversion ratio corresponding to the

minimum input voltage. They are given by

$$M_{1,min} = \frac{V_{C_{str}}}{V_{g,max}} \tag{13.2}$$

$$M_{1,max} = \frac{V_{C_{str}}}{V_{g,min}}. \tag{13.3}$$

Now, express the magamp's duty ratio D_M as a function of known parameters D, $M_{1,min}$, and $M_{1,max}$ from the expressions of the input current averaged over switching period. Input or rectified line current is given by

$$\bar{i}_g = \frac{V_g|sin\theta|D_M^2 T_s}{2L_1} \cdot \frac{M_1}{M_1 - sin\theta} \tag{13.4}$$

Even though the input current is not a pure sine-wave we can assume in the first approximation that

$$\bar{i}_g \simeq I_g sin\theta. \tag{13.5}$$

The error made by using $\sqrt{2}I_g$ as an r.m.s. value of the input current is less than 5% for $M_{1,min} > 1.4$ (for $M_1 = 1.4$, power factor $PF = .97$ and $THD = 23\%$). By substituting Eq. (13.5) into Eq. (13.4), for upper and lower limits of the input voltage, we get

$$I_{g,min} = \frac{V_{g,max} D_{M_{1,min}}^2 T_s}{2L_1} \frac{M_{1,min}}{M_{1,min} - 1} \tag{13.6}$$

$$I_{g,max} = \frac{V_{g,min} D_{M_{1,max}}^2 T_s}{2L_1} \frac{M_{1,max}}{M_{1,max} - 1} \tag{13.7}$$

where, $D_{M,max} \leq D$. Dividing Eq. (13.6 by Eq. (13.7) and solving for $D_{M,min}$, we get

$$D_M = \gamma D \sqrt{\frac{M_{1,min}}{M_{1,max}} \frac{M_{1,min} - 1}{M_{1,max} - 1}} = \kappa D \tag{13.8}$$

where,

$$\gamma = \frac{D_{M,max}}{D} \leq 1. \tag{13.9}$$

In practice, γ is usually chosen to be at minimum input voltage and 120% of the nominal load, in order to operate input stage in DICM. This approach minimizes the maximum transistor's current stress at minimum input voltage. For simplicity, it is assumed that $\gamma = 1$ at nominal load (100%) in the rest of the chapter.

Finally, we need to calculate the duty ratio D. To do this, D_2, D_B and D_R (see Fig. 13.2) are expressed as a function of D at the maximum input voltage, since $D_{M,min}$ has been already calculated in Eq. (13.8).

From the volt-second balance on the input inductor (L_1 in Fig. 13.2), it follows that

$$D_{2,max} = \frac{\kappa D}{M_{1,min} - 1}. \tag{13.10}$$

Similarly, $D_{R,min}$ can be calculated, from equality of volt-seconds stored and volt-seconds blocked by magamp, as:

$$D_{R,min} = \frac{D_B}{M_{1,min} - 1} = \frac{1 - \kappa}{M_{1,min} - 1} D. \tag{13.11}$$

By substituting Eqs. (13.10)-(13.11) into

$$D + D_{2,max} + D_{R,min} = 1 \tag{13.12}$$

and solving for D, we finally get

$$D = \frac{M_{1,min} - 1}{M_{1,min}}. \tag{13.13}$$

Equation (13.13) gives the duty ratio of transistor $Q1$ in Fig. 13.2 as a function of the input stage conversion ratio at the maximum input voltage, $M_{1,min}$, which is a known design parameter. Also, Eq. (13.13) can be used to find $M_{1,min}$ if the duty ratio D is fixed by the circuit topology, for example bridge topologies with full duty ratio on the primary side for which $D = .5$.

The minimum value of $M_{1,min}$, which determines voltage stress on the transistor $Q1$ and diodes $D1$ and $D2$, is determined by the minimum reset time θ_R required for corresponding value of $D_M T_s$. In practice, it is usual that even in DC-to-DC application, single-ended topologies have voltage stress on the transistor usually $1.5V_g$ or higher. Therefore, it is reasonable to specify $M_{1,min} = 1.5$. Moreover, with $M_{1,min} = 1.5$ and constant D_M, the power factor will theoretically be greater than .98 for the boost-like automatic current shapers (Fig. 10.9).

The preliminary design procedure, in which the transistor's duty ratio, D, and the magamp's duty ratio, $D_{M,min}$, are calculated consists of three steps which are summarized below.

Step 1. Calculate $M_{1,min}$ and $M_{1,max}$ from Eqs. (13.2) and (13.3), respectively.

Step 2. Calculate D from Eq. (13.13).

Step 3. Calculate $D_{M,min}$ from Eq. (13.8).

After these two quantities are calculated the design procedure of the converter is the same as in the original circuit without a magamp. It should be noticed that the above approach provides minimum current stress in the input stage, constant voltage on the energy storage capacitor and thus, allows optimized design of the output stage.

13.5 Control of Magamp Used for Input Current Shaping

There are two different control methods of the magamp used for input current shaping with slow regulation of $V_{C_{str}}$ (Fig. 13.2). One method is to keep the duty ratio of the magamp constant during the line period and provide input current shaping automatically as in the original circuit [66], but now with constant switching frequency and reduced voltage stress on the components. The other method is to program the input current to follow the line voltage by closing the current feedback loop (multiplier approach). This method provides unity power factor.

Before doing any analysis, it is necessary to establish what limits of the magamp have to be taken into account in this particular application – input current shaping. By operating input stage in DICM, input current starts from zero and returns to zero during a switching period. It becomes obvious that, in contrast to CCM, the saturated inductance does not reduce the effective duty ratio of the magamp when converter operates in DCM. There are still two undesirable flux reset components caused by core squareness and reverse recovery time of the series diode $D1$. The latter effect requires a rather complicated analysis and the final result depends on diode parameters as well as core material [70, 71].

For simplicity, only core squareness is considered as an undesirable reset component in the following analysis. Both automatic current shaping (constant duty ratio) and multiplier approach are discussed for input current shaping.

13.5.1 Automatic Current Shaping with Magamp

In order to provide input current shaping automatically, the duty ratio of the magamp has to be kept constant during the line period, regardless of the variations in the transistor's duty ratio. The quality of the input current should be the same as in the DCM boost shaper (Section 10.4.1).

Core squareness is taken into account through the flux $\Lambda_{sq} = \Lambda_s - \Lambda_r$ (Fig. 13.7). Both the voltage and the current reset methods are considered in this section.

VOLTAGE RESET

Referring to Fig. 13.4, the magamp's duty ratio can be expressed as:

$$D_M = D - D_B. \tag{13.14}$$

Total volt-seconds stored in the core are given by:

$$\begin{aligned} \Delta\Lambda_c &= \Lambda_{sq} + \Lambda_c \\ &= \Lambda_{sq} + V_c D_R T_s \end{aligned} \tag{13.15}$$

where, V_c is the reset voltage applied on the magamp during time $D_R T_s$ (Fig. 13.3). From equality of the volt-seconds blocked and the volt-seconds stored on the magamp, we can write

$$V_g(D - D_M) = V_r D_R T_s + \Lambda_{sq} \tag{13.16}$$

where, D_R can be expressed as:

$$D_R = (1 - D)T_s - \frac{V_g}{V_o - V_g} D_M T_s. \tag{13.17}$$

By substituting both input voltage $v_g(\theta) = V_g|sin\theta|$ and Eq. (13.17) into Eq. (13.16) and solving in $V_r(\theta)$ we get:

$$V_r(\theta) = \frac{(M_1 - |sin\theta|)(D - D_M)}{(1 - D)(M_1 - |sin\theta|) - D_M|sin\theta|} V_g|sin\theta| - \frac{\Lambda_{sq}(M_1 - |sin\theta|)}{(1 - D)(M_1 - |sin\theta|) - D_M|sin\theta|}. \tag{13.18}$$

As one can see from Eq. (13.18), the voltage reset method requires a very complicated control circuit. Having also in mind that this control method will not provide unity power factor, it is obvious that automatic current shaping with voltage reset of the magamp is not suitable for practical realization.

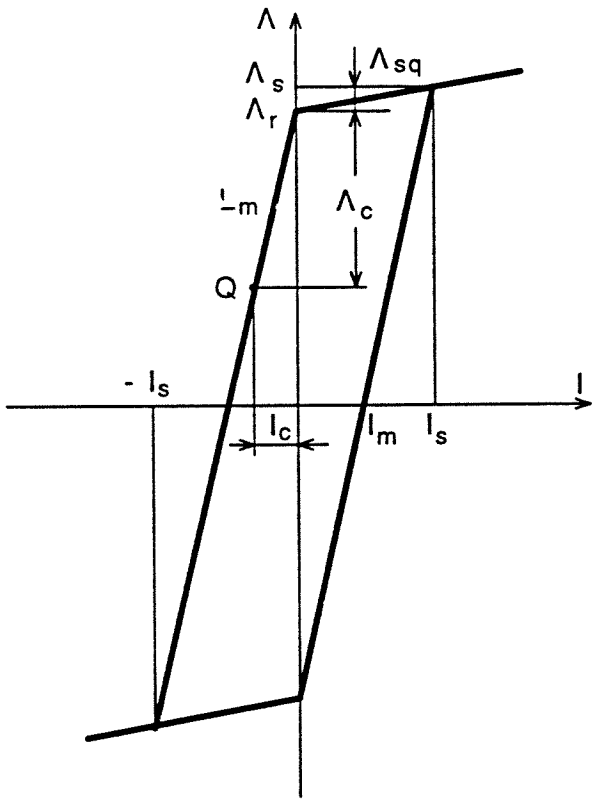

Figure 13.7: Simplified the $\Lambda - I$ characteristic of the saturable inductor used as a magamp with current reset control.

CURRENT RESET

Since the gain of the magamp with current reset depends on the unsaturated inductance, the $\Lambda - I$ characteristic needs to be specified. The second-order parameters of the core, which are not important for the basic principle of the control, are neglected in the following analysis.

The simplified $\Lambda - I$ characteristic of the saturable inductor used as magamp is shown in Fig. 13.7. It is assumed that unsaturated inductance L_m is constant and inductor runs out of saturation at $i = 0$, which corresponds to residual flux Λ_r.

The volt-seconds stored in the magamp, Λ_c, due to control or reset current, I_c, are given by:

$$\Lambda_c = L_m I_c. \tag{13.19}$$

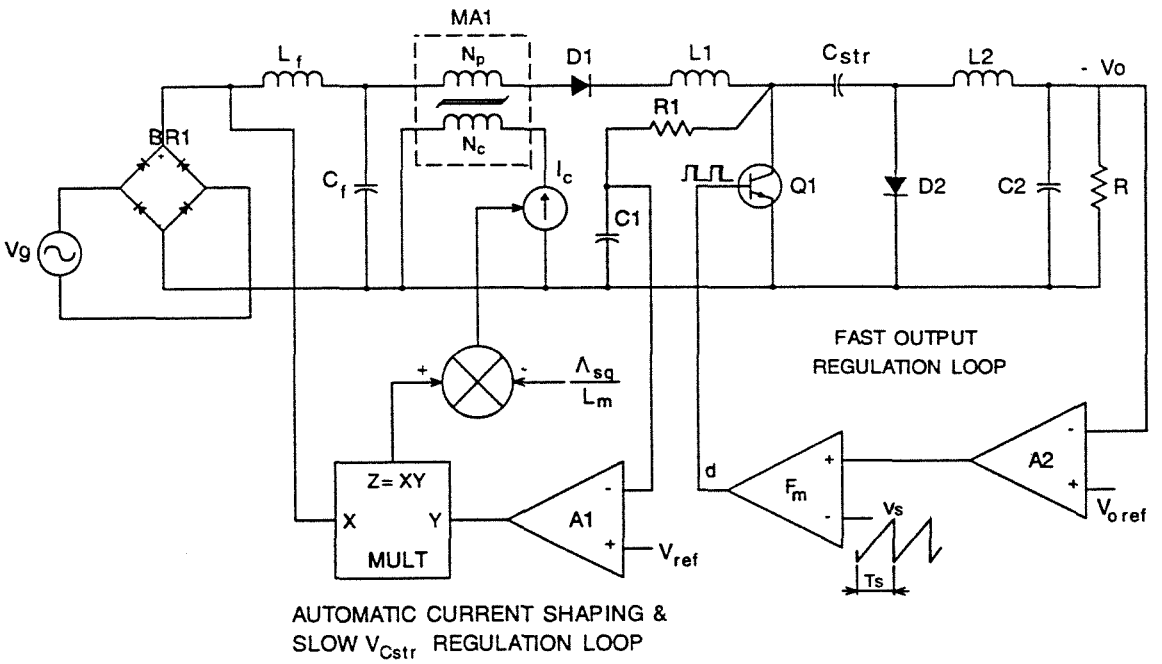

Figure 13.8: The schematic of the ACSISMA *with current reset of the magamp.*

By using the expression for Λ_c given by Eq. (13.19), instead of the one for the voltage reset in Eq. (13.16), and following the same procedure described for the voltage reset, the control current I_c, can be written as:

$$I_c(\theta) = \frac{(D - D_M)T_s}{L_m} V_g |sin\theta| - \frac{\Lambda_{sq}}{L_m}. \tag{13.20}$$

Equation (13.20) shows that the duty ratio of the magamp is constant when the control current is proportional to the rectified line voltage. The second term on the right-hand side of the Eq. (13.20), Λ_{sq}/L_m, is constant for the given core material, core geometry and number of turns. The current reset control is relatively simple and practical realization requires analog multiplication and subtractions, which can be done very easily as shown in Fig. 13.8.

Therefore, the current reset method should be used for the automatic current shaping with magamp due to a much simpler reset circuit than that required for the voltage reset method. This result shouldn't be surprising because when the current reset is used, the nonlinear dependance of the reset interval $D_R T_s$, on both line voltage and the energy storage capacitor's voltage is eliminated by the gain of the magamp L_m/T_s. Conversely,

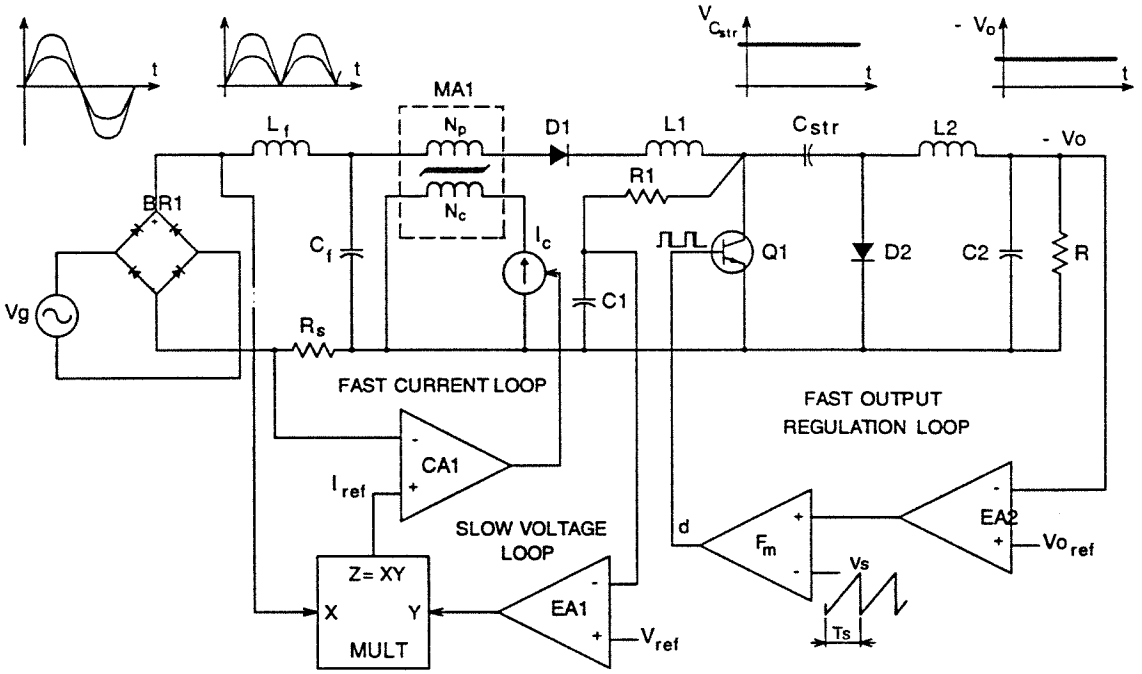

Figure 13.9: A single transistor AC-to-DC converter with unity power factor and fast output regulation. Input current shaping is provided by magamp $MA1$, while the fast output regulation is provided with transistor $Q1$.

if the voltage reset method is used, the reset interval $D_R T_s$ introduces a high degree of nonlinearity as evident from the expression for the reset voltage given by Eq. (13.18).

13.5.2 Input Current Shaping with Magamp Using Average Current Mode Control

A single stage AC-to-DC converter with a high quality input current waveform and fast output regulation employing magamp for input current shaping is shown in Fig. 13.9. The input current shaping is provided by average current mode control, while the fast output regulation is provided by a separate PWM controller. It should be mentioned that an average current mode control is mostly used for shapers operated in CCM [56], while the shaper using magamp (Fig. 13.9) is always operated in DICM.

There are two feedback loops in the control circuit for the shaper in Fig. 13.9: a) high bandwidth input current loop, and b) low bandwidth regulation loop of the energy storage capacitor's voltage, $V_{C_{str}}$. The voltage V_{cstr} is compared with reference V_{ref} in the error amplifier A_1. Output voltage of the amplifier A_1 is then multiplied with

attenuated rectified input voltage $K_1 V_g|sin\theta|$ to adjust amplitude of the reference for the input current, I_{ref}. Voltage on the current sense resistor R_s is compared with current reference in the current amplifier CA_1. The output voltage of the CA_1 controls the reset current I_c of magamp $MA1$. By varying the reset current of the magamp, the duty ratio of the input stage is adjusted such that input current is proportional to the rectified line voltage.

Even though the control circuit from Fig. 13.9 looks the same as that from Fig. 10.6, there is a major difference in the switch controller. Namely, in the conventional shaper with average current mode control (Fig. 10.6), the output of the current amplifier CA_1 is compared with sawtooth waveform in pulse-width modulator, F_m, which modulates the duty ratio of the transistor $Q1$. In contrast to that, the magamp's duty ratio, D_M, is modulated by the current I_c, controlled by the current amplifier CA_1. In addition, instead of having a driver with a high pulse current capability for driving the transistor $Q1$ (usually the high voltage MOSFET) in the conventional shaper, magamp is driven by the low current source.

Therefore, the magamp in the shaper of Fig. 13.9 combines both PWM modulator and switch into a single power component.

Notice that in the shaper of Fig. 13.9, only the input current can be sensed since the transistor's current is the sum of the input inductor current and load current.

The duty ratio of the magamp, $d_M(\theta)$, required for unity power factor, is found from Eq. 13.4, by substituting its left-hand side with expression for desired input current waveform, $I_g|sin\theta|$, and solving for $d_M(\theta)$. The result is given by

$$d_M(\theta) = \sqrt{K_{em}\frac{M - |sin\theta|}{M}} \tag{13.21}$$

where, $K_{em} = 2L_1 f_s / R_{em}$ is a dimensionless conduction parameter of the shaper, and R_{em} is the emulated resistance of the shaper.

Both voltage and current reset methods can be used, but the current reset is preferable because of the much simpler reset circuit.

In summary, the control circuit for the shaper using magamp is simpler than one used in the conventional shaper with input current feedback loop. The main disadvantage of the circuit from Fig. 13.9 is discontinuous input current which requires additional

input filter, L_fC_f. On the other hand, possibility of eliminating the input inductor and achieving unity power factor with reduced voltage stress on the switches, makes the proposed method a good choice as a cost effective solution, particularly for power levels up to a few hundred watts. The maximum power level is limited by the high current stress when converter operated in DCM, and *not* by the magamp.

13.6 Shapers with Discontinuous Input Current

In this section, single-stage input current shapers with internal energy storage and input stage operated in DICM are considered. They can be divided, according to the original DC-to-DC converters, into two main groups :

a) Single transistor shapers.

b) Bridge topology shapers.

The principle of operation and DC analysis, described in Section 13.2 and Section 13.4 respectively, are the same for both of these topologies.

13.6.1 Shapers Using a Single Transistor Converter

The proposed input current shaping method with magamp can be used in all DCM single transistor shapers with internal capacitive energy storage simply by either adding magamp in series with the input inductor or replacing the input inductor with magamp. Both constant duty ratio and an average current mode control, described in Section 13.5, can be used. Some of the possible topologies are shown in Figs. 13.10 through 13.12.

It should be noticed that shapers from Figs. 13.11 and 13.12 have three main differences compared to the shapers in Figs. 13.1 and 13.10:

a) The input stage is flyback-like instead of the boost-like.

b) Reduced in rush current at least an order of magnitude.

c) Two additional diodes are required.

13.6.2 Bridge Topology Shapers

Input current shaping with the magamp can also be provided if the magamp and fast diode are connected in series with input inductor in the half-bridge (Fig. 13.13 (a)) and

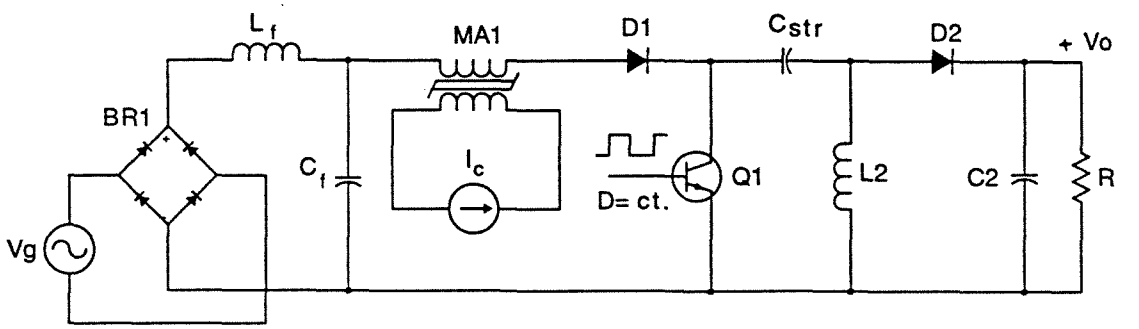

Figure 13.10: Current shaping with magamp in the Sepic topology with internal energy storage.

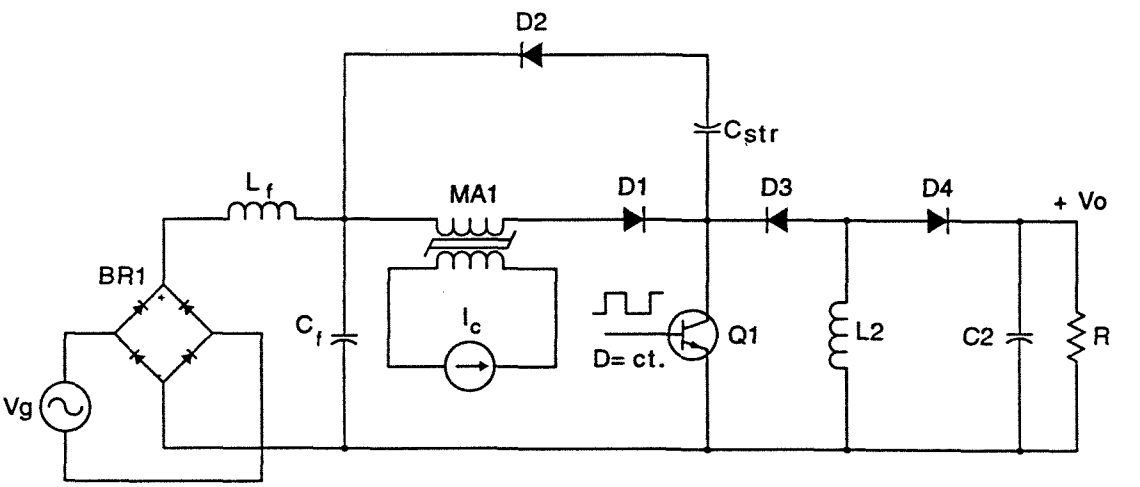

Figure 13.11: Current shaper with magamp in a single transistor converter with "quadratic" conversion ratio.

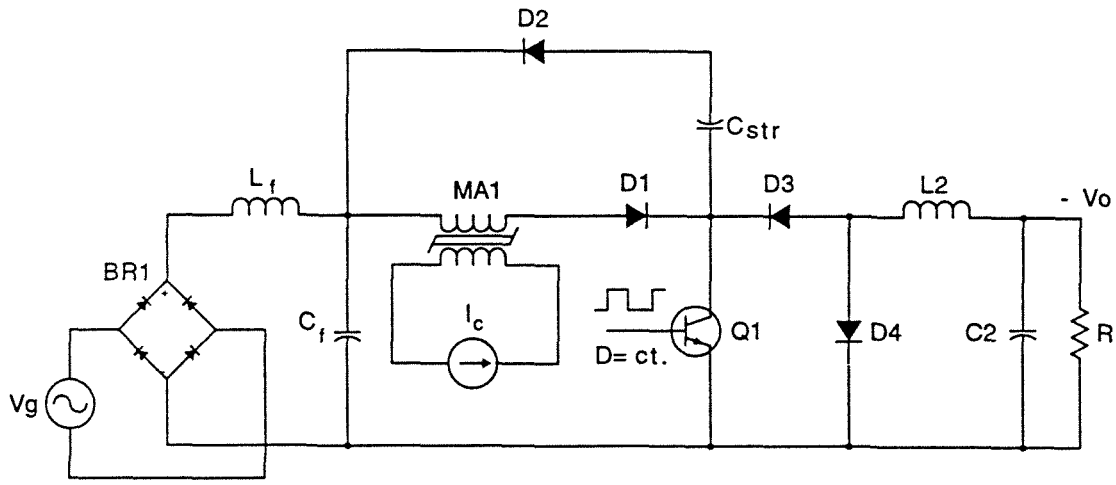

Figure 13.12: Current shaper with magamp in a single transistor converter with "quadratic" conversion ratio.

the full-bridge (Fig. 13.13 (b)) converter topology. The input stage of these converters is operated in $DICM$. Even though only one leg of the full-bridge can be used for input current shaping, it is advantageous to use both legs and have a magamp, fast diode, and input inductor for each leg of the bridge. Both current stress of the switches and input current switching ripple are reduced (Figs. 13.14-13.16) compared to either a single transistor or the half-bridge shaper.

By proper design of the converter, it is possible to maintain continuous input current in the full bridge shaper since two legs of the bridge operate out of phase. Due to this, only the capacitive input filter could be required (C_f in Fig. 13.13 (b)), instead of the LC filter required for DICM shapers ($L_f C_f$ in Fig. 13.13 (a)). The increased number of the components required for the DICM full-bridge topology is usually compensated by the higher power level which can be processed compared to the half-bridge shaper.

The principle of operation of the shapers in Fig. 13.13 is the same as described for the shaper using single-transistor topology in Section 13.2. For the proper operation, the top switch in the bridge leg must be current bidirectional. In addition, two switches in the same leg of the bridge must conduct out of phase and with no dead-time between their conduction. Therefore, there are two possible control methods of the duty ratio of

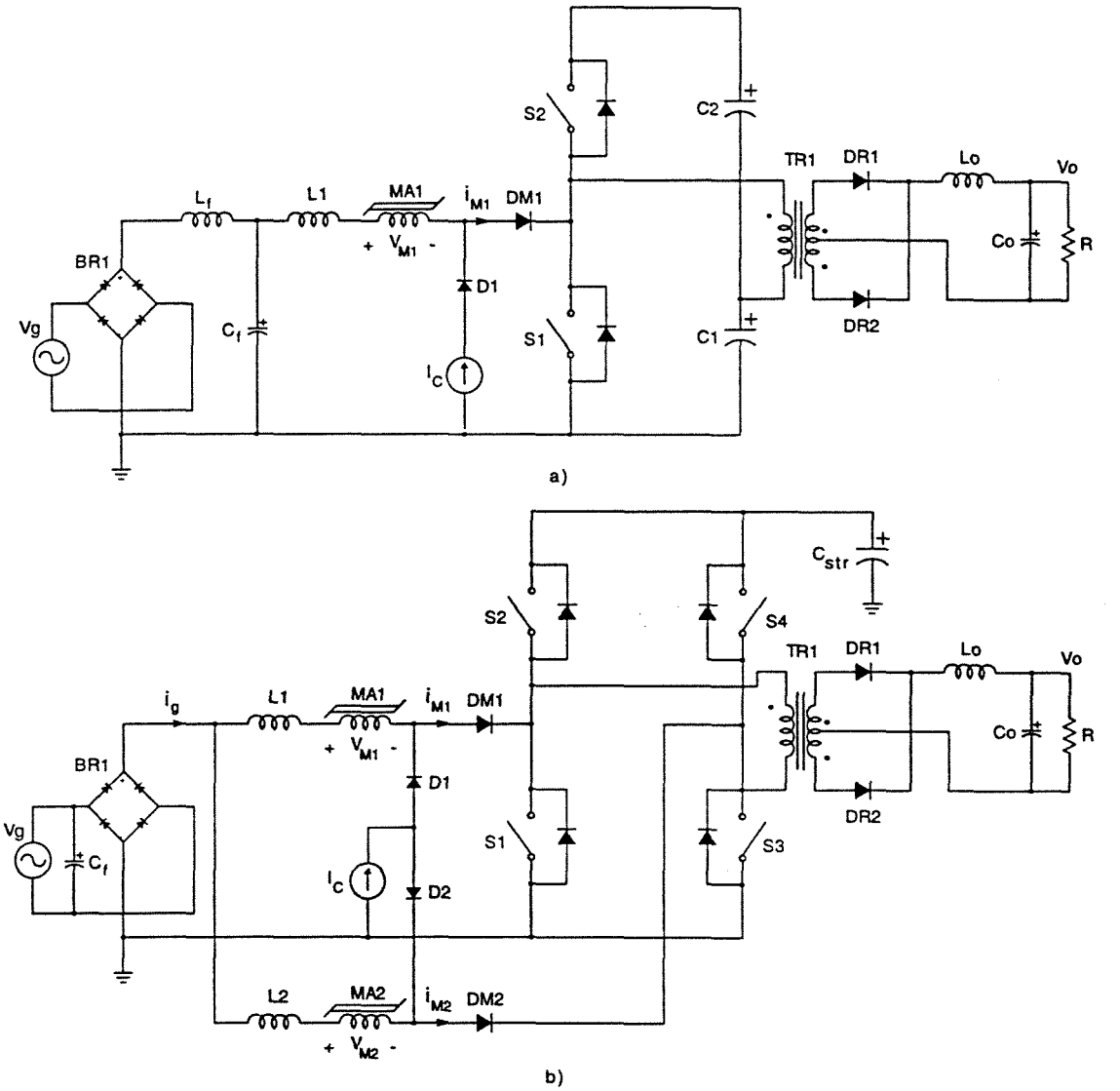

Figure 13.13: Input current shaping with magamps can also be used in a) the half-bridge, and b) the full-bridge topologies operated at fixed, 50%, duty ratio of their switches.

the primary side switches:

1. The duty ratio for all switches is fixed at 50% and the output voltage is then regulated by additional switches on the secondary side (for instance, with magamps).

2. The duty ratio of the switches in the same leg of the bridge is unbalanced or asymmetrical, and the output voltage regulation is provided by PWM modulation of the bridge switches [26, 72].

Both of these two control methods have their pros and cons which are addressed next.

FIXED DUTY RATIO CONTROL

The advantages of using fixed, 50%, duty ratio are:

1. Input and output stages are completely de-coupled.

2. There is no need for feedback isolation between primary and secondary circuits.

3. Both the input and the output power stages as well as the input current and the output voltage regulation loops can be optimized independently.

The input current and the output voltage are indeed controlled independently since there is no duty ratio modulation of the primary side switches. Any variation in the output will not affect input current waveform during half of the line period. Moreover, any modulation in the load current at the higher frequencies than the crossover frequency of the energy storage capacitor's regulation loop (which is typically less than 10Hz) will not be seen in the input current waveform. Similarly, since the voltage on energy storage capacitor is dc and regulated with primary side control loop, secondary side control is used only to regulate output voltage against load variations. This allows the highest possible bandwidth of the output voltage control loop (usually one third of switching frequency).

Idealized waveforms in the full-bridge shaper of Fig. 13.13 are shown in Fig. 13.14 for fixed 50% duty ratio. Each magamp has the same behavior as in either single-ended or half-bridge topologies.

This method is also well suited for a multiple-output extension when more than one output has to be tightly regulated and protected. For instance, by using multiple-output extension of the novel soft switching converters, described in Chapter 6, each

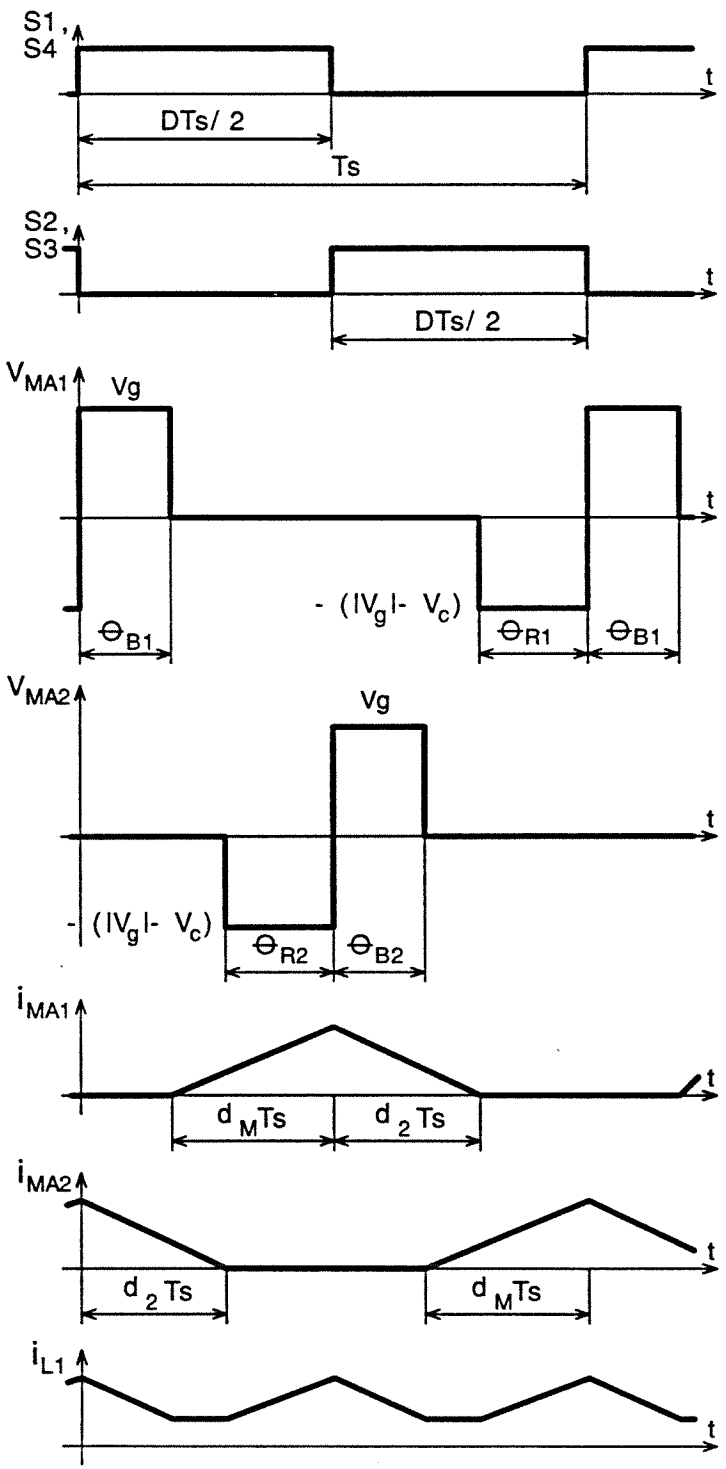

Figure 13.14: Idealized waveforms in DICM full-bridge shaper with fixed 50% duty ratio.

output can be regulated independently while the input current shaping and constant bus voltage, in this case V_{Cstr}, are both provided by the magamp in the input stage. The magamp regulators on the secondary side can be optimally designed since the constant volt-seconds are applied to each secondary winding of the transformer.

The main disadvantage of this approach is voltage stress on the primary side switches. Namely, according to Eq. (13.13), the minimum conversion ratio of the input stage, $M_{1,min}$, is two, and consequently, voltage stress on the bridge switches is $2V_{g,max}$. While this voltage stress is usually acceptable for the line voltage in range 80VAC-140VAC, it cannot probably be accepted at the higher voltages, for instance, 180VAC-250VAC or higher. Therefore, the applications of the bridge-type shapers with fixed, 50%, duty ratio are limited to the lower line voltages.

THE ASYMMETRICAL DUTY RATIO CONTROL

By using the asymmetrical duty ratio for the switches in the same leg of the bridge, their voltage stress can be kept lower than $2V_{g,max}$.

There are a large number of soft-switching half-bridge converter topologies with the asymmetrical duty ratio [26, 72, 27] as well as resonant topologies, widely used as a fluorescent lamp driver, to which the proposed input current shaping with magamp can be applied. In any case, the bus voltage and, consequently, voltage stress on the switches are reduced if the bottom switch always has a lower duty ratio than the upper switch in the same leg of the bridge.

As an example, the half-bridge inverter used as a fluorescent lamp driver, which employs magamp for input current shaping, is shown in Fig. 13.15.

The DICM full-bridge shaper can also operate with asymmetrical drives. Idealized waveforms are shown in Fig. 13.16.

13.7 Shapers with Continuous Input Current

The input stage of the full-bridge shaper with magamps, described in Section 13.6.2, can also be operated in *CCM*. This mode of operation is possible when two input inductors, L_1 and L_2 in the circuit of Fig. 13.13 (b), are replaced with a single inductor L_1 which is connected between the bridge rectifier and two magamps, MA_1 and MA_2,

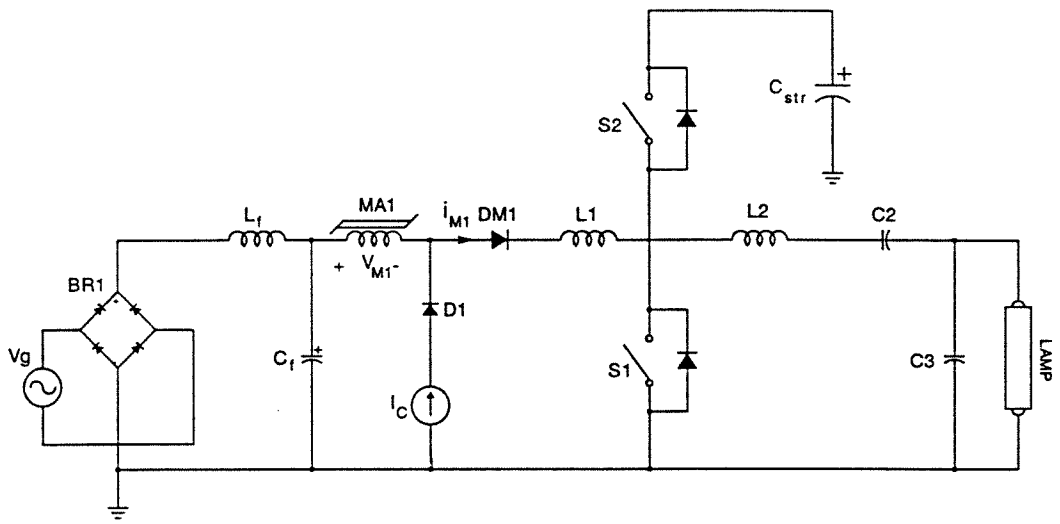

Figure 13.15: The half-bridge inverter used as a fluorescent lamp driver employing magamp for unity power factor.

as shown in Fig. 13.17. Each magamp is then connected by the series diode in series to the mid-point of its corresponding leg of the bridge. The energy transfer capacitor, C_{str}, is connected across two rails of the bridge. The effective load resistance, R_L, which is reflected load resistance to the primary, is connected across the energy storage capacitor C_{str} for the simplicity of analysis.

The operation of the input stage of the full-bridge shaper in CCM requires a slightly different DC analysis from that described for DCM in Section 13.4. Idealized waveforms of the shaper during a switching period are shown in Fig. 13.18, while the equivalent circuits, describing four different operating states of the shaper, are shown in Fig. 13.19.

Two diagonal switches of the bridge ($S1, S4$ and $S2, S3$ in Fig. 13.17) are simultaneously driven at constant frequency and exactly 50% duty ratio, while two switches in the same leg ($S1, S2$ and $S3, S4$) are driven out of phase as shown in Fig. 13.18. Energy is stored in the input inductor during conduction of the bottom switches ($S1$ and $S3$) and realized into the energy storage capacitor and load during conduction of the top switches ($S2$ and $S4$).

Each magamp blocks during the conduction interval of the bottom switch in the

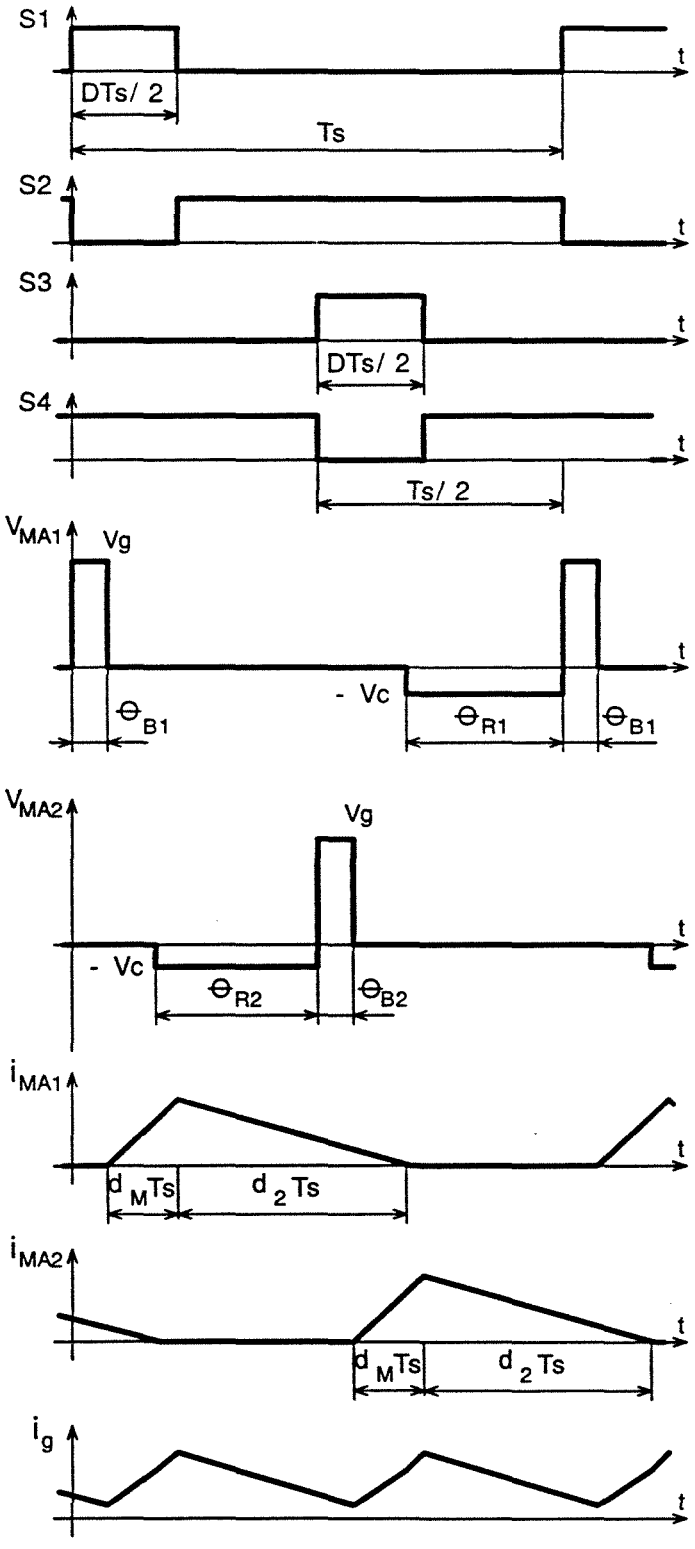

Figure 13.16: Idealized waveforms in DICM full-bridge shaper with the asymmetrical drives.

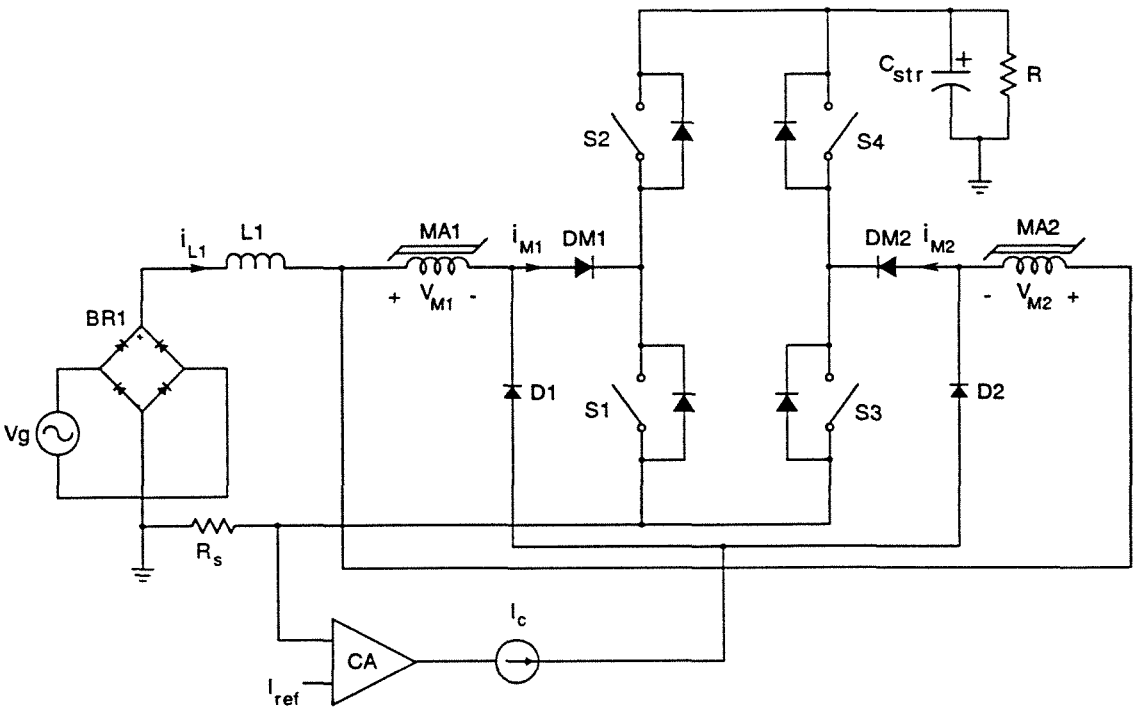

Figure 13.17: In the full-bridge current shaper with input stage operated in CCM, a single input inductor, L_1, and two magamps, MA1 and MA2, with series diodes, DM1 and DM2, are required for this mode of operation.

corresponding leg ($S1$ for $MA1$ and $S3$ for $MA2$), and resets during the conduction interval of the bottom switch in the opposite leg ($S3$ for $MA1$ and $S1$ for $MA2$) as shown in Fig. 13.18. Thus, each magamp delays conduction of the bottom switch in its corresponding leg and controls power flow from the input into the energy storage capacitor.

Assume that at $t = 0$, the switch $S3$, which was conducting the input inductor current, is turned off and the switches $S1$ and $S4$ are simultaneously turned on. Since the magamp $MA1$ was reset during conduction of the switch $S3$, it blocks during the interval θ_{B1} and forces demagnetization of the input inductor, through the switch $S4$, into the energy storage capacitor C_{str} (Fig. 13.19 (a)). During the blocking stage of the magamp $MA1$, the magamp $MA2$ is still saturated and the input inductor current, i_{L1}, linearly decays.

The magamp $MA1$ saturates at $t = \theta_{B1}$ causing the turn-off of the diode $DM2$, and

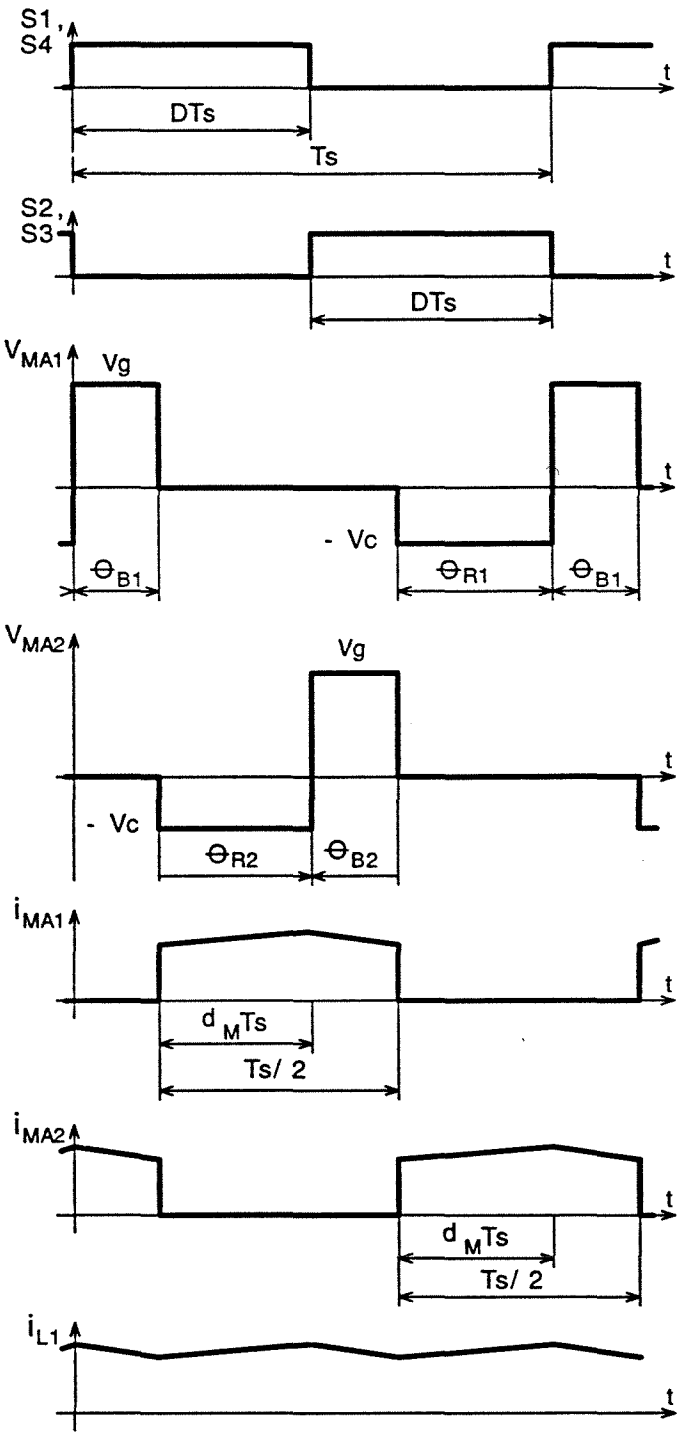

Figure 13.18: Idealized waveforms in the novel full-bridge current shaper with symmetrical drives and the input stage operated in CCM.

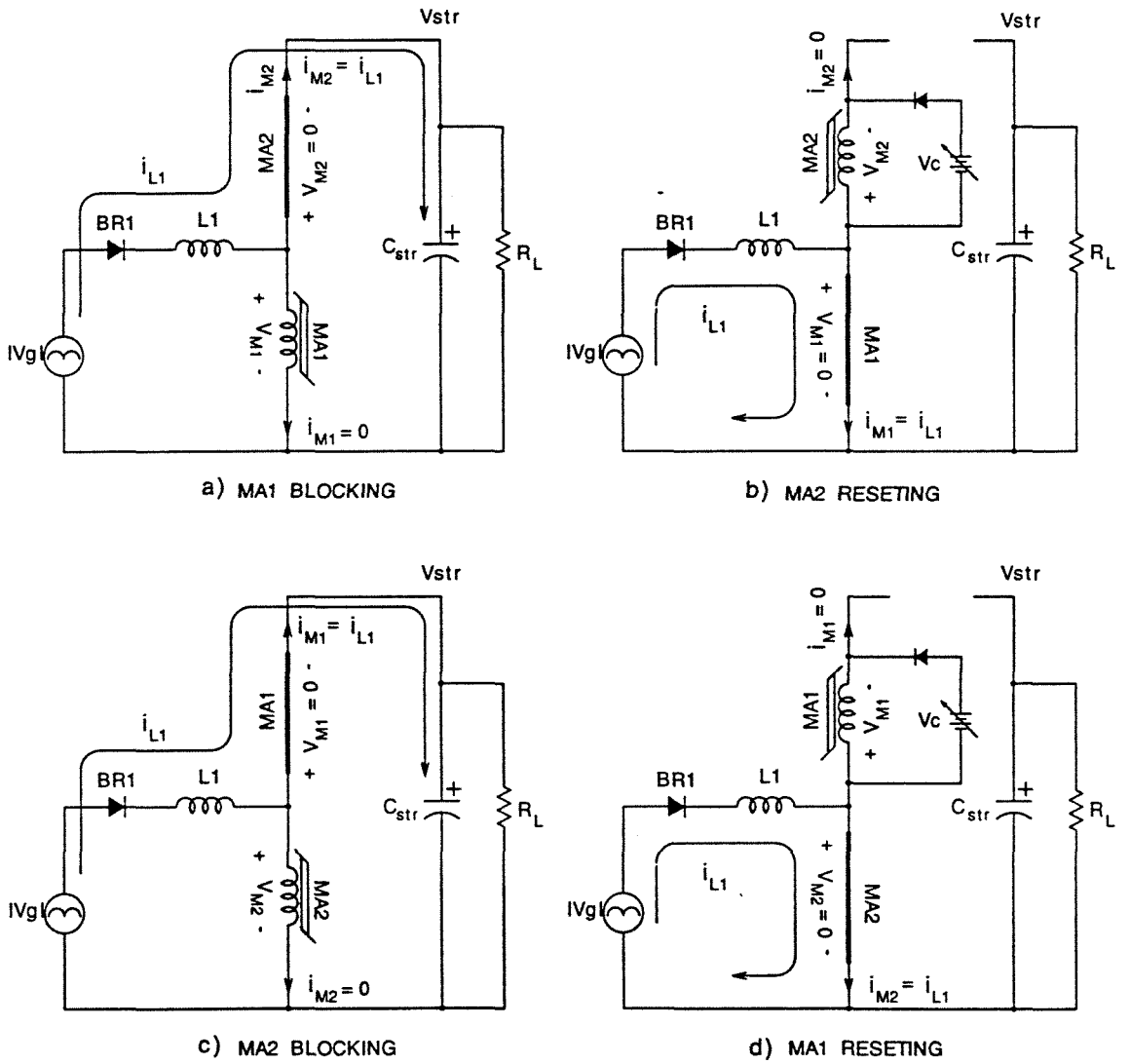

Figure 13.19: Equivalent circuits of the full-bridge shaper with input stage operated in CCM during four different operating states: a) blocking state of the magamp MA1, b) resetting state of the magamp MA2, c) blocking state of the magamp MA2, and d) resetting state of the magamp MA1.

the magamp $MA2$ runs out of saturation. The blocking state of magamp $MA1$ is finished and the reset state of magamp $MA2$ starts (Fig. 13.19 (b)). During the interval θ_{R2}, the input inductor current flows through the saturated magamp $MA1$ and the bottom switch $S1$, while the magamp $MA2$ is resetting by the control voltage V_c . The first half of the switching period is finished by turning off the switch $S1$ and turning on switches $S2$ and $S3$, which initiates the blocking state of the magamp $MA2$ and the second half of the switching period (Fig. 13.19 (c)).

During the interval θ_{B2}, the magamp $MA2$ blocks and forces demagnetization of the input inductor, now through switch $S2$, into the energy storage capacitor C_{str} (Fig. 13.19 (c)). During this interval, the magamp $MA1$ is still saturated and the input inductor current, i_{L1}, linearly decays.

The magamp $MA2$ saturates after the time θ_{B2} causing the turn-off of the diode $DM1$ (Fig. 13.17), and the magamp $MA1$ runs out of saturation. As a consequence of that, the input inductor current flows through the saturated magamp $MA2$ and the bottom switch $S3$ during the reset state of magamp $MA1$ (Fig. 13.19 (d)). During the interval θ_{R1}, magamp $MA1$ is resetting by the control voltage V_c.

The second half of the switching period, and therefore one switching period, are finished by turning off switch $S3$ and turning on switches $S1$ and $S4$. The operating states of the converter repeat after this.

The conversion ratio of the shaper, $M_1 = V_{cstr}/V_g$, is calculated from the volt-second balance on the input inductor as:

$$M_1 = \frac{V_{cstr}}{V_g} = \frac{1}{1 - 2d_M} \tag{13.22}$$

where, d_M is the magamps' duty ratio. Notice that due to the symmetry

$$\theta_{B1} = \theta_{B2} = D - d_M \tag{13.23}$$

$$\theta_{R1} = \theta_{R2} = d_M \tag{13.24}$$

where, D is the duty ratio of the bottom switches of the bridge. For the symmetrical drives (Fig. 13.18) $D = .5$. We are now interested in the minimum conversion ratio, $M_{1,min}$ which occurs at the maximum input voltage, $V_{g,max}$, and is determined by the

minimum achievable duty ratio of the magamps, $d_{M,min}$ (the maximum blocking capability). The minimum duty ratio $d_{M,min}$ is determined by the reset voltage V_c, which is limited to $V_{C_{str}}$ (Fig. 13.19 (b) and (d)). From the equality of the volt-seconds stored and the volt-seconds blocked, we can write:

$$V_c d_M = V_{C_{str}}(D - d_M). \tag{13.25}$$

The duty ratio of the magamp is then calculated from Eq. (13.25) as:

$$d_M = D\frac{V_{C_{str}}}{V_{C_{str}} + V_c} = \frac{1}{1+\alpha}D \tag{13.26}$$

where,

$$\alpha = \frac{V_c}{V_{C_{str}}} \leq 1. \tag{13.27}$$

For $D = .5$, the minimum duty ratio, $d_{M,min} = .25$, is achieved for $V_c = V_{C_{str}}$ ($\alpha = 1$), which results in minimum conversion ratio $M_{1,min} = 2$. The main disadvantage of the symmetrical 50% drives is voltage stress on the active switches $S1 - S4$ which is twice the input voltage ($2V_{g,max}$). Thus, the applications of the full-bridge shaper with magamps and 50% duty ratio are limited to the lower line voltages.

The minimum conversion ratio $M_{1,min}$, can be reduced below two if the asymmetrical drives are used. Idealized waveforms of the full-bridge shaper from Fig. 13.17 with the asymmetrical drives are shown during a switching period in Fig. 13.20.

The principle of operation is the same as with symmetrical drives (Fig. 13.18). During the intervals when the bottom switches ($S1$ and $S3$) are both turned off and the top switches ($S2$ and $S4$) are turned on, one magamp is saturated and carries the input inductor current while the voltage on the other magamp is limited to zero. Therefore, as before, each magamp (for instance, $MA1$) is reset only during the simultaneous conduction of the other magamp and its corresponding bottom switch ($MA2$ and $S3$).

The minimum duty ratio of the magamp, $d^a_{M,min}$, and the minimum conversion ratio, $M^a_{1,min}$, where superscript a is used for the asymmetrical drives, are calculated from Eq. (13.26) as:

$$d^a_{M,min} = \frac{D}{2} \tag{13.28}$$

$$M^a_{1,min} = \frac{1}{1-D}. \tag{13.29}$$

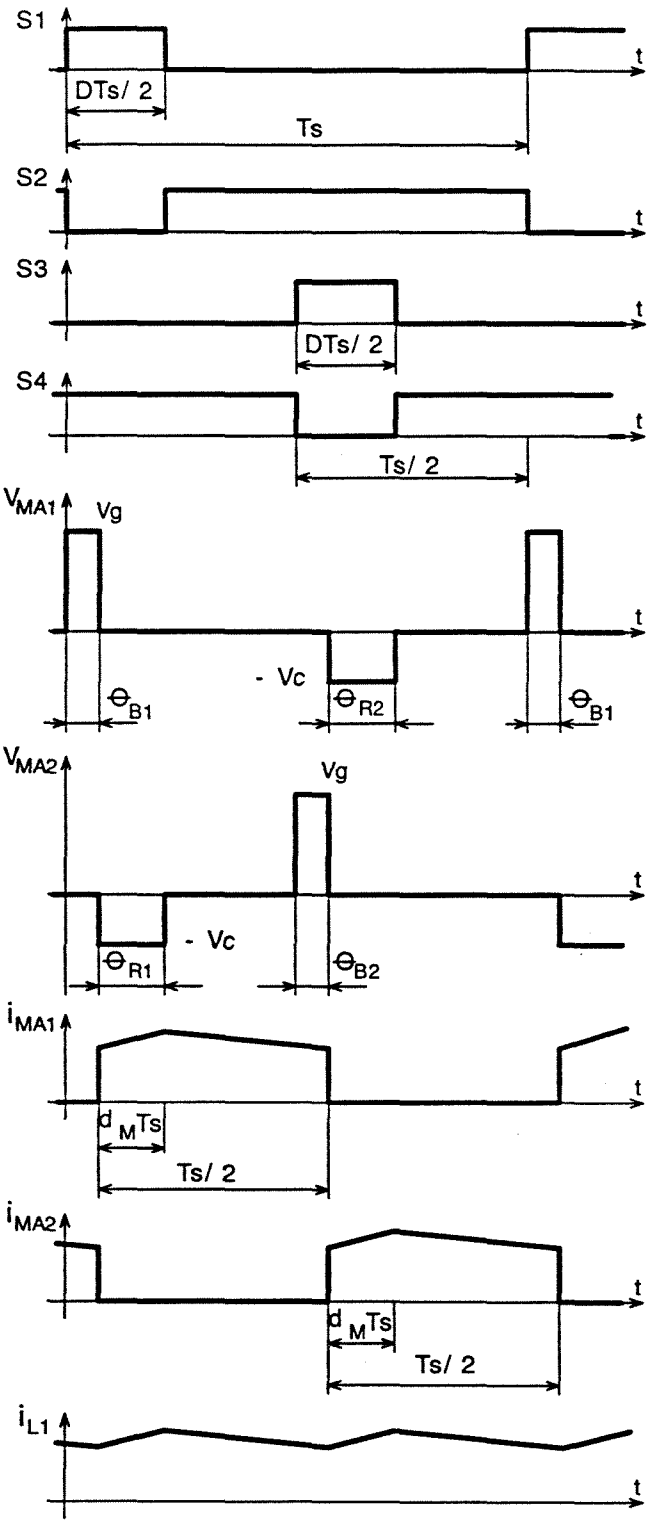

Figure 13.20: Idealized waveforms in the novel full-bridge shaper with the asymmetrical drives and input stage operated in CCM.

Equation (13.29) gives the same relation between the minimum conversion ratio of the shaper with magamp and the duty ratio of the active switches as Eq. (13.13) derived for DICM.

It is evident from the above analysis that the proposed full-bridge shaper from Fig. 13.17 has the same conversion ratio and input current waveform as the boost shaper operated in CCM. The main advantages of the novel shaper are:

1. Input current is controlled by modulating blocking state of the magamps instead of by pulse-width modulation of the active switches.

2. Soft-switching of the diodes $DM1$ and $DM2$ is inherently provided by magamps $MA2$ and $MA1$, respectively.

3. Input inductor is reduced since it operates at a twice higher frequency than the switching frequency of the converter.

4. The input current shaping and output voltage regulation are completely decoupled if the controllable switches are used on the secondary side.

5. Isolation between the line and load is provided.

13.8 Experimental Results

In this section experimental results obtained on two prototypes, one single transistor automatic current shaper and other the full-bridge shaper operating in CCM, are presented.

13.8.1 DICM Single Transistor Shaper

The schematic of the 80W, 48V automatic current shaper with magamp operated at constant switching frequency of 200KHz is shown in Fig. 13.8. The shaper was operated from the line voltage 110VAC. The component used in the prototype are listed below:

Transistor: $Q1$ = IRF740

Diodes: $BR = VH248$, $D1, D2$ = 10CTF40

Magnetic amplifier: $MA1$ - core MB18/12/4.5, N_p = 35T, N_c = 5T

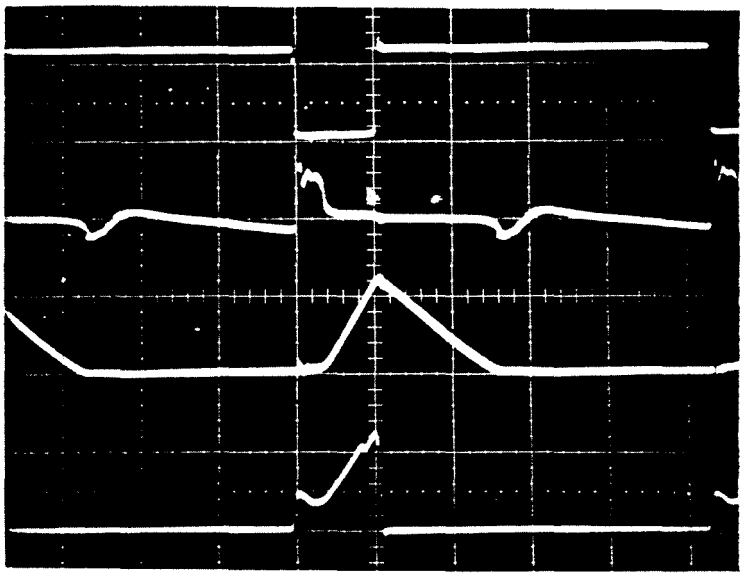

Figure 13.21: Waveforms in the ACSICMA during a switching period: a) drain-to source voltage of the $Q1$ (top trace: 200V/div.), b) voltage on the control winding N_c (trace 2: 50V/div.), c) input inductor current (trace 3: 4A/div.), and d) transistor current (bottom trace: 5A/div.). Time scale: 1μs/div.

Capacitors: $C_f = .82\mu\text{F}$, $C_{str} = 680\mu$, $C_2 = 470\mu\text{F}$

Inductors: L_f=125μH, L_1=17μH, L_2=500μH

The current reset method is used in order to keep the duty ratio of the magamp constant, as explained in Section 13.5.1. To verify the principle of operation, both voltage feedback loops in Fig. 13.8 were disconnected, and the duty ratio of the transistor $Q1$ was kept constant. The reset current is then adjusted manually for the output voltage 48V.

Waveforms of the $Q1$'s drain-to-source voltage, voltage on the control winding N_c, the input inductor current, and the transistor currents are are shown during one switching period at nominal load (1.75A) and line voltage 110VAC in Fig 13.21 . As can be seen from the waveforms, they agree very well with predicted waveforms in Fig. 13.4. The voltage overshoot in the magamp voltage waveform right after the inductor current reached zero is due to reverse recovery current of the diode $D1$.

The line voltage and the line current waveforms, obtained at the nominal line voltage

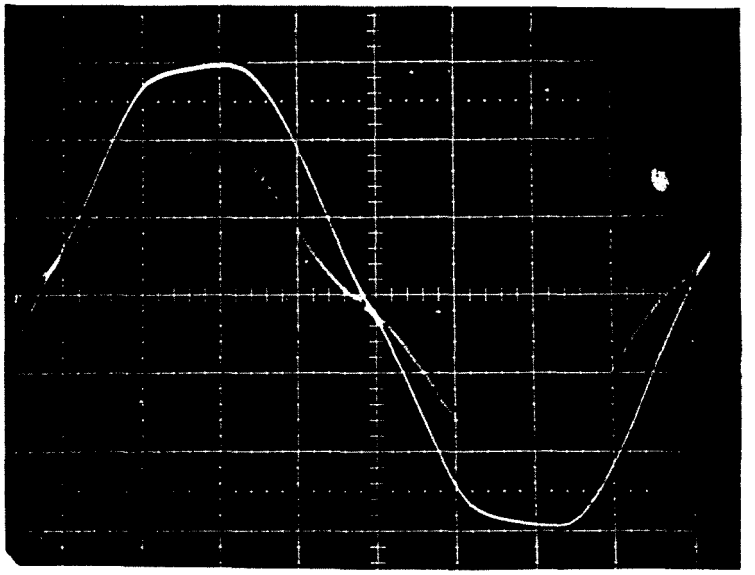

Figure 13.22: The Line current (0.5A/div.) follows the line voltage (50V/div.) automatically in the novel current shaper with magamp. Time scale: 2ms/div.

(110VAC) and 1A load current with slow voltage regulation loop closed, are shown in Fig 13.22. The voltage on the energy storage capacitor C_{str} was 240VDC, which corresponds to the conversion ratio M_1=1.56. The line current waveform is slightly distorted as predicted by Fig. 10.9. Power factor and THD for the DCM boost shaper are .98 and 17%, respectively.

The measurement is then repeated for the load current 0.23A (13% of nominal load) and the waveforms are shown in Fig. 13.23. The line current still follows the line voltage even at light load. In addition, the energy storage capacitor's voltage is maintained constant.

13.8.2 CCM Full-Bridge Shaper

Experimental waveforms obtained in the 150W, 50V prototype of the full-bridge shaper from Fig. 13.17 are shown in this section. Converter was operated at 150KHz and fixed 50% duty ratio from the line voltage 110VAC. The component values used in the prototype are listed below:

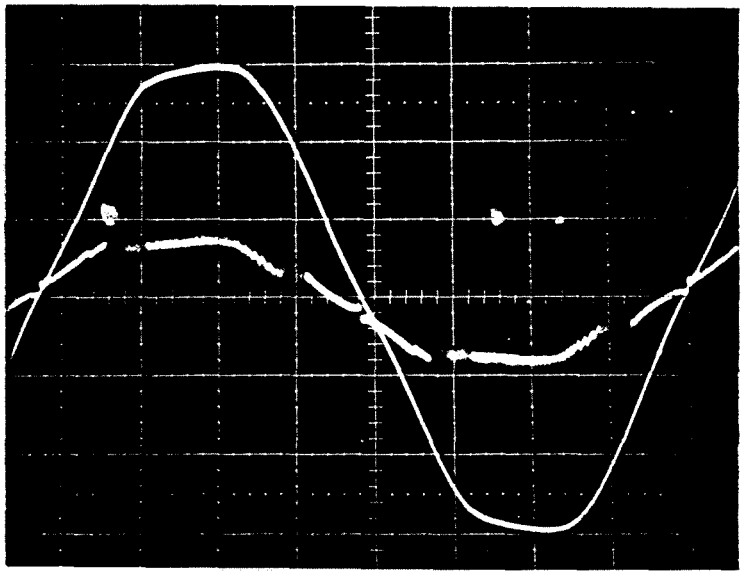

Figure 13.23: The line current (0.5A/div.) follows the line voltage (50V/div.) automatically even at light load. Time scale: 2ms/div.

Transistors: $Q1$ - $Q4$ = IRF640

Diodes: $BR1$ = VH248, $DM1, DM2$ = 10CTF40

Input inductor: $L1 = 300\mu$H

Filter capacitor: $C_f = 1\mu$F

Magnetic amplifiers: $MA1, MA2$ - 30T 8 X AWG30 wire on core 50B45-1E (Magnetics)

Capacitors: $C_{str} = 470\mu$F

Drive waveforms for the MOSFETs and currents in two magamps are shown during the switching period at the peak of the line voltage in Fig. 13.24 to verify predicted behavior from Fig. 13.18. The small asymmetry in the current waveforms of the two magamps is consequence of the mismatched diodes $DM1$ and $DM2$, and cores used for magamps. This asymmetry is inherent to all symmetrical topologies, particularly when the current reset method is used for the magamps.

The line voltage and the line current waveform during the line period are shown for three different load currents 3A (100% load), 1.5A (50% load), and .75A (25% load) in Figs. 13.25-13.27, respectively. As can be seen, the line current follows line voltage for

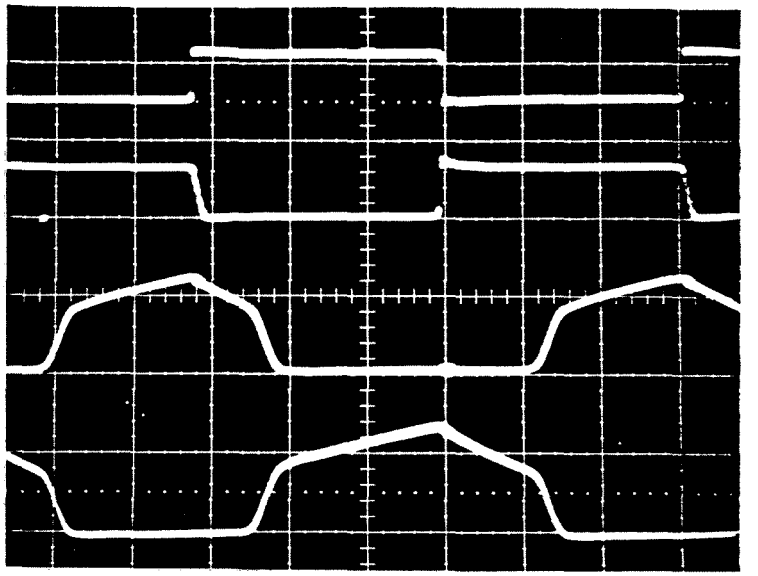

Figure 13.24: Waveforms in the full-bridge shaper with magamps operated in CCM during the switching period at the peak of the line voltage: a) drive signals for the $Q1$ and $Q4$ (top trace: 20V/div.), b) drive signals for the $Q2$ and $Q4$ (trace 2:20V/div.), c) current in the magamp $MA2$ (trace 3: 2A/div.), and d) current in the magamp $Q1$ (trace 4: 2A/div.) with time scale: 1μs/div.

wide range of load current. The crossover distortion in the line current is consequence of reverse recovery current of the diodes $DM1$ and $DM2$ which introduce undesirable reset of the magamps at the zero crossing of the line voltage. This is not a serious problem and can be very easily solved with some additional circuitry.

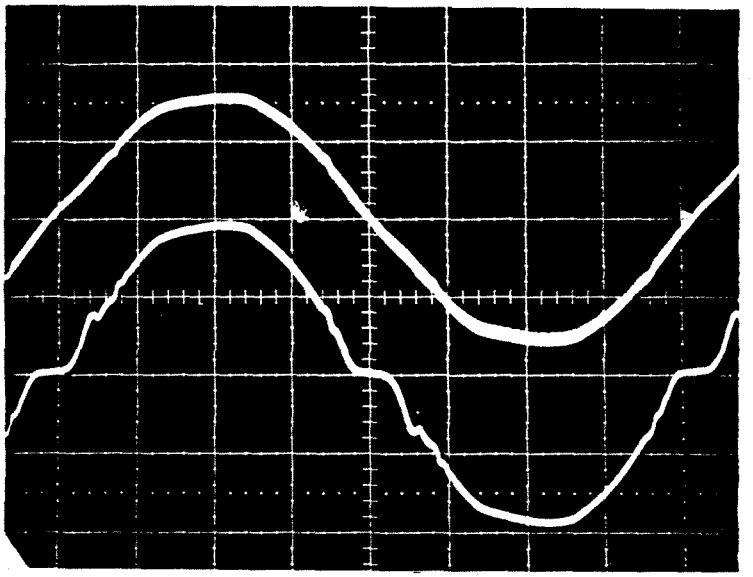

Figure 13.25: Measured the line voltage (top trace: 100V/div.) and the line current (bottom trace: 1A/div.) waveforms at full output power of 150W during the line period (time scale: 2ms/div.).

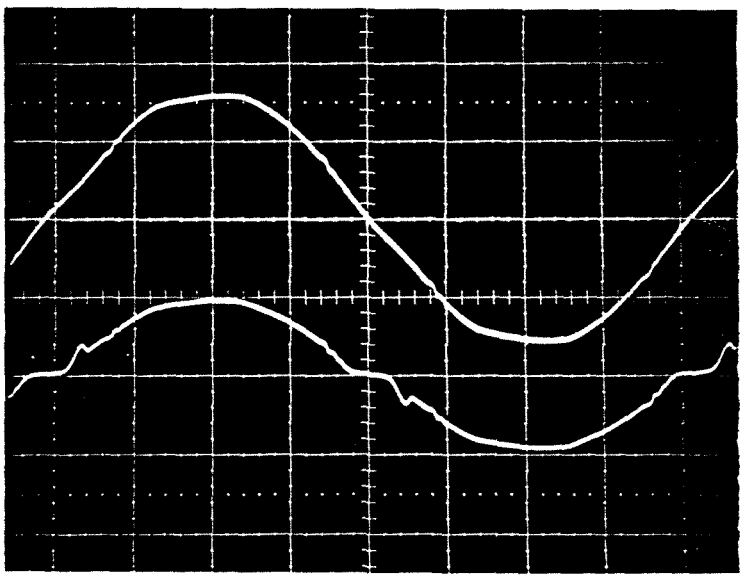

Figure 13.26: Measured line voltage (top trace: 100V/div.) and line current (bottom trace: 1A/div.) waveforms at 50% load current during the line period (time scale: 2ms/div.).

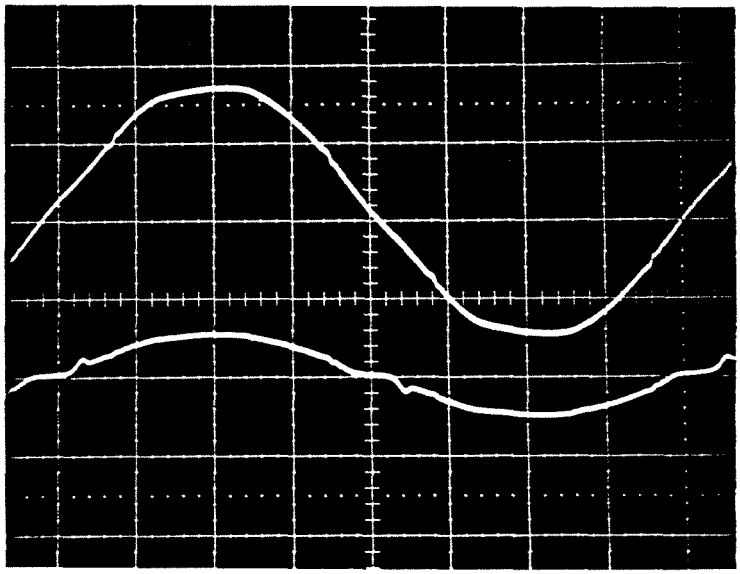

Figure 13.27: Measured the line voltage (top trace: 100V/div.) and the line current (bottom trace: 1A/div.) waveforms at 25% load current during the line period (time scale:2ms/div.).

Chapter 14

Conclusion

Automatic input current shaping with external and internal capacitive energy storage is undertaken in this part of the thesis. After examining the fundamental limitations of the existing approaches, three novel solutions are proposed. The first solution, an automatic current shaper with external capacitive energy storage, is based on the Ćuk converter with integrated magnetics operated in DICM. The other two solutions have internal energy storage and combine automatic input current shaping and fast output regulation in a single converter. While the second novel topology is based on the soft-switching Ćuk converter, the third solution, which is applicable to a large number of AC-to-DC and AC-to-AC converter topologies, uses magamp for input current shaping. Original contributions of this thesis in improving the quality of the input current as well as of the output voltage are summarized below:

1. High Performance Automatic Current Shaper with External Energy Storage and Unity Power Factor

Ćuk converter behaves as the ideal current shaper, and performs current shaping automatically with no control when operating in DICM. By keeping both duty ratio and switching frequency constant, the input current is indeed linearly dependent on line voltage since the input part of the Ćuk converter inherently emulates a resistor.

High inrush current during start-up as well as the overload current during short circuit, which are serious drawbacks in the boost converter, are reduced in the Ćuk converter by almost two orders of magnitude.

Integrated magnetics topology inherent to isolated version of the Ćuk converter is successfully applied in current shaping applications where isolation is required. Essentially zero input and output switching current ripples are obtained for all operating conditions without additional filtering or increase of the switching frequency, while still keeping the

size of the magnetics small. The high leakage inductance in the integrated magnetics structure further reduces inrush current at least by a factor of 3.

The full advantages of the Ćuk converter with integrated magnetics used in current shaping applications are evident: automatic current shaping, zero input and output switching current ripple, isolation between line and load, wide range of input and output voltages, small size of magnetics even at switching frequency of 35kHz, natural protection against startup inrush current or overload current, and high overall efficiency.

Experimental results demonstrate high performance of the current shaper based on the Ćuk converter with Integrated-magnetics operating in DICM.

2. Soft-Switching Automatic Current Shaper with Fast Output Regulation

A new AC-to-DC converter using the soft-switching Ćuk converter combines automatic current shaping, fast output voltage regulation and loss-less zero voltage switching into a single stage. By keeping duty ratio constant, the input current follows the line voltage automatically, and output voltage is regulated against load variations at the same time.

By inserting a diode in series with the source in the basic Ćuk converter operated in DICM with constraint $L_2 > ML_1$ (Fig. 12.2), two completely new modes of operation are discovered (Fig. 12.5). These two new DICM modes effectively decouple the input boost-like part of the Ćuk converter, operated always in DICM, from its buck-like output, operated either in DICM or CCM, and allow the energy transfer capacitor voltage to be independent of the input voltage. Decoupled DICM modes now offer an attractive feature: DICM mode of boost-like input stage can be operated as an automatic current shaper with constant duty ratio and internal capacitive energy storage which can allow fast output voltage regulation at constant duty ratio when output buck stage operated always in CCM.

It was shown that in an isolated version of the shaper, when the magnetizing inductance is small and properly designed, only one large energy storage capacitor is required on the primary side, while the secondary side capacitor can be small. The output filter is therefore also a high-frequency component.

When the output diode in the basic Ćuk converter of Fig. 12.6 was replaced with

MOSFET, the output inductor current became bidirectional and provided soft-switching. Since in this mode, the output stage always operated in CCM, almost constant duty ratio was required to regulate output voltage against load variations.

Complete decoupling of the input DICM boost stage of the Ćuk converter from its output buck stage allowed wide bandwidth of the output voltage regulation loop (30kHz bandwidth for 100kHz switching frequency).

In order to limit maximum voltage on the MOSFETs for wide line and load variations, low-bandwidth, variable switching frequency control is added in addition to duty ratio control.

Experimental results obtained on 50W, 12V prototype demonstrate high performance of the proposed utility-to-DC interface based on the soft- switching, automatic current shaper, isolated Ćuk converter.

3. High Performance Single Stage Converters Using Magamp for Input Current Shaping

The input current shaping with magamp is introduced for the first time in literature. A novel class of single stage AC-to-DC and AC-to-AC converters with unity power factor and fast output regulation is synthesized and analyzed. These converters use a magamp for the input current shaping, while the active switch is used for fast output regulation. By using the core material for magamps with high saturated permeability, and operating the input stage of the converter in DICM, the linear input inductance can be replaced by the saturated inductance of the magamp. Thus, the magamp combines the functions of a controllable switch and a linear inductor into a single device.

These topologies offer four significant improvements to the existing single-stage current shapers with internal energy storage:

a) Both the input current and the energy storage capacitor's voltage can be regulated with magamp and independently of the output voltage regulation.

b) Unity power factor is obtainable.

c) Input inductor can be replaced with the saturated inductance of the magamp which provides lower core losses and higher overload capability.

d) Constant switching frequency.

The proposed method of current shaping with magamps is successfully extended to the full-bridge topologies with their input, boost-like stage operated in continuous conduction mode.

Experimental results obtained on different prototypes confirm advantages of the proposed topologies with magamps.

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