

Grid Mixers and Power Grid Oscillators

**Thesis by
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To my Family and Friends

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Grid Mixers and Power Grid Oscillators

Abstract

Power-combining schemes involving planar grids of solid-state devices quasi-optically coupled in free space are an efficient means of combining power at microwave and millimeter-wave frequencies. The quasi-optical coupling of these grid circuits makes them ideal for millimeter-wave and submillimeter-wave applications by eliminating waveguide sidewall losses and machining difficulties. The planar property of the grids potentially allows thousands of devices to be integrated monolithically. In this thesis, a grid mixer suitable for mixing or detecting quasi-optical signals is presented. The mixer is a planar grid structure periodically loaded with diodes. The grid mixer power handling and dynamic range scales as the number of devices in the grid. The conversion loss and noise figure of the grid are equal to that of a conventional mixer. A variation of the grid mixer, the sideband generator grid, is shown to be an efficient package for increasing the theoretical operating frequency and output power of monolithic planar diodes at terahertz frequencies. Techniques for designing power grid oscillators to produce Watt-level output powers are described. Designs and experimental results for MESFET grid oscillators operating in X-band with output powers of 0.9 W to 10.3 W are presented in detail. Methods that make use of finite-element electromagnetic solvers for analyzing grid structures of arbitrary shape are discussed.

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Chapter 1

Introduction

The field of quasi-optics is generating substantial interest and debate among members of the microwave community. This interest is fueled by the trend in the microwave industry towards higher frequencies, particularly the millimeter-wave band, and higher powers. The millimeter-wave band, generally considered to be from 30 GHz to 300 GHz, has broad applications from the measurement of molecular resonance lines in radio astronomy [1] to commercial mobile personal communication networks (PCNs) [2] and short-range military radars [3]. To make high-frequency electronic devices, one needs to be able to control tolerances to a small fraction of a wavelength. In the millimeter-wave band this is on the order of a few microns, a size sufficiently small that the fabrication of conventional microwave circuits becomes both difficult and costly. Consequently, alternative techniques based on quasi-optics are a sensible and practical approach at these frequencies. Quasi-optics allow the mature technology of optics to be scaled down to operate in the microwave and millimeter-wave bands. These techniques promise greater power and performance in the millimeter-wave band than is presently achievable with conventional circuit designs [4].

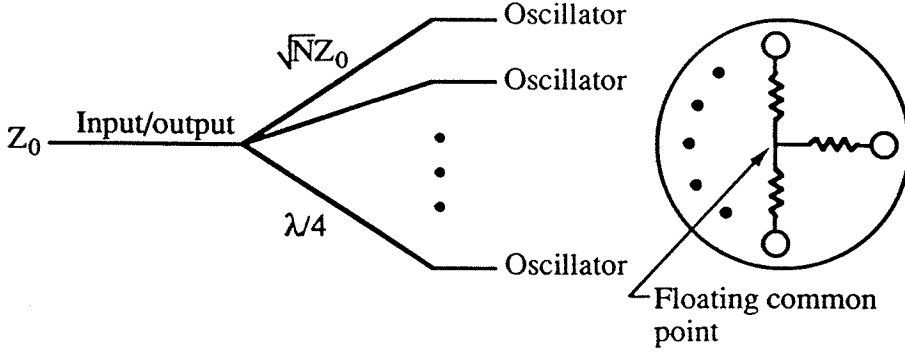
1.1 QUASI-OPTICAL POWER COMBINING

Quasi-optical power combining is an efficient method of coupling many devices together. Quasi-optic circuits look very different from conventional microwave and millimeter-wave combining circuits. A traditional microwave com-

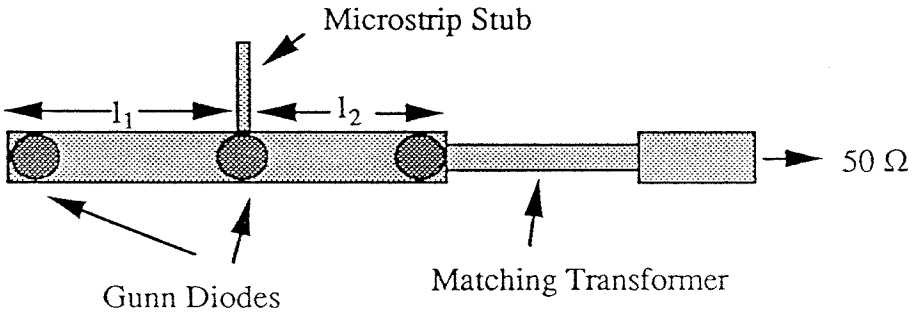
biner is based on transmission lines, frequently waveguide or microstrip, and lumped-element circuits with the devices electrically connected to the combining circuit with metal conductors (Figure 1.1). Such structures exhibit significant limitations as the frequency of operation increases. They are subject to conduction and radiation losses which degrade efficiency, their fabrication becomes complex and expensive due to the small size of the circuits, particularly waveguide, at high frequencies, and they are unsuitable for combining more than a small number of devices. Their small size also makes them relatively fragile and unreliable.

Quasi-optical power combining eliminates these problems by coherently combining the outputs of many devices in free space. By eliminating the metal walls found in waveguide systems, quasi-optic systems reduce sidewall conduction losses that can reduce efficiency in waveguide combiners. Through the use of dielectric slabs, polarizers, metal-patterned grids on substrates, and surfaces embedded with hundreds of individual solid-state devices, microwave components can be synthesized quasi-optically that behave similarly to conventional lumped circuit elements and transmission lines, but with much greater power-handling capabilities. However, unlike conventional circuit elements, quasi-optical components have dimensions that are large compared to a wavelength avoiding the fabrication problems that plague conventional circuits designed to operate in the millimeter-wave band.

Although quasi-optical circuits look more like optical devices (Figure 1.2), they can be modelled with reasonable accuracy using simple transmission-line and lumped-element components. This has the fortunate consequence that the immense knowledge and sophisticated computer-aided design tools developed for conventional microwave circuits can be readily applied to the design and modelling of quasi-optical circuits. In addition, active quasi-optical circuits are often highly suited for manufacture using planar photolithographic techniques in com-



(a)



(b)

Figure 1.1 Conventional combining techniques use transmission lines and lumped elements to combine devices together. (a) Wilkinson microstrip combiner used to combine the outputs of several devices [5]. (b) A single resonant planar power-combining technique for combining three devices. The length l_1 and l_2 are chosen to resonate with the device reactance to form a filter-like structure. This technique is analogous to direct-coupled waveguide cavity filters [6].

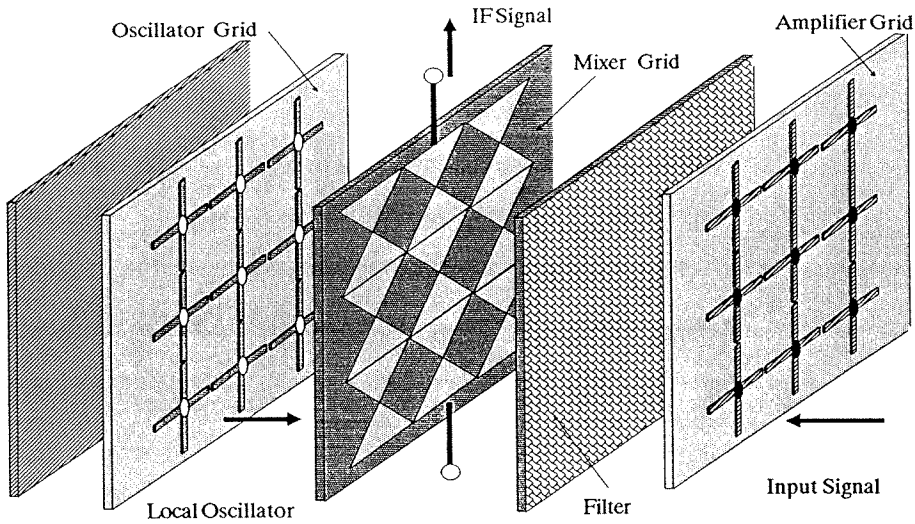


Figure 1.2 A quasi-optical receiver [7].

mon use by the semiconductor industry. This significantly decreases the capital expenditure required to implement quasi-optical systems and allows seamless integration of quasi-optic components into existing semiconductor fabrication processes.

1.2 GRID MIXERS

A variety of quasi-optical configurations have been explored including phase-shifters [8,9], frequency multipliers [10,11], oscillators [12]–[24], and amplifiers [25,26]. One configuration that has not been extensively examined is the quasi-optical grid mixer. A grid loaded with diodes produces a nonlinear device suitable for mixing or detecting quasi-optical signals with improved dynamic range compared to conventional single-diode mixers. This is particularly important for superconducting tunnel-junction (SIS) receivers where dynamic range is limited [27]. Millimeter-wave high-dynamic-range front-ends are also the subject of a

U.S. Navy initiative addressing current needs in its microwave electronics operational capability [28]. Indeed, very few circuit topologies and devices address the problems of intermodulation distortion and dynamic range in high-frequency mixers [29]. It should be possible to manufacture the grid mixer as a planar monolithic circuit allowing a large number of diodes to be combined on a single wafer. This approach should give significant improvements in power-handling and dynamic range for mixers operating in the millimeter-wave band and above.

The planar grid mixer is shown in Figure 1.3. Diodes are loaded periodically in the grid, each diode defining a unit cell. The diodes in the array are presented with an embedding impedance which is a function of the grid structure repeated throughout each unit cell. There is a flat metal mirror behind the grid to act as a reactive tuning element. Diodes in each column are connected in series. The IF voltages add along each column and are collected at the diode terminals forming the top and bottom edges of the grid. A dc bias may also be applied at the grid edges.

Depending on the application, the grid mixer can be used as a downconverter for receiving signals, or as an upconverter for use in a millimeter-wave transmitter or a tunable signal source. Coupled together with quasi-optical amplifiers, oscillators, and filters, the grid mixer forms a key component in a quasi-optical receiver or transmitter for radar, remote sensing, and telecommunication applications. Such systems promise to outperform conventional waveguide receivers in the millimeter-wave band in terms of improved dynamic range, power handling, and lower system noise temperatures.

1.3 POWER GRID OSCILLATORS

For many years there has been a substantial effort to obtain more power from high-frequency solid-state devices. The need for reliable, inexpensive, high-power sources is particularly urgent in the development of solid-state millimeter and submillimeter-wave systems because devices at these frequencies give much

lower output power than in the lower microwave frequency band (Figure 1.4).

For this reason, power combining schemes involving solid-state devices quasi-optically coupled in free space have received considerable attention as an efficient means of combining the output power of many devices at microwave and millimeter-wave frequencies. A quasi-optical grid oscillator consists of a two-dimensional array of active devices producing a planar sheet with a reflection coefficient greater than unity. A resonator can be used to provide feedback to couple the devices together to form a high-power oscillator. By integrating large numbers of devices into the grid, very large powers can be achieved. The planar configuration of the grids is suitable for monolithic integration and provides an attractive means of obtaining high power from solid-state devices that is scalable to millimeter-wave frequencies.

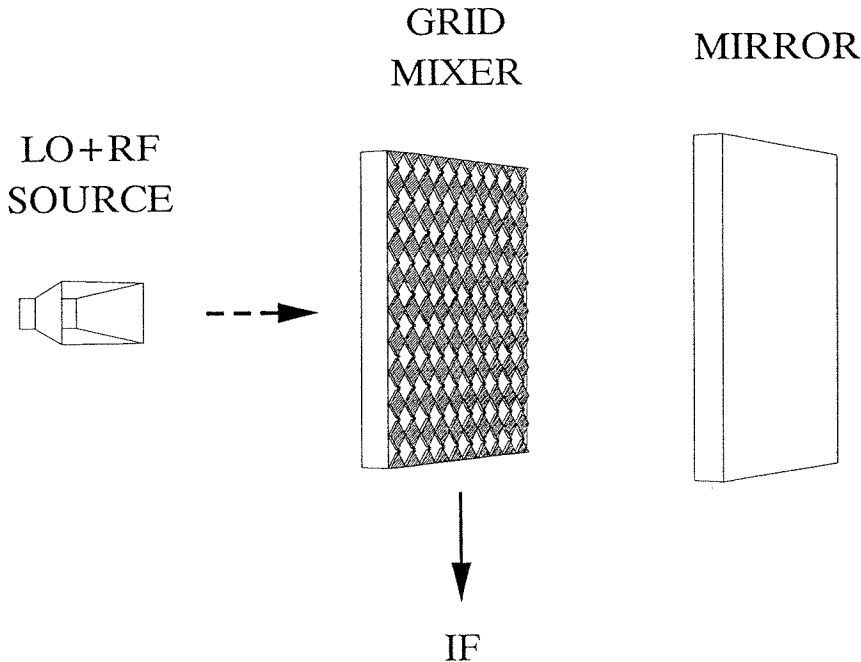


Figure 1.3 Quasi-optical grid mixer configuration. The RF and LO signals couple to the diodes quasi-optically through the face of the grid. The IF signal is generated across the top and bottom grid edges. The mirror is used to tune out the capacitive reactance of the diodes for a better match to free space.

Recent work on grid oscillators [13]–[19] has convincingly demonstrated proof of concept. However, these grids have all used relatively low-power devices and have not delivered the promised large powers (Table 1.1). To date, the highest published total radiated power for a transistor grid oscillator is 550 mW at 5 GHz from a 100-element grid [15]. These powers are substantially lower than those developed by vacuum tube sources at these frequencies and, more importantly, are substantially lower than the 10 W to 1 MW needed for effective integration into millimeter-wave systems [28]. This is hardly surprising, however, as little or no attempt was made to design these oscillators for maximum power.

In order to demonstrate Watt-level powers from a quasi-optical grid oscillator, existing power oscillator design principles must be integrated with quasi-optical grid oscillator theory. Factors which need to be taken into consideration

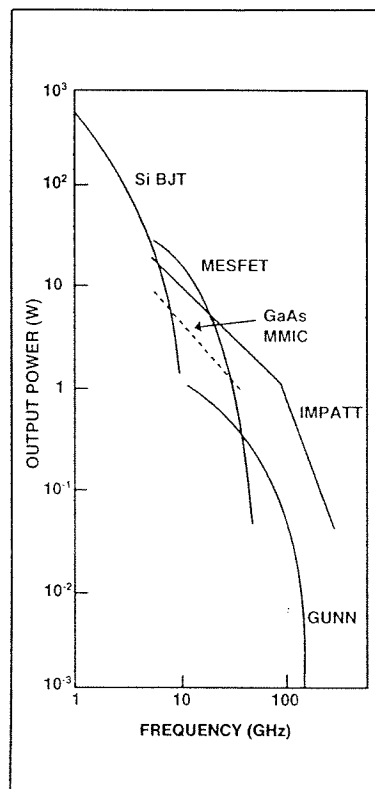


Figure 1.4 State-of-the-art performance of solid-state devices [30].

Frequency (GHz)	No. of Sources	Type	ERP (W)	Power (mW)	Efficiency (%)	Reference
8.3	18	Gunn	—	123	—	[23]
12.0	6	FET	—	0.4	—	[23]
55.8	3	Gunn	—	+3 dB [†]	—	[24]
9.6	16	Gunn	22	415	1.0	[17]
8.2	16	FET	10	184	26.0	[17]
9.7	25	FET	20.7	464	14.5	[13]
3.1	36	FET	3.0	220	22.0	[14]
5.0	100	FET	21	550	20.0	[15]
11.6	16	FET	15	335	20.0	[16]
17.0	36	FET	3.3	235	7.0	[16]
6.0	16	FET	28.2	—	—	[21]
34.7	36	HBT	0.170	—	—	[18]
9.9	200	HBT	6.3	—	—	[19]
60.0	8	IMPATT	23	1400	3.6	[22]
9.2	16	FET	27.6	1480	21.0	[Chapter 5]
9.8	100	FET	657	10300	23.1	[Chapter 5]

Table 1.1 Examples of quasi-optical power combiners and their reported total radiated power.

[†] power increase over a single oscillator

when designing for maximum power include device characteristics, device load impedance and feedback loop gain optimization, heat dissipation, device biasing, and grid edge effects. Since the design of power oscillators is in itself a rapidly evolving subject, particularly with respect to commercial CAD software, non-proprietary public-domain techniques were chosen whenever possible to predict and optimize oscillator power. This avoids using “black box” solutions that are impossible to duplicate by others without access to a particular version of CAD software. Fortunately, simple load-line analysis and linear theory for oscillator power prediction are often surprisingly accurate [31] and serve as a solid founda-

tion for future work in this area.

1.4 ORGANIZATION OF THE THESIS

This thesis consists of two main sections. Chapters 2 and 3 discuss grid mixers. Two grid mixer designs are developed, one for use as an X-band down-converter, and the second, a monolithic design, for use as a 1.6 THz tunable signal source or upconverter. The second section, chapters 4 and 5, is concerned with the design of grid oscillators for maximum power. Experimental results for four power grid oscillator designs are included.

Chapter 2 describes the theoretical performance of grid mixers and the way we approach their design. Modelling of quasi-optical grid mixers is detailed using simple equivalent transmission-line circuits derived from the EMF method analysis developed by Robert Weikle [32], and the *Hewlett-Packard High Frequency Structure Simulator* (HFSS) [33]. Finally, an X-band grid mixer for use as a downconverter is discussed and experimental results are compared with theory.

In chapter 3, the design of a monolithic 1.6 THz sideband generator grid is presented. Several techniques for extracting equivalent circuits for the embedding impedance presented to a device connected at points internal to the grid unit cell are discussed. Theory is developed to allow the use of the *Hewlett-Packard High Frequency Structure Simulator* to extract equivalent circuit models for arbitrary shaped unit cell patterns. Two sideband generator designs are presented, one suitable for use with a quartz substrate, and the other for use with a GaAs substrate. These designs are being used by the Semiconductor Device Group at the University of Virginia to fabricate monolithic grids for applications in terahertz upconversion and frequency multiplication. Several groups including the Max Planck Institute in Bonn, the University of Virginia, the Jet Propulsion Lab, and Caltech have expressed interest in obtaining these grids for further experimental research in terahertz technology.

Chapter 4 presents an overview of power oscillator design and develops tech-

niques for applying power oscillator design principles to quasi-optical grid oscillators. Issues discussed are thermal design, device load impedance optimization, compensation for device parasitic reactance, feedback loop gain optimization, and grid edge terminations. Several interesting structures are examined including the use of half-wave U-shaped strips as edge terminations, and meander lines for controlling feedback loop gain.

Four experimental power grid oscillators are the subject of chapter 5. The first grid uses only device load impedance optimization. The second grid includes compensation for device parasitics. The third grid adds feedback loop gain optimization to control the level of transistor saturation. The final grid includes all the optimization techniques from the previous grids but scales the grid size from 16 elements to 100 elements to produce a total radiated power of 10.3 W. This is 12.7 dB greater than the previous highest reported output power for a transistor grid oscillator. A discussion of oscillator noise patterns demonstrates the improvement in signal-to-noise ratio as the number of elements in the grid is increased.

In chapter 6, suggestions for future research on quasi-optical grid mixers and power oscillator and amplifier grids are discussed.

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Chapter 2

Grid Mixers

Power combining schemes involving solid-state devices quasi-optically coupled in free space have attracted attention as an efficient means of combining power at microwave and millimeter-wave frequencies [1]–[3]. In this chapter a Schottky diode grid mixer suitable for mixing or detecting quasi-optical signals is presented. The mixer is a planar bow-tie grid structure periodically loaded with diodes. A simple transmission-line model is used to predict the reflection coefficient of the grid to a normally incident plane wave. The grid mixer power handling and dynamic range scales as the number of devices in the grid. A 10 GHz 100-element grid mixer has shown an improvement in dynamic range of 16.3 to 19.8 dB over an equivalent single-diode mixer. The conversion loss and noise figure of the grid are equal to that of a conventional mixer. The quasi-optical coupling of the input signals makes the grid mixer suitable for millimeter-wave and submillimeter-wave applications by eliminating waveguide sidewall losses and machining difficulties. The planar property of the grid potentially allows thousands of devices to be integrated monolithically.

2.1 FUNDAMENTALS OF THE GRID MIXER

High-performance mixer research would appear to be falling out of favour recently, particularly at frequencies below the millimeter-wave band, because of the ready availability of low noise FET and HEMT amplifiers that make mixer performance a secondary consideration. While the availability of low-noise broad-

band amplifying devices has largely removed the need for ultra low-noise mixers below 100 GHz, a new performance issue, dynamic range, has become a critical factor in recent receiver designs. Indeed, microwave receivers today are often as severely limited by intermodulation and spurious responses as the last generation receivers were limited by noise [4]. An indication of the severity of the situation is revealed by a U.S. Navy initiative addressing current needs in its microwave electronics operational capability that places a high priority on the development of high-dynamic-range front-ends [5]. Thus, there is a need for mixer designs that can extend dynamic range.

Another active area of mixer research is in the development of new mixer circuit topologies that do not rely on elements such as baluns, transformers, and 3-dB hybrids. Such components are generally incompatible with monolithic microwave integrated circuits (MMICs) which favor planar circuits that can be photolithographically fabricated. The ability to manufacture a circuit with fine-line photolithographic precision is particularly critical for devices operating in the millimeter-wave band where circuit tolerances on the order of microns must be maintained.

A mixer design that addresses both these issues is the quasi-optical grid mixer. A grid loaded with diodes produces a nonlinear device suitable for mixing or detecting quasi-optical signals with improved dynamic range compared to conventional single-diode mixers. The grid mixer is ideally suited for photolithographic fabrication, making it an excellent candidate for monolithic integration on high-performance semiconductor substrates. It should be possible to manufacture the grid mixer as a planar monolithic circuit allowing a large number of diodes to be combined on a single wafer.

The planar grid mixer is shown in Figure 2.1. Diodes are loaded periodically in the grid, each diode defining a unit cell of the grid. There is a flat metal mirror behind the grid to act as a reactive tuning element. The grid mixer reflection

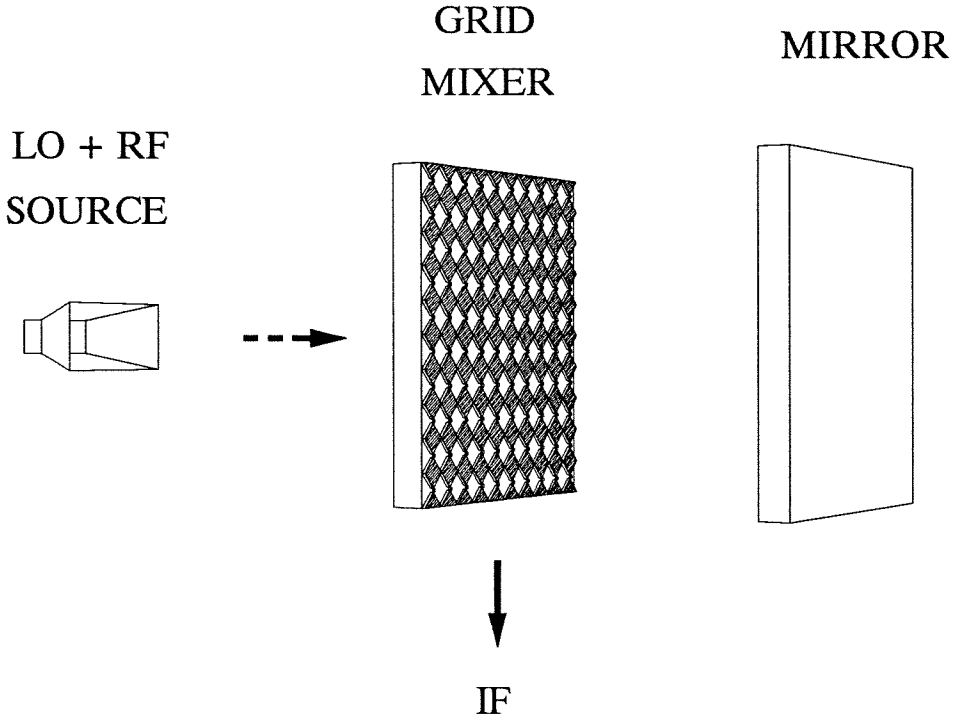
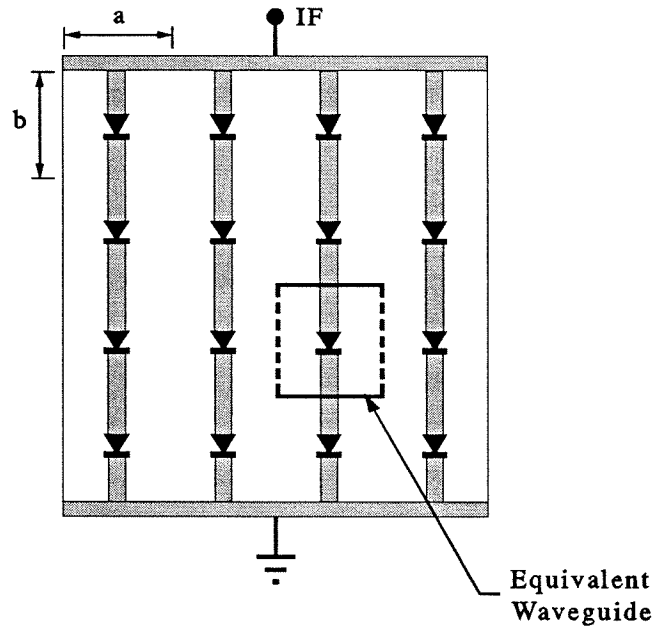


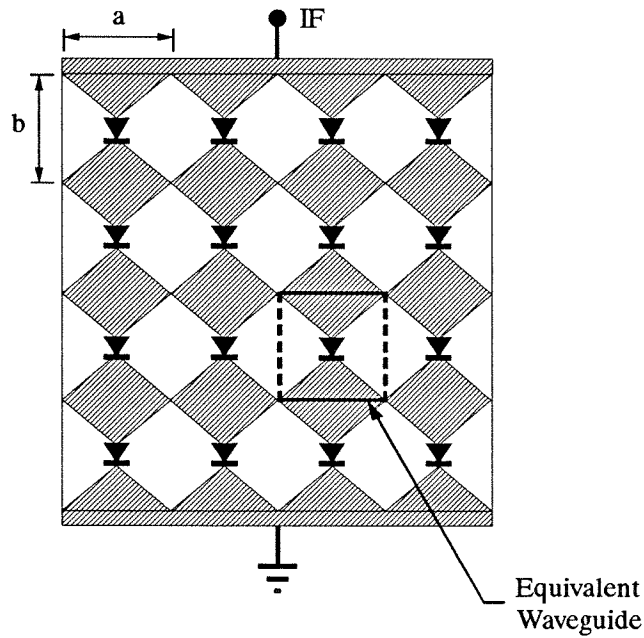
Figure 2.1 The grid mixer. The RF and LO signals couple to the diodes quasi-optically through the face of the grid. The IF signal is generated across the top and bottom grid edges. The mirror is used to tune out the capacitive reactance of the diodes for a better match to free space.

coefficient is optimized for incident signals at the design frequency by optimizing the dimensions and metal pattern of the unit cell and the electrical properties of the grid substrate. Diodes in each column are connected in series. The IF voltages add along each column and are collected at the diode terminals forming the top and bottom edges of the grid. A dc bias may also be applied at the grid edges. The symmetry of the grid cancels any RF currents along the horizontal rows.

Each diode in the array is presented with an embedding impedance which is a function of the grid structure repeated throughout each unit cell. Two grid designs that work well are the dipole (Figure 2.2(a)), consisting of a vertical strip running down the center of the grid unit cell with the diode bridged across a gap



(a)



(b)

Figure 2.2 (a) Grid mixer with dipole shaped metallization. The embedding impedance for this grid is primarily inductive. (b) Grid mixer with bow-tie shaped metallization. The grid embedding impedance for the bow-tie behaves like a short piece of transmission line.

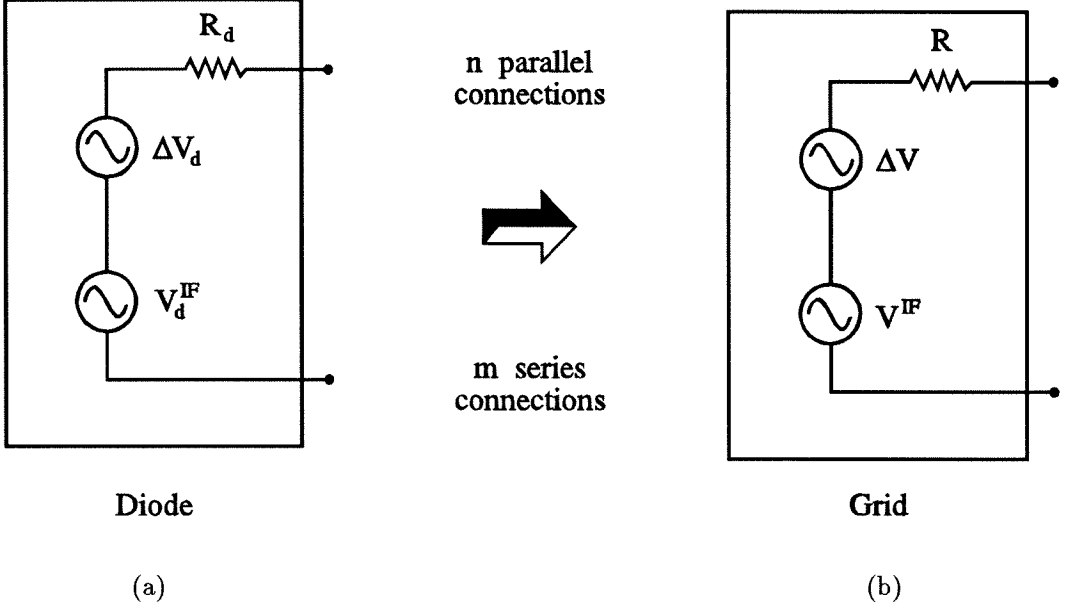


Figure 2.3 (a) Thevenin equivalent circuit for a single diode. (b) Thevenin equivalent circuit for the entire grid [6].

in the strip, and the bow-tie (Figure 2.2(b)) with the diode located at the apex of the two bow-ties.

In order to understand how the grid mixer improves signal power handling and dynamic range, we first need to investigate the noise performance of a grid of diodes. One might expect that the noise power of the grid mixer is the same as the noise power of a single-diode mixer because the individual noise powers from each diode are uncorrelated. Consequently, the noise figure of the grid mixer will be the same as an equivalent single-diode mixer. This can be shown mathematically if we look at the equivalent circuit of a single diode shown in Figure 2.3(a). A single diode can be represented as a Thevenin equivalent circuit with a source resistance R_d , in series with an rms noise voltage ΔV_d , and an rms IF signal voltage V_d^{IF} so that

$$P_d^{IF} = P_d^{RF} / L_C, \quad (2.1)$$

and

$$P_d^{IF} = \frac{(V_d^{IF})^2}{R_d}, \quad (2.2)$$

where L_C is the RF to IF conversion factor of the diode, a function of the local oscillator power, P_d^{IF} is the converted IF signal power, and P_d^{RF} is the RF signal power absorbed by the diode. If the diodes are connected in a rectangular grid with m rows and n columns, then there will be m diodes in series per column, and n diodes in parallel per row. Consequently, we can define a Thevenin equivalent circuit for the grid as shown in Figure 2.3(b), where the total resistance of the grid, R , is

$$R = R_d(m/n). \quad (2.3)$$

Assuming that the noise voltage of each diode is independent, then the total noise voltage across a series connection of m diodes is

$$\sum_{m} \Delta V_d = \sqrt{m} \Delta V_d, \quad (2.4)$$

and consequently the noise voltage of the grid, ΔV , is given by

$$\Delta V = \Delta V_d \sqrt{m/n}. \quad (2.5)$$

From which it follows that the noise power of the grid, ΔP , is

$$\Delta P = \frac{(\Delta V_d \sqrt{m/n})^2}{R_d(m/n)} \quad (2.6)$$

$$= \Delta P_d. \quad (2.7)$$

From this we can conclude that the noise power of the grid is the same as that of an equivalent single diode. That is, the noise figure of the grid mixer will be equal to the noise figure of a single diode mixer placed in an equivalent embedding circuit.

A similar line of reasoning can be used to show the conversion loss of the grid mixer is the same as that of an equivalent single diode. Namely, if P^{RF} is the

available power of the incoming RF signal to be converted to the IF frequency, then for the single diode case, using equation (2.1), we expect a converted IF power of

$$P_d^{IF} = P^{RF} / L_C. \quad (2.8)$$

The corresponding converted IF signal power for the $m \times n$ grid, P^{IF} , assuming the incoming RF power is distributed evenly among all the diodes in the grid, is given by

$$P^{IF} = \frac{(V^{IF})^2}{R} \quad (2.9)$$

$$= \frac{(mV_d^{IF})^2}{R} \quad (2.10)$$

$$= \frac{m^2(R_d P^{RF} / (L_C m n))}{R_d(m/n)} \quad (2.11)$$

$$= P^{RF} / L_C. \quad (2.12)$$

Comparing equations (2.8) and (2.12) shows that the converted IF power is the same for both the single diode and the grid for a given RF signal power. In other words, the conversion loss of the grid mixer is the same as for a single diode with the same embedding impedance. We have done this analysis for the conversion loss for the IF, but the same reasoning holds for any mixing product. In particular, the ratio of the third-order intermodulation products to the IF power is, for the grid, the same as that for a single diode. However, the total power for the grid scales with the number of diodes. This means that the third-order intercept scales as the number of diodes in the grid.

Finally, it is worthwhile to compare the power handling of the grid mixer to an equivalent single diode mixer. If we assume that the maximum RF input power that a single diode can safely handle is \tilde{P}_d^{RF} , and we assume uniform illumination of the grid mixer so that the incoming RF signal power is distributed

evenly among all diodes in the grid, then for our $m \times n$ grid, the maximum power handling of the grid mixer, \tilde{P}^{RF} is simply

$$\tilde{P}^{RF} = mn\tilde{P}_d^{RF}. \quad (2.13)$$

In other words, the power handling scales with the number of devices in the grid.

This reveals an important property of the grid mixer, its ability to increase dynamic range without compromising sensitivity. We have shown that since the RF power is spread among all the devices, the saturation power of the grid is increased by a factor of the number of devices. However, the noise figure of the grid remains equal to that of a single-diode mixer. Consequently, the dynamic range is increased by a factor of the number of devices in the grid as well. Of course, the trade-off is that the required local oscillator power is also raised by the same amount. This trade-off between dynamic range and local oscillator power is one that occurs in virtually all mixers. The advantage of the grid is that we can increase the local-oscillator power, and hence dynamic range, virtually without limit by increasing the number of diodes in the grid. At the same time, the conversion loss and noise figure of the grid can be independently optimized by adjusting the local-oscillator power per diode. This decoupling of sensitivity and power handling makes the grid mixer particularly attractive for SIS mixer designs where power handling of the nonlinear element is fundamentally limited [7].

As mentioned, the primary disadvantage of the grid mixer is that in order to maintain the same local-oscillator power per diode, the total incident local-oscillator power on the grid must also be scaled with the number of diodes in the grid. Consequently, for large grid mixers, a suitable high-power local-oscillator source must be available to get the best performance possible from the mixer diodes. One possible source suitable for the grid mixer local oscillator is the power grid oscillator. Such a source is the topic of the second part of this thesis. The grid oscillator output power also scales with the number of devices in the

grid, so it is a natural counterpart to the grid mixer. It is also reasonable to think of using a chain of quasi-optical grid amplifiers as a high-power local-oscillator source. Grid amplifiers suitable for this task have already been demonstrated [8,9]. Using grid amplifiers, the signal source could even be a conventional low-power oscillator feeding a horn antenna, which would allow integration of existing conventional local oscillators into a quasi-optical receiver.

2.2 GRID MIXER TOPOLOGIES

There are two basic configurations that can be used when designing a grid mixer. Depending on the application, the LO and RF signals may be combined quasi-optically before being directed onto the grid mixer surface as shown in Figure 2.4. This has the advantage that if the grid is orientated so that the diode side faces the mirror, the substrate can then be used as an impedance transformer to improve the match between the diodes and free space. This technique will be discussed in greater detail in section 2.3.

Alternatively, the LO and RF signals can be kept isolated from each other. For example, the RF might be incident from the back surface of the grid, and the LO signal incident from the front. Bandpass filter grids on either side of the grid mixer could then be used to isolate the LO from the RF as shown in Figure 2.5. This design has the advantage that the grid mixer can be tuned to optimize the reflection coefficient at both the LO and RF frequencies independently by adjusting the properties and position of the bandpass filter grids. This design is also potentially more convenient for use in a quasi-optical receiver where the RF signal would first pass through a grid amplifier in front of the grid mixer, and the LO would be generated by an LO source and a chain of grid amplifiers or a grid oscillator behind the grid mixer.

Once the basic grid mixer configuration is established, the design of the unit cell metal pattern must be considered. The choice of the unit cell metal pattern affects the embedding impedance presented to the diode in the grid. The use of

narrow strips results in a predominantly inductive embedding impedance, which can be useful for resonating out the junction capacitance of the diode to obtain a better impedance match with free space. This results in a narrowband design that will typically have bandwidths on the order of a few percent of the fundamental frequency. Fortunately, at millimeter-wave frequencies this can still be several GHz, a large bandwidth by microwave standards.

If a bow-tie pattern is chosen, the embedding impedance resembles a shunt section of low-impedance transmission. The electrical length of the transmission line is only a fraction of a wavelength making the bow-tie suitable for broadband circuits if the diode has a small junction capacitance. In cases where bandwidth and impedance match are both critical, a combination of a bow-tie and a strip can be used to help tune out diode capacitance without sacrificing too much bandwidth or excessively degrading grid return loss.

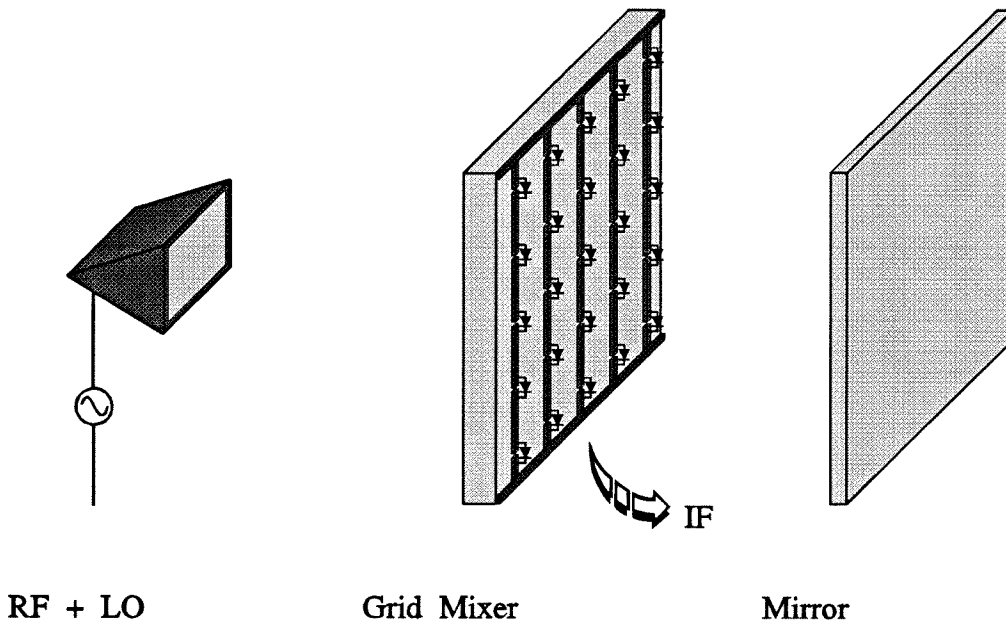


Figure 2.4 One-sided grid mixer configuration where the LO and RF signal beams are combined prior to being directed onto the grid mixer surface. In this case, LO and RF isolation is the responsibility of the external beam combiner.

2.3 GRID MIXER EQUIVALENT CIRCUIT MODELS

At the RF and LO frequencies, the quasi-optical grid mixer can be modelled as a three-port network. Ports 1 and 2 are respectively the front and back of the grid itself, and the third port is the location in the grid unit cell where the diode is mounted. Obtaining the three-port scattering parameters of an arbitrary quasi-optical grid mixer is a challenging problem. To date, solutions for arbitrary shaped unit cell metal patterns are still not available. However, significant progress has been made for specific metal patterns such as bow-ties and strips for grids assumed to be infinite in extent [10]. Solutions of this type make use of grid symmetry to reduce the problem of analyzing the entire grid to the simpler analysis of an equivalent waveguide unit cell. The equivalent waveguide

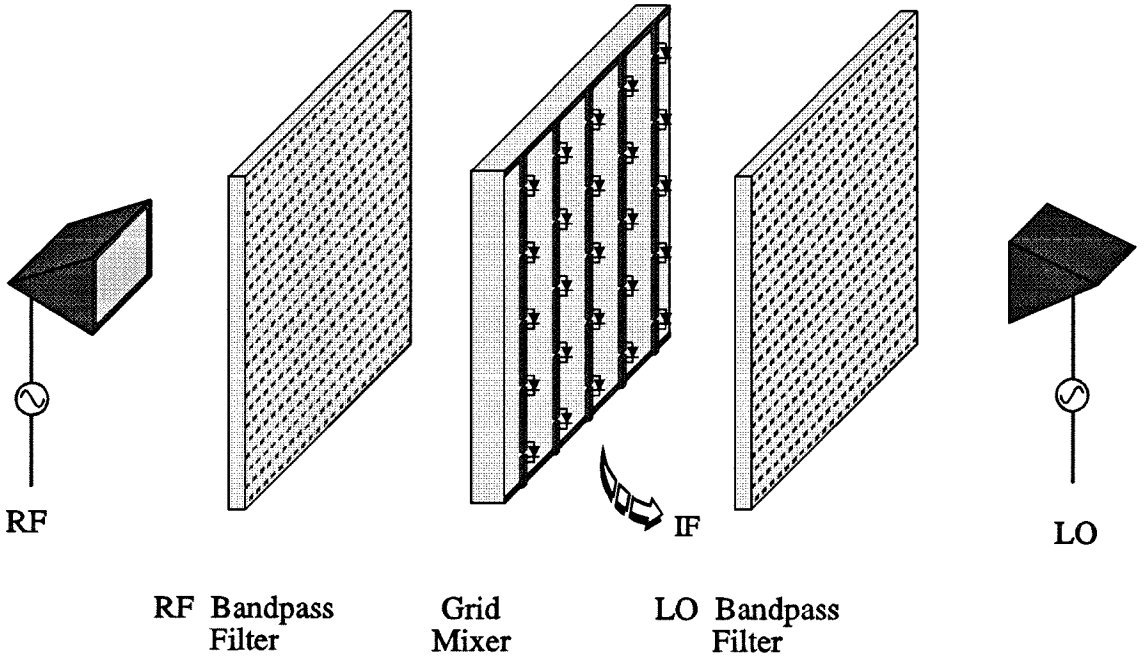


Figure 2.5 Two-sided grid mixer configuration where the LO and RF are kept separate and are incident on the front and back surfaces of the grid mixer respectively. Bandpass filter grids are used to isolate the LO and RF signal beams.

can then be solved using techniques developed for the analysis of structures placed inside waveguides, or by the use of numerical three-dimensional finite-element electromagnetic solvers. Solutions of this type, because they assume grids of infinite extent, completely ignore grid edge effects. Nevertheless, they have been found to provide reasonably good accuracy.

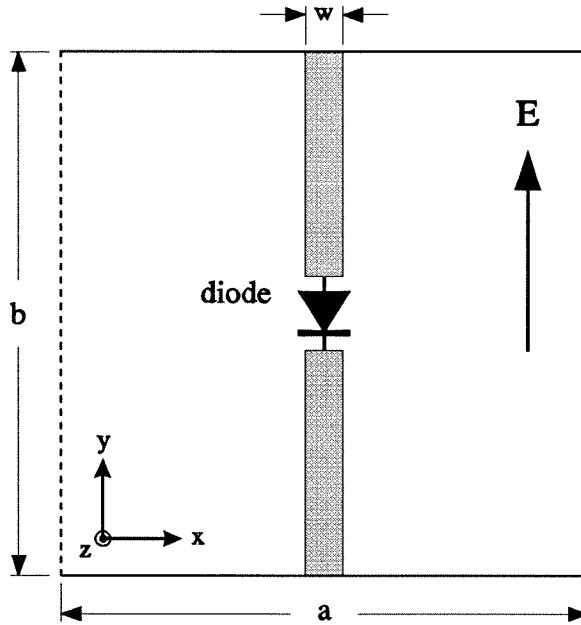
We begin the equivalent waveguide unit cell analysis by assuming an infinite grid with a uniform plane wave normally incident upon the grid surface. Symmetry then allows us to replace the walls of the unit cell in the grid with electric and magnetic walls to form an equivalent waveguide unit cell. For the case of vertical electric field polarization, this waveguide has magnetic walls on the sides and electric walls on the top and bottom, as shown in Figure 2.6(a). The walls extend in the $+z$ and $-z$ directions, with the diodes in the $z = 0$ plane. In effect, this reduces the problem of analyzing the grid to that of analyzing an equivalent waveguide with electric and magnetic walls. The propagating mode is TEM, and the evanescent modes couple to the currents in the unit cell metal pattern.

For simple geometric metal patterns like the strip and bow-tie, the impedance presented to the terminals of a diode in the grid can be found by following a procedure similar to the EMF analysis in the paper by Eisenhart and Kahn [11]. This approach is valid only for grid unit cell sizes that are small compared to a wavelength. The calculations are described in detail by Weikle [10], and only the final results will be repeated here.

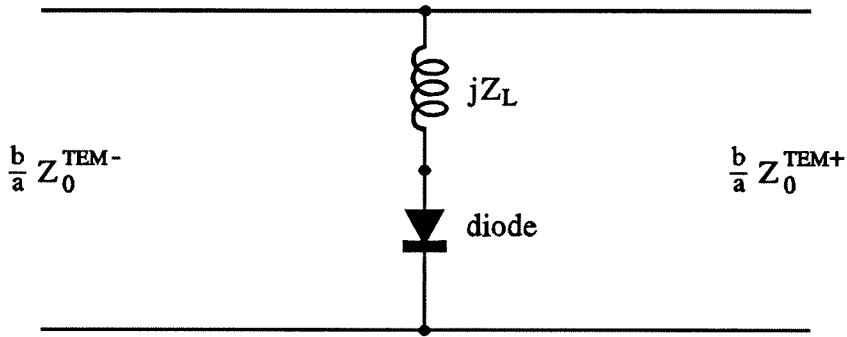
For a unit cell with a vertical strip of width w , (Figure 2.6(a)), the equivalent circuit is a simple shunt inductor, L , (Figure 2.6(b)) whose reactance can be computed using

$$Z_L = \frac{2b}{a} \sum_{m=1}^{\infty} \cos^2\left(\frac{m\pi}{2}\right) \operatorname{sinc}^2\left(\frac{m\pi w}{2a}\right) (Z_{m0}^{\text{TE}+} \parallel Z_{m0}^{\text{TE}-}), \quad (2.14)$$

where $Z_0^{\text{TEM}} = \sqrt{\mu/\epsilon}$, and $Z_{mn}^{\text{TE}} = \omega\mu/k_z$, and k_z is the propagation constant and



(a)



(b)

Figure 2.6 (a) Simple vertical strip unit cell. Boundary conditions are imposed by the grid symmetry. The solid lines (—) are electric walls ($E_{\text{tangential}} = 0$) and the dashed lines (---) are magnetic walls ($H_{\text{tangential}} = 0$). (b) Simplified equivalent circuit model for the vertical strip grid mixer. The diode is modelled using the manufacturer's equivalent circuit.

is given by

$$k_z = \sqrt{\omega^2 \mu \epsilon - \left(\frac{m\pi}{a}\right)^2 - \left(\frac{n\pi}{b}\right)^2}. \quad (2.15)$$

For a unit cell with a bow-tie metal pattern, shown in Figure 2.7(a), the equivalent circuit is a shunt transmission line of characteristic impedance, Z_{BT} , and electrical length, θ_{BT} , as shown in Figure 2.7(b). These values are given by

$$Z_{BT} = \sqrt{\frac{Z}{Y}} \quad (2.16)$$

$$\theta_{BT} = \sqrt{ZY}, \quad (2.17)$$

where

$$Z = \frac{1}{ab} \sum_{\substack{m=1 \\ n=0}}^{\infty} 2\epsilon_{0n} \frac{k_c^2}{k_x^2} A_{mn}^2 (Z_{mn}^{\text{TE}+} \parallel Z_{mn}^{\text{TE}-}), \quad (2.18)$$

$$A_{mn} = \frac{\int_0^b \int_0^\phi \frac{\cos(k_x y \tan \psi)}{\sqrt{\sin^2 \phi - \sin^2 \psi}} \cos k_y y \, d\psi dy}{\int_0^\phi \frac{d\psi}{\sqrt{\sin^2 \phi - \sin^2 \psi}}}, \quad (2.19)$$

$$Y = \frac{1}{ab} \sum_{\substack{m=0 \\ n=1}}^{\infty} 2\epsilon_{m0} \frac{k_c^2}{k_y^2} B_{mn}^2 (Y_{mn}^{\text{TM}+} + Y_{mn}^{\text{TM}-}), \quad (2.20)$$

$$B_{mn} = \frac{\int_0^a \int_0^\theta \frac{\cos(k_y x \tan \xi)}{\sqrt{\sin^2 \theta - \sin^2 \xi}} \cos k_x x \, d\xi dx}{\int_0^\theta \frac{d\xi}{\sqrt{\sin^2 \theta - \sin^2 \xi}}}, \quad (2.21)$$

and $Y_{mn}^{\text{TM}} = \omega \epsilon / k_z$, $k_x = m\pi/a$, $k_y = n\pi/b$, $k_c^2 = k_x^2 + k_y^2$, and

$$\epsilon_{mn} = \begin{cases} 1, & \text{if } m = n; \\ 2, & \text{otherwise.} \end{cases} \quad (2.22)$$

For design purposes, we generally want to find the reflection coefficient of an infinite grid for a plane wave at normal incidence on the front surface of the

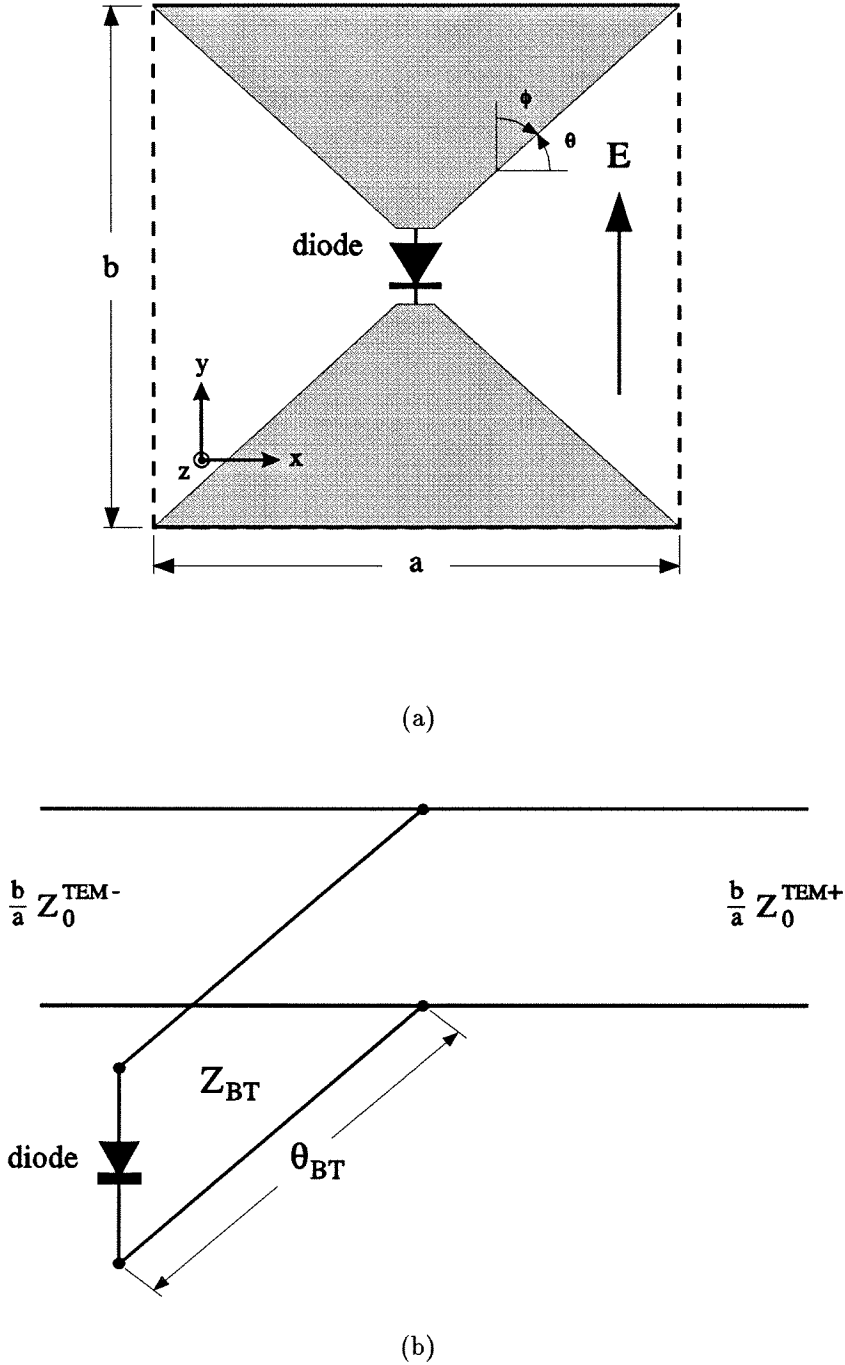
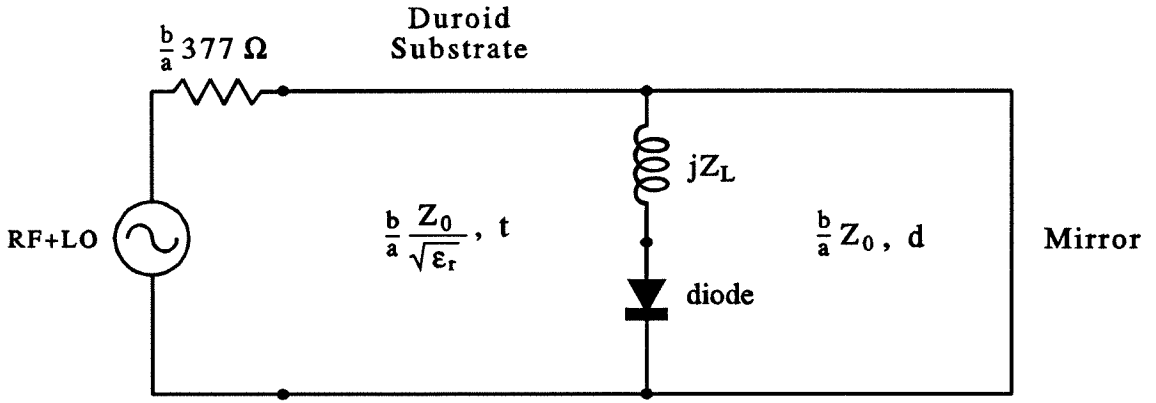


Figure 2.7 (a) Simple bow-tie unit cell. Boundary conditions are imposed by the grid symmetry. The solid lines (—) are electric walls ($E_{\text{tangential}} = 0$) and the dashed lines (---) are magnetic walls ($H_{\text{tangential}} = 0$). (b) Simplified equivalent circuit model for the bow-tie grid mixer. The diode is modelled using the manufacturer's equivalent circuit.

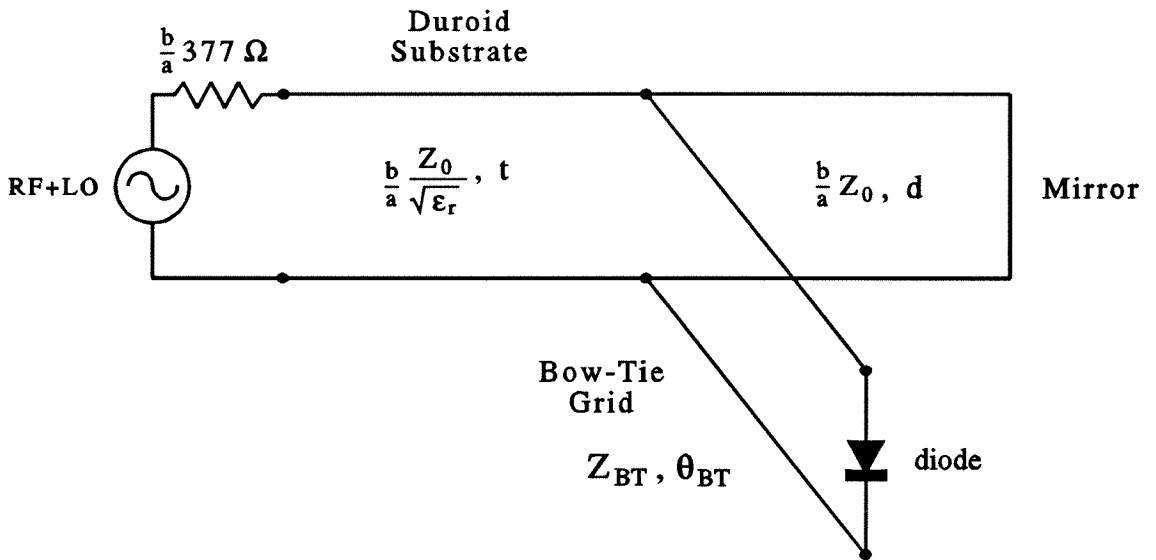
grid. For the purpose of this discussion, it is reasonable to assume that we have the configuration shown in Figure 2.4, that is, a mirror behind the grid with the diodes facing the mirror. The case of the two-sided grid mixer shown in Figure 2.5 can be handled similarly; one need only add the two-port s -parameters of the bandpass filter grids to complete the model.

The equivalent circuit for the grid mixer with a mirror a distance d behind the grid is shown in Figure 2.8 where the circuit shown in Figure 2.8(a) is for a vertical strip unit cell, and the circuit in Figure 2.8(b) is for a bow-tie shaped unit cell. As described earlier, the grid is modelled as a three-port network. Ports 1 and 2 are respectively the front and back of the grid, and the third port is defined at the diode terminals, where the diode is mounted to the grid. The incident LO+RF TEM mode signal is modelled as a $377\,\Omega$ source connected to port 1. The mirror placed behind the grid terminates port 2 in a short-circuited stub, and port 3 is terminated by the mixer diode. The entire grid is in this way reduced to a one-port equivalent circuit. A transmission line represents the propagating TEM mode as it passes through the substrate which supports the grid. As mentioned previously, the bow-tie grid is modelled as a short section of transmission line with characteristic impedance Z_{BT} and electrical length θ_{BT} . Values for Z_{BT} and θ_{BT} are obtained from equations (2.16, 2.17) derived using the EMF analysis. Similarly, the strip is modelled as a shunt inductor with reactance Z_L , given by equation (2.14).

The diode is added to the grid model by using the manufacturer's equivalent circuit. Modelling the nonlinear behaviour of a mixer diode is a difficult problem, and most of the popular commercially available harmonic balance software is inadequate for accurately characterizing the behaviour of mixers [4]. To make matters worse, the models used by such software are almost always proprietary, which makes their use in an academic environment of limited value. Fortunately, most diode manufacturers provide a linear equivalent circuit for the RF and



(a)



(b)

Figure 2.8 (a) Transmission line model for the grid configuration of Figure 2.4 with (a) vertical strip unit cell metal pattern, (b) bow-tie unit cell metal pattern.

LO frequencies that can be used to design efficient matching networks to give good mixer performance. While such simple linear models cannot be used to predict conversion loss or intermodulation characteristics of the mixer, they are nevertheless invaluable in designing the RF, LO and IF sections of the mixer embedding network for optimum mixer performance.

Simulation of the grid is carried out by calculating the reflection coefficient the grid presents to the RF and LO source connected to port 1. The design is optimized by matching the grid impedance to free space ($377\ \Omega$) at the design frequency of the mixer.

2.4 AN X-BAND GRID MIXER

A grid mixer designed to test the theoretical performance improvements of the quasi-optical grid mixer concept was constructed for operation at X-band [12]. This frequency was chosen because it allows grid dimensions to be used that are large enough that a hybrid construction technique using discrete beam-lead diodes epoxied to a copper-clad microwave substrate can be used.

The diodes chosen for the grid are commercially available Hewlett-Packard low-barrier Schottky beam-lead diodes (HSC-5332) suitable for mixers and detectors operating through the *Ku*-band [13]. The equivalent circuit for the diode was obtained from the manufacturer and is shown in Figure 2.9. During the design phase, a number of grid configurations were simulated using *Puff*, a linear microwave circuit modelling tool for the IBM PC developed at Caltech [14]. The grid design was optimized for the best impedance match to free space ($377\ \Omega$) at 10 GHz. Both the vertical strip and the bow-tie unit cell pattern were simulated. In each case, the unit cell dimensions, substrate thickness and dielectric constant, and mirror position were varied to try to obtain the best possible impedance match. In the case of the bow-tie shaped unit cell, plots of bow-tie characteristic impedance and electrical length (Figure 2.10) were used to speed up the analysis as the bow-tie computations are quite lengthy.

The best impedance match was obtained on a Duroid dielectric substrate 3.2 mm thick with a relative dielectric constant $\epsilon_r = 10.5$, using a 3-mm square bow-tie unit cell, and with a mirror 1.7 mm from the face of the grid. The theoretical free-space reflection coefficient is shown in Figure 2.11. The predicted 10-dB bandwidth is 1 GHz, and the reflection coefficient is -23 dB at 10 GHz.

A 10×10 grid mixer mask was designed using the optimized unit-cell dimensions. In order to accommodate the physical length of the beam-lead diodes, the bow-ties were pulled apart by 0.3 mm at the apex. This gave the unit cell a rectangular shape and theoretically results in a 10% increase in the free-space characteristic impedance. This change was assumed to be negligible and was not compensated for in the model. Figure 2.12 shows the artwork used to generate the mask for the grid. Figure 2.13 shows a photo of the assembled grid. Silver epoxy was used to bond the diodes to the Duroid substrate.

The design of the IF feed was somewhat difficult as it had to connect across

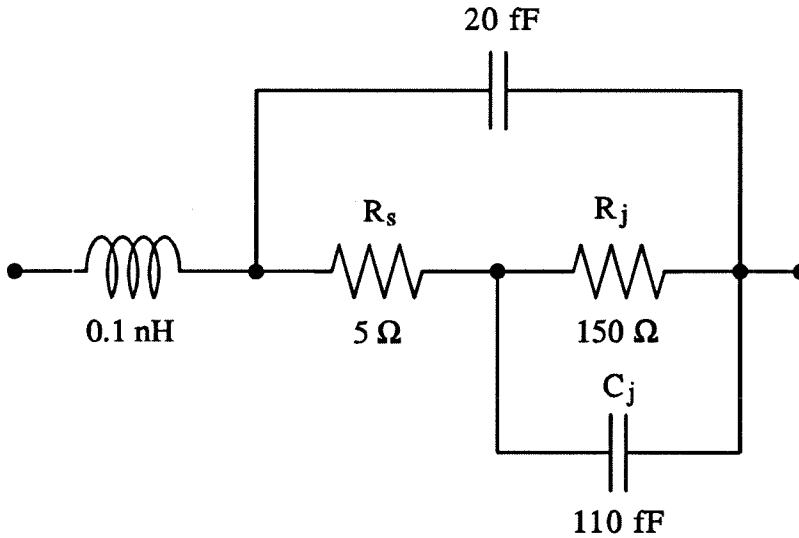


Figure 2.9 Equivalent circuit for the Hewlett-Packard HSCH-5332 Schottky beam-lead diode at 10 GHz with a 1 mA dc bias [13].

the top and bottom edges of the grid, a distance of over 33 mm for the 10×10 grid mixer. The layout settled upon uses an empirically-designed exponential taper at the top edge of the grid to “funnel” the grid edge to a point which can then be soldered to the center conductor of the IF coaxial cable. At the opposite end of the grid, a flexible copper sheet, the width of the entire grid, was soldered between the grid edge and the mirror behind the grid as shown in Figure 2.14. The mirror thus served as a return ground for the IF current. By attaching the outer conductor of the IF coaxial cable to the mirror, the IF circuit was completed. The use of the flexible copper sheet allowed the mirror position to still be tuned over a limited range without interference. It was hoped that by adjusting the diode bias current, a good match to the $50\ \Omega$ IF coaxial cable would be possible.

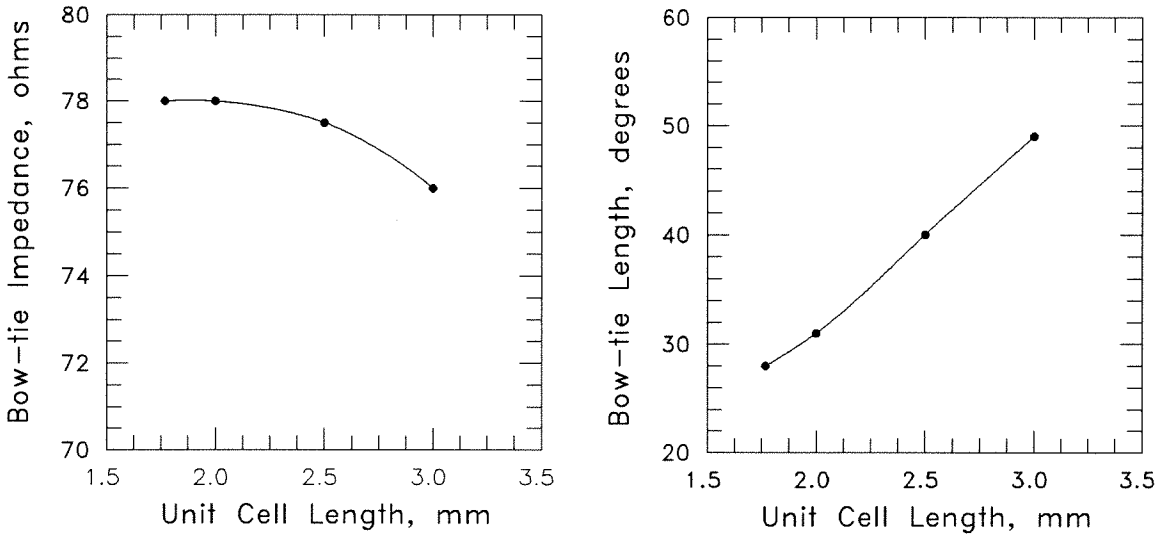


Figure 2.10 Bow-tie characteristic impedance, Z_{BT} , and electrical length, θ_{BT} , as a function of unit cell size, a , at 10 GHz for a substrate with $\epsilon_r = 10.5$ and thickness 3.2 mm.

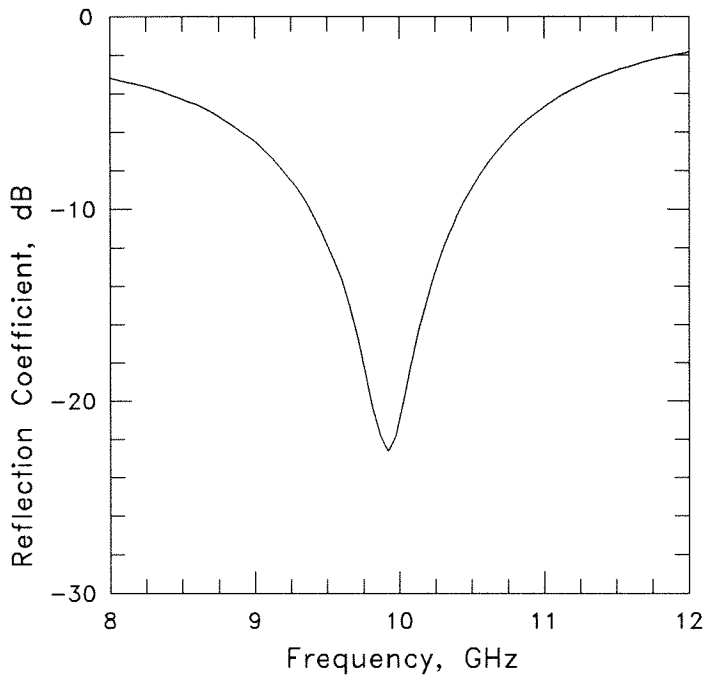


Figure 2.11 Theoretical grid mixer reflection coefficient using the transmission line model developed for the grid and the Schottky diode model provided by the manufacturer.

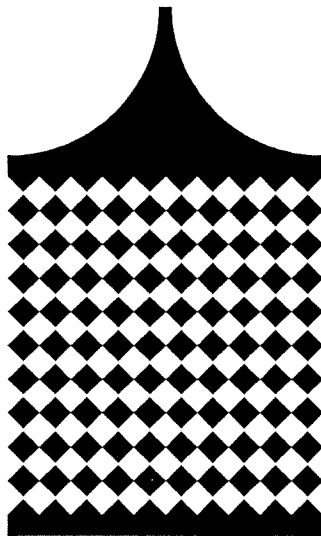


Figure 2.12 Artwork for the X-band grid mixer mask.

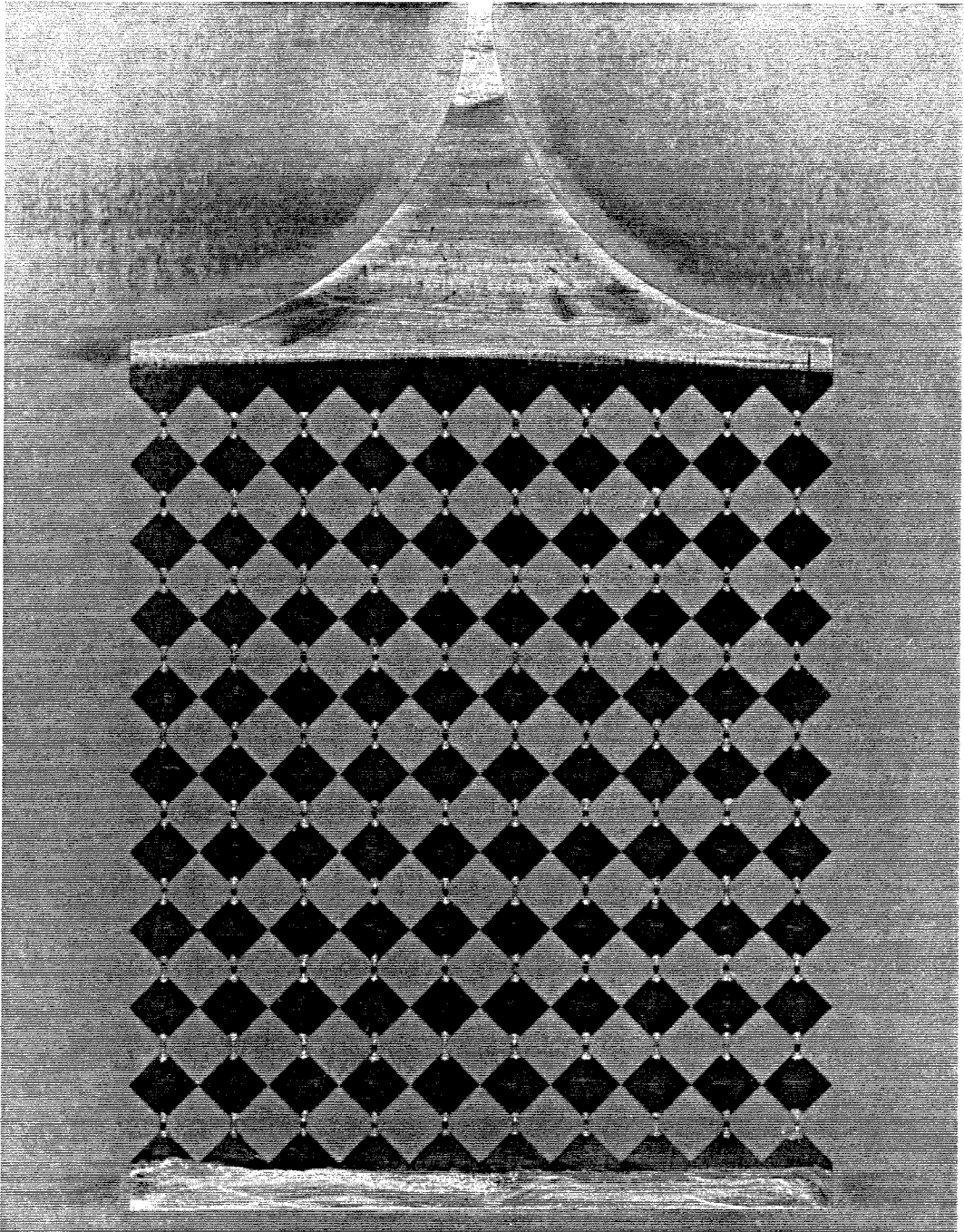


Figure 2.13 Photograph of the 100 element X-band grid mixer. The unit cell width is 3 mm. The incident RF and LO electric fields are polarized vertically. The IF signal is taken off the top and bottom edges of the grid. The diodes are bonded to the grid with silver epoxy.

2.5 X-BAND GRID MIXER MEASUREMENTS

The grid reflection coefficient was measured using a three-term error corrected diffraction-limited quasi-optical reflectometer. The reflectometer consisted of a broadband horn placed inside an anechoic chamber and connected to an HP 8510 network analyzer as shown in Figure 2.15. The grid was positioned approximately 300 mm from the face of the horn during the measurement. The reflectometer was calibrated using three known standards, a short, a delayed short, and a matched load, in place of the grid. A mirror was used as the short, and a piece of Emerson and Cuming Eccosorb AN-74 absorber served as the matched load.

A measurement of the grid reflection coefficient at three different mirror positions using the quasi-optical reflectometer was found to be in reasonable agreement with theory as shown in Figure 2.16(a)–(c). Reflectometer calibration error is the likely cause of the reflection magnitude exceeding unity above 11 GHz. Later experiments with a lens-focused reflectometer gave better results [15], but

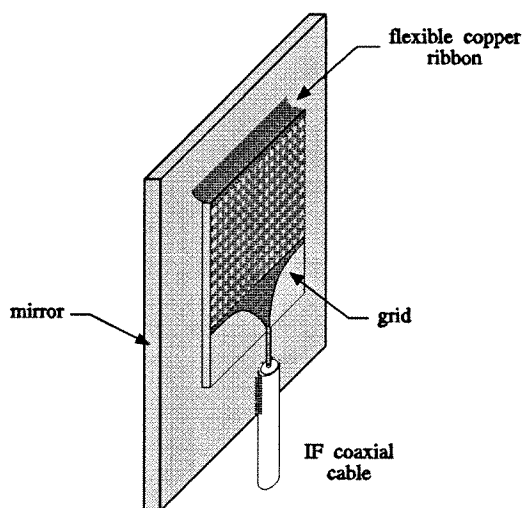


Figure 2.14 IF feed structure for the X-band grid mixer.

such a system was unavailable at the time of these measurements. Figure 2.16(d) shows the measured IF return loss. A dc bias current of $450\text{ }\mu\text{A}$ per diode was required to match the IF impedance to $50\text{ }\Omega$.

Previously, we showed that the conversion loss of the grid mixer is the same as a single-diode mixer in an equivalent embedding impedance. For the purpose of comparison, a single-diode microstrip mixer was designed and built with a diode of the same type used in the grid (Figure 2.17). This allows us to compare the performance of the grid to that of an equivalent single-diode mixer. The microstrip mixer employs transmission line matching circuits for the RF/LO and IF sections of the mixer [16]. The RF and LO signals were combined externally using a hybrid coupler to simplify the design. A dc bias was applied to the mixer diode through a bias-tee connected to the IF port.

We define the conversion loss of the grid mixer as the power of the IF signal at the IF port divided by the total RF power incident upon the grid surface. For

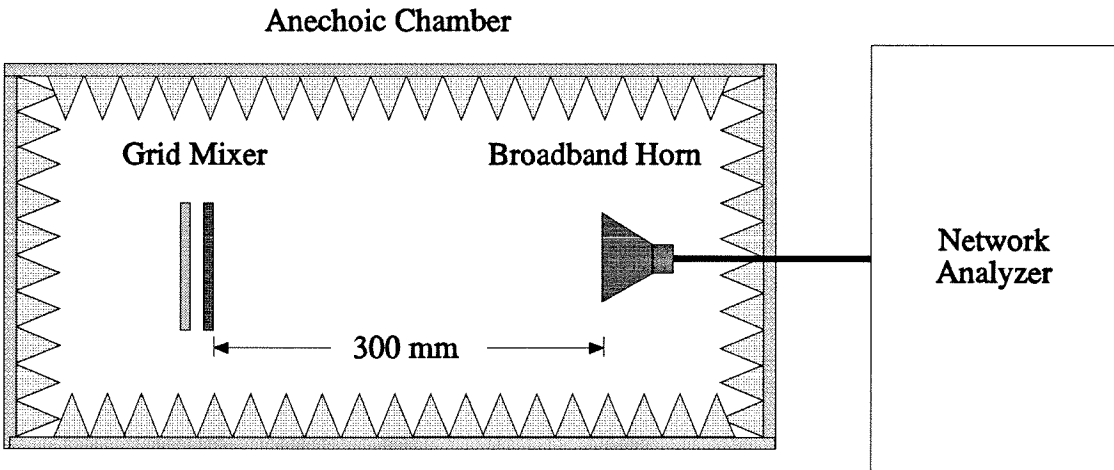


Figure 2.15 Diffraction limited quasi-optical reflectometer. Calibration was done with a short, a delayed short, and a matched load. The short was a mirror, and the load was a piece of microwave absorber.

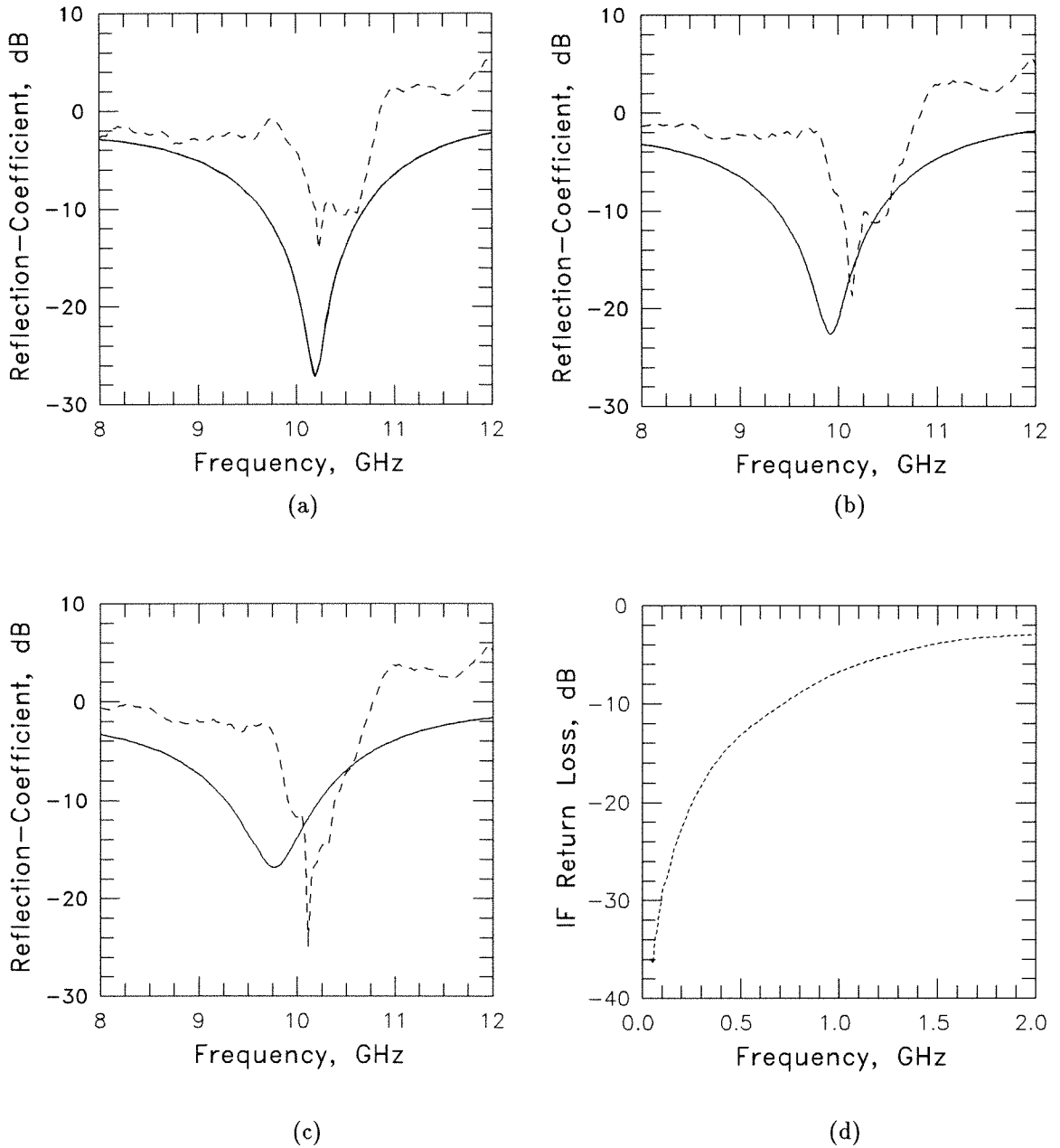


Figure 2.16 (a) Theoretical (—) and measured (---) grid mixer reflection coefficient for mirror separations of (a) 1.2 mm (14.6°), (b) 1.7 mm (20°), (c) 2.1 mm (25.4°) with a dc bias of $450\ \mu\text{A}$ per diode. The theoretical curve was obtained using the transmission line model developed for the grid, and the model provided by the manufacturer of the Schottky diode. (d) Measured grid mixer IF return loss with a dc bias of $450\ \mu\text{A}$ per diode.

the conversion loss and noise figure measurements, the RF and LO signals were combined and fed to a single broadband horn. In order to accurately compute the incident RF and LO power densities at the grid surface, a calibration was made by removing the grid and placing an identical receive horn at twice the distance from the transmit horn. A measurement of the total system path-loss between the two horns with a network analyzer determined the horn gain and free space path-loss allowing an accurate computation of the power density at the grid surface. The power incident upon the grid was then defined as the product of the power density at the grid surface and the area of the grid. Thus, the grid conversion loss and noise figure measurements will also include any mismatch loss between the grid mixer and free space.

Figure 2.18 shows how the conversion loss was measured. Two signal generators generate the RF and LO signals, which are combined and sent to the

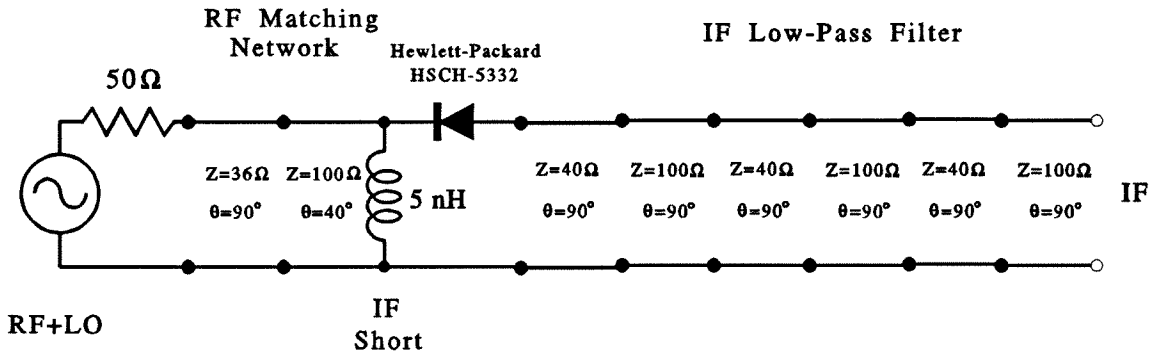


Figure 2.17 Schematic of the microstrip mixer used for comparison with the grid mixer. The electrical lengths are specified at the LO design frequency. The IF low-pass filter provides a short at the RF/LO frequency. The lumped inductor shorts the RF/LO port at the IF frequency. The RF and LO signals are combined externally with a hybrid coupler. A dc bias was applied to the diode through a bias-tee connected to the IF port.

transmit horn. We define the conversion loss by the equation

$$P_{IF} = \frac{P_t}{L_C} \left(\frac{GA}{4\pi r^2} \right), \quad (2.23)$$

where P_{IF} is the converted IF signal power and P_t is the RF signal generator power. G is the gain of the transmitting horn, A is the physical area of the grid mixer, and r is the distance between the horn and the grid. The term in parentheses is the space-loss factor. To compute the conversion loss, we first measure the received power between two identical horns at twice the grid-horn separation to establish a calibration power P_c given by

$$P_c = \frac{P_t G^2 \lambda^2}{(4\pi)^2 (2r)^2}. \quad (2.24)$$

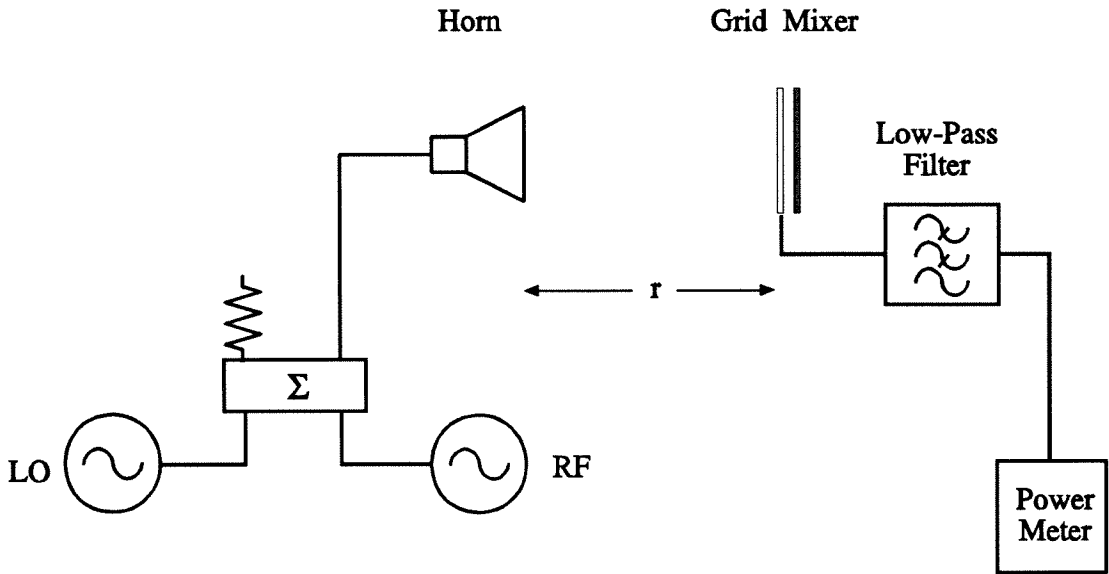
From these two equations we can write an expression for the conversion loss

$$L_C = \frac{P_c}{P_{IF}} \frac{16\pi A}{G\lambda^2}. \quad (2.25)$$

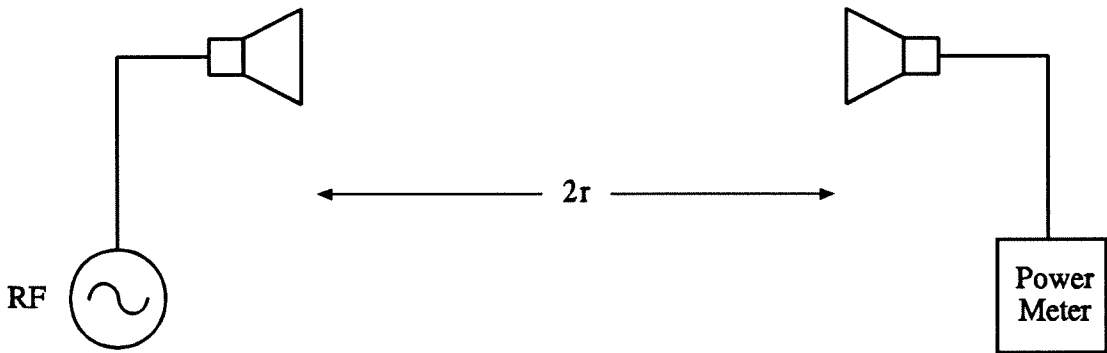
This simple formula allows us to calculate the conversion loss of the mixer from a relative power measurement and three well-known parameters. In our measurements r was 310 mm and A was 990 mm².

Figure 2.19(a) shows the measured conversion loss of the grid mixer as a function of local oscillator power per diode for a combined 10.225 GHz LO signal and a 10.439 GHz RF signal normally incident upon the grid. Figure 2.19(a) also shows the measured conversion loss of the equivalent single-diode microstrip mixer. The results verify that the grid mixer conversion loss is nearly equal to the single-diode mixer. The difference can be attributed to the slightly unequal impedances presented to the diodes for the two mixer designs. A grid conversion loss of 7.9 dB was measured for a local oscillator power of -4 dBm per diode.

The frequency response of the grid conversion loss is shown in Figure 2.19(b) for a local oscillator power of -20 dBm per diode. Again, the performance of the equivalent single-diode mixer is included for comparison. The grid is band-limited by the reactive mirror tuning element.



(a)



(b)

Figure 2.18 (a) Measuring the grid mixer conversion loss. The gain of the horn is about 10 dB at these frequencies. (b) Calibration measurement with another horn substituted for the grid at twice the grid-horn separation.

In order to measure the noise figure of the grid, a Hewlett-Packard 8970 Noise Figure Meter was modified to allow quasi-optical noise figure measurements (Figure 2.20). The noise figure calibration was identical to that used for the grid mixer conversion loss measurement. The grid was placed in an anechoic chamber to shield the measurement system from external disturbances. Figure 2.21 shows the measured noise figure of the grid for a local oscillator power of -20 dBm per diode. Again, the performance of the equivalent single-diode mixer is included for comparison. The results verify that the grid mixer noise figure and the single-diode mixer noise figure are nearly equal. The difference in noise figure can again be attributed to the slightly unequal impedances presented to the diodes for the two mixer designs.

In order to measure the improvement in power handling of the grid, the lin-

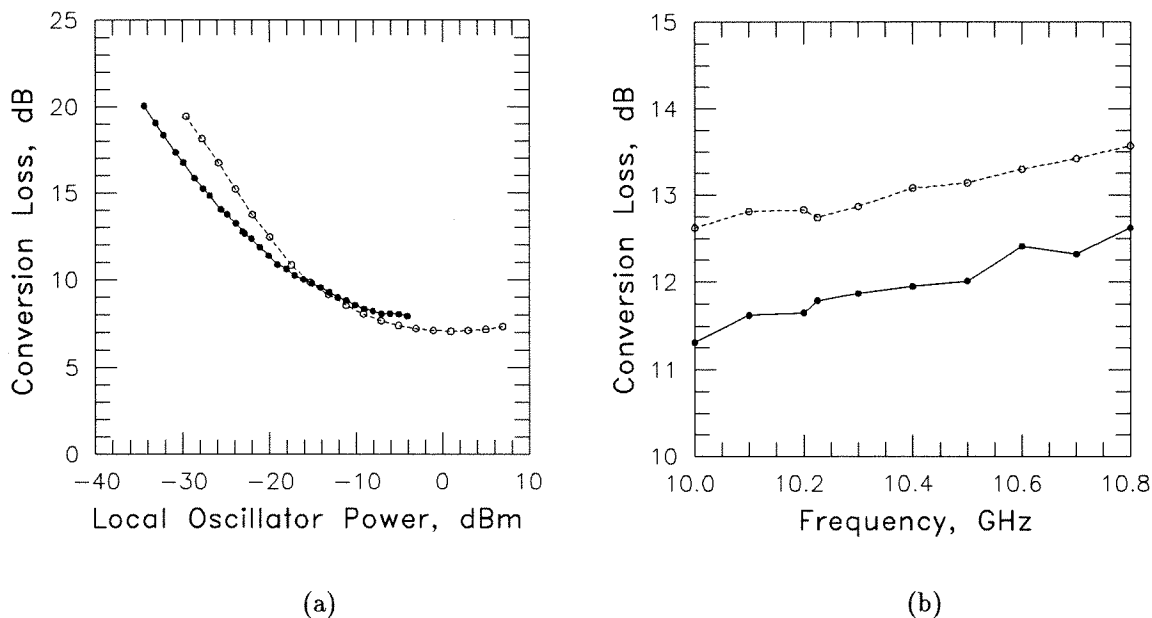


Figure 2.19 (a) Measured grid mixer conversion loss (—) and equivalent single-diode mixer conversion loss (---) as a function of LO power per diode for an LO frequency of 10.225 GHz and an IF frequency of 214 MHz. The conversion loss of the grid mixer is comparable to the single-diode mixer. (b) Measured grid mixer conversion loss (—) and equivalent single-diode mixer conversion loss (---) as a function of frequency for a local oscillator power of -20 dBm per diode. The bandwidth of the grid mixer is primarily limited by the reactive tuning mirror.

earity of the grid mixer was measured and compared to the single-diode mixer. The linearity of the mixer was characterized by computing the third-order intercept point (IP3) of the mixer for two equal-power RF input tones separated by 10 MHz. For the same local oscillator power per diode, the grid mixer third-order intercept point should be 100 times larger than that of the single-diode mixer, a factor equal to the number of diodes in the grid.

Figure 2.22 shows the test setup used to measure the third-order intercept point of the grid mixer. Two closely separated equal-power RF input tones of frequency f_a and f_b , are combined with the LO of frequency f_L and fed to a horn. Ideally, the two tones will be mixed down to the IF frequency, generating two signals at $f_1 = |f_L - f_a|$ and $f_2 = |f_L - f_b|$. In practice, spurious intermodulation products will also be created by the mixer due to higher order nonlinearity in the mixer transfer function. Of these, the most important are the third-order

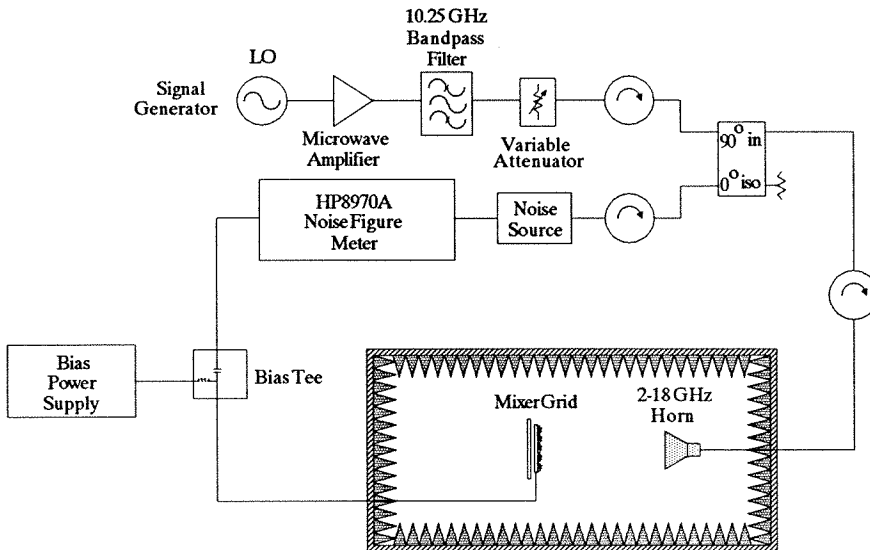


Figure 2.20 Quasi-optical Noise Figure meter. A high-temperature noise source is used to overcome the large system pathloss. The microwave amplifier used was an HP 8349B solid-state amplifier for LO powers below -20 dBm per diode, and a 10 Watt travelling-wave-tube amplifier for LO powers above -20 dBm per diode.

intermodulation products, which will show up at frequencies $2f_1 - f_2$ and $2f_2 - f_1$ alongside the desired IF signals, as shown in Figure 2.23. This type of distortion can seriously degrade the performance of a receiver. For example, third-order intermodulation distortion products will show up as diagonal black lines on a television receiver, a notorious problem with poorly-designed cable television systems.

The third-order intercept point is the power at which the undesired third-order intermodulation products are equal to the power of the desired signal. For a mixer, power is typically defined to be the input RF power of one of the desired signals, denoted P_{REF} . The third-order intermodulation distortion products are typically measured relative to the desired IF signal, and is denoted IMD_3 . Since the third-order intermodulation distortion products increase three times faster than the desired signals (Figure 2.24), from these two measurements

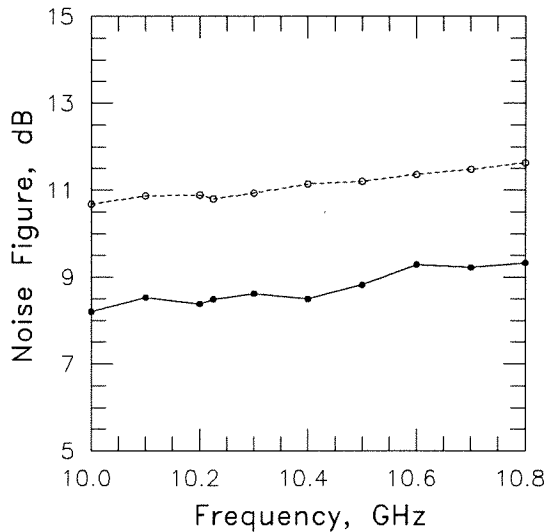


Figure 2.21 Measured grid mixer noise figure (—) and equivalent single-diode mixer noise figure (---) as a function of frequency for a local oscillator power of -20 dBm per diode. The noise figure of the grid mixer is comparable to that of a single-diode mixer. Excess noise from the TWT amplifier prevented swept frequency noise figure measurements for LO powers above -20 dBm per diode.

the extrapolated power at which the desired and undesired signals will have the same power, the third-order intercept point, can be computed using

$$IP_3 = P_{REF} + \frac{IMD_3}{2}. \quad (2.26)$$

The linearity of a diode is a function of local-oscillator power, P_{LO} , and for low local-oscillator power, IP_3 is approximately linearly related to P_{LO} . For example, the HSCH-5332 diode used in the grid has a third-order intercept point that increases by 20 dB as the local-oscillator power is increased from -20 dBm

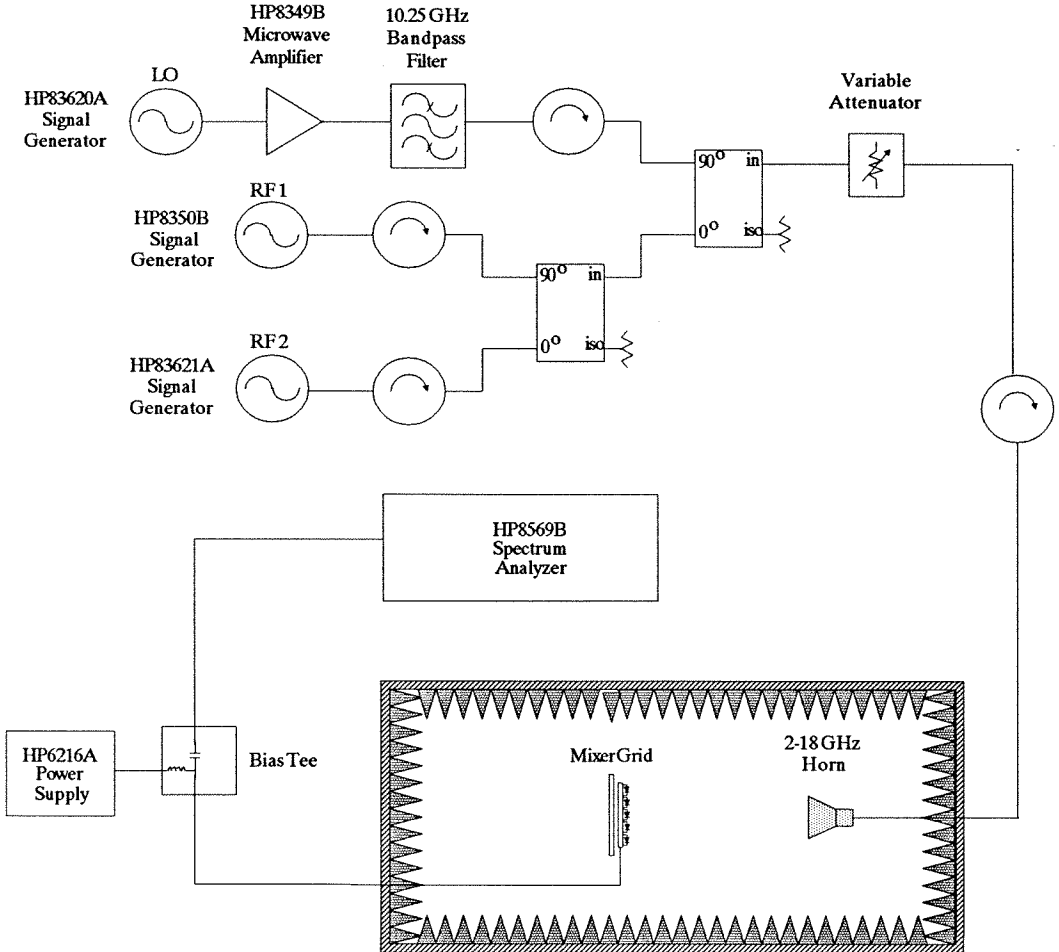


Figure 2.22 Third-order intercept test setup.

to 0 dBm. For local-oscillator powers near the maximum for the diode, 10 dBm for the HSCH-5332, this linearity breaks down, with further increase in local-oscillator power not resulting in a higher IP3. For this reason, it is essential to compare the single-diode mixer linearity with the grid mixer using the same local-oscillator power per diode.

Figure 2.25(a) shows the measured third-order intercept point for both the grid mixer and the single-diode mixer. Figure 2.25(b) shows the difference in third-order intercept point for the two mixers. Improvements of 16.3 to 19.8 dB were measured over a 30-dB range of local oscillator powers. This compares favorably with the expected improvement of 20 dB predicted from theory for a 100-element grid.

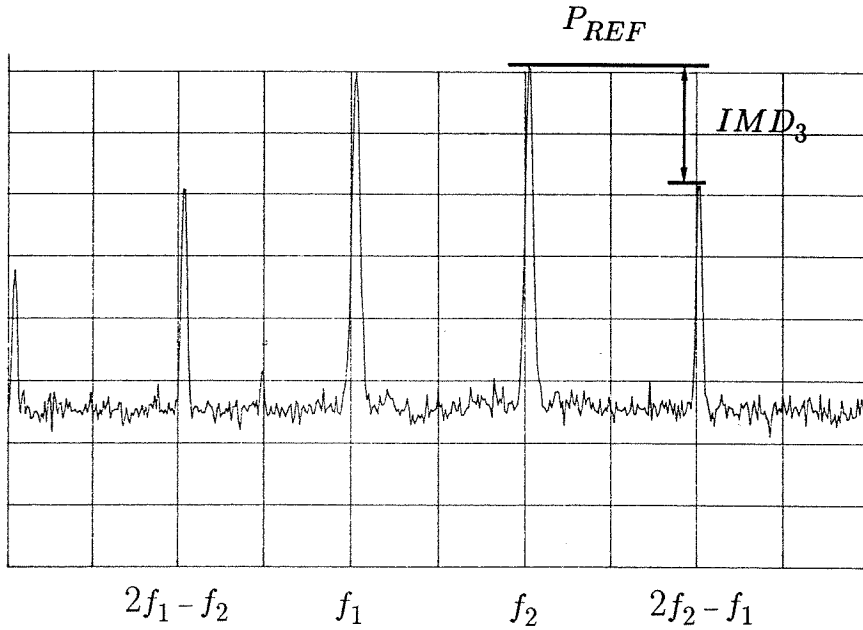


Figure 2.23 Third-order intermodulation distortion products created when two equal power RF tones are input to the mixer. The desired signals f_1 and f_2 are flanked by the undesired third-order intermodulation products $2f_1 - f_2$ and $2f_2 - f_1$. The lower the undesired signals, the more linear the mixer is said to be.

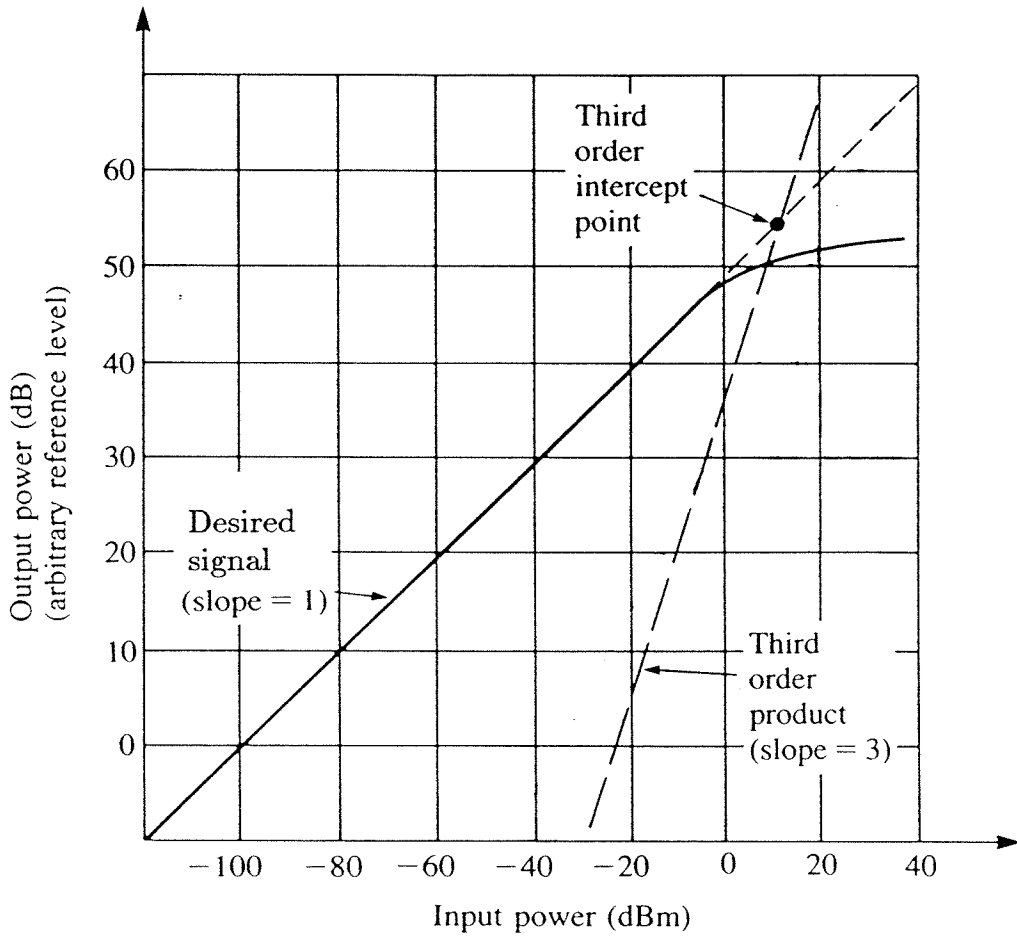


Figure 2.24 The third-order intercept point is extrapolated from relative power measurements of the desired signal and the undesired third-order intermodulation products. From [17].

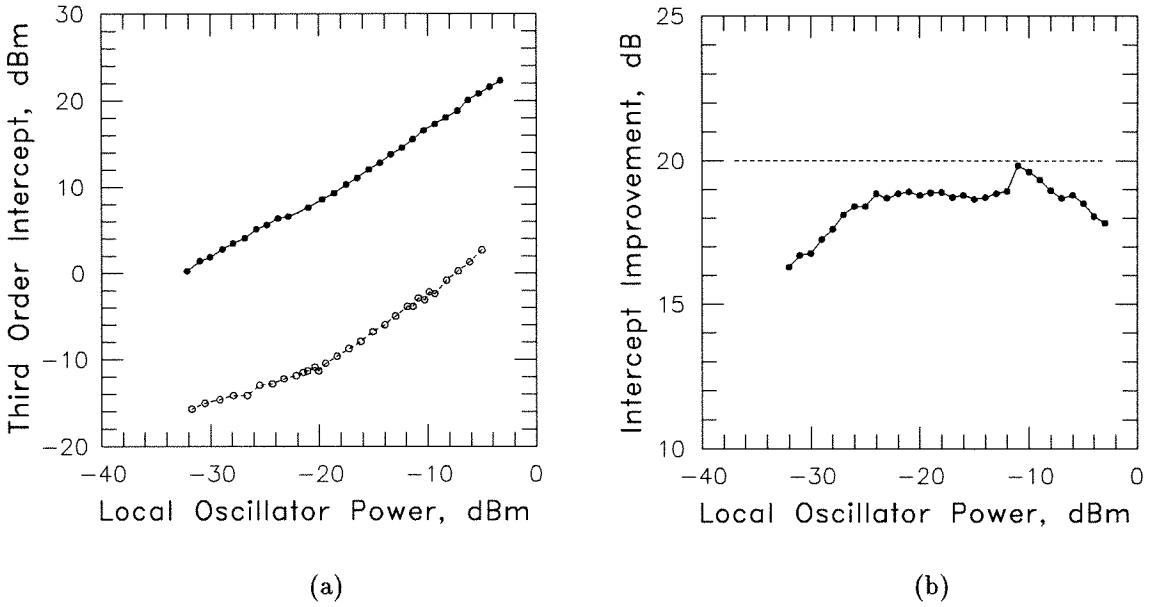


Figure 2.25. (a) Measured grid mixer third-order intercept point (—) and equivalent single-diode mixer third-order intercept point (---) as a function of local oscillator power per diode. Two RF tones at 10.434 GHz and 10.444 GHz were used to measure the intermodulation products. (b) Measured improvement in third-order intercept point for the grid mixer over the single-diode mixer (—) as a function of local oscillator power per diode. Theory (---) predicts a 20-dB improvement for a 100-element grid.

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Chapter 3

Terahertz Sideband Generator Grid

The submillimeter-wave spectral region, generally considered to be from 300 GHz to 3 THz, has many important applications including molecular spectroscopy, particularly in astronomy and atmospheric physics, plasma and laser diagnostics, semiconductor physics, and environmental research [1]. This interest has fostered a need for submillimeter-wave receivers, sources, and mixers. In particular, there is a strong requirement for a tunable source that can be used as the local oscillator for very high sensitivity and resolution heterodyne submillimeter-wave receivers. Aside from frequency agility, such a source should also have a number of additional properties including high-output power (Schottky diode mixers typically require 1 mW of LO power for good performance), high-spectral purity, and excellent frequency stability to facilitate long integration times during measurements. Unfortunately, the traditional high-power source in this region, the laser, is a fixed frequency device unsuited to the task. However, diode multipliers and upconverters possess the required frequency agility and can be used to generate terahertz frequencies from lower-frequency solid-state tunable signal sources such as Gunn diode oscillators.

Current diode multipliers and mixers have mostly been single-diode structures, typically consisting of a Schottky diode placed in some type of antenna or waveguide structure, and fall short of the desired 1 mW of output power. For example, the power reported for a recent 803 GHz Schottky diode tripler is 120 μ W with a 0.8% efficiency [2]. One approach to overcome the low-power inherent

with solid-state devices operating in the submillimeter-wave band is to efficiently combine a large number of them together. A grid of diodes quasi-optically coupled in free space is ideal for this purpose and potentially allows thousands of diodes to be combined together in a single monolithic structure. Using this approach, a pulsed 99 GHz frequency tripler consisting of several thousand diodes has been demonstrated that produced 5- W at 99 GHz [3]. Similarly, a grid mixer can be used to upconvert a tunable low-frequency signal, the IF, to the terahertz region by using a high-frequency fixed source, for example a sub-millimeter laser, as the local oscillator. We refer to such a structure as a sideband generator grid.

In this chapter a design for a diode sideband generator grid suitable for operation at terahertz frequencies is presented. This project is a joint effort between the MMIC group at Caltech and the Semiconductor Devices Laboratory at the University of Virginia, who are responsible for its fabrication and testing. This will be the first application of a quasi-optical diode grid at terahertz frequencies. The grid will use state-of-the-art planar Schottky diodes [4,5] monolithically integrated on a quartz or GaAs substrate. Fabrication of 169 individual 36-element grids is presently underway.

Previous attempts at generating submillimeter-wave power using sideband generators have been disappointing. Typical conversion loss for such structures, defined as the power in one sideband relative to the power in the incident carrier, have varied from -58 dB at 890 GHz [6] to -40 dB at 2520 GHz [7]. Reported powers have ranged from 100 nW at 890 GHz from Bicanic [6] to 9.5 nW at 2.52 THz from Grossman [7], a power that is too low to be useful even for superconducting tunnel junction (SIS) receivers. If successful, a sideband generator grid consisting of hundreds of devices should be capable of much greater output power than reported for these single-diode designs.

3.1 DESIGN GOALS

The terahertz sideband generator grid is a nonlinear device intended to up-

convert a variable low-frequency 1–20 GHz IF signal onto a 1.6 THz LO signal generated by a laser. A narrow bandpass filter is used to filter out one of the two RF sideband signals generated around the LO providing an accurate variable-frequency terahertz signal source for use in a heterodyne receiver. As mentioned previously, power generation at terahertz frequencies using this scheme is not new. Sideband generators at 2.52 THz using single whisker-contacted diodes placed in a corner cube reflector have already been demonstrated [7]. However, due to the difficulty in designing efficient mixers and antennas at these frequencies, power levels reported by these designs have been extremely low.

To date, planar diode circuits for use as terahertz mixers and frequency multipliers have typically been fabricated using planar transmission-line circuits such as microstrip. While microstrip circuits are amenable to monolithic fabrication at the required dimensions using fine-line photolithography, they suffer from excessive radiation and conduction losses which makes power combining even a few devices impractical. In addition, the parasitic capacitance and excessive ohmic contact series resistance of planar Schottky diodes has currently prevented their use at frequencies above 345 GHz [8].

Many of these problems disappear or are reduced in severity when planar diodes are incorporated into a grid. The planar grid structure is suitable for monolithic construction potentially allowing hundreds or thousands of devices to be combined quasi-optically in a single grid. Since each diode is effectively in its own equivalent unit-cell waveguide, many of the parasitic capacitances that plague planar diodes mounted on substrates over a ground plane vanish. Additionally, problems with resistive losses at ohmic contacts are reduced because ac current paths are limited to the very small dimensions of the unit cell, and the ohmic contact can be distributed over the entire metal pattern within each equivalent waveguide cell. Consequently, the sideband generator grid is a highly attractive structure for extending monolithic planar diode technology to terahertz

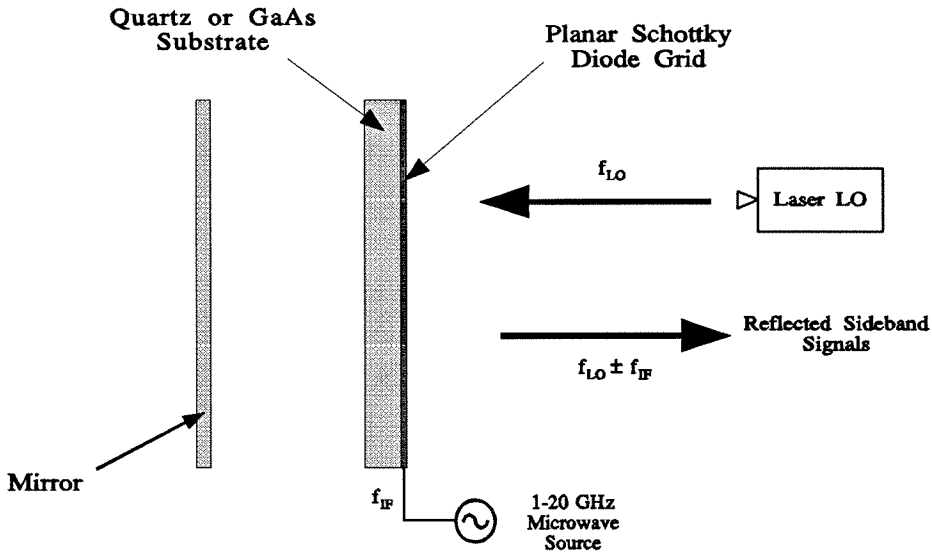


Figure 3.1 The sideband generator grid. The incident LO signal and reflected sideband signals couple to the diodes quasi-optically through the face of the grid. The mirror is used to tune out the capacitive reactance of the diodes for a better match to free space. The preferred substrate for the grid is quartz.

frequencies.

Figure 3.1 shows the basic configuration proposed for the sideband generator grid. A grid periodically loaded with diodes is placed normally incident to a incoming 1.6 THz local-oscillator beam generated by a conventional gas laser. A mirror behind the grid is used to help tune the grid for a good impedance match to free space. This allows good coupling efficiencies to the LO signal to be achieved. A novel fabrication technique allows the GaAs substrate to be removed and replaced with quartz [8]. A substrate composed of quartz is preferred as the lower dielectric constant of quartz allows a larger unit cell with a bow-tie metal pattern to be used, and simulations show this results in greater bandwidth.

A 1–20 GHz microwave sweeper is used to generate the high-power IF signal to be upconverted. The IF is fed to the grid using a coplanar waveguide feed as shown in Figure 3.2. The center conductor of the coplanar waveguide is

connected to the center row of the grid and the edges of the grid are connected to the outer conductors of the IF coplanar waveguide. For a square grid, the impedance presented to the coplanar IF waveguide line will be $Z_{IF}/4$. This will transform the typical $200\ \Omega$ IF impedance of the diode to the $50\ \Omega$ output of the microwave sweeper. DC bias is fed to the center horizontal row of the grid and flows to the top and bottom edges which are grounded to the outer conductors of the IF coplanar waveguide. The polarity of the diodes is flipped above and below the center row to allow dc bias to flow outwards to either edge of the grid.

The size of the entire terahertz sideband generator grid chip is expected to be less than a millimeter square. In order to make handling easier, and to allow reliable IF and dc signal connections, the grid will need to be mounted in a holder. Figure 3.3 shows a proposed design for a grid holder that could be fabricated out of alumina. The grid is glued into the hole in the center of the

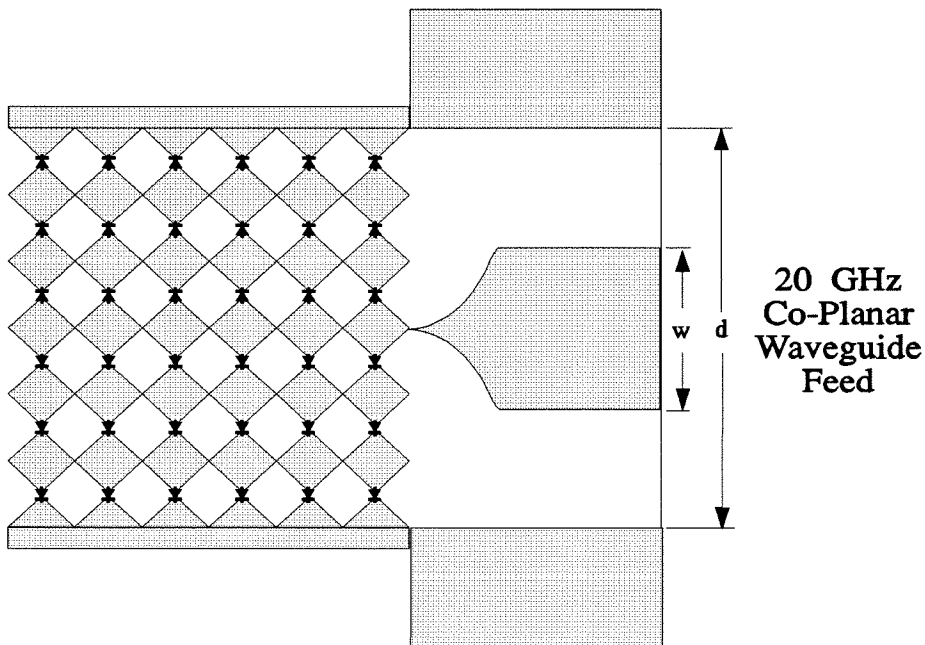


Figure 3.2 Details of the 1–20 GHz IF feed structure. A coplanar waveguide feed is used to feed both dc bias and IF signals to the diodes.

mount and wirebonded to the $50\ \Omega$ coplanar waveguide on the mount surface. An SMA connector on the mount is used to connect with IF source and dc biasing equipment while the hole in the mount allows access to the back of the grid for positioning a mirror.

Flipping the diode polarity above and below the center row of the grid is inadvisable for frequency multiplier grids as it is equivalent to placing a magnetic wall along the center row of the grid. This destroys the grid symmetry that allows an equivalent waveguide unit cell to be used to analyze the grid embedding impedance as discussed in chapter 2. However, in the case of the sideband generator grid, where the IF signal is much larger than the LO, the IF signal will switch the diodes on and off in unison, and the grid will appear as a slowly varying variable reactance sheet to the incident LO beam as shown in Figure 3.4. The reflected LO signal will then be phase modulated by the varying reactance of the grid. Under this condition, the grid symmetry is not disturbed by the flipped diode polarity across the grid center, and the equivalent waveguide unit

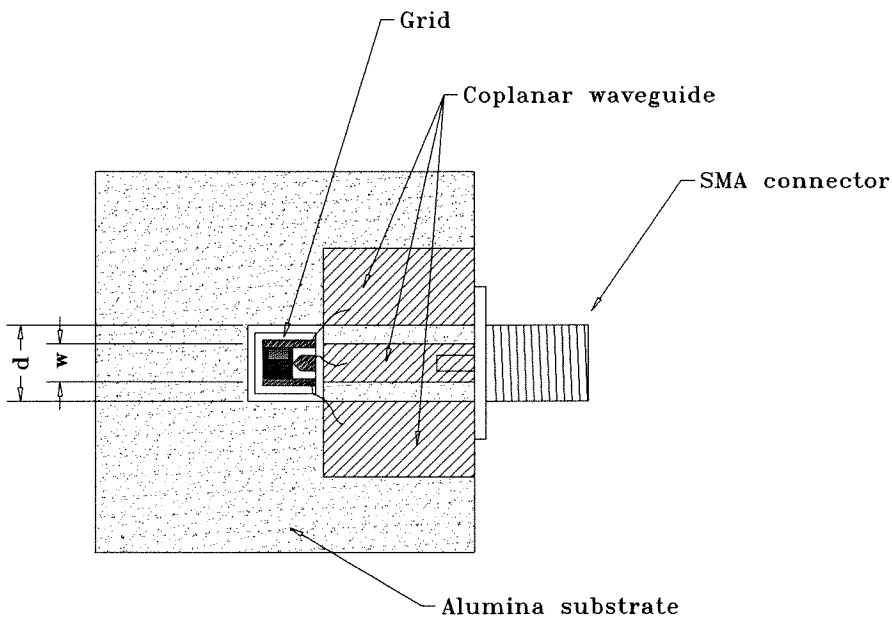
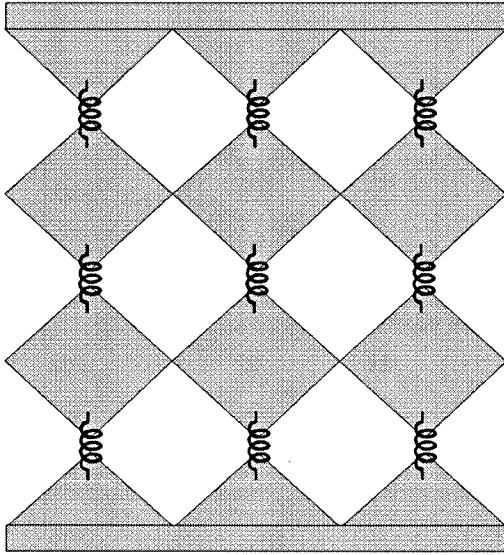


Figure 3.3 Alumina grid mount.

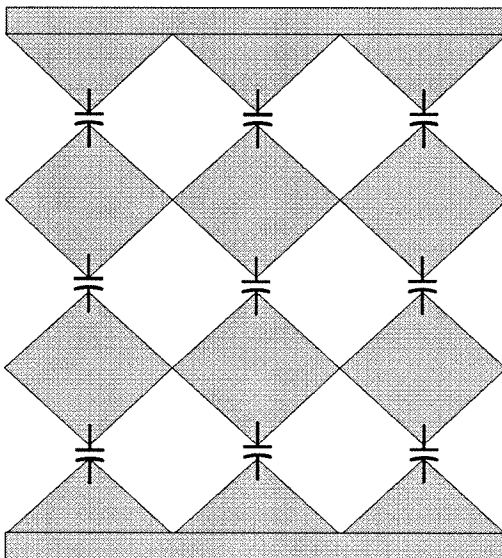
cell analysis is still valid.

The design of the grid is similar to that described in chapter 2 for the 10 GHz grid mixer. Exploiting grid symmetry, the entire grid is reduced to an equivalent waveguide unit cell whose embedding impedance can be modelled using simple transmission-line models. The grid was designed for use with LO frequencies of 1.5878 THz ($190\ \mu\text{m}$), 1.629 THz ($184\ \mu\text{m}$), and 1.675 THz ($179\ \mu\text{m}$). Figure 3.5 shows the dimensions of the planar diodes incorporated into the grid. The diode is composed of a $14\text{-}\mu\text{m}$ long finger consisting of a $1\text{-}\mu\text{m}$ wide anode finger and a $2\text{--}4\text{-}\mu\text{m}$ wide cathode n^+ finger. Figure 3.6 shows the equivalent circuit used to model the diode. Due to the experimental nature of the diode, this model only approximates the actual diode impedance. The diode model was incorporated into the grid transmission-line model as was previously done for the grid mixer. This allows the reflection coefficient the grid presents to the incident LO signal to be simulated and optimized for the best match to free space.

Past experience has shown that it is desirable to keep the grid unit cell as small as possible to avoid the generation of undesirable substrate modes. If λ_d is the wavelength in the dielectric, then for unit cells larger than λ_d , substrate modes will begin to propagate. It should be reasonable to build grids as large as $\frac{4}{5}\lambda_d$; however, to date grids only up to $\lambda_d/2$ have been tested. For 1.6 THz, this places an upper bound for the unit cell at $77\ \mu\text{m}$ for quartz and $41\ \mu\text{m}$ for GaAs. Given that the diode is on the order of $14\text{-}\mu\text{m}$ long and $1\text{--}4\text{-}\mu\text{m}$ wide, it is clear that, unlike the 10-GHz grid, the diode size cannot be ignored in the analysis. For the GaAs case in particular, the diode will be at least 33% of the length of the unit cell. For simple unit cell geometries such as the vertical strip and the bow-tie, the EMF method can be used to find the grid embedding impedance as discussed in chapter 2. Unfortunately, the large and irregular shape of the planar diode used in the sideband generator grid precludes using a simple strip or bow-tie as anything but a gross approximation to the actual



Diodes Biased On
by IF Signal



Diodes Biased Off
by IF Signal

Figure 3.4 The large IF signal slowly modulates the reactance the diodes present to the smaller LO signal. We can represent the grid as a slowly time-varying reactive sheet. The reflected LO signal will be phase modulated by the grid to produce the desired sidebands.

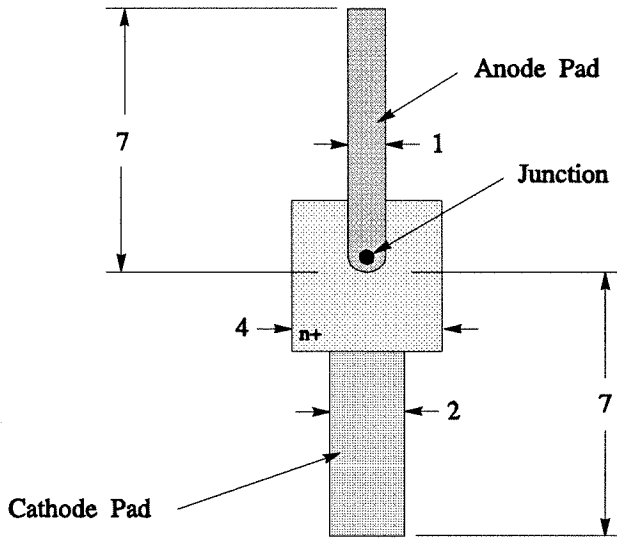


Figure 3.5 Physical dimensions of the planar Schottky diode to be used in the terahertz sideband generator grid. The junction diameter is $1.0\ \mu\text{m}$. All dimensions given in micrometers.

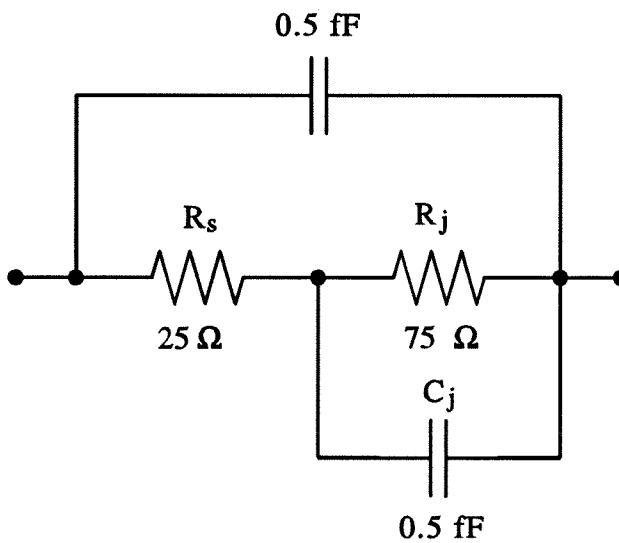


Figure 3.6 Equivalent circuit used to model the planar Schottky diode impedance to a terahertz signal.

circuit. For this reason, it was decided to explore the use of the *Hewlett-Packard High Frequency Structure Simulator*, a finite-element electromagnetic solver, to extract the embedding impedance of the complex geometry of the unit cell [9].

3.2 GRID EMBEDDING CIRCUIT EXTRACTION TECHNIQUES

Modelling the embedding impedance a quasi-optical grid presents to a port located arbitrarily inside a grid unit cell is a challenging problem. We start by assuming an infinite grid and use grid symmetry to reduce the problem to the analysis of an equivalent unit cell waveguide with magnetic and electric walls. For simple unit cell metal patterns we can use the EMF method to solve the waveguide problem. This approach has been successful for analyzing strips and bow-tie metal patterns [10]. More complicated metal shapes are not so readily solved using the EMF method, and numerical techniques must be investigated instead.

It is convenient to consider two classes of grid embedding impedance problems: three-port circuits for attaching two terminal devices, such as diodes, to the grid, and four-port circuits for connecting three-or-four-terminal devices, such as transistors, to the grid. Three-port circuits are considerably simpler to analyze and will be discussed first. Four-port circuits are much more difficult. Only limited success to date has been achieved analyzing four-port circuits using numerical techniques.

3.2.1 THREE-PORT GRID CIRCUIT EXTRACTION

Figure 3.7 shows an arbitrary three-port grid unit cell. Such a structure can be modelled using a three-port s -parameter matrix. Ports 1 and 2 are respectively the front and back of the grid, and port 3 is the internal port on the grid unit cell where the two-terminal device will be attached.

It is almost always the case that there is symmetry between the left and right, and top and bottom portions of a three-port grid. Under these conditions, the

grid unit cell can be further reduced to a quarter piece as shown in Figure 3.8. The internal port will now be exposed at the edge of the grid where a short section of well-defined transmission line can be attached. A rectangular coaxial stub is frequently convenient for this purpose. This stub can be defined in the HP structure simulator as the third port, producing a three-port structure that can be solved directly for the s -parameters (Figure 3.9). A simulation over the frequency range of interest is carried out and post-processing is performed on the s -parameter matrix to remove the effect of adding the transmission line stub to port 3, and to normalize the s -parameters to a convenient impedance.

If the three-port grid unit cell cannot be reduced to a quarter-piece through application of symmetry, or if the internal port cannot be made accessible to the edge of the grid, a more cumbersome approach can be used to extract the s -parameters of the grid.

First, to simplify the problem, a mirror is placed behind the grid. This reduces the grid model to a two-port where port 1 is the front of the grid, and

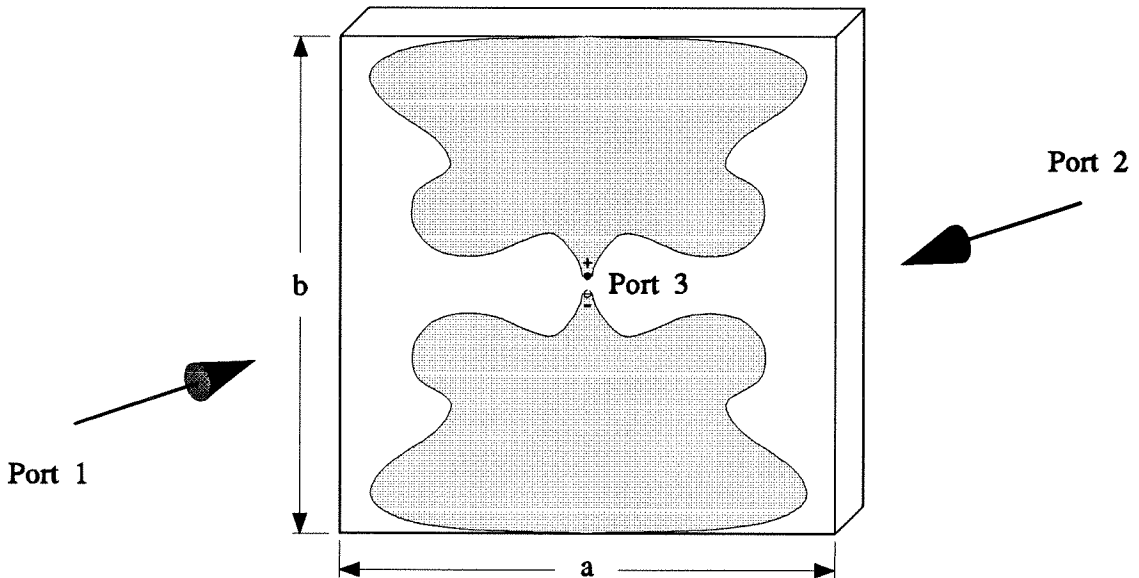


Figure 3.7 Arbitrary three-port grid unit cell.

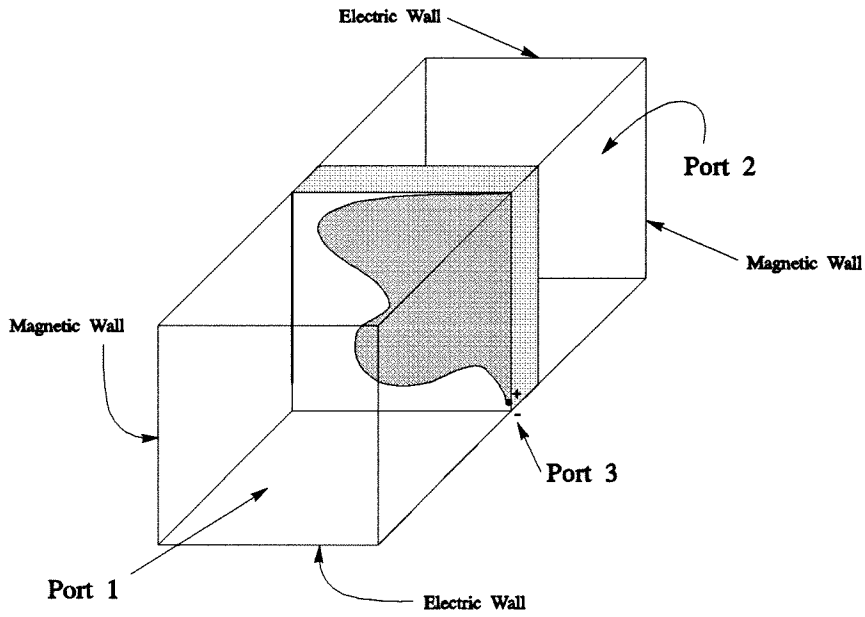


Figure 3.8 Arbitrary three-port grid unit cell reduced to a quarter piece through further application of symmetry.

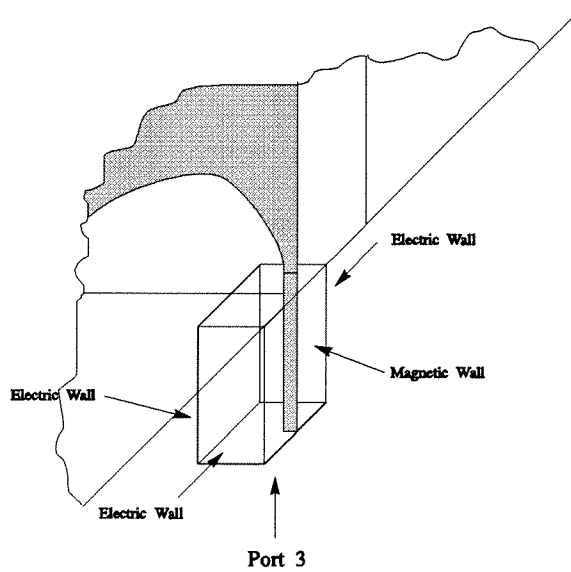


Figure 3.9 Detail view of the coaxial stub used to access the internal third port.

port 2 is now the internal port in the unit cell. Application of reciprocity to the grid allows us to note that $s_{21} = s_{12}$, and we are left with solving the matrix

$$\mathbf{S} = \begin{pmatrix} s_{11} & s_{12} \\ s_{12} & s_{22} \end{pmatrix}. \quad (3.1)$$

We can now apply a method developed for the calibration of a one-port network analyzer. A series of three electrically distinct loads are placed across the internal port. This reduces the structure to a one-port, where port 1 is the front of the grid. Typically these would be a short circuit, an open circuit, and a matched load. Version 1.0 of the HFSS does not permit lossy material to be specified, so the matched load must be replaced by a delayed short or open which can be much less convenient. Version 2.0 of the HFSS does permit lossy materials, so a matched load is a reasonable choice if using a later version of HFSS. Simulations of the structure over the frequency range of interest are carried out for each of the three loads generating three one-port s -parameter files, e_m , e_s , e_o corresponding to the matched termination, short-circuit, and open-circuit, respectively. These calibration s -parameters can then be used to find the two-port s -parameters of the grid using

$$s_{11} = e_m \quad (3.2)$$

$$s_{22} = \frac{e_o + e_s - 2e_m}{e_o - e_s} \quad (3.3)$$

$$s_{12}s_{21} = \frac{2(e_o - e_m)(e_s - e_m)}{e_s - e_o}. \quad (3.4)$$

In practice, it is possible to combine the above techniques with some intuition to shorten the analysis. For example, an equivalent circuit model for the grid can be guessed at, perhaps by the addition of one or two extra components to an existing EMF model of a similar metal pattern, to account for the differences in the grid metal pattern. Structure simulations using just a short or open across the internal port can then be compared to the modified equivalent circuit model,

also with a short or open across the internal port, using a linear circuit simulator such as *Puff*. The model parameters can then be fine-tuned until the model s -parameters agree with the structure simulator results. Frequently, the model parameters computed using the EMF method can be used as a starting point for the modified circuit. In this manner a good approximation to the grid embedding impedance can be realized very quickly.

An example of this is shown in Figure 3.10 where a bow-tie pattern is shortened and a thin strip added between the vertices. Intuitively, we would expect the thin strip to add some inductance to the circuit and to shorten the electrical length calculated using the EMF model for the bow-tie shunt transmission line. Comparison with the s -parameters from the structure simulator show that this is indeed the case. The values used for the equivalent circuit model are shown, with the EMF computed values in parentheses. Figure 3.11 shows the structure simulator s -parameters superimposed on the s -parameters computed from the modified equivalent circuit shown in Figure 3.10. The agreement is excellent. As would be expected, the electrical length of the bow-tie shunt transmission line is shortened by about a third, corresponding to the amount the bow-ties were physically shortened to accommodate the vertical strip.

This technique of modifying an existing EMF equivalent circuit to account for differences in the actual unit cell metal pattern from the ideal EMF case, and then using the structure simulator to compute the new values for the added components, has proven extremely effective. The sideband generator grid was modelled using this technique, and the power oscillator grids discussed in chapters 4 and 5 were designed in this manner as well. The technique is also fundamentally safer than simply relying on the structure simulator to generate an s -parameter matrix of a unit cell pattern that is then blindly accepted without further qualification. By comparing the numerical results with an intuitive model of the grid, simulation convergence problems can be much more reliably detected.

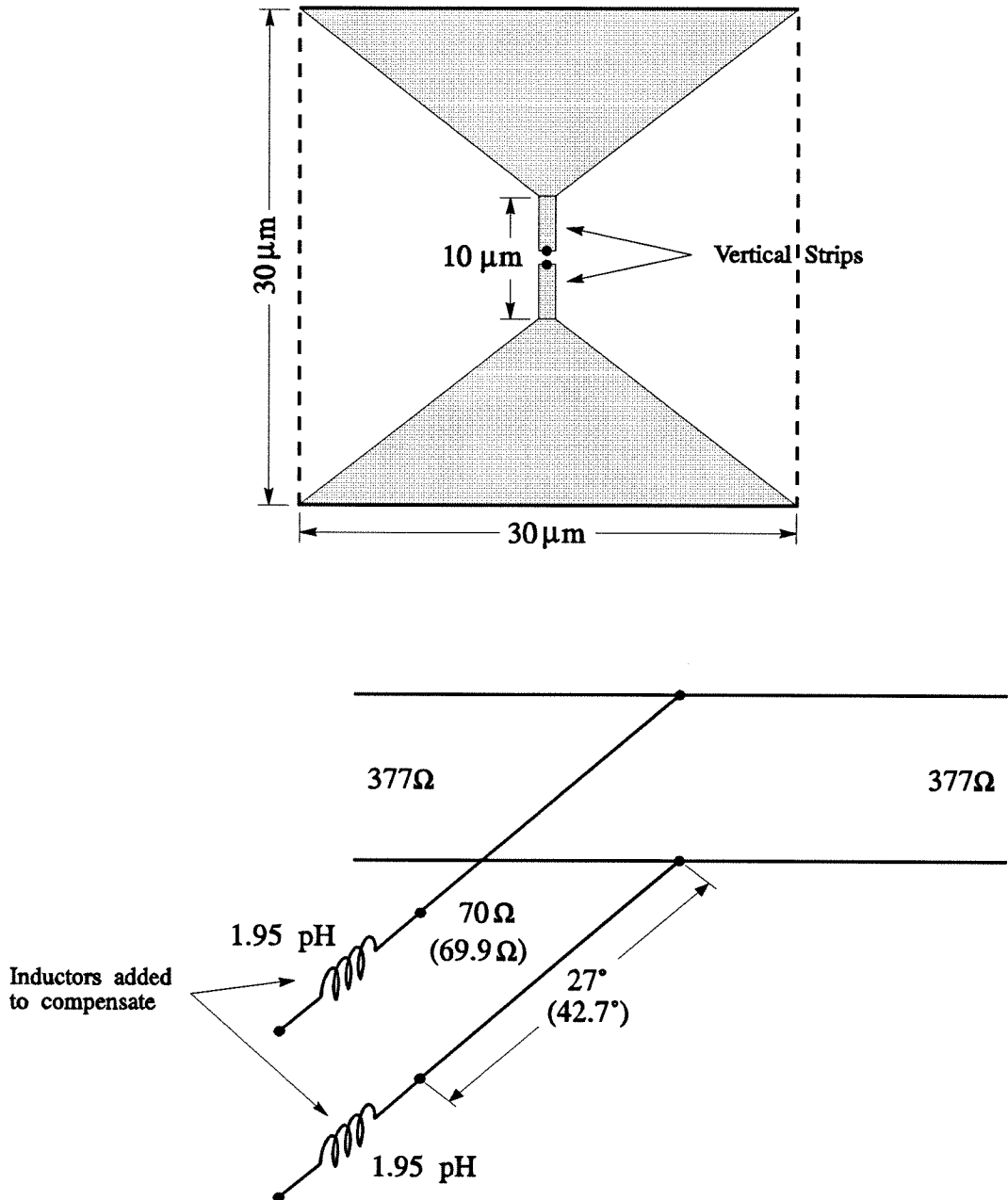


Figure 3.10 An example of modifying an existing EMF equivalent circuit to account for slight changes to the grid metal pattern. In this example the addition of the metal strips is accounted for in the model by the addition of two inductors. (Compare with Figure 2.7.)

3.2.2 FOUR-PORT GRID CIRCUIT EXTRACTION

Figure 3.12 shows an arbitrary four-port grid unit cell. Such a structure can be modelled using a four-port s -parameter matrix. Ports 1 and 4 are respectively the front and back of the grid, and ports 2 and 3 are the internal ports on the grid unit cell where a three or four terminal device, such as a transistor, will be attached.

We can make a number of simplifications to reduce the computational effort of computing 16 terms in the four-port s -parameter matrix. First, it is usually reasonable to place a mirror behind the grid. By eliminating the back port of the grid, we reduce the grid to a three-port network and the s -parameter matrix to 9 terms (Figure 3.13). Since the grid is assumed to be a passive, lossless, reciprocal structure, reciprocity tells us that $s_{21} = s_{12}$, $s_{13} = s_{31}$, and $s_{32} = s_{23}$.

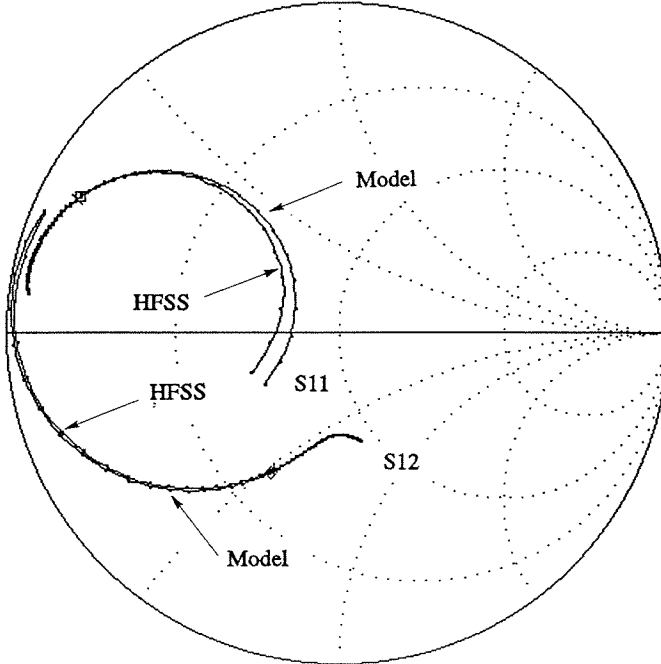


Figure 3.11 Comparison of modified equivalent circuit s -parameters (s_{11} , s_{12}) with the structure simulator s -parameters from 1–2 THz for the example shown in Figure 3.10. The markers are at 1.6 THz. A mirror is placed 150° behind the grid.

In order to proceed further, we need to make some assumptions about the symmetry of the unit cell pattern. It is frequently the case that the grid is symmetric across the top and bottom and left and right halves of the unit cell. Assuming this to be true, the fields and induced currents on the grid will have to obey certain symmetry conditions at the internal ports. If we assume a vertically polarized incident E-field incident on port 1 from free space, we expect fields induced across the internal ports 2 and 3 to be anti-symmetric. Given the port definitions shown in Figure 3.13, we can then say that $s_{21} = -s_{31}$ and $s_{22} = s_{33}$.

The above assumptions effectively reduce the number of independent complex s -parameter variables to four: s_{11} , s_{22} , s_{21} , and s_{32} . The corresponding s -parameter matrix for the grid is then given by

$$\mathbf{S} = \begin{pmatrix} s_{11} & s_{21} & -s_{21} \\ s_{21} & s_{22} & s_{32} \\ -s_{21} & s_{32} & s_{22} \end{pmatrix}. \quad (3.5)$$

In order to find the four unknown s -parameters that describe the grid, we can

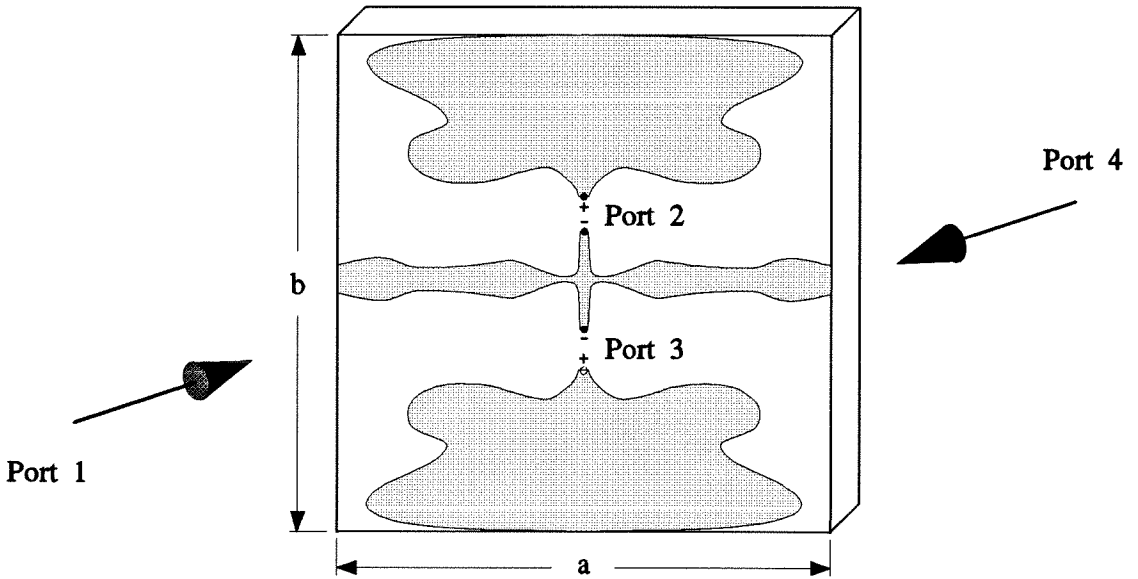


Figure 3.12 Arbitrary four-port grid unit cell.

simulate the grid unit cell with known calibration loads on the internal ports and extract the unknown grid s -parameters from the calibration data.

From our initial assumptions we know that the grid unit cell must have symmetry top and bottom and left and right. Thus, by symmetry we can reduce the problem to a quarter cell as was done for the three-port problem described earlier. Figure 3.14 shows the quarter-cell layout which we shall refer to as the primed system. In forming the quarter cell, we have folded ports 2 and 3 on top of each other to form port 2' of the new two-port prime network. Referring to the face of the grid, port 1', we see that the incident power and reflected power for the primed system are both reduced to a quarter the value of the full unit cell. Hence, it follows that

$$s'_{11} = s_{11}. \quad (3.6)$$

Interpreting the value at port 2' is a little more difficult. In forming port 2'

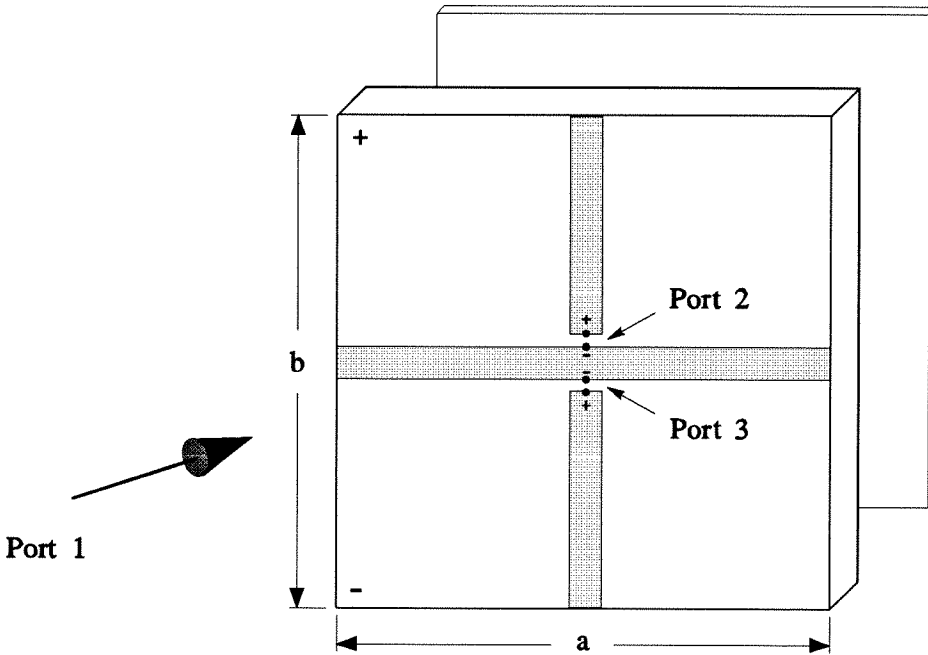


Figure 3.13 Prototype three-port unit cell obtained by placing a mirror behind the grid to eliminate the back port. The polarity definitions for the two internal ports and remaining front port are shown.

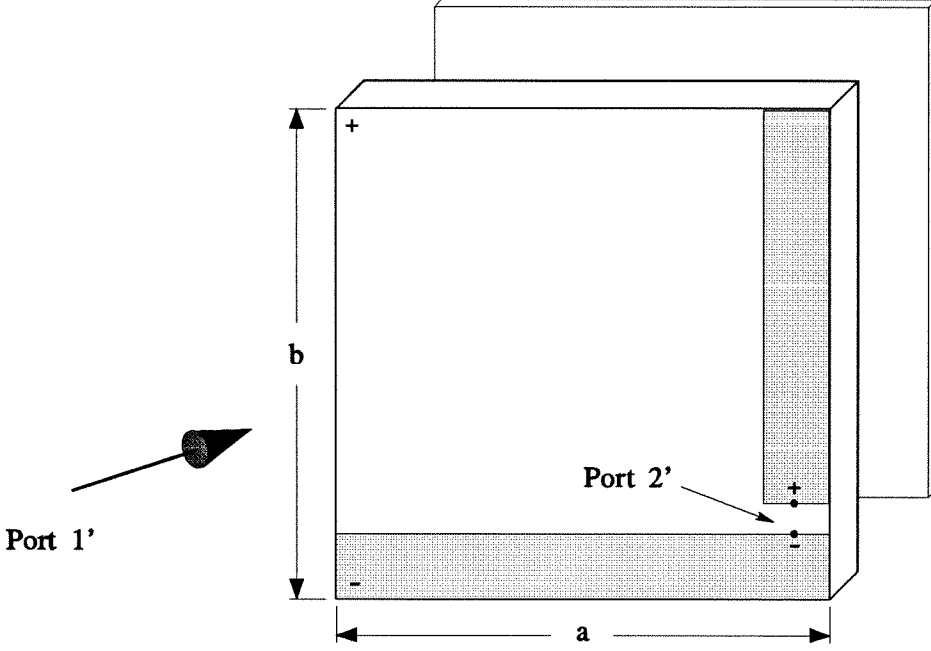


Figure 3.14 Primed system. By symmetry we can reduce the grid to the quarter cell, where ports 2 and 3 have been combined into a single port, port 2'.

out of ports 2 and 3 of the original problem, we will capture twice the power, and so it follows that

$$s'_{12} = \sqrt{2} s_{12}. \quad (3.7)$$

Finally, we need to understand how to relate s'_{22} back to the original grid. We note that an incident wave on port 2' is equivalent to driving ports 2 and 3 of the original grid with signals 180° out of phase with each other. Recalling that $s_{23} = s_{32}$ gives

$$s'_{22} = s_{22} - s_{32}. \quad (3.8)$$

We now have three equations and need one more relation to solve for the grid s -parameters. We can get the final relation by placing a short across port 2 and an open across port 3 as shown in Figure 3.15. We refer to this as the double-primed system. Using signal flow graph theory [11,12] we can solve for

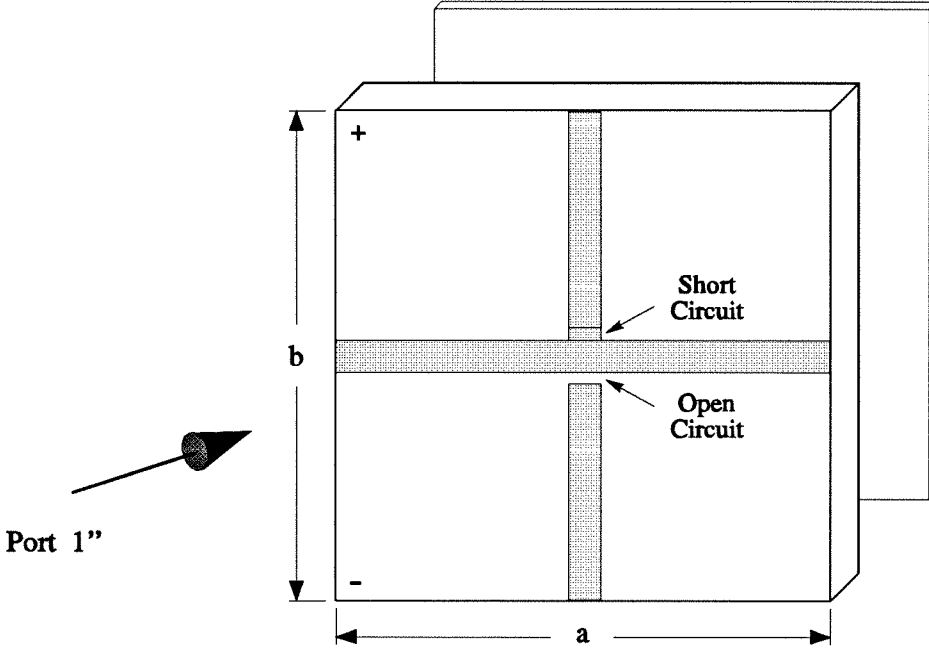


Figure 3.15 The double-primed system formed by placing a short across port 2 and an open across port 3.

the port 1'' reflection coefficient to get

$$s''_{11} = s_{11} + \frac{2s_{21}^2(s_{22} + s_{32})}{1 - s_{22}^2 + s_{32}^2}. \quad (3.9)$$

Solving the four equations (3.6)–(3.9) for the original s -parameters in terms of the simulated primed and double-primed parameters gives the following set of equations:

$$\begin{aligned} s_{11} &= s'_{11} \\ s_{12} &= \frac{s'_{12}}{\sqrt{2}} \\ s_{32} &= \frac{(s''_{11} - s'_{11})(1 - (s'_{22})^2) - (s'_{12})^2 s'_{22}}{2(s'_{12})^2 + 2s'_{22}(s''_{11} - s'_{11})} \\ s_{22} &= s'_{22} + s_{32}. \end{aligned} \quad (3.10)$$

To test this theory, the grid shown in Figure 3.13 was simulated at 10 GHz and compared with the results obtained by Weikle [10] using the EMF method. The grid dimensions used were 8.6 mm square with 0.5 mm wide strips on a 2.54 mm thick $\epsilon_r = 2.2$ substrate. Table 3.1 lists the two sets of s -parameters for comparison. The extracted values of the s -parameters are in good agreement except for s_{22} and s_{32} which have large differences in phase and magnitude. It is not clear if these differences are due to poor convergence of the HFSS numerical simulations, or are unexpected effects of using short transmission lines to get access to the internal ports of the simulated structures.

3.3 SIDEBAND GENERATOR GRID DESIGN

Two designs were developed for a sideband generator grid operating at a nominal frequency of 1.6 THz. One grid design assumes a quartz substrate, and uses a bow-tie shaped unit-cell in a 70- μm square unit cell to obtain a 10 dB reflection coefficient bandwidth of over 170 GHz. The other design is based on a GaAs substrate and uses a dipole shaped unit cell in a 30- μm square unit cell.

s -parameter	EMF	HFSS
s_{11}	$0.8929 \angle 13.73^\circ$	$0.9202 \angle 18.78^\circ$
s_{12}	$0.3184 \angle -63.72^\circ$	$0.2767 \angle -75.99^\circ$
s_{13}	$0.3184 \angle 116.28^\circ$	$0.2767 \angle 104.01^\circ$
s_{21}	$0.3184 \angle -63.72^\circ$	$0.2767 \angle -75.99^\circ$
s_{22}	$0.5956 \angle 93.95^\circ$	$0.8502 \angle 38.21^\circ$
s_{23}	$0.7375 \angle 177.33^\circ$	$0.4478 \angle 122.44^\circ$
s_{31}	$0.3184 \angle 116.28^\circ$	$0.2767 \angle 104.01^\circ$
s_{32}	$0.7375 \angle 177.33^\circ$	$0.4478 \angle 122.44^\circ$
s_{33}	$0.5956 \angle 93.95^\circ$	$0.8502 \angle 38.21^\circ$

Table 3.1 Comparison of s -parameters for the same grid unit cell using the EMF method and the HP structure simulator.

This grid has a much narrower 10-dB reflection coefficient bandwidth of only 30–40 GHz. The advantage of the GaAs design is in its simpler fabrication, as the quartz design requires several additional steps to strip away the GaAs substrate and bond the grid to a quartz die. The disadvantage of the GaAs design, beside the much narrower bandwidth, is its small size. The unit cell of the GaAs grid is only twice the length of the diode itself. For this reason, the equivalent circuit models may not be as accurate, and the error between theory and experiment may be substantial.

3.3.1 SIDEBAND GENERATOR GRID DESIGN ON QUARTZ

The quartz sideband generator grid is designed for a 25- μm thick quartz substrate having a relative dielectric constant of $\epsilon_r = 3.78$. Figure 3.16 shows the bow-tie-shaped metal pattern used for the unit cell. The Schottky diode junction is placed at the center of the unit cell, and two 7- μm fingers connect the anode and cathode of the diode to the bow-ties. The need to include the diode finger lengths in the grid metal pattern precluded the use of the simple bow-tie EMF analysis developed by Weikle [10] and used in the 10 GHz grid mixer design. Instead the approach described in section 3.2.1 was used to extract the embedding circuit for the grid unit cell by using a modified equivalent circuit model and the HP structure simulator.

Intuitively, one would expect the effect of the diode fingers would be to add some series inductance to the shunt transmission line normally used to describe the embedding impedance of the bow-tie and to shorten the bow-tie transmission line electrical length. Figure 3.17 shows the modifications made to the standard bow-tie equivalent circuit to account for the diode fingers. The circuit component values are obtained from the HFSS simulations. The values shown in parentheses are computed from the EMF solution for a bow-tie in the same size unit cell and are provided for comparison with the HFSS extracted values. Figure 3.18 shows the agreement between the equivalent circuit model, and the HFSS simulation

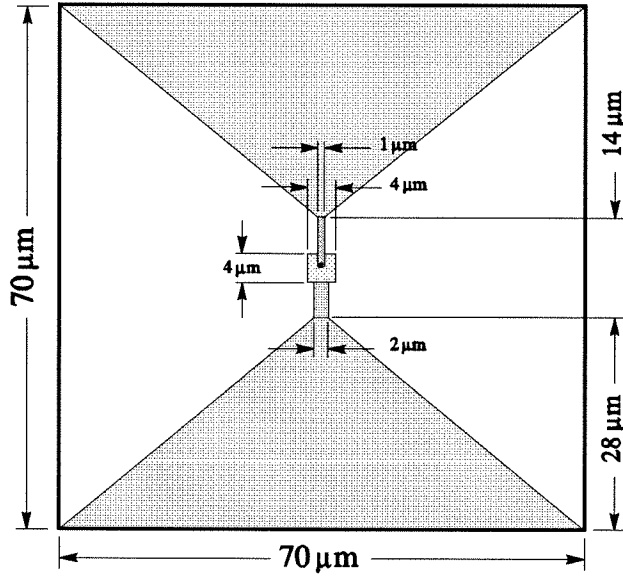


Figure 3.16 The unit cell dimensions and metal pattern for the 1.6 THz sideband generator grid on a 25- μm thick quartz substrate.

after adding 2.90 pH of series inductance and using a transmission line model for the bow-tie with $Z_{BT} = 119 \Omega$ and $\theta_{BT} = 57^\circ$. The agreement is seen to be excellent.

Figure 3.19 shows the theoretical reflection coefficient of the grid from 1 THz to 2 THz. The reflection coefficient null can be tuned from 1.5 THz to 1.9 THz by adjusting the position of the mirror behind the grid. The 10-dB bandwidth at 1.6 THz is 170 GHz.

The coplanar waveguide dimensions needed for a 50- Ω characteristic impedance IF feed were computed using a quasi-static approximation [13]. The width between the outer ground strips, d , of the coplanar waveguide was adjusted to be equal to the width of the entire grid. Consequently, the value of d , and also the width of the inner conductor, w , will vary as a function of the number of elements in the grid. Table 3.2 lists the computed dimensions for square grids of 36, 100, 400, and 1600 elements. Since the required center strip width for

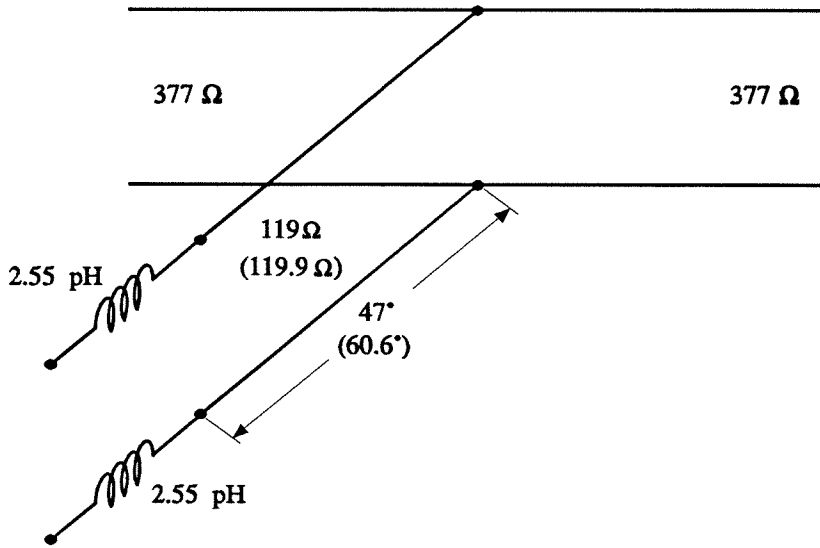


Figure 3.17 Modified equivalent circuit used to simulate the bow-tie grid with diode fingers. Values in parentheses are those obtained from an EMF analysis of a bow-tie pattern in the same size unit cell.

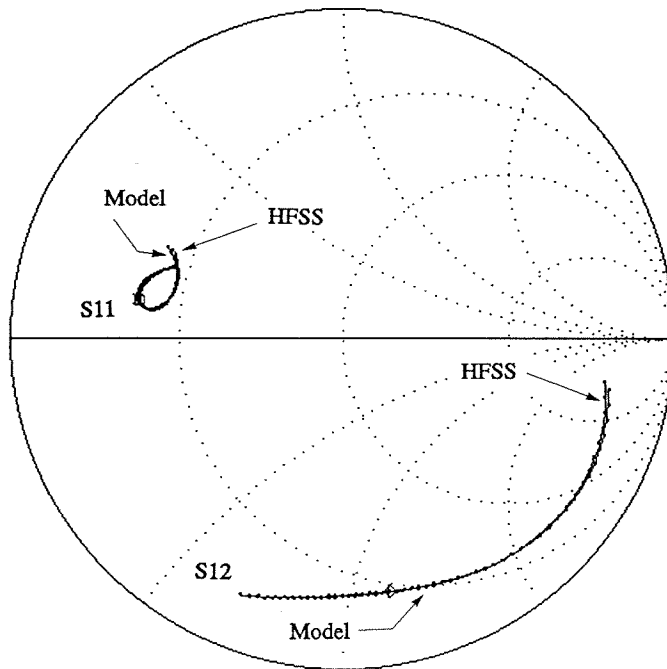


Figure 3.18 *s*-parameter plots for the HFSS simulation and the modified bow-tie equivalent circuit of Fig. 3.16. The two are almost indistinguishable.

a $50\text{-}\Omega$ characteristic impedance is very wide, it has to be tapered down where it joins the center row of the grid as shown in Figure 3.2. The effect of this tapered transition section is assumed negligible because its length is less than 1° at 20 GHz.

grid size	d (μm)	w (μm)	Z_0 (Ω)	ϵ_{eff}
6×6	420	388	50.1	1.63
10×10	700	655	50.1	1.51
20×20	1400	1330	49.9	1.38
20×20	2800	2686	50.1	1.26

Table 3.2 Quartz coplanar waveguide dimensions for the IF feed.

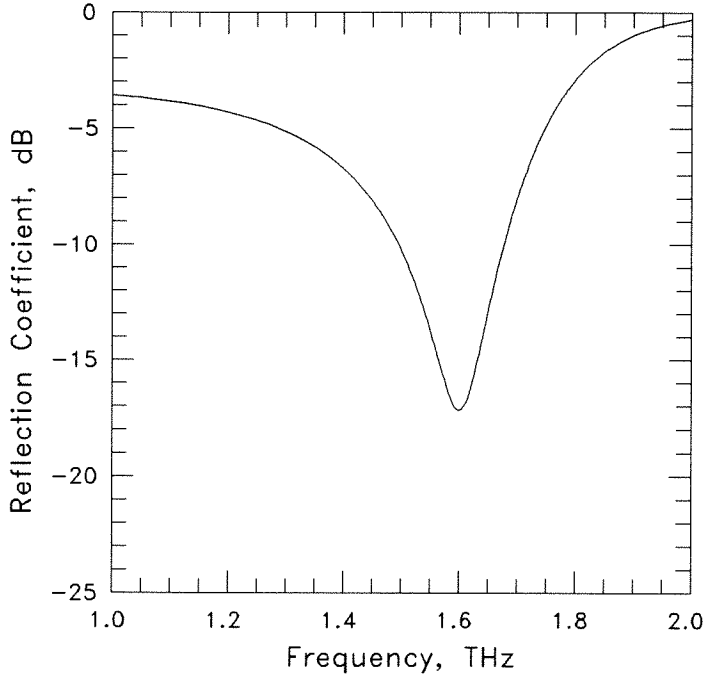


Figure 3.19 Theoretical reflection coefficient for the sideband generator grid on a quartz substrate.

3.3.2 SIDEBAND GENERATOR GRID DESIGN ON GALLIUM ARSENIDE

The GaAs sideband generator grid is designed for a 25- μm thick GaAs substrate having a relative dielectric constant of $\epsilon_r = 13$. Figure 3.20 shows the dipole-shaped metal pattern used for the unit cell. The Schottky diode junction is placed at the center of the unit cell. Two designs have been developed, differing only in the width of the diode fingers. Design A has diode fingers 1- μm wide compared with 2- μm wide fingers for design B. The wider fingers of design B should improve diode yield, but the trade-off is a narrower bandwidth.

Again, the need to include the diode finger lengths in the grid metal pattern precluded the use of the simple vertical strip EMF analysis. Instead the embedding circuit for the grid unit cell was extracted using the HP structure simulator.

The grid structure was simulated as a three-port network. The resulting s -parameter file was used directly in the simulation of the grid reflection coefficient, and the intermediate step of developing a transmission line equivalent circuit was skipped. Simulations for both the 1- μm wide and 2- μm diode fingers were performed. Figure 3.21 shows the layouts of the quarter cells used to simulate the grids. A 5- μm long rectangular cross-section coaxial stub was used to get access to the internal port of the grid where the diode is connected. This stub was de-embedded from the computed s -parameters before simulating the grid reflection coefficient.

Figure 3.22 shows the theoretical reflection coefficient of the two grids from 1 THz to 2 THz. The reflection coefficient can be tuned from 1.45 THz to 1.7 THz by adjusting the position of the mirror behind the grid. The 10 dB bandwidth at 1.6 THz is 40 GHz for the 1- μm wide diode finger design, and 30 GHz for the 2- μm wide finger design.

The coplanar waveguide dimensions needed for a 50- Ω characteristic impedance IF feed were again computed using a quasi-static approximation [13]. Like

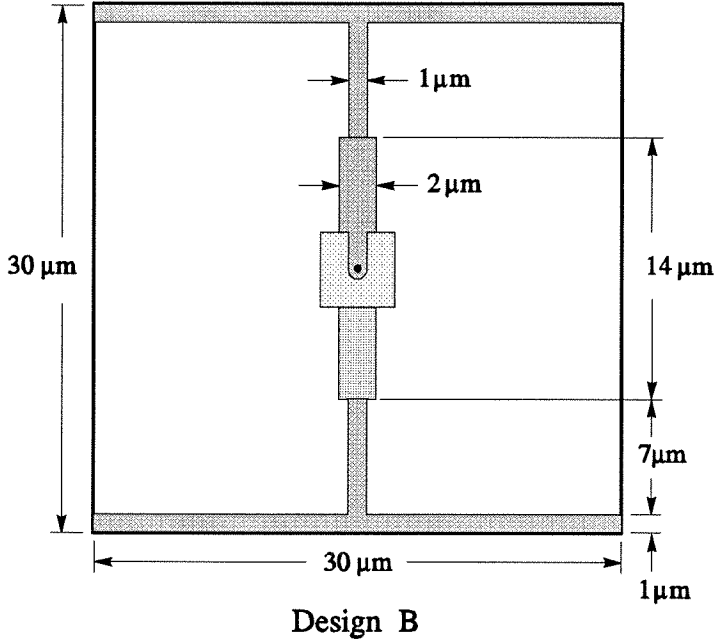
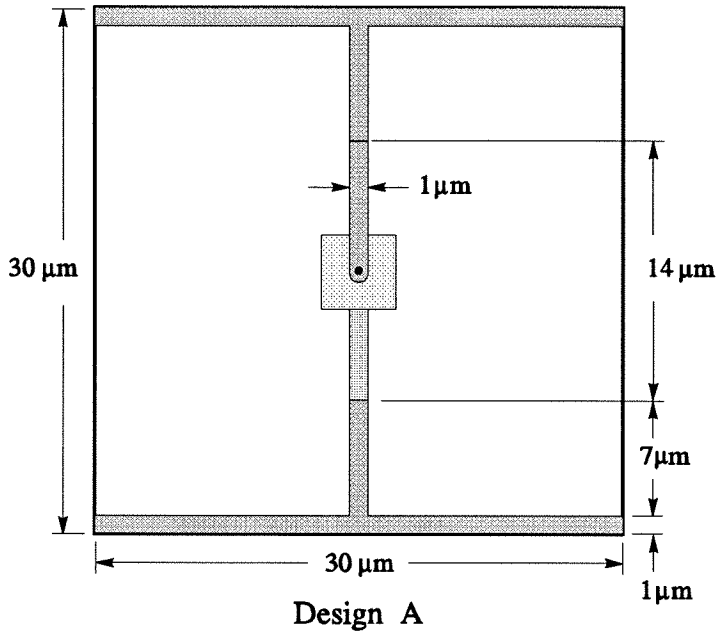
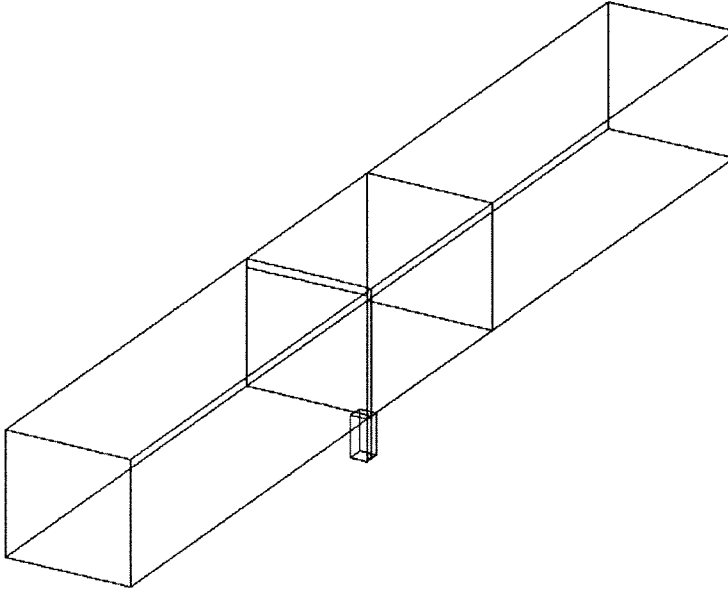
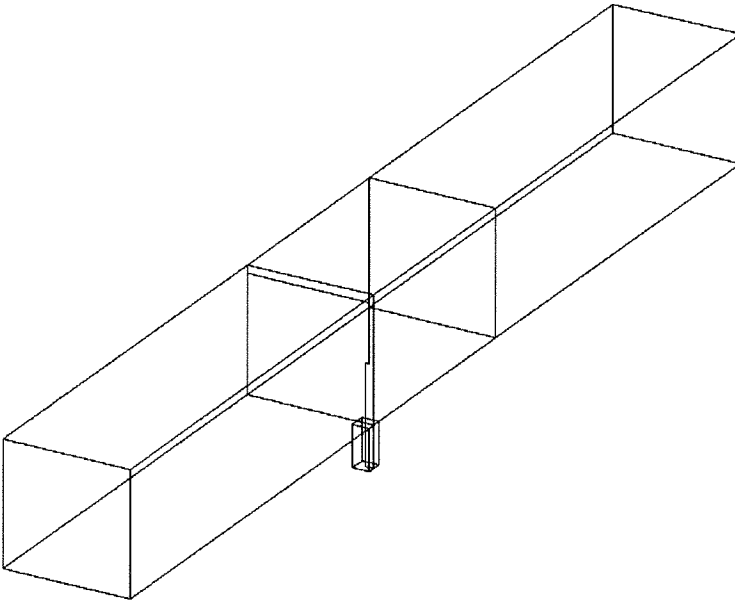


Figure 3.20 The unit cell dimensions and metal patterns for two 1.6 THz sideband generator grid designs on a GaAs substrate. Two designs have been developed, differing only in the width of the diode fingers.



Design A



Design B

Figure 3.21 Layouts of the HFSS quarter-cells used to simulate the two grid designs on GaAs. The coaxial stub used to get access to the internal port of the grids was de-embedded from the final s -parameter file.

the previous design, the width between the outer ground strips, d , of the coplanar waveguide was adjusted to be equal to the width of the entire grid. Table 3.3 lists the computed dimensions for square GaAs grids of 36, 100, 400, and 1600 elements.

grid size	d (μm)	w (μm)	Z_0 (Ω)	ϵ_{eff}
6×6	180	118	50.1	4.02
10×10	300	219	50.1	3.33
20×20	600	486	50.1	2.64
20×20	1200	1041	50.1	2.15

Table 3.3 GaAs coplanar waveguide dimensions for the IF feed.

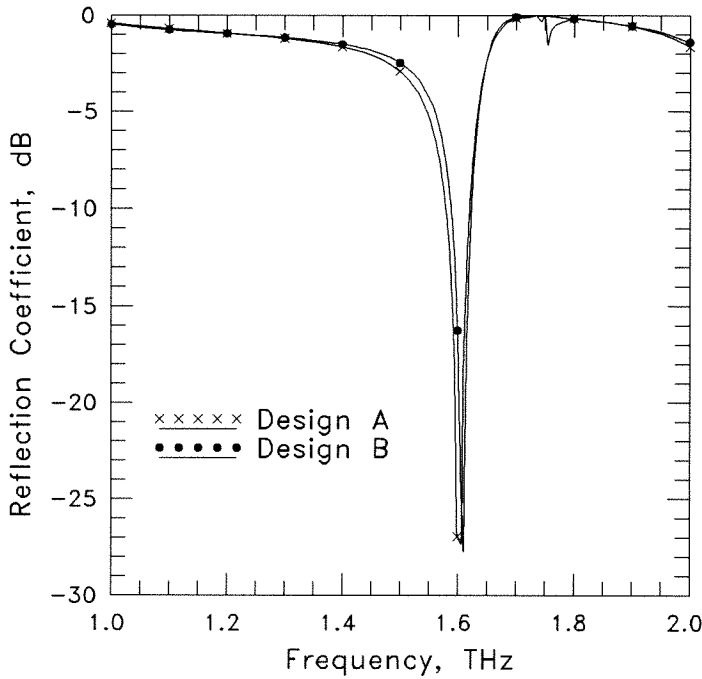


Figure 3.22 Theoretical reflection coefficients for the two sideband generator grid designs on a GaAs substrate. The plot with crosses is for the $1\text{-}\mu\text{m}$ wide diode finger (design A) and the plot with dots is for the $2\text{-}\mu\text{m}$ wide diode finger (design B).

3.4 FUTURE EXPERIMENTAL WORK

Unfortunately, the fabrication of the sideband generator grids was still underway at the time this thesis was written. For this reason, no experimental results can be given at this time. A mask set consisting 169 6×6 grids has been developed for the three grid designs presented here. Several groups including the Max Planck Institute in Bonn, the University of Virginia, and a Caltech-UCSB collaboration plan to test the grids when they become available.

We can crudely estimate the output power for the 36-element sideband generator grid based on the measured double sideband conversion loss of 14.9 dB for a 760-GHz planar integrated Schottky receiver using the same diodes [14]. If we assume the conversion loss will degrade by a factor of two at 1.6 THz, we get an estimated single sideband conversion loss of 20.9 dB. Using this value, and assuming a 100 mW laser we get an estimated output power for the sideband generator grid of $800 \mu\text{W}$ at 1.6 THz before any filtering.

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Chapter 4

Power Grid Oscillator Theory and Design

Recent work on grid oscillators [1]–[5] has convincingly demonstrated proof of concept. However, these grids have all used relatively low-power devices and have not delivered the promised large output powers that make quasi-optical power-combining so attractive. To date, the highest published total radiated power for a grid oscillator is 550 mW at 5 GHz from a 100 element grid [2] and the highest reported power-per-device is 26 mW at 9.6 GHz from a 16 element array of Gunn diodes [4]. These powers are substantially lower than those developed by vacuum tube sources at these frequencies and are even well below the 7.2 W reported for a single monolithic HEMT MMIC chip at 17 GHz [6]. More importantly, these powers are lower than the 10 W to 1 MW needed for effective integration into millimeter-wave systems [7]. This is hardly surprising, however, as these grids used small numbers of low-power devices and little or no attempt was made to design these oscillators for maximum power.

With the above in mind, a power grid oscillator project was initiated to develop substantially more power from a grid oscillator than had been previously reported in the literature and to develop techniques for optimizing grid oscillator output power. Lacking a source of state-of-the-art microwave power transistors, it was decided to design the power grid around a commercial medium-power Fujitsu 0.5 W MESFET chip transistor. While this decision meant that more devices would be required to be combined to get the high-power desired, it would have the desirable effect of showing that high-powers could be achieved with devices

having relatively low performance compared to the best research-grade power-devices now being produced. It also relieved us of the burden of doing both device and circuit development simultaneously.

4.1 OVERVIEW OF POWER OSCILLATOR DESIGN

In order to demonstrate Watt-level powers from a quasi-optical grid oscillator, existing power oscillator design principles must be integrated with quasi-optical grid oscillator theory. Factors which need to be taken into consideration when designing for maximum power include device characteristics, device load impedance and feedback loop gain optimization, heat dissipation, device biasing, and grid edge effects.

The design of power oscillators is in itself a rapidly-evolving subject, particularly with respect to commercial CAD software. We consciously avoided proprietary software and device models except as secondary checks to escape using “black box” solutions that are impossible to duplicate by others without access to a particular version of CAD software. Fortunately, simple load-line analysis and linear theory for oscillator circuit optimization are often reasonably accurate and serve as a solid foundation for future work in this area [8].

The design of power oscillators and amplifiers falls into two general categories: techniques that use linear theory to approximate large signal behaviour of a circuit, and techniques that use full nonlinear analysis and device models to accurately predict large-signal behaviour. Current research almost exclusively focuses on nonlinear analysis. However, nonlinear techniques tend to require large computational resources, elaborate software, and depend on accurate nonlinear models of the components used in the circuit. It is this last requirement that is particularly troublesome. Nonlinear models tend to be either proprietary or require a vast amount of measured data to characterize a specific device [9,10]. Nonlinear device models are almost never available from the manufacturer. Worse, all of our quasi-optical grid equivalent circuits assume the unit cell

is small compared to a wavelength, a serious constraint on nonlinear simulations that require impedance data at harmonics of the fundamental frequency where the current grid models are invalid.

Small-signal s -parameter design has been used to design microwave oscillators with consistent results by many groups [11]–[17]. It has been shown to give a good approximation to the final large-signal oscillation frequency of grid oscillators [2,3] and can even be used to provide an upper-bound for oscillator output power. More importantly, simple load-line techniques [8] and power-gain saturation estimates based on small-signal data [15] can be used to optimize the oscillator embedding network for maximum oscillator power with good results.

The design of a power oscillator grid encompasses more than just the design of a circuit to provide an optimal embedding impedance to the active device. Thermal design is also critical. It is important to ensure that the channel temperatures of the active devices are kept below the maximum safe level if good reliability is to be achieved. Power devices require large dc bias currents, so the dc power sub-system must also be carefully thought out. Finally, we need to understand and minimize the effect the edges of the grid have on grid performance. The remaining sections of this chapter will discuss these concerns in greater detail.

4.2 THERMAL DESIGN

The high powers dissipated by power transistors and the high device densities achieved with quasi-optical grid techniques mean that careful thermal design of the grid is required if the device channel temperatures are to remain within safe limits (typ. $< 150^\circ\text{C}$).

There are basically two paths for the removal of heat from devices loaded in a grid. The heat can be extracted by conduction through the substrate to the grid edges, or the heat can be extracted by convection and radiation to the ambient medium surrounding the grid.

To date, our planar hybrid grids (chip packaged devices) have been fabricated exclusively on *Duroid*, a microwave material with relatively poor thermal conductivity. Consequently, the thermal resistance through the substrate is high, and most of the cooling occurs by radiation and convection to the ambient medium surrounding the grid, in this case air.

To examine the feasibility of cooling a grid by substrate conduction, Michael De Lisio, of Caltech, developed a program to compute the thermal resistance by conduction through a substrate for a square grid with uniform heat flux entering from the top, and grid edges maintained at a constant temperature. This would simulate the case of a grid mounted on a heatsink frame as shown in Figure 4.1. The analysis essentially solves Laplace's equation,

$$\nabla^2 T = 0 \quad (4.1)$$

with boundary conditions $T = T_{sink}$ at the grid edges, and $\psi = \text{const}$ for the top face, and $\psi = 0$ for the bottom face. T is the grid temperature, T_{sink} is the heatsink temperature, a constant, and ψ is the heat density flux at the grid surface. Based on this type of analysis, the temperature will reach a peak at the center of the grid where the devices are furthest from the heatsink. Figure 4.2 shows the expected temperature profile for a grid of 100 Fujitsu FLK052XP chip transistors dissipating 1.2 W per device mounted on a 75-mm square grid for two different 1.6-mm thick substrates. The peak transistor channel temperature at the center of the grid is given by

$$T_{ch} = P_d(R_{th} + R_{gh}), \quad (4.2)$$

where T_{ch} is the transistor channel temperature, P_d is the device power dissipation, R_{th} is the transistor channel to case thermal resistance (25.0 K/W), and R_{gh} is the equivalent grid thermal resistance at the center and is given approximately by

$$R_{gh} = n \left(\frac{0.29}{ka} \right) \left[1 + \left(\frac{0.254a}{t} \right)^{2.55} \right]^{1/2.55} \quad (4.3)$$

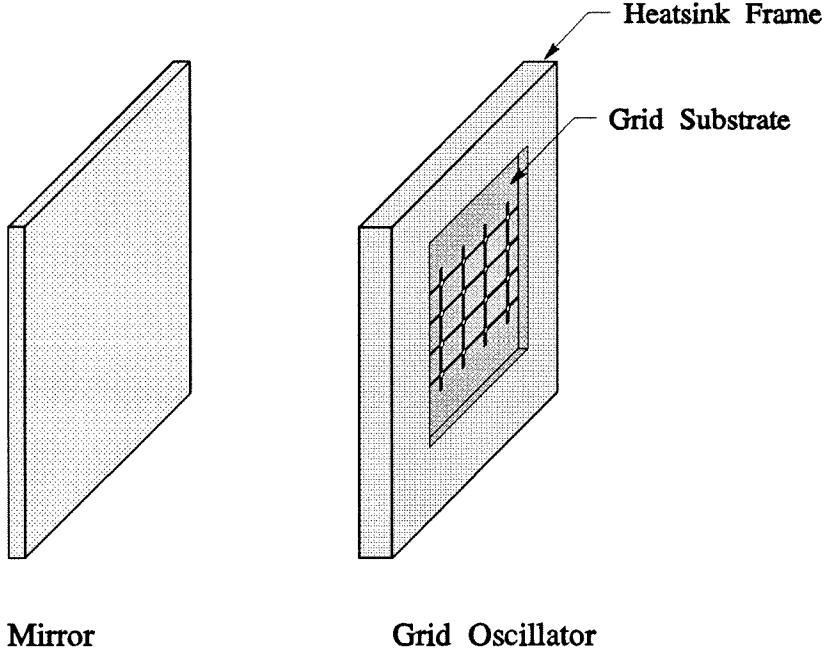


Figure 4.1 Grid cooling by thermal conduction through the substrate to a frame held at a constant temperature.

where a is the grid length, t is the substrate thickness, n is the number of devices in the grid, and k is the substrate thermal conductivity.

For a *Duroid* 5880 substrate, thermal conductivity $k = 0.26 \text{ W/mK}$, and a heatsink temperature of 0°C , the peak theoretical channel temperature assuming conduction cooling only is $21,300^\circ\text{C}$. Using an aluminum-nitride substrate, thermal conductivity $k = 170 \text{ W/mK}$, the channel temperature is 62.5°C , a value well below the maximum safe channel temperature of 150°C .

These simulations show that a grid using *Duroid* cannot rely exclusively on heat conduction through the substrate for cooling the active devices. If heat conduction was the only criteria, these results indicate a grid built on Al-N would be preferable to one built on *Duroid* when large powers need to be dissipated. Unfortunately, the dielectric constant of Al-N, $\epsilon_r = 8.6$, is much higher than *Duroid* 5880, $\epsilon_r = 2.2$, and past results for grid oscillators on high-dielectric

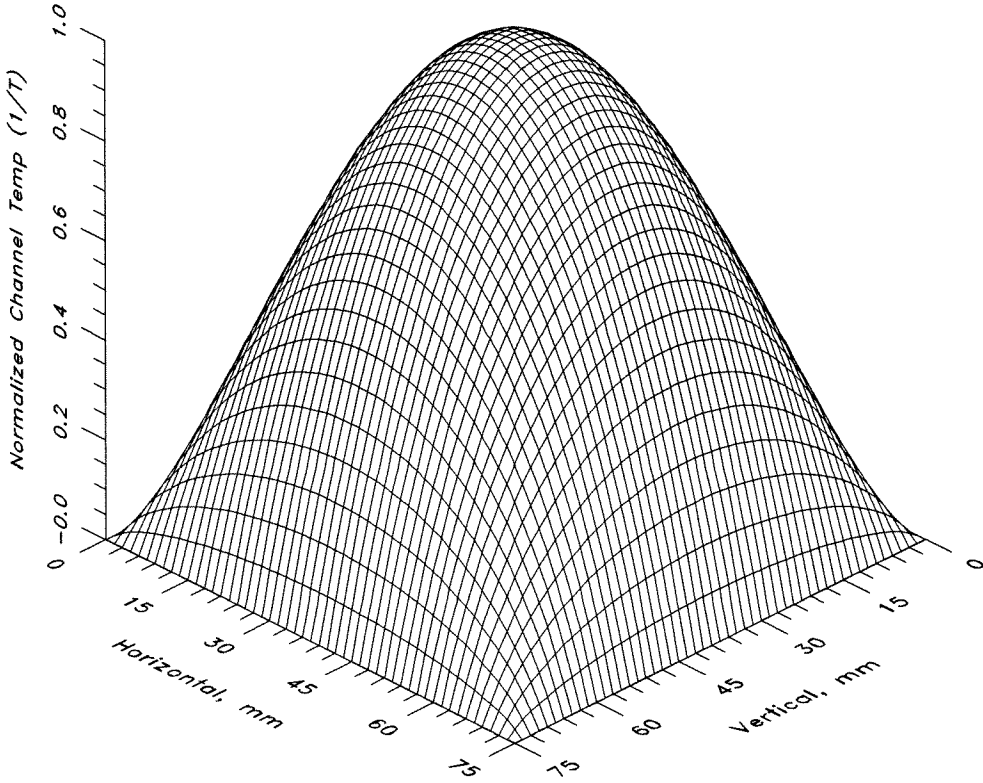


Figure 4.2 Normalized transistor channel temperature profile for 100 Fujitsu FLK052XP MES-FET transistors dissipating 1.2 W per device. The grid is assumed to be 75-mm square and 1.6-mm thick. The theoretical peak channel temperature is 21,300°C for a *Duroid* 5880 substrate, and 62.5°C for an aluminum-nitride substrate.

constants have been unsuccessful. For this reason, we were reluctant to use Al-N, and instead investigated cooling the grid using forced-air convection.

Modelling heat flow by convection is much more difficult than the conduction case described above. Simple models to describe convection are not available, and most published work is empirical in nature [18]. For this reason, we did not try to model convection heat flow. Instead, in order to characterize the grid thermal resistance due to convection, a thermocouple was used to measure the case temperature of low-power devices mounted to a grid fabricated out of *Duroid*. Another alternative would be to use resistors in place of the low-power

devices. By computing the power dissipated by the devices, it was then possible to compute the thermal resistance of the grid. This thermal resistance, along with the high-power device case-to-channel thermal resistance could then be used to predict the channel temperatures for the high-power transistors.

Figure 4.3 shows the measured temperature profile for a 25-element grid on a *Duroid* 5880 substrate. The grid is 43-mm square and the average power dissipated per device was 109 mW. The temperature distribution is very irregular. This is most likely due to variations in power dissipation per device, some devices being biased at greater currents than others, as they all share a common gate bias voltage, and the pinch-off voltage varies substantially from device to device. We see that the device temperatures peak a little toward the center of the grid, but in general the temperature distribution does not follow the theoretical distribution for conduction cooling shown in Figure 4.2. This is to be expected because the poor thermal conductivity of *Duroid* implies most of the cooling must be through convection. Convection cooling should give a more uniform temperature distribution because the majority of heat will flow through the front and back faces of each unit cell, and this area is constant regardless of cell position in the grid.

Figure 4.4 shows the extrapolated channel temperature, based on measurements of the 25-element grid, for a 100-element grid of transistors dissipating 1.2 W per device. In still air, an average grid thermal resistance of 370 K/W was calculated. Corresponding channel temperatures for the Fujitsu FLK052XP MESFET would approach 400° C at the recommended Q-point. This was clearly unacceptable. To reduce this temperature, forced-air cooling with a refrigerated heat exchanger was implemented. The forced-air was directed along the grid surface from a nozzle pointing from the side of the grid. Using this setup, the measured average grid thermal resistance dropped to 130 K/W and the Fujitsu FLK052XP predicted channel temperature dropped to 175° C. While 175° C

channel temperature is still higher than desirable, and would be unacceptable for a commercial product where long term reliability is critical, it was considered adequate for a grid that was experimental in nature.

Clearly, thermal design is an important consideration when designing high-power quasi-optical grids. Our work has shown that power grid cooling requirements can be satisfied through the use of high-thermal-conductivity substrates such as aluminum-nitride, or even diamond for monolithic grids that are sufficiently small that the cost of a diamond substrate is not prohibitive. Diamond has a thermal conductivity almost 8 times better than Al-N, and simulations have shown that power densities of at least 100 kW/m^2 can be safely handled by a GaAs grid glued to a diamond substrate. For hybrid grids built on *Duroid*,

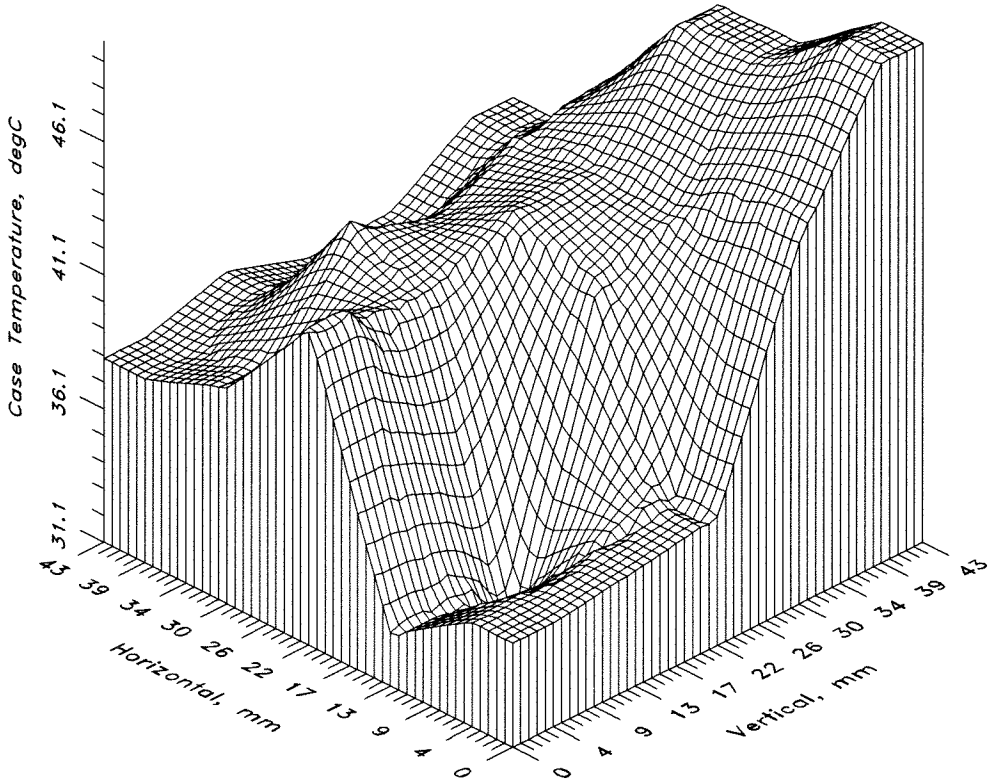


Figure 4.3 Measured transistor case temperature profile for a 25-element MESFET grid on *Duroid* 5880 with forced-air blown across the grid's front face. The grid is 43-mm square and 2.5-mm thick. The total power dissipation was 2.7 W for the grid.

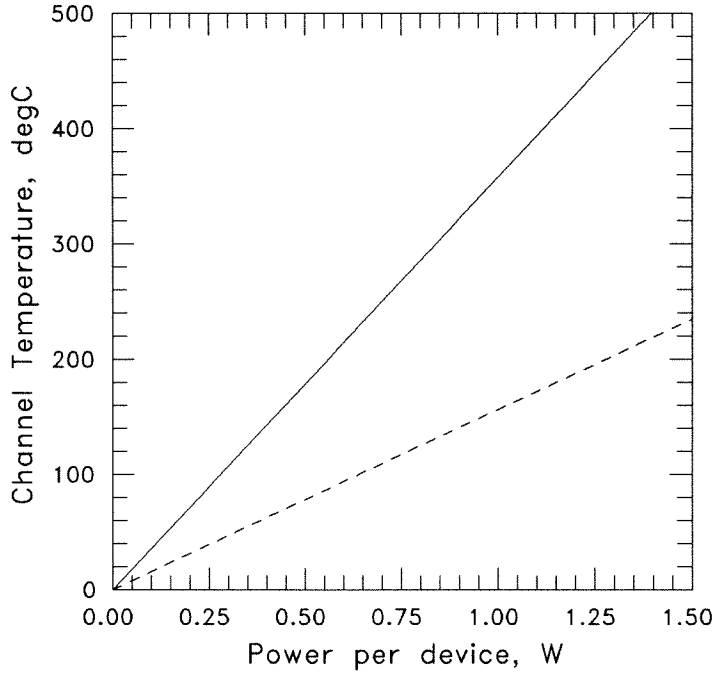


Figure 4.4 Extrapolated channel temperatures for a Fujitsu FLK052XP MESFET as a function of device power dissipation. Data is taken from temperature measurements of a 25-element grid. In still air (—) the channel temperature reaches an undesirable 400°C at 1.2 W. With forced-air cooling (---) the channel temperature drops to 175°C, still a little high, but acceptable for an experimental grid.

refrigerated forced-air convection cooling is the only way to keep power devices sufficiently cool. Forced-air cooling will decrease the thermal resistance of a *Duroid* grid almost three times over the same grid in still air. The use of forced-air cooling allows grids to be built on low-dielectric constant *Duroid* substrates. Such substrates allow larger unit cells to be used which helps ease fabrication tolerances. Grid oscillators built on high-dielectric constant substrates are still poorly understood and have performed poorly in the past for reasons that are still not understood at this time. For this reason, forced-air cooling of a grid oscillator built on *Duroid* was chosen for this project even though Al-N substrates theoretically have superior cooling abilities.

4.3 TRANSISTOR LOAD IMPEDANCE OPTIMIZATION

In order to get the most power out of the transistors, the grid must be designed to provide an optimum impedance across the transistor drain-source terminals. Ideally, a nonlinear model for the transistor would be used to simulate the saturated transistor in the grid circuit. Unfortunately, this method, although evolving rapidly, is still very cumbersome to implement with available microwave CAD systems. In addition, nonlinear analysis requires grid embedding impedance data at harmonics of the fundamental design frequency which can not be reliably determined using our existing EMF grid models. Fortunately, approximations can be made that allow linear design tools to be substituted with reasonable accuracy.

One such approximation is based on a simple load-line analysis described by Cripps [8,16]. This simple theory can be used to compute the approximate optimal load impedance to present to the transistor for maximum power. This method has been employed successfully for years in the design of power amplifiers. Indeed, a state-of-the-art 7 W Ku-Band monolithic amplifier chip was recently presented that was designed using this method [6].

The optimal load is defined as the impedance that allows the transistor output terminals to swing between the maximum allowable voltage and current limits. This optimal load resistance R_{opt} is given by

$$R_{opt} = \frac{2V_{DC}}{I_{DSS}}, \quad (4.4)$$

where V_{DC} is the drain-source dc bias voltage and I_{DSS} is the maximum saturated drain current. This resistance is presented to the current source terminals of the transistor equivalent circuit as shown in Figure 4.5.

For the Fujitsu FLK052XP transistor, biased at the recommended drain-source voltage of 10 V and drain current of 120 mA, the optimal load impedance is 83Ω . If the load impedance is less than the optimal value, the design will be

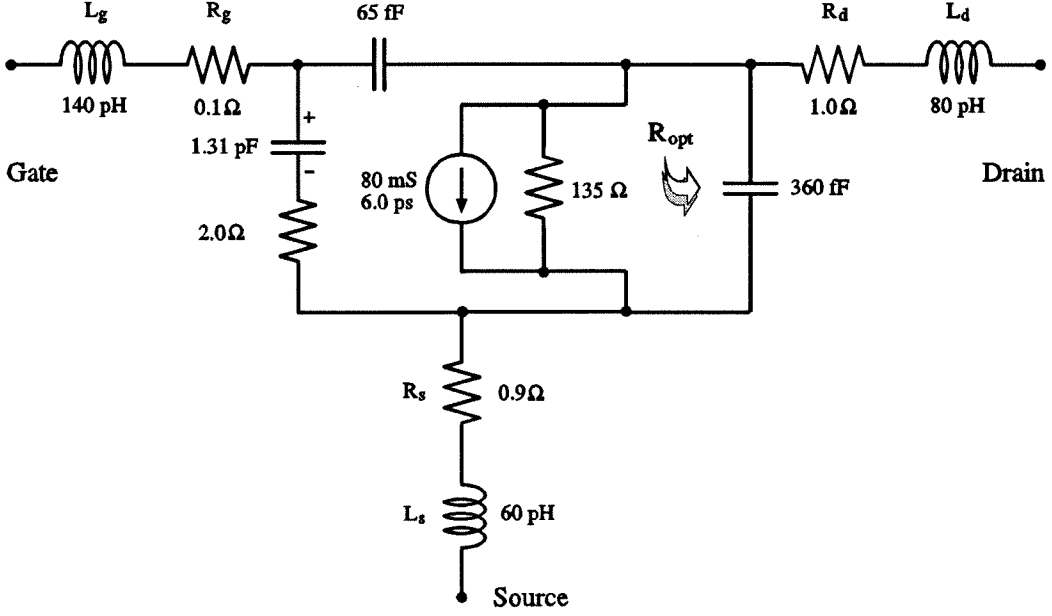
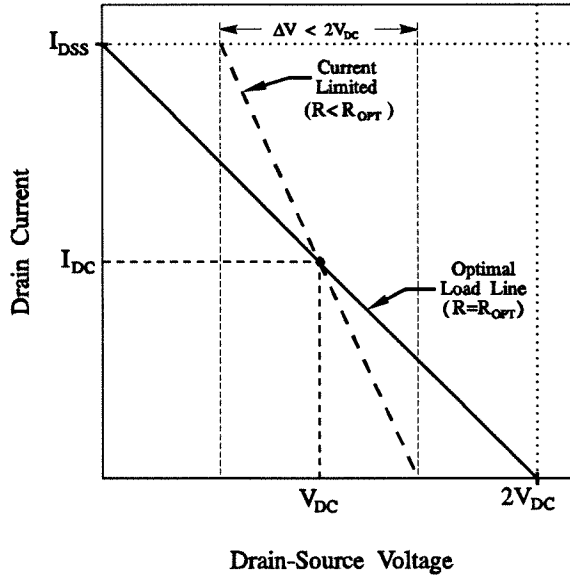


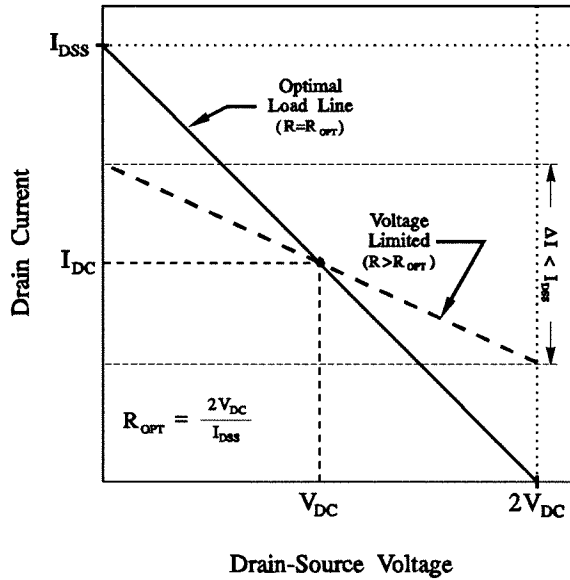
Figure 4.5 Linear lumped-element model for the Fujitsu FLK052XP MESFET. The approximate optimal load impedance R_{opt} calculated using (4.4) is presented across the terminals of the internal current source of the MESFET model.

current-limited, and the voltage across the output will be less than the maximum allowed as shown in Figure 4.6(a). Similarly, if the load impedance is too large, the design will be voltage-limited, and the current through the output terminals will be less than the maximum allowed as shown in Figure 4.6(b). Either case will result in less power being delivered to the load.

Although defining the approximate optimum load impedance R_{opt} is relatively simple, designing a grid oscillator to present that impedance to the transistor is quite challenging. The design and modelling of grid oscillators has been described in detail previously and need not be repeated here [2]. Concisely, the grid oscillator is reduced to an equivalent circuit using one of the techniques described in chapters 2 and 3 of this thesis. The transistor model is then connected to this circuit and the internal loop gain of the oscillator is computed using linear analysis. The grid dimensions are adjusted until the loop gain has a magnitude



(a)



(b)

Figure 4.6 Simple load line theory can be used to find the approximate load impedance to present to the drain-source terminals of the device to permit simultaneous development of peak voltage and current swing at the transistor terminals. (a) The case where the load impedance is too low and the transistor is current-limited. (b) The case where the load impedance is too high and the transistor is voltage-limited.

greater than unity and 0° phase at the desired oscillation frequency.

In order to simulate the load impedance presented to the transistor, a commercial linear microwave design package, Hewlett-Packard's *Microwave Design System*, was used to model the circuit [19]. The internal feedback loop of the circuit was broken at the voltage-controlled current source of the MESFET model. A known current was injected into the circuit at this point and the corresponding voltage across the gate-source capacitor computed, as well as the currents and voltages at the nodes within the circuit. Using this technique, both the loop gain and impedance at the transistor terminals could be simulated. In addition the percent of power delivered to the load, in this case free space modelled as a $377\ \Omega$ resistor, could also be determined to find the relative amount of power fed back to the transistor input terminals, and that delivered to the load. Figure 4.7 shows an example of an equivalent circuit used to model a grid having a crossed-dipole metal pattern.

The design approach for optimizing load impedance was largely empirical. Simulations were made to determine the required grid dimensions to achieve the desired optimum load impedance at the frequency of oscillation. By varying substrate thickness, the grid pattern, unit cell size, and the mirror separation behind the grid, it is usually possible to obtain a circuit that oscillates at the desired frequency and provides the desired load impedance to the transistor.

4.4 TRANSISTOR FEEDBACK OPTIMIZATION

For maximum oscillator power, Johnson has shown that the transistor must be operating at the point where maximum power-added efficiency occurs [15]. Since this is a function of gain compression, or transistor saturation, it can be controlled by varying the amount of feedback applied to the transistor. Too little feedback will result in not enough saturation of the transistor, resulting in low output power. Too much feedback will cause too much power to be fed back to the transistor, decreasing available output power as well as potentially damaging

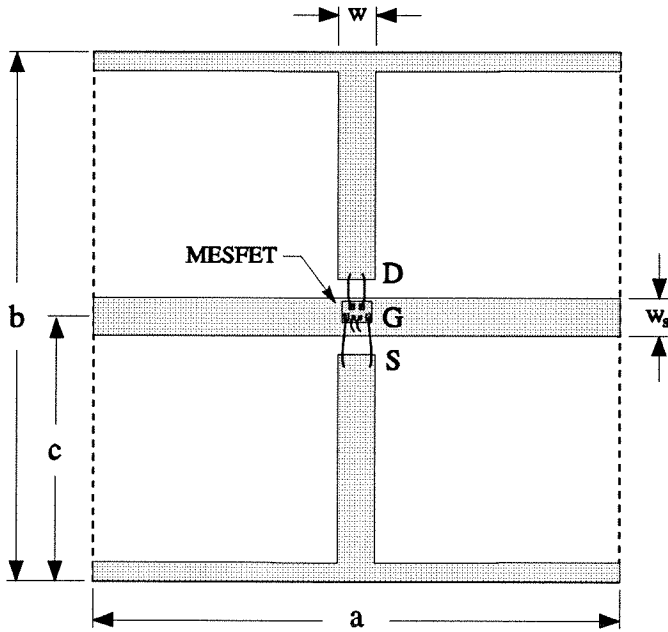
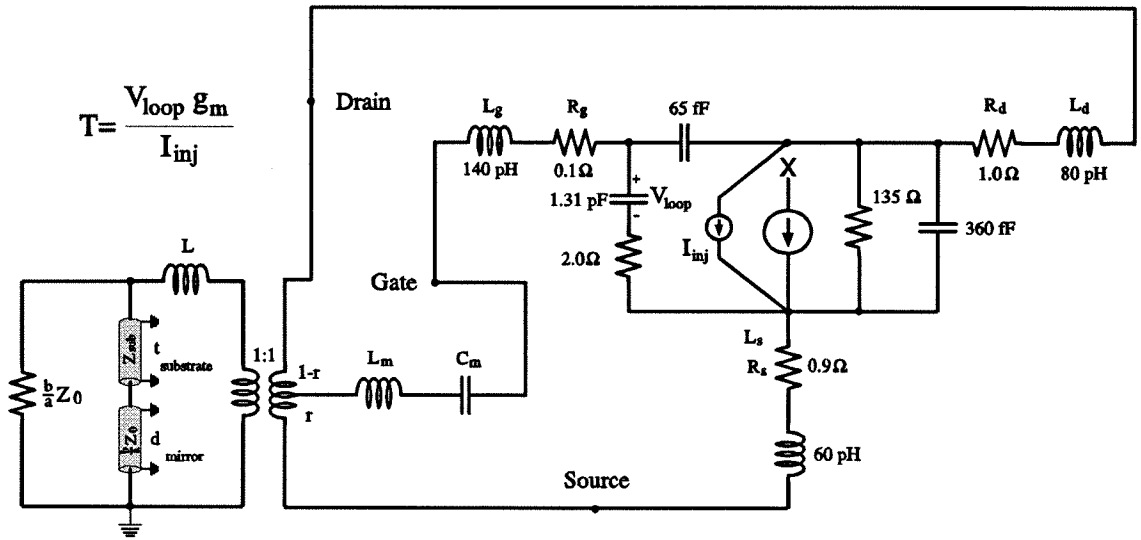


Figure 4.7 Equivalent circuit used to compute the loop gain and transistor load impedance for the grid pattern shown. In the equivalent circuit $r = c/b$.

the devices.

The oscillator output power P_{osc} is given by

$$P_{osc} = P_{out} - P_{in}, \quad (4.5)$$

where P_{out} is the output power of the transistor, and P_{in} is the power fed back to the transistor input. Since P_{out} cannot increase above the saturated power of the transistor, a plot of P_{osc} versus P_{in} will show a maximum value for some intermediate value of P_{in} (Figure 4.8).

The maximally-efficient power gain G_{ME} is defined by Kotzebue [20] as the power gain which maximizes the two-port added power for a given input power,

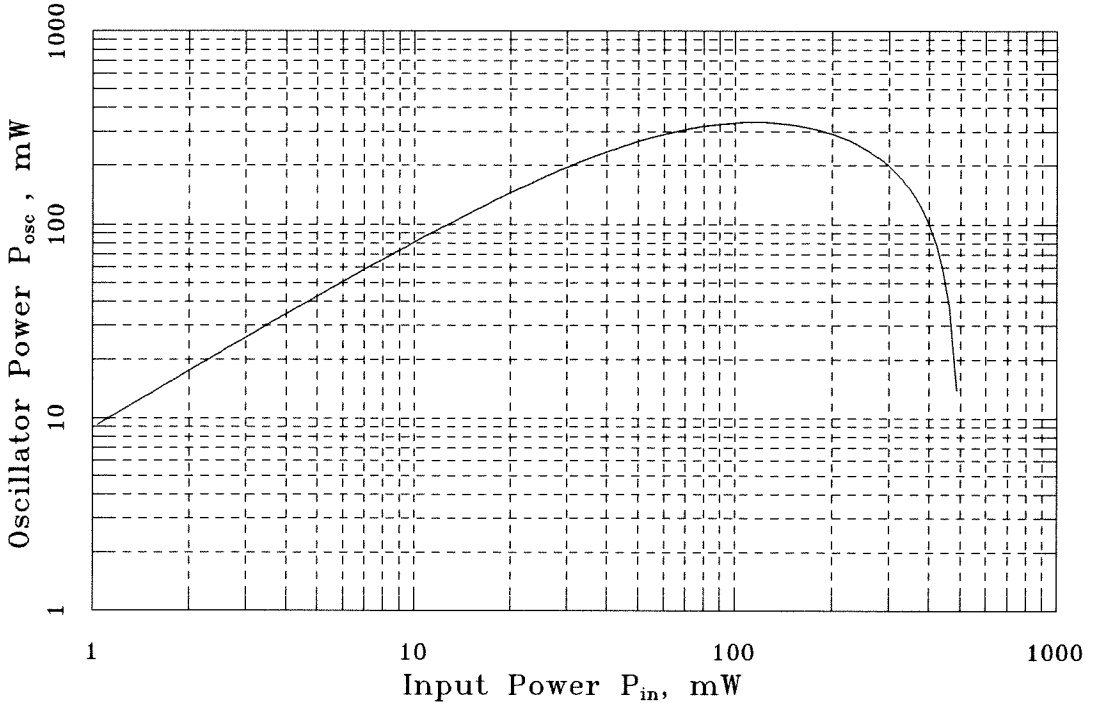


Figure 4.8 A plot of oscillator output power P_{osc} versus input power P_{in} for the Fujitsu FLK052XP at 10 GHz. The peak power of 330 mW occurs at 4 dB of gain compression.

that is, the gain that maximizes $(P_{out} - P_{in})/P_{in}$ and can be computed using

$$G_{ME} = \frac{\left| \frac{s_{21}}{s_{12}} \right|^2 - 1}{2 \left[K \left| \frac{s_{21}}{s_{12}} \right| - 1 \right]}, \quad (4.6)$$

where K is the Rollett stability factor given by

$$K = \frac{1 + |s_{11}s_{22} - s_{21}s_{12}|^2 - |s_{11}|^2 - |s_{22}|^2}{2|s_{12}||s_{21}|}. \quad (4.7)$$

We can approximate the power saturation curve of a MESFET using the following exponential fit

$$P_{out} \simeq P_{sat} [1 - e^{(-G_{MEss} P_{in} / P_{sat})}], \quad (4.8)$$

where P_{sat} is the maximum saturated power of the transistor and G_{MEss} is the small-signal maximally-efficient gain computed using the transistor small-signal s -parameters and equation (4.6). We solve for maximum oscillator power by maximizing $P_{out} - P_{in}$, that is by solving $\partial P_{out} / \partial P_{in} = 1$, which gives us

$$P_{osc}(max) = P_{sat} \left[1 - \frac{1}{G_{MEss}} - \frac{\ln G_{MEss}}{G_{MEss}} \right]. \quad (4.9)$$

The corresponding maximally-efficient gain that gives maximum oscillator power, G_{MEsat} , is then

$$G_{MEsat} = \frac{G_{MEss} - 1}{\ln G_{MEss}}. \quad (4.10)$$

The required level of saturation can then be determined by the simple formula

$$SAT = G_{MEss} - G_{MEsat}. \quad (4.11)$$

An analysis of the Fujitsu FLK052XP MESFET was made using the above formulas to find the theoretical maximum power we can expect from this device when used as an oscillator, and the appropriate level of saturation to achieve that power level. Table 4.1 summarizes the results for the frequency range from

8 to 12 GHz. At 10 GHz, we can expect a maximum output power of 338 mW per device at 4.1 dB of gain saturation.

Grid oscillator designs to date have used unit cells that provide a feedback path that is largely internal to the grid. This intra-grid feedback is difficult to control with any precision by varying the usual physical grid parameters such as unit cell size and lead widths. The resulting feedback also tends to be much larger than is desirable from the standpoint of maximum oscillator output power.

An examination of the equivalent circuit for the crossed-dipole grid used with good success in the past for grid oscillators (Figure 4.9) shows that the components that most directly affect feedback are the center-tapped inductor, L_m , and capacitor, C_m , of the grid equivalent circuit. The values of both of these components are complicated functions of many variables that describe the unit cell geometry. It is not generally possible to adjust these components individually without affecting the values of everything else in the equivalent circuit. However, it is possible to gain some control over these components by altering the shape and position of the horizontal strip that connects to the gate of the

Frequency (GHz)	K	G_{MEss} (dB)	G_{MEsat} (dB)	Sat (dB)	P_{osc} (W)
8.0	1.13693	10.963	6.579	4.384	0.359
8.5	1.15619	10.697	6.395	4.301	0.353
9.0	1.12439	10.558	6.300	4.258	0.349
9.5	1.09726	10.398	6.191	4.207	0.345
10.0	1.07849	10.114	5.998	4.117	0.338
10.5	1.03858	9.848	5.818	4.030	0.331
11.0	1.01428	9.623	5.666	3.957	0.325
11.5	0.96557	9.452	5.552	3.900	0.320
12.0	0.81539	9.821	5.800	4.022	0.330

Table 4.1 Maximum saturated power calculations for the Fujitsu FLK052XP MESFET.

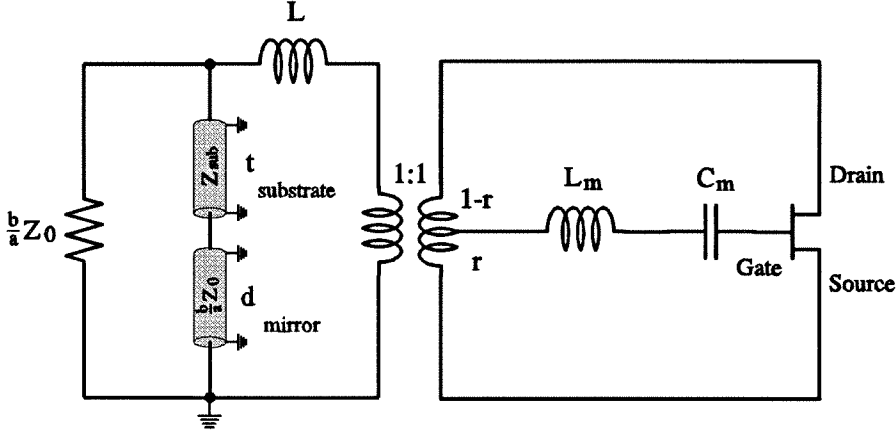
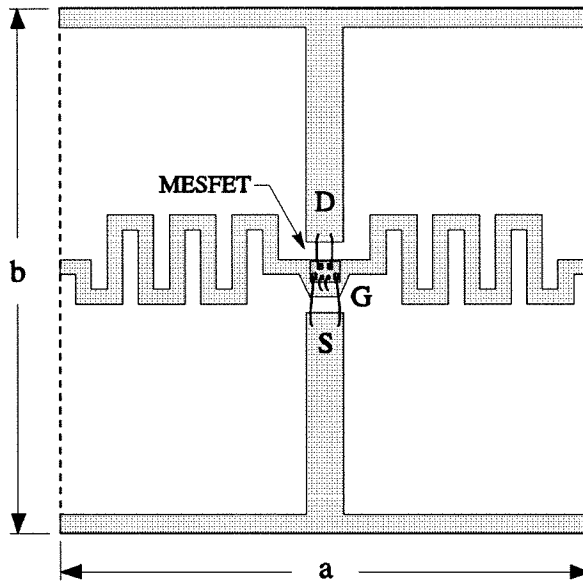


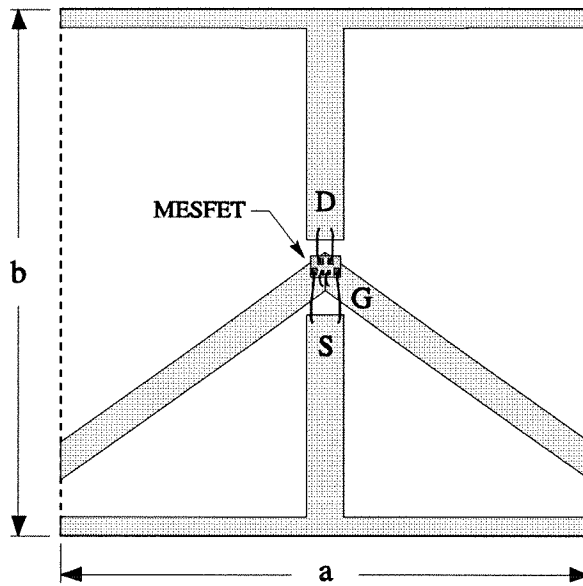
Figure 4.9 Equivalent circuit for the crossed-dipole grid oscillator with the horizontal strip of the grid unit cell connected to the gate of the transistor.

transistor. Figure 4.10 shows the basic idea. To increase the inductance L_m , we can *meander* the center lead as shown in Figure 4.10(a). This will decrease the internal feedback loop gain. To vary the capacitive coupling to the center lead, we can bend the center lead into a V-shape as shown in Figure 4.10(b). If the strip is bent closer to the vertical strip connected to the transistor's drain, drain-gate coupling, and hence feedback loop gain, should increase. Conversely, if the strip is bent closer to the vertical strip attached to the transistor's source, drain-gate coupling should decrease.

Of these two schemes, the meandered center lead is the easiest to implement as the same equivalent circuit can be used that was found for the original crossed-dipole unit cell EMF analysis shown in Figure 4.9. The value of the inductance L_m is computed using the HP structure simulator in a manner very similar to that outlined for the design of the sideband generator grid described in chapter 3. The inductance L in Figure 4.9 is computed from simulations of a grid with short-

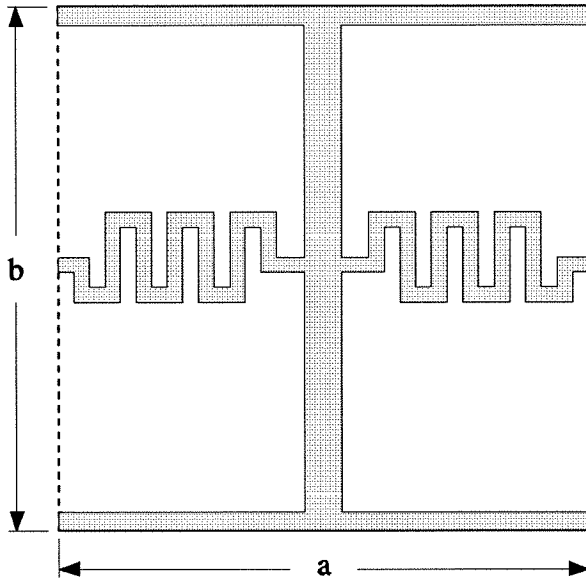


(a)

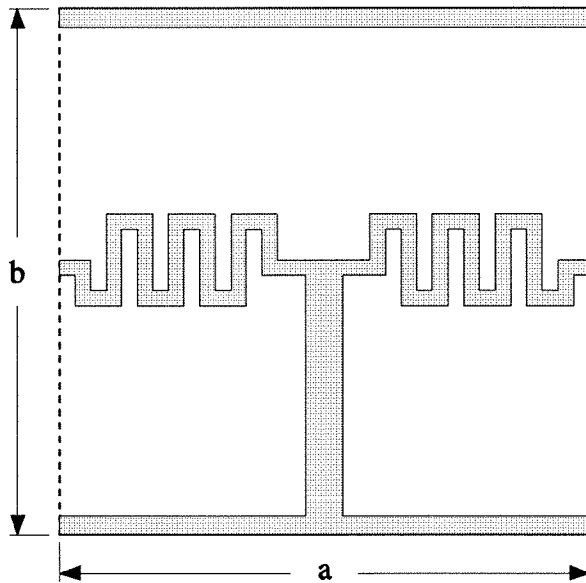


(b)

Figure 4.10 Controlling intra-grid feedback loop gain. (a) Meandering the horizontal strip connected to the transistor's gate can be used to increase the value of L_m . (b) Bending the horizontal strip towards or away from the vertical strip connected to the transistor's drain lead varies the drain-gate coupling.



(a)



(b)

Figure 4.11 The HP structure simulator can be used to find the equivalent circuit elements of Figure 4.9 for the meandered grid. (a) Unit cell used to find L . (b) Unit cell used to find L_m and C_m .

circuits across the two internal ports of the grid as shown in Figure 4.11(a). One short is then removed and the grid is re-simulated to get the values of C_m and L_m as shown in Figure 4.11(b). To extract both C_m and L_m , it is helpful to add a mirror behind the grid, which will add another reactive element to the circuit. A plot of impedance looking into the grid will usually show several distinct resonances, one between L_m and the mirror from which L_m can be determined, and another between L_m and C_m which can be used to determine C_m .

Figure 4.12 shows a plot of L_m versus total meander width for 0.15-mm wide meander line and 7.35-mm square unit cell. The corresponding inductance computed using the EMF method for a straight strip of equal width is also shown. By varying the meander width, a reasonable range of inductance values can be achieved. For the widths plotted, the meander inductance is nearly double the straight strip value. Note that an analysis of meander-line inductance that assumes a uniform current distribution along the meander line will not give accurate values for L_m . This is because the current distribution along a horizontal meander line in the unit cell is not uniform as shown in Figure 4.12. Unless this current distribution is accounted for in the model, estimates of L_m will be too large.

Using a meandered horizontal strip is not a completely independent method of controlling feedback loop gain because it also affects the oscillation frequency and transistor load impedance. However, it was determined that varying the device offset within the unit cell and increasing the gate lead inductance allows the feedback to be reduced while preserving the desired transistor drain-source load impedance. Empirically, it was observed that increasing the gate lead inductance lowers the loop gain, but also lowers the real impedance and increases the inductive reactance presented to the transistor drain-source terminals. It also tends to shrink the unit-cell size for a given oscillation frequency. The in-

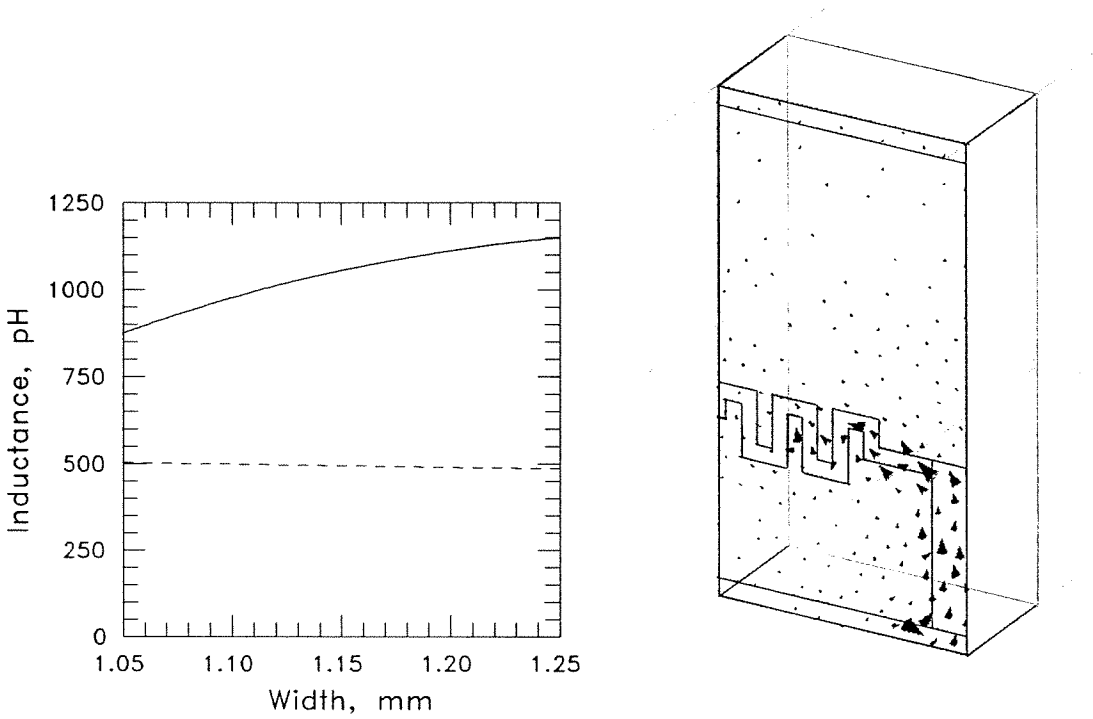


Figure 4.12 Plot of L_m versus meander width for a meander line (—) and L_m versus strip width for a straight strip (---). Values shown are for a 7.35-mm square unit cell on an $\epsilon_r = 2.2$ substrate. The current distribution for the meander line computed by the HP structure simulator is also shown.

crease in inductive reactance can be compensated for by offsetting the transistor position in the unit cell so that the drain-lead length is shortened. Fine tuning of the mirror position can then be used to find the point where the loop gain and real resistance presented to the transistor are as close as possible to the desired values.

4.5 GRID EDGE TERMINATIONS

Our simulations assume grids that are infinite in extent so that we may use symmetry to simplify the analysis. Obviously this is not the case for grids that

are actually built and tested in the lab. For this reason, care must be taken to try to simulate the boundary conditions at the physical edges of the grid to approximate as closely as possible the magnetic and electric walls assumed in the analysis.

An electric wall looks like a short circuit. For a grid edge that is to simulate an electric wall, we want the impedance presented to the edge to be as low as possible. Weikle has used quarter-wave open-circuited stubs for this purpose [3]. The quarter-wave stubs transform the open-circuit at one end of the stub to a short-circuit at the other end. If the edge of the grid is connected to the short-circuit end of the stub, the resulting low-impedance should approximate an electric wall at the grid edge. The required electrical length is computed assuming a guide wavelength that is the mean of the free space and substrate values

$$\lambda_g = \frac{\lambda_0}{\sqrt{\frac{\epsilon_r + 1}{2}}}. \quad (4.12)$$

A magnetic wall is harder to simulate. One reasonable approximation is an open circuit at the grid edge. Unfortunately, the magnetic walls are along the vertical grid edges that must be connected to the dc power supply. Popović empirically determined that ferrite beads on the bias wires can be used to increase the inductance of the dc supply at the grid edges to better simulate an open circuit [2]. For a power grid, the bias currents are quite large, and the use of ferrite beads is not always adequate as the ferrite will saturate. Consequently, several alternative edge terminations for simulating magnetic walls were investigated.

Figure 4.13 shows a high-impedance bias connection using a thin ferrite slab glued on top of a meander line. A plot of the reactance of this termination at the grid edge is shown in Figure 4.13 from 8 to 12 GHz. The impedance is seen to be relatively large and frequency insensitive. Alternatively, the meander line can be replaced with 0.7-mil diameter gold bond wires with similar results. The

bond wires are added in parallel until the required current handling capability is achieved.

An alternative approach is to use a guide structure at the grid edge to mirror the boundary condition at an adjacent cell wall. If the guide is a half-wavelength long, the impedance at one end of the guide will be mirrored at the other end. If both ends of the guide terminate on a unit cell magnetic wall, then symmetry will be maintained. Figure 4.14 shows the basic idea. A U-shaped planar metal strip is used to connect adjacent rows together. The path length of the metal is adjusted to be a half-wavelength at the design frequency. The HP structure simulator can be used to find the guide wavelength of the structure and the pathloss for a wave travelling from one end of the guide to the other. Simulations show that approximately 1 dB of loss can be expected for a half-wavelength guide.

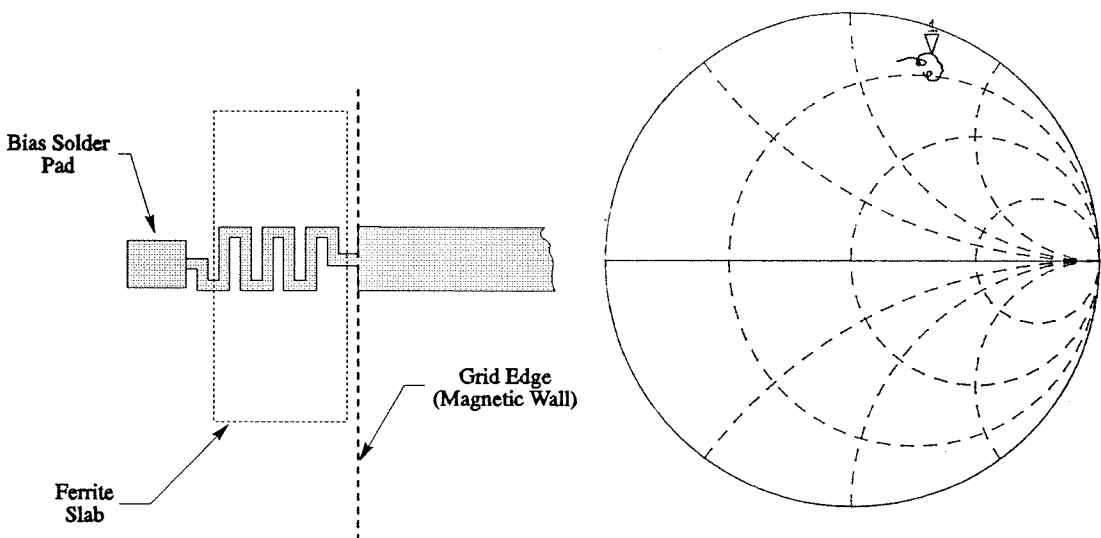


Figure 4.13 A ferrite slab glued over bond wires or a meander line can be used to approximate a magnetic wall at the grid edge. The impedance data ($50\ \Omega$) is from 8–12 GHz; the marker is at 10 GHz.

A grid oscillator built using these structures to simulate magnetic walls on the vertical edges oscillated at 20% above the design frequency and radiated very little power. Removing the guide structures reduced the oscillation frequency and an 18-dB increase in output power was observed. One explanation for this behaviour is that the structures only work at the design frequency where they are a half-wavelength long. At other frequencies, the mirroring effect will not occur and the grid edge impedance will be very different, possibly allowing undesired oscillation modes to occur.

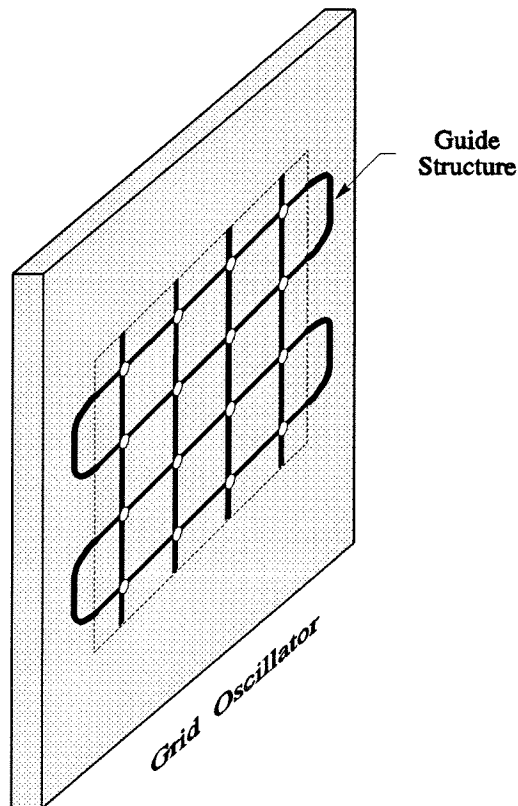


Figure 4.14 A U-shaped metal strip a half-wavelength long can be used at the grid edge to couple adjacent cells together to maintain symmetry. Such an edge termination can be used to simulate electric or magnetic walls.

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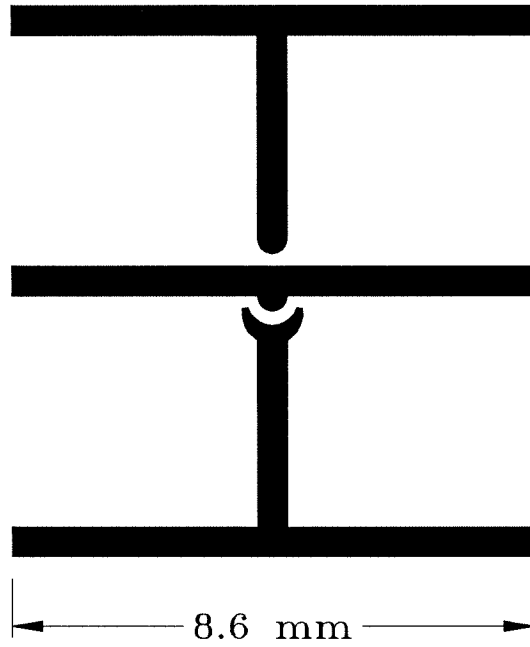
Chapter 5

Power Grid Oscillator Measurements

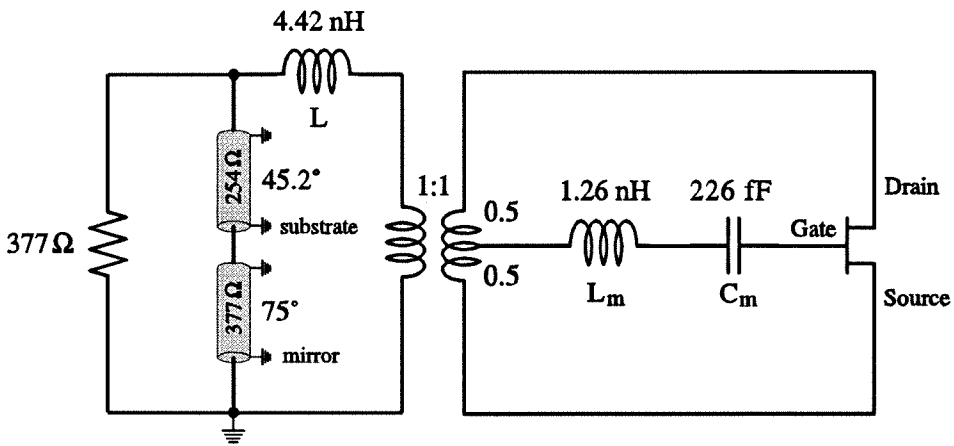
In the previous chapter the theory for the design of grid oscillators for maximum output power was presented. This chapter attempts to experimentally verify these procedures. Four power grid oscillator designs are presented along with experimentally measured results. The grids represent a progression from a simple design based only on optimizing transistor load impedance, to more complicated grid designs that attempt to control load impedance, feedback loop gain, and device parasitics. Medium power Fujitsu FLK052XP MESFET chip transistors were used as the active device and the grid substrates were *Duroid* 5880 with a dielectric constant $\epsilon_r = 2.2$. All the fabricated grids were 16-element arrays with the exception of the fourth design, that was also built as a 100-element grid. This grid achieved the highest total radiated power of any grid reported to date, 10.3 W.

5.1 POWER GRID ONE

The first power grid oscillator design uses a conventional crossed-dipole unit cell pattern. The unit cell was designed to present the optimum load impedance to the transistor at the oscillation frequency as discussed in Section 4.3. Figure 5.1 shows the unit cell dimensions of the grid and the corresponding equivalent circuit used to predict the grid oscillation frequency and transistor load impedance. The unit cell is 8.6-mm square and the bias lines are 0.5-mm wide. The *Duroid* 5880 substrate is 2.54-mm thick. The component values for



(a)



(b)

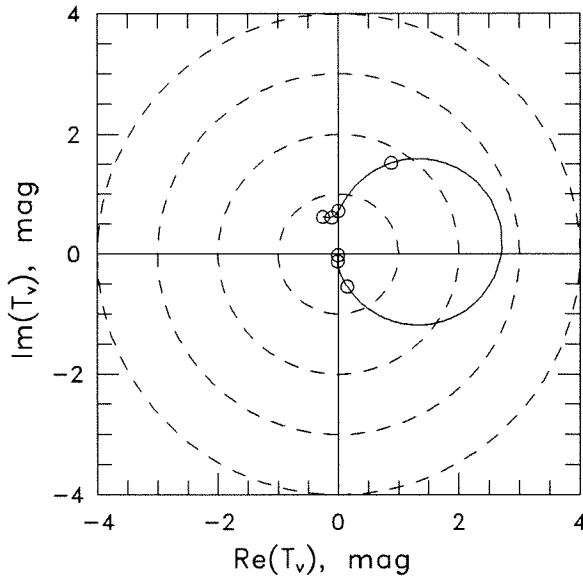
Figure 5.1 (a) Unit cell metal pattern for Power Grid 1. The grid was designed for optimum transistor load impedance only. (b) Equivalent circuit model used to predict the theoretical performance of the grid. Values were calculated based on an induced EMF analysis of the grid equivalent waveguide unit cell.

the grid equivalent circuit were obtained from an EMF analysis of the unit cell equivalent waveguide [1].

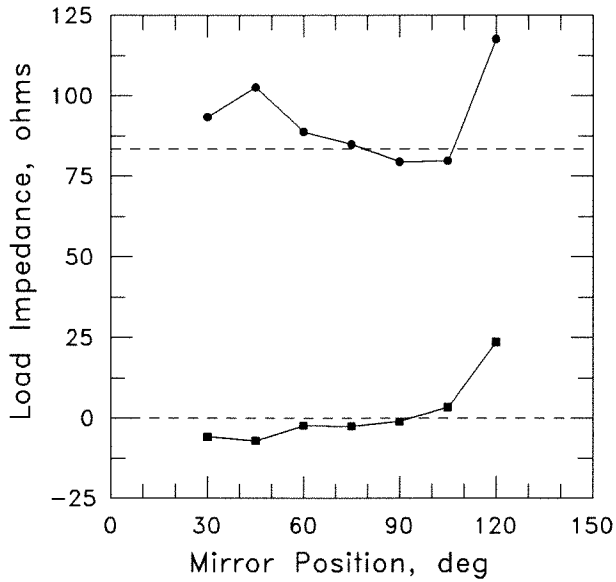
Figure 5.2(a) shows the theoretical feedback loop gain based on the equivalent circuit of Figure 5.1. The predicted oscillation frequency is 9.94 GHz and the unoptimized loop gain at this frequency is 2.6 (8.3 dB). Figure 5.2(b) shows the theoretical load impedance presented to the transistor as a function of mirror position at the oscillation frequency. The grid was optimized to present $83\ \Omega$ to the transistor output terminals. Note that at microwave frequencies, the effects of parasitic elements, especially the output capacitance, must be de-embedded as part of the external load before this simple theory is applied (refer to Figure 4.5 for the definition of R_{opt}). The grid is seen to present the desired load impedance to the transistor over a wide range of mirror positions.

Figure 5.3 shows a photograph of the fabricated 16-element grid. The chip transistors were soldered to the gold-plated copper traces of the *Duroid* substrate. 0.7-mil diameter gold wire was used to connect the transistor terminals to the grid with a commercial wire bonder. The peak total radiated power for the grid was 1.48 W, which corresponds to 92.5 mW per device. This is substantially higher than the reported power-per-device of 26 mW at 9.6 GHz for a grid of Gunn diodes [2] and 21 mW per device at 5 GHz for a grid of MESFET transistors [3]. The grid drain-source bias voltage was 7.15 V and the total drain current for the grid was 980 mA resulting in an overall dc-to-rf efficiency of 21%. This efficiency is significantly higher than the 2% reported for the Gunn diode grid [2], and similar to the 20% reported for the 5 GHz MESFET grid [3].

Table 5.1 summarizes the measured and theoretical parameters of interest for the grid. A simple-minded approach was taken to predict the output power. The dc bias current and voltage were assumed to place upper limits on the peak voltage and current that the current source of the MESFET model can deliver to the load. The power delivered to the load was computed assuming a peak voltage



(a)



(b)

Figure 5.2 (a) Theoretical loop gain of Power Grid 1 from 5 to 15 GHz. The predicted oscillation frequency is 9.94 GHz and the loop gain is 8.3 dB. 100 MHz intervals are marked with a (o). (b) Theoretical load impedance presented to the transistor as a function of mirror spacing at the frequency of oscillation. The load impedance is split into real (•) and imaginary (■) plots. The dashed lines are the theoretical values for maximum output power.

of 7.15 V (5.06 Vrms) across the current source which gives a corresponding load power of 99.7 mW. This is very close to the measured value of 92.5 mW per device. Predicting the power for the dc bias drain current is more complicated as the two middle-rows were biased at 48 mA per device and the two edge-rows at 75 mA per device. Using the higher current of 75 mA predicts a load power of 66.0 mW per device, and the lower current predicts a power of 27.0 mW per device. Adding the powers together predicts a total grid power of 0.74 W, 3.0 dB lower than measured. These calculations are consistent with the load line theory. The optimum load impedance for a bias of 7.15 V and 75 mA is $95\ \Omega$, which would suggest the grid, which was designed for an optimum load impedance of $83\ \Omega$, is current-limited. In light of the simple nature of this theory, and also noting that

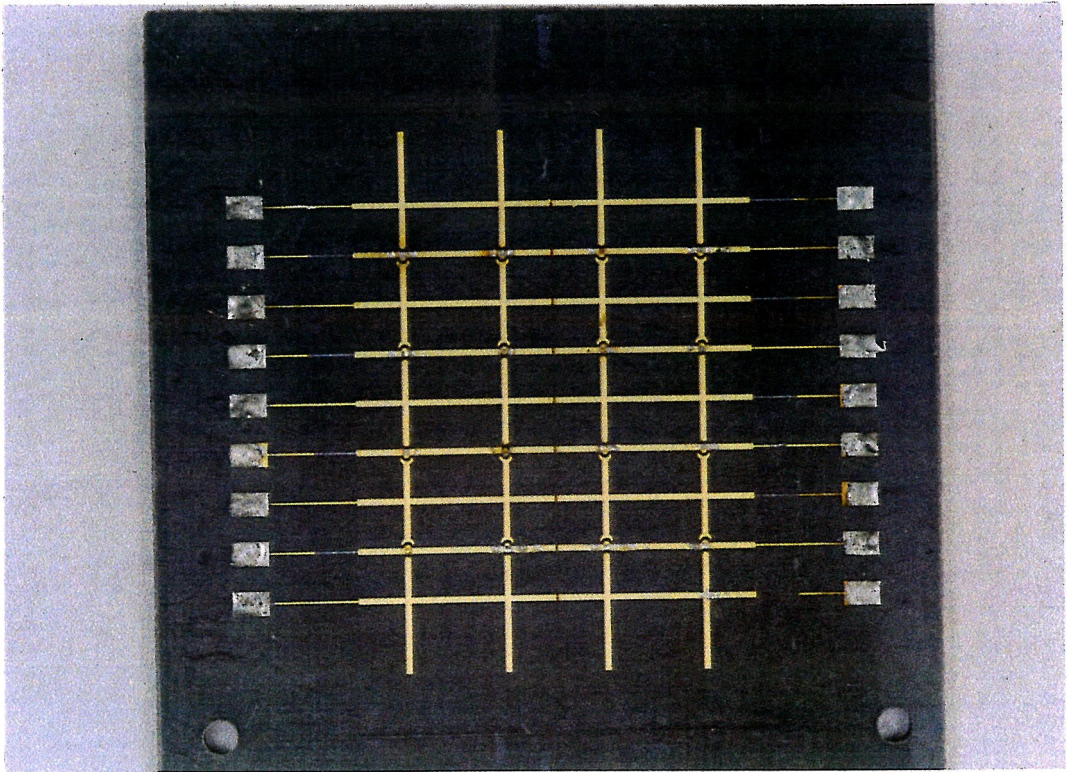


Figure 5.3 Photograph of Power Grid 1. The grid has 16 elements and developed 1.48 W total radiated power with a dc-to-rf efficiency of 21%.

	dc V_{ds} (V)	dc I_{ds} (mA)	Frequency (GHz)	Directivity (dB)	ERP (W)	Power (W)	P/device (mW)	Eff. %
Theory (V)	7.15	—	9.94	11.5	22.3	1.59	99.7	22.8
Theory (I)	—	75/48 [†]	9.94	11.5	10.4	0.74	46.3	10.6
Measured	7.15	75/48 [†]	9.2	12.7	27.6	1.48	92.5	21

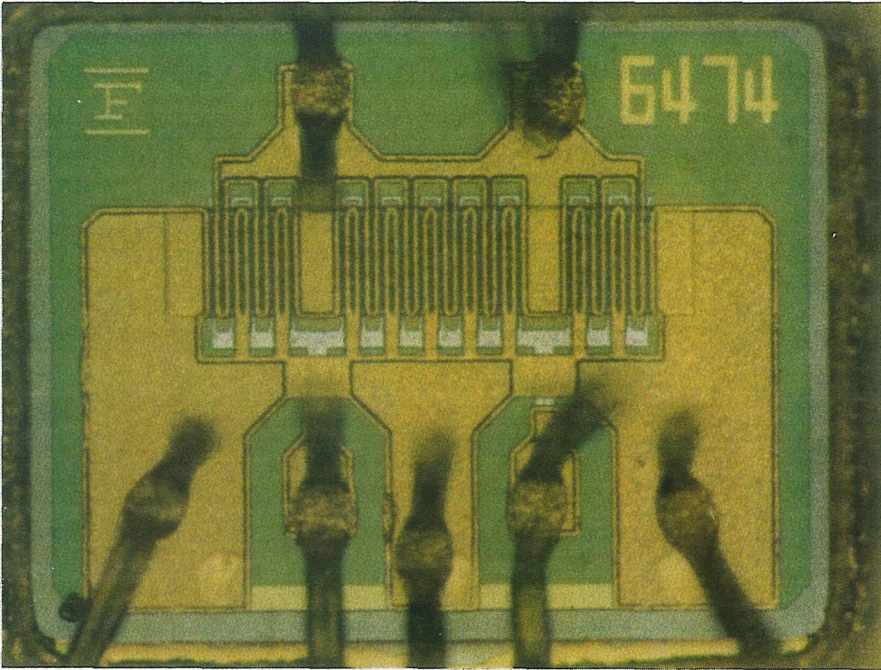
Table 5.1 Comparison of theoretical and experimental data for Power Grid 1.

[†] (edge-row bias current/middle-row bias current)—see text.

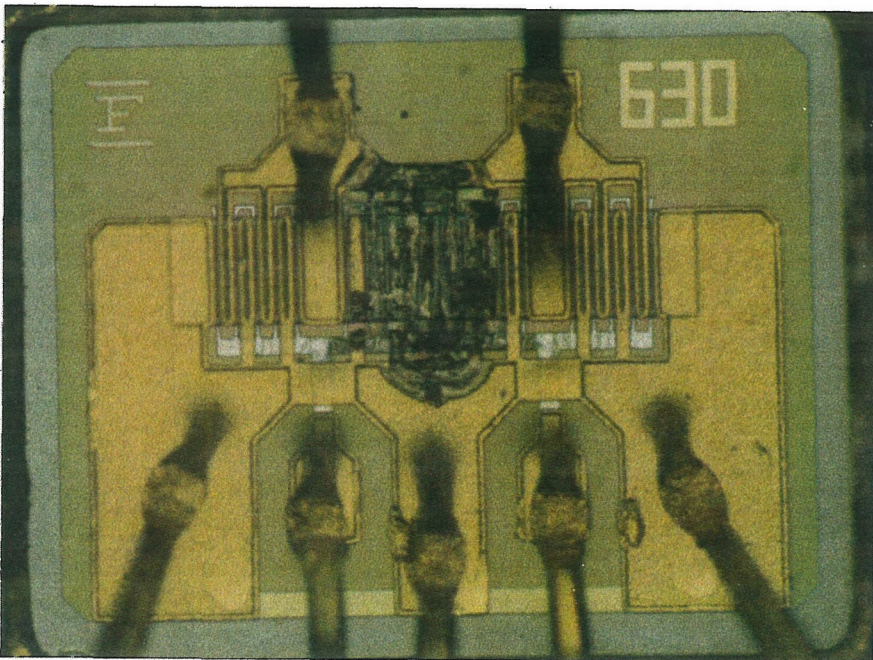
the device model is for a bias of 10 V at 120 mA, the 3.0-dB error between theory and experiment seems reasonable.

Attempts to run the grid at bias voltages greater than 7.15 V resulted in device failure. The failure mode was a short-circuit, which resulted in the entire grid shutting down as all the devices are biased in parallel. Figure 5.4 shows a close-up of MESFET bonded to grid, and also a failed device after biasing above 7.15 V. Three possible causes of the failures are excessive channel temperature due to overheating, too much power being fed back into the gate, or an impedance mismatch in the output circuit. A thermal analysis of the grid shows that with a 7.5 V drain-source bias, the worst-case (i.e., 0% dc-to-rf efficiency) channel temperature should be no more than 140° C. This would suggest that the problem is more likely related to excessive loop gain causing too much power to be fed back to the gate of the device or to excessive voltages across the transistor terminals related to standing waves created by an impedance mismatch in the output circuit.

The measured frequency of 9.2 GHz is 7.5% lower than the predicted value of 9.94 GHz. Previous grid oscillators have shown better agreement between theory and experiment. Weikle predicted frequencies within 1% for two grid oscillators measured [4]. An examination of the FLK052XP transistor source metallization



(a)



(b)

Figure 5.4 (a) Photograph of a Fujitsu FLK052XP MESFET in the unit cell of Power Grid 1. (b) Photograph of a failed device after the drain-source dc bias voltage was increased above 7.15 V.

suggests one possible reason for the observed frequency shift. The source metal pattern covers approximately 30% of the chip surface, and the chip die, to reduce thermal resistance, is only 60- μm thick. This results in an additional parasitic capacitance between the source metal and the gold plate on the back of the chip. Assuming negligible fringing fields, the estimated capacitance is 120 fF. Normally the source is grounded so this capacitance would be shorted out. However, in the grid application, the transistor is mounted on the gate lead, and this extra capacitance will show up as additional gate-source capacitance. With this additional capacitance added to the circuit, the revised predicted frequency is lowered to 9.90 GHz, but is still 7.0% higher than the measured value.

5.2 POWER GRID TWO

The second power grid oscillator design attempted to correct for the frequency shift observed in Power Grid 1. The EMF method used to compute the equivalent circuit for the grid does not take into account the complicated metal structure near the transistor used to facilitate wire bonding the device to the grid (Figure 5.1(a)). It was surmised that the metal structure here could add extra capacitance to the center lead capacitor, C_m of the equivalent circuit. Consequently, an extra capacitance was introduced in parallel with C_m to account for this effect. The value of additional capacitance needed to bring the theoretical oscillation frequency in line with the measured frequency was 80 fF. With this extra capacitance added to the model, the grid unit cell dimensions were re-adjusted to present the optimum load impedance to the transistor at an oscillation frequency of 10 GHz.

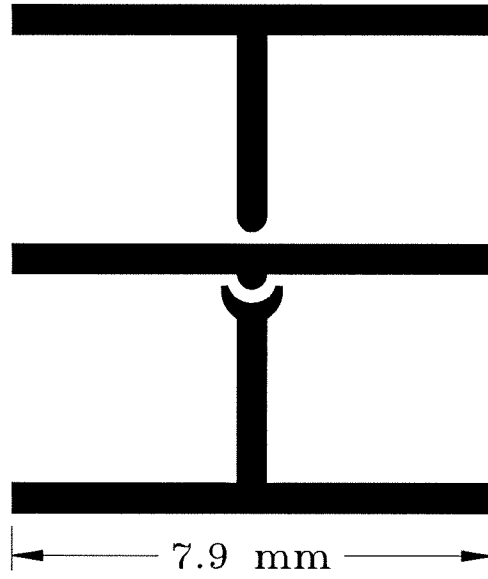
Figure 5.5 shows the unit cell dimensions of the grid and the corresponding equivalent circuit used to predict the grid oscillation frequency and transistor load impedance. The only change required from Power Grid 1 was the use of a smaller unit cell 7.9-mm square. A thinner *Duroid* 5880 substrate 1.59-mm thick was also used, but this just affected the position of the mirror behind the

grid. Figure 5.6 shows the theoretical feedback loop gain based on the equivalent circuit of Figure 5.5. The predicted oscillation frequency is 9.80 GHz, and the unoptimized loop gain at this frequency is 3.1 (9.8 dB).

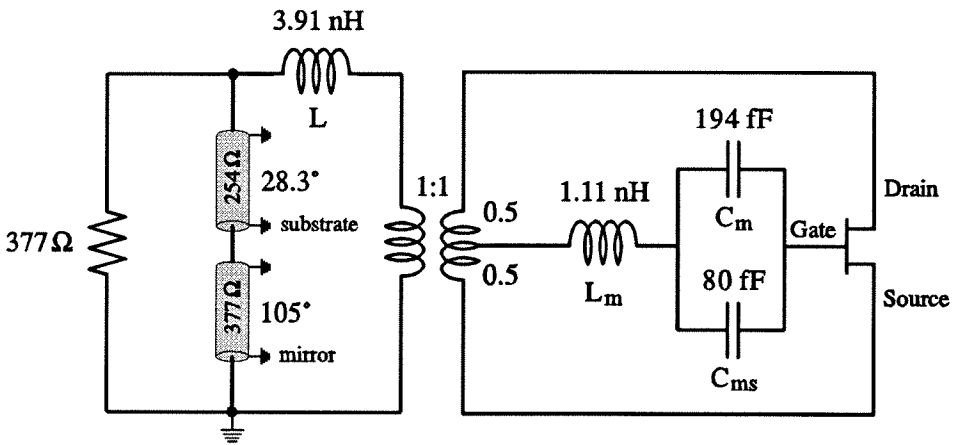
Figure 5.7 shows a photograph of the transistor bonded into the unit cell of the grid. The measured oscillation frequency of 10.1 GHz is 3.1% higher than the predicted value of 9.80 GHz. This is closer than the 7.5% difference between theory and experiment for Power Grid 1 and is probably as good as can be expected given the large signals of the transistor and the simple linear model used to obtain the theoretical frequency.

The measured total radiated power for the grid was 0.89 W, which corresponds to 55.5 mW per device. This is 2.2 dB lower than Power Grid 1. The grid drain-source bias voltage was 6.50 V and the total drain current for the grid was 1160 mA resulting in an overall dc-to-rf efficiency of 12%. This efficiency is lower than the 21% recorded for Power Grid 1.

Table 5.2 summarizes the measured and theoretical parameters of interest for the grid. The theoretical power delivered to the load was computed assuming a peak voltage of 6.50 V (4.60 V_{rms}) across the current source which gives a corresponding load power of 0.59 W (36.6 mW per device). This is 1.8 dB lower than the measured value of 0.89 W (55.5 mW per device). Predicting the power for the dc bias drain current is more complicated as the two middle rows were biased at 58 mA per device and the two edge rows at 88 mA per device. Using the higher current of 88 mA predicts a load power of 75.1 mW per device, and using 58 mA per device predicts 32.4 mW. Adding the two predicts a total power for the grid of 0.86 W, a value within 0.2 dB of the measured power. Figure 5.8(a) shows a plot of measured power for the grid versus drain-source bias voltage. Also shown is the theoretical power computed using the actual bias voltage and bias current of each measured point. The bias current prediction is seen to be a better estimate of measured power than the bias voltage, which consistently underestimates the



(a)



(b)

Figure 5.5 (a) Unit cell metal pattern for Power Grid 2. (b) Equivalent circuit model used to predict the theoretical performance of the grid. An extra capacitance C_{ms} was added to compensate for the observed frequency shift in Power Grid 1.

	dc V_{ds} (V)	dc I_{ds} (mA)	Frequency (GHz)	Directivity (dB)	ERP (W)	Power (W)	P/device (mW)	Eff. %
Theory (V)	6.50	—	9.80	11.6	8.5	0.59	36.6	7.8
Theory (I)	—	88/58 [†]	9.80	11.6	12.4	0.86	53.8	11.4
Measured	6.50	88/58 [†]	10.1	13.3	19.0	0.89	55.5	11.8

Table 5.2 Comparison of theoretical and experimental data for Power Grid 2.

[†] (edge-row bias current/middle-row bias current)—see text.

measured power for this grid. Figure 5.8(b) shows the corresponding efficiency as a function of dc bias voltage. Again, the efficiency calculated using the bias current is in better agreement with the measured results. Attempts to run the grid at bias voltages greater than 6.5 V resulted in device failure similar to that experienced with Power Grid 1.

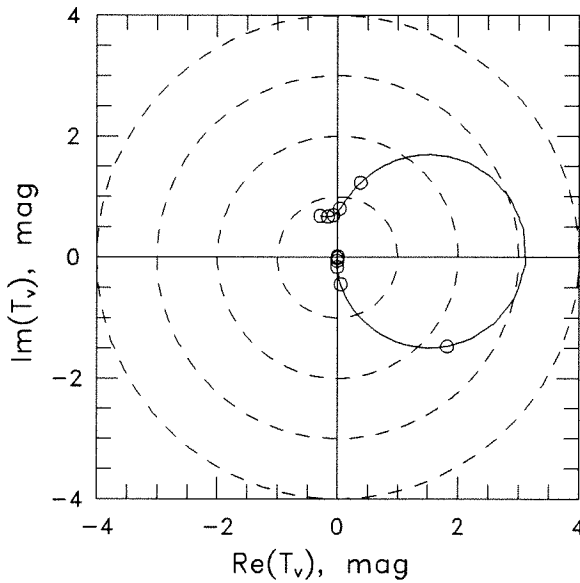


Figure 5.6 Theoretical loop gain of Power Grid 2 from 5 to 15 GHz. The predicted oscillation frequency is 9.80 GHz and the loop gain is 9.8 dB. 100 MHz intervals are marked with a (o).

Figure 5.9(a) shows the two-dimensional radiation pattern measured by placing the grid on a gimbal mount in an anechoic chamber. The measured pattern was integrated to find the directivity of the grid oscillator, which was then used to determine the total radiated power (TRP) from the measured effective radiated power (ERP). The measured directivity was 13.3 dB which compares favorably with the estimated directivity of 11.6 dB computed by assuming the effective area of the grid is equal to the sum of the physical area of the grid unit cells. Figure 5.9(b) shows the measured and theoretical E-plane radiation pattern for Power Grid 2. The theoretical plot was calculated for a uniform array of short dipoles on a dielectric slab with a mirror behind the grid [5].

In order to verify whether the optimum load impedance was being presented

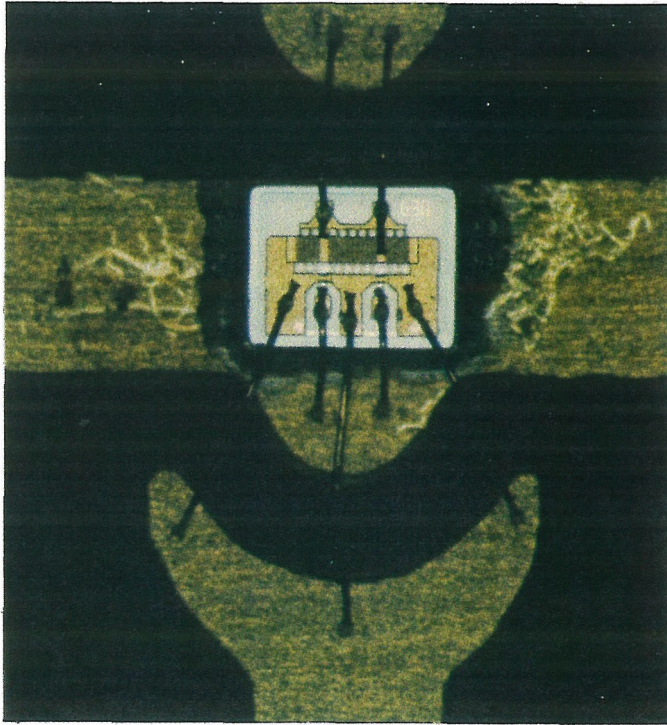


Figure 5.7 Photograph of transistor bonded into the unit cell of Power Grid 2. The grid has 16 elements and developed 0.89 W total radiated power at 10.1 GHz with a dc-to-rf efficiency of 12%.

to the transistor for maximum oscillator power, a load-pull test was performed. The test setup consisted of two dielectric slabs placed in front of the grid and mounted on optical translation stages. The identical slabs had electrical lengths of 98.8° at 10 GHz and a relative dielectric constant of 10.5. The slabs behave like coaxial slug tuners, and by varying the slab-grid and slab-slab separation, the impedance presented to the grid can be varied to cover almost the entire Smith chart if the mirror distance behind the grid is adjusted to present an open circuit to the back of the grid. An automated test setup was built to measure the power and frequency of the grid as the slab positions were varied. Figure 5.10 shows the measured load-pull contour for the grid plotted on a Smith chart normalized to free space ($377\ \Omega$). The peak power is seen to occur at the center of the Smith chart where the impedance of free space ($377\ \Omega$) is presented to the grid. This

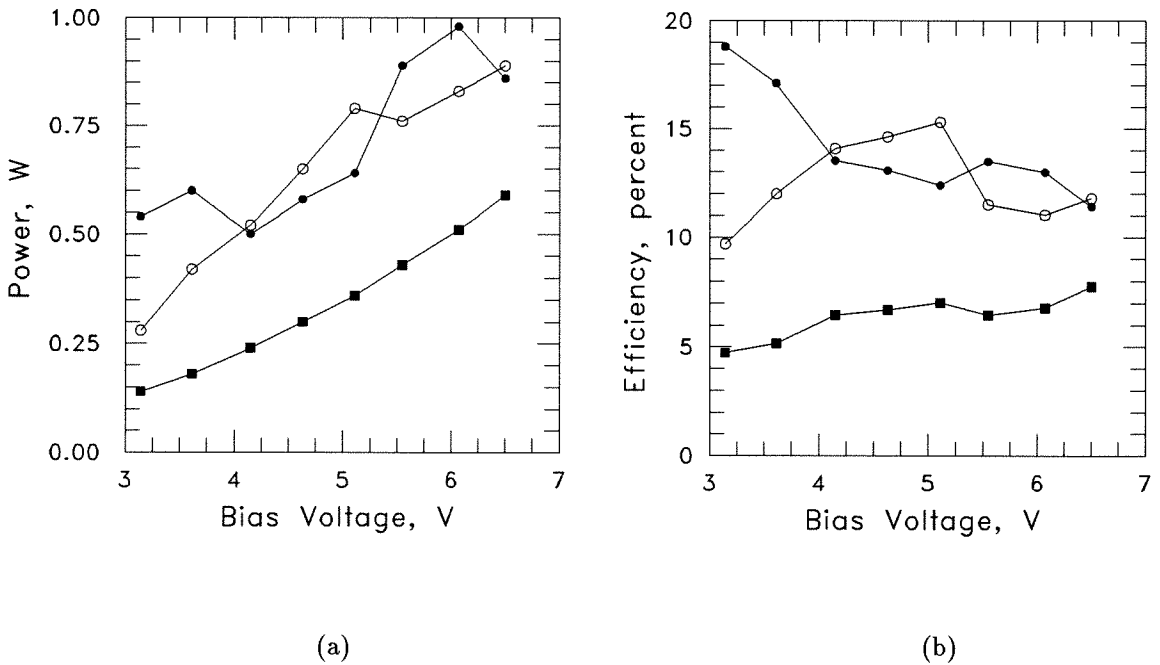
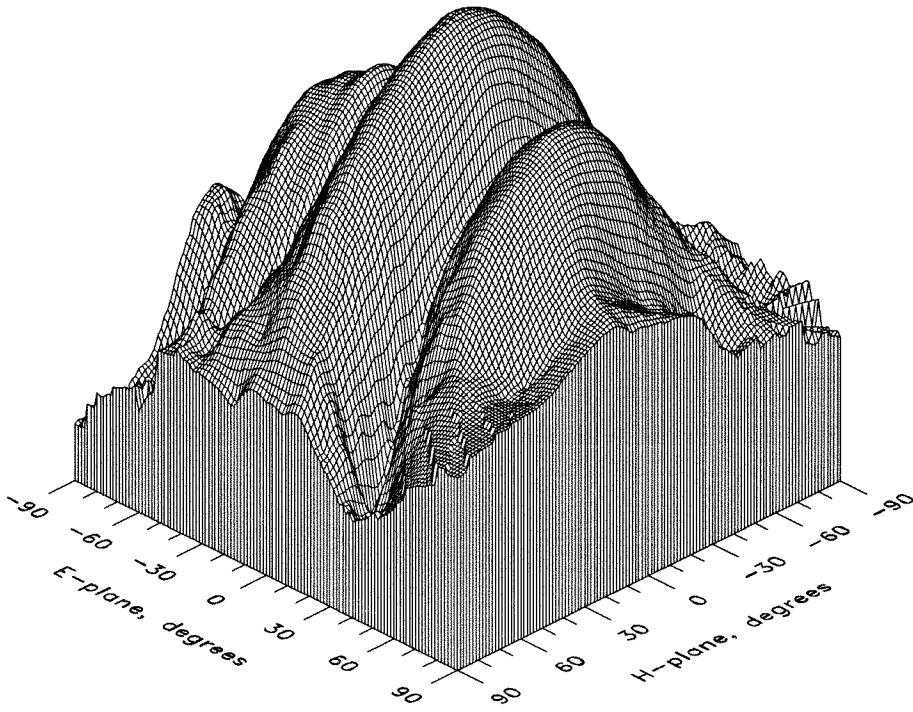
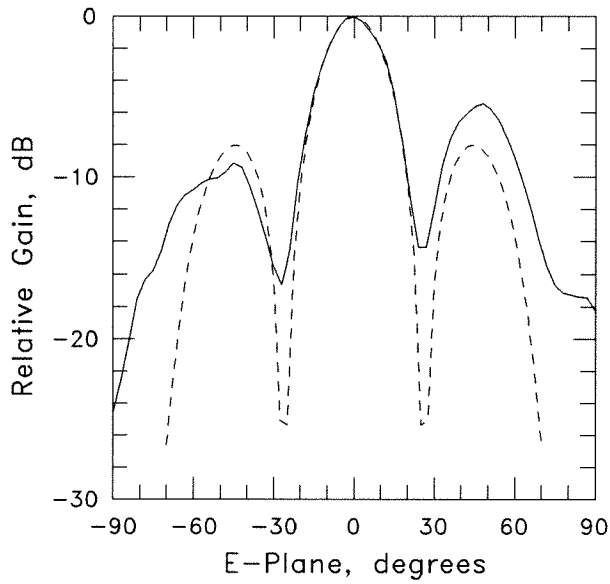


Figure 5.8 (a) Total radiated power versus dc bias voltage. Measured power (o) is bracketed by the theoretical power calculated based on dc drain current (•) and dc bias voltage (■). (b) Corresponding efficiencies for the power plotted in (a).



(a)



(b)

Figure 5.9 (a) The measured radiation pattern of Power Grid 2. The axes are given in terms of spherical coordinates, $\theta_E = \theta \sin \phi$ and $\theta_H = \theta \cos \phi$. The vertical scale is logarithmic in power. (b) Experimental pattern (solid line) and theoretical pattern (dashed line) for a mirror distance of 14.7 mm.

was also the impedance used when designing the grid for optimum transistor load impedance. Thus, we can conclude that the grid unit cell is presenting the optimum load impedance to the transistor when the grid is coupled to free space and the design model is sufficiently accurate.

5.3 POWER GRID THREE

Both Power Grid 1 and 2 produced less than the theoretical maximum power per device of 330 mW calculated for the Fujitsu FLK052XP in Section 4.4. In addition, both grids could not be run at the manufacturer's recommended bias of 10 V at 120 mA. Power Grid 1 failed for bias voltages above 7.7 V and Power Grid

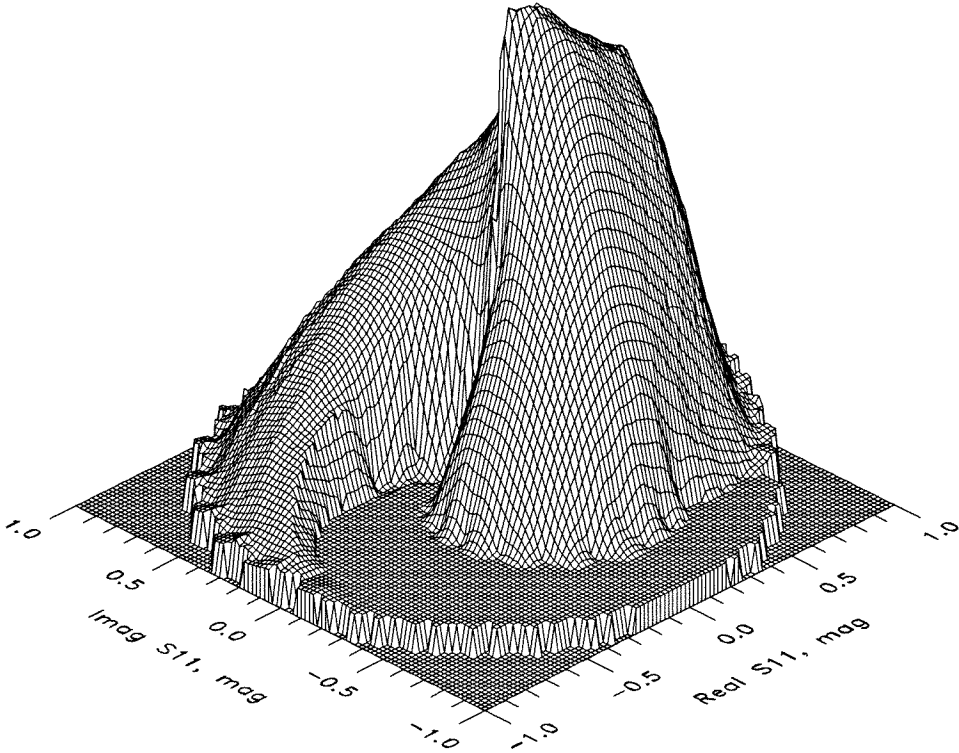
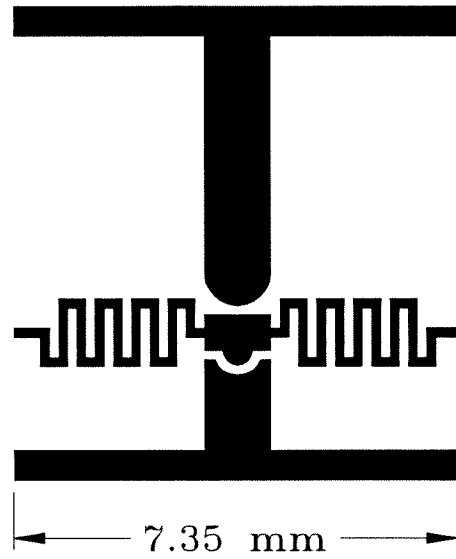


Figure 5.10 Load-pull contour measured for Power Grid 2. The vertical scale is linear in power. The contour is plotted on a Smith chart normalized to $377\ \Omega$. The peak power occurs for a load impedance very near $377\ \Omega$, confirming that the grid is presenting the optimum load impedance to the transistor as designed.

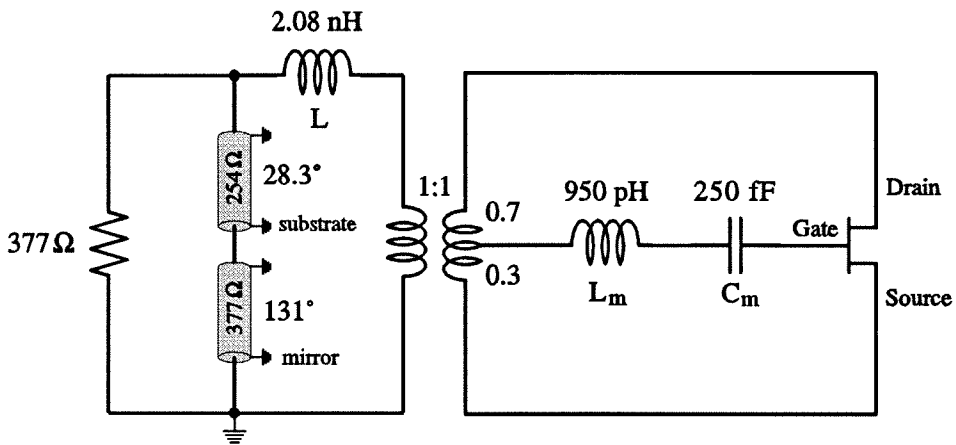
2 failed for voltages greater than 6.5 V. The load-pull tests seem to confirm that the correct load impedance was being presented to the transistors. A thermal analysis indicates that the worst-case transistor channel temperatures are below 150° C at these low bias voltages, which suggests that the failures are caused by too much power being fed back into the input port of the transistor. Referring to the calculated loop gains for the two previous designs, we see that Power Grid 1 has 8.3 dB of loop gain and Power Grid 2 has 9.8 dB of loop gain, both significantly higher than the optimum value of 4 dB computed in Section 4.4. Moreover, the higher loop gain of Power Grid 2 explains why it had lower output power compared to the less saturated design of Power Grid 1.

In order to reduce the loop gain, a new grid was designed that used a meandered horizontal lead as described in Section 4.4. Figure 5.11 shows the unit cell dimensions of the grid, and the corresponding equivalent circuit used to predict the grid oscillation frequency and transistor load impedance. In order to get the desired transistor load impedance, the transistor was offset in its unit cell. The unit cell is 7.35-mm square. The vertical lead is 1.10-mm wide and the meandered lead is 1.125-mm wide with a line width of 0.15 mm. The offset ratio for the unit cell is 0.30. The *Duroid* 5880 substrate was again 1.59-mm thick. The component values for the grid equivalent circuit were obtained from an HP structure simulator analysis of the unit cell equivalent waveguide as outlined in Section 4.4. Figure 5.12 shows the theoretical feedback loop gain based on the equivalent circuit of Figure 5.11. The predicted oscillation frequency is 10.68 GHz and the unoptimized loop gain at this frequency is 1.8 (5.3 dB). This is 3-dB lower than Power Grid 1 and 4.5-dB lower than Power Grid 2, and within 1.3 dB of the theoretical optimum of 4 dB.

Figure 5.13 shows a photograph of the fabricated 16-element grid. The measured oscillation frequency of 11.4 GHz is 6.7% higher than the predicted value of 10.68 GHz. The measured total radiated power for the grid was 0.92 W, which



(a)



(b)

Figure 5.11 (a) Unit cell metal pattern for Power Grid 3. (b) Equivalent circuit model used to predict the theoretical performance of the grid. Values were computed using the HP structure simulator.

corresponds to 57.5 mW per device. This is 2.1-dB lower than Power Grid 1. The grid drain-source bias voltage was 5.50 V and the total drain current for the grid was 1120 mA resulting in an overall dc-to-rf efficiency of 15%. This efficiency is lower than the 21% recorded for Power Grid 1. The theoretical power for a bias voltage of 5.50 V is 117 mW per device, and for a bias current of 70 mA, is 121 mW per device, 3.1 dB and 3.2 dB respectively higher than measured. Table 5.3 summarizes the measured and predicted parameters of the grid.

Severe overheating was observed for bias voltages above 5.5 V. The overheating was so extreme that the solder was observed to melt on some of the devices. For this reason the power capability of the grid was never realized, and the power was limited to 0.92 W at a very low 5.5 V dc bias. The cause of the overheating is due to mounting the transistor on the meandered horizontal lead. This 0.15-mm wide lead is 70% narrower than the horizontal lead of the previous grids which

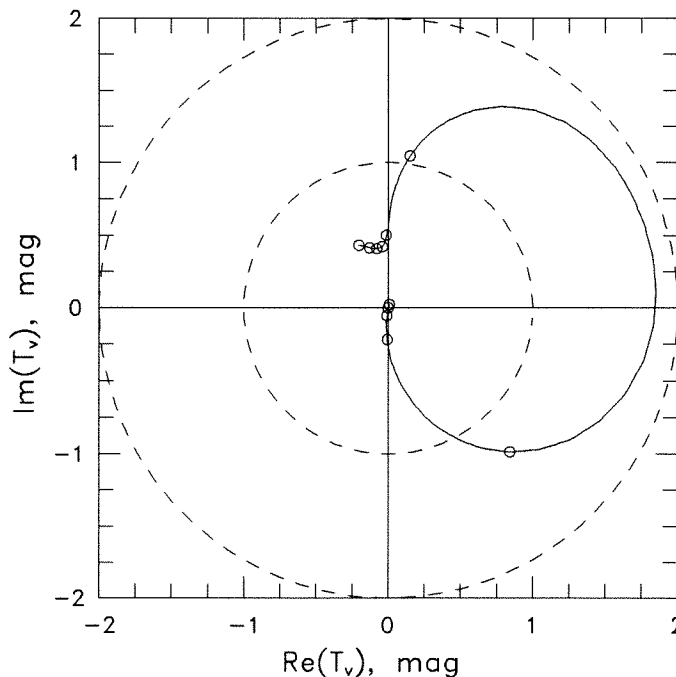


Figure 5.12 Theoretical loop gain of Power Grid 3 from 5 to 15 GHz. The predicted oscillation frequency is 10.68 GHz and the loop gain is 5.3 dB. 100 MHz intervals are marked with a (o).

	dc V_{ds} (V)	dc I_{ds} (mA)	Frequency (GHz)	Directivity (dB)	ERP (W)	Power (W)	P/device (mW)	Eff. %
Theory (V)	5.50	—	10.68	12.0	29.6	1.87	117	30.4
Theory (I)	—	70	10.68	12.0	30.6	1.93	121	31.4
Measured	5.50	70	11.4	10.0	9.2	0.92	57.5	15.0

Table 5.3 Comparison of theoretical and experimental data for Power Grid 3.

severely decreases its ability to carry heat away from the device and dissipate it by convection to the surrounding air.

Additionally, the radiation pattern of Power Grid 3 was a monopulse pattern

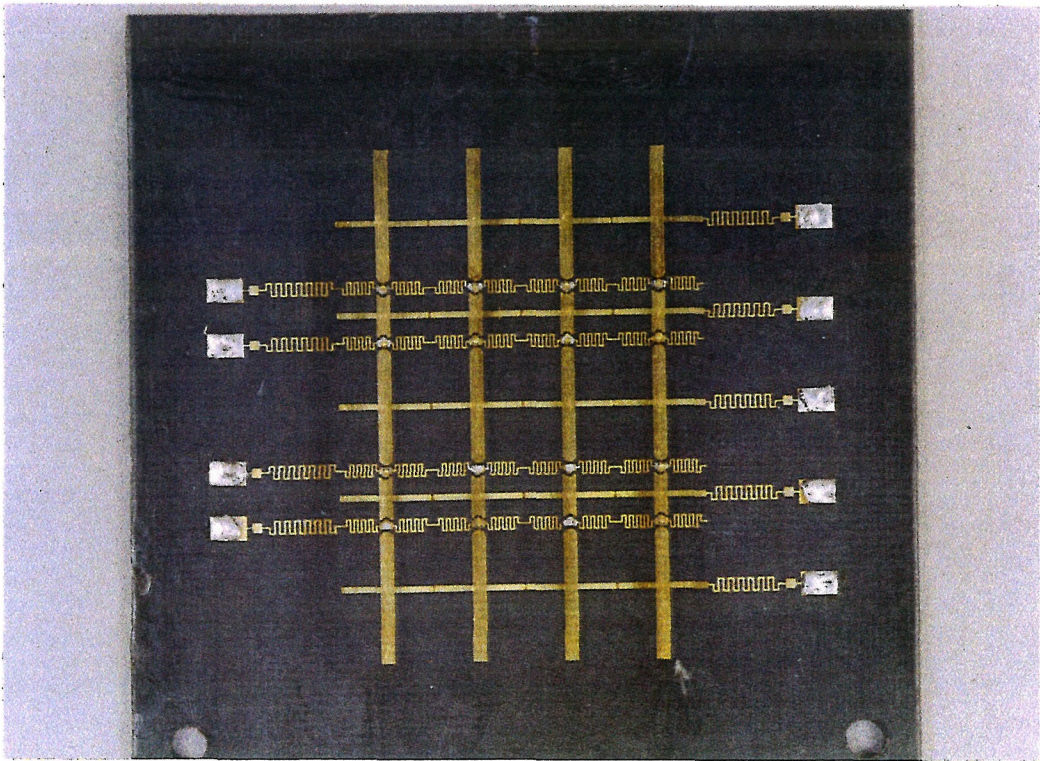


Figure 5.13 Photograph of Power Grid 3. The grid has 16 elements and developed 0.92 W total radiated power at 11.4 GHz with a dc-to-rf efficiency of 15%.

as shown in Figure 5.14. The measured gain of the grid was 10.0 dB at 18° off the boresight. The theoretical gain is 12.0 dB. This peculiar pattern was attributed to mounting the transistor offset in the grid unit cell. This meant that adjacent rows of transistors were alternately 4.41 mm and 10.3 mm apart. At the frequency of oscillation, a dielectric half-wavelength is 8.8 mm, a value that lies between the two separation lengths. We surmise that the top and bottom two rows, which are close together, were locking together in phase, but the two top rows were locked out of phase with the two bottom rows, which are separated by a distance greater than a dielectric half-wavelength, producing a monopulse response.

5.4 POWER GRID FOUR

The fourth power grid oscillator design was a compromise based on the

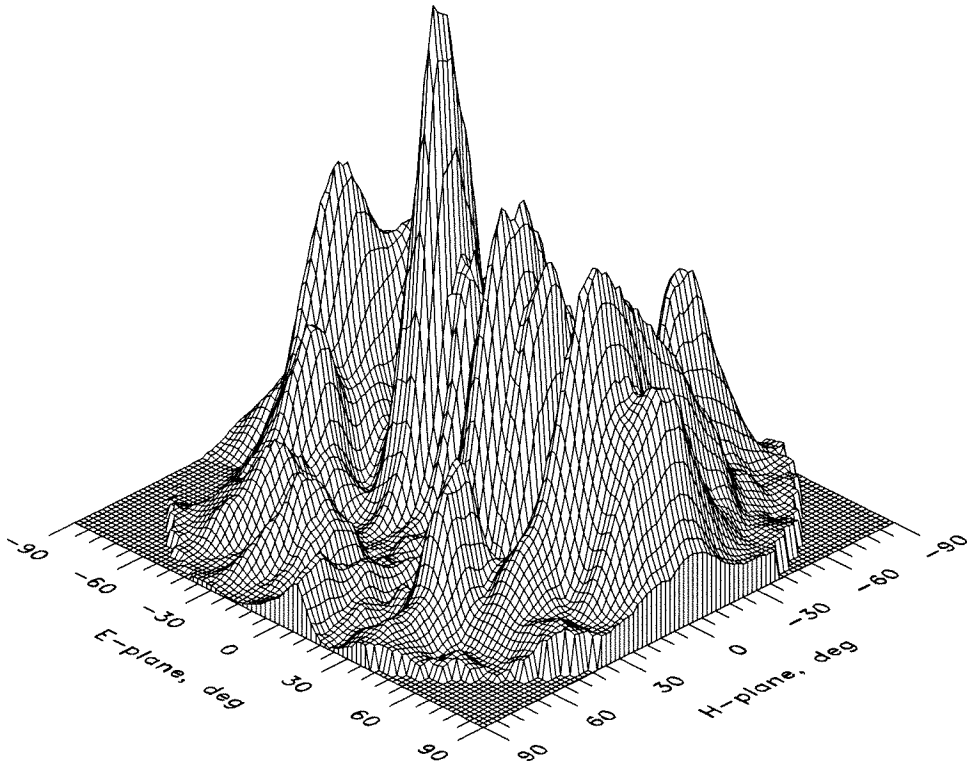


Figure 5.14 The measured radiation pattern of Power Grid 3. The vertical scale is linear in power. The pattern is a monopulse response, with the peak gain of 10.0 dB occurring 18° off the boresight.

results of Power Grid 3. The offset unit cell design was discarded to eliminate the poor radiation pattern observed with Power Grid 3. The transistor was mounted on the drain lead to improve transistor cooling. The meandered center lead was retained, but the requirement that there be no offset in the unit cell meant that the load impedance presented to the transistor had significant reactance associated with it. At a predicted oscillation frequency of 10.0 GHz, the load presented to the transistor is $85+j30\ \Omega$ and the loop gain is 1.54 (3.7 dB). This was not seen as a problem, though, as simulations with two slabs in front of the grid, as was done for the load-pull measurements, showed that this reactance can be tuned out. Figure 5.15 shows the locus of transistor load impedance as the separation between slabs and grid is varied from 12–27 mm.

Figure 5.16 shows the unit cell dimensions of the grid, and the corresponding equivalent circuit used to predict the grid oscillation frequency and transistor

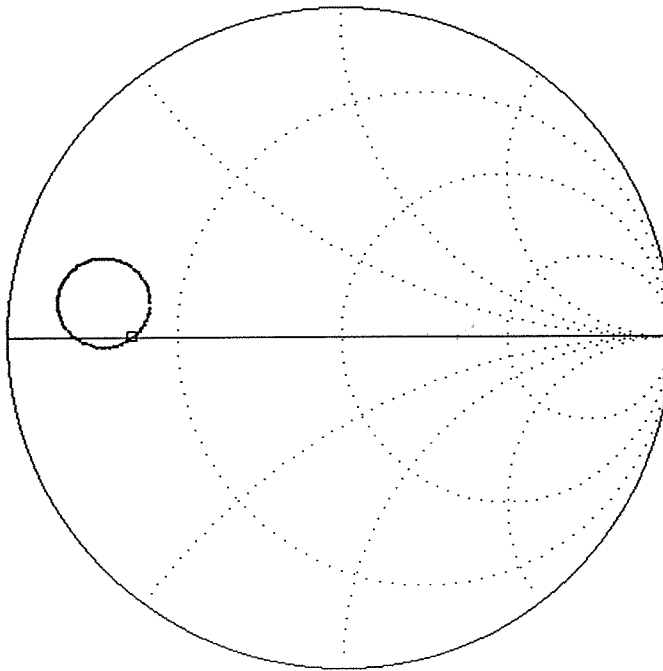


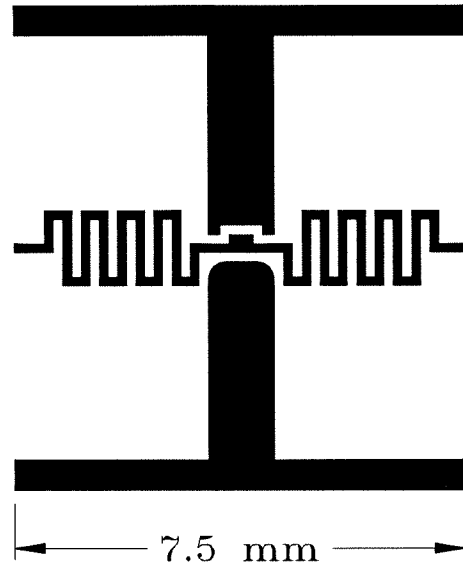
Figure 5.15 Locus of transistor load impedance as the separation between slabs and the grid is varied from 12–27 mm. The separation between slabs is a constant 14.4 mm. The optimum load impedance, shown by the marker, occurs for a grid-slab separation of 13.2 mm.

load impedance. The unit cell is 7.50-mm square. The vertical lead is 1.10-mm wide and the meandered lead is 1.25-mm wide with a line width of 0.15-mm. The component values for the grid equivalent circuit were obtained from an HP structure simulator analysis of the unit cell equivalent waveguide. Figure 5.17 shows the theoretical feedback loop gain based on the equivalent circuit for the grid.

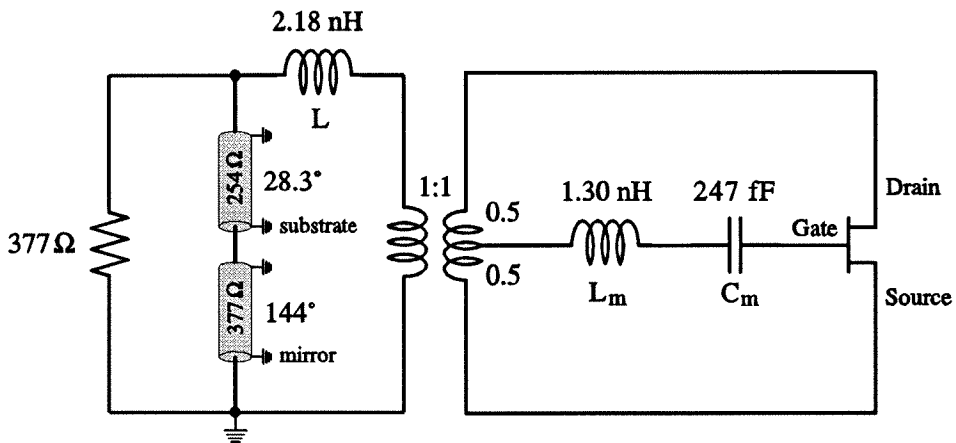
Two grids were built based on this design, a 16-element grid and a 100-element grid. Figure 5.18 shows a photograph of the complete grid and a close-up of the transistor for the 100-element grid. The measured oscillation frequency of the 16-element grid was 9.35 GHz, and the 100-element grid oscillated at 9.8 GHz. This is within 6.5% and 2% respectively of the predicted frequency of 10.0 GHz. One source of frequency error is in the etched width of the metal lines of the grid. The etch accuracy in our lab is approximately 0.05 mm which is 33% of the designed 0.15 mm width of the meander lines. Variation in meander line width of this order was observed in the fabricated grids and would help explain the observed frequency shift between the two grids.

The measured effective radiated power for the 100-element grid was 657 W. This corresponds to a total radiated power of 10.3 W, or 103 mW per device. The measured power per device is 0.5 dB better than Power Grid 1, and 10.3 W is the highest reported total radiated power for a grid oscillator. The grid drain-source bias voltage was 7.40 V, and the total drain current for the grid was 6.02 A, resulting in an overall dc-to-rf efficiency of 23%. This efficiency is slightly better than the 21% recorded for Power Grid 1.

Table 5.4 summarizes the measured and theoretical parameters of interest for the grid. The theoretical power delivered to the load was computed assuming a peak voltage of 7.40 V (5.23 V_{rms}) across the current source which gives a corresponding load power of 20.5 W (205 mW per device). This is 3.0 dB higher than the measured value of 10.3 W (103 mW per device). Predicting the power



(a)



(b)

Figure 5.16 (a) Unit cell metal pattern for Power Grid 4. (b) Equivalent circuit model used to predict the theoretical performance of the grid. Values were computed using the HP structure simulator.

for the dc bias drain current is more complicated as the eight middle rows were biased at 70 mA per device and the two edge rows at 21 mA per device. Using the higher current of 70 mA predicts a load power of 150 mW per device, and using 21 mA per device predicts 13.5 mW. Adding the two predicts a total power for the grid of 12.2 W, a value within 0.7 dB of the measured power. A non-linear simulation of the grid using the EEsof Libra harmonic balance software gave a predicted power of 146 mW per device at a frequency of 10.2 GHz for a 7.5 V bias, a power within 1.5 dB of the measured value of 103 mW per device.

Two conditions prevented higher powers from being observed for this grid. First, the transistors appeared to have degraded during the time the grid radiation pattern was measured. It is very difficult to reliably cool the grid when mounted in the anechoic chamber. Although the grid was biased at a reduced voltage for these measurements, power measurements made before the grid was

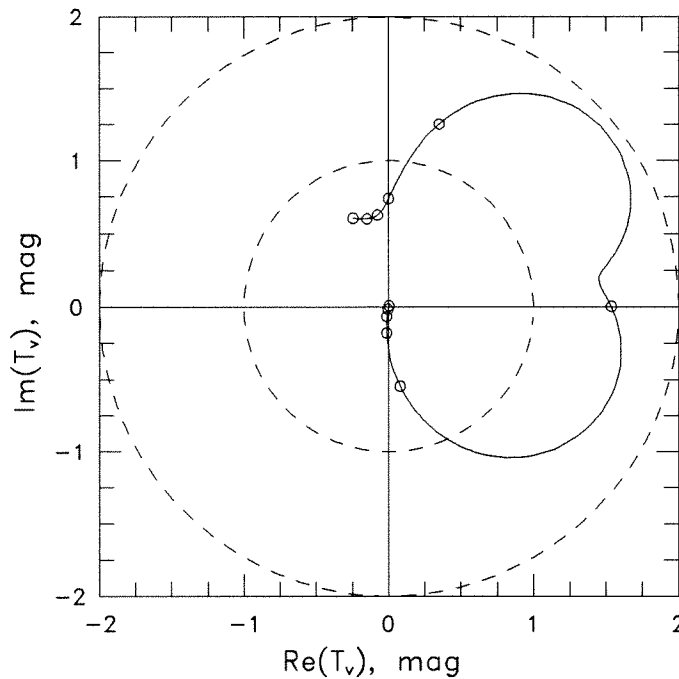
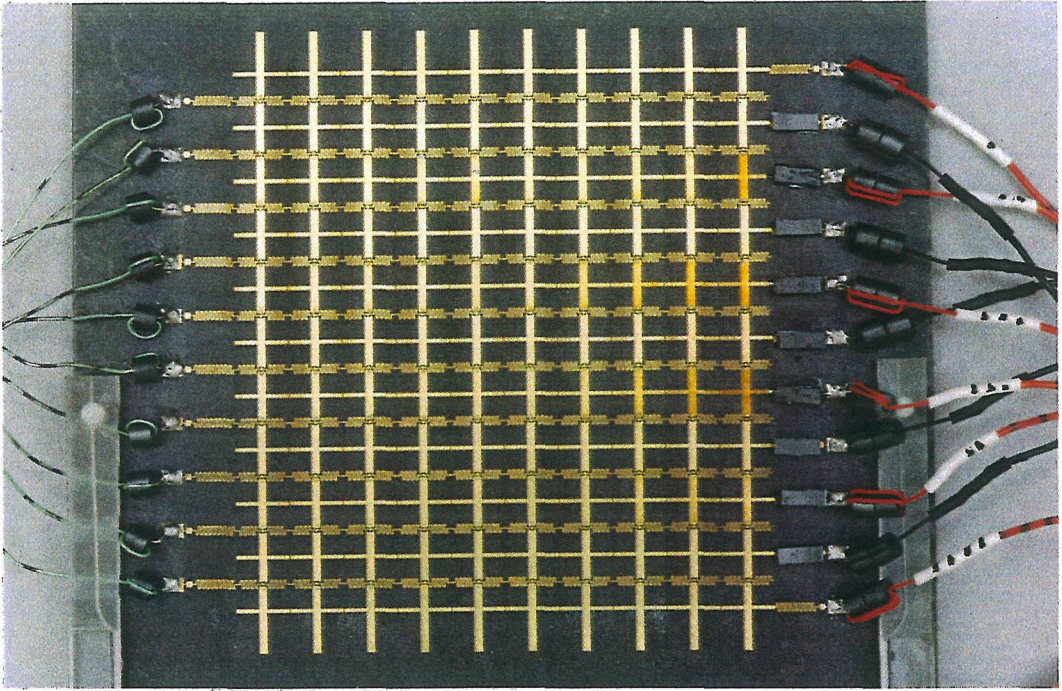
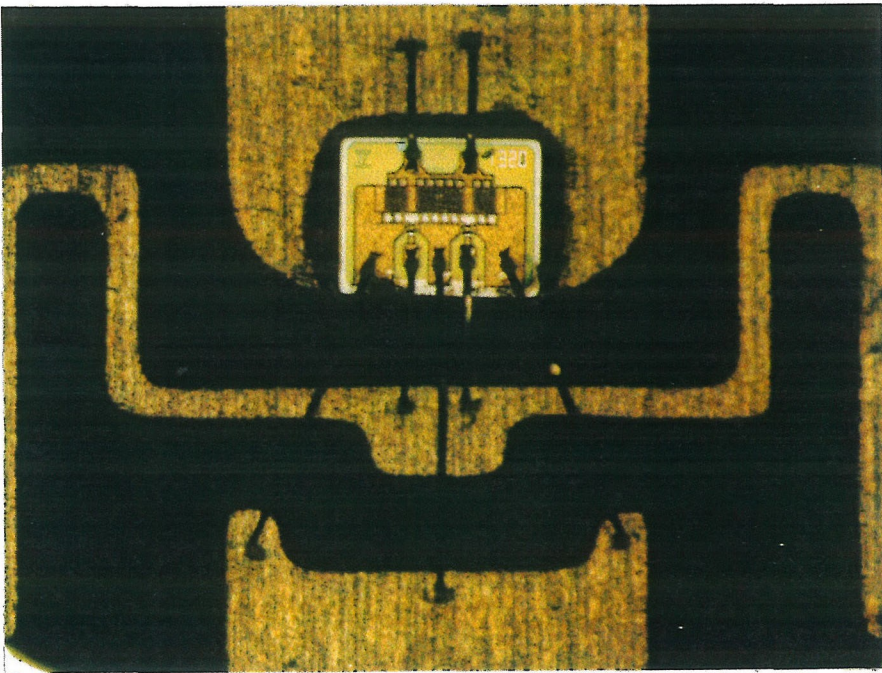


Figure 5.17 Theoretical loop gain of Power Grid 4 from 5 to 15 GHz. The predicted oscillation frequency is 10.0 GHz and the loop gain is 3.7 dB. 100 MHz intervals are marked with a (o).



(a)



(b)

Figure 5.18 (a) Photograph of the 100 element version of Power Grid 4. The 100-element grid produced 10.3 W with a dc-to-rf efficiency of 23%. (b) Photograph of the Fujitsu FLK052XP mounted in the grid unit cell.

placed in the anechoic chamber could not be repeated afterwards. Secondly, when the grid was biased above 7.4 V, the center row devices on the vertical edge where the drain and source dc bias lines were attached failed. Very high rf currents were present on these transistors as the bond wires fused on several of the devices. High currents were also observed on the edge terminations for the drain bias feeds for the center rows. Five 0.7 mil bond wires connected in parallel with a measured dc current handling of over 6 A repeatedly fused at these edge terminations. Since the dc bias for the leads was current limited to 2.0 A, this suggested the presence of very high rf currents on these structures. One possible source of these currents is bias line oscillations. Bias line oscillations are polarized horizontally and can be eliminated in some cases by changing the edge termination impedances. Various edge terminations were investigated, but the problem persisted at high bias voltages preventing operation of the grid above 7.4 V.

Figure 5.19 shows the measured two-dimensional radiation pattern of the 100-element grid. The measured directivity was 18.0 dB which compares favorably with the estimated directivity of 18.8 dB computed by assuming the effective area of the grid is equal to the sum of the physical area of the unit cells. Figure 5.20 shows the measured and theoretical E-plane (a) and H-plane (b) radiation patterns for the 100-element grid, and the measured and theoretical

	dc V_{ds} (V)	dc I_{ds} (mA)	Frequency (GHz)	Directivity (dB)	ERP (W)	Power (W)	P/device (mW)	Eff. %
Theory (V)	7.40	—	10.0	18.8	1540	20.5	205	46.0
Theory (I)	—	21/70 [†]	10.0	18.8	915	12.2	122	27.5
Measured	7.40	21/70 [†]	9.8	18.0	657	10.3	103	23.1

Table 5.4 Comparison of theoretical and experimental data for the 100 element version of Power Grid 4.

[†] (edge-row bias current/middle-row bias current)—see text.

E-plane (c) and H-plane (d) radiation patterns for the 16-element grid. To account for the quarter-wave stub edge terminations added to the top and bottom rows of the grids, two additional elements were assumed for the E-plane array factor computations, ie. 6 elements for the 4×4 grid and 12 elements for the 10×10 grid. These extra elements were not added for the H-plane array factor simulations. As expected, the larger 100-element grid has a narrower beamwidth. The measured directivity of the 16-element grid was 12.6 dB, 5.4 dB less than the 100-element grid.

A load-pull measurement was performed on the 100-element grid in order to verify whether the optimum load impedance was being presented to the transistor for maximum oscillator power. Figure 5.21 shows the measured load-pull contour for the grid plotted on a Smith chart normalized to free space (377Ω). The peak

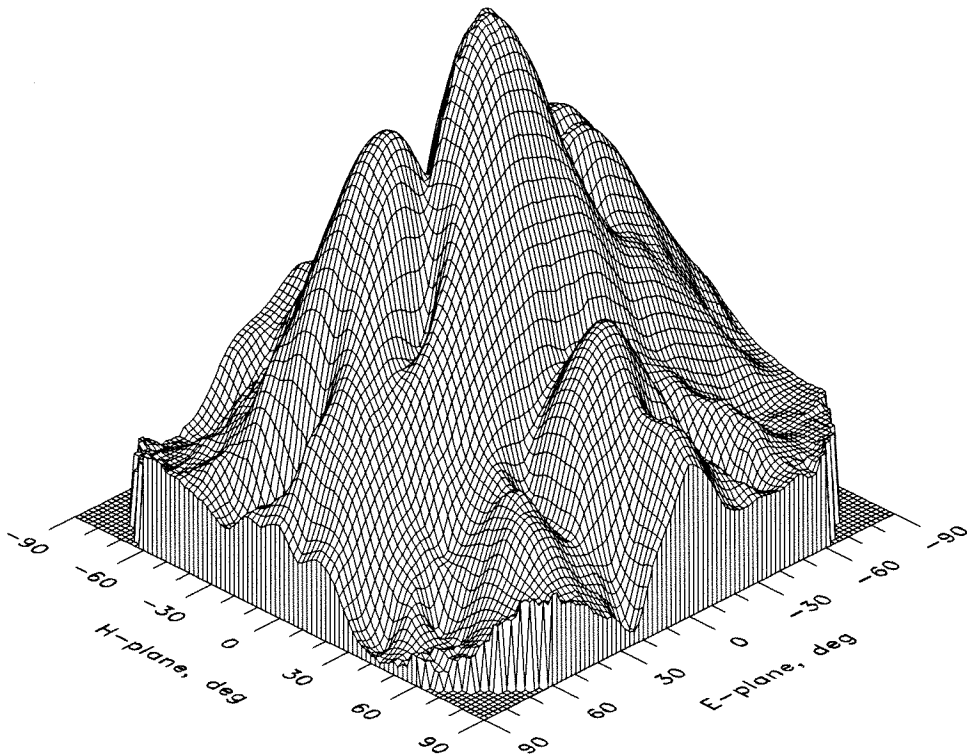


Figure 5.19 The measured radiation pattern of the 100-element grid version of Power Grid 4. The vertical scale is logarithmic in power. The measured directivity was 18.0 dB.

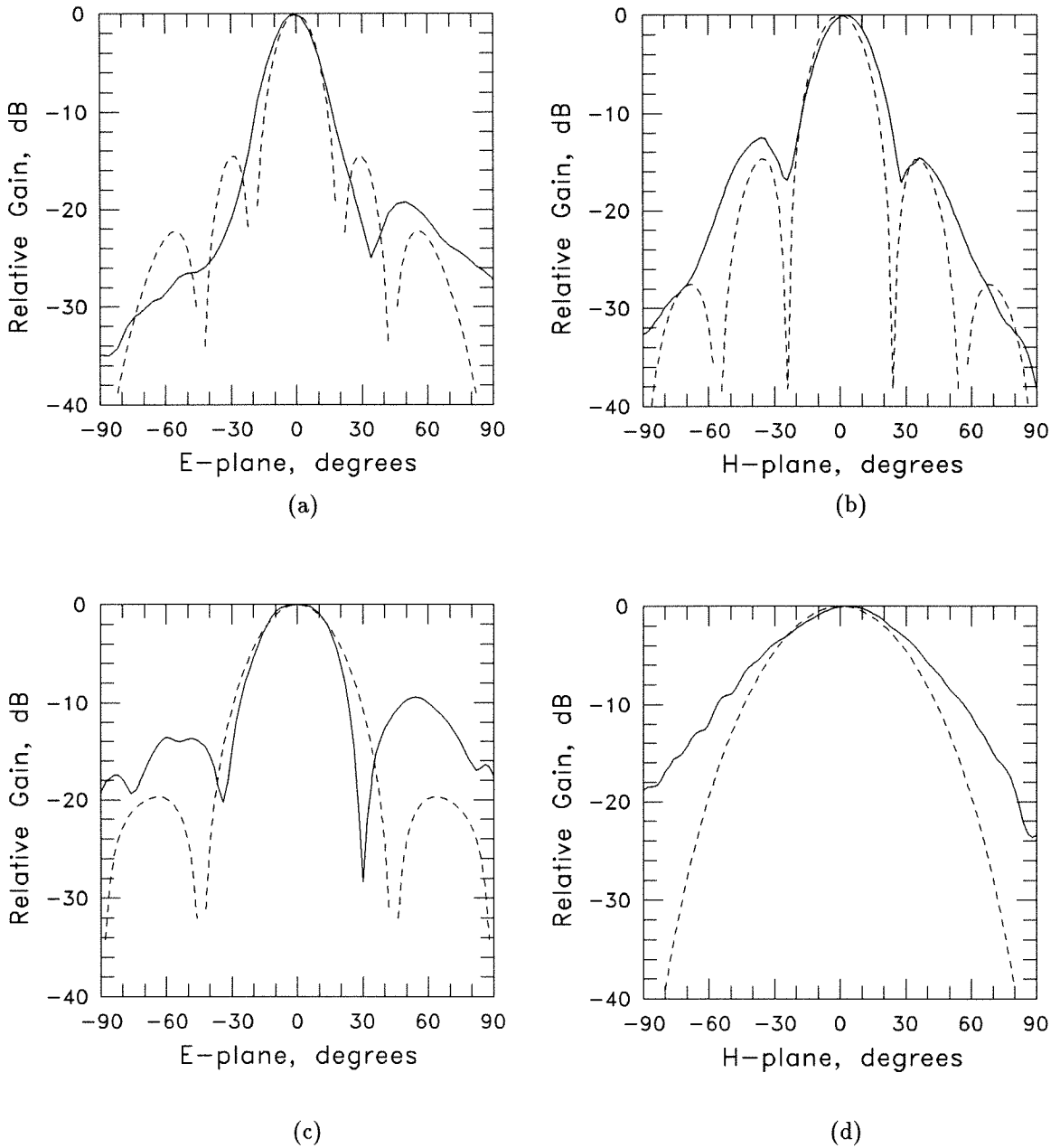


Figure 5.20 Measured E-plane and H-plane patterns (solid lines) and theoretical patterns (dashed lines) for (a, b) the 100 element grid with 0.4-mm mirror spacing, and (c, d) the 16-element grid with 0.4-mm spacing. Two extra elements were added for the E-plane array factor computations in the theoretical plots, i.e. 6 elements for the 4×4 grid and 12 elements for the 10×10 grid, to account for the quarter-wave stub edge terminations added to the top and bottom rows of the grid.

power occurs for a load impedance of $490 + j660 \Omega$. This is in agreement with the model. The requirement that Power Grid 4 not use an offset unit cell meant that the optimum load impedance for the transistor could not be obtained with a free-space impedance presented to the face of the grid.

The single-sideband noise pattern of the two grids was measured. We suspect that the primary source of noise in the oscillator is channel noise in each transistor. We would expect the drain noise in each transistor to be uncorrelated, and hence the noise pattern should be the same regardless of the number of elements in the grid. The signal power, however, is correlated, and so it will increase in proportion to the number of devices in the grid. Consequently, the improvement in SSB noise should also be proportional to the number of grid

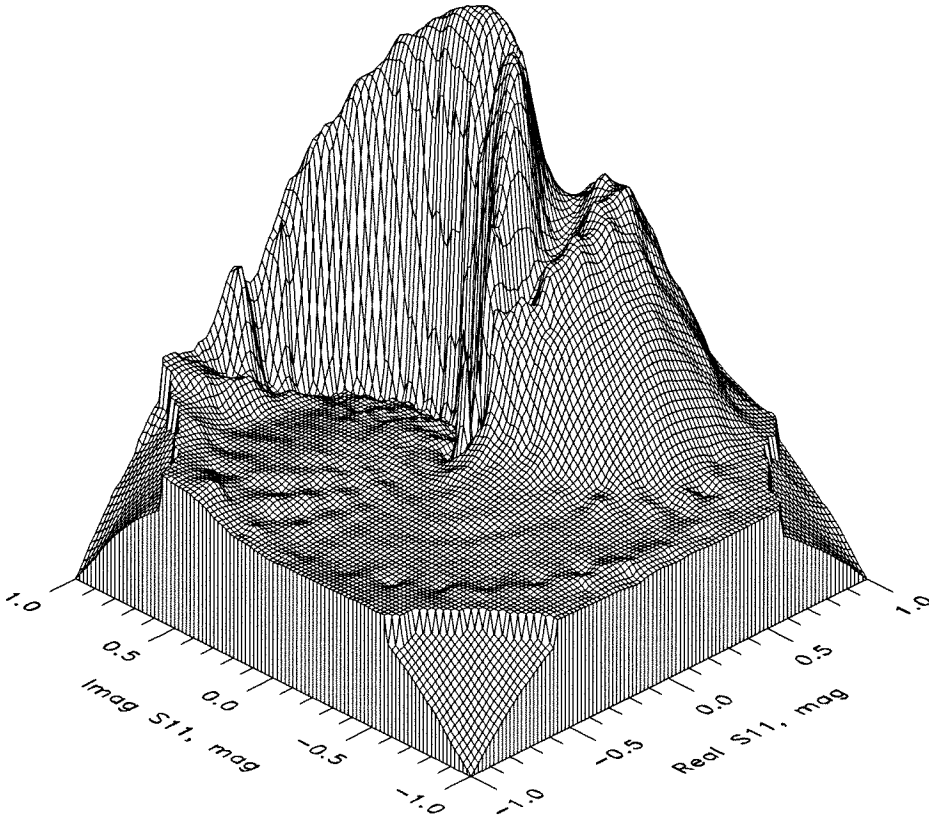


Figure 5.21 Load-pull contour measured for the 100-element grid. The vertical scale is linear in power. The contour is plotted on a Smith chart normalized to 377Ω . The peak power occurs for a load impedance of $490 + j660 \Omega$.

elements. For a 100-element grid, we expect to see an improvement of 100/16 (8.0 dB) over an equivalent 16-element grid.

Figure 5.22 shows the SSB noise spectrum near the carrier for the 100-element grid. Figure 5.23 shows the measured SSB noise pattern in the E and H planes for the two grids. The noise was measured at a 150 kHz offset from the carrier using a spectrum analyzer with a resolution bandwidth of 30 kHz. The H-plane pattern was essentially flat for both grids. The mean measured improvement in H-plane SSB noise of the 100-element grid compared to the 16-element grid was 4.9 dB. For the E-plane, the mean measured improvement for the SSB noise was 5.9 dB. The E-plane pattern has two nulls that correspond to the nulls in the measured E-plane radiation patterns. The nulls are not visible in

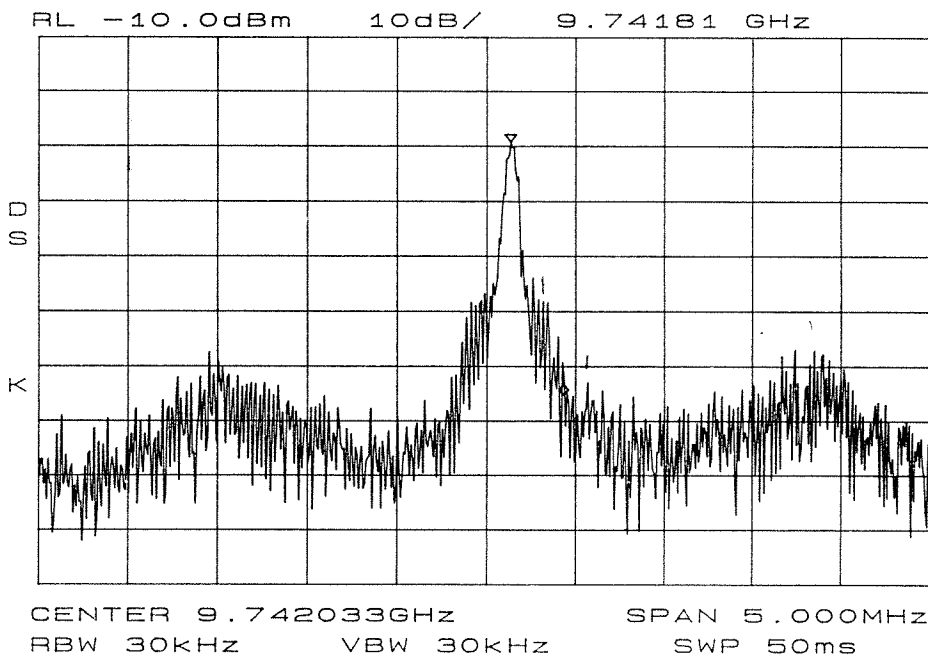
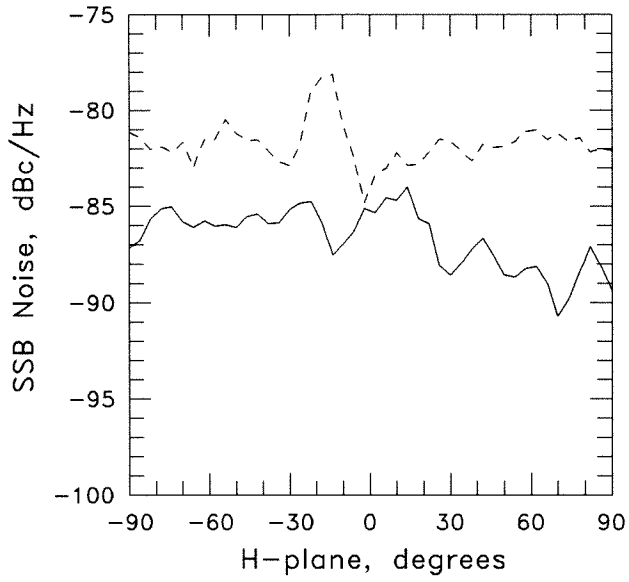
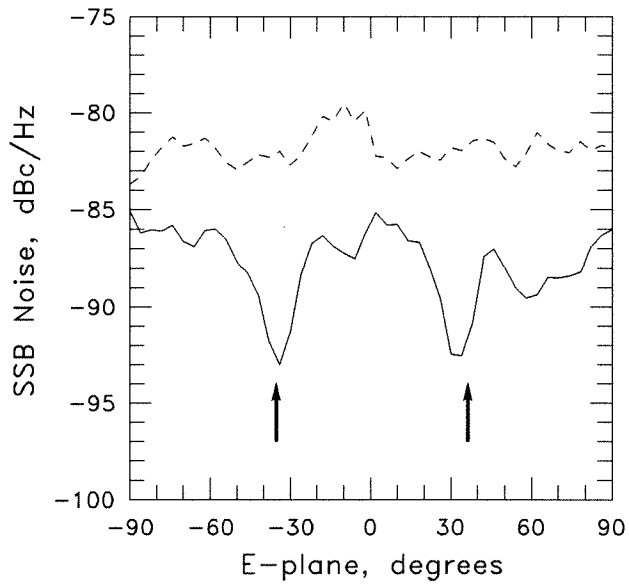


Figure 5.22 SSB noise spectrum for the 100-element grid. The bumps at 1.75 MHz offset from the carrier are typical of injection-locked oscillators.



(a)



(b)

Figure 5.23 Measured SSB noise at 150 kHz offset from the carrier for the 100-element grid (solid line) and the 16-element grid (dashed line) in (a) the H-plane and (b) the E-plane. The two arrows indicate the position of the nulls in the E-plane radiation pattern measured for the 100-element grid.

the H-plane. We suspect that substrate modes are being excited that propagate to the grid edge and radiate from there to contribute to filling in the nulls in the H-plane. We can explain this qualitatively by examining the behaviour of substrate modes excited by a dipole on a substrate [5]. Since our substrate is thin relative to a wavelength, the TM_0 substrate mode will have relatively less power than the dominant TE_0 . Consequently, there will be little observable effect in the E-plane. However, in the H-plane, the strong TE_0 mode will propagate to the grid edge and radiate. Since the distance from each cell to the grid edge varies, we would expect a broad unstructured pattern from this substrate mode radiation that would tend to fill in the nulls.

The output of the grid was fed to a detector to determine if the SSB noise was predominantly phase-noise or amplitude noise. No discernible noise power was observed from the detected signal for frequencies up to 40 MHz. The NEP of the AM detector was -125 dBm, which is 25 dB below the typical SSB noise measured from the grid. Based on these measurements we can conclude that the SSB noise of the grid near the carrier is predominantly due to phase noise.

5.5 SUMMARY

A high-power X-band 100-element grid oscillator has been demonstrated. The grid embedding circuit was designed to provide the optimum load impedance and feedback loop gain to the transistor for maximum power. The measured effective radiated power was 657 W and the directivity was 18.0 dB. This corresponds to a total radiated power of 10.3 W, or 103 mW per device. The grid drain-source bias voltage was 7.40 V and the total drain current for the grid was 6.02 A, resulting in an overall dc-to-rf efficiency of 23%. The SSB noise pattern was measured and found to be independent of the number of cells in the grid. An average improvement in SSB noise of 4.9 dB for the H-plane and 5.9 dB for the E-plane was measured for a 100-element grid compared to a 16-element grid.

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Chapter 6

Discussion and Suggestions for Future Work

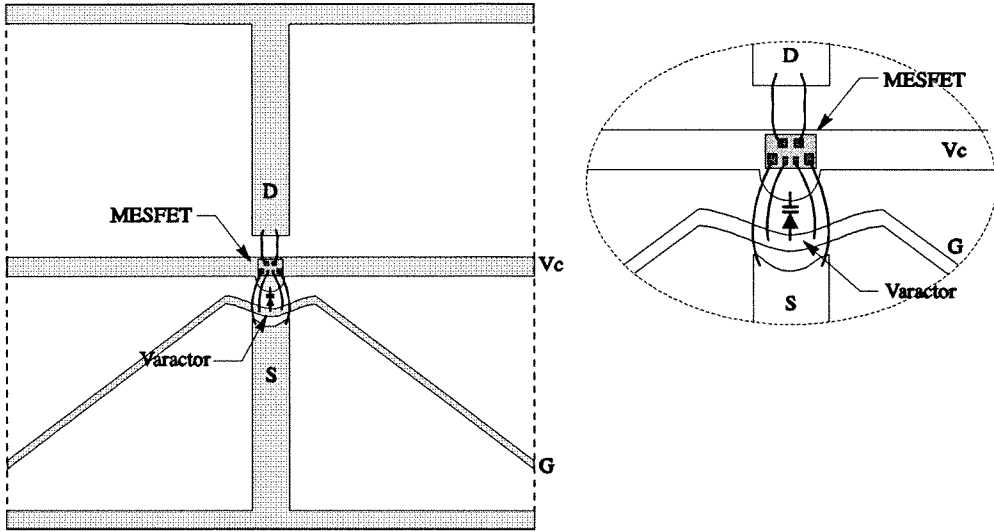
This thesis discusses the use of quasi-optical grids loaded with active devices for use as mixers, sideband generators, and power oscillators. The grid mixer power handling and dynamic range were demonstrated to scale as the number of devices in the grid, an important characteristic for receivers where power handling of the nonlinear element is often a limitation. A sideband generator grid was shown to be an efficient package for increasing the theoretical operating frequency and power output of monolithic planar diodes at terahertz frequencies. Techniques for designing power grid oscillators to produce Watt-level output powers have been described. Finally, methods that make use of electromagnetic solvers such as Hewlett-Packard's *High-Frequency Structure Simulator* have been developed to model grid structures of arbitrary shape with good results.

Unfortunately, the power grid oscillators presented in this thesis were not able to fully exploit the output power capability of the transistors. The observed device failures at high bias voltages seem to be related to the build up destructively high localized rf currents on the grid. It is likely that improved grid edge terminations can be developed to suppress these modes. Further work is necessary in this area. Of even greater importance is the design of oscillator grids on high-dielectric substrates. Terahertz grid applications demand monolithic construction methods, and in turn this will force grids to be fabricated on high-dielectric substrates, as will the use of high-thermal conductivity substrates such as aluminum nitride. Results to date have been poor for grids fabricated

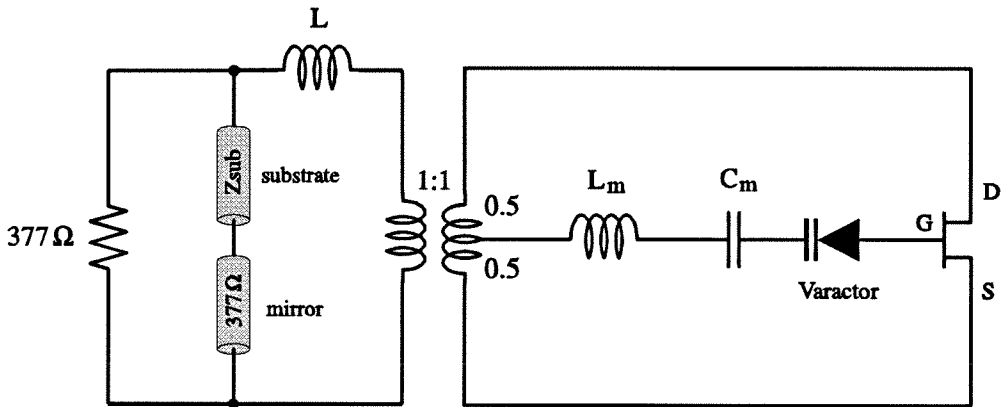
on substrates with dielectric constants greater than 2.2. The cause of these failures needs to be better understood. Hybrid microwave grids fabricated on aluminum nitride substrates offer an attractive approach to learning more about high-dielectric constant grid design and cooling by thermal conduction.

Although grid oscillators have been demonstrated with large output powers, their phase noise and frequency accuracy remain poor in comparison with commercial oscillators. One possible approach to overcome these shortcomings is to use a phase lock loop (PLL) circuit to lock the output of the grid oscillator to a lower frequency reference signal. Such circuits require that the oscillator frequency be controllable, typically by the use of varactor diodes in the oscillator feedback loop. A unit cell design for a voltage-controlled oscillator grid (VCOG) is shown in Figure 6.1. Varactor diodes are added to the unit cell to allow the oscillation frequency to be varied. Figure 6.2 shows a plot of oscillator frequency versus varactor capacitance for a grid based on the unit cell of Power Grid 1 and a varactor whose rf capacitance can be varied from 0.1 pF to 10 pF. The ability to accurately control the grid oscillator frequency and to substantially improve phase noise is critical if grid oscillators are to be used in commercial applications.

There has recently been much interest in extending the concept of quasi-optical power combining to amplifiers. Grid amplifiers at C and X-band have been successfully built by Kim [1]–[3]. Demonstration of a high-power grid amplifier is the next logical step. It would be convenient to use commercially available power transistors to build a microwave-frequency grid amplifier with Watt-level output powers as was done with the grid oscillator. Unfortunately, the grid amplifiers fabricated so far have used low-power differential-pair transistors. Obtaining equivalent high-power devices is likely to be difficult. Figure 6.3 shows a proposed grid amplifier that uses two commercial medium-power PNP bipolar transistors (NEC NE90100 or better) connected to a slightly modified version of the custom differential-pair HBT transistors used by Kim [2]. The result is a



(a)



(b)

Figure 6.1 (a) Proposed unit cell for a voltage-controlled grid oscillator. (b) Equivalent circuit model used to predict the theoretical oscillation frequency of the voltage controlled grid oscillator.

differential pair of Sziklai connected transistors. This interesting configuration should be capable of output powers up to 29 dBm per device at L Band [4].

There is a lot of interesting work yet to be done at this early stage in the development of quasi-optical planar grid circuits. Substantial progress on understanding the capabilities and applications of these circuits has been made, but there is still much to be learned.

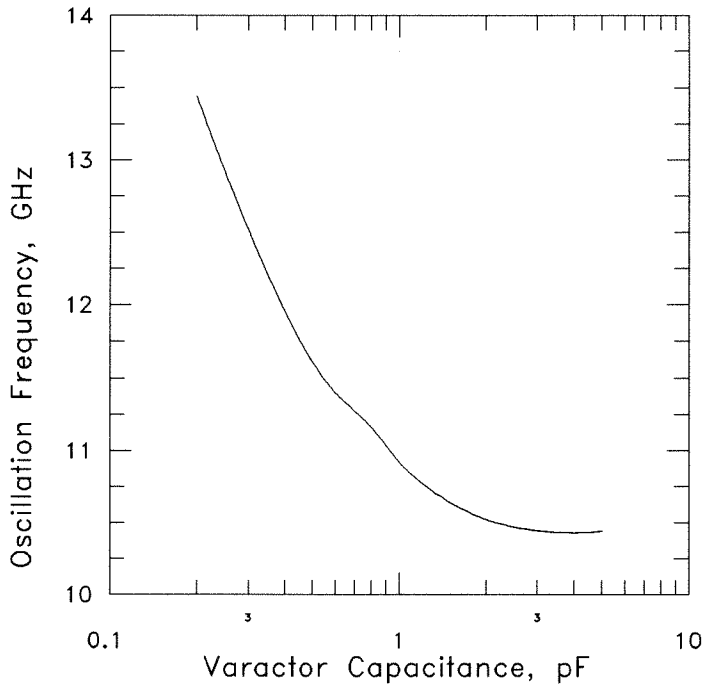
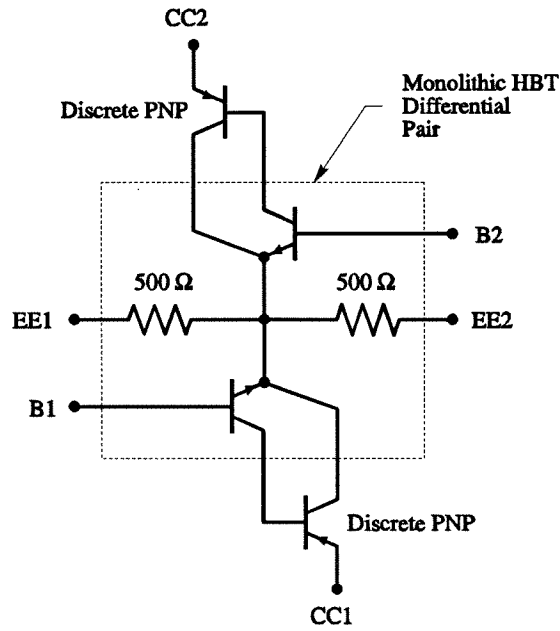
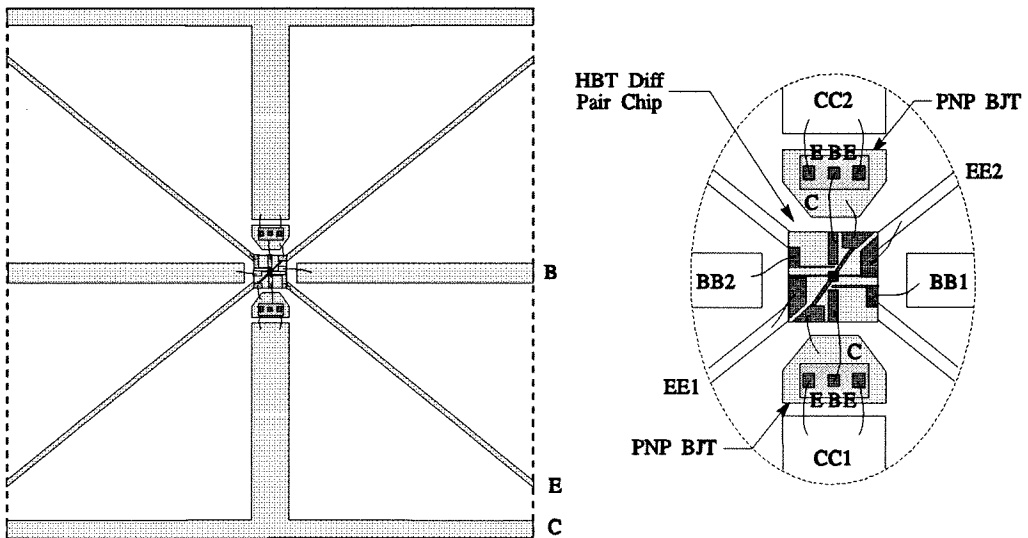


Figure 6.2 Plot of theoretical oscillation frequency versus varactor capacitance for the proposed voltage-controlled oscillator grid based on the unit cell design of Power Grid 1.



(a)



(b)

Figure 6.3 (a) Medium-power differential pair of Sziklai connected bipolar transistors. (b) Layout of the proposed Sziklai power amplifier grid.

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