

**GROWTH, CHARACTERIZATION, AND  
SIMULATION OF NOVEL  
SEMICONDUCTOR TUNNEL STRUCTURES**

Thesis by  
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## Abstract

This thesis presents investigations of novel semiconductor heterostructure devices based on quantum mechanical tunneling. Due to their small characteristic dimensions, these devices have extremely fast charge transport properties. Thus, it is expected that tunnel structure devices will be well-suited to high frequency and optoelectronic applications. The work presented here can be divided into three sections. In the first section, a theoretical model for simulating current-voltage behavior in single barrier heterostructures is developed. The simulations are then used to design a novel single barrier negative differential resistance (NDR) device. The second section consists of detailed experimental characterizations of single barrier  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  heterostructures, including the first demonstration of the novel single barrier NDR mechanism. Growth of III-V semiconductor heterostructures by molecular beam epitaxy (MBE) is the subject of the third section. Several aspects of tunneling are explored through characterization of these III-V structures.

In chapter 2, a theoretical model is developed to simulate tunneling currents in single barrier heterostructures. The model includes band bending effects and a two band treatment of electron attenuation coefficients in the barrier. It is proposed that certain material systems have the appropriate band alignments to realize a novel single barrier negative differential resistance mechanism. A thorough theoretical analysis of these single barrier NDR structures is presented.

The first experimental demonstration of the single barrier NDR mechanism is reported in chapter 3. The  $\text{HgCdTe}/\text{CdTe}$  material system was selected for the demonstration. In this material system, low temperatures ( $<20$  K) are needed to observe the NDR effect. However, it has been demonstrated recently that room temperature NDR can be obtained from  $\text{InAs}/\text{GaAsSb}$  single barrier structures. High temperature (190–300 K) current-voltage curves from the single barrier  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  heterostructures have also been investigated, leading to a direct

electrical measurement of the controversial HgTe/CdTe valence band offset.

In chapter 4, results are presented from several studies of III-V heterostructures grown by MBE. A measurement of the GaAs/AlAs valence band offset by x-ray photoemission spectroscopy yields a value of  $0.46 \pm 0.07$  eV, independent of growth sequence. Optical measurements of electron tunneling times in GaAs/AlAs double barrier heterostructures are performed by growing structures with very thin cap layers. Tunneling times as short as  $\approx 12$  ps are measured. Triple barrier GaAs/AlAs tunnel structures are found to display strong NDR, indicating that the tunneling process is coherent (as opposed to sequential) in nature. Finally, a technique for depositing high quality InAs buffer layers on GaAs substrates is developed.

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**Tunneling in MOCVD Grown GaAs-AlAs-GaAs Heterostructures,**

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**Negative Differential Resistances from  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$ -CdTe Single Quantum Barrier Heterostructures,**

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**Negative Differential Resistances from  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$ -CdTe Single Barrier Heterostructures,**

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**Evidence for Coherent Tunneling in Resonant Triple Barrier Structures,**

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# Contents

<b>Acknowledgements</b>	<b>ii</b>
<b>Abstract</b>	<b>v</b>
<b>List of Publications</b>	<b>vii</b>
<b>List of Figures</b>	<b>xv</b>
<b>List of Tables</b>	<b>xviii</b>
<b>1 Introduction</b>	<b>1</b>
1.1 Introduction to Thesis . . . . .	1
1.1.1 Overview . . . . .	1
1.1.2 Summary of Results . . . . .	2
1.1.3 Outline of Chapter . . . . .	3
1.2 Motivation . . . . .	4
1.2.1 High Speed Devices . . . . .	4
1.2.2 Heterostructures – Novel Electrical Properties . . . . .	5
1.2.3 Optoelectronics Applications . . . . .	8
1.3 Theoretical Simulations . . . . .	9
1.3.1 Band Offsets . . . . .	9
1.3.2 Band Bending Calculations . . . . .	11

1.3.3	Current-Voltage Simulations . . . . .	13
1.3.4	Tunneling Times . . . . .	14
1.4	Molecular Beam Epitaxy . . . . .	16
1.4.1	General Approach . . . . .	17
1.4.2	III-V growth . . . . .	19
1.4.3	II-VI MBE . . . . .	24
1.4.4	Group IV growth . . . . .	25
1.5	Single Barrier Negative Differential Resistance . . . . .	26
1.5.1	Overview . . . . .	26
1.5.2	Origin of NDR in Single Barrier Structures . . . . .	27
1.5.3	Summary of Experimental Results . . . . .	31
1.6	Outline of Thesis . . . . .	33
	References . . . . .	35
<b>2</b>	<b>Single Barrier Electron Tunneling: Theory and NDR Devices</b>	<b>39</b>
2.1	Introduction and Outline . . . . .	39
2.2	Theoretical I-V Simulations . . . . .	41
2.2.1	Band Bending . . . . .	41
2.2.2	Tunneling Currents . . . . .	43
2.3	Single Barrier GaAs/AlAs Structures . . . . .	53
2.4	Hg <sub>1-x</sub> Cd <sub>x</sub> Te Negative Differential Resistance Devices . . . . .	57
2.4.1	Growth Parameters . . . . .	59
2.4.2	Effects of Valence Band Offsets on NDR . . . . .	65
2.5	Other Material Combinations for Single Barrier NDR . . . . .	65
2.5.1	InAs-Ga <sub>1-x</sub> Al <sub>x</sub> Sb Single Barrier Heterostructures . . . . .	67
2.5.2	Pb <sub>1-x</sub> Sn <sub>x</sub> Te Single Barrier Heterostructures . . . . .	69
	References . . . . .	72

<b>3</b>	<b>Electrical Studies of <math>\text{Hg}_{1-x}\text{Cd}_x\text{Te}</math> Single Barrier Heterostructures</b>	<b>74</b>
3.1	Introduction . . . . .	74
3.1.1	Motivation and Background . . . . .	74
3.1.2	Summary of Results . . . . .	76
3.1.3	Outline of Chapter . . . . .	77
3.2	Samples . . . . .	78
3.3	Demonstration of NDR at Low Temperatures . . . . .	81
3.3.1	Sample TS6 . . . . .	81
3.3.2	Device Fabrication . . . . .	82
3.3.3	Low Temperature Electrical Contacts . . . . .	87
3.3.4	I-V Results at Low Temperatures . . . . .	88
3.4	Electrical Determination of the HgTe/CdTe Valence Band Offset . . . . .	95
3.4.1	Theoretical Simulations of Hole Currents . . . . .	95
3.4.2	Device Fabrication . . . . .	99
3.4.3	I-V Results and Analysis . . . . .	99
3.5	Other Samples . . . . .	105
3.6	Summary of Conclusions . . . . .	107
	References . . . . .	108
<b>4</b>	<b>Molecular Beam Epitaxy of III-V Heterostructures</b>	<b>110</b>
4.1	Introduction . . . . .	110
4.1.1	Background . . . . .	110
4.1.2	Summary of Results . . . . .	112
4.1.3	Outline of Chapter . . . . .	114
4.2	Standard $\text{Al}_x\text{Ga}_{1-x}\text{As}$ Heterostructures . . . . .	115
4.2.1	Substrate Preparation . . . . .	115
4.2.2	$\text{Al}_x\text{Ga}_{1-x}\text{As}$ Growth Parameters . . . . .	116
4.2.3	Double Barrier Heterostructures . . . . .	118

4.2.4	Quantum Well Photoluminescence . . . . .	121
4.2.5	Modulation doped GaAs layers . . . . .	123
4.2.6	Characterization of Thick GaAs Films . . . . .	124
4.3	Determination of the GaAs/AlAs Valence Band Offset . . . . .	125
4.3.1	Motivation and Background . . . . .	125
4.3.2	X-ray photoemission spectroscopy . . . . .	125
4.3.3	Samples . . . . .	126
4.3.4	Results . . . . .	128
4.4	Tunneling Times in GaAs/AlAs Double Barrier Heterostructures . .	129
4.4.1	Motivation and Background . . . . .	129
4.4.2	Measurement Technique . . . . .	130
4.4.3	Samples . . . . .	131
4.4.4	Results . . . . .	134
4.4.5	Ongoing Experiments . . . . .	135
4.5	Electron Coherence in Resonant Tunneling Structures . . . . .	136
4.5.1	Motivation and Background . . . . .	136
4.5.2	Samples . . . . .	137
4.5.3	Results . . . . .	139
4.6	Growth of InAs on GaAs substrates . . . . .	141
4.6.1	Motivation and Background . . . . .	141
4.6.2	Growth and In Situ Analysis . . . . .	142
4.6.3	Characterization . . . . .	144
4.7	Summary of Conclusions . . . . .	146
	References . . . . .	149
<b>A</b>	<b>MBE System</b>	<b>152</b>
A.1	Introduction and Outline . . . . .	152
A.2	Transfer Mechanism . . . . .	154

A.3	III-V Chamber Modifications . . . . .	155
A.3.1	Sb cracker . . . . .	155
A.3.2	Source Loading Information . . . . .	156
A.3.3	Liquid Nitrogen Plumbing . . . . .	157
A.3.4	Water Cooling . . . . .	157
A.3.5	Instrument Coating . . . . .	158
A.4	Prep/Analysis Module Modifications . . . . .	158
A.5	Metallization Chamber Modifications . . . . .	159
<b>B</b>	<b>Cleanroom</b>	<b>161</b>
B.1	Purpose . . . . .	161
B.2	Design of Cleanroom Facility . . . . .	162
B.2.1	General . . . . .	162
B.2.2	Specifications . . . . .	165
B.2.3	Utilities . . . . .	166

# List of Figures

1.1	Layer diagram of a typical HEMT . . . . .	6
1.2	Conduction band edge in a double barrier heterostructure. . . . .	7
1.3	Band diagrams for a GaAs/Al <sub>x</sub> Ga <sub>1-x</sub> As single barrier heterostructure . . . . .	12
1.4	Schematic diagram of MBE system . . . . .	18
1.5	Band diagram for Hg <sub>1-x</sub> Cd <sub>x</sub> Te NDR structure . . . . .	28
1.6	$K$ vs. $E$ in the energy gap of CdTe . . . . .	30
1.7	I-V curve from Hg <sub>1-x</sub> Cd <sub>x</sub> Te single barrier heterostructure . . . . .	32
2.1	Transmission coefficient for a square Al <sub>x</sub> Ga <sub>1-x</sub> As barrier . . . . .	49
2.2	Band diagram for a single barrier GaAs/AlAs heterostructure . . . . .	54
2.3	Measured and Calculated J-V curves for a single barrier GaAs/AlAs heterostructure . . . . .	56
2.4	Band diagram for a typical Hg <sub>1-x</sub> Cd <sub>x</sub> Te single barrier structure . . . . .	58
2.5	J-V curves for three electrode doping densities . . . . .	62
2.6	Current density vs. barrier thickness for a Hg <sub>1-x</sub> Cd <sub>x</sub> Te single barrier heterostructure . . . . .	64
2.7	Linear and Log current density vs. voltage plots for several choices of $\Delta E_v$ . . . . .	66
2.8	Band Diagram for a single barrier InAs/GaAs tunnel structure . . . . .	68

2.9	J-V curve for a single barrier InAs/GaAlSb tunnel structure . . . . .	70
3.1	TEM photograph of the GaAs/CdTe interface . . . . .	80
3.2	Side view of a fabricated device (schematic) . . . . .	84
3.3	Log current vs. log mesa diameter for a typical preparation of sample TS6 . . . . .	86
3.4	Reverse bias I-V curves at 4.2 and 15 K . . . . .	89
3.5	Forward bias I-V curve at 4.2 K . . . . .	91
3.6	High-resolution TEM picture of the single barrier interfaces . . . . .	93
3.7	Forward bias I-V curve from a 67 $\mu\text{m}$ diameter device . . . . .	94
3.8	Reverse bias I-V curve from a 67 $\mu\text{m}$ diameter device . . . . .	96
3.9	Experimental and theoretical J-V curves at 300 K from sample TS6	100
3.10	Experimental and theoretical J-V curves at 300 K from sample ML26A' . . . . .	102
3.11	$\text{Log}_e(J/T^2)$ vs. $1/kT$ . . . . .	104
3.12	Log current vs. log mesa diameter for a preparation of sample TS4 .	106
4.1	I-V curves for a typical double barrier structure at 300 K and 77 K	120
4.2	Photoluminescence spectrum of a single GaAs quantum well . . . . .	122
4.3	Four types of samples grown for XPS experiment . . . . .	127
4.4	Schematic diagram of growth sequence for tunneling time samples .	132
4.5	High-resolution TEM print of a sample with 34 $\text{\AA}$ barriers . . . . .	133
4.6	Schematic diagram of triple barrier heterostructure samples . . . . .	138
4.7	I-V curve from a triple barrier heterostructure . . . . .	140
4.8	Schematic layer diagram of InAs layer on GaAs . . . . .	143
4.9	RHEED oscillations for growth of InAs . . . . .	145
A.1	Schematic diagram of MBE system . . . . .	153

B.1 Drawing of the cleanroom . . . . . 163

# List of Tables

3.1	Table of growth parameters for $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$ single barrier heterostructure samples . . . . .	79
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# Chapter 1

## Introduction

### 1.1 Introduction to Thesis

#### 1.1.1 Overview

This thesis is concerned with the design and realization of novel semiconductor electronic devices based on quantum mechanical tunneling. It is possible to break the process of creating these devices into three distinct subprocesses: (i) theoretical simulations of device behavior, (ii) growth of the ultrathin layered heterostructures needed for tunneling, and (iii) the fabrication and characterization of the devices. This thesis includes work which would fall into each of these three categories. The theoretical models developed here are intended to facilitate the design of tunnel structures; emphasis is placed on simplicity and qualitative accuracy. A few semiconductor growth techniques have been proven capable of producing heterostructures which display reproducible tunneling behavior. In this thesis, the technique of molecular beam epitaxy (MBE) is employed to produce almost all of the tunnel structures studied. This choice is made because of the flexibility and straightforward process offered by MBE. Characterization of the tunnel structures is directed towards observing novel electronic properties and measuring

heterostructure material parameters which influence tunneling behavior strongly.

### 1.1.2 Summary of Results

One of the major results of this thesis is the proposal of a novel single barrier negative differential resistance (NDR) mechanism. A theoretical model is developed to simulate the current-voltage (I-V) behavior of single barrier heterostructures. The model includes band bending effects and a two band model for the electron imaginary wavevector (attenuation coefficient) in the barrier. The simulations are first applied to GaAs/AlAs single barrier structures. It is found that simple elastic tunneling through the AlAs  $\Gamma$ -point does not adequately explain the observed experimental I-V curves. Next, the theoretical model is used to analyze a  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  single barrier heterostructure. It is found that strong NDR behavior due to the novel mechanism can be expected from  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  single barrier structures with appropriately chosen parameters. Other material systems are also suggested as candidates for single barrier NDR.

The first demonstration of the novel single barrier NDR mechanism is also discussed in this thesis. I-V curves from a  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  single barrier structure are taken at low temperatures ( $<20$  K) to realize this result. The observation of NDR suggests that the HgTe/CdTe valence band offset is very small ( $<100$  meV) at low temperatures. High temperature I-V curves in these heterostructures are also investigated and analyzed. It is found that the valence band offset is large ( $>300$  meV) at 300 K. The high temperature I-V data (190–300 K) are consistent with a temperature dependent valence band offset.

This thesis also reports results from a number of studies of III-V heterostructures grown by molecular beam epitaxy. Several initial  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  “calibration” structures are discussed, including double barrier heterostructures, single quantum wells, and high electron mobility transistors. An x-ray photoemission spectroscopy

measurement on MBE grown heterojunctions yields a value of  $0.46 \pm 0.07$  eV for the GaAs/AlAs valence band offset, independent of growth sequence. Samples grown for an optical measurement of electron tunneling times in double barrier heterostructures are discussed. The measurement yields tunneling times as short as 12 ps for electrons escaping from a GaAs quantum well sandwiched by two 16 Å AlAs barriers. The tunneling times are found to depend exponentially on barrier thickness, in good agreement with theory. Triple barrier GaAs/AlAs heterostructures are found to yield strong resonant tunneling effects, indicating a coherent nature to the electron tunneling process. Finally, a technique for depositing high quality thick InAs layers on GaAs substrates is developed.

### 1.1.3 Outline of Chapter

The purpose of chapter 1 is to provide some introduction and background for the thesis, and to give an overview of the following chapters. Section 1.2 attempts to describe some of the motivations for developing heterostructure electronic devices whose behavior is governed by tunneling. Section 1.3 discusses the successes and limitations of a few theoretical models which are frequently applied to tunnel structures. Included in the discussion are band bending calculations, current-voltage simulations, band offset models, and tunneling time calculations. Section 1.4 describes the growth process of molecular beam epitaxy. Particular emphasis is placed on III-V semiconductor growth, although brief discussions of II-VI and group IV techniques are included. In section 1.5, a novel single tunneling barrier device is introduced. This device displays current-voltage characteristics which yield a negative differential resistance region due to elastic electron tunneling. The remainder of the thesis is summarized in section 1.6.

## 1.2 Motivation

### 1.2.1 High Speed Devices

Over the past two decades, increases in the frequencies at which semiconductor electronic devices can operate have triggered large scale technological changes in the world. Computer operations which previously required days can now be performed in fractions of a second. Microprocessors are commonly found in virtually every electronic system produced, including communications, medical, manufacturing, and consumer electronics equipment. It is a strong possibility that the next generation of high performance computers will rely upon GaAs devices, which are faster than their silicon counterparts because electrons in GaAs move approximately six times faster than in silicon. It seems likely that significantly faster devices will find applications. The degree to which older devices are replaced by newer, faster ones will probably be determined by cost/performance comparisons.

In general, the smaller an electronic device can be made, the faster it will be. Quantum mechanical tunneling effects through semiconducting films become important when layer thicknesses are reduced to 10–200 Å, depending upon the specific choices of materials. By comparison, it is difficult to obtain field effect transistors (FETs) with submicron channel lengths. One might therefore expect tunneling devices to be much faster than the current generation of semiconductor electronic devices. The prospect of extremely fast electrical devices is one of the major motivations for developing tunnel structures. The question of exactly what operating frequency can be attained for tunnel structures is a matter of debate. Many conflicting theoretical predictions for tunneling times in various structures have been published over the past twenty years.[1,2,3,4,5,6,7] Conversely, experimental measurements of these times have only recently been attempted because of the lack of adequately fast electronics. In fact, all of the measurements which have

been made utilize optical probing to resolve tunneling response times as short as a few picoseconds.[8,9,10,11] Structures grown by MBE for one of these measurements are discussed in Section 4.4.

## 1.2.2 Heterostructures – Novel Electrical Properties

In addition to having characteristic dimensions small enough for quantum mechanical tunneling effects, all of the devices studied in this thesis are *heterostructures*, consisting of thin epitaxial layers of different semiconducting materials. The ability to fabricate heterostructures by techniques such as MBE creates additional degrees of freedom in designing devices with novel properties. There are many examples of heterostructure devices which yield device characteristics not obtainable from bulk semiconductors. One application of heterostructures which does not involve tunneling is the high electron mobility transistor (HEMT). The layer sequence for a typical HEMT is illustrated in Fig. 1.1. The heterostructure consists of a heavily doped  $n$ -type  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  layer grown on top of an undoped  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  spacer layer and a thick film of undoped GaAs. In the structure, the dopants in the  $n$ -type  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  layer become ionized, yielding a high concentration of electrons in the GaAs film.\* These electrons carry current in the device by moving laterally through the GaAs film, with high mobilities at low temperatures resulting from the lack of ionized impurities in the GaAs. This *modulation doping* yields a heterostructure field effect device which is much faster than conventional FETs.

Another good example of the additional degree of freedom provided by heterostructures is the double barrier tunnel structure. This heterostructure requires at least two semiconducting materials with different energy gaps. The basic struc-

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\*These electrons actually become localized near the interface with the  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  spacer as a two-dimensional electron gas.

50 Å	GaAs, $n=1 \times 10^{18} \text{ cm}^{-3}$
600 Å	$\text{Al}_{.3}\text{Ga}_{.7}\text{As}$ , $n=1 \times 10^{18} \text{ cm}^{-3}$
200 Å	$\text{Al}_{.3}\text{Ga}_{.7}\text{As}$ , undoped
1.0 $\mu\text{m}$	GaAs, undoped
	Semi-Insulating GaAs Substrate

Figure 1.1: Schematic layer diagram of a typical GaAs –  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  high electron mobility transistor. Free electrons are placed in the undoped GaAs layer by growing a thin, heavily doped  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  layer, which becomes fully depleted. High mobilities result from the spatial separation of the ionized donor atoms from the free electrons.

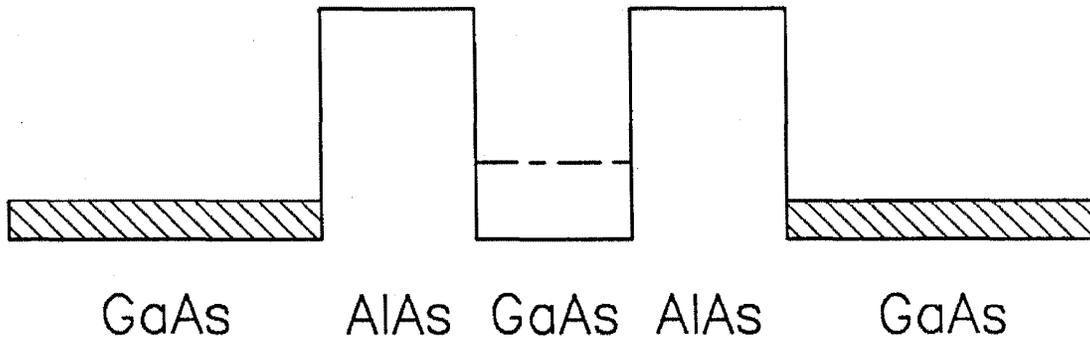


Figure 1.2: Schematic diagram for the conduction band edge in a GaAs/AlAs double barrier heterostructure as a function of distance in the direction perpendicular to the layers. The dashed line indicates the energy of the confined state in the quantum well. The shaded rectangles represent free electron gases in each of the  $n$ -type electrodes.

ture begins with a thick, doped layer of the smaller band gap material, forming an electrode. This is followed by two ultrathin, undoped layers of the larger band gap material which sandwich an ultrathin, undoped layer of the smaller band gap material. These three layers form a quantum well for electrons (and/or holes). Finally, a thick doped cap layer of the smaller band gap material is grown to form a second electrode. A schematic diagram for the conduction band edge in a typical GaAs/AlAs double barrier heterostructure is given in Fig. 1.2. In this example, GaAs has the smaller energy gap, and is used for the quantum well and electrodes. The AlAs is used for the thin quantum barriers. Because the barriers are thin ( $\approx 50 \text{ \AA}$ ), it is possible for electrons in the  $n$ -type GaAs cladding layers to tunnel across the structure. When a bias is applied between the electrodes, a tunneling current can be measured. This current is strongly enhanced when the applied

voltage becomes sufficiently large that the tunneling electrons have energies equal to the confined state energy in the quantum well. When the voltage becomes large enough that the conduction band edge in the negatively biased electrode is at a higher energy than the confined state in the quantum well, the enhanced tunneling vanishes, leading to a pronounced negative differential resistance. It has been proposed that these *resonant* tunneling structures could be used in high frequency oscillators, amplifiers, and mixers.

### 1.2.3 Optoelectronics Applications

In general, silicon is not a good material for optical and optoelectronic applications because its energy gap is not direct. Therefore, it is often necessary to use other semiconducting materials, such as GaAs. Many of these materials are well suited to epitaxial growth techniques like MBE. It is often difficult to make conventional electrical devices from these semiconductors. For example, metal-oxide-semiconductor (MOS) devices cannot be easily fabricated on semiconductors other than silicon because of the lack of a stable oxide. Some materials, such as InAs, are not suitable for conventional FETs because their energy gaps are too small to support the electric field induced by a metal gate. These difficulties increase the likelihood that tunnel structures could become important electrical devices for integration with optical and optoelectronic elements. Furthermore, optical devices are presently being explored as high speed alternatives to electrical devices in certain situations. In many of these applications, it may become necessary to provide high speed electronic links between the fast optical devices to realize their full potential. Tunnel structures seem to be a likely alternative for this purpose.

## 1.3 Theoretical Simulations

Published theoretical treatments of the various aspects of tunneling in semiconductors range from highly sophisticated models to calculations which could be performed on the back of an envelope, with no direct correlation between usefulness and sophistication. This section attempts to review some of the theoretical treatments of the relevant issues for the tunnel structures studied in the thesis. Where possible, comparisons are made to published experimental observations.

### 1.3.1 Band Offsets

Whenever a semiconductor is grown epitaxially on top of another semiconducting material, a discontinuity exists in the valence (and conduction) band edge at the interface. This discontinuity is often referred to as the band offset. The value of the valence band offset\* is crucial for many heterostructure devices because it determines the potential throughout a given structure. In cases of structures with quantum-sized dimensions, the band offsets play large roles in determining confinement energies and barrier heights. Without reasonably accurate knowledge of the band offset it is virtually impossible to predict even qualitative device behavior.

Several theoretical treatments of band offsets in semiconductors have been published. One of the earliest models proposed was the "common anion rule", which states that the valence band offsets in polar semiconductors are determined solely by the anions, i.e., the column V and VI elements in III-V and II-VI semiconductors, respectively.[12] Some predictions of this rule are that the valence band offset between InAs and GaAs should be zero, and that the CdTe/ZnSe valence band offset should be the same as for ZnTe/CdSe (assuming transitivity of band

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\*The conduction band offset can always be determined if the valence band offset and the two energy gaps are known.

offsets). The physical reasoning behind this model is that the states near the valence band maximum are derived mainly from the p-like atomic states of the anion. Therefore, the electronegativity of the anion largely determines the position of the valence band maximum. It should be pointed out that McCaldin et al.[12] do not claim that this rule will work for Al or Hg containing compounds.

More recently, it has been proposed that semiconductor-semiconductor interfaces should be treated analogously to metal-metal interfaces, with dipoles forming at the interfaces to shift the valence band offset away from the common anion value in certain cases.[13] The argument for the existence of dipoles is based upon the midgap states which form in semiconductors when they are terminated at an interface. For a particular value of the valence band offset, ordinary bulk states from one semiconductor are able to tunnel into these midgap states in the other semiconductor, leading to interface dipoles. It is argued that materials will tend towards a zero dipole band lineup. Another recent theoretical paper proposes that since semiconductor energy gaps change with temperature due to the electron-phonon interaction, the band offsets between different semiconductors should have some temperature dependence also.[14] It is proposed that in some cases, this temperature dependence can be quite large.

To date, it has been difficult to verify the results of most of the band offset theories. This difficulty can be attributed to a lack of experimental data for most of the semiconductor heterojunctions and conflicts between different published experimental measurements. Even for the heavily studied GaAs/AlAs band offset, a large range of experimental values of the valence band offset has been reported.[15,16,17,18] Furthermore, the two most heavily studied cases, GaAs/AlAs and HgTe/CdTe, do not test the common anion rule as stated by McCaldin et al.[12] The more recent theory of Tersoff[13] is in reasonable agreement with most published results for GaAs/AlAs and InAs/GaSb.[19] However, fur-

ther experimental data is needed to test the predictive value of this theory. In chapter 3 of the thesis, experimental results from electrical studies of single barrier HgCdTe heterostructures are given, and used to show evidence for a temperature dependent band offset in HgTe/CdTe. The theoretical model of Malloy et al.[14] is in reasonable agreement with these results.

### 1.3.2 Band Bending Calculations

Whenever a bias is applied between the two outer cladding layers of a semiconductor heterostructure, the conduction and valence band edges in the heterostructure must bend to accommodate the voltage. A calculated diagram of the conduction band edge vs. distance in the direction perpendicular to the layers of a GaAs/ $\text{Al}_x\text{Ga}_{1-x}\text{As}$  single barrier tunnel structure is given in Fig. 1.3(a). The method used to calculate the diagram is described briefly in section 2.2, and in complete detail by Bonnefoi.[20]

It is assumed in Fig. 1.3(a) that a constant quasi-Fermi level in each electrode can be defined, with the applied voltage equal to the difference between the two quasi-Fermi levels. The meaning of this assumption is that the chemical potential in each electrode is constant, i.e., ohmic voltage drops are ignored. The band diagram is then calculated by solving Poisson's equation self-consistently throughout the heterostructure. At each semiconductor-semiconductor interface, two boundary conditions are satisfied: (i) a step discontinuity equal to the conduction band offset between the two materials is placed in the conduction band edge at the interface, and (ii) the electrostatic displacement is continuous, i.e., the first derivative of the conduction band edge with position changes by the ratio of the dielectric constants of the two semiconductors as the interface is crossed. It can be seen from Fig. 1.3(a) that part of the applied voltage drops across the cladding layers as well as the barrier region.

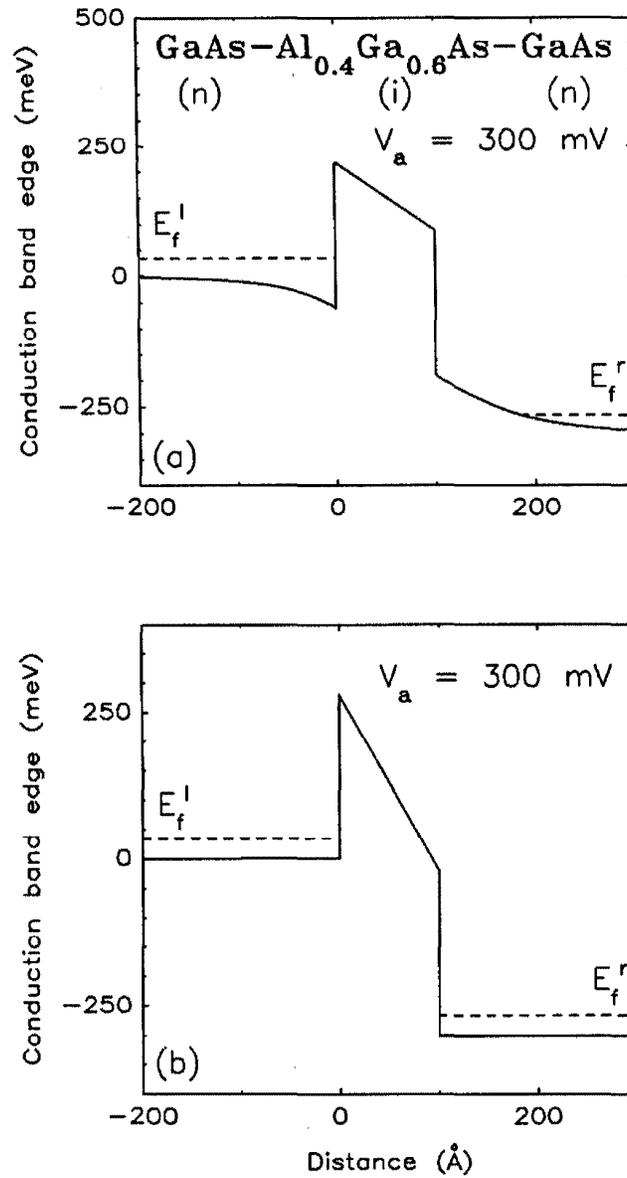


Figure 1.3: Conduction band edge of a GaAs - Al<sub>x</sub>Ga<sub>1-x</sub>As single barrier heterostructure with a 100 Å thick barrier layer under an applied bias of 300 mV. The electrodes have *n*-type doping densities of  $5 \times 10^{17} \text{ cm}^{-3}$ . (a) is calculated by the method of Bonnefoi et al.[23], while (b) is calculated by assuming that all of the applied voltage drops across the barrier.  $E_f^l$  ( $E_f^r$ ) represents the quasi-Fermi level in the left (right) electrode.

The treatment described above is classical in that it does not include two dimensional electron gases which result from quantum mechanical confinement in regions such as the accumulation layer in the left electrode of Fig. 1.3(a). However, the model does provide a more realistic picture of the conduction band edge in a heterostructure than the diagram obtained by assuming that the cladding layers are metal-like conductors. Figure 1.3(b) depicts the diagram obtained when the second boundary condition given above is replaced by the requirement that the electrodes maintain zero electric field. In this diagram, all of the applied voltage appears across the barrier region. It has been shown that predicted current-voltage (I-V) behavior in tunnel structures is considerably different both qualitatively and quantitatively when voltage drops in the cladding layers are ignored.[21,22,23,24] Furthermore, experimental I-V curves from GaAs-AlAs tunnel structures are in better agreement with the predictions of models which incorporate band bending than with those which assume that the barrier sustains all of the applied voltage.[23,25]

### 1.3.3 Current-Voltage Simulations

Although it is hoped that tunnel structures will operate as very high frequency electrical devices, DC current-voltage (I-V) measurements are often used to help characterize the structures. This is done largely because low frequency measurements can be performed with straightforward electronic techniques, and device response does not change, in general, until very high frequencies are reached. An example of a common DC characterization is the negative differential resistance (NDR) region in double barrier heterostructures. These structures are usually characterized by the peak current densities and peak-to-valley current ratios in their I-V curves. "State of the art" results for GaAs-AlAs double barriers are peak current densities of  $10^4$  A/cm<sup>2</sup>, and peak-to-valley current ratios of 20:1 at

77 K.

Theoretical simulations of I-V behavior in tunnel structures range from nearly closed form equations to large scale computer calculations.[26,27,28,22] In almost all cases, it is possible to obtain correct qualitative behavior, but nearly impossible to generate quantitatively consistent I-V curves. For example, all of the models correctly predict that the double barrier should show NDR, and some of them can predict the resonant voltages in close agreement with experiment. However, all of the models predict peak-to-valley current ratios which are orders of magnitude larger than those observed experimentally.[22,24] Two possible explanations for these failures exist. The first is that the transmission coefficient for electrons to tunnel across a barrier is strongly exponential with the thickness and height of the barrier, and the effective mass and energy of the tunneling carriers. Small errors in the choices of these parameters can produce differences of several orders of magnitude in the tunneling current. A second possibility is that transport mechanisms other than elastic tunneling may contribute strongly to the current, especially under conditions such as off-resonant biases in double barriers.

A fairly simple calculation of I-V curves for single barrier tunnel structures is developed in section 2.2.

### 1.3.4 Tunneling Times

In section 1.2.1, it was mentioned that the high frequency behavior of tunnel structures is a topic of interest. A number of different theoretical approaches to calculating the time required for an electron to tunnel through a potential barrier have been published.[1,2,3,4,5,6,7] Many of the approaches produce conflicting results, although most of them agree that the theoretical limit is shorter than 50 picoseconds and longer than 1 femtosecond. One fairly straightforward approach is to use the time dependent Schrödinger equation, starting with an electron wave

packet incident on the potential barrier(s).[1,5,3] The time required for the packet to traverse the structure is labeled the tunneling time. Another method explicitly calculates the RC time constant for a double barrier heterostructure by examining the theoretical small signal response of the current density to an applied voltage which modifies the potential profile of the double barrier.[6] A third approach is to calculate the tunneling time for monoenergetic electrons incident on a time-varying potential barrier.[2,7] Reconciling the differences between these models is well beyond the scope of this thesis.

For double barrier heterostructures, it is reported by Harada et al.[3] that the energy width of the resonance in the electron transmission coefficient,  $\Gamma$ , can be related to the tunneling time,  $\tau$ , through the uncertainty principle, i.e.,

$$\tau = \frac{\hbar}{\Gamma}. \quad (1.1)$$

This approach is particularly attractive because the electron transmission coefficient can be determined analytically by solving the time independent Schrödinger equation. The values of  $\tau$  determined by this method were found to agree with those produced by the time dependent Schrödinger equation approach.[3] Furthermore, recent photoluminescence experiments appear to yield tunneling times which are in reasonable agreement with the values predicted by this method.[9,10] These experiments measure the rate of decay of charge in the quantum well of a double barrier heterostructure. However, it is claimed by Guo et al.[5] that the time required for charge to build up in the well can be much longer than that needed for decay. It is likely that further experimental results will be needed to establish a valid theoretical model of tunneling times.

## 1.4 Molecular Beam Epitaxy

Molecular beam epitaxy (MBE) is a process for growing crystalline solids in which the constituent atoms or molecules are deposited on a heated substrate under ultrahigh vacuum (UHV) conditions. Beams of the constituent atoms or molecules are produced by evaporating ultrapure elemental or compound source materials. High quality epitaxial\* films are achievable because of precisely controlled substrate temperatures and molecular beam fluxes. Typically, MBE can produce films with monolayer abruptness. Other keys to good crystalline quality include substrate preparation (both chemical etching outside of vacuum, and oxide removal within the vacuum system) and surface structure during film deposition.

Two advantages of MBE for semiconductor research are the straightforwardness and flexibility of the growth process. Other techniques, such as chemical vapor deposition, require specific chemical reactions to occur at the substrate surface, in which many molecules other than those which are constituents of the epitaxial film are present. These chemical processes are often more difficult to understand and control than UHV deposition. Furthermore, the mean free paths of molecules in UHV are longer than the distances from the evaporation sources to the substrate. This means that complications involving gaseous or liquid flow patterns do not arise in MBE. The flexibility of MBE derives from the fact that it is possible, at least in principle, to evaporate any pure semiconductor source material under UHV conditions. It has been proven possible to grow most (but not all) of the known III-V, II-VI, and group IV semiconductors by choosing substrate temperatures and beam fluxes appropriately. Furthermore, two *in situ* growth analysis techniques are available in most MBE systems. Reflection high energy electron diffraction (RHEED) provides a method for analyzing the surface structure of the epitaxial

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\* *Epitaxial* means *along the same axis*. In the case of epitaxial films, it is taken to mean that the film has a crystallographic structure which is related to that of the substrate.

film during MBE growth, further enhancing the flexibility of MBE for research applications. Residual gas analysis (RGA) can provide information about possible sources of impurities in the UHV environment. A final consideration is the relative safety of MBE as compared to chemical vapor deposition, which often involves extremely toxic materials at high volume levels. This factor is often strongly weighted in the university research environment.

### 1.4.1 General Approach

Fig. 1.4 is a schematic diagram of the MBE system used to produce the heterostructures described in chapter 4. The system includes three separate growth chambers dedicated to III-V, II-VI, and group IV semiconductors, respectively, and an ESCA/Auger system, all connected by ultrahigh vacuum transfer tubes. The internal transfer mechanism is designed to allow the transfer of samples throughout the entire system without removing the samples from the UHV environment. The system also features a separate chamber for *in situ* metalization, a substrate heating and cleaning stage, and three sample introduction loadlocks. Gate valves are included at each of the points of connection between the systems and transfer tubes, allowing the chambers to be run independently, if desired. Brief descriptions of some of the special features of each of the chambers are given in Appendix A.

Whenever a semiconductor surface (or just about any other material surface) is exposed to atmosphere, radical changes in the surface composition occur due to the reaction of surface molecules with the molecules which make up the atmosphere, such as oxygen. Even at partial pressures as low as  $10^{-6}$  Torr, the surface molecules undergo collisions with the gaseous molecules once per second. In general, a surface which has been exposed to non-UHV conditions for any period of time has large concentrations of impurity atoms and poor crystalline properties. This degraded semiconductor surface is generally not suitable for further epitaxial

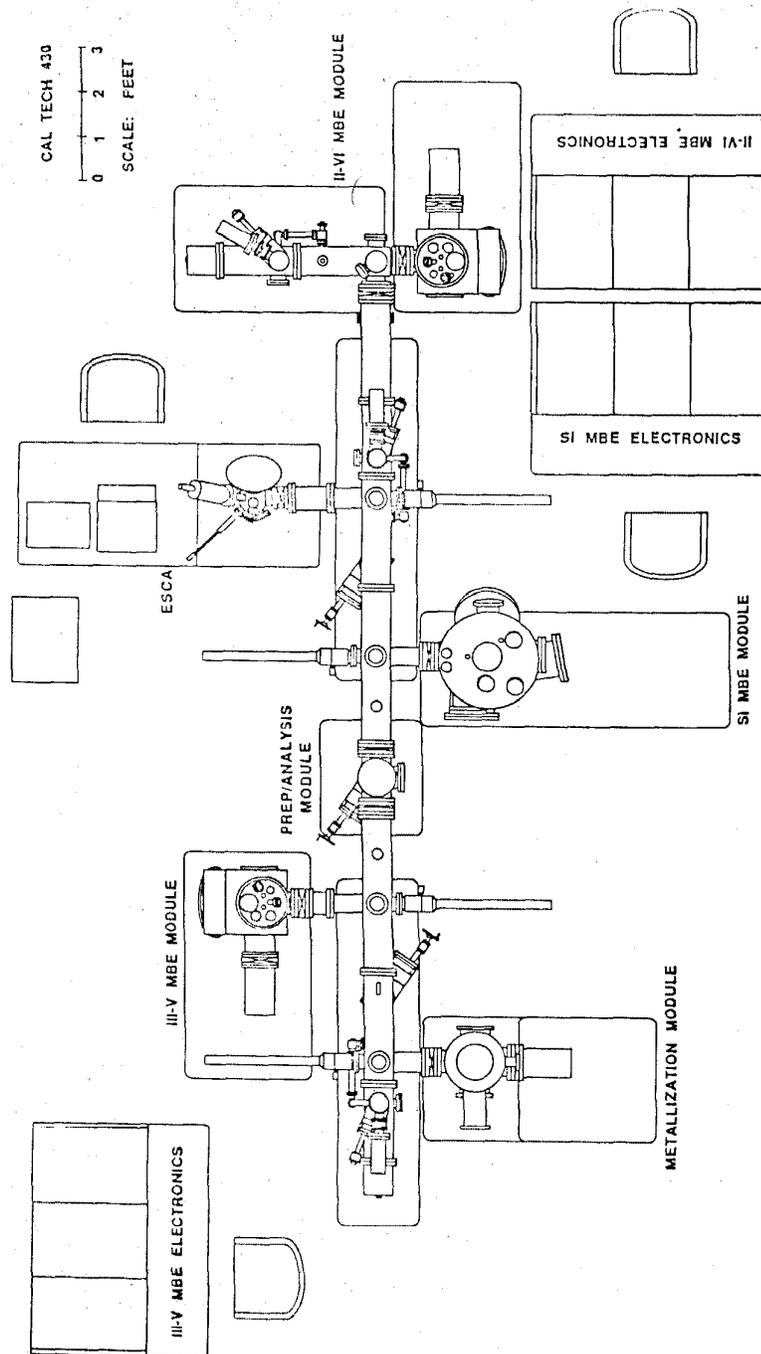


Figure 1.4: Schematic diagram of MBE system. The system has separate III-V, II-VI, and group IV growth chambers, and an ESCA/Auger system, connected by ultrahigh vacuum transfer tubes.

growth, and cannot be used to give an accurate picture of the surface conditions during growth. The intent of the MBE system depicted in Fig. 1.4 is to maintain maximum flexibility in the choices of materials for heterostructure devices (e.g., II-VI films on top of III-V films) and to allow each of the growth chambers to access the surface analysis capabilities of the ESCA/Auger chamber without removing the samples from vacuum. It would not be nearly as appropriate to place all of these growth and analysis capabilities into a single chamber (i.e., no gate valves between the processes) because even small background levels of impurities from different classes of semiconductors can produce large changes in the optical and electrical properties of a material. For example, an Arsenic concentration of 1 part per million in Silicon produces a background  $n$ -type doping level of  $5 \times 10^{16} \text{ cm}^{-3}$ , which is too large for many devices.

### 1.4.2 III-V growth

All of the heterostructures discussed in chapter 4 were produced in the III-V growth chamber portion of the MBE system depicted in Fig. 1.4. Detailed descriptions of the growth parameters used for each of these structures are given in chapter 4. The purpose of this section is to introduce some of the guiding principles behind III-V growth, and to review the specific materials characteristics of several of the III-V compounds. Of these compounds, GaAs and AlAs (and  $\text{Al}_x\text{Ga}_{1-x}\text{As}$ ) are by far the most extensively grown by MBE, with InAs a distant third.[29] Sufficient work has been done on GaSb, AlSb, and InSb to prove that MBE is capable of growing high quality epitaxial films of these materials. Phosphides have proven difficult to produce by MBE because of severe pumping difficulties associated with high phosphorous vapor pressures.[30]

An important characteristic of all of the III-V compounds is that they preferentially desorb group V atoms from their surfaces at their growth temperatures.

Therefore, it is necessary to provide an overpressure of the group V species at all times in order to maintain a stable crystalline structure at the surface of a III-V semiconductor. In the case of GaAs, which is typically grown at 600°C, a steady As flux is usually maintained on the material throughout the heating, oxide desorption, growth, and cooling processes. Growth is usually initiated by exposing the substrate to a Ga flux, with the growth rate determined by the arrival rate of Ga atoms at the surface. The arrival rate of As atoms must always be larger than that of the Ga atoms in order to maintain a stable surface. However, the ratio of the group V flux to the group III flux is usually not chosen to be significantly higher than what is needed to maintain the surface. For GaAs, an As/Ga ratio of approximately 6 is considered to be optimal.[29] Stoichiometry is easily preserved during growth because the excess group V atoms are not incorporated into the film. The *congruent sublimation temperature* is an important material constant for the III-V compounds. Above this temperature, the group V atoms are preferentially desorbed from the surface even under a steady group V flux. Optimal growth temperatures are usually near to, but not above, the congruent sublimation temperature for a material.

#### GaAs/ $\text{Al}_x\text{Ga}_{1-x}\text{As}$ Heterostructures

The combination of GaAs and  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  has been by far the most popular choice for MBE grown heterostructures, in which abrupt changes in energy gaps and refractive indices are desired.[31] The popularity of GaAs- $\text{Al}_x\text{Ga}_{1-x}\text{As}$  is largely due to the nearly perfect lattice match between GaAs and AlAs, which facilitates the growth of high quality epitaxial layers by removing considerations of strain. The usual procedure for growing these structures is to start with an etched GaAs substrate, and to remove its oxide by heating in an arsenic flux at approximately 600°C. Next, a thick epitaxial GaAs layer is often grown to

provide a very smooth buffer layer for the heterostructure. The GaAs growth rate is usually chosen to be approximately  $1 \mu\text{m/hr}$  ( $\approx 1$  monolayer/sec), at a substrate temperature of  $600^\circ\text{C}$ . For reasonably small values of  $x$ , the Al source oven temperature is varied to produce the desired  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  composition. It has been shown that higher quality  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  can be obtained by increasing the substrate temperature to as much as  $700^\circ\text{C}$ . [32] However, it is generally agreed that  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  and AlAs bulk films cannot be grown with as smooth a surface as GaAs. Furthermore, for  $x > 0.8$ , the  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  surface is not stable upon removal from vacuum due to its reactivity with atmosphere. N-type doping of these materials is usually accomplished by coevaporating a small amount of silicon during growth. Although Si would be an acceptor if it were to occupy As sites, it appears to prefer the group III sites, making it a donor. [33] Beryllium is the most commonly used  $p$ -type dopant for GaAs and  $\text{Al}_x\text{Ga}_{1-x}\text{As}$ .

In chapter 4 of this thesis, the growth procedures used for several varieties of GaAs- $\text{Al}_x\text{Ga}_{1-x}\text{As}$  heterostructures are discussed in detail. The following is a brief summary listing of each type of heterostructure studied, the purpose for the study, and a brief statement of the results obtained.

- 1) **Double Barrier Heterostructures.** These structures were prepared as two-terminal electrical devices. The I-V curves were used as a benchmark for interface smoothness and material quality. The best results for GaAs-AlAs structures are peak-to-valley current ratios of 2.5:1 and 10:1 at 300 K and 77 K, respectively. Peak current densities of  $10^4 \text{ A/cm}^2$  have been obtained.
- 2) **Single Quantum Wells.** Photoluminescence spectra were taken from these samples, with the linewidth of the peak from the confined state in the quantum well being used as a measure of the sharpness of the heterostructure interfaces. Full widths at half maximum of 3.8 meV have been observed for

50 Å GaAs quantum wells, corresponding to fluctuations in well thickness of one monolayer or less.

- 3) **High Electron Mobility Transistors.** The electron mobility in these modulation doped structures can be used as a measure of the background impurity quality and interface smoothness. Both the inverted and noninverted geometries (GaAs on  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  and vice-versa) have been studied. The heterostructures yielded electron mobilities which were far less than the best published results, but which nevertheless displayed enhancement due to the spatial separation between the electron gas and the ionized donors.
- 4) **GaAs-AlAs Superlattice.** One of these structures was grown for a calibration of a Raman scattering experiment. Superlattice phonon modes were observed.
- 5) **GaAs/AlAs Heterojunctions.** Several of these structures were grown for a measurement of the GaAs-AlAs valence band offset by x-ray photoemission spectroscopy. The band offset was found to be commutative, with a value of  $0.46 \pm 0.07$  eV.[15]
- 6) **Double Barriers for Optical Tunneling Rate Experiments.** These structures were designed with very thin (300 Å) GaAs cap layers so that the double barrier could be probed optically. In particular, the decay of the photoluminescence from the confined state in the quantum well was used as a measure of the time required for electrons to tunnel out of the well. This time is of extreme interest because it may govern the maximum frequencies at which double barrier devices can be operated. An exponential dependence of decay times with barrier thickness was observed.[10]
- 7) **Triple Barrier Heterostructures.** These structures were grown in order to

explore the issue of coherent vs. sequential tunneling. Two terminal I-V curves were observed to vary strongly with middle barrier thickness, yielding an estimate for the coherence time, i.e., the amount of time that an electron retains its phase information in the quantum well.[34]

## InAs

InAs is a potentially useful material for semiconductor heterostructures because it has a high electron mobility ( $10^4$  cm<sup>2</sup>/V-s at 300 K) and a small energy gap (350 meV at 300 K). In combination with AlAs, larger band gap materials can provide very high potential barriers for tunneling electrons or holes. This can greatly reduce the thermionic effects which tend to compete with tunneling currents. For example, the largest peak-to-valley current ratio ever reported for a double barrier heterostructure was observed in a structure which had In<sub>0.53</sub>Ga<sub>0.47</sub>As for the electrode and well material, and AlAs for the barrier material.[35] InAs may also have optical and optoelectronic applications due to its infrared energy gap. Growth considerations for InAs are remarkably similar to those for GaAs, with the major difference being the lower substrate temperature ( $\approx 520^\circ\text{C}$ ) needed for InAs.

The major stumbling block to widespread use of InAs in combination with GaAs and AlAs in heterostructures is the severe lattice mismatch (7%) between the materials. Extremely large strain energies result when more than one or two monolayers of InAs are grown with an in plane lattice constant equal to that of GaAs. For thicker InAs films, the strain energy is usually relieved by the appearance of misfit dislocations. Unfortunately, these dislocations are generally detrimental to device behavior.[36] One approach for avoiding the formation of dislocations in heterostructures containing InAs is to use large band gap materials, such as GaSb, AlSb, ZnTe, or CdSe which lattice match reasonably well with InAs. None of these materials is nearly as well understood as GaAs and AlAs for

MBE growth. Furthermore, high quality substrates are scarce and/or expensive for all of these materials (including InAs). Therefore, methods for growing buffer layers on GaAs which terminate with dislocation-free InAs are highly desirable. In section 4.6, a scheme is discussed, in which superlattice interfaces are used to getter dislocations in an InAs buffer layer on GaAs. The resulting bulk InAs layers are characterized by RHEED, Hall measurements, and x-ray diffraction.

### **Sb containing compounds**

The ability to grow antimonides (InSb, GaSb, AlSb) in addition to arsenides by III-V MBE should allow for increased flexibility in tailoring band edges and lattice constants in heterostructures. Unfortunately, little systematic work has been published regarding the influence of growth conditions on epitaxial layer properties for these materials. It is generally agreed that the material quality is more strongly dependent on the Sb to group III flux ratio in these semiconductors than for the arsenides.[37,38] This is largely due to the stronger tendency for excess Sb to become incorporated into the epilayers at the growth temperatures used. It is interesting to note that while the antimonide growth temperatures are somewhat lower than those for the arsenides, Sb evaporation is usually done near 600°C, as compared to near 300°C for As. Several applications have been proposed and/or realized for heterostructures containing Sb compounds, including high electron mobility devices, single and double barrier negative differential resistance devices, and infrared detectors.[39,40,41,42]

### **1.4.3 II-VI MBE**

Most of the known II-VI semiconductors have large direct energy gaps. Hence, many of the proposed applications for these materials are optical, with emphasis on the visible portion of the spectrum. Very little work has been reported on

the MBE growth of II-VI semiconductors, with most of the available literature coming from Japan. Although little of this thesis is devoted to the growth of II-VI materials, a few brief comments are made here for contrast to the growth considerations previously discussed for III-V semiconductors.

It is well known that most of the II-VI materials sublime congruently up to fairly high vapor pressures. In fact, it is common practice for MBE growth of these semiconductors to be accomplished by evaporating bulk material of the desired compound, e.g., evaporating ZnTe at 600°C in a Knudsen cell and growing it on a ZnTe substrate at 300°C. Elemental sources can also be used, with stoichiometry usually preserved in excess overpressures of either constituent.[43] Substrate temperatures for these materials are usually considerably lower than for III-V semiconductors. In general, an MBE system which is intended to be used for the growth of II-VIs can have the same design as one for III-Vs. Notable exceptions to this rule are systems designed to grow Hg-containing compounds. Because of the extremely high vapor pressure of mercury, special design considerations must be made to handle and remove it from the system routinely. In spite of these difficulties, a considerable amount of effort has been directed towards the MBE growth of  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$ . This interest stems mostly from the unique infrared tunability of the  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  energy gap.[43]

#### 1.4.4 Group IV growth

Although silicon is by far the most extensively studied and best understood of all of the semiconductors, MBE growth of Si is a relatively new technology. The lag in the development of Si MBE is largely due to the high temperatures required to evaporate significant quantities of silicon. Standard Knudsen cells are not capable of achieving these temperatures without significant chemical reactions occurring between the crucible material and the silicon charge. This problem has

been solved by bombarding the silicon charge with a beam of high energy electrons which evaporate it locally within the charge. Unfortunately, this technique requires the additional complication of installing electron guns inside the UHV chamber. The potential applications for Si MBE stem from the low growth temperatures which are possible, and the prospect of heterostructures which combine Si and Ge.<sup>†</sup>[44,45]

## 1.5 Single Barrier Negative Differential Resistance

### 1.5.1 Overview

Perhaps the most significant result reported in this thesis is the proposal and realization of a single barrier tunnel structure which displays a novel negative differential resistance (NDR). The active portion of this device consists of a thin epitaxial layer of one semiconductor which forms a quantum barrier between two thick cladding layers of another semiconductor. Electrons tunnel through the quantum barrier under an applied bias, producing a current. The I-V curves from this class of structures can have NDR regions when the tunneling electrons have energies close to the valence band edge of the barrier material. Although the device is demonstrated here for a  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  heterostructure, a few other material combinations are candidates for the single barrier NDR phenomenon. In fact,  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  is probably not the best choice for practical applications because its thermionic currents are high at room temperature, and it is a fragile material, making it difficult to achieve reproducible devices. At the time of this writing, the

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<sup>†</sup>Silicon and germanium are the only two conventional group IV semiconductors. Diamond has a prohibitively large energy gap, making it an insulator, and tin displays metallic behavior.

single barrier NDR concept has been demonstrated in a second heterostructure combination: InAs–Ga<sub>1-x</sub>Al<sub>x</sub>Sb.[40]

The motivation for developing single barrier NDR structures is to produce electrical devices which can operate at extremely high frequencies. In these applications, the NDR feature is useful because it can be exploited in designing oscillators, amplifiers, and mixers.[46] Furthermore, single barrier heterostructures may have better high-frequency response and are easier to fabricate than double barrier devices, which produce NDR due to resonant electron tunneling. The possibility of enhanced speed is due to the absence of a quantum well, which must be charged and discharged as electrons pass through it. To date, no experimental measurements of the time required for an electron to tunnel through a single barrier have been made.

### 1.5.2 Origin of NDR in Single Barrier Structures

This section attempts to give a basic physical argument for expecting NDR from single barrier heterostructures under certain conditions. A more detailed mathematical simulation of single barrier tunneling is provided in chapter 2. The specific case of NDR from single barrier structures is treated in section 2.4.

Figure 1.5 is a calculated energy band diagram for the single barrier heterostructure studied experimentally in chapter 3 under an applied bias of 50 mV. The device consists of a thin CdTe layer sandwiched between two Hg<sub>0.78</sub>Cd<sub>0.22</sub>Te electrodes, doped *n*-type. These materials were selected for the single barrier heterostructure because their band alignments satisfy the requirement for observing NDR. Assuming a small valence band offset between HgTe and CdTe,\* the tunneling electrons which originate in the Hg<sub>0.78</sub>Cd<sub>0.22</sub>Te electrodes lie much closer in energy to the valence band edge in CdTe than to the conduction band edge. This

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\*The actual value of the valence band offset is still a matter of debate

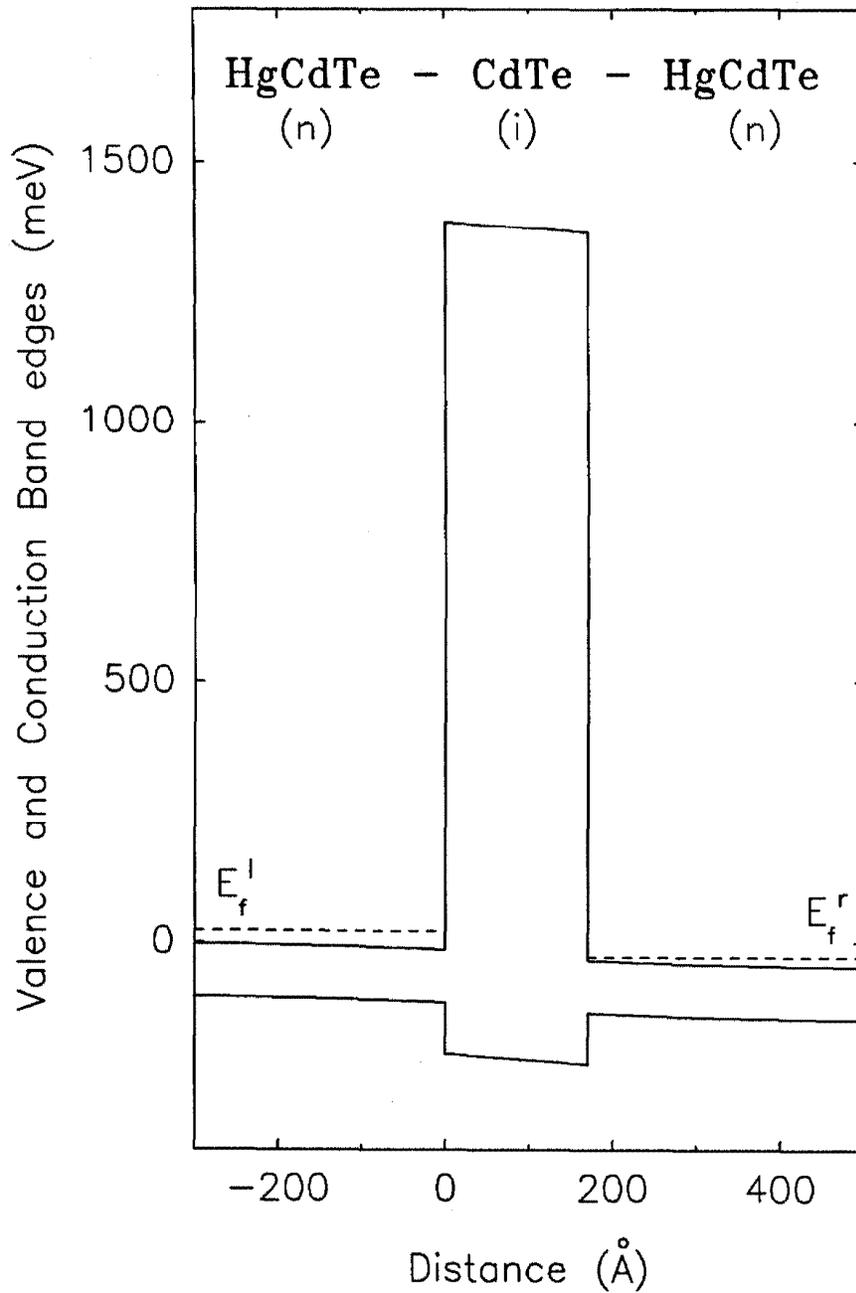


Figure 1.5: Valence and conduction band edges in the  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  single barrier heterostructure under an applied bias of 50 mV. A 170 Å CdTe barrier layer is sandwiched between two  $n$ -type  $\text{Hg}_{0.78}\text{Cd}_{0.22}\text{Te}$  electrodes with carrier densities of  $4 \times 10^{16} \text{ cm}^{-3}$ .

situation is uncommon among the well-studied combinations of semiconductors. In addition to these band alignments, there are two conditions which must be satisfied in order to observe NDR from a single barrier heterostructure. The first of these is that the total current must be dominated by elastic electron tunneling. The second condition is that a reasonably large fraction of the total applied voltage must be dropped across the barrier, instead of across the cladding layers. For example, the band diagram in Fig. 1.5 depicts a situation in which roughly 40% of the total bias appears across the CdTe layer. The remainder of the voltage is lost in creating depletion and accumulation regions in the electrodes. Simulations indicate that the quantum barrier must drop at least 25% (roughly) of the total voltage in order to observe NDR.

In the WKB approximation, an electron has a transmission probability of tunneling through a single quantum barrier,  $T$ , given by:

$$T \propto \exp \left[ -2 \int_0^w K dx \right], \quad (1.2)$$

where  $K$  is the imaginary part of the electron wavevector in the forbidden region, and  $x$  is the distance in the direction perpendicular to the layers, with  $x = 0$  and  $x = w$  defined to be the positions of the interfaces between the barrier and the electrodes. In this situation,  $K$  behaves as the attenuation constant for an electron tunneling through the single barrier. The numerical value of  $K$  is determined by the specific barrier material and the energy of the tunneling electron. In a direct band gap semiconductor, such as CdTe, the electron wavevector is purely imaginary for energies in the forbidden gap, and purely real for energies in the conduction and valence bands. Since the electron wavevector must be continuous with energy, both the real and imaginary parts must go to zero at the conduction and valence band edges. Figure 1.6 contains the results of a two band model,  $k \cdot p$  theory calculation which gives  $K$  as a function of energy,  $E$ , in the energy gap of CdTe.[47] In this plot,  $K$  is seen to go to zero at the conduction and valence band edges, with a

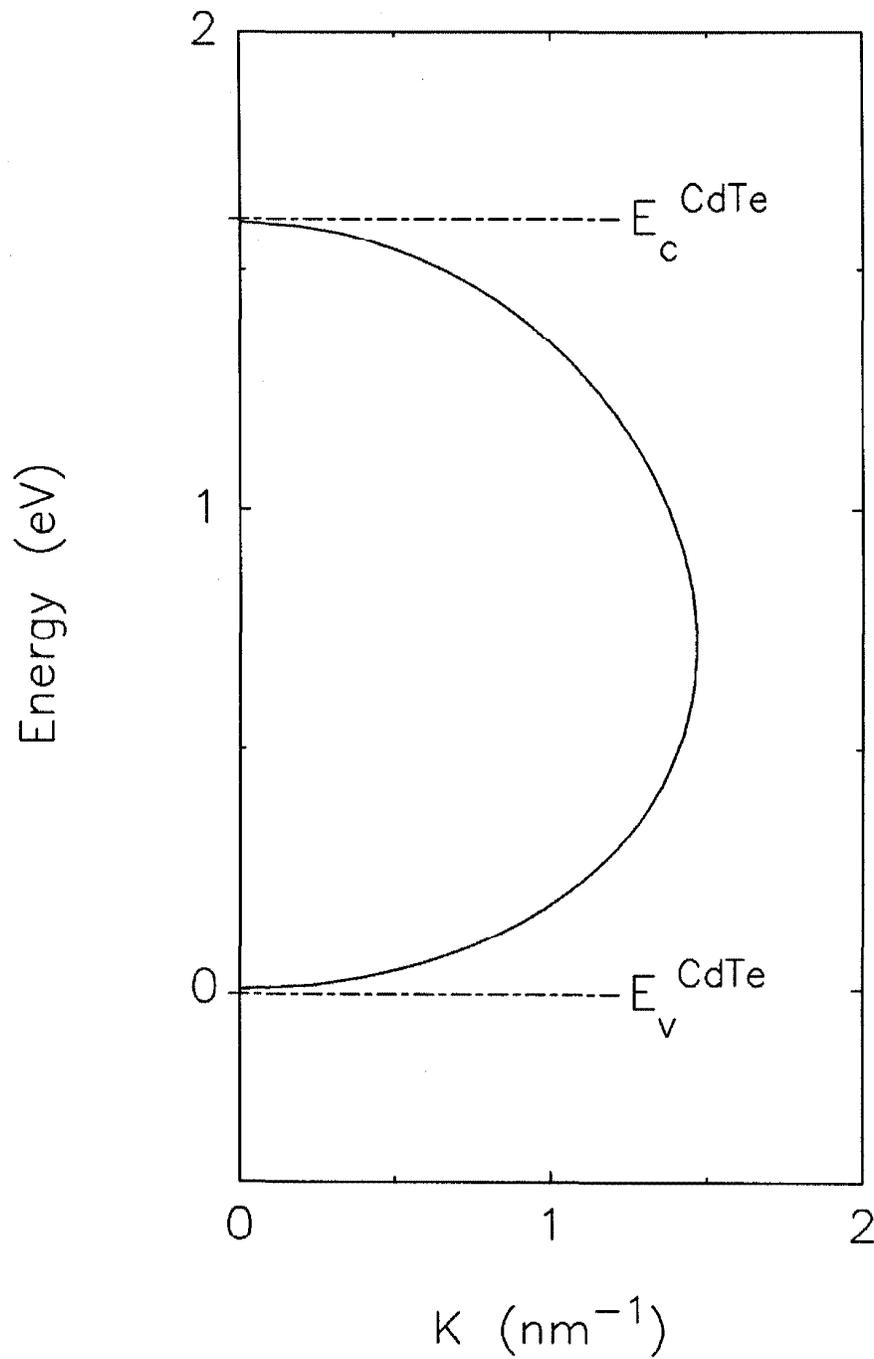


Figure 1.6: Calculation of the imaginary part of the electron wavevector,  $K$ , in the energy gap of CdTe.  $E_v$  ( $E_c$ ) denotes the valence (conduction) band edge in CdTe. Two band  $k \cdot p$  theory was used to calculate the curve.[47]

maximum near the middle of the energy gap. Hence, the transmission probability for electrons incident upon a CdTe barrier is largest for electrons with energies near the band edges, and smallest for electrons with energies near midgap. Since the tunneling electrons in the heterostructure depicted in Fig. 1.5 have energies which are closer to the valence band edge energy than to the conduction band edge in the CdTe barrier, the low energy part of the  $E$  vs.  $K$  curve in Fig. 1.6 is the portion of interest for this device. As the voltage applied to the heterostructure is increased, the tunneling electrons move to higher energies with respect to the CdTe barrier. Hence, they are confronted with increasing values of  $K$ , leading to decreasing transmission probabilities in Eqn. 1.2. As the transmission probability decreases, the tunneling current also decreases, yielding negative differential resistances. The NDR is a direct result of the uncommon band alignment in this heterostructure.

### 1.5.3 Summary of Experimental Results

To date, single barrier NDR has been observed in semiconductor heterostructures fabricated from two distinct material combinations. The first demonstration of single barrier NDR was made for the  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  heterostructure described above. Details of growth, device preparation, and measurements from this structure are explored in chapter 3. An I-V curve, taken at 4.2 K from the  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  single barrier heterostructure, is given in Fig. 1.7. The curve displays a peak-to-valley current ratio of 2:1, with a peak current density of  $0.51 \text{ mA/cm}^2$ . Both of these figures of merit are considerably lower than typical results from double barrier tunnel structures in GaAs-AlAs. Furthermore, it is likely that room temperature operation will be highly desirable in most of the practical applications of tunnel structures. The second realization of single barrier NDR was obtained from an  $\text{InAs-Ga}_{1-x}\text{Al}_x\text{Sb}$  structure.[40] Room temperature NDR was observed in this structure, with enhanced behavior at 100 K. Although the current density from

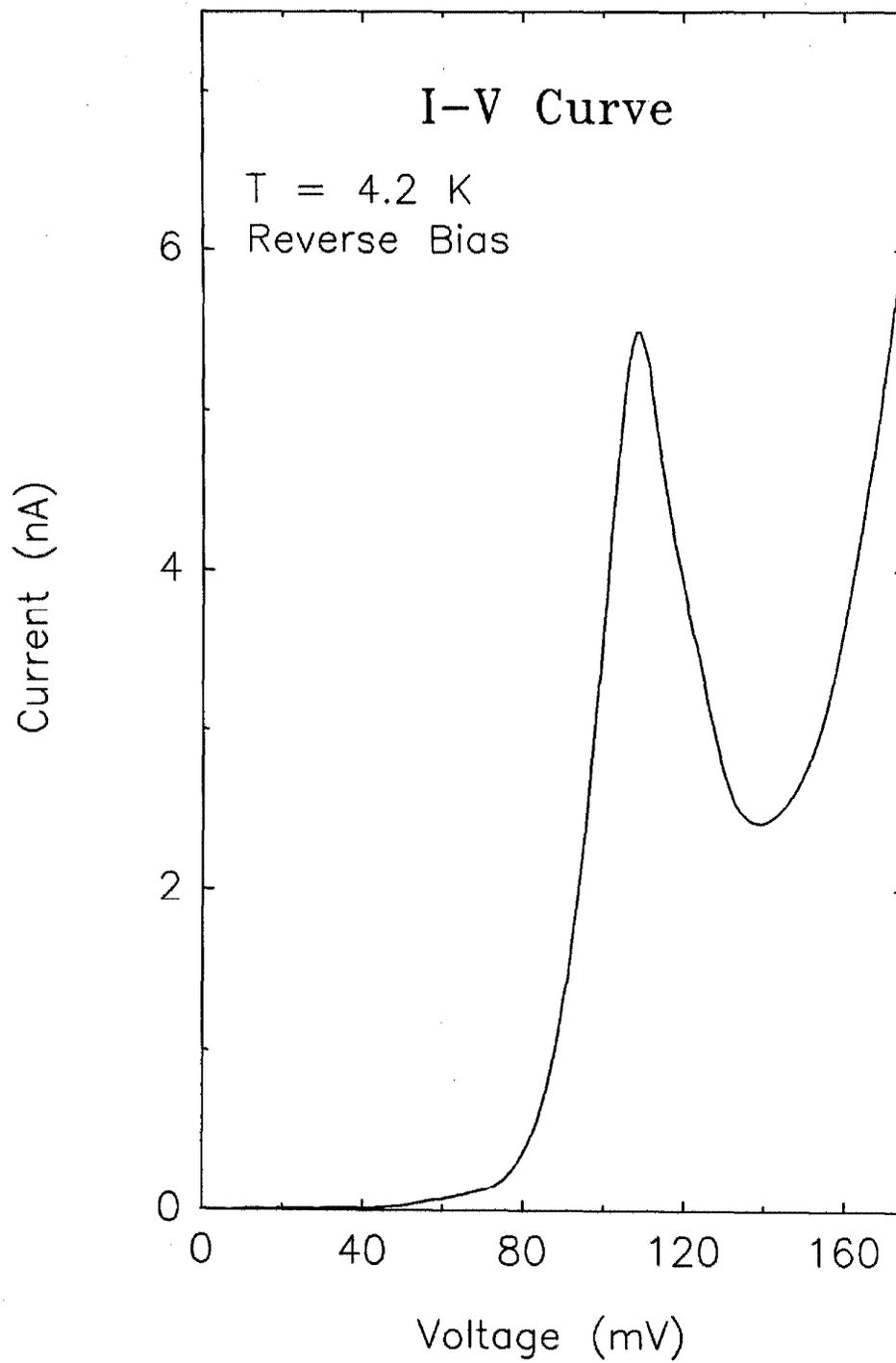


Figure 1.7: Experimental I-V curve, obtained at 4.2 K from a  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  single barrier heterostructure.

this structure was reasonably good ( $\approx 300A/cm^2$ ), the peak-to-valley current ratio was a very low 1.1:1. Further development of growth and processing techniques for these structures could improve behavior significantly.

## 1.6 Outline of Thesis

In chapter 2, a theoretical model is developed for simulating the electrical behavior of single barrier tunnel structures. Included in the model are calculations of band bending, imaginary wavevectors, transmission coefficients, and I-V curves. Simulations of single barrier GaAs-AlAs structures are presented and compared to experimental results. The model is then used to quantify the predictions of NDR from single barrier heterostructures fabricated from certain combinations of semiconductors.

Chapter 3 contains an experimental study of the current-voltage behavior of  $Hg_{1-x}Cd_xTe$  single barrier heterostructures. Growth and processing considerations are discussed, in addition to measurement techniques. Low temperature I-V curves are shown to display NDR due to the novel single barrier mechanism discussed previously. At higher temperatures, the thermionic hole currents are used to determine the valence band offset between HgTe and CdTe. The measured currents are found to be consistent with a temperature dependent band offset.

Several experimental studies which involved samples produced by the III-V MBE chamber are explored in chapter 4. Emphasis is placed upon the specific growth requirements and designs for each study. Several standard heterostructures are employed as diagnostic tools for the quality of materials and interfaces produced by the MBE chamber. Four major projects are then undertaken: (i) A measurement of the GaAs/AlAs valence band offset by x-ray photoemission spectroscopy, (ii) An optical measurement of the tunneling escape rate of electrons in

the well of a double barrier heterostructure, (iii) A test of coherent vs. sequential tunneling in a triple barrier heterostructure, and (iv) Development of a method (involving superlattice buffer layers), for reducing dislocations in bulk InAs films grown on GaAs.

Appendix A contains information regarding special features in the designs of several of the chambers of the MBE system depicted in Fig. 1.4. Appendix B describes the cleanroom in which the MBE system and most of the processing facilities used in this thesis are housed. Special design considerations are discussed, with emphasis upon adaptations made to tailor the cleanroom to the university research environment.

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## Chapter 2

# Single Barrier Electron

# Tunneling: Theory and NDR

# Devices

## 2.1 Introduction and Outline

In this thesis, *single barrier heterostructures* are defined to be epitaxial layered structures in which a single, thin layer of one semiconducting material forms a potential barrier to electrons or holes traveling between two bulk layers of another semiconductor. Although structures containing multiple quantum barriers and/or wells offer increased flexibility and variety in device behavior, ample motivation exists for studying single barrier heterostructures. For most of the possible combinations of semiconducting materials, fundamental heterojunction parameters, such as the valence band offset, are still unknown. These parameters are often critical in designing heterostructures for a particular purpose. A single barrier structure generally offers the most straightforward measurement of these parameters because its behavior is the most directly determined by them. Furthermore, single barrier

tunnel structures may be more suitable than multiple barrier devices for high speed applications, because quantum well charging and discharging times are eliminated.

This chapter develops a theoretical model for predicting the tunneling current through a single barrier heterostructure under an applied bias. Due to the relative simplicity of the potential in a single barrier structure (as compared to multiple barrier structures), it is possible for straightforward simulations of current-voltage (I-V) behavior to yield reasonable qualitative and quantitative accuracy. The theoretical model developed here is divided into two sections. In the first section, the band diagram for the single barrier structure is calculated as a function of applied bias. The band diagram is then used in the second section to calculate the tunneling current. Considerations of electron transmission probabilities and complex bandstructure are included in the second section.

In section 2.3 the I-V simulation is applied to single barrier GaAs/AlAs heterostructures. At high voltages, experimental tunneling currents are found to be larger than those predicted for elastic tunneling across the AlAs  $\Gamma$ -point. A combination of tunneling through the AlAs X-point with  $\Gamma$ -point tunneling is found to be consistent with the experimental I-V data.

As discussed in section 1.5, the proposal and realization of a single barrier negative differential resistance (NDR) device is one of the major results of this thesis. The  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  version of this device is analyzed theoretically in section 2.4. Theoretical predictions of peak-to-valley current ratios and peak current densities are given. Two other material combinations which are candidates for single barrier NDR, InAs/GaAlSb and PbSnTe, are also analyzed in section 2.5.

## 2.2 Theoretical I–V Simulations

### 2.2.1 Band Bending

As discussed previously in section 1.3.2, the conduction and valence band edges in a semiconductor heterostructure must bend to accommodate an applied bias. This section gives a brief summary of the method used in this thesis to calculate band diagrams for single barrier heterostructures. A more detailed explanation is given by Bonnefoi.[1] It is assumed here that a constant quasi-Fermi level in each electrode can be defined, with the applied voltage equal to the difference between the two quasi-Fermi levels. Ohmic voltage drops, i.e., changes in the conduction band edge due to electrical current passing through the electrode material, are ignored in this assumption. For most of the structures studied here, ohmic voltage drops are negligible because the total device resistance is much greater than the ohmic resistance of the cladding layers.

The basic formula for calculating band diagrams of heterostructures is to solve Poisson's equation in one dimension for each of the layers:

$$\frac{d^2 E_c(z)}{dz^2} = \frac{e\rho(z)}{\epsilon_0\epsilon_r}, \quad (2.1)$$

where  $E_c(z)$  is the conduction band edge as a function of  $z$ , the distance in the direction perpendicular to the layers,  $e$  is the electron charge,  $\rho(z)$  is the charge density as a function of  $z$ ,  $\epsilon_0$  is the permittivity of free space, and  $\epsilon_r$  is the dielectric constant of the material. In this equation,  $E_c(z)$  is used instead of the more familiar electrostatic potential,  $\phi(z)$ , for reasons of convenience. The two can be related by:

$$E_c(z) = -e\phi(z). \quad (2.2)$$

The charge density,  $\rho(z)$ , can be determined by summing the densities of ionized

dopants and free charge carriers;

$$\rho(z) = -e(n(z) - p(z) + N_A(z) - N_D(z)), \quad (2.3)$$

where  $n(z)$  and  $p(z)$  are the free electron and hole densities, respectively,  $N_A(z)$  is the density of ionized acceptors and  $N_D(z)$  is the density of ionized donors. For the structures of interest here, the densities of acceptor and donor atoms are determined from growth parameters. It is usually reasonable to assume that the donors and acceptors are fully ionized. The free carrier densities are related to the relative positions of the conduction and valence band edges with respect to the Fermi level. In the model used here, the  $T = 0$  K expressions for  $n(z)$  and  $p(z)$  are used as an approximation to the actual carrier densities;

$$n(z) = \begin{cases} 0 & E_f < E_c \\ \frac{1}{3\pi^2} \left[ \frac{2m_e^*}{\hbar^2} (E_f - E_c(z)) \right]^{3/2} & E_f \geq E_c \end{cases} \quad (2.4)$$

and

$$p(z) = \begin{cases} 0 & E_f > E_v \\ \frac{1}{3\pi^2} \left[ \frac{2m_h^*}{\hbar^2} (E_v(z) - E_f) \right]^{3/2} & E_f \leq E_v \end{cases}, \quad (2.5)$$

where  $E_f$  is the Fermi level,  $m_e^*$  ( $m_h^*$ ) is the electron (hole) effective mass, and  $E_v(z)$  is the valence band edge. Upon substituting the carrier densities in Eqns. 2.4 and 2.5 into Eqn. 2.1, a second order, nonlinear differential equation is obtained for  $E_c(z)$ . This equation can be solved numerically.

Once the solutions to Eqn. 2.1 have been obtained for each of the layers of a heterostructure, they can be joined by using two boundary conditions. The first is that the conduction band edge at an interface ( $z = z_0$ ) between two semiconductors, must take a discontinuous step equal to the conduction band offset between those two semiconductors:

$$E_c^A(z_0) = E_c^B(z_0) + \Delta E_c^{AB}, \quad (2.6)$$

where  $E_c^A$  is the conduction band edge in material A,  $E_c^B$  is the conduction band edge in material B, and  $\Delta E_c^{AB}$  is the conduction band offset between materials A and B. The second boundary condition is that the electric displacement,  $D(z)$ , must be continuous across an interface, i.e.,

$$\epsilon_A \frac{dE_c^A(z_0)}{dz} = D^A(z_0) = D^B(z_0) = \epsilon_B \frac{dE_c^B(z_0)}{dz}. \quad (2.7)$$

In addition to employing the  $T = 0$  K expressions for the free carrier densities, this model neglects two dimensional subbands, which should form in the potential wells created by accumulation layers. Both of these assumptions simplify the mathematics greatly, but can produce erroneous results under certain conditions. In particular, the  $T = 0$  K approximation is most valid for degenerate doping concentrations and low temperatures. Two dimensional subbands become more prominent at large applied biases, i.e., where the conduction band edge is the most steeply sloped. Although these approximations restrict the validity of the model, it is clear that the band diagrams generated are more physically correct than an assumption of no voltage drop in the electrodes.

## 2.2.2 Tunneling Currents

Once the band diagram for a single barrier heterostructure has been determined, it is possible to calculate the tunneling current through the structure. Several methods for performing this calculation have been published.[2,3,4,5,6,7] In this thesis, the method of Tsu et al.[3] is chosen because of its straightforward formalism. This method utilizes the time independent Schrödinger equation to compute transmission coefficients and current densities through the barrier. Modifications to this approach have been incorporated to include band bending results and non-square barriers.

The tunneling current calculation is based upon an assumption of nearly free

electron gases in the left and right electrodes. The electron wavefunctions,  $\Psi$ , are written:

$$\Psi = \frac{\exp(i\mathbf{k} \cdot \mathbf{r})}{\sqrt{V}}, \quad (2.8)$$

where  $\mathbf{r}$  is the distance vector,  $\mathbf{k}$  is the electron wavevector, and  $V$  is the crystal volume (used for normalization). The electrons follow the dispersion relation

$$E = E_c + \frac{\hbar^2 k^2}{2m_e^*}, \quad (2.9)$$

where  $E_c$  is the conduction band edge,  $E$  is the total energy, and  $m_e^*$  is the electron effective mass.

Due to the layered nature of the heterostructure, the potential can be treated as varying in only one dimension, i.e.,

$$E_c = E_c(z), \quad (2.10)$$

where  $z$  is the distance in the direction perpendicular to the layers of the heterostructure. The three dimensional Schrödinger equation can then be separated into perpendicular and parallel parts (relative to the layers of the heterostructure):

$$-\frac{\hbar^2}{2m_e^*} \left[ \frac{d^2}{dx^2} + \frac{d^2}{dy^2} \right] \Psi + \left[ -\frac{\hbar^2}{2m_e^*} \frac{d^2}{dz^2} + E_c(z) \right] \Psi = E\Psi. \quad (2.11)$$

Two mathematical simplifications result from this separation. The first is that the total energy is the sum of perpendicular and parallel energies;

$$E = \frac{\hbar^2}{2m_e^*} (k_x^2 + k_y^2) + E_z, \quad (2.12)$$

where  $E_z$  is defined to be the perpendicular energy. The second result is that  $\Psi$  is the product of a function which depends only on the parallel distances  $y$  and  $x$ , with a function which depends only on  $z$ ;

$$\Psi = \psi(z) \exp[i(k_x x + k_y y)]. \quad (2.13)$$

It should be noted that, since  $E_c(z)$  is independent of  $x$  and  $y$ , it is assumed that  $k_x$  and  $k_y$  are constant for an electron tunneling elastically across the heterostructure.

The current density in the  $z$  direction for an occupied state is given by :

$$J_z = \frac{e\hbar}{2m_e^*i} \left( \Psi^* \frac{\partial \Psi}{\partial z} - \Psi \frac{\partial \Psi^*}{\partial z} \right). \quad (2.14)$$

For an occupied state tunneling from the left electrode to an available state in the right electrode, we assume that

$$\psi_{left}(z) = \frac{1}{\sqrt{V}} [\exp(ik_z z) + r \exp(-ik_z z)], \quad (2.15)$$

and

$$\psi_{right}(z) = \frac{1}{\sqrt{V}} [t \exp(ik_z z)]. \quad (2.16)$$

Application of Eqn. 2.14 to Eqn. 2.15 yields

$$J_z^{left} = \frac{e\hbar k_z}{m_e^* V} (1 - r^2) \quad (2.17)$$

and

$$J_z^{right} = \frac{e\hbar k_z}{m_e^* V} t^2. \quad (2.18)$$

The requirement that the current density be constant throughout the structure in steady state then gives:

$$1 - r^2 = t^2 \quad (2.19)$$

as expected. The quantity  $t^2$  ( $r^2$ ) is called the transmission (reflection) coefficient, and is assumed to be a function of the perpendicular energy of the tunneling electrons only. Furthermore, it is assumed that  $t^2$  is the same for particles moving left to right as for particles moving right to left.

To calculate the elastic tunneling current from the left electrode to the right electrode, it is necessary to multiply Eqn. 2.18 by the probability that the states in the left are occupied and that the states in the right are empty;

$$J_{l \rightarrow r} = \frac{e\hbar k_z}{m_e^* V} t^2 f_l(E) [1 - f_r(E)], \quad (2.20)$$

where  $f_l(E)$  ( $f_r(E)$ ) is the Fermi distribution function in the left (right) electrode. Letting  $E_{fl}$  and  $E_{fr}$  represent the quasi-Fermi levels in the left and right electrodes, respectively, yields:

$$f_l(E) = \frac{1}{1 + \exp[(E - E_{fl})/kT]}, \quad (2.21)$$

$$f_r(E) = \frac{1}{1 + \exp[(E - E_{fr})/kT]}. \quad (2.22)$$

Similarly, the tunneling current from the right electrode to the left electrode is given by:

$$J_{r \rightarrow l} = \frac{e\hbar k_z}{m_e^* V} t^2 f_r(E)[1 - f_l(E)]. \quad (2.23)$$

The net tunneling current at a particular energy,  $J_{net}(E)$ , is then given by:

$$J_{net}(E) = J_{l \rightarrow r} - J_{r \rightarrow l} = \frac{e\hbar k_z}{m_e^* V} t^2 [f_l(E) - f_r(E)]. \quad (2.24)$$

Equation 2.24 can be multiplied by the density of states in  $k$ -space, and integrated over all available states to obtain an expression for the total tunneling current;

$$J = \int d^3k \frac{e\hbar k_z}{4\pi^3 m_e^*} t^2 [f_l(E) - f_r(E)]. \quad (2.25)$$

Utilizing the identity for the electrodes,

$$\frac{\partial E}{\partial k_z} = \frac{\partial E_z}{\partial k_z} = \frac{\hbar^2 k_z}{m_e^*}, \quad (2.26)$$

Eqn. 2.25 becomes:

$$J = \frac{e}{4\pi^3 \hbar} \int dk_x \frac{\partial E_z}{\partial k_z} t^2 \iint dk_x dk_y [f_l(E) - f_r(E)]. \quad (2.27)$$

Finally, performing the integration over all  $k_x$  and  $k_y$ , and rewriting the integral over  $k_z$  in terms of the perpendicular energy yields:

$$J = \frac{em_e^* kT}{2\pi^2 \hbar^3} \int_{E_c(z_0)}^{\infty} dE_z t^2 \log \left( \frac{1 + \exp[(E_{fl} - E_z)/kT]}{1 + \exp[(E_{fr} - E_z)/kT]} \right). \quad (2.28)$$

The lower integration limit,  $E_c(z_0)$ , is the conduction band edge at the interface between the barrier and the negatively biased electrode.

Equation 2.28 is easily integrated numerically once the transmission coefficient and band diagram are known. The formula is sufficiently general that it can be adapted to include a transmission coefficient for an arbitrary barrier potential. Calculated band diagrams are used to determine the conduction band edge in the barrier and the parameters  $E_{fl}$ ,  $E_{fr}$ , and  $E_c(z_0)$ . It should be noted that the inclusion of band bending effects is slightly inconsistent since non-flat electrode bands do not yield plane wave solutions. However, this inconsistency is ignored here for the sake of simplicity.

### Transmission Coefficients

In general, it is possible to determine the transmission coefficient for tunneling through a single barrier heterostructure by solving the Schrödinger equation (Eqn. 2.11) in each of the layers of the structure. At each interface ( $z = a$ ), the solution for layer  $i$ ,  $\psi_i(z)$ , can then be matched to the solution for layer  $i + 1$ ,  $\psi_{i+1}(z)$ , by the boundary conditions:

$$\psi_i(z = a) = \psi_{i+1}(z = a) \quad (2.29)$$

$$\left. \frac{1}{m_e^*} \frac{d\psi_i}{dz} \right|_{z=a} = \left. \frac{1}{m_e^*} \frac{d\psi_{i+1}}{dz} \right|_{z=a} \quad (2.30)$$

The effective mass enters Eqn. 2.30 because of the condition of constant probability current across the interface.

For a single "square" potential barrier between two identical flat electrodes,  $t^2$  can be written in closed form;

$$t^2 = \left[ \frac{16m_e^2 m_b^2 k_l k_r K_b^2}{(k_l^2 m_b^2 + K_b^2 m_e^2)(k_r^2 m_b^2 + K_b^2 m_e^2)} \right] \exp(-2K_b w), \quad (2.31)$$

where  $w$  is the barrier width,  $m_e^2$  ( $m_b^2$ ) is the electron mass in the electrodes (barrier),  $k_l$  ( $k_r$ ) is  $k_z$  in the left (right) electrode, and  $K_b$  is the imaginary part of the electron wavevector in the barrier. In this formula, the exponential factor,

$\exp(-2K_b w)$ , tends to dominate the prefactor for typical problems of interest.[8] For an arbitrary potential barrier, the Wentzel–Kramers–Brillouin (WKB) approximation is used in place of the closed form exponential factor in Eqn. 2.31:

$$t^2 = \left[ \frac{16m_e^2 m_b^2 k_l k_r K_b^2}{(k_l^2 m_b^2 + K_b^2 m_e^2)(k_r^2 m_b^2 + K_b^2 m_e^2)} \right] \exp(-2 \int_0^w K_b dz), \quad (2.32)$$

where the integration limits,  $z = 0$  and  $z = w$ , are the left and right interfaces between the barrier and the electrodes.

### Imaginary Part of the Electron Wavevector

As discussed in section 1.5.2, the imaginary part of the electron wavevector,  $K$ , is determined by the energy of the tunneling state, and the properties of the barrier material. It was argued previously that  $K$  should go to zero at the conduction and valence band edges of a direct energy gap semiconductor, with a maximum near midgap. This section gives an abbreviated derivation of a two band model  $k \cdot p$  theory formula for  $K$  as a function of energy,  $E$ , in the direct bandgap of an arbitrary semiconductor. A more general derivation is given by Kane.[9] This formula differs substantially from the commonly used “one band” formula:

$$K = \left( \frac{2m_e^*(E_c - E)}{\hbar^2} \right)^{1/2}. \quad (2.33)$$

Fig. 2.1 depicts the transmission coefficient for tunneling across a square  $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$  barrier as calculated with the one and two band formulas. The error made by the one band model becomes increasingly more pronounced as the energy is lowered towards the valence band edge.

The  $k \cdot p$  method gives the bandstructure of a semiconductor by constructing bands from well-known parameters (energy gaps and effective masses). Initially, the electronic states are written as Bloch functions:

$$\Psi_n(\mathbf{k}, \mathbf{r}) = \exp(i\mathbf{k} \cdot \mathbf{r})u_n(\mathbf{k}, \mathbf{r}), \quad (2.34)$$

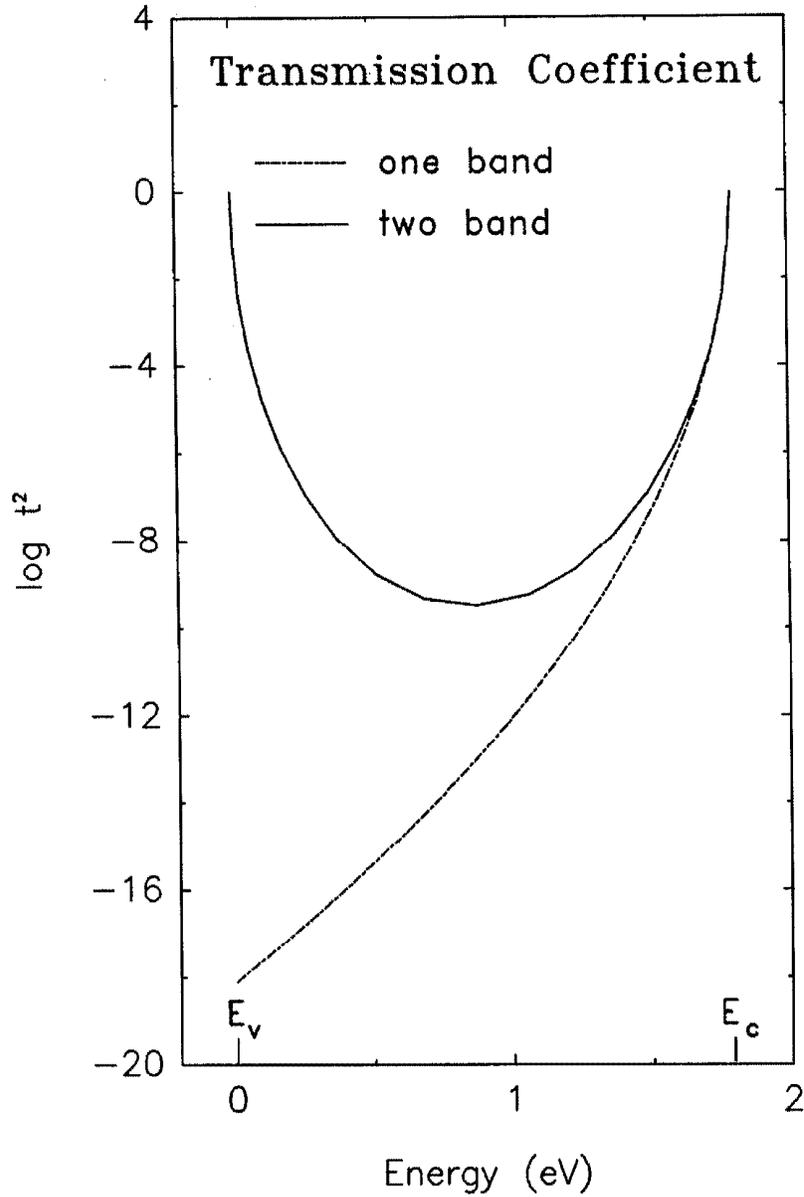


Figure 2.1: Log of the transmission coefficient for electrons tunneling across a 100 Å  $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$  barrier. The zero of energy is taken to be the valence band edge in  $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ .  $E_v$  ( $E_c$ ) represents the valence (conduction) band edge energy. The dashed and solid lines represent the curves generated by calculating  $K$  with the one and two band formulas, respectively. The prefactor in Eqn. 2.31 is taken to be unity, since it is a function of the electrode material parameters.

where the index  $n$  refers to the band being described (e.g., conduction or valence),  $\mathbf{k}$  is the electron wavevector (real),  $\mathbf{r}$  is the distance vector, and the functions  $u_n$  have the periodicity of the crystal potential,  $V(\mathbf{r})$ .  $\Psi_n(\mathbf{k}, \mathbf{r})$  satisfies the Schrödinger equation,

$$H\Psi_n(\mathbf{k}, \mathbf{r}) = \left[ \frac{P^2}{2m} + V(\mathbf{r}) \right] \Psi_n(\mathbf{k}, \mathbf{r}) = E_n(\mathbf{k})\Psi_n(\mathbf{k}, \mathbf{r}), \quad (2.35)$$

where  $H$  is the Hamiltonian,  $P$  is the momentum operator,  $m$  is the free electron mass, and  $E_n(\mathbf{k})$  are the energy eigenvalues. Substituting the Bloch function expression for  $\Psi_n(\mathbf{k}, \mathbf{r})$  into the Schrödinger equation yields:

$$\left[ \frac{P^2}{2m} + \frac{\hbar\mathbf{k} \cdot \mathbf{P}}{m} + \frac{\hbar^2 k^2}{2m} + V(\mathbf{r}) \right] u_n(\mathbf{k}, \mathbf{r}) = E_n(\mathbf{k})u_n(\mathbf{k}, \mathbf{r}). \quad (2.36)$$

For direct semiconductors, the valence band maximum and conduction band minimum both occur at the center of the Brillouin zone. Hence, the energy eigenvalues between the two bands are known to be separated by the energy gap,  $E_g$ , at  $\mathbf{k} = 0$ . Defining the valence band edge to be the zero of energy, Eqn. 2.36 can be evaluated at  $\mathbf{k} = 0$ :

$$\left[ \frac{P^2}{2m} + V(\mathbf{r}) \right] u_v(0, \mathbf{r}) = 0u_v(0, \mathbf{r}), \quad (2.37)$$

and

$$\left[ \frac{P^2}{2m} + V(\mathbf{r}) \right] u_c(0, \mathbf{r}) = E_g u_c(0, \mathbf{r}), \quad (2.38)$$

where  $u_v(0, \mathbf{r})$  ( $u_c(0, \mathbf{r})$ ) is the valence (conduction) band eigenstate at  $\mathbf{k} = 0$ . Since we are considering only two bands in the semiconductor, \* the states at  $\mathbf{k} = 0$  are a complete basis in which eigenstates for arbitrary  $\mathbf{k}$  can be expanded:

$$u_v(\mathbf{k}, \mathbf{r}) = c_{vv}u_v(0, \mathbf{r}) + c_{vc}u_c(0, \mathbf{r}) \quad (2.39)$$

$$u_c(\mathbf{k}, \mathbf{r}) = c_{cv}u_v(0, \mathbf{r}) + c_{cc}u_c(0, \mathbf{r}), \quad (2.40)$$

---

\*More bands can be included in the calculation through a straightforward extension of the basic principles.[9]

where the complex coefficients,  $c_{mn}$ , satisfy the condition

$$|c_{mv}|^2 + |c_{mc}|^2 = 1. \quad (2.41)$$

Rewriting Eqn. 2.36 with the expanded expression for the conduction band state gives:

$$\left[ \frac{P^2}{2m} + \frac{\hbar \mathbf{k} \cdot \mathbf{P}}{m} + \frac{\hbar^2 k^2}{2m} + V(\mathbf{r}) - E_c(k) \right] (c_{cv} u_v(0, \mathbf{r}) + c_{cc} u_c(0, \mathbf{r})) = 0, \quad (2.42)$$

where it has been assumed that  $E_c(\mathbf{k}) = E_c(k)$  (this is true for direct gap semiconductors near  $k = 0$ ).

At this point, several identities are needed. The eigenstates at  $k = 0$  are orthogonal and chosen to be normalized,

$$\int d^3 r u_c^*(0, \mathbf{r}) u_v(0, \mathbf{r}) = \int d^3 r u_v^*(0, \mathbf{r}) u_c(0, \mathbf{r}) = 0, \quad (2.43)$$

$$\int d^3 r u_v^*(0, \mathbf{r}) u_v(0, \mathbf{r}) = \int d^3 r u_c^*(0, \mathbf{r}) u_c(0, \mathbf{r}) = 1. \quad (2.44)$$

Next, axes are chosen such that

$$\mathbf{k} \cdot \mathbf{P} = kP. \quad (2.45)$$

Since  $P$  is a Hermitian operator,

$$\int d^3 r u_v^*(0, \mathbf{r}) P u_c(0, \mathbf{r}) = \int d^3 r u_c^*(0, \mathbf{r}) P u_v(0, \mathbf{r}) \equiv p. \quad (2.46)$$

Finally, since the  $k = 0$  eigenstates are band extrema,<sup>[9]</sup>

$$\int d^3 r u_v^*(0, \mathbf{r}) P u_v(0, \mathbf{r}) = \int d^3 r u_c^*(0, \mathbf{r}) P u_c(0, \mathbf{r}) = 0. \quad (2.47)$$

All of the integrals above are taken over the unit cell for the crystal.

Utilizing the above identities, Eqn. 2.42 can be multiplied by  $u_v^*(0, \mathbf{r})$  and integrated over the unit cell, yielding:

$$\left( \frac{\hbar^2 k^2}{2m} - E_c(k) \right) c_{cv} + \frac{\hbar k p}{m} c_{cc} = 0. \quad (2.48)$$

Performing the same operation with  $u_c^*(0, \mathbf{r})$  gives:

$$\frac{\hbar k p}{m} c_{cv} + \left( E_g + \frac{\hbar^2 k^2}{2m} - E_c(k) \right) c_{cc} = 0. \quad (2.49)$$

The requirement for a solution to Eqns. 2.48 and 2.49 is that

$$\begin{vmatrix} \frac{\hbar^2 k^2}{2m} - E_c(k) & \frac{\hbar k p}{m} \\ \frac{\hbar k p}{m} & E_g + \frac{\hbar^2 k^2}{2m} - E_c(k) \end{vmatrix} = 0. \quad (2.50)$$

Solving the determinant in Eqn. 2.50 for  $E_c(k)$  yields

$$E_c(k) = \frac{E_g}{2} + \frac{\hbar^2 k^2}{2m} \pm \frac{E_g}{2} \left[ 1 + \frac{4\hbar^2 k^2 p^2}{E_g^2 m^2} \right]^{1/2}. \quad (2.51)$$

Only the root with the positive sign in Eqn. 2.51 gives  $E_c(k=0) = E_g$  as required by the choice of energy eigenvalues. In order to calculate the bandstructure (i.e., find  $E_c(k)$ ), it is necessary to determine a value for  $p$ . For small values of  $k$ ,

$$\frac{4\hbar^2 k^2 p^2}{E_g^2 m^2} \ll 1, \quad (2.52)$$

and Eqn. 2.51 can be simplified:

$$E_c(k) = E_g + \frac{\hbar^2 k^2}{2m} \left[ 1 + \frac{2p^2}{mE_g} \right]. \quad (2.53)$$

The electron effective mass is defined by:

$$\frac{1}{m_e^*} \equiv \frac{1}{\hbar^2} \left( \frac{\partial^2 E_c}{\partial k^2} \right). \quad (2.54)$$

It follows that,

$$\frac{1}{m_e^*} = \frac{1}{m} \left[ 1 + \frac{2p^2}{mE_g} \right], \quad (2.55)$$

or

$$\frac{2p^2}{m} = E_g \left( \frac{m}{m_e^*} - 1 \right). \quad (2.56)$$

Since the electron effective mass is well known for most direct gap semiconductors,  $p$  is easily determined. It is assumed that  $p$  is independent of  $k$  in this model.

Eqn. 2.51 is then a closed form dispersion relation for the conduction band energy as a function of  $k$ .

From Eqn. 2.51, values of  $E_c$  which are between 0 and  $E_g$  are obtained when  $k$  is imaginary. Making the substitution,

$$k = iK \quad (2.57)$$

and requiring real values of  $K$  yields an expression for the imaginary part of the electron wavevector in the energy gap:

$$K = \left(\frac{2m}{\hbar^2}\right)^{\frac{1}{2}} \left\{ \left[ E_g^2 \left(1 - \frac{m}{2m_e^*}\right)^2 + E_g E_c \left(\frac{m}{m_e^*} - 1\right) \right]^{\frac{1}{2}} - E_c - E_g \left(\frac{m}{2m_e^*} - 1\right) \right\}^{\frac{1}{2}}. \quad (2.58)$$

The formula in Eqn. 2.58 has the predicted qualitative behavior, with  $K = 0$  at  $E_c = (0, E_g)$ , and maximized near midgap.

## 2.3 Single Barrier GaAs/AlAs Structures

Although AlAs is often used in combination with GaAs in tunnel structures, there remains some doubt as to how it should be treated as a barrier material. The ambiguity arises from the fact that AlAs is an indirect semiconductor, with its conduction band minimum towards the Brillouin zone edge in the [100]-direction.\* In fact, the indirect (X-point) energy gap is only 2.17 eV at 300 K, as compared to 3.02 eV for the direct ( $\Gamma$ -point) gap.[10] The potential barrier height seen by electrons tunneling from GaAs into AlAs is therefore considerably lower at the X-point than at the  $\Gamma$ -point. Fig. 2.2 is a band diagram for a single barrier GaAs/AlAs/GaAs tunnel structure which depicts this situation. In the figure, a valence band offset of 0.55 eV is assumed.[11]

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\*The AlAs valence band maximum is at the zone center, with characteristics similar to most direct gap semiconductors.

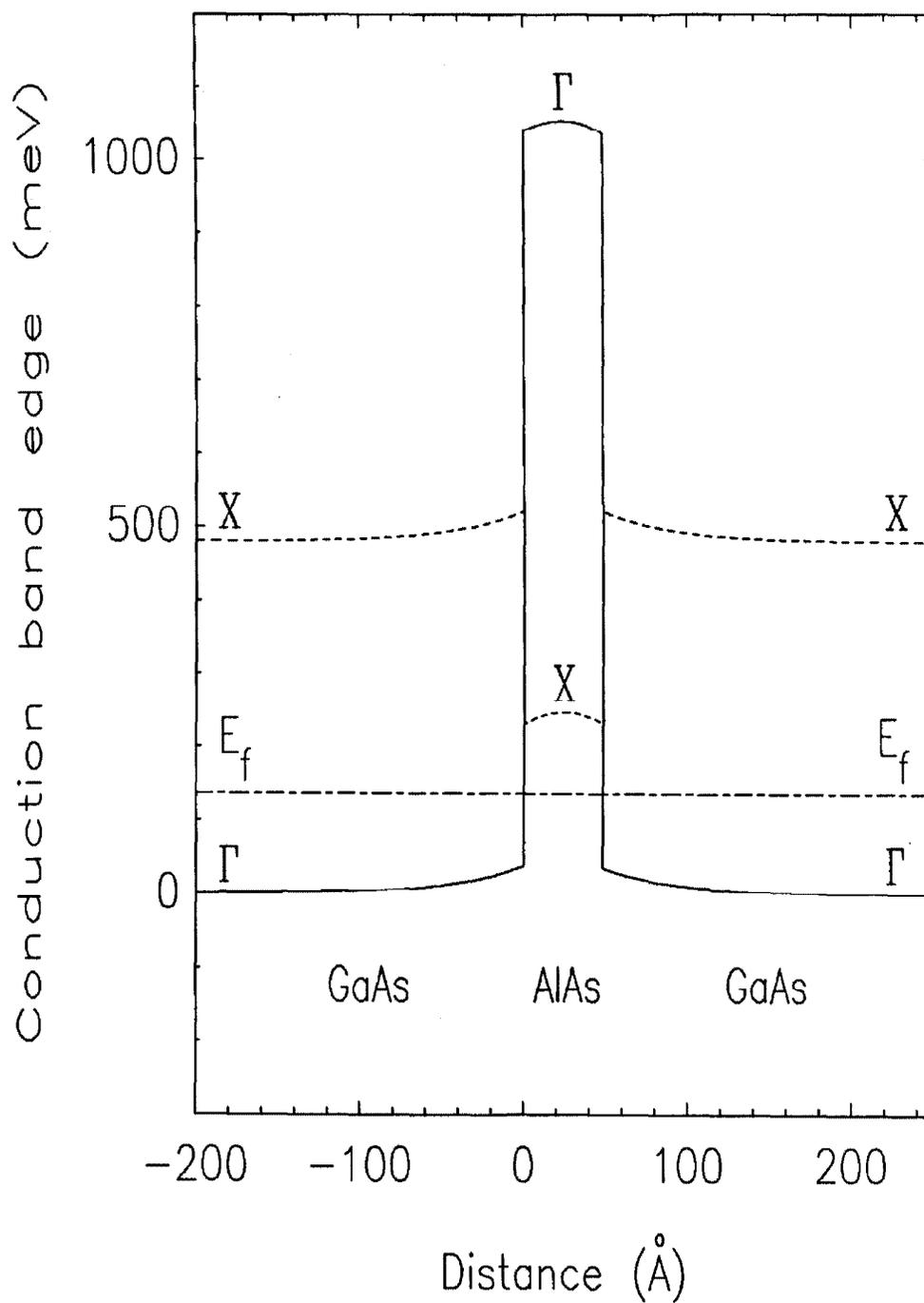


Figure 2.2: Calculated  $\Gamma$ - and X-point band edges in a single barrier GaAs/AlAs heterostructure at zero applied bias. The electrodes are doped  $n$ -type, with a carrier density of  $4 \times 10^{18} \text{ cm}^{-3}$ . The barrier is doped  $3 \times 10^{18} \text{ cm}^{-3}$ ,  $p$ -type.

Tunneling through the structure depicted in Fig. 2.2 can be treated as the parallel combination of tunneling through the AlAs  $\Gamma$ -point with tunneling through the AlAs X-point. Since the  $\Gamma$ -point is a local minimum for the AlAs conduction band which lies at  $k = 0$ , the two band  $k \cdot p$  method presented in section 2.2.2 is applicable to tunneling through the direct gap. Hence, the imaginary part of the electron wavefunction for  $\Gamma$ -point tunneling is given by Eqn. 2.58, with  $m_e^* = 0.15m$ . [10] For tunneling through the X-point, the one band formula is more appropriate because the conditions needed for the two band method are not satisfied. Furthermore, the tunneling electrons are much closer in energy to the X-point, making the one band formula a reasonable approximation. The imaginary part of the electron wavefunction for X-point tunneling can be obtained from Eqn. 2.33, with  $m_e^* = 0.78m$ , the longitudinal mass. [10]

Despite the low barrier height of the AlAs X-point, there are strong physical factors which enhance tunneling through the  $\Gamma$ -point. The large effective mass at the X-point leads to large values of  $K$  whenever the energies of the tunneling electrons are not very close to the conduction band edge. In fact, the value of  $K$  at the X-point becomes larger than the  $\Gamma$ -point value for energies more than  $\approx 100$  meV below the indirect conduction band minimum. Furthermore, the tunneling states in the GaAs electrodes lie near the GaAs  $\Gamma$ -point. Hence, their wavefunctions are considerably more like the  $\Gamma$ -states in AlAs than the X-states. The result is an enhancement of approximately  $10^4$  in the tunneling current through the AlAs  $\Gamma$ -point relative to the X-point. For these reasons, it has often been predicted theoretically that tunneling in GaAs/AlAs structures should be governed by the AlAs  $\Gamma$ -point. [12,13]

Figure 2.3 contains an experimental current density vs. voltage curve for the heterostructure represented in Fig. 2.2. Also presented is a theoretical curve, generated by the method outlined in section 2.2. The calculation only includes

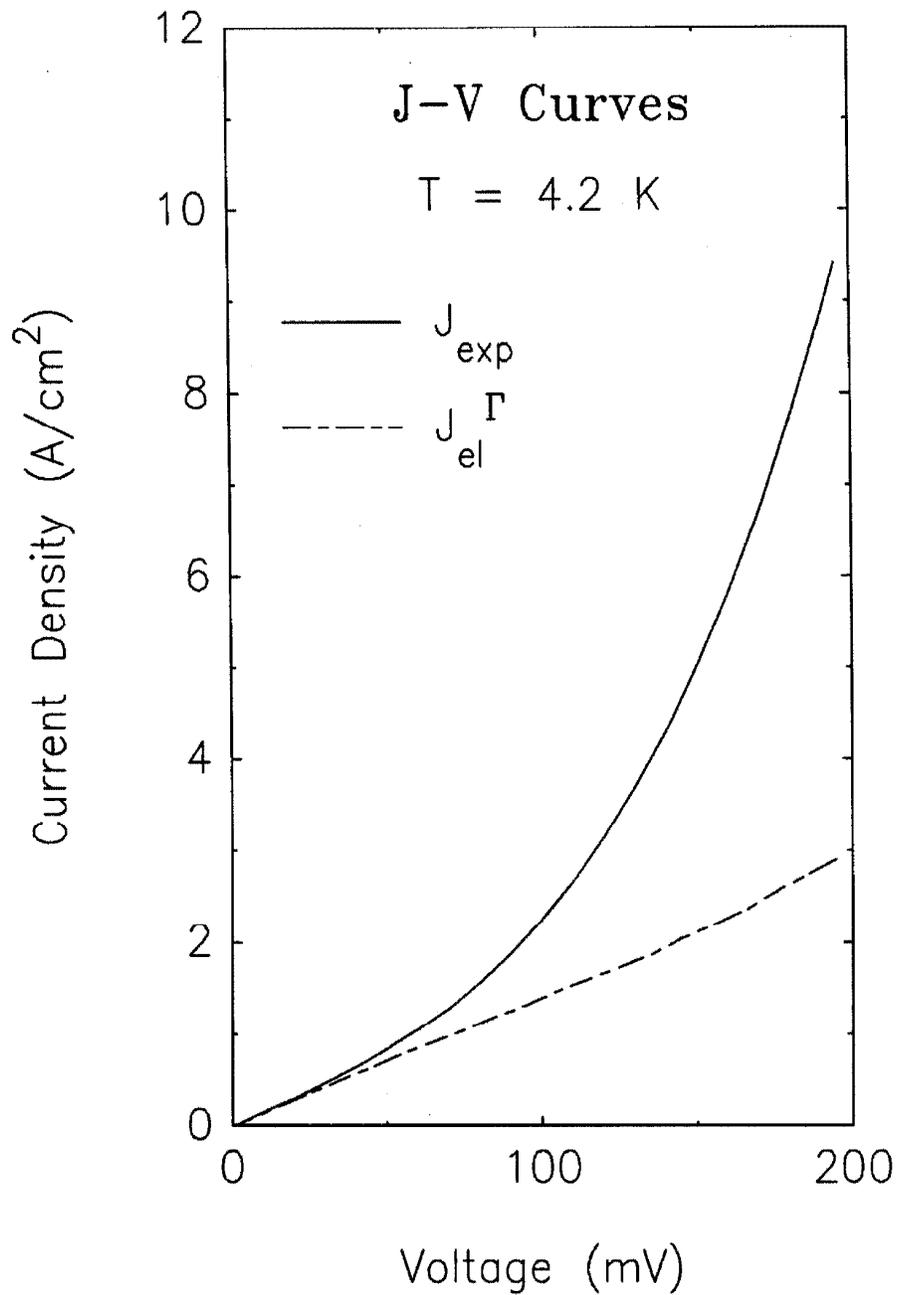


Figure 2.3: Experimental and theoretical current-voltage characteristics for the single barrier structure depicted in Fig. 2.2. The solid line corresponds to the experimental current density,  $J_{exp}$ . The dashed line is the calculated  $\Gamma$ -point elastic current density,  $J_{el}^{\Gamma}$ .

elastic tunneling through the AlAs  $\Gamma$ -point. Near zero bias, the agreement between the theoretical and experimental current densities is surprisingly good. However, it is likely that this agreement is at least somewhat fortuitous, given the uncertainties in experimental and theoretical parameters. The most notable characteristic of Fig. 2.3 is the qualitative and quantitative disagreement between the theoretical and experimental curves at larger voltages. The divergence of the two curves indicates that current transport mechanisms, other than simple elastic tunneling through the  $\Gamma$ -point, contribute to the total current. It has been suggested that these alternative transport mechanisms could be elastic and/or inelastic tunneling via the AlAs X- point.[1]

## 2.4 $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$ Negative Differential Resistance Devices

In this section, the current-voltage simulation developed earlier in the chapter is used to analyze  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  single barrier heterostructures theoretically. Emphasis is placed upon optimizing the predicted negative differential resistance behavior by maximizing current densities and peak-to-valley ratios. The effects of varying growth parameters, such as electrode composition, doping density, and barrier thickness, are studied. It is shown that careful choices of these parameters must be made in order to obtain NDR. Finally, changes in device behavior due to variations in the value of the HgTe-CdTe valence band offset,  $\Delta E_v$ , are explored. The tunneling current is found to depend strongly on  $\Delta E_v$ , both quantitatively and qualitatively. In fact, NDR disappears completely when the HgTe valence band edge is more than 100 meV above that of CdTe. A calculated band diagram for a typical  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  single barrier heterostructure is displayed in Fig. 2.4. It is assumed in the figure that  $\Delta E_v = 0$  eV.

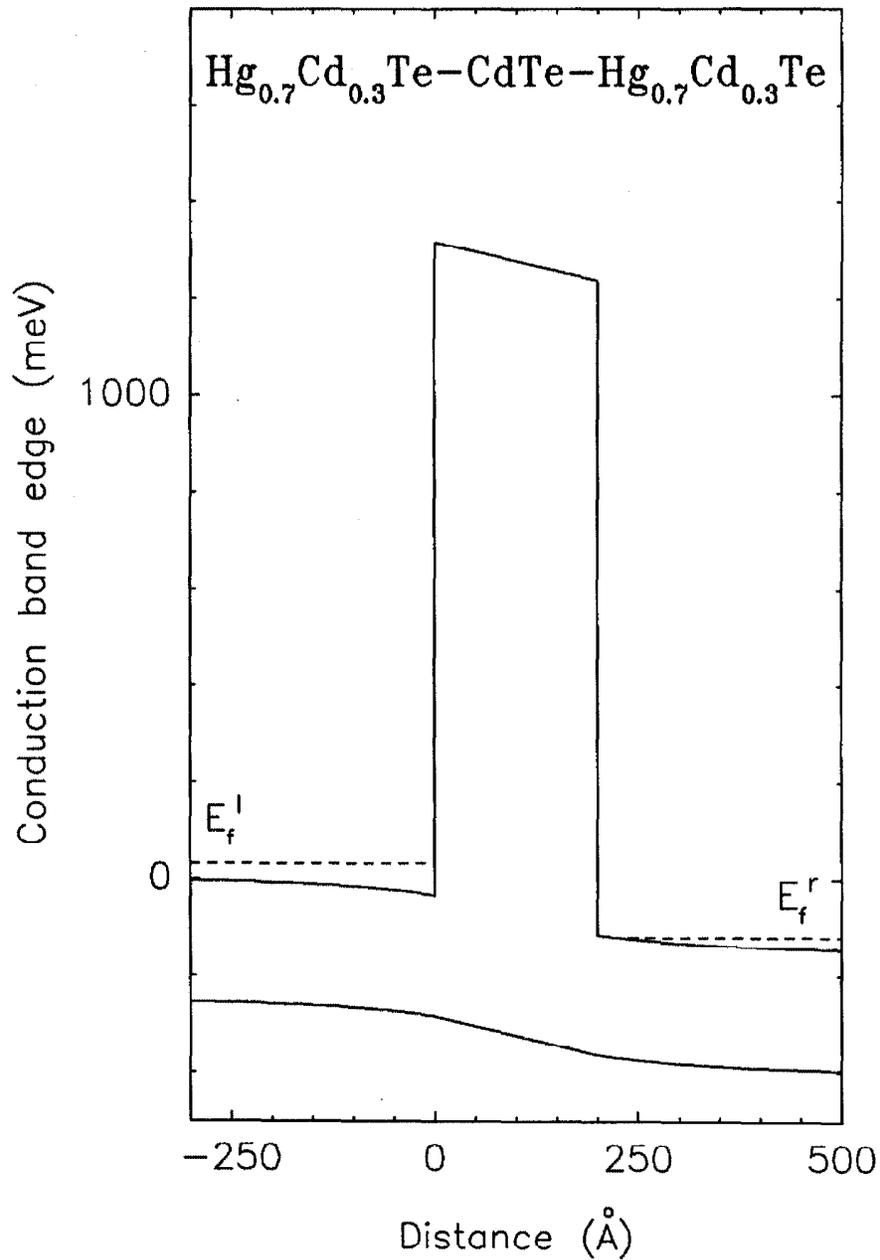


Figure 2.4: Calculated band diagram for a  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  single barrier heterostructure under an applied bias of 150 mV. Both the conduction and valence band edges are shown, along with the quasi-Fermi levels. The electrodes are  $\text{Hg}_{0.7}\text{Cd}_{0.3}\text{Te}$ , with  $n = 1 \times 10^{17} \text{ cm}^{-3}$ . The barrier is a 200 Å thick CdTe layer. The valence band offset is taken to be zero.

It should be noted that the calculations in this section are performed at 4.2 K. This choice is made because of the requirement for NDR that electron tunneling dominate the current through the heterostructure. At higher temperatures, thermionic mechanisms need to be considered. A treatment of thermionic hole currents in these structures is developed in chapter 3.

### 2.4.1 Growth Parameters

#### Electrode Composition

The alloy  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  is a highly unusual semiconductor. For  $x < 0.16$ , the energy gap is zero, with the conduction and heavy hole bands degenerate at  $k = 0$ .<sup>[8]</sup> This situation comes about because HgTe has an inverted band order, with the “conventional” \* conduction band having negative curvature in  $k$ -space and lying below the “conventional” light hole band, which has positive  $k$ -space curvature. The “conventional” light hole band then becomes the conduction band, degenerate with the heavy hole band as in most semiconductors. For values of  $x > 0.16$ ,  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  is a more traditional semiconductor with an energy gap which varies nearly linearly with  $x$  (there are quadratic corrections, but they are relatively small) over the range 0–1.6 eV:<sup>[8]</sup>

$$E_g(T = 4.2K) \approx (-0.3\text{eV}) + (1.9\text{eV})x \quad 0.16 < x < 1.0. \quad (2.59)$$

Examination of Fig. 2.4 reveals that, as the electrode band gap is widened, the energies of the tunneling electrons increase with respect to the valence band edge in the CdTe barrier. Hence, larger electrode energy gaps weaken the NDR effect, because the transmission coefficient changes most sharply for energies near the valence band edge of the barrier (see, for example, Fig. 2.1). It follows that small

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\* “Conventional” is taken to mean the band assignment in more standard semiconductors, such as GaAs and CdTe.

values of  $x$  are desirable for the  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  cladding layers. However, a nonzero energy gap in the electrodes is needed because filled states in the valence band of one electrode can tunnel across the barrier into empty states in the conduction band of the opposite electrode if the two bands overlap. In fact, valence to conduction band tunneling is allowed whenever the voltage applied to the structure becomes larger than the electrode band gap. Therefore, it is necessary to choose  $x$  such that the  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  energy gap is somewhat larger than the operating voltages for the structure. Typically, the optimal electrode energy gap is in the range 100 – 200 meV, corresponding to  $0.21 < x < 0.26$ . This range is quite narrow in terms of growth considerations.

### Barrier Composition

Due to the high vapor pressure of Hg at room temperature, MBE systems which grow  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  require special design features for the handling and removal of excess Hg. Despite these features, all CdTe layers grown in a  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  MBE system incorporate some Hg. Estimates of the minimum attainable background concentration vary from 5 to 15 percent.[5,20] The consequence of background Hg incorporation for the single barrier heterostructure is an alloying of the barrier layer. For uniform alloying, the energy gap of the barrier is in the range  $1.32 \text{ eV} < E_g^{\text{CdTe}} < 1.5 \text{ eV}$ , as compared to 1.6 eV for CdTe. In the single barrier NDR structure, most of the energy gap difference between the cladding layers and barrier is absorbed in the conduction band offset, with the valence band offset affected to a lesser degree by changes in barrier composition. Since device behavior is largely determined by the valence band offset, little qualitative change is seen in theoretical I-V curves generated for slightly alloyed barriers as compared to pure CdTe barriers. The overall current density is found to decrease somewhat due to a decrease in the effective mass used to calculate  $K$  in Eqn. 2.58.

## Electrode doping

The concentration of free carriers in the  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  electrodes plays an important role in determining the I-V behavior of the single barrier heterostructure. Two effects are involved. First, the amount of voltage dropped in the cladding layers as determined by band bending is strongly affected by the charge concentration in the electrodes. Since the NDR effect relies upon changing electron transmission coefficients by placing a voltage across the barrier, minimizing the voltage “lost” in bending the cladding layer bands is critical. The voltage lost in the cladding layers becomes larger as the electrode doping is decreased due to less effective screening of the electric field. Second, the peak of the I-V curve occurs when additional states are no longer added to the tunneling integral as the voltage is increased. This point is reached when the conduction band edge in the negatively biased electrode is raised to an energy equal to the quasi-Fermi level in the opposite electrode. For larger free carrier concentrations in the electrodes, the quasi-Fermi levels become larger, and the voltage required to reach the peak condition is increased. Low operating voltages in these structures are desirable because NDR disappears when the voltage surpasses the energy gap in the electrodes, as discussed previously. Thus, the two effects of electrode doping density work in opposite directions; low densities are better for low operating voltages, while high densities are better for dropping applied voltage in the barrier. Fig. 2.5 displays J-V curves for a single barrier structure, calculated by choosing three different electrode doping concentrations. All three curves were generated with the model developed in section 2.2, choosing a CdTe barrier thickness of 170 Å, zero valence band offset, and  $x = 0.22$  in the  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  electrodes. The best NDR performance is obtained for the middle value of electrode doping. As predicted, the peak of the curve calculated for higher carrier concentration is shifted to higher voltage. The weak NDR in the case of low electrode doping is due to large voltage drops in the cladding layers.

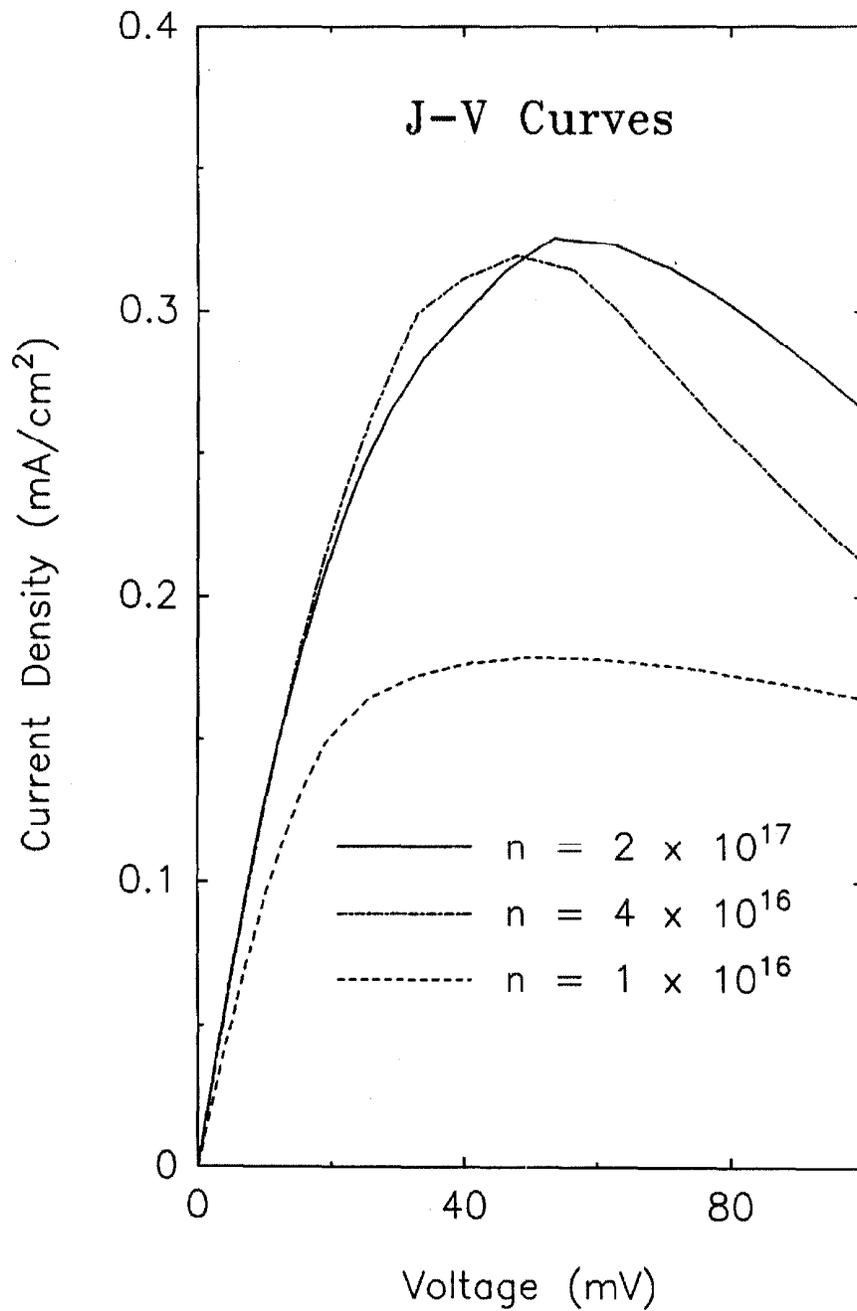


Figure 2.5: Current density vs. voltage for a  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  single barrier heterostructure with three different electrode doping densities. The electrode material is  $\text{Hg}_{0.78}\text{Cd}_{0.22}\text{Te}$ . The barrier is a 170 Å thick CdTe layer. The valence band offset is taken to be zero.

### Barrier Thickness

Figure 2.6 is a plot of the current density vs. barrier thickness for a single barrier structure with  $\text{Hg}_{0.78}\text{Cd}_{0.22}\text{Te}$  cladding layers and a CdTe barrier under an applied bias of 50 mV. The magnitude of the tunneling current in the  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  single barrier heterostructure is strongly dependent upon the thickness of the barrier layer. As is the case in many tunnel structures, this dependence arises from the exponential factor in the transmission coefficient (see Eqn. 2.32). In order to observe NDR, electron tunneling must dominate the current through the single barrier structure. Thin barriers are desirable because they enhance the tunneling current as compared to other currents, and yield higher operating current densities. However, two problems arise from barriers which are too thin. First, the strength of the NDR effect is directly related to the magnitude of the exponential factor:

$$\exp\left(-2 \int_0^w K dx\right). \quad (2.60)$$

As the barrier becomes thinner, the effect of increasing  $K$  values as the energies of the tunneling electrons increase is reduced. As a result, smaller peak-to-valley current ratios are observed, or NDR is lost completely. Second, the amount of voltage dropped in the barrier decreases as the barrier thickness decreases because the increased electric fields require more band bending in the electrodes. As discussed previously, large cladding layer voltage drops can weaken or eliminate NDR. Clearly, barrier thicknesses can be too small or too large for the single barrier heterostructure to yield NDR. However, optimal barrier thicknesses are difficult to quantify because competing current transport mechanisms are not well understood.

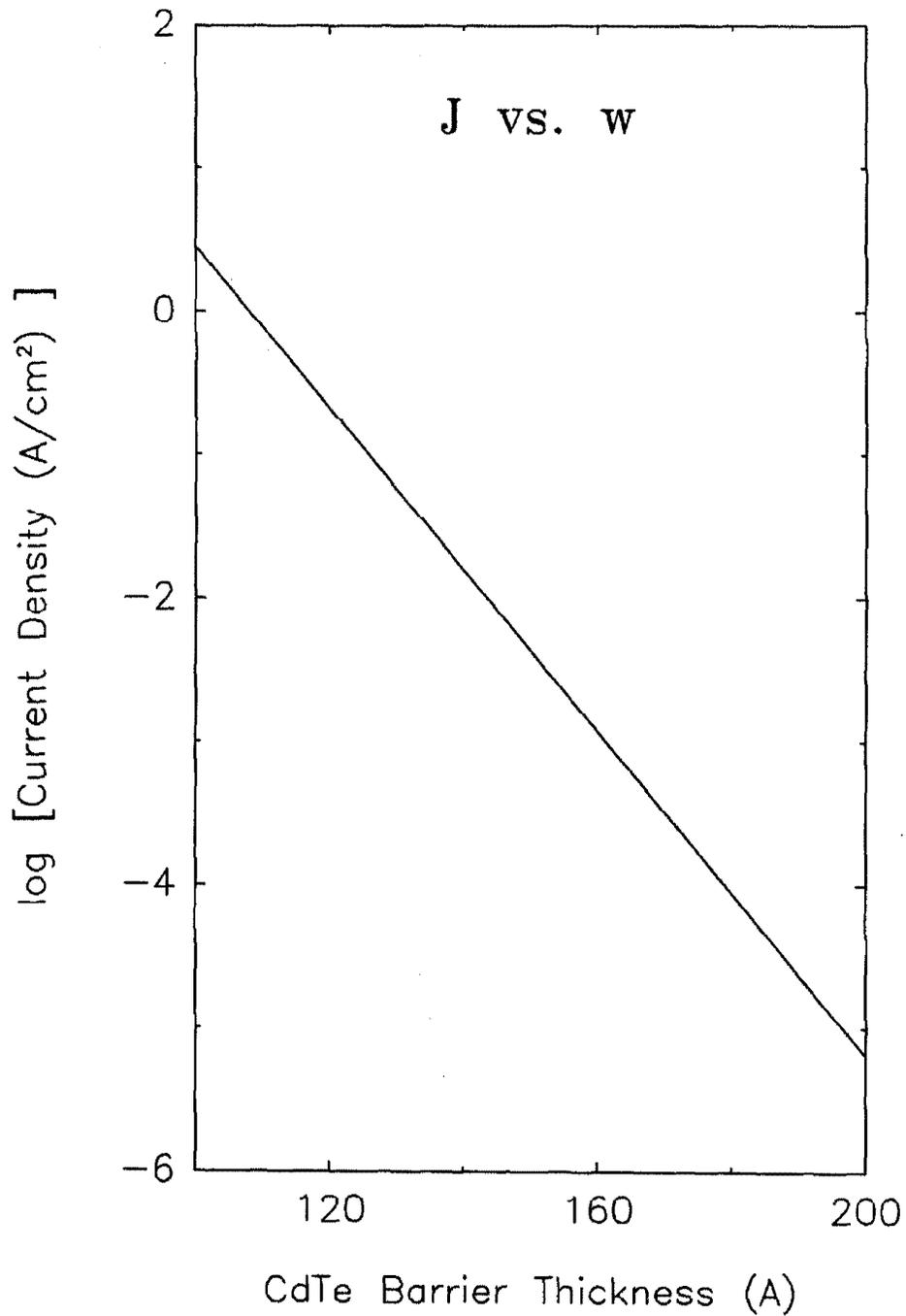


Figure 2.6: Log of the current density through a  $\text{Hg}_{0.78}\text{Cd}_{0.22}\text{Te}/\text{CdTe}$  heterostructure vs. the CdTe layer thickness. The electrode doping density is  $4 \times 10^{16} \text{ cm}^{-3}$ . The applied bias is 50 mV.

## 2.4.2 Effects of Valence Band Offsets on NDR

In contrast to most of the growth parameters discussed in the previous section, the effect of the valence band offset,  $\Delta E_v$ , on NDR from the  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  single barrier heterostructure is monotonic.<sup>†</sup> Smaller values of  $\Delta E_v$  yield significantly better NDR than larger values. Figs. 2.7 (a) and (b) contain linear and log current density vs. voltage plots for several choices of  $\Delta E_v$  in a single barrier  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  heterostructure. The linear plots demonstrate that peak-to-valley current ratios and total current densities are strongly reduced as the valence band offset is increased. In fact, NDR disappears altogether for  $\Delta E_v > 100$  meV. The log plots quantify the drop in current density at higher  $\Delta E_v$ 's. As the valence band offset is increased, the conduction band edges in the  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  electrodes are moved up in energy with respect to the barrier. The drop in current density is due to the increasing values of  $K$  seen by tunneling electrons at energies further away from the valence band edge in the barrier. The reduction in peak-to-valley current ratios is a result of the gentler slope of  $K$  with energy at higher energies in the barrier.

## 2.5 Other Material Combinations for Single Barrier NDR

A few material combinations other than  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$ -CdTe are possible candidates for single barrier NDR. In this section, two of these heterostructures are analyzed conceptually and theoretically. A second demonstration of single barrier NDR has recently been made in one of these material combinations, InAs- $\text{Ga}_{1-x}\text{Al}_x\text{Sb}$ .<sup>[1]</sup>

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<sup>†</sup>It is relatively certain that  $\Delta E_v$  is not extremely negative, i.e., the HgTe valence band edge is not well below the CdTe valence band edge.

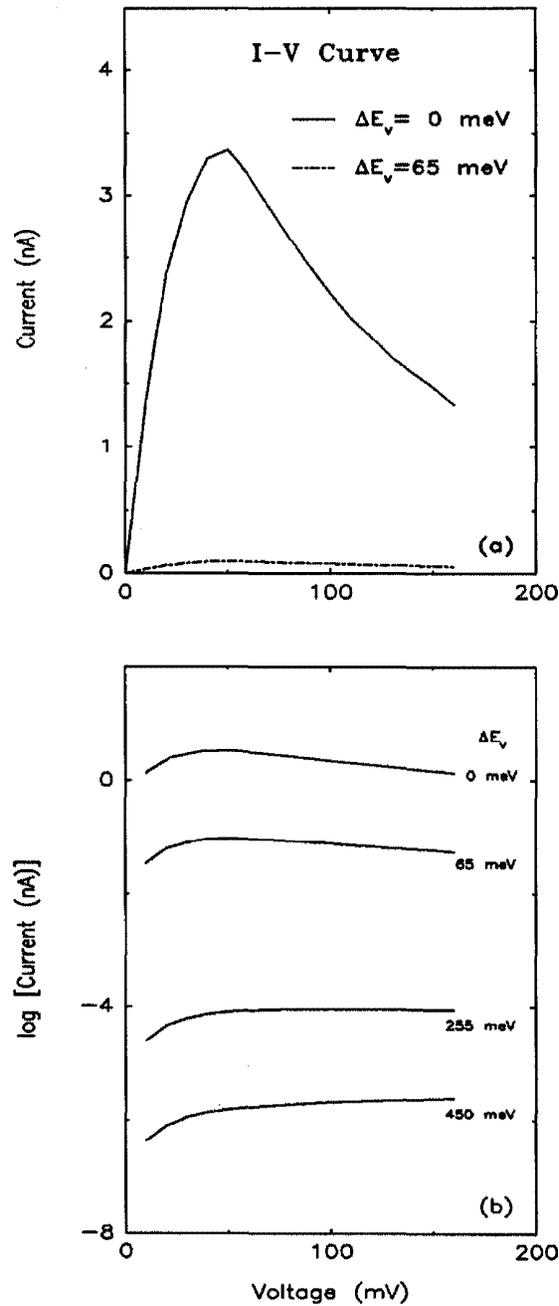


Figure 2.7: Linear (a) and log (b) plots of the current density vs. voltage behavior calculated for a single barrier  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  heterostructure. Curves for several values of  $\Delta E_v$  are plotted. The electrodes have  $x = 0.22$ , and an electron concentration of  $4 \times 10^{16} \text{ cm}^{-3}$ . The barrier is a 170 Å thick CdTe layer.

### 2.5.1 InAs–Ga<sub>1-x</sub>Al<sub>x</sub>Sb Single Barrier Heterostructures

InAs–GaSb heterostructures have been of interest for some time.[18] However, considerably less experimental literature exists for this system than GaAs/AlAs, largely because growth techniques for the antimonides have lagged behind the those for the arsenides. The most unique feature of the InAs–GaSb heterojunction is a completely staggered band alignment. Recent x-ray photoemission measurements have placed the valence band offset between the two materials ( $E_v^{GaSb} - E_v^{InAs}$ ) at 0.51 eV.[19] Since the InAs energy gap is only 0.35 eV at 300 K, the InAs conduction band minimum lies *below* the GaSb valence band maximum by 0.16 eV. Thus, InAs–GaSb tunnel structures have no barriers, since neither material can have free carriers which lie at energies in the forbidden gap of the other.

The semiconductor AlSb has a large indirect energy gap, with a “normal” type I band alignment against GaSb. X-ray photoemission experiments have yielded a valence band offset ( $E_v^{GaSb} - E_v^{AlSb}$ ) of 0.40 eV.[17] Assuming a linear variation of the Ga<sub>1-x</sub>Al<sub>x</sub>Sb valence band edge with  $x$ , it is possible to deduce a relation for the InAs–Ga<sub>1-x</sub>Al<sub>x</sub>Sb valence band offset:

$$E_v^{InAs} \approx E_v^{GaAlSb} - (0.51\text{eV}) + (0.40\text{eV})x. \quad (2.61)$$

For single barrier NDR structures, device behavior is optimized when the conduction band edge in the electrodes is nearly aligned with the valence band edge in the barrier. For an InAs–Ga<sub>1-x</sub>Al<sub>x</sub>Sb–InAs heterostructure, this alignment can be obtained by choosing:

$$x \approx \frac{0.51\text{eV} - 0.35\text{eV}}{0.40\text{eV}} = 0.4. \quad (2.62)$$

A calculated band diagram for a single barrier structure with  $x = 0.45$  in the Ga<sub>1-x</sub>Al<sub>x</sub>Sb layer is given in Fig. 2.8. In the diagram, the InAs conduction band edge lies 20 meV above the Ga<sub>1-x</sub>Al<sub>x</sub>Sb valence band edge.

This material combination has several advantages over Hg<sub>1-x</sub>Cd<sub>x</sub>Te for single

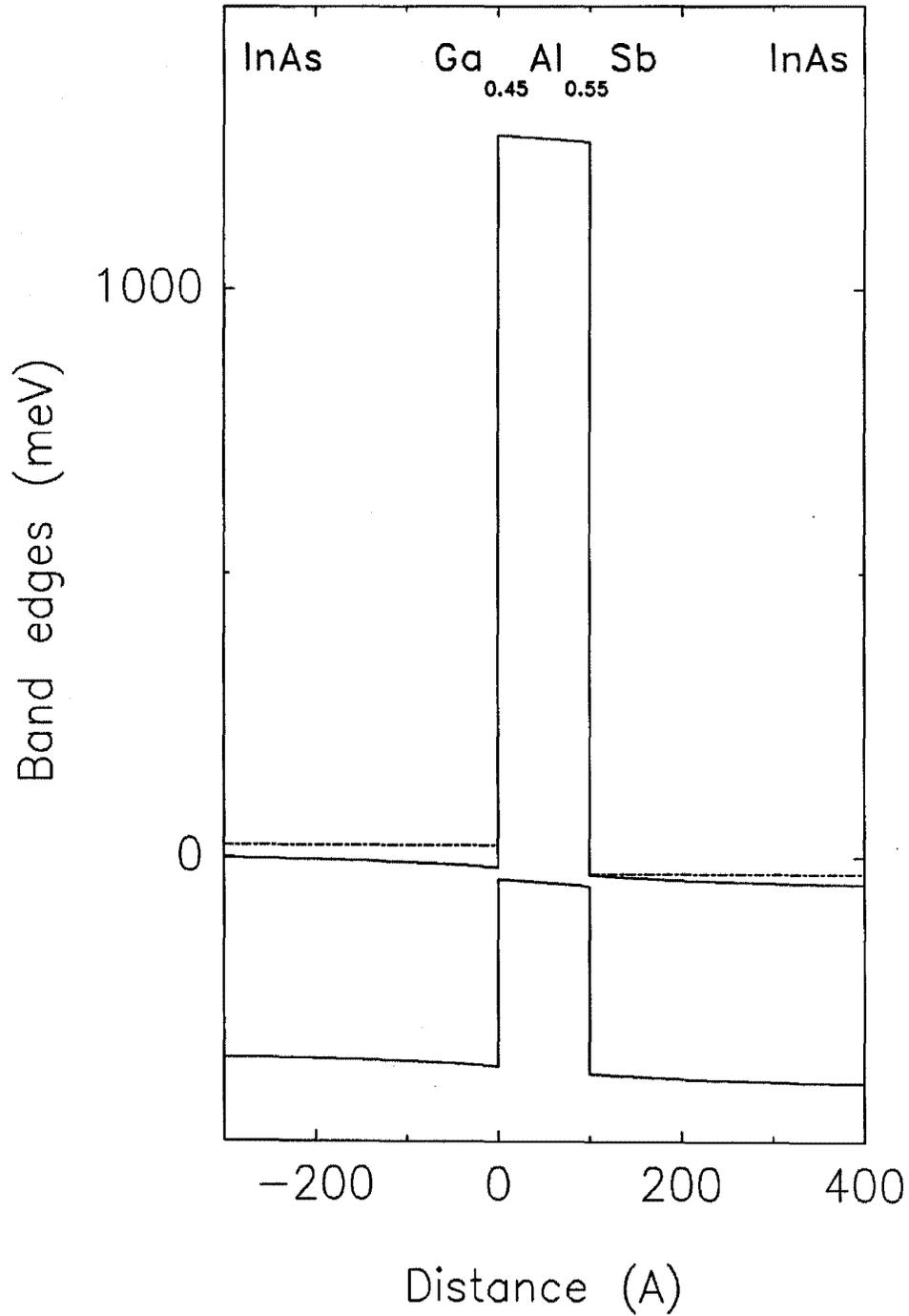


Figure 2.8: Calculated valence and conduction band edges for an InAs-Ga<sub>0.45</sub>Al<sub>0.55</sub>Sb-InAs heterostructure under an applied bias of 50 mV. The electrode doping density is taken to be  $5 \times 10^{18} \text{cm}^{-3}$ .

barrier NDR structures. (i) The ability to tune the position of the valence band in the barrier by varying the Al mole fraction provides a degree of freedom which does not exist for  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  structures. (ii) Assuming that the band offsets given above are correct, it is possible to position the tunneling electrons very close in energy to the valence band maximum in the barrier. (iii) III-V semiconductors are better for device fabrication and are more stable than  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$ . (iv) Thermionic hole currents in this system are limited by the InAs energy gap, which is significantly larger than that of  $\text{Hg}_{0.78}\text{Cd}_{0.22}\text{Te}$ . Thus, room temperature operation may be possible. A calculated J-V curve for a single barrier InAs/ $\text{Ga}_{0.55}\text{Al}_{0.45}\text{Sb}$  structure with a 100 Å thick barrier layer is displayed in Fig. 2.9.

### 2.5.2 $\text{Pb}_{1-x}\text{Sn}_x\text{Te}$ Single Barrier Heterostructures

The ternary semiconductor  $\text{Pb}_{1-x}\text{Sn}_x\text{Te}$  has an extremely narrow energy gap,  $E_g$ , over the entire composition range:[21]

$$E_g(T = 12K) \approx \begin{cases} 0.19 + 0.54x & x < 0.35 \\ 0 & x > 0.35. \end{cases} \quad (2.63)$$

It has been proposed by Heremans et al.[22] that single barrier NDR could be observed in a heterostructure fabricated from different compositions of this material. This argument is based upon the pinning of the Fermi level in these materials by the addition of indium doping during growth. It is assumed that the bands in the electrodes and barrier will strongly screen electric fields, resulting in the bulk (pinned) alignments of the bands. Thus, band offsets are ignored. In fact, it is proposed that the barrier should have  $x = 0.3$ , with the electrodes having  $x = 0.2$ , i.e., the electrode energy gap is *larger* than that of the barrier. This choice is made because the Fermi level in bulk, indium doped  $\text{Pb}_{1-x}\text{Sn}_x\text{Te}$  rises strongly with increasing Pb content, so that it rests in the conduction band for  $x = 0.2$ , and near the valence band edge for  $x = 0.3$ . Alignment of the Fermi level across the entire

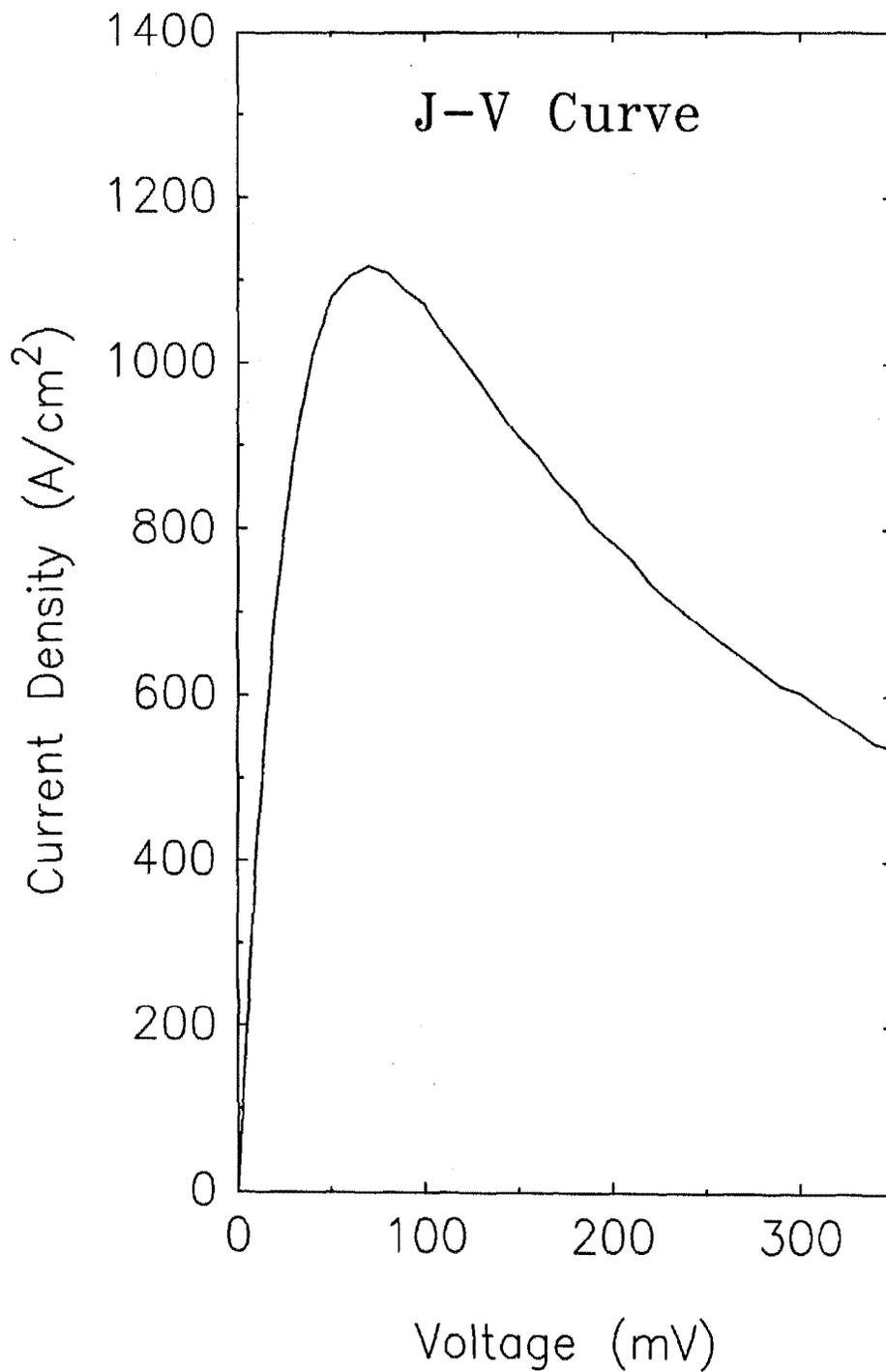


Figure 2.9: Calculated current density vs. voltage curve for the single barrier structure depicted in Fig. 2.8.

heterostructure results in the required single barrier NDR band alignment, with the conduction band in the  $\text{Pb}_{0.8}\text{Sn}_{0.2}\text{Te}$  electrodes lying slightly higher in energy than the valence band in the  $\text{Pb}_{0.7}\text{Sn}_{0.3}\text{Te}$  barrier.

Several conceptual and practical problems make it unlikely that the  $\text{Pb}_{1-x}\text{Sn}_x\text{Te}$  single barrier device will show NDR. First, a physically correct view of the band diagram (accounting for band offsets) will shift the band alignment away from the desired configuration. Furthermore, including band bending effects weakens predicted NDR behavior significantly. Second, the energy gap in the barrier is only 30 meV. Hence, extremely thick barriers are needed to produce any attenuation of the tunneling electrons, and voltages larger than 30 mV push the tunneling electrons to energies higher than midgap of the barrier. Third, the extremely narrow energy gaps lead to large competing thermionic currents. Finally, the addition of indium doping in the barrier is likely to introduce scattering centers, substantially reducing the probability of elastic tunneling across the thick barrier layer.

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## Chapter 3

# Electrical Studies of $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$ Single Barrier Heterostructures

### 3.1 Introduction

#### 3.1.1 Motivation and Background

This chapter presents results from an experimental study of the current-voltage (I-V) behavior of single barrier  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  heterostructures. The original intent in undertaking this study was to demonstrate the novel single barrier negative differential resistance (NDR) mechanism described in section 1.5. The motivation for developing single barrier NDR structures is to obtain electrical devices which can operate at extremely high frequencies. In these applications, the NDR feature can be exploited in designing oscillators, amplifiers, and mixers. Furthermore, single barrier heterostructures may have better high-frequency response than double barrier (resonant tunneling) devices, in which a quantum well must be charged and discharged during high speed switching. Further motivation for studying the particular choice of  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  single barrier devices is derived from current interest in heterostructures containing  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$ . The ternary compound  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$

has been a far-infrared detector material of choice because of its tunable narrow energy gap.[1] More recently, a great deal of attention has been focused upon the high quality layered growth of HgTe, CdTe, and  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$ , largely due to the potential applications of the HgTe–CdTe superlattice as an infrared material.[2,3,4,5] Another device of interest is the double barrier HgTe/CdTe heterostructure, from which room temperature NDR has been demonstrated.[6,7] Electrical studies of single barrier heterostructures can provide fairly direct measurements of material and heterojunction properties, such as barrier penetration distances and band offsets. Detailed knowledge of these properties can facilitate the design of more elaborate heterostructure devices.

Published theoretical and experimental values of the HgTe/CdTe valence band offset ( $\Delta E_v$ ) range from 0 to 500 meV.[9,10,11,12,13,14,15,16,15,18] A few explanations can be suggested for the disagreement between the various experimental measurements. Firstly, many of the experimental techniques measure the band offset in an indirect fashion. For example, most of the measurements on superlattice samples rely on superlattice bandstructure calculations to determine the band offset. Secondly, many of the experiments are performed under different conditions (e.g., different temperatures). Finally, growth techniques for  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  are not yet reproducible enough to be certain that samples grown in different places and/or times are of comparable quality. Many of the current transport mechanisms in single barrier heterostructures are strongly dependent on the valence band offset. In the case of the  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  structures studied here, thermionic hole currents have a direct exponential dependence on  $(\Delta E_v/kT)$ . At high temperatures this thermionic mechanism can dominate transport, yielding a fairly direct measurement of  $\Delta E_v$ . When conditions are such that elastic electron tunneling dominates the current, the theoretical simulations of section 2.4 show that NDR can be observed only if  $\Delta E_v$  is less than 100 meV. Hence, the successful demonstration of

NDR places an upper limit on ( $\Delta E_v$ ).

### 3.1.2 Summary of Results

NDR has been observed from a single barrier  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  heterostructure at temperatures accessible with liquid helium, but not at higher temperatures. Due to the extremely tedious nature of the low temperature bonding technique used here, only a few devices were studied, with roughly half displaying NDR. The best device yielded a peak-to-valley current ratio of 2:1, with a peak current density of  $0.51 \text{ mA/cm}^{-2}$ . The strongly temperature dependent behavior is probably attributable to competing current transport mechanisms which freeze out at extremely low temperatures. It is possible that a temperature dependent valence band offset also plays a role in restricting NDR to low temperature I-V curves. The observation of NDR places an upper limit of 100 meV on  $\Delta E_v$  at 4.2 K. The demonstration of NDR in this material system verifies the predicted single barrier NDR mechanism. It is possible that other material combinations could yield room temperature NDR and better device performance.

The theoretical analysis of  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  structures given in section 2.4 indicates that stringent selection of growth parameters is a requirement for achieving single barrier NDR in this material system. Thus, the successful demonstration of NDR is indicative of a relatively controllable and reproducible growth technique. Furthermore, reasonable material quality is indicated by these results, because crystal defects and impurities tend to provide transport paths which can compete with or dominate elastic tunneling.

At higher temperatures ( $>80 \text{ K}$ ), a more detailed investigation of I-V behavior was made. Two  $\text{HgTe/CdTe}$  single barrier samples were studied in addition to the  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  sample which displayed NDR at low temperatures. Measured currents were found to vary linearly with device area in all three samples, indicating

the absence of surface leakage currents. Over the temperature range 190–300 K, the observed current is attributed to the sum of two transport mechanisms: (i) thermionic emission of holes across the barrier layer, and (ii) holes tunneling across a “triangular-shaped” barrier. This interpretation of the current is supported by good agreement between observed current–voltage curves and theoretical simulations which include only these two mechanisms. The dependence of the measured current with temperature was then used to determine  $\Delta E_v$ . Results from the three samples at 300 K yielded values of  $\Delta E_v$  between  $290 \pm 50$  and  $390 \pm 75$  meV. In all three samples, data taken over the range 190–300 K are consistent with a valence band offset which decreases at lower temperatures.

Several other  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  single barrier samples were grown for this study. Most of them displayed reproducible I–V behavior, with measured currents varying linearly with device area. However, the CdTe barriers in these samples were considerably thinner than in the three samples discussed above. The effect of thin barriers is to enhance elastic and inelastic tunneling currents while leaving thermionic currents unchanged. The measured currents in these samples could not be attributed to the thermionic hole mechanism at high temperatures. Therefore, the data from these samples were not used to determine  $\Delta E_v$ . Current–voltage experiments at liquid helium temperatures were not attempted in these samples.

### 3.1.3 Outline of Chapter

A description of the samples grown for the  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  single barrier study is given in section 3.2. Section 3.3 describes the experiment used to demonstrate NDR at liquid helium temperatures. I–V data from a few devices are presented, including two curves taken at different temperatures from a single device. Higher temperature current–voltage behavior from three single barrier structures is investigated in section 3.4. A straightforward theoretical model of thermionic and

tunneling hole currents is developed and used to analyze the I-V data. The HgTe-CdTe valence band offset is then determined over the temperature range 190–300 K. Section 3.5 gives brief descriptions of the electrical behavior observed from other samples grown for this study. Finally, conclusions are summarized in section 3.6.

## 3.2 Samples

Table 3.1 contains a listing of the single barrier  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  heterostructures grown for this study by molecular beam epitaxy (MBE). The majority of the samples (TS1 through TS16) were grown at the University of Illinois at Chicago (UIC) by I.K. Sou and J.P. Faurie. Three additional samples (ML26 A, A', B) were provided by F.A. Shirland and O.K. Wu at Hughes Research Laboratories (HRL) in Malibu, California.

Semi-insulating GaAs was used as a substrate material for the samples grown at UIC. Growth commenced with a thick CdTe buffer layer ( $\approx 3 \mu\text{m}$ ), which provided a high quality, lattice-matched template for growth of the first  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  electrode.\* High resolution transmission electron microscope (TEM) pictures of the GaAs/CdTe interface indicate that an amorphous CdTe layer forms initially on the GaAs (100) surface. After the first few hundred angstroms of growth, highly crystalline (111)-oriented CdTe is nucleated and maintained for the remainder of the layer. A typical high resolution TEM print of this interface is shown in Fig. 3.1. Following the CdTe buffer, a thick  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  layer was grown to form the bottom electrode of the heterostructure. This layer was usually doped *n*-type with indium, although defect doping was attempted in a few samples (TS1, TS3, TS5). A thin CdTe layer was then deposited to form the single quantum barrier. Due to the constant Hg overpressure in MBE systems which grow  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$ , the

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\*The lattice constant of CdTe (6.481 Å) is nearly identical to that of HgTe (6.462 Å).[8]

Growth Parameters for  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  Single Barrier Samples

Sample No.	Electrode $x$	Bottom Electrode		CdTe Barrier Width ( $\text{\AA}$ )	Top Electrode	
		Thick-ness ( $\mu\text{m}$ )	Doping ( $10^{16}\text{cm}^{-3}$ )		Thick-ness ( $\mu\text{m}$ )	Doping ( $10^{16}\text{cm}^{-3}$ )
TS1	0.20	3.0	p - 0.45	100	0.5	p - 0.45
TS2	0.23	3.0	2.25	100	0.5	2.25
TS3	0.20	2.6	0.08	86	0.43	0.08
TS4	0.22	3.0	3.57	100	0.5	3.57
TS5	0.22	2.6	p - 0.01	80	0.46	p - 0.01
TS6	0.22	3.0	3.58	150	0.5	3.58
TS7	0.33	2.59	80.	80	0.44	80.
TS8	0.32	3.17	50.	80	0.51	50.
TS9	0.295	3.3	40.	80	0.59	40.
TS10	0.315	2.84	?	80	0.46	?
TS11	0.33	3.26	60.	70	0.53	100.
TS12	0.21	2.82	2.0	80	0.46	4.0
TS13	0.235	3.15	6.0	80	0.52	8.0
TS14	0.27	2.45	20.	80	0.41	50.
TS15	0.30	2.66	20.	70	0.44	100.
TS16	0.31	2.73	20.	80	0.46	100.
ML26A	0.0	1.0	60.	180	0.5	60.
ML26A'	0.0	1.0	60.	180	0.5	60.
ML26B	0.0	1.0	60.	180	0.5	60.

Table 3.1: Table of growth information for  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  single barrier samples. Samples TS1-TS16 were grown at the University of Illinois at Chicago on GaAs (100) substrates. Samples ML26 A, A', B were grown at Hughes Research Laboratories on CdTe (111), CdZnTe (111), and CdTe (100), respectively. All doping densities are  $n$ -type, unless otherwise noted with a 'p'. Carrier concentrations for the samples grown at UIC (HRL) were measured at 30 K (300 K). All CdTe layers are nominally undoped.



Figure 3.1: High resolution transmission electron microscope photograph of the GaAs(100)/CdTe(111) interface.

barrier layer is alloyed to some extent. The actual composition is estimated to be  $\text{Hg}_{0.05}\text{Cd}_{0.95}\text{Te}$ . [19] Finally, an  $n$ -type  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  top electrode was grown, with a layer thickness of  $\approx 0.5 \mu\text{m}$ .

The three samples from HRL were grown on three different substrates:  $\text{CdTe}(100)$ ,  $\text{CdTe}(111)$ , and  $\text{Cd}_{0.5}\text{Zn}_{0.5}\text{Te}(111)$ . A thick  $\text{CdTe}$  buffer layer ( $\approx 3 \mu\text{m}$ ) was grown on each of these substrates prior to the growth of the single barrier heterostructure. In contrast to the samples grown at UIC, the intent in designing these samples was solely to determine  $\Delta E_v$  by measuring thermionic hole currents across the single barrier (i.e., NDR was not sought from these samples). This shift in focus resulted in a choice of pure  $\text{HgTe}$  as the electrode material instead of a narrow gap  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  alloy. The advantage in using  $\text{HgTe}$  is to simplify the analysis of the measured thermionic hole current. In addition, the  $\text{CdTe}$  barriers in the samples grown at HRL were made thicker to suppress elastic and inelastic tunneling mechanisms. Hg incorporation in the barriers of these samples is estimated to reduce their composition to  $\text{Hg}_{0.15}\text{Cd}_{0.85}\text{Te}$ . [20]

### 3.3 Demonstration of NDR at Low Temperatures

#### 3.3.1 Sample TS6

Upon including band bending effects in the current-voltage simulations developed in section 2.2, sample TS6 was found to be the only sample from which strong NDR could be expected. Thus, major efforts were concentrated on TS6 in this study. Several TEM runs were performed on this sample in addition to over 10 preparations for electrical measurements. Sample TS6 was the only sample studied at liquid helium temperatures.

The major difference between TS6 and the other samples grown at UIC is the thickness of its barrier layer. In table 3.1, this width is listed as 150 Å, which is the thickness estimated from growth rate calibrations. All of the other samples are estimated to have barrier layers of 100 Å or less. As discussed in section 2.4, thicker barriers allow less of the total applied bias to be lost in bending the cladding layers. Furthermore, peak-to-valley current ratios rise dramatically with thicker barriers because the exponential factor in the electron transmission coefficient becomes more heavily weighted. The disadvantages of thicker barriers are the reduction of the peak current density and the increased role of competing transport mechanisms. These competing currents are often more strongly temperature dependent than elastic tunneling. Hence, low temperature measurements are often used to observe tunneling effects while freezing out other mechanisms. Extremely low temperatures were needed to observe NDR in sample TS6 ( $< 20$  K).

### 3.3.2 Device Fabrication

To study current-voltage behavior in a semiconductor heterostructure, it is almost always necessary to electrically isolate small areas of the sample. Isolation is usually accomplished by forming mesas in the sample. The mesa heights are selected to be greater than the film thickness from the sample surface to the active portion of the structure. This approach has several benefits. (i) Sample nonuniformities, such as large crystal defects, can cause an electrical device to become short circuited. If sufficiently small mesa areas can be achieved, these nonuniformities can be excluded from a large number of the mesas. (ii) Operating currents are reduced by smaller device areas, lessening the detrimental effects of parasitic series resistance sources (such as contacting wires and measurement circuitry). (iii) Fabricating a large number of small devices on a single sample, instead of a few very large devices, allows a more extensive study of electrical behavior. (iv) For samples

in which electrical contact cannot be made to the substrate, the bottom electrode can only be contacted by removing the active region of the heterostructure over a portion of the sample area.

The result of the device fabrication process is depicted schematically in Fig. 3.2. The figure shows the side view of a single mesa along with contacts to the top and bottom electrodes. The following list is the procedure used to fabricate two terminal devices in sample TS6.

1. A small piece ( $\approx 3 \text{ mm} \times 4 \text{ mm}$ ) of the sample is selected by cleaving with a Circon microscribe. In the remainder of the procedure list, this small piece is referred to as the 'sample'.
2. The sample is cleaned by successive immersion in acetone, methanol, and deionized water for 1 minute each. The water is then blown off with dry nitrogen.
3. Positive photoresist (Shipley AZ 5214) is spun onto the sample. Photolithographic procedures are then used to expose and develop the photoresist film. The result is an array of circular photoresist dots, with varying diameters ranging from 35 to 70  $\mu\text{m}$ .
4. Mesas are fabricated in the sample by wet etching with  $\text{Br}_2:\text{HBr}:\text{H}_2\text{O}$  in a 0.005:1:3 ratio by volume. The etch rate is approximately 0.4  $\mu\text{m}/\text{min}$ . This chemical etch permits the use of conventional positive photoresist in photolithographic procedures, as opposed to the more commonly used  $\text{Br}_2$ :methanol which attacks most positive resists. The etch leaves a surface which is somewhat less smooth than the unetched surface. The photoresist circles are then removed with acetone. Etching depths are checked with a stylus profilometer.

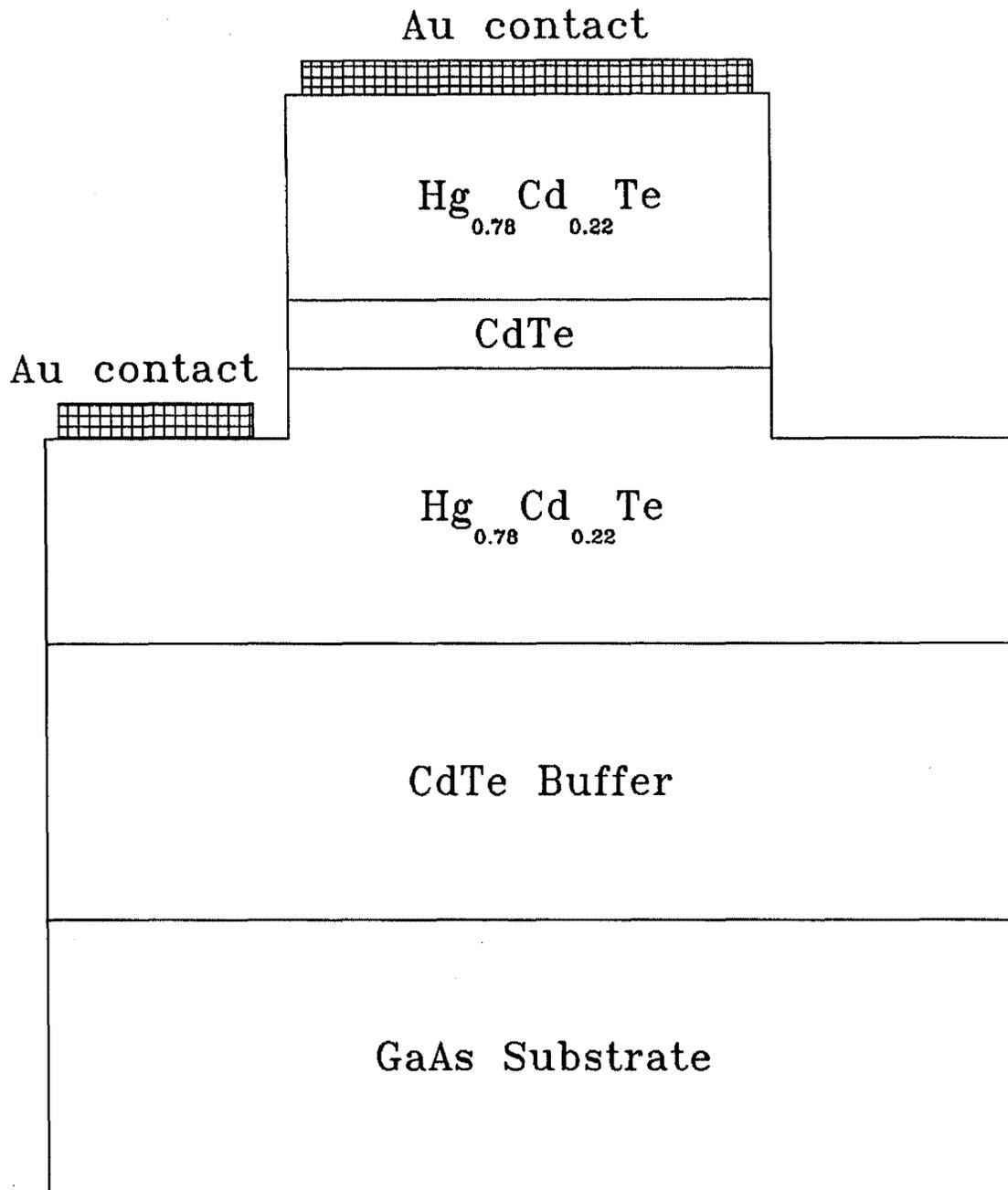


Figure 3.2: Schematic diagram depicting the result of the device fabrication process for sample TS6. The diagram shows the side view of a single mesa along with Au contacts to the top and bottom  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  cladding layers.

5. A second coating of photoresist is spun onto the sample, exposed, and developed. The second mask is inverted with respect to the first mask, and has slightly smaller circular features. Holes result in the photoresist film; they are aligned with the tops of the mesas.
6. A gold film is evaporated over the entire sample. The sample is then immersed in acetone and exposed to an ultrasonic cleaner. As a result, the gold film is lifted off of the sample everywhere except for on top of the mesas, forming a contact to the top electrode. This contact was found to be ohmic by probing circular gold dots on an unetched sample.
7. A contact to the bottom electrode is made by evaporating gold on the sample near one end only. The series resistance which arises due to electrons traveling laterally through the bottom  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  layer was found to be negligible by comparing devices which were different distances away from the gold 'back' contact.

Room temperature electrical tests of fabricated devices in sample TS6 have been made by probing the mesas with a 25  $\mu\text{m}$  diameter gold wire. Fig. 3.3 is a log-log plot of the current at 300 K vs. mesa diameter for a typical preparation of sample TS6. The data were obtained at an applied bias of 25 mV. Although the spread of measured currents is fairly large, the slope of the best fit line to the data in Fig. 3.3 is nearly 2, indicating that the current varies linearly with device area. This condition verifies that surface leakage currents and/or isolated defects do not dominate current transport in the fabricated devices. Roughly 25% of the devices probed were "short-circuited", with markedly higher currents and nearly linear I-V curves. These "short-circuited" devices were not included in the plot of Fig. 3.3.

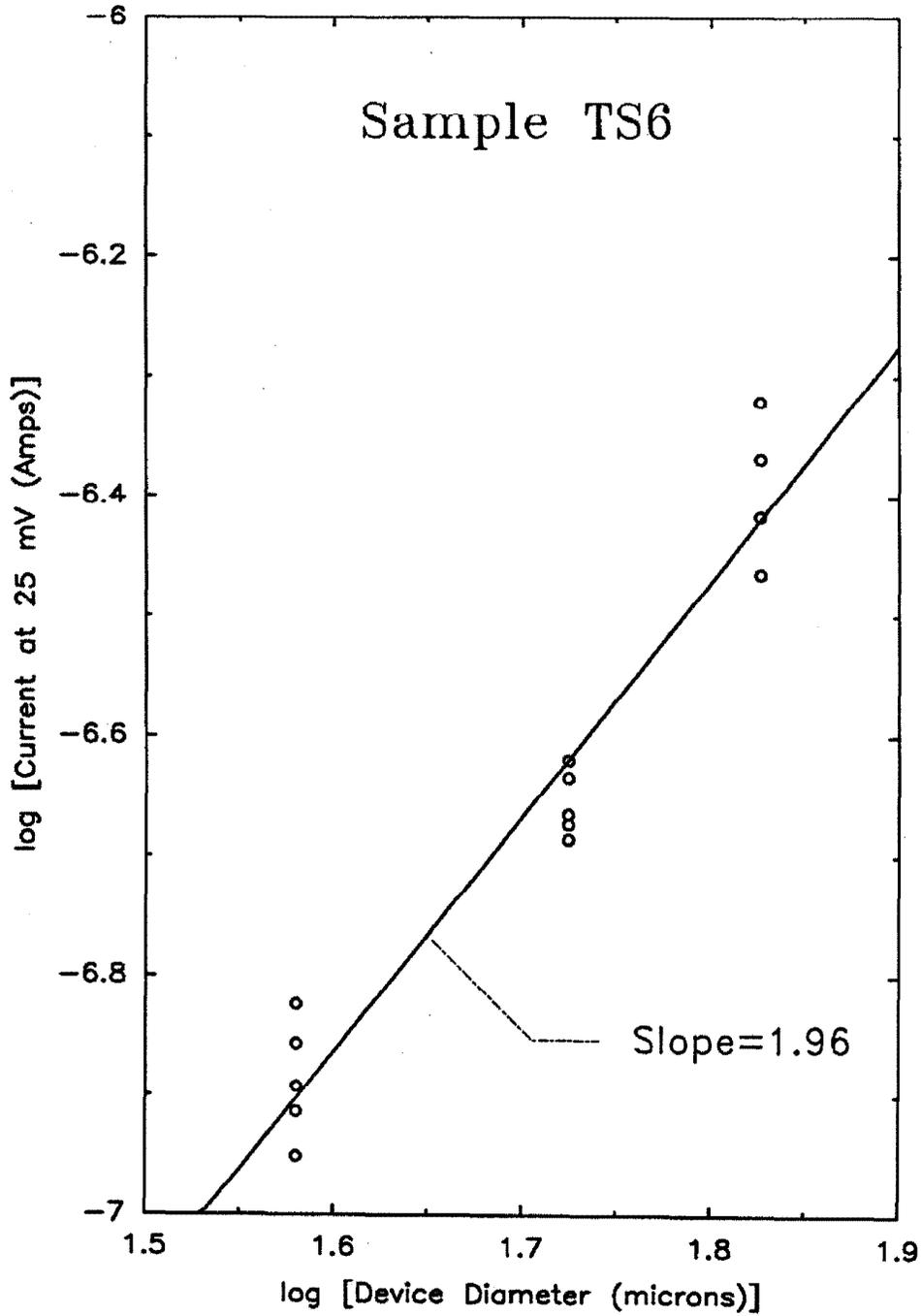


Figure 3.3: Log-log plot of the current vs. mesa diameter for a typical preparation of sample TS6. The current measurements were made at 300 K under an applied bias of 25 mV.

### 3.3.3 Low Temperature Electrical Contacts

Current-voltage measurements at low temperatures ( $<80$  K) were performed by placing the prepared samples into a liquid helium immersion dewar. Since probe wires could not be used inside the dewar, it was necessary to develop a permanent bonding scheme for the fabricated devices. Conventional wire bonding machines were not suitable for this purpose because the  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  devices were damaged by the ultrasonic bonding pulse. The following is a description of the permanent bonding technique used.

1. The technique creates bonds which are approximately  $100 \mu\text{m}$  diameter circles. Since the fabricated devices are smaller than the bonds, it is necessary to insulate the etched surface of the sample. Photoresist is spun on to the sample, exposed, and developed by standard photolithographic procedures. The second mask of the two mask process described in section 3.3.2 is used during exposure. Thus, an insulating photoresist film is placed on the sample, with holes aligned such that only the tops of the mesas are exposed.
2. The sample is mounted on an 8-pin header with silver print.
3. A conductive epoxy, Acme E-Solder No. 3021, is mixed. This epoxy can be cured at room temperature.
4. A thin gold wire ( $25 \mu\text{m}$  diameter) is mounted on a manipulator. The end of the wire is then dipped in the conductive epoxy.
5. With the assistance of a microscope, the wire is guided to a device by the manipulator. Good electrical contact is verified by measuring the I-V characteristic on a curve tracer during this process.
6. The epoxy is left to cure overnight.

7. Epoxy is applied to a pin on the header. The wire is then carefully clipped near the manipulator mount, and guided with tweezers to the header pin. The epoxy on the pin is then left to cure overnight.
8. The excess wire beyond the header pin is clipped.
9. Contacts to the etched surface are made in the same fashion, with the end of the wire epoxied to the gold pad at the end of the sample.

Room temperature I-V behavior from bonded devices was found to be identical to that obtained prior to bonding. The technique described above is both tedious and time consuming, and results in bonds which are not particularly resilient at low temperatures. In fact, cracking of the photoresist film and/or the epoxy bond often occurs upon cooling the sample to liquid helium temperatures. Consequently, only a few devices have been studied. It should be noted that low temperature stations which allow *in situ* probing of samples do exist. The use of such a station should enhance the reproducibility of this experiment considerably.

### 3.3.4 I-V Results at Low Temperatures

As discussed previously, the low temperature I-V behavior of sample TS6 was investigated by immersing bonded devices in liquid helium. Sample headers were mounted on a probe with electrical feedthroughs and a temperature sensor. The current-voltage curves shown in this subsection were obtained with a HP 4145A Semiconductor Parameter Analyzer. At low biases, it was possible to limit background current fluctuations to less than 10 pA by shielding all of the measurement cables. Data were stored in digital form on a HP9816 computer, and transferred to a DEC Microvax computer for plotting via an IEEE 488 bus.

Figure 3.4 contains I-V curves, taken from a 37  $\mu\text{m}$  diameter device at two temperatures, 4.2 and 15 K. The curves were obtained under reverse biased con-

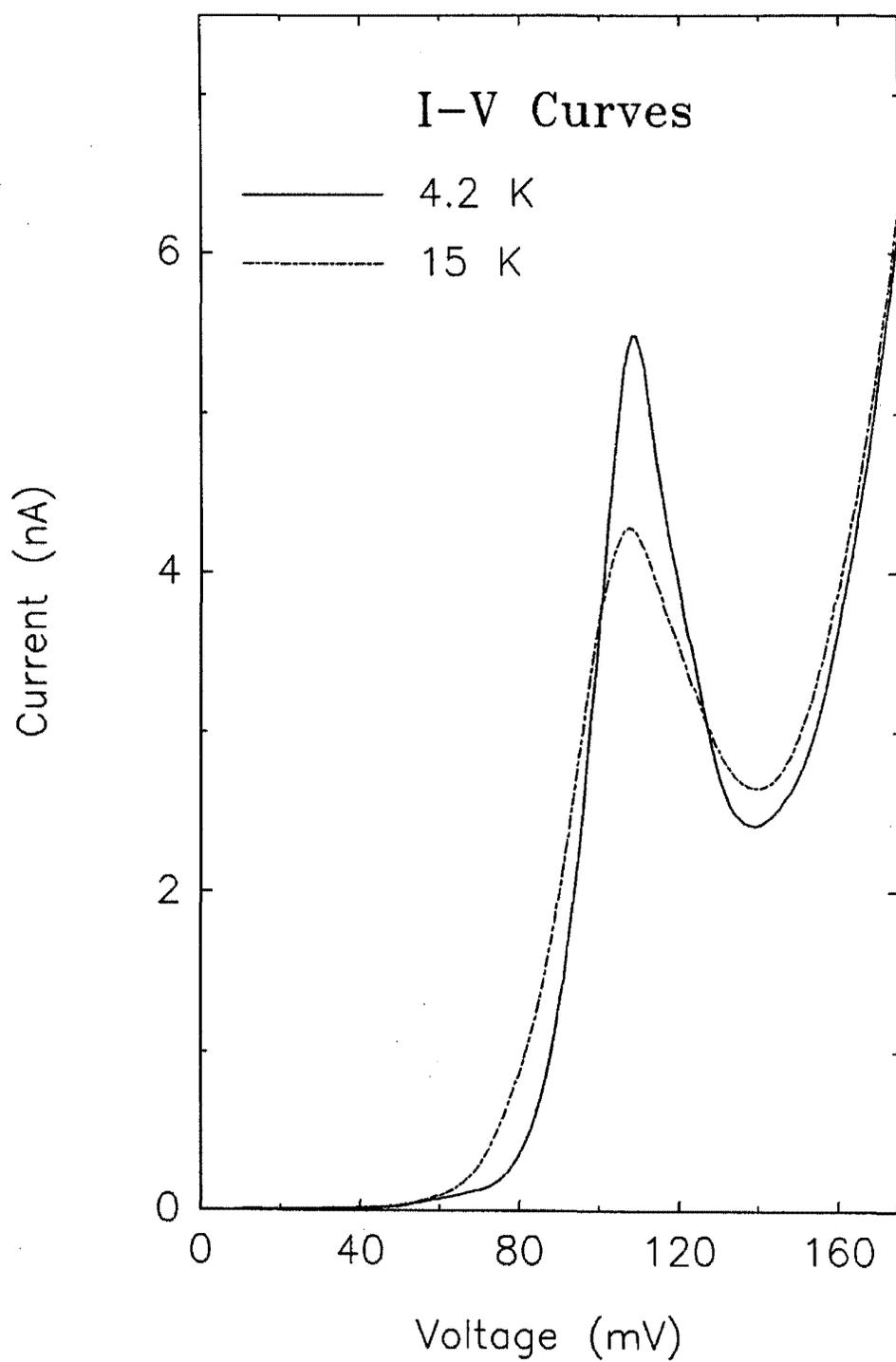


Figure 3.4: Reverse bias I-V curves from a  $37 \mu\text{m}$  diameter device. The solid (dashed) line is the curve obtained at 4.2 K (15 K).

ditions (negative voltage on the top electrode). The curve taken at 4.2 K displays negative differential resistance, with a peak current density of  $0.51 \text{ mA/cm}^{-2}$  at 109 mV. The peak-to-valley current ratio is slightly greater than 2:1, in reasonable agreement with the simulation results of section 2.4. However, the simulations also indicated that NDR should be displayed over the voltage range 50–100 mV (roughly), in contrast to the 109–139 mV range observed in Fig. 3.4. It is possible that a large contact resistance develops in the epoxy bonds at low temperature, leading to a shift of the tunneling characteristics to higher biases.

As shown in Fig. 3.4, the effect of lowering the temperature from 15 K to 4.2 K is to increase the peak-to-valley current ratio from 1.6:1 to 2.3:1. This increase is mainly due to an enhancement of the peak current, indicating that tunneling is enhanced at low temperatures. In contrast, double barrier tunnel structures often display increased peak-to-valley ratios at low temperatures due to the freeze out of nonresonant transport mechanisms. This freeze out results in a drop in the valley current. Increases in the tunneling current with decreasing temperature are difficult to understand because tunneling is a fairly temperature independent process. Two possible explanations are consistent with the observed data. (i) The tunneling electrons are nearer to the conduction band edge in the  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  electrodes at lower temperatures due to sharpening of the Fermi distribution. This effect would result in smaller imaginary wavevectors (and therefore, larger transmission coefficients). (ii) The valence band offset decreases as temperature decreases, leading to smaller imaginary wavevectors. Section 3.4 presents evidence for a temperature dependent valence band offset in this material system. The observation of NDR implies that the low temperature valence band offset is less than 100 meV, as discussed in section 2.4.

Figure 3.5 displays the forward bias I-V curve at 4.2 K from the  $37 \mu\text{m}$  diameter device discussed above. The curve shows two distinct NDR regions, with peak

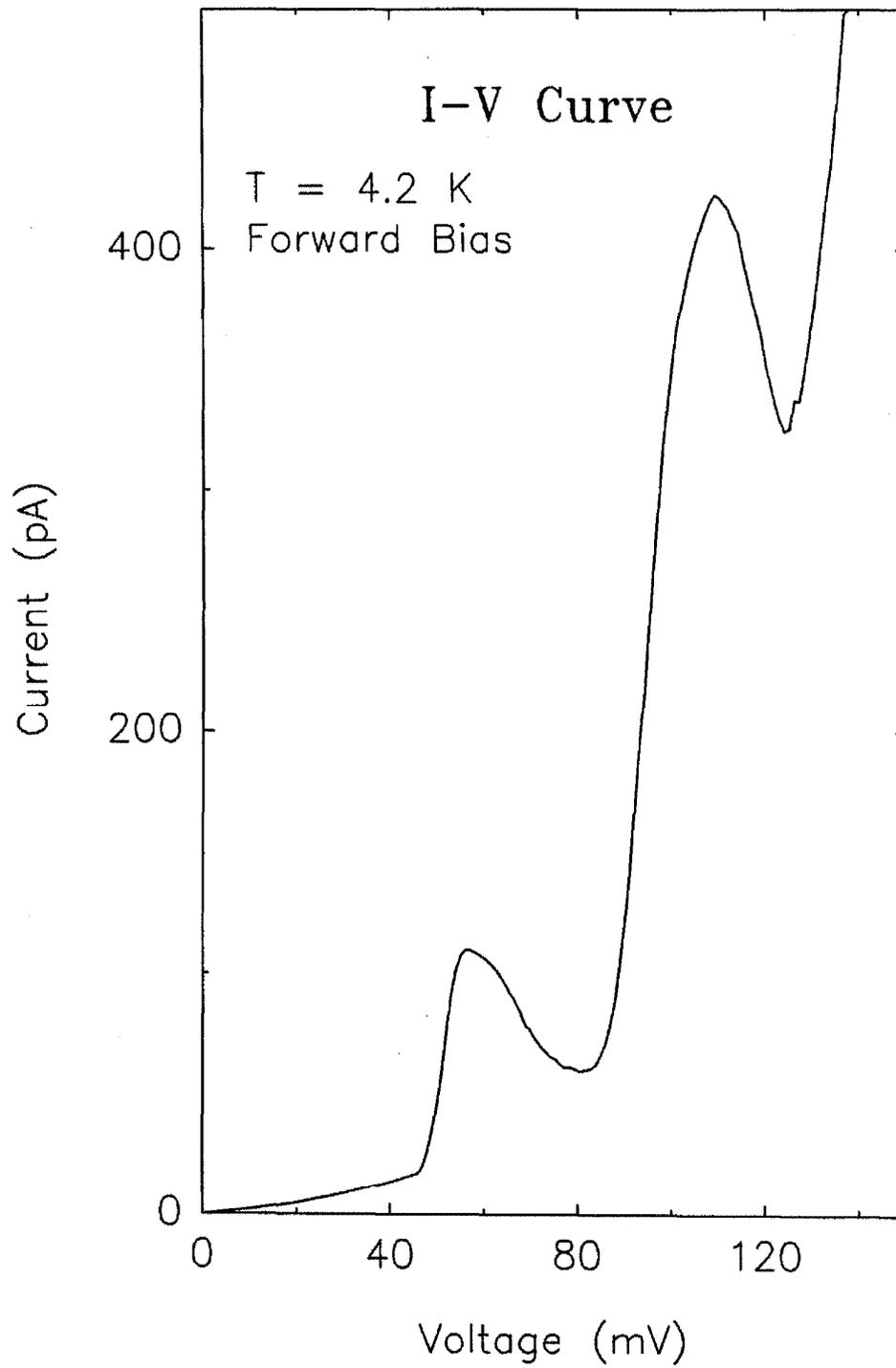


Figure 3.5: Forward bias I-V curve from same device as in Fig. 3.4. The curve was obtained at 4.2 K.

current densities of  $0.01 \text{ mA/cm}^2$  at 57 mV and  $0.039 \text{ mA/cm}^2$  at 109 mV. This bimodal characteristic is not predicted by our straightforward electron tunneling model. It is possible that nonuniformity in the portion of the sample covered by this device is responsible for the observed behavior. TEM studies indicated that the CdTe barrier thickness varies laterally from 170 to 250 Å in sample TS6. Another possible explanation is the presence of filled interface states, lying within the energy gap of the  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  electrodes. Such states could contribute electrons to the tunneling current, yielding discrete peaks as they become aligned with the conduction band edge in the opposite electrode.

The asymmetry between the forward and reverse bias I-V curves may be caused by an asymmetry between the interfaces on either side of the CdTe barrier. Fig. 3.6 is a high-resolution TEM photograph of the active region of the sample. A twin boundary is seen at the interface between the top  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  electrode and the CdTe barrier. In contrast, the interface between the barrier and the bottom  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  layer shows no evidence of twinning. The two types of interfaces are similar to the type A and B orientations which have been observed for  $\text{NiSi}_2$  on Si.[21] In both cases, the [111] growth direction gives rise to the two possible orientations. The  $\text{NiSi}_2$ :Si barrier height was shown to vary by greater than 100 mV, depending upon which type of interface was grown.[21,22]

Other devices tested at low temperatures gave a variety of results. A set of devices was fabricated on a second piece of sample TS6 to test the reproducibility of the observed NDR. A forward biased I-V curve taken from a 67  $\mu\text{m}$  diameter device on the second piece is shown in Fig. 3.7. The curve displays NDR over the voltage range 48-65 mV, with a peak-to-valley current ratio of 1.4:1. However, the peak current density is almost two orders of magnitude lower than that displayed in Fig. 3.4. This device also displayed inflections ( $d^2I/dV^2$  changed from positive to negative) at a higher positive bias, and in reverse bias. The reverse bias

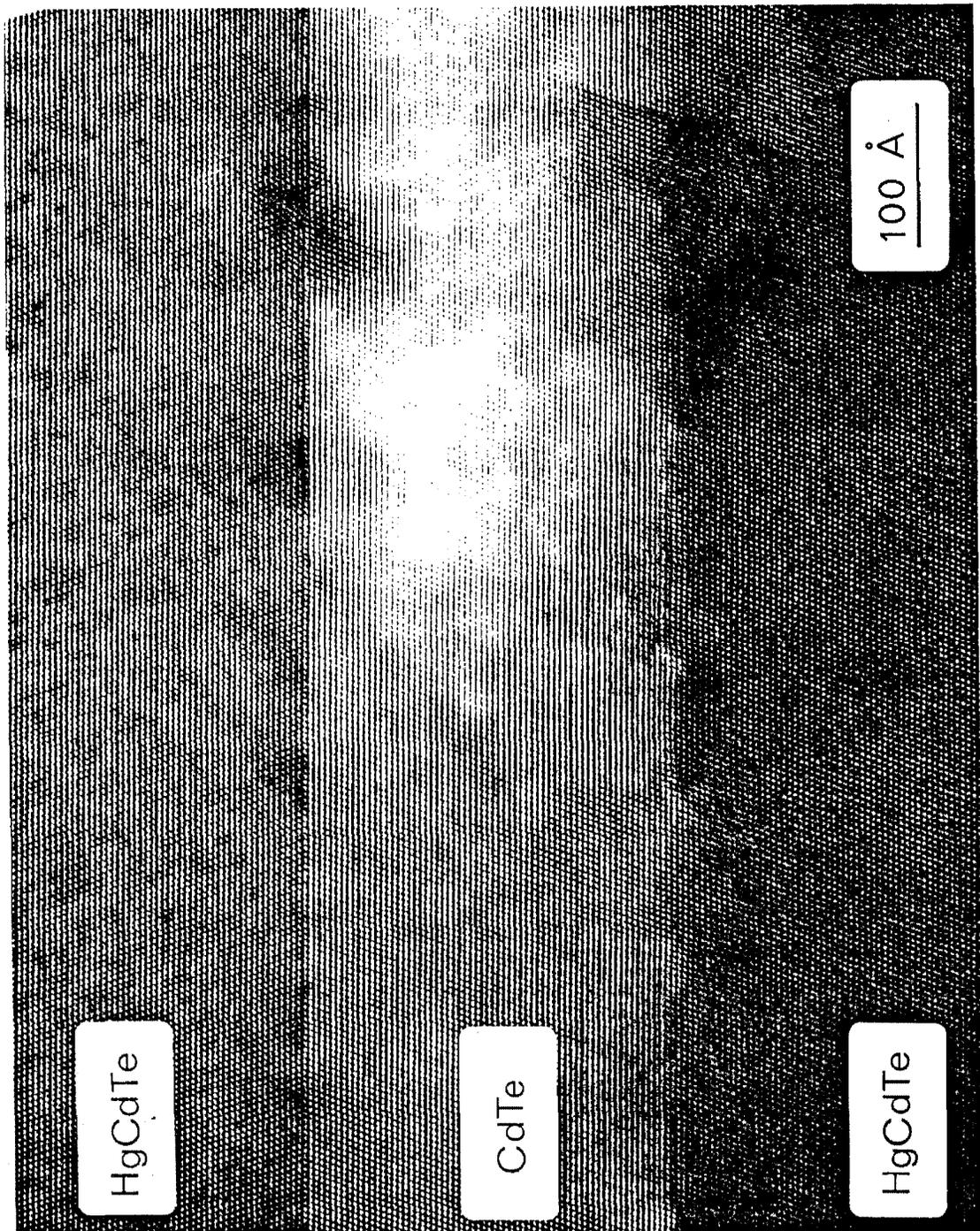


Figure 3.6: High resolution TEM picture of the active region of the  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  single barrier heterostructure. The picture reveals a twin boundary at the interface between the top  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  layer and the  $\text{CdTe}$  barrier.

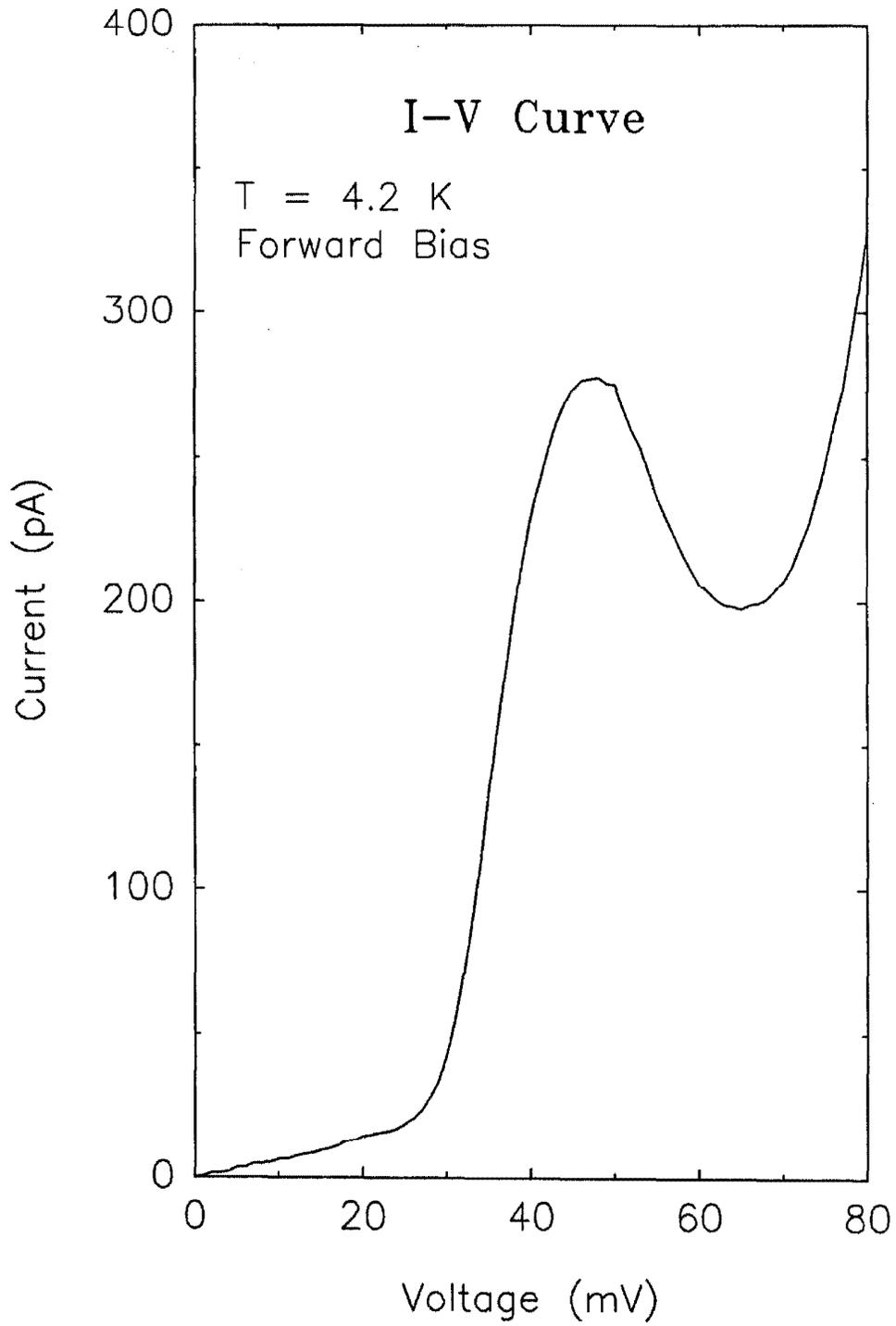


Figure 3.7: Forward bias I-V curve from a 67  $\mu\text{m}$  diameter device on sample TS6. The curve was obtained at 4.2 K.

characteristic is displayed in Fig. 3.8. Two other devices also displayed inflections at 4.2 K. However, three tested devices did not display any inflections or NDR. The variations in the I-V behavior of different devices may have been caused by nonuniformity in the sample or by the poor resiliency of the epoxy bonds at low temperatures.

### 3.4 Electrical Determination of the HgTe/CdTe Valence Band Offset

This section presents a study of the high temperature ( $>160$  K) I-V behavior of three  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  single barrier samples: TS6, ML26A, and ML26A'. The growth parameters for these samples were described in section 3.2. At high temperatures, the measured current is interpreted to be the sum of thermionic and tunneling hole currents. Both of these transport mechanisms depend exponentially upon the HgTe-CdTe valence band offset,  $\Delta E_v$ . Hence, analysis of the I-V data can yield a determination of  $\Delta E_v$ .

#### 3.4.1 Theoretical Simulations of Hole Currents

Energy band diagrams of  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  single barrier heterostructures with thick CdTe barriers (see for example, Fig. 1.5) suggest that the dominant source of current at high temperatures is the thermionic emission of holes from the  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  cladding layers across the CdTe valence band barrier. It is important to note that the  $n$ -type doping of the electrodes does not prohibit this transport mechanism because the electrode energy gaps are small (in this case,  $\leq 200$  meV). In fact, the thermionic barrier for electrons is much larger than that for holes, due to the large conduction band offset in these heterostructures.

A simple theoretical treatment, similar to the Bethe model for Schottky

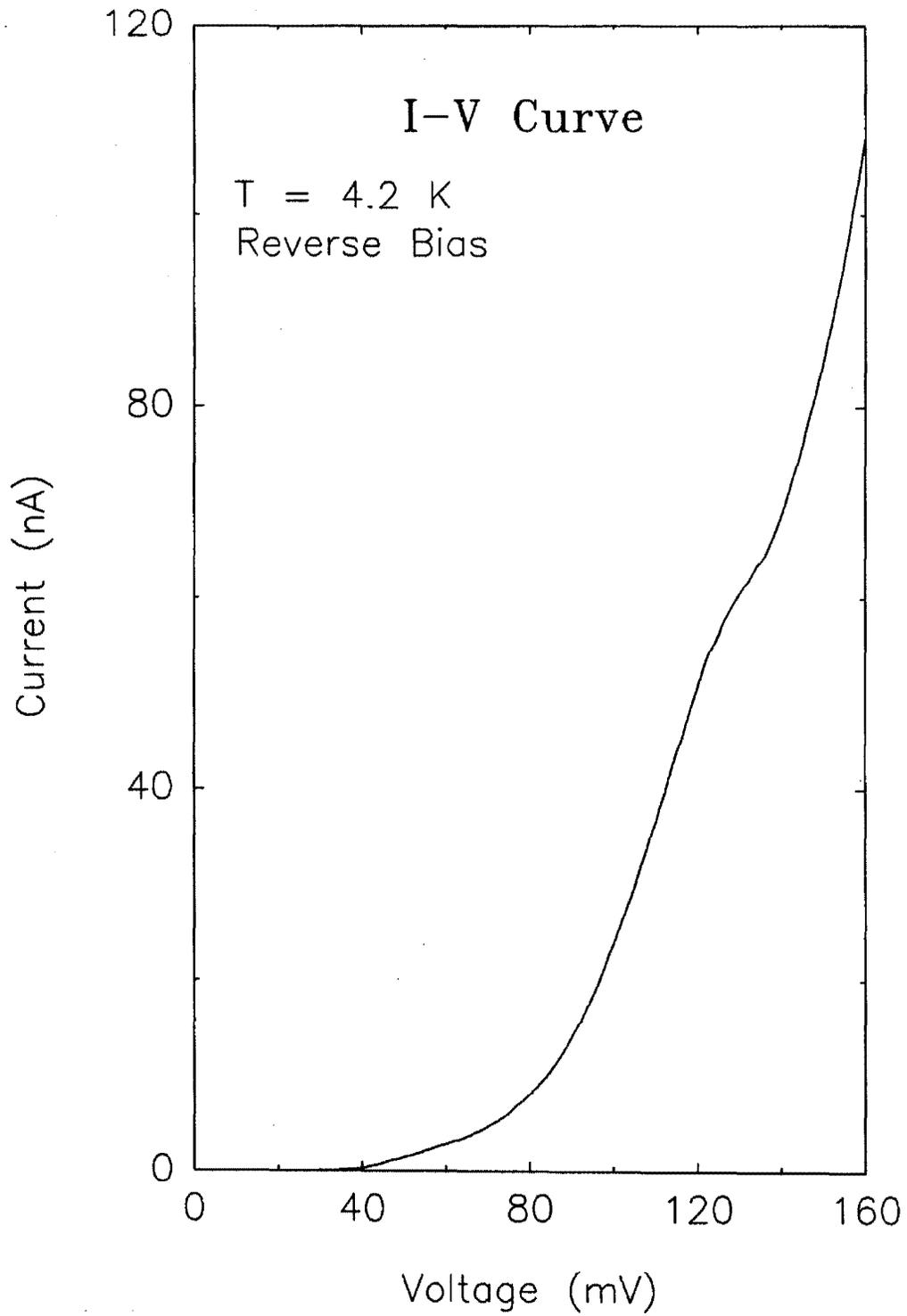


Figure 3.8: Reverse bias I-V curve at 4.2 K from the same device as in Fig. 3.7.

barriers,[23] can be developed to calculate thermionic and tunneling hole current densities across a single barrier as a function of applied voltage. The portion due to thermionic emission,  $J_{therm}$ , can be written:

$$J_{therm} = A^*T^2 \exp\left(\frac{-\phi + ceV}{kT}\right) \left[1 - \exp\left(\frac{-eV}{kT}\right)\right], \quad (3.1)$$

where  $A^*$  is the modified Richardson constant,  $\phi$  is the potential barrier height,  $T$  is the temperature,  $e$  is the hole charge, and  $c$  is the fraction of the total applied voltage which drops across the positively biased electrode. For these heterostructures,  $A^*$  is  $120(m_h^*)$  in  $A/cm^2K^2$ , where  $m_h^*$  is the unitless hole mass. The contributions from the light and heavy hole bands are summed to give the total current from this mechanism in the analysis of sample TS6. For samples ML26A and ML26A', only the heavy holes contribute to the current significantly, because the light hole band is split off in HgTe. It is important to note that the factor  $c$  is a function of the voltage applied across the heterostructure, and must therefore be derived from the energy band diagram for each individual bias condition. In this study,  $c$  has been calculated by the method outlined in section 2.2. The value of  $c$  is generally in the range 0.1 – 0.4 for the heterostructures studied here, as compared to the case of a Schottky barrier, where  $c = 1$ .

For sample TS6, the potential barrier height,  $\phi$ , in Eqn. 3.1 can be written:

$$\phi = E_f + E_g^{x=0.22} + (E_v^{x=0.22} - E_v^{x=0.95}), \quad (3.2)$$

where  $E_f$  is the Fermi energy relative to the conduction band minimum in the electrodes,  $E_g^{x=0.22}$  is the energy gap in the electrodes, and the quantity  $(E_v^{x=0.22} - E_v^{x=0.95})$  is the valence band offset at the  $Hg_{0.78}Cd_{0.22}Te-Hg_{0.05}Cd_{0.95}Te$  interface. The barrier height is reduced in samples ML26A and ML26A' due to the zero band gap HgTe electrodes:

$$\phi = E_f + (E_v^{x=0} - E_v^{x=0.85}), \quad (3.3)$$

where the quantity  $(E_v^{x=0} - E_v^{x=0.85})$  is the valence band offset at the HgTe–Hg<sub>0.15</sub>Cd<sub>0.85</sub>Te interface. It should be noted that the reduction in barrier height due to the HgTe cladding layers is partially compensated for by the larger composition difference between the barrier and the electrodes.

For applied voltages of  $\approx 50$  mV and higher, hole tunneling across the triangular shaped CdTe barrier makes a contribution to the total current through the heterostructure. This transport mechanism can be treated theoretically in a manner which is analogous to the model for the thermionic hole current. The resulting expression for the hole tunneling current density,  $J_{htun}$ , differs from that for  $J_{therm}$  by an integral term which replaces the contribution to  $\phi$  from the valence band offset. For sample TS6, we obtain,

$$J_{htun} = A^*T^2 \exp\left(\frac{-E_f - E_g^{x=0.22} + ceV}{kT}\right) \left[1 - \exp\left(\frac{-eV}{kT}\right)\right] \int_0^{u_A} t^2 u \exp\left(\frac{-u^2}{2}\right) du. \quad (3.4)$$

In this expression,

$$\frac{u^2}{2} = \frac{m_h^* v_l^2}{kT}, \quad (3.5)$$

where  $v_l$  is the group velocity of the holes in the growth direction,  $u_A = [2(E_v^{x=0.22} - E_v^{x=0.95})/kT]^{1/2}$ , and  $t^2$  is the transmission coefficient for holes tunneling through the CdTe barrier. Similarly, for samples ML26A and ML26A',

$$J_{htun} = A^*T^2 \exp\left(\frac{-E_f + ceV}{kT}\right) \left[1 - \exp\left(\frac{-eV}{kT}\right)\right] \int_0^{u_B} t^2 u \exp\left(\frac{-u^2}{2}\right) du, \quad (3.6)$$

where  $u_B = [2(E_v^{x=0} - E_v^{x=0.85})/kT]^{1/2}$ . In this study,  $t^2$  is calculated by the method described in section 2.2. The two band  $k \cdot p$  theory formula was used to find imaginary light hole wavevectors in the CdTe barrier, while imaginary heavy hole wavevectors were determined from the one-band formula.

### 3.4.2 Device Fabrication

Device preparation for sample TS6 was performed according to the procedure described in section 3.3.2. Samples ML26A and ML26A' were prepared by a slightly different procedure. Chemical etching was accomplished by the use of  $\text{Br}_2$ :ethylene glycol instead of  $\text{Br}_2$ : $\text{HBr}$ : $\text{H}_2\text{O}$ . The change in procedure was adopted because  $\text{Br}_2$ : $\text{HBr}$ : $\text{H}_2\text{O}$  was found to etch these samples nonuniformly, with material removed in large flakes. However, the  $\text{Br}_2$ :ethylene glycol recipe left a surface which was comparable in quality to the unetched surface. Circular mesa diameters were reduced to 15–40  $\mu\text{m}$  for preparations of ML26A and ML26A'. Measured currents were found to vary linearly with device area in all three samples, indicating the absence of surface leakage currents.

### 3.4.3 I–V Results and Analysis

In this subsection, experimental current–voltage measurements are presented, and analyzed via the theoretical model developed in section 3.4.1. High temperature ( $>80$  K) current–voltage curves were measured by probing the fabricated devices with a thin (25  $\mu\text{m}$  diameter) gold wire. Temperatures below 300 K were reached with an MMR Joule–Thompson cooling station.

Figure 3.9 contains an experimental current density–voltage (J–V) curve, taken from sample TS6 at 300 K. Also plotted is the J–V curve generated by the theoretical model discussed above for a barrier height  $\phi = 514$  meV. This value of  $\phi$  was chosen by requiring the theoretical and experimental current densities to be equal at 50 mV, and was the *only* adjustable parameter used. Selecting a different value of the applied bias results in changes in  $\phi$  of  $<10$  meV over the voltage range depicted in Fig. 3.9.

The electrode carrier concentrations given in table 3.1 for sample TS6 were determined at low temperature (30 K). Hall measurements have been performed

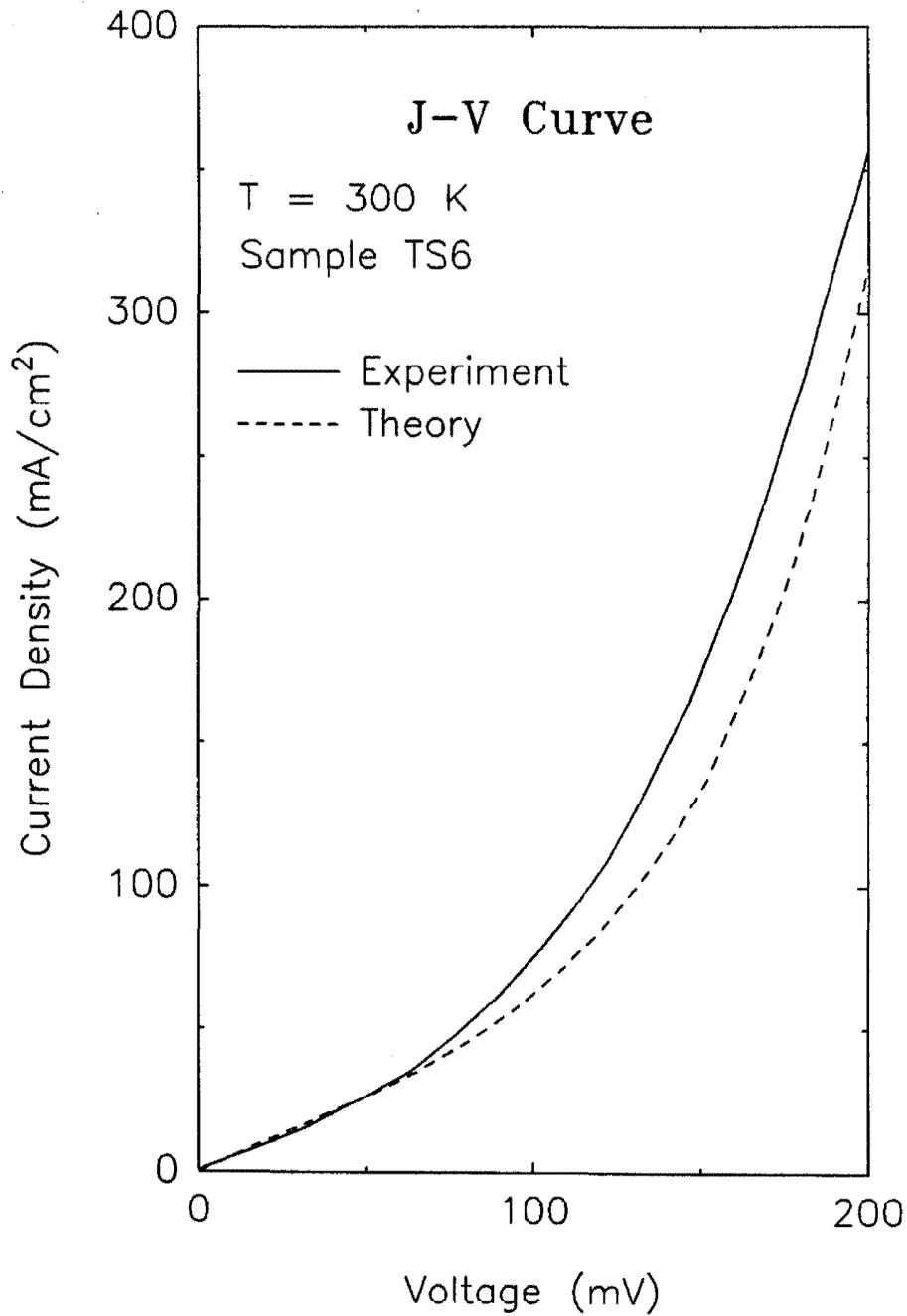


Figure 3.9: Experimental J-V curve taken from sample TS6 at 300 K. Also plotted is a theoretical curve calculated for a HgTe-CdTe valence band offset of 390 meV.  $\Delta E_v$  is the only adjustable parameter used to generate the theoretical curve.

at 300 K, yielding a free electron concentration of  $1.5 \times 10^{17} \text{ cm}^{-3}$  in the cladding layers of sample TS6. Assuming that the electrons form a nearly free Fermi gas,  $E_f$  can be estimated to be  $44 \pm 10$  meV above the conduction band edge in the  $\text{Hg}_{0.78}\text{Cd}_{0.22}\text{Te}$  electrodes. The value of  $E_g^{x=0.22}$  is taken here to be  $185 \pm 20$  meV at 300 K.[8] In addition, the uncertainty of the cladding layer compositions is estimated to produce an uncertainty of  $\approx 15$  meV in the value of the electrode energy gap. Eqn. 3.2 then gives,

$$(E_v^{x=0.22} - E_v^{x=0.95}) = 285 \pm 55 \text{ meV.} \quad (3.7)$$

A linear extrapolation of this expression to a pure HgTe–CdTe heterojunction yields  $\Delta E_v = 390 \pm 75$  meV.

As discussed previously, samples ML26A and ML26A' are expected to yield higher current densities than sample TS6. Furthermore, the higher electron densities in the pure HgTe electrodes result in less of the applied voltage being dropped there, i.e., , the factor  $c$  in Eqn. 3.1 is smaller for samples ML26A and ML26A'. Thus, the current density varies more slowly with voltage in these samples. Fig. 3.10 contains an experimental J–V curve taken from sample ML26A' at 300 K. Also plotted is the theoretical curve generated for a barrier height  $\phi = 332$  meV, which was selected in the same manner as the  $\phi$  used in Fig. 3.9. As expected, Fig. 3.10 displays larger current densities than Fig. 3.9, and shows a weaker voltage dependence.  $E_f$  is estimated to be  $75 \pm 30$  meV for the HgTe cladding layers at 300 K. Eqn. 3.3 then gives,

$$(E_v^{x=0} - E_v^{x=0.85}) = 257 \pm 40 \text{ meV.} \quad (3.8)$$

Linear extrapolation of this expression to a pure HgTe–CdTe heterojunction yields  $\Delta E_v = 300 \pm 50$  meV. A similar analysis of 300 K data from sample ML26A obtains  $\Delta E_v = 290 \pm 50$  meV.

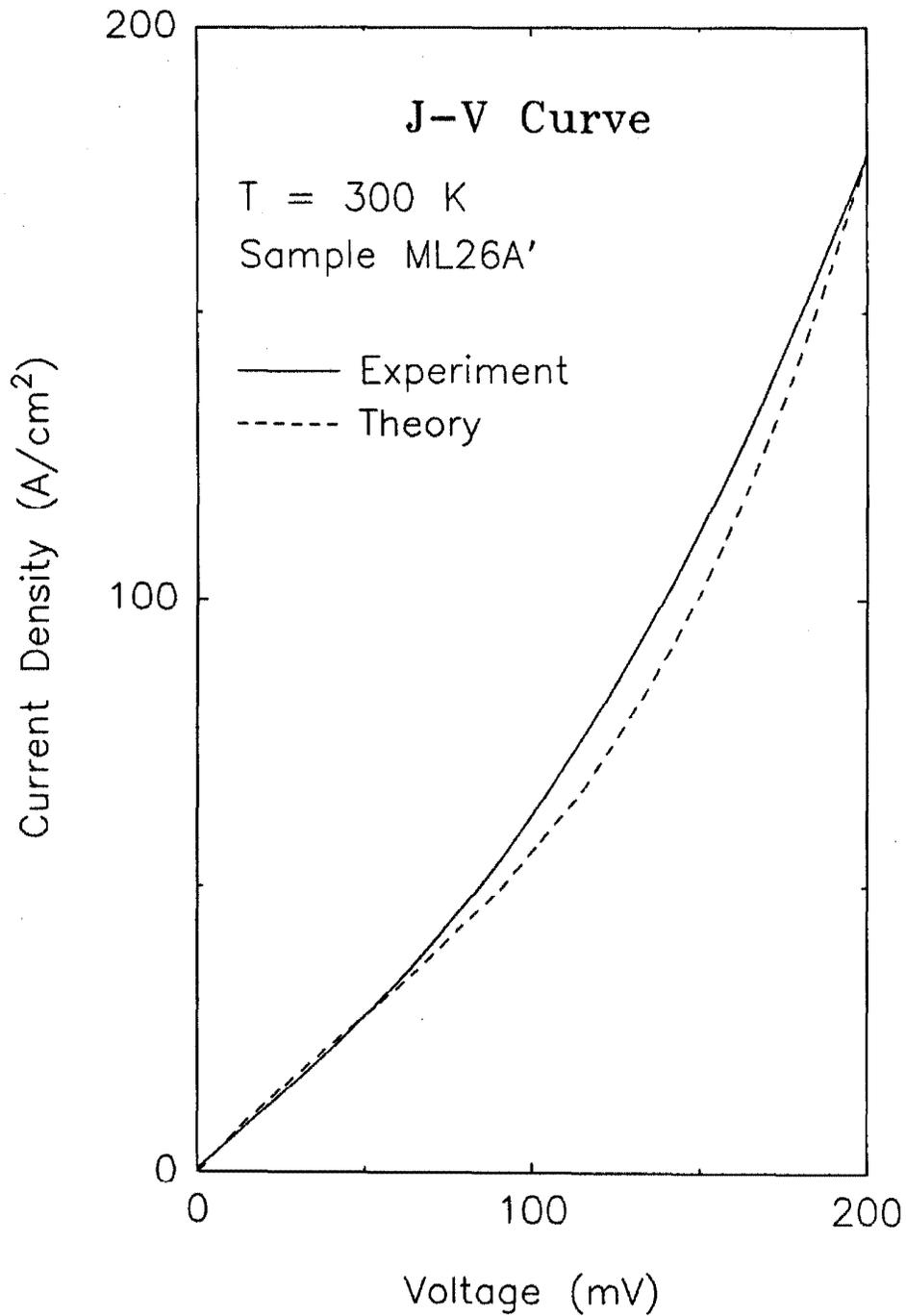


Figure 3.10: Experimental J-V curve taken from sample ML26A' at 300 K. Also plotted is a theoretical curve calculated for a HgTe-CdTe valence band offset of 300 meV.

Figure 3.11 contains the measured current density from each of the three samples as a function of temperature over the range 190–300 K. The data were taken for an applied bias of 50 mV and are displayed in the standard  $\log(J/T^2)$  vs.  $1/kT$  format. As discussed previously, the current density in sample TS6 is considerably less than in the other two samples at all temperatures. In addition, samples ML26A and ML26A' yield currents with nearly a  $T^2$  temperature dependence, while sample TS6 varies more strongly with temperature. These results can be shown to be consistent with a valence band discontinuity which decreases nearly linearly as the temperature decreases.

In samples ML26A and ML26A',  $E_f$  behaves roughly as  $(\text{const} \times T)$  due to the nearly intrinsic HgTe cladding layers. Thus, if

$$(E_v^{x=0} - E_v^{x=0.85}) \propto T, \quad (3.9)$$

then Eqn. 3.3 yields,

$$\phi \propto T. \quad (3.10)$$

The current density in Eqn. 3.1 would then have a  $T^2$  dependence, in agreement with the data shown in Fig. 3.11.

On the other hand, Eqn. 3.2 has an extra term,  $E_g^{x=0.22}$ , which has a temperature independent part:[8]

$$E_g^{x=0.22} \text{ meV} \approx 100 + 0.284 \times T. \quad (3.11)$$

In addition, the Fermi level in the cladding layers of sample TS6 is not due to intrinsic carriers, and will therefore have a temperature independent part over the range of interest here.\* This part can be estimated to be 25 meV from the carrier densities given previously. Therefore, we suggest that the barrier height in sample

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\*sample TS6 was indium doped; no intentional impurity doping was used in the growth of samples ML26A and ML26A'.

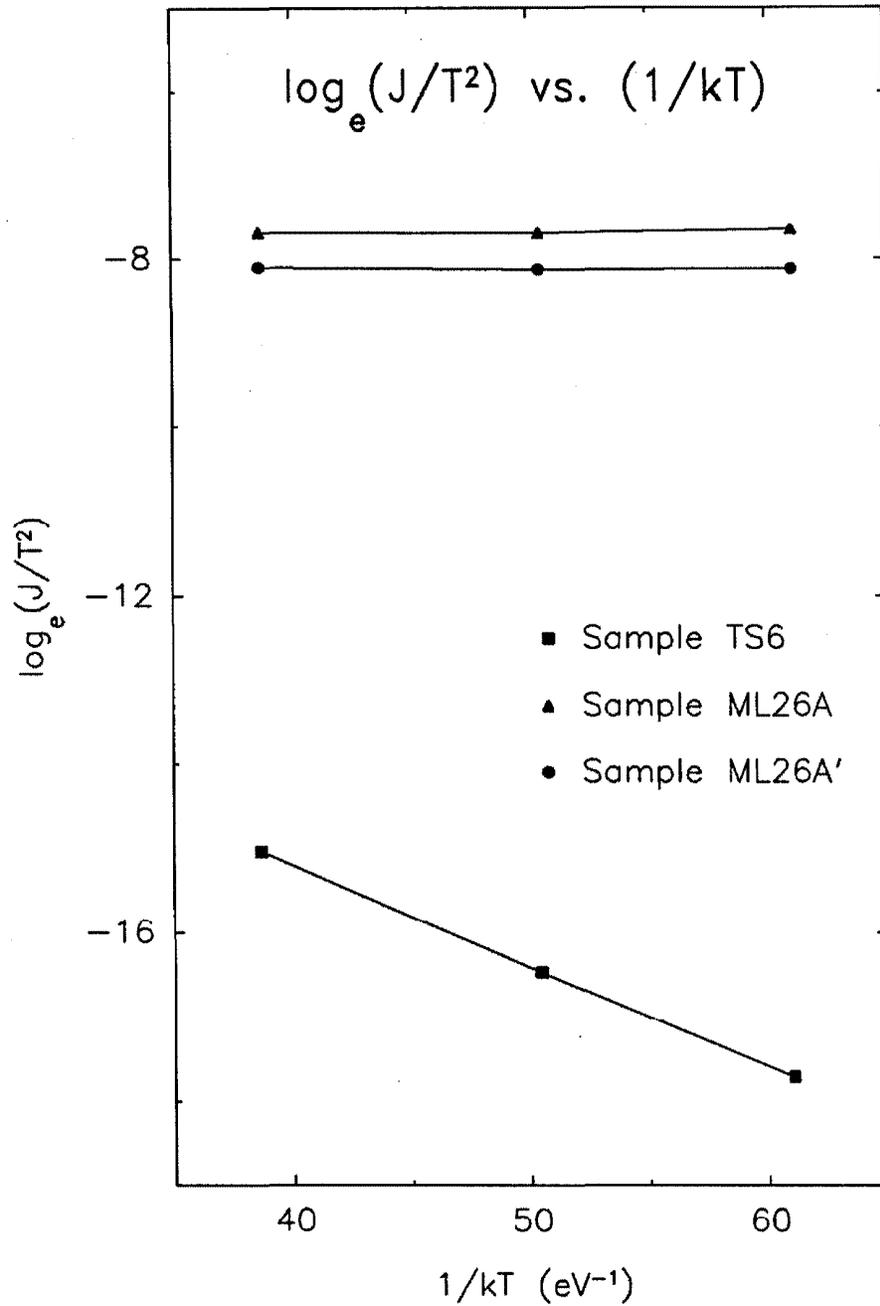


Figure 3.11: Measured current density from samples TS6, ML26A, and ML26A' as a function of temperature, plotted in a  $\log_e(J/T^2)$  vs.  $1/kT$  format. The data from all three samples are consistent with a valence band offset which decreases linearly as the temperature decreases.

TS6 can be written:

$$\phi = 125\text{meV} + (\text{const} \times T). \quad (3.12)$$

This behavior would give a current density in Eqn. 3.1 which depends on temperature as  $[T^2 \times \exp(-125/kT)]$ . The line in Fig. 3.11 has a slope of  $-120$  meV, in reasonably good agreement with this hypothesis.

It should be noted that if an unknown transport mechanism is contributing to the observed currents, the above analysis will lead to false determinations of the band offsets. However, the fact that the experimental J-V behavior is very close to that predicted by the theoretical model used here supports the assertion that the observed current is due solely to thermionic and tunneling hole currents.

### 3.5 Other Samples

As discussed previously, the remainder of the samples listed in table 3.1 were unsuitable for single barrier NDR effects because of their thin barrier layers. None of these samples has been studied at liquid helium temperatures. Furthermore, these samples were not used for the band offset determination of section 3.4 because the observed currents could not be attributed to the thermionic hole mechanism. Nevertheless, the majority of the samples display nonlinear I-V curves, indicating that the CdTe barrier plays an active role in limiting current. It is possible that elastic and/or inelastic tunneling dominate the high temperature transport across thin CdTe layers.

Figure 3.12 is a log-log plot of current at 300 K vs. mesa diameter for a preparation of sample TS4. Although the spread of measured currents is large for each device diameter, the slope of the best fit line to the data in Fig. 3.12 is nearly 2, indicating the absence of surface leakage currents. Most of the samples listed in table 3.1 yielded currents which scaled linearly with device area. However, four

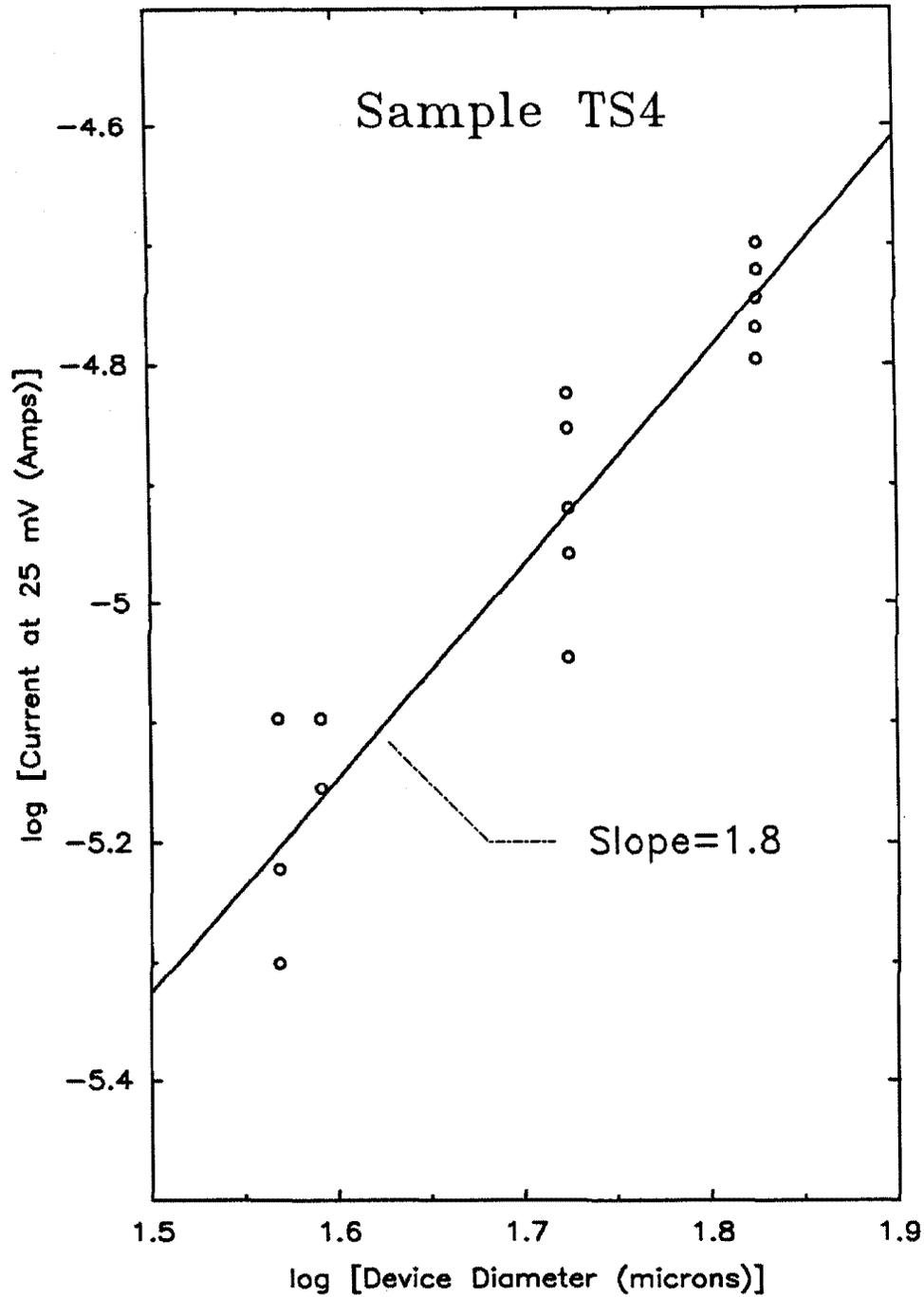


Figure 3.12: Log-log plot of current vs. mesa diameter for a preparation of sample TS4. The current measurements were made at 300 K under an applied bias of 25 mV.

of the samples, TS1, TS3, TS5, and ML26B, did not satisfy this criterion. In the cases of the UIC samples, doping difficulties (TS1 and TS5 were  $p$ -type, while TS3 had virtually no carriers) are the most likely cause of the unusual I-V behavior. Sample ML26B may suffer from structural defects due to the (100) orientation of the CdTe substrate.

### 3.6 Summary of Conclusions

We have reported the first experimental observation of NDR due to electron tunneling in a single barrier heterostructure. The sample used to demonstrate NDR consisted of a thin CdTe layer sandwiched between two  $\text{Hg}_{0.78}\text{Cd}_{0.22}\text{Te}$  electrodes. The largest peak-to-valley current ratio attained was slightly greater than 2:1. In the  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  material system, NDR can only be achieved at low temperatures ( $T < 20$  K) due to the dominance of thermionic hole currents at high temperatures. The observation of NDR in this system implies that the low temperature valence band discontinuity at the HgTe-CdTe interface is less than 100 meV.

High temperature current-voltage behavior from three  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  heterostructures has been investigated. The measured currents have been interpreted to be the sum of thermionic and tunneling hole currents. This analysis yielded values of the HgTe-CdTe valence band offset between  $290 \pm 50$  meV and  $390 \pm 75$  meV at 300 K. In all three samples, data taken over the range 190-300 K were consistent with a valence band offset which decreases at lower temperatures.

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## Chapter 4

# Molecular Beam Epitaxy of III–V Heterostructures

### 4.1 Introduction

#### 4.1.1 Background

The purpose of the molecular beam epitaxy (MBE) system described in section 1.4 is to supply semiconductor heterostructures for many different research projects. Thus, a large menu of available semiconducting materials is desirable because it enhances the flexibility of the system for growing novel heterostructure devices. Unfortunately, a combination of many different source materials in a single MBE chamber often results in a loss of semiconductor purity due to cross-contamination of the various materials. Hence, the pursuit of novel heterostructures as a general goal results in a trade off of material purity for variety of samples. Structures which require extremely high purity and reproducibility are not well-suited to such a research program, and are generally better produced in a more development oriented situation. Due to the nature of semiconductors, even systems which are designed for high flexibility can be contaminated to the extent

that desired structures cannot be grown. Clearly, a balance between purity and flexibility is needed.

As was discussed in section 1.4, the MBE system used here has chambers for each of the three major classes of semiconductors. This greatly reduces the probability of contamination due to elements from different columns of the periodic table, which is considerably worse than contamination within a class. For example, a one part per thousand concentration of indium in MBE grown GaAs is considerably less serious than the same incorporation of tellurium. This is due to the fact that tellurium is a dopant in GaAs, and would result in very degenerate  $n$ -type material, in contrast to the small indium alloying effect which has little effect upon the behavior of many GaAs devices. The separation of the MBE system into independent growth chambers for different classes of semiconductors prevents the more serious cross-contamination possibilities, while maintaining a large degree of flexibility in designing novel heterostructures.

The III-V growth chamber portion of the MBE system has been used to produce all of the samples discussed in this section. Most of the work presented here involves the heavily studied GaAs/AlAs system. This material combination continues to be of interest for high speed and optoelectronics applications, and for studies of fundamental quantum phenomena. Although much of the current research being performed with the III-V chamber involves other materials, it is likely that  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  heterostructures will continue to be of interest for quite some time. Thus, it is highly desirable to retain the capability to grow high quality GaAs, AlAs, and  $\text{Al}_x\text{Ga}_{1-x}\text{As}$ . Periodic growths of a few standard, well-characterized  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  heterostructures are performed in the III-V chamber routinely to check for contamination problems.

### 4.1.2 Summary of Results

A few standard  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  structures have been characterized to provide reference points for the status of the system at any given time. GaAs/AlAs double barrier heterostructures have been found to yield I-V curves which display reproducible negative differential resistance (NDR) behavior. Peak-to-valley current ratios of 2.5:1 at 300 K and 10:1 at 77 K are routinely obtained under good system conditions. Photoluminescence spectra from single quantum well heterostructures have been shown to yield sharp exciton peaks at the expected confinement energy. The full width at half maximum of these peaks corresponds to fluctuations of less than one monolayer in well thickness. Modulation doped GaAs layers (or high electron mobility transistors) have been characterized by Hall effect measurements. A pronounced enhancement in the electron mobility at 77 K is observed due to the spatial separation of free carriers and ionized impurities. Bulk (lightly doped *n*-type) GaAs layers have also been characterized by photoluminescence and Hall effect measurements.

A measurement of the GaAs/AlAs valence band offset by x-ray photoemission spectroscopy has been made. This experiment was performed by growing GaAs/AlAs heterojunctions and bulk samples in the III-V chamber and transferring them through the UHV transfer tube to the ESCA chamber. The GaAs valence band maximum was found to lie  $0.46 \pm 0.07$  eV above that of AlAs, independent of growth sequence (the offset is commutative). The capability to study the MBE grown samples without exposing them to atmosphere was ideal for this measurement.

A set of double barrier GaAs/AlAs heterostructures has been grown for optical measurements of electron tunneling rates. These structures were designed to have varying AlAs barrier thicknesses, constant GaAs well thicknesses, and a very thin top GaAs cladding layer ( $\approx 300$  Å). This sample geometry permitted time resolved

measurements of the quantum well photoluminescence, which was found to decay as electrons tunnel out of the well. Measured tunneling times ranged from 12 ps for 16 Å barriers to 800 ps for 34 Å barriers. An exponential dependence of decay time with barrier thickness was observed.

Triple barrier GaAs/AlAs heterostructures have been grown and prepared as two terminal electrical devices as a test of electron coherence in resonant tunneling structures. NDR has been observed in the I-V curves of these devices, with multiple resonances indicating a coherent nature of the tunneling process. Thin middle AlAs barriers have been found to yield the best NDR behavior in terms of peak-to-valley current ratios and number of resonances. As the middle AlAs barrier thickness is increased, the NDR behavior is degraded due to a loss of coherence. Unusually large peak-to-valley current ratios (as large as 19:1) have been observed at 77 K from these structures.

A method for growing high quality (relaxed) InAs on GaAs substrates has been developed and tested thoroughly. The method relies on a short period  $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}/\text{GaAs}$  superlattice at the InAs/GaAs interface. It is hypothesized that the superlattice suppresses island formation during the initial, heavily dislocated growth, allowing a high quality bulk InAs layer to be deposited once the film has reached the unstrained InAs lattice constant. A set of 2 μm thick InAs layers has been grown in this fashion, and tested by *in situ* RHEED analysis, Hall effect measurements, optical surface morphology, and x-ray diffraction. Electron mobilities comparable to bulk InAs values have been obtained. RHEED oscillations, comparable in quality to the best reported for InAs growth, have been observed.

### Recent Results

Current research activities on the III-V growth chamber involve a larger variety of materials. Unfortunately, most of these results are too recent for detailed

reports to be included in this thesis. A quick summary of some of the current activities is given here. InAs/AlSb double barrier heterostructures have been grown and demonstrated to show resonant tunneling behavior which rivals that of GaAs/AlAs double barriers. Furthermore, InAs/AlSb structures are potentially much faster than their GaAs/AlAs counterparts due to the high InAs mobility and the high conduction band offsets in this system. The InAs/GaAlSb single barrier NDR structure discussed in section 2.5 has been grown and demonstrated to have considerably better performance than that reported by Munekata et al.[1] InAs/GaSb superlattices have been grown and demonstrated to yield infrared photoluminescence. These structures have been proposed to be well suited to applications as far-infrared detectors with the addition of In to the GaSb layers, and/or the use of thicker superlattice layers. All of these newer structures have been grown on thick InAs buffer layers, deposited on GaAs substrates by the previously described method.

### 4.1.3 Outline of Chapter

Section 4.2 presents growth parameters and characterization data for a number of standard GaAs/Al<sub>x</sub>Ga<sub>1-x</sub>As heterostructures. Included in the discussion are double barrier structures, single quantum wells, high electron mobility transistors, and bulk film properties. Brief descriptions of substrate cleaning procedures and general growth information are also included in this section. The samples grown for the measurement of the GaAs/AlAs valence band offset by x-ray photoemission are discussed in section 4.3. Section 4.4 contains results from an optical study of tunneling times in GaAs/AlAs double barrier heterostructures. Emphasis is placed on design and MBE growth of samples for the study. Section 4.5 presents an investigation of electron coherence in triple barrier GaAs/AlAs heterostructures. The development of a method for growing high quality InAs bulk layers on GaAs

substrates is discussed in section 4.6. Finally, the conclusions of this chapter are summarized in section 4.7.

## 4.2 Standard $\text{Al}_x\text{Ga}_{1-x}\text{As}$ Heterostructures

As discussed previously, several  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  heterostructures have been characterized and used as standards for the status of the III-V chamber. This section contains descriptions of the standard structures and typical figures of merit obtained under good system conditions. Brief discussions of substrate preparation procedures and typical  $\text{GaAs}/\text{Al}_x\text{Ga}_{1-x}\text{As}$  growth conditions are also included.

### 4.2.1 Substrate Preparation

All of the samples discussed in this chapter have been grown on GaAs substrates, which are cheaper and generally of higher quality than most commercially available III-V substrates. These substrates can be obtained in either conductive (heavily doped  $n$ -type) or insulating form. Etch pit densities are typically on the order of  $10^3\text{cm}^{-2}$  to  $10^4\text{cm}^{-2}$  for (100)-oriented substrates.

Generally, GaAs substrates are etched and polished mirror smooth by the companies that sell them (such as Sumitomo). The procedure for preparing these substrates for MBE growth is fairly well known,[2] although minor variations are found from one laboratory to the next. The procedure followed in our laboratory is given here. Initially, the substrates are immersed successively in warmed solvents (trichloroethane, acetone, and isopropyl alcohol) to remove organic contaminants from the surface. Next, the substrates are rinsed in deionized water, blown dry, and etched in 5:1:1  $\text{H}_2\text{SO}_4:\text{H}_2\text{O}:\text{H}_2\text{O}_2$  for 2 minutes. This etch removes approximately 10  $\mu\text{m}$  of material from the surface, and serves to eliminate polishing damage and contaminants near the surface. A protective oxide is left on the GaAs surface.

Finally, the substrates are rinsed in deionized water and blown dry with filtered nitrogen gas.

Once etched, GaAs substrates are carefully cleaved into suitably sized pieces and indium bonded to molybdenum blocks. These blocks are then loaded into a small "intro hatch" which can be pumped down from atmosphere to the  $10^{-8}$  Torr quickly. Each of the three intro hatches on the MBE system can accommodate six blocks, and can be heated to approximately  $100^{\circ}\text{C}$  to remove water vapor prior to entry into the UHV chamber.

The protective oxide on a GaAs substrate is removed once it has entered the III-V chamber by heating it to approximately  $600^{\circ}\text{C}$  in an As flux. The desorption of the oxide can be monitored by reflection high energy electron diffraction (RHEED). At the time of oxide desorption, the RHEED pattern is observed to change from a hazy uniform background with a few diffraction spots to a clear set of streaky spots on a dark background. It has been observed that the power output from the substrate heater power supply required to reach the oxide desorption temperature is nearly constant for a given block once it has been well coated.

#### 4.2.2 $\text{Al}_x\text{Ga}_{1-x}\text{As}$ Growth Parameters

Optimum growth parameters for GaAs,  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  and AlAs have been thoroughly studied.[2] The three major parameters are substrate temperature, As/Ga (or As/Al) flux ratio, and growth rate.

For all of the GaAs/ $\text{Al}_x\text{Ga}_{1-x}\text{As}$  heterostructures discussed in this chapter, the substrate temperature was chosen to be  $\approx 600^{\circ}\text{C}$ . This temperature is considered to be optimal for GaAs growth. However, it has been reported that better quality  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  and AlAs layers are usually obtained at higher temperatures (up to  $\approx 700^{\circ}\text{C}$ ).[2,3] Five methods have been used to monitor substrate temperatures in this study: (i) optical pyrometry, (ii) thermocouple readings on the back of

the molybdenum block, (iii) block color, (iv) output power of the substrate heater power supply, and (v) observation of oxide desorption by RHEED. Of these methods, the optical pyrometer has proven to be the most reliable. Output power is reproducible for a given block, but is more cumbersome to use, since it doesn't give a direct temperature readout. Oxide desorption provides a good calibration point for the other methods, and block color is useful as a rough check at high temperatures. Thermocouple readings generally provide only relative information about substrate temperatures.

Flux ratios are difficult to measure quantitatively. However, it has been reported that the optimum As flux for GaAs growth is slightly greater than that required to maintain the As-stabilized surface. This surface is characterized by a  $2 \times 4$  reconstruction, which can be observed by RHEED. We have calibrated residual gas analyzer (RGA) scans to the transition from the As-stabilized surface to the Ga-stabilized surface. The desired flux ratio is then obtained by adjusting the As evaporator temperature until the RGA peak heights are in the appropriate range. A flux monitor ("nude" ion gauge) is also used to check the flux ratio. Since the congruent sublimation temperature for  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  is high (compared to GaAs), a smaller As flux than that used for GaAs is usually sufficient to maintain the As-stabilized surface for  $\text{Al}_x\text{Ga}_{1-x}\text{As}$ .

As discussed previously, III-V growth rates are usually determined solely by the group III flux. We have measured growth rates for bulk MBE grown films by shadowing a small portion of a substrate with a tantalum wire, and measuring the depth of the resulting trench with a stylus profilometer. The rates obtained this way have been found to be reproducible to within 2% for films grown within a few days (i.e., within a few growths) of each other. RHEED intensity oscillations have also been used to calibrate thin film growth rates. The thin film rates are usually found to be approximately 10% higher than the bulk rates. This disparity may be

caused by temperature transients in the ovens initiated by opening the shutters, or by enhancement of the growth rate due to the incident electron beam. We have usually grown GaAs at a rate of 1  $\mu\text{m}/\text{hour}$ , or approximately 1 monolayer/second. AlAs has been grown at rates ranging from 0.1  $\mu\text{m}/\text{hour}$  to 1  $\mu\text{m}/\text{hour}$ . The  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  growth rate has been found to be identical to the sum of the GaAs and AlAs rates for given Ga and Al oven temperatures, respectively.

### 4.2.3 Double Barrier Heterostructures

As discussed in chapter 1, extensive work has been reported on resonant tunneling in double barrier  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  heterostructures. Since much of our research is directed towards tunneling in semiconductors, these double barrier structures are a logical choice for standard growths. Two terminal electrical devices are defined in these structures, and tested for negative differential resistance (NDR). Peak-to-valley current ratios and peak current densities are used as measures of growth quality.

We have employed two standard double barrier geometries. Each of these heterostructures begins with a 0.5  $\mu\text{m}$ , heavily doped  $n$ -type GaAs layer, grown on a conductive GaAs substrate. Next, a 500  $\text{\AA}$  lightly doped ( $n \approx 2 \times 10^{16} \text{cm}^{-3}$ ) GaAs spacer layer is grown, followed by a 25  $\text{\AA}$  undoped GaAs spacer layer. These lightly doped and undoped layers have been found to greatly improve NDR behavior in double barrier structures.[4] One of the standard heterostructures has an active region consisting of a 60  $\text{\AA}$  GaAs quantum well sandwiched between two 60  $\text{\AA}$   $\text{Al}_x\text{Ga}_{1-x}\text{As}$  barriers, with  $x = 0.45$ . The other standard structure has a 45  $\text{\AA}$  GaAs well between two 25  $\text{\AA}$  AlAs barriers. Each structure is capped with a 25  $\text{\AA}$  undoped GaAs spacer layer, followed by a 500  $\text{\AA}$  lightly doped GaAs layer ( $n \approx 2 \times 10^{16} \text{cm}^{-3}$ ), and a 2500  $\text{\AA}$  heavily doped  $n$ -type GaAs top electrode.

Typical I-V curves for a standard double barrier structure with  $\text{Al}_{0.45}\text{Ga}_{0.55}\text{As}$

barriers are shown in Fig. 4.1. The curves were measured at 300 K and 77 K from a 147  $\mu\text{m}$  diameter device. NDR is displayed in both bias directions, with nearly symmetric current peak positions. The reverse bias peak-to-valley current ratio is 5:1 (1.3:1) at 77 K (300 K). The forward bias peak-to-valley ratio is 2:1 (1.3:1) at 77 K (300 K). Peak current densities are on the order of 200  $\text{A}/\text{cm}^2$  in both bias directions. We consider these results to be fairly typical for this heterostructure geometry under good system conditions (i.e., we have observed both better and worse peak-to-valley current ratios and current densities). A noticeable degradation in NDR behavior from these standard double barrier structures has been observed when material quality is relatively poor. For example, it is well known that the first few growths following a venting and bakeout of an MBE chamber tend to incorporate high background impurity levels. This effect is thought to be caused by contaminants which condense on the source material during venting. Standard double barrier structures (with  $\text{Al}_{0.45}\text{Ga}_{0.55}\text{As}$  barriers) grown shortly after a venting and bakeout of the III-V chamber usually show no NDR at room temperature, and small peak-to-valley ratios at 77 K. The sensitivity of the I-V curves from this double barrier heterostructure to system conditions makes for a useful standard.

Improved resonant tunneling characteristics have been observed from the other standard double barrier geometry described above. The improvement is largely due to the thin AlAs barriers, which allow larger tunneling currents, while presenting a high potential barrier to thermionic currents.[5] These structures typically yield room temperature NDR with peak-to-valley current ratios greater than 2:1. Peak current densities are in the range  $10^4$   $\text{A}/\text{cm}^2$ . Low temperature I-V measurements are somewhat more difficult for these structures because the high current densities require the use of small diameter devices (5 to 20  $\mu\text{m}$ ). Permanent wire bonded contacts are too large to be made to these devices without shorting to the etched

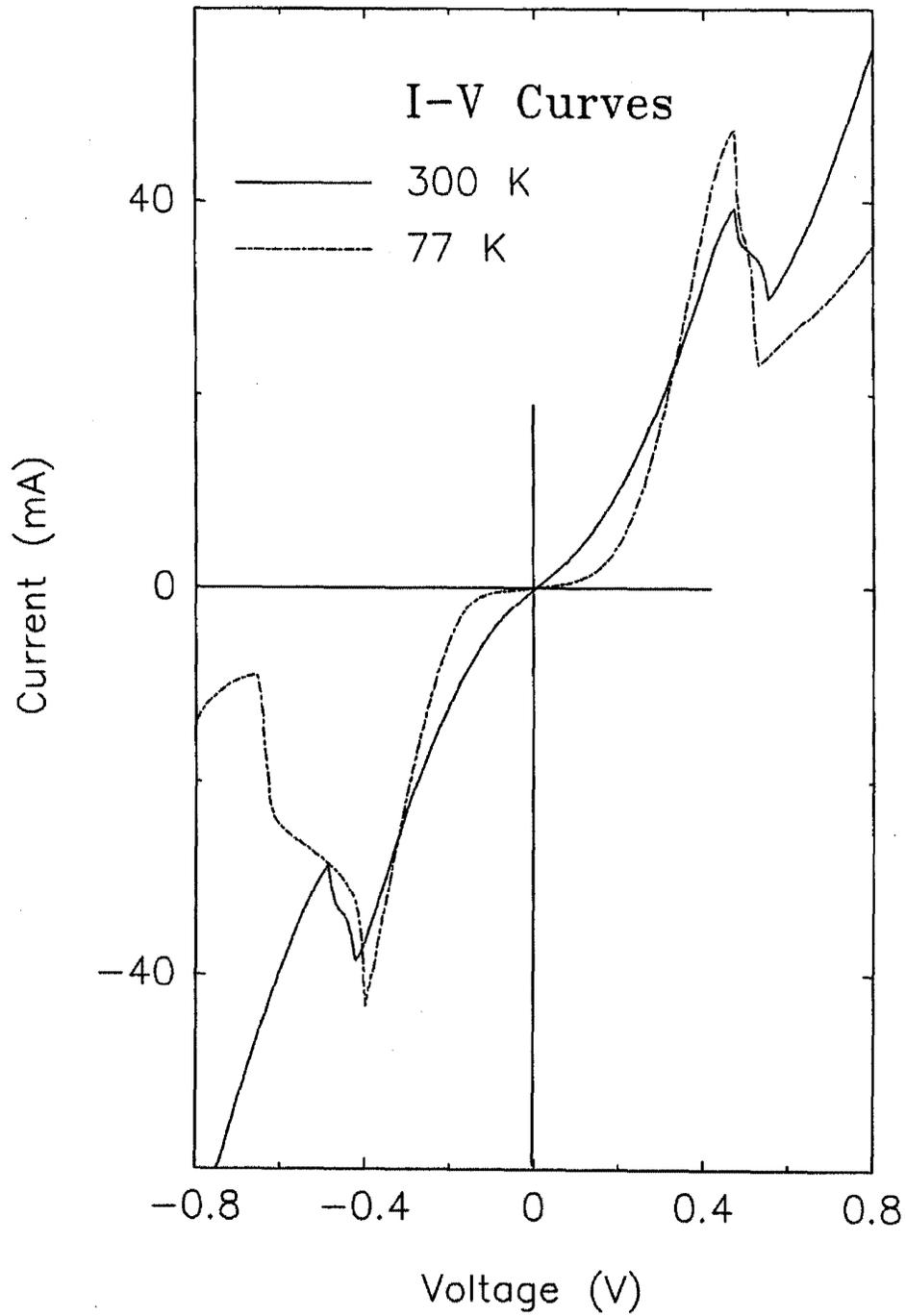


Figure 4.1: I-V curves from a double barrier tunnel structure with  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  barriers. The curves were taken from a  $147 \mu\text{m}$  diameter device. The solid (dashed) curve was taken at 300 K (77 K).

surface. Thus, immersion of the devices in liquid nitrogen is difficult. Nevertheless, these double barrier heterostructures make excellent standards, because their room temperature NDR behavior is reproducibly good under reasonable system conditions.

#### 4.2.4 Quantum Well Photoluminescence

A thin layer of GaAs sandwiched between two  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  barriers forms a quantum well for both electrons and holes. The energy difference between the electron and hole ground states in the quantum well,  $E^0$ , is larger than the energy gap of GaAs:

$$E^0 = E_g^{\text{GaAs}} + \epsilon_e^0 + \epsilon_h^0, \quad (4.1)$$

where  $E_g^{\text{GaAs}}$  is the energy gap of GaAs, and  $\epsilon_e^0$  ( $\epsilon_h^0$ ) is the confinement energy of the electron (hole) ground state in the quantum well. In a photoluminescence experiment, electrons and holes are generated by an incident photon flux (usually from a laser), and allowed to recombine, yielding photons at characteristic energies. Thus, the photoluminescence spectrum from a single quantum well should show a peak near  $E^0$ .

The quantities  $\epsilon_e^0$  and  $\epsilon_h^0$  can each be obtained through a straightforward numerical solution for the ground state of a square quantum well, using the band offsets, effective masses, and well thickness as input parameters.[6] The thicknesses of the barrier layers do not influence the confined state energies significantly.

Figure 4.2 is a typical photoluminescence spectrum taken from a sample with a 58 Å GaAs quantum well. The peak of the spectrum is centered at 1.624 eV (7633 Å), 105 meV above the GaAs energy gap. The value of  $E^0$  calculated for this structure is 1.648 eV. The width of the photoluminescence peak in Fig. 4.2 can be used as a standard for interface abruptness. A change in the GaAs quantum well thickness of 1 monolayer would result in an energy shift of 9 meV for the

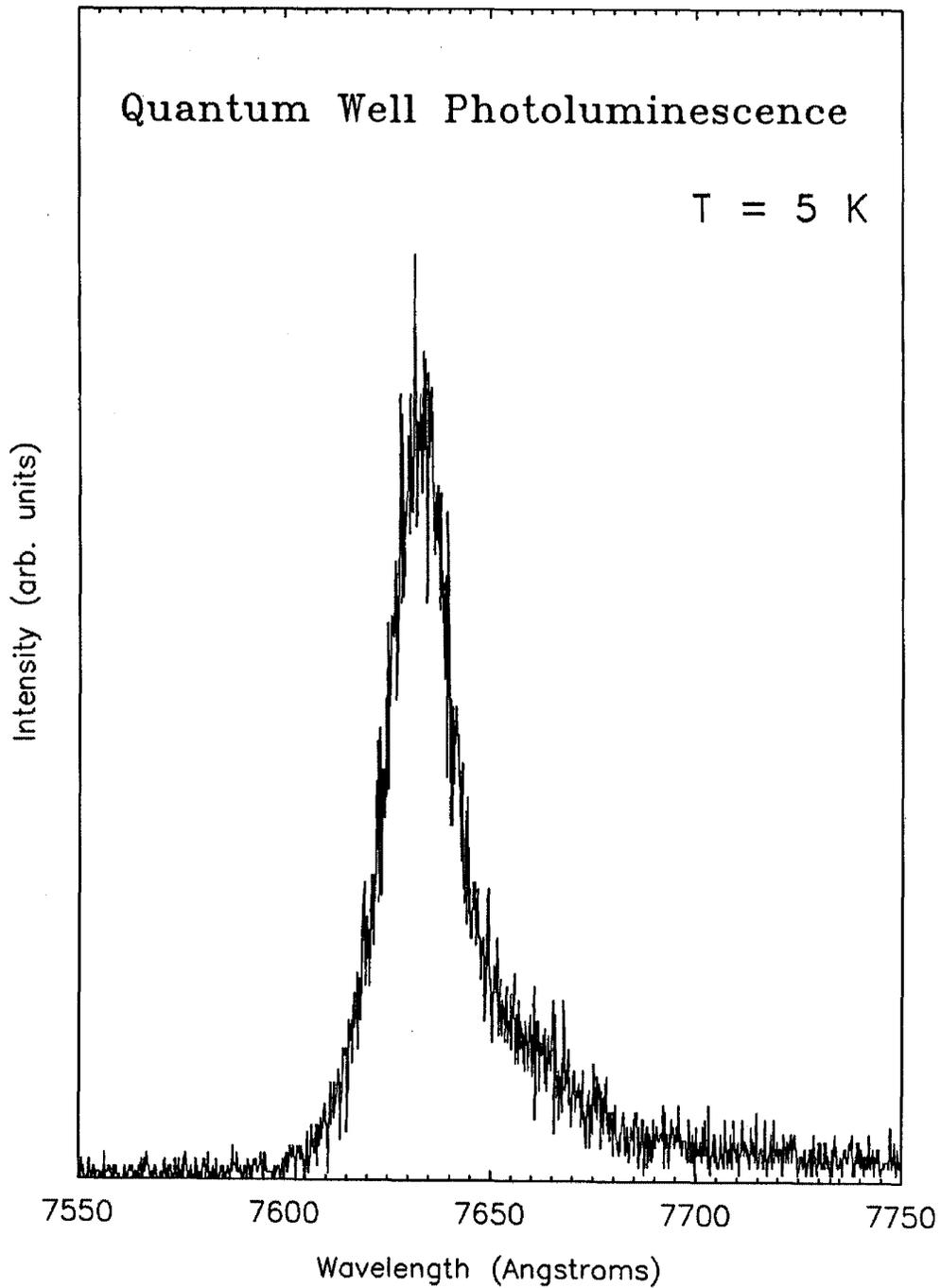


Figure 4.2: Photoluminescence spectrum of a single 58 Å GaAs quantum well at 5 K. The excitation source was set at 5145 Å with an intensity of 1 mW/cm<sup>2</sup>. The spectrum shows a narrow peak at 7633 Å (1.624 eV).

structure discussed here. Thus, the width of the photoluminescence peak can be an indication of the layer thickness fluctuations in the lateral area covered by the incident laser spot. The full width at half maximum of the peak in Fig. 4.2 is 4.7 meV (22 Å), consistent with fluctuations of one monolayer or less in the thickness of the quantum well.

#### 4.2.5 Modulation doped GaAs layers

As discussed briefly in chapter 1, a free electron distribution can be placed in an undoped GaAs layer by growing a heavily doped  $n$ -type  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  layer within a distance of 200 Å. These *modulation doped* GaAs layers have high electron mobilities for lateral transport, due to the spatial separation of electrons from ionized impurities. High electron mobility transistors (HEMTs) are based upon this concept.

Two different HEMT geometries exist.[3] 'Normal' structures begin with undoped GaAs on insulating GaAs substrates, followed by an undoped  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  spacer and the heavily doped  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  layer. Electron mobilities greater than  $10^6 \text{ cm}^2/\text{V-s}$  have been reported for these structures.[7] 'Inverted' HEMTs have the undoped GaAs grown on top of the  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  layers. These structures generally yield lower mobilities than the 'normal' versions because  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  tends to outdiffuse impurities to the surface (including dopants). These impurities provide scattering centers for the free electrons, reducing mobilities. Recently, superlattice buffer schemes have been shown to greatly reduce this problem by providing impurity-gettering interfaces in the large band gap (Al containing) material.[8]

We have grown both HEMT geometries as a means for checking material and interface quality. A home built Hall effect system has been constructed and used to measure mobilities and carrier concentrations in the HEMTs. The van der Pauw method has been used to make the Hall measurements (four corner contacts). A

magnetic field of 4000 Gauss was provided by two permanent magnets on opposite sides of the sample holder.\* For both structures, we have obtained mobilities which are considerably lower than the best reported values (approximately one order of magnitude lower), even under good system conditions. The low mobilities are probably due to nonoptimized structure parameters and relatively high background impurity levels. It should be noted that the MBE systems which produce the highest HEMT mobilities are generally dedicated to these structures.

#### 4.2.6 Characterization of Thick GaAs Films

We have characterized thick GaAs films ( $\approx 1 \mu\text{m}$ ) by Hall effect measurements and photoluminescence. These characterizations can be used as reference points for the status of the III-V chamber at any given time.

Thick GaAs layers for Hall effect measurements have usually been lightly doped  $n$ -type to avoid total depletion of the material by the surface potential. A carrier concentration of  $\approx 1 \times 10^{16} \text{ cm}^{-3}$  is obtained reproducibly for a GaAs growth rate of  $1 \mu\text{m}/\text{hour}$  and a silicon oven temperature of  $950^\circ\text{C}$ . The measured mobility for these lightly doped films is typically  $4000 (15,000) \text{ cm}^2/\text{V-s}$  at  $300 (77) \text{ K}$ , which is comparable with the best reported mobility for MBE grown films.[9]

Photoluminescence spectra from bulk GaAs films typically show two major peaks. The higher energy peak is near the band gap of GaAs, and is attributable to free exciton luminescence. The lower energy peak has been identified as an exciton bound to the carbon acceptor level.[9]

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\*An electromagnet has recently been installed to replace the permanent magnets.

## 4.3 Determination of the GaAs/AlAs Valence Band Offset

This section presents results from a study of the GaAs/AlAs valence band offset by x-ray photoemission spectroscopy. The independence of the band offset with respect to growth sequence (commutativity) is verified.

### 4.3.1 Motivation and Background

Band offsets are extremely important in the design of most semiconductor heterostructure devices, because of their impact on potential profiles in the structures. In many devices, predicted behavior is drastically changed by even small changes in the band offsets. Furthermore, band offsets are physically interesting because of their fundamental nature.

Although the GaAs/AlAs material system is the most extensively studied of all of the heterojunctions, published experimental results for the GaAs/AlAs valence band offset,  $\Delta E_v$ , vary significantly. Even recent experimental papers have reported a range of values from 0.36 eV to 0.55 eV for  $\Delta E_v$ . [10,11,12,13,14] Furthermore, the commutativity of the band offset has been an unresolved experimental issue. [10,11]

### 4.3.2 X-ray photoemission spectroscopy

X-ray photoemission spectroscopy (XPS) has become a well-established technique for measuring valence band offsets over the last few years. Several heterojunction material systems have been studied, including GaAs/AlAs, [10,11] HgTe/CdTe, [15] InAs/GaSb, [16] and GaSb/AlSb. [17] The applicability of XPS to band offset measurements is derived from the surface sensitivity of the technique. A typical escape depth for photoemitted electrons is 25 Å. It is usually

straightforward to maintain a constant potential profile within this distance of a heterojunction interface (i.e., band bending effects can be made negligible over this distance).

The XPS band offset measurement is usually performed on a heterojunction interface which is near the surface of a sample so that the photoemitted electrons originate from regions near the interface. Our MBE system is ideal for these measurements because heterojunction samples can be transferred to the ESCA chamber for XPS analysis without removing them from ultrahigh vacuum conditions. Thus, contaminants are not introduced on the surfaces of the samples, eliminating the possibility of potential changes due to chemical bonding of the surface atoms. We have found that GaAs and AlAs samples can be left in ultrahigh vacuum conditions for 48 hours before surface contaminants can be detected by Auger electron spectroscopy.

Three different samples are required for an XPS measurement of the valence band offset between two semiconductors, A and B. The photoemission spectrum of a bulk sample of semiconductor A is used to obtain the energy separation between its valence band edge and a convenient core level,  $E_v^A - E_{core}^A$ . A similar sample of semiconductor B is used to obtain the energy separation between its valence band edge and a core level,  $E_v^B - E_{core}^B$ . Finally, a sample with a heterojunction interface between semiconductors A and B near the surface is scanned to obtain  $E_{core}^A - E_{core}^B$ . These three energy separations then give the valence band offset,  $E_v^A - E_v^B$ .

### 4.3.3 Samples

Four types of samples were grown in the III-V chamber for the XPS measurement of the GaAs/AlAs valence band offset. Fig. 4.3 depicts these four sample geometries schematically. All of the samples were grown on conductive GaAs

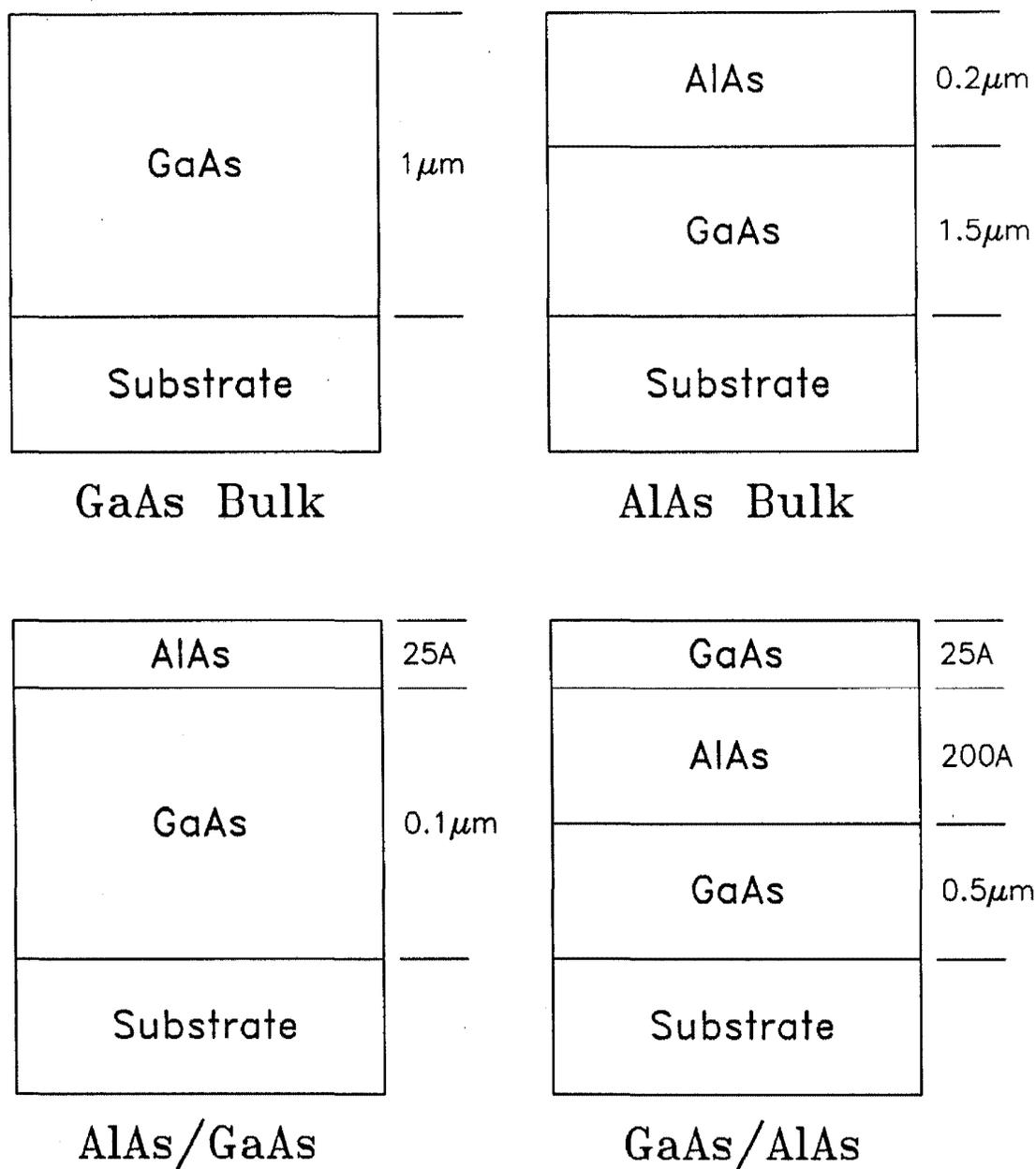


Figure 4.3: Schematic diagrams of the growth sequences used to grow the four different types of samples required for the XPS band offset measurement. The upper left (right) diagram depicts the bulk GaAs (AlAs) sample. The two types of heterojunction samples, AlAs/GaAs and GaAs/AlAs, are depicted in the lower left and lower right corners, respectively.

(100) substrates at 600°C. The substrates were cleaned prior to growth by the procedure described in section 4.2.1. (As)/(group III) flux ratios and growth rates were selected by the method discussed in section 4.2.2. All of the samples were lightly doped *n*-type with Si ( $n \approx 1 \times 10^{16} \text{ cm}^{-3}$ ) to avoid sample charging effects. Heavy doping was avoided because short surface depletion lengths can result in a significant amount of band bending near the surface.

Thick GaAs layers ( $>1 \mu\text{m}$ ) were grown for measurements of the energy separation between the valence band edge and the Ga3*d* core level in GaAs. Thick AlAs layers ( $>2000 \text{ \AA}$ ) were used to obtain the energy spacing between the valence band edge and the Al2*p* core level in AlAs. To check the commutativity of the band offset, two types of heterojunction samples were grown: thin AlAs (25 Å) on thick GaAs (1000 Å) and thin GaAs (25 Å) on thick AlAs (100, 200, or 500 Å). These heterojunctions were used to measure the energy separation between the Ga3*d* level in GaAs and the Al2*p* level in AlAs.

#### 4.3.4 Results

XPS measurements on GaAs and AlAs bulk films yielded

$$E_{\text{Ga}3d}^{\text{GaAs}} - E_{\text{v}}^{\text{GaAs}} = 18.73 \pm 0.05 \text{ eV} \quad (4.2)$$

and

$$E_{\text{Al}2p}^{\text{AlAs}} - E_{\text{v}}^{\text{AlAs}} = 72.71 \pm 0.04 \text{ eV}. \quad (4.3)$$

For the AlAs on GaAs heterojunction, the core level separation was found to be:

$$E_{\text{Al}2p}^{\text{AlAs}} - E_{\text{Ga}3d}^{\text{GaAs}} = 54.43 \pm 0.02 \text{ eV}. \quad (4.4)$$

It follows that the valence band offset for AlAs on GaAs is  $0.45 \pm 0.07 \text{ eV}$ . The GaAs on AlAs heterojunction yielded a core level separation:

$$E_{\text{Al}2p}^{\text{AlAs}} - E_{\text{Ga}3d}^{\text{GaAs}} = 54.45 \pm 0.02 \text{ eV}, \quad (4.5)$$

leading to a value of  $0.47 \pm 0.07$  for the valence band offset. These results indicate that the band offset is commutative within experimental uncertainties, as expected for ideal interfaces. The measured GaAs/AlAs valence band offset is  $0.46 \pm 0.07$  eV. This value of the band offset is in agreement with most of the recent published results for the GaAs/AlAs (100) interface.

## 4.4 Tunneling Times in GaAs/AlAs Double Barrier Heterostructures

This section contains results from an investigation of electron tunneling times in double barrier heterostructures by photoluminescence excitation correlation spectroscopy.

### 4.4.1 Motivation and Background

One of the major reasons for the current interest in double barrier tunnel structures is their potential for high speed applications. Due to the small characteristic dimensions of these structures, it is possible for charge carriers to traverse the active regions of the devices in very short times. As was discussed in section 1.3, tunneling times have been the subject of much debate for several years. Many different theoretical approaches have been applied to this problem, with conflicting results.[18,19,20,21,22,23,24] However, most of the theoretical predictions agree that the theoretical limit is shorter than 50 ps and longer than 1 fs.

Experimental measurements of tunneling times are difficult because the time scales are shorter than those which can be accessed by conventional electronic means. Hence, optical excitation and sampling techniques are usually needed. In fact, most of the published experimental measurements of double barrier response times have been either optical or optoelectronic.[25,26,27,28]

#### 4.4.2 Measurement Technique

The photoluminescence (PL) intensity,  $I_{pl}$ , from the quantum well of a double barrier heterostructure is given by:

$$I_{pl} \propto n \times p, \quad (4.6)$$

where  $n$  and  $p$  are the number of electrons and holes, respectively, in the quantum well. If electrons and holes are placed in the quantum well by a short excitation pulse (at an energy above the quantum well peak energy), then the PL peak intensity will decay with time as the carriers escape from the well. Hence, "time-resolved" photoluminescence can be used to measure tunneling rates out of the quantum well when tunneling is the dominant escape mechanism for the carriers.

The most obvious technique for performing time-resolved PL is to generate carriers with short laser pulses and detect the luminescence with a very fast detector. This method has been recently demonstrated to yield a reasonable tunneling time measurement.[26] However, signal-to-noise problems and detector (streak camera) response limitations prevented measurement of tunneling times shorter than 60 ps.

We have used photoluminescence excitation correlation spectroscopy (PECS) to measure tunneling times in GaAs/AlAs double barrier heterostructures with varying barrier thicknesses. The PECS technique has been described in detail elsewhere.[29] A very brief description is given here. A colliding pulse mode-locked ring dye laser is used to generate a train of very short pulses (200 fs full width at half maximum). This beam is then split into two pulse trains. Next, one set of pulses is forced to traverse an extra distance, delaying it with respect to the other pulse train by a short time,  $\gamma$  ( $-500 \text{ ps} \leq \gamma \leq 500 \text{ ps}$ ). The two beams are then chopped at different frequencies,  $f_1$  and  $f_2$ , and focused down to a spot on the sample surface. Finally, the photoluminescence signal from the sample

is synchronously detected through a lock-in amplifier set to the sum of the two chopping frequencies,  $f_1 + f_2$ . It can be shown that the photoluminescence signal at the sum frequency decays with increasing  $\gamma$  exponentially, with a time constant equal to the characteristic carrier escape time.

### 4.4.3 Samples

The growth sequence used to produce samples for the tunneling time vs. barrier thickness investigation is depicted schematically in Fig. 4.4. All of the samples were grown on GaAs (100) substrates at 600°C. The substrates were cleaned prior to growth by the procedure described in section 4.2.1. (As)/(group III) flux ratios and growth rates were selected by the method discussed in section 4.2.2. None of the samples were intentionally doped.

Growth commenced with a 0.5  $\mu\text{m}$  GaAs layer, followed by a superlattice buffer layer consisting of five periods of  $\text{Al}_{0.35}\text{Ga}_{0.65}\text{As}$  (50 Å) and GaAs (500 Å).<sup>\*</sup> A 0.7  $\mu\text{m}$  GaAs layer was grown next to eliminate any optical effects from the superlattice. The GaAs/AlAs double barrier structure was then grown symmetrically, with a GaAs well thickness of 58 Å. Seven different samples were studied, with AlAs barrier thicknesses of 16,22,28,34,34,48, and 62 Å. Finally, a 300 Å GaAs cap layer was grown. This thickness was sufficient to prevent quantum confinement effects in the cap layer, while allowing optical probing of the quantum well.

Barrier and well thicknesses were determined from bulk growth rates. However, high-resolution transmission electron microscopy (TEM) was used to measure the layer thicknesses in the 16 Å barrier sample and one of the 34 Å barrier samples. Fig. 4.5 is a high-resolution TEM print of the double barrier region in the 34 Å barrier sample. The TEM print confirms the 34 Å AlAs barrier thickness, with

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<sup>\*</sup>The intention in growing this buffer layer was to improve material quality. However, we have found no difference in experimental results with the superlattice deleted.

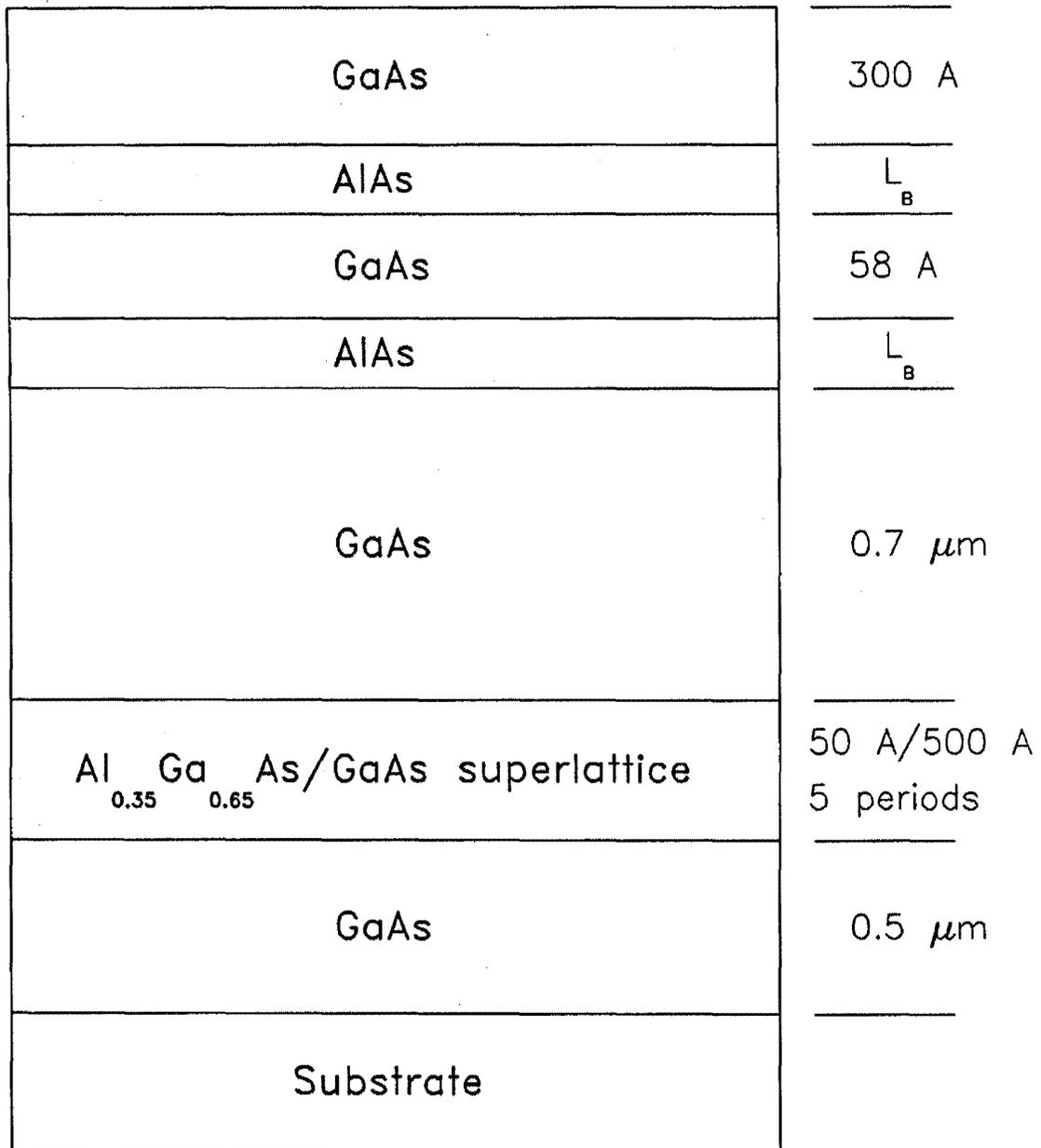


Figure 4.4: Schematic diagram depicting the growth sequence used to produce double barrier heterostructures for the optical tunneling time measurement. The AlAs barrier thickness,  $L_B$ , was varied, with all other growth parameters held constant.

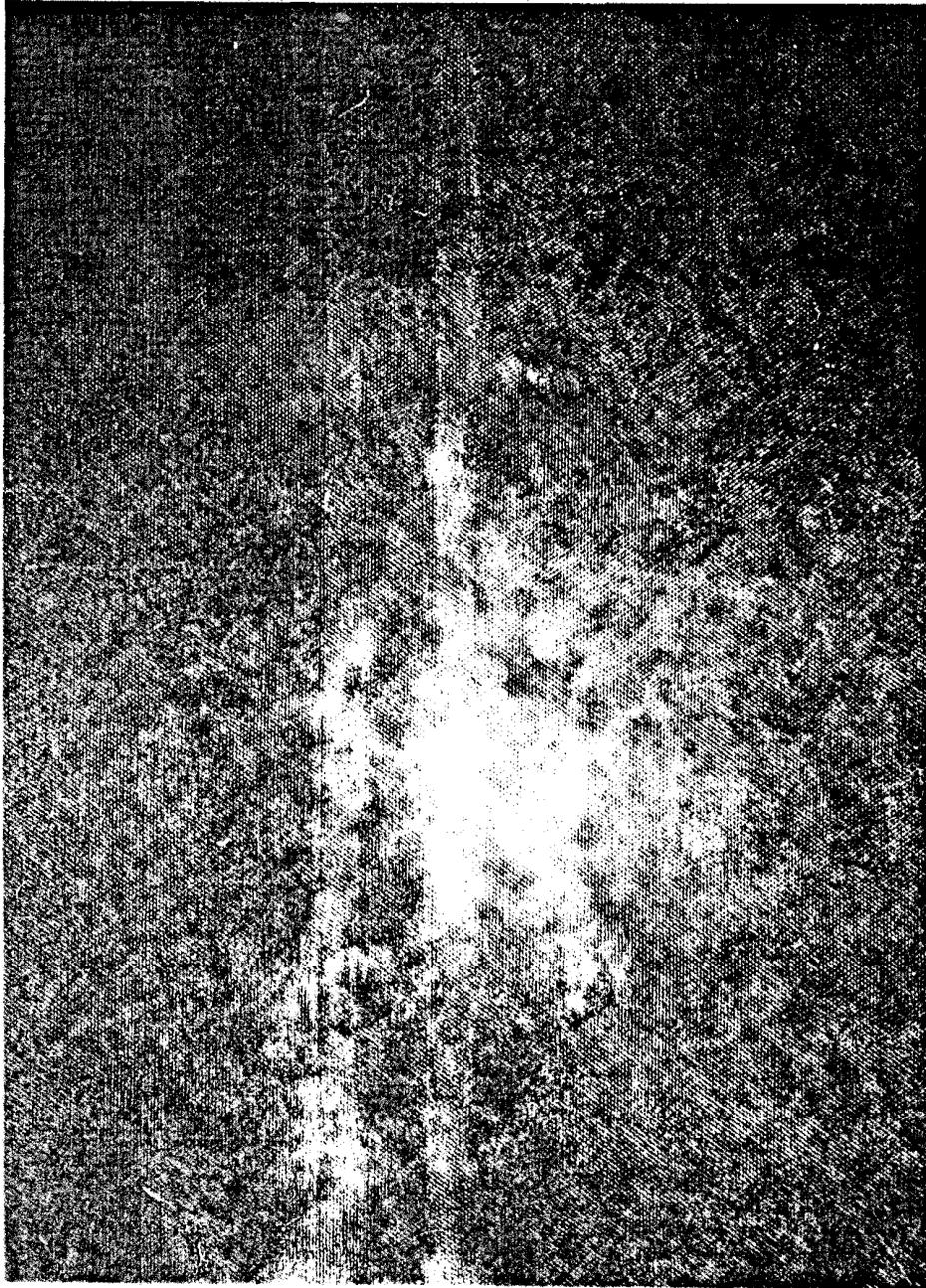


Figure 4.5: High-resolution TEM photograph of the double barrier region of a sample with 34 Å AlAs barriers and a 58 Å GaAs quantum well. The layer thicknesses can be obtained by counting monolayers, to an uncertainty of one monolayer per interface.

an uncertainty of two monolayers.[30] Possible lateral fluctuations in layer thicknesses have been investigated by checking the linewidths displayed in one beam photoluminescence. The resulting quantum well peaks are narrow ( $\leq 6$  meV), consistent with fluctuations of 1 monolayer or less in layer thickness.

A heterostructure with symmetric barriers consisting of three 8.5 Å AlAs layers, separated by two 8.5 Å GaAs layers has also been grown for the PECS experiment. The structure was grown with a 49 Å GaAs quantum well, and a 300 Å GaAs cap layer. This double barrier geometry has been shown to yield the highest reported peak-to-valley ratio for GaAs/Al<sub>x</sub>Ga<sub>1-x</sub>As resonant tunneling structures.[4]

#### 4.4.4 Results

Each of the samples discussed in the previous section displayed a clear photoluminescence peak attributable to the lowest energy confined state in the quantum well. For the thinnest AlAs barriers, the photoluminescence intensity was relatively weak due to the rapid escape of tunneling electrons out of the well. For each of the samples with varying AlAs barrier thicknesses, scans were made of the sum frequency photoluminescence intensity,  $I_{sum}$ , as a function of delay time,  $\gamma$ . These scans showed a simple decaying exponential dependence of  $I_{sum}$  with increasing  $\gamma$ . The characteristic decay times of  $I_{sum}$  were identified as the times required for electrons to tunnel out of the quantum wells.

For the sample with the thinnest AlAs barriers (16 Å), the tunneling time was measured to be  $\approx 12$  ps, the shortest such time ever reported. The tunneling time for the samples with 34 Å barriers was measured to be  $\approx 800$  ps. A simple exponential dependence of tunneling time on barrier thickness was observed for samples with barrier thicknesses between 16 and 34 Å. This result is consistent with a straightforward method of calculating tunneling times for double barrier structures. In this approach, the electron tunneling time,  $\tau$ , is related to the

width of the resonance in the transmission coefficient,  $\Gamma$ , through the uncertainty principle:

$$\tau = \frac{\hbar}{\Gamma}. \quad (4.7)$$

This method is particularly attractive because the transmission coefficient for double barriers is well known and easily calculated.

The sample with barriers consisting of three 8.5 Å AlAs layers separated by two 8.5 Å GaAs layers was found to display an electron tunneling time of  $350 \pm 60$  ps out of the 49 Å quantum well.

#### 4.4.5 Ongoing Experiments

Further PECS experiments on GaAs/AlAs double barrier heterostructures are currently being pursued. Doped structures have been grown and prepared as two terminal electrical devices with thin (60 Å) Au/Ge contacts on the tops of the mesas. These devices can be biased into the NDR region, and probed optically to measure tunneling times under conditions in which significant tunneling current is present.

A set of undoped structures with progressively narrower GaAs quantum wells has been grown. As the wells become thinner, it is expected that the quantum well conduction band states will rise in energy until they are comparable to the AlAs X-point energy. At this point, significant mixing between the quantum well state and the AlAs X-point state is expected. The onset of this mixing should cause a sharp transition in the observed photoluminescence decay behavior.

## 4.5 Electron Coherence in Resonant Tunneling Structures

This section presents a study of electron tunneling in triple barrier heterostructures. The results provide evidence for a coherent model (as opposed to a sequential model) of electron tunneling through thin AlAs barriers.

### 4.5.1 Motivation and Background

Double barrier tunnel structures are the subject of a considerable amount of current research. The first proposal of negative differential resistance (NDR) in these structures was based on a model of tunneling in which the electron wavefunctions are *coherent* across the entire structure.[31] In this context, coherent is taken to mean that the electrons retain their phase information throughout the tunneling process. In more intuitively meaningful terms, coherent electrons are not scattered as they tunnel through the double barrier structure. In the coherent picture of double barrier tunneling, the electron transmission coefficient has a resonance, similar to the Fabry-Perot effect for optical waves.

Recently, Luryi[23] has proposed that a sequential tunneling model can adequately explain the observation of NDR in double barriers. The basis of Luryi's argument is that electron tunneling from a 3-dimensional set of states to a 2-dimensional set of states will always show NDR if the total energy and parallel wavevector of each tunneling electron is conserved. Under these conditions, NDR occurs when the conduction band edge in the negatively biased electrode is raised above the 2-dimensional subband minimum in the quantum well by an applied voltage. The basic difference between the two tunneling models is that the electrodes and quantum well are treated as independent sets of states in the sequential model. In the coherent model, the electron states are extended throughout the dif-

ferent regions of the heterostructure. The two models are thought to be virtually indistinguishable in double barrier I-V curves.

We have grown triple barrier heterostructures in an attempt to resolve the coherent vs. sequential tunneling issue. Electrons tunneling through these structures must pass between two quantum wells. Hence, sequential tunneling conditions become more stringent, because the electrons must hop from one set of 2-dimensional states to another. In fact, if the different regions of the triple barrier heterostructure are treated independently, tunneling currents can only become significant when a subband minimum in the first quantum well aligns precisely with a subband minimum in the second well. Thus, we expect NDR to be difficult to achieve if electron tunneling between the two wells is sequential in nature. In contrast, the coherent tunneling model allows the electron wavefunctions to penetrate from one quantum well to the next, so that NDR behavior should be similar to the double barrier case (provided that the middle barrier is sufficiently thin).

### 4.5.2 Samples

Figure 4.6 is a schematic diagram of the growth sequence used for the triple barrier heterostructure samples. All of the samples were grown on conductive GaAs (100) substrates at 600°C. Growth commenced with a 0.5  $\mu\text{m}$  heavily doped *n*-type GaAs layer. Next, a 500 Å lightly doped ( $n = 2 \times 10^{16} \text{ cm}^{-3}$ ) GaAs spacer layer was grown, followed by a 25 Å undoped GaAs spacer. The symmetric triple barrier portion of the structure was then grown; it consisted of 30 Å AlAs outer barrier layers, 54 Å GaAs quantum wells, and an AlAs middle barrier with a variable thickness. Undoped (25Å) and lightly doped (500 Å) GaAs spacer layers were grown on top of the triple barrier region. Finally, a 2500 Å heavily doped *n*-type GaAs cap layer was deposited. Four samples were studied, with middle barrier thicknesses of 0, 3, 6, and 12 monolayers.

## Triple Barrier Heterostructure

GaAs, $n=5 \times 10^{18} \text{cm}^{-3}$	0.25 $\mu\text{m}$
GaAs, $n=2 \times 10^{16} \text{cm}^{-3}$	500 Å
GaAs, undoped	25 Å
AlAs, " "	30 Å
GaAs, " "	54 Å
AlAs, " "	W
GaAs, " "	54 Å
AlAs, " "	30 Å
GaAs, " "	25 Å
GaAs, $n=2 \times 10^{16} \text{cm}^{-3}$	500 Å
GaAs, $n=5 \times 10^{18} \text{cm}^{-3}$	0.5 $\mu\text{m}$
Substrate	

Figure 4.6: Schematic diagram depicting the growth sequence used to produce GaAs/AlAs triple barrier tunnel structures. The middle barrier thickness,  $W$ , was varied, with all other growth parameters held constant.

The samples were prepared as two terminal electrical devices by standard photolithographic and wet etching techniques. Wire bonds were attached to the devices for liquid nitrogen temperature experiments.

### 4.5.3 Results

All four of the samples studied displayed I-V curves with NDR, and the three thinnest middle barrier (0,3, and 6 monolayers) samples had multiple resonances. These results suggest that the electron wavefunctions do penetrate across the middle barrier region, and are inconsistent with the sequential picture of tunneling as proposed by Luryi. Furthermore, the resonances are extremely strong. Fig. 4.7 is an I-V curve taken from the sample with a 3 monolayer barrier at 77 K. The curve displays three distinct NDR regions, with a peak-to-valley current ratio of 19.3:1 for the second peak. This is comparable to the largest peak-to-valley ratio ever reported for a GaAs/AlAs structure,[4] and is higher than any of those reported for conventional GaAs/AlAs double barrier heterostructures. These results clearly indicate that the electron wavefunction is coherent across the *middle* barrier layer.

The samples with 3 and 6 monolayer middle barriers both show stronger NDR behavior than the sample with no middle barrier. However, the sample with a 12 monolayer middle barrier shows only one degraded NDR region in its I-V curve. This poor performance may indicate a loss of coherence across the thicker middle barrier. A possible explanation for this result is the longer tunneling time expected for tunneling through the thicker barrier. Longer time scales for tunneling may make scattering more likely, reducing the probability of coherent transport.

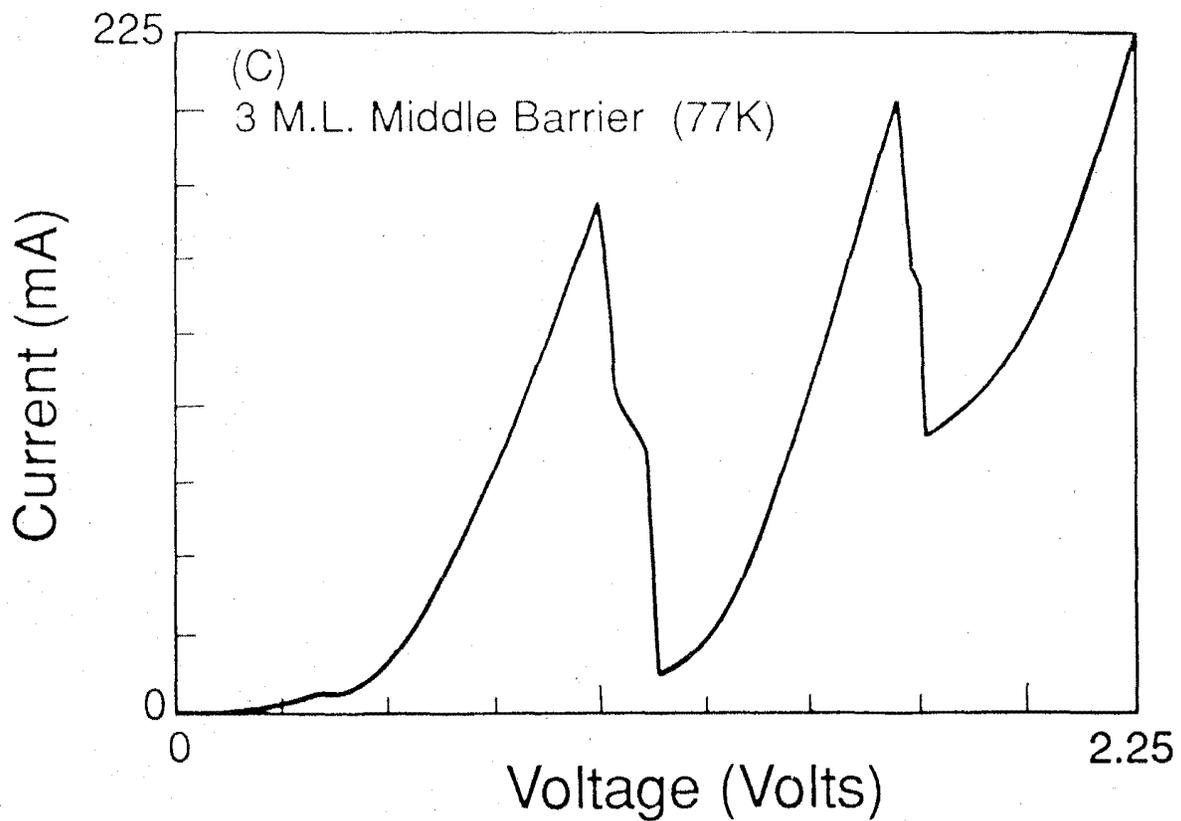


Figure 4.7: I-V curve from a GaAs/AlAs triple barrier tunnel structure, taken at 77 K. The AlAs middle barrier thickness is 3 monolayers. The curve displays three distinct NDR regions, with a peak-to-valley current ratio of 19.3:1 for the second NDR region.

## 4.6 Growth of InAs on GaAs substrates

This section presents the development of a method for growing high quality thick InAs films on GaAs substrates.

### 4.6.1 Motivation and Background

Combinations of the nearly lattice-matched semiconductors InAs, GaSb, and AlSb are promising for a number of interesting heterostructures. Some of these structures have already been realized, as discussed previously in section 4.1.2. However, lattice-matched substrates for these materials are a problem. Even the highest quality InAs substrates have etch pit densities (dislocations) that are more than ten times higher than those of standard GaAs substrates. Reasonably high quality GaSb substrates can be obtained, but cleaning procedures for these substrates have not been well studied. Furthermore, both InAs and GaSb are considerably more expensive than GaAs (by a factor of approximately 6). AlSb is not stable to atmospheric exposure. Hence, a technique for depositing a high quality buffer layer of InAs, GaSb, or AlSb on GaAs is highly desirable.

The difficulty with growing a thick buffer layer on a poorly lattice matched substrate is that relaxation of the buffer material to its natural lattice constant occurs through dislocation formation. These dislocations tend to thread through the entire buffer layer, with adverse effects on optical and electrical properties. Recently, it has been reported that a short period strain layered superlattice can reduce the number of dislocations in extremely thick InAs films (6  $\mu\text{m}$ ) grown on GaAs substrates.[32] The dislocation densities were inferred from measurements of electron mobilities. However, MBE growth rates are usually limited to about 1  $\mu\text{m}/\text{hour}$ , so that extremely thick buffers are impractical. We have attempted to obtain electron mobilities comparable to those reported by Kalem et al.[32]

for reasonable InAs buffer layer thicknesses ( $2 \mu\text{m}$ ) on GaAs. Growth parameters such as substrate temperature, As/In flux, and superlattice buffer layers have been varied, with *in situ* monitoring by RHEED, optical pyrometry, and residual gas analysis (RGA).

#### 4.6.2 Growth and In Situ Analysis

Figure 4.8 is a schematic layer diagram of the growth sequence used to deposit InAs layers on GaAs substrates. All of the samples were grown on insulating GaAs (100) substrates. The substrates were cleaned prior to growth by the procedure described in section 4.2.1. Initially, a  $0.5 \mu\text{m}$  undoped GaAs layer was deposited at a substrate temperature of  $600^\circ\text{C}$ . The growth was then interrupted (As flux only) while the substrate temperature was lowered to that desired for the InAs layer. Two different superlattice buffers at the GaAs/InAs interface were studied. Some of the samples had a five period  $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}/\text{GaAs}$  (2 monolayer/2 monolayer) superlattice only. Other samples had an additional five period  $\text{InAs}/\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$  ( $100 \text{ \AA}/6 \text{ \AA}$ ) superlattice grown immediately after the first superlattice. Finally, a  $2 \mu\text{m}$  undoped InAs layer was grown.

Several different substrate temperatures were used for the InAs layers, spanning the range  $490\text{--}550^\circ\text{C}$  as measured by the optical pyrometer. The RHEED pattern from the InAs surface was observed to indicate a transition from a  $2 \times 4$  reconstructed surface to a  $4 \times 2$  reconstructed surface at a substrate temperature of  $530\text{--}535^\circ\text{C}$ . This transition is believed to be due to a change from an As-stabilized surface at low temperatures to an In-stabilized surface at high temperatures. The  $\text{As}_2/\text{In}$  flux ratio was estimated to be between 10:1 and 20:1 for all of the samples by measuring RGA peak heights.

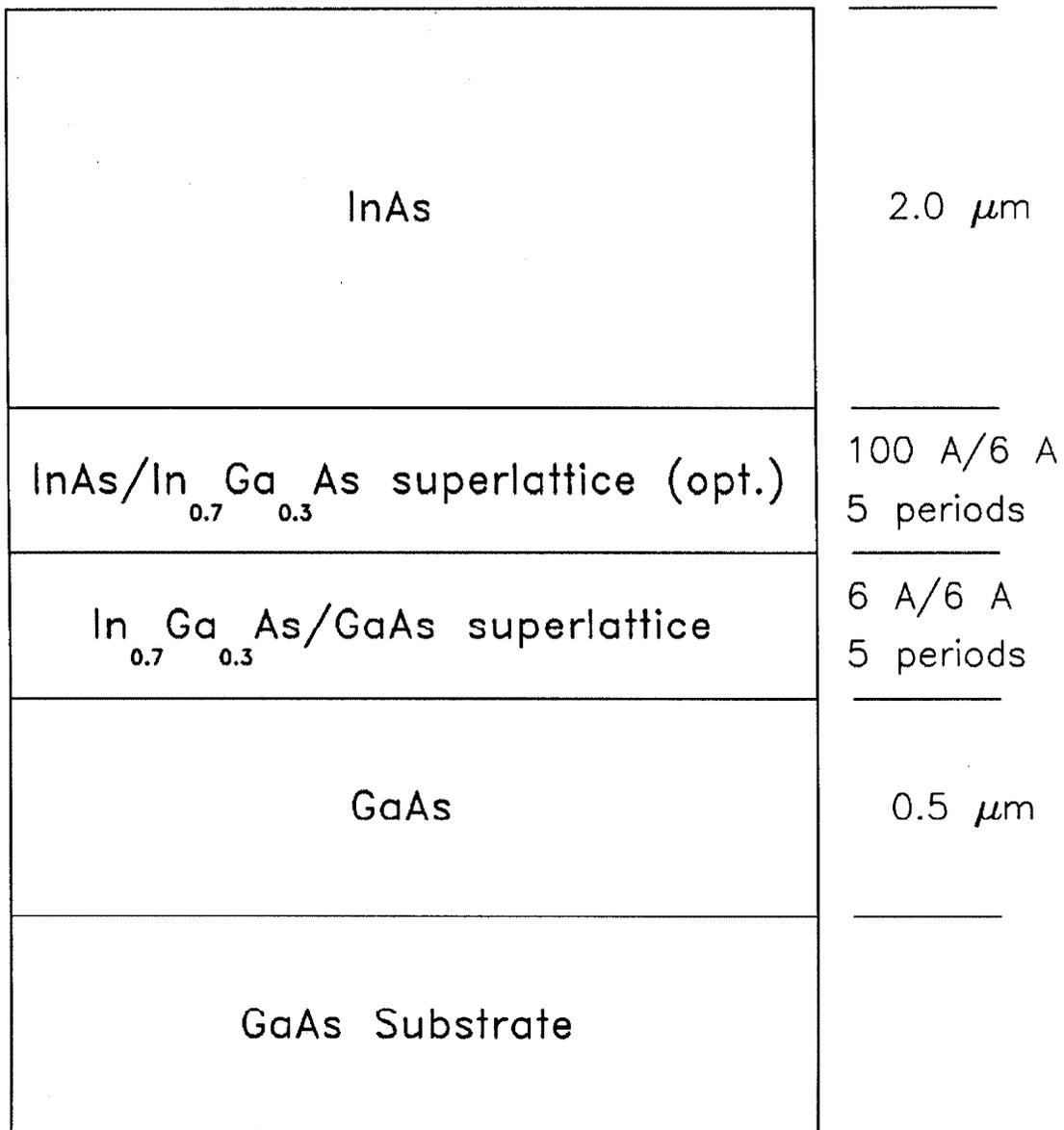


Figure 4.8: Schematic diagram depicting the growth sequence used to deposit thick InAs layers on GaAs. The second ( $\text{InAs}/\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ ) superlattice was used for a few of the samples.

### InAs RHEED oscillations

RHEED intensity oscillations have been observed for InAs layers grown under As-stabilized conditions. These oscillations in diffraction intensity are believed to be caused by periodic surface roughness changes which occur during deposition of each monolayer of material.[33] Thus, the oscillations can be used to calibrate growth rates for thin layers. Furthermore, strong oscillations are usually indicative of good layer-by-layer growth. Fig. 4.9 shows the RHEED intensity oscillations observed during growth of an InAs layer. The RHEED intensity was measured by placing one end of a thick fiber optic cable on the phosphor RHEED screen, and directing the other end of the cable to a photodiode. A chart recorder was used to record the signal from the photodiode as a function of time. The data in Fig. 4.9 were obtained by interrupting the InAs growth for one minute after  $0.5 \mu\text{m}$  of material had been deposited. The specular spot in the 2-fold RHEED pattern ([110]-azimuth) was chosen as the point seen by the fiber optic cable. Over twenty oscillations can be seen in Fig. 4.9, indicating a growth rate of  $3.17 \text{ \AA/s}$ . To our knowledge, these are the most intense RHEED oscillations ever reported for InAs growth.[34]

#### 4.6.3 Characterization

All of the InAs samples grown under As-stabilized conditions had good surface morphology, though not quite as good as is usually obtained for high quality GaAs growth. Samples grown under In-stabilized conditions had rough hazy surfaces.

Hall effect measurements were made at 77 and 300 K on all of the InAs layers. Van der Pauw (four corner) contacts were made by evaporating Au/Ge through a foil mask. The homemade Hall apparatus was calibrated against results from a Hall effect experiment at Hughes Research Labs. All of the samples were found to be *n*-type, with background carrier concentrations in the  $10^{16} \text{ cm}^{-3}$  range.

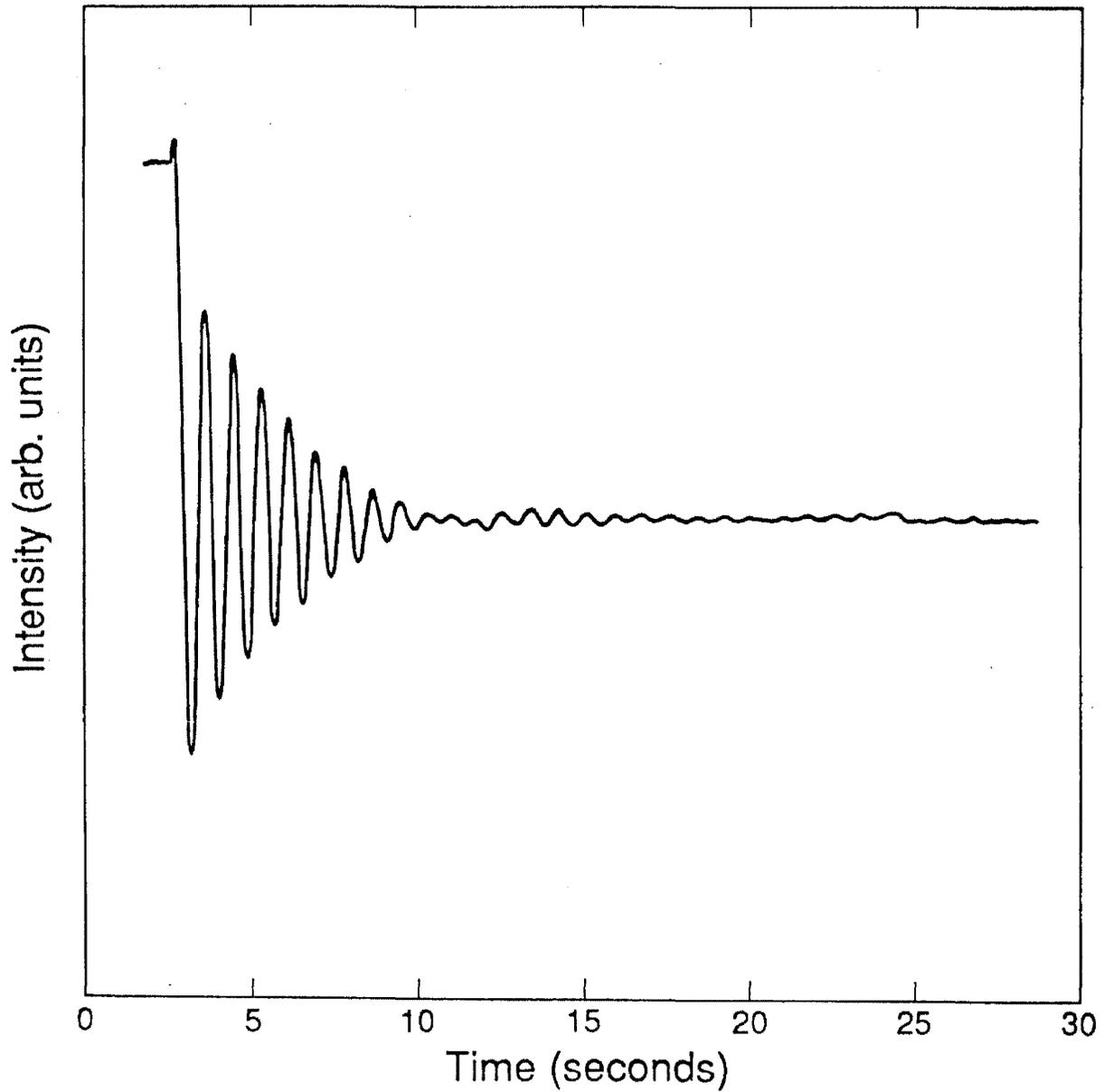


Figure 4.9: RHEED intensity oscillations observed during the growth of InAs. The oscillations were obtained by interrupting the growth (As flux only) after  $0.5 \mu\text{m}$  of InAs had been deposited.

The highest room temperature electron mobility observed was  $18,900 \text{ cm}^2/\text{V-s}$ , comparable to the results obtained by Kalem *et al.* on much thicker ( $6 \mu\text{m}$ ) layers. The best 300 K mobilities were obtained from samples grown under As-stabilized conditions with only one short period superlattice interface layer. We believe that the lowest number of dislocations in the InAs film is achieved under these growth conditions. In contrast, samples grown under Ga-stabilized conditions yielded the best 77 K mobilities ( $35,500 \text{ cm}^2/\text{V-s}$ ), independent of whether one or two superlattice interface layers were used. The 77 K results can be explained by measured background carrier concentrations, which were found to be lower for samples grown under Ga-stabilized conditions by a factor of four. The difference in background doping is probably attributable to lower impurity incorporation during growth under Ga-stabilized conditions.

X-ray diffraction was performed on an InAs sample grown under As-stabilized conditions with two superlattice interface layers. The lattice constant of the film was found to be  $6.08 \pm 0.04 \text{ \AA}$ . This result is close to the bulk InAs lattice constant of  $6.06 \text{ \AA}$ , and indicates that the InAs film is almost completely relaxed. However, the x-ray diffraction peak was found to be extremely broad for a  $2 \mu\text{m}$  film, indicating a variation in lattice constant. The broadening may be caused by the portion of the InAs layer near the GaAs interface, which is probably heavily dislocated.

## 4.7 Summary of Conclusions

A number of standard GaAs/ $\text{Al}_x\text{Ga}_{1-x}\text{As}$  growths have been characterized, including double barrier tunnel structures, single quantum wells, HEMT's, and bulk GaAs. These structures have been used as reference points for the status of the III-V chamber at various times. Under good system conditions, most of

the standard structures yield results comparable with the best results reported for MBE growth.

A measurement of the GaAs/AlAs valence band offset has been made by x-ray photoemission spectroscopy (XPS). Samples for this experiment were produced in the III-V growth chamber, and transferred under ultrahigh vacuum to the surface analysis chamber. This arrangement is ideal for the surface sensitive XPS technique because the sample surface is not contaminated by exposure to atmosphere. The measured GaAs/AlAs valence band offset is commutative, with a value of  $0.46 \pm 0.07$  eV.

Double barrier heterostructures have been produced in the III-V chamber for a measurement of electron tunneling times by photoluminescence excitation correlation spectroscopy. The structures were grown with thin (300 Å) GaAs cap layers to permit optical probing of the quantum well region. Decay times as short as 12 ps have been measured for electrons escaping from a 58 Å GaAs quantum well surrounded by two 16 Å AlAs barrier layers. The electron tunneling times are found to depend exponentially upon barrier thickness, in good agreement with a calculation based on resonance widths in the electron transmission coefficient.

A study of coherent vs. sequential tunneling in triple barrier GaAs/AlAs heterostructures has been performed. For thin AlAs middle barriers (<12 monolayers), these structures yield I-V curves with multiple strong NDR regions. Particularly large peak-to-valley current ratios are observed (19.3:1 at 77 K), indicating that the electron wavefunctions are coherent across the middle barrier. A loss of coherence for thick AlAs middle barriers is suggested.

A method for growing high quality 2 μm InAs layers on GaAs substrates has been developed. Good results are obtained by inserting a short period strain layered superlattice at the InAs/GaAs interface. A careful optimization of the InAs growth parameters has also been performed. Intense RHEED oscillations

have been observed for growth under As-stabilized conditions. The resulting InAs layers have electron mobilities comparable to the best ever reported. This method for depositing InAs buffer layers on GaAs has since been used in growths of novel heterostructures from combinations of the nearly lattice-matched materials InAs, GaSb, and AlSb.

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# Appendix A

## MBE System

### A.1 Introduction and Outline

Figure A.1 is a schematic diagram of the McGill group MBE system. The figure is identical to Fig. 1.4, but is shown again here for convenience. As discussed previously, the MBE system was designed to have a high degree of flexibility; in terms of both the types of semiconductor heterostructures which can be grown, and the different experiments which can be performed. Although each of the chambers on the system are adaptations of standard Perkin Elmer equipment, integration of the different chambers required a number of special design considerations. The purpose of this appendix is to document these considerations, in addition to modifications of the standard Perkin Elmer chambers which have been made. Features of the chambers which are considered to be standard are not discussed here, as they are well-documented in the system manuals.

Section A.2 discusses the transfer of samples throughout the MBE system. Modifications made to the III-V chamber are documented in section A.3. Some practical considerations for III-V source loading are also given. Section A.4 lists the modifications made to the standard Perkin Elmer prep/analysis module. Fi-

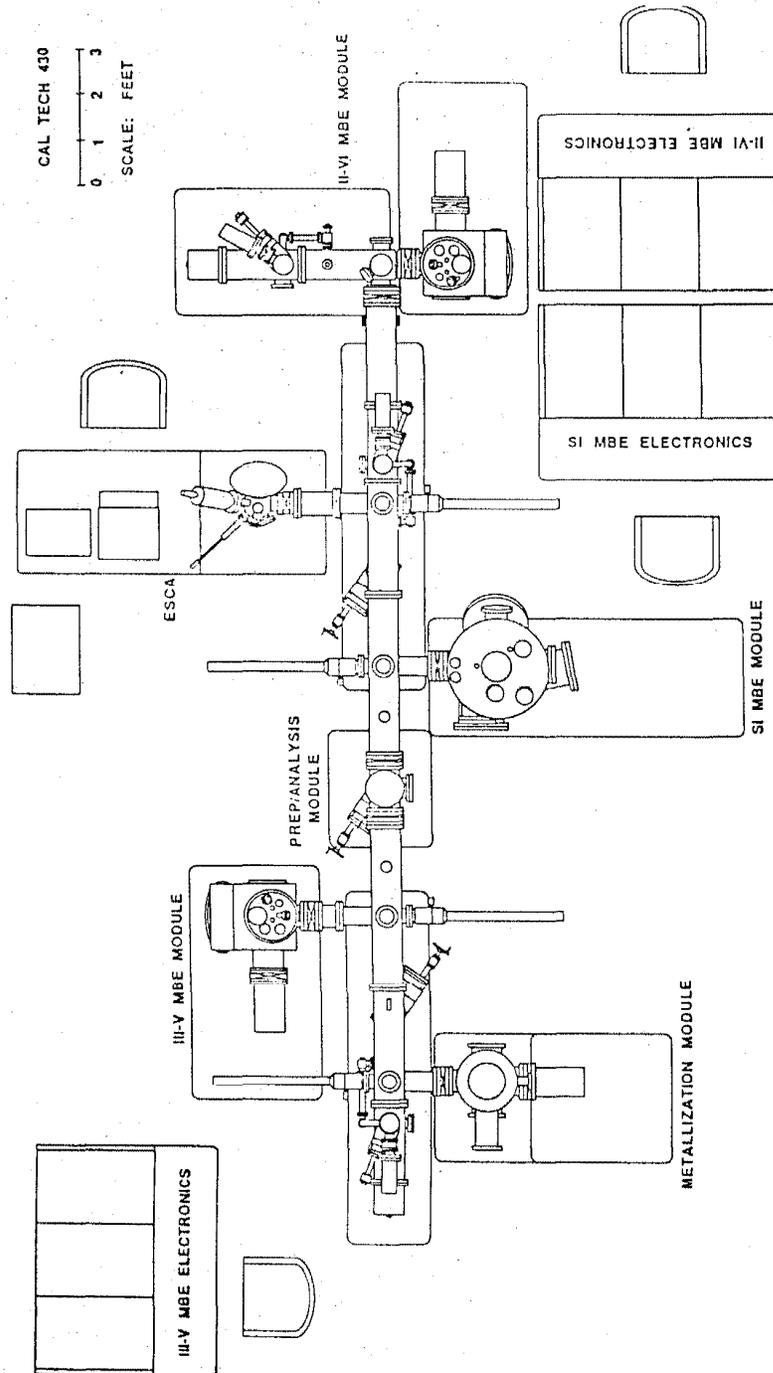


Figure A.1: Schematic diagram of the McGill group MBE system. The system has separate III-V, II-VI, and group IV growth chambers, and an ESCA/Auger system, connected by ultrahigh vacuum transfer tubes. The system also includes a prep/analysis module and a metallization chamber.

nally, modifications made to the standard Perkin Elmer metallization chamber are documented in section A.5.

## A.2 Transfer Mechanism

The MBE system is designed to accommodate wafers up to 3" in diameter. Substrates are mounted on molybdenum blocks by either In bonding or specially designed clips, depending upon which variety of block is used. Each of the molybdenum blocks has a groove ( $\approx 0.5$  cm wide) around its side. This feature allows the block to be held by a transfer fork which has prongs designed to slide into the groove.\*

Each of the three transfer tubes depicted in Fig. A.1 has a transfer fork which runs its length. The fork in the middle transfer tube (the one attached to the ESCA and group IV chambers) has been specially designed to permit blocks to be transferred out both ends of the tube. Four additional transfer forks are mounted perpendicular to the two long transfer tubes, opposite the metallization, III-V, group IV, and ESCA chambers. These forks are used to move blocks from the transfer tubes into the chambers.

Parking stages have been installed at each place in the system where it is necessary to release blocks from one transfer fork and pick them up with another (six places, including the stage in the prep/analysis module). Blocks can be set on and taken off of the stages with the transfer forks. In addition, each of the transfer tubes has an elevator which can hold a cassette for storage of up to six blocks. These elevators are positioned directly beneath the three intro hatches, and are the mechanism for transferring the blocks into and out of ultrahigh vacuum.

At least two gate valves must be opened in order to transfer a block from

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\*The blocks for the group IV growth chamber are designed differently, but are compatible with the system transfer mechanism.

one chamber to another. In general, it is a good practice to open these valves sequentially, so that only adjacent chambers are exposed to each other at any given time. Moving a block from one end of the system to the other has been found to take approximately 15 minutes.

### A.3 III-V Chamber Modifications

The III-V chamber is basically a standard Perkin Elmer 430 system, with no major modifications. However, some procedures not discussed in the manufacturer's manual have been developed from our experience with the system, and should be documented. In addition, an Sb cracker made by another vendor has been installed on our source flange.

#### A.3.1 Sb cracker

We have purchased and installed an EPI PE-75 cracking effusion cell, along with a matching EPI-PSC power supply. Both the bulk evaporator and cracker sections of the cell are water cooled, allowing the Sb evaporation temperature ( $\approx 600^\circ\text{C}$ ) to be accessed. The crucible for the cell consists of a cylindrical tantalum can with a long thin tube (cracking zone) extending out its top. The crucible can be dismantled from the system for source loading without removing the body of the cell from the system. A simple calculation indicates that dimers ( $\text{Sb}_2$ ) are produced by the cell whenever the cracker section is held above  $700^\circ\text{C}$ . Typical operating conditions during growth are  $625^\circ\text{C}$  at the bulk evaporator section, and  $850^\circ\text{C}$  along the cracking zone.

Unfortunately, the EPI power supply requires 120 VAC power, and the Perkin Elmer electronics rack is designed for mostly 220 VAC (single phase) power. It has been determined that running the Sb cracker from the 120 VAC section of the

pressure interlocked power can cause the system circuit breaker to trip, resulting in an abrupt power shutdown. Therefore, we connect the power supply to a wall outlet in the cleanroom during growth.\* When the system is idling, we connect the EPI power supply to the pressure interlocked power so that it will be safeguarded in the event of vacuum loss.

### A.3.2 Source Loading Information

Although the III-V source flange has eight ports, several of the source ovens have loading restrictions which limit the possible arrangements of sources. These restrictions are listed here.

1. The Sb cracker is better placed such that it tilts back slightly, since the Sb is sometimes melted during operation and can flow out under gravity. However, the cell will not fit in the bottom two ports of the source flange due to its length.
2. The 60 cc In cell should not be placed in a port which has a shutter pivot mechanism below it, because the In can flow down the shutter into the mechanism. This can result in a freezing of the shutter. The two bottom ports on the source flange are ideal for this cell.
3. The 60 cc Ga cell should be placed such that it tilts back. The four bottom ports of the source flange can accommodate this cell.
4. The 60 cc Al cell should not be loaded with a large quantity of Al (<12 g). This will prevent cracking of the crucible provided that slow ramp downs of the oven temperature are used.

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\*The wall outlet is supplied through a 20 Amp breaker. The EPI power supply is rated for 20 Amps maximum.

5. The As cracker should be placed on one of the top two ports on the source flange. The cell can be loaded by dismounting the bulk evaporator from the system.

### A.3.3 Liquid Nitrogen Plumbing

We have found that the III-V system can be run in a closed cycle liquid nitrogen mode in spite of its small source flange tubing (the II-VI and group IV growth chambers have larger diameter tubing). Our plumbing arrangement is a 'T' at the end of the triax feed line from the liquid nitrogen phase separator, with one branch feeding the source flange directly, and the other feeding the system cryopanel through the Perkin Elmer manifold. The return lines from the source flange and manifold are then merged in another 'T' with the semiflex return line to the phase separator. We generally cool the system down to liquid nitrogen temperature with open loop operation, then switch to closed loop once the system is cold. It is occasionally necessary to switch to open loop operation when most of the source ovens are hot ( $>900^{\circ}\text{C}$ ).

### A.3.4 Water Cooling

We run each of the parts of the system which require water cooling in series. This arrangement assures that the flow rate through each of the parts is the same. The EPI cracking cell presents the largest resistance to flow as it has the smallest diameter tubing. Therefore, it is best to run the supply line to the EPI cell first to prevent building up large back pressures on the other parts of the system. We *do not* run water into the bellows for the substrate heater. Perkin Elmer has determined that water cooling of the substrate heater is unnecessary, and can lead to direct leakage of water into the chamber if (and when) the bellows wear out.

### A.3.5 Instrument Coating

We have found that the analysis instruments (ion gauge, RHEED gun, RGA, flux monitor) in the III-V chamber tend to become coated due to the high As and Sb pressures during growth. This coating eventually results in short-circuiting of the electrical elements in these instruments. Removing the shorted elements for cleaning requires breaking vacuum and a bakeout, resulting in at least one week of down time. It has been found that satisfactory functioning can be restored by passing electrical current through the short (particularly a fairly resistive short), reevaporating the coating material. We generally use a curve tracer for this operation, set to the minimum amount of output power necessary to remove the short. High voltages (up to 1.6 kV) can be used, provided that the elements are well-insulated (other than the short). Of course, safety precautions should be exercised when applying high voltages to prevent bodily injury and/or equipment damage.

## A.4 Prep/Analysis Module Modifications

The prep/analysis module depicted in Fig. A.1 is a modified version of a standard Perkin Elmer chamber. Standard design features include a heater stage which can reach 1200°C, a water jacketed chamber, an ion pump, and two 8" gate valves. The changes and additions made to the standard design are listed here.

1. An 8" flange has been added at the top of the chamber. The flange is positioned appropriately for a Princeton Research Instruments reverse view LEED (low energy electron diffraction) analyzer.
2. A heat shield for the LEED analyzer has been installed on a 1.33" flange. The shield is connected to the flange through a rotary feedthrough which allows it to be moved into and out of position.

3. A sputter gun port (nonstandard, 4.75" flange) has been designed for a differentially pumped Ion Tech gun. The port is approximately 10" from the sample holder, at an angle of 45°.
4. The docking viewport on the system is mounted on a 4.5" flange, at an angle of 30° to the substrate.
5. An optical access port has been added at the angle of reflection to the docking viewport (for reflection of light from the sample surface). The port has a 2.75" flange, and could be used for a number of optical applications, such as pyrometry, laser annealing, ellipsometry, and interferometry.
6. An ion gauge has been mounted on a port with a 2.75" flange.
7. A 6" flange has been added in case a cryopump is desired.
8. A 4.5" flange for a UTI 100 residual gas analyzer has been added to the chamber.

Drafted layouts for this chamber are stored in the file cabinet in Watson building, room 270.

## A.5 Metallization Chamber Modifications

The metallization chamber depicted in Fig. A.1 is a modified version of a standard Perkin Elmer chamber. The changes and additions made to the standard design are listed here.

1. A 'T' has been placed between the standard CTI CT-8 cryopump and the chamber so that an ion pump can be added at a later date.
2. A nonstandard 4.75" flange has been added for an Ion Tech sputter gun.

3. A 6" flange has been added at an angle of 135° from the sample introduction port. This flange is intended to be used for attaching additional modules to the MBE system. Alternatively, the docking viewport (90° from the introduction port, 135° from the additional 6" port) could be used as a point of connection to additional modules. The window for viewing sample docking would then be moved to the additional 6" flange.
4. A 4.5" flange for a UTI 100 residual gas analyzer has been added at the end of a long, shuttered tube.
5. Two 10" e-gun ports have been placed on opposite sides of the chamber. These ports should be sufficiently large to house multiple crucible or single crucible guns from Airco Temescal, Leybold-Heraeus, or another manufacturer.
6. Nine 2.75" conflat flanges have been added at various points on the chamber for other sources, cryopanel, crystal thickness monitors, and shutters.

Drafted layouts for this chamber are stored in the file cabinet in Watson building, room 270.

# Appendix B

## Cleanroom

### B.1 Purpose

The principal purpose of the McGill group cleanroom is to provide a clean, controlled environment for molecular beam epitaxy and photolithography. Both of these experimental facilities encompass a number of pieces of equipment and procedures, which require varying degrees of cleanliness. Attempting to house all of the activities under the most stringent cleanliness conditions would be very expensive and difficult to maintain. Instead, we have separated the cleanroom into sections, with different cleanliness requirements in each section.

Many pieces of equipment housed in the cleanroom have special utility requirements (such as liquid nitrogen). Another purpose of the cleanroom is to organize the supply of these utilities such that connections to equipment are convenient. Furthermore, the cleanroom serves to partially isolate utility supplies from those routed to other laboratories, reducing their vulnerability to external fluctuations.

Finally, an important purpose of the cleanroom is to enhance safety (both for people and equipment). Some of the MBE and photolithography procedures involve hazardous materials, which are more easily isolated in a controlled environ-

ment. Large electrical power loads can also be safeguarded better in the controlled cleanroom environment.

## **B.2 Design of Cleanroom Facility**

This section contains general information about the design of cleanroom, including specifications for cleanliness, environment, and materials. Utilities built into the facility are also discussed. Complete as-built drawings, manuals, and specifications for the cleanroom facility can be found in Watson building, room 270.

### **B.2.1 General**

Figure B.1 is a diagram of the cleanroom, drawn to scale. The space for the facility was obtained by combining Labs 251 and 253 of the Thomas J. Watson Sr. Laboratory of Applied Physics. All interior walls in and between the two rooms were demolished. Building plumbing and ducting were rerouted around the cleanroom.

The cleanroom facility has been partitioned into six separate rooms. The following is a listing of each room and its function.

1. The **MBE room** houses the Perkin Elmer MBE system.
2. The **prep room** contains two hoods for MBE substrate preparation.
3. The **lithography room** houses all of the equipment for photolithography (mask aligner, photoresist spinner, ovens, microscope, etc.).
4. The **Vestibule** provides a space for people to put on cleanroom gowns, caps, and booties prior to entering the rest of the facility.

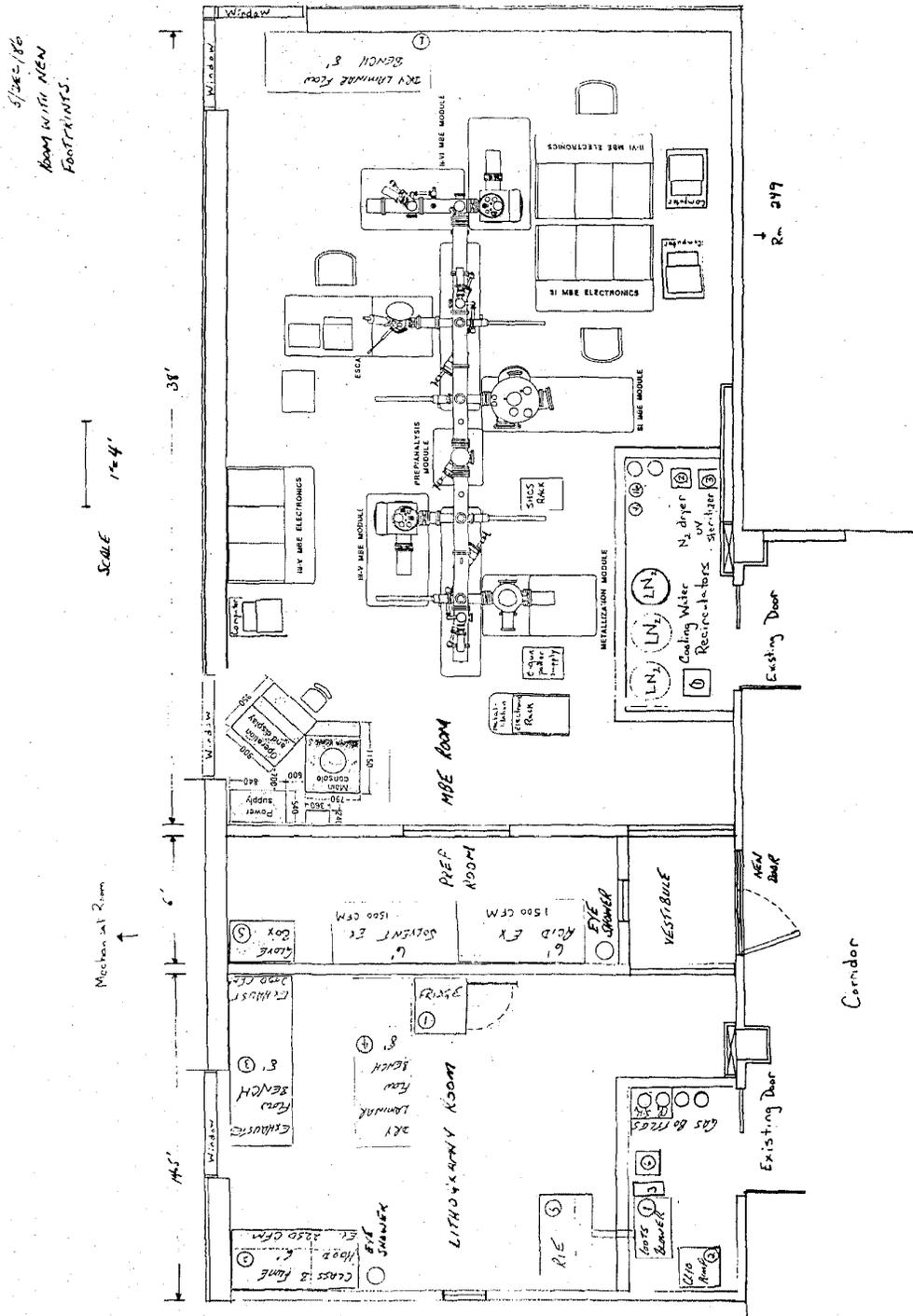


Figure B.1: Diagram of the cleanroom facility, drawn to scale. The facility has six separate rooms, with an overall specification of Class 10,000. The facility houses equipment for molecular beam epitaxy and photolithography.

5. **Utility room 1** is a nonclean room which houses utilities and dirty equipment needed by the MBE system.
6. **Utility room 2** is a nonclean room which houses utilities and dirty equipment needed by the photolithography and substrate preparation equipment.

### **Connection of Rooms**

Access between the various rooms is provided as follows:

1. **Sliding glass doors** connect the vestibule to the lithography and MBE rooms. The door to the lithography lab is tinted yellow. Another sliding glass door connects the prep room to the MBE room.
2. **Windows** are located on the wall between utility room 1 and the MBE room, and on the wall between utility room 2 and the lithography room.
3. **Removable walls** have been placed between utility room 1 and the MBE room, and between utility room 2 and the lithography room. These walls can be dismantled to move large pieces of equipment into and out of the cleanroom facility.
4. **Plumbing passthroughs** are used as points of entry for utility lines from the utility rooms to the MBE and lithography labs.
5. A **chemical passthrough cabinet** is located on the wall between the vestibule and the prep room. The cabinet is large enough to hold several one gallon chemical bottles. Transparent cabinet doors are mounted on both the vestibule and prep room sides, so that bottles can be transferred into the prep room without being carried through the MBE room.
6. A **sample passthrough cabinet** (identical in design to the chemical passthrough cabinet) is located on the wall between the lithography room and

Lab 255. This cabinet facilitates the removal of samples from the cleanroom. The transparent cabinet doors are tinted yellow.

7. **Doors** to the corridor from the vestibule and the two utility rooms have been made.

### **Air Handling**

Air handling for the cleanroom facility is separated into two sections. One air handler is dedicated to the MBE room. Air is supplied through the HEPA filter units in the ceiling, pushing air out of the room through grates at the bottom of return air walls and the wall to utility room 1. The return air plenum consists of the return air walls, utility room 1, and the space between the MBE room ceiling and the Watson roof. Air is drawn from the plenum for refiltering and recirculation into the MBE room. A purge fan has been installed to exhaust air from the room if desired. Make up air is drawn from the outside. The second air handler services the lithography room, prep room, and vestibule. Once again, air is supplied through HEPA filter units in the ceiling. Considerably more air is exhausted from these rooms due to four exhausted hoods. Hence, less of the air is recirculated. The return air plenum consists of return air walls, utility room 2, and the space between the Watson roof and the lithography room, prep room, and vestibule ceilings. All of the air handling equipment is located on the Watson roof, above the cleanroom facility.

### **B.2.2 Specifications**

The following is an abbreviated list of specifications for the cleanroom facility.

1. The overall cleanroom classification is Class 10,000, which means that there are fewer than 10,000 particles of size  $0.5 \mu\text{m}$  or larger per cubic foot. Particle

counter measurements consistently yield smaller numbers of particles than this specification.

2. Several specific areas are designed to be cleaner than the rest of the facility. The work spaces under the laminar flow hoods and benches should be Class 100 areas due to complete HEPA filter coverage. Three 4' x 4' vinyl curtained areas have been set up above each of the three intro hatches on the MBE system. These areas enclose two 2' x 4' HEPA filters each, making them roughly Class 100. Finally, the prep room is probably Class 1000 due to the large number of HEPA filters per unit area in the room.
3. The temperature in the facility is thermostatically controlled. The air handling system should be capable of maintaining a temperature of  $72 \pm 5^\circ\text{F}$ .
4. The humidity in the facility should be controllable to  $40\% \pm 5\%$  RH.
5. The existing walls in the cleanroom have been coated with an epoxy paint which generates very few particles.
6. Modular cleanroom wall panels have been used for all new cleanroom walls.
7. The ceiling of the clean room is a Comp-Aire 2" system. Con-web clean room ceiling panels have been used.
8. The flooring material in the cleanroom facility is mipolan. This material is resistant to chemical spills, but can be cracked by liquid nitrogen.

### **B.2.3 Utilities**

The following is a list of all of the utilities available in the cleanroom and how each of them can be accessed.

1. **Liquid nitrogen** is needed for the three growth chambers on the MBE system and for sorption pumps. A Vacuum Barriers phase separator has been installed on the roof of Watson above utility room 1 for this purpose. Three triax feed lines (inner-liquid, middle-liquid and gas, outer-vacuum) have been dropped from the phase separator and plumbed to each of the three growth chambers. The lines have been routed via a plumbing passthrough and cable trays in the MBE room. Semiflex return lines (inner-liquid and gas, outer-vacuum) run back to the phase separator from the chambers. The phase separator is filled by 160 liter liquid nitrogen dewars, housed in utility room 1.
2. **Electrical panels** for the facility have been placed in the utility rooms. Three 225 A panels, located in utility room 1, service the MBE room. One 225 A panel, located in utility room 2, services the lithography and prep rooms. All of the large (permanent) equipment in the cleanroom facility has been hard-wired to the electrical panels.
3. **Unfiltered deionized water** is available in the utility rooms. It has also been plumbed to the water filtration systems installed in the prep and lithography rooms.
4. **Filtered, sterilized deionized water** is generated by the water filtration systems in the prep and lithography rooms. Each of these systems consists of a Millipore filtration unit and an Aquafine ultraviolet sterilizer. The water is then delivered to each of the four wet hoods in the facility.
5. **Closed loop (Watson building) water** for equipment cooling can be accessed in both of the two utility rooms.

6. **A NESLAB filtered, closed loop, cooling water recirculator** has been installed in utility room 1. The NESLAB unit supplies cooling water for the MBE system via a cooling water manifold located in the MBE room. Heat is exchanged from the NESLAB to the Watson equipment cooling water lines.
7. **Hot and cold tap water** are available in both of the utility rooms, as well as the fume hood in the lithography room.
8. **Natural Gas** is available in both of the utility rooms.
9. **High pressure air (85 PSI)** is available in both of the two utility rooms, as well as two of the hoods in the lithography room and both of the hoods in the prep room.
10. **Unfiltered nitrogen gas** is available in both of the utility rooms.
11. **Filtered, dried nitrogen gas** has been plumbed to all of the hoods in the facility. A separate, regulated supply has been connected to a manifold in the cable tray above the MBE system via a plumbing passthrough. The manifold has six output connectors (Swagelok) for hooking up the different MBE chambers.
12. **High pressure nitrogen (for MBE pneumatics)** is supplied by a gas cylinder in utility room 1. A high pressure hose carries the nitrogen to a cross in the cable tray above the MBE system. The three remaining branches of the cross are connected to each of the three growth chambers via high pressure hoses. A stainless steel manifold has been placed in the cable tray for this utility, but has never been used.
13. **Helium gas** is supplied by a gas cylinder in utility room 1. A stainless steel manifold has been placed in the cable tray for this utility, but has never been used.

14. **A vacuum pump** has been placed in the Watson mechanical pod nearest to the cleanroom. The pump can be switched on in either the lithography room or the prep room. Vacuum lines have been plumbed to each of the hoods in the facility.
15. **Drains:** all of the hood drains have been tied together and plumbed to an open drain in utility room 2. Because of this connection scheme, all solvents (except alcohols) must be stored in waste bottles, and all acids must be neutralized before they are flushed down the hood drains. An open drain has also been left in utility room 1 for use in the event of flooding.
16. **RS232 lines** (for computer terminals) have been placed at convenient points throughout the cleanroom.