EXPERIMENTAL STUDIES OF HETEROSTRUCTURE DEVICES: RESONANT TUNNELING TRANSISTORS AND GaAs/AlAs/GaAs CAPACITORS

Thesis by

Ted K. Woodward

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To my mother and father,

for love and courage.

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Abstract

This thesis is concerned with the experimental study of two kinds of heterostructure devices. The resonant tunneling transistor (RTT) is the subject of the first part of the thesis. The RTT is a new class of electronic device that has a controllable negative differential resistance (NDR) as its distinguishing characteristic. Since the first realization of a device of this type, in 1985, about 6 types of transistor structures have been reported that exhibit controllable NDR. We report the development of two types of RTTs, which are series integrations of GaAs/$Al_xGa_{1-x}As$ double-barrier heterostructures with field-effect transistors. Samples were produced by metalorganic chemical vapor deposition (MOCVD). Several fundamental applications of these devices are also presented.

The first device is an integration of a resonant tunneling double-barrier heterostructure with a vertical field-effect transistor. The composite device is referred to as a DB/VFET. The device exhibits NDR in its source-drain I–V curve at 77 K, which is controllable with gate bias. Novel device features include the observation of NDR at large voltages (greater than 10 V) in one bias direction. One device exhibits NDR at room temperature. Typical 77 K peak-to-valley current ratios were about 5. Frequency multiplication and microwave oscillations at 0.8 and 3.3 GHz have been observed in this device. This device is discussed in Chapter 3 and Chapter 5.

The second device is an integration of a double-barrier heterostructure with a planar field-effect transistor, in this case a metal-semiconductor field-effect transistor (MESFET). The composite device is referred to as a DB/MESFET. It also exhibits NDR in its source-drain I–V curve, but is qualitatively different from the DB/VFET in its behavior. A variety of output characteristics may be obtained by varying the double-barrier and MESFET parameters. Logic operations are of interest for this device, and a flip-flop circuit is demonstrated with a single

DB/MESFET. This device is described in Chapters 4 and 5.

In Part II of the thesis, studies of a different heterostructure are reported. GaAs/AlAs/GaAs single-barrier capacitor structures, characterized by relatively thick AlAs barriers ($1000 - 4000$ Å) are the subject of this part of the thesis. Samples were grown by MOCVD. A variety of electrical and optical measurements were performed on these structures. These included capacitance–voltage (C–V), current–voltage (I–V), deep-level transient spectroscopy (DLTS), and photoresponse measurements. This structure, a fundamental part of many heterostructure devices, exhibits novel C–V and I–V behavior that can be attributed to significant densities of electron trap states near one of the GaAs/AlAs interfaces, or in the AlAs. Estimates of the deep-level concentration can be made from both C–V and I–V measurements, which have been confirmed with DLTS measurements. DLTS confirmed that the trap levels are localized. These studies are described in Chapter 6. Photoresponse measurements of the structures are interesting, and are described in Chapter 7. These studies explain the observation of zero-bias photocurrent consistent with electron transport from the back of the sample to the front.

Parts of this thesis have been or will be published under the following titles:

Part I:

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T. K. Woodward, T. C. McGill, and R. D. Burnham, *Appl. Phys. Lett.* **50**, 451 (1987).

Integration of a Resonant Tunneling Structure with a Metal Semiconductor Field-Effect Transistor,
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Resonant Tunneling Field-Effect Transistors,
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Applications of Resonant Tunneling Field-Effect Transistors,
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Part II:

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Electrical Behavior of GaAs-AlAs Heterostructures,
T. K. Woodward, T. C. McGill, and R. D. Burnham, *J. Vac. Sci. Technol. B* **4**, 1022 (1986).

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T. K. Woodward, T. C. McGill, and R. D. Burnham, *J. Appl. Phys.* **60**, 3755 (1986).

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Chapter 1

Introduction and Overview

This thesis is concerned with the experimental study of two types of semiconductor devices. One project is concerned with the realization of three-terminal devices utilizing the novel properties of the double-barrier tunnel structure. The second project is an investigation into the basic properties of thick single-barrier GaAs/AlAs/GaAs capacitors. Both the double barrier and the capacitor can be classified as *heterostructures*, or composite devices consisting of more than one semiconductor material. These materials are usually arranged atop one another in layers that have a definite crystalline registration to one another.* The experimental results reported here are confined to GaAs/$Al_xGa_{1-x}As$ heterostructures.

This chapter serves as an overview and summary of the document. It explains some of the reasons for doing the work and describes the major results. In Section 1.1 the major results are briefly summarized. Following this is Section 1.2, a brief explanation of the importance of heterostructure devices to modern microelectronics. Three-terminal device research is covered in Section 1.3, and single-barrier research in Section 1.4.

*Referred to as *epitaxial* layers.

1.1 Results Summary

Two types of new transistor structures have been successfully demonstrated. Both are integrations of double-barrier tunnel structures with field-effect transistors. One combines a double barrier with a vertical field-effect transistor structure (DB/VFET). The other combines a double barrier with a planar metal-semiconductor field-effect transistor (DB/MESFET). These devices exhibit gate-controlled negative differential resistance (NDR) in their source-drain characteristics. Results of DC characterization of the devices are described and interpreted in terms of sample geometry in Chapters 3 and 4. In particular, a wide range of characteristics can be obtained, depending upon the relationship between the double barrier and the field-effect parts of the device. Applications of these devices to logic, signal processing, and oscillators are described. Samples were produced by metalorganic chemical vapor deposition (MOCVD). MOCVD growth is rare for resonant tunneling structures, the vast majority of which are produced by molecular beam epitaxy (MBE). We have recently begun efforts to produce double-barrier tunnel structures by MBE. Some success has been achieved, which will be discussed in Chapter 2.

Single-barrier GaAs–AlAs–GaAs structures were also studied. Devices consisted of a 1000–4000 Å barrier of AlAs lying between a degenerately doped GaAs top layer and a nondegenerately doped GaAs backside layer. Capacitance–voltage (C–V) curves showed hysteresis and photosensitive behavior attributed to deep levels. Deep-level transient spectroscopy (DLTS) confirmed the presence of these levels and indicated that they are localized in the AlAs or near the interface between the AlAs and the GaAs. Current-voltage (I–V) measurements gave additional evidence for the deep levels in the form of hysteresis at low current levels. Estimates of deep level concentration obtained from all three techniques are in reasonable agreement with one another. These results are described in Chapter 6.

Finally, measurements of the photovoltage induced in the device under front side illumination were made, at a variety of external applied biases. The photovoltage measured with zero applied bias was consistent with electron transport from the back of the device to the front. Further measurements were used to explain this observation as being due to built-in voltages in the device. These experiments are explained in Chapter 7.

1.2 Why Heterostructures?

The electrical behavior of semiconductors can be controlled to an exquisite degree. This is why semiconductors form the basis of a technology. Greater control of the behavior of a potential electrical device can be achieved with the use of more than one semiconductor in the same device. Many of these ideas rely on the concept of band offsets. This fundamental issue is a subject of current investigation and so is somewhat controversial. It deals with the question of what happens to the potential experienced by an electron at the interface between two materials. It is commonly assumed that the change in potential occurs abruptly, resulting in potential steps (band offsets) in the valence and conduction bands that add up to the band-gap difference.

The value of heterostructures can be illustrated by considering the bipolar transistor. In an *n-p-n* transistor, the injection of electrons from the emitter into the base is desirable. The injection of holes from the base into the emitter is undesirable, representing base-emitter leakage current. The ratio of the desired injection to the undesired injection is an important quantity, defined here as Γ. In a conventional homojunction transistor under low injection conditions, ignoring diffusion constants and length factors, it is related to the doping concentration on either side of the junction, and the difference in potential energy across the

junction:

$$\Gamma \sim \frac{n_p}{p_n} = \frac{n_n e^{q(V-V_{bi}^n)/kT}}{p_p e^{q(V-V_{bi}^p)/kT}},$$

where n_n is the electron concentration in the n type emitter, n_p is the electron concentration in the p type base, V_{bi}^n is the barrier height for electrons between emitter and base, and V is the amount of forward-bias voltage, with similar definitions for holes. In an ordinary bipolar transistor the exponential factors are the same and we are left with $\Gamma = n_p/p_n = n_n/p_p$. Large values of Γ therefore impose a number of design constraints on the transistor, particularly on base doping level.

Consider a case in which the n–type emitter is made from a wider band-gap material than the base. Assuming that the smaller energy gap lies within the larger (a type I heterojunction), the potential steps in the conduction and valence bands combine to yield an increased barrier for hole injection. Now the ratio of injected electrons to injected holes is roughly:

$$\Gamma \sim \frac{n_p}{p_n} = \frac{n_n}{p_p}\left(e^{q\ \Delta E_g/kT}\right),$$

where ΔE_g is the difference in band-gap between the two materials. For semiconductors with large band offsets the improvement in Γ can be quite significant. Such a device is called a Heterojunction† Bipolar Transistor (HBT).[1]

This example illustrates what can happen when an additional degree of freedom is introduced; in this case the adjustability of hole and electron barrier heights across a p-n junction. In addition to improving the performance of conventional devices, altogether new devices can be constructed with the new freedoms provided by heterostructures. The geometry of interest here is the resonant tunneling double-barrier structure.

† A *heterojunction* is a single interface between two semiconductors. A *heterostructure* contains an arbitrary number of heterojunctions.

1.3 Resonant Tunneling Transistors

1.3.1 Double Barriers

A double-barrier heterostructure consists of a thin (about 50 Å) layer of narrow band-gap material separated from electrodes by two equally thin layers of wider band-gap material. GaAs and $Al_xGa_{1-x}As$ are the two materials commonly used for the narrow and wide band-gap materials, respectively. The thin GaAs region forms a quantum well, the thin nature of which gives rise to quasi-bound states. Because the barrier regions are also thin, there is a significant probability that carriers will tunnel out of the well region. Therefore the states in the well cannot be considered true bound states, but should be viewed as resonant energies for transmission from one electrode region to the other. Transport through the structure in this ideal case is via quantum-mechanical tunneling. The most interesting feature of the device is the existence of a negative differential resistance (NDR) in its I–V characteristic.

A simple model of the device illustrates the origin of the NDR. For simplicity, consider the problem one-dimensionally, and assume that energy is conserved during carrier transport. For electrons in the left electrode to tunnel through the resonance level into the right electrode (referred to as *resonant tunneling*), two conditions must be satisfied. First, there must be an occupied electronic state in the left electrode with the same energy as the resonance level (in which there must be an empty state). There must also be an empty state in the right electrode at the same energy as the resonance level. For small amounts of applied bias, both conditions can be satisfied, and resonant tunneling is allowed. At a critical bias the first condition will no longer be satisfied, due to band bending of the resonance level below the conduction band of the left electrode region. The result is an abrupt decrease in the current. This process is schematically illustrated in Fig. 1.1.

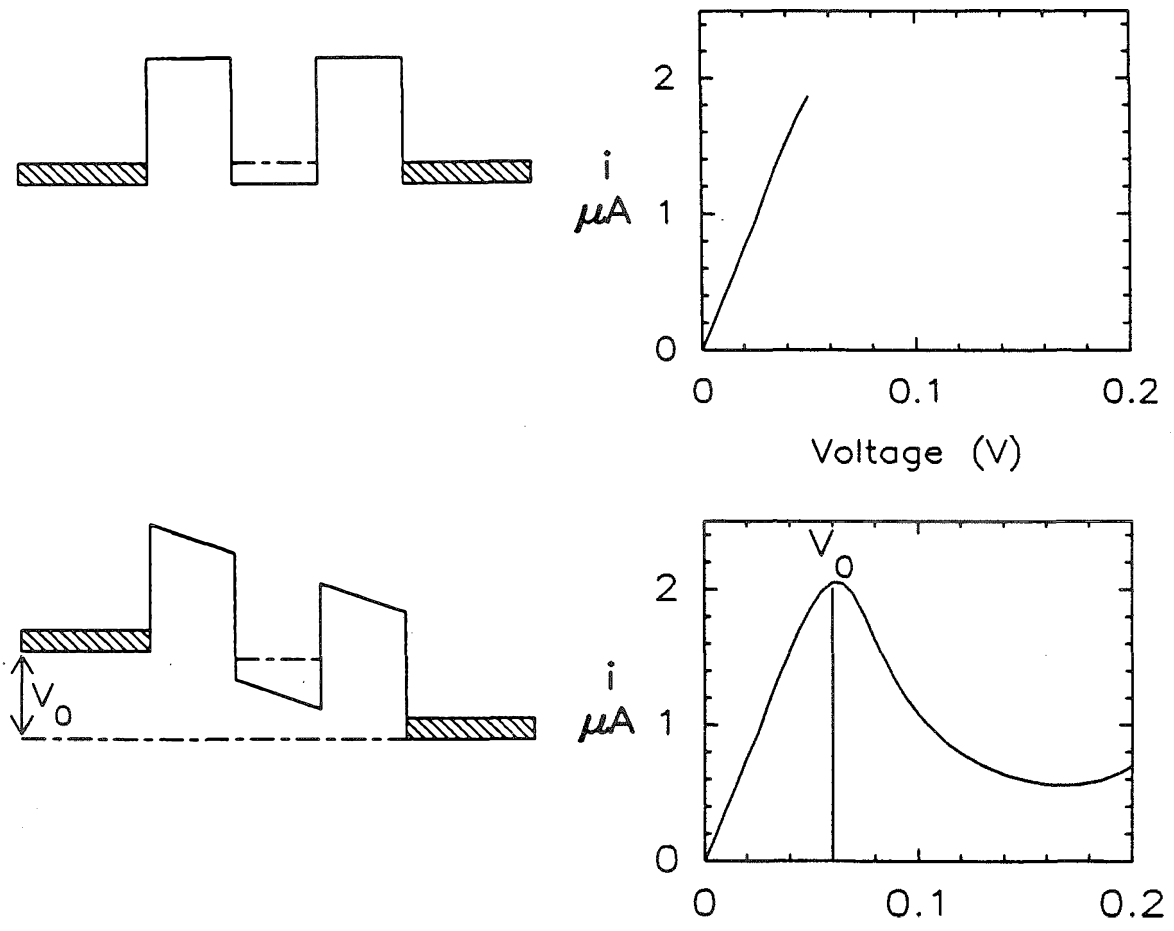

Figure 1.1: I–V curves and conduction-band diagrams for for the double barrier. The top pair of diagrams illustrates the zero-bias band diagram and I–V curve for low bias levels. For low biases, electrons may tunnel through the resonance level. The bottom band diagram and I–V curve illustrate the resonance-voltage band diagram and the entire I–V curve. When the resonance level is brought to the same energy as the conduction-band edge of the left electrode, resonant tunneling is quenched, and negative differential resistance is observed.

In the world of microelectronics, 'small' often translates into 'fast,' and fast is good. By this analysis the double barrier, with critical dimensions of about 100 Å, should be the very good indeed. In fact, the potential for high-speed devices is the driving force behind most of the double-barrier research done today. In practice, things are not so simple. Practical constraints such as capacitive charging effects and unknowns such as tunneling transit times cloud the issue of the ultimate speed of the double barrier. Theoreticians have taken many approaches to the double barrier. A partial review of the theoretical literature on the double barrier is contained in Chapter 2.

Experimental results have demonstrated that carrier transport through the double barrier can be very fast. Oscillator structures operating at millimeter wave frequencies (56 GHz, 102 GHz, and 200 GHz) have been demonstrated, with predictions of 600 GHz devices.[2,3] Terahertz (1 THz = 1×10^{12} Hz) response of the double barrier has been measured.[4] At this point it seems clear that the double barrier is a high-speed device. Exactly how fast is unclear. Oscillators and amplifiers are therefore a clear area of interest for the double barrier. Another potential area of application is in logic and digital systems.

1.3.2 State of the Art

Resonant tunneling was first experimentally observed in the derivative of an I–V curve of a double-barrier heterostructure in 1974.[5] Since then, great strides have been made. In 1983 the first observation of room temperature NDR was made.[6] These results were obtained with heterostructures grown by MBE. In 1984 NDR was reported in a structure grown by metalorganic chemical vapor deposition (MOCVD).[7,8,9] The results described in this thesis were obtained with samples grown by MOCVD.

A figure of merit for the double barrier is the peak-to-valley (P/V) current

ratio of the NDR, obtained by dividing the current at the peak of the NDR by the minimum current at voltages greater than the peak voltage. This ratio qualitatively measures the sharpness of the resonance and the amount of current due to mechanisms besides resonant tunneling. A peak-to-valley current ratio of 21.7 has been reported for an MBE grown (Ga,Al)As double barrier at 77 K. This ratio fell to 3.9 at 300 K.[10] For comparison, tunnel diodes—an older kind of NDR device formed from p^+n^+ diodes—had maximum oscillation frequencies of about 100 GHz, in devices with P/V current ratios of about 7.[11] P/V current ratios exceeding 20 have been reported for GaAs tunnel diodes.[12]

Uniform and abrupt interfaces are critical to the successful growth of a double-barrier structure.[13] Equally important for good operation of the device is the cladding-layer geometry on either side of the barrier. The most successful room-temperature device operation has been achieved with the placement of undoped or lightly-doped spacer layers on either side of the double-barrier heterostructure.[10,14,15] These spacer layers apparently reduce impurity and thermally assisted tunneling, which tend to reduce the NDR P/V current ratio, particularly at room temperature. Spacer layers are discussed further in Chapter 2.

A highly desirable feature in a system for double-barrier growth is a large conduction-band offset. Thus, the GaAs/AlAs materials system may not be the ideal system for double-barrier growth. It has been used extensively because it is technically well understood compared to many other systems. A number of other systems have produced working double barriers. These include HgTe/CdTe[16] and its alloys, InP/GaAs and alloys[17], and $In_xGa_{1-x}As/In_xAl_{1-x}As$ systems.[14] Of these, the (In,Ga,Al)As system appears very promising. The largest P/V current ratios yet reported have been achieved in an $AlAs/In_xGa_{1-x}As/AlAs$ double barrier.[18] This ratio was an impressive 14 at 300 K, and increased to 35 at 77 K.

For high-speed applications a very important value is the current density passing through the structure. The current density is usually reported at the peak of the NDR and represents the ability of the device to modulate charge rapidly. Values in the $10^4 A/cm^2$ range have been reported.[2,14] This value is adjustable by varying barrier thickness as well as by modifying the thickness and doping of cladding layers surrounding the double-barrier structure.

1.3.3 Introduction to Three-Terminal Devices

The ability to isolate input from output, the added flexibility of a third controlling electrode, and the possibility of amplification are all reasons for preferring three-terminal devices to two-terminal ones. It can be argued that the double-barrier structure would benefit from the addition of a third electrode, especially for logic and signal-processing applications. Oscillators might also benefit from the additional electrode. Additionally, virtually all NDR devices are two-terminal in nature; a three-terminal device exhibiting NDR would be unique. These issues notwithstanding, the structures would likely be interesting of themselves.

The goal of a three-terminal negative-resistance device is the modulation of the negative resistance with a third electrode. A variety of ways of doing this have been proposed.[19,20,21,22] All of the ideas that have resulted in functioning devices have combined the double-barrier structure with a more conventional device. Double barriers have been combined with bipolar transistors[20,23], hot-electron transistors[22], and field-effect transistors[21,24,25] to form a new class of device; the resonant tunneling transistor (RTT). Trade-offs between the various devices are discussed in Chapter 2. The two types of devices described below were first proposed by Bonnefoi *et al.*[19,26,27]

Changing the resistance of one of the electrode regions of the double barrier will

alter the applied voltage at which the resonance condition[‡] is satisfied. Varying amounts of bias will have to be applied to the entire device to satisfy the resonance condition across the double barrier, due to the changing series resistance. The electrode resistance can be varied by placing a field-effect transistor in series with the double barrier. This effect could be achieved with lumped elements and wires. By integrating the two devices into a single semiconductor device, two advantages are accrued. First, parasitic effects are reduced. In fact, as will be seen, the double barrier becomes part of the transistor structure. Second, a more fundamental interaction between the devices becomes possible. An excellent example of this kind of interaction, in this case involving two *p-n* junctions, is provided by the bipolar transistor.

1.3.4 DB/VFET Devices

This section presents an overview of the project to integrate a double barrier with a vertical field-effect transistor. The device is simple in concept. A lightly-doped electrode region is pinched off by Schottky barriers placed along its vertical sides in a manner similar to a junction field-effect transistor (JFET).[28]

The ideal DB/VFET device would place electrodes on the sides of a vertical mesa structure; a formidable fabrication challenge. Devices of this type have been made. They are quite intricate, and capable of operation at about 70 GHz.[29,30] In order that our device be fabricated with simple techniques, many design modifications were made. These are described in detail in Chapter 3. The resultant structure makes a number of sacrifices in performance, but is relatively easy to fabricate. Almost any performance improvement will require a more complex fabrication procedure.

[‡]The *resonance condition* is satisfied when the device is biased such that the resonance level lines up with the conduction-band edge of the injecting electrode.

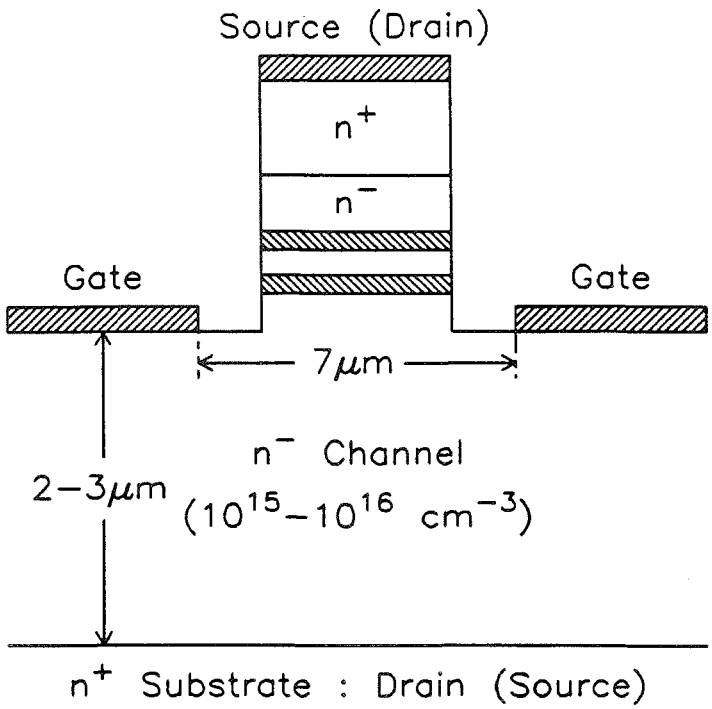

Figure 1.2: Final design of DB/VFET optimized for ease of fabrication. The tolerances for horizontal alignment are 1 micron.

The finished device is schematically illustrated in Fig. 1.2. It places the gate electrodes on a horizontal rather than vertical surface and relies on horizontal spreading of the primarily vertical depletion region under the gate to vary the resistance of the channel region. This design imposes stringent requirements on mesa width, gate spacing, and channel doping. One would like to have a thick, lightly-doped channel, a very narrow offset between the gate and the mesa containing the double barrier, and a very narrow mesa. More details are given in Chapter 3.

Results for a representative device are presented in Fig. 1.3. An interesting effect of the design is the high voltage at which NDR is observed. This is due to the presence of a large, lightly-doped region on one side of the double barrier. In *one* bias direction this region is depleted and provides a large region over which to drop bias. To satisfy the resonance condition across the double barrier, a much

larger bias must be applied across the entire device. It should be emphasized that this lightly-doped region does not represent a large series resistance, but rather forms a drift region, whose resistance can be modulated. Results for samples with different channel-doping levels show a consistent trend toward higher NDR voltage with decreasing channel doping, provided that the lightly-doped region is sufficiently thick. Modulation of the position of the NDR is achieved by the lateral extension of the gate field, and its interaction with the channel through which source-drain current flows.

Also of interest is the operation of the device in forward bias. Qualitative differences between forward- and reverse-bias operation were observed and attributed to the differences between the two bias configurations, specifically with respect to the role played by the lightly-doped channel region. These results are discussed in Chapter 3.

Some final comments about the DB/VFET are in order. Quite interesting I–V curves can be obtained. The double barrier and the FET segments of the device interact with one another to yield I–V curves that are not what would be achieved from wiring together lumped elements, as evidenced by the production of NDR at a high voltage. Several working DB/VFETs were eventually produced. While the device is not optimized for high-speed applications, sophisticated processing could be applied to greatly improve performance, as in advanced VFET structures.[29,30]

Some interesting applications of this device have been demonstrated. One is a frequency doubler, which uses the fact that an operating point may be moved completely through the NDR region by application of gate bias. Another application is to oscillator structures; microwave oscillators have been demonstrated at 0.8 and 3.3 GHz, with an output power of about 700μW at 3.3 GHz. An interesting potential use of the DB/VFET geometry as a transit-time device has been

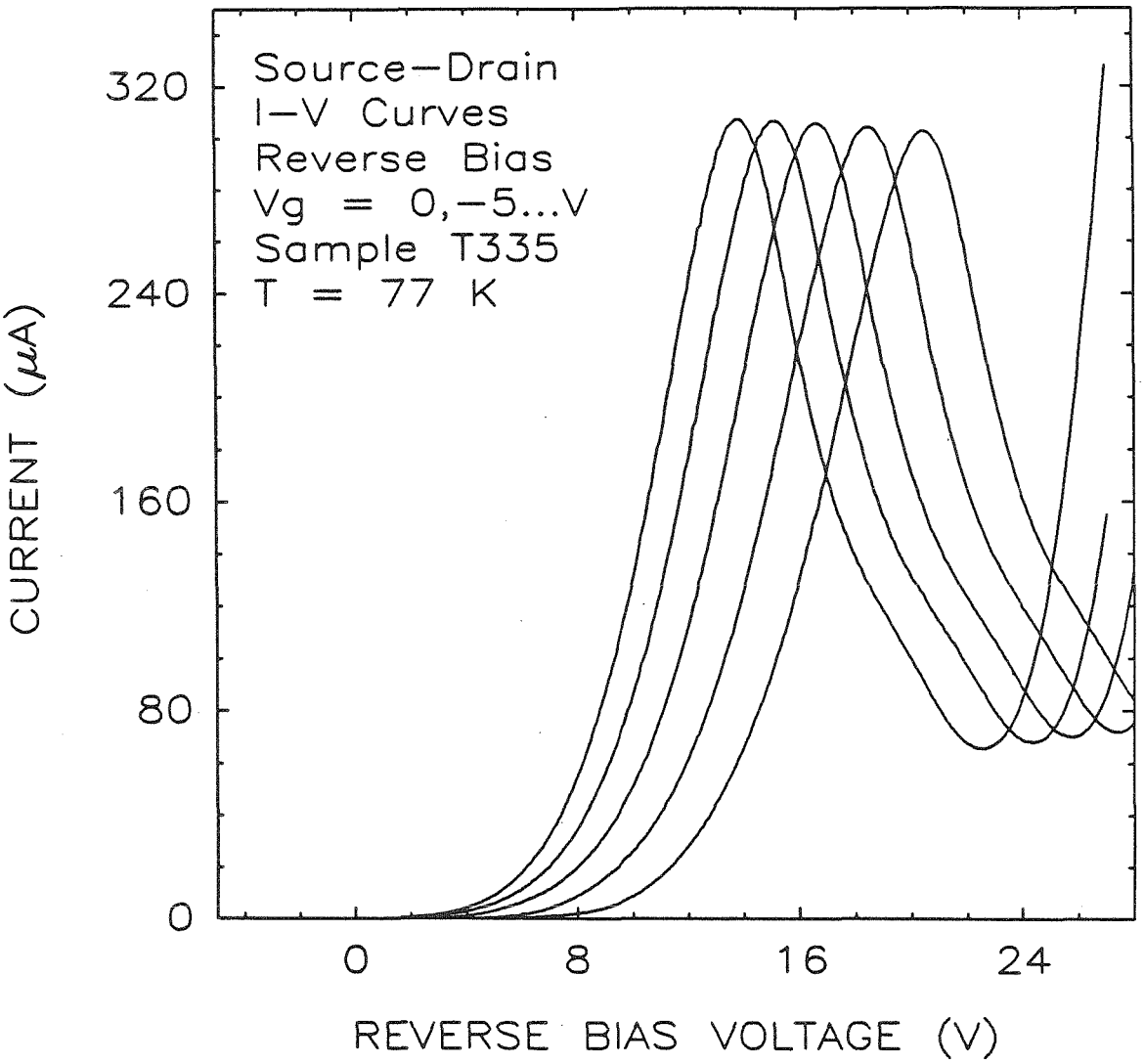

Figure 1.3: I–V curves for a DB/VFET device in reverse bias. The leftmost I–V curve was taken with zero gate bias (V_g). V_g is incremented in -5 V steps, resulting in shifts of the NDR region to larger biases.

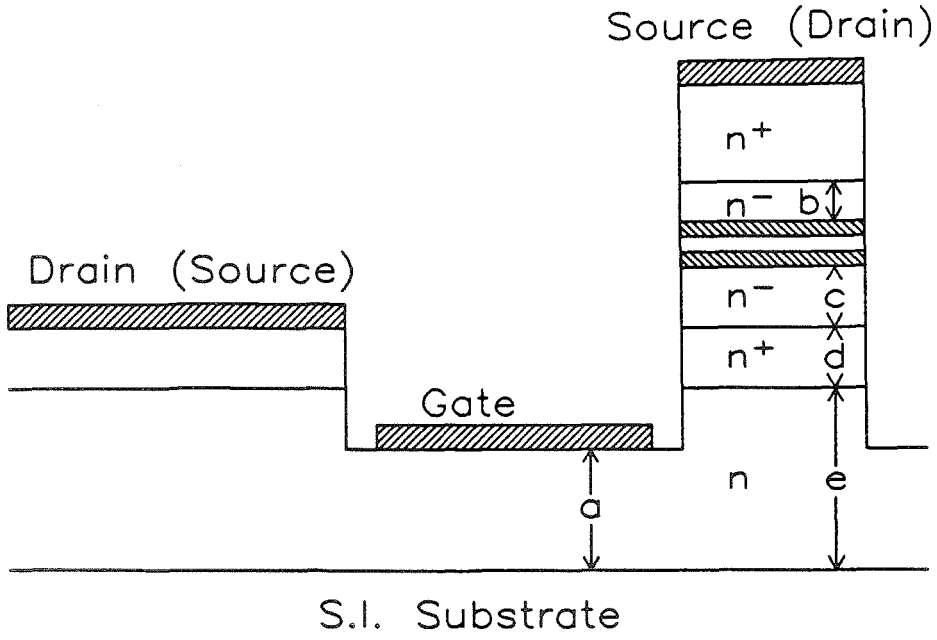

Figure 1.4: DB/MESFET cross-sectional diagram, showing recessed-gate design.

proposed, by Kesan *et al.*, which would be interesting to explore.[31] It should be possible to fabricate interesting logic elements with these structures as well. These topics are discussed in Chapter 5.

1.3.5 DB/MESFET Devices

This section deals with efforts to combine resonant tunneling diodes with planar field-effect devices, in particular a metal-semiconductor field-effect transistor (MESFET). The composite device is referred to as a DB/MESFET. This device is a logical companion to the DB/VFET.

The DB/MESFET avoids the conceptual problems associated with the DB/VFET by using a planar layout. The final device is a series combination of a double barrier and a MESFET. A finished device is schematically illustrated in Fig. 1.4. Fabrication procedures for the DB/MESFET were more complex than for the DB/VFET,

requiring 3 masks, 2 alignments, 2 etches, and 3 evaporations. The recessed-gate design was used to allow a wider latitude for channel dopings, and to ensure good ohmic contacts. Devices with channel dopings from $1 \times 10^{16}\,\mathrm{cm}^{-3}$ to $3 \times 10^{17}\,\mathrm{cm}^{-3}$ were made.

Results for a particularly instructive device are presented in Fig. 1.5. The NDR characteristic of a resonant tunneling structure is evident near zero bias, and the saturation characteristics of a MESFET are apparent at larger voltages. For zero gate bias (V_g), the resistance of the double barrier is dominant at low drain biases(V_d). As V_g is made more negative, the resistance of the FET portion of the device becomes comparable to the double barrier. The increased channel resistance results in a shift of the NDR to larger biases, followed by its eventual elimination, when the FET portion of the device becomes the dominant resistance. Note that shifts in the NDR begin to become significant at $V_g = -0.5$ V; NDR is eliminated by the time $V_g = -0.7$ V, illustrating the relative efficiency of the gate voltage in this device, as compared to the DB/VFET. The small amount of bias required to turn off the NDR may be relevant for switching applications.

This device presents a case in which the NDR lies near zero bias, in the linear region of the MESFET. It is possible to obtain a variety of other types of I–V curves. By decreasing the well width in the double barrier, the NDR shifts to larger biases. The addition of a relatively resistive channel will shift the NDR out of the linear region of the FET, resulting in bistable hysteresis regions in the I–V characteristic. By increasing the thickness of layer 'c' in Fig. 1.4, one can obtain characteristics similar to DB/VFETs. These results are discussed in more detail in Chapter 4.

Provided that successful growth of the double barrier can be obtained, the DB/MESFET is readily amenable to existing integrated-circuit fabrication techniques, because the fabrication procedures for this device can be made virtually

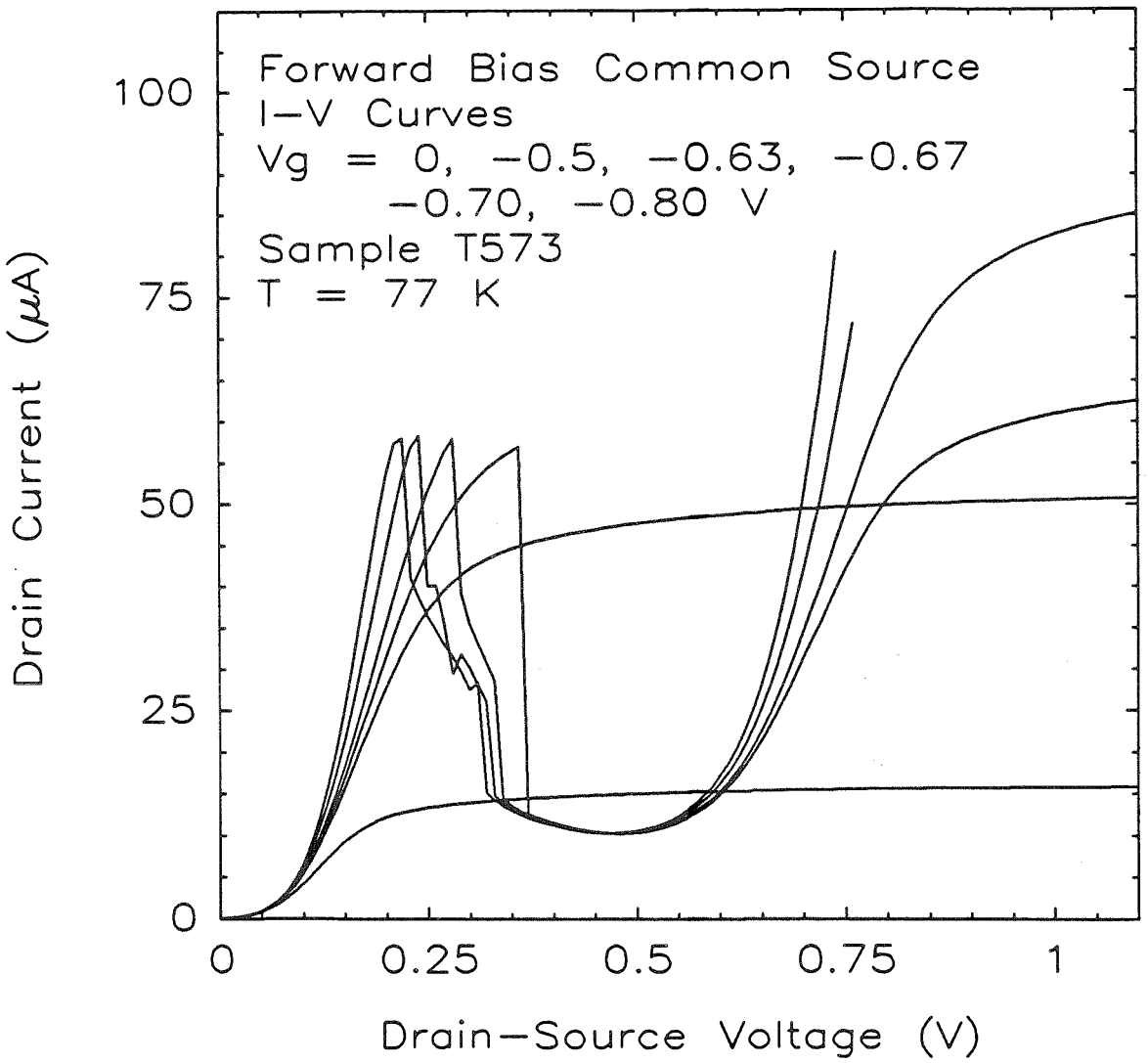

Figure 1.5: Forward-bias common-source I–V curve for a DB/MESFET device. Both resonant tunneling and MESFET behavior can be seen. The NDR peak of the $V_g = 0$ V characteristic lies closest to zero bias. As V_g is made more negative, the peak of the NDR shifts to higher biases, and is eventually eliminated, at $V_g = -0.7$ V. The 'step' in the NDR region of the curves is due to oscillation, see also Chapter 5.

identical to MESFET fabrication techniques.

Applications for the DB/MESFET lie primarily in logic and signal processing. The same features that allow frequency multiplication in the DB/VFET should work with the DB/MESFET, too. To explore one area of interest, flip-flop circuits were demonstrated using *single* DB/MESFET devices. The two stable states of the flip-flop are obtained from the bistable intersection of a load-line with the negative resistance characteristic. The states are controlled with gate bias. Two DB/MESFET samples have demonstrated this operation. Additionally, many interesting applications were developed for tunnel diodes, but fell from favor due the difficulty of integrating these devices with others.[32] Some of these applications may prove feasible with DB/MESFET devices. These topics are the subject of Chapter 5.

1.3.6 Conclusions

Two types of three-terminal NDR devices have been made. Both combine resonant tunneling heterostructures with field-effect devices. The two devices operate in different ways and exhibit characteristics qualitatively different from each other and from two-terminal double-barrier diodes. The devices presented here are pioneering efforts. Perhaps because of this, neither the double barrier nor the FET sections of the device is particularly remarkable or state of the art. It is their combination that is unique.

1.4 AlAs Capacitors

1.4.1 Introduction

This section presents an overview of the topics to be discussed in greater depth in Part II of this thesis. Here, we are concerned with the study of single-barrier

heterostructures. The particular geometry studied here consists of a layer of AlAs several thousand angstroms in thickness, separating two GaAs regions from each other. One of these GaAs regions is degenerately doped; the other is nondegenerately doped. All doping is n type. The AlAs layer is intended to form a barrier to electron transport. This topic was studied with samples produced by MOCVD. The source of the material was Xerox Research Labs in Palo Alto, California.

There are several reasons to be interested in epitaxial barrier materials. The epitaxial nature of the barrier material allows the subsequent deposition of further crystalline structures. Crystalline regrowth is much more difficult on top of amorphous layers. Resistance to electrical conduction perpendicular to the layer, and the ability to modulation-dope the barrier create some useful device possibilities.

One of these interesting devices is the GaAs-gate field-effect transistor.[33] It depends upon the ability to accumulate electrons against an $Al_xGa_{1-x}As$ barrier. This device has been demonstrated and has the potential to operate at very high speeds. This device is similar in concept to a silicon MOSFET. If the GaAs-gate FET could operate in inversion, a low-power consumption, high-speed logic system could be devised in GaAs, similar to the CMOS system in silicon. The $Al_xGa_{1-x}As$ (or $In_xAl_{1-x}As$) single barrier is important to several other devices, most notably the modulation-doped field-effect transistor (MODFET).[34] This device is currently one of the fastest transistor structures known.

1.4.2 Capacitance Measurements

In concept the n^+–GaAs/i–AlAs/n–GaAs heterostructure can be viewed as an MOS (or MIS) capacitor. The n^+–GaAs top layer behaves like a metal; the n–GaAs backside layer is semiconducting with a moderate to low carrier density. The AlAs should be a barrier; therefore, it may be either undoped, p-type, or very lightly n-type. Since this geometry would not be expected to draw a lot of current,

capacitance measurements might be informative. The theory of the MOS device is well developed.[35,36] In particular, the capacitance–voltage (C–V) behavior is well understood. Should the single barriers studied here exhibit similar C–V behavior, a GaAs-AlAs-GaAs MOSFET-like device might be possible.

All samples exhibited similar C–V behavior. Light sensitive C–V behavior was seen, with a photosensitive peak in the illuminated data being the dominant feature. The light sensitivity of the samples led to extensive nonilluminated characterization of the samples, the results of which will now be summarized.

Fig. 1.6 presents data for sample H399, taken in darkness. Arrows indicate the direction of bias sweep, and the rate of data acquisition is indicated. A dramatic drop in the size of the illuminated capacitance peak was observed in nonilluminated C–V data. A region of relatively constant capacitance is observed in forward bias. A thickness estimate can be obtained from the equation

$$C = \frac{\epsilon}{d}, \tag{1.1}$$

where C is the capacitance per unit area, ϵ is the dielectric constant of the material multiplied by the permittivity of free space, ϵ_0, and d is the barrier thickness. The thickness predicted is 2250 Å, in fairly good agreement with scanning electron microscope (SEM) measurements of 2500 Å for the AlAs thickness and suggests that the region of constant capacitance arises due to carrier accumulation against the AlAs.

A dominant feature of the dark C–V data is the observation of hysteresis. The hysteresis is rate dependent, with slowly scanned C–V data showing very little hysteresis, and no discernible peaks in the capacitance. To understand the hysteresis, bias polarities need to be thoroughly understood. Positive voltages in Fig. 1.6 refer to positive voltage on the top n^+ layer. Such a configuration is referred to as forward bias. Conversely, reverse bias occurs when negative voltage is applied to the top electrode. The nondegenerate n-type layer beneath the double

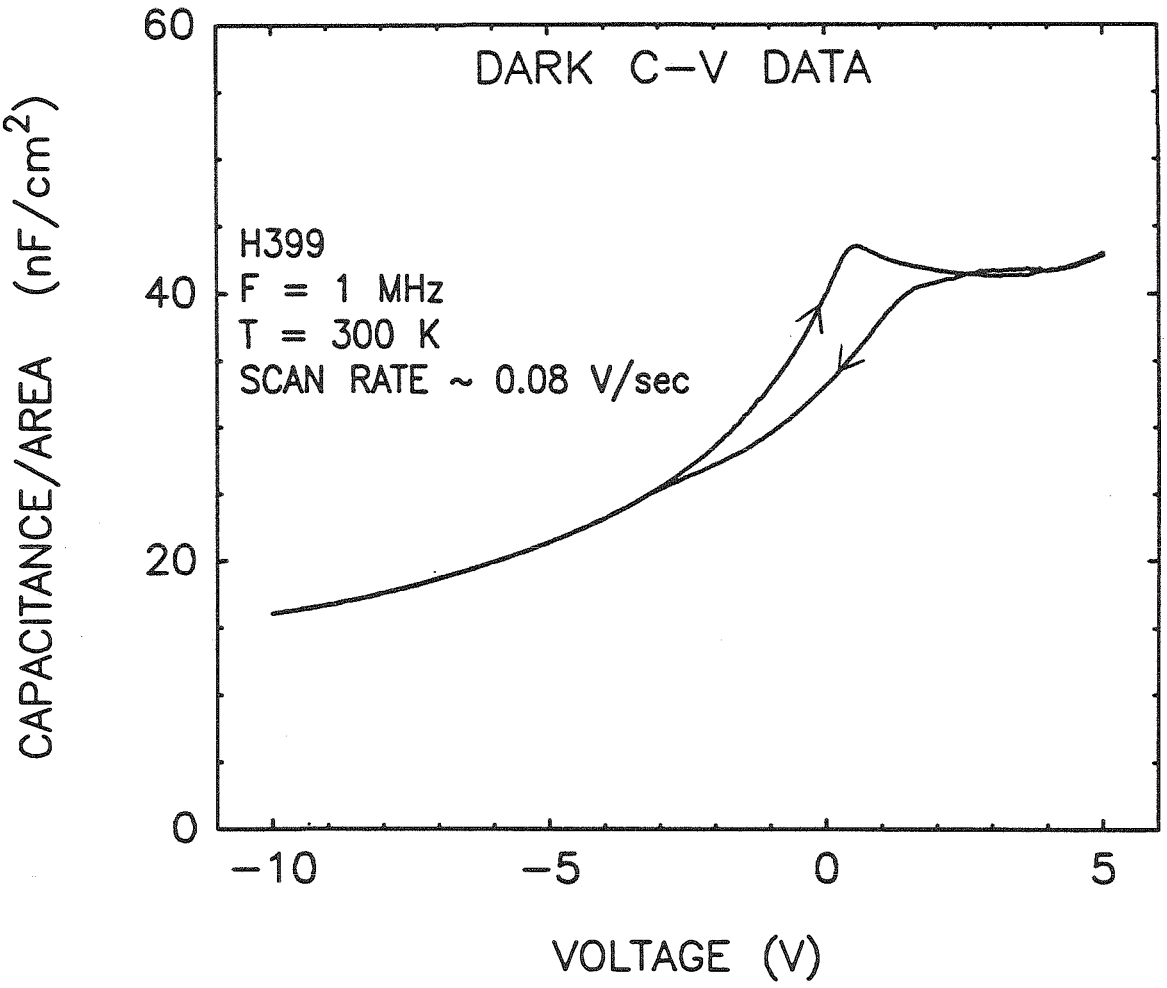

Figure 1.6: C–V data for sample H399, taken in darkness. Forward bias denotes positive bias application to the top layer of n^+GaAs. Direction of bias sweep is indicated by arrows.

barrier is depleted of carriers in reverse bias.

In the dark, for sweep rates like those illustrated in Fig. 1.6, the capacitance is higher when voltage is swept from reverse to forward bias than when swept the other way. This nonequilibrium situation is highly suggestive of the presence of a long-lived state, or deep level.[§] Since this hysteresis does not persist for the entire C–V curve, it is reasonable to suspect that the deep levels are spatially localized.

The hysteresis can be explained by considering the effect of a large number of electron traps spatially localized near the GaAs/AlAs interface (between the lightly-doped GaAs and the AlAs). These levels would be empty in reverse bias, because there would be no electrons around to populate them. An empty electron trap carries a positive charge and will drop a certain amount of bias. When most of the traps are empty, they can make a significant contribution to the charge in the depletion layer, thus allowing a smaller amount of bulk depletion, and a higher capacitance than if they were not present. When the bias on the structure becomes zero or slightly positive, electrons accumulate near the AlAs barrier, filling the levels. When bias is then swept from forward to reverse biases, the trap levels begin to empty when the depletion edge sweeps over them, but this emptying may be a slow thermal process taking many seconds. To drop a given voltage, additional depletion of the nondegenerate material will be required as compared to the forward-going sweep. Consequently, the capacitance will be lower than the forward-going case. Eventually, the trap population reaches equilibrium, and the two curves coincide with each other.

This hypothesis has been tested with the selective application of light pulses during the hysteresis. It was possible to cause the capacitance to move from

[§] A *deep level*, or *trap*, can be viewed as a spatially localized energy level lying in the forbidden gap of the semiconductor, typically far from the band edges. This level may have several charge states and is characterized by an activation energy and a capture cross section. See Ref. 37 for more information.

the branch of the hysteresis associated with filled trap states to that associated with empty trap states by application of a light pulse. See Chapter 6 for more information.

A concentration estimate for the deep levels may be made by considering the area enclosed by the hysteresis. This area can be converted to a charge, and thence to a concentration, under the assumption that all the levels fill and are emptied during the hysteresis, and that they are located at the edge of the depletion region. Values obtained at low temperature (77 K), when the hysteresis is larger, yield estimates of $1 \times 10^{11}\,\mathrm{cm}^{-2}$.

No evidence of inversion was observed in our C–V studies. Normally, a high frequency MOS C–V curve exhibits a region of constant capacitance in reverse bias corresponding to voltages at which large numbers of minority carriers are generated near the insulator interface. Since inversion is not observed, the operation of inversion-mode devices would not be possible with these structures. Many other capacitance studies were performed, including variation of temperature, sweep rate, and measurement frequency. These measurements were performed on several samples. Detailed results of these studies are presented in Chapter 6. In summary, the major results of capacitance studies are the lack of inversion, and evidence for localized deep levels.

1.4.3 DLTS Measurements

Deep-level transient spectroscopy (DLTS) allows a more detailed examination of the capacitive transient behavior seen in the previous section. DLTS is done by suddenly filling or emptying the levels and then measuring the time required for the level populations to return to equilibrium, by examining the transient capacitance of the structure. DLTS is best applied to structures whose impedance is mainly capacitive, *i.e.*, devices that draw little current. An explanation of the DLTS

technique may be found elsewhere,[8,37,38,39] and in Chapter 6.

DLTS was applied to several samples, two of which were studied in detail. Results corroborate and expand the C–V data presented previously. No trap signatures were observed until the bias on the sample during the pulse neared zero. This observation showed that the deep levels were localized at or near the interface between the AlAs and the low doped GaAs, with possible extension into the AlAs evidenced by increase in trap signature for forward-bias pulses.[¶] Some evidence for an interface character to the levels was seen.

Activation energies were measured for both samples. Both samples showed activation energies of about 500 meV. Capture cross sections consistent with a very long trap emission time (many seconds) were obtained, in agreement with C–V data. It is interesting that both samples exhibited nearly identical trap signature, suggesting that the same trap is seen in *all* the samples. The attributes of the level indicate that it might be a 'DX' center.[40]

Concentration estimates can be performed using a standard method.[39,41,40] This method underestimates the true trap concentration, particularly when the deep-level concentration approaches that of the shallow level. Thus, the estimate of $1 \times 10^{15}\,\mathrm{cm}^{-3}$ obtained in this manner is probably too low. A sheet concentration of $1 \times 10^{10}\,\mathrm{cm}^{-2}$ is obtained if these levels are assumed to be distributed over 1000 Å, which is lower than that obtained by C–V estimates.

DLTS studies yield several supporting pieces of information. Deep levels were identified and localized to an area near the GaAs/AlAs interface. Since evidence of the traps continued to be seen when the devices were pulsed into forward bias, they may also be distributed in the AlAs. The extent to which the AlAs was probed is not known, because the amount of AlAs being scanned by the trap-filling pulses is uncertain. Very similar results were obtained for two samples, suggesting that the

[¶]Forward-bias DLTS behavior showed some evidence of conduction.

same level is present in all samples.

1.4.4 Current–Voltage Measurements

I–V measurements were made on all samples. Measurements were made both with and without illumination. The samples draw very little current when not illuminated. Illuminated *I–V* curves are the subject of the following section. When examining the *I–V* curves of nonilluminated samples, hysteresis could be observed. This hysteresis was investigated as a function of rate, temperature, and illumination.

In Fig. 1.7, *I–V* data for a representative sample are presented. No light falls on the sample over the voltage range depicted. The direction of bias sweep is indicated. When bias is swept from negative to positive, a sudden jump in current is observed, which persists until large-scale conduction is observed at the far right of the figure. This current step is not seen when bias is swept the other way.

The hysteresis seen in Fig. 1.7 can be explained by the same deep levels evidenced in *C–V* and DLTS measurements. Consider the case in which bias is swept from reverse to forward values. At large reverse biases, the trap levels should be depopulated of electrons. The sample can be briefly exposed to light in reverse bias, to ensure the depopulation of the levels. As voltage becomes positive, electrons are brought near the trap levels, and they begin to fill. The trap filling represents a removal of carriers from the circuit. This time rate of change of carriers is the current enhancement observed.

When bias is swept from forward to reverse values, the trap levels are filled at the start of the sweep. As the depletion layer envelops the deep levels, they begin to empty thermally. This process does not suddenly change the number of carriers in the circuit, so no current jump is seen.

Trap-level concentration estimates may be made by considering the area under

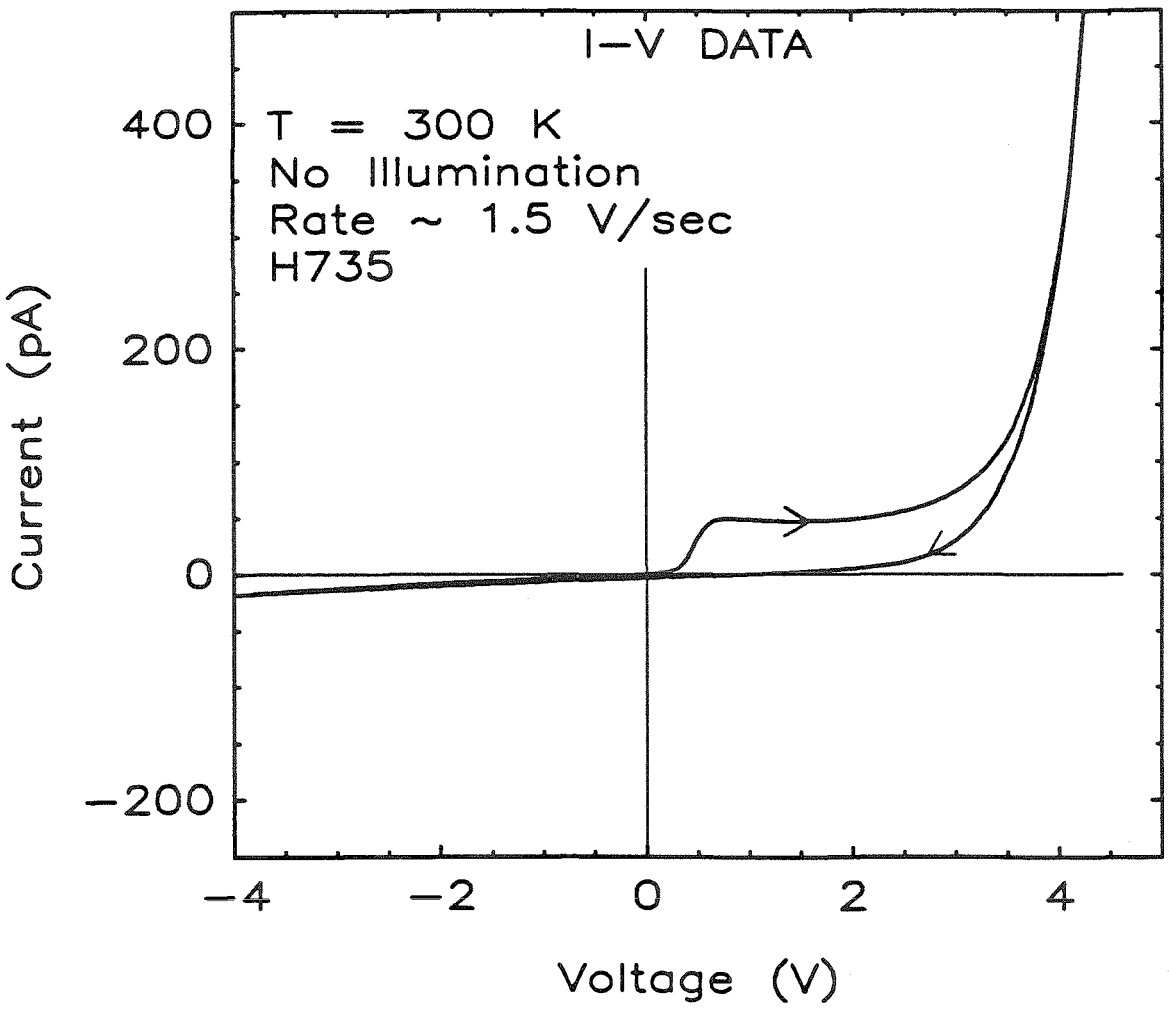

Figure 1.7: *I–V* curves for sample H735 at room temperature. Direction of sweep is indicated by arrows. In the forward-going sweep, trap levels were emptied at about −5V by brief exposure to light. The hysteresis is due to trap-filling effects.

the current step. This area may be converted to a charge, and then to a sheet concentration. One obtains a value of $3 \times 10^{11}\,\mathrm{cm}^{-2}$, which is in good agreement with estimates made from C–V data. The current jump was investigated as a function of temperature and sweep rate. More details of this work are contained in Chapter 6.

1.4.5 Conclusions

This section has described electrical measurements on AlAs capacitor structures that were grown by MOCVD. An analogy to MOS or MIS devices was put forward and seen to be inadequate to explain the C–V behavior of the device. A lack of inversion was seen under all conditions. Light sensitive C–V and I–V behavior was observed. Hysteresis in the C–V and I–V data was observed. These effects were attributed to deep levels in the sample, which were observed more directly with DLTS techniques. Trap-level concentration estimates were obtained from all three techniques and were in rough agreement with one another.

The results of this study have implications for devices. The lack of inversion observed make the devices unsuitable for use as inversion-mode FETs. GaAs-gate FETs operating in accumulation mode may be possible, since the devices can sustain several volts before forward conduction begins. The deep levels evidenced in C–V, I–V, and DLTS studies would degrade the operation of such a device, because they would decrease the number of carriers in the accumulation layer. More work on the production of high-quality MOCVD AlAs films is needed before these materials will be useful in devices.

1.5 Photoresponse Measurements

This section reports some new experimental results in the photoresponse behavior of single-barrier heterostructures. Photoresponse measurements record the electrical response of a device as a function of the light energy falling on it and can provide information about the device. The behavior of our AlAs single-barrier heterostructures differs from that of symmetric thin-barrier samples, whose photoresponse has been reported by Schlesinger *et al.*[42,43]

The photocurrent response of several samples was studied. All samples showed similar behavior. These are the same samples on which the electrical measurements described in the previous section were performed. Photocurrent measurements are made while the sample is illuminated. Therefore the deep levels present in the samples are empty and are not expected to play a dominant role in determining the photoresponse.

The basic photoresponse phenomena of interest are well illustrated by considering a DC I–V curve taken under illuminated conditions. Such a curve is presented in Fig. 1.8. Recall that forward bias refers to positive voltage on the degenerately doped top layer of GaAs. Positive current enhancement is observed in forward bias, as compared to the nonilluminated data presented in Fig. 1.7. No hysteresis was evident for illuminated data. In reverse bias, negative current enhancement is observed. Data of this sort were taken for several samples, at a variety of temperatures ranging from 80 to 320 K.

Positive current is seen when positive charges travel from the front to the back of the sample, or when electrons travel from the back of the sample to the front. These data do not delineate between electron and hole current, but since the samples are entirely n-type it is reasonable to expect that the current enhancement observed is due to a net electron transport. Energy-resolved photocurrent studies confirm that the motion of electrons creates the observed current. The data of

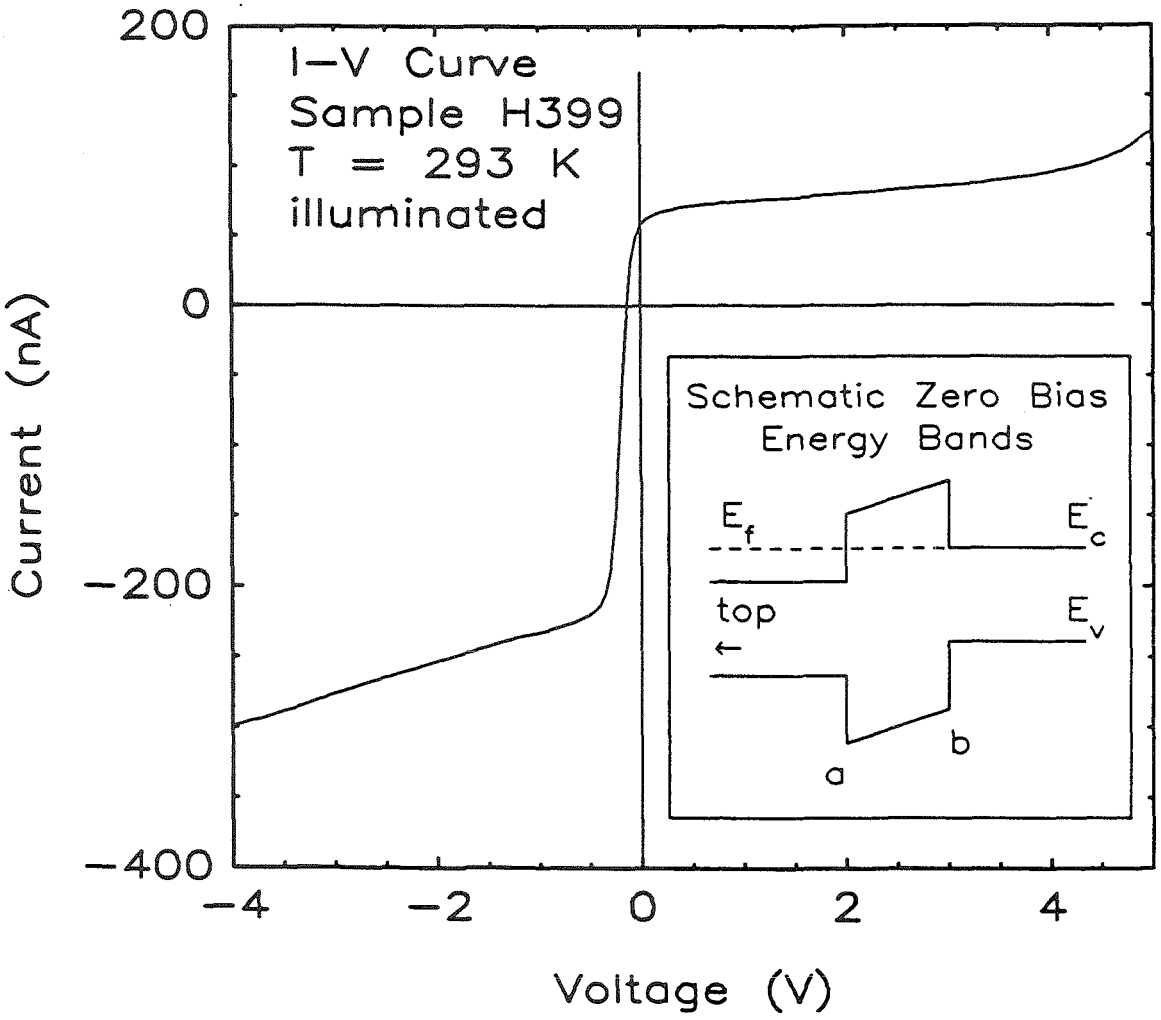

Figure 1.8: *I–V* data for a representative sample (H399) taken at room temperature under incandescent illumination. Zero-bias photocurrent is consistent with electron transport from the back of the sample to the front. The inset shows a schematic band diagram for the structure at zero bias. The schematic is not drawn to scale and does not include band bending.

Fig. 1.8 clearly indicate a net transport of electrons from the back of the sample to the front in forward bias. This transport is not difficult to understand, because the bias on the sample favors electron transport in this direction. Similarly, negative current enhancement is observed in reverse bias.

Consider the zero-bias photocurrent. This current is positive, consistent with net transport of carriers from the back of the AlAs to the front at zero external bias. This result differs from that obtained with symmetric structures[43], and is curious, since the doping concentration in the top layer of GaAs is greater than that on the back side of the barrier. In addition, since the structure is illuminated from the top side, there are more photons in the top layer than in the back layer.

In the samples studied here the AlAs plays an important role. The AlAs is thick enough to allow significant energy loss to take place across it. This fact makes the presence of an electric field in the AlAs important. Depending on the bias conditions, the conduction-band edge of the AlAs will be at a higher energy at either interface (a) or interface (b), as labeled in the inset of Fig. 1.8. Suppose interface (b) is at a higher energy than interface (a). Then backside electrons will be collected as soon as they cross this interface, whereas photoelectrons generated in the top layer must cross the entire AlAs barrier before reaching the highest energy barrier.

There are two interfaces, but only one is important for current collection. It is the concentration gradient of photoexcited electrons across this "collecting interface" that drives the photocurrent. At zero applied bias, there is a built-in voltage across the AlAs layer, due to doping asymmetries in the structure. This built-in voltage places the collecting interface at (b) in Fig. 1.8, and explains why positive photocurrent might be expected at zero bias. When bias becomes negative, this interface shifts to position (a) of the figure. Now the collecting interface is nearest the region of greatest electron and photon population, explaining the greater

current enhancement observed in reverse bias as compared to forward bias.

More detailed studies of these photocurrent mechanisms were made to test this explanation of the photoresponse of the structures. These experiments were performed with optical apparatus that permitted exposure of the sample to well-defined photon energies. Photocurrent can then be measured as a function of the incident photon energy. These studies were very interesting and confirmed the explanations presented here. These data can be found in Chapter 7.

1.6 Guide to Remaining Chapters

Chapter 2 begins Part I of the thesis and contains an assortment of topics not appropriate for other chapters. A detailed review of the current theoretical literature on double barriers begins the chapter. The successful MBE production of double barriers, recently accomplished in our research group, is described next. Finally, the MOCVD growth process is summarized, and various three-terminal device concepts are discussed. Chapter 3 begins begins the discussion of the major work of the thesis. This chapter is concerned exclusively with the DB/VFET device. The concept, design, fabrication, testing, and analysis of this device are described in Chapter 3. Chapter 4 continues in a similar vein, but for the DB/MESFET device. Chapter 5 switches gears a bit, by describing some basic applications of the DB/VFET and DB/MESFET devices. These applications were only briefly touched on in Chapter 1.

Chapters 6 and 7 make up Part II of the thesis. These chapters are concerned with the investigation of single-barrier AlAs capacitor structures. The electrical measurement of these devices is the subject of Chapter 6, with some introductory material at the beginning of the chapter. Chapter 7 describes some optical characterization measurements, in the form of photoresponse behavior.

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Part I

RESONANT TUNNELING TRANSISTORS

Chapter 2

Double Barriers and Three-Terminal Devices: Background, Theory, and Materials

This chapter covers a variety of topics in an introductory manner. The theory of the double barrier, growth of the structure, and basic three-terminal device concepts are the topics to be discussed. Except for the results of our work on the MBE growth of double barriers presented in Section 2.3 and the discussion of the transistors at the end of the chapter, the material contained in this chapter is in the nature of a review article.

2.1 Outline and Summary of Results

Even though this is an experimental thesis, an understanding of the basic theory of the double barrier is important. Therefore, a review of the existing literature

on the theory of the double barrier will be presented. Following this, a recently undertaken project to produce double barriers by MBE is described, and our initial experimental results are presented. $Al_xGa_{1-x}As/GaAs/Al_xGa_{1-x}As$ double barrier diodes (DBDs) with 300 K NDR have been grown. After this, the MOCVD growth process is discussed, and important points relating to the growth of double barriers by MOCVD are mentioned. The chapter concludes with a discussion of three-terminal device concepts.

2.2 Theory of the Double Barrier

This section contains a summary of the current theoretical understanding of the double-barrier heterostructure, as determined from a literature review. This thesis is of an experimental nature. Therefore, this review has been conducted with an eye to experimentally relevant parameters, such as transit times and P/V current ratios. The material presented in this section provides background, but is not essential to the understanding of the experimental data composing the bulk of the thesis.

The DBD, as the two-terminal resonant tunneling heterostructure is often called, has been the subject of intense theoretical study, as described in References 1 through 15. The most important single concept obtained from a review of this literature is that extensive theoretical calculation has been only partially successful in modeling real DBDs. Therefore, experimental results tend to drive the field, rather than theoretical prediction. Nevertheless, there are a number of valuable insights to be gained from a basic theoretical consideration of the device.

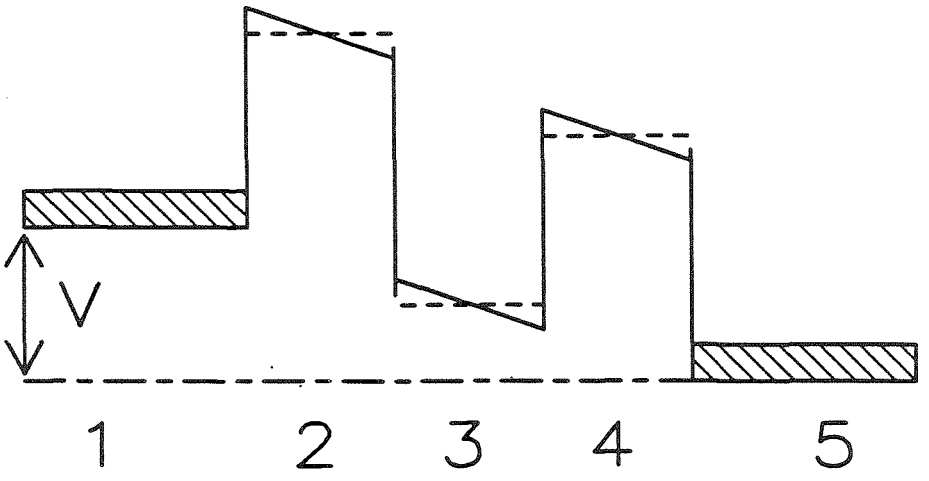

Figure 2.1: Simple band diagram for double barrier. Regions 1 through 5 are labeled. Approximations to rectangular barriers are indicated by the dashed lines.

2.2.1 Expression for Current

The basic potential diagram for the structure is presented in Fig. 2.1. We wish to find the current through such a structure. Two basic assumptions are made, which reduce the three-dimensional problem to a one-dimensional case:

1. Conservation of the component of the electron wavevector parallel to the interfaces ($k_{||}$).

2. Conservation of total energy during the tunneling process.

An equation for the current from region 1 to region 5 can be derived from considerations of the carrier distribution region 1, the transmission coefficient for the double-barrier structure, and distribution of empty states in region 5. It can (imprecisely) be thought of as writing down $j = nev$ for the structure in k–space. This procedure was outlined in Ref. 1. The result is

$$J = \frac{2e}{(2\pi)^3\hbar}\int d^3k\,|T(E_1)|^2[f(E_1) - f(E_5)]\frac{\partial E_1}{\partial k_z}\,, \tag{2.1}$$

where E_5 is the energy of the electron in region 5, and E_1 is the energy in region 1, related by $E_5 = E_1 + eV$, where V is the applied voltage. T(E) is the transmission coefficient, e is the electron charge, and f(E) is the Fermi distribution in each electrode. The transmission coefficient is taken to be symmetric and a function of only that part of the energy perpendicular to the barriers, which can be written

$$E = E_{\|} + E_{\perp} = \frac{\hbar^2}{2m^*}\left[(k_{\perp})^2 + (k_{\|})^2\right]. \tag{2.2}$$

In rectangular coordinates $k_{\|} = \sqrt{k_x^2 + k_y^2}$, with k_z acting as $k_{\perp}$. The three-dimensional integral is reduced to a single integral over the perpendicular component of the energy in region 1 by doing the integration over the parallel k vectors. This integration can be done analytically, yielding a final expression[1]

$$J = \frac{ekTm^*}{2\pi^2\hbar^3}\int dE_{\perp}|T(E_{\perp})|^2 \ln\left\{\frac{1+\exp\left(E_{f1}-E_{\perp}\right)/kT)}{1+\exp\left(E_{f5}-E_{\perp}-eV\right)/kT}\right\}, \tag{2.3}$$

where E_{fi} is the Fermi energy in region i.

2.2.2 Transmission Resonances

A basic method for calculating the transmission coefficient has been developed.[1,2] This method utilizes a transfer matrix to connect the wave function from one side of the structure to the other. Separating variables in the time independent Schrödinger equation along the same lines described above ($k_{\|}$ and $k_{\perp}$) allows the wave function to be written as a product of plane waves in the parallel direction, and leaves a one-dimensional problem in the direction perpendicular to the barriers. For the approximation of constant potentials and rectangular barriers, the solutions are of the form:

$$\Psi(z)_i = a_i e^{ik_i z} + b_i e^{-ik_i z}\ , \tag{2.4}$$

where $k_i \equiv \frac{1}{\hbar}\sqrt{2m^*(E_\perp - \Phi_i)}$ is the wavevector in region i, with Φ_i being the potential there.* These solutions are valid in regions of constant potential, and must be matched to each other across the various interfaces. The appropriate boundary conditions at the interface between region i and region $i+1$ are[3]

$$\Psi_i = \Psi_{i+1}\,, \tag{2.5}$$

$$\frac{1}{m_i^*}\frac{d\Psi_i}{dz} = \frac{1}{m_{i+1}^*}\frac{d\Psi_{i+1}}{dz}. \tag{2.6}$$

The addition of the effective mass in the derivative boundary condition is required to conserve current through the structure.

These boundary conditions may be appropriately described as a 2×2 matrix operating on the coefficients of the solutions in each region.[2]

$$\begin{pmatrix} a_1 \\ b_1 \end{pmatrix} = \mathbf{M_1} \begin{pmatrix} a_2 \\ b_2 \end{pmatrix}\,, \tag{2.7}$$

where $\mathbf{M_1}$ is the transfer matrix between region 1 and region 2.

This technique can be applied to an arbitrary number of barriers by simply stringing together the transfer matrices. There are four basic forms of M, depending upon the types of potentials are being connected.[4] Assume that region 5 is the electrode region, wherein there is no reflected wave ($b_5 = 0$). One then can obtain an expression for the transmission from region 1 to region 5:[2,4]

$$|T|^2 = \frac{|a_5|^2 k_5}{|a_1|^2 k_1} = \frac{k_5}{k_1 |\mathbf{M_T}|_{11}^2}\,, \tag{2.8}$$

where

$$\mathbf{M_T} = \mathbf{M_1 M_2 ... M_4}. \tag{2.9}$$

The precise expression for $|T|^2$ is complicated[2], but it approaches 1 when the energy of the incident particle satisfies a particular condition:[4,2]

$$k_3 d_3 = \tan^{-1}\left(\frac{k_2}{k_3}\right) + \tan^{-1}\left(\frac{k_4}{k_3}\right) + (n-1)\pi\,, \tag{2.10}$$

*This expression for k comes from a one-band model.

where d_3 is the width of region 3. Physically, this condition is satisfied when the incident energy matches the energy of the quasi-bound state in the quantum well. Eq. 2.10 defines the positions of the resonance levels in the quantum-well region. In a real structure it is possible to quench this resonance by dropping the quasi-bound state below the band edge of region 1, thus preventing Eq.2.10 from being satisfied, and creating a NDR region. The full width at half maximum (FWHM) of the transmission resonance is usually referred to as the resonance width (Γ).

The transfer matrix technique was introduced by Kane[2], and applied by Tsu and Esaki to a finite superlattice and to the double-barrier case.[1] It was extended to trapezoidal barriers by Vassell *et al.*, and was given a very thorough exposition by Araki.[5,6] Ricco and Azbel have extended the technique to an arbitrary potential and obtained an equation for the resonance condition, similar to Eq. 2.10 above;

$$\int_a^b k_3(z)\,dz = \tan^{-1}\left[\frac{k_3(a)}{k_2(a)}\right] + \tan^{-1}\left[\frac{k_3(b)}{k_4(b)}\right] + (n-1)\pi\,, \qquad (2.11)$$

where the integration runs between the classical turning points in the quantum well at a and b. Since the potential may vary continuously, k becomes a function of z, and $k_i(z)$ refers to the wavevector at a particular point z in the appropriate region.

The above formalism enables one to deal with the case of an arbitrary potential profile, which is very important for accurately determining the position of the resonance and the true transmission coefficient. A framework for calculating the band-bending via numerical solution to Poisson's equation has been developed by Bonnefoi.[7,17] Using this accurate representation of the potential profile, Eq. 2.11 can be used to determine the energies, and thence the voltages, at which the resonances occur.[7]

2.2.3 Barrier Heights

The height of the barrier in the double-barrier structure is important in determining the transmission, because it plays a role in determining the resonance width, and also affects other undesirable current mechanisms, such as thermionic emission. A serious question has developed in the GaAs/AlAs system as to what barrier height is seen by the electrons in the GaAs, because AlAs is an indirect band gap material, whereas GaAs is direct. The conduction band offset between the direct Γ valleys in both materials is large, about 1 eV. Between the Γ point in GaAs and the X point in AlAs is a band offset of about 0.2 eV. The precise value of the band offset between the two materials continues to be a point of some debate.[18,19,20] †

Recently, experimental evidence for at least partial X point transport has been found by Bonnefoi. This evidence takes the form of resonant tunneling current peaks, which can be correlated to quantum-well states confined by AlAs X-point barriers.[7] Others have claimed that the Γ barrier is the important one.[21] The exponential

$$e^{ik_i x} = \exp\left[-\frac{1}{\hbar}\sqrt{2m^*(\Phi_i - E_\perp)}\right] \tag{2.12}$$

measures the decay length for the penetration of a state into the barrier. This exponential decay has different magnitudes, depending upon whether X point or Γ point values are used. This suggests that barrier thickness, as well as scattering, may be important in determining the degree to which Γ or X point transport is observed.[22]

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† These are only three papers of a large body of literature on this topic.

2.2.4 Peak-to-Valley Ratio

Having obtained the transmission coefficient via this mechanism, the current through the structure may be calculated. Results fail to agree with experiment in a rather spectacular fashion. Wu has calculated the peak-to-valley ratio in an elastic approximation. Typical values ranged from about 10^4 to over 10^6, as barrier thickness varied from 20 to 40 Å. More details may be found in Ref. 8. This discrepancy is believed to be due to the idealized nature of both the postulated structure and the method used to calculate the result.

2.2.5 Resonance Width

The width of the transmission resonance (Γ) is an important parameter. It plays a role in determining the peak-to-valley ratio, as well as determining the resonance lifetime ($\tau = \hbar/\Gamma$), which is important in determining the overall speed of the structure. Values of less than 0.1 to more than 1 meV have been obtained for the ground state, using the elastic formalism described above, for a typical AlAs/GaAs/AlAs double barrier (assuming the Γ–Γ band offset).[6] This half width corresponds to a resonance time ranging from 7×10^{-12} sec. to 7×10^{-13} sec. Other estimates for the resonance time as long as 10^{-11} sec. have been made, using a multiple reflection method of calculation.[9] Inasmuch as scattering times may be as fast as 10^{-13} sec, inelastic effects may be important.[9]

2.2.6 Inelastic Effects

This section describes what happens when energy conservation assumptions are relaxed in the calculation of the transmission. The introduction of inelastic scattering will broaden the resonance and decrease the peak-to-valley current ratio. These effects are difficult to incorporate into the transfer matrix technique outlined

above. Wu has incorporated phonon scattering effects into a calculation of the peak-to-valley current ratio and observed dramatic effects. The peak-to-valley ratio was decreased by as much as a factor of 1000.[8] Even so, the predicted peak-to-valley ratio was about 1000. Bonnefoi describes a variety of inelastic tunneling mechanisms that could be important for the double barrier, including phonon-plasmon coupling and impurity assisted tunneling.[7]

The structure of the transmission coefficient is of primary interest near its resonances. An approximate form for the near-resonance transmission coefficient has been obtained by Stone and Lee, utilizing a Breit-Wigner formalism.[10] The particularly interesting thing about this formalism is that inelastic effects can be included in a relatively convenient manner. Expressions for $|T|^2$ appear below, for purely elastic (T_e) and a combination of inelastic and elastic effects (T_{e+i}).

$$|T_e|^2 = \frac{(\frac{1}{2}\Gamma_e)^2}{(E-E_r)^2+(\frac{1}{2}\Gamma_e)^2}, \tag{2.13}$$

$$|T_{e+i}|^2 = \frac{\frac{1}{4}\Gamma_e\Gamma}{(E-E_r)^2+(\frac{1}{2}\Gamma)^2}, \tag{2.14}$$

where Γ_e is the elastic resonance energy width, $\Gamma = \Gamma_e + \Gamma_i$ with $\hbar/\Gamma_i$ being the inelastic scattering time. At the resonance energy ($E = E_r$), the transmission coefficient is reduced by Γ_e/Γ. NDR will continue to be observed, but inelastic effects may cause the P/V current ratio to decrease, although this point is not universally accepted.[9,12]

Brown *et al.* have used a generalization of Eq. 2.14 and Eq. 2.3 to obtain an analytic approximation for the current near resonance.[11] This quasi-empirical calculation was obtained using MODFET mobilities to obtain the inelastic scattering time (and therefore Γ_i), and by requiring Γ_e to have a value such that the peak experimental current was obtained. The resonance width (Γ_e) obtained was 1.65 meV.[11]

For elastic tunneling, the wave-function of the electron is coherent from one

electrode to the other, and is referred to as *coherent* tunneling. As we have seen, inelastic effects can be important. If tunneling were entirely inelastic, it could be thought of as *sequential* in nature. NDR can be seen in both types of transport. The extent to which each effect is taking place will not be addressed here. The term "resonant tunneling" will be used without regard to sequential or coherent implications, as a generic term referring to the current transport through a double-barrier structure.

2.2.7 Speed Considerations

The speed of the double barrier is in some sense related to the resonance time ($\tau = \hbar/\Gamma$). As mentioned previously, these times vary between 10^{-12} and 10^{-13} sec. There have been a number of theoretical attempts to predict the speed of the double barrier. Some estimates of the upper bound on the speed have already been exceeded by experiment. Several authors have proposed models that predict intrinsic frequencies in the Terahertz range.[13,14,15] Logic switching times of 1 picosecond or less have also been predicted.[15] Experimentally, an optical measurement of the resonant lifetime has been made, and is in basic agreement with the $\tau = \hbar/\Gamma$ theoretical prediction, for relatively long lifetimes of 60 to 200 picoseconds, with Γ calculated by the methods outlined in this chapter.[16] Shorter lifetimes need to be investigated.

There are a variety of other effects that probably have more bearing on the maximum oscillation frequency in a DBD. These have to do with parasitic effects, and transit-time delays elsewhere in the structure. Brown *et al.* have made attempts to model the speed of high-frequency DBD oscillators by calculating the dynamic negative conductance of the double barrier and the transit time delay, as well as series resistance effects. These estimates have shown that currently realizable structures could have maximum oscillation frequencies of 600 GHz in an

AlAs/GaAs/AlAs structure.[11]

2.2.8 Summary

Our review of the state of current theoretical efforts in resonant tunneling is now concluded. As can be seen, the field is somewhat turbulent. The major problems seem to result from the basic assumptions of energy and $k_{||}$ conservation. The appropriate way to relax these assumptions is at the center of the current theoretical debate. The usual method by which theory is compared to experiment is to compute a basic theoretical curve, using the methods of Tsu and Esaki[1], and to require the peak current to match experiment.

2.3 MBE Growth of Double Barriers

Molecular beam epitaxy (MBE) is an epitaxial layer deposition technique. This technique has been widely applied to the production of resonant tunneling heterostructures. It has achieved widespread popularity in research circles because of the high degree of control it allows over very thin layers. This section briefly presents the initial results of a program of research into the behavior of novel structures produced by MBE. The first test of this program was the production of $Al_xGa_{1-x}As$/GaAs double barriers.

The MBE process has been extensively studied. The literature on the growth process, as well as the quality of the films produced, is voluminous. An excellent review of the subject is contained in Ref. 23. The MBE process is an ultra-high vacuum technique in which molecular beams of elemental materials are directed at a heated substrate. The molecules physically adsorb to the surface, where they are incorporated into the film by bonding to nearby atoms. The molecular beams are created by heating a pure sample of the desired material. The heating is usually

done with a heated effusion cell. These cells may be shuttered to allow controlled deposition. Ideally, this method allows very abrupt transitions from deposition of one type of material to another; ideal for the creation of abrupt heterojunctions. Control of film thickness to single monolayer levels is possible through the use of reflected high-energy electron diffraction (RHEED) off the growing film.[23]

These factors make MBE an excellent vehicle for the creation of heterostructures. The growth of the DBD is a good test of such a growth technique, because the structure is very sensitive to interface abruptness, uniformity, and impurity distributions. These effects would all tend to broaden the transmission resonance and decrease the peak-to-valley current ratio by increasing inelastic effects.

2.3.1 Results

A Phi 430 MBE system was installed in our class 10,000 clean room facility in August 1987. This system was used for the deposition of GaAs, AlAs, and alloys, with the facility of n-type doping with Si. We have recently attempted the fabrication of DBDs utilizing this system. The basic geometry for two samples is outlined in Table 2.1

The dimensions of the double barrier were chosen primarily from our background with double barriers and also from a review of the literature. The spacer layers between the heavily doped contact regions were inserted to diminish thermal effects and impurity scattering effects.[24,25] The contacts were doped heavily to reduce contact resistance.

Results for two samples are illustrated below. These represent the first working double barrier produced in the system, and a refinement of that growth. One observes considerable improvement from relatively small modifications to the doping structure, particularly at room temperature.

The major problem with Sample III-33 is believed to be an asymmetry in the

MBE DBD geometry

Layer No.	Composition	Doping (cm^{-3})	Thickness (Å) III-33	Thickness (Å) III-47
Substrate				
1	GaAs	2×10^{18}	5000	5000
2	GaAs	$\sim 5 \times 10^{16}$	500	500
3	$Al_xGa_{1-x}As$	undoped	55 ($x \sim 0.32$)	60 ($x \sim 0.45$)
4	GaAs	undoped	50	60
5	$Al_xGa_{1-x}As$	undoped	55 ($x \sim 0.32$)	60 ($x \sim 0.45$)
6	GaAs	$\sim 5 \times 10^{16}$	500	500
7	GaAs	2×10^{18}	2500	2500
Surface				

Table 2.1: Geometry for MBE double-barrier growths. $x \sim Y$ refers to the Al mole fraction in the barriers.

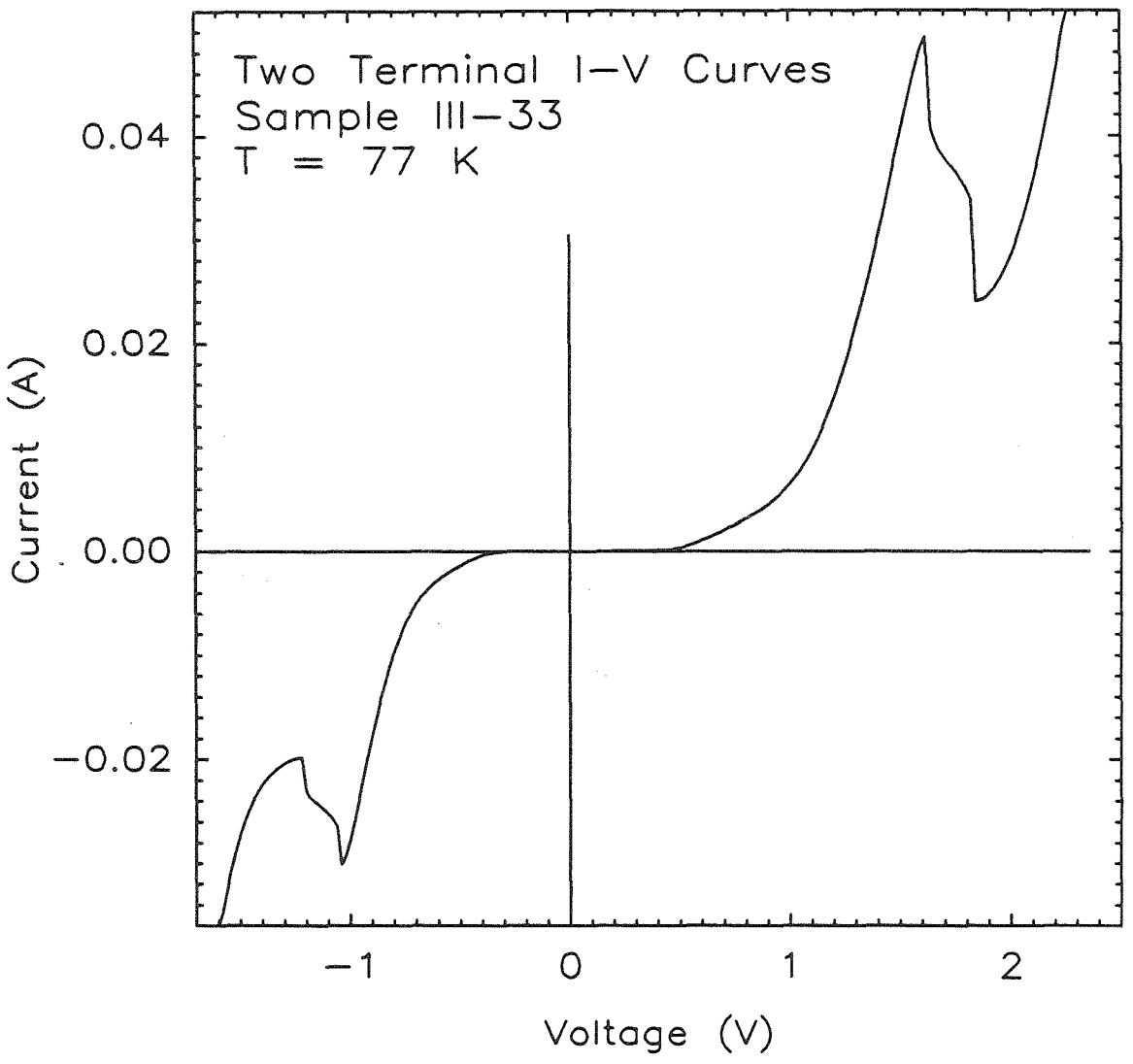

Figure 2.2: *I–V* curves for sample III-33, at 77 K. Asymmetry is attributed to buffer-layer doping asymmetries. Several samples of similar geometry exhibited NDR in only one bias direction. This was our first double barrier sample.

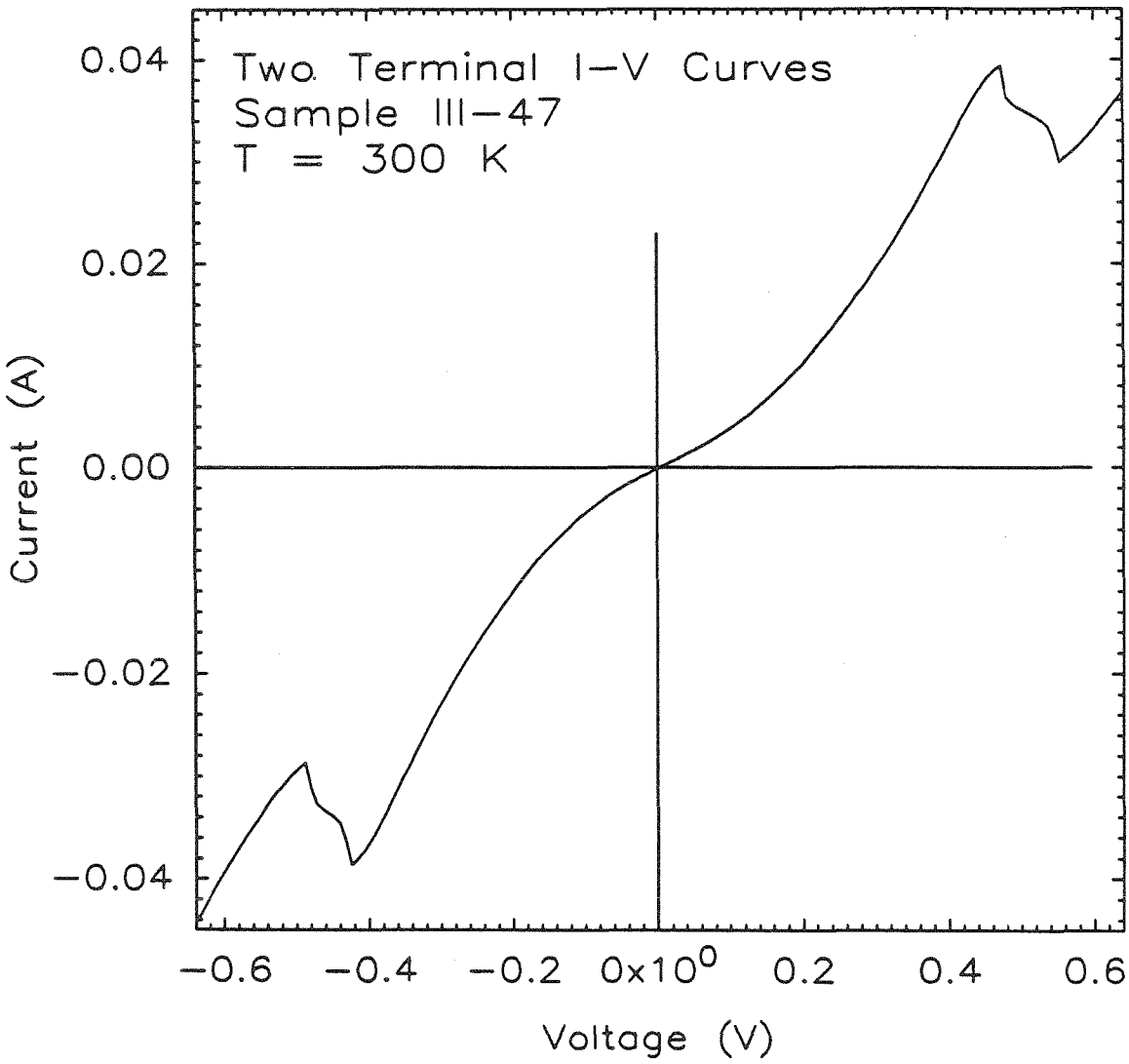

Figure 2.3: *I–V* curves for sample III-47, at 300 K. Peak-to-valley ratio is about 1.5.

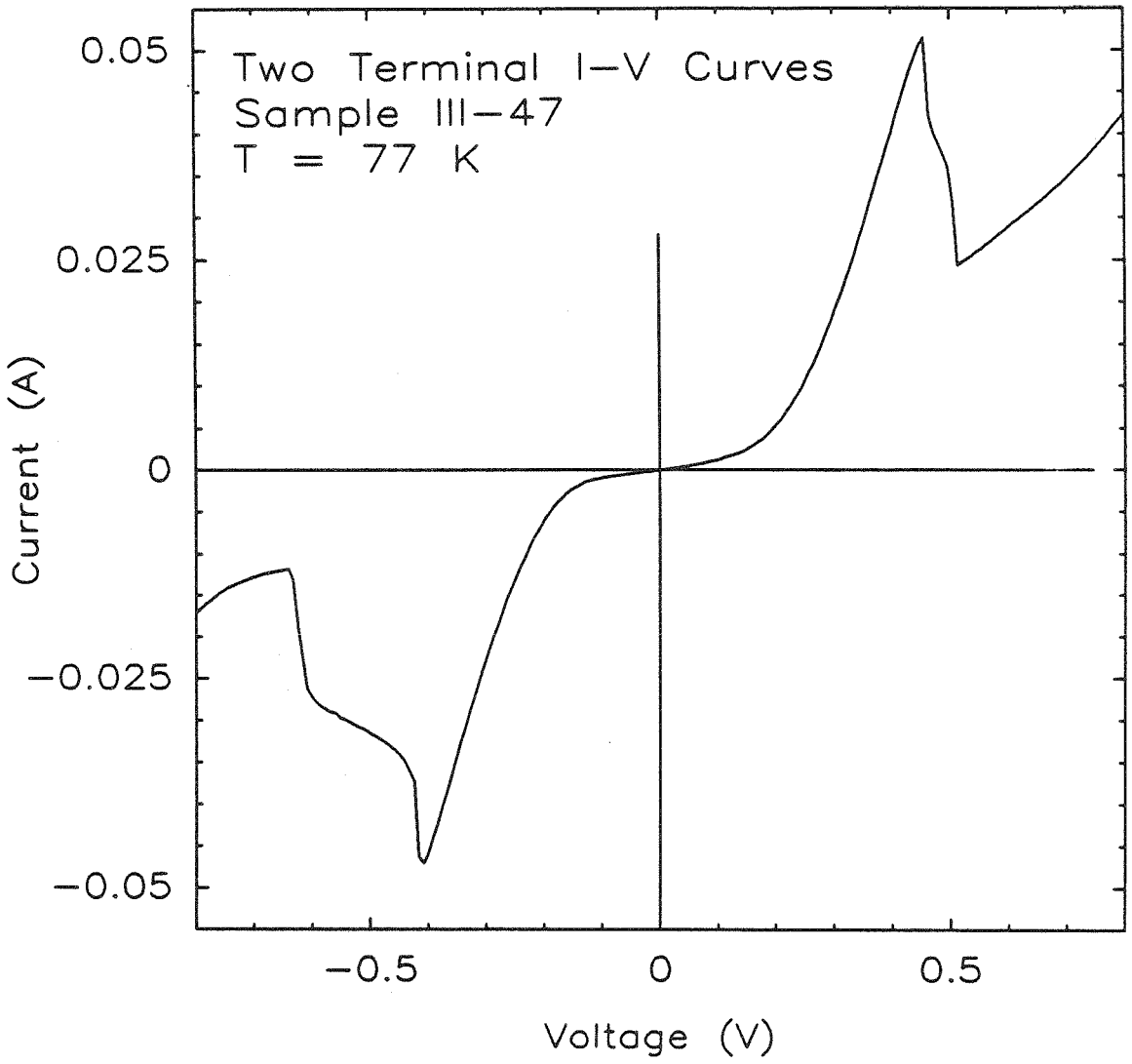

Figure 2.4: *I–V* curves for sample III-47, at 77 K. Doping asymmetries were reduced in this sample. Al percentage was increased as compared to III-33. NDR is more symmetric than in III-33 and has a maximum P/V current ratio of about 4.5 in reverse bias.

doping in layers 2 and 6. This came about because the Si oven used to dope the layers did not reach the proper temperature between layers 1 and 2. Thus layer 2 was probably doped in the 10^{17} range. This asymmetry was reflected in the results, in that superior NDR was exhibited in forward bias, which corresponds to injection into the lower-doped top layer. The effect was more dramatically exhibited in several samples, which exhibited NDR in forward bias (samples III-34, 38, 39, and 42). This effect was also observed in MOCVD-grown samples[‡] and suggests that it is more important to have low doping on the side of the structure into which carriers are injected, rather than on the side from which they are injected.

Two major refinements were introduced in sample III-47. The doping asymmetry between layers 2 and 6 was eliminated by ramping the Si to a lower temperature prior to growth of layer 2 and then increasing to the temperature required to obtained the desired doping.[§] Additionally, the Al percentage in the barriers was increased to about $x \sim 0.45$. These factors were expected to enhance resonant tunneling effects, especially at room temperature.

Another sample (III-46) was grown with the use of 25 Å undoped layers outside the double barriers These spacers were the only major difference between this sample and sample III-47. This sample exhibited superior low temperature and room-temperature NDR behavior, with peak-to-valley ratios of about 9.5 at low temperature, and 2 at room temperature. These 25 Å spacer layers were employed to decrease impurity effects in the tunneling current.[25]

Growth interruptions were employed in some samples. These interruptions have been claimed to improve interface quality and uniformity.[26] The use of 60 second interrupts at each heterojunction did not improve our results. In fact, samples in which growth interruption was utilized showed poor NDR characteristics. We sup-

[‡]See Chapter 3.

[§]Si was dropped from 1250°C to 1000°Cand then ramped to 1050°C.

pose that there is a tradeoff between smoothing introduced by growth interruption, and the arrival of undesirable impurities at the interface. The temperature of the substrate is undoubtedly an important factor in determining the degree to which growth interruption is beneficial. The overall cleanliness of the reactor would also be important.

The optimum substrate temperature for production of DBDs has not been determined. All of our samples have so far been produced at a substrate temperature of about 600 °C. So long as good morphology can be maintained, lower temperatures are to be preferred because they permit decreased dopant migration and more abrupt interfaces.[26,27]

This section has presented the initial results from an ongoing project. D. H. Chow and B. Cole, who share responsibility for this work,¶ are currently pursuing novel structures and new materials using the MBE growth technique. The results presented here demonstrate the current state of our MBE growth capability, which is rapidly evolving.

2.4 MOCVD Growth

Metalorganic chemical vapor deposition (MOCVD) is an epitaxial growth technique that differs considerably from MBE. However, both methods are capable of producing high-quality heterostructures. MOCVD is a chemical process in which gaseous carrier molecules are used to transport appropriate elements to a heated substrate. Most of the fundamental work was done by Manasevit.[28] In a hot zone near the substrate, the carriers break down, and the desired elements incorporate into the growing film. The literature of MOCVD is as voluminous as that associated with MBE. A good review may be found in Ref. 29.

¶They are not responsible for this description of the work.

2.4.1 Comparison to MBE

As mentioned, MOCVD is quite different from MBE. The first difference is the atmosphere surrounding the substrate. In MBE it is an ultra-high vacuum, on the order of 10^{-9} Torr or less. In MOCVD the pressures are very much higher, typically about 1 atmosphere. The partial pressures of the growing specie are much greater than in MBE, and the growth rate is commensurately higher. Typical growth rates for MBE are about 160 Å/minute (1 μm/hour), whereas they are about 2000 Å/minute (12 μm/hour) in MOCVD. For the double barrier the deposition of each component of the structure requires 10-30 seconds. In MOCVD this time decreases to 1-3 seconds.

In MBE the growth constituents are brought directly to the surface by molecular beam. In MOCVD chemistry must occur to break down the carrier gases.[31] The MOCVD ambient therefore contains a large number of hydrocarbons as well as hydrogen. The fluid mechanics of the gas flow in the reactor can affect the growth. In MBE it plays no role. The purity of the gas feedstock is a critical issue and is somewhat more difficult to control than the purity of the source material in MBE. The ability to produce uniform, abrupt interfaces with this technique depends to a large degree on a high flow rate through the reactor, which enables rapid turnover of the gases within it.[32] Further, the MOCVD process is capable of producing, in the same reactor, all of the III-V materials[29,30]; not currently possible with MBE.

Since the molecules used in the growth must be easily broken down, they are usually unstable and tend to be toxic. For example, the source materials for (Al,Ga)As growth are trimethyl gallium (TMGa), trimethyl aluminum (TMAl), and arsine. These materials are pyrophoric in the case of TMGa and TMAl, and highly toxic in the case of arsine. These materials are handled in large amounts at high flow rates. Safety is therefore a very significant issue with MOCVD. A

lot of current research is focused on finding satisfactory materials with lessened hazard potential. On the positive side, MOCVD has a much higher throughput potential than MBE, is lower cost, and has been argued to produce as good or better material than MBE.[29,32]

A cross-breed between MOCVD and MBE is currently being extensively studied. This type of epitaxial growth utilizes an MBE system with gaseous sources. The modifications range from use of arsine for the group V source, to the use of all the metalorganic sources (with or without arsine as the group V source). The pressure of the system is intermediate between the UHV environment of MBE and the atmospheric pressure of the CVD system, typically in the 10^{-5} Torr range.[29] This work is motivated by the desire to obtain the quality and control of MBE in a production-scale system.

An MOCVD reactor at Xerox Research Labs produced the samples described in this thesis. It is an RF heated, vertically-oriented reactor whose primary purpose is to produce heterostructure laser material. A schematic of such a reactor is presented in Fig. 2.5.[33]

2.5 Three-Terminal Devices: An Overview

2.5.1 Motivation

The tunnel diode was an interesting semiconductor device discovered in the late 1950s by Esaki.[34] A great deal of research was done on this device, some of which is summarized in Ref. 35. It was the first high-frequency semiconductor oscillator. Following it came the Gunn diode and the IMPATT diode. These devices were easier to produce and were capable of higher powers at equal or greater frequencies. The result was that the tunnel diode fell from favor and is now rarely used. Two problems resulted in the demise of the tunnel diode. First, the device

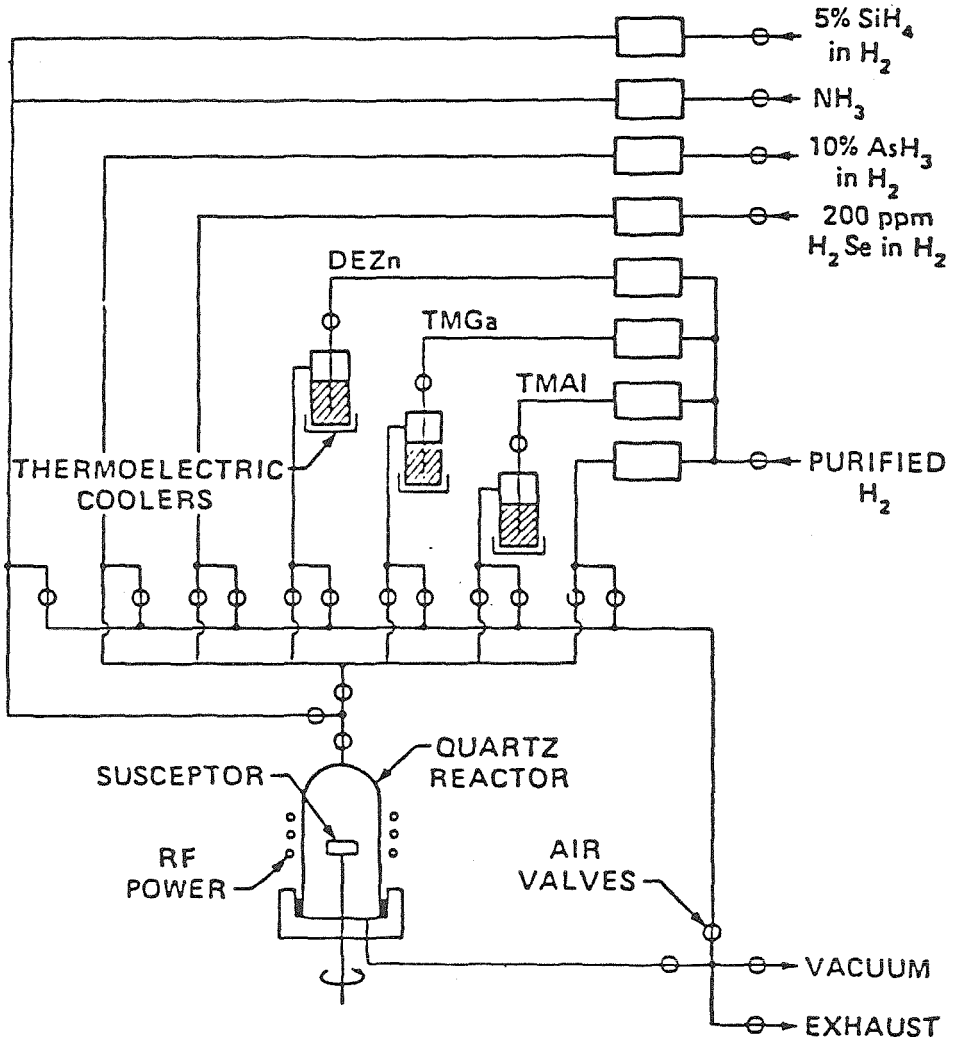

Figure 2.5: Schematic of MOCVD reactor, from R. D. Burnham.

was difficult to integrate with other structures because of the hyperabupt p^+ n^+ junction required. Further, it was difficult to produce and package and was difficult to use for logic applications because of the two-terminal nature of the device.

These two problems may be surmountable with the double barrier. The device is operational at 200 GHz, with predicted frequencies exceeding 600 GHz. The main problem with the DBD oscillator is not speed, but power. The output power at 200 GHz, for a single oscillator, was 0.2 μ W.[11] For comparison, an IMPATT diode is capable of generating milliwatts at 300 GHz.[36] There are two ways to solve this problem. One way is to push the operating frequency to a range in which no other device can compete. Another method is to pursue power-combining techniques and new designs aimed at increasing the output power. Both areas need attention.

The integration problem is addressed with the realization of a new class of device, the resonant tunneling transistor (RTT). This term is used to refer to any three-terminal device incorporating the resonant tunneling features of the double barrier.

2.5.2 Working Devices

DB/VFET and DB/MESFET : Types of RTFETs

The resonant tunneling field-effect transistor (RTFET) is the type of RTT with which this thesis is concerned. It is a combination of a double barrier with a field-effect transistor (FET). This combination has the desirable properties of the field-effect transistor with the added features of the double barrier. It should be realized by placing a double barrier in the source or drain of the FET structure, since these are the high-current terminals of the device. Two particular examples are the DB/MESFET and the DB/VFET.

There are many reasons for being interested in such a device. The FET struc-

ture is well matched to the double barrier insofar as growth is concerned. The FET is a unipolar device, as is the DBD. It is currently being realized in GaAs, which is the material in which the double barrier is most highly developed. The FET is capable of high-speed operation, as evidenced by the proliferation of microwave MESFETs. It can be used for logic applications, which was one of the major hoped-for applications of NDR devices such as the tunnel diode. Tunable oscillators, amplifiers, and signal-processing elements might also be envisioned. Additionally, a whole range of integrations are accessible. Planar MESFETs, vertical FETs, as well as modulation-doped field-effect transistors (MODFETs) and permeable base transistors (PBT) could be integrated with the DBD. The MODFET integration is particularly attractive for very high speed applications. Learning to successfully make one of these integrations should aid in realizing the remaining types.

RHET

The resonant tunneling hot-electron transistor (RHET) was the first RTT. It is a hot electron transistor with a double-barrier injector. It is described in Ref. 37. The most attractive feature of this device is the potentially high-speed nature of the hot electron transistor. This device is conceivably capable of speeds approaching that of the DBD. All three terminals of this device exhibit NDR. The most severe problem is associated with the hot electron transistor, which has a history of problems.[38] To overcome these problems, effort in new materials systems, such as GaSb, and Indium-based compounds, such as $In_xGa_{1-x}As$, is needed.[39,40] Recently, successful $In_xGa_{1-x}As$/(Ga,Al)InAs-based RHETs have been reported, with 77 K current gains of 25.[41]

RBT

The resonant tunneling bipolar transistor (RBT) has been realized by two groups.[42,43] The RBT has the advantages of the bipolar, with the added twist of resonant tunneling. Comparing this device to the RTFET is like comparing the bipolar transistor to the field-effect transistor. The devices are different, and each has its uses. For high-current applications, the RBT might be preferable to the RTFET. However, the RBT is a bipolar device, and therefore does not combine very well with the double barrier, which is naturally a unipolar structure. The most successful RBTs place the double barrier in the base of an *n-p-n* transistor, requiring that large numbers of acceptors be near the double barrier. This placement could be detrimental for the operation of the double barrier, due to increased impurity scattering. Finally, all three terminals exhibit evidence of the negative resistance.

RT Gate FET

There has been a report of a device integrating a double barrier into the gate of an FET.[44] This structure resulted in a device in which all terminals drew similar amounts of current. All terminals also exhibited NDR.

2.5.3 Quantum-Well RTTs

To date, the only realized RTTs are combinations of double barriers with more conventional structures. Several more sophisticated devices, in which the double barrier is not combined with a familiar structure, have been proposed. None have been made. Nevertheless, it is instructive to consider how a third terminal could be added to a fundamental double-barrier heterostructure. The only place to put such a terminal is in the quantum well. This feature is common to all the new devices, and presents a fabrication problem. This problem is not insurmountable.

We have devised methods whereby the quantum well can be contacted via the use of selective etches and contact annealing.

A representative new structure is illustrated in Fig. 2.6. The operational principle of the device has been explained elsewhere.[45] Carriers are removed from a quantum well, and the base of the transistor is placed at the back of the structure, accounting for the device's name: the inverted base–collector tunnel transistor. Field from the base contact depletes the thick $Al_xGa_{1-x}As$ barrier and places electric field in the quantum well. This field modulates the positions of the levels via band bending and the Stark effect.

The most serious problem with this device relates to the quantum-well contact. The resistance of the central-well contact can be very large. This tends to slow the device down, because capacitive delays become significant. The resistance is large because the quantum well forms a 50 Å wire through which carriers must flow. The resistance of this wire can easily be the dominant resistance of the device. Materials with very high mobilities would probably be needed in order to realize this type of structure.

We have attempted to realize the inverted base–collector tunnel transistor, using a few samples produced by MOCVD. Major difficulties were encountered in 2 areas. First, the resistance of the base $Al_xGa_{1-x}As$ layer was not sufficiently high. This problem was not expected and prevented many diagnostic measurements. The other major problem related to the resistance of the quantum-well contact, particularly when surface depletion at the GaAs was considered. Attempts to passivate the GaAs surface were made without success.[46] This made it very difficult to observe any transport between the mesa contact and the collector contact. We believe that successful contact to the quantum-well region was made. This was done with the growth of a thin marker layer of AlAs above the device structure. A selective etch of 250:1 H_2O_2 : NH_4OH (pH $\sim$ 7.5) was sufficiently selective to

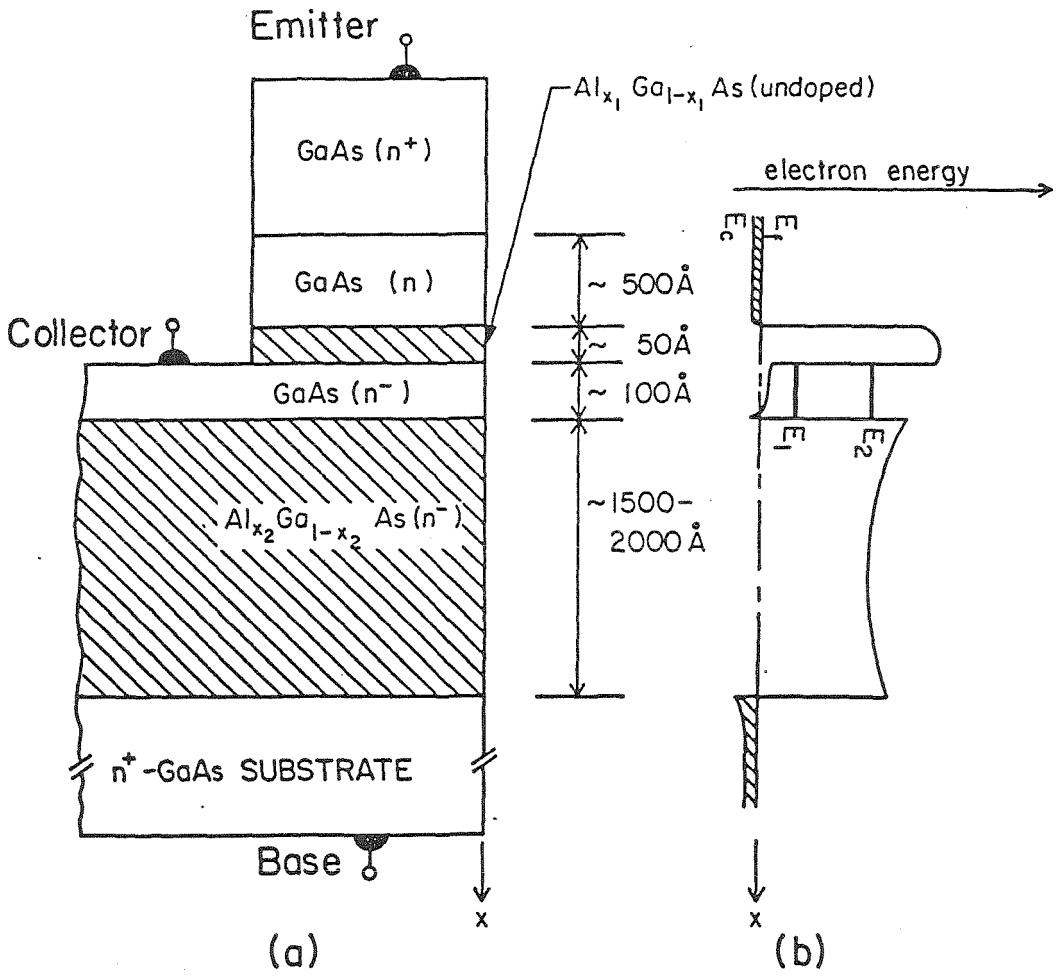

Figure 2.6: The inverted base–collector tunnel transistor, from Ref. 48.

stop at the AlAs marker layer. Au:Ge evaporation and annealing (as described in Chapter 3) contacts the quantum region. We did not observe short circuits between this contact and the backside layer, which leads us to conclude that this may be a satisfactory method for contacting thin layers.

2.6 Conclusions

This chapter has reviewed a number of topics. The major points are summarized below:

1. The theoretical literature of resonant tunneling has been reviewed.
   (a) An expression for the current was presented.
   (b) A transfer matrix technique for obtaining the elastic transmission coefficient was outlined.
   (c) Major theoretical issues were discussed.
2. An experimental project to produce DBDs by MBE was described.
3. An overview of the MOCVD process was presented.
4. Several RTTs were discussed, including efforts to fabricate the inverted base-collector tunnel transistor.

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Chapter 3

DB/VFET Devices

There are a variety of reasons for pursuing the study of three-terminal NDR devices. These were presented in Chapter 1. This chapter is concerned with the growth, fabrication, and testing of a double barrier combined with a vertical field-effect transistor (DB/VFET).

3.1 Results Summary

This section summarizes the main points of the chapter. Functioning resonant tunneling transistors were made. The device is referred to as a DB/VFET. Results for two DB/VFETs form the core of the chapter. The devices showed NDR in the source-drain characteristic of the FET, which was controllable with gate bias. The FET section of the device functioned at room temperature. The double-barrier component of the device did not function as well at room temperature as it did at 77 K. One sample exhibited NDR at room temperature, with a peak-to-valley current ratio not exceeding 1.15. Other samples exhibited NDR at 77 K. Transistor operation was observed in forward and reverse bias, and in common-drain as well as common-source bias configurations. NDR was observed at high-bias levels, which was attributed to interaction between the the double barrier and the FET parts

of the device.

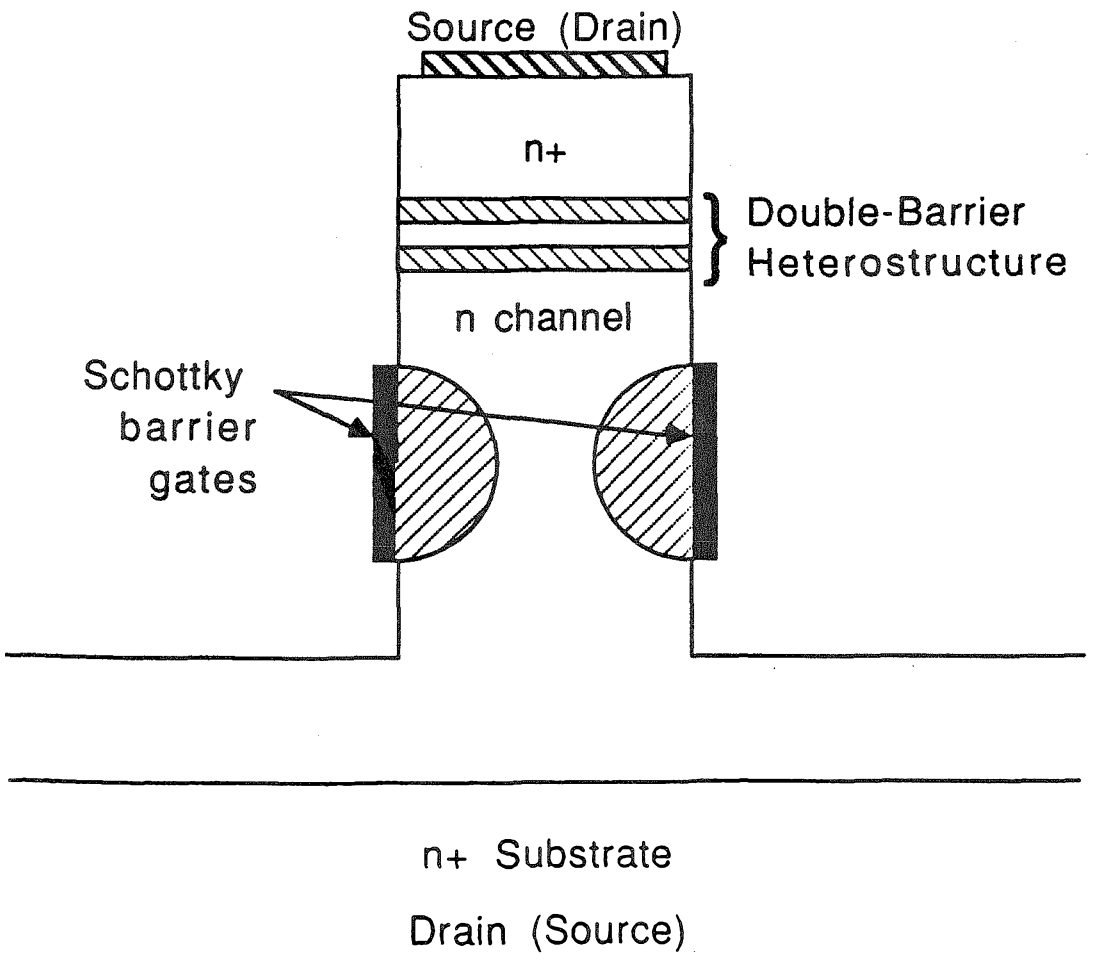
3.2 Outline of Chapter

The theme of this chapter is the DB/VFET device. The device concept, growth, and fabrication are described in Sections 3.3 through 3.6. The experimental set-up is described in Section 3.7. Basic results for two working DB/VFET devices are presented in Section 3.8. These results are then discussed, and logical follow-up measurements are presented in Section 3.9. Results for additional working DB/VFET devices are presented in Section 3.10. At the end of the chapter are several tables, which summarize results for the full complement of samples grown for this project.

3.3 Device Concept

The DB/VFET concept is a basic one. By changing the resistance of one of the electrode regions of the double barrier, the voltage at which negative differential resistance (NDR) is seen changes. The basic idea was described elsewhere.[1] In its purest form, the VFET is formed by Schottky barriers placed along the vertical sides of a mesa structure. The basic idea is illustrated in Fig. 3.1.

Very sophisticated processing techniques are necessary to realize a structure of the type shown in Fig. 3.1. The major difficulties are associated with the definition of the mesa, the sidewall deposition of the Schottky barriers, and attendant contacting issues. At Westinghouse such a device has been made, and had a maximum predicted frequency of about 60 GHz.[2] Fabrication of the structure required reactive ion etching of 0.3 μm mesas, carefully controlled gate evaporation, as well as air-bridge contact techniques. The final step was the removal of the substrate. The prohibitive expense and fragility of the resultant device make it unlikely that such



Fabrication difficulties

1. Vertical sidewall deposition difficult.
2. Mesa width must be comparable to depletion length.
3. Contact to mesa is difficult.

Figure 3.1: The basic DB/VFET concept. Some difficulties in realizing this concept are listed.

a structure would be useful in real circuits. The initial concept for the DB/VFET was similar to this device.

3.4 Actual Device Design

These techniques, while perhaps necessary for particular applications, may not be required in all cases. Generally, the right way to pursue new device concepts is to start with a simple design and refine it as needed to produce working structures. Performance considerations may then be applied to produce more sophisticated devices, like those mentioned above. Such was the philosophy with which the DB/VFET was pursued. A simplified design places the gates on a horizontal rather than a vertical surface. This concept is shown in Fig. 3.2.

While the horizontal placement of the gate electrode simplifies fabrication procedures, the question of whether the device can be made to work with horizontal electrodes remains to be answered. The operating concept is that lateral extension of the primarily vertical depletion region underneath the gate will provide transistor action. Whether this idea is reasonable or not is open to question at this point.

A basic idea can be had by considering the electrostatic problem of a capacitor with a hole in one plate, with free space between the plates. The two important length scales in this problem are the size of the hole and the separation of the plates ('X' and 'T' in Fig. 3.2). The ratio X/T defines a dimensionless scale for the problem. A small hole combined with a large plate separation ($X/T << 1$) should result in a field distribution approaching that of the uniform case, corresponding to large lateral field extension. Conversely, a large hole and a small plate separation ($X/T >> 1$) should look like two separate capacitors, with little lateral extension. Clearly, we want X/T to be small.

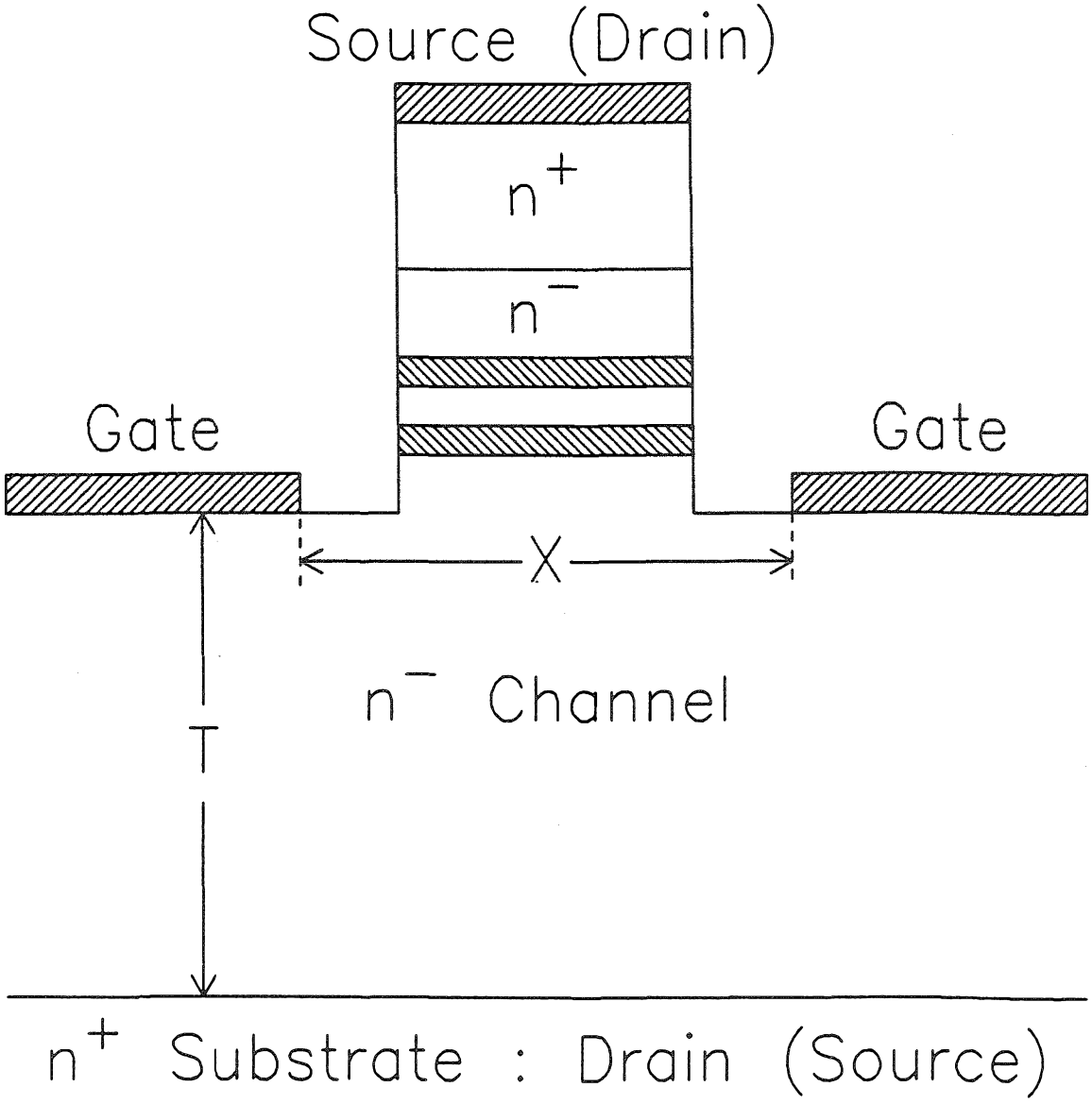


Figure 3.2: Actual DB/VFET cross-sectional diagram. Most devices were fabricated with $X = 7\,\mu$m, and a mesa width of $5\,\mu$m. Variable cross-section masks were made, with 'X' values of $7\,\mu$m, $12\,\mu$m, and $22\,\mu$m. Channel thickness 'T' ranged between 2 and $3\,\mu$m for working devices.

A more realistic problem would introduce charge between the plates and require the solution of Poisson's equation in at least 2 dimensions.* For a semiconductor device, $X/T \sim 1$, and asymptotic relations are not useful. A full solution to the problem would be an interesting theoretical project, which was not undertaken for this thesis.

A more experimental approach to this issue is to consider two length scales. The first is the depletion length of a Schottky barrier. In the abrupt approximation, the formula for this length is given by[3]

$$W = \left(\frac{2\epsilon}{qN_d} (V_{bi} - V - \frac{kT}{q}) \right)^{1/2}, \tag{3.1}$$

where W is the depletion length, ϵ is the dielectric constant of the material, N_d is the impurity concentration, q is the electron charge, k is the Boltzmann constant, V_{bi} is the barrier height of the Schottky barrier, and V is the applied bias. Breakdown via avalanche multiplication usually results at field strengths in excess of 5×10^5 V/cm. Fig. 3.3 shows plots of the maximum depletion width versus doping concentration, as well as the breakdown field strength, from Ref. 3. Maximum depletion lengths of 3 to 6 μm are possible for doping levels in the $5 \times 10^{15}\,\mathrm{cm}^{-3}$ to $1 \times 10^{16}\,\mathrm{cm}^{-3}$ range. These doping levels may be achieved with MOCVD methods.

The other important length scale deals with fabrication. For contact mask alignment and wet etching, 1 μm is about the limit for convenient alignment. Mesa widths of several microns are feasible with wet etching, with smaller mesas made more difficult by undercutting and resist stability. One may therefore conclude that DB/VFET devices with horizontal gates might work.

*3 dimensions might be preferable, allowing circular holes and slots in the top electrode to be differentiated.

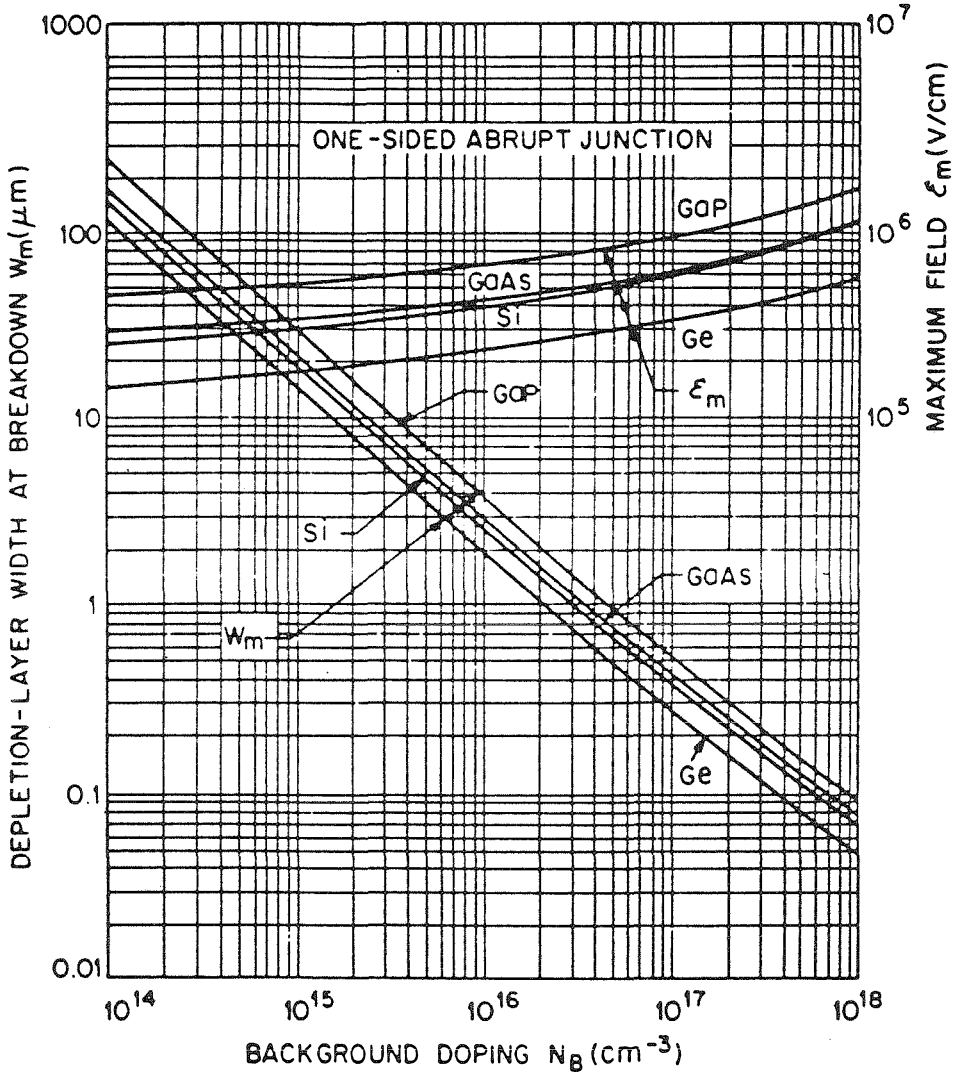


Figure 3.3: Plots of the maximum depletion length at breakdown in an abrupt *p-n* junction for various materials. Also indicated is the breakdown field strength. From Ref. 3.

3.5 Growth

All samples were produced by MOCVD at Xerox Research Labs in Palo Alto, California. Samples were grown on degenerately doped substrates. MOCVD growth technique is discussed in Chapter 2. A number of samples were produced in the effort to obtain working DB/VFET devices. Tables 3.2 and 3.3 contain relevant growth parameters for all the DB/VFET samples studied.

3.5.1 Double Barrier

The initial samples were used to find a successful recipe for production of double barriers with reasonable negative resistances. This recipe was used consistently for all the DB/VFET samples studied. Transmission electron microscopy (TEM) results, which were not obtained until well into the project, revealed that the typical dimensions of the double barrier were 80 to 110 Å for the barriers and 40 to 60 Å for the well. These values fluctuated, depending upon details of the growth conditions, and reflect the lower degree of thickness control possible with MOCVD as compared with MBE. Only a few samples were studied with TEM. Therefore, the table entries list growth parameters rather than actual thicknesses. On the top of the double barrier, 20 seconds of lightly-doped growth was deposited. These spacer layers are commonly used in double-barrier growth, to decrease impurity-assited excess currents, and are discussed in Chapter 2. This region was intended to be 500 Å thick and doped in the $10^{16}\,cm^{-3}$ range. The channel of the VFET lay beneath the double barrier, and was a thick, lightly-doped region.

Double barriers were produced with $Al_xGa_{1-x}As$ barriers. The Al percentage was intended to be 0.45. This choice was based on earlier studies of double barriers.[3] The Al percentage was determined by thick-layer calibration growth and therefore is subject to some uncertainty when applied to very thin layers.

Some samples did not exhibit NDR.

3.5.2 FET

The transistor portion of the device relies on a single lightly-doped layer. As mentioned, a thick region is desirable for maximization of the lateral depletion effects, and to avoid reach-through of the gate depletion to the degenerately doped substrate beneath. Some of the samples grown had thin channel layers. Achievement of low doping was difficult.

The n–type dopant used for these growths was selenium, which exhibits a "memory" effect.[5] This effect means that once a layer is grown with Se doping, subsequent layers will contain some Se. Prior to growth of the structure of interest, a buffer layer of heavily doped material is usually grown, to provide a good surface for epitaxial growth of the structure. "Memory effects" were found to be incompatible with successful production of DB/VFET layers. However, growth without a buffer layer was found to be acceptable. This project demonstrates that successful double-barrier growth can be obtained without a buffer layer, provided that a thick initial layer is grown. The doping in the channel layer will thus be the background doping level of the reactor. An ultimate background level of about $2 \times 10^{15}\,\mathrm{cm}^{-3}$ was achieved at a growth temperature of $775\,^{\circ}\mathrm{C}$.

3.6 Fabrication

This section covers the mask design, layout, and fabrication procedures developed for the DB/VFET. Layouts involving circular mesa structures with surrounding ring-gate contacts were rejected because the small mesas would have been very difficult to contact.

3.6.1 Layout

The selected layout begins with long, narrow mesas. Isolation of these mesas must be the function of one mask. Since any pattern on this mask would be replicated in a mesa structure, the only function of this mask must be to isolate the double barriers. Subsequent masks must be used to define gate and mesa contacts. Thus, the minimum number of masks possible for the DB/VFET fabrication procedure is two. There remains the problem of contacting these long, thin mesa structures. Wire bonding directly to the mesas is not possible. Surface passivation techniques or ion implantation could be used, but at the expense of complicating fabrication. By overlapping a gold pad with the edge of the mesa, a functional contact to the mesa can be made without resort to these techniques.

A three-dimensional schematic of the finished structure is shown in Fig. 3.4. Following isolation of three $75 \times 5\,\mu$m mesa structures (the elevated boxes in Fig. 3.4), a second mask was used to define planar Schottky barrier contacts offset $1\,\mu$m from the base of the mesa. This mask also forms a pattern allowing the deposition of a separate Au patch that overlaps the last $5\,\mu$m of the mesa fingers. Wire bonding to the Au patch also contacts the mesas that contain the double barrier. This bond forms a parallel connection of the three mesa fingers with a Schottky diode formed by the bonding pad. The high resistance of the diode, prior to forward-bias turn-on, means that significant current flows only through the tunnel structure.

Mask fabrication procedure is outlined below:

1. Determine pattern

2. Cut pattern from Rubylith acetate

3. First reduction (15-30 times reduction)

4. Second reduction utilizing step and repeat camera (4 or 10 times reduction)

VFET FABRICATION

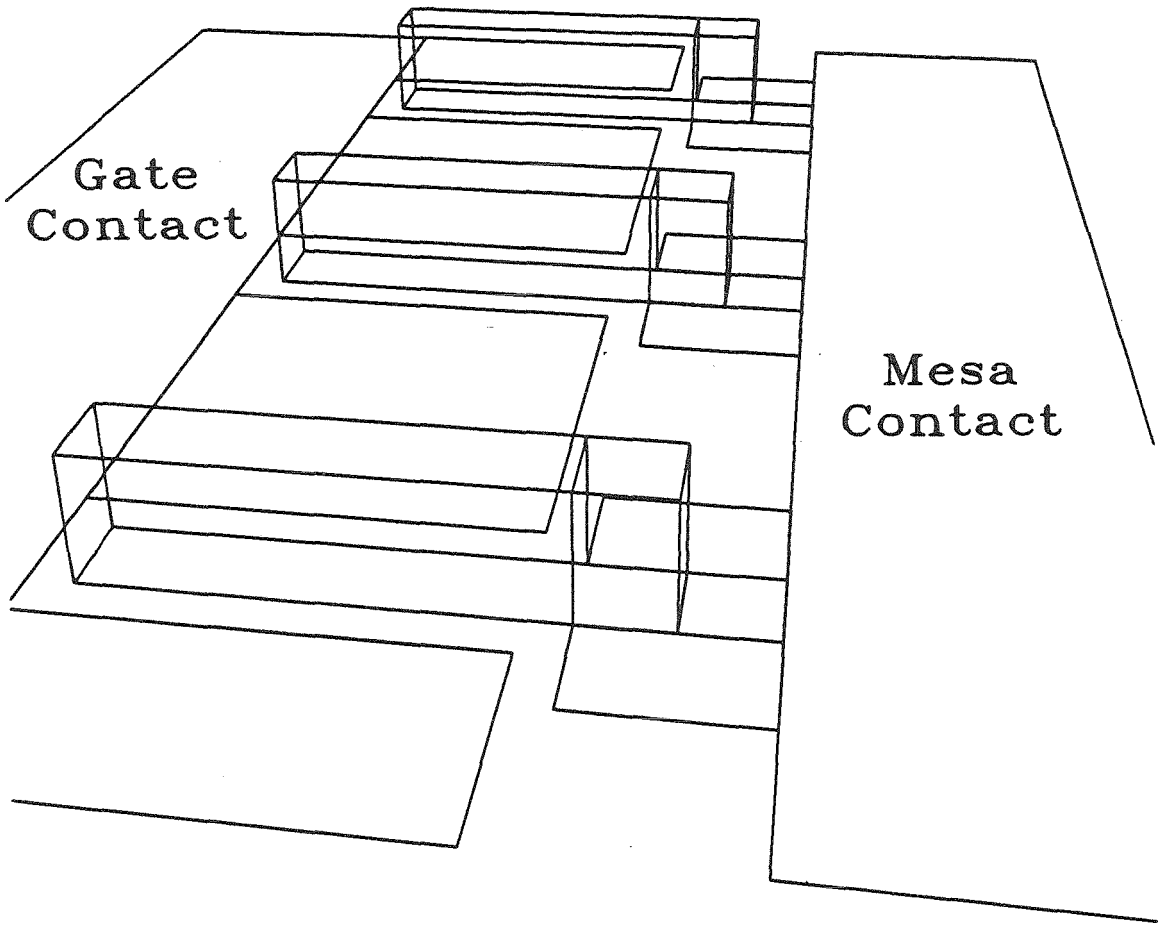


Figure 3.4: A three-dimensional view of the DB/VFET design. The boxed areas represent mesa structures, with gate contacts lying around them. The mesa contact pad overlaps the mesa fingers, forming the mesa contact.

5. Make iron oxide copy of original master blank

The two-mask set for fabrication of the DB/VFET consisted of an etch mask and a second lift-off mask, for two reasons. First, experimental results demonstrated that photoresist plus metal was a more effective etch mask than photoresist alone. The second reason has to do with the mask fabrication procedure. The net result of the photoreduction process is an increase in the size of clear areas and a decrease in the size of dark areas. If two lift-off masks are made, the relative sizes of the two masks can change by more than 1 micron during the process. Features on one mask that are supposed to be larger than matching features on the other will now be smaller, making alignment impossible. A pair of masks in which one is an etch mask and the other is a lift-off mask will undergo complementary fabrication distortion, retaining their alignment tolerances.

3.6.2 Procedure

The sample preparation procedure will now be described in detail. Initially, a small piece of the sample was cleaved from the main wafer. This piece, usually about 3 mm square, was rinsed in acetone and ethanol, and then cleaned in a 1:1 solution of HCl and water for one minute. This acid does not etch the GaAs appreciably, but removes any native oxide and organic solvent residue from the surface. The sample was then loaded into an evaporator, where 1000 to 4000 Å of Au-Ge alloy (88:12) was evaporated onto the top surface of the material at a pressure of about 1×10^{-6} Torr. A standard photolithographic process was then used to transfer the first mask's pattern to the photoresist-coated sample. Appendix A contains details of the procedure. Following this procedure, a gold etch[†] was used to remove the Au-Ge from the surface of the sample, except in areas protected

[†]Transene Co. Au etchant type TFA.

by the photoresist pattern. The sample was then etched in a liquid solution. The duration of the etch depended upon the desired etch depth, usually 0.4–0.6 μm. The solution used was a mixture of water, phosphoric acid, and hydrogen peroxide in a volume ratio 100:3:1. This mixture etches GaAs at a rate of about 400 Å per minute and is not selective for $Al_xGa_{1-x}As$. Slower or faster etch rates can be obtained by changing the water concentration. Etch rate data for a 50:3:1 mixture are presented in Chapter 4. Other etches are possible, but are usually too fast for this application.[6]

Upon conclusion of the first etch, photoresist was removed with acetone, and more Au-Ge was evaporated onto the back side of the sample under conditions similar to the first evaporation. Following the evaporation, the device was annealed in a reducing ambient (helium gas mixed with 12 percent hydrogen) at 400 °C for 30 seconds to form low-resistance contacts.[7]

A second mask was used to define another pattern on the material. This pattern had to be aligned to the mesas left behind from the first mask process. The tolerance for the alignment was 1 μm and could be done reproducibly, using a Karl Suss MJB-3 mask aligner. This time, a lift-off procedure was used (see Appendix A). Once this pattern was defined, Au was evaporated onto the sample, under similar conditions to the Au-Ge evaporations. Then the sample was ultrasonically agitated in an acetone bath to remove the resist and the Au on top of it. This Au "lift-off" gives the procedure its name.

Finally, the samples were photographed and mounted. Photographs were taken, to identify specific devices being tested. Samples were mounted on T0-8 transistor headers using silver paint. Electrical probes were used to measure room-temperature characteristics prior to wire-bonding specific devices for further testing using a West-Bond ultrasonic bonder.

3.6.3 Refinements

In addition to the particular mask discussed above, another type of layout was made. This mask set allowed the use of a variety of mesa widths. One expects transistor action to decrease as mesa width increases, because the lateral depletion becomes less significant. Therefore, a mask set allowing fabrication of variable size mesas is valuable. This layout incorporated a variety of mesa widths including $3\,\mu$m, $5\,\mu$m, $10\,\mu$m, and $20\,\mu$m. The fabrication procedure for this mask was the same as that outlined above.

There are several refinements to the fabrication process that can be imagined for this structure. Some of these are not practical, and others increase the complexity of the process. The first thing to be considered is a self-aligned structure, which would enable the edge of the gate to be somewhat closer to the edge of the mesa. The difficulty with this fabrication idea is that it offers no convenient way to make contact to the mesa structure. The difficulty arises because a self-aligned procedure necessarily uses the same mask for two purposes. The Au Schottky-barrier gate would therefore completely surround the mesa, and another mask would have to be used to remove the material from undesired areas, and still another to deposit the Au bonding pads. Additionally, a refractory metal would be needed for the gates.

Another possible refinement is to utilize a passivating layer, such as SiO_2, beneath the mesa contact pad. This idea is is a good one, but requires additional masking steps and dielectric evaporation. Ion implantation could be used for the same purpose. This refinement would also require at least one more mask and an implant.

Yet another refinement to the structure would be to utilize a several micron trench etch, which would then be filled with Au, effectively forming a vertical sidewall contact. This idea requires a dry etching process to create the narrow,

deep trench. Having created this trench, it must be effectively filled with metal.

Finally, one might actually try to fabricate the sophisticated VFET structure presented in Fig. 3.1. Such a device would probably have enhanced performance. A procedure of this type is described in Ref. 2.

3.7 Experimental

Basic DC electrical tests were performed on the samples after they were prepared. AC oscillation issues are addressed in Chapter 5. Initial room-temperature measurements were made on gate electrodes, to determine the quality of the Schottky barrier. Of interest here was the reverse breakdown voltage, as well as the ideality factor and barrier height of the gate. Typical breakdown voltages varied from sample to sample, but exceeded $V = -20$ V for working DB/VFETs. Mesas were tested for room-temperature NDR, prior to wire bonding individual devices.

Specific devices were wire-bonded and tested at room temperature and 77 K. Liquid nitrogen immersion provided access to the lower temperature. Variable temperature studies were not performed. Previous studies by Bonnefoi[4,8] have indicated that little improvement in resonant tunneling behavior is seen at temperatures below 77 K. I–V data were taken, using a Tektronix 577 curve tracer or a Hewlett Packard model 4145A Semiconductor Parameter Analyzer. This instrument is a digital curve tracer, acquiring data in a point-by-point fashion. It can be programmed to act as a current source/voltage monitor or a voltage source/current monitor. This instrument was controlled by an HP9816 personal computer via a BASIC computer program written for the purpose. Data were subsequently transferred to a Digital Equipment Corporation VAX 11/785 or MicroVAX II mainframe computer.

Bias polarities are as follows. For a two-terminal device, forward bias refers to

positive bias on the mesa containing the double barrier. These mesas are said to lie at the front of the sample. Positive current would thus correspond to electron transport from the back of the sample to the front. Positive current is observed in forward bias. Conversely, reverse bias refers to negative voltage on the mesa structure, resulting in electron flow from front to back. In a two-terminal device there are two ways to create a given bias configuration. For example, one way to create forward bias is to ground the substrate and apply positive bias to the top electrode. Another way is to ground the mesa and apply negative voltage to the substrate. In a three-terminal device, these two configurations are no longer interchangeable. The two configurations just mentioned represent common-source and common-drain connections, which are different from one another in an FET.[9]

3.8 Basic Results

This section presents basic results of DC characterization measurements of two DB/VFET samples. These samples represent the best working structures obtained. Relevant information for these samples is contained in Table 3.1. Several other samples showed DB/VFET behavior, but lacked NDR. A number of samples exhibited no NDR, but worked as FETs, while several showed NDR without transistor action. A summary of the operating behavior of all samples is contained in tables at the end of this chapter.

3.8.1 Sample T245

This section presents results for sample T245, the first functioning DB/VFET obtained. Important parameters for this sample are contained in Table 3.1. In Fig. 3.5 we present experimental I–V curves for this sample in reverse bias. In these curves, negative bias is applied to the mesas containing the double barrier,

Quantity	Sample T245	Sample T335
$Al_xGa_{1-x}As$	$x \sim 0.35$	$x \sim 0.35$
DB dim. (Å)	90/50/90	90/50/90
Channel (μm)	2.8	3.3
n_{ch} (cm^-3)	$1.5 \times 10^{16}\,cm^{-3}$	$2 \times 10^{15}\,cm^{-3}$
NDR P/V ratio	5.2(f)/3.1(r)	5.3(f)/4.7(r)
J_{peak} (A/cm^2)	45	264

Table 3.1: Important parameters for T245 and T335. 'DB' refers to the dimensions of the double barrier, n_{ch} refers to the doping in the channel layer. 'P/V' denotes the peak-to-valley current ratio of the NDR, and J_{peak} refers to the current density at the peak of the NDR. The Al percentage is approximate only, as are the double-barrier dimensions.

and the substrate is grounded. Thus, this figure illustrates operation in common-drain mode, rather than the more conventional common-source mode.

The basic effect observed is a shift of the NDR to larger bias levels, coupled with a decrease in the peak-to-valley current ratio, as expected for an addition of series resistance. This resistance is provided by gate bias, which was incremented in -5 V steps to a maximum of $V_g = -20$ V. Significant gate current was not seen during the acquisition of the data illustrated in Fig. 3.5.

Forward-bias operation of a device fabricated from sample T245 is illustrated in Fig. 3.6. In these curves the substrate is grounded, and positive bias is applied to the mesa structure containing the double barrier. This configuration of biases represents common-source operation. NDR is observed at much lower bias levels than in reverse bias. The large asymmetry in NDR location between forward and

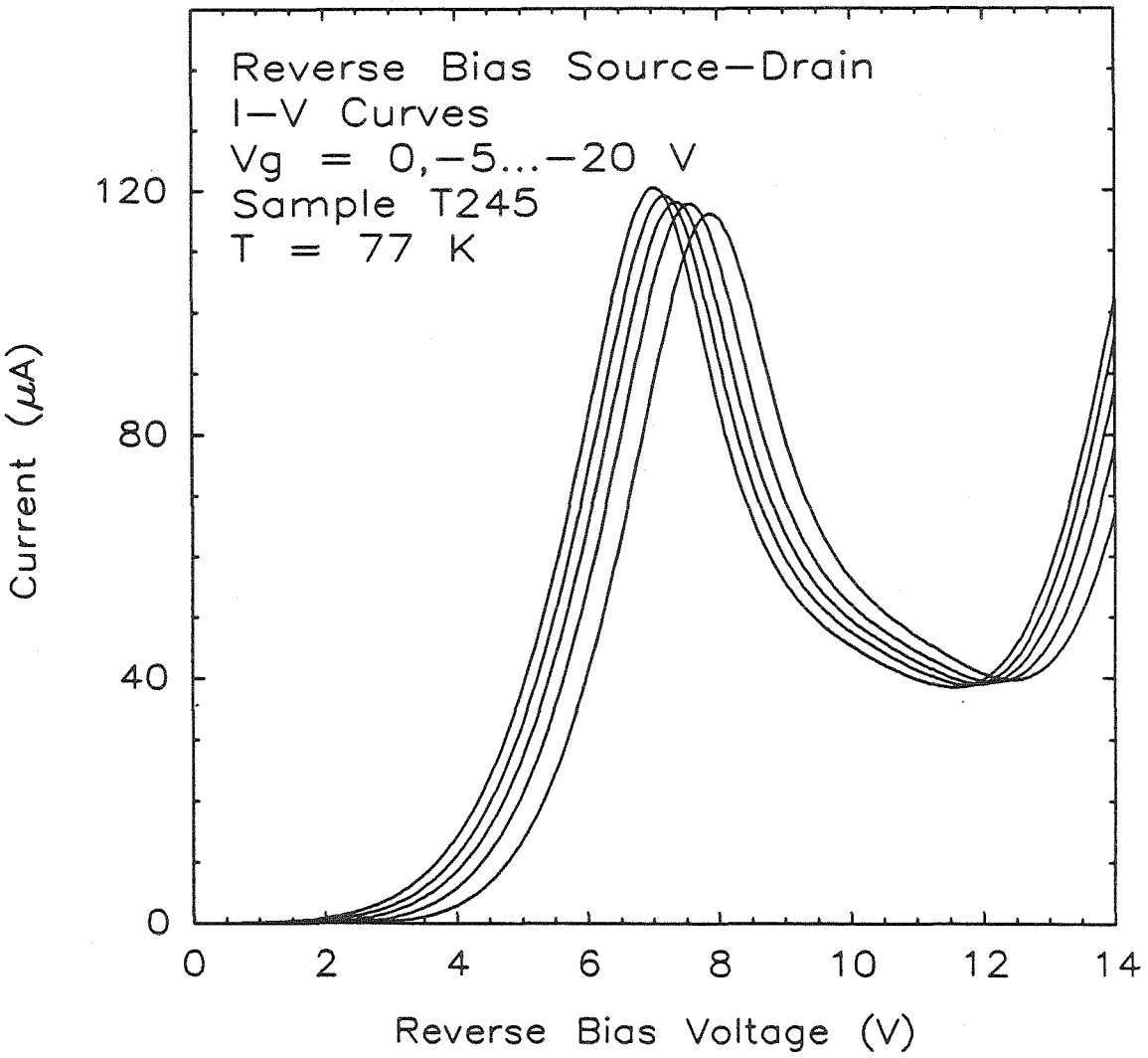


Figure 3.5: Common-drain reverse-bias I–V curves for sample T245 at 77 K, with gate voltage (V_g) as a parameter. The leftmost curve was taken with $V_g = 0$. The $V_g = 0$ peak-to-valley ratio is 3.12.

reverse bias can be explained by the extreme asymmetry of the structure. The large-scale conduction onset at the extreme right of Fig. 3.6 is due to the forward-bias turn-on of the Schottky barrier formed by the mesa bonding pad.

3.8.2 Sample T335

This section presents results for devices fabricated from sample T335. This sample exhibits DB/VFET behavior qualitatively superior to all other samples. Important sample parameters are summarized in Table 3.1. In Fig. 3.7 we present reverse-bias I–V curves for a device fabricated from sample T335, obtained at room temperature. In Fig. 3.8 77 K results for the same device are shown. For both figures the substrate was grounded, and negative voltage was applied to the mesa containing the double barrier. Thus, the mesa acts as the source of electrons, and the substrate forms the drain.

Room-temperature NDR was observed in this sample. It was the only sample studied that exhibited room-temperature NDR[‡]. It is interesting to note that room-temperature NDR was seen only in reverse bias. Additional data for sample T335 are presented in Fig. 3.9. Forward-bias operation is possible for this sample. Results are similar to those obtained for sample T245. These data are illustrated in Fig. 3.10.

3.9 Discussion and Further Study

3.9.1 Reverse-Bias Behavior

In reverse bias, both samples exhibit NDR at larger bias levels than ever previously reported. This is due to the presence of a thick, lightly-doped region on the

[‡]Some samples, notably T245, showed inflections in the I–V curve at room temperature.

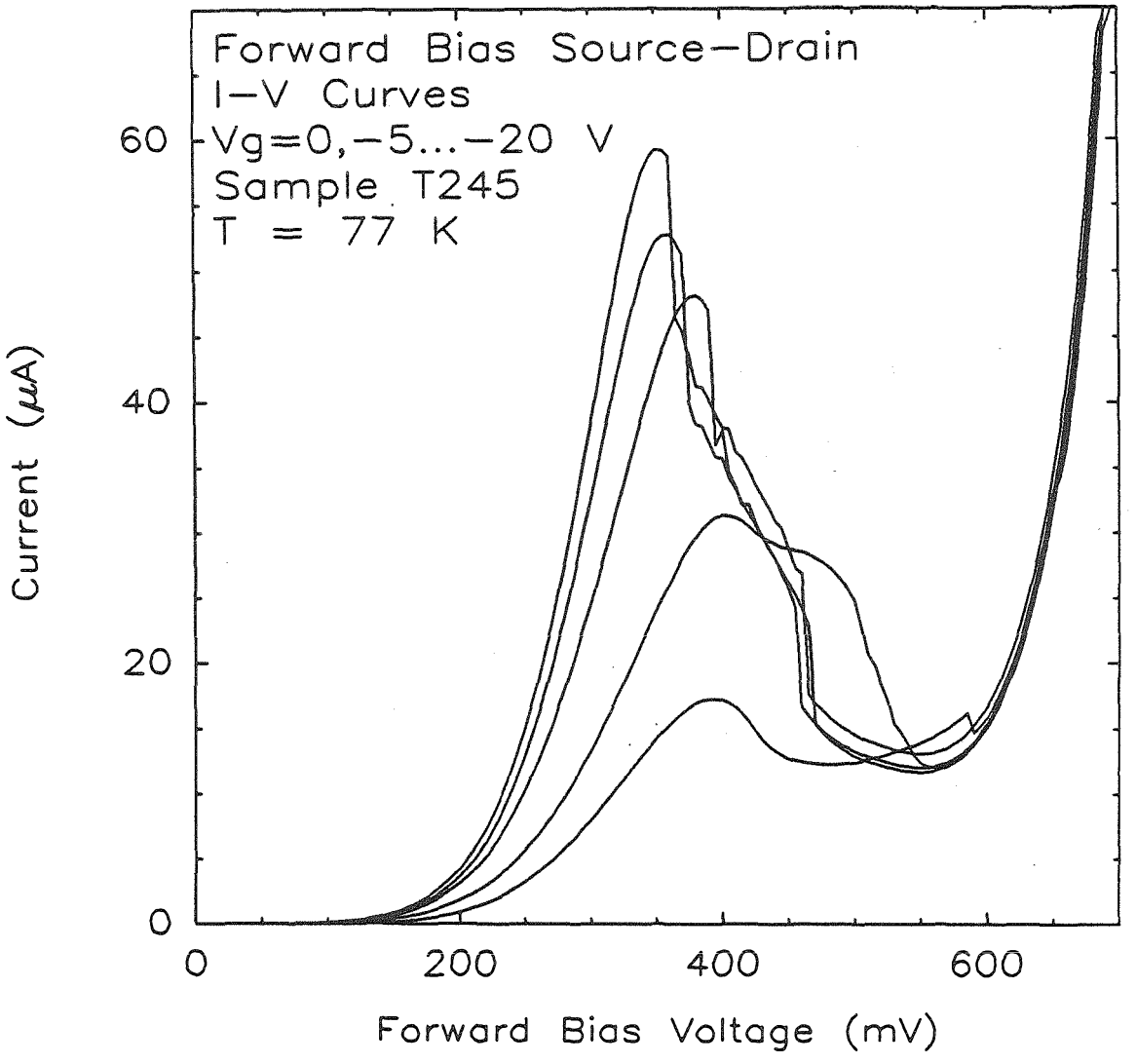


Figure 3.6: Forward-bias common-source data for sample T245, with V_g as a parameter. Peak-to-valley current ratio decreases with increasingly negative V_g. The $V_g = 0$ peak-to-valley current ratio is 5.24. The 'step' in the NDR regions are believed to be due to oscillation, see Chapter 5.

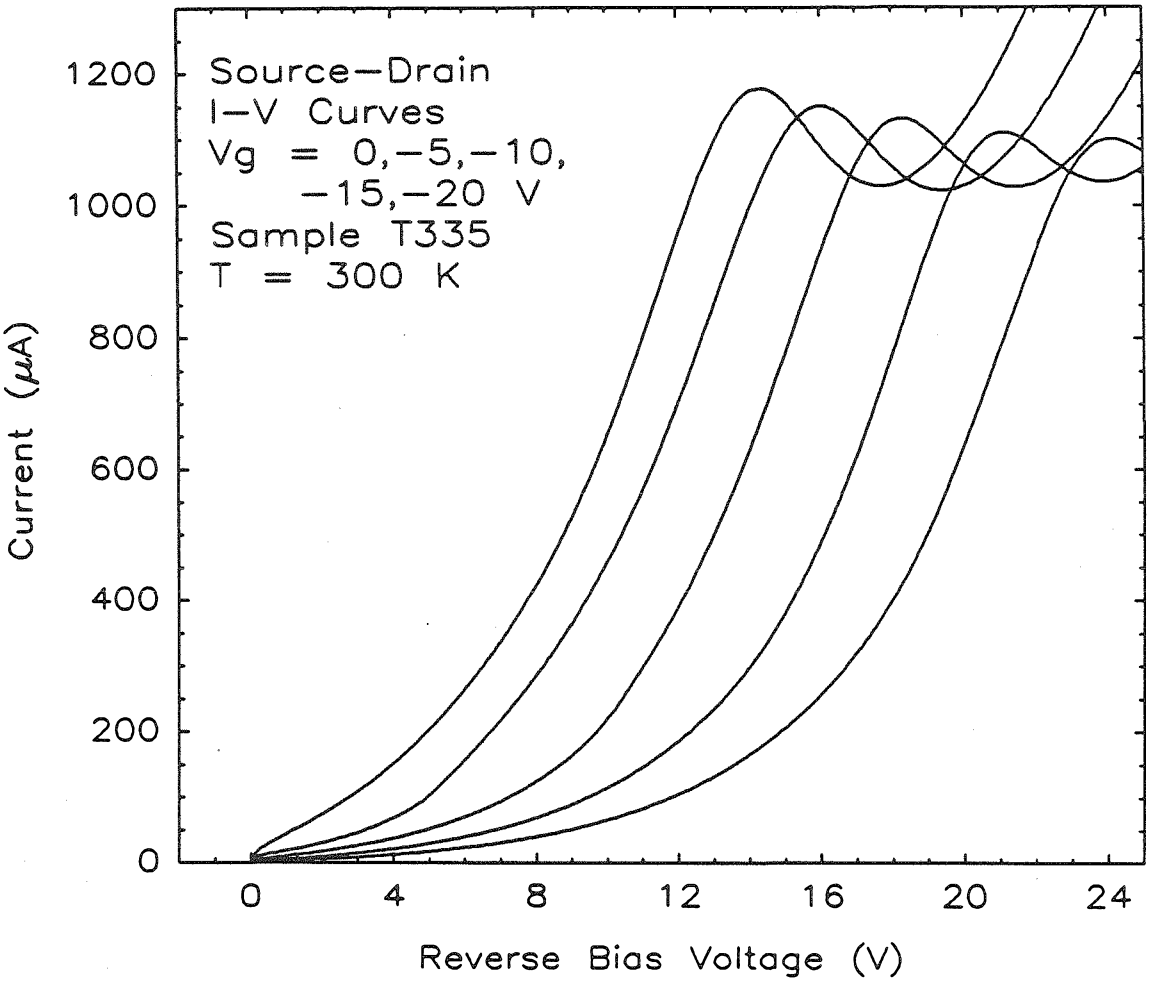


Figure 3.7: Reverse-bias common-drain I–V curves for sample T335 taken at 300 K, with V_g as a parameter. The leftmost curve was taken with $V_g = 0$. V_g is incremented in -5 V steps, to a maximum of $V_g = -20$ V. The same device is illustrated, at 77 K, in Fig. 3.8.

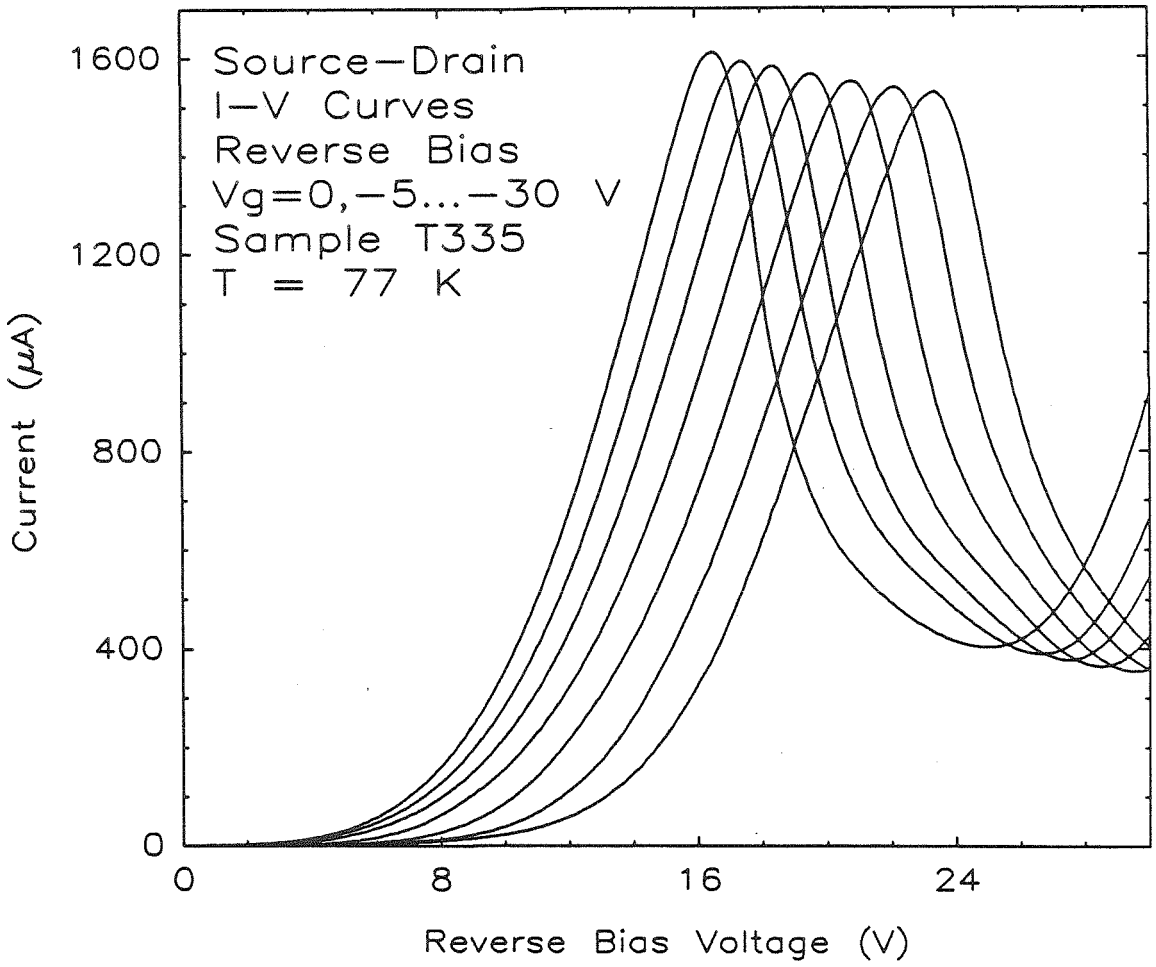


Figure 3.8: Reverse-bias common-drain I–V curves for sample T335 taken at 77 K, with V_g as a parameter. The leftmost curve was taken with $V_g = 0$. V_g is incremented in -5 V steps, to a maximum of -30 V. NDR shifts to higher biases at V_g is incremented. This is the same device illustrated in Fig. 3.7.

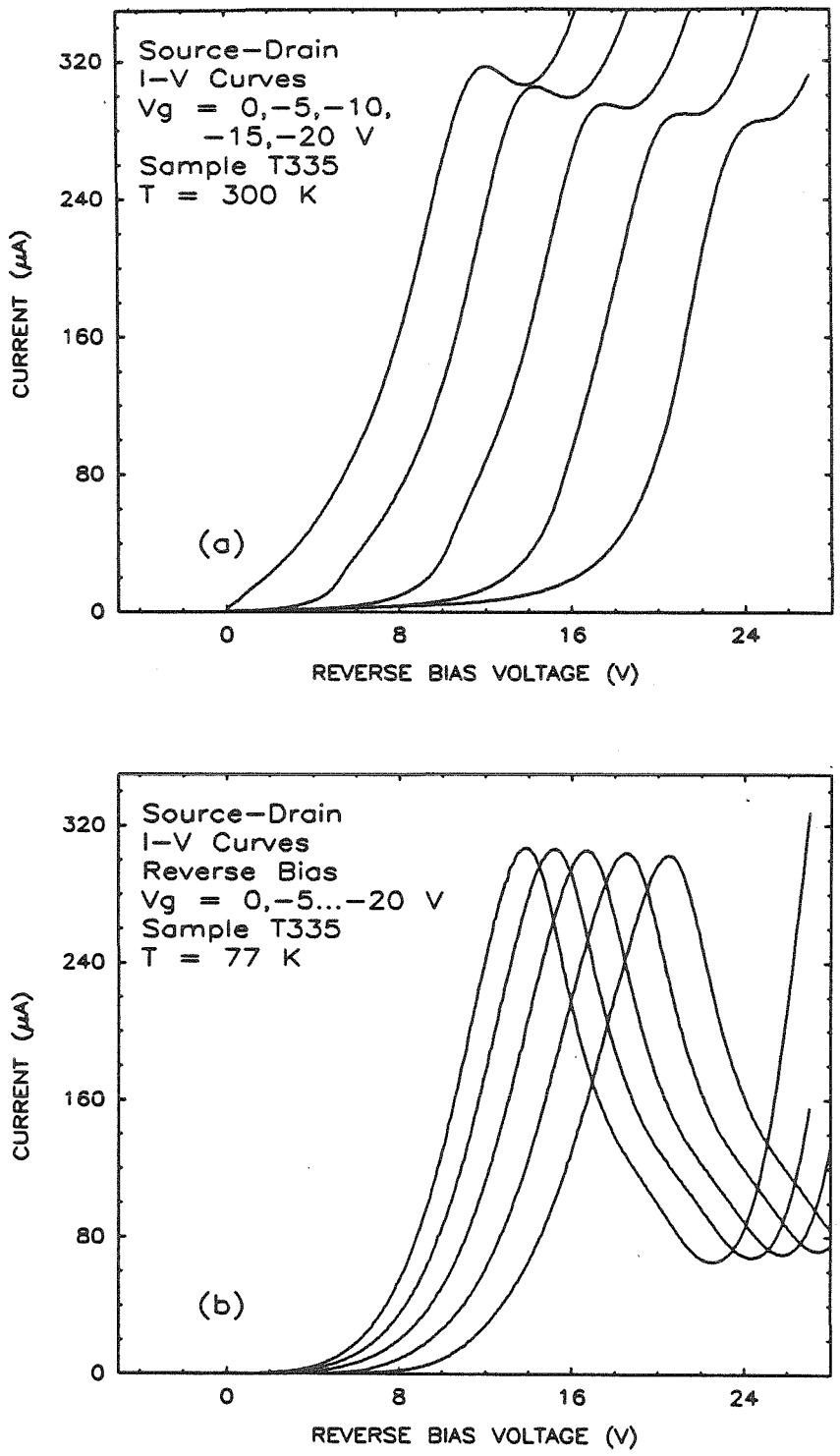


Figure 3.9: Additional data for sample T335. Conditions are similar to those described for Fig. 3.7. (a) 300 K data (b) 77 K data.

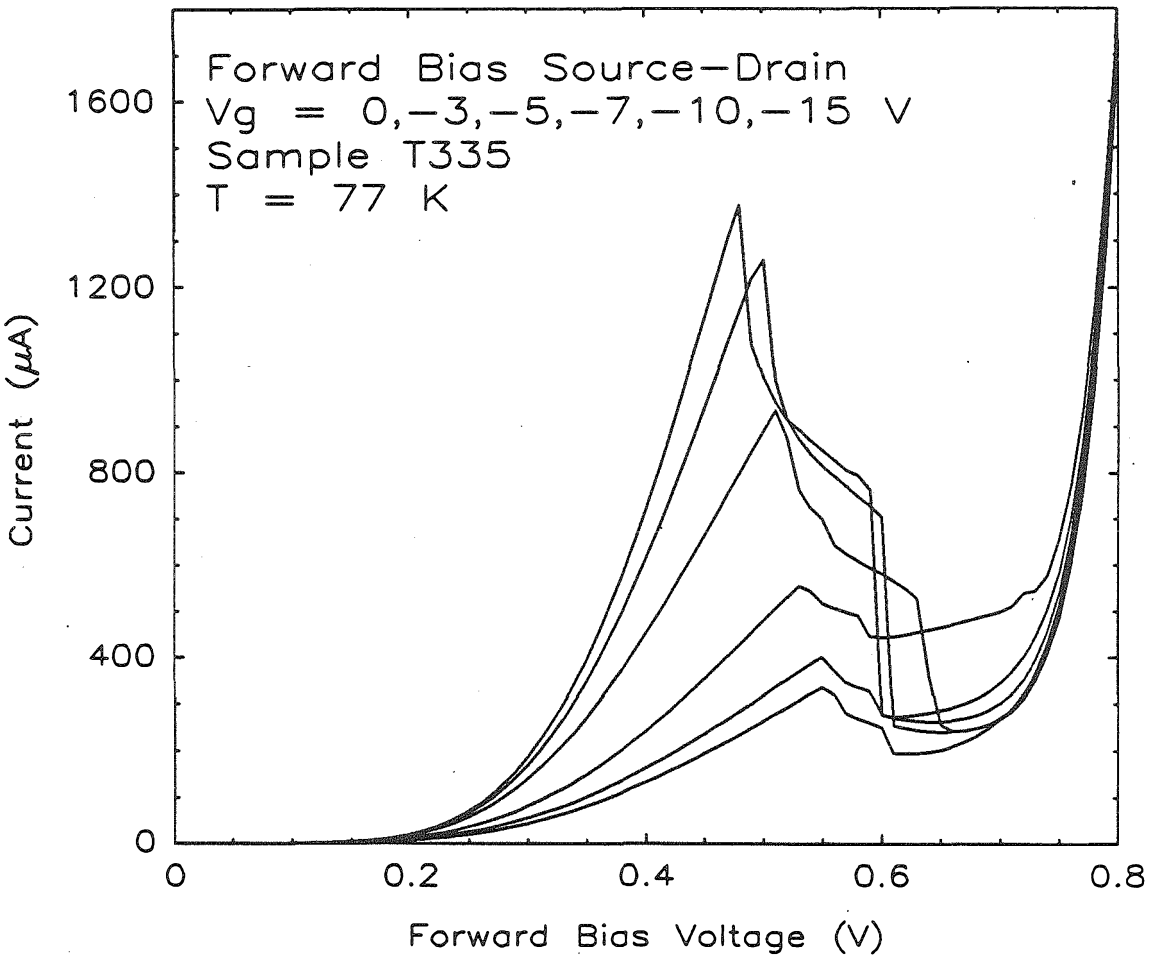


Figure 3.10: Forward-bias common-source data for sample T335 at 77 K, with V_g as a parameter. Data are similar to Fig. 3.6.

back side of the double barrier. This region is depleted in reverse bias and acts as a large region over which to drop bias. To satisfy the resonance condition across the double barrier, a larger bias must be applied across the entire structure.

A simple calculation demonstrates the validity of this explanation. Channel doping for sample T245 is about $1.5 \times 10^{16}\,\mathrm{cm}^{-3}$. From Fig. 3.5 we see that NDR is observed at about 7 V. Voltage drops quadratically with distance in a doped semiconductor, according to Poisson's equation:

$$\frac{d^2V(x)}{dx^2} = \frac{\rho(x)}{\epsilon}, \tag{3.2}$$

$$\frac{d^2V(x)}{dx^2} \approx -\frac{qN_d}{\epsilon} \; for \; 0 < x < W, \tag{3.3}$$

where $V(x)$ is the voltage and ρ is the charge density, and other symbols are defined as in Eq. 3.1. Eq. 3.3 is obtained by making the *depletion approximation*, which assumes that the entire voltage is sustained in a region $0 < x < W$ in which no free carriers are present.[3] This equation can be solved to determine the voltage drop as a function of distance in the material. The boundary conditions are that the voltage be equal to the applied voltage, V_0, at $x = 0$, and be equal to 0 at $x = W$, the edge of the depletion region. Solving for the potential above ground at a point x in the depletion region:

$$V(x) = \frac{qN_dW^2}{2\epsilon}\left\{\frac{x}{W} - \left(\frac{x}{W}\right)^2\right\} + V_0\left\{1 - \frac{x}{W}\right\}. \tag{3.4}$$

Substitution of the definition of W from Eq. 3.1 (neglecting the kT/q factor) yields the following expression:

$$V(x) = V_{bi}\left[\frac{x}{W} - \left(\frac{x}{W}\right)^2\right] + V_0\left[1 - \frac{x}{W}\right]^2, \tag{3.5}$$

where V_{bi} is the built-in voltage of the Schottky barrier, equal to about 0.9 V for Au on GaAs. From Eq. 3.1, W is about 8700 Å for a doping of $1.5 \times 10^{16}\,\mathrm{cm}^{-3}$ (the doping in sample T245) at a reverse bias of 7 V. Therefore, the voltage at

a position $x \sim 100\,\text{Å}$ (representing roughly the location of the double barrier) is about 6.85 V. The potential difference across the double barrier is therefore about 150 mV, a reasonable resonance voltage. This explains why NDR is observed at a large bias level.

The voltage drop arguments just presented have the effect of expanding the resonance along the voltage axis, making it possible to study any structure that might be evident in the resonance level by increasing the resolution along the voltage axis. In effect the lightly-doped region "blows up" the resonance region along the voltage axis. The effect is more pronounced in sample T335 because the doping is even lower, thus making W larger in Eq. 3.5 and requiring still greater voltages to observe resonance.

3.9.2 Forward-Bias Behavior

The observation of NDR close to zero bias is consistent with the asymmetry of the device. In forward bias the large lightly-doped region beneath the double barrier is not depleted, and therefore does not present a large region over which to drop bias. Therefore, NDR is seen close to zero bias. In fact, the position of the NDR will depend in detail on the dynamics of the accumulation region near the double barrier. Band-bending is critical in determining the voltage at which NDR is seen.[3]

Device behavior is radically different in forward bias, as compared to reverse bias. The peak-to-valley current ratio is more dramatically affected by V_g in forward bias than in reverse bias. This result, consistent for all DB/VFET samples that worked in both bias directions, indicates that more significant modulation of the peak-to-valley current ratio is possible when carriers are affected prior to injection rather than afterwards. There are two important differences between forward and reverse bias that may account for this effect. First, the depletion region under

the gate reaches its maximum extent near the drain end of the channel. In forward-bias operation the drain end of the channel lies near the double barrier and may be more effective in controlling the tunneling current. More importantly, tunneling electrons are injected from a region beneath the double barrier in forward bias. It is possible that the gate bias affects the carrier population in the accumulation region prior to injection across the double barrier. In reverse bias, carriers are injected from the degenerately doped top electrode, on whose population the gate has no effect.

3.9.3 Room-Temperature NDR

Room-temperature NDR was observed in one DB/VFET sample, T335. This sample exhibits room-temperature NDR in only one bias direction. In this direction (reverse bias), electrons were injected into the lightly-doped channel region of the VFET. This result suggests that it is more important to have low-doping on the side of the double barrier into which carriers are injected, rather that on the side from which they originate. This conclusion is supported by recent results obtained with our MBE machine.[§]

It is also interesting to note that the improvement in peak-to-valley current ratio seen with temperature is mainly due to a decrease in the valley current. This suggests that the improvement is mainly due to a decrease in excess current mechanisms, rather than an improvement in resonant tunneling. This point is illustrated by considering the previously illustrated data for sample T335 in Figs. 3.7, 3.8, and 3.9.

[§]Several MBE samples have been grown with known doping asymmetries (see Chapter 2 for more details), all of which exhibit NDR or inflections a bias direction that is consistent with the MOCVD results presented here.

3.9.4 Common Source versus Common Drain

In a three-terminal device, a variety of bias configurations are possible. For an FET the predominant configuration is referred to as common source. There is another configuration, however, in which the drain is common between gate and source, referred to as common-drain configuration. A common-source junction field-effect transistor (JFET) is illustrated in Fig. 3.11.

For a MESFET in the simple linear model, voltage drops linearly along the channel. Consider a common-source configuration similar to that illustrated in Fig. 3.11. Denoting the absolute value of the gate bias as V_g, and the drain bias as V_d, the bias on the gate at the drain end of the channel will be $V_g + V_d$. At the source end of the channel, the bias is simply V_g.

Consider a case in which the drain is grounded and the source is negatively biased. The flow of carriers is identical to the previous case, but the gate bias is different. The bias at the drain end of the channel is now V_g, and the bias at the source end is the difference of the source bias and the gate bias. Depending upon which terminal is more negative, a net positive bias may exist on the gate at the source end of the gate. A large positive gate current would then result, and a dramatic increase in the negative source current. This explanation points out the differences between common-source and common-drain operation.

The data presented in Section 3.8 were taken with the substrate grounded, meaning that reverse-bias data were taken in common-drain mode (the substrate was grounded and the mesas were biased negatively). The behavior of the device is qualitatively similar in either configuration. However, common-drain operation is preferable for these devices in most instances, for two reasons. Since the bias at the drain end of the channel is greater in common-source mode, one expects that NDR will be shifted to larger bias levels than for a common-drain operation, even at $V_g = 0$. The total bias on the gate can be large, since a lot of drain bias must

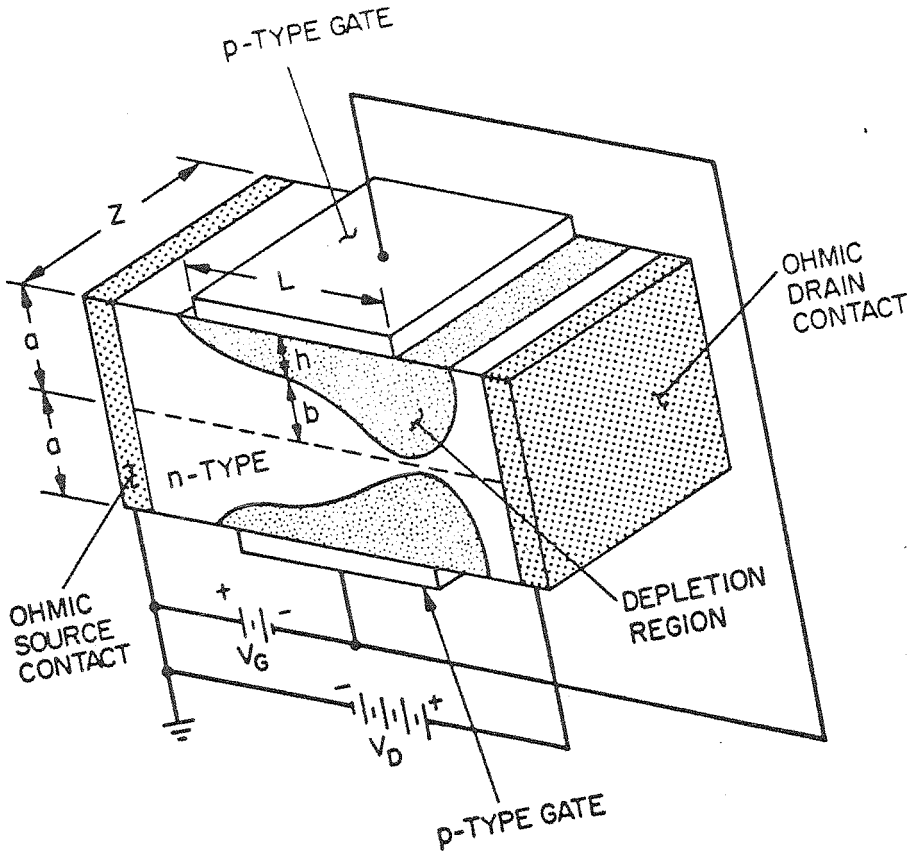


Figure 3.11: A schematic diagram of a JFET device connected in a common sour
configuration, from Ref. 2

be applied to observe NDR. This voltage ($V_g + V_d$) may exceed the breakdown voltage of the gate, resulting in incomplete characteristics. These two effects are illustrated in Fig. 3.12.

The net forward bias of the gate alluded to previously does not take place in these samples, because of the position of the gate contact. Since it does not lie physically on the channel, the bias at the gate contact does not become positive until substantial bias is applied between source and drain. Some devices did exhibit this phenomenon. For higher-performance devices, in which the gate would be placed directly on the channel, forward bias of the gate might become an issue, and common-source operation might be preferred.

In forward bias the source-drain bias is small compared with the gate bias. Therefore, there is no difference between common-drain and common-source operation.

3.9.5 Variable Cross Section

To confirm that the device is operating as we have described, we have fabricated devices from samples T335 and T245 that have variable mesa cross sections. Devices with nominal cross sections of 5 μm, 10 μm, and 20 μm were made. Measurements of the cross sections of the devices were performed using optical microscopy. These measurements showed the actual cross sections to be about 2.1 μm, 6.6 μm, and 16.7 μm. The discrepancy between designed and realized mesa width explains why the 3 μm designed mesas (also present on this mask) did not work. The gate-to-gate spacings remained as designed at 7 μm, 12 μm, and 22 μm. Data for common-source biasing of a variable cross-section preparation of sample T335 are illustrated in Fig. 3.12.

Several devices of each cross section were tested. Two major results come out of this study. First, improved performance with decreasing gate spacing was seen.

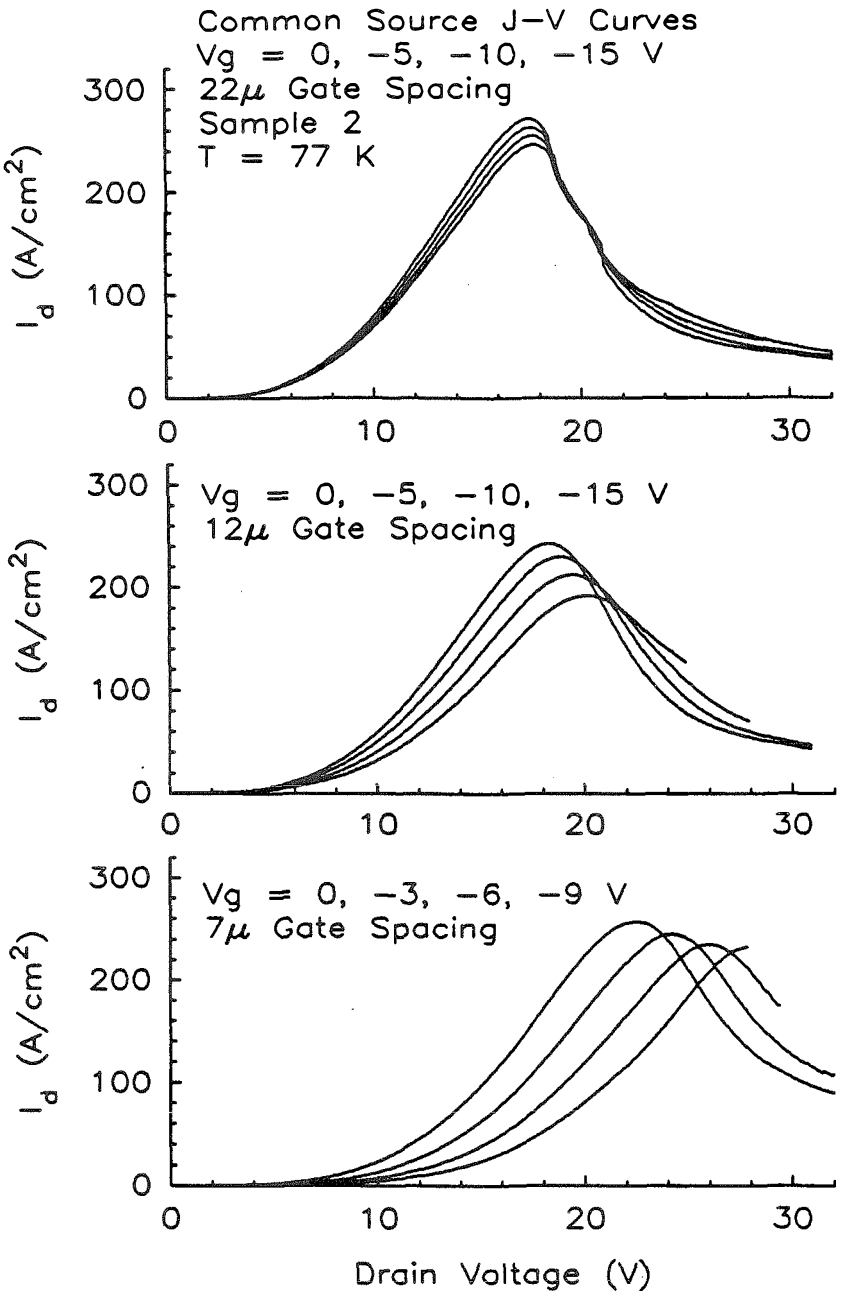


Figure 3.12: Common-source *I–V* data for sample T335 at 77 K, for a variety of gate-to-gate spacings. This figure illustrates a number of interesting points. First, it illustrates common-source biasing. Second, it shows that current scales with area. Finally, it verifies that device performance improves with decreasing gate spacing.

One expects such an improvement because the lateral extension of the depletion region is a more significant effect in smaller mesa devices. Second, current was found to scale with area. Calculations of current density at the peak of the NDR for devices with different cross section were made, taking into account surface depletion effects. Current was found to scale with area to within 10 percent in Fig. 3.12.

3.10 Supplementary Data

A total of 5 working DB/VFET devices were obtained. Samples T245 and T335 were clearly superior to the remaining three samples. Nevertheless, a complete description of the project requires the inclusion of samples T338, T410, and T411. This section presents these clearly supplementary results.

3.10.1 Sample T338

Sample T338 is characteristic of samples T336, T337, T338, and T339, which were produced with similar channel characteristics. Silane doping was used in these samples. This doping was used in an attempt to obtain a buffer layer without inducing a memory effect. The resultant structures exhibited markedly poor surface quality. Sample T335 was grown on the same day as these samples and had excellent surface morphology. The conclusion is that contaminated Silane may have been present or that the temperature was not optimum for good growth with Silane doping. T338 was the only sample of the four exhibiting any evidence of resonant tunneling. Data for sample T338 are illustrated in Fig. 3.13. These data are consistent with the T245 and T335 results.

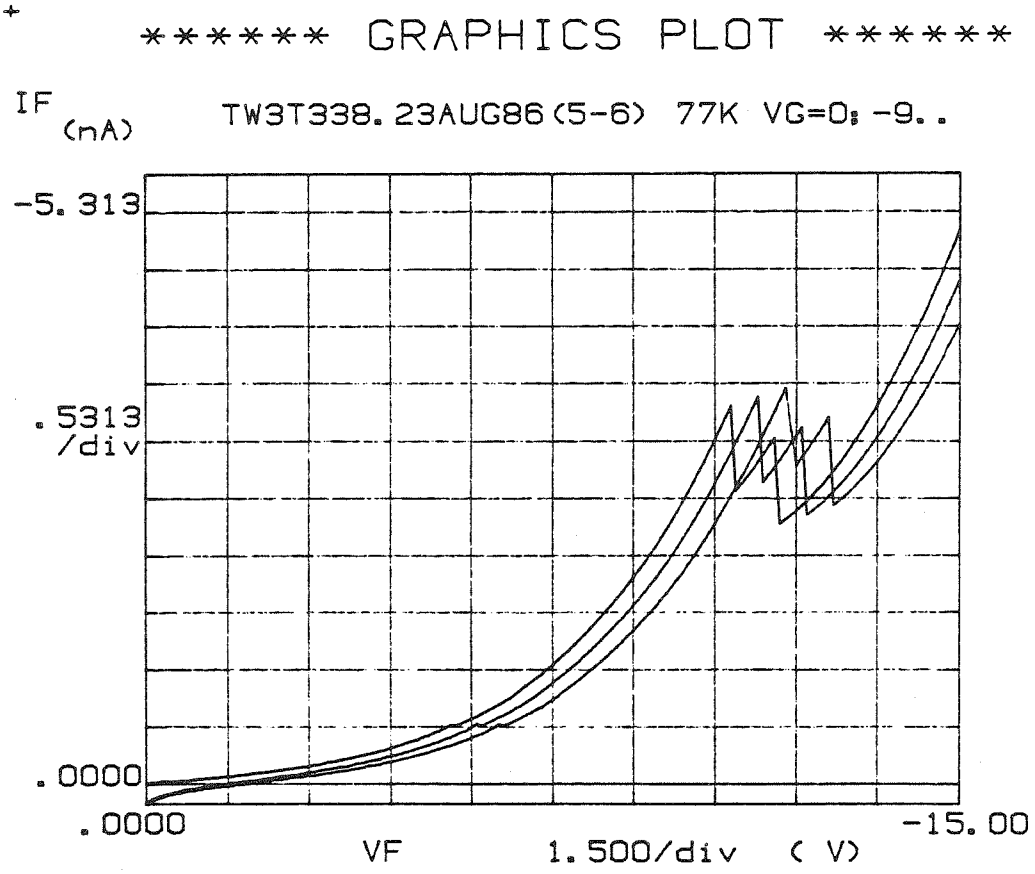


Figure 3.13: Reverse-bias common-drain data for sample T338, taken at 77 K with V_g as a parameter.

3.10.2 Sample T410

This sample differs from previous samples in that a lightly-doped spacer layer was not grown on top of the double barrier. The omission of the spacer layer had an impact on the I–V curve. Evidence for tunneling at zero bias was seen and is illustrated in Fig. 3.14. In particular, forward-bias NDR was seen at extremely low bias levels. suggesting that the geometry of the double barrier differs from samples T245 or T335. In particular, it is possible that the first resonance level is close to the bottom of the well *i.e.* that the well is thicker than in previous samples. This is probably true for sample T411 as well, since they were grown sequentially. The reverse-bias behavior suggests that tunneling at zero bias is quenched by the FET section of the device. In fact, the near zero bias I–V curve looks a lot like an FET characteristic. When higher levels of voltage are applied, NDR is observed, and shifted by gate bias. Is the NDR observed at high bias levels in this sample due to the ground state or the first excited state? The answer to this question is not known. It should be noted that relatively few data were taken on this sample.

3.10.3 Sample T411

This sample exhibits well defined DB/VFET characteristics. The common-drain characteristics of the sample are illustrated in Fig. 3.15. The major problem with the device is its extremely low current density. More current is drawn through the gate of samples T245 and T335 than is seen in the source-drain I–V of this sample. Thus, gate leakage current could be a problem for this device.

The behavior of this sample is consistent with that observed in other devices. C–V data for sample saturated at about $V = -3$ V and remained constant out to about $V = -35$ V. The capacitance saturation suggests that the channel is fully depleted at -3 V and that additional gate bias drops in the heavily doped substrate, with some lateral extension. The thickness estimated from these results

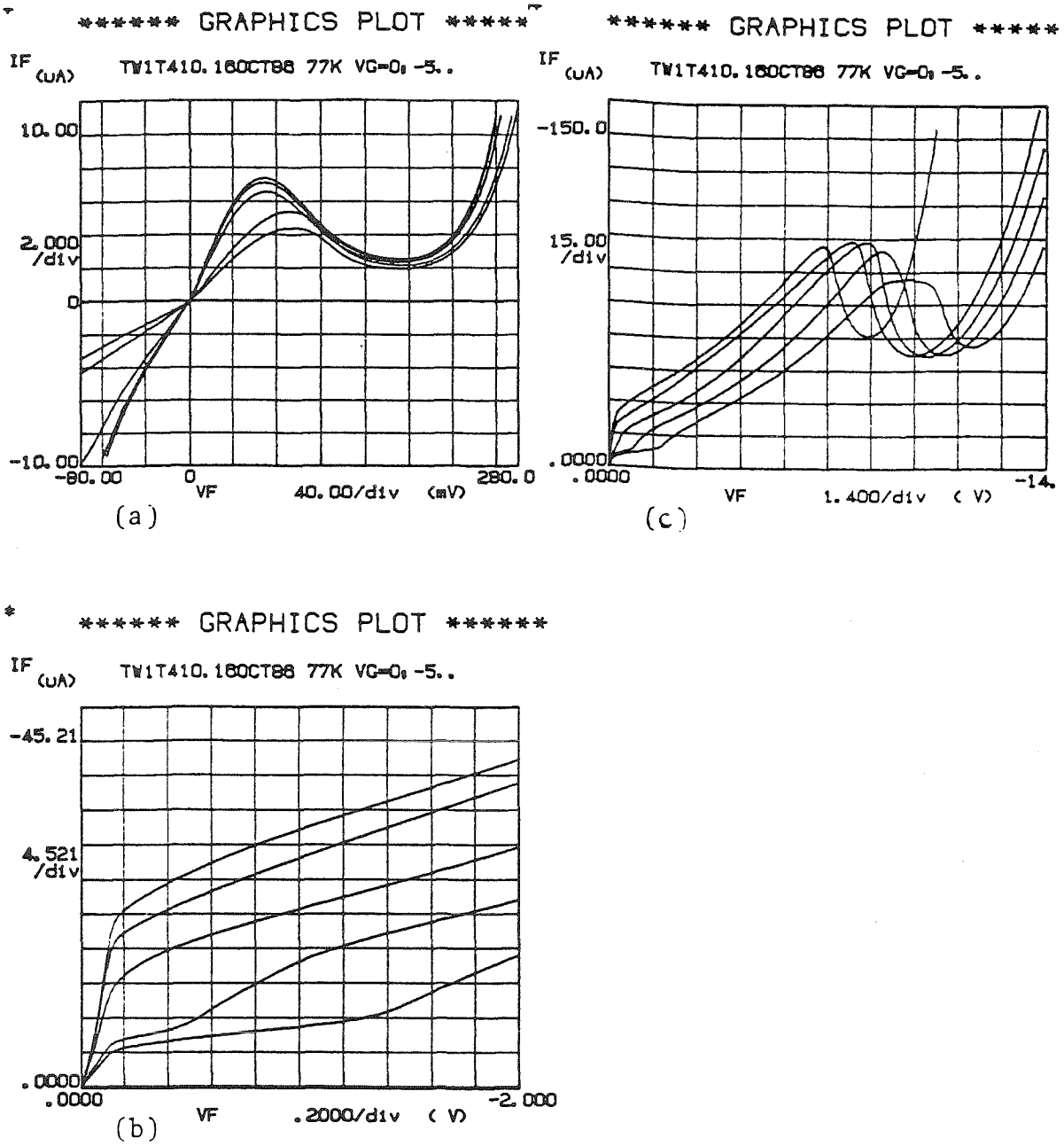


Figure 3.14: I–V data for sample T410. Several sets of curves are illustrated. (a) Forward-bias behavior at 77 K, with V_g as a parameter. V_g is incremented in -5 V steps to a maximum of -20 V. (b) Reverse-bias behavior at low voltage levels at 77 K, with V_g as a parameter. V_g is incremented in -5 V steps, to a maximum of -20 V. (c) Reverse-bias I–V behavior at high voltage levels, with V_g incremented as in (b).

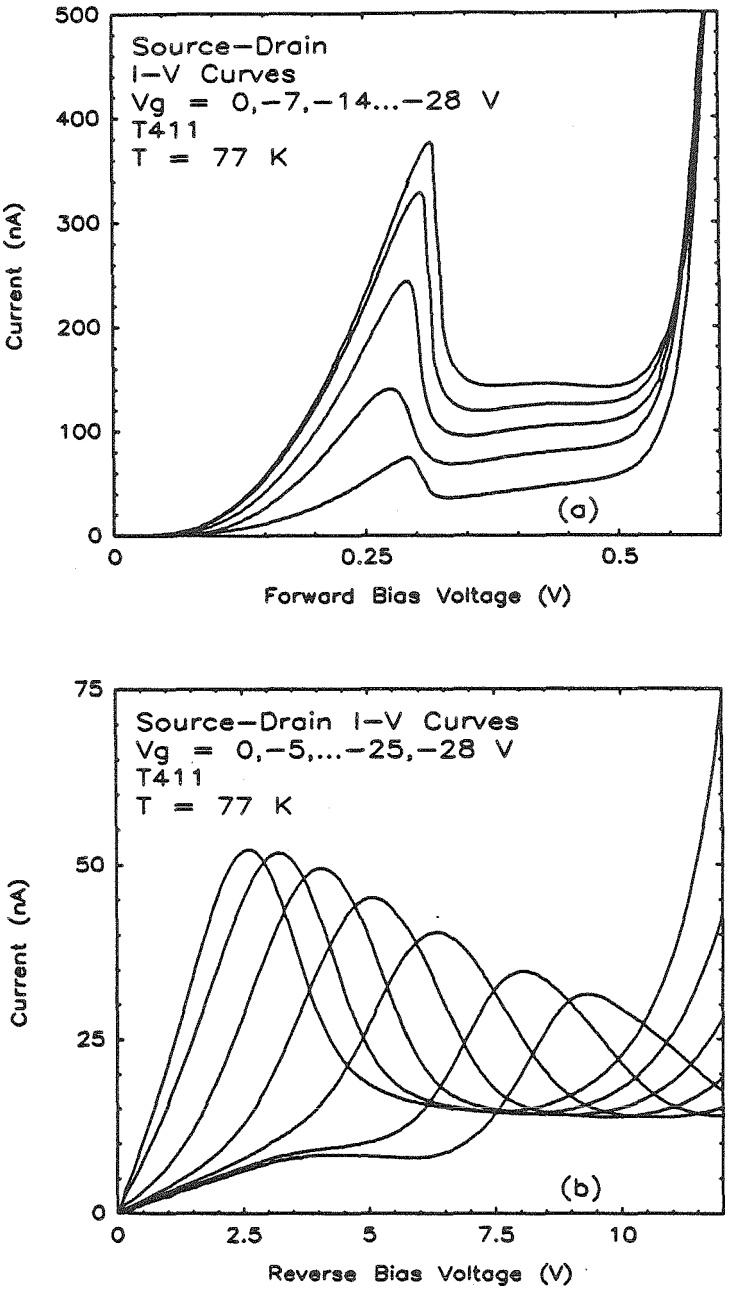


Figure 3.15: (a) I–V curves for sample T411 in forward-bias common-drain configuration, at 77 K, with V_g as a parameter. Gate voltage was incremented in -7 V steps. (b) Reverse-bias common-drain data for sample T411, at 77 K, with V_g as a parameter. V_g was incremented in -7 V steps, except for a -3 V step from -25 to -28 V.

is about 2μm. The lateral extension of the gate field should be the source of the shift in NDR with gate voltage, which is quite significant for this device. NDR is observed at about -3.0 V, which is about ten times larger than the forward-bias resonance position. This voltage shift in the position of the NDR is consistent with the explanation presented in Section 3.9.1.

By comparing with T410 data, we conclude that this sample exhibits tunneling at very low bias levels, possibly due to a different device geometry. This, and the decreased thickness of the lightly-doped channel, explains why NDR is not seen at biases comparable to sample T335. The thinner channel region does not allow as much bias to be sustained across it as in other samples. It may be that the presence of a lightly-doped spacer layer on top of the double barrier (present in this sample, but lacking in T410) allows a lower-voltage resonance to be seen in this sample, when it was absent in T410.

3.11 Theoretical Considerations

Modeling the DB/VFET would be an interesting theoretical problem. No theoretical modeling of the device was done for this thesis. However, several important issues were brought to light by this study. First, the DB/VFET device is not a simple device. The lack of simplicity comes from the fact that the double barrier and the VFET parts of the device interact with one another in a fundamental way. The interaction takes place in the thick lightly-doped channel region, and manifests itself in the appearance of NDR at high bias levels.

Another important issue was mentioned early in this chapter; the lateral depletion from the Schottky-barrier gate. This lateral extension is responsible for the transistor effects. The simple, heuristic model of a capacitor plate mentioned earlier needs to be elaborated upon in order to obtain a good theoretical understanding

of the device. In addition to the solution of Poisson's equation in two dimensions, the source-drain bias must be taken into account. The bias between source and drain depletes some of the channel underneath the double barrier, meaning that lateral extension of the gate field takes place in a region in which field is already present. It is clear from an examination of the data for sample T335 that the effect of the gate is *not* to add a simple series resistance to the source drain characteristic. If linear resistance were added, the peak of the NDR would shift along the voltage axis more than the valley would, because more current passes through the device at the peak than at the valley of the NDR. Since this is not the case, a nonlinear interaction between the various space charge regions may be occurring. The final model might resemble a vacuum tube.

3.12 Conclusions

This chapter presents several important results. They are summarized below.

1. Working VFETs with horizontal electrodes have been demonstrated.
2. Integration of a resonant tunneling heterostructure and a VFET was demonstrated.
3. Progress in MOCVD growth was made.
   (a) MOCVD-grown double barriers with room-temperature NDR were demonstrated.
   (b) Successful growth of DB/VFET devices without a buffer layer was demonstrated.
   (c) Background doping in the $1 \times 10^{15}\,\mathrm{cm}^{-3}$ range was achieved. This is the lowest background level recorded in the Xerox reactor.

4. Several novel DB/VFET properties were observed and explained.

   (a) NDR was observed at high voltage in reverse bias.

   (b) Modulation of the position of the NDR, without changing the peak-to-valley current ratio, was obtained in reverse bias.

   (c) Modulation of the peak-to-valley current ratio, without shifting the NDR voltage, was obtained in forward bias.

5. The importance of low doping of the side of the structure into which carriers are injected was demonstrated.

Double-Barrier Growth Parameters

Sample No.	Top Layer Data		Double-Barrier Data				Date Grown (DDMMMYY)
	Depth (μm)	Buffer (sec)	Barriers (sec)	Well (sec)	Dopant	Temp. (°C)	
S008	0.55	20	2.0	1.3	Mg	775	27FEB86
S031	0.6	20	2.0	1.3	Mg	775	13MAR86
S048	0.65	20	2.0	1.3	Mg	775	25MAR86
T223	0.6	20	2.0	1.3	Mg	775	20MAY86
T228	0.6	20	2.0	1.3	Mg	775	23MAY86
T231	0.7	20	2.0	1.3	Mg	775	28MAY86
T238	0.5	20	2.0	1.3	Mg	775	2JUN86
T245	0.37	20	2.0	1.3	Mg	775	5JUN86
T290	0.6	20	2.0	1.3	Mg	800	2JUL86
S192	0.3	20	2.0	1.3	Mg	825	30JUN86
T335	0.3	20	2.0	1.3	Mg	770	31JUL86
T336	0.45	20	2.0	1.3	Mg	775	31JUL86
T337	0.45	60	2.0	1.3	Mg	770	31JUL86
T338	0.5	20	2.0	1.3	–	770	31JUL86
T339	0.3	60	2.0	1.3	–	770	1AUG86
T361	0.5	20	2.0	1.3	Mg	775	14AUG86
T365	0.45	20	2.0	1.3	Mg	775	15AUG86
T367	0.5	20	2.0	1.3	Mg	775	21AUG86
T407	0.4	–	2.0	1.3	Mg	775	7OCT86
T410	0.3	–	2.0	1.3	–	775	8OCT86
T411	0.46	20	2.0	1.3	–	775	8OCT86
T422	0.36	–	2.0	1.3	–	775	16OCT86

Table 3.2: A table of double-barrier parameters for the DB/VFET. MOCVD growth parameters were as follows: TMGa flow rate was about 15 sccm, with the TMAl flow rate varied between 30 and 40 sccm to obtain $Al_xGa_{1-x}As$ with $x \sim 0.4$. The AsH_3 flow was about 500 sccm. H_2 was the carrier gas, at 3.0 SLM. See text for information on double-barrier dimensions.

FET Growth Data for DB/VFET Samples

Sample No.	Channel Data				Buffer (Y/N)
	Time (min)	Temp. (°C)	Thickness (μm)	Doping (cm^{-3})	
S008	2	775	0.5	10^{17} range	Y
S031	2	720	0.6	10^{17} range	Y
S048	5	775	1.0	10^{17} range	Y
	2	775	0.5	10^{17} range	
T223	2	725	0.3	est. 10^{17} range	Y (Si 1)
T228	2	725	0.2	10^{17} range	Y (Si 1)
T231	2	725	0.6	10^{17} range	Y (Si 1)
	2	775	0.6	10^{17} range	
T238	20	775	2.0	10^{17} range	N
	2	725	0.4	unknown	
T245	20	825	1.6	1.5×10^{16}	N
	5	725	0.6	$n < 1.5 \times 10^{16}$	
T290	15	850	1.5	low	N
	15	700	1.5	very low	
S192	20	825	2.0	10^{16} range	N
	5	775	0.5	2×10^{16}	
T335	25	750	3.2	$1 - 3 \times 10^{15}$	N
T336	5	800	0.6	est. 10^{17}:Si	N
	10	800	1.3	10^{15} range	
	10	725	1.3	10^{15} range	
T337	As in T336				
T338	As in T336				
T339	As in T336				
T361	Bad susceptor p-type doping				
T365	Bad susceptor p-type doping				
T367	20	750	4.8	$2 - 5 \times 10^{15}$	N
T407	10	775	2.2	low 10^{15} range	N
T410	10	750	2.2	low 10^{15} range	N
T411	10	750	2.0	low 10^{15} range	N
T422	10	825	1.6	low 10^{16} range	N

Table 3.3: A Table of channel data for the DB/VFET. MOCVD growth parameters were as in Table 3.2.

Operating Parameters of DB/VFET Samples, 77 K

Sample No.	NDR Data (F)orward and (R)everse Bias						FET (Y/N)
	Voltage (V)		J_{peak} (A/cm^2)		P/V Ratio		
	F	R	F	R	F	R	
S008	0.1	−0.1	10^{-1}	10^{-1}	4	4	N
S031	0.01	−0.09	–	–	1.2	1.05	N
S048	0.32	−0.1	–	–	1.1	1.1	N
T223	none	none	–	–	–	–	N
T228	0.04	−0.06	10^{-2}	10^{-2}	1.8	4	N
T231	0.9	none	10^{-1}	–	1.5	–	N
T238	0.05	−0.05	10^{-2}	10^{-2}	1.16	2.8	N
T245	0.35	−6.5	8	45	5	5.6	Y
T290	none	none	–	–	–	–	N
S192	none	none	–	–	–	–	Y
T335	0.5	−17	150	250	9	7	Y
T336	none	none	–	–	–	–	N
T337	none	none	–	–	–	–	N
T338	none	−11	–	10^{-4}	–	1.4	Y
T339	none	none	–	–	–	–	N
T361	none	none	–	–	–	–	N
T365	none	none	–	–	–	–	N
T367	none	–	–	–	–	–	Y
T407	none	none	–	–	–	–	N
T410	0.07	−7	1	10	2.7	2	Y
T411	0.3	−2	0.04	0.003	2.6	2.6	Y
T422	0.07	−0.18	1	2.5	5	2.3	N

Table 3.4: A summary of the operating characteristics of DB/VFET samples. This information was collated from 80 preparations of the listed samples. Voltages refer to the NDR peak and are averages, where possible. Peak-to-valley (P/V) current ratios are maximum values. Current densities are are obtained from the current at the peak of the NDR. FET (Y/N) refers to whether V_g affected the source-drain characteristic.

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Chapter 4

DB/MESFET Devices

This chapter is concerned with the growth, fabrication, and testing of a double-barrier heterostructure combined with a metal-semiconductor field-effect transistor (DB/MESFET).

4.1 Introduction

The DB/MESFET device is formed by the series integration of a double-barrier tunnel structure and a planar field-effect transistor, in this case a metal-semiconductor field-effect transistor. There are several reasons for pursuing the DB/MESFET. This device should have a high input impedance, with NDR at two of its three terminals. Such a device might be desirable for logic and signal processing. The DB/MESFET should differ operationally from the DB/VFET, because of the gate placement. Also, this kind of device structure could be integrated with existing GaAs circuits. Finally, the understanding of the MESFET is such that comparison to well-known theory could be made.

4.1.1 Summary of Results

Altogether, 11 samples were produced, all of which functioned to varying degrees. Transistor action was seen at much lower gate-bias levels than in the DB/VFET. Operational current densities ranging from less than 1 A/cm^2 to about 400 A/cm^2 were demonstrated. Results are compared to theory and found to be consistent with a simple linear MESFET model. Finally, a wide variety of characteristics were demonstrated, depending upon the relationship between the double barrier and the MESFET. The DB/MESFET, DB/VFET, and another integrated double-barrier structure were initially proposed in Ref. 1.

4.1.2 Outline of Chapter

This chapter has much the same structure as Chapter 3. Initially, the device concept and design are described. Growth issues are the next topic, wherein a novel doping technique is described. Mask design and fabrication procedure are covered next. Following this discussion, fundamental results for two devices are presented. A discussion follows, in which consistency with simple MESFET models is demonstrated. Supplemental results for an additional 5 samples are then presented. Finally, the main points of the chapter are summarized in a concluding section.

4.2 Concept and Design

The device concept for the DB/MESFET is to terminate a planar MESFET growth by the deposition of a double-barrier tunnel structure. The finished device is schematically illustrated in Fig. 4.1. This structure incorporates a recessed-gate design. The important point about this design for device considerations is that the n^+ region separates the double barrier and the MESFET, preventing device

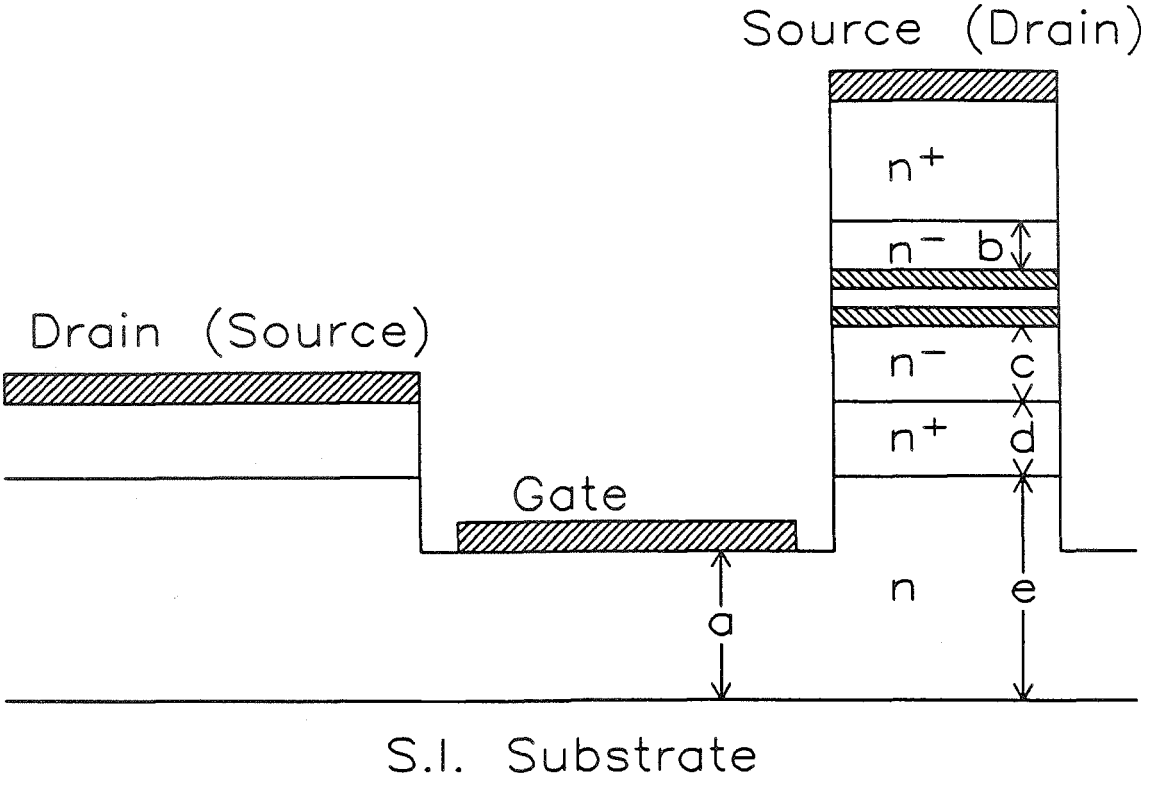

Figure 4.1: Cross section of recessed-gate DB/MESFET.

interaction of the sort seen in the DB/VFET. If this sort of interaction is desired, ion implantation techniques could be used.

The theory of the MESFET is well developed.[2] The basic idea is that the depletion region underneath a reverse-biased Schottky barrier is used to modulate the current transport through the region being depleted. Several models exist, which predict the behavior of the device quite well. The simple linear model is the least complex. For short-channel devices, a saturated velocity model may be more appropriate. These subjects will be dealt with in more detail in Section 4.6.

The operation of the device is straightforward. In common-source reverse-bias operation, electrons flow from the grounded mesa structure containing the double barrier, through the channel of the MESFET to the positively biased drain contact.

The resistance of the channel is variable and modulates the position and peak-to-valley current ratio of the NDR. Operation in the opposite bias direction, in which electrons travel the other direction in the channel, should also be possible. The two configurations do *not* have to yield the same characteristics.

4.3 Growth

Samples were grown at Xerox Research Laboratory, in Palo Alto, California. MOCVD epitaxial growth techniques were used to realize the structures. This project benefits from the work that has been done on the DB/VFET in perfecting the growth of negative resistance structures. All but one of the samples grown for this project exhibited NDR in their source-drain characteristics. The recipe for double-barrier growth was the same for most devices. Some modifications were introduced in later growths, which had a very pronounced effect on the device behavior. Growth parameters are summarized in tables at the end of the chapter.

4.3.1 Recessed Gate

The central problem associated with production of working DB/MESFET samples lay not with the double barrier, but with the MESFET portion of the device. For a planar MESFET, a good ohmic contact and a good Schottky contact must be obtained on the same material. This requirement restricts the acceptable doping level for the channel to a level around $1 \times 10^{17}\,\mathrm{cm}^{-3}$. This doping level is difficult to achieve in the MOCVD reactor with which our samples were produced. The reason has to do with the details of the reactor design and the purpose for which it was intended. To separate the two problems, a recessed-gate design was employed. A wider range of acceptable channel-doping levels can be accomodated with the use of a recessed-gate design. Such a design is shown in Fig. 4.1.

4.3.2 Pulsed Doping

The problem of channel doping remains. The doping level of interest is in the $10^{16}\,cm^{-3}$ range, which is higher than the background doping levels needed for the DB/VFET. It is possible to tailor the background level to be large enough for this purpose, but the background dopant is not well controlled, typically exhibiting photosensitive behavior. One would prefer to control the doping via introduction of a known shallow dopant.

A pulsed doping approach was found to be successful in obtaining moderate doping levels. Consider a case in which a layer of about 3000 Å is desired. At the usual growth rate of 2000 Å/minute, such a layer would take about 90 seconds to deposit. By cycling the H_2Se dopant on for 1 second and off for 3 seconds, a lower doping level may be obtained than if the Se were on for the entire growth. A range of dopings can be attained with this technique, as illustrated in Fig. 4.2. In addition to the cycle time, the H_2Se flow rate can be adjusted to increase the doping without increasing the cycle time. A first order approximation for the resultant doping is that it would decrease by a factor of four from the case in which the Se was on for the entire 90 seconds. There are other effects that prevent this decrease from being the observed. Most importantl is the memory effect already mentioned,* which will tend to increase the doping. The data presented in Fig. 4.2 show that this pulsed-doping method works.

Each sample was grown on semi-insulating *and* n^+ GaAs.† MESFET devices were fabricated from the semi-insulating growth. The n^+ sample was used for doping characterization. Rather than growing directly on the substrate, a buffer layer of several microns of undoped $Al_xGa_{1-x}As$ ($x \sim 0.45$) was grown prior to deposition of the desired device structure. In one case this buffer layer was omitted.

*See Chapter 3 for more about memory effects.

†A small piece of n^+ was loaded alongside half of a semi-insulating wafer.

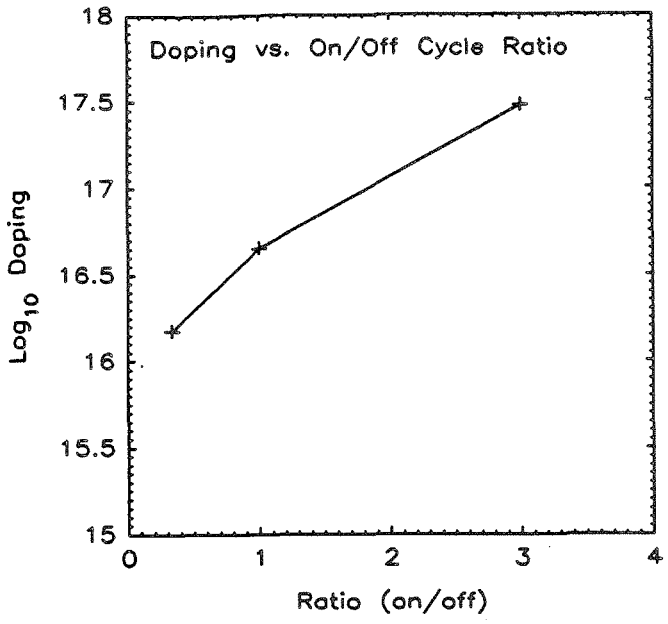

Figure 4.2: Plots of the doping versus the dopant source on/off ratio. The H_2Se flow rate during the 'on' state was 10 sccm. Only those samples that did not show light sensitivity are plotted.

Results for this sample suggest that the buffer layer was desirable.

4.4 Processing

The processing for the DB/MESFET was more involved than for the DB/VFET. The reason for the increased complexity is that all three contacts must be placed on the epitaxial layer. In the DB/VFET one of the contacts was to the substrate. As mentioned previously, growth issues prevented planar layouts from working. Therefore, another level of complexity was added, in the form of a recessed-gate design. Consider Fig. 4.1. The three contacts must be placed in three separate layers. The depth of the final etch will be important to the device function, since it will define the gate width. Careful monitoring of the etch depth is necessary.

4.4.1 Mask Layouts

Several types of layouts were made. Three masks were needed for DB/MESFET fabrication. In keeping with the philosophy of simplified design, it was decided that long gate devices with generous alignment tolerances would be made. Therefore, the first layout was a 30 μm non-recessed gate device with 10 μm alignment tolerances. This fabrication procedure utilized three masks, two etches, and two evaporations, with a mesa contact concept similar to that described in Chapter 3. The mesa containing the double barrier measured 20 $\times$ 80 μm. The finished layout is three-dimensionally illustrated in Fig. 4.3. The additional complexity of a recessed-gate geometry was accommodated *without* adding another mask step.

Three recessed-gate mask sets were made. Each served a particular purpose. The first was very similar to the initial layout illustrated in Fig. 4.3, which illustrates the finished product if one imagines the gate at a lower level. This first mask set utilized a 20 μm gate with 5 μm alignment tolerances, and a double-barrier mesa measuring 30 $\times$ 80 μm. A second layout eliminated the mesa bonding pad in favor of direct wire-bonding to the mesa, which required an increase in mesa area to 60 $\times$ 140 μm. 20 μm gates and 5 μm alignment tolerances were used. Once this mask was demonstrated to yield results unchanged from the first (non-bonded) mask set, most DB/MESFET devices were fabricated using this mask. A three-dimensional cutaway view of the finished fabrication is illustrated in Fig. 4.4. Finally, a narrow-gate mask was made. For ease of comparison to theory, a linear layout was used for this set of masks. The source and drain contacts were rectangular 60 $\times$ 150 μm pads, with a 5 μm gate lying between them, aligned to within 1 μm.

4.4.2 Procedure

The fabrication procedure for the recessed-gate DB/MESFET will now be described. Areas of overlap with the DB/VFET procedure will not be explained.

MESFET FABRICATION

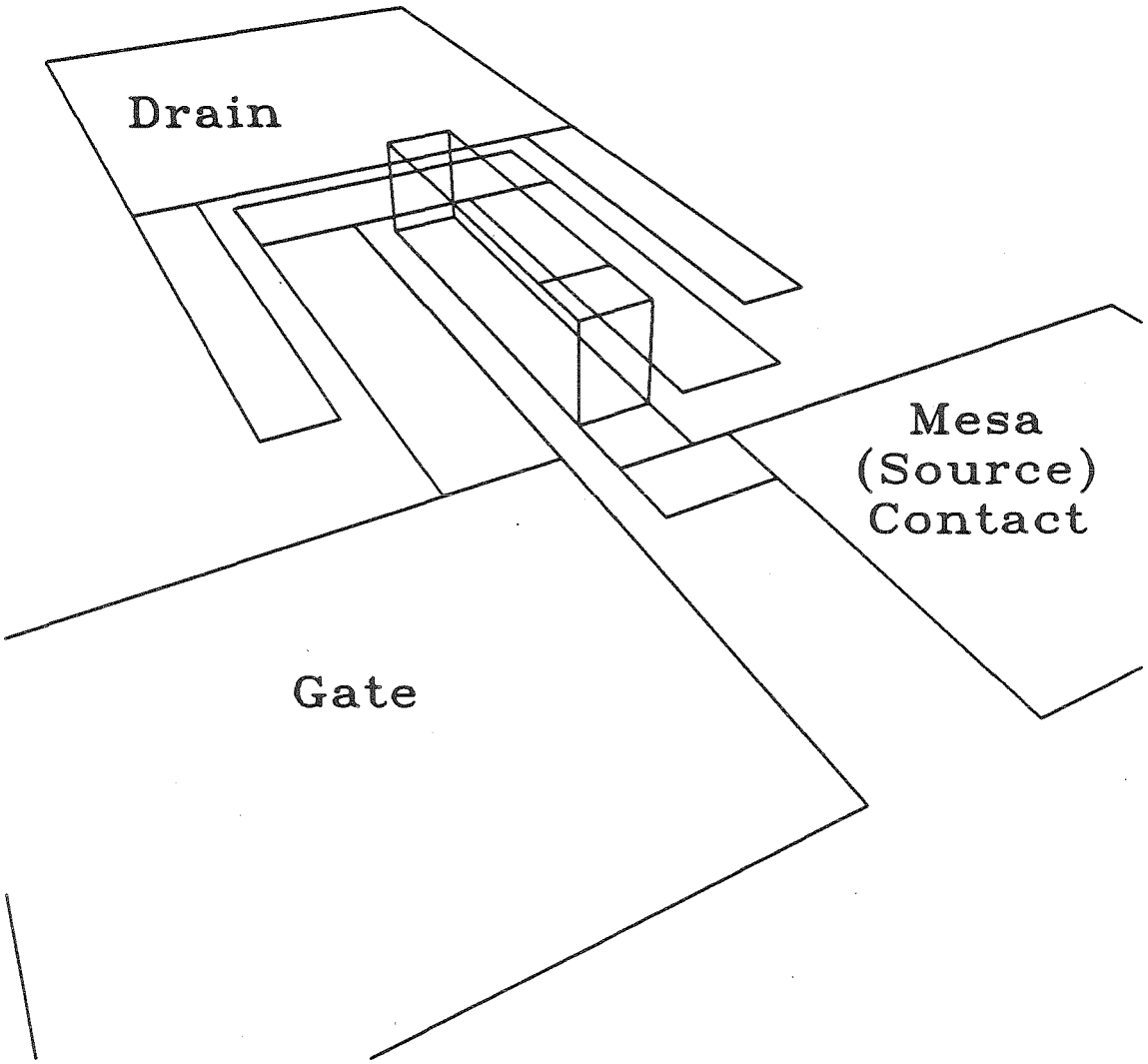

Figure 4.3: Three-dimensional view of a nonrecessed-gate DB/MESFET device. Gate length is 30 μm. The mesa is rectangular and measures roughly 20 μm $\times$ 80 μm. Recessed-gate fabrication would place the gate on a lower level from the drain.

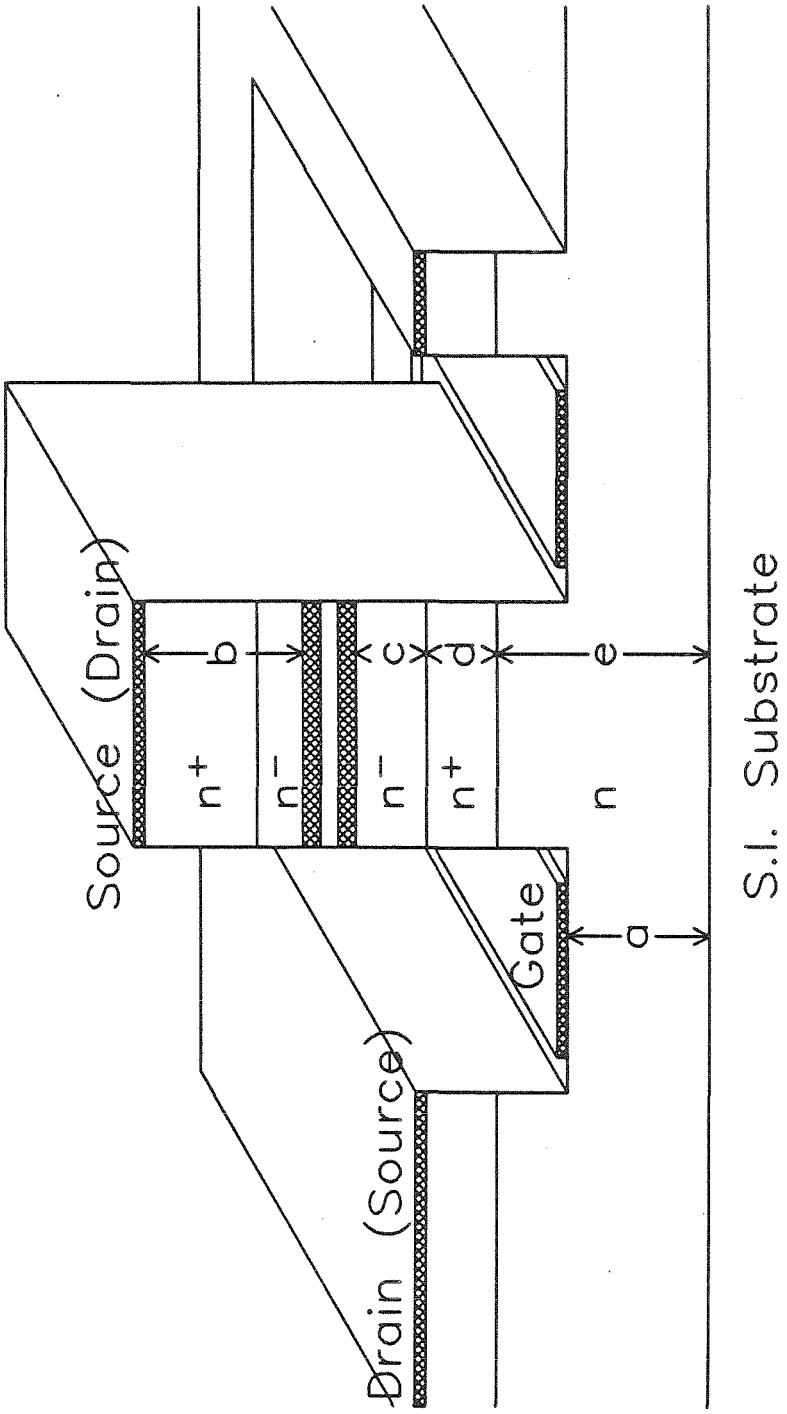

Figure 4.4: View of recessed-gate DB/MESFET, showing basic layout and wraparound drain contact. The mesa is directly wire-bonded and measures $60 \times 140\,\mu$m. The gate length is $20\,\mu$m.

Interested readers should refer to Chapter 3. Samples were cleaned in a manner previously described. The first mask was used to define rectangular mesas. These mesas were isolated with wet etching in a solution of water, phosphoric acid, and hydrogen peroxide in the volume ratio 50:3:1. The depth of this etch was monitored using a Tencor Instruments Alpha Step 200 stylus profiler. This instrument has demonstrated a capability of measuring step heights as small as 100 Å. Typical etch depth for this etch was about 4000 Å. This etch needed to be controlled to better than 2000 Åto be sure that the ohmic contact was being placed on the correct epitaxial layer (layer 'd' in Fig. 4.1). Consequently, careful statistics on the etch rate were kept. These data are illustrated in Fig. 4.5. A linear fit to the data yields an etch rate of about 800 Å/minute.

After the first etch, photoresist was removed and Au-Ge was evaporated over the entire surface of the sample. The second mask (an etch mask) was used in conjunction with an Au etch to selectively remove the Au-Ge. The photoresist and Au-Ge beneath it were then used to mask the surface during the second etch, done with a fresh batch of 50:3:1 mixture of H_2O:H_3PO_4:H_2O_2. This etch defined the channel and was also monitored. Both sets of etch data are plotted in Fig. 4.5. Following this final etch, the photoresist was removed, and the contacts were annealed.

The third mask (a lift off mask) was used to define the gate pattern. Au was evaporated onto this pattern, and a lift-off process removed unwanted Au, leaving the finished device. Devices were then photographed and mounted to TO-8 transistor headers prior to wire bonding using a West-Bond ultrasonic wire bonder.

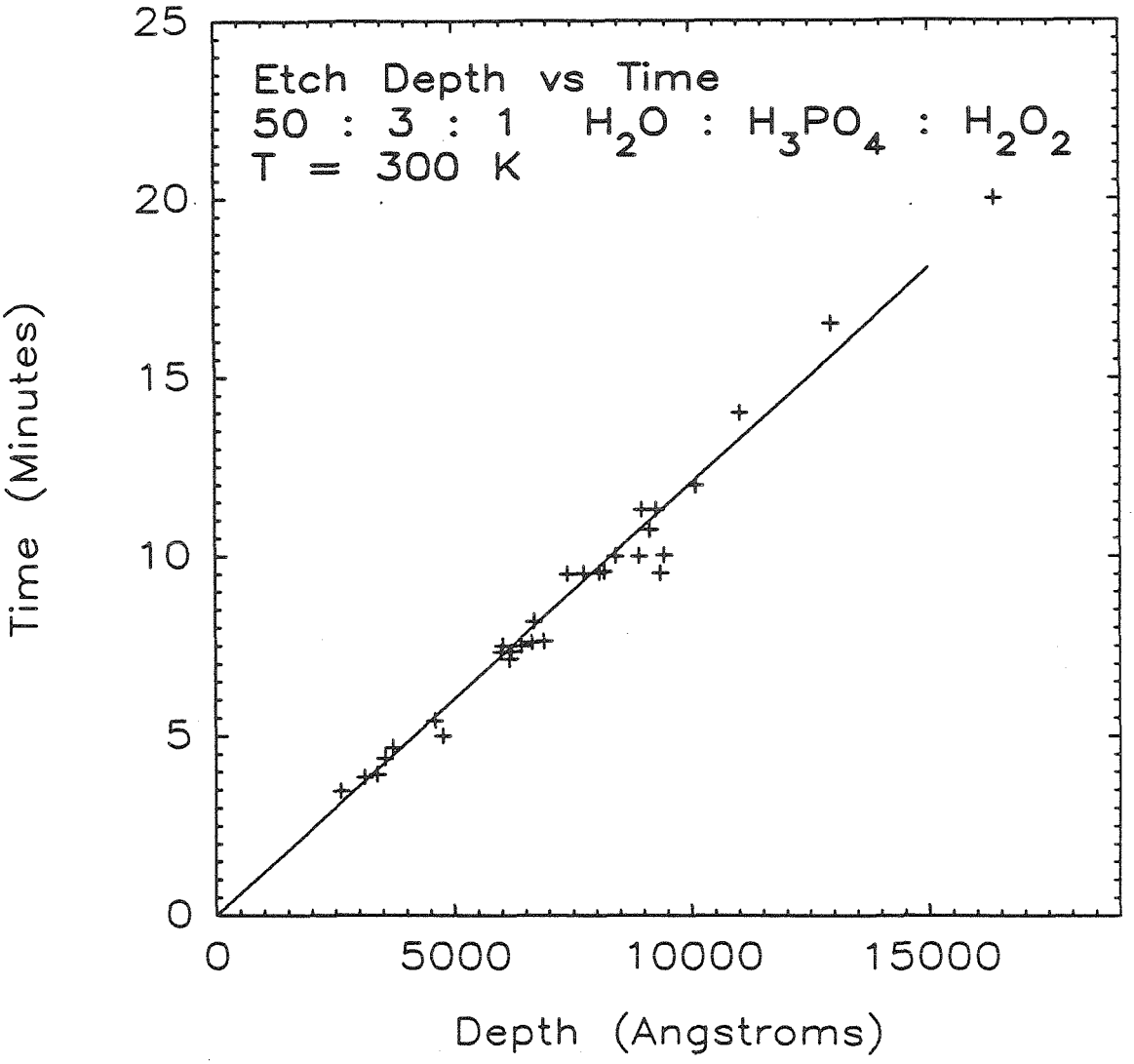

Figure 4.5: Etch-rate data for a 50:3:1 mixture of H_2O:H_3PO_4:H_2O_2. Data obtained via use of a stylus profiler. Data were obtained over many preparations throughout the entire project. A linear fit to the data is $T = 0.001217(d) - 0.1975$ where d is depth in Å and T is time in minutes.

4.5 Fundamental Results and Discussion

This section presents data for working DB/MESFETs. As mentioned, all the samples showed some sort of transistor action, and all but one showed NDR. Therefore, all the samples were working DB/MESFETs, in marked contrast to the DB/VFET project, wherein many samples did not work at all. Of course, some of the DB/MESFETs were better than others. This section presents major results for two representative samples that adequately reflect the character of the project. Results for another five samples, which are wholly consistent with the results presented here, will be given in Section 4.7. Information about all the samples may be found in tables at the end of the chapter.

Details of the experimental procedure were discussed in Chapter 3. DC measurements were made at 77 K and 300 K, using an HP4145 parameter analyzer. All data were taken in common-source mode. Significant gate current was not observed during acquisition of the presented data.

As mentioned, two bias configurations are possible for common-source operation. When the mesa containing the double barrier acts as the source of the FET, operation is said to be reverse bias. Conversely, when the mesa containing the double barrier (see Fig. 4.1) forms the drain of the FET, the device is said to be in a forward-bias configuration. The difference between the two relates to the direction of electron flow.

4.5.1 Overview

Several points are made in this section. Samples T573 and T640 are used to make these points. On a fundamental note, we wish to demonstrate that successful integration of a double barrier and a MESFET has been accomplished. Further, the types of I–V curves that can be obtained need to be explored. Finally, individual

behavior of the double barrier and the MESFET need to be explored because both influence the composite characteristic of the DB/MESFET. Sample T573 behaves most nearly as expected for a series combination of an FET and a double barrier. Theoretical comparisons were made to this sample. Sample T640 exhibits interesting behavior, demonstrating what happens when the NDR moves out of the linear region of the FET.

4.5.2 Sample T573

In Fig. 4.6 a two-terminal (floating gate) I–V curve for sample T573 is presented. NDR is exhibited in both bias directions and is highly asymmetric. The presence of a thick lightly-doped buffer layer on the back side of the double barrier (layer 'c' in Fig. 4.1) accounts for the asymmetry in the I–V. The current density at the peak of the NDR is less than 1 A/cm^2.

This sample exhibits DB/MESFET characteristics in both bias directions. In Fig. 4.7 the forward-bias common-source behavior of sample T573 is presented. Both the double barrier and the MESFET characteristics can be clearly seen. The NDR can be completely eliminated by application of sufficient gate bias. In Fig. 4.8 reverse-bias behavior is shown. These curves do not show evidence of MESFET saturation current.

Bias Asymmetries

This section discusses the differences between the reverse- and forward-bias curves for sample T573. A difference is observed because of an asymmetry in the device. This asymmetry takes the form of a thick, lightly-doped region on the back side of the double barrier. This region drops voltage in reverse bias, but is accumulated in forward bias. Thus, NDR is expanded along the voltage axis in reverse bias, much as in the DB/VFET. In forward bias, this expansion is not

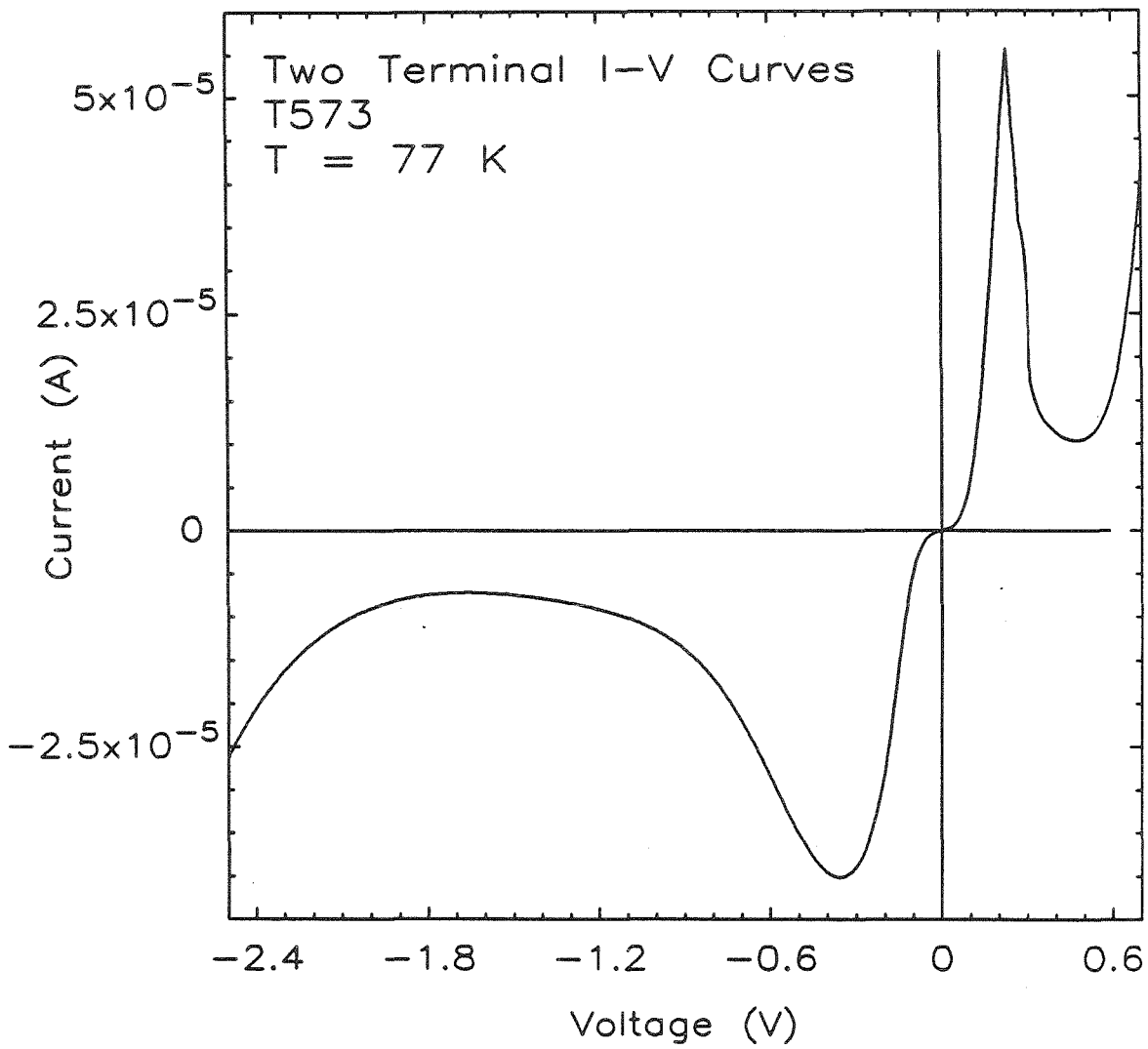

Figure 4.6: Two-terminal I–V data for sample T573. The extreme asymmetry is due to the presence of a lightly-doped layer on the back side of the double barrier. The peak-to-valley ratio is 5.6 in forward bias, and 5.7 in reverse bias.

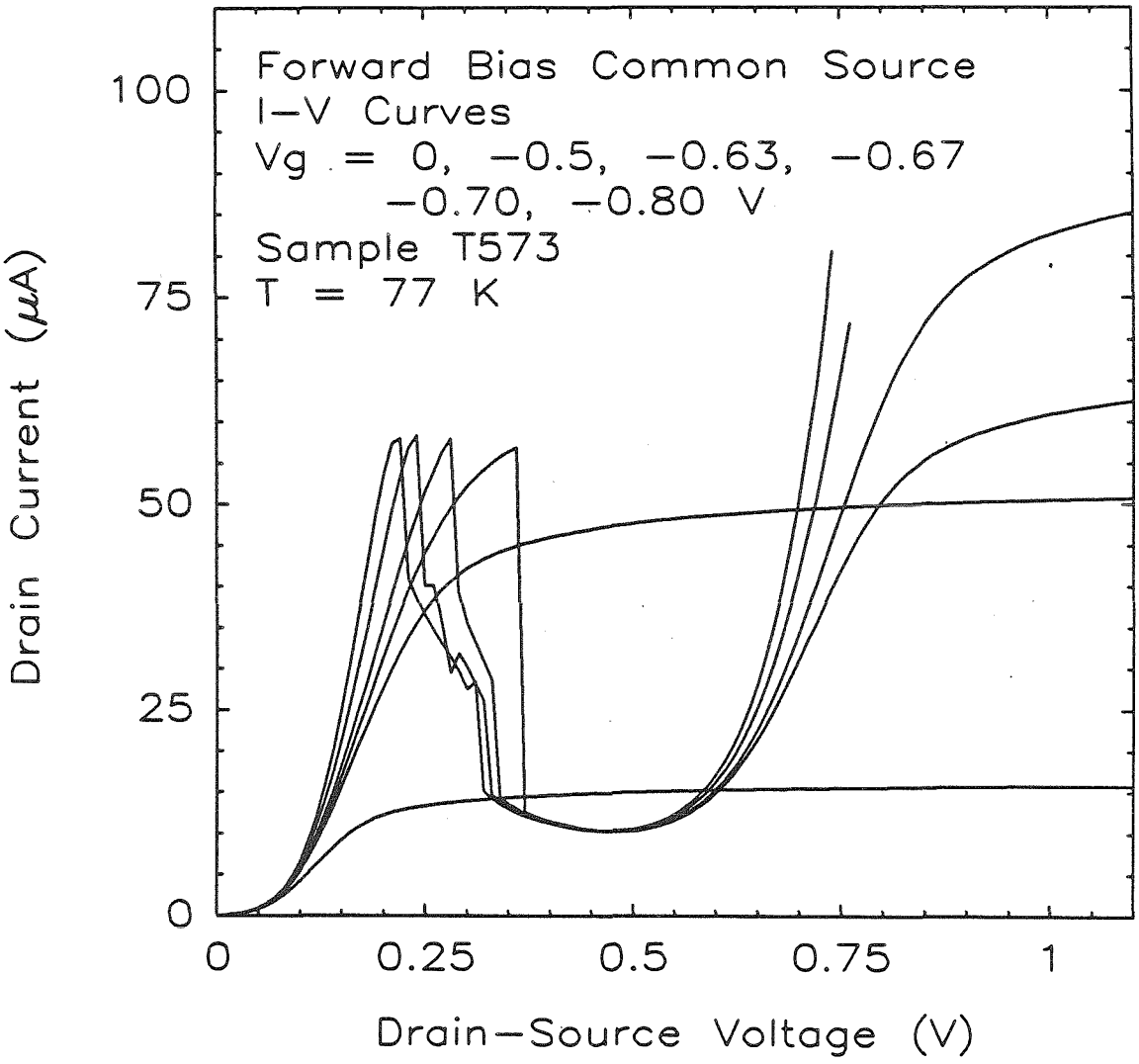

Figure 4.7: Forward-bias common-source I–V curves for T573, with V_g as a parameter. As V_g is made increasingly negative, the NDR peak-to-valley ratio decreases, and NDR is eventually eliminated.

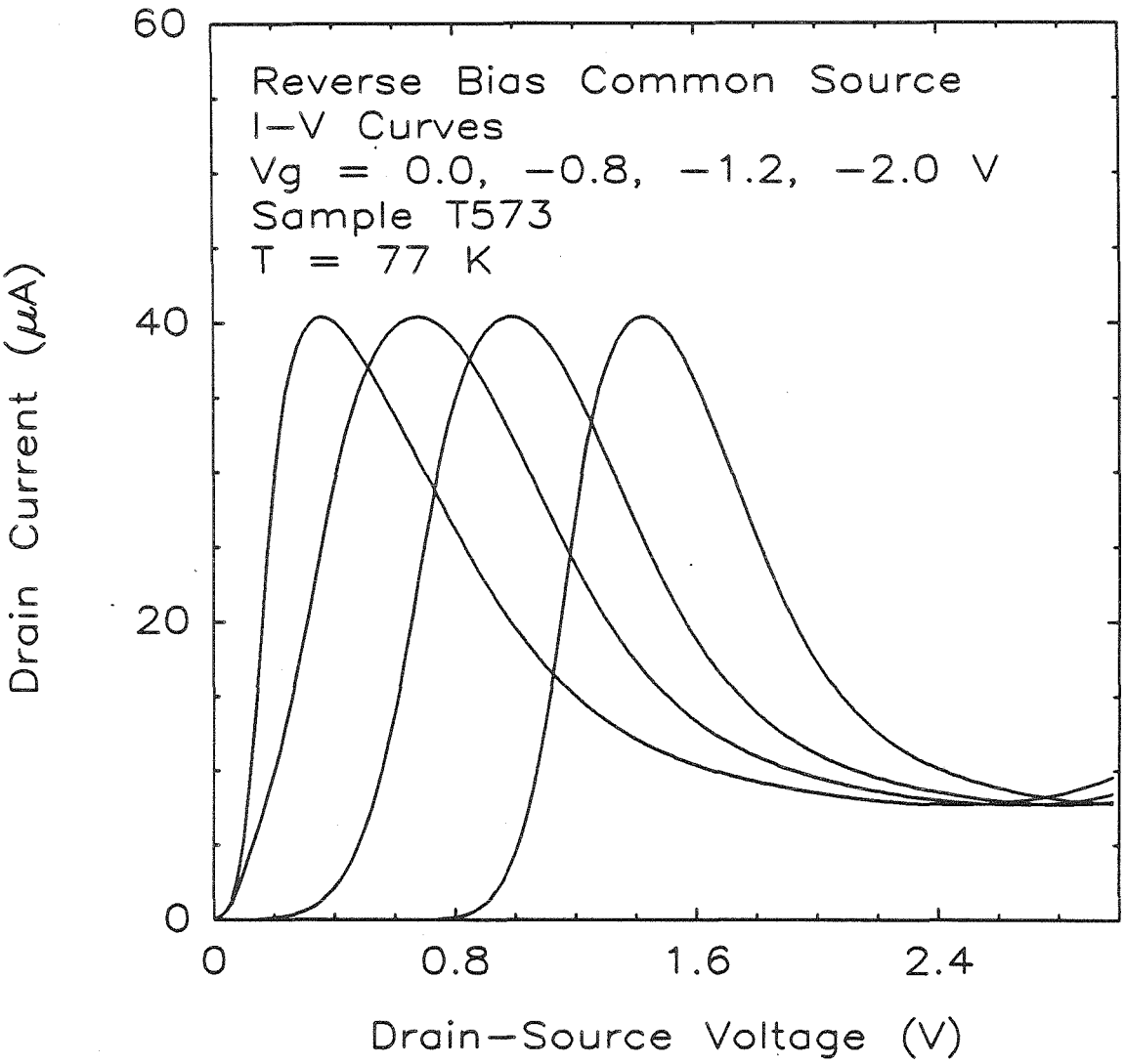

Figure 4.8: Reverse-bias common-source I–V curves for T573, with V_g as a parameter. NDR shifts to larger bias levels as V_g is made more negative.

observed. The shape of the curve differs from the DB/VFET, because the doping in layer 'c' is higher and the layer is thinner than the channel of the DB/VFET.[‡] This sort of asymmetry was seen in most of the DB/MESFET samples, but was largest in T573, because of the temperature and time of growth for this layer. The ability to tailor the asymmetry in the characteristics of the DB/MESFET might be a useful device design parameter.

Linear Region NDR Placement

The forward-bias characteristic of sample T573 (see Fig. 4.7) is very nearly a theoretically ideal DB/MESFET. For low gate biases, near zero drain voltage, the dominant resistance is clearly the double barrier. For biases in excess of about 0.6 V, the resistance of the double barrier is greatly reduced, and the FET portion of the device becomes the limiting resistance. It is not until the resistance of the MESFET becomes comparable to the double barrier that significant shifts of the NDR peak become apparent. For the illustrated case, significant shift of the NDR is seen when V_g exceeds -0.5 V. Note that NDR can be completely eliminated by application of $V_g = -0.7$ V. This could be relevant for switching applications. Via etch depth control, these voltages are adjustable.

In a broader sense the forward-bias behavior of sample T573 is exemplary of the behavior expected when the NDR lies in the linear region of the FET. This sort of behavior was seen in several other samples, some of which can be found in Section 4.7. These are the sort of samples for which modeling simulations might be expected to be most successful.

[‡] Doping is higher due to memory effects. See Chapter 3 for more information.

Dominance of Double-Barrier Resistance

What happens when the resistance of the double barrier does not become negligible? This case is well illustrated by the reverse-bias behavior of sample T573. These data are illustrated in Fig. 4.8 as well as Fig. 4.24. The lightly-doped region present in this sample results in a large double-barrier resistance over a wide bias range. The behavior is qualitatively similar to that seen in the DB/VFET, wherein NDR was not eliminated, but merely shifted along the voltage axis. Other samples, such as T548, exhibit signs of this behavior as well.

4.5.3 Sample T640

Sample T640 is very different from T573. This device was grown in an attempt to obtain higher current density operation. Higher currents were obtained by changing the dimensions of the double barrier and altering the buffer layer thickness. In fact, the top side buffer appears to play a dominant role in determining the current density. Also, the channel doping was increased. The resultant device exhibits NDR with a peak current density of about 400 A/cm^2. A two-terminal (thick channel, floating gate) I–V curve for sample T640 is shown in Fig. 4.9. NDR was observed in only one bias direction. The channel doping for this sample was between $2 \times 10^{17}\,\mathrm{cm}^{-3}$ and $3 \times 10^{17}\,\mathrm{cm}^{-3}$. The resultant device is very sensitive to channel depth, because of the depletion length scale in the channel. No three-terminal effects were seen for channel depths greater than 3000 Å. For devices having channel depths ('a' in Fig. 4.1) of 2500 Å, I–V characteristics are presented in Fig. 4.10. When the channel is thinned below 2000 Å, significant modulation of the NDR is observed. However, the resistance of the FET channel is now larger than the negative resistance at all gate-bias levels. The resulting load-line effect results in hysteresis in the characteristic.[4] These results are illustrated in Fig. 4.11. This bistability is interesting in that an operating point

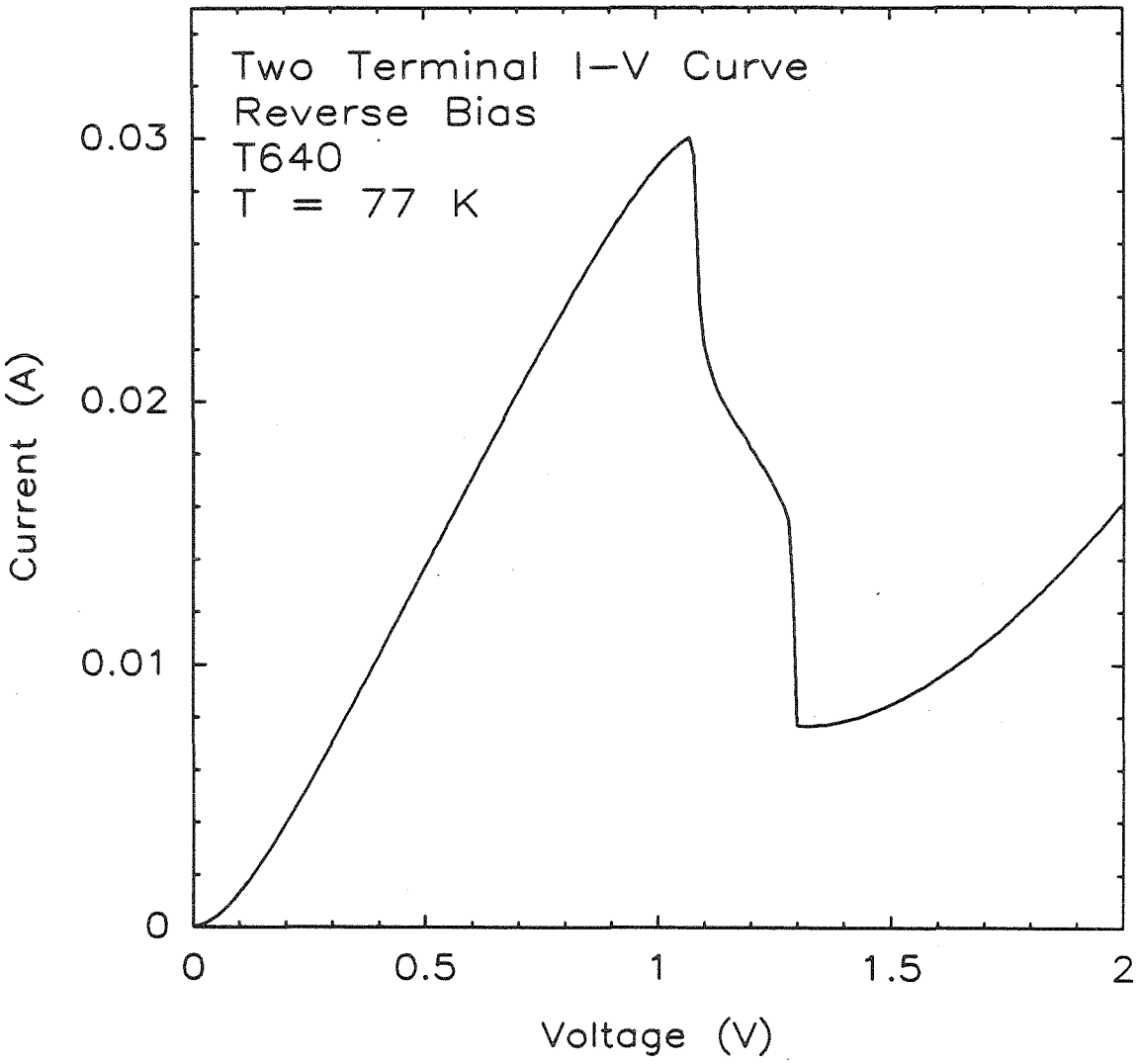

Figure 4.9: Two-terminal I–V behavior of sample T640. NDR was observed in one bias direction only.

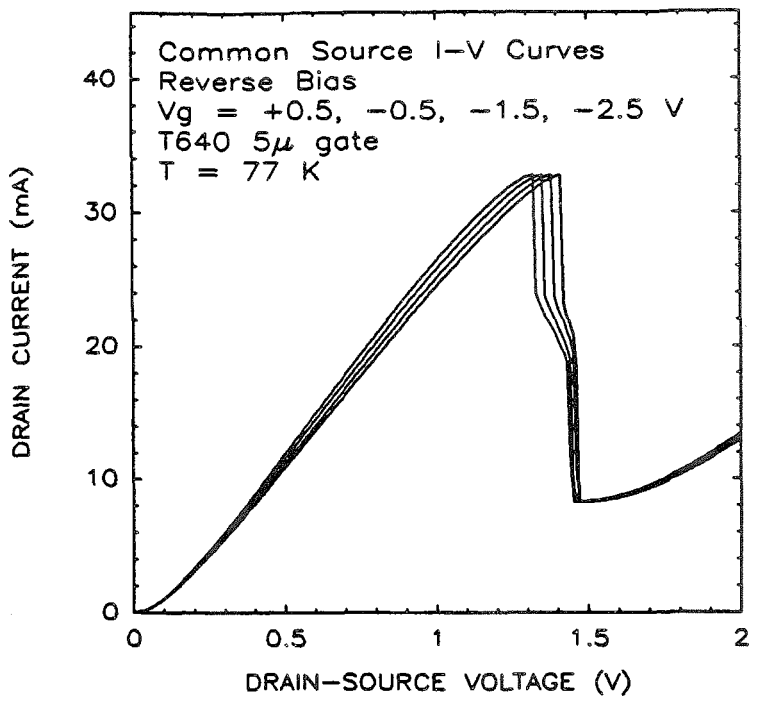

Figure 4.10: 2500 Å channel DB/MESFET characteristics for sample T640.

may be switched from one branch of the hysteresis to another, with voltage pulses to the drain *or* the gate. To further illustrate this point, we present drain current vs. gate bias plots, for a drain bias of 3.0 V. These results are shown in Fig. 4.12.

Load-Line Effects

For a 2500 Å channel, the resistance of the channel is not greater than the magnitude of the negative resistance. The three-terminal effects are small, because the channel is too thick. When the channel is thinned to less than 2000 Å, the effects become significant, and the NDR is replaced with a boxlike hysteresis region.

The effect can be understood by considering the distribution of bias across the entire device. When a particular voltage is applied, it divides between the FET

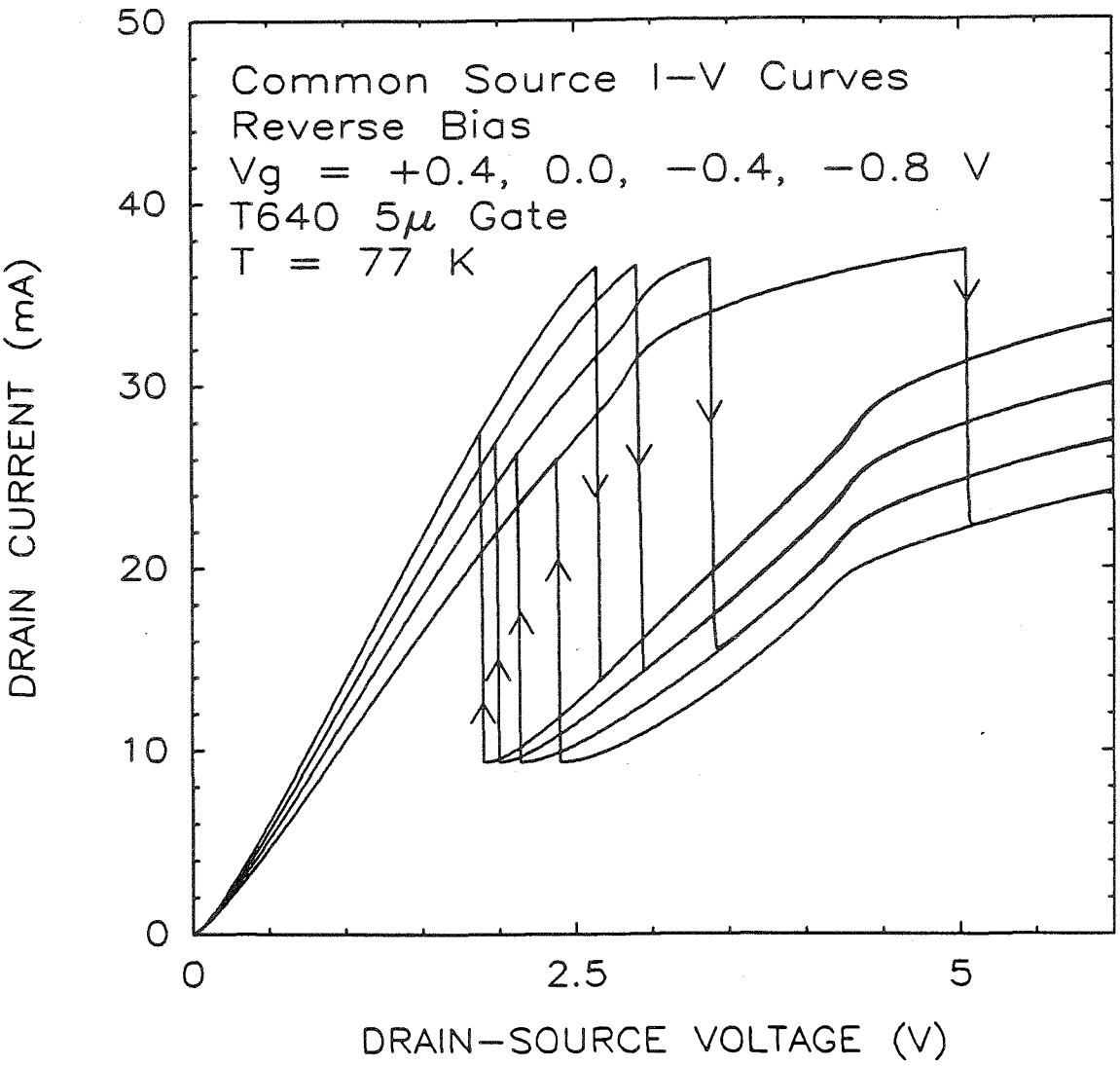

Figure 4.11: 2000 Å channel common-source reverse-bias I–V curves for sample T640. Direction of bias sweep is indicated by arrows. The hysteresis observed is due to series resistance addition. V_g is incremented in 0.4 V steps, and hysteresis increases in extent as V_g is made more negative.

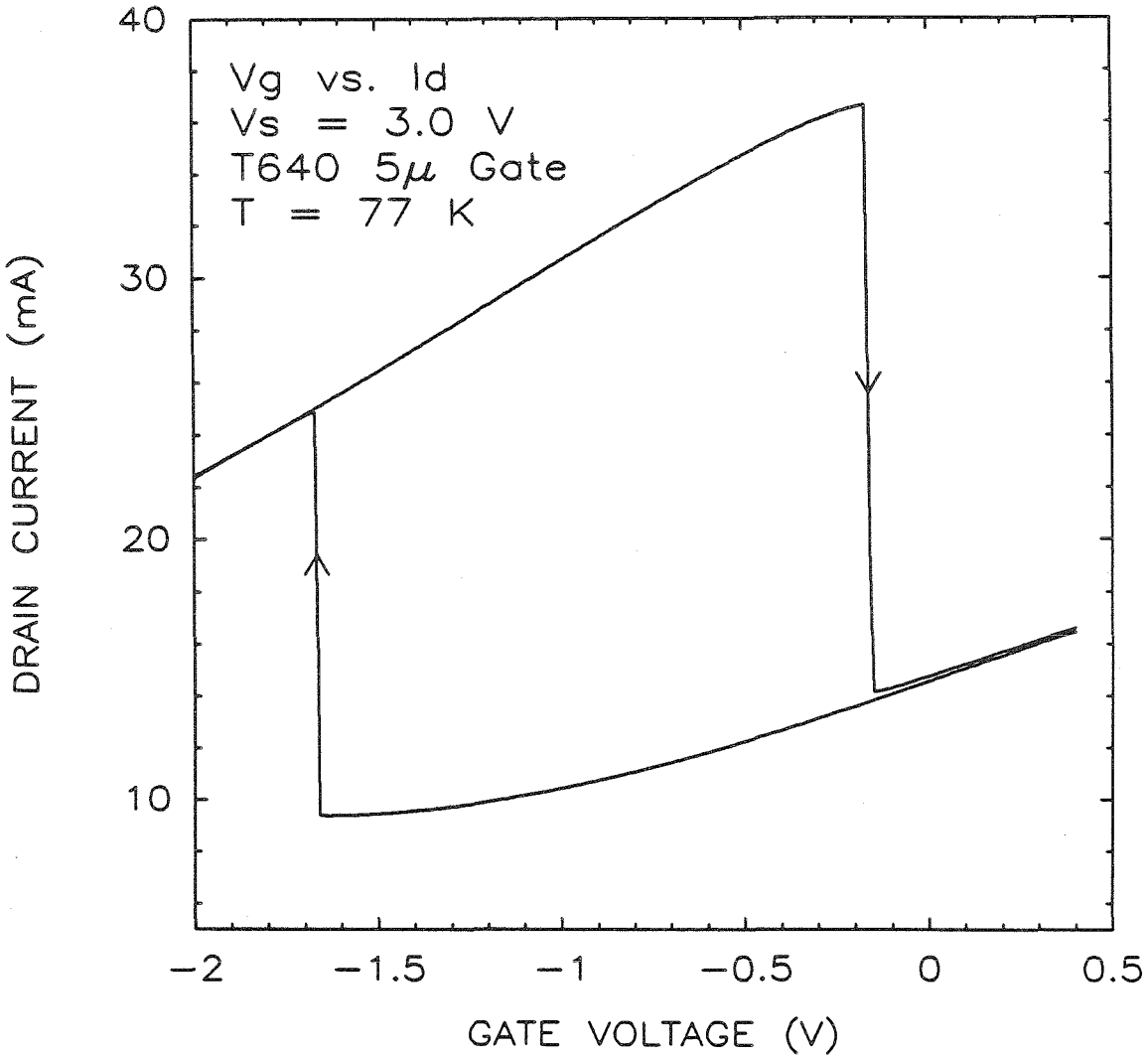

Figure 4.12: V_g versus I_d curves for the same device illustrated in Fig. 4.11, at 77 K, with $V_d = 3.0$ V. Direction of sweep is indicated by arrows. An operating point on one branch of the bistable curve may be switched to the other, via application of a gate, or drain, bias pulse.

and the double-barrier region. More current passes through the device at the peak of the NDR than at the valley. Consequently, the voltage across the channel of the FET at the peak of the NDR is larger than it is at the valley of the NDR, where the current is smaller. When the difference between these two voltages becomes larger than the difference between the peak and valley voltages of the NDR, a bistability develops. A condition for bistability can be written:

$$V_{FET}^{p} + V_{DB}^{p} > V_{FET}^{v} + V_{DB}^{v} \ , \tag{4.1}$$

where $V_{FET}^{p,v}$ is the voltage across the FET portion of the device at the peak or the valley, with similar quantities defined for the double barrier. Writing $V_{FET}^{p,v} = I^{p,v} R_{FET}$ leads to a simple expression for the critical resistance:

$$R_{FET} = \Delta V_{DB} / \Delta I^{p,v} = R_{NDR} \ , \tag{4.2}$$

where R_{NDR} is the magnitude of the negative resistance. This expression simply states that the resistance in series with the NDR must be less than the magnitude of the NDR value, or else the NDR will not be seen. This effect has been seen in tunnel diodes.[4]

Another way of looking at the same phenomena is to consider the load-line of the FET channel on the two-terminal I–V curve of the double barrier. For a steep load-line there is only one intersection of the load-line with the device characteristic. When the load-line becomes sufficiently shallow (defined by Eq. 4.2), multiple intersections with the load-line become possible. The particular state observed depends upon the history of the device. When the load resistor and the NDR are considered as a single device, the curves shown in Fig. 4.11 are obtained.

If the resistance of the channel could be decreased, this hysteresis might be eliminated. The resistance of the channel can be expressed as $\rho L/A$, where ρ is the resistivity of the material, L is the gate length, and A is the cross section. By decreasing the gate length, the channel resistance can be decreased. We were

therefore motivated to make 5 μm gate-length devices. These devices continued to exhibit hysteresis. Preparations having increased gate periphery and decreased gate length might succeed in eliminating the hysteresis, but it is probably easier to grow a different sample with slightly lower channel doping.

This section describes what happens when the series resistance of the FET channel impacts the NDR characteristic itself, effectively moving the NDR from the linear region to the saturation region of the FET. The ability to control the onset of bistability could be another useful device design parameter.

4.6 Simple Models

This section compares experiment to well-known theoretical models of the MESFET. Four things are done. First, a series resistance addition is considered. Then, a simple linear MESFET model is compared to T573 experimental results. An experimental test of the theory was performed by combining the I–V curves for separate preparations of the FET and the double barrier. Finally, velocity saturation effects and a two-region model are described.

Linear Resistance

The first approximation to the DB/MESFET is a simple series combination of the double barrier and a resistor. Sample T573 is well described in forward bias by this simple model. A FORTRAN program that added a constant series resistance to a two-terminal I–V of T573 was written. The results of this program are presented in Fig. 4.13. As can be seen, linear resistance addition is a good first-order approximation to the actual experimental data (see Fig. 4.7). This model is not successful for other samples. See, for example, Section 4.7.3.

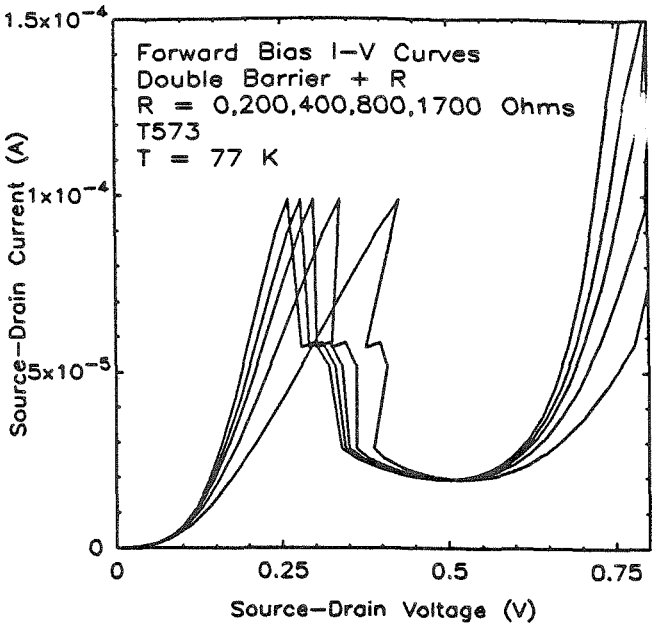

Figure 4.13: Linear-resistance addition model of DB/MESFET applied to sample T573.

Simple Linear Model

The 'long' channel, or simple linear model, is a basic MESFET model.[2] It is valid for cases in which the electron velocity in the channel of the MESFET is not saturated. The model is generally used for devices with gate lengths greater than a few microns. The 20 μm gates of our DB/MESFETs should fall into this category.

Modeling was done for two samples, T573 and T640. A fair comparison can be made by removing the double barrier from the sample by etching to layer 'c' in Fig. 4.1. Recessed-gate MESFETs were then fabricated as outlined previously. A comparison between these devices and the simple linear model can be made. A program to calculate MESFET characteristics was written, using the simple linear model. The input parameters are the gate length, the gate width, the channel depth and doping, and the mobility. Using experimentally measured values for

these parameters, and assuming a mobility of 8000 $cm^2/(Vsec)$ at 77 K, MESFET characteristics were calculated. The results are presented in Fig. 4.15 and can be compared to the experimental results presented in Fig. 4.14.

The theoretical curve agrees with the experimental data to within a factor of 2. Adjustment of parameters such as mobility, gate depth and doping, and gate width make it possible to match the data more precisely, but this is not the issue. The point is that the simple linear model is capable of modeling the experimental results adequately.

Combining the experimental FET-only data illustrated in Fig. 4.14 with a two-terminal I–V curve for the double barrier should yield data consistent with the experimental data for the complete DB/MESFET. These data are illustrated in Fig. 4.16.

Sample T640 is very different from T573 in doping and channel depth. The simple linear model was also applied to this sample for 5 μm gate lengths. A separate FET preparation was not done for this device. Thus, some discrepancy in voltage might be expected due to the added resistance of the double-barrier region. The saturated current for T640 in either bias direction at 300 K is between 30 and 40 mA, somewhat lower than that observed in the calculation.

Two-Region Model

A two-region model of the MESFET could also be applied.[2] This model assumes that a saturated velocity region exists under the gate near the drain. The model calculates the point at which the electric field is large enough to create velocity saturation, and assumes constant velocity transport beyond that point. The resultant curves show pinchoff at lower currents and lower voltages than in the simple linear model. Calculations for both models, taken with identical input parameters, illustrate the effect. Results are presented in Figs. 4.17 and 4.18.

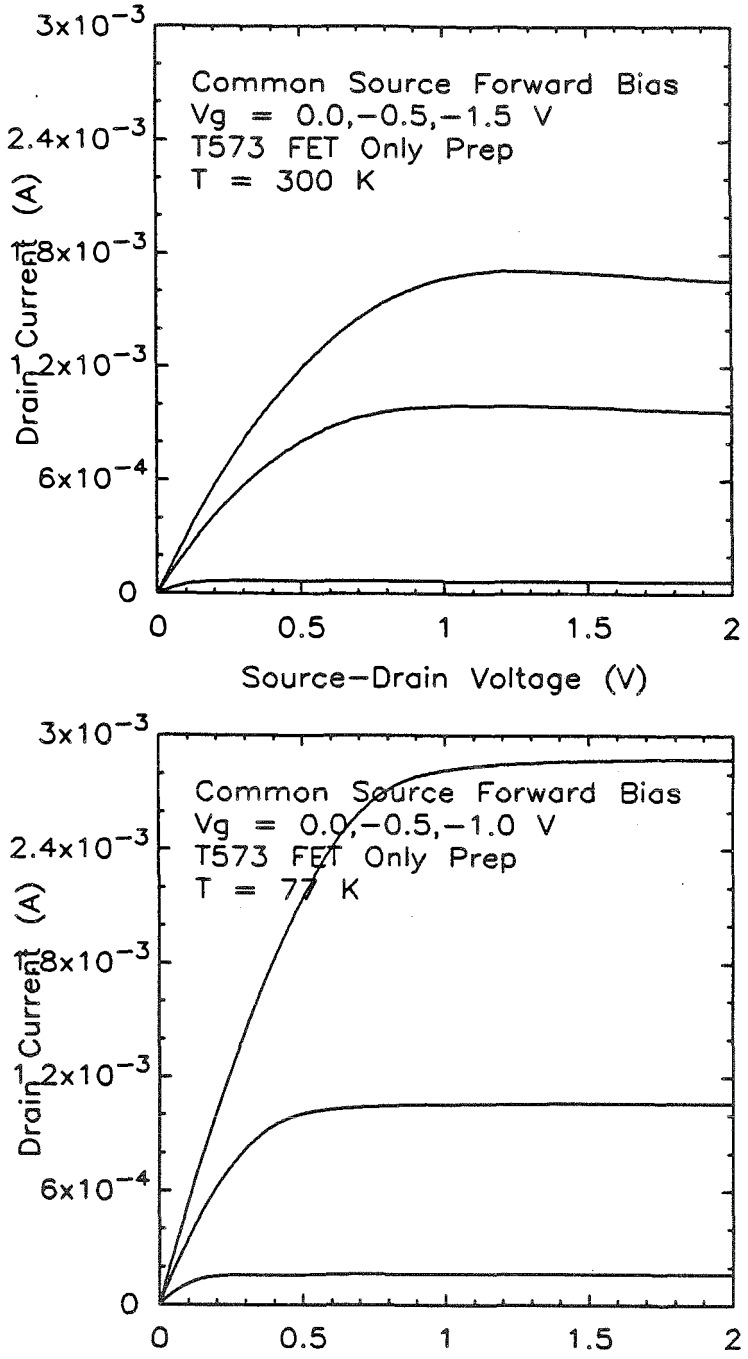

Figure 4.14: MESFET characteristics for a preparation of T573 in which the double barrier has been removed. Data obtained at 77 and 300 K. Note the increase in saturation current with decreasing temperature, indicating a rise in mobility with decreasing temperature.

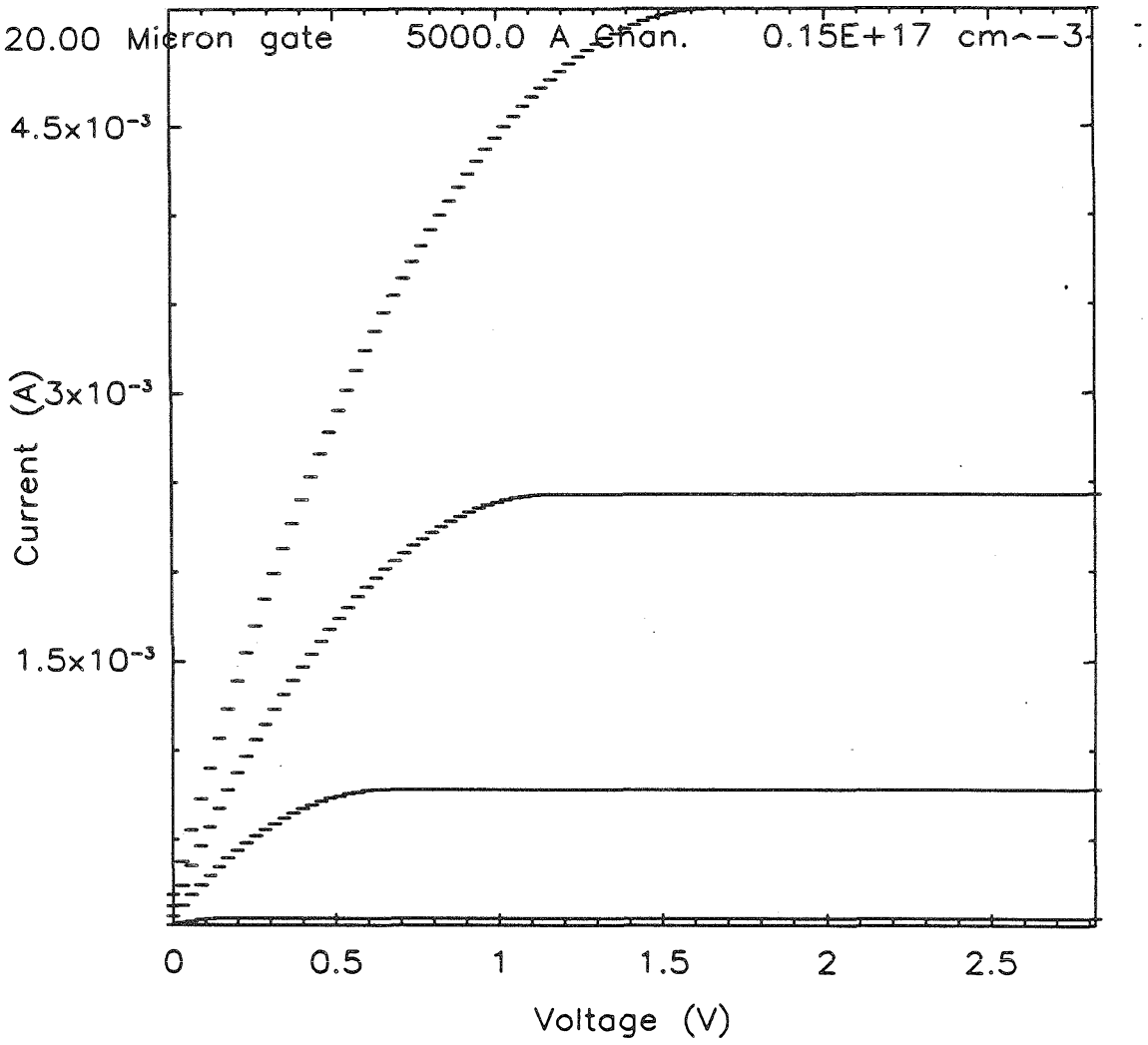

Figure 4.15: Calculated MESFET characteristics for sample T573, assuming a 5000 Å channel, 20 μm gate length, 8000 $cm^2/(Vsec)$ mobility, and $1.5 \times 10^{16}\,cm^{-3}$ channel doping. Gate voltages of 0, -0.5, -1.0, and -1.5 V are shown. Agreement with experimental data is to within a factor of 2.

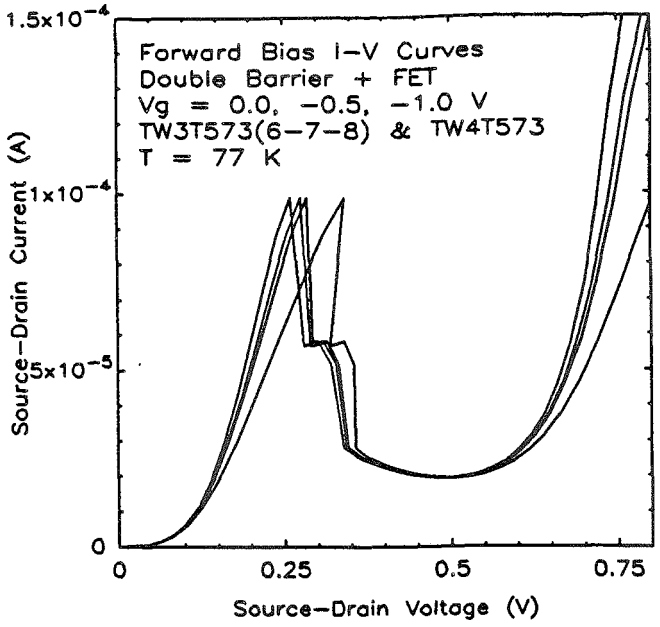

Figure 4.16: Series combination of two-terminal NDR characteristic with FET characteristics for T573.

Actual device behavior is more like the linear model than the two-region model in form, but is more like the two-region model in current scale. It should be noted that the behavior of GaAs MESFETs can be more complicated than the two-region model, due to the formation of a dipole layer underneath the gate.[5]

A scaling parameter z provides a measure of the importance of saturated velocity effects:[2]

$$z = \frac{\mu V_p}{v_s L} \tag{4.3}$$

where μ is the mobility, V_p is the pinchoff voltage, v_s is the saturation velocity, and L is the channel length. 'z' is just the ratio between the velocity predicted by constant mobility (at the maximum field V_p/L) , and the saturation velocity. Assuming a saturation velocity of 8×10^6 cm/s and a pinchoff voltage of 4 V, a gate length of 5 μm yields z values of between 2 and 10; for mobilities of 2000 to 10000 $cm^2/(Vsec)$. Typical microwave MESFETs have z values between 2 and 10,

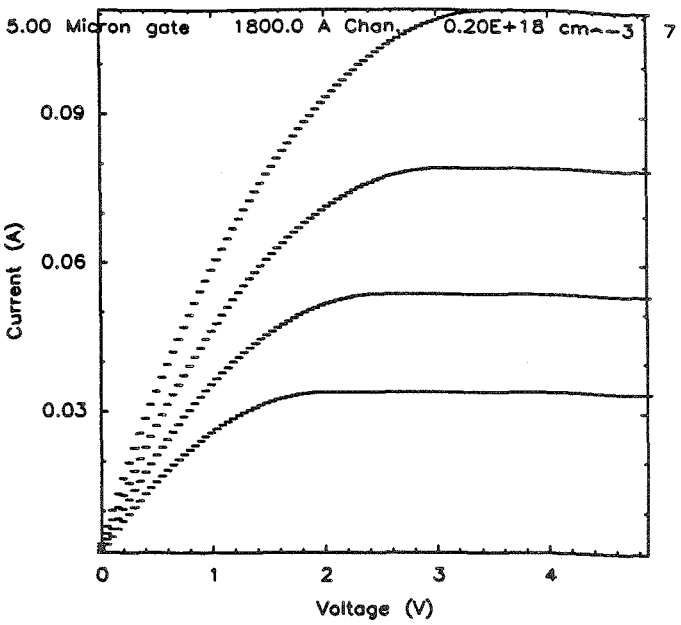

Figure 4.17: Linear model MESFET calculation for 5 μm gate device utilizing T640 sample parameters. Mobility was assumed to be 8000 $cm^2/(Vsec)$ in the channel. Gate voltages of 0, -0.5, -1.0, and -1.5 V are illustrated.

indicating that saturated velocity effects might be important for our devices.

4.7 Supplementary Results

This section presents extra results, not needed to understand the device or to make the major points of this chapter. They are included for completeness and to provide interested parties with a catalog of varied I–V characteristics.

4.7.1 Samples T424, T425, T498, and T499

These samples suffered from photosensitivity. Two of the samples were not of the recessed-gate type. Of particular concern was the presence of persistent voltage effects when data were taken in darkness. These effects were manifest by a

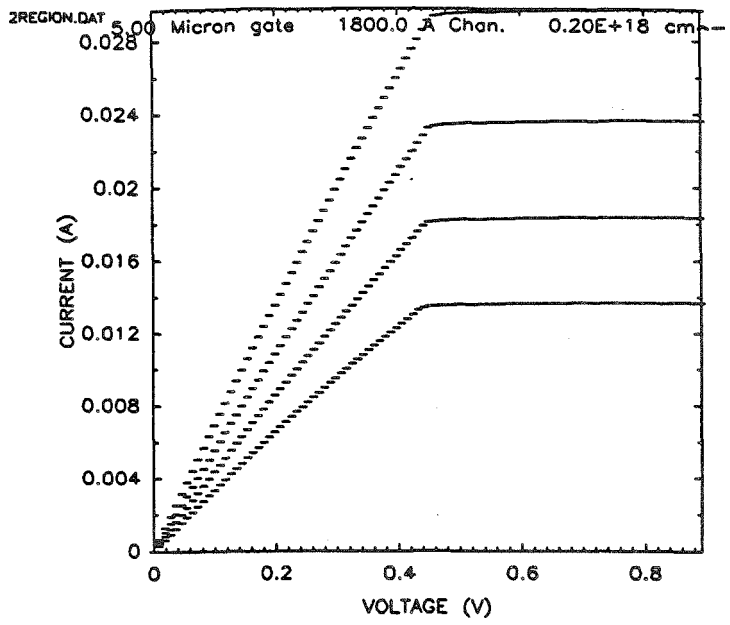

Figure 4.18: Two-region model MESFET calculation for 5 μm gate device utilizing T640 sample parameters. Mobility was assumed to be 8000 $cm^2/(Vsec)$ in the channel. Gate voltages of 0,-0.5, -1.0, and -1.5 V are illustrated.

change in the resistance of the sample after exposure to large voltages. This resistance was a long term behavior, with light exposure required to return resistance to the original values. These samples exhibited history-dependent DB/MESFET characteristics, which are not presented here.

4.7.2 Sample T548

Illustrated in Fig. 4.19 are two-terminal I–V data for sample T548. Clearly, NDR is more pronounced in reverse bias. The appropriate bias direction for this DB/MESFET is reverse bias. These data are illustrated in Fig. 4.20.

This sample is included in the chapter because it is the only sample shown in which the channel was *not* doped with the pulsed technique discussed in Section 4.3. Therefore, one can compare these data with those obtained in pulsed

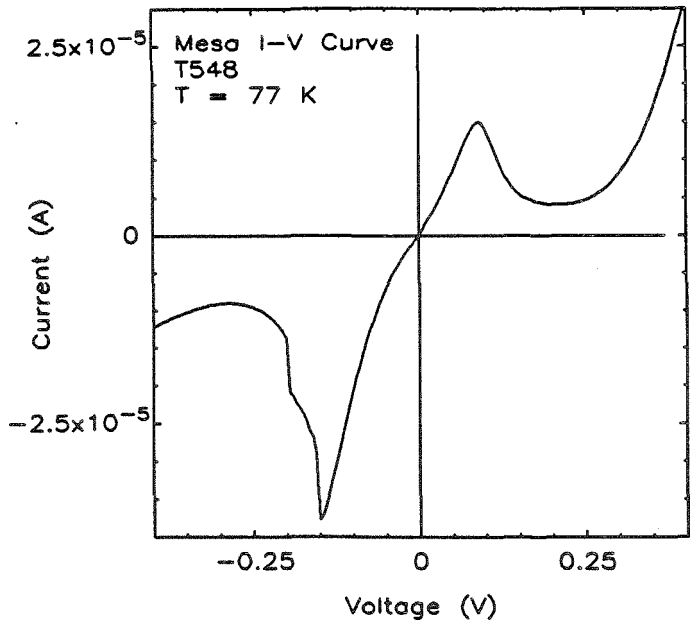

Figure 4.19: Two-terminal I–V behavior of T548. Peak-to-valley ratio is 4.2 in reverse bias.

doping growths. This sample was light sensitive. The channel doping was in the low 10^{16} range. Forward-bias operation was observed and was similar to the data illustrated for sample T573.

4.7.3 Sample T549

This sample illustrates a case of pulsed doping, to a level in the low $10^{16}\,\mathrm{cm}^{-3}$ range. Unfortunately, this sample also has light-sensitive I–V and C–V behavior. The source of this behavior was localized to the channel region and may be associated with deep levels or with the $Al_xGa_{1-x}As$ buffer layer. A peak-to-valley current ratio of ~ 7 is seen in reverse bias. Noticeably lower current was drawn in reverse bias, as compared to forward bias, similar to sample T573. The higher temperature at which the buffer layers were grown in this sample accounts for the higher current drawn here as compared to T573.

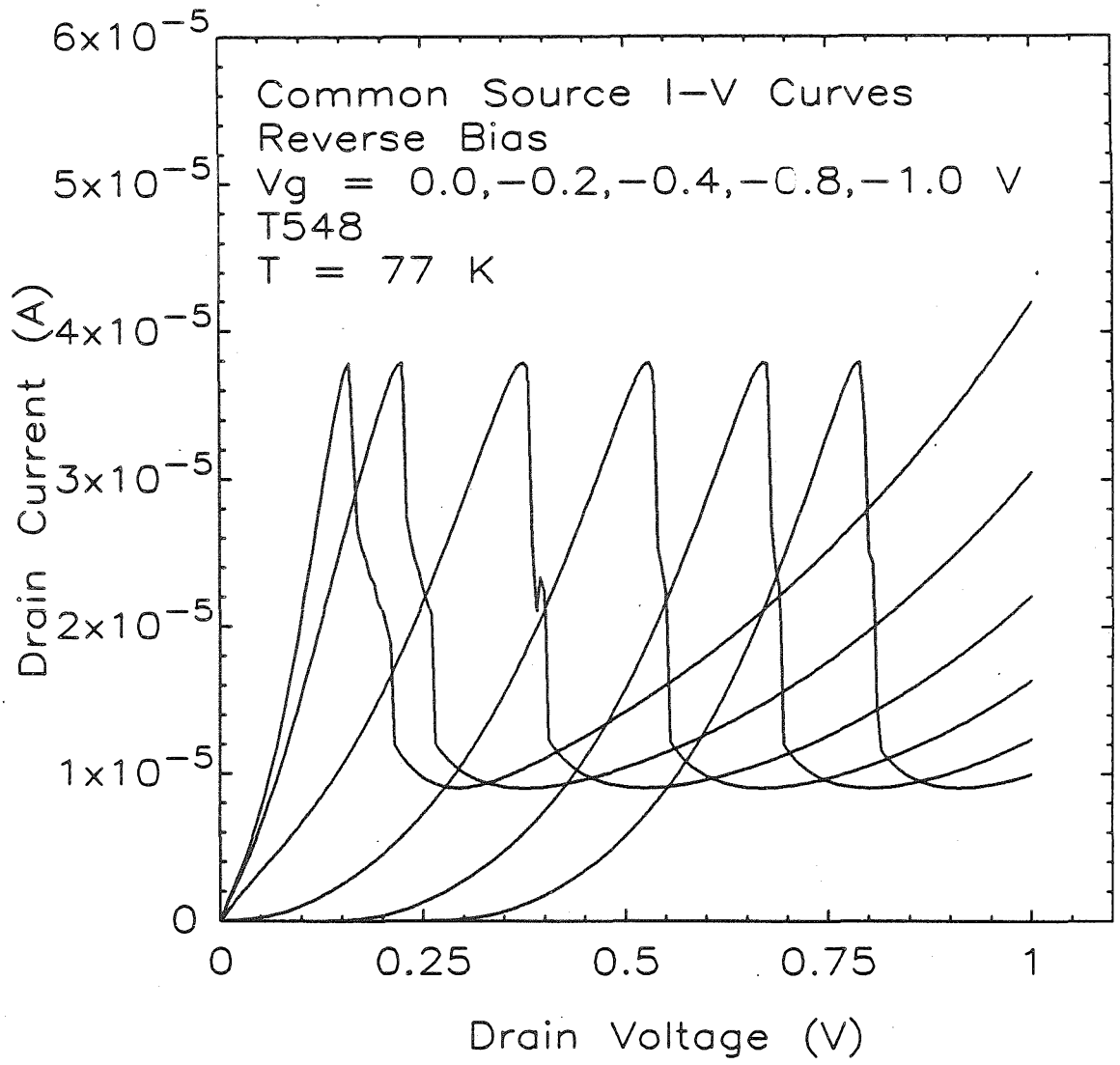

Figure 4.20: Reverse-bias common-source behavior of sample T548 obtained at 77 K, with gate bias (V_g) as a parameter. The leftmost curve was taken with $V_g = 0$, and the position of the NDR shifts outward with increasing V_g.

The reverse-bias FET behavior of this sample is interesting. Fig. 4.21 presents these data. A large degree of NDR modulation is possible, and the saturation curves of the FET are apparent at large gate bias levels. The peak-to-valley ratio is large, and considerable modulation of the position of the peak could be observed. Since light-sensitive behavior was observed, room light data are illustrated. These data could be obtained reproducibly. Data taken in darkness showed considerable variability, dependent on the history of the device.

The basic concept of the DB/MESFET is that the variable series resistance provided by the FET gate would modulate the position of the NDR. As a first-order approximation, linear resistance addition is fairly good. However, for sample T549, something more than a simple addition of a linear series resistance is taking place. This can be demonstrated by an attempt to model the characteristics of Fig. 4.21 with the addition of a constant resistance to the $V_g = 0$ curve. It is possible to match the peak of the $V_g = -0.4$ V curve by adding a resistance of $2450\,\Omega$ to the $V_g = +0.4$ V curve, but the rest of the curve is not well matched. Data are illustrated in Fig. 4.22. These results differ from the results obtained for sample T573, wherein a linear resistance model is successful.

4.7.4 Sample T550

This sample was grown without the $Al_xGa_{1-x}As$ buffer layer present in all the other samples. The characteristics of the sample suffer somewhat, probably because of the lack of a buffer layer. Three-terminal behavior was observed in this sample, but it was not of the same magnitude as seen in the previous two samples. This sample was the first to show negligible light sensitivity. No characteristics are presented for this sample.

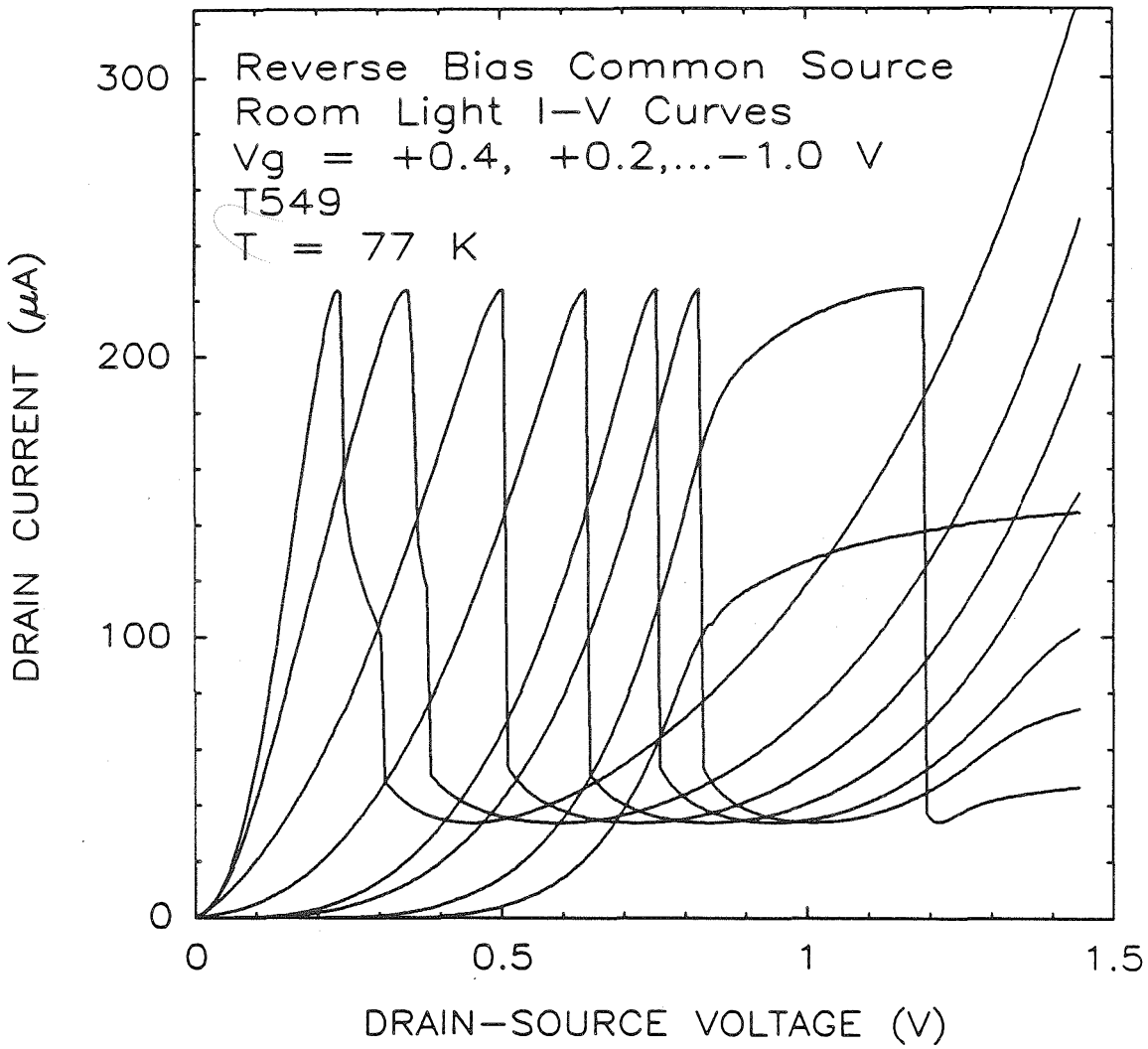

Figure 4.21: Reverse-bias common-source characteristics for Sample T549. Data taken under room light conditions, at 77 K. Gate bias shifts the position of the NDR to larger voltage levels.

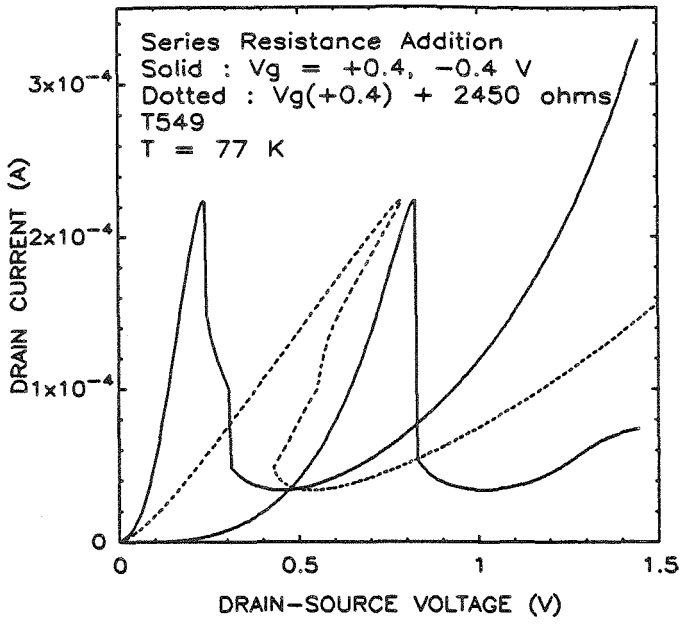

Figure 4.22: The dotted curve is obtained by addition of a constant series resistance of 2450 Ω to the left-hand I–V curve. It clearly fails to model the characteristics adequately.

4.7.5 Sample T573

A lot of data was taken on this sample, because it is so well behaved. Rather than present all of it in Section 4.5, some data have been reserved for this section. Included here are large scale I–V curves for the DB/MESFET, which show the saturation characteristics of the MESFET portion of the device. These results can be compared to the FET-only preparations illustrated previously.

The complete MESFET equivalent circuit parameters for the FET section of the DB/MESFET were not calculated, because the construction of a state-of-the-art MESFET was not the goal of this study. However, the transconductance was determined. The transconductance of the forward-bias device can be determined by examining the drain current as a function of gate bias, at a fixed drain bias in

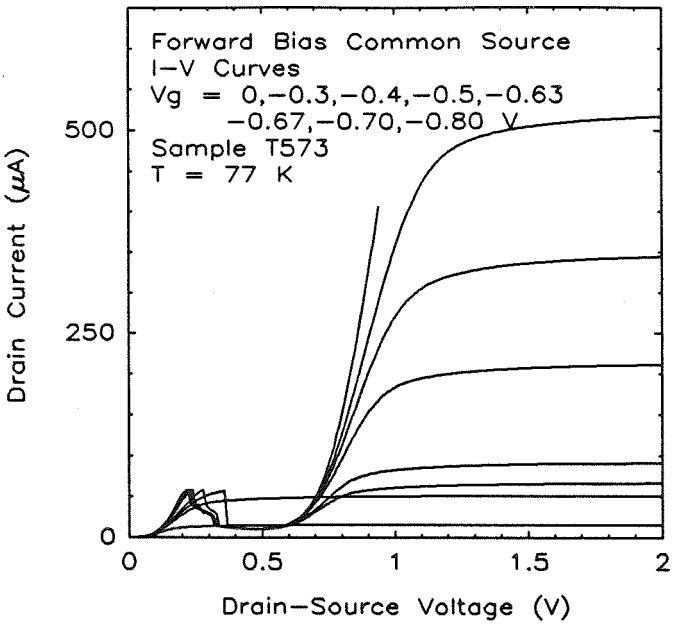

Figure 4.23: Larger-scale forward-bias behavior of DB/MESFET. MESFET saturation characteristics can be seen

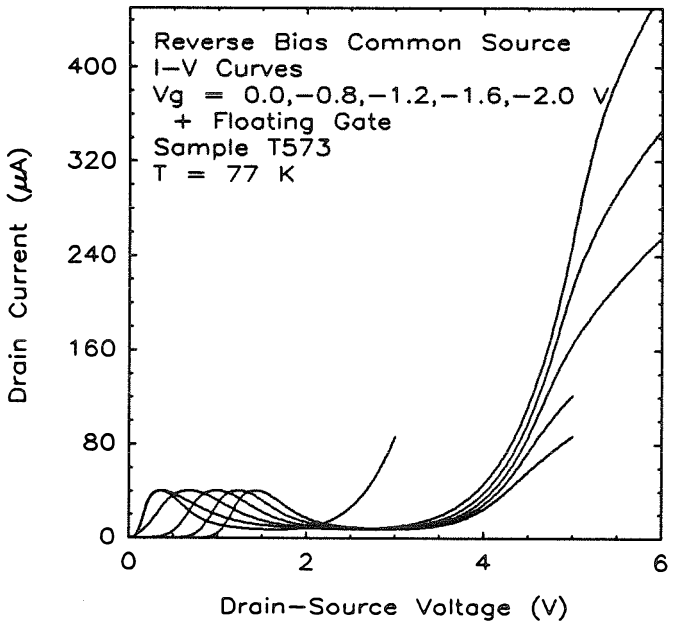

Figure 4.24: Larger-scale reverse-bias behavior of T573.

the saturation regime. The slope of this line is the transconductance (g_m) of the device. It is important in determining the gain of the transistor.[2] g_m for a device fabricated from sample T573 is plotted in Fig. 4.25. Dividing by the gate width (periphery) yields a normalized value, which can be compared to other results. A value of about 3 mS was obtained near $V_g = 0$ for a gate length of 20 μm. For an assumed gate periphery of 340 μm, one obtains a normalized value of 8.8 mS/mm. The channel mobility may be estimated from the drain voltage (V_{knee}) at which the drain current saturates, at zero gate bias. The current at this point is given by both $j = nev_{sat}$ and $j = ne\mu V_{knee}/L$.[6] Therefore $\mu = Lv_{sat}/V_{knee}$. A knee voltage of 1.5 V and a saturation velocity of 8×10^6 cm/sec yields $\mu = 10,000 cm^2/Vsec$. One may then calculate the expected g_m from

$$g_m = \frac{qN_d a \mu Z}{L}\left(1 - \sqrt{\frac{V_g + V_{bi}}{V_p}}\right), \tag{4.4}$$

where parameters have their standard definitions.[2] One obtains

$$g_m = 0.02\left(1 - \sqrt{\frac{V_g + V_{bi}}{V_p}}\right) S. \tag{4.5}$$

Assuming a pinchoff voltage of about 2 V, we obtain $g_m = 6$ mS. This agrees with the measured result of $g_m = 3$ mS to a factor of 2, which we take to be satisfactory agreement with theory.

4.7.6 Sample T624

This sample was grown in an effort to obtain increased current density operation. It is intermediate between the low values of T573 and the higher values of T640. Therefore, it further demonstrates the important role that small modifications in the double barrier can have on the DB/MESFET. The device characteristics are not as attractive as for other devices, because the double-barrier peak-to-valley ratio is not large. Additionally, thinner channel devices could be expected to exhibit the hysteresis behavior seen in T640.

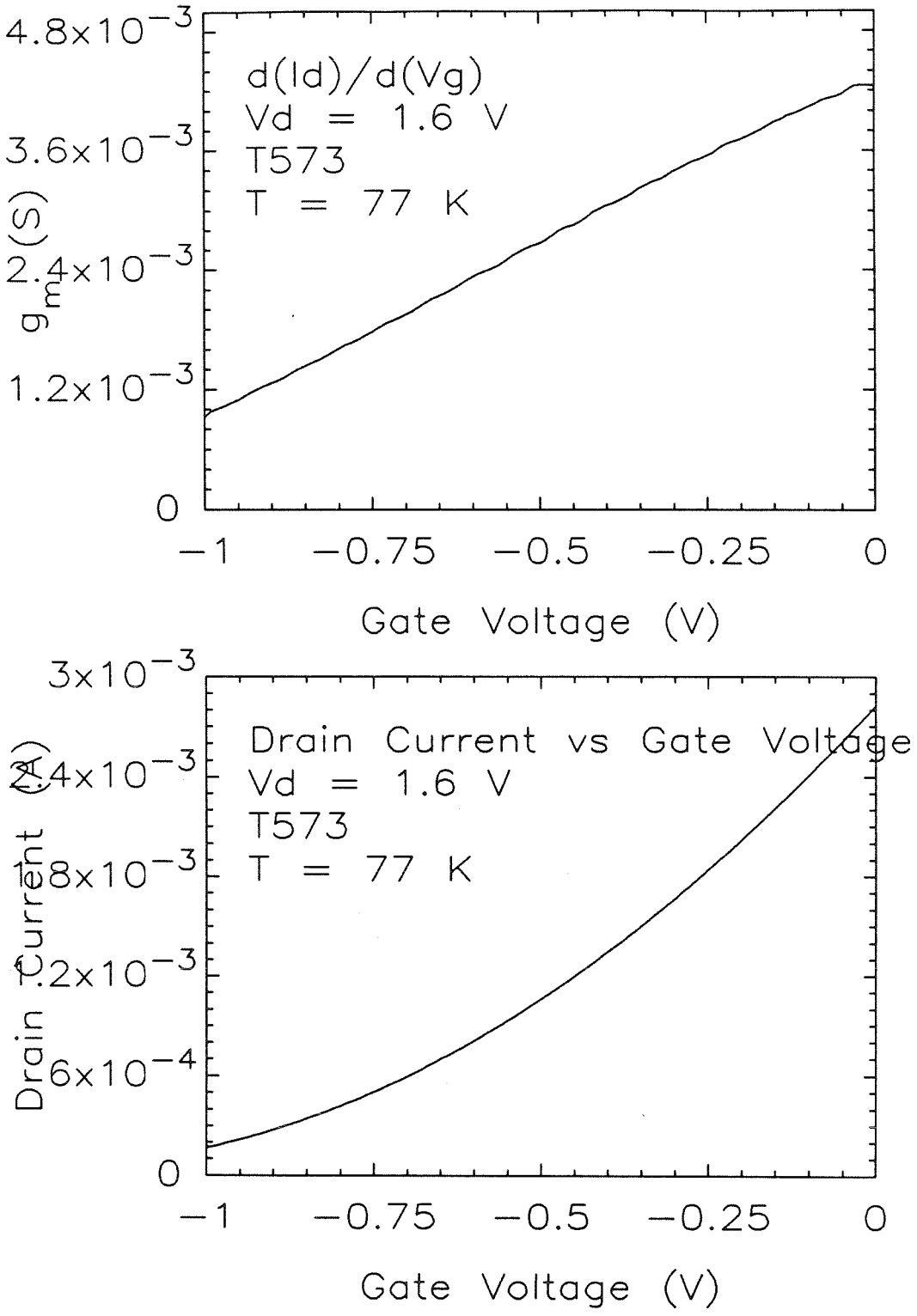

Figure 4.25: dI_d/dV_g vs. V_g and I_d vs V_g for T573 at 77 K, for a MESFET fabricated from T573 by removal of the double barrier

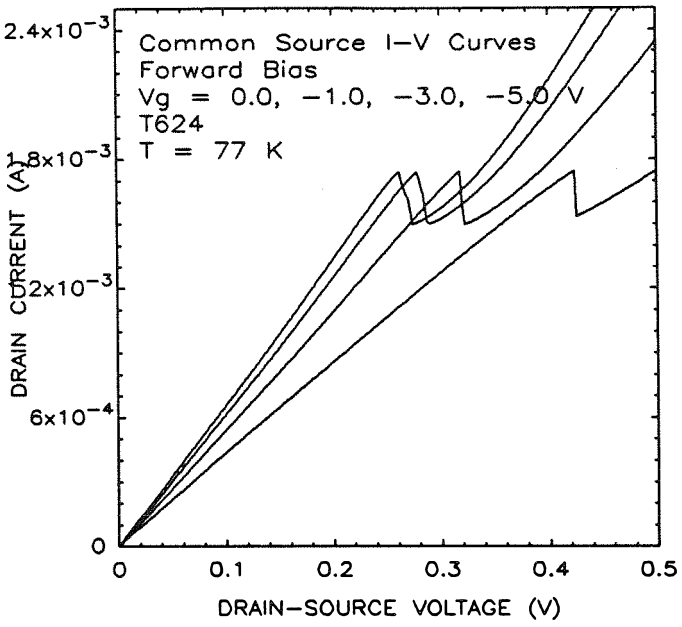

Figure 4.26: Forward-bias common-source I–V data for T624

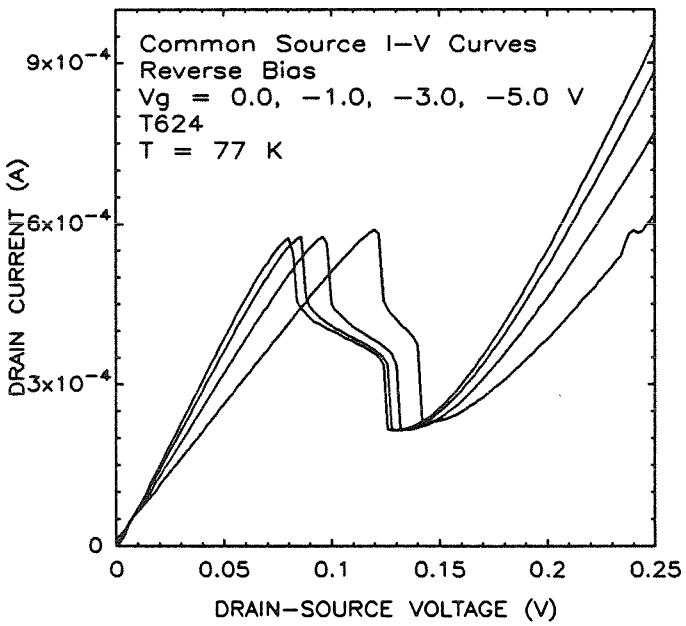

Figure 4.27: Reverse-bias common-source I–V data for T624

4.7.7 Sample T625

The characteristics for this device, illustrated in Fig. 4.28, are very interesting. NDR is seen in the saturation region of the FET. In this respect, the characteristics are similar to T640. This device also exhibits higher current operation than in other samples. Of three preparations made from this sample, only one device showed the DB/MESFET behavior illustrated, with other devices showing high resistance or a lack of NDR, or both. This fact suggests a problem in the growth of the sample, which is supported by its poor surface quality.

4.7.8 Sample T640

Transconductance

The transconductance varies for this sample, depending upon what branch of the gate hysteresis loop one is on. Values ranged between 0.002 and 0.007 S for 5 μm gate devices, with a gate width of 150 μm. This yields normalized values of 13 to 47 mS/mm. Full channel mobility calculations for this sample are somewhat questionable, since no FET-only preparations were made for this sample. Doing the calculation anyway yields a knee voltage of about 3.5 V at room temperature, which is consistent with a mobility of 1200 $cm^2/(Vsec)$, which is not out of line for the doping values in this device. The predicted mobility from Eq. 4.4 is

$$g_m = 0.02\left(1 - \sqrt{\frac{V_g + V_{bi}}{V_p}}\right) S. \tag{4.6}$$

This model predicts an actual value of $g_m \sim 10$ mS at $V_g = 0$.

4.8 Conclusions

There are several conclusions to be drawn from the work presented in this chapter. They are summarized in itemized form below.

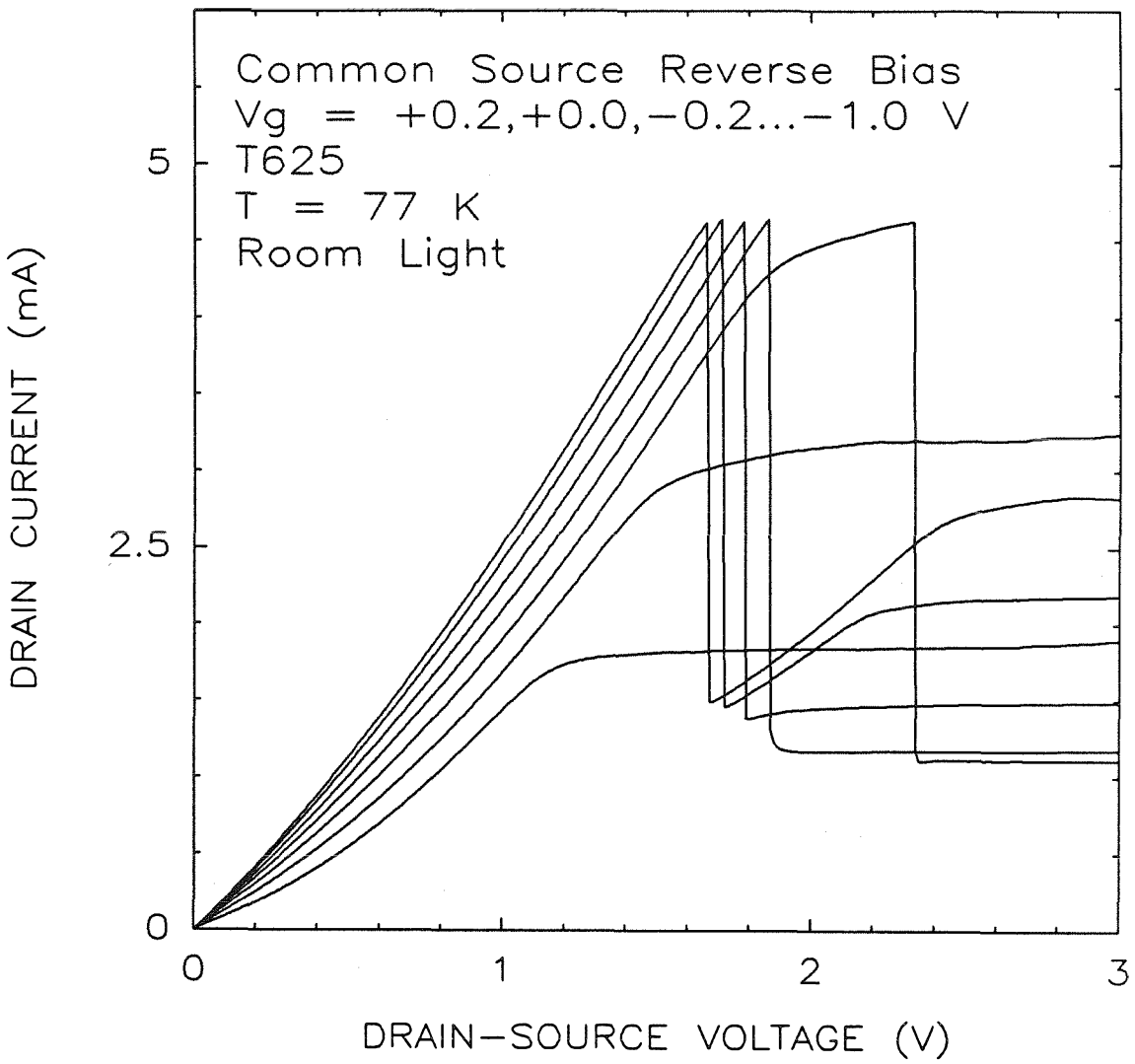

Figure 4.28: Reverse-bias common-source operation of T625.

1. Resonant tunneling transistors formed by the series integration of double barriers and MESFETs can be made.

2. A variety of characteristics can be obtained, depending upon the relationship of the double barrier and the MESFET. Several types of behavior have been identified:

   (a) Linear region NDR placement: the classic device. The resistance of the double barrier is large compared with the full channel resistance of the FET, but only near zero drain bias, allowing both devices to be distinguished. Fig. 4.7 illustrates this case.

   (b) Expansion of NDR along the voltage axis: the DB/VFET analogy. The resistance of the double barrier is large over a wider range of biases than for linear region placement. FET characteristics are not evident, and the device looks like a DB/VFET. Fig. 4.8 illustrates this case.

   (c) Resistive FETs : hysteresis and bistability. The resistance of the FET is large compared with the size of the NDR. The NDR shifts from the linear region to the saturation region, and bistable regions result. Samples T640 and T625 illustrate this behavior (see Fig. 4.11).

3. Double-barrier dimensions significantly influence the device behavior and enable control of peak current density. The cladding layers on either side of the double barrier play a major role in determining the current through the device.

4. Comparison to basic theory shows that devices are consistent with simple models.

Double-Barrier Geometry for DB/MESFET Samples

Sample No.	Top Layer Data		Double Barriers		Back-Side Spacer (min)	Date Grown (DDMMMYY)
	Depth (μm)	Spacer (sec)	Barriers (sec)	Well (sec)		
T424	0.4	20	2.0	1.3	N/A	17OCT87
T425	0.35	20	2.0	1.3	N/A	17OCT87
T498	0.5	20	2.0	1.3	1.5	21JAN87
T499	0.38	20	1.0	0.5	1.5	21JAN87
T548	0.38	20	2.0	1.3	2	10MAR87
T549	0.35	20	2.0	1.3	2	10MAR87
T550	0.45	20	2.0	1.3	2	10MAR87
T573	0.42	20	2.0	1.1	2	25MAR87
T624	0.38	20	1.8	1.1	1	13MAY87
T625	0.46	20	1.6	1.0	1	13MAY87
T640	0.35	10	1.6	1.0	1	22MAY87

Table 4.1: Table of double-barrier growth information for DB/MESFET samples. No Mg doping in any samples. TMAl flow at 40 sccm. TMGa flow at 15 or 16 sccm. AsH_3 at 500 sccm. Hydrogen carrier at 3.0 SLM. All samples have a buffer layer of $Al_xGa_{1-x}As$, except sample T550.

FET Growth Information for DB/MESFET Samples

Sample No.	Layer Thicknesses c (μm)	d (μm)	e (μm)	Channel Data Time	Temp. (°C)	Doping cm^{-3}
T424	–	–	0.9	4 min.	725	unknown
T425	–	–	0.8	$40[5s(0)/1s(5)]$	725	photosens.
T498	0.23	0.23	0.54	3.5 min.	820	10^{16} photosens.
T499	0.23	0.23	0.54	3.5 min.	820	10^{16} photosens.
T548	0.32	0.32	0.56	3.5 min.	825	10^{16} photosens.
T549	0.24	0.18	0.41	$40[4s(0)/1s(5)]$	825	10^{16} photosens.
T550	0.25	0.18	0.45	$40[4s(0)/1s(5)]$	825	$1 - 5 \times 10^{16}$
T573	0.43	0.43	0.86	$60[3s(0)/1s(10)$	775	1.5×10^{16}
T624	0.22	0.45	0.79	$105[1s(0)/1s(10)]$	775	4.5×10^{16}
T625	0.24	0.49	0.86	$70[2s(0)/1s(10)]$	775	10^{16} photosens.
T640	0.18	0.37	0.63	$50[1s(0)/3s(10)]$	775	2.5×10^{17}

Table 4.2: Table of FET growth information for DB/MESFET samples. Layer captions refer to Fig. 4.1. Layer thicknesses were determined from scanning electron microscope measurements of the total back-side layer thickness, assuming that the growth rate for all three layers was the same. T550 layer thicknesses are more approximate than others, because no $Al_xGa_{1-x}As$ buffer was grown. The notation $X[Ys(a)/Zs(b)]$ refers to pulsed doping; X cycles of Y seconds with the H_2Se at a sccm, and Z seconds with H_2Se at b sccm. Other parameters are as described in Table 4.1.

Operating Parameters of DB/MESFET Samples, 77 K

Sample No.	NDR Data (F)orward and (R)everse Bias						FET Data	
	Voltage (V)		J_{peak} (A/cm^2)		P/V Ratio		Channel	L
	F	R	F	R	F	R	(μm)	(μm)
T424	0.04	0.17	0.2	0.7	2.0	2.4	0.4–0.7	30
T425	none	0.5	–	2	–	1.2	0.4–0.7	30
T498	0.15	0.09	0.06	0.02	3.8	4.3	0.5	20
T499	none	none	–	–	–	–	0.5	20
T548	0.1	0.15	0.2	0.5	4	4.5	0.4	20
T549	0.5	0.5	12	2.6	4	7	0.3–0.4	20, 5
T550	0.16	0.1	1	0.2	2.2	3	0.45	20
T573	0.22	0.36	0.7	0.5	5.6	5.7	0.6	20, 5
T624	0.08	0.28	7	20	2.6	1.1	0.6	20
T625	none	1.7	–	60	–	3.3	0.7, 0.75	20, 5
T640	none	1.1	–	360	–	4	0.5	20
T640	none	1.33	–	390	–	4	0.25	20
T640	none	2–3	–	430	–	2.2	0.18	5

Table 4.3: Table of DB/MESFET operating parameters. This information was collated from results of over 56 preparations of the listed samples. Values obtained from averages where possible. Channel depth applies to samples that are illustrated in this chapter or exhibited working characteristics. 'L' refers to gate lengths prepared.

Comments on operation, DB/MESFET

Sample	Comments
T424	not working
T425	works in rev. bias (poorly), light sensitive
T498	works in both bias directions, light sensitive
T499	poor FET behavior, no NDR
T548	works in both bias directions, light sensitive
T549	works in both bias directions, light sensitive
T550	works poorly in both bias directions, not light sens.
T573	works well in both bias directions, $g_m \sim 9$mS/mm
T624	small NDR shifts, NDR not large
T625	load-lining, works in rev. bias, light sens.
T640	thin channel load lining, works in rev. bias, $g_m \sim 40$mS/mm

Table 4.4: Comments on the performance of DB/MESFET samples.

References

[1] A. R. Bonnefoi, T. C. McGill, and R. D. Burnham, *IEEE Electron Dev. Lett.* **EDL-6**, 636 (1985).

[2] S. M. Sze, *Physics of Semiconductor Devices*, 2nd Edition (Wiley, New York, 1981), Chapter 2.

[3] A. R. Bonnefoi, Ph.D. Thesis, California Institute of Technology, 1987.

[4] R. P. Murray, in *Tunnel-Diode and Semiconductor Circuits*, edited by J. M. Carrol (McGraw-Hill, New York, 1963), p. 22.

[5] C. A. Liechti, *IEEE Trans. Microwave Theory and Techniques* **MTT-24**, 179 (1976).

[6] R. C. Clarke and M. C. Driver in *NOSC Technical Document 1035*, Appendix C, 1986.

Chapter 5

Device Applications

There are a lot of interesting physical problems in semiconductor physics. The areas that get pursued most vigorously are generally those that offer potential for profitable market application in the future. As with most research areas, it is difficult to predict whether profitable application of the double barrier will be found and, if so, where it would be most useful. This chapter presents a few circuit applications of our devices. The results are in some cases preliminary and in all cases basic.

5.1 Summary of Results

The applications demonstrated in this chapter fall into three categories. The first category is logic. A fundamental logic element is the flip-flop. Flip-flops have been demonstrated, with single DB/MESFETs. The second category is signal processing. Frequency multiplication has been demonstrated with a DB/VFET device. Finally, DB/VFET oscillators have been studied. Oscillation at 3.3 GHz was observed, with an output power of 0.7 milliwatts (mW). Harmonics were observed to 10 GHz.

5.2 Outline of Chapter

The first topic is logic elements. Ways to realize logic structures with double barriers are described, and the advantages of the three-terminal structure are brought out. Next, frequency multiplication in the DB/VFET is described. The final topic is double-barrier oscillators. Experimental data for two-terminal DB/VFET devices are presented. A summary of important results concludes the chapter.

5.3 Logic Elements

5.3.1 Concept

We have attempted to use resonant tunneling field-effect transistors as logic elements. These devices may have advantages over the conventional transistor for logic applications. First, they have a built-in bistability. Further, fewer devices are needed for a given function. Additionally, the switching speed of the diode is high.[1] It should therefore be possible to fabricate circuits with fewer elements that are faster than standard logic circuits. The goal here is to demonstrate the feasibility of the circuits.

We have two RTT devices from which to choose. The DB/MESFET is used because it can be easily combined with conventional transistor circuits. The basic idea utilizes two stable intersections of a load-line with the I–V characteristic. These two intersections form the logical states of the system. An isolated third terminal is used to preset these states. The circuit diagram of the devices discussed in the following sections is presented in Fig. 5.1.

The experimental setup was as follows. The device, wire-bonded and mounted to a T0-8 transistor header, was immersed in liquid nitrogen with the use of a long

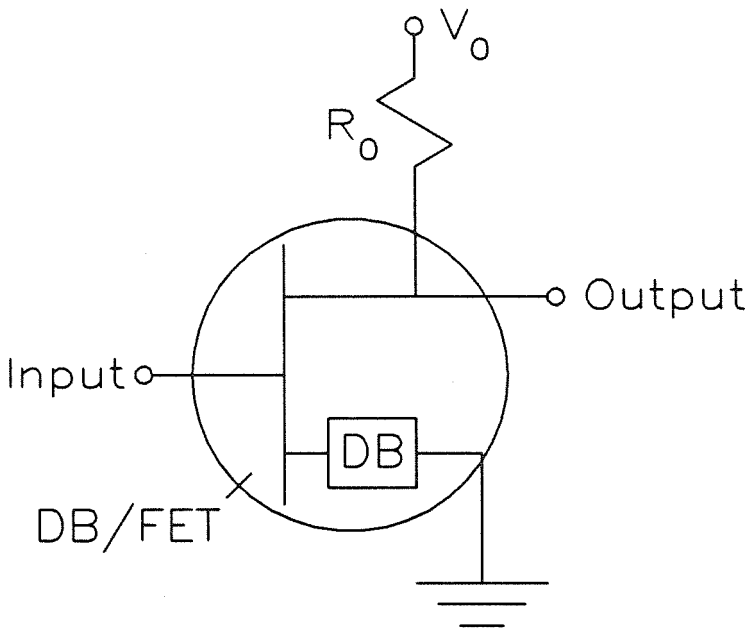

Figure 5.1: Circuit diagram for flip-flop (and frequency multiplier) applications. The DB/FET device is circled and is composed of an FET integrated with a series double barrier (the boxed 'DB').

probe. Leads from this probe were connected to bias supplies, bulk resistors, pulse generators, and an oscilloscope. The nature of the experiment prevents effective high-speed measurements.

5.3.2 Sample T640 Flip-Flops

T640 is a natural choice for this work because of its bistable characteristic. In Fig. 5.2 we present reverse-bias common-source I–V characteristics for a device fabricated from sample T640, with V_g as a parameter. Fig. 5.1 illustrates the circuit used for flip-flop demonstration. A load-line appropriate to this application is shown in Fig. 5.2. For the $V_g = -0.5$ V curve, there are two intersections of the load-line with the I–V curve. Device history determines the operating point.

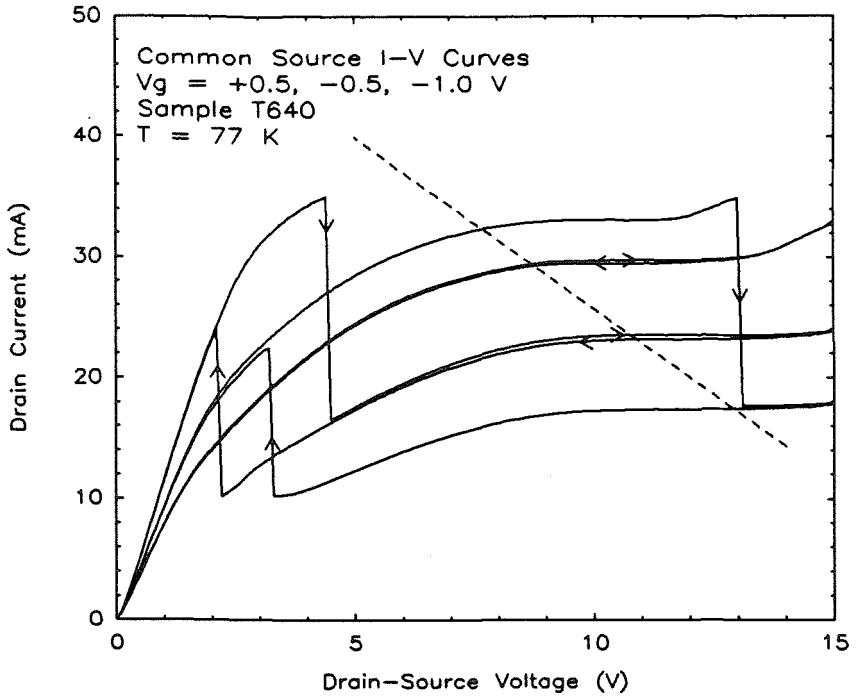

Figure 5.2: I–V curves for a T640 flip-flop device. A load-line appropriate to flip-flop operation is shown.

For example, suppose that the drain voltage (V_d) is increased from 0 to V_0. Then the stable operating point will be on the low-voltage side of the NDR, at about 7 V. If V_d is decreased from a high voltage to V_0, the stable point will be on the high-voltage side of the NDR, at about 12 V.

Consider the two other characteristics presented in Fig. 5.2. For $V_g = +0.5$ V, the resistance of the channel is decreased, and the hysteresis region shrinks. The intersection of the load-line with this characteristic is unique, and lies on the high-voltage side of the bistable region, at about 9 V. Similarly, the $V_g = -1.0$ V characteristic has a single intersection on the low-voltage side of the bistable region.

In these characteristics we have the essence of a two-state memory element, or flip-flop. Operation is illustrated in Fig. 5.3. The two stable states existing

at $V_g = -0.5$ V are interchanged with gate-bias pulses. Application of a positive voltage pulse to the gate causes the DB/MESFET to enter the high-voltage stable state at the end of the pulse. It remains in this state until a negative voltage pulse is applied to the gate, causing the device to switch to a lower voltage state. Switching was observed for 5 nanosecond pulses, the limit of our pulse generator. The ultimate switching speed was not determined.

5.3.3 Sample T573 Flip-Flops

In Fig. 5.4 we present forward-bias I–V data for a device fabricated from sample T573. Fig. 5.1 illustrates the circuit used for flip-flop operation. This device also shows flip-flop behavior. An appropriate load-line is shown. The two stable points are on the $V_g = 0$ curve. One intersection is on the low-voltage side of the NDR, at about 0.2 V. The other is on the high-voltage side of the NDR, at about 0.35 V. These two stable states can be toggled with gate bias in much the same way as in sample T640. There is one significant difference, however, in that unipolar bias pulses could be used with this sample.

For a load resistance of about 5kΩ, gate biases in the range $-1.1 < V_g < -0.65$ V yield a single stable intersection, on the low-voltage side of the NDR. When gate biases in this range are removed, the stable operating point returns to the low-voltage state. For gate biases more negative than -1.1 V, no NDR is present, and only one stable point exists. When this level of gate voltage is abruptly removed, the device stabilizes on the high-voltage side of the NDR. This behavior permits the operation of a flip-flop with unipolar bias pulses, an improvement over the bipolar pulses needed in sample T640.

In Fig. 5.5 we present input-output data for the T573 flip-flop. For clarity, operation with 5μs pulses is illustrated. A few hundred nanoseconds was found to be the shortest pulse that would interchange the states.

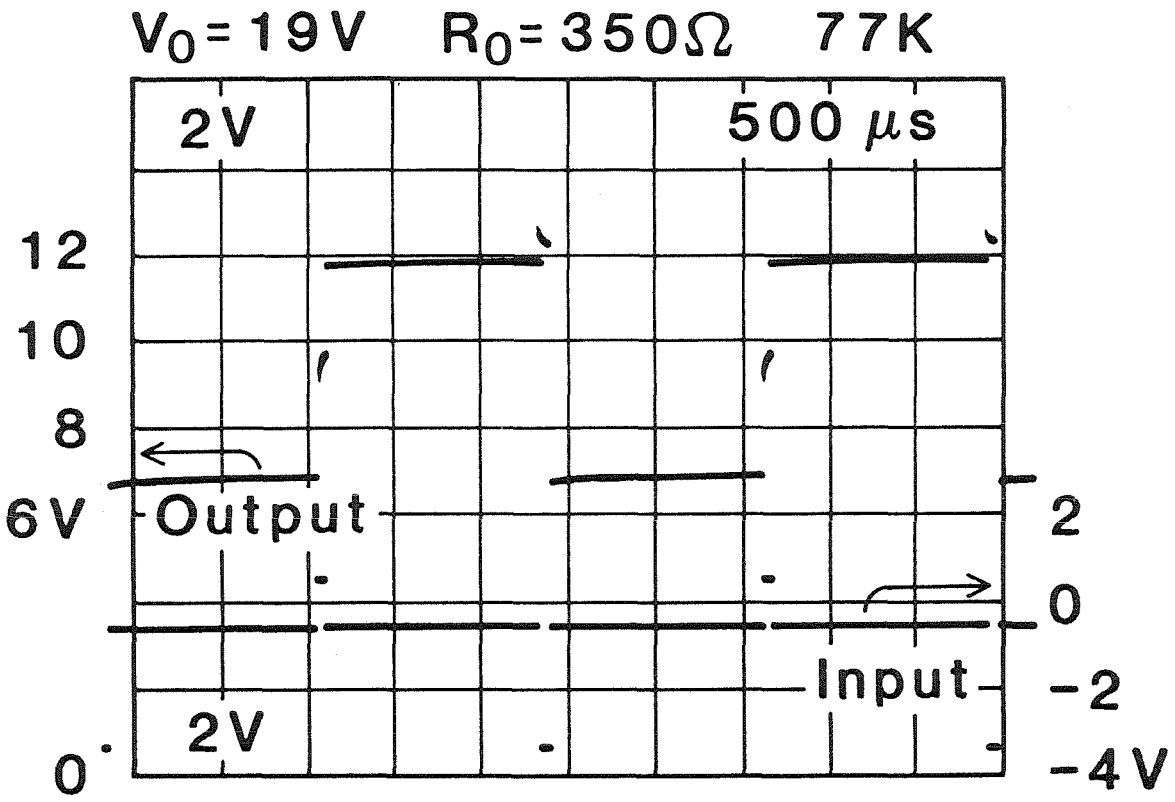

Figure 5.3: Input and output oscilloscope traces for a flip-flop fabricated from sample T640. The device characteristic is shown in Fig. 5.2. The lower trace is the input pulse train, at 2 V/div. The time scale is 500 μS/div. A variety of V_0 and R_0 values will work.

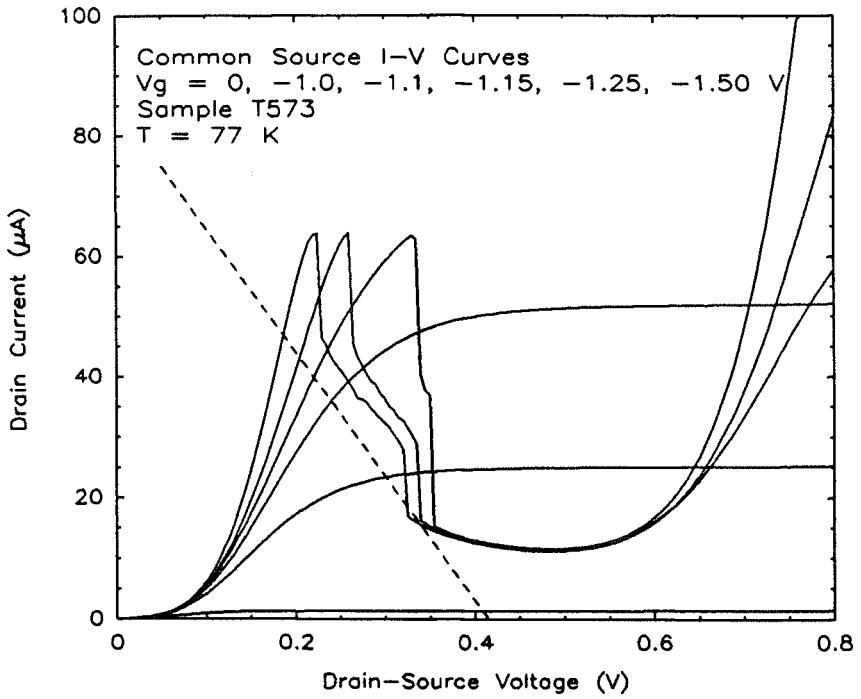

Figure 5.4: I–V data for sample T573 appropriate to flip-flop operation. A load-line for this function is shown in the figure.

Sample T573, from which these flip-flops were fabricated, has a very low current density, and consequently, does not exhibit extremely high-speed operation. Devices similar in operation to the T573 flip-flop, but with a greater ultimate speed, should be possible, by increasing the current density passing through the double barrier.

The operation of the sample T573 flip-flop relies on abrupt removal of gate bias. For example, consider a case in which $V_g = -1.5$ V is applied to the gate. A slow change in gate bias would eventually yield a $V_g > -1.1$ V state, from which we know the system returns to a low-voltage state. There is a sharp transition between gate biases that result in high-voltage stabilization and low-voltage stabilization. Either the voltage across the double barrier changes as gate bias passes this transition point, or the dynamics of charge rearrangement in the device play

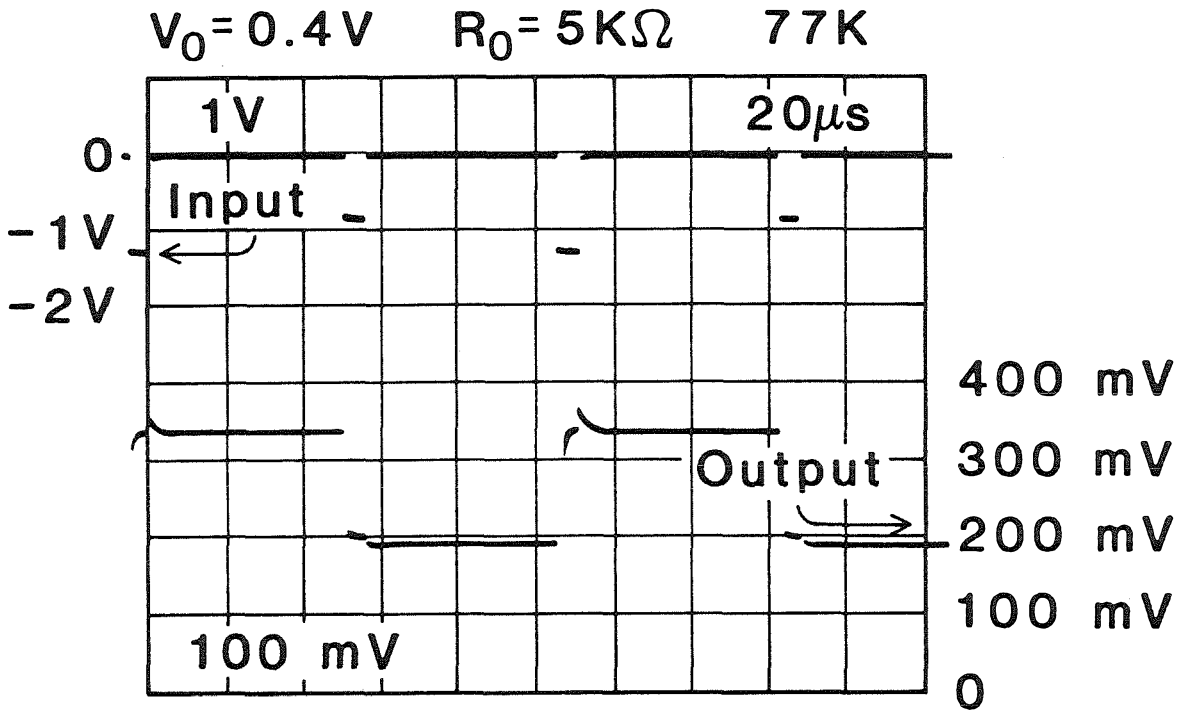

Figure 5.5: Input output oscilloscope data for a flip-flop fabricated from sample T573. The upper trace is the input pulse train, at 1 V per division. The lower trace is the output flip-flop data, at 100 mV per division. The time scale is 20μs per horizontal division.

a role in determining the operation.

5.3.4 Other Logic Operations

A two-input AND gate has been made utilizing a single DB/MESFET fabricated from sample T573. From Fig. 5.4 we can see that significant shifts of the NDR do not take place until gate voltages in excess of -1 V are applied. Thus, a level logic can be realized in which 0 or single -0.8 V inputs, do not cause a large output voltage, but -1.6 V does. In this case, the circuit load-line is not bistable.

A series combination of two T640 DB/MESFETs also produced AND operation. This operation was not ideal, because the two devices were not well matched to one another. The bistable switching features of both diodes are used in this operation; it is similar to a type of tunnel diode logic. It differs in that isolation via the transistor gates is provided. The basic idea is that the voltage will divide unequally across the devices, with the device receiving most of the potential being preset with gate bias. As supply voltage is increased, a variety of stable operating intersections are possible, because both devices exhibit bistable regions. The device executes the AND function over only a certain range of supply voltages, distinguishing it from ordinary two-transistor logic gates.

5.3.5 Other Devices

Other DB/MESFET devices should also be capable of performing logic operations. In fact, the ability to tailor the characteristic would be an attractive way of improving device behavior. The MBE growth capability that we now have would enable this tailoring. Additionally, DB/VFET devices should work as flip-flops, but the gate and drain voltages would be much larger.

Flip-flop and NOR gate logic operation has been reported for other types of RTTs. The RHET device (see Chapter 2) has demonstrated NOR gate and flip-flop

operation using a single transistor.[2,3] Capasso *et al.*have described more involved logic operations with combinations of the double barrier and more complex circuit elements.[4,5]

5.3.6 Extensions

A lot of refinements of this work are possible. A careful examination of the T573 flip-flop unipolar bias switching would be useful. Another interesting thing would be the fabrication of rudimentary integrated circuits. For example, two DB/MESFET devices could be combined on a chip to form the AND gate structure described previously. Other kinds of logic structures could probably be designed. The series combination of two double barriers could be easily accomplished in the DB/MESFET by the use of two mesas in series with the FET or by placing a double barrier in *both* the source and the drain of the device.

A serious issue is the interconnection of several flip-flops to form a simple digital system (a counter, for example). This input-output coupling will not be easy because of differences in level between input and output and, in some cases, the requirement of bipolar voltage pulses. We have not devised a method for direct input-output interconnection.

An important final refinement is possible with the parallel interconnection of several double barriers. By varying the voltage between the individual double barriers, a multiple-peaked characteristic can be obtained with more than two stable load-line intersections. For example, by connecting two double barriers in parallel and varying the voltage between them, two NDR regions can be obtained.[4] Two NDR regions yield three stable intersections with an appropriate load-line, and the possibility of multiple-valued logic. This idea could be productively applied to the DB/MESFET, where an isolated input terminal exists, which can control these stable states. A specific example would utilize the parallel interconnection of

two DB/MESFETs, with a variable voltage between the drains. This would yield a characteristic with 2 NDR regions and 3 stable states, which could be *independently* controlled with gate bias to the appropriate DB/MESFET. Extension to 5, 7, and more states might be possible.

5.3.7 Historical: Tunnel Diodes

Logic circuits using negative resistance elements are not a new idea. A variety of circuits were developed for the tunnel diode.[6] One of the logic systems developed for the tunnel diode is referred to as "majority decision" logic or "locked pair" logic. The fundamental unit is a series combination of two tunnel diodes. When connected this way and biased above the NDR voltage of one of the diodes, the voltage divides across the two diodes unequally. One of the diodes always has most of the voltage. This diode can be chosen, enabling one to perform logic operations.[7,8] The major problem with this circuit is one of isolation, as well as a requirement for well-matched pairs of diodes. Further, no amplification of output is provided.

A second concept sets out to solve the isolation problem with the use of a transistor. Such circuits were able to combine the switching speed of the diode with the transistor for isolation. The basic element was an emitter follower with a tunnel diode load. Logic levels were input to the base, and output across the tunnel diode switched between stable states on the high- or low-voltage side of the NDR. Switching speeds of 700 psec were obtained with these devices.[9] This device looks pretty good, but it required two non-integrated circuit components, the tunnel diode and the bipolar transistor. Successful input to output interconnection was not demontrated, and only isolated devices are reported in Ref. 9.

5.4 Frequency Multiplication

5.4.1 Concept

The idea for a frequency doubler comes from the observation that output goes from low to high to low as the input goes from high to low. This basic doubling function can be made to work most effectively in a system that allows stable intersections in the NDR region, so the load resistor should be less than the magnitude of the negative resistance. DB/VFETs are therefore the device of choice for signal processing work.

5.4.2 Results

The basic circuit configuration used to produce frequency doubling is illustrated in Fig. 5.1. In Fig. 5.6, we present I–V curves for sample T335, taken at 77 K, with V_g as a parameter. A load-line appropriate to frequency doubling is shown in the figure. In Fig. 5.7 we present a variety of input-output oscilloscope traces for this device. As can be seen, several waveforms are observed as the load-line sweeps through the NDR region. Fig. 5.7(c) illustrates a clear doubling of the input.

The load-line appropriate to the doubling action seen in Fig. 5.7(c) lies near the end of the NDR region of the device (as shown in Fig. 5.6). A number of interesting output waveforms are obtained as the load-line sweeps through the NDR region. Some of these are shown in Fig. 5.7(a) and (b). In (a), the load-line is just entering the NDR region (the precise voltages vary somewhat from device to device). In (b), the load-line is well into the region. The complex behavior seen may be due to multiple intersections of the load-line with the characteristic or with hysteresis.

The speed of the resultant device is not high. The maximum frequency at which doubling was evident was about 100 kHz. Measurement parasitics and gate charging effects are responsible. The change in gate capacitance for the actual

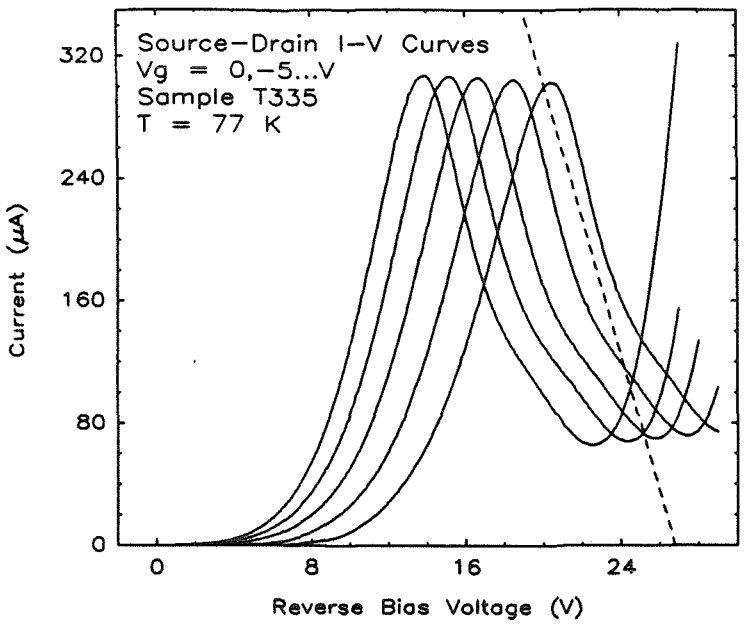

Figure 5.6: T335 I–V curves taken at 77 K, with V_g as a parameter. A load-line appropriate to the frequency doubling shown in Fig. 5.7(c) is shown.

DB/VFET device used to make the doubler over the input voltage range of 15 V was about 6 nF/cm^2 across an area of 220 × 260 μm, or about 3.5 pF. This charge can be modulated by 100 μA at about 2 MHz.* This estimate suggests that measurement parasitics are limiting us at the present. Ultimate performance could be greatly improved by decreasing the gate area, increasing the current density, and improving the transconductance. About 2 orders of magnitude improvement could probably be obtained with existing devices by decreasing gate area and increasing the drain current. Further improvement would probably require a more sophisticated device design (see Chapter 3).

*This is obtained by calculating the RC product as $\tau = CV/i$.

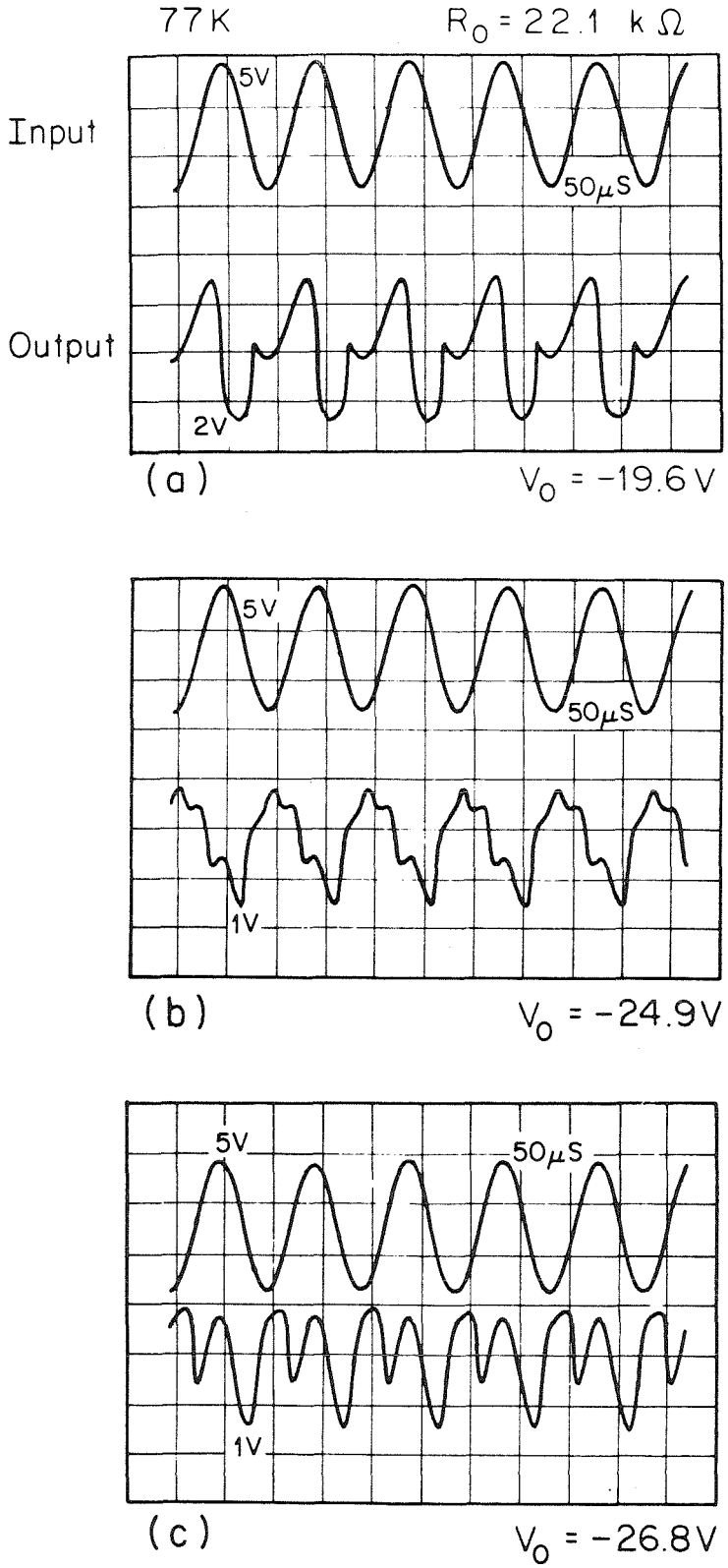

Figure 5.7: T335 frequency multiplier input and output oscillographs.

5.4.3 Refinements

Several extensions of this work can be envisioned. One could imagine using the DB/MESFET as a frequency doubling device. It is useful to be able to traverse the entire NDR region in this sort of application, to obtain a continuous output waveform, meaning that characteristics of the sort shown for the reverse-bias behavior of sample T573† might be useful here. Doubling of sawtooth waveforms is possible with bistable characteristics (like t640).

Another refinement would allow higher multiplication ratios. As mentioned in the last section, a parallel combination of double barriers can yield a multiple NDR regions. This double-peaked curve might permit output swings of "low-high-low-high-low" for inputs of "low-high." A different realization of tripling utilizing a multiple-stable point configuration was realized by Capasso *et al.*and is described in Ref. 4.

5.5 Oscillators

Oscillators are an immediate possibility any time a negative resistance element is seen. Tunnel diodes, IMPATT diodes, Gunn diodes, and their derivatives are all two-terminal NDR devices that were developed primarily for their oscillator properties. The advantage of a solid-state device lies in its low power consumption, small size, and high reliability.[10]

A lot of effort has been put into double-barrier diode (DBD) oscillators. Most of this work has taken place at MIT Lincoln Labs. These workers have been able to achieve 200 GHz oscillation from the double barrier and are expecting to reach 600 GHz.[11] Generally, three-terminal oscillators are not as fast as two-terminal oscillators. However, in a situation in which two- or three-terminal devices may be

†See Chapter 4 for these data.

used, the three-terminal device is often chosen. A good example of the desirability of three-terminal oscillators is the increasing popularity of MESFET oscillators and microwave amplifiers.[12] For this reason, it is reasonable to investigate the oscillator possibilities of the DB/MESFET and DB/VFET. This project is incomplete. A lot of interesting things remain to be done. Nevertheless, the results to date are worth presenting.

5.5.1 NDR oscillators

Negative resistance devices can be used as oscillators, and the NDR of the double barrier provides one method of constructing oscillators. Conceptually, the idea is to produce an RLC circuit with zero, or negative, R. Provided that transit-time effects and other physical differences can be neglected, tunnel-diode oscillator theory can be directly applied to the double-barrier diode (DBD).[13,14,15] The most basic theory is based on an equivalent circuit. A sample circuit diagram is presented in Fig. 5.8. We model the DBD, biased into the NDR region, as a negative resistance and a capacitance.[‡] Tunneling time is neglected. The inductance is that associated with measurement circuitry (wire bonds, intentional circuit elements, or perhaps transit delays in the device itself). The series resistance is associated with wiring, contacts, and degenerately-doped cladding layers.

The impedance of the circuit presented in Fig. 5.8 can be calculated, and the resistive (f_r) and reactive (f_i) cutoff frequencies determined:

$$Z_{in} = \left\{ R_s + \frac{-R_n}{1+(\omega R_n C)^2} \right\} + j \left\{ \omega L + \frac{-\omega R_n^2 C}{1+(\omega R_n C)^2} \right\} \tag{5.1}$$

$$f_r = \frac{1}{2\pi R_n C} \sqrt{\frac{R_n}{R_s} - 1} \tag{5.2}$$

$$f_i = \frac{1}{2\pi R_n C} \sqrt{\frac{R_n^2 C}{L} - \frac{1}{(R_n C)^2}}\,, \tag{5.3}$$

[‡]The capacitance of the DBD can be much less than that of a tunnel diode.

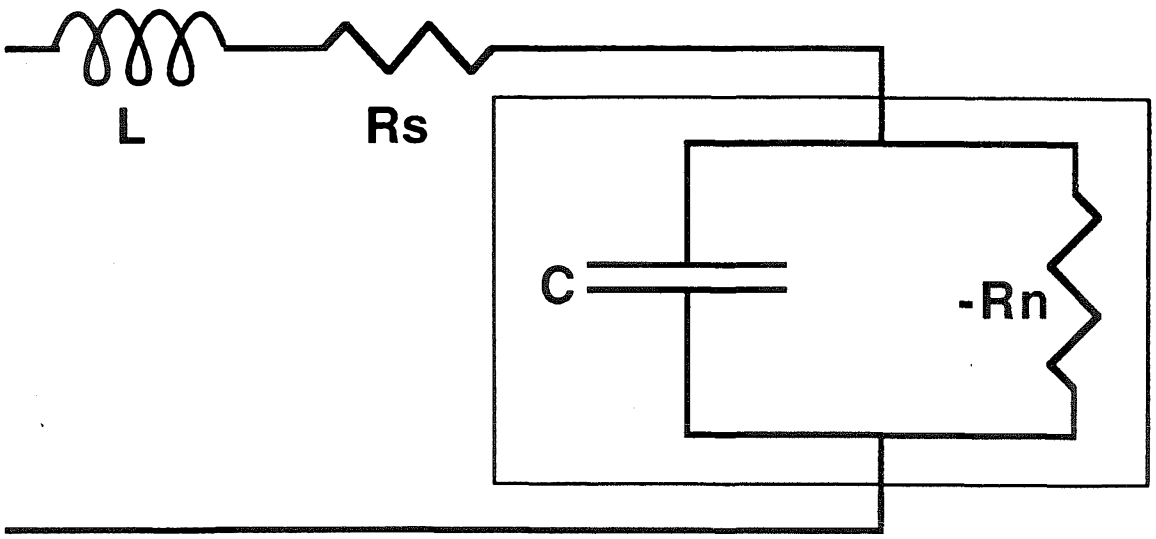

Figure 5.8: Equivalent circuit for double-barrier oscillator biased into the negative resistance region. R_n is the magnitude of the negative resistance. The box contains the most basic model of the double barrier, with series resistance and inductance representing external circuitry.

where circuit values are as defined in Fig. 5.8. The resistive cutoff (f_r) is the frequency above which the total resistance of the circuit is positive. For a given R_n, f_r determines the maximum oscillation frequency. As can be seen from Eq. 5.2, the maximum frequency is obtained at the smallest values of R_n. Obviously, for values of series resistance greater than than R_n, there is no frequency at which the circuit will oscillate.

The reactive cutoff frequency (f_i) is the self-resonant frequency. At f_i the imaginary part of the impedance is zero, and there is no phase difference between current and voltage. This (f_i) is the natural frequency at which the device will oscillate if $f_r > f_i$. In many circuit configurations, the self-resonant frequency is less than the resistive cutoff, and negative resistance will exist at f_i, which results in spontaneous oscillation when the device is biased into the NDR region.[15,16]

Oscillation can be easily identified by a plateau, or 'break,' in the NDR region of the DC I–V curve, as illustrated in data for several samples in this thesis.[§] This behavior was commonly observed in tunnel diodes, as described in Ref. 6. Two studies have specifically studied this plateau in the DBD, and correlated it with oscillation in the structure.[17,18] Our oscillator studies corroborate these results, since this distortion of the I–V could be observed when the device was oscillating and was absent when oscillation was not present.

Self-resonance does not happen when f_i is greater than the resistive cutoff frequency.[¶] This is desirable in some cases, especially when the external circuit should control the oscillations. Such circuit-controlled oscillation is possible when the circuit's resonant frequency is below f_r. For most DBDs, $f_i > f_r$ is difficult to obtain. Small devices have larger values of R_n, which favor $f_i > f_r$. The small size of the DB/VFET devices described in Chapter 3 (typical $R_n \sim 800\,\Omega$), coupled

[§] See, for example, Fig. 5.4.

[¶] $f_i > f_r$ can be achieved by decreasing 'L,' or by decreasing the size of the device, which increases R_n (see also Ref. 6).

with the presence of a large, lightly-doped drift region may account for the lack of strong, spontaneous oscillation in the devices illustrated in Chapter 3, by causing f_i to exceed f_r. An exact treatment would require evaluation of the equivilant circuit parameters illustrated in Fig. 5.8.

The circuit presented in Fig. 5.8 can be analyzed more thoroughly by solving the loop equations for the circuit. Solving the resulting second-order differential equation leads to an expression for the current in the device as a function of time, from which a stability diagram can be obtained.[13] Some aspects of DBD oscillator theory neglected in our discussion are described in Ref. 11.

To this point, we have ignored one of the most important parts of actually making oscillators, the power source. Somehow the DBD must be biased into the NDR region, but this bias must not affect the high-frequency circuit, or else the oscillation frequency will decrease. There are ways to isolate the bias circuitry from the device, which are often quite effective over a certain range of frequencies. The problem with the DBD (or the tunnel diode) is that it has a broadband NDR, which must be screened at virtually all frequencies. The higher the desired frequency, the more difficult this task.

5.5.2 Transit-Time Oscillators

A second class of DBD oscillator is a new idea, proposed by Kesan *et al.* This oscillator is a quantum-well injection transit-time (QWITT) device, which utilizes the double barrier as the injection device in a transit-time oscillator.[19]

The concept of a transit-time oscillator is different from the NDR oscillator ideas. The first transit-time oscillator was the impact ionization avalanche transit-time (IMPATT) diode. In an IMPATT diode, a lightly-doped *p-n* junction is biased near its breakdown voltage. RF modulation carries the device into breakdown and out again over the course of one RF cycle. Since avalanche breakdown is a highly

nonlinear phenomena, many more carriers are generated during the excursion into the breakdown region than at other times. These carriers drift across the depletion region to the electrodes. This drift takes some time. Avalanche delay plus transit-time delay results in a phase difference between the current and the voltage in the device, which can exceed 90°. This phase delay creates a dynamic negative resistance that can be used to convert DC power to RF power. The frequency is, in the simplest case, determined by the transit-time for carriers to travel from the avalanche region to the electrode region.[20]

As wonderful as IMPATT diodes are, there is room for improvement. The major problem with the device is its noise, which comes from the statistical nature of the avalanche process. A new idea, proposed by Kesan, *et al.*[19], would be to use the double barrier as the injection device. The RF voltage traverses the peak of the diode characteristic, resulting in a current injection similar to the IMPATT injection. This injected current drifts across the lightly-doped region, resulting in dynamic NDR. This device may have a number of advantages over the DBD oscillator and the IMPATT diode.[19,21] The device should be capable of operation with its quiescent bias point *outside* the NDR region, a major stabilization advantage that would permit the operation of much larger devices than are currently feasible, and yield commensurately higher power devices. The presence of the drift region results in the appearance of NDR at a higher bias level than in a conventional DBD. By coincidence, the device Kesan *et al.* have proposed has the same geometry as the DB/VFET device that we have made.

5.5.3 Results and Discussion

This section presents the initial results of a study of the oscillatory behavior of the DB/VFET device. A two-terminal configuration was used in these investigations. T335 was the sample tested. The first step in this work was the construction

of relaxation oscillators. The device was simply biased into the NDR region and an antenna was used to pick up any oscillations that were present. 135 MHz oscillations were observed, which could not be effectively controlled with external circuit elements. This lack of control may be due to excessive stray capacitances and ineffective power supply isolation. Later the device was connected directly to the spectrum analyzer (HP 8554B and HP 8552B modular units). The fundamental 135 MHz signal was observed, with harmonics clearly evident to about 1 GHz.

These experiments gave concrete evidence that T335 would oscillate. The next step was to pursue higher frequency oscillation, using microstrip circuits because of familiarity and convenience. Negative resistance oscillators were the object. Microstrip circuits were laid out, using a microstrip design program written by R. Compton and D. Rutledge.[22] This layout was photolithographically transferred to microstrip, which is a dielectric substrate with copper cladding on both sides.[‖] The finished circuits were connected to measurement apparatus, with connectors that mounted directly to the side of the DUROID, *i.e.*, no brass block was used. The sample was affixed to the DUROID with silver paint. The back of the substrate was connected to the back of the DUROID with a wire. Mesa devices were connected to the striplines using wire bonds.

Three circuits were made. Two circuits utilized external bias-tee structures[**] for application of external bias and shielding of the measurement apparatus. The bias tees were satisfactory at low microwave frequencies but were ineffective at higher frequencies, necessitating the design of circuits with the bias network on the microstrip. The basic circuit is most clearly illustrated in Fig. 5.9.

The concept behind the design is simple. The negative resistance of the double barrier has a magnitude R_n. The reflection coefficient at the device will therefore

[‖]The material used for these experiments was a DUROID substrate made by Rogers Corp. Chandler, AZ.

[**]Bias tees manufactured by Triangle Microwave.

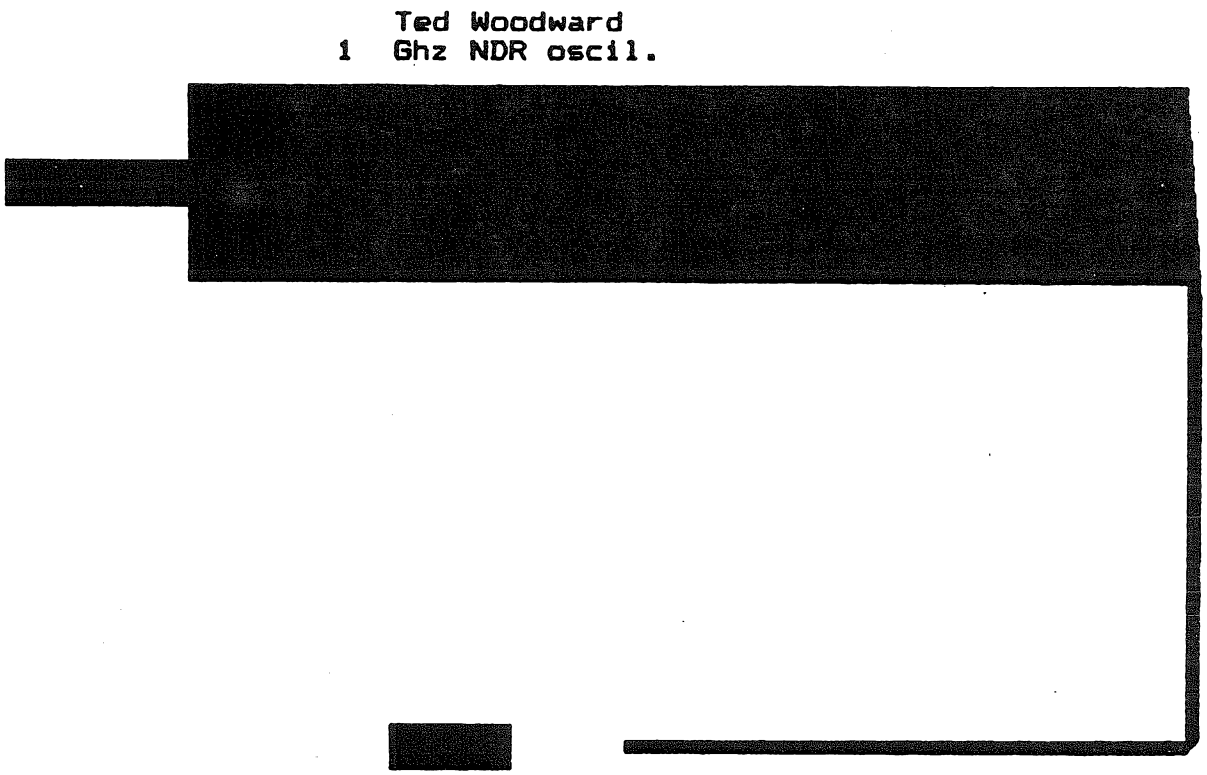

Figure 5.9: 1 GHz oscillator circuit layout, made with PUFF.[22] The quarter-wave matching segments are designed to match the negative resistance of the double barrier to the 50 Ω line.

be singular at frequencies at which the impedance of the line equals R_n. This frequency should be that at which oscillations are observed. Several drastic assumptions were made in designing this circuit. The quarter-wave sections were designed to match to the DC value of the negative resistance, $R_n = 850\,\Omega$ in the case of the 1 GHz circuit. Reactances were neglected entirely in this design. The 1 GHz circuit illustrated in Fig. 5.9 oscillated at a fundamental frequency of 0.8 GHz, with harmonics to 4 GHz observable. The power delivered to the $50\,\Omega$ load of a HP 8569B spectrum analyzer was -2 dBm, or about 1 mW. The DC power input was about 100 mW, for a conversion efficiency of roughly 1 percent. Data are presented in Fig. 5.10. The fundamental frequency did not shift very much with bias in the NDR region (less than 10 MHz).

A circuit, similar to the 1GHz case illustrated in Fig. 5.9, was made for 10 GHz. This circuit did not work because of oscillations through the power supply. 72 MHz 14 dBm oscillations were observed, with harmonics to 2 GHz.

Another circuit was fabricated for 10 GHz, with the bias network on the microstrip. The circuit is presented in Fig. 5.11. The power supply circuit is supposed to present a large mismatch at each fat/thin interface. Perfect screening occurs at frequencies at which the length of the line is a quarter-wavelength, presenting an RF short at each interface. For the 10 GHz circuit shown in Fig. 5.11 the quarter-wave match was designed for $250\,\Omega$ at 10 GHz. Measurements were made using an HP 8562A spectrum analyzer, with DC bias provided by a curve tracer. This biasing method enabled one to observe the operating point directly on the curve tracer. Similar to tunnel diodes, a smooth NDR region is observed when the device is not oscillating and a 'step' appears with the onset of oscillation.[23]

Fig. 5.12 presents spectrum analyzer data for a $116\,\mu$m device fabricated from sample T335. The device was biased into the negative-resistance region. No low frequency oscillation was observed. The fundamental frequency was about 3.3

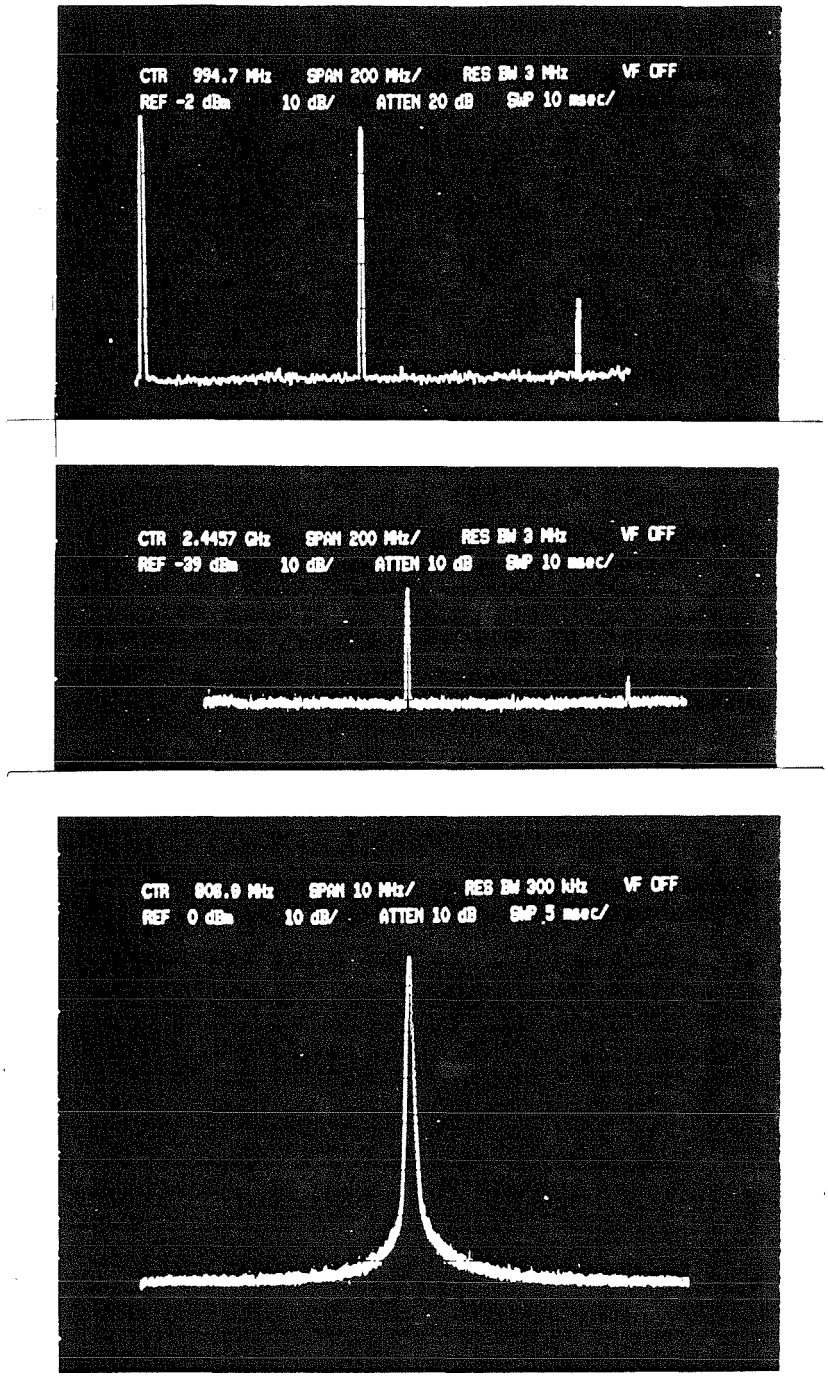

Figure 5.10: 800 MHz oscillator characteristics for sample T335. The DC voltage and current were about 20 V and 5 mA, for a power dissipation of 100 mW.

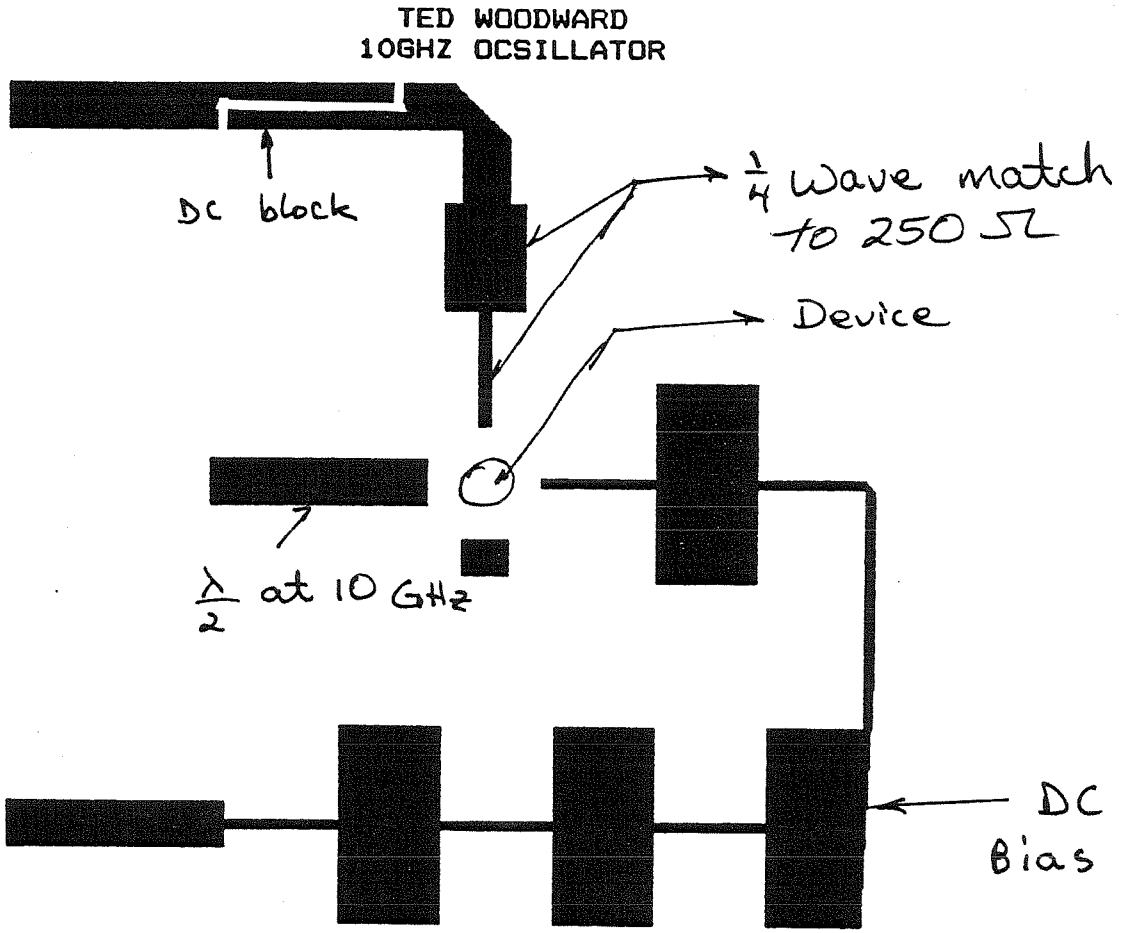

Figure 5.11: A 10 GHz oscillator circuit for use with sample T335. The various sections of the circuit and their functions are indicated. Circuit was laid out with PUFF.[22]

GHz, with a maximum output power of about 700μW. Harmonics were observed to 10 GHz. Power output at 10 GHz was only 5 nW, with about 400 nW observed at 6.6 GHz. Fig. 5.13 presents a closer view of the fundamental and first harmonic.

There are many reasons for the failure of the device to oscillate at the design frequency. The value of R_n may not be the same at 3 GHz as it is at DC. The capacitance of the device may be important. The series resistance and excess inductance of the silver paint and wire bonds, respectively, may be significant. Further, the DC block in the spectrum analyzer stripline probably changes the resistance of the transmission line, thus altering the matching impedance point. Finally, the bias circuitry did not completely shield the device from the power supply. This lack of shielding was demonstrated by the fact that device would not oscillate as readily when biased with a different power supply.

A DC characteristic for the device was obtained while it was mounted in the oscillator circuit. It is presented in Fig. 5.14. The oscillator bias point is indicated. As can be seen, this point is in the NDR region. At no time were any oscillations observed for bias points outside the NDR region, suggesting that the device is operating as a negative-resistance oscillator, rather than as a transit-time device. The transit-time frequency, assuming saturated velocity transport at 1×10^7 cm/sec across the lightly-doped region, is about 15 GHz.

Some additional measurements were performed. Larger diameter devices were tested in the same circuit in which the 116μm device was tested. As the device diameter increased, the peak power *decreased*, and the resonance became broader and peaked at a lower frequency. These results suggest that the best match to the circuit is provided by the 116 μm device and that the circuit is (at this point) the dominant actor in determining the frequency and power output of the oscillators.

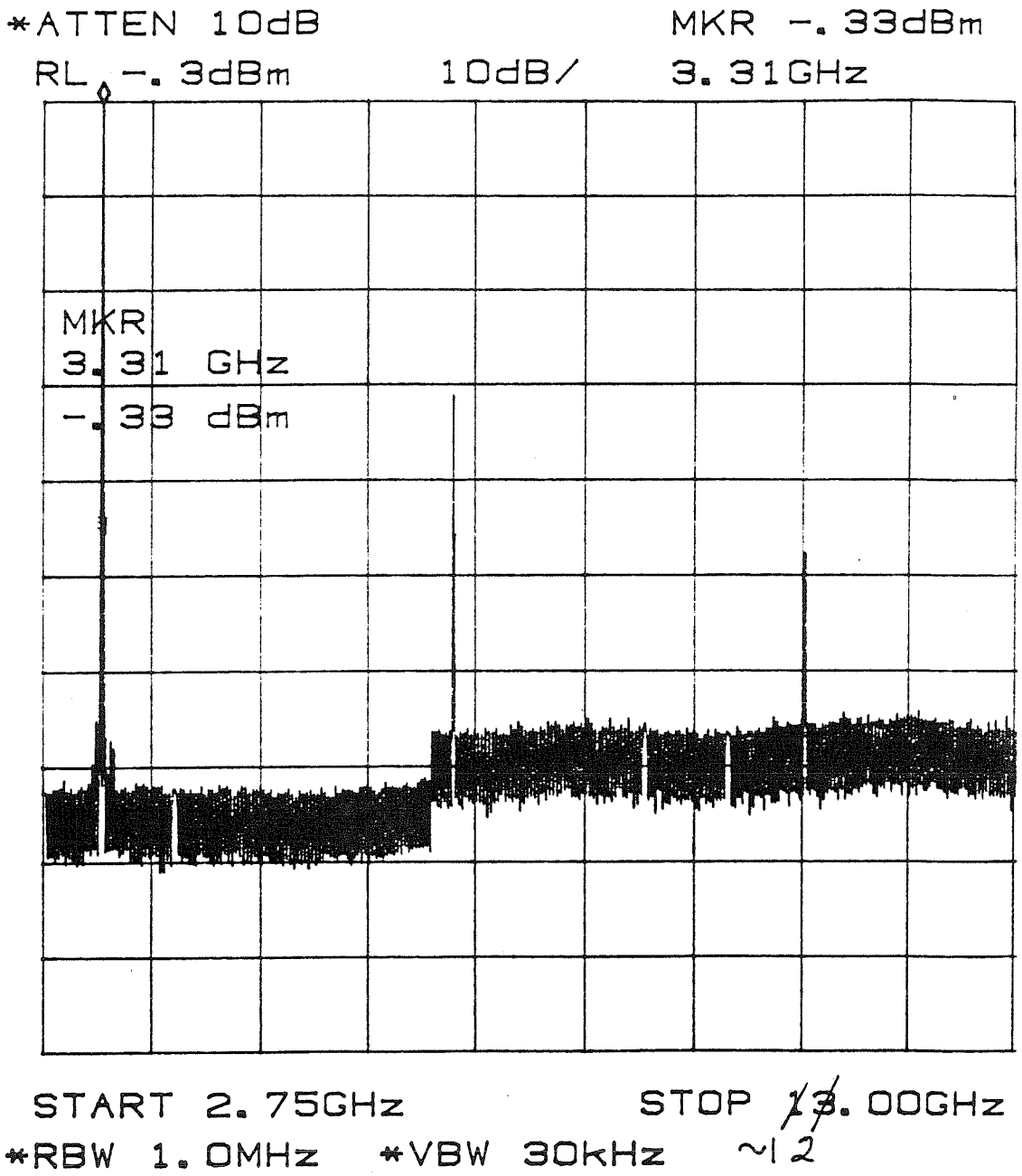

Figure 5.12: Wide-band spectrum analyzer output for a microstrip oscillator made with a 116 μm device, fabricated from sample T335. The left edge of the plot corresponds to 2.75 GHz, with the right edge being about 12 GHz (not 13).

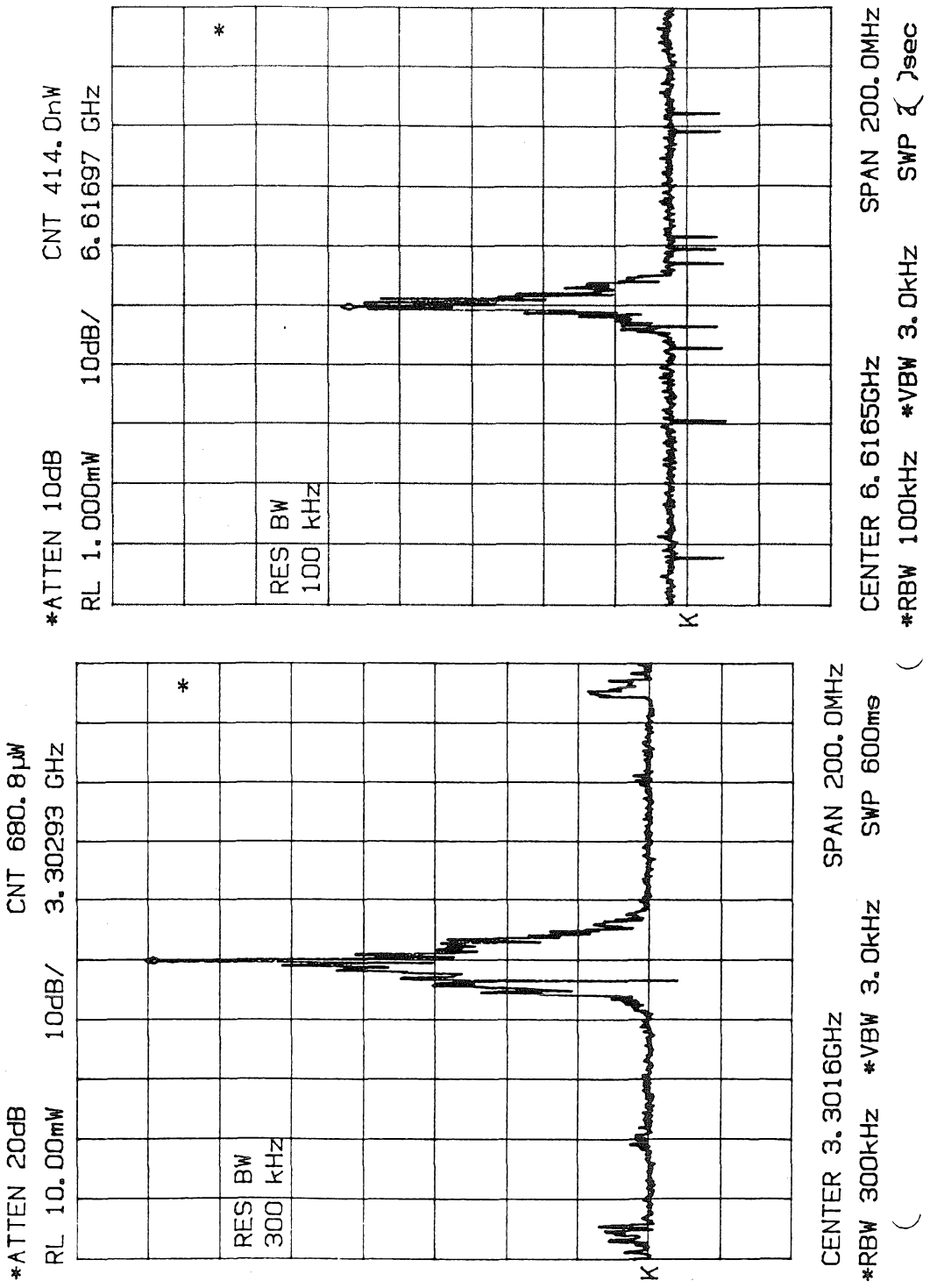

Figure 5.13: A closer view of the fundamental and first harmonic oscillation of sample T335.

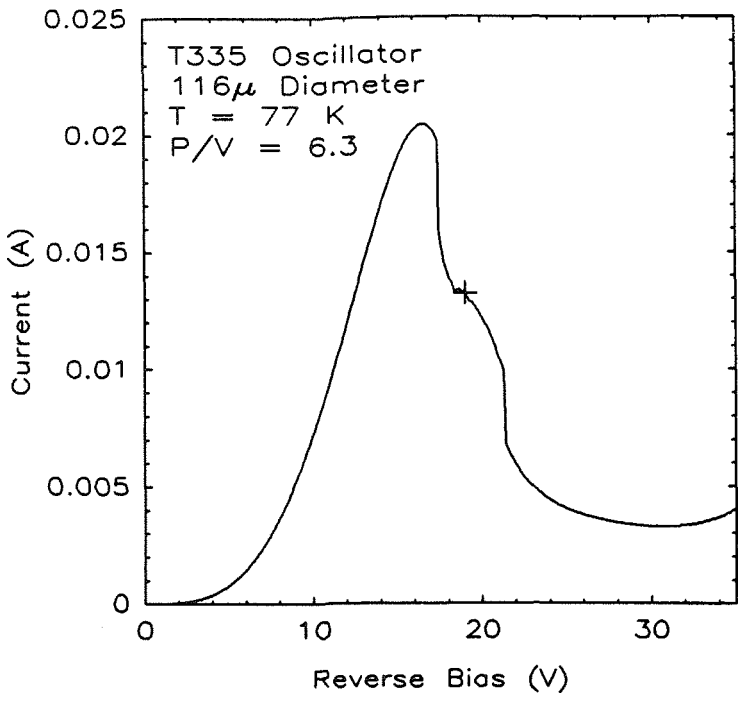

Figure 5.14: DC I–V curve for 116 μm mesa device for T335. The bias point for the oscillator illustrated in Figs. 5.12 and 5.13 is indicated.

5.5.4 Refinements

These results represent a beginning, not an end. The only definitive conclusion that can be reached from this work is that the DB/VFET is capable of microwave oscillation. Beyond that simple fact, a number of interesting questions remain. Network analyzer measurements could provide the impedance parameters of the device at high frequency, which would enable the design of more effective circuits. The use of tunable waveguide mounts would permit tuning to maximize oscillator output. This method would determine the maximum output power and oscillation frequency of the device. The QWITT device could be pursued further, to determine conclusively if such a device would work.

The addition of the third terminal might also be valuable. By modifying the

NDR parameters, the oscillation frequency or phase might be modulated. This additional degree of freedom opens the possibility of voltage-controlled oscillators, with single devices. Power combining from arrays of these oscillators, in a cavity, is possible. This novel power combining technique has been accomplished, with small arrays of Gunn diodes.[24] Having done this, the third terminal of the DB/VFET might be used to modulate the individual elements of the matrix, to create a phased array unit.

5.6 Conclusions

A couple of interesting applications of the DB/VFET have been presented in this chapter. The major results are summarized below.

1. Logic elements have been constructed with the DB/MESFET.
2. Frequency doubling has been demonstrated for the DB/VFET.
3. Microwave oscillations have been observed in the DB/VFET as a two-terminal device.
4. Extensions of these concepts have been discussed.

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Part II

GaAs/AlAs/GaAs CAPACITORS

Chapter 6

Electrical Measurements of GaAs–AlAs–GaAs Heterostructures

Single-barrier heterostructures are important constituents of many modern semiconductor devices. Devices as diverse as heterojunction bipolar transistors, quantum well lasers, modulation-doped field-effect transistors (MODFETs), and tunnel structures rely on the creation of barriers to electron transport. Research into the nature of epitaxial wide band-gap materials is therefore important.

6.1 Outline of Chapter

This chapter presents results of an experimental study of the electrical properties of n^+–GaAs/i–AlAs/n–GaAs single-barrier heterostructures. Following this outline, a summary of the major results of the chapter is presented. Background and motivation follow. Then the growth of the structure is discussed. After this the experimental details of the various measurements are described. The rest of

the chapter contains experimental results and discussion. The chapter ends with a summary of major conclusions.

6.1.1 Summary of Results

A number of samples were studied. All samples exhibited light-sensitive C–V behavior. Extensive nonilluminated data were obtained. All samples showed hysteresis in the C–V characteristics taken in darkness. The hysteresis was indicative of a nonequilibrium process. This process was investigated as a function of temperature, sweep rate, illumination, and measurement frequency. Results indicate that the hysteresis is due to the presence of deep levels. Inversion was not observed in any sample, making the structures unsuitable for use as inversion-mode FETs, although accumulation-mode GaAs gate FETs might be possible.

DLTS measurements were performed in support of the capacitance results just mentioned. These measurements confirm the results of the C–V studies. DLTS data indicate the presence of deep levels near the interface between the AlAs and the lightly-doped GaAs, with possible distribution in the AlAs. Measurements of the capture cross section and activation energy of the traps were made in two samples. Results for both samples indicate an activation energy of about 500 meV, with an emission time of many seconds.

I–V measurements were made on the samples. In darkness the samples were very resistive, with typical reverse-bias current densities being less than $10^{-7}\mathrm{A/cm^2}$. This current was light sensitive, increasing several orders of magnitude under incandescent illumination. Hysteresis was observed in the forward-bias I–V curve, at low current levels. This hysteresis was attributed to the same deep levels seen in C–V and DLTS measurements.

6.2 Introduction and Background

This chapter describes experimental studies of the electrical behavior of single-barrier GaAs/AlAs/GaAs heterostructures, which have thick (1000–4000 Å) AlAs layers. This particular system belongs to a larger class of heterostructures composed of a thick region of wide band-gap material in the midst of a narrower band-gap material. These epitaxial barrier structures are interesting for a number of reasons.

6.2.1 General Background

Epitaxial barrier structures have a number of device applications. Having created such a structure, carriers may be depleted away from, or accumulated up to, the heterojunction between the wide and narrow band-gap materials. The potential at the interface between the wide and narrow band-gap materials may be controlled because there is a barrier to electron transport at the interface. This barrier is created by the band offset between the two materials. Several devices rely on the creation of these depletion or accumulation regions. The modulation-doped field-effect transistor (MODFET) is the best known of these devices.[1]

Another property of the wide band-gap barrier structure is its resistance to electron transport perpendicular to the layer. Several devices rely on the creation of a resistive barrier region. These devices include the inverted-base collector tunnel transistor discussed in Chapter 2 as well as the so called real-space transfer devices.[2] Finally, devices that rely on the creation of an inversion layer* depend on the resistance of the wide-gap material to minority and majority carrier transport, as well as interface quality.

*An inversion layer is created when the band bending at the wide band-gap/narrow band-gap interface is sufficient to generate minority carriers at the interface. See discussions in Ref. 3 for further information.

The epitaxial nature of the barrier layer yields a number of advantages over other types of barrier layers. The most significant of these is the ability to deposit crystalline material on top of the insulating layer. Crystalling regrowth is difficult to achieve with amorphous insulators such as SiO_2. Additionally, the quality of the interface between the barrier and the conducting layer can be important. A large number of interface states are often present when amorphous insulators are deposited on compound semiconductors. Finally, the fact that the barrier layer is a semiconductor allows the possibility of introducing dopants into the barrier. The carriers created by these dopants may reside not in the barrier layer, but in the narrow band-gap material surrounding it, separating the carriers from the parent dopant atoms. The process is referred to as modulation doping and enables the operation of the MODFET, mentioned previously.

6.2.2 AlAs Barriers

Having described general reasons for being interested in the study of wide band-gap epitaxial materials, we now present specific reasons for being interested in AlAs barriers. The geometry we have chosen to study consists of an asymmetrically doped GaAs/AlAs/GaAs heterostructure. The top layer of GaAs was doped degenerately with Se. The back side layer of GaAs was doped nondegenerately. AlAs barriers were several thousand angstroms thick.

The stable oxide which makes the silicon metal-oxide-semiconductor field-effect transistor (MOSFET) possible is not available in GaAs. Oxides of GaAs and other amorphous insulators deposited on GaAs fail to passivate the surface, leaving a large number of defects and surface states. These result in leakage currents.[4,5,6] The use of a wide band-gap epitaxial semiconductor as the barrier in a GaAs-based device can alleviate this problem.

The structure described here could be used as a GaAs-gate field-effect transis-

tor. The name comes from the use of n^+–GaAs as the gate electrode instead of metal. This device is like a MODFET, in that an accumulation layer is used as the conducting channel of the FET. In the MODFET the accumulation layer is created by band bending. The threshold voltage of the device is therefore sensitive to the doping level in the $Al_xGa_{1-x}As$ barrier. In a GaAs-gate FET device, the accumulation layer is created by application of a forward bias to a degenerately doped GaAs layer lying on top of an undoped AlAs barrier layer. Such a device has been made by MBE, using an $Al_xGa_{1-x}As$ barrier.[7] This device has a number of potential advantages over MODFET devices, improved threshold control and a possible avoidance of DX centers being the most significant. GaAs-gate field-effect transistors and devices like them, have demonstrated high-speed operation (11 GHz frequency division) and are being investigated in a variety of materials.[8,9]

GaAs is the logical choice for the narrow gap material of our investigation because its production technology is relatively well understood. AlAs and $Al_xGa_{1-x}As$ alloys are logical candidates for barriers in GaAs. AlAs lattice matches well to GaAs, and can be grown at roughly the same temperature as GaAs. Further, it has a large band-gap. In addition to the accumulation mode device just mentioned, depletion mode FETs have been demonstrated with $Al_xGa_{1-x}As$ barriers.[11,12] All of these devices were produced by MBE techniques.

The difference in band-gap between the two materials may be thought of as taking place abruptly at the interface between the two materials. For the GaAs/AlAs system, it is known that the band-gap of GaAs lies within the band-gap of AlAs. This kind of band offset is referred to as a type I band alignment[13], and leads to a barrier to hole and electron transport from GaAs to AlAs. The exact value of the band-offset in GaAs/AlAs systems is, as mentioned in Chapter 2, a current research question. We use a value obtained by Batey and Wright of $\Delta E_v = 0.55x_{Al}$ eV,

where x_{Al} is the Al mole fraction, or $\Delta E_c = 200$ meV for pure AlAs on GaAs.†[14] This energy is about 7.5 times the thermal energy available to carriers at room temperature.

The band structure of $Al_xGa_{1-x}As$ as a function of x is interesting. For $x < 0.45$ or so, $Al_xGa_{1-x}As$ is a direct-gap material. At higher Al mole fractions, it is indirect. The valence-band offset of $Al_xGa_{1-x}As$ on GaAs has been found to be linear with x.[14] The conduction-band offset is not so simple. For the direct offset, it increases with x, to a maximum at pure AlAs of 1.05 eV. The offset between the Γ point in the GaAs band structure and the X point in $Al_xGa_{1-x}As$ decreases with increasing Al mole fraction. The result is that the conduction-band offset for thermal transport (the minimum band offset) is maximized at the direct-indirect transition at a value of about 350 meV.[14] Consequently, most device research has focused on barriers of $Al_xGa_{1-x}As$ with $x \sim 0.45$. A graph of the band offsets in the $Al_xGa_{1-x}As$ /GaAs system is presented in Fig. 6.1, from Ref. 14.

In spite of the decreased conduction-band offset, it is possible that the AlAs barrier could be as good or better than the alloy at resisting current transport perpendicular to the layer. Doping would enable one to increase the effective barrier of the AlAs. Additionally, the effective mass at the X point of the AlAs is much larger than that at the Γ point of the alloy. The increased mass decreases the tunneling current through the structure, which can be a significant leakage path. Finally, the increased valence-band offset in AlAs could be very valuable for p–type devices as well as for investigation of inversion in n–type structures. The use of both types of devices is important, because it can allow the realization of low power-dissipation complementary-logic circuits.[10]

†This offset is between the Γ point in the GaAs and the X point in the AlAs. If the Γ point in the AlAs is considered, the conduction-band barrier increases to about 1 eV.

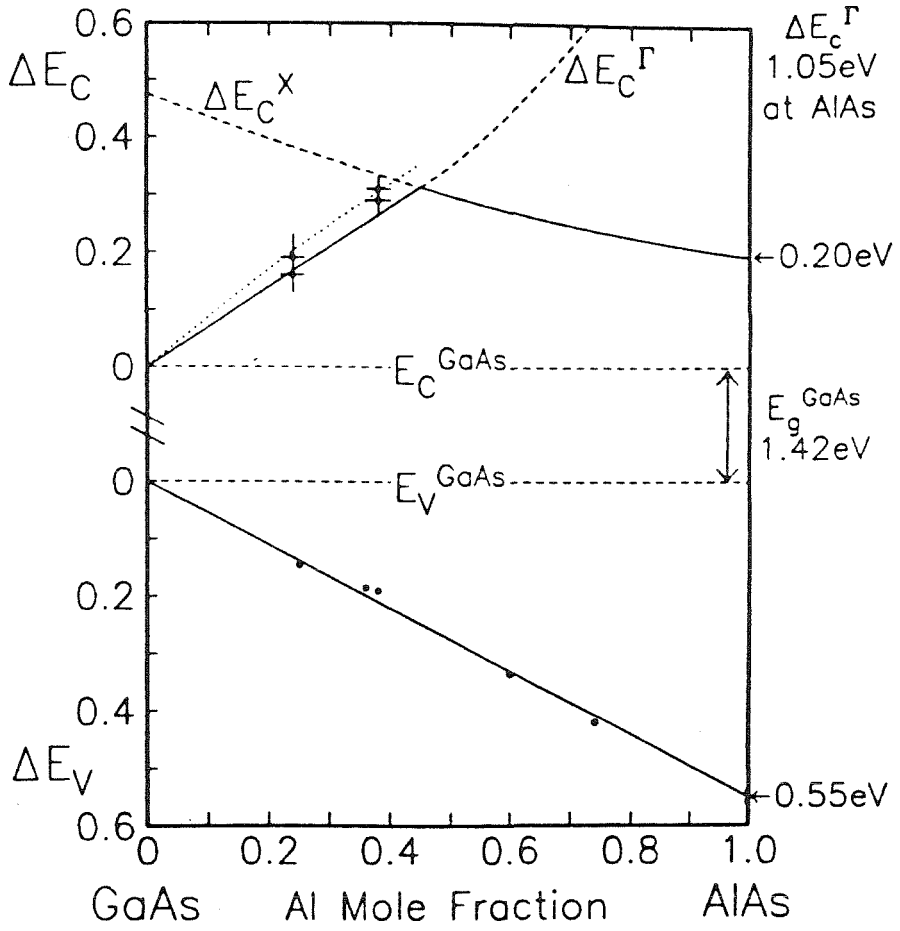

Figure 6.1: Band-offsets in the GaAs/$Al_xGa_{1-x}As$ system, from Ref. 14

6.3 Geometry and Growth

A number of samples were studied. The geometry of all samples was similar. Samples were grown by MOCVD on conducting GaAs substrates. The growth technique has been reviewed in Chapter 2. A buffer layer of varying composition and thickness was grown on top of the substrate. The first relevant device layer was a lightly-doped GaAs region, several microns in thickness. Following this, a layer of AlAs was deposited, of 1000 to 4000 Å in thickness. This layer was doped lightly n–type, p–type, or not intentionally doped. On top of the AlAs layer, a heavily-doped ($\sim 3 \times 10^{18}\,\mathrm{cm}^{-3}$) electrode region was deposited, whose thickness varied between 1 and 4 μm. Samples were grown at temperatures ranging from 700 to 800 $^{\circ}$C. A summary of important sample information for selected structures may be found in Table 6.1 at the end of this chapter.

Calculations of the equilibrium band diagram for this geometry are presented in Fig. 6.2. These diagrams were calculated using a computer program developed by Amikam Zur.[‡] The diagrams illustrate the shape of the potential for two cases: p–type barriers and n–type barriers. Note the small amount of band-bending in the degenerate electrode, as compared to the nondegenerate one. These diagrams are intended to provide an intuitive grasp of the geometry being studied and how it varies with doping.

6.4 Experimental

6.4.1 Fabrication

Photolithographic techniques were used to define Au-Ge mesa contacts with areas ranging from 70 to 450 μm. These contacts were isolated from each other by

[‡]This program, written while Dr. Zur was a graduate student, is not described in his thesis.

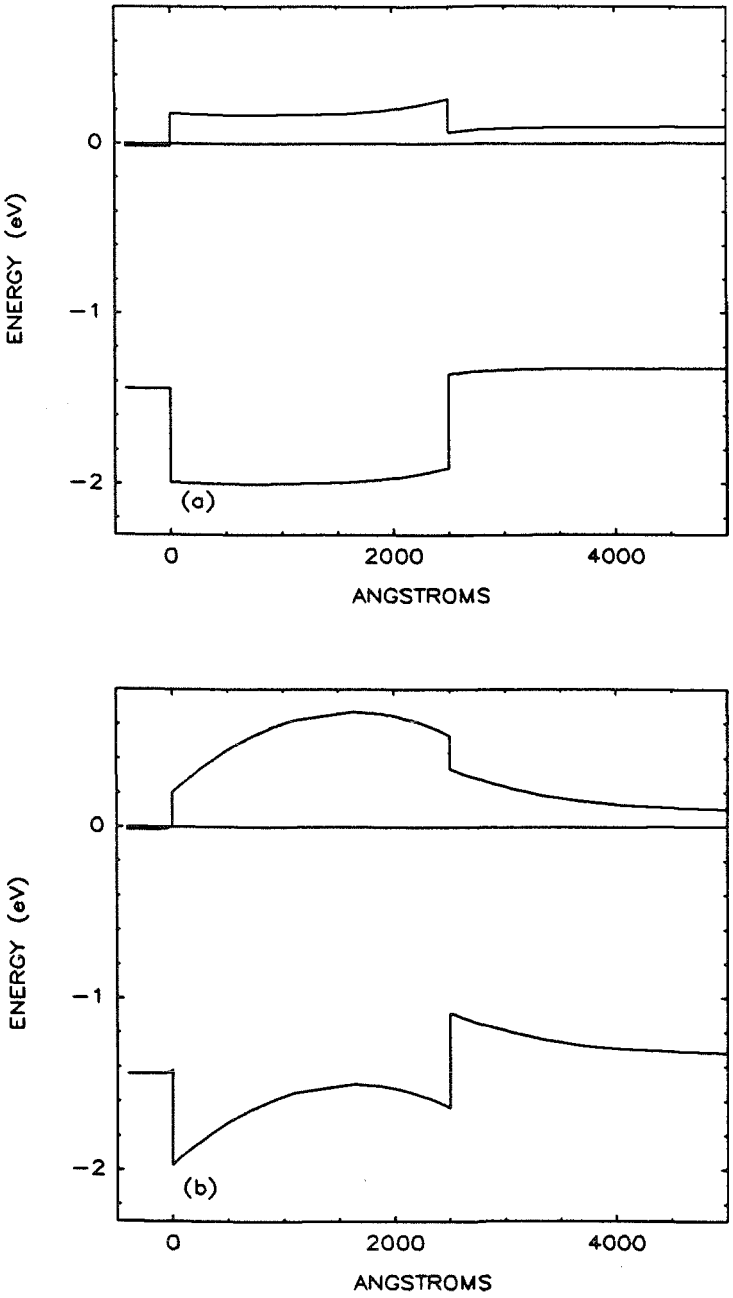

Figure 6.2: Equilibrium band diagrams for GaAs/AlAs/GaAs heterostructures. Left electrode doping is $3 \times 10^{18}\,\mathrm{cm}^{-3}$. Right electrode doping is $1 \times 10^{16}\,\mathrm{cm}^{-3}$. Barrier doping is $1 \times 10^{16}\,\mathrm{cm}^{-3}$ n–type in (a), and $2 \times 10^{16}\,\mathrm{cm}^{-3}$ p–type in (b). Band diagrams were calculated using a program written by Amikam Zur.

wet etching in a 4:1:1 solution of H_2SO_4 : H_2O_2 : H_2O. Preparation techniques have been described in Chapters 3, 4 and Appendix A.

6.4.2 C–V and I–V Measurements

C–V and *I–V* measurements were made using Hewlett Packard equipment. An HP4192 LF impedance analyzer was used for *C–V* measurements. An HP 4145 semiconductor parameter analyzer was used for *I–V* measurements. An HP 9816 computer controlled both instruments via a program written for the purpose. The impedance analyzer was capable of monitoring the phase angle of the impedance. The phase of the impedance was monitored during data acquisition. All data were acquired digitally. Low-temperature measurements were performed using an MMR Technologies refrigeration station. Incandescent light was the source for illuminated measurements. Bias polarities are as follows. Positive voltage application to the degenerate GaAs top layer is referred to as forward bias. Conversely, negative voltage applied to this layer is referred to as reverse bias. Positive current is observed in forward bias, and negative current is seen in reverse bias. Data were found to scale with area over the range of mesa diameters available.

6.4.3 DLTS

Deep-level transient spectroscopy (DLTS) measurements were performed using a method described by Lang.[15,16] An HP-85 computer was used to control an MMR Technologies refrigeration station. The computer was used to acquire data from a double boxcar integrator, which sampled the capacitance output from a Boonton 72DB capacitance meter operating at 1 MHz. More details of the measurement technique and theory may be found elsewhere.[17,18]

6.5 Capacitance Results and Discussion

The GaAs electrode regions on either side of the AlAs barrier are asymmetrically doped. The top electrode is at least 200 times more heavily doped than the back side GaAs layer. This doping asymmetry means that screening effects in the top layer of GaAs can be neglected to first order. This point is graphically illustrated by Fig. 6.2. A lot of information about such a device can be obtained by studying its capacitance–voltage (C–V) behavior. The capacitance of the MOS analog after which the device is fashioned can be used to try and understand the C–V.[3,19,20] Initially, one expects that the capacitance of the device would be the major component of the impedance. The doping of the nondegenerate electrode can be determined by plotting $(1/C)^2$ versus V.[3] If inversion occurs, it should be evidenced in the 1 MHz C–V as a region of constant capacitance in reverse bias.

6.5.1 Room-Temperature Observations

Nonilluminated Measurements

In Fig. 6.3 we present C–V data for two samples. These data are representative of all the samples studied. General features of the data include hysteresis for data taken without illumination. With illumination, no hysteresis is evident, and an enhanced peak near zero bias is apparent. We now discuss particular features of the nonilluminated data illustrated in Fig. 6.3.

For reverse biases in excess of a few volts, all the curves look more or less the same. Depletion is exhibited to the breakdown voltage of the device. This voltage ranged between 15 and 25 V for sample H399, and from 40 to 50 V for sample H464. High-frequency C–V data for an MOS structure usually become constant beyond a few volts of reverse bias, due to the creation of an inversion layer of

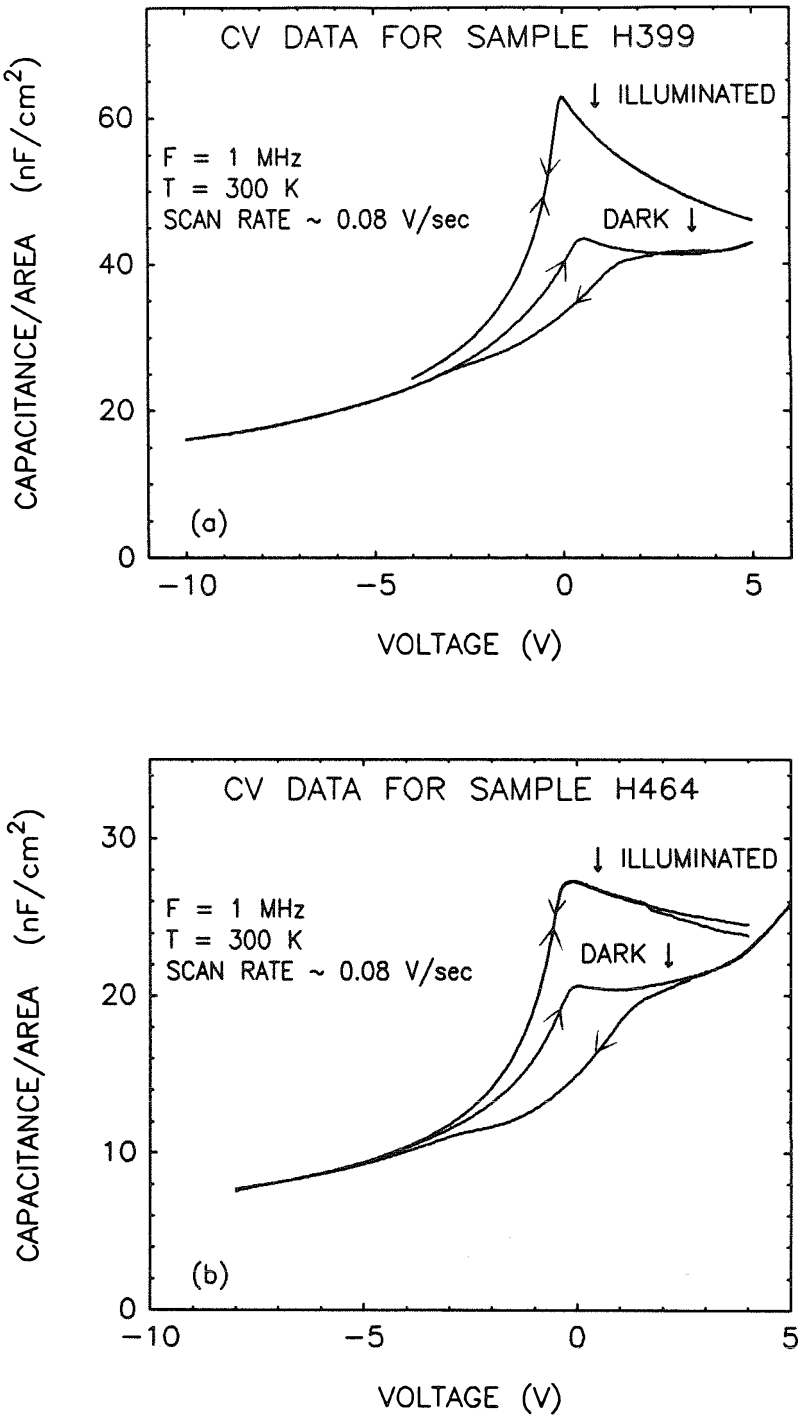

Figure 6.3: Representative C–V data for AlAs single-barrier samples. (a) Data for sample H399. Direction of bias sweep is indicated by arrows. (b) Similar data for sample H464.

minority carriers at the interface. This inversion layer prevents further expansion of the depletion region.[3] Inversion would be expected in these samples for reverse biases of about 5 V. No evidence of inversion is seen in the C–V. Lack of inversion may be due to poor confinement of the minority carriers by the valence band of the AlAs.[11]

In nonilluminated forward-bias data, there is some leveling off of the C–V curve, due to accumulation of electrons at the AlAs barrier. The capacitance at this bias is roughly that of the AlAs barrier,[§] according to the formula:

$$C = \frac{\epsilon}{d}, \tag{6.1}$$

where C is the capacitance per unit area, and ϵ is the dielectric constant of the semiconductor, multiplied by the permittivity of free space, and d is the barrier thickness. Forward-bias conduction in most samples became significant at voltages of 5 to 8 V, as measured from the phase angle of the impedance.

Near zero bias, hysteresis is evident in C–V curves taken in darkness. When voltage is swept from reverse to forward bias, the capacitance is higher than when bias is swept the other way. This behavior can be explained by the presence of electron traps near the interface between the lightly-doped GaAs and the AlAs, or with traps in the AlAs. The two charge states of these traps are positive (when empty) and neutral (when full). Thus, traps contribute to the charge in the depletion layer when they are empty, but not when they are full. Therefore, the capacitance of the structure will differ depending on the prevailing trap occupation state. A pictorial explanation of this effect is presented in Fig. 6.4.

Consider the case in which voltage is swept from reverse to forward bias, corresponding to points '1' through '4' in Fig. 6.4. Trap levels will be empty, positively charged. As the voltage is swept toward forward biases, the depletion width

[§]Thicknesses were determined by growth-rate estimates and scanning electron microscope measurements.

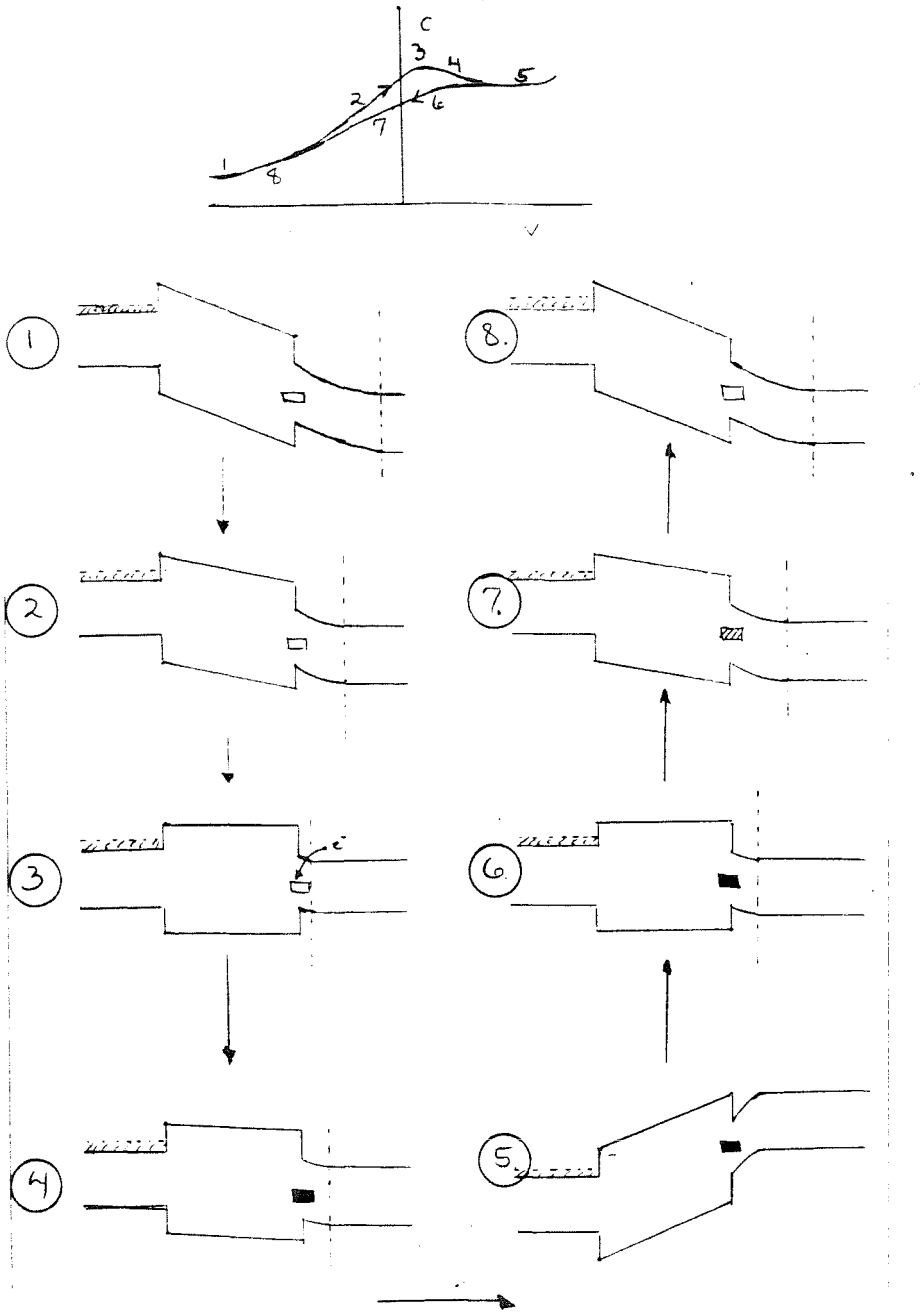

Figure 6.4: A pictorial representation of the C–V curve and schematic band diagrams for various points on the C–V curve. Band diagrams corresponding to various points on the C–V curve are illustrated. Occupied traps are represented as a solid box, with empty traps being hollow. The edge of the depletion region is denoted by a dashed line.

shrinks. When the edge of the depletion region, which is a few extrinsic Debye lengths wide,[21] sweeps over the spatial location of the traps, most of the levels fill, becoming neutral. This trap filling necessitates additional depletion of free carriers and a consequent decrease in capacitance. Capacitance stops dropping when the trap levels return to equilibrium with the applied bias.

We now discuss the case in which bias is swept from positive to negative values, corresponding to points '5' through '8' in Fig. 6.4. When bias is swept from positive to negative voltages, trap levels are initially filled. As the depletion region envelops the trap levels, they begin to empty. In the absence of illumination, this process is a thermal one. When voltage is swept fast enough, the population of filled levels will not be in equilibrium with the applied bias. Some levels that were empty during the reverse-to-forward bias sweep will now be filled, requiring additional depletion and a lower capacitance. The two curves meet when the number of empty levels reaches equilibrium.

This hysteresis depends on the data-acquisition rate. For slow acquisition, decreased hysteresis is observed. In Fig. 6.5, data for sample H399 are illustrated. Data were acquired sufficiently slowly to yield no hysteresis and no peak in the capacitance. Data for this figure were obtained at 0.5 V resolution, with 5 minute delays between successive points, in the dark. Some samples for which data of this type were taken continued to show hysteresis, but peaks were absent. For more rapid sweep rates than those depicted in the text, the size of the hysteresis increases somewhat, and the peak of the forward-going curve shifts to a slightly higher voltage.

Illuminated Measurements

Consider the illuminated C–V data illustrated in Fig. 6.3. When light is present, a nonthermal means of emptying traps is provided. Therefore, no hys-

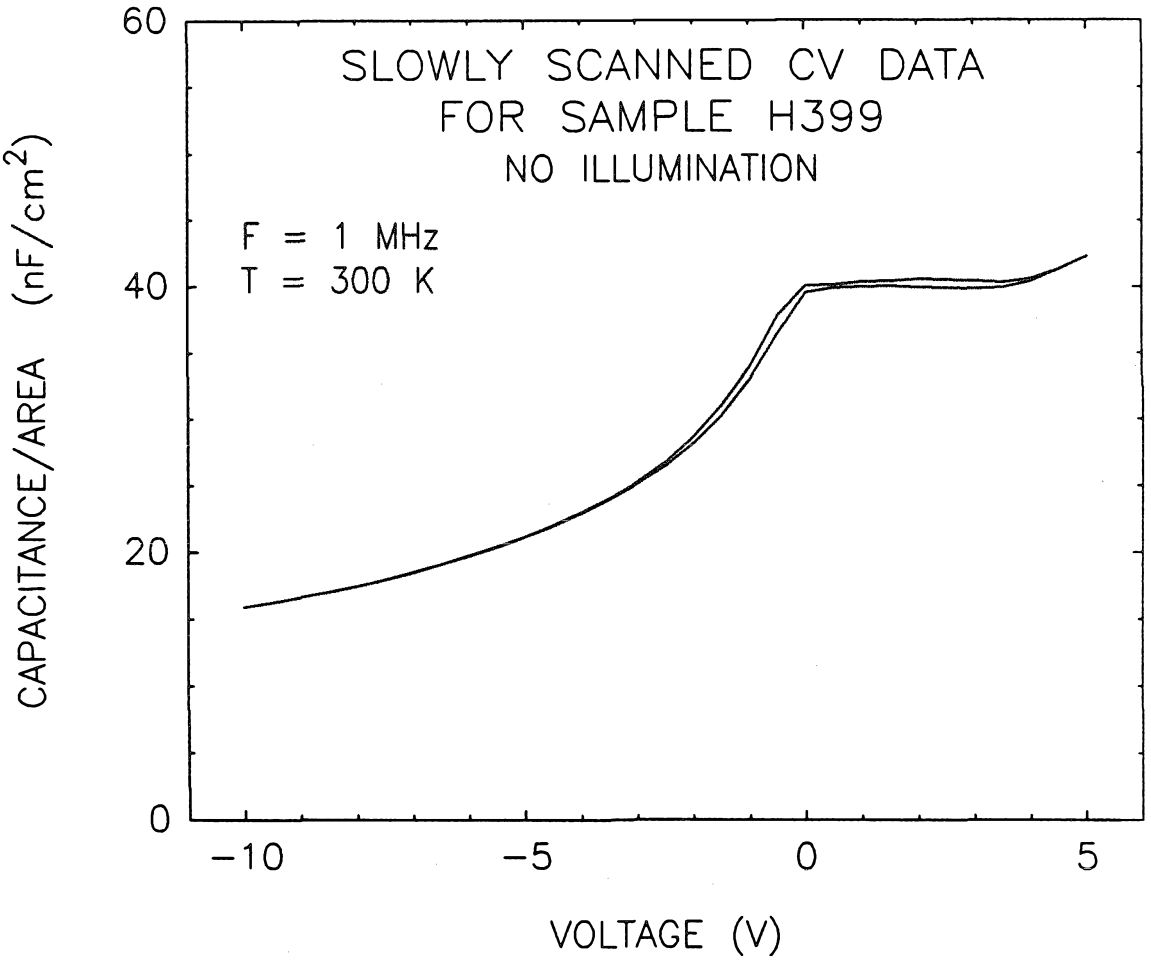

Figure 6.5: Slowly scanned C–V data for sample H399. The resolution is 0.5 V, with a 5 minute wait between successive points. Voltage was swept in both directions.

teresis is observed in illuminated C–V curves. Capacitance is greater because of increased charge in the depletion region due to illumination. A peak continues to be observed because the electron distribution around the traps continues to change with bias, thus necessitating a change in trap occupancy. Factors that affect the equilibrium trap occupancy result in changes in the size of the illuminated capacitance peak. These include temperature and the amount of light falling on the sample.

Simple MOS theory cannot explain the peak in the capacitance seen in Fig. 6.3. A more detailed theory, which takes into account the screening in the GaAs, semiconductor–insulator–semiconductor (SIS) theory can be considered.[20] This theory does predict capacitance peaks, which arise due to carrier depletion on both sides of the insulator. SIS theory mandates that a $(1/C)^2$ vs. V doping profile in forward bias yield a doping value equal to that of the top electrode (about $1 \times 10^{18}\,\mathrm{cm}^{-3}$). Further, the peak capacitance should be that predicted by Eq. 6.1. Neither is the case, suggesting that the peak in the capacitance is deep-level related.

It is interesting to note that the capacitance at the peak of the illuminated C–V curve is greater than that predicted by Eq. 6.1. A conclusive explanation for this has not been found. However, this observation suggests that traps are distributed through the AlAs. If charge is modulated *inside* the AlAs barrier, a capacitance exceeding the simple barrier capacitance would be possible. The increased current flowing in the structure during illumination may also be important. Many illuminated C–V curves exhibit a dip in the phase angle (of a couple degrees away from 90) of the impedance as the capacitance moves through its illuminated peak. Additional studies of the behavior of the sample under illumination were made and are reported in Chapter 7.

6.5.2 Pulsed Illumination Studies

The selective use of illumination to depopulate trap levels provides a way in which to test our theory of trap-induced hysteresis. This test involves the sudden exposure of the sample to illumination during a reverse-going capacitance sweep. As mentioned, this curve lies at lower capacitance than the forward-going sweep, because the trap levels do not empty rapidly enough to remain in equilibrium with the applied bias. By briefly exposing the sample to light during such a sweep, the trap levels can be depopulated. If the pulse of light occurs after the depletion region has enveloped the traps, they will not fill with electrons. After the pulse of light, the capacitance should therefore decay to values associated with the *forward-going* curve rather than the reverse-going one.

These data are illustrated in Fig. 6.6. The data in this figure are identical to those shown in Fig. 6.3(a), with the addition of one C–V curve. This curve was obtained by sweeping voltage from forward to reverse bias and briefly exposing the sample to light at about 0.3 V. This curve links all the data together, illuminated, forward-going, and reverse-going. This test supports the trap-level explanation for the hysteresis and capacitance peaks. Several samples were tested in this way and behaved as illustrated in Fig. 6.6.

6.5.3 Variable Frequency Studies

The capacitance of one sample was investigated as a function of measurement frequency in the dark. The hysteresis effect remained almost constant for AC oscillator frequencies ranging from 10 kHz to 5 MHz. In fact, the entire C–V curve changed very little with measurement frequency. This behavior is very different from studies of MIS devices in GaAs, where large variation of capacitance with frequency was observed.[5,6] The lack of capacitance variation over the measured frequency range indicates that the traps have a very slow emission rate, which

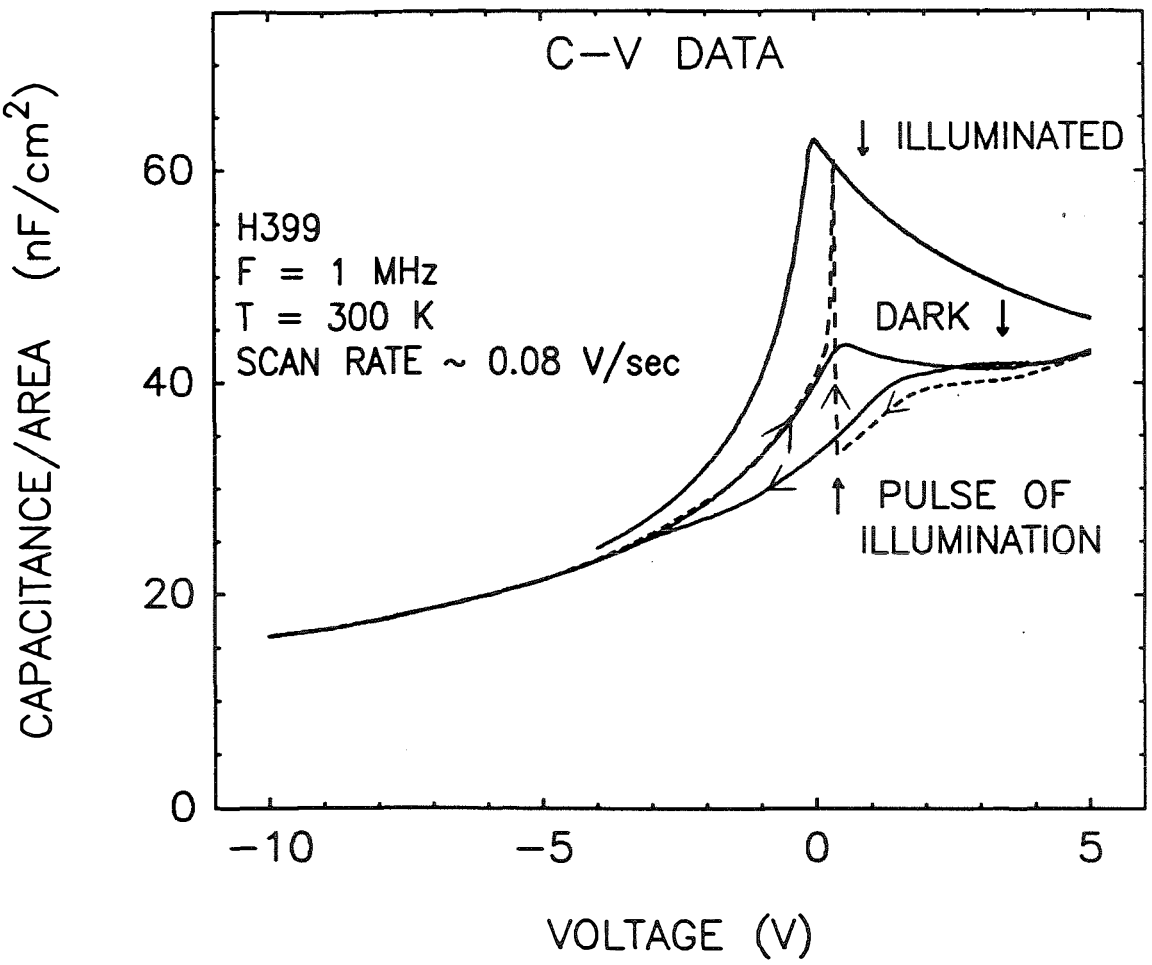

Figure 6.6: *C–V* data for Sample H399, with pulsed illumination curve. Except for the dotted curve, data are the same as in Fig. 6.3(a). The dotted curve was obtained by application of a pulse of light at the point indicated by the arrow.

is not capable of following the imposed frequency. Low-frequency, or quasi-static C–V measurements might prove interesting with these samples.

6.5.4 Variable-Temperature Studies

Temperature dependent studies of these samples were made. As temperature is increased, the energy available to modulate the trap population thermally is increased. The increasing energy should cause the hysteresis observed in Fig. 6.3 to decrease as temperature increases. In Fig. 6.7 we present data for sample H399 at elevated temperatures. As expected, the hysteresis decreases.

In Fig. 6.8, we present C–V data for two samples, at 300 and 77 K. The hysteresis described previously increases as temperature decreases. Additionally, the peak in the forward-going curve shifts to more positive voltage and is more pronounced. This observation can be explained by the longer emission time of the deep levels and the more sharply defined depletion edge,[¶] both of which are obtained at lower temperatures.

Some information about the deep levels can be obtained from Fig. 6.8. Initially, one observes that they must be electron traps, since they are positively charged when empty. Also, one observes that the trap emission time should be very long. Rough estimates indicate several seconds. A rough concentration estimate can be made by assuming that the difference in capacitance between the forward- and reverse-going curves is due to additional depletion of the GaAs. This difference can be written

$$\frac{1}{C_2} = \frac{1}{C_1} + \frac{\delta w}{\epsilon_s}\,, \tag{6.2}$$

where C_1 is the capacitance of the forward-going curve, C_2 is the capacitance of the reverse-going curve, δw is the additional depletion taking place in the reverse-going

[¶]The Debye length $L_D \equiv \sqrt{\frac{\epsilon kT}{q^2 N_d}}$ is proportional to $T^{1/2}$.[3]

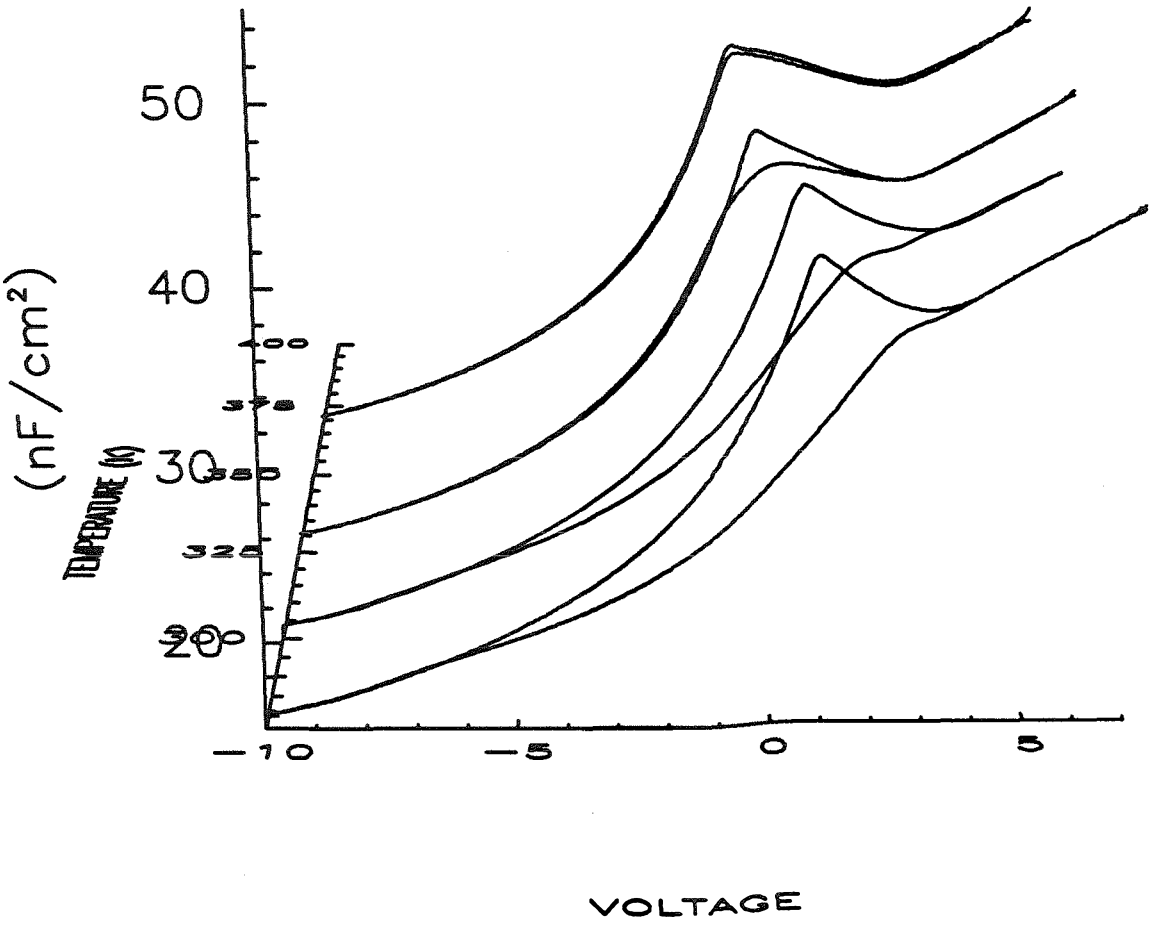

Figure 6.7: Three-dimensional plots of C–V data at a variety of temperatures for sample H399. Hysteresis decreases with increasing temperature. The sweep rate was about 0.08 V/sec in all cases. The decrease in hysteresis is due to the increased trap emission rate at higher temperatures.

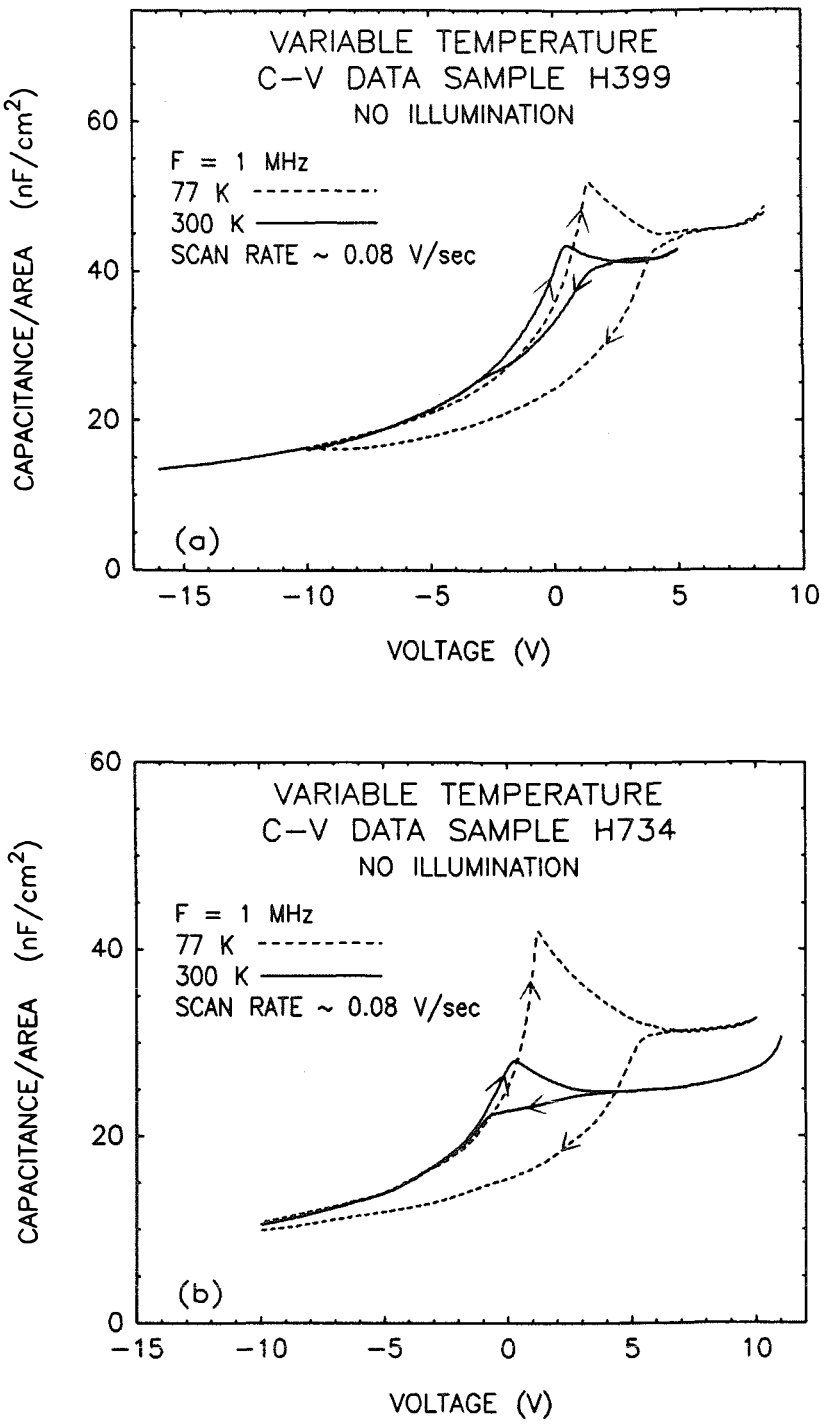

Figure 6.8: 300 K and 77 K data for samples H399 and H734, representative of all samples. Direction of bias sweep is indicated by arrows. Note the increase in hysteresis for 77 K data and the shift of the capacitance peak to higher bias levels.

curve, and ϵ_s is the dielectric constant of GaAs. One obtains a value for δw

$$\delta w = \frac{\epsilon_s(\delta C)}{C_1 C_2} , \tag{6.3}$$

where $\delta C = C_1 - C_2$. Equating the charge contained in δw to a sheet concentration obtains a rough estimate for the sheet carrier concentration of the traps:[‖]

$$N_d \delta w = N_t , \tag{6.4}$$

where N_d is the donor concentration, and N_t is the trap sheet density. This estimate yields concentrations in the $10^{11}\,\mathrm{cm}^{-2}$ range for both samples illustrated in Fig. 6.8, at 77 K. 300 K estimates are somewhat lower (less than an order of magnitude), owing to the shorter trap emission time at higher temperatures.

In Fig. 6.8 the saturation capacitance of the forward-bias C–V increases as temperature decreases. Conventional theory predicts that capacitance should level off at a value predicted by Eq. 6.1. Barrier thickness for sample H734 (illustrated in Fig. 6.8(b)) was measured by a scanning electron microscope (SEM) to be about 2500 Å. The thickness prediction at 77 K is about 2800 Å; at 300 K the prediction increases to about 3600 Å. The decrease in predicted thickness with temperature suggests that the barrier is charged. Negative charge would deplete parts of the nondegenerate GaAs, resulting in lower saturation capacitance. This charge could come from ionized acceptors, implying that the barrier is actually slightly p–type. As temperature decreases, some of this negative charge will freeze out, lessening the depletion of the GaAs. Donor density in the nondegenerate GaAs is higher for sample H399 than for sample H734, explaining why the change in saturation capacitance with temperature is smaller for sample H399 (in Fig. 6.8(a)) than for sample H734.

[‖] We assume that the traps are located at the edge of the depletion region. Our concentration estimate thus represents a lower bound on N_t. See Ref. 16 for more details.

Tests of a sample in which the barrier was intentionally doped heavily with Mg were done. In this case the discrepancy between the SEM measurement and the thickness predicted from Eq. 6.1 was quite large. Room-temperature C–V predicted 4000 Å, whereas SEM measured about 1000 Å. A rough calculation, treating the AlAs/GaAs interface as a p^+n junction, yields sufficient depletion to account for this discrepancy.

Finally, one sample that was intentionally doped n-type was studied. This sample showed much higher levels of conduction than other samples. We therefore suppose that p-type doping, or deep level compensation, is important in creating high-resistivity AlAs barriers. This supposition is consistent with previous studies of oxygen-doped $Al_xGa_{1-x}As$.[11]

6.5.5 Capacitance Conclusions

The major results of the capacitance measurements described in this section are summarized here. Evidence for the presence of deep levels in the AlAs or at the interface between the AlAs and the lightly-doped GaAs was found. A test of this explanation was made, with light pulses. The frequency dependence of the capacitance was investigated. No frequency dependence was found. Temperature dependence of the C–V was observed and qualitatively explained. Order-of-magnitude estimates for the sheet concentration of trap levels were made ($10^{11}\,cm^{-2}$). Evidence for acceptors in the AlAs was found.

No inversion was observed in any sample. There are two possible reasons. Initially, minority carriers may not be generated. This lack of generation demands that the Fermi level never reach the valence band edge, but remain 'pinned' near mid-gap at the AlAs interface. Pinning requires the presence of about $10^{14}\,cm^{-2}$ interface traps.[22] This amount is three orders of magnitude higher than the rough estimate of the sheet trap density. The other possibility is that carriers

are generated, but are not well confined by the valence band of the AlAs. The dominant leakage mechanism would likely be Fowler-Nordheim tunneling through the triangular AlAs barrier.[23] We did not see a sudden increase in leakage current at voltages that might correspond to inversion. One would not expect to see this leakage, because it would be masked by similar leakage from the conduction band of the degenerate GaAs top electrode.

6.6 DLTS Results and Discussion

Deep-level transient spectroscopy (DLTS) is a technique whereby localized impurity states in a semiconductor can be investigated. It was developed by Lang and has been widely used.[15,16] It can be applied to structures in which depletion regions can be created. Therefore, it can be used on our structures. Its results can be used to corroborate and expand the information obtained from capacitance measurements. The particular experimental apparatus used for these studies has been described elsewhere.[17,18]

In DLTS a sample is maintained at a particular reverse bias, which depletes part of the sample. Bias pulses are applied, which modify the occupation of the trap level. When the pulse is removed, the traps return to equilibrium with the quiescent reverse bias. Experimentally, this return to equilibrium can be observed as a capacitance transient following removal of the bias pulse. This capacitance transient is sampled with a boxcar integrator to obtain trap characteristics. A simple model of deep levels completely characterizes the trap with two parameters: the capture cross section and the activation energy. The expression for the emission rate of the trap is[15]

$$e_n = \sigma N_c v_{th} e^{-\Delta E/kT}, \tag{6.5}$$

where e_n is the emission rate in $\sec^{-1}$, σ is the capture cross section of the deep

level, N_c is the effective density of states in the conduction band, v_{th} is the thermal velocity, and ΔE is the activation energy of the trap. DLTS can provide two other quantities of interest: the concentration and spatial location of the deep level.

6.6.1 Spatial Localization

Deep levels were observed in several samples. Two samples, H399 and H464, were studied in detail. Trap levels were spatially localized to the AlAs layer, or the interface between the AlAs and the lightly-doped GaAs.

This conclusion is supported by data, some of which are presented in Fig. 6.9. This figure presents DLTS trap signatures taken at a variety of pulse heights, at a fixed quiescent bias and rate window. The fact that the peak moves downward confirms that a majority carrier trap is being observed, which for this sample corresponds to an electron trap. No traps were found in the lightly-doped GaAs. The data in Fig. 6.9 represent the only bias ranges over which traps could be seen. As can be seen, trap signature increases as pulse voltage becomes more positive. For these voltages, electrons are accumulated near the AlAs interface. The extent to which the AlAs is probed is not known. A quiescent reverse bias of -1 V corresponds to a depletion depth of about 1500 Å. The conclusion to be reached is that the deep levels are localized to within at least 1500 Å of the AlAs and are probably much more localized than this, since no trap signature is observed until pulses of -1.25 V are applied.

Similar spatial localization testing was done on sample H399. These tests localized deep levels to within 500 Å of the barrier and showed that the DLTS capacitance transient increased and then decreased in magnitude as quiescent voltage was brought into forward biases of about 4 V. Further, the DLTS capacitance transient changed its time constant as the quiescent reverse bias was brought into forward bias. This result suggests that the traps are distributed in the AlAs but

that forward conduction in the structure is affecting the device.

In addition to the increase in DLTS peak with pulse voltage, two other points should be made about the data shown in Fig. 6.9. The first is the shift in peak location with increasing pulse height. A simple bulk level does not exhibit this behavior. If the AlAs were an ideal insulator, the peak shift would indicate interface states,[24] because additional interface states distributed through the band gap would participate in the filling and and emptying process. Of course, the AlAs is not a perfect insulator, and other possibilities exist that could account for the peak shift. Multiple bulk levels, traps distributed in the AlAs and the GaAs, as well as a mixture of bulk and interface states, could account for the peak shift.

The final interesting feature of the data exhibited in Fig. 6.9 is the temperature at which the DLTS signal is peaked. The temperature is high and suggests that a lot of energy must be provided to empty the trap level efficiently. The high temperature is consistent with a long-lived state, and one would expect a long emission time. Long emission times are consistent with a large activation energy or a small capture cross section.

6.6.2 Activation Energies

The activation energy of the trap level can be determined from the trap signature using a method first described by Lang.[15] Each particular set of rate windows, or times t_1 and t_2 at which the capacitance transient is sampled, defines a peak emission rate for the trap. Plotting the log of this emission rate against $1/kT$ yields a line whose slope is related to the activation energy of the level and whose intercept provides capture cross section information. This Arrhenius plot can be corrected for the temperature dependence of the exponential prefactor in Eq. 6.5 by dividing the experimental emission rate by the square of the temperature at which it occurred. Two samples, H399 and H464, have been studied in

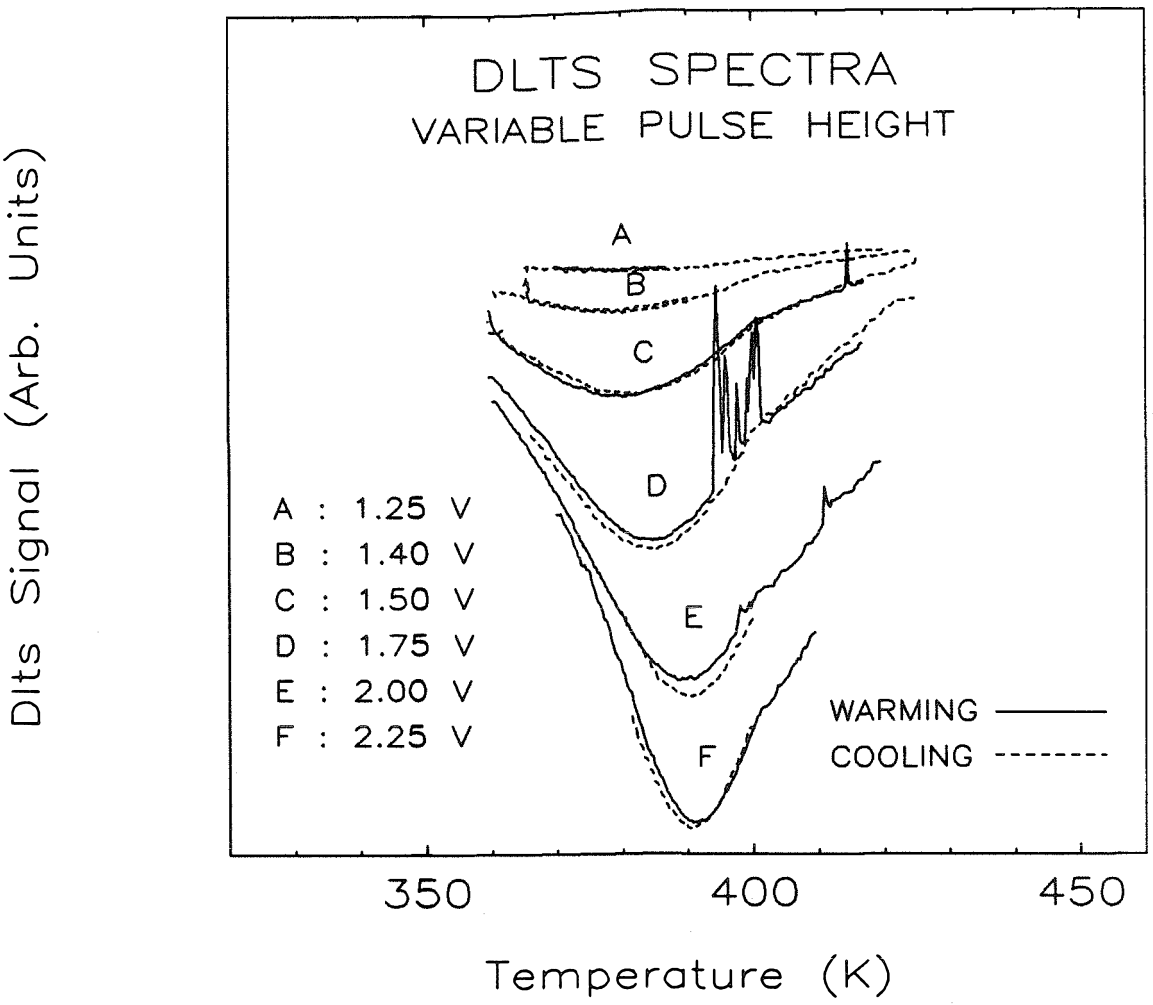

Figure 6.9: DLTS trap signatures for sample H464. Quiescent reverse bias, trap filling pulse width, and capacitance sampling rate windows are fixed. DLTS pulse bias magnitude is varied as indicated. Warming and cooling runs are presented. Quiescent reverse bias is -1.0 V. Note the shift of DLTS peak and increase in peak size with increasing pulse height.

this way. Since the peak shift phenomena observed in Fig. 6.9 is relatively small, this measurement still conveys information.

Fig. 6.10 presents activation energy plots for samples H399 and H464. The activation energy for both levels was about 500 meV, to within an error of about 70 meV. Since a relatively narrow range of emission rates was obtained, the capture cross section information is not very reliable. These capture cross sections are consistent with a long trap emission time (low emission rate). A better way to obtain capture cross section would examine the DLTS signal as a function of trap filling pulse *width*.[15] The main point of the data presented in Fig. 6.10 is that both samples exhibited very nearly the same DLTS behavior, suggesting that the same level is present in all samples.

Concentration estimates for the trap levels observed in both samples have been made using methods introduced by Lang.[15] These concentration estimates yield values of about $1 \times 10^{15}\,\mathrm{cm}^{-3}$ for the deep level. This value underestimates the true number of deep levels, especially when the concentration of levels approaches that of the shallow donor concentration. C–V data indicate that this is probably the case.

6.6.3 Conclusions

Some conclusions can be drawn about the trap level. We know that it occurs in the AlAs, or at the interface. We know its approximate activation energy. We know that the same level is probably present in all the samples. The emission rate of the trap is very slow, and it is probably the source of photosensistive capacitance behavior. A level having these properties has been observed in $Al_xGa_{1-x}As$. The level is referred to as a 'DX' center, because it is believed to be associated with a donor and a vacancy complex. Several authors have observed this level, but is has not been extensively studied in AlAs. One author reports a DX cen-

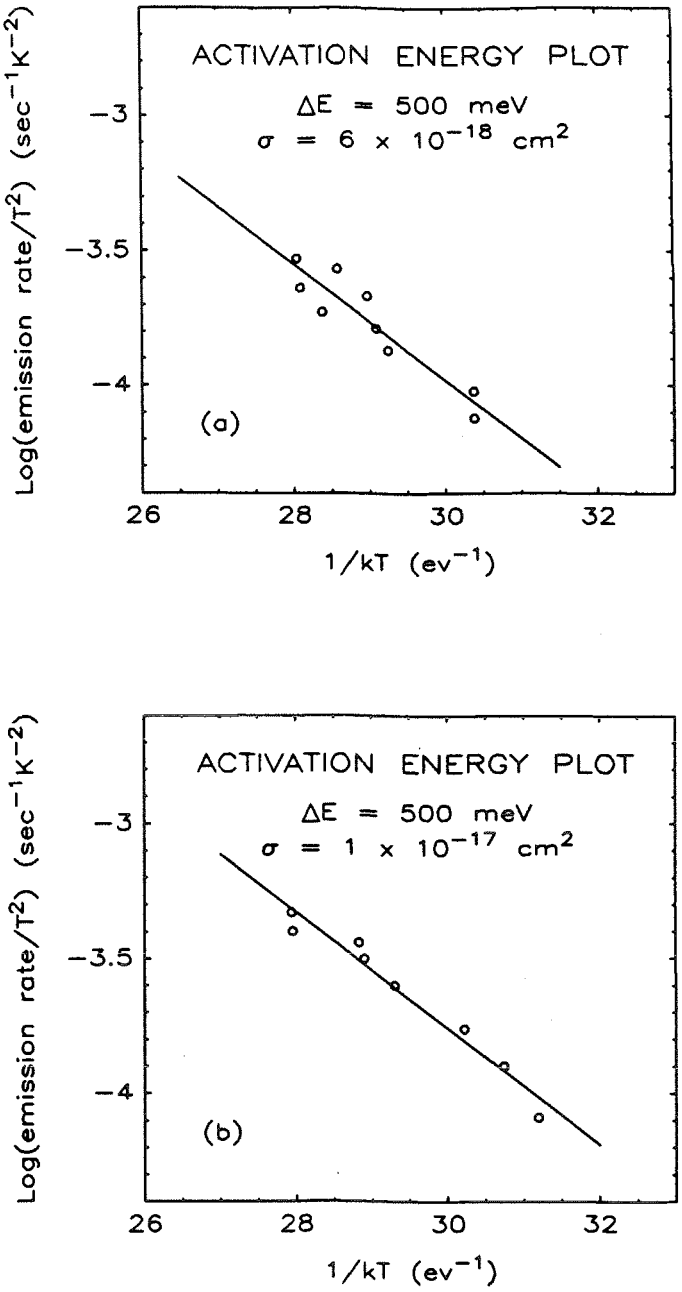

Figure 6.10: T^2-corrected activation energy plots for two samples, H464 and H399. ΔE is the activation energy. Standard error in ΔE is 70 meV for (a), and 40 meV for (b). A 95 percent confidence interval for ΔE is 500 ± 100 meV for both samples. σ is the capture cross section. Both samples show very similar trap characteristics.

ter in $Al_xGa_{1-x}As$ having a 500 meV activation energy.[25] Since Se doping is used, memory effects could account for the presence of donors in the AlAs. It is also possible that the level is oxygen related. A 640 meV level is associated with oxygen in $Al_xGa_{1-x}As$[11], and oxygen is often used to create high-resistivity $Al_xGa_{1-x}As$.[11,26] These layers were created by oxygen introduction in an MBE machine or by oxygen implantation after MBE growth. It should be noted that the MOCVD growth environment is highly reducing, making it difficult to imagine how significant amounts of oxygen could be unintentionally incorporated in our AlAs films.

6.7 Current–Voltage Measurements

This section describes the nonilluminated current voltage (I–V) behavior of our samples. The current through the structure when not illuminated is very low, typically below a nanoamp. Current density values below 10^{-8} A/cm^2 could be obtained for voltages ranging from 4 V to −20 V at room temperature for some samples.

Closer examination of the current near zero bias revealed interesting behavior. Fig. 6.11 presents I–V data for sample H735 taken without illumination. Hysteresis is seen in the I–V near zero bias. This type of hysteresis was observed in all of the samples. Consider the curve obtained by sweeping voltage from negative to positive values. With the sample in reverse bias, it was briefly exposed to light. As voltage becomes positive, a sudden increase in current is observed. This increased current remains at an almost constant level until large-scale conduction begins. The current step is not observed when the I–V curve is obtained by sweeping voltage in the other direction.

Our results can be explained by the same deep levels whose presence was ev-

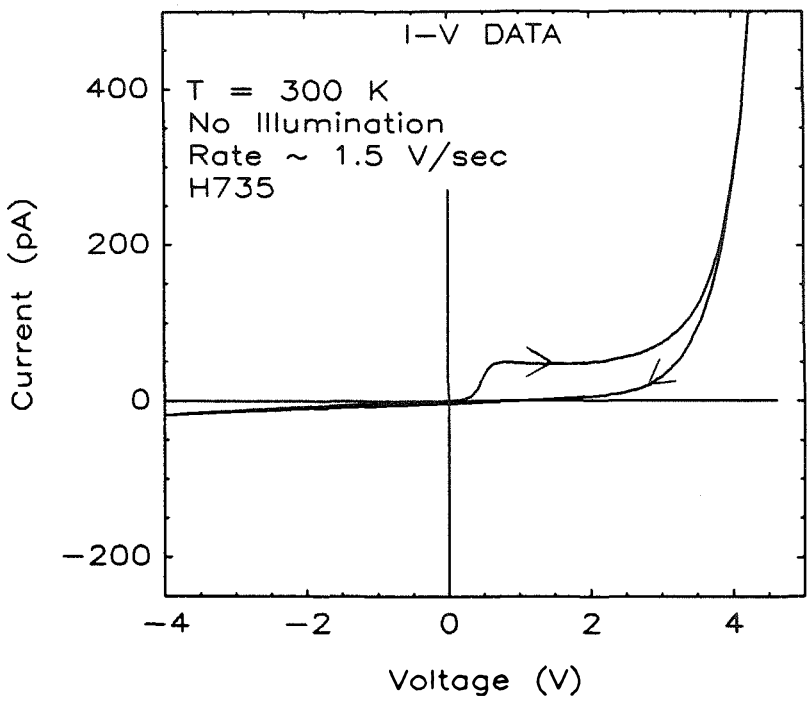

Figure 6.11: *I–V* data for sample H735 taken in darkness. Direction of bias sweep is indicated by arrows. Note the hysteresis in the characteristic.

idenced by *C–V* and DLTS studies. If the sample is illuminated in reverse bias, trap levels are emptied. They remain empty because no electrons are around to fill them. Thus, the light pulse provides a known initial state for the traps. As voltage is swept toward forward bias, electrons are brought near the spatial location of the deep levels, which begin to fill. As they fill, the number of electrons in the measurement circuit decreases. This rate of change of charge is the current enhancement observed.

When *I–V* data are obtained starting in forward bias, electrons are initially accumulated at the heterojunction interface, and traps are full. As the electrons are depleted from the area of the trap levels, the traps begin to emit electrons to return to equilibrium with the applied bias. This process is slow and does not produce a sudden change in charge. Therefore, no current jump is observed for

this direction of bias sweep.

An estimate of the number of deep levels required to create this effect can be made. The region under the enhanced current step in Fig. 6.11 can be approximated as a rectangle. The area of this rectangle can be converted to a charge, and hence to a sheet concentration:

$$N_t = \frac{I_s(\delta V)}{ARq}\,, \tag{6.6}$$

where $I_s \sim 40$ pA is the size of the current step, $\delta V \sim 2$ V is the voltage range over which hysteresis is evident, A is the area of the device (350 μm diameter mesas), R is the rate at which voltage is changed, and q is the electronic charge. This relatively crude model yields a value of $3 \times 10^{11}\,\mathrm{cm}^{-2}$ for N_t. This is in reasonable agreement with values obtained from C–V estimates.

The hysteresis effect is a function of the time allowed for the traps to empty in reverse bias. The time evolution of the current step is illustrated in Fig. 6.12, at 160 K. The leftmost current step was obtained in a manner similar to that illustrated in Fig. 6.11; by exposing the sample to light in reverse bias. After sweeping to +5 V, another scan was taken after a known time delay, during which the sample was held at zero bias. Various delay times were tested. The reason that the current step moves to higher biases relates to the trap emptying rate. After sweeping to forward bias, traps are completely full. If bias is then immediately returned to negative values and swept forward again, the voltage at which the current jump appears shifts to more forward values because all of the trap levels have not emptied. If about 40 seconds elapse between successive scans, all the trap levels will be almost completely empty, and a reverse-to-forward bias scan reveals a current step at low bias levels. Thus, a rough time constant of about 30 seconds is obtained for the trap emission time.

This hysteresis is a function of temperature and sweep rate. Fig. 6.13 illustrates the hysteresis effect in sample H735, as a function of temperature and sweep rate.

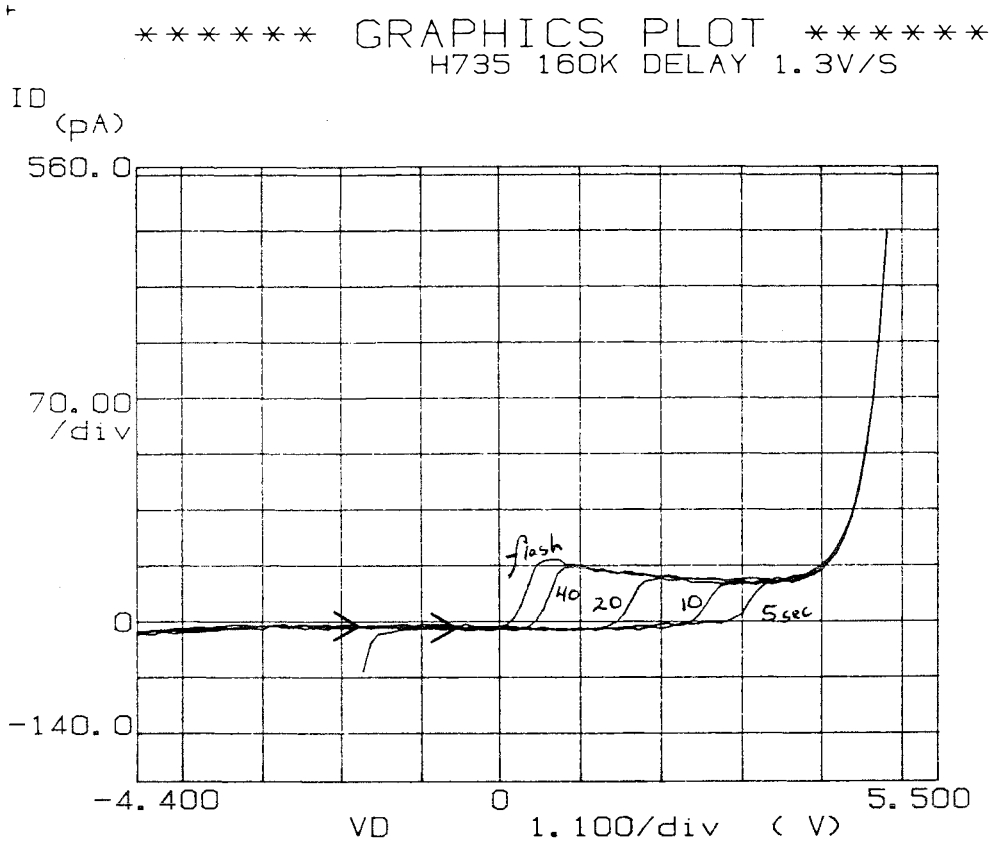

Figure 6.12: *I–V* curves for sample H735, at 160 K. Voltage is swept from reverse to forward biases. The labels indicate the amount of time elapsed between successive scans. The *I–V* curve with the leftmost current step was obtained by exposing the sample to light while in reverse bias. The indicated delay was introduced prior to taking a successive scan. These data indicate that the trap emptying time is about 30 seconds.

The faster rate, presented in Fig. 6.13(b), was obtained with less averaging by the HP4145, and thus is noisier than the more slowly acquired data shown in Fig. 6.13(a). For each of the curves shown in Fig. 6.13, the sample was briefly exposed to light in reverse bias, to provide a known initial state for the traps. The exact point at which the sample was illuminated will determine which levels are available to participate in the effect. The variation in onset voltage observed in Fig. 6.13 is due to this effect. No systematic variation in onset voltage with temperature was observed.

The height of the enhanced current step decreases as temperature decreases. The decrease can be explained by the general decrease in current as temperature goes down. The thermal energy of carriers decreases, making thermionic emission into the AlAs, and thermally assisted tunneling less likely. There are fewer electrons passing over the trap levels, and thus, the number that drop into traps to supply additional current is smaller as well. The decrease in current with temperature is demonstrated most clearly by the shift of large-scale conduction to higher bias levels with decreasing temperature. The decrease in current step size, coupled with the increase in voltage range of the hysteresis, combine to keep the trap concentration estimate (as calculated above) roughly constant in the $10^{11}\,\mathrm{cm}^{-2}$ range.

As the data-acquisition rate increases, the current jump becomes larger. This phenomenon can be seen by comparing Figs. 6.13(a) and (b). The step size increases with sweep rate because a faster sweep rate allows a more rapid change in the carrier population. This increased rate of change in the number of carriers results in a larger current jump. Since the number of traps being filled is about the same in each case, the trap concentration estimate, as obtained previously, is about the same for Fig. 6.13(a) and (b). Conversely, for very slow sweep rates the hysteresis is very small.

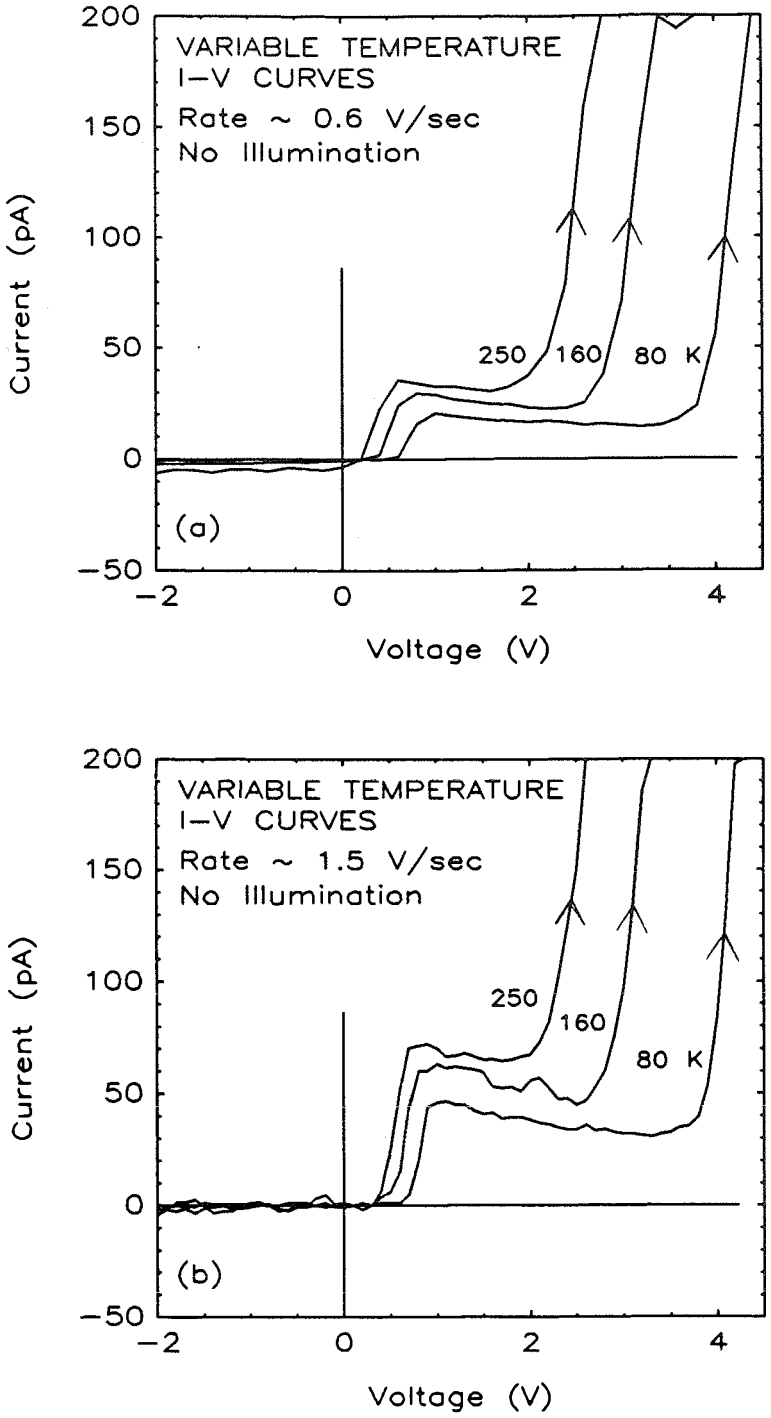

Figure 6.13: Variable-temperature I–V curves for sample H735 at different sweep rates. To empty trap levels, devices were exposed to brief illumination at about -4 V. Greater noise is observed in (b) because of decreased data averaging.

The presence of deep levels clearly influences the current at low bias levels. These levels make any electrical measurement of the band offset a questionable project at best. For this reason, activation energy determination of the band offset was not undertaken for these samples. However, a few more words on this subject are warranted. The current in the structure at low biases is very small and remains so for temperatures $77 < T < 300$ K. This prevents effective measurement of the barrier height with the activation energy method.[3] There are two possible reasons. The first is that the noise in the current measurement process is too large. The second is that the current is not dominated by thermionic emission. At higher bias levels ($\sim$4 V), plenty of current is present, but activation energy plots fail to show linear behavior in the 77 to 300 K range. This nonlinearity could be due to bias effects, or a continued failure of the thermionic model.

6.8 Conclusions

We have studied the behavior of MOCVD-grown GaAs/AlAs/GaAs heterostructures. C–V, I–V, and DLTS methods have been used. These measurements combine to provide a picture of the structures. They are low-current devices, having slightly p–type barriers. They do not exhibit inversion. Light sensitivity is seen in both the C–V and the I–V. Hysteresis is seen in *both* the nonilluminated C–V and I–V data. There are deep electron trap levels present in the samples, which have been localized to the AlAs barrier or the interface between the AlAs and the lightly-doped GaAs. The sheet concentration of these levels is in the $10^{11}\,\mathrm{cm}^{-2}$ range, and their activation energy is about 500 meV. This activation energy, the light sensitivity of the devices, and the extremely long emission time of the levels indicate that the traps may be DX centers.

Our results have implications for devices. The samples are obviously unsuited

Growth Geometry for Selected Single Barrier Samples

Sample No.	Growth Temp. (°C)	Top Layer d (μm)	Top Layer Doping (cm^{-3})	Barrier Thickness SEM (Å)	Barrier Thickness C–V (Å) (77/300 K)	Bottom Layer Doping (cm^{-3})
H399	782	3.6	3×10^{18}	2500	2000/2200	3×10^{16}
H464	782	0.8	2.5×10^{18}	4000	4100/3800	8×10^{15}
H490	782	1.1	2×10^{18}	1000	3000/4000	2×10^{16}
H734	795	4.3	1.5×10^{18}	2500	2800/3500	1×10^{16}
H735	795	3.2	1×10^{18}	1000	–/3300	1.5×10^{16}

Table 6.1: Physical parameters for selected single-barrier samples. Top layer thickness ('d') and doping (n-type) are indicated. Barrier thicknesses from SEM and C–V estimates are presented. The doping in the bottom layer is obtained via C–V profiling. Barrier doping in sample H399 is lightly n–type, heavily p–type in H490, and nonintentional in other samples.

for use as inversion-mode devices. Since AlAs has a larger valence band offset with GaAs than any $Al_xGa_{1-x}As$ barrier, this conclusion is relevant to $Al_xGa_{1-x}As$ barriers. Accumulation-mode GaAs-gate FETs may be possible with these materials, since they sustain several volts of forward bias before conducting. Investigations of the nature of the accumulation layer are needed, to examine this issue more carefully. The observed deep levels might degrade the performance of devices relying on conduction alongside the AlAs layer. These traps need to be greatly reduced if useful devices are to be made with our MOCVD AlAs layers. Should DX centers be the cause of the trapping, undoped AlAs might provide a means of eliminating the levels. Such growth requires a serious investigation of the proper conditions for MOCVD production of high-purity AlAs films.

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Chapter 7

Photoresponse Measurements of GaAs–AlAs–GaAs Heterostructures

This chapter describes an application of photoresponse techniques to the single-barrier GaAs/AlAs/GaAs heterostructures whose electrical behavior was reported in Chapter 6. Photoresponse combines optics and electronics. The electrical response of a material is measured as a function of the light falling on it.

There are two reasons for undertaking this work. The first is the insight into structural properties provided by photoresponse. A second reason relates to earlier work in the photoresponse of symmetrically doped, thin-barrier (< 240 Å) GaAs/AlAs/GaAs heterostructures. Such structures have been studied in detail, by T. E. Schlesinger.[1] The asymmetrically doped, thick-barrier GaAs/AlAs/GaAs heterostructures studied here exhibit a number of interesting differences from the symmetric case. These differences and their explanation are the second reason for undertaking the study.

7.1 Outline of Chapter

This chapter is divided into several parts. The first part summarizes major results and describes the experimental techniques used to obtain photocurrent and photovoltage data. The second part presents illuminated I–V data, which provide the basic framework for understanding the room-temperature photoresponse of the devices. The final part of the chapter presents photoresponse measurements as a function of incident light energy for three samples at a variety of external biases. These results are interpreted using the basic framework developed from the broad-band data.

7.2 Summary of Results

Incandescent illumination of the front of our samples at room temperature results in a zero-bias photocurrent consistent with electron transport from the back of the sample to the front. This result differs from earlier studies and led to further investigation. I–V curves were taken under incandescent illumination at a variety of temperatures. The size of the barrier and the asymmetric doping on either side of it are used to explain these results. The concept of a "collecting interface" is introduced to account for carrier energy loss and field in the AlAs.

Photocurrent per incident photon measurements were made as a function of incident light energy at a variety of external biases. Results for three samples are presented. Shifts in the wavelength at which photocurrent is peaked are seen with external bias. Changes in sign of the photocurrent are also observed. At particular biases photocurrent is double-peaked and two-signed. These features are correlated with top-layer thickness, top-layer doping, and barrier thickness. Consistency with earlier studies is demonstrated.

7.3 Experimental

Sample geometry, growth technique, and preparation methods have been described in Chapter 6. Ring-shaped Au-Ge contacts were defined on 350 μm diameter mesas. This allowed light to enter the device, without passing through the contact material.

Forward bias refers to positive voltage application to the ring contacts on the top of the sample. Positive current is observed in forward bias. This current is consistent with electron flow from the back of the sample to the front. Reverse-bias current corresponds to electron flow from the front of the sample to the back and is negative.

The photoresponse of a device may be quantified as an open-circuit photovoltage or a short-circuit photocurrent. Both measurements were made, and equivalent results could be obtained for either method. However, the photocurrent measurement was preferable, especially when external biasing was desired. Photocurrent measurements are presented in this chapter.

Photocurrent was obtained as follows. Light from a 1000 watt quartz halogen lamp* was directed through collection optics and an optical filter into a SPEX 1269 spectrometer. The spectrometer output was chopped at 27 Hz and focused through a microscope objective onto the top of a particular device. Synchronous detection of the short-circuit current arising from this illumination, using a current-sensitive preamp† and a PAR 124A lock-in amplifier, assured that only the photocurrent was measured. This photocurrent was divided by a measure of the incident photon density to obtain the photocurrent per incident photon. These data should be system invariant, removing lamp and spectrometer responses. External biases

*An incandescent source was chosen to allow a smooth, spike-free distribution of photons at all wavelengths of interest.

†PAR model 181A, sensitivity 10^{-7} to 10^{-9} A/V.

were supplied by an HP 6002A DC power supply. The sign of the photocurrent (or photovoltage) induced in the device was measured using an oscilloscope or a voltmeter.

7.4 Illuminated Current–Voltage Measurements

By exposing the sample to incandescent illumination and measuring the I–V characteristic, the basic photoresponse behavior of the sample can be obtained. The source of illumination for these measurements was an incandescent lamp.[‡] I–V data were obtained with an HP4145, as described elsewhere in this thesis. Temperature dependent measurements were made, using an MMR Technologies refrigeration station.

7.4.1 Room-Temperature Measurements

In Fig. 7.1 we present illuminated I–V data for sample H399 at room temperature. This is representative of all of the samples studied. Currents are about three orders of magnitude larger than when not illuminated. In forward bias, positive current enhancement is observed. In reverse bias, negative current enhancement is observed. It is interesting to note that the zero-bias photocurrent is positive, consistent with electron transport from the back of the sample to the front. This observation differs from earlier results.[2–5]

Free carrier absorption in the conduction bands of the GaAs can be used to explain the observed photocurrent. Such absorption, which involves a phonon, can result in carriers being directed toward the barrier with energies greater than the conduction-band offset of the AlAs. Carriers that travel from one side of the AlAs to the other contribute to photocurrent. The photocurrent is determined by a

[‡] A Dolan-Jenner quartz halogen fiber-optic illuminator, model 180.

gradient in the photoexcited carrier population across the AlAs barrier. There are a number of reasons for believing free carrier absorption to be responsible for the observed photocurrents, which will be described later.[§] Since the photocurrent is supposed to be caused by light, the photon flux falling on the device should exceed the electron flux in the device. Rough calculations of the two quantities show this to be the case (see Appendix B).

In thin barrier samples that are symmetrically doped, the driving force behind the photovoltage is explained very well as being due to differences in the number of optically excited carriers between the two GaAs layers. This explanation is successful for two reasons. First, little energy loss can take place across the thin barrier. Also, the symmetric doping ensures that (at zero bias) the AlAs band edges are at the same energy at both interfaces.

In the samples studied here, the AlAs plays an important role, because it is thick enough to allow significant energy loss to take place across it. For example, free carriers in GaAs that are excited by a 1.4 eV near band-edge photon can lose energy in a variety of ways. The main point is that energy loss is extremely rapid. A typical time scale for relaxation via optical phonon emission for a hot carrier in low temperature material is 100 femtoseconds (1 femtosecond $= 1 \times 10^{-15}$ seconds).[6] Assuming transport at 1×10^{7} cm/sec, the mean free path between scattering events is only about 100 Å. This mean free path would permit 20 scattering events, and an energy loss of about 1 eV. This very simplistic analysis is *not* intended to be quantitatively accurate, but rather to demonstrate that energy loss in the AlAs can be very significant. For thin-barrier samples (< 200 Å), energy loss in the AlAs would not be as important.

Energy loss in the AlAs makes the presence of an electric field in the AlAs important. Depending on the bias conditions, the conduction-band edge of the

[§]See also Ref. 1.

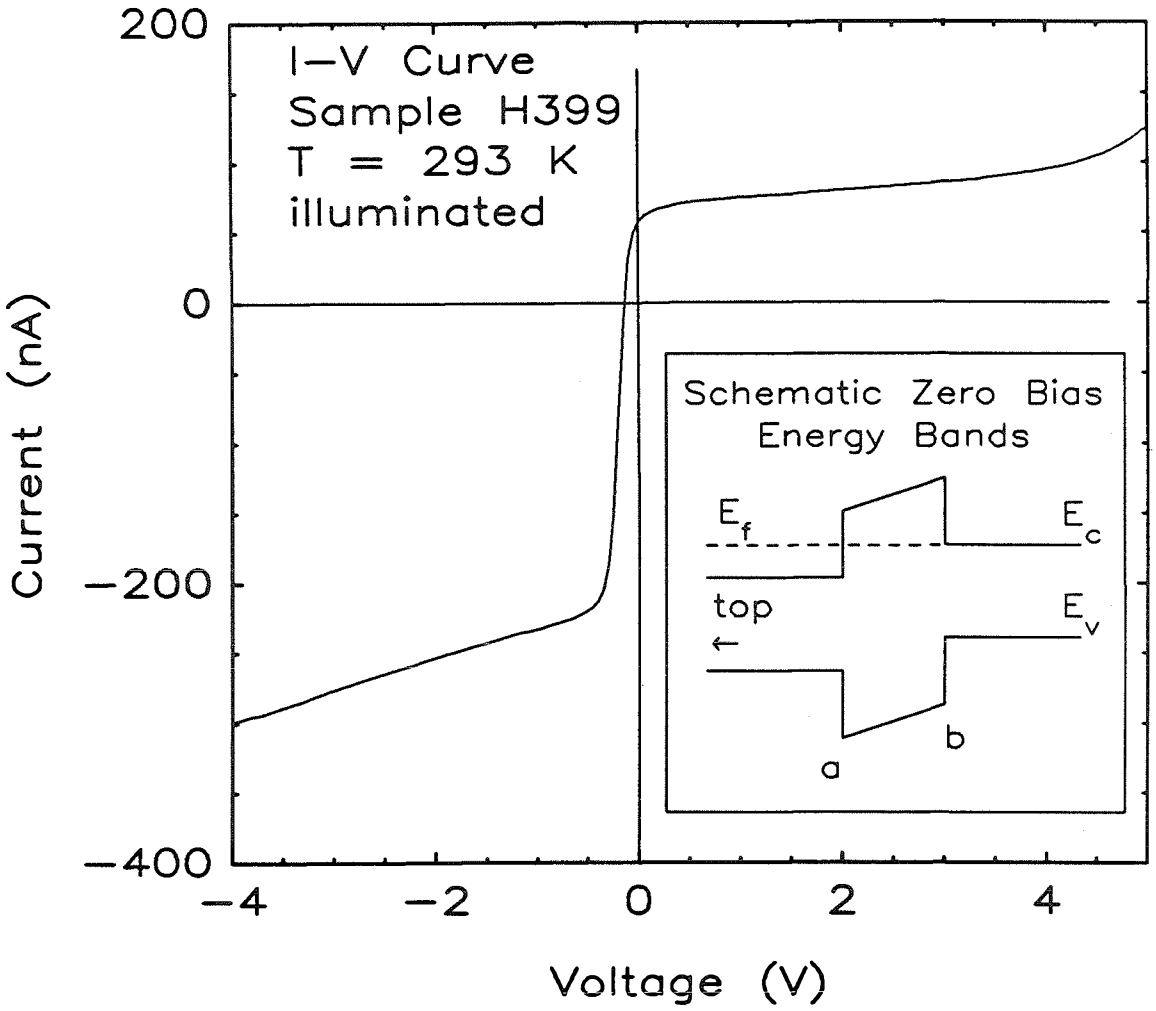

Figure 7.1: *I–V* data for sample H399 taken under illumination at room temperature. Zero-bias photocurrent is consistent with electron transport from the back of the sample to the front. The inset shows a schematic band diagram for the structure at zero bias. The schematic is not drawn to scale, does not include band bending, and is presented as a conceptual aid. Labels (a) and (b) refer to the two interfaces.

AlAs will be at a higher energy at either interface (a) or interface (b), as labeled in the inset of Fig. 7.1. If the interface happens to be the AlAs/GaAs interface (interface (b) in the figure), electrons from the back will be collected as soon as they cross this barrier, whereas electrons from the front must cross the entire AlAs region before reaching the highest energy barrier.

Positive external bias increases the height of the AlAs/GaAs interface (interface (b) in Fig. 7.1), as seen by front side electrons. We have two interfaces, but only one is important for current collection. It is the concentration gradient across this "collecting interface" that drives the photocurrent. We observe that at zero bias there is a built-in voltage across the AlAs due to the doping asymmetry in the structure. This built-in voltage fixes interface (b) as the collecting interface at zero bias, and explains why positive photocurrent is observed at zero bias.

The built-in voltage across the AlAs is essentially the Fermi degeneracy of the top electrode, since the back electrode is nondegenerately doped. This degeneracy can be expressed as

$$E_f - E_c = \left(\frac{3N_d\pi^2}{2\sqrt{2}}\right)^{2/3} \frac{\hbar^2}{m^*}, \tag{7.1}$$

where N_d is the doping of the electrode region. For a doping of $3 \times 10^{18}\,\mathrm{cm}^{-3}$, $E_f - E_c$ is about 110 meV. This voltage corresponds to a field of about 5000 V/cm across the AlAs, more than enough to result in saturated velocity transport in the direction of the field.

Scattering, accumulation, and depletion effects in the GaAs layers can also be important in affecting the population of excited carriers at the collecting interface. For example, forward bias may result in accumulation of carriers at the GaAs/AlAs interface, which would increase the number of optically excited carriers there.

Photoenhanced current is greater in reverse bias than in forward bias. This is because the application of reverse bias shifts the collecting interface to position (a) in Fig. 7.1, at the GaAs/AlAs interface, where the number of electrons and

photons is greater than at interface (b).

7.4.2 Variable-Temperature Measurements

Variable-temperature I–V measurements for samples H399, H734, and H735 were made. The basic shape of the curves was unchanged from Fig. 7.1. However, the overall photocurrent decreases with temperature. In Fig. 7.2 we present plots of the zero bias photocurrent versus temperature, under broad-band incandescent illumination. Data for three samples are presented. Data show an asymptote at lower temperatures. Activation energy plots do not show linear behavior over the entire range of temperatures. Variations in illumination level between successive temperatures were avoided but cannot be ruled out due to the experimental conditions under which data were obtained. The reasons for the overall decrease in photocurrent with temperature have not been conclusively identified because a number of factors may be at work. These include absorption coefficient variation, illumination level variation, band gap increase with decreasing temperature, and changes in carrier density with temperature. A detailed study of the temperature dependence of the photoresponse has not been done and might be interesting.

7.4.3 Summary

We have presented basic I–V curves taken under illumination for several samples. Photoenhanced current was observed. In forward bias the current is positive. In reverse bias the current is negative. Since there is a built-in voltage in the structure, the point of zero photocurrent does not coincide with zero applied bias. The effect of the light is to create a number of photoexcited carriers on either side of the AlAs barrier. In the absence of field in the AlAs, the photocurrent is directly proportional to the difference in light intensity on on either side of the barrier.[1] When the AlAs is sufficiently thick to allow significant energy loss and

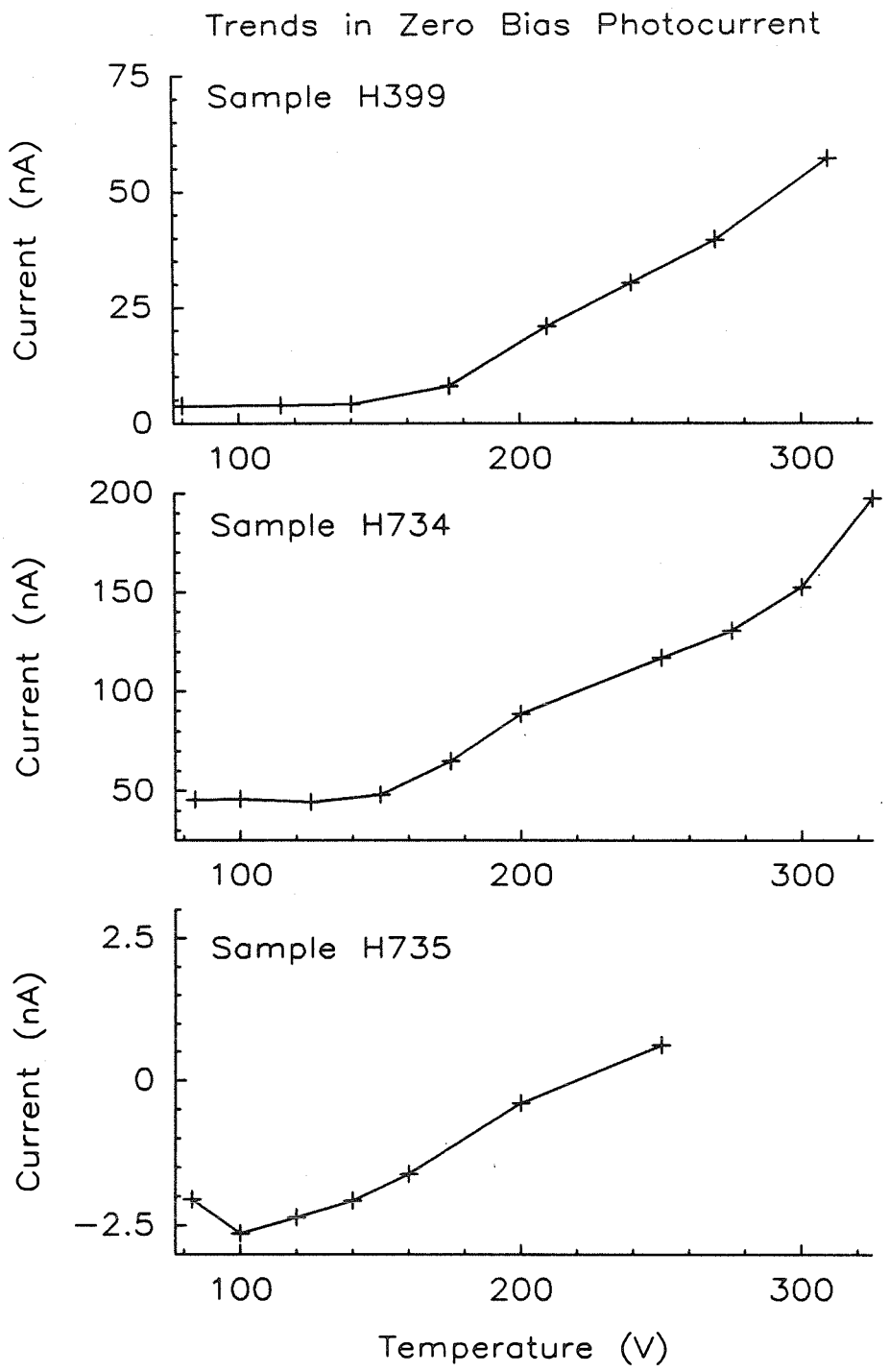

Figure 7.2: Zero bias photocurrent versus temperature for samples H399, H734, and H735. These data were extracted from complete I–V curves at each temperature.

field is present in the AlAs, the story is more complex. A simplifying concept is that of a collecting interface. Depending on which interface is at the higher energy, the collecting interface may be at the front or the back of the AlAs layer. It is the concentration gradient across this interface that determines the photocurrent.

7.5 Photocurrent versus Incident Photon Energy

This section describes efforts to determine the nature of the photocurrent in more detail. The nature of the photons that generate the photocurrent can be more effectively determined by examining the photocurrent as a function of the incident light energy. This type of measurement allows a more detailed examination of the effect of structural properties on the photocurrent. All of these studies were performed at room temperature.

7.5.1 Results

Photocurrent

In Figs. 7.3, 7.4, and 7.5 we present plots of the magnitude of the photocurrent as a function of incident light energy at several external-bias levels, for samples H399, H734, and H735. Relative intensities are accurately represented for each set of plots. The sign of the photocurrent depends upon the applied bias. For zero- and forward-bias scans (plots 'A' and 'B' in each figure), the photocurrent is positive, corresponding to electron flow from the back of the sample to the front. For strongly reverse-biased scans (plots 'D' and 'E' in the figures), the photocurrent is negative in sign. In plot 'C' of each figure, the photocurrent is double-peaked and two-signed. The photocurrent is negative near the lower-energy peak; it is

positive near the higher-energy peak. At high energies, photocurrent is small and negative. For Fig. 7.5, containing data for sample H735, the zero-bias photocurrent scan is double-peaked.

Indicated on the plots is the room-temperature band gap of GaAs.[¶] Also indicated is the band gap plus Fermi degeneracy of the top electrode, based on Eq. 7.1, and the doping level of the top electrode (see the table at the end of Chapter 6). This energy is relevant because it denotes the onset of strong band-to-band absorption in the top layer.

Signal versus Power

Signal versus power measurements were made for several samples at a variety of wavelengths. These measurements were made at room temperature. Representative data are presented in Fig. 7.6. Results indicate that signal is roughly linear with incident power. A log–log plot of the data in Fig. 7.6 is linear, with a slope of 1.2.

7.5.2 Analysis

Free-Carrier Absorption

The movement of holes is not believed to be the cause of the observed photoresponse. Holes are not created in large numbers in the top layer of GaAs until the incident photon energy exceeds the band gap plus Fermi degeneracy of the top layer. This point is indicated roughly by the higher-energy dotted line in Figs. 7.3 through 7.5. Even with the inclusion of band-gap shrinkage effects due to degenerate doping, the photoresponse is peaked at energies below which holes are created. Additionally, signal was found to be roughly linear with incident power, indicating

[¶]Band-gap shrinkage due to doping has been neglected. Doping might shift the band gap downward by as much as 20 mV for heavy doping. See Ref. 7 for more details.

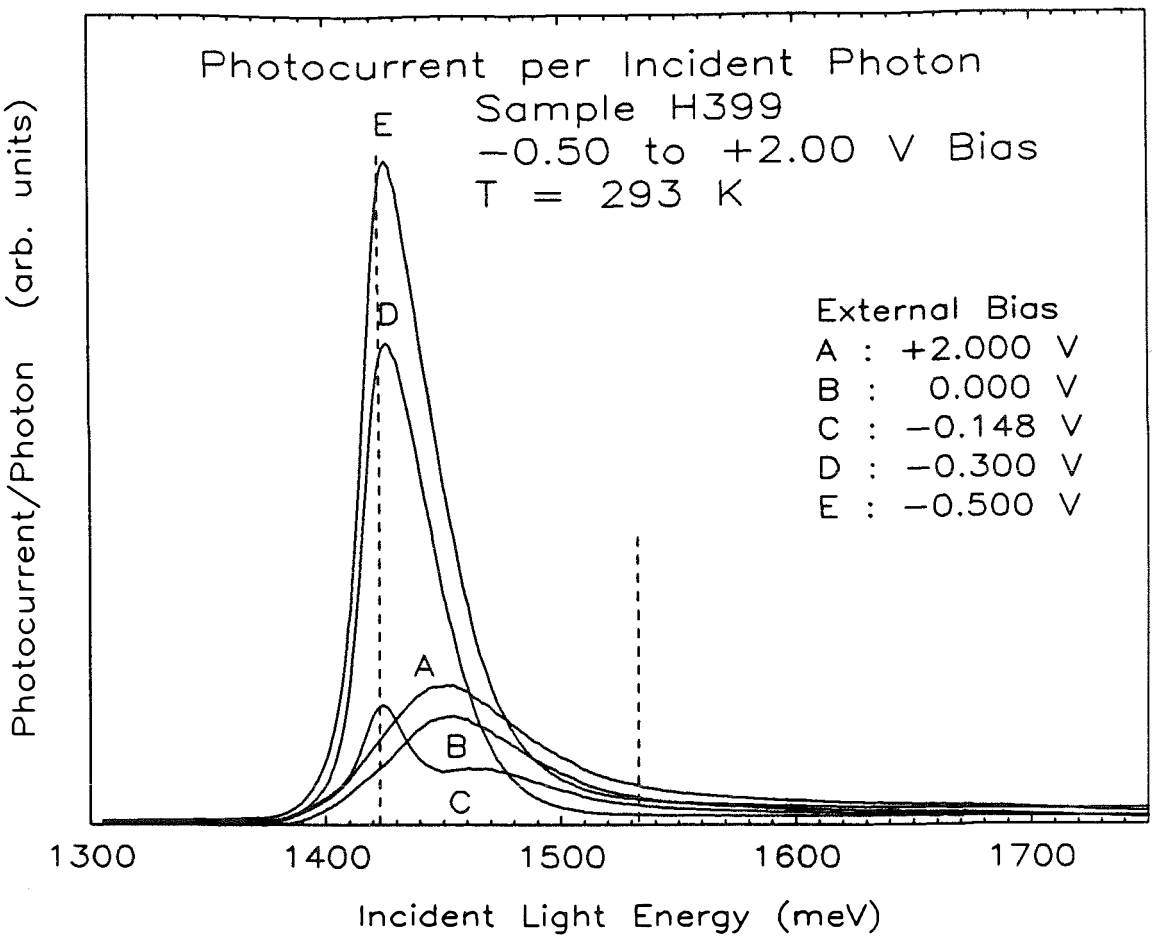

Figure 7.3: Plots of the magnitude of the photocurrent per incident photon as a function of incident photon energy at a variety of external biases. Data are for sample H399. The −0.148 V scan has positive and negative components. 0 and +2.0 V scans are positive in sign. −0.3 and −0.5 V scans are negative in sign.

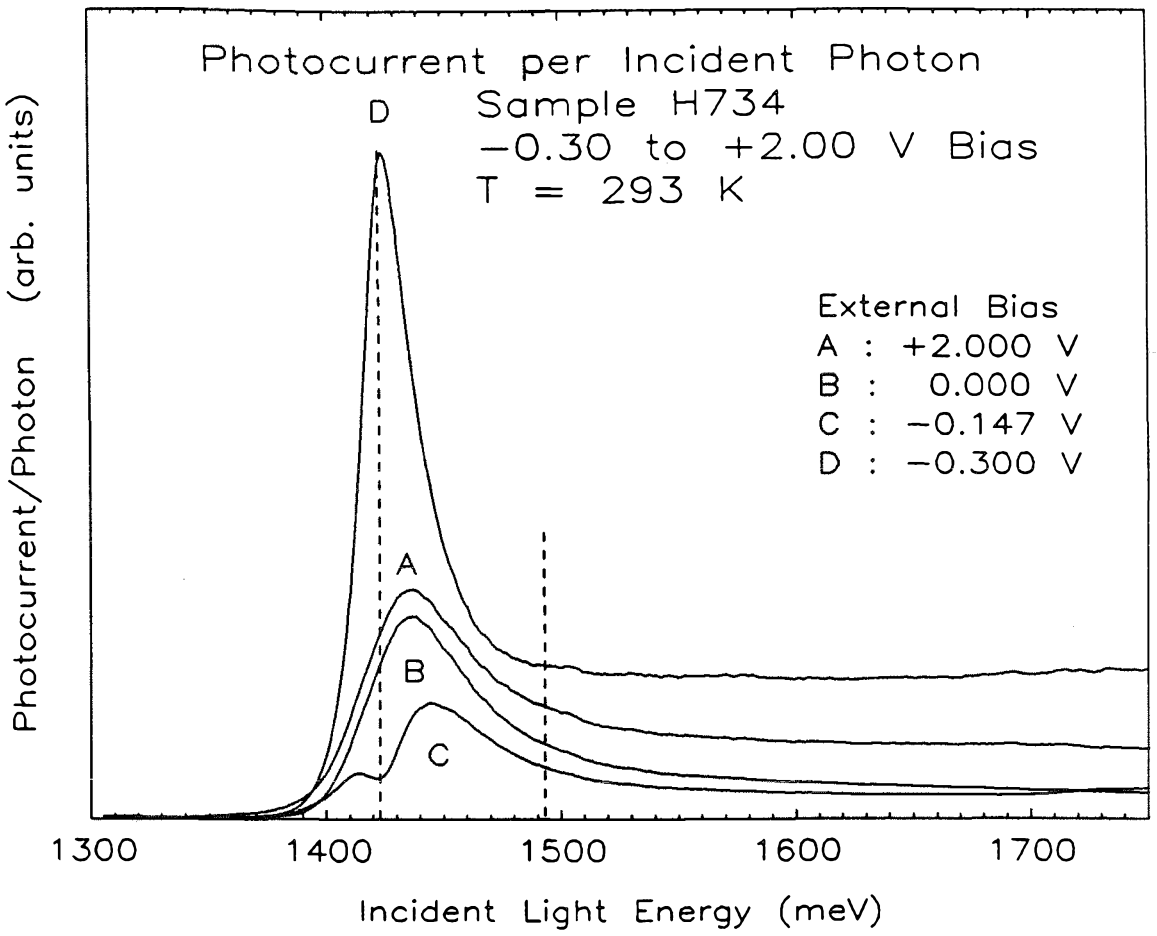

Figure 7.4: Plots of the magnitude of the photocurrent per incident photon as a function of incident photon energy at a variety of external biases. Data are for sample H734. The −0.147 V scan has positive and negative components. 0 and +2.0 V scans are positive in sign. The −0.3 V scan is negative in sign.

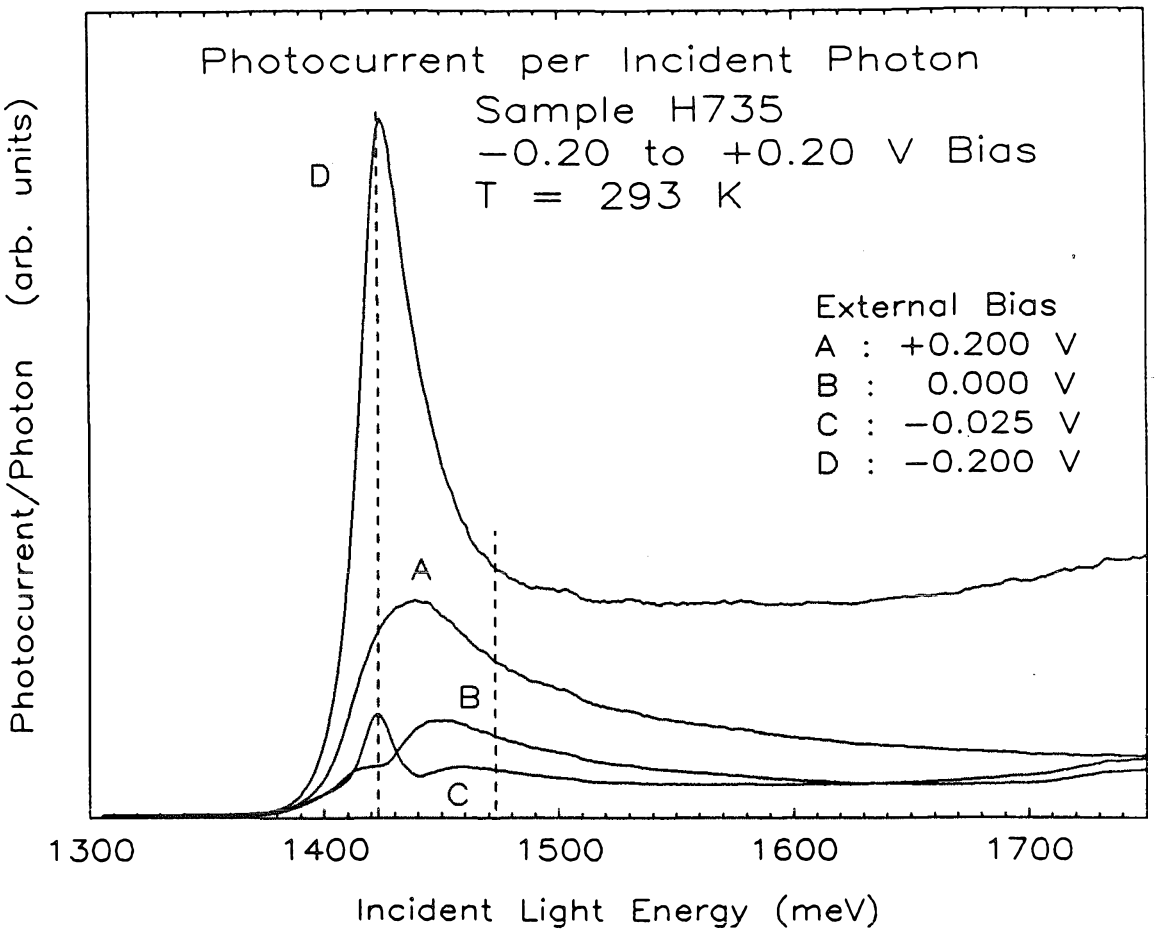

Figure 7.5: Plots of the magnitude of the photocurrent per incident photon as a function of incident photon energy at a variety of external biases. Data are for sample H735. Both the 0.00 and the −0.025 V scan have positive and negative components. Positive photocurrent prevails near the higher energy-peak. The +0.2 V scan is positive in sign. The −0.2 V scan is negative in sign.

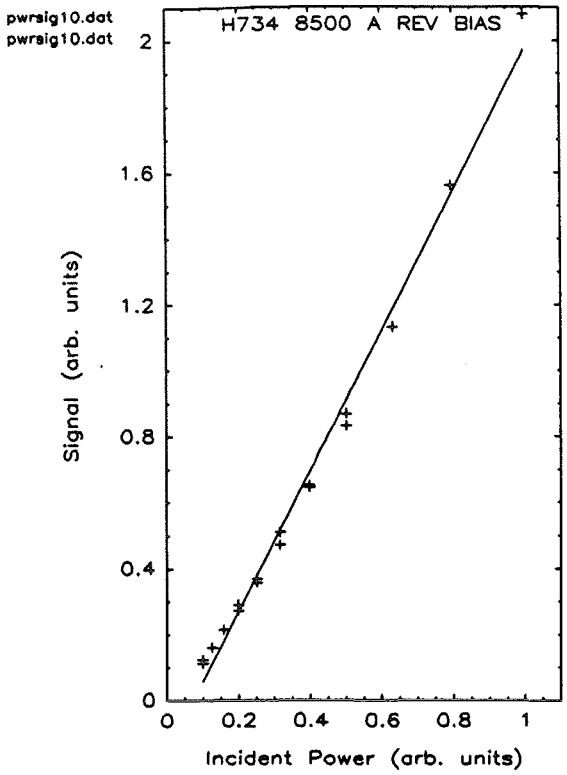

Figure 7.6: Signal versus power for one sample at 300 K.

that the absorption mechanism responsible for the observed photocurrents creates a single carrier. Free-carrier absorption is such a process; band-to-band absorption is not. The created carrier must surmount the AlAs barrier. Band-to-band absorption creates carriers at the band edge, which would not have sufficient energy to do this. Finally, above-band-gap photons would be strongly attenuated far from the barrier. These arguments are also valid for symmetric, thin barrier samples. Consequently, some of these points may also be found in Ref. 1. Trapping effects might also be important.

Basic Interpretation

As mentioned, the photocurrent arises from a gradient in the population of optically excited carriers across the collecting interface. At very long wavelengths, this difference is insignificant because few photons are absorbed. Signal is present at long wavelength, but it is small.[‖] At very short wavelengths, photons are strongly attenuated near the surface, and no signal is seen at the barrier. In between these two limits lies a region of photon energies at which significant differences in excited carrier concentrations can occur across the barrier. For a symmetric, thin-barrier sample this explanation can be made quantitative by calculating the difference in light intensity between the two sides of the barrier. This model was developed by Schlesinger *et al.*and found to explain the photoresponse of symmetric thin barrier samples in detail.[1–5] This method will never predict positive photoresponse because there will always be more photons in the top layer. Further, it will not account for fields and energy loss in the AlAs.

Detailed Interpretation

Certain general features are common to all the data presented in Figs. 7.3, 7.4, and 7.5. The structural properties of the samples determine these features. The position of the peak in reverse-bias photocurrent vs. incident photon energy spectra can be predicted. The doping asymmetry in the samples means that there will be a range of energies over which band-to-band absorption can take place in the lightly-doped GaAs, but *not* in the degenerately-doped top layer. Band-to-band absorption does not create photocurrent and is much more likely than free carrier absorption. Therefore, the number of free carriers excited at the back side of the AlAs will decrease, while the number created on the top will not. This situation

[‖]Long-wavelength studies of the photocapacitive behavior of the samples were the original intent of this study. See Epilogue at the end of the chapter.

decidedly biases events in favor of front-to-back transport. The maximum benefit will be exactly at the band gap of the back-side material.** Therefore, reverse-bias spectra are peaked at 1423 meV, the band gap of nondegenerate GaAs.

Zero- and forward-bias photocurrent spectra (positive in sign) are peaked at higher energies than the negative-signed reverse-bias spectra. This feature can be qualitatively explained. We have seen that front-to-back transport is most likely when the incident light energy is equal to the band gap of the lightly-doped GaAs. As incident energy increases, some band-to-band absorption takes place in the top layer, decreasing the number of optically excited free carriers there. This changes the concentration difference at the collecting interface to one more favorable to back-to-front transport (positive photocurrent). At energies greater than the Fermi-degeneracy plus band gap of the top layer, strong band-to-band absorption takes place near the surface, decreasing light intensity near the barrier. Between these two energies, there will be a point of maximum favorability to electron transport from back to front. Thus we conclude that the photocurrent should lie at higher energies in forward bias than reverse bias, but at less than the band gap plus degeneracy of the top layer (expect it to lie between the two dotted lines in Figs. 7.3 through 7.5).

Since the photocurrent is sometimes positive and sometimes negative, there must be a bias at which photocurrent is small. This bias level is about -150 mV for samples H399 and H464 and about -25 mV for sample H735. At these biases the sign of the photoresponse depends on the energy of the incident light. At light energies most favorable to negative photocurrent (near 1423 mV), one observes negative photocurrent. At other energies the photocurrent is positive. In addition, the photocurrent at very short wavelengths is small and negative. We have

**It might be interesting to examine highly asymmetric heterostructures, *e.g.*, GaAs/AlAs/$In_xGa_{1-x}As$.

already seen that reverse-bias photocurrent is greater than forward-bias photocurrent. Thus, it is not surprising that the peaks in the photocurrent spectrum are largest in reverse bias.

Differences in sample geometry are reflected in the photocurrent spectra. We now discuss specific differences in the photoresponse of samples H399, H734, and H735. The peak shift between forward- and reverse-bias photocurrent spectra can be correlated with the top-layer doping densities of the samples. The doping in H399 is about $3 \times 10^{18}\,\mathrm{cm}^{-3}$, and the peak shift is about 28 mV. This shift is significantly greater than the peak shifts for samples H734 and H735, which, being doped at 1 and 1.5 $\times 10^{18}\,\mathrm{cm}^{-3}$, have peak shifts of 9 and 14 mV, respectively. Higher dopings result in a greater energy difference between band-to-band absorption onsets on either side of the barrier, leading to a larger peak shift. Studies of sample H464, not presented here, support this trend.

The effect of barrier thickness can be seen by comparing samples H399 and H734 (which have 2500 Å barriers) to sample H735 (with a 1000 Å barrier). Less energy is lost across a thinner barrier. The effect is to decrease the amount of bias needed to create negative photocurrent (net front to back transport). In H399 and H734 about 150 mV of bias had to be applied to change the sign of the photoresponse. In H735 only 25 mV was necessary. For still thinner structures, one would expect to see negative photocurrent at zero bias. With H735, we thus demonstrate consistency with earlier results, wherein negative photocurrent was always observed at zero bias because of the thin barriers.[1–5]

Finally, a word about traps. These samples are loaded with deep levels. We have neglected these levels in this analysis, because the trap levels were assumed to be held empty by illumination. While the traps do not change the basic explanation for the observed results, they may provide a means of increasing the free carrier population in the lightly-doped GaAs layer. Increases in this population

can affect the photoresponse because they increase the free carrier absorption probability. Conclusive evidence of the role of deep levels in the photoresponse of these structures requires further study. The transient behavior of the sample might well depend on these levels. It should further be noted that the loss properties of the barrier could depend to some degree on the intensity of light in the barrier region, which would be important in determining the sign of the photocurrent.

7.6 Conclusions

We have presented an experimental study of the photoresponse behavior of asymmetrically doped GaAs/AlAs/GaAs heterostructures characterized by thick AlAs barriers. New results are observed, which can be explained with basic structural properties of the samples. Doping asymmetries are reflected in the magnitudes of the observed photocurrents. These asymmetries, coupled with the thick AlAs barriers, are also evidenced in the observation of positive photocurrent at zero bias. The photocurrent is seen to change sign when the structures are reverse biased. Less bias is required to do change the sign of the photocurrent as barriers decrease in thickness, establishing a trend that demonstrates consistency with earlier work.[1] The concept of a "collecting interface" is introduced to account for the effects of fields and scattering across the AlAs.

7.7 Epilogue: Loose Ends

This study grew out of a desire to observe optically the deep levels known to be present in these samples. Photocapacitance studies were undertaken in an attempt to determine the optical activation energy of the levels. The idea was to monitor the capacitance as a function of incident light energy. Since we know that the capacitance changes when the levels are depopulated (see Chapter 6), a change in

capacitance should be seen when the incident light energy becomes insufficient to depopulate the level.

These studies were not successful for several reasons. The typical energy of light needed to perform this study might be expected to be roughly the activation energy of the level. This is known to be roughly 500 meV from DLTS studies. This energy corresponds to a wavelength of 2.5 μm. We were unable to obtain sufficient intensity at this wavelength to observe meaningful changes in the capacitance. Since ordinary lenses begin to attenuate at these wavelengths, we might not be getting all the intensity available. Stray light might also be a problem, since light above 500 meV in energy can hold the levels empty. Since the experiment is performed with a 1000 W tungsten lamp, stray light can be a problem. The combination of low signal at 2.5 μmand stray light makes for a serious problem.

This chapter describes the DC photoresponse of our single barrier samples. DC response is measured because the incident light is chopped slowly (27 Hz). The issue of the transient response of the samples has not been touched on, but is an interesting question. When an oscilloscope trace is examined, transient response is observed at the start of each illuminated period. This transient response always takes the form of a 'spike' of negative photocurrent, which is of insignificant duration compared with the total illuminated period. The lock-in should see mainly the nontransient behavior, since the charge contained in the transient is generally less than that contained in the nontransient period. Since the current associated with trap filling is of the order of 50 pA (from Chapter 6), and since the illuminated current level is about 200 nA, it seems unlikely that trap effects are dominating the current, although further study of the transient behavior might prove more revealing. This transient response has not been explained, but may be due to trap emptying effects, or perhaps a surge of carriers from one side of the barrier to the other. The capacitance of the device, and the dependence of its capacitance

and resistance on illumination, would be important in attempting to explain these results.

Photoresponse measurement of the barrier height (band offset) might be possible in these samples, but was not done. This measurement would require that the structure be strongly reverse biased, to guarantee that the desired current mechanism is dominant. Even so, strong excitation of carriers on both sides of the barrier might prove overwhelming to the one-sided transport desired. The incident photon energy needs to be of the order of the barrier height. Since this barrier is known to be roughly 200 meV, we would need 300 to 800 meV light. Sufficient intensity at these energies was not available because of the light source and the optics used in the experiment. The illustrated data in Figs. 7.3 through 7.5 do not extend to these energies. The lowest energies are about 1300 meV. The photocurrent between 1300 and 1400 meV is not proportional to the square of the photon energy, as would be expected for photoemission over a barrier.[8,9]

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Appendix A

Photolithography

1. Clean substrate: Acetone and ethanol rinse; substrates must be clean and dry.

2. Photoresist: We currently have 3 types. The in-use resist dropping bottle should be changed when thickening of resist is observed. This will cause other process parameters to deviate from listed values. A general rule is to change the resist at least every 6 months.

   a) AZ 1350J-SF : The old standard, relatively insensitive to mid-UV.

   b) AZ 1518 : A new resist designed to directly replace 1350J, it uses a different (safer, we hope) solvent base. It has low mid-UV sensitivity.

   c) AZ 5214 : A new (1986) resist designed with increased mid-UV sensitivity. The resist of choice for most applications. (A note for specialists: see manufacturer's literature on this resist's image-reversing capability.)

3. Spin on photoresist: First apply adhesion promoter and spin 30 sec at about 4000 rpm (faster for thinner coatings). Finally, apply enough photoresist to cover the sample and spin for 30 sec at 4000 rpm. The result will be a 1 μm resist coating (roughly). More information on this can be found in AZ and Shipley literature.

4. Prebake: To evaporate solvents used in application of resist. 25 min at 85 °C. The time is important for liftoff processes only.

5. Expose: The important factor is the total energy deposited on the sample. Our mask aligner exposes at 320 nm. Use the log book to record mask aligner information.

   a) 1518 & 1350J : 12mW/cm^2 for 45 (540 mJ/cm^2) seconds works. Tests show that lower energy exposures will also work.

   b) 5214 : Tests indicate that good results can be had for exposure energies from 200 to 450 mJ/cm^2. We use 9 mW/cm^2 for 30 seconds (270 mJ/cm^2). Lower energies can usually be accommodated with longer developing times.

   c) The lamp: The lamp will require about 20 minutes to warm up after starting. Turn it off if no work is to be done in the next couple of days. While running, N_2 *must* blow on the lamp. When greater than 10 sec exposures consistently require more than 360 W of lamp power, the bulb should be replaced (see manual for procedure). At no time should lamp power exceed 400 W (an alarm will sound). These features are to lessen the chances of a lamp explosion (very messy).

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6. Chlorobenzene soak : 10 minutes, blow dry. Fresh chlorobenzene will require much shorter soak times for the first week or two of use (1-2 minutes).

7. Bake dry: 5 minutes at 85 °C

8. Develop 1:1 AZ developer : water for 1-3 minutes depending on conditions

WET ETCH PROCESSES

6. Develop: 1:1 AZ developer : water for 1 minute

7. Post bake: 30 minutes (at least) at 120°C. 1 or 2 hrs is OK, but the longer the postbake, the more difficult the resist is to remove when processing is finished.

NOTE: Some of the information used to compile this procedure was extracted from a process developed for use in Dr. D. Rutledge's research group. Other information was collected from various manufacturer's literature.

Appendix B

Photocurrent Details

Photovoltage and photocurrent measurement circuits are illustrated in Fig. B.1. The device is modeled as a capacitance and a resistance (C_d and r_d), with the effect of illumination modeled as a current source (i_p). These measurements are assumed to be DC (hence the low chopping frequency), and C_d should play no role, except insofar as the DC assumption is jeopardized.

Consider the photovoltage measurement circuit.[1] The supply voltage divides between the series resistance (R_s) and the parallel combination of the lock-in resistance (R_L) and r_d. The bias appearing across the sample is

$$V_a = V\left(\frac{r_d R_L}{R_s R_L + R_s r_d + r_d R_L}\right). \tag{B.1}$$

Since the current source is in parallel with all three resistances, the measured photovoltage at the lock-in is

$$V_p = i_p r_d\left(\frac{R_s R_L}{r_d R_L + R_s R_L + r_d R_s}\right). \tag{B.2}$$

The ideal measurement would record $i_p r_d$, but the actual measurement obtains this value only when R_L and R_s are much larger than r_d. However, R_s must be chosen in such a way that reasonable V_a is obtained. A compromise is to require $R_L >> R_s >> r_d$. This requirement can be troublesome when r_d is large, as

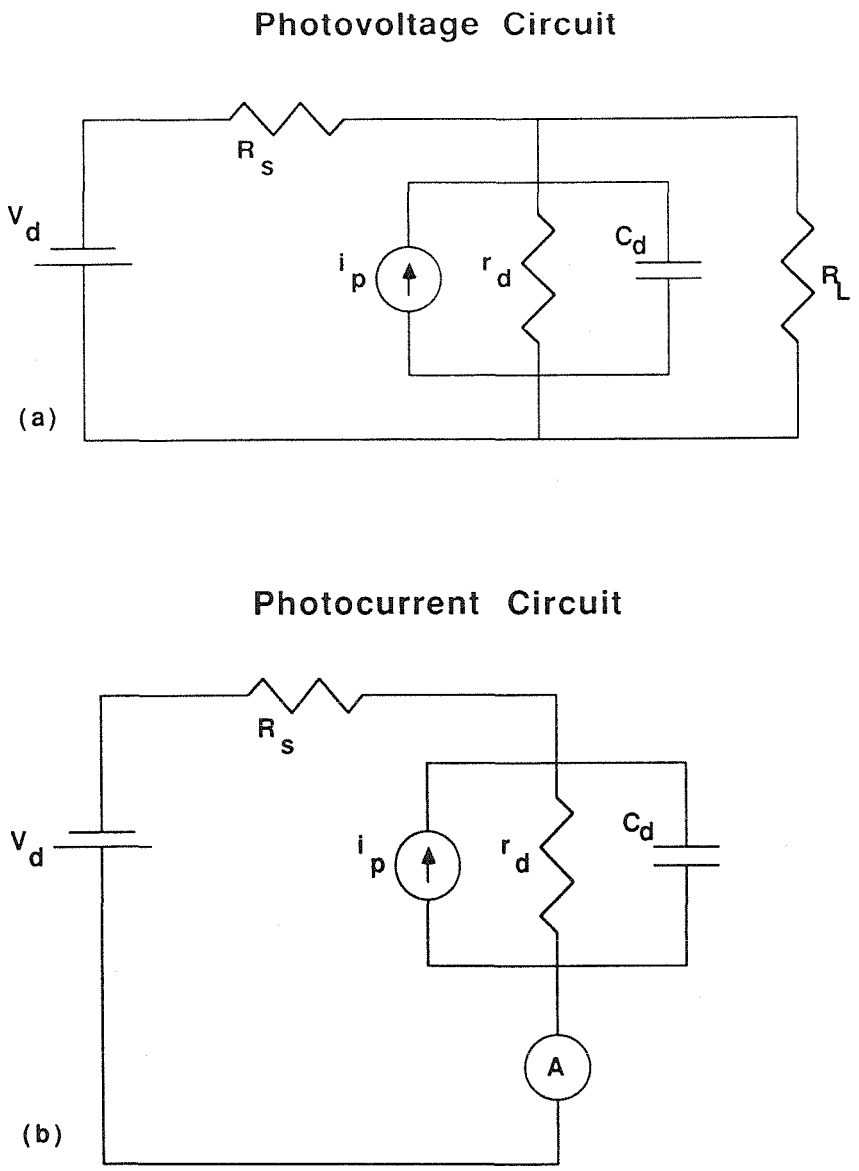

Figure B.1: Externally-biased photovoltage (a) and photocurrent (b) measurement circuits. The sample is modeled as a current source (i_p) due to illumination, a resistance (r_d), and a capacitance (C_d).

is the case with our samples. Finally, r_d changes as a function of illumination, modulating both V_a and V_p during a scan.

The photocurrent technique is more direct. It is achieved with the use of a current sensitive preamp whose input is a virtual ground. Our preamp converts current to voltage, with a sensitivity of 10^{-7} to 10^{-9} V/A. Parallel loading of the circuit is avoided, and i_p is measured directly. The resistance R_s can be very small compared to r_d, so the detected current is essentially the entire photocurrent, and changes in r_d are not important.

The quantity of interest in a photoresponse measurement is the photoresponse *per incident photon.* These data are universal, removing lamp and spectrometer effects. Photocurrent per incident photon is obtained by dividing the raw photocurrent by a measure of the incident photon density. This measure was obtained by substituting a Molectron P-4 optical pyrometer in place of the sample and measuring the induced photocurrent. The response of the pyrometer is constant over a very wide wavelength range. The resultant data provide a measure of the incident intensity $I(\omega)$, because the response of the pyrometer is constant over a very wide wavelength range. The incident intensity is related to the number of photons via

$$I(\omega) = c\hbar\omega N(\omega), \tag{B.3}$$

where c is the speed of light, $N(\omega)$ is the number of photons at frequency ω, and $\hbar\omega$ is the energy of these photons. By dividing $I(\omega)$ by $\hbar\omega$, a relative measure of the incident *photon density* is obtained. All photocurrent scans are divided by this measure of $N(\omega)$ to obtain photocurrent per incident photon.

Phase drift of the photocurrent signal as a function of wavelength was occasionally observed. To ensure that total photocurrent was obtained, each sample was measured at least twice, at lock-in quadratures perpendicular to one another. The magnitudes of these scans were added together, to obtain total photocurrent.

Since photons are postulated to create the electron current, the incident photon

flux must exceed the electron flux. A rough estimate of the various fluxes can be made. The size of the typical photoenhanced current is 200 nA. For 350 μm mesas, this is about 2×10^{-4} A/cm^2. The electron flux can be calculated from

$$\Phi_e = j/e = nv, \tag{B.4}$$

where j is the current density, v is the electron velocity, and e is the electronic charge. A value of $\Phi_e \sim 1 \times 10^{15}$ electrons/(cm^{2}sec) is obtained.

The broad-band incandescent illuminator used delivered an intensity of about $P = 40$ mW/cm^2 to the surface of the device, as measured by a power meter. The light is assumed to have a black-body distribution with a typical quartz-halogen temperature of 3000 K. The average photon energy for this distribution is $E_{av} = 2.7kT$, where k is the Boltzmann constant.[2] Thus, the photon flux at the surface can be estimated as

$$\Phi_p = \frac{P}{E_{av}}. \tag{B.5}$$

A value of about 3.6×10^{17} photons/(cm^{2}sec) is obtained. This photon flux exceeds the electron flux by about 2 orders of magnitude. Some of these photons are absorbed in the heterostructure, giving rise to the observed photocurrent.

Another relevant consideration is the photon flux *at the barrier*. This is important, since light must be present at the barrier to generate photocurrent on the back side of the AlAs. We know that the peak photocurrent is due to 1.4 to 1.5 eV light. About 10 percent of total power lies in this energy range[2], or about 4 mW/cm^2 incident at the device surface. The absorption coefficient at 1.45 eV is about $\alpha \sim 1000\,\mathrm{cm}^{-1}$[3], and the attenuation constant $e^{-\alpha x} \sim 0.67$. The incident flux at the AlAs barrier may be calculated as above, with $P = (0.67)(4)$ mW/cm^2, and $E_{av} = 1.45$ eV. After converting units, we obtain about 1.2×10^{16} photons/(cm^{2}sec), which exceeds the electron flux.

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Appendix C

TEM Data

This appendix summarizes all the cross-sectional transmission electron microscope (TEM) data obtained during the DB/VFET and DB/MESFET projects. S008 and S031 are DB/VFET samples. S032 was grown at the same time as S031, but was not tested as a DB/VFET sample. T549 and T640 are DB/MESFET samples. These samples were grown at 775 °C.

TEM results for DB/MESFET and DB/VFET samples

Sample No.	TEM Data			Growth Time
	Top Barrier (Å)	Well (Å)	Bottom Barrier (Å)	(sec./sec./sec.)
S008	110.5	64.3	110.5	2.0/1.3/2.0
S031	125	68	116	2.0/1.3/2.0
S032	102	45	105	2.0/1.3/2.0
T549	86	46	77	2.0/1.3/2.0
T640	74	30	62	1.6/1.0/1.6

Appendix D

Glossary of Acronyms and Abbreviations

cfm : Cubic feet per minute (flow rate).

C–V : Capacitance–Voltage.

DBD : Double-barrier diode.

DB/MESFET : Double barrier integrated with metal-semiconductor field-effect transistor.

DB/VFET : Double barrier integrated with vertical field-effect transistor.

DLTS : Deep-level transient spectroscopy.

FET : Field-effect transistor.

HBT : Heterojunction bipolar transistor.

IMPATT : Impact ionization and transit-time (oscillator).

I–V : Current–Voltage.

JFET : Junction field-effect transistor.

MBE : Molecular beam epitaxy.

MESFET : Metal-semiconductor field-effect transistor.

MIS : Metal insulator semiconductor.

MISFET : Metal-insulator field-effect transistor.

MOCVD : Metal organic chemical vapor deposition.

MODFET : Modulation-doped field-effect transistor.

MOS : Metal oxide semiconductor.

MOSFET : Metal oxide semiconductor field-effect transistor.

NDR : Negative differential resistance.

PBT : Permeable-base transistor.

P/V : Peak to valley (current ratio).

QWITT : Quantum-well injection transit-time (oscillator).

RBT : Resonant tunneling bipolar transistor.

RHET : Resonant tunneling hot electron transistor.

RTFET : Resonant tunneling field-effect transistor.

RTT : Resonant tunneling transistor.

sccm : Standard cubic centimeters per minute (flow rate).

SEM : Scanning electron microscope.

SIS : Semiconductor-insulator-semiconductor.

SLM : Standard liters per minute (flow rate).

TEM : Transmission electron microscope.

TMAl : Trimethyl aluminum.

TMGa : Trimethyl gallium.