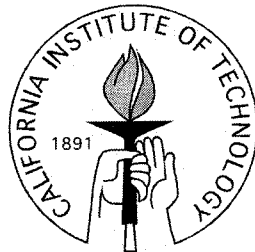# Through-Wafer 3-D Micromachining

# and Its Applications for

# Neural Interfaces and Microrelays

Thesis by

John A. Wright

In Partial Fulfillment of the Requirements

for the Degree of

Doctor of Philosophy



California Institute of Technology

Pasadena, CA 19925

Defended May 12, 1999

To the person who is a source of continual

love, support, and encouragement.

To one of the strongest people I know.

To a woman loved dearly by her children

though we may not always say it.


To my mother.

# ACKNOWLEDGEMENTS

# Through-Wafer 3-D Micromachining and Its Applications for Neural Interfaces and Microrelays

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## Abstract

The relatively new field of Micro Electro Mechanical Systems (MEMS) is proving to be a very powerful technology capable of producing devices beneficial to a wide range of disciplines. Instruments once impossible to fabricate can now made with relative ease opening up new possibilities in experimental research as well as commercial applications. Through-wafer, 3-D micromachining techniques used to produce two families of such devices are presented.

A functional silicon micromachined device that permits non-invasive, bi-directional, highly specific communication with cultured mammalian neurons is discussed. The mechanical and electrical nature of the system is reported and experimental data presented. In arriving at the present design, an iterative approach was

used to create a structure that allows normal growth of neurons and permits the formation of functional neural networks while preventing cell body escape.

The set of low-temperature (< 400°C) fabrication steps that have been used to develop two types of magnetically actuated MEMS relays are presented. Designed to be potentially compatible with CMOS substrates, the fabrication uses thick electroplated metal films (> 10 μm,) including Au, Cu and $Ni_{80}Fe_{20}$, and insulating material deposited at low temperatures. Millinewton force, variable-reluctance actuators have been realized with this technology and used as the basis of a miniature electromagnetic relay. Prototypes utilize > 5 μm contact gaps and produce 200 μN of force with a coil power of only 320 mW. Initial electrical tests show contact resistances of less than 1°. For a second application, magnetostatic relays have been designed to commutate miniature DC brushless motors. Large contact closure forces (> 5 mN) are generated to produce contact resistance of less than 35 milliohms. Commutation of a three-phase, four-pole DC brushless motor by three of the MEMS relays has been successfully demonstrated.

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# CHAPTER

# 1

# INTRODUCTION

In 1948, Bell Labs researchers announced an amazing invention: the transistor [9]. At best, public reception of the device can be described as less than enthusiastic. Over the course of the intervening 50 years, however, transistors have become a mainstay in nearly every product that uses electricity and have made possible the so-called Information Age in which we now live. Over the decades the technology used to produce transistors has been refined and improved to the point where the size of a single device can be expressed as easily in atomic radii as in conventional metric units. A complex, yet straightforward system of laying down layer upon layer of material, each patterned into specific shapes for a certain function is now utilized by hundreds of foundries that produce millions of components every year. The resulting multi-billion dollar infrastructure has made possible thousands of new enterprises and areas of scientific

research. Among these is a relatively new and very promising technology known as Micro Electro Mechanical Systems or MEMS.

## 1.1  A Brief History of MEMS

Foreseeing the miniaturization trend arising in semiconductor devices, Richard Feynman proposed that scientists and engineers should strive for a similar reduction in the size of mechanical components. He presented his ideas on this topic in a speech in 1959 and issued a challenge to anyone willing to take on the task [3]. He offered a prize of $1000 to "the first guy who can take the information on the page of a book and put it on an area 1/25,000 smaller in linear scale in such manner that it can be read by an electron microscope" and a second $1000 to "the first guy who makes an operating electric motor - a rotating electric motor which can be controlled from the outside and, not counting the lead-in wires, is only 1/64 inch cube." With this challenge, Feynman hoped to spur a new area of research and the development of new fabrication technologies. A year after the gauntlet was thrown down, William McLellan claimed the prize for the motor using conventional machining techniques [6]. While technically the winner, Mr. McLellan readily admits that his approach was not necessarily in the spirit of the contest. It wasn't until several decades later, in 1988, that an electric motor fabricated with truly new processing technology was finally realized [2]. During the intervening time, the field of micromachining was born, stagnated, and then given new life.

Approximately 10 years after Feynman's challenge, a group of scientists

published a paper on a device they called a "resonant gate transistor [7]." This novel structure aimed to reproduce the functionality of its semiconductor counterpart in a mechanical, rather than electronic fashion. More importantly, the team that conceived this device realized that the same technology used to integrated circuits could be used to fabricate very small-scale sensors and actuators. Like their electronic brethren, micromachined devices attracted limited attention in their initial years and save for a few publications went largely unnoticed. Recent developments and substantial commercial investment has shown that the technology was simply ahead of its time.

A resurgence of interest in MEMS devices arose 10 to 15 years ago that has since led to a burgeoning new field of research and industrial development. Beginning primarily in schools such as MIT and Berkeley the new crop of devices focused on the study of basic science and fundamental operation of microscopic machines. The common thread amongst all of this work was the use of microelectronic fabrication processes to produce the various devices.

From this basic research, MEMS programs in most major universities and large companies have been started with the goal of producing sensors and actuators that can be fabricated alongside with integrated circuits. Pressure sensors, ink jet printer heads, and accelerometers have been the most successful products realized to date. On the brink of commercialization are gyroscopic rate sensors, microrelays, microfluidic systems, and high-density data storage devices. Key to all of these products is their minimal size, weight, and low end-user complexity. Additionally, MEMS technology promises to

deliver these devices at very low cost, with very high reliability, and with in-package "intelligence."

## 1.2 MEMS Fabrication Technologies

All traditional micromachining technologies have been borrowed from the semiconductor-manufacturing sector. This multi-billion dollar industry has produced innumerable processes for the deposition and patterning of films of many different types of materials. From these, MEMS designers have selected a number of processes that can lay down structural, sacrificial, and masking materials. Using a variety of techniques, very intricate and highly functional devices can be produced. In general, the approaches used in the fabrication of a MEMS structure can be classified as bulk micromachining, surface micromachining, wafer-to-wafer bonding, or a hybrid of the three. Each method has its benefits and its limitation and all are widely used in the industry.

### 1.2.1 Bulk Micromachining

Bulk micromachining forms the structures of its MEMS devices from the bulk substrate wafer on which the parts are fabricated. The typical wafer material used is silicon because such a substrate will allow electronics to be integrated with the mechanical structures. By using the appropriate masking materials, wet and/or dry etchants can selectively remove material from the wafer to form structures such as membranes, cavities, mechanical springs, and through-holes. With the proper choice of

materials, freestanding structures such as cantilever beams and air bridges can be left after the etching is complete.

Two main benefits of bulk micromachining have led to its widespread use. The first is simplicity of the processing. The first is the minimal investment in equipment that is required for the wet processes. All that is needed are the means of depositing and patterning a masking material, such as oxide or nitride, and a large beaker in which relatively safe etchants can be heated and stirred. The second attractive aspect of this technology is that it forms the structural components of the MEMS devices out of bulk silicon. The mechanical properties of this single crystal material are excellent with strength and resonant quality factor values among the best available [8].

The main drawback of bulk micromachining is that it can only produce a limited number of device geometries. The nature of the wet etchants used in this type of processing is discussed more thoroughly in chapter 9 but suffice it to say that they are best suited to fashioning relatively large, square or rounded features. While a new plasma technology (i.e., DRIE) does permit arbitrarily shaped structures to be created, bulk micromachining typically only allows a single layer of material to be easily patterned to a single depth. Although novel processing can result in multiple depth structures [5], producing components such as hinges, vacuum cavities, and sliders is essentially impossible with bulk techniques.

### 1.2.2 Surface Micromachining

To create complex, interlocking structures, surface micromachining is used. The basis of this technology is the use of two types of material. The first material is used for

the structural members of the device. It is laid down in a film and patterned to form springs, pins, membranes, and beams. The second material is used to define spacings and gaps between the structural components. Termed "sacrificial," this material is removed at the end of the process. By laying down and patterning these two types of materials in alternating layers, a wide range of mechanical building blocks can be created including hinges, pins and sliders.

Since each layer is patterned after it is laid down, nearly any planar geometry can be realized. This is the strength of surface micromachining. Among the large number of devices that have been fabricated using this technology are plates that can pivot out of plane by 90°, magnetic cores that are wrapped with wires, electrostatic motors that rotate at high rates of speed, and mechanical transmission that greatly magnify the force produced by a weak actuator [1, 2, 10, 11]. In theory, an arbitrary number of levels can be surface micromachined; to date, it is believed that the largest number to be reported is seven [4].

The main limitations of surface micromachining are the thicknesses of the deposited films and their mechanical quality. Time considerations and build up of internal stresses typically limit deposited films to several microns of thickness. Large inertial masses and high out-of-plane stiffness are difficult to achieve with thin films. Reduction of parasitic coupling, both electrical and magnetic, between structures requires an increase in the overall footprint of the device. Finally, since the deposited films are typically polycrystalline, the high mechanical quality factors achieved in bulk single-crystal silicon beams are not matched in surface micromachined structures.

### 1.2.3  Wafer-to-Wafer Bonding

Wafer-to-wafer bonding is commonly employed to produce complex, bulk micromachined devices as well as to combine the benefits of both bulk and surface micromachining. Because bulk micromachining only produces single layer structures, wafer bonding allows several such substrates to be combined to create a multi-level device. Alternatively, a wafer with surface micromachined structures can be bonded to a bulk-machined substrate allowing each technology to be used to form those features they are best able to create. This can be further extended to allow a substrate containing electronics to be attached to the MEMS wafers producing a fully integrated, intelligent device. Wafer-to-wafer bonding is used widely in the commercial sector in the fabrication of pressure sensors and ink-jet heads.

While this approach does allow a greater range of devices to be fabricated when compared to the individual technologies, it still has its limitation. For the bonding of bulk micromachined wafers, truly free-form geometries are still not realizable. When bonding surface micromachined and electronics containing wafers, special care must be taken not to damage the resident structures. High pressures, temperatures and voltages are employed in the bonding process that could destroy the devices. Finally, forming electrical interconnections between the many layers is difficult to achieve which limits the usefulness of this approach.

## 1.3 Through-Wafer 3-D Micromachining

The aim of the research presented in this thesis is to develop a new base technology that allows 3D devices to be micromachined in silicon as well as other substrate materials. This is achieved by integrating bulk and surface micromachining technologies and introducing double-sided processing techniques. To demonstrate the flexibility of through-wafer machining several devices have been fabricated and tested. These include neural interfaces and microrelays.

Initial work utilized through-wafer micromachine processing to produce a family of devices that are called neurochips and neuroprobes. These are heavily bulk micromachined structures with surface micromachined features that are formed on a thin membrane inside a deep cavity. Accurate front-to-backside alignment techniques are developed to allow precise placement of microstructures on both sides of the silicon substrate. The majority of this work has used films that are deposited at relatively high temperatures. The most recent generation of neuro-devices, however, is being designed with low-temperature materials and processes. This will allow wafers with pre-fabricated CMOS circuitry to be used as the starting substrate for these devices.

The progression of the neural interface project towards the use of low-temperature processes gave rise to the development of micromachined microrelays. In addition to producing functional devices, this work seeks to develop fabrication techniques that are fully compatible with CMOS-containing silicon substrates. The majority of the structures in the microrelays are surface micromachined. This allows a high degree of flexibility in

geometric design as well as the use of multiple structural layers.    Through-wafer vias

allow the devices to take on a three dimensional layout that minimizes their footprint and

reduces parasitic losses.  The techniques and materials used in the microrelays have many

additional applications and can be used to produce a wide range of interesting devices.

# CHAPTER

# 2

# INTRODUCTION TO NEURAL SCIENCE

Neural science, in its present form, has only been in existence for the last two centuries. Regardless, man realized the importance of the brain as early as 1700 B.C. [14] and through the millennia worked to comprehend its function. Today, it is taken for granted that the central nervous system (CNS) is the center of thought, emotion and behavior in all animals. But this understanding grew slowly over the centuries as scientists fought to first understand the basic neuroanatomy and then strove to unlock the physiology of the individual nerve cells called neurons. Present research strives to understand how the nerve clusters that make up the CNS interact to perform high level functions associated with thought, emotion, perception, and motor reaction. To do this, a new host of tools must be developed to make such research possible.

## 2.1   Neural System Complexity

Tackling the function of the entire human brain as a whole is an intimidating task. Neurobiologists estimate that on the order of 100 billion ($10^{11}$) neurons make up the average human brain.   When one considers that the most complex computer chips presently made contain less than 100 million ($10^8$) transistors and that one neuron makes arguably 100 to 100,000 times more connections to its neighbors than the typical transistor, the problem seems intractable.   Still, great strides have been made in understanding the brain as a whole.   The human CNS can be broken down into several major centers that are generally attributed to motor, sensory and other mental functions. These centers can be further subdivided into specialized regions for those functions.   On the other end of the complexity scale, investigations into the neurophysiology of single neurons and the molecular and electrical mechanisms they employ have progressed rapidly and are a relatively mature area of research.   A much less understood area of neurobiology is the interaction between small numbers of neurons.   Neural plasticity, or how the interconnections between neurons change in response to activity patterns, is believed to govern how the mind learns and adapts as an animal grows from infancy, through childhood and into full maturity.

Understanding small to medium sized neural networks (tens to thousands of neurons) requires monitoring of a large number or perhaps all of the cells for long periods of time.   Preferably this would be done *in vivo*, meaning in a living and intact nervous system, but substantial research could be done *in vitro* on neurons cultured in a

controlled, easily monitored laboratory environment. Past approaches to both types of experimentation are presented in the following sections providing a basis for the motivation and design of the micromachined devices produced as part of this doctoral thesis.

## 2.2   Single Neuron Physiology

The complexity of the CNS was not fully appreciated until the invention of the microscope. Prior to that time, nerve tissue was thought to be glands that passed fluids throughout the body [40]. The microscope unveiled a complex network of individual cells connecting all over the body. Each cell or neuron has a body from which two major processes, the axon and the dendrites, or collectively called neurites, extend as shown in figure 2-1. When the tips of these processes encounter a neighboring neuron, they may form physical connections to its cell wall, which enable electrical and chemical information to be shared between the two cells. The contact points, called synapses,
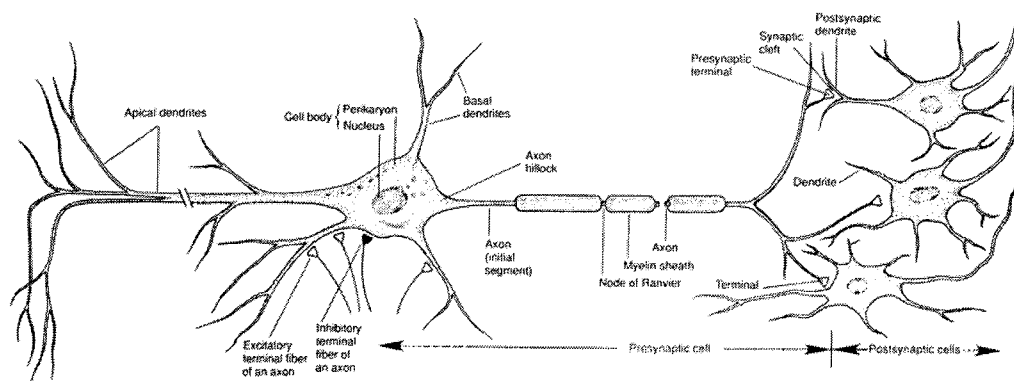


Figure 2-1: Stereotypical shape and attributes of a neuron [40].

allow biological neural networks to assemble that, in turn, perform the higher level functions of the brain.

It is difficult to specify a size for a given neuron due to the complexity of the cell. The diameter of the axon, dendrites and cell body can range from submicron to multi-millimeter in size and is dependent on both neuron type and animal type. The length, measured from the tip of the axon to the tip of a dendrite, can range from tens of microns to many meters. The diameter of a giant squid axon is on the order of millimeters. The axon diameter of human brain cells is from 0.2 to 20 microns [40].

When it was discovered that neurons convey information down the length of their bodies and from one nerve cell to the next, a giant leap forward to understanding the complexities of the brain was made. Technological advances in the relevant fields such as electrical and chemical sciences made possible work with the relative simple CNS of giant squids. In 1939, Hodgkin and Huxley [35] pioneered intracellular recordings of these cells using capillary micropipettes filled with saline solution. Once pierced through the cell membrane, the pipette becomes an excellent electrode capable of both recording and stimulating electrical activity in the neuron. This research explained how the all-or-none electrical pulses called action potentials, which are characteristic of nerve cells, are produced by ion gradients and voltage-gated ion channels. By understanding the mechanisms behind the action potential, the fundamental signal used by neurons to communicate rapidly over long distances within the body, research into how groups of neurons internally process external stimuli became possible.

## 2.3   The Action Potential

A full treatment of the generation, propagation and electrical properties of action potentials is provided in [40]. Presented here is an overview of the cellular processes responsible for the generation of these electrical spikes in neurons and is intended only to orient the casual reader. First, a physical model of a neuronal cell membrane must be introduced. This is shown in figure 2-2. Incorporated in the membrane of neural cells is a collection of active and passive ion channels formed by specific protein structures. While two ions, $Na^+$ and $K^+$, are the main driving force behind action potentials, a third ion, $Ca^{++}$, is usually included in general models. Not shown in figure 2-2, the passive channels work to expel or replenish ions that diffuse into and out of the cell due to concentration and electrical gradients. In the steady or resting state, the extracellular solution potential is typically 65 mV higher than the interior of the neuron. As drawn in
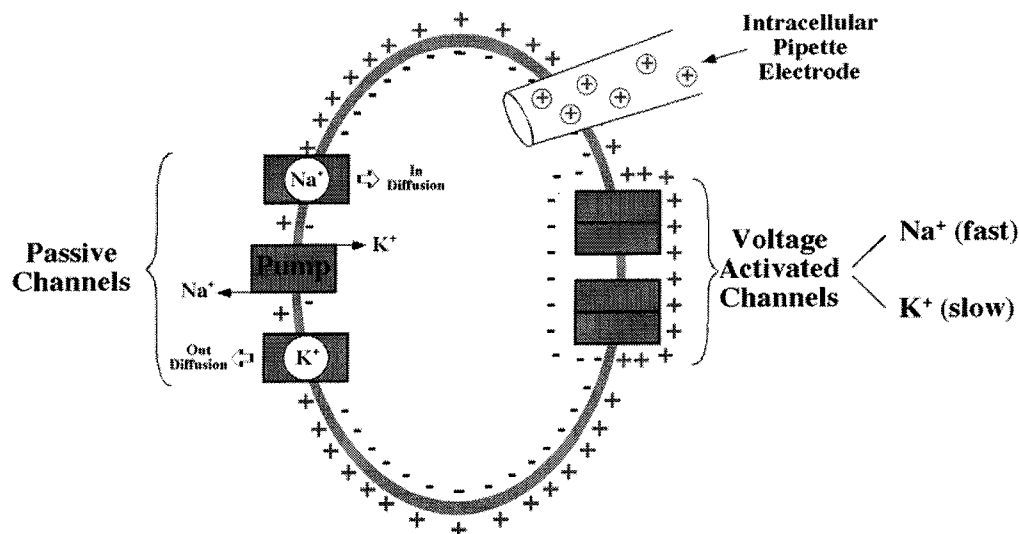
Figure 2-2: Schematic representation of the cell membrane and the ion channels contained within it. As shown the neuron is in its resting state.

figure 2-2, this produces a resting potential of $V_{cm}$ = -65 mV. In this state, the active or voltage-gated channels are closed and the only ion flow into and out of cell is through the passive channels. When a neuron becomes slightly depolarized, the voltage-gated channels still remain closed and the passive channels tend to return the cell interior to its resting state. Not until the depolarization exceeds the threshold voltage, or approximately $V_{cm}$ > -50 mV, does an action potential fire. At this point, an all-or-none response by the voltage-gated channels occurs. The $Na^+$ channels pull $Na^+$ into the neuron while the $K^+$ channels force $K^+$ out. The greater the depolarization, the greater the flow of ions across the membrane. The ion movement produces an electrical current that can be measured by both intracellular and extracellular electrodes.

The responses of the $Na^+$ and $K^+$ channels are self-sustaining and self-destructive in nature, respectively, and initiate and terminate the action potential. Figure 2-3a illustrates how the opening of the $Na^+$-gated channels further depolarizes the cell that results in a still greater influx of $Na^+$. Continued depolarization-runaway is avoided only



(a)                                                    (b)
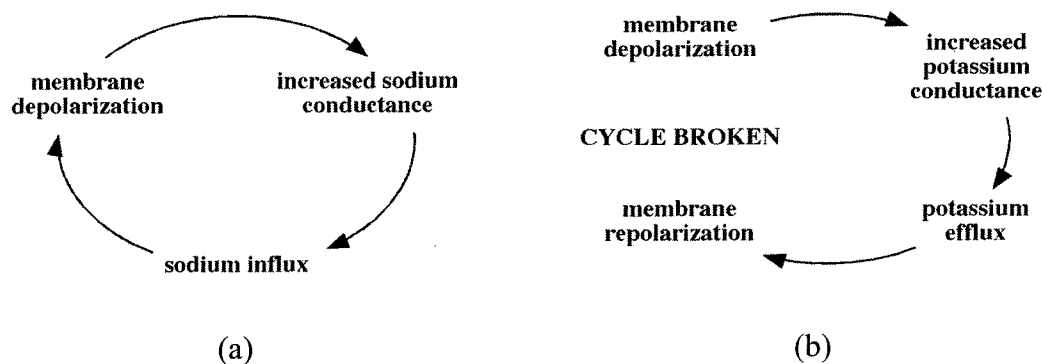
Figure 2-3: (a) $Na^+$ influx cycle is self-sustaining and extreme depolarization would result if the $Na^+$ channels did not "tire" quickly while (b) the $K^+$ outflux is a self-destructive cycle that repolarizes the cell and shuts itself off in doing so.

by the fact that the $Na^+$ channels can only sustain their ON state for a short period of time before shutting down and becoming inactive. A return to the resting potential of the cell membrane is then necessary to reactivate these channels. In the brief time that they are open, however, the cell becomes highly depolarized to approximately $V_{cm}$ = 55 mV. Reacting to this runaway depolarization, the $K^+$ channels slowly open forcing $K^+$ out. This creates a self-destructive cycle (figure 2-3b) that repolarizes the cell back towards its resting potential. As $V_{cm}$ returns to -65 mV, the $K^+$ begin to turn off. This does not happen immediately. The cell experiences a slight hyperpolarization until the passive channels are able to re-equilibrate the intracellular ion concentration to the true steady state.

If both the $Na^+$ and the $K^+$ channels were to open with equal strength at the start of depolarization, an action potential could never form. However, the quick and short duration of the $Na^+$ channels opening and the slow and steady response of the $K^+$ channels



(a)                                    (b)
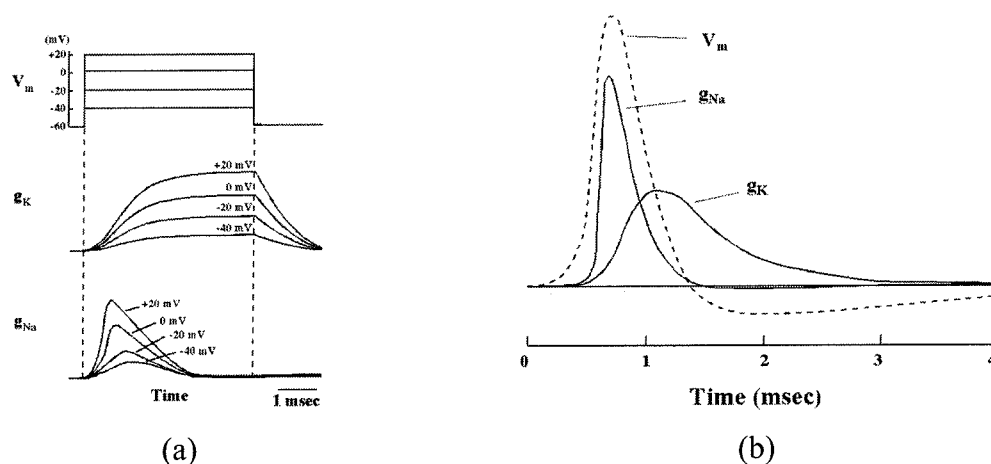
Figure 2-4:   (a) Relative speed and magnitude of the response each type of channel and   (b) how their effects on the membrane potential add together to create an action potential. Adapted from [40].

result in the 1 to 4 msec action potential spike characteristic of all neurons. Figure 2-4

details the relative speed and magnitude of the response of each channel and shows how

the voltage attributed to each channel adds to produce the action potential spike and its

all-or-none behavior. Figure 2-5 points out the distinct regions and the general values of

the action potential response.
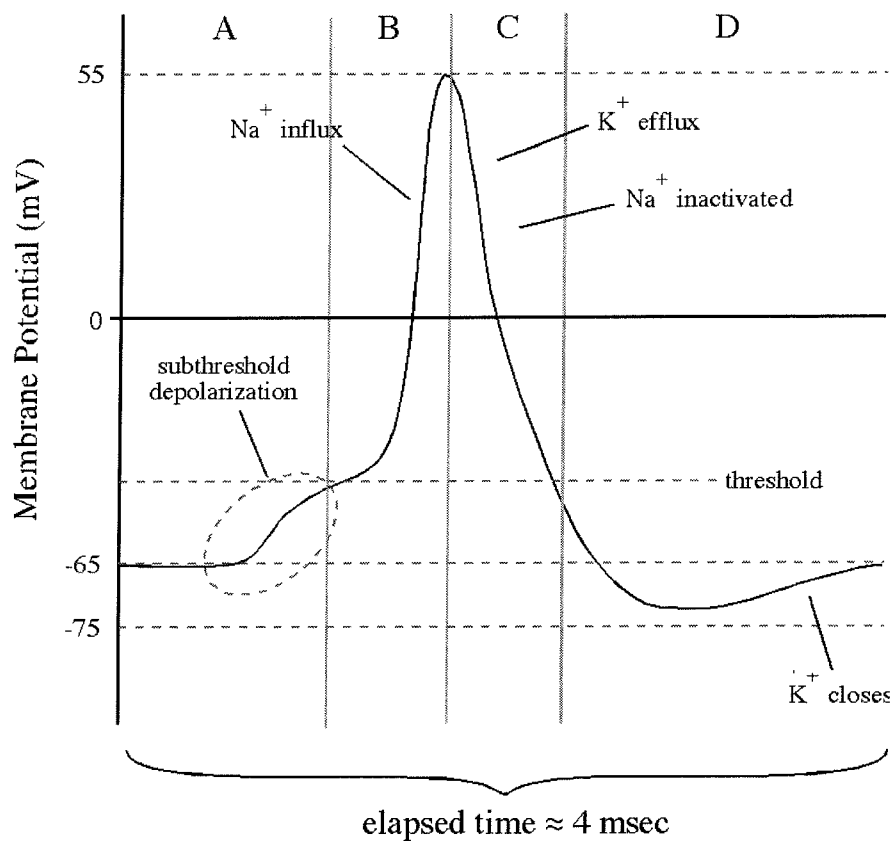


Figure 2-5: The stereotypical shape of an action potential elicited by an external triggering pulse. Region A shows the initial depolarizing impulse setting off the spike. In region B the fast acting Na+ channels depolarize the cell membrane to - 55 mV before, in region C, the response of the K+ channels begins to dominate driving the membrane potential to a slight hyperpolari-zation before completely shutting off. Finally, in region D, the passive channels return the cell to its resting state.

## 2.4   Cellular Recording Techniques

The goal of cellular recording is to capture the firing of action potentials in individual as well as groups of neurons. The sensitivity of the recordings is experiment dependent. Some investigations seek to simply detect the relatively large signal of action potential spikes. Others, however, demand access to the much smaller pre- and post-firing response as well as subthreshold signals seen by the neurons being studied. When working with large neurons, such as those in giant squids, good signal-to-noise ratios (SNRs) and sufficient neuronal survival can be achieved using intracellular recording. The study of mammalian cells requires finer, less invasive tools.

As studies of the much smaller neurons that comprise the human brain were initiated, existing techniques were refined and new tools were developed. The *in vitro* work with giant squids [35] used micropipettes with tips on the order of 100 microns in diameter. To study micron sized mammalian nerves, probe tips down to submicron size are often required. This was first achieved by Ling and Gerard in 1949 [44] who achieved intracellular penetration with good, highly resistive membrane seals around the pipette on the order of 500 megaohms. While still used to the present day, this technique does have its limitations. Since it requires impaling the target neuron, irreparable damage is done to the cell. The neurons rarely survive for more than several hours after the micropipette has been implanted. As a result, no long-term experimentation is possible.

For long-term studies, a non-invasive extracellular technique must be used. The most straightforward method to do this is to simply bring a metal electrode, or better, an

intracellular micropipette, into physical contact with the target neuron [26]. However, the SNR in such a scenario is significantly reduced as compared to intracellular recording. This is further worsened by the tendency of neurons to shift position over the course of hours, inevitably away from the electrode.

### 2.4.1   The Patch Clamp Technique

Improved SNR in extracellular recordings was achieved with a new technique dubbed the patch clamp. Using a micropipette similar to that used for intracellular recording, a pipette is pressed tightly against the neuron and a small portion of the membrane is sucked into the tip as shown in figure 2-6. In the least invasive form of patch clamping, the membrane is never penetrated so the cell is not damaged. When done properly, a gigaohm seal [33] is formed between the rim of the pipette tip and the

Channel

Ruptured
Membrane

(a)                                    (b)
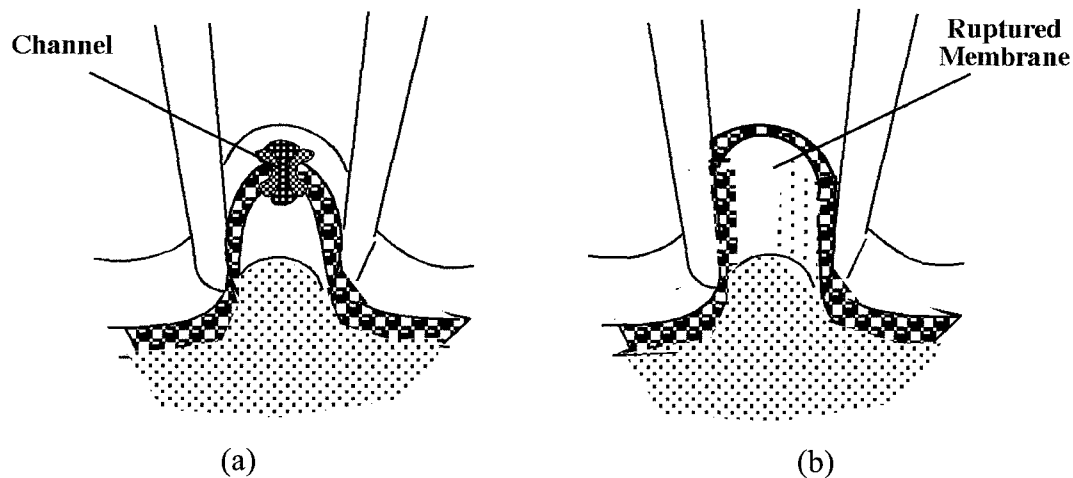
Figure 2-6: Pressing the tip of a pipette against the membrane of a neuron and applying gentle suction provides access to the interior of the cell by (a) isolating channels or by (b) inducing a rupture.

membrane. The portion of the cell in contact with the saline solution inside the bore of the pipette contains ion channels that provide an electrical connection to the interior of the cell. If desired, intracellular access can be achieved by causing the patch of membrane to rupture. This apparently causes minimal damage to the neuron as compared to traditional intracellular techniques. The gigaohm pipette-to-membrane seal that can be achieved by patch clamping makes possible measurements of neurons ranging down to just microns in diameter. Many variations of this technique such as the loose or whole-cell patch clamping are used today for a wide variety of electro, chemo and cytophysiological experimentation.

For long-term experimentation with large networks of neurons, patch clamping still has its drawbacks. To minimize damage to the cells due to movements of the pipette, a large manipulator stage must be used to position and hold the electrode in place. The size of these tools limits the number of pipettes to less than 10. Mounted to special vibration insensitive table, the manipulators are typically not installed inside the incubator in which the neurons are cultured. As such, continuous recording and stimulation is not possible. Rather, cultures are monitored for brief periods throughout the life of the experiment introducing the possibility that interesting, and perhaps important, neural activity is not being captured. To permit relatively large networks to be monitored, micromachining techniques began to be used to fabricate new recording devices.

## 2.4.2   Multielectrode Dishes

Using the same technology developed to lay down micron-sized wires on electronic integrated circuits, the bottom of culture dishes have been lined with insulated electrodes capable of single site extracellular recording and stimulation [55, 66, 71]. Such electrodes are capable of measuring changes in the cell potential via capacitative coupling. Figure 2-7 shows a neural network growing in the electrode region of such a dish developed at Caltech. These multielectrodes arrays are used for *in vitro* experimentation with semi-intact tissue such as retina [48] and brain slices [53], or with cultures of dissociated neurons [59]. In practice, the dishes are most suitable for large
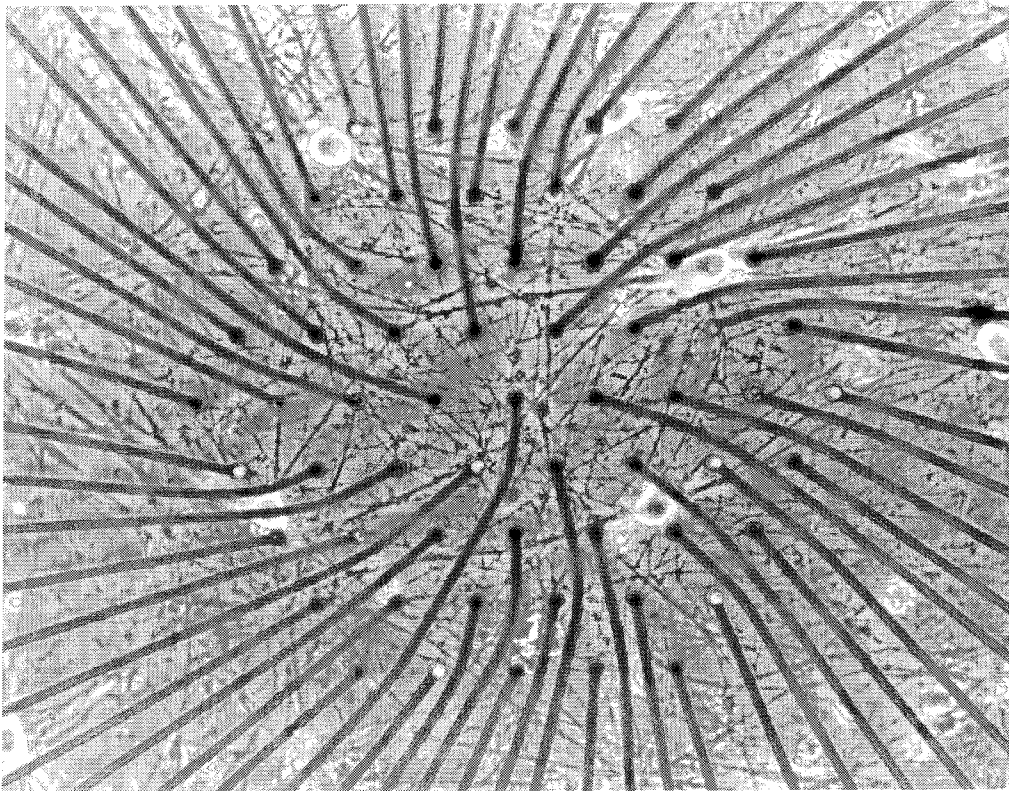


Figure 2-7:  Neurons growing on top of a multielectrode dish array.

invertebrate neurons that tend to grow over the electrode and form good electrical seals on the order of megaohms. This mimics loose-patch electrodes and recording and stimulation can be done reliably [57].

For smaller, more mobile neurons such as is seen in mammalian cultures, multielectrode dishes are less satisfactory. While extracellular recording and stimulation can be achieved even without direct electrode-to-neuron contact [55], the strength of electrical signals drops off rapidly with distance. In practice, the realized SNR is poor enough that postsynaptic potentials cannot be detected. Additionally, the random nature in which the neural culture is applied to the array is less than ideal. An electrode may record and stimulate from one, several or no neurons. Specificity between a given sensor site and a single neuron is never certain. Restricting the neurons to the immediate vicinity of the electrodes would result in more reliable recording and stimulation of specific cells. Attempts to constrain neurons to a specific electrode has been attempted by means of patterning cell adhesion molecules on a substrate [21] or by physical barriers to movement [22]. This thesis details the development a new chronic neural interface device that is an extreme example of a physical barrier.

## 2.5   *In Vitro* and *In Vivo* Experimentation

The ultimate goal of neurobiology is to understand the electrophysiology of individual neurons and how this building blocks interact in large groups to produce the high level functions associated with a complex central nervous system. To reach this

goal, experimental research with neurons in their host environment, or *in vivo*, must be done. When possible, the simpler technique of studying of biological neural networks cultured in a laboratory, or *in vitro*, is used. Each method of investigation has different benefits as well as drawbacks that dictate the use of one approach over the other. In practice, both techniques are used widely in research.

*In vitro* experimentation enables studies of specific regions of a CNS and of individual neurons. Working with the entire brain system of an animal requires understanding the operation of all its individual parts and how those pieces interact. To simplify the problem and to focus on a single region of neural function, brain slices are often removed and studied separate from the remainder of the CNS. This provides researchers direct access to the neurons in a given area of the brain. A prime example of the capability of the technique is demonstrated in [48, 53] in which up to 100 recording sites are monitored simultaneously. Such density is extremely difficult to achieve *in vivo* at the present time. In addition to slice work, cultures of dissociated neurons can be studied to answer questions such as how neural nets form and how long-term stimulation affects synaptic connections. A unique and intriguing potential of *in vitro* experimentation is the directed growth of biological neural networks. Predefined networks might be able to be formed and specific synaptic connections encouraged producing a neural "circuit" capable of useful computation. The cell recording tools described in the previous section are generally used for *in vitro* studies although slight variations of the methods can be used *in vivo*.

Studying the dynamics and interactions between the interconnected biological neural networks within the host animal requires the application of *in vivo* techniques. Gross imaging of relatively large numbers of neurons (on the order of millions, possibly as fine as many thousand) is often achieved using positron emission tomography or PET scans [40]. Overlaid on a three-dimensional magnetic resonance image of the target brain, those regions of the CNS that are active during high level processing can be pinpointed. This has been successfully used to definitively map the centers in predominant control of functions such as speech, vision and motor control. For finer detail and to allow external input to be introduced, electrodes must be inserted into the subject tissue. Early work used fine, insulated wires and wire bundles. In comparison to the neurons being observed, these electrodes are very large and in practice only a small number can be placed. Even for a relatively small implant, considerable damage is inflicted to the tissue and proper placement is difficult [42, 62, 63]. In recent years, significant improvements have been realized with the invention of micromachined probes [41, 50, 72]. Fabricated with micron-sized active regions positioned along a fine probe and available in three-dimensional structures, these devices can place dozens of electrodes into a host system while introducing no more tissue damage than caused by the implantation of a single wire. Such probes show great promise in chronic *in vivo* studies and open up the possibility of permanent implants capable of restoring sensory functions lost due to neural damage [52].

The drawbacks associated with *in vivo* and *in vitro* experimentation are largely complementary. Working with neurons in cultures permits easy access to the tissue and allows a variety of electrical, chemical and optical monitoring techniques to be employed. Probes can be accurately placed and moved during testing *in vitro*. In contrast, the nature of *in vivo* systems generally limits monitoring to electrical and magnetic resonance tools. Accurate placement during implantation is difficult and once in position it must typically be fixed in place. Data from cultured slices and dissociated neurons, however, does not necessarily capture the neural network activity present in *in vivo* tissue. Only experiments in a complete, living environment will provide such information. Additionally, there is no better incubator of live cells than the body of the host animal. While the use of the proper nutritional medium and environmental conditions can maintain culture viability for many months and even years, *in vivo* experimentation will always have better long-term survival.

For both *in vitro* and *in vivo* electrical studies of neural networks, attaining high signal-to-noise ratio signals from the neurons is crucial. In general, the proximity of an electrode to its target neuron sets the SNR. In the ideal case, the entire active area of the electrode is pressed against, or even penetrated inside, the cell wall and the resistance of the membrane-to-sensor seal is very large so that signal leakage to the extracellular liquid is minimized. In practice, such ideal conditions are difficult to attain and typically are possible for only a small number (less than five) of electrodes and for short periods of time (hours). When large sensor arrays are utilized, neuron-to-electrode distance is

typically random and non-zero.  For *in vivo* work the damaged tissue that tends to surround an implanted probe and separate it from direct contact with living neural tissue further worsens the situation [62].  A device capable of providing high SNR for a large number of neuron-specific sensor sites for both *in vitro* and *in vivo* research would be very beneficial.

## 2.6   Neuron-to-Electrode Specific Devices

In an attempt to achieve high SNR and one-to-one specificity between electrodes and neurons, two previous silicon microdevices have been developed at Caltech.  The first device, fabricated by Regehr [56], was a micro diving board structure with a cup-like electrode at one end of its long slender beam (see figure 2-8).  Attached to an insulated gold wire leading to external electronics, the electrode can be positioned over a neuron and then its base glued to the bottom of the culture dish. Both recording and stimulation
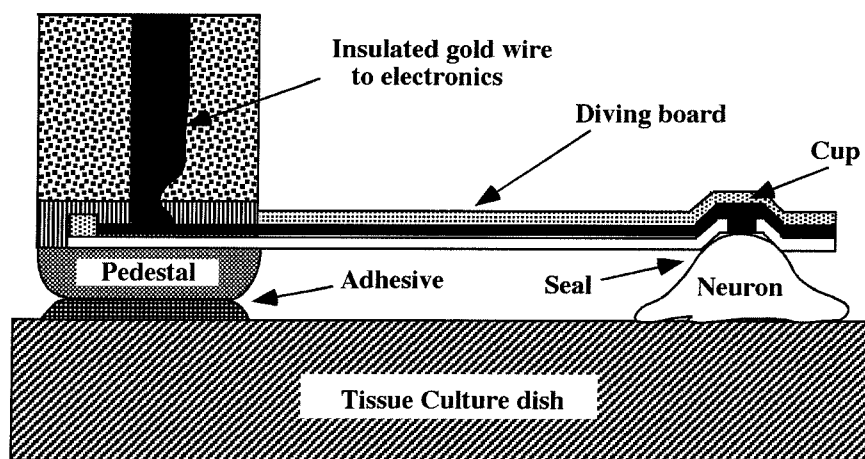
Figure 2-8:  Schematic of a micromachined diving-board electrode affixed in a culture dish and sealing against a neuron. (Adapted from [57].)
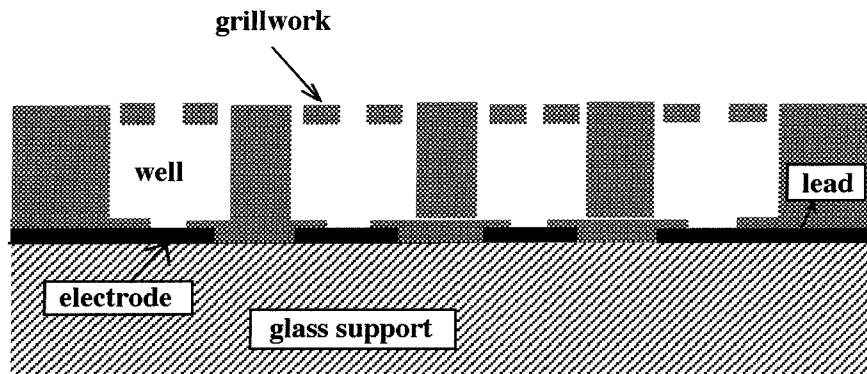
Figure 2-9:  Cross section of the evolved multiwell dish array.  (Adapted from [26]).

of neuronal activity can be achieved.  In practice, maneuvering the device into position and placing more than a few electrodes in a single dish proved very difficult [26].  By inverting the cup, fabricating it in a fixed position at the bottom of the culture dish and covering it with a specially designed grillwork, the diving board electrodes evolved into multiwell dish arrays.  A cross section of a line of these wells is shown in figure 2-9.

The multiwell dish arrays function in a similar manner to earlier multielectrode dishes with the unique feature being that the grillwork traps a single neuron to a single electrode throughout the life of the culture.  Unfortunately, the materials used in the construction of these arrays proved to be unstable when exposed to culture solution for extended periods of time.  The promising nature of this device prompted development of a new fabrication process using materials certain to be compatible with long-term neural cultures.  The result is a unique structure named the neurowell that can be arrayed into one, two and three-dimensional devices that can be used for chronic experimentation in both *in vitro* and *in vivo* environments.

# CHAPTER

# 3

# THE SILICON NEUROWELL

The requirements for a new neural electrophysiological instrument have been set. The device should be capable of chronic stimulation and recording of mammalian neurons in both *in vitro* and *in vivo* environments. Neuron-to-electrode specificity with good spatial resolution (both two- and three-dimensional) is desirable. Long-term biocompatibility and electrical stability is a must. For *in vivo* experimentation, a means of creating mechanically flexible, specific neural connections in the host system are of great benefit. This would minimize damage caused by as well as reduce the susceptibility to probe movement during long-term usage. Finally, the ability to place recording sites in an arbitrary, yet highly accurate manner is preferred. This would allow a variety of complex arrays to be produced by the same fabrication process.

To achieve these ends, a device micromachined from silicon was conceived. Based around a single microrecording structure, electrode arrays for both *in vitro* and *in*

*vivo* have been investigated. Through several design iterations the original concept has evolved into two new, fully functional devices called neurochips and neuroprobes.

## 3.1   The Neurowell Concept

Early work at Caltech [56, 57] has led to the development of a micromachined structure that houses an electrode for neural stimulation and recording. This innovation was subsequently named the neurowell and is shown schematically in figure 3-1 as it was initially conceived. The structure is formed from three main components: a micro cavity, a grillwork cover and an electrode (see figure 3-2).

The micro cavity has a three-dimensional truncated pyramid shape with a volume approximately the same as that of a mature neural cell body. In the case of this work, rat hippocampal pyramidal neurons are the target cells but the neurowell can be sized for any desired cell type. The use of hippocampal neurons led to forming microcavities that are
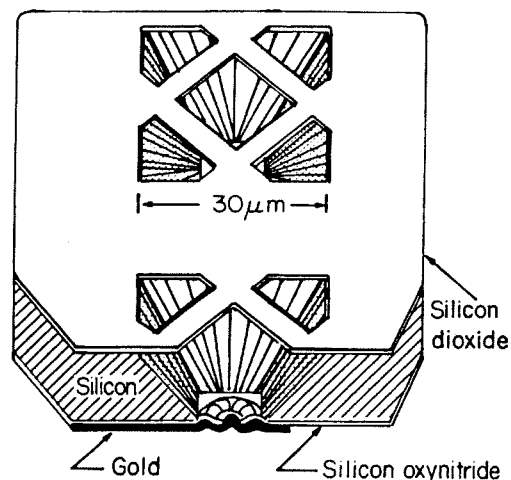


Figure 3-1:  Initial concept for a micromachined cage capable of containing, recording, and stimulating a neuron, making long-term experiments feasible.

16 microns deep, that are 30 microns square at their top and that have bases 8 microns square. Mature hippocampal neurons on a flat glass plate are typically pancake in shape and are about 20 microns in diameter and 5 to 10 microns thick.

Located in the center of the floor of the neurowell is an integrated gold electrode. Typically 6 microns in diameter, it is made of pure gold on the order of 0.5 to 2.0 microns thick. In the initial versions of the design, the electrode is rimmed by a 1 micron insulating step intended to simulate the tip of a patch clamp micropipette. Later neurowells did not include this feature and utilized a simpler, nearly flat bottom. Both electrode designs received an electroplating of platinum black (see section 4.2.2) which greatly increases capacitance and consequently the SNR of the well.

Covering the top of the neurowell is a specially patterned grillwork. A large hole, approximately 20 microns across, is located at its center. Around the periphery are smaller openings. Initial designs implemented simple holes of various shapes and sizes
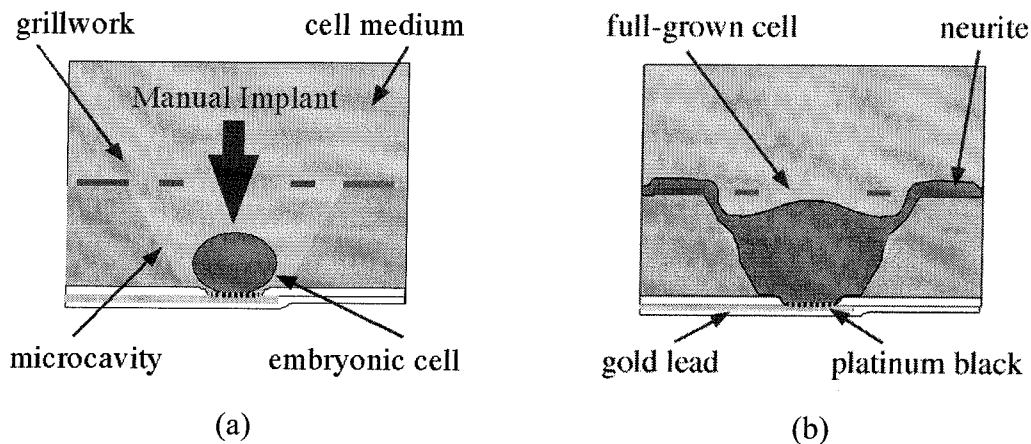


Figure 3-2: Schematic exhibiting the use of the neurowell. (a) Implantation of an embryonic neuron through the center of the grillwork. (b) As the cell grows it extends its axon and dendrites out through the fine features around the edge at the top of the microcavity, trapping itself against the electrode in the floor.

(see sections 3.2 through 3.4). The most recent and successful version incorporates microtunnels (see section 3.5). The central hole is sized to allow a freshly dissociated neuron to be loaded into the well but then traps the cell as it matures. Dissociated neurons are roughly spherical in shape and about 12 to 15 microns in diameter so they can just pass through the center of the grillwork. As the cell matures, it extends its neurites out into the surrounding environment (figure 3-2). The processes advance by attaching to and pulling on their surrounding environment. Assuming the neuron is sitting on the floor of the neurowell, the processes must first crawl up the sides of the cavity, which directs them towards the small peripheral holes or tunnels in the grillwork. As they thread through these openings, the neurites lock the cell body in the micro cavity where it remains trapped in close proximity to the gold electrode. For this scenario to be successful, the grillwork must offer no resistance to neuronal outgrowth; it must confine the cell body alone. If the cell body escapes, electrical stimulation and recording from that cell are impossible. Conversely, if the axon and dendrites are unable to extend out of the cavity, biological neural networks cannot form.

## 3.2    Neurowell Evolution

Mammalian nervous systems have arrived at their present form through millions of years of evolution enabling their hosts to contend with their ever-changing environments. So, too, has the neurowell been forced to evolve from a simple micro cavity with bars across its top into a much more complex structure. As might be expected, neurons do not willingly enter the wells nor do they grow in the manner desired

by their human experimenters. Structures considered small in the general scheme of the devices have been shown to be large obstacles to neurites. When these barriers are overcome, the cell bodies exhibit a strong desire and capability of exiting the confines of the small cavities, preferring the unencumbered environment outside of the wells.

In arriving at a biocompatible neurowell design, three major well types were fabricated and tested. Each iteration provided valuable data leading to an understanding of the conditions and structures preferred and tolerated by rapidly growing neurons. In the final round, a functional neurowell that can be readily fabricated has been produced and is presently being used in the laboratory. The trail leading to this device is outlined in the following sections.

## 3.3   The Prototype Neurowell

The prototype fabrication process sought to create neurowell arrays for both *in vitro* and *in vivo* devices by using purely bulk micromachining techniques. For *in vivo* experimentation, minimal invasiveness is a stringent requirement. This demands that the portion of the device to be implanted displace a minimal volume of brain tissue. At the same time, it is often necessary that the active sites be placed relatively deep in the target nervous system. To achieve this, it was determined that the neurowells must be fabricated on a very thin and narrow needle support. This constraint led to a process that forms the neurowells on a 16 to 20 micron thick silicon membrane. For the neurochip, the membrane is fully intact after dicing of the wafer. For the neuroprobe, an additional step carves the membrane into hair fine silicon needles along the length of which lie the

neurowells. In this way, a single process run can be used to produce both *in vitro* and *in vivo* devices with no special care given to either wafer type.

This approach led to a two sided process in which the three-dimensional structure of the wells is formed from the backside of the wafer and the electrical interconnects and electrodes are formed on the front. An optional dimple feature around the electrode can be included in this process. The dimple was tested to see if it would improve sealing between an implanted neuron and the electrode. Neurochips and neuroprobes have been fabricated with this process and experimentation with superior cervical ganglion (SCG) neurons led to the first successful demonstration of neurite outgrowth from these novel devices.

### 3.3.1 Prototype Neurowell Fabrication

Key to the fabrication of this generation of neurowell design is the use of silicon epi-wafers as the starting substrate. Totaling 500 microns thick, the purchased wafers consist of three distinct silicon layers shown schematically in figure N1-1 in appendix N1. The base of the wafers, approximately 500 microns thick, is standard lightly doped (1 - 10 •-cm), single crystalline silicon. On this starting substrate, a 4 micron thick, heavily p-type doped epitaxial silicon layer is grown. A final lightly doped layer of epitaxial silicon 16 microns thick then covers the well. Both boron and boron/germanium heavily doped buried layers have been used and their traits are discussed further in appendix N1. Additional issues concerning the use of these epi-wafers is discussed in appendix N2. In the final devices, the 500 lightly doped silicon becomes the supporting

pad frame or the handle for the neurochip and the neuroprobe respectively. The heavily

doped silicon buried layer is formed into the grillwork and the 16-micron thick top silicon

layer is etched to form the micro cavities of the neurowells.

The complete process containing all processing steps in detail is included in

appendix N5. The following is a brief synopsis of the overall process and these major

steps are shown in figures 3-3.

The steps described in this paragraph are used to form an oxide dimple at the

bottom of the fabricated neurowell. These steps are optional and subsequent well designs

eliminated them from the process. Beginning with the commercially available epi-wafer

described above, 50 nm of dry thermal oxide is grown on the wafer. A 0.5-micron layer

of low-stress LPCVD nitride is then deposited. The 50 nm of oxide acts as a stress-

relieving layer and plasma etch stop for this nitride. The two layers are patterned with a

single mask to form 6 micron nitride/oxide "islands" in the neurowell region and 10 mm
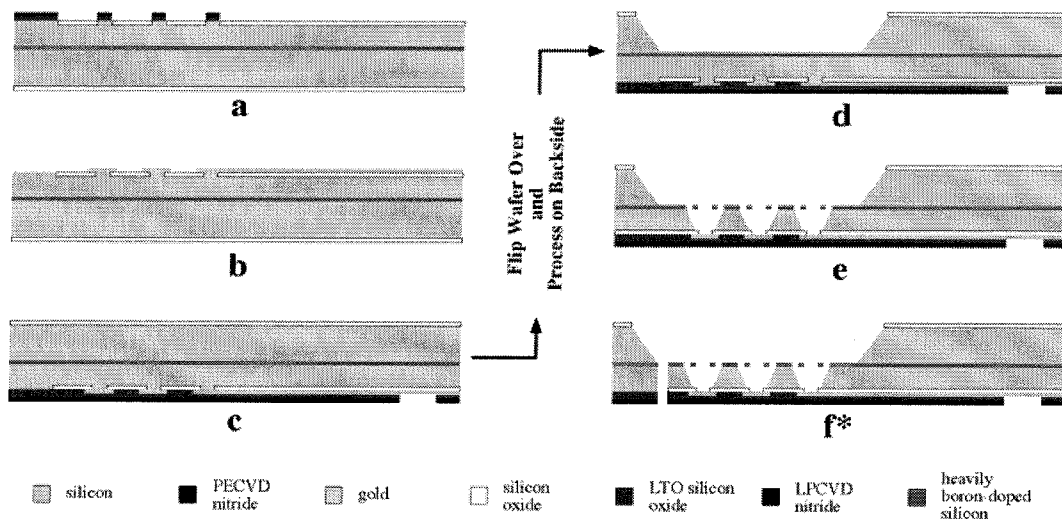


Figure 3-3: Fabrication cross sections for the prototype neurowell fashioned into
a probe or a chip.

x 1.8 mm windows in the bond pad areas. The freshly exposed silicon is further recessed by 0.4 microns with isotropic etchant. A fully recessed LOCal Oxidation of Silicon (LOCOS) grows 1 micron of thermal oxide from all areas with exposed silicon. The LOCOS also acts to replanarize the surface of the wafer. In the final neurowell, this creates a 1-micron oxide step surrounding the gold electrode at the bottom of the micro cavity. Figure 3-3.a shows the cross section to this point. In preparation for the next major step, the nitride is selectively stripped from the wafer and the pad oxide removed with a short buffered hydrofluoric acid (BHF) dip. Only the thick field oxide grown in the LOCOS step remains on the wafer.

Gold recording electrodes, interconnects, and bond pads are laid down next. This can be done with either a liftoff or metal etch process (figure 3-3.b). Liftoff is preferable as the resulting traces are much more crisply defined and very fine line widths and spacings can be achieved. In practice, liftoff is used for the neuroprobe wafers where the fine lines are needed while metal etch is used for the neurochips which have much large features. In both cases, Cr/Au/Cr (10 nm/200 nm/10 nm) is thermally evaporated onto the wafers. Here, the Cr acts as an adhesion layer for the gold. Gold alone would readily peel from the wafer. Likewise, the subsequently deposited 0.5 micron thick low temperature oxide (LTO) insulating film would flake off of pure gold while the top Cr layer is an excellent surface for such a deposition. For stress compensation and biocompatibility, 1 micron of PECVD nitride is deposited over the LTO. This cancels the large compressive stress in the underlying films. Additionally, the nitride covers the hydrophilic LTO. For long-term applications, it is believed that hydrophilic insulation

layers are inappropriate as they tend to swell when immersed in saline solution [32]. The insulation is patterned to expose the metal bond pads to which gold wires are attached at the end of the process. The cross section in figure 3-3.c illustrates the wafer at this stage.

At this point, processing on the front or epitaxial side of the wafer is complete and the substrate is flipped over and the processing is continued. During the LOCOS step described above, the backside of the wafer was also coated with 1 micron of thermal oxide. Windows 9 mm x 5 mm are etched to expose the underlying silicon substrate using a photoresist mask and BHF. The remaining field oxide becomes the masking material for an ethylenediamene-pyrochatecol (EDP) anisotropic silicon etch. The etch is allowed to progress all the way down to the 4 micron thick buried silicon etch-stop layer. EDP does not etch heavily doped p-type silicon and the result is a perfectly smooth silicon surface. Note that the front side of the wafer requires no special protection from the EDP, as all exposed surfaces are nitride, oxide or gold. Upon completion, the anisotropic etch has formed a 4 x 8 mm membrane that is approximately 20 microns thick as seen in figure 3-3.d.

All processing from this point on is performed on the relatively fragile silicon membranes. In practice typical fabrication steps do not break the membranes. Not applying vacuum to one side of the wafers is the only special care that must be taken. This requires that the vacuum chucks used by machines such as projection steppers and photoresist spinners must be bypassed. Careful hand loading of the wafers and/or special chucks (see figure N2-1 in appendix N2) virtually eliminates membrane breakage during processing. Other issues associated with micromachining in membranes and at

the bottom of deep cavities are covered in appendix N2.

The heavily doped epitaxial silicon layer, now exposed on the backside of the wafer, is patterned into the grillwork of the neurowell. Very accurate alignment to the features already present on the front side of the wafer must be achieved in this step. Appendix N3 describes the two techniques that have been used successfully to accomplish this requirement. With alignment attained, photoresist is spun and patterned to act as a reactive ion etch (RIE) mask. Using RIE, the mask pattern can be etched down into the silicon with minimal undercut. A vertical-to-sideways etching ratio of 4-to-1 is typically achieved. Care must be taken to etch only the heavily doped silicon epi-layer. The issues discussed in section 3.3.4 are exacerbated if the underlying lightly doped silicon epi-layer is penetrated. An ideal grillwork etch is shown in figure 3-15. In practice achieving this ideality is nearly impossible, especially across all dies on a wafer.



(a)                                              (b)
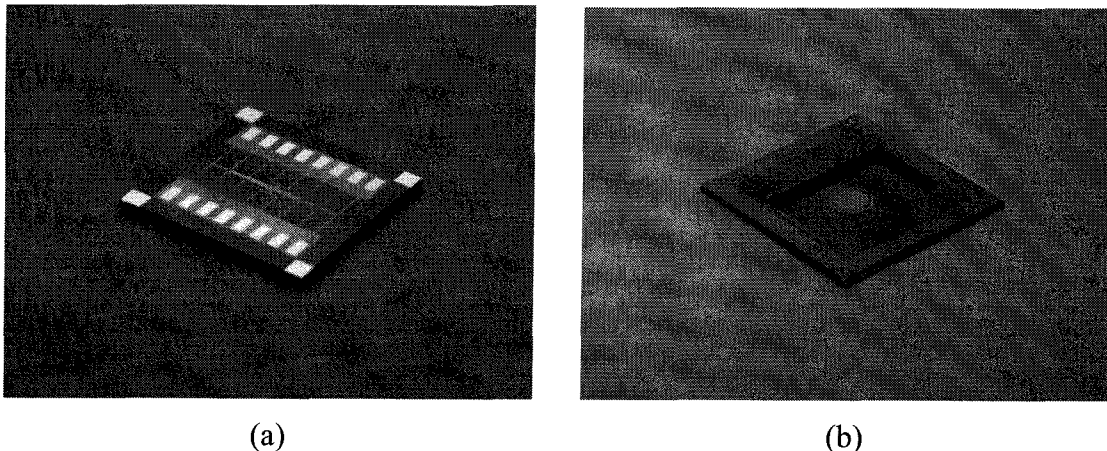
Figure 3-4: Neurochip dies after dicing. (a) The electrode side of the 1 cm-square die with thin wiring traces and large bond pads of gold visible. (b) The active side of the chip showing the 20-micron thick membrane at the bottom of the large 5 x 9 mm area, 500 micron deep cavities at the center of which is an array of neurowells.

Micro cavity formation is the final step in the formation of the neurowells. The wafers are again etched in EDP. This creates a truncated pyramid shaped hole beneath the patterned heavily doped silicon grillwork that is acting as the EDP etch mask. To minimize undercut, the length of the etch is kept to a minimum by frequent removal and monitoring with a microscope. The etch is determined to be complete when the gold electrodes on the front side of the membrane can be seen in the center of all the grillworks on the backside. A dip in chromium etchant strips the Cr adhesive layer exposing pure gold electrodes at the bottom of all the wells. At this point (figure 3-3.e) the neurochip process is complete save for dicing into 12.7-mm square dies. Photographs of such dies are shown in figure 3-4. Figure 3-5 is an SEM picture of the neurowell array in such a chip.
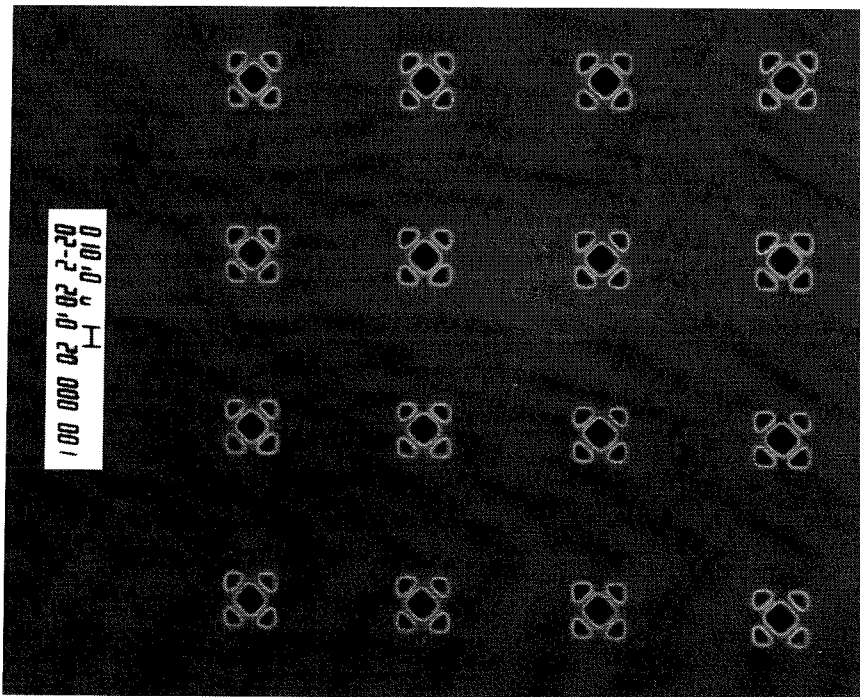


Figure 3-5:  SEM of a 4 x 4 array of neurowells fabricated into a neurochip.

One final step is required to produce neuroprobes as shown in figure 3-3.f*.  On the electrode side of the wafer, aluminum is deposited and patterned in the standard needle shape of the probes.  Using an RIE, trenches through the entire thickness of the membrane containing the neurowells are etched to complete the neuroprobes.  It should be noted that the probes are not diced from the wafer.  During the formation of the membranes in the steps described previously, score marks through the thickness of the wafer are also etched in the probe wafers.  This permits the individual devices to be snapped free of the supporting silicon wafer.  A dip in aluminum etchant to remove the RIE etch mask and the neuroprobes are ready for use.  Several completed neuroprobes are shown in figure 3-6 while figure 3-7 is an SEM picture of the linear neurowell array at the end of the silicon needle.
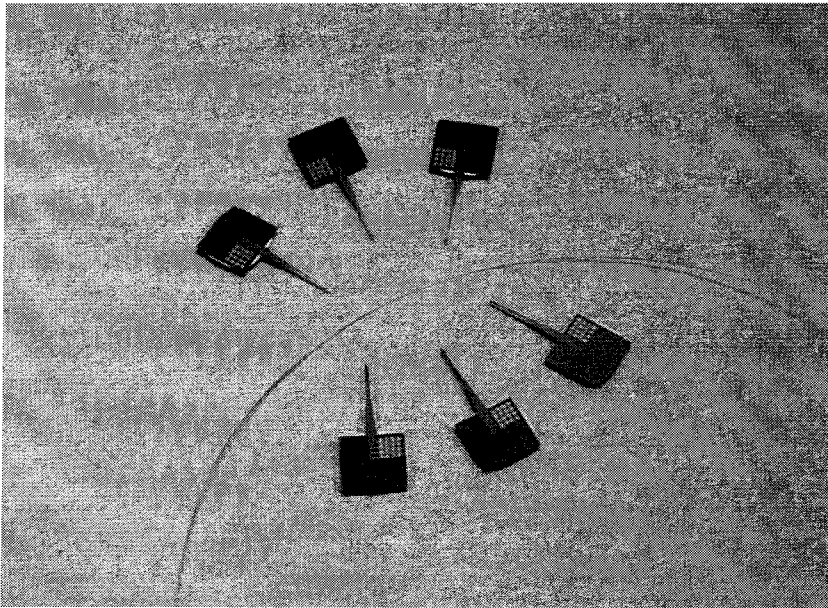


Figure 3-6:  Six fully functional neuroprobes with their silicon needles containing 15 prototype neurowells pointing at a strand of hair.  The hair is approximately 100 microns in diameter while the needles are 4-mm long, 120-microns wide and only 20-microns thick.
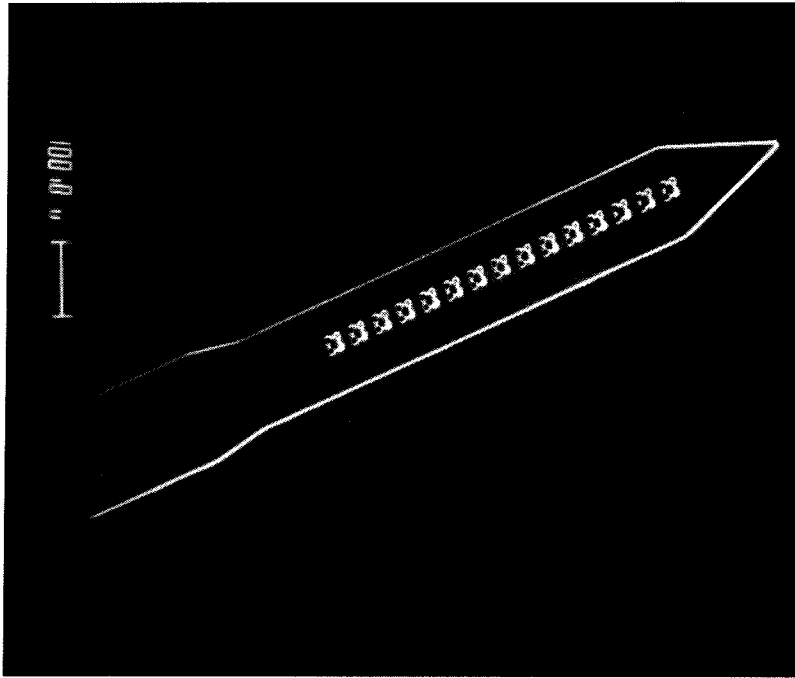
Figure 3-7: Photograph showing the end of a 4-mm-long neuroprobe needle containing 15 neurowell of the prototype design.
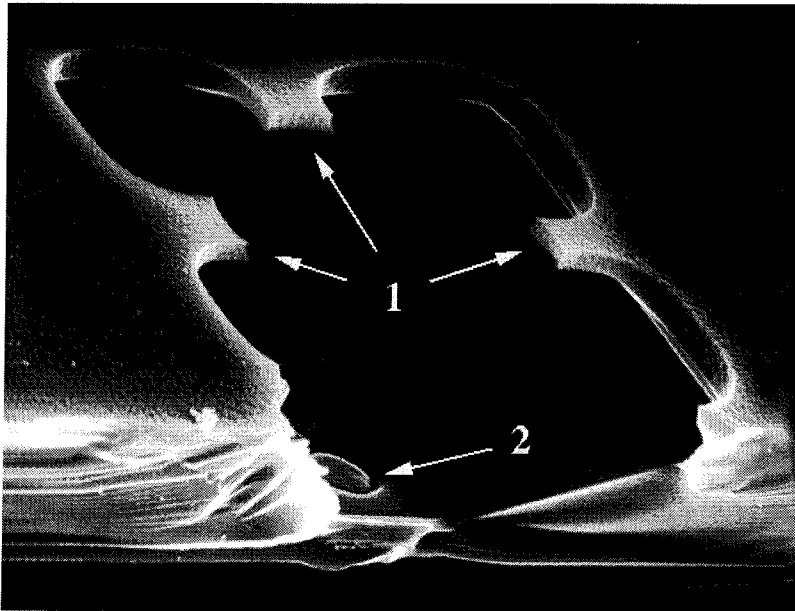


Figure 3-8: Close-up view of a prototype well that has been cross-sectioned after fabrication. (1) indicates the thick ($\approx$ 3 microns) boron-doped silicon grillwork and (2) points out the gold electrode surrounded by a 0.8-micron high oxide dimple.

The prototype process successfully generates all of the structures sought in the first neurowell design. The SEM photograph of a well cross section shown in figure 3-8 confirms all of the salient features. The grillwork proved to be quite thick, on the order of 3 microns. At the bottom of the truncated pyramidally shaped micro cavity, the gold electrode can be readily seen. This particular well incorporated the oxide dimple surrounding the electrode. Close inspection shows that it has the desired step height of about 1 micron. Once produced, research with implanted neurons began.

### 3.3.2   Prototype Neurowell Experimental Results

Initial neurophysiological research was conducted with neurochips fabricated with 4 x 4 arrays of the prototype neurowells. Individual chips were mounted as shown in figure 3-9 and described in section 3.4.1. The first neurons cultured in neurochips were
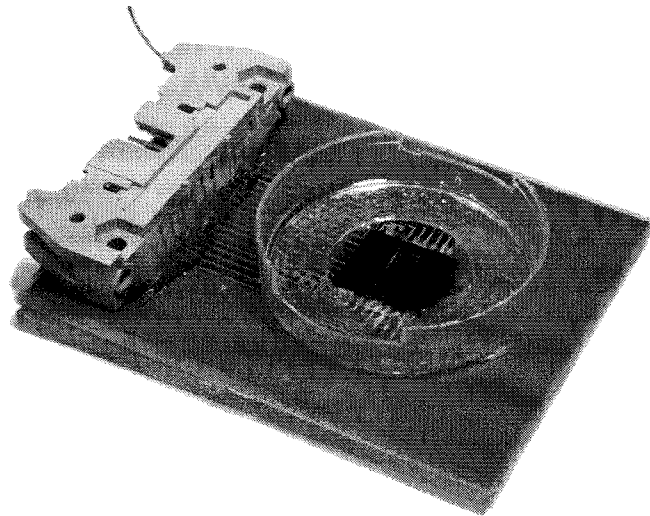


Figure 3-9: Neurochip mounted to a printed circuit board with a 25-pin ribbon cable connector. During culturing, the entire assembly is placed in a $CO_2$ incubator. When stimulating and recording from the array, the connector quickly interfaces the chip to a bank of dedicated electronic equipment.

neonatal rat SCG cells.  While the ultimate goal is to use neuroprobes in conjunction with

rat hippocampal pyramidal cells, SCGs are easier to culture in several respects.  The cells

come from an easily accessible sympathetic ganglion in the rat neck.  Once dissected and

implanted into neurowells, the neurons grow to fill the micro cavities in just a few days.

In suspension, a single cell type is easily identified of which 75% or more grow axons

and dendrites after plating in culture.

The first culturing attempts with the prototype neurowell neurochips produced

very promising results.  The Nomarski photograph in figure 3-10 shows a network that

has grown for 48 hours.  The background pattern is an optical artifact described in

appendix N1.  Despite this interference, the picture clearly shows a large number of
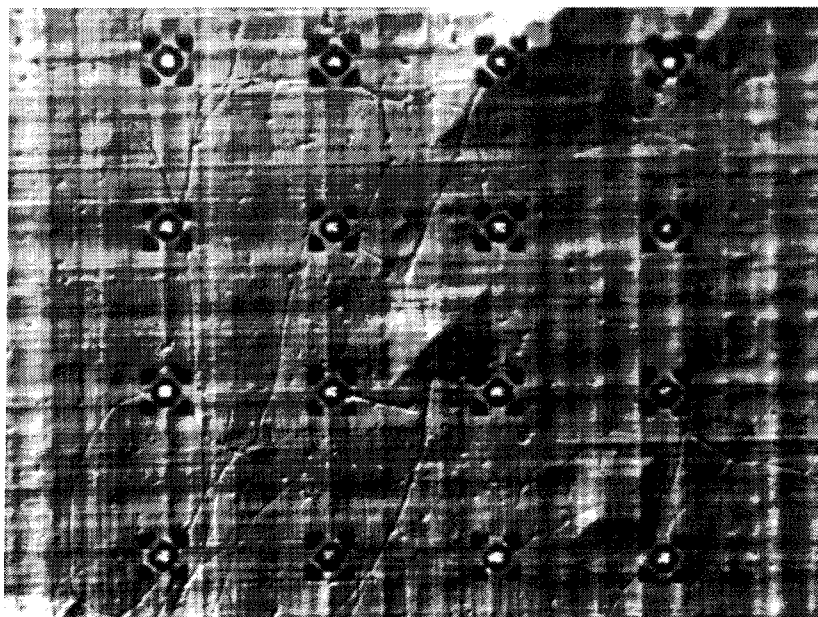


Figure 3-10:  This Nomarski photograph shows the typical 4 x 4 array of wells used in the neurochip.  These are prototype wells with implanted SCG neurons growing in them.  Though difficult to see with the "linen" pattern back grown (see appendix N1), the fine lines running between the wells are neural processes.

neurites growing from the neurons (not visible) in the wells. Of the 16 wells, all but 3 to 5 show successful neuronal outgrowth.

Survival lifetimes of preliminary cultures proved to be to short to enable electrophysiological testing to be completed. While neurons implanted into neurowells lived as long as controls grown in the same and separate dishes, cell culture limitations and fungal infections inevitably killed off the networks before they became electrically active. Instead of implementing more advanced techniques for SCGs, work to successfully grow long-term hippocampal cultures, the ultimate target system of this research, was undertaken. Outgrowth of hippocampal processes was extremely disappointing; only 1% of 588 neurons loaded into this neurowell design extended neurites. All cells died within 2-3 days. This remarkably poor outgrowth indicates that the prototype neurowell design is at least partially bio-incompatible. The evidence as to the cause of the incompatibility came from work, being conducted in parallel to the standard prototype design, to produce neurowells with transparent grillwork.

### 3.3.3    Prototype Neurowell Variations

Physically, a neuron can be thought of as a very thin, transparent "bag" filled with saline solution. Imaging the cell is difficult when on a mirror smooth surface. If placed on a textured substrate the neuron becomes all but invisible. To improve their visibility, cultured neurons are often stained with dies. An excitation light produces a fluorescing response from the cells that can easily be viewed or photographed. The high visibility of

neurons stained in such a manner and implanted in canopy neurochip (described in section 3.5) is shown in figure 3-11. In the case of the prototype neurowell design, however, the opaque material used to form the grillwork greatly inhibits this technique.

The heavily doped silicon grillwork reduces the fluorescent signal by as much as 75%. The opaque bars cover about 50% of the neurowell opening. This blocks 50% of the excitation light from entering the well and striking a stained neuron. Likewise, 50% of the fluorescing light produced by the dye is trapped within the well. By creating transparent grillwork, a factor of 4 increase in detected light can be achieved, greatly improving signal to noise ratio. Stronger signal returns are attained, or alternatively, the staining level (which is slightly toxic) of the cells can be reduced to improve culture
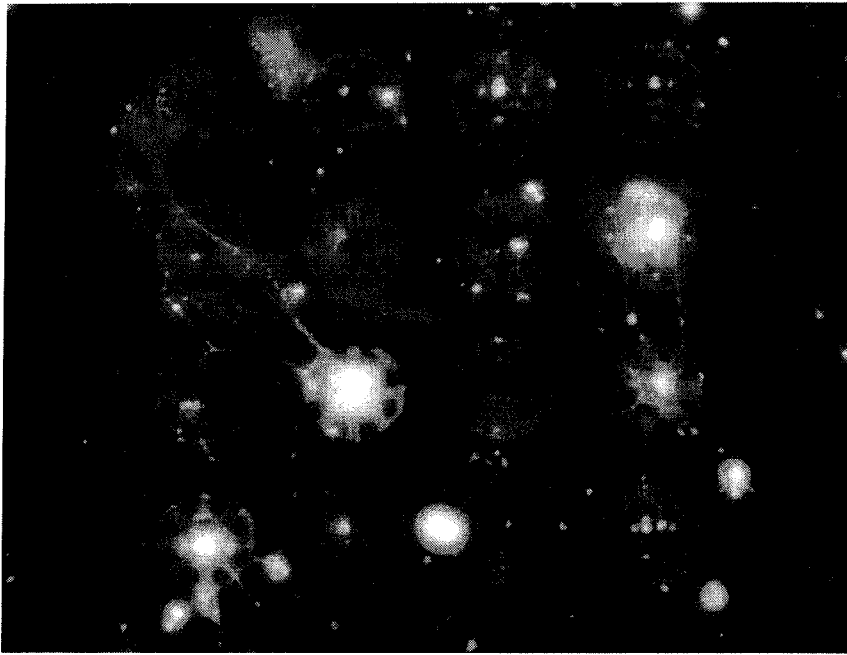


Figure 3-11: Color photograph of a living neural network grown in a canopy well array. The neurons were stained with a fluorescing-die prior to implantation allowing them to be readily viewed when excited by the light of a mercury lamp.

survivability.   A grillwork covering that is transparent would greatly improve the capabilities of devices incorporating neurowell.

In addition to achieving a transparent neurowell cover, improving the manufacturability of the devices also led to a modification in the fabrication process.  The original prototype neurowell fabrication process is a robust method of producing both neurochips and neuroprobes save for one step:  definition of the grillwork in the relatively thick heavily doped epitaxial silicon layer.   The difficulties with this step stem from several sources.  First, the lithography is done at the bottom of a 500-micron deep cavity. The issues associated with this are covered in detail in appendix N2.  Suffice it to say that patterning the sub 5 micron grillwork features in the 4 to 6 micron thick photoresist needed for an adequate RIE etch mask is difficult, even on a flat wafer.  Second, the RIE plasma used to transfer the photoresist pattern into the silicon etches heavily doped and lightly doped silicon at the same rate.  Thus, stopping at the interface between the two epitaxial layers is very difficult to control.  It must be accomplished by measuring the change in step height in the grillwork features during the etch.  But the RIE plasma etches both the silicon and the masking photoresist making an accurate measurement difficult. Additionally, the etch rate varies from die to die across the 10 cm wafer.  Finally, the step height is measured by an Alpha-Step 200 Surface Profilometer [12] that drags a stylus, attached to the end of a beam, over the features.  Deflection of the tip of the beam is monitored and the resulting data are used to calculate the step height.  As the tip of the stylus is 2 to 5 microns in diameter, similar to the dimensions of the holes being etched in

the silicon, there is significant room for error in the measurement. Such inaccuracies lead to the overhang issues discussed in section 3.3.4. A modification to the fabrication process that eliminated these difficulties was developed.

The solution to the patterning problems that also produces transparent grillwork is achieved by using either nitride or oxide in place of the heavily doped epitaxial silicon. Since both nitride and oxide are deposited or grown at temperatures higher than are compatible with Cr/Au/Cr features, the process flow for the prototype neurowell described above was slightly altered and this new procedure is given in appendix N6. Instead of depositing the Cr/Au/Cr metal layers near the start of the process, these steps are performed after the grillwork is patterned. The heavily doped epitaxial silicon is still used as the EDP etch stop for membrane formation. After the EDP step, the heavily doped silicon layer is stripped with a selective isotropic etch. The remaining 16-micron



(a)                                           (b)
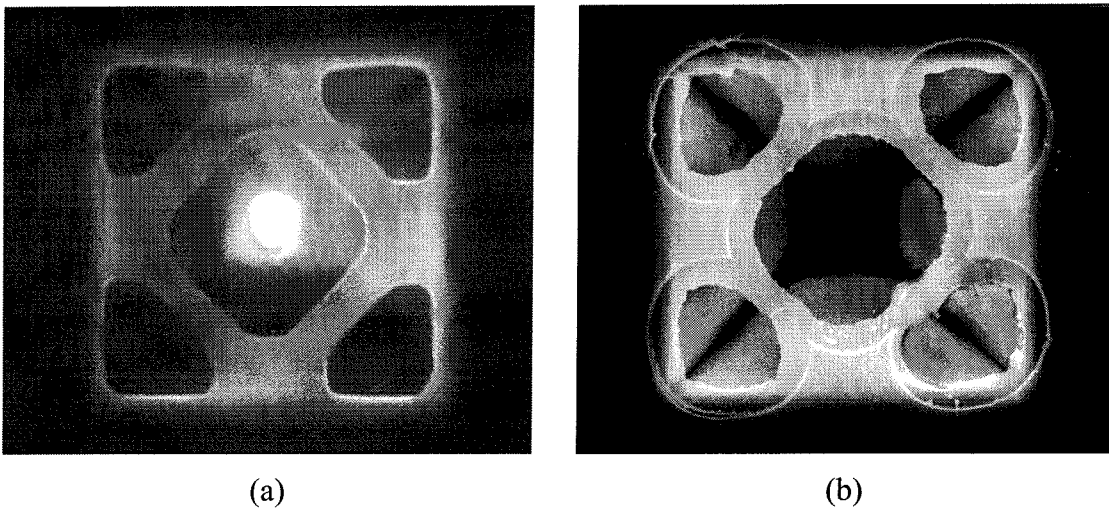
Figure 3-12:  Two photographs of the prototype variation wells fabricated with optically transparent grillwork material:  (a) LPCVD nitride patterned by plasma and (b) thermal oxide patterned by wet etch.

thick silicon membrane is coated with 1 micron of low stress nitride or thermal oxide. This much thinner grillwork material is still very robust mechanically and can be masked with relatively thin photoresist, on the order of 1 micron. An isotropic plasma that etches nitride more rapidly than silicon can be used to minimize penetration into the underlying epitaxial layer. In the case of oxide patterning, a wet BHF etch is used which does not etch silicon in any way. This permits a time insensitive etch to be used while still ensuring the material removal stops at the oxide/silicon interface. Neurowells produced using both of these materials have been fabricated and are shown in figure 3-12.

Hippocampal neuron outgrowth from the modified prototype neurowell design is more successful than with the original structures. Unfortunately, neurite development is inconsistent from one chip to another as well as from culture to culture in the same device. Overall, the results achieved were unsatisfactory. Examination of the neurowells provided circumstantial evidence that a physical overhang around the edge of the micro cavities was at least partly to blame for the lackluster outgrowth. This realization eventually led to further modifications of the fabrication process and the generation of a zero overhang neurowell design.

### 3.3.4   Overhang Bio-Incompatibility

Investigations into the lackluster neural outgrowth from prototype neurowells revealed that neurites are unable to climb past even small physical overhangs surrounding the micro cavities. The problem is illustrated in figure 3-13 showing a well with

overhang on the right edge and no overhang on the left.    Growth cones at the ends of

neurites pull the processes up the sidewalls towards the holes in the grillwork.    The

growth cones are typically very flat:    approximately 2 to 3 microns wide but only 0.1 to

0.2 microns thick.    When they encounter even a slight overhang, no part of it can extend

over the barrier and the cone cannot establish a foothold beyond the well.    Previously, the

amount of overhang was unclear, but it was assumed to be much less than 1-micron wide

and to have little effect on the cells.    Instead, closer inspection revealed that the EDP etch

regularly generated 1 to 2 microns of overhang.    In experiments with neurons, it was

shown that overhangs as small as 0.5 microns can prove to be insurmountable obstacles

to developing neurites.    If the neurites fail to escape the well within 24 to 48 hours after

implantation, the neuron inevitably dies as evidenced by cellular debris in wells once
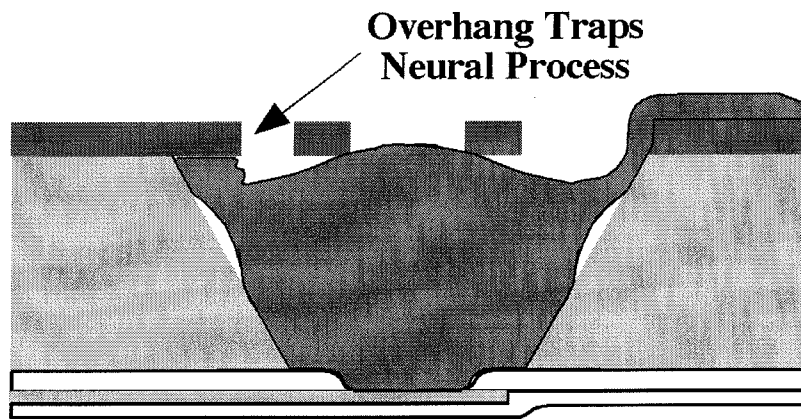


Figure 3-13:    Shelf-like overhang around the perimeter of neurowells poses a significant challenge to neural processes.    This schematic shows how a neurite encountering such a barrier (left side) is trapped in the well while a second process easily climbs the walls of the microcavity and grows out into its environment.

containing cell bodies.

Cross sectioning of several prototype wells eliminated all doubt that overhang is present in the fabricated structures and in some cases is extremely severe. The SEM in figure 3-14 shows the problematic shape of the wells. Instead of having sidewalls that slope down from the grillwork to the floor of the well at a 54° angle creating the expected truncated pyramid chamber, this well has a "hexagonal" shape. The amount of this type of distortion varies from well to well and, in some, is not present at all. Most, however, show at least a slight amount. The SEM shows one of the more extreme cases. It should be noted that such symmetry is rare. Most of the deformed wells showed little distortion on one side and gross distortion on the other. This is evidence that the RIE does not etch the grillwork uniformly, even on a per well basis.
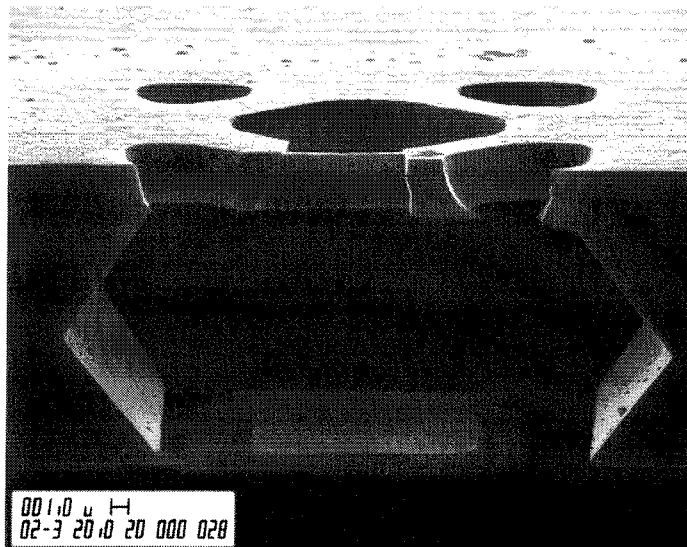


Figure 3-14: SEM photograph showing a grossly deformed neurowell as an example of an extreme case of overhang arising from the fabrication process. Overetch of the thick (≈ 3 micron) boron-doped silicon grillwork into the underlying lightly doped silicon resulted in the anisotropic wet-etch forming a hexagonally shaped well.

(a)                                                    (b)
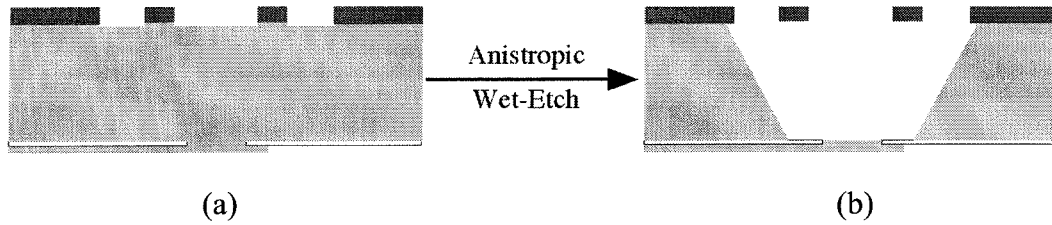
Figure 3-15: Ideal processing required to realize minimal overhang or grillwork material around the perimeter of a prototype neurowell. In (a), a plasma etch patterns the grillwork material stopping before there is significant penetration of the lightly doped silicon beneath. Following an anisotropic wet etch (b), the perimeter of the top of the microcavity is nearly flush with the edges of the grillwork and presents a negligible barrier to neurite outgrowth from implanted neurons.



(a)                                                    (b)
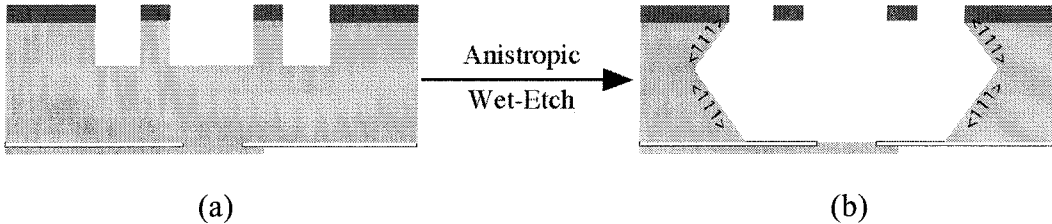
Figure 3-16: Schematics of the more likely scenario during grillwork patterning. In (a), the depth at which the plasma etch stops is not well-controlled and significant penetration of the lightly doped silicon results. (b) The anisotropic wet etch, which stops at <111> crystal planes, etches sideways as well as down creating a grossly deformed microcavity which is not conducive to neural processes outgrowth.

The cause of this unique and unexpected shape can be traced back to the step in which the RIE is used to etch the heavily doped epitaxial silicon to define the grillwork. This step has historically been one of the more demanding steps in the process as described previously in section 3.3.3. To be successful, first the grillwork must be patterned using photoresist and the stepper. Through experience, we have been able to

expose and develop the resist such that the resulting features, while not perfect, are still very good. The results from the RIE are a little less predictable.

After the resist is patterned, approximately 3 microns of the exposed heavily doped silicon must be etched using the RIE. In the ideal case, only the heavily doped silicon is etched and the underlying lightly doped silicon is not penetrated. Subsequent EDP etching results in a neurowell shaped as desired and with minimal overhang around its perimeter. In practice, stopping the RIE etch at the doped-undoped interface can never be achieved. A small amount of over etching must occur if the corners of the features are to be successfully defined as shown in figure 3-15.a. While still a significant barrier to the neurite growth cones, this amount of overhang should still allow neuronal outgrowth. This is evidenced by a small number of prototype neurochips producing regular and prolific networks. Figure 3-15.b shows the expected ideal geometry.

In too many cases, the etching of the large central hole in the grillwork has been significantly greater than that of the smaller corner holes. Whether this is caused by the difference in the feature sizes or poor photoresist patterning is uncertain. In either case, the result is that the etch at the center has extended a significant distance down into the underlying lightly doped silicon as shown in figure 3-16.a. EDP etching of such a vertical hole results in the hexagonal shaped wells shown in figure 3-16.b. Continuing with a fabrication process relying on such a critical processing step is not conducive to achieving high yields. The need to eliminate overhang from the neurowell and the desire to avoid any critical steps led to the development of the zero overhang neurowell design.

## 3.4    The Zero Overhang Neurowell

Biocompatibility is the first consideration when designing a tool to tap into a living neural network. Toxicity of the device is the mechanism that is usually considered when this topic is broached. Constructing the chips and probes from silicon, nitride, oxide and gold, materials known to be compatible with living tissue, avoids such rejection. Barriers that physically impede cell growth tend to be an incompatibility mechanism relatively unique to a given device. At present the only option available to overcome such physical barriers is to remove them.

### 3.4.1    Zero Overhang Neurowell Fabrication

To this end, a new process for the creation of the neurowell grillwork was devised. The main goal of the design is to guarantee that there will be no chance of overhang around the perimeter of the well. Based on the process used to fabricate the prototype neurowell variations (see section 3.3.3), this design uses nitride (or alternatively any readily patternable material) for the grillwork. Choosing nitride moves the steps for electrode formation to the end of the process, which is described in detail in appendix N7 and is shown schematically in figure 3-17. This is necessary since the electrode metals (Cr and Au) would be damaged by the high temperatures used in the nitride and oxide depositions of 850 °C and 1050 °C, respectively. The heavily doped epitaxial silicon layer now functions as an anisotropic etch-stop only. It is selectively removed from the 4 x 8 millimeter membrane formed by the backside cavity EDP etch.

(a)                              (b)                              (c)
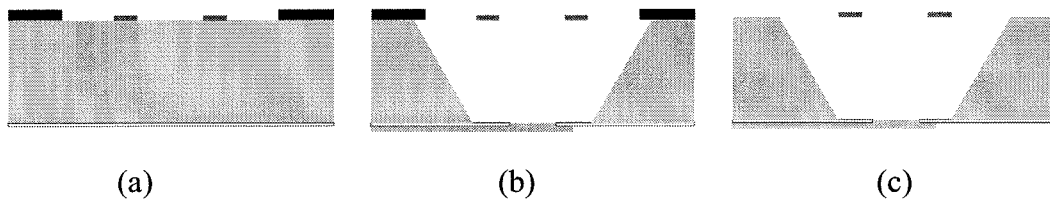
Figure 3-17: Neurowell cross sections for the final steps of the zero-overhang fabrication process. (a) The nitride is deposited and patterned into grillwork exposing silicon everywhere else. Thermal oxide is grown from this silicon and wet-etched to define the size of the top of the neurowell. (b) Gold is evaporated and patterned on the backside to form the electrode and the microcavity is formed by anisotropic wet-etch. (c) The oxide is stripped removing any overhangs that may be present creating a neurowell free of barriers to the exit of neural processes.

Formation of the neurowell begins with the deposition of 1 micron of LPCVD nitride. This material is patterned by an isotropic plasma etch that leaves behind only the bars of the neurowell grillwork; all field nitride is removed exposing the silicon beneath. Note that even excessive over etch is not problematic in this process at the same time that determining etch completion is greatly simplified. Thermal oxide is grown to seal all EDP etchable surfaces and is then selectively removed, by BHF etch, from the large central hole of the grillwork. Buffered HF only removes oxide and cannot penetrate into the underlying silicon. A subsequent EDP etch forms micro cavities with the expected truncated pyramid shape. Slight oxide overhangs around the perimeter of the neurowells may or may not be present at this point in the process (see figure 3-17.b). A final BHF etch, performed globally, easily removes any such undesirable oxide structures. The resulting geometry has nitride grillwork covering a properly shaped cavity that is guaranteed to have no overhang around its perimeter. Called a zero overhang neurowell, its cross section is pictured in figure 3-17.c.

Several fabrication runs proved that this process can repeatably produce neurowells with the expected geometry. Device yields in excess of 75% have been achieved with this design. The SEM photographs in figure 3-18 provide good views of a zero overhang well with excellent neural outgrowth from the cell body trapped within. The thin nitride grillwork, shaped like a "pointed" diamond with a central hole, sits on four silicon pedestals at the edges of the neurowell. Presence of the silicon pedestals indicates that the nitride was over etched during patterning. As expected, this did not adversely affect the final shape of the micro cavity. *In vitro* experimentation shows that these neurowells permit rapid and prolific neurite outgrowth and neural network formation.



(a)                                         (b)
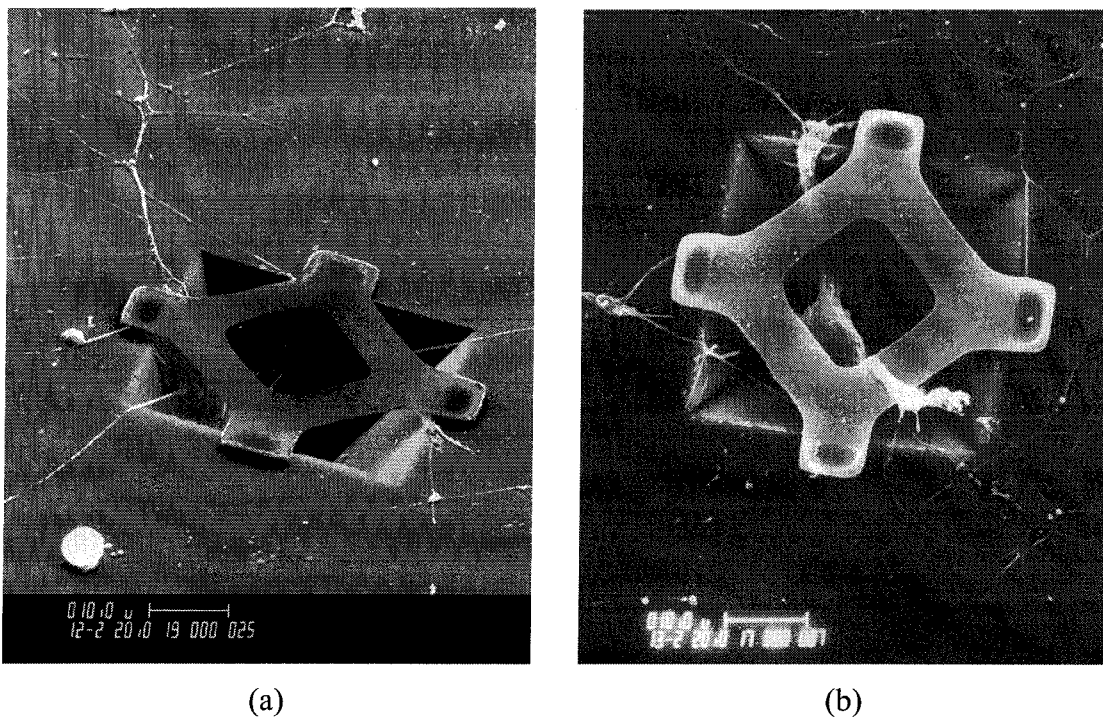
Figure 3-18: SEMs of a zero overhang neurowells loaded with SCG neurons. This culture has been fixed and dried for SEM work causing significant shrinkage of the axons and cell bodies and (a) has been computer colorized.

### 3.4.2   Neuron Cell Body Escape

The first fabrication run of this new neurowell design was initiated to verify that overhang is the main impediment to neurite outgrowth in the prototype wells.  The results from the first cell culture experiments bore out this hypothesis.  Shown in figure 3-19 is a picture of a hippocampal neural network growing vigorously in a zero overhang neurowell array.  While evidence that elimination of the overhang does permit rapid outgrowth of neural processes, the photograph also indicates two functional short comings with this neurowell design:  (1) poor sealing of the neuron over the electrode floor and (2) cell body escape.  The latter is a severe case of the former.
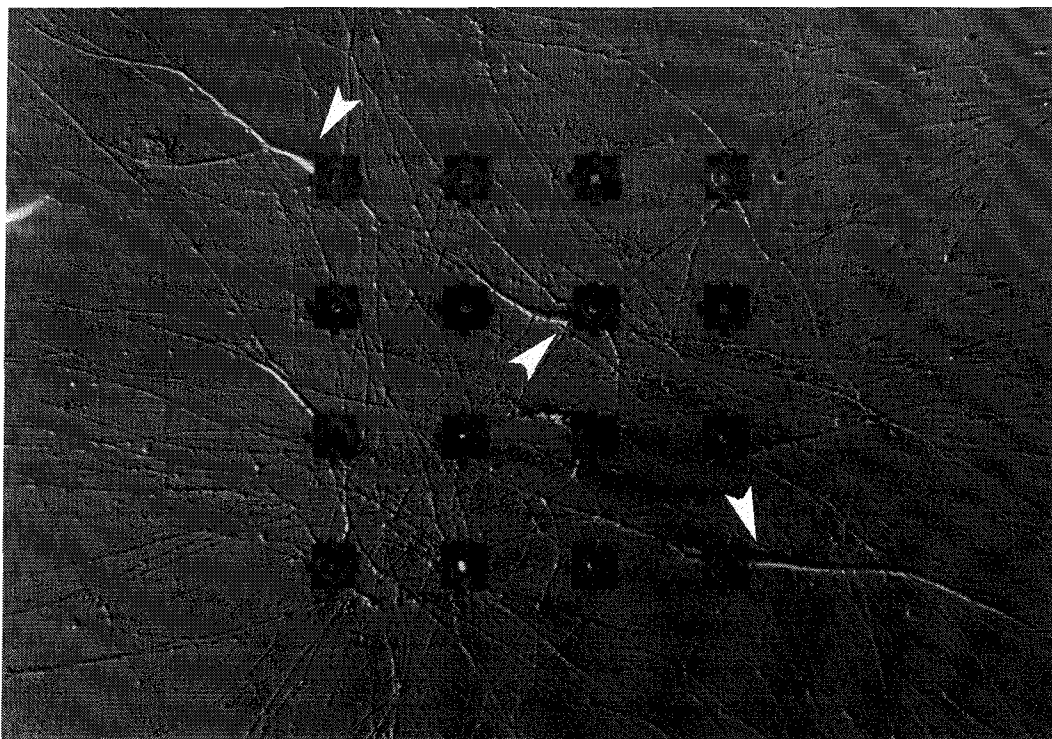


Figure 3-19:  A 4 x 4 neurowell array with growing SCG neuron culture.  The fine network of lines is neural process.  The large forms (arrows) are cell bodies that are escaping from their wells.

As neural processes mature, they tend to shorten and exert tension on their cell body. This is apparently a general phenomenon of CNS neurons and may be used by the brain to minimize wiring lengths [23]. Uneven tension pulls the neurons towards the "strongest" process. In the first two days of culture this is always the axon [43].

In the instances where the cell body remains in the micro cavity, the axonal tension drags the neuron up underneath the grillwork and away from the floor. Such an occurrence is seen in figure 3-18. The preparation of the sample in these images required that the neuron be dehydrated which causes the cell body to shrink to perhaps one half its wet size. Still, it is obvious that this position is not ideal if the cell body is to seal against the recording electrode in the floor. A degraded electrical SNR can be expected. While this shortcoming is undesirable, recording and stimulation should still be possible. It should be noted here that the proposed benefits of the dimpled bottom neurowell mentioned in section 3.3 are all nullified when neurons settle in such a position.

In more troubling cases, the tension exerted by the axon tows the neurons completely out of the neurowell. Just smaller than the triangular corner holes, the 10 to 20 micron diameter cell bodies can invariably squeeze out through the grillwork. Some neurons crawl out of their wells in a few days. Others appear to ooze out after a couple of weeks in culture. This scenario is obviously not conducive to any sort of long-term, stable recording or stimulation of the neural network.

### 3.4.3   Zero Overhang Neurowell Variations

To combat cell body escape, changes to the grillwork pattern were made. By fabricating perimeter holes that are much smaller than the diameter of a cell body, it was

hoped that neuron escape from the wells would be eliminated. No modification of the fabrication process is necessary to institute this change. Only simple revisions to two masks were made.

Four grillwork patterns were fabricated for *in vitro* testing. Shown in figure 3-20, each design sought to create perimeter holes no larger than 5 by 2 microns and as small as 2 by 0.5 microns. The patterns in figure 3-20.a and 3-20.b attempt to achieve this by patterning the nitride and the oxide with the exact feature size desired in the completed neurowells. To be successful, photoresist exposure and alignment need to be perfect.

Expecting such ideal results would be difficult to achieve, the patterns in figure 3-20.c and 3-20.d were also fabricated. These still require fine features to be etched in the nitride. However, the width of the perimeter holes is no longer set by an exposed pattern. The EDP access holes that determine the ultimate size of the neurowell micro cavities are smaller than necessary to create a top opening that is the desired 30 microns square.



(a)                    (b)                    (c)                    (d)
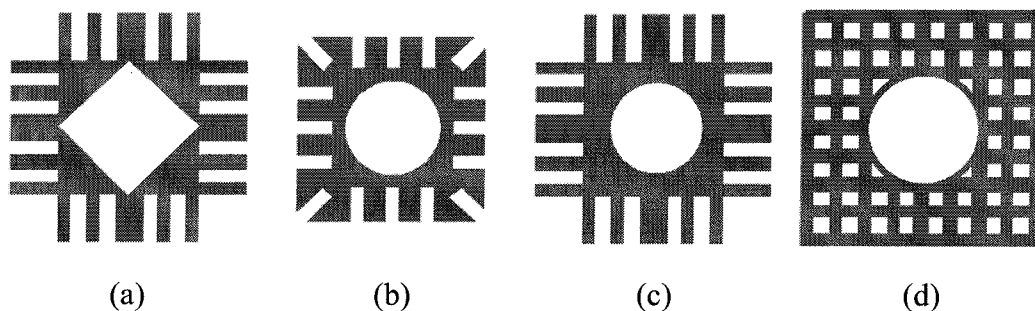
Figure 3-20: Grillwork patterns incorporated into the zero overhang neurowell design. The fine patterns were intended to result in very small holes that the neural processes could pass through but which would be an impassable barrier to the cell body.

Instead, the wells initially form slightly smaller than needed to open up exit holes around their perimeter. Over etching in EDP causes the sidewalls to slowly expand until they reach the fine openings at the patterned nitride edges. The etch rate of the sidewalls is on the order of 1 to 2 microns per hour. This is slow enough that the width of the perimeter hole openings can be kept to as little as 0.5 microns. A beneficial side effect of this approach is that the micro cavity is self-aligned to the central hole in the grillwork. Perfect alignment between the nitride and oxide patterning steps is not necessary.

With all four zero overhang neurowell variations fabricated in an abundant number of neurochips, investigations into the efficacy of the different designs were initiated. While informative, the results of this work were disheartening. None of the designs proved to effectively contain even a slight majority of the neurons implanted in them. Neurons have been seen to pull themselves through holes as small as 1 by 3 microns. This is somewhat surprising given that some relatively rigid structures within the cell body are larger than half a micron. The three photographs in figure 3-21 show a



(a)                              (b)                              (c)
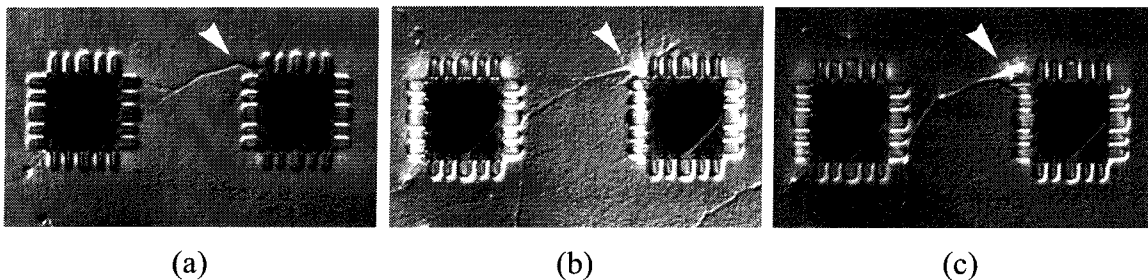
Figure 3-21: Time-lapse video frames of outgrowth and escape of a hippocampal neuron. The dimensions of the corner hole in the grillwork are approximately 1.0 x 3.0 microns. (a) outgrowth after 12 hours, (b) after 24 hours, the neuron is beginning to escape, and (3) after 3 days the neuron has escaped.

hippocampal neuron escaping from its well through a micron size hole over a 3-day period.

To see how such a large body is able to pass through such a small orifice, the physical makeup of a neuron needs to be understood. A neural cell is essentially a very thin "bag" filled with saline solution. Little damage occurs when opposite walls of the neuron are forced together at a localized point. The displaced volume simply flows and slightly inflates the uncompressed areas of the cell. Since there are no rigidly connected internal organs nor are there arteries or veins that could be constricted, even squeezing a portion of the cell down to a very small cross section does not seem to damage the neuron. Such capabilities are seen by some species of animals. Octopus are capable of squeezing through openings many times smaller than their normal size. Their inflexible beaks seem to be the only limiting factor to how small a hole they can successfully navigate. The schematic in figure 3-22.a depicts the ideal outgrowth situation while figure 3-22.b shows how the neurons seem to behave when cultured in the wells.



(a)                                            (b)
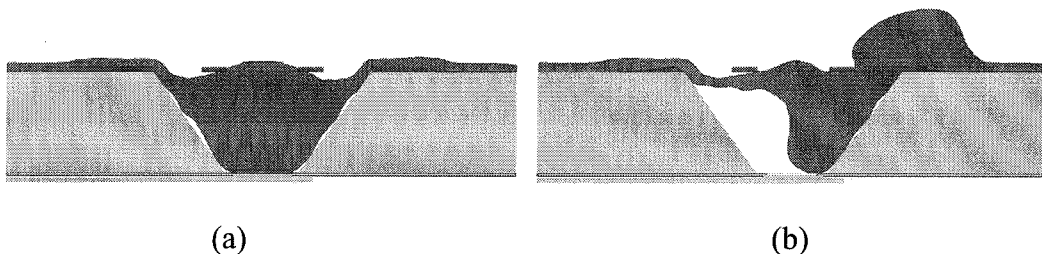
Figure 3-22: Neurons are capable of squeezing their cell bodies through very small openings. While the neurowell is designed for neurons that behave as in (a), the occurrence shown in (b) is more likely and using small holes in a thin membrane for containment is ineffective.

## 3.5    The Canopy Neurowell

It seems ironic that in solving the problem of minimal outgrowth of very fine neural processes, the problem of keeping very large cell body from escaping became the critical challenge. Many approaches, both mechanical and biological, were considered as possible remedies for this dilemma. Some, such as sealing over the wells with neurite penetrable scar tissue, were tried with varying degrees of success. The solution finally settled upon, support for which was found in a single paragraph of a single paper [68], was to replace the perimeter micro holes with long, narrow micro tunnels. Torre and Steward showed that pores approximately 10-microns long and less than 3-microns in diameter consistently allow hippocampal neurites to pass freely while denying access to the cell bodies. Such dimensions are readily produced by standard micromachining techniques. Fortuitously, a simple rearrangement of the processing steps used to fabricate the zero overhang wells and a few minor mask changes were all that was needed to



(a)                          (b)                          (c)
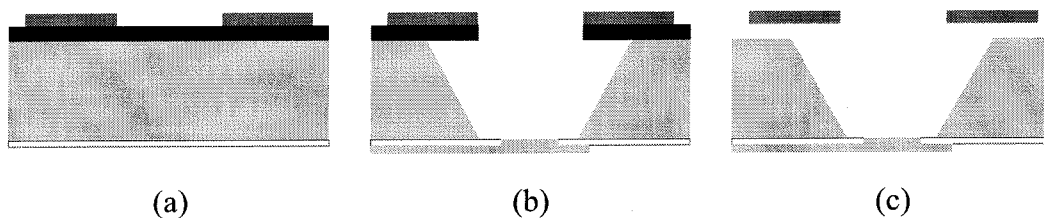
Figure 3-23: Neurowell cross sections for the final steps of the canopy neurowell fabrication process. (a) Low temperature oxide is deposited as a sacrificial layer and is patterned to provide anchor points to the underlying silicon (not shown). LPCVD nitride is then deposited over the LTO and patterned into the shape of the grillwork. (b) On the backside of the membrane, gold is evaporated and patterned to form the electrode. Returning to the well side, the oxide in the center of grillwork is selectively etched, and the microcavity is formed by anisotropic wet-etch. In the final step (c) The oxide is stripped, clearing it from beneath the nitride, removing any overhang that might be present, and opening up the microtunnels.

realize the micro tunnels. The unique shape of the grillwork used to cover the micro cavities in this design led to the structures being named canopy neurowells.

### 3.5.1 Canopy Neurowell Fabrication

Like the zero overhang neurowells, the canopy neurowells use nitride for their grillwork and oxide as a sacrificial material. However, a fast etching, low temperature oxide (LTO) is used instead of the more dense wet oxide of the previous design. Summarized in figure 3-23.(a-c), the detailed process can be found in appendix N8. In short, the LTO is deposited first and patterned by BHF to form anchor holes that expose the underlying silicon. Nitride is then laid down over the patterned LTO and etched. All field nitride is removed leaving behind 50 to 90 micron diameter canopies with 20-micron diameter central holes (figure 3-23.a). A non-critically aligned photoresist patterning allows BHF to selectively remove the LTO from the central holes of the wells and expose the underlying silicon. An EDP etch forms the micro cavity that self-aligns to the center of the canopy (figure 3-23.b). A 5 to 10 minute HF etch strips all LTO from the cavity side of the wafer, including from the tunnels beneath the nitride canopy. The resulting neurowell has no unwanted perimeter overhang yet presents only the entrances to micro tunnels as possible avenues of escape for growing neurites. Figure 3-24 is an SEM of a cross-sectioned canopy neurowell. As desired the micro cavity has a truncated pyramid shape with no overhang around the top perimeter. The nitride canopy sits over the well on anchors connected to the silicon membrane. The anchors also act to form the

sidewalls of the micro tunnels that, in this case, are about 30 microns long, 1 micron high

and 5 microns wide. In the center of the floor of the well, the gold electrode can be seen.

In a sense, the canopy design integrates narrow passages in conjunction with

extreme grillwork overhang to achieve the desired function. The schematic in figure 3-25

shows the expected outgrowth in such a well. The neurites grow up the sidewalls and are

forced to travel down the length of one of the radial tunnels. On reaching the end of the

passage, the neurite is able to move freely and seek out neighboring neurons. As the

process continues to grow, the short segment inside the micro tunnel becomes pressed
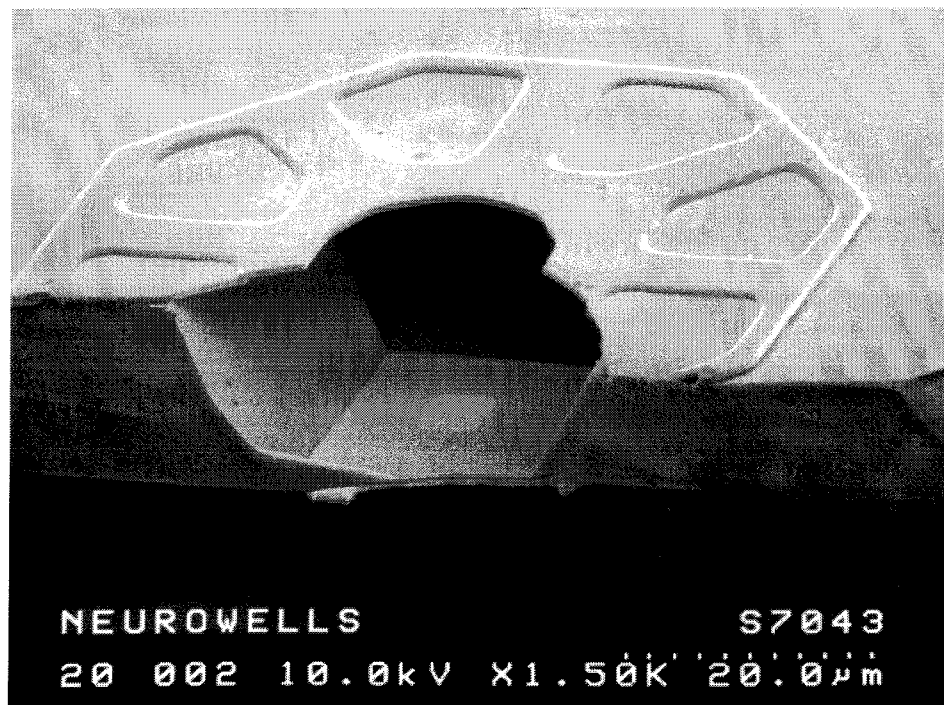


Figure 3-24: Scanning electron micrograph of a cross-sectioned canopy neurowell. The straight, raised bars in the octagonal grillwork cover are the micro-tunnels through which neural processes can grow but are impassable by the cell body. The floor is a suspended nitride film in the center of which is an exposed gold electrode.

between and, as a result, rigidly attached to the floor and ceiling. The segment now acts as a mechanical buffer between the neuron and the tugging neurite. Friction down the length of the micro tunnel prohibits passage of the large cell body.

To function properly and still be biocompatible, three criteria must be satisfied. First, the path through which the processes grow must be constrictive enough to prevent cell escape. Second, this path must not be too small or else the growth cones will not be able to pass through it. Third, as the neurites mature and thicken, they must not be so constricted that they cannot survive. In meeting these requirements, tunnel height, width and length can be varied. Tunnels with the following dimensions have been fabricated for neurite outgrowth and cell body containment testing: widths of 2, 4 and 10 microns; heights of 0.2, 0.3, 0.5 and 1.0 microns; lengths of 15 and 30 microns.

### 3.5.2   Canopy Neurowell Experimental Validation

*In vitro* neurophysiological experiments using neurochips containing 4 x 4 arrays of the canopy neurowells validated that this design is mechanically functional and
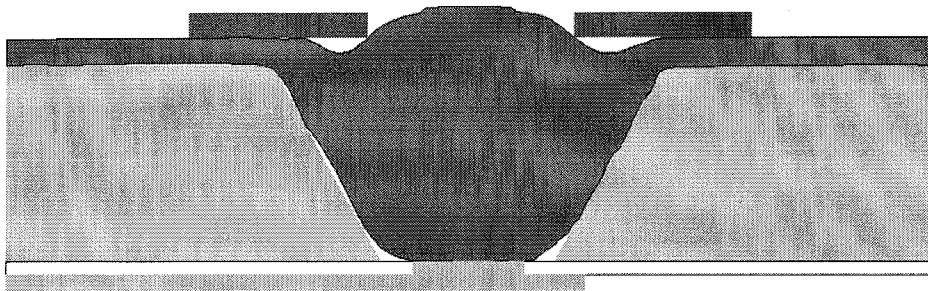


Figure 3-25: Idealized view of a neuron cultured in the canopy and trapping the cell body in the microcavity against the electrode as it extends its neurites through micro-tunnels formed in the grillwork.

biologically compatible. Hippocampal neurons harvested from embryonic rat fetus grow rapidly and prodigiously from the wells, through the micro tunnels and out into their surroundings. Figure 3-26 shows an 8-day-old culture. Processes extending out of 12 of the 16 wells can be clearly seen. In the field between neighboring octagonal canopies, the web-like interlacing of neural processes is readily visible.

The well design was optimized for fetal rat hippocampal neurons [46]. As seen in the earlier neurowell designs, the growth cones of hippocampal neurons appear to be unable to cross sharp acute angles. As they grow up the walls of the well, they normally pass into the tunnels and only rarely grow onto the underside of the canopy and out
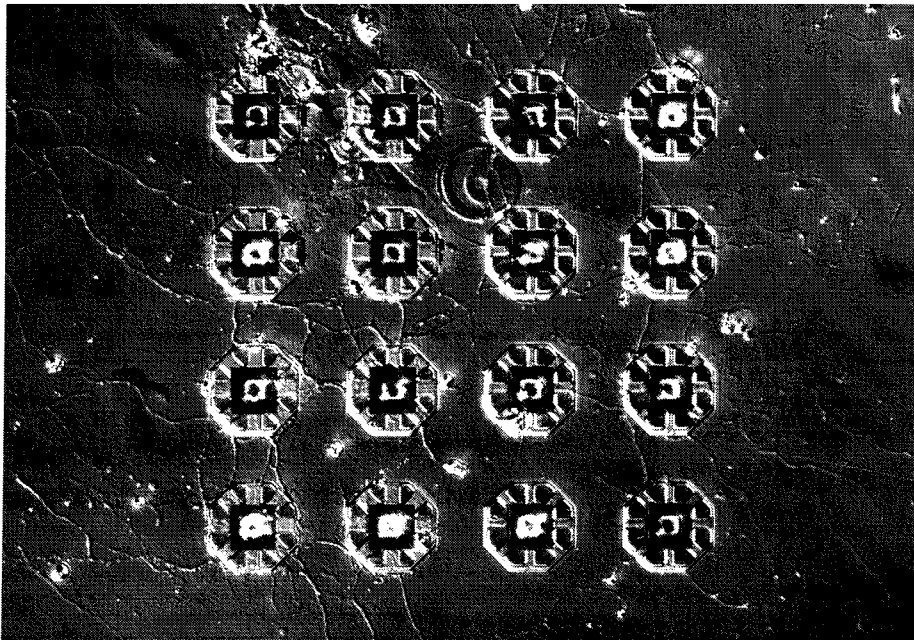


Figure 3-26:  Differential interference contrast micrograph of a hippocampal culture in a canopy neurochip. Several neurites emerge from most of the wells, forming a dense network. The patch of cells at the upper left corner is a small island of astrocytes. All processes visible come from neurons in the wells. (The circular pattern between the first two rows of wells is a lithography defect.)

through the central hole.  Tension on the cell body from maturing processes tends to pull the cell body towards the edges of the wells, and the cell migrates in the direction of the largest process.  Tunnel cross sections ranging from 0.2 micron high by 2 micron wide to 1 micron high by 10 micron wide have been investigated.  No significant differences between these designs, in terms of neuron survival or number of processes growing, are found.  Three of 105 cells surviving at least 6 days in neurowells with 10-micron wide, 0.5-micron high tunnels, escaped during the first three days in culture.  No additional neurons escaped from these wells during the remaining life of the network.  No escapes have been detected through the narrower tunnels (N = 104).

Neurons from the neonatal rat superior cervical ganglion have also been investigated with the canopy neurowells.  For the first week in culture, SCG neurons survived and remained trapped in the wells.  As they matured, however, the cell bodies tended to fill the wells.  Processes then began to grow out of the center holes, and the tension from these processes allowed the cell bodies to escape the wells.  Thus, a single well design is unlikely to be optimal for all cell types.  Testing of the existing well design must be conducted with each target cell type.  Slight redesigns may be necessary based upon the resulting neuron growth, lack thereof, or escape.  Assuming escape through the central hole in the grillwork is the main difficulty when culturing different cell types, an additional step in the fabrication process can be introduced.  This will provide an integrated cover for each well ensuring the only exit route from a well is the microtunnels.

Neurons implanted into canopy wells are now successfully cultured on a routine basis.   With adequate mechanical functionality of the neurowell achieved, fully functional arrays of this building block were produced.   With these devices, stimulation and recording experiments were pursued in order to demonstrate the full capability of such interfaces.

# CHAPTER

# 4

# NEUROWELL CHARACTERIZATION AND PRACTICAL CONSIDERATIONS

Proper analysis and device preparation must be performed in order to successfully use the neurowell structure as a neural recording and stimulation tool. Issues that must be addressed range from basic electrical characterization of the wells to pre-conditioning of the electrodes to proper mounting and/or packaging of the silicon devices. These topics are covered in the following sections. During the course of this work, several unexpected challenges have been tackled. All have been overcome with a combination of clever engineering, proper material selection and basic physical modeling. The final result is a microstructure that is biologically compatible and electrically functional. Presently, neurophysiological experiments are continuing with cultured neural networks.

## 4.1    Neurowell Electrical Characterizations

The electrical nature of both the neurowell and the implanted neurons directly affects the level of the signals that can theoretically be recorded and realistically be expected from these neural interfaces.  Analysis of the geometry and resulting electrical resistances of the neurowell is conducted first.  This leads to an equivalent circuit model for the structure.  The electrophysiological properties of the neurons to be implanted are then examined.  Realistic values of membrane capacitance and external electrical currents and voltages are determined.  Finally, this information is fed back into the circuit model for the neurowell and a series of conditioning steps can be devised to enhance the recording and stimulation capabilities of the electrodes.

### 4.1.1    Neurowell Equivalent Electrical Circuit

To understand the operation of the neurowell as a recording and stimulating tool, the physical device must be distilled down into an equivalent electrical circuit.  The schematic in figure 4-1 shows the relevant resistances formed in and from the neurowell
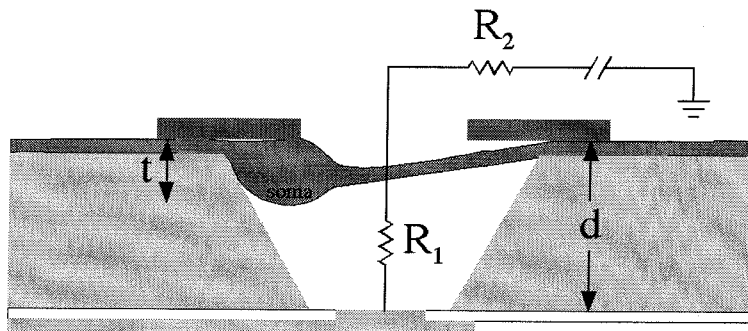


Figure 4-1:  Equivalent electrical circuit model for the neurowell immersed in a conductive saline solution.

when the structure is immersed in saline solution.

The path through the saline from the top of the neurowell to a platinum ground wire at a great distance is deemed the spreading resistance. It has been shown by [51] that this value is given by:

$$R_{spread} = \frac{\rho}{4r}$$
eqn. 4.1

This equation is an exact calculation for the spreading resistance from a circular disk, to infinity, on a planar insulating surface. For the typical neurowell, and the canopy version specifically, the relevant values and resulting resistance is:

$$r = 10 \times 10^{-6} \, m \qquad \rho = 0.70 \, \Omega\text{-}m \qquad => R_{well} = 17.5 \, k\Omega$$

This resistance closely agrees with calibration measurements made with test structures immersed in the culture medium used in actual *in vitro* experiments.

The resistance from the electrode at the bottom of a neurowell to the grillwork cover can be derived as follows:

$$R_{well} = \int_0^h \frac{\rho}{A(x)} dx$$
eqn. 4.2

At the interval dx:

$$A(x) = \left( a + \frac{b-a}{h} x \right)^2$$
eqn. 4.3

which results in:

$$R_{well} = \frac{\rho h}{ab}$$

<div align="right">eqn. 4.4</div>

where $\rho$ is the resistivity of the culture solution and a, b, and h are the physical dimensions of the microcavity which are shown in figure 4-2. As designed, the top of the microcavity is 30 microns square and the silicon is 16 microns thick. In practice the well openings are expected to be slightly larger, perhaps to as large as 35 microns square. This is due to two factors: (1) the anisotropic EDP etch that forms the microcavities does slowly etch the sidewalls as well as the floor due to non-ideal etch-plane selectivity and (2) achieving sharp definition of features at the bottom of a 500 micron deep cavity on a thin, slightly warped membrane is difficult (see appendix N2). In both cases, the well
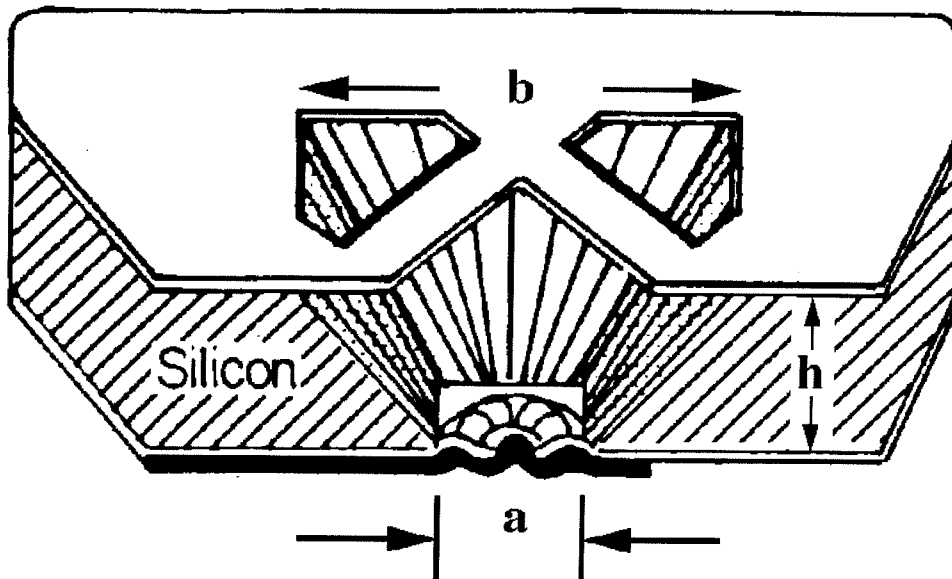


Figure 4-2: Schematic cross section of a neurowell detailing the salient dimensions used in equations 4.2 through 4.4.

opening is enlarged.   For factor (1), a reasonable (100):(111) selectivity of 30:1 and

intentional over etch assures a sideways etch of approximately 1 microns at each wall,

increasing the total length of a side by 2 microns.   The minimum expected well size is

then 32 microns square.   For factor (2), the actual increase of the length of a side is from

2 to 4 microns corresponding to a 1 to 2 micron blurring of each well side.   The results

are well openings as large as 36 microns square.   Choosing a middle ground, the resulting

parameters for such wells are:

$$a = 10.8 \pm 2.0 \text{ microns} \qquad h = 16.0 \text{ microns}$$

$$b = 34.0 \pm 2.0 \text{ microns} \qquad \rho = 70 \ \Omega\text{-cm}$$

$$\Rightarrow R_{well} = 30.6 \pm 7.8 \text{ k}\Omega$$

Resistances on the order of several tens of thousands of ohms are confirmed by

calibration measurements made with an electrode maneuvered over the top of a well

when immersed in culture medium.   Dimensional measurements of the fabricated well

shown in the SEM image in figure 3-24 show that the top of this microcavity is

approximately 34 microns square.   This is very reasonable for the process being used.   It

should be noted that since the precise size of the wells is not critical to their function, no

special effort was taken to control final dimensions.

The total resistance of the system shown in figure 4-1 is then simply the sum of

the well resistance and the spreading resistance:

$$R_{system} = R_{well} + R_{spread} = \frac{\rho h}{ab} + \frac{\rho}{4r} = 48.1 \pm 7.8 \text{ k}\Omega \qquad \text{eqn. 4.5}$$

In fabricated neurochips with canopy neurowell arrays, the real part of the 1 kHz electrode impedance is measured as $48 \pm 8$ k$\Omega$ (N = 16). Thus, the calculated resistance almost perfectly agrees with the measured values.

### 4.1.2   Electrophysiology Theoretical Issues

Reliably causing a neuron to fire an action potential requires raising part of the trans-membrane potential from its resting level by $\Delta V_t \approx 30$ mV for a time sufficiently long to open voltage-activated sodium channels. The time required is approximately 200 μs at room temperature [34]. Additionally, extracellular electrodes must supply relatively large currents for stimulation as the saline bath has low resistivity. In doing this, care must be taken to avoid the irreversible electrochemistry that occurs when the voltage drop across the capacitative bilayer of the saline next to the electrode exceeds 1.2V [60]. At this point hydrolysis takes place and produces atomic oxygen that is extremely toxic to nearby hippocampal neurons.

The large difference between the impedance of the interior of a cell and its membrane walls further complicates stimulation. The resistance of the saline within the cell body from the bottom membrane to the top is only approximately $R_{CB} \approx 50$ k$\Omega$. This is negligible in comparison to the very large impedance of the cell wall. Measurements of the membrane properties of hippocampal neurons after seven days in culture, in this

research and others [17, 73], show that the cells have a capacitance of $C_m \approx 80$ pF (this value, measured at the soma, includes the cell body and the dendritic tree). At 1 kHz this corresponds to a resistive impedance of approximately $R_{cw} \approx 2$ M$\Omega$. In response to an externally applied electric field, the interior of the cell body is an isopotential that follows the average exterior potential with a $R_{CB}C_m \approx 4$ $\mu$sec time constant. The potential drops due to a vertical external electric field are concentrated in the membrane at the top and bottom of the cell body. A current sufficient to cause a voltage drop of $2\Delta V_t \approx 60$ mV across the $t \cdot 5$ micron thickness of the cell body is required for stimulation, estimated to be:

$$I_{min} = 2\Delta V_t \left( \frac{\pi r^2}{\rho t} \right) = 5.4 \mu A \qquad \text{eqn. 4.6}$$

To supply 5.4 $\mu$A for 200 $\mu$s without exceeding 1 V across the electrode, the equation:

$$I = C\frac{dV}{dt} \qquad \text{eqn. 4.7}$$

gives the calculated electrode capacitance necessary is at least 1080 pF.

Regardless of the direction of the applied current for a monopolar stimulus, part of the cell membrane is hyperpolarized while a roughly equal area is depolarized toward threshold. Since only depolarization is significant in causing a cell to fire, either polarity should be equally potent. However, to minimize the stimulus artifact, we normally use bipolar stimuli (200 $\mu$s per phase). Voltage-gated sodium channels can open and close on

a 200 µs time scale, so that a patch of membrane, which is first depolarized, will have its action potential quenched by the subsequent hyperpolarizing pulse. An action potential starting in a patch of membrane that is first hyperpolarized, then depolarized, will instead be free to expand. In a geometrically symmetric system, one side of the cell will always be hyperpolarized first, regardless of the polarity of the first half of the bipolar stimulus, and therefore an action potential should result regardless of the polarity of the first half of the stimulus.

Contrary to the simple analysis discussed above, the response to a stimulus applied through the neurochip electrode is not symmetric with respect to current polarity (see section 5.5.2). That analysis assumes that the electric field across the cell body is uniform, which is almost certainly not true. If a small patch of membrane experiences a much larger membrane potential change during a stimulus, then it will initiate the action potential that then spreads across the cell. In all cells tested, bipolar stimuli with the negative phase first always have a lower current threshold than positive-leading stimuli. We conclude that the spikes are initiated in the top region of the cell body. This is consistent with the geometry of the well, since the electric field will be concentrated at the top of the well where it passes through the narrow central hole of the canopy.

## 4.2    Neurowell Electrode Pre-Conditioning

As fabricated, the surface area of the gold electrodes at the bottom of the neurowells is too small to effectively stimulate and record from neurons. A neurowell

relies on capacitive coupling from its electrode, through a short distance of saline solution, and across the cell membrane to transmit and receive small electrical signals. A bare-gold electrode placed into a grounded saline solution typically has on the order of 0.2 pF capacitance per square micron of exposed surface area [39, 61, 71]. This corresponds to less than 20 pF for a 10-micron diameter pad opened in the floor of a well. When compared to an estimated 150 pF of parasitic capacitances in the monitoring circuitry, the bare capacitance of the electrodes quickly becomes negligible. Treatment to enhance the sensing element must be employed.

### 4.2.1   Electrode Impedances

The electrical properties of the interface between a saline solution and a noble metal are an extremely complicated issue. In the linear regime (signal sizes that are too small for electrochemistry to occur), the impedance is dominated by diffusional re-arrangement of ions [61]. This impedance is approximated as a frequency-dependent capacitance, $C \approx f^a$ with a $\approx 0.5$, in parallel with a very large resistance. For stimulation and recording from neurons, it is convenient to consider the impedance as a constant in the frequency range of interest, namely 1 kHz (the time scale on which action potentials occur). Electrodes at 1 kHz typically have 0.2 pF capacitance per square micron of exposed electrode surface [61]. Electrode capacitance values quoted in this work are always determined at 1 kHz. The active area of an 8-micron diameter neurochip electrode is 50 $\mu m^2$, for a theoretical capacitance of about 10 pF. Measured bare

capacitances are 21±8 pF (N = 160, all uncertainties in this manuscript are quoted in mean ±S.D.). The larger measured value is attributed to enlargement of the active electrode area during the final HF etch, in which part of the nitride insulation covering the electrodes is removed.

For recording, the electrode capacitance must exceed the parasitic capacitances of the chip wiring, cables and pre-amplifier (approximately 150 pF) to avoid significant signal loss. For stimulation, however, we estimate that a capacitance of > 1000 pF is necessary (see section 4.1.2).

## 4.2.2  Electrode Platinization

To decrease their impedance to the bath, the electrodes are electroplated with platinum black. The platinizing solution contains 1% chloroplatinic acid (Sigma C-3044), 0.0025% hydrochloric acid, and 0.01% lead acetate in water. Electrodes are initially plated with 5 V through a 20 M$\Omega$ resistor for 10 seconds (300 mA/cm$^2$ current density). The platinum black appears to grow into a spongy, highly porous metallic layer that greatly increases the effective surface area of the electrodes.

The capacitance of electrodes has been reported to be increased by a factor of 10-100 by platinization [15, 39, 61, 71]. In our system, we typically see an increase of a factor of 170 (to 3600 ± 1000 pF) after a single platinization at 300 mA/cm$^2$, but this capacitance increase quickly degrades within a few hours to a factor of 30 (to 600 ± 200 pF). Work to improve this has resulted in a process that attains nearly a factor of 1000 permanent increase in capacitance. The electrodes are platinized daily for 5 days.

Between each electroplating, the chips are soaked at room temperature in 30% hydrogen

peroxide for 30 minutes then allowed to set in water overnight. The final thickness of the

platinum black is from 2 to 4 microns. The resulting 1 kHz effective capacitance

stabilizes at about 18000 ± 6000 pF. Apparently, the mechanical action of oxygen

bubbles formed when the platinum catalyzes the peroxide causes the most fragile

platinum spines to break off. Repeated platinizations then build up a stronger, high-

surface-area framework. This is similar to the effect seen by Marrese [47], in which

electrodes platinized in an ultrasonic bath achieved a higher, more stable capacitance than

control electrodes.

During platinizing, the rate of increase in electrode capacitance is initially quite

large and then slows as an asymptotic value is reached. A typical impedance vs.

platinization time curve is shown in figure 4-3.a. Continued platinizing over the 5-day
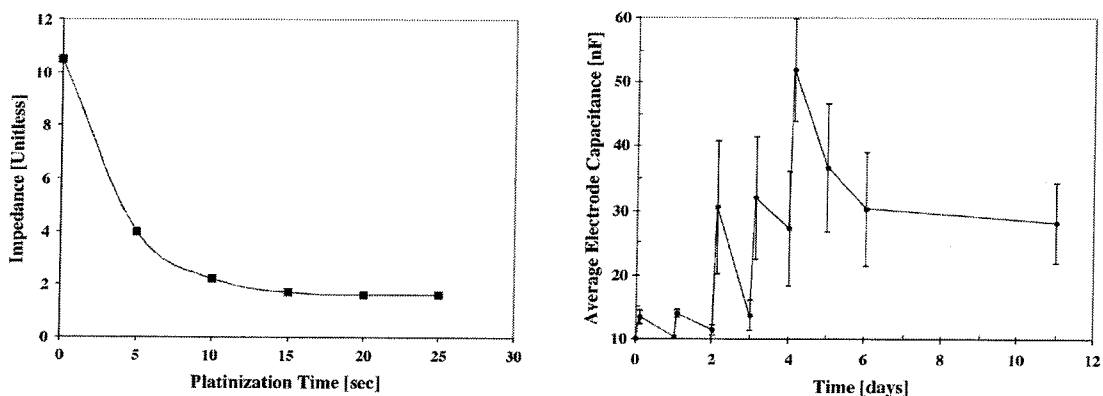


Figure 4-3: (a) Typical decrease in electrode-to-solution impedance realized as platinizing progresses. (b) Average electrode capacitance at 1 kHz as the 5-day platinization protocol proceeds. A higher value of capacitance is measured immediately after each platinization than is found the following day. Error bars indicate one standard deviation in spread of values of individual electrodes.

course described above continues to increase the realized electrode capacitance. Figure 4-3.b shows the average 1 kHz effective electrode capacitance of 16 neurochip electrodes measured before and after daily platinization over 5 days. The daily fall in capacitance became smaller over the course of this treatment, while the remnant capacitance continued to rise. At the end of the treatment, the capacitance fell to a stable level of 18000 ± 6000 pF. This represents a factor of 1000 increase in electrode surface area, far greater than any previously reported value.

Similar to previous reports [65], we find that the effective electrode capacitance decreases by approximately 50% after incubation with tissue culture medium. After 2 weeks in culture, electrode capacitances average 4000 ± 1000 pF (averaged over 75 electrodes on five neurochips). This is still large enough for safe stimulation (see section 4.1.2). After rinsing away the medium and cleaning with 5.25% bleach in water, the capacitance is fully restored to its value before adding medium, so it is likely that this capacitance reduction is due to adsorption of proteins, sugars, or lipids.

### 4.2.3   Cell Growth on Platinum Black

As noted above, the reason that depositing platinum black onto gold electrodes increases the capacitance is that it forms a rough, spongy and highly-porous surface. To determine if cells will grow normally on such a surface, 5 mm circles of platinum black were electroplated onto a glass plate covered with a thin, evaporated gold film. The capacitance of these circles to the bath increased by a factor of 20-50 after electroplating.

This decreased to a factor of 5-10 after several days.

After coating the surface of the gold/platinum plate with poly-L-lysine, newly
dissociated fetal hippocampal pyramidal cells stained with DiI were cultured on the
slides. Figure 4-4 shows fluorescence photomicrographs of this chip. The left half is on
gold and the right half is on platinum black. The bright spots are crystals of DiI that did
not dissolve and many dead cells are apparent (DiI is very toxic). Several live cells with
processes are visible. Identically stained cells plated onto standard glass coated with
poly-L-lysine showed similar amounts of DiI crystals, dead cells, and cell growth. There
are no apparent quantitative or qualitative differences between cells growing on platinum
black as compared to cells growing on gold.
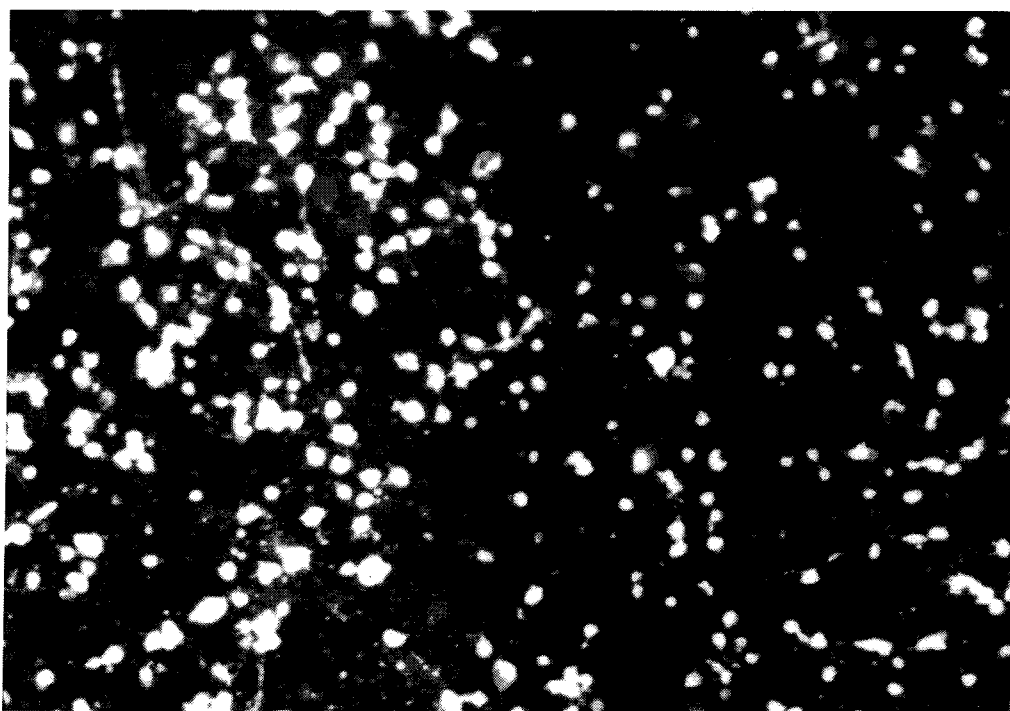


Figure 4-4:  Micrograph of fluorescing neurons grown on evaporated gold (left
half) and electroplated platinum black (right half) surfaces.

## 4.3    External Electronics

For electrical measurements, high source impedance signals from the electrodes are transferred through a 20 cm cable to an 11X non-inverting pre-amplifier [58], then to a 2X non-inverting buffer amplifier with a three-pole low pass filter (3 dB point at 5 kHz). The signals are then passed to two 8-channel 16 bit A/D converters, with 8X amplifiers and $\pm 10$ V range (National Instruments) in a Macintosh II personal computer. The net gain of the system is 1.8 $\mu$V/bit. The signals can be viewed in real time, then optionally stored to disk for subsequent analysis. Typically, data is saved at a low rate (2 kHz) to facilitate long-time recordings. Digitization is triggered using the 60 Hz line, so that AC pickup can be stored and digitally subtracted. The magnitude of the removed 60 Hz hum is on the order of 100 $\mu$V peak-to-peak. Software built in the LabVIEW environment (National Instruments) controls the data acquisition. Stimulation through well electrodes is controlled through a digital I/O card (National Instruments) in the Mac II, which sends amplitude information to a set of D/A converters on board the buffer amplifier. Stimulation timing is controlled through high-precision timers on the A/D converter cards. Biphasic pulses 0-10 msec long and 0-20 $\mu$A in amplitude can be fed to the electrodes through 500 k$\Omega$ resistors at the inputs to the pre-amplifiers.

Noise in the system is the main factor limiting the detection of low level signals from neurons implanted in the neurowells. As noted above, the R = 48 k$\Omega$ resistive path to ground dominates the impedance of the electrodes. The amplifiers have a bandwidth of B = 5 kHz. At room temperature, T = 293 Kelvin, the associated Johnson noise is [38]:

$$V_J = \sqrt{4k_B RBT} \approx 1.97 \ \mu V \ RMS \qquad\qquad \text{eqn. 4.8}$$

where $k_B$ = Boltzmann's constant = 1.38 x $10^{-23}$ J/K.  Using manufacturer specifications, an additional noise component from the pre-amplifier circuitry, attached directly to the neurowell electrodes, is predicted to be about 1.4 $\mu V$.  Summing these noise sources in quadrature yields a theoretical noise level of 2.4 $\mu V$.  The experimentally measured noise level is 2.5 $\mu V$ RMS or 1.4 A/D bits.  The resulting signal-to-noise ratio (SNR) for detected action potentials is from 70 to 90.  Neurowells should be able to detect subthreshold events with an expected SNR of 1 to 10.  Future experiments with cultured networks *in vitro* will be used to confirm this capability.

## 4.4   Neurochip Mounting for Electrophysiology

Neuron electrophysiology requires that the neurochip be packaged so that it can be fully immersed culture medium.  Additionally, all electrical connections must be protected from or able to resist constant exposure to the harsh environment of a $CO_2$ incubator.  Standard wiring connections using materials such as solder and tinned copper easily corrode in the 5% $CO_2$, 100% humidity, and 37 °C culturing atmosphere.  In developing a robust experimental assembly, several mounting procedures were explored.

The standard wire-lead bonding technique (shown in figure 4-5.a) used to electrically connect to IC chips to their packages can not be used when mounting a neurochip.  To permit access to the well array, the bond pads of the neurochip must face the surface of the package in which it is being mounted (see figure 4-5.b).  This

orientation makes it impossible for a lead bonder to attach a wire to the chip and then to

the package. Consequently, a new mounting technique had to be developed.

### 4.4.1    Printed Circuit Board Neurochip

The first bonding method implemented uses a conductive silver epoxy to attach

wire "legs" to the neurochip which are, in turn, epoxied to the bond pads of a printed

circuit board (PCB). Once the chip is in place, a plastic petri dish with a 1.5-cm diameter

hole in its bottom is permanently affixed to the PCB with 5 Minute™ epoxy. All non-

micromachined surfaces that will be exposed to culture medium during cell growth are

coated with Dow Corning Silastic MDX-4210 silicon elastomer (commonly known as

sylgard) to ensure the electrical connections are covered and the culture region is non-



(a)



(b)
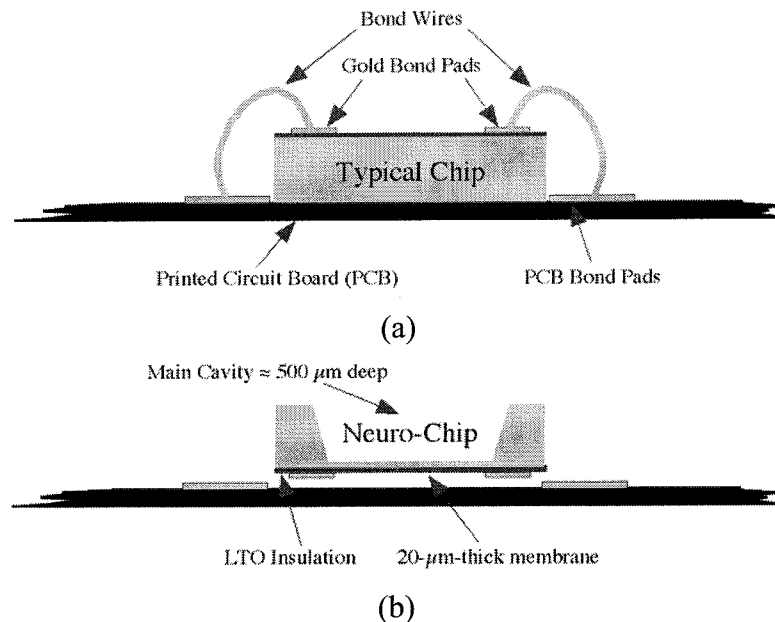
Figure 4-5:  Schematics showing (a) the standard wire-bonding technique used by
the IC industry. and (b) the required orientation of the neurochip. With the bond
pads of the neurochip facing the substrate, the technique in (a) cannot be used.

toxic. Figure 4-6 shows the ideal results of such an assembly.

Mounting a chip in this manner results in an air cavity between the underside of the chip and the PCB. Theoretically, this should be fine; in practice two problems arise. First, the thin silicon membrane of the chip is unsupported so all future work must be done very carefully to avoid breaking the fragile membrane. Second, while the air space should be a sealed environment, it is possible for liquid to find its way inside, through a pinhole or small crack. This shorts out all the bond pads rendering the chip useless.

As described above, the PCB mounting process has a more debilitating flaw. The silver epoxy used to bond wire "legs" to the neurochip is relatively fluid and is easily pulled along the wires by surface tension. With care, the epoxy will not bleed from one bond pad to another. It is much more difficult to keep it from coming in contact with the uninsulated edge (exposed as a result of wafer dicing) of the chip (see figure 4-7.a). Since the resistance of the silicon substrate is relatively low, on the order of a hundred ohms or less, the unwanted epoxy-to-silicon contact creates a parasitic path to ground that makes recording and stimulation with a neurowell impossible.
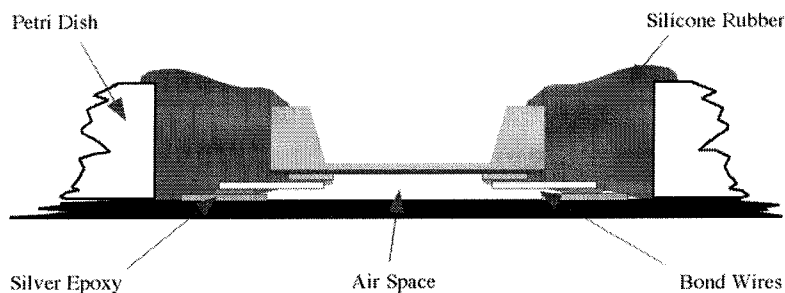


Figure 4-6: Ideal mounting of neurochip to printed circuit board using silver epoxy for electrical connections and sylgard to seal and insulate the leads as well as to cover any toxic surfaces.

For successful mounting of a neurochip to a printed circuit board, the above deficiencies must be addressed. Coating the bare sidewalls of the chip with Dow Corning 1-2577 Conformal Coating insulates them and eliminates silver epoxy-to-silicon shorting. Once the chip is connected to the PCB, additional conformal coating is flowed into the air space beneath the die as a precaution against leakage and to strengthen the membrane. The petri dish is then affixed and a sylgard coating spread over all non-micromachined surfaces to complete the assembly (see figure 4-7.b).

The realized PCB-neurochip assembly is shown in figure 4-8. It has 16 traces running from the bottom of the silicon die to a 25-pin ribbon cable connector. Neurons are plated and incubated in the same manner as is typically done in normal cell culturing. When conducting electrophysiology on the network, the PCB dish can be taken to a microscope platform and quickly connected into the required electronics. Testing can be performed for about 30 minutes in normal room conditions before the chips need to be
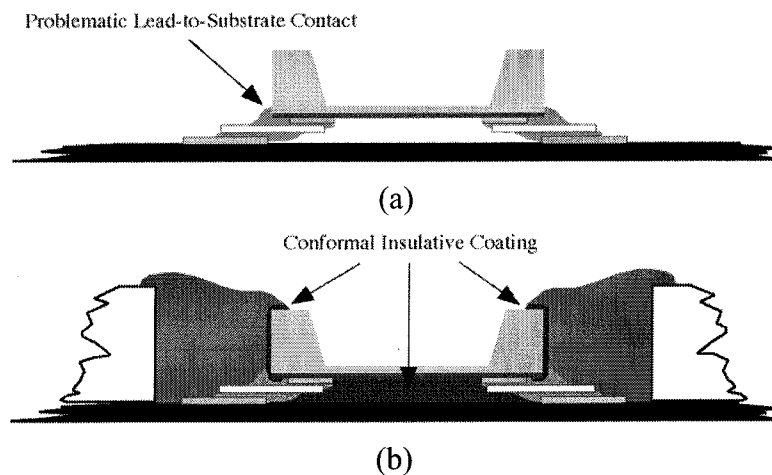


Figure 4-7: Problematic shorting between the bare silicon chip and the bond pads/wires (a) requires a conformal coating be applied to the edges of the dies (b) and for strength it is also flowed beneath the membrane to strengthen it.

returned to their $CO_2$ incubator. This system also allows continuous monitoring of the culture in a sealed oven for those experiments not requiring visual monitoring.

Although this system has been used successfully, the PCB-neurochip assembly slowly degrades over the course of weeks to months. Moisture from the culture medium and the high humidity incubator atmosphere is able to penetrate the overcoat of sylgard and slowly degrades silver and gold epoxies bonds, tin-lead solders, and bare tinned-copper wires. The unprotected pins in the ribbon cable connector are also subject to corrosion. Ultimately, the neurochips should be reusable and their electrical characteristics should not change over many years. The PCB-neurochip assembly fails to meet these requirements.

### 3.4.2   Ceramic Carrier Neurochip

Figure 4-9 shows a neurochip assembly mounted onto a ceramic component carrier with gold-plated pads and leads. Similar to the PCB mounting procedure described above, wire leads are bonded to the chip and then to the ceramic carrier, a petri dish is bonded to the package, and surfaces are coated with sylgard. Unlike the PCB-neurochip assembly, this system uses ultrasonically bonded gold wires to electrically connect the chip to the carrier. To accomplish this, it is necessary to wire-bond to the chip first, leaving the ends of the wires dangling rather than immediately attaching them to the package. To protect the delicate wire bonds from breakage, the entire backside of the chip is coated with sylgard before it is flipped over and glued to the carrier. The free

ends of the wires are then ultrasonically bonded to the gold-plated pads of the ceramic carrier. A separate gold wire attached with silicone to the inside of the culture dish serves as a permanent ground reference. A petri dish is then affixed and a sylgard coating spread over all non-micromachined surfaces to complete the assembly.

This mounting scheme is very robust. Eight chips mounted in this manner have survived regular re-use for more than a year. For electrical testing and experimental measurements, the neurochip carrier is mounted into a zero-insertion-force socket. Between experiments, continuous exposure to the $CO_2$ incubator environment does not pose a problem. Since all wires, bonds, and connector pins in this assembly are either solid or plated gold, corrosion is not an issue.

After a culturing session, which typically lasts 1 to 3 weeks, the chips are cleaned
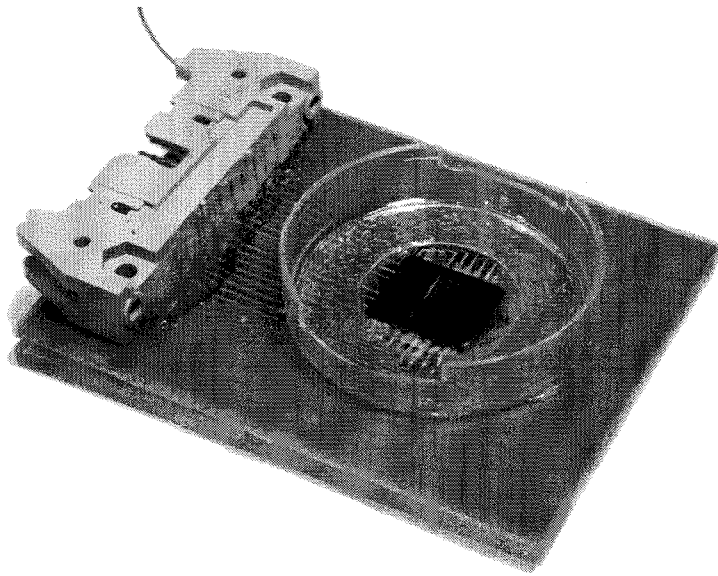


Figure 4-8: Final neurochip assembly employing a printed circuit board carrier that was used in initial electrophysiological experiments. This packaging proved to be incompatible with long-term exposure to the highly humid environment needed to grow neural cultures. Over time moisture penetrates the sealing silicone rubber and corrodes the chip-to-PCB bonds.

for re-use. No changes in electrical performance or cytotoxicity are seen. The cleaning protocol is: 30 minute soak in 5.25% household bleach in water; rinse with de-ionized (DI) water; soak 30 min in 30% hydrogen peroxide; rinse with DI water; soak in water overnight; dry. All steps are performed at room temperature. The bleach removes cell debris and the cell-adhesion molecules. The peroxide re-oxidizes surfaces for better adhesion with the next treatment of cell-adhesion molecules. The multiple rinsing steps are necessary to completely remove the toxic cleaning substances.
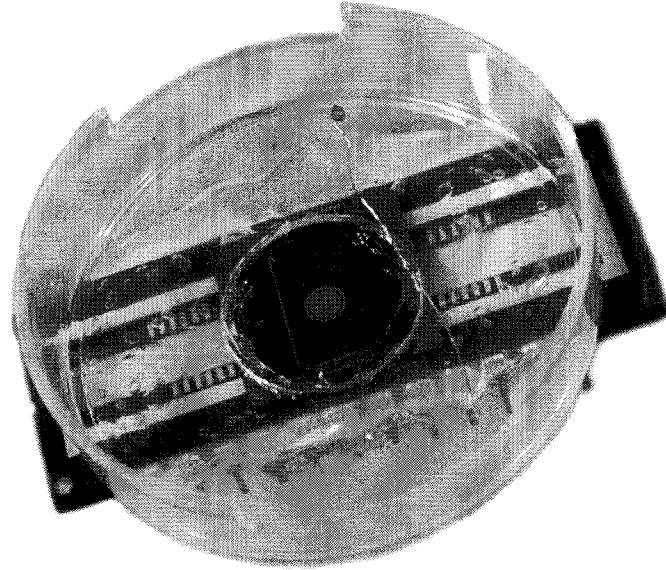


Figure 4-9: Ceramic carrier neurochip assembly that has been shown to be fully compatible with long-term exposure to the environmental conditions in a $CO_2$ incubator. This device has been used repeated for more than 12 months without any failures and with no notable degradation of the electrical properties of the neurochip itself.

# CHAPTER

# 5

# THE NEUROCHIP:
# NEURAL ELECTROPHYSIOLOGY
# WITH NEUROWELL ARRAYS

The ultimate goal of this research has always been to create a family of devices that will enable new avenues of research and rehabilitation. Developing a microstructure for the containment of and electrical interaction with a single neuron was deemed the preferred method to achieve this objective. Used as a building block, neurowell arrays formed into devices called neurochips and neuroprobes have begun to show their potential in both *in vitro* and *in vivo* environments, respectively. With continued research, more advanced versions of these proof-of-concept devices have the potential to address many of the challenges being faced in many of the fields that work with the central nervous system. The following chapter presents the preliminary results achieved

thus far.  The majority of experimentation to date has involved work *in vitro*.  Still, several important milestones have been achieved in the area of *in vivo* applications.

It should be noted that the sections of this chapter covering the cell culture experimental results are being included in this dissertation for the sake of completeness. Three teams of scientists working in close collaboration have made this research successful.  Each team is chiefly responsible for one of three areas:  micromachine design and fabrication, *in vitro* culture or *in vivo* experiments.  However, the iterative and evolutionary nature of this work has resulted in each team making notable contributions in the "fields" of the others.  While some of the research in the area of cell culture (most notably with SCGs) has been conducted by the author of this thesis, the majority of the results presented in the following pages should be considered as the work of the members of the *in vitro* and *in vivo* teams.


## 5.1   The Neurochip for *In Vitro* Experimentation

A single neurowell is of little practical use but when arrayed in large numbers the collection becomes a very powerful tool.  For *in vitro* experimentation a so-called neurochip has been created which utilizes a 4 x 4 array of neurowells.  In use, embryonic or neonatal neurons are cultured in each well.  As the neurites grow out into the surrounding environment, they encounter processes extending from the neighboring neurowells.  Over the course of several weeks, synaptic connections are created and an active neural network forms.  At present, this process is allowed to proceed in a random

fashion. Future work may include structures that preferentially direct the neurites to specific neighbors. Adding chemical and electrical stimuli during neurite outgrowth may allow the network to be programmed for a desired task or function.

The neurochips that have been fabricated up to the present time consist of 4 x 4 arrays of neurowells positioned at the center of a 4 x 8 millimeter, 16 micron thick membrane (see figure 5-1). This thin, fragile membrane is supported around its

gold leads/insulation

500 μm

1 cm

silicon

20 μm

3 mm

**3D view of a neurochip**

gold electrode          oxide/nitride insulation

thermal oxide

neuron wells

grillwork for cell body containment

**Neurochip in cross section        Magnified neurowell in cross section**
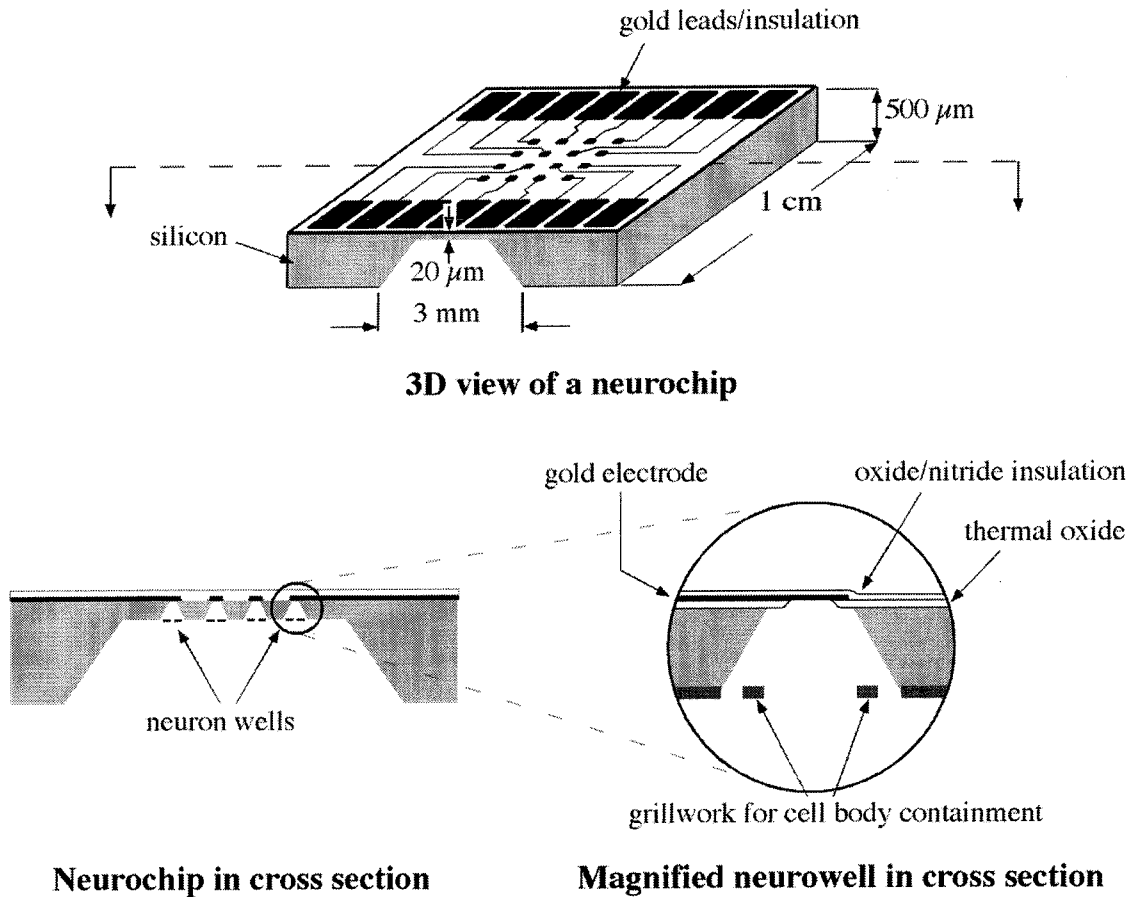
Figure 5-1: Schematics detailing the neurochip as a whole from the electrode side of the die (top center), as a cross section showing the 20-micron thick, neurowell-containing silicon membrane stretched across the 500-micron deep cavity (lower left), and a close-up of one of the neurowells in the membrane pointing out the salient features and the some of it construction materials (lower right).

periphery by a 500-micron thick frame of silicon.  The wells have been arbitrarily

positioned on 100 micron centers although spacings down to 35 microns (each well is 30

microns wide) are easily achievable.

Electrical connections from the neurowell electrodes to external electronics are

incorporated into the neurochip.  From the electrode at the bottom of each well, fine gold

wire traces run along the backside of the membrane to the thick pad frame.  On the thick

silicon are bond pads that sit on top of thermal oxide that is 1 to 2 microns thick.  The

oxide is necessary to minimize parasitic capacitance in the system.  Gold wire bonds

connect the bond pads to a commercial chip carrier that is readily plugged into an

external electronics board.  A completed neurochip assembly is shown in figure 5-2.
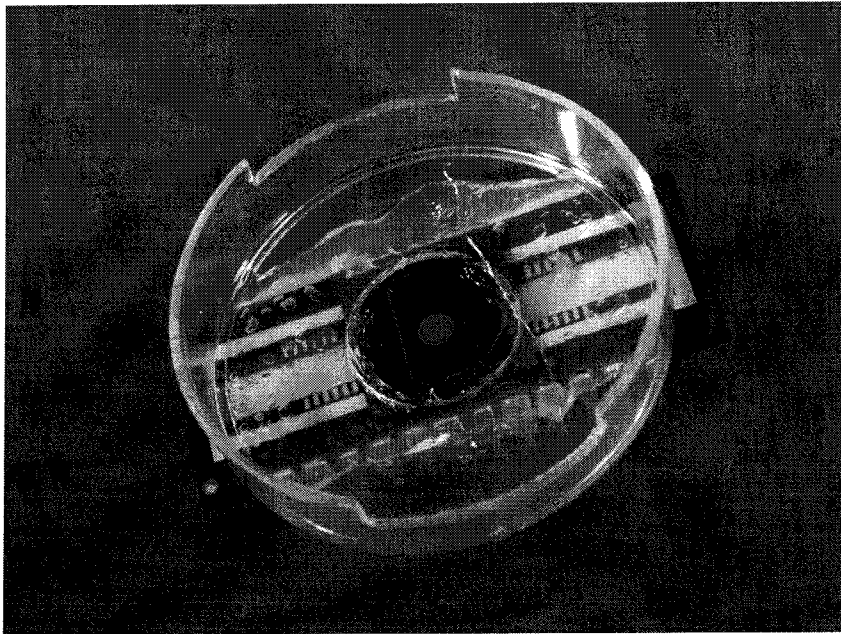


Figure 5-2:  Neurochip mounted in a ceramic chip carrier package, sealed with sylgard (silicone rubber), and surrounded with a petri dish.  This system allows a culture to be kept in a $CO_2$ incubator for long periods of time and then to be quickly connected into a dedicated electronics system in normal room conditions.

While preliminary neurochip designs have been limited to arrays of just 16 neurowells, much larger arrangements can be readily produced. On the present 4 x 8 millimeter membranes, arrays as large as 40 x 80 for a total of 3200 wells can be fabricated with minimal difficulty. The limitation to such a neurochip would be the wiring and sampling associated with so many neurons. Several wiring layers would be necessary and for practical use, on chip electronic multiplexers and amplifiers would need to be added to make off chip wiring manageable. The electronics could be added either by fabricating them in the silicon support frame of the neurochip or by using flip chip bonding. For ease of production, flip chip bonding would be the more desirable of the two options.

## 5.2   Cell Culture

The silicon and silicon nitride surfaces of the neurochips are treated to promote cell adhesion. The surfaces are first oxidized with 30% hydrogen peroxide at room temperature for 30 minutes followed by a thorough rinsing with DI water. After air-drying, the chips are sterilized with a 45 minute exposure to UV light. If water is introduced to a dry neurochip, surface tension prevents the water from entering the wells. Liquid is introduced into the wells by first wetting the chip with 95% ethanol for 5 minutes, then rinsing five times with sterile water. They are then soaked in a 0.22 micron filter-sterilized 1 mg/mL poly-DL-lysine solution dissolved in Hank's Balanced Salt Solution (HBSS, without divalent cations, Gibco #14170-120) for 45 minutes at room

temperature, then rinsed 5 times with sterile HBSS.  To promote rapid axonal outgrowth [43], the chips are next soaked with a 20 μg/mL solution of laminin (Sigma #L-2020) in tissue culture medium for 45 minutes at room temperature, then rinsed 5 times with tissue culture medium.

Fetal rat hippocampal neurons are prepared using a method modified from [16]. At 18 days gestation, embryos are removed by caesarian section from a pregnant, $CO_2$-asphyxiated Wistar rat.  Hippocampi are dissected from the embryonic brains and stored in ice-cold, oxygenated HBSS.  The extracellular matrix of the tissue is weakened by incubation at 37 °C in 0.25% trypsin (Gibco #15050-065), followed by dilution in tissue culture medium supplemented with 5% equine serum to neutralize the trypsin.  The partially digested tissue is centrifuged and re-suspended in tissue culture medium.  The cells are then fully dissociated by gentle trituration with a sterile plastic 1000 μL disposable Pipetman pipette tip.  This method gives an ≈ 90% yield of viable cells after one day in culture, with neurons composing ≈ 95% of the population (determined by cell morphology after one day in culture).  The few glia present during plating are killed by adding 2.5 μM cytosine arabinoside (Ara-C, Sigma #C-1768) to the medium after 24 hours in culture.

The tissue culture medium is Neurobasal™ (Gibco #21103-049) with B27 supplement (Gibco #17504-044) plus 500 μM glutamine (Gibco #35050-061).  The medium initially added to new cultures is also supplemented with 25 μM glutamate (Sigma #G-1251) and 25 μM β-mercaptoethanol (Sigma #M-6250).  Cultures are

maintained by replacing half the medium after four days in culture and once per week thereafter. Between treatments, the cells are incubated in a 5% $CO_2$, 100% humidity, and 37 °C atmosphere. This serum-free medium inhibits glia proliferation and has been shown to maintain good survival of hippocampal neurons for four days in culture [16]. Although not satisfactory for truly long-term experimentation, this culturing technique is adequate for demonstrating many of the capabilities of the neurowells. Survival beyond seven days in culture is very low in the absence of glia; a more complex technique that addresses this issue is discussed in more detail below.

Neurons are plated onto the neurochip at 100-500 cells/mm$^2$. Individual neurons are manipulated into neurochip wells using a pulled glass pipette whose tip is sealed into a 10-micron diameter ball using a hot platinum filament. On video, this procedure takes
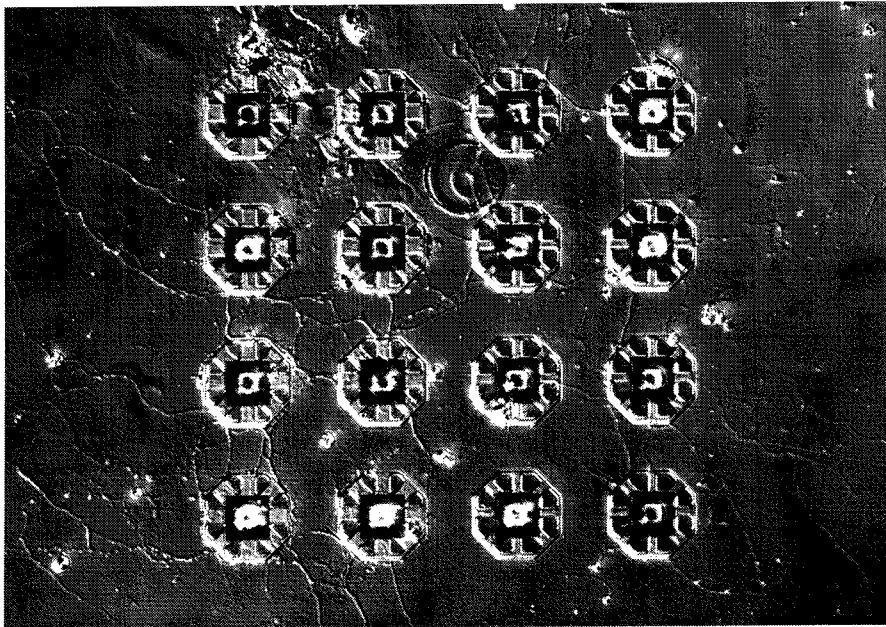


Figure 5-3: Nomarski micrograph of a hippocampal culture in a canopy neurochip with a prolific, interconnecting network of neural processes weaving themselves across the surface of the silicon in the area between the neurowells.

on the appearance of a micro hockey game with the neuron playing the part of the puck. All extra neurons within 2 mm of the wells are removed after cell attachment (2 hours) using gentle suction from a 25-micron tip diameter pipette. This procedure isolates the network in the neurochip wells from the other neurons in the culture, allowing an unambiguous identification of processes. Any neurites seen in the well region originate from cell bodies in the wells. Outside the 4-mm diameter area near the neurowells, the remaining neurons (approximately 3,000 to 16,000 cells) are allowed to grow normally to condition the medium and to act as a control. Fully separated control cultures are normally plated onto sterile plastic 35-mm tissue culture dishes coated with poly-DL-lysine and laminin as above. After 2 hours for adhesion, all dishes are flooded with 2 mL of tissue culture medium. Figure 5-3 is a photomicrograph of hippocampal neurons after eight days in culture growing in a neurochip, illustrating the survival and outgrowth of twelve neurons in the wells.

Hippocampal neurons in culture require additional growth factors produced mainly by astrocytes [30] which are absent in serum-free culture systems. In the absence of glia, neuron survival rarely exceeds 10% after 2 weeks in culture (the age at which enough synapses exist to consider the network to be mature). However, astrocytes on the surface of the neurochip tend to grow on top of the canopies and into the wells, covering the electrodes and occasionally giving the cell bodies of the neurons a pathway for escape. Separate cultures of glia are therefore grown on 20 mm cover slips by supplementing the Neurobasal medium with 5% defined equine serum (Hyclone #A-

3311-L) until confluence at 1-2 weeks. These cover slips contain a variable mixture of neurons, astrocytes, oligodendrocytes, and microglia. When a new neurochip culture is started, the glia cover slip is placed onto the neurochip, with the glia facing the neuron surface 2 mm away. Microglia tend to proliferate on these cover slips and usually comprise 2-10% of the cells (as determined by non-specific esterase activity (see [28]). Microglia are known to produce factors toxic to neurons [27], so the cover slips are treated with 20 mM L-leucine methyl ester [64] for 2 hours at 36 °C to kill the microglia. This procedure has no noticeable long-term effect on the macroglia or neurons on the cover slip, and yields improved survival of neurons on the neurochips. The leucine methyl ester treatment typically leaves approximately 10% of the microglia alive; the cover slips on neurochips are changed once weekly to reduce toxicity from proliferation of the remaining microglia.

## 5.3   Cell Viability

To determine whether being loaded into a neurowell is harmful to a cell, measurements of the viability of cells growing on flat silicon, away from the neurowell region, were made concurrently with observations of cells in the neurowells. Viability, defined as the current cell density divided by the plating density, is the preferred means of determining cell survival, as it is not necessary to determine the fate of the dead cells. If neuron density is not uniform, viability measurements can be hampered by measurement fluctuations and by cell migration. In the following measurements,

viability was determined by making each density count in the same, well-defined area on the chip.

Formal investigations into cell viability when cultured in canopy neurowells have been performed. Initial outgrowth testing was conducted by loading 46 sets of 16 neurowells with embryonic rat hippocampal neurons. Cultures were observed for six days, at which time synaptically driven activity in the network generally begins. Twenty-four cultures (52%) survived at least six days. On the 24 living arrays, 209 neurowells had living cells at six days in culture, for an average of 54% probability that a cell loaded into a neurowell will survive. Ten cultures died before six days owing to infection. The cause of early death in the remaining 12 cultures was not determined. For these experiments, neurochips were loaded with neurons in a non-sterile environment. A sterile neurochip-loading station has since been established and infection rates have been reduced to less than 5%, identical to controls. While not confirmed by further rigorous investigations, circumstantial evidence from subsequent experiments suggests that the improved plating conditions has also increased neuron survivability over the 54% stated above.

In determining the effect of neurowell confinement on cell viability, eight arrays of 16 wells were implanted with neurons. In close proximity to these cells, a gross plating of neurons were deposited as a control. Both sets of cells grow in the same medium and on the same surface to minimize culture variables. The graph shown in figure 5-4, presents the data collected; the x-axis displays cell viability of the control

group and the y-axis the cell viability of the implanted neurons. Data from the entire life span of these cultures were included, even as the cultures began to die (these are the data with low viabilities). The slope of the data is near one, suggesting that being in a neurowell has no detrimental effect on a cell. Not included in the data are the points from the first two days in culture, as the grillwork obscures the early stages of process growth and artificially lowers the apparent neurowell occupancy. There appears to be a ceiling; neurowell occupancies above 80% (13/16 neurowells) were not observed. Part of this effect may be due to the possibility of escape through the central hole immediately after the neurowells are loaded.
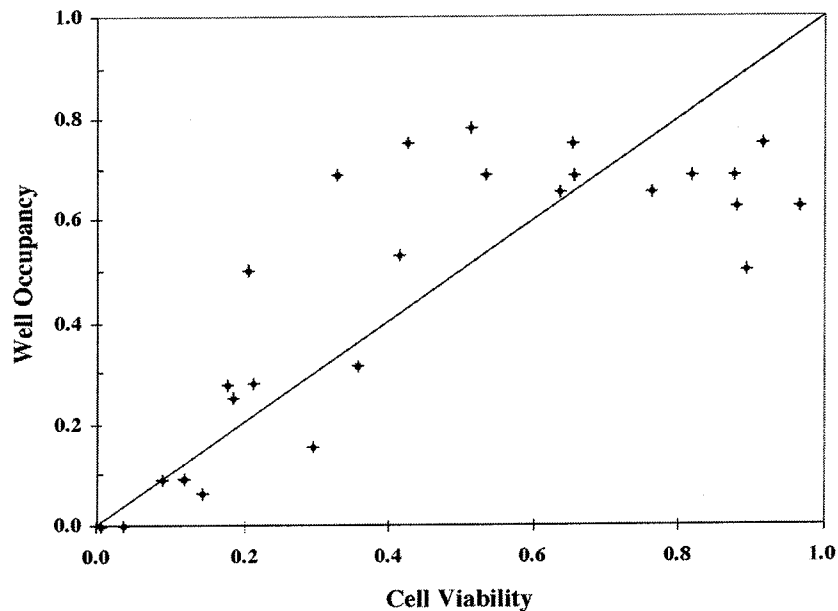


Figure 5-4: Graph comparing cell viability as a function of whether it has been implanted in a canopy neurowell or is growing in an open area. The data indicates that life in the microcavities does not seem to be detrimental to the growth and survivability of the neurons.

## 5.4   Neurowell Recording

When a neuron in a neurochip well fires an action potential, the extracellular signal detected by the electrode is determined (in this geometry) by the resistance from the neuron to ground and by the current emitted during the event. Since the cell bodies are generally pulled to the top of the well by tension generated as the processes mature, the resistance to ground is $R_{well}$ = 17.5 kΩ (see section 3.1). The actual shape of the signal can be quite complex [31, 58], but the largest component occurs when the voltage-gated sodium channels drive the fast depolarization of the membrane of the cell body and dendrites. As discussed in section 4.1, the neurons have a membrane capacitance $C_m$ = 80 ± 20 pF and the membrane potential rises at a maximum rate of $dV/dt$ = 100 ± 40 V/s when firing. After the peak in voltage of the action potential, voltage-gated potassium channels open and repolarize the membrane at $dV/dt$ ≈ -30 V/s. The electrode is therefore expected to record a -140 μV signal (given by - $C_m R_{well}$ $dV/dt$) during the fast, depolarization phase of the action potential, which lasts about 1 msec, followed by a +42 μV repolarization signal lasting 3 msec.

Spontaneous activity in these cells is driven by synaptic inputs, which drive current through the cell body to ground. Depending upon the synaptic strength, these cause the cell body to depolarize 10-30 mV in 0.5-5 msec, for a current emitted by the cell body ranging from 160 pA to 5 nA. Before the main stroke of the action potential, this is expected to generate a +3 to +88 μV signal at the neurochip electrode.

Figure 5-5 shows five spontaneous action potential signals detected by neurochip

electrodes from a 15 day-old culture, measured at 22 °C. The digitization rate is low to

facilitate long recording times, which were necessary to capture these relatively rare

events. The signals are aligned at their maximum negative deflections. The signals are

stereotyped and triphasic, with a +54 μV component, followed by a -90 μV phase and a

+30 μV phase. These three phases are consistent with the theory outlined above. We

therefore identify the first phase as being synaptically-drive, the second phase as the main

depolarizing stroke, and the third phase as the slower repolarization of the membrane

potential. Similar behavior has been observed in two cells. Superimposed on the data

traces in figure 5-5 is a whole-cell recording of an action potential in a hippocampal
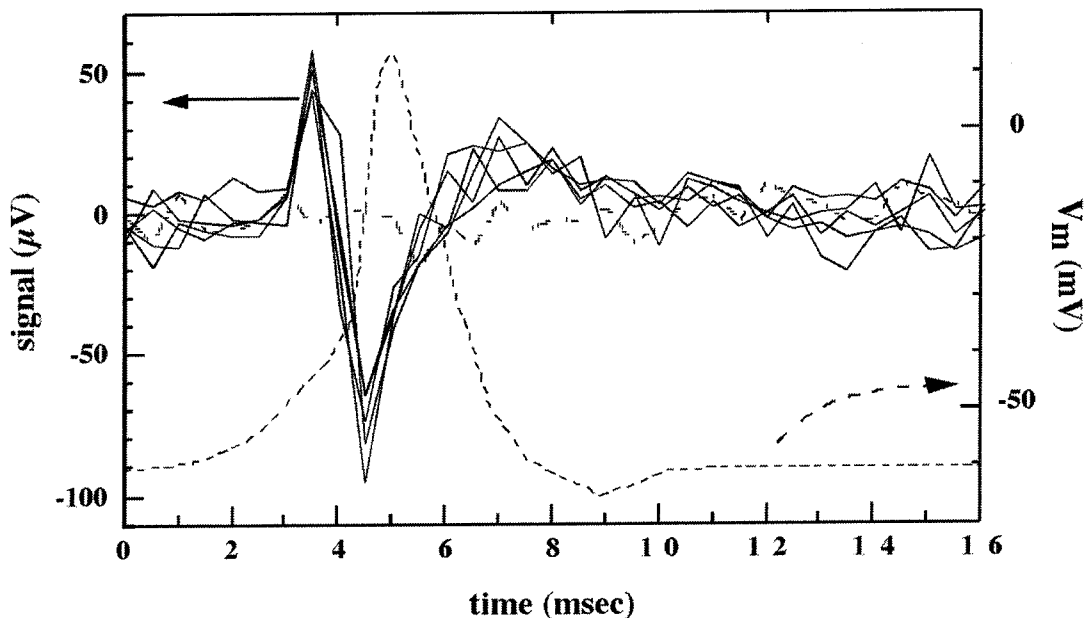


Figure 5-5:  Five recordings of spontaneous action potentials recorded from a
neuron implanted in canopy neurowell. The age of the culture was 15 days and
data were digitized at 2 kHz and a standard whole cell recording make with a
patch pipette is included (dashed line) for comparison.

neuron from a separate culture.   This illustrates our interpretation of the signal

components and shows that the time course of the neurochip signals is consistent with an

action potential.

Similar signals are observed in response to an external stimulus.  Stimulation was

achieved by applying a brief (1 to 10 msec) pulse of 1 M KCl from a 2-micron diameter

pipette in the vicinity of axons leading to the cell bodies, 500 microns from the wells.  In

control experiments, KCl puffs were found to be a reliable method of depolarizing the

cell and eliciting action potentials with undetectably small electrical artifacts.   Other

experiments show that this procedure will stimulate the axon and not the cell body.
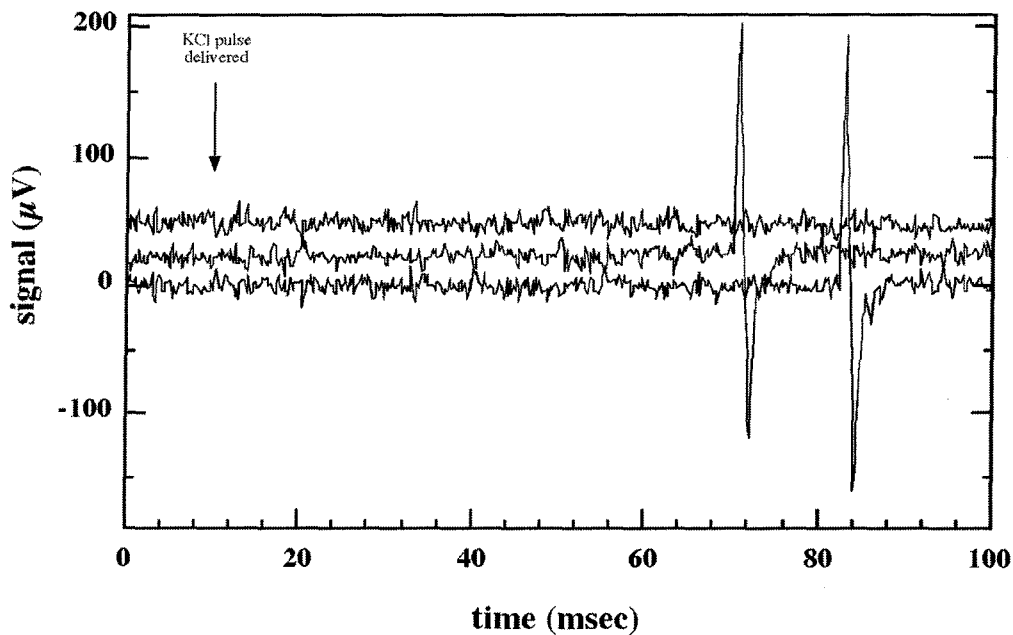


Figure 5-6:  Three neurochip recordings of a cell in a canopy well that is being
stimulated with pulses of 1 M KCl of varying length beginning at the arrow.  The
top trace has no elicited action potential spike and represent a 5 msec long pulse.
The lower two traces were recorded after a 7 msec KCl pulse and the resulting
action potential spikes are clearly observed.

Figure 5-6 shows voltage traces recorded from a neurochip electrode when the cell in the well is stimulated in this manner at 22 •C. The response exhibits all-or-none behavior, with no change in amplitude or shape at stimuli above threshold and no response below threshold. Similar behavior has been observed in two cells. The response is biphasic; the large positive stroke likely results from antidromic stimulation as the action potential from the axon invades the cell body, while the negative phase is driven by the voltage-gated sodium channels. No repolarization phase is visible here, probably because the extracellular potassium level rises due to the KCl pulse. In control cultures, cells stimulated with large KCl pulses take several hundred milliseconds to repolarize.

## 5.5    Neurowell Stimulation

To enable bi-directional interaction between neurowells and the neurons implanted within them, electrical stimulation of a cell body must be achieved. Due to the uniqueness of the micromachined structure, several non-traditional considerations must be taken into account when exciting a neuron. The following section addresses practical issues that arise in a canopy neurowell and the achieved experimental results. The theoretical analyses for stimulating an implanted cell with a neurowell electrode is presented section 4.1.

### 5.5.1    Fluorescent Dye Recording

When a neurochip electrode is used for stimulation, the stimulus artifact (of order

1 volt for • 10 msec) is too large and rapidly changing to allow clean detection of the

action potential signal from the neuron (of order 100 μV, 1-2 msec after the stimulus

ends). Therefore, we monitored the membrane potential of the cell in neurochip wells

with the voltage-sensitive fluorescent dye RH237 (Molecular Probes). RH237 is a

member of a class of voltage-sensitive dyes which operate partially on an electrochromic

mechanism, in which the transition to an excited state involves a physical displacement of

charge parallel to the electric field in the membrane [25, 45]. This causes the peak of the

excitation spectrum to shift dependent upon the membrane potential. When the dye is

excited in a single narrow wavelength band away from the excitation maximum, the

fluorescent yield depends on the membrane potential. In the case of RH237, a

depolarization of the cell membrane results in a reduction in fluorescence intensity.

We use a low-noise photodiode (Hamamatsu S1087-01) mounted in the trinocular

tube of an Olympus BHMJ microscope with a 40X, 0.75 NA water-immersion lens to

detect the fluorescence emission. The detector covers the image of one well. The light

source is a 100 W mercury arc lamp driven by a current-regulated power supply. Noise

in the light output is reduced to approximately 0.01% using a shunt regulator driven by a

second photodiode mounted inside the lamp house [19]. The dye is excited by the 546

nm green line of the arc lamp. A dichroic mirror and a long-pass optical filter direct the

red emission light toward the detector. The photodiode current passes through a low-

noise 6 GΩ transimpedance amplifier [20] and is digitized through a neurochip A/D

converter channel.

Photobleaching and phototoxicity complicate fluorescence imaging of live cells. These are both at least partially caused when oxygen absorbs the energy from excited dye molecules, generating singlet oxygen that destroys the dye and the cell membrane. To limit photodynamic damage, the cell membranes are loaded with the potent antioxidant, astaxanthin [29]. Astaxanthin was dissolved at 1 mM in DMSO containing 20% Pluronic F127. Sonicating for 1 hour at room temperature fully dissolves the astaxanthin, and the solution is filtered at 0.22 μm to sterilize and to remove debris. This stock solution is diluted in serum-free tissue culture medium and added to the cultures at a final concentration of 10 μM. Cultures are incubated for 1 hour at 36 °C before staining with fluorescent dyes. Pre-loading the cells with astaxanthin approximately doubles the safe exposure time. In these experiments, fluorescence intensity decreases exponentially with illumination time with a time constant of 6.0 ± 0.9 sec. Alteration in the membrane properties begins after roughly 5 sec of illumination. We use a mechanical shutter to give 100 msec illumination times so that roughly 50 trials are possible before irreversible damage occurs.

## 5.5.2    Detection of Evoked Action Potentials

The neurons are stained with 5 μM RH237 in recording saline for 10 minutes at room temperature. Figure 5-7.a shows the fluorescence signal of a cell given bipolar stimulus pulses from the neurochip electrode at 22 °C. In both traces shown, the cell has received a 12 μA biphasic (200 μs per phase) current stimulus passed through the well

electrode. Small responses can be seen when a cell is stimulated: (1) a small, fast fluorescence change during the current injection (in-phase response), and (2) a slower response beginning after a 1-2 msec delay (delayed response). We identify the fast response as the average membrane potential excursion of the cell body during the stimulus. Given the linearity of the dye response of RH237 [20], this signal should be zero if the cell is being stimulated symmetrically. In figure 5-7.a, the solid trace (negative current first) shows a clear action potential resulting from the stimulus, while the dotted trace (positive current first) shows no net response after the stimulus.

Figure 5-7.b summarizes the responses of a different cell to varying stimulus strength. The horizontal axis indicates the size of the first phase of the stimulus. The in-phase response of the fluorescence is roughly linear for all stimuli. For stimuli more negative than a threshold between -5 and -10 µA, the cell fires an action potential whose size and shape is independent of stimulus strength. Similar behavior has been observed in ten neurons. Note that the observed action potentials, normally 1.5-2 msec wide (figure 5-5), are widened to 4-5 msec in the dye recordings (figure 5-7a). Simultaneous whole-cell and voltage-sensitive dye recordings of hippocampal neurons grown on a flat plastic substrates showed that neurons heavily stained with RH237 show an increase in membrane capacitance by a factor of 2-3 relative to identical, unstained cultures, and similar increases in action potential width.

The fluorescence change during an action potential is disappointingly low, usually 0.5-1.0%. RH237-stained hippocampal neurons have been observed to give signals as
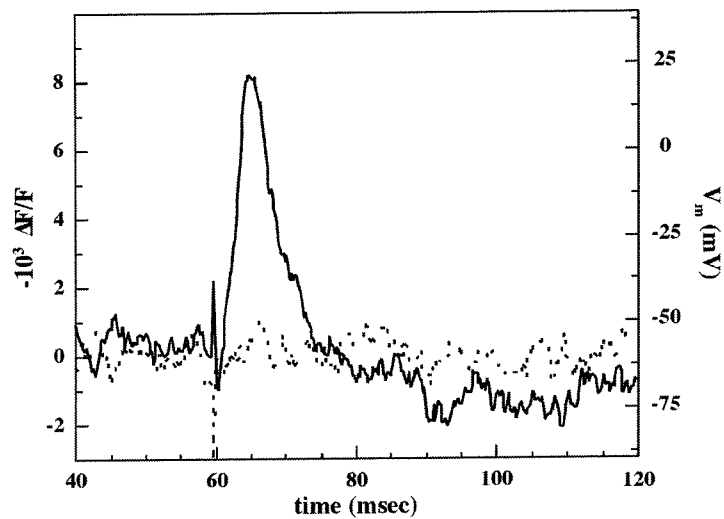
(a)
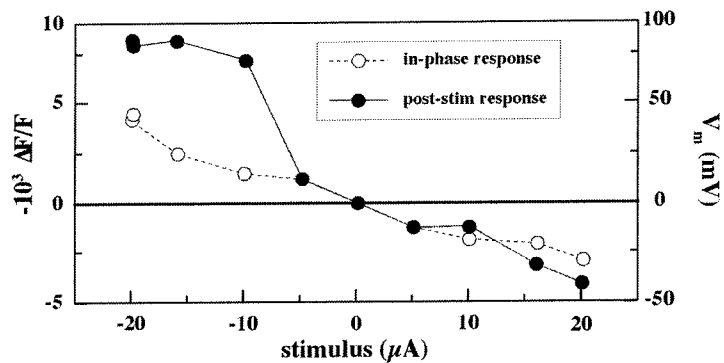


(b)

Figure 5-7:    (a) Fluorescence recording from a cell in a canopy neurowell stimulated by the neurochip electrode. Photo bleaching was removed by an exponential fit. The right axis is a voltage calibration assuming that the resting potential is -60 mV and the action potential is 80 mV high. The solid line is the fluorescing response measured when the neuron is stimulated with a negative-current-first biphasic pulse. The dotted line is the response of the same cell given the same stimulus but with a positive-current-first pulse by which no action potential was generated    (b) Plot showing the sign-dependence and threshold behavior of the response. Open circles indicate the response during the stimulus while the solid circles show the maximum fluorescence delayed response. The abscissa indicates the current during the first half of the biphasic stimulus. The right axis indicates the estimated voltage change from resting potential. The in phase response is linear with stimulus strength. For positive stimuli (which do not elicit action potentials), the post-stimulus response is also linear in stimulus strength. For stimuli more negative than -10μA, the delayed response shows a stereotyped size and shape.

large as 5% in control cultures. The cell bodies of hippocampal neurons in culture tend to collect debris, which stains brightly with membrane-bound dyes and adds to the background, potential-insensitive signal. This problem is exacerbated in the neurochip wells, where weakly bound debris is relatively sheltered from being dislodged.

## 5.6    *In Vitro* Experimentation Summary

Action potentials arising from individual hippocampal neurons placed within the wells of the neurochip can be detected with a signal-to-noise ratio of 35-70:1, with no detectable crosstalk between channels. Action potentials can also be elicited with a threshold charge delivery more than a factor of two smaller than the hydrolysis level. Thus, the neurochip can now be used to study isolated neurons over long periods.

Hippocampal neurons from E18 rats in culture form large numbers (on the order of 1000) of functional synapses, beginning at around 3 days and maturing after approximately 2 weeks [13, 24, 69]. Thus, it is expected that the neurochip will be a useful device for studying networks of these neurons. The main barrier is low survival of cultured hippocampal neurons beyond 7 days in culture in the absence of glia. Occasional cultures have high survival (similar to [16]); however, we typically achieve less than 10% survival in NB/B27. So far the work has been conducted in a serum-free system because if glia are allowed to proliferate on the neurochip, they tend to pack the wells, sealing off the electrodes and forcing the neural cell bodies out of the microcavities. Recent work has shown that low densities of glia (50 cells/$mm^2$, primarily astroglia) support high survival rates (> 50% at 3 weeks in culture) without entering the wells. Thus it is reasonable to expect that soon, the neurochip will be able to be used to conduct long-term studies of cultured hippocampal neuronal networks.

# CHAPTER

# 6

# THE NEUROPROBE: NEUROWELL ARRAYS FOR *IN VIVO* EXPERIMENTATION

*In vivo* experimentation requires a tool quite different than that used *in vitro*. In traditional *in vivo* recording techniques, insulated wires or micromachined probes with metal exposed in one or more regions are inserted into the host system. Local tissue damage is unavoidably caused by this penetration creating a layer of damaged or dead cells in the vicinity of the probe. Over time the damage causes the host environment to encapsulate the probe in the equivalent of scar tissue. This can significantly reduce the SNR, as healthy neurons are not in immediate contact with the electrodes. With chronic stimulation, the non-specific inputs may introduce unintended and undesirable changes in the stimulated nervous system (so-called "rewiring"). Furthermore, these devices indiscriminately (with respect to cell type) stimulate or record all nearby neurons.

## 6.1    Neuroprobe Configuration

Incorporating neurowells into an implantable probe allows "linking neurons" to bridge the damaged region surrounding the device. This concept is show schematically in figure 6-1. The embryonic neurons, freshly implanted into the probe, extend their processes into the brain tissue into which the probe has been inserted. If the "linking neurons" establish functional synaptic connections with the surrounding neural tissue, they can serve as an interface between the recording electrodes and the host nervous system. In a sense they act as spies who target neurons of the same kind as they are. The resulting living bridge can eliminate the problems related to neuronal damage around the probe and the resulting poor SNR.
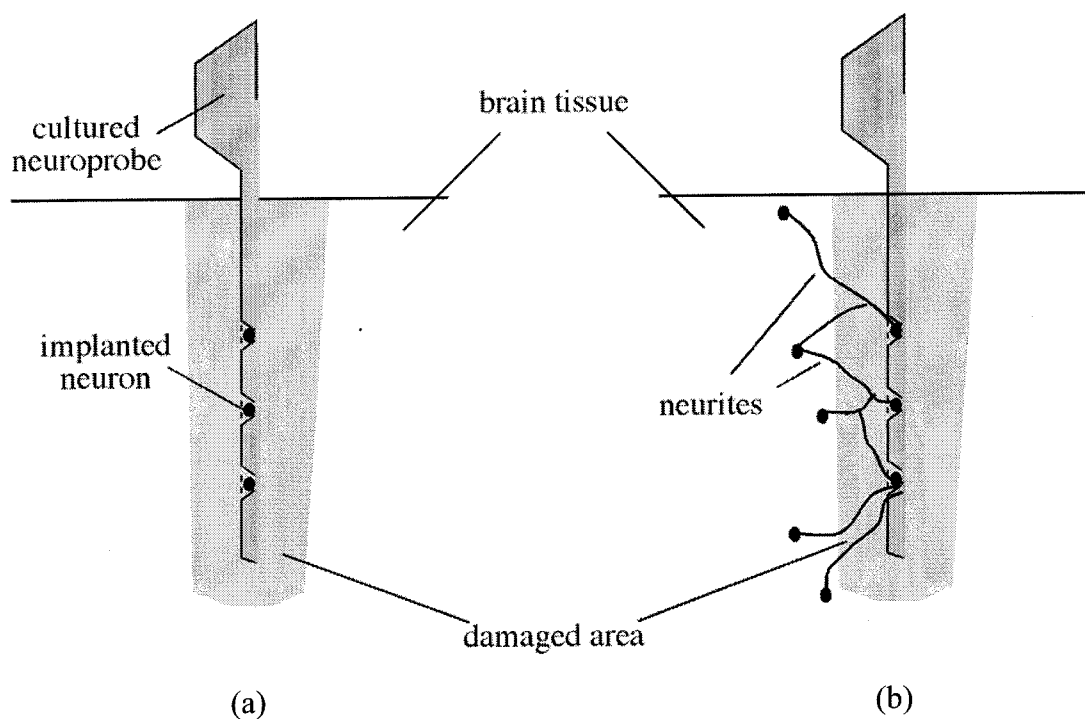


Figure 6-1: The schematic use of the cultured neuroprobe: (a) cross section of the brain immediately after the insertion of the probe; (b) cross section after the formation of synaptic connections.

Problems arising from probe motion should be less significant as the connections made by the "linking neurons" between the probe and the brain tissue are relatively flexible yet fixed at each end. This is expected to enable long-term, reliable devices for prosthetic applications.

For the *in vivo* device, a linear array of 1 x 16 neurowells is formed at the end of a 4 millimeter long, 100 micron wide and 16 micron thick silicon needle to create a so-called neuroprobe (figure 6-2). The length of the needle and the placement of the wells at its tip is intended to position implanted neurons at the proper depth inside the hippocampus when the probe is implanted in a host animal. The hair-fine needle is attached to a 500-micron thick silicon handle that is several square millimeters in size.



(a)                              (b)
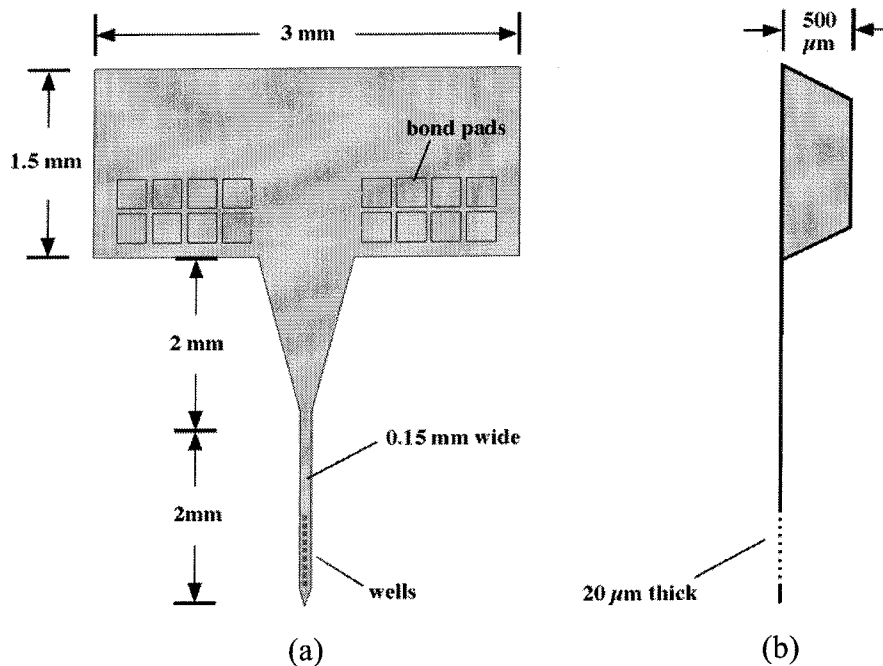
Figure 6-2: Geometric shape and dimensions of a neuroprobe. (a) Top view showing a typical footprint of the device which is defined by plasma etching and (b) the side view of the probe that is set by the thickness of the substrate wafer and the epitaxial silicon layer.

From the electrode at the bottom of each well, fine gold wire traces run along the backside of the needle to the thick handle which, like the neurochip, has gold bond pads on top of thermal oxide. Unlike the neurochip, insulated gold wires that run to a skull plug are attached to the bond pads. This assemblage is shown schematically in figure 6-3.
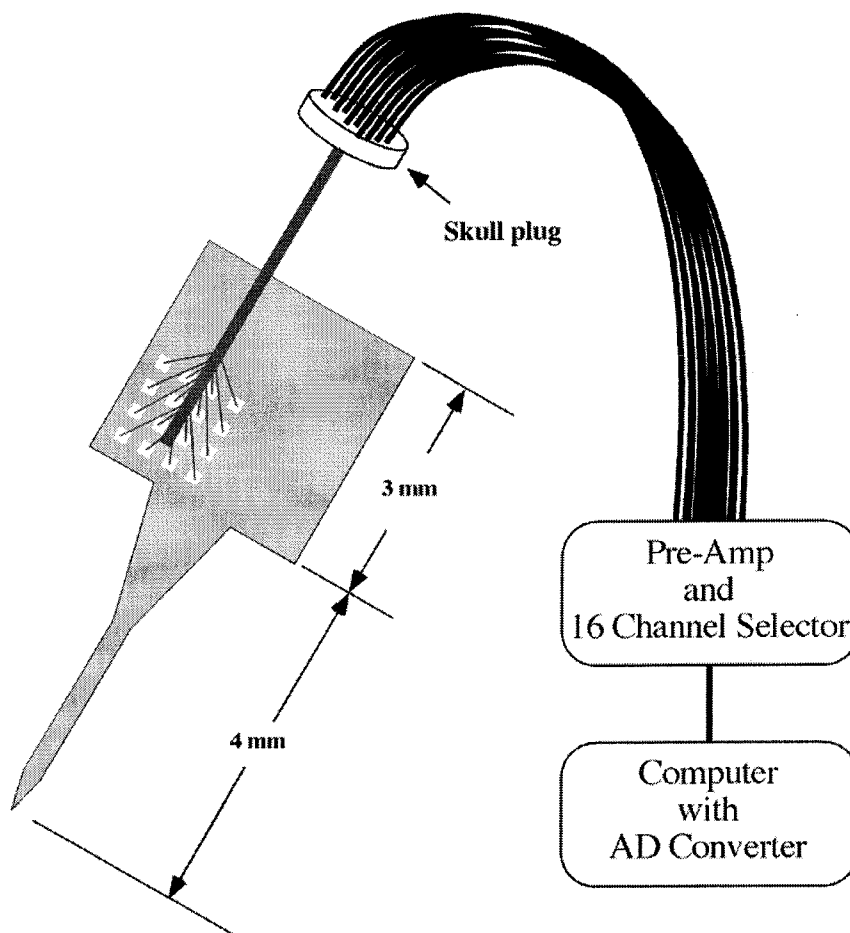


Figure 6-3: Conceptual preparation of a neuroprobe to be implanted into a host. The 4-mm long silicon needle places the active sites at the proper depth, the 3-mm-square handle holds the pads to which wires are bonded and run to a skullcap. From the cap, larger wires run to the electronic monitoring/stimulating system. In more advanced designs, the silicon handle contains CMOS circuitry to allow multiplexing and signal processing much closer to the neurowells, increasing signal-to-noise ratios as well as minimizing the size of the wiring-harness running to the outside world.

While a linear array of active sites is a useful tool, a more complex three-dimensional device would enable a much larger range of experiments and target systems. The ability to arbitrarily position the active site and to fabricate the probes in complex shapes is also desirable. Shown in figure 6-4 is a demonstration model fabricated using the techniques described in the chapter 3. While this assembly is not a fully functional device, it does exhibit the flexibility inherent to the processes described in this thesis.
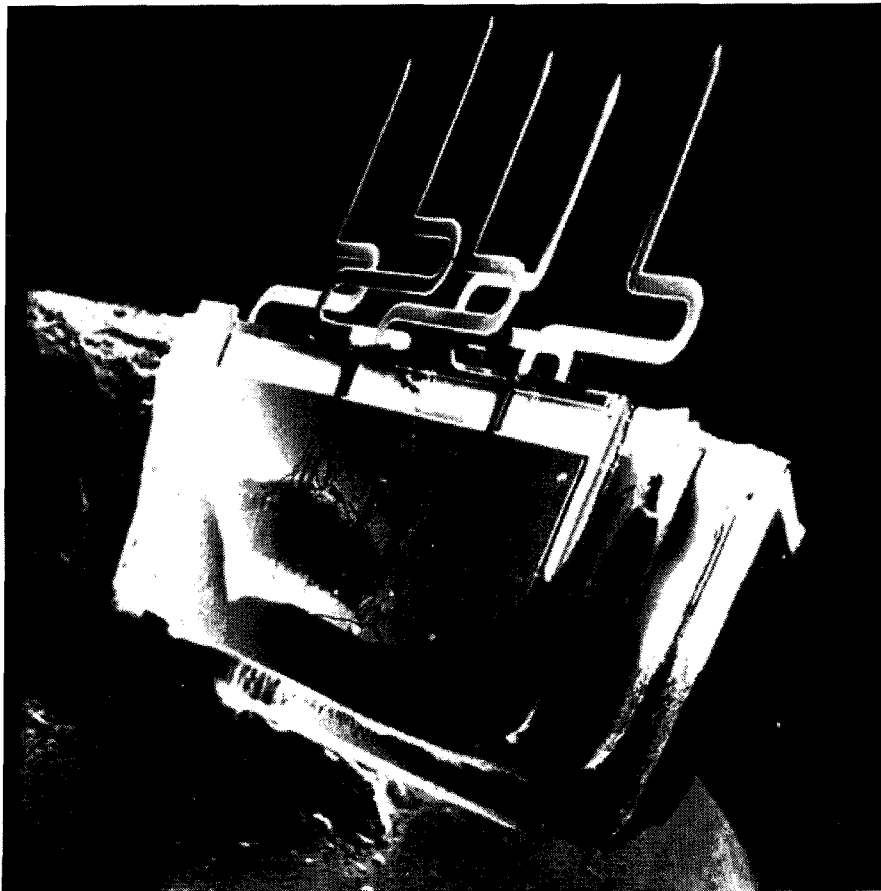


Figure 6-4: Three-dimensional array of neuroprobes incorporating a serpentine needle design. These probes do not have electrically connected neurowells. It was assembled from three, two-dimensional probes (up to three needles per handle) by stack and bonding the handles together. This demonstrates the flexibility with which the needles can be patterned as well as the ability to make 3D arrays.

## 6.2    Mechanical Strength Characterization

The unique application of the neuroprobes demands long and slender structures that are strong and stiff. Mechanically these requisites are counter to one another. In this instance, however, miniaturization is actually beneficial. Pearson, *et al.*, [54] reported that silicon structures with cross sections smaller than 2000 $\mu m^2$ have a maximum fracture strength which is six times larger than the fracture strength of bulk silicon. Mechanical bending experiments with fabricated neuroprobes have been conducted to investigate if this strength enhancing property is maintained when small through holes, such as neurowells, are introduced into such structures.

### 6.2.1   Physical Requirements

The neuroprobe must penetrate through several millimeters of brain tissue in order to position its active sites in the hippocampus of adult rats. This requires that the probe be strong enough to pass through the very tough protective layers surrounding the brain as well as several layers of brain tissue beneath. In doing so, it must induce minimal damage in those tissues. Otherwise, brain function may be seriously impaired. A long, very slender, probe design has been implemented for this purpose. With a total length of 4 mm, the 16 active sites are all located within approximately 1 mm from the tip. This permits the neuroprobe to pass through up to 3 mm of tissue and still position all of the implanted neurons within the targeted hippocampal structures. Width of the probe is set by the 16 electrode traces that must run the length of the silicon needle, along its back, to the probe handle. Using 4-micron wide leads set on an 8 micron pitch (or

spacing between trace edges of 4 microns) allows the needle to be just 150 microns wide.

The probe thickness is set by the neurowell design and is between 16 to 20 microns.

The mechanical strength, and especially the stiffness, of such a fine structure might be expected to be quite small. The above dimensions correspond to a wood plank that is 2 inches (5 cm) thick, 18 inches (46 cm) wide, and nearly 42 feet (12.7 m) long. Such a board would undoubtedly break under its own weight if lifted by one end. Silicon micromachined with such dimensions, however, results in a relatively rigid member. To determine the actual failure strengths of the probes, they were exposed to bending and buckling tests. Since influence of the neuron wells on the fragility of the probes was not clear, mechanical tests were carefully performed on probes with and without the microcavities etched in their tips.
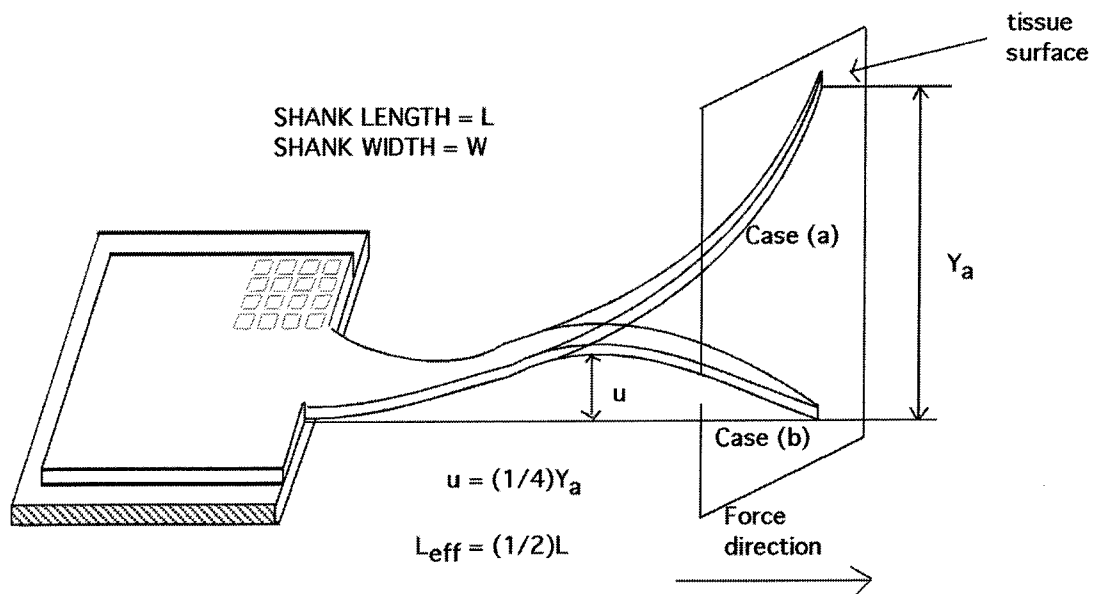


Figure 6-5:  Diagram of silicon probe needles under two deflection conditions: (1) the probe tip is allowed to freely move parallel to the surface of the tissue and bending occurs; and (b) the probe tip is pressed against the tissue and cannot slide resulting in buckling.

During the penetration of brain tissue, loading at the tip of the probe can induce two flexing profiles. The first is pure bending where the tip moves off axis and the length of the needle curves to form a simple arc roughly approximated by a quarter circle. The second case is that of buckling where the tip is pushed toward the handle along the axis of the probe. The center of the needle moves off axis forming a relatively complex, compound arc. Figure 6-5 presents a schematic illustrating these two types of deflections. The testing results of both conditions are presented in the sections below.

### 6.2.2 Theoretical Analysis

Solutions for the stress experienced by the slender members in both pure bending and buckling have been solved by a number of sources. The maximum and average stresses on the silicon needle of the probe in pure bending (at the base and center of the needle, respectively) are given by [70]:

$$\sigma_{max} = \frac{3\,tEy_A}{2\,L^2} \qquad\qquad \text{eqn. 6.1}$$

$$\sigma_{avg} = \frac{3\,Ey_A}{4\,L^2} \qquad\qquad \text{eqn. 6.2}$$

where:

t = needle thickness          E = modulus of elasticity of silicon

L = needle length            $y_A$ = maximum deflection of tip

These equations are easily calculated and can be used to predict the fracture point of the silicon probes. In the case of buckling, the more likely occurrence in most neural applications, such analytical solutions are much more complicated. However,

experimental measurements acquired by Najafi and Hetke [49] show that the above

equations still hold if an effective length, $L_{eff}$, is used in place of the actual length, L.

Their work gives $L_{eff} = 0.5$ L and results in the magnitude of tip deflection being reduced

by a factor of 4.

The fracture stress of silicon probes is a function of the cross sectional area of the

member. From figure 6-6, it can be seen that the fracture stress is approximately constant

for cross sections less than 2000 $\mu m^2$ at 1.75 x $10^{10}$ dynes/$cm^2$. As the cross section

increases, the fracture stress drops exponentially until the area surpasses 20,000 $\mu m^2$ and

it again approaches a constant value of 3.5 x $10^9$ dynes/$cm^2$, the same value attributed to

bulk silicon. These results suggest that to attain the maximum fracture strength, the cross

sectional area of the probe should be designed to be 2000 $\mu m^2$. For the neuroprobe, the

size of the target neurons sets the silicon needle to be from 16 to 20 microns thick. To

achieve the maximum fracture strength, the probe should be between 100 to 125 microns
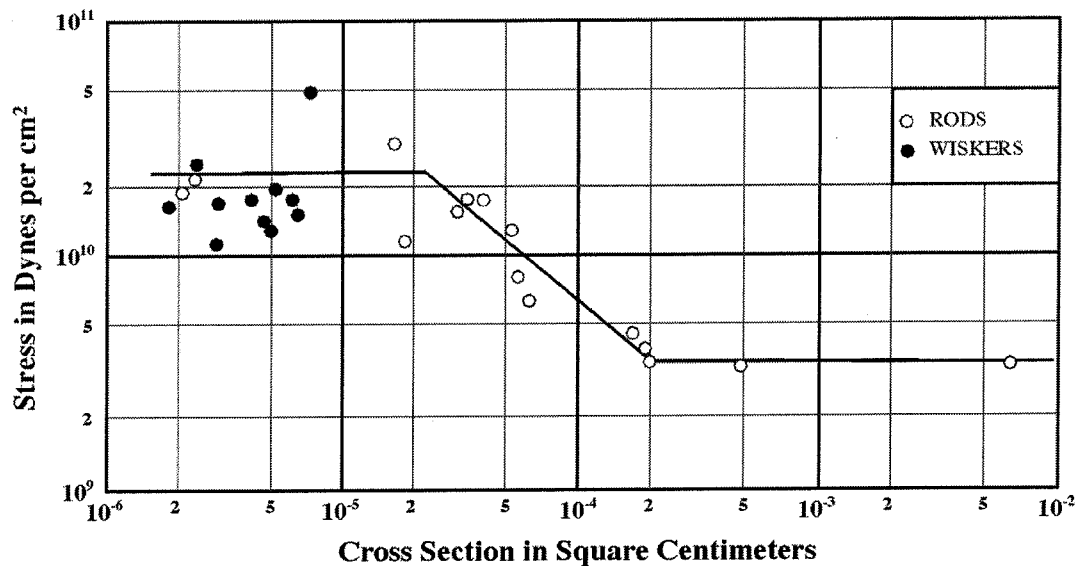


Figure 6-6: Effect of cross-sectional area on the room-temperature fracture strength of silicon rods and whiskers. Adapted from [54].

wide. At the present 150-micron width, the neuroprobes are estimated to have a fracture strength approximately 71% of the maximum value.

### 6.2.3   Bending Tests

The bending tests were performed on a static load-testing set-up assembled at Caltech (see figure 6-7). The instrument consists of a load cell to measure applied forces, a linear voltage differential transformer (LVDT) to measure z-displacement, and a solid surface against which the sample is pressed. The minimum force and displacement resolutions of this setup are 10 $\mu$N and 2.54 $\mu$m, respectively. The probe is mounted with its silicon needle orthogonal to the central axis of the load cell. A micrometer slowly raises this assembly into contact with an immovable pin such that the tip of the pin presses down 1 mm from the tip of the probe. Force as a function of load cell position, and thus probe deflection, is then recorded. A typical loading curve obtained with this
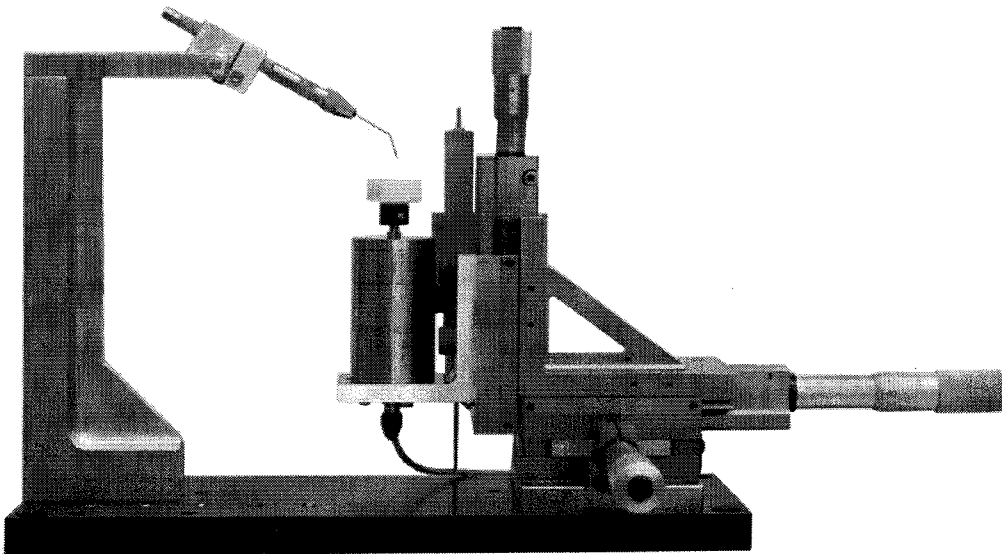


Figure 6-7:   Static load-deflection instrument used to acquire bending and buckling mechanical data from the probe needles.

procedure is shown in figure 6-8 and corresponds to bending stiffness of in the z-direction of 1.15 N/m.

The bending tests showed that the neuroprobe is very compliant in the z-direction. The picture in figure 6-9 was taken just before the probe broke. At this point, the tip of the probe is approximately 75° from horizontal. This is amazing when one considers common experience with brittle materials, such as glass, where even small deflections can result in catastrophic shattering.

In the bending test, at the point of failure, these values were:

$$t = 20 \text{ microns} = 0.002 \text{ cm} \qquad\qquad E = 1.9 \times 10^{12} \text{ dynes/cm}^2$$
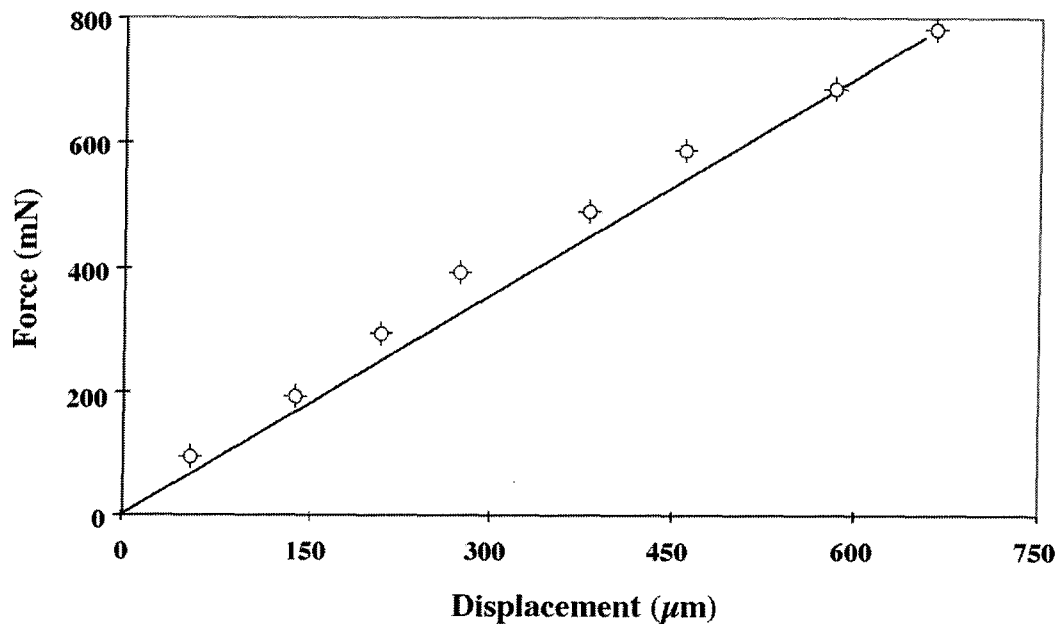


Figure 6-8: A typical loading curve for the needle of a cultured neuron probe. The probe is 4-mm long, 120-microns wide, and 20-microns thick.

$$L = 0.292 \text{ cm} \qquad\qquad\qquad y_A = 0.170 \text{ cm}$$

$$\Rightarrow \sigma_{avg} = 1.14 \times 10^{10} \text{ dynes/cm}^2$$

$$\Rightarrow \sigma_{avg} = 2.84 \times 10^{12} \text{ dynes/cm}^2$$

These numbers are in good agreement with the results reported in [54] and as can be seen in figure 6-6. It should be noted that this form of loading is expected to be rare during insertion into brain tissue. Bending requires that the tip of the probe be free to slide across the surface of the brain matter. In all likelihood, the spongy tissue will grip the tip and, if penetration does not occur, the force will project down the length of the needle causing buckling.
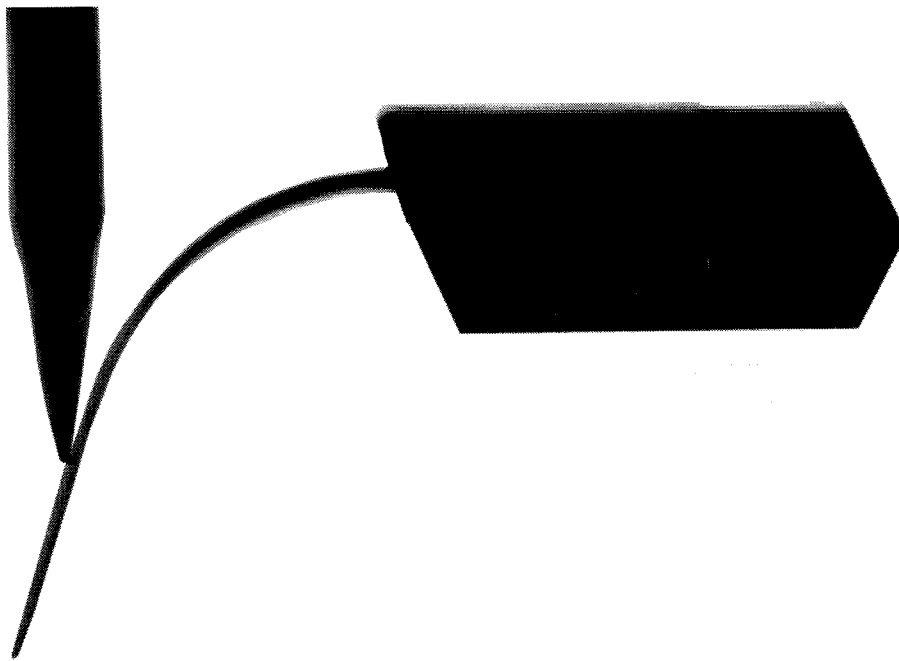


Figure 6-9: Photograph of the probe taken as bending data was being acquired. The flexibility of the silicon needle is quite dramatic showing it can withstand handling much more severe than it will ever see during actual use.

### 6.2.4  Buckling Tests

Using the same experimental setup used for the bending experiments, the buckling performance of the probes has also been measured.  As noted above, this is expected to be the most likely mode of deformation experienced by the devices during insertion.  The actual shape of a neuroprobe under buckling conditions in the testing apparatus is seen in figure 6-10.  Using the values of force and deflection of the needle just before breaking, the maximum stress is calculated as $8.7 \times 10^{12}$ dynes/cm$^2$.  The data presented in [49], and reproduced in table 6-1 suggests that the neuroprobes should easily survive insertion through the pia arachnoid and the dura layer surrounding the hippocampus of an adult rat.  To qualitatively confirm that the probes could survive such treatment, a single probes was repeatedly inserted into a portion of flank steak estimated to be at least as tough as brain matter.  The probe easily penetrated (N = 20) into the meat
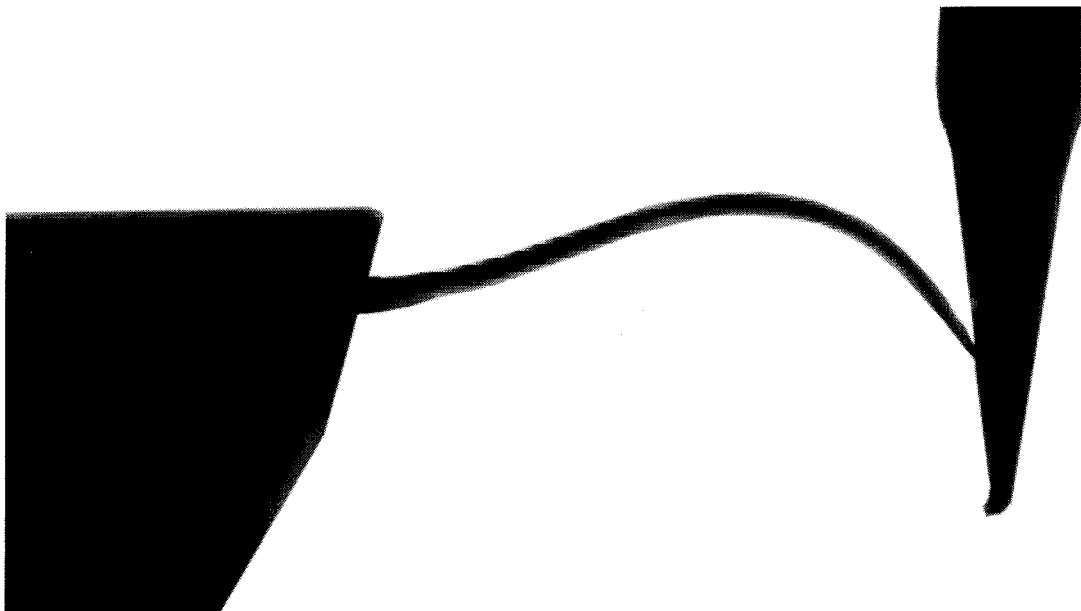


Figure 6-10:  The maximum buckling that the probe needle survived.  This photograph was taken just before fracture occurred.

to its full depth without breaking. Subsequent grilling and eating of said steak suggested it was, in fact, much tougher than the target tissues.

## 6.3  *In Vivo* Experimentation

The continued evolution of the neurowell structure precluded the timely fabrication of fully functional neuroprobes. For *in vivo* experimentation conducted in this work, devices denoted "dummy" probes were fabricated. Probes incorporating each generation of neurowell were fabricated. Several runs produced fully functional probes. Most runs, however, created dummy probes which are mechanically identical to true neuroprobes but do not have the integrated electrodes. As such, electrical stimulation and recording with these devices is not possible. The dummy probes allow mechanical functionality to be verified and allowed *in vivo* experimentation to proceed as the final

| Probe Thickness | Guinea Pig Pia Penetration Stress Dynes/cm$^2$ | Guinea Pig Dura Penetration Stress Dynes/cm$^2$ | Rat Pia Penetration Stress Dynes/cm$^2$ | Rat Dura Penetration Stress Dynes/cm$^2$ |
|---|---|---|---|---|
| 15 μm | $5 \times 10^8$ | $1.7 \times 10^{10}$ | | |
| 30 μm | small | $3.5 \times 10^8$ | $4 \times 10^8$ | $2 \times 10^8$ |
| 40 μm | small | $4.2 \times 10^8$ | $1.2 \times 10^7$ | $3.7 \times 10^8$ |
| 50 μm | small | $6.5 \times 10^8$ | | |

Table 6-1:  Maximum stress levels seen by different probes when penetrating guinea pig and rat pia arachnoid and dura layers. [49]

neurowell design was refined. In practice, the dummy probes demonstrated that neurons could be successfully cultured in linear neurowell arrays that, in turn, can be implanted into the central nervous system of a host animal. Functionality was determined by imaging brain slices for neural processes growing out from an implanted probe. The following details work which was done largely by collaborators at Rutgers University. It is included here for completeness.

### 6.3.1   Probe Implantation

The animal chosen for the *in vivo* experimentation are adult Sprague-Dawley rats. Prior to probe implantation, the brain is lesioned to enable subsequent imaging of implanted cells at the end of the experiment. The animals are first anesthetized with a mixture of 4 mg/kg of ketamine (25 mg/kg), xylazine (1.3 mg/kg) and acetopromazine (0.25 mg/kg). Once unconscious, the scalp is opened and the brain meninges removed by scissors. A cavity is made in both hemispheres by aspirating the medial portion of the parietal cortex and cingulate cortex (about a 2.0 mm gap), the cingulate bundle, the supracallosal stria, the corpus callosum, the dorsal fornix, the fimbria and the ventral hippocampal commissure. More commonly referred to as a fimbria-fornix or FF-lesion, this procedure assures complete denervation of the dorsal hippocampus from its subcortical inputs, including the medial septum. This can be visualized and quantified by the lack of acetylcholinesterase (AChE) positive fibers in the denervated hippocampus. The goal of this procedure is to remove all septal cholinergic fibers from the hippocampus and allow assessment of axonal outgrowth from cholinergic cells implanted

in a neuroprobe.  Subsequent to lesioning, the incisions are closed and the rats allowed to recover for one to four days.

Septal cells are implanted into the neurowells of the probe.  The surface of the probes are coated with 0.1% or 1.0% poly-L-lysine.  After placing the neurons into the wells, the probe is kept stationary for at least 60 minutes to allow the neurons to attach to the interior of their neurowells.  The neurons are cultured for 24 to 48 hours in an incubator in NBM/B27 medium as described in the *in vitro* culturing section of this thesis.

On the day of the implantation procedure, the probes are kept in tissue culture medium at room temperature.  While submerged in solution, the probes are inserted into a special holder.  A hole in the skull above the hippocampus is drilled and two stainless watch screws are driven into the parietal bone 2 mm in front and behind the hole.  Next, the dura mater is split using two microforceps under the surgical microscope.  The cell-loaded probe is inserted into a stereotaxic holder and lowered into the hippocampus.  The
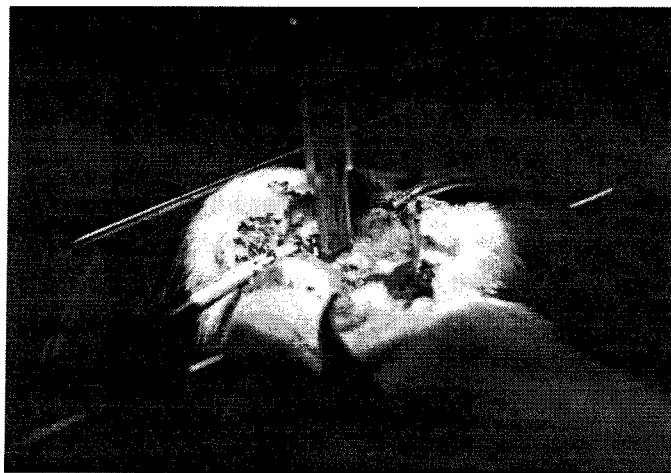


Figure 6-11:  Photograph of the surgical procedure used to implant a neuroprobe into the brain of a mature rat subject.

time elapsed between removing the probe from the tissue medium and inserting it into the brain does not exceed 2 minutes and is typically shorter than 1 minute. During insertion, special care is taken to avoid penetration through pial vessels. Figure 6-11 shows a photo at this point in the surgery. The handle area of the probe is fixed to the skull with dental acrylic. The rats are returned to their enclosure for 4 to 8 months to allow detectable innervation to occur.

## 6.3.2   Neural Process Outgrowth

Outgrowth or lack thereof, of neural processes from the neuroprobe cells into the surrounding living brain tissue can, unfortunately, only be verified by autopsy. The animals are deeply anesthetized and perfused through the heart with saline and ice-cold 4% paraformaldehyde (400 mL). The brains are removed and postfixed overnight in the perfusate. By Vibratome, 100-micron sections are sliced from the bulk tissue and stained



Figure 6-12:   Hippocampal slice into which a neuroprobe has been inserted (visible on the right) into the brain tissue, reaching down into the region of the hippocampus.

with the modified Koella process to reveal AChE-positive fibers. Care is taken to cut the slices in such a way that the probe, or at least a very large part of it, is contained in a single 100-micron section. Figure 6-12 shows a low magnification photo of such a section. The track left in the brain tissue by the probe can be readily seen transversing several cortical structures and penetrating into the hippocampus.

Higher magnification images, shown in figure 6-13, verify that outgrowth of neurons from the probes does occur. The dark, square region the left side of the photo is the end of the implanted probe. Extending from this area towards the right, dark lines can be readily seen. These are AChE stained neurites growing out as much as a millimeter from the probe into the surrounding tissue, one month after implantation.
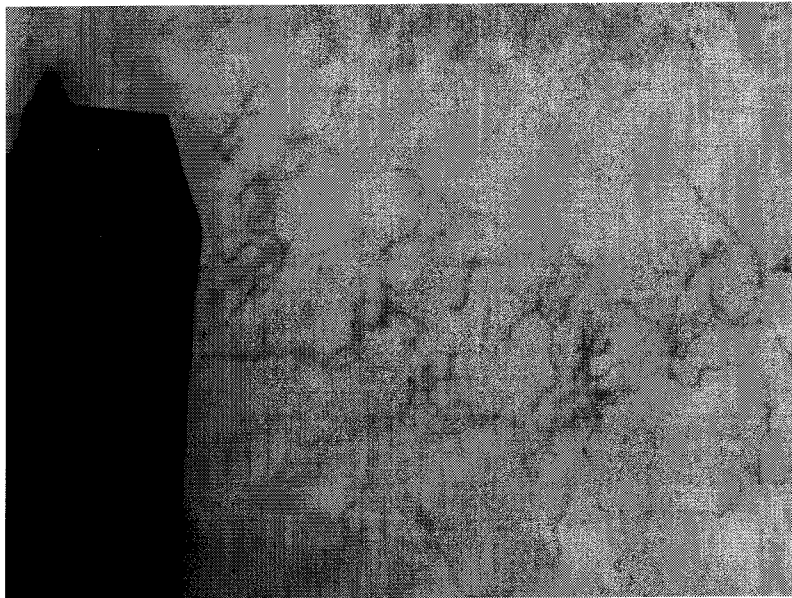


Figure 6-13: Image taken of stained neural processes growing out of a probe that had been implanted into a host animal for several months. Following autopsy, this section of brain containing the probe was Vibratomed into 50 to 200-micron thick slices then selectively stained to expose those processes coming from the neurowells. Significant outgrowth is seen with the neurites extending several hundred microns into the surrounding tissue.

## 6.4   *In Vivo* Experimentation Summary

The data acquired from the *in vivo* research should be viewed as qualitative only. Regular repeatability of these results has not been achieved. This is attributable to many factors including the many designs utilized, changes in cell culture techniques over the years, changes in personnel and the difficulty of the many steps involved. Still, sufficient confidence in the results allows several conclusions to be made. Neurons can be successfully cultured in neuroprobes which, in turn, can be successfully implanted into a living system. These neurons can extend axons and dendrites out into the host system while the cell body remain in close proximity to the probe. Finally, the distance these processes can travel and the high level of innervation imaged suggest the implanted neurons can thrive in the host body and potentially act as interconnects for future artificial, chronic neural interfaces.

**CHAPTER**

# 7

# NEURAL INTERFACES CONCLUSION

Through successive iterations in the design process, a new chronic neural interface system in which the cell bodies of rat hippocampal neurons are confined in a micromachined structure has been realized. The close proximity to an extracellular electrode enables recording from and stimulating of activity in individual cells in a culture. The research to date has laid the groundwork for this new family of neural interfaces. Future work to improve the manufacturability, to increase the number of neurowells in a given array, and to integrate on-chip electronics will lead to devices with much greater functionality. From the basis presented in this thesis, it is hoped that the neurochips and neuroprobes will evolve into tools that will help researcher unlock the intricacies of neural network formation and function, that they will open new avenues of

testing and qualifications of pharmaceuticals, and that they will enable doctors to restore neural functions to patients who have suffered nerve trauma or who were born with limited neural utility.

## 7.1   Summary

Neural interfaces micromachined from silicon and based on a single structure named a neurowell have been conceived, fabricated and tested. Grouped in linear, planar and three-dimensional arrays, the neurowells provide the means to contain, culture and electrically record and stimulate from living neural networks. This approach can significantly improve the signal-to-noise ratio characteristic of many of the typical devices presently used for extracellular stimulation and recording of neurons. Electrophysiological experiments have been conducted and the biocompatibility of the devices has been proven over periods of several weeks *in vitro*. In same experiments with implanted neurons, recording of spontaneous action potentials, recording of action potentials that are chemically and electrically triggered by an external probe, and stimulation action potentials using the electrodes in the neurowells have been demonstrated. Of equal importance, the growth of cultured neurons placed in neuroprobes that are in turn implanted in to the brains of host rats has also been confirmed.

In hippocampal cultures, the large number of processes present after one week of growth is consistent with observations of low-density cultures [13] and suggests that, at 2-3 weeks, significant connectivity exists between neurons in neurowells. The neurochip

is currently being used to map the synaptic connections of these neural networks. Future research will utilize such cultured networks to study the development, pharmacology, and activity dependence of the synaptic connections. Because of the non-invasive and specific bi-directional connections to every element of the network, the neurochip represents a powerful tool with which we will explore information processing in a mammalian neural network. It may also be an excellent system with which to test neural network and artificial intelligence theories.

Limited numbers of investigations have also been conducted with neurons from newborn rat superior cervical ganglion. Growth cones and processes from these peripheral neurons appear to be able to grow on the underside of the canopy and out through the central hole. Furthermore, the mature cell body volume overfills the neurowell, and mature processes are too large to fit inside the tunnels. Thus, these cells rarely remained in the neurowells beyond a week in culture. These results suggest that a single neurowell design is unlikely to be suitable for all neuron types. Each cell type must be tested in the existing designs, and the neurowells may have to be redesigned based upon the resulting growth.

## 7.2    Future Work

The detailed behavior of biological neural networks is extremely difficult to study owing to the inability to record simultaneously from more than a small fraction of the neurons in a culture or in a brain. With the neurochip system, it is now possible to follow all the elements of a small network. From the present 4 x 4 array, chips with a larger number of neurowells should be designed and fabricated. With this increase in size, more

automated loading and culturing techniques must be developed. With research well underway with the neurochips, a push to develop the neuroprobes should be initiated. Fabricating electronics in the same silicon used to form the neurowell structures will lead to implantable probes that do not require hard wired connections between the implanted devices and the external monitoring hardware. Ultimately, stand-along neural interfaces similar to the heart pacemakers of today could be realized in the future.

Scaling the neurochip technology to larger networks is relatively straightforward. For medium-sized arrays, i.e. up to 10 x 10 neurowells, the fabrication processes presented in this thesis can be readily employed. For larger arrays, say 100 x 100 neurowells, a moderate change to the processes is suggested. Chiefly, the fabrication procedure should be reworked to produce one-sided chips. This will eliminate the need to perform critical processes on large, thin, and fragile silicon membranes. Additionally, it will make possible the multiple layers of metal that will be needed to route the wiring from all of the wells to their recording and stimulation circuitry.

Large arrays will require on-chip electronics. For a 100 x 100 array of neurowells, running interconnects from each microcavity to its own bond pad and out to external electronics is not realistic. At a minimum, multiplexing circuitry will be needed. Adding pre-amps and a moderate level of data signal processing, while requiring a fair amount of work, should be able to be achieved with CMOS technology available from a number of silicon foundry services. Adding a serial interface and possibly an on-chip RF transceiver circuit will produce devices that are highly functional and require minimal knowledge of the end user.

The neurochip is envisioned primarily as a research tool with applications in the investigation of neural networks. Current views of neural network operation usually assume a set of oversimplified neurons, with fixed interconnections, that is searching for a minimum of some energy function (e.g. [36]). Although this approach shows promise, it is not yet known what properties are necessary to include in the modeling, or even what features are used by biological networks to convey information [37]. While the models can always be upgraded to include new features, neural network models need more information about biological networks. Neurochips with large arrays of neurowells will provide insight into cultured neural networks of a size that, to date, have been impossible to study with traditional techniques.

An exciting new area of *in vitro* pharmaceutical screening is made possible by the neurochip. Presently pharmaceuticals are tested by conducting long, complicated, and expensive animal trials. If successful, these investigations are followed by more testing in human subjects. The unknown safety risks, high monetary costs, animal and human rights issues, and long time frames associated with such testing makes an alternate solution very attractive to the drug industry. The neurochip is such a possible alternative. The ability to monitor neural networks electrically makes them readily applicable to long-term, automated testing. If the nominal state of a given network can be ascertained over the course of hours or days and stored, the deviation from this norm due to the application of a chemical agent could be determined. While unlikely to the present testing process described above, the neurochips can introduce an additional initial step in which any drug can be quickly and inexpensively tested without regard to the moral or

safety issues associated with animal research. Only those drugs found most likely to be successful in the standard trials will be advanced for further study.

The neuroprobe is presently being developed for long-term implantation into the brain of an adult rat. Embryonic neurons survive and apparently integrate into the adult brain [18, 67]. The neuroprobe thus has the potential to give a direct interface between a computer and an intact nervous system. This could allow restoration of lost neurological function, such as restoring the link between brain and muscle across a damaged spinal cord. Additionally, these neuro devices hold the potential to be able to create interfaces between man and machine. Motor cortex signals could be captured and used to control prosthetic devices. Vision systems might replace or enhance the human eye, driving the visual cortex directly. In several decades, it is not unreasonable to believe that chronic neural interfaces similar to the neuroprobe will also be used for more than the restoration of lost neural function. Bi-directional interfaces between the central nervous system and machines will open up an enormous number of possibilities for the enhancement of the natural abilities of man.

# CHAPTER
# 8

# INTRODUCTION TO MICROMACHINED MICRORELAYS

In recent years, interest in microrelays has been grown rapidly with particular attention being given to those devices that are fabricated using a micromachining approach. MEMS technology holds the promise of being able to batch fabricate microrelays, to simplify present production methods, to eliminate assembly, and to improve performance. In doing so and by doing so, smaller, less costly devices that have tighter tolerances, fewer parts, and lower power consumption can be realized. Manufacturers of the next generation, high-end electronic products require smaller and smaller subsystems for their designs. At the same time they are demanding that these modules be faster, better, and cheaper. A fully integrated MEMS microrelay can be batch-fabricated with many thousands of devices produced on a single substrate. Economies of scale hold the promise that the cost per microrelay will fall sharply once a process flow is finalized and put into production. All of the devices will be fabricated at the same time and require no individual component

assembly steps. The results will be microrelays with tighter part-to-part tolerances and less variable performance characteristics. The very fact that the MEMS devices can be single monolithic modules will decrease total part count to just one. This alone promises great improvements in overall reliability.

## 8.1  Electromechanical Relay Benefits

Perhaps one of the most common questions encountered in the course of this research has been "Why use relays?" Today, most circuit designers use transistors exclusively in their work and barely know what a mechanical relay is, let alone what benefits it provides. In a paper written in 1962 [91] this very topic is covered and in it the author discussed the future of the relay in a time when the transistor was just beginning to dominate. In the years since this paper was released, the ubiquitous use of transistors in nearly everything electrical has proven it to be the more flexible component. However, mechanical relays are still used widely throughout the electronics industry. They are most often found in those applications requiring true electrical isolation, inexpensive power switching, or the switching of high frequency signals.

Electromechanical relays offer the ability to create a physical break in a circuit that has minimal parasitic capacitance. By separating the wire, true electrical isolation can be achieved. This is extremely important in environments where sensitive electronics must be protected from high-level line transients. Inexpensive relays capable of withstanding thousands of volts across the open contact gap are readily available. Alternatively, in a

situation where very low level measurements are being made, the very high off-resistance (often $> 10^{12}$ $\Omega$) of a relay minimizes leakage currents that could make accurate readings impossible. When closed, the metal contacts provide very low on-resistance on the order of tens of milliohms. This results in minimal insertion loss in a typical application as well as the capability of passing relatively high currents. Transistors having, simultaneously, very high off-resistance, very low on-resistance, and a large current carrying capability are not readily available and those that can be purchased are very expensive. Finally, such transistors typically rely on large size and/or surface area to achieve these characteristics. The cost for this approach is high parasitic capacitance. In a properly designed mechanical relay, such parasitics are minimal.

## 8.2 Electromechanical Relay Drawbacks

Transistors have many benefits that are not matched by relays. Most notable is their near-infinite switching cycles lifetime. A second attractive feature is their high switching speeds. Because the transistor has no mechanical parts and there are no surfaces that must make and break, there are no components to wear out over time. Typically a transistor only fails when it is exposed to electrical conditions outside of its specified operating range. Relays, however, have lifetimes measured in, at most, hundreds of millions of cycles. As the moving parts have mass, they are limited to switching speeds on the order of several kilohertz. Transistors, in comparison, easily operate above a megahertz.

In addition to lifetime and speed, semiconductor devices can be batch fabricated

while historically relays have been produced by serial processes. Thus, only one relay may be produced at a time on the assembly line. The processes also involve many steps that require human intervention. In 1999 the soldering and assembly of many electromechanical relays still requires hands-on fabrication steps. In order to increase production efficiencies, manufacturers are attempting to use more automated production lines but the manufacturing process remains serial in nature. These automated lines are generally limited to relays that have a high volume of sales in order to justify the capital expense.

Because of the present production methods for electromechanical relays, their costs remain relatively fixed and the solid-state alternatives are becoming more attractive with each passing year. If relays could be batch fabricated they would become even more competitive allowing them to maintain and possibly gain market share. Micromachining technology is making this goal a reality while at the same time greatly reducing the size of the devices and potentially permitting circuits containing multiple relays to be produced in a single package. The result will be increased performance, greater reliability, and a larger target application set.

Two major types of devices encompass current electromechanical relay technology. These are reed and armature relays, both of which typically employ electromagnetic actuation. Both types of relays are briefly covered below as the micromachined microrelays presented in subsequent chapters are based on these macroscopic designs.

## 8.3 Reed Relays

Of the two kinds of relays, the reed type is the simplest. At the center of this device is a pair of magnetic blades, or reeds, whose tips overlap one another and are separated by a small air gap. These tips are usually coated with a special contact metal to improve the switching performance of the device. The two reeds are hermetically sealed inside a glass cylinder that is typically filled with a special gas mixture that minimizes arcing and metal oxidation. A coil with a large number of windings then wraps this assembly to produce the final relay. Such a device is shown schematically in figure 8.1.

Actuation of the blades in the reed relay is achieved by energizing the coil. This generates magnetic flux along the central axis that magnetizes the reeds and causes them to attract one another. The air gap and blade overlap area are designed so that sufficient force is produced to create a wiping action of the two contacts over one another allowing clean, low-resistance making to occur during each switching cycle. Because of this design, the mechanical and magnetic forces present in a reed relay are closely coupled. Larger forces are generated on thicker blades but at the same time, thicker blades require larger bending
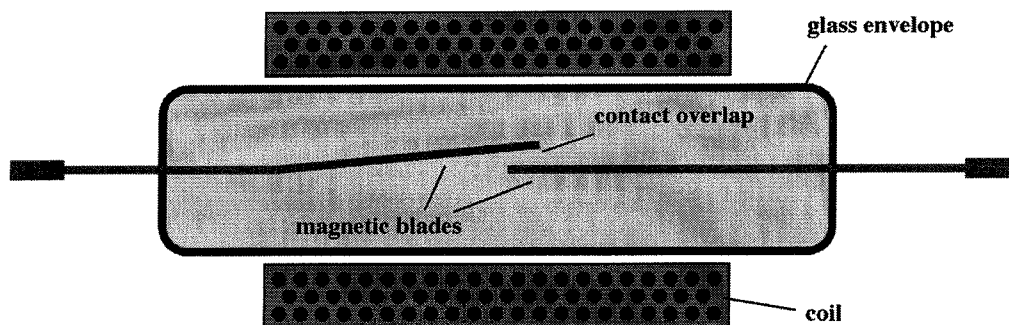
Figure 8.1: Realization of a reed relay by wrapping a reed contact with a coil. Contacts are shown in the normally open configuration.

forces to close the contacts. Because the reeds must be made of a magnetic material, they are typically more resistive than could be realized by using a metal such as copper. Still, with proper design, reed relays can function very well and are some of the most reliable relays available on the market.

The main drawback of reed relays is that they are sensitive to external magnetic fields. As an example, many applications use the movement of a permanent magnet rather than a coil to activate the devices. In such an implementation, reed relays can perform very nicely as interlock safeties and control inputs. In a circuit application, this type of sensitivity to external magnetic fields is undesirable. The fields produced by adjacent relays are typically the greatest concern, as they may cause undesired switching to occur. This is mainly due to the fact that outside the coil there is no defined return flux path for the magnetic field to follow. In applications that require close device spacing, reed relays are typically packaged with additional magnetic elements that guide fringing fields away from the ferrous blades.

The minimum size of a reed relay is set mainly by the tolerances that can be achieved during manufacture. The smaller the device, the smaller the gap between blades that must be used and the tighter the tolerance that must be held from relay to relay. The gap is set by a machine that holds the two reeds while the glass cylinder is sealed. Smaller and smaller dimensions require more and more capable, and thus more and more expensive assembly equipment. At present, components called microminiature or ultra-miniature reed relays are available with minimum glass dimensions reported as 0.8 mm in diameter and

3.6 mm long [158]. When the electromagnetic coil and packaging is added, the realized final dimensions are at least twice this size. One product by Coto Wabash measures 9.525 x 4.953 x 4.699 mm, can switch up to 0.25 A (3 W contact rating), is rated for 100 million operations at 1 V and 1 mA, and has a off-resistance of at least $1 \times 10^{10}$ $\Omega$ at 100 VDC. Devices of this type find the greatest amount of use in automatic test equipment where their ability to efficiently pass RF signals in the GHz range and their stable contact resistance over their rated life are requirements of the application.

## 8.4  Conventional Armature Relays

Armature relays are used in more general type applications as compared to reed relays. The layout and operation of such devices are covered in depth in chapter 14. Designs exists which are capable of passing low level signals as well as switching very high power loads. Typically the larger the armature relay, the higher the current and voltage rating that it has. In recent years, end users have been demanding smaller and smaller devices with ratings similar to those found for reed relays and many conventional armature relay manufacturers have been working to supply such components [90, 113, 124, 144].

Key to the push for miniaturization is the desire for relays to no longer be exotic components on surface mount (SMD) printed circuit boards. For components taller than 6 mm, special tooling must be used to place them on an SMD board. As such, a push to the next generation sized device has led to a number of commercially available devices that have dimensions on the order of 9 x 5 x 5 mm [113, 144]. These products are still

manufactured in the traditional serial manner with each new generation utilizing automated equipment to a greater and greater extent. While this has allowed miniaturization to proceed, it raises production costs and limits the type of relays that can be shrunk with this approach to those which can be sold in very high volumes.

## 8.5  Previously Reported Micromachined Microrelays

Activity towards the development of a MEMS microrelay was reported as early as the 70's, but only in the last 5 years have devices been developed that have performance capabilities that are suitable for the commercial market. Initial work used electrostatic forces for contact make and break and are to be considered more as proof-of-concept devices rather than attempts to produce commercial quality products. Electrostatic actuation is attractive as such devices are very simple to fabricate. The same processes used by CMOS circuit manufacturers can be utilized unaltered. Electromagnetic microrelays have not been widely researched due to their much greater complexity and their requirements for high quality ferrous materials. In general, magnetic MEMS is in its infancy at the present time and is being pursued by only a handful of groups worldwide. The last major type of microrelay is based around thermal actuation. This approach has proven to be the "winner" in the first-to-market race for a fully micromachined switching device.

### 8.5.1 Electrostatically Actuated Micromachined Microrelays

Electrostatic forces are by far the most popular mode of actuation in the micromachining community. This stems largely from the fact that this approach can be

realized with conventional CMOS fabrication technology and requires no modifications or special additions to such processes. To create such a device, all that is required are two conducting plates in close proximity to one another. This can be achieved by laying one plate of material over another with a small gap between them (parallel plate actuator) or by patterning a single layer of material into an interlacing finger geometry. The latter approach is the more popular and the device produced is commonly referred to as a comb actuator. The basic theory and analysis of such actuators is covered well in [146].    Parallel    plate devices are used less frequently in MEMS generally but is more popular in microrelay designs due to its simplicity and larger realized forces per unit area. As such, it deserves some derivation here. The analysis begins with an expression for the capacitance of two parallel plates which is simply [127]:

$$C = \frac{\varepsilon A}{d}$$ 
<div align="right">eqn. 8.1</div>

where $\varepsilon$ is the permittivity of the gap, A is the area of the parallel plates, and d is the distance separating the two plates. Generally, the permittivity of the gap in a parallel plate actuator is just that of free space or $\varepsilon_0$. The potential energy across two such plates when a voltage, V, is applied across them is given by [127]:

$$E_{cap} = \frac{1}{2} CV^2 = \frac{1}{2} V^2 \frac{\varepsilon_0 A}{d}$$ 
<div align="right">eqn. 8.2</div>

The force generated between the two plates is simply the partial derivative of this energy taken with respect to the direction of motion. For a comb actuator, this would be in the x and y directions (where A is a function of x and y.) In the case of a parallel plate, the motion is in the z direction and is such that it increases or decreases the value of d. Differentiating equation 8.2 with respect to z gives:

$$F_{elec} = \frac{\partial E_{cap}}{\partial z} = -\frac{1}{2}V^2 \frac{\varepsilon_0 A}{d^2} \qquad \text{eqn. 8.3}$$

It is useful to compare this force equation to the equation that describes the forces generated by a traditional electromagnetic actuator. The derivation included in chapter 14 produces the following equation:

$$F_{mag} = -\frac{1}{2}(NI_o)^2 \frac{\mu_o A}{d^2} \qquad \text{eqn. 8.4}$$

Here, $NI_o$ is the ampere-turns in the device and $\mu_o$ is the permeability of free space. All other variables are the same as in equation 8.3. Taking the ratio of the two forces, assuming the same values for gap area and gap distance in the equations, gives:

$$\frac{F_{mag}}{F_{elec}} = \frac{-\frac{1}{2}(NI_o)^2 \frac{\mu_o A}{d^2}}{-\frac{1}{2}V^2 \frac{\varepsilon_0 A}{d^2}} = \frac{\mu_o (NI_o)^2}{\varepsilon_0 V^2} = 1.42x10^5 \frac{(NI_o)^2}{V^2} \qquad \text{eqn. 8.5}$$

Here, the five orders of magnitude difference between the value of the permeability ($4\pi$ x $10^{-7}$) and the permittivity ($8.85$ x $10^{-12}$) of free space results in much larger magnetic forces. To see the true difference between realistic devices, some practical numbers should be introduced. Namely, voltages higher than 100 volts and currents above 0.5 A are undesirable in most applications. Substituting these numbers into equation 8.5 gives:

$$\frac{F_{mag}}{F_{elec}} = 1.42x10^5 \frac{(0.5)^2}{(100)^2} N^2 = 3.55N^2 \qquad \text{eqn. 8.6}$$

So even for a single turn electromagnetic device, the forces it generates is 3.55 times that of the same sized electrostatic actuator. This larger force translates into electromagnetic relays being able to utilize larger contact gaps and being able to produce higher contact forces.

In choosing one actuator type over the other, additional points that need to be considered are ease of manufacture and operating power requirements. In both these aspects, the electrostatic actuator is the winner. The fabrication of a parallel plate capacitor is very straightforward. The only major consideration is what sacrificial material will define the gap distance and how will it be removed at the end of the process. For an electromagnetic device, wrapping a many-turn coil around a magnetic core is much more difficult. Likewise, in operation the electromagnetic relay draws constant current when on, resulting in substantial power dissipation. Electrostatic actuators draw power only for the brief time required to change between the off and on, on and off states. In a practical application the amount of power consumed is negligible.

A fair number of MEMS microrelays have been reported.  Typically actuation voltages are in the range of 100 volts.  The first reported microrelay [128] used gold contacts and achieved a contact resistance of 5 $\Omega$ and a switching speed of 10 $\mu$sec with a typical 70 V actuation voltage.  More recently, Gretillat [100, 101] has published results for polysilicon electrostatic microrelays with current carrying capabilities on the order of 10 mA at control voltages of approximately 40 V (DC offset plus driving voltage).  These devices switch up to 100 kHz and have been demonstrated to have lifetimes in excess of $10^9$ operations.  A number of other microrelays have been reported with similar or lesser capabilities [95, 130, 132, 133, 157].  More recent electrostatic devices have achieved greater performance levels.  In [134], a device capable of switching currents up to 200 mA with actuation voltages of less than 24 V is reported.  Still, for all the work that has conducted on this type of relay, such devices have yet to be made commercially available.

## 8.5.2 Electromagnetically Actuated Micromachined Microrelays

As noted above, electromagnetic actuation holds the promise of larger forces and larger gap sizes for devices of similar size.  The higher power draw is often not a concern in many applications while the high voltages demanded by electrostatic microrelays are troublesome.  Examples include automatic test equipment (ATEs) for integrated circuits and automotive applications.  High currents are easily produced in these environments but high voltages either require voltage converters or are deemed unsafe.   Electromagnetic microrelays are widely used in these situations.

The majority of previously reported magnetic microrelays have not been fully integrated devices. Large, on the scale of micromachined components, relays have been made which use hand-wound, external electromagnets as their source of actuation force [107, 108]. Others micromachine the coil with a magnetic core and add an armature with contact points at the end of the process [113, 150]. The use of external components or the requirement of final assembly steps limits the minimum size of the microrelays that can be produced. Additionally, many of the benefits and cost savings that could be realized by a fully integrated process are lost when this hybrid approach is used. An attractive aspect of this method, however, is that it allows the relay industry to slowly introduce micromachining technologies into their factories and their product lines can evolve over many years rather than change radically in a single generation. Devices based on the external coil approach have been able to achieve contact resistances between 100 m$\Omega$ and 150 m$\Omega$ [108]. Those produced with micromachined coils have been reported to have performance characteristic very similar to commercially available relays rated for 1 to 2 ampere switching [113].

To date, it is believed that only three groups have reported fully integrated electromagnetic microrelays. The first was fabricated using a LIGA process but the only performance information provided was its ability to switch 1 mA between the contacts and that an estimated 250 mN of forces is generated when 1 A is applied to the coil. Much more complete data were provided by Taylor, et. al [84, 147-149] who produced a magnetic microrelay with a very novel geometry. On-resistances for Au-to-Au contacts are reported to be as low as 22.4 m$\Omega$ and switch up to 150 mA with coil powers of 320 mW.

Using other contact materials, hot-switching up to 1.2 A with 3 VDC across the gap has been demonstrated. At lower levels, lifetimes in excess of 1 million cycles were realized with operation frequencies on the order of 1 kHz. The third group producing fully integrated magnetic microrelays is Caltech and is the subject of this thesis.

### 8.5.3 Electrothermally Actuated Micromachined Microrelays

Several groups have produced microrelays based on thermal actuation with varying levels of success. The use of thermally controlled actuation scheme results in relatively large forces, but will tend to increase the switching time. In one reported device [138], a polysilicon heater is placed on top of a $SiO_2$-$Si$-$SiO_2$, clamped beam and deflections on the order of 40 microns are realized with an input voltage of about 45 V and operate times of 5 msec. A force of 19.6 mN with a 25-micron deflection is reported for an actuation-input power of 675 mW (27 V, 25 mA). No contact ratings are given.

Perhaps the most successful thermal design has been produced by MCNC, now Chronos Integrated Microsystems. They have made commercially available a fully integrated MEMS microrelay that utilizes thermal actuation. The data sheet for these devices with Ni-to-Au contacts states that they can switch up to 300 mA at 10 V or 10 mA at 70 V. Switching times are 8 msec although the maximum witching frequency is rated at 30 Hz. Lifetime at 10 mA/ 10 V is given as 4 million cycles. It is believed that this is the first micromachined relay ever to be sold in commercial quantities.

## 8.6   Research Objectives

The objective of this research is to combine through-wafer 3-D micromachining techniques with other low temperature processing steps to produce two families of magnetically actuated microrelays.  The fabrication processes used are designed to be compatible with starting silicon substrates containing CMOS circuitry.  The batch fabrication possible with the micromachining approach is in sharp contrast to the serial process typically used in the production of electromechanical relays.  Of particular interest is the possibility of producing large arrays of relays that are pre-wired for specific functions.  All design, testing, and characterization of the devices is conducted in the Caltech micromachining lab.  One family of microrelays is targeted specifically for the commutation of DC brushless motors.  It is also designed in such a manner as to allow it to be a testing platform for a variety of contact materials.  The second family of devices is of a more general type that can be operated by a single control signal and should have many applications in low level and RF signal switching.

# CHAPTER
# 9

# MICROMACHINING PROCESSES FOR MICRORELAY FABRICATION

In the world of micromachining, many different materials are employed to fabricate

a wide range of MEMS devices. Early work used polysilicon and bulk single crystal

silicon as the structural material [96, 109, 122, 129, 143]. In the case of relays, however,

the relatively low electrical conductance of these materials is unsatisfactory. Contacts

formed from polysilicon have been reported to produce resistances on the order of 10 kΩ

which greatly limits their usefulness [100, 101]. As discussed in chapter 10, metal

contacts are required to achieve high performance switching. Save for relatively thin

interconnects, metal has not been heavily used in the fabrication of MEMS devices. Only

in recent years have a select few groups begun to explore the potential of metal structures.

The majority of the devices that have been reported are either surface micromachined in an

integrated process [83, 126, 149] or assembled from discrete components using a process

called LIGA [102, 103].

In addition to using metal as a structural material, several additional technologies must be implemented to fabricate MEMS microrelays. Key to proper actuation performance is the ability to lay down relatively thick, highly permeable layers of magnetic material. Targeted for this work is an alloy of nickel and iron commonly referred to as permalloy. Electrical insulation must be placed between the multiple metal layers to avoid shorting between the coil and the magnetic circuit. Due to the effect of high temperatures on permalloy films, the insulation must be deposited at low temperatures or prior to the formation of the magnetic circuit. To create freestanding structures, surface micromachining requires the use of a sacrificial material. The conditions in which the material is laid down and method in which it is removed must be compatible with metal films. Finally, the ability to create through holes in the substrate wafer is desirable. This allows devices with smaller effective footprints to be produced as well as improves the performance of the realized magnetic circuit. While several of these processes are well established, others were developed in the course of this research.

## 9.1 Photoresist Mold Electroplating

Thick, high aspect ratio metal structures that are closely spaced cannot be attained through standard patterning processes. The dominant methods of metal definition are liftoff and wet, isotropic etching. Liftoff requires a highly directional deposition process, such as evaporation, and is typically limited to patterning films less than 1 micron thick. As such this technique cannot be used to define thick, electrodeposits. Isotropic wet

etchants remove material in the sideways direction at the same rate at which they etch down. This limits the minimum spacing possible between two given structures to twice the total thickness of the metal being patterned. Such a constraint makes this an impractical approach. Some directional, anisotropic patterning of metal is available in the form of ion milling and sputter-etch. These use high energy, high momentum ion bombardment to physically and chemically remove unprotected areas on a substrate. However, these processes are only suitable to removing thin ($< 1000$ Å) layers of material. Patterning tens of microns of metal in this way is not practical.

### 9.1.1 Electroplating Fundamentals

Electroplating or electrodeposition is a process in which metal ions can be deposited onto a conductive surface from a liquid solution. Used widely in industry, layers tens of microns thick can be quickly formed using inexpensive chemical and a simple deposition system. A wide range of pure metals and metal alloys can be easily plated. The physics of electrodeposition is well established and is covered well in [89]. In simple terms, current in the form of ions passes from an anode to a cathode through an electrolyte. Upon reaching the cathode, the current-forming ions deposit on the conducting surface and over time build up a solid film. Proper selection of the chemicals added to the bath can permit a wide range of pure metals, as well as alloys, to be plated. If an insulating material covers areas of the cathode, no deposition will take place. This principle forms the basis of selective electroplating using photoresist as a mold material.

## 9.1.2 Photoresist as a Mold Material

Electrodepositing material up through a patterned insulating mold is the best means to form the thick, closely spaced structures required in the MEMS microrelays. For this work, photoresist is the chosen mold material. AZ 4400 and AZ 4620 positive resists made by Clariant [74] are used predominantly as they can produce up to 10-micron layers in a single spin application and up to 50 microns in multiple spins. The resists can be exposed with standard contact, proximity, or projection UV systems, have good thermal stability (within their operating range) and are developed by solutions that do not attack the materials present in the microrelays. Wafer coating and resist patterning is performed using standard processes. After developing, the photoresist may be used directly as a plating mold or it can be hardbaked to reflow sharp corners prior to electodeposition steps. After the metal has filled the resist-free regions, the photoresist is easily removed using a global UV exposure and a second developing. This is found to be superior to the alternate techniques that include stripping with acetone and oxygen plasma ashing. The former approach tends to leave troublesome residue on the wafer while the later is very slow and will oxidize any copper features that are exposed.

Photoresist compatibility with a given plating bath must be assessed prior to use in the fabrication of a micromachined device. Most positive photoresists are developed in a high-pH or alkaline solution (typically dilute KOH or NaOH) and are designed to be chemically resistant to low-pH chemicals [131]. In general, a plating bath with pH in excess of 8.0 is not compatible with a positive resist mold. It is preferably to choose a

solution with a pH that is less than 6.0 to minimize problems. Other factors that may preclude the use of positive resist in plating are excessive hydrogen formation during deposition and the presence of cyanide in the bath. Atomic hydrogen aggressively attacks resist and quickly degrades the polymer to the point where a high density of cracks forms in the mold material. While most cyanide baths also have high pH levels, some solutions at lower pH are available. The actual mechanism that causes the resist to degrade in such baths has not been investigated in this work but incompatibility with AZ brand resists has been verified. The plating solutions used in this research are all acidic baths. The permalloy solution is maintained at a pH of $2.70 \pm 0.03$, the copper solution is essentially a dilute sulfuric acid bath, and the gold solution is kept at a pH of approximately 4.5.

### 9.1.3 Electroplating Seedlayers

The surface of the substrates used in micromachining must be highly conductive in order for features to be plated. Referred to as a seedlayer, a thin metal layer is deposited globally across the face of the wafer to serve as the cathode in the plating system. For this research, both copper and gold have been regularly used and are laid down in a thermal evaporation system at a thicknesses of approximately 1000 Å. Adhesion of these metals to the many surfaces that can be exposed on a micromachined device is typically not good. To enhance seedlayer adherence, a very thin adhesion layer (100 Å) of chrome or titanium is deposited prior to the thicker seedlayer-metal evaporation. This is done without breaking the vacuum used in the evaporating system to ensure no oxide forms on the Cr or Ti.

In general, chrome is the better adhesion material and is used whenever possible. In certain cases, removal of the chrome becomes difficult. This is particularly noticeable when it is in direct contact with copper and is heated to temperatures greater than 150 °C or exposed to a gas plasma. These conditions are believed to form a very chemically resistant oxide layer and/or chrome-copper alloy though no investigations have been conducted to confirm this. For steps where subsequent processing will expose a seedlayer to the aforementioned conditions, titanium is used in place of chrome. Overall the four metals used to form the seedlayers are easily patterned and provide a good surface from which to electroplate all the metals used in the MEMS microrelays.

## 9.1.4 Selective Seedlayer Patterning

The underlying seedlayer covering the entire surface of the wafer must be patterned. This can be done in several manners and at a number of points in the electroplating process. The most straightforward method is to globally etch the seedlayer after plating and after removal of the mold photoresist. When plating large, simple structures, the seedlayer can be pre-patterned with electrical connections running from each feature to the pad frame left in place. If very fine features are being formed and maintaining a high level of planarization is important, the seedlayer can be evaporated over a permanent pre-mold and then the temporary plating mold can be deposited. The benefits and limitations of each of these approaches are covered in the following paragraphs.

The very thin seedlayer can often be removed by isotropic wet etching following the

plating of thick features.  Since the etching time required is very short, even if the etchant does attack the plated features, the amount of material removed is negligible.  The thick, plated features actually act as a mask for the seedlayer patterning.  This approach does require that the photoresist mold be removed after plating raising issues of surface planarity.  If planarization is not a concern, this technique is quick and simple though it is prudent to use heavily diluted etchants.  Aggressively removing the seedlayer, especially the adhesion metal, can often result in liftoff of the plated features.  A much slower, more controllable etch produces superior results.

In some cases, leaving the photoresist in place is desirable.  The nature of mold plating tends to produce a reasonably smooth, self planarized layer after the deposition is completed.  Heating to the reflow temperature further smoothes out the surface and if photoresist peaks still rise above the plated structures, the can be removed with an oxygen plasma etch.  Leaving the mold in place, however, requires that the seedlayer be patterned prior to plating.  For large structures, where fine traces leading from the features to the pad frame are permissible, pre-patterning of the seedlayer can be done.  The interconnecting traces can be stripped by etchant in a final step (if subsequent processing has or can expose them) or they can be severed during wafer dicing.  For the situations where fine-conducting leads cannot be used, a layer of photoresist can be spun, patterned with the plating mold mask, and hardbaked.  The seedlayer is then evaporated and covered by a soft baked resist, again patterned with the plating mold mask.  Metal can then be electrodeposited, the softbaked mold removed and the seedlayer stripped.  The first layer of hardbaked resist

remains in place acting as a permanent structural material that maintains relatively good planarity.

In patterning the seedlayer, wet etching is most often used though a directional, dry strip is sometimes preferred. As noted above, aggressive removal of the seedlayer can often result in liftoff of the plated features. This is particularly true when very fine (< 5 micron), yet thick traces have been plated. Most common during the removal of the adhesion layer, etching of the interface between the plated metal and the seedlayer or between the seedlayer and the substrate can occur much more rapidly than the etching of the seedlayer itself. This may be due to the presence of an easily etched oxide at these interfaces. Another possibility is that strain energy present at the interface may be being transferred into the chemical reaction [152]. In either case, a wet etch sometimes does not work.

In place of the wet etching, ion milling or sputter etching can be used. These processes strip material layers from those surfaces facing the ion source. This means that sideways etching is negligible especially when a vertical layer only 1000 Å thick is being removed. These techniques rely more on physical bombardment ablation rather than chemical reactions at the surface and so can be used to strip nearly any material. For fine, thick features, this is the preferred approach.

## 9.1.5 Mold Plating Used in This Work

All three modes of mold plating have been used in the course of this research. Each

delivers satisfactory results for the various micromachining processes in which they have been used. Wet etching is used predominately to pattern the seedlayer. Ion milling and sputter etch have be tested to show that they can adequately remove material at the bottom of deep, narrow trenches. In practice, the slight improvement in performance that the dry processes provided was negated by the added time and expense associated with them. The minimum feature size of approximately 10 microns used in the microrelays permits adequate performance of the wet etchants.

## 9.2   Electrodeposited Metals

The materials used to produce most of the structures in the microrelays presented in this thesis are formed from electrodeposited metals. Also know as electroplating, this technique of laying down metal from a liquid is very powerful. Key for this work is its ability to deposit very thick, in micromachining terms, metal layer. A large range elemental and alloyed films can be realized through electrodeposition with copper, gold, solder and permalloy ($Ni_{80}Fe_{20}$) being used extensively in the development of the microrelays discussed in this work. The properties of the plated films are discussed in the following sections and processing limitations considered.

### 9.2.1 Copper, Gold, Rhodium and Solder

The plating of copper and gold is used extensively in both microrelays developed in the course of this research. To a lesser extent, rhodium and solder have also be used. In

the case of copper, a simple copper sulfate and sulfuric acid bath is used with great success. No maintenance, other than cleanliness is needed. While the surface roughness is not negligible at approximately 1000 to 2000 Å RMS per micron plated it is adequate for this work. The realized stress is not problematic unless the films are exposed to high temperatures. Deposition thicker than 100 microns have been successfully plated onto silicon substrates. The recipe for the copper plating bath is given in appendix R1.

The baths for gold, rhodium and solder were purchased from commercial suppliers. Experiments with a number of different solutions have been performed with those from Technics seeming, overall, to give the best results with the least hastles. The particular information on these solutions is given in appendix R1.

The plating system these metals can be as simple as a beaker or as complicated as the agitation tank used for permalloy (see section 9.2.3). In the case of beaker plating, a four liter reflux system is set up on a temperature controlled hot plate. For gold plating, a temperature of 55 °C is required to attain good films. Due to the poor leveling characteristics of the copper solution, a plating system like that used for permalloy is employed. Since the application of a magnetice field during plating has no affect on the quality of this plated metal, the large permanent magnet is not included in the copper plating tank. It should be noted for all the plating systems, the most frequent cause of plating problems is cross contaminations between the baths. For this reason, a separate plating system is dedicated to each of the metals used in the fabrication of the microrelays.

## 9.2.2 Permalloy

Key to the successful fabrication of functional microrelays is the ability to deposit thick, high quality magnetic films. Electroplating is the chosen method for depositing such layers in this work. When choosing the magnetic material to plate, the ability to control compositional uniformity throughout thickness and to achieve high saturation magnetizations are the most important issues that must be considered. Secondary, but still important considerations, is the compatibility of the plating bath with photoresist and the internal stress levels in the deposited films. A search of the available literature led to the decision to form the magnetic circuit of the relay from plated permalloy, a composite of nickel and iron have an approximately 80:20 ratio, respectively, of the two constituent materials.

Permalloy is a soft magnetic material that will saturate when exposed to relatively low external magnetic fields. This corresponds to it having a large permeability constant. In the films plated for this work, relative permeabilities as high as 5000 have been achieved (number not corrected for demagnetization). Values greater than 1000 (not corrected for demagnetization) are regularly attained for films patterned for use as microrelay structures. These films have a saturation magnetization from 0.8 to 1.0 Tesla.

The recipe for mixing the permalloy plating bath solution is given in appendix R1. In addition to the chemicals that provide the nickel and iron ions that form the deposit, several other compounds are found in the bath. In alloy plating, the composition of the plated material depends on the ratio of the reducible cations in the area near the cathode

(also know as the depletion region). In the case of permalloy plating, nickel is less readily reduced than iron. This requires a higher nickel-to-iron ion ratio then would be initially expected to attain an 80:20 blend in the deposited film.

To improve the deposition conditions in the bath, anions are introduced into the solution. These include sulfamate to reduce the hydrogen evolution and to increase deposition efficiency at high current levels. The tank used in this research employs a pure nickel anode that is dissolved at the same rate that nickel is deposited at the cathode. This decomposition process is aided by the chloride ions present in the bath.

A number of other additives are used to condition the plating solution and to control the stress in the deposited permalloy films. The first type of additives are non-reducible cations and serve to increase the conductivity of the bath. Sodium is the cation of choice for this recipe and the salt from which it is derived is a supporting electrolyte. To maintain pH, boric acid is added as a buffering agent. Experience has shown that tight control of pH is required to achieve repeatable results. In addition to the boric acid, an external monitoring system is used to maintain the pH at 2.70 ± 0.03 using a HCl based makeup solution.

The final chemical included in the recipe is sodium saccharin. This is added as a leveling, brightening and stress reducing agent. The proper amount of this additive can theoretically adjust the stress in the deposited permalloy to near zero though at the expense of degraded magnetic properties. In practice, a tensile stress on the order of 50 to 100 MPa is used in compromise to achieve a balance between the various parameters (see section 9.2.4 below).

## 9.2.3 Magnetic Plating System

A special tank is used to electroplate the permalloy films. The tank itself is a plexiglass box approximately 6 inches wide, 12 inches long, and 5 inches deep. On the floor of the tank is a pure nickel anode. Parallel to and approximately 2 inches above the anode is a wafer holder into which the circular substrate is placed face down. The wafer is supported by a ring that covers approximately 2 to 3 mm of its periphery, providing electrical contact to an external power supply. Between the cathode and the anode is a stirring paddle that agitates the solution with particular attention given to ensuring the bath near the anode and the cathode does not become depleted of ions. The paddle is moved at about 30 RPM. External to the tank is a C-shaped, permanent magnet that produces a constant parallel field across the face of the cathode. The presence of this field induces a crystalline anisotropy in the permalloy introducing an easy axis to the deposited film and improving the magnetic performance of the alloy.

## 9.2.4 Residual Stresses in Plated Metal Films

The origin of the internal stress often seen in electrodeposited permalloy films is most likely caused by hydrogen introduced into the lattice during the plating process [86, 141]. The conjecture is that either elemental or metallic hydride is co-deposited in the permalloy film. In the presence of these compounds, the lattice temporarily expands. After deposition, the hydrogen diffuses out of the film resulting in a shrinkage of the lattice and the development of a tensile stress [116, 154, 155]. It should be noted that while hydrogen

may be a major source of residual stress, it is likely not the sole cause of the phenomenon.

To combat the intrinsic stress that can arise in plated permally, the additive saccharin is frequently used.  It is believed that it limits the formation of hydrogen during plating and thus reduces the realized film stress [86].  An alternate explanation is that the saccharin changes the structure of the crystal lattice through the adsorption and inclusion of sulfur.  In either case, it has been reported in [119] that a 60 nm thick permalloy film plated from a saccharin-free bath had a stress of 332 MPa while a similar film deposited from a saccharin-containing bath had a stress of only 60 MPa.  This latter value is in the same range realized in the films plated for this work.

It should be noted that there does not seem to be a stress gradient through the thickness of the films.  This is evidenced by the fact that even in thick platings, where the metal deposits delaminate from their substrate, patterned structures such as cantilever beams do not curl.  If the stress at the top surface of the deposited film was not equal to that present in the bottom, the difference would tend to bend the strips of the material.  Since this does not occur, yet delamination of thick films is a problem, it is concluded that the residual stress is uniform throughout the material.

A limitation imposed by permalloy is that it should not be exposed to excessive heat during processing.  The stress in these films tends to greatly increase in the presence of high temperatures.  This effect has been noted by others [111, 115] and in the course of this work levels above 300 °C were found to be incompatible with permalloy.  Above this temperature, even plated films 1 or 2 microns thick quickly delaminate.

## 9.2.5 Magnetic Characteristics of Plated Metal Films

Using this tank, a range of plating rates were used to produce a number of permalloy test samples [123]. The magnetic properties were measured using a hysteresis loop tracer and are shown in figure 9-1 with the corresponding deposition conditions given in table 9-1. These data show that plating currents up to 15 mA/cm² produce permalloy films of acceptable quality for use in relays. At higher current levels, the properties of the films begin to degrade. The relative permeabilities of these samples ranged from 128 to 5000. Corrections for demagnetization were not made as the length and width of the test structures are much greater than their thickness, minimizing such effects.

In the films plated at less than 15 mA/cm², a linear relationship between applied field and the resulting flux density can be seen. Plating at higher rates produces deposits with a decidedly non-linear relationship. The higher current density films also show no indication of a clearly defined easy or hard axis, while those plated at 10 mA/cm² clearly display such a evidence. Finally, the coercivities measured range from a low of 5 Oe (10 mA/cm²) to a high of 52 Oe (25 mA/cm²) with bulk 80:20 permalloy having a reported

| Sample Number | Current Density [mA/cm²] | Plating Rate [μm/min] | Deposited Thickness [μm] |
|---|---|---|---|
| 1 | 10 | 0.066 | 4 |
| 2 | 15 | 0.15 | 4.4 |
| 3 | 20 | 0.20 | 3.75 |
| 4 | 25 | 0.25 | 3.9 |

Table 9-1: Plating condition for B-H loops shown in figure 9-1 [123].

value of 0.05 Oe.  For this work, these values are acceptable though not ideal.  In practice a

deposition rate of less than 4 μm/hr is used to ensure high quality deposits.  Films plated in

this manner are well suited for the MEMS microrelay application.
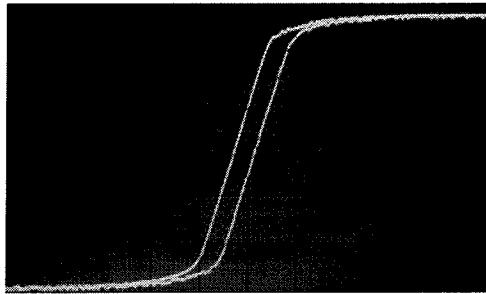


(a)  Sample 1:  Easy Axis:
Horizontal axis: 398 A/m / div
(5 Oe / div) Vertical axis: Uncalibrated
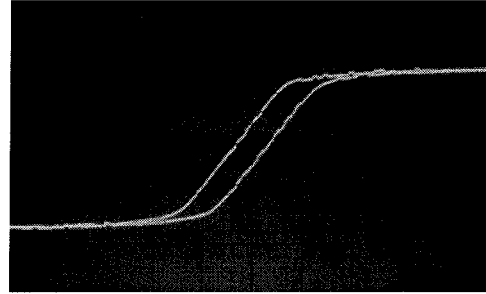


(b) Sample 1: Hard Axis:
Horizontal axis: 398 A/m / div
(5 Oe / div) Vertical axis: Uncalibrated
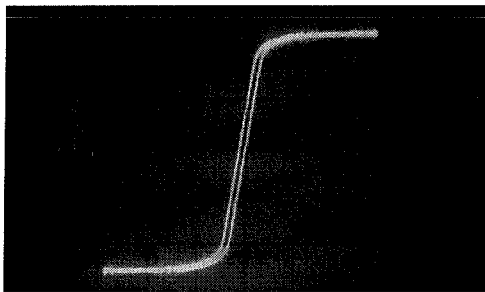


(c) Sample 2:
Horizontal axis:  796 A/m /div
(10 Oe / div) Vertical axis: Uncalibrated
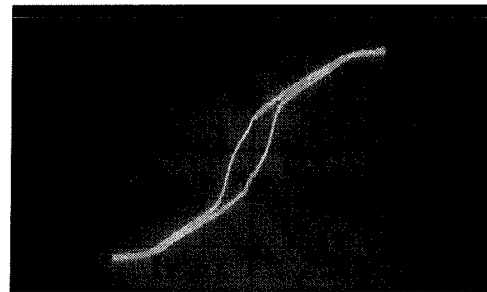


(d) Sample 3:
Horizontal axis:  796 A/m /div
(10 Oe / div) Vertical axis: Uncalibrated
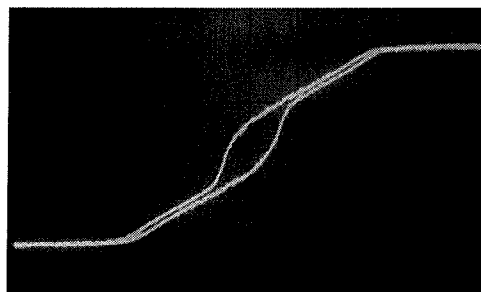


(e) Sample 4:
Horizontal axis: 1.6 KA/m /div
(20 Oe / div) Vertical axis: Uncalibrated

Figure 9-1:  B-H loops for samples plated using the conditions listed in table 9-1.

## 9.3   Bulk Silicon Micromachining

In the fabrication of micromachined devices, it is often beneficial to selectively etch into the silicon substrate. This process is known as bulk silicon micromachining and is used to form thick structures, grooves, membranes, and through holes. Removal of the silicon can be achieved in several ways the most popular of which are wet etching, plasma etching, and gas etching. Gas etching is a relatively new technique whose acceptance has yet to be determined. Wet etching is arguably the most widely used bulk micromachining technology though plasma processes are quite common and are a growing in popularity.

In bulk etching, silicon can be removed in either an isotropic or anisotropic fashion. Isotropic etching removes material at a uniform rate in all directions. In the case of etching through a pinhole, a perfect half sphere will be formed beneath the masking material (see figure 9-2.a). Anisotropic etchants, on the other hand, etch down into the substrate much more quickly then they etch sideways. This allows high aspect ratio structures to be formed in the wafer (see figures 9-2.a and 9-2.b). Both forms of etching are obtained with wet, plasma, and gas etching.



|        (a)        |        (b)        |        (c)        |
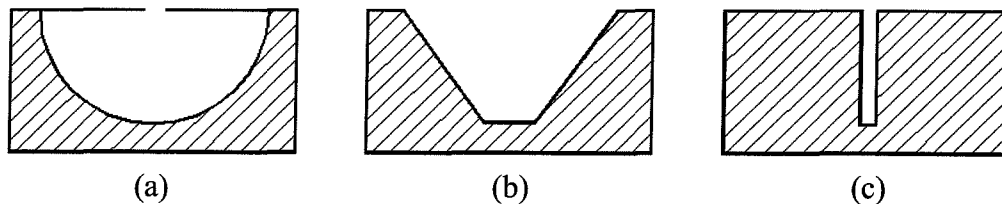
**Figure 9-2**: (a) Half sphere formed by isotropic etching through a pinhole. (b) Cavity shape formed by anisotropic wet silicon etching. (c) High-aspect ratio structure that can be produced by DRIE plasma etching.

### 9.3.1 Gas Etching

In gas etching, a fluorine-based reactant vapor is introduced into a vacuum chamber where it attacks exposed silicon surfaces [93, 153]. The etching occurs at room temperature in the absence of a plasma and the reactants formed are gaseous compounds that readily diffuse away from the area being etched. Etch rates are typically high and a wide range of easily definable masking materials may be used. This technique is isotropic which limits its effectiveness in forming patterned structures extending deep into the substrate. While the results achievable with the gas etching may be adequate, a system capable of producing this type of etch was not available until towards the end of this research and therefore was not used.

### 9.3.2 Plasma Bulk Micromachining

Plasma or reactive ion etching (RIE) is an etching process where reactant gases are excited into a plasma to provide both isotropic and anisotropic removal of material. The anisotropic capabilities of such systems are of the most interest for deep, through-wafer etching. Traditional RIEs are capable of producing wall aspect ratios of up to 10:1 vertical etch to sideways etch. Depth limitations and speed typically prevent these machines from forming through wafer type features.

A new technology, designated Deep RIE (DRIE), has recently gained wide acceptance in the micromachining community. Etch rates up to several microns per minute and aspect ratios better than 50:1 have been reported [87] and through wafer etching has

been demonstrated [88, 92].   For application in MEMS microrelay fabrication, the capabilities of the RIE are not sufficient.  While the results achievable with the DRIE are adequate, a system capable of producing this type of etch was not available until towards the end of this research and therefore was not used.

### 9.3.3 Wet Anisotropic Silicon Etchants

Wet etching is commonly used in silicon processing due to its low cost, good reliability, and high throughput capabilities.  While the features that can be formed with this technology are not as varied as those promised by DRIE, a wet etch system only requires a beaker, a hot plate with stir bar and some readily obtainable solutions of potassium hydroxide (KOH), ethylene-diamenepyrocatachol (EDP), or tetramethyl-ammounium-hydroxide (TMaH).  The listed chemicals are anisotropic wet etchants.  The isotropic variety will not be discussed here.  Anisotropic wet silicon etchants enable the formation of straight walls along the <111> crystal plane of a silicon lattice.  Etch ratios of greater than 150:1 between the <100>:<111> and <110>:<111> are readily achieved (see appendix W1).  Proper selection of wafers with particular crystal faces allow the fabrication of a wide variety of structures [117].

### 9.3.4 Bulk Micromachining in This Work

The through-hole formation process required in the fabrication of the MEMS armature microrelay is achieved used KOH.  While EDP and TMaH could also be used,

KOH is friendlier than EDP and it provides the fastest etch rate. All of these etchants will attack metals with KOH and EDP doing so aggressively. For this reason, the throughhole formation step must be executed at the beginning of the processing run or adequate protection must be provided for any existing metal structures. The former is the easier approach and the one used in this work.

## 9.4   Sacrificial Materials

The choice of sacrificial material is one of the most important steps in producing freestanding, surface micromachined structures. In selecting the material, three parameters must be considered. The first is mechanical stability and maximum layer thickness, the second is compatibility with the processing steps to which it will be exposed, and the third is the release agent required to remove the sacrificial layer at the end of the process. For the MEMS microrelays, the sacrificial layer must be relatively thick. To be able to standoff several hundred volts across open contacts, a 5 to 10 micron gap is needed. The sacrificial material defines this gap. The processing steps that the sacrificial layer sees are relatively benign and are low temperature. Mainly they are photoresist deposition, thermal evaporation of thin metal seedlayers, and metal electrodeposition. Finally, the releasing agent should only attack the sacrificial layer and none of the other materials in the device. In the case of the relay, possible materials exposed to the release agent are permalloy, copper, gold, titanium, rhodium, silicon, LTO, and photoresist.

### 9.4.1 CVD Materials as Sacrificial Layers

The most widely used sacrificial material in micromachining is LTO. Typically used in conjunction with polysilicon surface micromachining, its releasing agents are 48% HF and BHF. For the MEMS microrelays it turns out that LTO is not a very suitable sacrificial material. Depositing three or more microns of this oxide is very difficult due to internal film stresses that tend to cause it to crack. Even if such thicknesses were attainable, 10 or more hours would be needed to deposit 5 to 10 microns. Additionally, HF readily attacks titanium and after long-term exposure, surface discoloration of permalloy is seen. In those cases where photoresist might remain on the substrate, HF will quickly strip it from the wafer. Finally, the LTO used to insulate the coils will be attacked along with the sacrificial LTO. These issues preclude the use of low temperature oxide for defining the contact gap during the fabrication of the microrelay.

A second material gaining more widespread use as a sacrificial material is polysilicon. A gas phase as well as a wet release is available that does not attack any other materials in the microrelays making it attractive at first glance. However, like LTO, film stresses and long deposition times limit its usefulness in this application. Its truly debilitating drawback is that is must be deposited at temperatures in excess of 400 °C, typically in the 800 to 900 °C range. This is incompatible with the materials over which it must be coated and so eliminates it as a potential sacrificial material.

### 9.4.2 Sacrificial Metal Release

A newly reported use for electroplated copper is as a sacrificial layer [151]. Deposition by electroplating is readily compatible with the microrelay fabrication process

and has several advantageous properties.  Copper films are readily deposited to many tens

of microns in thickness.  Since it is conductive, it can double as an electroplating seedlayer

for subsequent platings.  Stripping of the copper raises several points of concern, however.

Primary is the presence of the copper coil in the armature microrelay.  While this could

potentially be protected from the copper etchant, it is cause for concern.  The possibility of

copper contamination of the contact materials is also of issue.  Electroplated gold, the first

target contact material, is known to be relatively porous.  When in direct contact with

copper, copper ions tend to migrate through the gold to the surface of the contact [125]

where it will oxidize and greatly degrade switching performance.  Typically a barrier layer

of nickel is used to prevent this.  Such a layer covering the sacrificial material would

obviate the primary function of this copper.  Finally, the copper films produced by the bath



(a)                                              (b)
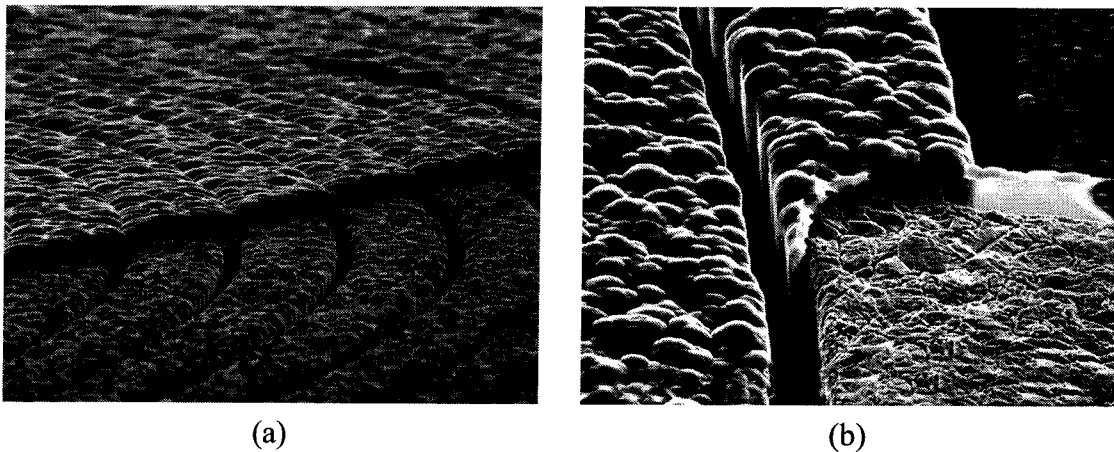
**Figure 9-3**: (a) Good quality copper lines electroplated with a current density of
10 mA/cm$^2$.  In the bottom half of the SEM, the copper traces are coated with LTO
and in the top half they are covered by an additional layer of permalloy.   (b)
Magnified view of the surface of one of these lines.  In the upper left the copper is
coated with LTO.  In the lower right, the LTO has been stripped away to reveal the
pure electroplated copper beneath.  The RMS roughness to be approximately 1
micron.

recipe included in appendix R1, have a relatively high surface roughness.  Figure 9-3 is a

high magnification SEM photo of the surface of a 10 micron-thick plated copper film

exhibiting an RMS roughness of approximately 1 micron.  What effect this level of

featuring on the face of the contacts has on device operation is not known but it was

deemed sensible to be able to be able to form smooth mating surfaces.  For these reasons,

copper was excluded as a viable choice of sacrificial material.

It is possible to use aluminum to release MEMS structures [135, 160].  Aluminum

films can be aggressively removed by solutions of HF or by more selective, commercially

available etchants.  Deposited by sputtering or evaporation, mirror-smooth films can be

produced but at limited thicknesses.  Achieving aluminum layers of 5 to 10 microns is

difficult and time consuming.  In practice, this metal is not a readily applicable to the

MEMS microrelay fabrication processes.

## 9.4.3 Organic Materials

Parylene and polyimide have limited use as release layers in the MEMS fabrication

process.  Their ability to be deposited in a wide range of thicknesses over highly non-

planar surfaces is very attractive.  The conformality and thickness control possible,

especially with parylene, would make them well suited to defining the contact gap in the

microrelays.  However, the predominant, and perhaps only gentle, means of stripping

these materials from a wafer is with oxygen plasma ashing.  The nature of plasma etching

limits the amount of sideways undercut that can be achieved with such a process.  In

practice, structures about two times wider than the thickness of the underlying sacrificial material can not be adequately released. Introducing a large number of etch holes throughout a film (creating a mesh-like appearance) can be used to free wide structures but at the expense of removing much of the volume of the material. In the case where the meshed film is a purely structural component, adequate rigidity can be maintained for use in a device. In the case of a magnetic circuit, however, the corresponding extreme decrease in effective cross sectional area of such components destroys their flux channeling characteristics.

Photoresist presents itself as a near ideal sacrificial material for use in the MEMS microrelays. Thick layers, in excess of 50 microns, can be easily deposited and patterned. After patterning, treatment at elevated temperatures (up to 200 °C), referred to as ultrabaking, can be used to fully polymerize the resist. This both eliminates its sensitivity to subsequent UV exposures as well as increases its chemical resistivity. A further benefit of this heat treatment is to reflow the material, eliminating sharp corners, improving surface planarity, and minimizing step coverage issues with subsequent layers. This work has shown that photoresist prepared in this manner can survive all subsequent microrelay processing steps.

Some care must be taken to minimize heating of this polymerized resist due to the potential of cracking. The releasing agent for the ultrabaked resist is a commercially available resist stripper that seems to only remove organic materials. Silicon, nitride, oxide and all relay metals show no signs of being attacked by the stripper even at temperatures

greater than 150 °C. Since the stripper removes all organics from the device during sacrificial etching, this approach ensures that hydrocarbon contamination is not an issue from any device-related source. These qualities make photoresist the logical choice of sacrificial material for microrelay fabrication.

# THEORETICAL AND PRACTICAL ASPECTS OF MICRORELAY CONTACTS

The electrical contact points and the contact gap region are arguably the most

important portion of a relay. The physics governing their performance must be understood

before the design of any successful relay can begin. To this end a chapter covering the

theoretical and the practical aspects of contacts that must be considered are included here.

The information within is applicable to both the MMC and the armature microrelays

presented in the following chapters. The equations below have been used to analyze the

devices fabricated in the course of this research while the practical data from the work of

others and industry has provided some insights into the performance characteristics of the

contacts in the MEMS devices. Carefully evaluating the experimental results and providing

scientific explanations for the observed phenomena has set forth new avenues of research

that will lead to further improvements in the design and fabrication of this latest class of

micro electro mechanical systems.

## 10.1 Introduction

The ultimate purpose of all the component pieces in a relay is to create a physical connection between two wires that will allow current to flow. Low contact resistance and long-life are the desired traits demanded by all types of relays. How these are achieved and what contributes to their failure, however, depends largely on the loads that the device will switch. In signal relays, life-long stability of the contact characteristics is paramount. In power applications it is the high-switched current and large standoff voltage capabilities. A wide variety of contact materials, contact conditioning and contact configurations are employed in macroscale relays to meet these wide ranging requirements. Many of the same approaches can be utilized in MEMS devices. Some, however, must be radically modified to accommodate the restrictions imposed by micromachining technology. Still others must be discarded completely. In determining which parameters to vary and which relay designs to use, an understanding of what makes a good electrical contact is needed.

For the purpose of contact material selection, it is useful to class the available materials into several functional groups. Much can be learned by looking at the materials being used in commercially available, macroscale relays as well as those used in MEMS microrelays developed by various research groups. Here, relay power ratings are the chosen criterion for classifying the many materials in present use. This automatically accounts for the voltage and current capabilities of the contacts.

## 10.2 Contact Materials in Commercial Relays

For high power loads, powdered metal composites are traditionally used. In this case, high power is defined as loads drawing tens of amps at tens to hundreds of volts.

For a general purpose relay of this type, silver-tin-oxide alloys are widely used due to their low material transfer, low rate of erosion and good anti-welding characteristics [105]. Additional alloys that are commonly used are silver-cadmium-oxide, silver-nickel and silver-graphite. As noted above, the processes that form these are presently incompatible with micromachining.

For moderate power switching of one to ten amps at tens of volts, a wide range of contact materials is found in commercial relays. Often used are silver, palladium/platinum and their alloys. Key to the effectiveness of these metals is their resistance to forming hard surface oxides. In the case of palladium and platinum, oxide formation is very low. In the case of silver, oxidation and tarnishing does not readily occur except in the presence of sulfur [78]. These oxides, however, tend to be soft and can be overcome with adequate closure forces.

Low power or signal switching applications are those applications where the switched currents are low and the corresponding voltages not excessive. Currents up to one amp and tens of volts are fall within this regime. When switching signals, contact resistance stability or the life of the relay is paramount [104]. The next important parameter to be met is low insertion loss. To meet lifetime stability requirements, the mating surfaces should not oxidize nor react chemically in air. To minimize insertion loss, contact resistance must be kept as low as possible. Such conditions make precious metals the most widely used contact materials for relays that switch these types of loads. Three common metals are gold, mercury and platinum. Rhodium and Ruthenium have also been shown to

exhibit good signal switching performance [104, 112]. With the exception of mercury, all of these materials can be deposited by electroplating from baths that are compatible with photoresist. Mercury vapor deposition can be, and has been [118], used in micromachined devices but due to its hazardous properties and environmental concerns, this metal was not considered in the course of the research.

## 10.3 Previously Reported Microrelay Contact Materials

As noted in the introduction chapter, there have been a fair number of microrelays fabricated using MEMS technology conducted over the last two or three decades. Like the many modes of actuation used in these devices, a wide variety of contact materials have been explored. Gold and nickel seem to be the dominant contact types although silver, palladium, mercury, nickel-iron and polysilicon have been reported. Contact resistances achieved in the microrelays range from 20 m$\Omega$ to > 10 k$\Omega$ while hot-switching currents in excess of 1 amp. A review of the previous data provides valuable information of practical microrelay contact performance.

Polysilicon, one of the most popular MEMS materials, has seen limited use as a contact material in microrelays. This is not surprising due to its relatively high resistivity 1 to 10 $\mu\Omega$-m, its extreme hardness of approximately 100 x 10$^8$ N/m$^2$, and its tendency to grow a touch, insulating native oxide on its surface in air [142]. The fact that it has been used in this manner at all is more attributable to the structural members of these relays being formed from polysilicon and so no additional fabrication steps were required to pattern it

into contacts. The polysilicon-to-polysilicon contacts reported in [100, 101] were limited to switched currents of a few mA and with contact resistances in the > 10 kΩ range. Polysilicon-to-mercury [140] contacts seem to perform slightly better but are still consigned to low-level signal switching due to their 1 ohm-range contact resistance which passes only tens of milliamps of current.

In relatively widespread use as a contact material in microrelays is nickel and permalloy. As with polysilicon this popularity is probably due largely to the simultaneous forming of these metals into structural and magnetic components. Relays implemented with nickel-only metals [130] have reported contact resistances on the order of 5 Ω. Similar resistance levels are seen when nickel-iron is used for one contact and a different metal is used for its mate. For Cu, Ru, and Au a switch employing a high-force actuator achieved resistance levels of 30 Ω, 5 to 30Ω, and 2 to 3 Ω respectively [147]. A fully micromachined, relay using nickel-to-gold contacts achieves a packaged resistance of < 400 mΩ which are reliable enough to allow the device to be sold commercially [80]. For many applications this is satisfactory though when minimum insertion loss is other materials is needed.

Gold repeatedly shows itself to produce the lowest on-resistance values in micromachined devices. The low bulk resistivity, physically soft material can produce microrelay operating parameters very similar to those seen in their macroscopic relatives. When paired with platinum, a respectable 200 mA can be passed through the 220 mΩ closed contacts creating a RF microswitch with less then 0.1 dB insertion loss at 4 GHz

[157]. Gold-to-gold contacts win the contest for lowest reported on-resistance with a value of 22.4 m$\Omega$ [147]. Looking at the data for all of the devices using such contacts show a broad range of values with a more typical minimum value of 50+ m$\Omega$ to highs of tens of milliohms [95, 121, 133, 150, 160]. Current levels that can be hot-switched with such contacts are reported to be < 200 mA. Above 100 mA, issues of excessive melt of the contacts and on-condition welding cause a rapid decrease in lifetime and performance of the microrelays.

## 10.4 Contact Resistance Theory

A good electrical connection in a relay requires sufficient force to bring the two contact points together and form a low resistance region. The relationship between the contact force and contact resistance of clean contacts can be expressed as [106]:

$$R_{contact} = \frac{\rho_{mat1} + \rho_{mat2}}{2} \sqrt{\frac{H_{material}}{F_{contact}}} \qquad \text{eqn. 10.1}$$

$R_{contact}$ = contact resistance $\qquad\qquad$ $F_{contact}$ = contact force

$\rho_{mat1}$ = resistivity of contact first material $\qquad$ $\rho_{mat2}$ = resistivity of contact second material

$H_{material}$ = hardness of softer contact material

This equation is specified for a force range of 100 mN < $F_{contact}$ < 100 N. For microrelays,

100 mN is the high end of the forces that can reasonably be achieved.  Values down in the 1 to 10 mN range are more realistic.  Still, equation 10.1 should at least describe the relative resistance versus force curve that can be expected.    An idealized plot of contact resistance versus closure force is shown in figure 10-1.  Obviously, the conductivity of the contact material has a direct effect on the minimum contact resistance.  Perhaps not as expected is the square-root relationship the resistance has with the contact material hardness over the contact force applied.

Material hardness and closure force enter the equation as they determine the true size of the area in electrical contact.  The two faces of two discrete contact points never mate perfectly to one another.  There are always micro irregularities on the two surfaces that form peaks and valleys.  When the two contacts are forced together, two peaks will
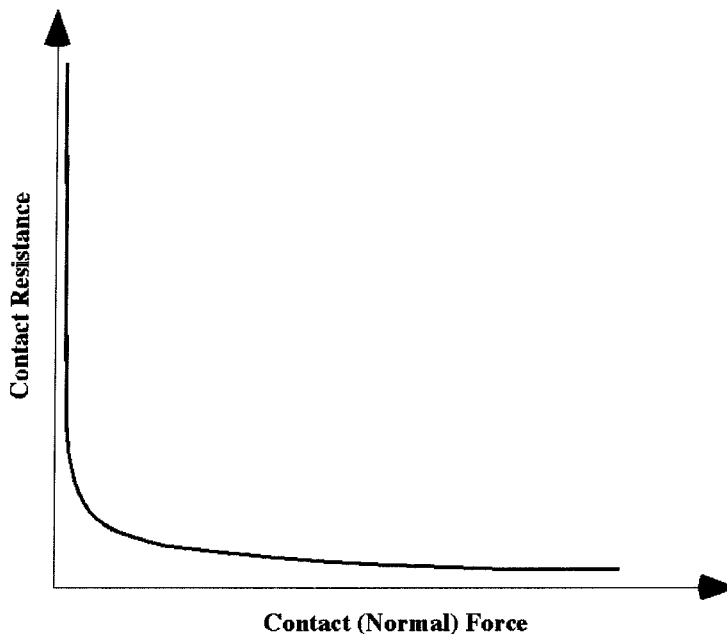


Figure 10-1:   Idealized relationship between the normal contact force and the electrical contact resistance of a relay contact set.

connect before any other portion of the surfaces. For a given force, the hardness of the material determines is those two peaks will deform sufficiently to allow more peaks to come into contact with one another and if so, how many. In the case of very large forces and very soft material, the two faces of the contacts can experience sufficient deformation that the entire area defined as contacts can become a path for electrical conduction. In practice, however, the forces that can be generated only produce a conducting region that is partially complete.

The limitation of forces available in microactuators requires that the proper contact material be chosen when designing a MEMS microrelay. For a number of useful metals, the material properties are given in table 10-1. While by no means an exhaustive list of all the materials that can be used, and in fact that have been used, in relay contacts, this table includes the most common pure metals utilized for the full range of light to high load applications. Reviewing the values for hardness and electrical conductivity, equation 10.1 would suggest that metals such as Ag, Au, Sn and Hg would be widely used in relay manufacture. This is indeed the case. However, other considerations (see the following sections) offer limit the usefulness of these metals and require that other types of materials be employed.

Not listed are many of the alloys regularly used in commercially available relays. Not surprisingly, mixing two or more metals in the proper ratio can produce an alloy that has significant improvement in one or more areas of performance. Perhaps the best examples of this are the widely used silver-tin-oxide and silver-cadmium-oxide contacts.

Typically used for switching loads that produce a high energy arc, these materials, when compared to pure silver, have superior resistance to material transfer and material loss due to arcing [79].    The price for this performance is slightly greater interface resistance between the mated contacts.

| Material | Density $kg/m^3$ | $\rho$ electric resistivity $10^{-8}$ $\Omega$-m | E Young's Modulus $10^{10}$ $N/m^2$ | H Hardness $10^8$ $N/m^2$ | softening $T_s$ temp $^\circ$C | softening $U_s$ voltage v | melting $T_l$ temp $^\circ$C | melting $U_l$ voltage v |
|---|---|---|---|---|---|---|---|---|
| Ag | 10.5 | 1.65 | 7 | 2.9 to 6.7 | 150 to 200 | 0.09 | 960 | 0.35 |
| Ag +30%Pd | 10.9 | 16 | - | 8.99 | - | - | 1220 | - |
| Al | 2.7 | 2.7 to 3.3 | 7 | 1.7 to 9 | 150 | 0.1 | 658 | 0.3 |
| Au | 19.3 | 2.3 | 8 | 1.46 to 8.4 | 100 | 0.08 | 1063 | 0.45 |
| Cd | 8.6 | 7.3 to 7.7 | 6 | 2.25 | - | - | 321 | 0.15 |
| Cr | 7 | 20 | - | 14.6 | - | - | 1800 | - |
| Cu | 8.9 | 1.75 | 11 | 3.9 to 5.6 | 190 | .012 | 1083 | 0.43 |
| Fe | 7.9 | 5 to 9 | 20 | 6.7 | 500 | 0.21 | 1530 | 0.60 |
| Mo | 10 | 4.2 to 5.8 | 30 | 13.5 to 28.1 | 900 | (0.3) | 2800 | 0.9 |
| Ni | 8.8 | 7 to 9 | 20 | 7.9 to 24.7 | 520 | 0.22 | 1455 | 0.65 |
| Pt | 21.4 | 10 to 13.6 | 13 | 5.6 to 9 | 540 | 0.25 | 1773 | 0.70 |
| Rh | | 4.3 | - | | - | - | 1966 | - |
| Ru | | 17.2 | - | | - | - | 2500 | - |
| Sn | 7.3 | 11 to 12 | 5 | 0.5 to 0.67 | 100 | 0.07 | 232 | 0.13 |
| Ta | 16.6 | 12 to16 | 19 | 5.6 to 39.3 | 700 to 1000 | 0.3 | 2900 | 1.0 |
| W | 19.3 | 5.3 to 7 | 38 | 14.1 to 41.6 | 1000 | 0.4 | 3400 | 1.0 |

Table 10-1:  Physical constants often used for calculations on contacts.  Taken from [106].

The majority of alloyed contacts must be eliminated from the list for potential use in micromachined relays as the manner in which they are produced is incompatible with many MEMS processes. Continuing with the example above, silver-tin-oxide contacts are typically produced by powder metallurgy in which the constituent materials are mixed together then formed into contacts by a press, sinter and extrusion process [136]. Such treatment would shatter the base silicon substrate on which MEMS microrelays are fabricated. Such incompatibilities may be overcome by sputtering the contact material onto the wafer. However, since many of the beneficial traits of these alloys arise from the grain structures produced by their production processes, the sputtered films may not perform as well as the bulk material. Additionally, depositing the many microns of material needed is very time consuming and expensive. Finally, patterning of the thick films is also non-trivial. From a micromachining standpoint, materials that can be selectively deposited at arbitrary thicknesses are the most attractive.

Electroplated metals are the most readily micromachined contact materials. By plating through a photoresist mold, the metal can be selectively deposited on nearly any structure in nearly any desired shape. In most cases, thicknesses up to tens of microns can be easily attained. Furthermore, with the proper selection of bath solution, a wide range of plated alloys can be realized. This flexibility is very attractive when developing prototype devices. For this work, only those metals that can be plated have been considered for the contact materials. These include Ag, Au, $Au_xNi_y$, Cr, Cu, Fe, Ni, $Ni_xFe_y$, Pd, Pt, Rh, Ru, and Sn. This is still a relatively large number of choices and other criteria must be set to allow the final selection of contact material.

## 10.5 Properties of Switched Loads

In choosing the proper material for a relay, the loads that will be switched by the device must be considered. This will allow the most important contact parameters to be determined. The types of loads that are switched by relays can be separated into three main classes: resistive, motor and lamp. These can be broken down further into light, moderate and high switched powers. Whether these loads are hot-switched or cold-switched also needs to be considered. In hot-switching, the load voltage is seen across the contacts as the relay closes. This means current will begin flowing as soon as the mating surfaces touch. In the case of cold-switching, the contact are brought together and any bouncing that may occur allowed to die out before the load voltage is applied and current begins to flow. Obviously, hot-switching is the more demanding and contact-damaging closure mode. The special demands made by the different load types and switching modes complicate the process of contact material selection.

Motor loads, also referred to as inductive loading, are perhaps the most demanding. Initial inrush currents can be many times the steady-state value. Typically hot-switched, these excessive currents can quickly destroy contacts rated for the steady-state load. During relay break, the disconnected motor windings can produce very large transient voltage spikes across the contact gap (arising from the $V = L\dfrac{dI}{dt}$ relation). Without special bypass circuitry, arcing invariably results and can lead to early failure of the contacts.

Lamp loads may seem to be simply resistive at first glance, however, their operation can be nearly as punishing to contacts as that experienced with inductors. The

difficulty arises from the large change in resistance that a filament experiences as it heats from room temperature to the operating regime. The cold resistance can easily be 5 to 10 times lower than the hot value producing initial inrush currents many times that expected by the power rating of the lamp bulb. This extreme condition always occurs as the relay is closing and the armature is possibly bouncing which exacerbates the wear experienced by the contacts. The main solution to this problem is to employ a relay rated for the peak current load generated by the lamp. As with motor loads, this application usually requires hot-switching but unlike motors, no inductive voltage spikes are generated during contact break.

Resistors are the most easily designed for loads seen in relay applications. The inrush and steady-state current levels are identical and no transient spikes are generated during switching. The only care that must be taken is to assure that the circuit being switched is truly resistive. Often, discrete or parasitic capacitances act a large current sinks during relay make and break. If not identified during relay specification, excessive contact wear can result. Both hot- and cold-switching are common for this category of loads.

## 10.6 Contact Erosion Phenomena

The power switched by the relay to a given load also greatly affects the life of the contacts. From a simple $I^2R$ resistive heating argument, the larger the switched current, the higher the contact operating temperature. High temperatures can quickly degrade the contacts and make it easier for contamination to impede switch function (see section

14.7.4).  In the case of cold-switching, heating only arises from the load current flowing through the resistance of the closed contacts.  In general the temperature levels generated are not excessive and mechanical where is more often the cause of failure in relays switched in this manner.  For hot-switching, however, the contacts are subject exceedingly hot temperature with each opening and closing of the relay.  This is due to the fact that for an instant in each switching operation, the area of contact is nearly zero resulting in very high local current densities.  Temperatures can easily rise high enough to melt and even boil the contact material [79].

A commonly seen mode of failure is the creation of spike-and-crater formations in and on the contact surfaces [77].  This phenomenon arises when there is material transfer from one contact to the other and is made possible by the localized heating mentioned above.  A "crater" forms in the surface of the contact losing the material while a "spike" builds up on the face of the other contact (see figure 13.12) for an example of this effect in a MEMS microrelay).  This type of material transfer condition is typically associated with a direct current application.

High voltages placed across the contact gap during switching will produce arcing. The arc degrades the contacts through excessive heating and material transfer and/or loss. The arc typically arises from and terminates on a very small area of the contact and can cause the same melting and boiling conditions seen during localized current density heating. Material transfer will occur from the hotter cathode to the cooler anode along the path of the arc [77].  If the arc forms during closure, material loss from the melt zones may occur due to splatter.  These melted regions can cause the contacts to lock or weld together as the

material re-solidifies.  During opening, the force available may be insufficient to break these welds and an uncontrolled-on condition can result.

## 10.7 Low Closure Force Contact Performance

Proper selection of contact material for a given application often requires real life testing of several metals or alloys deemed suitable by the general characteristics given above.  In the little researched realm of ultra-low closure forces attainable in MEMS actuators, this may be a necessary step in qualifying a given material.  To this end, Hosaka, et. al [108], collected several sets of useful data.  Gathered for gold, palladium, and silver, graphs of $R_{contact}$ vs $F_{contact}$ and breakdown voltage vs electrode gap are reproduced in figure 10-2.

The plot of $R_{contact}$ vs $F_{contact}$ provides several very important pieces of information.  First, the overall shape produced by the data points trace out the general shape of the curve predicted by equation 10.1.  Recall that this equation was developed for forces in excess of
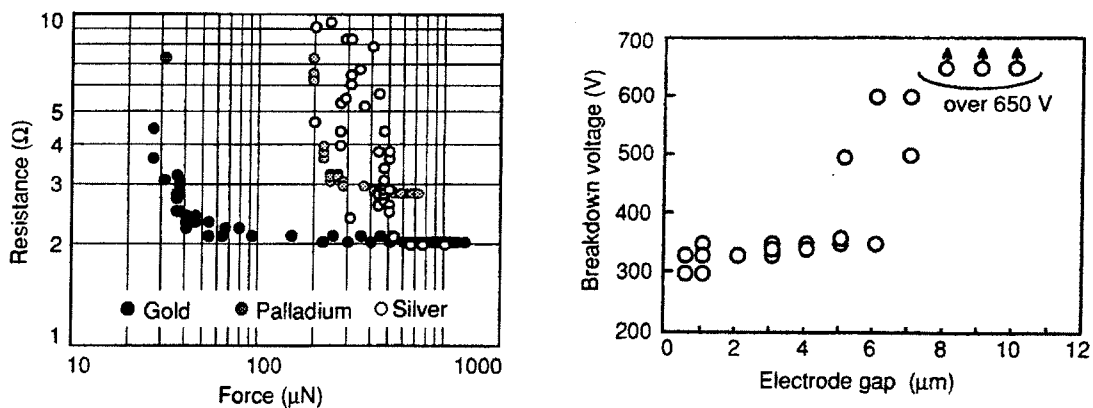


Figure 10-2: Experimental data showing the relationship between (a) on-resistance and contact force for the metals Au, Pd, and Ag, and (b) between breakdown voltage and contact gap.  Taken from [108].

100 mN.   The Hosaka data suggest that the formula still holds down into the $\mu$N force range.   Second, this data indicates a minimum target $F_{contact}$ needed to attain minimum contact resistance for the metals studied.   For gold this value is roughly 100 $\mu$N.   For palladium and silver a minimum force on the order of 500 $\mu$N is needed.   Gold is perhaps the softest contact metal and so it reasonable to assume that at least 100 $\mu$N closure forces are needed regardless of the contact material being used.   This force level rules out electrostatic actuation and suggests that the high performance electromagnetic actuator produced in the course of this research is needed.

In the case of breakdown voltage vs electrode gap, the Hosaka data is again illuminating.   It shows that breakdown does not occur across gaps ranging from 1 to 5 microns when up to several hundred volts are applied.   However, for the more demanding application where 350 or more volts must not cause breakdown, gaps greater than 5 microns must be maintained.   Again, traditional electrostatic actuation will not work in this case.   Piezoelectrics are only capable of small deflections and are also of little use here. That leaves electromagnetic and thermal actuation as viable alternatives.   As noted in section 8.4.3, the slow switching speeds attainable with thermal devices leads to the selection of electromagnetics.

## 10.8 Contact Materials Selected for This Work

The highly varied performance of the contacts reported by different research groups is particularly noteworthy.   As expected, the characteristics between devices fabricated with

different contact materials are dissimilar. Using an argument based on just the variables in equation 10.1 (i.e., contact force, hardness, and resistivity), however, all of the Au-to-Au microrelays with similar force capabilities should produce similar contact resistance values. This is not the case. Some of the reported on-resistances having as much as an order of magnitude difference for devices that generate the same order of magnitude closure forces. This suggests that contact configuration, surface condition, and mode of closure can affect overall operation as much as contact material characteristics. A comforting trend in the published papers is that the expected fall in contact resistance is seen when, in general, larger and larger forces are applied allowing some faith in equation 10.1 to be maintained.

For the majority of the work performed in the course of this research, electroplated Au contacts have been used. Electrodeposition of gold is easily realized and the resulting films can be tens of microns thick with minimal surface roughness. Furthermore, it plates satisfactorily from a number of seed layer materials including evaporated gold and copper and electroplated permalloy. All of these metals are used in the construction of the MEMS microrelays. The 100 μN required to minimize gold-to-gold contact resistance, as shown by the Hosaka data, should be achievable even by a poor quality electromagnetic actuator. Published data for microrelays produced by other researchers suggest that acceptable contact resistance performance can be achieved at lower force level as well. Some relays with a thin layer of rhodium plated over the gold have been fabricated to investigate if this harder metal will extend the life of the contacts in higher current, motor load applications.

# CHAPTER
# 11

# MAGNETOSTATIC MICRORELAYS FOR DC BRUSHLESS MOTOR COMMUTATION

The first family of microrelays presented in this thesis has been developed to commutate motors used in space applications. These devices operate on the magnetostatic actuation principle discussed in section 11.4 that allows the contact forces generated in the switches to easily reach the millinewton level. In the initial target application, the MEMS Motor Commutation (MMC) microrelay acts as both an active switching component and a rotor position sensor. Actuation energy and commutation timing information is provided by the permanent magnets on the shaft of the motor itself allowing the MMC microrelays to be simple and small.

The MMC microrelay-based commutation system aims to simplify the control of brushless motors to a level equal to that of brush motors while maintaining the reliability of the brushless system. Ultimately the microrelays will be placed within the windings of the motor effecting a great reduction (and possible elimination of) in the total size of the

external control circuitry. The prototype commutation system based on these devices is less than 10% the mass and volume of the electronics it replaces, it eliminates all but two wires from the wiring harness, it requires no external control and it dissipates less than 1/1000th the total motor power. The remaining two wires, DC power and ground, run between the motor and a power source through a single ON/OFF control relay (not a MEMS device ... at present).

Microrelay design, fabrication and testing is presented. Electroplating forms all of the constituent pieces of the device. The process design is compatible with a large variety of starting substrates and several different types are explored. The mechanical and electrical performance of the resulting microrelays is fully characterized and lifetime testing is performed. After being switched to failure, the devices are taken apart and the failure mode analyzed. Finally, performance of a target motor commutated with the MMC microrelays under a variety of environmental conditions is discussed.

## 11.1 Motivation

DC electric motors are extensively employed in space born applications as the motive device for linear and rotary drives. Due to the DC power bus utilized by most space born vehicles and to the difficult and inefficient conversion of DC-to-AC power, AC motors are seldom used. The expensive nature of launching large, heavy equipment out of the gravity well of Earth demands that smaller and lighter systems that can be used in spacecraft be developed. These new assemblies must also meet or exceed the performance specifications of the components that they are replacing.

The commutation subsystem of a motor drive assembly is the presetn limiter of total system miniaturization. In brush motors, the relatively fixed size of the contactors result in significant motor lengthening as total volume decreases. In brushless motors, the commutation electronics are the main driver of the total size and weight of realized systems. The disparity between motor and controller size becomes excessive in extremely miniaturized motors such as the commercially available 3-mm-diameter shown in figure 11-1 [99] that is being targeted for future NASA microrover missions (similar to the Mars Sojourner rover but smaller). Here, the electronics easily occupy ten times the volume of the motor they are designed to control. Units presently used in flight hardware also suffer from poor motor-to-controller size ratios as can be seen in figure 11-2. The motor, approximately 1 inch in diameter, sits on top of its commutation electronics package that is nearly four times the volume of the motor itself. By reducing or eliminating present motor control systems, large gains will be realized in the system-wide design of future spacecraft.
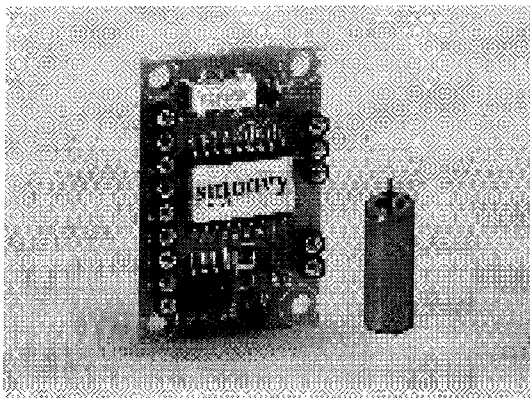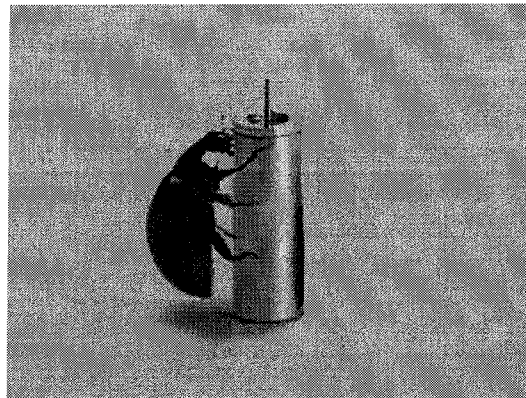


(a)                                    (b)

Figure 11-1: This very small (3-mm diameter) DC brushless motor is being targeted for future space missions. In (a) the motor is dwarfed by its controller while in (b) its very small size is emphasized by showing that it is not much larger than a lady bug.

### 11.1.1   Forces Driving the Miniaturization of Space-Qualified Motors

Savings, even small ones, in power budget, complexity, mass, and volume of flight instruments have a highly leveraged effect on the total cost and reliability of the spacecraft in which they are used. For a given set of mission parameters, every savings in one system directly corresponds to larger savings in support systems. Lower power budgets require a smaller power generator (typically solar cells), smaller heat sinks, and smaller battery reserves. Reduced instrument size and weight permits the use of a lighter, more compact support frame. All size and weight reductions directly translate into smaller, less expensive booster rockets, higher attainable orbits, and/or faster flight times to interplanetary points of interest. Once in space, the reduced mass demands less fuel and power for attitude stabilization and course corrections translating into smaller rockets and gyroscope wheels. Through the miniaturization of DC motors, spacecraft designers will be able to devote more of the limited available resources to the mission goals and less to the
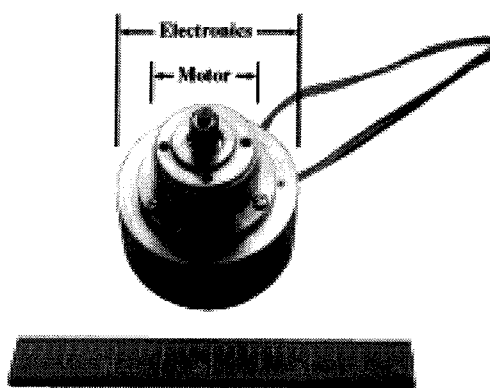


Figure 11-2: A DC brushless motor and controller assembly presently used in space-qualified systems. The electronics package is larger, heavier, and more complex the the motor that it commutates.

systems necessary to place the instruments at their target coordinates.

Selecting between brush and brushless motor types involves choosing those performance characteristics that are required while minimizing total system complexity, cost, and size. Brush motors are typically considered to have moderate size, weight, power efficiency, and complexity as well as low monetary cost. Overall reliability for these motors, however, is poor. For high reliability, brushless motors are chosen. The price for this dependability is an increase in system size, weight, complexity and monetary cost as well as a decrease in power efficiency and lower temperature capabilities. Since a system is only as reliable as its weakest component and since routine maintenance in space is an impossibility at present, spacecraft designers typically hold reliability at a premium. However, the limitations imposed by current rocket and space power generation technologies often override this directive. A prime example of the tradeoffs required can be seen in the design of the Mars rover, Sojourner. DC brush motors provided the locomotion for this small vehicle. The power available, the weight permissible and the extreme environment of this mission eliminated the more desirable and reliable option of DC brushless motors.

## 11.1.2   Advantages of MEMS Motor Commutation Relays

Control of DC brushless motors is traditionally achieved by a complex package of position sensing and power electronics. To properly operate, a given winding of the motor must be energized for only a portion of a given revolution. If the winding is active

otherwise, it retards motor rotation, decreasing efficiency and increasing torque ripple. For this reason, shaft position must be accurately sensed, usually by Hall effect sensors or an encoder. The signals from the sensors are used by the commutation electronics to generate the appropriate waveforms for each motor winding. The end result is a complex controller consisting of a hundred or more components, occupying a relatively large volume, and consuming a notable amount of power. To keep pace with motor miniaturization, reduction of part count and complexity is needed.

One MMC microrelay per motor phase can replace the commutation electronics and position sensors presently used in DC brushless motor systems. Micromachining permits the microrelays to have nearly negligible size and weight. For space qualified hardware, this will allow the devices to be encased inside the motor windings. Mounting the components inside the motor provides two very attractive benefits. First, the distance of the wires run between the motor and the microrelays is minimized. Second and most importantly, the motor itself provides the actuation energy and timing control for the devices. The magnetic fields generated by the magnets on the shaft of the motor fluctuate as the rotor turns. By proper design and placement of the MMC microrelays, these fields can act as both the control signal and the actuating force for device switching. The results are high closure forces and perfect synchronization of switching time versus rotor position.

Eliminating the need for the sensing and control circuits reduces system complexity. No external power source is needed to actuate the microrelays. Energy is saved and the number of wiring connections in the system is minimized, which improves reliability.

Since the microrelays have nearly negligible size and weight, the motor, not the controller, drives the mass and volume of the final system. When flight mission parameters permit, arc suppression circuitry can be added to minimize contact wear and extend the electrical life of the microrelays. With proper design and the use of silicon wafers, it may be possible to include this circuitry in the substrate each device.

Space qualification costs for a motor with integrated microrelays will be less than half that of a traditional system. At present, the motor and the commutation electronics are qualified separately to ensure they operate adequately in the vibration, temperature, vacuum, and radiation environments to which they will be exposed. After successfully passing these tests, the two subsystems are combined. The assembled motor system must undergo its own round of tests, many the same as those performed on the subsystems, to insure proper function. In the case of the motor with integrated microrelays, there is just one system to qualify. The microrelays are inside the motor housing and are tested at the same time as the motor. In practice, the cost savings promised could be quite substantial.

## 11.1.3   Space Operating Environment Considerations

The potentials of being able to properly function under the wide environmental conditions that may be encountered on a space mission make MEMS microrelays especially attractive. Typical space applications in which motors are used expose the systems to near-perfect vacuum and high radiation levels. For bulky electronic commutators, vacuum poses a challenge due to the very poor thermal conduction that it provides. Heat generated

in the circuit boards is not readily dissipated and special care must be taken to ensure they do not overheat. Radiation induced damage in semiconductor devices is always a problem in space and typically requires special shielding and/or fault tolerant circuit design (typically with redundant and possibly oversized components). Both result in increased system size, weight, and complexity.

A less common, but potentially incapacitating, exposure condition is large temperature extremes. This may occur on special missions where the motor system will be in direct contact with an interplanetary body or the surface of a planet. The motor can easily fall below liquid nitrogen temperatures (77 K) in these circumstances, taxing even the hardiest electronics. Semiconductor devices are designed to operate at room temperatures. At 77 Kelvin, electrical properties may be altered though failure is more likely to arise from the packages that are typically composed of several materials, each with dissimilar thermal expansion coefficients. While it may be possible to custom design an electronics package capable of operating in this regime, the cost and time associated with qualification testing makes such an approach prohibitive for most missions being proposed in the current "faster, better, cheaper" NASA programs.

MEMS microrelays can be designed to be insensitive to the environmental conditions. Fabricated from electroplated metals, radiation has no semiconductor junctions to degrade or punch through. In an environment where sufficient radiation is encountered to cause metal embrittlement, electronic components would fail much more rapidly than mechanical devices. Vacuum should only act to enhance the break down voltage range achievable by the contact gap (with no atoms to ionize, no arc should form). Embedded in

the motor windings, the motor becomes an intimate heat sink for the relatively small

thermal load generated at the contacts as current flows through the device. In order to be

used at liquid nitrogen temperatures, special care will have to be taken to ensure the thermal

cycling does not damage the microrelay. Making this part of the performance specification

for the first generation device allows a single round of tests to qualify the microrelay for

use in all potential motor commutation applications.


## 11.2 DC Brushless Motor Operation

Brushless motors develop their mechanical torque from the interaction between

magnetic fields produced by currents flowing in wire coils and permanent magnets. For

the sake of clarity, only 3-phase, 4-pole brushless motors, the target platform for MMC



■■■■ => position of sensor or relays

(a)                                              (b)
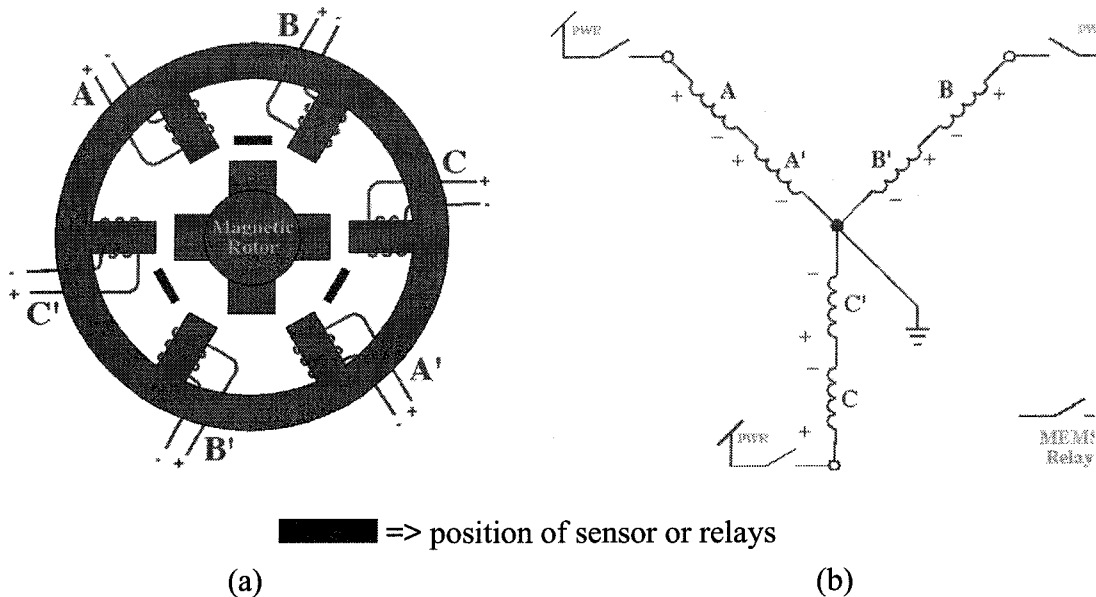
Figure 11-3: Schematics showing (a) a generic cross section for a 3-phase, 4-pole, DC brushless motor with integrated Hall effect position sensors that monitor rotor position, and (b) one possible manner in which the 6 winding can be wired together and attached to power. The position of the MMC microrelays will be the same as the Hall effects shown in (a).

microrelay integration, will be discussed here.   In general, however, this discussion is

valid for brushless motors that employ a different number of phases and poles.   Shown in

figure 11-3.a is a schematic of a cross section of the target motor.   Here, the housing is

formed from magnetic core material and is shaped to produce six stator poles.   Low

resistance wires wrap each pole forming stator windings.   Along the central axis of the

motor runs the rotor or shaft to which two permanent magnets are affixed with their four

poles directed orthogonal to the axis (hence the term 4-pole).



(a)                          (b)                          (c)

(c)                          (d)                          (e)
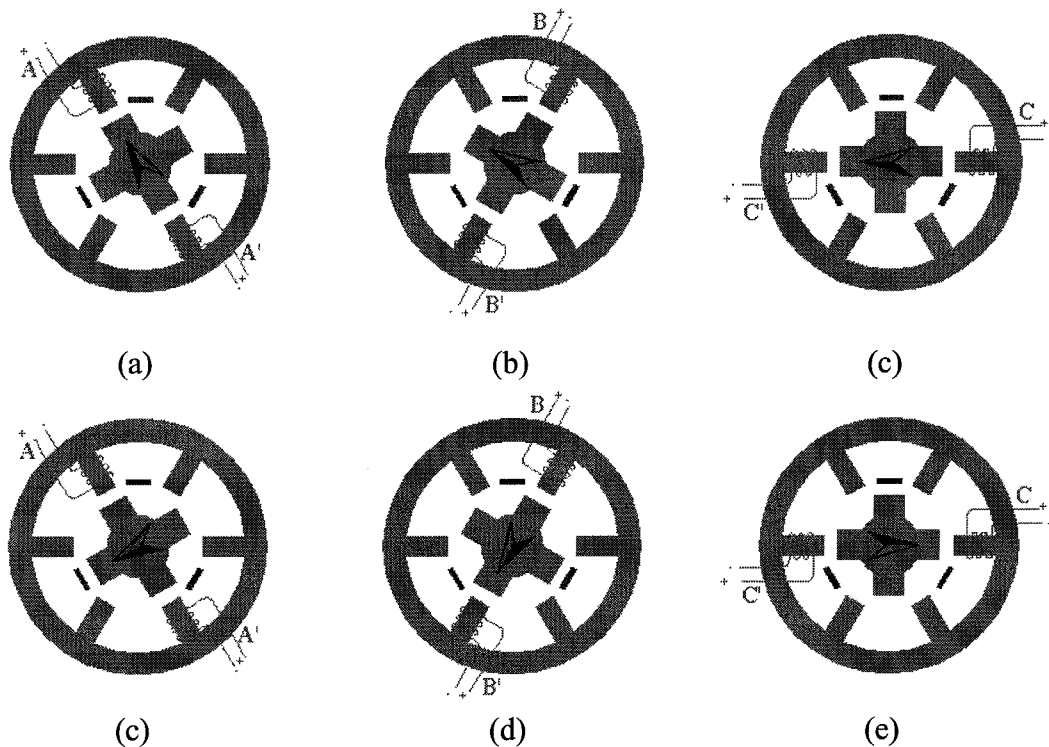
Figure 11-4:  Sequential schematics showing the commutation and resulting rotation of a DC brushless motor using Hall effect sensors (or MMC microrelays).  In each frame, only one pair of windings is included and is the set energized for that 30° rotation section.  Note how the sequence of activating the coils "rotates" clockwise while the actual rotor motion is counter-clockwise.  The 6 diagrams show the first 180° of rotation.  Continuous rotation is achieved by repeated cycling of the coil activation pattern of (a) through (f).

Stator windings are energized in opposing pairs creating magnetic fields directed at the rotor magnets. This creates a torque on the shaft causing it to rotate in the direction that will align the permanent magnet poles with the stator fields. By serially addressing neighboring coil-pairs an artificial rotating magnetic field can be created that is followed by the magnets on the shaft, allowing continuous rotary motion to be achieved. One of the main benefits of this type of motor is that it does not require an electrical connection be made to the spinning shaft like is needed in a brush-type motor. Such a motor can be driven using three sinusoidal waveforms that are phase shifted with respect to one another by 120° (hence the term 3-phase motor). This does not require any control electronics. The rotation speed and shaft power output is being set by the AC line frequency and voltage level, respectively.

For a DC supply to be used as the power source for such a motor, commutation electronics must be used. Unlike the case with a 3-phase AC source applied, this mode of implementation passes a constant current through one set of opposing-pair windings while the other two are electrically disconnected. After the shaft rotates to align with the magnetized stators, that set of windings is de-energized and the DC voltage is applied the next coil-pair. In this manner, the shaft rotates in a step-wise fashion with the total of steps per revolution equaling the number of poles times the number of phases (12 steps in this case). The sequence (first 6 steps) in figure 11-4 schematically shows the rotor position, the winding that are energized, and the effective waveform seen by the motor over during one-half revolution cycle. The term stepper motor is often applied to these devices for this

reason. Continuous motion can be achieved by actively sensing the position of the rotor using embedded Hall effect sensors or a shaft encoder. This allows the electronic commutator to switch in and out the proper coils at the proper time, achieving smooth rotation.

## 11.3 Target Motor and Winding Configuration

The motor targeted to demonstrate the proof of concept of MEMS microrelay commutation is shown in figure 11-5. The cylindrical housing actually contains two 3-phase, 4-pole brushless motors. The two coaxial motors, or dual drive, can be powered singly or together to provide backup redundancy or double drive power respectively. The double redundancy is typical of space flight hardware, which requires system backups to ensure that failure of no one component will disable an entire instrument. The outer diameter of the motor housing measures approximately 2 inches and the dual drive only weighs around 2 lbs. Mounted on the sides of the motor are two boxes which contain the commutating electronics. Each box is a separate commutator controlling one of the coaxial motors. The two sets of electronics weigh on the order of 2 lb. As these weight values suggest, and as can be seen in the figure, the commutators contribute as much, if not more, to the mass and volume of the total system as does the dual drive motor itself. The added complexity of the electronics is substantial with the circuit contained in each box comprised of on the order of 100 components.

For this work, only one of the dual drive motors is commutated with MMC

microrelays with its mate connected to no external circuitry nor power supply. Maximum DC operating voltage is 28 VDC at approximately 450 mA stall-torque current. Maximum rotational speed is on the order of 1200 RPM. Stator winding DC measurements show a resistance of 62 Ω and an inductance of 8 mH. The permanent magnets inside the motor housing produce an external magnetic field of at least 2500 Gauss. These values set the switching specifications for the MMC microrelay and the available actuating magnetic field strength. Some insight into the amount of inductive spiking that can be expected when breaking current flow through the windings is also provided.

Included in figure 11-5 is the Hall effect sensor that is embedded in the motor windings. Three of these devices, positioned 120° relative to one another in the motor, are used by the commutation electronics to sense rotor position (see figure 11-3.a). As
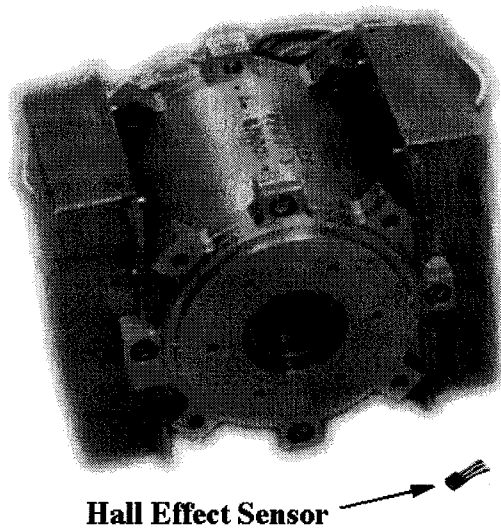
Hall Effect Sensor

Figure 11-5: The motor targeted for commutation by the prototype MMC microrelays. Mounted on each side of the motor are two boxes of electronics being replaced by the MEMS approach. In the foreground is a sample Hall effect sensor of the type wound inside the stator coils.

packaged, their dimensions are approximately 4.2 x 6.0 x 1.4 millimeters. Two of the design parameters for the MMC microrelay is that it replace the function of this sensor and that it be nearly the same packaged size to allow it to be embedded inside the motor.

## 11.4    MMC Microrelay Actuation

Design of an electromagnetic relay requires that the mode of opening and closing of the contacts be fully understood. In electromechanical relays, contact make and break is achieved using forces derived from the magnetic fields of permanent magnets. The MMC microrelay actuation is arises from the torque generated on a strip of magnetic material when it is placed inside an external magnetic field. In determining the force level available in the device, special attention must be given to those parameters shared by both the mechanical and the magnetic structures. Optimizing a component for mechanical performance often destroys its magnetic characteristics and vice-a-versa. Only with a system-wide approach can a satisfactory magnetic MEMS device be realized.

### 11.4.1  Magnetostatic Actuation

The mode of magnetic actuation chosen to provide the closing forces needed in the MMC microrelay employs external permanent magnets. A plate of permalloy material, exposed to an external magnetic field, can experience a deflection that corresponds to the strength of the applied field and the dimensions of structure. The force, or more properly the torque, that produces the bending arises from the interaction between the external field

and the magnetic moment it induces in the permalloy metal. This mode of actuation will be referred to as magnetostatic actuation in this thesis due to the use of permanent magnets. This terminology is not wholly accurate as the magnets need to be in motion during relay operation and therefore their fields are technically not static. Still, to avoid confusion with the actuation mode in the variable-reluctance relays, magnetostatic is chosen as the best compromise.

## 1.4.2 Magnetostatic Actuation Theory

In an isolated environment, a plate of ideal soft magnetic material holds no remnant magnetization. In the presence of an external magnetic field, however, the plate becomes magnetized along its easy axis. An induced magnetization, **m**, is created along this axis and interacts with the magnetic field to produce a moment. Upon removal of the field, the soft magnetic material loses its induced moment and **m** falls back to zero. In the work presented here, permalloy (see section 9.2.2) is the soft magnetic material employed in the fashioning of the relay. Even small external fields fully magnetize this metal and establish a saturated magnetic flux density within its volume.

The actuated structure in the microrelay is a large plate of permalloy. The force acting on this ferromagnetic metal can be estimated by using an effective magnetic charge model also presented in [114, 120, 123]. The system is shown schematically in figure 11-6 in which the plate is introduced nearly perpendicular to the field. One end is fixed at a pivot while the other end is free to move vertically. As the field is applied, the magnetic

moment that is induced can be modeled as the formation of two magnetic charges of, opposite polarities, at the two ends of the plate. This model results in two point forces arising on the two ends of the permalloy in opposing vertical directions. Since one end is fixed, that force can be neglected. At the free end of the plate, the force is given by:

$$F = Bending\ Force = M_s(WT)H\cos\theta \qquad\qquad \text{eqn. 11.1}$$

where:

L = plate length [μm]     T = plate thickness [μm]     W = plate width [μm]

$\theta$ = deflection angle [degrees]     $M_s$ = saturation magnetization [Tesla]

H = external magnetic field strength [Amp/turns]

1 Tesla = 10,000 Gauss = 796,000 Amp/turns

This equation assumes that the external field is uniform though it will still hold to first order for a divergent field. In the case of the relay, the additional forces associated with a non-uniform field are negligible and therefore are not considered here.

An additional note for this mode of actuation is that the plate should be introduced to the field at an angle slightly greater than zero, as defined above. Maximum force is generated at the zero angle however this introduces a slight unknown to device operation. In theory, the permalloy can become magnetized either parallel or anti-parallel to the length of the plate. The former results in upward deflection as desired while the latter causes downward deflection. In practice the presence of the substrate just microns beneath the beam creates an energetically favorable push toward upward deflection. however, this is

not guaranteed. Considering assembly and placement tolerances for the final application (see sections 12.4 and 12.5) it is wise to preferentially orient the plate at an initial two to three degree angle for reliable operation.
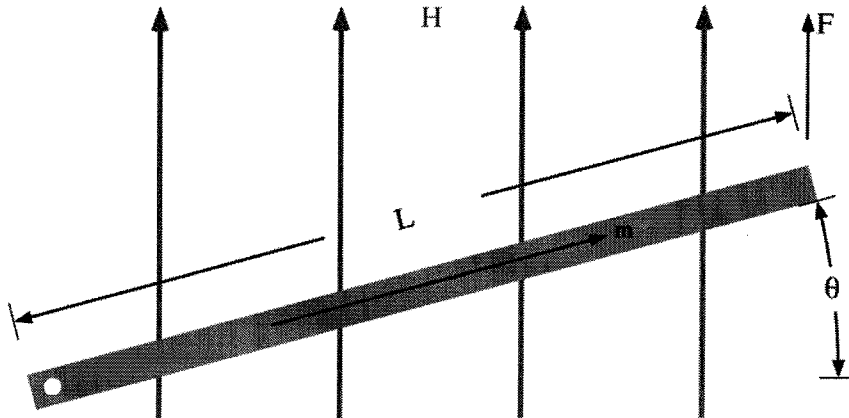


Figure 11-6: Simple cross section of the magnetostatic actuator system. A beam introduced across an external magnetic field acquires an induced moment, **m**, and, if one end (the left in this case) is held in place, a force rotates/bends the tip tending to align it to the field. This system is described by equation 11.1.

# CHAPTER

# 12

## DESIGN AND FABRICATION
## OF MMC MICRORELAYS

The design and fabrication of the MMC microrelays must be executed with a target motor systems already identified. The size, speed, current and voltage levels, and the internal makeup of the motor all affect the performance level that will have to be achieved by the device. Because this research is focused on developing prototype devices, some relaxation in the final microrelay fabricated can be allowed. Still, the ultimate goal of this project is to develop a device that will be the enabling component for a new, space-qualified, DC brushless motor commutation technology.

## 12.1　Design of MMC Microrelays

The targeted microrelay performance specifications for use in motor commutation are set by several considerations. The first is the target motor itself. The maximum nominal operating conditions of the target motor are 28 VDC at up to 450 mA and rotational speed up to 1200 RPM. This requires that the microrelays must be able to hot-switch these voltages and currents at frequencies up to 80 Hz (number of poles * 1200 RPM / 60 sec). Contact resistance should be less than 1% (620 m$\Omega$) of the stator winding resistance for the

life of the device and should be able to withstand a fair amount of wear due to inductive arcing. The minimum breakdown voltage level across the contacts is targeted for greater than 1000 volts setting a gap spacing of at least 20 microns. This should to accommodate all realistic inductive-switching transient. The packaged dimensions of the microrelay need to be about the same as those for the Hall effect sensor described above. Though not stated as a requirement for the prototype devices, the desire to operate the microrelays at liquid nitrogen temperature should be kept in mind while determining the fabrication processes and materials.

Fabrication may be achieved with either a single substrate or multiple substrate design. For space qualified applications, the increase in mechanical strength possible and the reduction in relay-to-relay performance variations produced by a one-substrate process will make a monolithic approach most favorable. For research and development purposes, however, the multi-piece design is more attractive. Simple fabrication steps, design flexibility and processing times are achieved with this approach and the cost of final hand-assembly is acceptable. Construction from multiple substrates permits non-destructive analysis of microrelay performance and contact wear. Additionally, it allows for more controlled shaping of the mating electrical surfaces.

Regardless of the fabrication process, magnetostatic actuation is the mechanism used to achieve high closure and contact forces. The magnetic field available from the rotor magnets is greater than 2500 Gauss. The microrelays are designed to have a closure force greater than 5 mN to ensure low contact resistance even when hard contact materials are used. The contact break force is set to about one-tenth the make value. This force level should be adequate to ensure that welding does not cause premature electrical failure under normal operation.

Using the magnetostatic theory discussed in section 11.4 and the beams-in-bending theory covered in section 14.5 dimensions for a large cantilevered plate can be calculated.

The thickness of the plated permalloy film is limited to 10 microns due to stress considerations (see section 9.2.4). Note that the only geometry variables in equation 11.1 describing the magnetostatic forces at the end of the cantilever are thickness and width; length does not add to the realized forces. The width of the plate is set to 2.8 mm, the largest practical value allowed by the packaging dimensions limitation. This permits a range of contact gaps and plate lengths to be used to provide the desired make plus break

| Summary of MMC Microrelay Design Parameters | |
|---|---|
| **Device and Environmental Parameters** | |
| actuation plate material | permalloy |
| saturation magnetization: permalloy | 0.8 to 1.0 Tesla |
| modulus of elasticity: permalloy | $\approx 100$ GPa |
| external magnetic field strength ($H_{ext}$) | > 2500 Gauss |
| actuation plate angle (see figure 11-6) | 2 to 3 degrees |
| actuation plate dimensions: | |
| width | 2800 microns |
| length | 2000 microns |
| thickness | 10 microns |
| contact gap | 75 microns |
| base contact material | soft gold |
| **Targeted Values** | |
| contact make force | > 5 mN |
| contact break force | > 0.5 mN |
| break down voltage | > 1000 volts |
| hot-switch | $\leq 450$ mA @ 28 VDC |
| switching speed | > 80 Hz |
| operate in vacuum | yes |
| operate at 77 Kelvin | attempt |
| packaged dimensions | $\approx 4.2$ x 6.0 x 1.4 mm |

Table 12-1:  Values used in the design and fabrication of the MMC Microrelay.

forces of 5.5 mN. Processing variations and lithography limitations make it likely that as-designed and as-fabricated dimensions will differ by as much as 10 microns. To minimize the effect this may have on the device-to-device variations in closure force, the length is set to 2 mm. As a cubed term in the bending equation, a 10-micron variation in length will only produce a 1.5% variation in deflection force. A contact gap of 75 microns is then required to set the desired deflection force of 0.5 mN. This dimension has a linear relationship with force and can easily be controlled to within less than 1 micron. The values used to arrive at this design are summarized in table 12-1.

The contact material chosen to be micromachined into the microrelays is soft plated gold. As the information covered in chapter 10 shows, gold produces the lowest contact resistance for a given level of closure force. Inclusion into the relays should ensure good initial contact performance at lower (< 200 mA) current levels. Above this value, a harder, more durable contact material will be needed. Rhodium is chosen for this range. Rather than executing a separate fabrication run to make microrelays with this contact metal, the rhodium is plated on a device by device basis over the base gold contact material. This minimizes the time required to produce microrelays designed for different current levels. The flexibility intrinsic to this approach allows many different platable materials to be tested in a straightforward manner. The main drawback to the technique is that fine control of the thickness plated is relatively difficult to achieve.

## 12.2 Two-Substrate Microrelay Fabrication

The first generation devices are assembled from two component pieces processed on separate substrates. The majority of the micromachining is performed on just one of these pieces. The process attaches a freestanding permalloy plate complete with integrated contact strip to the substrate wafer. Processing of the second substrate is much simpler.

Contact material is deposited globally onto the wafer and an insulating spacer material is laid down and patterned into strips. After dicing into the appropriately sized dies, wires can be attached to the two pieces, which are then bonded together.

The main processing steps used to produce the heavily micromachined piece used in this microrelay design are shown in figures 12-1 with the complete process included in appendix R2. Fabrication begins on a conducting substrate. An oxidized silicon wafer coated with an evaporated Cr/Au seedlayer is typically used though some runs with solid copper wafers have been performed. A sacrificial layer of photoresist is deposited to a thickness ranging from 2 to 20 μm and patterned to provide access holes to the substrate. Over the spacer, a seedlayer is deposited and a photoresist mold laid down and patterned in preparation for the plating of the 10-micron-thick permalloy actuation plate. A second photoresist mold is prepared to allow soft gold to be selectively plated along the end of this wide cantilever beam. The last processing step for this piece is freeing of the structure by
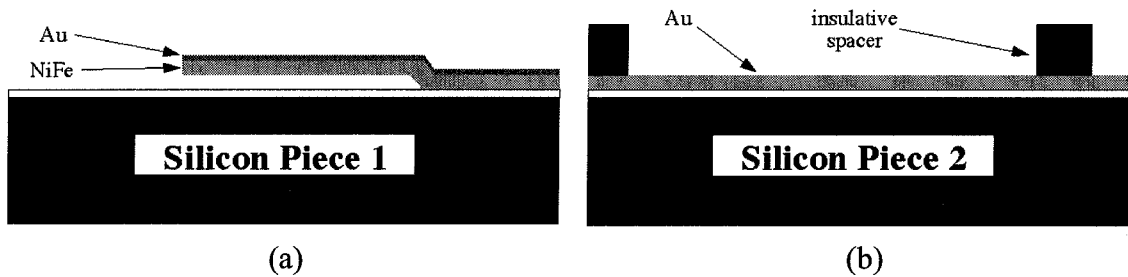
Figure 12-1: Cross sections of the two micromachined pieces that form the first generation MMC microrelays.
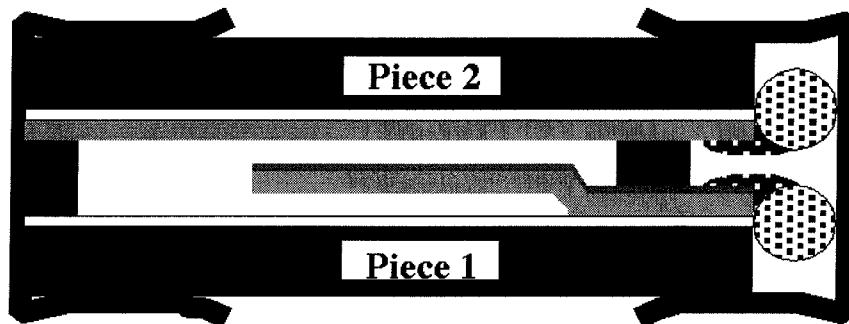
Figure 12-2: Assembly of the two pieces into a fully functional MMC microrelay.

removing the sacrificial spacer in hot photoresist stripper.

Fabrication of the second piece of the dual substrate design is very simple. Contact material is laid down on a rigid substrate followed by the deposition and patterning of a permanent spacer layer (typically formed from ultrabaked photoresist) 75-microns thick. Wafer dicing defines the final dimensions of this piece.

As the last step in the process, the two substrate are assembled into the final microrelay as shown schematically in figure 12-2. Wires are hand-soldered to the two pieces which are then bonded together using either tape, heat shrink tubing or epoxy. Tape and tubing are attractive since they allow the two microrelay pieces to be easily separated for failure analysis. Epoxy produces more durably packaged devices and makes it possible to seal the contact area. A point to consider when fully encapsulating the microrelay in epoxy is that vapors may be given off during curing, a portion of which will be sealed inside the device. If they contain hydrocarbons, carbon contamination of the contacts may occur. In practice, heat shrink tubing was the bonding material most frequently used for assembly. This technique is quick and simple and clamps the full length of the two substrates with equal force. After lifetime testing of a microrelay is completed, the tubing is slit with a razor separating the two pieces. This facilitates easy access to the contact regions so that wear and failure analysis can be conducted via microscope and SEM.

## 12.3    Two-Substrate Design Processing Issues

When silicon wafers are used, problems with delamination of the electrodeposited permalloy cantilevered plate require that anchor holes be etched into the substrate. This is done before the seed layer is deposited by patterning the oxide with round holes and etching in KOH for about 10 minutes. The anisotropic etchant produces square cavities in the silicon whose corners have overhanging oxide "shelves." Evaporating a seedlayer over

such cavities coats parts of their sloped sidewalls sufficiently to allow metal to be plated inside during permalloy electrodepostion. Sideways growth occurs during such a thick plating and locks the metal film to the substrate by anchoring to the overhanging oxide shelves.

In theory this technique seems reasonable but in practice results were less than ideal. The stress in the 2.8-mm wide, 4-mm long (2 mm for beam, 2 mm for anchor) plated films is large enough to break the oxide shelves and pull the metal anchors out of the substrate. Figure 12-3 show a high magnification photograph of one of these anchors. Though it is hard to see in this picture, oxide shelf fragments are embedded in the permalloy matrix. The delamination keeps fabrication yields for such structures to less than 5%.

The delamination of the plated permalloy film is not the sole challenge posed by this fabrication process. By simply adding more saccharin to the plating bath, less stressful films should be achievable though at the possible cost of poorer magnetic properties (see
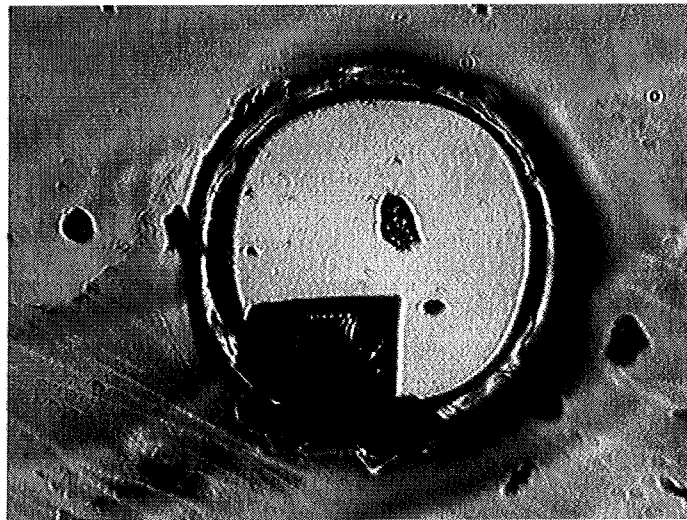


Figure 12-3: A photograph of a pemalloy anchor point that was plated inside a cavity with overhanging oxide "shelves" that were intended to improve adhesion. These shelves have broken and shards can be seen in the metal matrix around the perimeter of the round anchor plug. Also present is a large chunk of the silicon wafer that was ripped out of the substrate wafer during delamination.

section 9.2.4). More of an issue is the shaping of the contact points along the end of the permalloy beam. It turns out that the leveling capabilities of the gold plating bath (see appendix R1) is rather poor. Current crowding at the edge of the patterned mold causes the plated thickness at the center of the features to be less than that grown at their edges. Rather than forming as relatively spherical domes, the realized shape of the contacts is more like that of a cake whose center has fallen while its edges remain in place. It was expected that the performance of such contacts would be inferior ones more ideally shaped so a new fabrication process was developed.

## 12.4    Three-Substrate Microrelay Fabrication

The fabrication process that successfully produces MMC microrelays creates three component pieces on three separate substrates. The processing steps of all three pieces are

Permally Flap with Moving Contact

Bond Traces Substrate
with Alignment Pegs

Stationary Contact
and Gap Spacer
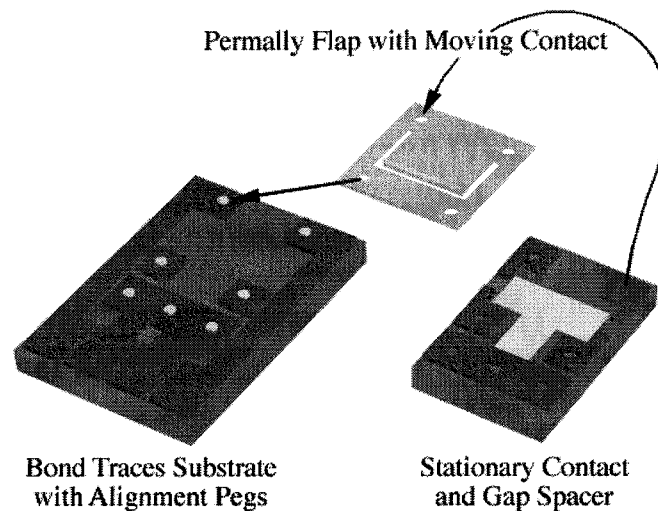
Figure 12-4: Drawings of the pieces fabricated and assembled to produce the three-substrate microrelay. To the left is the bond traces piece, in the center is the permalloy plate with integrated contact strip, and to the right is the final piece containing the stationary contact and the spacer pedestals which define the contact gap. Note how the bond traces substrate has 7 plated alignment pegs on its structures with the other two pieces containing alignment holes that fit down over these points making assembly quick, reliable, and accurate.

kept very simple and have no critical steps. This allows fabrication runs to be completed in just days while providing full control over all aspects of the microrelays such as spacer thickness and contact point shaping. The first component is a permalloy actuation plate with integrated gold contact points. The second piece holds the stationary contact and plated-copper spacer pedestals. The third substrate is technically not required for proper relay operation but it connects the first two pieces to large bond pads, aids in final assembly, and creates a roughly packaged device. Fabrication yields in excess of 95% are achieved with this approach. The main processing steps used to produce the three micromachined pieces are shown in figures 12-4 with the complete process included in appendix R3.

The magnetic plate with integrated contacts is fabricated on the first substrate. Processing begins by forming a release layer of hard baked photoresist. A second thick layer of photoresist is then spun, patterned and hard baked to create smooth depressions in which the contact points will be subsequently grown. A plating seed layer of Ti/Au



Figure 12-5: Photograph of the three fabricated pieces prior to assembly. From left to right is the bond traces substrate, the permalloy plate piece, and the spacer pedestal part.

(100Å/1000Å) is evaporated and a thick plating (greater than 5 microns) of gold is deposited inside a soft baked photoresist mold. The soft baked mold is removed and 10 microns of permalloy is plated inside a fresh mold patterned in the shape of a 2.8 mm x 2.0 mm cantilevered plate surround by a 1.0 mm wide frame (see figure 12-5). The completed magnetic plate structure is freed by stripping the soft baked mold, the plating seed layer and the underlying hard baked sacrificial resist. The titanium coating over the gold contacts is removed by a short dip in dilute HF. For size comparison, this permalloy piece is shown in figure 12-6 alongside the Hall effect sensor being replaced by the microrelay.

The second substrate processed contains the stationary contact and spacers that define the air gap in the assembled relay. A Cr/Au (100Å/1000Å) seed layer is evaporated on an insulating substrate (quartz or glass wafers are typically used) and 5 microns of gold are plated and patterned to form the stationary contact. The next step plates copper through a photoresist mold to form 75-micron tall spacer pedestals. This copper is "dusted" with a thin layer of plated gold to prevent oxidation. The photoresist and underlying seed layer is

**1 cm**
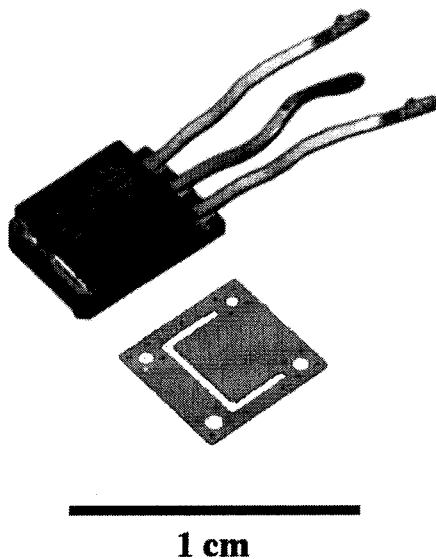
Figure 12-6: Photograph of permalloy plate piece next to the Hall effect sensor being replaced by the MMC microrelay. The sizing of the micromachined component is such that one-to-one replacement of the Hall effect device is possible.

then stripped, completing the piece.

The third and final substrate of the microrelay, while not necessary, provides solderable bond traces and an integrated alignment platform for the two pieces described above. It also caps the microrelay to minimize the debris seen by the contacts and to permit rough handling during experimental testing. From a Cr/Au (100Å/1000Å) seed layer on an insulating wafer, approximately 20 microns of copper is mold plated to form wire traces connected to four large bond pads. On these traces, an additional 20 microns of copper is plated to form alignment pegs. As with substrate two, the copper is "dusted" with plated gold before the photoresist and plating seed layer are stripped. After dicing of this wafer, the dies may be individually plated with solder which can act as the mechanical and electrical bonding agent used for microrelay assembly.

The completed assembly of the three pieces is shown in figure 12-7. During assembly, small dots of solder paste are dispensed onto the alignment pegs of substrate three. (Note: If the bond traces piece has been plated with solder this step is obviously not necessary.) The magnetic plate is then sandwiched between this piece and the second
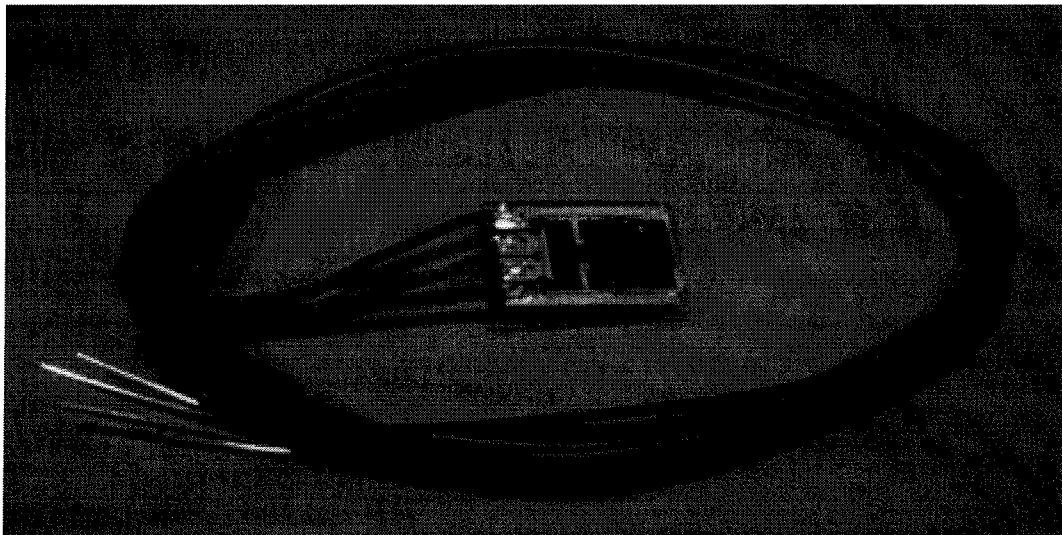


Figure 12-7: Photograph of an assembled MMC microrelay with the wires attached to its bond pads looped around it.

substrate.  Through-holes in the permalloy plate and in the spacer pedestals of the stationary contact substrate automatically align these two pieces to the pegs on the bond traces piece ensuring proper alignment of the three pieces.  The parts are lightly clamped together and heated until the solder reflows.  Upon cooling, the solder mechanically bonds the three pieces together and provides a high quality electrical connection from the contacts out to large bond pads.  Wires can be easily attached to these pads.

Four bond pads are provided for this single contact point microrelay to allow 4-wire-contact resistance measurements to be made and continuously monitored during in-situ operation.  The current is set by a load resistor and the voltge drop across the microrelay.  Using Kirkoff's voltage law, V = IR, the small series resistance of the permalloy actuation plate and the contact resistance can be determined.  The parasitic resistances of the connections to the bond pads and of cables running between the microrelay and the ohm-meter are removed with this measurement technique.

## 11.5   Three-Substrate Design Processing Notes

There are several points concerning this fabrication process that are worth mentioning.  The permalloy actuation plate can be fabricated on any rigid substrate as the completed piece is a fully freed, plated metal component.  The baking temperature of the unpatterned photoresist release layer laid down at the start of this piece should be kept as low as possible.  If ultra-baked, undercutting the millimeter-dimensioned plated structures can be very time consuming.  Of greater concern is the tendency for the metal film to slightly curl during release.  This is caused when the perimeter of the film is released long before the center is freed.  At the release layer etch front, a stress gradient from the pinned film to the freed film arises which is apparently large enough to produce a slight curl.  On examining a fully freed piece by clamping one edge rigidly, the curling produces a total deflection across the 3 to 5 millimeter structures of up to 100 microns.  The manner in

which the microrelays are assembled does remove some of this bowing and devices with good switching performance can still be produced. Zero-curl is obviously preferred. Keeping the release layer baking temperature low enough so that the photoresist can be stripped by acetone produces flat structures.

Quartz and glass wafers are the preferred substrates for the two stationary contact and bond trace pieces. In these components, the only functions of the substrates are to electrically isolate the metal features patterned on them and to define the "packaged" dimensions of the final device. Choosing transparent wafers allows confirmation and monitoring of beam actuation during in-situ operation by microscope, laser, or interferometry. Silicon is opaque to visible light and if used, device operation could only be monitored electrically. Failure to operate, either immediately following assembly or after hot-switched cycling, could only be determined by separating the three pieces. This would make diagnosis of the cause of a high make-resistance failure, for example, very difficult.

Finally a note on the removal of seedlayers and assembling with solder bonding. To strip the gold seedlayers, a selective gold etchant that does not attack the other metals must be used. Standard iodine based solutions etch copper and permalloy films more quickly than they do gold. The solder bonding of the three pieces of the microrelay allows the devices to be easily disassembled in a non-destructive fashion. Simply heating to approximately 200 °C melts the solder and allows the pieces to be easily separated. This facilitates easy access to the contact regions for wear and failure analysis.

# MMC MICRORELAY CHARACTERIZATION, EXPERIMENTAL TESTING AND CONTACT FAILURE ANALYSIS

The performance of the MMC microrelay discussed in the remaining sections cover, unless otherwise stated, devices fabricated by the three-substrate process. The majority of the testing was performed on microrelays containing gold-to-gold contacts plated in a solid bar across the tip of the permalloy actuation plate. When data covering other contact materials and contact configurations are given it will be so stated.

Characterization of the actuation forces and the electrical properties of the fabricated relay has been performed. The resulting data provide a baseline for the maximum performance that can be achieved by the devices when operating in ideal conditions. All analysis was performed in the Caltech micromachining lab on standard equipment as well as on testing setups developed specifically for these devices.

## 13.1    Actuation Plate Characterization

Recording all of the salient parameters that need to be measured in the MMC

microrelay while it is in in-situ operation is not practical.  Of particular interest are the

magnetic fields seen by the actuation plate, the force levels that these fields induce, the

contact force seen by the mating surfaces, and the manner in which these surfaces strike

one another during closure.  To ensure that the values seen by and generated in the

microrelays are reasonably close to the numbers used during the design phase, a series of

calibration experiments have been conducted to characterize the mechanical, magnetic, and

closing dynamics of the actuation plate.

### 13.1.1    Force Deflection Testing

Bending tests were performed on a static load-testing set-up assembled at Caltech

(see figure 6-8).  The instrument consists of a load cell to measure applied forces, a linear
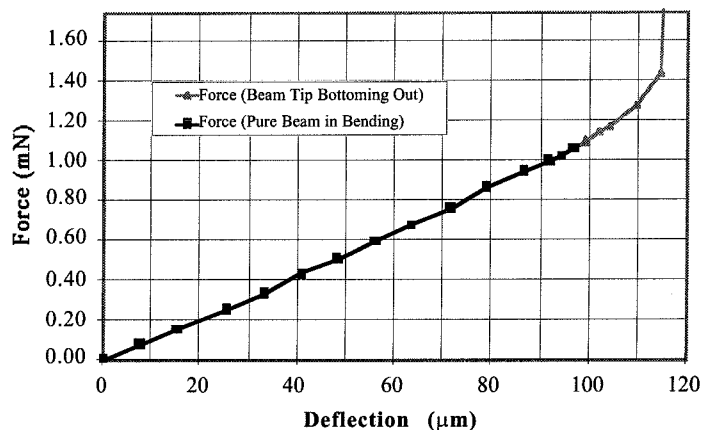


Figure 13-1:  Typical force vs. deflection data measured during static load testing.
Force was ramped up until the tip of the permalloy plate bottomed out and then was
removed.  No mechanical hysteresis is seen and the recorded response is linear, as
expected.

voltage differential transformer (LVDT) to measure z-displacement and a sharp metal pin

which contacts the sample inducing controlled deflection.  The permalloy actuation plate is

mounted in a sample holder that clamps the frame surrounding the cantilevered beam.  The

sample is mounted with the plate orthogonal to the central axis of the load cell.  A

micrometer slowly raises this assembly into contact with the immovable pin such that the

tip of the pin presses down 50 microns from the tip of the 2000-micron long plate and at

the center of its 2800-micron width.  Force as a function of load cell position, and thus

probe deflection, is then recorded.  A typical loading curve obtained with this procedure is

shown in figure 13-1 and corresponds to bending stiffness of in the z-direction of 11.1

N/m.  This data verify the linear beam-in-bending approximations made in the design phase

of the device.  The spring constant calculated from the graph is close to that predicted by
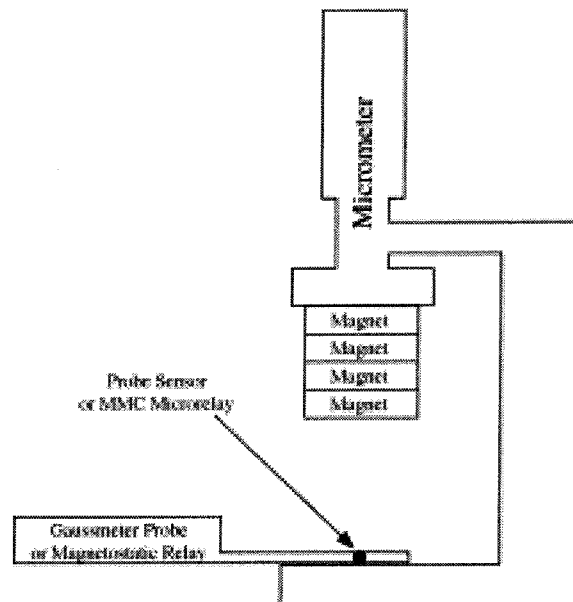


Figure 13-2:   Schematic of testing setup used to calibrate the contact resistance
versus external magnetic field strength of the MMC microrelays.

theory and results in the desired 0.5 to 1.0 millinewton range break force for assembled

microrelays employing a 75 micron contact gap spacing.

## 13.1.2   Magnetic Actuation Calibration

Characterization of the 4-wire contact resistance as a function of magnetic field

strength is performed using a custom setup shown schematically in figure 13-2.  Four high

field strength, iron-cobalt-molybdenum magnets are mounted on a large throw micrometer

that is itself attached to a rigid stand.  Initial calibration measurements of the field strength

as a function of distance of the magnet stack from the base of the stand are made with a

gaussmeter probe.  The xyz position of the active sensing element of the probe is marked

and subsequently mounted microrelays are placed such that the center of the permalloy plate

is at the same location.  At zero gap, the maximum field seen by the probe is approximately
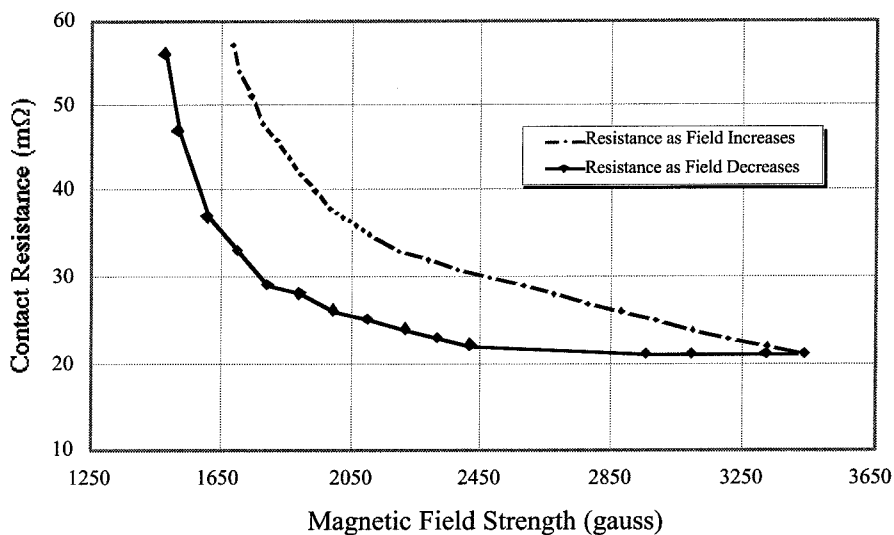


Figure 13-3:  Typical data curve measured for a three-substrate MMC microrelay showing the contact resistance as a function of external field.

3700 Gauss which is about 50% higher than the fields that should be available in the motor commutation application. The realized curve is nonlinear with the field seen at the probe being roughly inversely proportional to gap distance. This is the predicted behavior for a field emitted by a pole that diverges over a half sphere surface.

The gaussmeter probe is removed and a microrelay in mounted in the same position. The magnet stack is initially positioned at the maximum distance possible from the device. In 25 micron increments, the magnets are stepped closer to the microrelay and a 4-wire contact resistance measurement taken. The final data recorded corresponds to the point at which the magnet stack "crashes" into the microrelay. The process is then reversed to acquire contact release data as the applied field is slowly reduced. A typical curve acquired in this manner is shown in figure 13-3. For this data set, contact make occurs at an applied field of 535 Gauss with a corresponding contact resistance of 2390 m$\Omega$. Contact break occurs when the applied field falls below 529 Gauss with a final resistance reading of 3500 m$\Omega$. At 2500 Gauss, the field that will be available in the target application, the contact resistance is less than 35 m$\Omega$. This is well below the 620 m$\Omega$ maximum allowable contact resistance value set as a design parameter in table 12-1.

The force present at contact make as determined by magnetostatic actuation equation 11.1 does not agree precisely with the force-deflection data in figure 13-3 presented in the previous section. From the experimental deflection data, bending the permalloy actuation by 75 microns, the contact gap used in the microrelay, requires a force of 800 $\mu$N. The calculated actuation force generated by a 535 Gauss field is from 0.95 to 1.19 mN

(saturation magnetization is from 0.8 to 1.0 Tesla for the permalloy film).  The discrepancy is explained by the Hosaka data (see figure 10-2) in which it is shown that a contact force of approximately 100 μN is required to achieve a stable gold-to-gold contact resistance. Add this value to the 800 μN required to bend the beam and there is good agreement with the low end of calculated actuation force.  If one assumes the saturation magnetization of the permalloy film is closer to 1.0   than 0.8 Tesla, the most likely explanation for the remaining calculated vs. measured error is permalloy plating thickness variations across the face of the substrate wafer.  Since thickness is a cube factor in the bending equation, a 6.3% variation in actuation plate thickness between devices fabricated on the same substrate will cause the 20% error seen.  Plating uniformity is typically maintained at approximately 10% across a wafer making these numbers seem very reasonable.

Clearly seen in the plot is the asymptotic limit of the contact resistance.  The minimum resistance is approximately 22 mΩ and the asymptotic approach to this value is predicted by the theory in section 10.4.   Equation 10.1 describes an $R_{contact} \propto F_{contact}^{-0.5}$ relationship.  Taking the inverse square root of magnetic field (which is proportional to force) it is found that for applied fields above 2200 Gauss, the trace is linear as expected. Failure of the model below this value is attributed to the use of a wide actuation plate tipped with a contact bar.  A smooth contact sphere that forms a point contact on initial closure was used to develop equation 10.1.  Full closure of the contact strip does not occur until a field greater than 2200 Gauss is reached.  Only above this value does the additional force generated by the actuation plate contribute solely to squeezing the contacts together and thus reproduce the same conditions used for the theoretical model.

The hysteretic response of the contact resistance is attributed to adherence sticking of the gold mating surfaces. This phenomenon is not the same as welding and is covered in [106]. In short it is believed that cold-welding is taken place where small surface irregularities are squeezed together and interlock, somewhat like nano-velcro. Looking at the release trace in figure 13-3 at a field level of 1500 Gauss, the same contact resistance is maintained at a magnetic field strength approximately 250 Gauss lower than the field required to attain that value during closure. This corresponds to a 15% lower force level.

## 13.2    Contact Characterization and Performance

The ultimate measure of microrelay performance is the current and voltage switching limits and the rated electrical lifetime of the contacts. As was done with the magnetic actuation plate, a full set of experimental tests has been conducted to measure the capabilities of the contacts used in the MMC microrelay. Resistance vs. closure force has been measured directly, make and break performance has been investigated and lifetime testing performed for a range of hot-switched currents and loads. This work shows that the gold-to-gold contacts in the microrelay perform at a similar level to those seen in commercially available devices.

### 13.2.1   Contact Resistance Calibration

Contact resistance as a function of contact force is measured on the static load-testing set-up assembled used to measure the bending stiffness of the magnetic actuation

plate (see previous section). The displacement capabilities of the instrument are not used in

this case. Instead, 4-wire resistance data is collected as force is increased on the contact

bar. Sample placement on the load cell is the same as with the permalloy actuation plate.

For this test, the bond traces substrate (piece 3 of the three-substrate design) was removed

to provide the instrument with access to the beam. Testing was initiated with the actuation

plate deflected to the point where the solid contact bar along its tip was just shy of touching

the stationary contact.

A typical contact resistance vs. contact force data set collected in this manner is

shown in figure 13-4. Not shown on the graph is contact make and break which occurred

at 1.27 mN (1042 m$\Omega$) and 1.245 mN (334 m$\Omega$), respectively. As with the resistance data

collected using magnetic actuation, the curve exhibits hysteresis upon release. This data

shows that at the designed contact closure force of 5 mN, the contact resistance is 30 m$\Omega$.
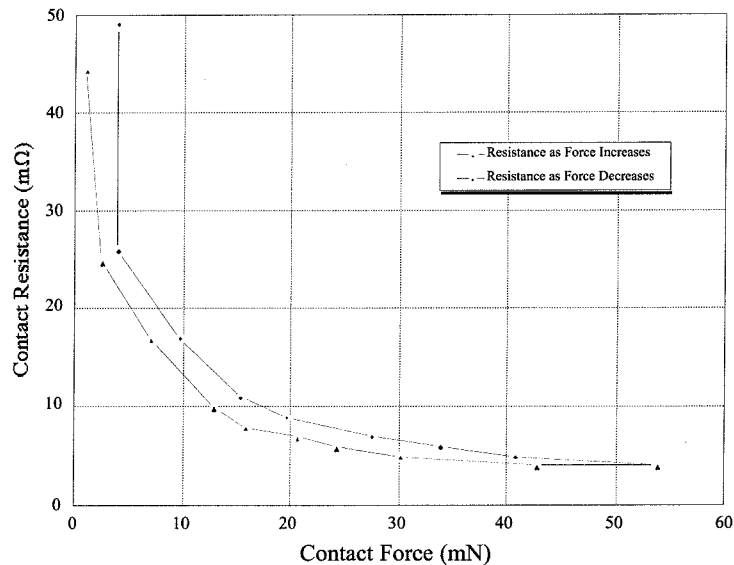


Figure 13-4: Typical data curve generated for contact resistance as a function of contact force up into the millinewton range.

This agrees well with the less than 35 m$\Omega$ value attained in the magnetic actuation test.

## 13.2.2   Lifetime Testing Setup

Lifetime measurements of the MMC microrelay require the construction of a custom testing setup. Generating a 2500 Gauss field electronically requires an electromagnet with a high-turn wire coil that can pass several amps. Assuming this is available, switching ampere-level currents at 100 to 1000 Hz requires a very capable (i.e., very expensive) power supply. If this, too, can be procured, the ability to saturate and quench such large fields at such frequencies is still not a trivial matter.

To avoid all of these problems, a testing setup composed of a scavenged DC motor, a shaft extender, two flat faceplates, and 16 high-external-field, iron-cobalt-molybdenum magnets was constructed. This setup is shown in figure 13-5. Four pairs of magnets are epoxied to each of the two faceplates and are spaced 90° relative to one another. The shaft extender is attached to the axle of the motor and the first faceplate with the embedded
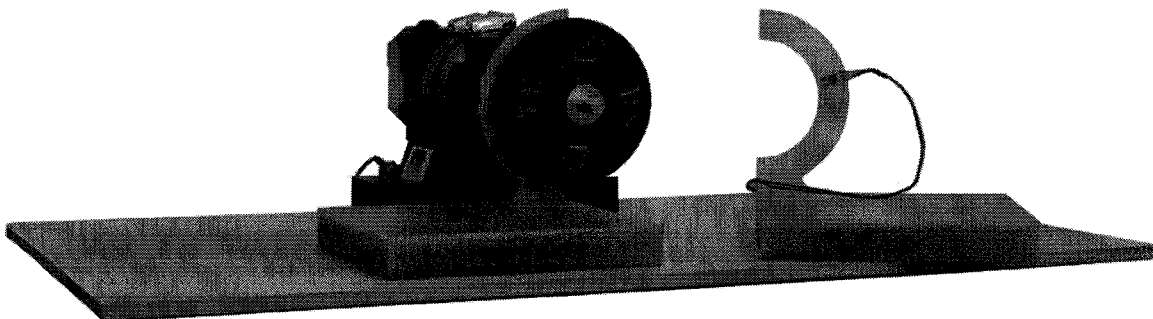


Figure 13-5: Testing setup used for the lifetime testing of the MMC microrelays. The instrument consists of two plates, each containing four high-strength magnets, attached to the axle of a DC motor. The relays are attached to a fiberglass stand and slide between the two plates during testing.

magnets is slipped onto it followed by a number of spacer washers. The second face plate

is then put into place and locked into position such that its magnets line up with the magnets

on the first plate. This creates a strong, uniform field of approximately 2800 Gauss in the

space (set to $\approx$ 1 cm) between the two plates. Applying DC power to the motor rotates

these magnets at up to 2000 RPM. With four magnets passing a fixed point per revolution,

this setup generates a roughly square waveform, varying magnetic field at frequencies up to

133 Hz. The diameter of the faceplates and the size of the magnets result in the magnetic

waveform having an on-duty-cycle of 37%.

For testing, an MMC microrelay is attached to a non-magnetic holder and set in

place in the gap between the faceplates. The device is positioned so that its actuation plate

is oriented with an angle $\theta$ (see equation 11.1) of approximately zero and so that the end of
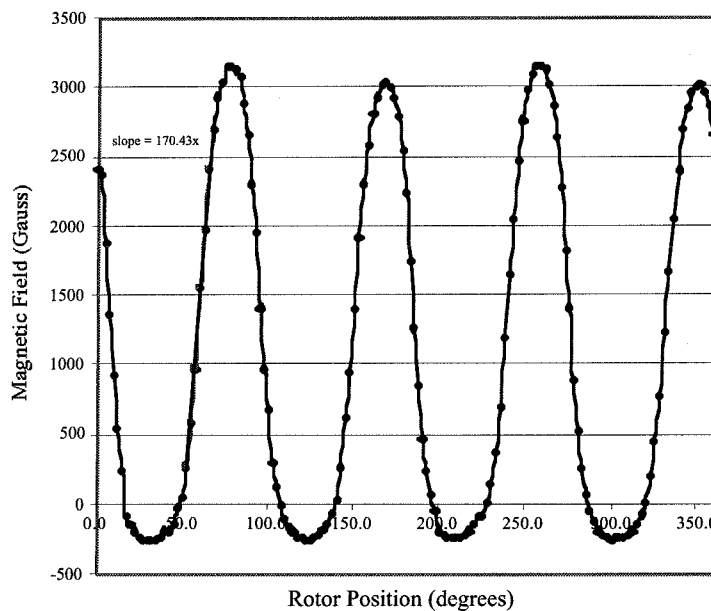


Figure 13-6: Magnetic field seen by an MMC microrelay during lifetime testing in the experimental setup shown in figure 13-5.

the plate is tangential to the arc traced out by the permanent magnets as they are rotated by the motor. The magnetic field seen by the relays in this placement is shown in figure 13-6.

### 13.2.3   Make and Break Performance

Using the lifetime testing setup, the make and break performance of the MMC microrelay has been investigated. In neither case is any evidence of contact bounce seen. This my be the nature of the device itself or could be due to the fact that the transition from zero field to maximum field produced by the rotating magnets is not truly binary. The field seen by the microrelay ramps up and down allowing "soft-switching" to occur; i.e., the beam is not snapped down and abruptly released - rather it is pulled down and released in smooth continuous motion. Since this is the same manner that the devices will see in their target application, this method of testing is deemed more appropriate than a system that could generate a true square magnetic waveform.
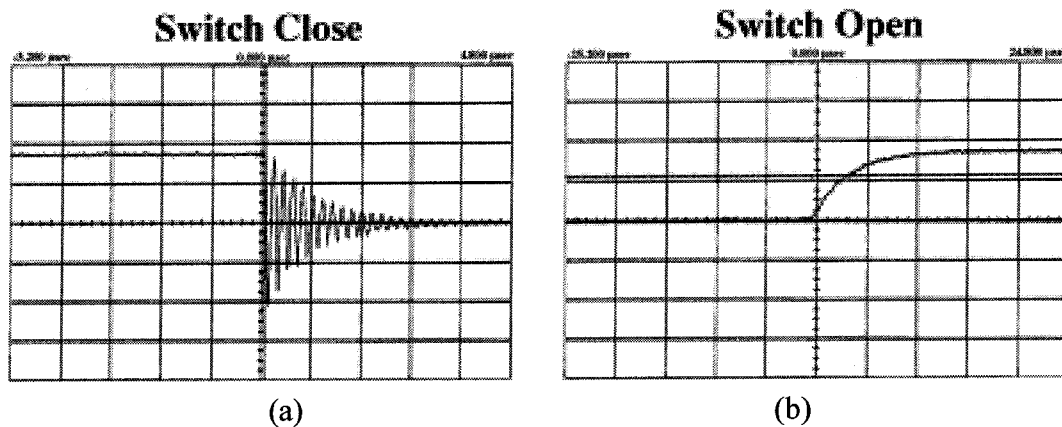
Figure 13-7: Traces detailing the quick and clean, opening and closing action of the MMC microrelays during operation.

Figure 13-7 are scope traces captured during make and break, respectively. The oscillations seen in 13-7.a and the exponential rise time in 13-7.b are artifacts of parasitics in the circuit used to capture the waveforms and are not due to the microrelay itself. Looking past this noise, it can be seen that the time to make and break electrical contact is measured in microseconds. Note that due to the "soft-switching" of the microrelays, this is not the actual speed at which the devices open and close but rather a measure of how cleanly the mating surface connect and separate. This good performance is seen at > 130 Hz which is the upper limit of the rotational speed (4 x 1200 RPM) of the testing setup.

### 13.2.4  Lifetime Testing Performance

Testing of the MMC microrelays to failure at various currents and loads was conducted to determine the lifetime of the devices. All tests were conducted under hot-switched conditions at 100 Hz with 28 VDC across the contact gap. With resistive loading, currents of 0.1, 100, 250 and 500 mA were hot-switched until contact failure occurred. Failure was defined as an uncontrolled on-condition due to welding or high-contact resistance at closure. Here, high-contact resistance was defined as 1.24 $\Omega$ which is two times the acceptable maximum resistance (620 m$\Omega$) as defined during the design phase of the project (see table 12-1). Continuous monitoring of switching performance was not conducted during these tests as an automated setup was not available. Rather, the setup was attended for the first 1 million cycles (3 hours) with the voltage drop across the microrelay monitored on an oscilloscope. If failure had not yet occurred, the setup was left

unattended for the next 1 million cycles and then monitored for 15 minutes.   If no

degradation in performance was seen, this procedure was repeated until 10 million cycles

were complete.   If contact resistance was still in the acceptable range, monitoring was

reduced to one 15 minute period per day (100 Hz => 8,640,000 cycles/day) until failure

occurred.

Lifetime performance results for the MMC microrelays is presented in table 13-1.

The 0.1 mA switching data shows that the mechanical life of the devices is greater than 500

million cycles.   No degradation in switching performance or contact resistance was seen

during this test which was arbitrarily terminated after two months of testing.   For the tests

conducted with higher level currents, signs of impending failure begin to appear at

approximately 90 to 95% of the lifetime cycles noted in table 13-1.   Initially very infrequent

"stutters" begin to appear on the oscilloscope trace monitoring the voltage drop across the

microrelay terminals.   This trace is a square wave with the relay ON-state represented by

| MMC Microrelay Lifetime Testing Results | | |
|---|---|---|
| Load Switched | Current (mA) | Lifetime (cycles) |
| Resistive (28 VDC) | 0.10 | > 500 million |
| Resistive (28 VDC) | 100 | 1 to 10 million |
| Resistive (28 VDC) | 250 | 0.1 to 1 million |
| Resistive (28 VDC) | 500 | 0.01 to 0.1 million |
| 4.2 mH Inductive | 250 | 0.01 to 0.1 million |
| Motor Commutation | 80 to 120 | > 30 million |

Table 13-1:   MMC microrelay hot-switched lifetimes for a range of operating currents and conditions.

zero volts and the OFF-state by 28 volts.  The "stutters" are brief ($<$ 5% of the total ON time) spikes to 28 volts.  As cycling continues to wear the contact, the "stutters" turn into "dead zones" which are 10 to 30% of the total ON time.  When the "dead zones" become greater than 30% of the ON time, microrelay failure is declared.  Often, the transition from "stuttering" to 100% OFF occurs in less than 1% of the total lifetime cycles of the device. For a device lifetime of 5 million cycles, the time to cover 1% and 10% of the total cycles is 0.13 and 1.3 hours, respectively.

Failure due to welding when hot-switching resistive loads is seldom seen. "Stuttering" and "dead zone" failure are caused by the formation of high resistance zones along the contact area and spike-and-crater contact wear (see section 13.3).  Typically, the contact resistance of a microrelay run to failure is several megaohms.  Welding, while still not the dominant failure mode, is seen more often when switching inductive loads.  This suggests greater contact melting, possibly due to higher temperatures created by arcing.

As expected, lifetime is dramatically reduced at the higher current levels.  Failure rates above 100 mA are so quick that the microrelays with gold-to-gold contacts have little practical use in the target application at these currents.  At 100 mA and below, the performance of the contacts is found to be similar to the specified lifetimes of commercially available devices that utilize the same contact material [110].

## 13.2.5   Lifetime Performance Under Special Conditions

Additional testing has been conducted with inductive loads, multi-fingered multiple contact configurations, and rhodium-to-rhodium contacts.  The quantity of data collected

for these conditions is limited due to the time consuming nature of the measurements.  As such, the results included in this section should be considered as quantitative data that has not been statistically confirmed.

As noted in table 13-1, the addition of a 4.2 mH inductive load reduces microrelay lifetime to that of a resistive load hot-switched at twice the current level.  This indicates that contact wear due to inductive arcing is significant in these devices.  Adding by-pass zener diodes and/or resistor-capacitors to the test circuit increases inductive load lifetimes to approximately 75% of that found for pure resistive switching.

A number of contact configurations have been explored with the most promising being a multi-fingered actuation plate tip with multiple discrete contact points.  Gold-to-gold contacts are again used but rather than being a solid bar running the width of the 2800-micron wide actuation plate, the bar is patterned into 50-micron square points spaced on 70-micron centers.  Additionally, the end of the actuation plate is patterned into 200-micron
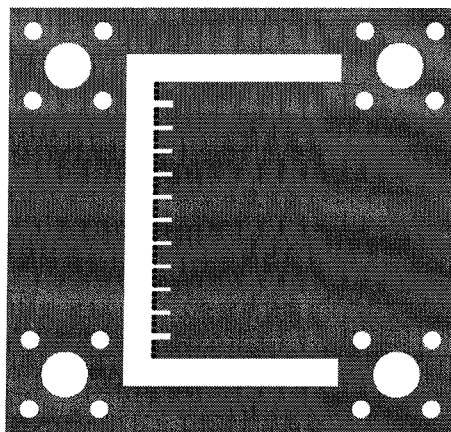


Figure 13-8:  By patterning the end of the actuation plate and subdividing the contact bar into many discrete contact points, a qualitative increase in microrelay lifetime of 3 to 5 time is seen.

wide, 200-micron long "fingers." Each finger holds three contacts for a total of 36 contact points (see figure 13-8). In lifetime tests with 100 mA hot-switched resistive loads, this contact configuration appears to extend microrelay life by 3 to 5 times.

For rhodium-to-rhodium contacts, a static contact resistance attained by a 2500 Gauss field is between 200 and 300 m$\Omega$. Resistive load testing at 100 mA hot-switched current levels indicates that this harder, higher temperature material extends microrelay life by 8 to 15 times over Au-to-Au. The multi-finger, multi-contact configuration discussed above was not tested with Rh-to-Rh contacts. Assuming such patterning could increase this performance by 3 to 5 times as is done with Au-to-Au contact material, the resulting 24 to 750 million electrical lifetime would allow these microrelays to be used in a wide range of space qualified flight hardware.

## 13.2.6   Zip-Lock Contact Closure

The arc traveled by the field producing permanent magnets closes the contacts in a unique, zip-lock fashion. As noted in the discussion of the experimental setup, the line defined by the end of 2800-micron wide actuation plate is positioned tangential to the arc traced out by the magnets attached to the shaft of the motor. This results in one corner, then the center, and then the final corner of the actuation plate being exposed to the leading edge of the actuating external magnetic field. The result is that the end of the beam "zip-locks" down as the magnet moves by; i.e., the leading corner strikes the stationary contact first then, in a continuous fashion, the rest of the armature contact is pulled down until

finally the trailing corner mates with the stationary contact. A similar "un-zip-locking" mode is seen on contact release. The ramifications and possible benefits of this mode of closure are discussed at the end of the following section.

## 13.3    Contact Failure Phenomena

Examination of the microrelays after they are driven to failure shows evidence of melt, splatter and redeposition of metal from one contact to the other. As mentioned above, the devices utilize a beam-wide bar, not a point, for their contacts. Minor irregularities along the length of the bar give rise to increased wear zones along the mating surfaces. The zip-lock mode of contact closure generates the greatest amount of wear at the corners of the plate. Evidence of considerable contact melting is readily apparent in these areas. Melt and redeposition of contact material produces a number of contact wear patterns seen in
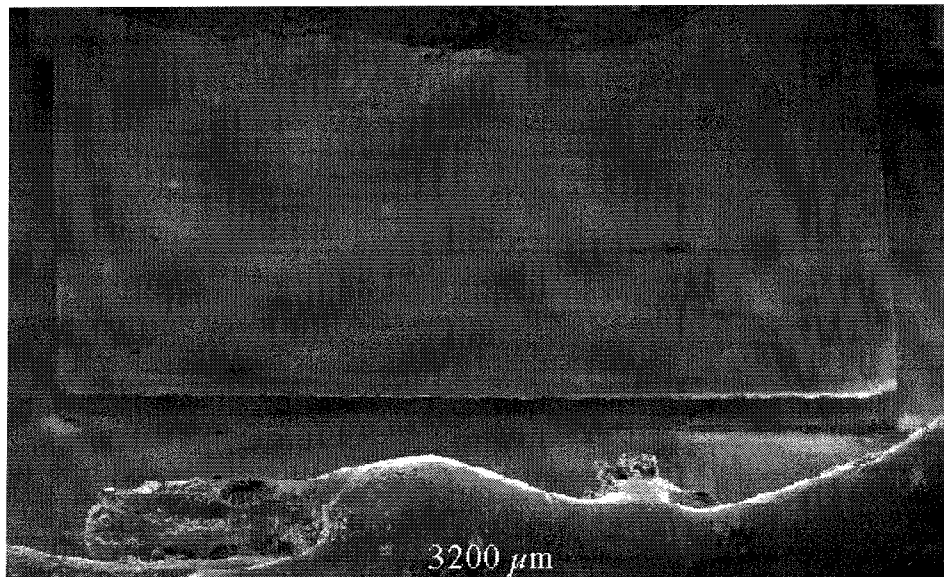


Figure 13-9: Entire width of contact bar region showing the contact wear points at very low magnification.

macroscale devices as well as some unique to micromachined relays. Sprayed out from these regions are debris fields that are attributed to contact material splatter. Particles in the areas can be tens of microns in diameter. The following looks at a single microrelay that has been examined by SEM and points out the various failure phenomena seen. To this
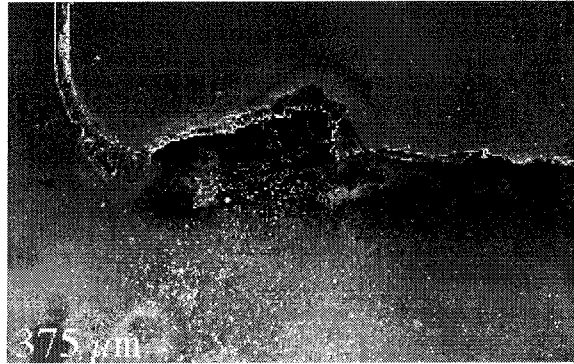


(a)
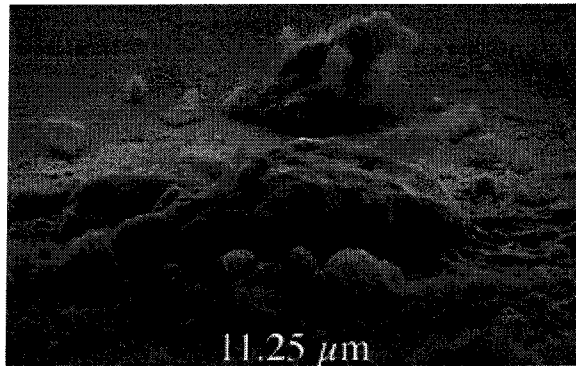


(b)
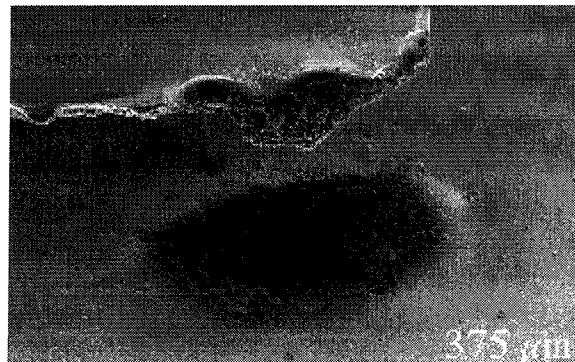


Figure 13-10-A,E: High magnification images of the contact wear in regions A and E.

end, a relatively low magnification photo showing the entire 2800-micron wide contact region is shown in figure 13-9. The dotted circles denoted A through E indicate the specific portions of the contact strip that are discussed below.

## 13.3.1 Contact Wear Features

Regions A and E focus on the left and right corners of the actuation plate, respectively. Higher magnification SEM photos are shown in figure 13-10-A,Ea, 13-10-A,Eb & 13-10-A,Ec. The corners show classic spike-and-crater contact wear as discussed in section 10.6. Surrounding these structures are debris fields composed of particles up to tens of microns in diameter (see figure 13-10-A,Ec). The micro-rubble extends as far as several hundred microns away from the actual contact mating area.

Region B shows a microrelay wear phenomenon denoted as punch-through. Photos at two magnifications are shown in figure 13-10-B. In an MMC microrelay the stationary contact material lies on a rigid substrate that is electrically insulating and has relatively poor thermal conduction. The punch-through feature is thought to result from a combination of high local electric field, material melt and splatter, and material property discontinuities at the contact-substrate interface. It appears that conditions arise that creates an arc discharge. The arc is sufficiently concentrated to allow it to blast through the contact material until it is terminated by the insulating substrate. The intense heat generated by the discharge melts and probably boils the region producing a micro-explosion that creates a hole through the thickness of the stationary contact material. No mention of such a wear

feature has been found in literature covering macroscale relays. In macroscale relays the

contacts are solid metal, even though the actual contact material thickness is only several

microns thick.

Trenches hundreds of microns long and extending down to the insulative substrate

are evident in the stationary contact in region D (see figure 13-10-D). These structures
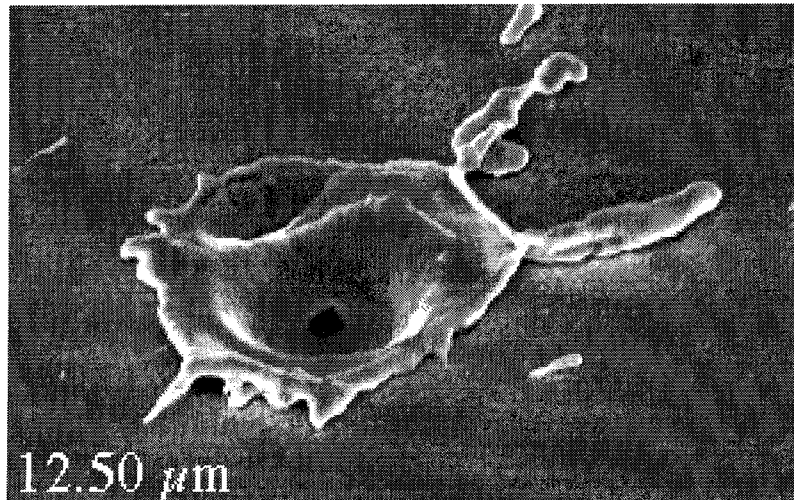


(a)
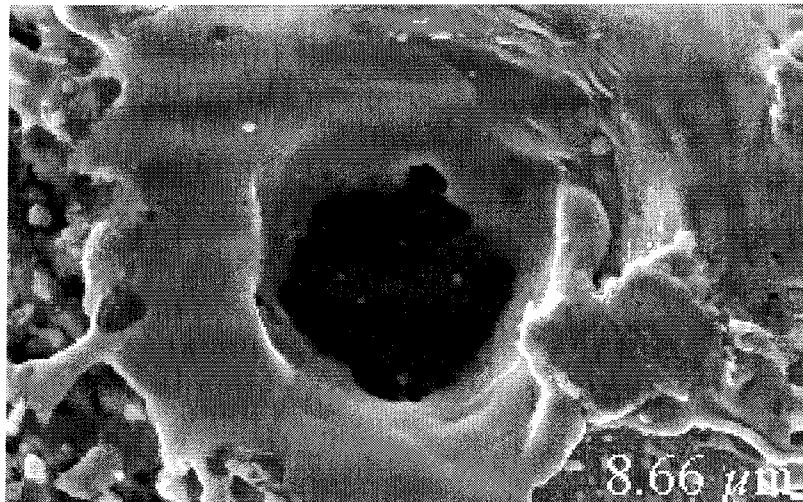


(b)

Figure 13-10-B: High magnification images of the contact wear punch-through
phenomena found in regions B.

explain the high contact resistance "sputter" and "dead zone" performance seen in lifetime testing. The large areas of melted material clearly illustrate that local heating can easily generate conditions that can lead to contact welding. Regions like these are suspected to be the main mode of failure of the microrelay at high, hot-switched current levels. As with the punch-through phenomenon, this is believed to be a form of contact wear unique to
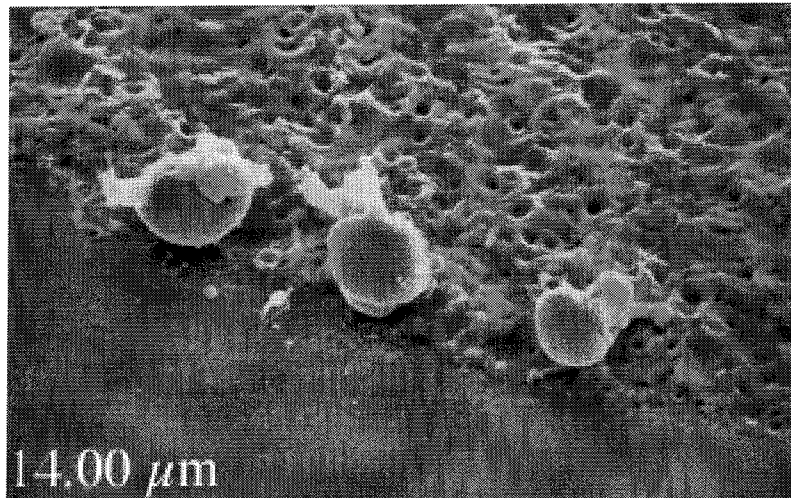
(a)
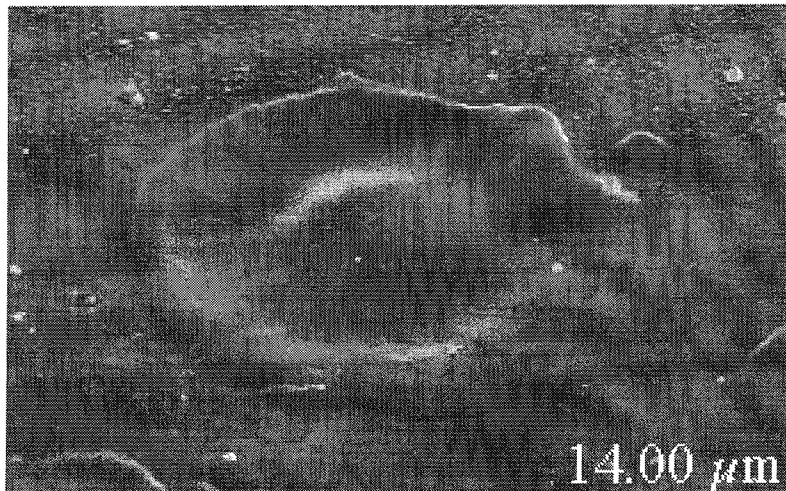
(b)

Figure 13-10-C: High magnification images of the less severe contact wear seen in region C.

microrelays that arises from the presence of an underlying insulating substrate.

The close-ups of area C shown in figure 13-10-C display the transition region from the high contact wear zones seen at the corners into the near wear-free surfaces that characterize the center of the plate-wide contact strip.   Photo 13-10-Ca shows the inner edge of region D where significant melt is occurring but at a low enough level that the underlying substrate is not exposed.  Note the three somewhat spherical balls at the edge of the melts.  These indicate that the gold has been liquefied and pushed/splattered out of the contact "squeeze" zone.  The SEM in 13-10-Cb is still closer to the center of the plate.  This feature shows an area of contact material that has been heated enough to make the metal readily malleable but not so much that it has become liquid.  It is believed that this feature is caused by stiction of a high point on the mating portion of armature contact.  As the tip of
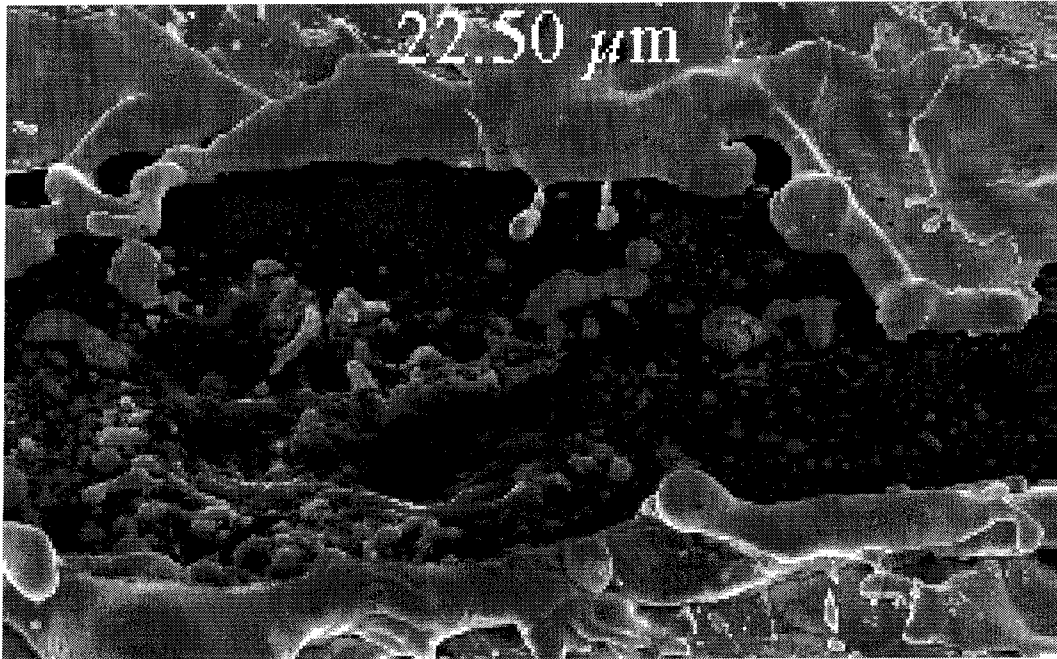


Figure 13-10-D:  High magnification images of the high melt zones seen in region D that has exposed the underlying insulating substrate.

the actuation plate pulls away from the stationary contact, the softened gold film is pulled

up from its substrate until tension in the metal overcomes the stiction force at the Au-to-Au

interface.  The pulled zone cools as it falls back to the substrate and solidifies into a "pond-

ripple" feature before it can fully flatten.


## 13.3.2   Multiple Contact Material for Improved Contact Wear

The high contact wear seen at the corners of the actuation plate and the relatively

wear-free region through the center suggest the cause of, and perhaps the cure for, MMC

microrelay failure.  At first glance, the wear at the corners is attributed to the concentration

of electric field at these "sharp" geometries leading to a greater probability that an arc

discharge will occur there.  This type of wear, however, is seen in devices used to switch

both inductive and resistive loads.  Since arcing should be minimal for resistive loads a less

obvious cause is suspected.

The zip-lock manner in which the contact surfaces come together is the likely source

of high contact wear at the corners.  One corner initiates every closure.  The second corner

completes every separation.  As discussed in chapter 10, the current crowding through the

extremely small contact area present for a split second during contact make and break can

easily heat the region to the point where the contact material can melt and boil.  The fact that

the armature of the MMC microrelay touches down with a "sharp" geometry feature first

only exacerbates this phenomenon.  Once a good portion of the contact strip is closed, the

current crowding is alleviated and contact wear due to heating stops.  From figure 13-10

this happens at about 30% closure. This accounts for the relatively undamaged gold throughout the central range of the contact strip.

The uneven wear pattern could be looked upon as something to be eliminated. If one were to attempt to eliminate this wear pattern, the first thing to try would be to mount the microrelay in the motor so that the entire width of the tip of the actuation plate sees the same magnetic field at all times. This, theoretically, will pull the armature down such that the entire length of the contact strip mates all at once. In practice this will never be achieved. Other logical changes involve redesigning the structure to eliminate flexure across the width of the plate. Again, this will be difficult and much time, effort, and money will be spent trying to attain a near-impossible goal.

Viewing the uneven wear pattern as an advantage (it's not a bug, it's a feature!) leads to a new and exciting solution that is probably only cost effective in a micromachined relay. Different contact materials can be used in the differently worn sections of the contact strip. As an example, the corner areas could be tungsten, the transition regions could be platinum and the central region could continue to be gold. The composite contact will produce a microrelay with all of the beneficial traits of each material while avoiding their drawbacks. Take the case of contact closure. The hard, high-temperature tungsten will handle the harsh make and break conditions seen at the corners. As the contact zip-closes further the lower temperature but higher conductivity platinum will begin to take up the current load from the high resistivity tungsten. The platinum can easily handle the lower, but non-zero heating rate and arc-free condition present at this time. Once the contact has

closed to the point where heating due to current crowding is no longer present, the gold contact region comes into play and provides the microrelay with a minimal contact resistance. While such a composite contact would be very difficult and expensive to implement in a macroscale relay, micromachining technology can easily integrate it into the microrelay.

Time pressures and other interesting research projects did not permit this idea to be pursued. Perhaps for the next Ph.D.

## 13.4    DC Brushless Motor Commutation

Proof-of-concept DC brushless motor commutation has been demonstrated. Three MMC microrelays have been mounted to a space qualified motor and testing performed.
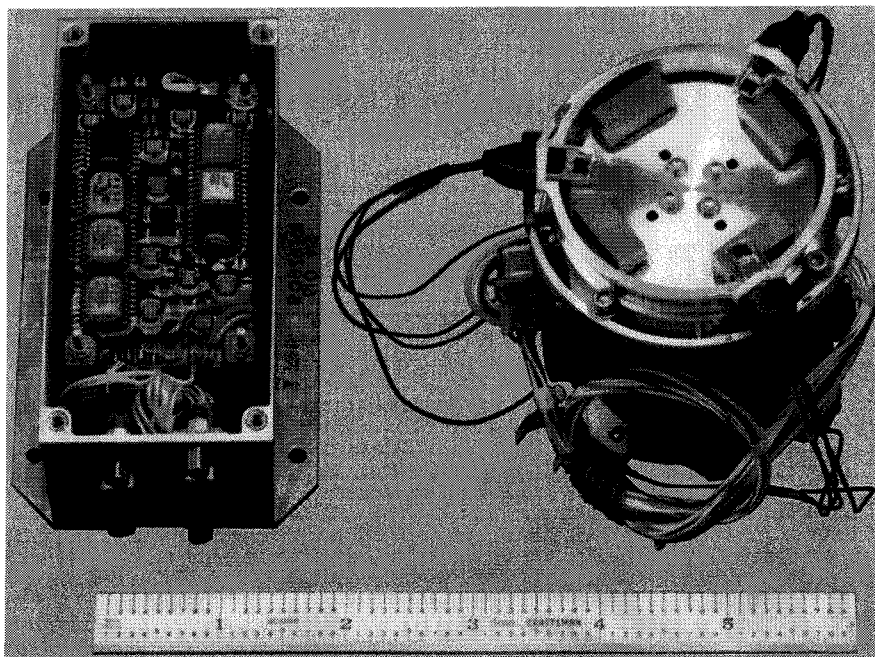


Figure 13-11: MMC microrelay prototype commuation system mounted on the housing and axle of the target motor.

Successful commutation at the maximum motor specification is shown. Proper operation in vacuum and at cold temperatures is confirmed.

### 13.4.1  Experimental Motor Platform

The target motor with three MMC microrelays mounted on its housing is shown in figure 13-11 next to the commutation electronics box being replaced. To simplify mounting, the relays are not installed inside the motor as they would be in space qualified hardware. As such, the motor magnets can not be used as the source of the actuating external magnetic field. Instead, four permanent magnets that generate fields comparable to the motor magnets (approximately 2500 gauss) are attached to an aluminum plate that is mounted to the motor shaft. Fixed to the motor housing, the three relays are positioned at 120-degree intervals around its perimeter so that they extend over the magnets. Figure 13-
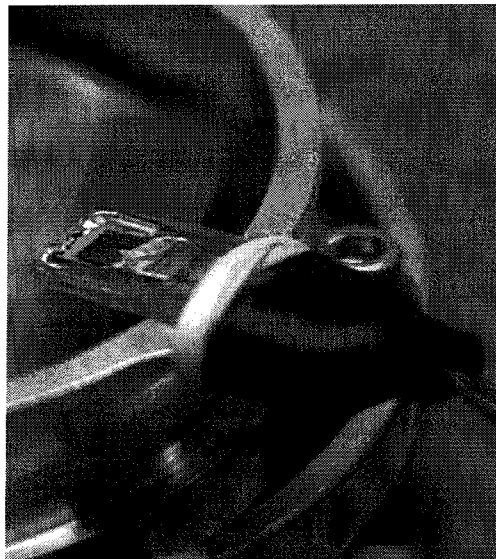


Figure 13-12: Close-up showing an MMC microrelay hanging over the edge of the motor housing as one of the magnets attached to the rotor approaches.

12 (close-up of relay on housing) shows a close-up on one of the mounted relays.  With the motor turning, fine alignment of each relay is performed until the torque ripple of the motor is minimized.

### 13.4.2  DC Brushless Motor Commutation

Validation of the magnetostatic MMC microrelay commutation system was achieved with the successful commutation of this three phase, four pole DC brushless motor.  Initial operation utilized no arc suppression circuitry to protect the microrelays from the large voltage spike associated with switching the approximately 8 mH inductive load of the motor windings.  Regardless, intermittent testing over the course of a day demonstrated commutation of the motor up to its maximum rotation speed of 1200 RPM and up to the maximum winding current of 450 mA.  This demonstration of was followed by several days of continuous motor commutation at 6 VDC/50 mA.  These relays were removed before failure for evaluation of contact wear.

Lifetime and relay performance testing has been conducted under a range of environmental conditions.  For these tests, the current switched was kept between 80 to 120 mA and suppression circuitry was added to eliminate inductive arcing.  This was done to explore the maximum lifetime of a useful MEMS commutation system for space applications.  Continuous commutation led to microrelay failure by a high-impedance, uncontrolled-OFF condition of one of the relays after more than 30 million switching cycles.  Figure 13-13 shows a typical switching trace for one microrelay as it commutates

the motor. Note the sharp transitions as the relay opens and closes. No contact bounce is evident during make and break. The spikes seen on the scope trace are voltage transients produces as the other two microrelays make and break the current into their corresponding motor windings.

The microrelays have successfully commutated the motor in space-like conditions. Using an environmental chamber, pressure was decreased to less than 5 microtorr with the motor turning. No change in performance was noted. Back at atmospheric pressure, the temperature was decreased to below freezing. At -25 °C the motor began to slow and finally seized at -30 °C. The chamber was then warmed with power still applied to the motor. When the temperature reached between -25 to -20 °C normal motor operation
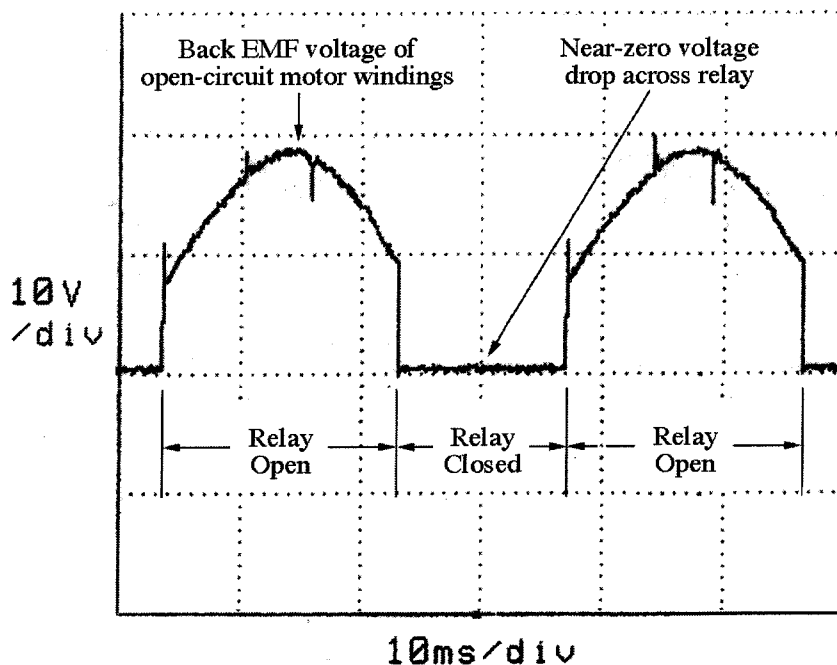


Figure 13-13: This scope trace shows the voltage across a relay as it commutates a motor. No contact bounce is seen during make and break. The spikes on the back EMF waveform are transients produced as the other two motor windings are switched on and off.

resumed.  It is believed that "freezing" of the axle lubricant and not to any failure of the MMC microrelays caused the motor seizure.

## 13.5    MMC Microrelay Conclusion and Future Work

As a whole, the performance achieved by the gold-to-gold contact MMC microrelays is satisfactory but not outstanding.  The electrical lifetime of 30 million 100 mA hot-switched cycles permits continuous motor commutation at 400 RPM for up to 2 weeks. This level of performance is adequate for many space applications such as deployment of high gain antennas, opening dust covers that protect light apertures during launch, and short lifetime microrover missions.  For more aggressive applications such as long-life rover missions, sample drilling and extraction, and mini-submarine propulsion, more robust devices must be developed.

The next step in this work is to explore a range of contact materials, contact configurations, and multiple material composite contacts.  Initial qualitative results suggest that at least an order of magnitude improvement in lifetime can be achieved.  With proper development, two orders of magnitude should be realizable.  If the multiple material composite contact approach is as successful as is hoped, lifetimes three orders of magnitude longer than the gold-to-gold contact presented here may be achievable.  This would allow motors to operate continuously for 35 years.  Such microrelays would be fantastic with near-endless applications.  Even the 3.5 year life achieved with just two orders of improvement is very useful.

Finally, miniaturize, miniaturize, and miniaturize.  The microrelays presented here are quite large by typical micromachining standards.  Reduction in device area is a must if these components are to be used in future motor designs.  The present fabrication process will need to be modified slightly but not substantially.  The most notable change will be to separate the mechanical bending forces from the magnetic actuation forces.  This is readily accomplished by moving away from cantilever bending to torsional flexure.  This one alteration should allow microrelays with the same actuation forces to be produced with a footprint of less than 1 square millimeter.

Further development is left to the casual micromachinist.

# CHAPTER
# 14

## VARIABLE-RELUCTANCE ELECTROMAGNETIC ARMATURE MICRORELAYS

The family of microrelays presented in the following chapters has been developed to demonstrate that conventional relay technology can be miniaturized through the use of micromachining fabrication technology. The macroscale configuration chosen for reproduction as MEMS devices is commonly referred to as electromechanical armature relays. Initial target applications include low to moderate level current switching at DC to RF signal frequencies. These devices operate on the variable reluctance actuation principle discussed in section 14.3 that allows the contact forces generated in the switches to reach into the millinewton level. Passing current through a fully integrated planar coil provides the actuation energy. The unpackaged volume of the microrelays realized in this research is less than 1/100th that of their smallest reported [76, 113], packaged macroscale brethren.

The MEMS approach to fabricating armature microrelay aims to simplify production,

eliminate assembly and improve performance. In doing so and by doing so, smaller, less costly devices that have tighter tolerances, fewer parts and lower power consumption can be realized. Manufacturers of the next generation, high-end electronic products require smaller and smaller subsystems for their designs. At the same time they are demanding that these modules be faster, better and cheaper. A fully integrated MEMS microrelay can be batch-fabricated with many thousands of devices produced on a single substrate. Economies of scale hold the promise that the cost per microrelay will fall sharply once a process flow is finalized and put into production. All of the devices will be fabricated at the same time and require no individual component assembly steps. The results will be components with tighter part-to-part tolerances and less variable performance characteristics. The very fact that the MEMS microrelay is in fact a single monolithic module decreases total part count to just one. This alone promises great improvements in overall reliability.

Relay design, fabrication and testing is presented. Electroplating and low temperature insulators form all of the constituent pieces of the relay. The process design is compatible with a large variety of starting substrate though only silicon is explored. The mechanical and electrical performance of the resulting microrelays is fully characterized and lifetime testing is performed. After being switched to failure, the devices are taken apart and the failure mode analyzed. Finally, overall performance of a microrelays is assessed and future avenues for the development of higher performance designs are discussed.

## 14.1    Motivation

Electromechanical relays are widely used in applications requiring high off-resistance, low circuit parasitics, and economical switching solutions. As mentioned in the general introduction to relays in chapter 8, many of the functions traditionally employing relays are being co-opted by transistors due to their much better lifetimes and ease of operation. In many cases, particularly in the switching of high powers and high frequencies, transistors just do not have the performance capabilities required. Often, if a semiconductor device can be used, it is much too expensive. The excellent performance and typically low cost solution that is provided by relays under these situations can many times be the only option that is available to an engineer.

Conventional production techniques do not readily permit the miniaturization of electromechanical relays down into the millimeter and submillimeter dimensions. Manufacturers are struggling to extend the capabilities of their production lines to allow the next generation devices to be produced without a major retooling of their factories. The packaged dimensions being sought are approximately 9 mm x 6 mm x 5 mm [113]. This is being accomplished but typically by moving to highly automated, very costly assembly machines. Suggest to a floor manager that he will need to improve the capabilities of the line to a level where it can produce relays with dimensions of 1 mm x 2 mm x 0.5 mm and expect to be met with a stream of hysterical laughter.

This is not to say that producing a micromachined armature relay is straightforward. The equations governing the operation of this new class of devices are much different than

those which describe the MMC microrelays and must be developed seperately. Additionally, the actuated element in the armature design introduces additional complexities for which beams-in-bending theory is needed in order to understood their effects. Finally, processes for depositing insulation at low temperatures must be examined and added to those techniques presented in section 14-6 through 14-8. The following sections detail this additional information that is required for the design and fabrication of a successful armature-type MEMS microrelay.

## 14.2    Armature Microrelay Actuation

Design of an electromagnetic relay requires that the mode of opening and closing of the contacts be fully understood. In electromechanical relays, contact make and break is achieved using forces temporary magnetic fields generated by in the device. The armature microrelay actuation is based on a variable reluctance, electromagnetic circuit. Energizing a coil wrapped around a magnetic core generates a magnetic field that is focused at a gap. The forces that arise in this region act to close a set of mating contacts. When this circuit is deactivated, the force for contact separation is provided by mechanical energy stored in a cantilever beam that is deflected during closure. In determining the force level available in the device, special attention must be given to the design of the magnetic structures. Due to the processing limitations imposed on certain micromachined structures, assumptions used to simply the force equations applicable to macroscale relays do not necessarily hold in their magnetic MEMS counterparts.

## 14.3     Variable-Reluctance  Relays

Variable-reluctance actuation is a magnetic property used widely in the fabrication

of relays.  Typically used in the class of devices called armature relays, a schematic of a

macroscale device is shown in figure 14-1.  At the heart of the actuator is a u-shaped core

of high permeability, soft magnetic material.  Wound around this core is a wire coil with a

high number of turns.  Across the ends of the u-shape is an armature, also made of soft

magnetic material, that is free to pivot about one end.  Attached to the armature near the

pivot point is a mechanical spring.  Fixed in the other end of the armature is the moving

contact point.  Beneath it, set in the packaging of the relay, is the corresponding stationary

contact point.  The gap between the armature and the magnetic core at the pivot point is

designed to be very small and to have a large cross sectional area.  In contrast, the

armature-to-core gap near the contact points is relatively large and its area relatively small.

Special attention is given to the design of the area of this region of overlap as the geometry
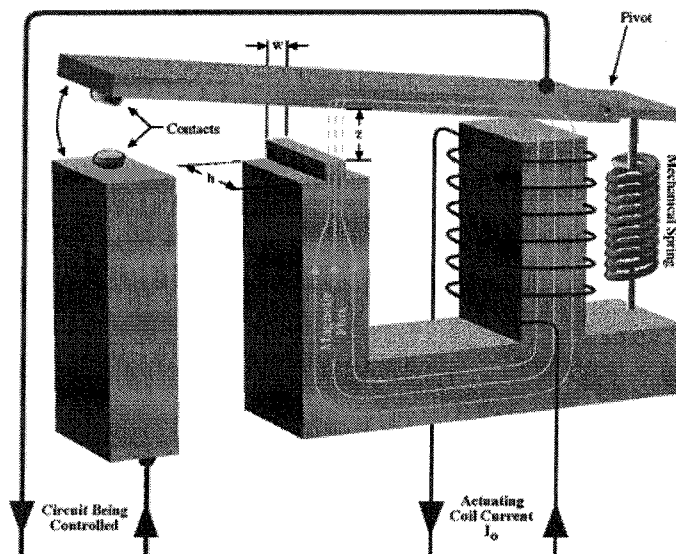


Figure 14-1:  Drawing denoting the important parts of a conventional armature relay.

of this gap defines the ultimate contact force achievable by the relay. Together, the core, armature, coil, and the two gaps are referred to as the magnetic circuit of the relay. During operation, the force generated on the armature during closure arises from a variance in the reluctance of the magnetic circuit - hence the term variable-reluctance actuator.

## 14.3.1 Variable-Reluctance Actuation Concept

When current is passed through the wire coil, it produces magnetic flux that is concentrated in the u-shaped core that it surrounds. The high permeability magnetic material comprising the core contains and magnifies the flux and directs it down the armature and into the gap region. It can be shown (see section 14.3.2 below) that a closure force is generated that tends to minimize the length of the gap and hence to pull the armature closed. This is caused by the fact that it is energetically favorable to minimize the reluctance in a magnetic circuit. The deflection of the armature brings the mating contacts together that can be used to close an electrical circuit.

De-energizing the coil removes the source of magnetic flux and the electromagnetic force on the armature disappears. The mechanical spring pulls the contacts apart and re-establishes the reluctance gap in the magnetic circuit. It should be noted that the energy provided by the spring is stored during the closure of the relay. This means that the realized contact force is the maximum force delivered by the magnetic circuit less the contact break force.

## 14.3.2   Macroscale Variable-Reluctance Theory

The value of interest in a variable reluctance actuator is the magnitude of the force generated on the armature during closure. The analysis begins by modeling the relay as an inductor.   To aid writing subsequent equations in terms of reluctance, the following relationships are useful [127]:

$$V = L\frac{dI}{dt} = N\frac{d\Phi}{dt} \qquad \Phi = \frac{NI}{\mathfrak{R}} \qquad => \qquad L = \frac{N^2}{\mathfrak{R}} \qquad \text{eqn. 14.1}$$

L = inductance     V = voltage     I = coil current

$\mathfrak{R}$ = magnetic reluctance          N = number of coil windings

Now recall that the energy in an inductor is given by [127]:

$$E_{mag} = \frac{1}{2}LI^2 = \frac{1}{2}\frac{N^2}{\mathfrak{R}}I^2 \qquad\qquad \text{eqn. 14.2}$$

Since the variable of interest is force and force is just the derivative of energy, equation 14.2 gives:

$$F_{mag} = \frac{dE_{mag}}{d\ell} = \left(\frac{1}{2}\frac{(NI)^2}{\mathfrak{R}}\right)\frac{d}{d\ell} = -\frac{1}{2}\left(\frac{NI}{\mathfrak{R}}\right)^2\frac{d\mathfrak{R}}{d\ell} \qquad \text{eqn. 14.3}$$

The reluctance of the magnetic circuit of the relay is modeled as three reluctances in series. The three values represent the u-shaped core, the armature and the flux concentrating gap. For this analysis, the negligible reluctance of the gap near the restoring spring is ignored

and only the gap near the contact points is considered (refer to figure 14.1). Reluctance is defined as [137]:

$$\Re_{total} = \oint_{cir} \frac{d\ell_{cir}}{\mu_{cir}A_{cir}} = \frac{\ell_{core}}{\mu_{core}A_{core}} + \frac{\ell_{arm}}{\mu_{arm}A_{arm}} + \frac{\ell_{gap}}{\mu_{gap}A_{gap}} \qquad \text{eqn. 14.4}$$

$$\Re_{total} = \Re_{core} + \Re_{arm} + \Re_{gap} \qquad \text{eqn. 14.5}$$

$\ell$ = length of loop segment $\qquad\qquad$ $\mu$ = magnetic permeability

A = cross sectional area of loop segment

In the case of macroscopic relays, the total length of the magnetic circuit is less 100 times longer than the length of the flux concentrating air gap. At the same time, the permeability of the air gap is hundreds to thousands time less than that of the magnetic material of the core and the armature. Finally, the cross sectional area of the magnetic circuit is maximized in all circuit legs except at the air gap where it is typically much smaller. In terms of equations:

$$\ell_{core} + \ell_{arm} < 100\ell_{gap} \qquad\qquad A_{core} = A_{arm} > 10A_{gap} \qquad \text{eqn. 14.6}$$

$$\mu_{core} = \mu_{gap} \geq \mu_{gap} = \mu_{air} \approx \mu_0$$

$\mu_0$ = permeability of free space = $4\pi \times 10^{-7}$ H/m

Using these relative values:

$$\Re_{core} + \Re_{arm} << \Re_{gap} \qquad => \qquad \Re_{total} \approx \Re_{gap} \qquad \text{eqn. 14.7}$$

$$\frac{d\Re}{d\ell} = \frac{1}{\mu_0 A_{gap}}$$

<div align="right">eqn. 14.8</div>

Introducing equations 14.7 and 14.8 allows equation 14.3 to be reduced to:

$$F = -\frac{1}{2}(NI_o)^2 \frac{\mu_o A_{gap}}{\ell^2_{gap}}$$

<div align="right">eqn. 14.9</div>

where the negative sign indicates that the force tends to reduce the length of the air gap.

## 14.3.3    Analysis of Force Equation

Parsing equation 14.4 reveals a unique feature of the force equation is the form of the $A_{gap}(NI_0)^2$ term. This indicates that not only does the applied external current result in an increase in force, but so does the complexity of the physical structure of the relay. By comparison, consider the equation for electrostatic actuation derived in section 8.4.1 (see equation 8.3). The corresponding term there is $A_{plate}V^2$. In both cases, the size of the device affects the magnitude of the force. However, only in the variable-reluctance actuator does the complexity of the device, more specifically the number of turns fashioned into the coil, play a role in the equation. Being a squared term, the complexity can play a dominant role if the proper design is implemented.

An additional note of interest elucidated by equation 14.9 is that as the armature is pulled in, the force increases as an inverse function of the decrease in gap length. It is reasonable to assume that the gap will shorten by at least a factor of ten upon closure

resulting in a 100-fold increase in force for a given coil current.  As a practical relay issue, an actuating coil current that initially produces just enough force to begin to close the armature when it is fully open is magnified by the closure.  When fully closed, significant contact force is present to minimize contact resistance.

This inverse-squared gap term introduces the likelihood of the phenomena of snap-down.  In many actuators, an increase in force and deflection can only be attained by an increase in the applied power.  Often, to move an additional $\Delta x$, a greater increase in power must be applied than was necessary to move the first $\Delta x$.  This is not the case with this variable-reluctance actuator.  If the armature is held fixed, a given force, $F_1$, is generated by a given applied current, $I_1$.  Upon releasing the armature, the beam is drawn toward the core and the gap length decreases.  Once the armature position stabilizes, the magnetic force present on the beam has increased to $F_2 > F_1$ although the coil current has remained constant at $I_1$.  If the coil current is slowly increased, eventually it will reach a value, $I_{critical}$, producing a closure force, $F_{critical}$.  Any further increase in current (or possibly a mechanical perturbation that decreases the gap slightly) creates a runaway positive feedback loop of force versus deflection that abruptly "snaps down" the armature.  After snap down, $F_{closed}$ >> $F_{critical}$ allowing the coil current to be reduced while still maintaining full closure of the armature.  Alternatively, the coil current can be maintained at $I_{critical}$ and the additional force left in place to minimize contact resistance.

Finally, in designing a macroscopic relay, the simplifying assumptions that were made to produce equation 14.9 need to be heeded.  At first glance, the force can be made

arbitrarily large by simply increasing the area of the air gap.  Above a certain size, however, the assumption that the reluctance of the air gap is much larger than the reluctance of the remainder of the magnetic circuit no longer holds.  At this point, more of the energy introduced through the coil will be stored in the magnetic material of the core than will be present at the gap.  Eventually, the closure force will become negligible and the actuator will no longer function.  The key that makes the above analysis manageable is the fact that the only the reluctance of the gap need be considered.  Removing the simplifying assumptions greatly increases the complexity of the analysis and sets several challenging requirements for the fabrication of the device.

### 14.3.4   Micromachined Variable-Reluctance Actuator Issues

Micromachining a variable-reluctance actuator would be straightforward if the simplifications made in the macroscale analysis held in the world of MEMS devices. Unfortunately, present micromachine fabrication technology does not allow the same assumptions to be made.  First, MEMS structures are typically fabricated from thin film materials.  This translates an air gap length that is much shorter than the magnetic circuit length. Micromachined components typically have a much greater surface-to-volume ratio than those in macroscale relays.  This results in increased parasitic reluctance paths. Finally, the practical cross sectional area of the magnetic circuit is approximately the same as that achievable for the air gap.  Reviewing the assumptions in equation 14.6, it is obvious that the simplifications made for the macroscale devices do not hold in MEMS

relays.   With the appropriate choice of materials, careful layout of magnetic circuit geometry, and proper design of the fabrication process, the best that can be expected is for the reluctance of the gap to be slightly larger than the reluctance of the magnetic circuit.

To confirm these speculations, the introduction of some firm numbers is in order. Stresses in deposited coatings limit the maximum thickness of good quality magnetic material films to about 10 microns. A reasonable length of the magnetic core and armature assembly is several millimeters. The width of these structures cannot be arbitrarily large if the device is to maintain a small footprint. Assuming a device area of several square millimeters, the maximum practical width is approximately 500 microns.   The easily attainable minimum feature size of films with the above projected thickness is 10 to 20 microns. The thinness of the magnetic material and the desire not to saturate the metal prematurely limits the minimum practical width of the traces leading to the gap. These set the minimum size of the rectangular area of the air gap to be about 20 microns by 200 microns. Finally, to avoid arcing between open contacts when hundreds of volts are placed across them dictate that the gap length be on the order of 5 to 10 microns (see section 10.7).  In terms of equations:

$$\ell_{core} + \ell_{arm} > 250\ell_{gap} \qquad A_{core} = A_{arm} \approx A_{gap} \qquad \text{eqn. 14.10}$$

Substituting these values into equation 14.4 gives:

$$\frac{\left(\ell_{core} + \ell_{arm}\right)}{\mu_{mag}} \approx \frac{250\ell_{gap}}{\mu_{gap}} \qquad \text{eqn. 14.11}$$

This sets the requirement for the permeability of the magnetic material used to construct the magnetic circuit. To bring the reluctance of the circuit just down to the level of the air gap, a permeability of 250 times that of free space must be achieved. The parasitic reluctance paths in the circuit require that a more realistic minimum permeability value of 1000 should be targeted.

It is possible to calculate the optimum ratio of circuit reluctance to gap reluctance required to maximize the actuation force when the circuit reluctance cannot be neglected. The most straightforward approach to this analysis is achieved by realizing that maximizing the magnetic force is analogous to the problem of maximizing the electrical power delivered to a load when the source resistance is non-zero. The ability to make such an analogy is part of the power of viewing the magnetic circuit in terms of reluctances. In the electrical case, the equivalent circuit is a simple resistive voltage divider. The power delivered to the load resistor in the circuit is simply:

$$P = I^2 R_{load} = \left( \frac{V}{R_{source} + R_{load}} \right)^2 R_{load} \qquad \text{eqn. 14.12}$$

Assuming that $R_{source}$ is fixed, differentiating equation 14.12 with respect to $R_{load}$ gives:

$$\frac{dP}{dR_{load}} = V^2 \left( \frac{1}{\left( R_{source} + R_{load} \right)^2} - \frac{2 R_{load}}{\left( R_{source} + R_{load} \right)^3} \right) \qquad \text{eqn. 14.13}$$

For this derivative to be zero, and thus for the power delivered to be maximum, requires

that:

$$R_{load} = R_{source} \qquad\qquad \text{eqn. 14.14}$$

Translating this result back into the variables for the magnetic circuit, when the reluctance

of the magnetic circuit is non-zero, the force exerted on the relay armature is maximized

when:

$$\left(\Re_{core} + \Re_{arm}\right) = \Re_{gap} \qquad\qquad \text{eqn. 14.15}$$

As shown in equation equation 14.11, reasonable micromachining techniques are expected

to produce a magnetic circuit with relative reluctance values that fulfill this precise equality.

All in all, this is a rather fortuitous coincidence.

## 14.3.5    Maximum MEMS Variable-Reluctance Force

The thickness limitation imposed by electroplated permalloy films may bound the

force that can be achieved by the MEMS variable-reluctance actuator.   As noted at the

beginning of this chapter, it is preferable to have the current-carrying capabilities of the coil

limit the ultimate closure force that can be generated in a relay.   In macroscale devices, this

is achieved by using a magnetic circuit with a large cross-sectional area.   This ensures that

the core never fully saturates.  In the analysis conducted in the previous section, it is noted

that achieving good quality permalloy films with acceptably low total internal stress

typically limits their thickness to about 10 microns.   Such a value does not allow a core

with a large cross section to be fabricated.  As such it is likely that the magnetic circuit will

saturate before the coil fails. When this happens, the flux magnifying and channeling characteristics of the magnetic material are lost and increasing coil current fails to add to the closure force. It is useful to know at what point the circuit will saturate and to what force level this corresponds.

Deriving the maximum force that can be produced when it is limited by saturation of the magnetic core begins with an equation for stored energy. When the magnetic flux density is increased from zero to B in a magnetic circuit, the energy stored in the gap can be expressed as [127]:

$$E_{max} = \frac{Volume}{2\mu_0} B^2 \qquad\qquad \text{eqn. 14.16}$$

Where the volume is the length, L, of the gap times its cross sectional area, A. Differentiating this equation with respect to length and setting the magnetic flux density to its saturated value gives the following expression:

$$F_{max} = \frac{A}{2\mu_0} B_{sat}^2 \qquad\qquad \text{eqn. 14.17}$$

From this equation the maximum force that the MEMS variable-reluctance relays can theoretically produce is determined. In the devices fabricated during the course of this research, the air gap is designed to have an area of 50 by 150 microns and be 5 to 10 microns long. The plated permalloy saturates at 0.8 to 1.0 Tesla and $\mu_0 = 4\pi \times 10^{-7}$. Entering these values into equation 14.17 shows that the maximum closure force that can

be expected in these relays is 2 to 3 mN. Choosing the highest force value and letting the gap length be 5 microns, the corresponding amp-turn value can be calculated using equation 14.9. Doing so shows that energizing the coil with an NI value greater than 16 just burns power and does not increase the closure force. Coils in these MEMS relays have 20, 40 or 60 turns with resistances of 12, 24 and 36 ohms respectively. This gives maximum useful current levels of 800 mA, 400 mA and 265 mA respectively with corresponding coil powers of 7.6 W, 3.8 W, and 2.5 W. Such power levels are very high. It is preferred for the relays to operate at coil powers below 0.5 W and preferably down in the tens of milliwatts range. In any case, it does not seem that core saturation will be a limiting factor in device operation and though requiring high coil powers, the prototype relays are capable of producing millinewton range forces.

## 14.4 Cantilever Beams

The final functional piece to be analyzed in these actuators is the component that provides the contact break force. In the macroscale device, this is a simple helical spring that is stretched when the relay closes then contracts when the coil current is removed. In micromachined devices, producing such a spring is nearly impossible. In place of such a complex structure, a cantilever beam is typically used instead. The cantilever replaces both the spring and the armature used in the macroscale device. Where once a pivot point held the base of the armature, a rigid attachment between one end of the cantilever and the substrate or core is used. The remaining length of the beam is freestanding and creates an

air gap between it and the substrate of several to tens of microns.  A schematic of the device is shown in figure 14-2.

In designing the cantilever beam, care must be taken to maximize its cross sectional area while not exceeding a specified stiffness.  This is particularly true for the variable-reluctance actuator.  Maximum cross sectional area is required to minimize the possibility of core saturation during the application of high coil currents.  The beam will be the "choke point" in the magnetic circuit.  If too small, the maximum force that the actuator will be able to generate will be set by the maximum magnetic flux that can flow through the beam without saturation occurring (see section 14.3.5).  Since monitoring the saturation state of any part of the magnetic circuit is nearly impossible, it is preferable to have the maximum force limited by the maximum carrying current of the coil.  If designed properly, the closure force will be accurately described by equation 14.9 and monitoring of the applied current will be all that is necessary.  Unfortunately, limiting the stiffness of the beam limits the cross sectional area that can be realized.
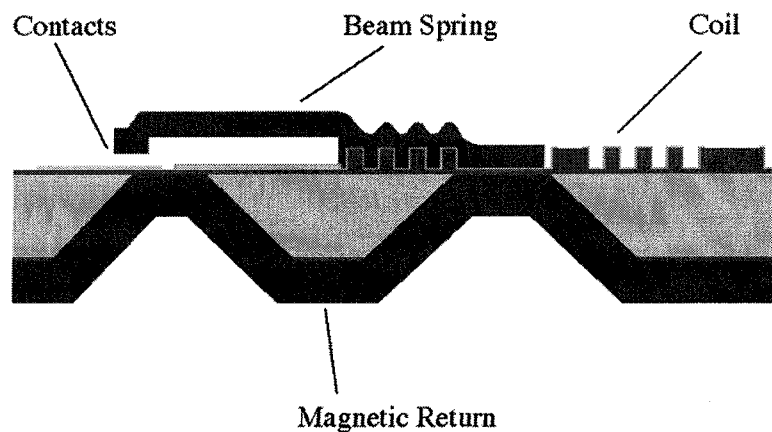


Figure 14-2:  Drawing showing the cross section of the MEMS microrelay.

It should be noted that different design other than those shown in figure 14.2 and figure 12.5 can be employed which separates the mechanical spring component from the magnetic flux path. For prototype relays, however, a key design consideration is that the relay geometry allows easy characterization of both the mechanical and the magnetic properties of the device. The simple structure and straightforward equations governing beams in bending make cantilevers an ideal, testable component for micromachined devices.

## 14.5    Linear Beam-in-Bending Theory

To identify those beam dimensions that can be readily varied to meet both the magnetic and mechanical requirements of a relay, the equations governing beams in bending must be examined. Derivation of the following is covered well in [94, 97, 159]. It is specified for convenience that the beam is horizontal and the loading is vertical. In short, it is assumed that the length of the beam is subjected to "pure bending," i.e., moments are applied at the ends of the beam that tend to "bend" it. The resulting curve of the beam is that of a circular arc with a certain radius of curvature. From this basic picture, equations for stress and strain can be derived. Equilibrium requirements, beam material, and beam cross section then lead to expressions for deflection as a function of force. While it is possible to calculate values for all manner of bending, restricting the beam to small deflections, or linear bending, greatly simplifies the modeling. In the typical micromachining application, the magnitude of the deflections experienced by structures

meet this condition.

For the cantilever that forms the armature of the micromachined relay the following equations are useful [159]:

$$F = \frac{3EI}{L^3} z \qquad\qquad \text{eqn. 14.18}$$

$$I = \frac{wt^3}{12} \qquad\qquad \text{eqn. 14.19}$$

z = beam deflection     E = modulus of elasticity     L = beam length

I = moment of inertia     t= beam thickness     w = beam width

Where the bending force, F, is applied perpendicularly to one end of the beam while the other end is held clamped.

From equations 14.18 and 14.19 it can be seen that the two variables that have the greatest effect on beam stiffness, due to their being cubed factors, are length and thickness. In practice, the thickness range of permalloy that can be readily deposited is limited to approximately ten microns. This in turn limits the realistic range of lengths for the beam. Footprint and practical minimum dimensions further constrain the lengths that may be used. Maximum deflection is set by the desired standoff voltage desired for the target device and the modulus of elasticity is set by the beam material, in this case permalloy. That leaves only the width of the beam as the geometric variable that may be readily adjusted to provide fine-tuning of beam stiffness. While this may seem limiting, it does allow for a relatively

large range of devices to be fabricated. For prototype devices where an order of magnitude range in stiffness is desired, combining changes in length and width allows all design targets for deflection force to be achieved.

## 14.6 Low Temperature Insulation

Multiple conductive layers must be electrically insulated from one another in the armature microrelay. The type of insulator and the process used to deposit them must be compatible with the metal layers they are insulating. With metal present on the substrates, high temperature processing must be avoided. At extreme temperatures, melt and reflow are the obvious concern. At temperatures below the melting point of the metals problems still arise. Most notably, film stress can increase dramatically to a level at which they can delaminate from the substrate. Discussed in section 9.2.4 temperatures above 300 °C were found to be incompatible with permalloy. Copper will also delaminate due to an increase in thermally induced internal stress at temperatures above 400 °C. A separate but important consideration pushing for low processing temperatures is the desire to use silicon substrates that contain pre-fabricated CMOS circuitry. Due to the materials used in their construction and dopant diffusion considerations, the total thermal budget of such wafers must be kept low.

To accommodate the low thermal constraints posed, several materials have been considered. Traditional micromachining techniques rely on PECVD and LPCVD deposited films of oxide and nitride. Sputtered insulators and spin-on-glass (SOG) are also

becoming more popular. For this work, a sputtering system was not available so it will not be considered here. Spin-on-glass was briefly investigated. Its step coverage of thick (> 5 micron) structures was found to be poor and SOG films thicker than 1 micron become greatly stressed and typically crack during cure. Photoresist, properly treated, can be an adequate insulator for a number of applications. Vacuum deposited parylene and teflon are presently being explored and show promise as good insulators that can coat surfaces at room temperature.

## 14.7 Organic Insulators

A range of polymer insulating materials is available for use in micromachining. Photoresist is perhaps the most common material used in both the integrated circuit and the micromachining fields. A very attractive feature is the simplicity of its patterning and its sub-200 °C processing range. Typically, however, it is used to pattern other materials. Only in the disk drive industry has it been extensively employed as a permanent insulating material. Having similar properties to photoresist, polyimide is also a common insulating material. Processing can be kept below 300 °C and so should be compatible with all the MEMS relay metals. Adhesion of this polymer and patterning are not as good or straightforward as photoresist. As such, special wafer preparation and several additional steps are needed to achieve adequate results. Finally, vacuum deposition systems for parylene have recently been introduced into the industry. Deposited at room temperature, these insulators show great promise for a number application though several years of

continued development may be required before they are able to be used widely in MEMS microrelay fabrication.

### 14.7.1 Photoresist as an Insulator

Photoresist is a photosensitive polymer material that is used extensively in commercial industry. It is typically employed as a masking layer in order to protect select regions during plasma and wet chemical etching. The disk drive industry, and increasingly the micromachining community, has used it to create plating molds for selective metal electrodeposition as well as to form permanent insulating and structural films. Photoresist is an attractive insulating material because its processing and patterning are simple. Spun on as a thick liquid, it readily covers highly non-planar features and can partially level such a surface as it coats. With a glass reflow temperature typically on the order of 120 °C, further planarization can be achieved. Reflowing essentially softens the photoresist allowing surface tension to pull the material from elevated regions into lower, neighboring areas. When baked at temperatures much higher than 120 °C, photoresist can be fully polymerized at the same time that volatiles are removed. The resulting film is an excellent dielectric and is mechanically sound enough to become part of a permanent structure.

The low temperature processing of photoresist that makes it attractive also makes it of questionable suitability for insulating in a MEMS microrelay. The disk drive industry regularly uses photoresist to insulate between multiple layers of copper coils in their read/write heads. In this application, relatively thin conductors on the order of 1 to 2

microns thick are used to pass low-level currents. Coil heating does not seem to be an issue. For the armature microrelay, however, relatively high coil powers are seen by the photoresist. Fabricated coils have measured resistances on the order of 10 ohms. Passing just 0.5 amps results in 2.5 W of dissipated power in an area of less than 1 square-millimeter. Temperatures can rise quickly in the coil region and in all likelihood exceed 200 °C. In tests, significant thermal expansion of photoresist films is seen at high coil currents. The corresponding deflections experienced by cantilever test structures were on the order of 5 to 10 microns, the same as the contact gaps designed in the microrelay. These results led to the search for other insulating materials that have greater thermal stability.

### 14.7.2  Polyimide

Polyimide is similar in many ways to photoresist but typically has superior mechanical and thermal properties. Spin coating is the preferred method of applying polyimide to a substrate and, like photoresist, results in good coverage and some planarization of highly featured surfaces. Published papers report it has good insulating [139] and reasonable mechanical properties [82, 85]. While available with a photosensitizer, investigations conducted in the course of this work found such solutions unsatisfactory. Adhesion is very poor and the features defined by UV exposure are typically quite distorted. Only pure polyimide is found to have adequate, though still non-ideal, adhesion to silicon substrates. This material requires substantially more processing to be pattern as compared to photoresist. A mask material must be deposited and defined to

permit a subsequent oxygen plasma etch to pattern the polyimide. Isotropic undercut then limits the minimum feature size and aspect ratio that can be achieved in the polymer film.

A number of MEMS devices have been produced using polyimide as a permanent, insulating material. Most notably is the relay and inductor work produced by [81, 147]. The realization of functional devices shows that this polymer is a viable choice of insulating material. Thermal performance was not reported and no mention of problems arising from the polyimide was made. This may be due to the unique structure of the high coil-power devices whose operation may not be susceptible to thermally induced flexing of the insulator. Additionally, the reported coil powers under normal operating conditions were all less than 0.5 W with coil footprints of more than 10 square millimeters. Such a large area may adequately sink any heat produced by the coil current. In the course of this thesis work, preliminary investigations suggested polyimide is better than photoresist in thermal performance but that thermal deflections are still seen at high coil powers. Whether this slightly superior performance is due to an intrinsic material property or to the fact that polyimide is designed to be processed at higher temperature is uncertain. The latter is suspected.

Polyimide was determined to have too many drawbacks for use in the MEMS relay. The additional processing complexity, the non-ideal thermal characteristics, and the possibility of hydrocarbon contamination ended the consideration of this polymer as an insulating material.

### 14.7.3  Parylene

A new class of materials making in roads into the integrated circuit industry is generically known as parylene. This unique family of thermoplastic polymers is formed on surfaces exposed to a rarified gas in a vacuum. The resulting linear, crystalline polymer coating possesses superior barrier properties per unit thickness, has extreme chemical inertness, and is free from pinholes. Colorless and transparent, parylene is the only commercially available polymer coating that is applied in a non-liquid manner [75]. Available with high dielectric strength and low dielectric constants, excellent thickness uniformity on all exposed surfaces of a substrate, including deep crevices, sharp points and planar areas can be readily achieved. The deposition process occurs at room temperature avoiding the problem of cure induced stresses generally experienced with the use of liquid coatings. The deposited films can be many tens of microns thick and are extremely pure and as such are nearly chemically inert. Parylenes can be readily patterning using a standard oxygen plasma etch.

These amazing traits seem to good to be true and, in fact, there is a limitation to these materials. The readily available parylenes begin to degrade in operating environments greater than 130 °C. This is due in part to thermal evaporation as well as reaction with oxygen species. As noted above, photoresist is found to be incompatible with relay coils due to the high temperatures generated. The available parylenes do not fair much better and their performance is unacceptable.

A new parylene presently being developed may overcome this limitation and retain

and even improve, the other desirable characteristics noted above. Designated AF-4 and Nova HT by its manufacturer [75], this is a fluorinated parylene. Data sheet specifications claim > 450 °C operating range, a low dielectric constant of 2.23, and a dielectric strength of 750 V/micron. At present, however, only engineering runs performed by the manufacturer are available and they are quite costly. When this technology moves from infancy into more wide spread use, this material should be revisited. For this work experimentation with the fluorinated parylene was not possible.

### 14.7.4 Hydrocarbon Contamination

Separate from the limitations noted in the above section, an additional issue associated with the use of an organic insulator in a microrelay is the potential for hydrocarbon contamination of the contacts. Specifically reported for gold, silver, platinum and palladium contacts [98, 145], the presence of an adhesive backed polyimide foil was found to increase the contact resistance. Generally accepted in the relay industry is the need to eliminate all volatile organics and sources of contaminant outgassing from the chamber containing the contacts. When switching in a hydrocarbon-containing atmosphere, the conditions experienced at the contacts tend to getter the contaminants and form carbon deposits on the mating surfaces. The deposits lower the electrical field and the minimum current at which an arc will ignite [78]. The duration the arcs last in the presence of the contaminants rises causing a rapid increase in the erosion rate of the contact material. The life of contaminated contacts can be reduced to as little as 10 to 30% that of clean contacts.

As polyimide is implicated as a possible contaminant by [98], it is not unreasonable to believe that photoresist and parylene are similarly suspect. If coil operating temperatures are kept low, the polymers are probably sufficiently stable and should produce minimal outgassing. If their thermal limits are exceeded, however, they undoubtedly will become a significant source of contamination. Introducing organics into a region where they will experience repeated heating and cooling is likely to cause unwanted carbon vapors to be generated. In a microrelay where many things must come together perfectly for proper operation to be achieved, inclusion of such materials is seen as tempting fate once too often and has been avoided in this work.

## 14.8  Chemical Vapor Deposited Insulators

Chemical vapor deposition (CVD) of insulator material is widely used in integrated circuit processing. Typically done at low pressures, CVD systems inject vapor phase chemical reactants into a chamber where they form non-volatile solid films on any exposed surface [156]. At low temperatures, the rate of reaction and surface mobility of the reactants and the deposited compounds are very low. A low reaction rate results in very slow film growth. Poor surface mobility causes poor uniform surface coverage or non-conformal coating as well as poor quality, pinhole-filled films. To improve the speed and quality of the deposition, high temperatures and/or plasmas are typically used. Temperature only systems are commonly referred to as low-pressure CVD (LPCVD) and the chambers typically operate in the 350 to 1000 °C range. Reactors that use plasma-

enhanced deposition are referred to as PECVD systems and often still require substrates to be heated to 200 to 300 °C.

## 14.8.1 PECVD Insulation

The low temperature range in which PECVD systems operate make insulators deposited by them an attractive choice. Such reactors can deposit both oxide and nitride, which are very good insulators. However, conformality in such reactors is non-ideal. Relatively thick layers must be deposited in order to ensure complete coverage of steep sidewalls. In the case of the coils integrated into the MEMS relay, insufficient coverage in the corners at the bottom of the 10 micron deep, 5 to 10 micron wide spaces between traces is found to be poor. Shorting between the coil and the overlayer of permalloy is commonly seen in devices employing PECVD insulation. A more reliable technique is necessary to achieve an acceptable yield.

## 14.8.2 LPCVD Insulation

The higher temperatures seen in LPCVD furnaces seem to preclude their use with copper and permalloy. Only at the low end of the temperature range is there an overlap in compatibility and even then permalloy must not be present on the substrate. LPCVD nitride is typically deposited at approximately 850 °C. Attaining good quality films at sub-400 °C is not to be expected. LPCVD oxide, often referred to as low temperature oxide (LTO), however, is used in the IC industry to insulate aluminum traces. It was developed to work

at approximately 450 °C.  Using the same gas recipe listing in the standard procedure,

reasonably good quality LTO films have been grown at temperatures down to 380 °C.  In

this environment, minimal pinhole density is seen although surface mobility is slightly

degraded.  Shown in figure 14-3 is a cross-section of several turns of a copper coil

insulated with LTO.  Note that the thickness on top of the coil traces is much thicker than

down the sides.  In fact, a distinct taper in LTO thickness down the side can be discerned

with the coverage at the corner formed at the base being quite thin.  In practice, to attain 0.5

microns of insulating coverage at the base, 2 to 3 microns of total LTO thickness must be

deposited onto the surface of the wafer.



Figure 14-3:  Scanning electron micrograph of a cross section of several of the
thick copper plated, planar coil traces that are covered with low temperature oxide
and plated permalloy.

As noted in the above sections, none of the available technologies meet all of the requirements for insulating the coil of the armature microrelay.  In the final work, LTO was chosen as the best compromise.  Through two-sided substrate micromachining and proper sequencing of the fabrication steps, the number of insulating layers required in the microrelay is kept to just one.  This only covers the copper coil and no permalloy structures are present on the substrate during LTO deposition.  Using the 380 °C furnace temperature results in material compatibility and fully functional devices.

# CHAPTER

# 15

# DESIGN AND FABRICATION
# OF ARMATURE MICRORELAYS

Figure 15-1 shows the top view of a representative microactuator that has been

fabricated. It consists of a planar electromagnetic coil that is wrapped around a high

permeability, quasi-3D magnetic circuit. This magnetic circuit consists of three main

components: a freestanding permalloy cantilever beam, an air gap and a permalloy

magnetic flux return path. Simultaneously optimizing the interdependent variables of these
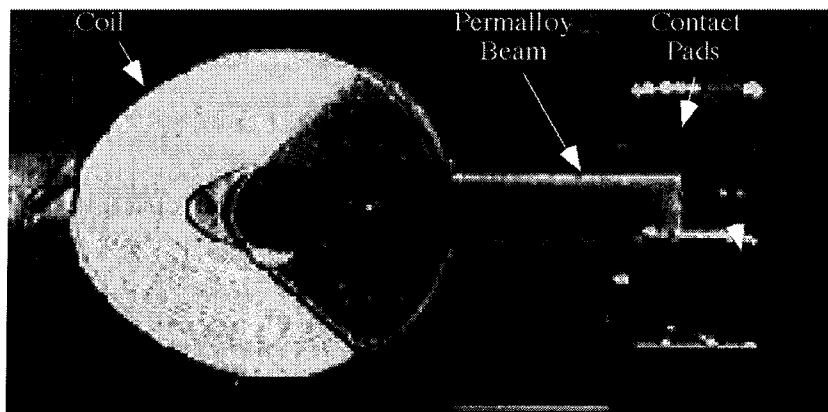


Figure 15-1: Photograph of an armature microrelay that has been fabricated and tested in the course of this research.

elements, while difficult, is required to produce an efficient magnetic actuator.  As noted in section 14.3, if the reluctance of the magnetic core ($\Re_{core}$) can not be neglected then magnetic power transmitted to the gap is maximized when $\Re_{gap} \approx \Re_{core}$.  For a realistic core length of several millimeters, it is estimated that a $\mu \geq 1000\mu_0$ is needed to produce an actuator that maximizes the force developed at the air gap.

## 15.1   Design of Armature Microrelays

Optimizing $\Re_{core}$ is complicated by the bending force requirements demanded of the cantilever beam which is an integral part of the magnetic circuit.  While a moderately stiff beam is needed in order to produce an actuator with a large break force and a high switching speed, it must be compliant enough to be deflected by the forces that can be generated at the air gap.  This limits the thickness of the permalloy that may be used to construct the beam.  As a result, $\Re_{beam}$ becomes a large component of $\Re_{core}$.  This requires that the remaining components of the magnetic core have minimal reluctance in order to maintain $\Re_{gap} \approx \Re_{core}$.  This is achieved by providing a magnetic flux-return path with a very large cross-sectional area across the backside of the device.  Neither width nor thickness of the plated permalloy used to form the return-path is limited with this approach and the result is that $\Re_{return} \ll \Re_{beam} \approx \Re_{core}$.  Practical beam dimensions of 10-$\mu$m-thick and 200-$\mu$m-wide were chosen to fabricate beams 500 microns and 1000 microns long with 5 to 10-micron air gaps.  These values produce cantilevers that provide up to several hundred micronewtons of break force and calculated resonant frequencies of up to 75 kHz.

To maximize amp-turns, it is desirable to maximize the number of coil turns. This reduces the required coil current and thus coil power ($P_{coil} = I^2 R_{coil}$). Two options are available to increase the number of turns. The first is to fabricate a multilayer coil. This approach minimizes the footprint of the final device but greatly increases fabrication complexity. An equally valid solution is fabricating one or several multi-turn pancake coils. While this does increase device real estate, the resulting fabrication process is extremely robust and microrelay yield very high. Figure 15-2 shows a switch fabricated with three pancake coils. Testing verifies that connecting the coils together in series produces the expected increase in the generated actuation force.
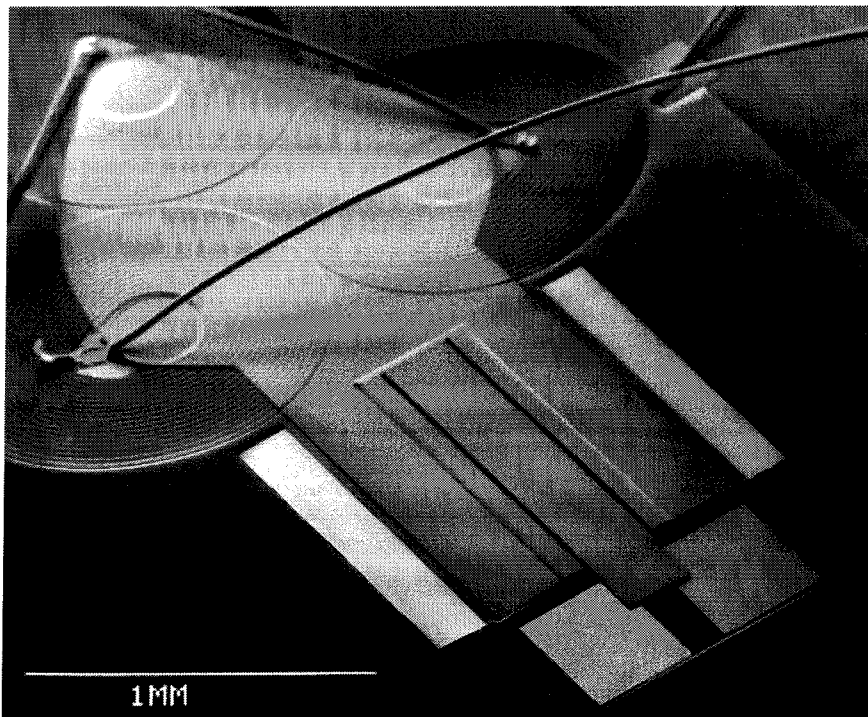


Figure 15-2: Scanning electron micrograph of a MEMS variable-reluctance electromagnetic actuator incorporating three planar coils in order to increase the ampere-turns of the device.

## 15.2 Armature Microrelay Fabrication

The major fabrication steps used to produce the armature microrelays prsented are shown schematically in figure 15-3. The process utilizes both bulk and surface micromachining techniques as well as metal plating processes. All processing is done at low temperatures (< 400 °C) and is expected to be compatible with substrates containing CMOS circuitry.

Processing begins with a nitride coated, 500-μm-thick, <100> silicon substrate. On the backside of the wafer, silicon access holes are patterned in the nitride and anisotropic etchant (potassium hydroxide) is used to form vias to the front side of the wafer. On the front, metal electrodes are evaporated and patterned. An electromagnetic coil is plated and coated with an insulation material to electrically isolate it from the rest of the device. A sacrificial layer is formed from photoresist on top of which discrete contact points of pure gold are plated. A permalloy cantilever is then plated on top of the sacrificial layer such that the gold contact points form the end of the beam. With processing on the front side complete, a final global permalloy plating is performed on the backside of the wafer. After dicing, the cantilever beam is freed by removing the sacrificial layer with hot photoresist stripper.

This process can be easily modified to meet different design criterion. The thickness of the plated metal layers can be varied from 0.1 microns to tens of microns to create a range of coil resistances and cantilever beam stiffnesses. Photoresist is very easily deposited and permits a wide range of air gaps, from 0.1 microns to tens of microns, to be

# MicroSwitch Double-Sided Fabrication Process



1) Form Backside Cavities and Front Side Nitride Membranes

2) Evaporate Gold Contact Points and Eloectroplate Thick Copper Coils

3) Insulate First Metal Layers then Lay Down PR Sacrificial Spacer and Plate Thick Permalloy Cantilever Beam

4) Global Plate Very Thick Permalloy on Backside of Wafer

5) Strip PR Sacrificial Spacer to Free Cantilever Beam

Top View

■ - Electroplated Copper          ▨ - Bulk Silicon

▨ - Evaporated Gold               ▨ - Sacrificial Photoresist

■ - Electroplated Permalloy       ■ - Silicon Nitride

Figure 15-3:  Cross sections of the major steps of the armature microrelay fabrication process.

fabricated. While the contact material has always been deposited by plating in this research, sputtering is also compatible with this process. This will allow nearly any contact material to be integrated into these microrelays. All steps are done at low temperature to permit wafers with CMOS circuitry to be used as the starting substrate. This makes it possible for future designs to incorporate electronic circuits on-chip without modifying the process.

## 15.3 Processing Issues

The most challenging part of the above fabrication process is ensuring that the planar coil is sufficiently insulated. If not completely covered, the coil will be electrically shorted by the subsequent permalloy plating that forms the cantilever beam. It is actually the flux path running from the fixed end of the armature, across the top of the coil, and to the through-wafer via that is problematic. This structure is plated in direct contact with the insulation covering the coil. The electrodeposition process grows metal on all exposed surfaces ensuring that the tops and sides of the traces as well as the valleys between them are coated with permalloy. If the coil is exposed in any way, be it bad coverage, pinholes, or cracks, the plated metal will short the traces together. In practice, the thickness of the insulation at the base of the traces is very thin. It is found that at least 2.5 microns of LTO must be deposited on the top of the coil to grow a satisfactorily thickness of insulator in the crevasses.

Proper orientation of the substrate wafer in the permalloy plating bath is required to introduce the proper easy axis in the magnetic circuit of the microrelay. These devices rely

on the ability of the permalloy core to collect and magnify the magnetic field from the planar coils for the generation of their closure forces. The flux amplifying effect arises from the small field produced by the coil aligning the magnetic domains in the ferromagnetic material that then add their fields to the total flux in the circuit. In macroscale devices, these magnetic domains are oriented randomly with respect to one another and their average size is set by the polycrystalline structure in the bulk metal. For thin plated films, the case is slightly different.

In a MEMS magnetic film, the size of the individual domains can be, and typically are, the same order of magnitude as the dimensions of the patterned microstructures. The result is that the physical geometry of the magnetic circuit can define the general orientation of the magnetic domains. In the case of the microrelay, two preferential alignments arise. These are parallel/anti-parallel and perpendicular/anti-perpendicular to the length of the magnetic circuit. Because the width of the structure is much smaller than the length, more domains are present if they are oriented in a perpendicular/anti-perpendicular fashion. If parallel/anti-parallel, it is possible for a single large domain to form. In the case of the latter, the domain(s) is already oriented in the desired direction and a field generated by the coil has nothing to align. With no change in flux, no actuation can occur. In the case of the former, the perpendicular/anti-perpendicular will be rotated 90° and their walls will expand until one large domain is formed parallel to the length of the magnetic circuit. The large change is flux will give rise to closure forces at the contact gap and the desired switching action will occur.

During plating, a magnetic field parallel to the face of the cathode surface is used to induce a known crystalline anisotropy in the deposited permalloy films. The microrelay wafer must be placed in the tank such that the vector direction of the cantilever beam being plated is perpendicular to the applied magnetic field. This will produce domains oriented perpendicular/anti-perpendicular to the length of the magnetic circuit. During the course of this research, one microrelay wafer was improperly position during the permalloy plating and not a single one of the devices functioned when tested at the end of the processing run. An expensive (in terms of lost time) lesson but it did offer verification of the above argument.

# ARMATURE MICRORELAY CHARACTERIZATION, EXPERIMENTAL TESTING, AND CONTACT FAILURE ANALYSIS

Characterization of the actuation forces and the electrical properties of the fabricated armature microrelays has been performed. The resulting data provide a baseline for the maximum performance that can be achieved by the devices when operating in ideal conditions. All analysis was performed in the Caltech micromachining lab on standard testing equipment.

## 16.1 Mechanical Characterization

Recording all of the salient parameters that need to be measured in the armature microrelay while it is in nominal operation is not practical due to its small size. Of particular interest are the force levels generated by the variable reluctance actuator, the contact force seen by the mating surfaces, and the manner in which these surfaces strike

one another during closure.  To ensure that the forces generated in the microrelays are reasonably close to the numbers predicted by theory, a series of calibration experiments have been conducted to characterize the cantilever beam forming the armature of the magnetic circuit.

## 16.1.1  Force Deflection Calibration

Bending force calibration was performed on a static load-testing set-up assembled at Caltech (see figure 6-7).  The instrument consists of a load cell to measure applied forces, a linear voltage differential transformer (LVDT) to measure z-displacement and a sharp metal pin which contacts the sample inducing controlled deflection.  The permalloy cantilever beams are removed from several microrelays complete with the flux shield that overlays the



**Permalloy Cantilever Beams in Bending**

Beam Length = 500 μm
k ≈ 49.2 μN/μm

Beam Length = 1000 μm
k ≈ 5.8 μN/μm

Force (μN)
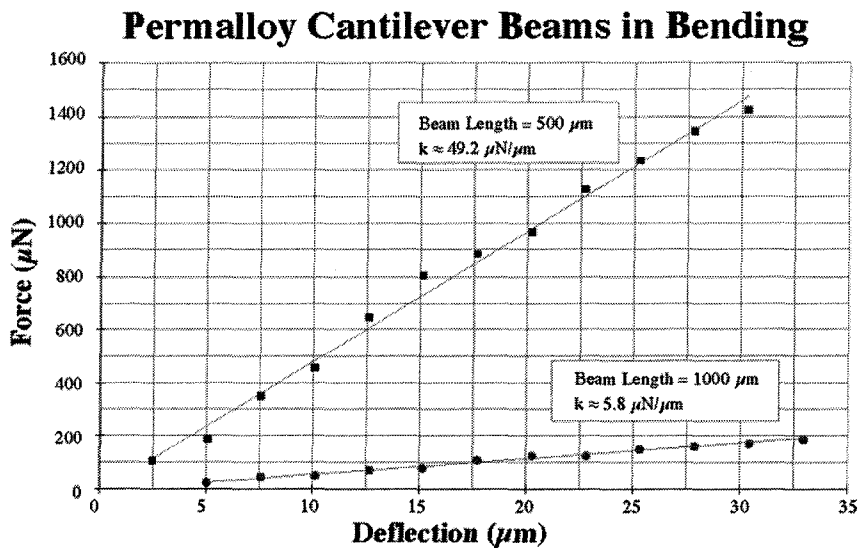
Deflection (μm)

Figure 16-1:  Experimental data showing beam deflection as a function of force applied to the tip of beams of two different lengths permitting spring constants to be calculated.

planar coils. These structures are clamped at the edge of a rigid substrate by the flux shield such that the beams extend out into free space. The assembly is then mounted with the beam orthogonal to the central axis of the load cell. A micrometer slowly raises this assembly into contact with the immovable pin such that the tip of the pin presses down at a known distance from the fixed end of the beam (500 microns or 1000 microns depending on which structure is being tested). Force as a function of load cell position, and thus beam deflection is then recorded.

Typical loading curves obtained with this procedure for the two cantilever beam lengths that have been fabricated are shown in figure 16-1. The measured bending stiffnesses are approximately 49 $\mu N/\mu m$ and 5.8 $\mu N/\mu m$ for the 500-micron and 1000-micron long beams, respectively. For a microrelay employing a 5-micron gap, these values translate to 245 $\mu N$ and 29 $\mu N$ contact break forces, respectively. This knowledge provides at least one immediate actuation force data point for functional microrelays. If mechanical deflection is seen and contact mating confirmed, the variable reluctance actuator in the device must be supplying, at a minimum, this much closure force. Due to the snap-down effect during make, the coil current at which the beam is released from the substrate is the more accurate measure of the power required to generate the force.

This bending data verify the linear beam-in-bending approximations made in the design phase of these devices. The spring constant calculated from the graphs are close to that predicted by theory and results in the desired appropriate one order of magnitude range of break forces in the microrelays.

## 16.1.2 Magnetic Actuation Calibration

Variable-reluctance actuation has been demonstrated in fabricated devices by beam

closure and electrical shorting of mated contacts. To verify that the closure forces are

magnetic in origin (and not, for example, thermal due to heating by the energized coil), data

of beam deflection as a function of coil current was collected for a number of devices. The

threshold current level required to attain contact mating was determined for the microrelays

prior to the testing. Then, a laser interferometer with better than 0.1-micron resolution

monitored the vertical position of the end of the armatures in the microrelays while a

triangle waveform current was applied to the coils. The data collected continuously as the

beam moves up and down. Those points measured during armature deflection are
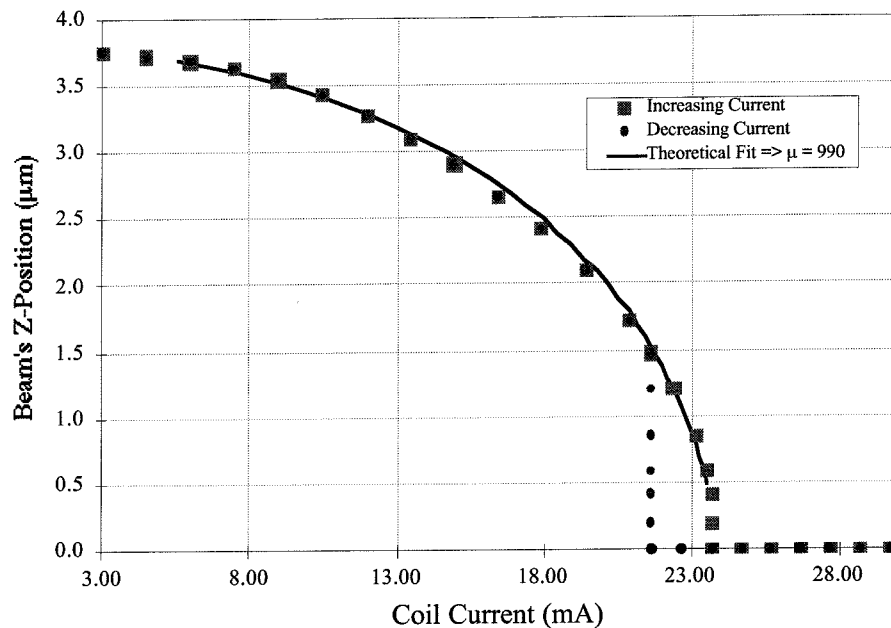
Figure 16-2: Experimental data showing beam deflection as a function of coil current. Note that the beam snap down and hysteretic release predicted by theory is present.

separated from those corresponding to beam release. The release data is manipulated to "flip" it about its vertical axis and allow it to be overlain on top of the deflection trace. The resulting composite elucidates a number of characteristics including the beam snap-down and the release-hysteresis predicted by theory.

The plot in figure 16-2 shows the deflection data for a 1000-micron long armature that was magnetically actuated in a microrelay employing a 5-micron gap. For the ease of reference, this device is designated A1000-5 (i.e., armature length 1000 microns with 5 micron gap). Note that the total realized deflection is only 3.8 microns, not the defined 5 microns just stated. This is because the beam is actually 650 microns long and the magnetic gap that generates the closure force is located 150 microns from its tip. During closure, the contact points at the tip strike their mating surfaces first. This keeps the contact gap from ever fully closing. As measured, the actual beam motion in the area of the magnetic gap is only 3.8 microns.

The data show that the tested device produces microns of deflections with just tens of milliamps of coil current. Contact make and break occur at an applied currents of 24.0 mA and 21.7, respectively. This particular microrelay uses three planar coils connected in series producing a total coil resistance of 36 $\Omega$. As noted above, the spring constant for the 1000-micron long beam is approximately 5.8 $\mu N/\mu m$. Putting these numbers together it is calculated that this variable reluctance actuator requires > 20.7 mW for contact make and produces a force of $\approx$ 22.0 $\mu N$ at an applied coil power of just 16.9 mW. Figure 16-2 clearly shows that displacement hysteresis between beam-deflection and beam-release

occurs in this device. A slight beam snap-down on closure is also seen. Both of these phenomena are predicted by the variable-reluctance actuator theory. Using the appropriate equations from section 14.3, the magnetic core in the microrelay can be characterized. It is found that a relative permeability of 1100 and an efficiency value of 83% best fit the measured data.

Deflection data for a second microrelay (designated A1000-10) fabricated with a 1000-micron long armature has been collected. The device employs a 10-micron actuation gap. Again, the actual deflection of the section of the beam over the gap area is not the full 10 microns experienced at the tip of the 1200-micron long beam. In this microrelay the measured displacement is limited to 7.6 microns. The collected data is plotted in figure 16-
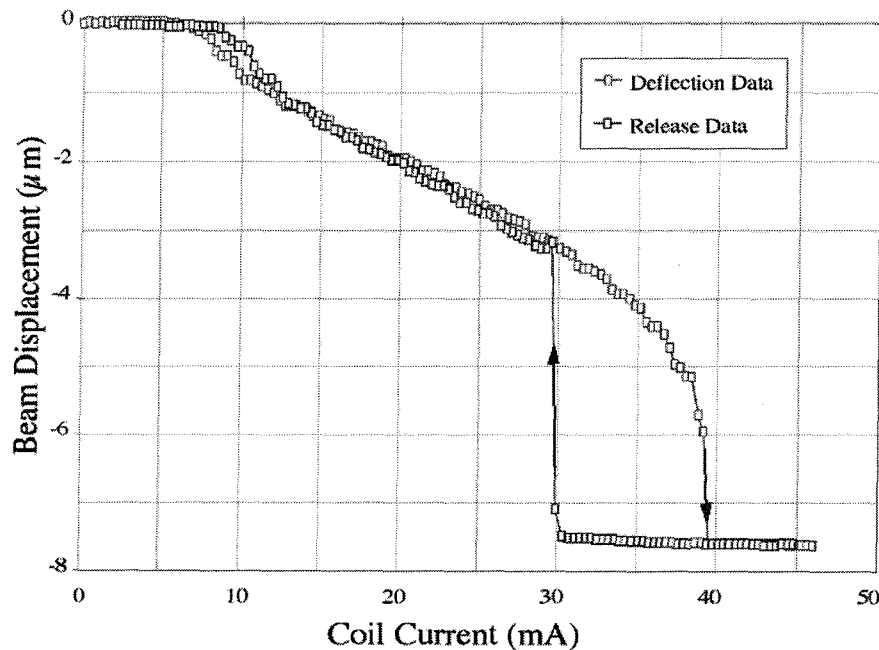


Figure 16-3: Experimental data showing beam deflection as a function of coil current. This data was collected from a microrelay with a 1000-micron long beam and a 10- micron actuation gap.

3. As with device A1000-5, snap-down and release hysteresis is seen. Full closure is realized with a current of 39 mA flowing through three serially connected planar coils (36 $\Omega$ resistance). Release occurs when the current falls below 29.9 mA. This corresponds to a required actuation power of 54.8 mW for contact make with a force of $\approx$ 44.1 $\mu$N being generated at a coil power of 32.2 mW.

Running the numbers shows that the expected force vs. current relationship. Equation 14.9 asserts that $F_{V-R\_magnetic} \propto (NI)^2$. The current required to hold the microrelay A1000-10 closed and the realized force is 1.38 and 2.00 times greater than found in device A1000-5, respectively. Squaring the difference in current levels gives 1.90 as the expected increase in force realized in A1000-10. This differs by only about 5 % from the calculated increase. This is very good agreement given the fabrication tolerances that can be expected.

Actuation of 500-micron long armature microrelays has also been demonstrated for devices having both 5 and 10-micron gaps. For the ease of reference, these devices are designated A500-5 and A500-10, respectively. No interferometric deflection data was collected from these microrelays. The spring constant for these beams is approximately 49 $\mu$N/$\mu$m. The deflection of the 500-micron armature portion of the 650 micron-long cantilever beams is calculated to be 3.5 and 6.7 microns for the 5 and 10-micron gap designs, respectively. This corresponds to deflection forces of 171.5 and 328.3 $\mu$N, respectively. As with the A1000 devices, these microrelays have three planar coils connected in series producing a coil resistance of 36 $\Omega$. For A500-5, coil current at contact

make is 68.3 mA (167.9 mW) and at break is 61.8 mA (137.5 mW). Make and break coil current values for A500-10 are 114.7 mA (473.6 mW) and 86.1 mA (266.9 mW), respectively.

Currents of 800 mA (limited by current source) have been passed through the planar coils for several minutes with no signs of failure or degradation. Calculations indicate that the magnetic circuit saturates at coil currents above 265 mA. The calculated maximum actuation force, limited by core saturation, is in the 2 to 3 mN range. Dropping the AC, 120 volt RMS line voltage (3.3 amps) from a wall socket across the coil results in a dramatic micro-explosion after which very little of the coil is left.

## 16.2  Microrelay Characterization and Performance

The ultimate measure of a microrelay is its electrical performance. Here the results of experimental testing are presented. Make and break performance has been investigated and data for a number of hot-switched currents have been collected. Following lifetime cycling, contact failure analysis has been performed. This work shows that the configuration and closing characteristics of the gold-to-gold contacts are not ideal. High-current switching for long lifetimes is not realized though the signal level performance is satisfactory.

### 16.2.1  Contact Resistance

Contact resistance under variable-reluctance actuation is measured using the 4-wire

method. The microrelays are wired such that when closed, the switched current runs down the length of the armature and out through both contact points. Therefore the resistance measurement is the sum of the contact resistance and the resistance of the 200-micron wide, 500-micron long cantilever beam. At the minimum coil currents required to bring the tip of the cantilever beam down into contact with the substrate, no electrical connection between the mating contact is seen. Typically the coil current must be increased by at least a factor of two before electrical contact make is seen. As shown by the Hosaka data in figure 10-2 this is to be expected as gold requires a contact force on the order of 100 μN for current to flow. The force generated in the microrelay at a coil current level producing physical contact make is used to bend the cantilever beam. The force arising from additional coil current is then used to squeeze the contacts together until electrical make occurs.

It is seen that the microrelays employing a 10-micron gap require a smaller proportional current increase as compared to the 5-micron gap devices. This is attributed not only to the fact that the coil current is already higher due to the larger force required to deflect the beam but also to the more pronounced snap-down action. In other words, the contacts in the A1000-5 devices come together "softly" while the contacts in the A1000-10 microrelays "slam" together. For the remaining experiments, the coil current used to close the microrelays was set to be at least 50% higher than the current level determined necessary to achieve electrical contact make. As this amount of current is believed to saturate the core of the A500 devices, the data was collected exclusively from 3-coil, A1000 devices. Typically the A1000-5 design was used with a coil excitation current of 120 mA (518 mW).

## 16.2.2  Make and Break Performance

Electrical testing of the switching capabilities of the armature microrelays has been performed.  All testing is done with resistive loads that are placed in series with the microrelay.  A DC voltage source is added to the circuit with power being connected to the resistor and ground to the relay.  An oscilloscope monitors the voltage drop across the relay.  A square wave generator circuit capable of driving up to 500 mA at greater than 10 kHz drives the coils in the microrelay.  Due to the lack of an automated system, all lifetime tests were hot-switched with 5 volts maintained across the contact gap when in the OFF-state.

Initial testing was performed with a near zero (0.1 $\mu$A) switched current.  At low switching frequency, nice, crisp make and break characteristics are seen.  No contact bounce is evident.  The best make and break speeds that have been measured are 0.06 msec and 0.08 msec (with an A500-5 microrelay), respectively.  The worst make and break numbers (with an A1000-5) are 1.1 and 1.3 msec with typical values being 0.4 and 0.55 msec.  Switching speed is defined as the delay seen between the transitions in the coil excitation waveform and the voltage drop across the microrelay waveform.  The values for typical switching speeds give maximum operating frequency of about 2 kHz.

Above 2 kHz, success of contact make from one cycle to the next is unpredictable.  Commonly seen are 3 or 4 good makes followed by several cycles where no or unstable electrical make is seen.  Squeeze-film damping of the moving armature is believed to cause this onset of switching failure.  The damping slows beam deflection and only by greatly

increasing the actuation force can higher frequency operation be achieved. Testing in vacuum would eliminate the damping and perhaps extend the performance range but no such measurements were made.

Measured contact resistance values are on the order of 250 to 350 m$\Omega$. For a given device, the contact resistance seems to be relatively stable over the life of the microrelay. For current levels above 1 mA some increase in contact resistance is seen. This is typically on the order of 10 to 20%. The initial contact resistance for a given device varies quite significantly from other microrelays in the same processing run. Over a sampling of 20 A1000-5 microrelays actuated with a 120-mA coil current, 4-wire contact resistances ranged from a low of 127 m$\Omega$ to a high of 765 m$\Omega$. This deviation is attributed as much to poor cleanliness of the contacts as to the capabilities of the different devices. It is very difficult to ensure that the entire photoresist sacrificial spacer layer has been removed before device testing begins. A long over etch is used but even after many hours in a heated photoresist stripper bath, debris is still found beneath the beams of many microrelays. Improving the agitation in the stripping beaker should eliminate this problem.

### 16.2.3   Lifetime Testing Performance

For the lifetime testing a switching frequency of 1 kHz and coil excitation current of 120 mA was used to drive the microrelays. All test were conducted under hot-switched conditions with 12 VDC across the contact gap. Only resistive loading conditions were used at currents of 0.01, 0.1, 1, 10, and 100 mA until contact failure occurred. Failure

was defined as an uncontrolled on-condition due to welding or high-contact resistance at closure. In the case of these relays, onset of failure was quite rapid, typically occurring within less than 1% of the total lifetime of the microrelay being tested and was characterized almost exclusively by extremely high (> 10 M$\Omega$) on-resistance. As with the MMC microrelay testing, the lack of an automated setup precluded continuous monitoring of switching performance. A similar procedure of constant attendance for the first one million cycles followed by intermittent monitoring was used in this case as described in section 12.2.4.

Lifetime performance results for the armature microrelays is presented in table 16-1. The 0.01 mA switching data shows that the mechanical life of the devices is greater than 1 billion cycles. No degradation in switching performance or contact resistance was seen during this test which was arbitrarily terminated after two weeks of testing. For the tests conducted with higher level currents, signs of impending failure typically do not appear

| Armature Microrelay Lifetime Testing Results | | |
|---|---|---|
| Load Switched | Current (mA) | Lifetime (cycles) |
| Resistive (12 VDC) | 0.01 | > 1 billion |
| Resistive (12 VDC) | 0.10 | 10 to 100 million |
| Resistive (12 VDC) | 1.00 | 0.5 to 5 million |
| Resistive (12 VDC) | 10.0 | < 500,000 |
| Resistive (12 VDC) | 100 | < 1000 |

Table 16-1: Armature microrelay hot-switched lifetimes for a range of operating currents and conditions.

until just before failure.  Contact make becomes inconsistent and when achieved, the contact resistance is quite large.  This situation quickly leads to total failure within, typically, a few thousand cycles.  Failure due to welding when hot-switching the resistive loads is seldom seen.

As expected, lifetime is dramatically reduced at the higher current levels.  Failure rates above 10 mA are so quick that the microrelays with gold-to-gold contacts have little practical use in the target application at these currents.  At 10 mA and below, the performance of the contacts is found to be satisfactory for a number of reasonable uses in the areas of signal switching.

## 16.3    Contact Failure Phenomena

As with the MMC microrelays, the armature type devices show evidence of melt, splatter are redeposition of metal from one contact to the other.  Unlike the larger device, the armature microrelays appear to create point contacts on closure with failure arising from the lack of a thick stationary contact.  Photographs taken with an SEM are shown in figures 16-4 and 16-5.  In figure 16-4 the end of the armature is seen with the integrated contact pads.  The beam has been elevated slightly to allow the stationary contact-mating region to be viewed.  Readily seen are two very small ablation regions, on corresponding to each of the armature contact pads.  The small size of these points indicates that the end of the beam strikes the substrate tip first and that there is insufficient force generated by the magnetic actuator to create any substantial bowing of the armature and thus subsequent sliding of the

armature contact over the substrate metal.  This is not surprising.  The fact that the contact

faces are not pulled together in a parallel manner is also to be expected due to the location of

the contacts at the end of the deflected beam.  After this photo was taken, the sample was
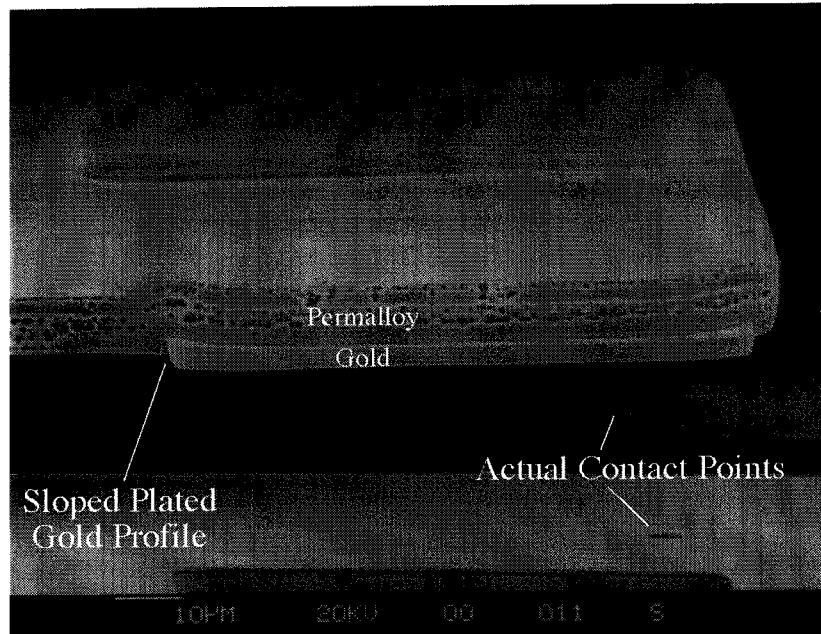


Figure 16-4: Plating the gold contacts with inverted sloped sidewalls permits the subsequent permalloy overplate to lock them into the tip of the cantilever beam.



(a)                                                    (b)
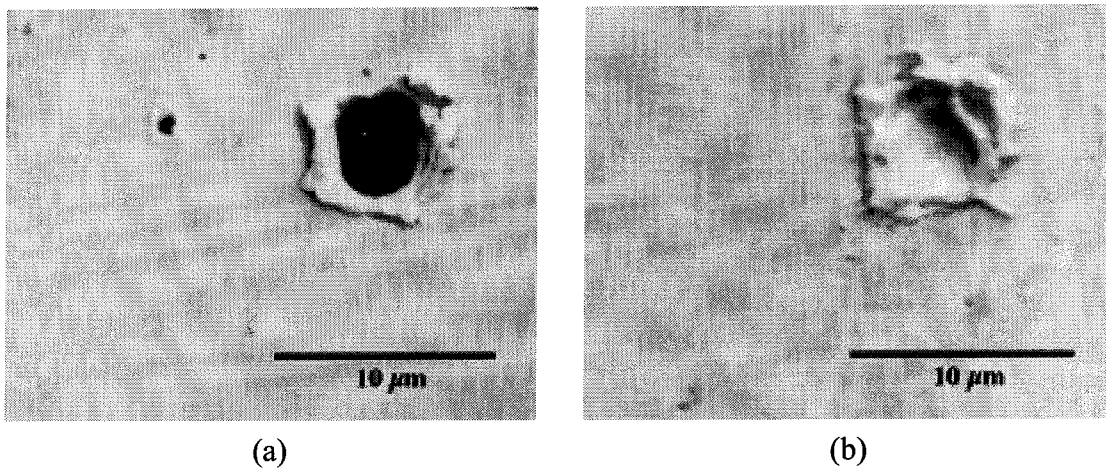
Figure 16-5: SEMs of mated contact failure points.  (a) stationary contact gold with hole melted through to the underlying substrate.  (b) moving contact gold with mound of gold transferred from the hole seen in (a).

removed from the SEM and the permalloy beam pulled from the substrate and flipped over.

Shown in figure 16-5 are two pictures of one of the ablation points seen in figure 16-4. In figure 16-5.a is the armature contact wear point while the corresponding area in the stationary contact metal is shown in figure 16-5.b. Clearly, the both areas show metal melt, reflow and redeposition. A mound of gold has formed on the armature contact. In the case of the stationary metal, a hole through its thickness has exposed the underlying insulating substrate. This metal, which was evaporated, is only 0.5 to 1.0 microns thick. As a result it can withstand only survive a small amount of redeposition wear. Such features account for the extremely high on-resistance of the microrelays at failure. Once the substrate has been exposed, the mound on the armature contact can remelt until a peak forms in the center or near the periphery of this hole. Any subsequent closures have gold mating to insulator.

Ideally, the stationary contact material would be thick enough to allow the moving contacts to wear into it sufficiently to produce a relatively large contact area. From the SEM photos, however, the actual mating area is only approximately 10 microns in diameter. For a 10 mA switched signal, the current density in such a contact point is > 12 $kA/cm^2$. This extremely high and accounts for the very poor lifetime values above the 1 mA level.

## 16.4 Planar Coil Inductive Measurements

A final measurement of interest that has been conducted on the armature microrelays

is inductive measurements of the planar electromagnetic coils.  While designed to energize

the magnetic circuit that produces the closure forces for the microrelays, the planar coils can

also be used as passive inductive components.  Measurements of devices with and without

the permalloy core of the microrelay have been made.  The resulting inductance as a

function of frequency is displayed in figure 16-6.  This data indicates that the air core coil

consisting of 20 turns with a footprint of approximately 1 mm-square have and relatively

constant inductance value of approximately 0.165 µH over the frequency range from 1 to

20 MHz shown.  For a coil of the same geometry but with a permalloy core, the inductance

value is, on average, approximately 0.65 µH.  This is 3.93 times larger than the air core

coil but it suffers from a non-flat frequency response.  At 1 MHz, the inductance value is as

high as 1.35 µH while a 20 MHz it falls to below 0.50 µH.



**Frequency Response of Planar Coils**
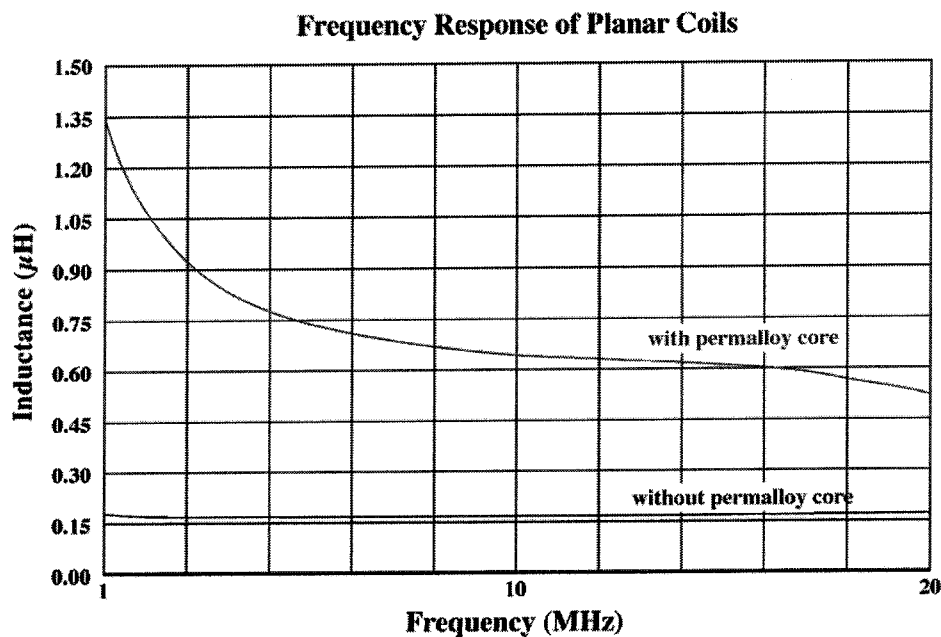
Figure 16-6:  Inductance as a function of frequency for the planar coils used in the armature microrelays.  Data is shown for coils with and without permalloy cores.

The quality factor, Q, is a value often quoted as a measure of worth of an inductor. For an RLC series circuit:

$$Q = \frac{2\pi f_n L}{R} \quad => \qquad \text{eqn. 16.1}$$

L = coil inductance        R = coil resistance        $f_n$ = resonant frequency

For these coils, the resistance of the 20 turns is approximately 12 $\Omega$. Choosing to set the resonant frequency at 10 MHz results in Q values of 0.86 and 3.4 for the air core and permalloy core coils, respectively. Discrete inductor components typically have quality factors on the order of 3 to 5.

## 16.5    Armature Microrelay Conclusion and Future Work

Micromachined electromechanical armature microrelays have be designed, fabricated and tested. Electromagnetic operation based on the variable reluctance actuator principle has been demonstrated using planar copper coils and high quality permalloy cores. Devices with air gaps ranging from 5 to 10 microns have been produced and actuation forces in excess of 328 $\mu$N are achieved at coil powers less than 500 mW. Contact resistances as low as 127 m$\Omega$ have been realized with the typically value ranging from 250 to 350 m$\Omega$. Reliable electrical make and break of the contacts is seen at speeds up to the kilohertz range. Device lifetimes are range from several hundred thousand to several million cycles when hot-switching currents of 10 mA to 1 mA, respectively.

Failure occurs due to contact wear characterized by metal melt and material transfer. The placement of the moving contact points at the end of a cantilever beam is found to be non-ideal for this application. The tilting action of the beam results in extremely mating surface areas between the closed contacts. The resulting current crowding is not conducive to long microrelay lifetimes.

With the proof of concept demonstrated, the next generation of fabricated microrelays should incorporate several design changes. Foremost is separation of the mechanical and magnetic components of the relay. Presently, the break force in the microrelay is provided by the restoring force of the cantilever beam. This beam is also the choke point in the flux path of the magnetic circuit. It is very difficult to optimize this member for both mechanical and magnetic operations. Replacing the beam with a permalloy "cap" attached to the substrate with torsional or circumferential cantilever beams is one attractive alternative. This approach will maximize the cross-sectional area of the magnetic flux path. Likewise, the break force for the microrelay can be designed independent of any other aspect of the device.

An increase in the number of turns of the coil will have a very significant effect on the actuation forces that can be generated as well as the coil powers required to produce them. Doubling the turn count will increase the realized force for a given current by a factor of four. Since it is beneficial to keep the overall footprint of the microrelays to a minimum, this enhancement requires that two or more levels of coil material be used. This, in turn, introduces more levels of insulation and high non-planarity of the resulting

surfaces. Regardless, the added fabrication difficulty is deemed acceptable for the expected increase in device performance.

Different contact materials should be investigated. As mentioned in the chapters covering the MMC microrelay, traditional contact metals such as silver, rhodium, and ruthenium can be electroplated. Research into which of these materials performs best in a micromachined device could lead to microrelays capable of matching or exceeding commercially available products such as reed relays.

Finally, the unique benefit of batch fabrication and to manufacture of integrated relay circuits should be explored. Through proper design and minimal additional processing steps, complex circuits capable of replacing large, heavy, and expensive printed circuit boards can be realized.

# APPENDIX N1

# PROPERTIES OF BURIED
# ETCH-STOP LAYERS

The thickness of the thin silicon membranes, formed during the fabrication of neurochips and neuroprobes, is set by a specially doped silicon buried layer. In several of the neurowell designs, this buried layer also defines the thickness of the grillwork cover. Certain silicon etchants do not attack doped silicon, or attack it very slowly. These same etchants will etch lightly doped silicon aggressively. The high selectively achieved with such chemicals allows large, thin membranes to be formed with minimal thickness variations across a wafer. Proper selection of the doping components allows optically smooth surfaces to be realized with near-zero stress in the material.

## N1.1 Buried Layer Wafers Overview

The wafer used as the starting substrate for the neurochips and neuroprobes has three distinct silicon layers. The majority of the wafer is lightly doped (1 to 20 $\Omega$-cm or 5 x $10^{14}$ to 2 x $10^{16}$ dopant atoms/cm$^3$ [169]) silicon approximately 500 microns thick of the

the last three to four years, the basic cross section of the SOI wafers is the same as the epi wafers. Instead of a buried, heavily doped silicon layer, the SOI wafers have a thick (up to several microns) buried oxide layer. SOI wafers allow a larger range of etchants and etching conditions to be used while still maintaining excellent etch stop selectivity. Most notably, epi-wafers are best etched with EDP, an etchant being phased out of commercial use. SOI wafers permit the use of KOH or TMaH, which are much less hazardous solutions.

## N1.2 Heavily-Doped P-Type Silicon Buried Layers

In specifying the initial thickness and doping concentration of the p-type etch-stop layer, several parameters must be considered. When the etch-stop layer is used as neurowell grillwork, as in the case of the prototype neurowell, the target thickness of the grillwork (2 microns) must contain the minimum p-type doping concentration necessary to act as an etch-stop. This concentration must be maintained until the neurowell grillwork is formed. In the fabrication process, high temperature steps are used to lay down materials such as oxide and nitride. Out-diffusion of the epi-layer dopants into the bounding lightly doped silicon layers occurs during these steps. Consequently, the starting thickness of the heavily doped layer decreases during fabrication. Calculations show that the predominant out-diffusion occurs during the 3 hour, 1050 °C thermal oxidation step performed at the beginning of the processing run.

## N1.2.1    Out Diffusion Analysis for Buried Boron-Doped Epi-Layer

The concentration of the dopant in the heavily-doped epi-layer can be modeled as a function of linear distance and time using Fick's second law of diffusion [169]:

$$\frac{\delta C(y,t)}{\delta t} = D\frac{\delta^2 C(y,t)}{\delta y^2}$$    eqn. N1.1

where:

   D = diffusion constant [cm²/sec]    y = axis in direction of solute flow [cm]

   C = solute concentration [atoms/cm³]    t = diffusion time [sec]

In the case of a heavily-doped buried layer, one can approximate that there is a fixed total amount of dopant per unit are $Q_T$ that diffuses into the bounding lightly doped silicon and that all of the dopant atoms remain in the silicon. Using the coordinate system shown in figure N1-1, the boundary conditions are:

   C(y,0) = 0    $C(\infty, t) = 0$    $\int_0^\infty C(y,t)dx = Q_T$

Searching for a solution to equation N1.1 that satisfies these conditions leads to:

$$C(y,t) = \frac{Q_T}{\sqrt{\pi Dt}}\exp\left(-\frac{y^2}{4Dt}\right)$$    eqn. N1.2

with [164]:

$$D = D_0 \exp\left(-\frac{E_A}{kT}\right) \qquad\qquad \text{eqn. N1.3}$$

For boron diffusing in silicon [164]:

$$D_0 = 10.5 \text{ cm}^2/\text{sec} \qquad E_A = 3.69 \text{ eV} \qquad k = 8.617 \times 10^{-5} \text{ eV/K}$$

$$\Rightarrow D_{\text{B-in-Si}} = 9.10 \times 10^{-14} \text{ cm}^2/\text{sec}$$

In order to calculate the initial etch-stop layer thickness, the minimum concentration of dopant required to act as an EDP etch stop and the initial concentration of the dopant must be known. These values are:

$$C_{\text{min}} \geq 5 \times 10^{19} \text{ atoms/cm}^3 \qquad\qquad C_{\text{doped}} = 2 \times 10^{20} \text{ atoms/cm}^3$$

Since the system is symmetric (the dopant from the buried layer is out-diffusing into both bounding lightly doped silicon layers), the coordinate system is best placed in the middle of the etch-stop layer as shown in figure N1-1. The initial thickness of the epi-layer needed is then calculated using half the target grillwork thickness ($\approx$ 2 microns) or 1 micron.

As noted previously, the longest and highest temperature step, the one that most affects the out-diffusion, is the 3-hour, 1050 °C thermal oxidation performed at the beginning of the process. Rearranging equation N1.2 gives:

$$C(y=1\mu m, t=10800s) = C_{\text{min}} \geq 5 \times 10^{19} \text{ atoms/cm}^3$$

$$\Rightarrow Q_T \geq 3.534 \times 10^{16} \text{ atoms/cm}^2$$

$$\Rightarrow Y_0 \geq 2\frac{Q_T}{C_{\text{doped}}} = 3.32 \text{ microns}$$

where $Y_0$ is the required thickness of the starting heavily doped buried layer (Note: the factor of 2 is due to choosing to set the coordinates at the center of the layer). In practice, a buried layer initially 4 microns thick is used. The slightly thicker value is chosen to accommodate additional high temperature steps (such as nitride at 850 °C) in the fabrication process.

The previous calculations pertain to a purely boron-doped layer. In practice, such an etch-stop works very well with EDP. It shows negligible etch rate in 100 °C solution allowing easily for several hours of over etch. The grillwork formed from such a layer is, as desired, several microns thick as can be seen in figures 3-8 and 3-14.

## N1.2.2     Linen-Pattern Phenomenon

To the naked eye, the membrane formed using a boron-doped etch stop is mirror smooth and shows minimal deformation due to stress introduced by the boron dopant. Unfortunately, viewing with a microscope shows the surface finish has a peculiar pattern. Shown in figure N1-2 the membrane appears to have closely spaced lines running vertically and horizontally over its surface. This "linen pattern" is believed to be caused by stress dislocations in the heavily tensile-stressed boron-doped layer. It is a purely optical property. Viewing with an SEM shows no such physical features. It is extremely difficult to visual the fine neurites growing from neurons cultured on such a surface since the axons and dendrites tend to be of similar size to the "threads" in the linen pattern

## N1.2.3     B-Ge-Doped Etch Stops

To solve the problem of the linen pattern, the use of a boron-germanium-doped

etch-stop layer was explored.  The tensile stress in the boron-doped etch-stop layer arises

from the boron atoms being smaller than the silicon atoms comprising the lattice into which

they are introduced.  Adding germanium, an electrically inactive dopant that is physically

larger than silicon atoms, cancels the size mismatch of the boron.  By choosing the proper

germanium dopant concentration, it is possible to achieve zero stress in the doped buried
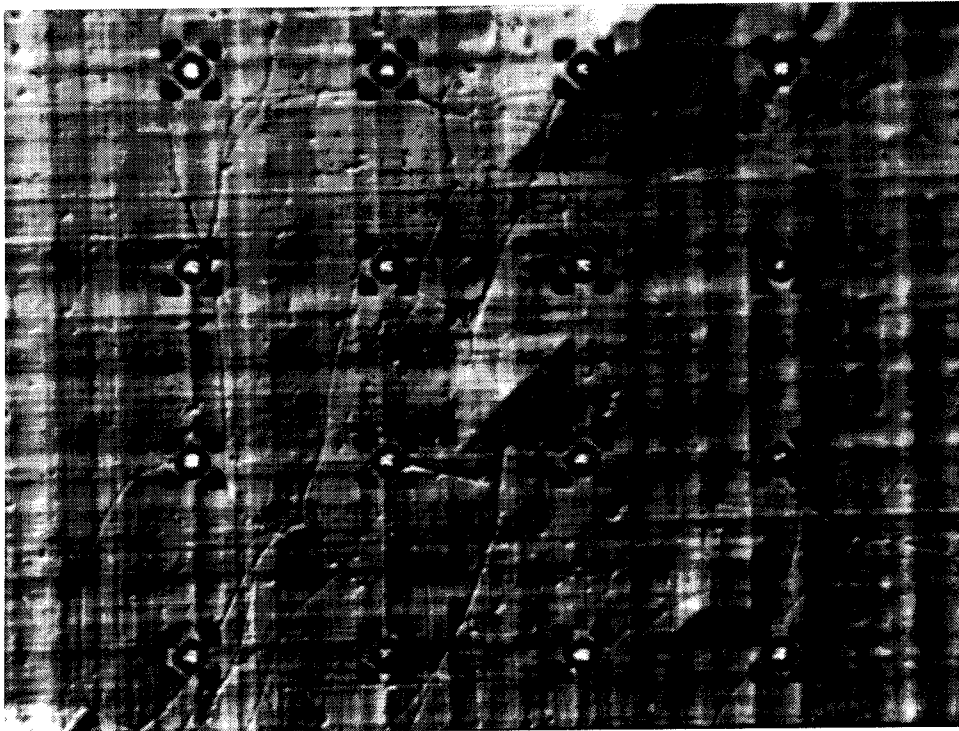


Figure N1-2:  This Nomarski photograph shows the typical 4 x 4 array of wells used in the neurochip. The linen pattern is an optical artifact produced by stress in the boron-doped epi-layer. In addition to this pattern, pyramid and mesa structures (see center and lower right of photograph) can also be seen. None of these features are actually present. When viewed in a scanning electron microscope, this surface appears flat except for the neurowells themselves. The wells in this photograph have neurons growing in them. The very fine lines running at angles between the wells are neurites. As can be seen, they are very hard to distinguish from the background linen pattern.

# DEEP CAVITY PHOTOLITHOGRAPHY

Key to the successful fabrication of the neurochip and neuroprobe dies is the ability to perform fine lithography on a thin membrane inside a deep, bulk micromachined cavity. Several challenges must be overcome to accomplish this. First, photoresist of adequate thickness and uniformity must be deposited. Depending on whether the photoresist will be used as a plasma or a wet etch mask, a number of different concerns must be addressed. Once laid down, exposing the resist with adequate focus at the bottom of the cavity must be achieved.

The presence of fragile membranes on the face of the wafer precludes the use of vacuum to hold the wafer in place during photoresist spinning. To overcome this obstacle, a special non-vacuum chuck has been used with great success. Three recessed, flat head screws are located with 120 degree spacing around the edge of the chuck on a circle slightly larger than the diameter of the wafer (4 inches). No conical recess has been machined into the screw holes resulting in the heads of the screws standing approximately one wafer thickness proud of the surface of the chuck. As the heads are conically shaped, their edges extend over perimeter of a wafer loaded into the chuck and act as near-zero force clamps. To load a wafer, it is placed in the chuck so that its major flat is facing one of screws. The wafer can then be rotated until an uncut wafer edge is beneath the three screw heads (see

figure N2-1. A small o-ring is typically used as a "washer" for one of the screws. This provides for overall flexibility of the chuck. The slight give in the o-ring eliminates the need to achieve tight tolerances when machining the chuck. Additionally, a range of different wafer thicknesses can be adequately held with only a slight adjustment to a single screw.

Photoresist is applied by filling each cavity with several drops of resist and spinning the wafer. The resulting film is non-uniform with variations as much as 50 % from center to edge. Still, a usably uniform thickness is achieved over a relatively large region at the center of the membrane. Thicknesses from 1 to 5 microns have been used. Exposure of the central region is possible assuming that the membrane is flat and that proper focusing is accomplished. The coverage of the sharp corners present at the membrane-to-bulk silicon interface around the perimeter of the cavity is very poor. When the photoresist is to be used as a plasma etch mask, these areas must be hand painted with a very fine brush to ensure an adequate thickness of photoresist is present. In the case of a



(a)                                    (b)
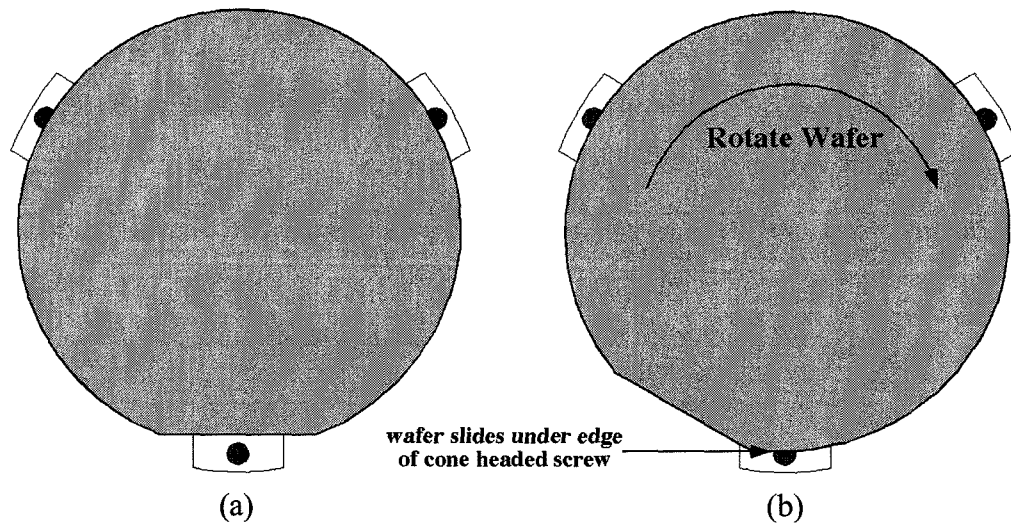
Figure N2-1: A schematic showing the (a) intial placement of the wafer on the non-vacuum chuck so that the major flat is next to one of the three cone headed screws. (b) Rotating the wafer slightly slides the edge of the wafer beneath that screw, locking the disk to the chuck manually and allowing it to be spun at high speeds without having to have it held by vacuum.

wet etch, such as BHF, the photoresist deposited during spinning, though extremely thin, is still usually sufficient to protect the edges.

Focusing at the bottom of the cavity cannot be done using a contact aligner. Attempts have been made but even at the bottom of cavities only 100 microns deep, feature resolution better than 7-8 microns cannot be achieved. For the neurowell grillwork, lines 3-4 microns wide must be exposed at the bottom of a 500-micron cavity.

By using a GCA 4800, 10X projection stepper, the focusing requirements are met. This approach places a restriction on the size of the smallest cavity that can be exposed. The stepper focuses on each die on the wafer during exposure using an infrared beam (see figure N2-2). The beam is aimed at the center of each die and bounces from the wafer to a photodiode. The signal from the diode is amplified, and the focusing stage of the stepper is adjusted until the strength of the infrared signal surpasses a preset threshold. Designed for use in IC chip manufacture, the stepper expects a flat surface on a wafer of within a certain thickness. A warped membrane or an obstruction can deflect the bounced beam away from
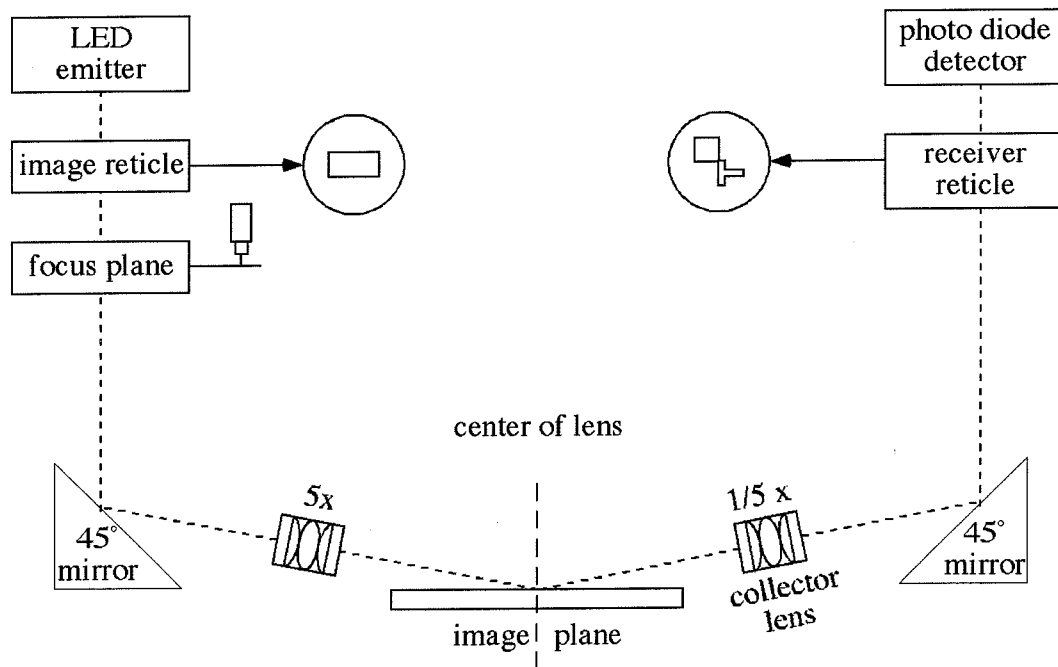


Figure N2-2:  Auto-focus illumination path of GCA 480 stepper.

the photodiode making it impossible to attain the focusing signal.

The size of the focusing beam and the depth of the cavity set the minimum size of the membrane. By shining white light through the lenses used by infrared sensing beam, and assuming that the optical properties of the system are approximately the same for both infrared and visible wavelengths, the spot size projected on the wafer was measured as approximately 2 x 4 mm$^2$ (see figure N2-3). The angle, $\theta$, at which the beams hits the die (see figure N2-4) is 11 degrees. This is quite large when compared with other types of projection steppers where the projected angle can be as small as 3-4 degrees. The large angle is fortuitous because it makes it easier for the beam to bounce in and out of the cavity.

The membrane-die wafers must be loaded into the stepper on a carrier wafer. If placed on the stepping stage without the carrier, the effective thickness of the dies seen by the stepper is just the thickness of the membranes (20 microns). By placing a 500-micron thick wafer beneath the neuro wafer, the wafer thickness seen by the stepper is 520 microns, which is within the tolerance of the tool. It should be noted that simply stacking the two wafers together and carefully loading them onto the stepping stage is adequate. No



infrared focusing beam, 2 mm x 4 mm          silicon wafer          die that is being exposed, 1 cm x 1 cm
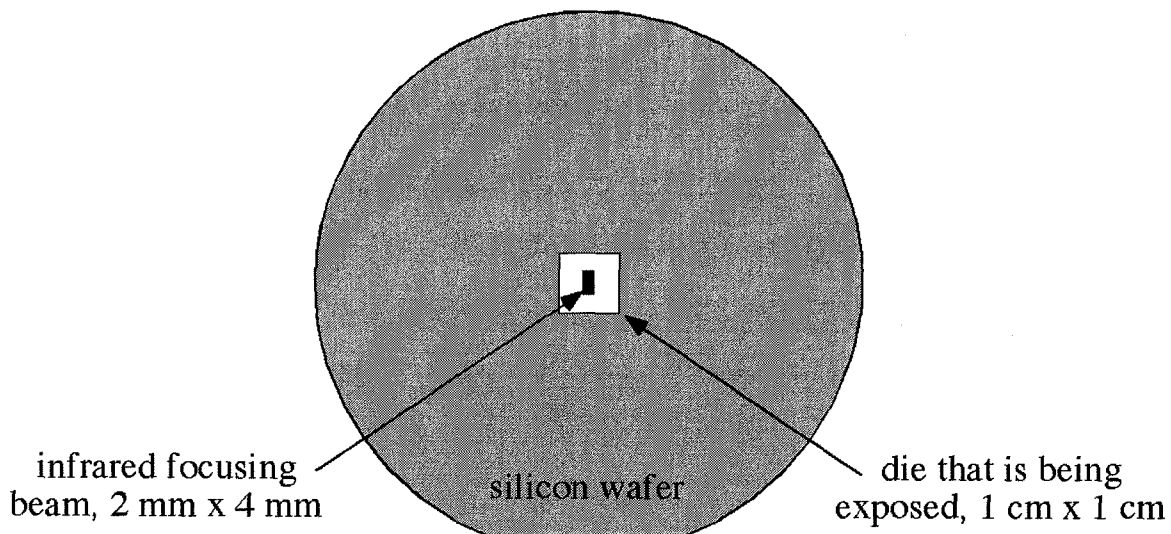
Figure N2-3: The size and the relative position of the infrared focusing beam with respect to a die on the silicon wafer.

adhesive is needed between the two substrates.

The smallest cavity in which successful focusing is possible is 9 x 3 mm. Initial neurochips were fabricated with this size membrane. The neuroprobe fabrication requires a cavity of at least 9 x 4 mm due to the length (4 mm) of the silicon needles desired. The latest fabrication runs utilize a 9 x 5 mm cavity opening (8 x 4 mm membrane). It is found that the larger size does not make the membranes, nor the wafer as a whole, significantly more fragile. It does greatly reduce the complexity of the preparations for and execution of exposures. A die-to-die step size of 12.7 mm is used for the exposure resulting in 7 rows and 7 columns on a wafer. Since the substrate is round, only 3 of the rows have the full 7 dies. Two rows have 5 dies and the remaining 2 rows have 3 dies. The maximum yield of neurochips from such a wafer is 37. For neuroprobes, with a typical die containing 3 devices, the maximum yield is 111.



Figure N2-4: The focusing beam bouncing in and out of the cavity formed in the silicon wafer.

## ACCURATE TWO-SIDED ALIGNMENT ON SILICON WAFERS

The fabrication processes used to produce the neurochips and the neuroprobes require that fine features be formed on both sides of the substrate wafer. Furthermore, fine alignment between the features on both sides must be achieved. Most notably, the 6-micron diameter electrode on the front side of the wafer must be positioned in the center of the neurowell microcavity that is defined from the backside. Several techniques can be employed to meet this requirement. In general, all of the approaches rely on alignment to a set of marks permanently etched into the wafer. The differences arise in whether the marks are placed on both the front and the back or just on the front. In the first case, precise alignment between the front and back marks must be achieved when they are first made on the substrate. In the second case, special optical systems must be employed during every mask step performed on the backside of the wafer that permit viewing of the alignment marks on the front side of the substrate.

## N3.1 Alignment Accuracy Limitations

In analyzing the accuracy of different front-to-back alignment techniques, several issues must be addressed. The most obvious consideration is the ability to maintain precise alignment from mask step to mask step. This challenge has been addressed by the IC industry and tools capable of submicron mask-to-mask alignment are commercially available. Not typically considered, but a source of significant front-to-back alignment error, is the substrate wafers themselves. As denoted by the wafer manufacturer, the specified errors in surface crystal orientation and slice taper across the wafer must be considered when choosing a front-to-back alignment technique. This is most important when anisotropically bulk micromachined structures on one side of the wafer must align through the thickness of the substrate to features on the other side. In practice, slice taper (typically ≤ 10 microns across the wafer [168]) has negligible affect on alignment accuracy (<< 1 micron) and only the crystal orientation need be considered [170].
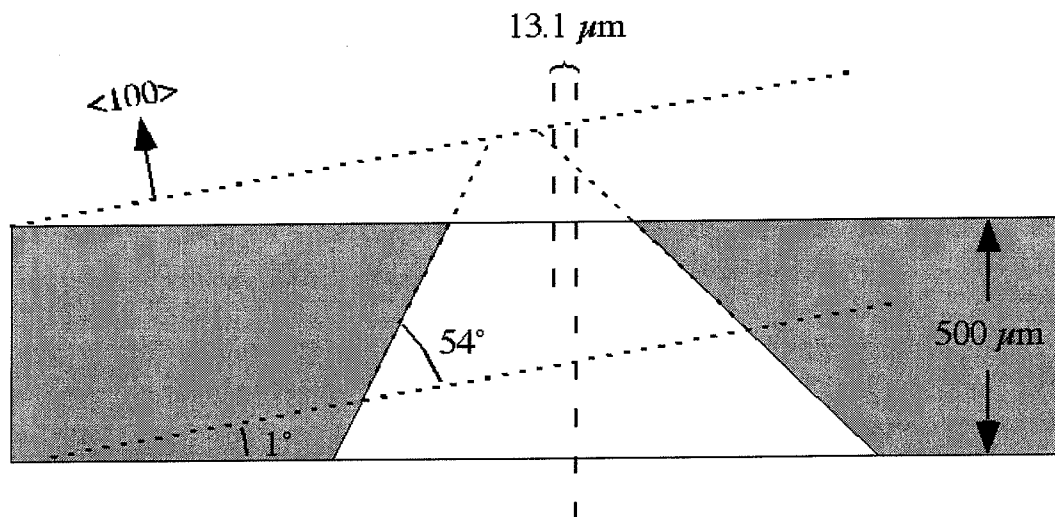
Figure N3-1: Influence on the alignment accuracy of a 1° offset of the wafer with respect to the <100> surface orientation.

Limiting this analysis to 4-inch, <100> single-crystal silicon wafers, the typical manufacturing tolerance for surface orientation offset is $\pm$ 1 $°$. Assuming the worst case of 1$°$ offset, the slopes of the sidewalls of a cavity formed using wet anisotropic silicon etching is not the expected 54.74 degrees. Shown in figure N3-1, the resulting cavity becomes deformed and the location of the center of the membrane being formed at the front side of the wafer shifts slightly. On a 500-micron thick wafer, the magnitude of the shift is:

$$\Delta X_{center} = \frac{1}{2}\left(\frac{1}{\tan 53.74°} - \frac{1}{\tan 55.74°}\right) = 13.1 \text{ microns} \qquad \text{eqn. N3.1}$$

This large error significantly degrades the accuracy of the simple alignment techniques described in section N3.3 below. In many cases, tens of microns of misalignment are acceptable. In the case of the neurowells, such inaccuracy would make it impossible to successfully fabricate neurochips and neuroprobes.

## N3.2    Through-Wafer Two-Sided Alignment

In the pursuit of high accuracy, extremely precise front-to-back alignment, the most reliable technique utilizes cavities extending through the full thickness of the wafer. The size and shape of the holes is typically unimportant. The method used to produce the cavities, however, should be the same as that used to form the features that are to be aligned. The ability to see through the full thickness of the wafer and view some form of mark on the opposing side makes possible the excellent alignment results that can be

achieved with this technique.  In general, the through wafer approach does require several preparatory steps be added to the overall fabrication process of a given device.

### N3.2.1  Caltech Novel Extra Accurate Method

Developed specifically for the chronic neural interface project, this technique achieves better than 1-micron front-to-back alignment accuracy.  Reported in [171], this approach forms alignment marks on the front side of the wafer then etches a cavity through the thickness of the substrate.  When viewed from either side, the alignment marks are readily visible and can be keyed to in a standard exposure tool.  The etched cavity may be through a thin membrane, as in the case of the neural devices in this thesis, or through the entire thickness of the substrate wafer.  The schematics shown in figure N3-2 illustrate the alignment structures that are formed.

This method achieves the accuracy necessary to fabricate the neurowells.  By imprinting standard alignment keys into the wafer, no special skills of the operator are required.  The affect of variations in the surface crystal orientation on alignment accuracy is removed and the alignment marks are visible from both sides of the substrate.  This allows standard photolithography tools and processing to be used and provides for accurate and inexpensive front-to-back alignment.

### N3.2.2    Alignment to Transparent Membranes

Double-side alignment can be achieved by keying to the center of a small transparent diaphragm.  Very similar to the method described in section N3.2.1, this

approach requires that a cavity extend from one side of the wafer to the other. A membrane typically caps one side of this cavity to permit normal photoresist spinning in subsequent processing steps. The membrane should be transparent so that its boundary is readily visible in the alignment tool. The cross hairs of the exposure reticle are then keyed to the center of the diaphragm. This requires that the operator be able to gauge the precise location of the center point. Alternatively, if a stepper is used for the exposure, the corners of the membrane (assuming anisotropic etchant is used to form the cavity) can act as initial alignment keys. In this case, the precise size of the membrane must be known so that the proper offset can be programmed into the tool. Described in [165], Kim, et al., claimed better than one micron alignment accuracy can be achieved. Used extensively in the fabrication of the electromagnetic armature relay described in this thesis, alignment accuracy in the 1 to 2 micron range has been repeatedly attained. Since the accuracy of the exposure tool, a GCA 4800 10X stepper, is specified to be 1 micron [162], the less than one micron claim by Kim seems reasonable.



(a)                     (b)                     (c)
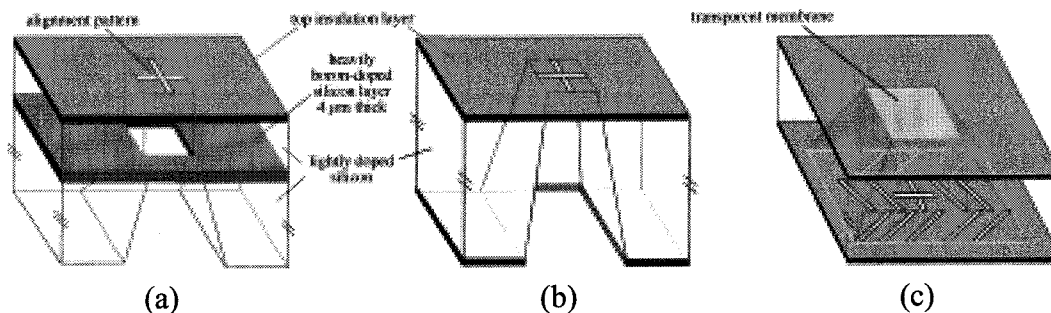
Figure N3-2: Three structures that can be formed to create very accurate front-to-back alignment marks. (a) Alignment across a thin membrane. (b) Through-wafer alignment hole with patterned membrane on one side and fully opened hole on the other. (c) Through-wafer alignment hole will intact transparent membrane on one side through which an alignment mark in a patterned membrane on the other side can be viewed for alignment.

# N3.3    Two-Sided Alignment without Through Holes

In many cases, forming a hole through the thickness of a wafer is not acceptable. If the design does not require highly accurate mating between the components on each side of the wafer, several other techniques can be employed. Ease of use is the main draw of these approaches as well as, in some cases, inexpensive tooling.

## N3.3.1    Infrared Alignment

Silicon wafers are transparent to infrared (IR) wavelengths. Although relatively expensive, IR backside and double-side mask aligners are commercially available. Their basic operation is simple. Alignment marks are first formed on the front side of a substrate. Standard alignment processes and tools are used for the mask steps performed on that side of the wafer. To expose features on the back, the silicon substrate is placed face down on a chuck containing an IR light source. Using an IR sensitive video camera, the marks on the front side can be viewed through the thickness of the wafer providing for relatively good double-side alignment. Typical IR backside aligners have an absolute limit for viewing of about ±6 microns. Double side IR mask aligners have an alignment accuracy of no better than ±2 microns [171]. As noted above, surface crystal orientation can further degrade the realized alignment between features on opposing sides of the wafer. Additionally, this technique requires that no IR-opaque materials be deposited over the alignment dies. Still, IR alignment is straightforward and can be used satisfactorily for many micromachining processes.

## N3.3.2  Sandwich Mask Tools

For inexpensive double-side alignment, a technique based on a sandwich mask tool can be used. This device has two plates that are bound together by a hinge in a manner similar to a book. Each plate contains a set of alignment marks . When hinging the two plates together, these two sets of marks are aligned to each other. A wafer coated front and back with photoresist can then be slide between the two plates and exposed with an ultraviolet light canon. Subsequent developing of the photoresist and transferring of the exposed pattern into the substrate with a quick silicon etch produces permanent front-to-back alignment marks on the wafer. It is estimated that a theoretical alignment accuracy of no more than 1 micron across a 250 micron thick, 2 inch wafer [172]. In the Caltech micromachining group, the best accuracy obtained with such a tool on 500-micron thick, 4-inch wafers is approximately 5 microns. Machining cost of such a sandwich tool can be as low as several hundred dollars. The major disadvantage with this technique is that any alignment error present in the tool is always transferred to the wafers on which it is used. The error introduced in this fashion varies and depends on the design and implementation of the tool [163]. To correct this type of error, realignment of the plates in the tool must be performed. The manner in which the two plates are attached typically makes this process very difficult.

# NEURON IMPLANTATION INTO NEUROWELLS

Neuron implantation into neurowells begins by flooding a suspension of freshly dissociated neurons in culture serum over the surface of a neurochip basin or a neuroprobe needle  The silicon device is placed in a $CO_2$ incubator to allow many of the neurons to settle onto surfaces.  After approximately half an hour, work is resumed on the stage of an upright microscope equipped with Nomarski optics, which improves the visibility of the semi-transparent neurons.

In initial work, cells were manipulated into wells by a pick-and-place method.  A pipette was drawn down to form a tip approximately 20 microns in diameter.  The larger end was attached to a suction device capable of drawing in very small volumes of solution. The fine tip was placed in the medium and an appropriate neuron located and sucked into the end of the pipette.  X-Y manipulators then moved an empty well in a neurowell array beneath the end of the tip.  The neuron was then slowly expelled from the pipette and allowed to fall through the central hole into the grillwork and to the bottom of the neurowell.

The pick-and-place method proved to be too cumbersome to allow rapid implantation of a neurowell array.  It is very difficult to adequately control the distance into the pipette that the neuron is pulled when it is sucked from the surface of the silicon.  If it

does not remain in view at all times, it essentially becomes lost and a new neuron must be chosen. Likewise, when pushing the cell out the tip, the speed at which it is expelled can be sufficient to blow it away from the neurowell and make the implant unsuccessful.

The more successful method of neuron implantation takes on the character of a game of micro-hockey. Instead of a hollow pipette used for sucking, the fine glass tube is sealed after it is pulled. This is done by holding the tip over a red-hot platinum wire and melting the glass tip into a smooth, round end. Proper technique allows the terminal 2 mm or so of the tip to be bent at an approximate 45° angle creating a "micro-hockey stick." Attached to a manipulator arm, and with the silicon device containing the neurowells sitting on an X-Y stage, the micro-hockey stick is used to prod and push neurons to empty wells. Once maneuvered into the central hole of the grillwork, the micro-hockey stick is placed over the well for 10 to 15 seconds to ensure that the neuron remains inside and falls to the floor of the microcavity. A series of screen captures showing this procedure for implanting a neuron are shown in figure N4-1. Team members Mike Maher and Hannah Dvorak developed this method and became quite efficient with the technique. To implant all 16 wells in the 4 x 4 array of a neurochip typically takes them less than 15 minutes.

Once each well has been filled with a neuron, the setup is left undisturbed on the microscope stage for approximately 30 minutes. This appears to give the neurons enough time to attach securely to the floor of the wells and decreases the likelihood that they will be dislodged by subsequent activities. After the 30 minutes has passed, all neurons in the field within 1 to 2 mm of the neurowell array are removed by suction with a 40 micron diameter glass pipette attached to a syringe. This ensures that all neurite growth seen in the array area originate from the neurons that were implanted in the neurowells.
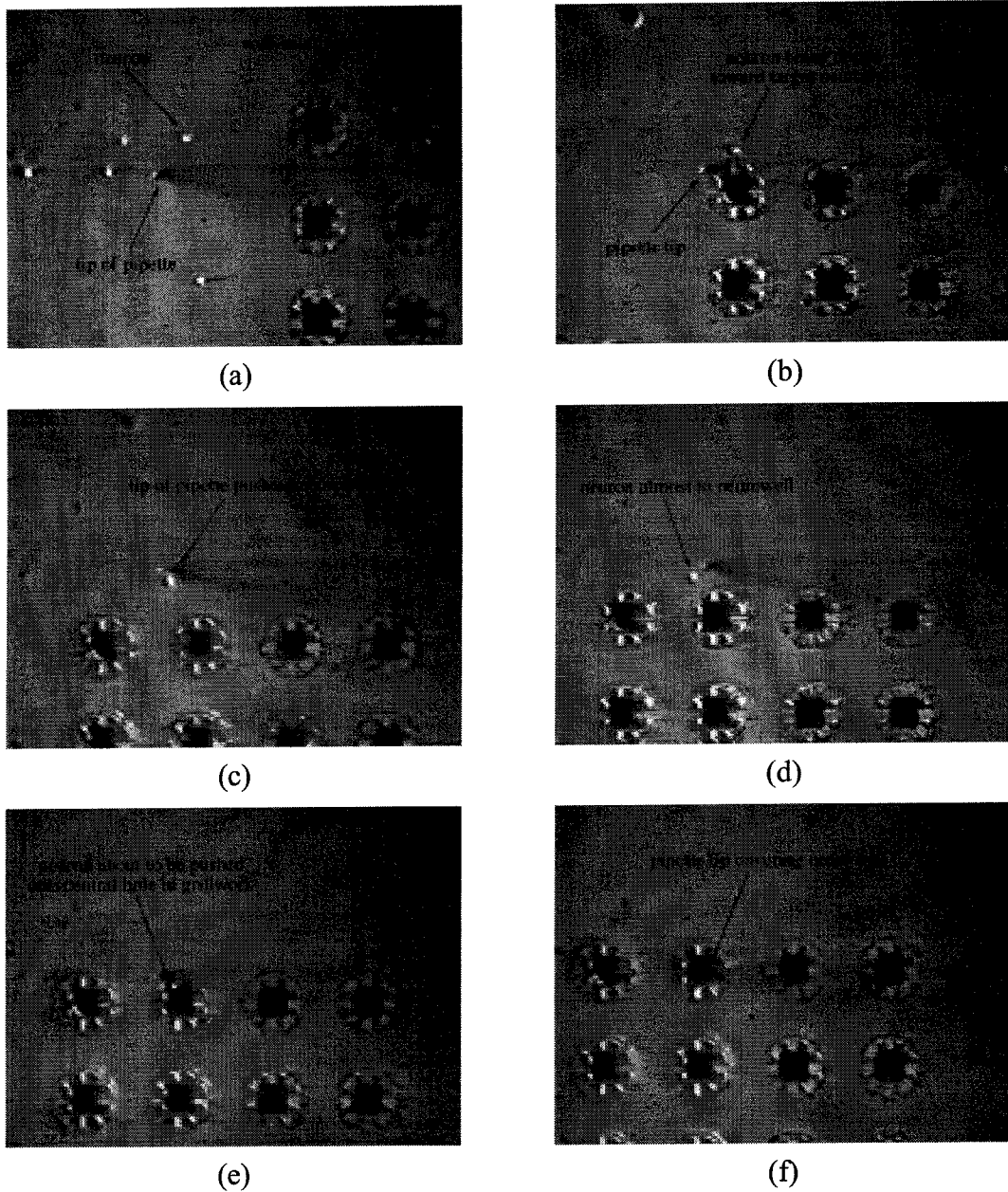
Figure N4-1:  Video screen captures of the implantation of a hippocampal neuron into a canopy neurowell.  (a)  Selection of a neuron and initial position of pipette tip.  (b-d)  Maneuvering of neuron across surface of silicon toward the target neurowell.  (e)  Neuron pushed right to the edge of the central hole of the grillwork.  (f)  Neuron has been pushed into neurowell and the tip of the pipette covers the central hole of the grillwork to allow it to fall to the floor of the microcavity undisturbed.

# THE DETAILED FABRICATION PROCESS FOR NEUROCHIPS AND NEUROPROBES CONTAINING PROTOTYPE NEUROWELLS

The fabrication process for the prototype neurochips and neuroprobes requires eight masks. In producing neuroprobes, a number of steps additional to those required to create the neurochip are added just prior to wafer dicing. Additionally, both dimple and flat-bottomed wells are created with the dimple wells required extra processing. In the following detailed process, the steps labeled as optional cover those supplementary steps that are needed to form the neuroprobes and the dimples.

To minimize the length of the detailed fabrication process, commonly used sequential steps are named. The first time a sequence, such as photoresist coating, is presented, it is named in bold face. Following this "header," the steps are indented and fully described and itemized. All subsequent references to the sequence are made using just the bold face name. This recognizes that slight, non-material modifications might be

required in a given circumstance for optimal performance. Only when such changes are

critical to the process will they be specified.

The base wafers used in this process are <100> epi-wafers (see appendix N1).

The buried layer is heavily-doped boron (with an optional 2% germanium added for

stress reduction and "linen pattern elimination) that is 4 microns thick. The wafers do not

have to be double side polished.

1) **Piranha clean**
    a) Piranha clean (80% $H_2SO_4$, 20% $H_2O_2$, 120 °C) for 15 min.
    b) Rinse in water until the resistivity of the DI water is > 10 MΩ-cm.
    c) Spin dry.
2) **Form rough front-to-back alignment marks**
    a) **Coat with AZ1350J** photoresist on front side of wafer
        i) Prime wafer with HMDS vapor
        ii) Spin AZ1350J at 3000 RPM
        iii) **Soft bake photoresist**
            (1) Oven environment
            (2) 100 °C for 30 min.
        iv) Final thickness ≈ 1 micron
    b) Cool the wafer and **coat with AZ1350J** photoresist on backside of wafer
    c) Do double-side contact printing with front and back alignment mark fixture.
        i) **UV canon expose**
            (1) 6 sec exposure (dose ≈ 50 mJ/cm$^2$) (manual shutter)
            (2) Optimum setting found using a test wafer
    d) **Hard bake photoresist**
        i) Oven environment
        ii) 120 °C for 30 min.
    e) **Etch rough double-side alignment marks** on the front side of wafer
        i) Transfer photoresist image into silicon 0.5 to 1.0 microns deep
        ii) **Silicon plasma etch**
            (1) $SF_6$ and $O_2$ plasma in PE IIA
            (2) From base pressure of ≈ 50 mtorr:
                (a) Set pressure to 250 mtorr with $SF_6$ flow
                (b) Increase to 300 mtorr with $O_2$ flow
            (3) Strike plasma at 300W
            (4) Etch rate ≈ 3000Å/min

f) **Etch rough double-side alignment marks** on the backside of wafer

3) **Strip photoresist** from the wafer

   a) Strip bulk of resist with acetone rinsed with isopropanol and DI water

   b) **Oxygen plasma descum** on both sides of wafer

      i) $O_2$ plasma in PE IIA

      ii) From base pressure of $\approx$ 50 mtorr set pressure to 300 mtorr with $O_2$ flow

      iii) Strike plasma at 300W

      iv) Etch for 2 min typically removes any photoresist residue

4) **Form the oxide dimples** at the bottom of the neuron wells (OPTIONAL STEP)

   a) **Piranha clean**

   b) Grow 500Å dry thermal oxide at 1000 °C

   c) **Deposit LPCVD nitride** 2000Å

      i) **Piranha clean** (Note: In this case, the wafers are taken directly from the oxidation tube and placed in the nitride furnace. This piranha clean step is included here as part of the general definition of LPCVD nitride depositions.)

      ii) 800 °C

      iii) 40 sccm DCS

      iv) 120 sccm $NH_3$

      v) Deposition rate $\approx$ 1 μm/hr

   d) **Coat with AZ1350J** on front side of wafer

   e) **Expose and develop photoresist** with Nitride Dots mask

      i) Expose with GCA stepper

         (1) Exposure time determined by strength of UV lamp and resist thickness

         (2) Optimum exposure typically set with a test wafer

         (3) Typical exposure times with Caltech stepper are:

            (a) 1 micron   =>   0.2 sec

            (b) 4 microns   =>   0.5 sec

            (c) 6 microns   =>   0.7 sec

            (d) 10 microns=>   2.0 sec

      ii) Develop with 100% AZ Developer

         (1) $\leq$ 4 microns   =>   2 min

         (2) $\geq$ 4 microns   =>   typically 2 to 5 min

         (3) These developing times are "targets" that are "met" with the appropriate exposure time

      iii) **Oxygen plasma descum**

   f) **Hard bake photoresist**

   g) **Oxygen plasma descum**

   h) **Plasma etch nitride**

      i) $SF_6$ and $O_2$ plasma in PE IIA

      ii) From base pressure of $\approx$ 50 mtorr:

         (1) Set pressure to 250 mtorr with $SF_6$ flow

         (2) Increase to 300 mtorr with $O_2$ flow

      iii) Strike plasma at 300W

      iv) Etch rate $\approx 2000\text{Å}/\text{min}$

i) Strip exposed pad oxide (see line (a) of this step) with 40 sec BHF etch

j) **Strip photoresist** from the wafer

k) **Wet etch silicon** down 0.4 microns

      i) Isotropic wet etching with $HNO_3:H_2O:HF = 50:20:1$

      ii) Etch rate $\approx 1000\text{Å}/\text{min}$

l) **Grow wet thermal oxide** approximately 0.8 microns thick

      i) **Piranha clean**

      ii) Temperature = 1050 °C

      iii) $H_2O$ rate of 15 drops/min

      iv) Growth rate $\approx 3$ hours/micron (non-linear)

m) Selectively strip nitride from both sides of the wafer with $H_3PO_4$ at 150 °C (requires 8 to 10 hours depending on number of wafers in batch)

n) Strip the now-exposed pad oxide dots with a 40 sec BHF etch

5) Deposit and lift-off pattern the metal for the electrodes, the interconnect traces, and the bond pads

  a) **Coat with AZ1350J** on front side of wafer

  b) **Expose and develop photoresist** with Metal Liftoff Pattern mask

  c) Thermal evaporate metal => Cr/Au/Cr $100\text{Å}/2000\text{Å}/100\text{Å}$

  d) Pattern using lift-off by sonicating in acetone then rinsing in isopropanol followed by DI water ($\approx 5$ min)

  e) **Oxygen plasma descum**

6) **Deposit and pattern insulator over the metal traces**

  a) **Deposit low temperature oxide (LTO)** to a thickness of 0.5 microns

      i) **Piranha clean** (Note: In this case, the presence of metal on the wafers does not allow them to be piranha cleaned. This piranha clean step is included here as part of the general definition of LTO depositions.)

      ii) 450 °C

      iii) 42.4 sccm $SiH_4$

      iv) 62.1 sccm $O_2$

      v) Deposition rate $\approx 0.5$ μm/hr

  b) **Deposit PECVD nitride** to a thickness of 1.5 microns

      i) $SF_6$ and $NH_2$ plasma in PD900

      ii) 300 °C

      iii) 9.1 sccm $SiH_4$

      iv) 25.9 sccm $NH_3$

      v) Strike plasma at 50W

      vi) Deposition rate $\approx 0.5$ μm/hr

  c) **Pattern the insulation**

      i) **Coat with AZ1350J** on front side of wafer

      ii) **Expose and develop photoresist** with Bond Pads mask and Alignment Marks mask

      iii) **Plasma etch nitride** through to the underlying LTO

iv) Wet etch LTO with BHF

v) Repeat (iv) (and (iii) if necessary) until etch completion is verified by:

(1) Viewing under microscope

(2) Electrical testing with probe station

7) **Form Main Backside Cavity and Large Membrane**

a) **Coat with AZ1350J** on backside of wafer

b) **Expose and develop photoresist** using stepper aperture opened to 9 mm x 3 mm

c) **Hard bake photoresist**

d) **Plasma etch nitride** through to the underlying LTO

e) Wet etch LTO thermal oxide with BHF until surface is hydrophobic

f) **Strip photoresist** from the wafer

g) Anisotropic etch using heavily-doped boron (or B-Ge) epi-layer as etch-stop

i) **Anisotropic EDP etch**

(1) Heat ethylenediamene-pyrochatecol (EDP) to 100 °C in reflux beaker

(2) BHF dip wafers to remove any native oxide

(3) Fully submerse wafers in heated solution with constant stirring with teflon-coated magnetic stir bar

(4) Silicon anisotropic etch rate approximately 45 Å/hr

(5) Immediately upon removal dip wafer in warm solution of KOH to remove remnants of EDP

ii) Takes ≈ 11 hours to form cavities through 500-micron thick wafer

iii) End of etching determined by visually

(1) During etch, etched silicon surface is very rough

(2) When heavily-doped boron (or B-Ge) etch-stop layer is reached surface becomes mirror smooth

iv) Rinse wafer with DI water and spin dry

8) **Remove etch-stop layer** from alignment dies

a) **Selective boron-doped silicon wet isotropic etch**

i) $CH_3COOH:HNO_3:H_2O$ ratio of 8:3:1  (Note: $CH_3COOH$ = acetic acid)

ii) Etches boron-doped silicon only

(1) Doped silicon surface turns black during etch

(2) Becomes mirror smooth when lightly doped silicon layer beneath is exposed

iii) Etch rate ≈ 1 μm/min

b) Rinse wafer with DI water and spin dry

9) Pattern the grillwork for the neurowells

a) **Coat with AZ1350J** on cavity side of wafer using special non-vacuum chuck (see appendix N2)

b) **Expose and pattern photoresist** with Grillwork Plasma Etch mask

c) **Hard bake photoresist**

d) Hand paint edges of cavity and corners at the membrane-to-wall interface with AZ1350J photoresist using a very fine sable or camel hair brush (Note: animal

hair brush is necessary as synthetic fibers are dissolved in photoresist and/or acetone)

   e) **Hard bake photoresist**
   f) **RIE etch silicon** down 4.5 microns
      i)  $SF_6$ and $O_2$ plasma in RIE
      ii) From base pressure of $\approx$ 1 mtorr:
         (0) Set $SF_6$ flow to 17 sccm
         (0) Set $O_2$ flow to 15 sccm
         (0) Resulting operating pressure is $\approx$ 300 mtorr
      iii) Strike plasma at 600W
      iv) Etch rate $\approx$ 2000Å/min

10) **Anisotropically etch microcavities of neurowells**
   a) **Anisotropic EDP etch**
   b) Using a microscope, look through large central hole in grillwork - seeing that electrodes have been exposed as the floor of the neurowells confirms that microcavity formation is complete

11) **Etch chrome** ($\approx$ 100 Å) from electrodes at bottom of neurowells to expose pure gold
   a) Use commercial chrome etchant at room temperature
   b) Etch rate approximately 200 Å/min
   c) Dip in 2 % sulfuric acid to neutralize chrome etchant
   d) Rinse wafer with DI water and spin dry

12) **Define the shape of the probe** (OPTIONAL STEP - not used for neurochips)
   a) Thermal evaporate 2000 Å aluminum onto front side of wafer
   b) **Coat with AZ1350J** on front side of wafer
   c) **Expose and develop photoresist** with Probe Shape mask
   d) **Hard bake photoresist**
   e) Etch exposed aluminum with commercial aluminum etchant
   f) **Pattern the insulation**
   g) **RIE etch silicon** until the membrane is patterned all the way through
   h) **Strip photoresist from the wafer** (Note: Photoresist most likely stripped by RIE plasma which is why aluminum is deposited as an RIE masking material)
   i) Strip aluminum from the wafer with commercial aluminum etchant
   j) Dip in EDP for 2 min to smoothen the edges

13) **Dice/Separate devices from wafer**
   a) In case of probes, the EDP etch of the main cavities also patterns the handles of the probes in such a way that the devices can be snapped out of the wafer - no dicing is required
   b) For neurochips, dice wafer into 12.7 mm dies
      i)  **Coat with AZ1350J** over the front side of the wafer
      ii) Attach wafer, cavity side down, to dicing tape
      iii) Dice wafer

14) Process complete

# THE DETAILED FABRICATION PROCESS FOR NEUROCHIPS AND NEUROPROBES CONTAINING PROTOTYPE VARIATION NEUROWELLS

The fabrication process for neurochips and neuroprobes containing prototype variation neurowells is very similar to the process for those with prototype neurowells (see appendix N5). Presented in this appendix is the process flow used to produce such devices. All prototype variation neurowells that have been fabricated are flat bottomed. Dimple bottomed wells can be created in a manner similar to that presented in appendix N5. They were included only in the prototype wells because, as noted in the chapters covering the neural interfaces, the neurons tend to pull themselves off the floor, up to the grillwork. This position negates the sealing benefits for which the dimpling is introduced.

As in the previous appendix, those sequences of steps repeatedly used throughout the fabrication are lumped under a single heading that is given in bold face. This helps to minimize the length and apparent complexity of the process presented. The step

sequences already defined in the previous appendices are used without definition in this appendix. New sequences are named with a bold face header and the corresponding steps are indented and fully described and itemized. All subsequent references to the sequence are made using just the bold face name. This recognizes that slight, non-material modifications might be required in a given circumstance for optimal performance. Only when such changes are critical to the process will they be specified.

The base wafers used in this process are <100> epi-wafers (see appendix N1). The buried layer is heavily-doped boron (with an optional 2% germanium added for stress reduction and "linen pattern elimination) that is 4 microns thick. The wafers do not have to be double side polished.

1) **Piranha Clean**
2) **Form rough front-to-back alignment marks**
3) **Strip photoresist** from the wafer
4) **Grow wet thermal oxide** approximately 1 micron thick
5) Pattern thermal oxide
   a) **Coat with AZ1350J** on front side of wafer
   b) **Expose and develop photoresist** with Bond Pad Oxide mask (NOTE: This is needed to minimize capacitance to the silicon substrate. If only the following 2000 Å of nitride were used, the signals from the electrodes in the neurowells would be shunted to ground and would never be seen by the external electronics.)
6) **Deposit LPCVD nitride** 2000Å thick
7) **Form Main Backside Cavity and Large Membrane**
8) **Remove etch-stop layer** from all dies
9) **Deposit LPCVD nitride** or **grow wet thermal oxide** 1 micron thick as grillwork material
10) **Pattern prototype variation grillwork** for the neurowells in alignment dies only
   a) **Coat with AZ1350J** on cavity side of wafer using special non-vacuum chuck (see appendix N2)
   b) Hand paint edges of cavity and corners at the membrane-to-wall interface with AZ1350J photoresist using a very fine sable or camel hair brush (Note: animal

hair brush is necessary as synthetic fibers are dissolved in photoresist and/or acetone)

   c) **Expose and pattern photoresist** with Grillwork Etch mask

   d) **Hard bake photoresist**

   e) Etch grillwork material

      i) Case of nitride grillwork material

         (1) **Plasma etch nitride**

         (2) Overetch into silicon must be minimized

      ii) Case of wet oxide grillwork material

         (1) Wet etch oxide with BHF

         (2) Etch stops at oxide-to-silicon interface but sideways etch is hard to control

   f) **Strip photoresist** from the wafer

11) **Anisotropically etch microcavities of neurowells** (Note: Since only the grillwork in the alignment dies has been patterned, neurowells form only in those dies. The etch is through to front side and forms transparent nitride membrane. For subsequent processing on front side of wafer, these membranes act as very accurate front-to-back alignment marks.)

12) **Coat with AZ1350J** on front side of wafer

   a) **Expose and develop photoresist** with Nitride Dots mask

   b) **Hard bake photoresist**

   c) **Plasma etch nitride** (time etch to minimize penetration into underlying silicon)

   d) **Strip photoresist** from the wafer

13) **Deposit and etch-pattern the metal for the electrodes, the interconnect traces, and the bond pads**

   a) Thermal evaporate metal => Cr/Au/Cr 100Å/2000Å/100Å on front side of wafer

   b) **Coat with AZ1350J** on front side of wafer

   c) **Expose and develop photoresist** with Metal Etch Pattern mask

   d) Pattern with commercially available gold and chrome wet etchants

   e) **Strip photoresist** from the wafer

   f) **Oxygen plasma descum**

14) **Deposit and pattern insulator over the metal traces** (OPTIONAL STEP required only for neuroprobes)

15) **Pattern prototype variation grillwork** for the neurowells in all dies

16) **Anisotropically etch microcavities of neurowells**

17) **Etch chrome** ($\approx$ 100 Å) from electrodes at bottom of neurowells to expose pure gold

18) **Define the shape of the probe** (OPTIONAL STEP - not used for neurochips)

19) **Dice/Separate devices from wafer**

20) Process complete

# THE DETAILED FABRICATION PROCESS FOR NEUROCHIPS AND NEUROPROBES CONTAINING ZERO OVERHANG NEUROWELLS

The fabrication process for neurochips and neuroprobes containing zero overhang neurowells is very similar to the process for those with prototype variation neurowells (see appendix N6). Presented in this appendix is the process flow used to produce such devices. As in the previous appendix, bold-faced names are used to indicate repeatedly used sequences of steps. This helps to minimize the length and apparent complexity of the process presented. The step sequences already defined in the previous appendices are used without definition in this appendix. New sequences are named with a bold face header and the corresponding steps are indented and fully described and itemized. All subsequent references to the sequence are made using just the bold face name. This recognizes that slight, non-material modifications might be required in a given circumstance for optimal performance. Only when such changes are critical to the process will they be specified.

The base wafers used in this process are <100> epi-wafers (see appendix N1).

The buried layer is heavily-doped boron (the more expensive B-Ge wafers are not used in this process since this epi-layer is stripped after the formation of the membrane) that is 4 microns thick. The wafers do not have to be double side polished.

1) **Piranha Clean**
2) **Form rough front-to-back alignment marks**
3) **Strip photoresist** from the wafer
4) **Grow wet thermal oxide** approximately 1 micron thick
5) Pattern thermal oxide
   a) **Coat with AZ1350J** on front side of wafer
   b) **Expose and develop photoresist** with Bond Pad Oxide mask (NOTE: This is needed to minimize capacitance to the silicon substrate. If only the following 2000 Å of nitride were used, the signals from the electrodes in the neurowells would be shunted to ground and would never be seen by the external electronics.)
   c) **Piranha clean**
6) **Deposit LPCVD nitride** 2000Å thick
7) **Form Main Backside Cavity and Large Membrane**
8) **Remove etch-stop layer** from all dies
9) **Deposit LPCVD nitride** 1 micron thick as grillwork material
10) Pattern the grillwork for the neurowells
   a) **Coat with AZ1350J** on cavity side of wafer using special non-vacuum chuck (see appendix N2)
   b) Hand paint edges of cavity and corners at the membrane-to-wall interface with AZ1350J photoresist using a very fine sable or camel hair brush (Note: animal hair brush is necessary as synthetic fibers are dissolved in photoresist and/or acetone)
   c) **Expose and pattern photoresist** with Grillwork Etch mask
   d) **Hard bake photoresist**
   e) Etch grillwork material
      i) **Plasma etch nitride**
      ii) Slight (< 2 microns) overetch into silicon is acceptable
      iii) Note: This process removes all field nitride leaving behind only that material used for the grillwork bars.
   f) **Strip photoresist** from the wafer
11) **Grow wet thermal oxide** approximately 1 micron thick from the silicon surrounding the grillwork nitride
12) **Pattern oxide in central hole of grillwork** of alignment dies only
   a) **Coat with AZ1350J** on cavity side of wafer
   b) **Expose and develop photoresist** with Neurowell Anisotropic Etch Access Pattern mask

    c) **Hard bake photoresist**
    d) Etch exposed oxide with BHF
    e) **Strip photoresist** from the wafer

13) **Anisotropically etch microcavities of neurowells** in alignment dies only (Note: This forms the accurate front-to-back alignment marks)

14) **Coat with AZ1350J** on front side of wafer
    a) **Expose and develop photoresist** with Nitride Dots mask
    b) **Hard bake photoresist**
    c) **Plasma etch nitride** (time etch to minimize penetration into underlying silicon)
    d) **Strip photoresist** from the wafer

15) **Deposit and etch-pattern the metal for the electrodes, the interconnect traces, and the bond pads**

16) **Deposit and pattern insulator over the metal traces** (OPTIONAL STEP required only for neuroprobes)

17) **Pattern oxide in central hole of grillwork** of all dies

18) **Form microcavities of neurowells**

19) **Etch chrome** ($\approx 100$ Å) from electrodes at bottom of neurowells to expose pure gold

20) **Define the shape of the probe** (OPTIONAL STEP - not used for neurochips)

21) **Dice/Separate devices from wafer**

22) Process complete

# APPENDIX N8

# THE DETAILED FABRICATION PROCESS FOR NEUROCHIPS AND NEUROPROBES CONTAINING CANOPY NEUROWELLS

The fabrication process for neurochips and neuroprobes containing canopy neurowells is very similar to the process for those with zero overhang neurowells (see appendix N7). Presented in this appendix is the process flow used to produce such devices. As in the previous appendix, bold-faced names are used to indicate repeatedly used sequences of steps. This helps to minimize the length and apparent complexity of the process presented. The step sequences already defined in the previous appendices are used without definition in this appendix. New sequences are named with a bold face header and the corresponding steps are indented and fully described and itemized. All subsequent references to the sequence are made using just the bold face name. This recognizes that slight, non-material modifications might be required in a given circumstance for optimal performance. Only when such changes are critical to the process will they be specified.

The base wafers used in this process are <100> epi-wafers (see appendix N1).

The buried layer is heavily-doped boron (the more expensive B-Ge wafers are not used in this process since this epi-layer is stripped after the formation of the membrane) that is 4 microns thick. The wafers do not have to be double side polished.

1) **Piranha Clean**
2) **Form rough front-to-back alignment marks**
3) **Strip photoresist** from the wafer
4) **Grow wet thermal oxide** approximately 1 micron thick
5) Pattern thermal oxide
   a) **Coat with AZ1350J** on front side of wafer
   b) **Expose and develop photoresist** with Bond Pad Oxide mask (NOTE: This is needed to minimize capacitance to the silicon substrate. If only the following 2000 Å of nitride were used, the signals from the electrodes in the neurowells would be shunted to ground and would never be seen by the external electronics.)
   c) **Piranha clean**
6) **Deposit LPCVD nitride** 2000Å thick
7) **Form Main Backside Cavity and Large Membrane**
8) **Remove etch-stop layer** from all dies
9) **Deposit low temperature oxide (LTO)** to a thickness from 0.2 to 2.0 microns depending on the height desired for the micro-tunnels
10) Pattern LTO to form anchors to the silicon membrane
    a) **Coat with AZ1350J** on cavity side of wafer
    b) **Expose and develop photoresist** with Canopy Anchor Points mask
    c) **Hard bake photoresist**
    d) Etch exposed oxide with BHF
    e) **Strip photoresist** from the wafer
11) **Deposit LPCVD nitride** 1 micron thick as canopy grillwork material
12) Pattern the grillwork for the neurowells
    a) **Coat with AZ1350J** on cavity side of wafer using special non-vacuum chuck (see appendix N2)
    b) Hand paint edges of cavity and corners at the membrane-to-wall interface with AZ1350J photoresist using a very fine sable or camel hair brush (Note: animal hair brush is necessary as synthetic fibers are dissolved in photoresist and/or acetone)
    c) **Expose and pattern photoresist** with Canopy Grillwork Etch mask
    d) **Hard bake photoresist**
    e) Etch grillwork material

    i)  **Plasma etch nitride**

    ii) Underlying LTO acts as etch stop

    iii) Note:  This process removes all field nitride leaving behind only that material used for the canopy grillwork.

  f)  **Strip photoresist** from the wafer

13) **Pattern oxide in central hole of grillwork** of alignment dies only

14) **Anisotropically etch microcavities of neurowells** in alignment dies only (Note: This forms the accurate front-to-back alignment marks)

15) **Coat with AZ1350J** on front side of wafer

  a)  **Expose and develop photoresist** with Nitride Dots mask

  b)  **Hard bake photoresist**

  c)  **Plasma etch nitride** (time etch to minimize penetration into underlying silicon)

  d)  **Strip photoresist** from the wafer

16) **Deposit and etch-pattern the metal for the electrodes, the interconnect traces, and the bond pads**

17) **Deposit and pattern insulator over the metal traces** (OPTIONAL STEP required only for neuroprobes)

18) **Pattern oxide in central hole of grillwork** of all dies

19) **Form microcavities of neurowells**

20) **Etch chrome** ($\approx 100$ Å) from electrodes at bottom of neurowells to expose pure gold

21) Strip LTO from the cavity side of the wafer using 48% HF (Note:  This cleans the LTO from the micro-tunnels as well as from the field.  If insulation has been deposited over the metal on the front side of the wafer, this etching must be confined to the cavity side only as PECVD nitride is etched rather quickly in HF.)

22) **Define the shape of the probe** (OPTIONAL STEP - not used for neurochips)

23) **Dice/Separate devices from wafer**

24) Process complete

# APPENDIX W1

# INTEGRATED SILICON MICROMACHINED WAVEGUIDE CIRCUITS FOR SUBMILLIMETER WAVE APPLICATIONS

## W1.1    Abstract

Rectangular waveguides are commonly used as circuit elements in heterodyne sensor systems at millimeter wavelengths. However, conventional machining techniques for such components operating above a few hundred GHz, are complicated and costly. Previously we reported on the development of silicon micromachining techniques for fabricating silicon-based waveguide circuits which can operate up to high submillimeter

wave frequencies. Continuing this work, we have used (110) silicon wafers as a substrate and fabricated WR-4 (170 - 260 GHz) waveguides. The new capability of placing a nitride membrane that runs the length of the waveguide's central axis has been developed and demonstrated. Submicron SIS tunnel junctions have also been successfully fabricated on nitride membranes which will allow them to be integrated into the waveguide design. This eliminates the traditional mounting problems of thin substrates for high frequencies. Low temperature, selective metallization techniques (electroless nickel) have been developed which coat the silicon waveguide walls but leave the nitride membranes untouched. By avoiding a high temperature metallization process, integration of the temperature sensitive Superconductor-Insulator-Superconductor (SIS) junctions with the waveguide channels is made possible. Insertion loss measurements of WR-4 waveguide sections show performance comparable to conventional metal waveguides.

## W1.2     Introduction

Rectangular waveguides are used in a variety of rf components and circuits. In particular, heterodyne radiometers use waveguide circuits at millimeter wavelengths and even recently at submillimeter wavelengths [176]. Conventional machining techniques for metallic waveguides become time consuming, costly, and difficult for frequencies above a few hundred GHz. Waveguide dimensions are comparable to the wavelength, which is $\lambda = 0.3$ mm at 1000 GHz for example. In addition, mounting small dielectric substrates with devices such as mixer diodes, filters and planar probes in these

waveguides is difficult.

We are developing and adapting silicon micromachining techniques [174, 175] to create waveguide circuits which can operate up to high submillimeter wave frequencies. Silicon micromachined waveguide components have several advantages, as previously discussed [178], including precise tolerance control, atomically smooth walls, rapid turnaround for optimization, and the inclusion of membranes as integrated substrates for planar devices and circuits. Initial efforts have produced straight waveguide sections for
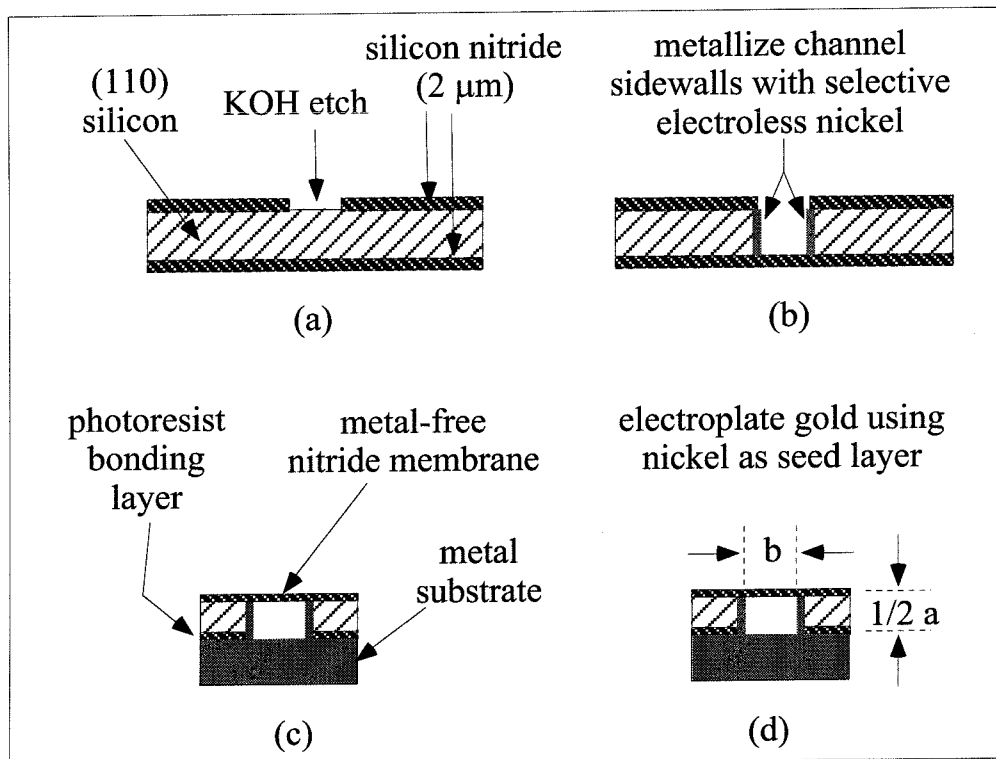
Figure W1-1: A cross section view of the fabrication process. (a) $Si_3N_4$ mask defines the waveguide height. (b) Wafer is etched completely through and the channel sidewalls are metallized (c) Wafer with waveguide channels is bonded to an smooth metal substrate which forms the floor of the half-channel. (d) Completed half-section of waveguide with gold plating. Two of these sections are mated to form the waveguide. "a" is the waveguide width and "b" is the height.

WR-10 band (75-115 GHz) [178]. In this work, the focus has been on higher frequencies (170-260 GHz), improved metallization techniques (electroless nickel), and incorporation of thin ($\approx 2$ $\mu$m) silicon nitride membranes which can support planar devices and circuits.

## W1.3     Fabrication Process

### W1.3.1     Process Overview

The major steps of the fabrication process for the half sections with emphasis on the cross section is shown in figure W1-1. Double-side polished silicon wafers with (110) surface orientation and 0.0215 inches thick are used. A thick ($\approx 2\mu$m) layer of Low Pressure Chemical Vapor Deposited (LPCVD) silicon nitride ($Si_3N_4$) is deposited on both sides of the wafer. Photoresist is used to pattern windows in the $Si_3N_4$ on the backside of the wafer with an $SF_6$ plasma. These windows define b, the waveguide height, shown in figure W1-1.d. The wafer is put in a reflux system and etched in a water based solution of potassium hydroxide (KOH) to form the channel. Figure W1-1.b shows the wafer after it has been etched completely through to form half of the waveguide. Not only does the etch create waveguide half-channels but it also forms the nitride on the front side of the wafer into a membrane as it removes silicon from behind. Metallization is done using a selective nickel plating bath, and a photoresist bonding technique is used to glue the channels to a smooth metal substrate, as shown in figure W1-1.c, to form the third wall of the half-channel. After patterning of the nitride membranes, the wafer is diced into individual waveguide halves 25.4 mm in length as shown in figure W1-1.d. Further

metallization is done to reduce rf conduction losses by electroplating gold to a thickness of $\approx 3$ μm.

## W1.3.2    Channel Formation

As noted above, a water based solution of KOH is used to etch the channels into the silicon wafer. We are using a continuously stirred 40% solution heated to 80°C. As we reported previously [178], the etching rate of (110) silicon by this solution is 2μm/min and the etching ratio of (110):(111) planes is 170:1. It is the large etching ratio that makes this etchant attractive. A (110) wafer has its (111) planes perpendicular to its surface. When etched by KOH, the (111) planes are effectively not etched when
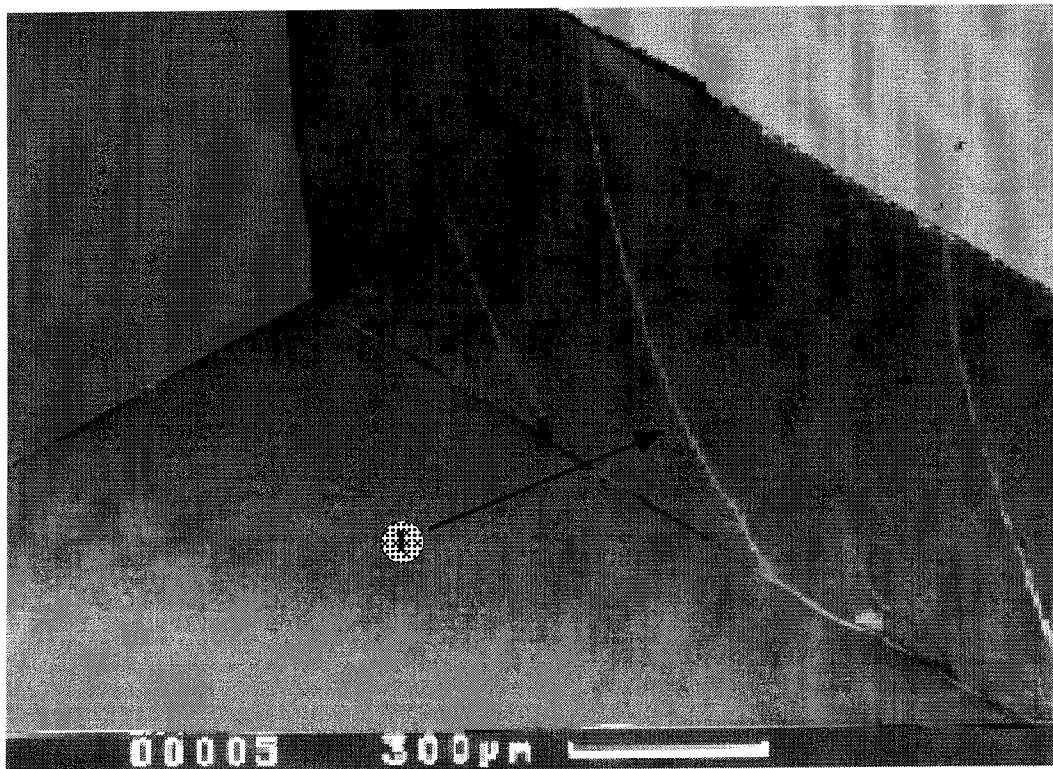


Figure W1-2:  SEM photo of a channel's sidewall. (1) indicates one of the curved steps that were formed during the KOH etching. They are caused by poor alignment to the (111) plane.

compared to the other planes. As a result, channels with vertical sidewalls can be obtained. If alignment to the (111) crystal plane is very accurate ($\approx 0.1°$), the walls of the channels will be atomically smooth. Figure W1-5 shows how smooth the (111) defined sidewalls can be when compared to the planes that are being etched down to form the channel. The figure shows a partially etched channel spanned by a patterned "air bridge." The sidewalls are extremely smooth as compared to the rough bottom which needs to be etched further. (Note the abrupt transition between the rough, wood-like texture of the bottom and the smooth sidewalls.)

Since extremely smooth sidewalls are desired, especially to minimize rf losses at higher frequencies, accurate alignment of the channel masks to the (111) crystal plane is required. The wafers used have their major flats cut along the (111) plane but alignment to this alone is insufficient to assure featureless sidewalls. Wafer specifications state that major flat alignment to the designated plane is only to within $\pm 1°$. We have found that alignment to the (111) plane must be within a $\pm 0.25°$ in order to avoid producing ridges in the sidewalls during etching (see figure W1-2)

Fine alignment to the (111) plane is achieved by KOH etching a fan pattern into the wafer before the channels are defined. The fan pattern consists of an array of lines with each line rotated $0.1°$ with respect to its neighbor. These fans consist of fifty one lines which allows for a correction of $\pm 2.5°$. The KOH etching of the fan pattern is short in comparison to the etch that creates the waveguide channels, being only about 30 minutes. This is sufficient to generate significant undercut in those lines that are poorly

aligned to the (111) crystal while negligible undercut occurs in the well-aligned lines. The pair of lines deemed to have the least amount of undercut is then used as the alignment marks for the exposure with the channel mask.

### W1.3.3    Membranes

Of particular interest is the development of a technique which permits thin membranes of dielectric material (such as silicon nitride) to be fabricated across the
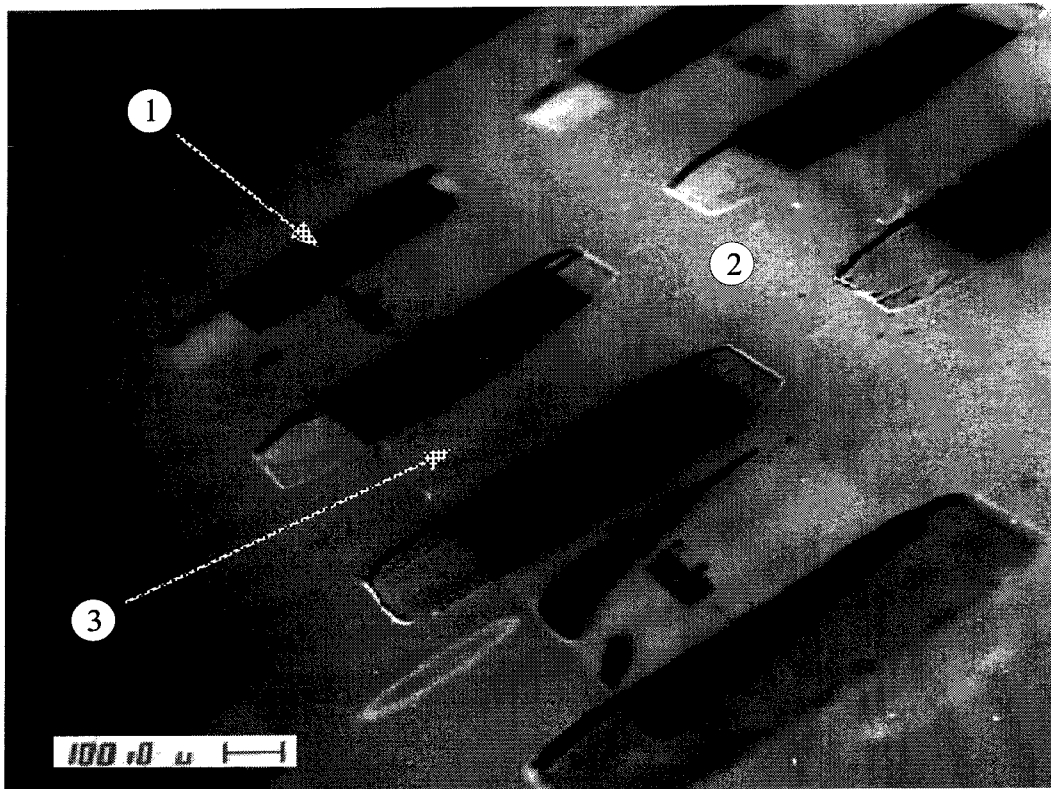


Figure W1-3:  SEM photo of a silicon waveguide channel spanned by three nitride air bridges, 2μm thick.  (1) show the channel, (2) shows the silicon substrate that is the channel's sidewall and (3) shows the one of the nitride air bridges.  The front nitride air bridge has fractured.  Both the front and back nitride air brides are inscribed with a name.  A portion of a second, neighboring channel can be seen in the upper right corner of the photo.

waveguide channels. As noted in the channel fabrication section, this is done by coating

the wafer with a relatively thick layer ($\approx 2$ µm) of nitride and etching away the silicon

from one side of the wafer. This permits the entire channel to be spanned by silicon

nitride and if desired, allows further processing to be performed on the wafer. This

provides for the possibility (but not the requirement) of fabricating SIS junctions and

planar tuning circuits on the membranes after the channels have been created. The

membranes can be patterned into air bridges if desired to limit the amount of dielectric

crossing the channel. Figure W1-3 shows waveguide spanned by three nitride air

bridges. The front and back air bridges have a name inscribed in them. The front bridge

is fractured due to handling but is still mainly intact. Figure W1-4 shows a close-up of a

single air bridge spanning the channel.
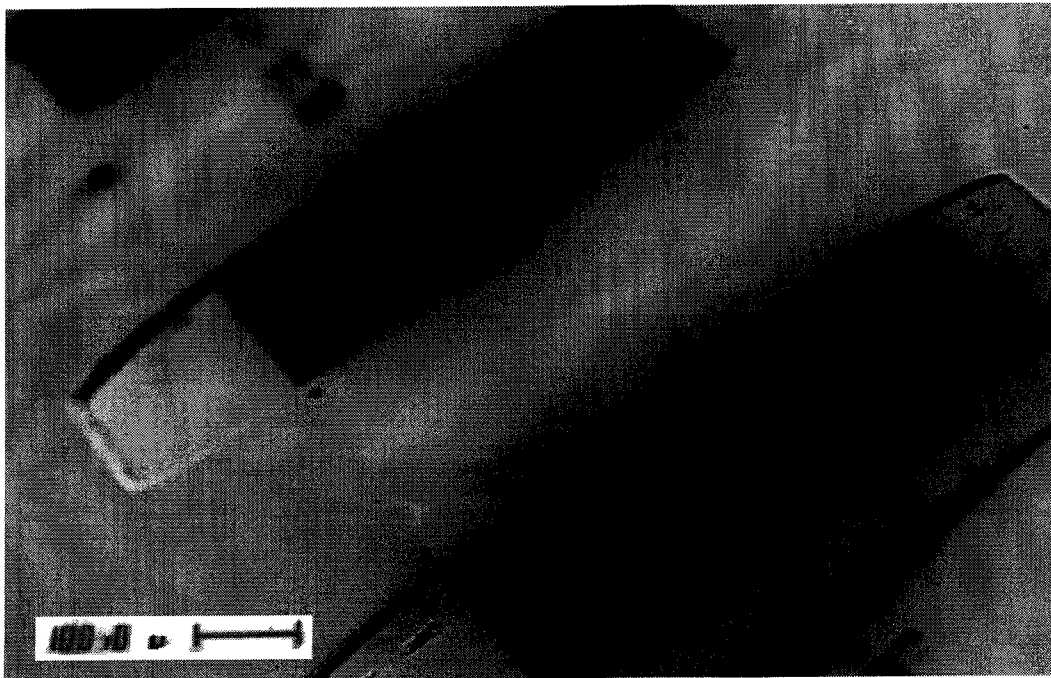


Figure W1-4:  Close-up of the blank air bridge identified in figure W1-3.

A second method for fabricating air bridges has been demonstrated which allows the channels to be etched from the membrane side of the wafer as opposed to the backside as used to produce the 200GHz waveguides. Figure W1-5 shows an air bridge spanning a partially etched channel. The diamonds holes in the nitride are needed to ensure that the silicon beneath the air bridge is removed. An improvement on this process which involves adding a sacrificial oxide layer beneath the nitride should eliminate the need for such holes but it has yet to be demonstrated.
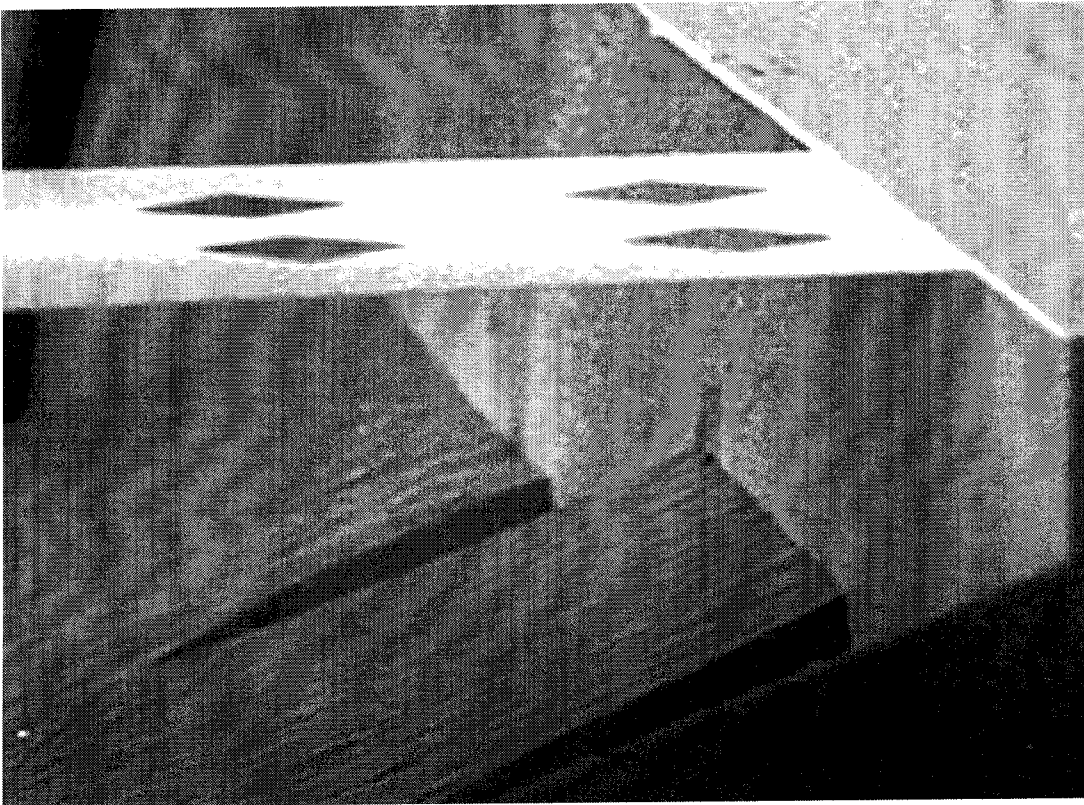


Figure W1-5: SEM photo of a partially etched waveguide spanned by a silicon nitride air bridge. Note the smoothness of the sidewalls as compared to the rough etched floor. The change from rough floor to smooth sidewalls is very abrupt.

## W1.3.4     Metallization

Metallization of silicon waveguides is a crucial step in fabricating components that show comparable insertion losses to conventional waveguides. Because the bulk material from which the channels are produced is a semiconductor and not metal, RF losses are extremely high. In previous work, evaporated metal, deposited at varying angles, was used to coat the walls of the silicon waveguides [178]. Followed by an electroplated gold step, this technique was shown to produce waveguides with good performance. Evaporation, however, cannot be used when nitride air bridges span the channels. Evaporation is not conformal, i.e. it is a directional deposition, and thus areas beneath the air bridges are "shadowed" and will not be metallized. Furthermore, the nitride membranes will themselves be metallized rendering any junctions or tuning circuitry on them useless. A final issue involved with evaporated metal is temperature. During the deposition the temperature of the wafer, and particularly the nitride air bridges, can easily exceed 150°C which will result in the destruction of sensitive devices such as SIS tunnel junctions.

One process we investigated that would have addressed most of these issues is LPCVD tungsten. In this process, tungsten metal selectively deposits on any exposed silicon surface. It is expected that even silicon "hidden" beneath air bridges can be coated. After a thin layer of metal is deposited it can act as a seedlayer for a subsequent electroplated gold layer. Unfortunately, the deposited tungsten layer has an very high intrinsic stress, too high it turns out to permit coating a continuous surface area as great

as the sidewalls of the waveguide channels. Extensive flaking of the tungsten film occurred after the deposition and the final metallization of the channels was spotty at best. If the stress in the film could be reduced, this may be a viable process for future waveguides. One additional constraint that must be observed if this process is used is that SIS junctions must be fabricated after the tungsten deposition since they will be destroyed by the high temperature used in the metallization technique.

The process finally developed that addresses all of the aforementioned issues is a selective, electroless nickel deposition. The plating solution used is an alkaline bath, pH 8 - 10, reported in [177]. This bath was chosen for its many attractive qualities which include selective plating of silicon, high quality, and excellent adherence (see figure W1-6). Because plating occurs in a liquid bath, issues of shadowing due to air bridges are no longer a concern. This process is also SIS junction compatible as the plating temperature is $< 95°C$.
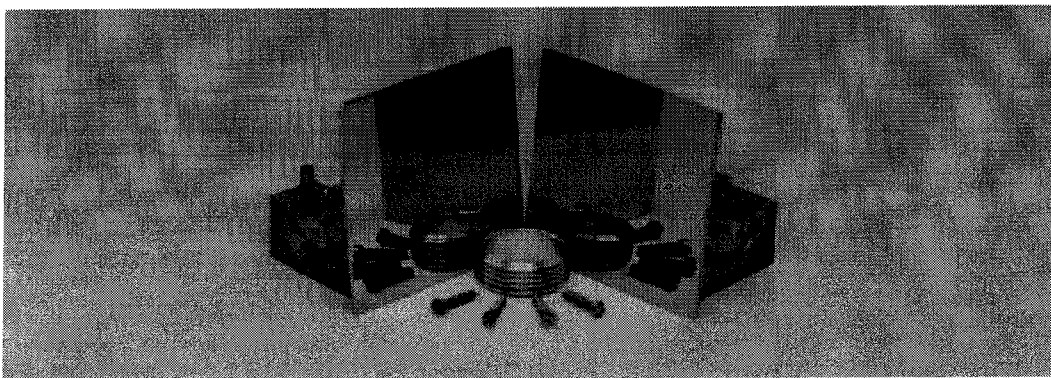


Figure W1-6: The photo shows two square, mirror-like samples positioned to create a reflective corner. The sample on the right is bare, polished silicon and on the left is a similar silicon sample onto which electroless nickel has been plated. The two samples are nearly indistinguishable.

Selectivity in the nickel plating is the main attraction of this process. Nickel is deposited only on those surfaces that are non-insulating. Thus for the waveguide components, only the silicon sidewalls will be plated by the bath. Nitride, however, being an insulator will remain metal free. This permits the nitride air bridges to be left unprotected during the metallization. Simultaneously, the silicon beneath such structures will be plated guaranteeing that there will be continuous metallization down the length of the channel.

It should be noted that the plated nickel will not be the final metal lining the channels. The layer deposited, while not necessarily thin, is kept thin for this process. As an RF conduction material, this nickel is relatively poor. It can, however, perform more than adequately as a seed layer upon which high quality gold or copper can be electroplated. Measurements indicate that 25.4 mm long channels metallized by nickel alone have an insertion loss on the order of -10dB. Once covered by electroplated gold, the losses become comparable to commercial waveguides as described in the following section. For gold electroplating we used AU125 by Selrex [173] which is an acidic bath that is heated to 60°C and continuously stirred.

## W1.3.5    Wafer Bonding

Due to the relatively large dimensions of the 200 GHz channels and size limitations of the silicon processing equipment, it is not possible to fabricate the half channels in a single silicon wafer. The present process relies on the wafer into which the

channels are etched to be as thick as the half-width, a/2, of the target waveguide. This means that once fabricated, the channels must be bonded to a substrate which forms the third wall, or bottom of the channel. The method of bonding is relatively unimportant as long as: 1) it is strong enough to withstand the processes which follow it, 2) the thickness of any adhesive layer used is negligible compared to the waveguide dimensions and 3) after bonding, gold can be plated onto the "third wall." Preferably the gold plate can electrically connect the bottom to the sidewalls.

We chose to use photoresist to bond the channels to the substrate. The main reason being ease of use. Since photoresist is a part of almost every major step in silicon processing, it is a well characterized, easily deposited material. Its bonding strength is adequate for our needs and it can withstand both dicing and gold electroplating steps. Of particular importance is the fact that it can be deposited in a very thin layer (1 to 2 $\mu$m) and it can be selectively removed after exposure to UV light.

Bonding with the photoresist is a very straightforward process. We first choose the substrate. The main requirement is that it is conductive. A silicon wafer coated with a layer of evaporated gold is used. A thin layer of positive photoresist (AZ1350J @ 3500RPM) is then spun onto the wafer. Immediately following the spinning step, the wafer into which channels have been etched and metallized is placed onto the photoresist coated wafer, membrane side up. The two bonded wafers are then soft baked at 100°C for half an hour. Following the bake, the two wafers are globally exposed with UV light and developed. This removes the photoresist from the bottom of the channels while

leaving the resist involved in the actual bonding intact. The end result is two wafers bonded together to form half channels. The distance between the sidewalls and the bottom is $\approx 2\mu m$ which should be easily covered by a $3\mu m$ thick gold plate, the final step in the waveguide fabrication process.

Photoresist is, of course, not the only option for the bonding step. Previously we have used polyimide as the bonding material which, in this process, is simply a more rugged form of photoresist [178]. Other bonding options include anodic bonding, metal-to-metal pressure bonding and common glue or epoxy bonding. There are benefits and drawbacks associated with each of these depending on the specific application for the waveguide component. Photoresist, however, is preferable for rapid turnaround development work. As a final note, for waveguides with target frequencies of 350 GHz and higher, wafer bonding will no longer be necessary. Instead, silicon-on-insulator (SOI) wafers can be used which are essentially two wafers bonded together with a layer of oxide between them.

## W1.4    Experimental Results

In order to perform insertion loss measurements, a pair of brass mounting blocks was designed and fabricated as shown in figures W1-7 and W1-8. The two waveguide half-sections are put in the brass mounting blocks and mated together. This allows the silicon waveguide to be connected to microwave test equipment using conventional waveguide round mini-flanges for WR-4 band. The silicon waveguides are rugged and

can be firmly clamped to metallic flanges. The insertion loss of the WR-4 waveguide was

measured over a frequency range of 200 GHz to 255 GHz in ≈ 10 GHz steps using a

backward wave oscillator as a swept-frequency source and a direct detector. For each

frequency a reference measurement was first taken without a waveguide section present,

and then measurements with the commercial and silicon waveguides were made.

These steps were repeated several times to reduce any variation from the

frequency source itself. The insertion loss measurements for a one inch long section of

waveguide is shown in figure W1-9. The measured loss is about -0.80 dB across the
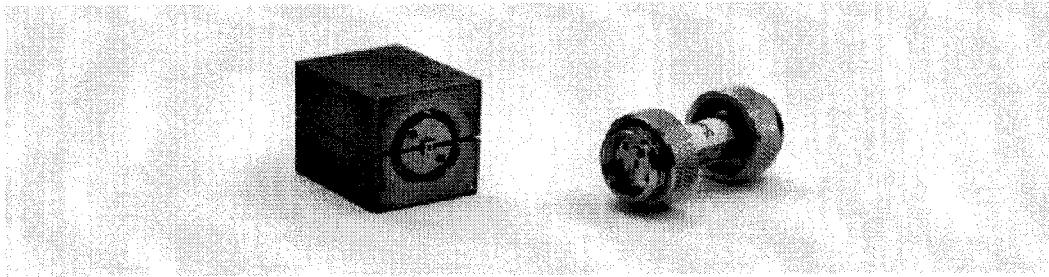


Figure W1-7: On the right is a 25.4 mm, commercial WR-4 waveguide section. On the left is our silicon micromachined WR-4 waveguide section. Two fabricated silicon half-channels are assembled in the mounting block to form a functional waveguide.
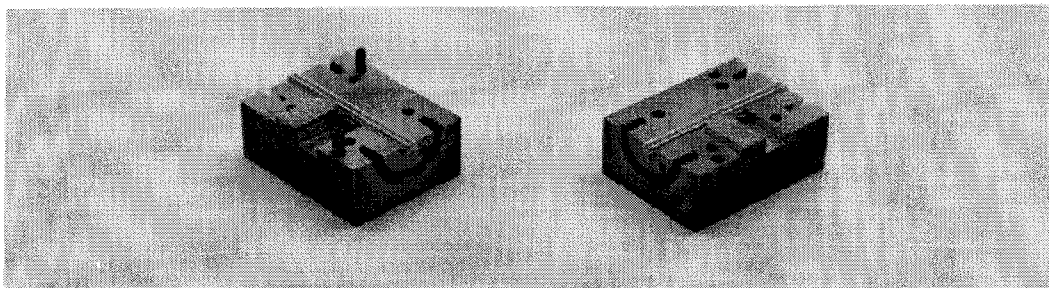


Figure W1-8: The photo shows our waveguide mounting block split into its two halves. A waveguide half-channel is mounted in each of the two mounting block pieces.

band for both the commercial and silicon waveguides. Assuming bulk copper as the wall material, calculations predicts a loss of ≈ -0.30 dB. The difference between theory and experiment is most probably due to differences in the quality of the gold plated surfaces and bulk copper. Calculations show that the metal coating the channels of both the commercial and silicon waveguides has ≈ 1/12 the conductivity of bulk copper which is reasonable for electroplated gold. A comparison between the two types of waveguides shows that the relative losses are < |0.25| dB. The data shows that the commercial channel performs better for the lower frequencies while the silicon guide performs better
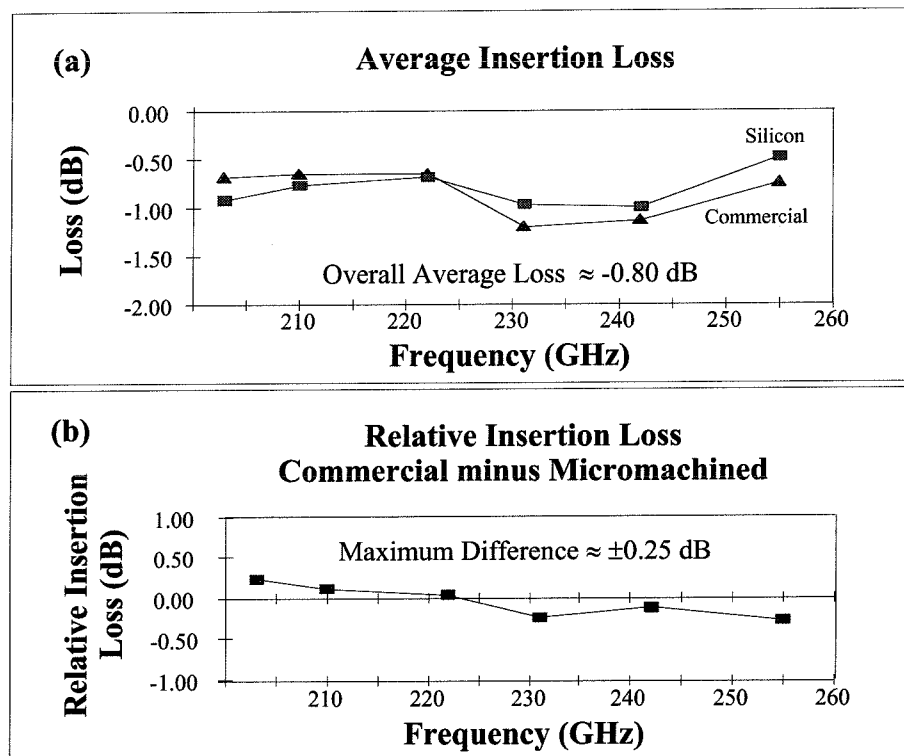


Figure W1-9: (a) Measured loss of a 25.4 mm long section of a silicon and a commercial WR-4 waveguide. The surface of the silicon was electroplated with gold to reduce rf losses. (b) Relative loss comparison between silicon and commercial waveguides showing maximum deviation between the two as < ±-0.25 dB.

at the higher frequencies. We believe that this apparent trend is an artifact of the measurement since the differences are within the experimental error, rather than it reflecting actual changes in performance. Regardless, these results show that there is little discernible difference in the performance of the two types of waveguides.


## W1.5     Summary

We have improved upon a new approach in fabricating waveguide circuits using silicon micromachining technology. In particular, we have fabricated a 200 GHz silicon rectangular waveguide spanned by $\approx 2\mu m$ thick silicon nitride air bridges. A new technique for metallizing the waveguide channels using an electroless nickel plating bath has been introduced to the fabrication process which produces a high quality, selectively deposited film. The plated nickel acts as a seed layer for a subsequent layer of electroplated gold. The measured insertion losses of the fabricated devices are found to be $\approx$ -0.80 dB which is comparable to losses incurred in commercially available, conventional waveguides. The present fabrication process is fully compatible with the integration of SIS junctions and planar RF tuning circuits with the devices.

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