UTILIZATION OF SILICIDES FOR VLSI -

CONTACTS WITH ALUMINUM AND THERMAL OXIDATION

Thesis by

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In Partial Fulfillment of the Requirements

for the Degree of

Doctor of Philosophy

California Institute of Technology

Pasadena, California 91125

1984

(Submitted January 26, 1984)

ACKNOWLEDGMENTS

It is my great pleasure to express my sincere appreciation and thanks to my advisor, Professor Marc-A. Nicolet, for his encouragement and guidance throughout the period of this research. His scientific advice, support and patience have "launched" me into this area of research. By introducing me into the scientific community at large, he enabled me to conduct meaningful work in the fast-paced field of microelectronic technology.

I am especially grateful to Professor S. S. Lau from the University of California at San Diego, for many stimulating discussions. Thanks are due to Ilkka Suni for his collaboration and insight into semiconductor processing technology.

I would like to thank Rob Gorris, Rouel Fernandez, and Ali Ghaffari for assistance with the experimental apparatus, and Michell Parks for excellent typing of all the manuscripts, including this one, and for her skillful proofreading.

Visiting Research Fellows, Dr. Leszek Wieluński, Dr. Adam Barcz, Dr. Martti Mäenpää, and Manuela Finetti; and fellow students, C.-D. Lien, Tom Banwell, K.T. "Bruce" Ho, and Sung Joon Kim, who helped to establish the creative environment that is so important in a research group, deserve grateful acknowledgment.

Special thanks go to Mr. Arnold Applebaum, President of Solid-State Devices, Inc., whose financial support and response to technical and equipment requirements have made this work possible.

Finally, the support of my wife, Rachel, so highly appreciated, is thankfully acknowledged.

PREFACE

Most of the scientific work performed at CALTECH to fulfill the requirements of my thesis is already published (or accepted for publication) in journals. To make this thesis a comprehensive presentation of my work, a separate list (Reference II) is included, which references only my own publications that are relevant to this thesis. These publications constitute an integral part of the thesis. Due to the requirements of the University Microfilms International, these publications cannot be reproduced since the reduced letter size of a reprint is unacceptable for microfilm reproduction. The papers are published in the following journals: THIN SOLID FILMS, JOURNAL OF VACUUM SCIENCE & TECHNOLOGY, APPLIED PHYSICS LETTERS, JOURNAL OF APPLIED PHYSICS, APPLIED PHYSICS A, JOURNAL OF ELECTROCHEMICAL SOCIETY, JOURNAL OF ELECTRONIC MATERIALS, and IEEE ELECTRON DEVICES LETTERS, and are available to the scientific community. For the convenience of the thesis examination committee, a set of reprints of all my relevant papers has been attached to this thesis. One manuscript that has been accepted for publication and is in press, but not available as reprint yet, is included as an Appendix.

ABSTRACT

The potential role of silicides in VLSI (very large scale integration) Si technology is described. A survey of trends and requirements exposes two difficult technological issues as the device dimensions shrink: contacts to the individual devices and interconnections between devices or functional blocks on the Si chip. For both, silicides play an important role.

The contact between the Si that contains the device and the top Al layer (Al is the preferred metal for metallization) has to be thermally stable, reproducible, reliable, and have low contact resistivity. After a brief survey of the available diffusion barriers designed to suppress the Al interaction with Si, I concentrate on the sacrificial barrier structure. The generalized layered structure approach, utilizing Si/silicide/sacrificial barrier/Al, is analyzed with Ti, V, or Cr as the sacrificial barrier material. A study of Cr as a barrier between Al and NiSi, Pd_2Si, or PtSi reveals that impurities in the as-deposited Cr film determine the barrier properties. The concept of the sacrificial barrier is critically reexamined in the light of these results. A study of a thin W layer, which is probably a stuffed barrier, as a barrier between NiSi and Al is reported. An outlook to future trends and approaches concludes this part of the thesis.

A major attribute of silicides as interconnection material is their capability to form SiO_2 upon thermal oxidation. A study of the oxidation characteristics of near-noble metal silicides (Co, Ni, Pd, and Pt) is presented in the second part of this thesis. The oxidation kinetics and the mass transport through the silicide during oxidation

are explored. The role of mass transport in the oxidation kinetics is reviewed in the light of all the reported experimental results. The effect of oxidation on: a) the epitaxial registration of a silicide on <111> Si substrate ($NiSi_2$, $CoSi_2$ and Pd_2Si), and b) the electrical resistivity ($NiSi_2$ and $CoSi_2$), is explored. Properties of SiO_2 grown on different (Ti, Co, Ni, Pd and Pt) silicides are found to be the same as for SiO_2 grown on Si substrates, except for the lower ($\sim 1.5 \times 10^6$ V/cm) dielectric breakdown. A preliminary implementation of interconnections with $NiSi_2$ demonstrates the applicabilty of this silicide for VLSI. Finally, a novel interconnection scheme is advanced as a possible method to produce self-confined metal interconnection lines.

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CHAPTER 1 INTRODUCTION

To appreciate the potential contribution of silicides as a valuable material for VLSI (very large scale integration) application, an in-depth survey of the needs and requirements of this advanced technology is called for. In this introduction, I intend to highlight the technological frontiers in VLSI implementation. I concentrate mainly on those aspects where silicides may play a dominant role in the future. This approach will place in a proper perspective my detailed experimental work described in this thesis.

With the advances in technology, the integrated circuit (I.C.) chip size, complexity, and device packing density are continuously increasing. Device scaling is being extensively employed to improve chip density and device performance. Historical trends analysis extending about 20 years back in time is popular in the I.C. technical community. Trends are usually plotted logarithmically in order to survey the progress and analyze the short term future. The technological advances and device modeling progress have enabled designers to reduce the minimum feature size λ by a factor of 1.14 a year since 1968. The minimum feature size can be fitted to the following form [1,2]

$$\lambda = 10 \exp [-0.135(\text{year}-1968)] \ \mu\text{m} \qquad (1)$$

which adequately presents the past since 1968, and projects submicron features in 1985 - an optimistic forecast. On the other hand, the improved manufacturing procedures are continuously reducing the number of defects per cm^2, thus making possible larger chip sizes. The chip size ($\sim \sqrt{\text{Area}}$) is growing by a factor of 1.08 per year. The fitted

formula

$$\sqrt{A} = 0.26 \exp[0.08(\text{year}-1968)] \text{ cm} \qquad (2)$$

is applicable. (The exponential factor 0.08 is the average over the data represented in Refs. 1 and 2.) For simplicity, I treat the technological implication of reducing λ and enhancing A separately.

It is important to recognize that scaling has been used in two different ways in the I.C. industry. The first application is an optical shrinkage of an existing layout. The linear dimensions (l) and the chip area (A) are scaled down by a factor of k (>1) and k^2, respectively. Here, the primary goal is to increase the total number of good chips per wafer. This scaling is primarily motivated by cost; the improved device performance is a bonus. On the other hand, scaling is also used to raise device performance and chip density, by increasing the size of memory chips or the complexity of logic chips. In this case, the actual chip size increases to the limit set by technology and yield, and the area is scaled up by a factor of M^2 (M>1).

In the following, I focus my attention on IGFET (isolated gate field effect transistor) devices scaling, but the general trend also applies for bipolar devices. The IGFET technology is the high density "state of the art" with regard to the number of devices per chip.

The theory on scaling down IGFET devices was introduced more than 10 years ago[3]. The transistor scaling relations are shown in TABLE I, (the parameters are defined in fig. 1) for both constant field and constant voltage conditions. The constant field condition represents an ideal case while the constant voltage represents a realistic implementation - where existing power suppply and circuit requirements impose the constant 5 V supply. The important enhancement of device

TABLE I

The effect of scaling on performance parameters

(k>1 , M>1)

	PARAMETER	CONSTANT FIELD	CONSTANT VOLTAGE	
TRANSISTOR	L,Z,t_{ox},X_j	1/k	1/k	
	Device Area	$1/k^2$	$1/k^2$	
	Voltages V, V_{th}, etc.	1/k	1	
	Current I	1/k	k	
	Power	$1/k^2$	k	
	Power per unit Area	1	k^3	
	Gate Delay $\tau_g \sim C \cdot V/I$	1/k	$1/k^2$	
CONTACT	W	1/k	1/k	
	$J_c \sim I/W^2$	k	k^3	
	$R_c \sim \rho_c/W^2$	k^2	k^2	
	$V_c/V \sim I \cdot R_c/V$	k^2	k^3	
INTERCONNECTION	t,h	1/k	1/k	1
	$J_l \sim I/(W \cdot t)$	k	k^3	k^2
	Chip Area	$1/k^2$ | M^2	$1/k^2$ | M^2	$1/k^2$ | M^2
	$R_l \sim l/(W \cdot t)$	k | Mk^2	k | Mk^2	1 | Mk
	$V_l/V \sim R_l \cdot I/V$	k | Mk^2	k^2 | Mk^3	k | Mk^2
	$C_{ls} \sim \varepsilon \cdot W \cdot l/h$	1/k | M	k | M	$1/k^2$ | M/k
	Line Delay $\tau_l \sim R_l \cdot C_l$	1 | M^2k^2	1 | M^2k^2	$1/k^2$ | M^2
	τ_l/τ_g	k | M^2k^3	k^2 | M^2k^4	1 | M^2k^2

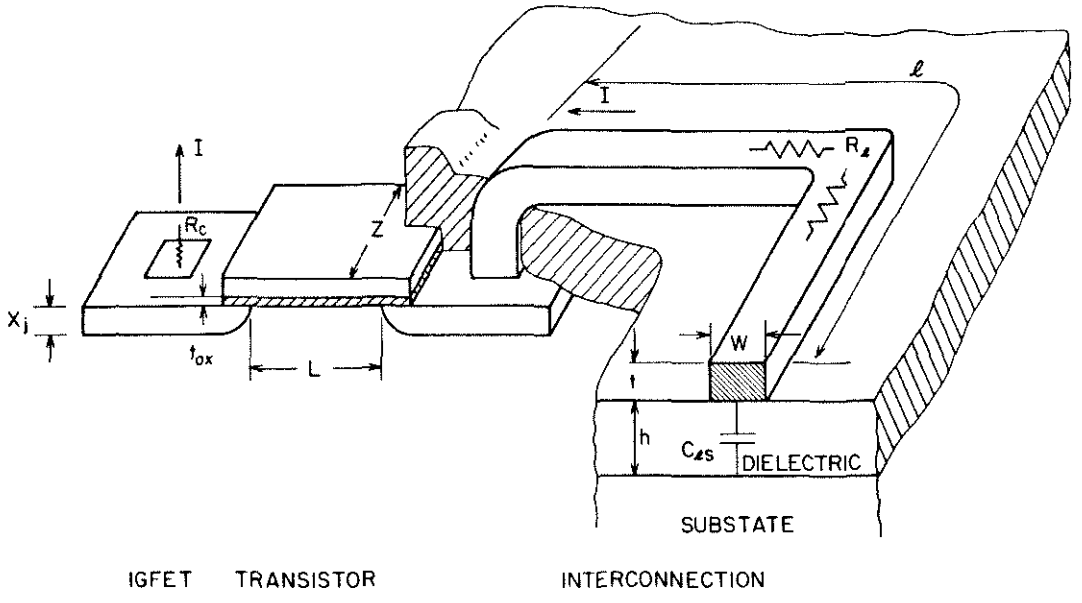


Figure 1 Schematic description of IGFET device and part of an interconnection line. Dimensions and parameters are defined for TABLE I.

performance, the reduction of the gate delay τ_g, is achieved in both cases.

The effect of scaling on contact parameters is also depicted in Table I. As dimensions shrink, the current density at the contact area increases and the normalized voltage drop across the contact (V_c/V), which influences the noise margins in the circuit, is increased. It is clear that, in order to maintain circuit performances, the contact resistivity, ρ_c, should be minimized. Contact reliability poses another severe requirement. According to Ref. 4, the median electromigration lifetime goes as $\sim (J_c)^{-10}$. This sensitivity to the current density makes Al unsuitable for small contact area. Solutions to this problem and the role that silicides might play in it are discussed in the first part of my thesis.

The striking effect of scaling on interconnections is described in the last part of Table I. I assumed, for simplicity, that the

capacitance between the interconnection and the substrate can be modeled as a parallel plate capacitor. The interaction with adjacent lines is not included, and the stray capacitance is neglected. Also, it is assumed that there is a linear relationship between $\sqrt{A}$ and l - the interconnection length. Of course, the length of many interconnection lines on a chip shrinks, but the length of long lines that connect different functions of the chip will stay constant in relation to the chip dimensions. The table incorporates the two scale down concepts: optical shrinkage ($A \sim 1/k^2$) or the maximum performance ($A \sim M^2$). As practical constraints play a major role in engineering solutions, the interconnect line thickness and the dielectric thickness were not scaled down as long as it was practical within the technological constraints. This enhances the interconnection performances due to smaller C_{ls} and lower R_l. A study of devices commercially available in recent years reveals that conductors and dielectrics have started to scale down substantially around the 3μm range of minimum feature size λ, hence, the column to the extreme right of Table I is the best case which is not attainable for $\lambda < 3\mu m$.

The importance of interconnection is manifested in two aspects: a) V_l/V, which is the normalized voltage drop in the long conductor, will be a factor of $Mk^2 \sim Mk^3$ higher. This parameter is important for noise margins and actually should be added to V_c/V. b) τ_l/τ_g which reveals whether the circuit operation is limited by gate delay ($\tau_l/\tau_g < 1/2$) or interconnection delay ($\tau_l/\tau_g > 1/2$). From Table I we see that τ_l/τ_g is scaled up by M^2k^2 up to M^2k^4. Using the historical trends (eqns. 1 and 2), τ_l/τ_g rose from 1968 to 1982 by a factor of 18×10^3 assuming conductor scale-down. The C_{ls} as given in Table I is actually too low

due to the omission of the contributions of fringe fields and sidewall capacitance, so that τ_1 is underestimated. A vivid example of the interconnection delay is supplied in Fig. 2 (taken from Ref. 1). Here the actual delay times for three different conductors (Al, silicide, and highly doped poly-Si) are compared to the "state of the art" gate delay time. An obvious conclusion of the above observation is that the line resistivity should be much lower than 500 μΩcm in order to utilize the built in speed of devices with feature size of less than 3 m.

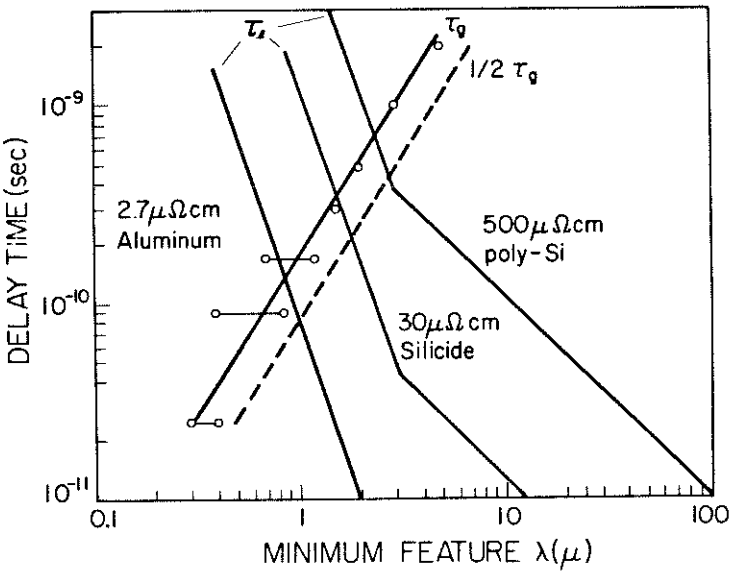


Figure 2 Comparison of gate (τ_g) and interconnection (τ_1) delay times as a function of the minimum feature size for several interconnection resistivities. (The change in slope at λ=3μm is due to the fact that thickness t,h must also be scaled down.)

The requirement for low resistivity interconnection line should be understood within the realm of I.C. technology. To do so, a short historical review is needed. The first IGFET processes introduced in the late 1960's used pure Al as a gate conductor. Since Al cannot withstand the high temperatures of diffusion and oxidation processes, it has to be deposited as a final processing step and aligned over the

source (S) and drain (D) area. The overlap capacitance to S and D area has a detrimental effect on transistor performance. It was then proposed that a metal capable of withstanding high temperature processing should replace the first level of Al. Refractory metals (W or Mo) with bulk resistivity of 5 μΩcm, were evaluated - but without success. Poor adhesion to SiO_2, silicide formation in the Si contact that consumed large amounts of Si and produced cracks due to volume changes, and uncontrolled oxidation of the metal (unstable metal oxides) were the major difficulties encountered. During the same period (late 1960's) another material, poly-Si, was proposed as the first layer interconnect [5]. Even though phosphorus- or boron-doped poly-Si presented much higher resistance (400μΩcm, at least) than either Mo or W, it immediately showed several properties that led to its dominance in the 1970's. Poly-Si can be deposited by chemical vapor deposition (CVD) techniques, and hence has good step coverage, oxidizes uniformly and controllably, adheres well to SiO_2, and can act as an implantation mask protecting the gate oxide during the source and drain implantation (self-aligned structure). As long as the minimun feature exceeded 3μm, the high resistance of poly-Si was no hindrance to its utilization (see Fig. 2). The possibility of exposing the poly-Si to high temperature oxidizing ambients was the key factor that established the Si-gate process as the uncontested dominator of the 1970's. Two key advantages thereby gained were: i) the possibility of oxidizing the source and drain regions as well as the edges of the poly-Si gate improves the breakdown voltages substantially and, consequently, enhances yield and reliability; ii) the grown SiO_2 provides isolation against an additional layer of poly-Si (or metal), thus making possible novel

stacked gate structures (EPROM'S) and increasing packing density of dynamic random access memories (DRAM'S). The ability to produce high quality SiO_2 with poly Si outwheighted the advantage of low resistivity of refractory metals. It was not until the late 1970's and early 1980's, when λ approached $3\mu m$, that poly-Si proved to be inadquate, and its replacement became one of the crucial issues in I.C. technology.

According to a recent report [6], out of 44 universities that are involved in VLSI research in the United States, ten conduct active research programs in interconnection technology. In Europe, where the only technological VLSI pilot project identified by the Common Market is "advanced interconnect for VLSI"[7], 26 out of 108 universities are exploring interconnection technology. At the industry level [6], 19 out of the 23 companies active in VLSI production in the United States are working on the interconnection problem. The interconnection technology is probably the most serious technological engineering problem in high-speed VLSI circuit, according to R.R.W. Pease [8].

Silicides present a possible solution for the interconnection problem. As I will show later, the two main requirements, low resistivity and the possibility to produce SiO_2 following thermal oxidation, are fulfilled. Furthermore, for complementary MOS technology (CMOS), metals in general are preferable to poly-Si [9] because their work function is adequate for both p-channel and n-channel devices (the work function is close to the Si midgap), while poly-Si has to be doped differently for each device type. In order to utilize silicides in VLSI technology successfully, an understanding of the oxidation process is mandatory. This topic is explored in the second part of this thesis.

CHAPTER 2 SILICIDE CONTACTS WITH Al

2.1 Introduction.

For I.C. technology, ohmic contacts are specified by i) the electrical resistivity ρ_c(Ωcm^2) and ii) the contact reliability. The resistivity of a planar contact, ρ_c, can be modeled[10] quite accurately. Two mechanisms are involved: the thermionic emission over the electronic barrier height of the contact (ϕ_B), and the tunneling through the barrier into the semiconductor. For doping level below 10^{17} cm^{-3}, the current is controlled by the thermionic emission and ρ_c is essentially independent of doping and depends only on ϕ_B. Tunneling will dominate when the Si doping level is above 10^{19} cm^{-3}. In order to achieve good ohmic contact (low ρ_c) , the highest surface concentration that is still compatible with the technological processing parameters is used. Silicides span a wide range of barrier heights to Si [11], and hence can be utilized to tailor ρ_c as needed.

Reliability of a contact structure has two aspects. One pertains to the reproducibility of ρ_c across the chip, the wafer, and from run to run; the other concerns the lifetime of the contact under operating conditions. What hinders the contact reproducibility most is the thin native oxide (10-20 Å) that forms quickly on Si as soon as it is exposed to air. Process-induced contaminations on the open contact window also affect ρ_c. To solve this problem, the contact material has to be able to break through the oxide and interact with the Si. Also, the reaction has to be uniform in order to inhibit spike formation that might short the shallow junction structure in the Si substrate. Al will reduce the

native silicon dioxide and will react with Si at the temperature range of 450 - 500°C. However, deep pits in the Si substrate can be observed if the Al is removed after the sintering operation. The depth of the dissolution pits depends strongly on the contact size (increasing as contact size decreases) which imposes a lower limit to practically achievable junction depths [12]. The lifetime of the contact depends on the current-induced mass transport into (or from) the metallic layer. Si electromigration in Al will consume material from the contact area, thus generating deep pits. The effect of contact electromigration in Al contacts to Si is similar to that observed during thermal annealing; pits develop in the Si, resulting in resistive contacts or shorted junctions.

Most silicides exhibit a very uniform reaction with Si [11]. The pitting problem does not occur. Silicides of Pd and Pt are already in use in bipolar I.C. technology, to produce Schottky barriers and ohmic contacts. In addition, the silicides delay the unwanted interdiffusion between Si and Al [13]. The compatibility of thick Al films with silicide layers is a problem of practical interest since Al remains a preferred metal for the final connection to other devices or to bonding pads.

An improved contact structure should consist of a silicide in intimate contact with the Si substrate, and a top layer of Al. But almost all silicides [I,II,III] react with Al. When the silicide is fully reacted, Al reaches the Si interface and the electrical properties of the contact deteriorate abruptly. Diffusion barriers should thus be introduced between the silicide and the top Al layer. The requirement on such a barrier is to produce low contact resistance and maintain the

Al silicide separation at temperatures needed for Al sintering (about 450 - 500°C).

2.2 Diffusion Barriers in Layered Contact Structure.[+]

The concept of a diffusion barrier is to interpose a material X between the deposited material A and the substrate material B, and thereby separate A and B from direct contact with each other [Fig. 1, Ref. I]. The conditions that an effective thin film diffusion barrier should meet are enumerated in our work [(I)]. Defects play a dominant role in determining the kinetics properties of a barrier layer, and the consequent importance of the deposition method and parameters prevailing during the deposition must be recognized [(I,III)].

A general classification for diffusion barriers has been proposed[(14)] that distinguishes three classes of barriers: i) Stuffed barriers are those whose low atomic diffusivities are attributable to the inhibiting effect of impurities along fast diffusion paths [Fig. 3, Ref. I]. ii) Passive barriers are thin conductive films that are chemically inert with respect to both materials A and B, and that have negligible solid solubility and diffusivities for A and B [Fig. 4, Ref. I]. iii) Sacrificial barriers exploit the fact that thin adjacent films often react with each other and form compounds in a laterally uniform way. By interposing a barrier layer that reacts uniformly and predictably with the materials A and B on either side of it, one effectively maintains a separation of A and B as long as the barrier is not fully consumed.

In my work I have concentrated on sacrificial barriers, which in concept offer engineering guidance rules for practical design. The point in time when the barrier is fully consumed is predictable when the

[+] For details see Ref. I.

two reaction rates are known as a function of temperature. As pointed out in the Introduction, the purpose is to separate the Al film from a silicide layer. In Ref. I we suggested the system be stabilized by using Ti, V, or Cr as a sacrificial barrier. The available data [15,16,17] indicates we can generalize that Cr reacts with a near-noble metal silicide (on a Si substrate) and forms $CrSi_2$ at a rate that is equal or slower than that of Cr reaction with bare Si substrate. Since this reaction (Cr with the Si substrate) is well characterized [11], it can serve as an upper limit to the reaction rate of Cr with a silicide layer. The same assumption was adopted for Ti and V [Table I, Ref. I]. The reaction and compound formation of Al films with Ti, V and Cr have also been well characterized [Table II, Ref. I]. Using the known time/temperature dependence of the sacrificial barrier (Ti, V or Cr), one can design a barrier for a particular application. Table III in Ref. I gives the minimum barrier thickness required, according to this concept, to maintain Al separation from the silicide on a Si substrate for thermal annealing at 500°C for 15 minutes.

The proposed contact structure is Si/silicide/sacrificial barrier/Al. In practice, when near-noble metals are used for the silicide (Ni, Pd, or Pt, for example), their silicide formation rate is much faster than any other reaction in the above system. It was shown [II,III,17] that the simplified structure of Si/(near-noble metal)/sacrificial barrier/Al, which can be deposited in sequential processing steps and subsequently preannealed at low temperature, can be used to generate the proposed contact structure. In this case, we have three interfaces, for each the reaction rate is known and the holding time of the sacrificial barrier can be predicted.

It is important to stress that the above picture is based on known rates of uniform reactions that are impurity-independent. No interfacial or bulk impurities are involved. It remains to be proven that such is the case in actual implementation.

2.3 Evaluation of the Sacrificial Barrier Concept - Cr as a Barrier.[+]

To check the model, as presented in the previous section, I chose Cr as the sacrificial barrier. All three relevant interface reactions (Si/metal silicide [11], Si/metal silicide/Cr [16,17], and Cr/Al [18]) have been thoroughly investigated. The metal silicides in the above cases were PtSi, Pd_2Si, and NiSi. The electrical stability of the contact structure was characterized by electronic barrier height measurements as an indicator for the integrity of the Si-silicide interface. This is the interface that the Cr barrier must protect from interaction with Al. In my study [III], Ni, Pd, and Pt silicides were chosen because they can be formed uniformly and reproducibly at relatively low temperatures on Si substrates. Pt and Pd silicides are widely utilized in Si contact structures. They also span a wide range of usable barrier heights (0.66, 0.74, and 0.85 eV for NiSi, Pd_2Si, and PtSi, respectively).

The main results of this study are twofold. It is first established that, with films deposited in a conventional fashion, Cr does indeed act as a sacrificial barrier as the model predicts. These results also agree with most of the observations reported in the literature. However, it was additionally found that Cr fails as a barrier when the films are deposited in a separate evaporation system and at high rates. Evidence suggests that impurities are critically associated with these different behaviors.

The successful design of a sacrificial barrier depends on two

[+] For details see Ref. III.

assumptions: i) that the reactions at both interfaces of the barrier be laterally uniform, and ii) that the reaction rates be known and reproducible. In the case of Cr vast variations are found in the reaction rates with Al, depending on the deposition conditions. The same also holds for Ti according to results reported bu other researchers (9,20,21 and 22 in Ref. III). The second requirement of known and reproducible reaction rates is thus not fulfilled. The fact that fairly consistent values for Cr/Al reaction have nevertheless been reported by independent investigators strongly suggests that impurities may actually help in equalizing reaction rates. Moreover, impurities may also improve lateral uniformity of a reaction by reducing the influence of diffusion along grain boundaries. The successful implementation of a sacrificial barrier may thus ultimately depend on the presence of impurities, in which case the concept of a sacrificial barrier emerges as a mere special case of a stuffed barrier. The sacrificial barrier may then be implemented for specific cases and in specific systems where the impurities are incorporated consistently from run to run.

2.4 Thin W as a Diffusion Barrier.

2.4.1 Thin film interactions.[+]

The experience accumulated with passive barriers indicates that the optimum film thickness is rather thin (e.g., 400-500 Å for reactively sputtered TiN [19]). This optimum presumably results from stresses that build up in the barrier film as it grows thicker. By its definition, the thickness of a passive layer plays no role in its efficiency as a barrier. The film integrity (e.g., no pinholes) is the major requirement for the chemically passive barrier material, and, evidently, reactively sputtered TiN few hundred Å thick yield a complete coverage reproducibly - and thus optimum performance.

Backscattering spectrometry (BS) as an analytical tool provides very direct insight into the reaction of thin films when the constituting elements have different atomic masses. But BS has been, so far, of limited value in analyzing Al-Si systems because the atomic masses of Al (27 a.m.u.) and Si (28 a.m.u.) are very close. When the barrier layer thickness is getting thinner, the energy loss through it will not suffice to separate the Al BS signal from that of the underlying Si. Hence, BS cannot provide the details of thin film interactions between the Al and Si, as long as the Al is the top layer.

In Ref. II, I have developed an experimental procedure that is capable of resolving the Al-Si interaction using BS. I used thin (about 2 kÅ) self-supported silicon substrates to investigate the Al/silicide interaction. The thin substrates enabled me to probe the interface from

[+] For more details see Ref. II.

the Si side as well. When the Si is the top layer, the Al and Si signals are distinguishable, can be isolated, and the reaction can be analyzed.

Using this method, an Al contact to the nickel silicide with a thin interposed W barrier, was explored [II]. A thin layer (250 Å) of W placed as a barrier between the Al and the silicide is shown to inhibit the Al-silicide reaction at 450°C for at least 40 minutes. Also, I described a procedure that only require a single deposition and single annealing step and yields a reliable Al contact to NiSi on a silicon substrate.

2.4.2 Electrical characterization+

The electrical characteristics of the metal-semiconductor interface are sensitive to concentrations of the Al penetration that are below the detection limit of BS. For example, a 50 Å surface layer doped with Al (N_A = 5 x 10^{18} cm^{-3}) increases the Schottky barrier height (SBH) by about 80 mV [20] which can be easily determined from the I-V characteristics, while BS cannot detect 2.5 x 10^{12} atoms of Al in the Si interface layer. To check the applicability of the W barrier, as suggested in the previous section, electrical measurements of the SBH should be conducted. This test is also the practically relevant one.

The study reported in Ref. IV shows that the thin W barrier removes the thermal instability that is observed in the Schottky diodes with an Al film on the NiSi contact to <Si>. As explained before, this structure can be formed by the sequential evaporation of Ni, W, and Al

+ For more details see ref. IV.

and the subsequent thermal annealing to form NiSi. SBH measurements show that the contact is thermally stable at 450°C up to about 1 hour annealing with very little change in the electronic barrier height.

Based on the electrical measurements, a model is proposed for the failure mode of the W barrier after excessive thermal annealing. The results can be modeled in terms of localized failures of the W barrier. This failure mode is likely in a thin film. The model represents the sample in terms of an equivalent circuit with two diodes in parallel. One diode has the original barrier height of the desired contact, and the other has the high SBH of the Al reacted layer. The area ratio between the two diodes determines the I-V characteristics.

Based on these experiments the distinction as to whether the W film acts as a stuffed or sacrificial barrier can't be made. Another study[21] concluded that a sputtered W layer, 2000 Å thick, between Al and silicide ($CoSi_2$, $MoSi_2$ and $Pt_xNi_{1-x}Si$) is an effective barrier against the Al interaction at temperatures below 500°C. This investigation didn't explore the detailed mechanism by which the W barrier works. In light of the results obtained with the Cr barrier it is most likely that W is a stuffed barrier because impurities (e.g., oxygen) are easily incorporated in the W film during deposition.

2.5 Further Studies.

The studies reported here are only a part of the massive effort toward a solution to the ohmic contact problem. Barriers are widely utilized in production; Ti-W (which is probably a stuffed barrier) is very popular, and TiN, which gains ground in numerous applications, are only two examples. But the VLSI requirements open a new frontier. As contact sizes approach the $1\mu m^2$ area, the planar approach does not hold anymore. The dielectric thickness, in which the contact window is opened, is in the order of $1\mu m$. Hence, the ratio between the linear dimension of the contact at the interface to the Si substrate and the height of the sidewalls of the dielectric is about 1:1. This nonplanar configuration poses a severe requirement on the barrier layer. The step coverage and the role of stress at sharp corners are crucial additional factors to consider (Fig. 3(a)). A case was brought to my attention where a barrier layer that operated successfully for $2\mu m$ geometry failed completely for a contact of $1\mu m$. The barrier had to be redesigned.

Novel approaches are currently explored for suitable contact structures. A self-aligned deposition process that selectively covers the exposed Si (or silicide) area at the bottom of the contact structure, but does not deposit on the dielectric (Fig. 2(b)), offers a solution that may avoid the weak spots at sharp edges. Contact studs (Fig. 2(c)), made by self-aligned CVD poly-Si[9], or metal plugs prepared by a complicated lift-off process[1] embody yet another promising solution that serves two purposes: i) elimination of the Al interaction with the Si substrate, and ii) planarization of the Al contact metallization.

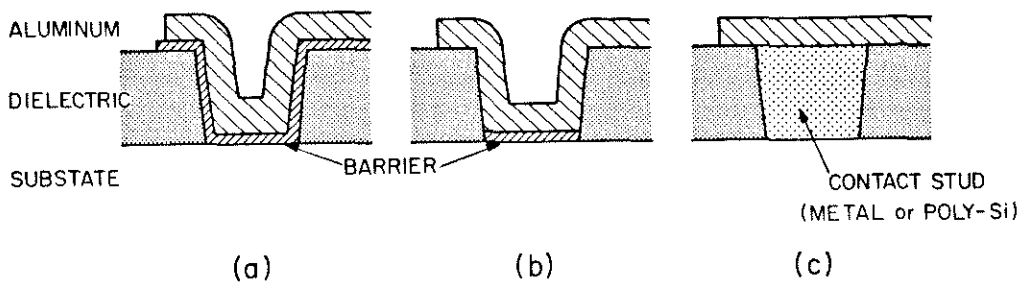


Figure 3 Barrier configurations in small contact window.

a) Barrier coverage, below the Al metallization, over the dielectric steps.
b) Self-aligned deposition of the barrier at the contact interface.
c) Contact study that planarizes the contact structure and solves the problem of Al step coverage.

The failure modes of such a novel contact structure are conceptually different from the simple one developed before [I] that assumes a uniform planar reaction. Adding a second dimension ("steps") to the contact configuration generates a new set of requirements and calls for reevaluation of the diffusion barrier characterization as defined in Ref. 14.

Such an abstract definition is difficult to formulate before the possible failure mechanisms are explored and understood. In order to do so, a special test vehicle should be developed for a confined structure evaluation. I feel that this is the route that diffusion barrier research should now take.

CHAPTER 3 SILICIDES OXIDATION

3.1 Introduction.

The importance of the oxidation characteristics of a silicide is addressed in the Introduction. The capability to form SiO_2 combined with a low resistivity defines a class of materials that are good candidates for VLSI interconnections. The electrical resistivity of almost all silicides is at least one order of magnitude lower than poly-Si[11]. In industry, some silicides ($TiSi_2$, $TaSi_2$, WSi_2 and $MoSi_2$) are already used in VLSI processing, and 256K memory chips built with silicide interconnections are being developed. The oxidation capabilities are not always utilized in these applications.

In this thesis, the oxidation processes, their control, and the final results are discussed in terms of their significance to VLSI application. First, I will describe oxidation kinetics studies of near-noble silicides that were not explored before. A deeper understanding of the oxidation process is gained from studies of the mass transport, that takes place in the silicide during oxidation. Then follows an overview of processes controlling silicide oxidation, and the role of mass transport in it. As will be seen, the transport of the oxygen-containing molecule through the growing SiO_2 layer is the rate-limiting step and is similar for all silicides. It is thus expected that the SiO_2 properties should also be similar for all silicides. Following a brief discussion of the effect of oxidation on the silicide properties (morphological and electrical), the SiO_2 properties that are important in I.C. applications are compared for

various silicides. The basic conclusion is that the properties are independent of the silicide on which the SiO_2 is grown. After this systematic treatment of the oxidation characteristics of silicides - and after having explained them - a test case is chosen for detailed evaluation. Some further studies and speculations conclude this chapter.

3.2 Silicide Oxidation Studies.

Most silicides films will grow a SiO_2 layer on their top upon thermal oxidation[V,VI]. As long as Si is in adequate supply from below (from <Si> substrate, or the poly-Si on insulating substrate), the silicide film will remain stable. The silicide layer in this case acts as a "membrane" with Si being transported through it.

To gain understanding and, eventually, control of the oxidation process, the first step is to characterize the SiO_2 growth kinetics. Reproducible results give a clue to a physical process that can be harnessed for utilization. These kinetics studies will reveal the significance of the silicide configuration (silicide on different <Si> substrate orientations, or on poly-Si, or the silicide thickness, for example). Further studies will branch out from there. The oxidation kinetics of $NiSi_2$, $CoSi_2$, Pd silicides and PtSi, will be reported first. These silicides of near-noble metals form a class that was not explored before. As will be shown later, they are also potential candidates for interconnection material in VLSI. The generalized overview, as derived from other silicide kinetics studies, is reported in section 3.4.

3.2.1 $NiSi_2$ oxidation kinetics.[+]

I investigated thermal oxidation of $NiSi_2$ on a Si substrate in the temperature range of 700-900°C, in a dry and a wet oxidation environment. The surface layer of SiO_2 grows parabolically with time. The growth rate is independent of the crystalline structure (epitaxial

[+] For details see Ref. VII.

or polycrystalline) and thickness of the $NiSi_2$ layer. From these results, I surmise that the rate-limiting oxidation mechanism is oxygen diffusion through the growing SiO_2 layer. Activation energies for the dry and wet oxidation are 1.0 $\pm$ 0.1 eV and 1.5 $\pm$ 0.1 eV, respectively. A detailed discussion and comparison of these oxidation kinetics with that of Si and of other silicides appear in section 3.4.

3.2.2 $CoSi_2$ oxidation kinetics.[+]

Nickel and Cobalt form quite similar disilicides. The structure (CaF_2), the formation temperature (650-750°C), and the epitaxial orientation on <111> Si substrate are common to both, but the growtu kinetics are dissimilar[11]. It is therefore of interest to compare the oxidation kinetics of those two disilicides. In the temperature range of 650°C - 1100°C, the oxidation kinetics of $CoSi_2$ are similar to those obtained for $NiSi_2$. A parabolic time dependence (transport limited process) and a rate independent on silicide parameters (thickness, orientation, etc.) are common to both. A comparison of the oxidation data for $NiSi_2$ and $CoSi_2$ (Ref. VIII Fig. 1) shows that the kinetics are practically the same. Since the growth kinetics of Ni and Co disilicides are dissimilar, the common oxidation rate must be a result of a common limiting process, which is the transport through the oxide of the oxygen-containing molecule.

[+] For details see Ref. VIII.

3.2.3 Pd_2Si and PdSi oxidation studies.

The Pd silicides differ from those of Ni or Co. The phase formation sequence of a thin Pd film interacting with Si is: Pd_2Si first, followed by PdSi at about 800°C, which is the final phase. Unlike Co or Ni, Pd has *no disilicide*. The crystal structure (Pd_2Si, hexagonal Fe_2P, PdSi, orthorhombic MnP)[11] is also different ($NiSi_2$ and $CoSi_2$ have cubic CaF_2 structure). It is then of interest to investigate the oxidation of Pd silicides. One should note that PdSi exists only between 800°C (formation temperature) and 900°C (melting point). At lower temperatures, the PdSi dissociates into Si and Pd_2Si[22]. Also, the interface of PdSi with the Si substrate is expected to be rough since it grows in a laterally non-uniform fashion[11].

For this oxidation study, I have performed eight experiments in parallel comparing the oxidation of PdSi and Pd_2Si, on a <111> versus <100> Si substrate, and for thin versus thick silicides. The deposited Pd thicknesses were 400 Å and 1000 Å for the thin and thick silicides, respectively. The formation temperatures were 500°C and 850°C for Pd_2Si and PdSi, respectively. As prepared, both silicides exhibit a planar interface with the Si substrate regardless of thickness or substrate orientation. For I.C. processing oxidation times longer than a few hours are unacceptable. Due to the low temperature range suitable for Pd silicides, the oxidation was characterized only for the wet oxidation process, which is faster than the dry one. The results, applicable only for wet oxidation, are as follows:

a) Oxidation performed at 750°C yields similar SiO_2 thickness for all eight samples. The growth rate is 3.2×10^6 $Å^2$/hr ± 15%.

The parabolic time dependence indicates a transport limited process which, as discussed before, is most probably the in-diffusion of the oxygen-containing molecule.

b) The silicide/substrate interface remains uniform and sharp for Pd_2Si on both <111> and <100> Si substrates. But for PdSi, a non-uniform morphology is observed (using BS analysis) following the 750°c oxidation. Optical microscope inspection reveals a non-uniform surface. X-ray analysis detects both Pd_2Si and PdSi, which is in agreement with the phase reversal expected at that temperature. Because of this transformation and morphological nonuniformity, I conclude that PdSi on a Si substrate is of doubtful utility. Oxidation of PdSi at 850°C improves the silicide morphology somewhat, but it is not as uniform as Pd_2Si oxidized at 750°.

c) It is well known that Pd_2Si grows epitaxially on both <111> and <100> substrates. Using x-rays, I confirmed the epitaxial registration of Pd_2Si on <111> substrate before the thermal oxidation and, as expected, found the same orientation after oxidation.

d) During the oxidation studies, a surface layer of PdO_x was noted on a few samples. The layer is less than 100 Å thick, but its appearance on the sample's surface was not consistent. According to Ref. 23, this phenomenon was observed also for $TiSi_2$ oxidation when the loading conditions into the oxidation furnace were uncontrolled. The claim is that before the sample reaches the oxidation temperature, metal oxidation occurs. But a recent study[24] of the same silicide ($TiSi_2$) disagrees with the above

argument and explains that the metal oxide surface layer is formed from oxygen contamination within the films (from sample preparation) that segregates and rises to the surface prior to the start of the SiO_2 formation. In the case of Pd_2Si, I find that different loading conditions do not inhibit (or enhance) the surface metal oxide layer. Samples loaded into the furnace in N_2 environment, and allowed to achieve the desired temperatures before wet O_2 was introduced, yielded the same results as the sample introduced directly into the oxidizing ambient. On the other hand, I found that fresh samples prepared less than four days before oxidation have no detectable PdO_x layer, while Pd_2Si samples from the same wafer, stored at room temperature for two months, and oxidized the same way, exhibit surface oxide. This tends to confirm the argument for imbedded oxygen impurities. It is surprising to find that some oxygen incorporation occurs at room temperature in Pd_2Si.

Bascially, the Pd_2Si oxidation is a controllable process since no detrimental effects on the silicide are detected. But the fact that this silicide is sensitive to storage conditions and can be oxidized only at temperatures below 750°C rules it out as a potential candidate for VLSI interconnections.

3.2.4 PtSi thermal oxidation.

Platinum silicides are similar to palladium silicides with respect to the crystal structure and phase formation sequence of a thin metal on a Si substrate (M_2Si first, and then MSi, where M is Pd or Pt). But PtSi (orthorhombic, MnP structure) is formed at a much lower temperature than PdSi (300°C versus 800°C), so that oxidation studies can be performed only for PtSi on top of the Si substrate. The lowest eutectic temperature of the Si-Pt system is 830°C. As a precaution, all of the oxidation studies were performed at 750°C. Initial studies performed in a wet oxidation environment to achieve a fast growth rate demonstrated that: i) the growth rate is independent of the Si substrate orientation (<111> or <100>), ii) the growth rate is independent of the silicide thickness (800 Å versus 1610 Å), iii) the time dependence of growth combines linear and parabolic terms, and iv) the silicide/silicon interface deteriorates due to the diffusion of Pt into the substrate. The last observation, also known to affect the electrical characteristics of PtSi contact to $Si^{(III)}$, is more pronounced than that observed in the PdSi case. This deterioration probably rules out the PtSi utilization for VLSI. But the fact that the oxidation kinetics is affected by a process other than the transport of oxidant through SiO_2 (all other silicides I investigated exhibit parabolic time dependence of oxidation) prompted my interest to try and resolve the problem. Detailed study of PtSi dry oxidation at 750°C yeilded the following results:

i) Silicides thinner than 500 Å are unstable. Following oxidation (about 1 h at 750°C) the average Pt concentration at the surface (silicide/oxide interface) drops below 50%. This drop is

accompanied by a slower oxidation rate. For an extreme case, when the Pt concentration is very low, one anticipates that the oxidation rate will approach that of bulk Si; hence the gradual reduction is no surprise. Further studies have to be done on thicker silicides, such that PtSi will remain stoichiometric at the interface with the oxide.

ii) Silicides thicker than 800 Å exhibit an oxidation rate which is independent of the thickness. Similar to wet oxidation, the time dependence of growth growth is composed of linear and parabolic terms.

iii) At early oxidation stages, less than 50 hrs at 750°C, silicides on a <100> substrate oxidize at a faster rate than on <111> substrate. After 50 hrs, the oxide thickness on <111> and <100> substrate differs by less than 10% and is the same as that observed for $CoSi_2$ and projected for $NiSi_2$.

iv) The Pt diffusion into Si is proportional to the oxidation time and is basically independent of the silicide thickness.

Observation ii) implies that the reduction in the oxidation rate is not due to the transport through the silicide. The other process that, in this case, can affect the oxidation kinetics, especially at early stages, is the reaction at the oxide/silicide interface. From observation iii), we can conclude that this reaction is different for PtSi on <111> or <100> Si. PtSi is known to grow epitaxially on both <111> and <100> Si[11]; hence different orientations of PtSi are expected at the silicide/oxide interface which can explain the observed different reaction rates. The overall picture of PtSi oxidation is quite complex, and at the present time not fully understood. But it is clear that PtSi is not a good choice for VLSI implementation.

3.3 Mass Transport Through the Silicide During Oxidation[+].

All the experimental results available point out that the oxidation rate of a silicide is independent of its thickness. But variations in the rates do exist for oxidations conducted in different laboratories. The transport through the silicide may well affect the initial oxidation stage, but will be masked at high temperature or after a long oxidation time. Since the establishment of a net Si transport through the silicide during oxidation is a very basic issue, I have undertaken to investigate that aspect of silicide oxidation as well.

I studied the diffusion process through the silicide as described in Ref. IX. Generally, the diffusion process through the silicide can be investigated to give an answer to the following questions:

i) What are the diffusing species?

ii) Via what mechanism does the diffusion take place?

iii) What is the value of the diffusion coefficient of each species?

The last question can be addressed only after the first two are answered, and is difficult to investigate. My study[(IX)] concentrates on the identification of the diffusion species. The experimental procedure required to identify the mechanism is also addressed in a general fashion. In brief, the question of the mechanism can be addressed with tracer experiments, after the diffusing species has been identified by an *inert marker experiment*.

The identification of the moving species is done using an inert marker that is imbedded in the silicide but does not interfere with the

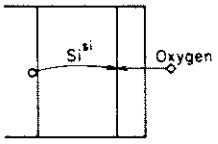
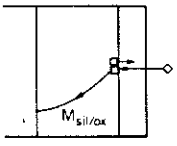
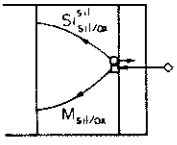
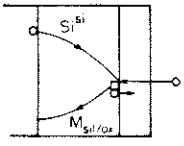
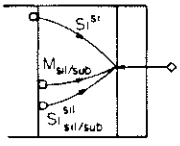
[+] For details see Ref. IX.

mass transport process. The marker position in the silicide layer is monitored by BS. A general transport model was developed that includes all the possible diffusion processes through the silicide that supplies Si to the growing SiO_2 layer and keeps the silicide stoichiometry intact. In Table II these processes are schematically described. With this model, the diffusing species can be identified directly from the position of the marker signal in the BS spectrum. Two limiting cases are listed first, where only Si is transported from the substrate through the silicide without apparently interacting with it or, the silicide dissociates at the silicide/SiO_2 interface and only the metal diffuses toward the Si substrate. A linear combination of these two limiting cases, and other less likely processes are listed next.

Inert markers (evaporated tungsten or ion-implanted xenon) were used to investigate the mass transport through Pd_2Si, PdSi, $NiSi_2$, and $CoSi_2$ during thermal SiO_2 growth. The metal is the dominant moving species during oxidation in all the above silicides, except in Pd_2Si where the experimental results point to Si diffusion, but these results can be questioned (see Ref. IX). In a recent study[25], we repeated the Pd_2Si experiment using ^{18}O as the inert marker and found again that Si is the dominant moving species during oxidation, but Pd also diffuses at a rate of about 1 Pd atom per 3 Si atoms. In that same study[25], we also investigate the diffusing species through PtSi, $CrSi_2$ and $TiSi_2$ during thermal oxidation, and find Pt, Cr, and Si to be the dominant moving species, respectively. Table II groups all the experimental results according to the basic processes. In the next section the implication of these results will be discussed.

TABLE II

The different possible processes of net Si transport through a silicide layer during oxidation. The experimental results are depicted.

MOVING SPECIES DURING OXIDATION	SCHEMATIC DESCRIPTION	EXPERIMENTAL RESULTS
	Si M_xSi SiO_2	
Si →	 Si supply	$TiSi_2$ Pd_2Si (?)
M ←	 dissociation	$CoSi_2$ PdSi
M ← Si ←	 "excess" dissociation	$CrSi_2$ $NiSi_2$ PtSi
M ← Si →	 dissociation + Si supply	
M → Si →	 Si supply causes metal release and diffusion	
M → Si ← Si ← M →	These processes do not preserve the silicide.	

3.4 The Role of Mass Transport in Oxidation Kinetics[+].

The investigations reported so far supply ample information to develop a general picture of the oxidation process. The four major steps controlling silicide oxidation are[V]: (1) oxidant transport through the silicide; (2) reaction at the silicide/oxide interface; (3) net transport of silicon atoms with respect to metal atoms in the silicide; (4) reaction at the silicide/Si interface. The oxidant transport is shown[VI] to be similar for all silicides. The reaction at the silicide/oxide interface is explored using equilibrium thermodynamics arguments. The experimental observation agrees quite well with the thermodynamics predictions. The net transport through the silicide was explored in section 3.3. Finally, the reaction at the Si interface cannot impede the oxidation kinetics; this conclusion is based on arguments derived from the silicide formation rates, and on the fact that the moving species during oxidation are the same as in the silicide formation.

The variation in the oxidation kinetics between Si and silicides, and between the silicides themselves, can be attributed to a different linear rate constant for different silicides. In particular, silicides in which the metal is the moving species oxidize more rapidly than bare Si.

Enhanced oxidation rates are desirable in IC processing since impurity diffusion in the Si with the already formed junctions should be minimized. The fact that an enhanced oxidation rate is associated with silicides that form by metal diffusion yields additional benefits for IC

[+] For details see Refs. V and VI.

processing. Those silicides are usually formed at relatively low temperatures (less than 450°C) with better control than refractory metal silicides, where Si diffuses during formation. When the metal moves during silicide formation, the Si/silicide interface is expected to be smooth. Kirkendall voids are not expected. Also from line width considerations and for self-aligned devices, it is preferable[23] that the metal move during silicide formation.

I thus conclude that, in those respects, silicides that form by metal diffusion are preferred candidates for IC interconnects.

3.5 Oxidation Effects on the Silicide Layer.

The overview presented in the previous section treats the silicide as a membrane layer that stays intact during the oxidation process. As was already discussed in subsections 3.2.3 and 3.2.4, the silicide layer is affected by the oxidation, and more so in some cases than in others. Optical microscope observation of all the silicides I investigated show some morphological changes. Stylus surface profiles, taken after removing the oxide chemically, indicate a rough silicide surface. From BS one deduces that the oxide form a uniform coating that duplicates the silicide surface layer morphologically (see also Ref. X). However, BS analysis cannot clearly resolve the silicide/Si interface; either the silicide has a very sharp interface with the Si substrate but varies with thickness or the metal diffuses into the Si and the interface is not sharp. These morphological changes depend on the Si substrate (<111>, <100>, poly-Si), on the silicide thickness, and on the oxidation conditions. Since it is difficult to characterize these structural changes, I chose the few silicides that are epitaxially oriented on single-crystal silicon, and monitored the epitaxial registry following oxidation.

The pertinent question to be answered is: what are the effects of oxidation on the electrical resistivity of the silicide? The conclusion is that in spite of the morphological changes, when care is taken, the electrical properties will not be affected.

3.5.1 Effect of oxidation on epitaxial structures.

Among the silicides studied, $CoSi_2$ and $NiSi_2$ yielded epitaxial layers that were of high enough quality to be quantitatively characterized by channeling before and after oxidation. For $CoSi_2$ and Pd_2Si, x-ray analysis was used to evaluate the layer registry.

$\underline{NiSi_2}$.[+] The study was conducted on <111> Si crystal. The quality of the epitaxial registry was monitored by channeling measurements, and quantified with χ_{min}, whose value is least for the best epitaxial layer. A series of samples was considered in which the initial thickness of the NiSi layers varied. The films were transformed to $NiSi_2$, in a first annealing step in vacuum, and then oxidized. It was found that χ_{min} was approximately the same for samples in which the total amount of Si consumed in these two annealing steps was the same. This similarity is readily understood when it is recognized that during oxidation, the silicide dissociates at the $NiSi_2/SiO_2$ interface and is reformed at the $Si/NiSi_2$ interface with nickel being the moving species[IX]. Oxidation-induced transport yields crystalline quality similar to that obtained after a correspondingly thicker silicide layer is formed.

$\underline{CoSi_2}$. The $CoSi_2$ layers, prepared simultaneously with the $NiSi_2$, were poly-crystalline due to the relatively low silicide formation temperature used (800°C). Following 1100°C oxidation, epitaxial

[+] For details see Ref. XI.

registry was observed using an x-ray Read Camera. Channeling experiments yielded a χ_{min} of 40% after 9 min of wet oxidation (2300 Å SiO_2) and 37% following 64 min wet oxidation (6100 Å SiO_2). Oxidation thus improves the epitaxial quality of $CoSi_2$. Similar samples annealed in vacuum at the same temperature were not transformed and remained poly-crystalline. On the other hand, $CoSi_2$ prepared at 1100°C yielded a χ_{min} of 8.6% after preparation and about 10% after oxidation, which is much better than the χ_{min} of $CoSi_2$ layers oriented during oxidation. The oxidation-induced transport causes the formation of the epitaxial $CoSi_2$. This can be explained, as for $NiSi_2$, by the fact that Co diffuses through the silicide and reforms as a new silicide on the Si substrate. At the high oxidation temperatures, the freshly formed $CoSi_2$ is epitaxially oriented.

Pd_2Si. As we have already discussed, the epitaxial structure of Pd_2Si is maintained during oxidation at 750°C. This case differs from $NiSi_2$ or $CoSi_2$ because Si is the dominant moving species, and the silicide is not reformed continuously at the Si interface.

The above observations of the dominant moving species (section 3.4) point out the similarity of the transport process during silicide formation and silicide oxidation. From the results of the epitaxial registration, I conclude that the transport induced by oxidation has similar effects on the silicide epitaxial registration as the transport during silicide formation.

3.5.2 Effect of oxidation on the electrical resistivity of a silicide layer.

The low electrical resistivity of silicides is one of their desirable attributes for VLSI interconnections. As seen from Fig. 3 (Chapter I) changes in the resistivity of an interconnection line results in an appreciable change of the line delay time. The effects of oxidation on the silicide resistivity should thus be investigated. Such a study was undertaken for $CoSi_2$ and $NiSi_2$ and the details are reported elsewhere[26,27]. The main results can be summarized as follows:

a) $CoSi_2$ and $NiSi_2$ behave similarly.

b) For a silicide layer on a single-crystal Si substrate, the resistance rises appreciably when the Si bound in the oxide exceeds 50% of the Si originally contained in the silicide film. For example, a 1000 Å thick silicide contains about $5x10^{17}$ Si atoms per cm^2 (for $CoSi_2$ or $NiSi_2$). When the oxide is 1100 Å thick, it contains $2.5x10^{17}$ Si atoms per cm^2; for oxides thicker than that, the resistivity increases. The silicide still contains $5x10^{17}$ Si atoms per cm^2, but as a result of the morphological changes induced by the reaction, the resistivity rises. Beyond this point, further oxidation produces fractures in the silicide layer and the resistivity may reach 10-100 times its original value. Thick $NiSi_2$ silicides ($\sim$ 3500Å) grown on <111> Si substrate exhibits microcracks[28]. We thus observe again, that oxidation has similar effects on the morphological structure as silicide formation. The big rise in the electrical resistivity is the result of the morphological evolution.

c) For silicide layers on an inert substrate (SiO_2 or Al_2O_3), Si is supplied by the decomposition of the silicide, which alters the electrical properties due to phase and morphological changes. Again, the rule of consuming less than 50% of the Si atoms in the silicide layer applies for practical applications. When the silicide film becomes metal-rich, a lateral instability develops that leads to the formation of a high resistance network of islands and finally a discontinuous film.

The conclusion from the above study is that in order to retain the good conductivity of Ni and Co silicides, the oxide thickness must be scaled to the silicide thickness. In actual application, up to 5000 Å thick silicide layers are utilized - hence at least 3100 Å of SiO_2 can be grown, which is adequate for processing.

3.6 The Properties of SiO_2 Grown on Silicides.[+]

On the basis of the similar growth characteristics of SiO_2 on different silicides, we expect the resultant oxide properties to be similar also. A comparative study of the SiO_2 properties grown on Ti, Co, Ni, Pd and Pt silicides (on a <Si> substrate) is reported in Ref. X. The density and stoichiometry of the oxide were found to be basically the same no matter what silicide was used. Electrical properties that were investigated are the dielectric constant, dielectric strength (breakdown field), and pinhole density. The dielectric constant was found to be 3.49 ± 0.24, which is similar to the values reported for SiO_2 grown on Si(3.2-3.8)[29]. The dielectric strength of the oxide layers depends on the polarity of the applied voltage, as is the case for oxide grown on poly-Si. For wet oxidation, the values are about 1.5×10^6 V/cm. This relatively low breakdown voltage (10×10^6 V/cm for SiO_2 on <Si>) is probably due to a rough silicide/oxide interface. The pinhole density in those oxides I examined is less than 40 per cm^2. I thus conclude that oxides grown on the silicides investigated hold promise for integrated circuits application.

[+] For details see Ref. X.

3.7 The Use of $NiSi_2$ as an Interconnection Material.[+]

All the oxidation studies reported so far in this thesis were conducted on large-area (about 1 cm^2), uniform samples. As a demonstration, a study on the applicability of $NiSi_2$ as an interconnect material was undertaken using narrow (5μm x 2600 μm) lines. The results of this study, reported in Ref. XII, demonstrate the applicability of thermal oxidation of a silicide line. Low-resistivity, high-dielectric strength of the grown SiO_2 and high-current capabilities are demonstrated. Also, a scheme is proposed to increase the local metallization level density using $NiSi_2$ as an interconnect.

[+] For details see Ref. XII.

3.8 Further Studies.

Of all the near-noble metal silicides investigated in this study, $CoSi_2$ seems to be the most promising one. It has a relativly low resistivity of 18-20 $\mu\Omega cm$[11] ($NiSi_2$ is about 40 $\mu\Omega cm$) and high-temperature processing capabilities[VIII]. It should be appropriate to repeat the study reported in section 3.6 for $CoSi_2$.

A speculative conclusion can be drawn from oxidation studies on inert substrates. As discussed in sub-section 3.5.2, Co or Ni silicide films become morphologically unstable as they turn increasingly metal rich upon thermal oxidation. But when the silicide is patterned to a narrow line structure, it is found[XIII] that the instability is attenuated. Long (more than 100μm) line segments remain uninterrupted and are actually reduced to crystaline Ni following extensive oxidation. Ref. XIII exploits this finding and proposes a novel method to produce metallic interconnection lines. One can generalize and suggest many other Si-metal combinations that would subsequently be reduced back to elemental high conductivity metal by oxidation.

My personal view is that the pursuit of the best interconnection technology should be carried out in the industry. The role of academic research is to explore the basic processes and to point out novel ideas. Only industry has the resources to pursue, exploit and utilize these ideas for VLSI technology. The investigations presented in this chapter yield a clear conclusion: silicides,(not only the refractory metal silicides), are excellent candidates for interconnections in VLSI.

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FINAL REMARKS

The written sequence of a thesis does not cover the true evolution of the scientific research project. The element of luck (or the lack of it) is screened. The freedom and the supportive guidance I received from my advisor, Dr. Marc-A. Nicolet, has enabled me to "follow my nose" and enjoy the excitement of discovery after an unexpected phenomenon caught my interest, and be "lucky," finally.

My original goal was to explore contact problems to Si utilizing silicides and diffusion barriers. In the early stages, when I was playing with the sample preparation techniques, I tried a "wild" idea.

In order to minimize surface leakage and develop a better test vehicle for metallization, I oxidized, at elevated temperatures, a contact pattern after the metal was already deposited. Of course, it did not work since the electrical characteristics of the silicide contact were changed drastically. (The reasons for that kind of change are currently explored using DLTS by Ms. Arati Prabhakar in Dr. T. C. McGill's group at the California Institute of Technology.) To my surprise, I found an SiO_2 layer on top of the silicide metallization. I reproduced the results and tried to characterize the process. The result of that work is summarized in the paper, "Thermal Oxidation of Nickel Disilicide"[(VII)]. Only while sorting the data and looking for references did I realize the potential applications of this process in VLSI technology. A comprehensive work on silicide oxidation was the result of the first "mishap." Another example is the thickness of the tungsten layer. Due to tungsten's high melting point (3410°C), I could not evaporate more than 250 - 300 Å thick layers. Since the multilayer

evaporation might include large amounts of impurities between subsequent layers, I tried the thin layer approach - and to my surprise it worked. Only later did I realized that for passive layers "the thinner the better" principle worked provided that no pinholes existed. Now after such a long road (being invited to talk about the subject), I feel that the importance of the first few steps of the project should be emphasized.

APPENDIX

Chromium as a diffusion Barrier Between NiSi, Pd_2Si or PtSi and Al

CHROMIUM AS A DIFFUSION BARRIER BETWEEN NiSi, Pd_2Si OR PtSi AND Al

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ABSTRACT

We show that the thermal instability that is observed in Schottky diodes with an Al film on NiSi, Pd_2Si or PtSi contact to <Si> can be removed by proper deposition of a Cr layer, 1000 - 2000 Å thick, between the Al and the underlying silicide layer. The structure can be formed by sequential evaporation of Ni, Pd, or Pt, Cr and Al, and subsequent thermal annealing to form the contact silicide and sinter the Al contact. Isochronal annealing for 30 min over the temperature range of 350°C - 500°C shows that the barrier holds electrically at 450°C and fails at 500°C. Forward I-V measurements are used to determine the barrier height, and elemental profiles are investigated using backscattering spectrometry. The successful utilization of the Cr barrier depends on the deposition conditions. Bilayers of Cr and Al deposited at high rates in another vacuum evaporator consistently reacted more rapidly than those usually observed by us and also reported in the literature. We believe that under usual deposition conditions the impurities incorporated in the films are essential for the successful operation of Cr as a sacrificial barrier.

Key Words: Diffusion barriers, Chromium barrier, contact metallurgy, solid-solid interfaces.

Introduction

Silicide contacts to Si have received much attention recently and are widely used as material to form ohmic contacts, Schottky rectifiers, IR detectors, and interconnects for integrated circuits. The compatibility of thick Al films with silicide layers is a problem of practical interest since Al remains a preferred metal for the final contact to other devices or to bonding pads. The direct contact between Al and near-noble metal silicides is unstable: metallurgically, Al forms metal compounds ($PtAl_2$, $NiAl_3$ or $PdAl_3$), and electrically, the Schottky Barrier Height (SBH) changes when all the silicide layer is consumed.

In a previous paper(1), we have suggested that the Al-silicide contact system can be stabilized with a sacrificial barrier between the Al layer and the silicide. A sacrificial barrier exploits the fact that thin adjacent films that react and form a compound often do so in a laterally very uniform fashion. A barrier layer that reacts uniformly with Al and silicide on either side of it effectively maintains a separation of the Al from the silicide as long as the barrier layer is not fully consumed by these reactions. This point in time is predictable when the two reaction rates are known as a function of temperature, provided that precautions are taken to avoid impurities in the films that might alter the reaction kinetics. We have suggested the use of Ti, V, or Cr for such barrier material.

In this paper, we evaluate Cr as a diffusion barrier between Al and NiSi, Pd_2Si or PtSi. We chose Ni, Pd, and Pt silicides because they can be formed uniformly and reproducibly at relatively low temperatures on a Si substrate. Platinum and palladium silicides are widely utilized in Si contact structures. They also span a wide range of usable SBH (0.66, 0.74, and 0.85 eV for NiSi, Pd_2Si, and PtSi, respectively). We characterize the electrical stability of the contact structure using barrier height measurements as an indicator for the integrity of the Si-silicide interface.

The main results of this study are two-fold. We first establish that with films deposited in a conventional fashion Cr does indeed act as a sacrificial barrier, as the model predicts. These results also agree with most observations reported in the literature. We additionally show, however, that Cr fails as a diffusion barrier when the films are deposited in a separate evaporation system and at high rates. Evidence suggests that impurities are critically associated with these different behaviors. In what follows, we therefore distinguish between results obtained with the "slow" or the "fast" evaporation systems.

Experimental Procedures

The Schottky diodes for our study were prepared on 0.003 Ωcm n^+ <111> silicon substrates covered with a 10 μm thick, 10 μcm n-type epi-layer. The contact areas ($1.16 \times 10^{-2} cm^2$) were photolithographically defined and opened using a buffered HF in a SiO_2 layer which was deposited on the wafers by low-temperature chemical vapor deposition (CVD). Prior to the loading for metal deposition, the wafers were etched for 10 sec in 1:10 HF. The metals (Ni, Pd or Pt), Cr and Al were sequentially evaporated without breaking the vacuum at pressures less than 5×10^{-7} torr. The depositions were conducted in two systems which are constructed similarly; both use ion pumps and e-guns. The only difference was the deposition rate of the metal layers. In the first ("slow") system, the deposition rate was 10-30 Å/sec with intermittent holds due to the manual control, while in the other ("fast") system, the deposition was maintained automatically at a fixed rate of 50 Å/sec. We also prepared samples only with silicide (no Cr or Al) and without the Cr barrier. For comparison, the silicides of some samples were prepared *in-situ* (at 400°C) before the Cr and Al were deposited. Large-area samples were prepared simultaneously for backscattering spectrometry (BS) analysis. Subsequent heat treatments were performed in a vacuum furnace at pressures less than 8×10^{-7} torr, or in N_2 flow in an open tube furnace.

The SBH was determined from fits of the forward I-V data to the ideal thermionic emission model. The reverse saturation current and Norde plots were also employed, where feasible, to confirm the results.

Elemental profiles were detected using BS with a 2 MeV $^4He^+$ beam.

Results and Discussion

1) Thin Film Interactions.

To perform as a sacrificial barrier Cr must react uniformly with the top Al film and with the bottom silicide layer. It is known that Cr reacts uniformly with Al, forming $CrAl_7$(2). The Cr consumption rate is $4.5 \times 10^{14} \times \exp(-1.91\ eV/kT)\ \mathring{A}^2\ sec^{-1}$(2) for annealing in dry nitrogen atmosphere at 300 - 450°C temperature range. The reaction of Cr with Pd_2Si has been investigated by Olowolafe, et al.(3), who demonstrate the uniform layer-by-layer growth of $CrSi_2$ on Pd_2Si. Also, Zingu, et al.(4), have clearly shown that the growth rate of $CrSi_2$ with an interposed Pd_2Si layer is equal to or slower than that on Si, depending on the Pd_2Si thickness. Previous studies of $CrSi_2$ growth on PtSi(5,6) or NiSi(6) have demonstrated a uniform layer-by-layer growth of $CrSi_2$.

Utilizing our slow system , we have investigated the reaction of Cr films with PtSi and NiSi films on Si. For these studies, we have used an initial configuration of Si/metal/Cr or Si/metal silicide/Cr; upon annealing, the former will transform into the latter at temperatures much below those at which Cr begins to react. The uniform formation of $CrSi_2$ on PtSi is shown in Fig. 1. Similar results are observed for <Si>/NiSi substrates. There is no detectable (using BS) mixing between the growing $CrSi_2$ layer and the underlying silicide. We

have shown(7) that the growth rate of $CrSi_2$ on <Si>/PtSi is slower than on <Si> substrate at the same temperatures. Also, there is a delay time before the $CrSi_2$ formation starts. This delay time is longer for Si/metal/Cr structures than for Si/silicide/Cr structures that were formed using *in-situ* heater.

Chromium was evaluated metallurgically as a diffusion barrier between Pd_2Si and Al(8) and electrically between PtSi and Al(9). It was shown(8) that Cr acts as a sacrificial barrier and inhibits the interaction of Al and Pd_2Si up to 90 min at 500°C. No electrical evaluations of this contact structure were reported. But on PtSi, it has been reported that there is a sharp drop in the SBH after the Cr layer is completely consumed by $CrAl_7$ formation(9). We conclude that metallurgically, Cr is adequate for a sacrificial barrier on top of NiSi and PtSi from our studies ("slow" system), and for Pd_2Si from the results of Refs. (3,4 and 8).

2) Electrical Stability.

Technologically, the process of sequential deposition without silicide formation (metal/Cr/Al) is preferable since it eliminates the need for *in-situ* heating and allows for a single sintering step outside of the evaporator. In our electrical measurements, we found no basic difference between the behavior of the Si/silicide/Cr/Al and the Si/metal/Cr/Al structures. The reason is that the metal silicide forms much before any other reaction takes place in the above structures. Our shortest annealing time will transform all the metal under the Cr

barrier to the silicide layer. We thus consider only the Si/metal/Cr/Al structures and compare them with the Si/metal/Al and the Si/silicide structures. The samples discussed in the following sections were produced in the "slow" Cr evaporation system and annealed in vacuum.

a) NiSi.

Failure of the Si/NiSi/Al contact structure is reported(10-12) to occur at 400°C after a very short annealing. The compound, $NiAl_3$, forms and the SBH rises above 760 mV. For such samples, we observed SBH as high as 800 mV following 350°C, 20 min vacuum annealing. On the other hand, isochronal annealing of <Si>/600 Å Ni/700 Å Cr/6000 Å Al structures for 20 min at 350, 400, and 450°C produced no change in the SBH (Fig. 2). Based on Ref. 1, a failure is predicted after 20 min at 465°C. At 500°C for 20 min, the barrier indeed fails. The SBH rises from 667 mV (which is the barrier height of NiSi) to 680 mV with an increase in the ideality factor. We presume that this is due to localized failures, similar to the failure mode that was suggested for tungsten barrier(12).

b) Pd_2Si.

The instability of the Si/Pd_2Si/Al structure was thoroughly investigated(13-15). A complex ternary phase is observed upon annealing at temperatures as low as 200°C(16). The SBH first decreases after 10 min at 300°C and then rises above its initial value(13). We show that the electrical stability of a <Si>/650 Å Pd/1700 Å Cr/7000 Å Al structure at 450°C is maintained for about 120 min (Fig. 3). The barrier height of Pd_2Si, 0.74 eV is maintained and the ideality factor

is constant before the contact fails. Calculation based on our model(1) predicts about 100 min before the barrier is fully consumed which agrees well with the facts.

c) PtSi.

The high value of the SBH of PtSi (850 mV) makes this contact very sensitive to any change at the Si/PtSi interface. It was reported(17) that the Si/PtSi/Al structure shows a reduction in the SBH when all the Pt in the silicide is transformed to $PtAl_2$. We find, for the Si/Pt/Al sample, an immediate decrease of SBH after 350°C, 20 min annealing of samples without a Cr barrier (<Si>/500 Å Pt/5700 Å Al, see Fig. 2). Also, BS spectra indicate that the atomic composition of the reacted layer is quite Al-rich (about 1:6 Pt to Al atomic ratio) and that about 0.25 at. % Pt is contained in the remaining Al layer. The effect of thermal annealing on a <Si>/700 Å Pt sample is described in Fig. 2, also, because for this silicide, the SBH is altered by annealing(18) even without Al. Figure 2 shows that after 20 min of annealing, the contact structure <Si>/630 Å Pt/1350 Å Cr/9500 Å Al starts to fail above 450°C, where there is a slight decrease in the SBH of PtSi from 0.85 eV to 0.83 eV. The sacrificial barrier model predicts(1) failure after 20 min at 485°C, which we consider in excellent agreement. After this 450°C annealing, BS analysis reveals that indeed there is a reaction between the Al and PtSi, but presumably not all the PtSi is consumed. Following a 500°C, 20 min annealing, Pt (at low concentration) was detected in the $CrAl_7$ layer and, as seen from the electrical measurements, the contact has failed.

3) Impurities Effect.

To check our results, we also prepared samples in the "fast" vacuum evaporator. In this case, reduced contamination levels (particularly of O_2) are expected. In a previous study(19) done with the "slow" system, about 7 at.% oxygen were detected (using SIMS) in the as-deposited Cr layer. For Cr films deposited in the "fast" system, we found by BS that the Cr reaction rate with Al was about 10 times faster than predicted in Ref. (1) at 460°C or than observed with the "slow" system. This annealing was conducted in an open tube furnace with N_2 flow. When the annealing was conducted in vacuum, the $CrAl_7$ formation rate was at least 100 times faster than the "slow" case. These samples had a very thick (2 m) Al layer, but apparently the impurities from the annealing environment diffuse quite easily through the Al layer at 460°C. It is important to note that even for such high reaction rates the $CrAl_7$ forms quite uniformly.

To check the effect of impurities in the Al layer, we prepared a sample in the "fast" system, but stopped the Al deposition after about 2000 Å. The system was opened to air briefly (thin Al oxide formation), and then pumped down again and the deposition was finished (in similar vacuum conditions) until about 2 m Al were deposited. In these samples, no reaction was observed after 3 h at 460°C, and electrically, the barrier height of the underlying NiSi was maintained. These results directly demonstrate that impurities do indeed affect this contact structure.

4) Sacrificial Barrier Holding Time.

The holding time of the Cr barrier prepared in the "slow" system reported above and in Ref. (9) agrees quite well with our prediction based on individual reaction rates(1).

On the other hand, the results obtained with the fast system indicate that these rates are system-dependent. The rates of reaction between Cr and Al reported by Ref. (2) and those extracted from holding times of Pd_2Si/Cr/Al(8), PtSi/Cr/Al(9) and our studies are all consistent with each other, although different systems are involved. One is thus forced to conclude that at least the Cr/Al reaction must be relatively insensitive to impurities above some threshold, but very sensitive below that. The identification of the impurities that affect the Cr/Al reaction and its quantitative characterization therefore emerges as one of the important issues raised by the present study. A corollary of these observations is that the notion of a sacrificial barrier may have to be reconsidered, because it is conceivable that in reality impurities must always be present to realize that concept.

Titanium films have also been investigated for sacrificial barrier application. One would expect, in light of the preceding comments, that inconsistencies should appear in the holding times reported for barrier structure prepared in different systems. Indeed, conflicting results exist as to the usefulness of Ti as a barrier. Solomonson, et al.(20), show that Ti really works as a sacrificial barrier and reacts uniformly with the silicide and the Al layer.

Merchant, et al.(9), also tested Ti as a barrier between PtSi and Al and found that the SBH is constant as long as some unreacted Ti is left. On the other hand, the same system was reported by Ting and Crowder (21) to fail much faster than predicted by our original model(1). From their data, we deduce a Ti consumption rate of about 140 $\mathring{A}^2$ sec^{-1} at 400°C, while we predict only 20 $\mathring{A}^2$ sec^{-1} based on Bower(22).

Conclusions

The concept of a sacrificial barrier depends on two assumptions: (i) that the reactions at both interfaces of the barrier layer be laterally uniform, and (ii) that the reaction rates be known and reproducible. The fulfillment of these assumptions will allow the design of a sacrificial barrier as outlined in Ref. (1). In the cases of Cr and Ti, we find vast variations in the reaction rates with Al, depending on the deposition conditions. The second requirement of known and reproducible reaction rates is thus not fulfilled. That fairly consistent values for the Cr-Al reaction have nevertheless been reported by independent investigators strongly suggests that impurities may actually help in equalizing reaction rates. By the same token, impurities may also improve the lateral uniformity of a reaction by reducing grain boundary diffusion. The successful implementation of a sacrificial barrier may thus ultimately depend on the presence of impurities, in which case the concept of a sacrificial barrier emerges as a mere special case of a stuffed barrier. The sacrificial barrier may then be implemented for specific cases and in specific systems where impurities are incorporated consistently from run to run.

Practically, the control of impurities in the film deposition or during annealing is difficult. A deliberate incorporation of impurities in the barrier (making it a stuffed barrier) in an amount which exceeds that needed to slow the reaction is a preferable procedure. The utilization of Cr(23) or Al(24) doped with oxygen was already suggested by others. It was shown(19) that oxygen in the Si is more effective in slowing down $CrSi_2$ formation than oxygen in the Cr, probably due to the fact that Si is the moving species. Since in $CrAl_7$ formation Al is expected to be the moving species(2), it may very well be that impurities in the Al layer have a dominant role in slowing the reaction rate. Indeed, we observed no degradation of the SBH even after 500°C when the Al was "stuffed" with impurities - probably mostly oxygen.

Chromium can be utilized as a barrier between Al and NiSi, Pd_2Si, and PtSi at 450°C, if the appropriate amount of impurities is incorporated in the film. Our study does not quantify this amount, but from our experience we can say that the evaporation performed at pressure higher than 1×10^{-6} torr at a rate lower than 10 Å/sec will result in films with a sufficient amount of impurities to make the barrier effective.

Acknowledgments

The authors wish to thank M. Parks for careful typing of the manuscript, and Solid-State Devices, Inc. (A. Applebaum, President) for partial financial and technical support.

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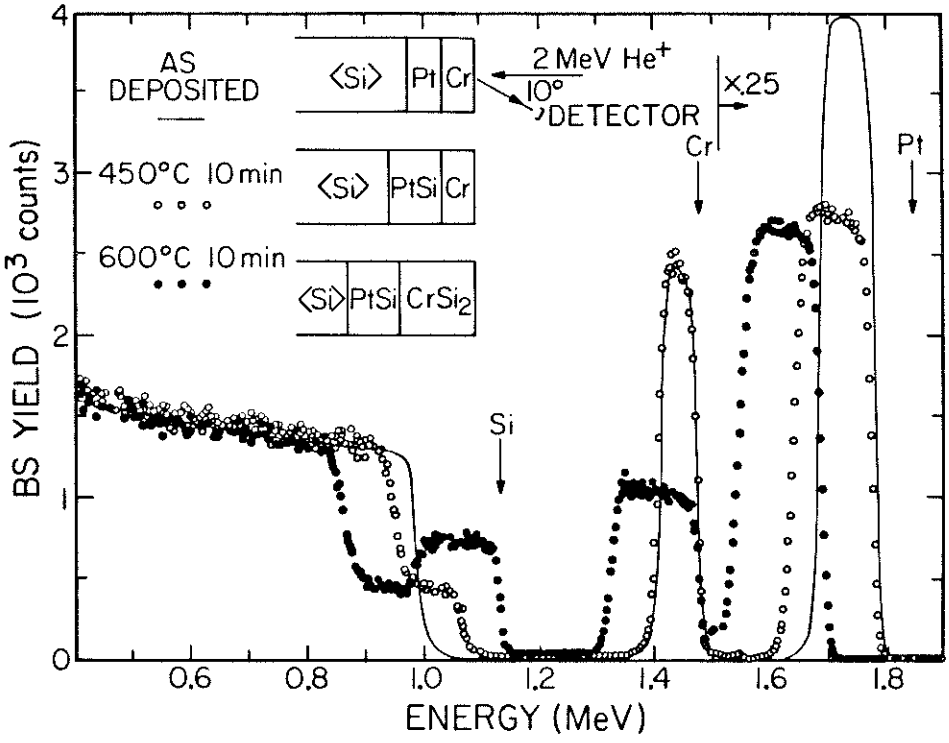

Figure 1 Silicide formation of Pt/Cr bilayer. First platinum silicide is formed and then at higher temperatures chromium disilicide is formed.

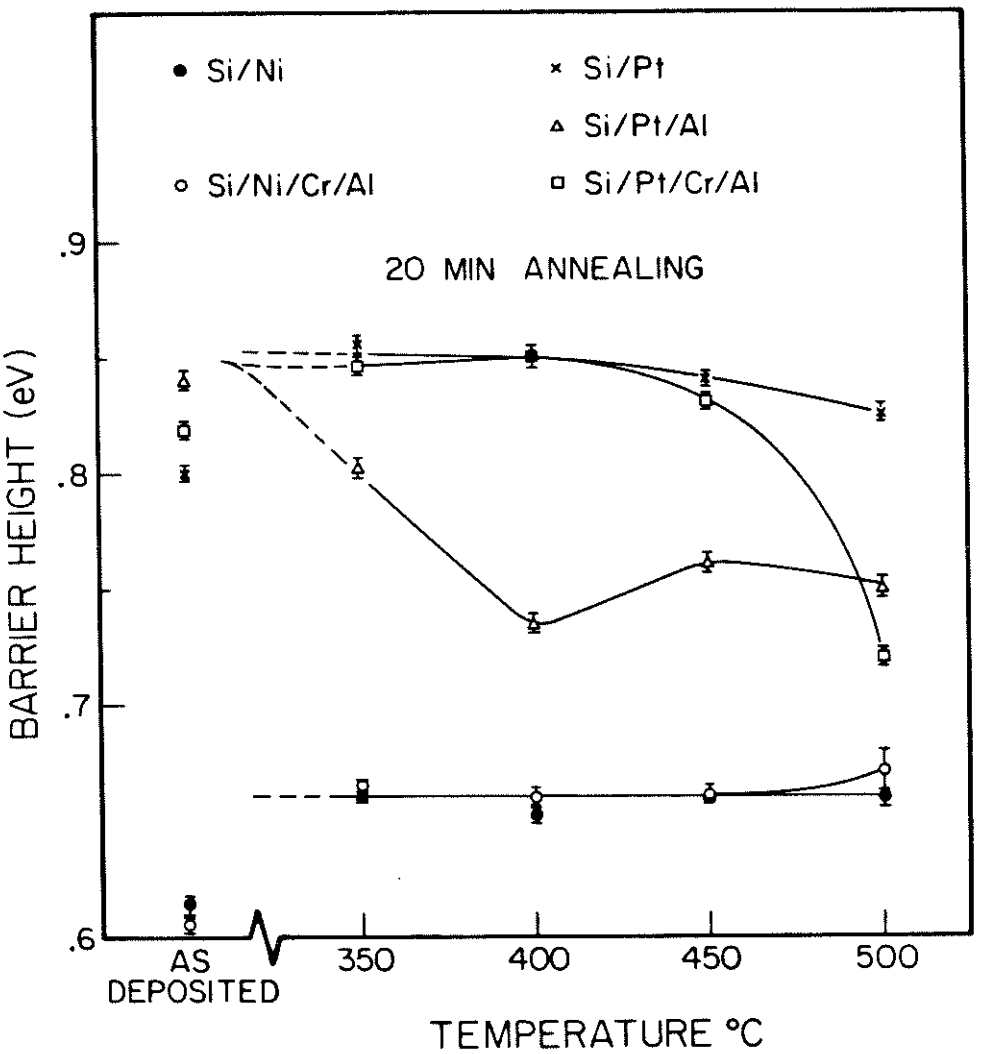

Figure 2 Schottky Barrier Height (SBH) of isochronal anneal of: • <Si>/590 Å Ni, ° <Si>/600 Å Ni/700 Å Cr/6000 Å Al, x <Si>/700 Å Pt, △ <Si>/500 A Pt/5700 Å Al and □ <Si>/630 Å Pt/1350 Å Cr/9440 Å Al. (Formed in "slow" deposition system.)

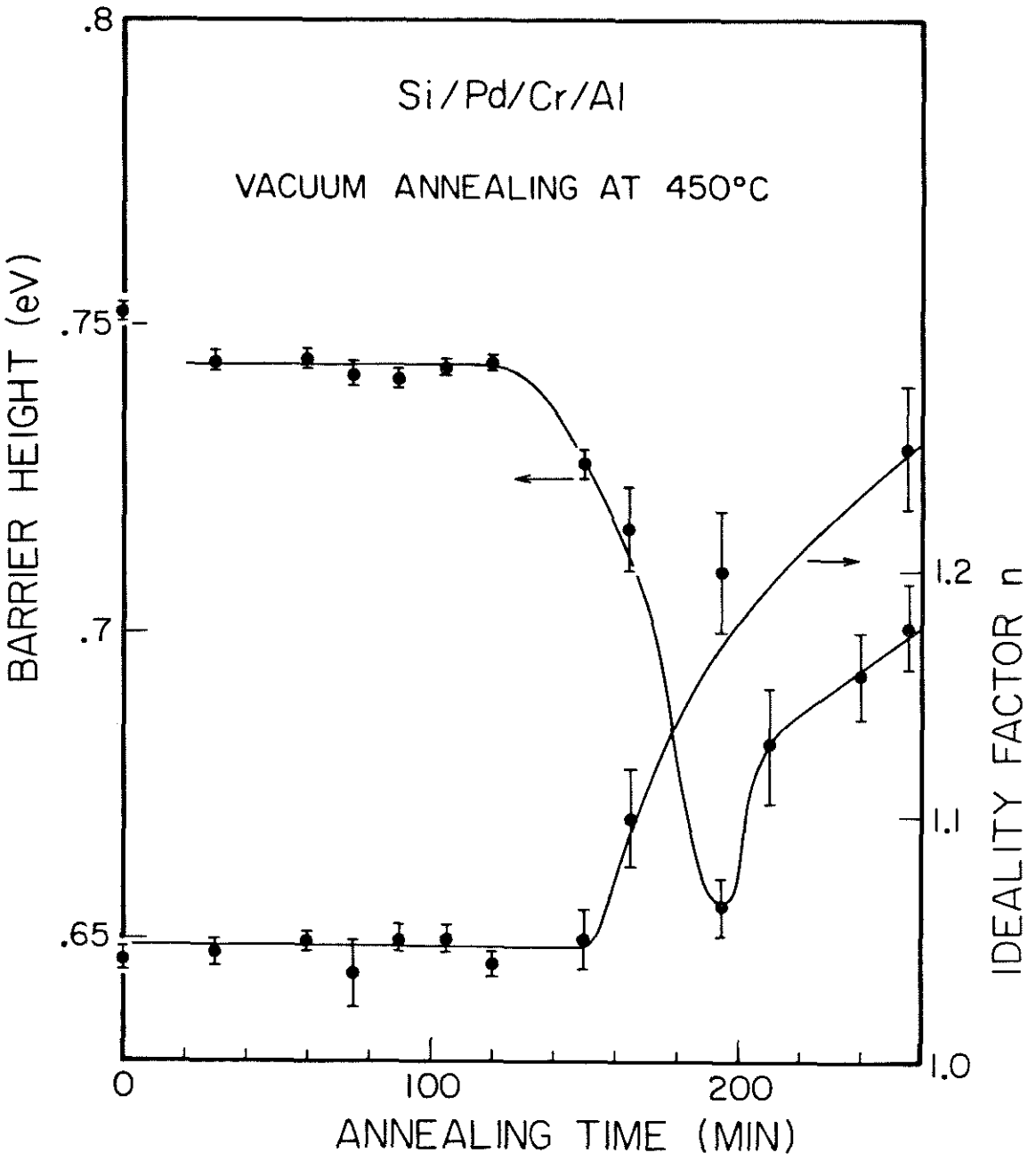

Figure 3 Schottky Barrier Height (SBH) of <Si>/650 Å Pd/1700 Å Cr/7000 Å Al as a function of isothermal vacuum annealing at 450°C. The ideality factor is also depicted. (Formed in "slow" deposition system.)