INVESTIGATION OF SUPERCRITICAL HEAT FLOW IN HELIUM II

Thesis by

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ABSTRACT

To investigate the validity of appending the Gorter-Mellink friction term to the equations of motion of liquid helium the temperature was measured along the axis of a channel carrying a supercritical heat current. A single thermometer on a traversing assembly was used permitting local measurements both in the interior of the channel and in the jet formed in the free fluid.

The temperature gradient in the interior of the channel is found to be in agreement with the Gorter-Mellink law up to the lamda point, but goes to zero within a channel diameter, in the free jet. Since the relative velocity between the two fluids is probably continuous along the axis of the jet in the vicinity of the exit, the disappearance of the temperature gradient appears to be inconsistent with the predictions of the Gorter-Mellink term.

The Gorter-Mellink A(T) was also measured up to the lamda point. A much stronger divergence is found as T_λ is approached than was indicated by previous measurements.

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I. Introduction.

In the two-fluid model of liquid helium below the lamda point, the fluid is considered as composed of two interpenetrating parts: the normal fluid with a density ρ_n and a velocity field $\underline{v}_n$, and the super fluid, with a density ρ_s and a velocity field $\underline{v}_s$. The total density of the fluid is the sum of the two, i.e.

$$\rho = \rho_n + \rho_s \tag{1}$$

while the total momentum density is given by:

$$\underline{j} = \rho \underline{v} = \rho_n \underline{v}_n + \rho_s \underline{v}_s \tag{2}$$

The normal fluid is normal in the sense that it is characterized by a viscosity η_n and it is possible to define a pressure p_n such that it satisfies a Navier-Stokes type of equation[1].

$$\rho_n \left(\frac{\partial}{\partial t} \underline{v}_n + \underline{v}_n \cdot \nabla \underline{v}_n\right) = -\nabla p_n + \eta_n \nabla^2 \underline{v}_n \tag{3}$$

The super fluid, on the other hand, is viewed as viscosity-free and irrotational. Its velocity field is therefore derivable from the gradient of a potential. In particular, its convective derivative is derivable as the gradient of a scalar field μ, i.e.

$$\frac{\partial}{\partial t}\underline{v}_s + \nabla\left(\tfrac{1}{2}v_s^2 + \mu\right) = 0 \qquad (4)$$

where arguments of Galilean invariance identify μ with the chemical potential per unit mass of the total fluid[2].

The super fluid component is regarded as entropy-free, and, to a first approximation, flows reversibly. Thus the flow of entropy is associated with the motion of the normal fluid. In particular, in the absence of entropy production,

$$\frac{\partial}{\partial t}\rho s + \nabla\cdot(\rho s\underline{v}_n) = 0 \qquad (5)$$

where s is the entropy per unit mass of fluid.

The temperature gradient term via the gradient of the chemical potential in the super fluid equation excludes heat conduction as a heat transport mechanism at steady state in the absence of any boundaries; a result borne by experiments. A convective, isothermal, transport of heat is the only mechanism of heat transfer under these restrictions. The heat flux vector is then given by the product of the entropy flux and the absolute temperature[3], i.e.

$$\underline{q} = \rho s T \underline{v}_n$$

In the presence of boundaries, the equations of motion allow temperature gradients to be established and maintained due to the

existence of the normal fluid viscosity. In particular, for a channel of constant cross section

$$\frac{\partial T}{\partial x} = - \left[\frac{G\eta_n}{(\rho s)^2 T} \right] q_x = - a q_x \qquad (6)$$

where G is a constant depending on the shape of the cross section (e.g. $G=8/R^2$ for a circular cross section of radius R). If the coefficient a does not vary appreciably in the channel, one finds that the temperature difference between the ends of the channel is proportional to the heat flux. This result is verified experimentally for low heat fluxes. At a certain critical value of q, however, one observes a new dependence of the temperature difference on the heat flux, which for values of q greater than this critical value, is empirically given by,

$$\Delta T = -\ell(aq + bq^3)$$

where ℓ is the length of the channel.

To account for this cubic dependence of the temperature gradient on the heat flux, Gorter and Mellink in 1949 postulated a frictional force between the two fluids proportional to the third power of the relative velocity[4]. In particular,

$$\underline{F}_{sn} = A\rho_n\rho_s w^2 \underline{w}$$

where

$$\underline{w} = \underline{v}_n - \underline{v}_s$$

With this term the equations of motion become,

$$\frac{\partial}{\partial t}\,\underline{v}_s + \nabla\left(\tfrac{1}{2}v_s^2 + \mu\right) = + A\rho_n w^2 \underline{w} \qquad (7a)$$

and

$$\frac{\partial}{\partial t}\,\underline{v}_n + \underline{v}_n \cdot \nabla \underline{v}_n + \frac{1}{\rho}\nabla p = \frac{\eta_n}{\rho_n}\nabla^2 \underline{v}_n - \frac{\rho_s}{\rho_n}\, s\nabla T - A\rho_s w^2 \underline{w} \qquad (7b)$$

In terms of this mutual friction, the coefficient b is found to be independent of the size and shape of the channel, and, in the case of pure counterflow, is given by

$$b = \frac{A\rho_n}{s(\rho_s sT)^3} \qquad (8)$$

This has been verified experimentally for the case of pure counterflow in wide channels (zero net mass flux) over a wide range of conditions. The coefficient A has been measured by Vinen[5] and is found to depend on temperature, but not the geometry of the counterflow channel.

The phenomenological equations of motion, however, as given by (7a) and (7b) do not appear to be quite correct. Experiments measuring temperature differences between the ends of channels in

which $\underline{v}_n$ and $\underline{v}_s$ could be varied independently of each other and of the heat flux show that any friction in the two fluids cannot be simply expressed as a function of the difference between the two velocities[6]. The dissipative mechanisms appear to be more complicated than mutual friction. Furthermore, equations (7a) and (7b) do not appear to be complete, since they predict a pressure gradient along the length of a tube, at steady state, given by,

$$\begin{aligned} \nabla p &= \eta_n \nabla^2 \underline{v}_n \\ &= \eta_n \nabla^2 \frac{q}{\rho s T} \end{aligned} \tag{9}$$

whereas direct measurements of pressure differences between the ends of channels indicate a more complicated dependence on the heat flux, for values of the heat flux in excess of a critical value[7].

Attempts to reconcile with these difficulties have been made by appending more friction terms in the equations of motion, depending on only $\underline{v}_n$ or $\underline{v}_s$ (see, for example, Atkins[8]). The situation, however, is far from satisfactory, since neither the processes which give rise to the dissipative mechanism, nor their analytical form is clear or, apparently, universal. Yet the fact remains that the Gorter-Mellink force describes a law for the heat transfer process in wide channels in pure counterflow. Should it be appended to the equations of motion? If, indeed, it is a volume friction term, its effect should also be detectable away from any solid boundaries in the free fluid. To investigate

this question, the following experiment was undertaken.

It was observed by Kapitza[9] that a well-defined jet emerges from the mouth of a counterflow channel that persists for many channel diameters in the free fluid without appreciable spreading. The two-fluid model would identify the effluent with the heat-convecting normal fluid which separates at the channel exit like a classical fluid. In this experiment this was verified by observing the deflection of the free surface of the liquid over the opening of a vertical channel (see figure 1.1). This arrangement creates a well-defined counterflow in the absence of any walls. The temperature along the axis of the channel, both inside and in the jet, was measured by means of a single thermometer mounted on a traversing assembly. This was done at various temperatures and counterflow heat fluxes for two different channels.

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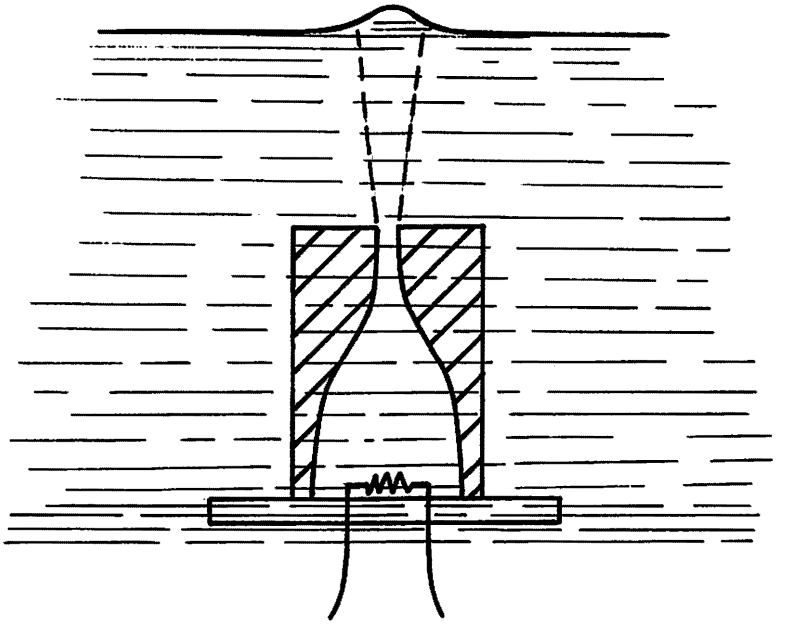

Figure 1.1 Free surface deflection by counterflow jet.

II. The Apparatus.

(i). Geometry.

Two different flow channels were used (figures 2.1 and 2.2). Machined out of plexiglas, they were shaped in such a way as to confine the region of high relative velocities and resulting temperature gradients to a small part of the channel away from the heaters. The heater, in each channel, was constructed with 0.005" Evanohm wire potted in Wood's metal to ensure uniform distribution of heat at the bottom of the channel. The thickness of the channel walls kept heat losses through heat conduction under 1% of the total heat input.

(ii). Sensors.

The bath temperature during the measurement was monitored and recorded by sensing the vapor pressure at the top of the cryostat with a 100 mmHg F.S. Barocel transducer. Bath temperature could be set and maintained, to within limits that depended on the heat input to the channel heater, with a condom pressure regulator. The temperature versus position along the channel axis was sensed by a carbon thermometer motorized with a variable speed, reversible D.C. motor. This was enclosed in the cryostat and situated at the top at room temperature. The shaft of this motor wound and unwound a nylon thread from which the traversing

MODEL I

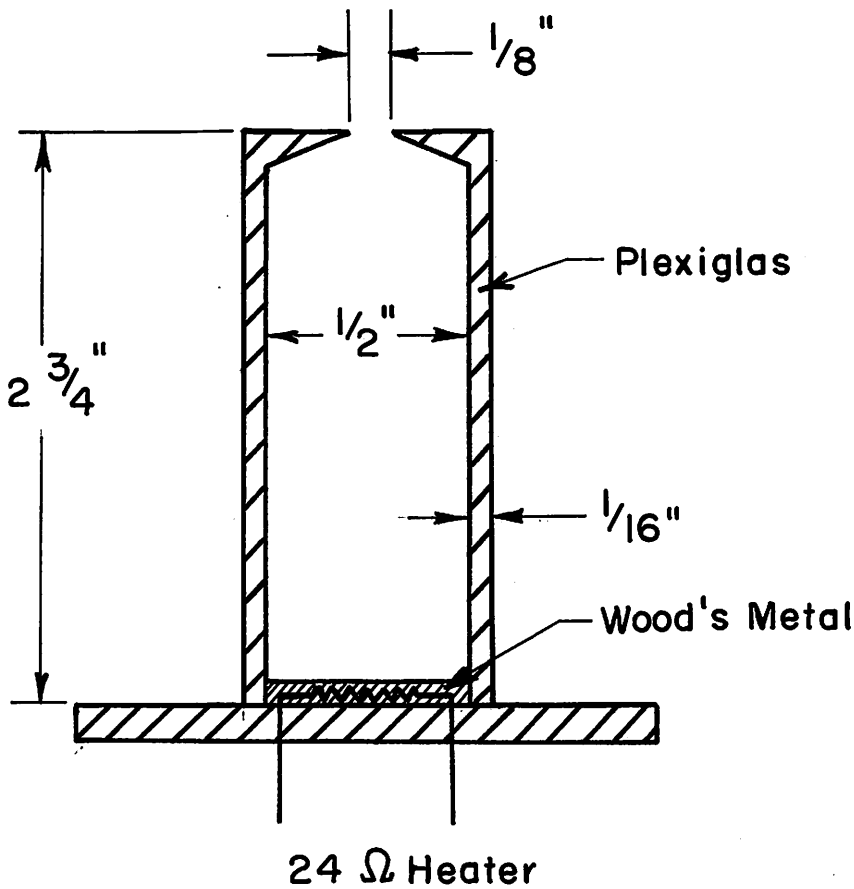

Figure 2.1 Orifice counterflow channel.

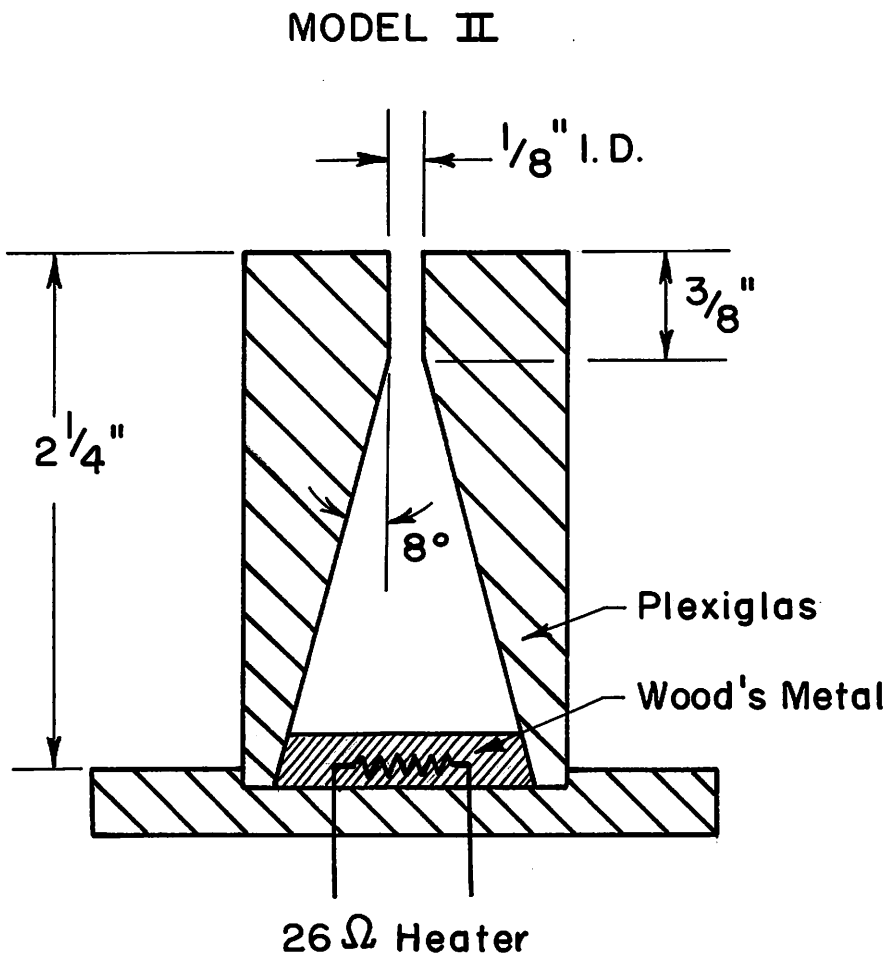

Figure 2.2 Constant area counterflow channel.

thermometer assembly was suspended. An optimum volume of approximately 1.5×10^{-5} cm^3 was selected for the thermometer tip as a compromise between signal-to-noise ratio which decreased with decreasing size and obstruction to the flow which had to be minimized. It was shaped under a microscope to resemble a cube, approximately 0.010" on the side. Two 0.001" enameled copper wires whose insulation was sanded off the ends were bonded on opposite faces of the cube with conducting silver paint. These wires were threaded through a 3 mm glass tube drawn to a 0.010" capillary 3" long and provided the mechanical support and electrical connections to the sensor. See figure 2.3. The glass tube was fitted to a stainless steel thin-walled tube inside a soft iron tube, and moved inside a stationary plexiglas tube with a 3" long coil wound on the outside using 0.010" magnet wire. The inductance of this coil, a function of the position of the soft iron core, was sensed as a means of measuring the position of the thermometer. The whole assembly could be aligned with the channel axis by means of two sets of three set-screws 120° apart. See figure 2.4.

(iii). Instrumentation and calibrations.

The 100 mmHg F.S. Barocel transducer was coupled to a 1014 Barocel Electronic Manometer whose 0.0 to 10.0 Volt F.S. linear output was multiplexed by means of an Analog Channel Selector (ACS) into a six-digit HP3450A Integrating Digital

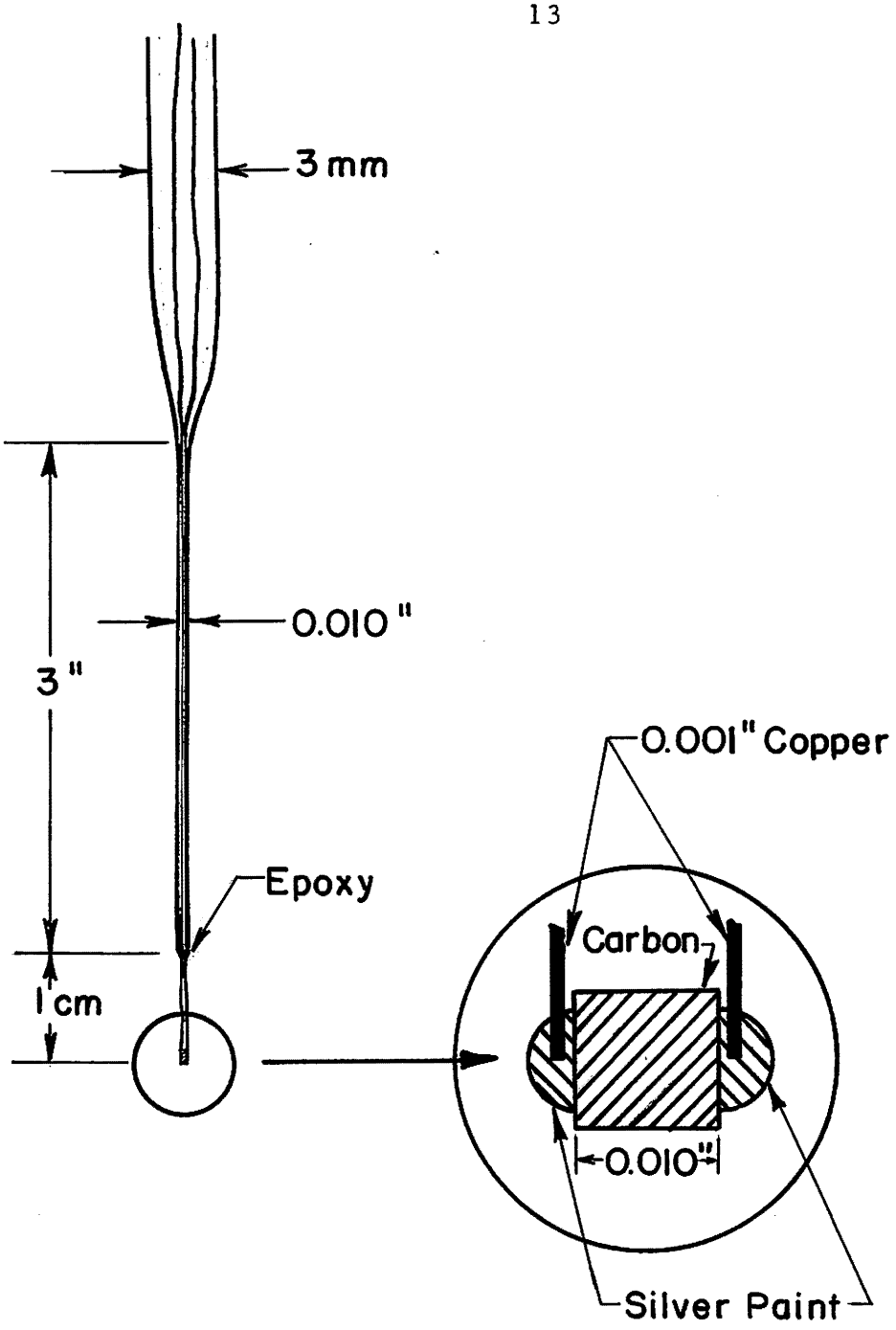

Figure 2.3 Temperature sensor.

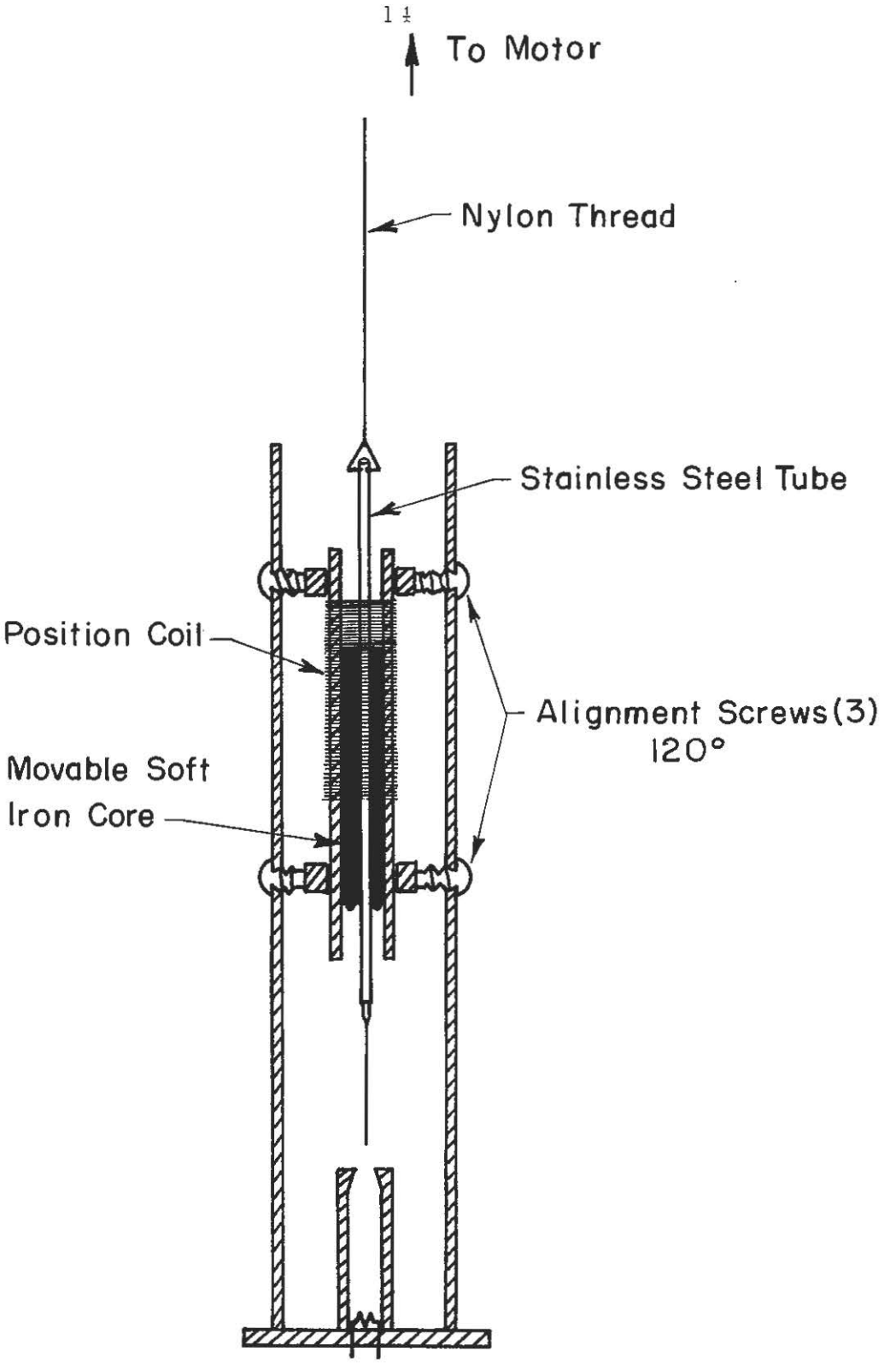

Figure 2.4 Thermometer assembly and counterflow channel.

Voltmeter (DVM). See figure 2.5. The resistance of the channel thermometer was measured by sensing the resistive voltage drop across the carbon tip with a 1.5 kc reference current with a PAR HR-8 Phase Locking Amplifier (PLA-I), whose linear output of -10.0 to +10.0 Volts was also multiplexed into the DVM. Power dissipation in the sensing element was kept under 10^{-8} W in order to minimize any temperature differences between the carbon tip and the surrounding liquid. Calibration of the thermometer was easily carried out before each run by multiplexing between the Barocel Electronic Manometer and PLA-I, as the bath temperature was allowed to drift slowly.

The inductance of the position sensing coil was measured on a second Phase Locking Amplifier (PLA-II) by observing the inductive voltage drop across the coil with a 30 kc reference current. Linearity was better than 0.1% over the traversing range of interest. Calibration was realized by noting the output of PLA-II versus measurements of the position of the temperature sensing tip with a cathetometer form the outside. The procedure yielded an absolute accuracy of the order of 0.01 cm with respect to the channel exit, as limited by the cathetometer readings through the two vessels. Note that possible stretchings of the nylon thread do not affect the accuracy of the position measurement, since the sensing is realized at the bottom of the dewar with a device that is integrally connected to the temperature sensing tip. The output of PLA-II was also multiplexed into the DVM.

Finally the voltage drop across a 100 ohm resistor, in series with the channel heater, was also multiplexed as a fourth input into the DVM. This monitored the power driving the counter - flow. The heater current was supplied by a Hewlett - Packard 6201B regulated power supply.

The Analog Channel Selector (ACS) utilized gold contact, sealed relay switches for both signal and ground to avoid common - mode errors and cross - talk between the channels. The four inputs were selected in sequence by the programming logic and connected to the guarded input of the DVM. No measurable contact noise or bias originating in the Analog Channel Selector was detectable on the DVM (1μV resolution). A description of the ACS unit appears in Appendix 1.

The 32 - bit output of the DVM was formatted into four 8 - bit characters (bytes) and written on a 9 - track, 800 BPI Kennedy 1600/360 Incremental Tape Recorder by a Coupler (CPL) described in Appendix 2. The tape was read on an IBM 360/75 to process the data and plot the results.

An X - Y plotter, connected to the inputs during each run, provided real - time monitoring of the data and an additional check on the computer processed results. A block diagram of the instrumentation package appears in figure 2. 5.

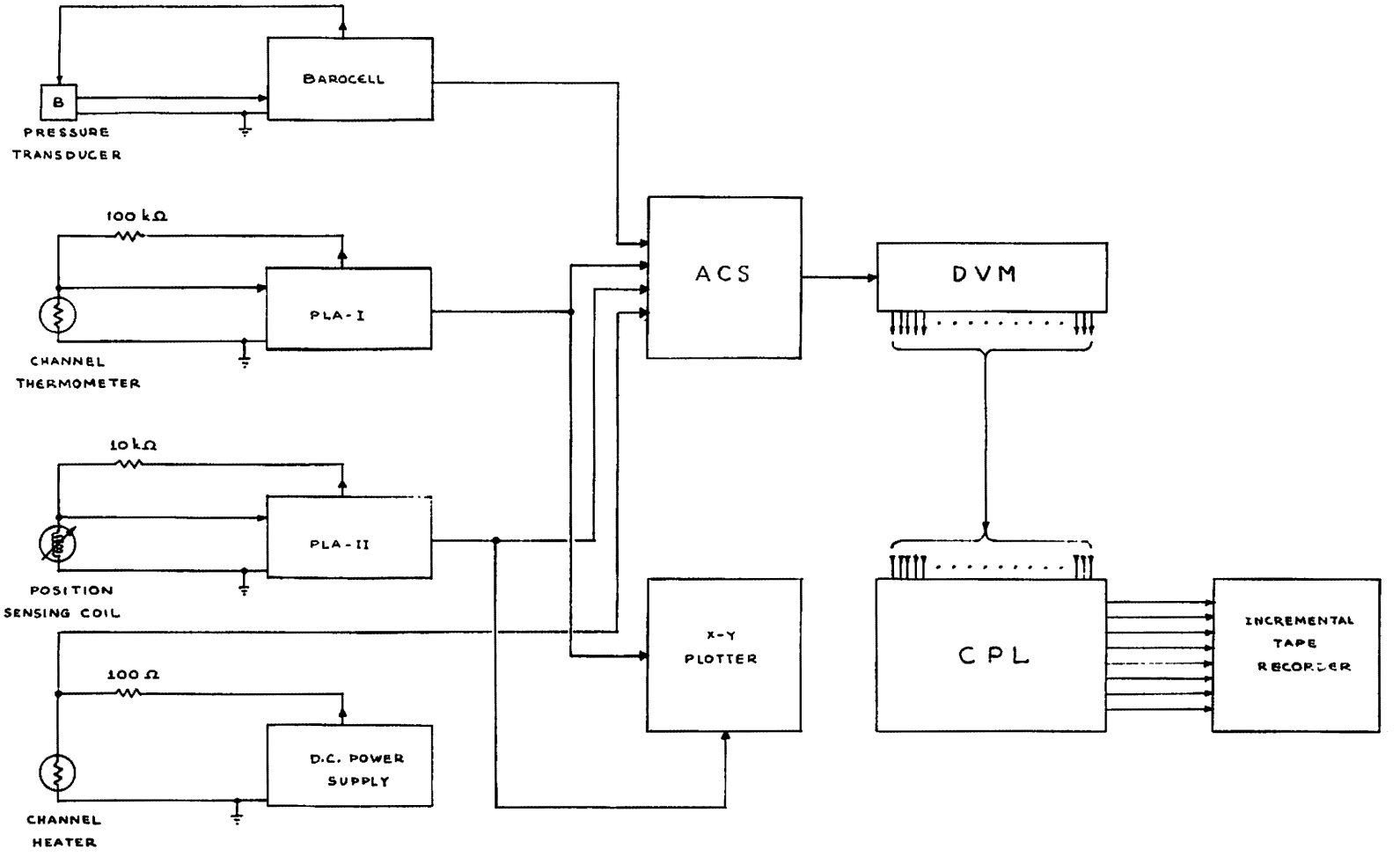

Figure 2.5 Instrumentation

III. Experimental Procedure.

The bath temperature was set to the desired value by means of the condom regulator and a trial traverse was made using the highest anticipated heat flux, as limited by cavitation[1] at the bottom of the channel, to determine the range of the output of PLA-I (channel thermometer sensing amplifier). This output was then calibrated versus vapor pressure, in a quiescent bath, by multiplexing between the Barocel output and PLA-I while the bath temperature was allowed to drift to cover the anticipated range. This calibration was recorded in one tape record on the incremental tape recorder in the manner described above. Sample calibration data are plotted on figure 3.1. Two traverses, one in each direction, were then made for each value of the heat flux. The voltage outputs from the Barocel, PLA-I, PLA-II, and heater current sensing resistor (100 ohms) were recorded in sequence (75 ms apart) at sampling intervals ranging from 0.5 s to 1 s depending on the rate of traverse and consistent with the 300 ms integrating times on the Phase Locking Amplifiers, as the thermometer traversed slowly. The data recorded in each traversing direction constituted one record on the tape. At the end of each tape file consisting of all the data taken at that temperature the output of PLA-II (position sensing amplifier) was calibrated versus position by means of a cathetometer. The data for this calibration were punched on computer cards that were submitted and processed with the tape. Parabolic least-squares fit were used to express

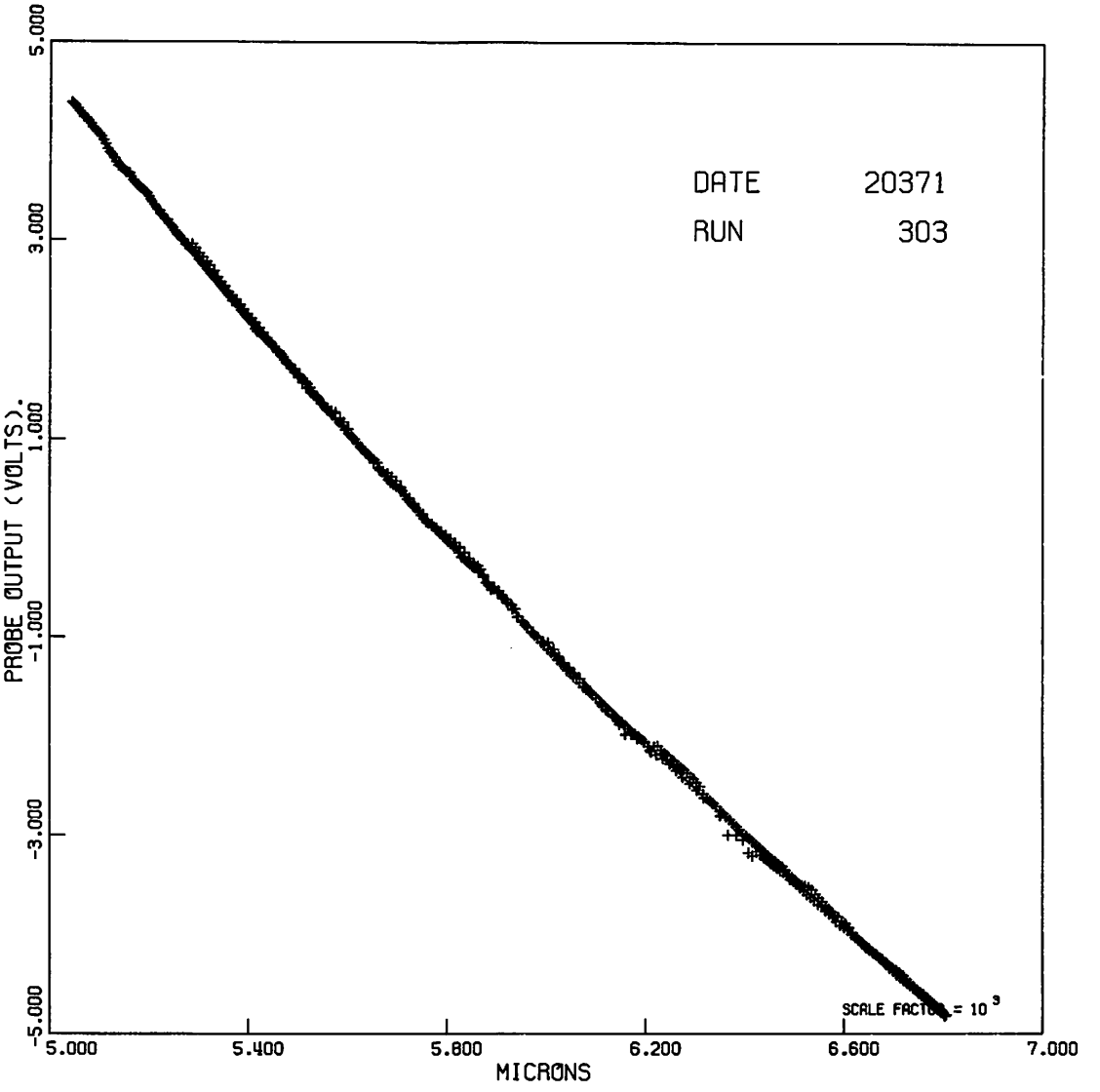

Figure 3.1 Probe Calibration in the Temperature Interval 1.571°K to 1.649°K.

in analytical form the PLA-I versus pressure and PLA-II versus position calibrations. The conversion from vapor pressure to degrees Kelvin was through an Aitken third order interpolation on the NBS 1958 He^4 temperature scale. Thus, the bath temperature, the channel temperature and the heater power could be calculated for each position x of the channel thermometer. At the power levels that were used to drive the counterflow small fluctuations in the vapor pressure regulating system necessitated computing the difference between the channel temperature and the simultaneous bath temperature. This difference was then added to the average bath temperature during the traverse. Sample data are plotted in figures 3.2, 3.3, and 3.4. The continuous line on figure 3.4 consists of straight line segments connecting 182 data points. The abscissa is scaled in centimeters along the channel axis as measured from the channel exit. Positive values of x correspond to positions in the jet. Negative values of x correspond to the interior of the channel. The ordinate is scaled in degrees Kelvin.

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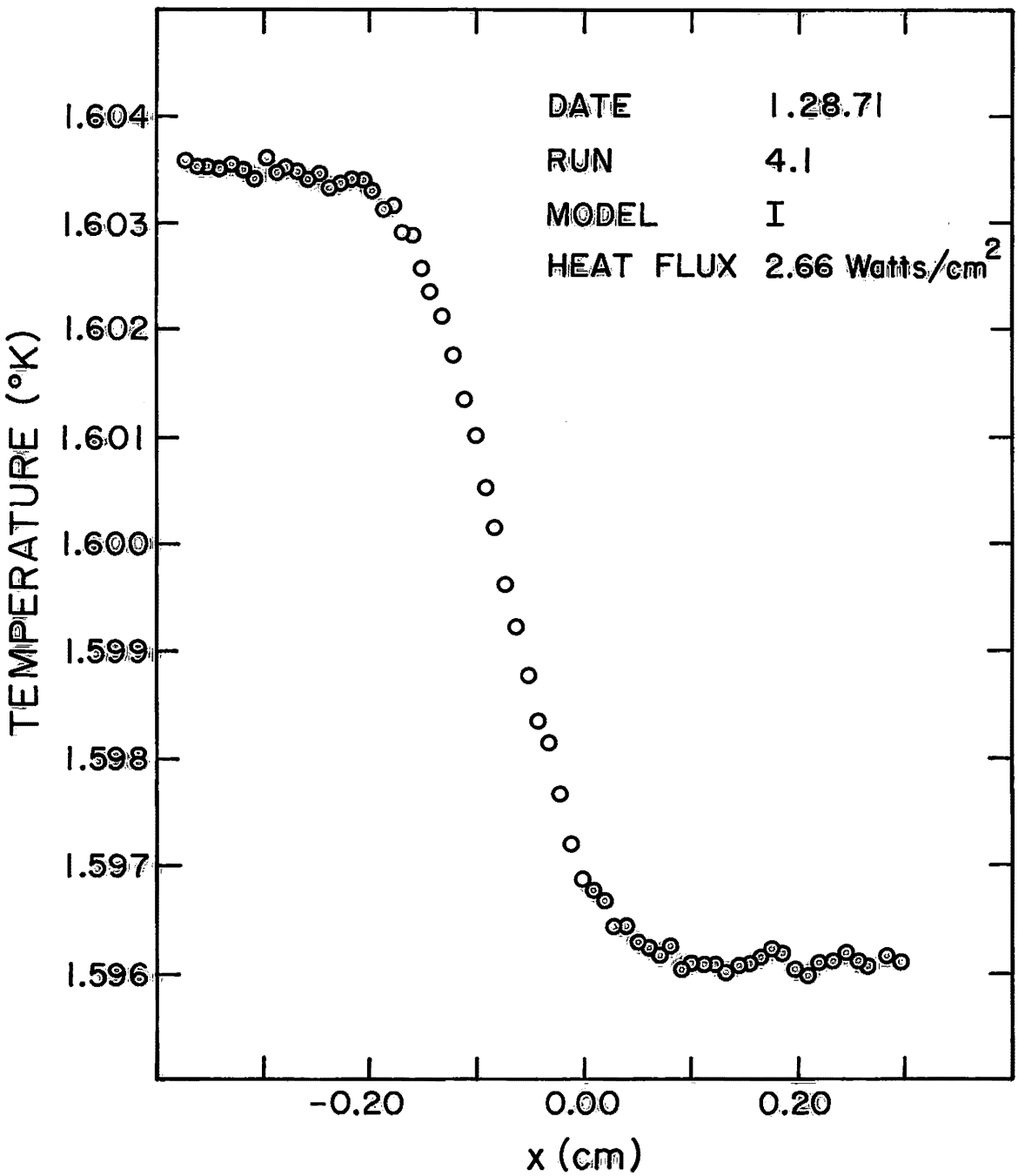

Figure 3.2 Temperature Field at 1.60°K

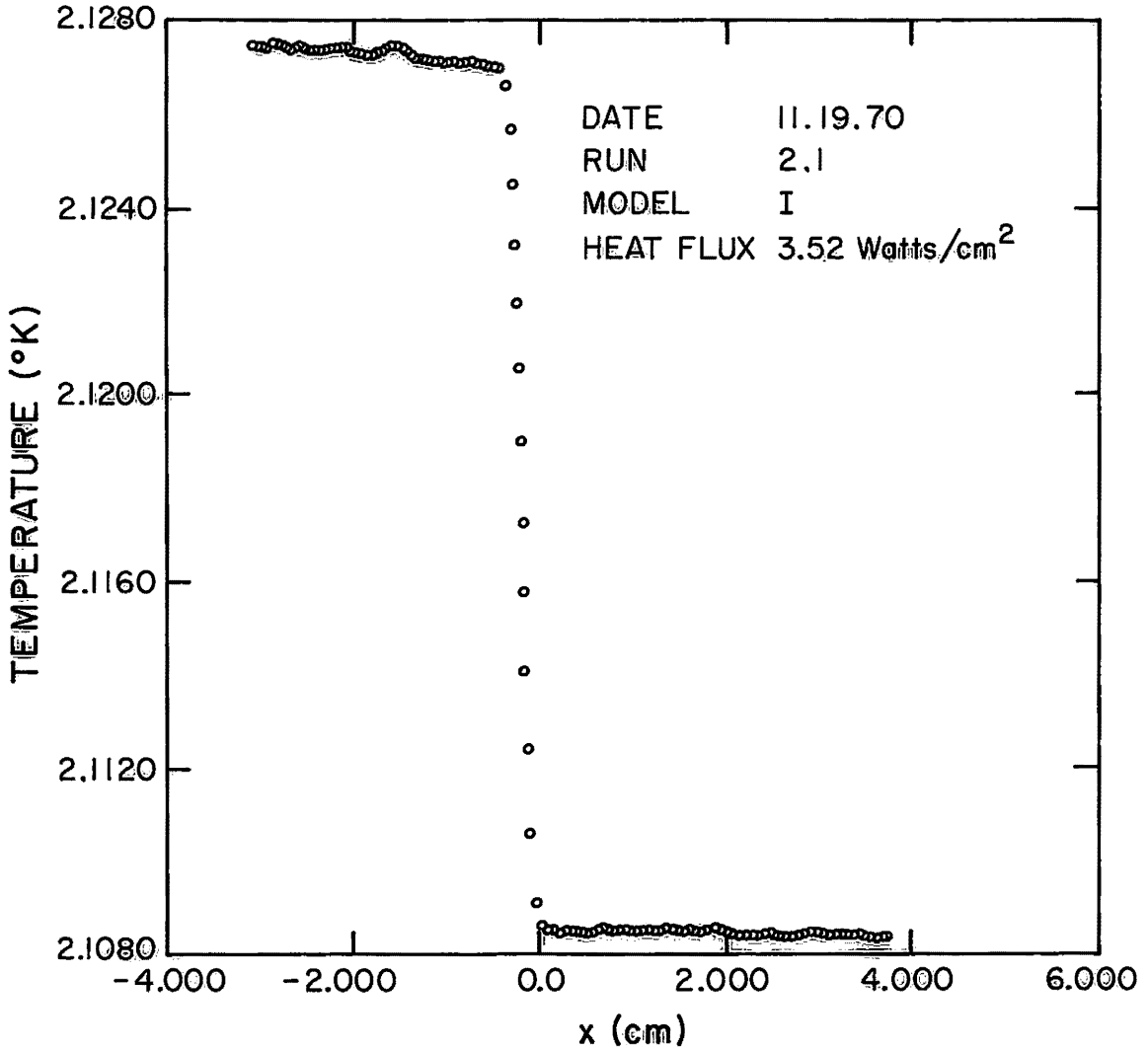

Figure 3.3 Temperature Field at 2.11°K

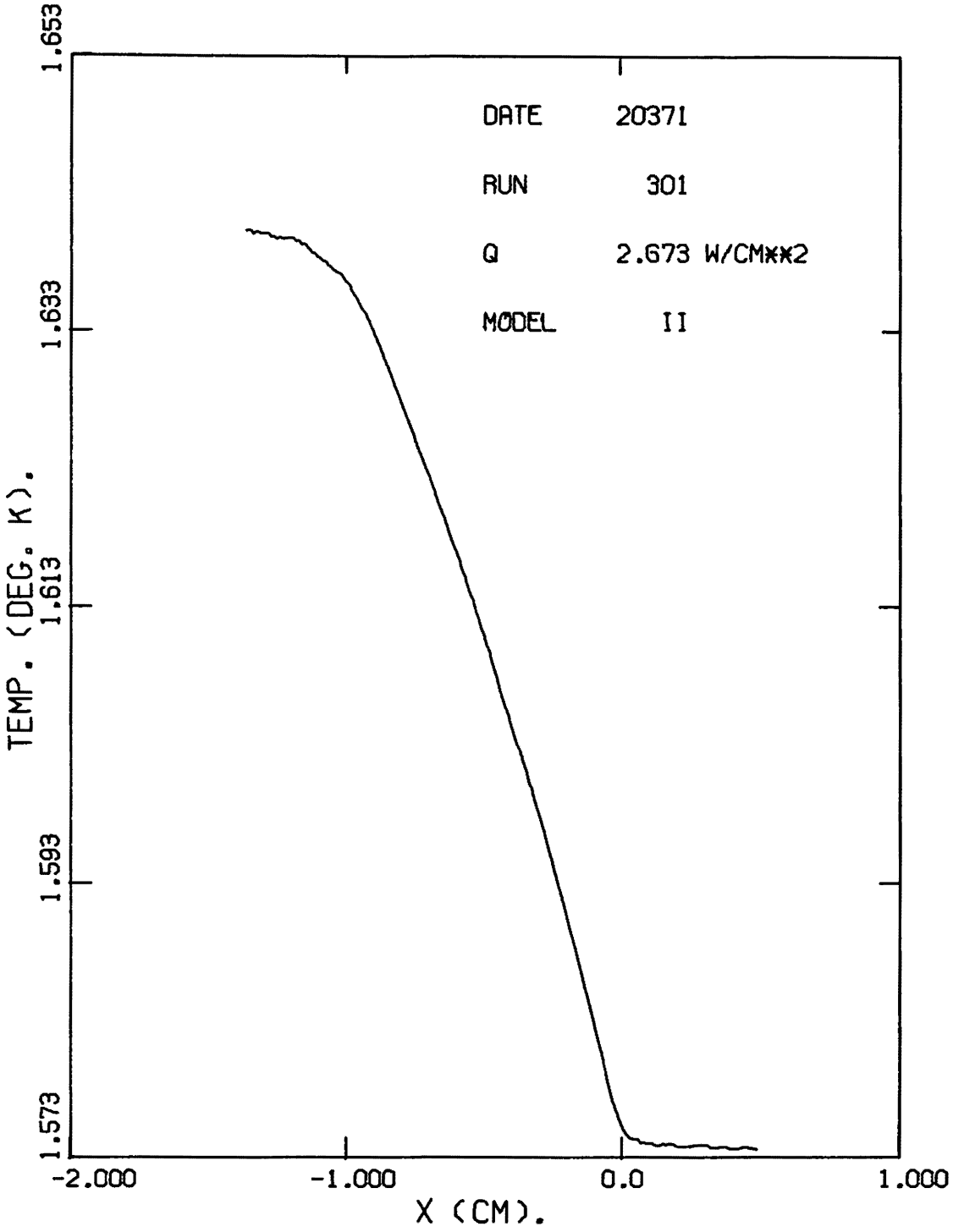

Figure 3.4 Temperature Field at 1.6°K.

IV. Results and Discussion.

Qualitatively, the most striking feature of the temperature measurements in this experiment is the absence of a temperature gradient outside the channel, as can be seen from the data in figures 3.2 and 3.3. In this region, the deviations of the resistance of the traversing thermometer from a constant value are random and reflect the low frequency noise spectrum that characterized the small carbon thermometer. The gradient that is found in the interior of the channel disappears in the free jet within, at most, one channel radius from the channel exit. This fact has to be reconciled with the presistence of the normal fluid jet for several channel diameters into the free fluid.

According to the Gorter-Mellink term, the disappearance of the temperature gradient implies the disappearance of the relative velocity between the two fluids. In the language of fluid mechanics, the normal fluid jet must entrain the superfluid. There are two reasons why this is an unlikely possibility. The first reason is the fact that the gradient is already zero within a radius from the channel exit. That would imply a stagnation point for the superfluid very close to the exit of the channel, with a bizarre resulting flow and pressure field in its vicinity. The second reason is that the temperature field remains self-similar, as will be shown later, for a range of superfluid flow velocities of three orders of magnitude. That would imply that a slow normal fluid jet and a fast normal fluid jet would be capable of reversing the

direction of the superfluid flow within the same distance from the exit of the channel. It is therefore unlikely that the relative velocity changes in any drastic way in the vicinity of the exit.

These considerations suggest that the Gorter-Mellink term turns itself off in the region outside the channel. Since the only distinguishing feature, as far as the flow is concerned, between the channel interior and the channel exterior in the vicinity of the exit, is the presence of the channel walls, the conclusion that the boundary conditions are essential to the mutual friction mechanism appears to be natural.

It should be noted that this is at variance with Vinen, who concluded "that the boundaries of the channel carrying the heat current play no essential role in the build-up, maintenance and decay of the Gorter-Mellink force"[1]. Theoretically the form of the Gorter-Mellink term yields results independent of the channel geometry, e.g., equation (8), and experimentally the temperature gradient along the heat transfer tube was found to be unaffected by the addition of obstructions along the length of the channel that do not seriously alter the channel cross section[2]. This observation led Vinen to the postulation that the mutual friction would take place in a "volume of helium of infinite extent carrying a homogeneous heat current"[1]. The proposed mechanism by Hall and Vinen[3], following a picture suggested by Feynman[4], for the friction between the two fluids is the scattering of the elementary excitations, that constitute the normal fluid, on the core of the quantized vortex lines that exist in the super fluid. In this

model, the super fluid is viewed as in some sort of homogeneous turbulent state which is generated when the super fluid velocity, relative to a solid boundary, exceeds a critical value.

It is easy to see, however, that such a picture cannot explain the present experimental data. Since the counterflow in the free jet can be considered "a volume of helium of infinite extent carrying a homogenous heat current," the vanishing of the temperature gradient there is inexplicable in those terms. Even if the assumption is made that this turbulent state of quantized vortex lines is initiated at the channel exit and is convected with the super fluid down the channel, we cannot explain why the temperature gradient extends even by one radius beyond the channel exit. Something analogous to the inlet length of classical pipe flow corresponding to a potential core for the incoming fluid would have been observed. The idea of an inlet length was considered by Vinen[5] on the basis of characteristic times which he measured for the buildup of the dissipative mechanism. Reasoning by analogy to classical boundary layer theory, he estimated an inlet length for the process given by the product of the flow velocity and the delay times he measured. He was forced to conclude from his own data, however, that any length computed on such a basis would be too large. The conclusion that is borne by the present data is that even the notion of an inlet length is inaplicable to the phenomenon; the temperature gradient would have vanished in the interior of the channel and not have extended at all in the jet.

The behavior, however, in the interior of the channels appears to be consistent with the predictions of the Gorter-Mellink term. This can best be seen in the data from model II.

From the equations of motion, with the Gorter-Mellink term appended, we have in the case of one-dimensional pure counterflow at high heat fluxes,

$$-s\frac{dT}{dx} = A\rho_n\left[\frac{q(x)}{\rho_s sT}\right]^3 \tag{10}$$

or

$$\frac{dT}{dx} = -b(T)\,q^3(x) \tag{10a}$$

where

$$b(T) = -\frac{A(T)\rho_n}{s(\rho_s sT)^3} \tag{8}$$

is a universal function of T, independent of geometry and boundary conditions (see figure 4.5).

It should be emphasized that the Gorter-Mellink law yields two independent predictions. One is that at any point in a given counterflow channel, held at a fixed temperature, the temperature gradient would be proportional to the cube of the local heat flux, and two, that the constant of proportionality, b(T), is a universal function of temperature.

The apparent "deviations" from the cubic law which are characteristic of experiments that measure temperature differences between the ends of a long tube as a function of the applied heat flux, are to be understood in terms of the temperature dependence

of b(T). This becomes apparent from the data taken from model II.

Within the constant area section of model II, q(x) is constant and equal to the value at the exit (x = 0). Therefore, if

$$q^* = q(0)$$

we have

$$\frac{1}{q^{*3}} \frac{dT}{dx} = - b(T)$$

If this is indeed a local law we should be able to observe a change in b(T) within the temperature interval that appears between the ends of the constant area section of model II. b(T) is found to decrease rapidly as T increases up to around 2.0°K and then increases very rapidly as T_λ is approached. A close look at figure 3.4 shows a systematic change in the slope dT/dx as a function of temperature. To check this, measurements in the constant area section of model II were fitted with a quadratic to obtain both the derivative dT/dx and the change in the derivative which gives db(T)/dT . Three such fits are plotted from data at 1.3°K, 1.4°K, and 1.5°K on figures 4.1, 4.2 and 4.3. From the quadratic fit, b(T) is then calculated at sixteen points as a function of T within the interval covered by each run. The results are plotted on figure 4.4. It can be seen that the measurements are consistent with each other, in as much as the smooth line that joins the three runs is consistent with the estimates of b(T) for the three intervals. It should be emphasized

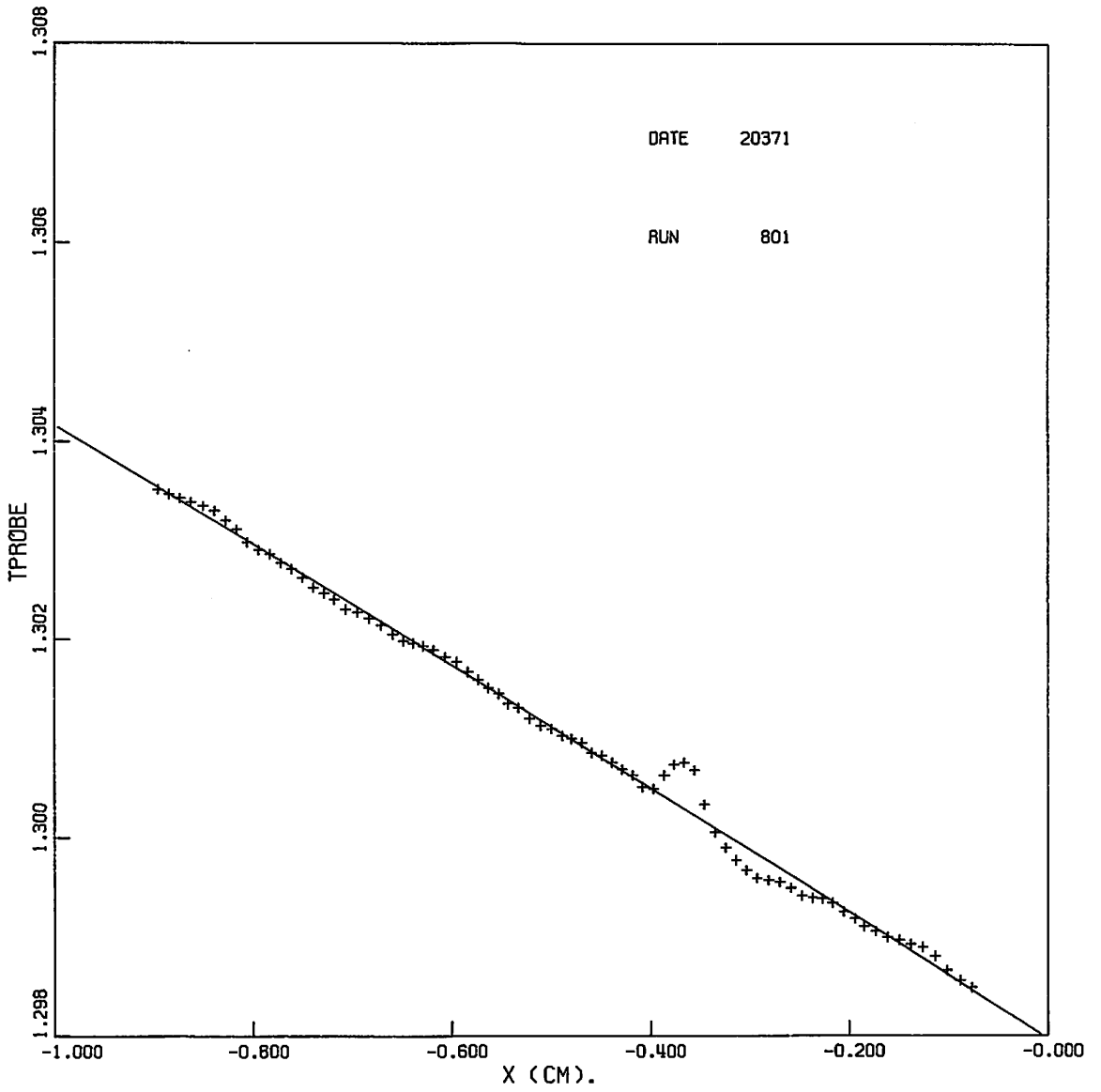

Figure 4.1 Model II Data. $q = 0.46\ W/cm^2$

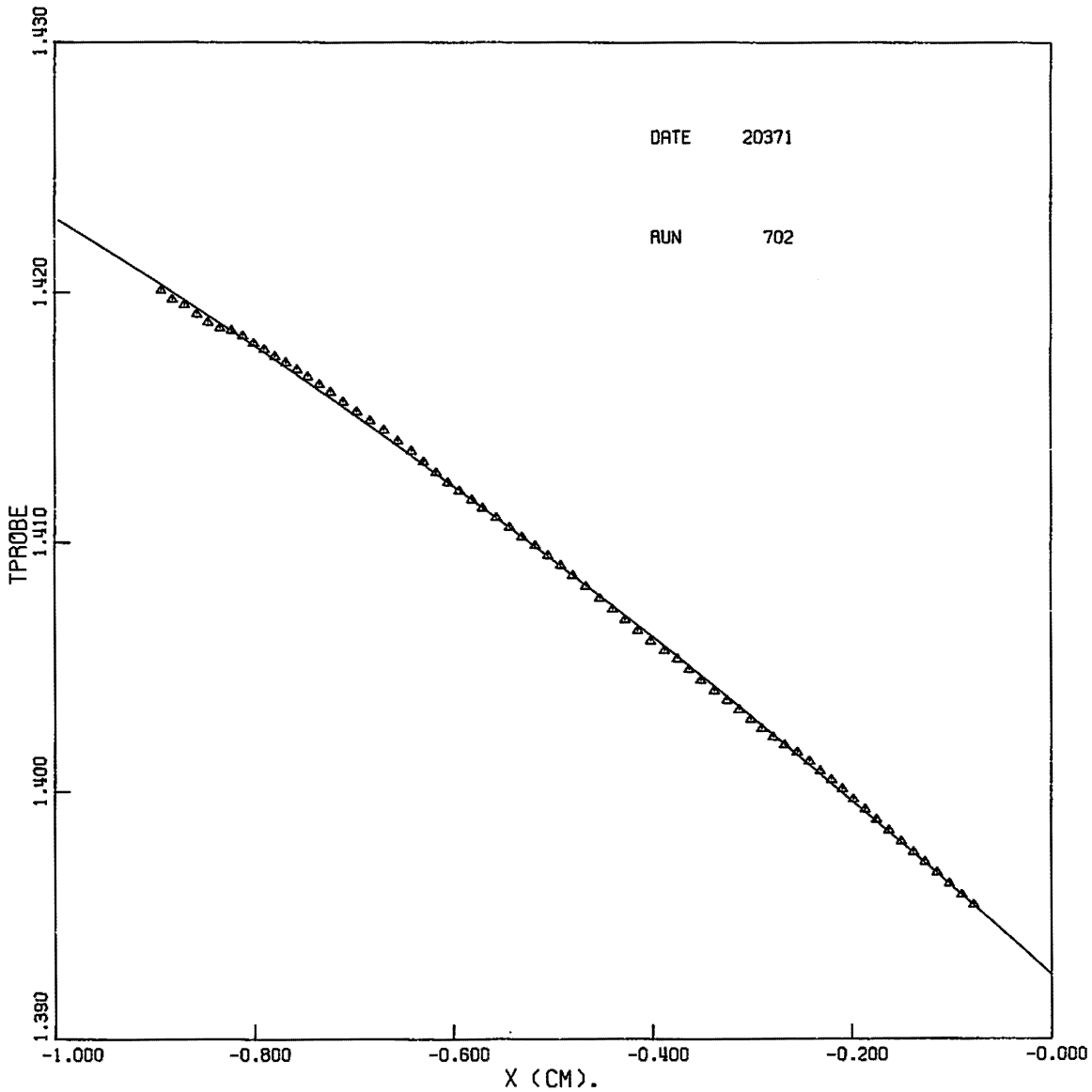

Figure 4.2 Model II Data. $q = 1.14\ W/cm^2$

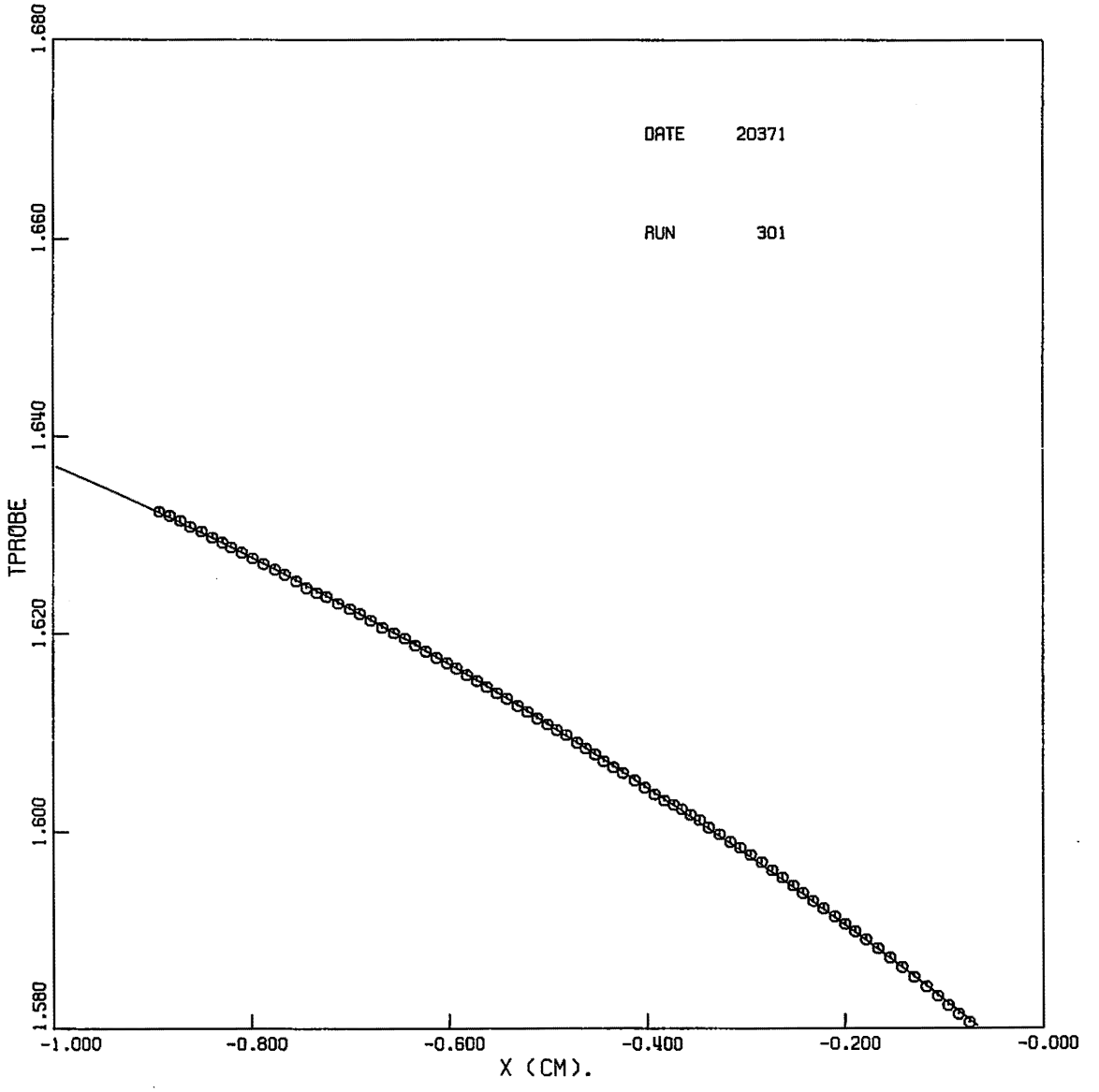

Figure 4.3 Model II Data. $q = 2.67\ W/cm^2$

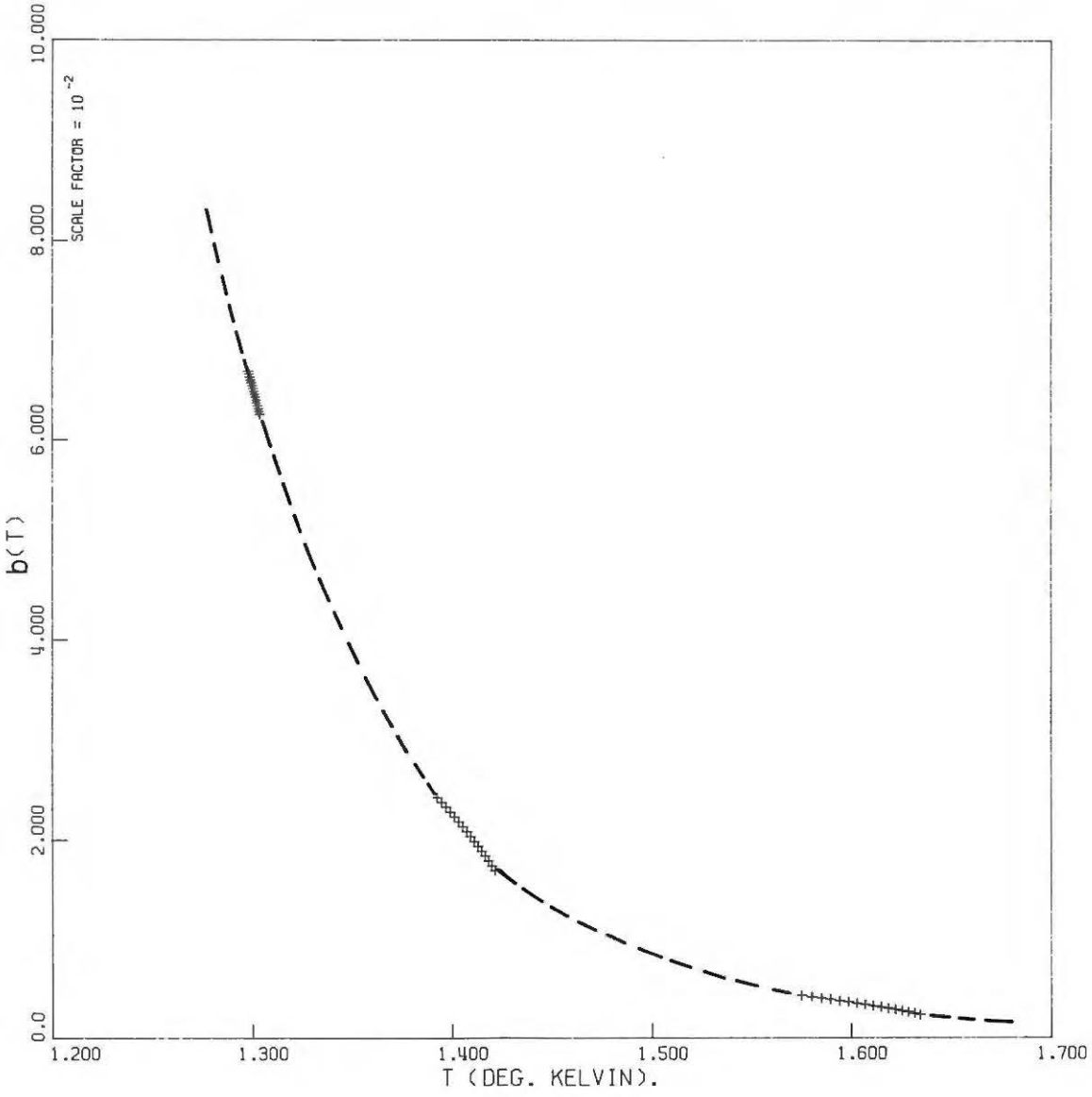

Figure 4.4 b(T) Calculated From Three Runs of Model II.

that in this way both $b(T)$ and $\frac{d}{dT} b(T)$ are determined in a constant area channel 3/8 of an inch long. The curvature of the estimates is seen to be in error since that would correspond to the third derivative of the data, which cannot be calculated from the quadratic fit. Higher order fits would have required a longer constant area section.

These data and data from model I are compared to those of Vinen[2] and Broadwell and Liepmann[6] on figure 4.5. It can be seen that the data from model II and those of Vinen agree very well with each other. It can be seen that $b(T)$ as deduced from the data from model I is systematically lower than the measurements of Vinen and those from model II. In the case of model I, $b(T)$ was calculated by dividing $(dT/dx)_{max}$ for each traverse, by q^{*3}. As can be seen from figure 3.2, the maximum gradient does not occur at the orifice but approximately half a millimeter inside the channel where the heat flux is probably a little smaller. The differences of the order of 10% which arise are probably attributable to this effect.

The data from model I, however, can be used to check the predictions of the Gorter-Mellink law in a different manner. To do this we must first show that the scaled temperature profile,

$$\theta(x) = \frac{T(x) - T_{bath}}{\Delta T}$$

where ΔT is the difference in temperature between the interior and the exterior, is independent of T_{bath} and q^*.

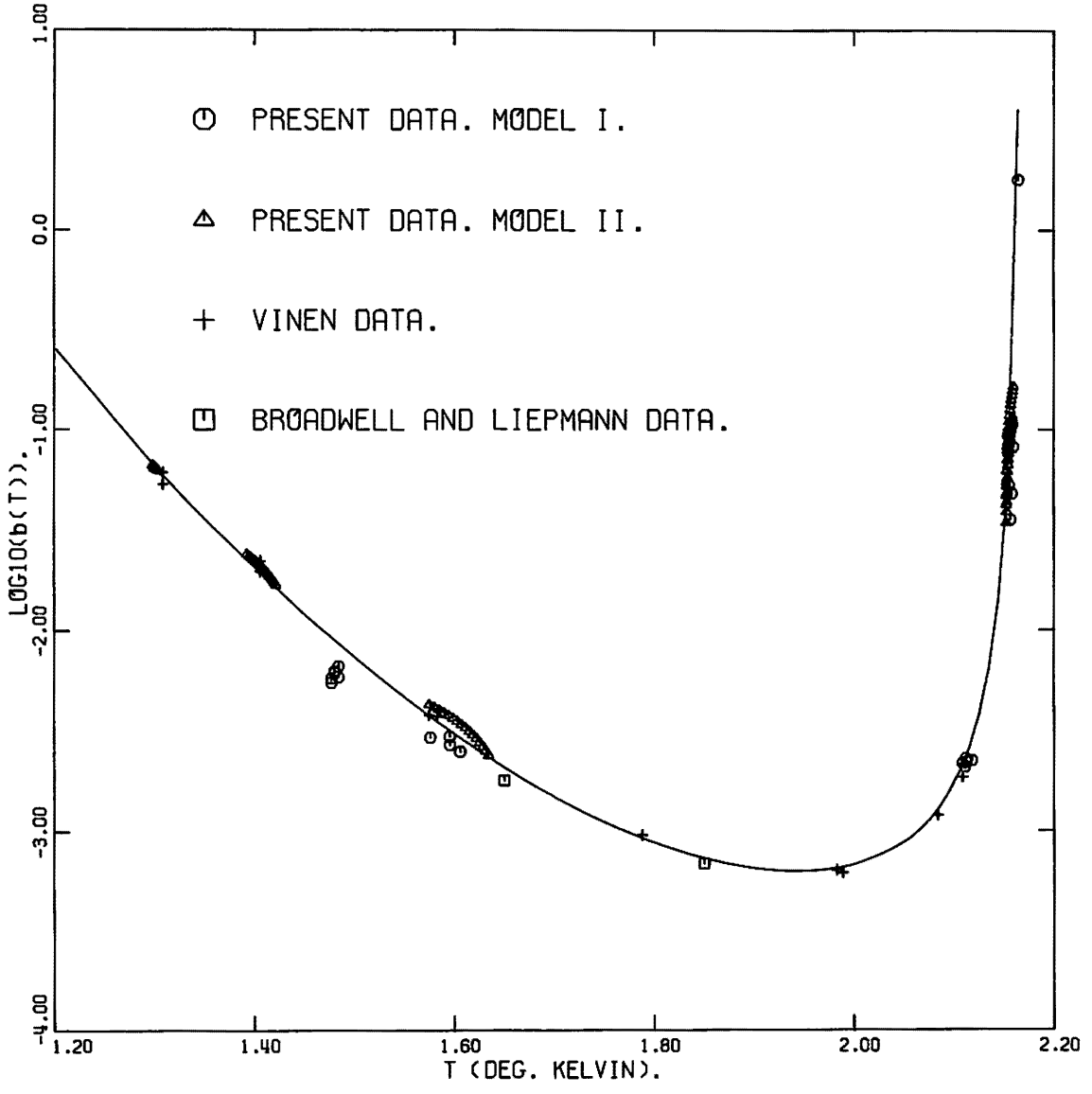

Figure 4.5 The Universal Function b(T).

Equation (10a) can be separated to give

$$\frac{1}{q^{*3}} \frac{dT}{b(T)} = - \left[\frac{q(x)}{q^*}\right]^3 dx$$

Thus we can integrate from a station x_1 to an arbitrary x to obtain

$$\frac{1}{q^{*3}} \int_{T(x_1)}^{T(x)} \frac{dT'}{b(T')} = - \int_{x_1}^{x} \left[\frac{q(x)}{q^*}\right]^3 dx \qquad (12)$$

By the mean value theorem,

$$\frac{1}{q^{*3}} \int_{T(x_1)}^{T(x)} \frac{dT'}{b(T')} \simeq \frac{1}{q^{*3} b(T)} \int_{T(x_1)}^{T(x)} dT'$$

$$= \frac{T(x) - T(x_1)}{q^{*3} b(T)}$$

where

$$T(x_1) < T < T(x)$$

If x_1 is a station in the free fluid and we integrate to a station x_2 in the interior of the channel we obtain

$$\frac{T(x_2) - T_{bath}}{q^{*3} b(T)} = \frac{\Delta T}{q^{*3} b(T)} = \int_{x_2}^{x_1} \left[\frac{q(x)}{q^*}\right]^3 dx$$

The integral on the right hand side is a constant with units of length, scaling the transition region in the temperature profile between

the channel interior and the channel exterior. Let,

$$\int_{x_2}^{x_1} \left[\frac{q(x)}{q^*}\right]^3 dx = \ell$$

Therefore

$$\frac{\Delta T}{q^{*3}\, b(T)} = \ell \qquad (13)$$

and

$$\frac{T(x) - T_{bath}}{q^{*3}\, b(T)} \propto \frac{T(x) - T_{bath}}{\Delta T} = \theta(x)$$

To check this, $\theta(x)$ was plotted versus x, for sample runs from model I, on figure 4.6. It can be seen that the similarity that is predicted by the equations of motion is borne by the experiment. We can also use equation (13) to check the dependence of ΔT on q^*. All the data from model I, except one traverse at 2.165°K (see figure 4.5), for which the change in $b(T)$ even within the small ΔT was large, are plotted on figure 4.7. The data have been grouped such that the temperature for each group, rounded off to three significant figures, is the same. This grouping corresponds to the clusters of points that appear on figure 4.5. The constant ℓ turns out to be equal to 0.126 cm. The straight line on figure 4.7 is a plot of

$$\frac{\Delta T}{b(T)} = 0.126\ q^{*3}$$

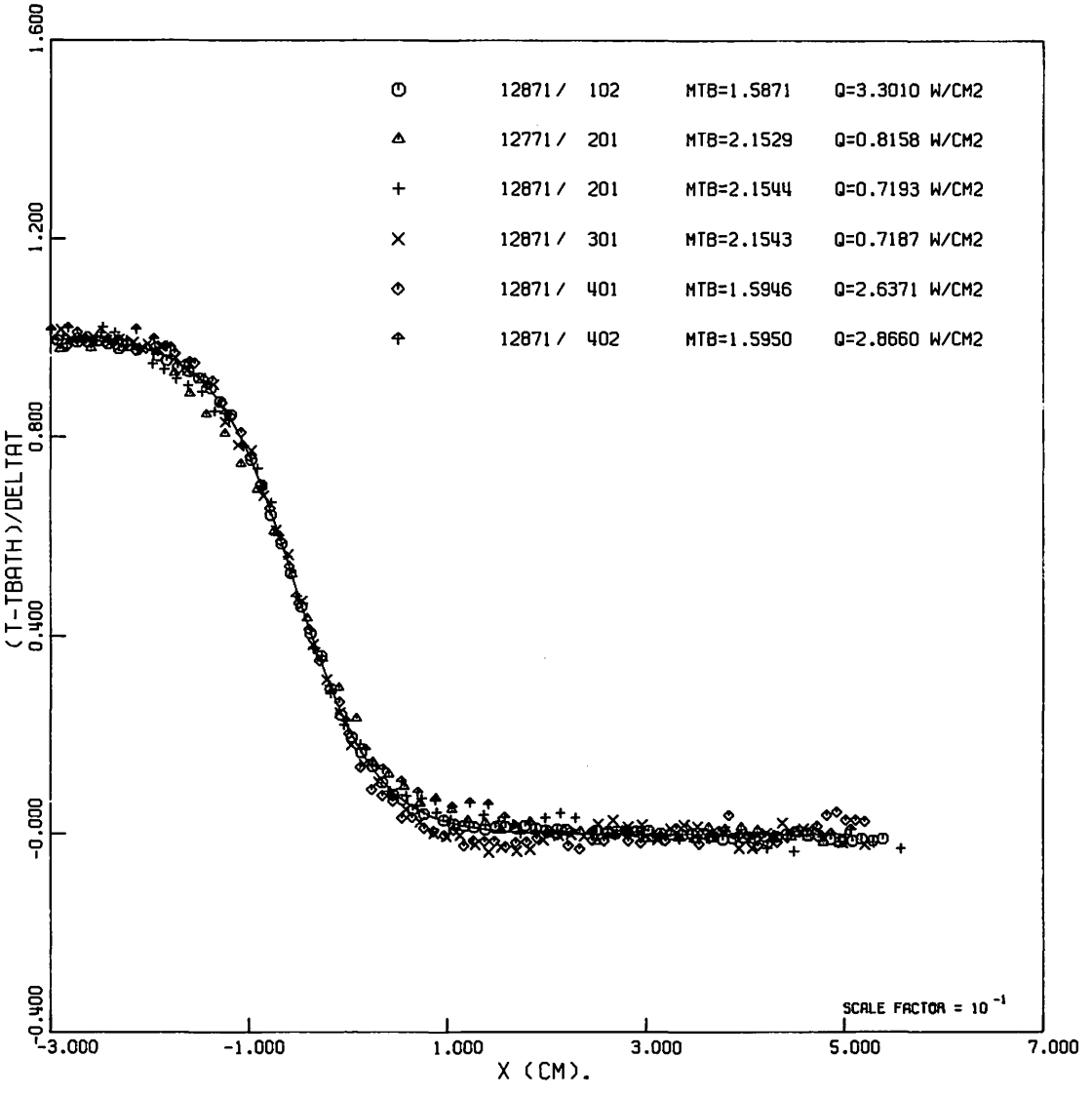

Figure 4.6 Model I Data Similarity.

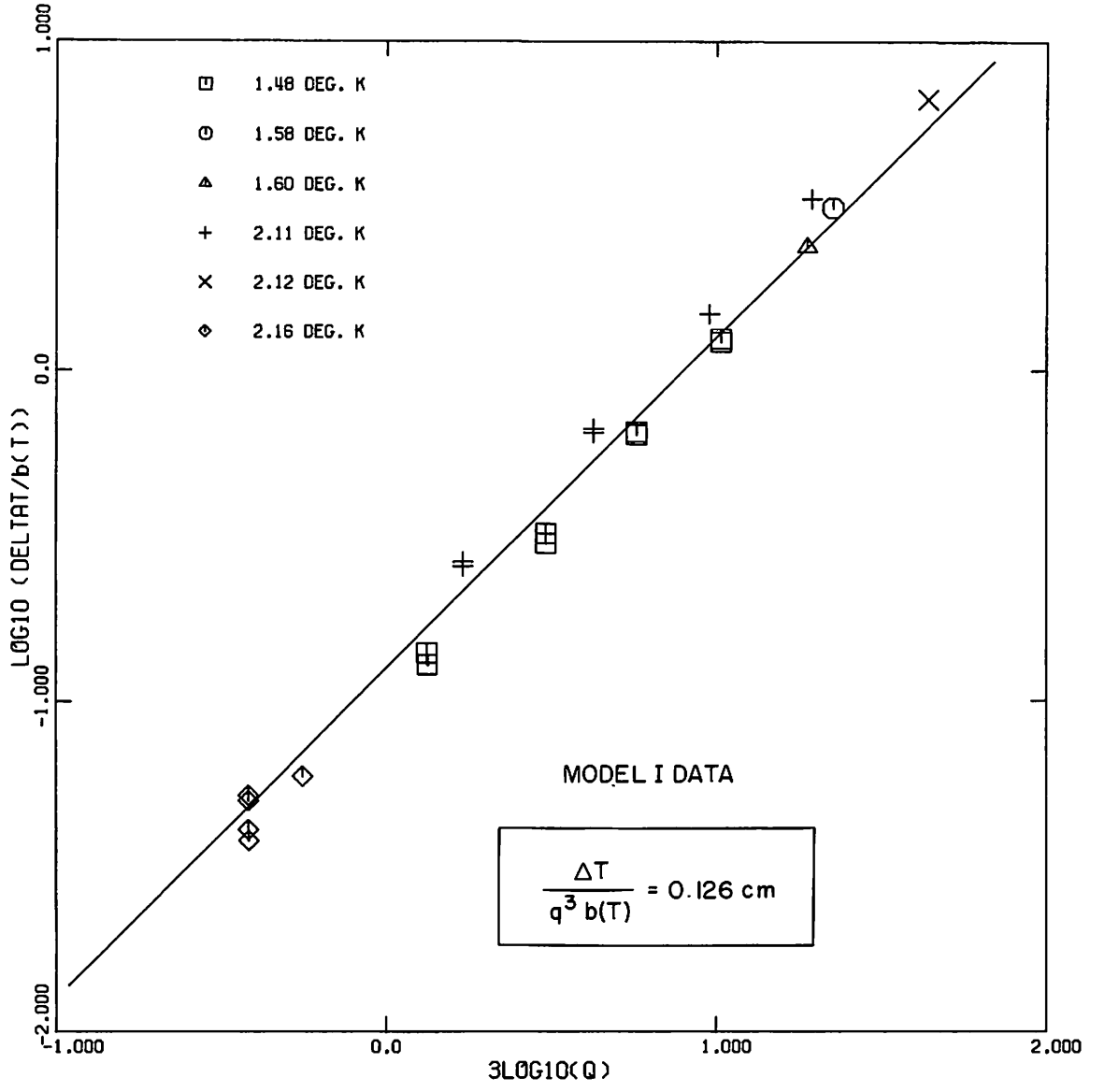

Figure 4.7 Model I Heat Transfer Data.

Error bars are smaller than the size of the symbols. The values of b(T) used to scale the temperature differences are taken from the smooth line on figure 4.5.

The calculation of the Gorter-Mellink constant A(T), from the experimentally determined b(T), on the basis of equation (8), involves the use of the thermodynamic functions for liquid helium and the ratio ρ_s/ρ as a function of temperature. Because errors have been found in the available tables in the literature, the values that were used in this calculation are tabulated in table 4.1. These were determined by requiring that the first differences between the entries, divided by the temperature difference, be a smooth function of temperature. The resulting values of $A(T)_{exp.}$ are plotted on figure 4.8. It can be seen that there exists a strongly divergent regime in the neighborhood of the lamda point that could not have been predicted by extrapolating Vinen's measurements.

A plot of log A(T) versus log T reveals a power law dependence on T for temperatures less than $2.0^{o}K$. It was found that the divergent part near the lamda point could be represented by an exponential divergence. The smooth line on figure 4.8 is a plot of the function

$$\log_{10} A(T) = c_1 + c_2 \log_{10} T + \frac{c_3}{1-T/T_\lambda} \qquad (14)$$

where a least squares determination of the three coefficients yielded

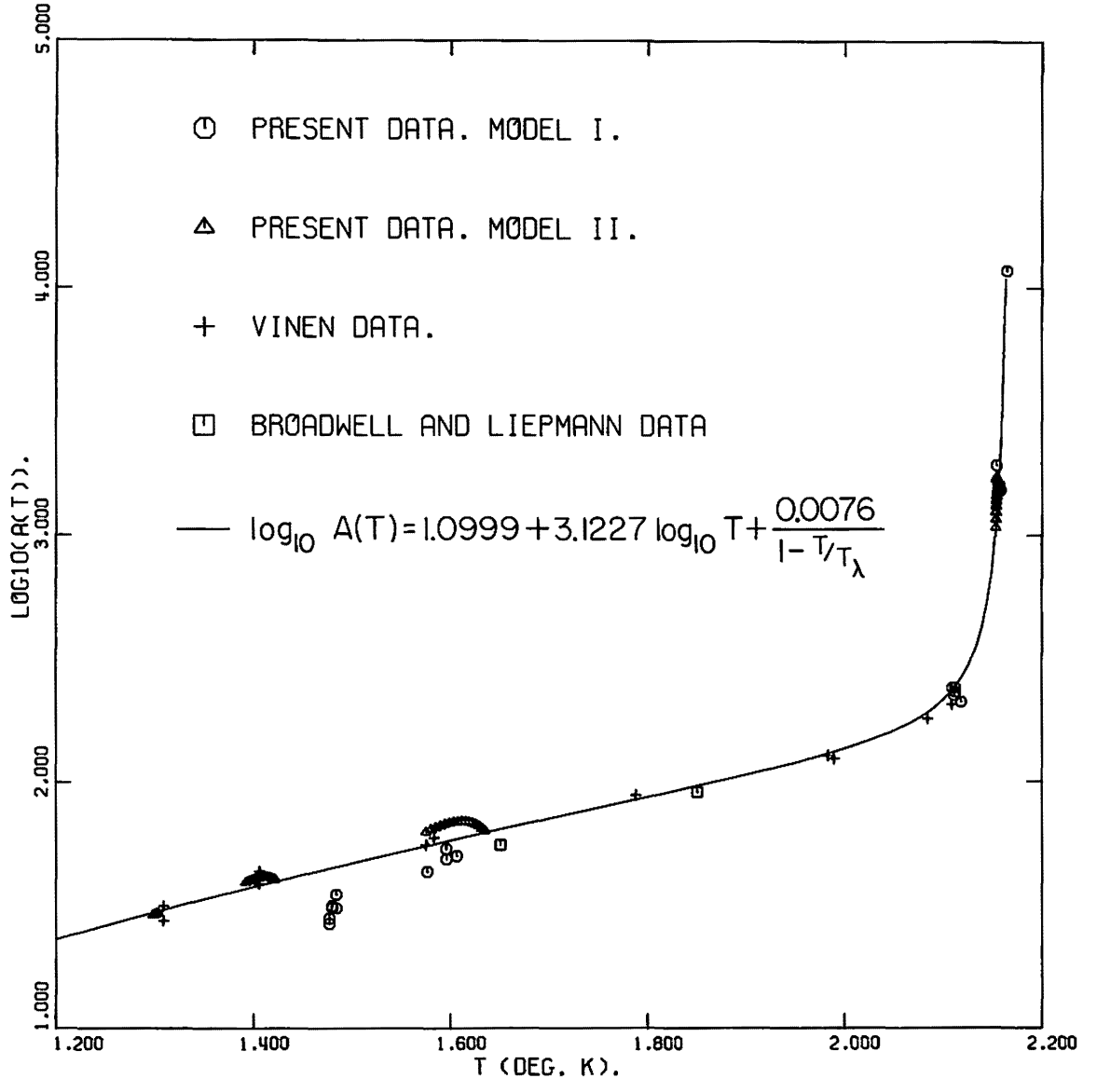

Figure 4.8 The Gorter-Mellink A(T).

$$c_1 = 1.0999$$

$$c_2 = 3.1227$$

$$c_3 = 0.0076$$

The smooth line on figure 4.5 for b(T) was calculated on the basis of equation (8) using the values of A(T) as calculated by equation (14).

Numerical values for A(T) and b(T) on the basis of equation (14) are given on table 4.1.

REFERENCES

[1] Vinen, W.F., Proc. Roy. Soc., A, 242, 493.

[2] Vinen, W.F., Proc. Roy. Soc., A, 240, 114.

[3] Hall, H.E. and Vinen, W.F., Proc. Roy. Soc., A, 238, page 215.

[4] Feynman, R.P., Prog. in Low Temp. Physics, (North Holland, 1955), I, II, page 36.

[5] Vinen, W.F., Proc. Roy. Soc., A, 240, 128.

[6] Broadwell, J.E. and Liepmann, H.W., The Physics of Fluids, 12, 8, page 1533.

Table 4.1

T	ρ_s/ρ	s	ρ	A(T)	b(T)
^oK	—	$J/g\cdot{}^oK$	g/cm^3	cm·sec/g	$\frac{^oK/cm}{(W/cm^2)^3}$
1.20	0.9721	0.0523	0.1451	2.31(1)	2.58(-1)
1.25	0.9629	0.0672	0.1451	2.63(1)	1.30(-1)
1.30	0.9527	0.0855	0.1451	2.98(1)	6.66(-2)
1.35	0.9392	0.1069	0.1451	3.36(1)	3.65(-2)
1.40	0.9233	0.1320	0.1451	3.78(1)	2.10(-2)
1.45	0.9057	0.1620	0.1451	4.23(1)	1.22(-2)
1.50	0.8842	0.1970	0.1451	4.72(1)	7.39(-3)
1.55	0.8594	0.2378	0.1451	5.26(1)	4.65(-3)
1.60	0.8314	0.2840	0.1451	5.84(1)	3.05(-3)
1.65	0.8000	0.3367	0.1451	6.47(1)	2.08(-3)
1.70	0.7645	0.3959	0.1452	7.15(1)	1.48(-3)
1.75	0.7247	0.4617	0.1452	7.91(1)	1.11(-3)
1.80	0.6804	0.5352	0.1453	8.74(1)	8.78(-4)
1.85	0.6310	0.6170	0.1453	9.67(1)	7.53(-4)
1.90	0.5757	0.7091	0.1454	1.07(2)	6.52(-4)
1.95	0.5138	0.8122	0.1455	1.20(2)	6.31(-4)
2.00	0.4448	0.9290	0.1456	1.37(2)	6.83(-4)
2.05	0.3678	1.0620	0.1457	1.62(2)	8.83(-4)
2.06	0.3510	1.0940	0.1457	1.69(2)	9.53(-4)
2.07	0.3330	1.1240	0.1457	1.77(2)	1.06(-3)
2.08	0.3150	1.1550	0.1458	1.87(2)	1.21(-3)
2.09	0.2960	1.1850	0.1458	2.00(2)	1.42(-3)
2.10	0.2769	1.2150	0.1458	2.16(2)	1.72(-3)
2.11	0.2550	1.2520	0.1458	2.39(2)	2.19(-3)
2.12	0.2318	1.2870	0.1459	2.73(2)	3.03(-3)
2.13	0.2068	1.3220	0.1459	3.30(2)	4.71(-3)
2.14	0.1782	1.3610	0.1460	4.44(2)	9.00(-3)
2.15	0.1442	1.4000	0.1460	7.73(2)	2.71(-2)
2.16	0.1044	1.4420	0.1464	3.31(3)	2.79(-1)

Note: Numbers in parentheses indicate powers of ten multiplying entries.

V. Conclusion

Qualitatively, certain aspects of the present data appear to be inconsistent with the two fluid model for liquid helium, in which the two fluids behave in a classical way. To assign the "mutual friction" to a turbulent state of the incoming super fluid leads to contradictions with the observed behavior at counterflow channel exits. The strange dependence of the phenomenon on boundary conditions renders the validity of appending a volume term to a differential equation of motion questionable.

In the interior of the channels, however, both the dependence of the temperature gradient on the cube of the heat flux and the universality of the constant of proportionality is found experimentally to be consistent with the predictions of the Gorter-Mellink term.

The Gorter-Mellink constant appears to diverge as T_λ is approached more rapidly than was indicated by measurements in the past. In fact, the empirical formula

$$\log_{10} A(T) = 1.10 + 3.12 \log_{10} T + \frac{0.0076}{1-T/T_\lambda}$$

is found to be a good representation for $A(T)$ in the range of temperatures $1.3^{\circ}K$ to $2.16^{\circ}K$ covered in this experiment.

APPENDIX 1

1. Introduction

The purpose of the Analog Channel Selector (ACS) is to provide a front end to the HP 3450A Integrating Digital Voltmeter, hereafter referred to as the DVM, or any other similar, externally triggerable instrument. It is designed to switch any one of the four input analog channels into the guarded input of the DVM, without introducing any common-mode errors on the guard line or any bias on the signal line. The 1 μV accuracy of the DVM dictated the use of relays for the purposes of channel switching. The channel lines are assumed to float, no ground connection is made in the ACS unit to any of the inputs. Signal and ground lines are switched independently for each input channel.

The unit is fully programmable and allows the input channels to be selected either manually, or by means of internal logic, or externally. Selection timing can be realized through the use of either of two internal clocks, or an external clock, to provide conditionally timed switching options.

2. Controls

(a) Front Panel. (See figure A1.1).

(1) Power switch and indicator light.

(2) Input Channel (floating) BNC connections.

(3) Input Channel indicators labeling channel presently connected to output BNC.

A1.1

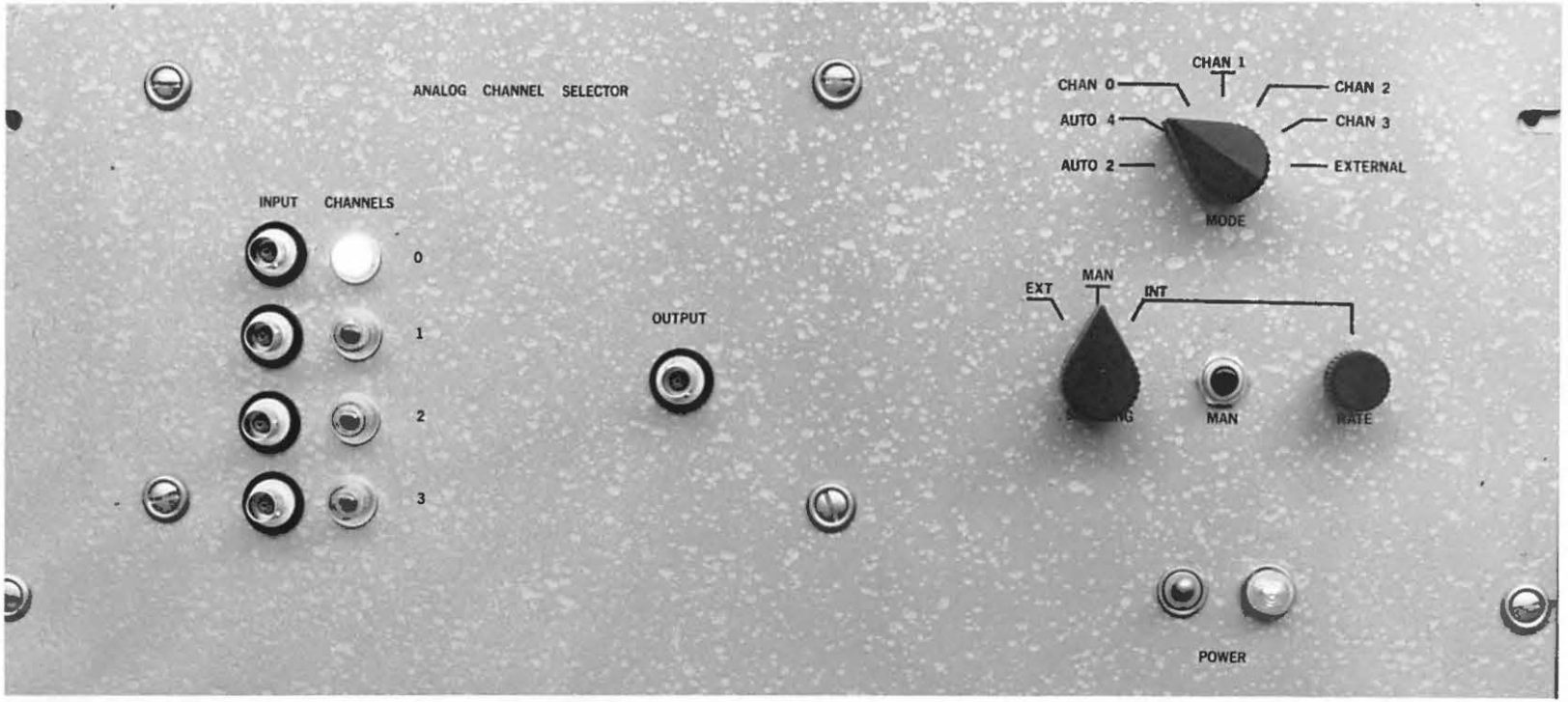

Figure A1.1 Analog Channel Selector Front Panel.

(4) Output BNC (floating).

(5) MODE control switch:

AUTO2: Internal sequential selection of first two channels, once in each sampling cycle. Selector returns to CH0 at the end of the cycle. Switching is synchronous with negative slope of multiplexing clock.

AUTO4: Internal sequential selection of all four channels in each sampling cycle. Selector returns to CH0 at the end of the cycle. Switching is synchronous with negative slope of multiplexing clock.

CH0:
CH1:
CH2:
CH3:
} Manual channel selection of a single input channel.

EXT: Channel selection is defined externally by supplying the channel address bits, EXT0 and EXT1 to the BNC connectors on the rear panel; see figure A1.2. Channel number selected given by $(EXT1\ EXT0)_2$

(6) SAMPLING control switch:

INT: A sampling cycle is inititiated when the internal SAMPLE CLOCK goes high. Sampling period, in this mode, is adjustable from 0.4 s to 2.4 s by means of RATE knob (8). This sampling pulse is available at the BNC connector labeled SAMPLE on the rear panel; see figure A1.2.

MAN: A sampling cycle is initiated when push-button (7) is pressed. Multiplexing is continuous as long as the button is depressed.

EXT: Sampling cycle is initiated when SAMPLE input (same BNC connector on rear panel) goes high. Multiplexing is continuous as long as bit remains high. Note that TTL circuitry assumes a logical 1 for a disconnected input. If no connection is made to the SAMPLE BNC in this mode, continuous multiplexing will result.

(7) MANUAL sampling: This button initiates a sampling cycle when depressed, if switch (6) is set to MAN. Multiplexing is continuous as long as button is depressed.

(8) RATE: Controls sampling period when switch (6) is set to INT.

(b) Rear Panel. (See figure A1.2).

(1) READ: (output) This is an open-collector output, matched for a negative transition to a 93 Ohm line. It is normally high and will draw current from a resistor in series with a voltage source (less than 20 Volts) to go low for 28 μs triggering the reading instrument (e.g. DVM). The READ pulse occurs 20 ms after the SAMPLE positive edge or the MPX CLOCK negative edge.

(2) SAMPLE: (input and output) This connector furnishes the SAMPLE pulse in the internal (INT) or manual (MAN) sampling mode for the purposes of synchronizing additional instruments to the ACS. In the external (EXT) sampling mode it serves as the input for the external sampling pulse.

(3) CLOCK control switch: This selects the MPX CLOCK from an internal FAST (75 ms period) or SLOW CLOCK (140 ms period), or an external timing source (EXT).

(4) CLOCK (BNC): (input or output) This serves as an output in the internal FAST or SLOW clock modes and as an input in the EXT mode. The external clock pulses must meet the following specifications:

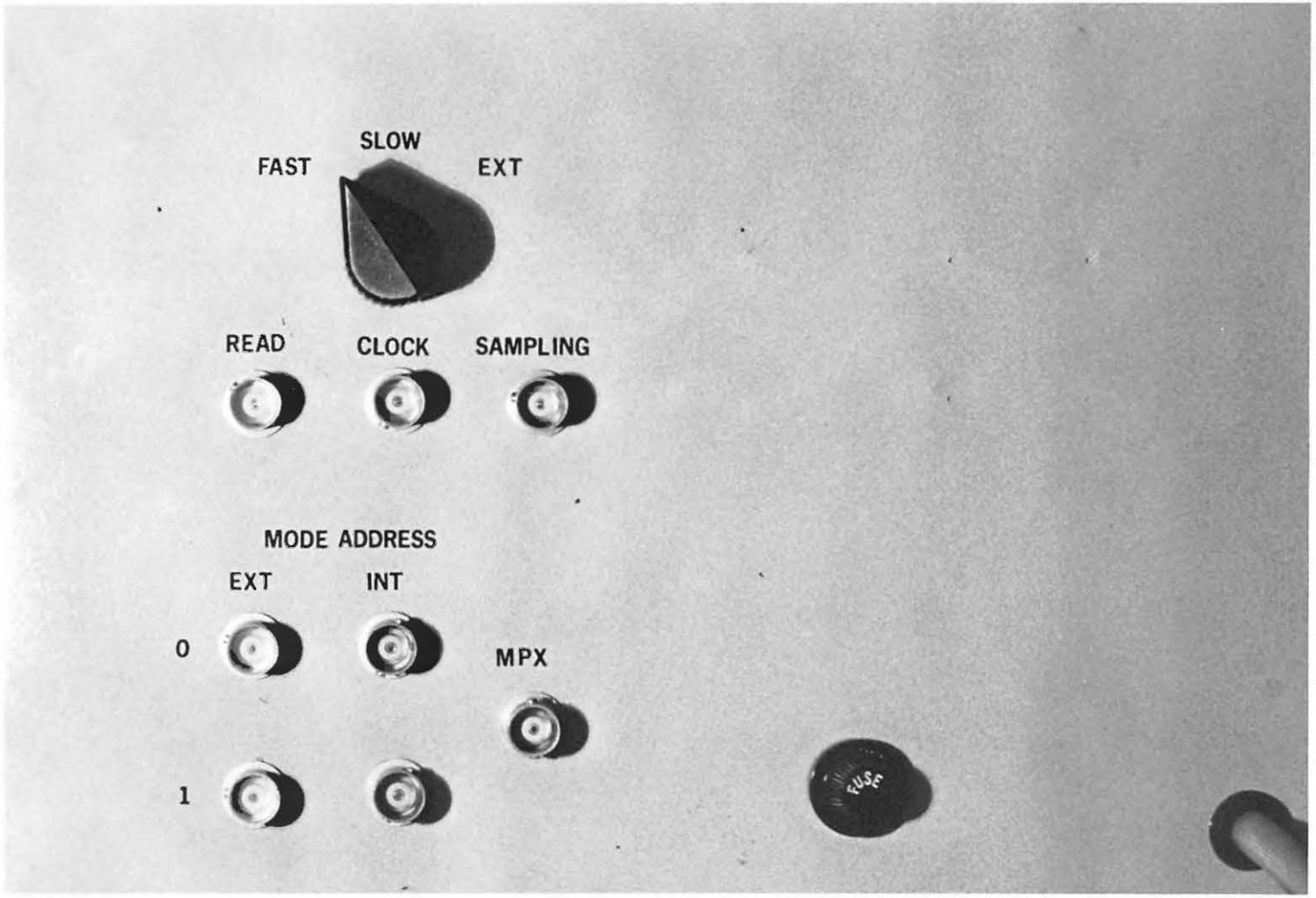

Figure A1.2 Analog Channel Selector Rear Panel.

(a) TTL compatible: Logical 0 between 0.0 V and 0.5 V, logical 1 between 3.5 V and 5.0 V.

(b) CLOCK must be normally low and stay so until a sample pulse occurs.

(c) First negative slope should occur no sooner than 20 ms after positive edge of sampling pulse. Consecutive negative slopes should be spaced by at least 20 ms.

(d) CLOCK should stay low after last multiplexed channel is switched in each sampling sequence.

NOTE: Channel switching is realized at the negative edge of the CLOCK, READ goes low. 20 ms later. Positive edge of clock has no timing effect.

(5) EXT0 and EXT1: (inputs) These are address bits defining the selected channel. Channel number is given by $(\text{EXT1 EXT0})_2$. These inputs are operative in the EXT position of the Control Switch.

(6) INT0 and INT1: (outputs) These are address bits defining internally selected channel number, given by $(\text{INT1 INT0})_2$. These bits are operative in all modes and are given by (see NOTE 1).

INT0 = S0

INT1 = 0 in AUTO 2, S1 otherwise.

(see figure A1.3 and page 59).

(7) MPX: (output) Low in AUTO4 mode, high otherwise.

3. Specifications

Operating line voltage	115 V a. c.
Internal D. C. Voltage supplies	+5. 0 V (regulated).
	-30 V (unregulated).
Logical 0	0. 0 to 0. 8 V
Logical 1	3. 0 to 5. 0 V
Internal Sample period	0. 4 to 2. 4 s
Internal Sample pulse duration	14 μ s
External Sample pulse specifications	see page 60 note 5
Internal MPX CLOCK period, FAST	@ 75 ms
SLOW	@ 150 ms
Internal MPX CLOCK duration, FAST	@ 50 ms
SLOW	@ 125 ms
External MPX CLOCK specifications	see page 48 and 50
READ command	20 ms after MPX CLOCK
	negative edge
READ command duration	28 μ s
FUSE and fuse location	1 A Sloblo, rear panel.

4. Circuit descriptions

a. Logic

The internal logic circuit, figure A1.3, provides the commands for the sequential channel selection when the unit is operated in the internal modes (AUTO2 and AUTO4).

The central circuit of the selection logic consists of a two-bit (S0 and S1) counter (S-counter) whose state determines the channel selection. The remaining components include:

Flip-flop E, normally at logical 1, is switched to logical 0 by the SAMPLE pulse and stays low during the sampling cycle. This signal inhibits any additional SAMPLE pulses when it is low and, thereby, serves at the "busy" bit.

One-Shot A provides the necessary delay of 20 ms between the internal command to switch the next channel and the output command to the reading instrument to read (READ). This allows for a 7 ms delay between the command to open a relay and the command to close the next one, and an additional 14 ms delay allowing the contact bounce and noise to subside.

One-Shot $\overline{\text{READ}}$ which saturates the open-collector output transistor for 28 μs providing the READ command on the rear panel.

Digital multiplexers X and Y which select the two channel address bits from the

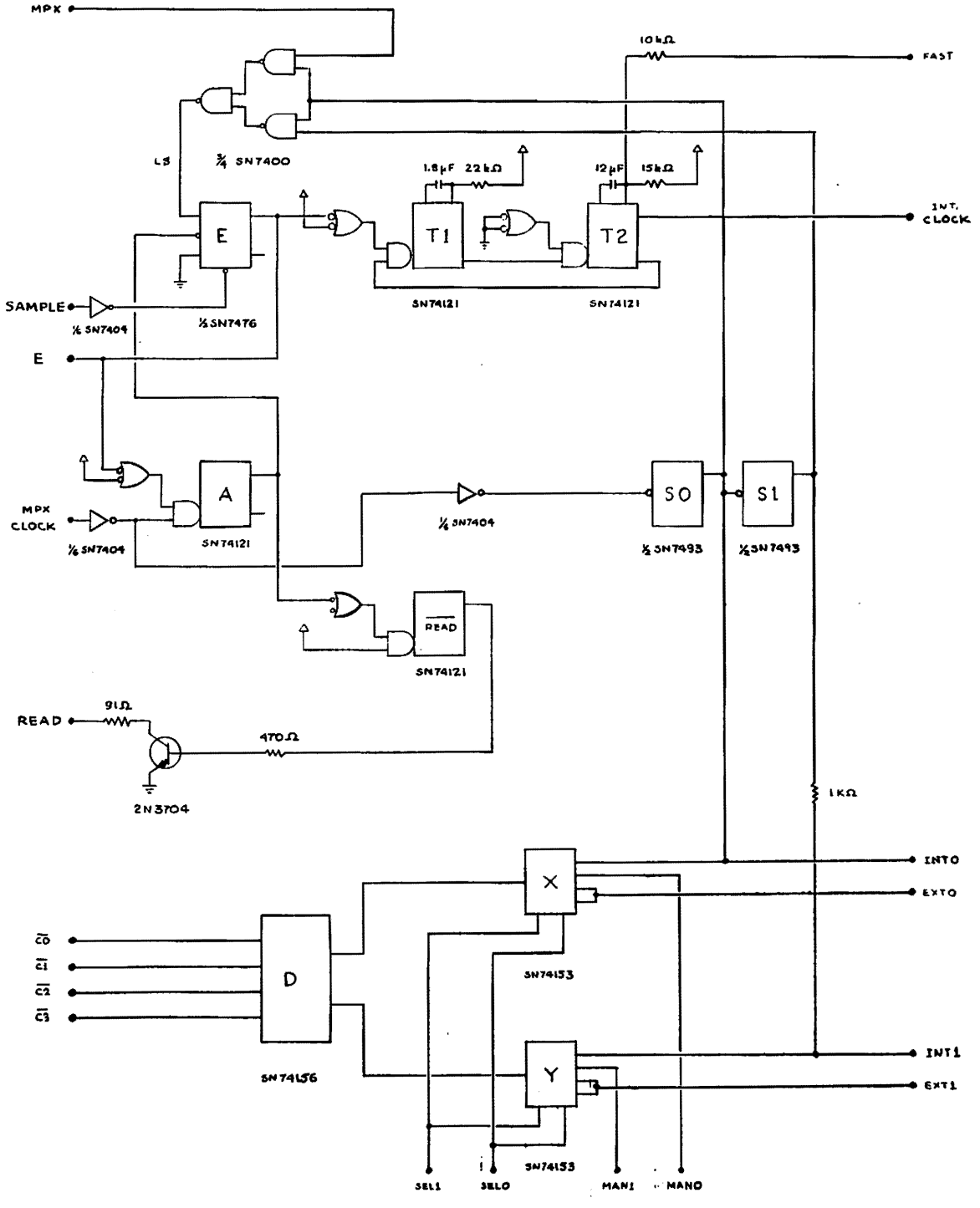

Figure A1.3 Analog Channel Selector Logic

(1) Internal address bits, (INT0, INT1) which are essentially S0 and S1 subject to the state of the MPX bit (see page A1.5) defining the last state in the sampling sequence, (see page 59 , Note 3).

(2) Manual address bits (MAN0 and MAN1) defined in manual modes by the MODE control switch. See page 58 .

(3) External address bits, EXT0 and EXT1, supplied to the rear panel BNC connectors in the EXT mode.

Digital "2-to-4" decoder C , which defines which relay, is activated in accordance with the X and Y address bits from the digital multiplexers.

The sequence of events in the internal modes, e.g. AUTO 4, INT CLOCK, INT Sampling, is as follows. (See figures A1.3 and A1.4).

(1) SAMPLE pulse resets E. E negative edge starts INT CLOCK (MPX CLOCK in this mode) and triggers A. Note that once started, INT CLOCK is a free-running oscillator as long as E is low. See page 60 .

(2) SAMPLE pulse goes low.

(3) A negative edge triggers $\overline{\text{READ}}$ which gives READ command to open-collector transistor. The reading instrument is triggered to read CH0.

(4) MPX CLOCK goes high.

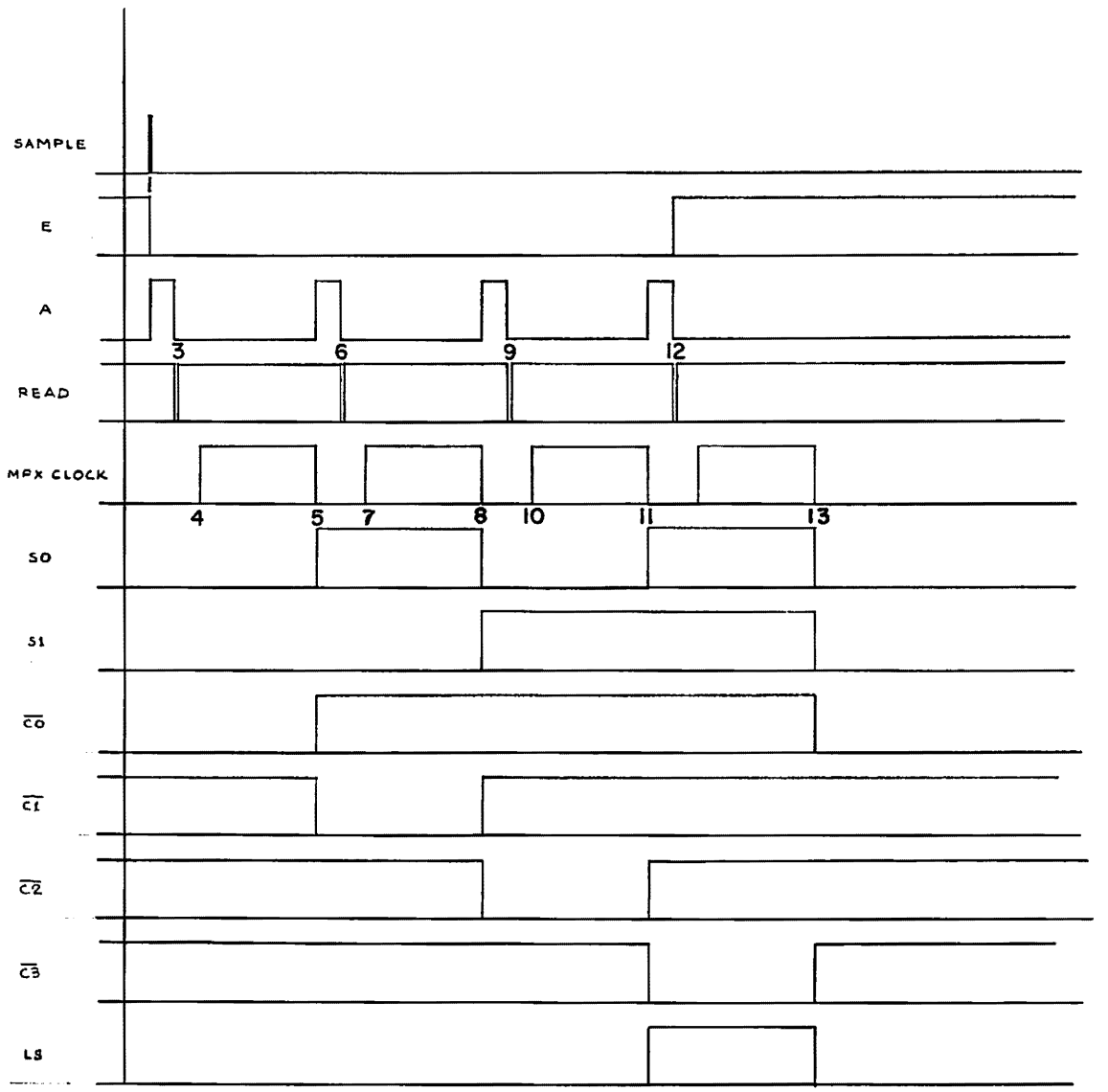

Figure A1.4 Timing Sequence

(5) MPX CLOCK goes low. The negative edge triggers A and increments S-COUNTER. $\overline{C0}$ goes high, $\overline{C1}$ goes low. CH0 relay opens and CH1 relay closes after a 7 ms delay provided for on the relay cards (see figure A1.5.). The 7 ms delay safeguards against mechanical differences in the relays which might result in two of them being closed at the same time thereby shorting the two input instruments with each other.

(6) A goes low, triggers $\overline{READ}$ one-shot which provides READ command for CH1.

(7) MPX CLOCK goes high.

(8) MPX CLOCK goes low triggering one-shot A and incrementing S-COUNTER to address CH2.

(9) A goes low, triggers $\overline{READ}$, CH2 is read.

(10) MPX CLOCK goes high.

(11) MPX CLOCK goes low triggering one-shot A and incrementing S-COUNTER to address CH3. In this mode (AUTO4), the Last State (LS) bit goes to 1 at this time.

(12) A goes low, triggers $\overline{READ}$, CH3 is read, E is set to logical 1 and T1 of INT CLOCK is disabled.

(13) T2 goes low resetting S-COUNTER to 0. CH0 is addressed again. Sampling sequence ends.

Mode selection is realized with the MODE control switch, described on page 46 , by defining: the digital multiplexer address bits SEL0 and SEL1 (see figure A1.3), the manual mode address bits MAN0 and MAN1, the MPX bit, and the INT1 bit, according to the truth table

	AUTO2	AUTO4	CH0	CH1	CH2	CH3	EXT
SEL0	0	0	1	1	1	1	X
SEL1	0	0	0	0	0	0	1
MAN0	X	X	0	1	0	1	X
MAN1	X	X	0	0	1	1	X
MPX	1	0	X	X	X	X	1
INT1	0	S1	X	X	X	X	S1

where: 0 designates logical 0, 1 designates logical 1 and X designates "don't care" (irrelevant state).

Each of the five control inputs assumes a logical 1 unless grounded, with the exception of INT1 which is equal to S1 unless grounded (see figure A1.3). The MODE control switch connects to ground only those inputs that have to be at logical 0. This is accomplished by a 3-pole, 7-throw non-shorting rotary switch with a connection matrix to ground:

t \ P	1	2	3
1	SEL1	SEL0	INT1
2	SEL1	SEL0	MPX
3	SEL1	MAN1	MAN0
4	SEL1	MAN1	n. c.
5	SEL1	MAN0	n. c.
6	SEL1	n. c.	n. c.
7	n. c.	n. c.	n. c.

where n. c. designates "no connection".

NOTE 2. In the AUTO2 mode, the output of S1 is ignored and the input to the digital multiplexer corresponding to S1, i. e. INT1, is set to zero by the MODE control switch.

NOTE 3. Last State bit (LS) goes to logical 1 when the last state is reached by the S-COUNTER, i. e.

$$(S1\ S0)_2 = 1 \quad \text{in AUTO2}$$

$$(S1\ S0)_2 = 3 \quad \text{in AUTO4}$$

or

$$LS = MPX \cdot S0 + S1 \cdot S0$$

NOTE 4. The clocking sequence has been designed to allow the $\overline{PC}$ (Print Command) bit from the HP 3450A output jack to serve as the external clock. This permits the use of the autorange feature of the HP 3450A, which

requires variable timing (see HP 3450A manual). With this external clock, the ACS will wait for the DVM to autorange and integrate before switching to the next channel. If the DVM is simultaneously connected to Coupler (CPL) (see Appendix 2), the $\overline{PC}$•CR bit from the rear panel of the CPL can be used instead.

NOTE 5. In using an external SAMPLE pulse it should be noted that E always stays low as long as the SAMPLE input is high (see figure A1.3). Thus if the SAMPLE bit is high when the Last State bit (LS) goes high the sampling sequence is not terminated and the cycle begins again. Consequently multiplexing is continuous in the external sampling mode, as long as the SAMPLE input is kept at logical 1. Thus if only a single sampling cycle is desired for each SAMPLE pulse, the SAMPLE pulse should go low before the first negative slope of the MPX CLOCK in the AUTO2 mode and the third negative slope of the MPX CLOCK in the AUTO4 mode (see figure A1.4). It should be noted that the timing restrictions imposed by this condition depend on the clocking scheme used (FAST, SLOW or EXT).

(b) Clocks.

(i) Internal Multiplexing Clock (INT. CLOCK). This consists of two SN74121 (TI) one-shots, T1 and T2 (see figure A1.3) working in tandem. The INT. CLOCK pulses are the Q-output of T2.

T1 is triggered by the negative slope of flip-flop E and stays high for approximately 25 ms. At the end of this interval $\overline{Q}$ of T1 rises to trigger T2. The Q-output of T2 stays high for 50 ms in the FAST mode and 125 ms in the SLOW mode. When $\overline{Q}$ of T2 rises, T1 is triggered once again and the cycle is repeated as long as E stays low. When E rises, T1 is disabled and the clock sequence ends when T2 goes low (see figure A1.4).

The 125 ms time-constant for T2 in the SLOW mode is realized with a 12 μ F (electrolytic) capacitor and a 15 kΩ resistor as the timing elements. The 50 ms time constant in the FAST mode is realized by connecting a 10 kΩ resistor in parallel to the 15 kΩ, thereby reducing the timing resistance to 6 kΩ. This is done by the CLOCK selection switch on the rear panel. Thus the internal multiplexing clock periods are 75 ms and 150 ms in the FAST and SLOW modes respectively.

(ii) Internal Sampling Clock (SAMPLE CLOCK). This consists of two SN74121 one-shots T3 and T4 (see figure A1.5), working in tandem as described above for the Internal Multiplexing clock (INT. CLOCK). The frequency of the one-shot pair is reduced by a $\div$ 16 frequency divider consisting of four flip-flops in sequency (SN7493). A third one-shot T5, defines the internal SAMPLE pulse duration of 14 μs, being triggered on every positive slope of the $\div$ 16 output.

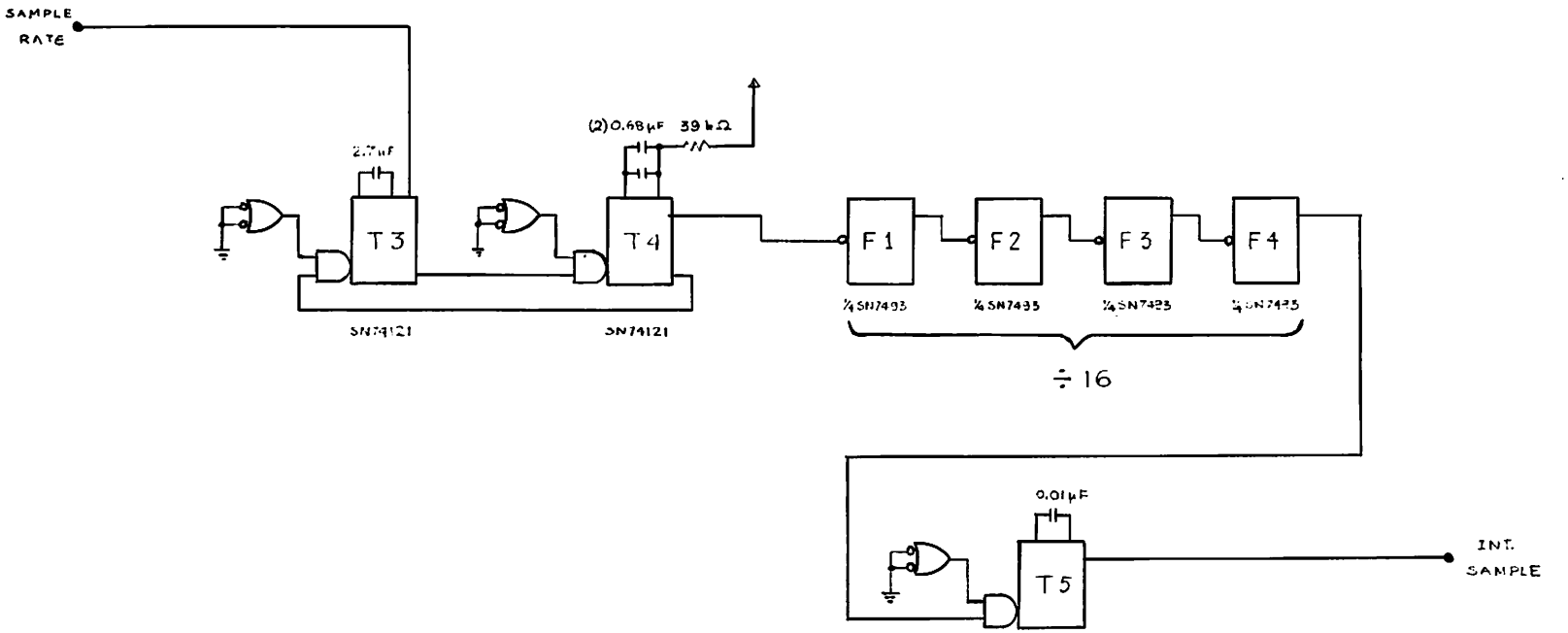

Figure A1.5 Internal Sampling Clock

The oscillator is started by supplying the + 5.0 Volt (V_{cc}) supply voltage with a fast rise-time; see power supply description on page 65. This is sufficient to start the oscillator automatically every time the unit is turned on. The SAMPLE period is varied by using a 50 kΩ potentiometer in series with the internal 2 kΩ timing resistor of the SN74121 (TS). The use of the ÷ 16 frequency divider and T5 was dictated by the duty-cycle and frequency limitations of the SN74121 and the SAMPLE pulse duration requirements imposed by the logic circuit (see note 4 on page 59).

c) Relay Cards.

Channel switching is realized by activating one relay card at a time with the corresponding command bit ($\overline{C0}$, $\overline{C1}$, $\overline{C2}$, $\overline{C3}$), (see pages 55 and 56 and figure A1.4). The relays used (AUTONETICS 455-0018-019) are double-throw, double-pole enabling both the signal and ground lines to be switched independently for each channel.

The negative edge of the command bit triggers a 7 ms one-shot (SN74121) whose $\overline{Q}$-output goes to a 2-input, open-collector NAND gate (SN7401). The second input of the NAND gate receives the command bit after it has been delayed by the three NAND gates remaining on the SN7401 chip. This allows for the delay in the gates of the one-shot ensuring that the one-shot output gets to the NAND gate first. Thus the output of the fourth NAND gate goes low 7 ms after the command bit negative edge saturates a PNP transistor (40410; RCA) in series with the relay coil and the relay

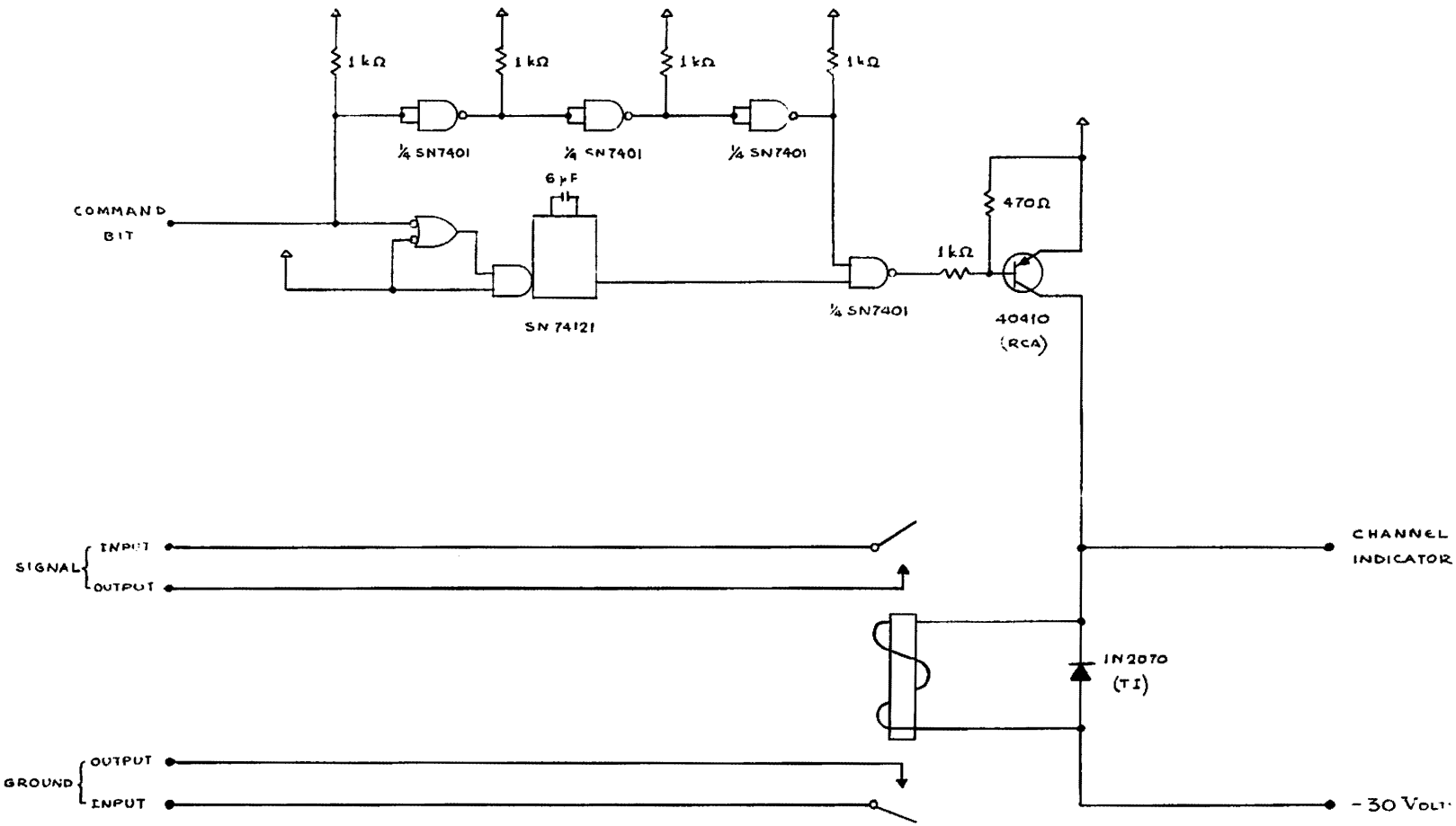

Figure A1.6 Relay Cards (4)

closes (see figure A1.6). A power diode (IN2070; TI) is connected across the coil to short the reactive negative voltage swing, a consequence of the fast rise-time of the applied voltage. The indicator light on the front panel corresponding to each channel is connected in parallel with the relay coil and is lit when the coil voltage is applied. The relay opens and the corresponding indicator light goes off when the command bit goes high.

d) Power Supplies.

(i) 5.0 Volt D. C. Regulated Power Supply. This uses a PNP bypass power transistor (40410; RCA) whose base current is regulated by a μA723 (FAIRCHILD) voltage regulator in order to keep the output at 5.0 Volts. The raw 15 Volts of DC is applied by an SCR (C20B; GE) with a 10 Volt Zener diode in series with its gate which waits for the filter capacitor after the bridge rectifier to be charged to at least 10 Volts (see figure A1.7). This insures that the μA723 has an adequate voltage when power is applied to it, so that the 5.0 Volt output will rise quickly to start the internal SAMPLE CLOCK as described on page 61 .

(ii) 35 Volt D.C. Unregulated Power Supply. This uses a 28 Volt center-tapped transformer secondary driving a full-wave rectifier with two filter capacitors in series (see figure A1.7). The positive line of this supply is tied to the 5.0 Volt output of the regulated supply leaving the other end at - 30 V as required by the relay cards (see figure A1.6).

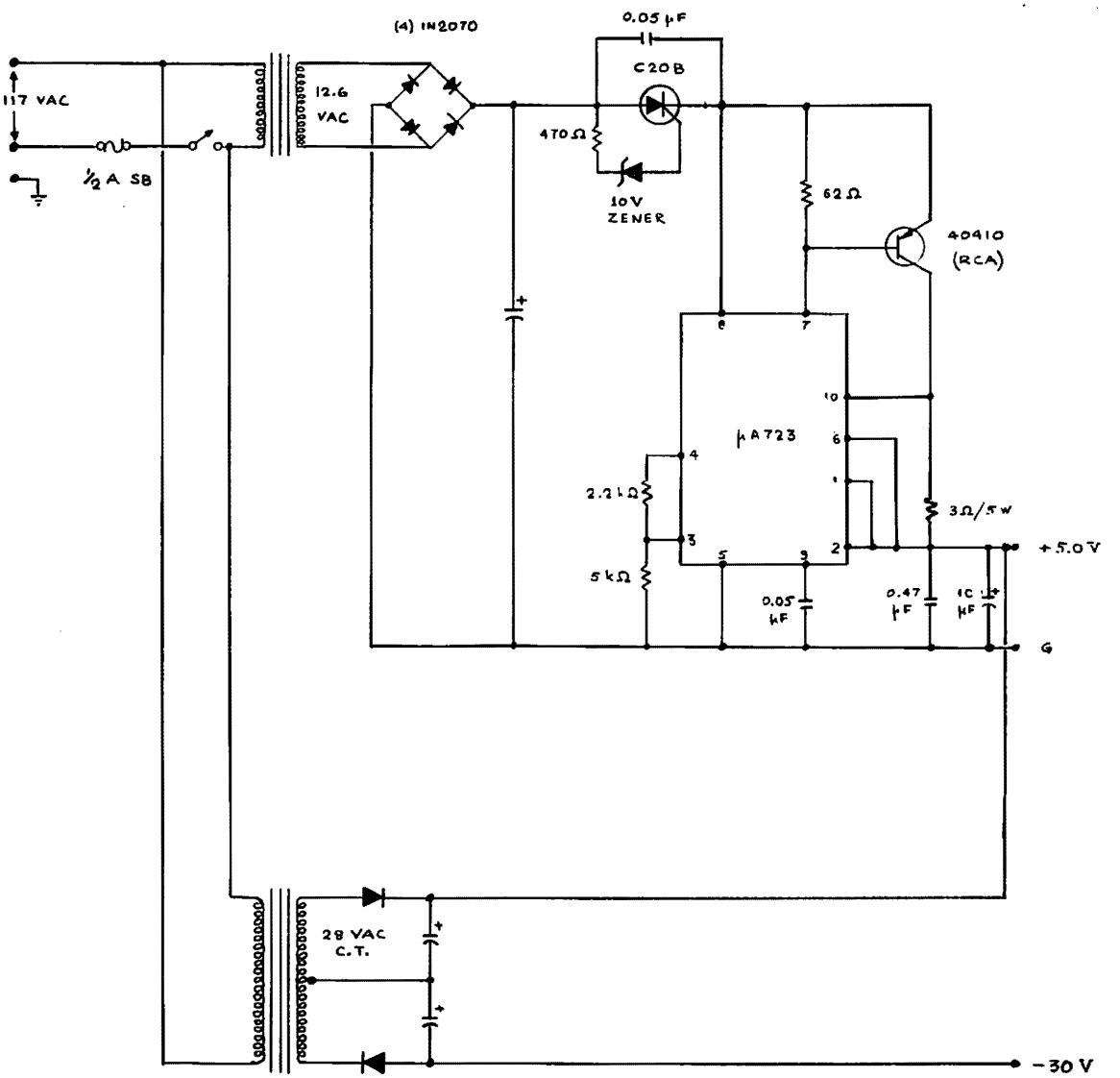

Figure A1.7 Power Supplies

Appendix 2

I. Introduction

The purpose of the Digital Data Coupler (CPL) is to provide an interface between the digital output of any laboratory instrument and an Incremental Tape Recorder. Even though it is specifically designed to take the output of an HP-3450A Digital Voltmeter and write it on a Kennedy 1600/360 Incremental Tape Recorder it can be modified by altering input and output interface cards to become compatible with an instrument whose digital output can be coded by means of 32 bits, and any Incremental Tape Recorder similar to the Kennedy 1600/360. The instrument output from a single readout is stored and held by the Coupler until it has been written on the tape recorder. It is formatted into a preselected number of bytes per readout (1 byte = 8 bits) and records of preselected length.

Octal counters on the front panel keep track of recorded data while manual controls allow the recording to be interrupted and resumed at any time.

2. Controls

(a) Front Panel (see figure A2. 1).

(1) Power switch and indicator light.

(2) BYTE COUNTER display. This is the output of an octal (1-2-4) counter which keeps track of the number of bytes in each record (see Note 1). This counter is reset automatically at the end of a record, or manually with the RESET button (10).

(3) BYTES PER READOUT switch. This selects the number of bytes to be written for each instrument readout. The choices of 1, 2, or 4 correspond to 8, 16, or 32 bit outputs. The option of 3 bytes is not offered so as not to force the record size to be other than a multiple of 4, as required by most tape reading programs.

(4) RECORD SIZE switch. This selects the number of bytes constituting one record. The options of 256, 1024, 2048 and 4096 are available. At the end of the preselected number of bytes an Inter-Record Gap (IRG) Command is given to the Tape Recorder. Any multiple of the record sizes available on the front panel can be obtained by using an external frequency divider and the EXTERNAL RECORD SIZE MULTIPLIER option on the rear panel (see item (8), p. 74).

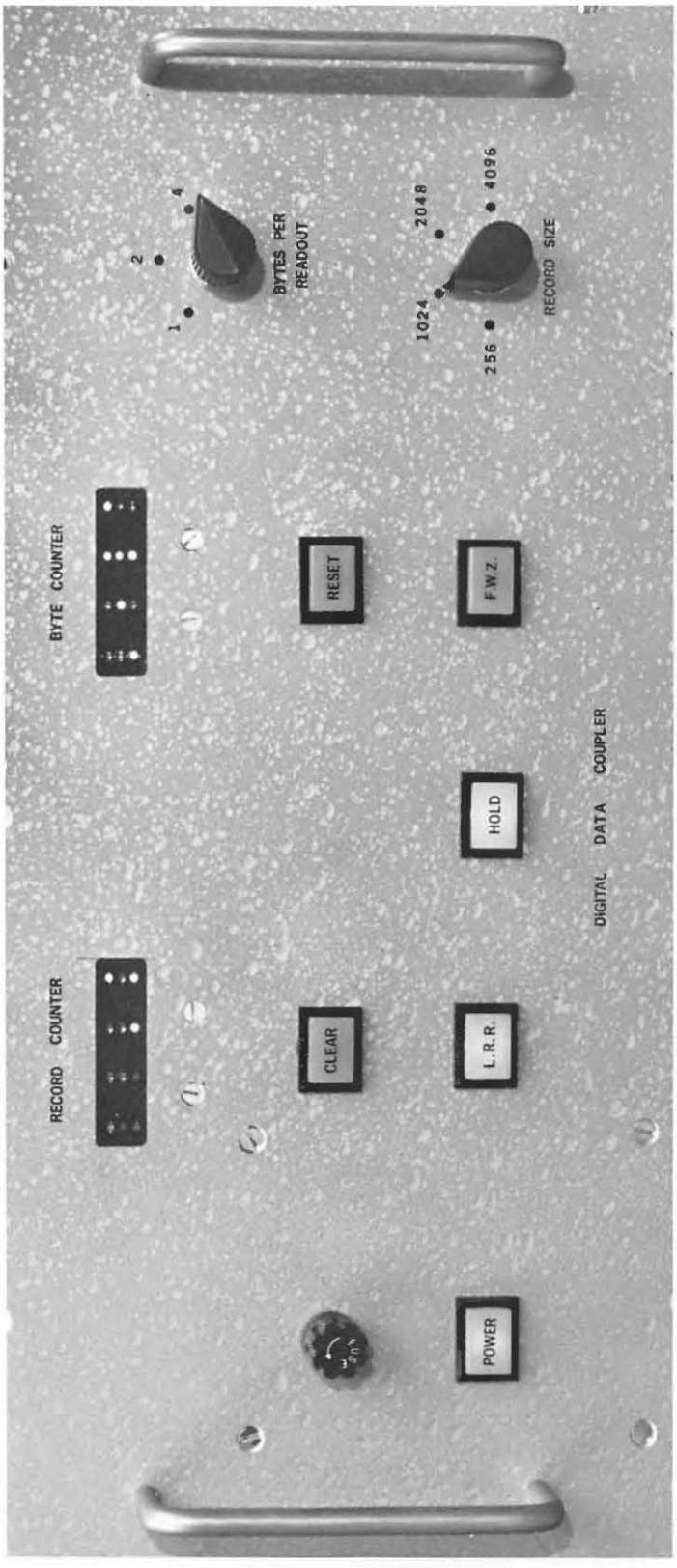

Figure A2.1 Coupler Front Panel.

A2.1

(5) RECORD COUNTER display. This is the output of an octal (1-2-4) counter which keeps track of the number of records that have been written on the tape (see Note 1). This counter can be reset to zero with the CLEAR button (6).

(6) CLEAR button. Resets record counter.

(7) HOLD button. This is an alternate action switch which inhibits the transmission of data to the tape recorder when lit. (Due to internal time constants the user must allow for 2 seconds before actuating the switch again).

(8) LRR (Last Record Request) button. This can be activated at any time (indicator lights up). The purpose of this switch is to stop data recording at the end of the present record. If the button is depressed before the record starts, the Coupler will write one record and stop, ignoring subsequent data (this allows data to be written one record at a time).

(9) FWZ (Fill With Zeros). Sometimes data ends somewhere in the middle of a record. Actuating this button will fill the remaining record with zeros at the maximum rate. In this case, the BYTE COUNTER display will retain the number of data bytes that were written. When the FWZ button is pressed the coupler assumes that the user is also requesting a stop at the end of the record and the LRR condition is actuated internally.

(10) RESET button. This lights up indicating that the "Last Record Requested" has been completed. Pressing the RESET button removes this condition and resets the BYTE COUNTER. The HOLD option is not affected by the RESET button. The RESET button and the CLEAR button (6) must be pressed after turning power on to initiate the logic states properly.

NOTE 1. The RECORD COUNTER and BYTE COUNTER are octal counters in which each column signifies a digit in a 4-digit octal number. The octal digit is coded in the standard 1-2-4 arrangement. A lit LED (light emitting diode) signifies a 1, an unlit LED signifies a zero. For example

o	●	●	●	(x 4)
●	o	●	●	(x 2)
o	●	●	o	(x 1)

designates the number:

$$2576_8 = (2 \times 512 + 5 \times 64 + 7 \times 8 + 6)_{10}$$

$$= 1406_{10}$$

(b) Rear Panel (see figure A2.2)

(1) INPUT Connectors. These 50-pin connectors (Amphenol 57-40500 or equivalent) are connected in parallel to allow an additional recording instrument to be simultaneously connected (e.g. HP 5050B printer). Pin designations are determined by the connections made on the Input Interface Cards #9 and #10 (see page 90).

(2) INTERNAL DATA Connector. This is a 50-pin connector (Amphenol 57-40500 or equivalent), not in use as of this writing (August 1972). It is allocated to provide internal data such as record size, bytes per readout, record number, etc., to a printer (e.g. HP 5050B) so as to create a tape log automatically as the data is recorded.

(3) OUTPUT Connector. This is a 36-pin connector (Amphenol 57-40360 or equivalent). Pin designations are determined by the connections made on the Output Interface Cards #7 and #8 (see page 94).

(4) CR (Coupler Ready; BNC Output). This output is high when coupler is ready to accept data and goes low when a readout is processed. Any data from the instrument supplied when CR is low will be ignored.

(5) $\overline{PC}$· CR (Conditional Print Command; BNC Output). This is the $\overline{PC}$ bit from the reading instrument subject to the condition CR (Logical $\overline{PC}$ and CR). This output can serve as a conditional clock pulse to synchronize

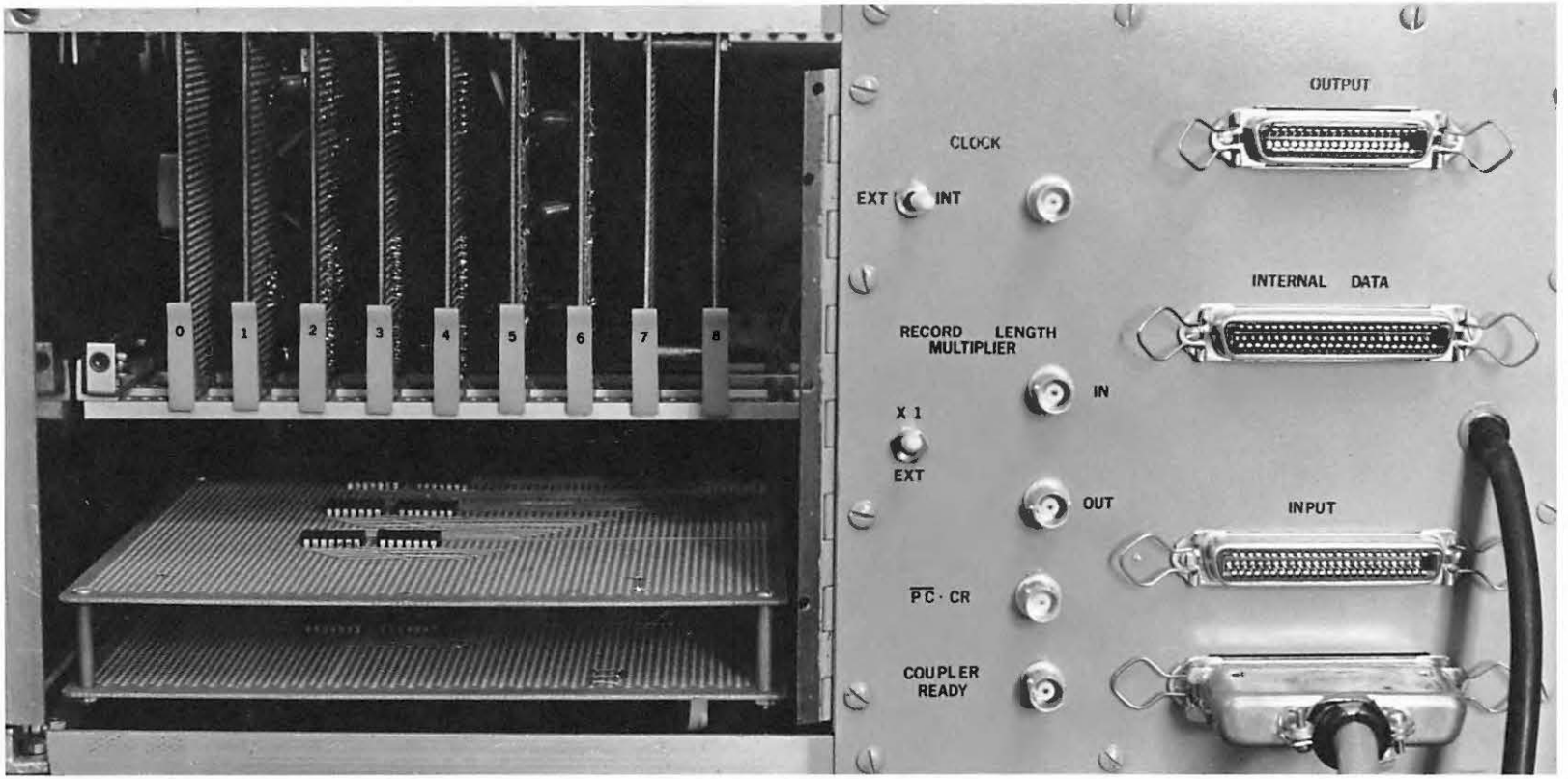

Figure A2.2 Coupler Rear Panel.

a front end to the reading instrument (e.g., Analog Channel Selector described in Appendix 1).

(6) CLOCK Selection Switch

INT: Internal clock with ≥ 2 m sec period, compatible with Kennedy 1600/360 maximum bit rate.

EXT: External Clock to provide slewing options for the Kennedy 1600/360.

(7) CLOCK (Input or Output BNC).

This connector serves as an output when the Internal Clock (INT) is used and as an input when the External Clock is used (EXT). If the CLOCK is external, the first positive slope must follow the negative slope of $\overline{PC}$ no sooner than 2 ms to observe the tape recorder bit-rate limitations. This can be decreased to 1 ms in a slewing mode (see Kennedy 1600/360 manual).

(8) RECORD LENGTH MULTIPLIER Switch.

X1 : The BYTE COUNTER counts the number of bytes written. Record length is the one selected on the front panel.

EXT: This allows a digital frequency divider by N in between the output BNC connector (10) and the input BNC connector (9). Since the BYTE COUNTER sees the pulses at the input connector (9), the record length selected on the front panel is multiplied by N. The output connector (10) and the input connector (9) are shorted in the

X1 position of the RECORD LENGTH MULTIPLIER Switch.

(9) IN (Input BNC). This serves as the input to the BYTE COUNTER. It is shorted with OUT (10) in the X1 mode of the RECORD LENGTH MULTIPLIER Switch.

(10) OUT (Output BNC). This is the output of the byte pulses. (One-shot A. See page 77).

2. Specifications

Operating Line Voltage	115 V A. C.
Fuse and fuse location	3A sloblo
Internal D. C. Supply	5.0 V D. C.
Logical 0 (Low)	0.0 to 0.8 Volts
Logical 1 (High)	3.0 to 5.0 Volts
Internal clock period	2 ms

3. Circuit Descriptions

(a) Logic (Card #2).

The Internal Logic Circuit (figure A2.3) provides the channel selection address bits (S0 and S1) and the Write Command (WC) to transfer the selected bits that constitute one byte to the tape recorder. In addition it keeps track of the various conditions that are active (e.g., Gap In Process, Hold, Fill with Zeros, etc.) to define the Coupler Ready bit (CR). This bit is high (TRUE) when the Coupler is ready to transmit additional data.

The Logic is composed of the following parts:

J-K flip-flop C, normally at logical 1, is reset to zero when $\overline{PC}$ (Print Command) from the reading instrument goes low. The negative slope of C starts the CLOCK (see page 82) and sets the CR bit to logical zero. It is clocked back to logical 1 at the end of a readout sequence and stops the CLOCK.

One-shot A provides a 28 μs pulse, 2 ms (or one clock period, if externally defined) after a WRITE pulse has been sent to the tape recorder. This increments the BYTE COUNTER and triggers the next WRITE pulse.

S-COUNTER (output S0 and S1), is a two bit counter whose output addresses the eight bits that form a byte on the tape. It is reset to zero when the $\overline{PC}$ bit from the reading instrument goes high, subject to the condition that the previous readout sequence is completed ($\overline{PC}\cdot$ CR bit, see figure A2.3).

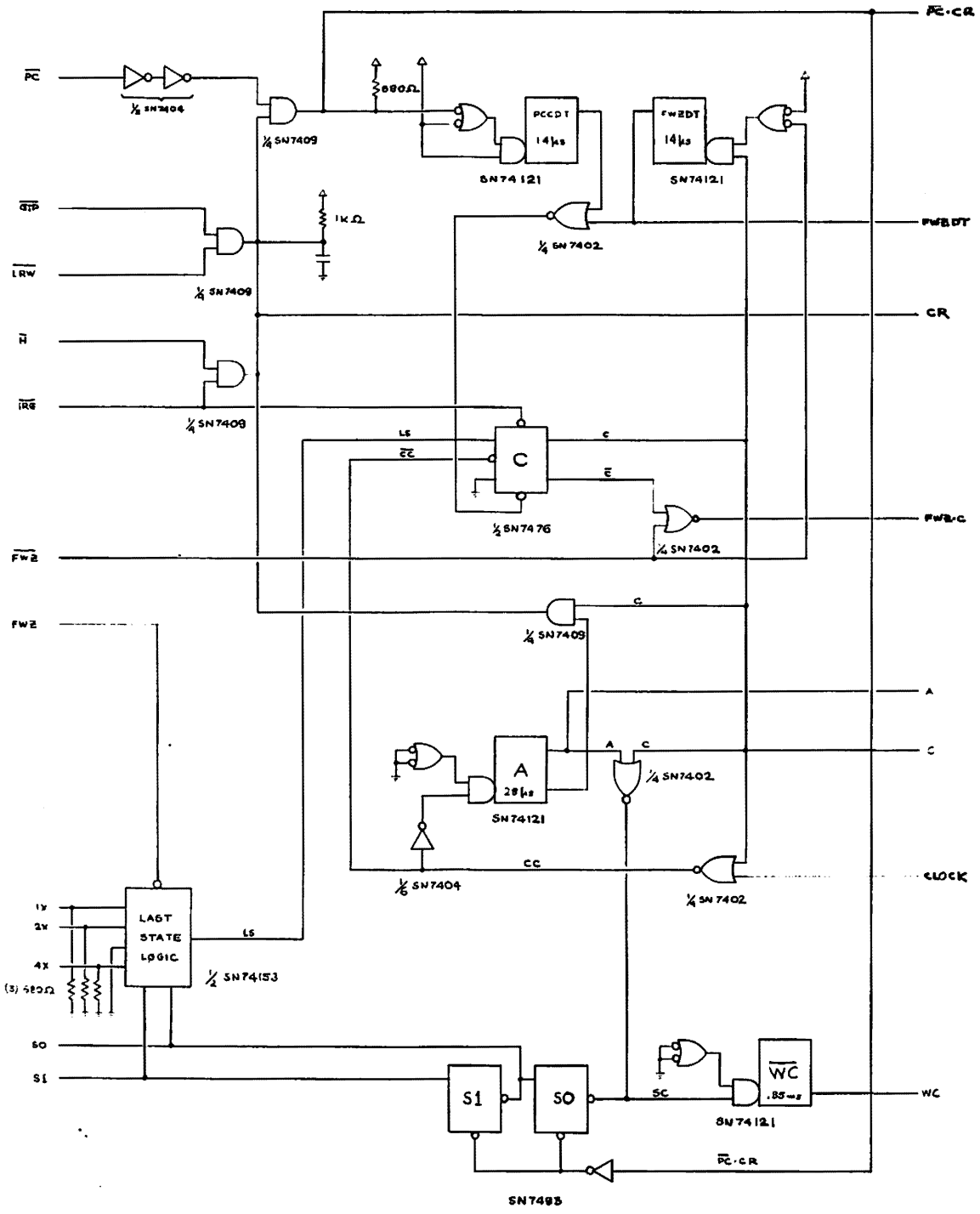

Figure A2.3 Coupler logic.

LAST STATE LOGIC (output LS). This is a one-out-of-four line selector (SN74153) in accordance with the state of the S-COUNTER. One of the input lines, with the exception of the third (see page 68 , item 3) is set to be logical 1 by the front panel BYTES PER READOUT switch. Thus the Last State bit (LS) goes high when the selected number of bytes have been written. The FWZ input acts as a strobe. LS is at logical 0 when FWZ is at logical 1 regardless of all the other inputs. The truth table is as follows:

S1	S0	FWZ	LS
x	x	1	0
0	0	0	1X
0	1	0	2X
1	0	0	0
1	1	0	4X

where x designates an irrelevant state.

CR AND-gate. This is a wire -AND gate composed of three open collector two-input AND gates (3/4 SN7409) CR is at logical 1 if the Coupler is ready to process additional data. This condition requires that:

(i) the present readout sequence is completed (C = 1 and A = 0).

(ii) the Inter-Record Gap is not being inserted (IRG = 1).

(iii) the data are not held manually through the front panel HOLD button ($\overline{H}$ = 1).

(iv) The remainder of the record is not being filled with zeros and that the last record, if requested, has not been written ($\overline{LRW}$ = 1).

A Print Command pulse ($\overline{PC}$) from the reading instrument will initiate the following sequence of events referred to as a readout sequence (for the purposes of example, 4 bytes per readout are assumed to be selected and the internal clock is used). See figure A2.4.

(0) $\overline{PC}$ goes high. If CR = 1, $\overline{PC}\cdot CR$ also goes high and resets the S-COUNTER to zero. The first set of eight bits (first byte) is selected on the input multiplexers (see page).

(1) $\overline{PC}$ goes low. This triggers a one-shot (PCCDT) whose output (14 μs) resets flip-flop C to zero. The negative slope of C triggers the first one-shot (T1) of the clock circuit (see figure A2.5) and $\overline{T1}$ goes low. It also causes the SC bit to rise ($SC = \overline{A}\cdot\overline{C}$) triggering the $\overline{WC}$ one-shot.

(2) PCCDT goes low.

(3) WC ($\overline{Q}$ - output of $\overline{WC}$ one-shot) rises after 0.35 ms triggering the WRITE one-shot (70 μs) whose output clocks the first eight bits (first byte) into the tape recorder.

(4) WRITE one-shot goes low.

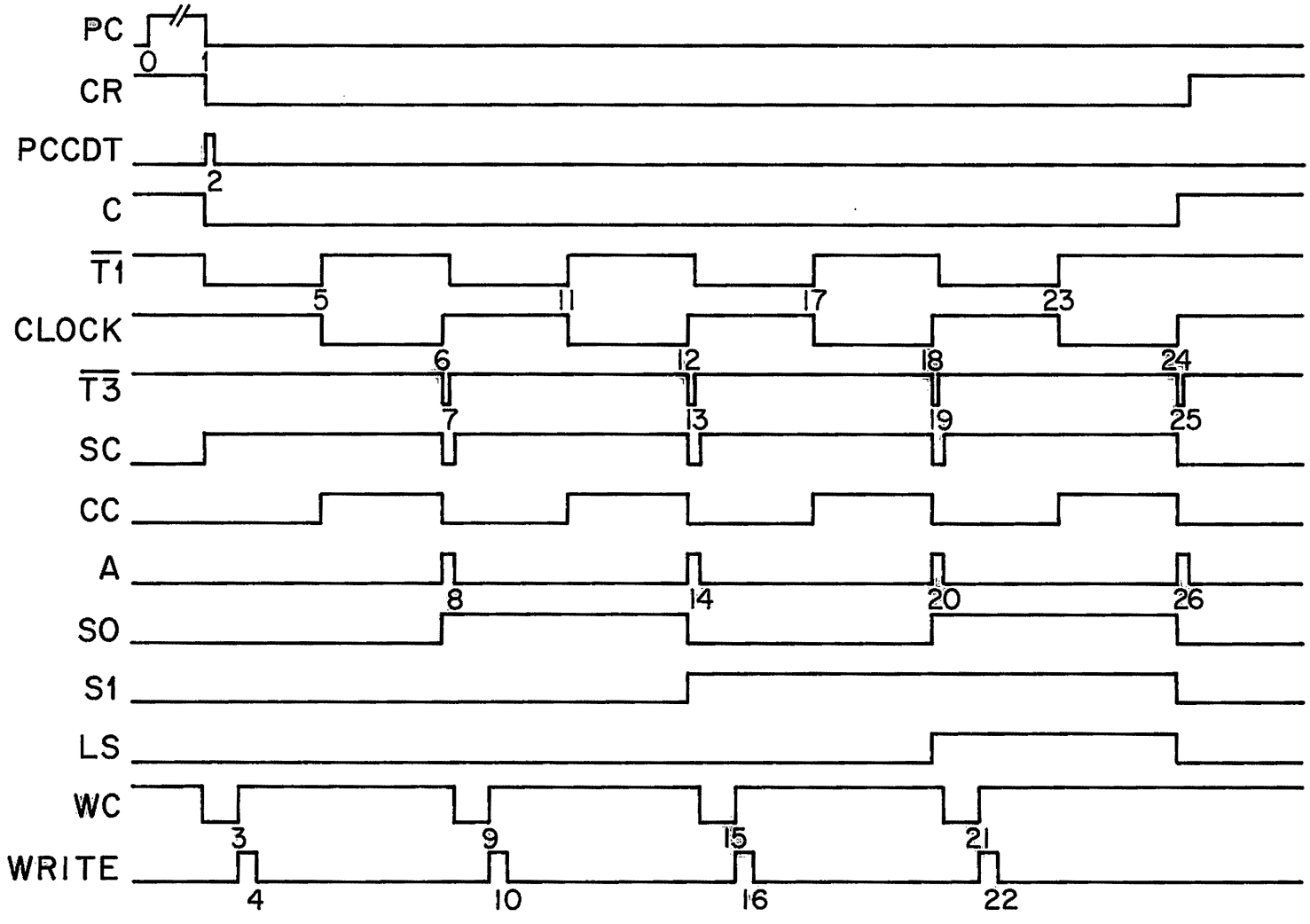

Figure A2.4 Readout timing sequence.

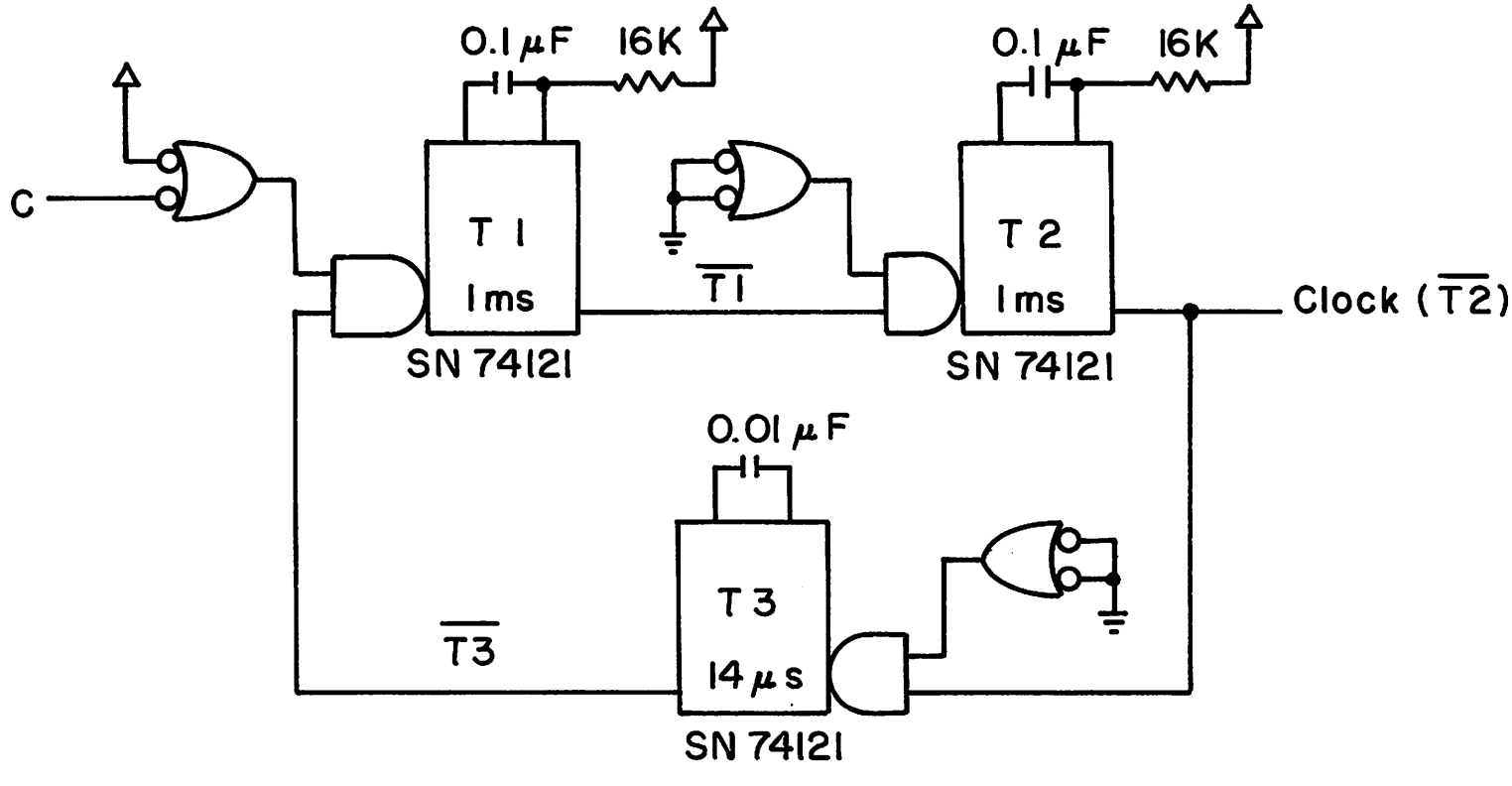

Figure A2.5 Internal Clock.

(5) $\overline{T1}$ of the clock circuit goes high, triggering the second one-shot (T2) whose $\overline{Q}$-output ($\overline{T2}$ serves as the internal CLOCK. $\overline{T2}$ goes low and CC rises (CC = $\overline{C} \cdot \overline{CLOCK}$).

(6) $\overline{T2}$ (CLOCK) rises triggering the third one-shot (T3) in the internal clock circuit. The positive slope of the CLOCK pulse triggers one-shot A (28 μs) through the negative slope of CC. The output of A causes SC to go low incrementing the S-COUNTER to SO = 1, S1 = 0. These S-COUNTER outputs

   (i) address the second set of eight bits (second byte), and

   (ii) address the second input (2X) of the Last State Logic. The Last State bit (LS) is left at logical 0.

(7) $\overline{T3}$ rises triggering T1. $\overline{T1}$ goes low.

(8) A goes low, SC goes high and triggers one-shot $\overline{WC}$.

(9) WC goes high triggering the second WRITE pulse.

(10) WRITE one-shot goes low.

(11) $\overline{T1}$ goes high triggering T2. $\overline{T2}$ goes low.

(12) T2 rises triggering T3. $\overline{T3}$ goes low. CC goes low triggering one-shot A. SC goes low incrementing S-COUNTER. Next set of eight bits is addressed (third byte). Next input of Last State Logic is addressed (LS is still at logical 0).

(13) $\overline{T3}$ rises, triggering T1. $\overline{T1}$ goes low.

(14) A goes low, SC goes high and triggers one-shot $\overline{WC}$. WC goes low.

(15) WC goes high triggering the third WRITE pulse.

(16) WRITE one-shot goes low.

(17) $\overline{T1}$ goes high triggering T2. $\overline{T2}$ goes low.

(18) $\overline{T2}$ rises triggering T3. $\overline{T3}$ goes low. CC goes low triggering one-shot A. SC goes low incrementing S-COUNTER. Next set of eight bits is addressed (fourth byte). 4X input of Last State Logic is addressed and LS goes high.

(19) $\overline{T3}$ goes high and triggers T1. $\overline{T1}$ goes low.

(20) A goes low, SC goes high and triggers one-shot $\overline{WC}$. WC goes low.

(21) WC goes high triggering fourth WRITE pulse.

(22) WRITE one-shot goes low.

(23) $\overline{T1}$ goes high and triggers T2. $\overline{T2}$ goes low.

(24) $\overline{T2}$ rises triggering T3. $\overline{T3}$ goes low. CC goes low clocking LS (J-Input to flip-flop C) to the output. C goes high disabling T1 and forcing SC to logical 0. S-COUNTER is incremented. A also fires but SC is already at logical 0. A has no effect other than keeping CR low.

(25) $\overline{T3}$ goes high. T1 does not fire (C is at logical 1).

(26) A one-shot goes low. CR goes high and the sequence ends.

TABLE A2.1

$t_1 = t_0 + \tau_{\overline{PC}}$	(duration of $\overline{PC}$)
$t_2 = t_1 + 14\ \mu s$	(" " PCCDT one-shot)
$t_3 = t_2 + 0.35\ ms$	(" " $\overline{WC}$ " ")
$t_4 = t_3 + 70\ \mu s$	(" " WRITE " ")
$t_5 = t_1 + 1\ ms$	(" " T1 " ")
$t_6 = t_5 + 1\ ms$	(" " T2 " ")
$t_7 = t_6 + 14\ \mu s$	(" " T3 " ")
$t_8 = t_6 + 28\ \mu s$	(" " A " ")
$t_9 = t_8 + 0.35\ ms$	(" " $\overline{WC}$ " ")
$t_{10} = t_9 + 70\ \mu s$	(" " WRITE " ")
$t_{11} = t_7 + 1\ ms$	(" " T1 " ")
$t_{12} = t_{11} + 1\ ms$	(" " T2 " ")
$t_{13} = t_{12} + 14\ \mu s$	(" " T3 " ")
$t_{14} = t_{12} + 28\ \mu s$	(" " A " ")
$t_{15} = t_{14} + 0.35\ ms$	(" " $\overline{WC}$ " ")
$t_{16} = t_{15} + 70\ \mu s$	(" " WRITE " ")
$t_{17} = t_{13} + 1\ ms$	(" " T1 " ")
$t_{18} = t_{17} + 1\ ms$	(" " T2 " ")
$t_{19} = t_{18} + 14\ \mu s$	(" " T3 " ")
$t_{20} = t_{18} + 28\ \mu s$	(" " A " ")
$t_{21} = t_{20} + 0.35\ ms$	(" " $\overline{WC}$ " ")
$t_{22} = t_{21} + 70\ \mu s$	(" " WRITE " ")
$t_{23} = t_{19} + 1\ ms$	(" " T1 " ")
$t_{24} = t_{23} + 1\ ms$	(" " T2 " ")
$t_{25} = t_{24} + 14\ \mu s$	(" " T3 " ")
$t_{26} = t_{24} + 28\ \mu s$	(" " A " ")

The timing in the preceding sequence is described in Table A2.1.

NOTE 2. The WRITE one-shot is part of the output interface circuit (page 94) since its specifications are particular to the tape recorder.

NOTE 3. The interval provided by one-shot $\overline{WC}$ allows the data inputs to the tape recorder (8 bits forming the byte to be written) to settle (minimum of 50 μs required by the Kennedy 1600/360) before the leading edge of the WRITE pulse arrives.

NOTE 4. The full clock period after the last WRITE command is provided to keep the CR bit low, safeguarding against the next $\overline{PC}$ negative edge arriving too soon. Since the readout sequence is initiated by the $\overline{PC}\cdot$ CR bit, if $\overline{PC}$ goes up and down before CR rises, the new data are ignored.

NOTE 5. The purpose of one-shot T3 is to give time to C to disable T1 at the end of the sequence.

NOTE 6. CR is kept low (after C has risen) by A to safeguard against a $\overline{PC}$ negative edge arriving during the 14 μs that T3 is active.

The FWZ (Fill With Zeros) sequence can be initiated at any time by pressing the FWZ button on the front panel (page 70, item (9)). The $\overline{FWZ}$ bit from the Front Panel Interface circuit (page 87, figure A2.6) acts like a $\overline{PC}$ bit triggering a 14 μs pulse

(FWZDT one-shot) which resets the C flip-flop (figure A2.3, page 77). If the FWZ button is activated in the middle of a read-out sequence, the FWZDT one-shot will wait until the sequence is completed. In both cases the C flip-flop goes low to start a sequence similar to the readout sequence. The difference in this case is that the FWZ bit also acts on the Last State Logic and keeps the LS bit from going high (see Truth Table, page 79). Thus C stays low and the sequence proceeds until the end of the record. The sequence is terminated with the $\overline{\text{IRG}}$ bit (page 98 , figure A2.1) which sets the C flip-flop to logical 1. Zeros are written because the FWZ bit acts as a strobe on the input multiplexers and gives zeros at the output regardless of the state of the inputs (see page 94 , figure A2.8).

(b) Front Panel Interface (Card #1).

The Front Panel Interface provides the pulses and levels required by the action of the front panel push-buttons, with the exception of the CLEAR button (item (6), page 70) which acts directly to clear the RECORD COUNTER (see page 70 , figure A2.12), the buttons are interfaced as follows (see figure A2.6):

The FWZ button (item (9), page 70) sets the FWZ flip-flop whose Q-output saturates a transistor which lights the FWZ indicator. The FWZ flip-flop is reset manually with the RESET button (item (10), page 71) described below.*

* The FWZ button has a second set of contacts which are connected in parallel to the LRR button (item (8), page 70). Pressing the FWZ button activates the LRR button (the converse is not true).

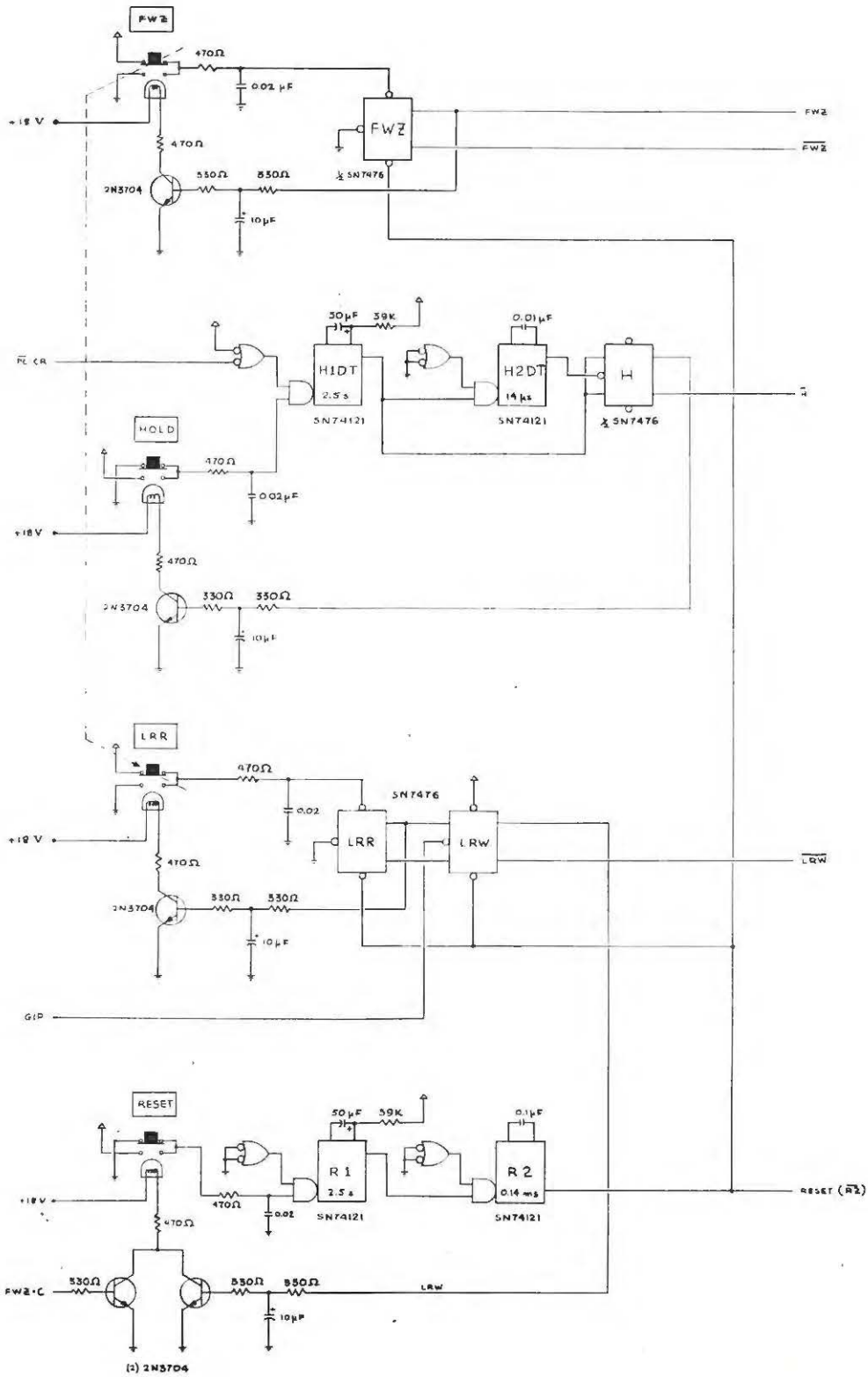

Figure A2.6 Front Panel Interface

The HOLD button triggers the H1DT one-shot (2.5 seconds) which triggers a 14 μs one-shot (H2DT) whose negative slope toggles flip-flop H (SN7476). Pressing the HOLD button again (after 2.5 seconds) generates a second 14 μs pulse which changes the state of flip-flop H. Thus the HOLD button acts as an alternate action switch.

The LRR (Last Record Request) button sets a flip-flop (LRR) (whose Q and $\overline{Q}$ outputs serve as the J-K inputs to a second flip-flop (LRW). When the LRR button is activated, the LRR flip-flop is set and the LRR indicator is lit. The negative slope of the GIP (Gap In Process) signal from the tape recorder clocks the LRR flip-flop outputs to the LRW flip-flop outputs when the record is written. This sets the LRW Q-output at logical 1 saturating a transistor which lights the RESET indicator. The RESET indicator has then to be pressed before data recording can be resumed.

The RESET button triggers a 2.5 s one-shot (R1) whose positive slope triggers a 0.14 ms one-shot (R2). The $\overline{Q}$-output of the second one-shot ($\overline{R2}$) serves as the RESET pulse to clear the BYTE COUNTER and remove the FWZ or LRR conditions if they are active. The RESET indicator is lit at the end of a record completed with zeros (FWZ$\cdot$C) or at the end of a record requested to be the last one (LRW). Note that in this arrangement the FWZ$\cdot$C bit is essentially redundant since it is always followed by the LRW transition to logical 1, delayed only by the record gap interval (70 ms for the Kennedy 1600/360 tape recorder).

c) Input Interface Cards (Cards #9 and #10)

The main purpose of the Input Interface cards is to provide the means to accomodate any allocation of pins in the input 50-pin connectors (item (1), page 72). A maximum of 34 connections is required, including the 32-bit output, the $\overline{PC}$ bit and a connection for the common ground. Any input combination can be realized on these cards. In addition, any necessary input logic can be hardwired such as level changes, coding changes (e.g. 1-2-2-4 to 1-2-4-8).

Two such pairs of cards are currently in use with the Coupler. The first one (figure A2.7a) provides standard interfacing with a 32-bit output in which the 32 bits are all arranged in sequence starting from one end of the 50-pin connector. Signal buffering is also realized through a double (logical) inversion with the TI SN74L04 as the first of the two inverters.

The second pair of Input Interface cards (figure A2.7b) provides an interface with the HP3450A Digital Voltmeter. In this case pins 15, 16, 41, 41, which code the FUNCTION digit (see HP3450A manual), are ignored and pins 17, 18, 42, 43 coding the POLARITY digit are used instead. Signal buffering was not necessary in this case.

d) Input Latches and Multiplexers (Cards #3 and #4).

The negative edge of $\overline{PC} \cdot CR$ clocks the 32-bits as arranged on the Input Interface Cards (page 90) to the output of eight 4-bit latches (SN7475) corresponding to the eight bits of each character (see figure A2.8). These are selected by the state of

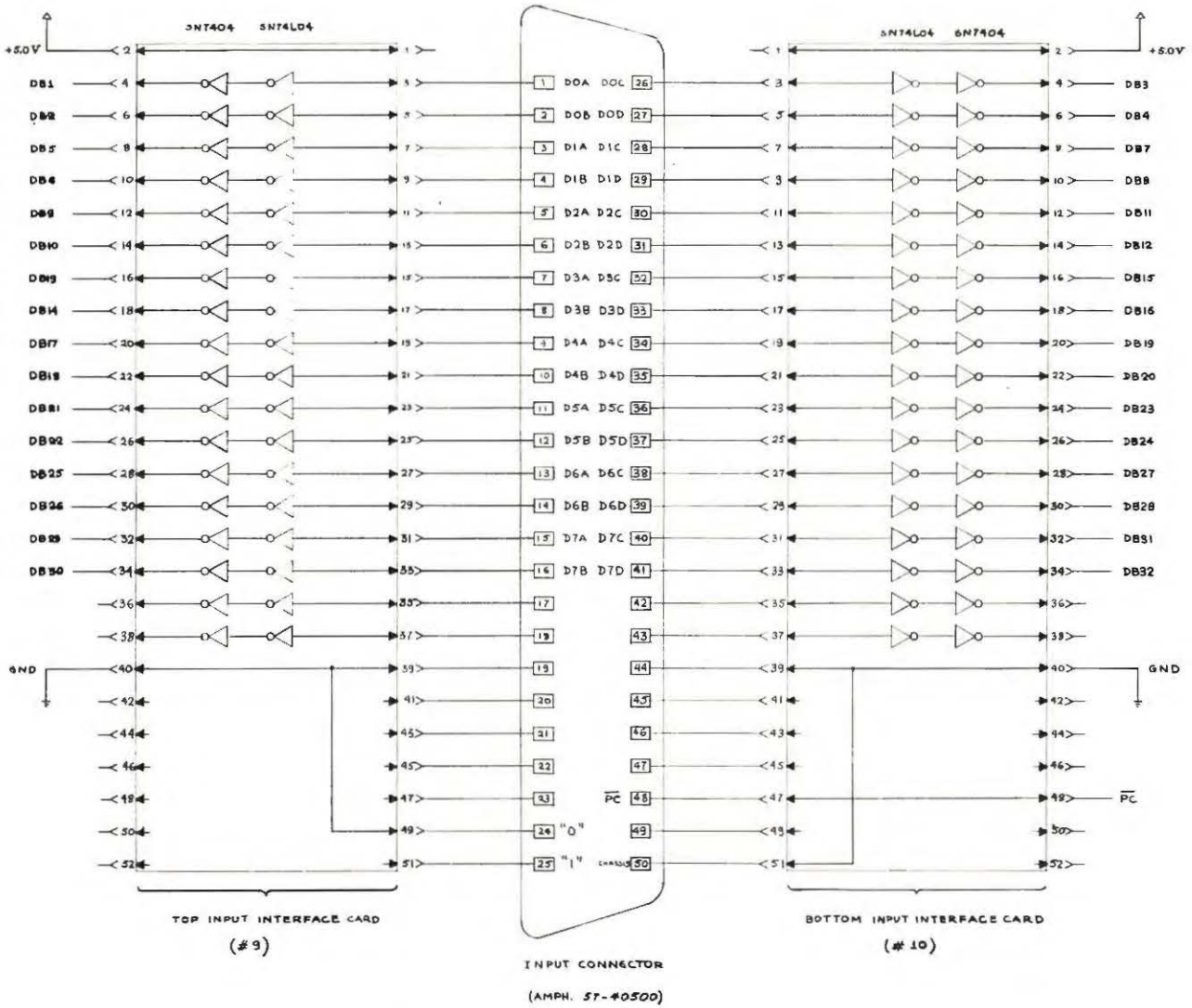

Figure A2.7a Standard Input Interface Card

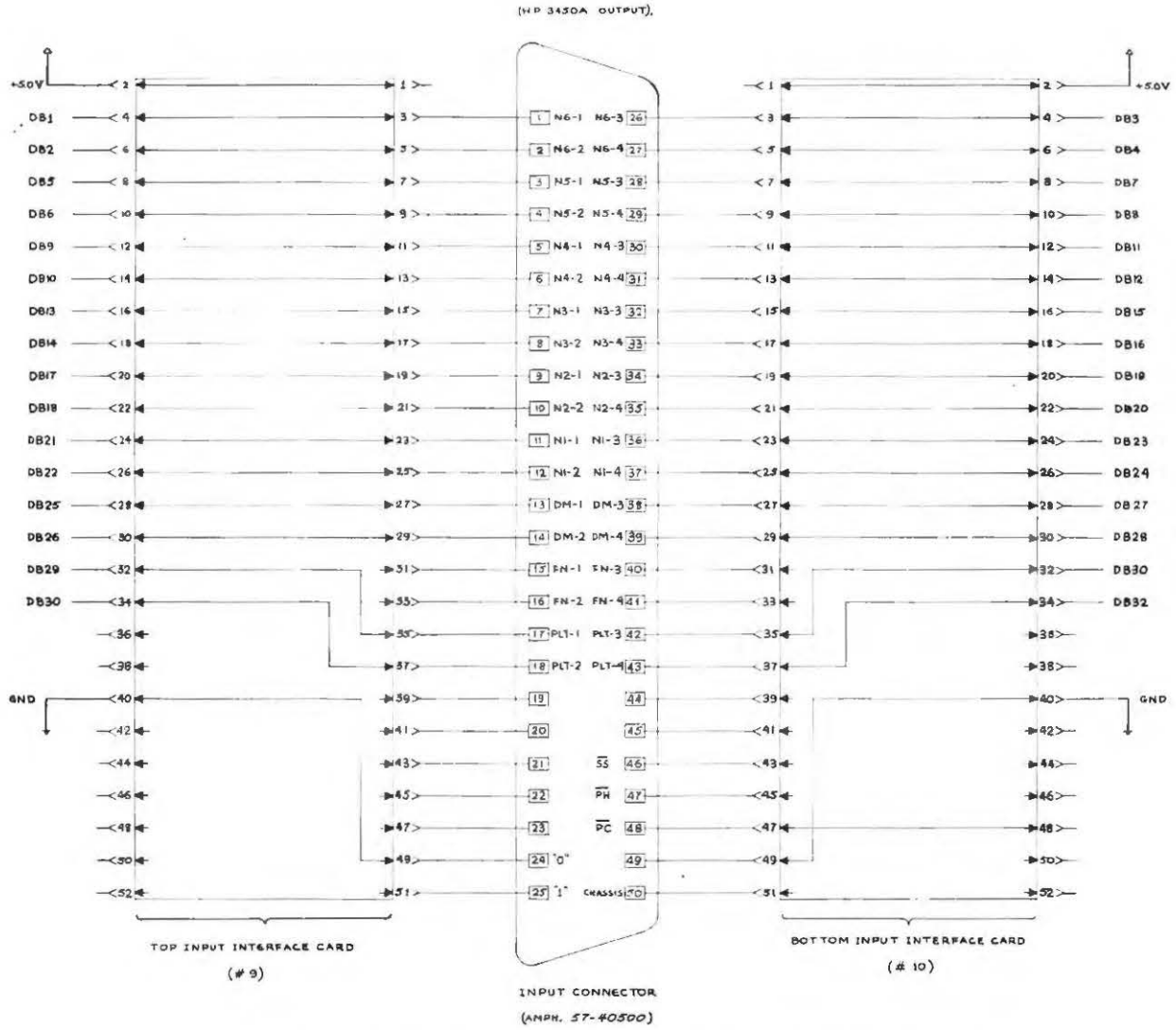

Figure A2.7b HP 3450A Input Interface Card

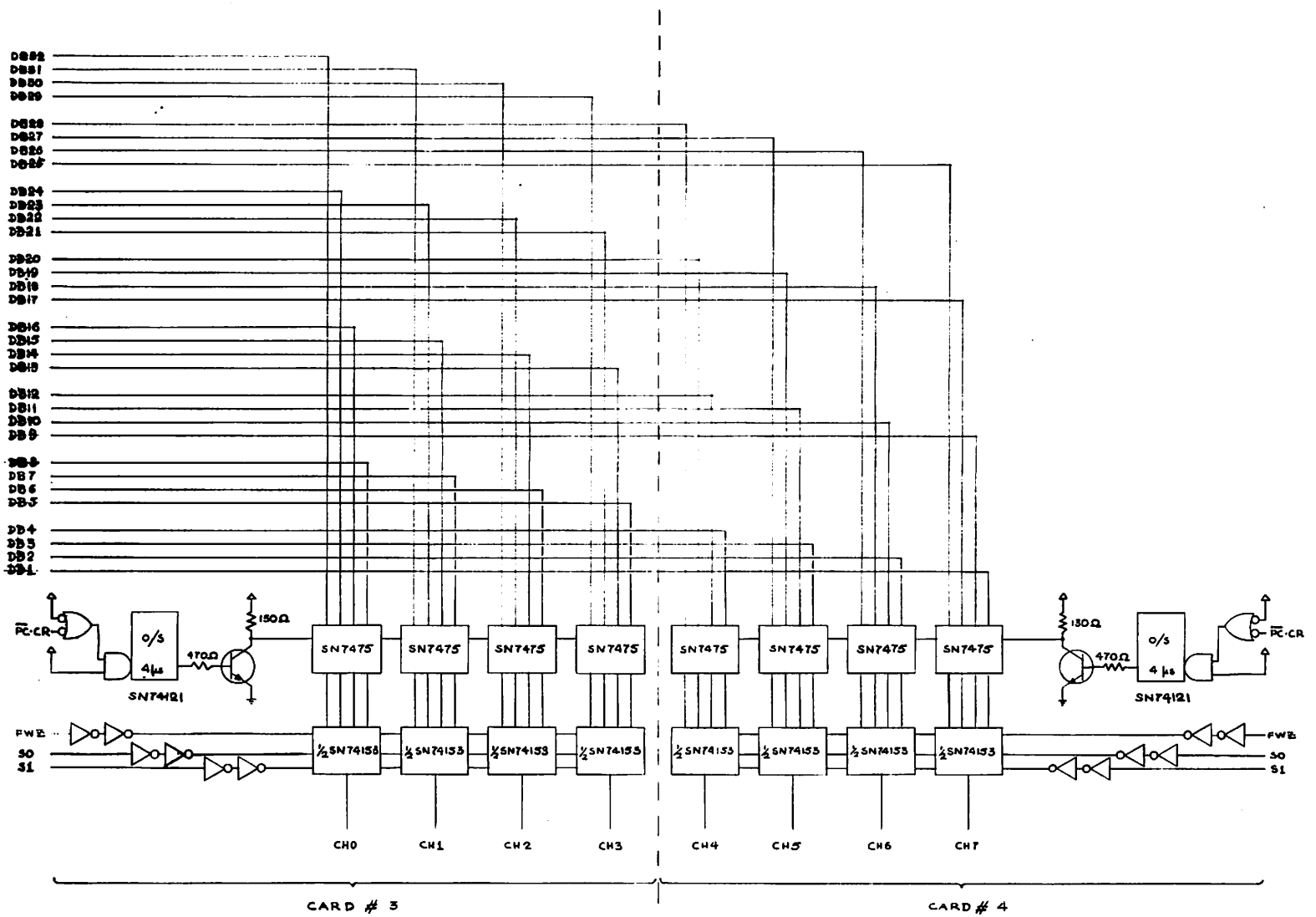

Figure A2.8 Input Latches and Multiplexers

S0 and S1 by means of one-out-of-four line selectors (SN74153) to form the four characters (bytes) on the tape.

The FWZ bit acts as a strobe and sets the output to logical 0 when a Fill With Zeros sequence is requested.

The latches are activated by a 4 μs clock pulse so that their outputs are stationary when the negative edge of PCCDT triggers the $\overline{WC}$ one shot (see figures A2.3, A2.4 and page 80).

e) Output Interface Cards (# 7 and #8).

These cards (figure A2.9) allow the user the means to patch with any combination of tape recorder input connector pin designations. In addition, the WRITE command circuit (70 μs one-shot) is mounted on these cards and the GIP (Gap in Process) output from the tape recorder is inverted to provide the AND-gate logic input for the CR (Coupler Ready) bit (see figure A2.3). The tape format that would result from a 4 byte per read-out (32 bit) output appears on figure A2.10. Note that the actual data allocation on the tape depends on the Input Interface Cards (page 90). Bit assignment indicated in parentheses corresponds to the interface cards for the HP3450A Digital Voltmeter (figure A2.7b). For pin designations of the tape recorder 36-pin connector, refer to manufacturer's manual (Kennedy 1600/360).

f) Byte Counter and Latches (Card #5)

The Byte Counter (figure A2.11) counts the outputs of one-shot A (see page 77 , figure A2.3) or the output of the external record size multiplier (item (8), page 74). The outputs of 12-bit

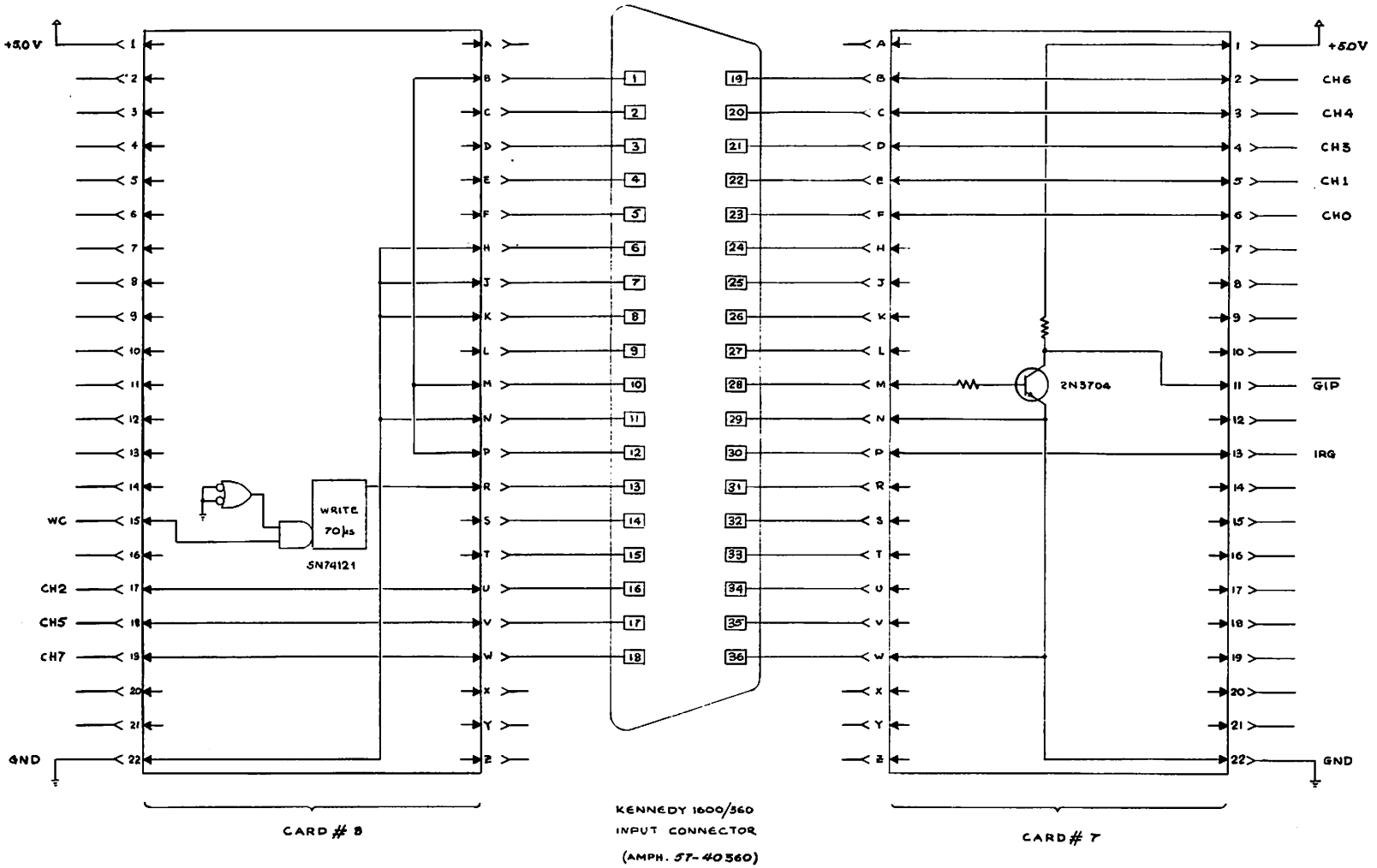

Figure A2.9 Output interface cards.

CH 0	DB32 (PLT-8)	DB24 (N1-8)	DB16 (N3-8)	DB8 (N5-8)
CH 1	DB31 (PLT-4)	DB23 (N1-4)	DB15 (N3-4)	DB7 (N5-4)
CH 2	DB30 (PLT-2)	DB22 (N1-2)	DB14 (N3-2)	DB6 (N5-2)
CH 3	DB29 (PLT-1)	DB21 (N1-1)	DB13 (N3-1)	DB5 (N5-1)
CH 4	DB28 (DM - 8)	DB20 (N2-8)	DB12 (N4-8)	DB4 (N6-8)
CH 5	DB27 (DM - 4)	DB19 (N2-4)	DB11 (N4-4)	DB3 (N6-4)
CH 6	DB26 (DM - 2)	DB18 (N2-2)	DB10 (N4-2)	DB2 (N6-2)
CH 7	DB25 (DM - 1)	DB17 (N2-1)	DB 9 (N4-1)	DB1 (N6-1)

Figure A2.10. Tape Format.

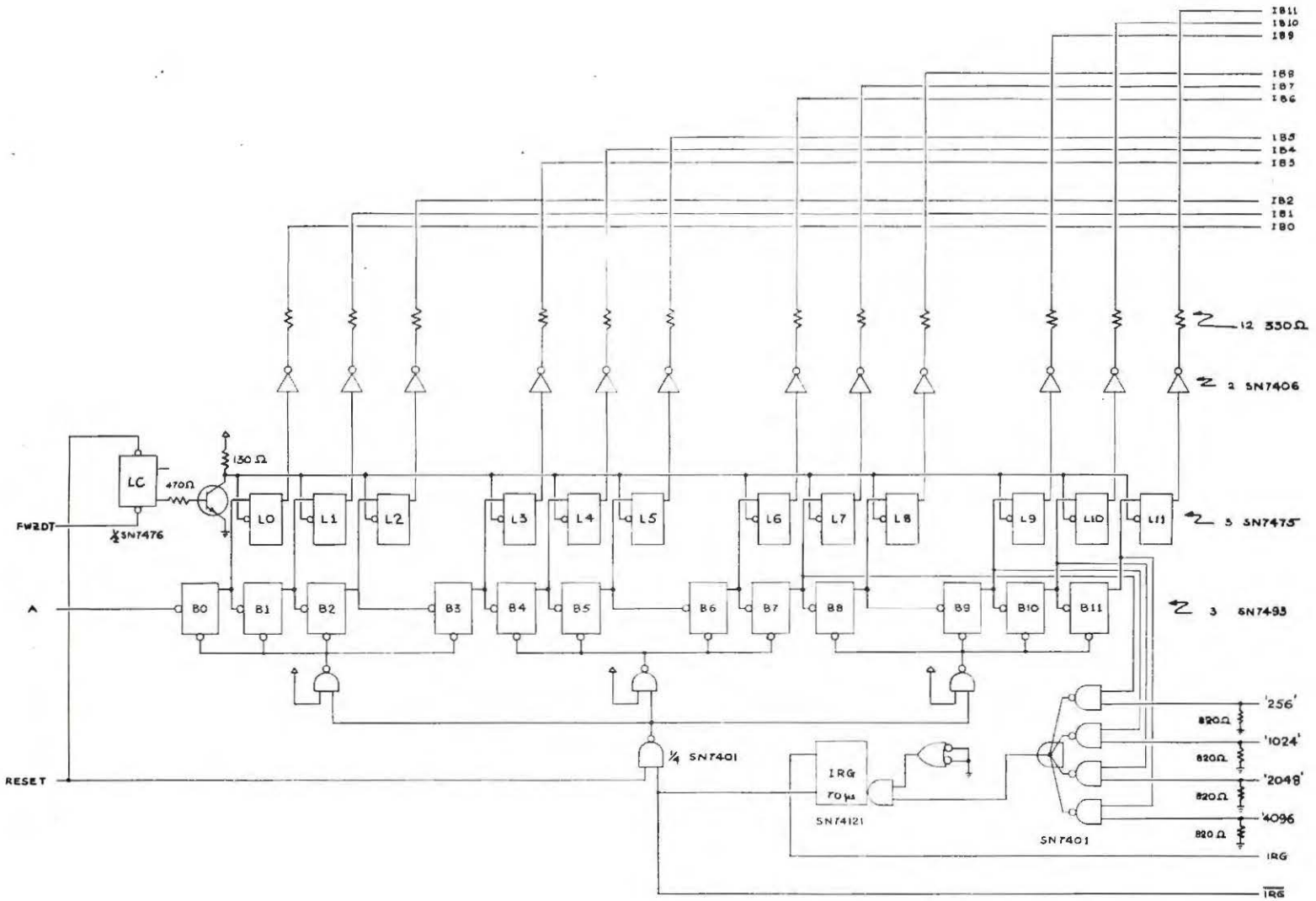

Figure A2.11 Byte Counter

Byte Counter (B0 through B11) are passed on to D type latches (SN7475) whose output tracks the input as long as the Latch Clock (LC) is high. The latches hold the Byte Counter when a FWZDT pulse comes which resets LC to zero at the beginning of a Fill With Zeros sequence. It is set to logical 1, after the end of the record, with the RESET button on the front panel.*

Record size is determined by the IRG one-shot which tries to write a record gap and reset the Byte Counter by the enabled output from the corresponding storage on the Byte Counter. This is, in turn, selected by the RECORD SIZE switch on the front panel (item (4), page 68).

g) Record Counter (Card #6)

The Record Counter (figure A2.12) counts the IRG pulses that are sent to the Tape Recorder. Its 12-bit output is displayed on the front panel in a fashion similar to the Byte Counter. It is reset with the CLEAR button on the front panel. This counter does not participate in the logic of the Coupler. It is provided for the user's aid in keeping a tape log and, in the future, for the INTERNAL DATA (item (2), page 72).

h) Power Supply (Card # 0)

The + 5.0 v D.C. power supply utilizes the μA723 voltage regulator integrated circuit with a N-P-N P-N-P bypass power transistor combination (see figure A2.13).

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* The outputs of the latches are inverted with open-collector inverters (SN7406) which are connected to the Light Emitting Diodes (LED's) through 330Ω in series with the +5.0 volt supply.

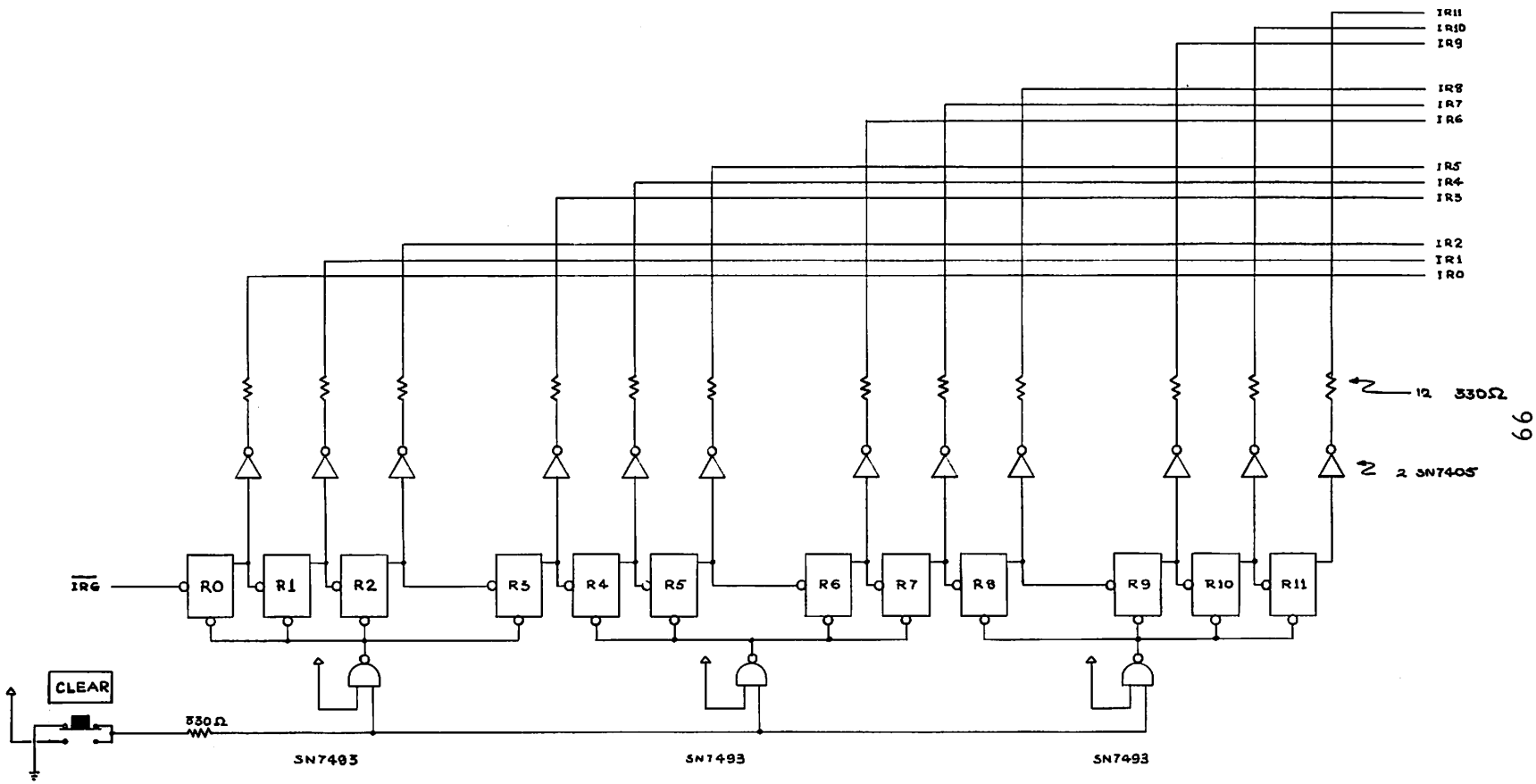

Figure A2.12 Record counter.

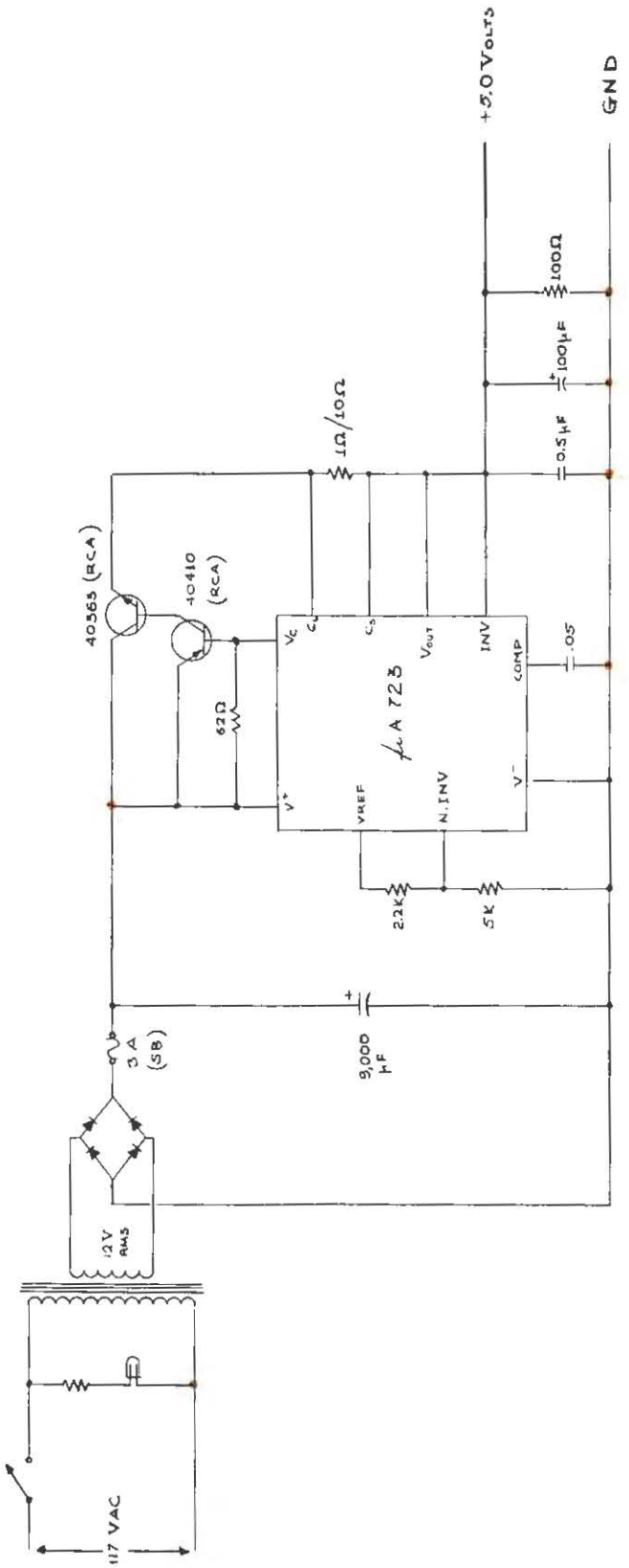

Figure A2.13 Power supply.