Synthesis of PWM Dc-to-Dc Power Converters

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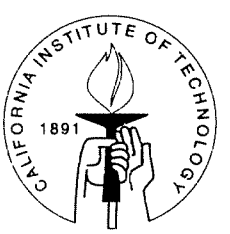

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to my parents Ting-Yang Zhou and Pian Fei

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Abstract

A novel systematical synthesis method of PWM dc-to-dc converters is established in this thesis. The new method can generate converters in an efficient way, with clear circuit insight.

The family of PWM dc-to-dc converters is defined to include converters with multiple-input and/or multiple-output; converters with arbitrary switched networks in each switching period; and converters with loops consisting only of capacitors and possibly a voltage source or cut-sets consisting only of inductors and possibly a current source in the individual switched networks.

This method is based on the equivalent ac and dc circuits of a PWM dc-to-dc converter, which consist only of switches in the converter.

The first part of the synthesis procedure is carried out without the participation of reactive elements. For a given number of switches and other requirements, the ac topology and its control sequence can be decided. Basic properties of ac and dc circuits are derived. Moreover, the topological relation between an ac circuit and its *associated* dc circuits is discovered. Based on the volt-second and ampere-second balance equations of the ac circuit and the matrix representation of dc circuits, a formalized dc model in terms of average switch voltages and currents is first developed. Consequently, the dc conversion ratio and switch implementation can be derived for each pair of ac and dc circuits. The associated dc circuits of the given ac circuit can be formally generated and sorted out according to the required dc conversion ratio, the types of switches, the order of the dc circuit, and other properties.

The insertion procedure for reactive elements is also formalized. The basic procedure generates the converters with the minimum number of inductors and capacitors. A modification of the basic procedure is given to generate converters with continuous input and output currents.

Different classes of converters are generated by the new synthesis approach. A class of three-switch converters are discovered, each of which has a loop of capacitors and possibly the voltage source. Some of these three-switch converters are of special practical interests.

Also, a class of three-switch, and two-output converters are discovered that can provide opposite polarity output voltages without using a transformer.

Most importantly, this systematic synthesis method provides an analytic and circuit-oriented approach to develop new converter topologies in order to meet new requirements introduced by ever growing number of applications.

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Chapter 1 Introduction

The function of power converters is to convert electrical energy from one voltage, current, or frequency to a different voltage, current, or frequency. As the size of electronic systems began to reduce dramatically several decades ago, it became obvious that bulky linear power processing would have to be replaced by much more efficient and smaller switched-mode power processing with modern power semiconductors. Depending on the form of input and output waveforms, power converters are classified as dc converters (dc-to-dc), inverters (dc-to-ac), rectifiers (ac-to-dc), and cycloconverters (ac-to-dc).

This thesis is focused on switched-mode dc-to-dc converters. The widespread applications of dc-to-dc converters include dc power supplies, battery chargers, solar cell regulators, and dc motor drivers. Also, the function of ac-to-dc conversion can be achieved by preceding a dc-to-dc converter with a simple rectifier and a possible filter. Moreover, dc-to-ac and ac-to-ac power converter systems frequently use ac-to-dc and dc-to-dc power conversion networks as basic building blocks. Some inverters (e.g., lamp ballasts) can be developed from a dc-to-dc converter by replacing the output low-pass filter with band-pass filter (often called matching resonant network).

The constant demand for lighter, more efficient and space-saving power converters has provided the impetus to the research work in switched-mode conversion technology. The increasing number of applications often introduce new requirements, which motivate the search for more suitable converter topologies. The conventional way to develop new converters is through circuit manipulations based on the known converters. The frequently used circuit techniques include cascade, cascode, rotation of source and load terminal designations, and transformation by duality theorem. These approaches are intuitive rather than analytic. It is always difficult to know whether the search is complete for a given complexity and other requirements. With the considerable maturity of power conversion principles in the past decade, the synthesis of power converters has been carried out in an analytical way. Successful efforts in this direction have led to the establishment of a systematic synthesis procedure for generation of PWM dc-to-dc converters, which was initiated in [3], and culminated in [5]. The term "PWM" (pulse-width modulation), is used to

distinguish "conventional" converters from resonant or quasi-resonant converters. A PWM converter, for the present purposes, is a converter with approximately rectangular (often called quasi-square) waveforms. Based on the rigorous definition of PWM converter networks, the synthesis of complete classes of PWM dc-to-dc converters is accomplished in an elegant and rigorous way in [5]. However, some classes of converters that are of important practical interests are excluded because of the assumption that there can neither be loops consisting only of capacitors and a possible voltage source, nor cut-sets consisting only of inductors and a possible current source in each switched-network of a PWM converter. Also, the complexity of the synthesis procedure in [5] directly depends on the number of switched networks during each switching cycle. Only the synthesis of converters with two switched-networks is carried out in [5]. For converters with more than two switched-networks, the synthesis procedure becomes extremely involved if not impossible.

Based on the conceptions of ac and dc equivalent circuits of PWM converters [17], a new systematic synthesis approach is developed in this thesis, which removes the aforementioned restrictions and generalizes the family of PWM dc-to-dc converters to include multiple-input, multiple-output dc-to-dc conversion networks.

In Chapter 2, fundamentals of PWM dc-to-dc power converters are reviewed. A generalized family of PWM dc-to-dc converters is formally defined. The ac and dc equivalent circuits of PWM converters are introduced. Basic properties of the ac and dc circuits are uncovered. The dc model of a PWM converter is established based on the ac and dc circuits of the PWM converter. The role of switches and the feature of power flow in PWM converters are discussed.

In Chapter 3, the previous synthesis approaches are reviewed. Then, based on the results of Chapter 2, a new systematic synthesis method is introduced.

Synthesis of two-switch converters is present in Chapter 4. Although all of these converters were previously found in [1, 5], the purpose of this chapter is to demonstrate the feature of the new synthesis procedure by use of familiar converters.

In [5], neither loops consisting of capacitors and possibly the voltage source, nor cut-sets consisting of inductors and possibly the current source are allowed in any of the individual switched networks. This restriction is removed in the new synthesis method. In Chapter 5, an interesting class of converters is discussed in detail - with three switches and a loop of capacitors and possibly the input voltage source during one time interval.

In Chapter 6, synthesis of four-switch converters is undertaken to generate converters with single transistors and desirable dc gains, which verifies the results in [5]. Furthermore, three new converters with $M(D) = \frac{D^2}{(1-D)^2}$ are discovered.

Synthesis of a group of three-switched-network converters is undertaken in Chapter 7. Since the synthesis is based on ac and dc circuits, rather than the switched networks, increasing the number of switched-networks does not aggravate the synthesis work. Chapter 8 is devoted to a class of three-switch, two-output converters, which give opposite polarity outputs without transformer.

Chapter 9 focuses on a particular three-switch converter developed in Chapter 5. This converter can operate into a capacitor-diode voltage multiplier, which offers simpler structure and control, higher efficiency, reduced EMI and size compared with traditional PWM regulated voltage multipliers. Topological extensions, dynamic analysis, soft-switching implementation and experimental verifications are given in Chapter 9.

Multiple-output converters are widely used in practice. Improvement in the cross-regulation is often achieved by use of the coupled-inductor technique. A detailed study is carried out in Chapter 10 to establish the quantitative relationship between the coupled-inductor parameters and the degree of the cross-regulation improvements. The effect of the coupling coefficient on the dynamic responses is also examined. An explicit design procedure of the coupled inductors is presented. Theoretical results are verified by computer simulations and experimental data.

Finally, important results presented in this thesis are summarized in Chapter 11.

Notations will be used in the following ways: capital letters represent average or dc quantities, small letters represent instantaneous quantities, and letters with boldface type represent vectors or matrices.

Chapter 2 Fundamentals of Ac and Dc Circuits of PWM Dc-to-Dc Converters

The aim of this chapter is to establish a framework for implementation of a systematic synthesis procedure in Chapter 3.

The class of dc-to-dc converters is defined in Section 2.1. The definition and basic principles of PWM dc-to-dc converters are discussed in Section 2.2, which is an extension based on the definition in [5]. The ac and dc equivalent circuits of PWM converter are introduced in Section 2.3.

Some general topological properties of ac and dc circuits are addressed in Section 2.4: Proposition 2.2 through 2.6.

The volt-second and ampere-second balance equations in terms of average switch voltages and average switch currents are introduced in Section 2.3. For two-switched-network converters, the balance equations can be explicitly linked to the ac topology, as in Section 2.5.1. The balance equations, together with the algebraic representation of the dc topology, can be used to generate a general dc model of PWM converters in Section 2.5.2. The topological connection between ac and dc circuits is given in Proposition 2.6. The dc conversion ratio, and average voltage and current of each switch can be derived from the dc model. The switch implementation is undertaken in Section 2.6. The extension to three or more switched-network converters is discussed in Section 2.7.

Finally, Section 2.8 addresses the feature of power flow inside PWM dc-to-dc converters. A dimensionless parameter - *switch utilization ratio* is defined there, which is among the key criteria to select optimum converter topology.

2.1 Definition of Switched-Mode DC-to-DC Converters

In the most general case, a dc-to-dc converter can be a multiple-input and multiple-output electrical network. Multiple-output converters are widely used in computers and other electronic devices where more than one dc levels are required ([26] - [33], also see Chapter 8

and Chapter 10 later in this thesis). Multiple-input converters are useful to get the regulated output voltage from several input sources, such as solar array, wind generator, fuel cell and so on ([34]).

"Averaging" is frequently used in analysis of switched-mode converters. The purpose of averaging is to replace rapidly-varying waveforms with slowly-varying waveforms that contain the same low-frequency information. The average value X of a function of time $x(t)$ is defined by

$$X \triangleq \lim_{T\to\infty} \frac{1}{T} \int_0^T x(t)dt. \tag{2.1}$$

For a PWM dc-to-dc converter in the steady-state condition, waveforms inside the converter are periodic with respect to the switching cycle. The "averaging" can be calculated in one switching cycle.

$$X = \frac{1}{T_s} \int_{nT_s}^{(n+1)T_s} x(t)dt, \tag{2.2}$$

where n is any integer.

Suppose there are N_g input ports and N_o output ports. Voltage and current at each input are denoted by v_{gi} and i_{gi}; and voltage and current at each output are denoted by v_{oj} and i_{oj}. By Eq. (2.2), the corresponding dc input and output quantities are denoted by V_{gi}, I_{gi}, V_{oj}, and I_{oj}. Then, from ith-input to jth-output, the voltage converter ratio (M_{Vji}) and the current conversion ratio (M_{Iji}) are defined by

$$M_{Vji} \triangleq \frac{V_{oj}}{V_{gi}}, \tag{2.3}$$

$$M_{Iji} \triangleq \frac{I_{oj}}{I_{gi}}, \tag{2.4}$$

$$\text{where } 1 \leq i \leq N_g, \tag{2.5}$$

$$\text{and } 1 \leq j \leq N_o. \tag{2.6}$$

The following definition of a dc-to-dc converter is generalized from the definition of a single-input and single-output converter in [8].

Definition 2.1 *A N_g-input ($N_g \geq 1$) and N_o-output ($N_o \geq 1$) network consisting of switches, inductors, capacitors, dc voltage source(s) and/or dc current source(s) at the*

input(s), and LTI [1] *resistor(s) (called load(s)) at the outputs, is a dc-to-dc converter if and only if* $M_{vji} > 1$ *or* $M_{Iji} > 1$, *where* $1 \leq i \leq N_g$ *and* $1 \leq j \leq N_o$.

In practice, many converters deliver power to nonlinear and/or time-varying loads, and there are problems involving transients and stability with such loads. However, the definition of a dc-to-dc converter here allows only LTI loads in order to analyze converter topologies in a simple and well-defined way. The effects of nonlinear and/or time-varying loads can be treated separately.

In the past decade, quasi-resonant converters, and more recently, soft-switching converters were developed to shape switch voltage and current waveforms appropriately in order to reduce the switching losses. This development is motivated by the increasing switching frequency in order to satisfy the constant requirement of smaller size. Both quasi-resonant and soft-switching converters can be viewed as modifications of a PWM converter by adding resonant components and possible auxiliary switches around the switches in the PWM converter. This thesis will focus on PWM dc-to-dc converters.

2.2 Definition of PWM Dc-to-Dc Converters

2.2.1 Types of PWM Dc-to-Dc Converters

In general, each input source can be voltage or current source. Also each load can be constant voltage output if the load is in a loop with capacitors, or constant current output if the load is in a cut-set with inductors. In practical applications, a current source can be considered as a voltage source in series with an inductor. Similarly, a voltage source can be considered as a current source in parallel with a capacitor. On the load side, a current output can be converted into a voltage output by connecting a capacitor in parallel with the load; while a voltage output can be converted into a current output by placing an inductor in series with the load. Because of these simple transformations, we can focus on only one type of converters. Through out this thesis, unless otherwise specified, we shall only consider the voltage-to-voltage converters, which are of most practical interest.

[1] "LTI" denotes "linear and time-invariant."

2.2.2 Ideal PWM Dc-to-DC Converters

The term "ideal PWM converter" is usually used to refer to a converter with 100% efficiency, i.e., all the components inside the converter are lossless: capacitors and inductors have negligible parasitics; switches are ideal (zero on-voltages and instantaneous switching transitions).

The use of an idealized model in synthesizing converter topologies can be justified as follows:

1. The efficiency is usually desired to be high (above 90% in many applications), hence the parasitic elements can be ignored.

2. The transitions for each switch from on to off position and vice versa must be short compared with the switching cycle, therefore they can be assumed instantaneous.

The assumption of idealized characteristics greatly simplifies the basic dc model of a PWM converter, without significant loss of accuracy. However, in comparison of converter topologies, non-ideal elements must be taken into account to sort out most efficient choices.

The *controllable* semiconductor devices include BJT (bipolar junction transistor), MOSFET (metal-oxide-semiconductor field effect transistor), GTO (gate-turn-off thyristor), and IGBT (insulated gate bipolar transistor). However, in order to represent controllable, unidirectional current and voltage switch, the symbol of BJT is used in this thesis. For consistency, a current-bidirectional switch is implemented by a BJT and a diode in parallel; a voltage-bidirectional switch is implemented by a BJT and a diode in series; and a four-quadrant switch is implemented by two current-bidirectional switches in series or two voltage-bidirectional switches in parallel. The criteria of switch implementation will be addressed in Section 2.6.

2.2.3 Definition of PWM Dc-to-Dc Converters

A family of ideal PWM Dc-to-Dc converters is defined through five assumptions ($A1 - A5$) in [5]. Since a converter network is an interconnection of lumped elements, it can be represented by a graph G with branches named after the elements of the converter network. The definition in [5] is generalized as follows:

Definition 2.2 *An ideal dc-to-dc converter is a network N for which Assumptions A1 through A5 are satisfied:*

A1: N consists of only the following circuit elements:

1. *A set of dc voltage sources,* $\mathbf{V}_g = \{V_{gi},\ i = 1, \ldots, N_g\}$.
2. *A set of LTI load resistors,* $\mathbf{R_o} = \{R_{oi},\ i = 1, \ldots, N_o\}$.
3. *A set of LTI inductors,* $\mathbf{L} = \{L_i,\ i = 1, \ldots, N_L\}$.
4. *A set of LTI capacitors,* $\mathbf{C} = \{C_i,\ i = 1, \ldots, N_C\}$.
5. *j sets of switches,* $j \geq 2$, *such that switches belonging to the same set are on and off simultaneously during the whole switching period* T_s.

A2: Each load R_i *forms a loop with a subset of elements in* $\mathbf{C} \cup \mathbf{V}_g$.

A3: In graph G, there are neither loops consisting only of elements in $\mathbf{C} \cup \mathbf{V}_g$ *nor cut-sets consisting only of elements in* $\mathbf{L}$.

A4: G is a non-separable[2] *graph.*

A5: In graph G, there are neither loops nor cut-sets that consist only of switches that belong to the same set.

To simplify the systematic synthesis procedure of PWM converters, transformers and coupled inductors are not included in Definition 2.2. They can be treated as extensions of basic converter topologies.

Compared with the definition in [5], the family of PWM dc-to-dc converters here is extended from single-input, single-output converters to multiple-input and/or multiple-output converters, and from two-switched-network converters to converters with arbitrary number of switched-networks. Also the loops consisting only of capacitors and possible voltage source(s) are allowed in individual switched-networks, so are the cut-sets consisting only of inductors.

Assumption A2 ensures that each output voltage has relatively small ac ripple, which is a requirement for all practical dc-to-dc converters.

[2] A connected graph G is said to be *separable* if there exists a subgraph g in G such that $\bar{g}$ (the complement of g in G) and g have only one node in common. All other connected graphs are called *non-separable*.

Assumptions A3 through A5 are necessary for a converter to be implemented with a minimum number of elements. To justify Assumption A3, suppose that there is a loop in G consisting only of capacitors and possible voltage source(s), one of the capacitors is redundancy. Thus a capacitor can be removed and the values of the remaining capacitors can be adjusted properly such that operation of the converter is unaffected. Analogous argument can be made for a inductor-only cut-set. For a converter without an isolation transformer, Assumption A4 guarantees that all the elements are electrically connected and take part in power conversion. Assumption A5 makes sure that none of the switches is redundancy, since if there is a loop of switches that belong to the same set, one of the switches can be removed without affecting operation of the converter. Similarly, if there is a cut-set of switches that belong to the same set, one of the switches can be replaced by a short branch.

A converter is a network with periodically varying structure. Generally, a converter has $n(n \geq 2)$ switched-networks in a switching period T_s. Consequently, T_s can be divided into n intervals: $D_i T_s$, $i = 1, \ldots, n$, where $0 < D_i < 1$. Assume the switching frequency is constant, there are $n-1$ independent time intervals since $\sum_{i=1}^{n} D_i = 1$. The independent time ratios (D_i $i = 1, \ldots, n-1$) are called *duty ratios*. Control over the dc gain(s) is accomplished through control over the duty-ratios. Note that, the value of duty ratio(s) can be determined by independent control input(s), like the conventional PWM control, or by both quantities inside the converter and independent control input(s), such as the current-mode control. Traditionally, the term "PWM control" is used to distinguish the specified control scheme from the current-mode control; while the term "PWM converters" is used to classify a type of converter topologies which are contrasted with "resonant converters." Thus, a PWM converter only refers to the converter topology, which can use either PWM control or current-mode control.

2.2.4 Small-Ripple Assumption

For a practical PWM dc-to-dc converter, it is required to have small ripple on output voltages. Thus, low-pass filters are always required to attenuate the ac ripple resulted from switched-mode operation. Although it is not necessary to have small voltage and current ripples inside a converter, the amplitudes of the ripples are frequently limited to reduce the losses on parasitic elements, and voltage and current stresses on semiconductor

devices. The small-ripple assumption can be justified if natural frequencies of the converter are well below the switching frequency f_s. This is the same requirement for transforming the exponential matrices into their first-order linear approximations in order to derive the continuous state-space averaged model [2].

Further, in an exaggerated form of the small-ripple assumption, we can assume that T_s can be made arbitrarily small, so that capacitors can be replaced by short-circuit branches, and inductors by open-circuit branches at switching frequency. As a result, the systematic synthesis procedure and comparison of converter topologies can be greatly simplified.

The small-ripple assumption is used throughout the thesis unless otherwise specified.

2.3 Introduction of Ac and Dc Circuits

To keep track of polarities, we need to assign reference directions for both the voltage and the current. In principle, these two reference directions can be arbitrarily chosen and independent of each other. However, for convenience and consistency of discussion, *associated reference directions* (Fig. 2.2(a)) are used for the switch voltage and the switch current:

Different equivalent circuits for a PWM dc-to-dc converter at dc and ac (switching frequency and its harmonics) are introduced as follows:

For switching frequency and its harmonics, the voltage sources and filter capacitors are shorted; while the current sources and filter inductors are removed. Therefore, only switches remain in the ac equivalent circuit of a PWM dc-to-dc converter.

At dc, the filter capacitors are removed and the filter inductors are shorted. If we consider the sources and loads as external one-port elements, the *dc circuit* of the internal converter consists of only switches; while the dc equivalent circuit enclosing the external elements is called the *extended dc circuit.*

As an example, the *ac circuit* and *dc circuits* of a Sepic converter is shown in Fig. 2.1.

After we introduce the definitions of ac and dc circuits, the next question is what quantities should be used to model the switch elements inside ac and dc circuits. Under the small-ripple assumption, a PWM converter has approximately rectangular waveforms

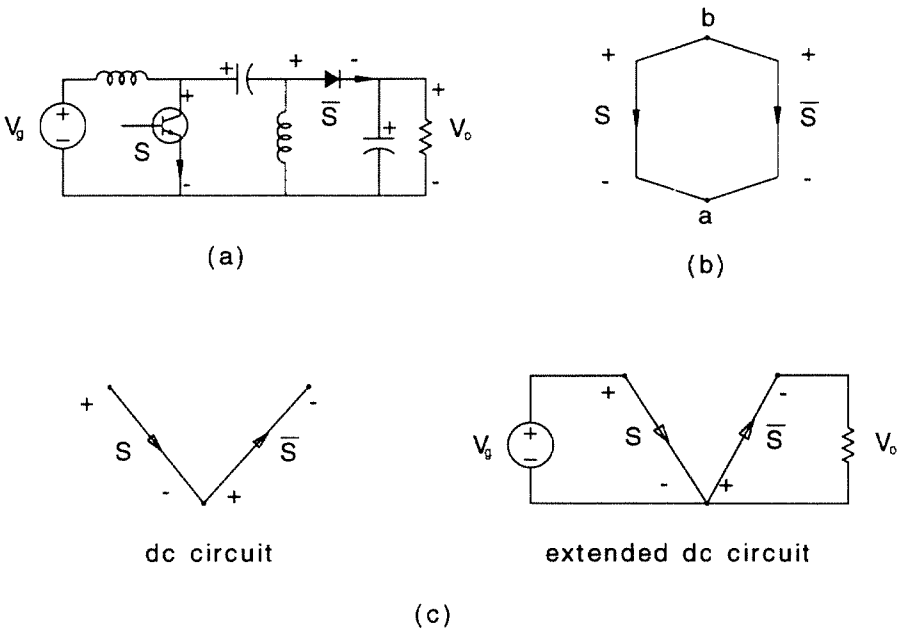


Figure 2.1: A Sepic converter (a), its ac equivalent circuit (b), its dc and extended dc equivalent circuits (c).

across its semiconductor switches. The typical voltage and current waveforms of a switch are shown in Fig. 2.2 (a) and (b). Each waveform can be separated into two parts: the first part is the average value of the voltage or current waveforms in a switching cycle: V_s or I_s; the second part is the ac voltage waveform or current waveform obtained by subtracting the corresponding dc quantity from v_s or i_s, which are shown in Fig. 2.2 (b) and (d), respectively. Since the associated reference directions are assumed, the voltage and current waveforms in Fig. 2.2 are the waveforms of a transistor; while V_s and I_s of a diode have opposite polarities.

It is obvious that a switch in dc circuit can be replaced by either a constant voltage source V_s or a constant current source I_s. It is important to note that the same dc quantities can be used to model the switch in ac circuit. In Fig. 2.2(c) and (d), when the switch is on (DT_s), the ac switch voltage equals -V_s; when the switch is off ($D'T_s$), the ac switch current equals -I_s. Therefore, the ac model for the switch can be defined as

$$\begin{cases} -V_s & \text{switch on} \\ -I_s & \text{switch off}. \end{cases} \tag{2.7}$$

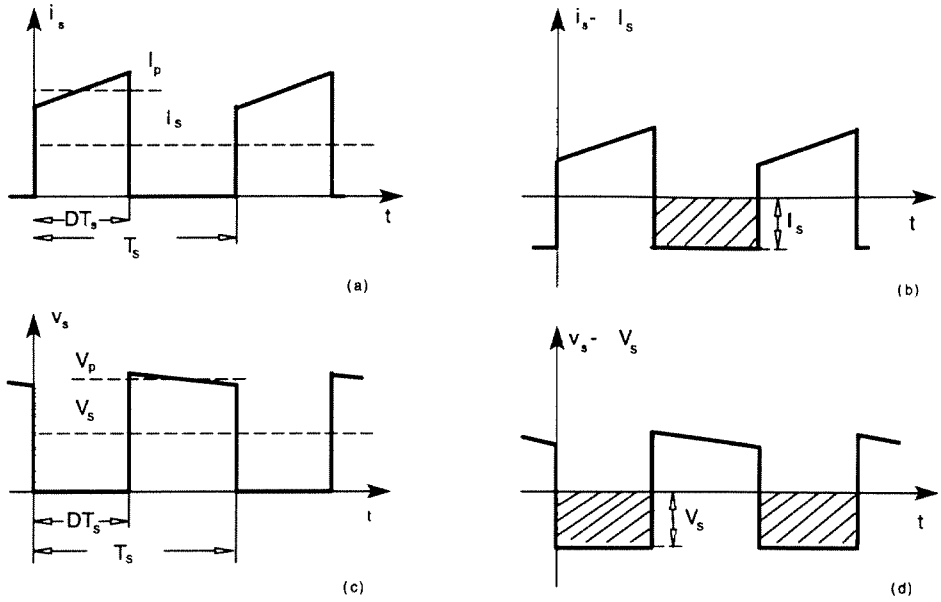


Figure 2.2: Waveforms of switch current and voltage in a PWM dc-to-dc converter with small- ripple(a) and (c), and ac components of the switch current and voltage waveforms(b) and (d).

The important feature of the aforementioned concepts is that both the ac and dc circuits are in terms of the same quantities (V_s and I_s). Based on this feature, we can further explore the relationship between ac and dc circuits and develop the systematic synthesis method later in this thesis.

Substituting the ac models for the switches into the ac circuit of the Sepic converter (Fig. 2.1(b)) yields two equivalent circuits shown in Fig. 2.3(a) and (b). In Fig. 2.3(a), S is on (modeled by a voltage source) and $\bar{S}$ is off (modeled by current source). In Fig. 2.3(b), the roles of S and $\bar{S}$ are exchanged.

As known, there is no dc value in the ac circuit. Therefore the integral of the ac voltage or current waveform of a switch in a switching cycle equals zero:

$$\begin{cases} V_s D + V_{\bar{s}} D' = 0 \\ I_{\bar{s}} D - I_s D' = 0\,. \end{cases} \tag{2.8}$$

Equation (2.8) reveals an inherent relationship between the two switches. It has the similar forms as the volt-second balance equation for an inductor and the ampere-second

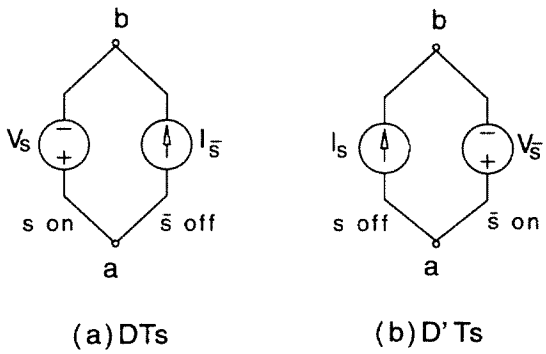


Figure 2.3: The equivalent circuit during time interval DT_s when S is on and $\bar{S}$ is off (a); and the equivalent circuit during time interval $D'T_s$ when S is off and $\bar{S}$ is on (b).

balance equation for a capacitor in a PWM dc-to-dc converter. In fact, they are just two different expressions for the same physical phenomenon. After shorting all capacitors and the voltage source in a two-switch converter, all the remaining inductors shall be in parallel with the switch pair. In other words, these inductors and switches share the same ac voltage waveform. Thus, both the ac model of the switches and the inductors should satisfy the same volt-second balance equation. Similarly, after removing all the inductors and shorting the voltage source, the only possible position for the remaining capacitor is inside the loop which contains the two switches. Since the ac current through the switches equals that through the capacitor, both are subject to the same ampere-second balance equation.

For simplification, the current and voltage waveforms of the switches in a PWM converter are assumed to have an equivalent flat-topped waveshape whose amplitudes V_p and I_p are the values at the center of the voltage and current ramps. This approximation is justified by the small-ripple assumption. V_p is called the off-voltage or voltage stress of a switch and I_p the on-current or current stress of a switch.

For the two-switch case, $V_s = D'V_{ps}$, $V_{\bar{s}} = DV_{p\bar{s}}$. Substituting these two expressions into Eq. (2.8), we have $V_{ps} = -V_{p\bar{s}}$, which means that each switch has the same off-voltage. Similarly, it can be shown that each switch has the same on-current. Therefore, switch

voltage and current stresses in a two-switch PWM converter can be denoted by V_{off} and I_{on}, respectively, as in [4].

2.4 Some General Properties of Ac and Dc Circuits

In Section 2.2, it has been mentioned that a converter network can be represented by graph G. Let G_a, G_d and G_{ed} be the graphs corresponding to the ac circuit, the dc circuit, and the extended dc circuit, respectively. G_a, G_d and G_{ed} are subgraphs of G.

Graph G_a of any non-isolated PWM converter contains only branches of switches. It has the following property:

Proposition 2.1 *In a non-isolated PWM converter:*

1. *There is no self-loop in G_a.*

2. *There is no pendant node[3] in G_a.*

Proof: If one switch branch forms a self-loop, the ac voltage of this switch is constantly zero, i.e., the voltage across the switch is a constant. If the constant is zero, the switch is always closed; otherwise, the switch is always open. In either case, it can be removed without affecting the operation of the converter. Note that, since a self-loop in a planar graph yields a pendant branch[4] in its dual graph, proof of Part 2 is actually a dual argument of that of Part 1. □

The next proposition is a direct result of Assumption A5, which gives a constraint between G_a and G_d of any PWM converter.

Proposition 2.2 *G_a and G_d of any PWM converter do not share any identical loop (or cut-set) of a set of switches which are on and off at the same time.*

Proof: If both G_a and G_d have an identical loop (or cut-set) of switches that are on and off simultaneously, G of the corresponding PWM converter has the same loop (or cut-set), which contradict Assumption A5. □

[3] A node having only one incident branch is called *a pendant node or an end node.*
[4] A branch incident on a pendant node is called *a pendant branch.*

Some General Properties of Ac and Dc circuits of Two Switch-Network Converters

Most converters in practical applications have two switched-networks per switching cycle if they are operated in the continuous inductor current mode (CICM). These converters share some important properties.

Note that, for a two-switched-network converter, there are only two sets of switches: $\mathbf{S}$ and $\bar{\mathbf{S}}$. The switches in the set $\mathbf{S}$ are on if $kT_s \leq t \leq kT_s + DT_s$ (where k is any integer.) and off otherwise. The switches in the set $\bar{\mathbf{S}}$ are on if and only if the switches in the set $\mathbf{S}$ are off.

Proposition 2.3 *In a two-switched-network converter, let G_1 (G_2) be the graphs corresponding to the switched-network when switches in $\mathbf{S}$ (or $\bar{\mathbf{S}}$) are on . Then:*

1. *There is loop(s) consisting only of capacitor(s) and possible voltage source(s) in G_1 (or G_2), if and only if, in G_a, there is loop(s) consisting only of switches in $\mathbf{S}$ (or only of switches in $\bar{\mathbf{S}}$)*

2. *There is cut-set(s) consisting only of inductors in G_1 (or G_2), if and only if, in G_a, there is cut-set(s) consisting only of switches in $\mathbf{S}$ (or only of switches in $\bar{\mathbf{S}}$)*

Proof: For the first part, if in G_a, there is a loop consisting only of switches in $\mathbf{S}$ (or $\bar{\mathbf{S}}$), by Assumption A5, these switches are in a loop with capacitor(s) and possible voltage source(s) in the corresponding converter. Thus, when the switches are on, the capacitor(s) and possible voltage source(s) are in a loop. The second part of the proposition can be proved in a dual manner. □.

Proposition 2.4 *In a two-switched-network converter:*

1. *None of the average switch voltages equals zero.*

2. *None of the average switch currents equals zero.*

Proof: The proof is quite obvious. In a two-switched-network converter, the average voltage of each switch is directly proportional to its off-voltage, which is a non-zero quantity determined by a set of capacitor voltages and/or the input voltage source. Hence, the

average voltages of switches are non-zero quantities. The proof for part two is completely analogous. □

The extended circuit of a converter is identified with the graph G_{ed}. The next property is a corollary of Proposition 2.4.

Proposition 2.5 *In a two-switched-network converter: no self-loop in G_d or pendant node exists in G_{ed}.*

Proof: According to Proposition 2.4, no branch in a two-switched-network converter has zero dc voltage or current. Hence there is no self-loop in G_d or pendant node in G_{ed}. □

In general, Propositions 2.4 to 2.5 can not be applied to three or more switched-network cases. This can be illustrated by the example of the three-switched-network (3SN) Ćuk converter, which was first introduced in [14]. The converter and its three distinct switched networks are shown in Fig. 2.4(a)-(d). The additional switch S_2 provides the second control variable, which can be used for multiple-output and unity power factor applications. As shown in Fig. 2.5, the current waveform of S_2 is divided into three parts:

$$i_{S2} = \begin{cases} -I_o & S_1 \text{ and } S_2 \text{ are on, } S_3 \text{ is off.} \\ 0 & S_1 \text{ and } S_3 \text{ are on, } S_2 \text{ is off.} \\ I_g & S_2 \text{ and } S_3 \text{ are on, } S_1 \text{ is off.} \end{cases} \tag{2.9}$$

Unlike the two-switched-network cases, S_2 here is *on* in two time intervals per switching cycle and has opposite polarity on-currents. The average current I_{S_2} equals zero since the positive ampere-second accumulation is canceled by the negative part. Physical explanation is the charge balance of the energy transfer capacitor, which is in series with S_2.

Dual argument can be used for voltage. Therefore, for three or more switched-network converters, some of the switches may have zero average voltage or zero average current.

2.5 Algebraic Representations of Ac and Dc Circuits

In the present and next sections, we will focus on two-switched-network converters. The extension to the general case will be discussed in Section 2.7.

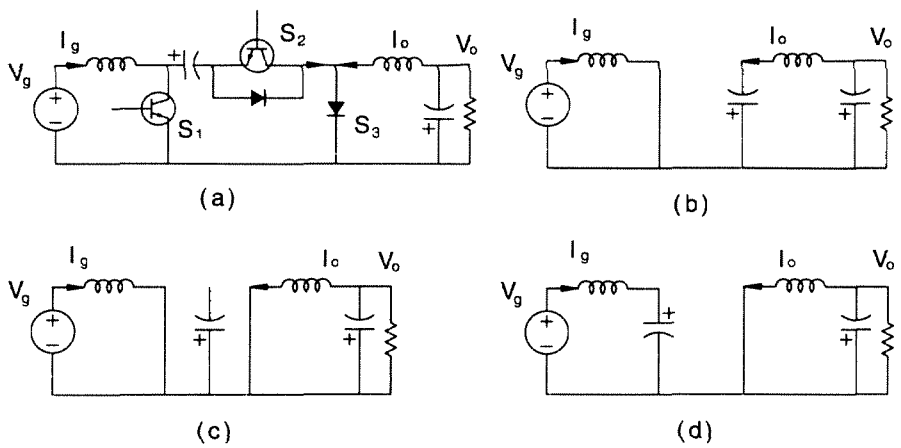


Figure 2.4: The 3SN Ćuk converter (a) and its three linear switched networks which occur during the intervals D_1T_s (b), D_2T_s(c) and D_3T_s(d). The addition of a third switched network makes available a second control input.

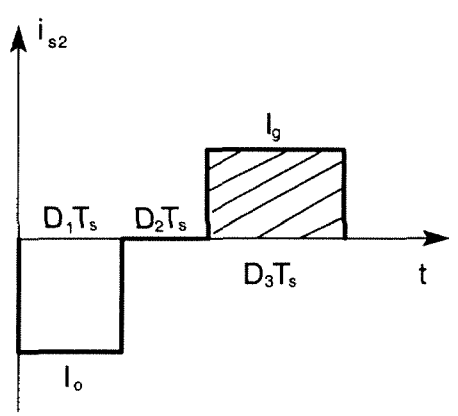


Figure 2.5: The current waveform for S_2.

2.5.1 Algebraic Representation of Ac Circuit

Following the definition in Section 2.2, ac circuit topology can be represented by the connected graph G_a, in which each branch is labeled as an element from the set $\mathbf{S}$ or $\bar{\mathbf{S}}$. Suppose G_a has n_{ta} nodes, and b branches. From fundamental graph theory, any tree T_a of graph G_a has $n_a = n_{ta} - 1$ *tree branches*, and the $l_a = b - n_{ta} + 1$ branches of G_a outside T_a are called *links (or chords)*.

Given graph G_a and an arbitrary tree T_a of G_a, the switches in the ac circuit can be divided into four sets:

1. $\mathbf{S}_t$ = a subset of $\mathbf{S}$ which are tree branches.
2. $\bar{\mathbf{S}}_t$ = a subset of $\bar{\mathbf{S}}$ which are tree branches.
3. $\mathbf{S}_l$ = a subset of $\mathbf{S}$ which are links.
4. $\bar{\mathbf{S}}_l$ = a subset of $\bar{\mathbf{S}}$ which are links.

It is obvious that:

$$\mathbf{S}_t \cup \mathbf{S}_l = \mathbf{S}\,,$$

$$\bar{\mathbf{S}}_t \cup \bar{\mathbf{S}}_l = \bar{\mathbf{S}}\,.$$

Applying KVL to each fundamental loop, we obtain a set of l_a linearly independent equations as follows:

$$\begin{bmatrix} \mathbf{v}_{sl} \\ \mathbf{v}_{\bar{s}l} \end{bmatrix} = -\mathbf{F}_a^{l_a \times n_a} \begin{bmatrix} \mathbf{v}_{st} \\ \mathbf{v}_{\bar{s}t} \end{bmatrix} = - \left[\begin{array}{c|c} \mathbf{F}_{lt} & \mathbf{F}_{l\bar{t}} \\ \hline \mathbf{F}_{\bar{l}t} & \mathbf{F}_{\bar{l}\bar{t}} \end{array}\right] \begin{bmatrix} \mathbf{v}_{st} \\ \mathbf{v}_{\bar{s}t} \end{bmatrix}\,. \tag{2.10}$$

The matrix $\mathbf{F}_a$ is partitioned into four submatrices, which relate the instantaneous voltages of $\mathbf{S}_l$ and $\bar{\mathbf{S}}_l$ with the voltages of $\mathbf{S}_t$ and $\bar{\mathbf{S}}_t$, respectively.

As discussed in Section 2.3, the switches can be modeled as dc voltage sources when they are on.

$$\text{During } DT_s: \quad \mathbf{v}_{sl} = -\mathbf{V}_{sl} \text{ and } \mathbf{v}_{st} = -\mathbf{V}_{st}\,. \tag{2.11}$$

$$\text{During } D'T_s: \quad \mathbf{v}_{\bar{s}l} = -\mathbf{V}_{\bar{s}l} \text{ and } \mathbf{v}_{\bar{s}t} = -\mathbf{V}_{\bar{s}t}\,. \tag{2.12}$$

In addition, in ac circuit, the average voltage of each switch per switching cycle equals zero. Therefore, we have the following equations:

$$\int_0^{DT_s} \mathbf{v}_{\bar{s}l} dt = \mathbf{V}_{\bar{s}l} D' T_s \,, \tag{2.13}$$

$$\int_0^{DT_s} \mathbf{v}_{\bar{s}t} dt = \mathbf{V}_{\bar{s}t} D' T_s \,. \tag{2.14}$$

Integrating Eq. (2.10) during time duration DT_s and using Eqs. (2.11), (2.13) and (2.14) yield:

$$\begin{bmatrix} \mathbf{V}_{sl} \\ \mathbf{V}_{\bar{s}l} \end{bmatrix} = -\mathbf{F}_{aD}^{l_a \times n_a} \begin{bmatrix} \mathbf{V}_{st} \\ \mathbf{V}_{\bar{s}t} \end{bmatrix} = - \left[\begin{array}{c|c} \mathbf{F}_{lt} & -\frac{D'}{D}\mathbf{F}_{l\bar{t}} \\ \hline -\frac{D}{D'}\mathbf{F}_{\bar{l}t} & \mathbf{F}_{\bar{l}\bar{t}} \end{array}\right] \begin{bmatrix} \mathbf{V}_{st} \\ \mathbf{V}_{\bar{s}t} \end{bmatrix} . \tag{2.15}$$

Equation (2.15) can be rewritten as:

$$\mathbf{B}_a \mathbf{V}_s \;=\; 0 \,, \tag{2.16}$$

$$\text{where } \mathbf{V}_s \;=\; \left[\begin{array}{c} \mathbf{V}_{la} \\ \hline \mathbf{V}_{ta} \end{array}\right] = \left[\begin{array}{c} \mathbf{V}_{sl} \\ \mathbf{V}_{\bar{s}l} \\ \hline \mathbf{V}_{st} \\ \mathbf{V}_{\bar{s}t} \end{array}\right] , \tag{2.17}$$

and the matrix $\mathbf{B}_a$ has the form

$$\mathbf{B}_a = \left[\begin{array}{c|c} \underbrace{\mathbf{1}_{la}}_{l_a \text{ links}} & \underbrace{\mathbf{F}_{aD}}_{n_a \text{ tree branches}} \end{array}\right] \Big\} \, l_a \text{ loops} \,, \tag{2.18}$$

where $\mathbf{1}_{la}$ designates a unit matrix of order l_a and $\mathbf{F}_{aD}$ designates a rectangular matrix of l_a rows and n_a columns. It is obvious that the rank of $\mathbf{B}_a$ is l_a, since $\mathbf{B}_a$ includes the unit matrix $\mathbf{1}_{la}$ and has only l_a rows. Therefore we have a set of l_a linearly independent equations in terms of the b average switch voltages. Equation (2.16) is the general form of volt-second balance equations for a two-switched network converter.

Cut-set analysis is the dual of loop analysis. Applying KCL to each of the n_a fundamental cut sets, we obtain a set of n_a linearly independent equations in terms of the instantaneous switch currents. Analogous to the derivation of volt-second balance equations, there are n_a linearly independent ampere-second balance equations in terms of the b

average switch currents

$$\mathbf{Q}_a\mathbf{I}_s = 0, \tag{2.19}$$

$$\text{where } \mathbf{I}_s = \left[\begin{array}{c}\mathbf{I}_{la}\\ \hline \mathbf{I}_{ta}\end{array}\right] = \left[\begin{array}{c}\mathbf{I}_{sl}\\ \mathbf{I}_{\bar{s}l}\\ \hline \mathbf{I}_{st}\\ \mathbf{I}_{\bar{s}t}\end{array}\right], \tag{2.20}$$

and the matrix $\mathbf{Q}_a$ has the form

$$\mathbf{Q}_a = \left[\begin{array}{c|c} \underbrace{\mathbf{E}_{aD}}_{l_a \text{ links}} & \underbrace{\mathbf{1}_{na}}_{n_a \text{ tree branches}} \end{array}\right] \Big\} n_a \text{ cut sets}. \tag{2.21}$$

Obviously, $\mathbf{Q}_a$ has a rank n_a since it includes the unit matrix $\mathbf{1}_{na}$. Hence, we have a set of n_a linearly independent equations in terms of the b average switch currents. Equation (2.19) is the general form of ampere-second balance equations for a two-switched network converter.

From basic circuit theory, we have $\mathbf{E}_a = -\mathbf{F}_a^T$, and consequently,

$$\mathbf{E}_{aD} = -\mathbf{F}_{aD}^T. \tag{2.22}$$

In conclusion, for any two-switched-network converter, the volt-second balance equations correspond one-by-one to the l_a linearly independent fundamental loop KVL equations of graph G_a. Analogously, the ampere-second balance equations correspond one-by-one to the n_a linearly independent fundamental cut-set KCL equations of graph G_a.

2.5.2 Algebraic Representation of Dc Circuit and General Dc Model

The aim of this section is to show the linkage between ac and dc circuits, and to develop the dc model in terms of average switch quantities.

For the simplicity of notations, we assume input voltage sources and output loads have the same ground, which is denoted by the datum node 0 in graph G_d of the dc circuit. Suppose the number of independent voltage sources is N_g and graph G_d has $n_d + 1$ nodes (including the datum node) and b branches. We number the nodes connected with the

voltage sources from 1 to N_g, the nodes connected with the outputs from N_g+1 to N_g+N_o, and the remaining internal nodes from N_g+N_o+1 to n_d. Note that, if $N_g+N_o=n_d$, there is no internal node.

For a two-switched-network converter, by Proposition 2.5, there is no self-loop in G_d. Therefore, we can write the reduced incidence matrix $\mathbf{A}_{fd}^T$, which relates the node-to-datum voltages $\mathbf{V}$ to the average voltages of the b branches(switches) $\mathbf{V}_s$ as follows:

$$\mathbf{V}_s = \mathbf{A}_{fd}^T\mathbf{V}, \tag{2.23}$$

$$\text{define } \mathbf{V} = \left[\begin{array}{c|c|c} \mathbf{V}_g & \mathbf{V}_o & \mathbf{V}_i \end{array}\right]^T, \tag{2.24}$$

$$\text{where } \mathbf{V}_g = [V_1,\ldots,V_{N_g}]^T, \tag{2.25}$$

$$\mathbf{V}_o = [V_{N_g+1},\ldots,V_{N_g+N_o}]^T, \tag{2.26}$$

$$\mathbf{V}_i = [V_{N_g+N_o+1},\ldots,V_{n_d}]^T. \tag{2.27}$$

Substituting Eq.(2.23) into Eq. (2.16), we have:

$$\mathbf{B}_a\mathbf{A}_{fd}^T\mathbf{V}=0, \tag{2.28}$$

where A_{fd}^T is a matrix of $b\times n_d$. Define

$$\mathbf{B}_a\mathbf{A}_{fd}^T \triangleq \left[\begin{array}{c|c|c} \mathbf{H}_g & \mathbf{H}_o & \mathbf{H}_i \end{array}\right], \tag{2.29}$$

where $\mathbf{H}_g$ is an $l_a\times N_g$ matrix, and $\mathbf{H}_o$ is an $l_a\times N_o$ matrix, and $\mathbf{H}_i$ is an $l_a\times(n_d-N_g-N_o)$ matrix. We can rewrite Eq. (2.28) as

$$\left[\begin{array}{c|c|c} \mathbf{H}_g & \mathbf{H}_o & \mathbf{H}_i \end{array}\right] \left[\begin{array}{c} \mathbf{V}_g \\ \hline \mathbf{V}_o \\ \hline \mathbf{V}_i \end{array}\right] = 0. \tag{2.30}$$

In the following definition, the term "associated" is used to link a dc circuit to an ac circuit if they are equivalent circuits for at least one viable PWM converter.

Definition 2.3 *If an ac circuit and a dc circuit correspond to at least one viable PWM converter, the dc circuit is called the associated dc circuit of the ac circuit, and G_d of the dc circuit is called the associated graph of G_a of the ac circuit.*

In general, each ac circuit has a set of associated dc circuits, each of which may correspond to different viable converters.

A practically viable dc-to-dc converter must have a unique, bounded steady-state solution for the dc quantities (average voltages and currents) of the switches. This implies an important topological connection between the ac circuit and each of its associated dc circuits, which is described in the following proposition.

Proposition 2.6 *Suppose graph G_a of an ac circuit has n_a tree branches and l_a links, then graph G_d of each associated dc circuit of the ac circuit has n_d tree branches and l_d links, which can be derived as follows:*

$$n_d = l_a + N_g\,, \tag{2.31}$$

$$l_d = n_a - N_g\,. \tag{2.32}$$

Proof: Equation (2.31) follows directly from Eq. (2.30) and the requirement of a unique and bounded solution. Equation (2.32) is given by the fact that the ac circuit and its associated dc circuit have the same number of branches, i.e. $b = n_d + l_d = n_a + l_a$. □

Note that, Eq. (2.32) implies that

$$N_g \leq n_a\,. \tag{2.33}$$

If all inputs and outputs share the same ground, the number of outputs $N_o = n_d - N_g$, by Eq. (2.31), we have

$$N_o \leq l_a\,. \tag{2.34}$$

With $n_d = l_a + N_g$, and the following condition

$$det \begin{bmatrix} \mathbf{H}_o & \mathbf{H}_i \end{bmatrix} \neq 0\,, \tag{2.35}$$

the unique and bounded solution to Eq. (2.30) is found to be

$$\begin{bmatrix} \mathbf{V}_o \\ \mathbf{V}_i \end{bmatrix} = - \begin{bmatrix} \mathbf{H}_o & \mathbf{H}_i \end{bmatrix}^{-1} \mathbf{H}_g \mathbf{V}_g \,. \tag{2.36}$$

Then the average switch voltages $\mathbf{V}_s$ can be found by Eq. (2.23), and the load currents are given by

$$\mathbf{I}_o = \mathbf{G}_o \mathbf{V}_o \,, \tag{2.37}$$

$$\text{where } \mathbf{G}_o = diag(1/R_{o1}, \ldots, 1/R_{oN_o}) \,, \tag{2.38}$$

$$\text{and } 1 \leq N_o \leq n_d - N_g \,. \tag{2.39}$$

The next step is to find the dc currents for the switches and the input sources. First, we need to extend the dc circuit to include input sources and output loads. The incidence matrix for this extended dc network is

$$\mathbf{A_{ed}} = \left[\begin{array}{c|c|c} \mathbf{A}_{fd} & \mathbf{A}_g & \mathbf{A}_o \end{array} \right] , \tag{2.40}$$

where A_{ed} is a matrix of $n_d \times (b + N_g + N_o)$. Kirchhoff's circuit theory (KCL) gives

$$\left[\begin{array}{c|c|c} \mathbf{A}_{fd} & \mathbf{A}_g & \mathbf{A}_o \end{array} \right] \left[\begin{array}{c} \mathbf{I}_s \\ \hline \mathbf{I}_g \\ \hline \mathbf{I}_o \end{array} \right] = 0 \,. \tag{2.41}$$

The $n_d = l_a + N_g$ equations in Eq.(2.41), together with the n_a equations in Eq. (2.19), are used to derive the $b + N_g$ unknown current quantities. With the condition

$$det \begin{bmatrix} \mathbf{A}_{fd} & \mathbf{A}_g \\ \mathbf{Q}_a & \mathbf{0} \end{bmatrix}^{-1} \neq 0 \,, \tag{2.42}$$

the solution to Eq.(2.41) is found to be

$$\begin{bmatrix} \mathbf{I}_s \\ \mathbf{I}_g \end{bmatrix} = -\begin{bmatrix} \mathbf{A}_{fd} & \mathbf{A}_g \\ \mathbf{Q}_a & \mathbf{0} \end{bmatrix}^{-1} \begin{bmatrix} \mathbf{A}_o \\ \mathbf{0} \end{bmatrix} \mathbf{I}_o \,. \tag{2.43}$$

Here, the solution involves the inverse matrix of rank $(b + N_g)$. If the number of the switches is big (such as $b \geq 4$), the calculation is tedious. However the matrix can be reduced by using the relation $\mathbf{I}_{ta} = -\mathbf{E}_{aD}\mathbf{I}_{la} = \mathbf{F}_{aD}{}^T\mathbf{I}_{la}$.

Equation (2.41) can be rewritten as

$$\left[\begin{array}{c|c|c|c} \mathbf{A}_{la} & \mathbf{A}_{ta} & \mathbf{A}_g & \mathbf{A}_o \end{array}\right] \left[\begin{array}{c} \mathbf{I}_{la} \\ \hline \mathbf{I}_{ta} \\ \hline \mathbf{I}_g \\ \hline \mathbf{I}_o \end{array}\right] = 0 \,, \tag{2.44}$$

$$\tag{2.45}$$

which can be simplified as

$$\left[\begin{array}{c|c|c} \mathbf{A}_{la} + \mathbf{A}_{ta}\mathbf{F}_{aD}^T & \mathbf{A}_g & \mathbf{A}_o \end{array}\right] \left[\begin{array}{c} \mathbf{I}_{la} \\ \hline \mathbf{I}_g \\ \hline \mathbf{I}_o \end{array}\right] = 0 \,. \tag{2.46}$$

Suppose that

$$det \left[\begin{array}{c|c} \mathbf{A}_{la} + \mathbf{A}_{ta}\mathbf{F}_{aD}^T & \mathbf{A}_g \end{array}\right] \neq 0 \,, \tag{2.47}$$

$\mathbf{I}_{la}$ and $\mathbf{I}_g$ can be found as

$$\begin{bmatrix} \mathbf{I}_{la} \\ \mathbf{I}_g \end{bmatrix} = -\left[\begin{array}{c|c} \mathbf{A}_{la} + \mathbf{A}_{ta}\mathbf{F}_{aD}^T & \mathbf{A}_g \end{array}\right]^{-1} \mathbf{A}_o\mathbf{I}_o \,, \tag{2.48}$$

$$\text{and} \quad \mathbf{I}_{ta} = \mathbf{F}_{aD}^T\mathbf{I}_{la} \,. \tag{2.49}$$

The rank of the inverse matrix has been reduced to n_d.

So far, we have derived the dc model to find the dc conversion ratios and the average switch voltages and currents. The dc conversion ratio is an important criterion in select-

ing the desirable converters in the synthesis procedure of Chapter 3. The average switch quantities can be used to implement switches as discussed in the next section.

2.6 Implementation of Switches

For a two-switched-network PWM converter, the average voltage for each switch V_s is directly proportional to the off-voltage (V_p) across the switch. Therefore, V_s and V_p have the same polarity. Similarly, the average current for each switch I_s is proportional to and has the same polarity as the on-current (I_p) through the switch.

Since V_s and I_s for each switch can be derived as in Section 2.5, the type of the switch can be determined without knowing the positions of the capacitors and inductors in the converter.

The associated reference directions are used for the switch voltage and the switch current as assumed in Section 2.3. In practice, the switches are implemented by transistors and diodes. For a transistor, the off-voltage (V_p) and the on-current(I_p) have the same polarity, i.e., $V_s I_s > 0$. While, for a diode, the off-voltage (V_p) and the on-current(I_p) have the opposite polarity, i.e., $V_s I_s < 0$. In general, V_s and I_s are functions of the duty ratio D. The switch current or voltage may change signs during $0 < D < 1$. Each switch can be implemented in one of the following five types (Fig. 2.6):

1. $V_s I_s > 0$: the switch can be implemented as a transistor (bipolar or MOS).
2. $V_s I_s < 0$: the switch can be implemented as a diode.
3. Only I_s changes sign: the switch can be implemented as a current-bidirectional switch.
4. Only V_s changes sign: the switch can be implemented as a voltage-bidirectional switch.
5. Both I_s and V_s change sign: the switch is four-quadrant.

It is important to point out that a transistor (bipolar or MOS) can not block the opposite polarity voltage. A bipolar transistor cannot block the reverse voltage because the E-B junction has a much lower breakdown voltage than the C-B junction as a result of the very heavy emitter doping used to increase the beta. Typical E-B breakdown voltages are 5 to 20V. While a MOS transistor cannot block the reverse voltage because of the inherent body diode; a MOS transistor is, for the same reason, a current-bidirectional switch.

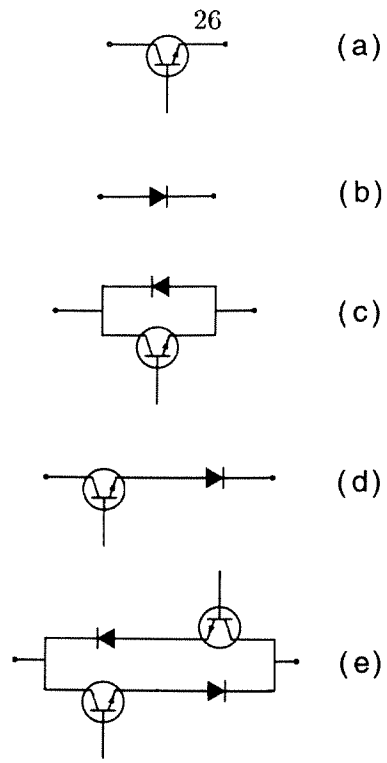


Figure 2.6: The switch can be implemented as a transistor(a); a diode(b); a current bidirectional switch(c); a voltage bidirectional switch(d); or a four-quadrant(e).

Since the polarities of V_s and I_s are dependent on duty ratio D. In some applications, instead of varying from 0 to 1, D can be restricted so that a bidirectional or four-quadrant switch can be replaced by a transistor or diode.

2.7 Extension to Converters with Three or More Switched Networks

Discussions in the last two sections have been limited to converters with two linear switched networks. Algebraic representations of ac and dc circuits are derived for these converters. The topological relation between ac and dc circuits is found as in Proposition 2.6. Finally the dc model is derived in terms of average switch quantities. In this section, we will extend the previous results to converters with three or more switched networks.

Note that, for a three or more switched-network converter, it is possible that at least one switch has zero average voltage, which means a self-loop in G_d consisted by this switch (such as in a three-switched-network buck-boost converter [13]). This case will be treated

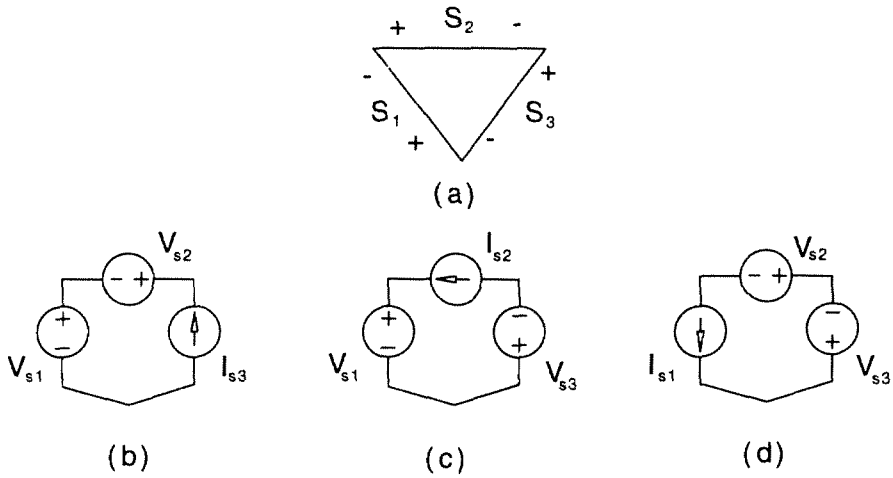


Figure 2.7: The ac circuit of the 3SN Ćuk converter (a) and its equivalent circuits during the intervals D_1T_s (b), D_2T_s (c) and D_3T_s (d).

separately in Appendix B. Here, the restriction is introduced to consider only converters without any self-loop in G_d of their dc circuit. Therefore, the l_d links of G_d are well-defined, and the incidence matrix can be used to represent G_d.

Recall that, for a two-switched-network converter, the volt-second accumulation of each switch during DT_s can be obtained either from the voltage source model Eq. (2.11), if the switch is off; or from the fact that the volt-second accumulated during DT_s must be canceled by that accumulated during $D'T_s$ (Eqs. (2.13) and (2.14)), if the switch is on. Thus, the l_a linearly independent fundamental loop KVL equations in terms of instantaneous switch voltages (Eq. (2.10)) can be rewritten one-by-one into the volt-second balance equations in terms of the average voltages: $V_{s_1}, \ldots, V_{s_b}$, as in Eq. (2.15). By duality, n_a linearly independent equations in terms of the average current $I_{s_1}, \ldots, I_{s_b}$ can be obtained.

However, these results can not be directly applied to three or more switched-network cases. The three-switched-network Ćuk converter shown in Fig. 2.4 can again be used as an example. The ac circuit of this converter and its time-varying models during the three intervals are shown in Fig. 2.7.

Each switch here is *off* in one interval and *on* in two intervals. When a switch is off, it

can be modeled by a dc current source, which is equal to the negative of the average switch current. However, the switch is subject to different on-currents in the two on-intervals. The sum of the ampere-second accumulation during the two on-intervals is equal to the multiplication of the average current and off-time. However, the two different on-currents cannot be determined individually. Consequently, there is not a one-to-one correspondence between the fundamental cut-set equation in terms of the instantaneous currents and the current balance equation in terms of the average currents, i.e., the number of independent current balance equations does not equal to the number of links l_a. Analogously, the number of independent voltage balance equations does not equal to the number of tree branches n_a.

From Fig. 2.7, the current balance equation for S_1 can be written as

$$I_{S3}D_1 + I_{S2}D_2 + I_{S1}D_3 = 0\,, \tag{2.50}$$

which can be rearranged into

$$I_{S3} = -\frac{D_3}{D_1}I_{S1} - \frac{D_2}{D_1}I_{S2}\,. \tag{2.51}$$

Also, the voltage balance equations can be written for S_2 and S_3. Simple algebraic manipulation gives

$$V_{S1} = \frac{D_3}{D_1}V_{S3}\,, \tag{2.52}$$

$$V_{S2} = \frac{D_2}{D_1}V_{S3}\,. \tag{2.53}$$

Suppose the number of linearly independent volt-second balance equations is denoted by q. It will be proved in Appendix A that the number of linearly independent ampere-second balance equations is equal to $b-q$. Here, $q=2$, which is, as predicted, not equal to $l_a(=1)$.

The voltage and current balance equations can be illustrated by an equivalent circuit shown in Fig. 2.8. The three-port network has two transformers with turn ratios in terms of the duty ratios. The voltages of the first and second ports can be expressed in terms of the voltage of third port, and the current of the third port can be expressed in the current of the first and second ports. For simplicity, we call the first and second ports *current ports*, and the third port *voltage port*.

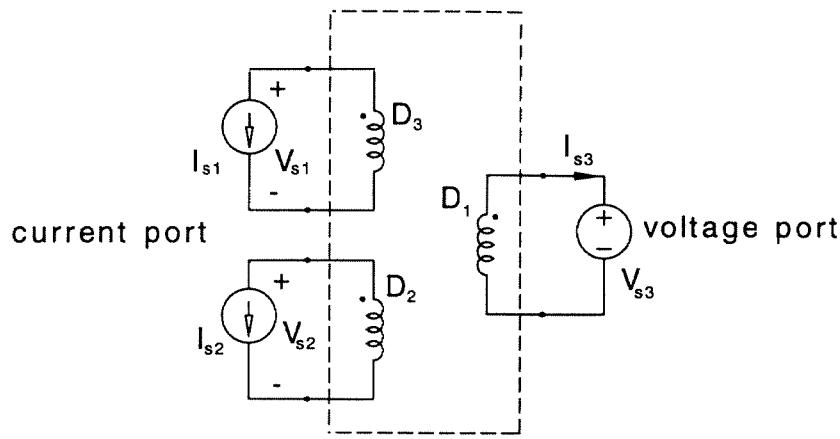


Figure 2.8: The equivalent three-port network of the ac circuit the 3SN Ćuk converter.

Generally, if we have b switches, the voltage and current balance equations of the ac circuit can be represented by a b-port network. Assume $\mathbf{V}_I$ and $\mathbf{I}_I$ to be the voltages and currents of the q current ports, and $\mathbf{V}_V$ and $\mathbf{I}_V$ to be the voltages and currents of the $(b-q)$ voltage ports. We have

$$\mathbf{V}_I = -\mathbf{H}_{12}\mathbf{V}_V\,, \tag{2.54}$$

$$\mathbf{I}_V = -\mathbf{H}_{21}\mathbf{I}_I\,. \tag{2.55}$$

Obviously, $\mathbf{H}_{12}$ is a $q \times (b-q)$ matrix, which implies q linearly independent volt-second balance equations; and $\mathbf{H}_{21}$ is a $(b-q) \times q$ matrix, which implies $(b-q)$ linearly independent ampere-second equations.

The following equation will be proved in Appendix A.

$$\mathbf{H}_{21} = -\mathbf{H}_{12}{}^T\,. \tag{2.56}$$

Compared with the results in Section 2.5.1, $\mathbf{H}_{12}$ and $\mathbf{H}_{21}$ are analogous to $\mathbf{F}_{aD}$ and $\mathbf{E}_{aD}$ there.

The topological structure of the associated dc circuits can be obtained from Proposition 2.6 with l_a replaced by q and n_a replaced by $(b-q)$.

$$n_d = q + N_g\,, \tag{2.57}$$

$$l_d = b - q - N_g\,. \tag{2.58}$$

As assumed, there is no self-loop in graph G_d, the incidence matrix of G_d can be derived. Furthermore, the results in Section 2.5.2 can be adopted here by replacing $\mathbf{F}_{aD}$ and $\mathbf{E}_{aD}$ with $\mathbf{H}_{12}$ and $\mathbf{H}_{21}$, respectively, and consequently, by replacing $\mathbf{B}_a$ with $\left[\begin{array}{c|c} \mathbf{1}_q & \mathbf{H}_{12} \end{array}\right]$, and $\mathbf{Q}_a$ with $\left[\begin{array}{c|c} \mathbf{H}_{21} & \mathbf{1}_{b-q} \end{array}\right]$.

For the known average switch voltages and currents, the switch implementation for three or more switched-network converters are not as obvious as two-switched-network converters. Since the voltage across a switch may change directions in a switching cycle, so does the current through a switch. However, under the assumption that there is no series (or parallel L-C combination), it can be proved that a switch has bidirectional voltage (or bidirectional current) in a switching cycle if and only if the average switch voltage V_s (or the average switch current I_s) is equal to zero. The physical interpretation is as follows: The voltage waveform across a switch is bidirectional if and only if the switch is in a loop with only inductor(s). Since each inductor has zero dc voltage, the dc component of the voltage waveform across the switch is zero. In a dual manner, the current waveform through a switch is bidirectional if and only if the switch is in a cut-set with only capacitor(s). Since each capacitor has zero dc current, the dc component of the current waveform through the switch is zero.

Therefore, the switch implementation of two-switched network converters in Section 2.6 can be extended to more than two-switched-network cases by adding the two additional rules:

6. $V_s = 0$: the switch can be implemented as a voltage-bidirectional switch.

7. $I_s = 0$: the switch can be implemented as current-bidirectional switch.

Note that, a series (or parallel) L-C combination is superfluous for energy transfer [5] and can be regarded as an extension of any basic converter topology. The synthesis procedure established later in this thesis shall generate only basic converter topologies. Thus, the assumption here is justified.

2.8 Power Flow and Switch Utilization Ratio of Dc-to-Dc Converters

A dc-to-dc converter is a power processing network which converts one dc voltage/current level to another dc voltage/current level in a controlled manner. In this section, we will discuss and compare the power flow patterns inside different converter topologies.

Suppose a two-terminal circuit element has $v(t)$ across it and $i(t)$ through it, and V is the average of $v(t)$ is a switching period, and I is the average of $i(t)$ in a switching period, the *dc power* and *ac power* absorbed by this circuit element are defined as follows:

Definition 2.4 *Suppose that the associated reference directions are used, the dc power absorbed by the two-terminal circuit element is the product of the average voltage V and the average current I:*

$$P_{dc} = VI\,. \tag{2.59}$$

Definition 2.5 *Suppose that the associated reference directions are used, the ac power absorbed by the two-terminal circuit element is the average of the waveform of $(v(t)-V)(i(t)-I)$:*

$$\begin{aligned} P_{ac} &= \lim_{T\to\infty}\frac{1}{T}\int_0^T (v(t)-V)(i(t)-I)dt \\ &= \lim_{T\to\infty}\frac{1}{T}\int_0^T v(t)i(t)dt - VI\,. \end{aligned} \tag{2.60}$$

The ac power is defined as the average of instantaneous power subtracted by the dc power For a PWM dc-to-dc converter in the steady-state condition, $v(t)$ and $i(t)$ are periodic to the switching cycle. The average of instantaneous power can be defined in one switching cycle.

The following important property is taken from [8]:

Proposition 2.7 *In order to convert dc power at one voltage or current level to a different voltage or current level, at least part of the input dc power has to be converted into ac power inside the converter and rectified into dc power at the output side of the converter.*

A LTI resistor cannot absorb negative dc power or negative ac power because of its basic characteristic $v(t) = Ri(t)$. Therefore, in a dc-to-dc converter, there is at least one non-linear and/or time-varying resistor to absorb at least part of the input dc power, and deliver the ac power; also, there is at least one non-linear and/or time-varying resistor to absorb ac power, and deliver at least part of the output dc power.

Since high efficiency is constantly required in power converters, semiconductor switches are used as the inevitable non-linear and/or time-varying resistors. In the following discussion, each switch is assumed to be ideal with zero loss and negligible switching transition. Therefore, the instantaneous power absorbed by a switch is constantly zero,

$$p_s(t) = v_s(t)i_s(t) = 0, \quad \text{for all } t. \tag{2.61}$$

The typical voltage and current waveforms of a transistor and a diode are shown in Fig. 2.9. Each waveform is decomposed into its dc component and ac component.

The following proposition gives the relation between P_{dc} and P_{ac}.

Proposition 2.8 *For each ideal switch, its ac power is the negative of its dc power:* $P_{ac} = -P_{dc}$.

Proof: This proposition follows Eqs. (2.61), (2.59) and (2.60) directly. □

Proposition 2.8 states that the dc power absorbed by an ideal switch equals the ac power delivered by the switch, vice versa. The next proposition illustrates the different roles played by transistors and diodes in dc-to-dc converters.

Proposition 2.9 *Suppose the switches in dc-to-dc converters are ideal:*

1. *Each transistor absorbs dc power and delivers the same amount of ac power.*

2. *Each diode absorbs ac power and delivers the same amount of dc power.*

Proof: For a transistor, $P_{dc} = V_s I_s > 0$. Thus a transistor absorbs dc power. Then by Proposition 2.8, it delivers the same amount of ac power. For a diode, $P_{dc} = V_s I_s < 0$, so

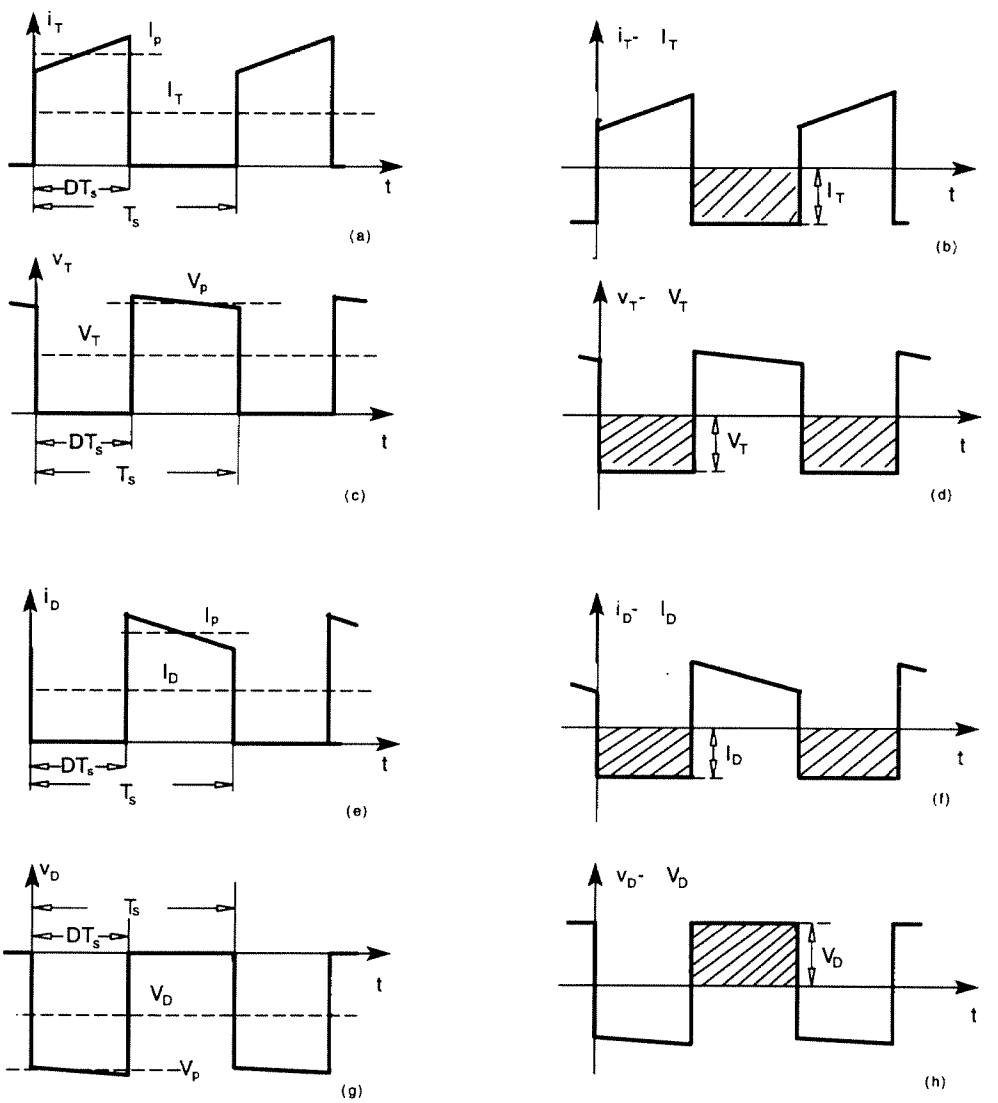


Figure 2.9: The typical voltage and current waveforms of a transistor and their corresponding dc components(a), (c) and ac components(b), (d); the typical voltage and current waveforms of a diode and their corresponding dc components(e), (f) and ac components(g), (h).

a diode delivers dc power. Again, by Proposition 2.8, it absorbs the same amount of ac power. □

A transistor can be viewed as an inverter switch which converts dc power into ac power, while a diode functions as a rectifier switch which converts ac power into dc power.

In any PWM dc-to-dc two-switched-network converter, each switch functions as a transistor or a diode for a given range of duty ratio D. In a converter with more than two switched-networks, a switch(es) may need to be voltage-bidirectional or current-bidirectional even when the duty ratio D is fixed, and as proved in Section 2.7, the average voltage V_s (or the average current I_s) of this voltage-bidirectional (or current-bidirectional) switch is equal to zero. The following property relates the dc power absorbed by all transistors in the converter with the power delivered by all diodes in the converter.

Proposition 2.10 *If a PWM dc-to-dc converter has n_T transistors (T_1 to T_{n_T}) and n_D diodes (D_1 to D_{n_D}) at the duty ratio D, the total dc power absorbed by the transistors in the converter equals the total dc power delivered by the diodes in the converter,*

$$\sum_{i=1}^{n_T} V_{T_i} I_{T_i} = -\sum_{i=1}^{n_D} V_{D_i} I_{D_i} \,. \tag{2.62}$$

Proof: The dc circuit consists of only the input sources, the output loads, the transistors and the diodes. Since the constraints imposed by Kirchhoff's voltage and current laws are satisfied, Tellegen's theorem can be applied to the dc circuit, together with the assumption of no power loss in the converter, we have

$$\sum_{i=1}^{n_s} V_{s_i} I_{s_i} = 0 \,, \tag{2.63}$$

where n_s is the number of all the switches in the converter. All the switches can be implemented by a transistor or a diode by limiting the range of duty ratio D, except those that have zero V_s or I_s. Thus, we have Eq. (2.62). □

Proposition 2.10 can be applied to dc-to-dc converters with arbitrary number of switched networks. For two-switched-network cases, since the average switch voltages and currents are directly proportional to the peak voltages and currents, Eq. (2.62) can be rewritten in terms of peak quantities, which can be approximately considered as switch stresses under the small-ripple assumption.

It is obvious that

$$V_{T_i} I_{T_i} = DD' V_{PT_i} I_{PT_i} , \tag{2.64}$$

$$V_{D_i} I_{D_i} = DD' V_{PD_i} I_{PD_i} . \tag{2.65}$$

By substituting Eqs. (2.64) and (2.65) into Eq. (2.62), we have:

$$\sum_{i=1}^{n_T} V_{PT_i} I_{PT_i} = -\sum_{i=1}^{n_D} V_{PD_i} I_{PD_i} . \tag{2.66}$$

Voltage stress and current stress of switches are the parameters that determine the choices of the semiconductor devices. Therefore, they are among the factors that decide the cost, size, and efficiency of PWM converters. For example, it is hard to find MOSFETs with low on-resistance and diodes with fast reverse recovery time at considerably high voltage ratings.

In order to compare the switch stresses for different two-switched-network converters at the same output power, we can define a dimensionless parameter.

Definition 2.6 *With $V_{oi} I_{oi}$ as the maximum rated power for the ith output, V_{PT_i} and I_{PT_i} as the peak voltage and current ratings of the transistor T_i, and V_{PD_i} and I_{PD_i} as the peak voltage and current ratings of the diode D_i, the utilization of the switches in a converter can be defined as*

$$\text{switch utilization ratio } \eta_s = \frac{\sum_{i=1}^{n_o} V_{oi} I_{oi}}{\sum_{i=1}^{n_T} V_{PT_i} I_{PT_i}} = \frac{\sum_{i=1}^{n_o} V_{oi} I_{oi}}{\sum_{i=1}^{n_D} V_{PD_i} I_{PD_i}} . \tag{2.67}$$

A similar parameter is defined in [15] to compare the utilization of switches in various single-phase inverters. In practical application, the switch utilization ratio would be much smaller than the definition because of the necessary safety margins, input variations, and ripple quantities.

Converters with one transistor and one diode are the simplest and most frequently used PWM converters. As an example, we will compare η_s in different two-switch converters and their isolation extensions.

Non-isolated converters are considered first. As proved in [5], the two switches have the same voltage stress, denoted as V_{off}; and the same current stress, denoted as I_{on}. Further,

if $M(D) = P(D)/Q(D)$ is the dc conversion ratio of a viable two-switch voltage-to-voltage PWM converter, we have

$$\frac{V_{off}}{V_g} = \frac{1}{|Q(D)|}, \tag{2.68}$$

$$\frac{I_{on}}{I_o} = \frac{1}{|Q(D)|}. \tag{2.69}$$

By Eqs. (2.67), (2.68) and (2.69), the switch utilization ratio η_s is

$$\eta_s = |P(D)|\,|Q(D)|. \tag{2.70}$$

To make a fair comparison of the utilization of switches in various non-isolated two-switch converters, we shall find η_s in terms of the dc conversion ratio M by using $D = D(M)$ in Eq.(2.70).

Buck-Type Converters

$$M(D) = D \quad Thus, \quad \eta_s = D = M. \tag{2.71}$$

Boost-Type Converters

$$M(D) = \frac{1}{D'} \quad Thus, \quad \eta_s = D' = \frac{1}{M}. \tag{2.72}$$

Ćuk, Buckboost, Sepic, Zeta, and etc.

$$M(D) = \frac{D}{D'} \quad Thus, \quad \eta_s = DD' = \frac{M}{(1+M)^2}. \tag{2.73}$$

Obviously, for the same M, buck-type (always step-down voltage) and boost-type (always step-up voltage) converters have higher switch utilization ratio than the converters which can both step-down and step-up voltage. The physical meaning of this feature is illustrated in Fig. 2.10. By Proposition 2.7, at least part of the input dc power has to be processed as ac power inside the converter. For buck-type or boost-type converters, only part of input dc power is inverted into ac power through a transistor, then rectified to dc power through a diode at the output; the remaining dc power is transferred directly to the

output without involving the switches. However, for step-up/step-down converters, all the input dc power has to be processed as ac power inside the converters and then rectified to dc power at the output. Therefore, for the same output power, step-up/step-down converters need switches with high power rating, compared with buck-type converters or boost-type converters.

This scenario changes when isolation is required. Isolation transforms are frequently used in PWM converters to provide galvanic isolation, additional step-up or step-down ratio, or multiple outputs. As known, only ac power can pass through the transformer. Since all dc power has been converted into ac power in step-up/step-down converters (Ćuk, buckboost, sepic ...), isolation can be obtained either by splitting an energy transfer capacitor and inserting an ideal ac transformer in between, or by replacing an inductor with a transformer. Both cases will not increase the number of switches or the stresses of the original switches. Therefore, the switch utilization ratio η_s keeps the same . However, in the buck or boost converter, only part of the input dc power has been converted into ac power. Thus, the number of the switches and/or the ratings of the original switches need to be increased to convert the remaining dc power into ac power, which can pass through the isolation transformer.

Next, the common buck-derived isolation converters are used to illustrate this phenomenon. All the converters are shown in Fig. 2.11.

For a converter with an isolation transformer, the maximum duty ratio D_{max} can be chosen to reduce the switch stresses and increase η_s, while the turns ratio of the transformer is determined by the required conversion ratio and the chosen duty ratio. Therefore, only the maximum available η_s is of practical importance and will be compared among different converter topologies. Since the turns ratio of an isolation transformer will not affect the power ratings, it is assumed to be 1:1 for simplicity of notation. The duty ratio D is defined as $\frac{T_{on}}{T_s}$, with T_{on} the on-time of each transistor.

In the single-ended forward converter, the current stress of the transistor is the same as in the buck converter; while the voltage stress depends on the reset scheme. A low reset voltage can reduce the voltage stress, with the compromise of lower maximum available duty ratio. If the turns of reset winding N_r is chosen to equal N_p, the off-voltage stress (exclusive of the leakage spike) is twice of the input voltage and the available D_{max} is 0.5.

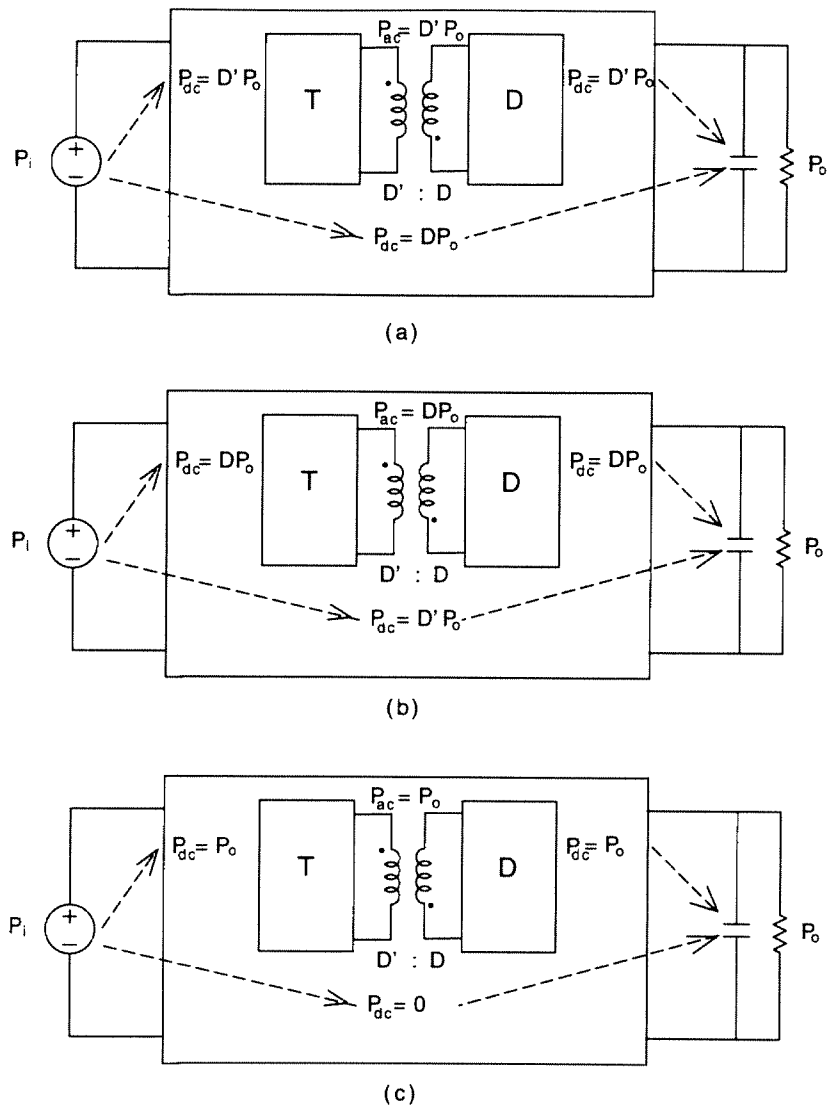


Figure 2.10: Power process in a buck-type converter(a), in a boost-type converter(b) and in a step-up/step-down converter(c) (assume $P_i = P_o$).

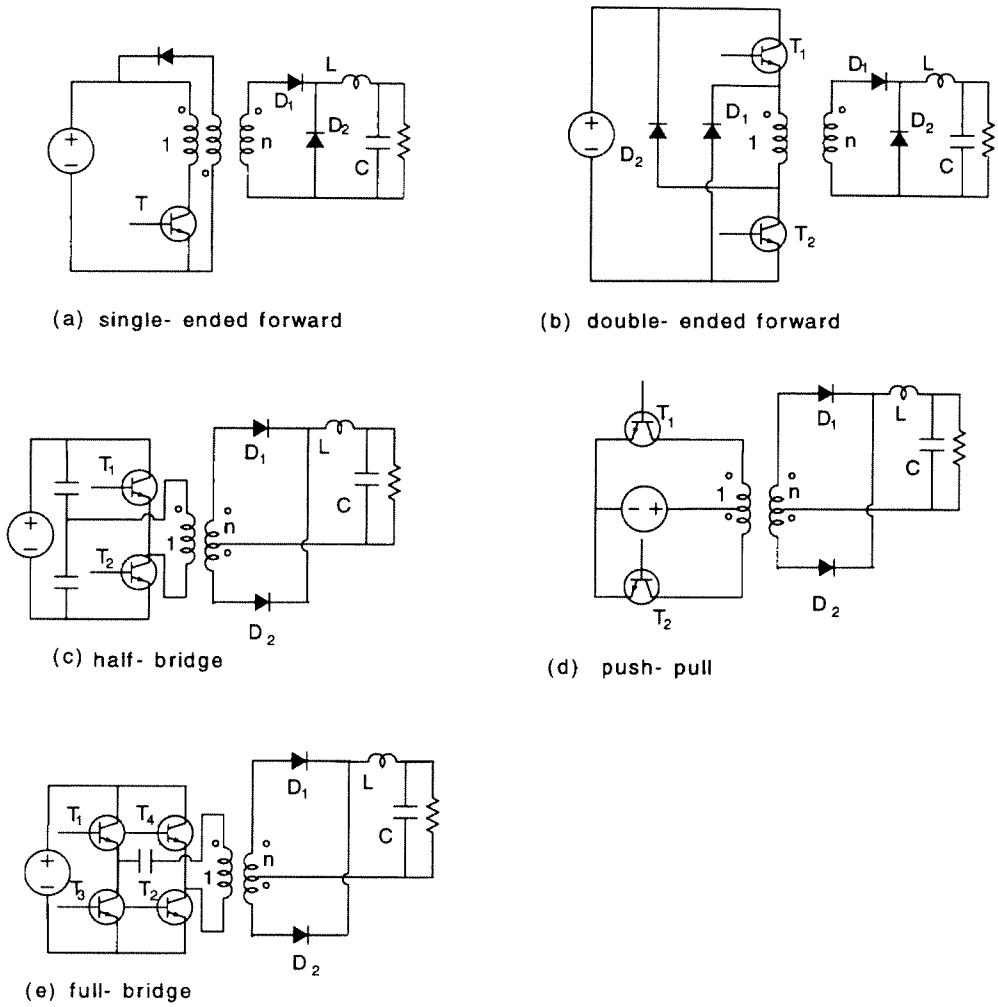


Figure 2.11: The common buck-derived isolated converters: the single-ended forward converter(a), the double-ended forward converter(b), the half-bridge converter(c), the push-pull converter(d), and the full-bridge converter(e).

Thus

$$\eta_s = \frac{D}{2} \leq 0.25\,. \tag{2.74}$$

In fact, it can be proved that the switch utilization ratio η_s of each of the other four converters in Fig. 2.11 has the same expression and upper bound as in Eq.(2.74).

The switch utilization ratio η_s of the step-up/step-down converters keep the same as in Eq. (2.73), with the same maximum value of 0.25 at $D = 0.5$. However, the isolation is easier to implement in step-up/step-down converters since no additional switch is needed.

It is worth pointing out that the switch utilization ratio is only one of the parameters that can be used to compare different converters. The choice of a particular converter topology also depends on other criteria.

For example, both the double-ended forward and half-bridge converters have the same switch stresses and the same η_s. However, the main difference between these two converters is that the half-bridge provides a full-wave output instead of a half-wave one in the forward converter. Hence, the half-bridge converter requires a smaller LC output filter, which places it in a favorable position.

Another case is to compare the half-bridge and full-bridge converters. As mentioned before, the maximum η_s of the full-bridge is the same as that of the half-bridge. However, the practical semiconductor devices have limited peak voltage and current ratings. If using the same transistors, the maximum available output power of the full-bridge is twice of that of the half-bridge. Thus, in the high power application, we shall consider the full-bridge topology.

Notice that, in the above discussion, we have divided the two-switch converters into two groups. While converters in the first group keep the same switches when extended to the isolated versions; those in the second need to increase the number of switches and/or the ratings of the original switches in order to implement isolation. A more general statement is given as follows:

Proposition 2.11 *For a PWM converter with arbitrary number of switches: If graph G_{ed} of the extended dc circuit of the converter is separable and if there is no loop in G_{ed} containing both input and output branches, then the isolation can be implemented without increasing the number or the ratings of the original switches.*

Proof: Since G_{ed} is separable with no loop enclosing both input and output branches,

there is no dc power transferred directly to output. All the power flowing to output is first converted into ac power. Therefore, the isolation transformer(s) can be inserted without adding a new switch or increasing the ratings of the original switches. □

Chapter 3 Introduction to Synthesis of PWM Dc-to-Dc Converters

Based on the results of Chapter 2, a systematic synthesis procedure for PWM dc-to-dc converters is developed in this chapter. The idea of reducing systematic synthesis of converter topologies to systematic generation of their matrix representations was originated in [3], where the fundamental loop matrices were used to represent the corresponding switched networks. There are several main drawbacks of this approach: First, there is not a one-to-one correspondence between the switched network and its fundamental loop matrix. Consequently, the converters generated are incomplete. Second, the switches are not taken into account explicitly and could not be inserted systematically into the chosen switched networks. Moreover, some fundamental loop matrices may not represent realizable converter networks. All these problems were eliminated in [5], where incidence matrices were chosen to represent the different switched networks. Since the incidence matrices give the exact position of the circuit elements, it is easy to construct only those that represent realizable networks and implement. This synthesis method is briefly reviewed in Section 3.1.

A different approach is used in this thesis. Instead of constructing incidence matrices for all possible pairs of switched networks and comparing each pair of incidence matrices to insert the switches, we enumerate all possible dc circuit topologies for a given ac circuit, and insert the necessary inductors and capacitors by comparing the incidence matrices of G_a and G_d.

3.1 Review of the Previous Synthesis Method [5]

In addition to the assumptions made in Chapter 2, the family of PWM dc-to-dc converters in [5] is subjected to the following restrictions:

1. A single dc voltage source, and a single LTI load resistor.

2. Two switched networks in each switching cycle.

3. There are neither loops consisting of capacitors and possible voltage source, nor cut-sets consisting of inductors and possible current source in any switched network.

Graph G of the converter reduces to graph G_1 (G_2) when switches in $\mathbf{S}$ ($\bar{\mathbf{S}}$) are on. Graphs G_1 and G_2 are represented by the corresponding incidence matrices $\mathbf{H}_1$ and $\mathbf{H}_2$. The synthesis of complete classes of converters is equivalent to the enumeration of all possible pairs of incidence matrices: $\mathbf{H}_1$ and $\mathbf{H}_2$.

The synthesis procedure starts by selecting the number of inductors and capacitors, then the positions of reactive elements are enumerated and the corresponding pairs of incidence matrices ($\mathbf{H}_1$, $\mathbf{H}_2$) are generated.

Under the small-ripple assumption, a general dc model of a PWM converter follows from the *state-space averaging* analysis method [2]. The dc model can be expressed in the fundamental loop matrices of the converter [3]. Since the fundamental loop matrices can be found from the incidence matrices $\mathbf{H}_1$ and $\mathbf{H}_2$, the dc model can be utilized in the synthesis procedure after knowing the incidence matrices.

The degree of the dc conversion ratio can be defined as follows:

$$\deg M(D) \triangleq \max(\deg P(D), \deg Q(D)) . \tag{3.1}$$

The pair ($\mathbf{H}_1$, $\mathbf{H}_2$) is considered *non-degenerate* if and only if the corresponding dc model equations have a unique, bounded steady-state solution and $\deg M(D) \geq 1$.

After elimination of the redundant and degenerate cases, the minimum number of ideal switches can be inserted by comparing the incidence matrices $\mathbf{H}_1$ and $\mathbf{H}_2$. Furthermore, the off-voltage and on-current of the switches can be determined from the dc model. Consequently, the switches can be implemented by appropriate semiconductor devices.

It has been shown that given a pair of ($\mathbf{H}_1$, $\mathbf{H}_2$), graph G of the converter (with minimum number of switches) is *unique* if and only if switches in $\mathbf{S}$ ($\bar{\mathbf{S}}$) do not form a path of length greater than one.

A set of properties, such as the dc conversion ratio $M(D)$, the number of switches, the number of transistors, continuous input and/or output current, and possible coupling of inductors, can be chosen as criteria of sorting out the converters.

This synthesis approach provides an elegant and rigorous way to generate *complete* classes of converters that satisfy a set of prescribed requirements. However, it excludes some

useful converters that do not satisfy Assumption 3 given at the beginning of this section. Moreover, since this approach is based on enumeration of all possible sets of incidence matrices that represent distinct switched networks, the complexity of the synthesis work directly depends on the number of switched networks during each switching cycle. If the classes of converters extend to more than two-switched-network cases, the synthesis work becomes very complicated if not impossible.

These difficulties are overcome in the new synthesis approach, which is discussed in the next section.

3.2 Fundamentals of the New Synthesis Method

Instead of studying the linear switched networks of each converter, we can derive the equivalent circuits of the converter at different frequency ranges, dc and ac (harmonics at switching frequency) as in Chapter 2. The resulted ac and dc circuits can be represented by a pair of graphs: G_a and G_d.

The synthesis procedure starts from a given ac circuit. All possible associated dc circuits have the same structure (n_d and l_d), which can be obtained from Proposition 2.6 for two-switched-network converters, or from Eqs. (2.57) and (2.58) for three or more switched-network converters which have no self-loop in their dc circuits. Synthesis of converters with self-loop(s) in their dc circuits is carried out in Appendix B.

As mentioned in Section 3.1, an essential step in the development of an systematic synthesis procedure is to select a proper matrix representation for the converter topology. Again, since the incidence matrix corresponds one-by-one to the represented graph and describes the exact positions of the elements in the graph, it is the natural choice. Graphs G_a and G_d are represented by the corresponding incidence matrices, $\mathbf{A}_a$ and $\mathbf{A}_d$.

Volt-second and ampere-second balance equations can be derived for the given ac circuit as in Section 2.5.1 or Section 2.7. Also, for each associated dc circuit, the reduced incidence matrix $\mathbf{A}_{fd}$ can be obtained from $\mathbf{A}_d$ by deleting the row corresponding to the datum (ground) node. Then, the dc model derived in Section 2.5.2 can be used to find the average voltage and current of each switch, and the dc voltage conversion ratio $M(D)$. After eliminating the redundant and degenerate cases, ideal switches can be implemented by semiconductor devices as in Section 2.6 and Section 2.7. Recall that, the positions of the

inductors and capacitors have not been taken into account explicitly. Since a unidirectional switch or a current-bidirectional switch (which can be implemented by a MOSFET) only needs one semiconductor device, they are preferable to other switch types (voltage bidirectional and four-quadrant). Dc circuits can be sorted out by desirable conversion ratios and switch implementation before considering the positions of inductors and capacitors. Therefore, the synthesis procedure can be carried out efficiently.

The next step is to insert the *minimum* number of inductors and capacitors that are necessary to generate valid PWM converter(s) for a given pair (G_a and G_d). The insertion procedure based on comparison of $\mathbf{A}_a$ and $\mathbf{A}_d$ must guarantee that the resulted converter reduces to the dc circuit when inductors are shorted, capacitors are removed, and to the ac circuit when inductors are removed, capacitors are shorted.

Definition 3.1 *The order of a dc circuit can be defined by the minimum number of inductors and capacitors that need to be inserted in this dc circuit to generate at least one valid PWM converter.*

Up to now, we have only considered generating valid PWM converters with the minimum number of inductors and capacitors, i.e. the minimum complexity for the given pair (G_a and G_d). However, the minimum complexity of converter topology may not necessarily lead to the optimum converter. Specifically, for lower ripple currents and lower EMI noise applications, it is often preferred that input and output current waveforms are continuous. The synthesis procedure can be modified to take into account the required feature. Details will be carried out in Chapter 4.

Generally, each pair of graphs (G_a and G_d) may correspond to different converter topologies. Since the dc model in terms of the average switch voltages and currents is determined by a given pair (G_a and G_d), all the converters generated from pair (G_a and G_d) have the same average switch quantities and dc conversion ratio $M(D)$. Furthermore, the implementation of ideal switches can be resolved by using the signs of V_s and I_s, regardless of the number and positions of inductors and capacitors. Thus, the synthesis procedure is simplified compared with the previous one, where switch implementation and $M(D)$ need to be determined for each individual converter.

It is worth mentioning that the number of the capacitors N_C of a PWM converter is related to the number of inductors N_L of the converter, and the relation depends on the

topology of ac circuit. The following proposition describes this property.

Proposition 3.1 *Suppose that a PWM converter has N_C capacitors and N_L inductors, graph G_a of the converter has n_{ta} nodes and q linearly independent volt-second balance equations, the number of the capacitors is related to the number of inductors as follows:*

$$N_C - N_L = q - n_a \,. \tag{3.2}$$

Proof: Consider the difference between the numbers of nodes of G_d and G_a ($n_{td} - n_{ta}$): each inductor reduces the difference by one; while each capacitor or voltage source increases it by one. Thus, we have

$$n_{td} - n_{ta} \;=\; N_C + N_g - N_L \,. \tag{3.3}$$

Also, by Eq. (2.57), we have

$$n_{td} - n_{ta} \;=\; q + N_g - n_a \,. \tag{3.4}$$

Equation (3.2) follows directly from Eqs. (3.3) and (3.4). □

For two-switched-network converters, q equals l_a, Eq. (3.2) can be rewritten into:

$$N_C - N_L = l_a - n_a \,. \tag{3.5}$$

For the classes of converters covered in [5], l_a equals n_a. Consequently, N_C equals N_L. The same statement is given by Proposition 3.3 in [5]. However, Proposition 3.1 is a much generalized statement regarding the topology of dc-to-dc PWM converters.

The synthesis procedure described so far is general since it is not limited by the number of switches, reactive elements, input voltage sources, output loads and switched networks. In this thesis, however, the discussions will be focused on classes of converters that are of most practical interest. Converters covered are within the following scope:

1. A single dc voltage source V_g.

2. One (or two) LTI loads R_o (or R_{o1} and R_{o2}), and each load is in parallel with a single capacitor.

3. The dc voltage source V_g and load(s) R_o (or R_{o1} and R_{o2}) share a common ground (datum node).

4. The number of switches is between two and four.

5. The number of switched networks is two or three.

Chapter 4 Synthesis of Two-Switch Dc-to-Dc Converters

The aim of this chapter is to illustrate the basic ideas of the synthesis procedure through the synthesis of two-switch converters.

The generic ac circuit for all two-switch converters and the corresponding balance equations are introduced in Section 4.1. The enumeration of dc topologies results in six valid dc circuits in Section 4.2. In Section 4.3, the synthesis procedure is limited to only generate converters with minimum reactive elements. In Section 4.5, the procedure is modified to generate converters with both continuous input and output currents.

4.1 The Ac Circuit for Two-Switch Converters

Recall that in Section 2.3, the ac circuit of the Sepic converter is derived and shown in Fig. 2.1(b). In fact, this is the generic ac circuit of all the two-switch converters with $\deg M(D) \geq 1$. The derived balance equations are rewritten here,

$$\begin{bmatrix} V_s \\ I_{\bar{s}} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{D'}{D} \\ \frac{D'}{D} & 0 \end{bmatrix} \begin{bmatrix} I_s \\ V_{\bar{s}} \end{bmatrix}. \tag{4.1}$$

G_a has $l_a = 1$ links and $n_a = 1$ tree branches. By Proposition 2.6, each associated G_d has no link and $n_d = 2$ tree branches. Enumeration of possible dc topologies is carried out in the next section.

4.2 Enumeration of Possible Dc Topologies

The number of possible dc circuits of two-switch converters is sufficiently small so that the enumeration can be accomplished by hand.

Since n_d is equal to two, graph G_d contains three nodes, labeled as 0, 1, 2. V_g is connected between node 1 and 0. R_o and C_o are connected between node 2 and 0. The

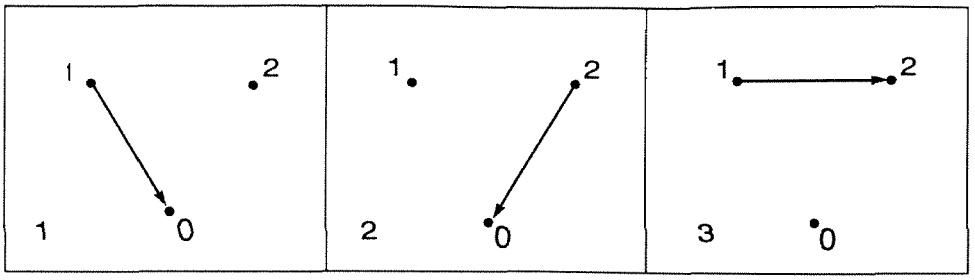


Figure 4.1: Possible positions of the switches in a two-switch dc circuit.

possible positions for each of the two switches are listed in Fig. 4.1. Each dc circuit is represented by a number of the form $(i_1 i_2.n)$, where $i_1, i_2 \in \{1, 2, 3\}$ denote the positions of the two switch branches according to Fig. 4.1. Since the same dc circuit occurs if orientations of both switches are changed in the graph, the branch of S takes the reference orientation by default; while $n \in \{1, 2\}$ denotes the orientation of the branch of $\bar{S}$. $n = 1$ is used to denote the orientations as in Fig. 4.1, and $n = 2$ is used to denote the opposite orientation. Thus the problem of enumeration of all possible dc circuits is reduced to the problem of enumeration of possible numbers of $(i_1 i_2.n)$ that represent the dc circuits.

Since i_1 shall not equal i_2, the possible number of pairs is $C_3^1 C_2^1 \times 2 = 12$. Some of the representations may lead to identical dc circuits. Thus the next task is to eliminate the redundant cases.

Numbers $(i_1 i_2.n)$ and $(i_2 i_1.n)$ represent identical dc circuits with S and $\bar{S}$ interchanged, i.e., with conversion ratios $M(D)$ and $M(1-D)$, respectively. To avoid the redundant cases, i_1 is chosen to be less than i_2, which further reduces the number of valid pairs to 6.

Then, the dc circuits need to be checked to exclude degenerate cases. The term "degenerate" is used to refer to cases in which the dc circuit does not correspond to any valid PWM converter with a unique, bounded steady-state solution.

Definition 4.1 *A dc circuit is non-degenerate if and only if the corresponding equations in terms of average switch voltages and currents have a unique, bounded steady-state solution and* $degM(D) \geq 1$. *Furthermore, for two-switched-network cases, none of the average switch voltages and currents are equal to zero.*

The six dc circuits are drawn in Fig. 4.2. Based on dc circuit topology and the balance equations from the generic ac circuit, the dc conversion ratio $M(D)$ and average quantities for switches of each dc circuit can be derived. By definition, all the six dc circuits are

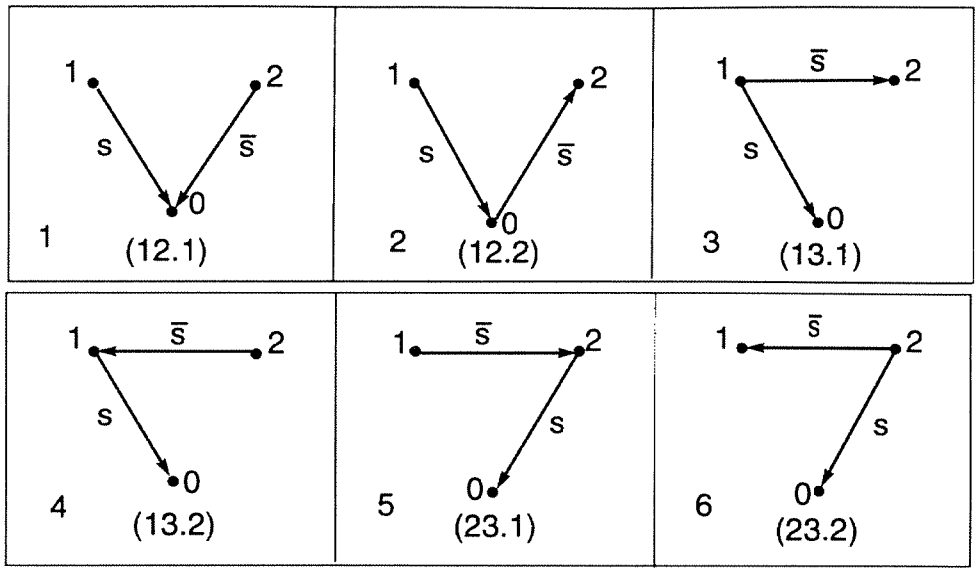


Figure 4.2: Dc circuits for two-switch converters.

non-degenerate. Furthermore, the ideal switches can be implemented with semiconductor devices as explained in Section 2.6. Dc circuit (1) is used to demonstrate this procedure.

In Dc circuit (1), S is connected with input voltage source V_g, and $\bar{S}$ is connected with the load R_o. Therefore, V_s equals V_g, and $V_{\bar{s}}$ equals V_o. From the volt-second balance equation

$$V_{\bar{s}} = -\frac{D}{D'}V_g\,, \tag{4.2}$$

$$\text{and} \quad M(D) = \frac{V_{\bar{s}}}{V_s} = -\frac{D}{D'}\,, \tag{4.3}$$

$$I_{\bar{s}} = -I_o = \frac{D}{D'}\frac{V_g}{R_o}\,. \tag{4.4}$$

From the current-second balance equation

$$I_s = \left(\frac{D}{D'}\right)^2 \frac{V_g}{R_o}\,. \tag{4.5}$$

The switches can be implemented by use of the results in Section 2.6

$$V_s I_s > 0: \quad S \text{ is a transistor.}$$

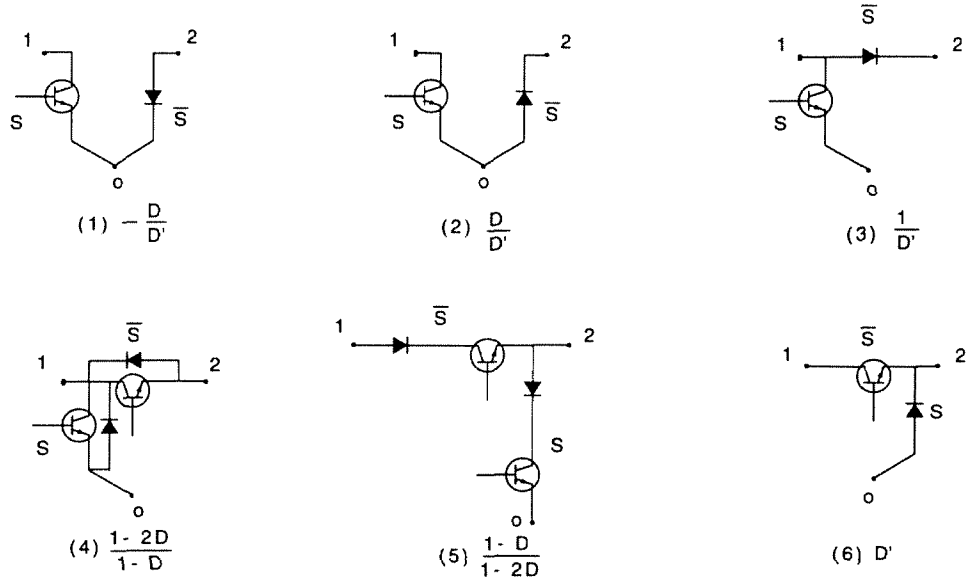


Figure 4.3: The switch implementation of the six dc circuits with distinctive $M(D)$.

$$V_{\bar{S}} I_{\bar{S}} \; < \; 0: \quad \bar{S} \text{ is a diode.}$$

The same procedure can be carried out on the other five dc circuits in Fig. 4.2. The switch implementation of the six dc circuits together with their distinctive $M(D)$ are shown in Fig. 4.3.

Note that, since there are only two switch branches, the dc model is derived by inspection. However, the same results can be obtained formally as in Section 2.5. For three or more switches converters, the task of enumerating and sorting out enormous number of topologies can only be carried out efficiently by a computer program, in which the formalized dc model with matrix representations is indispensable.

The advantage of knowing $M(D)$ and switch implementation before inserting the inductors and capacitors is obvious. If $M(D)$ is prescribed, only dc circuit(s) with the specified $M(D)$ need to be worked on to generate the desirable converters. Also since the switch implementation is determined by the dc circuit regardless of the positions of inductors and capacitors, it can be applied to all the converters developed from the same dc circuit. Therefore, the synthesis procedure is greatly simplified, compared with the previous procedure where $M(D)$ and switch implementation can only be determined after knowing each

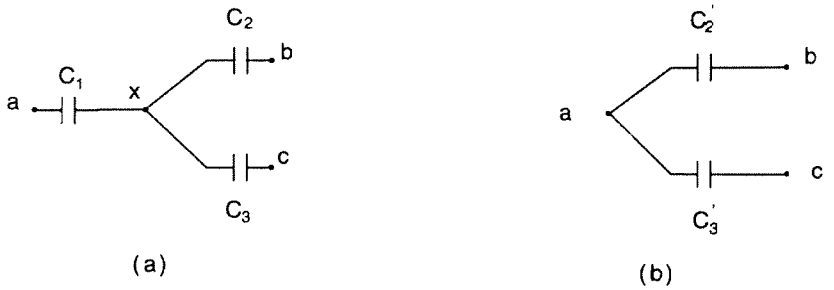


Figure 4.4: A cut-set of capacitors in a dc-to-dc converter (a) can be transformed to a circuit with less capacitors (b).

individual converter topology.

4.3 Insertion of Minimum Inductors and Capacitors

The final step in the synthesis procedure is to insert inductors and capacitors in the dc circuit to obtain the full converters. In this section, we will discuss the synthesis procedure to construct all the possible converters with a *minimum* number of inductors and capacitors.

When a PWM dc-to-dc converter reduces to its dc circuit, some of the nodes in the converter are missing because inductors are shorted. A few more words are needed here to explain that all the missing nodes are caused by shorted inductors. If there was a cut-set consisted only of capacitors in the converter, as shown in Fig. 4.4(a), node x would disappear in G_d, when all the capacitors were removed. However, we can replace the circuit in Fig. 4.4(a) with its equivalent in Fig. 4.4(b). In the new circuit, only two capacitors are needed. To be equivalent, the voltage rates and values of C_2 and C_3 have to be modified. Therefore, a cut-set of capacitors can not exist in a converter with minimum number of elements.

Graphs G_d and G_a can be represented by incidence matrices A_d and A_a, respectively. A_d and A_a have the same number of columns that correspond to the switch branches.

The insertion procedure goes as follows: First, we compare the rows of A_d with that of A_a to determine the position of the inductors. After inserting all the necessary inductors into graph G_d, we have recovered all the nodes in the converter. The task of inserting

capacitors is straightforward. We just group all the nodes that shall merge into one node in graph G_a, and use capacitors to connect them together.

Since the number of capacitors N_C is related to the number of inductors N_L (Proposition 3.1), after knowing N_L, we can determine the order of the converter (Definition 3.1). Every minimum reactive-element converter generated from the dc circuit has the same order. Only the dc circuits with required properties and relatively lower order are of practical interest. Therefore, N_L is one of the important criteria to select dc circuits.

For the two-switch cases, both l_a and n_a equal one. By Proposition 3.1, the number of capacitors N_C equals the number of inductors N_L.

The incidence matrix A_a of graph G_a in Fig. 2.1(b) is

$$A_a = \begin{array}{c} \\ a \\ b \end{array} \begin{array}{c} \begin{array}{cc} S & \bar{S} \end{array} \\ \begin{pmatrix} -1 & -1 \\ 1 & 1 \end{pmatrix} \end{array} \tag{4.6}$$

Dc circuit (2) in Fig. 4.2 is used to illustrate L- and C- insertion procedure. The incidence matrix A_d is

$$A_d = \begin{array}{c} \\ 0 \\ 1 \\ 2 \end{array} \begin{array}{c} \begin{array}{cc} S & \bar{S} \end{array} \\ \begin{pmatrix} -1 & 1 \\ 1 & 0 \\ 0 & -1 \end{pmatrix} \end{array}. \tag{4.7}$$

Because V_g and C_o are shorted in ac circuit, terminal nodes 0, 1, 2 are combined into one node in G_a: either node a or node b.

In the first case, suppose nodes 0, 1, 2 are combined into node a. Thus, rows 0, 1, 2 of A_d are compared with row a of A_a. Since entries "1" in rows 0 and 1 do not appear in row a, rows 0 and 1 have to be split. As shown in Fig. 4.5. Node 0 is split into node 0 and node $0'$, and node 1 is split into node 1 and node $1'$, which physically means the insertion of two inductors, one between nodes 0 and $0'$, the other between node 1 and $1'$. Taking into

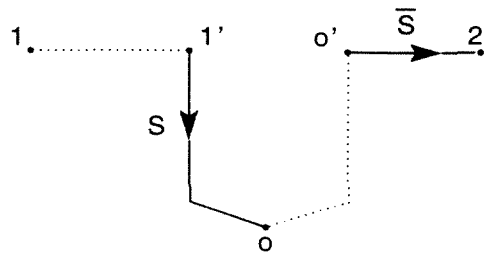


Figure 4.5: The structure after splitting nodes 0 and 1 in the dc circuit.

account the two nodes added by the inductors, the incidence matrix A_d becomes

$$\begin{array}{c} \\ 0 \\ 1 \\ 2 \\ 0' \\ 1' \end{array} \begin{array}{c} \begin{array}{cc} S & \bar{S} \end{array} \\ \begin{pmatrix} -1 & 0 \\ 0 & 0 \\ 0 & -1 \\ 0 & 1 \\ 1 & 0 \end{pmatrix} \end{array} \tag{4.8}$$

The five nodes can be separated into two groups: terminal nodes 0, 1, 2 that belong to node a in G_a; and nodes $0'$, $1'$ that belong to node b in G_a. Since terminal nodes have already been connected by V_g and C_o. Only one capacitor is needed to connect $0'$ and $1'$. The result is the Sepic converter with a two-switch 2L1C converter cell.

It is obvious from this example that each inserted inductor splits a node in G_d into two, which belong to two different nodes in G_a, respectively. No inductor inserted is in a loop with capacitors and possible voltage source, since if it were, the two terminals of the inductor would be shorted into one node in G_a, which contradicts the defined inductor insertion rule.

Generally, the inductors in a PWM dc-to-dc converter can be classified by the following definition:

Definition 4.2 *In a PWM dc-to-dc converter, each inductor that is not in a loop with only elements in* $\mathbf{C} \cup \mathbf{V}_g$ *is called essential inductor; while each inductor that is in a loop with only elements in* $\mathbf{C} \cup \mathbf{V}_g$ *is called non-essential inductor.*

Note that, all the inductors inserted by the defined minimum-element insertion rule are *essential* inductors, which have rectangular ac voltage waveform. While the *non-essential* inductors are mainly used to improve input and output waveforms. They are not essential to the basic operation of the converter. Converters with non-essential inductors are generated in Section 4.3, where the insertion procedure is modified to generate converters with continuous input and output currents. An easy way to distinguish essential inductors from non-essential inductors is to short all capacitor(s) and voltage source(s) in the converter, the inductors retained in connection with switches are essential inductors; while those shorted by capacitors and possible voltage source(s) are non-essential inductors. The following proposition can be used to decide whether or not the coupled-inductor technique is applicable.

Proposition 4.1 *In a PWM dc-to-dc converter, a set of inductors* $\mathbf{L}_c$ *can be coupled on a single magnetic core if they are in parallel when retained in* G_a.

Proof: The proof follows the fact that inductors in $\mathbf{L}_c$ share the same voltage waveforms. □

Consider the special case when G_a has only two nodes, all the essential inductors are in parallel if retained in G_a, and therefore, can be coupled. This applies to the converters generated in the present section, and those in Chapter 5 and Chapter 8.

Similarly, the capacitors in a PWM dc-to-dc converter can be classified by the next definition.

Definition 4.3 *In a PWM dc-to-dc converter, each capacitor that is not in a cut-set with only elements in* $\mathbf{L} \cup \mathbf{V}_g \cup \mathbf{R}_o$ *is called essential capacitor; while each capacitor that is in a cut-set with only elements in* $\mathbf{L} \cup \mathbf{V}_g \cup \mathbf{R}_o$ *is called non-essential capacitor.*

Except the output capacitor(s), all the capacitors inserted by the defined rule are *essential* capacitors. An easy way to distinguish essential capacitors from non-essential capacitors is to open all the inductors in the converter, the capacitors retained in a loop with switches are essential ones.

In the second case, suppose nodes 0, 1, 2 are coalesced into node b. The same insertion procedure results in the dual Sepic (Zeta) converter with again a two-switch 2L1C cell.

In conclusion, for dc circuit (2), there are two possible converter cells with minimum inductors and capacitors (2L1C), which are shown in Fig.4.6. Taking into account the

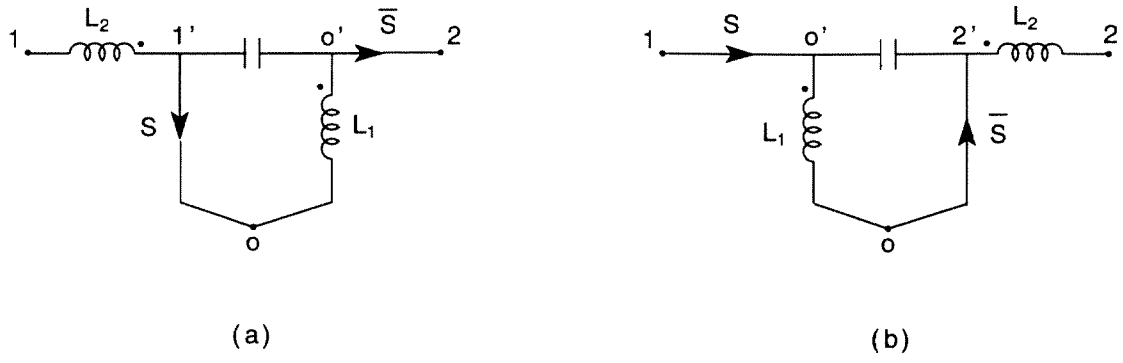


Figure 4.6: The converter cells from dc circuit (2) with minimum L's and C's (2L1C).

output capacitor, N_C equals N_L as predicted.

Dc circuits (4) and (5) can be generated from dc circuit (2) by changing the terminal connections. Thus converters with dc circuits (4) and (5) can be generated from the converters with dc circuit (2) by changing the terminal connections(i.e., by rotating the converter cells with ideal switches). Since the switch implementation depends on the individual dc circuit topology, after the cell rotations, the idea switches are replaced by the semiconductor devices as in Fig. 4.3 (4) and (5), respectively.

Similarly, L- and C- insertion only need to be implemented on one of the three dc circuits: (1), (3), (6); while the other two can be obtained by rotating the converter cell. Here, for each dc circuit, the converter with minimum reactive elements ($N_C = N_L = 1$) is unique. The switch implementations for the three dc circuits are shown in Fig. 4.3(1), (3) and (6).

All nine converters with minimum reactive elements are shown in Fig. 4.7: Converter (a) is from dc circuit (1); converters (b) and (c) are from dc circuit (2); converter (d) is from dc circuit (3); converters (e) and (f) are from dc circuit (4); converters (g) and (h) are from dc circuit (5); and converter (i) is from dc circuit (6).

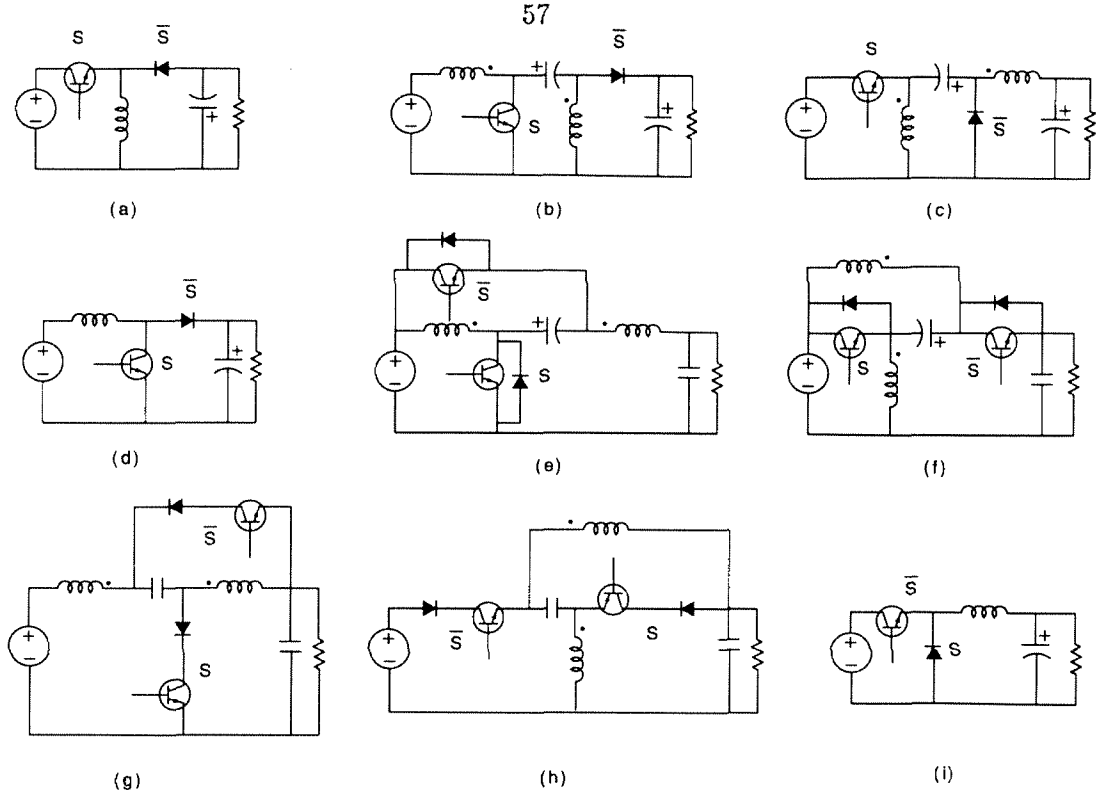


Figure 4.7: The nine two-switch converters with minimum L's and C's.

4.4 Calculation of Rms Currents by Use of the Ac and Dc Circuits

Converters generated from the same ac and dc circuits have identical switch voltage and current stresses.

The parasitic resistance associated with each converter element contributes to the total loss of the converter. For comparison, rms currents for all elements can be found by use of ac and dc circuits.

As an example, the dual Sepic converter with parasitic resistances is shown in Fig. 4.8(a), together with the dc circuit (b), ac circuit(c) and its equivalent circuits during DT_s(d) and during $D'T_s$(e).

Under the small-ripple assumption, the inductor currents and dc component of the input current can be found from the dc circuit:

$$I_{L1} = I_{r_{L1}} = I_s = MI_o\,, \tag{4.9}$$

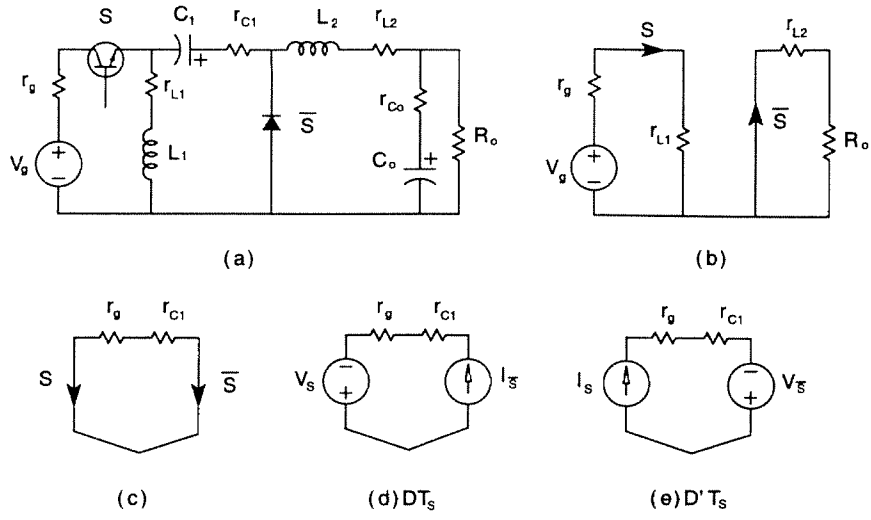


Figure 4.8: The dual Sepic converter with parasitic resistances(a), its dc circuit(b), ac circuit(c) and the equivalent circuit for time interval DT_s (d) and time interval $D'T_s$ (e).

$$I_{L2} = I_{r_{L2}} = I_{\bar{s}} = I_o\,, \tag{4.10}$$

$$I_{gd} = I_s = MI_o\,. \tag{4.11}$$

The rms currents of capacitor C_1, and ac component of the input current can be found from the ac equivalent circuits:

$$I_{C1rms} = I_{garms} = \sqrt{{I_{\bar{s}}}^2 D + {I_s}^2 D'} = \sqrt{M} I_o\,. \tag{4.12}$$

Then,

$$I_{grms} = \sqrt{{I_{gd}}^2 + {I_{garms}}^2} = \sqrt{M + M^2} I_o\,. \tag{4.13}$$

Note that, r_{Co} does not appear in the ac circuit, since only negligible ripple current goes through C_o.

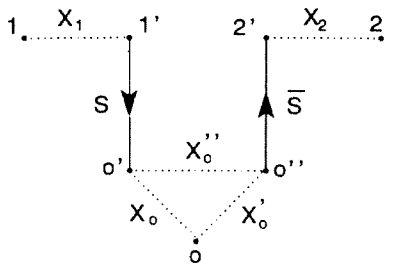


Figure 4.9: The possible positions for inductors.

4.5 Generation of Converters with Continuous Input and Output Currents

For lower EMI and lower losses on parasitic resistances, continuous input and output current waveforms are often preferred. Converters generated in Section 4.3 with minimum elements do not satisfy this requirement. However, the synthesis procedure can be modified to include this property at the beginning of inserting inductors and capacitors.

The information of continuous input or output currents can be obtained explicitly from the incidence matrix. For example, in the incidence matrix in (4.8), both entries in the row corresponding to terminal node 1 are zero and no internal nodes ($0'$ and $1'$) are connected with node 1. Thus node 1 is connected with the converter cell only by an inductor, which indicates continuous input current. Same statement can be made for the output current, if node 2 instead of node 1 has the above features.

A single input and single output converter has three terminal nodes (0, 1, 2). The requirement of continuous input and output waveforms is equivalent to having any two terminal nodes connected with the converter cell only by inductor(s). Dc circuit (2) is again used as an example. For simplification of discussion, the dc topology is shown in Fig. 4.9, together with the five possible positions for inductors. All possible converter topologies with continuous input and output currents are enumerated as follows

1. Terminal nodes 1 and 2 are connected with the converter cell only by inductors: Three inductors are placed at X_1, X_2 and X_0'', respectively, either node $0'$ or node $0''$ is

#	I_{L1}	I_{L2}	I_{L3}	Coupled	Drive
$A1$	M	1	1	L_1, L_2	D
$A2$	M	M	1	L_2, L_3	F
$A3$	M	$\|M-1\|$	1	L_1, L_3	D
$A4$	M	M	$\|M-1\|$	L_1, L_2, L_3	D
$A5$	M	M	1	L_1, L_3	D
$A6$	1	$\|M-1\|$	1	L_1, L_2, L_3	F
$A7$	M	$\|M-1\|$	1	L_1, L_3	F
$A8$	M	1	1	L_1, L_3	F

Table 4.1: Comparison of converters generated from dc circuit (2) with continuous input and output current waveforms.

shorted with the ground (node 0). Two converters are generated as in Fig. 4.10: $A1$, $A2$. Converter $A1$ is Sepic converter with an output filter; while converter $A2$ is dual Sepic converter with an input filter.

2. Terminal nodes 0 and 1 are connected with the converter cell only by inductors: One inductor is placed at X_1; while the other two inductors can be placed at either two of X_0, X_0', and X_0''. The resulted three converters are shown in Fig. 4.10: $A3$, $A4$, $A5$.

3. Terminal nodes 0 and 2 are connected with the converter cell only by inductors: One inductor is placed at X_2; while the other two inductors can be placed at either two of X_0, X_0', and X_0''. The resulted three converters are shown in Fig. 4.10: $A6$, $A7$, $A8$.

All eight converters have three inductors and three capacitors, which are the minimum elements needed for dc circuit (2) to have continuous input and output currents. For each converter, in the ac circuit, the ESRs associated with C_1 and C_2 are in a loop with S and $\bar{S}$. Therefore, rms current of C_1 or C_2 equals $\sqrt{M}I_o$ as in Eq. (4.12). The losses on the ESRs are the same if the same capacitors are used for each converter. Other parameters relevant for comparison of converter topologies are summarized in Table 4.1. All the currents are normalized to I_o. Inductors that can be coupled on a single magnetic core are enclosed in Column (Coupled); while D indicates direct drive and F indicates floating drive in the last column.

Converter $A4$ is favorable with regard to the coupled-inductor (all three inductors can be coupled on a single core) and direct drive features. However, if isolation is required, $A4$ needs two transformers; while some other choices ($A1$ and $A2$) need only one. Thus, the choice of a particular converter topology depends on the practical requirements.

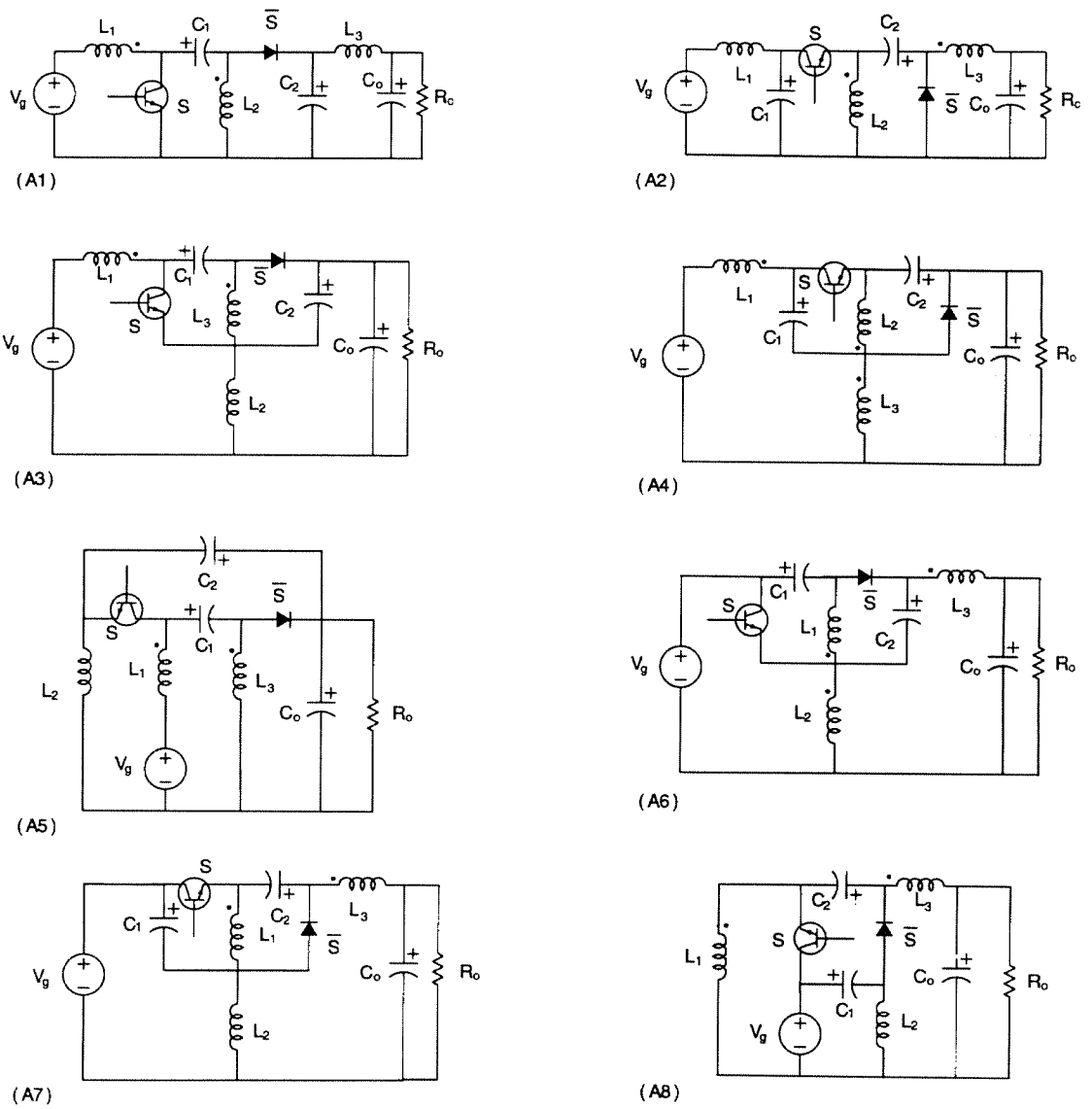


Figure 4.10: Eight converters generated from dc circuit (2) with continuous input and output current waveforms.

The converters with dc circuits (4) and (5) can be generated by rotating the converter cells and replacing the switches with the corresponding ones in Fig. 4.3(d) and (e). All the coupled-inductor features are kept after the rotations.

For dc circuit (1), there are three possible converters with continuous input and output currents, which are shown in Fig. 4.11. By comparison, $B1$ (Ćuk converter) is the most desirable choice since L_1, L_2 can be coupled, and direct drive is used. Actually, the coupled-inductor can be designed to have all the leakage inductance on the output side winding. Then, $B1$ has identical two-switched networks as $B2$. In this case, all the ripple current is steered to the input side, and the output current has zero ripple. Similarly, $B1$ has identical two-switched networks as $B3$ when all the leakage inductance is on the input side winding. Thus, $B1$ physically combines two inductors into one and has the flexibility to steer the ripple current into either the input or the output side. Consequently, the size and cost are reduced, and efficiency is increased. Furthermore, when isolation is required, only one transformer is needed in $B1$; while two are needed in $B2$ and $B3$.

Again, converter cell rotations can generate the converters with dc circuits (3) and (6). Moreover, the coupled-inductor feature is maintained after the rotations.

4.6 Conclusion

As a summary, for two-switch converters, there are six possible dc circuits. The synthesis procedure is first defined to generate all the converters with minimum L's and C's. As a result, nine converters are generated in Section 4.3. Then, in Section 4.5, the procedure is modified to generate the converters with continuous input and output currents.

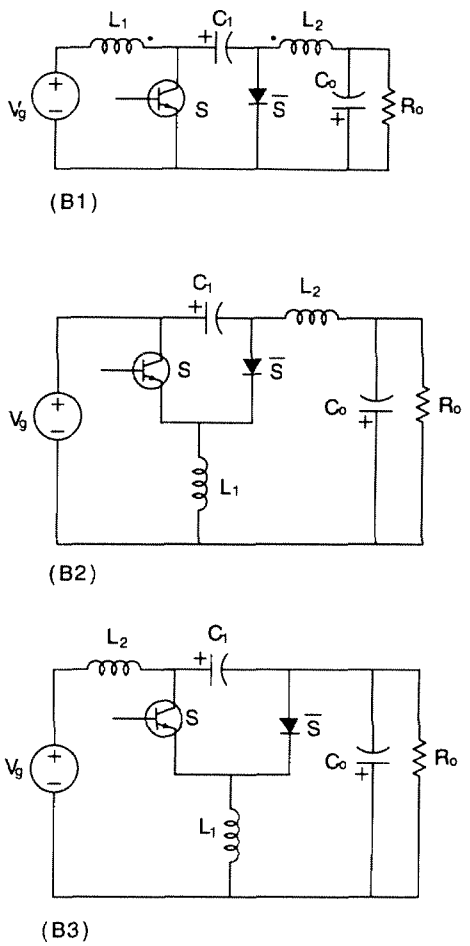


Figure 4.11: The three converters generated from dc circuit (1) with continuous input and output current waveforms.

Chapter 5 Synthesis of Three-Switch Dc-to-Dc Converters

This chapter is devoted to the synthesis of three-switch converters with two switched- networks.

The two possible ac circuits are given in Section 5.1. Since one is the dual of the other, synthesis procedure only need to be carried out on one ac circuit: ac circuit (1) is chosen here. Enumeration of associated dc circuits for ac circuit (1) is given in Section 5.2, which results in total of 66 dc circuits. In Section 5.3, a formalized procedure is discussed to determine the number and positions of reactive elements for a given dc circuit.

5.1 The Ac Circuits of Three-Switch Converters

Three-switch converters with two switched-networks have two possible ac circuits, as shown in Fig 5.1. Ac circuit (2) is dual to ac circuit (1). In ac circuit (1), there is a loop of S_1-branch and S_2-branch. by Proposition 2.3, any converter generated from ac circuit (1) has a loop that consists only of capacitors and possible voltage source when S_1 and S_2 are on. By dual argument, any converter generated from ac circuit (2) has a cut-set that consists only of inductors and possible current source when S_1 and S_2 are on.

In this chapter, only the class of converters developed from ac circuit (1) is discussed, the other class can be obtained by duality.

Ac circuit (1) with reference orientations is shown in Fig 5.2 (a), together with the ac equivalent circuits during two intervals, Fig. 5.2 (b) and (c). Suppose $\bar{S}_3$ is the tree branch, and S_2 and S_3 are the links, using the results in Section 2.5.1, we have the following balance equations:

$$\begin{bmatrix} V_{s1} \\ V_{s2} \\ I_{\bar{s}3} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{D'}{D} \\ 0 & 0 & -\frac{D'}{D} \\ \frac{D'}{D} & \frac{D'}{D} & 0 \end{bmatrix} \begin{bmatrix} I_{s1} \\ I_{s2} \\ V_{\bar{s}3} \end{bmatrix}. \tag{5.1}$$

In the ac circuit, there are $l_a = 2$ links and $n_a = 1$ tree branch. By Proposition 2.6,

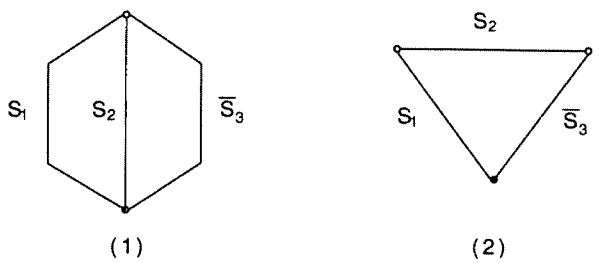


Figure 5.1: The two ac circuits of three-switch, two-switched-network converters.

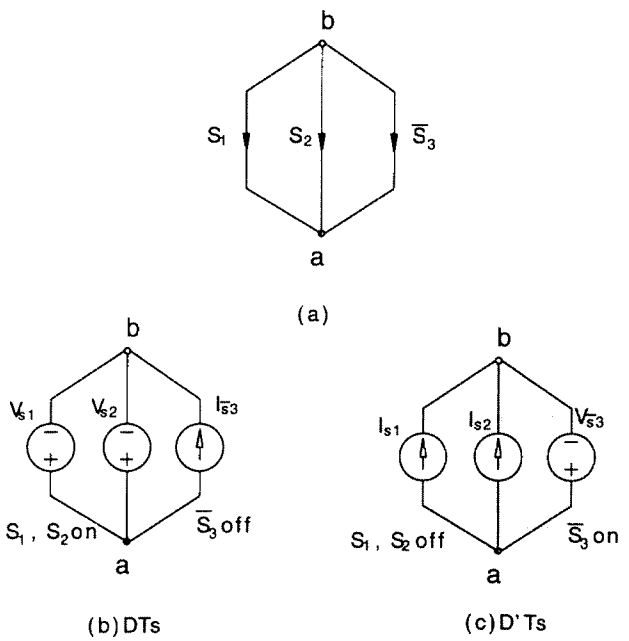


Figure 5.2: The ac circuit with reference orientations(a) and its equivalent circuits: during time interval DT_s when S_1, S_2 are on and $\bar{S}_3$ is off(b), and during time interval $D'T_s$ when S_1, S_2 are off and $\bar{S}_3$ is on(c).

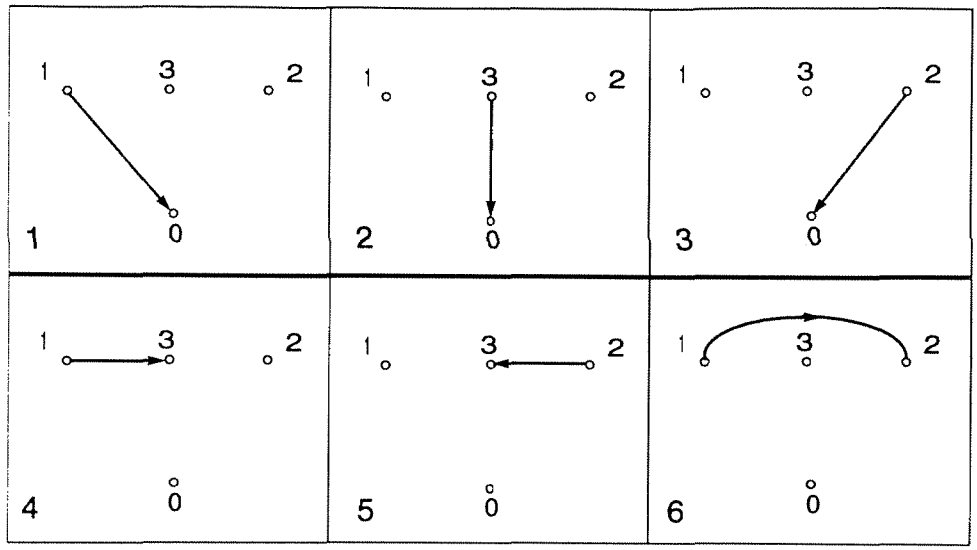


Figure 5.3: Possible positions of switches in a three-switch dc circuit.

n	S_2	$\bar{S}_3$
1	+	+
2	+	−
3	−	+
4	−	−

Table 5.1: Orientation of the switches in a three-switch dc circuit.

each associated dc circuit has no link and $n_d = 3$ tree branches. In the next section, we will enumerate all possible dc circuits.

5.2 Enumeration of Possible Dc Topologies

Each dc circuit has four nodes, which can be divided into two groups: terminal nodes 0, 1, 2, and internal node 3. The six possible positions for each switch branch are shown in Fig. 5.3.

Each dc circuit can be represented by a number of the form $(i_1 i_2 i_3.n)$, where i_1, i_2, $i_3 \in \{1,2,3,4,5,6\}$ denote the positions of switches S_1, S_2, $\bar{S}_3$, respectively. The same dc circuit occurs if orientations of all three switches are changed simultaneously. Thus S_1 takes the reference direction by default, as shown in Fig. 5.3; and $n \in \{1,2,3,4\}$ denotes orientations of the other two switch branches according to Table 5.1, with + the reference orientation.

From basic topology theorem [7], for four labeled nodes, there are $4^{(4-2)} = 16$ trees.

Since S_1 and S_2 play the same role, we can assume $i_1 < i_2$ to avoid redundancy cases. In each tree, $\bar{S}_3$ can be placed at any of the three tree branches and there are four possible orientations as in Table 5.1, which gives the total number as $16 \times 3 \times 4 = 192$.

Because the number of topologies is much larger than that of the two-switch case, a simple computer program is written based on the formalized dc model derived in Section 2.5, in which the degenerate cases can be easily eliminated by Definition 4.1. The number of possible dc circuits of three-switch, two-switched-network converters is 66, which is shown in Appendix C. For each dc circuit, the dc conversion ratio $M(D)$ and implementation of switches are resolved before inserting the inductors and capacitors.

5.3 Insertion of Minimum Inductors and Capacitors

Since the number of dc circuits with three switches are much larger than that of the two-switch case, a computer program is used to insert inductors and capacitors. An explicitly defined reactance-insertion procedure is in order to generate all possible converters with *minimum* number of inductors and capacitors for a given dc circuit.

Note that, an important characteristic of a dc circuit is its order (by definition, the minimum inductors and capacitors needed to generate at least one viable converter). By Proposition 3.1, N_C is equal to $N_L + 1$ for all the converters generated from ac circuit (1). Therefore, the order of the dc circuit is determined after knowing minimum N_L.

The four nodes in dc circuit are divided into two groups: nodes 0, 1, 2 are *terminal* nodes; and node 3 is an *internal* node.

In order to discuss the insertion procedure, we need first define the "comprow" function and introduce some terms. Remember in Section 4.3, the positions of the inductors are determined by comparing row of A_d with that of A_a. This procedure can be formalized by the following algorithm. First, the "comprow" function is defined as $r_{xy} = \text{comprow}\ (A_d[x]\ A_a[y])$. $A_d[x]$ is the row in A_d corresponding to node x and $A_a[y]$ is the row in A_a corresponding to node y, where $x \in \{0, 1, 2, 3\}$, $y \in \{a, b\}$. Each entry in row r_{xy} is determined by the following rules:

1. if $A_d[x, j] = 1$, $A_a[y, j] = 1 \Longrightarrow r_{xy}[j] = 0$

2. if $A_d[x, j] = 1$, $A_a[y, j] \neq 1 \Longrightarrow r_{xy}[j] = 1$

3. if $A_d[x,j] = -1$, $A_a[y,j] = -1 \Longrightarrow r_{xy}[j] = 0$

4. if $A_d[x,j] = -1$, $A_a[y,j] \neq -1 \Longrightarrow r_{xy}[j] = -1$

5. if $A_d[x,j] = 0$, $\Longrightarrow r_{xy}[j] = 0$

where $j \in \{1,2,3\}$, corresponding to the three switch branches, respectively.

Suppose terminal nodes 0, 1, 2 are combined into node a in G_a. Each node in G_d needs to be compared with node a by using "comprow". All possible cases are discussed as follows:

1. If row r_{xy} is zero: no split is needed for node x, i.e. $A_d[x] \subset A_a[a]$.

2. If row r_{xy} equals row $A_d[x]$: every branch incident with node x is not incident with node a. There are two different cases:

   - If x is any of the terminal nodes: x is split into node x and node x', where $A_d[x']$ keeps the same as before, and $A_d[x]$ is zero.
   - If x is node 3: Since G_a has only two nodes, and therefore two rows in A_a. Thus $A_d[x] \subset A_a[b]$ and no split is needed for node x.

3. Otherwise: x is split into node x and x', where $A_d[x'] = r_{xy}$, and $A_d[x] = A_d[x] - r_{xy}$.

$nl[a]$ is used to denote the times of splitting, i.e., the number of inserted inductors. After all the necessary splitting, capacitors are placed to connect the internal nodes that belong to node b, and possibly to connect the internal node that belongs to node a with any of the three terminal nodes.

Similarly, suppose terminal nodes 0, 1, 2 are combined into node b in G_a; each node in G_d is compared with node b, and $nl[b]$ is used to denote the total inductors needed in this case.

The minimum number of inductors is the smaller one of $nl[a]$ and $nl[b]$. If $nl[a]$ and $nl[b]$ are equal, there are two possible ways to insert the minimum number of inductors.

Note that, since the given G_a here has only two nodes, each node in G_d needs to split at most once. Generally, if G_a has n_{ta} ($n_{ta} \geq 2$) nodes, the times of splitting of each node in G_d does not exceed $(n_{ta} - 1)$, i.e., each dc node needs to be compared with at most $(n_{ta} - 1)$ ac nodes. Consequently, "comprow" function is called at most $(n_{ta} - 1)$ times to determine the splitting pattern of each dc node.

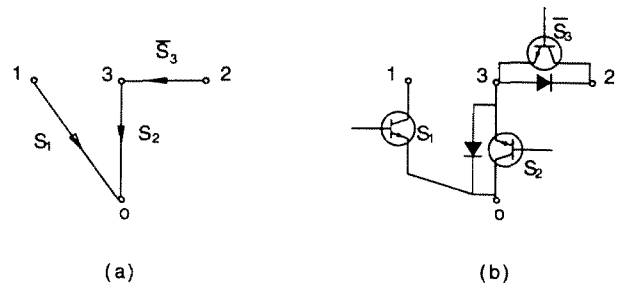


Figure 5.4: The structure of dc circuit 125.1(a) and its switch implementation(b).

An example is used to illustrate the aforementioned insertion procedure. The structure of dc circuit (125.1) and its switch implementation are shown in Fig 5.4.

The incidence matrix of graph G_a in Fig. 5.2(a) and the incidence matrix of graph G_d of dc circuit (125.1) are

$$A_a = \begin{array}{c} \\ a \\ b \end{array} \begin{array}{c} \begin{array}{ccc} S_1 & S_2 & \bar{S}_3 \end{array} \\ \begin{pmatrix} -1 & -1 & -1 \\ 1 & 1 & 1 \end{pmatrix} \end{array}, \tag{5.2}$$

$$A_d = \begin{array}{c} \\ 0 \\ 1 \\ 2 \\ 3 \end{array} \begin{array}{c} \begin{array}{ccc} S_1 & S_2 & \bar{S}_3 \end{array} \\ \begin{pmatrix} -1 & -1 & 0 \\ 1 & 0 & 0 \\ 0 & 0 & 1 \\ 0 & 1 & -1 \end{pmatrix} \end{array}. \tag{5.3}$$

First, suppose terminal nodes 0, 1, 2 are combined into node a. Rows of A_d are compared with $A_a[a]$ to determine the positions of inductors.

$$\text{comprow}(A_d[0], A_a[a]) = [\,0\,0\,0\,] \Longrightarrow A_d[0] \subset A_a[a]$$

$$\text{comprow}(A_d[1], A_a[a]) = [\,1\,0\,0\,] \Longrightarrow A_d[1] \rightarrow \begin{cases} A_d[1] = [\,0\,0\,0\,] \subset A_a[a] \\ A_d[1'] = [\,1\,0\,0\,] \subset A_a[b] \end{cases}$$

$$\text{comprow}(A_d[2], A_a[a]) = [\,0\,0\,1\,] \Longrightarrow A_d[2] \rightarrow \begin{cases} A_d[2] = [\,0\,0\,0\,] \subset A_a[a] \\ A_d[2'] = [\,0\,0\,1\,] \subset A_a[b] \end{cases}$$

$$\text{comprow}(A_d[3], A_a[a]) = [\,0\,1\,0\,] \Longrightarrow A_d[3] \rightarrow \begin{cases} A_d[3] = [\,0\,0\,-1\,] \subset A_a[a] \\ A_d[3'] = [\,0\,1\,0\,] \subset A_a[b] \end{cases}$$

The number of inductors inserted $nl[a]$ is 3. The total 7 nodes can be separated into two groups: nodes 0, 1, 2, 3 $\subset$ node a in G_a, and nodes $1'$, $2'$, $3'$ $\subset$ node b in G_a. In the first group, since terminal nodes have been connected by V_g and C_o, only one capacitor is needed to connect internal node 3 with one of the terminal nodes, which gives three choices. In the second group, there are $C_3^2 = 3$ choices to insert the two capacitors which connect nodes $1'$, $2'$, $3'$ together. Thus the total number of converters generated from this case is 9.

Next, suppose terminal nodes 0, 1, 2 are combined into node b, the corresponding rows of A_d are compared with $A_a[b]$ as follows:

$$\text{comprow}(A_d[0], A_a[b]) = [\,-1\,\,-1\,0\,] \Longrightarrow A_d[0] \rightarrow \begin{cases} A_d[0] = [\,0\,0\,0\,] \subset A_a[b] \\ A_d[0'] = [\,-1\,\,-1\,0\,] \subset A_a[a] \end{cases}$$

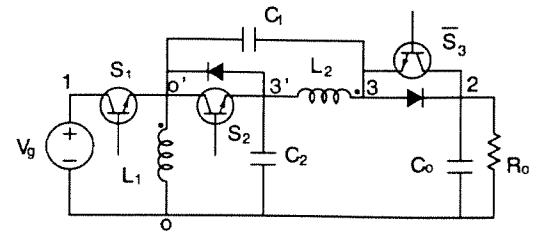
$$\text{comprow}(A_d[1], A_a[b]) = [\,0\,0\,0\,] \Longrightarrow A_d[1] \subset A_a[b]$$

$$\text{comprow}(A_d[2], A_a[b]) = [\,0\,0\,0\,] \Longrightarrow A_d[2] \subset A_a[b]$$

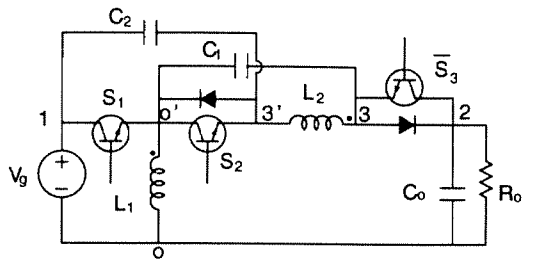
$$\text{comprow}(A_d[3], A_a[a]) = [\,0\,1\,0\,] \Longrightarrow A_d[3] \rightarrow \begin{cases} A_d[3] = [\,0\,0\,-1\,] \subset A_a[a] \\ A_d[3'] = [\,0\,1\,0\,] \subset A_a[b] \end{cases}$$

The number of inductors needed $nl[b]$ is 2, which is less than $nl[a](= 3)$. Thus, converters generated from this class have minimum inductors and capacitors (2L3C). Since there is a capacitor-loop, this dc circuit is fourth-order.

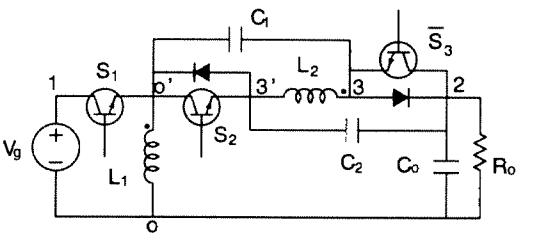
The total 6 nodes after inserting the two inductors can be separated into two groups: nodes 0, 1, 2, $3'$ $\subset$ node b in G_a, and nodes $0'$, 3 $\subset$ node a in G_a. In the first group, since terminal nodes have been connected by V_g and C_o, only one capacitor is needed to connect internal node $3'$ with one of the terminal nodes, which gives three choices. In the second group, one capacitor is needed to connect node $0'$ with node 3. Thus three converters are generated from this class, which are shown in Fig. 5.5. Since node a and node b are the only two nodes in G_a, both L_1 and L_2 are between node a and node b if left in G_a, by



(1)



(2)



(3)

Figure 5.5: Converters generated from dc circuit 125.1 with minimum reactive elements.

Proposition 4.1, they can be coupled on a single magnetic core.

The 66 dc circuits can be divided by their orders as in Appendix C. There are 24 second-order dc circuits, 24 fourth-order dc circuits, and 18 sixth-order dc circuits. Since least possible elements are desired in practical applications, only the converters generated from second-order dc circuits are discussed.

Each second-order dc circuit can generate one converter with one inductor and two capacitors. Out of the 24 converters, there are ten step-up converters, ten step-down converters, and four step-up/step-down converters.

Three-Switch, 1L2C, Step-Up Converters

Ten three-switch, 1L2C, step-up(SU) converters are shown in Fig. 5.6. Converters SU(1) and SU(2) with $M(D) = -\frac{1}{1-D}$, and converters SU(3) and SU(4) with $M(D) = \frac{1}{1-D}$, are of special interest in high-voltage applications. The doubler at the output side of any of these four converters can be extended to a capacitor-diode voltage multiplier, which increases the output voltage range. Also, SU(1) and SU(4) have the desirable feature of providing continuous input current. Isolation is easy to implement by splitting the floating capacitor into two in series, and inserting an ac transformer between the two capacitors. For SU(2) and SU(3), we can also replace the inductor with an isolation transformer.

A detailed study of converter SU(1) including topological extensions, dynamic analysis, soft-switching implementation and experimental verification will be given in Chapter 9. Similar analysis can be carried out for any of the other converters.

Three-Switch, 1L2C, Step-Down Converters.

Ten three-switch, 1L2C, step-down(SD) converters are shown in Fig. 5.7. Each of converters SD(1) to SD(4) have a floating capacitor, and thus, is easy to insert an isolation transformer. In fact, these four converters can be developed from converters SU(1) to SU(4), respectively, by exchanging the source and the load. Analogous to the capacitor-diode voltage-multiplier extensions for converters SU(1) to SU(4), a capacitor-transistor voltage-divider can be incorporated in converters SD(1) to SD(4), which can provide large step-down ratios.

As an example, a two-stage, voltage-divider SD(4) converter is shown in Fig. 5.8(a). During DT_s, transistors S_1, S_4 and diode S_2 are on, and transistors $\bar{S}_4$ and $\bar{S}_5$ are off, capacitors C_1 and C_2 are in parallel, capacitor C_F is discharging through S_1 and S_2. During DT_s, transistors $\bar{S}_4$ and $\bar{S}_5$ are on, and transistors S_1, S_4 and diode S_2 are off, capacitors C_2 and C_3 are in parallel, capacitor C_1 provides the power to the output. Since the voltages

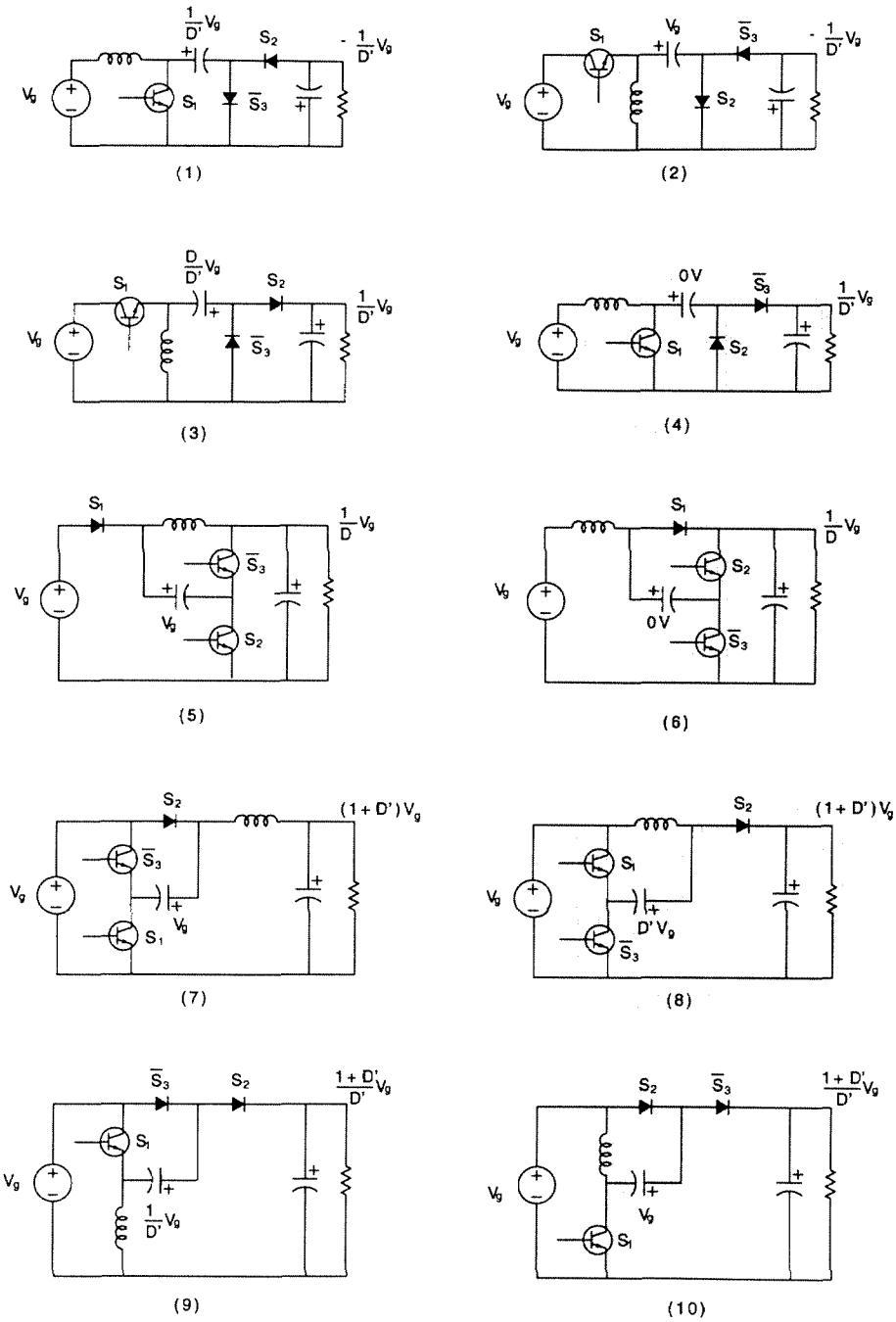


Figure 5.6: Three-switch, 1L2C, step-up converters.

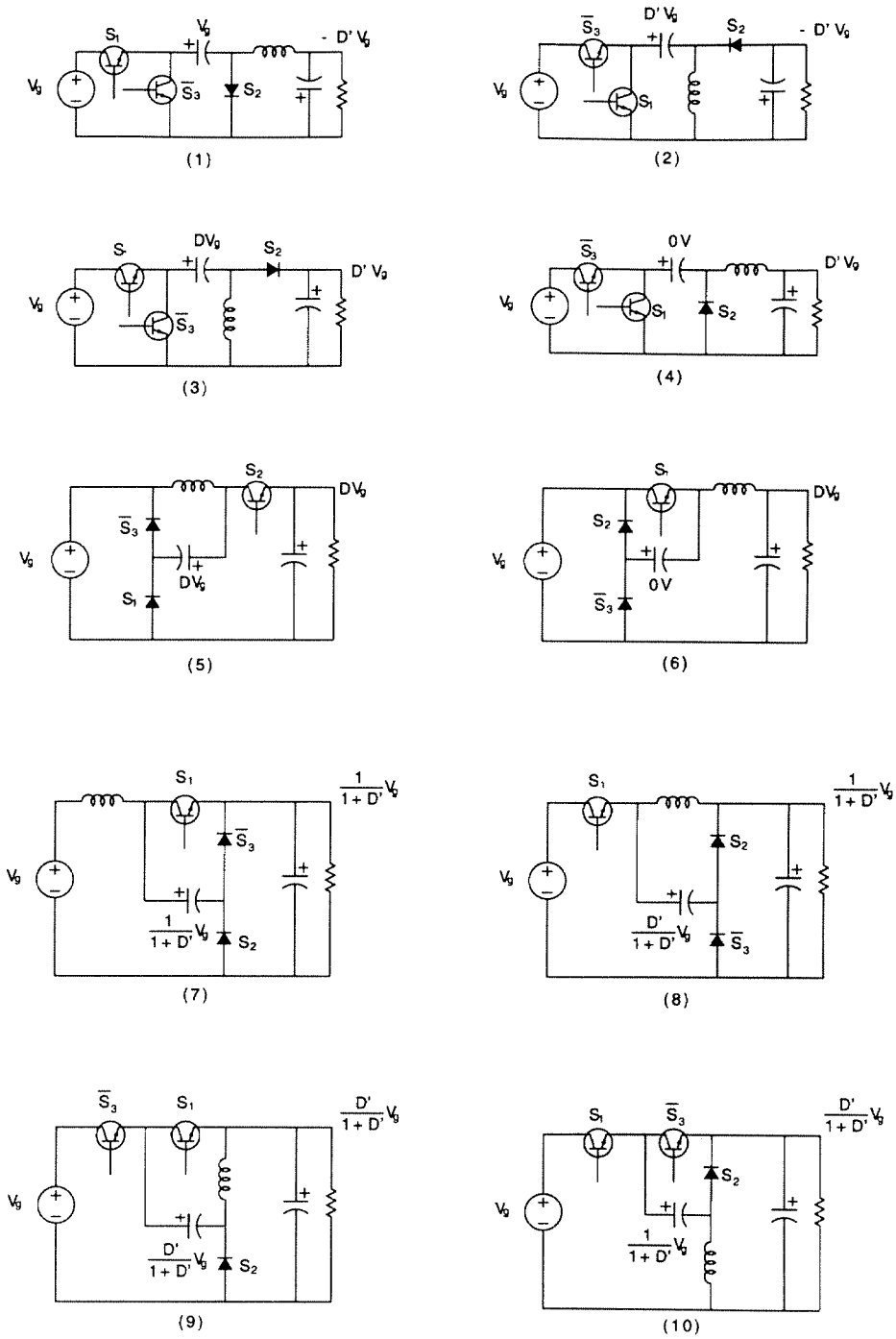


Figure 5.7: Three-switch, 1L2C, step-down converters

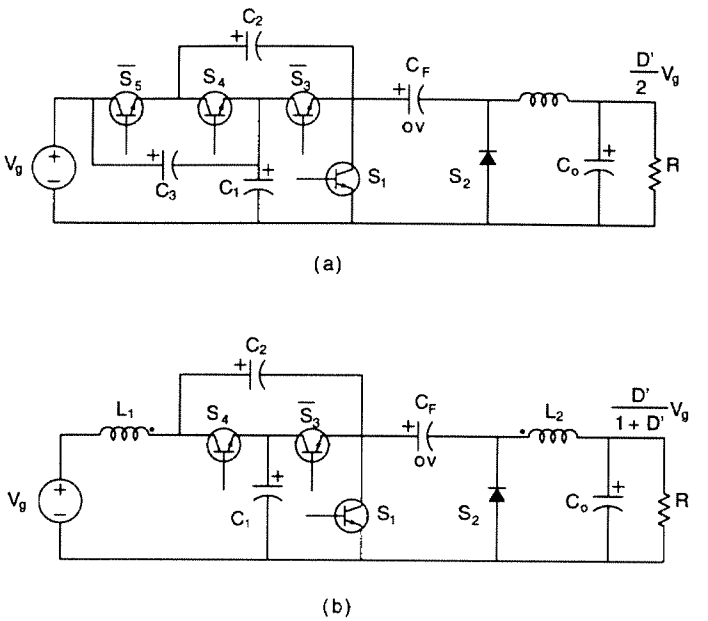


Figure 5.8: Two extensions of converter SD(4): with a two-stage voltage-divider(a); and with continuous input and output currents(b).

across C_1 is $\frac{V_g}{2}$, effectively, a two-to-one voltage division is introduced, and the overall conversion ratio is $M = \frac{D'V_g}{2}$. This voltage-divider can be easily generalized to n-stage, with $M = \frac{D'V_g}{n}$. Another interesting extension is the converter in Fig. 5.8(b), where both the input and output currents are continuous. The two inductors have identical ac voltage waveforms and can be coupled on a single magnetic core. Again, a voltage-divider can be incorporated to further increase the step-down ratio. Similar extensions can be implemented for converters SD(2) to SD(4).

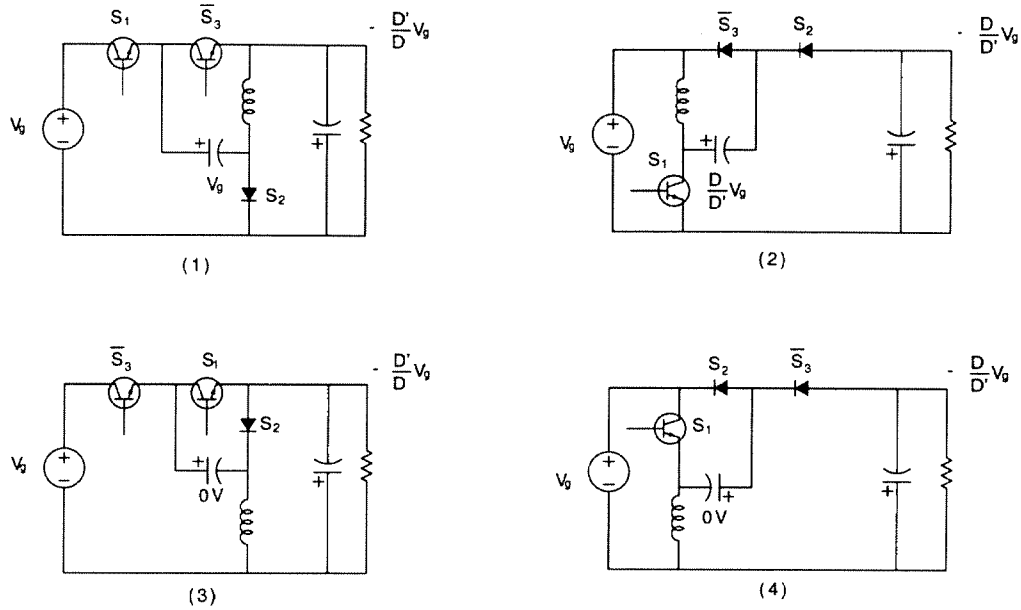


Figure 5.9: Three-switch, 1L2C, step-up/step-down converters.

Three-Switch, 1L2C, Step-Up/Step-Down Converters

Four three-switch, 1L2C, step-up/step-down(SUSD) converters are shown in Fig. 5.9.

Chapter 6 Synthesis of Four-Switch Converters

Instead of going through the enormous four-switch converters exclusively, this chapter will focus on the class of four-switch converters generated from one specified ac circuit. The main purpose is to illustrate the synthesis procedure of four-switch converters.

In Section 6.1, all the possible ac topologies for four-switch converters are introduced and balance equations are derived for the ac circuit of special interest. It will be demonstrated that this ac circuit is the generic ac circuit for all four-switch (single-transistor and three-diode), fourth-order converters discovered in [5]. Enumeration of dc circuits is carried out in Section 6.2. In Section 6.3, converters are generated from dc circuits with single-transistor and prescribed dc gains. Three new single-transistor converters are discovered with $M(D) = \frac{D^2}{(1-D)^2}$.

6.1 The Ac Circuits of Four-Switch Converters

The nine possible ac circuits for four-switch, two-switched-network converters are given in Fig. 6.1. Out of the nine circuits, five have two switches in $\mathbf{S}$ and two switches in $\bar{\mathbf{S}}$; and the other four circuits have one switch in $\mathbf{S}$ and three switches in $\bar{\mathbf{S}}$. Ac circuit (4) is dual to ac circuit (5), so is ac circuit (6) to ac circuit (7), and ac circuit (8) to ac circuit (9). The dual circuits of ac circuits (1), (2) and (3) are themselves. By Proposition 2.3, only the converters generated from ac circuits (1) and (2) have neither a loop of capacitors and possible voltage source nor a cut-set of inductors and possible current source in G_1 (or G_2), which is the assumption made in [5].

The graph of ac circuit (2) is separable and can be considered as a combination of two two-switch ac circuits. Thus, each converter of this class is a direct cascade of two-switch converters, and has two transistors and two diodes. Therefore, all the four-switch, single-transistor converters satisfied the assumptions in [5] have ac circuit (1). In this chapter, ac circuit (1) is chosen to demonstrate the synthesis procedure of four-switch converters.

Ac circuit (1) with the reference orientations is shown in Fig. 6.2(a), together with the equivalent circuits during DT_s and $D'T_s$ in (b) and (c). Suppose that $\bar{S}_2$ and $\bar{S}_4$ are chosen

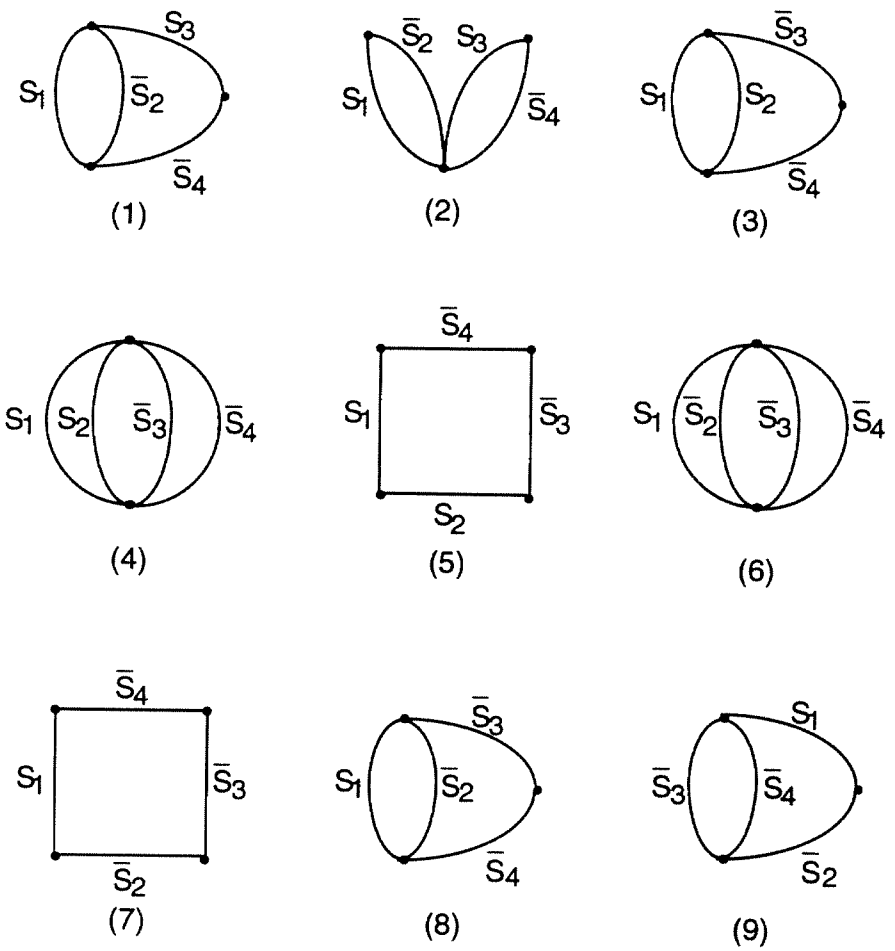


Figure 6.1: The ac circuits of four-switch converters.

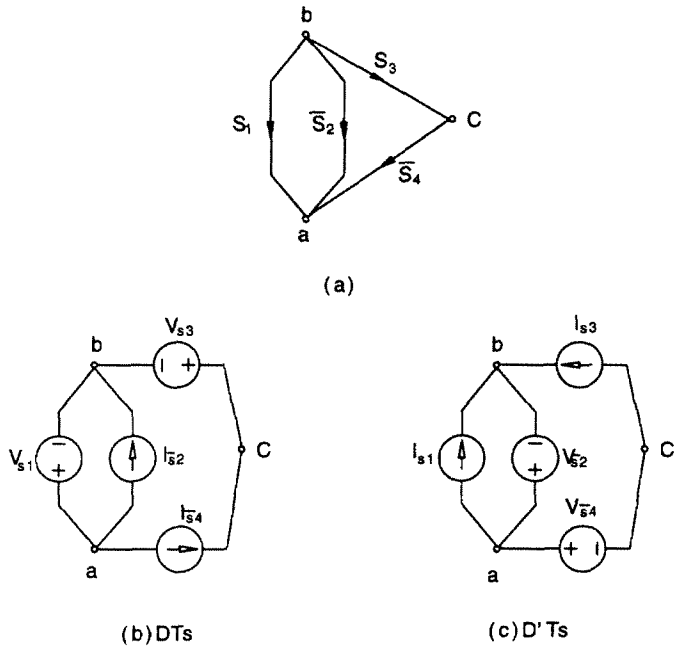


Figure 6.2: The ac circuit with reference orientations(a) and its equivalent circuits: during time interval DT_s when S_1, S_3 are on and $\bar{S}_2$, $\bar{S}_4$ are off(b), and during time interval $D'T_s$ when S_1, S_3 are off and $\bar{S}_2$, $\bar{S}_4$ are on(c).

as tree branches, and S_1 and S_3 as links. Based on the results in Section 2.5.1. We have the following balance equations:

$$\begin{bmatrix} V_{s1} \\ V_{s3} \\ I_{\bar{s}2} \\ I_{\bar{s}4} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{D'}{D} & 0 \\ 0 & 0 & -\frac{D'}{D} & \frac{D'}{D} \\ \frac{D'}{D} & \frac{D'}{D} & 0 & 0 \\ 0 & -\frac{D'}{D} & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{s1} \\ I_{s3} \\ V_{\bar{s}2} \\ V_{\bar{s}4} \end{bmatrix}. \tag{6.1}$$

In ac circuit (1), both l_a and n_a equal two. By Proposition 2.6, in each associated dc circuit the number of tree branches n_d is three and the number of links l_d is one. Enumeration of dc circuits is carried out in the next section.

6.2 Enumeration of Four-Switch Dc Topologies

Each dc circuit associated with ac circuit (1) has four nodes: three terminal nodes 0, 1, 2 and one internal node 3. The possible positions of each switch branch are the same as those for the three-switch dc circuits in Chapter 5, which are shown in Fig. 5.3. A number of the

n	$\bar{S}_2$	S_3	$\bar{S}_4$
1	+	+	+
2	+	+	−
3	+	−	+
4	+	−	−
5	−	+	+
6	−	+	−
7	−	−	+
8	−	−	−

Table 6.1: Orientation of the switches in a four-switch dc circuit.

n	1	2	3	4	5	6	7	8
n'	1	3	2	4	8	6	7	5

Table 6.2: The corresponding relations of n and n'.

form $(i_1 i_2 i_3 i_4.n)$ is used to represent each dc circuit, where i_1, i_2, i_3, $i_4 \in \{1,2,3,4,5,6\}$ denote the positions of switches S_1, $\bar{S}_2$, S_3, $\bar{S}_4$, and $n \in \{1,2,3,4,5,6,7,8\}$ denotes the orientations according to Table 6.1, with + the reference orientation. Notice that S_1 takes the reference orientation by default to avoid redundant cases.

The same converter occurs if S_1 and $\bar{S}_2$, S_3 and $\bar{S}_4$ are interchanged simultaneously. I.e., code $(i_1 i_2 i_3 i_4.n)$ and code $(i_2 i_1 i_4 i_3.n')$ represent identical converter with conversion ratios $M(D)$ and $M(1-D)$, respectively. Since S_1 takes the reference orientation in $(i_1 i_2 i_3 i_4.n)$, while S_2 takes the reference orientation in $(i_1 i_2 i_3 i_4.n')$, n and n' are different. The corresponding relations of n and n' are listed in Table 6.2.

The redundant cases and degenerate cases (Definition 4.1) can be easily eliminated in the computer program implemented to generate dc circuits. The total number of eligible dc circuits is 1864.

6.3 Insertion of Minimum Inductors and Capacitors

As in Chapter 5, a computer program is written to determine the order of dc circuits and implement the reactance-insertion procedure. The algorithm is based on the comparison of two incidence matrices A_a and A_d. It is important to point out that Graph G_a of ac circuit (1) has an isomorphic form $G_a{}'$ as shown in Fig. 6.3. The term "isomorphic" is defined in the following statement [7]:

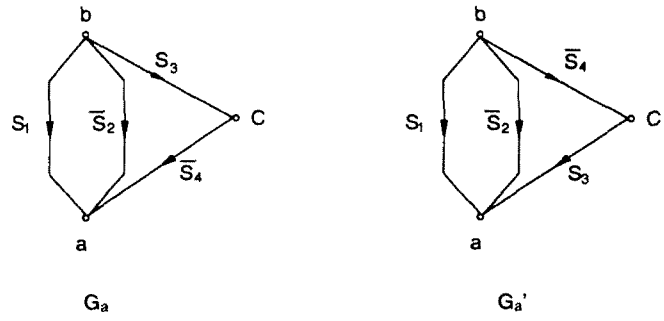


Figure 6.3: Graph G_a of ac circuit (1) has an isomorphic form $G_a{}'$.

Definition 6.1 *Two graphs G and G' are said to be isomorphic (to each other) if and only if their incidence matrices $A(G)$ and $A(G')$ differ only by permutations of rows and columns.*

Suppose that the incidence matrix of $G_a{}'$ is $A_a{}'$. In order to determine the order of a dc circuit (Definition 3.1), A_d of the dc circuit shall be compared with both A_a and $A_a{}'$, respectively. Also, since $l_a = n_a = 2$, by Proposition 3.1, $N_C = N_L$.

As a result, the dc circuits can be classified as follows: 288 fourth-order ($2L2C$) dc circuits; 996 sixth-order ($3L3C$) dc circuits; 526 eighth-order ($4L4C$) dc circuits; and 54 tenth-order ($5L5C$) dc circuits.

A full list of the 288 $2L2C$ (fourth-order) dc circuits can be found in Appendix D, with corresponding dc gains $M(D)$ and switch implementation.

Fourth-order dc circuits with single transistor and particular dc gains $M(D) = D^2$, $M(D) = \frac{1}{(1-D)^2}$, $|M(D)| = \frac{D^2}{1-D}$, $M(D) = \frac{D^2}{(1-D)^2}$ are of special practical interests [5]. They can be used in application where large step-down or step-up is required without transformer or in application that require an extremely large conversion range (such as laboratory power supplies). Converters with minimum elements can be generated from these dc circuits.

Two dc circuits with conversion ratio $M(D) = D^2$ and single transistor are found as shown in Fig. 6.4, together with the two generated converters. Converter $A1$ is generated from dc circuit (4263.5); while converter $A2$ is generated from dc circuit (2463.5).

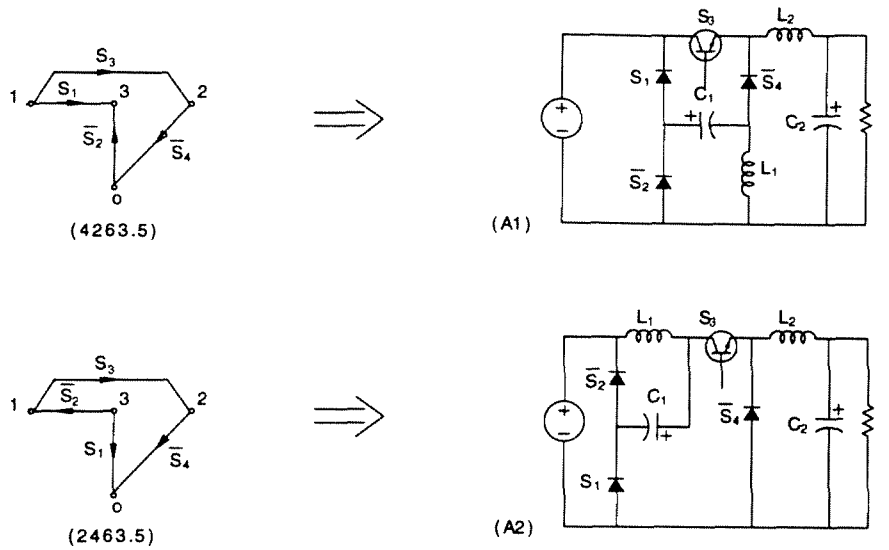


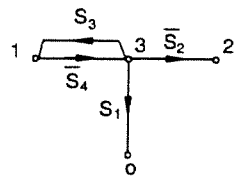
Figure 6.4: Single-transistor dc circuits with $M(D) = D^2$ and the corresponding converters.

One dc circuit (2544.7) is found with conversion ratio $M(D) = \frac{1}{(1-D)^2}$ and single transistor. Four converters can be generated from this dc circuit. The dc circuit and the corresponding converters $B1$, $B2$, $B3$, $B4$ are shown in Fig. 6.5. The positions of inductors are the same for $B2$, $B3$, $B4$. Only the capacitor C_1 connects the internal node $3'$ with different external nodes: 0, 1, or 2, which results in the three distinctive converters.

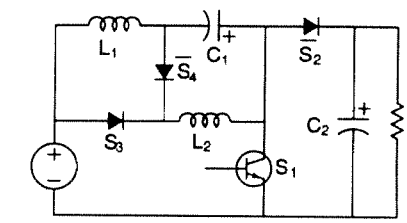
There are three dc circuits that have $|M(D)| = \frac{D^2}{1-D}$ and single transistor, which gives three converters: C_1, C_2, and C_3, respectively. Both the dc circuits and converters in this class are shown in Fig. 6.6.

All the above results tally with those in [5]. However, for conversion ratio $M(D) = \frac{D^2}{(1-D)^2}$, in addition to the only converter discussed in [5], three more are discovered by the new synthesis procedure.

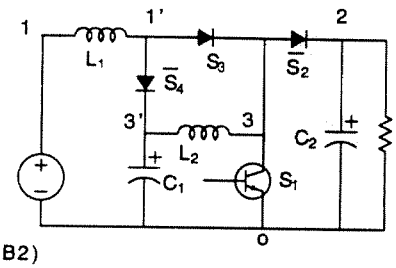
The three dc circuits with conversion ratio $M(D) = \frac{D^2}{(1-D)^2}$, together with the generated converters, are shown in Fig. 6.7. Converter $D1$ is generated from dc circuit (1423.6); $D2$ is generated from dc circuit (2342.8); $D3$ and $D4$ are generated from dc circuit (4522.4). Converter $D2$, $D3$, $D4$ are first discovered.



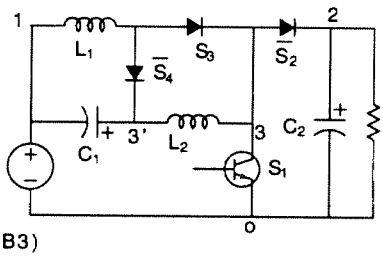
(2544.7)



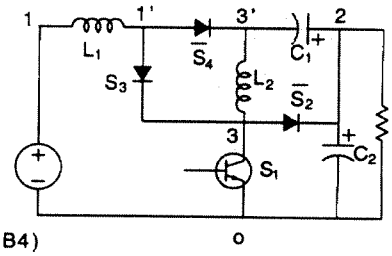
(B1)



(B2)



(B3)



(B4)

Figure 6.5: Single-transistor dc circuits with $M(D) = \frac{1}{(1-D)^2}$ and the corresponding converters.

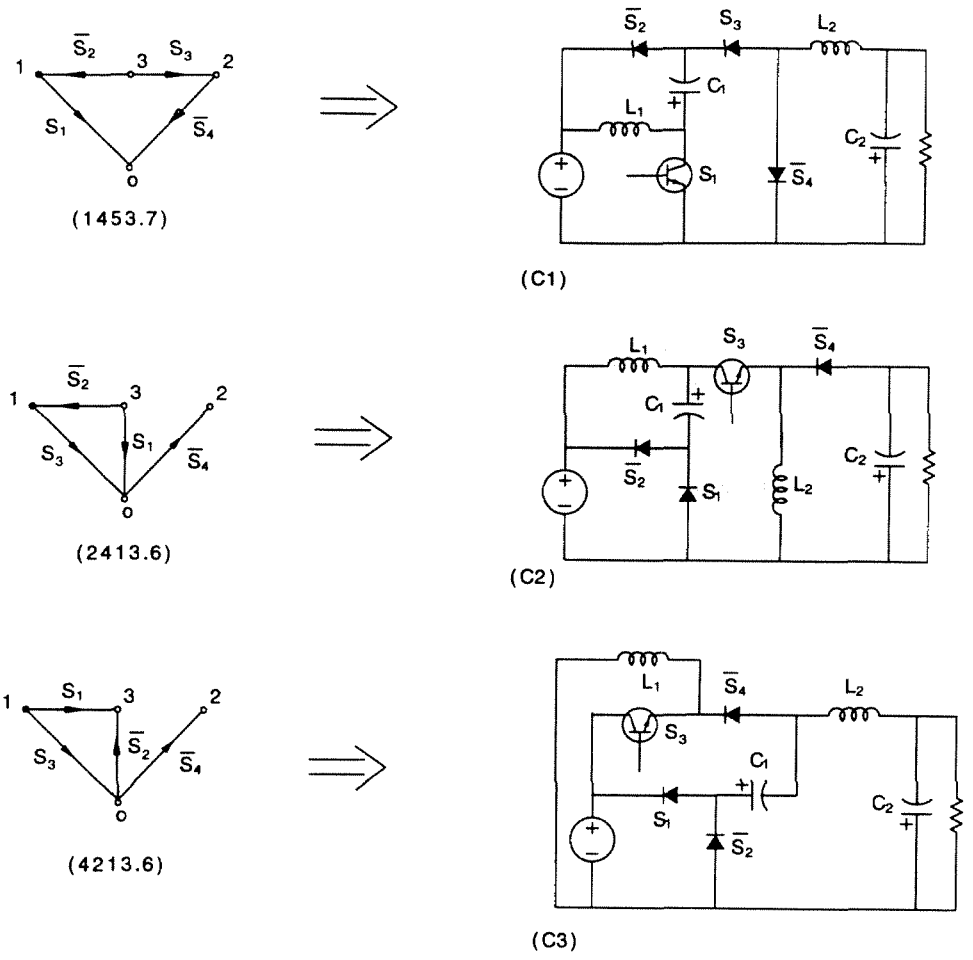


Figure 6.6: Single-transistor dc circuits with $|M(D)| = \frac{D^2}{1-D}$, and the corresponding converters.

Converter $D1$ operates properly only when $D \leq 0.5$. When $D > 0.5$, diodes $\bar{S}_2$ and S_3 clamp the output voltage to V_g so that the step-up function is impossible.

The new converter $D2$ operates with $M(D) = \frac{D^2}{(1-D)^2}$ when $D \geq 0.5$; when $D < 0.5$, diode S_3 is always on and diode S_4 is always off, and converter $D2$ functions as a Sepic converter with $M(D) = \frac{D}{1-D}$.

The new converter $D3$ and converter $D4$ operate properly only when $D \geq 0.5$. When $D < 0.5$, the output voltage is clamped to V_g by diodes S_1 and $\bar{S}_2$ so that step-down function is impossible.

Parameters relevant for comparison of the three new converters are summarized in Table 6.3. For the purpose of comparison, the switches are labeled with t, d_1, d_2, and d_3 as in Fig. 6.7. All the parameters are the same for converter $D3$ and converter $D4$; while with respect to drive, converter $D3$ is the favorable choice compared with D_4 since it employs direct drive. Converter $D2$ also uses direct drive, in addition, it has the advantage of having the step-down function by operating as a Sepic converter when $D < 0.5$. Converter D_2 has less current stress on diode d_2, but higher voltage stress on diode d_3, compared with converters D_3 and D_4. The differences reduce with increasing duty ratio D. Moreover, as proved in Section 2.8 (Eq. (2.66)), $V_{tp}I_{tp} = \sum_{i=1}^{3} V_{dip}I_{dip}$ for any of these converters.

6.4 The Generic Averaged Switch Model

Up to now, we have seen how the separation of switches from the remaining circuit elements can simplify the synthesis procedure of PWM dc-to-dc converters. Another important topic is modeling of large- and small-signal dynamics in PWM converters. The main difficulty in modeling is caused by the non-linear and time-varying features of the switches in PWM converters. Separating the switches from the remaining linear and time-invariant circuit elements poses a new way to model switches. This modeling method is originated in [17], and extended to a generic model for converters with current-mode control or converters in discontinuous inductor current mode [37]. In this section, this method is used to derive the generic averaged switch model for the four-switch converters generated in the present chapter.

All the converters in this chapter are generated from the generic ac circuit in Fig. 6.1(a), with the balance equations in Eq.(6.1). By perturbing Eq.(6.1) and using the small-signal

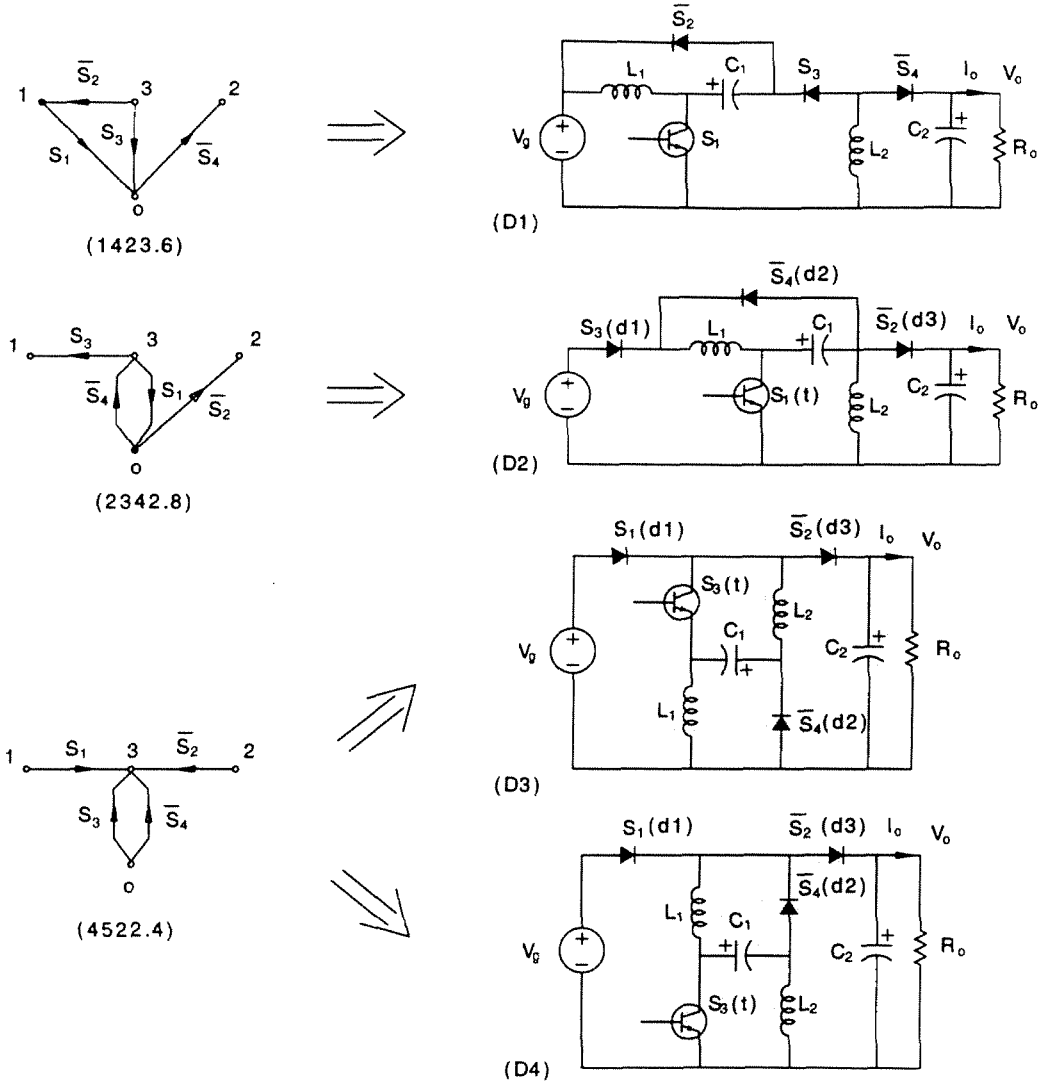


Figure 6.7: Single-transistor dc circuits with $M(D) = \frac{D^2}{(1-D)^2}$, and the corresponding converters.

	D_2	D_3, D_4
V_{tp}	$\frac{D}{(1-D)^2}$	
I_{tp}	$\frac{1}{(1-D)^2}$	
V_{d1p}	$\frac{2D-1}{(1-D)^2}$	
I_{d1p}	$\frac{D}{(1-D)^2}$	
V_{d2p}	$\frac{1}{1-D}$	
I_{d2p}	$\frac{D}{(1-D)^2}$	$\frac{1}{(1-D)^2}$
V_{d3p}	$\frac{D}{(1-D)^2}$	$\frac{2D-1}{(1-D)^2}$
I_{d3p}	$\frac{1}{1-D}$	
I_{L1}	$\frac{D}{(1-D)^2}$	
I_{L3}	$\frac{1}{1-D}$	
I_{C1rms}	$\frac{1}{1-D}\sqrt{\frac{D}{1-D}}$	
I_{C2rms}	$\sqrt{\frac{D}{1-D}}$	
I_{grms}	$\frac{D}{(1-D)^2}\sqrt{D}$	
V_{C1}	$\frac{1}{1-D}$	
V_{C2}	$\frac{D^2}{(1-D)^2}$	

Table 6.3: Comparison of the three new converters with $M(D) = \frac{D^2}{(1-D)^2}$.

assumption, we have the following set of small-signal equations:

$$\hat{V}_1 = \frac{V_2 - V_1}{D}\hat{d} - \frac{D'}{D}\hat{V}_2\,, \tag{6.2}$$

$$\hat{V}_3 = \frac{V_2 - V_3 - V_4}{D}\hat{d} - \frac{D'}{D}\hat{V}_2 + \frac{D'}{D}\hat{V}_4\,, \tag{6.3}$$

$$\hat{i}_2 = -\frac{I_1 + I_2 + I_3}{D}\hat{d} + \frac{D'}{D}\hat{i}_1 + \frac{D'}{D}\hat{i}_3\,, \tag{6.4}$$

$$\hat{i}_4 = \frac{I_3 - I_4}{D}\hat{d} - \frac{D'}{D}\hat{i}_3\,. \tag{6.5}$$

Based on the balance equations, the averaged large-signal model for the switches is shown as in Fig. 6.8(a), which can be used to predict averaged large-signal responses as long as the PWM converter is in continuous inductor current mode. The small-signal circuit model derived from the set of small-signal equations is shown in Fig. 6.8(b), where

$$E_1 = \frac{V_2 - V_1}{D}\,, \tag{6.6}$$

$$E_3 = \frac{V_2 - V_3 - V_4}{D}\,, \tag{6.7}$$

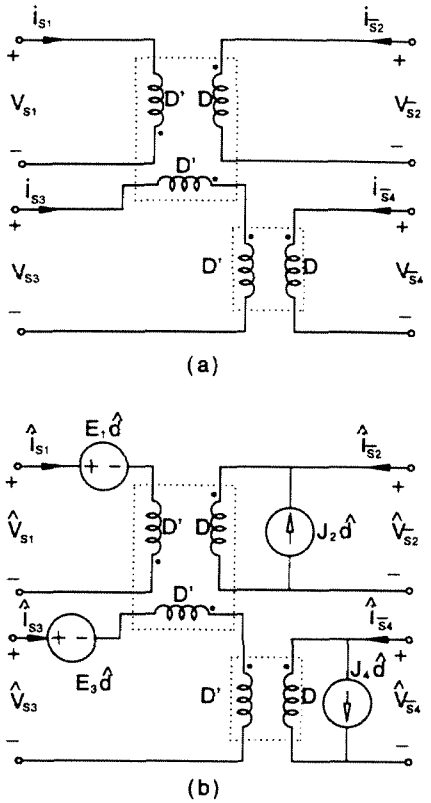


Figure 6.8: The generic averaged switch models for the four-switch converters with the given ac circuit : the large-signal model (a); and the small-signal model (b).

$$J_2 = \frac{I_1 + I_2 + I_3}{D}, \tag{6.8}$$

$$J_4 = \frac{I_3 - I_4}{D}. \tag{6.9}$$

Both models are generic for all the converters generated from this ac circuit, and can be inserted into the converters point-by-point. Therefore, this modeling method is ready to be used in common computer simulation programs (such as PSPICE).

The parasitic elements in the PWM converters (such as ESR associated with capacitors) can be easily taken into account by retaining them in the ac circuit, and consequently in the balance equations. In order to deriving a general model, we can put a symbolic parasitic resistor in each of the switch branch in the generic ac circuit. When the generic model is

applied to a particular PWM converter, the symbolic parasitic resistors can be replaced by physical parasitic elements in the converter, and some of them may have negligible values.

As for the case of two-switch converters [37], extensions of the generic small-signal model can be developed to modeling converters with current-mode control, or converters in discontinuous conduction mode. Further extensions can also be made to cover quasi-resonant converters and soft-switching converters.

6.5 Discontinuous Inductor Current Mode of the Three New Converters

In this section, with the small-ripple assumption removed for inductor currents, converters $D2$, $D3$, $D4$ in Fig. 6.7 are analyzed in the discontinuous inductor current mode (DICM).

In these converters, the DICM occurs when the current through diode d_2 or diode d_3 drops to zero before the end of the transistor off-time.

Define parameters K_1 and K_2 as

$$K_1 \triangleq \frac{2L_1 f_s}{R_o}, \tag{6.10}$$

$$K_2 \triangleq \frac{2L_2 f_s}{R_o}. \tag{6.11}$$

First, consider converter $D2$. As mentioned before, $D2$ operates as a Sepic converter if $D < 0.5$, with diode d_1 constantly on and diode d_2 constantly off. When the transistor is off, the sum of currents i_{L1} and i_{L2} goes through diode d_3, the diode current decays linearly and reaches its minimum at the end of the transistor off-time. For the converter to operate in CICM, the minimum should be positive, i.e.,

$$I_{L1} + I_{L2} - \frac{\Delta I_{L1}}{2} - \frac{\Delta I_{L1}}{2} > 0, \tag{6.12}$$

where I_{L1} and I_{L2} denote the average currents of L_1 and L_2, respectively; and ΔI_{L1} and ΔI_{L2} denote the peak-to-peak ripple currents of L_1 and L_2, respectively. After evaluating the average and ripple currents in terms of V_g, L_1, L_2, R_o and f_s, we have the boundary

condition as

$$K_e > (1-D)^2, \tag{6.13}$$

$$\text{where } K_e \triangleq K_1 \parallel K_2. \tag{6.14}$$

In fact, this is the boundary condition for any two-inductor converters with $M(D) = \frac{D}{D'}$ (such as, Ćuk converter, Sepic converter and Dual Sepic converter). Also the dc gain can be obtained as

$$M(D) = \frac{D}{\sqrt{K_e}}. \tag{6.15}$$

When $M(D) \geq 1$, i.e., $D \geq \sqrt{K_e}$, the output voltage is clamped to V_g by diodes d_1, d_2, and d_3. The operating modes for $D < 0.5$ can be summarized as follows:

1. If $K_e > (1-D)^2$, converter $D2$ operates in CICM, with $M(D) = \frac{D}{D'}$.

2. If $D^2 < K_e < (1-D)^2$, converter $D2$ operates in DICM, with $M(D) = \frac{D}{\sqrt{K_e}}$.

3. If $K_e < D^2$, V_o is clamped to V_g, i.e., $M(D) = 1$.

If $D > 0.5$, converter $D2$ operates with $M(D) = \frac{D^2}{(1-D)^2}$. When the transistor is off, diode d_3 conducts current i_{L2}. A similar analysis gives the boundary condition as

$$K_2 > (1-D)^2, \tag{6.16}$$

which is the same as the boundary condition for the buckboost converter. Again, analysis for diode d_2 yields

$$K_1 > \frac{(1-D)^4}{D^2}. \tag{6.17}$$

This condition can also be viewed as the condition for the buckboost converter, except that load R_o is reflected to the input stage by the inverse square of the output stage dc gain $\frac{D}{1-D}$.

Since converters $D3$ and $D4$ only operate effectively for $D > 0.5$, analysis of boundary condition for operation is carried out for converters $D3$ and $D4$ in this duty ratio range. The results are the same as in Eqs. (6.16) and (6.17).

For converters D_3, D_4, and converter D_2 in the range of duty ratio $D \geq 0.5$, the

boundary conditions in Eqs. (6.16) and (6.17) become most restrictive when $D = 0.5$, i.e.,

$$K_1 > 0.25, \tag{6.18}$$

$$K_2 > 0.25. \tag{6.19}$$

For converter D_2 in the range of duty ratio $D < 0.5$, the boundary condition in Eq. (6.13) becomes most restrictive when $D = 0$, i.e.,

$$K_e > 1, \tag{6.20}$$

which can be rewritten into

$$\frac{1}{K_1} + \frac{1}{K_2} < 1. \tag{6.21}$$

Under the condition in Eq. (6.21), the sum $K_1 + K_2$ is minimized when $K_1 = K_2 = 2$, which is, equivalently speaking, the case of the minimum boundary inductances for converter D_2 to operate in CICM in the whole duty ratio range (0,1).

6.6 Experimental Verification of the Three New Converters

Prototypes of converter $D2$ and converter $D4$ are built to verify the theoretical predictions. Parameters of the experimental circuits are:

1. - inductors: $L_1 = L_2 = 0.46mH$;
2. - capacitors: $C_1 = 30\mu F$, $C_o = 100\mu F$;
3. - transistor: IRF640;
4. - diodes: UES1306;
5. - switching frequency: $f_s = 50kHz$;
6. - input voltage: $V_g = 10V$;
7. - load resistor: $R_o = 180\Omega$.

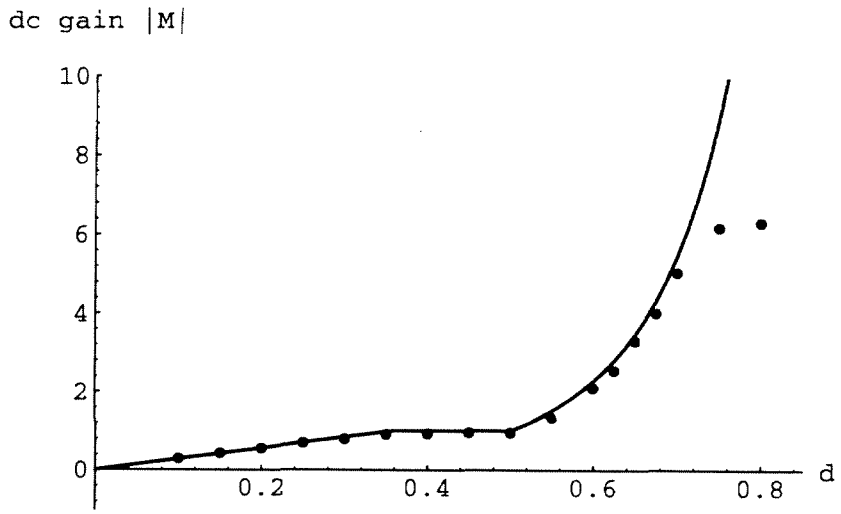


Figure 6.9: The measured and predicted conversion ratios for converter $D2$.

For the given parameters, we have $K_1 = K_2 = 0.256$. Since conditions (6.18) and (6.19) are satisfied, converter $D2$ and $D4$ operate in CICM for duty ratio $D \geq 0.5$. On the other hand, condition (6.13) is always not satisfied for duty ratio $D < 0.5$, thus, converter $D2$ operates in DICM when $D \geq \sqrt{K_e} = 0.357$; For $0.357 < D < 0.5$, the output voltage is clamped to $V_g - V_d$ (where V_d is the diode forward drop) by diodes d_1, d_2 and d_3.

The measured dc gain of converter $D2$ as a function of the duty ratio, together with the theoretical curve, is shown in Fig. 6.9. The measured ratios are slightly below the theoretical prediction, since the on-voltages of the semiconductor devices and the parasitic elements in the converter has not been taken into account in the analysis (although if desired, they could be easily taken into account). The discrepancy becomes more obvious with the increasing duty ratio D since the increasing load current aggravates the on-voltages and voltage drops on parasitic elements.

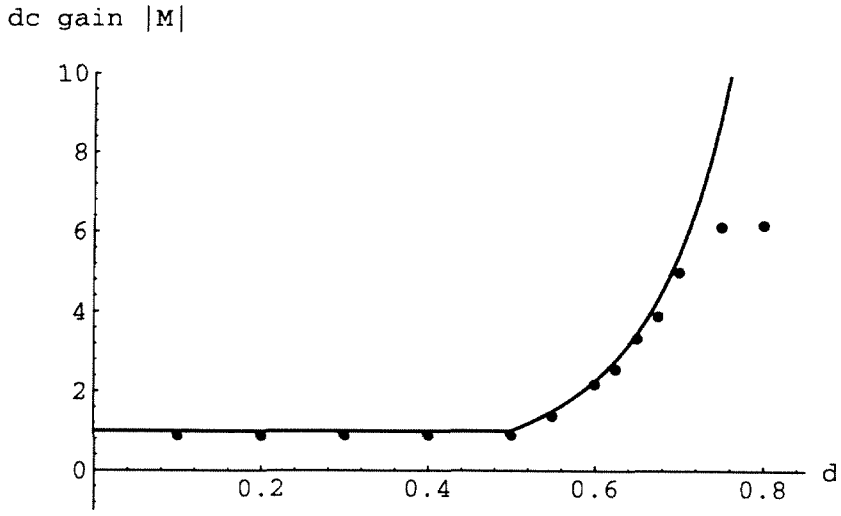


Figure 6.10: The measured and predicted conversion ratios for converter $D4$.

The measured dc gain of converter $D4$ as a function of the duty ratio, together with the theoretical curve, is shown in Fig. 6.10. As predicted, when the duty ratio $D < 0.5$, the output voltage is clamped to $V_g - 2V_d$ by diode d_1 and diode d_3.

Chapter 7 Synthesis of Three-Switch, Three-Switched-Network Dc-to-Dc Converters

In this chapter, the synthesis procedure is extended to converters with more than two switched-networks. Without loss of generality, key ideas of this extension are illustrated through synthesis of a class of three-switch, three-switched-network (3SN) converters.

The generic ac circuit is described and balance equations are given in Section 7.1. Enumeration of dc topologies with a set of prescribed properties is carried out in Section 7.2. Finally, inductors and capacitors are inserted to generate 3SN PWM converters. Only the converters with relatively lower order ($2L2C$) are of most practical interest and are given in Section 7.3.

It needs to be mentioned that most of the converters generated in this chapter were first found in [14]. However, the systematic synthesis procedure here guarantees that the search of the whole class is complete.

7.1 The Ac Circuit for the Class of Three-Switch Three-Switched-Network Converters

The generic ac circuit is shown in Fig. 7.1. The control sequence is as follows: During D_1T_s, S_1, S_2 are on, and S_3 is off; during D_2T_s, S_1, S_3 are on, and S_2 is off; and during D_3T_s, S_2, S_3 are on, and S_1 is off. Recall that, this is the ac circuit of 3SN Ćuk converter discussed in Section 2.7, and the equivalent circuits are shown in Fig. 2.7. The derived balance equations are

$$\begin{bmatrix} V_{s1} \\ V_{s2} \\ I_{s3} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{D_3}{D_1} \\ 0 & 0 & \frac{D_2}{D_1} \\ -\frac{D_3}{D_1} & -\frac{D_2}{D_1} & 0 \end{bmatrix} \begin{bmatrix} I_{s1} \\ I_{s2} \\ V_{s3} \end{bmatrix}. \tag{7.1}$$

The number of linearly independent volt-second balance equations q equals 2. By Eqs. (2.57) and (2.58), each associated dc circuit has $n_d = 3$ tree branches and no link.

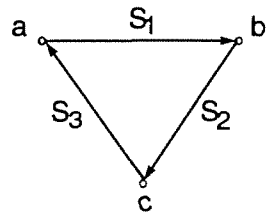


Figure 7.1: The generic ac circuit of a class of 3SN converters.

The possible associated dc circuits with prescribed properties are enumerated in the next section.

7.2 Enumeration of Possible Dc Topologies

The general dc structure has four nodes, which is the same as that of two-switched-network converters in Chapter 5. The six possible positions for each branch are shown in Fig. 5.3. Instead of enumerating all the possible dc circuits exclusively, we are going to select only the dc circuits with prescribed properties.

Recall that, the basic converters with single controllable duty-ratio have to regulate the output voltage against both input voltage and load current variations. The possible wide input voltage range leads to large variation in the duty ratio and operating point. Consequently, the bandwidth has to be compromised to insure stability under all operating conditions. In a 3SN converter, with the additional control variable provided by the third switched-network, it is possible to decouple the two disturbance sources. Since the roles of S_1, S_2 and S_3 are exchangeable, we can assume that the two controllable duty-ratios are D_1 and D_3. The decoupling in the dc conversion ratio is possible if and only if the output voltage of the converter is of the form:

$$V_o = f_1(V_g\,,\, D_1)\; f_2(I_o\,,\, D_3)\,, \tag{7.2}$$

where f_1 and f_2 are two arbitrary functions, and I_o is the load current.

Also, to avoid redundant cases, i_1 is chosen to be less than i_2. The only possible dc gain which satisfies Eq. (7.2) is

$$|M(D)| = \frac{D_1}{D_3}\,. \tag{7.3}$$

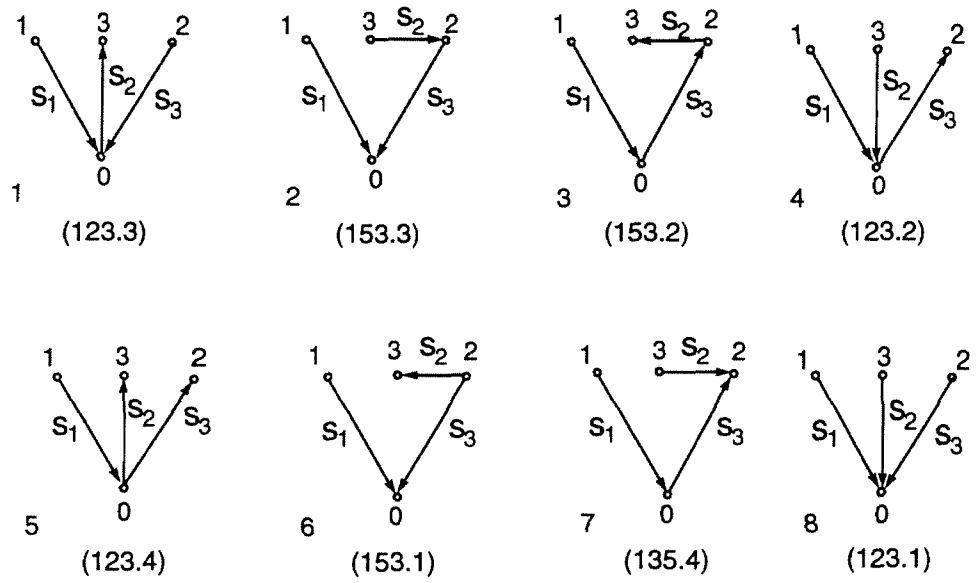


Figure 7.2: Dc circuits for three-switch, 3SN converters with decoupled input and output control variables.

Thus, in the dc topology, S_1 is placed at position 1, and S_3 is placed at position 3, where the positions are defined in Fig. 5.3. Consequently, the positions for S_2 are position 2, position 4 and position 5. In each position, S_2 is the only branch connected with node 3, therefore, we have $I_{s2} = 0$. From Section 2.7, S_2 is a current-bidirectional switch. Also, it can be shown that S_1 is a transistor and S_3 is a diode. Since it is preferred to have one controllable switch at the secondary side when isolation is implemented, position 4 is excluded for S_2. Furthermore, to avoid redundancy cases, the reference orientation is chosen for S_1 by default, and the orientations for S_2 and S_3 are denoted by n as in three-switch, two-switched-network case (Table 5.1). Similarly, each dc circuit is represented by a number of the form $(i_1 i_2 i_3.n)$. A total of eight dc circuits are generated as shown in Fig. 7.2.

7.3 Insertion of Inductors and Capacitors

The positions of inductors and capacitors are decided by comparing the incidence matrices of graphs G_a and G_d. Similar to the four-switch case in Chapter 6, graph G_a has an isomorphic form $G_a{}'$ as shown in Fig. 7.3.

The incidence matrix A_d shall be compared with the incidence matrices of both isomorphic graphs (A_a and $A_a{}'$) to determine the minimum number of necessary reactive elements.

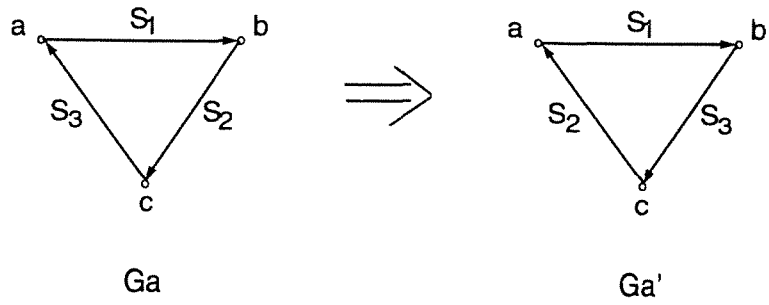


Figure 7.3: Isomorphic graph $G_a{}'$ of the graph G_a.

As a result, five out of the eight dc circuits are fourth-order (where $2L2C$ are the minimum elements needed to generate at least one viable converter.): dc circuits (1) through (5). The remaining three dc circuits (6, 7, 8) are sixth-order (3L3C). Only the fourth-order dc circuits are discussed here.

Converters from dc circuits (1) and (2) are shown in Fig. 7.4(a) and (b), which can be viewed as extensions of Sepic and Zeta converters, respectively.

The three possible converters from dc circuit (3) are shown in Fig. 7.4(c), (d) and (e). The converter in (c) is the most favorable choice since the isolation is easier to implement compared with the other two; also only the input current goes through L_1 instead of the sum of input and output currents. This converter is an extension of the Ćuk converter.

The four converters generated from dc circuit (4) are shown in Fig. 7.4(f) through (i). Note that, converters (f), (g) and (h) are developed by enumerating the two inductors between the three positions among nodes 0, 0′ and 0″, with all the other circuit elements being kept in the same positions. In graph G_d of their dc circuits, the two inductors are shorted. Consequently, the three nodes are combined into one as required. From application point of view, the converter in (h) is not suitable, since if L_2 is replaced by an isolated transformer, both controllable switches S_1 and S_2 are on the primary side, a separate control on the secondary side is impossible. Among the converters in (f), (g), and (i), the benefit of converter (f) is that L_1 is only subject to input current. While converter (i) has the advantage of using direct drive for S_2.

Finally, the converters derived from dc circuit (5) are the same as those from dc circuit (4) with the positions of S_2 and C_1 interchanged.

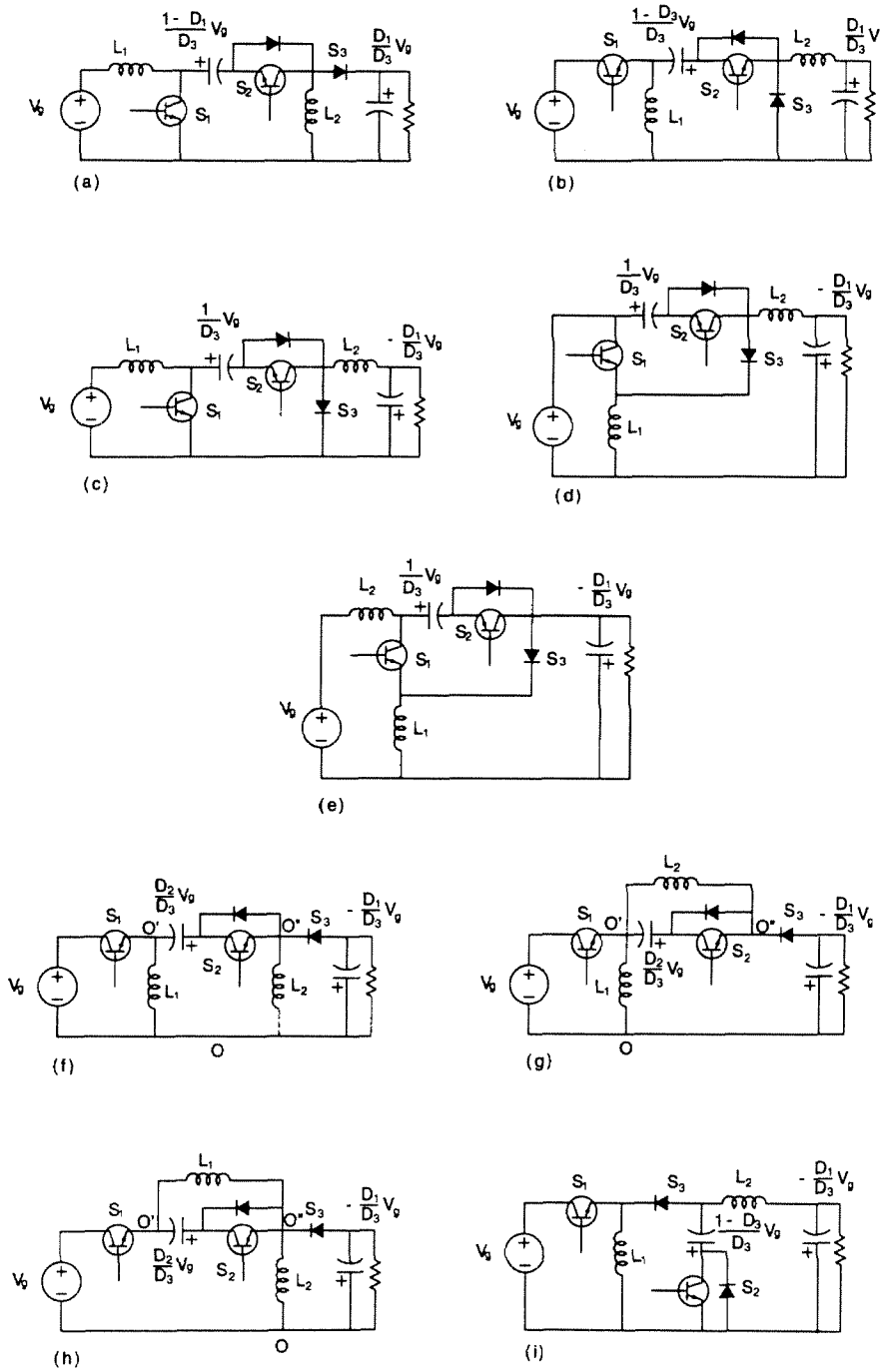


Figure 7.4: Three-switch, 3SN, PWM converters.

7.4 Conclusion

Converters in Fig. 7.5(a), (b), (c), (i) are the same as the capacitor idling converters originally proposed in [14]. However, the systematic synthesis approach here guarantees that the search of the converters with a set of prescribed properties is exclusive.

Chapter 8 Synthesis of Three-Switch, Two-Output Dc-to-Dc Converters

In applications which require more than one dc voltage, multiple-output converters are often used to reduce size and cost and to increase efficiency.

A special class of converters is generated in this chapter. Each has two outputs with equal value but opposite polarity voltages. For applications when galvanic isolation is not required, these converters provide a simple way to supply both positive and negative output voltages without using transformers.

Another important issue about multiple-output converters is how to improve cross-regulation, especially during light load condition. A detailed study about cross-regulation improvement at light load by use of the coupled inductors will be given in Chapter 10.

8.1 The Ac Circuit of Three-Switch, Two-Output Converters

There are two possible ac structures for three-switch converters as shown in Fig. 5.1. In ac circuit (1), l_a equals 2, by Eq. (2.34), the number of outputs $N_o \leq 2$. While in ac circuit (2), l_a equals 1, by Eq. (2.34), only one output is possible. Therefore, intervals. The corresponding balance equations are

$$\begin{bmatrix} V_{\bar{s}2} \\ V_{\bar{s}3} \\ I_{s1} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{D}{D'} \\ 0 & 0 & -\frac{D}{D'} \\ \frac{D}{D'} & \frac{D}{D'} & 0 \end{bmatrix} \begin{bmatrix} I_{\bar{s}2} \\ I_{\bar{s}3} \\ V_{s1} \end{bmatrix}. \tag{8.1}$$

As in Chapter 5, each associated dc circuits has four nodes. Enumeration of dc circuits with certain property is carried out in the next section.

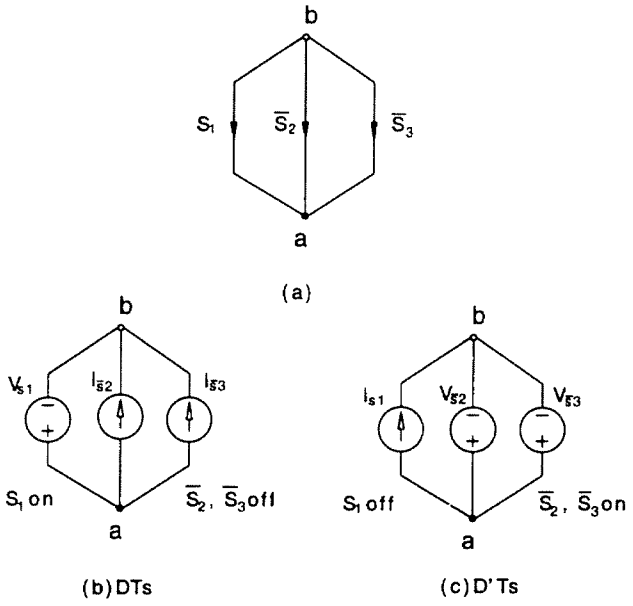


Figure 8.1: The ac circuit of three-switch, two-output converters(a), and its equivalent circuits: during DT_s when S_1 is on and $\bar{S}_2$, $\bar{S}_3$ are off(b); and during $D'T_s$ when S_1 is off and $\bar{S}_2$, $\bar{S}_3$ are on(c).

8.2 Enumeration of Dc Circuits with Equal and Opposite Polarity Outputs

For the two-output case, all four nodes in each G_d are terminal nodes. Suppose the first output is connected between node 2 and the ground (node 0); and the second output is connected between node 3 and the ground. Define $M_1 = \frac{V_{o1}}{V_g}$ and $M_2 = \frac{V_{o2}}{V_g}$. We can sort out three distinctive dc circuits that provide equal value and opposite polarity output voltages, which are shown in Fig. 8.2.

For each dc circuit, M_1, M_2 can be determined and switches can be implemented from the balance equations and dc topologies. The results are as follows:

Dc circuit 1: $M_1 = \frac{D}{D'}$, $M_2 = -\frac{D}{D'}$. S_1 is transistor, $\bar{S}_2$ and $\bar{S}_3$ are diodes.

Dc circuit 2: $M_1 = D$, $M_2 = -D$, S_1 is transistor, $\bar{S}_2$ and $\bar{S}_3$ are diodes.

Dc circuit 3: $M_1 = \frac{D}{2D-1}$, $M_2 = \frac{D}{1-2D}$. S_1, $\bar{S}_2$, and $\bar{S}_3$ are voltage-bidirectional switches: when $D < 0.5$, S_1 is transistor, $\bar{S}_2$ and $\bar{S}_3$ are diodes; when $D > 0.5$, S_1 is diode, $\bar{S}_2$ and $\bar{S}_3$ are transistors.

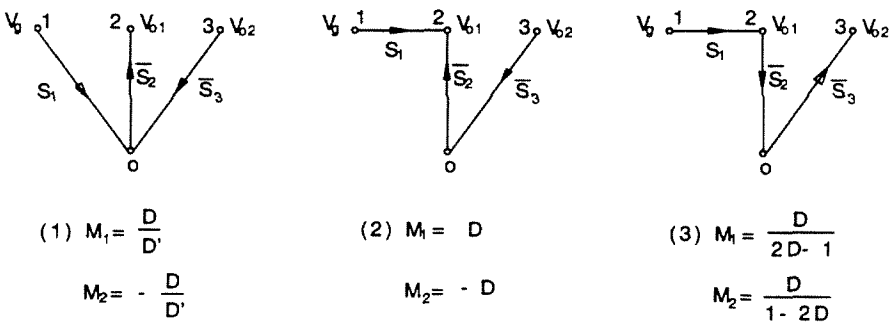


Figure 8.2: The three dc circuits that provide equal and opposite polarity output voltages.

The switch implementations of the three dc circuits are shown in Fig. 8.3.

Note that, for dc circuit (3), the theoretical $M(D)$ goes to infinity when D is close to 0.5, which implies that the actual conversion ratio near $D = 0.5$ is determined by parasitic elements that are not included in the idea model here. Consequently, dc circuit (3) is of less practical interest.

8.3 Insertion of Inductors and Capacitors

By Proposition 3.1, the number of capacitors N_C is always greater than the number of inductors N_L by 1 in all the converters generated from the generic ac circuit in Fig. 8.1. Here, we only include the converters with $N_L \leq 3$ and $N_C \leq 4$. Furthermore, since there are only two nodes in G_a, by Proposition 4.1, all the *essential* inductors inserted have the same voltage waveform and therefore can be coupled on a single magnetic core to save space and steer the ac ripple from input and/or output terminals.

For dc circuit (1), four converters generated are shown in Fig. 8.4. Converter $A1$ has the minimum number of inductors and capacitors. It can be viewed as a combination of a flyback converter and a dual Sepic converter, with S_1 and L_1 shared by both. The dual Sepic side gives the positive output voltage and the flyback side provides the negative output voltage. The positive output has continuous current, also the ac ripple in this output can be reduced to ideally zero by coupling L_1, L_2 and steering all the ripple to L_1. Converter

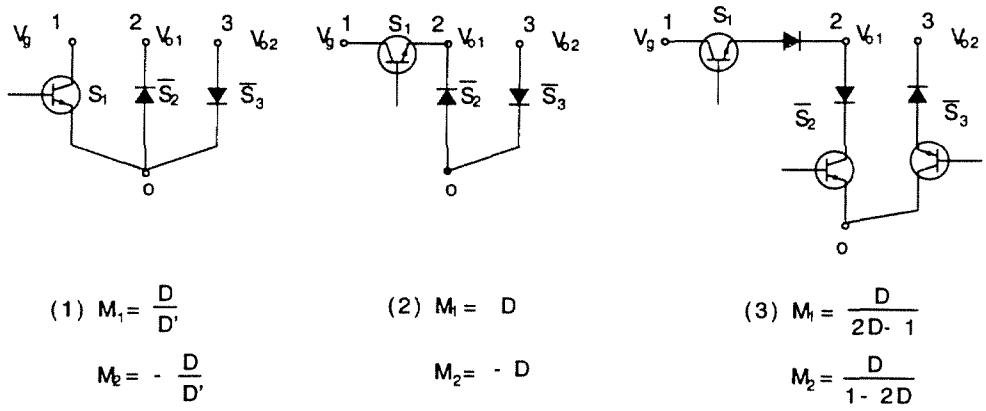
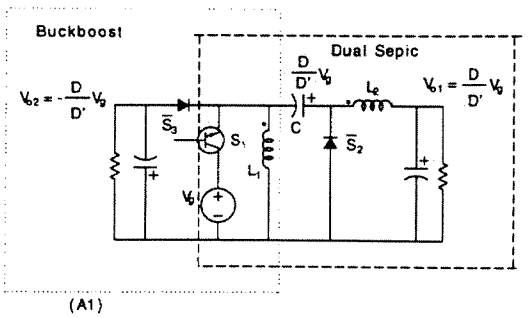


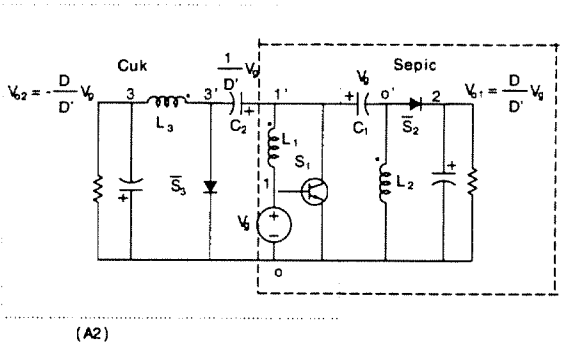
Figure 8.3: The switch implementation of three-switch dc circuits of two-output converters.

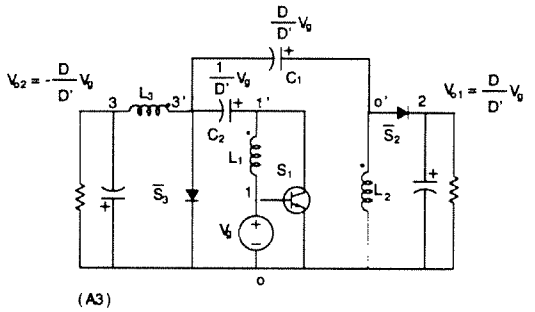
$A2$ can be considered as a combination of a Ćuk converter and a Sepic converter with S_1 and L_1 shared by both. Converter $A3$ can be derived from converter $A2$ by keeping C_2 in the same position and changing C_1 to that between nodes $0'$ and $3'$, and converter $A4$ can be derived by keeping C_1 in the same position and changing C_2 to that between nodes $0'$ and $3'$. Here, the requirement is that, in graph G_d of the ac circuit, nodes $0'$, $1'$, and $3'$ have to be shorted by capacitors into one node. Obviously, the sum $V_{C1} + V_{C2}$ is minimized in converter $A4$. Except the two capacitors, the other circuit elements keep the same position in converters $A2$, $A3$, and $A4$. The three inductors in each converter can be coupled on a single core, and ripple steering can be used to remove the ac ripple from the input and the negative output side. Converters $A2$, $A3$, and $A4$ have the advantages of continuous input current and direct drive compared with converter $A1$, with the price of an additional inductor and capacitor.

Four converters generated from dc circuit (2) are shown in Fig. 8.5. Converter $B1$ has the minimum number of reactive elements, and continuous output current at the positive side. Converters $B2$, $B3$ and $B4$ have continuous input current and continuous output current on the negative output side. Again, converters $B3$ and $B4$ can be derived from converter $B2$ by changing the position of C_1 or C_2. The sum of the voltage stresses on C_1 and C_2 is minimized in Converter $B2$. All the inductors can be coupled in each of the four converters.

Six converters are generated from dc circuit (3), as shown in Fig. 8.6. Each has three







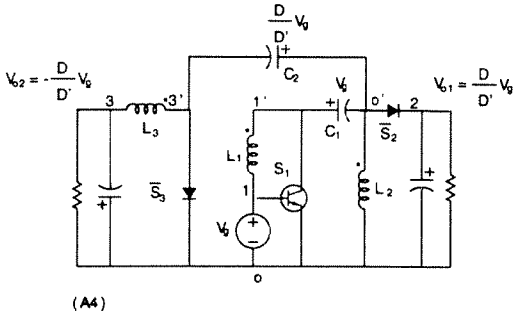


Figure 8.4: Two-output converters from dc circuit (1): $|M(D)| = \frac{D}{D'}$.

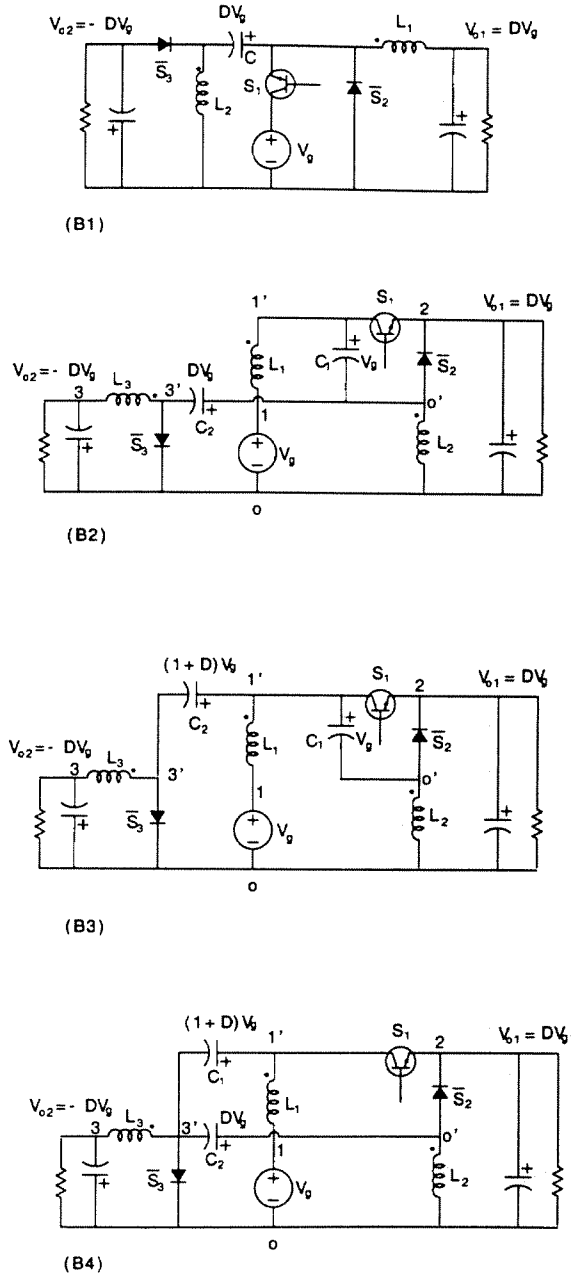


Figure 8.5: Two-output converters from dc circuit (2): $|M(D)| = D$.

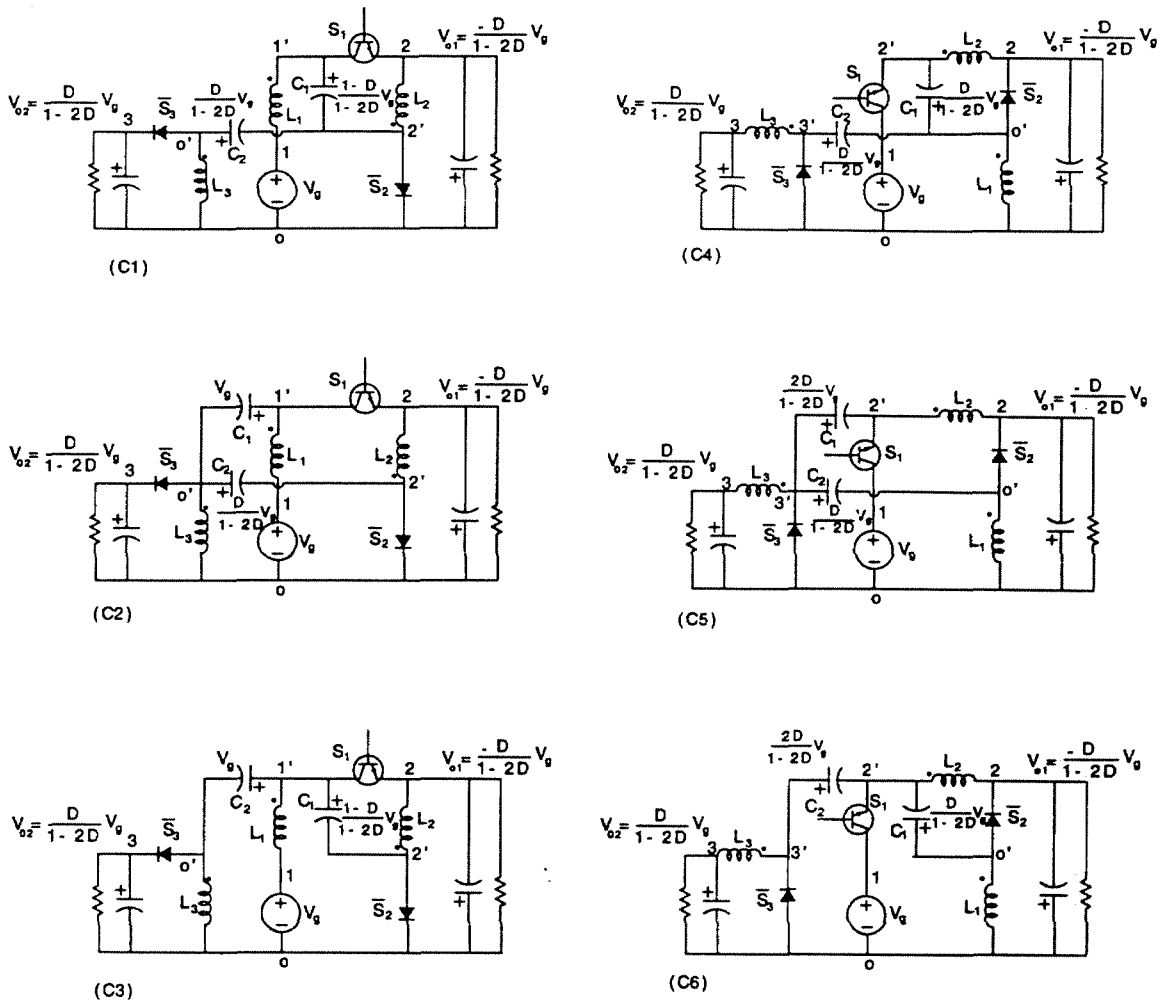


Figure 8.6: Two-output converters from dc circuit (3): $|M(D)| = \frac{D}{2D-1}$.

inductors and four capacitors. All the inductors can be coupled and ripple steering can be applied if needed. Again, converters $C2$ and $C3$ can be derived from converter $C1$ by changing the positions of capacitors; and in a similar way, converters $C5$ and $C6$ can be derived from converter $C4$. Note that, the types of switches of dc circuit (3) shown in Fig. 8.6 are for $D < 0.5$. If $D > 0.5$, the transistor should be replaced by a diode, and the diodes should be replaced by transistors. Or if D varies in the whole range of (0, 1), voltage-bidirectional switches should be employed.

If independent control of each output is desired, it can be achieved by operating one output in continuous inductor current mode (CICM) and the other in discontinuous inductor current mode (DICM) [11, 12]. Therefore, a second control variable, namely the switching

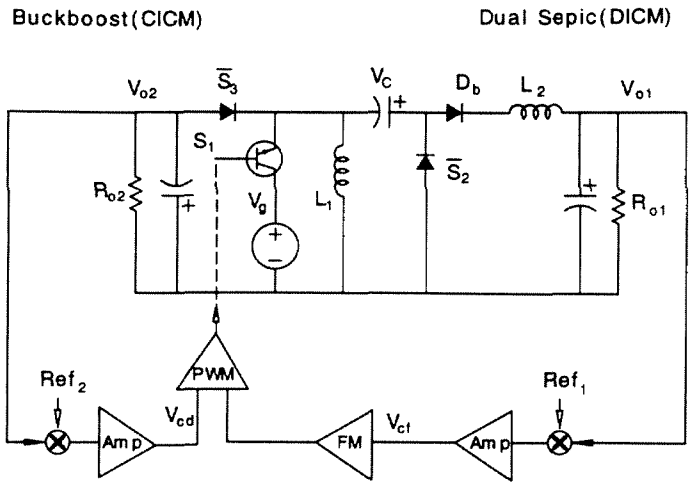


Figure 8.7: The two-loop control scheme to have independent outputs is illustrated on converter $A2$.

frequency, can be used to regulate the DICM output.

The scheme of the two-loop regulator is illustrated on converter $A1$, as shown in Fig. 8.7. Diode D_b is used to decouple the voltage waveforms across L_1 and L_2. L_2 can be designed to have discontinuous inductor current; while the current in L_1 remains continuous. Consequently, the first output is in DICM, and the second output in CICM. The control loop for the second output is closed through the pulse-width modulator in the common way, and the control loop for the first output is closed through a frequency modulator so that the switching frequency f_s is modulated by the amplified error signal from this DICM output. The conversion ratio for the first output is

$$M_1 = \frac{V_{o1}}{V_g} = \frac{D}{\sqrt{K}}, \tag{8.2}$$

$$\text{where} \quad K = \frac{2L_2 f_s}{R_{o1}}. \tag{8.3}$$

The difference between V_{o1} and V_c is supported by diode D_b. Same scheme can be used for any of the converters generated in this chapter. For example, in converter $A2$, we can add a diode in series with L_2, or in series with L_3 to decouple the voltage waveforms across them. Then, L_2 or L_3 can be designed to have the corresponding output operating in DICM, so that the two outputs can be controlled independently.

Chapter 9 A Three-Switch High-Voltage Converter

The aim of this chapter is to study a novel three-switch converter (SU(1) in Fig. 5.6).

This converter can operate into a capacitor-diode voltage multiplier, which offers simpler structure and control, higher efficiency, reduced EMI, size and weight savings compared with traditional switched-mode regulated voltage multipliers. Two significant advantages are the continuous input current and easy isolation extension. The new converter is experimentally verified. Both the steady state and dynamic theoretical models are correlated well with the experimental data.

9.1 Introduction

In high-voltage/low-current applications, such as TV-CRT's, lasers, X-ray systems, ion pumps, electrostatic systems etc., a capacitor-diode voltage multiplier is usually preferable to a transformer with large turns ratio and diodes with enormous breakdown voltages. A transformer with a large turns ratio is undesirable because it exacerbates the transformer nonidealities: the leakage inductance and the winding capacitance. These nonidealities cause voltage and current spikes, and increase loss and noise.

A common PWM-controlled voltage-multiplier [21] is shown in Fig. 9.1, where a buck converter is followed by a push-pull voltage multiplier. The main disadvantages of this converter are: the circuit requires two stages including three switches and complex control system, which increases loss and cost; the input current is discontinuous, thus input filter is invariably required to smooth out the switching ripple; high power factor is hard to realize with the buck pre regulator.

In this chapter, we propose a novel single stage high-voltage converter , which can be used to drive voltage multipliers [16]. It eliminates the above drawbacks, reduces the size and cost, increases the efficiency and reliability.

The basic operation of the new converter is explained in Section 9.2. Dynamic analysis

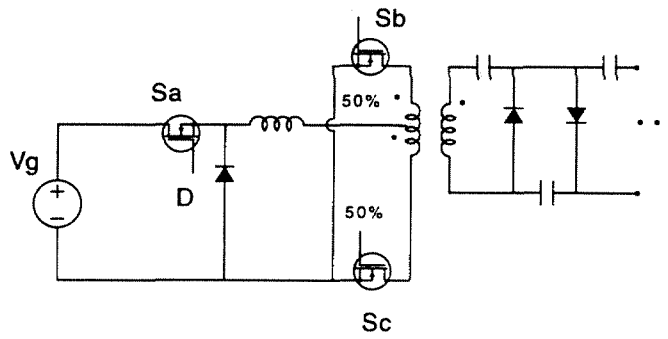


Figure 9.1: A common PWM-controlled voltage multiplier.

and transfer functions are given in Section 9.3. In Section 9.4, extensions for the basic three-switch version are discussed. Soft-Switching mechanism is explained in Section 9.5. The experimental results are present in Section 9.6, and conclusion is given in Section 9.7.

9.2 Basic Operation of the New Converter

9.2.1 Continuous Inductor Current Mode (CICM)

The basic version of the HV converter is shown in Fig. 9.2(a). It appears like the Ćuk converter, except that the output inductor of the Ćuk converter is replaced by a diode. The cost for doing so is the loss of continuous output current, but in applications which require very high output voltage and small output current, the new converter gives substantial savings in size and weight.

The basic operation for the converter is as follows: At the beginning of each switching cycle, Q_1 is turned on, the equivalent circuit is shown in Fig. 9.2(b). Since the voltage across C_1 is larger than that of C_2, D_2 is turned on simultaneously, and D_1 is off because of the negative output voltage across it. C_1 is charging the output capacitor C_2 and the load resistor R_L (note that the peak of the charging current is limited by ESR's associated with C_1 and C_2). At the end of DT_s period, Q_1 is turned off, the circuit is equivalent to that of Fig. 9.2(c). The input inductor current forces D_1 to turn on. Then, D_2 is turned off by the

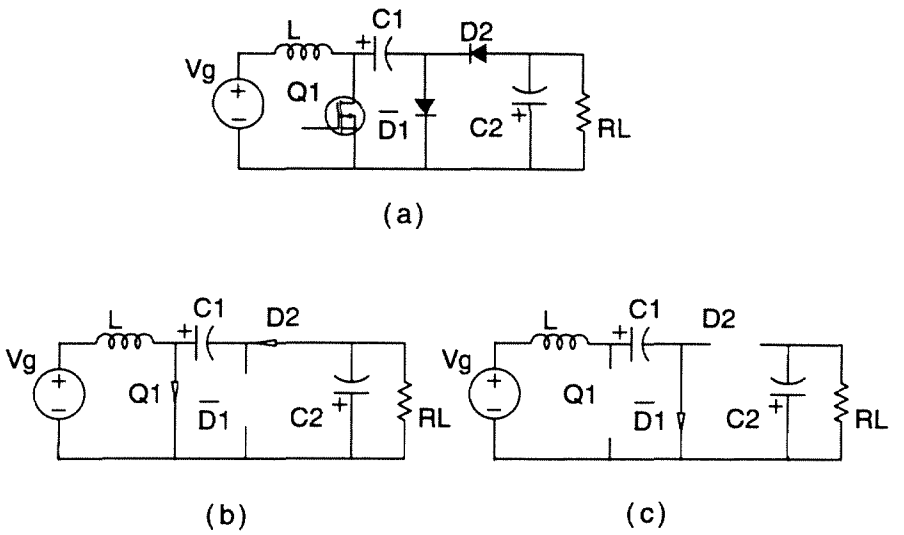


Figure 9.2: The new three-switch HV converter: the basic version(a); the equivalent circuit during DT_s (b); and the equivalent circuit during $D'T_s$(c).

negative output voltage. In this period, C_1 is being charged up by the inductor current; while C_2 is being discharged to supply the load current. If the parasitics are neglected, the voltage conversion ratio M can be easily derived as in Chapter 5.

$$M = \frac{V}{V_g} = -\frac{1}{D'}. \tag{9.1}$$

The new converter can also be developed from the boost converter, by exchanging the positions of the diode and the capacitor in the boost converter, and adding another diode and output capacitor. As a result, the new converter shares many similar properties with the boost converter. However, unlike the boost converter, the new converter can be easily extended to provide dc isolation and drive capacitor-diode voltage multiplier. These features will be discussed later in Section 9.4.

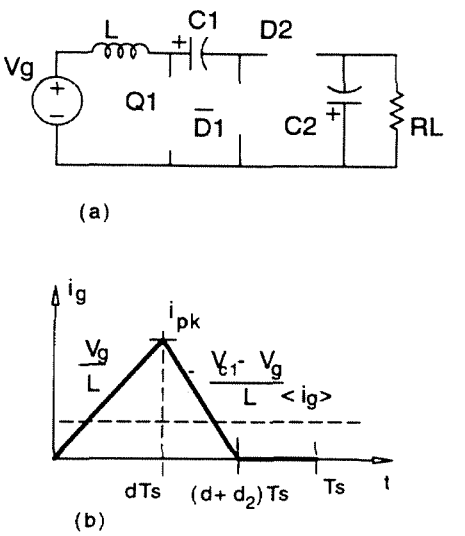


Figure 9.3: The three-switch converter operates in DICM: the third interval i_L=0 (a); the input inductor current waveform(b).

9.2.2 Discontinuous Inductor Current Mode (DICM) and Automatic Current Shaping

If the input inductor current is discharged to zero before the end of the switching cycle, the converter is operating in discontinuous inductor current mode (DICM). The equivalent circuit in this interval is illustrated in Fig. 9.3(a), and the current waveform in Fig.9.3(b). The steady state analysis is the same as that of the boost converter [20].

The conversion ratio at DICM is

$$M = \frac{1 + \sqrt{1 + \frac{4D^2}{K}}}{2}, \tag{9.2}$$

where the conduction parameter K is defined as

$$K = \frac{2L}{RT_s}. \tag{9.3}$$

The converter operates in CICM when

$$K > DD'^2 , \tag{9.4}$$

and in DICM, when

$$K < DD'^2 . \tag{9.5}$$

For off-line applications, the new converter can work as an "automatic" current shaper when operating in DICM.

The input inductor current averaged over one switch period is given by

$$\begin{aligned} \bar{i}_g(\theta) &= \frac{|V_g(\theta)|}{2L} dT_s[d + d_2(\theta)] \\ &= \frac{|V_g(\theta)|}{2L} d^2 T_s[1 + \frac{|V_g(\theta)|}{V_{c1} - |V_g(\theta)|}] \\ &= \frac{|V_g(\theta)|}{R_{em}}[\frac{M}{M - |sin\theta|}], \end{aligned} \tag{9.6}$$

where

$$V_g(\theta) = V_g \sin\theta , \tag{9.7}$$

$$M = \frac{V_{c1}}{V_g} , \tag{9.8}$$

$$\text{and} \quad R_{em} = \frac{2L}{T_s d^2} , \tag{9.9}$$

is emulated resistance of the shaper.

By keeping the duty ratio and switching frequency constant, the power factor is theoretically greater than 0.97 for conversion ratio $M > 1.5$. Notice that this is the same result as obtained in the boost "automatic" current shaper [4].

9.3 Small-Signal Dynamics

The method of state-space averaging [20] or averaged switch model [17, 18] can be used to determine the dynamic responses for the three-switch converter (Fig. 9.2(a)). Both methods are justified by the assumption of the approximately linear capacitor voltage ripple, which requires the time constant of capacitor charging loop to be sufficiently longer than the switching period, i.e., $\tau_c = (C_1 \parallel C_2)(r_{c1} + r_{c2}) \gg DT_s$.

The control-to-output-voltage transfer function is found as

$$\frac{\hat{V}}{\hat{V}_d} = \frac{V}{D'} \frac{(1+\frac{S}{\omega_{z1}})(1-\frac{1}{Q_{zo}}\frac{S}{\omega_{zo}}+\frac{S^2}{\omega_{zo}^2})}{(1+\frac{S}{\omega_{p1}})(1+\frac{1}{Q_{po}}\frac{S}{\omega_{po}}+\frac{S^2}{\omega_{po}^2})}, \tag{9.10}$$

where

$$L_e = \frac{L}{(D')^2}, \tag{9.11}$$

$$\omega_{zo} = \frac{1}{\sqrt{L_e C_1}} \sqrt{\frac{D^2 R}{D'(r_{c1}+r_{c2})}}, \tag{9.12}$$

$$Q_{zo} = \frac{1}{\sqrt{\frac{L_e}{C_1}}} \sqrt{\frac{D'R(r_{c1}+r_{c2})}{D^2}}, \tag{9.13}$$

$$\omega_{z1} = \frac{1}{C_2 r_{c2}}, \tag{9.14}$$

$$\omega_{po} = \frac{1}{\sqrt{L_e(C_1+C_2)}}, \tag{9.15}$$

$$Q_{po} = \frac{R}{\sqrt{\frac{L_e}{(C_1+C_2)}}} \frac{1}{1+\frac{R}{L_e/C_2}(\frac{r_{c1}}{DD'}+\frac{r_{c1}C_1}{D'C_2}+\frac{r_{c2}}{D})}, \tag{9.16}$$

$$\omega_{p1} = \frac{D}{(C_1 \parallel C_2)(r_{c1}+r_{c2})}. \tag{9.17}$$

The double RHP (right half-plane) zero w_{zo} is separated into two real zeros when $Q_{zo} << 1$, the two zeros are

$$\omega_1 = \frac{R}{L_e}, \tag{9.18}$$

$$\omega_2 = \frac{D^2}{D'}\frac{1}{C_1(r_{c1}+r_{c2})}. \tag{9.19}$$

Note that w_1 is exactly the same RHP zero as that of the boost converter, and w_2 is typically at much higher frequency range.

Also, the line-to-output transfer function is given by

$$\frac{\hat{V}}{\hat{V}_g} = \frac{1}{D'}\frac{1+\frac{S}{\omega_{z1}}}{(1+\frac{S}{\omega_{p1}})(1+\frac{1}{Q_{po}}\frac{S}{\omega_{po}}+\frac{S^2}{\omega_{po}^2})}. \tag{9.20}$$

If the time constant of capacitor charging loop τ_c is comparable to the switching cycle, the linear ripple assumption is not satisfied. Therefore, the state space averaging does not apply. However, the expression for the dominant double poles w_{po} remains the same as in Eq. (9.15), since they are caused by the resonance between input inductor and the two capacitors, which are independent of τ_c. The accurate small signal analysis in higher frequency range can be carried out by using the method of state space analysis without the linear ripple approximation. The results need to be computed numerically, since the symbolic expressions for matrices exponential are too involved to be useful.

9.4 Extensions of the Basic Three-Switch Converter

The first extension of the basic three-switch converter is adding capacitor-diode voltage multiplier at its output. A quadrupler version of the HV converter is shown in Fig. 9.4. The output voltage is $\frac{-2V_g}{1-D}$. Generally, for an n-stage multiplier $M = \frac{-nV_g}{1-D}$. (one stage consists of two diodes and two capacitors). By using the voltage multiplier, the voltage stress on each switch or capacitor is reduced. Because fast diodes with enormous reverse voltage ratings are hard to find, reduction of the diode ratings decreases the reverse-recovery current in each diode. However, all the diodes are in series with the output at dc (when capacitors can be considered as open branches since no averaged dc current goes through them), the on-loss caused by the forward voltage drop of the diodes is increasing. Also the capacitance charging loss increases with the number of stages. In addition, output voltage ripple and the dc output resistance increase rapidly with the increasing of n [22]. Therefore, after choosing reasonable voltage ratings for devices, the minimum possible stages should

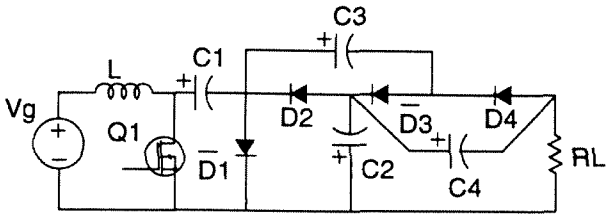


Figure 9.4: A capacitor-diode quadrupler extension of the basic three-switch HV converter.

be used to reduce loss and output voltage ripple.

The full dynamic analysis for the voltage multiplier in Fig. 9.4 will not be discussed in this chapter. However, it is worthwhile to mention the dominant double poles, which can be simply expressed as

$$\omega_{po} = \frac{1}{\sqrt{L_e \sum_{i=1}^{4} C_i}}, \tag{9.21}$$

where, L_e is defined as in Eq. (9.11).

This result can be extended to n-stage voltage multiplier, with the summation of all $2n$ capacitance replacing that of the four capacitance in Eq. (9.21). The physical insight is as follows: at low frequency, all capacitors function as though they are in parallel. The total capacitance is resonant with the equivalent inductance, which gives rise to the dominant double poles.

Similarly, a voltage multiplier can be incorporated in converters SU(2), SU(3) and SU(4) in Fig. 5.6.

Another interesting extension of the three-switch converter is shown in Fig. 9.5, in which both input and output currents are continuous. The input inductor L_1 and the output inductor L_2 are in a loop with V_g, C_1, C_2, and C_4, which appear as short circuits at switching frequency and its harmonics. So L_1, L_2 are effectively in parallel and have identical ac voltage waveforms. Hence, the two inductors can be coupled to reduce size and provide the ripple-steering feature.

This converter can be viewed as an extension of the Ćuk converter by inserting a voltage

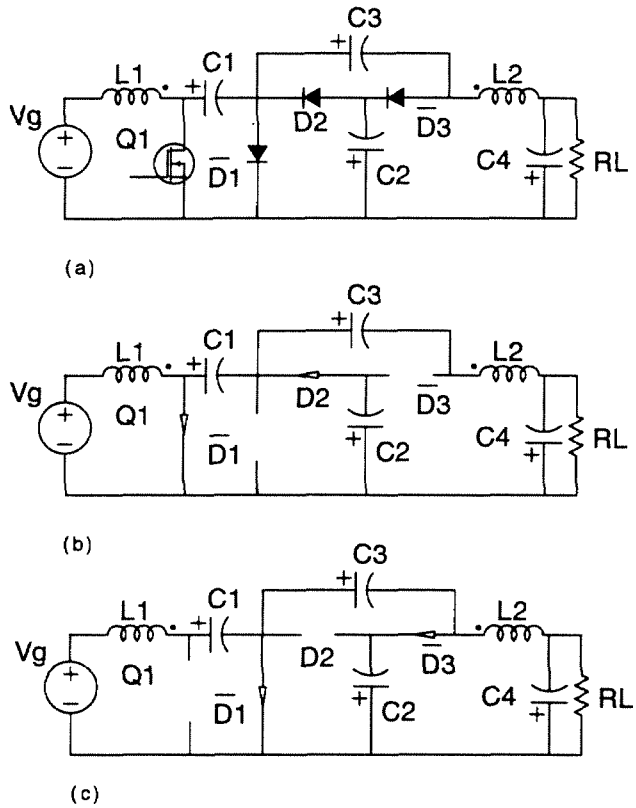


Figure 9.5: An extension of the three-switch HV converter, with continuous input and output currents(a); the equivalent circuit during DT_s (b); and the equivalent circuit during $D'T_s$.

doubler before the output inductor. The conversion ratio for this converter is $\frac{1+D}{1-D}$, which can be easily derived from equivalent circuits of the converter in intervals DT_s and $D'T_s$ (Fig. 9.5(b) and (c)).

In comparison with the basic Ćuk converter, the new converter operates at lower duty ratio for the same overall conversion ratio. The relation between the corresponding duty ratios D_N and D is obtained from

$$\frac{1+D_N}{1-D_N} = M = \frac{D}{1-D}\,, \tag{9.22}$$

which leads to

$$D_N = 2D - 1\,. \tag{9.23}$$

Clearly, D_N is always lower than D. (D is greater than 0.5 when the Ćuk converter works as a step-up converter.)

The voltage stress on the transistor and diodes is

$$V_{off}^N = \frac{V_g}{1-D_N} = \frac{V_g}{2(1-D)}\,, \tag{9.24}$$

which is half of the switch stress in the basic Ćuk converter.

The peak voltage stress on L_1 and L_2 is

$$V_L^N = \frac{D_N}{1-D_N}V_g = \frac{2D-1}{2(1-D)}V_g\,, \tag{9.25}$$

which is less than half of that in the basic Ćuk converter.

Theoretically, a capacitor-diode multiplier with more stages (such as a quadrupler) can be inserted in place of the doubler in Fig. 9.5. However, this will introduce more losses as explained at the beginning of this section.

For many applications, it is essential to provide dc isolation between input and output, and/or multiple outputs of different voltages and polarities. Similar as the Ćuk converter, the three-switch HV converter and its extension have an energy transfer capacitor. By splitting this capacitor into two in series, we can easily insert an ac transformer between the two capacitors. An isolated three-switch HV converter is shown in Fig. 9.6, where the

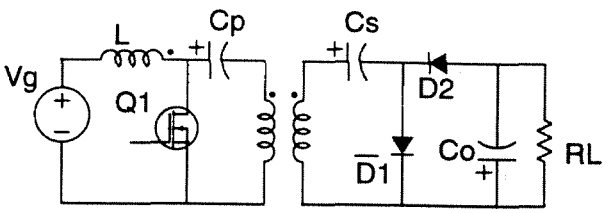


Figure 9.6: The dc isolated three-switch converter, (where the input inductor can be coupled with the transformer).

input inductor and the transformer can be coupled. In the isolated version of the converter in Fig. 9.5, all the magnetics (input and output inductors and transformer) can be coupled.

9.5 Zero-Voltage Switching

For hard-switching converters, in every switching cycle, charge stored in the junction capacitance during the turn-off transition is dumped into the transistor at the beginning of the transistor turn-on. This switch turn-on loss is proportional to switching frequency. The loss becomes significant in high switching frequency and high voltage applications. Moreover, the discharging current introduces high spike and high di/dt in the transistor, which result in high switch stress and EMI noise. In order to achieve zero-voltage switching at constant switching frequency, the diode D_1 in the three-switch converter (Fig. 9.2(a)) is replaced by the controllable MOSFET Q_2. Soft-switching of both transistors is provided by discharging the junction capacitor across the MOSFET before it is turned-on [23]. The simplest way is to design the input inductor such that its current is bi-directional (the peak-to-peak ripple current greater than twice of its average dc current at maximum load). During the transition periods, all the switches are off, the input inductor and the two junction capacitors exchange energy in the lossless, resonant mode to realize zero-voltage switching.

The mechanism for soft-switching is illustrated in Fig. 9.7(a)-(c). The bi-directional input current is shown in Fig. 9.7(a). Two resonant intervals t_{r1} and t_{r2} are introduced by

delaying the turn-on of each switch after the turn-off of the other. The resonant intervals are assumed to be short compared with the switching period. Therefore, the input inductor can be replaced by a current source in Fig. 9.7(b)and(c). Each MOSFET is replaced by a composite switch, consisting of a main switch, an anti-parallel diode, and a junction capacitor. The energy transfer capacitor is replaced by a constant voltage source.

The first resonant interval t_{r1} starts when Q_{s1} is open and D_2 is open simultaneously. The positive peak input current I_p is charging C_{s1} and discharging C_{s2}. When the voltage on C_{s2} is discharged to zero, D_{s2} conducts and clamps the voltage at zero. Hence, Q_{s2} can be turned-on at zero-voltage.

The second resonant interval t_{r2} starts when Q_{s2} is turned-off. The input current $(-I_n)$ is negative now, C_{s1} is discharged towards zero, and C_{s2} is charged towards V_{c1}. Since I_n is smaller than I_p, t_{r2} is always longer than t_{r1}. There is another difference from the first transition: D_{s1} will never conduct. This can be explained by looking at the loop consisting of C_1, C_2, D_{s1}, and D_2. At the beginning of DT_s, V_{c1} is always bigger than V_{c2}. When $V_{c1} - V_{c2} - V_{cs1} > V_{d2}$ (turn-on voltage of D_2), D_2 would turn on first. The capacitor charging current is usually bigger than the negative inductor current, the difference of these two currents will charge C_{s1} , and V_{cs1} will never reach zero. Therefore, we should turn-on Q_{s1} before D_2. Fortunately, the difference between V_{c1} and V_{c2} is usually very small. Thus, Q_{s1} is turned-on very close to zero-voltage.

The resonant transitions also provide zero-voltage turn-off for D_2 and reduce the loss caused by the reverse recovery current in D_2.

9.6 Experimental Results

First, a prototype of the basic three-switch converter was built to verify analytic results. Components used in this prototype are: $Q_1 = IRF540$, $D_1 = D_2 = ERC88 - 009$, $L = 480uH$, $C_1 = C_2 = 43uF$, $r_{c1} = r_{c2} = 0.55\Omega$.

The measured and the predicted dc voltage conversion ratios are shown in Fig. 9.8 and Fig. 9.9 ($f_s = 50kHz$). In Fig. 9.8, $R_L = 50\Omega$, the converter is always in CICM. The deviation at the high end of the duty cycle is due to the parasitics (lossy elements) inside the converter. When R_L equals 630Ω, the converter goes into DICM when the duty ratio is less than 0.65, which is consistent with the result from Eq. (9.5): in DICM when

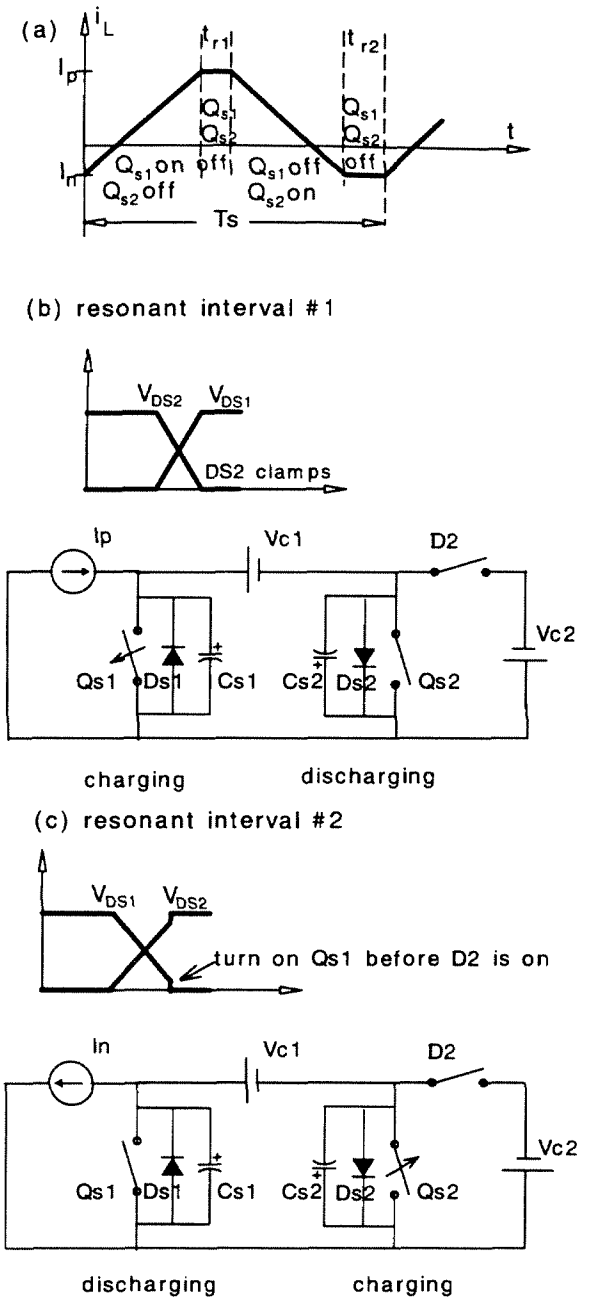


Figure 9.7: Soft-switching mechanism: bi-directional inductor current (a); the first resonant interval (b) and the second resonant interval (c).

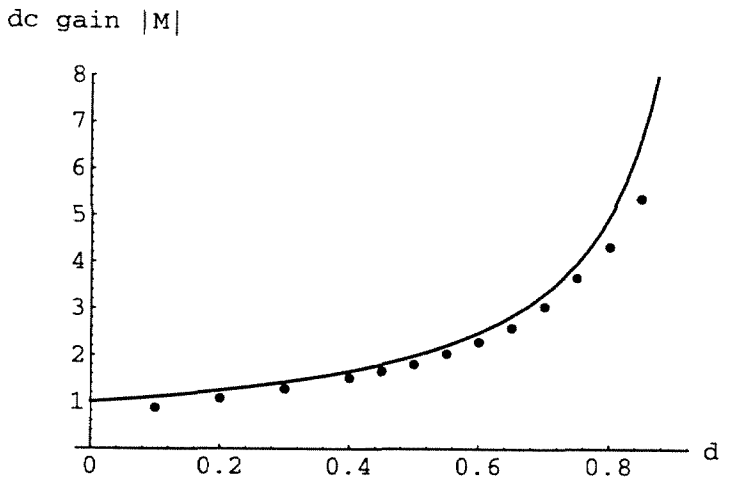


Figure 9.8: Theoretical (line) and experimental (dot) dc gain characteristics of the three-switch HV converter in CICM.

$0.094 < D < 0.655$. Since the load current is very small in this case, the parasitic elements have negligible effect as shown in Fig. 9.9.

Fig. 9.10 gives the measured control-to-output transfer functions, together with the predictions from Eq. (9.10), where $f_s = 100kHz$. Good agreements can be observed up to half switching frequency.

The voltage conversion ratios of the two extensions of the basic three-switch converter (Fig. 9.4 and Fig. 9.5) were measured. Results are displayed in Fig. 9.11 and Fig. 9.12.

Finally, experiments were done to demonstrate the soft-switching mechanism. Waveforms with and without soft-switching are shown in Fig. 9.13(a)-(d) for comparison. In the experimental circuit, the drain-to-source voltage of each MOSFET is sensed to control the corresponding gate signal. Each MOSFET is turned on when its V_{ds} is close to zero. In Fig. 9.13(a), it can be seen that there is a large current in D_{s2} when Q_{s2} is turned on. Therefore, Q_{s2} is turned on without switching losses. In Fig. 9.13(c), negative input inductor current discharges V_{ds1} to negligible small value, and the control (gate) signal turns Q_{s1} on before D_2 starts to conduct. After Q_{s1} conducts, D_2 is turned-on. The current through Q_{s1} is the summation of the input inductor current and the output capacitive charging current. The high current spike and oscillation in hard-switching converter are eliminated by soft-switching technique.

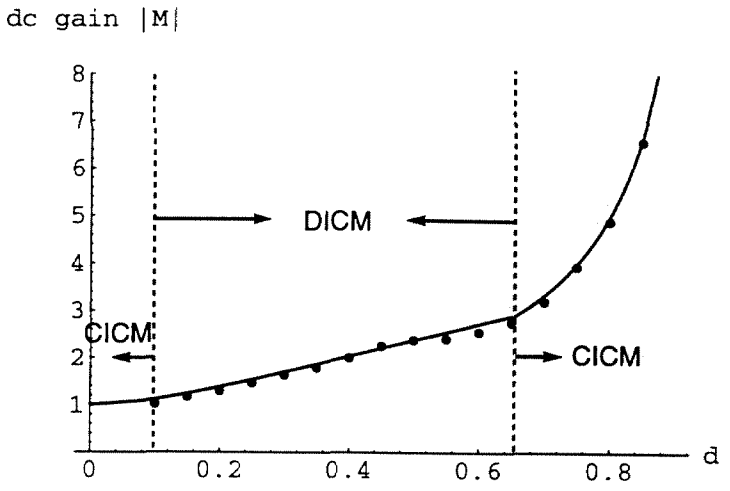


Figure 9.9: Verification of the conduction mode type and dc gain in the three-switch converter: in DICM when duty cycle is less than 0.65. Theoretical (line) and experimental (dot).

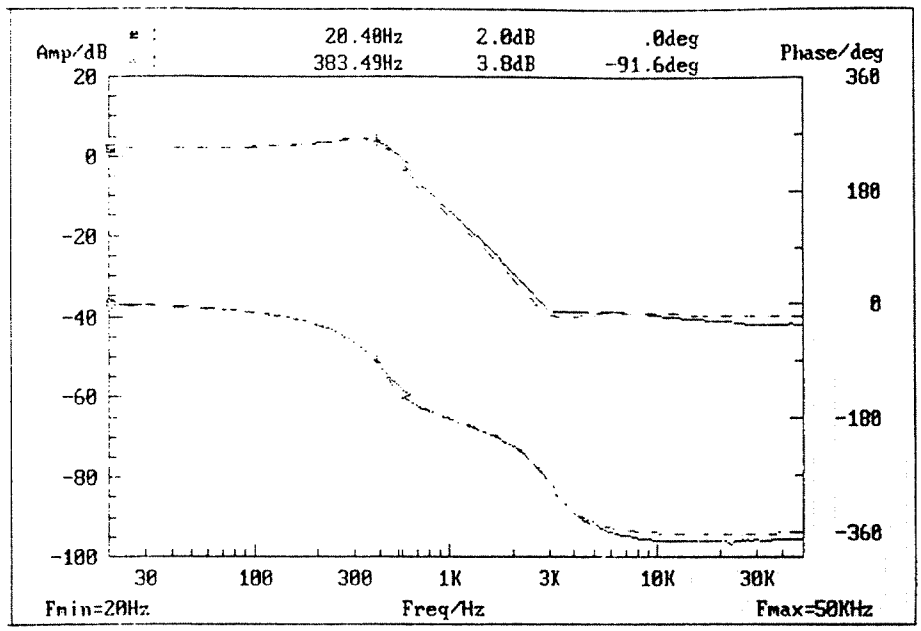
9.7 Conclusion

A novel three-switch HV converter is discussed in this chapter. It has the boost-like front-end. Automatic current shaping is obtained by operating the converter in DICM. Dc and dynamic analyses reveal that it has many similarities to the boost converter. However, exchanging of the positions of the diode and the capacitor in the boost converter provides significant benefits due to the floating capacitor. First, it can be used to drive capacitor-diode multiplier, which is the common solution for ultra high voltage application. Second, the isolation of input and output can be easily achieved as in a Ćuk converter by splitting the energy transfer capacitor into two and inserting an ac transformer in between.

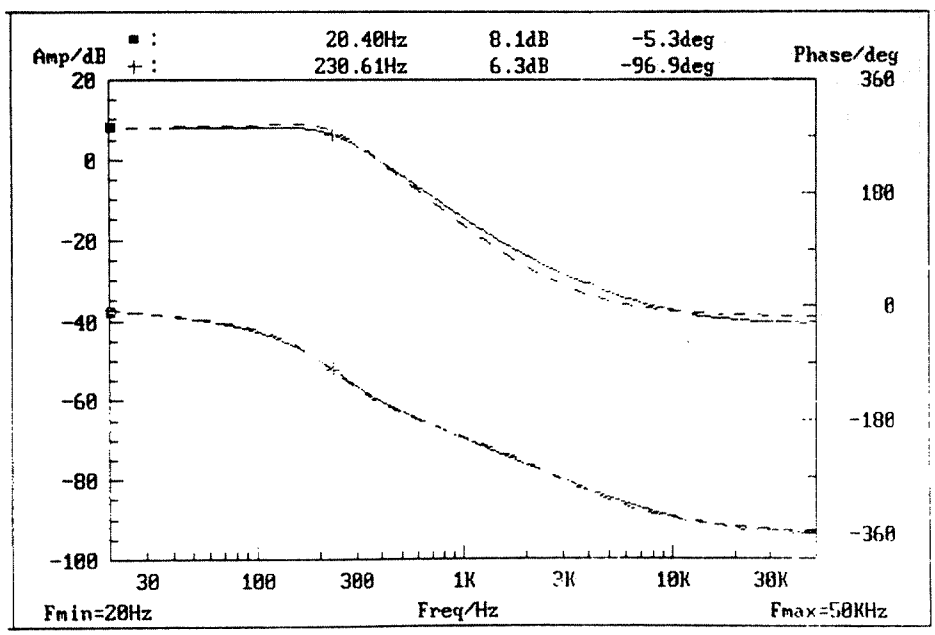
Another interesting extension, which features both continuous input and output current, is also introduced. The inductors in this converter can be coupled.

Experimental results agree well with the predictions.

Similarly, a capacitor-diode voltage-multiplier can be incorporated in converter SU(2), SU(3), or SU(4) (Fig. 5.6) to obtain large step-up conversion ratio.



(a)



(b)

Figure 9.10: Measured (solid lines) and predicted (dashed lines) control-to-output-voltage transfer function: D equals 0.5 in (a);and D equals 0.7 in (b).

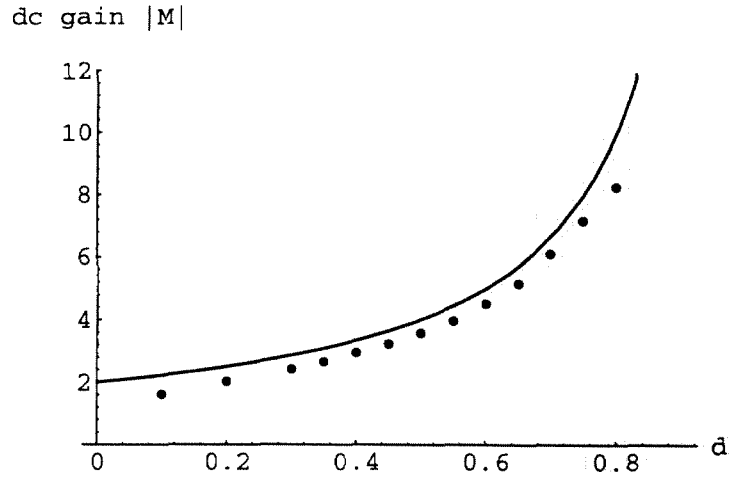


Figure 9.11: Theoretical (line) and experimental (dot) dc gain characteristics of the quadrupler extension.

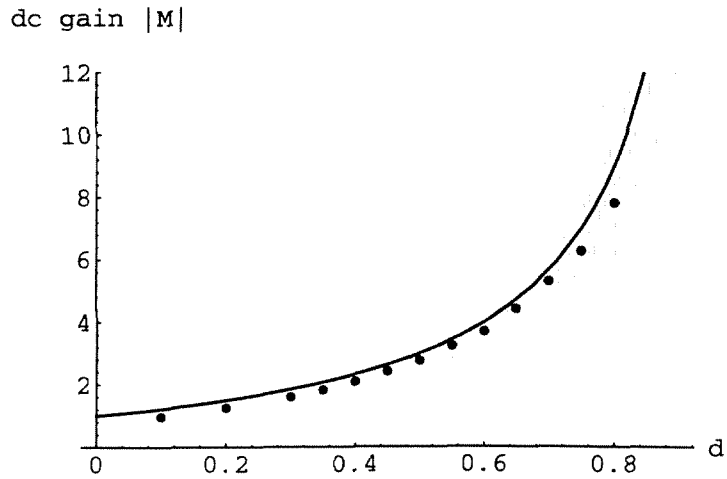


Figure 9.12: Theoretical (line) and experimental (dot) dc gain characteristics of the continuous input and output currents extension.

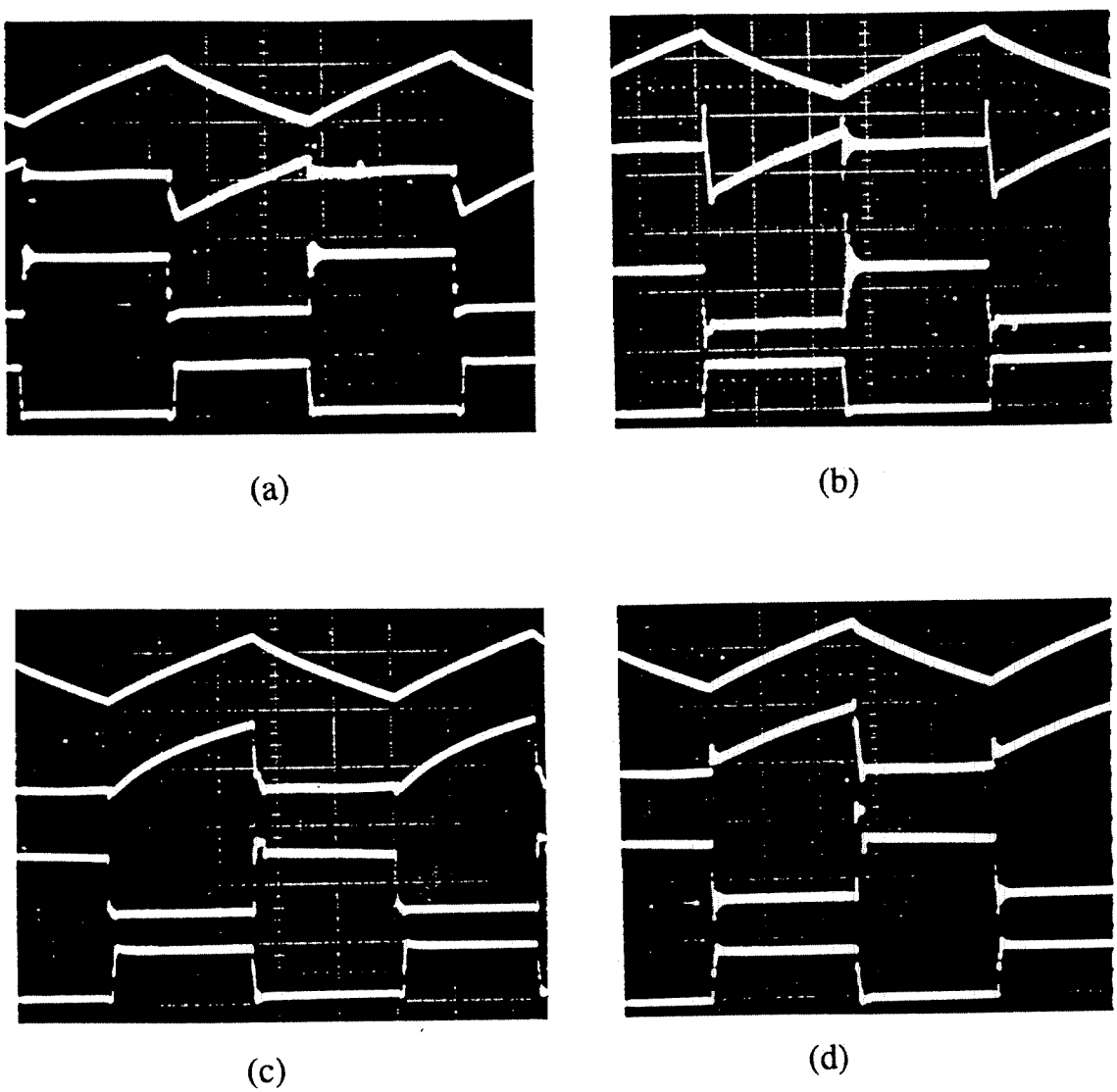


Figure 9.13: Comparison of the three-switch converter with or without soft-switching. In each oscillogram photo: upper trace: input inductor current (5A/div); upper middle trace: drain-to-source current (5A/div); lower middle trace: drain-to-source voltage (20v/div); lower trace: gate voltage (10v/div); time scale: 2uS/div. (a) Waveforms in Q_2 with soft-switching. (b) Waveforms in Q_2 without soft-switching. (c) Waveforms in Q_1 with soft-switching. (d) Waveforms in Q_1 without soft-switching.

Chapter 10 Cross-Regulation Improvement at Light Loads by Use of the Coupled Inductors

Some multiple-output converters (forward, push-pull, etc.) exhibit serious cross-regulation problems when one or more outputs operates at light load, that is in discontinuous inductor current mode (DICM). By coupling the inductors, the cross-regulation in DICM is significantly improved. This chapter establishes the quantitative relationship between coupling coefficient and the degree of the cross-regulation improvement in general and for special case of zero ripple current. The effect of the coupling coefficient on the small-signal responses is examined. This study provides the guidelines for the design of the coupled inductors to achieve optimum steady-state and dynamic performance. Finally theoretical predictions are verified by computer simulations and experimental results.

10.1 Introduction

Power supplies for computers and other electronic devices are often required to have more than one isolated DC output voltages. In these applications, multiple-output switching converters are usually employed for cost effectiveness and space efficiency. The most commonly used control scheme is to fully regulate one output by use of the feedback, while cross-regulating the other outputs. Without post-regulator, the cross-regulated outputs may severely deviate from the desired values. Cross-regulation errors depend on converter topology, load conditions and circuit parasitics.

For some types of multiple-output converters (forward, half-bridge, push-pull, etc.), when only lightly loaded or fully unloaded, the unsensed outputs can soar to as much as two or three times their nominal values because of the change of operating mode from continuous inductor current mode (CICM) to discontinuous inductor current mode (DICM). The brute-force solution to this problem is to pre-load the outputs with some dummy load, which is clearly wasteful of power and space. A much more elegant way is to couple the output filter inductors in these converters. This method leads to dramatic improvements on

both dc and ac cross-regulation. It can also steer the ac ripple current from one output to another. Hence, a single coupled-inductor magnetics structure can be designed to eliminate the ripple current from all but one of the output inductors. In this case, only one output has to satisfy the minimum load current requirement in order to avoid going into DICM. From another point of view, the output which is loaded, is through the coupling, making the fully unloaded outputs look like they are effectively loaded.

Although coupled inductors have been used in multiple-output converters [9, 26], a full quantitative analysis has not been carried out to establish the design criteria. The purpose of this study is to develop an analytical model, and based on that provide the quantitative relationship between the coupling coefficient and the degree of the cross-regulation improvement. This, together with the small-signal analysis, can provide tools for optimum design.

In Section 10.2, different sources of cross-regulation errors are reviewed and classified. Section 10.3 discusses the improvements on the cross-regulation by use of the coupled-inductor technique. Small-signal model and dynamic analysis for current-programmed multiple-output converters are developed in Section 10.4. The dc characteristic of multiple-output forward converters is given in Section 10.5. Design procedure of the coupled-inductor and experimental results are given in Section 10.6. Key issues are summarized in Section 10.7.

10.2 Different Types of Cross-Regulation errors

In multiple-output converters, a number of sources contribute to the cross-regulation errors [27]-[32]. They can be divided into three groups:

The well-known error sources are the circuit parasitics, which include the winding resistors of the transformer secondaries and of the output filter inductors, the leakage inductors of the transformer secondaries, the forward voltage drop and "on" resistors of the diodes. Note that, only the parasitics at the separate outputs will affect the cross-regulation. Since the effects of the parasitic resistors and forward voltage drops are straightforward, we only need to explain the effects of *leakage inductors* of the transformer. In the following discussion, we assume all the circuit elements are ideal, except the transformer leakage inductors.

As shown in Fig. 10.1, leakage inductors (L_{tp}, L_{t1}, L_{t2}) have the effect of delaying the

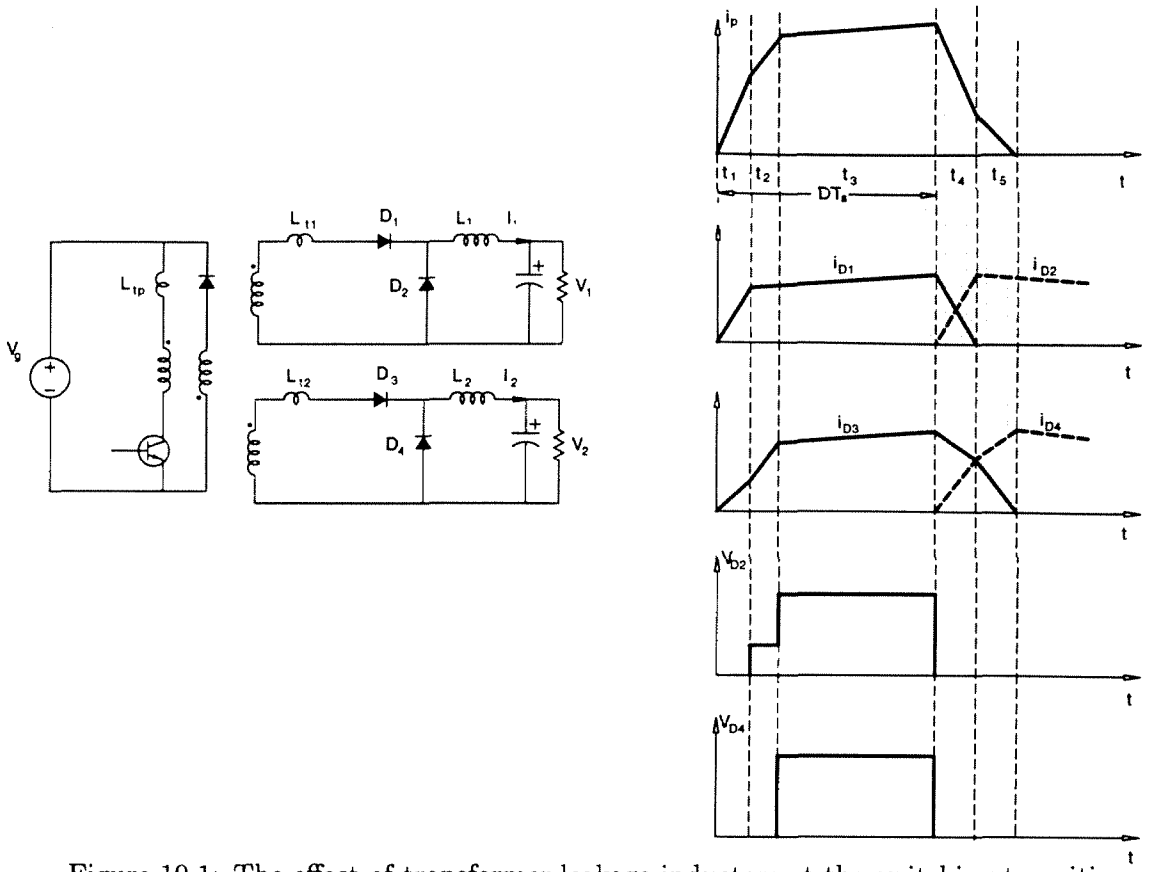


Figure 10.1: The effect of transformer leakage inductors at the switching transitions.

transfer of current between forward and free-wheeling diodes at the switch "turn-on" and "turn-off" instants.

During *turn-on* (t_1 and t_2): This results in the delayed rising of voltages across free-wheeling diodes. Since the output voltages are the average of $v_{D_2}(t)$ and $v_{D_4}(t)$ in each switching cycle, the *turn-on delay* reduces the effective D, and consequently the output voltage. During *turn-off* (t_4 and t_5): leakage inductors delay the transfer of current back to the free-wheeling diodes. However, since D_2 and D_4 are on during this transition, $v_{D_2}(t)$ and $v_{D_4}(t)$ are clamped to zero. Therefore, the *turn-off delay* has no effect on the output voltages.

A quantitative study gives the equivalent circuit shown in Fig. 10.2, where the effects of the transformer leakage inductors are revealed. It is interesting to notice that the ratios of the leakage inductors to switching cycle T_s appear as equivalent series resistors in the circuit. Therefore, the effect of the leakage inductors exaggerates with the increasing of the switching frequency and/or the load currents. As expected, L_{tp} has the same effect on both

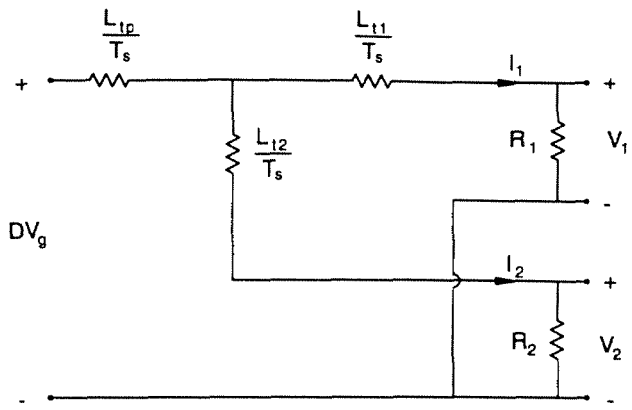


Figure 10.2: The effects of the leakage inductors are illustrated by a equivalent circuit.

outputs. Thus, the cross-regulation error is caused only by L_{t1} and L_{t2}.

$$V_1 - V_2 = \frac{I_2 L_{t2} - I_1 L_{t1}}{T_s} . \tag{10.1}$$

Obviously, this type of cross-regulation error can be greatly reduced by winding the transformer secondaries tightly together to reduce secondary leakage inductors, and by reducing the wire inductors between the transformer secondaries and the junctions of the diodes, which have the same effect as the transformer leakage inductors.

Another error source is the unequal capacitor discharge time, which happens in the converters involving capacitive energy transfer (such as Ćuk and flyback converter). This phenomenon has been discussed in the past [35]. The brief explanation is as follows: Generally speaking, the energy transfer capacitors for different outputs are discharged to different values at the end of the period DT_s, when the transistor turns off, the diodes connected with the capacitors cannot turn on at the same time. The averaged difference between the capacitor voltage waveforms in per switching cycle gives rise to the deviation of the output voltages. It should be pointed out that this difference is always less than half the capacitor ripple voltage, and can be reduced by choosing large capacitors.

The errors we discussed above are classified as the second-order errors. The worse scenario happens when the operating mode of one or more outputs changes from CICM to

DICM during light loads (typically less that 20 % of the full loads). In this chapter, we call this the first-order cross-regulation error.

In DICM, the output voltages depend on both duty ratio and load currents. For the same duty ratio, reducing the load current increases its output voltage. For multiple-output converters, the cross-regulation characteristics in DICM vary widely over different converter configurations (Fig. 10.3). For those in which all outputs share the same inductor (such as flyback), all the outputs go into DICM together, and their voltages increase by the same ratio, which can be easily corrected by the feedback control of the main output, and good cross-regulation is maintained. Others (like Ćuk converter) have the energy transfer capacitors, by choosing sufficient large capacitors, they can keep the voltage waveforms on the diodes of individual outputs essentially identical. Therefore, the output voltages which are the average of the diode voltage waveforms throughout the whole switching cycle are closely tracking to each other even in DCIM. However, in buck-derived converters, forward diodes separate the individual outputs, each output has its operating mode which is determined by its own load condition. One or more outputs can operate in DICM, while the others stay in CICM, i.e., there is no tracking at all between these output voltages. If any of the unsensed outputs is in DICM, the increased voltage cannot be detected and corrected by the feedback control; on the other hand, if DICM happens in the main output, closed-loop control of this output will decrease the voltages in those slaved outputs which are operating in CICM from their desired values. To overcome this problem, coupled-inductor technique is frequently used in multiple-output buck type converters. This technique can greatly reduce the first-order cross-regulation error; while it basically has no effect on the second-order errors.

10.3 Improvement on the Cross-Regulation by Use of the Coupled-Inductor Technique

Without loss of generality, the following analysis is performed on a two-output coupled-inductor forward converter. To simplify the notations, the isolation transformer is assumed to have unity turns ratios, so the two outputs have identical voltages when both operate in CICM. In the case of different output voltages, the outputs can be scaled by the transformer turns ratio, which leads to the same model we are going to discuss here. The π-model

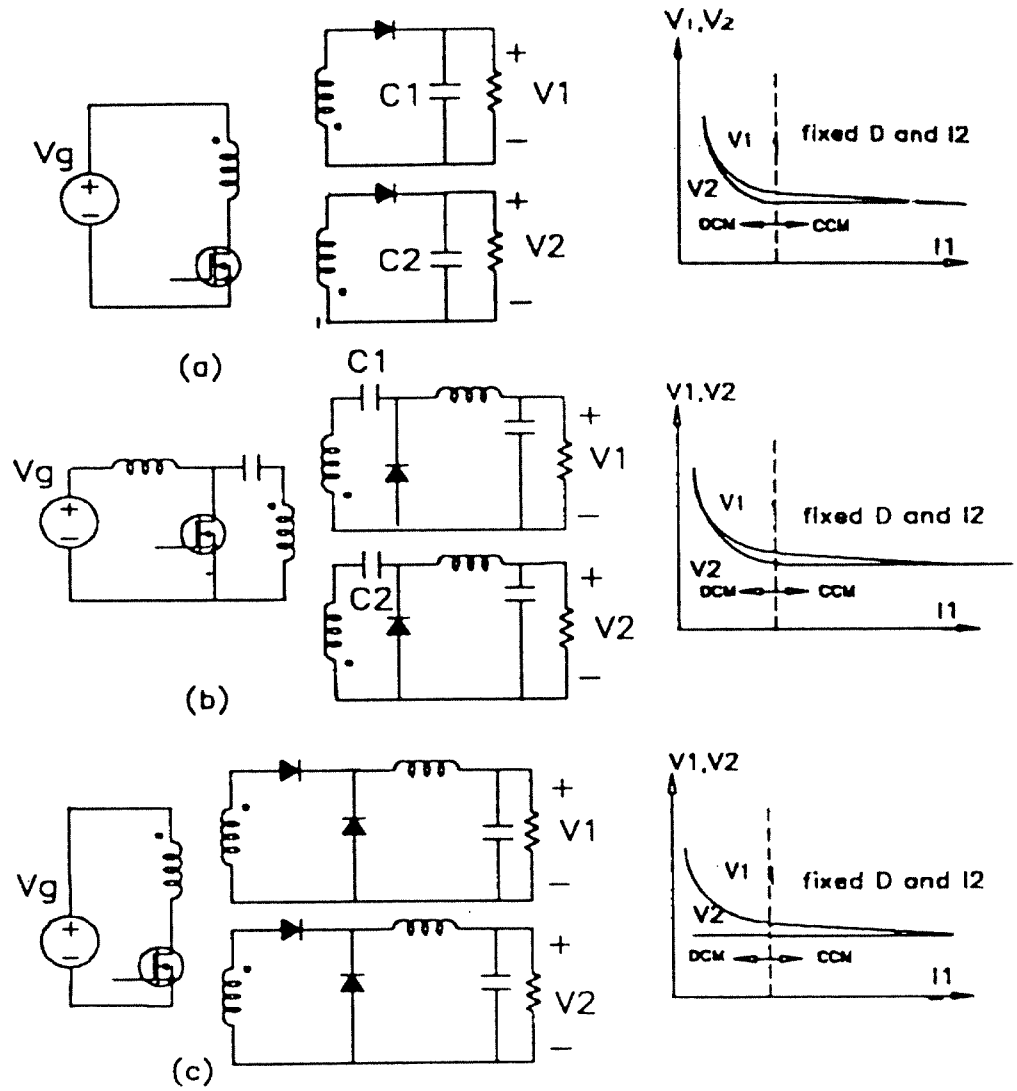


Figure 10.3: Cross-regulation characteristics for different converters: (a) flyback converter, (b) Cuk converter, and (c) forward converter.

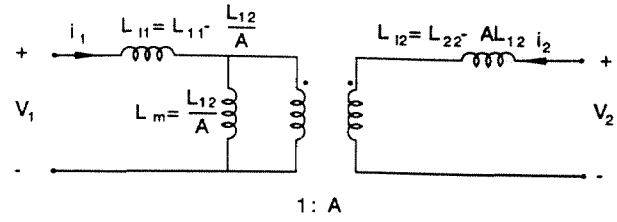


Figure 10.4: The π-model for a two-winding coupled inductors.

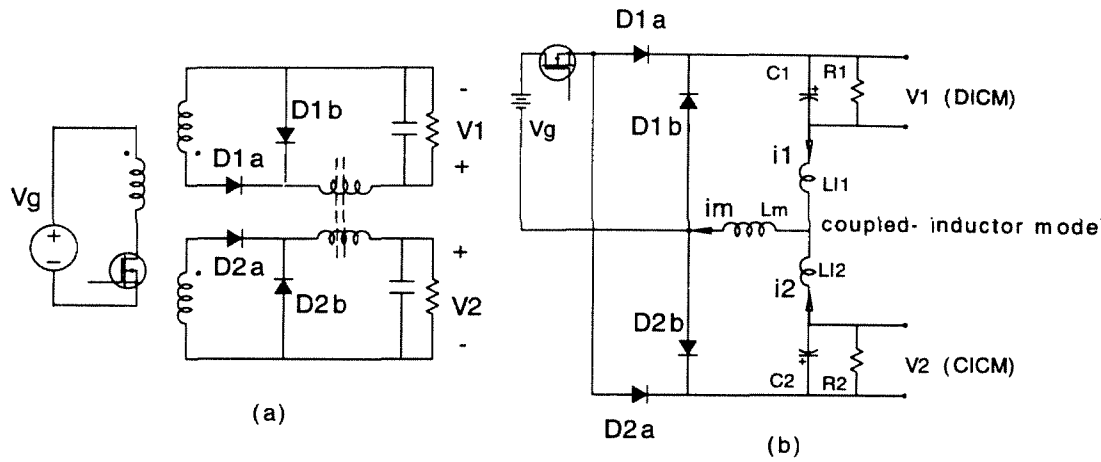


Figure 10.5: (a) A two-output coupled-inductor forward converter, and (b) The equivalent circuit of this converter.

for the two-winding coupled-inductor is shown in Fig. 10.4. There are four parameters L_{l1}, L_{l2}, L_m, and A in the model, but only three constants L_{11}, L_{22}, and L_{12}. Therefore the model is *underdetermined* and the effective turns ratio A can be chosen arbitrarily [35]. In order to simplify the circuit, A is chosen to be equal to one. The two-output forward converter and its equivalent circuit are shown in Fig. 10.5.

If tightly coupled inductors are used, the two outputs actually share the same inductor (mutual inductor L_m), therefore, the cross-regulation is good in both CICM and DICM. However, if there is a slight mismatch between the voltages across the two inductor windings (which may be caused by the different diode voltage drops, a small error in the transformer turns ratio, or other nonidealities in the converter circuit), large ripple currents appear in both outputs. Since there is no leakage inductance, the ripple currents are only limited by the ESR of the output capacitors. Because of the trade-off between cross-regulation and the sensitivity of the ripple currents, for the optimum design of the coupled inductors, we need to find out the relationship between the leakage inductors and the output voltages

at DCIM. First, the boundary condition between CICM and DICM is found in the next section.

10.3.1 The Boundary Condition between CICM and DICM

In the first case, suppose that a separate inductor is used in each output. In order to have the first output operating in CICM, the following condition must be satisfied:

$$I_{1pp} \leq 2I_{1min}\,, \tag{10.2}$$

where I_{1pp} is the peak-to-peak ripple current of i_1, and I_{1min} is the minimum load current. I_{1pp} is given by

$$I_{1pp} = \frac{V_1 D' T_s}{L_1}\,. \tag{10.3}$$

From Eqs. (10.2) and (10.3), we have $L_1 \geq \frac{V_1 D' T_s}{2I_{1min}}$. The boundary inductor is denoted by L_{1crit}, and

$$L_{1crit} = \frac{V_1 D' T_s}{2I_{1min}}\,. \tag{10.4}$$

It is often convenient to define a dimensionless parameter to combine all the parameters responsible for determining the operating mode.

$$K_1 \triangleq \frac{2f_s L_1}{R_1}\,. \tag{10.5}$$

From Eqs. (10.4) and (10.5), the corresponding K_{1crit} is equal to $1 - D$. When K_1 is less than K_{1crit}, the first output operates in DICM. Same results can be derived for the second output.

Next, if the two inductors are coupled, from Fig. 10.5(b), we have

$$(L_m + L_{l1})I_{1pp} + L_m I_{2pp} = V_1 D' T_s\,, \tag{10.6}$$

$$L_m I_{1pp} + (L_m + L_{l2})I_{2pp} = V_2 D' T_s\,. \tag{10.7}$$

Two parameters are defined to simplify Eqs. (10.6) and (10.7):

$$k_1' \triangleq \frac{L_m}{L_{l1} + L_m}\,, \tag{10.8}$$

$$k_2' \triangleq \frac{L_m}{L_{l2}+L_m}. \tag{10.9}$$

Note that, the prime sign "'" is used to distinguish k_1' and k_2' from the coupling coefficient k_1 and k_2. For example, k_1 is defined as the ratio of mutual flux to total flux when only the first winding is driven[9]

$$k_1 \triangleq \frac{\phi_{21}}{\phi_{11}} = \frac{N_1}{N_2}\frac{L_{12}}{L_{11}}. \tag{10.10}$$

From the π-model, with $A=1$, we have $L_m = L_{12}$, and $L_{l1} = L_{11} - L_{12}$. Therefore, k_1' equals $\frac{N_1}{N_2}k_1$. Similarly, it can be shown that k_2' equals $\frac{N_2}{N_1}k_2$.

WIth k_1' and k_2', and the fact that V_1=V_2 in CICM, I_{1pp} and I_{2pp} can be derived from Eqs. (10.6) and (10.7):

$$I_{1pp} = \frac{(1-k_2')V_1 D'T_s}{(\frac{1}{k_1'}-k_2')L_m}, \tag{10.11}$$

$$I_{2pp} = \frac{(1-k_1')V_2 D'T_s}{(\frac{1}{k_2'}-k_1')L_m}. \tag{10.12}$$

There are two cases:

1. If $I_{1min} < \frac{(1-k_2')k_1'}{(1-k_1')k_2'} I_{2min}$, the first output goes into DICM first. Define $K_m \triangleq \frac{2f_s L_m}{R_1}$, we have

$$K_{mcrit} = \frac{k_1' - k_1'k_2'}{1-k_1'k_2'}D'. \tag{10.13}$$

2. If $I_{1min} > \frac{(1-k_2')k_1'}{(1-k_1')k_2'} I_{2min}$, the second output goes into DICM first. Define $K_m \triangleq \frac{2f_s L_m}{R_2}$, we have

$$K_{mcrit} = \frac{k_2' - k_1'k_2'}{1-k_1'k_2'}D'. \tag{10.14}$$

If the inductors are 100% tightly coupled, i.e. $k_1' = k_2' = 1$, Eq. (10.13) or Eq. (10.14) is undetermined. However, the boundary L_m can be found directly from Eq. (10.6) or Eq. (10.7), and condition in (10.2),

$$L_{mcrit} = \frac{V_1 D'T_s}{2(I_1+I_2)_{min}}. \tag{10.15}$$

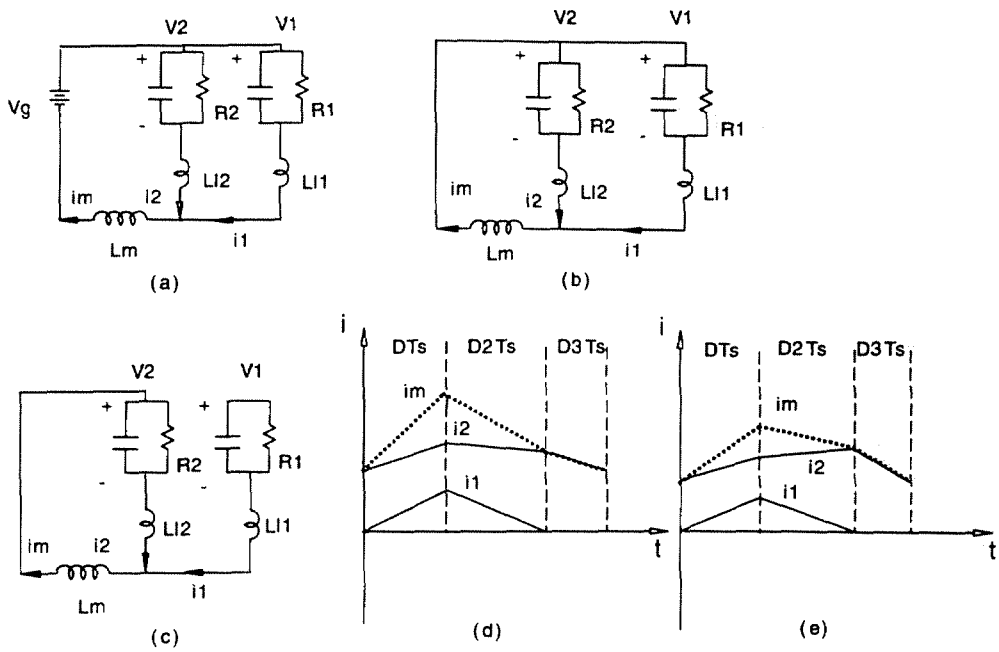


Figure 10.6: Circuit models for coupled-inductor forward converter with the first output in DICM during three time periods: (a) DT_s; (b) D_2T_s; and (c) D_3T_s. Typical inductor current waveforms: (d) when $V_1 < \frac{(L_{l1}+L_m)V_2}{L_m}$; and (e) when $V_1 > \frac{(L_{l1}+L_m)V_2}{L_m}$.

If define $K_m \triangleq \frac{2f_sL_m}{R_1 \| R_2}$, we have

$$K_{mcrit} = D' , \tag{10.16}$$

which is the same as in separate inductor case, only K_m is defined in terms of the parallel of two load resistors instead of a single load resistor.

10.3.2 Dc Characteristic of the Two-Output Coupled-Inductor Forward Converter

Assuming that the load current of the first output in Fig. 10.5 is small so that i_1 reaches zero before the end of the switching cycle. The first output operates in DICM, while the second output remains in CICM. The diode D_{1b} will turn off when i_1 falls to zero, and there will be three states in one switching cycle, as shown in Fig. 10.6(a)-(c). The Kirchhoff's voltage law and the integration of the inductor currents during $(D+D_2)T_s$ time period lead to

$$(L_m + L_{l1}) \int_0^{(D+D_2)T_s} di_1 + L_m \int_0^{(D+D_2)T_s} di_2 = (V_g - V_1)DT_s - V_1 D_2 T_s \,, \quad (10.17)$$

$$L_m \int_0^{(D+D_2)T_s} di_1 + (L_m + L_{i2}) \int_0^{(D+D_2)T_s} di_2 = (V_g - V_2)DT_s - V_2 D_2 T_s \,. \quad (10.18)$$

Also we have

$$\int_0^{(D+D_2)T_s} di_1 = 0 \,, \quad (10.19)$$

$$I = \frac{i_{1max}}{2} = \frac{[(L_m + L_{l2})(V_g - V_1) - L_m(V_g - V_2)]D}{2L_{eq}^2 f_s} \,, \quad (10.20)$$

$$\text{and} \quad I = \frac{V_1}{R_1(D + D_2)} \,; \quad (10.21)$$

$$\text{where} \quad L_{eq}^2 = L_{l1}L_m + L_{l2}L_m + L_{l1}L_{l2} \,. \quad (10.22)$$

Solving these equations gives the two output voltages:

$$V_1 = V_g \frac{2(m + D)}{1 + m - \frac{\alpha K_1}{D} + \sqrt{(m + 1 - \frac{\alpha K_1}{D})^2 + \frac{4\alpha K_1}{D^2}(m + 1)(m + D)}} \,, \quad (10.23)$$

$$V_2 = DV_g \,, \quad (10.24)$$

where m, α, and k_1 are defined as:

$$m \triangleq \frac{L_{l2}}{L_m} \,, \quad (10.25)$$

$$\alpha \triangleq \frac{L_{l1} + L_{l2} \parallel L_m}{L_{l2} \parallel L_m} \,, \quad (10.26)$$

$$K_1 \triangleq \frac{2f_s L_m}{R_1} \,. \quad (10.27)$$

The two dimentionless parameters m and α reflect the effect of the leakage inductors on dc voltage gain.

There are several comments from the above results:

First, the value of the first output depends on only its own load, but not the load of the other output.

Second, when the leakage inductors go to zero, m is close to zero, and α close to one,

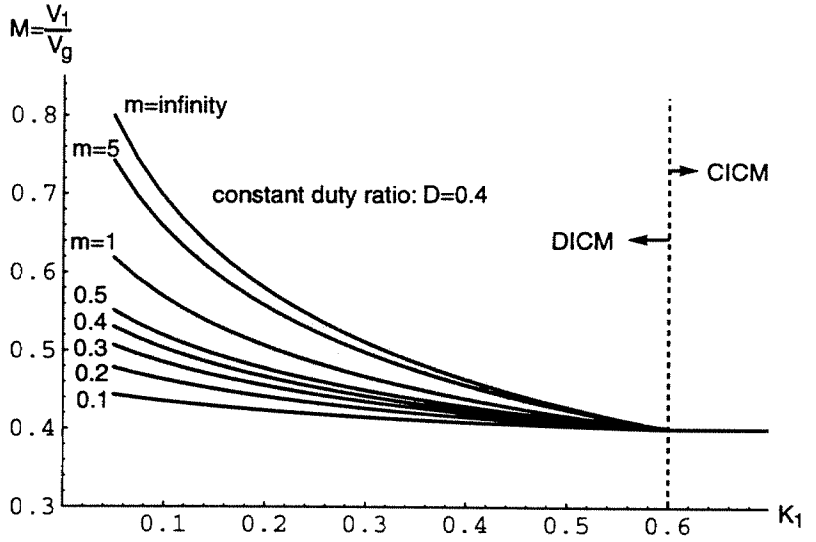


Figure 10.7: Conversion ration of the first output vs. its conduction parameter K_1 when the second output has zero ripple current (m is the running parameter).

from Eq.(10.23), V_1 tends to DV_g, which is the predicted result for tightly coupled case.

A special and very useful case is to properly design the coupled-inductor, so that the effective leakage inductance in one output equals zero in CICM, and all the ripple current is steered into this output, while the other output has zero ripple current. Assume the second output is the zero ripple output, effective leakage inductor in the first output equals zero, then $\alpha = 1$, and Eq.(10.23) becomes

$$V_1 = V_g \frac{2(m+D)}{1+m-\frac{K_1}{D}+\sqrt{(m+1-\frac{K_1}{D})^2+\frac{4K_1}{D^2}(m+1)(m+D)}}. \tag{10.28}$$

In this case, as long as the current i_1 does not drop to zero before the end of the switching cycle, reducing the current of the second output will not make the output go into DICM. However, if the first output operates in DICM, the second output no longer has zero current ripple since there is non-zero voltage across L_{l2}.

The relation between the conversion ration M of the first output and its load under zero-ripple condition is shown in Fig. 10.7 for different m (Duty ratio equals 0.4 in this plot). The deviation of the V_1 from its desired value is less than 35% when m is less than 0.3; while for separate inductors, V_1 is more than doubled.

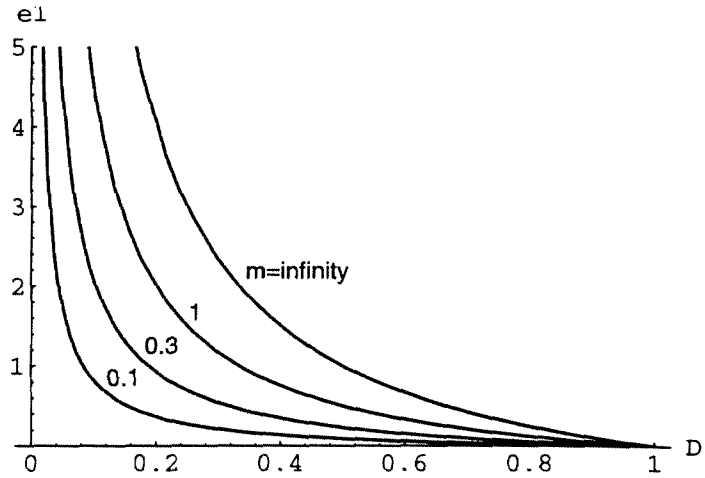


Figure 10.8: The relation between the first-order cross-regulation error and duty ratio D with different m.

The first output has the maximum voltage when it has no load ($K_1 = 0$). From Eq.(10.23), this ceiling value is found to be

$$V_{1max} = \frac{m+D}{m+1} V_g \,. \tag{10.29}$$

Define cross-regulation error for the first output as:

$$e_1 = \frac{|V_{1max} - V_{1min}|}{V_{1nom}} \,. \tag{10.30}$$

If we neglect the second-order error, by Eqs.(10.29) and (10.30),

$$e_1 = \frac{m}{m+1} \frac{1-D}{D} \,. \tag{10.31}$$

It's obvious in Eq.(10.31) that e_1 is bigger at lower duty ratio for the same m, which means that smaller leakage inductance is allowed at lower D to satisfy the same error specification. This result agrees with the fact that a forward converter goes into DICM more frequently at lower duty ratio. The relation between e_1 and duty ratio D is shown in Fig. 10.8 with m as the running parameter.

We have shown how the dc cross-regulation can be improved by coupling inductors.

Now we are going to discuss what happens to the ac cross-regulation. If individual filter inductor is used in each output, the sudden load change and other disturbance on any slaved output need propagate through the high ac impedance of the filter inductors in order to reach the sensed output. Therefore the control loop responds slowly to the load changes at the slaved outputs. When the current-programming control is applied to a single output converter, it introduces a substantial lossless damping resistance in series with the output choke [24], which normally eliminates resonant behavior in the inductor current and output voltage waveforms at sudden load changes. However, for the multiple-output case, with the transformer secondaries usually tightly coupled, all the outputs are driven in parallel at the input of their separate filter inductors. Thus, the damping resistance given by the current-programming control is not directly in series with the individual inductors, the damping effect is reduced. Consequently, resonant waveforms appear in the inductor currents and capacitor voltages, and it takes a long time for them to reach the nominal values. After coupling the inductors, mutual inductor (L_m) appears in the common branch in series with the lossless damping resistance and only small leakage inductors stay in the individual outputs. Thus the resonant effect is normally well-damped.

PSPICE program is used to demonstrate dynamic cross-regulation with and without inductor coupling. A two-output forward converter with zero-ripple in the second output is simulated based upon the model in [25]. The initial inductor currents are set at $14A$ for the first output, and $6A$ for the second. While at the beginning of the simulation, the loads suddenly change from $14A$ and $6A$ to both $10A$, since the inductor currents cannot change instantaneously, the $4A$ change must travel through the 0.02Ω ESR of the filter capacitors. Figure 10.9(a) and (c) show the inductor current and output voltage waveforms with separate inductors, the resonant characteristic degrades the transient responses. However, the transient performance can be dramatically improved by coupling the inductors of the two outputs as shown in Fig. 10.9(b) and (d), where simulations have been run for different values of m. Even when m equals 0.3, there is still a great improvement compared to the uncoupled case.

The bottom line is that reasonable leakage inductance which is required to reduce the ripple currents will not significantly degrade the improvements on dc and ac cross-regulations.

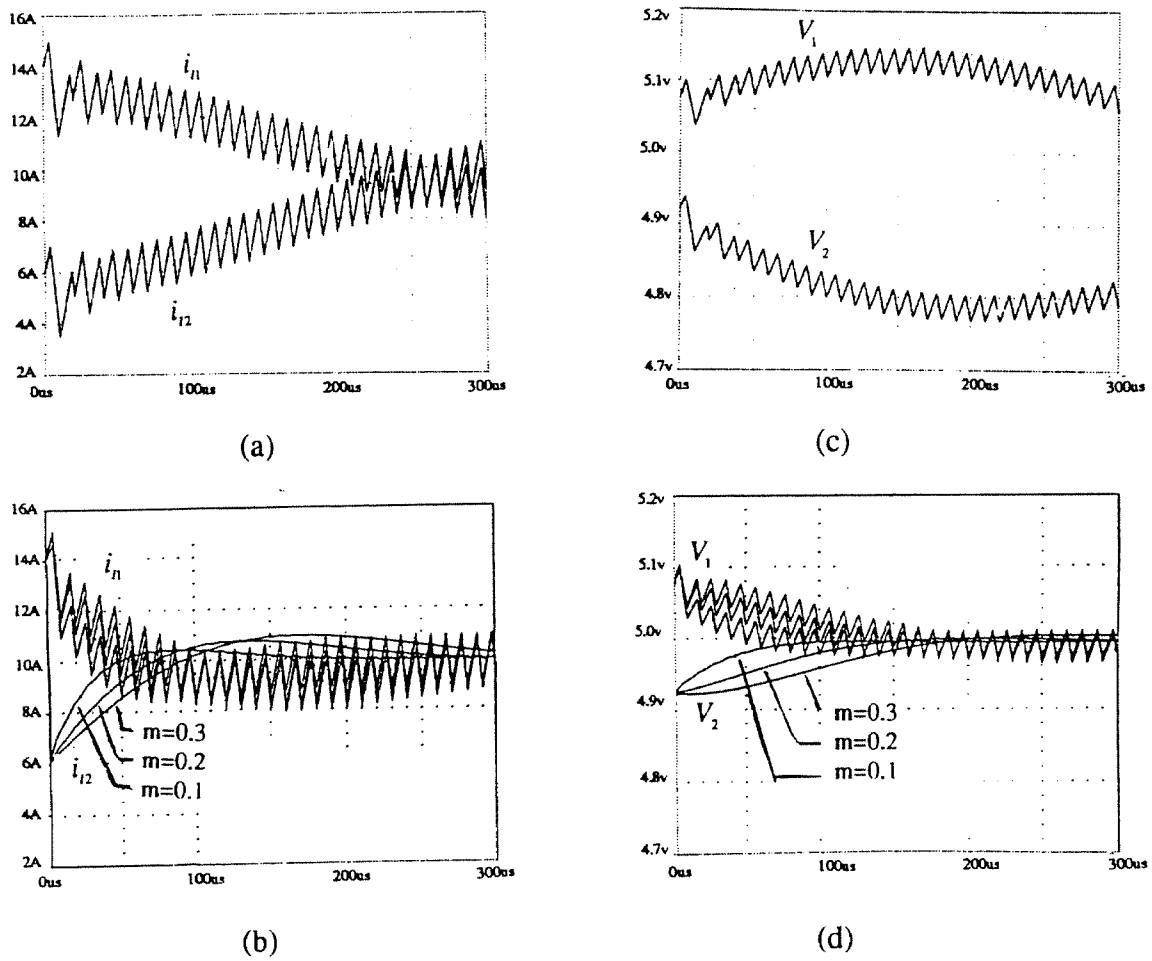


Figure 10.9: PSPICE simulation results for dynamic cross-regulation: (a) inductor current waveforms without coupling inductors. (b) inductor current waveforms with coupled inductors. (c) output voltage waveforms without coupling inductors. (d) output voltage waveforms with coupled inductors.

10.4 Small-Signal Model of Current Programmed Two Output Forward Converters

Current-programming has become widely adopted in switching power converters because of several advantages as line-noise rejection, automatic overload protection, easy paralleling of multiple converters, and design flexibility in improving dynamics.

A unified model for current-programmed converters has recently been proposed [36], which is an extension of a familiar model [24]. This method is used in this section to derive analytical model of the two-output forward converter shown in Fig. 10.3. Several assumptions are made as follows:

1. Continuous conduction mode is considered here.

2. All the switches are ideal.

3. The transformer is ideal.

4. The output filter inductors have negligible core and winding losses.

5. The output capacitors have zero ESR.

The circuit parasitics introduce more damping to the circuit, and add high frequency ESR zeros, which can be neglected in the first-order analysis.

Figure 10.10 shows the small-signal low frequency model of the forward converter in Fig. 10.5 by use of the new unified model. The feedback of the inductor current and the feedforward of the line voltage introduced by current-programming are shown explicitly.

The sensed current i_{lm} can be expressed as

$$i_{lm} = i_c - M_c T_s d - \frac{dd' T_s}{2L_e} V_g \,, \tag{10.32}$$

$$\text{where} \quad L_e = \frac{L_{eq}^2}{L_{l1} + L_{l2}} = L_m + L_{l1} \parallel L_{l2} \,. \tag{10.33}$$

M_c is the stabilizing ramp slope, and i_c is the reference current. Perturbation of Eq. (10.32) yields

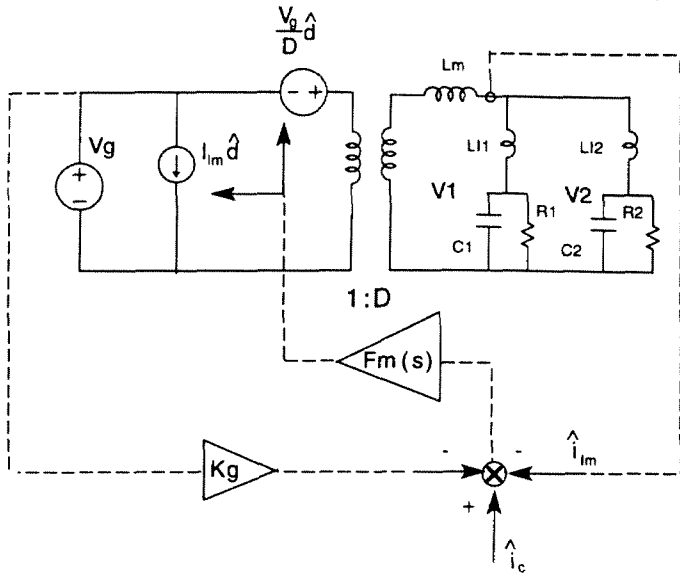


Figure 10.10: Small-signal low frequency model of the current programmed dual output forward converter.

$$\hat{i}_{lm} = \hat{i}_c - [M_c + \frac{(D'-D)V_g}{2L_e}]T_s\hat{d} - \frac{DD'T_s}{2L_e}\hat{V}_g\,. \tag{10.34}$$

Equation (10.34) can be further manipulated into the duty-ratio control law

$$\hat{d} = \frac{2L_e f_s}{V_g(nD'-D)}(\hat{i}_c - \hat{i}_{lm} - \frac{DD'}{2L_e f_s}\hat{V}_g)\,. \tag{10.35}$$

Therefore, it is found in Fig. 10.10:

$$F_m = \frac{2L_e f_s}{V_g(nD'-D)}\,, \tag{10.36}$$

$$k_g = \frac{DD'}{2L_e f_s}\,. \tag{10.37}$$

Here, "n" relates the stabilizing ramp M_c to the slope of the mutual inductor current

during the transistor on-time:

$$n = 1 + \frac{2M_c}{M_1}. \tag{10.38}$$

State-space averaging method is used to derive the basic transfer functions with the current loop closed. Consequently, design of the outside voltage feedback loop can be pursued in the same way as design of a duty-ratio programmed converter.

The state equations for ac small-signal model are:

$$\hat{\dot{X}} = A\hat{X} + b\hat{V}_g + [(A_1 - A_2)X + (b_1 - b_2)V_g]\hat{d}, \tag{10.39}$$

$$\text{where} \quad X = [i_{L_{l1}} \;\; i_{L_{l2}} \;\; v_1 \;\; v_2], \tag{10.40}$$

$$b_1 = \begin{bmatrix} \frac{L_{l2}}{L_{eq}^2} & \frac{L_{l1}}{L_{eq}^2} & 0 & 0 \end{bmatrix}, \tag{10.41}$$

$$b_2 = 0, \tag{10.42}$$

$$A_1 = A_2 = \begin{bmatrix} 0 & 0 & \frac{L_m + L_{l2}}{L_{eq}^2} & \frac{L_m}{L_{eq}^2} \\ 0 & 0 & \frac{L_m}{L_{eq}^2} & \frac{L_m + L_n}{L_{eq}^2} \\ \frac{1}{C_1} & 0 & -\frac{1}{C_1 R_1} & 0 \\ 0 & \frac{1}{C_2} & 0 & -\frac{1}{C_2 R_2} \end{bmatrix}. \tag{10.43}$$

Substituting Eq. (10.35) into Eq. (10.39), we can derive the control-to-output transfer function and the line-to-output transfer functions (audio susceptibility).

$$A_{1c} = \frac{\hat{V}_1}{\hat{i}_c} = \frac{R_{22} \parallel R_1 \parallel R_2}{1 + \frac{s}{w_c}} \frac{1 + \frac{1}{Q_z}\frac{1}{w_z} + (\frac{s}{w_z})^2}{(1 + \frac{s}{w_{pl}})(1 + \frac{s}{Q_p w_{po}} + \frac{s^2}{w_{po}^2})}, \tag{10.44}$$

$$A_{1g} = \frac{\hat{V}_1}{\hat{V}_g} = \frac{D(nD' - 1)}{2f_s L_e} \frac{R_{22} \parallel R_1 \parallel R_2}{1 + \frac{s}{w_c}} \frac{1 + \frac{1}{Q_z}\frac{1}{w_z} + (\frac{s}{w_z})^2}{(1 + \frac{s}{w_{pl}})(1 + \frac{s}{Q_p w_{po}} + \frac{s^2}{w_{po}^2})}, \tag{10.45}$$

$$\text{where} \quad R_{22} = \frac{w_s}{\pi(nD' - D)} L_e, \tag{10.46}$$

$$w_z = \frac{1}{\sqrt{C_2 L_{l2}}}, \tag{10.47}$$

$$Q_z = R_2\sqrt{\frac{C_2}{L_{l2}}}, \tag{10.48}$$

$$w_{po} = \sqrt{\frac{1}{(L_{l1}+L_{l2})(C_1 \parallel C_2)}}, \tag{10.49}$$

$$Q_p = \frac{\frac{1}{R_o}}{\frac{C_1}{C_1+C_2}\frac{1}{R_2}+\frac{C_2}{C_1+C_2}\frac{1}{R_1}+\frac{C_1L_{l1}+C_2L_{l2}}{(L_{l1}+L_{l2})(C_1+C_2)}\frac{1}{R_{22}}}, \tag{10.50}$$

$$\text{and} \quad R_o = \sqrt{\frac{L_{l1}+L_{l2}}{C_1 \parallel C_2}}, \tag{10.51}$$

$$w_{p1} = \frac{1}{(C_1+C_2)(R_1 \parallel R_2 \parallel R_{22})}, \tag{10.52}$$

$$w_c = \frac{w_s}{\pi(nD'-D)}. \tag{10.53}$$

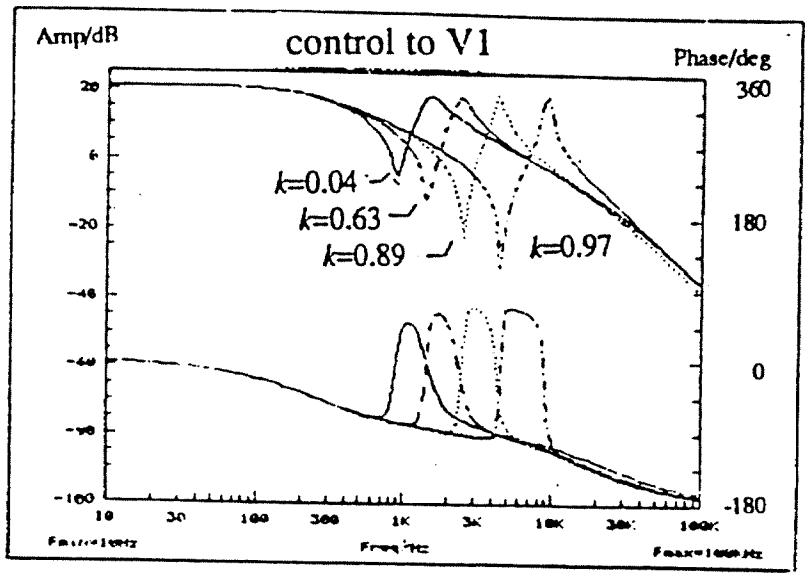
By exchanging the roles of the two outputs, we can get the transfer functions for the second output.

Simulations have been performed with SCAMP (Switching Converter Analysis and Measurement Program) developed by Caltech. The frequency responses are shown in Fig. 10.11, which agree with the predictions.

Notice that in A_{1c} (Fig. 10.11(a)), the resonant zeros come before the resonant poles; while, A_{2c} (Fig. 10.11(b)) has the resonant poles first. Feedback design is easier if the first output is sensed and directly controlled. However, if both small ripple and tight regulation are required of the same output, such as in the preferred zero ripple case, the resonant zeros cannot be used to compensate for the resonant poles. The details for the design will be demonstrated by an example in the next section. Also, in a real converter circuit, parasitics cause more damping effect to reduce the value of Q, and ESR associated with output filter capacitors gives rise to high frequency zeros. All these effects need to be considered in a practical design.

As an extension of the low frequency model, it has been proved [36] that the sampling effect of a switching converter can be represented by one additional pole in the current-loop gain derived from the low frequency model. The extended model can predict high frequency dynamics of current-loop gain with good accuracy up to the half switching frequency. This additional pole, together with w_c , gives a pair of poles in quadratic form $(1+\frac{1}{Q_s}\frac{s}{w_s/2}+$

a)



b)

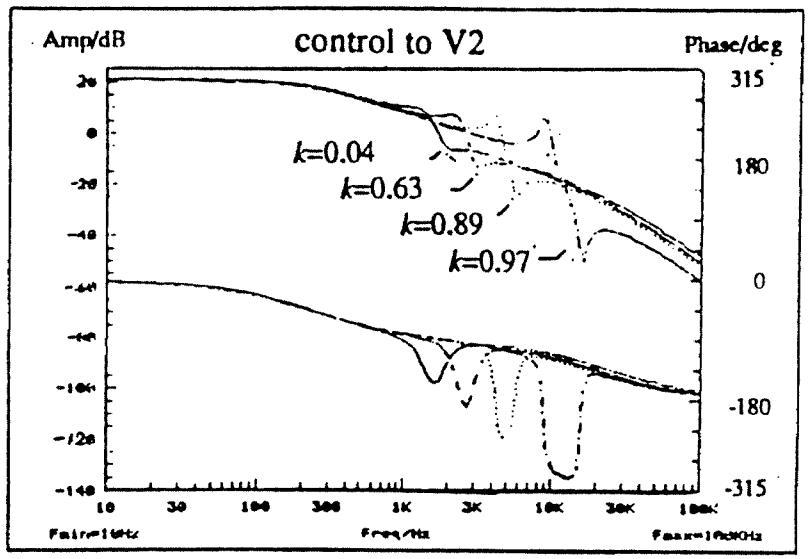


Figure 10.11: SCAMP simulation transfer functions of current-programmed dual output forward converter: (a) control to the first output. (b) control to the second output. (with the coupling coefficient k as the running parameter)

$\frac{s^2}{(w_s/2)^2}$) in Eqs. (10.44 and (10.45), and $Q_s = \frac{2}{\pi(nD'-D)}$. If no compensating ramp is used, Q_s is high, producing peaking at $\frac{f_s}{2}$. When wide bandwidth of the feedback control is required, this can affect the designed phase margin. On the other hand, if $Q_s \ll 0.5$, the sampling effect is barely visible. However, when M_c is too large, the benefits of the current-programming control are lost. Therefore, M_c has to be properly designed.

10.5 Generalization to Multiple-Output Forward Converters

Suppose that a Forward converter has n_o outputs, and all the output inductors are coupled together. The operating mode is as follows: the first output is in DICM; while all the other outputs are in CICM. We have

$$V_2 = V_3 = \cdots = V_{n_o} = DV_g\,. \tag{10.54}$$

The remaining of this section is devoted to find V_1.

The coupled-inductor with n_o windings has the following circuit equations:

$$\begin{bmatrix} v_1 \\ v_2 \\ \vdots \\ v_n \end{bmatrix} = \begin{bmatrix} L_{11} & L_{12} & \cdots & L_{1n_o} \\ L_{21} & L_{22} & \cdots & L_{2n_o} \\ \vdots & \vdots & \ddots & \vdots \\ L_{n_o1} & L_{n_o2} & \cdots & L_{n_on_o} \end{bmatrix} \begin{bmatrix} \frac{di_1}{dt} \\ \frac{di_2}{dt} \\ \vdots \\ \frac{di_{n_o}}{dt} \end{bmatrix}. \tag{10.55}$$

By reciprocity theorem, $L_{ij} = L_{ji}$. Thus, the inductance matrix is symmetric. Thereafter, $\mathbf{L}$ denotes the inductance matrix, and $\mathbf{L}_{ij}$ denotes the cofactor of element L_{ij}.

Integrals of i_1 can be found from Eq. (10.55), and have to satisfy the following two constraints:

$$\int_0^{(D+D_2)T_s} di_1 = 0\,, \tag{10.56}$$

$$\int_0^{DT_s} di_1 = I_{1pp} = \frac{2V_1}{R_1}\,. \tag{10.57}$$

If we define

$$K_1' \triangleq \frac{2f_s L_{11}}{R_1}, \tag{10.58}$$

$$\alpha' \triangleq \frac{det\mathbf{L}}{L_{11}\sum_{j=1}^{n_o}\mathbf{L}_{1j}}, \tag{10.59}$$

and use Eqs. (10.54)-(10.57), we can solve V_1.

$$V_1 = V_g \frac{2(\mathbf{L}_{11} + D'\sum_{j=2}^{n_o}\mathbf{L}_{1j})}{\mathbf{L}_{11} + \frac{\alpha' K_1'}{D}\sum_{j=2}^{n_o}\mathbf{L}_{1j} + \sqrt{(\mathbf{L}_{11} + \frac{\alpha' K_1'}{D}\sum_{j=2}^{n_o}\mathbf{L}_{1j})^2 + \frac{4\alpha' K_1' \mathbf{L}_{11}}{D^2}(\mathbf{L}_{11} + D'\sum_{j=2}^{n_o}\mathbf{L}_{1j})}}. \tag{10.60}$$

A special case is the zero ripple condition in all except the first winding. From Eqs. (10.54) and (10.55), we have

$$L_{11} = L_{12} = \cdots = L_{1n_o}. \tag{10.61}$$

If the $n_o - 1$ conditions (Eq. (10.61)) are satisfied simultaneously, all ripple current is steered into the first winding.

Substituting Eq. (10.61) into Eq. (10.59) gives $\alpha' = 1$. Thus, Eq. (10.60) can be simplified by replacing α' with 1 as in the two-output case.

For the two winding coupled-inductor model in Section 10.3,

$$\mathbf{L}_{11} = L_m(1+m), \tag{10.62}$$

$$\sum_{j=2}^{n_o}\mathbf{L}_{1j} = -L_m. \tag{10.63}$$

The result derived by substituting Eqs. (10.62) and (10.63) into Eq. (10.60) coincides with that in Section 10.3 (Eq. (10.23)).

10.6 Experimental Verification

A prototype of dual output forward converter with the current-programmed feedback control is built to verify the predictions. The second output is sensed for tight regulation.

The operating conditions are as follows: Input voltage is $24V$, nominal voltages for both outputs are $12V$, full load currents are $3A$, and the switching frequency f_s is 50kHz.

Main components used in the prototype are listed below: transistor: IRF640, diodes:

ERC8849-009, C_1, C_2: 120uF, ESR of the capacitors: 0.13 Ω, current programmed controller: UC3846, core for isolation transformer: PQ32/30. The coupled-inductor is designed in Subsection 10.6.1.

10.6.1 Design of the Coupled-Inductor

In this subsection, a design procedure for zero ripple two-winding coupled inductors with a specified cross-regulation parameter m is developed.

The common design specifications are as follows [9, 38]:

1. Zero ripple condition must be satisfied.

2. Inductor L_m is designed by the ripple current requirement.

3. Flux density everywhere in the core must be less than the saturation flux density B_m.

Here, we have another requirement: m is prescribed to give required cross-regulation performances.

A EE core is chosen for this design example. The two windings are wound side-by-side around the center leg of the core (Fig. 10.12(a)). The reluctance model and inductance model are shown in Fig. 10.12(b) and (c). Assume $R_{l1} = R_{l2}$. Consequently, $L_{l1} = L_{l2}$. For the case of zero ripple current in the secondary winding, the turns ratio has to be designed as:

$$\frac{N_1}{N_2} = \frac{L_m}{L_{l1} + L_m} = \frac{R_{l1}}{R_{l1} + R_m}, \tag{10.64}$$

$$\text{where} \quad R_m = R_x \parallel R_l + R_x, \tag{10.65}$$

$$L_m = \frac{N_1^2}{R_m}, \tag{10.66}$$

$$L_{l1} = \frac{N_1^2}{R_{l1}}. \tag{10.67}$$

With the zero ripple condition, the circuit model can be simplified as in Fig. 10.12(d), where

$$L'_m = L_{l1} + L_m, \tag{10.68}$$

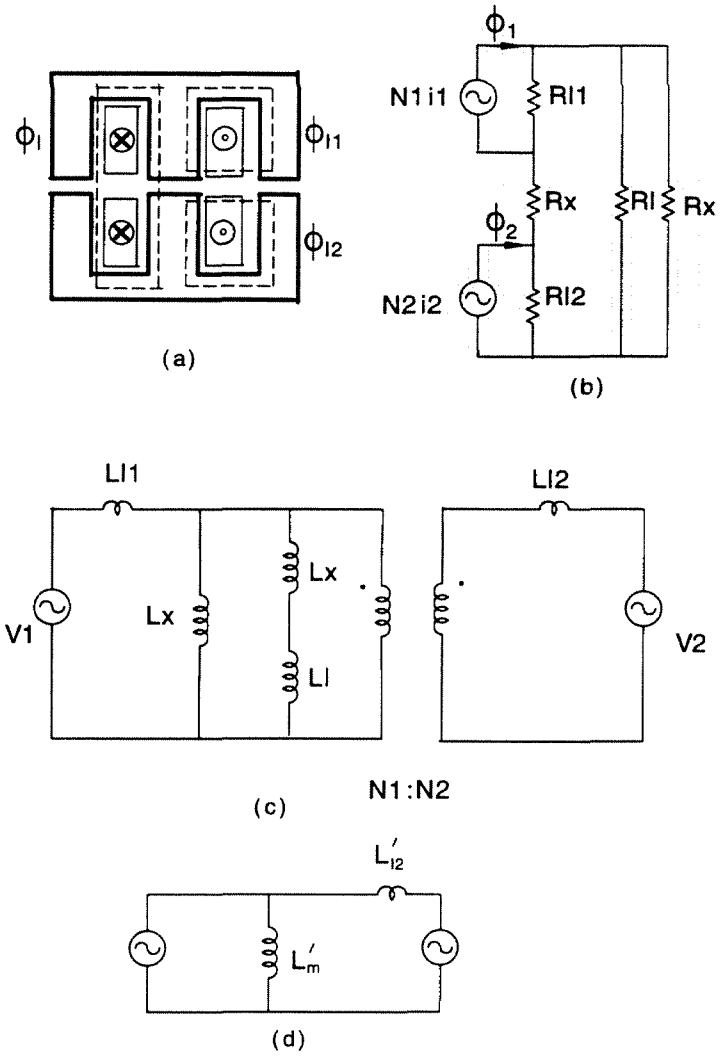


Figure 10.12: (a) A coupled-inductor structure; (b) the reluctance model; (c) the inductance model; and (d) equivalent circuit to get zero ripple in the secondary winding.

$$L'_{l2} = L_{l2} + L_{l1}\frac{L_{l1}+L_m}{L_m}. \tag{10.69}$$

Also, we have

$$m = \frac{L'_{l2}}{L'_m} = \frac{R_m(R_m+2R_{l1})}{R_{l1}^2}. \tag{10.70}$$

which gives

$$R_m = (\sqrt{1+m}-1)R_{l1} \triangleq \beta R_{l1}. \tag{10.71}$$

Note that, β is defined to simplify the notation in the following design procedure.

From the reluctance model (Fig. 10.12(b)), the maximum flux is in the center leg. Assume ϕ_1 is the peak flux in the top part center leg, and ϕ_2 is the peak flux in the bottom part center leg. They are given by

$$\phi_1 = \frac{N_1 I_1}{R_m \parallel R_{l1}} + \frac{N_2 I_2}{R_m \parallel R_{l2}}\frac{R_{l2}}{R_m+R_{l2}} = \frac{L'_m}{N_1}(I_1+I_2), \tag{10.72}$$

$$\phi_2 = \frac{N_2 I_2}{R_m \parallel R_{l2}} + \frac{N_1 I_1}{R_m \parallel R_{l1}}\frac{R_{l1}}{R_m+R_{l1}} = \frac{L'_m}{N_1}(\frac{N_1}{N_2}I_1 + \frac{N_2}{N_1}I_2). \tag{10.73}$$

Equations (10.64), (10.65), (10.68), (10.72) and (10.73) can be rewritten in terms of β by use of Eq. (10.71), all the design equations are written here for convenience:

$$L'_m = (1+\frac{1}{\beta})\frac{N_1^2}{R_{l1}}, \tag{10.74}$$

$$\frac{N_2}{N_1} = \beta + 1. \tag{10.75}$$

$$R_x \parallel R_l + R_x = R_m = \beta R_{l1}, \tag{10.76}$$

$$B_m S \geq \phi_1 = \frac{L'_m}{N_1}(I_1+I_2), \tag{10.77}$$

$$B_m S \geq \phi_2 = \frac{L'_m}{N_1}[\frac{I_1}{\beta+1} + (\beta+1)I_2]. \tag{10.78}$$

The above equations are used to solve the four unknown quantities: the core cross-section S, N_1, N_2, and the gap width x.

First, we need to estimate the core cross-section S. Leakage parameters l and l_1 are

defined as

$$R_l = \frac{l}{\mu_o S}, \tag{10.79}$$

$$R_{l1} = \frac{l_1}{\mu_o S}. \tag{10.80}$$

Leakage parameter l was originally defined in [9], where it was found that for many standard cores it has an approximately constant value $l \approx 2mm$. Since for some common cores, R_{l1} is measured about three times bigger than R_l. Therefore, we use $l = 6mm$ in estimation of the core cross-section.

Recall that the parameter m, consequently, β is prescribed by the cross-regulation specification. S is determined by the more restrictive one of Eq. (10.77) and Eq. (10.78). Without loss of generality, Eq. (10.78) is used here

$$S \geq \frac{L'_m}{B_m N_1}[\frac{I_1}{\beta+1} + (\beta+1)I_2], \tag{10.81}$$

N_1 can be derived from Eq. (10.74). Therefore,

$$S \geq \frac{\mu_o L'_m[\frac{I_1}{\beta+1} + (\beta+1)I_2]^2(\beta+1)}{B_m^2 l_1 \beta}. \tag{10.82}$$

Once the core is chosen, we can measure the actual R_{l1} and check whether B_m is less than the specified value. If not, a core with bigger size should be used.

Next, the design equations (10.74), (10.75) and (10.76) are solved to give the closed form solution for N_1, N_2 and x:

$$N_1 = \sqrt{\frac{\beta}{\beta+1} L'_m R_{l1}}, \tag{10.83}$$

$$N_2 = (\beta+1)N_1, \tag{10.84}$$

$$R_x = \frac{\sqrt{4R_l^2 + \beta^2 R_{l1}^2} + \beta R_{l1} - 2R_l}{2}. \tag{10.85}$$

As an example, we shall design the couple inductors in the prototype. The dc operating conditions are listed at the beginning of Section 10.6. Assume the peak-to-peak ripple

current $I_{1pp} = 20\%I_1 = 0.6A$, we have

$$L'_m = \frac{\int_{DT_s}^{T_s} v_{Lm'}dt}{I_{1pp}} = \frac{V_1 D'T_s}{I_{1pp}} = 0.2mH\,. \tag{10.86}$$

Assume that $m = 2.7$ and $B_m = 0.35T$. It is found that Eq. (10.78) is more restrictive than Eq. (10.77). The cross-section $S = 124mm^2$ is derived from Eq. (10.82). A EE40 core is chosen, which has a cross-section $S = 148mm^2$. The measured leakage reluctance are: $R_{l1} = 35[1/\mu H]$; $R_l = 10[1/\mu H]$. Thus, $l_1 = 6.5mm$ and $l = 1.86mm$, which are close to the estimated values. The maximum flux density is 0.28T, which is less than the specified B_m. Therefore, the choice of core is valid.

By definition, $\beta = \sqrt{1+m} - 1 = 0.127$, Eqs. (10.83) to (10.85) give

$$N_1 = 28\,, \tag{10.87}$$

$$N_2 = 31\,, \tag{10.88}$$

$$R_x = 2.5[1/\mu H]\,, \quad \text{which gives} \quad x = 0.4mm\,. \tag{10.89}$$

Note that, although the design procedure is illustrated on a spacer gap core and side-by-side winding arrangement. The basic ideas can be applied to different gap structures (such as one-leg gap) and winding arrangements (such as top-bottom windings).

As a summary, the design procedure for zero ripple coupled inductors used in multiple-output converters are as follows:

1. Given the cross-regulation specification, the maximum relative first-order error is determined, and the required parameter m can be found from Eq. (10.31).

2. Inductance L'_m in the non-zero output is determined by the ripple current specification.

3. Given L'_m, m, and B_m, the core size is estimated by use of the leakage parameter.

4. For the given core, leakage resistances are measured, the turns ratios and gap size can be determined by required inductance, m, and the zero ripple condition.

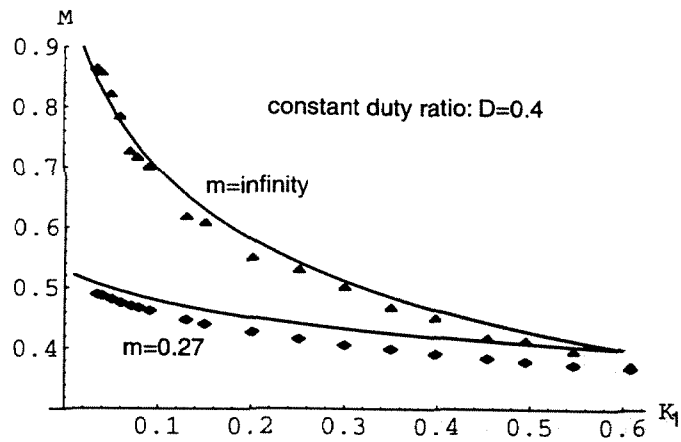


Figure 10.13: Measured data for the conversion ratio M vs. K_1, theoretical predictions are plotted in line as comparison.

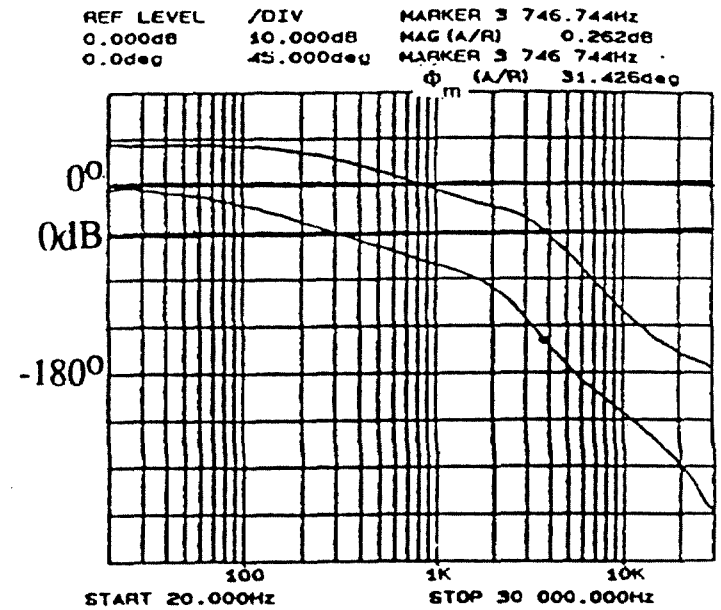
10.6.2 Measurements

L'_m is measured as 0.192mH, and L'_{l2} is measured as 0.052mH. Therefore, m is 0.27 as designed.

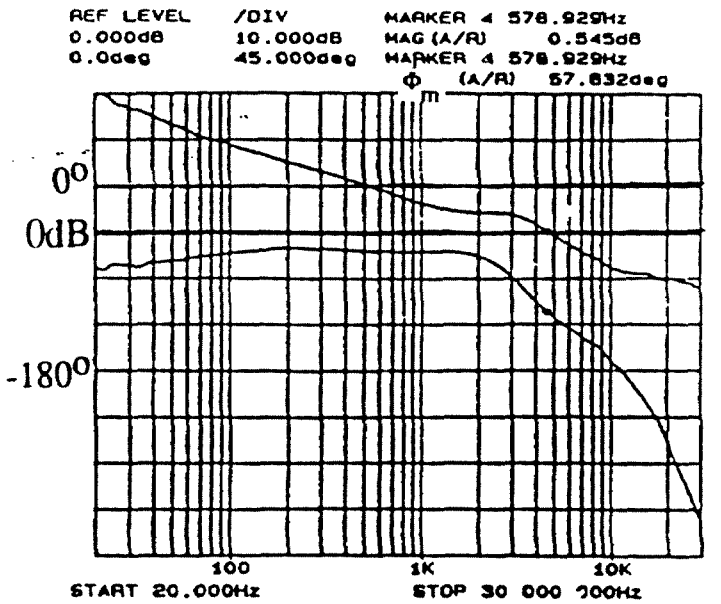
Measured data for the conversion ratio M vs. K_1 are plotted in Fig. 10.13, for m equals 0.27 and infinity, respectively. They match well with the theoretical curves. The slight deviation is caused by the parasitics in the circuit that are not taken into account in the prediction.

The closed-loop control to the second output transfer function without compensation is given in Fig. 10.14(a), with both loads at 6 Ω and duty ratio at 0.5. This verifies the calculations: $f_{po} = 250Hz$, $f_{p1} = 2.85kHz$, and two ESR zeros at $10kHz$. The stabilizing ramp M_c in current loop is chosen to have Q_s close to 1. Therefore, there are two resonant poles at half switching frequency with no peaking effect. This also explains why the phase curve goes to $-270°$ before half switching frequency.

To improve dynamic characteristic, a three-pole and two-zero compensation network is added in the voltage feedback loop. The first pole is placed at the origin for tight dc regulation, the second pole is placed to cancel one of the ESR zero, the final pole is placed around $25kHz$. The first zero is placed before f_{p1} of the power stage, the second zero is placed before the resonant frequency f_{p2}. The measured response is shown in Fig. 10.14(b).



(a)



(b)

Figure 10.14: Closed-loop control to the second output frequency response: (a) without compensation; (b) with compensation

10.7 Conclusion

In buck-derived converters, the coupled-inductor technique offers a simple method to considerably improve dc cross-regulation during light loads and reduce the resonant effect and time delay in ac cross-regulation. From cross-regulation point of view, the tighter the coupling is, the better the performance can be achieved. However, non-ideal factors in the converter will give rise to the voltage conflict across the windings of the coupled inductors, requiring certain amount of leakage inductance to reduce the circulating current. With the full understanding of this phenomenon, the choice of a good trade-off between the cross-regulation characteristic and the sensitivity of the ripple current can be made according to design specifications.

The coupled inductors can be designed to eliminate the ripple currents from all but one of the output inductors, thereby erase the minimum load requirement on most outputs. Zero ripple current design is preferred in many applications. In addition to the conventional coupled-inductor design criteria [9], the value of m, which is directly related to the cross-regulation performance, becomes an important design parameter in regard to the choices of core size and winding configuration.

A small-signal model for a two output current programmed forward converter is established. Transfer functions with current programming loop closed are derived, then the familiar methods for single-loop feedback systems can be employed to close the voltage loop [24].

Although the analysis and design are mainly carried out on a two output forward converter, the results can be extended to any buck-derived converter with three or more outputs.

Chapter 11 Conclusion

Synthesis of PWM dc-to-dc converters is a fundamental issue in power electronics. A new synthesis approach is developed in this thesis. This approach is analytic which guarantees the search for a whole class of converters with given properties is complete. On the other hand, it still keeps the circuit insight. The synthesis of PWM converters can be carried out efficiently in a generalized range without limited by the number of input sources, the number of output loads, and the number of switched-networks in each switching cycle.

The new synthesis method is based on the recognition of the equivalent ac and dc circuit of a PWM converter, which separates the switches from the remaining LTI elements (capacitors and inductors).

The first part of synthesis procedure is carried out without the presentation of inductors and capacitors: For a chosen ac circuit, each switch can be modeled by a voltage or current source in individual switching intervals. The value of each source is given in terms of corresponding average switch voltage or current. Volt-second and ampere-second balance equations can be derived from the ac circuit, which, physically, can be interpreted by the corresponding volt-second balance equation for an inductor or ampere-second balance for a capacitor. Furthermore, since both ac and dc circuits are in terms of average (dc) quantities, the topological relation between ac and its associated dc circuits is uncovered (Proposition 2.6 for two switched-network converters; Eqs. (2.57) and (2.58) for three or more switched-network converters without self-loop(s) in their dc circuits; Eqs. (2.57) and (B.6) for converters with self-loop(s) in their dc circuits). Therefore, the dc circuits can be enumerated. Based on the balance equations of the ac circuit and the matrix representations of the associated dc circuits, a formalized dc model is established for two-switched-network converters in Section 2.5.2, and extended to three or more switched-network converters in Section 2.7 and Appendix B. By use of the dc model, the degenerate dc circuits can be excluded; and the dc conversion ratio and switch implementation can be derived for each non-degenerate dc circuit. The desirable dc circuits can be sorted out by the dc gain, the order of the dc circuit (Definition 3.1), types of the switches (Section 2.6), and isolation implementation (Proposition 2.11) and other properties.

It is worth noting that, in a PWM dc-to-dc converter, the main function of each switch is either converting dc input power into ac power or rectifying ac power back into dc power at the output side. These two types of switches together provide the feature of a *controllable* transformer (whose operating range extends down to dc) and give the *controllable* dc voltage gain or dc current gain of the converter. The power flow characteristics is discussed in Section 2.8, where an important parameter - *switch utilization ratio* is defined for the comparison of different converter topologies.

The reactive elements are indispensable to remove the fundamental and harmonics of switching frequency components in the switch voltage and current waveforms. The insertion of inductors and capacitors is completely formalized (Chapter 3 to Chapter 5). The basic insertion procedure guarantees all the reactive elements inserted are *essential* (Section 4.3), and the converters with minimum elements can be selected. In order to generate converters with continuous input and output current, the insertion procedure can be modified to guarantee continuous terminal currents in advance (Section 4.5).

The synthesis procedure can generate converters with loops consisting only of capacitors and possibly the voltage source, or cut-sets consisting only of inductors and possibly the current source. For example, a class of three-switch converters is generated in Chapter 5, each of which has a loop of capacitors and possibly the voltage source during one time interval. The detail analysis for a particular three-switch converter is carried out in Chapter 9. This converter is of special interest in high-voltage applications.

Synthesis of a class of four-switch converters is undertaken in Chapter 6. Three novel single-switch converters are found with large step-up ratio. Discussion of the operation modes and experimental verifications are given in Chapter 6.

The synthesis procedure is based on ac and dc equivalent circuits. Therefore, increasing the number of switched-networks in each switching cycle does not affect the complexity of synthesis work. Synthesis of a class of three-switch, three-switched-network converters is completed in Chapter 7. The main difference compared with synthesis of two-switched-network converters is that, one or more switches in a three-switched-network converter may have zero average current or zero average voltage. While zero average current of a switch has little effect on the synthesis procedure (Chapter 7); zero average voltage of a switch means the existence of a self-loop in the corresponding dc circuit, which poses some difficulty in deriving the matrix representation. This case is tackled separately in Appendix B.

Synthesis of multiple-output converters is illustrated in Chapter 8 through the generation of a class of three-switch, two-output converters, which can provide opposite polarity output voltages without a transformer.

Multiple-output converters are used in many applications. For some converter topologies, the cross-regulation performances can be improved dramatically by coupling the inductors. A detailed study in Chapter 10 gives the quantitative relationship between coupled-inductor parameters and the degree of cross-regulation improvements, which leads to the establishment of an explicit design procedure for the coupled inductors.

Finally, it is worthy to mention that, the discovery of a generic ac circuit model also leads to a novel averaged model for switches based on small-signal perturbation of the balance equations. This modeling method is originated in [17], and extended to a generic model for converters with current-mode control or converters in discontinuous inductor current mode [37]. Extensions can also be made to cover quasi-resonant and soft-switching converters. The averaged switch model for the single-transistor four-switch converters is given in Section 6.4.

In summary, because of their different characteristics and functions, the separation of switches from the remaining linear and time-invariant circuit elements in a PWM converter is the underlying idea for both the systematic synthesis method established in this thesis, and the development of the novel model of switches.

Appendix A Proof of the Relation $\mathbf{H}_{21} = -\mathbf{H}_{12}^T$

The purpose of this appendix is to prove the relation given in Eq. (2.56), namely, $\mathbf{H}_{21} = -\mathbf{H}_{12}^T$.

The proof consists of two parts: First, it is proved that the dimensions of $\mathbf{H}_{12}^T$ and $\mathbf{H}_{21}$ are the same. Then, Tellegen Theorem is used to prove that the two matrices are equivalent.

The notations used here are defined as follows: b is the number of switch branches; n_a is the number of tree branches in the ac circuit; l_a is the number of links in the ac circuit; n_{V_loop} is the number of all linearly independent loops of voltage sources in the ac equivalent circuits during individual time intervals; n_{I_cutset} is the number of all linearly independent cut-sets of current sources in the ac equivalent circuits during individual time intervals; q is the number of linearly independent voltage equations in terms of the average switch voltages.

Part One of the Proof

In the first part of proof, for easy understanding, the basic ideas is illustrated on a three-switch three-interval ac circuit. The ac circuit and its three equivalent circuits are shown in Fig. A.1. In the ac circuit, $n_a = 1$ and $l_a = 2$.

From the equivalent circuits, the voltage of S_1 can be modeled as:

$$v_{s1} = \begin{cases} -V_{s1} & \text{during } D_1 T_s\,, \\ -V_{s1} & \text{during } D_2 T_s\,, \\ -V_{s3} & \text{during } D_3 T_s\,. \end{cases} \tag{A.1}$$

Since the average of any ac voltage in per switching cycle is equal to zero, we have

$$\frac{1}{T_s}\int_0^{T_s} v_{s1}\,dt = -V_{s1}D_1 - V_{s1}D_2 - V_{s3}D_3 = 0\,. \tag{A.2}$$

Similarly, volt-second balance equations can be written for S_2 and S_3. In a summary,

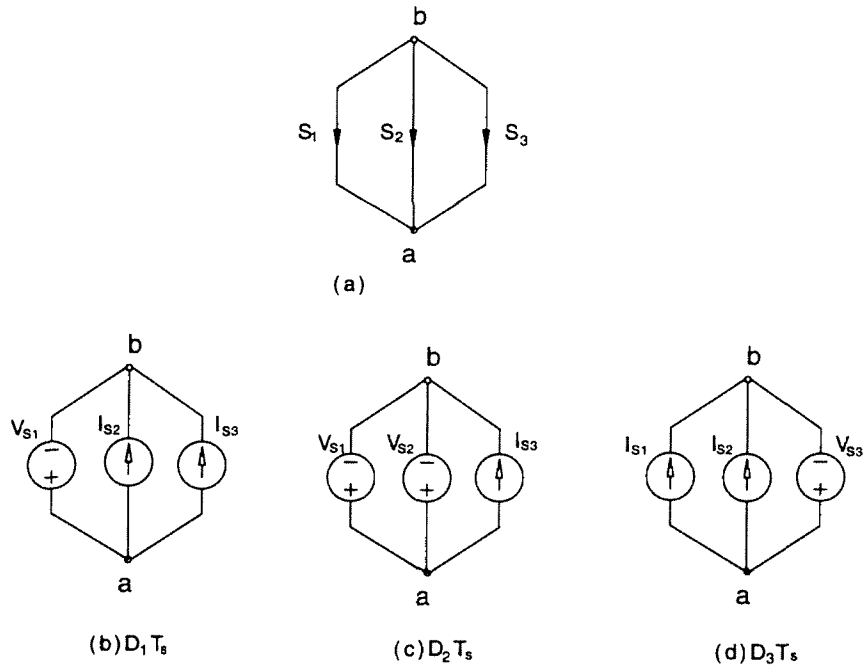


Figure A.1: The ac circuit with reference orientations(a) and its equivalent circuits: During time interval D_1T_s, S_1 is on, and S_2, S_3 are off(b); during time interval D_2T_s, S_1, S_2 are on. and S_3 are off(c); and during time interval D_3T_s, S_3 is on, and S_1, S_2 are off(d).

we have the following $b = 3$ equations

$$\begin{matrix} v_{s1} \\ v_{s2} \\ v_{s1} \end{matrix} \begin{pmatrix} -V_{s1} & -V_{s1} & -V_{s3} \\ -V_{s1} & -V_{s2} & -V_{s3} \\ -V_{s1} & -V_{s1} & -V_{s3} \end{pmatrix} \begin{pmatrix} D_1 \\ D_2 \\ D_3 \end{pmatrix} = 0 . \tag{A.3}$$

From the ac circuit topology, there are $l_a = 2$ constrains between the three ac voltages:

$$v_{s1} = v_{s2} , \tag{A.4}$$

$$v_{s1} = v_{s3} . \tag{A.5}$$

Therefore, out of the $b = 3$ voltage equations in Eq. (A.3), only $b - l_a = 1$ is linearly independent.

In addition, one loop consisting only of voltage sources is found in equivalent circuit for

time interval D_2T_s. Thus, $n_{V\_loop} = 1$, and

$$V_{s1} = V_{s2}\,. \tag{A.6}$$

Consequently, this ac circuit has $q = b - l_a + n_{V\_loop} = 2$ linearly independent voltage equations expressed as follows:

$$\begin{bmatrix} V_{s1} \\ V_{s2} \end{bmatrix} = \begin{bmatrix} -\frac{D_3}{D_1+D_2} \\ -\frac{D_3}{D_1+D_2} \end{bmatrix} V_{s3} = -\mathbf{H}_{12} V_{s3}\,, \tag{A.7}$$

where $\mathbf{H}_{12}$ is a $q \times (b-q)$ matrix.

Next, we are going to derive the current equations. In the equivalent circuit for time interval D_2T_s (Fig. A.1), $i_{s1} + i_{s2} = -I_{s2}$; however it is impossible to uniquely determine i_{s1} and i_{s2}, because both switches are modeled by voltage sources, which form a loop.

The average of $i_{s1} + i_{s2}$ in per switching cycle is equal to zero, so is the average of i_{s3}. Thus, we have the following $b - n_{V\_loop} = 2$ equations:

$$\begin{matrix} i_{s1} + i_{s2} \\ i_{s3} \end{matrix} \begin{pmatrix} I_{s3} & I_{s3} & -I_{s1} - I_{s2} \\ -I_{s3} & -I_{s3} & I_{s1} + I_{s2} \end{pmatrix} \begin{pmatrix} D_1 \\ D_2 \\ D_3 \end{pmatrix} = 0\,. \tag{A.8}$$

Also, from the ac circuit topology, there is $n_a = 1$ constrain between the three ac currents, which is $i_{s1} + i_{s2} + i_{s3} = 0$. Therefore, only one of the $b - n_{V\_loop} = 2$ current equations in Eq. (A.8), namely, $b - n_{V\_loop} - n_a = 1$ is linearly independent. Since $b - n_{V\_loop} - n_a = b - q$, the only linearly independent current equation can be written as

$$I_{s3} = \begin{bmatrix} \frac{D_3}{D_1+D_2} & \frac{D_3}{D_1+D_2} \end{bmatrix} \begin{bmatrix} I_{s1} \\ I_{s2} \end{bmatrix} = -\mathbf{H}_{21} \begin{bmatrix} I_{s1} \\ I_{s2} \end{bmatrix}\,, \tag{A.9}$$

where $\mathbf{H}_{21}$ is a $(b-q) \times q$ matrix. Thus $\mathbf{H}_{21}$ has the same dimensions as $\mathbf{H}_{12}^T$.

In this example, there is no cut-set of current sources in any of the ac equivalent circuits (Fig. A.1(b)-(c)), however, in a dual manner, we can prove that each linearly independent cut-set of current sources in the equivalent circuits shall reduce the number of linearly independent voltage equations by one, and increase the number of linearly independent current equations by one.

Thus, in the most general cases, there are q linearly independent voltage equations, where

$$q = b - l_a + n_{V\_loop} - n_{I\_cutset}\,, \tag{A.10}$$

and $b-q$ linearly independent current equations. If these equations are written by the hybrid matrices $\mathbf{H}_{12}$ and $\mathbf{H}_{21}$ as in Eqs. (A.8) and (A.9), the dimensions of $\mathbf{H}_{21}$ are equivalent to those of $\mathbf{H}_{12}^T$.

Part Two of the Proof

As discussed in Section 2.7, an ac circuit with b switches can be represented by a b-port network. An example of three-port network is shown in Fig. 2.7.

From the result in the first part of this appendix, the voltages of q switches(ports) can be expressed in terms of the voltages of the remaining $b-q$ switches(ports); while the currents of the $b-q$ switches(ports) can be expressed in terms of the currents of the q switches(ports). As in Section 2.7, the q ports are named current ports and the $b-q$ ports are named voltage ports. $\mathbf{V}_I$ and $\mathbf{I}_I$ denote the voltages and currents of the q current ports; while $\mathbf{V}_V$ and $\mathbf{I}_V$ denote the voltages and currents of the $b-q$ voltage ports.

Equations (2.54) and (2.55) can be rewritten as

$$\left[\begin{array}{c}\mathbf{V}_V\\ \hline \mathbf{V}_I\end{array}\right] = \left[\begin{array}{c}\mathbf{1}_{b-q}\\ \hline -\mathbf{H}_{12}\end{array}\right]\mathbf{V}_V\,, \tag{A.11}$$

$$\left[\begin{array}{c}\mathbf{I}_V\\ \hline \mathbf{I}_I\end{array}\right] = \left[\begin{array}{c}-\mathbf{H}_{21}\\ \hline \mathbf{1}_q\end{array}\right]\mathbf{I}_I\,. \tag{A.12}$$

Transposing of Eq. (A.12) and multiplying it by Eq. (A.12) give

$$\mathbf{I}_V^T\mathbf{V}_V + \mathbf{I}_I^T\mathbf{V}_I = \mathbf{I}_I^T\left[-\mathbf{H}_{21}^T - \mathbf{H}_{12}\right]\mathbf{V}_V\,. \tag{A.13}$$

It has been proved by Tellegen theorem (Eq. (2.63)) that the right-hand side of Eq. (A.13), namely, $\mathbf{I}_V^T\mathbf{V}_V + \mathbf{I}_I^T\mathbf{V}_I$, is constantly zero for arbitrary $\mathbf{I}_I$ and $\mathbf{V}_V$. Therefore,

$$\mathbf{H}_{21} = -\mathbf{H}_{12}^T\,. \tag{A.14}$$

The proof is thus completed. □

Note that, the switching sequence in Fig. A.1 has been chosen to illustrate the key ideas in the proof. Since $D_1 + D_2 = 1 - D_3$, only one independent control variable exists in Eqs. (A.7) and (A9), i.e., the class of three-switch converters have the same function as two-switch converters. Thus, this switching sequence has little practical meaning. For the same ac circuit, the switching sequence introduced in Appendix B (Fig. B.1) is of most practical interest.

Appendix B Modification of the Synthesis Procedure to Include Converters with Self-Loop(s) in Their Dc Circuits

The aim of this appendix is to modify the synthesis procedure in order to include the converters with self-loop(s) in their dc circuits.

In the basic synthesis procedure presented in Chapter 2 and Chapter 3, we assume that converters have no self-loop in their dc circuits . This assumption is always satisfied for two-switched-network (two-interval) converters (Proposition 2.5). However, for converters with three or more intervals, one or more self-loop may exist in their dc circuits. Furthermore, some of these converters provide desirable features, which will be shown later in this appendix. Therefore, it is worthwhile to extend the synthesis procedure beyond this assumption.

B.1 Basic Ideas of Modification

Recall that, in the synthesis procedure discussed in this thesis, the reduced incidence matrix of the dc circuit $\mathbf{A}_{fd}$ is used to derive the dc model (Section 2.5.2), and the incidence matrix $\mathbf{A}_d$ is employed to insert the reactive elements (Chapter 3). Since incidence matrix can not be written directly for a graph with self-loop, some modifications are needed in the synthesis procedure.

The notations used here are defined in Chapter 2 and Appendix A. In addition, n_{lp} is used to denote the number of self-loops in graph G_d of a dc circuit.

In order to derive the dc model, the reduced incidence matrix $\mathbf{A}'_{fd}$ is written excluding the self-loop branch(es), and equations involving the dc quantities of the self-loop branch(es) are served as additional constraints. Note that, the prime sign " $'$ " is used to distinguish $\mathbf{A}'_{fd}$ from the conventional reduced incidence matrix $\mathbf{A}_{fd}$.

In order to insert the reactive elements, the matrix $\mathbf{A}'_d[i,j]$ is written as a conventional incidence matrix $\mathbf{A}_d$, except that $\mathbf{A}'_d[i,j] = 2$ if branch j is a self-loop incident at node i.

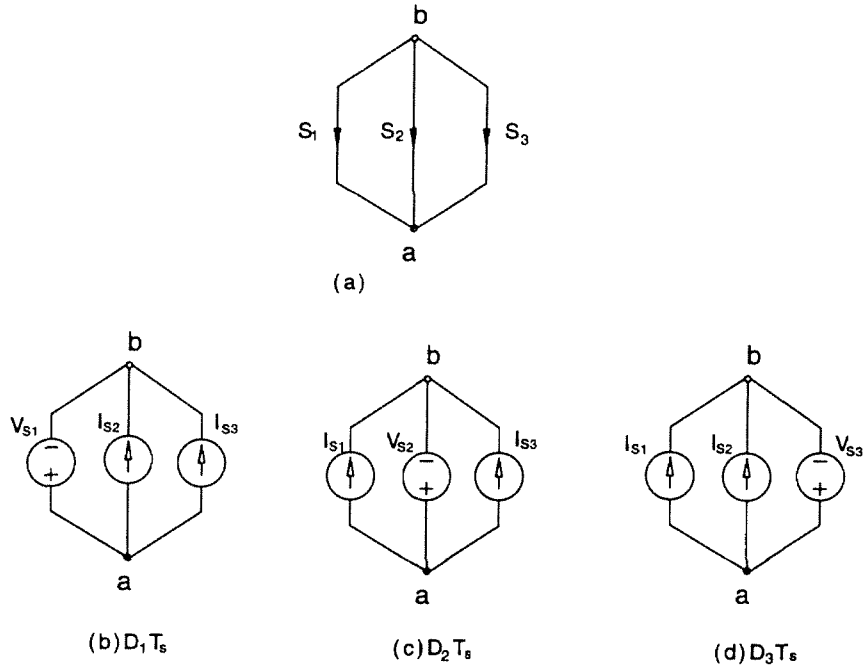


Figure B.1: The ac circuit with reference orientations(a) and its equivalent circuits: During time interval D_1T_s, S_1 is on, and S_2, S_3 are off(b); during time interval D_2T_s, S_2 are on, and S_1, S_3 are off(c); and during time interval D_3T_s, S_3 is on, and S_1, S_2 are off(d).

Consequently, the algorithm of "comprow" function (originally defined in Section 5.3) can be modified to insert the *minimum* inductors and capacitors.

B.2 The Ac Circuit and Balance Equations

The key steps can be illustrated on the following example. Suppose that the ac circuit , together with its equivalent circuits for the three intervals, is given as in Fig. B.1. From the ac circuit topology, $n_a = 1$ and $l_a = 2$.

From the equivalent circuits, $n_{V\_loop} = n_{I\_cutset} = 0$. Therefore, by Eq. (A.10), there is $q = b - l_a = 1$ linearly independent voltage balance equation, which can be derived by integrating v_{s1} in per switching cycle

$$\frac{1}{T_s}\int_0^{T_s} v_{s1}dt = -V_{s1}D_1 - V_{s2}D_2 - V_{s3}D_3 = 0\,, \tag{B.1}$$

which can be rewritten into

$$[\mathbf{1}_q \quad \mathbf{H}_{12}] \begin{bmatrix} V_{s1} \\ V_{s2} \\ V_{s3} \end{bmatrix} = 0\,, \tag{B.2}$$

$$\text{where} \quad \mathbf{H}_{12} = [\,\tfrac{D_2}{D_1} \quad \tfrac{D_3}{D_1}\,]\,. \tag{B.3}$$

The current balance equations are given by the fact $\mathbf{H}_{21} = -\mathbf{H}_{12}^T$

$$\begin{bmatrix} I_{s2} \\ I_{s3} \end{bmatrix} = \begin{bmatrix} \frac{D_2}{D_1} \\ \frac{D_3}{D_1} \end{bmatrix} I_{s1} = -\mathbf{H}_{21} I_{s1}\,, \tag{B.4}$$

which can be rewritten into

$$[\mathbf{H}_{21} \quad \mathbf{1}_{b-q}] \begin{bmatrix} I_{s1} \\ I_{s2} \\ I_{s3} \end{bmatrix} = 0\,. \tag{B.5}$$

B.3 Modification in the Dc Model

Assume the number of input voltage source $N_g = 1$, by Eq. (2.57), in each associated dc circuit, the number of tree branches $n_d = q + N_g = 2$, and Eq. (2.58) is changed to

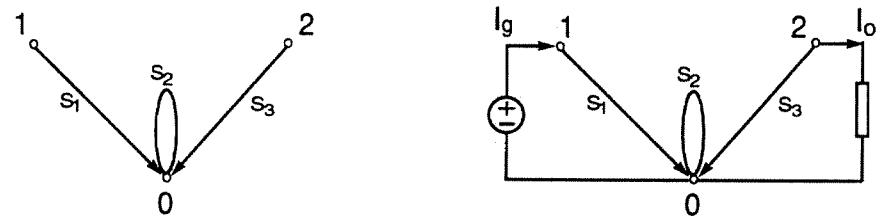
$$l_d + n_{lp} = b - q - N_g\,. \tag{B.6}$$

Here, $l_d + n_{lp} = 1$. Each dc circuit can have at most one self-loop.

Instead of enumerating the possible dc circuit exclusively, we will focus on one dc circuit and show the key modifications in the basic synthesis procedure. The dc circuit is shown in Fig. B.2(a). S_1 branch and S_3 branch are the two tree branches; while S_2 branch is a self-loop.

As mentioned before, the reduced incidence matrix $\mathbf{A}'_{fd}$ can be written for S_1 branch and S_3 branch:

$$\mathbf{A}'_{fd} = \begin{array}{c} \\ 1 \\ 2 \end{array} \begin{array}{c} \begin{array}{cc} S_1 & S_3 \end{array} \\ \begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix} \end{array}, \tag{B.7}$$



(a) dc circuit (b) extended dc circuit

Figure B.2: The dc circuit with a self-loop(a) and extended dc circuit including input and output branches(b).

with the additional constraint

$$V_{s2} = 0\,. \tag{B.8}$$

By use of Eq. (B.8), Eq. (B.2) can be simplified as

$$[\,\mathbf{1}_q \quad \mathbf{H}'_{12}\,]\begin{bmatrix} V_{s1} \\ V_{s3} \end{bmatrix} = [\,1 \quad \tfrac{D_3}{D_1}\,]\begin{bmatrix} V_{s1} \\ V_{s3} \end{bmatrix}. \tag{B.9}$$

It is obvious that matrix $\mathbf{H}'_{12}$ is derived from matrix $\mathbf{H}_{12}$ by removing the column(s) corresponding to the self-loop branch(es) (here, S_2 branch). Also, from the dc circuit, we have

$$\begin{bmatrix} V_{s1} \\ V_{s3} \end{bmatrix} = \mathbf{A}'^{T}_{fd}\begin{bmatrix} V_g \\ V_o \end{bmatrix}. \tag{B.10}$$

Substituting Eq. (B.10) into Eq. (B.9) gives:

$$[\,\mathbf{1}_q \quad \mathbf{H}'_{12}\,]\,\mathbf{A}'^{T}_{fd}\begin{bmatrix} V_g \\ V_o \end{bmatrix} = [\,1 \quad \tfrac{D_3}{D_1}\,]\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}\begin{bmatrix} V_g \\ V_o \end{bmatrix} = 0\,, \tag{B.11}$$

which gives

$$M(D) = \frac{V_o}{V_g} = -\frac{D_1}{D_3}\,. \tag{B.12}$$

By Eqs. (B.10) and (B.12), we have

$$V_{s1} = V_g > 0\,, \tag{B.13}$$

$$V_{s3} = V_o = -\frac{D_1}{D_3} < 0\,. \tag{B.14}$$

As in Eq. (2.40), the incidence matrix A'_{ed} for the extended dc network (Fig. B.2(b)) is:

$$\mathbf{A}'_{ed} = \left[\begin{array}{c|c|c} \mathbf{A}'_{fd} & \mathbf{A}_g & \mathbf{A}_o \end{array} \right] = \begin{array}{c} \\ 1 \\ 2 \end{array} \begin{array}{c} \begin{array}{cccc} I_{s1} & I_{s3} & I_g & I_o \end{array} \\ \left(\begin{array}{cccc} 1 & 0 & -1 & 0 \\ 0 & 1 & 0 & 1 \end{array} \right) \end{array} . \tag{B.15}$$

Again, the column corresponding to the self-loop branch S_2 is removed.

Equations in (B.5) can be divided into two groups:

$$\mathbf{Q}'_a \begin{bmatrix} I_{s1} \\ I_{s3} \end{bmatrix} = [-\tfrac{D_3}{D_1} \quad 1] \begin{bmatrix} I_{s1} \\ I_{s3} \end{bmatrix} = 0 , \tag{B.16}$$

$$I_{s2} = [\tfrac{D_2}{D_1} \quad 0] \begin{bmatrix} I_{s1} \\ I_{s3} \end{bmatrix} . \tag{B.17}$$

By Eq. (2.43), with $\mathbf{A}_{fd}$ replaced by $\mathbf{A}'_{fd}$, and $\mathbf{Q}_a$ replaced by $\mathbf{Q}'_a$, we can obtain

$$I_{s1} = I_g = (\frac{D_1}{D_3})^2 \frac{V_g}{R} > 0 , \tag{B.18}$$

$$I_{s3} = \frac{D_1}{D_3} \frac{V_g}{R} > 0 . \tag{B.19}$$

Then, by Eq. (B.17), we have

$$I_{s2} = \frac{D_1 D_2}{D_3^2} \frac{V_g}{R} > 0 . \tag{B.20}$$

The switches can be implemented as in Section 2.7

$$V_{s1} I_{s1} > 0 : \quad S_1 \text{ is a transistor.} \tag{B.21}$$

$$V_{s2} = 0 : \quad S_2 \text{ is a voltage bidirectional switch.} \tag{B.22}$$

$$V_{s3} I_{s3} < 0 : \quad S_3 \text{ is a diode.} \tag{B.23}$$

B.4 Modification in the Procedure of Inserting Minimum Inductors and Capacitors

In order to insert minimum inductors and capacitors, the matrix representation shall correspond to graph G_d of the dc circuit one-by-one and describe the exact positions of the switch branches. Therefore, we have to include the self-loop branch(es). As mentioned in Section B.1, the matrix $\mathbf{A}'_d[i,j]$ is written as a conventional incidence matrix $\mathbf{A}_d$, except that $\mathbf{A}'_d[i,j] = 2$ if branch j is a self-loop incident at node i. Also, the following rules are added to the "comprow" function in Section 5.3:

7 if $A'_d[x,j] = 2$, $A_a[y,j] = 1 \Longrightarrow r_{xy}[j] = -1$

8 if $A'_d[x,j] = 2$, $A_a[y,j] = -1 \Longrightarrow r_{xy}[j] = 1$

9 if $A'_d[x,j] = 2$, $A_a[y,j] = 0 \Longrightarrow r_{xy}[j] = 2$

$\mathbf{A}_a$ and $\mathbf{A}'_d$ of the dc circuit in Fig. B.2 are

$$A_a = \begin{array}{c} \\ a \\ b \end{array} \begin{array}{c} \begin{array}{ccc} S_1 & S_2 & S_3 \end{array} \\ \begin{pmatrix} -1 & -1 & -1 \\ 1 & 1 & 1 \end{pmatrix} \end{array}, \tag{B.24}$$

$$A_d = \begin{array}{c} \\ 0 \\ 1 \\ 2 \end{array} \begin{array}{c} \begin{array}{ccc} S_1 & S_2 & S_3 \end{array} \\ \begin{pmatrix} -1 & 2 & -1 \\ 1 & 0 & 0 \\ 0 & 0 & 1 \end{pmatrix} \end{array}. \tag{B.25}$$

For the first case, suppose terminal nodes 0, 1, 2 are combined to node a. Rows of A_d are compared with $A_a[a]$ to determine the positions of inductors.

$$\text{comprow}(A_d[0], A_a[a]) = [\,0\ 1\ 0\,] \Longrightarrow A_d[0] \rightarrow \begin{cases} A_d[0] = [\,-1\ \ -1\ \ -1\,] \subset A_a[a] \\ A_d[0'] = [\,0\ 1\ 0\,] \subset A_a[b] \end{cases}$$

$$\text{comprow}(A_d[1], A_a[a]) = [\,1\ 0\ 0\,] \Longrightarrow A_d[1] \rightarrow \begin{cases} A_d[1] = [\,0\ 0\ 0\,] \subset A_a[a] \\ A_d[1'] = [\,1\ 0\ 0\,] \subset A_a[b] \end{cases}$$

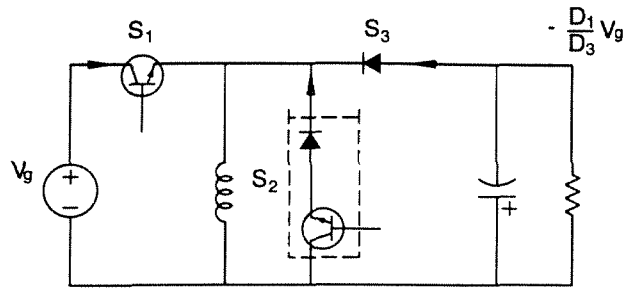


Figure B.3: The generated converter with minimum reactive elements: the 3SN buckboost converter.

$$\text{comprow}(A_d[2], A_a[a]) = [\,0\,0\,1\,] \Longrightarrow A_d[2] \rightarrow \begin{cases} A_d[2] = [\,0\,0\,0\,] \subset A_a[a] \\ A_d[2'] = [\,0\,0\,1\,] \subset A_a[b] \end{cases}$$

The number of inductors needed in this case is 3.

For the second case, suppose that terminal nodes 0, 1, 2 are combined into node b, the corresponding rows of A_d are compared with $A_a[b]$ as follows:

$$\text{comprow}(A_d[0], A_a[b]) = [\,-1\;\;-1\;\;-1\,] \Longrightarrow A_d[0] \rightarrow \begin{cases} A_d[0] = [\,0\,1\,0\,] \subset A_a[b] \\ A_d[0'] = [\,-1\;\;-1\;\;-1\,] \subset A_a[a] \end{cases}$$

$$\text{comprow}(A_d[1], A_a[b]) = [\,0\,0\,0\,] \Longrightarrow A_d[1] \subset A_a[b]$$

$$\text{comprow}(A_d[2], A_a[b]) = [\,0\,0\,0\,] \Longrightarrow A_d[2] \subset A_a[b]$$

Only one inductor is needed in this case. There are four nodes after inserting the inductor. Nodes 0, 1, 2 $\subset$ node b in G_a, and node $0' \subset$ node a in G_a. Since the terminal nodes have been connected by V_g and C_o, no additional capacitor is needed. The converter generated is shown in Fig. B.3. (Fig. 7.4).

This converter is originally proposed in [13], where it was named three-switched-network(3SN) buckboost. The additional switch S_2 provides the second control variable, which can be used for multiple-output and high power factor applications. In multiple-output extensions, each output can be precisely regulated without adding post-regulation circuit, and

consequently improves dynamic response. In ac-dc power conversion, the two independent control variables can provide both high power factor and fast output regulation [4]. If we consider the input and output inductors in the Ćuk converter transform the voltage ports into current ports, the 3SN buckboost converter is actually a dual network of the 3SN Ćuk converter

Appendix C Dc Circuits of Three-Switch Two Switched-Network Converters

As discussed in Chapter 5, a computer program is used to implement the synthesis procedure. The generated dc circuits are classified by their orders. The outputs of the computer program are listed in Table C.1 to Table C.3. Entries in the tables have the following format:

$$\#\ i_1 i_2 i_3.n\ \ a_0\, a_1 /\ b_0\, b_1\ S_1\, S_2\, \tilde{S}_3\ . \tag{C.1}$$

As described in Chapter 5, $(i_1 i_2 i_3.n)$ is the number used to represent positions of three switches in the dc circuit. The conversion ratio is defined as

$$M(D) = \frac{P(D)}{Q(D)} = \frac{a_0 D + a_1}{b_0 D + b_1}\,. \tag{C.2}$$

The switch implementations are given in entries S_1, S_2, and $\tilde{S}_3$, where the type of each switch is denoted by transistor (t); diode (d); current-bidirectional (c); voltage-bidirectional (v); or four-quadrant switch (x).

1:	125.2	0	1/	-1	1	t	d	d	13:	265.2	0	-1/	1	-2	d	t	d
2:	125.3	0	-1/	-1	1	t	d	d	14:	265.4	0	1/	1	0	t	d	t
3:	145.1	-1	0/	-1	1	t	d	d	15:	342.2	-1	1/	0	1	d	t	t
4:	145.4	-1	2/	-1	1	t	d	d	16:	342.3	-1	1/	0	-1	d	t	t
5:	152.2	0	-1/	1	-1	t	d	d	17:	345.1	-1	1/	-1	2	d	t	t
6:	152.3	0	1/	1	-1	t	d	d	18:	345.4	-1	1/	-1	0	d	t	t
7:	154.1	1	-2/	1	-1	t	d	d	19:	354.1	1	-1/	1	0	d	t	t
8:	154.4	1	0/	1	-1	t	d	d	20:	354.4	1	-1/	1	-2	d	t	t
9:	234.2	-1	1/	0	1	t	d	t	21:	462.2	1	0/	0	1	d	t	d
10:	234.4	-1	1/	0	-1	t	d	t	22:	462.4	1	-2/	0	-1	t	d	t
11:	264.2	-1	0/	0	-1	d	t	d	23:	562.2	0	1/	-1	2	d	t	d
12:	264.4	-1	2/	0	1	t	d	t	24:	562.4	0	-1/	-1	0	t	d	t

Table C.1: All second-order dc circuits

1:	125.1	2	-1/	1	-1	t	c	c	13:	256.2	-2	2/	-1	2	d	d	t
2:	145.2	-1	0/	1	-1	c	t	d	14:	264.1	-1	0/	-2	1	v	x	v
3:	152.1	-2	1/	-1	1	t	c	c	15:	265.3	2	-1/	1	0	c	t	c
4:	154.3	1	0/	-1	1	c	t	d	16:	342.1	1	-1/	2	-1	x	v	v
5:	234.1	1	-1/	2	-1	v	x	v	17:	345.3	1	-1/	-1	0	c	d	t
6:	243.1	-1	0/	-2	2	t	t	d	18:	354.2	-1	1/	1	0	c	d	t
7:	245.1	-2	1/	-2	2	c	t	c	19:	451.3	-1	2/	1	0	d	d	t
8:	245.2	0	-1/	2	-2	c	t	d	20:	452.3	0	1/	2	-1	v	x	v
9:	246.1	1	-2/	2	-2	t	t	d	21:	452.4	2	-1/	0	1	t	c	c
10:	251.1	2	-2/	1	0	d	d	t	22:	453.4	1	0/	-1	2	t	t	d
11:	254.1	2	-2/	2	-1	v	x	v	23:	462.1	1	0/	2	-1	v	x	v
12:	254.2	-2	2/	0	1	c	d	t	24:	562.3	-2	1/	-1	0	c	t	c

Table C.2: All fourth-order dc circuits

1:	125.4	-2	1/	1	-1	t	c	c	10:	264.3	3	-2/	2	-1	x x x
2:	145.3	3	-2/	1	-1	c	c	c	11:	265.1	-2	1/	-3	2	x v x
3:	152.4	2	-1/	-1	1	t	c	c	12:	342.4	1	-1/	-2	1	x v v
4:	154.2	-3	2/	-1	1	c	c	c	13:	345.2	1	-1/	3	-2	x v v
5:	234.3	1	-1/	-2	1	v	x	v	14:	354.3	-1	1/	-3	2	x v v
6:	243.2	-1	0/	2	-2	t	t	d	15:	451.4	3	-2/	1	0	c c c
7:	246.2	-3	2/	-2	2	c	c	c	16:	453.3	1	0/	3	-2	v v v
8:	251.2	-2	2/	1	0	d	d	t	17:	462.3	-3	2/	-2	1	x x x
9:	256.1	2	-2/	3	-2	v	v	v	18:	562.1	2	-1/	3	-2	x v x

Table C.3: All sixth-order dc circuits

Appendix D Dc Circuits of Four-Switch Two Switched-Network 2L2C Converters

A computer program is developed to implement the synthesis procedure of four-switch converters discussed in Chapter 6. The generated dc circuits can be classified by their orders: 288 fourth-order (2L2C) dc circuits; 996 sixth-order (3L3C) dc circuits; 526 eighth-order (4L4C) dc circuits; and 54 tenth-order (5L5C) dc circuits. Fourth-order dc circuits are of most practical interests and are listed in Table D.1.

Entries in the Table 6.1 have the following format:

$$\#\ \ i_1 i_2 i_3 i_4.n\ \ a_0\, a_1\, a_2/\ \ b_0\, b_1\, b_2\ \ S_1\, \bar{S}_2\, S_3\, \bar{S}_4\ \ . \tag{D.1}$$

As described in Chapter 6, $(i_1 i_2 i_3 i_4.n)$ is the number used to represent positions of four switches in the dc circuit. The conversion ratio is defined as

$$M(D) = \frac{P(D)}{Q(D)} = \frac{a_0 D^2 + a_1 D + a_2}{b_0 D^2 + b_1 D + b_2}\ . \tag{D.2}$$

The switch implementations are given in entries S_1, $\bar{S}_2$, S_3, and $\bar{S}_4$, where the type of each switch is denoted by transistor (t); diode (d); current-bidirectional (c); voltage-bidirectional (v); or four-quadrant switch (x).

1:	1223.1	0	-1	0 /	1	-2	1	tdtd	55:	1645.7	0	-2	1 /	0	-1	1	cccc
2:	1223.2	0	-1	0 /	-1	2	-1	tdtd	56:	1652.5	0	2	-1 /	0	1	-1	cccc
3:	1223.7	0	1	0 /	-1	2	-1	tdtd	57:	1654.6	0	2	-1 /	0	1	-1	cccc
4:	1225.1	1	-2	0 /	1	-2	1	tdtd	58:	1654.7	0	-2	1 /	0	-1	1	cccx
5:	1225.5	-1	0	0 /	-1	2	-1	tdtv	59:	1655.6	0	2	-1 /	0	1	-1	cccc
6:	1243.3	1	-2	0 /	1	-2	1	tdtd	60:	1655.7	0	-2	1 /	0	-1	1	cccc
7:	1245.2	0	1	0 /	-1	2	-1	tdtd	61:	2312.1	1	0	0 /	0	1	-1	cccc
8:	1246.3	0	0	-1 /	-1	2	-1	tdtd	62:	2312.3	-1	0	0 /	0	1	-1	cccc
9:	1246.6	0	2	-1 /	-1	2	-1	ccxc	63:	2312.7	-1	0	0 /	0	-1	1	tdtd
10:	1251.3	-1	1	-1 /	-1	1	0	tddt	64:	2314.2	0	1	0 /	0	1	-1	cccc
11:	1252.5	-1	2	0 /	-1	1	0	tddt	65:	2315.2	1	0	0 /	1	0	-1	cccc
12:	1254.3	0	0	-1 /	-1	1	0	tddt	66:	2324.1	1	-1	0 /	1	-2	1	cccc
13:	1256.4	1	-3	1 /	0	-1	1	cccc	67:	2324.8	-1	1	0 /	-1	0	1	tddt
14:	1256.5	1	-1	1 /	0	-1	1	tddd	68:	2334.2	-1	1	0 /	-1	1	-1	tddt
15:	1423.3	-1	2	0 /	-1	2	-1	tdtd	69:	2342.1	1	0	0 /	1	0	-1	cccc
16:	1423.6	-1	0	0 /	-1	2	-1	tdvd	70:	2342.8	-1	0	0 /	-1	2	-1	tdvd
17:	1425.1	-1	1	-1 /	-1	2	-1	tdtd	71:	2345.3	-1	0	0 /	0	-1	1	cccc
18:	1426.3	0	0	1 /	1	-2	1	tdtd	72:	2354.2	-1	1	0 /	0	0	-1	tddt
19:	1445.2	0	0	1 /	1	-2	1	tdtd	73:	2364.2	0	1	0 /	1	1	-1	xxxx
20:	1445.6	0	2	-1 /	-1	2	-1	cccx	74:	2364.6	0	1	0 /	1	-1	1	tdtt
21:	1446.1	1	-1	1 /	1	-2	1	tdtd	75:	2365.4	-1	0	0 /	0	0	-1	tdtd
22:	1446.2	-1	3	-1 /	-1	2	-1	cccc	76:	2365.8	-1	0	0 /	0	-2	1	xxxc
23:	1446.7	-1	1	-1 /	-1	2	-1	tdtd	77:	2413.6	1	0	0 /	0	1	-1	ddtd
24:	1451.1	0	0	1 /	-1	1	0	tddt	78:	2413.7	1	-2	0 /	0	-1	1	tttd
25:	1452.1	-1	1	1 /	-1	1	0	tddt	79:	2415.6	0	2	-1 /	0	1	-1	cccc
26:	1453.2	-1	2	0 /	0	-1	1	tdtd	80:	2416.6	1	-1	1 /	0	-1	1	ddtd
27:	1453.7	-1	0	0 /	0	-1	1	tddd	81:	2416.7	1	-1	-1 /	0	1	-1	tttd
28:	1454.7	0	-1	0 /	-1	1	0	tddt	82:	2425.5	1	-2	1 /	0	-1	1	cccc
29:	1456.8	0	-2	1 /	0	-1	1	cccc	83:	2425.6	-1	2	-1 /	0	1	-1	cccc
30:	1521.3	1	-1	1 /	1	-1	0	tddt	84:	2425.8	1	0	-1 /	0	1	-1	cccc
31:	1521.6	1	-3	1 /	1	-1	0	ccxc	85:	2431.6	1	-2	1 /	0	-1	0	dddt
32:	1522.2	-1	0	0 /	0	-1	1	tdtt	86:	2431.7	1	0	-1 /	0	1	0	ttdt
33:	1522.3	-1	2	0 /	0	1	-1	tddd	87:	2433.6	1	-1	0 /	0	0	-1	ttdd
34:	1524.1	0	-2	1 /	0	-1	1	cccc	88:	2433.7	1	-1	0 /	0	0	1	ttdd
35:	1541.2	0	2	-1 /	1	-1	0	ccxc	89:	2435.8	0	1	-1 /	0	2	-1	ccxx
36:	1541.7	0	0	-1 /	1	-1	0	tddt	90:	2436.5	1	0	-1 /	0	0	-1	ttdt
37:	1544.6	1	-1	1 /	0	-1	1	tdtt	91:	2436.8	1	-2	1 /	0	0	1	dddt
38:	1544.7	1	-1	-1 /	0	1	-1	tddd	92:	2445.6	1	1	-1 /	0	1	-1	dtdv
39:	1546.2	0	2	-1 /	0	1	-1	cccc	93:	2445.7	1	-3	1 /	0	-1	1	cccc
40:	1552.1	-1	2	0 /	-1	2	-1	tdtd	94:	2445.8	-1	1	-1 /	0	1	-1	cccc
41:	1553.2	0	1	0 /	1	-2	1	tdtd	95:	2446.8	0	-2	1 /	0	-1	1	cccc
42:	1553.7	0	-1	0 /	1	-2	1	tdtd	96:	2452.5	1	0	-1 /	0	-1	0	dtdt
43:	1554.7	0	0	-1 /	-1	2	-1	tdtd	97:	2452.7	-1	2	-1 /	0	1	0	ttdt
44:	1556.1	1	-1	1 /	1	-2	1	tdtd	98:	2452.8	1	-2	1 /	0	1	0	dtvt
45:	1556.8	1	-3	1 /	1	-2	1	cccc	99:	2454.7	1	-1	0 /	0	1	0	tddt
46:	1622.6	0	-2	1 /	0	-1	1	cccc	100:	2455.6	1	0	-1 /	0	0	-1	dtdd
47:	1622.7	0	2	-1 /	0	1	-1	cccc	101:	2455.7	1	-2	1 /	0	0	1	dttt
48:	1624.5	0	-2	1 /	0	-1	1	cccc	102:	2455.8	-1	2	-1 /	0	2	-1	ccxx
49:	1624.8	0	2	-1 /	0	1	-1	ccxc	103:	2456.7	0	1	-1 /	0	2	-1	tcvv
50:	1625.5	0	-2	1 /	0	-1	1	cccc	104:	2461.6	1	-1	1 /	0	1	0	dddt
51:	1642.8	0	-2	1 /	0	-1	1	ccxc	105:	2461.7	1	-1	-1 /	0	-1	0	ttdt
52:	1644.6	0	2	-1 /	0	1	-1	cccc	106:	2462.5	0	2	-1 /	0	1	0	cccc
53:	1644.7	0	-2	1 /	0	-1	1	cccc	107:	2463.5	1	0	0 /	0	0	1	ddtd
54:	1645.6	0	2	-1 /	0	1	-1	cccx	108:	2463.8	1	-2	0 /	0	0	-1	tttd

109:	2466.6	1	-1	1 /	0	0	1	ddtt	163:	3422.2	0	1	-1 /	1	0	0	dtdd
110:	2466.7	1	-1	-1 /	0	0	-1	ttdd	164:	3422.3	0	-1	1 /	1	-2	0	dttt
111:	2511.6	0	0	1 /	-1	1	0	ddtt	165:	3423.3	-1	1	0 /	-1	1	-1	dttd
112:	2511.7	0	0	-1 /	-1	1	0	ddtt	166:	3423.6	-1	1	0 /	-1	3	-1	vvvv
113:	2513.6	0	1	0 /	-1	2	-1	tttd	167:	3425.1	0	1	-1 /	0	2	-1	xxxc
114:	2513.7	0	-1	0 /	-1	0	1	ddtd	168:	3441.2	-1	2	-1 /	0	-1	0	dtdt
115:	2514.8	0	-2	1 /	0	-1	1	xxcc	169:	3441.7	-1	2	-1 /	0	1	0	dtdt
116:	2516.6	0	0	1 /	-1	0	1	ddtd	170:	3442.1	1	-2	1 /	1	-2	0	dtdt
117:	2516.7	0	0	-1 /	-1	2	-1	tttd	171:	3445.7	1	-2	1 /	0	0	1	dtdt
118:	2524.8	0	-1	1 /	-1	0	1	tddt	172:	3446.2	-1	2	-1 /	-1	1	-1	dtdt
119:	2531.6	0	-1	1 /	-1	0	0	ttdt	173:	3446.7	-1	2	-1 /	-1	3	-1	vvvv
120:	2531.7	0	1	-1 /	-1	2	0	dddt	174:	3453.2	-1	1	0 /	0	-2	1	vvtv
121:	2534.6	0	-1	1 /	0	-2	1	xxxx	175:	3453.7	-1	1	0 /	0	0	1	dttd
122:	2536.5	0	1	-1 /	-1	1	-1	ttdt	176:	3455.6	0	1	-1 /	-1	1	-1	dtdd
123:	2536.8	0	-1	1 /	-1	1	1	dddt	177:	3455.7	0	-1	1 /	-1	1	1	dttt
124:	2542.5	0	1	0 /	-1	0	1	tdtd	178:	3521.3	1	-2	1 /	1	-2	0	dtdt
125:	2542.7	0	-1	0 /	1	-2	1	ddtd	179:	3521.6	1	-2	1 /	1	0	0	dtvt
126:	2542.8	0	-1	0 /	-1	2	-1	tdvd	180:	3524.1	1	-2	1 /	1	-1	1	dtdt
127:	2544.6	0	0	1 /	-1	0	1	tdtt	181:	3526.4	-1	2	-1 /	0	0	-1	dtdt
128:	2544.7	0	0	-1 /	-1	2	-1	tddd	182:	3541.2	0	1	-1 /	1	-2	0	dtdt
129:	2544.8	0	-2	1 /	1	-2	1	xxcc	183:	3541.7	0	1	-1 /	1	0	0	dttt
130:	2545.7	0	-1	0 /	-1	1	0	cccc	184:	3542.1	1	-1	0 /	1	-1	-1	dttd
131:	2545.8	0	-1	0 /	1	-1	0	cccc	185:	3543.1	1	-1	0 /	0	0	-1	dttd
132:	2546.8	0	-2	1 /	0	-1	1	xxcc	186:	3545.7	1	-1	0 /	0	1	0	dttd
133:	2554.6	0	-1	1 /	-1	-1	1	xxxx	187:	3554.2	-1	2	-1 /	0	0	-1	dtdt
134:	2554.7	0	1	-1 /	-1	3	-1	xxxx	188:	3554.6	1	-2	1 /	0	-2	1	xxxc
135:	2554.8	0	-1	1 /	1	-1	1	dddt	189:	3556.1	1	-2	1 /	1	-3	1	vvvv
136:	2556.7	0	1	-1 /	0	2	-1	vxvv	190:	3556.2	-1	2	-1 /	-1	1	-1	dtdt
137:	2561.6	0	0	1 /	-1	2	0	dddt	191:	3556.8	1	-2	1 /	1	-1	1	dtdt
138:	2561.7	0	0	-1 /	-1	0	0	ttdt	192:	3622.2	0	1	-1 /	0	2	-1	xxxx
139:	2562.7	0	-1	0 /	0	-2	1	xxxx	193:	3622.3	0	-1	1 /	0	-2	1	xxxx
140:	2563.5	0	1	0 /	-1	1	1	ddtd	194:	3624.1	0	1	-1 /	0	2	-1	xxxx
141:	2563.8	0	-1	0 /	-1	1	-1	tttd	195:	3625.1	0	1	-1 /	0	2	-1	xxxc
142:	2566.6	0	0	1 /	-1	1	1	ddtt	196:	3625.4	0	-1	1 /	0	-2	1	xxcx
143:	2566.7	0	0	-1 /	-1	1	-1	ttdd	197:	3642.1	0	-1	1 /	0	-2	1	xxxx
144:	2612.3	-1	-1	1 /	0	-1	1	cccc	198:	3644.2	0	-1	1 /	0	-2	1	xxxx
145:	2612.7	-1	1	-1 /	0	1	-1	cccc	199:	3644.3	0	1	-1 /	0	2	-1	xxxx
146:	2614.6	0	2	-1 /	0	1	-1	cccc	200:	3645.2	0	-1	1 /	0	-2	1	xxcx
147:	2625.5	1	-2	1 /	0	-1	1	cccc	201:	3645.3	0	1	-1 /	0	2	-1	xxxc
148:	2632.3	0	-1	1 /	1	-1	1	dtdt	202:	3652.4	0	1	-1 /	0	2	-1	xxcx
149:	2632.7	0	1	-1 /	1	1	-1	xxxx	203:	3654.2	0	-1	1 /	0	-2	1	xxxc
150:	2635.2	0	-1	1 /	0	-2	1	xxxc	204:	3654.3	0	1	-1 /	0	2	-1	xxcx
151:	2642.1	0	0	1 /	-1	0	1	tdtd	205:	3655.2	0	-1	1 /	0	-2	1	xxxx
152:	2644.2	-1	1	1 /	-1	0	1	tdtt	206:	3655.3	0	1	-1 /	0	2	-1	xxxx
153:	2644.3	-1	1	-1 /	-1	2	-1	tddd	207:	4415.3	0	2	-1 /	0	1	-1	cccc
154:	2645.7	0	-2	1 /	0	-1	1	cccc	208:	4416.1	0	-2	1 /	0	-1	1	cccc
155:	2652.5	1	0	-1 /	0	0	-1	dtdt	209:	4425.1	0	0	-1 /	0	1	-1	cccc
156:	2654.3	0	1	-1 /	0	2	-1	xxcx	210:	4425.3	0	2	-1 /	0	1	-1	cccc
157:	2655.6	1	0	-1 /	1	-1	-1	dtdd	211:	4425.4	0	0	1 /	0	-1	1	cccc
158:	2655.7	1	-2	1 /	1	-1	1	dttt	212:	4426.4	0	2	-1 /	0	1	-1	cccc
159:	2664.2	0	0	1 /	1	-1	1	tddt	213:	4435.1	0	1	-1 /	0	2	-1	ccxx
160:	2664.6	0	2	-1 /	1	1	-1	xxxx	214:	4451.2	0	2	-1 /	0	1	0	cccc
161:	2665.4	-1	-1	1 /	0	-2	1	xxxc	215:	4452.2	0	2	-1 /	0	1	0	cccc
162:	2665.8	-1	1	-1 /	0	0	-1	dttd	216:	4461.1	0	-2	1 /	0	-1	0	cccc

217:	4462.4	0 2 -1 /	0 1 0	cccc
218:	4511.2	-1 1 -1 /	-1 1 0	ddtt
219:	4511.3	-1 1 1 /	-1 1 0	ddtt
220:	4512.4	0 1 0 /	0 -1 1	vvtd
221:	4513.2	-1 0 0 /	-1 0 1	ddtd
222:	4513.3	-1 2 0 /	-1 2 -1	tttd
223:	4514.1	0 -2 1 /	0 -1 1	cccc
224:	4516.2	-1 1 -1 /	-1 2 -1	tttd
225:	4516.3	-1 1 1 /	-1 0 1	ddtd
226:	4522.2	-1 0 0 /	-1 0 1	tdtt
227:	4522.3	-1 2 0 /	-1 2 -1	tddd
228:	4522.4	1 0 0 /	1 -2 1	vvtd
229:	4523.4	0 1 0 /	0 -1 1	vvtd
230:	4524.1	-1 -1 1 /	-1 0 1	cccc
231:	4524.3	1 -1 1 /	1 -2 1	ddtd
232:	4524.4	-1 3 -1 /	-1 2 -1	ccxc
233:	4525.4	-1 2 0 /	-1 1 0	cccc
234:	4526.4	0 2 -1 /	0 1 -1	cccc
235:	4531.2	-1 2 -1 /	-1 2 0	dddt
236:	4531.3	-1 0 1 /	-1 0 0	ttdt
237:	4533.2	-1 1 0 /	-1 1 1	ttdd
238:	4533.3	-1 1 0 /	-1 1 -1	ttdd
239:	4534.3	0 -1 1 /	0 -2 1	xxxx
240:	4536.1	-1 0 1 /	-1 1 1	ttdt
241:	4536.4	-1 2 -1 /	-1 1 -1	dddt
242:	4542.4	-1 1 0 /	-1 0 1	dttd
243:	4551.2	0 2 -1 /	0 1 0	cccc
244:	4552.1	-1 2 0 /	-1 3 -1	xxxx
245:	4552.2	1 0 0 /	1 -1 1	tttd
246:	4552.4	-1 0 0 /	-1 -1 1	xxxx
247:	4553.1	0 1 0 /	0 2 -1	vxvv
248:	4561.2	-1 1 -1 /	-1 0 0	ttdt
249:	4561.3	-1 1 1 /	-1 2 0	dddt
250:	4562.2	0 -1 0 /	0 -2 1	xxxx
251:	4563.1	-1 0 0 /	-1 1 -1	ddtd
252:	4563.4	-1 2 0 /	-1 1 1	tttd
253:	4614.1	-1 1 -1 /	0 1 -1	cccc
254:	4614.3	1 1 -1 /	0 1 -1	dtdt
255:	4614.7	1 -1 1 /	0 -1 1	tdtd
256:	4615.1	0 0 -1 /	1 0 -1	cccc
257:	4624.1	0 0 -1 /	1 0 -1	cccc
258:	4624.8	0 2 -1 /	-1 2 -1	ccxc
259:	4625.4	1 -1 1 /	0 -1 1	cccc
260:	4632.2	1 0 -1 /	1 1 -1	xxxx
261:	4632.6	1 -2 1 /	1 -1 1	dtdd
262:	4635.3	1 0 -1 /	0 0 -1	dtdt
263:	4635.7	1 -2 1 /	0 -2 1	xxxc
264:	4642.8	0 -1 1 /	-1 0 1	dttd
265:	4652.4	1 -1 -1 /	0 0 -1	tddt
266:	4662.2	0 0 -1 /	-1 1 -1	tddt
267:	5514.1	0 -2 1 /	0 -1 1	cccc
268:	5516.4	0 2 -1 /	0 1 -1	cccc
269:	5524.3	0 -1 1 /	0 -2 1	ccxx
270:	5534.3	0 -1 1 /	0 -2 1	ccxx
271:	5541.1	0 -2 1 /	0 -1 0	cccc
272:	5542.2	0 -1 0 /	0 -2 1	ccxx
273:	5561.4	0 2 -1 /	0 1 0	cccc
274:	5562.2	0 -1 0 /	0 -2 1	ccxx
275:	5612.2	-1 1 -1 /	-1 2 -1	cccc
276:	5612.6	-1 -1 1 /	-1 0 1	cccc
277:	5614.3	0 2 -1 /	-1 2 -1	ccxx
278:	5614.7	0 0 1 /	-1 0 1	tdtd
279:	5624.8	0 1 -1 /	-1 1 -1	dtdt
280:	5625.4	1 -2 1 /	0 -2 1	xxcx
281:	5625.5	-1 0 1 /	0 0 1	dtdt
282:	5634.5	-1 0 1 /	0 0 1	dtdt
283:	5635.3	0 1 -1 /	-1 1 -1	cccc
284:	5635.5	0 -1 1 /	1 -1 1	dtdt
285:	5635.7	0 -1 1 /	-1 -1 1	xxxx
286:	5642.8	0 0 1 /	-1 1 1	dttd
287:	5652.4	1 0 -1 /	0 1 -1	cccc
288:	5662.8	1 -1 1 /	0 0 1	dttd

Table D.1: Fourth-order dc circuits

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