Deterministic Jitter in Broadband Communication

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Abstract

The past decade has witnessed a drastic change in the design of high-speed serial links. While Silicon fabrication technology has produced smaller, faster transistors, transmission line interconnects between chips and through backplanes have not substantially improved and have a practical bandwidth of around 3GHz. As serial link speeds increase, new techniques must be introduced to overcome the bandwidth limitation and maintain digital signal integrity. This thesis studies timing issues pertaining to bandwidth-limited interconnects. Jitter is defined as the timing uncertainty at a threshold used to detect the digital signal. Reliable digital communication requires minimizing jitter.

The analysis and modeling presented here focuses on two types of deterministic jitter. First, dispersion of the digital signal in a bandwidth-limited channel creates data-dependent jitter. Our analysis links data sequences to unique timing deviations through the channel response and is shown for general linear time-invariant systems. A Markov model is constructed to study the impact of jitter on the operation of the serial link and provide insight in circuit performance. Second, an analysis of bounded-uncorrected jitter resulting from crosstalk induced in parallel serial links is presented.

Timing equalization is introduced to improve the signal integrity of high-speed links. The analysis of deterministic jitter leads to novel techniques for compensating the timing ambiguity in the received data. Data-dependent jitter equalization is discussed at both the receiver, where it complements the operation of clock and data recovery circuits, and as a phase pre-emphasis technique. Crosstalk-induced, bounded-uncorrected jitter can also be compensated. By detecting electromagnetic modes between neighboring serial links, a transmitter or receiver anticipates the timing deviation that has occurred along the transmission line.

Finally, we discuss a new circuit technique for submillimeter integrated circuits. Demands of wireless communication and the high speed of Silicon Germanium transistors provide opportunities for unique radio architectures for submillimeter integrated circuits. Scalable, fully-integrated phased arrays control a radiated beam pattern electronically through tiling multiple chips. Coupled-oscillator arrays are used for the first time to subharmonically injection-lock across a chip or between multiple chips to provide phase coherence across an array.

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Chapter 1

Introduction

The rapid expansion of communication technologies is profoundly impacting our society. In the past hundred years, information exchange, once limited to letters and telegraphs, moves near the speed of light and is accessible to the general public. With estimates of the number of households in the United States subscribing to cable and direct-subscriber lines (DSL) data services topping 25 million in 2005, broadband access is indispensable [1]. Our society, once satisfied with telephony, creates more information and services to take advantage of the growing information capacity. This trend drives the demand for data communication, which has superseded the original role of telephony networks for voice communication. Business and consumer demands encourage future investment in communication technologies. Integrated circuit technologies for high-speed communication are central to the development of new networks.

Since the development of Arpanet, the first computer network for military applications in the 1960s, high-speed data communication technologies have proliferated throughout society. Several factors have contributed to this proliferation. First, computers became available to consumers and not just to businesses. This established the requisite infrastructure within which low-cost modems and, later, ethernet cards would provide network access to home users. Second, academic institutions, businesses, and governments discovered the advantages of organizing information on computer servers. Ethernet and TCP/IP standards provided seamless interoperability between these information servers and home internet users. Finally, telephone companies as well as cable companies have competed to lower the cost of equipment, routing, and data transmission, making network connections affordable to home users.

A major force behind this movement has been cost. Silicon integrated circuits (ICs) have been tremendously successful as a fabrication technology for consumer electronics. Both computers and network equipment have become affordable due to the high yield, volume, and low cost of Silicon manufacturing processes. In this thesis, high-speed communication ICs, the hardware that makes networking and information servers viable, is studied.

Modern high-speed communication is grouped primarily among wireless and wireline channels. Wireless communication is currently comprised of cellular communication for mobile telephony and broadband data communications using standards such as IEEE 802.11b/g [2]. Wireless data communications are expected to grow through the deployment of WiFi networks and data services over cellular communication. While the focus of recent investment and consumer demand has accelerated the development of wireless infrastructure, the workhorse of data communication remains wireline technology. Wireline networking is comprised of local area networks (LAN), storage area networks (SAN), wide-area networks (WAN), and long-haul communication. These divisions are focused on the distance and speed of the network.

Wireline communications are typically designed to support the highest data rates over a physical channel. Optical fiber is the backbone of telecommunications networks around the world. Optical fiber features extremely low loss over great distances and large bandwidths. Protocols such as the Synchronous Optical Network (SONET) have benchmarked the progression of optical communication networks [3]. Fiber-to-the-home (FTTH) technologies extend this broadband access directly to the consumer, providing data rates over 1Gb/s [4]. Current barriers for FTTH are economic, requiring bundling data, voice, and video communication for consumers [5]. However, hardware costs, both optical and electrical, account for a fifth of the installation cost [4].

Computing and communication circuit design have traditionally been treated separately, but the growth of communication networks places new demands on

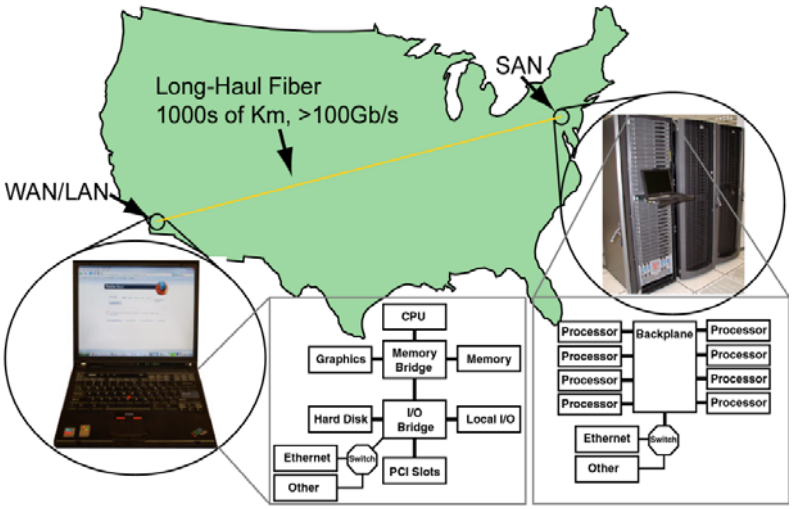

Figure 1.1 An overview of the applications for high-speed communication circuits. Server photo courtesy of Caltech's Center for Advanced Computing Research.

computational systems in SANs. Computer networking has stimulated data rate demands in serial communication. Several different communication demands exist in computers. First, the processor must communicate with peripheral RAM and other chips through the memory bus as shown in Figure 1.1. As processor speeds have increased dramatically over the past decades, more emphasis has been placed on the data rates of the serial link. Chip-to-chip communications require data rates of nearly 1Gb/s over several centimeters. While the serial link transceiver circuits have kept pace with the increase in processor speed, the physical interconnect between the devices has changed very little. New bus standards such as peripheral component interconnect (PCI) express have been adopted to meet future bus needs in personal computers [8].

Larger computers such as servers and supercomputers consist of hundreds of parallel processors. Blade cards have become prominent in server applications [6]. Midplane and backplane serial communication connects the processors and cards in a rack mounted box [7]. While these servers currently operate at 2.5Gb/s, backplane rates of nearly 10Gb/s over distances of a meter are anticipated. Backplane interconnects have become the focus of serial link research, as higher speeds are needed. However, signal attenuation, dispersion, and connector reflections limits the bandwidth of these links. Recent protocols

that support high-speed backplane communication such as InfiniBand, Gigabit Ethernet, and FibreChannel have been adapted to consider the signal integrity issues in high-speed backplanes [9][10].

This thesis studies how timing issues, specifically deterministic jitter, can be overcome so as not to impede high-speed wireline communication. Opportunities for developing more sophisticated equalization for bandwidth-limited channels have not been fully realized. In particular, understanding the generation of jitter in serial links provides means for predicting the signal integrity problems that occur in wireline channels. Through the analysis and modeling of jitter in bandwidth-limited interconnects, I develop methods for determining bit-error rate (BER) performance as well as new types of equalization to overcome bandwidth limitations.

1.1 Background: The Evolution of Serial Communications

The role of serial communication is to transmit and receive information over a channel. High-speed serial links are the input/output (I/O) interconnect between two chips. Because of space and size constraints, the number of parallel serial links is often limited, and the goal of circuit designers is to increase the speed at which each link operates. The basic communication link is demonstrated in Figure 1.2. A transmitter takes several parallel data paths and multiplexes them into a single serial data stream. The

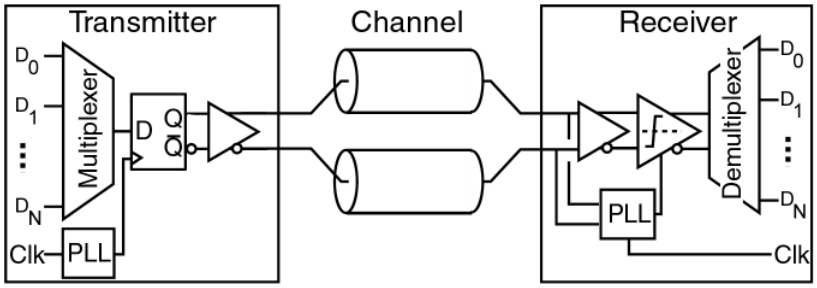

Figure 1.2 A basic communication link demonstrating the transmitter and receiver functions.

transmit phase-locked loop (PLL) re-times each bit and drives them electrically or optically over a fixed channel. At the receiver, two operations must be performed. First, the signal must be amplified and detected to determine the appropriate transmitted bit. Second, a receiver PLL must generate a sampling clock to determine when the bit detection occurs. The serial stream is then demultiplexed into parallel data.

In the past, the channel environment could be, for the most part, ignored. The loss and dispersion introduced by electrical interconnects was negligible because the bandwidth far exceeded the data rates and, consequently, the data rates of high-speed links were limited primarily by the speed of devices in a standard Silicon technology.

Early serial interfaces provided noise immunity through current integration [11]. As rate demands increased, multiplexing was introduced to create a serial stream [12]. The burden of these architectures was generating low jitter clock phases. These phases oversampled the received data and detected the transition boundaries. More attention was concentrated on the problems of timing jitter and circuits that produced low jitter while providing time delay [13].

Delay-locked loop (DLL) circuits have favorable jitter attenuation properties [14] and were enhanced using injection locking [15]. Interest in DLLs was spurred by limitations of PLLs used for clock and data recovery (CDR) of optical signals. Jitter was reduced through combining DLL and PLL circuits [16]. CDR designs for optical communication were steadily taking advantage of new processes to reach the SONET rates [17]-[19].

Oversampling receivers migrated into new circuit technologies to reach the bandwidth limitations (4Gb/s) of process technology [20]. However, the electrical interconnect in these systems is not ideal and has a limited bandwidth. Once link speeds increased beyond 3Gb/s, circuit designers were forced to consider new techniques for managing signal integrity in bandwidth-limited channels. Equalization was introduced to serial links both in the transmitter and receiver to compensate for data degradation due to attenuation and dispersion.

Pre-emphasis equalization amplifies the high-frequency signal components that are attenuated by the channel. As link speeds became channel-limited, several integrated circuit designs were proposed that introduced one- and two- tap amplitude pre-emphasis [21]-[23]. However, amplitude pre-emphasis was limited by the need for some adaptation for the channel behavior. Recent work has demonstrated backchannel adaptation through a low frequency signal transmitted over the common mode of the differential lines [24]. This common mode technique is also referred to as “phantom” mode communication and was proposed to reduce the wiring constraints of serial links [25].

In the receiver, new schemes implementing decision feedback equalization (DFE) were introduced [26]. These schemes were adapted from early work on echo cancellation caused by dispersion in optical fiber communications [27]. DFE designs have expanded to allow for compensation over several bit periods and included adaptation schemes [28][29].

Additionally, the data rate demand has increased interest in signaling beyond two-level pulse amplitude modulations schemes (2-PAM). In particular, the use of quaternary modulation such as four-level pulse amplitude modulation (4-PAM) was demonstrated in [30][31]. These schemes sacrifice signal-to-noise ratio in integrated environments where voltage scaling occurs with process migration. However, 4-PAM can achieve twice the data rate with roughly the same bandwidth. A general description of serial link design for channel-limitations and M-PAM communication is provided by Stojanovic [33].

The past decade has seen new approaches to the characterization of jitter through measurement techniques. Early studies of jitter focused on digital transmission through long haul fiber-optic networks [34][35]. Additionally, jitter became critical in the performance of high-speed sampling circuits, in particular analog-to-digital conversion [36]. In communication testing, the relationship between behavioral models of jitter and measurement needed to be established accurately for low BER. Li and Wilstrup discussed tail fitting the BER function to establish deterministic and random sources of jitter [37].

Subsequently, they established limitations on the accuracy of this jitter separation [38][39]. The result of these new modeling efforts has been a jitter standard for FibreChannel [40]. Currently, modeling work has attempted to refine the analysis of sources of deterministic jitter [41] as well as to link jitter to the performance of frequency references [42]-[45].

Advancing data rates requires attention to equalization techniques to handle the bandwidth limitations of the channel. In this thesis, the effect of bandwidth limitation on deterministic jitter characteristics is modeled and analyzed. The development of equalization techniques for deterministic jitter promises to enhance the signal quality of the communication over these channels while offering low power implementations.

1.2 Organization

This thesis describes timing jitter in high-speed communication links. In Chapter 2 signal integrity is discussed in the context of bandwidth limited systems. Bandwidth limitation introduces strong deterministic impairments to the data sequence that are compounded by random noise sources. The predicted bit errors due to timing and voltage errors are demonstrated, and the sources of random jitter in modern high-speed links are discussed. Additionally, the relationship between the deterministic jitter and the performance of high-speed PLLs is discussed.

In Chapter 3 deterministic timing deviations correlated to the data sequence [data-dependent jitter (DDJ)] are analyzed, and expressions for the threshold crossing times are derived for several different types of linear time-invariant (LTI) channels. Additionally, DDJ in quaternary signaling is discussed. The general expression of the threshold crossing times is useful for introducing a Markov model for the progression of the threshold crossing times and calculating time domain behavior such as cycle-to-cycle jitter. The power spectral density of the DDJ is calculated using the Markov model.

Chapter 4 introduces a novel technique for compensating the data-dependent jitter introduced in bandwidth-limited channels. This equalizer leverages the unique relationship between the data sequence and the threshold crossing time to reposition the transition edge. Two circuits are presented in this chapter to correct DDJ. The first is built into a clock and data recovery circuit. The second compensates rising and falling edges individually in situations where the signal response is not linear.

The use of data-dependent jitter equalizers is not restricted to the receiver, and Chapter 5 discusses the design and implementation of a phase pre-emphasis scheme that can augment the performance of amplitude pre-emphasis. Phase pre-emphasis introduces a timing deviation to the data edge before the signal is transmitted, with the assumption that the channel response will correct the timing. This technique is particularly interesting because phase pre-emphasis is not subject to error propagation in the receiver and does not require large power consumption.

In Chapter 6 the role of crosstalk on jitter is introduced. Crosstalk couples unwanted energy between adjacent serial links. The relationship between crosstalk and deterministic signal jitter is discussed and compared for different data modulation schemes. Chapter 7 employs the derived relationship between the crosstalk-induced jitter and the occurrence of signal transitions on neighboring lines to remove this source of jitter. Hardware results are presented for a complementary metal-oxide semiconductor (CMOS) process, and the testing demonstrates that a crosstalk-induced jitter equalizer can drastically improve the timing margins of the data eye.

Finally, Chapter 8 introduces a new architecture for submillimeter integrated radios. The technology scaling in Silicon Germanium (SiGe) has pushed device speeds into submillimeter frequencies. Consequently, the integration of entire radios including signal generation, a power amplifier, and an antenna is possible on a single chip. Furthermore, the small wavelengths at submillimeter frequencies provides a unique opportunity to integrate several radios on a single die and create a phased array antenna. This chapter

discusses the frequency generation and distribution problems for fully integrated submillimeter phased array transmitters. The design uses a coupled oscillator array which places oscillators at each element of the array. To generate a coherent phase, each oscillator is locked to a neighboring oscillator. Driving the array with a low-phase noise external master reduces the phase noise across the entire array. Hardware results in a SiGe process demonstrate the performance of these oscillator arrays.

Chapter 2 Signal Integrity in Broadband Communications

Signal integrity is a metric for discussing the achievable bit error rate (BER) of a communication link. This chapter discusses signal integrity and the impact of timing jitter. The architecture of a broadband communication system involves three principle components as illustrated in Figure 2.1. The first component is a transmitter that generates a data signal. The signal at the output of the transmitter is denoted $x(t)$. Typically, the transmitted digital signal consists of two amplitude levels, generally called two-level pulse amplitude modulation (2-PAM), representing the one or zero bit, a_k. When the bits are transmitted for one bit period, 2-PAM is referred to as a non-return-to-zero (NRZ) signal. The second component is a communication channel over which the data propagates. This channel can be wireless or wireline. For broadband signal transmission over wireline channels, the channel bandwidth has the low-pass response, $G(f)$, shown in the figure. After the signal has passed through the channel, it is distorted by the channel and is denoted $y(t)$. Finally, the third component is a receiver that detects the data signal and recovers the transmitted bits. Each block is designed to operate in a particular channel

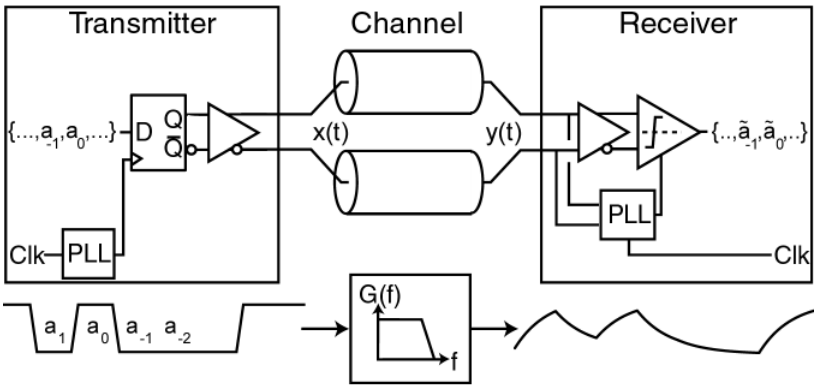

Figure 2.1 A basic communication link demonstrating the transmission of a 2-PAM signal over a broadband channel and the receiver recovery of the signal.

environment. In this chapter we describe the operation and jitter generation of each of these blocks.

2.1 Shannon's Theorem

Claude Shannon formalized the ultimate limit of capacity in communication channels in his seminal paper [46]. The implications of this work directed communication theory and formed the foundations of information theory by establishing a relationship between signal-to-noise ratio (SNR), channel bandwidth, and communication capacity. The Shannon limit is given by the channel capacity, *C*, and is

$$C = BW \cdot log_2\left(1 + \frac{P_{signal}}{P_{noise}}\right), \tag{2.1}$$

where *BW* describes the bandwidth of the channel, P_{signal} is the signal power, and P_{noise} is the noise power. The channel capacity in (2.1) assumes that the communication channel is linear and that the noise is additive. The ratio of the signal and noise power is referred to as the signal-to-noise ratio (SNR). For large SNR, the capacity is much greater than the channel bandwidth.

In practice, designing high-speed circuits that operate at data rates much greater than the channel bandwidth is difficult. Shannon's Theorem demonstrates the communication capacity, while circuit designers must develop clever methods to realize this capacity. Examining conventional digital communication schemes builds appreciation of these challenges.

2.1.1 Signal Power

For NRZ signals, each binary symbol is transmitted over a bit period, *T*. For an uncoded data sequence, each symbol is uncorrelated to adjacent symbols. Therefore, the data symbol, a_k, satisfies the convolution property, $a_n \otimes a_k = \delta(n-k)$ [47]. Consequently, the autocorrelation of the NRZ signal is expressed as

$$R_{xx}(\tau) = V_s^2 \begin{cases} 1 - \dfrac{|\tau|}{T} & T > \tau \geq -T \\ 0 & \tau \geq T,\ \tau < -T \end{cases}, \tag{2.2}$$

where V_s is the signal swing. The power spectral density (PSD) for this autocorrelation is calculated with the Fourier transform:

$$S_{xx}(f) = \Im\{R_{xx}(\tau)\} = V_s^2 T\left(\frac{\sin(\pi fT)}{\pi fT}\right)^2 \qquad \left[\frac{V^2}{Hz}\right]. \tag{2.3}$$

In Figure 2.2, the PSD of (2.3) is illustrated. The plot of $S_{xx}(f)$ indicates that the power is concentrated at frequencies below $1/T$. The total power that reaches the receiver is limited by the low-pass bandwidth of the channel. For a low-pass transfer function, $G(f)$, with bandwidth, BW,

$$P_{signal} = 2\int_0^{\infty} S_{xx}(f)|G(f)|^2 df \qquad [V^2]. \tag{2.4}$$

This result gives the power of the signal at the receiver required to determine (2.1).

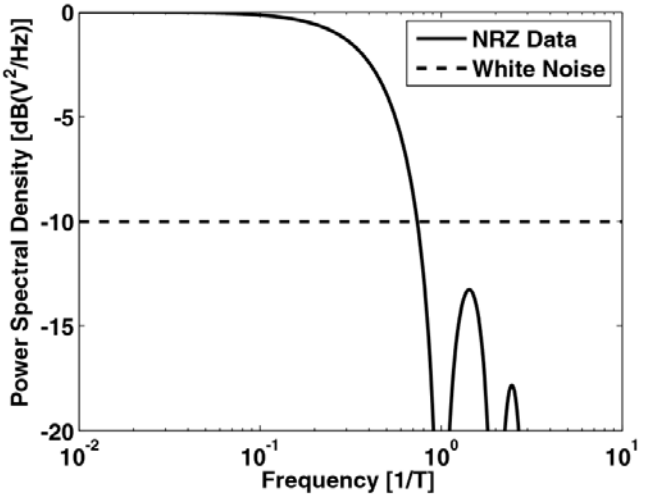

Figure 2.2 Power spectral density of the NRZ data sequence and white noise.

2.1.2 Noise Power

Noise is inevitable in any electronic system and exhibits a different PSD than the signal. For an additive white noise source, the autocorrelation of the noise is

$$R_{nn}(\tau) = \frac{N_o}{2}\delta(\tau), \tag{2.5}$$

demonstrating that the noise is uncorrelated. Therefore, the noise PSD is

$$S_{nn}(f) = \frac{N_o}{2} \qquad \left[\frac{V^2}{Hz}\right]. \tag{2.6}$$

The noise PSD is superimposed with the signal PSD in Figure 2.2. The noise power is calculated by integrating (2.6):

$$P_{noise} = N_o\int_0^\infty |G(f)|^2 df \qquad [V^2]. \tag{2.7}$$

Returning to (2.1), the signal and noise power are functions of the bandwidth. The integrated power of the noise increases linearly with bandwidth while the integrated signal power in (2.4) falls off. Finally, the SNR is

$$SNR = \frac{P_{signal}}{P_{noise}} = \frac{V_s^2}{N_o} \cdot \frac{2T\int_0^\infty \left(\frac{\sin(\pi fT)}{\pi fT}\right)^2 |G(f)|^2 df}{\int_0^\infty |G(f)|^2 df}. \tag{2.8}$$

The SNR can be evaluated with a model of the communication channel transfer function.

2.1.3 Bandwidth

The bandwidth directly improves the capacity in (2.1) and affects the SNR in (2.8). Bandwidth is useful for limiting noise in the link, but, more recently, data rates in high-speed serial links are restricted by the bandwidth. While the bandwidth in optical communication systems is tailored to maximize (2.8), bandwidth in serial links is fixed by frequency dependent attenuation and reflections in the transmission line and connectors.In

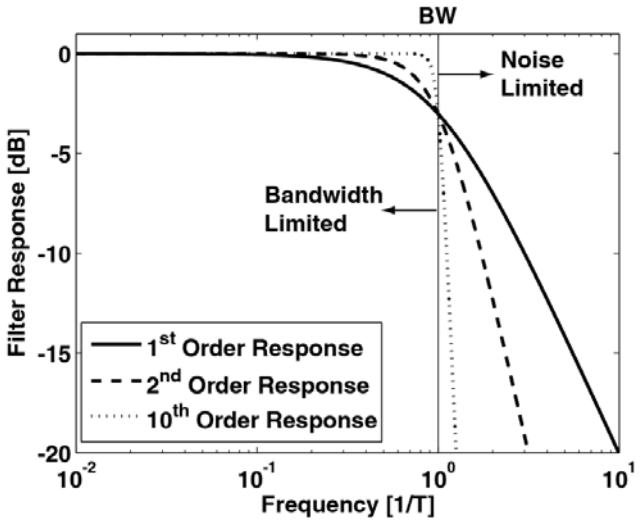

Figure 2.3 Bandwidth for butterworth filters with different roll-offs.

Figure 2.3, ideal low-pass responses are plotted. The higher-order filters approach the limit of the "brick-wall" filter, ideal for filtering the noise PSD demonstrated in Figure 2.2. Once the signal PSD falls below the noise PSD, the response should attenuate the noise to maintain the SNR. In optical receivers, the bandwidth of the receiver is often chosen to be around 70% of the bit rate [53]. Higher bandwidths become noise-limited, while lower bandwidths reduce the signal energy. In the following sections, bandwidth limitations of high-speed optical and electrical channels are reviewed.

2.1.3.1 High-Speed Serial Links

Currently, data rates in high-speed serial links are impeded by bandwidth-limitation. High-speed serial links are designed with transmission line channels that connect the input/output (I/O) between different chips. A shielded cable is a simple serial link. In servers and parallel computers, a backplane, shown in Figure 2.4, provides I/O between different boards. Two peripheral boards are connected to the backplane through high-speed connectors. The differential transmission line starts at one chip and is routed through the peripheral boards and backplane. The transmission lines have vias created by fabricating the transmission lines from one layer to another layer. Thus, the backplane link

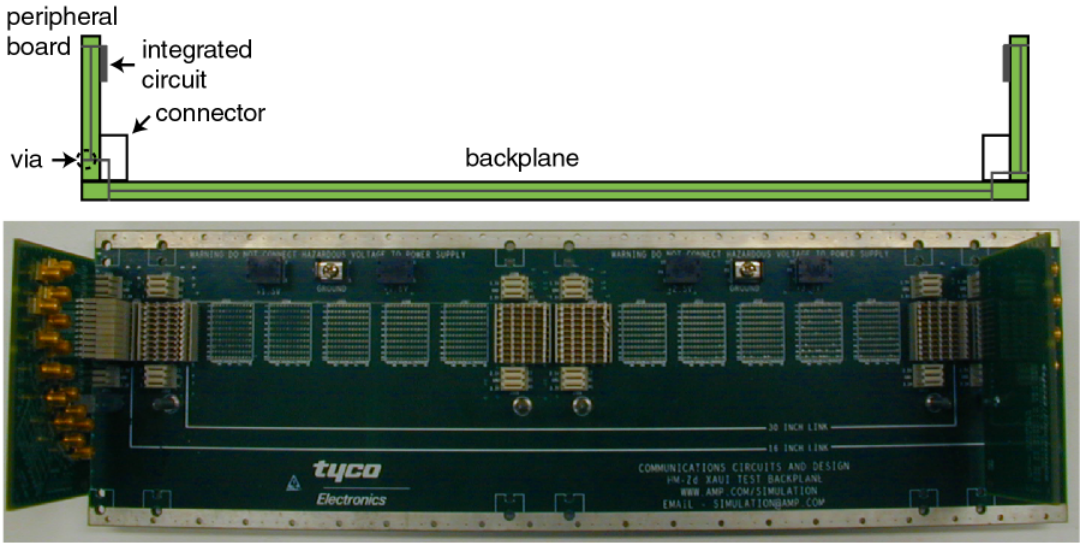

Figure 2.4 FR4 backplane with peripheral boards and connectors for serial communication.

contains the impedance discontinuities introduced by the vias and connector. Complete shielding is not possible due to the routing density and several serial links run in parallel.

Shielded transmission lines are limited by skin-effect losses and dielectric losses. Skin effect arises from non-uniform electric field in conductors. Consequently, the resistance of the wire increases and is accompanied by an effective internal inductance [51]. The skin loss can be expressed as

$$G_{skin}(f) = e^{-(1+j)l\sqrt{\pi\mu\sigma f}}, \tag{2.9}$$

where l is the wire length, μ is the permeability, and σ is the conductivity. The loss is a function of frequency, which is why it is generally referred to as a frequency-dependent loss. The phase shift and amplitude attenuation are identical for skin effect.

Additionally, the dielectric material of the FR4 material causes loss:

$$G_{dielectic}(f) = e^{-l\frac{\sqrt{\varepsilon_r}\tan\delta}{c}f}, \tag{2.10}$$

where ε_r is the dielectric constant and $\tan\delta$ is the loss tangent of the material. A thorough discussion of the skin and dielectric losses in modern materials is given by Deutsch [52].

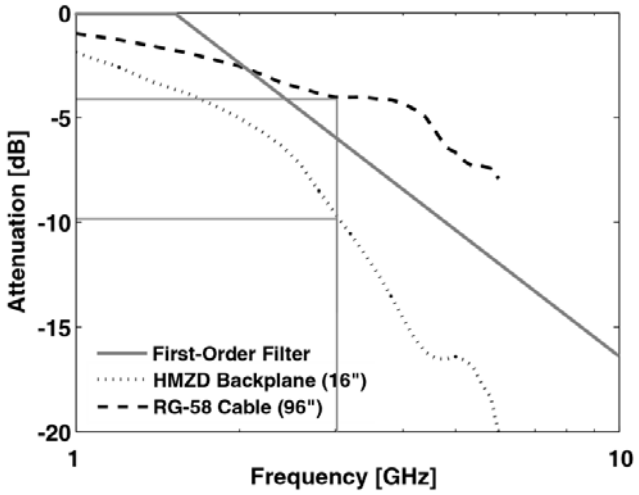

Figure 2.5 Signal attenuation for a commercial FR4 material and for a shielded cable.

The via stubs and connectors cause signal reflections at gigahertz frequencies. These reflections also cause dispersion and, consequently, intersymbol interference in the link. In Figure 2.5, the FR-4 frequency response features bumps that are attributable to these reflections. Finally, the connectors and parallel transmission lines in the backplane can generate crosstalk between neighboring lines. The crosstalk also limits the bandwidth.

For modern backplanes, these loss and dispersion mechanisms limit the bandwidth of interconnects to around 3GHz. Consequently, the bandwidth is fixed, and the challenge for circuit designers is to reach higher data rates through equalization, different modulation schemes, and coding.

2.1.3.2 Optical Links

Optical fiber represents broadband channel that may replace electrical interconnects. The loss of fiber is low over a wide range of optical frequencies. At the 1.55μm wavelength, the loss of 0.2dB/km extends over 10THz. In principle, this window could support a data capacity of 4 Tb/s [54]. However, in long-haul fiber-optic communication dispersion limits the modulation frequency and the optical bandwidth is split into 10Gb/s

channels using wavelength-division-multiplexing (WDM). Reaching 40Gb/s is possible if fiber dispersion is controlled.

The origins of dispersion depend on the fiber [55]. Initially, fibers were designed with large fiber diameters (50-100μm). As light propagates down the fiber, it reflects off the fiber walls randomly. The different path lengths cause modal dispersion given by the range of arrival time for the optical signal, ΔT:

$$\Delta T = \left(\frac{n_{core} - n_{clad}}{8c \cdot n_{core}} \right)^2 L, \tag{2.11}$$

where L is the fiber length, c is the speed of light, and n_{core} and n_{clad} are the index of refraction of the cladding and the core. Over 1km of fiber, this dispersion is greater than 100ps. In response, fiber manufacturers developed single mode fiber with a narrower core (8-10μm).

Next, the modulated signal suffers from a group-velocity dispersion, characterized by the variation in the group velocity variation, D. The amount of dispersion depends on the modulation bandwidth and, hence, the data rate. Group velocity dispersion is given by

$$\Delta T = |D| \cdot \Delta\lambda \cdot L, \tag{2.12}$$

where the modulation bandwidth is the range of wavelengths, $\Delta\lambda$.

Finally, optical bandwidth is limited by polarization mode dispersion. The modulated light is composed of two polarizations that propagate at different speeds. This causes a statistical spread in the arrival time due to the time-varying coupling between modes:

$$\overline{\Delta T} = D_{pmd}\sqrt{L}, \tag{2.13}$$

where D_{pmd} is the polarization mode dispersion.

Tremendous optical bandwidth exists, but the design of optical transceivers above 10Gb/s must consider the use of electronic as well as photonic equalization techniques for lightwave communication [56].

2.1.4 Capacity

In Figure 2.6, the channel capacity is plotted against the bandwidth of the Butterworth filters in Figure 2.3. The NRZ PSD is constant, i.e., the bit rate is fixed. Increasing or decreasing SNR shifts the capacity curves vertically. Notably, most of the capacity improvement occurs when using a second-order response over a first-order response. The channel capacity typically reached in high-speed systems is shown for comparison. Here the (3dB) cut-off frequency, f_c, is 70% of the bit-rate, f_b. The margin between the achievable capacity and the actual data rate is lost to preserve simplicity in system and circuit design. Shannon provided a limit for communication capacity. However, this theory does not offer insight into *how* to design circuits for a communication link. As high-speed serial links are increasingly bandwidth-limited, communication theory suggests appropriate modulation schemes and equalization techniques to reach the channel capacity limit [47]. For instance, maximum-likelihood sequence estimation can ideally recover an extremely distorted or bandwidth-limited signal. In high-speed integrated circuit design, the possible implementations are curtailed dramatically, and circuit designers must rely on a subset of the signal processing tools to maximize data rates. The computational power required by many equalization techniques is unrealizable both from the standpoint of power as well as circuit speed. Early equalization of

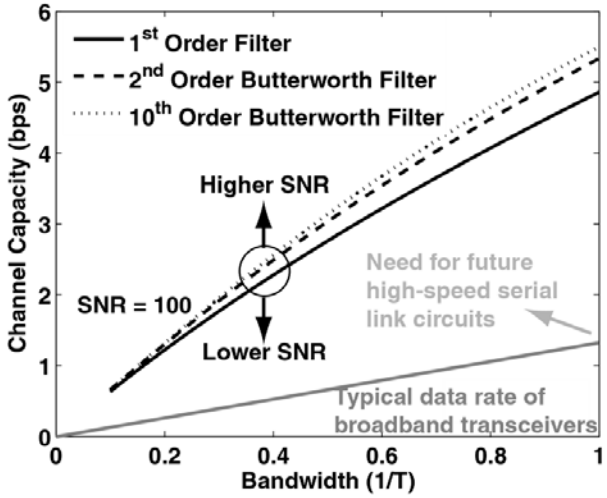

Figure 2.6 The Shannon capacity as a function of bandwidth.

bandwidth-limited channels focused on data transmission over the legacy Bell telephone network [50]. In the following section the signal integrity of communication in the bandwidth-limited region is discussed. The impact of the bandwidth limitation on the signal motivates the analysis of deterministic effects and equalization techniques introduced in later chapters.

2.2 High-Speed Signal Integrity

2.2.1 Bit Detection

A common receiver scheme is to detect the digital data stream through sampling the input analog signal as illustrated in Figure 2.7. First, the input signal, $y(t)$, is amplified and filtered. Next, the comparator makes a decision about the value of the analog signal by comparing the value to a voltage threshold, v_{th}. This decision is made with the sampling clock signal, *clk*. Once the comparator samples the analog data signal, the result, $\tilde{y}(t)$, is interpreted as the digital symbol, either 0 or 1 for 2-PAM.

Hence, the analog signal must surpass the voltage threshold at the sampling time to detect the bit without error. The actual implementation of a comparator places more

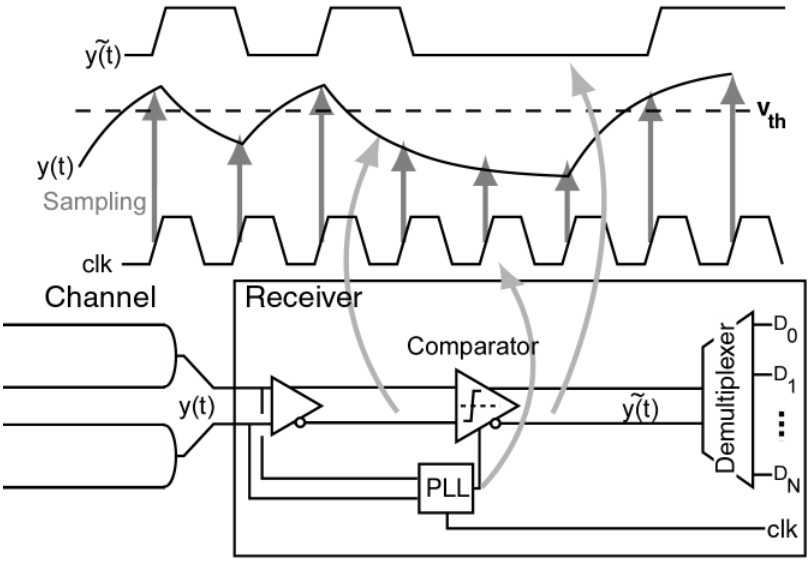

Figure 2.7 Digital regeneration through sampling of the analog signal in a comparator.

restrictions on the analog signal swing. The comparator has metastability issues for small inputs and, consequently, the signal swing must typically significantly surpass the voltage threshold for proper operation. Additionally, for small signal swings, the comparator needs a certain amount of hold time during which the analog signal remains above the voltage threshold to generate the proper digital value. The comparator requires a minimum voltage and timing margin on the signal to operate without generating additional errors.

To gauge the average voltage and timing margins, the signal is folded every bit period to create an overlapping set of possible signal voltages. This is a data eye, so called because the center of the plot is open, determining the voltage and timing margins with respect to the sampling clock. The data eye facilitates calculating the bit-error rate (BER) from the signal. Consequently, the data eye will provide qualitative and quantitative definitions for the signal integrity of the analog signal. An example of a data eye is shown in Figure 2.8 for a first order system. The voltage margin is ΔV and the timing margin is ΔT. Each is respectively defined at a sampling time and voltage threshold.

2.2.2 Voltage and Timing Margins

In this section the deterministic effects of bandwidth limitation on eye closure are discussed. Lowering the bandwidth or increasing the bit rate reduces the eye opening,

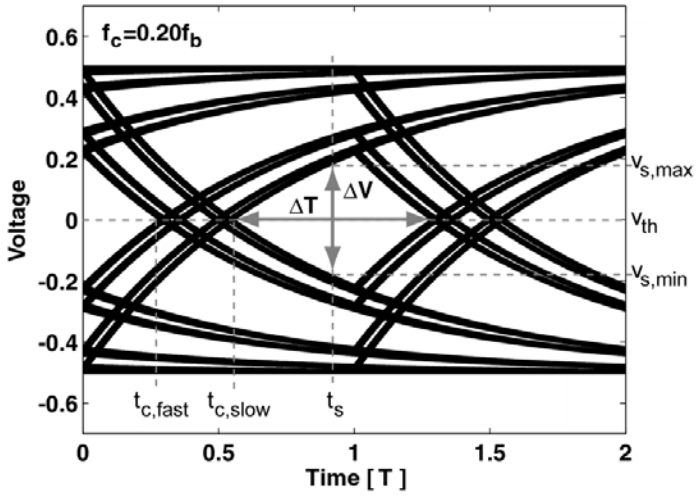

Figure 2.8 Illustration of the analog signal as a data eye and signal integrity definitions.

aggravating the detection of digital symbols from the analog signal. Since bit-by-bit signal detection requires a sampling clock and a voltage threshold, signal integrity is defined as the relationship of the voltage and timing margins of the data eye to a bit-error rate (BER).

The threshold crossing time at which the analog signal passes the voltage threshold is denoted, t_c, i.e. $y(t_c)=v_{th}$. Part of the contribution of this thesis is the analysis of the threshold crossing time deviations, which will be discussed in the next chapter. For LTI responses, the voltage threshold occurs where the timing margins are the greatest. The fastest edge on the left and right side of the eye data are identical, and the timing margin is

$$\Delta T = T - (t_{c,\,slow} - t_{c,\,fast}). \tag{2.14}$$

The optimal sampling time is chosen to minimize errors. The timing margin given by (2.14) determines the sampling time. Equally spacing the sampling time between the slowest and fastest edges gives

$$t_s = t_{c,\,slow} + \frac{\Delta T}{2} = \frac{T}{2} + \frac{t_{c,\,slow} + t_{c,\,fast}}{2}. \tag{2.15}$$

Now, the voltage margin is defined from this sampling time. Alternatively, the voltage margin could be maximized to determine the sampling time:

$$\Delta V = v_{s,\,max} - v_{s,\,min}. \tag{2.16}$$

Equations (2.14) and (2.15) are worst-case definitions of the voltage and timing margins. In many cases, the worst-case is too severe in communication applications because a small BER might be acceptable. Finding the margins for a given BER is possible by studying the probability for the deterministic features of the signal.

2.2.3 Modeling of Intersymbol Interference and Data-Dependent Jitter

Intersymbol interference (ISI) reduces the voltage margins of the data eye from the maximum swing. The voltage margins achieved in (2.16) are a subset of the actual logical values. If the maximum voltage swing is $2V_s$, the peak-to-peak reduction due to ISI is

$$V_{pp,\,ISI} = 2V_s - \Delta V. \tag{2.17}$$

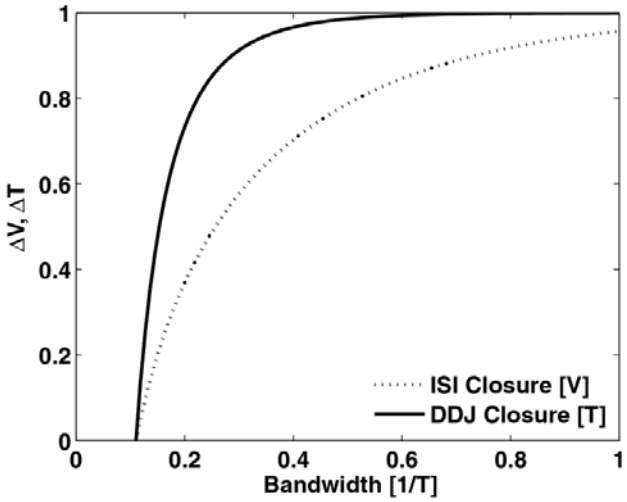

Figure 2.9 The reduction of voltage and timing margins due to ISI and DDJ in a first-order system as a function of bandwidth.

Since the margins depend on the precise sampling time, the ISI is only meaningful for a particular sampling time. The deterministic reduction in the timing margins due to bandwidth is peak-to-peak data-dependent jitter (DDJ) and from (2.14) is

$$J_{pp,\,DDJ} = T - \Delta T. \tag{2.18}$$

The definition for jitter is only meaningful at a particular voltage threshold. The peak-to-peak reduction in the timing and voltage margins is shown in Figure 2.9 as a function of the bandwidth of a first-order channel. The eye opening is normalized both in the voltage domain as well as the timing domain. At larger bandwidths the ISI is the dominant constraint. As the bandwidth reaches about f_c=0.3f_b, the DDJ increases and the timing margins become restrictive. Once f_c = 0.11f_b, the eye becomes completely closed for a first-order system and the voltage and timing margins go to zero. Therefore, in extremely bandwidth-limited situations, understand the timing and voltage degradation is important.

To understand the relationship of ISI and DDJ on non-zero BER, modeling the worst-case trajectories predicts probabilistically how often these margins are reached. A “bathtub” curve is the BER cumulative-distribution function (CDF) and is shown in

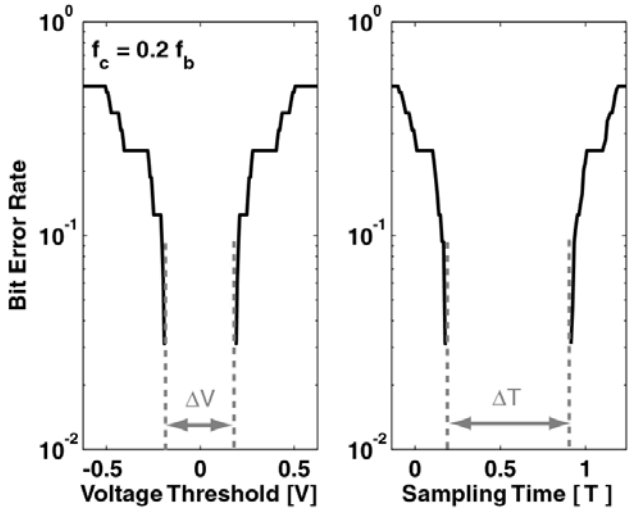

Figure 2.10 Cumulative distribution function for BER for DDJ and ISI in the absence of random noise. The margins are the gap in the center of each bathtub.

Figure 2.10, where a data eye is scanned at different voltage thresholds and sampling times and the bit-errors are counted.

Since signal integrity is defined for a specific BER, a distinction between peak-to-peak performance and the performance at a given BER is necessary. If we were satisfied with an error of 10^{-1}, the margins would be expanded significantly. In serial links errors are tolerable, if they ever occur. Typically, we are ultimately interested in the signal integrity for 10^{-12} BER. In practice, simulating the response for 10^{12} bits is difficult and, hopefully, unnecessary. For deterministic effects, the worst-case scenarios occur more regularly. Simulating *n*-bit sequences captures the relevant deterministic reduction in the BER if the reduction in the margins occurs with *n* bits.

The CDFs in Figure 2.10 suggest modeling the ISI and DDJ with an *ad hoc* probability density function (PDF). The step gradient along the bathtub edges suggest modeling the PDFs for ISI and DDJ as a combination of dirac delta functions:

$$PDF_{ISI}(v_s) = \frac{1}{2^k}\sum_{i=1}^{2^k}\delta(v_s - v_i) \quad \text{and} \quad PDF_{DDJ}(t_c) = \frac{1}{2^{k-1}}\sum_{i=1}^{2^{k-1}}\delta(t_c - t_i), \qquad (2.19)$$

where the sampled voltage, v_s, and threshold crossing time, t_c, occur at each delta function located at voltages, v_i, and threshold crossing times, t_i, which are determined by the particular data sequence that is k bits long. The number of peaks in (2.19) depends on k. Notably there are 2^{k-1} threshold crossing times, but 2^k voltages. Bandwidth limitations tend to increase the number of dominant PDF peaks. In many cases several threshold crossing time delta functions overlap into a single DDJ peak, providing a more compact the PDF than in (2.19). The simplest form of DDJ occurs when two peaks are present:

$$pdf_{DDJ}(t_c) = \frac{1}{2}[\delta(t_c - t_o) + \delta(t_c - t_o - t_{c,\,DDJ})]\,. \tag{2.20}$$

This PDF is sometimes called the absolute jitter since it is compared to an ideal reference. The purpose of Chapter 3 is to investigate the location of these peaks. Given the DDJ PDF, we can analyze some statistical properties. We can calculate the mean, m_{DDJ}, and variance, $(\sigma_{DDJ})^2$, of (2.20). From measurements, the root-mean-square (rms), J_σ, is σ_{DDJ}, and we use J to imply jitter. The rms jitter will be used in subsequent sections to calculate BER. J_{pp} gives the absolute range for the transition arrival. From (2.20), the rms and peak-to-peak DDJ is

$$J_{\sigma,\,DDJ} = \frac{t_{c,\,DDJ}}{2} \quad \text{and} \quad J_{pp,\,DDJ} = t_{c,\,DDJ}\,. \tag{2.21}$$

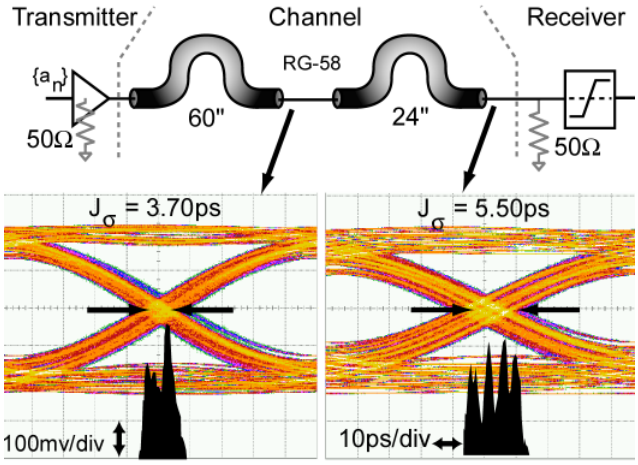

Figure 2.11 The data-dependent jitter generated over RG-58 cable at 10Gb/s and jitter histograms.

To illustrate the impact of DDJ on a real data eye, Figure 2.11 demonstrates a 10Gb/s data sequence transmitted over RG-58 cable. The cable bandwidth reduces with increasing length. After 60” of cable, the data suffers from both ISI and DDJ. The total rms jitter is 3.70ps after 60” and increases to 5.50ps after transmission over an additional 24”. The additional length reduces the bandwidth of the link and increases the jitter. Qualitatively, the DDJ in the two eyes justifies the delta function model. In the first plot the jitter has two dominant peaks. In the second plot four distinct peaks appear. However, these peaks are obscured by random jitter which we will now discuss.

2.2.4 Random Noise and Jitter in Bit Error Rate

This section discusses the impact of random, or non-deterministic, sources of noise on the link performance. Noise is an inevitable feature of any electronic system. Johnson and Nyquist determined that the thermal noise resulting from a resistance behaves as uniform power spectral density (PSD) [48][49]. Heffner demonstrated that any resistance resulted in a PSD that was essentially flat to 80THz [57].The PSD for a resistance is

$$S_r(f) = 4kTR \qquad \left[\frac{V^2}{Hz}\right], \tag{2.22}$$

which resembles our noise PSD assumption in (2.6). Uhlenbeck and Ornstein demonstrated that any bandlimited thermal process is modeled with a Gaussian PDF [58]. In electrical interconnects we assume that bit detection is limited by Gaussian noise processes. A general Gaussian PDF describing the voltage noise is given as

$$PDF_n(v) = \frac{1}{\sqrt{2\pi\sigma_n^2}} e^{-\left(\frac{v^2}{2\sigma_n^2}\right)}, \tag{2.23}$$

where $\sigma_n^2 = 4kTR$. Random noise increases the probability of error. The voltage noise is added to the signal, creating a possibility that the bit is detected incorrectly. The probability of an error is expressed as the combination of the probability that the signal will be detected as a one when a zero was transmitted and vice versa [47]:

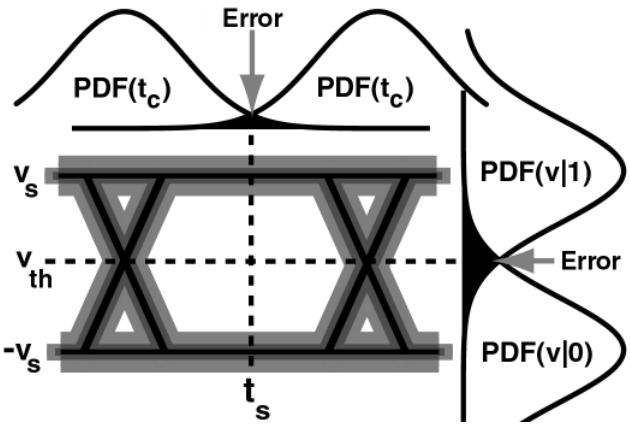

Figure 2.12 Random noise and jitter distributions and their relationship to the data eye.

$$Pr(error) = Pr(1|0)Pr(0) + Pr(0|1)Pr(1). \tag{2.24}$$

In most situations, $Pr(0)=Pr(1)=1/2$, and the PDF is expressed with (2.23):

$$Pr(error) = \frac{1}{2}\frac{1}{\sqrt{2\pi\sigma_n^2}}\left(\int_{v_{th}}^{\infty} e^{-\left(\frac{(v+v_s)^2}{2\sigma_n^2}\right)} dv + \int_{-\infty}^{v_{th}} e^{-\left(\frac{(v-v_s)^2}{2\sigma_n^2}\right)} dv\right). \tag{2.25}$$

To express the BER, (2.25) is multiplied by the rate at which bits are transmitted, which is $1/T$ for NRZ transmission. In high-speed digital communication, the finite rise and fall times introduce timing jitter. Random jitter can be described as a translation of the voltage noise into timing deviations through the signal slope [59]:

$$RJ(t_c) = \frac{n(t)}{|x'(t_o)|}. \tag{2.26}$$

The threshold crossing time deviation, *RJ*, due to voltage noise is also a random variable. This expression relies on an implicit relationship between the slope "near" the threshold crossing time and the actual threshold crossing time. The perturbation due to noise is assumed to be small. This type of random timing jitter in digital signals is clearly a bounded distribution since the rise and fall time of the transition is finite while the voltage noise is unbounded. Nevertheless, the analysis of random jitter will be approached as the

linear translation of a Gaussian process. Therefore, the timing jitter is also a Gaussian process:

$$PDF_{RJ}(t_c) = \frac{1}{\sqrt{2\pi\sigma_{RJ}^2}} e^{\frac{-(t_c - t_o)^2}{2\sigma_{RJ}^2}}, \tag{2.27}$$

where $\sigma_{RJ} = \sigma_n / \left|x'(t_o)\right|$. The implicit dependence on the slope is estimated with t_o, the unperturbed threshold crossing time.

The probability of error is calculated by considering a transition in the data. If such a transition occurs, then there will be a threshold crossing time. The threshold crossing time can either be early or late. Therefore,

$$Pr(error) = [Pr(t_c > t_s | a_{-1} \neq a_0) + Pr(t_c < t_s | a_1 \neq a_0)] Pr(a_{-1} \neq a_0). \tag{2.28}$$

Notice that in (2.28) the sampling events described by the first and second term on the right-half side are in adjacent bit intervals. Nevertheless, the probability that there is a transition is the same for both edges. Therefore,

$$Pr(error) = \frac{1}{2} \frac{1}{\sqrt{2\pi\sigma_{RJ}^2}} \left(\int_{t_s}^{\infty} e^{-\left(\frac{(t_c - t_o)^2}{2\sigma_{RJ}^2}\right)} dt_c + \int_{-\infty}^{(t_s - T)} e^{-\left(\frac{(t_c - t_o)^2}{2\sigma_{RJ}^2}\right)} dt_c \right). \tag{2.29}$$

Finally, the total errors in the link could be calculated by adding (2.25) and (2.29) if we assume that the noise at the threshold crossing time is uncorrelated to the noise at the sampling time. This correlation depends on the bandwidth and the time interval between the threshold crossing time and sampling time. In Figure 2.13, the BER is simulated in the presence of random jitter for the same bandwidth limitation in Figure 2.10. The RJ is superimposed on the ISI and DDJ. The margins of the eye are further reduced in the presence of RJ. RJ and DDJ are uncorrelated PDFs for NRZ data and the total jitter (TJ) PDF is the convolution of the RJ and DDJ PDFs:

$$PDF_{TJ} = PDF_{RJ} \otimes PDF_{DDJ}. \tag{2.30}$$

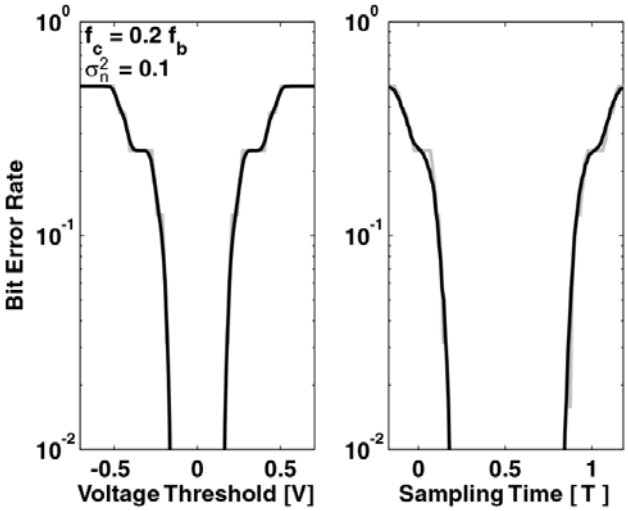

Figure 2.13 BER under the influence of ISI and DDJ with random noise. Voltage margins and timing margins are represented by gap in the center of the data eye.

Therefore, the RJ is mapped onto each DDJ peak. The variance of the TJ is the sum of the RJ and DDJ contributions:

$$\sigma_{TJ}^2 = \sigma_{DDJ}^2 + \sigma_{RJ}^2. \tag{2.31}$$

In Figure 2.14, the simulated data eye for different voltage thresholds and sampling times is compared to a BER calculation using the convolution in (2.30) with the DDJ PDF

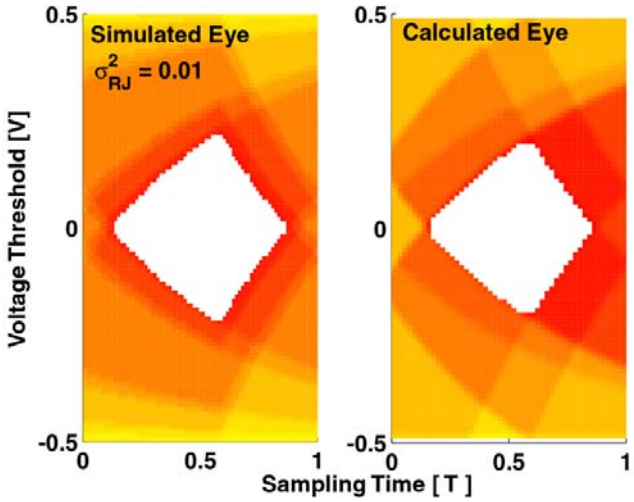

Figure 2.14 Two-dimensional plot of the BER. The color contours follow the trajectories of the signal.

in (2.20) and the RJ PDFs in (2.25) and (2.29). Many of the general features of the BER contour are similar between the two plots. The simulated BER demonstrates additional DDJ and ISI effects because of the simple DDJ PDF model. Both BER plots show a similar region of the data eye that can be sampled for low BER.

2.2.5 Jitter and Clock Recovery

The total jitter aggregated through the link affects the operation of the clock and data recovery circuit (CDR) in the receiver. Oftentimes, high-speed links do not transmit a clock to the receiver. Consequently, the receiver must determine the frequency and phase of the data signal to generate the sampling clock. CDR circuits are often phase-locked loops (PLL) that lock to the received data transitions. The PLL is demonstrated as part of the receiver in Figure 2.1. A detail of the CDR operation is shown in Figure 2.15 and is described in detail in [60]. The receiver local oscillator is locked through a feedback loop to the incoming data edges. Alternatively, the clock recovery can be performed with a delay-locked loop (DLL) when the frequency is known or is not required in the receiver [14][16]. Similarly, DLLs rely on feedback to provide phase lock to the data transitions.

Early timing recovery systems were based on DLL architectures, and the relationship between noise and jitter variance in threshold crossing detection was first described by Saltzberg [61]. In early optical communications, a clock signal was generated from square-law devices that generated spectral energy at the clock frequency from NRZ sequences [62]. Statistical analysis of the random jitter in these systems quickly became critical for long-haul communication networks [63]-[65]. However, the rise of integrated circuits for communications allowed the use of more sophisticated timing recovery

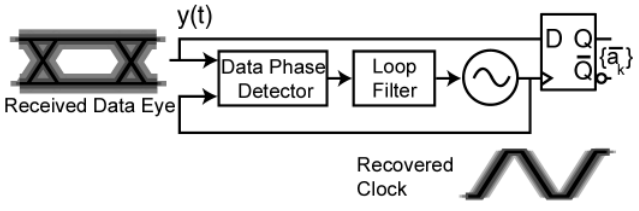

Figure 2.15 Phase-locked loop for clock and data recovery. Any jitter on the data is transferred to the recovered clock.

techniques. In early circuits the clock harmonic was generated with a one shot [66], and jitter was studied in these systems [67]. A study of synchronization for square law devices as well as zero-crossing detection is provided in Meyr, Moeneclaey, and Fechtel [68].

This analysis studies charge-pump PLLs often used in integrated circuit receivers. Since the data transitions provide synchronization, any phase ambiguity in the data signal causes ambiguity in the sampling time of the local clock. Therefore, deterministic jitter degrades the performance of the PLL by varying the phase of the data transition. The ability of the PLL to reject these phase ambiguities depends on the feedback dynamics.

The CDR circuit inherently produces jitter as well. The local oscillator and phase detector circuit produce timing jitter that contributes to the total jitter of the receiver sampling clock. Depending on where noise is introduced to the feedback loop, the PLL responds differently [69]. At this point we consider random jitter at the input to the phase detector and phase noise of the VCO. In Figure 2.16 the linear model for a charge-pump PLL is demonstrated with these jitter sources.

The phase detector is influenced by phase variations of the transmitter clock phase noise and DDJ. If a white jitter source is at the input of the PLL, $S_{\phi,i}$, that is proportional to the variance of the total jitter at the input, the influence of the noise PSD can be applied to the loop dynamics to calculate the output jitter. For a charge-pump PLL, the closed loop transfer function from the phase detector input to the PLL output is

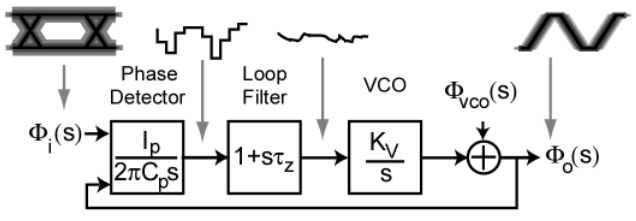

Figure 2.16 Linear model of a charge-pump PLL.

$$\frac{\Phi_o(s)}{\Phi_i(s)} = H(s) = \frac{1 + \frac{s}{\omega_n Q}}{1 + \frac{s}{\omega_n Q} + \left(\frac{s}{\omega_n}\right)^2}, \tag{2.32}$$

where $\omega_n = \sqrt{I_p K_v / (2\pi C_p)}$ and $Q = 1/(\omega_n \tau_z)$. These dynamics describe a low-pass filter. Higher order loop filters can be used to tailor the response to reject additional phase noise and jitter [70]. For the input jitter, the output jitter PSD is

$$S_{\phi_o}(f) = |H(f)|^2 S_{\phi_i}(f), \tag{2.33}$$

where we assume a noiseless VCO. The voltage controlled oscillator phase noise has received extensive study [71]-[74]. The basic phase noise characteristics of the VCO can be characterized by a $1/f^2$ region and a $1/f^3$ region corresponding to the perturbation of white and flicker noise sources in the VCO. Consequently, the PSD for the oscillator phase noise is assumed to follow

$$S_{\phi_{vco}}(f) = f_b^2\left(\frac{c_2}{f^2} + \frac{c_3}{|f|^3}\right), \tag{2.34}$$

where c_2 and c_3 are defined by the VCO topology as discussed by [71][73]. The transfer function from the VCO phase noise to the output is

$$\frac{\Phi_o(s)}{\Phi_{vco}(s)} = 1 - H(s). \tag{2.35}$$

This function is a high-pass response. At low frequencies a zero attenuates the VCO phase noise. At high frequencies the output phase follows the VCO phase noise. Similar to (2.33), the output jitter PSD under the influence of VCO noise is

$$S_{\phi_o}(f) = |1 - H(f)|^2 S_{\phi_{vco}}(f) \tag{2.36}$$

when we consider a jitterless input. The right-hand sides of (2.33) and (2.36) combine to quantify the total jitter PSD of the PLL output. In CDR circuits, the timing jitter is useful for describing the circuit performance. To relate the phase PSD to the output timing jitter,

the Wiener-Khinchin theorem translates the jitter PSD to the output sampling variance, σ_s [75]:

$$\sigma_s^2 = \frac{2}{\omega_b^2}\int_0^\infty S_{\phi_o}(f)df, \tag{2.37}$$

where $\omega_b = 2\pi/T$. Analytical results for (2.37) are possible if the loop dynamics are constrained. In the following equations, we assume that the loop is critically damped, i.e. $Q = 1/\sqrt{2}$. For other damping factors, the timing jitter can be solved numerically. For the contribution of white input jitter, we find the timing jitter variance is

$$\sigma_s^2 = \sigma_{TJ}^2 \frac{3\omega_n T}{2\sqrt{2}}. \tag{2.38}$$

This result is similar to the theoretical calculation for zero-crossing synchronization in [68]. Now we ignore the jitter at the input of the PLL. The timing jitter introduced by the phase noise of the VCO input is

$$\sigma_s^2 = \frac{c_2}{2\sqrt{2}\omega_n} + \frac{\pi c_3}{2\omega_n^2}. \tag{2.39}$$

The loop bandwidth, ω_n, influences the relative contribution to output timing jitter of the input jitter and VCO phase noise. By reducing the bandwidth, the output timing jitter is increasingly dependent on the phase noise and not the input jitter. The total output timing jitter is found by directly adding (2.38) and (2.39). Optimization of the input jitter and VCO phase noise is studied by Mansuri [70]. Typically, jitter specifications for a CDR circuit determine the acceptable cut-off frequency.

Returning to our discussion on the random jitter influence of BER, we can calculate the BER induced by both the jitter in the data eye and the sampling uncertainty of the clock using (2.29):

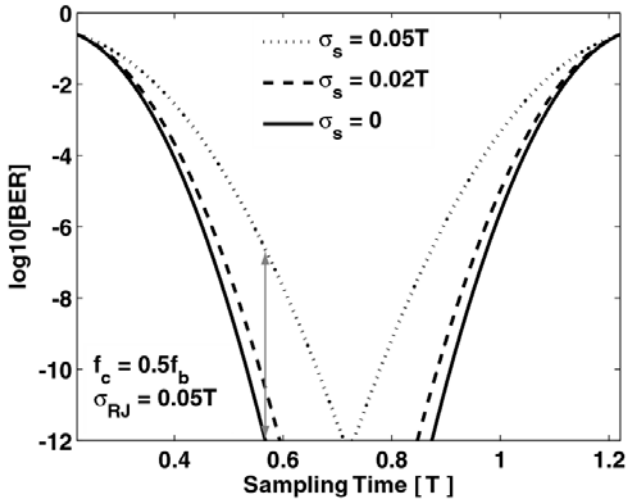

Figure 2.17 BER under the influence of sampling uncertainty. The transition edges and sampling uncertainty are governed by different random processes.

$$Pr(error) = \frac{1}{\sigma_s\sqrt{2\pi}} \int_{-\infty}^{\infty} Pr(error|t_s) e^{-\left(\frac{(t_s - t_{s,\,opt})^2}{2\sigma_s^2}\right)} dt_s, \tag{2.40}$$

where $t_{s,opt}$ is the mean sampling time. The effect of sampling uncertainty is plotted for different standard deviations in Figure 2.17. Notably, the impact of sampling uncertainty increases the BER. If the rms RJ on the transitions and the sampling time are 5% of the bit period, the BER is degraded by more than 10^{-5}. For rms jitter below two percent of the standard deviation the sampling uncertainty does not affect the BER drastically. In fact, the effect of the sampling uncertainty can be expressed as an additional contribution to the total jitter. Only one Gaussian density function needs to be calculated for the ambiguity of the data transitions, and the total jitter from (2.31) is modified to

$$\sigma_{TJ}^2 = \sigma_{DDJ}^2 + \sigma_{RJ}^2 + \sigma_s^2. \tag{2.41}$$

This observation indicates that the filtering in the CDR need only to reduce the variance of the sampling clock to a fraction of the RJ and DDJ such that the BER performance will be dominated by the RJ on the data transition edges and not sampling uncertainty.

2.3 Definitions of Jitter

At this point, jitter has been defined by the timing deviation from an ideal reference. This is often called absolute jitter. In Figure 2.18 each data edge has a threshold crossing time, t_c, that progresses with each edge. Since we observe this threshold crossing time in the data eye, we assume it is normalized to the bit period. The rms and peak-to-peak values of absolute jitter have been calculated in (2.21).

Cycle-to-cycle jitter is also useful to characterize circuit performance. This is calculated as the difference in adjacent threshold crossing time deviations:

$$\Delta t_c[m] = t_c[m+1] - t_c[m]. \tag{2.42}$$

This definition is useful for clock signals or other periodic signals that have transitions every cycle. However, as depicted in Figure 2.18, transitions for NRZ occur randomly. Therefore,

$$\Delta t_{c,n}[m] = t_c[n+m] - t_c[m] \tag{2.43}$$

is the long term jitter across n bit intervals. This definition is more practical for NRZ data since the jitter for each interval can be studied and averaged to deduce the cycle-to-cycle jitter. This will be discussed in Chapter 3.

In [76] Lee performs an analysis of jitter in PLL and notes that while absolute jitter is calculated from (2.37), the cycle-to-cycle jitter for the clock is calculated as

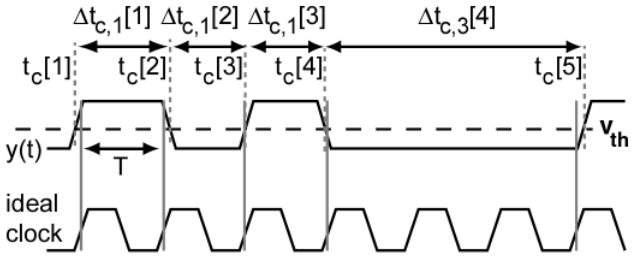

Figure 2.18 Definitions for (absolute) jitter and cycle-to-cycle jitter.

$$\sigma_{\Delta s}^2(\tau) = \frac{8}{\omega_b^2}\int_0^\infty S_{\phi_o}(f)(\sin(\pi f\tau))^2 df, \tag{2.44}$$

where τ is the time lag, in this case, *kT*, after an initial reference edge. Notice that while the absolute jitter variance does not change with the lag, the cycle-to-cycle jitter changes depending on the length of time between the edges. To compare the translation of input timing jitter to cycle-to-cycle output jitter we apply (2.33) to (2.44):

$$\sigma_{\Delta s}^2(\tau) = \sigma_{TJ}^2\frac{3\omega_n T}{\sqrt{2}}\left[1 - e^{\frac{-\tau\omega_n}{\sqrt{2}}}\left(\cos\left(\frac{\tau\omega_n}{\sqrt{2}}\right) - \frac{1}{3}\sin\left(\frac{\tau\omega_n}{\sqrt{2}}\right)\right)\right]. \tag{2.45}$$

This implies that the output timing jitter due to RJ is bounded depending on the bandwidth of the loop as well as the variance of the input jitter:

$$\lim_{\tau\to\infty}\sigma_{\Delta s}^2 = \sigma_{TJ}^2\frac{3\omega_n T}{\sqrt{2}}. \tag{2.46}$$

Notice that this result is twice the absolute jitter in (2.38) [76]. Similarly, the timing jitter introduced by the VCO phase noise is

$$\sigma_{\Delta s}^2(\tau) = \frac{c_2}{\sqrt{2}\omega_n}\left[1 - e^{\frac{-\tau\omega_n}{\sqrt{2}}}\cos\left(\frac{\tau\omega_n}{\sqrt{2}} - \frac{\pi}{4}\right)\right]. \tag{2.47}$$

As before, the bound of this result is twice as great as the absolute jitter. In Chapter 3 Markov chains are applied to DDJ to calculate the cycle-to-cycle behavior.

2.4 Sources of Jitter in Communication Links

With this understanding of RJ and DJ and how they influence the BER, we take a practical look at sources of jitter in a communication link. Standards bodies have formulated the basic characterization of jitter that is observed in serial links [40]. In Figure 2.19, the basic categorizations of total jitter are shown hierarchically. All

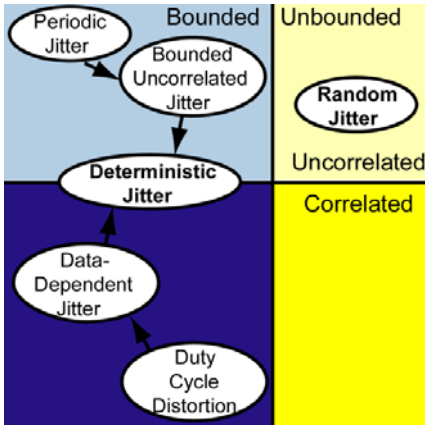

Figure 2.19 Categorization of different jitter sources of total jitter

unbounded jitter is called random jitter and has a Gaussian distribution for practical applications. All bounded jitter is called, by definition, deterministic jitter (DJ). However, deterministic jitter is further categorized by whether the jitter is correlated to the data sequence. Data-dependent jitter is the most prominent form of correlated jitter. Duty-cycle distortion (DCD) is a particular manifestation of DDJ that occurs when the voltage threshold is misplaced. Bounded, uncorrelated jitter (BUJ) is a general description of jitter that results from crosstalk, power supply noise, and periodic variations. The remainder of this thesis details analysis, modeling techniques, and equalization schemes for DDJ and crosstalk-induced jitter (CIJ).

In Figure 2.20 a communication link is illustrated with three basic sources for jitter. Random jitter introduced on the transmitter side of the channel is summarized with the rms notation, $J_{TX}(v_{th})$. The argument of the rms jitter is the voltage threshold since the jitter is specific to the comparator threshold. Transmitter jitter results from transmit clock phase noise and jitter generated by buffers and the line driver. The transmitter is also susceptible to power supply variations which will affect the transmitted signal. In environments with parallel interconnects, near-end crosstalk (NEXT) results from strong coupling between the neighboring lines and causes additional noise on the neighboring serial links [77][78].

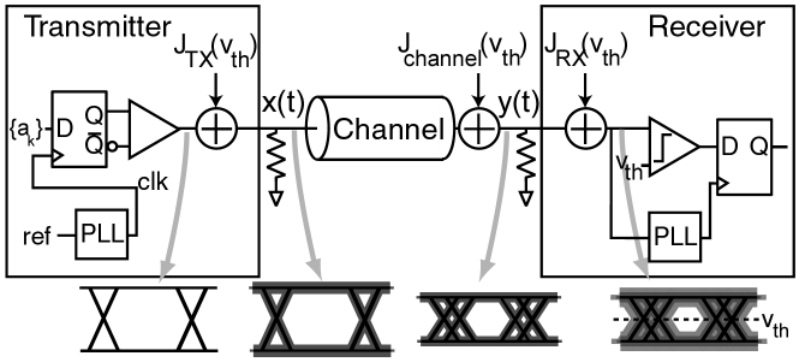

Figure 2.20 A basic model for the accumulation of jitter through a communication link.

The communication channel introduces additional jitter and is denoted $J_{channel}(v_{th})$. The transmitted data sequence propagates as a microwave through the transmission lines in a serial link. Consequently, impedance matching is required to deliver the maximum available power to the receiver. By convention, the transmission lines are designed for 50 Ohm. Source and load resistive terminations are required to avoid reflecting the signal energy. These resistances introduce a small random jitter. Additionally, the channel introduces a bandwidth limitation that results in data-dependent jitter (DDJ). As the serial rates are increased on legacy backplanes, managing DDJ becomes increasingly important. This discussion is addressed in the Chapter 3.

In the receiver the jitter is denoted $J_{RX}(v_{th})$. The amplifier and comparators introduce random jitter but, more interestingly, mismatches in the receiver chain also introduce jitter. As discussed in Section 2.2.5, the CDR circuit contributes to the jitter introduced by the receiver. Power-supply variations in the receiver also affect the received signal since the received signal is oftentimes weak. Parallel interconnects feature an additional source of noise due to coupling between serial links called far-end crosstalk (FEXT).

The following sections discuss some of the sources of random jitter in serial links. Recall from (2.30) that the random jitter and deterministic jitter convolve and, consequently, the variances add of RJ and DJ add to determine the total jitter.

2.4.1 Transmitter Jitter

One of first and most important sources of timing jitter is the transmitter. The data are multiplexed in the transmitter with a bit rate clock. As discussed for the receiver CDR, any phase noise on the transmit clock translates into timing jitter. Therefore, understanding the generation and limits of transmit clock phase noise is worthwhile. Typically a PLL locks the on-chip transmit clock to a low phase noise reference. Current technology relies on high-quality crystals to provide a frequency reference. In addition to low phase noise, crystal oscillators (XO) have low frequency drift due to temperature and aging. However, XO are limited in terms of the frequency of operation, and the highest frequency crystals are available in the 155MHz-660MHz range for communication applications.

The operation of the frequency multiplying PLL, often called a clock multiplier unit (CMU), is illustrated in Figure 2.21. The reference is compared to the high-frequency transmit clock by dividing the frequency. This divider as well as the implementation of the phase detector are the primary differences between the CMU and the CDR PLL. The closed loop transfer function from the reference input to the PLL output is similar to (2.25), except that the divider impacts the phase feedback dynamics:

$$\frac{\Phi_{CMU}(s)}{\Phi_{ref}(s)} = NH(s), \tag{2.48}$$

where N is the frequency ratio of the transmitter clock and the reference frequency, $\omega_b = N\omega_{ref}$. Note that $H(s)$ is defined in (2.32), where ω_n is also reduced by N. The transfer function in (2.48) and phase noise of the reference XO determine the transmit clock jitter:

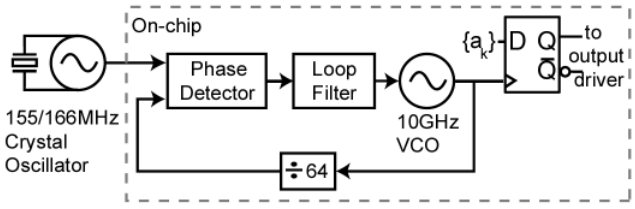

Figure 2.21 Phase-locked loop for clock multiplication. A low-phase noise crystal oscillator is used to reduce the phase noise of a 10GHz VCO.

$$S_{\phi_{CMU}}(f) = N^2|H(f)|^2 S_{\phi_{ref}}(f) + |1-H(f)|^2 S_{\phi_{VCO}}(f). \quad (2.49)$$

Since phase noise of the reference is generally not cyclostationarity [74], the Wiener-Khinchin theorem relates the phase noise PSD to the output timing jitter as in (2.37). The phase noise PSD describing the reference oscillator can be modeled with (2.34), i.e. $S_{\phi ref} = c_{XO}(f_{ref}/f)^2$. With (2.44), the output cycle-to-cycle timing jitter is calculated using (2.49):

$$\sigma^2_{\Delta,\,CMU}(\tau) = N^2 c_{XO}\left(\tau + \frac{1}{\sqrt{2}\omega_n}\left(1 - e^{\frac{-\tau\omega_n}{\sqrt{2}}}\left(\cos\frac{\tau\omega_n}{\sqrt{2}} + 3\sin\frac{\tau\omega_n}{\sqrt{2}}\right)\right)\right). \quad (2.50)$$

The linear growth of the variance in (2.50) indicates that the timing jitter is, after long enough, limited by the $1/f^2$ behavior of the reference, and the frequency multiplication amplifies this affect. On short time scales,

$$\sigma^2_{\Delta,\,CMU}(\tau) \approx N^2 c_{XO}\left(\frac{3\omega_n\tau^2}{4}\right). \quad (2.51)$$

Since the ω_n is scaled by N, the variance of (2.51) increases as N. Comparing the timing jitter to the bit period demonstrates the potential eye closure in the serial link indicating that margin is lost to transmit jitter as the data rate increases.

Previous transmitter jitter for SONET applications are summarized Table 2.1. The results at 10Gb/s indicate that the rms jitter is around 400fs, small compared to the 100ps bit period. At 40Gb/s, the rms jitter increases to around 600fs, while the bit period decreases to 25ps. The peak-to-peak jitter increases to around 4ps, one-sixth of the bit period. This decreasing timing margin emphasizes the future jitter challenges in broadband communication.

Next, random jitter accumulates through the output buffers and drivers. As discussed in Section 2.2.4, jitter is generated through the translation of voltage noise to timing deviation during the finite switching time of the transistor stages. This effect is illustrated

Table 2.1: Recently Recorded Transmitter Jitter in SONET Transceivers

Reference	Frequency	RMS Jitter	Peak-to-Peak Jitter
Cao *et al* [79]	10Gb/s	600fs	6.5ps
Hendrickson *et al* [80]	10Gb/s	N/A	3ps-5.1ps
Muthali *et al* [81]	10Gb/s	440fs	1.8ps
Werker *et al* [82]	10Gb/s	200fs	2.0ps
Meghelli *et al* [83]	40Gb/s	590fs	3.4ps
Meghelli [84]	40Gb/s	600fs	4.6ps
Kim *et al* [85]	40Gb/s	650fs	4.9ps

in Figure 2.22. Each buffer increases in size with respect to the previous stage until the output load, the 50Ohm transmission line impedance, can be driven. This requires a large drive current at the final stage and, therefore, large transistors to switch this current.

Early studies on jitter generation in buffer stages focused on the use of ring oscillators [71][72]. In [71], McNeill demonstrates that for a bipolar stage, the additive rms jitter is

$$\sigma_{buffer} = \frac{qC_L r_{bx}}{3I_{tail}}, \tag{2.52}$$

where r_{bx} is the effective input (base) noise resistance, C_L is the buffer load capacitance, and I_{tail} is the differential pair current. In most designs, the slew rate, I_{tail}/C_L, is essentially constant and the variance of the buffer jitter depends on the number of stages.

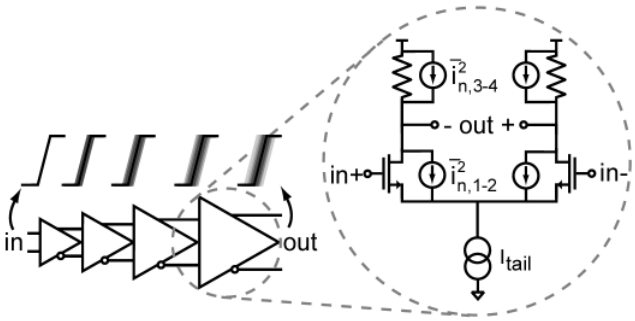

Figure 2.22 Chain of buffers and line driver in transmitter. Each stage contributes additional random jitter due to thermal sources in the MOS devices and resistors.

Weigandt expanded the first-order analysis of McNeill to consider the jitter in MOS stages with a time-varying noise model for the transistor switching [72]. The buffer jitter is determined to increase with

$$\sigma_{buffer} = \sqrt{\frac{kTC_L}{2}} \cdot \frac{1}{I_{tail}} \cdot \xi, \tag{2.53}$$

where $\xi^2 = 2(\gamma_p + \gamma_n a_v)$ is the noise multiplication factor that depends on the MOS noise factor, γ, for p- and n- MOS devices, and $a_v = g_m R_L$, the small signal gain. Notably, the difference between (2.52) and (2.53) is that the slew rate is not proportional to the rms jitter.

For example, the final output stage might drive a 500mV signal swing on the transmission line. In current fabrication technology, the total capacitance of the MOS parasitics and bond pad capacitance is around 50fF. Driver gain is close to unity and, therefore, the rms jitter is roughly 2fs, quite small compared to the transmit clock jitter.

In summary, the RJ components in the transmitter can be traced to the phase noise of the bit rate clock and the conversion of thermal noise to buffer jitter:

$$J_{TX} = \sqrt{\sigma_{CMU}^2 + \sum \sigma_{buffer}^2}. \tag{2.54}$$

Deterministic jitter sources can also be found in the transmitter, in particular when sub-rate clocks are used to multiplex the data to the bit rate. Pulse-width distortion in these cases increases the timing deviation on one of the multiplexer paths and causes a DJ in the data eye [30].

2.4.2 Channel Jitter

Much of this thesis discusses deterministic jitter introduced through the channel. However, there are additional sources of random jitter in the communication channel. The 50Ohm terminations at the transmitter and the receiver contribute thermal noise to the data signal. The real impedance required to attain maximum power transfer across the

transmission line has an effective noise voltage. This thermal noise impacts the switching signal similar to the buffer noise.

Nyquist analyzed thermal noise by considering two resistors separated by an ideal transmission line [49]. In this case we consider the bandwidth limitation of the transmission line. Consequently, the translation of thermal noise to random jitter is different at the receiver and transmitter. In Figure 2.23 a step response is illustrated as it propagates through the line. At the transmitter, the data transitions are sharpest. After transmission, the edges are slower and the translation of noise to jitter is greater. However, the transmitter noise is also filtered by the bandwidth. At its departure, a noise voltage generated by the termination is added to the signal:

$$v_{tx} = x(t) + n_{TX}(t). \tag{2.55}$$

This noise is convolved by the response of the channel, $g(t)$, which can be determined using a linear transfer function or microwave measurements. At the receiver, we find

$$y(t) = g(t) \otimes (x(t) + n_{TX}(t)) + n_{RX}(t). \tag{2.56}$$

The total noise contribution due to both the transmitter and receiver is

$$n_{total}(t) = g(t) \otimes n_{TX}(t) + n_{RX}(t). \tag{2.57}$$

The channel bandwidth passes different noise bandwidths for the two termination resistors at the receiver. The available power spectral density for the termination is calculated in (2.22). Therefore,

$$\sigma^2_{n,\,term} = 4kTR_{term}(BW_G + BW_{RX}). \tag{2.58}$$

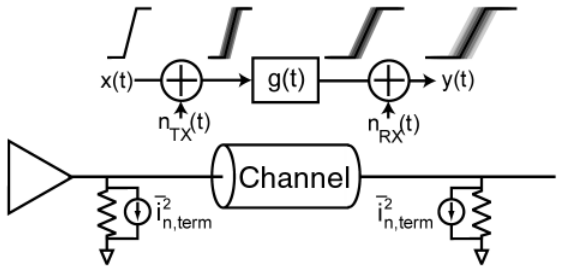

Figure 2.23 Thermal noise of terminations also adds random jitter. The bandwidth limitation of the channel impacts the variance of the additional jitter.

where BW_G is the bandwidth of $g(t)$, the path from transmitter to the receiver, and BW_{RX} is the bandwidth of the receiver. The total noise is reduced with BW_G. However, the bandwidth reduction also reduces signal slope. For the signal slope,

$$y'(t) = g'(t) \otimes x(t). \tag{2.59}$$

For a first-order response, the slope near the ideal voltage threshold is

$$y'(t_c) = \pi BW_{tx} \tag{2.60}$$

The noise bandwidth for the first-order system is $\pi BW_{tx}/2$ using the Personick Integrals [53]. Therefore, the translation of termination noise to jitter is

$$\sigma^2_{RJ,\,term} = \frac{4kTR_{term}(BW_G + BW_{RX})}{2\pi BW_G{}^2} = \frac{2}{\pi} kTR_{term}\left(\frac{1}{BW_G} + \frac{BW_{RX}}{BW_G{}^2}\right). \tag{2.61}$$

If no bandwidth limitation is present, the minimum random jitter is

$$\sigma^2_{RJ,\,term} = \frac{4kTR_{term}}{\pi BW_{RX}}, \tag{2.62}$$

while if the $BW_G = 0.25BW_{RX}$, the variance is ten times larger. Therefore, bandwidth reduction lowers the thermal noise while increasing the random jitter.

Consider a pair of 50Ω loads in a 10Gb/s link. Over a 5GHz bandwidth, each resistor generates a 80μV rms voltage. The slope translates the data edges through a receiver and transmitter bandwidth of 5GHz to generate a random jitter of 7fs. If the bandwidth of the channel is one-quarter of this bandwidth, this jitter increases to 23fs rms. This is still a small contribution. This analysis could be extended to study the impact of bandwidth on any random timing deviation in the signal.

2.4.3 Receiver Jitter

Finally, the receiver introduces additional sources of jitter. The random jitter is generated in gain stages through the same process described in the transmitter discussion. Since the gain linearly increases the variance in (2.53), the receiver will introduce

additional rms jitter on the signal to compensate attenuation. Recall in Figure 2.5 that the bandwidth of the backplane response drops by 10dB at 3GHz.

Since the receive signal is weaker and the device mismatches impair the operation of differential stages, power supply variations can also be serious in the receiver. Alon observed in serial links operating at 4Gb/s power supply variations of +/- 10mV on the digital supply [87]. Were these variations to occur randomly, they would cause jitter on the order of 1ps. However, Alon notes that these variations are deterministic. Consequently, the power supply variation behaves quasi-periodically.

Another interesting source of deterministic jitter occurs for an offset voltage threshold. Technology scaling into deep submicron lengths increases random transistor mismatch [88]. Consequently, the voltage threshold offset introduces transition ambiguity. We will study the role of the voltage threshold in the generation of DDJ in Chapter 3.

In summary, the receiver sources of random jitter include amplification in the signal buffers and the sampling uncertainty introduced by the CDR circuit. Additionally, the deterministic sources of jitter in the receiver include power-supply variations and DDJ. Since these terms are basically uncorrelated we can summarize the receive jitter as

$$J_{RX} = \sqrt{\sigma_{buffer}^2 + \sigma_{DDJ}^2 + \sigma_{BUJ}^2 + \sigma_s^2}\,. \tag{2.63}$$

2.5 Summary

This chapter reviews the channel capacity for broadband communication and discusses the limitations of current broadband channels. Currently, the design of broadband serial transceivers must focus on operation in a bandwidth-limited region where new modulation schemes and equalization techniques help push the data rate of the serial link to the channel capacity. We investigate the impact of bandwidth limitation on digital signal transmission and describe how signal integrity in the data eye causes intersymbol interference and data-dependent jitter. The deterministic effects of jitter are discussed with a probabilistic model of DDJ. Next, random jitter is introduced and the

impact on BER is discussed. The jitter also impacts the recovery of a sampling clock in the receiver. A model of a PLL used in CDR circuits demonstrates the impact of input jitter on sampling uncertainty. The impact of sampling uncertainty is described as an additional source of jitter that limits the BER.

We discuss different types of jitter that can be measured in the link and illustrate the categorization of jitter within the groups of random jitter and deterministic jitter. The sources of jitter through a communication link accumulate and we discuss some of these contributions to provide a framework for understanding the role of DDJ in serial links.

Chapter 3 Analysis of Data-Dependent Jitter

3.1 Introduction

Advancing serial data rates requires attention to timing accuracy. Timing jitter is composed of random jitter (RJ) and deterministic jitter (DJ). While RJ is uncorrelated to the data sequence, data-dependent jitter (DDJ) is a prominent form of DJ that arises from limited link bandwidth, signal reflections, and duty-cycle distortion [35][40]. This chapter presents a theoretical study of DDJ [89][90][92]. Building upon the qualitative characteristics of DDJ discussed in the previous chapter, this analysis provides quantitative relationships for the bandwidth and voltage threshold impact on the threshold crossing times. The analysis predicts the timing variation of data transitions in first- and second-order systems, and we compare these predictions with experimental results. Additionally, the analysis is extended to general linear time-invariant (LTI) systems such as transmission lines. This analysis will be used in the next chapter to motivate equalization techniques for data-dependent jitter.

The unique relationship between the data sequence and the threshold crossing time provides the opportunity to construct a Markov model to identify how the threshold crossing times are sampled. This Markov model predicts the cycle-to-cycle behavior of timing jitter as well as clarifies the full behavior of the DDJ power spectral density (PSD) in clock and data recovery circuits. These predictions are compared to simulation results for the jitter behavior and determine the severity of DDJ on circuit operation as well as on bit-error rate performance.

3.2 Analysis of Data-Dependent Jitter

The response of a causal system with finite bandwidth to a data bit is not only determined by the current bit but also the previous bits. Effectively, the system response has limited bandwidth and retains memory of the previous bits. At each transition the sequence of previous bits shifts the output amplitude and changes the time the signal crosses a decision voltage threshold, v_{th}. This timing deviation, illustrated in Figure 3.1 for 3 bits, depends on the particular data sequence.

The system response determines the behavior of DDJ. The transmitted non-return-to-zero (NRZ) data signal is

$$x(t) = \sum_{n=-\infty}^{\infty} a_n p(t-nT) \quad \text{where } p(t) = \begin{cases} 1 & 0 < t \le T \\ 0 & t \le 0,\ T < t \end{cases}. \tag{3.1}$$

Here, a_n is the binary value, $p(t)$ is the bit-period pulse response, and T is the bit period. The received signal, $y(t)$, is affected by the response of the channel. Typically, this is a LTI system, and the received pulse response is related to the channel response.

$$y(t) = \sum_{n=-\infty}^{0} a_n g(t-nT) \quad \text{where } g(t) = h(t) \otimes p(t) \quad , \tag{3.2}$$

where $h(t)$ is the channel impulse response and $g(t)$ is the received pulse response. The threshold crossing time, t_c, is when the received signal reaches the voltage threshold:

$$v_{th} = y(t_c) = \sum_{n=-\infty}^{0} a_n g(t_c - nT). \tag{3.3}$$

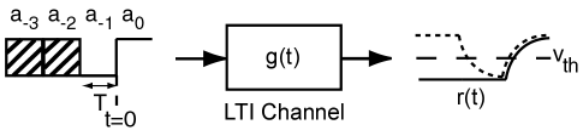

Figure 3.1 The generation of the transmitted data sequence into DDJ through a bandwidth-limited channel.

In (3.3) the threshold crossing time can be solved implicitly considering the particular function for $g(t)$.

DDJ is the probabilistic deviation of t_c for arbitrary bit sequences. Since NRZ data is generated statistically, DDJ is described by a probability density function (PDF). With a unique relationship between each sequence and a threshold crossing time, we can generalize the DDJ PDF to

$$PDF_{DDJ}(t_c) = \frac{1}{2^{k-1}} \sum_{i=1}^{2^{k-1}} \delta(t_c - t_i), \tag{3.4}$$

where t_i is the threshold crossing time for a particular sequence and k is the number of bits under consideration [91]. The mean and variance are generally expressed as

$$m_{DDJ} = \frac{1}{2^{k-1}} \sum_{i=1}^{2^{k-1}} t_i \quad \text{and} \quad \sigma^2_{DDJ} = \frac{1}{2^{k-1}} \sum_{i=1}^{2^{k-1}} t_i^2 - m^2_{DDJ}. \tag{3.5}$$

In many cases it is simpler and sufficient to average the various peaks to study only a few average jitter peaks. Making accurate approximations for the values and separation of the jitter peaks is discussed in the next sections. Since variance of the total jitter in (2.31) increases with the variance of the DDJ, this delta function separation is an important value for total jitter. Using (3.3) and the pulse response, expressions for DDJ are found and the jitter peaks in (3.4) are predicted.

3.2.1 First-Order Response[1]

Reducing the DDJ of the entire communication link into the contributions of individual blocks allows jitter analysis of each component. Oftentimes electronic circuit responses can be approximated with a first-order system. In this case, the received pulse response can be written analytically:

1. In collaboration with Behnam Analui.

$$g(t) = \begin{cases} 0 & t < 0 \\ 1 - e^{-t/\tau} & 0 \le t < T \\ e^{-(t-T)/\tau}(1 - e^{-T/\tau}) & t \ge T \end{cases}, \tag{3.6}$$

where τ is the time constant of the first-order response. Substituting (3.6) into (3.3), we discard non-causal terms

$$v_{th} = a_0\left(1 - e^{-t_c/\tau}\right) + \sum_{n=-\infty}^{-1} a_n e^{-t_c/\tau}[e^{(n+1)T/\tau} - e^{nT/\tau}]. \tag{3.7}$$

We define $\alpha = e^{-T/\tau}$, which represents the ratio between the bandwidth and the bit rate of the system. This ratio is magnified with α. For instance, if the bandwidth, f_c, is 70% of the bit rate, f_b, $\alpha = 0.0123$. If $f_c = 0.35\ f_b$, $\alpha = 0.111$. Since t_c can be extracted from the summation, (3.7) has a closed-form solution for the first-order response.

$$t_c = \tau \cdot \ln\left[\frac{-a_0 + \sum_{n=-\infty}^{-1} a_n[\alpha^{-(n+1)} - \alpha^{-n}]}{v_{th} - a_0}\right] \tag{3.8}$$

Equation (3.8) indicates how each data sequence affects the threshold-crossing time. If we consider a sequence of k bits, there are 2^{k-1} sequences with data transitions at the current bit. Each sequence with a data transition is mapped to a particular t_c in Appendix A and is graphed as a function of f_c in Figure 3.2. Assuming that the voltage threshold is equally spaced between the logic levels, i.e. $v_{th} = 0.5$, the rising and falling edge threshold crossing times are identical.

As bandwidth increases, the values of t_c converge and the variation is small. Because $\alpha < 1$, α^n is exponentially decreasing. Therefore, a_{-2} has the most dominant effect on the DDJ, and earlier bits have a diminished effect on the threshold crossing time. The slow

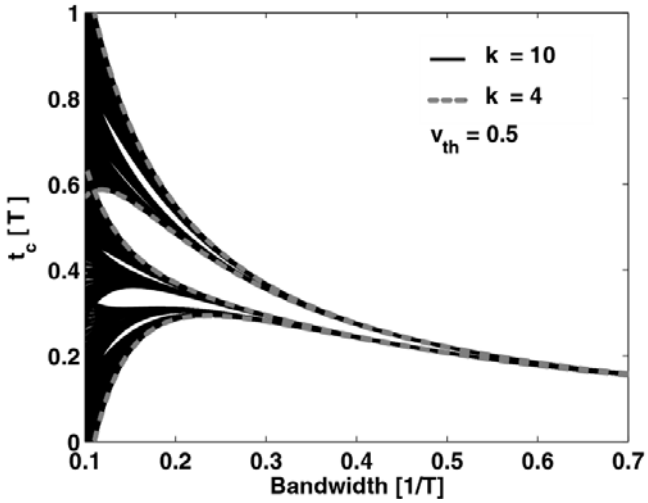

Figure 3.2 Normalized threshold crossing time with respect to the bit rate and system bandwidth for the first-order system and different bit sequence lengths.

group is associated with the 001 sequence (i.e. the step response) because the reduced bandwidth prevents the signal from reaching the binary levels. For decreasing bandwidth, the impact of additional bits appears in the DDJ PDF as the t_c split and spread in Figure 3.2. When the bandwidth is small enough that both a_{-2} and a_{-3} are significant, the DDJ PDF will have four distinct peaks instead of two.

At a given bandwidth we can locally magnify each t_c in Figure 3.2 and find the same spreading on a smaller scale. In general, the DDJ PDF in a first-order system is self-similar and forms a fractal. When α is one-half, the self-similar behavior collapses because the bandwidth is so constrained that the step response does not reach the voltage threshold within *T*. The bifurcation parameter is the *k*, the number of bits in the data sequence. For each additional *k*, each t_c bifurcates into two values. For $k = 3$, t_c takes two values depending on the penultimate bit. For $k = 4$, four values of t_c illustrated in Figure 3.2 are apparent because of the impact of the third most recent bit. Every successive transition reveals the bifurcation of t_c into two additional threshold crossing times.

Averaging all threshold crossing times eliminates the deterministic structure of DDJ in Figure 3.2. For instance, when both the fast and slow t_c are averaged together, the single

mean provides less information than two separate means for calculating bit-error rate. More information is provided about the statistical properties of t_c by conditioning the expectation on a particular previous transition. Conditioning the expectation helps determine which transition has the strongest impact on the DDJ. In the first-order response, the slow set is denoted by $E[t_c|a_{-1} = a_{-2}]$, where E is the expectation operator conditioned on the penultimate bit and $E[t_c| a_{-1} \neq a_{-2}]$ designates the fast set. The peaks of the DDJ PDF in (3.4) are represented by these expected values. For the first-order response, the impact of the kth previous bit on t_c decreases, and the mth conditioned mean is the expectation conditioned on the mth previous transition. The conditioned mean is denoted as

$$t_{c,\,DDJ}^{(m)} = E[t_c|a_{-m} = a_{-m-1}] - E[t_c|a_{-m} \neq a_{-m-1}]. \tag{3.9}$$

Assuming $v_{th} = 0.5$, we calculate the expectation from (3.8) for sequence lengths of $k = 4$,

$$\begin{aligned} E[t_c|a_{-1} = a_{-2}] &= \frac{\tau}{2}\ln[4(1-\alpha^2)] \quad \text{and} \\ E[t_c|a_{-1} \neq a_{-2}] &= \frac{\tau}{2}\ln[4(1-\alpha)(1-\alpha+\alpha^2)] \end{aligned}. \tag{3.10}$$

These means are the expected slow and fast threshold crossing times and constitute the dominant peaks for the DDJ. The difference in the conditioned mean is

$$t_{c,\,DDJ}^{(1)} = \frac{\tau}{2}\ln\left[\frac{1+\alpha}{1-\alpha+\alpha^2}\right], \tag{3.11}$$

where the superscript gives the separation for the first conditioned mean. Since the impact of previous bits diminishes, this mean difference provides an accurate quantitative description of the delta function spread of DDJ for first-order responses. Since the conditioned mean of the penultimate bit is the dominant conditioned mean for any previous transition, we write $t_{c,\,DDJ} = t_{c,\,DDJ}^{(1)}$ since the DDJ is due to the first conditioned mean. For comparison, this calculation is compared with the threshold crossing map in

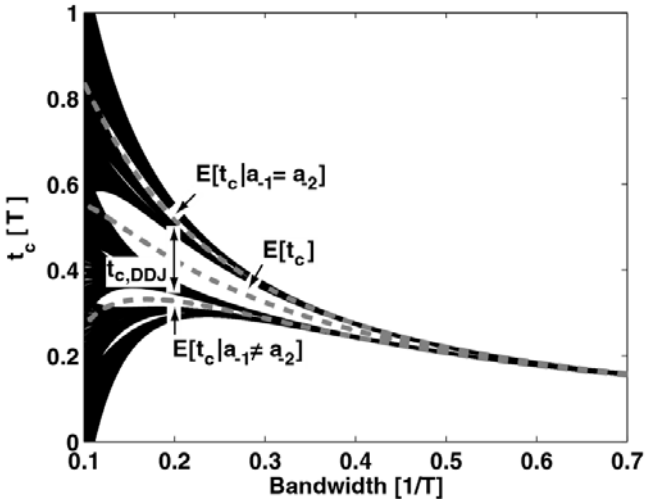

Figure 3.3 Data-dependent jitter mean and conditioned mean for determining the average probabilistic behavior.

Figure 3.3. The mean for all threshold crossing times is graphed as well. The distance between the two expectations determines the variance for the jitter.

In summary, we can approximate the DDJ PDF for the first-order response with the conditioned expectations in (3.10):

$$PDF_{DDJ}(t_c) = \frac{1}{2}\left[\delta\left(t_c - \frac{\tau}{2}\ln[4(1-\alpha^2)]\right) + \delta\left(t_c - \frac{\tau}{2}\ln[4(1-\alpha)(1-\alpha+\alpha^2)]\right)\right]. \quad (3.12)$$

The mean and variance for this distribution are calculated in Appendix A. A similar approach can be used to determine additional peaks in the DDJ PDF when necessary.

3.2.2 Higher-order Systems[1]

In general, the expression of $g(t)$ for second-order systems is a more complex function of time. Therefore, (3.3) will not have a closed form solution because t_c cannot be separated from the summation as in (3.7). However, linearization techniques such as the Taylor series expansion approximate the DDJ for higher order systems. While numerical

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methods can be introduced, series expansion provides insight about the relationship of the system response to the observed DDJ [89]. Additionally, perturbation techniques can be applied to determine the relative impact of the previous transitions [92].

Qualitatively, the possible behavior of a second-order systems includes overdamped, critically damped, and underdamped responses. A general response for second order system is expressed as

$$G(s) = \frac{1}{1 + \frac{2\zeta s}{\omega_n} + \frac{s^2}{\omega_n^2}}, \tag{3.13}$$

where ω_n is the bandwidth and ζ is the damping factor. Underdamped systems have complex poles that result in ringing. Ringing impacts the strength of previous bits on the current, t_c. For example, the 001 sequence and 101 sequence were demonstrated for the first-order system to result in the slow and fast t_c, respectively. However, for a second order response, these roles can be reversed. This implies the existence of parameters that result in minimization of the DDJ.

A first-order Taylor series approximates the step response of the second-order system:

$$g(t - nT) = g(t_o - nT) + (t - t_o)g^{(1)}(t_o - nT). \tag{3.14}$$

The superscript denotes the order of the derivative. Substituting (3.14) into (3.3), the threshold crossing time, t_c, is

$$t_c = t_o + \frac{v_{th} - \sum_{n=-\infty}^{0} a_n g(t_o - nT)}{\sum_{n=-\infty}^{0} a_n g^{(1)}(t_o - nT)}. \tag{3.15}$$

Notably, the denominator contains the slope and the numerator contains bit period delayed values of the step response. This relationship suggests that slow waveforms suffer

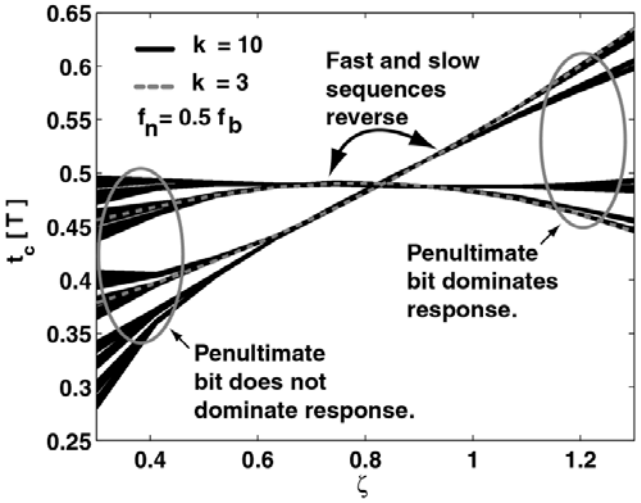

Figure 3.4 Threshold crossing time with respect to the bit rate and system bandwidth for second-order system. The intersection of the dashed lines demonstrates the data-dependent jitter minimization.

from greater DDJ. Considering *k*-length sequences of bits, the exact solution can be solved numerically. Figure 3.4 is the t_c as a function of the damping factor at a fixed bandwidth. The 001 and 101 sequences, shown in gray, do indeed intersect for a damping factor of about 0.85. This intersection verifies the anticipated DDJ minimization. Since the RJ is convolved with the DDJ, such system response should demonstrate a local minima for the rms jitter. For the over-damped response on the left side of Figure 3.4, the structure is similar to the first-order response.

Equation (3.15) can be simplified if we consider k = 3. For 001 and 110 sequences, (3.15) is zero since, by definition, $g(t_o)=v_{th}$. For the 101 and 010 sequences,

$$t_{c,\,DDJ} = \frac{g(t_o + T) - v_{th}}{g^{(1)}(t_o + T)}. \tag{3.16}$$

The threshold crossing time deviation described by (3.16) is positive when v_{th}-$g(t_o+T)$ is negative since denominator is the falling edge slope. If the response exhibits ringing, the numerator can be negative.

Jitter minimization occurs when there is an overshoot such that the response satisfies $v_{th}=g(t_o+T)$. This observation concurs with the criteria suggested by Gibby and Smith for

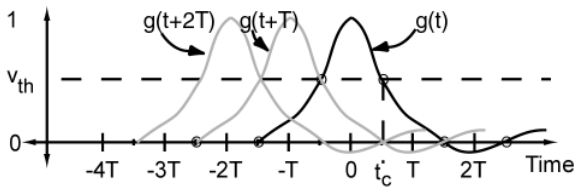

Figure 3.5 Hypothetical pulse response that minimizes jitter in a second-order system.

pulse distortionless transmission [93]. Specifically, the received pulse response should be a function, as illustrated in Figure 3.5. At the threshold crossing time, t_o, $g(t)$ reaches the voltage threshold. At $t_o + T$, the response again reaches the voltage threshold.

Microwave measurements are based on S-parameter characterization or time-domain reflectometry (TDR). For TDR/TDT, the input signal is a step response. Therefore, determining DDJ characteristics of high-speed signals from the step response can be useful in LTI channels. The pulse response of the channel is related to the step response, $s(t)$, by $s(t) = p(t) - p(t-T)$. The filtered step response is denoted $f(t)$, and

$$g(t) = f(t) - f(t-T). \tag{3.17}$$

The first-order Taylor series approximation described in (3.14) is applied to the step response. Therefore, the threshold crossing time, t_c, is modified from (3.15) and is

$$t_c = t_o + \frac{v_{th} - \sum_{n=-\infty}^{0} a_n[f(t-nT) - f(t-(n+1)T)]}{\sum_{n=-\infty}^{0} a_n[f^{(1)}(t-nT) - f^{(1)}(t-(n+1)T)]}. \tag{3.18}$$

For $k = 3$ and assuming $v_{th} = 0.5$, there are two different t_c. For the 001 and 101 sequences, $t_c = t_o$ since, by definition, $f(t_o)=v_{th}$. For the 101 and 010 sequences,

$$t_{c,\,DDJ} = \frac{1 - f(t_o + T)}{f^{(1)}(t_o + T) - f^{(1)}(t_o)}. \tag{3.19}$$

Compared to (3.16), this equation offers a different way to calculate the DDJ without relying on the pulse response.

Finally, for k = 3 sequence lengths, the first-order DDJ PDF consists of a double dirac function

$$PDF_{DDJ}(t_c) = \frac{1}{2}[\delta(t_c - t_o) + \delta(t_c - t_o - t_{c,\,DDJ})]. \tag{3.20}$$

If additional bits are considered, each delta function in (3.20) splits into two delta functions (and, correspondingly, jitter peaks) with half the probability per peak. This simple distribution has a mean and variance of

$$m_{DDJ} = t_o + \frac{t_{c,\,DDJ}}{2} \quad \text{and} \quad \sigma^2_{DDJ} = \frac{t^2_{DDJ}}{4}. \tag{3.21}$$

3.2.3 Experimental Results for First- and Second-order Filters.[1]

We demonstrate the accuracy of the DDJ predictions with a broadband amplifier and a bandwidth-limiting output filter. To measure the jitter resulting from a first-order response, a series RC filter with bandwidth of 25 MHz was placed between an amplifier and oscilloscope. The input signal is a 2^7-1 pseudo-random bit sequence (PRBS), and the threshold crossings in the data eye were observed. Since RC filters provide poor matching, the bit rate was scanned from 50Mb/s to around 150Mb/s to avoid the impact of signal reflection. Furthermore, the low bit rate reduces the impact of RJ.

The jitter peaks of the measured jitter PDF were averaged to find the two dominant peaks, and the relative time between these peaks determined the measured $t_{c,DDJ}$. Figure 3.6 plots the difference between the measured jitter peaks with the predicted values in (3.12). Two data eyes are recorded at different α to demonstrate the anticipated peak

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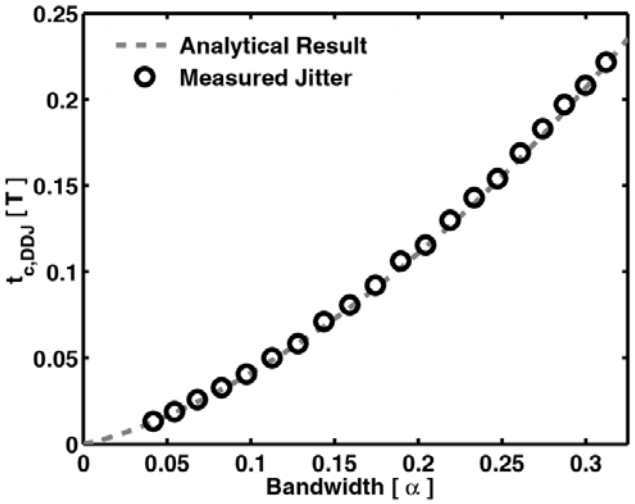

Figure 3.6 Comparison of the first-order response DDJ prediction with experimental results.

doubling in Figure 3.7. The first data eye corresponds to $f_c = 0.36\ f_b$. In Figure 3.7(b), $f_c = 0.18\ f_b$ and each of the jitter peaks has split into a second set of fast and slow jitter peaks.

The same experimental setup was used to verify the DDJ for a second-order response. A parallel inductor-capacitor (LC) filter with natural frequency of 75MHz and damping factor of 0.7 was placed between the amplifier and the oscilloscope and the bit rate was scanned. Figure 3.8 demonstrates the predicted and measured DDJ. As the bit rate

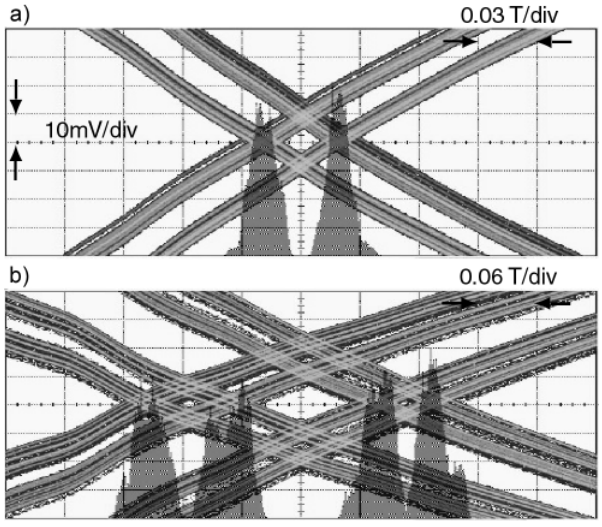

Figure 3.7 Data eyes for first-order response at (a) α = 0.1 and (b) α = 0.31 from Figure 3.6.

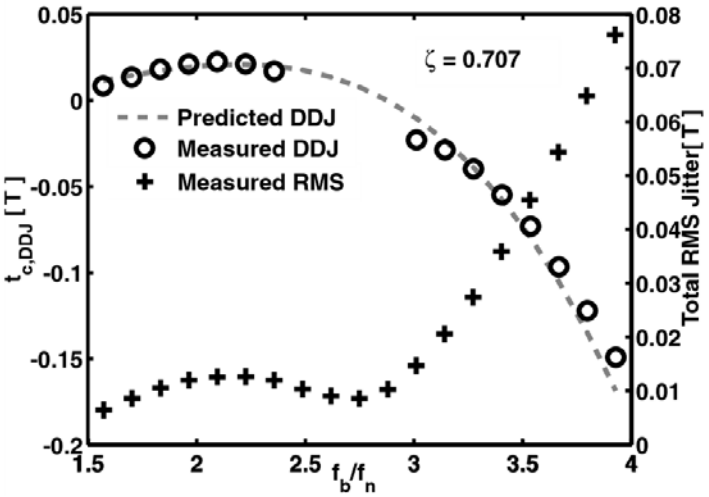

Figure 3.8 Comparison of second-order prediction and measured DDJ on the left axis and corresponding rms jitter on the right axis.

increases, the DDJ increases at first, but then begins to decrease. Near the slow and fast response intersection, the DDJ is undetectable, and these points have been neglected. The negative values of $t_{c,DDJ}$ do not mean that the DDJ is negative but that the relative positions of $E[t_c|a_{-1} = a_{-2}]$ and $E[t_c|\ a_{-1} \neq a_{-2}\ ]$ switch. Therefore, the total jitter is always non-negative, but the negative values stress the dynamics of the response. The zero

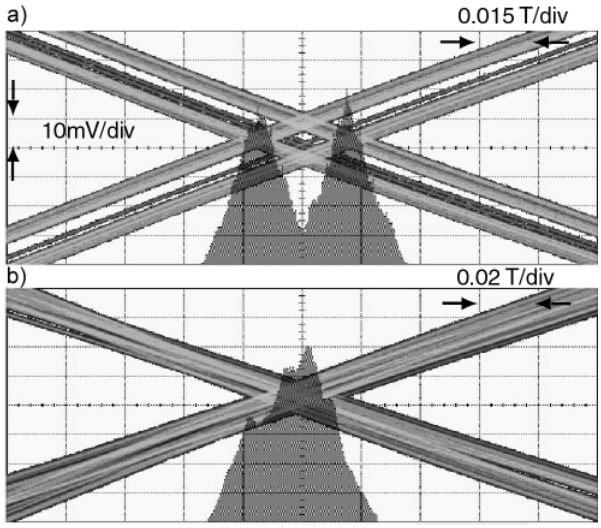

Figure 3.9 Threshold crossing eye diagram with superimposed histogram at normalized bit rate of (a) 2 and (b) 2.9 from Figure 3.8.

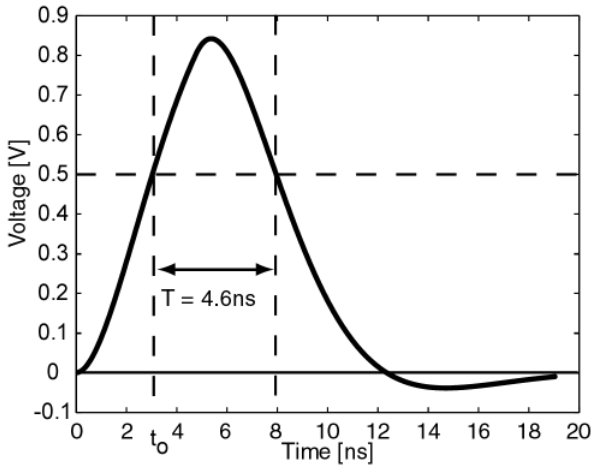

Figure 3.10 Received pulse response at the point of the jitter minimization and the measured waveform.

crossing of the curve corresponding to the minimum DDJ is also a local minimum of the total jitter, as illustrated on the second axis in Figure 3.8. This minimum provides a guideline to design low bandwidth blocks and still achieve low timing jitter. It is notable that the bit rate must be cut by nearly 40% to reach the same rms jitter. Figure 3.9 demonstrates the transitions of the data eye diagrams at two different bit rates. The bit rate of the first eye diagram is twice the bandwidth. The bit rate of the second eye diagram is nearly three times the bandwidth. Clearly, the superimposed jitter histogram reflects the lower rms jitter at the higher bit rate.

Finally, the pulse response is plotted to see how the jitter minimization agrees with the prediction in Figure 3.10. The second-order filter with the given parameters was simulated with a 010 sequence. To satisfy $g(t_o+T) = v_{th}$, we determine that T = 4.6ns. Clearly, this indicates that the bit rate that satisfies the zero jitter condition is 218Mb/s. From Figure 3.8, this point is at $2.8f_n$ = 210Mb/s. Therefore, we have anticipated from the pulse response with good accuracy the zero jitter condition.

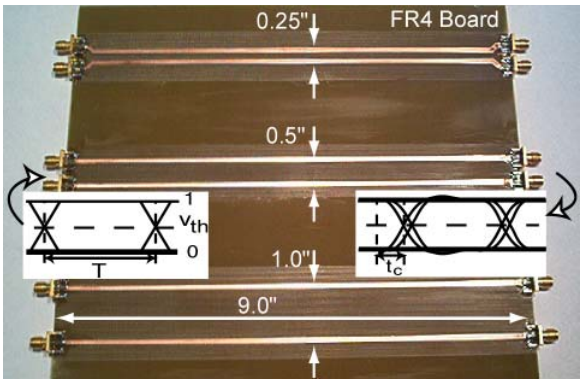

Figure 3.11 FR-4 transmission line experimental set-up.

3.2.4 Experimental Results for Transmission Lines[1]

Transmission lines do not behave as a simple first- or second-order filter. Consequently, it is important to demonstrate how our predictions can be used to verify the DDJ measured in bandwidth-limited transmission lines. The FR4 board shown in Figure 3.11 has three 9” coupled microstrip lines separated by 0.25”, 0.5”, and 1”. Network analysis of the lines is plotted in Figure 3.12. S_{21} indicates that the 3dB bandwidth is 2.5GHz for the 0.25” lines and 3.8GHz for the 0.5” and 1” lines. The measured step responses are also plotted in Figure 3.12 and are used to calculate the DDJ

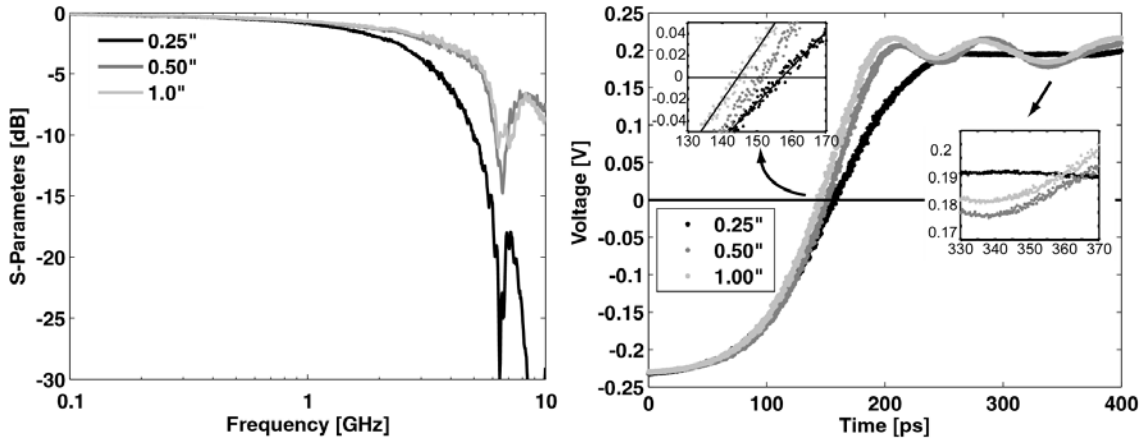

Figure 3.12 S-parameters and step response for transmission lines constructed in Figure 3.11.

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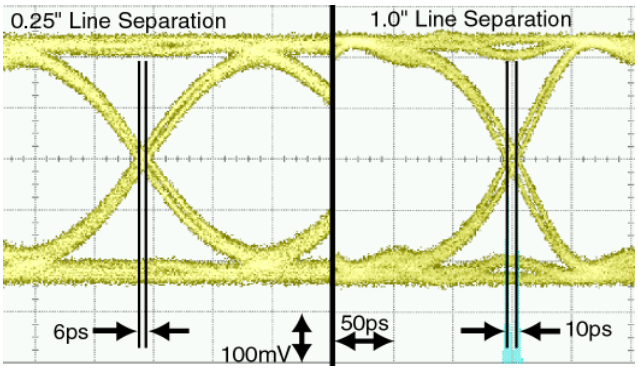


Figure 3.13 Data-dependent jitter measured in FR4 coupled transmission line.

in Table 3.1. The 0.25” lines feature a frequency null near 9GHz, and the step response is slowest. The negative value for the DDJ indicates that the 101 sequence is faster than the 001 sequence. Interestingly, while the 0.25” line step response in Figure 3.12 is slowest, the DDJ of this line calculated in Table 3.1 is the smallest. This emphasizes the importance of the slope after one period. Figure 3.13 illustrates the data eyes at 5Gb/s for the 0.25” and 1.0” lines. The DDJ values are measured from the eye and compared to the measurements from the eyes in Table 3.1. The DDJ measured from the data eyes agrees with the predicted DDJ value in (3.19) with error under 15%. Higher-order modeling of the DDJ from the Taylor series can improve the accuracy of the prediction.

Table 3.1: Calculated and Measured DDJ for FR4 Coupled Microstrip

Line	$f(t+T)$	$f^{(1)}(t)$	$f^{(1)}(t+T)$	**Predicted** $t_{c,DDJ}$	**Measured** $t_{c,DDJ}$	**Error**
0.25”	0.98 V	3.4e9 V/s	-9.8e7V/s	-5.1ps	-6ps	15%
0.5”	0.95V	4.2e9 V/s	5.7e8 V/s	-11ps	-10ps	10%
1”	0.96 V	4.5e9 V/s	2.7e8 V/s	-8.8ps	-10ps	12%

The experimental results for first- and second-order systems as well as for transmission lines demonstrates how we can predict the properties of DDJ and link them to actual measured data eye signal integrity. This is important in understanding the role of deterministic jitter in the overall bit-error rate performance of serial links.

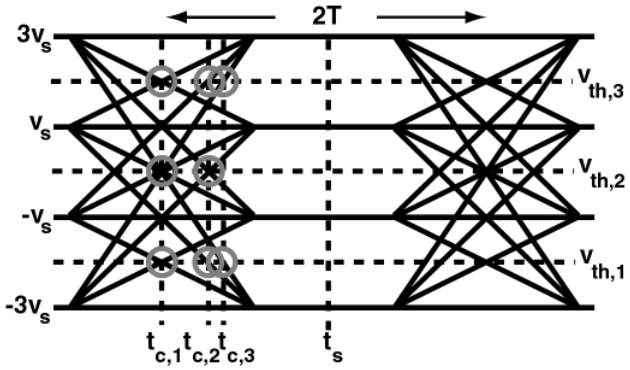


Figure 3.14 Data eye for 4-PAM signal transmission.

3.3 Data-Dependent Jitter in 4-PAM

Higher-order modulation techniques are often considered when facing bandwidth limitations. One method of improving the capacity is to transmit 4 level PAM (4-PAM). This relies on taking advantage of the linearity of the channel to transmit larger amplitudes over twice the signal period compared to 2-PAM NRZ transmission discussed in the previous sections. A 4-PAM data eye is shown in Figure 3.14. The complication of the 4-PAM scheme comes from the need for various voltage thresholds for the detection of the different signal levels. Consequently, three signal transitions occur between the four different allowable signal levels. This causes an inherent data-dependent jitter in 4-PAM. In Figure 3.14, three separate threshold crossing times are circled in gray. Each inherent threshold crossing time, $t_{c,m}$, is identified for a transition through m-levels. Consequently, using the 4-PAM scheme trades the higher voltage levels for more transition ambiguity.

Each quaternary level, $a_k = \{0,1,2,3\}$, is assumed to be equally probable. Therefore, there are $4^2 = 16$ different sequence combinations for $k = 2$. Of these, twelve have data transitions, implying that the transition density is 75%. This is an important difference from 2-PAM, where the uncoded transition density is 50%.

We encounter ambiguity for constructing PDFs describing DDJ in 4-PAM. From a measurement standpoint, we can only measure a jitter histogram around a particular

threshold level. Two calculations are possible: measuring at $v_{th,1}$(or, equivalently, $v_{th,3}$) and $v_{th,2}$. For the middle voltage threshold, $v_{th,2}$, the peaks can be deduced geometrically and are listed from left to right:

$$PDF_{DDJ,\,2}(t_c) = \frac{1}{4}[\delta(t_c - (2t_{c,\,1} - t_{c,\,2})) + 2\delta(t_c - t_{c,\,1}) + \delta(t_c - t_{c,\,2})]. \qquad (3.22)$$

When we look at the bottom voltage threshold, $v_{th,1}$, there are five peaks:

$$PDF_{DDJ,\,1}(t_c) = \frac{1}{6}\left[\begin{array}{l}\delta(t_c - (2t_{c,\,1} - t_{c,\,3})) + \delta(t_c - (2t_{c,\,1} - t_{c,\,2}))\\ + 2\delta(t_c - t_{c,\,1}) + \delta(t_c - t_{c,\,2}) + \delta(t_c - t_{c,\,3})\end{array}\right]. \qquad (3.23)$$

Neither of these PDFs correctly identifies the BER due to DDJ since the desired threshold crossing times is for a given voltage threshold and, consequently, for the given symbol, a_0. While it cannot be directly measured on an oscilloscope, the PDF for calculating the BER is

$$PDF_{DDJ,\,BER}(t_c) = \frac{1}{6}[3\delta(t_c - t_{c,\,1}) + 2\delta(t_c - t_{c,\,2}) + \delta(t_c - t_{c,\,3})]. \qquad (3.24)$$

This reflects the fact that the transitions across one level are more probable than transitions across either two or three levels. This summarizes the modeling of the inherent DDJ PDF for 4-PAM. Now we can also investigate the impact of bandwidth limitations on these threshold crossing times.

The DDJ in 4-PAM modulation schemes is analyzed through the application of (3.8). Since the data coefficients in this equation have been derived generally, we can apply the quaternary levels without any adjustment to the equation. However, the voltage thresholds change depending on which bit is detected. Thus, the general definition of the voltage threshold for PAM is

$$v_{th} = a_0 + \frac{1}{2}\text{sign}[a_{-1} - a_0]. \qquad (3.25)$$

Substituting this into the denominator of (3.8) allows us to make a map of the threshold crossing times as a function of bandwidth as we did for 2-PAM in Figure 3.2. This is shown in Figure 3.15, where the same time constant, τ, for the filter bandwidth is assumed

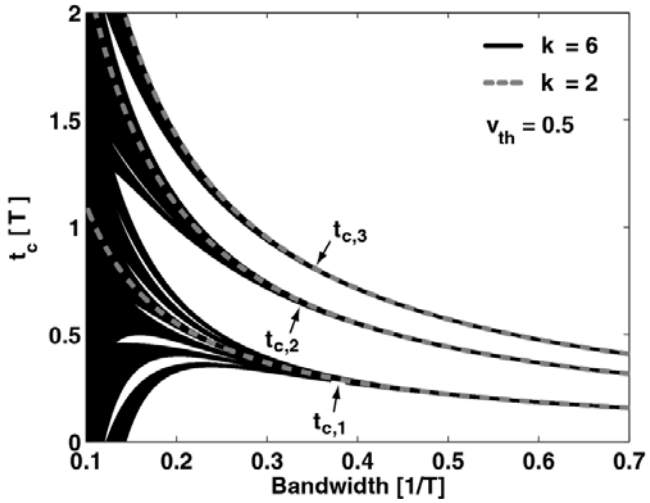


Figure 3.15 Normalized threshold crossing time for 4-PAM with respect to system bandwidth.

but the bit period is extended to $T = 2$ to maintain the same data rate. The plot is demonstrated for $k = 2$ where the effect of bandwidth does not cause DDJ due to the penultimate symbol. In this case, the three threshold crossing times are the inherent deviations due to the existence of the three voltage thresholds. The change in these threshold crossing times is related to the change in slope of the rising and falling transitions of the data. For $k = 6$, the effect of DDJ over several symbols is apparent. Even at large bandwidths, the threshold crossing times begin to spread over a large range of the bit period. Notably, the spreading is most prominent on the fast transitions closest to the x-axis, while the spreading is less pronounced on the slow transitions. Comparing Figure 3.15 to the 2-PAM plot in Figure 3.2, we notice that the bandwidth over which 4-PAM is sustainable is lower than 2-PAM. In fact, the DDJ limits the operation of 4-PAM to $\alpha = 0.167$. This is a bandwidth of $0.285f_s$, the symbol rate, or $0.142f_b$.

3.4 Duty Cycle Distortion

Our definitions for DDJ have relied on an appropriately chosen voltage threshold, $v_{th} = 0.5$, that is placed at the intersection of the rising and falling edges. In real receivers, there exist voltage offsets and device mismatches that do not allow exact sampling at the

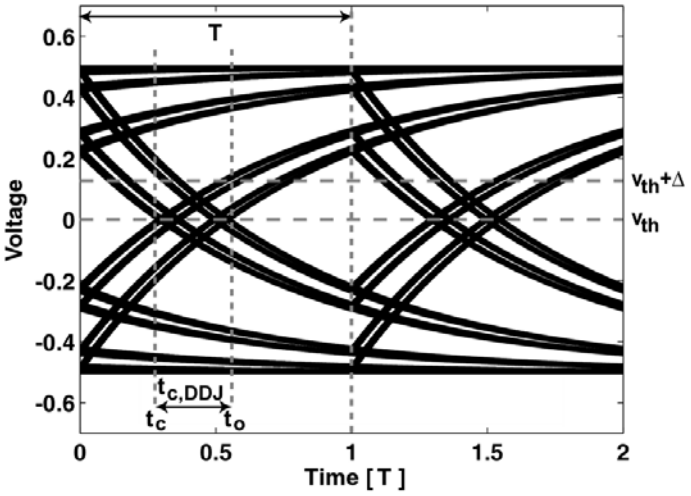


Figure 3.16 The effect of a voltage threshold offset is to introduce additional timing ambiguity in the data eye.

voltage threshold. However, in situations where the voltage threshold is offset, additional timing ambiguity is introduced by the variation between the rising and falling edges. In Figure 3.16, the offset voltage threshold intersects a greater range of threshold crossing times. Therefore, the rms and peak-to-peak jitter will increase. The spread of transition times at the threshold is larger when a voltage offset is present. This voltage threshold offset causes duty-cycle distortion (DCD) jitter.

The DCD PDF represents the statistical behavior of the threshold crossing times in the presence of the voltage threshold offset. For k = 3, the peaks of the DDJ PDF in (3.12) are separated according to whether the transition is a rising or falling edge. For simplicity, we assume $\alpha^2 \sim 0$.

$$PDF_{DCD}(t_c) = \begin{aligned} &\frac{1}{4}\delta\left(t_c - \tau\ln\left[\frac{1}{v_{th}}\right]\right) + \frac{1}{4}\delta\left(t_c - \frac{\tau}{2}\ln\left[\frac{(1-\alpha)}{v_{th}}\right]\right) \\ &+ \frac{1}{4}\delta\left(t_c - \tau\ln\left[\frac{1}{(1-v_{th})}\right]\right) + \frac{1}{4}\delta\left(t_c - \frac{\tau}{2}\ln\left[\frac{(1-\alpha)}{(1-v_{th})}\right]\right) \end{aligned} \tag{3.26}$$

If v_{th} = 0.5, two of the four peaks will overlap, and the DCD PDF is identical to the DDJ described in (3.12). The mean and variance are

$$m_{DCD} = \frac{\tau}{2} \cdot \ln\left[\frac{1-\alpha}{v_{th}(1-v_{th})}\right] \quad \text{and}$$
$$\sigma^2_{DCD} = \frac{\tau^2}{4}\left[\left(\ln\left[\frac{v_{th}}{1-v_{th}}\right]\right)^2 + (\ln[1-\alpha])^2\right]. \tag{3.27}$$

The variance for the DCD PDF indicates that the effect of the voltage threshold and the effect of the bandwidth are separable.

For the general LTI response, the effect of the voltage threshold offset changes the DDJ PDF to

$$PDF_{DCD}(t_c) = \frac{1}{4}\delta\left(t_c - t_o + \frac{\Delta}{g'(t_o)}\right) + \frac{1}{4}\delta\left(t_c - t_o - t_{c,DDJ} + \frac{\Delta}{|g'(t_o+T)|}\right)$$
$$+ \frac{1}{4}\delta\left(t_c - t_o - \frac{\Delta}{g'(t_o)}\right) + \frac{1}{4}\delta\left(t_c - t_o - t_{c,DDJ} - \frac{\Delta}{|g'(t_o+T)|}\right), \tag{3.28}$$

which reduces to (3.20) if Δ=0. The peaks are listed in order of the two falling edges and the two rising edges. The $t_{c,DDJ}$ is the same definition used in (3.16), where v_{th} = 0.5 and describes the minimum amount of DDJ. Therefore, the mean and variance are

$$m_{DCD} = t_o + \frac{t_{c,DDJ}}{2} \quad \text{and}$$
$$\sigma^2_{DCD} = \left(\frac{t_{c,DDJ}}{2}\right)^2 + \frac{\Delta^2}{2}\left(\frac{1}{g'(t_o)^2} + \frac{1}{|g'(t_o+T)|^2}\right). \tag{3.29}$$

Again, DCD can be isolated probabilistically from DDJ. The variances of the DDJ and the DCD add in (3.27) and (3.29). This implies that DDJ and DCD are uncorrelated. The DCD effect is unchanged regardless of how much DDJ is present. The voltage offset, $v_{th}+\Delta$, creates an additional source of jitter that is independent from the bandwidth limitation described by DDJ. The variance of DCD jitter is

$$\sigma^2_{DCD} = \frac{\Delta^2}{2}\left(\frac{1}{g'(t_o)^2} + \frac{1}{g'(t_o+T)^2}\right). \tag{3.30}$$

Comparing (3.16) and (3.30), the relative impact of DCD jitter and DDJ can be compared. The DCD jitter dominates if $|0.5 - g(t_o)|$ is much smaller than $|\Delta|$. Consequently, a small voltage threshold offset can dominate the impact of DJ.

3.5 Markov Sampling of Threshold Crossing Times

Using the unique relationship between the threshold crossing times and bit sequences, a Markov chain is developed to sample each threshold crossing time and demonstrate a time domain description of data-dependent jitter. This Markov chain description also determines the jitter power spectral density for data-dependent jitter. We use the results of the threshold crossing time calculation from (3.8), where each data sequence is mapped to a particular threshold crossing time but the following analysis can be generalized.

A sequence of k bits is a state $S = \{a_{-k+1}...a_{-1}a_0\}$. Half of these states have transitions at the a_0 bit and are a subset, S_c, of S that have threshold crossing times. An element of S, S_i, represents the state with decimal representation i. For example, S_3 is the sequence 011, which is not a member of S_c. We construct the following state transition matrix for S, where we assume that all data sequences are equiprobable.

$$\bar{T} = \begin{bmatrix} 1 & 1 & 0 & 0 & \dots & 0 & 0 \\ 0 & 0 & 1 & 1 & \dots & 0 & 0 \\ \dots & \dots & \dots & \dots & \dots & \dots & \dots \\ 1 & 1 & 0 & 0 & \dots & 0 & 0 \\ 0 & 0 & 1 & 1 & \dots & 0 & 0 \\ \dots & \dots & \dots & \dots & \dots & \dots & \dots \\ 0 & 0 & 0 & 0 & \dots & 1 & 1 \end{bmatrix} \tag{3.31}$$

The dynamics from state i to state j are expressed in the state transition matrix. For instance, $T_{1,2}$ is the state transition from S_1 to S_2, i.e. 001 to 010. A pictorial summary of

the state progression for the threshold crossing time is shown in Figure 3.17. When starting in any state, two states are possible depending on whether the next bit is a one or zero. There are two highlighted states corresponding to the fast and slow timing deviations.

We can extend the idea of the state transition matrix by introducing a state probability transition matrix, $P_{i,j}$, to describe the probability of moving from S_i to S_j. For this work, we assume that a logical one or zero is equally probably and, consequently, the transition probability is $p = 0.5$. Therefore,

$$\bar{P} = p\bar{T}. \tag{3.32}$$

3.5.1 Time Domain: Cycle-to-Cycle Behavior

The Markov model is particularly useful for calculating cycle-to-cycle and long term jitter behavior of DDJ. Since the data sequence is not periodic, such as a clock, we define cycle-to-n^{th}cycle jitter from (2.43) as the difference in the threshold crossing time deviations of *adjacent* transitions. Since transitions occur randomly, two transitions may be separated by an n bit interval. Nevertheless, transition sensitive circuits are unaware of the number of bit intervals that have passed. Therefore,

$$\Delta t_c[nT] = t_c[(m+n)T] - t_c[mT]. \tag{3.33}$$

The variance of the cycle-to-n^{th}cycle jitter is

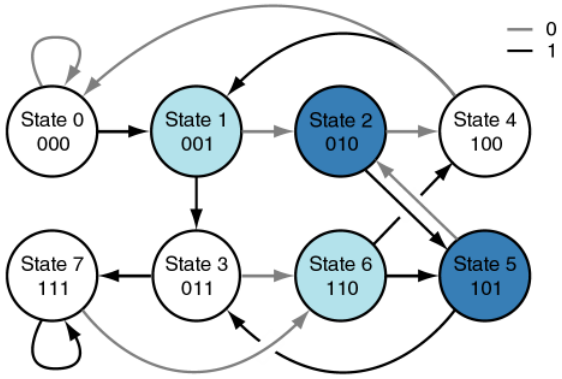


Figure 3.17 The state space progression for the threshold crossing times where $k = 3$. The fast events are highlighted in dark blue while the slow states are highlighted in light blue.

$$\sigma_{cc}^2[n] = E[\Delta t_c^2[nT]] - (E[\Delta t_c[nT]])^2 . \tag{3.34}$$

This variance can be calculated using the state transition notation. We are interested in conditioning the variance on the number of bit intervals that will pass. Therefore we want to find the difference in threshold crossing times:

$$\Delta t_c[nT] = (t_j - t_i)\big|n , \tag{3.35}$$

where t_i and t_j are the adjacent threshold crossing times for states i and j conditioned over an n bit interval. We can easily determine whether t_i leads to t_j by examining $T_{i,j}^n$. However this will calculate all the transitions that occur in the n bit interval. Instead, this calculation should calculate only the adjacent transitions. Therefore, the dynamics must be filtered to stop the progression of states that have reached a transition. We construct a transition halting matrix, $\bar{H}$, based on two conditions: i) H_i is zero for any S_i that is not an element of S_c and ii) $H_{i,j}$ is zero for any state S_j that is an element of S_c. All other elements are one. The first condition ensures that we do not find transitions for states that did not initially have transitions, while the second condition stops the state progression once we reach a transition. Therefore, the transition from S_i to S_j is captured by

$$\bar{C} = \begin{cases} \bar{T}^0 & \text{for } n = 0 \\ \bar{T}^1 & \text{for } n = 1 \\ \bar{T}.\bar{H}\bar{T} & \text{for } n = 2 \\ \bar{T}.\bar{H}\bar{T}.\bar{H}\bar{T} & \text{for } n = 3 \\ \bar{T}.\bar{H}\bar{T}.\bar{H}\bar{T}.\bar{H}\bar{T}\ldots & \text{for higher } n \end{cases} , \tag{3.36}$$

where the operation, *T.H,* is the element-by-element array multiplication and *HT* is a normal matrix multiplication. Now that the state progression for the cycle-to-n^{th}cycle behavior is described, we can calculate the mean:

$$E[(t_j - t_i)\big|n] = E[E[(t_j - t_i)\big|n, S_i]] = \sum_i Pr[S_i](E[C_{i,j}^n t_i] - t_i) , \tag{3.37}$$

where $Pr[S_i]$ is the probability operator and, for uncoded data, is p. Finally, the cycle-to-n^{th}cycle variance is

$$\sigma_{cc}^2[n] = p\sum_i (E[C_{i,j}^n t_i] - t_i)^2 - p^2\left(\sum_i (E[C_{i,j}^n t_i] - t_i)\right)^2. \quad (3.38)$$

This calculation is easily performed for the analytic expressions for the threshold crossing time in (3.8) and tabulated in Appendix A. Consequently, we can plot the cycle-to-cycle behavior for n bit periods. If we want to make the same calculation for only rising (or falling) edges, the transition halting matrix is modified to stop only states that progress from one rising edge to another.

Finally, the total cycle-to-cycle behavior can be calculated from the cycle-to-n^{th}cycle variance. The total cycle-to-cycle behavior just averages the probability of a transition after n periods. Therefore,

$$\sigma_{cc}^2 = \sum_{n=0}^{\infty} p^n \sigma_{cc}^2[n]. \quad (3.39)$$

3.5.1.1 Rising and Falling Edge Sensitivity

In Figure 3.18 the cycle-to-n^{th} cycle variance and total cycle-to-cycle behavior is demonstrated for rising and falling edges. The variance is zero for zero bit lag and increases to a maximum value after the first period. This occurs since it is probable that we move directly from a slow transition into a fast transition. After a two bit interval, the variance drops to about half the value. This occurs since it becomes likely that we move from a slow transition to a slow transition. For higher intervals the variance flattens out. The effect of an offset voltage threshold is also shown and causes a uniform shift in the variance. The total cycle-to-cycle variance is plotted across a large range of bandwidths and is compared to the variance of the absolute jitter. Notably, the voltage threshold offset does not affect the behavior significantly at low bandwidths, where the DDJ is a stronger effect than DCD, but at higher bandwidths the DCD creates a jitter floor.

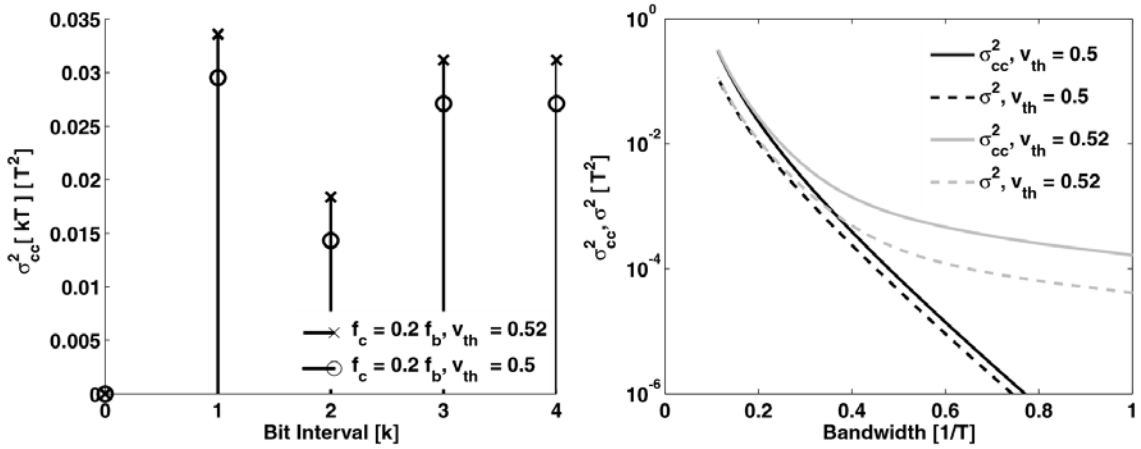


Figure 3.18 The cycle-to-n^{th} cycle and cycle-to-cycle behavior of the first-order response with and without a voltage threshold offset.

3.5.1.2 Rising Edge Sensitivity

In Figure 3.19 the variances are demonstrated for rising edge sensitivity. Since a rising edge cannot be followed by a rising edge, the one bit interval does not have a cycle-to-cycle contribution. After two bit intervals the variance is small because the data sequence that has two rising edges in this interval is progressing from a fast transition to

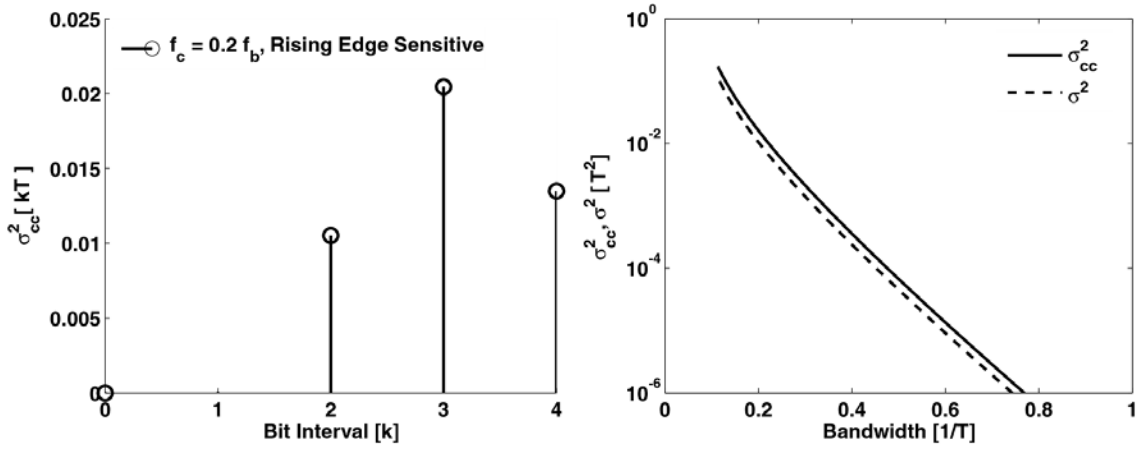


Figure 3.19 The cycle-to-n^{th} cycle and cycle-to-cycle behavior of the first-order response for rising edge sensitivity

another fast transition. The variance is maximum for the third bit interval and reaches a fixed value at greater bit intervals. The final value for the cycle-to-n^{th} cycle variance is roughly half of the jitter for the rising and falling edge sensitivity. Plotting the total cycle-to-cycle behavior demonstrates similar behavior to the earlier situation in Figure 3.18. However, this time the behavior is not sensitive to the voltage threshold offset.

3.5.2 Frequency Domain Interpretation: Jitter Power Spectral Density

The threshold crossing times are mapped alternately as threshold crossing phases:

$$\phi_i = 2\pi\frac{t_i}{T}. \tag{3.40}$$

The jitter PSD is the Fourier transform of the autocovariance of the phase, $R_\phi[nT]$, of the data transitions. For stationary processes, the piecewise representation of the autocovariance function is fourier-transformed to the frequency domain to find the PSD. The PSD is transformed to continuous time PSD in the PLL through the sampling process in the phase detector [75].

$$S_\phi(f) = T\omega_o^2\left(\frac{\sin(\pi fT)}{\pi fT}\right)^2 \sum_{n=-\infty}^{\infty} R_\phi[nT]e^{-j2\pi fnT} \tag{3.41}$$

The filter bandwidth of the PLL is much smaller than 1/T and (3.41) is approximated as

$$S_\phi(f) = T\omega_o^2 \sum_{n=-\infty}^{\infty} R_\phi[nT]e^{-j2\pi fnT}. \tag{3.42}$$

$R_\phi[0]$ is the expected power of the jitter. If only $R_\phi[0]$ is significant, then the jitter PSD is characterized as a white noise floor, i.e. $S_\phi(f)=T\omega_o{}^2R_\phi[0]$. In general, the phase autocovariance is

$$R_\phi[nT] = E[(\phi_i - m_\phi)(\phi_j - m_\phi)] = \left(\frac{2\pi}{T}\right)^2 (E[t_i t_j | n] - m_t^2), \tag{3.43}$$

where we have related the phases, ϕ_j and ϕ_i, that occur n bits apart and the mean of the phase, m_ϕ, to the threshold crossing times and the mean of the threshold crossing times (3.5). The conditioned expectation for the transition autocorrelation is

$$E[t_i t_j | n] = \sum_{S_i \in S_c} E[t_j t_i | t_i, n] Pr[t_i] = \sum_{S_j \in S_c} \sum_{S_i \in S_c} P_{ij}^n t_j t_i Pr[t_i]. \tag{3.44}$$

Now we have calculated the autocorrelation in (3.43) in (3.44). After n periods the probability of each state is given by the nth power of the $P_{i,j}$. However, any phase is equiprobable after n exceeds the sequence length, k. Therefore, after k bits no covariance exists for the phases associated with Markov chain generated data and the autocovariance is zero.

$$R[nT] = 0 \qquad n \geq k \tag{3.45}$$

Now consider the different cases for $S_\phi(f)$.

3.5.2.1 Rising and Falling Edges Sensitivity

To begin, we calculate the autocovariance terms individually. $R_\phi[0]$ is

$$R_\phi[0] = \left(\frac{2\pi}{T}\right)^2 \sigma_{DDJ}^2, \tag{3.46}$$

where the variance of the DDJ was calculated in (3.5). Simplifying the expression for k = 3, the variance calculated in the Appendix is

$$R_\phi[0] = \frac{1}{4}\left(\frac{2\pi\tau}{T}\right)^2 \left[(\ln[1-\alpha])^2 + \left(\ln\left[\frac{v_{th}}{1-v_{th}} \right] \right)^2 \right]. \tag{3.47}$$

Again, (3.47) is minimized for v_{th} = 0.5, and deviations from this optimal point increase the $R_\phi[0]$. Additionally, reducing the bandwidth increases this term. For k = 3, the one period lag autocovariance, $R_\phi[T]$, is zero. Furthermore, higher order terms are also zero because of (3.45). This is not generally true. If k = 4, $R_\phi[T]$ is non-zero and is given by

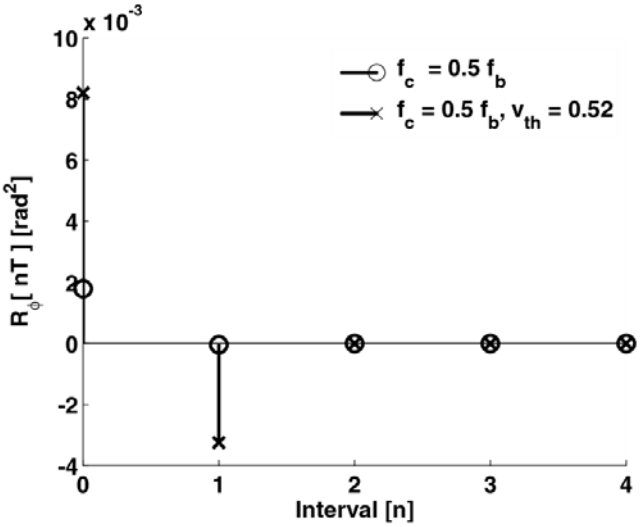


Figure 3.20 Autocovariance for data transition phase in a first-order system.

$$R_{\phi}[T] = \frac{1}{32}\left(\frac{2\pi\tau}{T}\right)^2 \left[\begin{array}{l} -14\left(\ln\dfrac{v_{th}}{1-v_{th}}\right)^2 + \ln(1-\alpha)\ln(1+\alpha) \\ \qquad + \ln(1-\alpha+\alpha^2)\ln\left(\dfrac{1-\alpha+\alpha^2}{1-\alpha^2}\right) \end{array} \right]. \tag{3.48}$$

Examination of (3.48) reveals that $R_{\phi}[T]$ is negative for all α since $\ln(1 - \alpha)$ is negative.

Figure 3.20 examines the autocovariance with $k = 4$. The $R_{\phi}[nT]$ terms are plotted with respect to bandwidth in black and voltage threshold in gray. The change in $R_{\phi}[0]$ is evident, and $R_{\phi}[T]$ demonstrates a small negative value as the bandwidth drops. Therefore, the PSD of DDJ, in this case, is primarily a white noise. For voltage threshold variations, $R_{\phi}[T]$ increases dramatically, implying that rising and falling edge-sensitive phase detection circuits are particularly susceptible to threshold variation.

3.5.2.2 Rising Edges Only

For rising edges alone, we need to calculate (3.46) for only rising edges. Therefore, the variance and mean in this expression are different. For $k = 3$,

$$R_{\phi}[0] = \frac{1}{8}\left(\frac{2\pi\tau}{T}\right)^2 [\ln(1-\alpha)]^2 . \tag{3.49}$$

This result is a factor of two smaller than (3.47) when v_{th} = 0.5. Additionally, this expression does not depend on the voltage threshold. $R_{\phi}[T]$ is identically zero since it is impossible to go from rising edge to rising edge in one bit period.

$$R_{\phi}[0] = 0 \tag{3.50}$$

For k = 3, $R_{\phi}[2T]$ and the higher-lag autocovariance terms are zero from (3.45).

Since $R_{\phi}[nT]$ is not dependent on the threshold voltage, there is an advantage to implementing phase detectors that are sensitive only to rising (or falling) edges. A primary difference is that $R_{\phi}[0]$ is one-half of the value for the rising and falling edge detection.

3.5.2.3 Jitter Power Spectral Density Simulations

Ten thousand threshold crossing samples were collected for the frequency domain analysis, and the spectral density was calculated using Welch's method. The jitter performance was simulated using a Simulink model for a pseudo-random bit sequence (PRBS) generator and a first-order LTI system. The data are filtered with a first-order filter of bandwidth of 50% of the bit rate. The statistics of the threshold crossing times are collected based on sensitivity to both the rising and falling edges and just the rising edges.

The PSD of the DDJ is plotted in Figure 3.21 for rising and falling edge sensitive detection. The theoretical results are calculated from the Fourier transform of (3.47) and (3.48) are compared to the simulated PSD. The curves demonstrate agreement between the theoretical and simulated results. For v_{th} = 0.5, the noise is white. When v_{th} = 0.52, the noise is colored and demonstrates that the PSD is a strong function of the voltage threshold as anticipated from (3.48). This coloring is an important result for the Markov description.

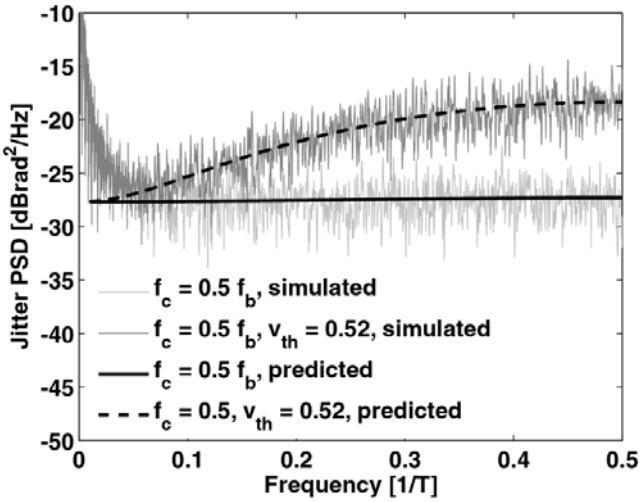


Figure 3.21 Jitter power spectral density for first-order response with rising and falling edge sensitivity.

The PSD for rising edge sensitive phase detection is plotted in Figure 3.22. The theoretical results are calculated from (3.49). The noise is perfectly white over the entire range and increases, as expected, with lower bandwidth. For the same bandwidth, rising edge sensitive circuits feature 3dB lower spectral density. Since the PSD for this situation is insensitive to v_{th}, the noise coloring that occurred for the rising and falling edge sensitive detection does not occur.

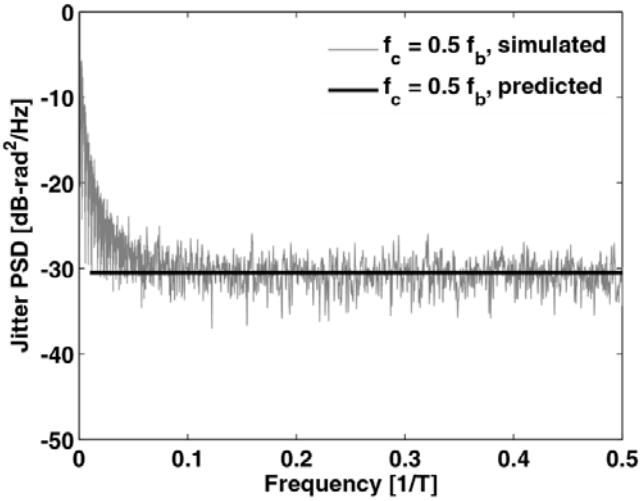


Figure 3.22 Jitter spectral density for first-order response with rising edge sensitivity.

3.5.3 Circuit Implications: Hogge Phase Detector

Markov modeling provides intuition about improving circuit robustness to data-dependent jitter. Notably, cycle-to-cycle jitter and the jitter PSD both indicate that the one-bit lag has a large unnecessary variance. The cycle-to-cycle jitter was reduced for circuits sensitive to only rising edges. In Figure 3.23, a Hogge phase detector is shown on the right and was proposed by DeVito to remove internal pattern dependence [94][95]. This circuit uses the comparison of half-period pulses created from the input data, $x1$, and compares them with half-period pulses created from the recovered clock, $x2$-$x4$. The difference, $x1$-$x2$-$x3$+$x4$, gives the phase error. Any phase variation on the rising and falling edges of the data is translated to a phase error as shown by the highlighted regions. This rising and falling edge sensitivity is undesirable from the results of our discussion in the previous sections. The Hogge phase detector can be modified to make it sensitive to only rising edges by dividing down the data signal at the input. Consequently, the phase detection is only calculated every time there is a rising edge (or alternatively on a falling edge). The disadvantage of this implementation is that the transition density is cut in half. Furthermore, the data is retimed after any of the latches in the left schematic. In the right

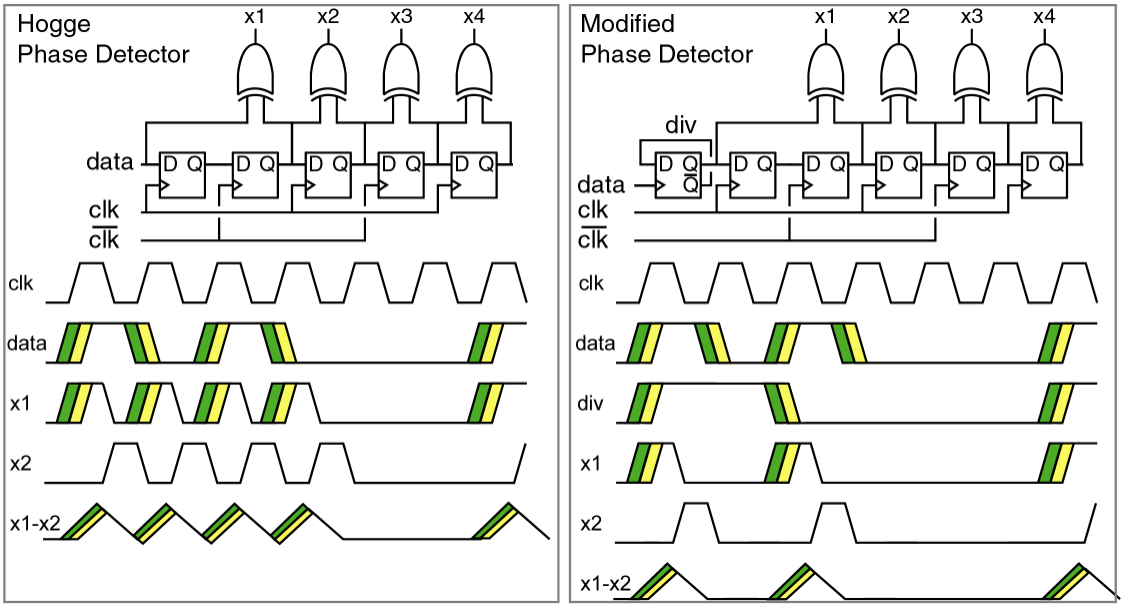


Figure 3.23 Modifications to a Hogge phase detector to rejection jitter. The original phase detector is sensitive to rising and falling edges. The modified circuit is only sensitive to rising edges.

schematic, the data can not be retimed directly with the phase detector, requiring additional latches and circuitry for data retiming. While this analysis has been performed for a Hogge phase detector, similar results hold for Alexander or bang-bang phase detectors [96][97]. In the next chapter we discuss equalization techniques that can correct the data-dependent jitter before affecting phase-detector operation.

3.6 Summary

This chapter relates the modeling for DDJ with a probability density function to a channel response. The analysis of DDJ begins with studying the threshold crossing times for LTI systems. For a first-order system, the threshold crossing times can be calculated with a closed form solution and are plotted as a function of bandwidth. We find that the behavior of the threshold crossing times is to spread with increasing bandwidth. This spreading is self-similar so long as the bandwidth is not overly-constrained. The basic properties of DDJ in a first-order system are used to extract an accurate probabilistic model for DDJ. For higher-order LTI systems, we introduce simulation and series approximations to determine the DDJ. We demonstrate that a second-order system provides an inherent trade-off between damping and natural frequency that allows for jitter minimization. A step-response approach is introduced for studying microwave transmission lines. This analysis is compared to experimental evidence in amplifiers featuring first- and second-order responses as well as in transmission lines. We find that the approximations can predict the observed DDJ within 15%.

The analysis is extended to study 4-PAM modulation schemes. This scheme is particularly interesting because it relies on multiple voltage thresholds to detect each symbol. Consequently, there is an inherent threshold crossing time deviation depending on what symbols the signal moves between. We demonstrate PDF calculations consistent with measurement as well as BER calculation. Additionally, we extend the first-order analysis to 4-PAM and directly compare the DDJ trade-offs to 2-PAM.

Finally, the analysis is extended to study the impact of voltage threshold offsets on deterministic jitter. The resulting DCD PDF shows that the DCD can be treated separately as an independent source of jitter.

The unique relationship between the threshold crossing times and the data sequence motivates the construction of a Markov model to study circuit performance under the influence of DDJ. This model helps determine the cycle-to-cycle behavior, and jitter PSD is compared to simulations carried out with Matlab. Finally, we provide an example of the Markov model that can improve the design of phase detector circuits by eliminating the sensitivity to DDJ.

Chapter 4 Equalization of Data-Dependent Jitter

4.1 Introduction

Bandwidth demands are driving circuit speeds above conventional package and transmission line bandwidths. Increasingly, the channel behavior must be considered and compensated appropriately to reach the highest information capacity. Significant attention has recently been dedicated towards pushing data rates over legacy FR-4 towards 10Gb/s [31][32][99]. Noise considerations dictate the choice of equalization technique. While traditional choices for channel compensation manage the effect of intersymbol interference (ISI) on the data eye [47], this chapter discusses compensation of data-dependent jitter (DDJ). Jitter represents timing deviations of the data transitions when compared to a reference clock and reduces the horizontal opening of the data eye, lowering the bit error rate (BER) performance.

In Section 4.2 a novel scheme for reducing the timing deviations due to DDJ is presented. This circuit detects transitions in the previously detected data sequence and adjusts the timing at current edges. Section 4.3 discusses the implementation issues involved in the design of DDJ equalizers and compares them to current issues in the design of decision feedback equalizers. Finally, the results of the circuit implementation are discussed in Section 4.4. The reduction in the DDJ is measured both in the data eye as well as through the clock and data recovery circuit. It is demonstrated that DDJ equalization can significantly improve the timing margins of the received data but can incur an additional penalty in terms of random jitter.

4.2 DDJ Equalization

The relationship between the data sequence and DDJ discussed in Chapter 3 suggests that the effect of the bandwidth limited channel might be mitigated. Consequently, jitter penalties can be substantially reduced. In this section we propose the implementation of deterministic jitter equalization (DJE) schemes for DDJ.

Removing the presence of DDJ involves minimization of deviation in the threshold crossing. From (3.8), the threshold crossing times for a first-order system are

$$t_c = \tau \cdot \ln\left[\frac{-a_0 + \sum_{n=-k}^{-1} a_n[\alpha^{-(n+1)} - \alpha^{-n}]}{v_{th} - a_0}\right] \tag{4.1}$$

and can be approximated from (3.15) in higher-order responses as

$$t_c = t_o + \frac{v_{th} - \sum_{n=-k}^{0} a_n g(t_o - nT)}{\sum_{n=-k}^{0} a_n g^{(1)}(t_o - nT)} \tag{4.2}$$

for any k-length sequence. A simple solution to this problem for amplitude equalization in DFE is presented in [47]. Here, the pulse response is studied at the threshold crossing voltage. To simplify notation, we define $c_k=g(t_o\text{-}kT)$ and $d_k=g^{(1)}(t_o\text{-}kT)$. The relationship between these coefficients and the pulse response is illustrated in Figure 4.1.

Eliminating DDJ implies setting the numerator of (4.2) to zero. Consequently,

$$v_{th} - \sum_{n=-\infty}^{0} a_n c_n + \sum_{n=-\infty}^{0} a_n \varepsilon_n = 0, \tag{4.3}$$

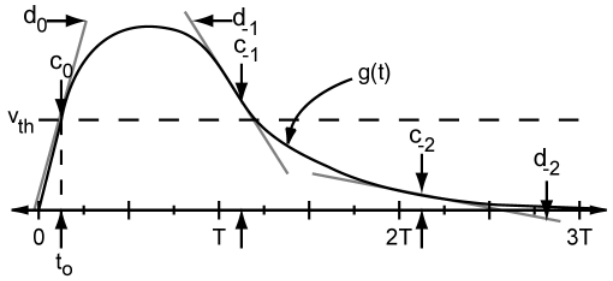


Figure 4.1 Definition for tails of pulse response for DDJ equalization.

where ε_n are the compensation coefficients. Assuming $v_{th} = 0.5$, we approach DDJ compensation by detecting transitions as opposed to particular bits. Therefore, a bit-wise operation can be performed on the previous bits to determine when transitions occurred. Using an exclusive-or (XOR) operator ($\oplus$), transitions are detected, and the response for complementary bit sequences is identical (i.e. 101 and 010 are compensated identically). We define a transition coefficient, $x_n = a_{-1} \oplus a_n$. Notice that $x_{-1} = 0$. Additionally, $x_0 = 1$ implies that a transition occurs at the current bit. Applying this operation to (4.3),

$$\frac{1}{2} - c_o - \sum_{n=-\infty}^{-2} x_n c_n + \sum_{n=-\infty}^{-2} x_n \varepsilon_n = 0. \tag{4.4}$$

By construction, $c_0 = 0.5$ and the signal is compensated with the voltage values

$$\varepsilon_n = c_n \quad \text{for} \quad n \le -2. \tag{4.5}$$

This DDJ compensation scheme is reminiscent to DFE algorithms, except that the coefficients are calculated at the transitions instead of the center of the data eye. However, an important distinction of DJE is that the compensation can be applied in the time domain. This offers the advantage of just affecting the phase characteristics of the signal. Furthermore, time compensation is necessary in situations where the linearization of the signal near the threshold crossing is not valid. For DDJ in (4.2),

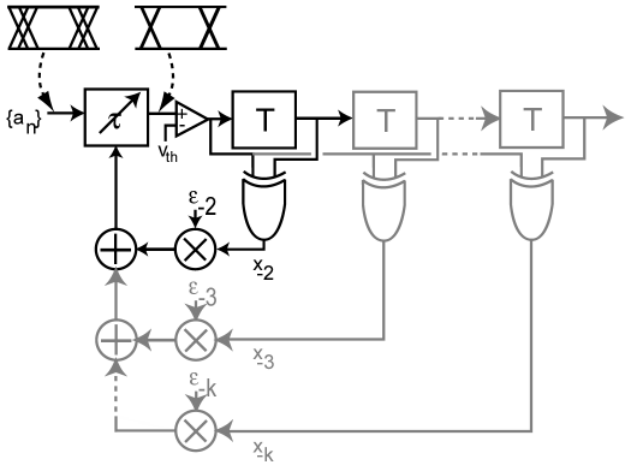


Figure 4.2 The block diagram for the DJE and the extension, shown in gray, for compensating over multiple samples.

$$\sum_{n=-\infty}^{-2} x_n \varepsilon_n - \frac{\sum_{n=-\infty}^{-2} x_n c_n}{d_0 + \sum_{n=-\infty}^{-2} x_n d_n} = 0 . \tag{4.6}$$

Now the equalization scheme generates a time delay adjustment. Perfect compensation in this situation is impossible because we have one parameter to adjust for two unknowns, c_n and d_n. A useful approximation is derived when the slope decays rapidly (i.e. $d_0 \gg d_k$, for $k < -2$) and the coefficient can be calculated as

$$\varepsilon_n = \frac{c_n}{d_0} \qquad n \le -2 . \tag{4.7}$$

A DJE architecture based on this construction is shown in Figure 4.2. This scheme generalizes the circuit discussed in [98]. Transitions are calculated through a cascade of bit-period delays. Since the delays occur after a decision is made, these delays can be implemented as digital gates. When a transition is detected, the compensation coefficient is added to other weighted transition detection signals, and this value adjusts the receiver delay before the next transition reaches the threshold detector.

When c_n and d_n are not independent, as for the first-order response, the dominant time-delay compensation can be determined and compensated exactly from (4.1).

$$\tau_p \ln\left[1 + \sum_{n=-\infty}^{-2} \varepsilon_n\right] = \tau_p \ln\left[1 + \sum_{n=-\infty}^{-2} (\alpha^{-n} - \alpha^{-n+1}) x_n\right] \tag{4.8}$$

Voltage compensation is introduced with the logarithm because of the dependence on transition history. If only the penultimate bit is compensated, the compensation coefficient is in the time domain.

$$\varepsilon_{-2} = \tau_p \ln[1 - x_{-2}(\alpha - \alpha^2)] \tag{4.9}$$

This result will be used to demonstrate the eye improvement of DJE schemes.

Finally, the detection of prior rising or falling edges allows individual compensation of the consecutive falling and rising edges, respectively. The illustration in Figure 4.3 demonstrates how a logical AND gate detects either a rising or falling edge after the data value is decided. Parallel adjustments are provided and combined in a variable time delay element. This scheme is presented in [100] and is particularly useful when a non-linear response introduces different DJ on the rising and falling edges.

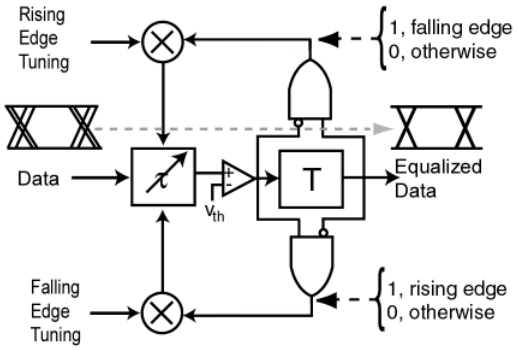


Figure 4.3 DJE with independent control of the rising and falling edges.

4.2.1 Eye Improvement with DJE in a First-Order Channel

While it may seem that DJE only works on open data eyes, this technique has limited capability for completely closed eyes. This is illustrated in this section for the first-order system. In Figure 4.4 the data eye is shown with and without DDJ compensation at f_c = $0.20f_b$ and $f_c = 0.10f_b$. For the higher cutoff frequency, the transitions converge when (4.9) is used as the compensation scheme. Removing the timing deviations also enhances the voltage margins of the data eye and improves both the timing and voltage margins.

For the lower cutoff frequency, the first-order response closes the data eye. When DJE is introduced, the data eye is re-opened. Consequently, the maximum bit rate is increased before the eye is completely closed with DJE. To quantify this theoretical eye opening, we simulate the voltage and timing margin enhancement in Figure 4.5. The timing margin is calculated at the voltage threshold, and the sampling time for the voltage margins is calculated in the center of the timing margin. Interestingly, the DJE is capable of keeping the data eye open to more than 12Gb/s, an improvement of 3Gb/s than without DJE.

4.2.2 Comparison to Decision Feedback Equalization

The operation of the DJE resembles DFE insofar as that previous decisions about the data are used to dynamically adjust the receiver response. Additionally, many of the implementation issues associated with DJE are analogous to issues pertaining to DFE. For

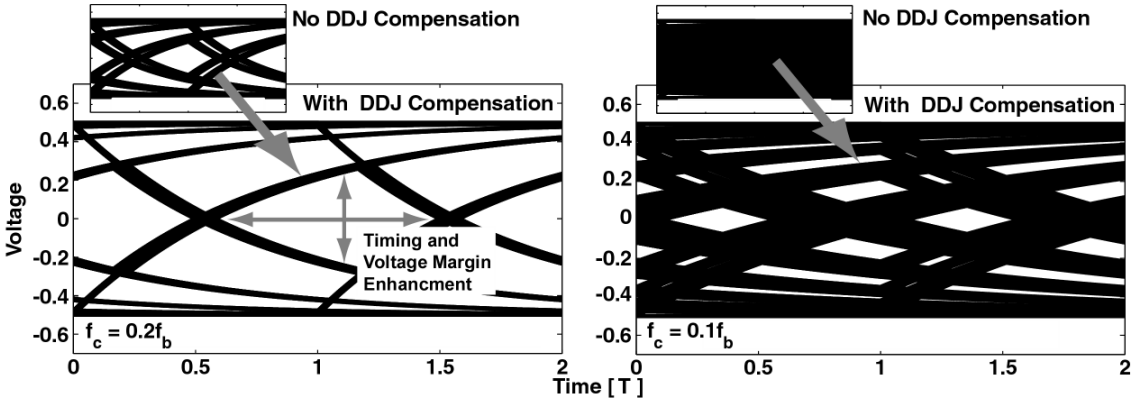


Figure 4.4 Opening a closed data eye with the use of only DDJ compensation.

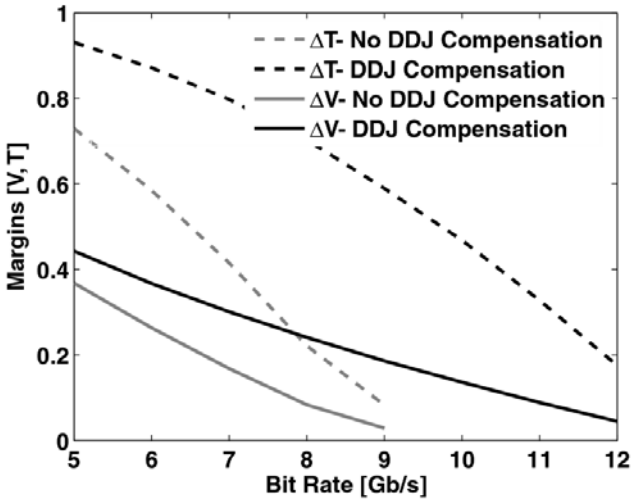


Figure 4.5 Theoretical timing and voltage margin improvement for first-order channel with DJE.

instance, DJE implementations are subject to similar critical path timing requirements as DFE [101].

Several distinctions between the schemes are noteworthy. Firstly, the feedback of the DJE carries information about transitions rather than specific bits. This information is inferred from bit period delayed bit samples. Analog feedback could also be implemented without actually sampling the data to compensate the DDJ.

Second, the DJE relies on a time delay adjustment in the receiver instead of varying the decision voltage threshold. In some situations, these two processes are similar. For instance, small variations of delay can be viewed as shifting the voltage threshold. However, when the transition of the data edge is non-monotonic, these approaches are essentially different because the linearization of the slope does not translate into a unique correspondence between the voltage and time-delay. Furthermore, in situations where the compensation is required over a time interval greater than the rising or falling edge, a true time delay is required instead of simply a voltage threshold adjustment.

DJE can be implemented in the transmitter or the receiver. When DJE is implemented as a pre-emphasis technique, the DDJ peaks at the transmitter are reversed such that the effect of the channel is to neutralize the DDJ at the receiver and create consistent

transitions. The peak power constraints of the output driver de-emphasize the transmitted signal but do not limit DJE techniques. DJE can improve the timing margins of the eye by manipulating the transmit clock which, in principle, does not incur significant power consumption.

In the receiver, DJE could enhance the performance of DFE techniques. In general, DFE techniques are well-suited for channels with strong attenuation, while DJE is useful for dispersive channels. In [32] and [101], the DFE is implemented by multiplexing between two voltage comparators with different voltage thresholds. Once the decision on the previous bit is complete, the output of one of these multiplexers is selected for the next bit. Simultaneously, we could imagine the same process in the time domain. Every bit is sampled at two different sampling times, and on the basis of the previous detected bit we would choose one or the other same. Ultimately, combining both techniques to adjust both the voltage threshold and the transition (or sampling) time on a bit-by-bit basis could provide the optimal BER performance.

4.3 Circuit Implementations

The discussion of data-dependent jitter has identified a technique for removing jitter from the data signal. This increases both the timing margins of the recovered data as well as the clock output jitter. Two integrated circuits have been designed to test different aspects of DJE for DDJ. The first circuit consists of a DJE that is integrated with a CDR circuit. The second circuit is a MOSFET implementation of a DJE with independent control of the rising and falling edges of the data eye.

4.3.3 DJE and CDR (DJE CDR)

A chip microphotograph for the first design is provided in Figure 4.6. The fabrication technology is 0.18μm SiGe with bipolar f_T of 120GHz. The circuit consists of the DJE, a PLL, and 50 Ohm output drivers. A circuit schematic of the DJE CDR is illustrated in

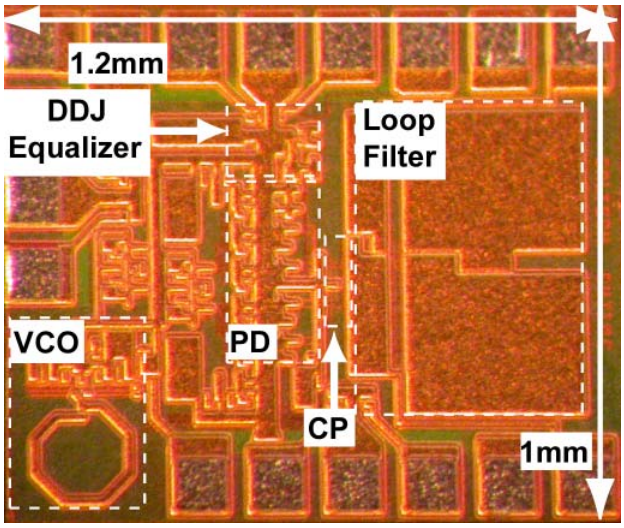


Figure 4.6 Chip microphotograph of the DJE CDR.The circuit includes an on-chip loop filter.

Figure 4.7. The DJE corrects for jitter caused by the penultimate bit. It functions essentially as described in the dark portion of the schematic in Figure 4.2.

The PLL is designed with a modified Hogge phase detector (PD) [94][95]. The Hogge PD comprises cascaded DFFs. The output of each flip-flop is a bit period shifted version of the received signal. The DJE taps the input of the Hogge phase detector and the first DFF as demonstrated in Figure 4.7. Since the delays depend on the DFF driven by the recovered clock, the equalization only operates correctly when the PLL is locked. The delay stage is based on the current-starved differential pair suggested in [16]. Each path is driven by the transition-detection multiplier implemented with a logical XOR gate.

The operation of the DJE requires that the current is fully steered within one bit period. Since detection of a previous transition compensates the timing of the current transition, the transition must be detected and the delay adjusted within a symbol period. While the use of look-ahead logic suggested in [27] can relax the feedback requirement, it comes at the disadvantage of power and complexity.

The circuit demonstrated Figure 4.7 only requires one logical gate delay. As this XOR is an emitter-coupled logic (ECL) gate, the gate delay is about 20ps in a 0.18μm SiGe technology. Faster speeds are possible in this technology given additional power

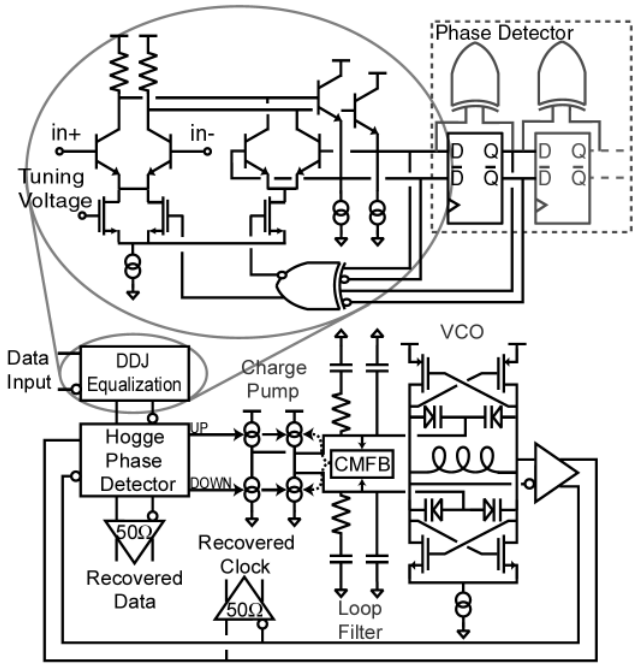


Figure 4.7 The circuit diagram for the DJE CDR.

consumption [102]. Since the delay is based on current steering, the delay stage adjusts quickly to the transition data. NMOS transistors provide smooth transition of the current between the differential pairs. The amount of variation between the two delay values is controlled by the equalizer tuning voltage. The NMOS transistor acts as a current bypass to the transition-detection multiplier. When the applied voltage is high, the current is steered through the by-pass transistor. Otherwise, the transistor controls how much current is switched between the two transistors. Since the ECL gate only provides around 300mV of signal swing, the NMOS transistor is sized to provide the desired current variation when the transition detection is asserted. In simulation the delay variation is 10ps.

The phase detector drives a differential charge pump (CP) with a current of 400μA. An on-chip loop filter is designed with a bandwidth of about 50 MHz and a damping factor of about 0.7. The loop capacitor is, therefore, around 1pF, and the series resistance is around 4kΩ. The loop filter generates a differential control voltage for the complementary cross-coupled oscillator. The control voltages adjusts the frequency through complementary MOS varactors. The advantage of the differential tuning is rejection of

common-mode noise. Several PLL designs have demonstrated the benefit of differential tuning [103][104]. However, the common-mode must be set with feedback, as shown in Figure 4.7. The tuning range of the oscillator is 9 to 11.5GHz to provide robustness to process variations. The output of the oscillator is buffered and drives the phase detector and a 50 Ohm buffer.

The chip area measures 1.2mm by 1mm, including the loop filter and pads. The circuit consumes 70mA from a -3.5V supply. The DJE area is 100μm by 80μm and draws 10mA of this current.

4.3.4 CMOS DJE

The second circuit is implemented with 0.12μm MOSFETs in IBM 8HP. A chip microphotograph is provided in Figure 4.8. The circuit schematic is illustrated in Figure 4.9. This design was intended to remove the restrictions on implementing the DJE within a CDR circuit and uses variable delay stages for buffering. As this was the initial fabrication of the 8HP process (which combines both 0.12μm bipolar devices and CMOS devices), the MOSFET models were expected to exhibit some process variations. To satisfy the maximum feedback propagation delay, the topology uses look-ahead feedback that introduces a delay to compensate for the propagation delay, τ_{prop}. Consequently, this approach targets DJ accumulation in high-speed circuits.

High-speed current-mode logic (CML) AND gates detect transitions at 10Gb/s. This logic gate approach is more robust to process variations and is sufficient for a

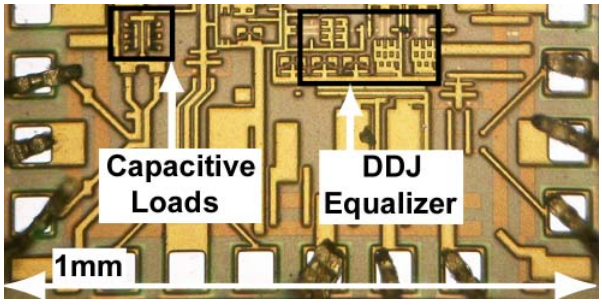


Figure 4.8 Chip microphotograph of the CMOS DJE.

proof-of-concept of the DJE. The implementation of the AND gate is demonstrated in Figure 4.9. The CML gates generate logical values when the rising or falling edges occur, and this logical value is weighted to adjust the variable time delay.

The variable time delay is demonstrated in Figure 4.9 and is the NMOS analogue to the cross-coupled latched used in the ECL implementation. Additionally, the delay control is provided for two different control signals. This avoids explicitly combining the falling and rising edge control signal before the delay stage and lowers the feedback latency. Each delay signal occurs exclusively since rising and falling edges do not occur simultaneously. The rising and falling edge detection signals are combined in the tail of each differential pair. The DJE area is 130μm x 80μm. From simulation, the circuit draws 20mA per channel. Additional current consumption supports the output buffering as well as additional circuits tested in [106].

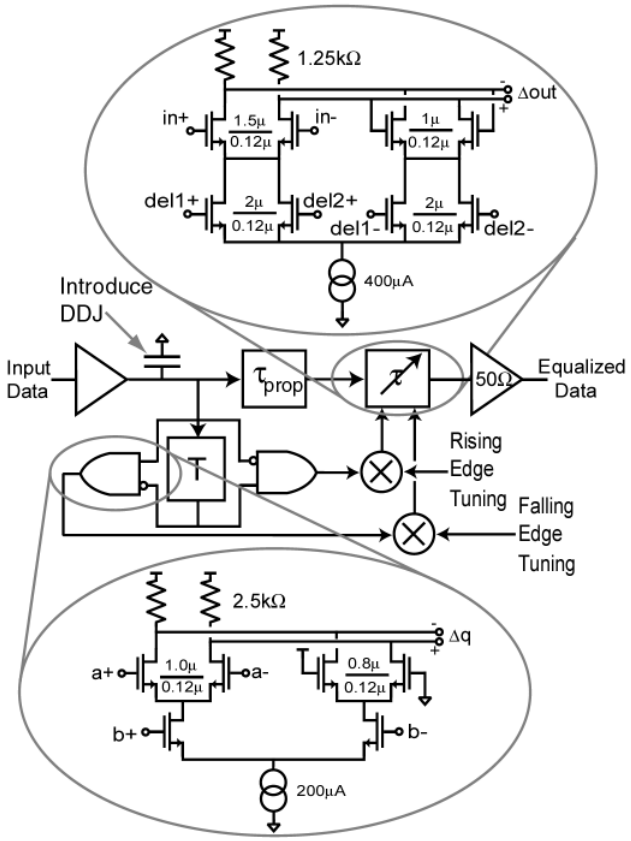


Figure 4.9 Schematic for the CMOS DJE. Inset includes schematic for low-power CML AND gate and delay cell.

4.4 Results

To test the DJE described in the previous sections, we need to introduce a controllable amount of DDJ. Some circuit alternatives are illustrated in Figure 4.10. Ease of implementation and testing issues determine the best scheme. A bandwidth-constrained buffer stage is shown in Figure 4.10A. The dominant time constant introduces a first-order response. This scheme is easily implemented on-chip at high speeds to avoid reflections.

Next, DDJ can be introduced between differential transmission lines through cable attenuation and, consequently, bandwidth reduction as shown in Figure 4.10B. At high speeds the lines are impedance-matched and reflections are typically attenuated over the length of the fiber. However, it is difficult to change how much DDJ is introduced.

Finally, the circuit in Figure 4.10C correlates the data through a one bit delay. The multiplier controls the sign and amplitude to create either a positive or negative replica of the original bit. The bit and bit-delayed signal are coupled through transmission lines. The coupling advances or slows the velocity of the data transition through the mode between the lines [77][106]. This coupling behavior shifts the time of flight for the transition on the microstrip line. The amount of DDJ that is introduced is given by

$$t_{c,\,DDJ} = \tau_f \frac{V_{pp,\,replica}}{V_{pp,\,signal}}, \tag{4.10}$$

where the time constant is a high-pass filter time constant defined in [106] and the numerator and denominator are the peak-to-peak signal swings. Adjusting the swing gives a

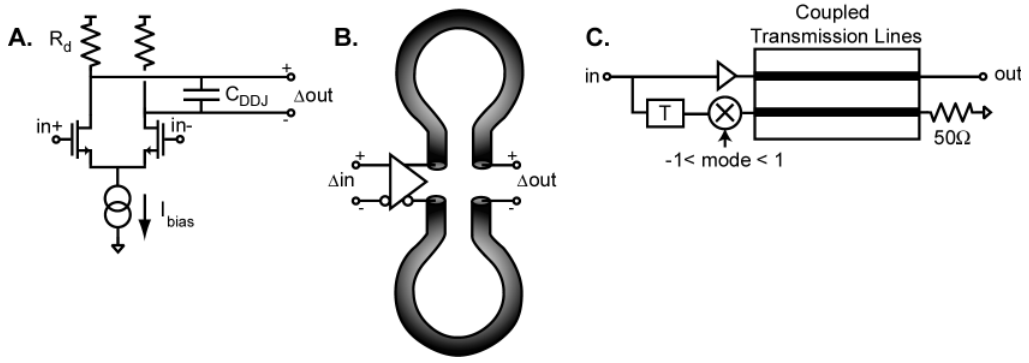


Figure 4.10 Testing schemes for generating DDJ.

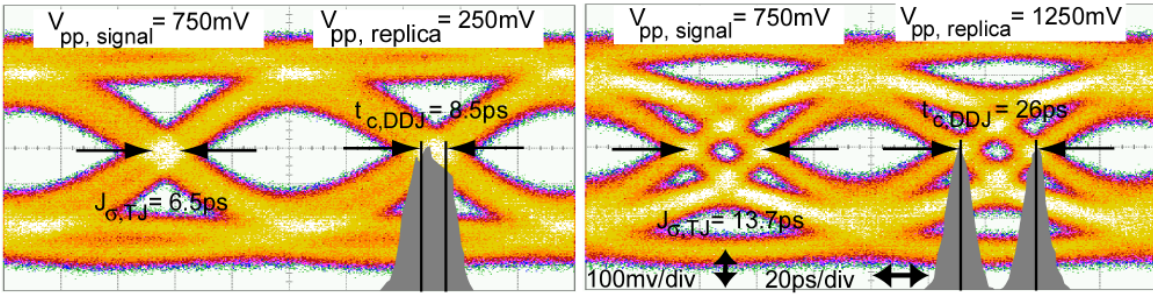


Figure 4.11 Eyes with variable amounts of DDJ for testing.

linear adjustment of the DDJ peak separation. Using a 10Gb/s Anritsu MP1763C pulse pattern generator (PPG), the differential output swing of the PPG can be controlled independently. One data output is introduced directly to the coupled transmission lines. The complementary data output is delayed by one bit using wideband phase shifters before entering the coupled transmission lines. Varying the complementary output amplitude allows manipulation of (4.10). In Table 4.1, the total rms jitter is measured from the data eye for various ratios. $J_{\sigma,RJ}$ is 4.75ps and is discounted from the total jitter according to (2.31). Then, the distance between the DDJ threshold crossing time peaks is calculated. Two eyes are shown in Figure 4.11 with different ratios of (4.10). The DDJ peaks in the two eyes are separated in time by 8.5ps and 26ps, respectively. Comparing these values for the DDJ peaks with the anticipated values in Table 4.1 demonstrates the close agreement (less than 0.4ps deviation) with the theory. This scheme provides a flexible platform to control the amount of DDJ with impact to the ISI.

Table 4.1: DDJ generated from coupled wires scheme (V_{signal} = 750mV) and anticipated CDR jitter.

$\mathbf{V_{replica}}$	$\mathbf{J_{\sigma,TJ}}$	$\mathbf{J_{\sigma,DDJ}}$	$\mathbf{t_{c,DDJ}}$	$\mathbf{J_{\sigma,CDR}}$
250mV	6.5ps	4.4ps	8.8ps	1.6ps
500mV	8.3ps	6.8ps	13.6ps	2.1ps
750mV	10.1ps	8.9ps	19.8ps	2.5ps
1000mV	11.9ps	10.9ps	21.8ps	3.0ps
1250mV	13.7ps	12.8ps	25.6ps	3.4ps

These results predict the rejection of DDJ through the CDR. The natural frequency of our loop filter is near 50MHz, and the damping factor is about 0.7. Therefore, the equations expressed in Section 2.2.5 for $\zeta = 0.707$ approximate the expected results. In this case, the long term jitter is anticipated to be

$$J_{\sigma,\,CDR} \;=\; J_{\sigma,\,DDJ}\sqrt{\frac{3\omega_n T}{\sqrt{2}}} \;=\; 0.25 \cdot J_{\sigma,\,DDJ}\,. \tag{4.11}$$

In Table 4.1 this relationship is demonstrated across the range of the DDJ inputs.

4.4.5 DJE CDR

For the DJE CDR, DDJ is introduced with the schematic in Figure 4.10C. Several steps are taken to demonstrate the performance of the DJE CDR. First, the bias voltage of the VCO is scanned to determine the lowest phase noise. The phase noise is measured with an Aeroflex NTS-1000B. The phase noise is measured when the CDR is locked to a periodic (1010...) sequence at 5Gb/s and is demonstrated in Figure 4.12. The phase noise under this condition is more than 10dB below the phase noise when the PRBS is applied. Additionally, the phase noise of the PPG is measured with an alternating one and zero

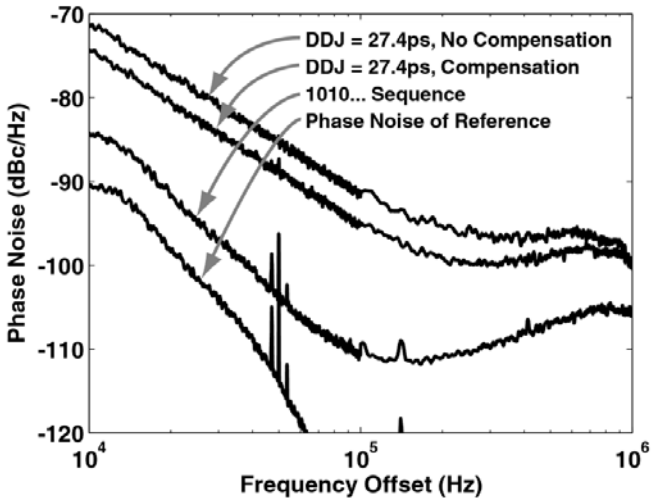


Figure 4.12 Phase noise of the recovered clock under various test conditions.

pattern to demonstrate the noise contributed by the CDR circuit and the VCO. The phase noise increases above 100kHz due to the additional impact of the VCO phase noise.

Next, the phase noise is measured with a 2^{31}-1 PRBS sequence. The phase noise is measured without any DDJ compensation and with the maximum compensation. Below 1MHz (the cutoff of the phase noise analyzer), the phase noise is generally improved and is decreased by 4dB at the 100kHz offset when the DDJ is compensated.

The data eye and recovered clock are illustrated in Figure 4.13 without the influence of DDJ. Using an Agilent 81600B wide-bandwidth oscilloscope, the timing statistics are collected from 5000 histogram points. The rms jitter of the recovered data is slightly greater than the recovered clock due to DDJ in the output driver. The rms jitter on the recovered clock is comparable to the jitter reported at 10Gb/s in [19]: 0.78ps, or [125]: 0.95ps. The timing jitter is recorded for DDJ condition described in Table 4.1 and illustrated in Figure 4.14 for the jitter of the recovered clock and data. Increasing the tuning of the DJE lowers the jitter by 0.3ps.

The predicted $J_{\sigma,CDR}$ due to the input $J_{\sigma,DDJ}$ is on the order of the measured $J_{\sigma,CDR}$. However, the total variation reflected in the curves in Figure 4.14 is not as great as the variation in Table 4.1. One explanation is that other sources of jitter, such as the noise added by the operation of the DJE, limits the minimum improvement. This trade-off is described at the end of this section.

Finally, a bathtub curve is generated for the DDJ and ISI of the data eye to demonstrate the BER improvement. The sampling voltage and time is scanned with an Anritsu

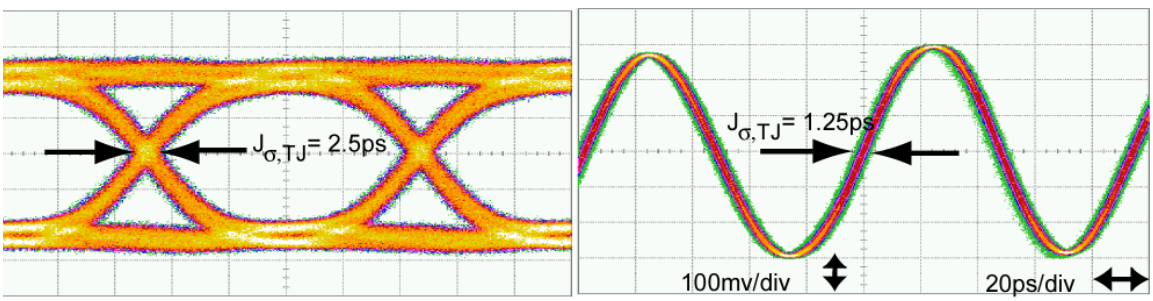


Figure 4.13 Typical eye and recovered clock from the DJE CDR with no input DDJ.

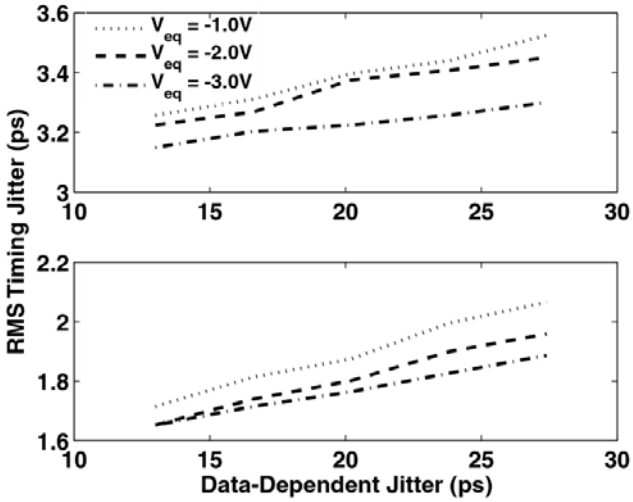


Figure 4.14 Timing jitter of the recovered data (top) and the recovered clock (bottom) for the DJE CDR.

MP1764C error detector, and the BER at each sampling point is recorded. The collection of these BER measurements forms two bathtub curves in Figure 4.15. For this bathtub curve, we switched our testing environment to 60” of RG-58 cable used to motivate this discussion of DDJ in Figure 2.8. Notably, the data is retimed internally in the Hogge phase detector. Therefore, the bathtub curve in this case demonstrates the ability of the PLL to reduce the contribution of DDJ to the recovered clock timing jitter. Interestingly,

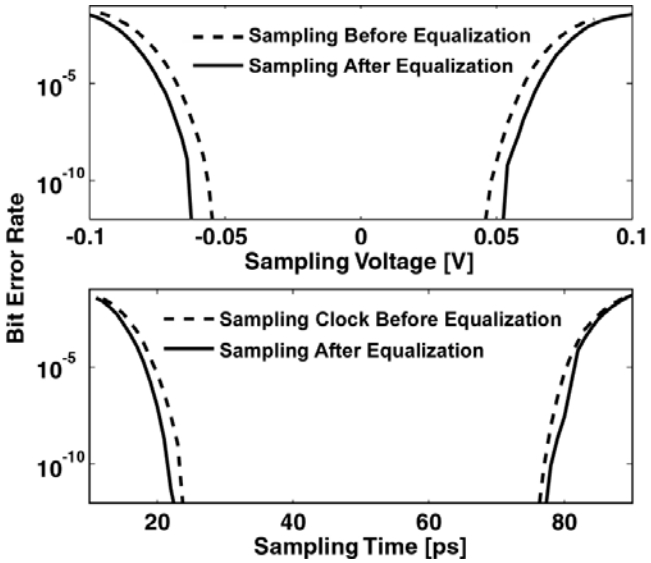


Figure 4.15 Bathtub curve of sampling time and sampling voltage before and after equalization for DJE CDR.

improvement was measured in both the voltage and timing margins. The timing margins at 10^{-12} BER were increased by about 3ps, while the voltage margins increased around 10mV at 10^{-12} BER.

4.4.6 CMOS DJE

To introduce DDJ in this implementation, on-chip capactive loaded amplifiers, as described in Figure 4.10A, were used to simplify testing. A 2.5mA buffer is loaded with three large, laser-trimmable capacitors. The capacitors are metal-insulator-metal (MIM) located near the top analog metal (AM) layer, which is easy to trim. Each capacitor loads the amplifier with 91fF. Using the first-order relationships for jitter in Section 3.2.2, we predict the DDJ introduced due to this loading at 10Gb/s in Table 4.2. The largest load capacitance is used for testing the DJE at 10Gb/s.

Table 4.2: DDJ introduced in the load amplifiers of CMOS DJE.

Load Capacitance	τ	α	$\mathbf{t}_{c,DDJ}$
91fF	18ps	0.0041	0.074ps
182fF	36ps	0.064	2.3ps
273fF	54ps	0.16	8.0ps

The data eye measurement results for the DJE are shown in Figure 4.16 and in Table 4.3 at 10Gb/s. Four eyes are demonstrated to show the independent equalization of the rising and falling edges.

Table 4.3: DDJ improvement at 10Gb/s (ps) for CMOS DJE.

Equalization	$\mathbf{J}_{\sigma,TJ}$	$\mathbf{J}_{pp,TJ}$	**10^{-12} BER**
None	9.3ps	50ps	30ps
Falling Edge	7.4ps	41ps	41ps
Rising Edge	7.1ps	34ps	43ps
Rising and Falling	4.6ps	35ps	52ps

The individual compensation of the rising and falling edges reduced J_σ by similar amounts. J_{pp} was clearly improved entirely by rising edge equalization.The compensation of the rising edge was slightly better since the rising edge suffers from more DJ than the falling edge. The additional DJ on the rising edge is a circuit-induced asymmetry that occurs in the rising edge equalization path but not in the falling edge path.

To analyze these results, we assume that the minimum rms jitter recorded in the data eye was contributed solely by random jitter in the circuit, $J_{\sigma,RJ}$ = 4.6ps. To understand the expected rms jitter when only one edge contributes to the DDJ, as we observe in Figure 4.16, the PDF for DDJ is modified to study DDJ when only one edge is compensated. Now,

$$PDF_{DDJ}(t_c) = \frac{1}{4}\delta\left(t_c - t_o + \frac{t_{c,DDJ}}{2}\right) + \frac{1}{2}\delta(t_c - t_o) + \frac{1}{4}\delta\left(t_c - t_o - \frac{t_{c,DDJ}}{2}\right), \qquad (4.12)$$

where the minimum DDJ occurs when the compensated edge occurs between the two edges that suffer from additional DDJ. Consequently, the rms jitter can be expressed as

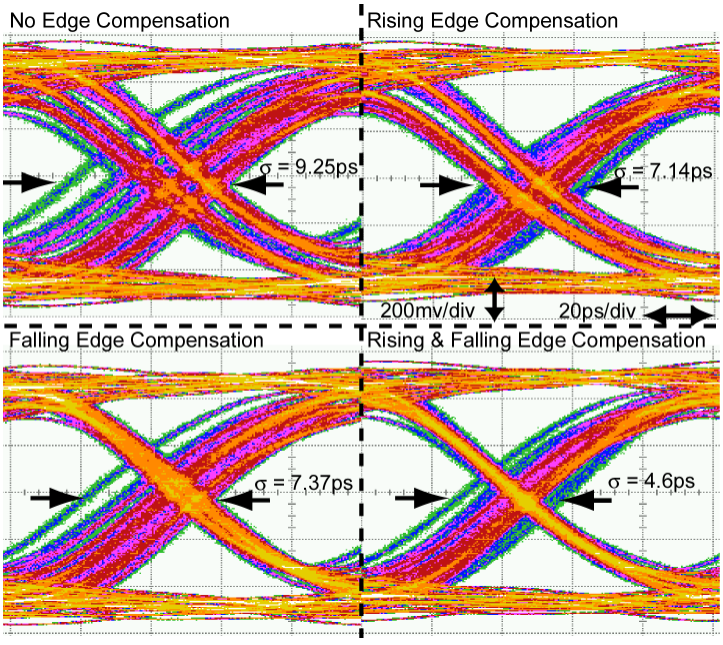


Figure 4.16 Data eyes demonstrating compensation of different edges and the jitter statistics associated with each edge.

$$J_{\sigma,\,DDJ} = \frac{t_{c,\,DDJ}}{2\sqrt{2}}. \tag{4.13}$$

Notably, this is 1.4 times smaller than if the DDJ is present on both edges. With (4.13), the contribution of DDJ is determined in Table 4.4. The RJ component is discounted to determine $J_{\sigma,DDJ}$ and the threshold crossing time variation. This expression gives consistent expectations for the threshold crossing time deviation.

Table 4.4: Data-dependent jitter contribution at 10Gb/s for CMOS DJE.

Equalization	$\mathbf{J_{\sigma,TJ}}$	$\mathbf{J_{pp,TJ}}$	$\mathbf{10^{-12}}$ **BER**
None	9.3ps	8.1ps	16.2ps
Falling Edge	7.4ps	5.8ps	16.4ps
Rising Edge	7.1ps	5.4ps	15.3ps
Rising and Falling	4.6ps	0ps	0ps

The calculation of $t_{c,DDJ}$ indicates that the actual DDJ is twice as great as the DDJ contributed from the capactive load in Table 4.2. Additional sources of parasitics were studied to determine the source of 7ps of DDJ. The layout contained a long connection loading a 500μA buffer with 38.5fF. This implies that τ = 48ps and α = 0.12. Therefore, this buffer introduced an additional 5.6ps of DDJ, accounting for a significant portion of the additional DDJ. This example illustrates interconnect challenges for signal integrity on-chip.

Finally, the BER bathtub curve is calculated directly through the MP1764C error detector to verify the BER improvement of the DJE in Figure 4.17. The BER demonstrates that equalizing the individual edges resulted in similar eye-opening. The equalization of both edges increased the eye opening that achieved BER of 10^{-12} from 30ps to 52ps over the 100ps unit interval.

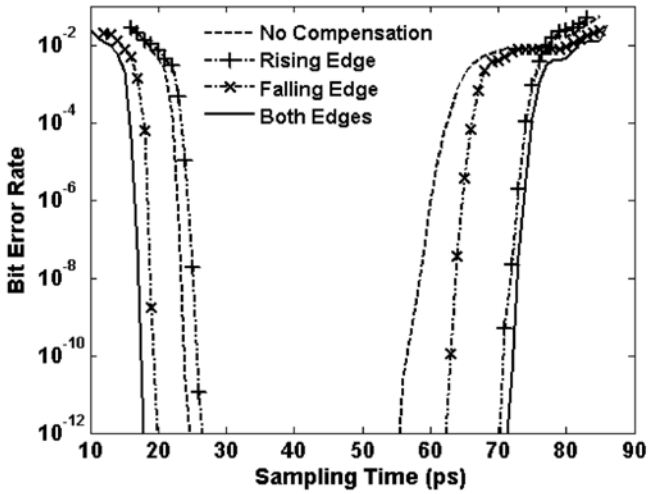


Figure 4.17 Bathtub curve resulting before and after equalization in CMOS DJE.

4.4.7 Trade-off between DDJ Compensation and RJ.

In the described DJE schemes, delay variation is introduced through a buffer stage. Therefore, a design trade-off exists between compensating DDJ and introducing additional random jitter. From [105], the random jitter introduced through a CMOS buffer stage is

$$J_{\sigma,\,buffer} = \sqrt{kTC_L}\frac{\xi}{I_{ss}}, \tag{4.14}$$

where C_L is the load capacitance, I_{ss} is the stage bias current, and ξ is a bias dependent term. The delay of the stage, if slew rate limited as in our cross-coupled stages, is $t_d = C_L V_S / I_{ss}$ where V_S is the logic swing. Therefore, delay variation is achieved by varying the stage current between I_{ss1} and I_{ss2}:

$$\Delta t_d = \frac{C_L V_s}{I_{ss1}}\left(\frac{I_{ss1}}{I_{ss2}} - 1\right) = t_{d1}\Delta d, \tag{4.15}$$

where t_{d1} is the minimum stage delay and Δd is the percentage delay variation. This delay stage introduces random jitter that depends on the delay variation. From (4.15), the RJ is

$$J_{\sigma,\,delay} = \frac{\xi}{I_{ss1}}\sqrt{\frac{kTC_L}{2}}\sqrt{1+\left(\frac{I_{ss,\,1}}{I_{ss,\,2}}\right)^2} = J_{\sigma,\,buffer}\sqrt{\frac{1+(1+\Delta d)^2}{2}}, \tag{4.16}$$

where this is expressed with the percentage of delay variation and the minimum buffer jitter. The total jitter with DJE is expressed

$$J^2_{\sigma,\,TJ} = \left(J_{\sigma,\,DDJ}-\frac{\Delta t_d}{2}\right)^2 + J^2{}_{\sigma,\,delay}. \tag{4.17}$$

The expression in (4.16) is substituted into (4.17) and we find

$$J^2_{\sigma,\,TJ} = J^2_{\sigma,\,DDJ} + J^2_{\sigma,\,buffer} + \Delta t_d\left(\frac{J^2_{\sigma,\,buffer}}{t_{d1}} - J_{\sigma,\,DDJ}\right) + \Delta t_d{}^2\left(\frac{J^2_{\sigma,\,buffer}}{t^2_{d1}}+\frac{1}{4}\right). \tag{4.18}$$

If the DDJ is removed, i.e. $\Delta t_d = 2J_{\sigma,DDJ}$, the minimum jitter in (4.18) becomes

$$J^2_{\sigma,\,TJ} = J^2_{\sigma,\,buffer}\left(1+\frac{2J_{\sigma,\,DDJ}}{t_{d1}}\right)^2. \tag{4.19}$$

For the TJ to be less than our original DDJ, (4.19) should be less than $J^2{}_{\sigma,DDJ}$. Therefore,

$$J_{\sigma,\,DDJ} > \frac{1}{\dfrac{1}{J_{\sigma,\,buffer}}-\dfrac{2}{t_{d1}}} \approx J_{\sigma,\,buffer}, \tag{4.20}$$

where $J_{\sigma,buffer}$ is assumed to be much less t_{d1}. The strength of the inequality in (4.20) determines the effectiveness DJE. If $J_{\sigma,DDJ}$ is large relative to $J_{\sigma,buffer}$, the TJ should reduce dramatically with DJE. If $J_{\sigma,DDJ}$ is relatively small, little improvement will result in the overall TJ.

This analysis provides one explanation for the slight improvement in Figure 4.12 and Figure 4.14. In particular, the noise of the cross-coupled delay stage adds significant jitter and reduces the benefit of DJE. Furthermore, the delay stage is susceptible to

power-supply variations which could add an additional jitter penalty and, consequently, (4.20) is a lower bound criteria for introducing DJE.

4.5 Summary

We have proposed the use of deterministic jitter equalization for minimizing DDJ and have studied the signal integrity and BER improvement. This study includes a comparison to well-known decision-feedback equalization techniques. Deterministic jitter equalization may enhance the performance of DFE techniques in future serial transceivers. Two circuit implementations are presented to demonstrate the operation of data-dependent jitter equalization. While both of these circuits have been oriented for the first post-cursor DDJ, the technique can be applied to more general equalization schemes that involve longer latency reflections. The first data-dependent jitter equalizer is integrated into a clock and data recovery circuit. Jitter creates phase errors in the feedback loop of the PLL circuit. A Hogge phase detector is modified to adjust the timing of each data transition according to the previously detected bits. This circuit demonstrates reduces jitter on the recovered sampling clock by 0.5ps rms. Additionally, the recovered data eye timing and voltage margins are improved. The second data-dependent jitter equalizer is designed to provide independent adjustment of the rising and falling data transitions. The timing margins of the data eye at 10^{-12} BER are improved by 22ps. Finally, we provide an analysis of the trade-offs between using a DDJ equalization scheme and the introduced random jitter from the variable time delay required for equalization.

Chapter 5

Phase Pre-emphasis Techniques[1]

5.1 Introduction

Equalization of high-speed serial links has evolved to compensate intersymbol interference (ISI) caused by frequency-dependent attenuation found in electrical interconnects. Pre-emphasis-based equalization in the transmitter and decision feedback equalization in the receiver figure prominently in overcoming signal degradation and improving BER [29][31]. An important challenge of equalization is minimizing power consumption while still improving signal integrity in the presence of attenuation and reflections.

We expand the notion of pre-emphasis beyond amplitude compensation of ISI and introduce phase pre-emphasis for compensating data-dependent jitter (DDJ). Amplitude pre-emphasis compensates ISI introduced by the bandwidth limitations of the interconnect [107][108]. In Figure 2.5, the loss of the RG-58 cable is roughly 4dB at 3GHz, one-half the bit rate of 6Gb/s. For the backplane with connectors, the loss is close to 10dB at 3GHz and rolls off more quickly than the cable attenuation. The use of amplitude pre-emphasis techniques such as feed-forward equalization increases the power consumption and places additional demands on the dynamic range of the transmitter. Finding new methods for lowering power consumption in serial links has been explored through low common mode signaling [99] and through low-supply operation [109]. This design targets a 5mW/Gb/s power consumption target while offering equalization appropriate for shorter (under 16”), less dispersive interconnects.

1. In collaboration with Dr. Mounier Meghelli at IBM TJ Watson Research Center.

The use of phase pre-emphasis is motivated by reducing power consumption dedicated to amplitude pre-emphasis. In particular, phase pre-emphasis does not require substantial power consumption because it is introduced through dynamically adjusting the transition times of the data. Consequently, using phase and amplitude pre-emphasis to improve signal integrity can reduce the total power consumption of the transmitter. The effectiveness of phase pre-emphasis depends on the behavior of the interconnect channel response.

In Section 5.2 we summarize the operation and power consumption in amplitude pre-emphasis transmitters. In Section 5.3 an analysis of the signal integrity enhancement of amplitude pre-emphasis is demonstrated for a simple channel to understand the trade-off between power and channel capacity. Section 5.4 introduces the notion of phase pre-emphasis and discusses a general algorithm for reducing DDJ at the receiver. We demonstrate the potential to introduce phase pre-emphasis to improve the signal integrity with little additional power consumption in the transmitter. The analysis concludes with a calculation of the power-to-bit rate ratio for a transmitter with and without phase pre-emphasis. In Section 5.5, we discuss the implementation of a 6Gb/s transmitter with amplitude and phase pre-emphasis. Finally, the hardware results are discussed in Section 5.6 over both a bandwidth-limited cable and a backplane interconnect.

5.2 Analysis of One-Tap Transmit Pre-Emphasis

Transmit pre-emphasis compensates for high-frequency loss. The block diagram for a one-tap feed-forward pre-emphasis scheme is shown in Figure 5.1. The circuit consists of two cross-coupled drivers that compete to drive the line. The pre-emphasis driver transmits data delayed by one bit period, *T*. The pre-emphasis gain, *G*, is the ratio of current in the pre-emphasis driver and main driver, I_{preemp}/I_{bias}. The transfer function for this stage is expressed as

$$H_{preemp} = \frac{TX(s)}{X(s)} = I_{bias}(1-Ge^{-sT}) \quad . \tag{5.1}$$

A first-order Pade approximation is used to express the time delay as a rational function, $e^{-sT} = (1-sT/2)/(1+sT/2)$. The transfer function for the scheme is written as

$$H_{preemp} = \frac{TX(s)}{X(s)} = I_{bias}(1-G)\frac{1+s(T/2)(1+G)/(1-G)}{1+s(T/2)}. \tag{5.2}$$

This transfer function reveals that the pre-emphasis scheme reduces the dc gain by *G*. For this reason, pre-emphasis is often considered "de-emphasis." The dc gain can be increased to maintain a constant voltage swing by increasing the bias current. High-frequency amplification is introduced through a zero that depends on *G*. The transfer function has an additional pole at 1/*T*. Other poles in an actual implementation limit the all-pass behavior. In Figure 5.1, the operation of transmit pre-emphasis creates four distinct transmit levels. The higher level, 1 + *G*, is transmitted when there is a data transition. As noted in the fig-

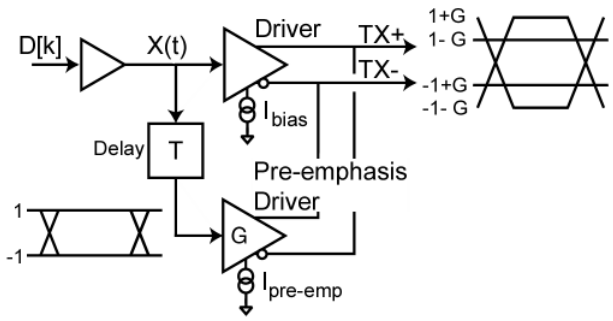


Figure 5.1 Block diagram for pre-emphasis driver.

ure, the binary levels are split into high and low levels. The minimum and maximum output swings are

$$\Delta V_{min} = 25\Omega \cdot (I_{bias} - I_{preemp}) \quad \text{and} \quad \Delta V_{max} = 25\Omega \cdot (I_{bias} + I_{preemp}), \tag{5.3}$$

where 25Ω is the load of the driver termination and the line impedance. Combining the two equations in (5.3) to remove the bias dependence, we find that

$$\Delta V_{max} = \Delta V_{min} \frac{(1+G)}{(1-G)}. \tag{5.4}$$

The gain factor in (5.4) also appears in the zero of (5.2). Two system constraints are placed on ΔV_{min} and ΔV_{max} and limit the maximum range for effective pre-emphasis. First, the receiver has a minimum swing to meet the sensitivity of the input stage, and we refer to this minimum swing as ΔV_{RX}. Second, the transmitter has a fixed peak power that will limit the maximum swing, and we call this ΔV_{TX}. This implies that a system bound on the amount of pre-emphasis gain is

$$G_{max} = \frac{(\Delta V_{TX}/\Delta V_{RX} - 1)}{(\Delta V_{TX}/\Delta V_{RX} + 1)}. \tag{5.5}$$

Larger ratios push the maximum pre-emphasis gain towards one. If the receiver swing is at least 200mV and the maximum transmitter swing is limited to 1V, the maximum pre-emphasis gain will be 0.667. Consequently, the zero is five times the pole frequency in (5.2). The total power consumed in the transmitter is

$$P = V_{DD}(I_{bias} + I_{preemp}) = V_{DD} I_{bias}(1+G). \tag{5.6}$$

Substituting (5.4) into (5.6), the power consumption for one-tap amplitude pre-emphasis is determined by the minimum of receiver and the transmitter power constraints,

$$P = \frac{V_{DD}}{25\Omega} \cdot min\left\{ \Delta V_{RX} \frac{(1+G)}{(1-G)}, \Delta V_{TX} \right\}. \tag{5.7}$$

Power consumption is a critical issue in modern serial link design, and this relationship motivates introducing equalization without running into the amplitude pre-emphasis gain limitation in (5.5) or power consumption demands.

5.3 Power and Signal Integrity in Bandwidth-Limited Channels

Ultimately, we are interested in the amount of transmit power required to equalize a bandwidth-limited channel. A performance analysis of amplitude pre-emphasis can be demonstrated when modeling the bandwidth limitations of modern interconnects with a first-order low-pass filter, where the cutoff frequency is chosen to close the eye. Modern high-speed serial links are limited by more severe environments as shown in Figure 2.5. The frequency domain representation of the first-order filter is

$$H_{channel}(s) = \frac{1}{1 + s\tau}. \tag{5.8}$$

The data eye is closed when the step response of this function does not reach the midpoint between the logical levels in one period, i.e. one-half for binary data. Therefore, $1 - e^{-T/\tau} = 1/2$, and channel time constant, τ, is $\tau = T\ln(0.5) \sim 0.69T$. The 3dB cutoff frequency, f_c, is 0.11 of the bit rate, f_b.

The cascaded transfer function of the pre-emphasis transmitter and the channel is

$$H_{link}(s) = H_{channel}(s) \cdot H_{preemp}(s) = I_{bias}(1-G)\frac{1 + s(T/2)(1+G)/(1-G)}{(1 + s\tau)(1 + s(T/2))}. \tag{5.9}$$

The response to a bit period pulse in the transfer function in (5.9) is

$$y(t) = \begin{cases} 0 & t > 0 \\ I_{bias}\left[1 - G - \left(1 + G\frac{T+2\tau}{T-2\tau}\right)e^{-\frac{t}{\tau}} + \left(\frac{2GT}{T-2\tau}\right)e^{-\frac{2t}{T}}\right] & T > t \geq 0 \\ I_{bias}\left[\left(1 + G\frac{T+2\tau}{T-2\tau}\right)\left(e^{\frac{T}{\tau}} - 1\right)e^{-\frac{t}{\tau}} - (e^2 - 1)\left(\frac{2GT}{T-2\tau}\right)e^{-\frac{2t}{T}}\right] & t \geq T \end{cases} . \quad (5.10)$$

The timing margins and voltage margins can be determined directly from the isolated bit-period pulse response for a first-order system or well-damped second order system [89], as discussed in Chapter 3. A family of curves is illustrated in Figure 5.2 for $f_c = 0.1f_b$ and fixed I_{bias}. Without pre-emphasis gain, the signal will not reach the voltage threshold, v_{th}, within the bit period. Too little pre-emphasis gain still results in an ISI impairment. Too much pre-emphasis gain causes overshoot, and the margins are reduced from lower signal swing in (5.3). With excessive pre-emphasis gain, the margins are limited by the minimum swing in (5.4). For linear systems, the voltage margin at this sampling point is

$$\Delta V = \begin{cases} 2(y(t_s) - v_{th}) & 50\Omega \cdot I_{bias}(1-G) > y(t_s) \\ 50\Omega \cdot I_{bias}(1-G) & 50\Omega \cdot I_{bias}(1-G) < y(t_s) \end{cases} . \quad (5.11)$$

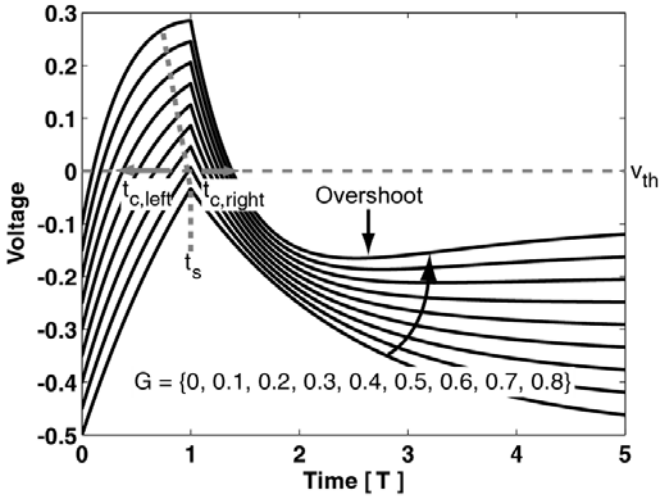


Figure 5.2 Pulse response curves for different pre-emphasis gains (f_c=0.1f_b).

The timing margin for the data eye of (5.9) can be calculated by comparing the rising and falling edge of the pulse response. The threshold crossing times are denoted t_c and are calculated from intersection of the pulse response, $y(t)$, with the voltage threshold, v_{th}, at $y(t_{c,left}) = v_{th}$ for the rising edge of the pulse, and $y(t_{c,right}) = v_{th}$ for the falling edge. When T is greater than the timing margins of the pulse response, $t_{c,right}$ - $t_{c,left}$ represents the minimum margin [89]. Any other transmitted sequence will have a large timing margin. When the pulse response margins are greater than T, the pulse response is overcompensated and the bit margins are reduced. For (5.10), the timing margins are

$$\Delta T = \begin{cases} t_{c,\,right} - t_{c,\,left} & T > t_{c,\,right} - t_{c,\,left} \\ 2T - (t_{c,\,right} - t_{c,\,left}) & T < t_{c,\,right} - t_{c,\,left} \end{cases}. \tag{5.12}$$

The voltage and timing margins are solved numerically for the pulse response of the transfer function in (5.9) with $f_c = 0.1f_b$ in Figure 5.3. The rising and falling threshold crossing times are plotted where G and I_{bias} is fixed and give the timing margin. Using the timing margin to calculate the sampling time, the voltage margin is also determined. Several conclusions about pre-emphasis can be reached from this plot. First, the minimum G for eye opening is 0.1. Second, the optimal G occurs around 0.55. Finally, the maximum

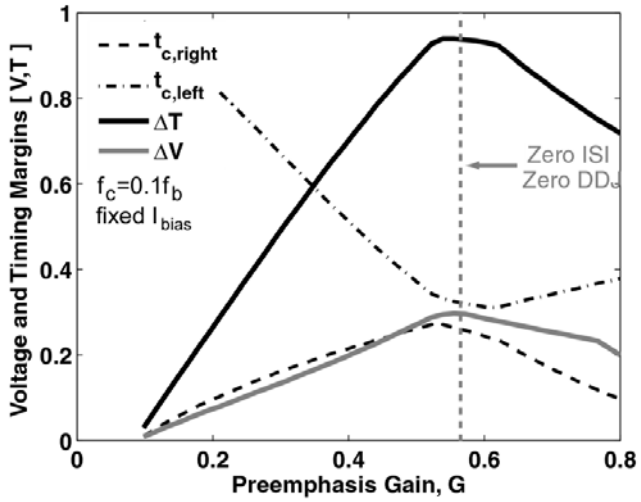


Figure 5.3 Variation of signal integrity with pre-emphasis gain.

voltage margin is reduced significantly from the full signal swing of 1V. Additionally, we note that the left edge improves much faster than the falling edges for increased *G*, which is also evident in Figure 5.2.

With these relationships between signal integrity and pre-emphasis gain we can numerically calculate the power required to open the data eye to specified voltage and timing margin. The power contour in Figure 5.4 illustrates the trade-offs in opening the data eye. The minimum receiver differential swing is 200mVpp and the acceptable timing margin is ΔT=0.75T. These minimum margins constrain the range of G and I_{bias} that can be used. Additionally, the peak transmitted swing is 1Vpp across the 50Ω load and imposes an additional constraint on G and I_{bias}. Recalling (5.2), the zero of the pre-emphasis response places an additional restriction on the power contour and depends on the channel bandwidth that must be compensated. The pre-emphasis gain is increased until both margin conditions are met. From this power contour, the lowest power consumption to reach the desired voltage and timing margins is determined.

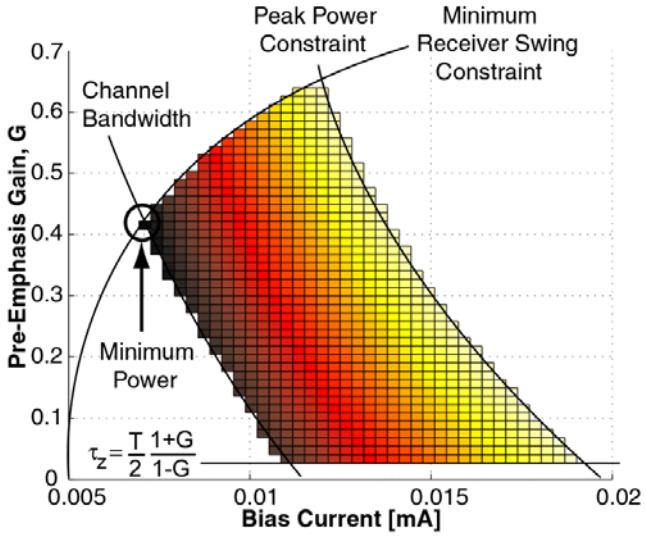


Figure 5.4 Constrained power contour for channel with first-order response (f_c=0.2f_b).

5.4 Phase Pre-emphasis

To alleviate the timing margin requirements in the data, phase pre-emphasis is introduced to the transmitted signal to compensate DDJ. In this section the operation of the phase pre-emphasis is described. In Chapter 3 the relationship between the channel response and the DDJ is established. In particular, it is shown that the DDJ is related to previous transitions. If we assume that the channel is linear, the timing deviation of complementary signals, i.e. a 101 and 010 data sequences, is identical. In [98] we demonstrated the adjustment of the data transition timing at the receiver to compensate for the effect of DDJ. This work focuses on DDJ compensation in the transmitter, where there are several implementation advantages.

The impact of previous transitions on the DDJ tends to increase with more recent transition. This is described in Chapter 3, where the DDJ resulting from a first-order response was shown to depend on when the previous transition occurred. In Figure 5.5 the transitions of the data eye are magnified. In particular, the timing deviations due to

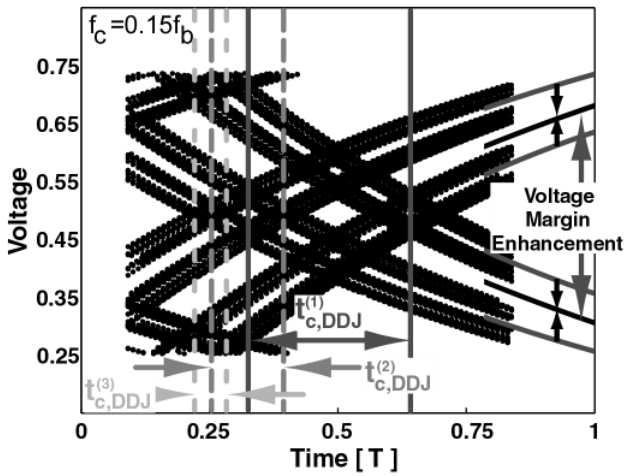


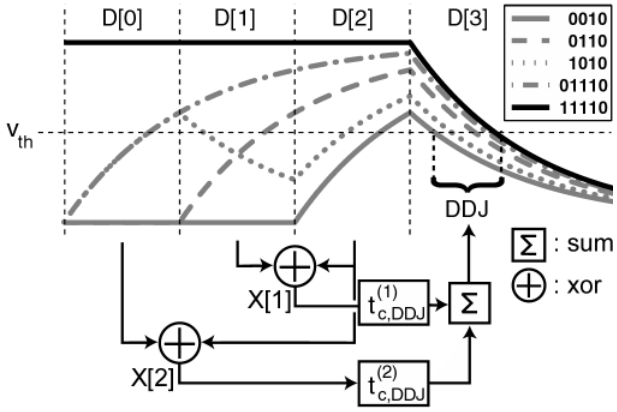
Figure 5.5 Data eye showning the contribution to data-dependent jitter of previous transitions.

previous bits are shown. For the *k*th previous transition, the transition between the -*k* and -*k-1* bit, we denote the timing deviation as $t_{c,\,DDJ}^{(k)}$, the conditioned mean described in (3.9). For instance, the first transition describes the transition between the previous and the penultimate bit. Figure 5.5 illustrates that the magnitude of the DDJ due to the *k*th transition tapers off quickly. After the third transition, the magnitude is small compared to the period. Phase pre-emphasis manipulates the data transitions to neutralize DDJ.

The relationship between different data sequences and the threshold crossing time is illustrated in Figure 5.6. A few data sequences are plotted to demonstrate the associated timing deviation and to illustrate the operation of the pre-emphasis scheme. Detection of each previous transition is used to compensate the current transition time. The detection of *k*th previous transition is denoted $X[k]$ for the current bit, $D[n]$, and is calculated from $X[k] = D[n-1] \oplus D[n-1-k]$, where $\oplus$ is the XOR operator. The compensated transmit time is calculated through the following algorithm.

$$t_{comp}[n] = X[1]t_{c,\,DDJ}^{(1)} + X[2]t_{c,\,DDJ}^{(2)} + X[3]t_{c,\,DDJ}^{(3)}. \tag{5.13}$$

For example, the 0010 sequence results in the fastest threshold crossing time for a first-order system. For this sequence, $X[1]$ and $X[2]$ are both one, implying that we will introduce the largest delay to compensate the fast transition for this sequence. On the other



D[0]	D[1]	D[2]	D[3]	X[1]	X[2]	t_{comp}
0	0	1	0	1	1	$t_{c,DDJ}^{(1)}+t_{c,DDJ}^{(2)}$
0	1	1	0	0	1	$t_{c,DDJ}^{(2)}$
1	0	1	0	1	0	$t_{c,DDJ}^{(1)}$
1	1	1	0	0	0	0

Figure 5.6 Phase pre-emphasis operation and truth table for compensating DDJ.

hand, the 1110 sequence results in the slowest threshold crossing time. For this sequence *X*[1] and *X*[2] will both be zero and the transmitter will introduce not introduce delay in the transmitted bit timing. In this example, we illustrate two 1110 curves corresponding to whether the initial condition, the unshown previous bit, is zero or one. Ideally, compensation is introduced for each previous transition until the DDJ contributed by these two curves is negligible.

In Figure 5.7, we demonstrate how phase pre-emphasis, along with amplitude pre-emphasis, introduces DDJ and ISI to the signal that is removed by the loss mechanisms in the serial link. The combination of both approaches can provide more signal integrity. In essence, the feed-forward amplitude pre-emphasis is a symbol-spaced FIR filter. The addition of phase compensation is to introduce an approximation for a half symbol-spaced FIR filter. While the use of amplitude pre-emphasis alone can provide some improvement in the DDJ, the symbol-spaced FIR filter cannot generally adjust the DDJ and the ISI to be simultaneously zero. Consequently, the use of half symbol-spaced FIR filters can minimize both the DDJ and ISI.

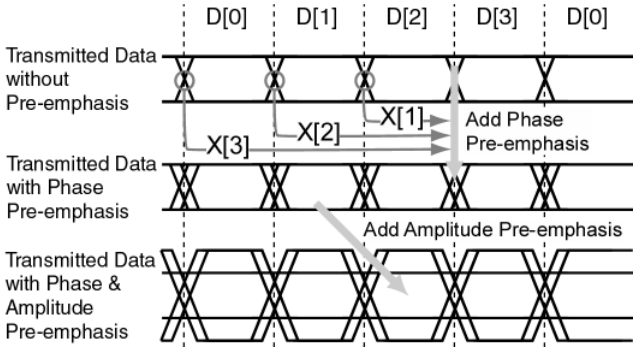


Figure 5.7 Operation of phase and amplitude pre-emphasis.

For the purposes of this work the coefficients of the equalizer are assumed to be adjusted *ad hoc*. The DDJ in simple LTI systems can be solved exactly to calculate the necessary timing compensation but generally some pulse response characterization or equalizer adaptation is required to adjust both phase and amplitude pre-emphasis coefficients. The coefficients for the phase pre-emphasis could be compensated by sampling the timing deviation at the receiver for particular transmitted data sequences. For instance, in Figure 5.6 the 0110 sequence introduces the delay $t_{c,\,DDJ}^{(2)}$ while the 0101 sequence introduces the delay $t_{c,\,DDJ}^{(1)}$. At the receiver, these particular sequences could be detected and a timing interval could be calculated from the mean transition timing. The coefficients would be transmitted back to the transmitter in a back-channel scheme.

Additionally, phase pre-emphasis improves the voltage margins. By aligning the transition deviations of the DDJ, the pulse response rises farther before the sampling time. This is illustrated in Figure 5.5, where the compensation of first transition brings the two separate groups of rising and falling edges together to a common edge. Consequently, the voltage margins between the slowest rising and falling edges increases.

The power-to-bit rate ratio (PBRR) is compared for a feed-forward transmitter with and without phase pre-emphasis. PBRR measures the marginal improvement between power consumption of the serial link and the equalization needed to achieve higher rates. Minimizing this ratio is important in environments where thousands of serial links operate simultaneously. First, we calculate the timing and voltage margins for each possible value

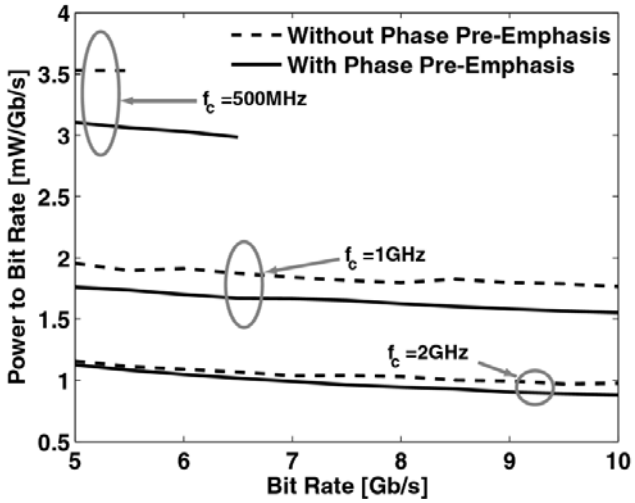


Figure 5.8 Power consumption as a function of bit rate for various channel cutoff frequencies with and without the use of phase pre-emphasis.

of G and I_{bias} and determine whether these parameters meet a minimum receiver differential swing of 200mV and timing margin of ΔT=0.75T. For all the G and I_{bias} that meet the margins, we choose the values that achieve the lowest power consumption according to (5.7), as in Figure 5.4. The phase pre-emphasis is assumed to consume no power, which is not the case, but the difference in power with and without phase pre-emphasis indicates the power target that must be met to make phase pre-emphasis worthwhile. The calculation is performed over numerous bit rates to observe the trend in power consumption with and without phase pre-emphasis for several different channel bandwidths.

The result of this calculation is shown for three different channel cutoff frequencies in Figure 5.8. For f_c=2GHz, the power consumption with phase pre-emphasis is improved by about 0.1mW/Gb/s. For f_c=1GHz, the difference between the minimum power consumption with and without phase pre-emphasis increases to 0.25mW/Gb/s. Additionally, it is clear that the power-to-bit rate ratio decreases slowly with higher bit rates. For f_c=500MHz, the difference in the PBRR is around 0.5mW/Gb/s and changes slightly over the range of achievable bit rates. Clearly, phase pre-emphasis extends the achievable bit rate by 1Gb/s. This illustrates that the use of phase pre-emphasis can

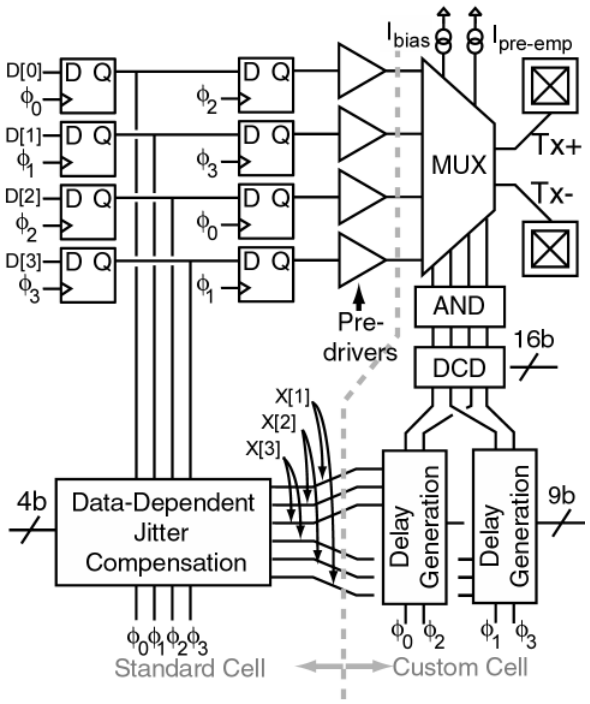


Figure 5.9 Transmitter schematic showing DDJ computation from parallel data and delay generation in clock path. Clock phases are independently adjusted for DCD and ANDed at output multiplexer.

provide some power savings for each serial link given that the power consumption for phase pre-emphasis does not overwhelm the power consumption savings.

5.5 Circuit Implementation

The architecture for the low-power phase and amplitude pre-emphasis transmitter is illustrated in Figure 5.9. The design is based on a 4:1 output multiplexer to provide amplitude pre-emphasis, combinatorial logic for phase pre-emphasis, delay generation cells for controlling the clock edges of the multiplexer, and duty-cycle control for each clock phase, which is useful for counteracting process variations. Each of the quarter-rate clock phases is ANDed with its neighbor to generate a 25% duty cycle clock at the 4:1 multiplexer.

The transmitter is implemented in IBM CMOS 9SF, a 90nm bulk triple-well CMOS technology. Static logic in this technology operates above 2Gb/s, and, consequently, can

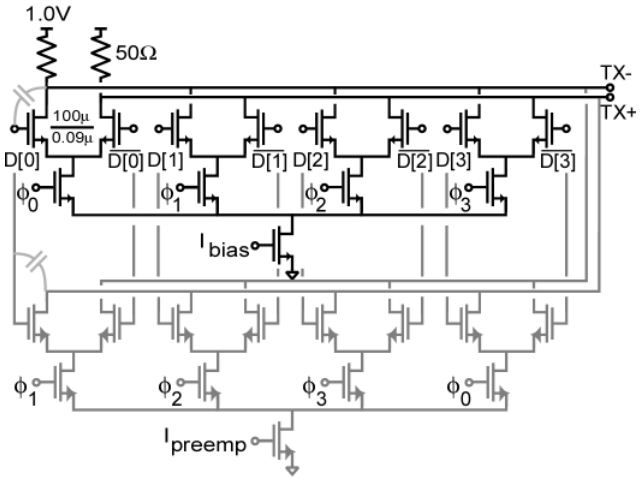


Figure 5.10 Output multiplexer schematic. The primary 4:1 multiplexer, in black, transmits the current data bit, while the pre-emphasis multiplexer, in gray, is cross-coupled to transmit an inverted replica of the previous data bit.

directly drive a 4:1 output multiplexer, lowering the power dedicated to a pre-driver. The output multiplexer is a current-mode logic (CML) stage which is linear, operates at a low supply voltage, and has a relatively fixed large-signal output impedance to avoid strong reflections present in other low-power transmit schemes [99].

Furthermore, the 4:1 output multiplexer provides interesting advantages when considering amplitude pre-emphasis [108]. The output multiplexer is illustrated in Figure 5.10. Each bit is transmitted sequentially and is available for three bit periods during which the next bit must be set-up. Using two cross-coupled multiplexers we can implement one-tap pre-emphasis. The first multiplexer transmits the original bit, and the second multiplexer is cross-coupled to invert the signal during the following period. Sequential clock phases trigger the two multiplexers to provide one bit delay. Therefore, the 4:1 multiplexer adds pre-emphasis to the output data without requiring additional circuitry and power to latch and hold the data. The only cost to this scheme is the additional pre-driver current required to drive twice the capacitance at the input of the output stage. However, this pair of cross-coupled multiplexers also reduces the ISI and DDJ inherent in the output multiplexer architecture. The gate-drain capacitance of the output stage provides a parasitic path for energy coupling between the input and output as

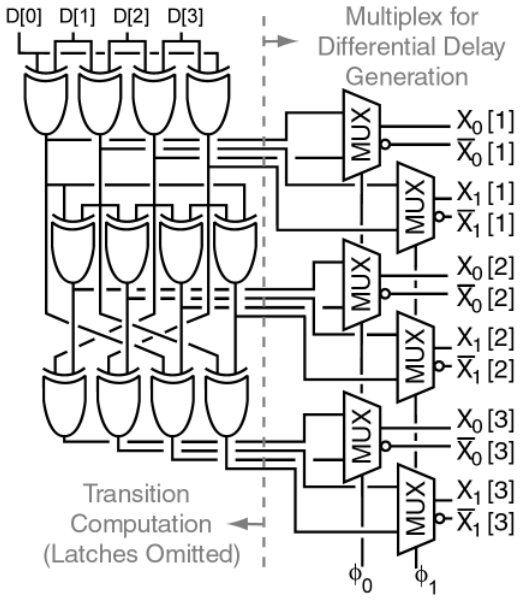


Figure 5.11 Phase pre-emphasis implementation. The logical gates calculate the existence of transitions in the data sequence for the past four bits. The multiplexers adjust the clock phase.

shown in Figure 5.10. With the cross-coupled multiplexer, the gate-drain capacitance is neutralized. The accuracy of this neutralization is subject to the limits of process variations and mismatch for these large output multiplexer transistors (W = 100μm) [110]. The output swing, ΔV, is designed for 600-mVpp differential, a trade-off between the link sensitivity requirement and the headroom restrictions of a 1V supply.

The phase pre-emphasis combinatorial logic is shown in Figure 5.11. The stage is implemented with standard cell static logic. The transitions in the data are calculated with a cascade of XOR stages that implement the algorithm in (5.13). Each stage of XORs calculates a previous transition in the data. The transition calculations are stored with a DFF at each stage to store the transition calculation. The pre-emphasis calculation results in three bits for each of the four lines. Each line adjusts an appropriate clock phase.

A 3GHz quadrature differential clock generates the four phases used in a quarter rate architecture as shown in Figure 5.12. The first and third clock phases are fully differential and control the timing of the first and third bits. The second and fourth clock phases are fully differential and control the timing of the second and fourth bits. Therefore, the transition detection output of the phase pre-emphasis combinatorial logic must be muxed

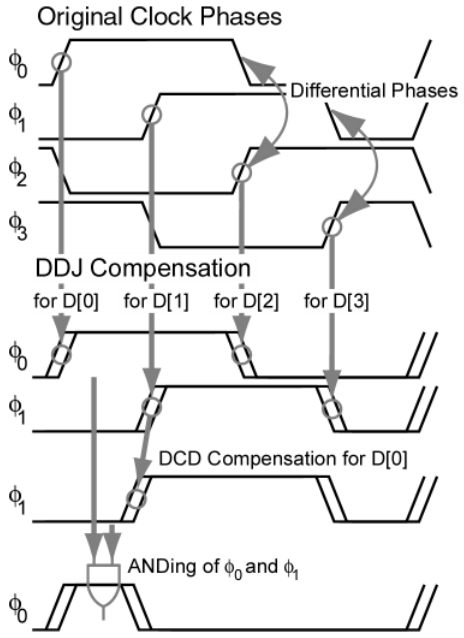


Figure 5.12 Delay introduction and clock duty cycle operation. Four clock phases are individually adjusted for the DDJ compensation and then ANDed to create the appropriate duty cycle.

to a 3GHz rate and control the rising and falling edges of the clock for the first and third bits, respectively. For instance, the rising edge of one differential clock controls the output timing of the first bit while the falling edge of this clock controls the output timing of the third bit. Consequently, the transition multiplexer introduces the phase pre-emphasis for the first and third bits for the rising and falling edges, individually. This multiplexer is modulated with the quadrature differential clock to ensure the appropriate setup and hold times.

The transition multiplexer output signals switch two independent delay generation cells that handle each of the quadrature differential clocks. These delay generation cells, shown in Figure 5.13, are designed with fully differential CML logic to benefit from the power supply rejection on the clocks. Each delay generation cell consists of a cascade of three 3b programmable delay cells. The delay generation is provided by multiplexing between two versions of the clock: one programmable delay and one nominal delay. The programmable delay is introduced when a transition is detected in the transmitted data. Each consecutive delay cell is used to handle the timing deviation corresponding to a

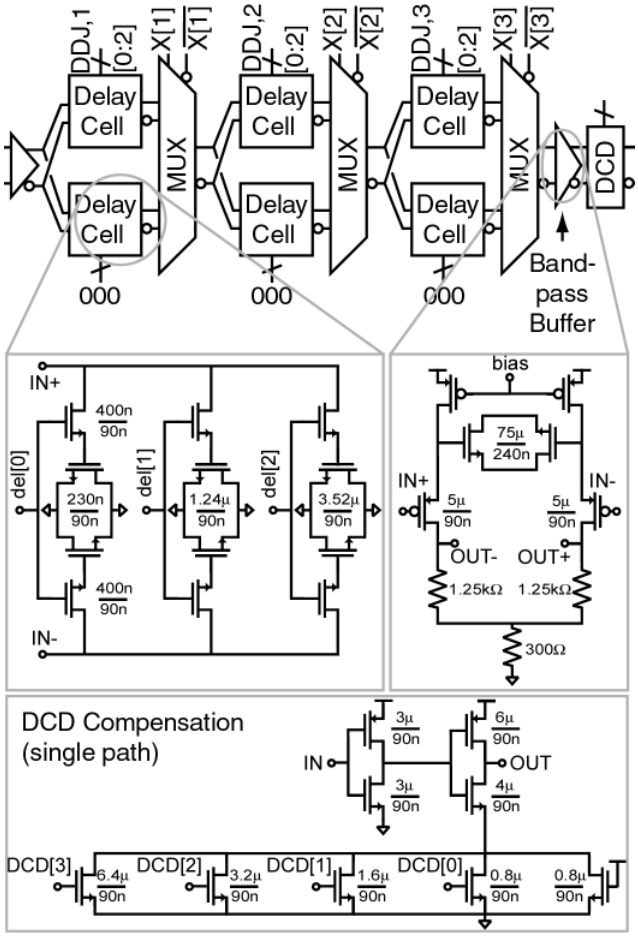


Figure 5.13 Delay generation schematic. Detailed schematics are presented for the delay cell, clock amplifier, and DCD compensation circuits.

previous transition. The programmable delay cell is designed to provide 1.5ps of delay for each digital bit. Consequently, the maximum $t_{c,\,DDJ}^{(k)}$ that can be implemented is 16ps.

The output buffer of the delay generation cell is designed as a bandpass buffer stage to reject low-frequency noise. Since the phase pre-emphasis scheme is implemented by modulating the clock phases as opposed to modulating the data edges as in [98], bandpass buffering can be used to pass only frequency content around the 3GHz clock. The bandwidth of the bandpass must meet the phase modulation requirements for the clock. A source degenerated PMOS driver is implemented to provide low-frequency noise rejection.

At this point the fully differential clocks are split into four different clock phases and duty cycle distortion (DCD) is compensated. DCD control is implemented through four individual pathways, each with four control bits as illustrated in Figure 5.9. Independent DCD control allows adjustment for process and transistor matching variations that influence the duty cycle of each data path [108]. Since the DCD is a static adjustment, it will not interfere with the DDJ adjustment on the clock. The compensation of DCD for each clock phase is illustrated in Figure 5.12.

Finally, neighboring clock phases are ANDed together. This ideally converts each clock phase to a duty cycle of one-quarter the bit period. Notably, ANDing neighboring clock phases is useful for the phase pre-emphasis scheme. The DDJ timing variations are introduced to the clock phase that ends the transmission of the current bit. This phase also triggers the transmission of the consecutive bit. Hence, we avoid any clock overlap issues that might otherwise arise from introducing timing variations on four different clock phases.

5.6 Results

Two break-out sites are shown in Figure 5.14. The top break-out is the entire output transmitter without the phase pre-emphasis capability. The bottom site is the entire

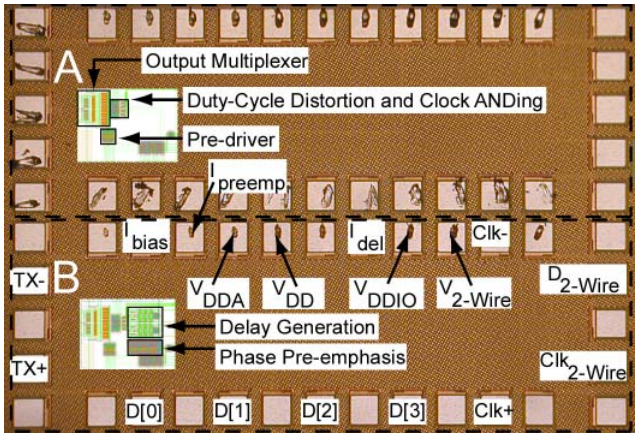


Figure 5.14 Chip microphotograph of two breakout sites. Top site does not have phase pre-emphasis. Bottom site features phase pre-emphasis.

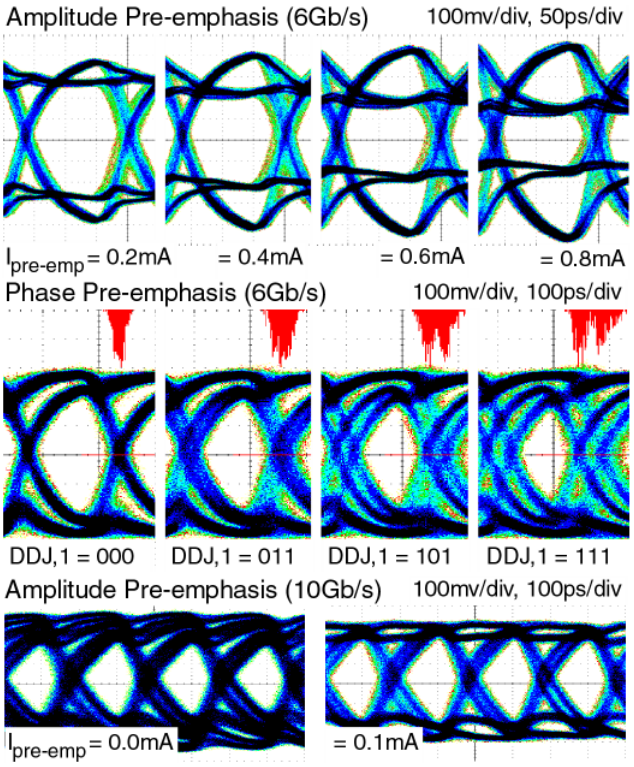


Figure 5.15 Data eyes at 6Gb/s and 10Gb/s demonstrating amplitude and phase pre-emphasis. The first row shows the amplitude pre-emphasis at 6Gb/s as a function of pre-emphasis current. The second row illustrates the phase pre-emphasis as a function of the compensation code.

transmitter with the phase pre-emphasis capability. The total area of the transmitters is 240µm by 150µm, roughly the area required for two pads. The transmitters also include a two-wire interface for programming the DCD and DDJ delay cells.

The operation of the amplitude and phase pre-emphasis is demonstrated in Figure 5.15. The first set of eyes show amplitude pre-emphasis with increasing pre-emphasis current at 6Gb/s. The pre-emphasis gain is set through a reference current that is recorded for each data eye. As shown in the figure, the minimum swing decreases while the maximum swing increases with pre-emphasis current. The second row of data eyes show the use of phase pre-emphasis. The DDJ introduced to the signal depends on the digital code used to program the delay generation scheme. The first transition, $t_{c,\,DDJ}^{(1)}$, is compensated, and the two resulting threshold crossing times are observed from the jitter histogram. The separation between the peaks increases with the code value. For the 000

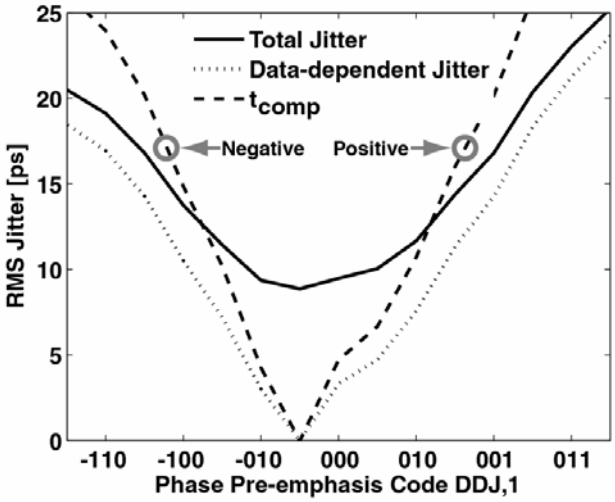


Figure 5.16 Total and data-dependent jitter versus phase pre-emphasis codes for the first previous transition. The variation in DDJ can be used to calculate the time delay variation.

code, the rms jitter is 10.05ps. For 011, the jitter increases to 14.38ps. For 101, the jitter is 20.36ps and reaches 25.24ps for 111. Finally, the bottom row of data eyes demonstrates the operation to 10Gb/s of the transmitter without pre-emphasis. The use of amplitude pre-emphasis opens the data eye slightly at 10Gb/s to counteract the limited bandwidth of the transmitter stage. Four consecutive eyes are shown to demonstrate the relative DCD matching between each of the four paths in the multiplexer.

The separation between the peaks increases with the code value. The variation in the total jitter is measured as a function of the pre-emphasis code in Figure 5.16. The DDJ component is normalized out of this total jitter and the time delay compensation can be caculated from the DDJ peak separation. The linearity of the time delay compensation is assessed from the slope of this curve curve as a function of the digital code.

To test the transmitter featuring phase and amplitude pre-emphasis, a 2^{31-1} pseudo-random bit sequence at 6Gb/s was passed through two test channels. The first channel, 96” of RG-58 cable, has 4dB of loss at 3GHz. Three data eyes are illustrated in Figure 5.17. The first is the eye without any compensation. The second eye is compensated using the first-transition phase pre-emphasis. The rms jitter reduces from

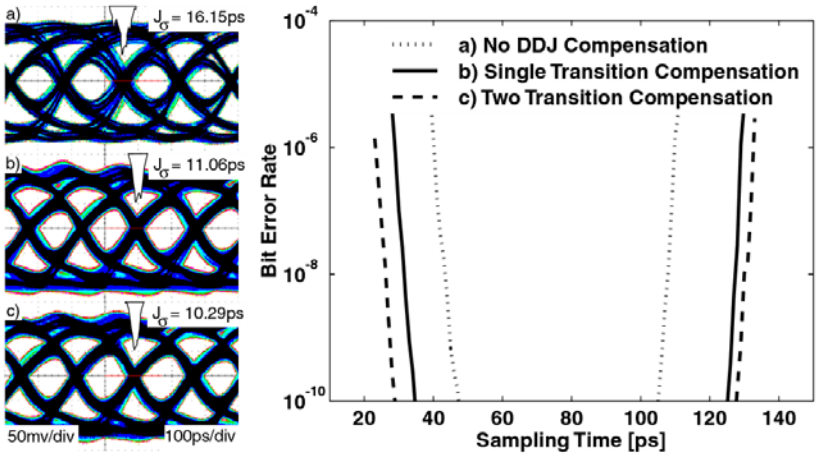


Figure 5.17 Performance on 96” of RG-58 cable. The uncompensated eye is shown in a) while phase pre-emphasis is introduced in b) and c).

16.15ps to 11.06ps when the DDJ code is 011. The third eye includes first- and second-transition pre-emphasis, and the rms jitter drops to 10.29ps with the DDJ code for the second transition set to 001. The RJ is measured from a periodic pattern and has a jitter of 8.06ps. The BER bathtub curve demonstrates that at 10^{-9} BER the timing margin increases from 62ps to 95ps with first transition pre-emphasis, and compensating the second transition opens the bathtub by an additional 6ps.

The second channel, a 16” FR-4 backplane interconnect with Tyco Hm-Zd connectors, has 10dB of loss at 3GHz. The high frequency-dependent attenuation in this case is reflected in the closed data eye shown in Figure 5.18. Amplitude pre-emphasis is used exclusively in the first data eye. With the data eye open, phase pre-emphasis is used to open the eye further. The change in the rms jitter is demonstrated is a function of the pre-emphasis (DDJ,1) code in Table 5.1. Clearly, DDJ,1 = 010 minimizes the rms jitter in the data eye. The rms jitter reduces from 13.84ps to 10.24ps using first transition phase pre-emphasis. The improvement at 10^{-9} BER is shown across sampling times and voltage

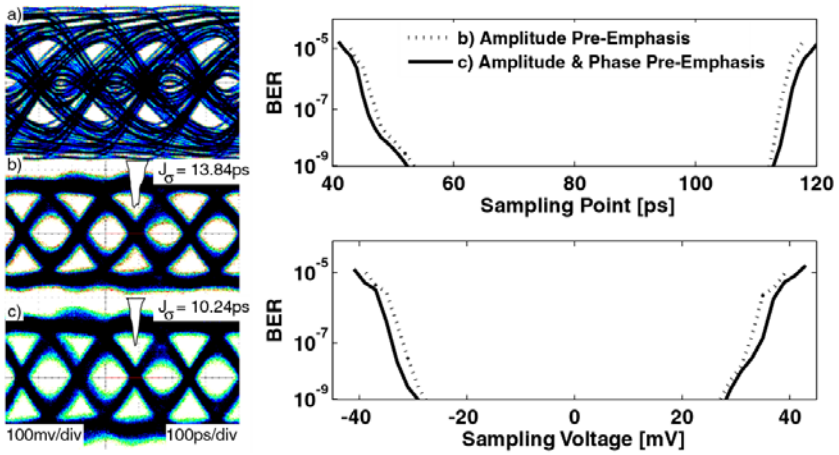


Figure 5.18 Performance on 16” of FR-4 backplane with connectors. The uncompensated eye is closed in a). In b), amplitude pre-emphasis opens the eye and phase pre-emphasis improves the DDJ in c).

thresholds. Notably, the phase pre-emphasis opens the data eye slightly in the time domain and voltage domain.

Table 5.1 Measured RMS jitter across Backplane versus Phase Pre-emphasis Codes

Code	**-100**	**-011**	**-010**	**-001**	**000**	**001**	**010**	**011**	**100**
TJ	21.5ps	19.9ps	17.3ps	14.8ps	13.8ps	10.9ps	10.2ps	11.3ps	13.9ps

The transmitter nominally operates at 1.0V but can operate from 0.8V to 1.2V, offering a trade-off between power consumption and performance. The transmitter without phase pre-emphasis consumes a minimum of 18mW of power at 6Gb/s with a 600mVpp swing, giving a power budget of 3mW/Gb/s. The output multiplexer draws 12mA while the data buffers and clock driver, including DCD control and phase ANDing, consume the remaining 6mA from a 1V supply. The power consumption of the two-wire interface and clock generation are not included in this power. Amplitude pre-emphasis increases the power budget through the current drawn through the pre-emphasis multiplexer. The transmitter with phase pre-emphasis consumes a minimum of 21mW of power at 6Gb/s, giving a power budget of 3.5mW/Gb/s. This additional power is consumed primarily in the custom designed CML delay generation stages and the pre-emphasis combinatorial

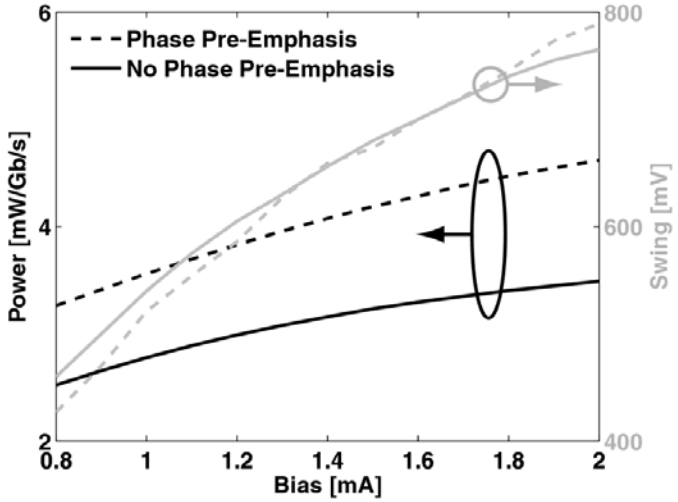


Figure 5.19 Power consumption per bit rate as a function of bias current.

logic. The power consumption is scanned with the bias current in Figure 5.19 to show the achievable signal swing and power consumption. The voltage swing is demonstrated on the right axis, and the power consumption is on the left axis. As expected, the voltage swing tracks the power consumption for both implementations of the transmitter. The transmitter with phase pre-emphasis demands roughly 0.5mW/Gb/s more over the entire output swing range. If we compare this to the theoretical result in Figure 5.8, we conclude phase pre-emphasis is only slightly advantageous to implementing the transmitter with just amplitude pre-emphasis. However, the power consumption of the phase pre-emphasis scheme is not fundamentally limited to 0.5mW/Gb/s, and migration of the delay generation from CML logic to static logic should realize additional power advantages.

5.7 Summary

This work describes a novel equalization technique for amplitude and phase pre-emphasis to extend data rates in bandwidth-limited interconnects. Phase pre-emphasis is introduced to compensate for data-dependent jitter introduced over the channel. The analysis discusses the power trade-offs of amplitude pre-emphasis and demonstrates the power advantage and bandwidth advantage of using phase pre-emphasis. This amplitude

and phase pre-emphasis transmitter is implemented in 90nm CMOS. The architecture builds upon a 4:1 multiplexer that allows for efficient implementation of both pre-emphasis schemes through the use of standard cell logic. The transmitter consumes between 18-21mW of power at 6Gb/s, giving a power budget of 3-3.5mW/Gb/s/channel. The transmitter operation is demonstrated to reduce the rms jitter over a 96” cable from 16.15ps to 10.29ps using only phase-pre-emphasis. In a backplane interconnect with connectors, amplitude pre-emphasis is used to overcome the high attenuation. When pre-emphasis is introduced the rms jitter is reduced from 13.84ps to 10.24ps. The corresponding improvement in the voltage and timing margins is demonstrated at 10^{-9} BER.

Chapter 6 Crosstalk-Induced Jitter

6.1 Introduction

Broadband communication links face many signal propagation challenges as speeds move into microwave frequencies. In particular, dense environments, required to satisfy demand for high aggregate throughput, need special consideration to meet future data rates. At high-frequencies, serial links are susceptible to electromagnetic interference as well as strong attenuation and reflections caused by poor electrical interfaces. Backplane interconnects are particularly limited at higher-frequencies. These interconnects suffer from attenuation due to skin losses, via stubs, and connectors, severely limiting the signal integrity [52][111][112]. In backplanes as well as integrated circuit environments, a premium on space precludes creating completely shielded links. Different data sequences are transmitted across parallel interconnects. The mutual capacitance and inductance induces fluctuations on adjacent transmission lines. Crosstalk results from the interaction

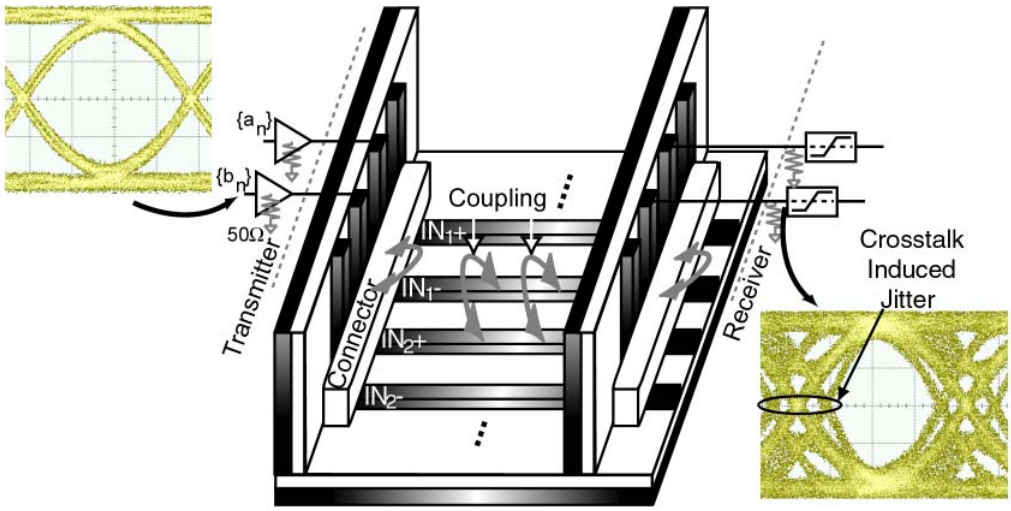


Figure 6.1 The crosstalk jitter generated in the data eye due to the influence of a neighboring signal.

of electromagnetic fields generated by neighboring data signals as they propagate through transmission lines and connectors as shown in Figure 6.1. Two signals are transmitted simultaneously from the receiver on the left. As the two data sequences propagate along the transmission lines, energy couples from one link to the neighbor. This coupling manifests as near-end crosstalk (NEXT) at the receiver and far-end crosstalk (FEXT) at the transmitter [77]. Additionally, backplane connectors introduce multi-pin crosstalk. When signal transitions occur, high-frequency energy couples between adjacent wires. At the receiver, the timing of both data eyes is obscured as shown in the figure. This timing deviation due to FEXT is called crosstalk-induced jitter (CIJ). While FEXT causes CIJ, CIJ behaves differently than FEXT for digital modulation schemes. In particular, CIJ is insensitive to signal swing and rise time. CIJ is a type of bounded-uncorrelated jitter (BUJ), a subset of deterministic jitter (DJ) [40][41]. DJ reduces the sampling range of the data eye, degrading the bit error rate (BER) [39].

As link rates increase, more electromagnetic energy is coupled into neighboring channels. A review of crosstalk mechanisms in different backplane and on-chip interconnections is offered by A. Deutsch [52]. In VLSI applications wiring capacitances tend to dominate interconnect crosstalk [112] and also affect the performance of integrated digital circuits.

This chapter reviews crosstalk in signals on coupled lines. We review the basic crosstalk generation in Section 6.2. The impact of crosstalk on jitter is described in Section 6.3. The discussion of crosstalk induced jitter is extended to PAM4 in Section 6.4.

6.2 Crosstalk in Transmission Lines

A lumped-element model for the transmission lines demonstrates the effect of coupled electromagnetic energy in Figure 6.2. The model consists of the self capacitance, C_s, and inductance, L_s. The coupling occurs through the mutual capacitance, C_m, and the mutual inductance, L_m. The telegraphist's equations describe the spatial and temporal variation of voltage and current on the adjacent lines [113].

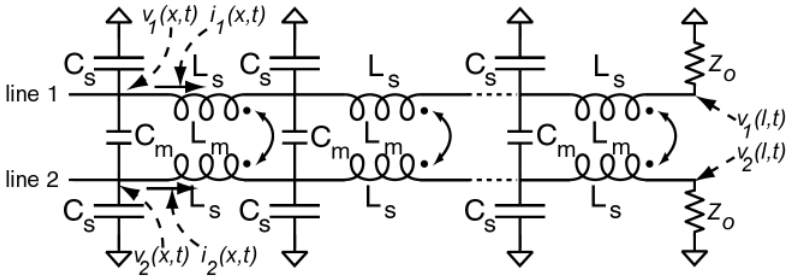


Figure 6.2 Lossless coupled transmission line model consisting of the self capacitance and inductance and mutual capacitance and inductance.

$$\frac{\partial}{\partial z}\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = -\begin{bmatrix} L_s & L_m \\ L_m & L_s \end{bmatrix}\frac{\partial}{\partial t}\begin{bmatrix} i_1 \\ i_2 \end{bmatrix}$$
$$\frac{\partial}{\partial z}\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = -\begin{bmatrix} C_s & -C_m \\ -C_m & C_s \end{bmatrix}\frac{\partial}{\partial t}\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \quad (6.1)$$

Solutions to this problem are eigenmodes associated with an even and odd mode. The even mode is excited when $v_1(x,t) = v_2(x,t)$ and the odd mode is excited when $v_1(x,t) = -v_2(x,t)$. Any arbitrary excitation is represented through a linear combination of these two modes. For data communications, we are concerned primarily with three modes: the even, odd, and superposition, when no data transition occurs. We illustrate these three situations in Figure 6.3. The even and odd mode effectively see two different coupling mechanisms. For instance, the even mode transition sees little coupling capacitance. The data transitions occur independently on adjacent lines and, therefore, the mode changes randomly. Consequently, we want to demonstrate the variation in the propagation time for transitions on the lines.

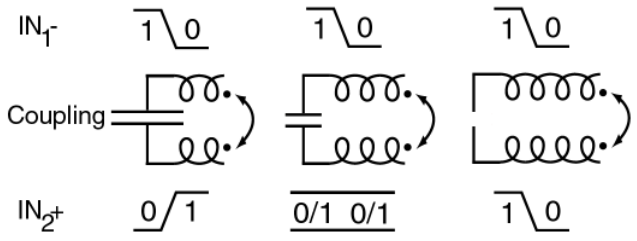


Figure 6.3 Electromagnetic modes that occur between the coupled transmission line during binary digital communication.

The impact of the coupling mode on data transitions is intuitively approached by calculating the time of flight (TOF). TOF is determined from the propagation constants for the eigenmodes. From [113], the propagation constants can be written as

$$\beta_o = \omega\sqrt{(L_s - L_m)(C_s + C_m)} \quad \text{and} \quad \beta_e = \omega\sqrt{(L_s + L_m)(C_s - C_m)}. \tag{6.2}$$

The relationship between the propagation constant and the phase velocity, $v_p = \omega/\beta$, determines the TOF. Consequently, the odd and even TOF are

$$T_o = l\sqrt{(L_s - L_m)(C_s + C_m)} \quad \text{and} \quad T_e = l\sqrt{(L_s + L_m)(C_s - C_m)}. \tag{6.3}$$

As expected, the TOF increases with the length, l, of the line. While the odd and even mode TOFs differ, the superposition mode is not readily determined due to the nature of pulse propagation down the line. As an edge propagates down the transmission line, it induces a voltage spike on the quiet adjacent line. This spike, in turn, propagates with the edge and grows in amplitude. Eventually, the spike will, in turn, influence the arrival time of the original edge.

The speed of the two modes are equal if $L_m/L_s = C_m/C_s$. This condition is guaranteed when the transmission line is homogeneous. Homogeneity holds in stripline transmission lines because of field symmetry. For microstrip lines, homogeneity is not generally guaranteed since the electric and magnetic fields above and below the line are not symmetric [114]. In general, interconnects are often implemented as microstrip and are inhomogeneous.

To determine the superposition mode arrival time, the FEXT generated between two transmission lines is solved. If we assume weak coupling between the lines, we can ignore the impact of secondary reflections (*i.e.* $\Gamma^2 \sim 0$). In this case, the even and odd mode voltages are delayed versions of the generator voltage. Additionally, the superposition essentially reduces to

$$v_{1(2)}(l, t) = \frac{1}{2}[V(t - T_e) \pm V(t - T_o)], \tag{6.4}$$

where the sum is for line 1 and the difference is for line 2. Therefore, the voltage on line 2 is zero if the two modes propagate at the same speed. In inhomogeneous lines they do not, and a voltage spike results on the line without a transition. The qualitative upshot of the weak coupling argument is that this spike does not in turn affect the line 1 significantly.

This derivation for weak coupling allows a Taylor series approximation of the modes [113]. The time of arrival for the superposition mode is thus expressed as

$$T = l\sqrt{L_s C_s - L_m C_m} \sim l\sqrt{L_s C_s}. \tag{6.5}$$

Consequently, we can express the even and odd modes as

$$T_{e(o)} \approx T\sqrt{1 \pm l\left(\frac{L_m}{Ls} - \frac{C_m}{C_s}\right)}, \tag{6.6}$$

where the even mode is the addition and the odd mode is the difference. The mode TOF demonstrated in (6.3) are perturbations of (6.5). Using the binomial expansion for the square root, this equation reduces to

$$T_{e(o)} \approx T \pm \frac{l}{2}\left(\frac{L_m}{Z_o} - C_m Z_o\right). \tag{6.7}$$

The perturbation in (6.7) can be expressed as a forward coupling time constant, τ_f, defined as

$$\tau_f = \frac{l}{2}\left(C_m Z_o - \frac{L_m}{Z_o}\right). \tag{6.8}$$

The forward coupling time constant behavior depends on the implementation. For high impedance lines, the capacitance dominates and $\tau_f \sim lC_m Z_o/2$ [112][114]. In this case, the odd mode is slower than the even mode. For low impedance lines, the inductance dominates and $\tau_f \sim lL_m/(2Z_o)$. In this case, the arrival time of the even and odd modes reverse.

Analytical results for strong coupling are difficult to reach. Furthermore, strong coupling is problematic for binary data communications since the waveforms are greatly distorted during transmission. It is useful to develop a limit on the coupling to determine

whether a given transmission line geometry will result in strong coupling. Coupling severely distorts the different waveforms when the arrival times of the even and odd mode become widely separated. When the odd mode occurs well before the even mode, for instance, the superposition mode does not interpolate smoothly between these two modes. Consequently, the transition of the superposition mode may no longer be monotonic.

Therefore, a useful limit on strong coupling relates the transition time of the waveform to the amount of coupling. To ensure that the even and odd edges begin and end in the same time interval,

$$t_r < 2\tau_f \,, \tag{6.9}$$

where t_r is the rise time (or fall time, whichever is longer) of the signal.

6.3 Crosstalk-Induced Jitter

While crosstalk-induced jitter is caused by FEXT, the behavior differs from FEXT in several ways. In this section, the TOFs of the even, odd, and superposition mode are incorporated into a model for data communications to define crosstalk-induced jitter (CIJ). Discussions and measurements of CIJ support these results.

Oftentimes, high-speed data are transmitted differentially. Between the differential lines, a virtual ground exists. Depending on the relative intra-pair and inter-pair spacing of the differential lines, CIJ depends on one adjacent data signal. The jitter on the differential lines, IN_1+ and IN_1-, might be generated by different neighbors. To simplify the analysis, we study coupling between only two neighbors. However, more sophisticated modeling can analyze the effect over a larger number of neighbors.

If adjacent transitions occur simultaneously, we can develop a time domain representation for the induced jitter. However, even with some timing skew between lines, the derivation of CIJ can still be applied, as will be discussed later. If we label $r_1(t)$ the victim signal and $r_2(t)$ the aggressor signal, these signals can be represented as

$$r_1(t) = \sum_{n=-\infty}^{0} a_n g(t-nT) \quad \text{and} \quad r_2(t) = \sum_{n=-\infty}^{0} b_n g(t-nT), \tag{6.10}$$

where a_n and b_n are independent data sequences and $g(t)$ is the pulse response of the channel, which is assumed to be identical on both lines. Following the derivation in [90], we calculate the arrival time of the victim signal at the decision threshold. When there is no aggressor present, $v_{th} = r_1(t_c)$ and variations of the threshold crossing time, t_c, are related to other sources of jitter (random and deterministic jitter). These jitter sources have been discussed extensively in Chapter 2 and Chapter 3. When the aggressor signal is present, the coupling introduces the data from the aggressor to the victim. The time constant derived in the previous section defines a high-pass filter and couples the high-frequency components of the aggressor data. Therefore, the arrival time in the presence of crosstalk, t_x, are found from the solution of this algebraic equation:

$$r_1(t_x) + \tau_f \frac{d}{dt} r_2(t_x) = v_{th}. \tag{6.11}$$

To calculate the threshold crossing time deviation due to crosstalk, we can apply a first-order Taylor series to the victim and aggressor signals using the original result for an unaffected signal. This is reasonable since oftentimes the rising edge is purely monotonic. The victim signal is approximated as

$$r_1(t_x) = \sum_{n=-\infty}^{0} a_n (g(t_c-nT) + (t_x - t_c) g^{(1)}(t_c-nT)). \tag{6.12}$$

In this expression, $g^{(1)}(t)$ is the first derivative of the pulse response. The first term in this equation represents the pulse response *without* the aggressor signal. Therefore, (6.12) becomes

$$\sum_{n=-\infty}^{0} a_n (t_x - t_c) g^{(1)}(t_c-nT) + \tau_f b_n g^{(1)}(t_x-nT) = 0. \tag{6.13}$$

Unfortunately, the argument of the derivative of the pulse response contains different times. To handle this, we make a Taylor series approximation for $g^{(1)}(t_x\text{-}nT)$. Consequently, we have a closed form solution for t_x.

$$t_x = t_c - \tau_f \frac{\sum_{n=-\infty}^{0} b_n g^{(1)}(t_c - nT)}{\sum_{n=-\infty}^{0} (a_n g^{(1)}(t_c - nT) + \tau_f b_n g^{(2)}(t_c - nT))} \tag{6.14}$$

Two approximations are particularly relevant. First, the numerator and denominator both contain the derivative of the pulse response. Typically, this derivative is strongest at the rising and falling edges (t_c = 0 and T), respectively. Consequently, all other terms in the summation can be assumed to be zero. Additionally, the solution simplifies further if we assume both the rising and falling edges have the are equal and opposite transitions, *i.e.* $g^{(1)}(t_c) = -g^{(1)}(t_c + T)$. Now,

$$t_x = t_c - \tau_f \frac{b_0 - b_{-1}}{a_0 - a_{-1} + \tau_f \frac{g^{(2)}(t_c)}{g^{(1)}(t_c)}(b_0 - b_{-1})}. \tag{6.15}$$

Finally, we can make the assumption that the second derivative of the slope can be taken to be zero near t_c. The threshold crossing time in the presence of the aggressor can be simply expressed as

$$t_x = t_c\text{-}\tau_f \cdot \frac{b_o - b_{-1}}{a_o - a_{-1}}. \tag{6.16}$$

The crosstalk-induced jitter is defined as

$$t_{c,\,CIJ} = -\tau_f \cdot \frac{b_0 - b_{-1}}{a_0 - a_{-1}}. \tag{6.17}$$

The denominator represents the transition in the victim data, and the numerator represents the transition in the aggressor data. Note that (6.17) is only valid when a transition occurs on the victim data, i.e. a_0 does not equal a_{-1}.

Most importantly, the details of $g(t)$ are not apparent in (6.17). This is an interesting result because it highlights the differences between CIJ and FEXT voltage noise. For FEXT, slower transitions generate less crosstalk-induced noise on the victim line [77]. However, in terms of jitter, the victim edges are also slow and more susceptible to jitter. Therefore, the CIJ is *not* sensitive (to the first-order) to the transition slope.

Additionally, the amplitudes of a_n and b_n cancel out of the ratio of the aggressor and victim data. This implies that the CIJ is independent of signal swing. Therefore, pre-emphasis does not significantly impact CIJ and cannot be used to improve it.

6.3.1 Experimental Measurements of Time of Flight

To verify these expressions for CIJ, a set of 8” single-ended microstrip lines were constructed with Rogers 5880 duroid ($\varepsilon_r = 3.3$). The dielectric thickness was 62.5mil and each 50Ω transmission line was 200mil wide. The coupled lines are designed with impedance matched to the superposition mode. The microstrip lines are separated by

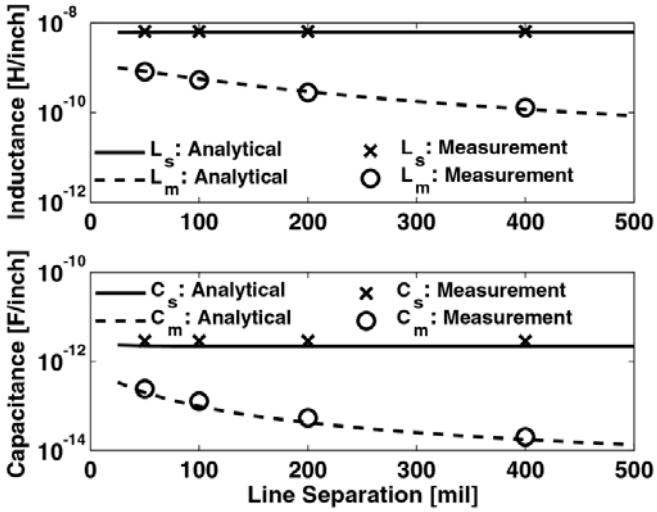


Figure 6.4 Comparison of calculated and measured inductances and capacitances for coupled microstrip lines on Rogers 5880.

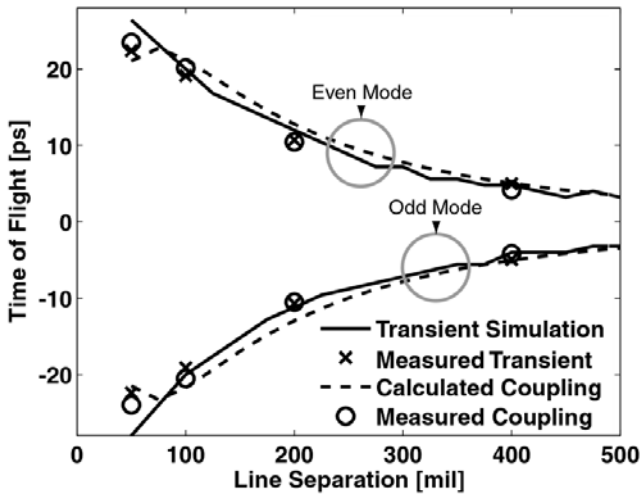


Figure 6.5 The time of flight for the microstrip lines normalized to each inch. The predicted mutual inductance and capacitance are compared to an ADS transient simulation.

50mil, 100mil, 200mil, and 400mil. The capacitance and inductance of the lines are calculated analytically from formulas presented in [115][116]. These calculated self inductance and capacitance and mutual inductance and capacitance are measured experimentally with an LCR meter. The inductance and capacitances match well at each of the line separations as shown in Figure 6.4.

The TOF of the even and odd modes is calculated from the extracted parameters in Figure 6.5. Furthermore, ADS transient simulations are also used to calculate the mode TOF. The superposition time of flight normalizes the plot so that the results reflect the differential TOF. The plot demonstrates that the TOF increases with decreasing line spacing. Furthermore, the odd mode travels faster than the even mode over the transmission lines indicating that the inductance is the dominant coupling effect for the transmission lines.

6.3.2 Effect of Timing Offset Between Victim and Aggressor

While, thus far, the analysis assumes isosynchronous signal transmission over the interconnect, CIJ is relatively insensitive to timing offsets between the victim and the aggressor. Examining our analysis for CIJ, a phase offset could be added in the numerator

or denominator. Notably, the slope of $g(t)$ in the numerator and denominator cancels out. At small timing offsets, the slope is constant and (6.17) still holds. Basically, we expect that the range of time when the crosstalk translates into CIJ follows the rise and fall time of the signal slope. For larger timing skew, the crosstalk occurs in the data eye and has little effect on the transition timing. Consequently, there is a phase offset at which CIJ becomes an amplitude ISI problem.

In Figure 6.6, the jitter is recorded as a function of the offset between the victim and aggressor signals. Both the peak-to-peak and rms jitter are recorded. Additionally, the arrival time of the even and odd modes is plotted on the right axis. Two features are striking. First, the CIJ is pronounced after a small offset range. Second, the peak-to-peak and rms jitter are essentially constant over a large range of offsets. A small minimum occurs in the rms jitter when the even and odd mode arrival times are equally spaced from the superposition mode.

Notably, in many backplane applications, the skew specifications for adjacent channels are much larger than the rise and fall times of the signals. Consequently, it is difficult to predict whether FEXT between a pair of adjacent signals will result in CIJ.

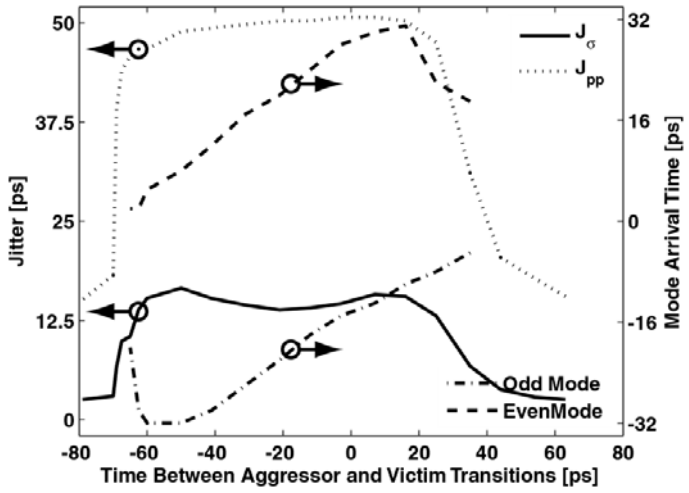


Figure 6.6 Timing offset between the aggressor and victim data at 5Gb/s does not dramatically affect the rms and peak-to-peak jitter.

6.4 Crosstalk Jitter in M-PAM

Recent papers have proposed the use of 4-PAM to overcome channel limitations [30]-[28], and we can discuss the jitter issues relevant to 4-PAM. In this section the CIJ expression is applied to 2-PAM and 4-PAM schemes, and we develop expressions for rms and peak-to-peak expressions for the jitter based on uncoded data statistics. These expressions are useful in comparing 2-PAM and 4-PAM in terms of the CIJ penalty.

6.4.1 2-PAM

For binary data ($a_n = \{0,1\}$), the ratio in (6.17) can assume only three different values: -1, 0, and 1. Thus, the coupling spreads the transition time of the victim data (and, symmetrically, the aggressor data) between three discrete values as shown in the original eye in Figure 6.1. The probability density function is

$$PDF_{CIJ}(t_c) = \frac{1}{4}\delta(t_c + \tau_f) + \frac{1}{2}\delta(t_c) + \frac{1}{4}\delta(t_c - \tau_f). \tag{6.18}$$

The middle, unaltered data transition occurs twice as frequently because the superposition mode occurs twice as often as either the odd or even modes. With this PDF, we calculate the BER penalty resulting from the crosstalk. The rms value CIJ, $J_{\sigma,CIJ}$, is determined from the PDF in (6.18). The rms value is useful for determining the timing margins that will achieve a particular BER.

$$J_{\sigma,\,CIJ} = \frac{\tau_f}{\sqrt{2}} \tag{6.19}$$

Additionally, the peak-to-peak jitter, $J_{pp,CIJ}$, is calculated from the bounds of this discrete PDF. The peak-to-peak jitter gives the total range over which transitions occur. Note that the rms jitter is always a subset of the peak-to-peak jitter.

$$J_{pp,\,CIJ} = 2\tau_f \tag{6.20}$$

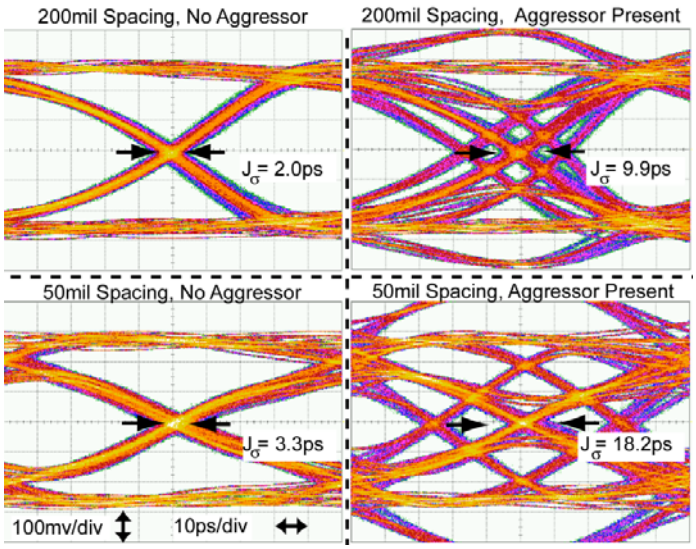


Figure 6.7 2-PAM data eyes at 10Gb/s shown with and without the aggressor.

In Figure 6.7 a 10Gb/s data eye is demonstrated for two line separations. These eyes illustrate the three distinct peaks and increased separation between the peaks for narrow separations. The jitter statistics are calculated for each of the line separations. Each data eye is recorded with and without the effect of the aggressor to normalize for other sources of jitter. This correction for the rms and pp jitter is

$$\begin{aligned} J_{\sigma,\,CIJ} &= \sqrt{J^2_{\sigma,\,meas,\,agg} - J^2_{\sigma,\,meas,\,no\ agg}} \\ J_{pp,\,CIJ} &= J_{pp,\,meas,\,agg} - J_{pp,\,meas,\,no\ agg} \end{aligned} . \tag{6.21}$$

Statistics are recorded from a histogram recorded with the Agilent 81600B wide bandwidth oscilloscope. The rms jitter is recorded from the histogram, and we use (6.8) to calculate the forward coupling time constant and compare it with the results in Figure 6.5. The statistics are presented in Table 6.1 for all four line separations. $J_{\sigma,CIJ}$ increases with decreasing line separation. Additionally, the time constants associated with the rms and pp jitter are similar and provide reasonable agreement with the results of Figure 6.5.

Table 6.1: Crosstalk-Induced Jitter in 2-PAM.

Line Separation	400mil	200mil	100mil	50mil
J_σ, No Aggressor	2.5ps	2.0ps	2.3ps	3.3ps
J_σ, Aggressor	5.4ps	9.9ps	14.5ps	18.2ps
$J_{\sigma,CIJ}$	2.7ps	9.7ps	14.3ps	17.9ps
Extracted τ_f	6.6ps	13.7ps	20.2ps	25.3ps

6.4.2 4-PAM

When equally probable quaternary signaling is employed (a_n={0,1,2,3}), the analysis of jitter is more sophisticated. Examining the ratio in (6.17), we anticipate that the CIJ in 4-PAM results in fifteen different threshold crossing deviations, significantly more than the three calculated for 2-PAM.

Furthermore, the larger signal swings imply that stronger aggressive signals can couple into weaker victim transitions. Additionally, if the symbols are equally probable, the transition density of 4-PAM is 75%, which is higher than the transition density for 2-PAM. The multiple transitions make 4-PAM CIJ more problematic.

Relating measurements of the jitter in 4-PAM to the BER is not straightforward. Because of the multiple thresholds required to detect a four level signal, there are many transitions in the 4-PAM data eye. The peak-to-peak jitter depends on the effect of other deterministic jitter sources. Additionally, 4-PAM suffers from an inherent data-dependent jitter that results from the required three threshold voltages and the finite rise time of the transitions. The jitter due to data-dependent jitter must be removed to calculate the appropriate jitter statistic. For detecting any one symbol, only a subset of these transitions is important.

In particular, we use a definition for the jitter that is straightforward from a measurement perspective. Locating the histogram around the center of the middle transition captures many, but not all of the transitions that occur. A PDF describing the CIJ can be constructed for analyzing the jitter statistics for a histogram located at the middle transition crossing (i.e. 0*V*).

$$\begin{aligned} PDF_{CIJ}(t_c) = {} & \frac{1}{64}\delta(t_c + 3\tau_f) + \frac{1}{32}\delta(t_c + 2\tau_f) + \frac{1}{32}\delta\left(t_c + \frac{3\tau_f}{2}\right) + \frac{1}{8}\delta(t_c + \tau_f) \\ & + \frac{1}{32}\delta\left(t_c + \frac{2\tau_f}{3}\right) + \frac{3}{32}\delta\left(t_c + \frac{\tau_f}{2}\right) + \frac{3}{64}\delta\left(t_c + \frac{\tau_f}{3}\right) + \frac{1}{4}\delta(t_c) \\ & + \frac{3}{64}\delta\left(t_c - \frac{\tau_f}{3}\right) + \frac{3}{32}\delta\left(t_c - \frac{\tau_f}{2}\right) + \frac{1}{32}\delta\left(t_c - \frac{2\tau_f}{3}\right) + \frac{1}{8}\delta(t_c - \tau_f) \\ & + \frac{1}{32}\delta\left(t_c - \frac{3\tau_f}{2}\right) + \frac{1}{32}\delta(t_c - 2\tau_f) + \frac{1}{64}\delta(t_c - 3\tau_f) \end{aligned} \tag{6.22}$$

In the absence of noise, expressions for the rms and peak-to-peak jitter for CIJ can be calculated as for 2-PAM. The standard deviation of the CIJ for 4-PAM, $J_{\sigma,4PAM}$, is determined from the PDF in (6.22).

$$J_{\sigma,\,CIJ} = \tau_f\sqrt{\frac{145}{144}} \approx \tau_f \tag{6.23}$$

A direct comparison with the CIJ calculated for 2-PAM demonstrates that the standard deviation of jitter for 4-PAM is 40% greater than for 2-PAM. The effect of crosstalk is demonstrated in Figure 6.8 and shows the ambiguity introduced into the timing deviations of the data eye due to the aggressive signal. The results for each of the four line separations is shown in Table 6.2. Again, the measurements are used to calculate the forward coupling time constant from (6.8). The rms jitter, however, does not agree as closely for close line separations due to the contribution of DDJ.

Table 6.2: Crosstalk-Induced Jitter in 4-PAM.

Line Separation	**400mil**	**200mil**	**100mil**	**50mil**
J_σ, No Aggressor	16.4ps	19ps	22.4ps	22.9ps
J_σ, Aggressor	17.6ps	23ps	27.7ps	29.5ps
$J_{\sigma,CIJ}$	6.4ps	12.9ps	16.3ps	18.5ps
Extracted τ_f	6.4ps	12.9ps	16.3ps	18.5ps

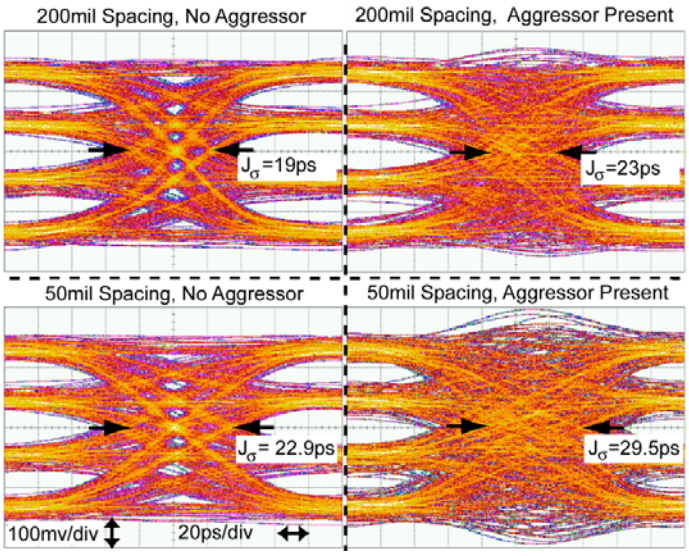


Figure 6.8 4-PAM data eyes at 10Gb/s shown with and without the aggressor.

6.5 Summary

This chapter discusses the effect of electromagnetic coupling in high-speed serial communications on transition timing. The transition timing deviation is demonstrated to depend on the electromagnetic mode between neighboring channels. The CIJ is distinguished from FEXT by an insensitivity to rise time and voltage swing. The coupling is determined from a forward time constant that is related to the mutual capacitance and inductance of the line. The crosstalk-induced jitter analysis demonstrates that three modes occur, and we introduce a PDF model for CIJ. The analysis and modeling is demonstrated for both 2-PAM and 4-PAM communication schemes and compared with experimental evidence through measured data eyes and the statistics of the peak-to-peak and rms jitter. Comparing 2-PAM and 4-PAM indicates that the impact of CIJ is aggravated in 4-PAM by the coupling between a strong aggressor and a weak victim. Consequently, the rms jitter in 4-PAM is twice as strong as in 2-PAM.

Chapter 7 Crosstalk-Induced Jitter Equalization

7.1 Introduction

To combat high-frequency attenuation, amplitude equalization is introduced in the transmitter (pre-emphasis) or receiver (post-emphasis) [29][117]. Pre-emphasis compensates high-frequency attenuation prior to the addition of noise over the interconnect. Recent work has addressed crosstalk amplitude equalization issues between neighboring serial links [28][119]. However, no effort to date has been made to equalize the timing jitter resulting from crosstalk.

To minimize the BER in the serial link, we want to avoid the timing ambiguity introduced by CIJ. In Chapter 6 we developed an analysis of crosstalk-induced jitter and probability density function (PDF) for the threshold crossing time deviation. The separation of discrete peaks is related to the strength of the coupling between the two lines and the signaling scheme.

Reducing DJ is important to designing robust links with low BER. We propose general equalizer implementations for minimizing the impact of CIJ. In Section 7.2 we discuss the general form of a CIJ equalizer for 2-PAM and 4-PAM modulations. The CIJ equalizer determines the electromagnetic modes of transitions and adjusts the delay of each transition. These equalizers rely on dynamic adjustment of the transition time of the data signal and not amplitude emphasis. A CMOS implementation of a 2-PAM circuit is discussed in Section 7.3. The results are discussed in Section 7.4 at 5Gb/s and 10Gb/s in different crosstalk environments.

7.2 M-PAM Crosstalk-Induced Jitter Equalization

7.2.1 2-PAM

A general analog scheme for a CIJ equalizer for 2-PAM is shown in Figure 7.1. A symbol period time delay, *T*, is used to capture the data values before and after the transition. The summing device computes the difference between these data values to produce a three level signal corresponding to whether the current transition is a rising or falling edge. This result is multiplied by the result of the neighboring line to resolve the transition mode. The resulting tri-state signal indicates the electromagnetic mode of the transitions. For example, if both the victim and aggressor data lines have a rising (or falling) edge, the multiplication results in one, indicating the even mode. The tri-state value associated with the detection of this mode is weighted by an appropriate crosstalk equalization coefficient, which adjusts the time delay of the transition. This shifts timing deviations that occur in (6.17) to a consistent transition edge. Notably, this adjustment can be implemented in either the transmitter as a pre-emphasis technique or the receiver before detection of the signal value.

The algorithm demonstrated in Figure 7.1 exactly compensates the effect of CIJ. The compensation introduces a time delay, t_{comp}, to both channels equal to

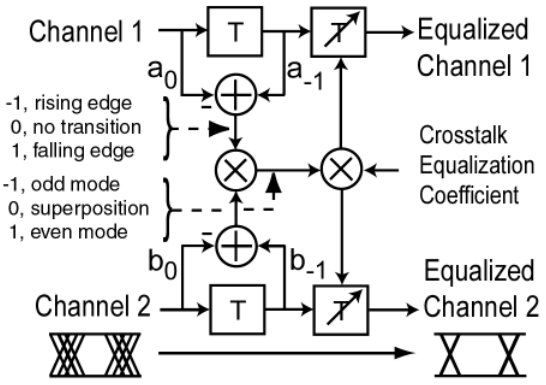


Figure 7.1 Schematic of a two-channel crosstalk-induced jitter equalization. The circuit detects the difference in the data on adjacent channels to determine the electromagnetic mode.

$$t_{comp} = \tau_f (b_0 - b_{-1})(a_0 - a_{-1}). \tag{7.1}$$

When this is added to the deviation occurring due to the CIJ, we have a total timing deviation of

$$t_{c,\,CIJ} + t_{comp} = \tau_f \cdot (b_0 - b_{-1})\left[- \frac{1}{(a_0 - a_{-1})} + (a_0 - a_{-1}) \right]. \tag{7.2}$$

Therefore, this CIJ equalizer operates correctly as long as $|a_0 - a_{-1}| = 1$, and this scheme will not function properly for 4-PAM schemes. The advantage of the proposed circuit in Figure 7.1 is its ease of adaptation to high-speed mixed signal implementation. Additionally, the circuit in Figure 7.1 can be extended to multiple neighbors with a straightforward adaptation of the demonstrated algorithm. The compensation calculated between additional neighbors is changed by a different forward coupling time constant calculated from (6.7). Expanding this scheme will come at the cost of additional circuit and wiring complexity to route the mode detection signal between other neighboring links.

7.2.2 4-PAM

A hypothetical CIJ equalizer for 4-PAM is suggested in Figure 7.2. In this schematic we have used a division element to compute the voltage ratio in (6.17). Two calculations are required because the compensation is different for each channel. In particular, the

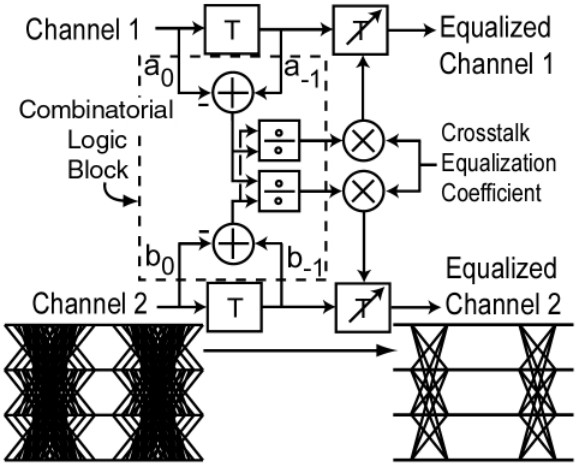


Figure 7.2 Schematic of a two-channel 4PAM crosstalk-induced jitter equalization.

channels are reciprocally related and, therefore, the computational symmetry of CIJ in 2-PAM does not hold. This proposed CIJ equalizer for 4-PAM compensates all the possible crosstalk-induced timing deviations.

In principle, this equalizer circuit could be implemented in high-speed links. However, the challenge is to maintain low complexity and, consequently, low power consumption. One approach is not to attempt to compensate all of the fifteen threshold crossing time deviations, as the schematic does, but to reduce the problem to compensating only critical deviations. For instance, the victim signal is most severely impacted when the data transition is small ($|a_0 - a_{-1}| = 1$) and the aggressor signal swing is large ($|b_0 - b_{-1}| = 2,3$). Compensating these conditions would correct for the largest timing deviations, $2\tau_f$ and $3\tau_f$. Notably, analog implementations of FIR filters have been the best solutions for 4-PAM crosstalk cancellation [28]-[119].

7.3 Circuit Implementation

The circuit is implemented with 130nm MOSFETs using the IBM 8HP process. A chip microphotograph is provided in Figure 7.3 and includes the CIJ equalizer as well an on-chip coupled wire section for testing the circuit operation. These are described in more

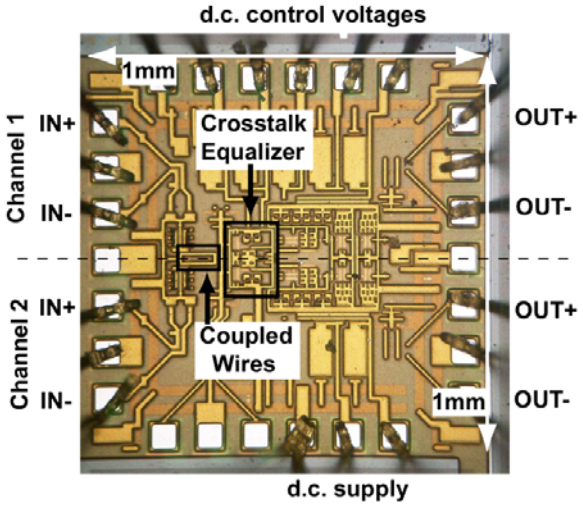


Figure 7.3 Chip microphotograph of the crosstalk-induced jitter equalizer.

detail in the results section. The circuit implementation focuses on compensating CIJ between 2 channels using 2-PAM. It consists of high-speed current-mode logic (CML) exclusive-or (XOR) and AND gates to detect transitions and compare the symmetry at 10Gb/s as illustrated in Figure 7.4. While analog implementations of the circuits in Figure 7.1 are possible, this logic gate approach is more robust to process variations and is sufficient for a proof-of-concept of the jitter equalizer.

The logic gates generate logical values when the even or odd modes occur and are multiplied by a coefficient to adjust a variable time delay. An XOR detects a transition on each line. The results of the neighboring line are ANDed to determine whether either the even or odd mode has occurred. An XOR between each line determines which mode is present. Since the timing adjustment in this case is feed-forward, the delay of the logic gates can be compensated by adding delay in the data paths.

The multiplexer combines the results of the even and odd transition detection to adjust the time delay. The multiplexer circuit diagram and operation are illustrated in Figure 7.5. Three output voltages are generated that depend on the differential control of the select input. When either the even or odd modes occur, the output is driven between + or

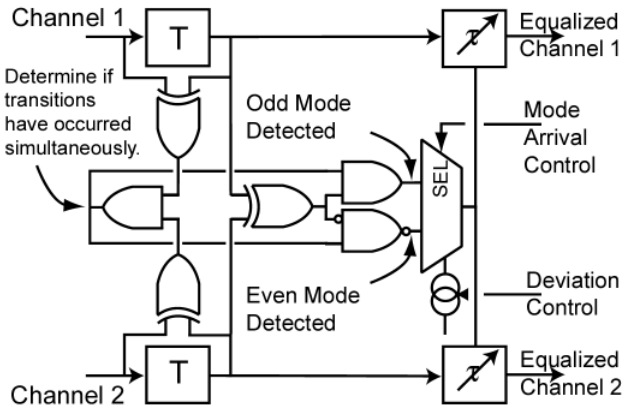


Figure 7.4 Implemented version of two-channel CIJ equalizer.

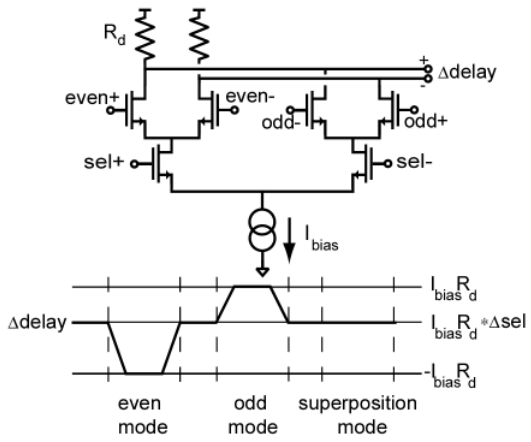


Figure 7.5 Schematic and operation of the mode multiplexer.

$-I_{bias}R_d$, respectively. Consequently, control over the total range of arrival times for the odd and even mode can be controlled with I_{bias}.

While the arrival time of the superposition mode is ideally between the even and odd modes, the discussion of the timing offsets and illustration in Figure 6.6 of the relative timing of the odd, superposition, and even modes implies that control over the superposition delay is also useful. Additionally, the non-linear delay variation described in the following paragraphs suggests that independent control of the superposition mode delay is essential. Consequently, the *select* input controls the relative position of the superposition timing. Note that if the differential *select* voltage is zero, the voltages corresponding to the odd and even modes are equally spaced.

The time delay element consists of a simple cross-coupled differential pair through which current can be starved. The schematic for the delay stage is shown in Figure 7.6. The cross-coupled differential pair can be analyzed as a negative resistance loading the output drain resistance [120]. The advantage of the cross-coupled delay stage is the constant large-signal swing while providing variation of the small-signal characteristics. Additionally, the time delays are tuned for the appropriate tap delay and bit rate.

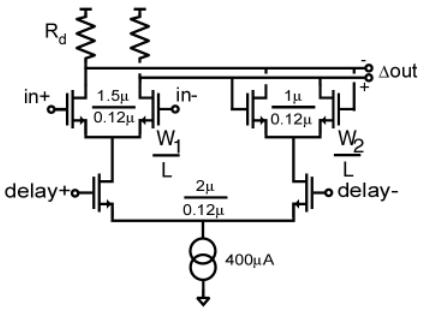


Figure 7.6 Schematic of the delay cell. The sizing of the two differential pairs controls the relative delay variation that can be achieved.

A first-order analysis demonstrates the delay variation possible in the delay cell. The equivalent circuit for this cell places a negative resistance that depends on the current steered through cross-coupled pair in parallel with R_d. Consequently, the first-order transfer function for this stage is

$$A_v(s) = \frac{g_{m1}R'_d}{1-g_{m2}R'_d} \cdot \frac{1}{1+s\dfrac{R'_dC_d}{1-g_{m2}R'_d}}, \tag{7.3}$$

where $R'_d = R_d \| r_{o1} \| r_{o2}$. This implies that the delay of the stage is found from the time constant associated with the pole [121].

$$\tau_d = \frac{R'_dC_d}{1-g_{m2}R'_d} \tag{7.4}$$

This variation has been plotted against the actual transient simulation in Figure 7.7. This plot also demonstrates the proper sizing of the cross-coupled differential pair with respect to the differential pair. In particular, the desired delay variation is chosen from the amount of crosstalk-induced jitter that should be compensated. Consequently, the size of W_2 is chosen as a ratio to W_1. The obvious trade-off for delay variation from the analysis in (7.3) is the bandwidth for the high-speed signal. It is clear that the circuit provides for at most 30ps of delay variation. Consequently, the CIJ equalizer can compensate τ_f of 15ps.

The important characteristic of the delay variation in Figure 7.7 is that it is non-linear. If the application only required between two delay values, the non-linearity of the delay

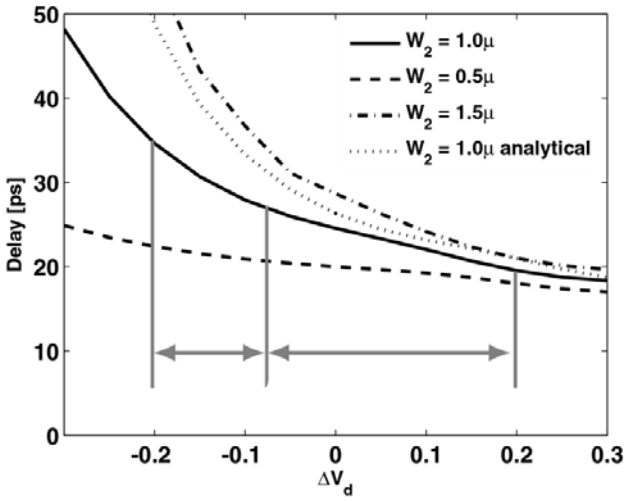


Figure 7.7 Transient and analytic delay variation.

variation would not be an important design consideration. However, for this equalizer, three specific delays need to be selected. Consequently, if we desire equally spaced variation as described by the PDF in (6.18), the voltage swing must be unequal. Therefore, the variable control over the superposition time delay in Figure 7.5 improves the operation. Other delay elements offer more tuning linearity and might be considered alternatively, but achieving high linearity over a wide range is difficult [13].

The entire two channel circuit consumes 330mA from a 2V supply. The supply was higher than specified for this fabrication technology because the MOS models were slightly slow. The chip area measures 1mm x 1mm. The actual area of the CIJ equalizer is 140μm x 100μm. From simulation, the crosstalk equalizer consumes 40mA. The remaining current consumption supports the output buffering.

7.4 Results

Two measurements are presented to show the performance improvement of the CIJ equalizer. The first measurement shows a decrease in the rms and peak-to-peak jitter in the

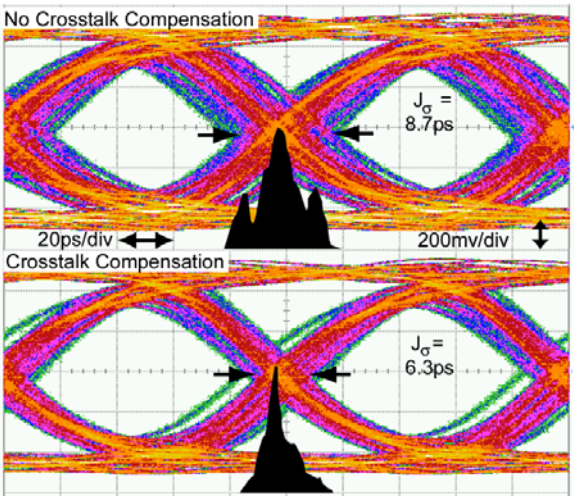


Figure 7.8 Data eyes at 10Gb/s before and after equalization.

data eye. The second measurement is the improvement in the timing margins that achieves at 10^{-12} BER.

The chip is wirebonded to a Rogers 5880 duroid test board on a brass mount. To generate uncorrelated data sequences at 5-10 Gb/s, differential outputs of an Anritsu MP1763C pulse pattern generator (PPG) are delayed with respect to one another by 10 bits. The pseudo-random bit sequences generated by the MP1763C are maximal length sequence, which has low (~zero) autocorrelation after one bit [47].

For this work the delay value is adjusted manually to reduce the CIJ. It is possible to include adaptation by using a time-to-voltage conversion that samples the timing deviations for particular bit sequences between the neighboring lines.

For 10Gb/s testing, the two data paths are coupled through 40μm-long on-chip transmission lines spaced 400nm apart. The coupling capacitance for these lines is 3.34fF, and the coupling is dominated by the mutual capacitance since the two lines are not terminated by the line impedance but instead by the drain resistance. Consequently, the capacitive term in (6.8) dominates the coupling. These transmission lines are driven with a 400μA buffer and terminated with 4kΩ. The predicted forward crosstalk coupling time constant is calculated as 6.7ps. However, the transient simulations indicate that τ_f is 6ps.

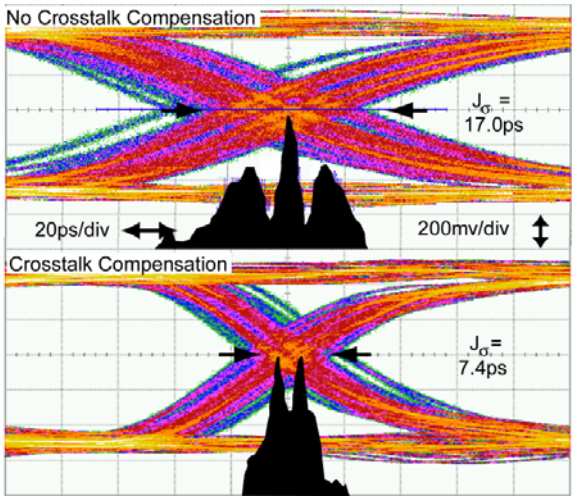


Figure 7.9 Data eyes at 5Gb/s before and after equalization.

The first measurement collects jitter statistics around the center of the data eye where the jitter is lowest. The rms jitter and peak-to-peak jitter are measured with and without CIJ equalization. The compensation voltage is tuned to provide the minimum jitter. In Figure 7.8, the data eye demonstrates that J_σ reduces from 8.7ps to 6.3ps at 10Gb/s. J_{pp} reduces from 48.9ps to 34.2ps. Using (6.21), the rms value indicates that the circuit reduced the rms jitter contribution CIJ by 6ps. The peak-to-peak value indicates that the circuit reduced the peak-to-peak contribution of CIJ by 14.7ps. From (6.19) and (6.20), this implies the τ_f is 7.4 and 8.5ps, respectively. These values are only slightly higher than the τ_f expected from simulation.

For testing at 5Gb/s, the two data sequences are coupled through a series combination of the on-chip transmission lines and coupled microstrip lines fabricated on Rogers 5880 duroid described in Section 6.2. A 100mil line spacing is used for the coupled lines. From Table 6.1, $J_{\sigma,CIJ}$ is 14.3ps at the input of the receiver. This contribution overwhelms the impact of the on-chip transmission lines. In Figure 7.9 the data eye demonstrates that J_σ reduces from 17ps to 7.4ps at 5Gb/s. Using (6.21), the rms value indicates that the circuit reduced the rms jitter contribution CIJ by 15.3ps. The peak-to-peak value indicates that the circuit reduced the peak-to-peak contribution of CIJ by 44.7ps. This implies the τ_f is

21.6ps and 22.3ps, respectively. Since the designed delay variation was nominally limited to 15ps, this indicates that the delay variation has increased due to the process. A summary of the jitter statistics at 5 and 10Gb/s is also shown in Table 7.1.

Table 7.1: Improvement of Crosstalk-Induced Jitter at 5 and 10Gb/s.

Rate, Equalization	10Gb/s, Before	10Gb/s, After	5Gb/s, Before	5Gb/s, After
J_σ	8.7ps	6.3ps	17ps	7.4ps
$J_{pp,CIJ}$	48.9ps	34.2ps	86ps	41.3ps
10^{-12} BER	17	45ps	102ps	143ps

The second measurement sketches the bathtub curve for the eye opening with the Anritsu MP1764C error detector. The BER is recorded at each particular sampling time to form a curve. The notable improvement of J_σ and J_{pp} is reflected by the larger eye opening in Figure 7.10 and Figure 7.11 after compensation. A summary of these results at 5 and 10Gb/s is also shown in Table 7.1. To define a figure for performance of the equalizer, we quote the BER at 10^{-12} for the purposes of determining the eye opening. The BER curve measured before compensation shows an opening of 17ps at BER of 10^{-12} and 45ps after

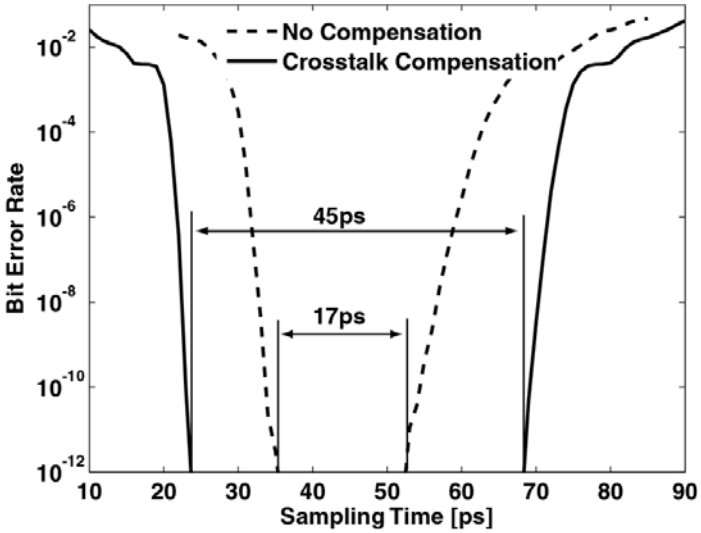


Figure 7.10 Bathtub curve resulting before and after equalization at 10Gb/s.

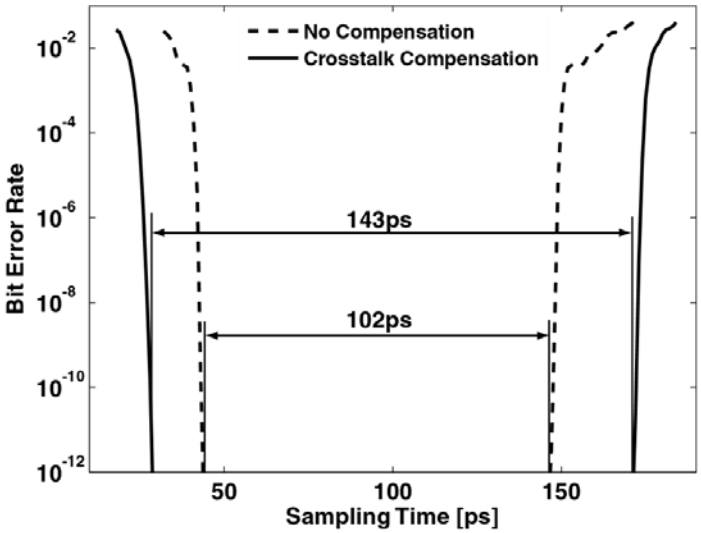


Figure 7.11 Bathtub curve resulting before and after equalization at 5Gb/s.

compensation at 10Gb/s. At 5Gb/s, the eye opening increases from 102ps to 143ps. This indicates the substantial eye improvement possible due to the CIJ equalizer.

7.5 Summary

This chapter discusses the equalization of crosstalk on timing jitter in high-speed serial communications. Using the analysis of crosstalk-induced jitter derived in the previous chapter, we propose a new scheme to eliminate the timing deviations. This equalizer compares the transition symmetry between neighboring lines. Implementations are discussed for 2-PAM and 4-PAM. An equalizer for 2-PAM is designed that uses standard logic to perform the mode calculation. The circuit is fabricated in 130nm MOSFET technology and operates between 5 and 10Gb/s. Reduction in the rms and peak-to-peak jitter is demonstrated in the data eye. Bathtub curve measurements verify enhanced timing margins. At 5Gb/s the timing margins are improved by 41ps with the use of the crosstalk equalizer, while at 10Gb/s the margins increase by 28ps.

Chapter 8 Subharmonic Coupled Oscillators Arrays

8.1 Introduction

Unlicensed operation at the 59-65GHz band is stimulating unique radio architectures for millimeter wave integrated circuits. The available bandwidth offers data rates at gigabits/second, and high absorption at 60GHz is an important feature for dense networking. Transceiver circuits that operate at millimeter wave frequencies were demonstrated with SiGe [126]-[128]. However, the integration of a complete phased array transceiver with antennas on a single chip offers new design choices and opportunities. Phased array designs at the 24GHz ISM band have demonstrated new receiver circuit architectures [129]-[131]. This paper demonstrates a coupled oscillator array for a millimeter wave silicon integrated transmitter.

Coupled oscillators are well suited for fully integrated phased array circuits. First, the small wavelength at 60GHz allows fully integrated arrays on a single die. Scalable architectures are particularly appropriate for creating larger arrays by tiling several dies. In Figure 8.1, scalability is demonstrated for a phased array transmitter. The phased array requires phase coherence between all elements. Since each chip requires frequency generation, neighboring chips are locked to ensure phase coherence. If oscillators are located at each antenna element, injection locking can lock the oscillators both on-chip and between chips. This tiling approach is useful not only for phased arrays but for MIMO applications where the separation between antennas might be set after the development of a single radio cell.

Furthermore, injection locked coupled oscillators offer a new approach to the distribution of the carrier frequency between different elements. Previous integrated

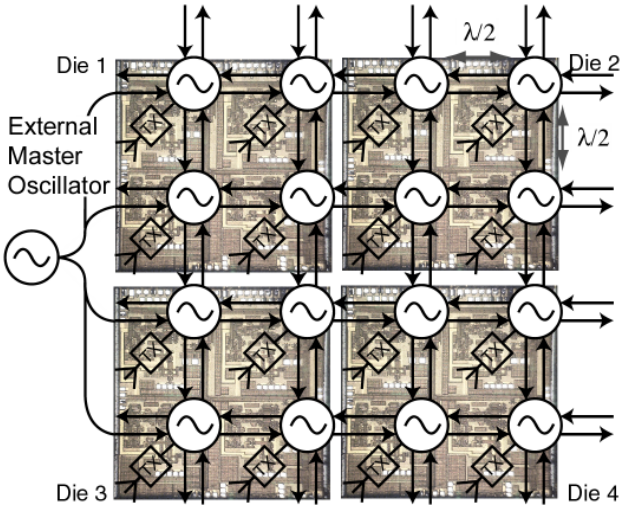


Figure 8.1 Coupled oscillator approach for fully integrated phased-array transmitter. Each oscillator drives a transmit chain with a DAC controlled phase shifter, power amplifier, and antenna.

phased arrays provide sixteen phases across the entire chip, resulting in an excessive amount of wiring and power consumption [129]. Global frequency distribution becomes increasingly difficult at millimeter frequencies.

In this transmitter implementation a 2x2 array of transmitter cells is integrated on a single chip with antennas.[1] The design of the coupled oscillator network is motivated by demonstrating array scalability as well as avoiding the on-chip coupling that occurs with power-amplifiers and antennas. The measured results show that the phase noise of each element can be suppressed when locked to an external array across a single chip as well as across two chips.

1. In collaboration with Aydin Babakhani, who was responsible for the power amplifier and antenna design, and Abbas Komijani, who was responsible for the phase shifter design.

8.2 Coupled Oscillators

Adler described the unilateral locking phenomena in coupled oscillators [132], and Kurokawa later studied the microwave dynamics [133]. The phase relationship between neighboring oscillators is

$$\Delta\phi = \sin^{-1}\left(\frac{2Q}{\omega_o}\frac{I_{osc}}{I_{inj}}\Delta\omega\right), \tag{8.1}$$

where $\Delta\phi = \phi_o - \phi_{inj}$ and $\Delta\omega = \omega_o - \omega_{inj}$ are the phase difference and frequency detuning between the two oscillators, ω_o is the carrier frequency, Q is the quality factor for the oscillator, and I_{osc} and I_{inj} are the oscillator and injection current. The locking range is defined as twice $\Delta\omega_m = \omega_o I_{inj}/2QI_{osc}$ and allows the phase difference to vary from -90 to 90 degrees. The frequency detuning relationship is demonstrated in Figure 8.2. Increasing the locking range is possible with increasing I_{inj} or decreasing Q or I_{osc}, which strongly affect the oscillator phase noise. Therefore, we tend to concentrate on controlling the injected current.

Bilateral oscillator arrays were first proposed by Stephan [134]. York et al. proposed coupled oscillators for electronic beam steering through injection at the periphery of the

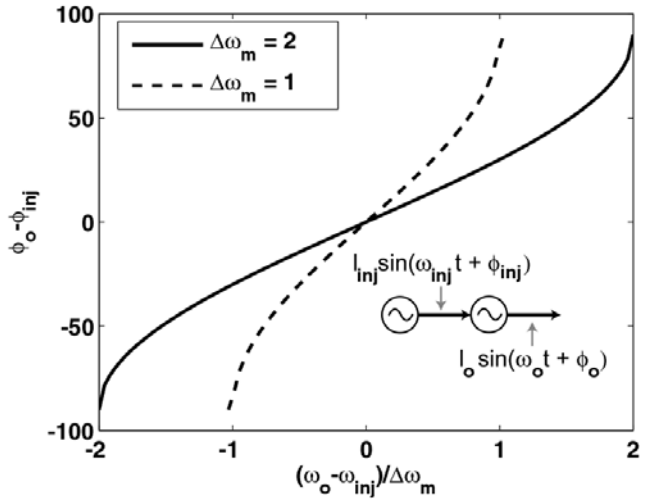


Figure 8.2 Unilateral injection scheme and relationship between frequency and phase detuning.

array [135]-[137]. The effect of bilateral injection locking is to modify the behavior in (8.2). In this case, the phase dynamics of the array would produce a linear phase gradient across the array. In [137] the dynamics for a coupled oscillator array with bilateral injection locking and external injection locking for beam steering are described:

$$\frac{d\phi_i}{dt} = \Delta\omega_i - \frac{\omega_i}{2Q}\frac{I_{osc}}{I_{inj}}(\sin(\Delta\phi_i) - \sin(\Delta\phi_{i-1})) + \frac{\omega_i}{2Q}\frac{I_{osc}}{I_{ext}}\sin(\phi_{ext} - \phi_i), \qquad (8.2)$$

where $\Delta\omega_i$ is the detuning at the *i*th oscillator, $\Delta\phi_i = \phi_i - \phi_{i+1}$ is the phase difference between neighboring oscillators, and I_{ext} and ϕ_{ext} are the external injection current and phase, respectively. The continuum dynamics for beam-steering have been studied by Pogorzelski et al. [138], and experimental results have recently demonstrated the array pattern for oscillator arrays of discrete components [139].

The on-chip process and voltage variations between different oscillators introduce phase errors between neighboring elements. Other characteristics of coupled-oscillator arrays are worth consideration. First, the phase noise increases as the phase difference between neighboring oscillators is detuned [140]. The phase noise additionally limits the bounds on the phase detuning that can be achieved in Figure 8.2. As the edges of the locking range are approached, the oscillators can lose lock. Second, analysis of coupled oscillator dynamics demonstrates the possibility for unwanted modes in the phase dynamics [141][142].

Instead of exploiting the phase relationship in (8.2) to control the beam angle, this work instead relies on injection locking primarily as a means to distribute and phase lock the carrier signal across a single chip or between neighboring chips. The locking range consequently must be large enough to satisfy the process, voltage, and temperature variations in a particular technology. Slight supply variations shift the natural frequencies of neighboring oscillators as will be demonstrated in the results section. Digital control of the array beam steering is provided for practical data modulation, and DAC controlled phase shifters are included in this design.

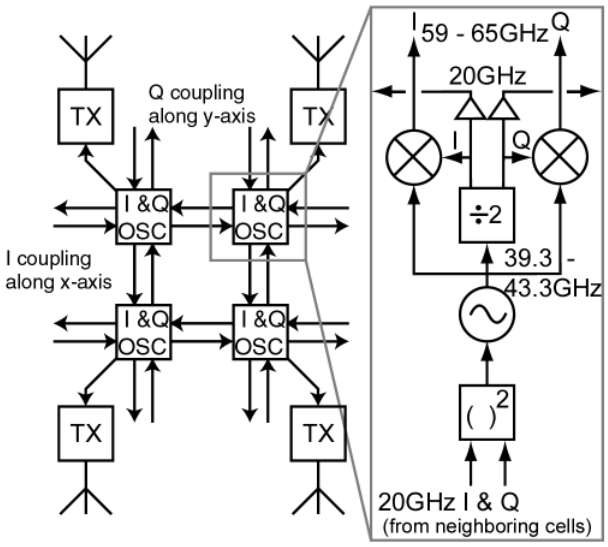


Figure 8.3 Implemented coupled oscillator topology. The oscillators are coupled along two dimensions. The coupling network operates at one-third the carrier frequency.

8.3 Scalable 2D Oscillator Array

The basic coupled oscillator topology is shown in Figure 8.3. The 2x2 phased array contains four oscillators at each transmit (TX) stage. The block diagram demonstrates the implementation of the oscillator cell. Each oscillator is designed to operate at 40GHz. Isolating the oscillator from the power amplifier and antenna is critical because on-chip coupling is difficult to accurately model and can greatly impact performance. By shifting the oscillator frequency to 40 GHz, the unwanted coupling is reduced. The oscillator is divided to 20GHz and mixed with the 40GHz signal to achieve the 60GHz in-phase (I) and quadrature (Q) signals. This frequency planning motivates many of our other design choices.

8.3.1 Interconnections

Coupling between chips requires considering an interconnect. If wirebonds are used to provide the interconnect, frequencies above 20GHz incur high losses. Tiling chips can

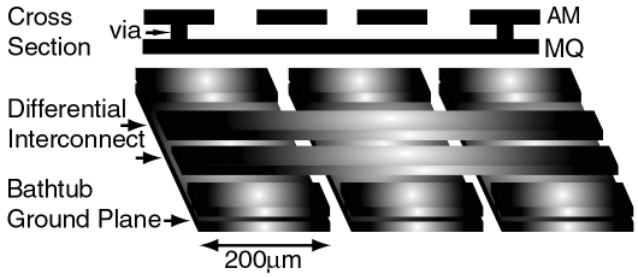


Figure 8.4 Interconnect structure with severed bathtub to prevent coupling to integrated antenna.

keep the inter-chip spacing small (<200μm). Consequently, we choose to injection lock at a subharmonic. The first subharmonic at 20GHz is available from the carrier generation scheme described in the previous paragraph. Since the static dividers provide I and Q signals, we propose an I/Q scheme for coupling within a 2-D array of oscillators. In Figure 8.3 the 20GHz I signal is coupled in the East-West direction, while the Q signal is coupled along the North-South direction.

Coupled oscillators can simplify the distribution of high-frequency carrier energy over a phased array. However, electromagnetic simulations indicate the on-chip antenna will radiate substantially within the silicon substrate and silicon dioxide metal stack. Clearly, the presence of a global transmission line interconnect grid will absorb much of this radiated energy. The transmission line structure for the injection interconnections was modified to reduce the impact on the radiated energy. The transmission line scheme is shown in Figure 8.4. The transmission line ground plane is a bathtub which shields the differential interconnects from the substrate similar to the transmission lines discussed in [143]. The bathtub ground plane, however, is severed every 200μm to mitigate the absorption of millimeter wave energy. The signal travelling in the differential line is relatively unaffected by the severed ground plane since the return currents in this structure are relatively localized. IE3D simulations indicate that the characteristic impedance of the lines changes by less than 5%. A segmented transmission line test structure was designed to compare the s-parameters with a regular bathtub transmission line. The measured

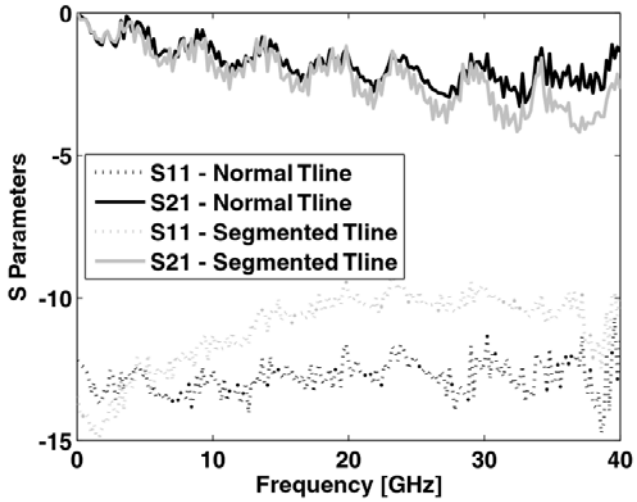


Figure 8.5 Measured interconnect S-parameters over 1mm of interconnect.

s-parameters in Figure 8.5 demonstrates that the loss of the segmented transmission line and the loss over 1mm is around 3dB. However, the measured return loss is increased by 3dB.

8.3.2 Frequency Doubler

Since the injected signal is a subharmonic, the injected frequency must be doubled at the oscillator. Injection locking with quadrature subharmonic signals increases the 2nd harmonic power since $[\sin(\omega t)+\cos(\omega t)]^2 = 1 + \sin(2\omega t)$. A circuit schematic for the frequency doubler and oscillator is shown in Figure 8.6. The I/Q signals are picked up by a receiver that drives a pair of differential bipolar devices. These transistors are biased below the forward active region to generate strong second harmonic content through rectification. Changing the bias voltage, V_{bi}, allows control over the injected current at the second harmonic. The basic collector current dependence on the base-emitter diode voltage is

$$I_c = I_s\left(e^{-V_{be}/V_T} - 1\right), \tag{8.3}$$

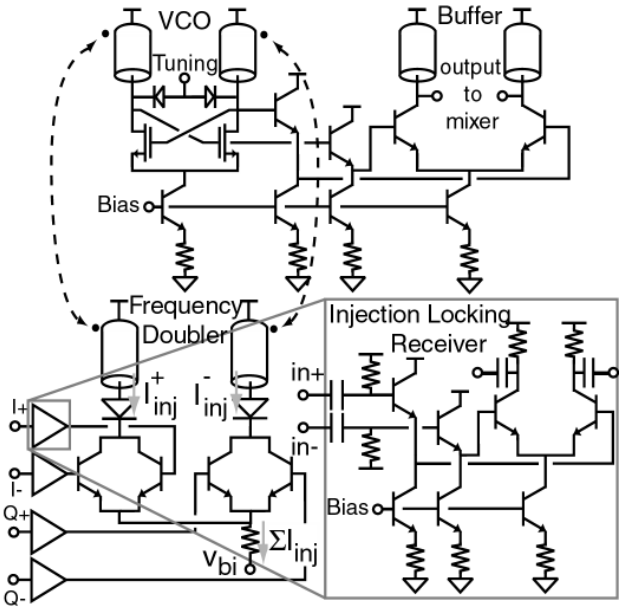


Figure 8.6 Schematic of the subharmonic injection locked VCO and buffer.

where I_s is the saturation current and V_T is the thermal voltage. If we assume that the bases are driven with a differential, ac-coupled injection signal, +/-V_{inj}sin($\omega_o t$), the sinusoidal dependence in the exponent is expressed through the series expansion

$$e^{-(\pm V_{inj}\sin(\omega_{inj}t))/V_T} \approx 1 \mp \frac{V_{inj}}{V_T}\sin(\omega_{inj}t) + \frac{V_{inj}^2}{2V_T^2}(\sin(\omega_{inj}t))^2 \ldots \tag{8.4}$$

Odd harmonic terms cancel when the differential current is added at the collector. Resistor degeneration at the emitter of the bipolar transistors provides common mode rejection. Emitter degeneration is introduced with the resistor, R_{inj}, in the emitter, and the base-emitter voltage changes to

$$V_{be} = V_{inj}\sin(\omega_{inj}t) - R_{inj}\Sigma I_{inj}, \tag{8.5}$$

where ΣI_{inj} is the common mode current. Recalculating (8.3), the differential collector current for the I and Q paths is

$$\begin{aligned} I_{inj}^{+} &= I_s\left(\left[2+\left(\frac{V_{inj}}{V_T}\sin(\omega_{inj}t)\right)^2\right]e^{\frac{R_{inj}\Sigma I_{inj}}{V_T}}-2\right) \\ I_{inj}^{-} &= I_s\left(\left[2+\left(\frac{V_{inj}}{V_T}\cos(\omega_{inj}t)\right)^2\right]e^{\frac{R_{inj}\Sigma I_{inj}}{V_T}}-2\right) \end{aligned} \quad . \tag{8.6}$$

Finally, the difference of the expressions in (8.6) gives the desired injected signal.

$$\Delta I_{inj} = I_{inj}^{+} - I_{inj}^{-} = -I_s\frac{V_{inj}^2}{V_T^2}\cos(2\omega_{inj}t)e^{\frac{R_{inj}\Sigma I_{inj}}{V_T}} \tag{8.7}$$

The injected current is twice the frequency of the I/Q signals and depends quadratically on the amplitude of the injected current. The total current through the emitter resistor is found from adding the currents in (8.6).

$$\Sigma I_{inj} = I_{inj}^{+} + I_{inj}^{-} = I_s\left(\left[4+\frac{V_{inj}^2}{V_T^2}\right]e^{\frac{R_{inj}\Sigma I_{inj}}{V_T}}-4\right) \tag{8.8}$$

The bias current is constant through the stage but depend on the input power as the differential current did in (8.7). For small current levels, this transcendental equation can be approximated with a series for the exponential dependence on ΣI_{inj}. In this case,

$$\Sigma I_{inj} \approx \frac{I_s(V_{inj}^2/V_T^2)}{1+\frac{I_s R_{inj}}{V_T}(4+V_{inj}^2/V_T^2)} \tag{8.9}$$

When the tail resistance is small, $I_{inj} \approx I_s V_{inj}^2/V$ and the total current depends on the power. For large power levels, the total current saturates as $I_{inj} \approx V_T/R_{ir}$. For a tail resistance of 20Ω, this current is roughly 1.3mA. Substituting (8.9) into (8.7), the differential mode current is

$$\Delta I_{inj} = -I_s \frac{V_{inj}^2}{V_T^2} \cos(2\omega_{inj} t) \left(\frac{1 + \frac{4 I_s R_{inj}}{V_T}}{1 + \frac{I_s R_{inj}}{V_T}(4 + V_{inj}^2 / V_T^2)} \right). \quad (8.10)$$

For large power levels, the total differential current saturates at $\Sigma I_{inj} \approx -\left(\frac{V_T}{R_{inj}} + 4 I_s \right) \cos(2\omega_{inj} t)$. This describes the current when no dc bias is provided across the base-emitter diode.

A simulation of the complete frequency doubling circuit is demonstrated in Figure 8.7. The simulation is performed as a function of the input subharmonic power. Different values of tail resistance are shown in the plot, and results are provided for energy at the subharmonic as well as at the carrier frequency. Larger resistance provides more rejection of the subharmonic frequency but limits the current injected into the tank. For this design, we chose 20Ω for the tail resistance as a trade-off between the desired injection current and the rejection of the subharmonic frequency. Additionally, varying V_{bi} at the tail resistance can provide a dc bias that puts the bipolar devices closer to the forward active region. This effect is plotted in Figure 8.7 for V_{bi}= -1.0V. Now, the injection current depends weakly on the input subharmonic power, and the injection current remains fixed

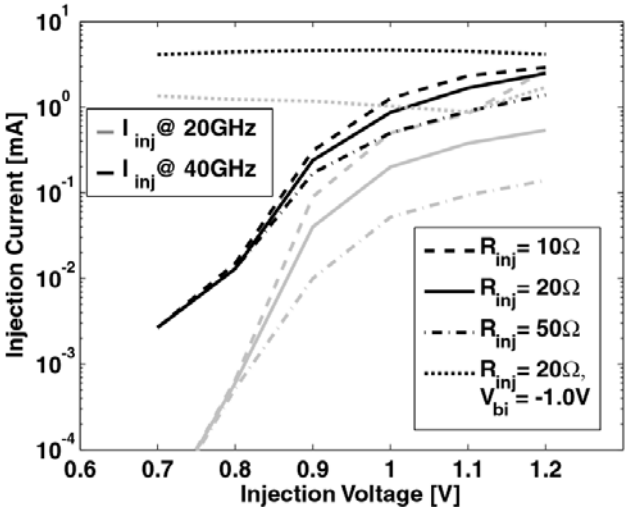


Figure 8.7 Current injected at oscillator frequency and subharmonic.

at around 4mA. However, the circuit also provides less rejection of the subharmonic energy.

8.3.3 Oscillator Injection Locking

Energy can be injected at many different points of the oscillator core. Injection locked frequency dividers inject energy in the tail of a cross-coupled differential pair [144]. However, the tail is useful primarily for superharmonic injection locking and rejects subharmonic energy. Alternatively, coupled oscillators have been proposed for quadrature generation [145]. These schemes use a differential pair connected in parallel to the cross-coupled pair in the oscillator core to inject energy. The sizing of these devices controls the coupling strength. This topology can be difficult to implement at submillimeter wave frequencies because the parasitic loading can reduce the tuning range. Other papers have shown direct injection locking for quadrature generation through a separate differential stage that drives a ring oscillator [146].

For this design the frequency doubler output is coupled into the VCO core with a coupled transmission line. The coupled transmission line is part of the VCO tank circuit and has less parasitic loading but limits the coupling strength. S-parameter simulations of

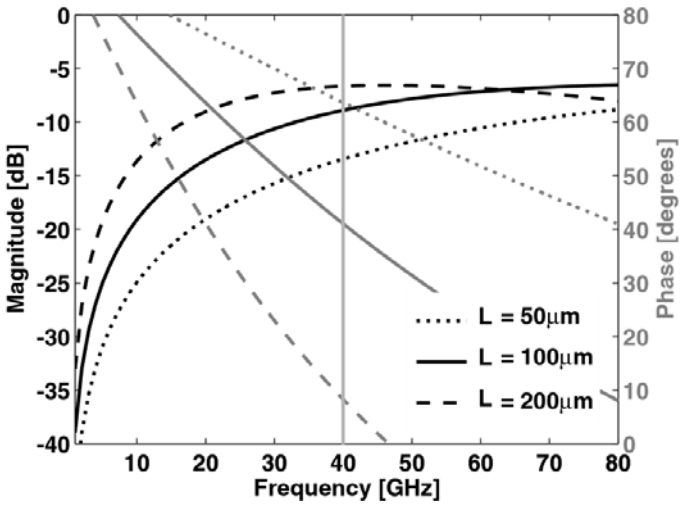


Figure 8.8 S-parameters for coupled transmission lines in VCO.

coupled transmission lines in this fabrication technology are shown in Figure 8.8. The simulations are swept for three different transmission line lengths. At 40GHz, the coupling between the injection locking circuit and the VCO depends on the coupling length. The 50μm lines show a -15dB coupling strength between the two circuits, while the 200μm lines provide -7dB coupling. Interestingly, the coupling reaches a maximum around this value and decreases at higher frequencies. In this case the total inductance of the transmission line tank of the VCO limited the coupled transmission line section to 100μm, providing -10dB coupling. Additionally, the coupling strength at 20GHz can provide some rejection. The coupled transmission lines can provide some rejection at this frequency, -15dB, for the 100μm length.

On the left side of the schematic in Figure 8.6, a simple cross-coupled NMOS VCO is shown. The oscillator tank consists of transmission lines for inductance, which limits the fields generated by the VCO. The tuning range of the VCO is over 4GHz, about 10% of the carrier frequency. Notably, the oscillator self-mixing enhances the tuning range at 60GHz.

8.4 Results

The coupled oscillator array was constructed in IBM 8HP, a 0.12μm SiGe process with bipolar and CMOS devices. The maximum f_T of the bipolar devices is 210GHz. The array is shown in Figure 8.9 and occupies an area of 3.5mm by 5mm. The wavelength of a 60GHz signal determines the spacing between on-chip antennas. In air, the array spacing ($\lambda/2$) is roughly 2.5mm. However, the illumination for the array is intended through the die substrate where a silicon lense is used to absorb the radiated energy [127]. Consequently, the array spacing is designed for $\varepsilon_r = 11.7$ and the array spacing is 0.7mm. Unfortunately, the element spacing is too constrictive given geometry considerations for the on-chip antenna. The array spacing was chosen for 1.7mm. This limits the beam-steering and causes undesirable sidelobes but is still useful for the proof-of-concept.

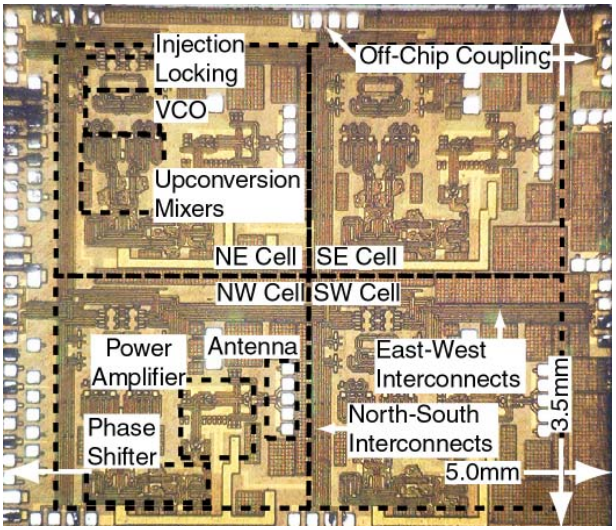


Figure 8.9 Chip microphotograph for complete 60GHz transmitter with coupled oscillator array.

The chip includes a DAC controlled phase shifter, power amplifier, and antenna located in each cell. Each oscillator consumes 25mA for the static frequency divider and 125mA for the oscillator, frequency doubler, and coupling buffers. This number is driven up by the use of the quadrature injection locking scheme since each oscillator drives four 50Ω buffers.

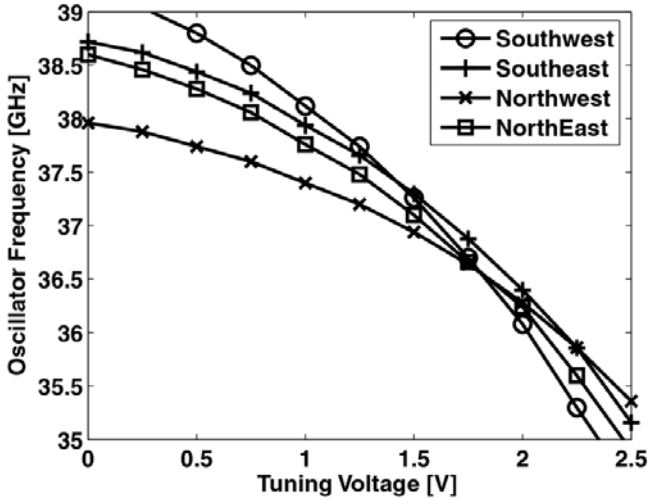


Figure 8.10 Tuning range for each oscillator in 2x2 array. The difference between the natural frequencies of each oscillator is greatest near the bottom of the tuning range.

The VCO frequency varies between 35.5 and 39.5GHz, falling 3.5GHz below the desired range of 39 to 43GHz. The tuning curve for each of the oscillators is shown in Figure 8.10. The variation in the oscillator tuning range varies with location. The southern oscillators have a higher natural frequency than the northern oscillators. Additionally, the output power of these oscillators is about 3dB lower. In this case, both southern oscillators demonstrated lower power. To prevent coupling to the antenna, the power supply connections were run from along one axis on the chip. The power supply was provided along the x-axis in the microphotograph in Figure 8.9. Consequently, both northern oscillators are located closer to the power supply pads, and the resulting drop in power seems most likely due to voltage drop along the supply lines. As the oscillators are tuned together, the locking range determines the usable oscillator frequency range.

To characterize the performance of the coupled oscillator array, a VCO test-structure is initially measured under injection locking conditions. The phase noise of the free-running oscillator as well as the locked oscillator is demonstrated in Figure 8.11. The locked oscillator phase noise tracks the injected reference with 6dB higher phase noise. The injected signal is at 20GHz, and the phase noise is measured at 40GHz. Consequently, there is a 6dB penalty in the phase noise of the locked on-chip oscillator. At 1MHz offset, the phase noise of the locked oscillator is at -112dBc/Hz. The injection locking characteristics are measured as a function of injection power. In Figure 8.12, the carrier

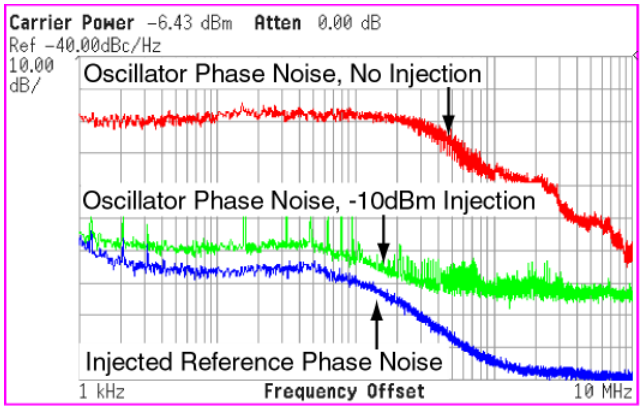


Figure 8.11 Phase noise of reference, injection locked oscillator, and unlocked oscillator.

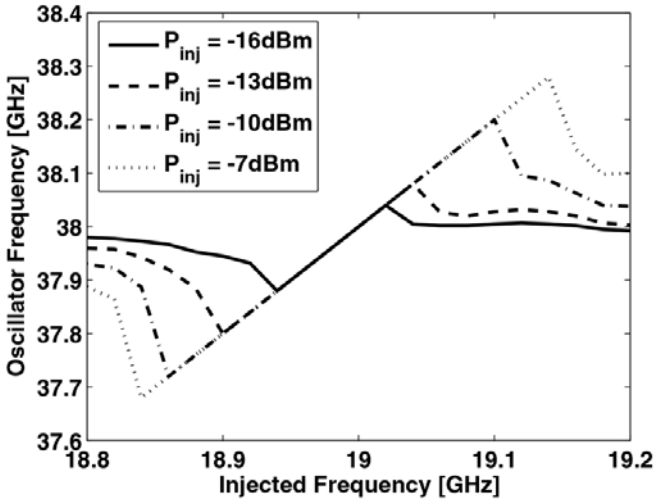


Figure 8.12 Locking range for the VCO as a function of injected power.

frequency is measured as a function of the injected subharmonic frequency. At P_{inj} = -16dBm, the locking range is around 60MHz and increases to 320MHz at P_{inj} = -7dBm. To verify these locking range results, we compare the expression for the locking range to these measured results. If the locking range is 320MHz and the tank Q is around 10,

$$I_{inj} = I_{osc}\frac{2Q\Delta\omega_m}{\omega_o} = 10mA\frac{2(10)(320MHz)}{(40GHz)} = 1.6mA. \quad (8.11)$$

Comparing this to our simulations in Figure 8.7 provides agreement about anticipated injection current levels.

In Figure 8.13 the phase noise of the 2x2 coupled oscillator array structure is shown with and without injection locking. In this case, the average phase noise of each oscillator is around -93dBc/Hz at 1MHz offset. Next, a -10dBm external reference is injected at the NW and SW oscillators. The injection current, controlled with V_{bi}, was set to draw 8mA per cell. The oscillator phase noise was consecutively measured without changing the operating conditions. The phase noise of the injection locked VCOs is around -114dBc/Hz at 1MHz offset and the phase noise of the reference oscillator. The locking range for the array under these conditions is about 200MHz. The operation of the locked array is limited

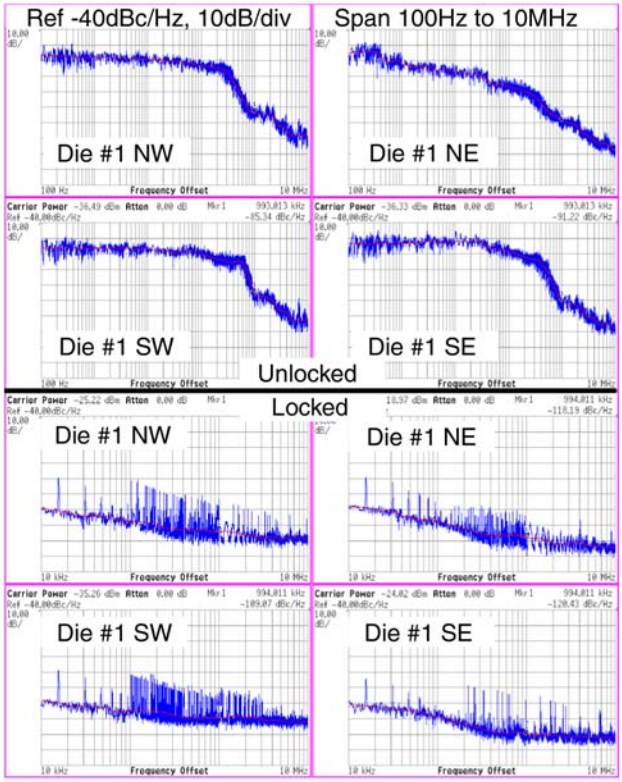


Figure 8.13 Phase noise of each oscillator in 2x2 single chip array without (Top) and with (Bottom) injection locking.

by the natural frequency and power variations for each oscillator due to process and circuit mismatches. This affects the phase noise of each oscillator in the array.

The phase of each oscillator can also be measured at 20GHz with a high-speed sampling scope. The externally injected signal is used to trigger the high-speed scope. The phase progression of each oscillator is demonstrated in Figure 8.14. Each oscillator demonstrates a phase variation of roughly -60 to 70 degrees over the 220MHz locking range. This locking range is measured at the subharmonic frequency, but the phase variation is calculated for the actual carrier frequency. Voltage variations strongly influence the locking range. The southern oscillators demonstrate a smaller locking range.

Additionally, the frequency detuning between the reference oscillator and the natural frequency was scanned to measure the change in the phase noise. As demonstrated in

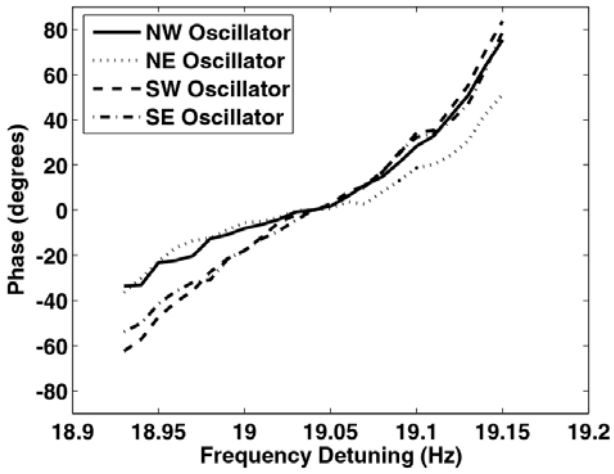


Figure 8.14 Phase of each oscillator in array across locking range.

[140], the phase noise changes as function of the frequency detuning depending on the frequency offset. The curve in Figure 8.15 qualitatively agrees with those predictions, as the phase noise increases near the edges of the locking range. To achieve the best phase noise performance across a grid of oscillators we need to minimize the frequency detuning to also achieve the lowest global phase noise.

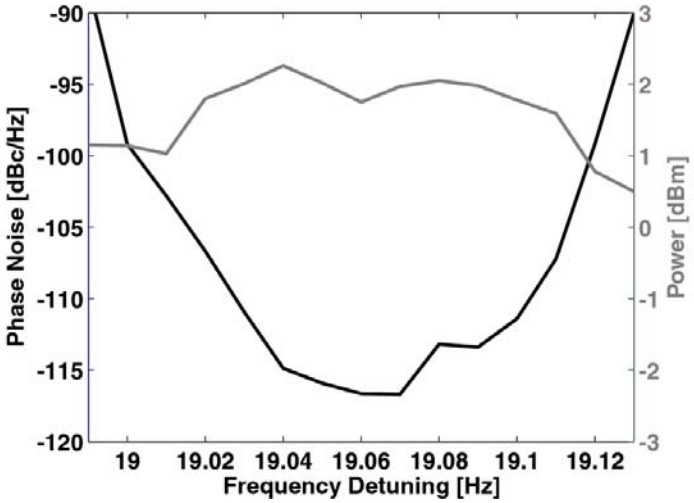


Figure 8.15 Phase noise of NW oscillator as a function of frequency detuning.

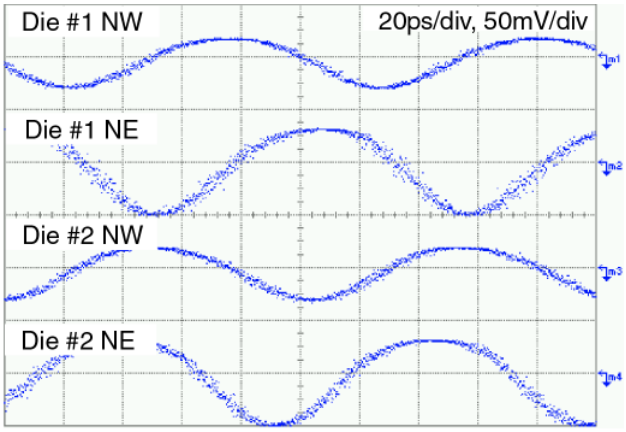


Figure 8.17 Oscilloscope waveforms for 20GHz injection across 1X4 array.

Finally, a 1x4 oscillator array is measured in Figure 8.16 with an external injection signal of -10dBm at the NW oscillator of die #1. The locking range under these conditions is roughly 60MHz and is reduced because only the in-phase signals are used to injection lock the array. The phase noise at 1MHz at the oscillator locked to the external reference is -110dBc/Hz. Each consecutive oscillator has phase noise of -105dBc/Hz, -107dBc/Hz, -108dBc/Hz. The phase noise would ideally increase across the array but does not display this pattern. This behavior results from the natural frequency detuning between the neighboring oscillators as well as the oscillator bias variations. Nonetheless, the low phase noise across the two chips is encouraging for demonstrating larger arrays by locking on-chip oscillators to off-chip reference signals. The phases of each oscillator in the 1x4

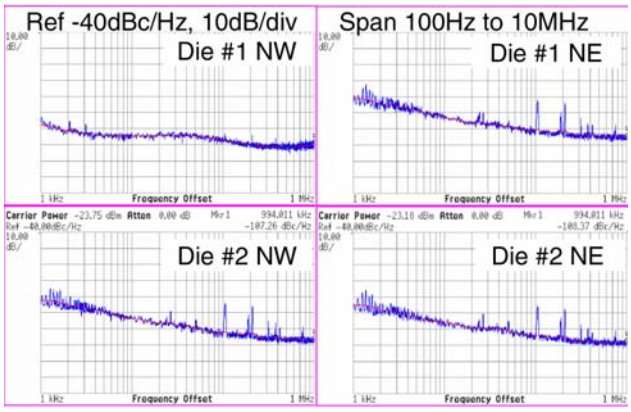


Figure 8.16 Phase noise of oscillators across a 1x4 array with 2 chips.

array are shown in Figure 8.17. The phase shift introduced between the two dies is nearly 180 degrees, while the phase difference between the on-chip oscillators is smaller.

8.5 Summary

This paper describes the implementation of a coupled oscillator array for submillimeter applications. The coupled oscillator employs quadrature subharmonic injection locking to couple neighboring chips connected through wirebonds. Measurement of the oscillator array demonstrates reduced phase noise when locked to an external reference. The locking range was measured to be 220MHz for the oscillators on a single die and is limited by the process and voltage variations that exist over the large die area.

Chapter 9 Conclusions

9.1 Thesis Summary

This thesis introduced new methods to analyze and model deterministic jitter in broadband communication links. The analysis is used to demonstrate new equalization techniques targeted at reducing deterministic jitter. The analysis and modeling of data-dependent jitter (DDJ) focus on the particular bandwidth limitations that occur in high-speed serial communication. Closed-form analytical solutions are shown for a first-order system. The threshold crossing times spread across a greater range of the total bit period as the bandwidth decreases. The analysis is shown to provide a probabilistic model for the purpose of calculating the BER impairment due to DDJ. DDJ in higher-order systems can be estimated with a first-order approximation from the channel response. The analysis is compared to jitter observed in data eyes subjected to first- and second-order filters as well as transmission lines. The experimental results show that the simple approximations predict the observed jitter peaks with 15% error.

The analysis is extended to study 4-PAM modulation schemes. This scheme is particularly interesting because it relies on multiple voltage thresholds to detect each symbol. Consequently, there is an inherent threshold crossing time deviation depending on what symbols the signal moves between. We demonstrate PDF calculations consistent with measurement as well as BER calculation. Additionally, we extend the first-order analysis to 4-PAM and directly compare the DDJ trade-offs to 2-PAM.

Finally, the analysis is extended to study the impact of voltage threshold offsets on deterministic jitter. The resulting DCD PDF shows that the DCD can be treated separately as an independent source of jitter.

The analysis relates the DDJ to a particular data sequence. Therefore, we construct a Markov model to study the cycle-to-cycle behavior of jitter as well as the jitter PSD. These behaviors are important to the operation of clock and data recovery circuits and other transition sensitive functions. However, they are not readily available from the probabilistic interpretation of DDJ. The Markov model provides information about the stochastic progression through each particular DDJ. The model demonstrates agreement with the simulated jitter PSD. Finally, we provide an example of the Markov model that can improve the design of Hogge phase detector circuits by eliminating the sensitivity to DDJ.

The analysis of DDJ provides new insight into jitter equalization. Since the data sequence can be uniquely related to individual threshold crossing times, these equalizers observe the data sequence and compensate the timing through the transmitter or receiver to compensate the DDJ introduced through the communication channel. Several CMOS and BiCMOS implementations for the DDJ equalizer are suggested. Data-dependent jitter equalization is discussed at the receiver where it can complement the operation of clock and data recovery circuits. This circuit demonstrates that the use of data-dependent jitter equalization reduces the phase noise on the sampling clock and opens the data eye. Consequently, minimizing the data-dependent jitter benefits the bit-error rate performance of the communication link.

Next, data-dependent jitter equalization is discussed as a phase pre-emphasis technique. Conventionally, the channel bandwidth is compensated with amplitude pre-emphasis at the transmitter. This type of equalization increases the gain for high-frequency signal components relative to the low-frequency components. However, this increases the power consumption of the transmitter drastically. We discuss a new transmitter that combines phase and amplitude pre-emphasis simultaneously. Phase pre-emphasis only varies the transmitted data edges and can provide much lower power consumption. Consequently, using a combination of phase and amplitude pre-emphasis

may offer lower power consumption while providing significant channel compensation. In a cable, the jitter pre-emphasis reduces the jitter by 5ps rms. In a 16” backplane, the jitter pre-emphasis is shown to improve the jitter by 2.6ps rms.

Crosstalk is unavoidable in practical high-speed serial links because several adjacent serial links operate simultaneously. The links are unshielded because of density requirements and pass through connectors which introduce additional crosstalk. The crosstalk-induced jitter was demonstrated to be related to the mutual inductance and coupling between neighboring transmission lines. The timing deviation was demonstrated to consist of three discrete values that depend on the relationship between the mode on the neighboring lines. When more complex modulation schemes such as 4PAM are introduced, the timing ambiguity is increased.

Bounded-uncorrelated jitter due to crosstalk can also be compensated. By detecting the electromagnetic modes between neighboring serial links, a transmitter or receiver can anticipate the timing deviation that has occurred along the transmission line. Consequently, delay can be introduced to remove the crosstalk-induced transition deviation. An equalizer for 2-PAM is designed that uses standard logic to perform the mode calculation. The circuit is fabricated in 130nm MOSFET technology and operates between 5 and 10Gb/s. Reduction in the rms and peak-to-peak jitter are demonstrated in the data eye. Bathtub curve measurements verify the improved timing margins. At 5Gb/s the timing margins are improved by 41ps with the use of the crosstalk equalizer.

Finally, we discuss a new circuit technique for submillimeter integrated circuits. The demands of future wireless networks will incorporate fully integrated phased arrays which can control a radiated beam pattern electronically. The high speed of Silicon Germanium transistors allows unique architectures for the design of submillimeter integrated phased array circuits. Distributing the carrier signal to every element is difficult. However, keeping the phase coherent between neighboring phased array elements is essential to optimal phased array operation. Therefore, we suggest placing the oscillator at each

antenna element and injection locking neighboring oscillators to produce phase coherence between the neighboring elements. These oscillators are locked across a die or between multiple chips through a subharmonic injection locking scheme. We demonstrate a 60GHz transmitter with fully integrated antennas and discuss the design challenges for the demands of a silicon integrated antenna and the coupling between oscillators. The measured oscillator phase noise across a locked array is below -110dBc/Hz when locked to an external reference.

9.2 Future Investigation

The development of future high-speed serial transceivers is motivated by 1) maximizing the bandwidth per pin and 2) minimizing the power per bandwidth. The first goal will motivate research into more complicated modulation and equalization techniques to manage bandwidth limitations. The second goal compels simplicity in both circuit implementations as well as the computational complexity required for equalizer adaptation.

Additionally, three trends in electronics will significantly impact both of these goals. First, the speed of CMOS standard cell logic is catching up to link bandwidths. The first trend implies that in the future additional digital signal processing may be available for the serial transceiver. This might provide low-power coding as well as more complicated equalization such as maximum-likelihood estimation. Second, newer device technologies feature multiple-Vt devices for power minimization. Thus, the circuit designer can assign speed sensitive circuits to low-Vt technologies that have much higher leakage current while implementing high-Vt devices for lower speed digital signal processing. Third, voltage scaling will force the supply below one volt.

Thus we have some idea of the goals and limitations of future serial links. Let us consider how different modulation schemes fit into these criteria. The first is 4PAM, which has been discussed to some extent in this thesis and in greater detail by Stojanovic

[33]. Unfortunately, while 4PAM allows greater utilization of the bandwidth, it requires a range of amplitude levels and, hence, more voltage headroom which does not allow voltage supply scaling. The use of thick-oxide devices may overcome this limitation with multiple supplies on a single chip. However, 4PAM does not benefit our jitter problem.

The second modulation scheme is duo-binary which inherently compensates the ISI introduced through the channel. This modulation technique is particularly interesting since the pulse response tailoring in the receiver may become easier with additional signal processing.

High-speed equalization circuits have been studied in great detail for both optical and serial communication. Several extensions introduced in this thesis may benefit the design of decision feedback equalizers, currently popular in serial links. The DFE circuit could be modified to adjust both the voltage threshold and sampling time dynamically, offering the simultaneous advantages of both DDJ equalization and DFE. Effectively, we can imagine the data eye cut into four quadrants where we alternately sample the quadrants depending on the different bit sequences. This sampling technique is shown in Figure 9.1. The data eye chooses sampling times based on previous transitions and voltage thresholds based on the previous bit. Therefore, the likelihood of bit error due to the voltage and timing degradation is minimized.

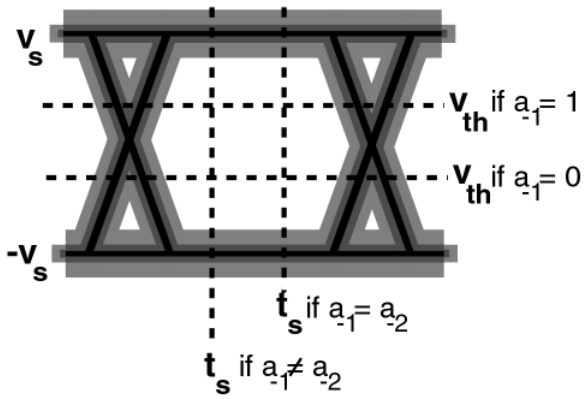


Figure 9.1 Suggested future implementation of combination DDJ equalizer and DFE to appropriately sample the data eye in bandwidth-limited interconnects.

It seems likely that equalization will eventually be limited by the computational power required to adapt the equalizer coefficients for each of the thousand links that might exist in a serial link. As each DFE may have several coefficients to cancel the effects of channel reflections and bandwidth limitation, the computational problem of determining the appropriate coefficients becomes more difficult. In particular, one approach is to train the coefficients initially and to provide little adaptation during the operation of the serial link.

Finally, the migration of electrical serial links seems inevitable given a suitable opto-electronic packaging technique. The optical bandwidth provided over these short lengths is greater than 20Gb/s. However, the electronic transceiver problems will likely remain. Many of the lessons of high-speed electrical transceivers will translate to this new optical domain, and the equalization techniques will focus on dispersion in the link as opposed to the attenuation introduced by frequency-dependent loss. Consequently, there is some reason to believe that the data-dependent jitter equalizers suggested in this thesis will be useful in future optical interconnects.

Appendix

A

First-Order Threshold Crossing Times

A.1 Threshold Crossing Times and Mean and Variance

From (3.8), the threshold crossing times for a first order system can be calculated. If we limit ourselves to data sequences with only four bits, the eight possible threshold crossing times are calculated in Table A.1.

Table A.1: List of Threshold Crossing Times in a First-order Response, $k = 4$.

Sequence i	Threshold Crossing Time
t_1	$\tau \log\left[\frac{1}{1-v_{th}}\right]$
t_2	$\tau \log\left[\frac{1-\alpha}{v_{th}}\right]$
t_5	$\tau \log\left[\frac{1-\alpha+\alpha^2}{1-v_{th}}\right]$
t_6	$\tau \log\left[\frac{1-\alpha^2}{v_{th}}\right]$
t_9	$\tau \log\left[\frac{1-\alpha^2}{1-v_{th}}\right]$
t_{10}	$\tau \log\left[\frac{1-\alpha+\alpha^2}{v_{th}}\right]$
t_{13}	$\tau \log\left[\frac{1-\alpha}{1-v_{th}}\right]$
t_{14}	$\tau \log\left[\frac{1}{v_{th}}\right]$

These values can be used to approximate the mean for the threshold crossing times. Assuming that all values are sampled equally,

$$m_{DDJ} = \frac{\tau}{4}\log\left[\frac{(1-\alpha)(1-\alpha+\alpha^2)(1-\alpha^2)}{v_{th}^2(1-v_{th})^2}\right]. \tag{A.1}$$

The variance is calculated easily by determining $E[(t_i - m_{DDJ})^2]$ and is

$$\sigma_{DDJ}^2 = \frac{\tau^2}{64}\left[\begin{array}{l} 4\left(\log\left[\frac{v_{th}^2}{(1-v_{th})^2}\right]\right)^2 + \left(\log\left[\frac{1}{(1-\alpha)(1-\alpha+\alpha^2)(1-\alpha^2)}\right]\right)^2 \\ \quad + \left(\log\left[\frac{(1-\alpha)^3}{(1-\alpha+\alpha^2)(1-\alpha^2)}\right]\right)^2 + \left(\log\left[\frac{(1-\alpha+\alpha^2)^3}{(1-\alpha)(1-\alpha^2)}\right]\right)^2 \\ \quad + \left(\log\left[\frac{(1-\alpha^2)^3}{(1-\alpha)(1-\alpha+\alpha^2)}\right]\right)^2 \end{array}\right]. \tag{A.2}$$

When the precision of these terms is unnecessary, these equations can be approximated for $k = 3$ by setting $\alpha^2 \sim 0$, and we find

$$m_{DDJ} = \frac{\tau}{2}\log\left[\frac{(1-\alpha)}{v_{th}(1-v_{th})}\right] \tag{A.3}$$

and

$$\sigma_{DDJ}^2 = \frac{\tau^2}{4}\left[\left(\log\left[\frac{v_{th}}{1-v_{th}}\right]\right)^2 + (\log[1-\alpha])^2\right]. \tag{A.4}$$

In both (A.2) and (A.4) the duty-cycle variation is immediately separable.

If we consider the situation when only the rising or falling edge is important, we eliminate half of the states in Table A.1. For instance, if we consider rising edge sensitivity, the mean is

$$m_{DDJ,\,r} = \frac{\tau}{4}\log\left[\frac{(1-\alpha)(1-\alpha+\alpha^2)(1-\alpha^2)}{(1-v_{th})^4}\right] \tag{A.5}$$

and the variance is

$$\sigma^2_{DDJ,\,r} = \frac{\tau^2}{32}\left[\begin{array}{l}\left(\log\left[\frac{1}{(1-\alpha)(1-\alpha+\alpha^2)(1-\alpha^2)}\right]\right)^2 + \left(\log\left[\frac{(1-\alpha+\alpha^2)^3}{(1-\alpha)(1-\alpha^2)}\right]\right)^2 \\ \quad + \left(\log\left[\frac{(1-\alpha)^3}{(1-\alpha+\alpha^2)(1-\alpha^2)}\right]\right)^2 + \left(\log\left[\frac{(1-\alpha^2)^3}{(1-\alpha)(1-\alpha+\alpha^2)}\right]\right)^2\end{array}\right], \tag{A.6}$$

which is the one-half of (A.2). Additionally, the duty-cycle distortion term is no longer present. These equations can be approximated for $k = 3$ as

$$m_{DDJ,\,r} = \frac{\tau}{2}\log\left[\frac{(1-\alpha)}{(1-v_{th})^2}\right] \tag{A.7}$$

and

$$\sigma^2_{DDJ,\,r} = \frac{\tau^2}{2}(\log[1-\alpha])^2 \tag{A.8}$$

for comparison to the approximated mean and variance in (A.3) and (A.4).

A.2 Cycle-to-*n*th Cycle Jitter

We capture the movement from one state to another in the state transition matrix in (3.31) as it applies for cycle-to-n^{th} cycle jitter. In this definition we want to consider that if a particular transition occurs how long will it take to reach the next transition and what transition can we expect. In Table A.2, we summarize the movement between state *i* to state *j* for rising and falling edge sensitivity.

Table A.2: Possible Transitions for Cycle-to-n^{th} Cycle Jitter (Rising and Falling Edges)

n	**1**	**2**	**3**	**m**
P{N=n}	1/2	1/4	1/8	$1/2^m$
Possible Transitions	$t_1 \to t_2$ $t_2 \to t_5$ $t_5 \to t_{10}$ $t_6 \to t_{13}$ $t_9 \to t_2$ $t_{10} \to t_5$ $t_{13} \to t_{10}$ $t_{14} \to t_{13}$	$t_1 \to t_6$ $t_2 \to t_9$ $t_5 \to t_6$ $t_6 \to t_9$ $t_9 \to t_6$ $t_{10} \to t_9$ $t_{13} \to t_6$ $t_{14} \to t_9$	$t_1 \to t_{14}$ $t_2 \to t_1$ $t_5 \to t_{14}$ $t_6 \to t_1$ $t_9 \to t_{14}$ $t_{10} \to t_1$ $t_{13} \to t_{14}$ $t_{14} \to t_1$	$t_1 \to t_{14}$ $t_2 \to t_1$ $t_5 \to t_{14}$ $t_6 \to t_1$ $t_9 \to t_{14}$ $t_{10} \to t_1$ $t_{13} \to t_{14}$ $t_{14} \to t_1$

From this table it is clear that the mean for each progressive bit interval changes. The mean after the nth interval without a transition is denoted $m_{DDJ,\Delta n}$. For Table A.2, we find

$$\begin{aligned} m_{DDJ,\Delta 1} &= \frac{\tau}{2}\log\left[\frac{(1-\alpha)(1-\alpha+\alpha^2)}{v_{th}(1-v_{th})}\right], \\ m_{DDJ,\Delta 2} &= \frac{\tau}{2}\log\left[\frac{(1-\alpha^2)^2}{v_{th}(1-v_{th})}\right], \text{ and} \\ m_{DDJ,\Delta 3} &= \frac{\tau}{2}\log\left[\frac{1}{v_{th}(1-v_{th})}\right]. \end{aligned} \tag{A.9}$$

From these means we calculate the variance after each bit interval in Chapter 3. Similarly we can calculate this behavior when only one transition (rising) edge is important. In Table A.3 the possible rising edge states and consecutive states are illustrated.

Table A.3: Possible Transitions for Cycle-to-n^{th} Cycle Jitter (Rising Edge Only)

n	**1**	**2**	**3**	**m**
P{N=n}	0	1/2	1/4	$1/2^{m-1}$
Possible Transitions		$t_1 \rightarrow t_5$ $t_5 \rightarrow t_5$ $t_9 \rightarrow t_5$ $t_{13} \rightarrow t_5$	$t_1 \rightarrow t_9, t_{13}$ $t_5 \rightarrow t_9, t_{13}$ $t_9 \rightarrow t_9, t_{13}$ $t_{13} \rightarrow t_9, t_{13}$	$t_1 \rightarrow t_1, t_9, t_{13}$ $t_5 \rightarrow t_1, t_9, t_{13}$ $t_9 \rightarrow t_1, t_9, t_{13}$ $t_{13} \rightarrow t_1, t_9, t_{13}$

The mean after the n^{th} interval is

$$m_{DDJr,\,\Delta 1} = \tau \log\left[\frac{(1-\alpha+\alpha^2)}{(1-v_{th})}\right],$$

$$m_{DDJr,\,\Delta 2} = \frac{\tau}{2}\log\left[\frac{(1-\alpha^2)(1-\alpha)}{(1-v_{th})^2}\right], \text{ and} \qquad \text{(A.10)}$$

$$m_{DDJr,\,\Delta 3} = \frac{\tau}{3}\log\left[\frac{(1-\alpha^2)(1-\alpha)}{(1-v_{th})^3}\right]$$

These expressions can be used to calculate the variance for the cycle-to-n^{th} cycle jitter and determine the effect on transition sensitive circuits.

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