SWITCHING CONVERTERS FOR INPUT CURRENT SHAPING AND REGULATION OF MULTIPLE OUTPUTS

Thesis by
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Abstract

A novel class of isolated Capacitive Idling switching power converters featuring decoupled primary and secondary side feedback loops is presented. While preserving the cost, size and simplicity of the conventional multiple output dc-to-dc converters, this new class of isolated converters possesses the following advantages: no need to cross isolation barrier in the feedback, full regulation of all outputs from no-load to full-load, faster transient response, and independent short circuit protection of each output.

Operation of the Capacitive Idling converters in single-phase ac-to-dc power conversion systems is also analyzed. It is found that these converters perform input current shaping automatically, i.e., without an input current feedback loop. This is achieved by operating primary side inductance(s) in discontinuous inductor current mode (DICM). Consequently, the high power factor performance is obtained without any penalty in complexity, cost and size of the converter.

Input current shaping and full regulation of multiple outputs is made possible by the internal energy storage and presence of one secondary-side active switch for each output. When compared to conventional current shaper-regulator configurations involving up to three cascaded power stages, the new converter class represents a very attractive alternative. The main advantages of the Capacitive Idling shapers are:

— current shaping and regulation in a single power stage,

— simplified control implementation with no feedback isolation,

— wide bandwidth loop gain on all outputs,

— independent short-circuit protection of each output.

Analysis of the Capacitive Idling converters reveals that the input current shaping mode of operation involves a trade-off between the high power factor and the increased switch voltage stress. Boundary of the DICM of operation is determined, resulting in a design equation for the primary side inductance(s). Experimental results verify the analysis and confirm that these

converters represent a viable and attractive approach for input current shaping and multiple output regulation.

Contents

Chapter 1
Introduction

Switching power converters have over the decades emerged as an indispensable, yet often overlooked part of our everyday life. From electronic office equipment to automobiles, power converters can be found in all signal processing electronic systems that are so vital in this age of information technology, in safety electro-mechanical devices such as anti-lock brakes, and in comfort and luxury features of power adjustments from mirrors to seats found in most modern cars. Moreover, efficient and environmentally clean electric vehicle is no longer a futuristic dream, but a technologically viable approach.

The need for power converters stems from the fact that the available power source seldom matches needs of the load at hand. Instead, the voltage level and/or frequency of the source need to be converted in order to meet the requirements of the load. Depending on the type of input and output waveforms, switching converters can be classified in several categories: dc-to-dc, ac-to-dc, ac-to-ac and dc-to-ac. The focus of this thesis will be mainly on dc-to-dc and single-phase ac-to-dc switching converters.

Motivation

Most modern switching power supplies are prone to several practical problems:

—For safety and other reasons, an isolation transformer is required in most switching converters. In addition to the isolation in the power processing stage, this also requires isolation in the control circuitry, leading to a significant increase in complexity and cost of the overall system [1].

—For cost and size reasons, multiple output converters are preferred in the majority of practical applications. These converters provide multiple output voltages in a single power stage. The problem is that only one output can be fully regulated, leading to unacceptable voltage variations on auxiliary outputs when the converter enters discontinuous conduction mode of operation. This problem is usually solved by addition of a switching post-regulator to each

auxiliary output [2]. However, this substantially degrades the conversion efficiency and increases total cost of the power supply.

—Another drawback of conventional multiple output regulators is that the power stage has high order dynamics and, consequently, complicated frequency response. In addition to that, input voltage variations strongly affect the low frequency gain and corner frequencies of the converter control transfer function. This imposes a very severe limitation on the bandwidth, since the loop-gain has to be closed at a relatively low frequency before the phase lag exceeds the stability limit of 180°. Consequently, the converter crossover has to be chosen at a conservatively low frequency in order to meet the worst case scenario.

—In ac-to-dc applications, a requirement for low harmonic content of the input current is increasingly promoted by new regulations [3]. Such standards require addition of an input current shaping feature to virtually all single-phase ac-to-dc switching converters. The conventional solution is to use the front-end switching converter to perform input current shaping, followed by an isolated downstream converter providing regulated output voltage. This additional front-end power stage increases size and weight of the power supply and reduces the overall conversion efficiency. The situation is even worse when there is a need for several fully regulated output voltages, in which case a separate post-regulator is added for each auxiliary output.

Organization of the Thesis

The thesis describes a novel class of switching regulators which overcomes each of these practical problems. Parts of this work have been published in [4] and [5].

Chapter 2 introduces a Capacitive Idling class of dc-to-dc converters. The advantages of the new converter class are demonstrated on the example of the Capacitive Idling Ćuk converter. The dc properties of this converter are analyzed in Section 2.2 and the decoupling of the dc conversion ratio described in Section 2.3. This leads to the elimination of feedback isolation as described in Section 2.4, and furthermore to the multiple output extension capable of providing full regulation of all outputs. Beneficial decoupling of the frequency responses of the two feedback loops is described in Section 2.5, with experimental results shown in Section 2.6. Generalization to the entire class of Capacitive Idling converters is described in Section 2.7.

In Chapter 3 the extension of Capacitive Idling converters to single-phase ac-to-dc applications is described. It is demonstrated that these converters can perform both input current shaping and wide bandwidth regulation of multiple outputs in a single power stage. The analysis is focused on four prominent members of the Capacitive Idling (CI) converter class: CI inverse SEPIC, CI flyback, CI Ćuk, and CI SEPIC. In Section 3.2, topology requirements for input current shaping and load regulation are examined. Dc-to-dc mode of operation of the CI converters is reviewed in Section 3.3, with emphasis on decoupled primary and secondary side feedback loops. All three discontinuous inductor current modes (DICM) that are possible in these converters are identified in Section 3.4. The analysis of this Section is focused on one particular discontinuous mode where the primary side inductor current is discontinuous, while the output inductor current is continuous. In Section 3.5 the expressions for power factor and DICM boundary in ac-to-dc mode of operation are derived. Section 3.6 presents experimental results that illustrate the concept and verify the analysis. The principal conclusions are discussed in Section 3.7.

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Chapter 2
Capacitive Idling Converters with Decoupled Input Voltage and Load Regulation Loops

Abstract — **A novel class of isolated capacitive idling converter topologies featuring decoupled primary and secondary side feedback loops is presented. While preserving the cost, size and simplicity of the conventional multiple output converters, this new converter class possesses the following advantages: no need for isolation in the feedback, full regulation of all outputs from no-load to full-load, faster transient response, and independent short circuit protection of each output.**

2.1 Introduction

A typical switching dc-to-dc regulator, such as the forward converter shown in Fig. 2.1, consists of an isolated power stage with multiple outputs and a feedback control circuitry sensing output voltage on the secondary side and driving a primary side active switch. This seemingly simple configuration suffers from three serious practical problems:

1. The need for crossing of the isolation barrier in the control path, leading to a major increase in the circuit complexity and cost [1]. Even this rudimentary feedback implementation requires two isolation transformers in the control circuitry, while feedback circuits featuring some basic protection schemes could have as many as four isolation transformers.

2. Poor cross-regulation in discontinuous conduction mode, leading to an unacceptable voltage variation of the unregulated output. Full load regulation on a second output is usually obtained by use of the cascaded switching post-regulator [2], as shown in Fig. 2.1. However, this substantially degrades efficiency, since the input power is processed twice. Coupling of the output inductors could improve the cross-regulation [3], but the full regulation of multiple outputs is possible only if the number of independent control variables is greater-than or equal to the number of regulated outputs. These control variables could be obtained by introducing an additional controllable device for each output, such as magnetic amplifier [4], or active switch

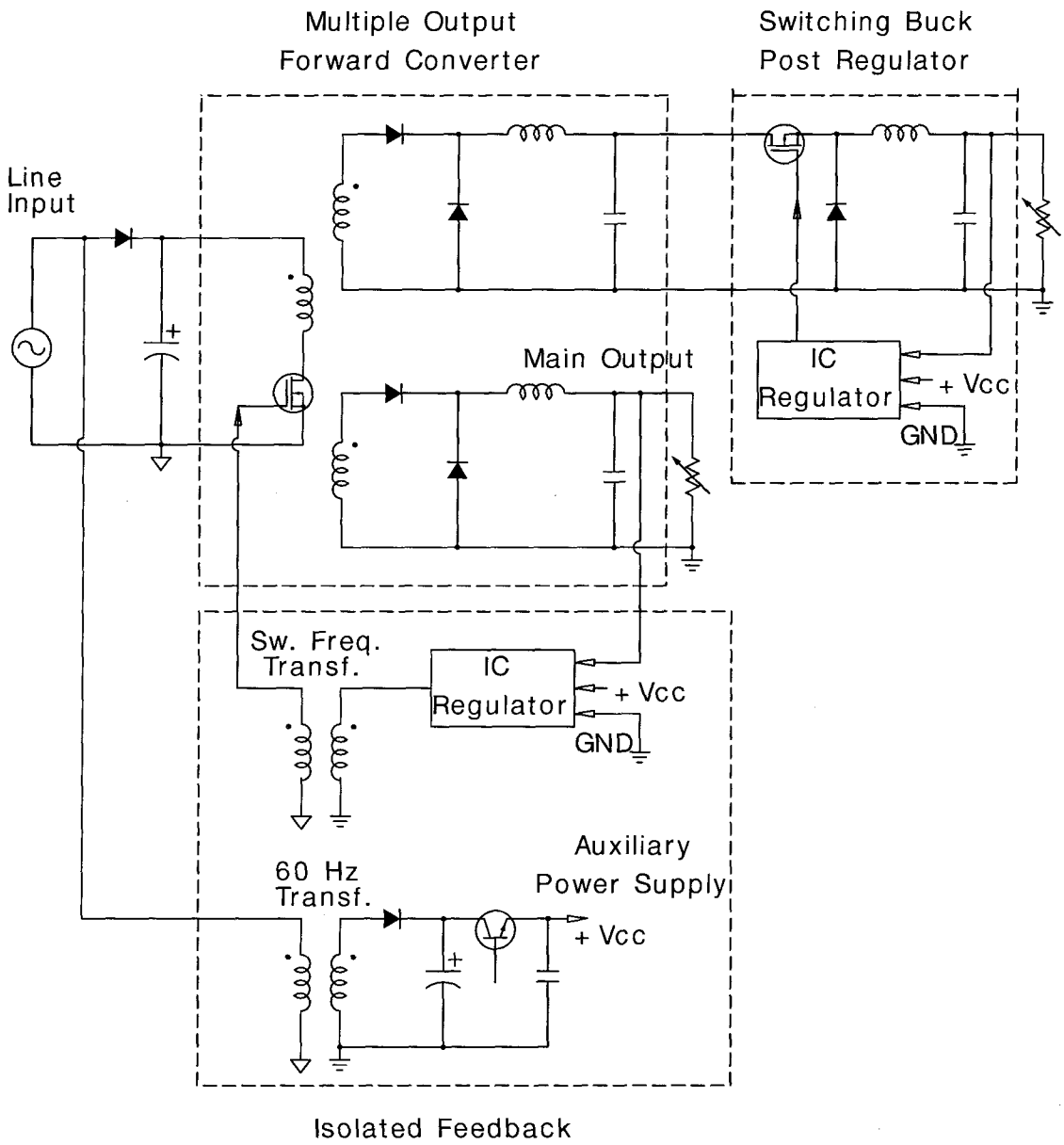


Figure 2.1: *Typical isolated multiple output forward converter with cascaded switching post-regulator requires at least two isolation transformers in its feedback circuitry.*

[5–7], or by operating a second output of the dual output converter in a discontinuous conduction mode while using switching frequency modulation to independently regulate it [8].

3. High order dynamics (fourth-order or higher) and a wide input voltage range lead to a conservative choice of the crossover frequency resulting in a poor transient response. The reason for this is that the frequency response of many fourth-order converters typically exhibits

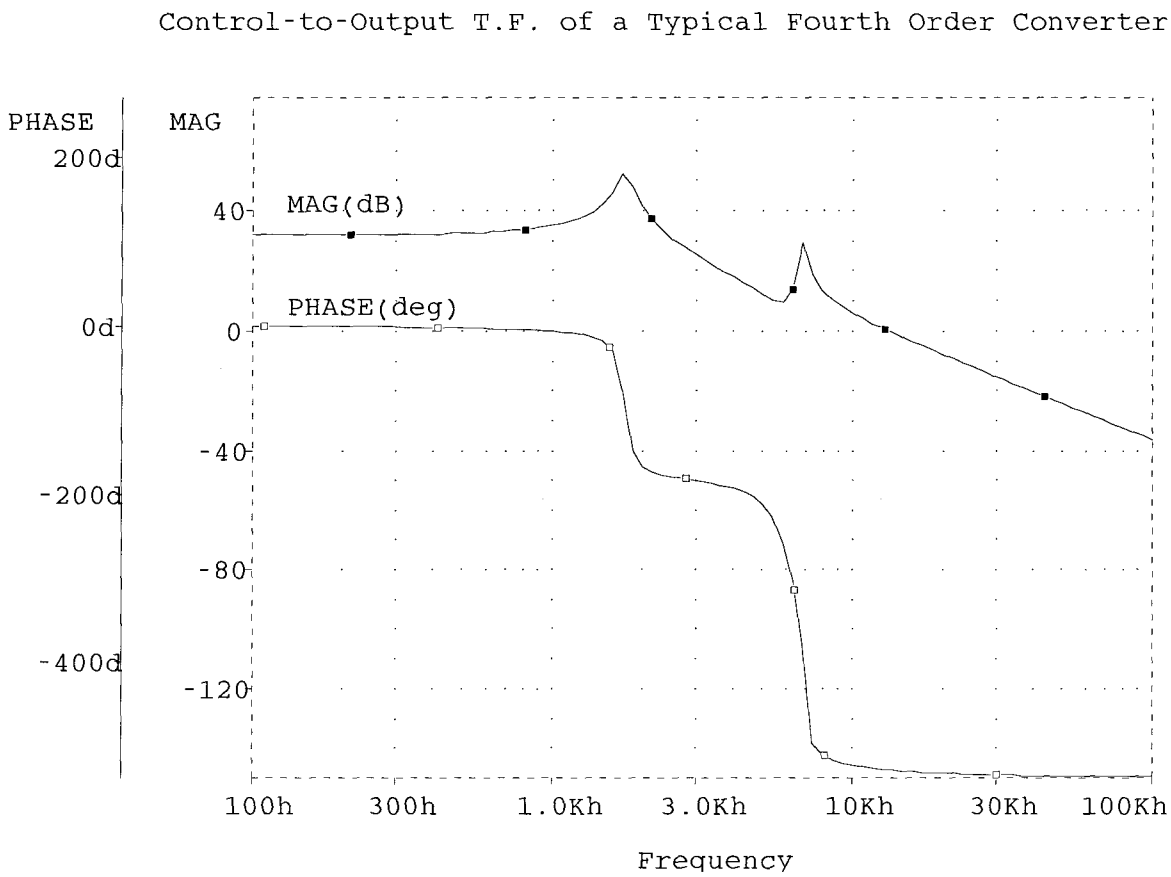


Figure 2.2: *Typical frequency response of the fourth-order converter featuring a pair of right half-plane zeros.*

a nonminimum phase response due to the presence of undesirable right half-plane (RHP) zeros [9]. Figure 2.2 shows the control to output transfer function of a typical fourth-order converter (buck with input filter, boost-buck, etc.). This imposes a very severe limitation on the bandwidth, since the loop-gain has to be closed at a relatively low frequency before the phase lag exceeds the stability limit of 180°. A wide range of input voltage further limits the bandwidth due to the fact that large variation of duty ratio strongly affects corner frequencies and the low frequency gain of the converter control transfer function. Consequently, the converter crossover has to be chosen at an even lower frequency in order to meet the worst case scenario.

Here, a novel class of switching regulators which overcomes each of these three problems is described. The advantages of the new converter class are demonstrated on the example of the Capacitive Idling Ćuk converter. The dc properties of this converter are analyzed in Section

2.2 and decoupling of the dc conversion ratio described in Section 2.3. This leads to the elimination of feedback isolation as described in Section 2.4, and furthermore to the multiple output extension capable of providing full regulation of all outputs. Beneficial decoupling of the frequency responses of the two feedback loops is described in Section 2.5, with experimental results shown in Section 2.6. Generalization to the entire class of Capacitive Idling converters is described in Section 2.7.

2.2 Capacitive Idling Class of Three Switched-Network Converters

It was reported in [7] that the Three Switched-Network (3SN) Ćuk converter can independently regulate multiple output voltages in a single power stage. A nonisolated, single output version of this 3SN topology is shown in Fig. 2.3(a). As explained in [7], the operation of this converter is very similar to that of the basic Ćuk converter. The only difference is the introduction of an idling period $(D - D_1)T_S$, during which the energy transfer capacitor C is disconnected from the rest of the circuit (Fig. 2.4). Independent variation of this idling period is made possible by the presence of an additional pair of switches Q_1, D_1. The position of these two switches is not unique, and Fig. 2.3(b) shows another switch implementation of the same converter. Both of these converters have identical switched networks and consequently the same dc and ac characteristics. However, there is a slight difference in efficiency between the two practical implementations of the Capacitive Idling Ćuk converter. The reason is that during the charging interval of the capacitor C, current i_C is returning through the diode D in the converter of Fig. 2.3(a), as opposed to both diodes D and D_1 in the new topology of Fig. 2.3(b), which makes practical implementation of Fig. 2.3(a) more efficient.

One practical advantage of the new converter of Fig. 2.3(b) is that its current bidirectional switch could be implemented using a single MOSFET device, reducing cost of the power converter.

As explained in Section 2.7, this novel version of the 3SN Ćuk converter provided a valuable insight and motivated the search for new 3SN topologies that resulted in a discovery of an entire class of converters. Their common feature is the idling interval of the energy transfer capacitor (it is neither charging nor discharging, as seen in Fig. 2.4(b)), prompting an alternative name for this converter class: **Capacitive Idling Converters**.

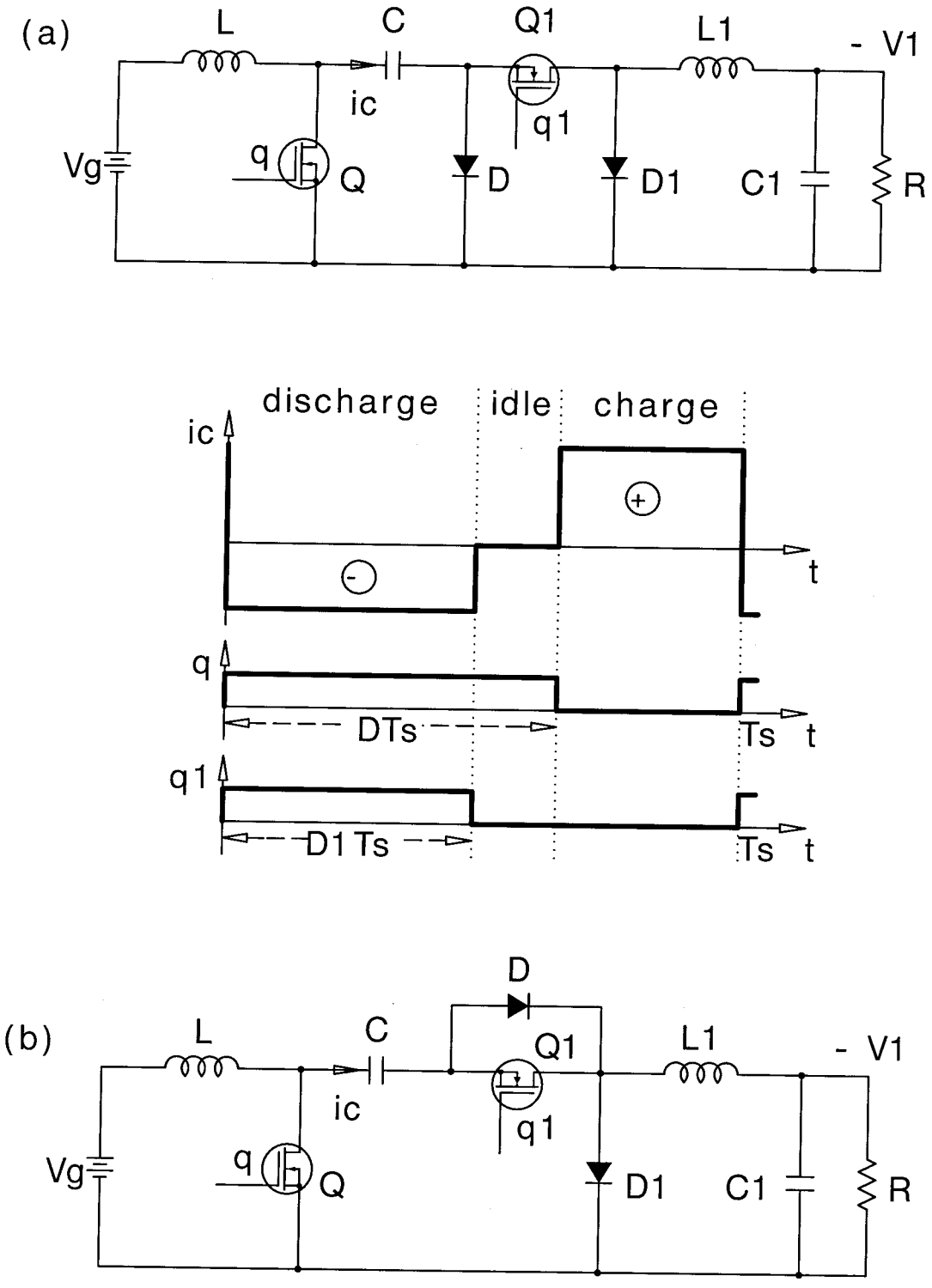


Figure 2.3: *Basic Capacitive Idling Ćuk converter with key waveforms (a) and its alternative switch implementation (b).*

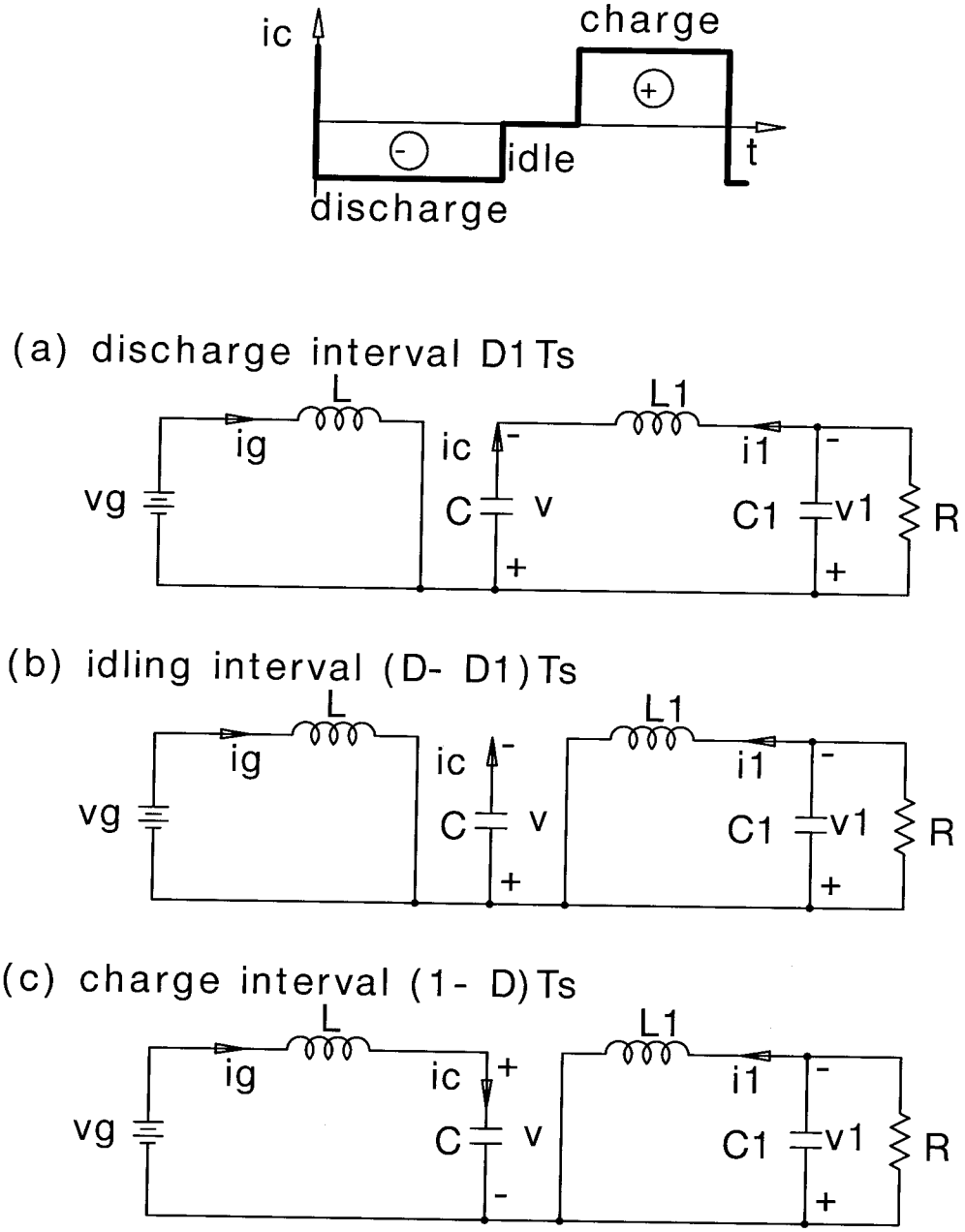


Figure 2.4: Three linear switched-networks of the Capacitive Idling Ćuk Converter.

2.2.1 DC Properties of the Capacitive Idling Ćuk Converter

It is now clear that the addition of the switch pair Q_1, D_1 has introduced an extra degree of control while preserving the charge balance of the energy transfer capacitor C. One has to be careful to interpret the dc conversion properties in terms of newly defined control variables; duty ratio D of Q, and duty ratio D_1 of Q_1 transistor (Fig. 2.3(a)). From the charge balance on the

energy transfer capacitor C and 100% efficiency assumption, the ideal dc conversion ratio is:

$$\frac{I_g}{I_1} = \frac{V_1}{V_g} = \frac{D_1}{1-D} \,. \tag{2.1}$$

As in the basic Ćuk converter, the dc conversion ratio of the Capacitive Idling converter is given by the ratio of the discharge interval to the charge interval of the energy transfer capacitor.

The volt-sec balance on the two inductors yields:

$$V = \frac{V_g}{1-D} \tag{2.2}$$

$$V_1 = V D_1 \,. \tag{2.3}$$

This means that the energy transfer capacitor voltage V is dependent only on the input dc voltage and duty ratio D, while the output voltage is dependent on the voltage V and the transistor Q_1 duty ratio D_1 only. These fundamental equations are of key importance in establishing two separate and independent feedbacks of the converter, as shown in the next Section.

2.3 Decoupling of the Two Main Sources of Disturbance: Input Voltage and Load Current

The control strategy of all basic converters with a single control variable is to regulate the output voltage in the presence of both input voltage and load current variations. Note, however, that the input voltage variation has more significant influence on the duty ratio than the load current change. For example, a 4 to 1 input voltage change (15 to 60 volts) may cause a change of duty ratio from 0.2 to 0.5 or 250%. On the other hand, a load current change of 10 times (from 10% load to full load) causes only a small perturbation of the output voltage as long as the converter remains in the continuous conduction mode of operation. The small change of the output voltage is due to the parasitic losses. The more efficient the converter, the smaller the duty ratio adjustment for the load current regulation. For a 90% efficient converter, the duty ratio may experience only a 10% change. Clearly, it would be very beneficial to separate these two disturbances by preventing wide input voltage changes from affecting the output voltage.

While the Capacitive Idling Ćuk converter has two controllable switches, it is not obvious that there exists a control method which would enable a complete decoupling of these two

disturbances. In fact, in the control method used in [7], the duty cycle D of the converter's main switch Q was kept **constant** and both the input voltage and output load variations were absorbed by the duty ratio D_1 of the additional switch Q_1.

2.3.1 Decoupled Feedback Loops in the Capacitive Idling Ćuk Converter

One can postulate that decoupling of these two sources of disturbance in the converter with two controls D and D_1 is possible if the converter's output voltage is of the form:

$$V_1 = f_1(V_g, D) \cdot f_2(I_1, D_1) \tag{2.4}$$

where f_1 and f_2 are two arbitrary functions, and I_1 is the load current. In the case of an ideal Capacitive Idling Ćuk converter, the output voltage is:

$$V_1 = \frac{V_g}{1-D} \cdot D_1 \tag{2.5}$$

which indicates that the proper control method could eliminate input voltage changes by adjusting the duty ratio D, while the duty ratio D_1 could be used to regulate against load current changes.

The implementation of the two separate control feedback loops in the Capacitive Idling Ćuk converter can be best understood with reference to the cascaded boost-buck converter of Fig. 2.5(a). The front-end boost converter has the output voltage V on the capacitor C given by:

$$V = \frac{V_g}{1-D} \tag{2.6}$$

where D is the duty ratio of the switch Q. The output voltage V_1 of the buck stage is:

$$V_1 = V D_1 \tag{2.7}$$

where D_1 is the duty ratio of the transistor Q_1. It is clear that the feedback loop can be closed around the front-end boost converter to regulate the voltage V against input voltage changes. Obviously, a separate feedback loop can be placed around the output buck converter in order to regulate its output voltage V_1 against load current changes. Thus the **decoupling** of controls into two feedback loops in the straightforward boost-buck cascade of Fig. 2.5(a) is easy to understand. Furthermore, the same is true for the Capacitive Idling Ćuk converter shown in Fig. 2.5(b). Except for the polarity inversion, this converter is equivalent to the boost-buck cascade. This stems from the fact that both converters have identical switched linear networks, as shown in

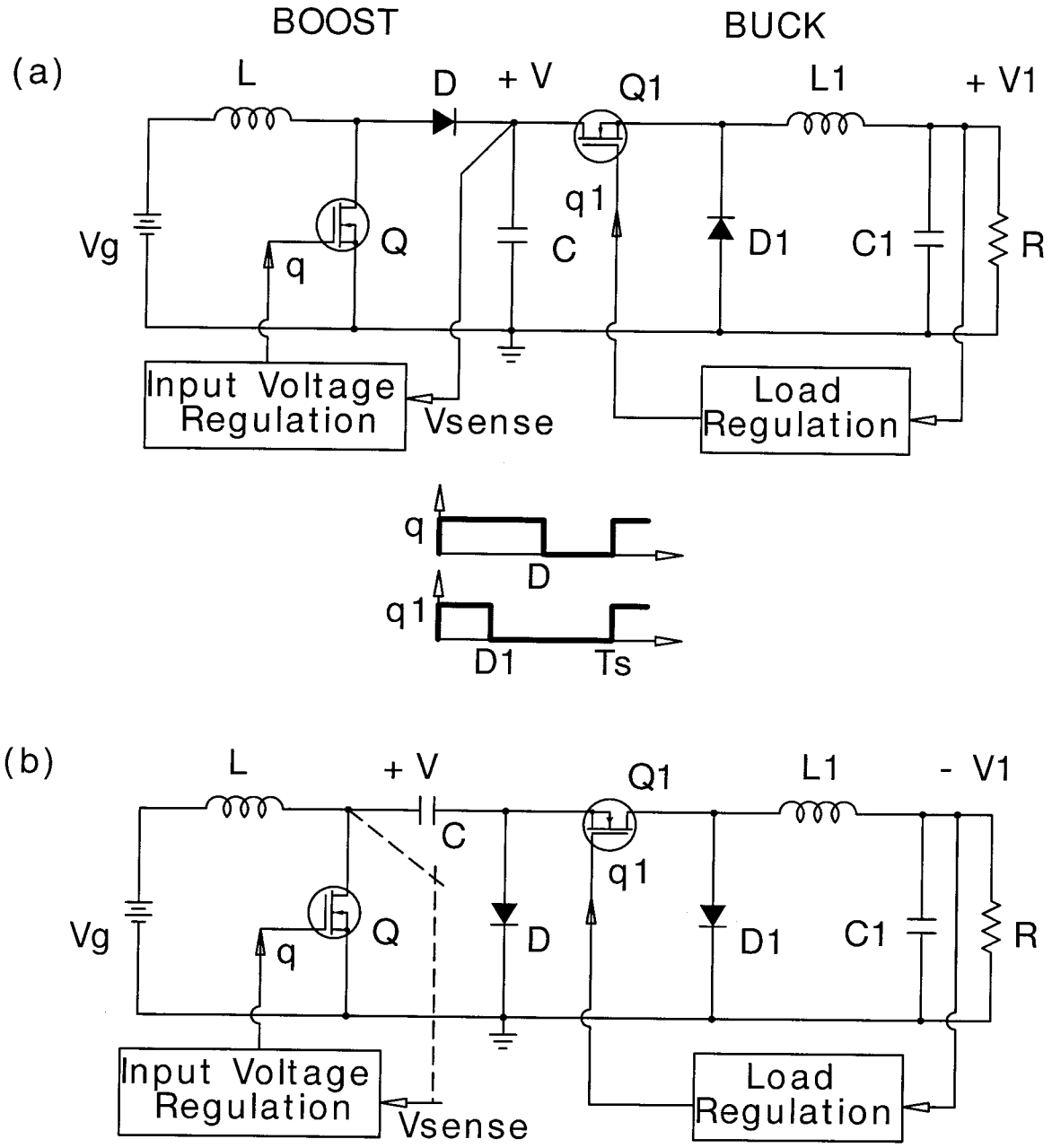


Figure 2.5: *The obvious decoupling of feedback loops in cascaded boost-buck converter (a) helps understand the novel control strategy in the Capacitive Idling Ćuk converter (b).*

Fig. 2.4. Figure 2.5(b) shows a separate feedback loop closed around the input boost-like stage, regulating against input voltage changes. Likewise, the output buck-like stage has a separate feedback loop to regulate against load current changes. Sensing implementation of Fig. 2.5(b) is explained in the next Section.

The key difference between the two regulators of Fig. 2.5 is that the Capacitive Idling Ćuk converter features the floating capacitance C, instead of the grounded capacitance C in the boost-buck converter. This makes a tremendous practical difference, since an isolation transformer can be introduced in the basic Ćuk converter [10], and in the same way into the Capacitive Idling Ćuk converter [7]. Note that the straightforward cascaded boost-buck converter of Fig. 2.5(a) has no practical isolated version with two active switches placed on opposite sides of the isolation transformer.

2.4 Elimination of Feedback Isolation

The isolated version of the Capacitive Idling Ćuk converter is obtained by splitting the energy transfer capacitance C into two and introducing an isolation transformer at the point of the split. All properties of the nonisolated Capacitive Idling converter of Fig. 2.5(b) are retained in its isolated extension of Fig. 2.6.

Moreover, the same decoupling of the two feedback loops in the nonisolated case of Fig. 2.5(b) is now made possible in its isolated version. In fact, the isolation transformer now completely separates the feedback to the primary side feedback loop, and the secondary side feedback loop [11]. The importance of the decoupling discussed in the previous Section becomes obvious. The feedback loop on the primary side regulates against the input voltage variation, while the secondary side feedback loop regulates only against the load current changes, as shown in Fig. 2.6. Duty ratio waveforms sketched in the lower part of this figure qualitatively show variations of the two duty ratios. While the duty ratio D of the primary side switch varies over a wide range as the input voltage changes, the secondary side duty ratio D_1 has to make only minor adjustments as the load current changes. This is true as long as the converter operates in the continuous conduction mode.

It is important to note that the quantity to be regulated by the primary side loop is the sum of two energy transfer capacitor voltages, $V_P + V_S$, since this is, effectively, the power supply voltage presented to the output buck-like stage (equivalent to V in the nonisolated case). This could, possibly, pose a problem of sensing the secondary side capacitor voltage V_S by the primary side feedback. In principle, the sensing could be done in many different ways, but the very process of transferring a signal from the secondary to the primary side would involve isolation in the

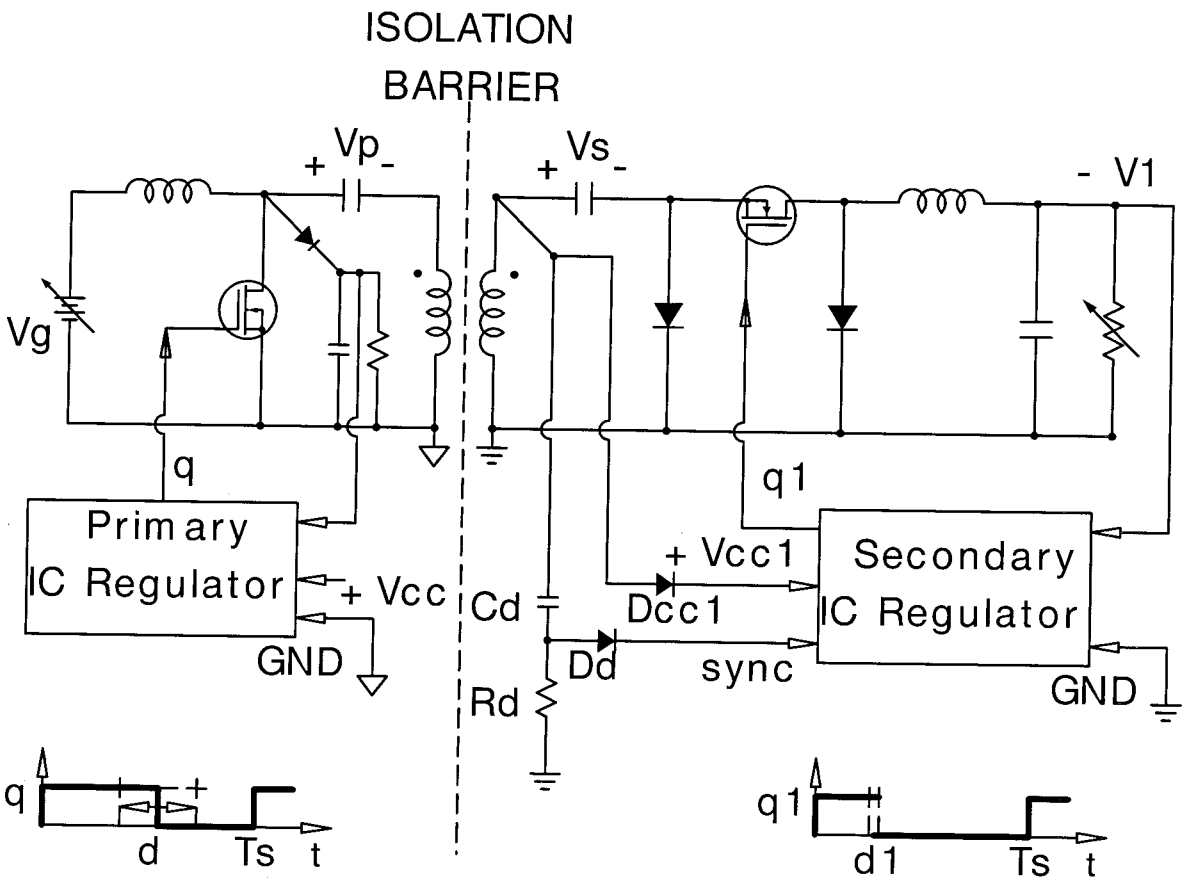


Figure 2.6: *Complete elimination of isolation in the feedback control circuitry.*

feedback circuitry. Fortunately, the voltage $V_P + V_S$ is available in a somewhat hidden form on the primary side. When the primary side transistor is OFF, its blocking voltage is equal to the sum of two energy transfer capacitor voltages. Hence, by sensing this OFF voltage, we obtain a sensed signal for the primary side feedback loop. Once again, this is accomplished entirely on the primary side, completely eliminating the need for isolation in the feedback circuitry and resulting in the same decoupled control described in the previous Section.

Sensing of the transistor OFF voltage on the primary side could be done in many different ways. Figure 2.6 shows one possible method where the transistor OFF voltage is rectified into a dc voltage using a simple peak-detector circuit. More accurate sensing could be done using a sampling scheme at the expense of increased circuit complexity.

Also shown in Fig. 2.6 is a C_d, R_d differentiating circuit for synchronization of the secondary side IC regulator. By differentiating a squarewave voltage on the secondary of the

isolation transformer and gating only positive pulses via signal diode D_d into the *sync* input of the secondary side IC regulator, synchronized operation of the two control circuits is provided.

Finally, the supply voltage to the secondary side IC regulator is provided by simply rectifying the voltage on the transformer secondary using the diode D_{CC1}. Thus, no separate housekeeping power supply is needed for the secondary side control circuitry and the absence of isolation transformers in the feedback is preserved.

2.4.1 Multiple Output Extensions

The presence of a controllable secondary side switch naturally leads to a multiple output extension of the Capacitive Idling Ćuk converter shown in Fig. 2.7. Note that each output has its own feedback providing no-load to full-load regulation. Another advantage of the Capacitive Idling Ćuk converter is that the secondary side switch is placed in series with the load. Hence, a short-circuit condition on one output of the converter of Fig. 2.7 does not shut down the whole converter to protect it. Instead, the active switch in the affected output is opened, enabling the other output(s) to continue to function and provide regulated voltage(s) to the load(s).

2.5 Decoupled Frequency Responses

Previous analysis has shown that the Capacitive Idling Ćuk converter eliminates the problem of feedback isolation and provides full regulation of multiple outputs in a single power stage. It is now interesting to determine if the frequency response of this fourth-order converter exhibits the same nonminimum phase response typically found in other fourth-order converters (Fig. 2.2).

In the approach of decoupled feedback loops described in Section 2.3, the primary side feedback prevents the input voltage changes from affecting the secondary side load regulation feedback loop. This means that the low frequency gain of the load regulation loop remains constant in the presence of input voltage changes. Load variations also have little effect on the steady-state value of the secondary side switch duty ratio D_1. The load regulation loop thus has relatively constant low frequency gain, an improvement over conventional switching regulators with a single control loop. It is, however, far more important to find out if the load regulation loop exhibits a minimum phase response (no RHP zeros) and to determine if its corner frequencies depend on the input voltage.

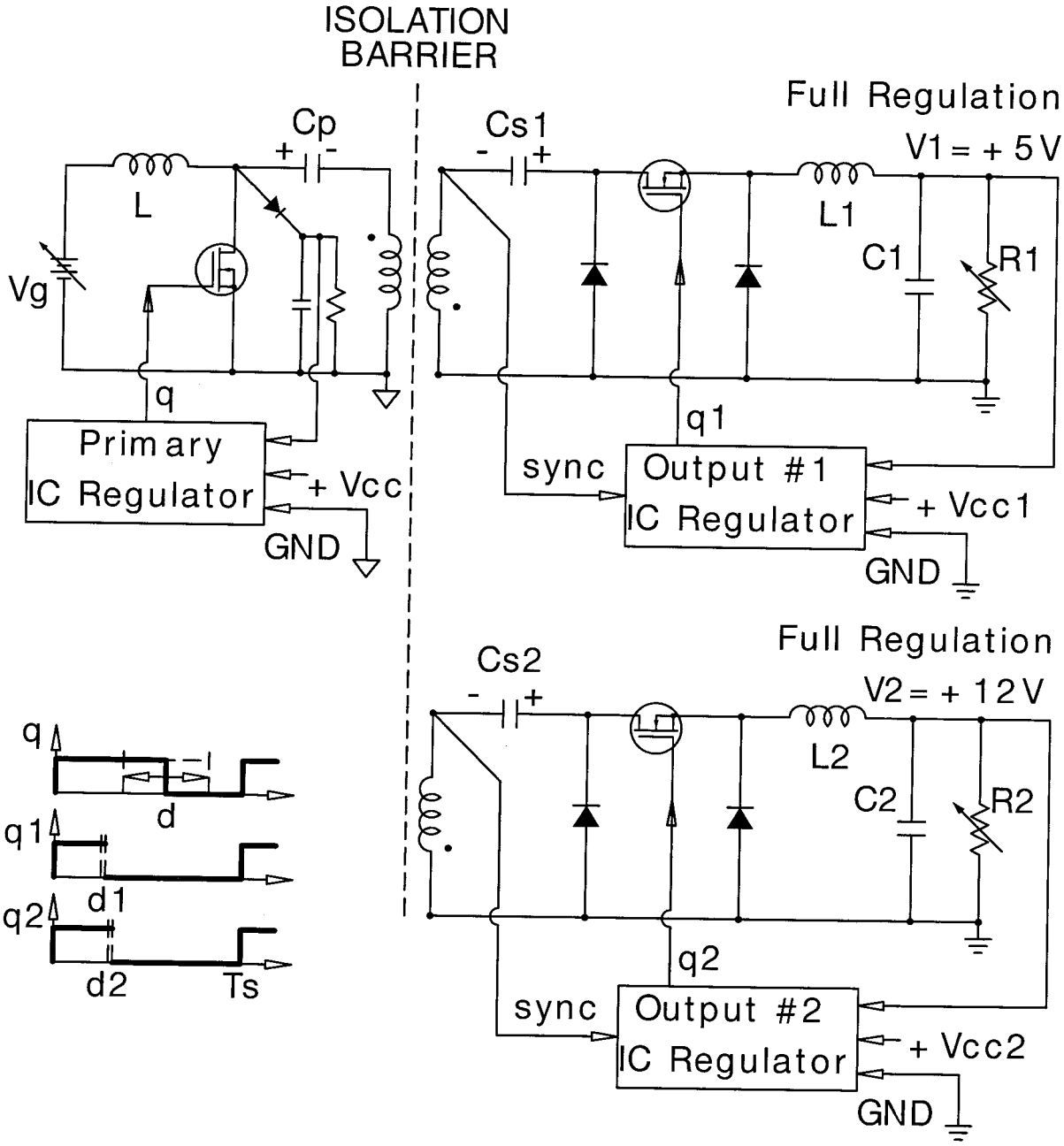


Figure 2.7: *Fully regulated multiple output voltages, no need for isolation in the feedback and independent short circuit protection of each output are key features of this regulator.*

Next, we show that under certain conditions this converter's frequency response decouples into a second-order load regulation transfer function with no RHP zeros and the second-order primary side transfer function featuring one RHP zero. We now proceed to derive analytical expressions for these two transfer functions and establish analytical criterion for the minimum

phase response of the load regulation loop.

It was demonstrated in [7] that the state space averaging technique [12] applies to the Three Switched Network converters as well. Based on the three linear time-invariant switched networks of Fig. 2.4, the averaged state equations for the Capacitive Idling Ćuk converter are:

$$\begin{aligned} L\frac{di}{dt} &= v_g - v(1-d) \\ L_1\frac{di_1}{dt} &= vd_1 - v_1 \\ C\frac{dv}{dt} &= i(1-d) - i_1 d_1 \\ C_1\frac{dv_1}{dt} &= i_1 - \frac{v_1}{R}\,. \end{aligned} \tag{2.8}$$

Perturbation and linearization yield:

$$\begin{vmatrix} sL & 0 & 1-D & 0 \\ 0 & sL_1 & -D_1 & 1 \\ -(1-D) & D_1 & sC & 0 \\ 0 & -1 & 0 & sC_1+\frac{1}{R} \end{vmatrix} \begin{vmatrix} \hat{i} \\ \hat{i}_1 \\ \hat{v} \\ \hat{v}_1 \end{vmatrix} = \begin{vmatrix} 1 \\ 0 \\ 0 \\ 0 \end{vmatrix} \hat{v}_g + \begin{vmatrix} V \\ 0 \\ -I \\ 0 \end{vmatrix} \hat{d} + \begin{vmatrix} 0 \\ V \\ -I_1 \\ 0 \end{vmatrix} \hat{d}_1\,. \tag{2.9}$$

Two transfer functions of key importance to the approach of the decoupled feedback loops are: $\hat{v}/\hat{d}$ and $\hat{v}_1/\hat{d}_1$. From (2) it follows that:

$$\frac{\hat{v}}{\hat{d}} = \frac{V}{1-D}\frac{\left(1-\frac{s}{\omega_{z1}}\right)}{\left[1+\frac{1}{Q_p}\frac{s}{\omega_p}+\left(\frac{s}{\omega_p}\right)^2\right]} \tag{2.10}$$

$$\frac{\hat{v_1}}{\hat{d_1}} = \frac{V_1}{D_1}\frac{1-\frac{1}{Q_z}\frac{s}{\omega_z}+\left(\frac{s}{\omega_z}\right)^2}{\left[1+\frac{1}{Q_p}\frac{s}{\omega_p}+\left(\frac{s}{\omega_p}\right)^2\right]\left[1+\frac{1}{Q_{p1}}\frac{s}{\omega_{p1}}+\left(\frac{s}{\omega_{p1}}\right)^2\right]} \tag{2.11}$$

where:

$$\begin{aligned} \omega_p = \omega_z &= \frac{1}{\sqrt{L_e C_e}}\,, & Q_p = Q_z &= R\sqrt{\frac{C_e}{L_e}} \\ \omega_{p1} &= \frac{1}{\sqrt{L_1 C_1}}, & Q_{p1} &= R\sqrt{\frac{C_1}{L_1}} \\ \omega_{z1} &= \frac{R}{L_e} \end{aligned} \tag{2.12}$$

and L_e, C_e are defined as:

$$L_e \equiv L\left(\frac{D_1}{1-D}\right)^2, \qquad C_e \equiv \frac{C}{D_1^2}\,. \tag{2.13}$$

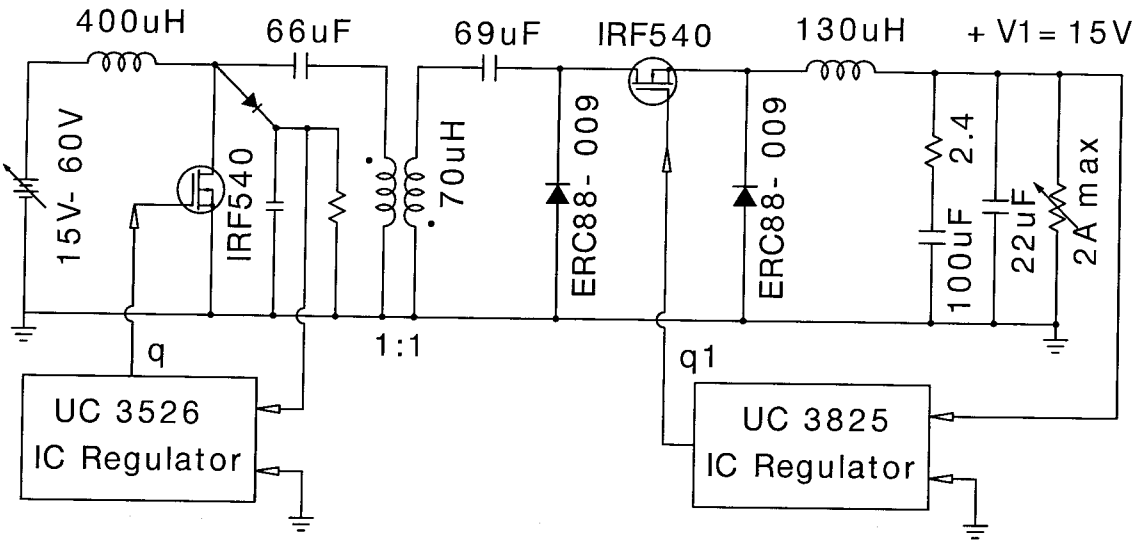


Figure 2.8: *Experimental circuit featuring isolated Capacitive Idling Ćuk converter.*

Examination of (2.11) and (2.12) reveals that the load regulation loop of the Capacitive Idling Ćuk converter has a double pole ω_p and a double RHP zero ω_z at the frequency $1/\left(2\pi\sqrt{L_eC_e}\right)$. The other double pole ω_{p1} is at the output filter corner frequency $1/\left(2\pi\sqrt{L_1C_1}\right)$. This means that the $\hat{v}_1/\hat{d}_1$ transfer function exhibits a nonminimum phase frequency response with 540° total phase lag.

However, frequency response measurements performed on the experimental circuit of Fig. 2.8 showed no RHP zeros in the $\hat{v}_1/\hat{d}_1$ frequency response, suggesting that nonidealities play an important role in determining the nature of ω_z. This was confirmed by state-space averaging analysis of the converter with two parasitic resistances included: R_l of the input inductor L and R_{l1} of the output inductor L_1. The modified expression for the numerator of the $\hat{v}_1/\hat{d}_1$ transfer function is:

$$N(s) = 1 + \frac{(R_{l1} - R_{le})}{R} + \left[\left(1 + \frac{R_{l1}}{R}\right)R_{le}C_e - \frac{L_e}{R}\right]s + \left(1 + \frac{R_{l1}}{R}\right)L_eC_es^2 \qquad (2.14)$$

where $R_{le} \equiv R_l(D_1/1-D)^2$. It can be seen from (2.14) that in the presence of the parasitic resistances R_l and R_{l1}, zeros of the $N(s)$ can move to the LHP if the inequality

$$D_1^2 < \frac{\frac{R}{\sqrt{L/C}}}{\frac{\sqrt{L/C}}{(1+R_{l1}/R)R_l}} \qquad (2.15)$$

is satisfied. For any reasonably efficient switching converter, power delivered to the load RI_1^2 is much greater than the power dissipated in the parasitic resistance of the output inductor $R_{l1}I_1^2$,

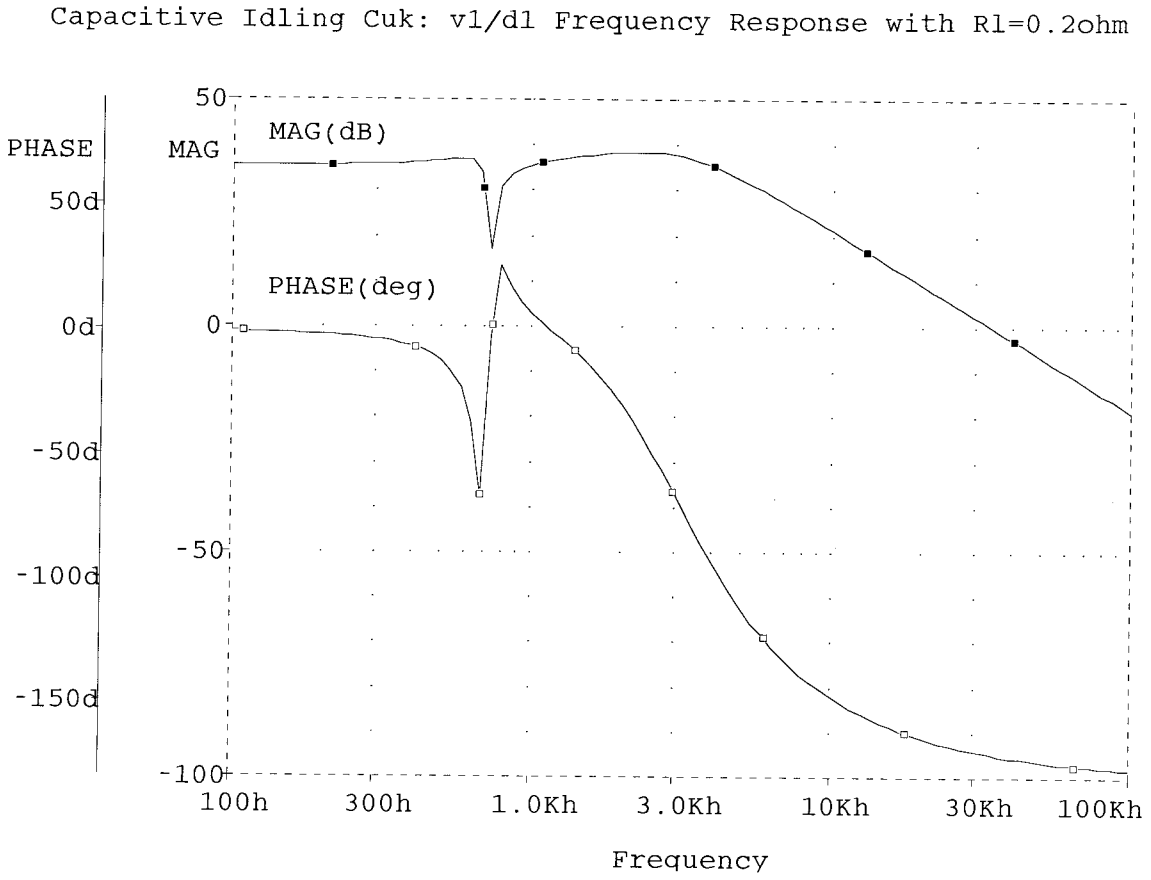


Figure 2.9: *Almost complete decoupling of the two feedback loops:* $\hat{v}_1/\hat{d}_1$ *frequency response.*

leading to the following approximation: $1 + R_{l1}/R \approx 1$. In this case the inequality (2.15) becomes:

$$D_1^2 < \frac{Q_{load}}{Q_{paras}} \tag{2.16}$$

with the load quality factor Q_{load} and the parasitics quality factor Q_{paras} defined as follows:

$$Q_{load} \equiv \frac{R}{\sqrt{L/C}}, \qquad Q_{paras} \equiv \frac{\sqrt{L/C}}{R_l}. \tag{2.17}$$

From (2.16) we can see that the converter has a pair of LHP zeros for any operating point D_1 if $Q_{paras} < Q_{load}$. In that case (2.11) becomes effectively a second-order transfer function of the buck converter:

$$\frac{\hat{v}_1}{\hat{d}_1} \approx \frac{V_1}{D_1} \frac{1}{1 + \frac{1}{Q_{p1}}\frac{s}{\omega_{p1}} + \left(\frac{s}{\omega_{p1}}\right)^2}. \tag{2.18}$$

This result can be verified on the experimental Capacitive Idling Ćuk converter of Fig. 2.8. Upon substitution of component values shown in Fig. 2.8 (including value of the parasitic resistance $R_l = 0.2\Omega$) in the inequality (2.16), we determine that the operating region where converter has LHP zeros is restricted to $D_1 < 0.35$. Since our converter has a nominal operating point $D_1 = V_1/V = 15V/75V = 0.2$, we conclude that it's zeros remain in the LHP for any line and load condition.

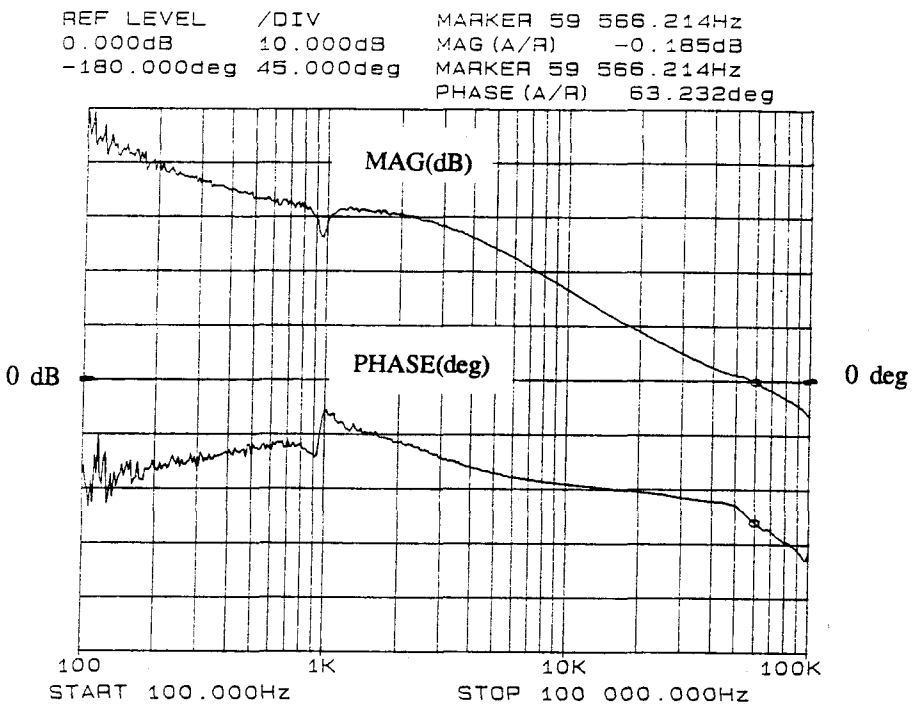
Figure 2.9 shows Spice [13] simulation of the $\hat{v_1}/\hat{d_1}$ transfer function of the converter described in Fig. 2.8. As expected, both zeros are in the LHP, while the glitch in both magnitude and phase plots of Fig. 2.9 indicates that the pole-zero cancelation in (2.11) is not perfect.

It is obvious from (2.10) and (2.18) that the approach of decoupled feedback loops has effectively decomposed the original fourth-order system into two well-behaved second-order subsystems. Moreover, the two second-order systems may be further optimized to improve overall converter dynamics and obtain a fast transient response which was not possible in the original fourth-order system. Improvement in the frequency response can be achieved by using current-mode programming or a lossless power filter damping network [9] on the secondary side. This would make the load regulation loop effectively a first-order system with a dominant low-frequency pole and essentially a 90° phase margin.

Also, the control method for the primary side feedback loop is not restricted to duty-ratio programming. Although it is not critical to achieve a wide bandwidth loop-gain of the primary side feedback, other control methods could result in better frequency response of this control loop. It is interesting to point out that the so-called feed-forward technique, known to be effective in rejecting the input voltage variations in the buck converter, is not as effective in the boost converter [14]. This means that use of feed-forward cannot achieve good results in the Capacitive Idling Ćuk converter with its boost-type primary side.

2.6 Experimental Results

Transient response measurements were performed on the experimental circuit of Fig. 2.8, operating at a 200 kilohertz switching frequency. A wide bandwidth loop gain was designed with the crossover frequency at 60 kilohertz (Fig. 2.10(a)). Since the input voltage to the buck-like regulator is constant, the frequency response is effectively unchanged for all load currents



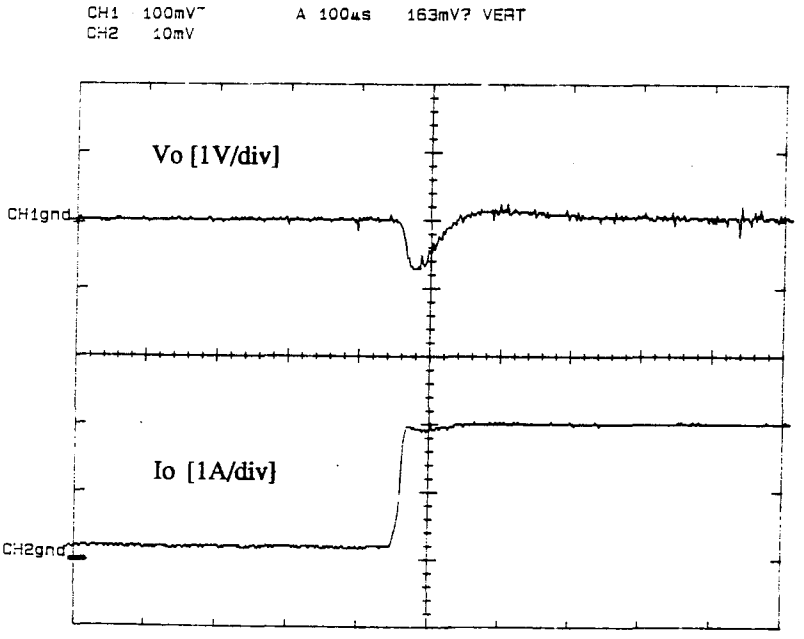


Figure 2.10: The experimental Capacitive Idling Ćuk converter switching at 200 kHz exhibits a superior 60 kHz bandwidth of the load regulation loop (a) under all operating conditions, resulting in the fast transient response (b).

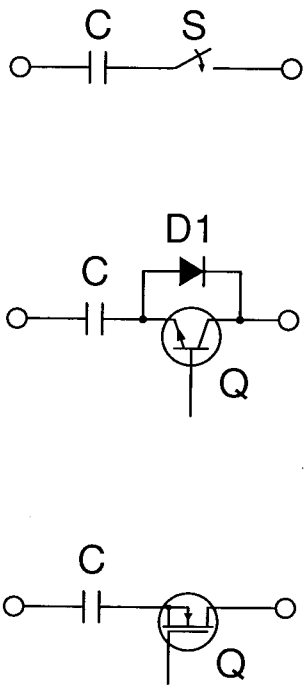


Figure 2.11: Current bidirectional switch in series with the energy transfer capacitor C.

and input voltage variations and the bandwidth is constant at 60 kilohertz. The response to an 1.8 ampere step load current (10%-100% load) is shown in Fig. 2.10(b), with output voltage overshoot of 5% and a remarkably short recovery time of only 100 microseconds.

The benefits of decoupled feedback loops can now be fully appreciated. To achieve this wide a bandwidth in the original fourth-order system operating at the same switching frequency would be impossible. For all practical purposes, the bandwidth of the fourth-order system is limited to only a small fraction of switching frequency, usually between $1/30$ to $1/100$ of the switching frequency. For a 200 kilohertz converter, this translates into a 2 kilohertz to 6 kilohertz crossover frequency. An order of magnitude lower bandwidth would clearly result in correspondingly worse transient response. To cure this problem, one would have to increase the size of the output capacitance at least 10 times, making the converter bigger and more expensive.

2.7 Generalization: A New Class of Capacitive Idling Converters

Described advantages of the Capacitive Idling Ćuk converter have motivated the search for other Capacitive Idling converters. The new class of converters is generated by inserting a current bidirectional switch in a branch of the energy transfer capacitor of a parent PWM converter (Fig.

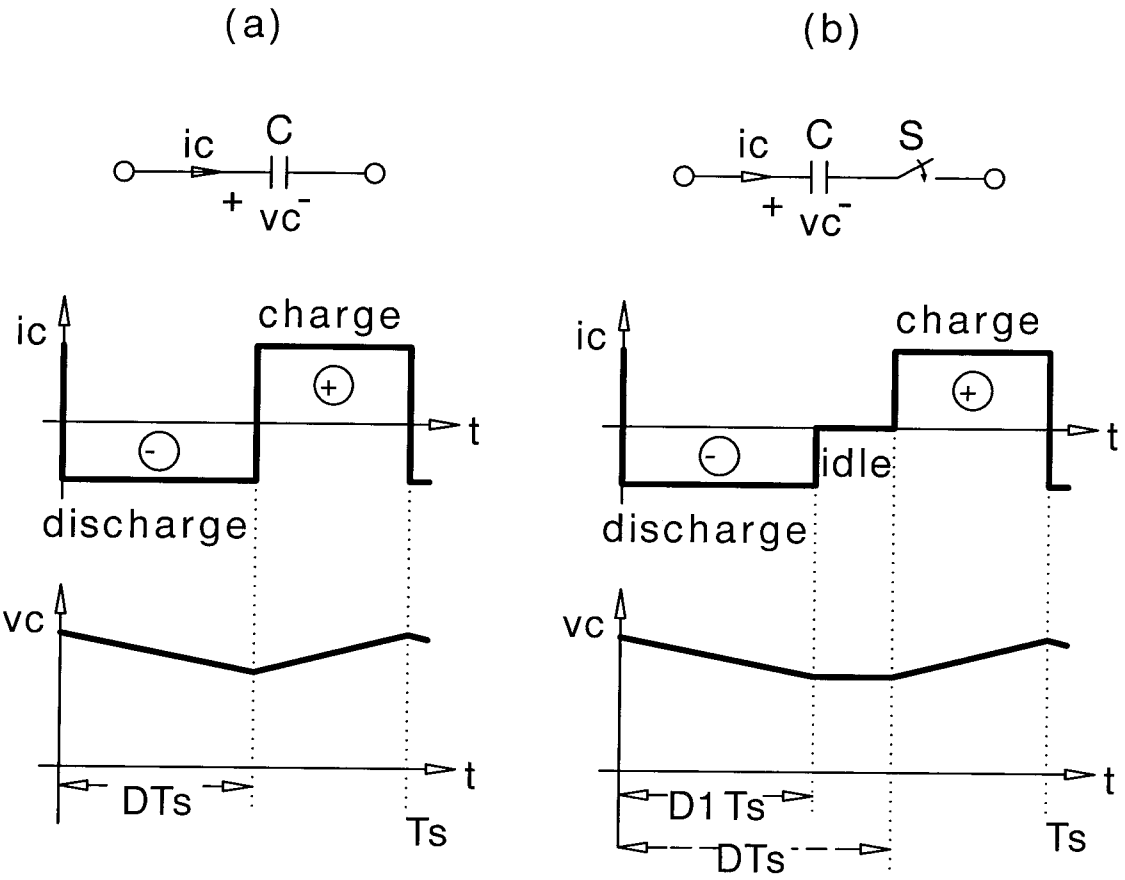


Figure 2.12: *Insertion of the current bidirectional switch in series with the energy transfer capacitor C of any basic converter (a) introduces the idling interval (b).*

2.11). By energy transfer capacitor we mean a capacitor whose idealized current waveform is a squarewave with distinct charge and discharge intervals, such as that shown in Fig. 2.12(a). Figure 2.12(b) shows waveforms of the energy transfer capacitor after insertion of the current bidirectional switch. In addition to charging and discharging intervals, a new idling interval is introduced, during which the switch S is open and the capacitor current is zero.

This synthesis procedure is carried out with the specific goal of generating Capacitive Idling switching converters that exhibit advantages similar to those found in the Capacitive Idling Ćuk converter. In order to uncover only those Capacitive Idling converters that are practically useful in multiple output applications, the parent PWM converters are selected according to the following requirements:

— existence of a practical isolated version,

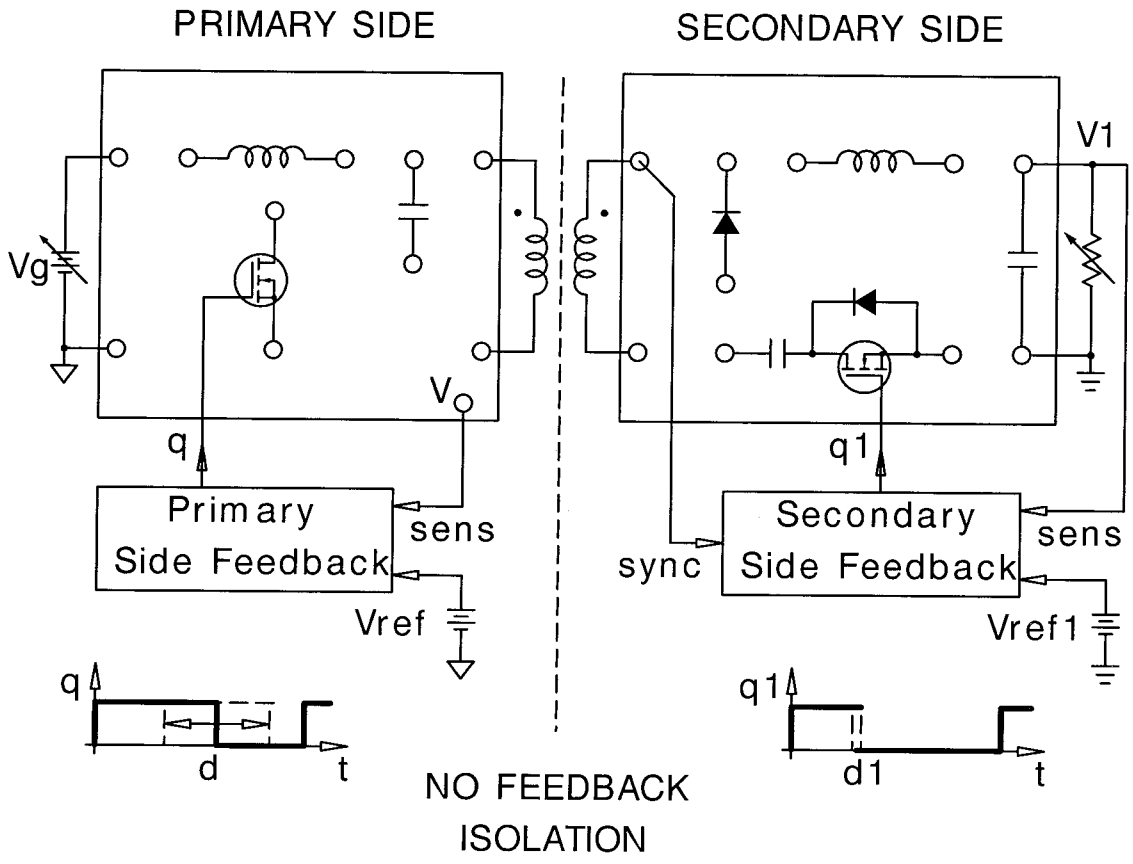


Figure 2.13: *General block diagram representation of the Capacitive Idling converters that satisfy a prescribed set of properties.*

— existence of the energy transfer capacitor on the secondary side and

— possibility for decoupling in the dc conversion ratio and appropriate sensing.

Figure 2.13 shows a generic Capacitive Idling converter satisfying this set of requirements. Based on these requirements, the synthesis of Capacitive Idling converters is performed. Figure 2.14 shows Capacitive Idling converters derived from the isolated versions of the three PWM parent converters: Inverse SEPIC, SEPIC and flyback. Capacitive Idling topologies with the current bidirectional switch implementation are shown in row (b) of Fig. 2.14, and row (c) shows their alternative switch implementation. For all six Capacitive Idling converters of Fig. 2.14 there exists an appropriate sensing method that leads to the decoupled feedbacks. Also, an independent short circuit protection on each output is possible in all converters of Fig. 2.14.

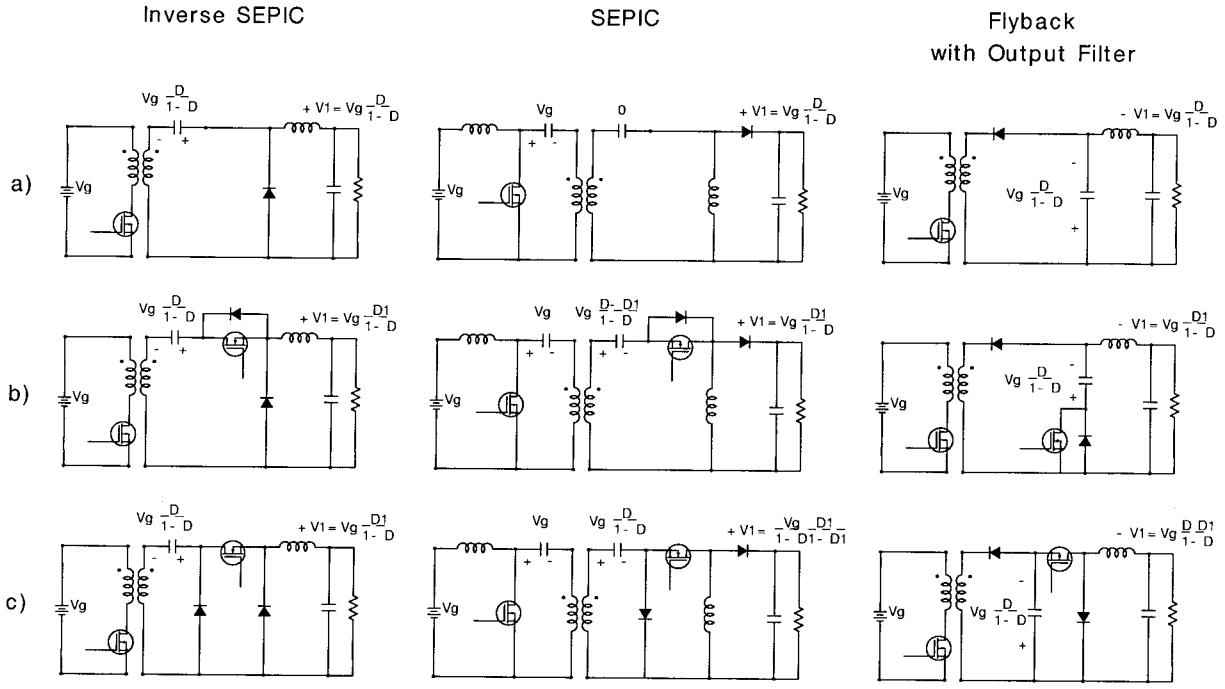


Figure 2.14: *Three basic isolated converters featuring energy transfer capacitor on the secondary side (a) and their respective Capacitive Idling extensions (b) and (c).*

2.8 Conclusions

A novel class of isolated Capacitive Idling converters featuring decoupled primary and secondary side feedback loops possesses following advantages over conventional converters:

1. Elimination of the need to cross the isolation barrier in the feedback control path.

2. Full regulation of multiple outputs in a single power processing stage.

3. Separation of the conventional feedback loop into two independent feedbacks: input voltage regulation and output load regulation loops, resulting in a wide bandwidth of the load regulation feedback loop, and consequently fast transient response.

4. Independent short circuit protection of each output.

Disadvantages of Capacitive Idling converters with respect to their PWM parent converters are: higher voltage stress and slightly lower efficiency owing to the losses incurred in the additional active switches. However, these disadvantages are far outweighed by the described advantages of the new converter class.

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Chapter 3
Input Current Shaping and Regulation of Multiple Outputs in a Single Isolated Converter

Abstract — **Input current shaping and wide bandwidth regulation of multiple outputs is demonstrated in a single power stage. These isolated Capacitive Idling converters, when operated in discontinuous inductor current mode (DICM) on the primary side, perform input current shaping automatically, i.e., without an input current feedback loop. Consequently, the high power factor performance is obtained without any penalty in complexity, cost and efficiency of the converter. Moreover, due to the internal energy storage and presence of one secondary-side active switch for each output, the Capacitive Idling converters provide full regulation and short-circuit protection of all outputs, and eliminate the need to cross the isolation barrier in the feedback path.**

3.1 Introduction

Some recent international regulations governing the amount of harmonic currents polluting the utility line, such as IEC 555-2 [1], require addition of the input current shaping feature to practically all single-phase electronic equipment. The conventional solution is to use the front-end switching converter to perform input current shaping, followed by an isolated downstream converter providing regulated output voltage. This additional front-end power stage increases the size and weight of the power supply and reduces the overall conversion efficiency. The situation is even worse when there is a need for several fully regulated output voltages, in which case a separate post-regulator is added for each auxiliary output.

This paper describes a new class of isolated converters that can perform both input current shaping and wide bandwidth regulation of multiple outputs in a single power stage. The analysis is focused on four prominent members of the Capacitive Idling (CI) converter class: CI inverse SEPIC, CI flyback, CI Ćuk, and CI SEPIC.

In Section 3.2, topology requirements for input current shaping and load regulation are examined. Dc-to-dc mode of operation of the CI converters is reviewed in Section 3.3, with

emphasis on decoupled primary and secondary side feedback loops. All three discontinuous inductor current modes (DICM) that are possible in these converters are identified in Section 3.4. The analysis of this Section is focused on one particular discontinuous mode where the primary side inductor current is discontinuous, while the output inductor current is continuous. In Section 3.5 the expressions for power factor and DICM boundary in ac-to-dc mode of operation are derived. Section 3.6 presents experimental results that illustrate the concept and verify the analysis. The principal conclusions are discussed in Section 3.7.

3.2 Topology Requirements for Input Current Shaping and Load Regulation

The generalized representation of an ac-to-dc converter in Fig. 3.1 shows the input terminals of the converter connected to a voltage source v_g. This source is the line voltage rectified by a bridge rectifier. The line voltage is a sinusoidal waveform with period $T_L = 2\pi/\omega$, which makes the voltage waveform on the load side of the bridge rectifier:

$$v_g(\omega t) = V_g|\sin(\omega t)| \; . \tag{3.1}$$

The ac-to-dc converter of Fig. 3.1 must perform three functions:

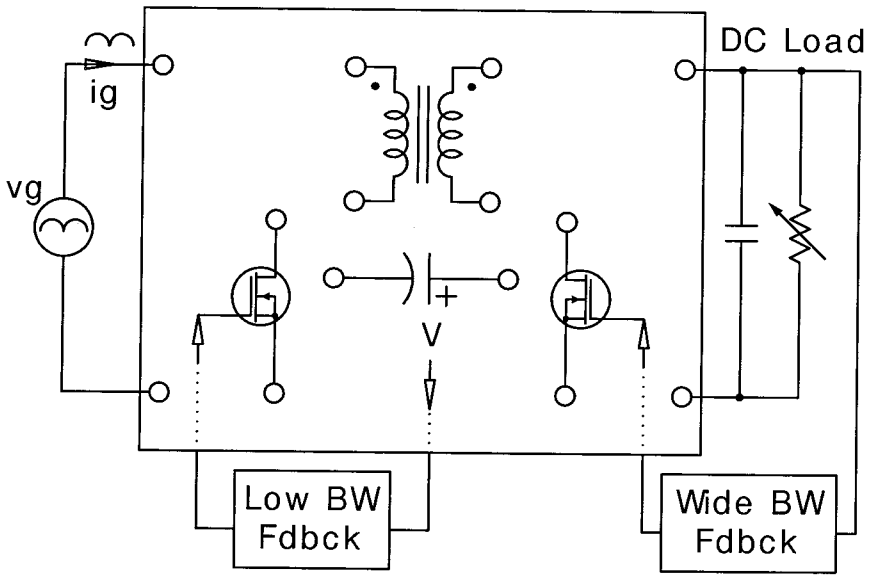

Figure 3.1: Generalized representation of an ac-to-dc converter performing input current shaping and output voltage regulation.

First, provide high power factor at the input. This means that the input current needs to have a low harmonic content and small displacement angle. In the case of sinewave input voltage, an in-phase sinusoidal current is most desirable, resulting in unity power factor and input power that is a time-varying function of the line frequency:

$$p_{in}(\omega t) = V_g I_g \sin^2(\omega t) \ . \tag{3.2}$$

On the output side, the dc load draws a dc output power:

$$P_{out} = V_{out} I_{out} = \frac{V_{out}^2}{R} \ . \tag{3.3}$$

This means that the current shaper must provide balance between the time-varying input and constant output power - store some energy internally.

Thus, the second requirement for the input current shaper in Fig. 3.1 is internal energy storage. For reasons of higher energy density, capacitive energy storage is preferred to inductive storage in most practical applications. The internal energy storage requirement means that the converter needs to have an internal storage component (capacitor that is not connected directly to a pair of external terminals). The difference between the instantaneous input and output power will cause the energy level in this component to fluctuate at the line frequency. It is even acceptable for the voltage of the energy storage capacitor to have large line frequency ripple, as long as the amount of stored energy is sufficient for proper operation of the converter throughout the line cycle. In terms of the peak energy stored in the energy storage capacitor at some point of each line cycle, the energy storage requirement is [2]:

$$U_{peak} \geq \frac{P_{out}}{\omega} \ . \tag{3.4}$$

It is important to note that the peak of the stored energy depends on the output power and the line frequency ω, and is independent of the switching frequency. This is different from the scaling of all other reactive components in the converter, whose size is dependent on the switching frequency.

Third, the converter needs to regulate the output voltage, possibly multiple output voltages. Strictly speaking, an ac-to-dc converter with one control variable cannot regulate the output voltage without a detrimental effect on the input current wave-shape. If the crossover frequency of the load regulation loop is higher than the line frequency, perturbations in this loop (for

instance a step-load change at the output) will affect the shape of the input current within one line period. Consequently, converter topologies with more than one control variable are needed in applications requiring wide bandwidth input current shaping and load regulation [2–4]. However, it was shown recently that a new family of ac-to-dc converters with a single control variable and an internal energy storage, can regulate the output voltage without significant input current distortion [5].

In shapers where regulation of multiple outputs is required, other approaches are needed. The addition of at least one control variable is necessary for each additional output. This can be done by placing a post-regulator at each auxiliary output. The penalty in this straightforward approach is in terms of cost, size and efficiency. An alternative approach is to use converter topologies with more than one control variable.

3.3 Capacitive Idling Converters

One such class of switching converters is the Capacitive Idling (CI) converters [6]. Figure 3.2 shows four prominent members of this new class of isolated converters. It was previously established [6] that this converter class exhibits several advantages in applications requiring isolation and regulation of multiple outputs. Namely, feedback implementation in these converters is considerably simplified because there is no need to transfer the feedback signal across the isolation barrier. Second, full regulation and shut-down protection of all outputs is provided in multiple output applications. Finally, owing to the feedback decoupling, these converters exhibit significantly improved frequency response, resulting in a wide bandwidth of the load regulation loop.

The control scheme for the dc-to-dc CI converters is based on the concept of decoupled feedback loops, described in [6]. In this approach, converter control is separated between the primary side feedback loop and the secondary side feedback loop, eliminating the need to cross the isolation barrier in the feedback path. This is illustrated on the example of the CI inverse SEPIC converter shown in Fig. 3.3, with primary and secondary control circuits separated by the isolation barrier. Note the independent duty ratio controls q and q_1 of the two active switches Q and Q_1. In this figure, the secondary side feedback regulates the output voltage V_1 by controlling the duty ratio d_1 of the secondary side transistor Q_1, while the primary side feedback loop

prevents the line voltage changes from affecting the duty ratio of the secondary side switch Q_1. The primary side feedback pre-regulates the OFF voltage $V + V_g$ of the primary side transistor Q, and the sensing is accomplished entirely on the primary side, eliminating the need for isolation in the feedback circuitry.

Duty ratio waveforms sketched in the lower part of Fig. 3.3 qualitatively show perturbations in the two feedback loops. While the duty ratio d of the primary side switch varies over a wide range as the input voltage changes, small variations in the secondary side duty ratio d_1 are caused essentially by load current changes only. This results in nearly constant crossover frequency and wide bandwidth of the load regulation feedback loop.

More important, the presence of independent primary and secondary side controls makes possible both input current shaping and wide bandwidth regulation of multiple outputs in a single power converter. Here, two different approaches can be used.

One is to implement on the primary side a fast input current feedback loop that would force an average input current to follow the rectified line voltage and result in unity power factor performance. Although the additional current loop makes the primary control circuit more complicated, the power stage is the same as that in Fig. 3.3, making this approach more efficient than the conventional.

The second approach is to operate the CI converter in discontinuous inductor current mode (DICM) at constant switching frequency and with constant duty ratio of the primary side switch Q. Here, the converter performs the input current shaping automatically, without the input current feedback loop, and is referred to as the "automatic" current shaper [2]. The advantage of this approach is that the input current shaping feature is obtained without changing the basic dc-to-dc CI converter. This special mode of operation results in high power factor performance without any penalty in complexity, size and efficiency of the converter.

In the remaining sections of this paper, discussion will be focussed on the latter method of providing high input power factor, the so-called automatic current shaping.

3.4 Dc-to-Dc Capacitive Idling Converters in DICM

This section deals with the analysis of dc-to-dc CI converters operating in DICM. Derivation of key results and full understanding of operation of these converters in dc-to-dc mode, will make

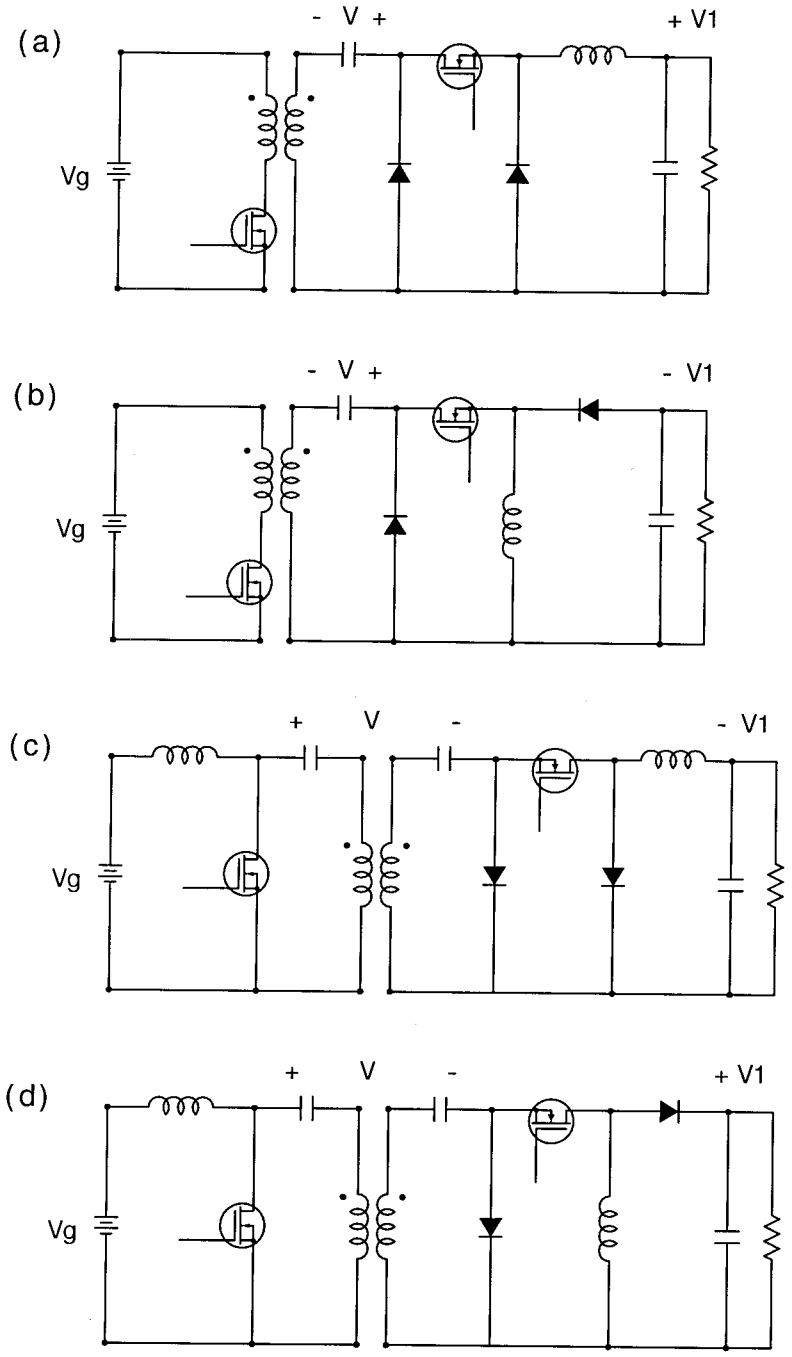

Figure 3.2: *Four isolated dc-to-dc converters suitable for input current shaping and wide bandwidth load regulation: Capacitive Idling inverse SEPIC (a), flyback (b), Ćuk (c), and SEPIC (d).*

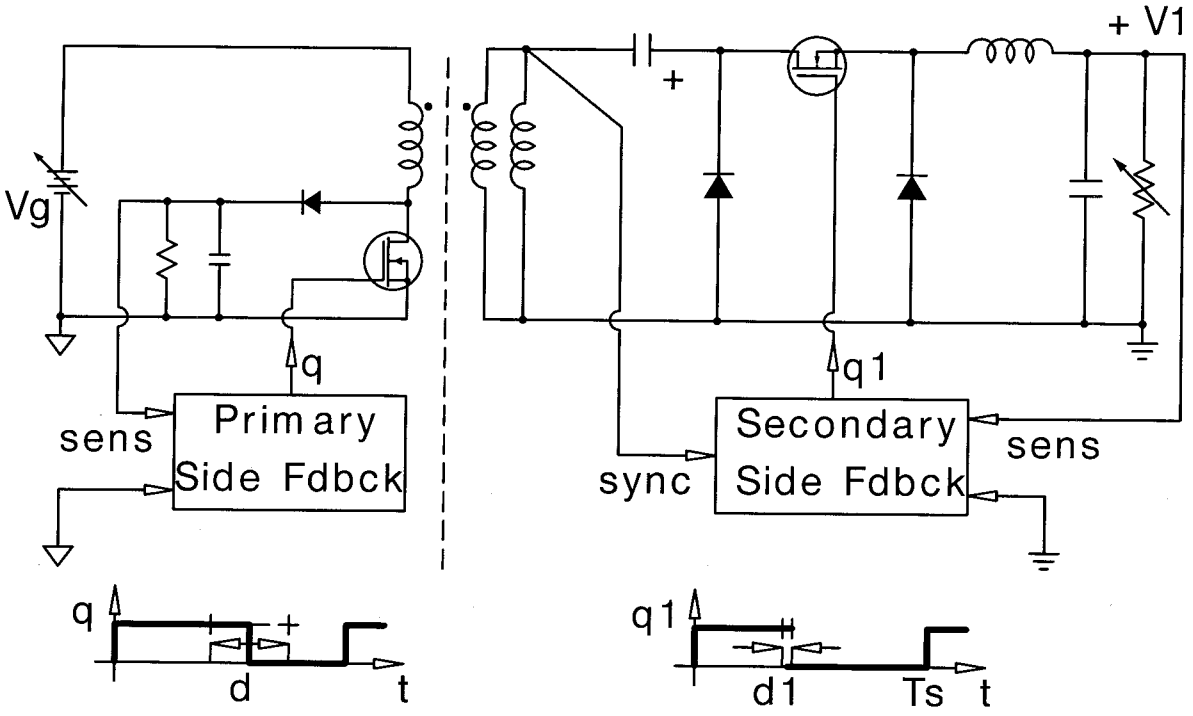

Figure 3.3: *Isolation barrier completely separates the feedback of the isolated Capacitive Idling inverse SEPIC converter to the primary and secondary side control loops.*

possible analysis and design of CI converters operating as both input current shaper and regulator.

3.4.1 Discontinuous Modes

It is well known that the unidirectional nature of the diode switch is responsible for the onset of the discontinuous inductor current mode [7]. Because of the presence of two passive switches, D and D_1, in each CI converter shown in Fig. 3.2, multiple discontinuous modes are possible. Depending on the type of discontinuous mode, the converter will exhibit drastically different behavior when operated as an ac-to-dc regulator. In this Section, all three possible DICM modes will be identified, but the analysis will focus only on one discontinuous mode.

Consider, as an example, the CI inverse SEPIC converter in Fig. 3.4. Converter operation in the continuous conduction mode (CCM) can be described by the periodic sequence of three linear, time-invariant networks:

Diode D is turned ON and OFF in synchronism with transistor Q, while the diode D_1 is synchronized with Q_1 (diode D is ON when transistor Q is OFF, and vice versa).

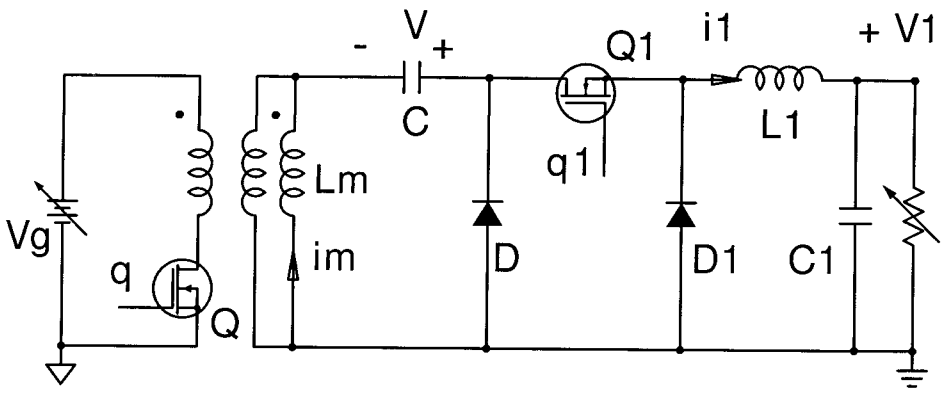

Figure 3.4: *Isolated Capacitive Idling inverse SEPIC converter.*

In this mode of operation, the CI inverse SEPIC converter in Fig. 3.4 has a dc voltage gain:

$$M_1(D, D_1) \equiv \frac{V_1}{V_g} = \frac{D_1}{1-D} \cdot \tag{3.5}$$

The other dc voltage gain is given by:

$$M(D) \equiv \frac{V}{V_g} = \frac{D}{1-D} \cdot \tag{3.6}$$

This converter will remain in CCM as long as the small-ripple assumption is satisfied for all inductor currents and capacitor voltages. This means that inductor currents and capacitor voltages are dc quantities, with relatively small ac ripple. Once the small ripple assumption is removed, the converter can enter different discontinuous modes [8].

Here, it is assumed that all capacitor voltages are dc quantities, restricting the analysis to various DICM only. Suppose that the small-ripple assumption is removed from the output inductor L_1 in Fig. 3.4. If the inductor current i_1 reduces to zero before the end of the third interval, diode D_1 will cease to conduct.

On the other hand, if the small ripple assumption is removed from the magnetizing inductance L_m, the magnetizing current i_m may become zero before the end of the third interval, and diode D will stop conducting.

Finally, both inductors can have a large ac ripple and both diodes D and D_1 can stop conducting before the end of the switching cycle.

Only the last two discontinuous modes can result in the high power factor ac-to-dc regulation. This analysis will focus on DICM where the magnetizing current i_m is discontinuous, and the output inductor current is continuous with a small switching ripple.

3.4.2 Dc Analysis in DICM

Figure 3.5 shows key waveforms and four linear time-invariant networks that characterize the CI inverse SEPIC converter of Fig. 3.4 operating in this discontinuous mode. Note that the output current is still continuous with a relatively small switching ripple. The steady-state analysis of this converter is now carried out.

Application of volt-second balance on the two inductors yields:

$$\frac{V}{V_g} = \frac{D}{D_2} \tag{3.7}$$

$$\frac{V_1}{V + V_g} = D_1 \, . \tag{3.8}$$

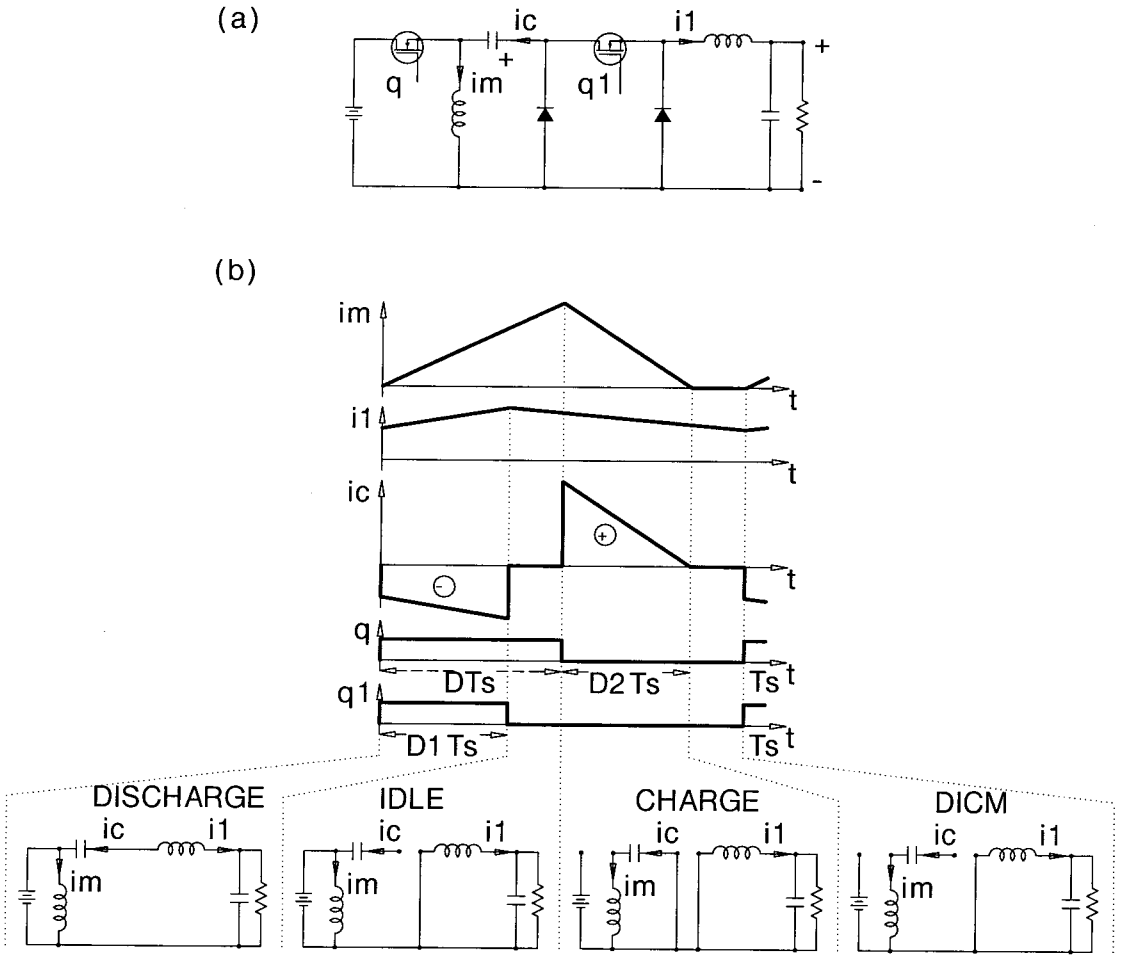

Figure 3.5: *Key switching waveforms of the Capacitive Idling inverse SEPIC converter of Fig. 3.4. Also shown are four linear, time-invariant networks, with DICM denoting the converter state reached after the inductor current i_m has reached zero level and the diode D ceased to conduct.*

Use of charge-balance on the energy transfer capacitor C leads to:

$$I_1 D_1 = \frac{V_g D T_s}{2L} D_2 \,. \tag{3.9}$$

By use of $V_1 = I_1 R$ in (3.8), the length of the interval $D_2 T_s$ can be determined from (3.8) and (3.9) as:

$$D_2 = \frac{K_e}{D} \cdot \frac{(V + V_g)}{V_g} \tag{3.10}$$

where K_e represents the dimensionless equivalent parameter which lumps together circuit parameters responsible for the discontinuous conduction mode. It is defined as:

$$K_e \equiv \frac{2L_e}{T_s R_i} \tag{3.11}$$

where $L_e = L_m$ in the CI inverse SEPIC converter. Also, R_i represents the effective dc loading to the front stage. In the case of the CI inverse SEPIC and Ćuk converters, the output stage has a buck-like transfer function, thus $R_i = R/D_1^2$. In the other two converters, the output stage is buck-boost, resulting in $R_i = R(1 - D_1)^2/D_1^2$. Substitution of (3.10) in (3.7) yields:

$$\frac{V_g}{V} = \frac{K_e}{D^2}\left(\frac{V}{V_g} + 1\right) . \tag{3.12}$$

The solution of this equation is:

$$M = \frac{V}{V_g} = \frac{-1 + \sqrt{1 + 4D^2/K_e}}{2} \,. \tag{3.13}$$

Like the dc gain of all basic converters operating in DICM, the dc gain M of the converter in Fig. 3.5 is a function only of the effective parameter K_e and the duty ratio D.

The overall conversion ratio M_1 is:

$$M_1 = D_1(M + 1) \,. \tag{3.14}$$

Following the same procedure, the dc transfer functions M and M_1 can be derived for the other three CI converters described in Fig. 3.2. The results are summarized in Table 3.1.

According to Table 3.1, values of M for the CI Ćuk and SEPIC converters are identical to the dc voltage gain of the DICM boost converter [7]. This is not surprising, because the dc gain

Table 3.1: *DC transfer functions of the converters shown in Fig. 3.2, with primary side operating in DICM.*

converter	$M(D,K_e)\equiv\frac{V}{V_g}$	$M_1(D_1,M)\equiv\frac{V_1}{V_g}$
CI inverse SEPIC	$\frac{-1+\sqrt{1+4D^2/K_e}}{2}$	$D_1\cdot(M+1)$
CI flyback	$\frac{-1+\sqrt{1+4D^2/K_e}}{2}$	$\frac{D_1}{1-D_1}\cdot(M+1)$
CI Ćuk	$\frac{1+\sqrt{1+4D^2/K_e}}{2}$	$D_1\cdot M$
CI SEPIC	$\frac{1+\sqrt{1+4D^2/K_e}}{2}$	$\frac{D_1}{1-D_1}\cdot M$

M of all three converters is identical in CCM as well. Table 3.1 also shows that the CI inverse SEPIC and flyback converters have the same dc gain M, which is also true for the CCM.

The boundary between DICM and CCM can be determined by evaluating the duration of the D_2T_s interval, labelled as 'charge' interval in Fig. 3.5.

Comparison between (3.7) and (3.13) yields:

$$D_2=\frac{K_e}{D}\cdot\frac{1+\sqrt{1+4D^2/K_e}}{2}\,. \tag{3.15}$$

The CI inverse SEPIC converter will operate in the DICM as long as:

$$D_2<1-D\,. \tag{3.16}$$

At the boundary between DICM and CCM $D_2=1-D$ and the equivalent parameter K_e attains its critical value:

$$K_c=D(1-D)^2\,. \tag{3.17}$$

Therefore, the operation in DICM is guaranteed by the following inequality:

$$K_e<K_c \tag{3.18}$$

and in the CCM otherwise. Values of the critical parameter for the other three converters are also given by the equation (3.17).

Table 3.2: *Critical value of the equivalent parameter Ke determines the boundary between the two conduction modes.*

converter	$K_c(D)$	$K_c(\gamma)$
all CI converters	$D(1-D)^2$	$\frac{\gamma-1}{\gamma^3}$

The critical parameter K_c can also be expressed as a function of γ, defined as the normalized switch voltage stress:

$$\gamma \equiv \frac{V_{off}}{V_g} \tag{3.19}$$

where V_{off} denotes the switch OFF voltage. In the case of the CI inverse SEPIC, the switch voltage stress is $V_{off} = V + V_g$ and $\gamma = 1 + M$. Substitution of (3.6) (dc transfer function M evaluated at the boundary between CCM and DICM) and (3.19) in (3.17) yields:

$$K_c(\gamma) = \frac{\gamma - 1}{\gamma^3} \cdot \tag{3.20}$$

Table 3.2 summarizes values of K_c for all four converters.

3.5 Current Shaping and Regulation

Attention is now turned to the analysis of CI converters in input current shaping applications. Results of the previous Section will be used to describe this relatively more complicated mode of operation.

Figure 3.6(a) shows the CI inverse SEPIC converter operating in the DICM. As described in Section 3.2, input current shaping and regulation require that the energy storage capacitor be placed internally. The only choice in the converter of Fig. 3.6(a) is to use capacitor C for the energy storage component.

The following assumptions are used in the analysis of the CI current shapers and regulators:

— input voltage is a perfect rectified sinewave,

— output is a regulated dc voltage V_1,

— dc voltage V of the energy storage capacitor C has no ac ripple,

— a 1:1 transformer turns ratio is assumed.

It is also assumed that the converter switching frequency f_s is much higher than the line frequency f_L.

Next, we derive the analytical expressions for the input current and the power factor, as well as the discontinuous mode boundary for the CI inverse SEPIC converter of Fig. 3.6.

3.5.1 Input Current Quality

Denote $\theta = \omega t$, so that the rectified input voltage is:

$$v_g(\theta) = V_g|\sin\theta| \ . \tag{3.21}$$

The output voltage is regulated by the secondary side feedback, and the required duty ratio $d_1(\theta)$ is:

$$d_1(\theta) = \frac{v_1(\theta)}{v(\theta) + v_g(\theta)} = \frac{V_1}{V + V_g|\sin\theta|} \cdot \tag{3.22}$$

Performance of the CI inverse SEPIC converter in input current shaping can be evaluated by finding the expression for the input current waveform. Figure 3.6(b) shows the input current and other key switching waveforms of the converter in Fig. 3.6(a).

During the first interval D_1T_s, input current is the sum of the output inductor current i_1 and the magnetizing current i_m of the transformer. After the transistor Q_1 is turned OFF, the input current is equal to the rising magnetizing current only. Keeping in mind that the converter operates in DICM, the expression for the input current of the CI inverse SEPIC converter is:

$$i_g(\theta) = \frac{D^2T_s v_g(\theta)}{2L_m} + I_1 d_1(\theta) \ . \tag{3.23}$$

Substitution of (3.21) and (3.22) in the above equation yields:

$$i_g(\theta) = \frac{D^2T_s}{2L_m} \cdot V_g|\sin\theta| + \frac{V_1 I_1}{V + V_g|\sin\theta|} \cdot \tag{3.24}$$

Here, it is convenient to use normalized switch voltage stress γ defined in (3.19), where $V_{off} = V + V_g$ is a switch voltage stress at the peak of the line voltage ($\theta = \pi/2$). Upon substitution of (3.19) and $P_{out} = V_1 I_1$ in the previous equation and rearrangement, the expression for the input current of the CI inverse SEPIC shaper is:

$$i_g(\theta) = \frac{P_{out}}{V_g}\left(f \cdot |\sin\theta| + \frac{1}{\gamma - 1 + |\sin\theta|}\right) \cdot \tag{3.25}$$

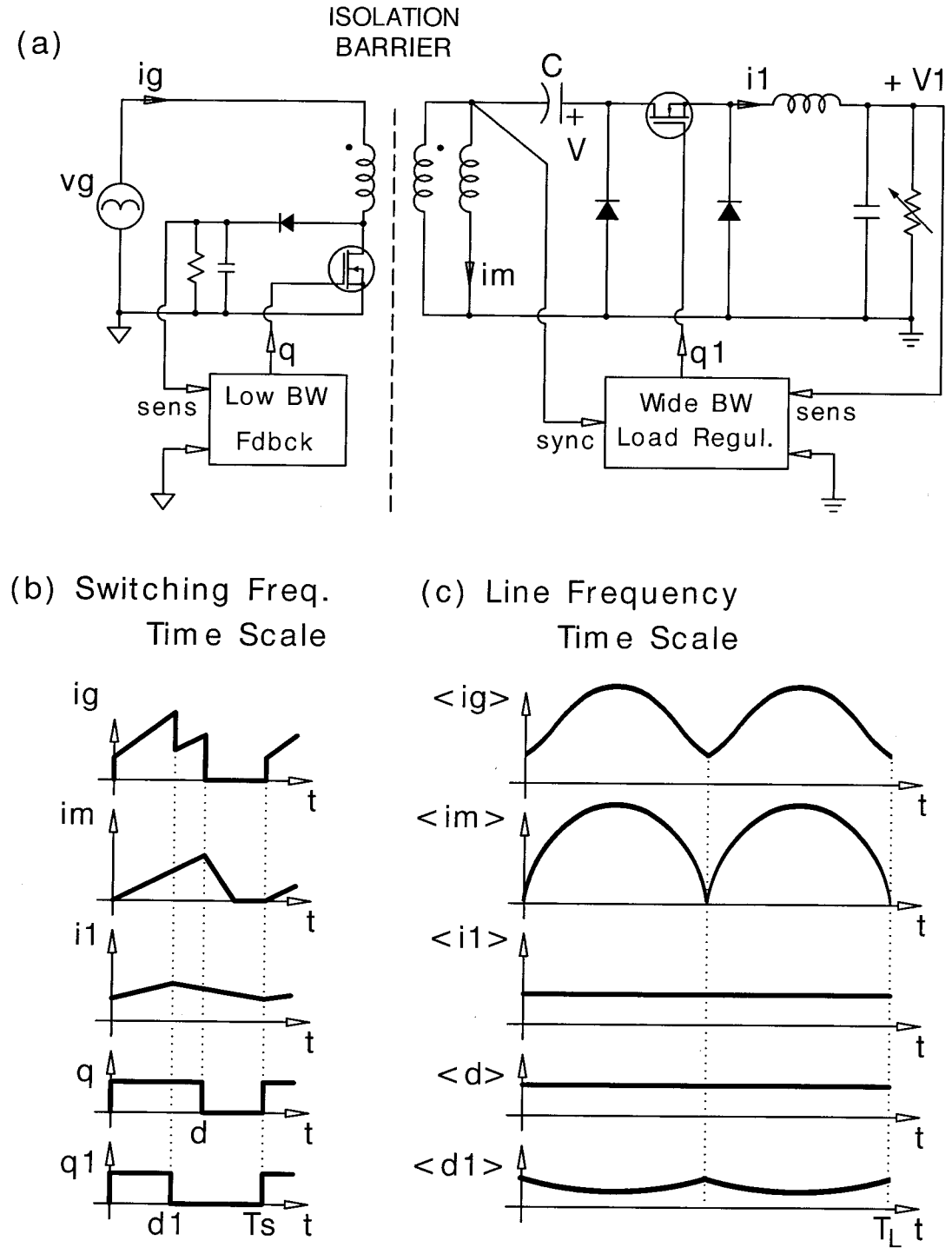

Figure 3.6: *(a) Isolated Capacitive Idling inverse SEPIC regulator operating in the DICM provides a high power factor automatically, i.e. without the input current feedback loop. Also shown are: (b) key switching waveforms and (c) averaged switching waveforms displayed as continuous, time-varying functions in the line frequency time scale.*

Quantity f lumps together several circuit parameters and it appears to be a function of the input voltage, dc output power and duty ratio D. The following analysis shows, however, that f is a function of the normalized switch voltage stress γ only. It is evaluated through the power balance equation. The output power of the ac-to-dc regulator equals the average input power:

$$P_{out} = \frac{P_{out}}{\pi} \int_0^{\pi} \left(f \cdot \sin^2 \theta + \frac{\sin \theta}{\gamma - 1 + \sin \theta} \right) d\theta \, . \tag{3.26}$$

From here, it follows that:

$$f(\gamma) = 2 \left(1 - \frac{1}{\pi} \int_0^{\pi} \frac{\sin \theta}{\gamma - 1 + \sin \theta} d\theta \right) \tag{3.27}$$

where the integral does not have a closed form solution. Nevertheless, (3.27) shows that $f = f(\gamma)$ is a function of one variable only — the normalized switch voltage stress γ.

The input current (3.25) of the converter in Fig. 3.6 has two components. One is proportional to the rectified sinewave input voltage, while the other causes distortion and results in less-than ideal power factor. Figure 3.6(c) qualitatively shows the average input current waveform along with several other averaged switching waveforms displayed in the line frequency time scale. All these waveforms are obtained by averaging the corresponding switching waveform of Fig. 3.6(b), and are shown as continuous, time-varying functions.

Definition for power factor $PF \equiv P_{in}/(I_{gRMS} \cdot V_{gRMS})$ applied to the converter in Fig. 3.6 yields:

$$PF = \sqrt{\frac{2\pi}{\int_0^{\pi} \left(f(\gamma) \cdot \sin \theta + \frac{1}{\gamma - 1 + \sin \theta} \right)^2 d\theta}} \, . \tag{3.28}$$

Again, this result does not have a closed form solution. However, it can be solved numerically for different values of parameter γ. The power factor as a function of γ is plotted in Fig. 3.7, and it approaches unity as the value of γ increases. This means that the design of an ac-to-dc regulator based on the CI converters will involve a trade-off between good power factor and the higher switch voltage stress.

It is important to note that the high power factor in the converter of Fig. 3.6 is obtained by keeping the duty ratio d of the primary side switch constant throughout the line cycle (Fig. 3.6(c)). The input current shaping is performed automatically, without the input current feedback loop, and the converter is referred to as the "automatic" current shaper.

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3.5.2 Discontinuous Mode Boundary

Because an automatic current shaper can have a high power factor only when it operates in DICM, it is essential to determine condition that would ensure operation in DICM throughout the line cycle.

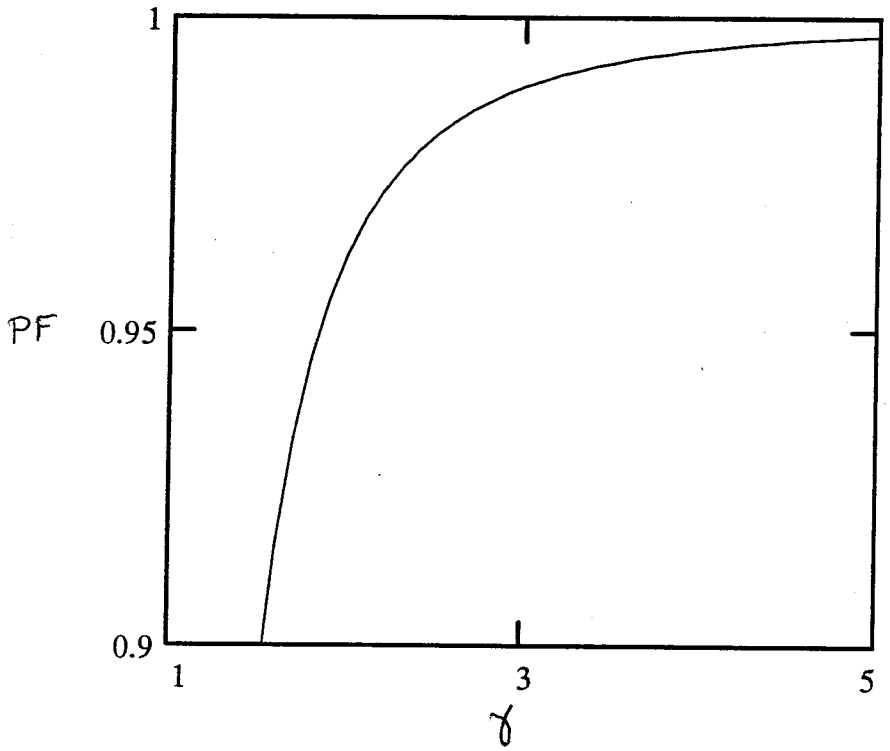

Figure 3.7: Power factor of Capacitive Idling ac-to-dc converters as a function of the normalized switch voltage stress γ.

between zero and peak value during the line cycle. For example, in the case of a unity power factor rectifier, the input power is given by (3.2), and it changes from $P_{min} = 0$ to $P_{peak} = 2P_{out}$.

Obviously, this property of input current shapers has to be taken into account when defining the DICM boundary for these converters. Based on this discussion, we define a critical parameter $k_c(\gamma)$ for ac-to-dc converter operating as an input current shaper:

$$k_c(\gamma) \equiv K_c(\gamma)\frac{P_{out}}{P_{peak}} \tag{3.29}$$

in terms of the previously defined critical parameter $K_c(\gamma)$ for a dc-to-dc converter, output power P_{out}, and peak input power P_{peak}. As previously mentioned, all unity power factor rectifiers have a peak input power $P_{peak} = 2P_{out}$, and according to (3.29) the critical parameter for these ideal current shapers is $k_c(\gamma) = 2K_c(\gamma)$. This is in agreement with the results obtained in [2] and [9]. More important, the definition of the critical parameter (3.29) enables us to determine the DICM boundary for the Capacitive Idling current shapers even though the input current waveform is not an ideal sinewave. This was not possible following the approach used in [2] and [9].

In input current shapers the peak of the input power coincides with the input voltage peak ($\theta = \pi/2$) and can be written as:

$$P_{peak} = V_g I_g \tag{3.30}$$

where I_g denotes value of the input current at $\theta = \pi/2$. According to (3.25):

$$I_g = i_g(\theta)|_{\theta=\pi/2} = \frac{P_{out}}{V_g}\left(f(\gamma) + \frac{1}{\gamma}\right). \tag{3.31}$$

Substitution of (3.30), (3.31) and (3.20) in (3.29) leads to:

$$k_c(\gamma) = \frac{\gamma - 1}{\gamma^3} \cdot \frac{1}{f(\gamma) + 1/\gamma}. \tag{3.32}$$

This result represents the DICM boundary for the CI inverse SEPIC shaper. In other words, the converter of Fig. 3.6 operates in DICM throughout the line cycle, if the following inequality is satisfied:

$$K_e < k_c(\gamma) \tag{3.33}$$

where K_e is given by (3.11). This result is very useful, because it provides a criterion for the design of the magnetizing inductance L_m of the converter in Fig. 3.6. From (3.33) and (3.11):

$$L_m < \frac{RT_s k_c(\gamma)}{2D_1^2} \tag{3.34}$$

where $D_1 = V_1/(V + V_g)$ is duty ratio value at $\theta = \pi/2$.

From the design point of view, it would be more convenient to have a closed form expression for the critical parameter $k_c(\gamma)$. While the closed form solution of (3.32) can not be found, the lower bound for the $k_c(\gamma)$ is:

$$k_{cmin}(\gamma) = k_c(\gamma)|_{min} = \frac{1}{2} \cdot \frac{\gamma - 1}{\gamma^3} = \frac{1}{2} \cdot K_c(\gamma) \tag{3.35}$$

and is approached as the power factor approaches unity. This is to be expected, because the peak power of an ideal current shaper is double the output dc power.

Thus, by satisfying a more conservative condition:

$$K_e < \frac{\gamma - 1}{2\gamma^3} \tag{3.36}$$

the discontinuous inductor current mode of operation is guaranteed throughout the line cycle.

All results of this Section have been derived for the converter of Fig. 3.6. Nevertheless, they apply to the other CI shapers as well. In particular, the expressions for the input current and the power factor of the other three converters are also given by the equations (3.25) and (3.28), respectively. The same is true for the DICM boundary given by the inequality (3.36).

3.6 Experimental Results

An experimental converter was built to operate from 110 volt, 60 hertz ac line and provide regulated +5 volt, 50 watt and –12 volt, 30 watt outputs. The circuit diagram, along with the component values of the prototype, is shown in Fig. 3.8. The schematic shows a somewhat unusual configuration of the CI converter. The advantage is that this two-output converter has only one secondary transformer winding, a single energy storage capacitor and a single diode D, with the limitation that both outputs are connected to the same ground. Effectively, this converter consists of two different isolated CI converters: the CI inverse SEPIC converter (output V1) described in Fig. 3.2(a), and the CI flyback (output V2) described in Fig. 3.2(b). By rearranging

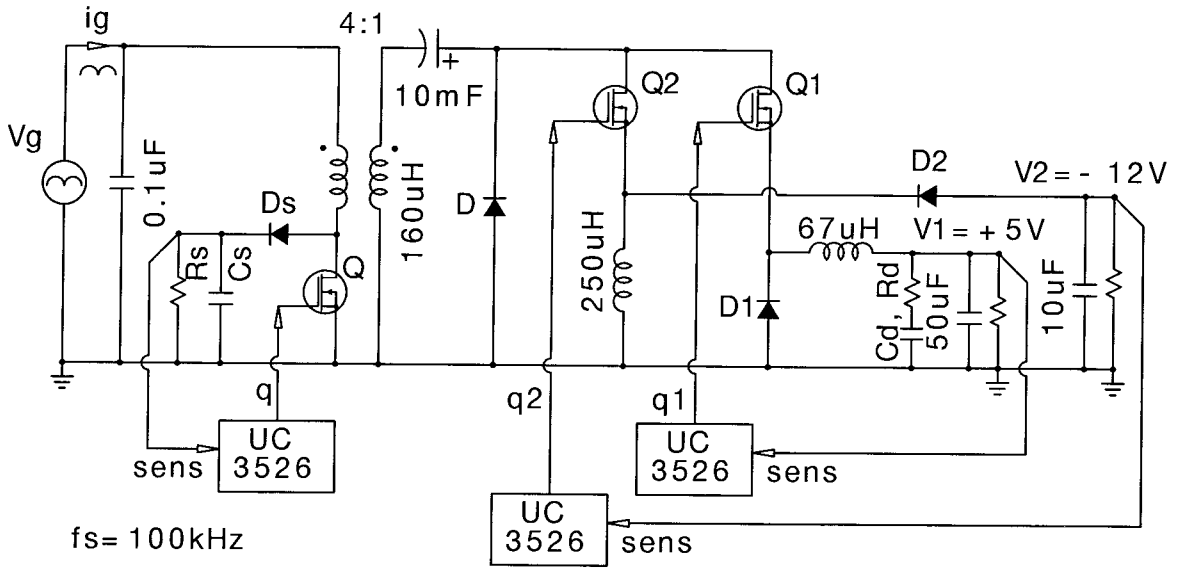

Figure 3.8: *Experimental, two-output ac-to-dc regulator was built to demonstrate feasibility of two different isolated converters: the Capacitive Idling inverse SEPIC (output V1) described in Fig. 3.2(a), and the Capacitive Idling flyback (output V2) described in Fig. 3.2(b).*

the power stage on the primary side, the other two CI converters have also been tested: the CI Ćuk converter (output V1) described in Fig. 3.2(c), and the CI SEPIC (output V2) described in Fig. 3.2(d).

The component values were chosen to ensure operation in the desired DICM. Using inequality (3.34), with the values of load resistance R and duty ratio D_1 reflected to the primary side, the maximum value of the magnetizing inductance is $L_m \leq 300\mu H$. Capacitance and voltage of the secondary side energy storage capacitor were chosen to satisfy both the minimum energy storage and the minimum hold-up time requirements. The nominal voltage of this capacitor was 35 volts, and when reflected to the primary side this resulted in the normalized switch voltage stress γ=2. The switching frequency of 100 kilohertz was chosen for size and efficiency reasons.

The switching waveforms shown in Figs. 3.9 and 3.10 demonstrate DICM operation of the CI inverse SEPIC—flyback and the CI Ćuk —SEPIC converters. Note that the switching current waveform of the CI Ćuk —SEPIC converter is always positive with relatively small switching ripple. This is because the onset of DICM in these two converters is determined by the equivalent inductance representing the parallel combination of magnetizing and input inductance $L_e = LL_m/L + L_m$. A small value of the magnetizing inductance is usually preferred because it reduces the amount of switching ripple at the input.

The line current waveforms shown in Figs. 3.11 and 3.12 agree with the analytical expression for the input current waveform derived in Section 3.5. The measured power factor in both cases is 95.5%, resulting in total harmonic distortion of 31%. These results are very close to the predicted power factor value in Fig. 3.7 for the given value of γ=2. Although the input current waveform is not a perfect sinewave in either example, it meets the IEC 555–2 regulations. This was verified under the assumption that the harmonic current limits in 220 volt systems can be applied to 110 volt systems by multiplying the standard values by 2.

3.7 Conclusions

A new Capacitive Idling class of dc-to-dc converters has been extended to applications requiring ac-to-dc regulation. These isolated converters provide both input current shaping and wide bandwidth regulation of multiple outputs in a single power stage. When compared to a conventional approach involving up to three cascaded power stages, the new converter class represents a very attractive alternative.

The main advantages of the Capacitive Idling shapers are:

— Current shaping and regulation in a single power stage,

— Simple control implementation with no feedback isolation,

— Wide bandwidth loop gain on all outputs,

— Independent short-circuit protection of each output.

The analysis has shown that the input current shaping mode of operation of the Capacitive Idling converters involves a trade-off between the high power factor and the increased switch voltage stress (Fig. 3.7). Operation in DICM throughout the line cycle can be guaranteed by the inequality (3.36).

The experimental results verify the analysis and confirm that the Capacitive Idling shapers represent a viable and attractive approach for input current shaping and multiple output regulation.

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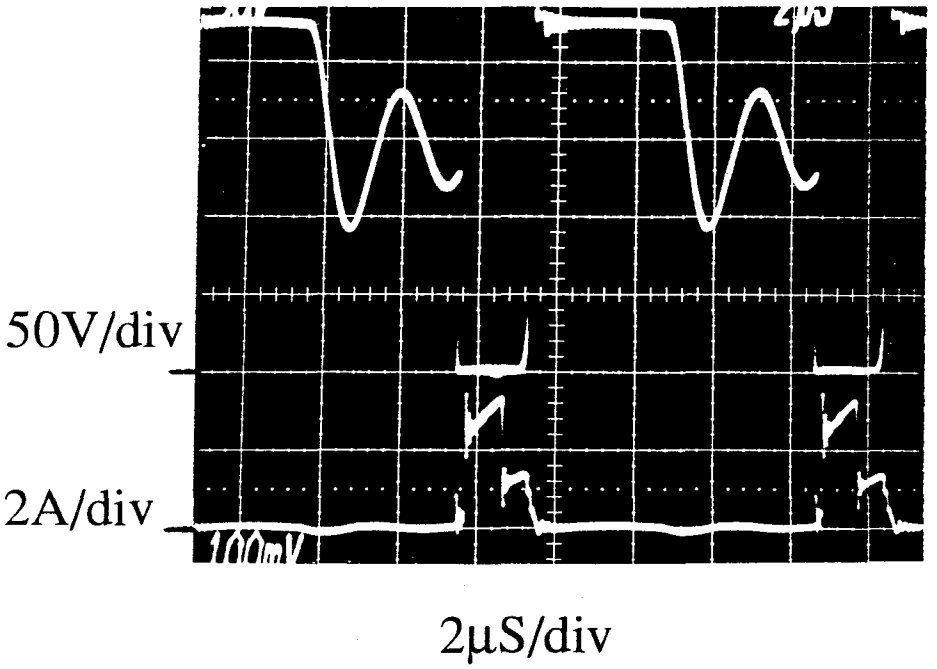


Figure 3.9: Measured switching waveforms of the Capacitive Idling inverse SEPIC—flyback prototype described in Fig. 3.8. Shown is drain-to-source voltage (50V/div) and drain current (2A/div) of the primary side transistor. Time scale is 2μS/div.

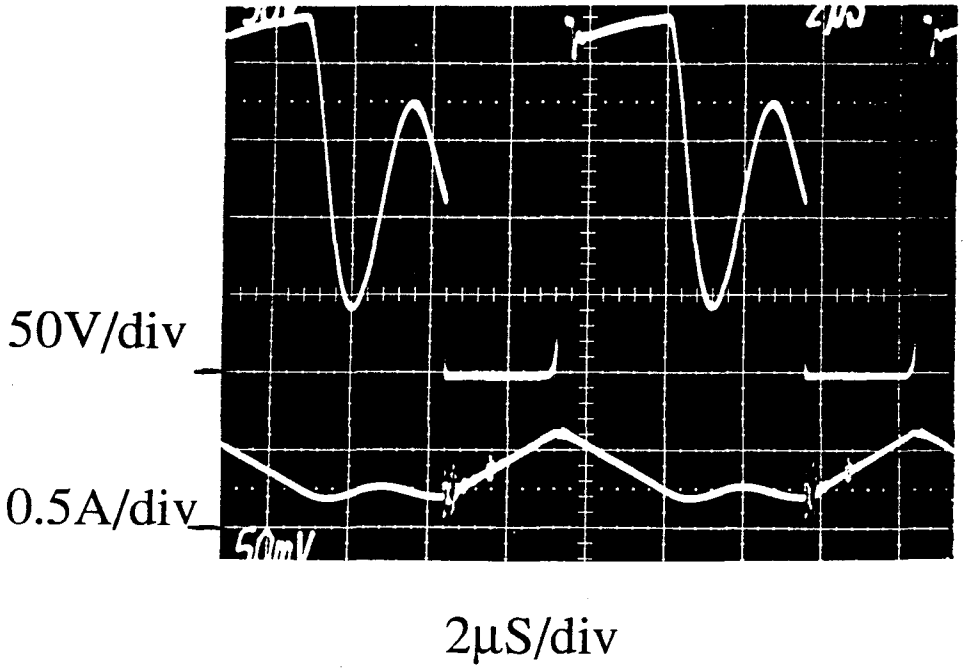


Figure 3.10: Measured switching waveforms of the Capacitive Idling Ćuk—SEPIC prototype. Shown is drain-to-source voltage (50V/div) of the primary side transistor and input current [0.5A/div]. Time scale is 2μS/div.

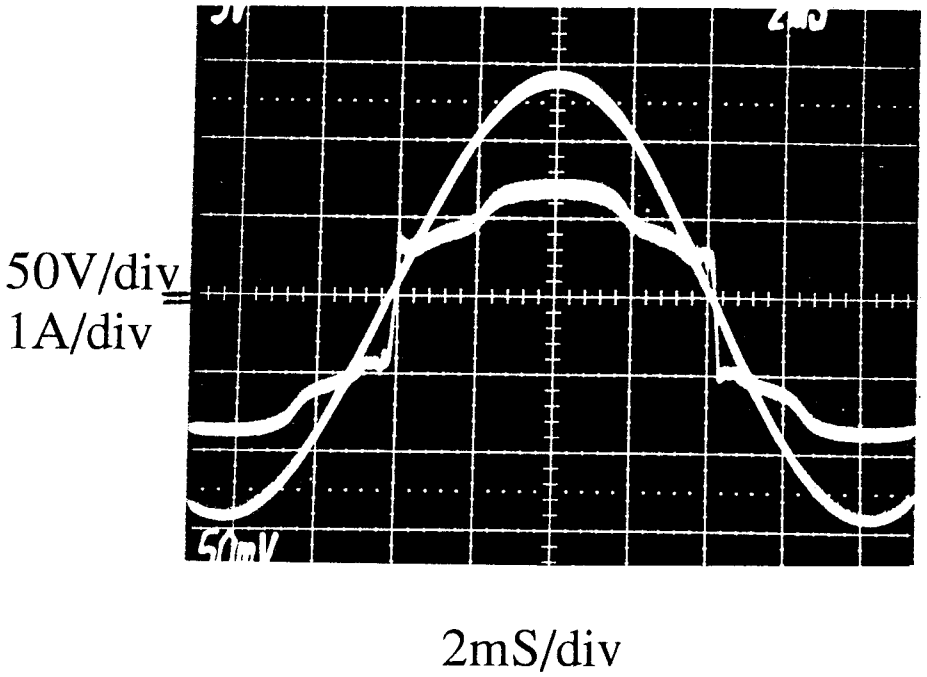


Figure 3.11: Measured line voltage (50V/div) and current (1A/div) waveforms of the experimental converter shown in Fig. 3.8, with 50W load at output V1, and 30W load at V2. Time scale is 2mS/div.

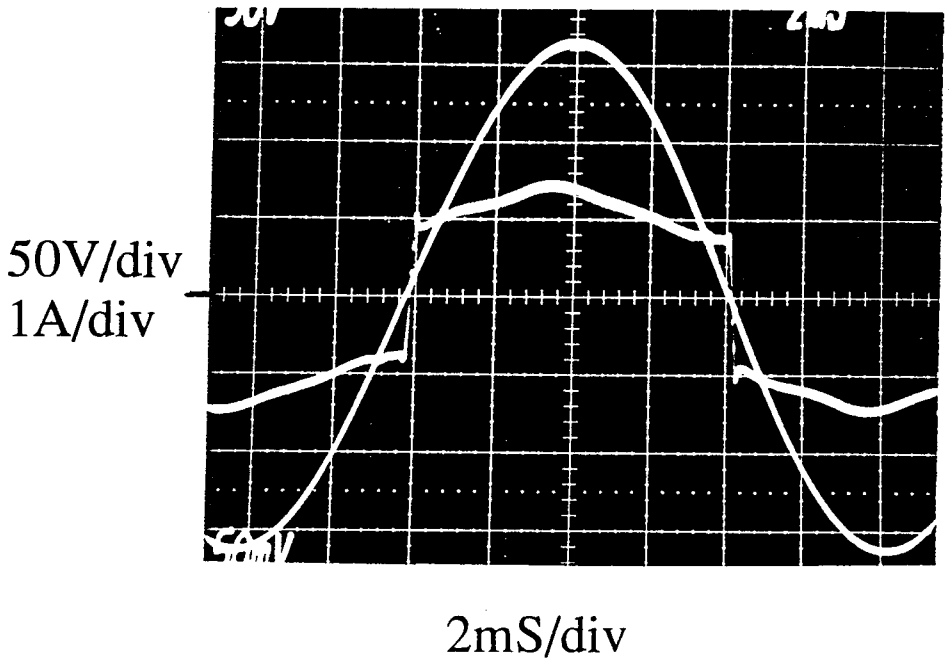


Figure 3.12: Measured line voltage (50V/div) and current (1A/div) waveforms of the experimental Capacitive Idling Ćuk — SEPIC converter, with 50W load at output V1, and 30W load at V2. Time scale is 2μS/div.

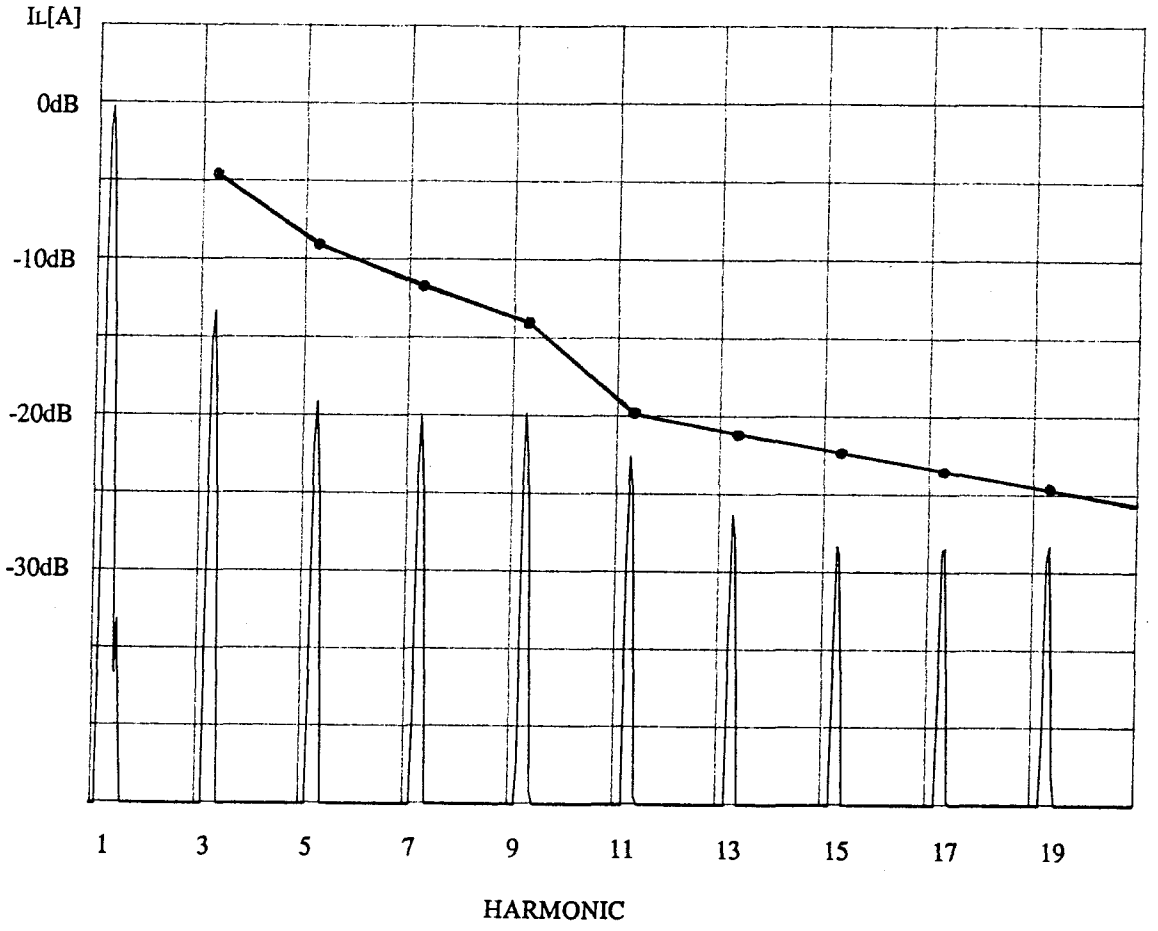


Figure 3.13: Measured line current harmonic content of the automatic current shaper shown in Fig. 3.8 satisfies the harmonic current limitations imposed by the IEC 555–2 standard.

Addendum A
General Stability Criteria For Cascaded Switching Converters

The solution to the special problem of stability investigation of the boost regulator cascaded by the buck regulator and its Capacitive Idling Ćuk converter counterpart with decoupled primary and secondary dynamics, points to the solution of the more general problem encountered in practice, that of two cascaded switching regulators having arbitrary topology. Very often, an off-line isolated switching regulator (such as a forward converter, full bridge, push-pull, etc.) is loaded by a number of separate regulated converter modules, such as buck, flyback, boost, etc. The stability of such complex switching systems is often assessed through an exhaustive simulation of all possible operating conditions to eliminate possible unstable operation. It is our goal to understand the nature of interaction of the cascaded regulators and arrive at general analytic criteria that would, with much greater certainty, guarantee stable and reliable operation of the overall system.

The problem of stability of the cascaded boost-buck converter is similar to the problem of placing an input filter in front of the switching regulator, as in Fig. A.1. If the input filter is improperly chosen it might cause instability and oscillations even though the regulator alone is stable and well behaved. This problem was traced in [1] to the fundamental property of the closed loop switching regulator having negative input impedance due to constant output power P, and analytic criteria for stable design were derived. It was shown in [1] that the regulator loop gain is not significantly altered by addition of an input filter if the magnitude of the input filter output impedance $|Z_o|$ is sufficiently smaller than:

1) the open-loop null double injection [2] input impedance $\left|Rf(s)/M^2\right|$,

2) the open-loop input impedance $\left|Z_{ei}/M^2\right|$.

Also, if $|Z_o|$ is sufficiently smaller than the open-loop input impedance with a short circuit at the output $\left|(R_e + sL_e)/M^2\right|$, then the closed-loop output impedance will be essentially unaffected by the addition of the input filter. These three impedance inequalities provide relatively simple design guidelines for a regulator with input filter. Moreover, it was shown in [1] that these inequalities are more-than-necessary conditions for the stability of the switching regulator with

input filter. It was found that stability of a switching regulator with input filter depends on the stability of the "minor loop gain" T_i, defined as the ratio of Z_o and the regulator closed-loop input impedance Z_i.

However, there is an important difference in stability requirement between a regulator with input filter and the cascaded connection of two regulators. In the case of the regulator with input filter of Fig. A.1, variation of input voltage induces variation of regulator DC gain, which in turn changes the magnitude of the regulator input impedance. This effect can be observed by plotting the two impedances for three different values of input voltage, low line, nominal line and high

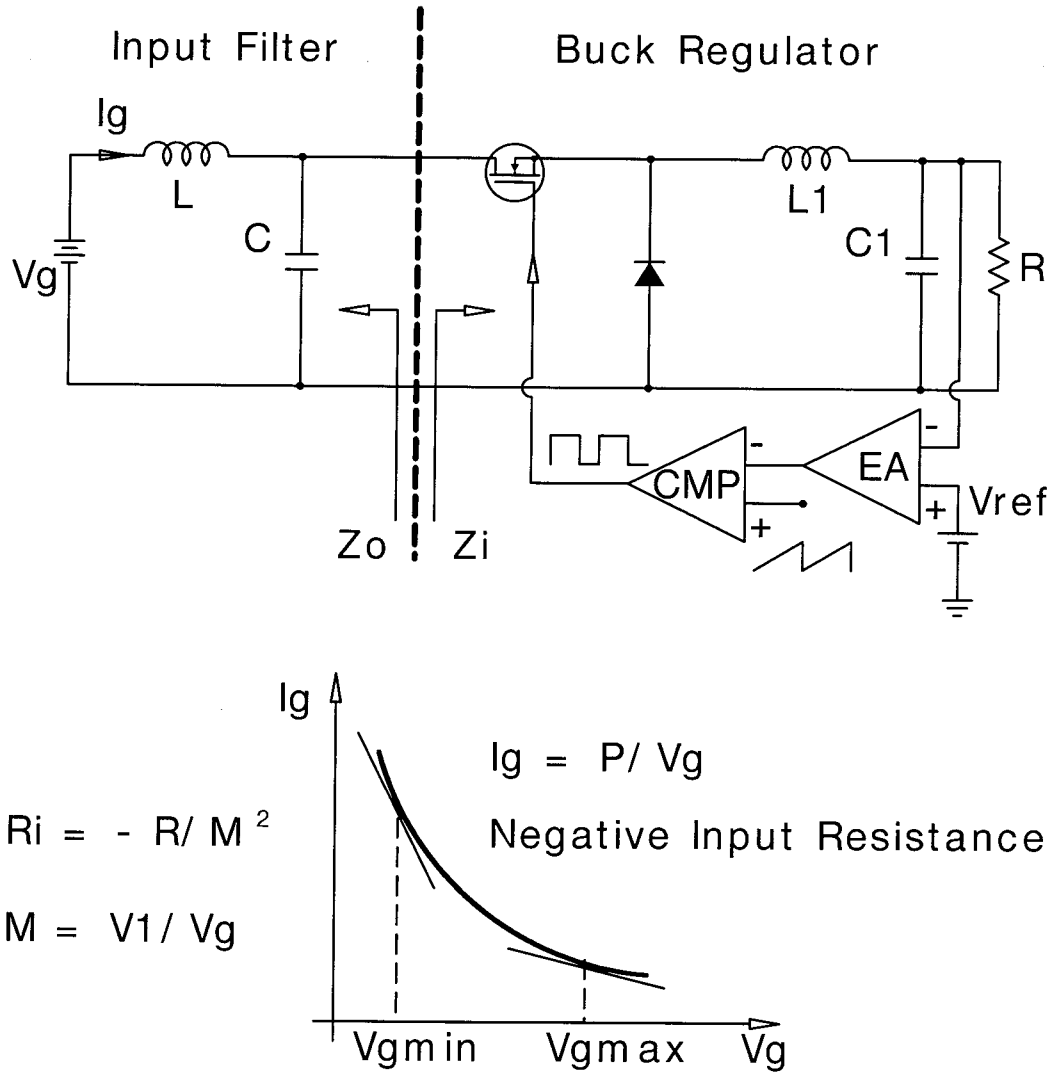
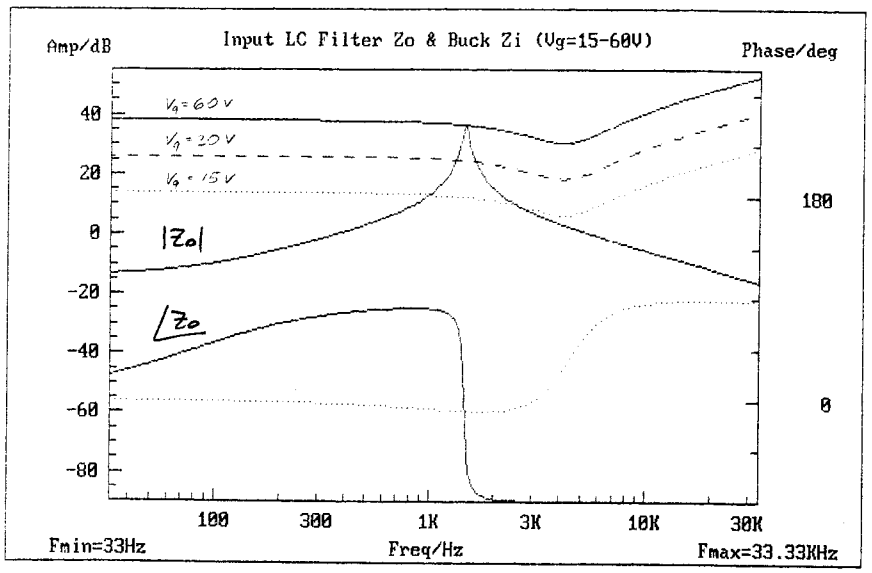


Figure A.1: *Adding input filter to the switching regulator can cause stability problems due to the negative input resistance of the regulator.*

a)



b)

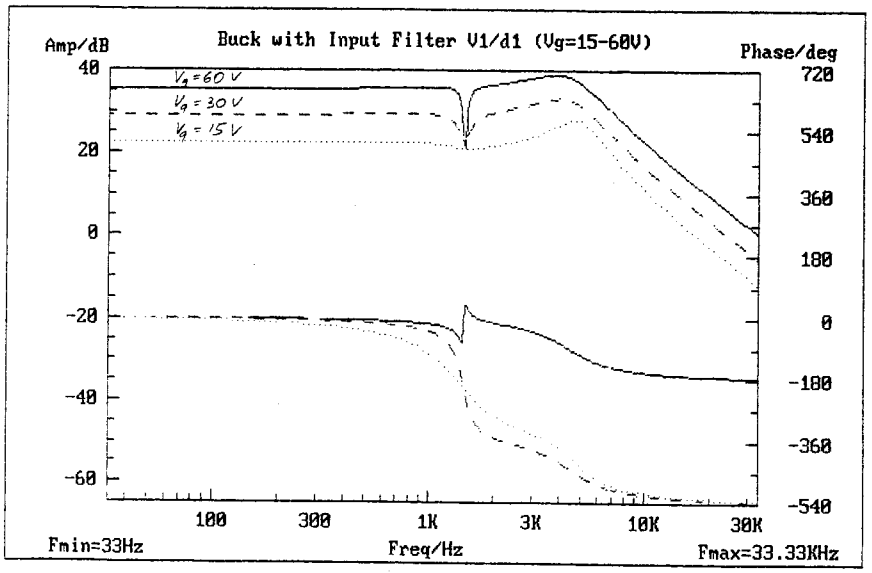


Figure A.2: Magnitudes of the input filter output impedance Z_o and the open loop input impedance Z_i of the buck switching regulator of Fig. A.1 are affected by input voltage variations (a) causing severe degradation of the duty-ratio-to-output transfer function (b).

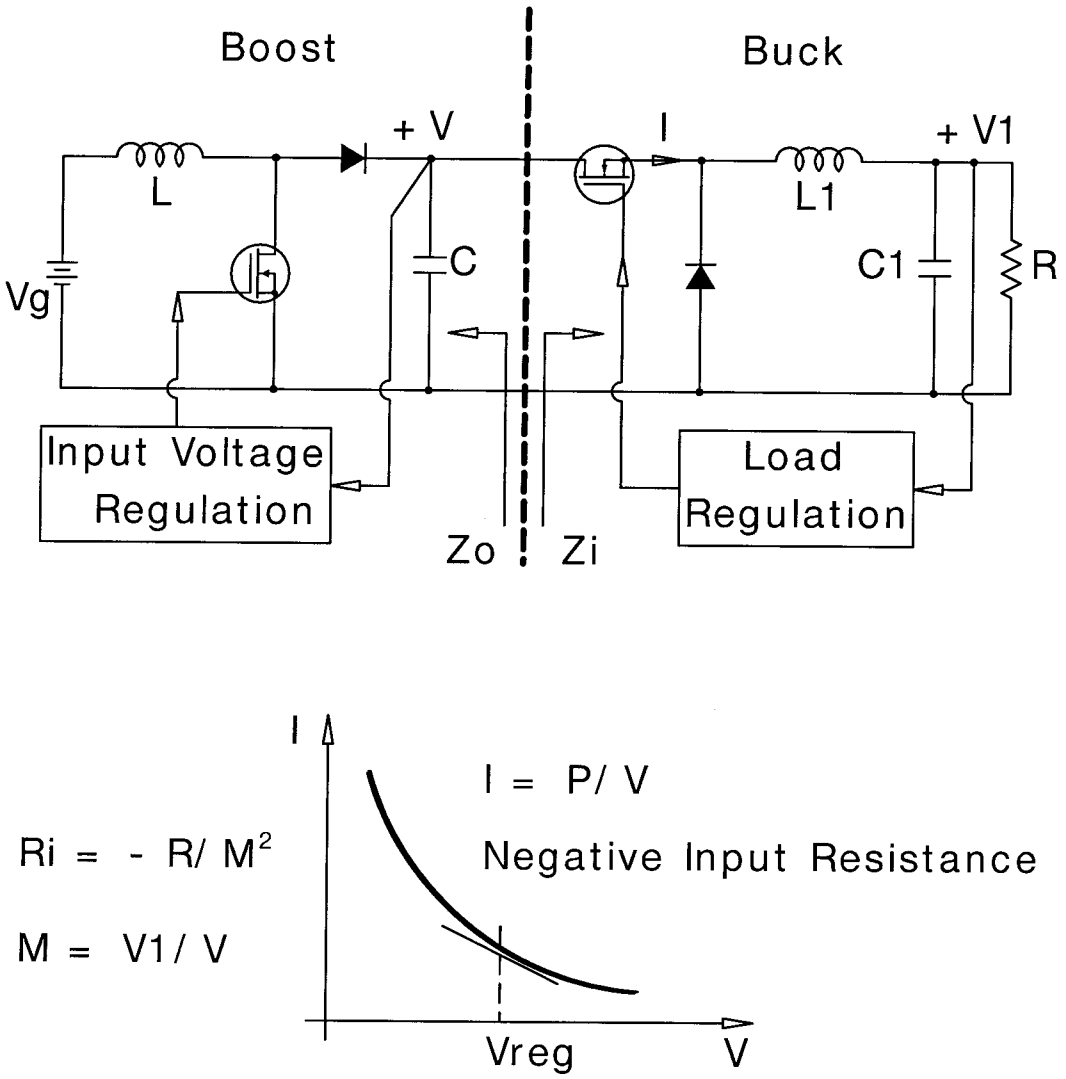


Figure A.3: *Cascaded connection of two closed loop switching regulators can also be unstable due to the negative input resistance of the post-regulator.*

line (15V, 30V and 60V). It is obvious from Fig. A.2(a) that the input filter output impedance Z_o does not change, while the magnitude of the regulator input impedance $|Z_i|$ moves in the vertical direction. This means that the input filter design has to meet the worst case scenario requirement, which puts a severe constraint on its output impedance Z_o. If the impedance criteria for input filter design are not met for all operating conditions, as is clearly the case in Fig. A.2(a), regulator loop gain is severely affected (Fig. A.2(b)), leading possibly to instability of the system.

The situation is different in the case of the cascaded connection of two regulators of Fig. A.3. Here, the pre-regulator provides a constant intermediate voltage feeding the post-regulator

stage. Consequently, the input impedance of the second stage is constant, while the pre-regulator output impedance changes. However, the peak of the output impedance remains constant, while its frequency changes, making it easier to satisfy the impedance inequality conditions. Figure A.4(a) displays impedance plots of the cascaded boost-buck converter for three different input voltage values, while Fig. A.4(b) shows a rather limited effect of the input voltage variation on the buck post-regulator transfer function in all three cases. This suggests that the stability criteria for a cascaded regulator are not as restricting as those of the regulator with input filter.

A.1 Analytic Results

The assumption is that each of the two subsystems is stable.

In the case of cascaded regulator, the ordinary input filter of Fig. A.1 is replaced with the switching pre-regulator. Hence the interaction becomes that of the two closed loop regulators, as illustrated on the example of a cascaded boost-buck converter of Fig. A.3. In general, the small signal model [3] of the cascaded connection of two regulators is shown in Fig. A.5, including notation slightly different from the one used in [1] (changes were necessary in order to accommodate this more complicated situation). Without going into detailed analysis of the model in Fig. A.5, we outline the following results:

Suppose that a current load is connected to the separate front-end converter during measurements of the loop gain T. If the value of the current load is chosen to be similar to the load presented to the front-end converter by the post-regulator, the conduction mode (CCM or DCM) and consequently the DC gain of the front-end converter is same in both cases. When the front-end converter is loaded with the post-regulator, its loop gain T' can be expressed in terms of the measured loop gain T of the separate pre-regulator:

$$T' = T\frac{1}{1+\frac{Z_o}{Z_{i1}}} \tag{A.1}$$

Here, Z_o is the closed loop output impedance of the pre-regulator supplying the current load and Z_{i1} is the post-regulator closed loop input impedance.

Post-regulator loop gain T_1 is also affected by the presence of the pre-regulator, with the new expression [1]:

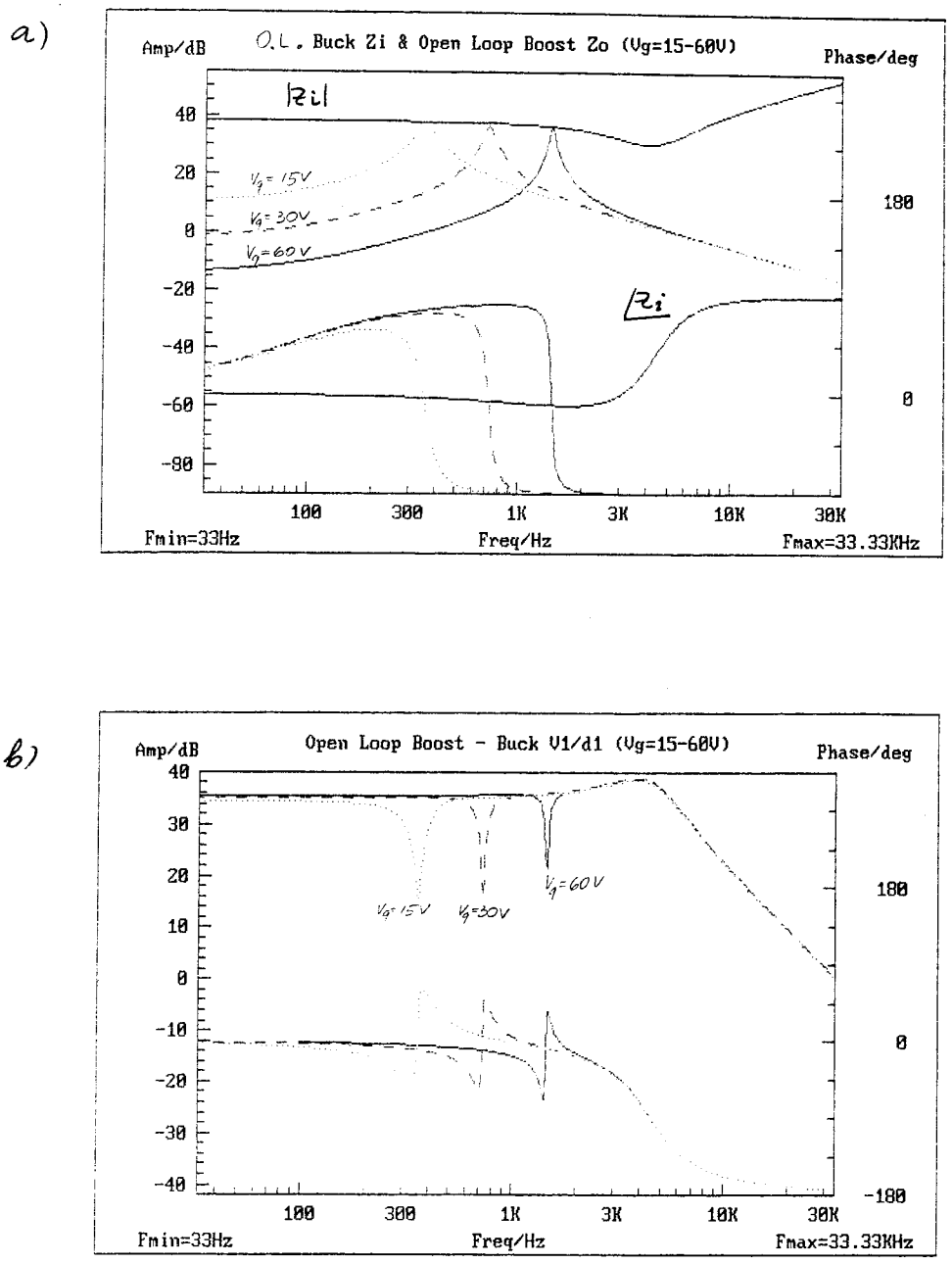


Figure A.4: Frequency response of the cascaded boost-buck switching regulator with two decoupled feedback loops is essentially unaffected by the input voltage changes.

Here, M_1 is a DC gain of the second stage, $f_1(s)$ it's frequency dependent factor introduced

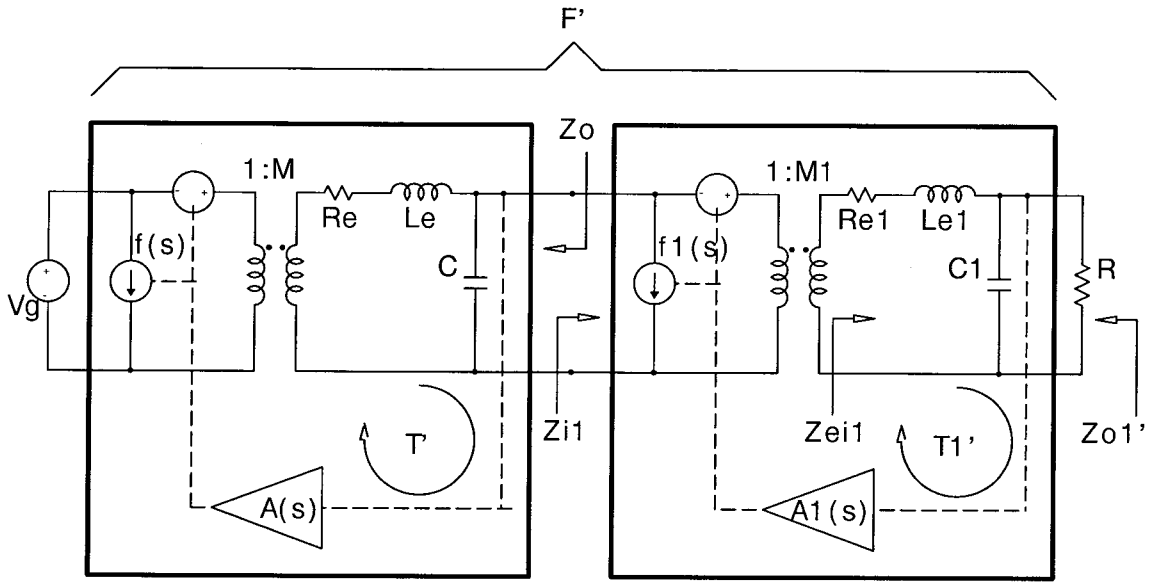


Figure A.5: *Small-signal model for the cascaded connection of two arbitrary switching regulators.*

$$T_1' = T_1 \frac{1 - \frac{Z_o M_1^2}{R f_1(s)}}{1 + \frac{Z_o M_1^2}{Z_{ei1}}} \cdot \tag{A.2}$$

Here, M_1 is the DC gain of the second stage, $Rf_1(s)/M_1^2$ is the open-loop null double injection input impedance, and Z_{ei1}/M_1^2 is the open loop input impedance of the regulator.

The line transfer function of the cascade can be expressed as a product of two individual closed loop line transfer functions (F and F_1), and a loading factor:

$$F' = F F_1 \frac{1}{1 + \frac{Z_o}{Z_{i1}}} \cdot \tag{A.3}$$

The closed loop output impedance Z_{o1}' in the presence of the pre-regulator can be expressed in terms of the output impedance Z_{o1} of the separate post-regulator:

$$Z_{o1}' = Z_{o1} \frac{1 + \frac{Z_o M_1^2}{R_{e1} + sL_{e1}}}{1 + \frac{Z_o}{Z_{i1}}} \tag{A.4}$$

where $R_{e1} + sL_{e1}$ is the impedance of the second stage filtering inductor.

The post-regulator closed-loop input impedance Z_{i1} remains unaffected by the presence of the pre-regulator:

$$\frac{1}{Z_{i1}} = -\frac{T_1}{1+T_1} \cdot \frac{M_1^2}{Rf_1(s)} + \frac{1}{1+T_1} \cdot \frac{M_1^2}{Z_{ei1}} \cdot \tag{A.5}$$

The condition determining stability of the cascaded system can be found by the following argument. Out of four system properties affected by the cascaded connection, (A.1) through (A.4), three contain the factor $1/(1+Z_o/Z_{i1})$. As it was done in [1], we identify the ratio Z_o/Z_{i1} as a "minor loop gain" T_i, and for stability of the cascaded system require that $(1+T_i)$ must not have roots in the right half-plane. From (A.5), T_i is given by:

$$T_i \equiv \frac{Z_o}{Z_{i1}} = -\frac{T_1}{1+T_1} \cdot \frac{Z_o M_1^2}{Rf_1(s)} + \frac{1}{1+T_1} \cdot \frac{Z_o M_1^2}{Z_{ei1}} \cdot \tag{A.6}$$

To ensure stability of the cascaded system, it is sufficient that the minor loop gain T_i is stable, i.e. satisfies the Nyquist stability criterion. Obviously, a more than necessary condition for the system stability is that:

$$|T_i| \equiv \left|\frac{Z_o}{Z_{i1}}\right| \ll 1 \, . \tag{A.7}$$

Note that equation (A.7) merely ensures stability of the cascaded system, while no guarantee can be made concerning the resulting modification of the individual transfer functions T, T_1 and Z_{o1}.

However, if the cascaded regulators are designed to satisfy the following impedance inequalities:

$$|Z_o| \ll \left|\frac{Rf_1(s)}{M_1^2}\right| \tag{A.8}$$

$$|Z_o| \ll \left|\frac{Z_{ei1}}{M_1^2}\right| \tag{A.9}$$

the pre-regulator loop gain T of (A.1) and the post-regulator loop gain T_1 of (A.2) become effectively unchanged by the cascaded connection. In addition to this, if we satisfy the inequality:

$$|Z_o| \ll \left|\frac{R_{e1} + sL_{e1}}{M_1^2}\right| \tag{A.10}$$

the post-regulator output impedance Z_{o1} of (A.4) is also unaffected by the pre-regulator.

It is important to note that the inequalities (A.8) through (A.10) guarantee stability of the cascaded system through the more-than-necessary condition (A.7).

References

[1] R.D. Middlebrook, "Input Filter Considerations in Design and Application of Switching Regulators," *IEEE Industry Applications Society Annual Meeting*, 1976, pp. 366–382.

[2] R.D. Middlebrook, "Null Double Injection and the Extra Element Theorem," *IEEE Trans. on Education*, vol. 32, no. 3, August 1989, pp. 167–180.

[3] R.D. Middlebrook and S. Ćuk, "A General Unified Approach to Modelling Switching Converter Power Stages," *IEEE PESC Record*, 1976, pp. 18–34.

Addendum B
Analysis of the Capacitive Idling Ćuk Converter

Consider an isolated Capacitive Idling Ćuk converter shown in Fig. B.1(a). Key switching waveforms describing operation of this converter in discontinuous conduction mode are shown in Fig. B.1(b). When the diode current becomes zero before the end of the switching cycle, the converter enters a discontinuous conduction mode of operation described in Fig. B.1(b). The onset of this discontinuous conduction mode is determined by two inductor currents: input inductor current i_g and magnetizing inductance current i_m. The sum of these two currents represents the current of diode D during interval D_2T_s of the switching period. Note that, as in the basic Ćuk converter operating in the DICM [7], the two inductor currents i_g and i_m of Fig. B.1(b) can have a nonzero value I at the end of switching period. The expression for this residual current I can be derived from the charge balance equation for the primary-side capacitor C':

$$I_1 D_1 + \frac{D^2 T_s V_g}{2L_m} - ID = \frac{DT_s V_g}{2L_m} D_2 + I(1-D)\,. \tag{B.1}$$

After rearrangement, the expression for the residual current I is:

$$I = I_1 D_1 + \frac{DT_s V_g}{2}\left(\frac{D}{L_m} - \frac{D_2}{L}\right)\cdot \tag{B.2}$$

According to (B.2), the residual current depends both on the operating conditions (D, D_1, T_s, V_g) and the choice of component values (L, L_m, R).

In the previously analyzed Capacitive Idling inverse SEPIC shaper of Fig. 3.6(a), choice of the internal energy storage capacitor is obvious since the capacitor C is the only internal capacitance of this converter. In the case of converters which have more than one internal capacitor, this choice is dictated by additional considerations. For example, an overriding issue determining practicality of a switching converter topology is its size, weight and cost. As pointed out in [2], the position of the internal energy storage capacitor affects the size of the isolation transformer in some converters.

To determine how choice of the energy storage capacitance influences the size of the isolation transformer, we consider the Capacitive Idling Ćuk converter of Fig. B.2. It was stated in [2] that the isolation transformer of this converter (the 3SN Ćuk shaper) is subject to line-frequency

voltages and is consequently large. Next, we will show that this is not necessarily the case and illustrate the analytical procedure that will enable us to make a choice of the energy storage capacitor that results in a small size of the isolation transformer.

The ac-to-dc Capacitive Idling Ćuk converter of Fig. B.2 has two internal capacitors: $C^{'}$ and $C^{''}$. Suppose this converter operates in the DICM described in Fig. B.1. In that case both the input inductance L and the magnetizing inductance L_m satisfy the volt-second balance during each switching cycle. Using notation of Fig. B.2, the volt-second balance equation for the input inductance L is:

$$DT_s v_g(\theta) = d_2(\theta)T_s\Big[v^{'}(\theta) + v^{''}(\theta) - v_g(\theta)\Big] \tag{B.3}$$

and for the magnetizing inductance L_m:

$$DT_s v^{'}(\theta) = d_2(\theta)T_s v^{''}(\theta)\ . \tag{B.4}$$

Linear combination of these two equations yields:

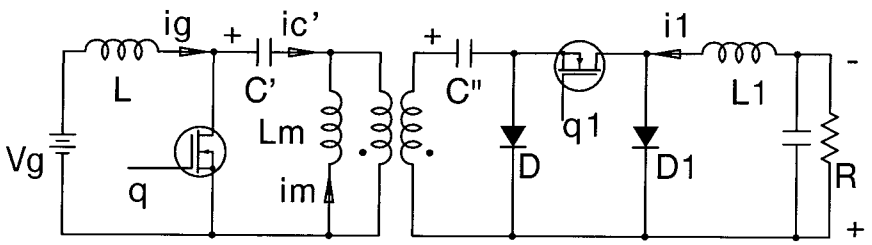
$$\frac{v^{'}(\theta)}{v^{''}(\theta)} = \frac{v_g(\theta)}{v^{'}(\theta) + v^{''}(\theta) - v_g(\theta)}\ . \tag{B.5}$$

From this, we obtain:

$$v^{'}(\theta) = v_g(\theta)\ . \tag{B.6}$$

This result shows that if the converter of Fig. B.2 operates in DICM, the voltage $v^{'}(\theta)$ of the primary side capacitor $C^{'}$ equals the rectified sinewave: $v^{'}(\theta) = V_g|\sin(\theta)|$. Note that in this analysis we did not make any assumption about the purpose of the capacitor $C^{'}$, namely whether it is an energy storage component or not. We know that, if $C^{'}$ is to be used as the energy storage capacitor, it has to satisfy the energy storage requirement (3.4). In practice, this means that its capacitance has to be large, making its voltage approximately constant. On the other hand, the converter of Fig. B.2 operating in DICM needs to satisfy (B.6), which requires the voltage $v^{'}(\theta)$ to be equal to the input voltage waveform. These two requirements are contradicting, and we conclude that the primary side capacitor $C^{'}$ cannot be used as the energy storage component in the Capacitive Idling Ćuk shaper described in Fig. B.2. As a result, the only other choice for the energy storage capacitor is the secondary side capacitance $C^{''}$.

(a)



(b)

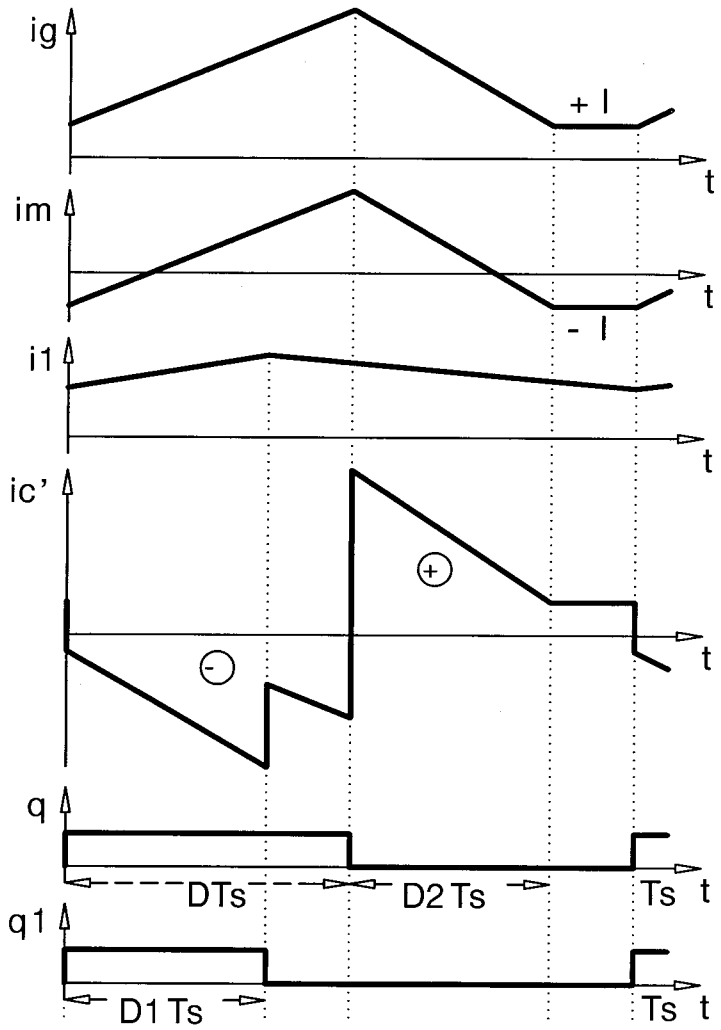


Figure B.1: *Key switching waveforms of the isolated Capacitive Idling Ćuk converter operating in discontinuous inductor current mode.*

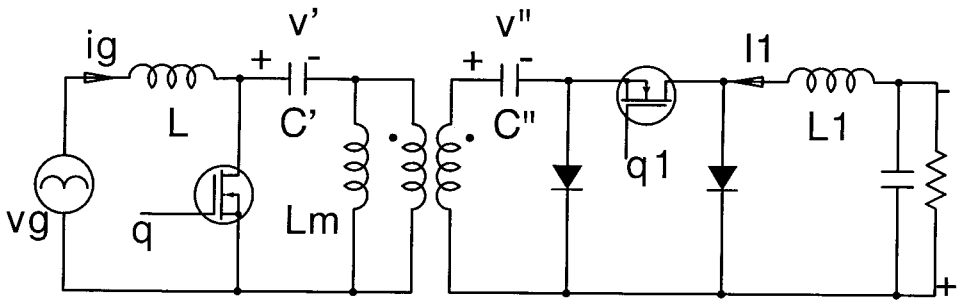


Figure B.2: *Isolated ac-to-dc Capacitive Idling Ćuk converter operating in discontinuous inductor current mode.*

Next, we derive the expression for the input current waveform of the Capacitive Idling Ćuk current shaper. According to the input current waveform shown in Fig. B.1(b), the average value of the input current is:

$$i_g(\theta) = \frac{DT_s v_g(\theta)}{2L}[D + d_2(\theta)] + i(\theta) \ . \tag{B.7}$$

Substitution of the expression for the residual current $i(\theta)$ given in (B.2) yields:

$$i_g(\theta) = \frac{DT_s v_g(\theta)}{2}\left[\frac{D + d_2(\theta)}{L} + \frac{D}{L_m} - \frac{d_2(\theta)}{L}\right] + I_1 d_1(\theta) \ . \tag{B.8}$$

After rearrangement, the input current of the converter in Fig. B.2 is:

$$i_g(\theta) = \frac{D^2 T_s v_g(\theta)}{2L_e} + I_1 d_1(\theta) \tag{B.9}$$

where $L_e = LL_m/(L + L_m)$. This result is the same as the expression (3.23) for the input current of the CI inverse SEPIC shaper (except for the equivalent inductance $L_e = LL_m/(L + L_m)$ instead of L_m). Similar analysis for the other two converters described in Fig. 3.2, the CI flyback and the CI SEPIC, also yields the same result for the input current waveform. This means that all four shapers of Fig. 3.2 offer the same power factor performance, approaching unity power factor as the normalized switch voltage stress increases (Fig. 3.7). As a result, the problem of selecting the most appropriate CI converter with respect to a given set of requirements will be decided by other considerations, such as: number of power components, presence of the switching frequency ripple in the input current, etc.