SPACE-CHARGE-LIMITED CURRENT IN GERMANIUM

Thesis by

Alex Shumka

In Partial Fulfillment of the Requirements

For the Degree of

Doctor of Philosophy

California Institute of Technology

Pasadena, California

1964

(Submitted March 2, 1964)

ACKNOWLEDGMENTS

The author is greatly indebted to Dr. M-A Nicolet under whose direction and constant encouragement this work was carried out. Thanks are due to Dr. K. Das Kuptas for verifying the crystallographic alignment of the wafers by X-rays and to the members of the Solid-State Laboratory for the Hall effect measurements. Hughes Semiconductor Division generously donated the germanium crystal. This work was initiated and supported in part by the funds made available by the California Institute of Technology Jet Propulsion Laboratory and completed under the support of the Naval Ordnance Test Station.

ABSTRACT

An experimental verification of the theory of space-charge-limited hole current in germanium is presented. Alloyed p-n-p solid-state diodes of various base widths W are fabricated. The V-I characteristic of each diode is measured at an ambient temperature of 78° K. These results are compared with theory. Dacey (4) predicts: $J = 1.43\epsilon\epsilon_o \mu_o E_c^{1/2} V^{3/2} W^{-5/2}$ where μ_o is the low field mobility of the holes and E_c is the critical electric field. This expression assumes a field dependence of hole mobility of $\mu = \mu_o(E_c/E)^{1/2}$.

The three halves power relationship between current and voltage is observed over nearly two current decades. In that same current range, a direct proportionality of V with $W^{5/3}$ at a constant current density is also observed to within the accuracy of base width and area measurements which are better than 5%. The value of the critical electric field obtained agrees with that estimated by Shockley's model (11).

Measurements are also made at higher ambient temperatures. The current decreases as expected from hot carrier considerations.

These results represent the first detailed verification of the validity of the theory of pure space-charge-limited current of hot carriers in solids. The measured

peak current density of 180 a/cm^2 is greater than any value reported on space-charge-limited current in solids by an order of magnitude.

Photographic materials on pp. 39, 40, 68, 89 and 91 are essential and will not reproduce clearly on Xerox copies. Photographic copies should be ordered.

TABLE OF CONTENTS

INTRODUCTION 1

CHAPTER I

SPACE-CHARGE-LIMITED CURRENT IN GERMANIUM: THEORY AND EXPERIMENT

Introduction 4

Section 1 Theory of Space-Charge-Limited Current in an Idealized Solid 5
- 1.1 One-Dimensional Model 5
- 1.2 Properties of the Idealized Solid-State Diode 7
- 1.3 Voltage-Current Relationship 7
- 1.4 Impedance 10

Section 2 Discussion on Space-Charge-Limited Current in Practical Solids 10
- 2.1 Insulators 10
- 2.2 Semiconductors 12
- 2.3 Field Dependent Mobility in Germanium 14

Section 3 Theory of Space-Charge-Limited Current in Germanium 17
- 3.1 Germanium P-N-P Structure as a Solid-State Diode 17
- 3.2 Three Ranges of Operation 19
  - 3.2a Punching-Through Range 21
  - 3.2b The High Current Range 22
  - 3.2c Low Current Range 24
- 3.3 Temperature Dependence 27
- 3.4 Impedance 29
- 3.5 Discussion on Validity of Assumptions 31

Section 4 Experimental Results 36
- 4.1 Fabricated Germanium P-N-P Solid-State Diode 36
- 4.2 Voltage-Current Relationship 36
- 4.3 Base Width Dependence 45
- 4.4 Critical Electric Field 49
- 4.5 Temperature Dependence 50

CONCLUSIONS 55

CHAPTER II

FABRICATION, EVALUATION AND MEASUREMENT

Introduction 57

Section 1 Measurement of Material Properties . 59
1.1 Resistivity Measurements 59
1.2 Hall Effect Measurements 63
1.3 Lifetime Measurements 64

Section 2 Crystal Alignment 65
2.1 Optical Apparatus for Crystal Alignment 65
2.2 Crystal Preparation for Alignment . 69
2.3 Crystal Alignment 70

Section 3 Fabrication of P-N Junctions and P-N-P Structures 76
3.1 Preparation of Wafers for Alloying . 76
3.2 Masking 76
3.3 Masking Procedure 78
3.4 Surface Treatment before Alloying . 79
3.5 Alloying P-N Junctions 81
3.6 Alloying P-N-P Structures 84
3.7 Surface Treatment after Alloying . . 84

Section 4 Measurement of P-N Junction and P-N-P Structure Properties 87
4.1 Metallurgical Analysis 87
4.2 Alloyed Junction Area 92
4.3 Ohmic Contacts 92
4.4 Depletion Capacitance 96
4.5 V-I Characterization of P-N Junctions 101
4.6 Junction Separation Distance in P-N-P Structures 104
4.7 V-I Characterization of a P-N-P Solid-State Diode 111

APPENDIX A Impedance of Space-Charge-Limited Currents with Field Dependent Mobility 113

APPENDIX B Resistance-Base Width Relationship: Theory 122

APPENDIX C Electrical Measuring Apparatus . . . 126

REFERENCES 131

INTRODUCTION

The effect of space charge in limiting the flow of electrons through vacuum in thermionic vacuum tube diodes and related devices is well known. Similar conditions can exist in solids such as insulators and semiconductors into which holes or electrons are injected. The objective of constructing solid-state devices which are analogs of the vacuum tube devices is a tantalizing one and its inevitable success will be an important contribution to the field of electronics. The best survey on the expanding interest in this field is given by Wright (1). The reader is referred to this recent article which also includes an extensive bibliography.

There exist several important theoretical studies on space-charge-limited (abbreviated scl) current in solids. Mott and Gurney (2) have considered a solid-state diode in which holes or electrons flow through a perfect crystal of infinite bulk resistivity from an ideal emitter to an ideal collector. For this idealized solid-state diode, the scl current is directly proportional to the square of the applied voltage. Shockley and Prim (3) modified this idealized model to include fixed ions in the solid. This analysis is applicable to scl current in semiconductors. Dacey (4) extended this result to include the effect of field dependent mobility. Rose (5) considered the influence

of traps, which are normally present in insulators. These theoretical contributions are representative of the important advancements toward understanding scl current in practical solids.

A limited amount of experimental work has been done on scl current in practical solids. Dacey (4) has made measurements on a germanium solid-state diode. In a semi-quantitative manner his results indicate scl current flow. Rose and Smith (6) and Wright (7), among others, have performed experiments on cadmium sulfide to which they succeeded in making injecting and collecting contacts. They observed non-ohmic current which can be interpreted as scl current in the presence of traps. This result has a firm semi-quantitative basis, but the theory of scl current has not been completely verified so far.

The subject matter to be presented here is an experimental verification of the theory of scl current in solids. Germanium is chosen as a suitable practical solid in which the theory can be tested. The following description is one that can be divided into three principal parts.

Part one outlines some theoretical aspects of scl current in solids (chapter I, sections 1, 2 and 3, and Appendix A). The primary objective is to consider the effect of different properties of the solid on scl current. This is accomplished by modifying the idealized case to include the properties of practical solids. A detailed

theory of scl current in germanium is given.

Detailed experimental results for scl current in germanium are presented and compared with theory in the second part (chapter I, section 4).

Part three describes the material used in the fabrication of the germanium p-n-p solid-state diodes. The techniques of fabrication, evaluation and measurement are outlined (chapter II, and appendices B and C).

CHAPTER I

SPACE-CHARGE-LIMITED CURRENT IN GERMANIUM: THEORY AND EXPERIMENT

Introduction

This chapter is divided into two parts. The first part outlines the theory of scl current in solids. The second part compares this theory with experimental results obtained in germanium.

The theory of scl current in solids is given in the first three sections. In section 1, an idealized solid-state diode similar to that assumed by Mott and Gurney is described. The current-voltage relationship is derived for a one-dimensional current flow. In section 2, the advantages and disadvantages of different types of solids as practical representatives of the idealized solid are discussed. Germanium is selected as the most suitable practical solid in which to verify the validity of the theory. In section 3 an alloyed p-n-p germanium structure, as a practical analog of an idealized solid-state diode, is considered. A theoretical treatment of scl current in such a solid-state diode, which is essentially that presented by Dacey, is outlined. Experimental results obtained from current-voltage measurements on fabricated germanium p-n-p solid-state diodes of different n-region (base) width are presented in section 4. From these results the

interrelationship between current, voltage, ambient temperature, and base width, are determined and compared with theory.

1 Theory of Space-Charge-Limited Current in an Idealized Solid

1.1 One-Dimensional Model. A solid of width W bounded by two parallel and planar electrical contacts is considered. One of the electrical contacts is assumed to inject charge carriers into the solid while the other contact acts as a collector. The injecting contact is called the emitter, the collecting contact the collector, and the region in between the base. A one-dimensional model for such a geometric arrangement is represented in figure 1.1. The x-axis has the emitter-solid boundary as the origin and is directed towards the collector. The electric field intensity vector $\overline{E}$, the current density vector $\overline{J}$, and the charge transport velocity vector $\overline{v}$ are considered as being directed in the positive x-axis direction. The potential of the emitter is measured with respect to the collector which is at zero potential.

The emitter is considered to inject holes only when it is at a positive potential. When it is at a negative potential no charge carriers are injected into the solid. This physical model is very similar to that of a thermionic vacuum tube diode where the cathode which injects electrons

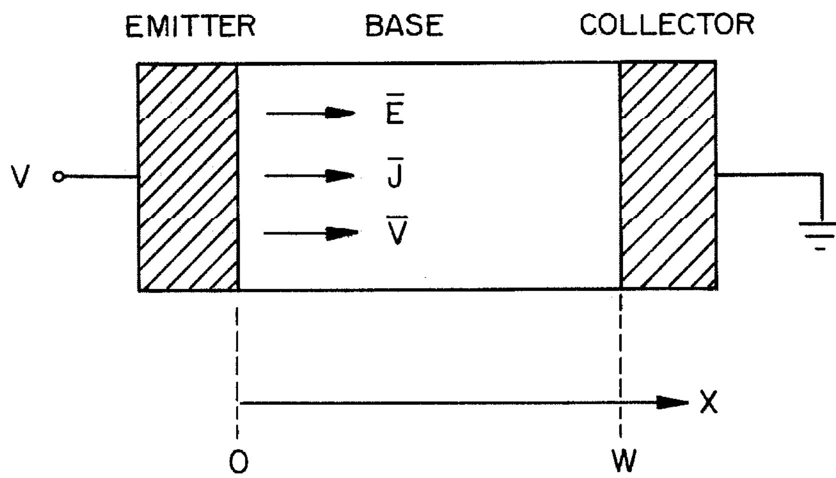


Figure 1.1. A one-dimensional model for a solid-state diode.

into the vacuum corresponds to the emitter, and the anode to the collector.

The model described here is called a solid-state diode. It will be used to study scl current in solids.

1.2 Properties of the Idealized Solid-State Diode. To obtain a simple theory for space-charge-limited current in solids, it is necessary to consider an idealized solid-state diode. Its properties are as follows:

1. The emitter is an infinite source of holes and the collector an ideal sink.

2. The resistivity of the solid is infinite.

3. There are no traps, no recombination centers, no defects of any kind in the solid.

4. The injected charge carriers are transported through the solid by drift only.

5. The drift velocity is directly proportional to the electric field.

1.3 Voltage-Current Relationship. When a voltage V is applied at the emitter an electric field will be established in the solid. If this voltage is positive then the holes injected into the base will be transported by the electric field to the collector. The transport velocity v of the holes is directly proportional to the electric field E and the proportionality constant is μ which is called

the hole mobility in the solid, as indicated in equation 1.1.

$$v = \mu E \tag{1.1}$$

For charges transported in vacuum, the charge carriers act as free particles. In this case, it is the acceleration v of the particle which is directly proportional to the electric field E, as indicated in equation 1.2.

$$\dot{v} = (q/m)E \tag{1.2}$$

From these equations, it is apparent that the analogy between the solid and the vacuum conduction medium is not a direct one.

When injected holes are transported from the emitter to the collector, there is a net current flow. This current is directly proportional to the injected hole charge density $\rho(x)$ within the base and to the transport velocity $v(x)$ of the injected holes, as is expressed in equation 1.3

$$J = \mu(x)\ v\ (x) \tag{1.3}$$

where J is the current density. At steady state, this current density is independent of x and t. The hole transport velocity $v(x)$ is expressed in equation 1.1 as a function of the electric field $E(x)$. Since the holes are injected into an originally charge neutral base, they will establish a space charge within the base by virtue of their charge. The electric field $E(x)$ which is established in the base by the injected charge density

$\rho(x)$ is given by Poisson's equation

$$\frac{dE(x)}{dx} = \frac{\rho(x)}{\epsilon\epsilon_o} \tag{1.4}$$

or

$$\frac{d^2\psi(x)}{dx^2} = -\frac{\rho(x)}{\epsilon\epsilon_o} \tag{1.5}$$

where $\psi(x)$ is the potential with respect to the collector, and ϵ the relative dielectric constant. Since an ideal emitter is considered, the electric field is zero at $x = 0$. The appropriate boundary conditions for determining the current-voltage relationship for the solid-state diode thus are:

$$\mathbf{E}(0) = 0, \text{ and } \quad \psi(0) = V. \tag{1.6}$$

By manipulating equations 1.1, 1.3, 1.4 and 1.5 in a straight forward manner and by applying the given boundary conditions, the current-voltage relationship can be determined and is expressed as follows:

$$J = \frac{9}{8}\frac{\epsilon\epsilon_o\mu}{W^3}V^2 \tag{1.7}$$

This result was first derived by Mott and Gurney (2). In equation 1.7 the current density J is directly proportional to the square of the applied voltage V and to the hole mobility μ, and inversely proportional to the cube of the base width W.

The corresponding current-voltage relationship for

the vacuum tube diode is expressed in equation 1.8 in which the current density J is directly proportional to the three-halves power of the applied voltage V and inversely proportional to the square of the width of the vacuum conduction medium W. This equation is known as Child's three-halves power law. The difference between the two current-voltage relationships stems from the difference in the transport velocity-electric field relationship expressed in equations 1.1 and 1.2.

$$J = \frac{4}{9}\left(\frac{2q}{m}\right)^{1/2} \frac{\epsilon_o}{W^2} V^{3/2} \qquad (1.8)$$

1.4 Impedance. The small signal impedance of the idealized solid-state diode has been calculated by Shao and Wright (8). Their results, along with those for the vacuum tube diode, will be presented in section 3.4 of this chapter where they will be compared with the results to be derived for the germanium solid-state diode.

2. Discussion on Space-Charge-Limited Current in Practical Solids

2.1 Insulators. It is of interest to modify the model of the idealized solid-state diode to include the electrical properties of practical solids. One of the stated conditions is that the resistivity of the solid be

infinite. This would restrict the consideration to insulators that have a wide band gap. Good insulators have resistivities of the order of 10^{12} Ω -cm. Another stated condition is that there be no traps, no recombination centers, no defects of any kind in the solid. However, it is a well known fact that wide band gap materials usually have large densities of traps. Finally, it is necessary to make injecting and collecting contacts to the solid. This presents a rather severe restriction on the electron affinity of the insulator and the work function of the metal contact. Often surface states prevent a large scale injection of charge carriers into the insulator. From these considerations it is evident that the theoretical treatment of practical scl current is more complex than already presented.

Experiments have been performed by Rose and Smith (6) and Wright (7) on CdS to which they succeeded in making injecting and collecting contacts. They were able to show, after taking into account the trapping mechanisms within CdS, that there is a square law dependence between the injected current and the applied voltage. This is an important result in that it indicates that space-charge-limited current can indeed flow through insulators.

To show that there is a direct correlation between theory and experiment, it is necessary to know how the injecting contact functions, what the effective width of the base is, and what the bulk electrical properties of the

solid are to at least a reasonable degree of accuracy. CdS at the present state of the technological art satisfies only the first condition and yet it is the only insulator in which scl current has been extensively studied. For these stated conditions to be satisfied, narrower band gap elemental materials such as germanium and silicon appear much more desirable.

2.2 Semiconductors (Germanium and Silicon). It would seem that the selection of semiconductors as practical solids in which scl current could be studied would be a serious violation of the restriction that the resistivity of the material be very large. However, this is not as severe a violation as one may believe. It will be shown in section 3 of this chapter that the important parameter is not the conductivity due to the majority mobile charge carrier density, but the conductivity due to the minority mobile charge carrier density. Since the density of the minority mobile charge carriers is exponentially temperature dependent, it is possible to reduce greatly their density by lowering the ambient temperature. In this way the bulk resistivity that is related to the minority mobile charge carrier density could be made very large.

From a large class of semiconductors only germanium and silicon appear to be the most suitable practical solids for consideration for the following reasons: there is a

large inventory of available information about the electrical properties of these two semiconductors that can be put to good use; the technological art of growing pure germanium and silicon crystals is highly developed in comparison with that of other materials; finally, the technology of fabricating p-n junctions is also more advanced.

The appropriate semiconductor structure in which scl current can be studied is an alloyed p-n-p structure in which the conductivity of the p-regions is much higher than that of the n-region. This makes it possible to consider one of the alloyed p-n junctions as an emitter and the other as a collector. The width of the solid conduction medium is the separation distance between the two alloyed p-n junctions. This p-n-p structure is the solid-state diode to be considered. Since the technology of germanium differs from that of silicon and since the solid-state diode had to be fabricated in the laboratory (see chapter II), only germanium has been considered.

In the practical solid-state diode to be studied, there are two important features that differentiate it from the ideal solid-state diode. First, the impurity doping in the n-type germanium must be accounted for as will be shown in section 3. Second, the mobility of the mobile charge carriers in the base is not independent of the electric field, as will be shown in the following section.

2.3 Field Dependent Mobility in Germanium. In the theory of scl current in an idealized solid, it is assumed that the mobility of holes or electrons is constant, that is, the drift velocity of mobile charge carriers is directly proportional to the electric field. This consideration is valid in practical solids such as insulators up to very high fields, since the mobility in these solids is low when compared with that of germanium. For materials in which the mobility is high, it takes but a relatively small electric field to give sufficient energy to the mobile charge carriers such that these carriers are out of thermal equilibrium with the surrounding solid. These carriers are called "hot" carriers, and their mobility is field dependent.

Ryder (9) has measured the mobility of holes and electrons in germanium and silicon as a function of the electric field, and found that the drift velocity of the mobile charge carriers is directly proportional to the electric field up to what he calls the critical electric field E_c. In this range the mobile charge carriers are in thermal equilibrium with the solid. For electric fields higher than the critical electric field, the drift velocity is directly proportional to the square root of the electric field. In this range, the mobile charge carriers are not in thermal equilibrium with the solid. Finally, for very high electric fields, the drift velocity ceases to increase further with the electric field and saturates at

the "limiting drift velocity". These results are graphically shown in figure 1.2.

The drift velocity v as a function of the electric field E for low and intermediate electric fields is expressed in equations 1.9 and 1.10, respectively.

$$v = \mu_o E \qquad \text{for } E < E_c \tag{1.9}$$

$$v = \mu_o \left(\frac{E_c}{E}\right)^{1/2} E \qquad \text{for } E_c < E < E_c' \tag{1.10}$$

where μ_o is the low field mobility, and E_c' is the electric field at which the drift velocity saturates. The limiting drift velocity is

$$v = \mu_o (E_c E_c')^{1/2}$$

From equations 1.1 and 1.2 we found that the relationship between the transport velocity and the electric field resulted in a different current-voltage dependence for the scl current in solid and vacuum. If the problem of scl current in germanium is to be solved, it is necessary to include the effect of the field dependent mobility. Before presenting the solution to the problem outlined, we will first describe the salient operating features of the germanium solid-state diode.

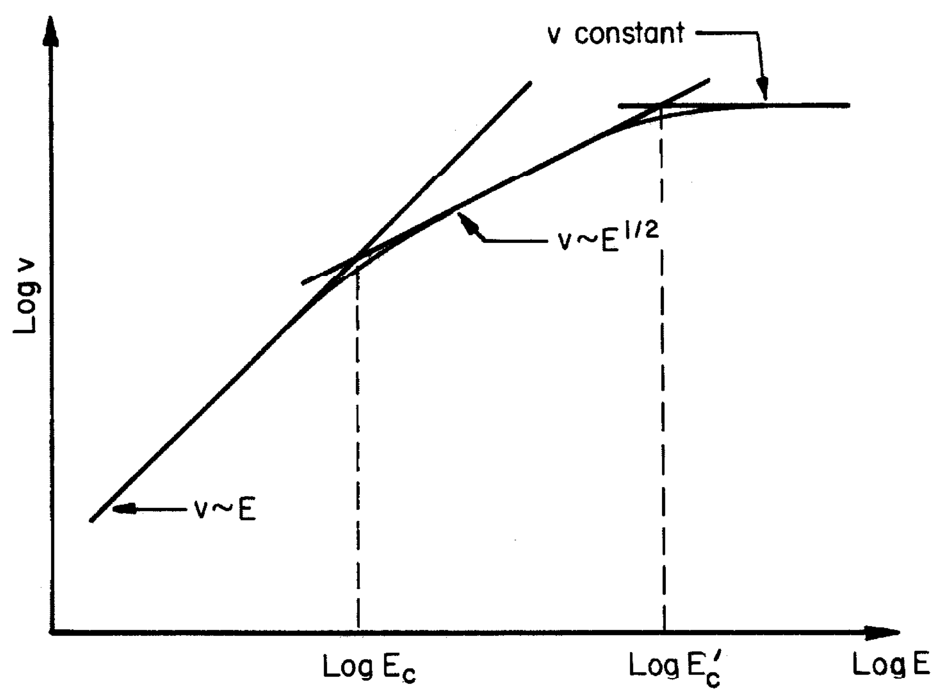


Figure 1.2. A graphical representation of the drift velocity v of a charge carrier in germanium and silicon as a function of the electric field E.

3. Theory of Space-Charge-Limited Current in Germanium

3.1 Germanium P-N-P Structure as a Solid-state Diode.

The germanium solid-state diode considered is an alloyed p-n-p planar structure in which the n-region is of much lower conductivity than the alloyed p-regions. The one-dimensional model for the structure is shown in figure 1.3a, which is the same representation as that used for the ideal solid-state diode.

When a positive voltage is applied, the emitter junction becomes forward biased whereas the collector junction becomes reverse biased. The mode of operation is essentially that of a junction transistor with floating base. Nearly all of the applied voltage appears across the reverse-biased collector and generates a depletion region in the base. The current is proportional to the saturation current of this junction. Upon further increase of the applied voltage the depletion region will eventually extend throughout the base. This "punching-through" will occur at a particular applied voltage V_{pt} which is called the "punch-through" voltage. A base region in the sense of the simple transistor model no longer exists. For applied voltages slightly larger than the punch-through voltage, the current increases rapidly because the additional electric field can be sustained only by mobile charge carriers (holes) injected into the base from the emitter. As long as their density

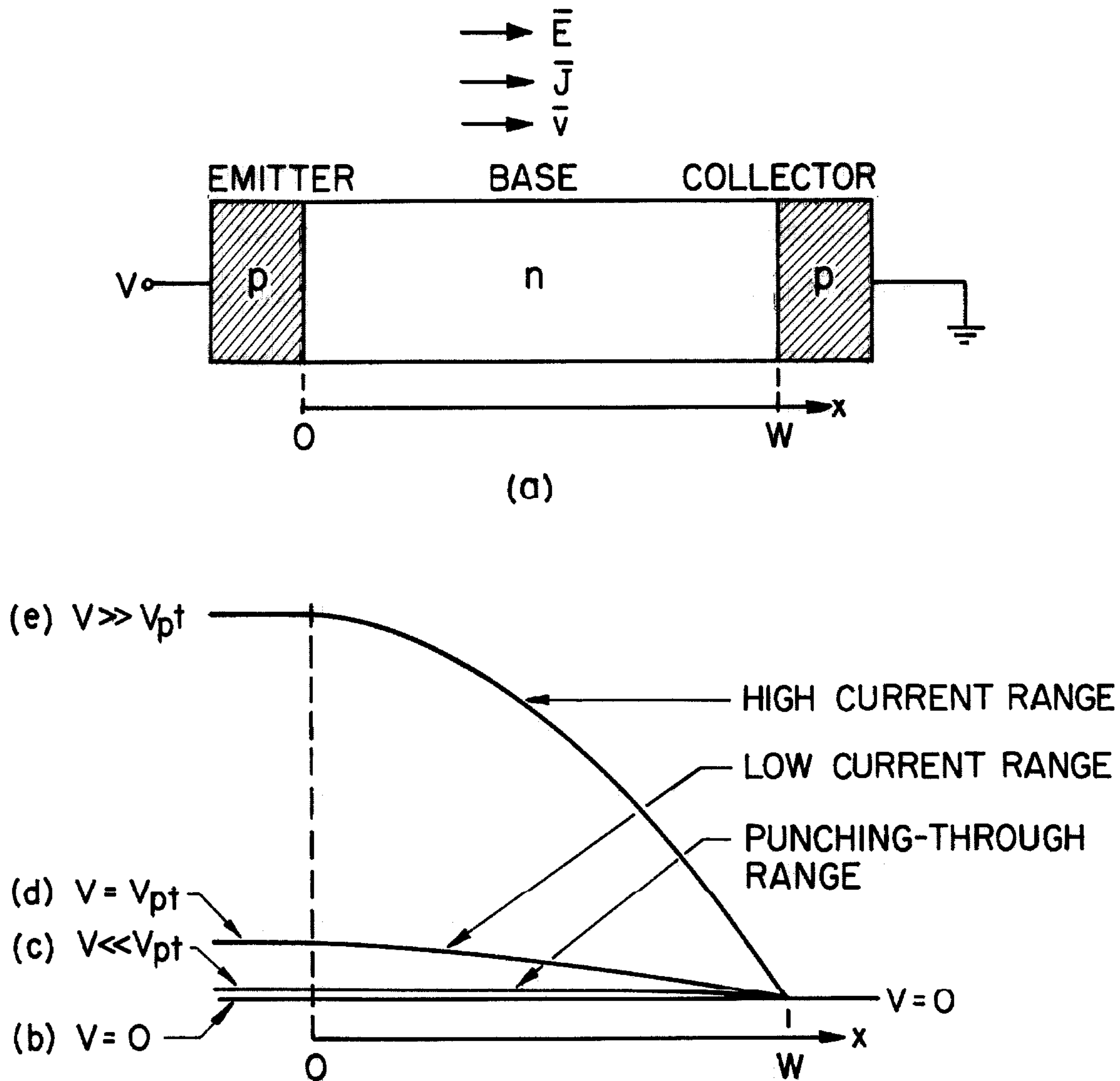


Figure 1.3. An alloyed p-n-p germanium solid-state diode: (a) a one-dimensional model, and a sketch of the potential distribution for (b) $V = 0$, (c) $V \ll V_{pt}$, (d) $V = V_{pt}$, and (e) $V \gg V_{pt}$.

is small compared with that of the fixed ionized donors in the base, this additional electric field is negligible compared with that due to the donor ions.

The fast increase in current ends when the additional electric field becomes dominant. The holes injected into the base finally outnumber the donor ions. It is then that the current becomes fully space-charge-limited.

There exist three distinct ranges of operation. In the first range, the applied voltage is less than the punch-through voltage and is referred to as the *punching-through range*. In the second range, the applied voltage is slightly larger than the punch-through voltage. The current increases rapidly, but the injected hole density is less than the donor ion density. This range is referred to as the *low current range*. In the third range the injected hole density is so large that the donor ion density can be neglected. This is referred to as the *high current range*. These three ranges are sketched in figures 1.3 and 1.4. A more detailed analysis follows.

3.2 Three Ranges of Operation. In this section the current-voltage relationships will be derived for the three ranges of operation. The following assumptions are made in addition to that of planar geometry:

1. The width W_t of the transition region at thermal equilibrium is negligible compared with the base width W.

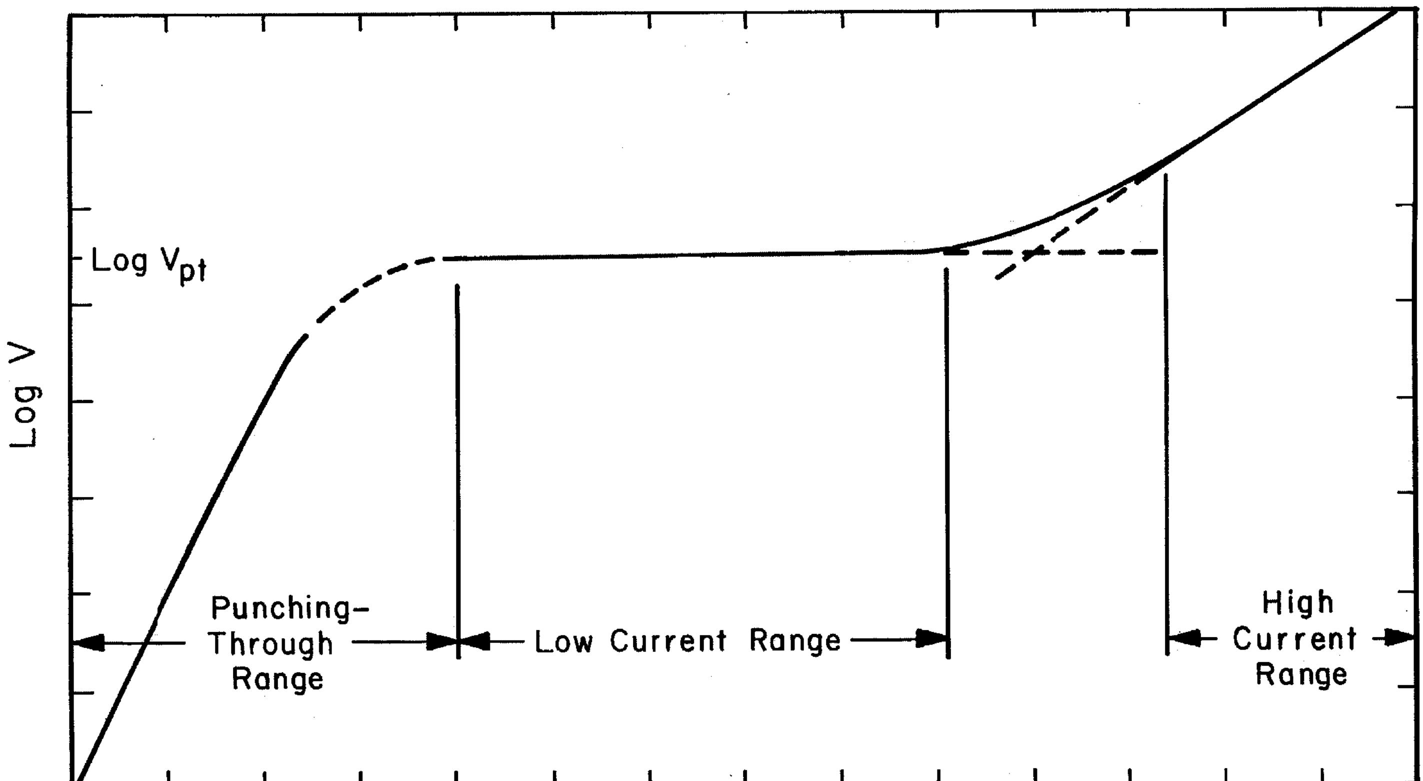


Figure 1.4. A sketch of the V-I characteristic of a germanium solid-state diode showing the three ranges of operation.

2. The built-in voltage V_j of the p-n junction at thermal equilibrium is negligible compared with the punch-through voltage V_{pt}.

In the low and high current ranges, it is also assumed that:

3. The electric field at the emitter is zero (ideal emitter).
4. Current flow is by drift only.
5. The effect of traps, recombination centers or defects of any kind is negligible.

<u>3.2a Punching-Through Range.</u> According to the theory of a reverse-biased abrupt (alloyed) p-n junction, the depletion layer in the lightly doped n-type base for an applied voltage V has a width Y where

$$V + V_j = \frac{qN_D}{2\,\epsilon\epsilon_o} Y^2 \tag{1.11}$$

V_j is the built-in potential of the junction and N_D the donor ion density. For a p-n-p structure of metallurgical base width W, punch-through is reached when $Y = W - W_t$. Hence

$$V_{pt} + V_j = \frac{qN_D}{2\,\epsilon\epsilon_o} (W - W_t)^2 \tag{1.12}$$

For the model of figure 1.3 this equation reduces to

$$V_{pt} = \frac{qN_D}{2\,\epsilon\epsilon_o} W^2 \tag{1.13}$$

since V_j and W_t are neglected. If it is assumed that charge

carrier generation in the depletion region is the dominant factor in the saturation current, then it is expected to be proportional to $Y \sim V^{1/2}$ (10) for $V < V_{pt}/10$. The analysis of the current dependence in the vicinity of punch-through is complex and has, to our knowledge, never been attempted. For a clear observation of the following range, however, the essential condition is that this saturation current does not appreciably increase until immediately prior to punch-through.

3.2b The High Current Range. This range of operation is identical to that of the idealized solid-state diode except that the hole mobility is field dependent. It is assumed that the current flow is by drift only. For this case the hole transport velocity $v(x)$ is expressed as a function of the electric field $E(x)$ (see section 2.3) as follows:

$$v(x) = \mu_o E(x) \tag{1.14}$$

for $x < x_o$, where $E(x_o) = E_c$, and

$$v(x) = \mu_o \left(\frac{E_c}{E(x)}\right)^{1/2} E(x) \tag{1.15}$$

for $x > x_o$, where $E(W) < E_c'$. The current-voltage relationship that results from the consideration of the field dependent mobility is

$$J = \frac{9}{8}\frac{\epsilon\epsilon_o\mu_o}{x_o^3}\left(V - \psi(x_o)\right)^2 \tag{1.16}$$

for $x \leqslant x_o$, and

$$J = \frac{2}{3}\left(\frac{5}{3}\right)^{3/2}\frac{\epsilon\epsilon_o\mu_o E_c^{1/2}}{W^{5/2}} V^{3/2}\left(\left(1 + \frac{1}{3}\frac{E_c^2}{E_1^2}\right)^{5/3} - \frac{1}{6}\left(\frac{4}{3}\frac{E_c^2}{E_1^2}\right)^{5/3}\right)^{-3/2} \tag{1.17}$$

for $x \geqslant x_o$, where

$$E_1 = \left(\frac{2JW}{\epsilon\epsilon_o\mu_o}\right)^{1/2} \tag{1.18}$$

Equation 1.16 represents the current-voltage relationship in the region where the hole mobility is not field dependent. In this region a square dependence between the voltage and current exists as in the case of the idealized solid-state diode. A deviation from the idealized solid-state diode resulting from the field dependent mobility is apparent in equation 1.17. Here E_1 is the electric field that would have been present at the collector had the mobility not been field dependent.

The electric field at the collector is always directly proportional to the net charge per unit cross-sectional area in the base. When holes are injected, then the net charge in the base is always greater than that due to fixed donor ions which is qN_DW. Thus, in the presence of scl current E_1 is always larger than E_2, where

$$E_2 = \frac{qN_D}{\epsilon\epsilon_o} W \tag{1.19}$$

Even for the most stringent case to be considered ($N_D = 10^{13}$ donor ions cm^{-3}, $W = 8.3\,\mu$, $T = 78^\circ$ K) $E_2 = 947$ V/cm and $E_c = 21$ V/cm. This indicates that the terms $(E_c/E_1)^2$ in equation 1.17 are much less than unity and can be neglected. Thus for practical considerations this equation, which was first derived by Dacey (4), can be expressed as

$$J = \frac{2}{3}\left(\frac{5}{3}\right)^{3/2} \frac{\epsilon\epsilon_o \mu_o E_c^{1/2}}{W^{5/2}} V^{3/2} \tag{1.20}$$

An identical result could have been obtained directly if the field dependent mobility had been assumed to hold everywhere in the base.

When the mobility becomes field dependent then the current-voltage relationship derived by Mott and Gurney (2) is no longer valid. According to equation 1.20 the current is directly proportional to the three-halves power of the applied voltage and inversely proportional to the five-halves power of the base width.

3.2c Low Current Range. In this range, the voltage is nearly constant and essentially equal to the punch-through voltage V_{pt}. The current, however, changes rapidly from values of the order of the saturation current in the punching-through range to values of the order of the scl

current in the high current range.

In the transition from the low to the high current range, the space charge of both the fixed ions and the injected charge carriers has to be considered. With the assumption that the field dependence of the mobility $\mu = \mu_o(E_c/E)^{\frac{1}{2}}$ holds throughout the base, Dacey (4) has arrived at the following parametric representation for the V-I characteristic

$$V = V_{pt}\frac{(3e^{2u} - 16e^{3u/2} + 36e^{u} - 48e^{u/2} + 6u + 25)}{3(e^{u} - 4e^{u/2} + u + 3)^2} \qquad (1.21)$$

$$J = 1.98\ J_{pt}(e^{u} - 4e^{u/2} + u + 3)^{-1/2} \qquad (1.22)$$

where u takes on positive values from zero to infinity, and J_{pt} is the current density for the applied voltage V_{pt} if there are no donor ions present in the base. The result of a numerical evaluation of this dependence is shown in figure 1.5 where the voltage is normalized with respect to the punch-through voltage V_{pt} and the current with respect to J_{pt}. When u tends toward infinity, the voltage approaches V_{pt} asymptotically while the current exponentially decreases with u. When u tends toward zero, the V-I characteristic approaches that of the fully scl current.

The parameter u can be expressed as $u = qN_D\mu_oT/\epsilon\epsilon_o$ where T is the time that charge carriers of constant mobility μ_o would take to traverse the base in the presence

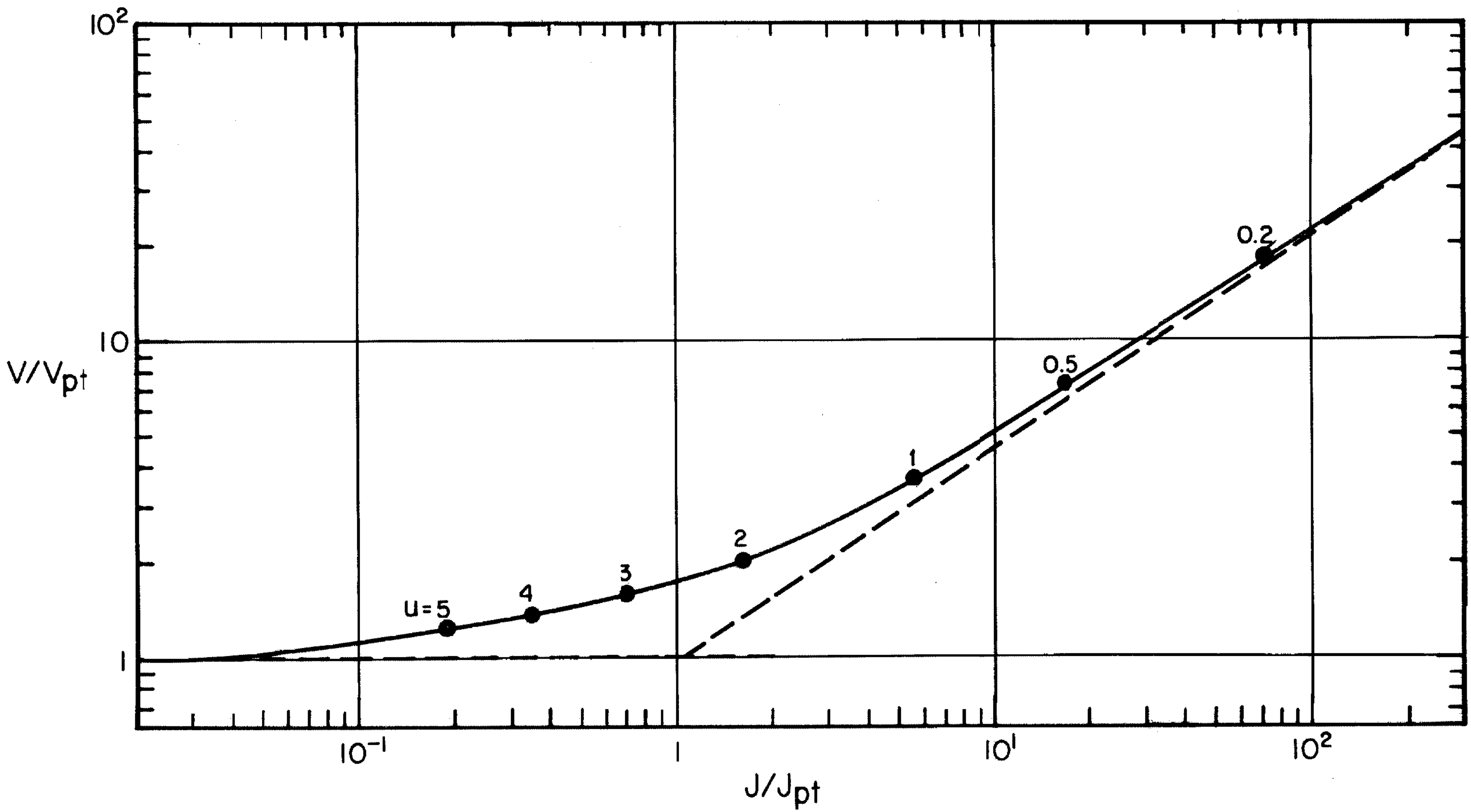


Figure 1.5. A theoretical normalized V-I characteristic for scl current in a germanium p-n-p solid-state diode.

of the actual field. The condition $u \ll 1$ for the presence of pure scl current therefore requires that

$$\frac{qN_D W}{\epsilon\epsilon_o} \ll \frac{W}{T\mu_o}$$

This expression shows that the average value of the electric field in the base must be much less than the electric field at the collector at punch-through. This inequality will be satisfied provided the injected charge carriers dominate over the fixed ions as indicated in section 3.2b.

3.3 Temperature Dependence. In the high current range the current density is proportional to the mobility of the hot holes. This mobility $\mu(T)$ is a function of the ambient temperature* T as expressed in the following equation.

$$\mu(T) = \mu_o(T) \left(\frac{E_c(T)}{E}\right)^{1/2} \tag{1.23}$$

The low-field mobility $\mu_o(T)$ as a function of the ambient temperature T is

$$\mu_o(T) = AT^{-3/2} \tag{1.24}$$

---

*The ambient temperature is that of the crystal and not of the hot holes.

where A is a constant. This equation is valid when the holes are predominantly scattered by the lattice. The mobility of the hot charge carriers for the same scattering mechanism has been studied by Shockley (11). He considers two limiting energy distributions of the hot charge carriers. For the Boltzmann energy distribution he obtains

$$E_c(T) = 1.84 \frac{c}{\mu_o(T)} \tag{1.25}$$

For the discrete energy distribution he obtains

$$E_c(T) = 1.03 \frac{c}{\mu_o(T)} \tag{1.26}$$

In both equations, c is the group velocity of the longitudinal acoustical waves in the lattice. He also considers an intermediate case for which he obtains

$$E_c(T) = 1.51 \frac{c}{\mu_o(T)} \tag{1.27}$$

By combining equations 1.23, 1.24 and 1.27 the mobility of hot holes as a function of the ambient temperature is obtained. From this result the current-voltage relationship can be derived as a function of the ambient temperature and is expressed as follows:

$$J = \frac{2}{3}\left(\frac{5}{3}\right)^{3/2} \frac{\epsilon\epsilon_o(1.51cA)^{1/2}\, T^{-3/4}}{W^{5/2}} V^{3/2} \qquad (1.28)$$

In this equation the current density is inversely proportional to the three-fourths power of the ambient temperature.

3.4 Impedance. The small signal impedance of the solid-state diode with field independent mobility has been derived by Shao and Wright (8). In appendix A this impedance is determined for a field dependent mobility of the form $v = \mu E_c(E/E_c)^{1/n}$. The result is given in table 1.1. The impedances of the idealized solid-state diode ($n = 1$), of the germanium solid-state diode in the full scl current range ($n = 2$), and of the vacuum tube diode are included for comparison.

It is seen that the values of the equivalent parallel capacitance C_1 for the cases of $n = 1$ and $n = 2$ differ by a ratio of $3/4 : 5/7 = 1.05$. The corresponding ratio for the equivalent ac resistance R_1 is $1/3 : 2/5 \simeq 0.83$. For values of n larger than 2 these ratios do not change significantly, since for $n \to \infty$, the corresponding ratios are 9/8 and 2/3. It is thus found that the value of the equivalent parallel capacitance of the small-signal impedance of space-charge-limited currents is only slightly affected by the mobility variations considered. The same

TABLE 1.1

$\omega T_o < \pi$	Vacuum (reference 26)	Solid (reference 8)		
Field-Velocity relationship	$\dot{v} = \frac{q}{m} E$	$v = \mu E$	$v = \mu (E_c E)^{1/2}$	$v = \mu E_c (E/E_c)^{1/n}$
dc transit time T_o	$\left(\frac{6d\epsilon_o m}{qj_o}\right)^{1/3}$	$\left(\frac{2d\epsilon\epsilon_o}{\mu j_o}\right)^{1/2}$	$\left(\frac{9d^2\epsilon\epsilon_o}{4\mu^2 E_c j_o}\right)^{1/3}$	$\left(\left(\frac{n+1}{n} d\right)^n \frac{\epsilon\epsilon_o}{\mu^n E_c^{\,n-1} j_o}\right)^{1/(n+1)}$
dc resistance R	$\frac{3}{4} \cdot \frac{T_o}{C_o}$	$\frac{2}{3} \cdot \frac{T_o}{C_o}$	$\frac{3}{5} \cdot \frac{T_o}{C_o}$	$\frac{n+1}{2n+1} \cdot \frac{T_o}{C_o}$
ac resistance R_1	$\frac{1}{2} \cdot \frac{T_o}{C_o}$	$\frac{1}{3} \cdot \frac{T_o}{C_o}$	$\frac{2}{5} \cdot \frac{T_o}{C_o}$	$\frac{n}{2n+1} \cdot \frac{T_o}{C_o}$
Equivalent parallel ac capacitance C_1	$\frac{3}{5} \cdot C_o$	$\frac{3}{4} \cdot C_o$	$\frac{5}{7} \cdot C_o$	$\frac{2n+1}{3n+1} \cdot C_o$

conclusion holds for the ac resistance R_1 of the small-signal impedance (as well as for the dc resistance R) as long as changes in the dc transit time T_o are accounted for explicitly.

These conclusions must be applied with caution. In practical cases, the mobility does not obey laws of the form $v = \mu E_c(E/E_c)^{1/n}$. For the range $0 < E < E_c$, a linear relation holds. In view of the present results, it seems likely that this more complex case will not exhibit properties which deviate significantly from those of the simple case with constant mobility. However, a more detailed analysis than the present one is needed to fully support this statement.

3.5 Discussion on Validity of Assumptions. The punch-through voltage V_{pt} is directly proportional to W^2 provided W is much larger than the width W_t of the transition region of the junction at thermal equilibrium. It is difficult to accurately evaluate W_t in near-intrinsic materials, but an estimate indicates that at liquid nitrogen temperature, W_t must be of the order of a few microns in germanium (12). The dependence of V_{pt} on W^2 is thus expected to break down at base widths of the order of 10 μ. An adequate theory for the current in the punching-through range as the applied voltage approaches V_{pt} is not available. However, even the simple model of a transistor in floating

base operation is sufficient to indicate that the current in the punching-through range will increase very rapidly with increasing temperature. Ultimately, there may be no distinction between this range and the low current range.

The effect of diffusion on the V-I characteristic for a solid-state diode in which the mobility is field independent has been considered by Lindmayer et al. (13). They find that for injection densities at the emitter larger than $p_e = 10^8\ W^2/cm^3$, where W is in cm., the V-I characteristic can be derived directly by assuming that the charge transport through the solid is by drift only. If it is assumed that this condition also holds for field dependent mobility, then for our thickest sample with W = 0.0107 cm p_e is approximately 10^4 holes/cm^3. But in the high current range, the injected hole density at the emitter is always greater than the 10^{13} donor ions/cm^3 in the base. The factor of 10^9 clearly indicates that the effect of diffusion on the V-I characteristic is negligible.

Since it is assumed that the electric field at $x = 0$ is zero in the low and high current range, the potential maximum must occur at $x = 0$. However, in the actual case the potential distribution in the base will exhibit a maximum in the vicinity of, but not at, $x = 0$. Hence the effective width of the conduction medium, which is the distance from this potential maximum ("virtual emitter") to

the collector, is less than the base width W. To determine the exact location of this virtual emitter is difficult. Therefore the following qualitative analysis is used. The current flow in the vicinity of the virtual emitter is essentially by diffusion. The hole density gradient at the potential maximum will be $(1/qD_p)J$ which is of the order of 1.3×10^{17} J cm^{-4}, where J is the current density in a/cm^2 and D_p the diffusion constant for the injected holes in cm^2/s. From this result it is evident that in the high current range ($J > 10$ a/cm^2) the density gradient must be higher than $10^{18}/cm^4$. In figure 1.6 the hole density distribution at thermal equilibrium and at high injection in the vicinity of the alloyed p-n emitter junction of the solid-state diode is sketched. The doping density in the p-region and the n-region is 10^{18} acceptors/cm^3 and 10^{13} donors/cm^3, respectively. From the sketch it is evident that hole density gradients of the order of 10^{18} holes/cm^4 at high injection appear within region I of figure 1.6. This is less than $0.8\ \mu$ at 78° K from the metallurgical junction as shown in figure 1.6 where the value of $0.8\ \mu$ corresponds approximately to $2(\epsilon\epsilon_0 kT/2qN_D)^{1/2}$. Thus in the high current range the effective width of the solid conduction medium can be approximated by the base width W provided $W \gg 0.8\ \mu$. In the low current range the potential maximum will be near the edge of the transition region of the

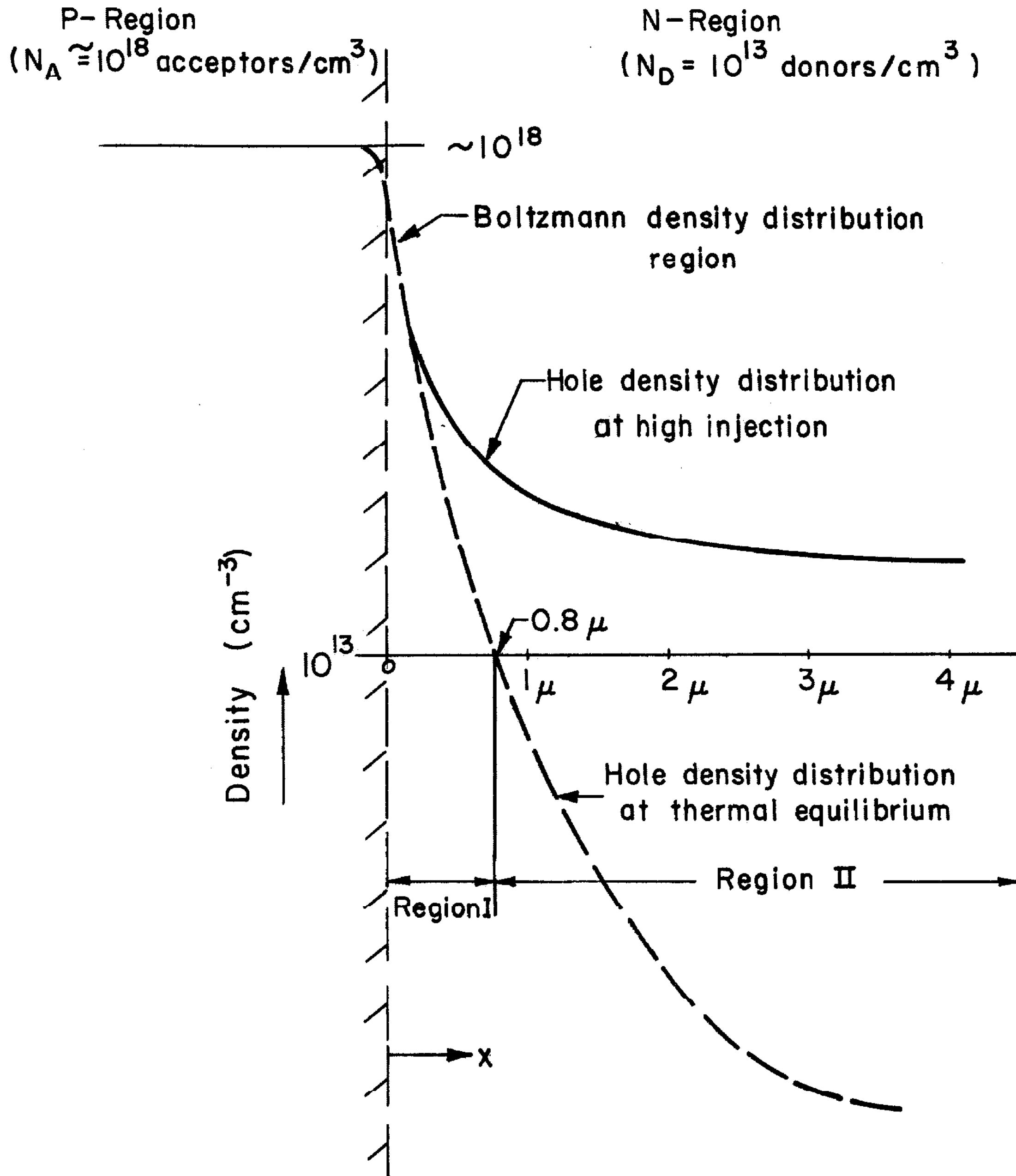


Figure 1.6. A sketch of the hole density distribution in the vicinity of the alloyed p-n emitter of the germanium solid-state diode.

emitter at thermal equilibrium, which is a distance W_t from the metallurgical junction. Thus in the low current range the effective width can be approximated by the base width W provided $W >> W_t$.

A one-dimensional model is assumed for a planar germanium solid-state diode. This assumption is valid provided the ratio of the lateral dimensions to the base width of the solid-state diode is much greater than unity. For the actual solid-state diodes fabricated this ratio is larger than 7.

It has been assumed that the effects of traps, recombination centers, or defects of any kind in the low and high current range are negligible. This assumption appears to be valid for high quality near intrinsic n-type germanium with a doping density as low as 10^{12} donors/cm^3 (4). Our measurements on germanium with a doping density of 10^{13} donors/cm^3 do not indicate the effects of this nature either.

4. Experimental Results

4.1 Fabricated Germanium P-N-P Solid-State Diode. The fabricated germanium solid-state diode (see chapter II, section 3) consists of a near intrinsic n-type wafer on which two parallel and planar p-type regions are alloyed as shown in figure 1.7. These alloyed p-n junctions form abrupt metallurgical contacts with the parent material (see chapter II, section 4). The separation distance between these two contacts represents the base width (see chapter II, section 4.6). The n-region which contains 10^{13} donors/cm^3 (see chapter II, section 1.1) is of a much lower conductivity than the alloyed p-regions which contain approximately 10^{18} acceptors/cm^3 (14). This high density of acceptors makes it possible to consider the p-n injecting junction as an ideal emitter and the p-n collecting junction as a metallic contact. The lateral dimensions of the p-n junctions are made large compared to the base width. From these considerations it is evident that the one-dimensional model discussed in section 3 of this chapter is a good representation of the fabricated germanium solid-state diode.

4.2 Voltage-Current Relationship. The V-I characterization of the fabricated germanium solid-state diode is described in chapter II, section 4.7. The V-I characteristics for two different samples as obtained on an

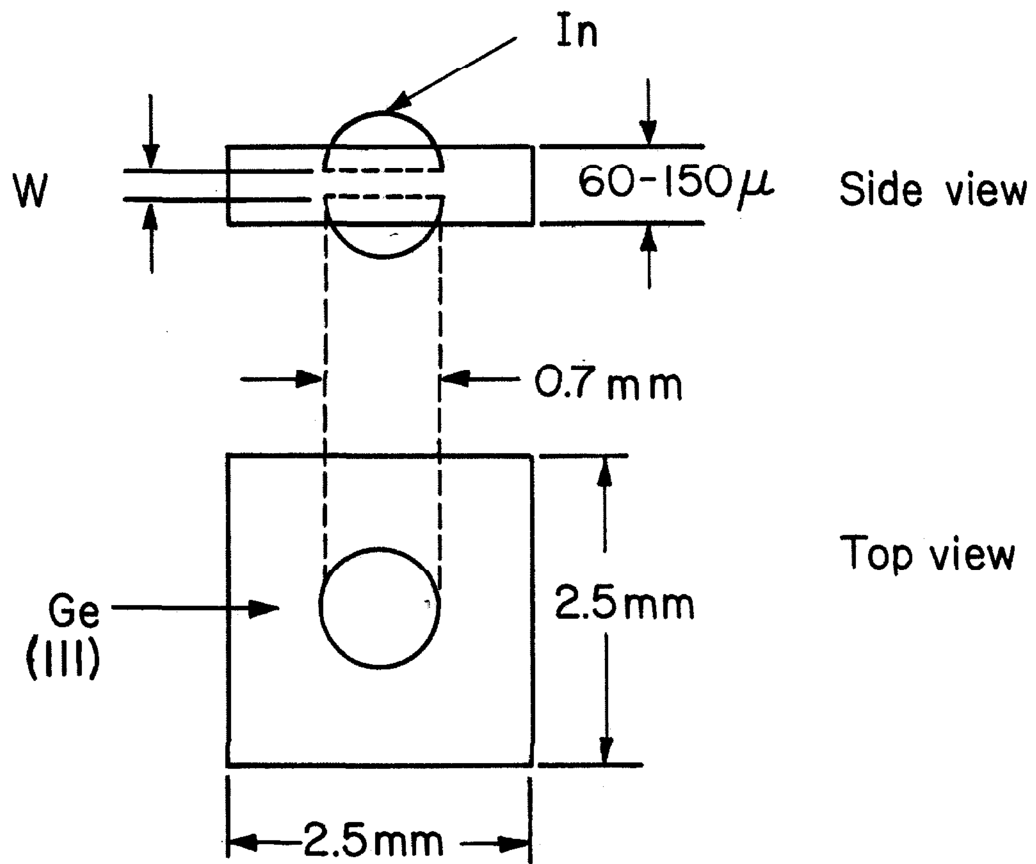


Figure 1.7. A schematic diagram of an alloyed p-n-p germanium structure (not drawn to scale).

oscilloscope display are shown in figures 1.8a and 1.8b. The V-I characteristic in figure 1.8a is of the sample with the narrowest base width (8.3 μ), and it clearly exhibits the operation of the solid-state diode in the high current range. For currents larger than 10 ma, the three-halves power relationship is obeyed as shown in figure 1.10. The maximum current passed through the sample is about 800 ma which is equivalent to 180 a/cm^2. In figure 1.8b the V-I characteristic exhibits very clearly the operation of the solid-state diode in the punching-through range. For voltages less than the punch-through voltage the saturation current is of the order of 1 μa.. This sample which has a 34.7 base-width also exhibits a three-halves power relationship as shown in figure 1.9, but this is at much higher currents than shown in figure 1.8b.

In figure 1.9 the experimental result for a fabricated 34.7 μ base width solid-state diode at an ambient temperature of 78° K is compared with theory. For this sample it is clearly evident that two straight lines can be drawn through the experimental points in figure 1.9: the V = 6.2 volt line (low current asymptote) and the $I \sim V^{3/2}$ line (high current asymptote). Furthermore, if the normalized theoretical curve shown in figure 1.5 is fixed between these two lines an excellent fit between the theoretical curve and the experimental points.

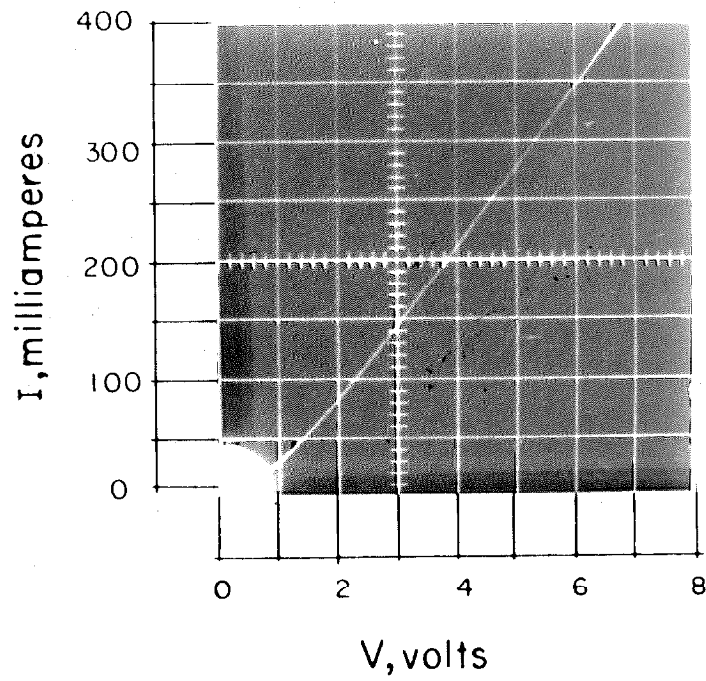


Figure I.8 a An oscilloscope trace of a V-I characteristic of the narrowest base width sample. ($W = 8.3\mu$, $V_{pt} \simeq 0.13V$, and $T = 78°K$)

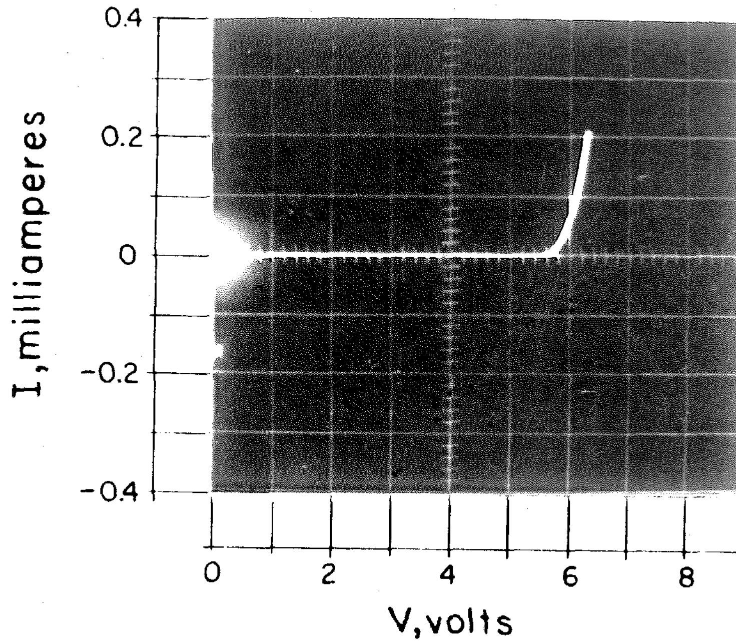


Figure I.8 b An oscilloscope trace of a V-I characteristic of a 34.7 μ base width sample. (V_{pt} = 6.2 V and T = 78°K)

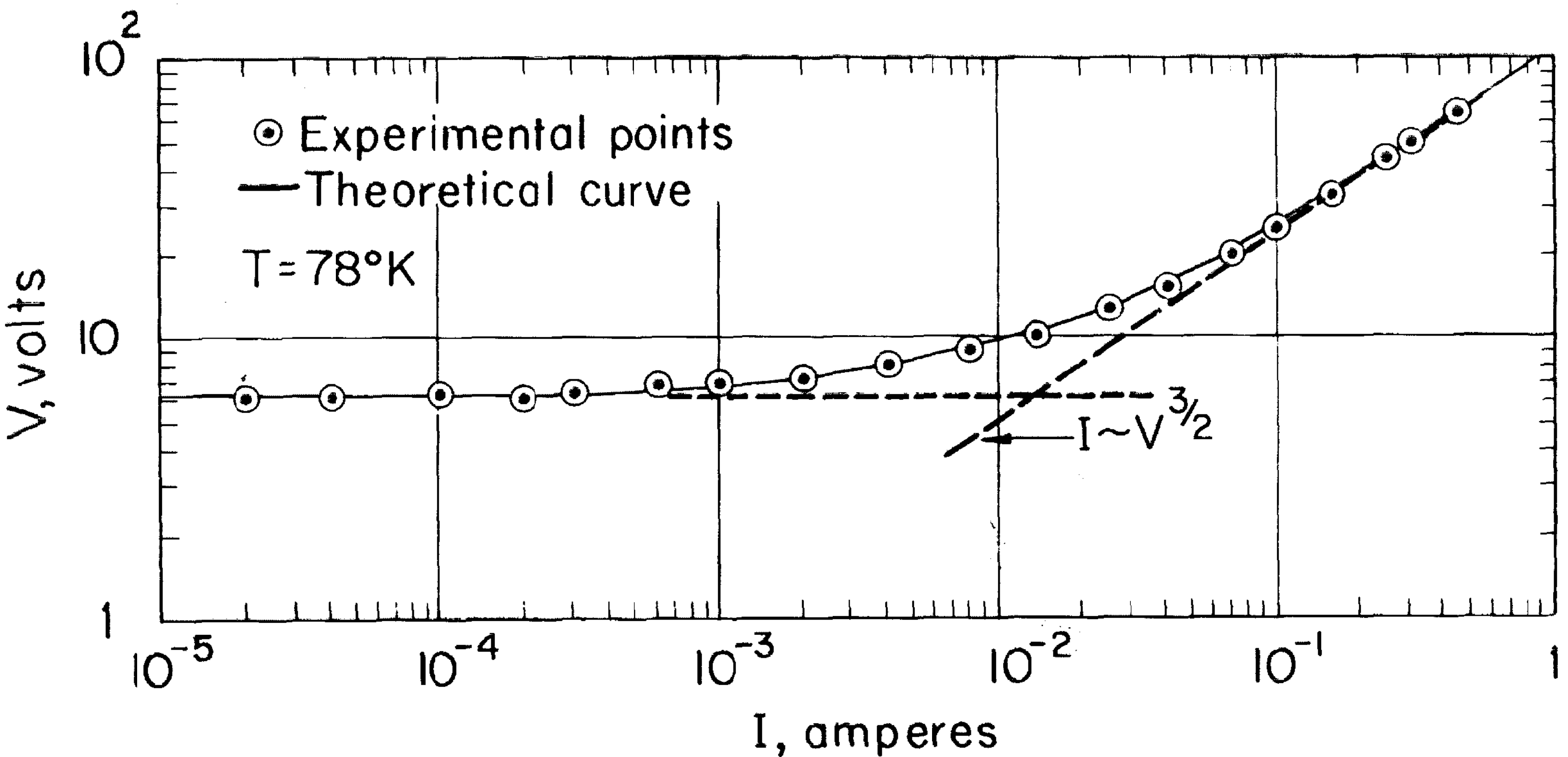


Figure 1.9. A comparison between theory and experiment for scl current in a p-n-p germanium structure at T = 78° K. (W = 34.7 μ, A = 4.24 10^{-3} cm^2, $N_D = 10^{13}$ cm^{-3}, and V_{pt} = 6.24V).

In figure 1.10 the experimental results for the solid-state diodes of various base widths at an ambient temperature of 78° K are given. The low and high current ranges can be represented by two straight lines as indicated in figure 1.9 except for the 8.3 μ and the 17.5 μ samples. For these samples the low current lines are determined by finding the best fit between the theoretical curve and the experimental points. The base width in each sample is indicated in the figure. The junction area and the base width of each sample are given in table 1.2.

TABLE 1.2

Base width 10^{-4} cm	Junction area 10^{-3} cm^2
8.3	4.52
17.5	4.24
27.7	4.31
34.7	4.24
60	4.24
107	4.18

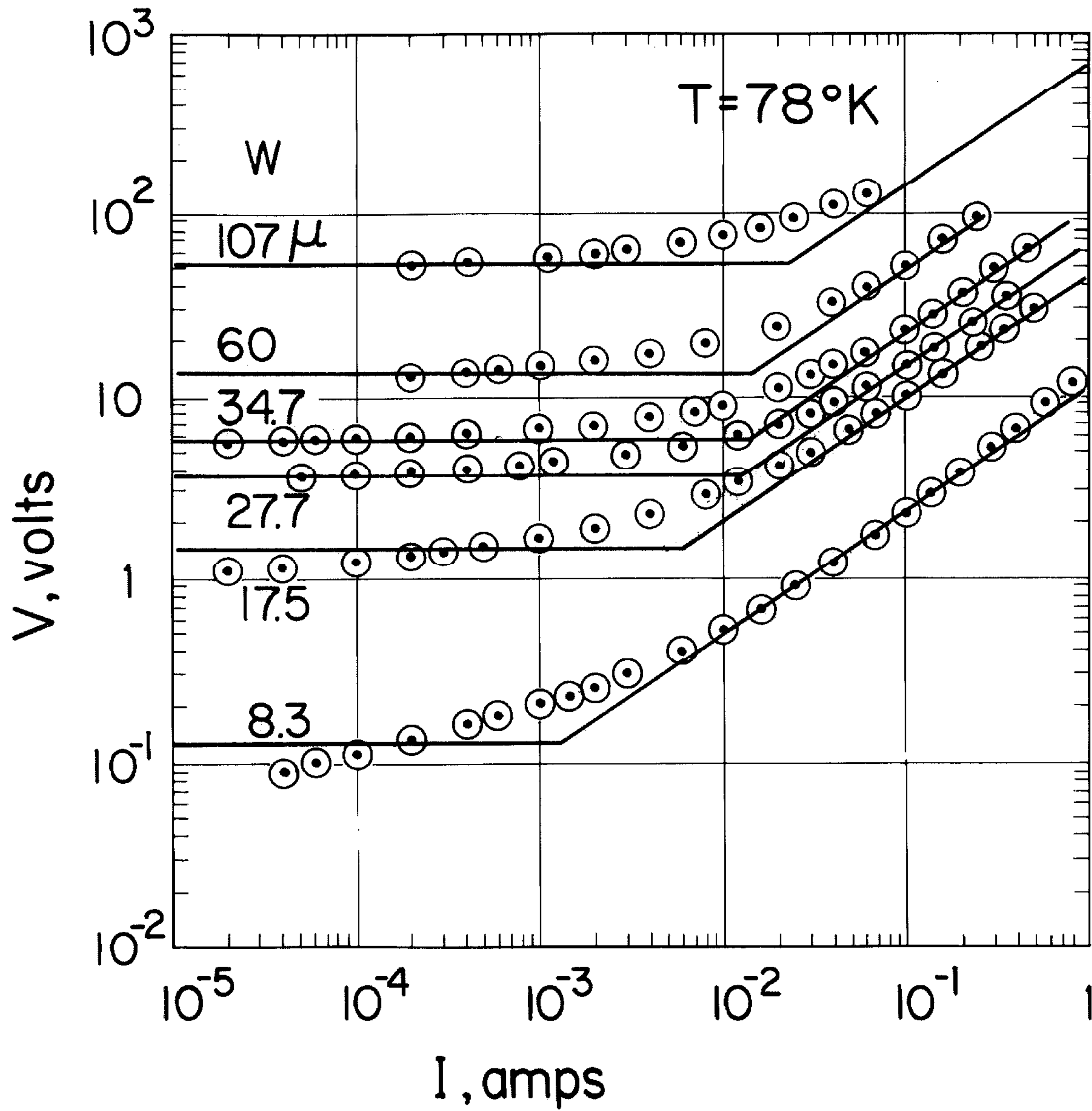


Figure 1.10. V-I characteristics of p-n-p germanium structures of different base widths at $T = 78^{\circ}$ K.

The base width ranges from 8.3 μ to 107 μ and the punch-through voltage ranges from 0.13 V to 55 V. The base width range of more than one order of magnitude and the corresponding punch-through voltage range of more than two orders of magnitude cover a wide range of operation in which the current-voltage characteristics of the fabricated samples are studied.

There are two anomalies observed in the 8.3 μ base width sample. First, in the high current range of this sample, the current-voltage characteristic deviates from the three-halves power relationship in the region in which the electric field at the collector is greater than 10^4 V/cm. It was mentioned in section 2.3 of this chapter that at very high electric fields the drift velocity becomes saturated. When this is the case, the current is directly proportional to the voltage. The tendency of the deviation observed is in the direction expected for saturating drift velocity. The value of 10^4 V/cm for the electric field is that expected from theory (11). Second, for this sample, as well as for the 17.5 μ base width sample, a deviation is also observed at very low currents. The theoretical analysis presented in section 3 of this chapter is based on the assumption that the punch-through voltage is determined by the base width W. This assumption is true as expressed in equation 1.13 provided the width of the transition region

of the emitter and collector junction for zero current is much less than the base width. However, for these samples, particularly for the 8.3 μ sample, this assumption is not valid. In this case a deviation is observed as expected.

The agreement between theory and experiment is excellent and where deviations do occur (for the narrow base width samples), there is valid reason for expecting these deviations. In fact, they tend to demonstrate the necessity of the assumptions made in the theory. The experimental results indicate that for each sample considered there is space-charge-limited current. Furthermore, they conclusively exhibit the two ranges of operation (the low and the high current range).

The only other published measurement of space-charge-limited current in germanium is that of Dacey (4). In his paper he presents the results for only one sample with a base width of 280 μ and a punch-through voltage of 40 V. The maximum current density of 10 a/cm^2 reported was not sufficient to exceed the intermediate current range.

4.3 Base Width Dependence. Another important feature in the theory of scl current is the base width dependence. A convenient way to express this dependence is to rearrange equation 1.20 into the following form

$$V = \left(\frac{(2/3)(5/3)^{3/2} \; \epsilon \epsilon_o \mu_o \; E_c^{1/2}}{J} \right)^{-2/3} \; W^{5/3} \qquad (1.29)$$

From this equation it is seen that if the current density J and the ambient temperature are kept constant, while the base width is allowed to vary, the applied voltage V is directly proportional to the five-thirds power of the base width.

A verification of this dependence is possible. Since there are samples of different base width, all that is necessary is to keep the ambient temperature and the current density constant for all samples and to measure the resulting applied voltages. These voltages can be obtained directly from figure 1.10. The constant current density chosen is 47 a/cm^2. This value is within the three-halves power range for all samples. In figure 1.11a this result is compared with theory.

The agreement between theory and experiment is excellent. Any deviation observed is within the expected experimental error of about 5%. From this result it is concluded that there is indeed the base width dependence as predicted by theory.

There is also a base width dependence at punch-through. In accordance with equation 1.13 the punch-through voltage is directly proportional to the base width squared.

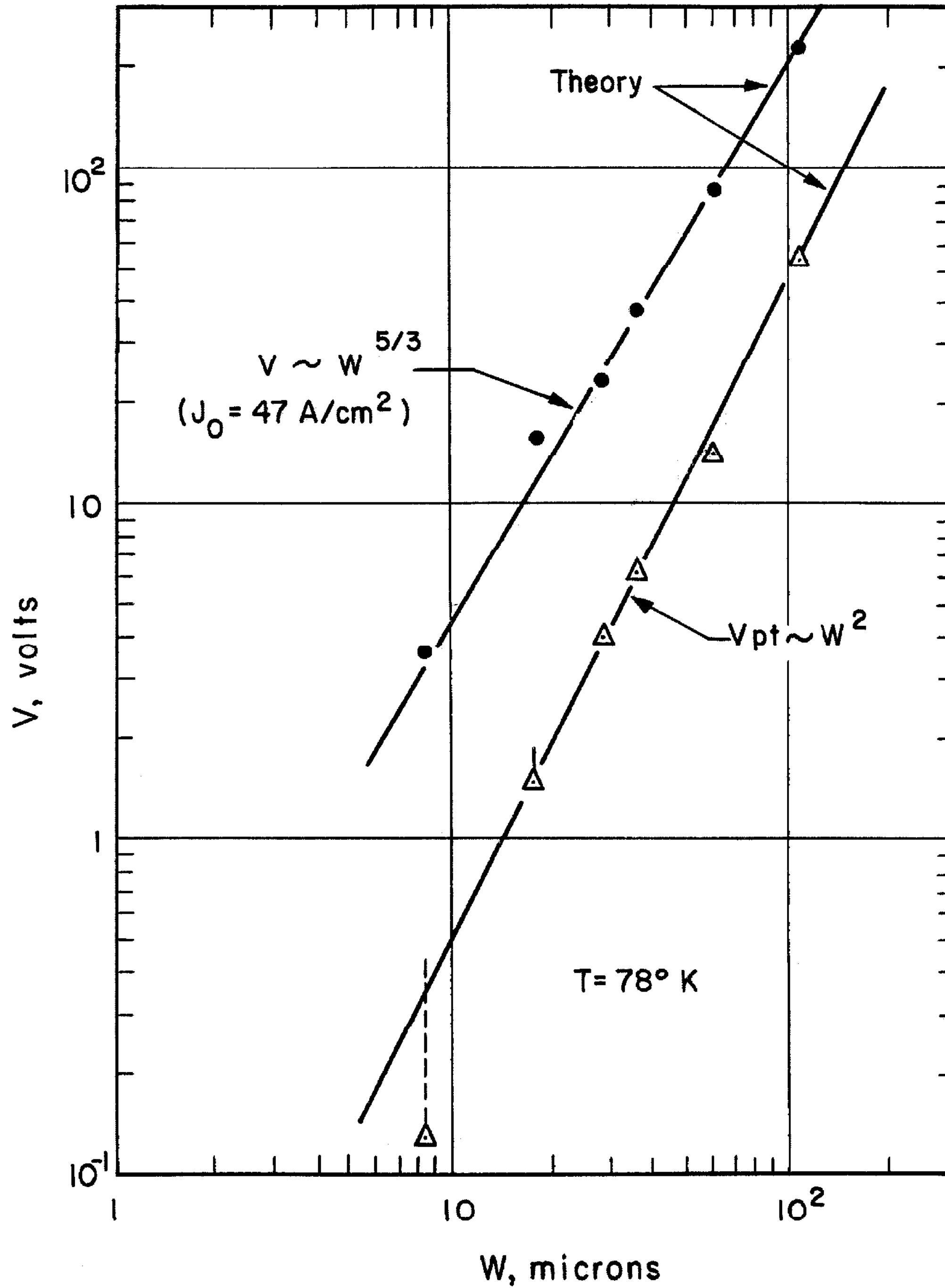


Figure 1.11. A comparison between theory and experiment for (a) scl current ($V \sim W^{5/3}$) (b) punch-through voltage ($V_{pt} \sim W^2$)

This relationship can be checked experimentally by referring to the very low current range in figure 1.10 where the punch-through voltage of each sample is measured. The experimental result obtained in this manner is plotted and compared with theory in figure 1.11b.

The agreement between theory and experiment is excellent for the samples of larger base width. A marked deviation from theory is observed for the 8.3 μ sample. The width of the emitter transition region for zero current is not negligible when compared with base widths of 8.3 μ and 17.5 μ as explained in section 4.2 of this chapter. For this case, and particularly for the 8.3 μ sample, the second power relationship does not hold as expected. For these two samples equation 1.12 cannot be reduced to equation 1.13. Furthermore the transition from the punching-through range to the high current range through the low current range is more rapid for the narrower base width samples. As a result the low current range for the very narrow base width samples may not be clearly defined.

From the experimental result for the punch-through voltage, the donor doping density N_D can be obtained. The value of N_D determined from figure 1.11b is 9.2×10^{12} donors/cm^3. This value agrees within the expected experimental error of approximately 10 percent with that deduced from resistivity measurements.

4.4 Critical Electric Field. The coefficient in the base width - voltage relationship expressed in equation 1.29 can be determined directly from the experimental result in figure 1.11a. Because the low field hole mobility μ_o can be expressed as $\mu_o = 1900 (300/T)^{1.7}$ cm^2/Vs, where T is the ambient temperature (see section 1.1 of chapter II), the critical electric field E_c can be determined from the experimental value of this coefficient. The value so obtained for 78° K is 21 V/cm. Similarly, the critical electric field can be determined from the current-voltage measurements made on a few samples for other ambient temperatures (see following section). These values as well as corresponding theoretical values are given in table 1.3.

The experimental values of the critical electric field in table 1.3 for 195° K and 273° K are the average of three and two samples, respectively. Although the variation in the value of E_c from sample to sample in this temperature range is appreciable, the average value compares favorably with the intermediate theoretical value. At 78° K the value of E_c is based on a much larger number of samples and as a consequence it is more reliable. This value is comparable to the theoretical value for the discrete energy distribution. In all cases, the experimental values of E_c fall within the range of the theoretical values. Ryder's

TABLE 1.3

Ambient Temperature T °K	Critical Electric Field V/cm			
	Theory*			Experiment
	E_{c1}	E_{c2}	E_{c3}	E_c
78	29	43	52	21
195	140	210	250	220(1 ± 0.4)
273	250	360	440	330(1 ± 0.3)

results (9), which are based on conductivity measurements, are more than a factor three higher. Compared to this, the present results are in good agreement with theory.

4.5 Temperature Dependence. In figure 1.12 the voltage-current characteristic of the 34.7 μ sample is plotted for different ambient temperatures to show its effect on scl current. The measurements are described in chapter II, section 4.7.

The important experimental results are: Scl current increases as the ambient temperature decreases for a constant applied voltage. This is the current-temperature

*The theoretical values E_{c1}, E_{c2}, and E_{c3} are for the Boltzmann, the discrete, and the intermediate hot hole distributions respectively (see chapter I, section 3.3).

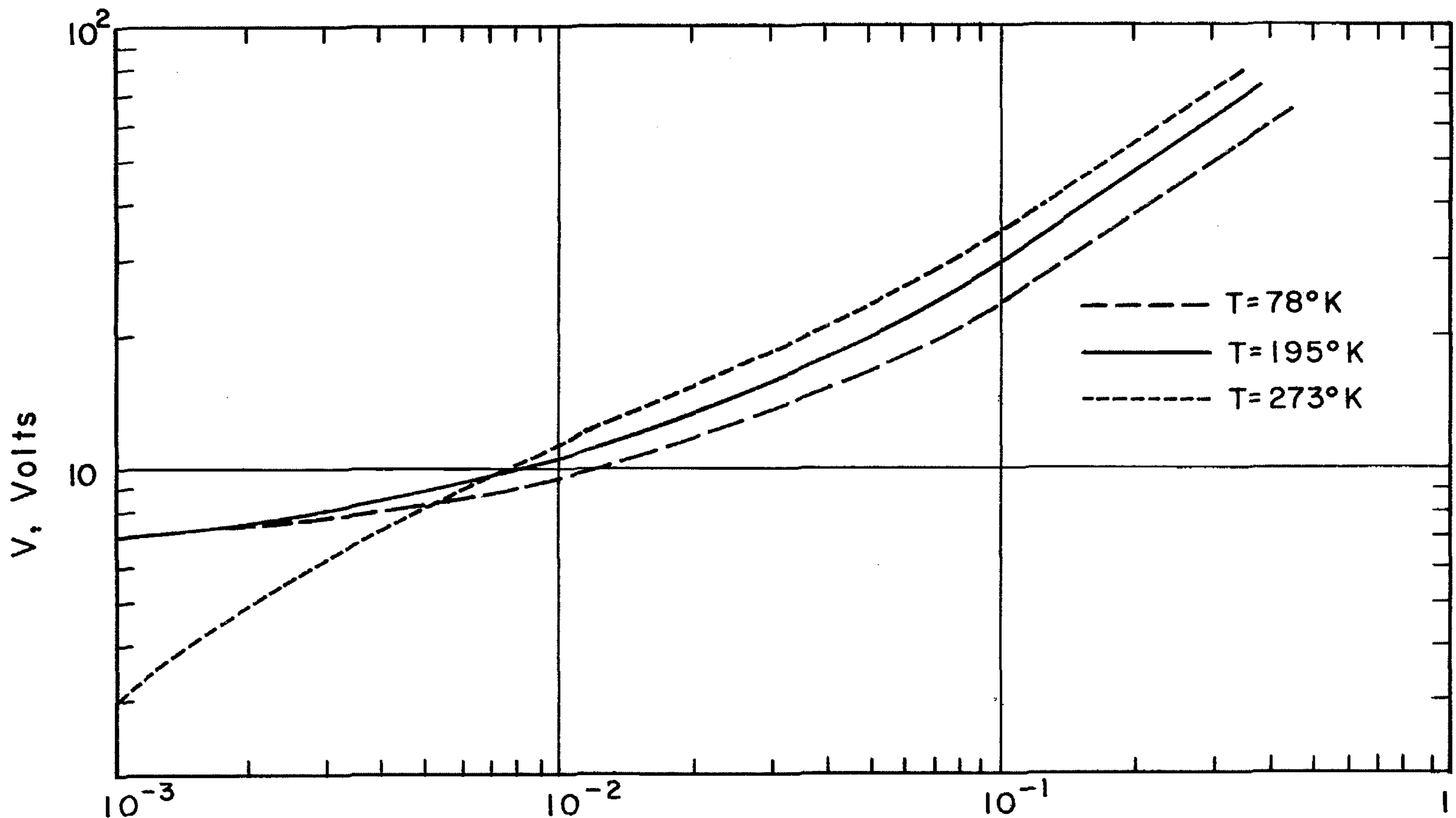


Figure 1.12. V-I characteristics of a p-n-p germanium structure ($W = 34.7\ \mu$) at different ambient temperatures.

tendency expected as expressed in section 3.3 of this chapter. The two ranges of operation described in section 3.2 of this chapter are observed for the three different ambient temperatures (273° K, 195° K and 78° K) considered. This is evident from the fact that the curve for 195° K is a translation of the curve for 78° K along the current axis. Except for very low currents, this also holds for the 273° K curve. The deviation observed is in the direction expected for large saturation currents. This is very probable since this deviation occurs at higher temperatures where larger saturation currents are present. No quantitative analysis of this deviation is given.

If we consider the solid-state diode in the high current range of operation in which the applied voltage is kept constant while the ambient temperature is varied, then a quantitative relationship between the current and the ambient temperature can be obtained. Furthermore, if we normalize the measured current to unity at one particular ambient temperature, it is then possible to represent the current-ambient temperature relationship for different samples on one graph. The results so obtained are shown in figure 1.13 where the temperature of normalization is 195° K.

A theoretical curve is also shown in this figure. Its slope of -0.85 is a modified value of -0.75 given in equation 1.28. This modification has been introduced to

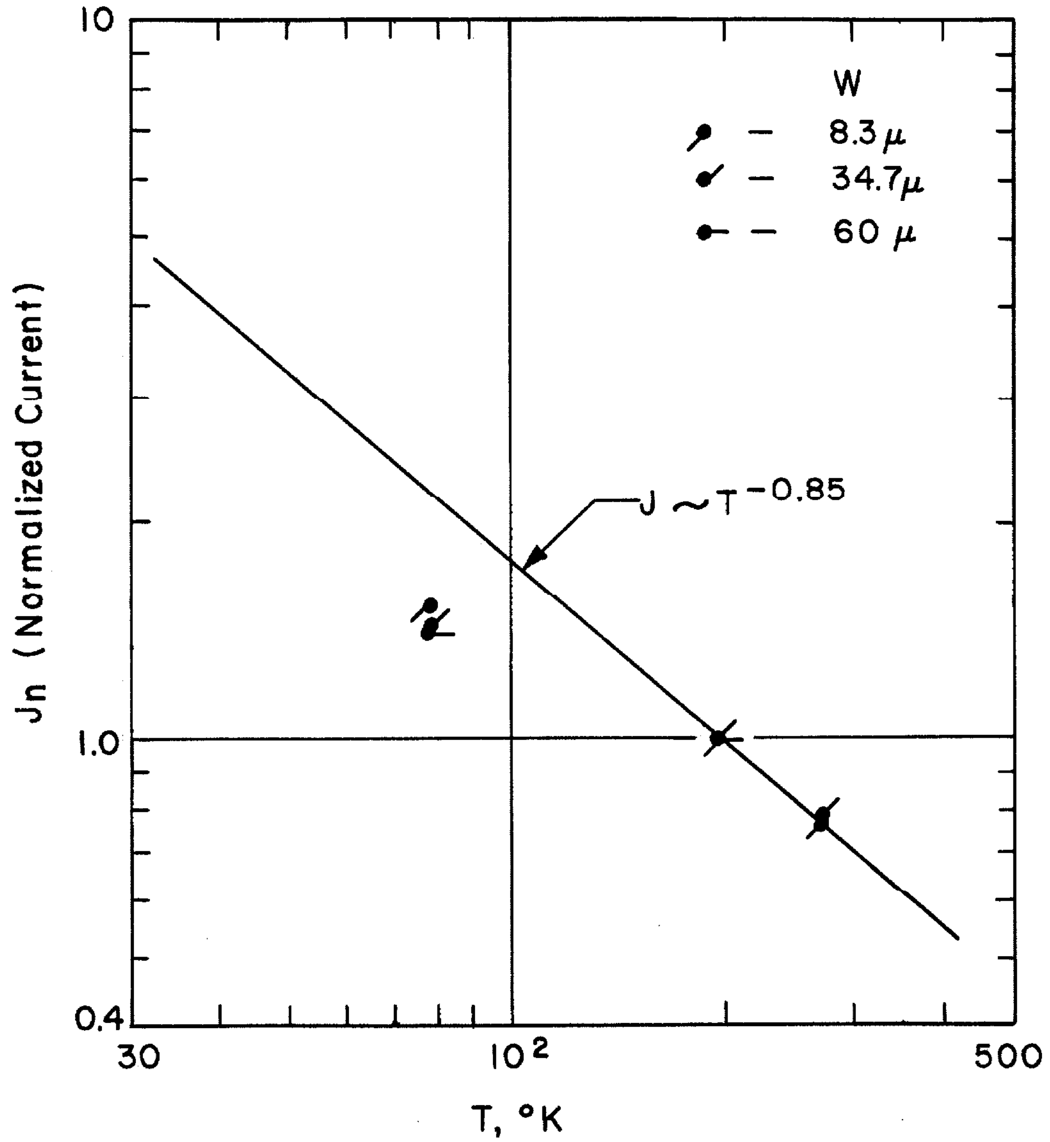


Figure 1.13. A comparison between theory and experiment for scl current as a function of the ambient temperature.

account for the temperature dependence of the low field mobility as measured (see chapter II, section 1.1), which is A $T^{-1.7}$ instead of A $T^{-1.5}$ as assumed in the theory.

In figure 1.13 a good agreement between theory and experiment exists for the high temperature range, but for 78° K there is a deviation of about 50 percent. However, the small number of measurements do not justify a quantitative comparison with theory. Furthermore, it is evident in section 3.3 of this chapter that the theory is itself semi-quantitative in that two different energy distributions are considered for the hot holes. Also, in section 4.4, the experimental results for the critical electric field tend to indicate a transition of the energy distribution of the hot holes from the Boltzmann distribution towards the discrete distribution as the temperature is lowered. If this were indeed the case, then from table 1.3 a deviation of about 50 percent would be expected in figure 1.13 at 78° K, as observed.

In summary, the agreement between theory and experiment is sufficient to indicate that a current-temperature dependence exists and that this dependence is of the magnitude expected.

CONCLUSIONS

The theory of scl current in a germanium p-n-p solid state diode predicts three regions of operation: the punching-through region, the low current range in which the effect of the donor ions is significant, and the high current range in which the effect of the donor ions is negligible. The presence of the low and the high current range is experimentally confirmed.

At punch-through the relationship between punch-through voltage and base width W has been experimentally determined. These observations agree with the theory and show a W^2 dependence as expected.

In the high current range the current is directly proportional to $V^{3/2}$. This is the dependence expected for pure scl current for the field dependent mobility. The relationship between voltage V and base width has also been determined in this range. The results verify the theory which predicts a dependence of $W^{5/3}$. A quantitative analysis of this relation leads to a value of 21 V/cm for the critical electric field E_c at 78° K. At 195° K E_c is $\simeq$ 220V/cm and at 273° K it is $\simeq$ 330V/cm. These values fall within the range indicated by Shockley's theory. It is the best correspondence between this theory and experiments obtained to date. This makes it possible to relate these results to the energy distribution of the hot holes.

There is an indication that at lower ambient temperatures the distribution tends to become discrete.

These results are the first detailed verification of the validity of the theory of scl current in solids.

The velocity of the hot holes is known to saturate at fields of approximately 10^4 V/cm. When this value was reached in one sample (8.3 μ sample), the V-I characteristic deviated from the three-halves power relationship as expected. The measured peak current density of 180a/cm^2 exceeds values reported so far on scl current in solids by one order of magnitude.

The theory of the impedance of a solid-state diode has been extended to include the case of a field dependent mobility. A verification of this theory is yet to be presented.

CHAPTER II

FABRICATION, EVALUATION AND MEASUREMENT

Introduction

A practical device, which can be represented adequately by the theoretical model for one-dimensional scl current flow in n-type germanium, must be a p-n-p structure with flat, parallel, and abrupt p-n junctions. Furthermore, the ratio of the lateral dimensions to the base width of the structure should be large to minimize edge effects. Finally, the n-type germanium must have a low uniform donor doping concentration and must be of high crystalline quality.

A commercially obtained single crystal of high quality near intrinsic n-type germanium is used for the fabrication of p-n-p structures. Pertinent physical parameters of the single crystal are measured as described in section 1 of this chapter. Since alloyed junctions offer the best approximation to the requirement of abruptness, the experimental devices to be described in this chapter are therefore alloyed p-n-p structures. The condition of flatness is most readily satisfied for junction orientations perpendicular to the [111] axis of the germanium crystal (15). Prior to the cutting and dicing operation, the single crystal must therefore be

crystallographically oriented. The procedure followed is described in section 2. In section 3 the details of the alloying process are presented. The structures obtained are characterized in section 4.

1. Measurement of Material Properties

A germanium ingot was obtained from Hughes Semiconductors with the specification that it was n-type and near intrinsic and that it was grown in the $[11\bar{1}]$ direction. The density of donors and the charge carrier mobility in the bulk material were not specified. These electrical properties had to be determined from the bulk resistivity and Hall measurements.

1.1 Resistivity Measurements. A rectangular filament of cross-sectional area $A = 6.6 \cdot 10^{-2}$ cm^2 and length $L = 1.87$ cm. is cut from the near intrinsic n-type germanium ingot with a diamond saw. Electrical contacts (see chapter II, section 4.3) are made to the end faces. It is then mounted on an electrically insulated copper block and immersed in a temperature bath. A direct current $I = 1$ ma is passed through it. Two tungsten probes positioned by micromanipulators are used to measure the potential drop along the filament. The voltage across the probes is measured with a galvanometer. The advantage of this probing method is that any variations in the bulk resistivity along the filament can be detected and that non-linearities in the end contacts do not affect the result. No variation in the bulk resistivity has been observed. It was also noticed that the electrical contacts were

blocking at temperatures below -100° C. In making resistivity measurements at different temperatures, three different temperature baths are used: liquid xylene for 25° C to 105° C, liquid pentane cooled with liquid nitrogen for 25° C to -125° C, and finally liquid nitrogen for -195° C.

The bulk resistivity ρ for a rectangular filament at a temperature T is

$$\rho = \frac{A}{L} \left| \frac{V_{p1} - V_{p2}}{I} \right| \tag{2.1}$$

where $V_{p1} - V_{p2}$ is the potential difference between the two probes. These results are shown graphically in figure 2.1a. The temperature dependence of the bulk resistivity is divided in two regions: for high temperatures the bulk material is intrinsic, and for low temperatures it is extrinsic. For the latter the temperature dependence is

$$\rho(T) = \frac{1}{q\, \mu_n(T) N_D} \tag{2.2}$$

where $\mu_n(T)$ is the electron mobility and N_D the donor density (full ionization assumed). The electron mobility as a function of temperature T is expressed as

$$\mu_n(T) = \mu_n(300^\circ\ K) \left(\frac{T^\circ K}{300^\circ K} \right)^m \tag{2.3}$$

where m is equal to -1.5 for lattice scattering (16). The experimental value of m is -1.7 as obtained from figure 2.1a. This is in good agreement with the value of

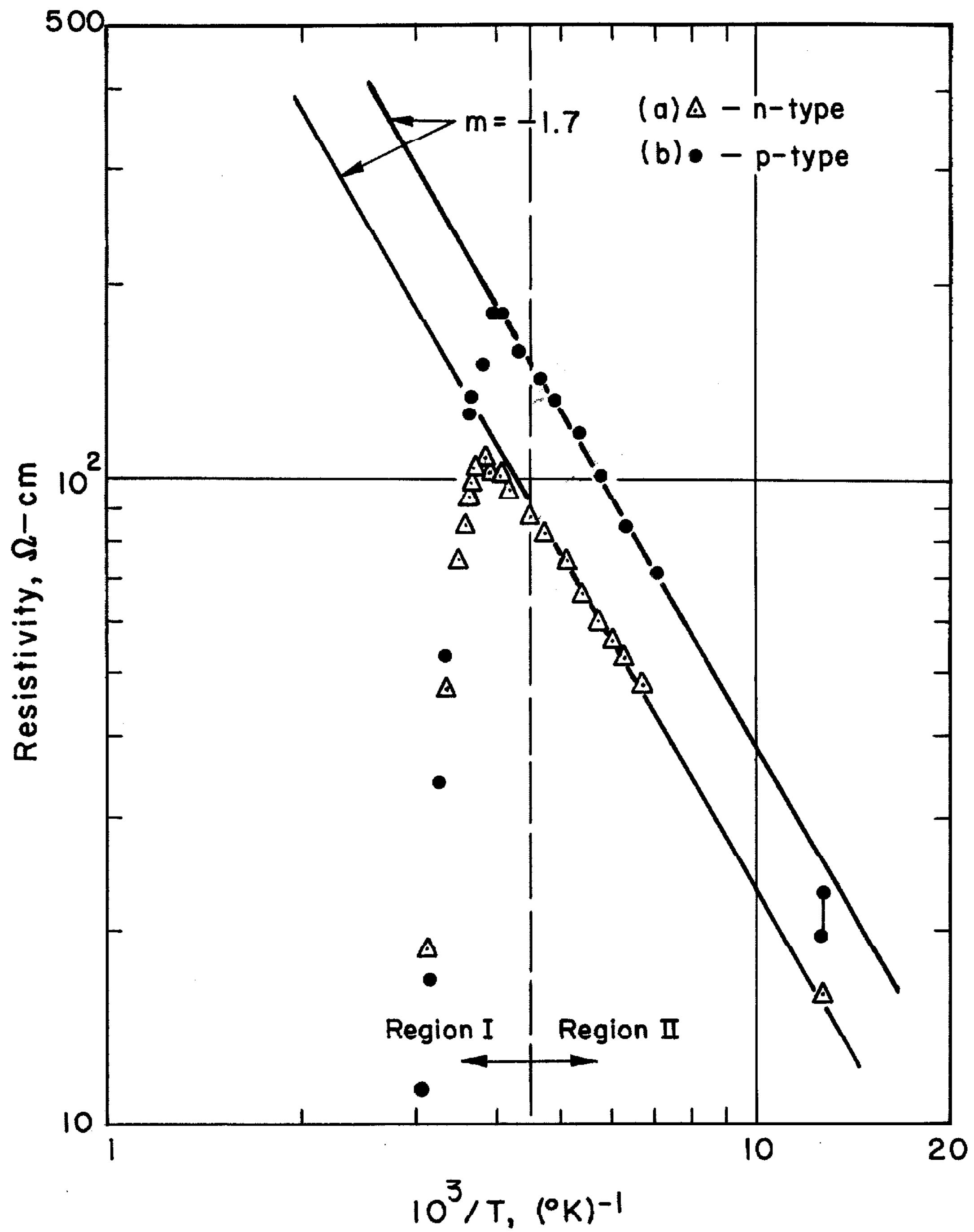


Figure 2.1. Resistivity measurements: (a) Hughes Semiconductors germanium crystal; (b) Semimetals' germanium crystal.

-1.64 of Debye and Conwell (17). Similarly the results for a near intrinsic Semimetals' germanium ingot are given in figure 2.1b. This specimen, as determined from Hall measurements, is p-type and not n-type, as specified by the manufacturer. For this case, the majority carrier (hole) mobility $\mu_p(T)$ as a function of temperature T is

$$\mu_p(T) = \mu_p(300^\circ\ K)\left(\frac{T^\circ\ K}{300^\circ K}\right)^{-1.7} \qquad (2.4)$$

Morin and Maita (18) observe a $T^{-2.33}$ dependence for the hole mobility in near intrinsic p-type material.

For electron and hole mobility values in germanium of 3900 cm^2/Vs and 1900 cm^2/Vs respectively at 300° K (19), a doping density of (1.0 ± 0.1) 10^{13} donors/cm^3 and (1.1 ± 0.1) 10^{13} acceptors/cm^3 in the near intrinsic n-type and p-type germanium respectively is determined. Furthermore the electron and hole mobility as a function of temperature is $3900(T/300)^{-1.7}$ and $1900(T/300)^{-1.7}$ cm^2/Vs respectively. These are the low field mobility values (see chapter I section 2.3).

An important parameter in the theory of scl current in germanium p-n-p solid-state diode is the minority mobile carrier (hole) mobility. This mobility should have about the same temperature dependence as that of the holes in the near intrinsic p-type germanium.

<u>1.2 Hall Effect Measurements</u>. The near intrinsic n-type germanium crystal has been analyzed quantitatively by Hall effect measurements. The procedure followed is that of Debye and Conwell (17). The results are:

1. The value of the resistivity as well as its temperature dependence agree completely with the 2 point probe measurements.

2. The donor impurity concentration N_D is (1.1 ± 0.1) 10^{13} cm^{-3} if corrections for scattering mechanisms are ignored. This compares well with the value of (1.0 ± 0.1) 10^{13} cm^{-3} deduced in the previous section. According to theory, N_D should be corrected by a factor of 1.18 in the case of pure lattice scattering. However, theory also predicts a temperature independent value of N_D. But measurements show a variation of about 10% between 78° K and 243° K, so that corrections of this order of magnitude are uncertain and have been omitted.*

3. The above results confirm that the temperature dependence of the mobility assumed in the previous section is valid.

4. Measurements made on the first and the last wafer cut from the crystal differ by less than 10%. The manufacturer considers this an unusually good result, since

---

*N_D can also be determined independently from junction depletion capacitance measurements, but not to the same degree of accuracy.

crystals of such low doping concentration often show much greater inhomogeneity.

1.3 Lifetime Measurements. The lifetime of minority charge carriers, which is an important parameter in evaluating the saturation current of a p-n junction, has been determined by the recovery time method (20). The result is 11 μs. This value is approximate since the analysis is based on a low injection model. A much longer lifetime is anticipated for materials of the purity of this near intrinsic n-type germanium single crystal. However, it has been suggested that a large concentration density of dislocations (of the order of 10^3 cm^{-2}) might be present which could account for this discrepancy.

2. Crystal Alignment

There are two principal methods to determine the orientation of a single crystal of germanium. They are the X-ray diffraction and the etch pit methods (21). The etch pit technique is chosen here for two reasons: first, the measuring apparatus can be constructed rather easily, and second, the necessary cutting, lapping and etching operations are similar to those needed also in fabricating p-n junctions.

2.1 Optical Apparatus for Crystal Alignment. The optical system consists of a collimated beam of light generated in an arc lamp. This beam is directed at a right angle to the etched germanium surface from which it is reflected onto a graduated image plane (figure 2.2). The distance of separation between the reflecting surface and the image plane is determined by the focal length of the lens and its distance from the surface. The focused image of the light source appears on the image plane.

An etched reflecting surface can be represented by a set of non-parallel reflecting planes. There will be an image for each one of these reflecting planes. The etched surface of a germanium crystal whose orientation is approximately perpendicular to the [111] axis can be represented by five non-parallel planes. Four of them correspond to

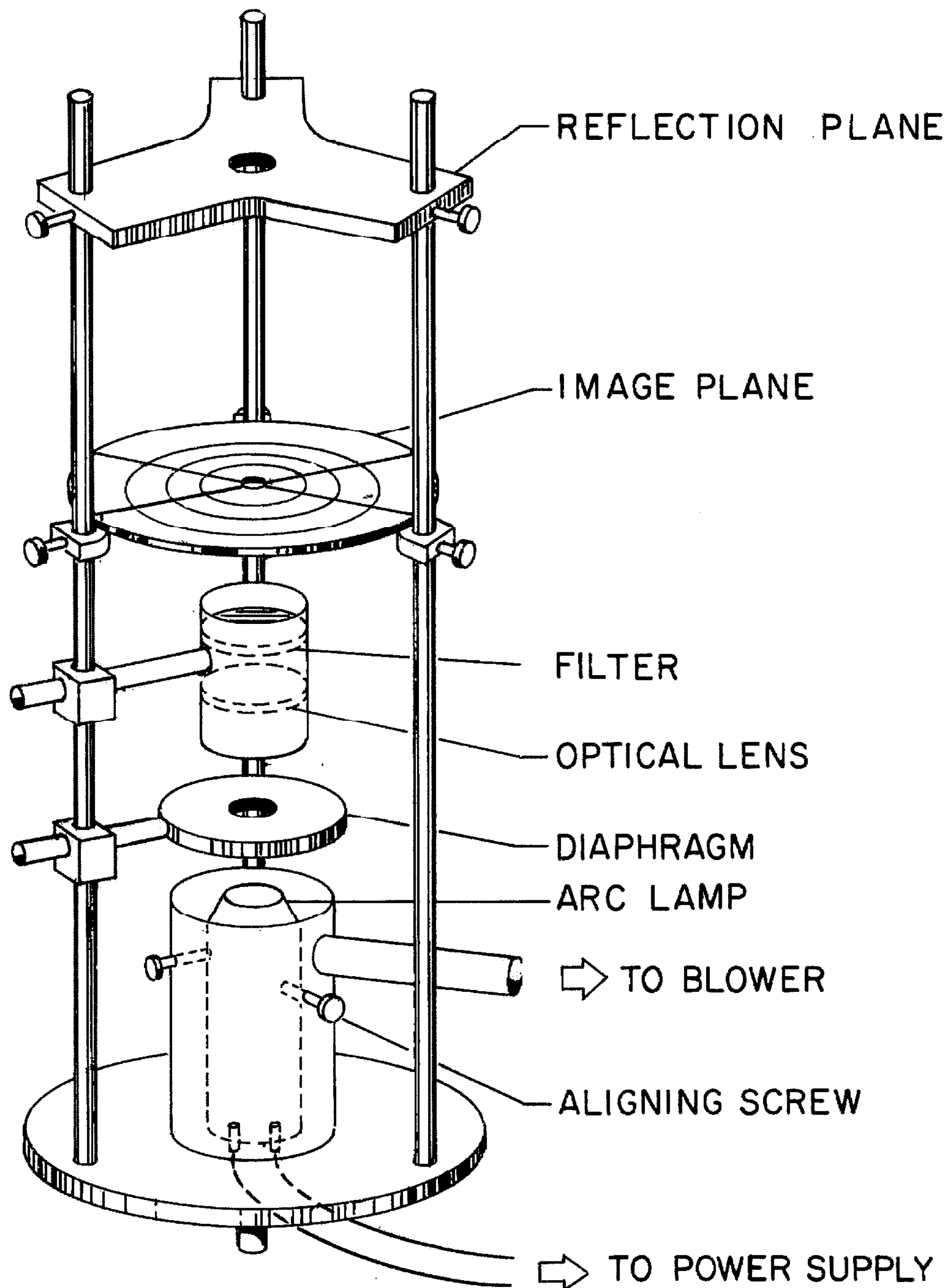


Figure 2.2. Optical apparatus for crystal alignment. Drawn approximately to 1/4 of actual size.

the facets of the etch pits which have the form of truncated triangular pyramids. The germanium surface itself corresponds to the fifth plane. There will be five images corresponding to these five planes. The position of these images on the focal plane reveals the relative angular orientation of these planes.

If the germanium surface is perpendicular to the [111] direction, then the reflecting plane corresponding to the truncated bottom of the etch pit pyramids is parallel to the crystal surface. Also, the three planes corresponding to the three sides of the etch pits will form the sides of a regular triangular pyramid. This will be indicated by a three-fold symmetry of the image pattern. The image pattern of an aligned crystal is shown in figure 2.3. The images do not have well defined but rather diffuse boundaries caused by small inequalities among the facets of different etch pits. The accuracy with which crystal alignment can be determined is limited to the accuracy with which the center of each image can be located.

If the germanium surface is not perpendicular to the [111] direction, then there will be five distinct images. Due to the preferential action of the etch, the bottom of the etch pits remains closely aligned with the (111) plane so that the corresponding image can be used as a reference for the alignment of the crystal.

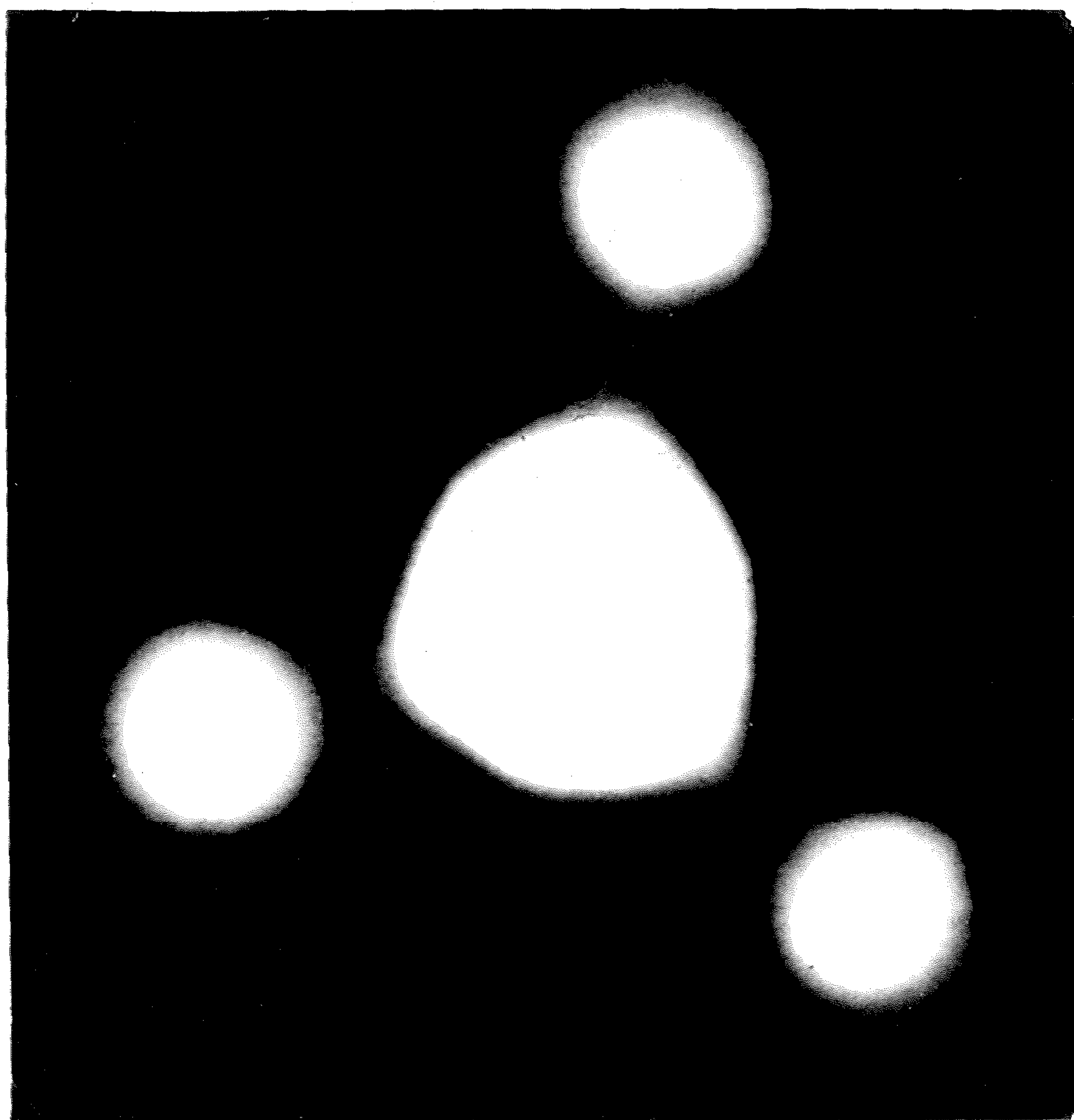


Figure 2.3 Image pattern of an etched (III) germanium crystal plane.

<u>2.2 Crystal Preparation for Alignment.</u> The face of the germanium ingot to be aligned crystallographically is etched with a superoxol etchant (22) to obtain a first approximate location of the (111) crystal planes. The ingot is then cemented with wax (Apiezon W) on a jig that is rigidly fastened to the horizontal cutting table of the diamond saw. Two horizontal lines are then scribed on the face of the ingot. A slice of approximately 1.5 mm thickness is cut from the ingot. This cut is oriented as closely as possible into the direction of the (111) plane as previously determined by rotating the table of the saw.

The pre-oriented side of the slice is lapped by hand on a 600A silicon carbide paper to remove the coarse mechanical damage, and then lapped to a fine uniform texture on 3200 mesh grinding compound on a glass plate. The slice is then cut along the scribed lines and the two ends of the remaining wafer are truncated also so that the wafer fits into a wafer holder. These last two cuts are not made parallel to each other to assure that the position of the wafer with respect to the ingot is not lost. The wafer is removed from its cutting jig with trichlorethylene which dissolves the wax, is washed in acetone to remove the trichlorethylene, rinsed in distilled water and dried by absorbing the water with Kimwipe tissue. The wafer is now cemented with its unlapped side on the wafer holder of the

orienting jig. This jig allows one to vary and set the angle of the lapping operations to follow.

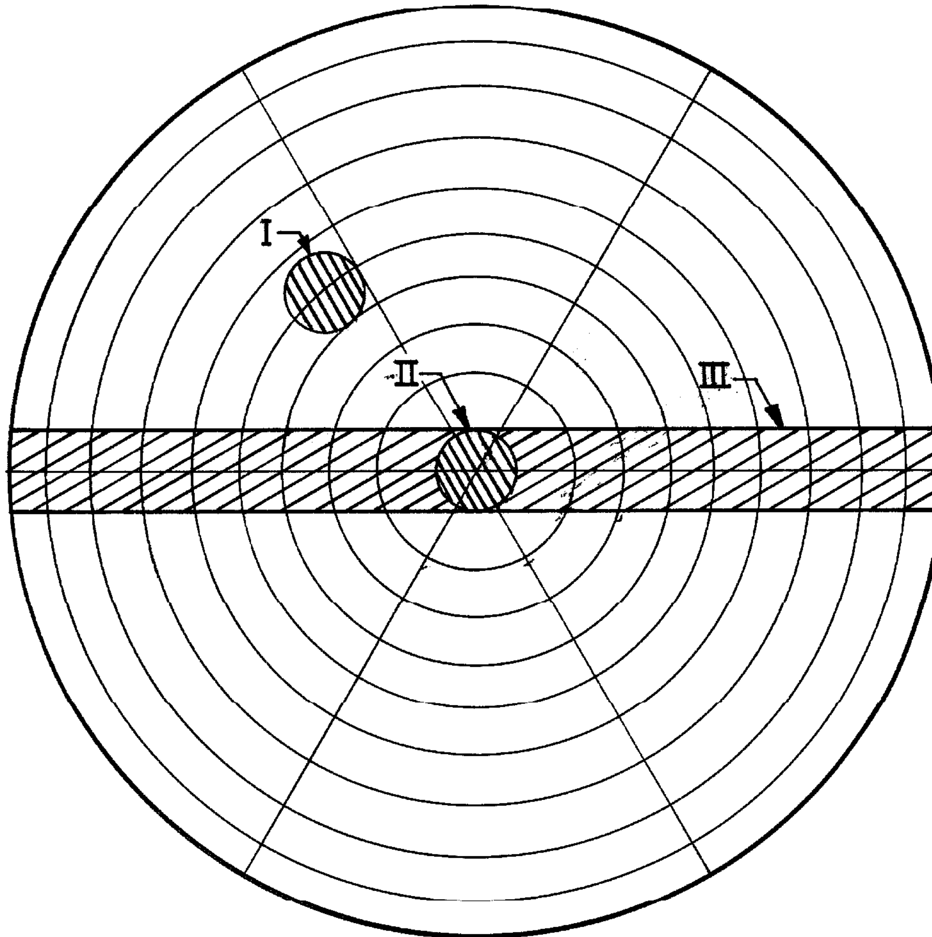
The wafer surface is de-oxidized with a concentrated solution of HF for two minutes, rinsed thoroughly with distilled water, immersed in a concentrated solution of H_2O_2 for ten minutes, and finally rinsed thoroughly with distilled water. The surface is then etched for about five minutes at room temperature with an etchant of 3 ppv concentrated H_2O_2 and 1 ppv concentrated HF, then thoroughly rinsed in distilled water and dried with Kimwipe tissue. If the reflection pattern of the surface is not well defined, the etching procedure is continued in one minute steps until a maximum of definition and intensity is obtained in the pattern. This etchant produces a relatively small density of large and well defined etch pits on the germanium surface, which gives a clear reflection pattern with little scatter.

2.3 Crystal Alignment. If the etched surface of the wafer is not well aligned with the (111) plane of the crystal, then there will appear five distinct images on the focal plane of the alignment apparatus. The wafer is then adjusted in the lapping jig until the image corresponding to the bottom plane of the etch pits coincides with the center of the focal plane. The wafer is re-lapped, re-etched,

and readjusted and these operations are repeated until the final adjustment compensates for the last differences in the relative intensities and for the deviations from the three-fold symmetry in the reflection pattern. An image of the pattern for an aligned crystal is shown in figure 2.3.

Once the wafer is aligned, its orientation relative to the original cut has to be measured. For this purpose, a section of the wafer surface had been covered by wax prior to the initial etch. Care was taken to protect this section from further lapping or etching during alignment. In a final operation, the aligned surface is re-lapped, the wax protecting the section of non-aligned surface is removed, and the whole surface is etched in a diluted superoxol etchant long enough to produce a polished texture. The surface of the wafer now forms two reflecting planes corresponding to the aligned and the original non-aligned surface. Lines parallel to the parallel sides of the wafer are scribed on the non-aligned section of the surface. The reflection pattern now consists of two images, corresponding to the two planes, and a narrow ribbon of light which is reflected from the scribed lines and is in a direction perpendicular to that of the lines. Such a pattern is shown in figure 2.4. The position of the images relative to the ribbon of light permits one to determine the angular displacements of the (111) crystal plane with respect to the

GRADUATED IMAGE PLANE



I — Image corresponding to the oriented surface
II — Image corresponding to the non-oriented surface
III — Image corresponding to the scribed lines

Figure 2.4. Image of the reflection pattern for crystal alignment.

horizontal and vertical axis on the pre-aligned surface of the ingot.

The geometrical representation used for the calculation of the displacements is shown in figure 2.5. For a typical case, CB = 1.7", AB = 6.95" and ∠CBD = 33.2°. The symbols are those given in figure 2.5. Angle CAB is twice the angular displacement between the aligned and non-aligned surfaces.

$$\angle CAB = \arctan (CB/AB)$$
$$= 10^{\circ}\ 44'$$

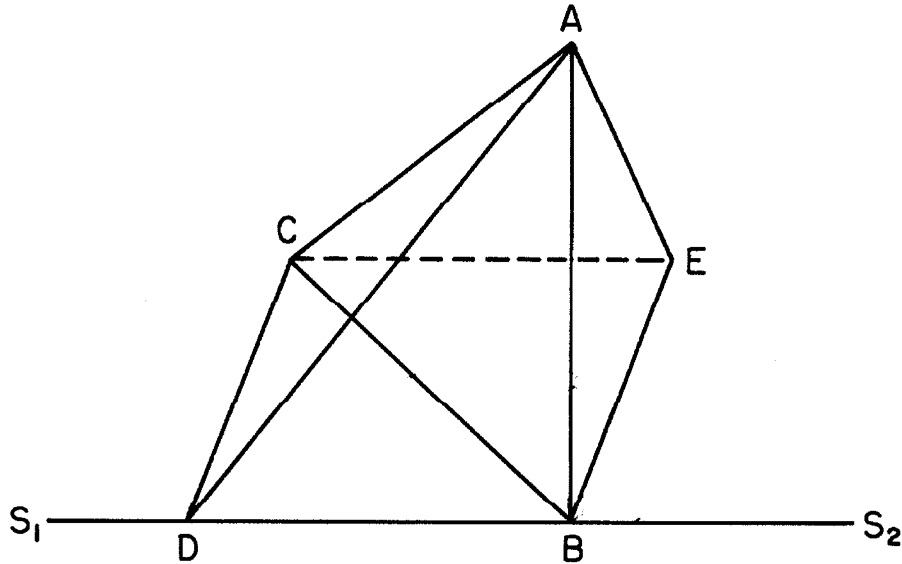
Angle DAB is twice the angular displacement between the aligned and the non-aligned surfaces in the plane perpendicular to the vertical axis on the cut surface of the ingot.

$$\angle DAB = \arctan (DB/AB)$$
$$= 11^{\circ}\ 33'$$

Angle BAE is twice the angular displacement between the aligned and the non-aligned surfaces in the plane perpendicular to the horizontal axis on the cut surface of the ingot.

$$\angle BAE = \arctan (BE/AB)$$
$$= 5^{\circ}\ 17'$$

To align the ingot, one end of the jig on which the ingot is mounted is raised so that the vertical angular



$AB \perp S_1S_2$, $CD \perp S_1S_2$, $EB \perp S_1S_2$, $EB \perp AB$, and $CD = EB$

Figure 2.5. A geometric representation used for calculating the angular displacements between the oriented and the non-oriented surface where B is the center of the image corresponding to the non-oriented surface, C the center of the image corresponding to the oriented surface, line S_1S_2 the center of the image corresponding to the scribed lines and A the center of the reflection plane.

displacement is 2° 38.5' and the horizontal cutting table is rotated by 5° 46.5' in the required direction. As a check of the accuracy of this method, the crystal orientation of the germanium wafer was determined by the X-ray diffraction method and then checked by the optical method. It was found that the accuracy of the alignment by the optical method is within 30 minutes of arc.

3. Fabrication of P-N Junctions and P-N-P Structures.

3.1 Preparation of Wafers for Alloying. The crystallographically oriented germanium ingot is cut into parallel slices of thicknesses ranging from 500 to 300 microns. These slices are cleaned in trichlorethylene to remove wax and grease. Each slice is lapped on 400 A and 500 A silicon carbide wet-dry paper to reduce its thickness, if necessary, and is then lapped on 600 A silicon carbide wet-dry paper to remove the coarse mechanical damage. Finally, the slice is lapped with 800 mesh grinding compound to a uniform texture. The lapping operation is carried out on both sides of the slice. The resulting surface could be made less coarse by lapping the slice with 3200 mesh grinding compound on micro-cloth; however, no marked advantage of such an operation was observed.

The lapped slice is cemented with wax to the diamond saw jig and is then diced into wafers 2.5 mm. square. These wafers, removed from the jig with trichlorethylene, are cleaned ultrasonically in trichlorethylene to remove grease, cutting residue and wax. They are then washed in acetone, rinsed in distilled water, and finally dried by absorbing the water with a Kimwipe tissue.

3.2 Masking. Alloyed p-n junctions of controlled area can be formed by restricting the alloying process on

the wafer to a fixed area. This is achieved by using a standard graphite jig technique. The graphite jig is carefully machined to hold a wafer of specified geometry on which a junction having a simple configuration such as a circle or a rectangle is alloyed. Different graphite jigs have to be designed for different wafer geometries and for different alloying areas. This method is not easily adaptable for fabricating p-n junctions with different junction areas on wafers of different sizes on a laboratory scale.

Another procedure which would overcome the restrictions of the graphite jig technique is one in which the alloying area is controlled not by mechanical means but by making the wafer surface inactive to the alloying process outside the desired alloying region. One way to accomplish this is to mask the wafer surface by depositing on the wafer a layer of material which is inactive to the alloying process. The advantages of this approach are that different alloying areas can readily be produced and that there are no limitations placed on the physical geometry of the wafer.

A material that completely satisfies this requirement is silicon monoxide. SiO, which can be deposited in a thin homogeneous layer on the wafer surface by vacuum deposition, is not wetted by the alloying material (indium in this case) at junction alloying temperatures. It strongly adheres to the wafer surface but can be easily removed by putting the

wafer into a solution of HF.

3.3 Masking Procedure. Before p-n junctions are alloyed on the germanium wafers, the wafer surfaces have to be free of mechanical damage to insure planar junctions. This damage can be best removed by chemical etching which not only removes the damaged material, but also gives the surface a highly polished texture. This can be achieved by etching the wafer with an etchant of 3 ppv of concentrated HNO_3 and 1 ppv of concentrated HF for about two or three minutes at room temperature. Since the etchant contains HF which reacts with the masking material, it is necessary that this etching operation take place before a mask is applied to the wafer.

The wafers must first be cleaned ultrasonically in alcohol, rinsed in distilled water, deoxidized in a diluted HF solution, and then rinsed in distilled water before being etched in the manner outlined above. After being etched, the wafers are washed in distilled water and dried by absorbing the water with Kimwipe tissues. They are now ready for masking.

Temporary masks are used to prevent the alloying regions on the wafer from being covered during vacuum deposition. These masks are thin flat platelets of tantalum of the geometry desired for the p-n junctions. They are,

with the aid of a microscope, carefully positioned on the regions to be alloyed. The wafers are kept on a glass slide.

The vacuum chamber consists of a bell jar placed on a machined aluminum cylinder in which insulated electrodes are placed to supply electric power to a heating filament and to a heating strip inside the vacuum chamber. Amorphous silicon monoxide is placed inside a 20 mil tungsten filament previously heat cleaned under vacuum. The glass slide with the wafers is then placed on the support table under the filament inside the vacuum chamber. After the chamber is pumped down to a vacuum of about 2×10^{-6} Torr, the filament is rapidly heated by passing a current of roughly 20 amperes for about 15 seconds every 2 minutes until the silicon monoxide deposited on the wafer is brown in color. The intermittent heating cycle prevents the wafers from getting hot. The color of the wafer is taken as an indication of the thickness of the SiO layer. If p-n junctions are to be made on both sides of the wafer then the outlined masking procedures are repeated on the opposite side of the wafer.

<u>3.4 Surface Treatment before Alloying</u>. It is very important to keep the alloying substrate (wafer surface) and the alloying material (indium) very clean if the alloying material is to wet the substrate uniformly. Contaminants such as oxide layers, dust and lint inhibit the

alloying process.

Chemical cleaning, the most common method, is not possible since HF removes the mask. Gas cleaning by chemical reduction of the oxide layer is another possibility. However, this procedure did not lead to fruitful results owing to the presence of contaminants in the gas system used. The method found most convenient is vacuum cleaning.

The procedure is as follows: immediately after the masking operation, the vacuum chamber is modified by replacing the filament containing silicon monoxide with a filament containing indium (99.999% pure), and by putting a 5 mil tantalum heating strip about 4.5 cm. below the filament. The heating strip is heat cleaned to remove surface contaminants and the indium is heat cleaned to remove the surface oxide layer. This cleaning is done in the vacuum chamber. The wafers are placed on the cleaned heating strip and heated to 750° C for 15 minutes in a vacuum of about 2×10^{-6} Torr. After the wafers have cooled down to room temperature, a layer of a few microns of indium is deposited on the substrates. Indium is evaporated by passing a 15 ampere current through the filament for 10 seconds every 2 minutes. When the alloying substrates are on opposite sides of the wafers, indium is deposited on both sides of the wafers. For this operation the wafers are removed from the vacuum chamber to be turned over. This is quickly carried out so as to minimize the oxidation of the exposed alloying substrate.

The advantages of such a procedure are that not only does a clean layer of alloying material come in contact with the clean alloying substrate, but also this clean layer prevents the substrate from being contaminated in any way before the actual alloying process takes place.

3.5 Alloying P-N Junctions. P-n junctions are alloyed in a horizontal strip heating furnace. The furnace consists of a 5 mil tantalum heating strip inside a cylindrical vacuum tight chamber. The heating strip is constructed to hold a small graphite cup in which p-n junctions are alloyed. Heating strip temperature is measured with an iron-constantan thermocouple. There is a gas inlet and outlet to the furnace.

The gas system is composed of a catalytic hydrogen purifier to de-oxidize the gas, two molecular sieve drying towers to remove the water from the gas and a flow meter to monitor the gas flow. The gas used is 80% nitrogen and 20% hydrogen forming gas. This gas, which flows through the furnace, is used both as a reducing agent and as a heat transfer medium.

Only one wafer can be placed inside the graphite cup which is designed to maintain the wafer in thermal equilibrium during alloying. Before the wafer is placed inside the graphite cup the layer of deposited indium is carefully scraped off with a very clean razor blade

everywhere except in the region to be alloyed. For p-n junctions to penetrate 10 to 40 microns below the wafer surface, more indium has to be added. This is simply accomplished by taking very clean strips of required additional indium of approximately the same area as the alloying areas and by pressing these strips onto the alloying areas with a very clean teflon plate. The wafer is then placed inside the graphite cup which had previously been heat cleaned inside the furnace. The chamber is evacuated and flushed with forming gas several times before the flow of forming gas is set to 1000 cu. cm. per minute.

The wafer is now ready for the heat cycle which consists of four different heating rates. First, the temperature of the wafer is continuously increased at a rate of about 30° C per minute to about 100° C above the melting point of indium to insure a uniform wetting of the added indium with the vacuum deposited indium. Then, the temperature of the wafer is continuously increased at a rate of 50° C per minute to about 450° C to insure a uniform wetting of the indium with the germanium substrate. From here on, the temperature of the wafer is increased at a very slow rate to about 540° C until the liquid indium acquires a shiny luster, balls up, and eventually covers the alloying area only. Finally, the temperature of the wafer is increased to the peak alloying temperature (550°C

in this case) and maintained at this peak temperature for about fifteen minutes so that the germanium-indium mixture is in a liquid-solid phase equilibrium. The electric power to the heating strip is controlled with a Variac.

In the cooling cycle the wafer is first cooled at a continuous rate of 21° C per minute for sixteen minutes. This first cooling rate permits a uniform rate of recrystallization of the liquid germanium-indium mixture onto the wafer substrate while at the same time the liquid-solid phase of germanium and indium is maintained in quasi-equilibrium. This recrystallized region which is p-type, makes a metallurgical contact with the substrate material, which is n-type, and a p-n junction results. The wafer is then cooled at a continuous rate of 42° C per minute until room temperature is reached. This final cooling rate allows the wafer to rapidly cool to room temperature without creating undue thermal stresses and strains in the regrowth region. The alloying process is viewed through a glass plate on top of the furnace with a x30 magnification microscope. The temperature of the wafer monitored with the thermocouple is charted on a strip chart recorder. Since it is important to control the cooling rate of the wafer to obtain good reproducible p-n junctions, the cooling cycle is carefully made to follow a prescribed cooling curve drawn on the chart.

The advantages of the mask technique are quite apparent. First, the added indium readily wets the vacuum deposited indium. Second, the clean alloying area is uniformly wetted by the clean surface of the deposited indium. Third, surface tension forces of liquid indium are sufficient to absorb the indium on the silicon monoxide surface into the alloying region. The shape of liquid indium then becomes the shape of the alloying region. It is evident from these operations that p-n junctions of different geometries can be alloyed.

3.6 Alloying P-N-P Structures. The procedure for preparing the wafer for alloying p-n-p structures is identical to that described for the p-n junctions. Both the bottom and the top junctions are alloyed at the same time. The graphite cup containing the wafer has a hollowed bottom to provide space for the indium of the lower junction. A cross-sectional view of the graphite cup and the wafer is shown in figure 2.6.

3.7 Surface Treatment after Alloying. The alloyed wafer is first placed in a diluted solution of HNO_3 for 2 minutes to remove any indium that may be present on the masked surface and to remove some indium on the periphery of the alloyed region. The wafer is then rinsed thoroughly in de-ionized distilled water and placed in a concentrated

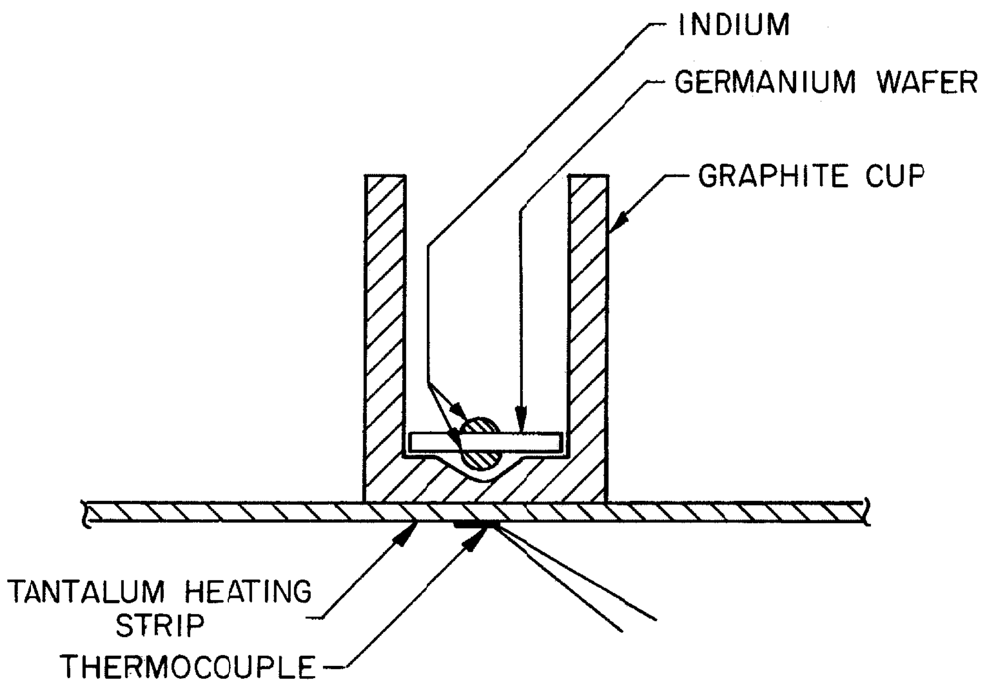


Figure 2.6. A cross-sectional view of the graphite cup and the wafer.

solution of HF for the length of time necessary for the SiO mask to be dissolved. The wafer is again rinsed in de-ionized distilled water and then placed in a concentrated solution of H_2O_2 for 10 minutes. This operation appears to oxidize uniformly the wafer surface and thus enables the final etching process to etch at a uniform rate on all parts. The wafer is lightly rinsed in de-ionized distilled water and is then etched from 5 to 10 seconds in a fresh concentrated solution of 3ppv of HNO_3 and 1 ppv of HF. This etching process removes any shorting channels on the surface between the alloyed region and the bulk material. Finally, the wafer is thoroughly rinsed in de-ionized distilled water and placed in a concentrated solution of H_2O_2 for about 10 minutes to oxidize the surface. This oxidation pacifies the surface and prevents the electrical characteristics of the junction from later deterioration. The wafer is removed from the H_2O_2 solution and dried by absorbing the H_2O_2 solution with a Kimwipe tissue.

Numerous other different surface treatments were studied on over twenty wafers. The surface treatment outlined above gave consistent results adequate for the intended application.

4. Measurement of P-N Junction and P-N-P Structure Properties

4.1 Metallurgical Analysis. The desired p-n-p structure must consist of an n-region separated by two parallel and planar alloyed p-n junctions. Two metallurgical techniques are used to determine whether or not the fabricated structures meet this requirement.

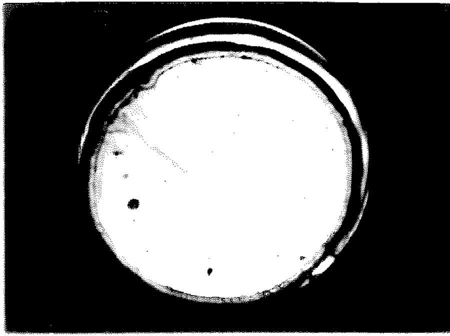
In the first method (23) the surface of the regrown germanium is displayed by removing the indium from the alloyed region by dissolving it in a concentrated solution of HNO_3. This surface is examined with a microscope. The method is used primarily to give a qualitative analysis of the wetting and dissolution of germanium by indium during alloying and of the recrystallization process after dissolution. In the second method (24) an arbitrary orthogonal cross-sectional cut of the p-n-p structure is made and the two alloyed junctions are exposed by a chemical etch. This method gives quantitative results.

The cross-sectional cut of the p-n-p structure is made in the following way: the wafer is placed vertically in a cylindrical aluminum foil cup by means of a wire frame holder to which it is pasted with a silver paste. A clear potting compound (potting compound No. 425) is poured into the cup and left to harden for 48 hours at room temperature. The aluminum foil is then removed. The base of the

clear cylindrical casement is lapped on very coarse silicon carbide paper until the bottom edge of the wafer appears. Then the operation is continued on a 500 A and 600 A silicon carbide paper until the alloyed structure appears. Finally, on 600 A silicon carbide paper lapping takes place across the width of the wafer cross-section. This eliminates any scratches that may appear lengthwise across the wafer cross-section and which may later be mistaken for the metallurgical junctions. The wafer cross-section is then polished with 800 mesh grinding compound on a micro-cloth.

Two different methods were used to chemically expose the junctions. In both cases the surface is first thoroughly rinsed in distilled water to remove the grinding compound, then deoxidized in a concentrated HF solution and finally rinsed in distilled water. In the first method a concentrated solution of H_2O_2 chemically etches in 20 to 30 minutes shallow grooves at the metallurgical junctions. In the second method deeper and more distinct grooves are obtained in about a minute if the etchant is 20 ppv of concentrated H_2O_2 and 1 ppv of concentrated HF. The etching time is determined by the amount of HF added to H_2O_2. After etching, the surface is rinsed in distilled water and dried by absorbing the water with a Kimwipe tissue.

On the more than 30 regrown surfaces examined only 5 distinctly different structures are observed (see figure 2.7). Structure (2.7a) with its flat surface and smooth

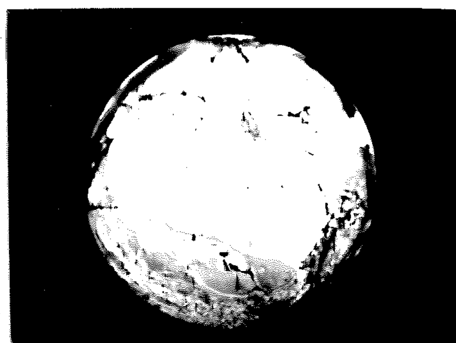


(a) FLAT STRUCTURE

(b) PLATELET STRUCTURE

(c) PITTED STRUCTURE

(d) REEF STRUCTURE



(e) GRAIN STRUCTURE

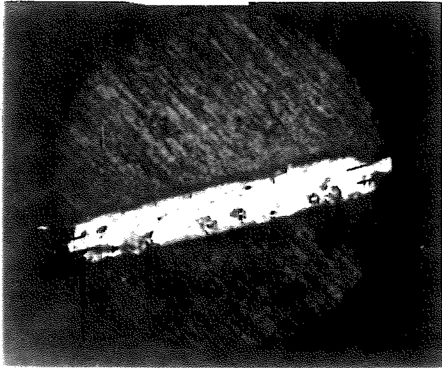
0 0.1 0.5 mm

Scale

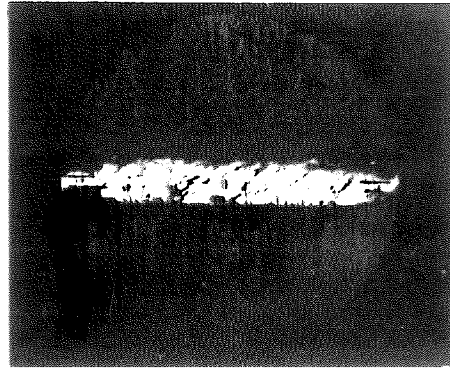
Figure 2.7 Five different structures of the regrown surface for germanium.

texture is representative of the ideal case wherein a uniform wetting and dissolution of germanium by indium is followed by a uniform recrystallization of germanium. The platelet structure in (2.7b) strongly indicates that regrowth takes place along the (111) crystal planes but not at a uniform rate. The pit structure in (2.7c) is usually obtained when the alloying takes place on the bottom side of the germanium wafer (see section 3.6). No detailed effort has been made to determine the causes of this effect. The reef structure in (2.7d) is probably due to non-uniformity in recrystallization even though wetting is uniform. In structure (2.7e) the large grain boundaries and the non-planar surface indicate a non-uniformity of wetting and dissolution. Of these five different structures, (2.7b) and (2.7c) are the most common.

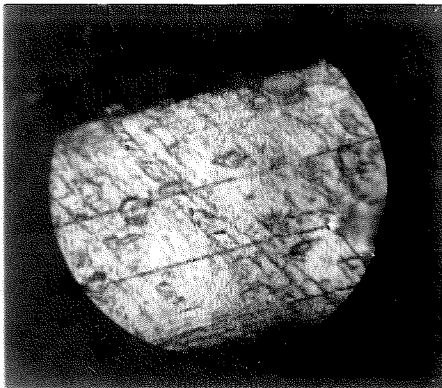
Metallurgical cuts of 10 samples show that for regrowth surfaces (2.7a, b, c, d), the junctions are flat and parallel to each other (see figure 2.8a) while for (2.7e) they are not (see figure 2.8b). Metallurgical cuts were made of all samples after the electrical measurements had been completed. Structures with non-parallel junctions were discarded in the final evaluation of the results. In no case was it found that the pits observed (see figure 2.8a) in the regrowth regions affected the electrical results. Junction separation distances are obtained from these cuts.



(a) PARALLEL JUNCTIONS



(b)NON-PARALLEL JUNCTIONS



(c) CUT (a) MORE HIGHLY MAGNIFIED

0 0.1 0.5 mm

Scale for (a) and (b)

0 10 50 100 μ

Scale for (c)

Figure 2.8 Metallurgical cuts of the alloyed pnp structures

The above analysis indicates that uniform wetting and dissolution of germanium by indium and an almost uniform regrowth of germanium after dissolution was achieved.

A photograph is taken of each metallurgically cut sample that is magnified 762.9 times with a microscope (see figure 2.8c). From these photographs the separation distance between the two metallurgical junctions can be accurately measured. The error of measurement is less than 2 percent.

4.2 Alloyed Junction Area. In the process of alloying, the molten indium not only penetrates perpendicularly but also laterally into the germanium wafer. This undercutting on the edges of the SiO mask gives rise to a junction area which is slightly larger than that defined by the mask. The actual area of the alloyed region must be measured if it is to be known to within 1 percent.

A photograph is taken of the alloyed junction that is magnified 110 times with a microscope. The area of the photographed junction is measured with a planimeter. The errors involved in the scaling factor and in the planimeter measurement are less than 1 percent.

4.3 Ohmic Contacts. Two external electrical connections have to be made to the p-n structure before the electrical behavior of the junction can be studied. The

contacts of these connections have to be ohmic. One of these connections consists of a tungsten probe or of a phosphor bronze strip in pressure contact with the indium already present on the alloyed junction. This contact is ohmic. The other connection consists of a metal in contact with a near intrinsic n-type germanium. Four different methods of making this contact ohmic were studied. One gave excellent results.

The first method was to fuse a metal with germanium in a controlled atmosphere of forming gas and in air with and without soldering fluxes. The materials used were pure tin, pure lead, and also a 50-50 lead-tin solder which contained some indium. The experimental results were irreproducible and the contacts not ohmic.

The second method was similar in many respects to the first except that the whole operation was carried out in vacuum. Here pure tin, pure lead, 50-50 lead-tin solder and gold were deposited on a hot and cold germanium substrate. The temperature of the hot germanium substrate was from 50 to 100° C above the eutectic temperature. The contacts were not ohmic.

Liquid mixtures formed from the different combinations of indium, gallium, and mercury were used in the third method. These mixtures were rubbed onto the germanium surface. Those containing mercury gave more favorable

results. The contacts in general did not exhibit a good ohmic behavior over a wide range of voltage and current and also tended to deteriorate with time.

In the fourth method a good reproducible contact was obtained which exhibited an ohmic behavior over a wide range of current and voltage at room temperature and did not tend to deteriorate appreciably with time. Here the ohmic contact is obtained by rubbing a liquid mixture of gallium and indium on the germanium surface with a piece of thallium until an intimate contact between the liquid mixture and the surface is made. The unusual wetting property of thallium was observed by V. J. King (25). To evaluate the quality of this contact, thin germanium wafers of 5 different resistivities (2 n-type and 3 p-type) were selected. Contacts were made on both sides of the sample. The results in table 2.1 show that the range of linearity between voltage and current is much larger for p-type than for n-type germanium. From the resistance measurements the bulk resistivities of the wafers can be determined. In figure 2.9 these results are compared with the corresponding resistivity values obtained with the 4 point probe. The largest deviation between these results tends to be for the n-type material; however, even this is within the experimental error of measurement which is of the order of 10%. On near intrinsic n-type germanium this

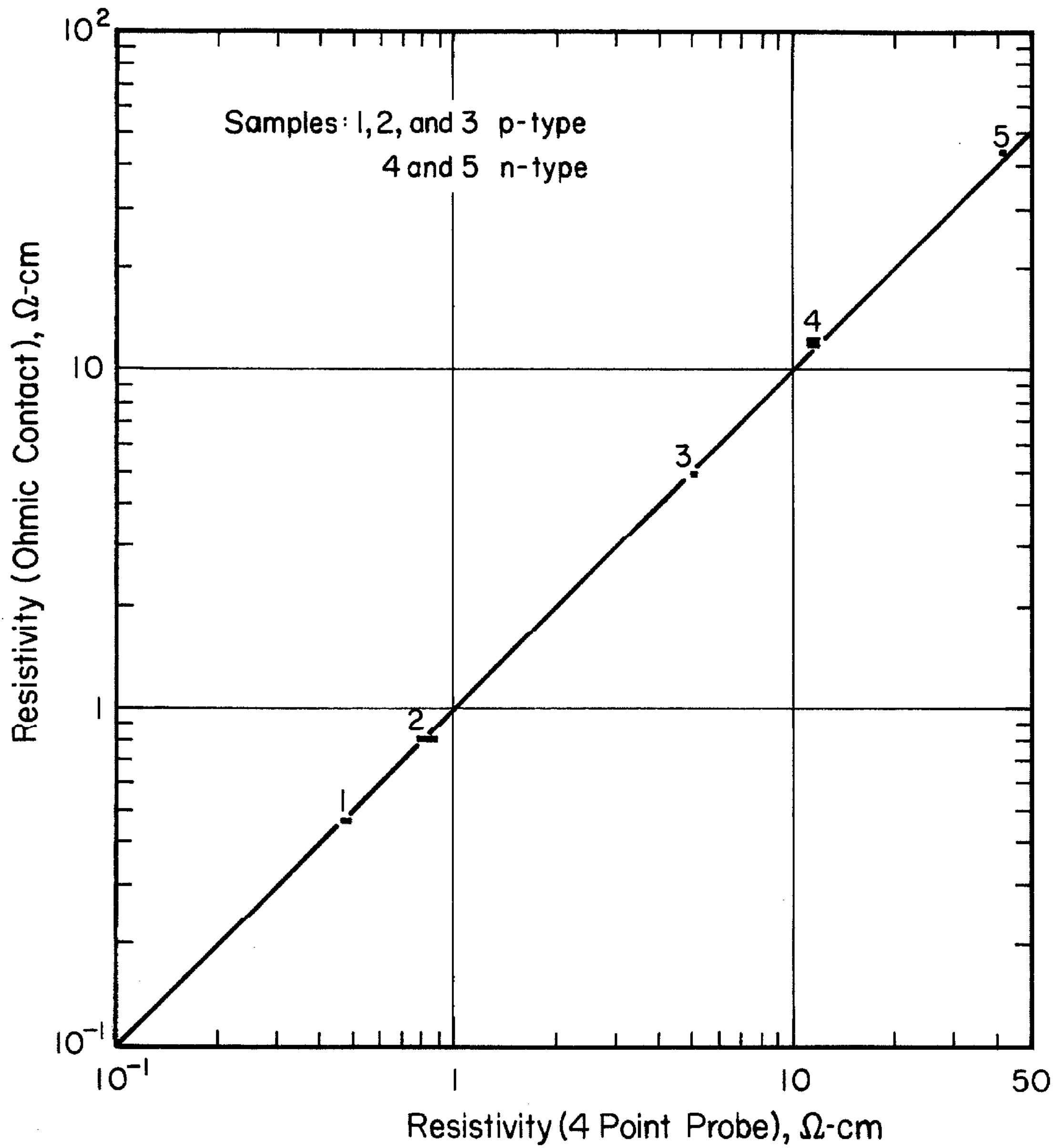


Figure 2.9. A comparison between the resistivity values measured by the 4 point probe and the ohmic contact technique.

contact is ohmic down to about -100° C but for lower temperatures begins to rectify (see chapter II, section 1.1).

Table 2.1

RANGE OF CURRENT AND VOLTAGE IN WHICH THE MAXIMUM DEVIATION FROM LINEARITY IS LESS THAN 5%

Resistivity of Sample in Ω-cm	Current Peak to Peak in Amps	Voltage Peak to Peak in Volts	Conductivity Type	Contact Area in 10^{-2} x cm^2
0.48	12	6.8	P	6.25
0.82	9.4	6.8	P	6.75
5.0	2.4	12	P	6.5
12.0	0.054	0.55	N	6.4
42.5	0.057	2.0	N	6.2

The advantage of this last method is that good reproducible ohmic contacts can be made in a matter of a few minutes. Also this contact can be removed easily in HF or HNO_3.

4.4 Depletion Capacitance. Ideally, the junctions of the p-n-p structure should be abrupt. The abruptness actually achieved is determined from a comparison of depletion capacitance measurements with the theoretical expression

for an ideally abrupt junction, for which

$$C_D = \left(\frac{\epsilon\epsilon_o q N_D}{2(V + V_j)}\right)^{1/2} \tag{2.5}$$

where C_D is the depletion capacitance per unit area, V the applied dc reverse bias, V_j the built-in junction potential, N_D the donor concentration in the n-region, and ϵ the relative dielectric constant. Providing there is no freezing-in of impurity atoms, the depletion capacitance is not a function of temperature.

The apparatus used to make measurements of the depletion capacitance at different ambient temperatures consists of an aluminum cylinder which is thermally insulated by being placed inside a closed dewar. The temperature is raised by a heating strip embedded inside the aluminum cylinder and is lowered by introducing an appropriate amount of liquid nitrogen into the dewar. A thermocouple measures the temperature of the cylinder. The diode rests with its n-type wafer on the cylinder with which it is in good thermal and electrical contact. An insulated probe establishes the electrical connection with the indium dot of the alloyed p-region (see chapter II, section 4.3). The capacitance is measured with a Boonton Capacitance Bridge Model 74C-S8 at a fixed frequency of 100 kc/s. The error of measurement is about 1 percent.

As a result of careful measurements, it has been

established that if one of the junction regions is near intrinsic then the capacitance is temperature dependent. The effect is present in a large range of reverse biases and cannot be explained in terms of a diffusion capacitance. To eliminate this effect, care was taken to make capacitance measurements at temperatures at which both junction regions were known to be extrinsic. Measurements were made at room temperature on diodes alloyed on 0.5 Ω-cm, 12 Ω-cm and 42 Ω-cm n-type wafers and at -65° C on diodes alloyed on near intrinsic n-type wafers. Room temperature measurements were also made on commercial 2N1308 General Electric alloyed germanium structures. The results are shown in figure 2.10. In this log-log plot, the slopes for the junctions alloyed in the laboratory range from -0.475 to -0.50 and is -0.45 for the commercial sample. These results, compared with the theoretical value of -0.5 predicted by equation 2.5, indicate that the diodes fabricated are abrupt junctions.

Another anomalous effect has been observed on these capacitance measurements. If, in a p-n-p structure, the reverse bias of the junction under observation is large enough for the depletion layer in the n-region to penetrate to the opposite junction, then an appreciable increase in the capacitance is observed, as shown in region II of figure 2.11. A large number of measurements were made on

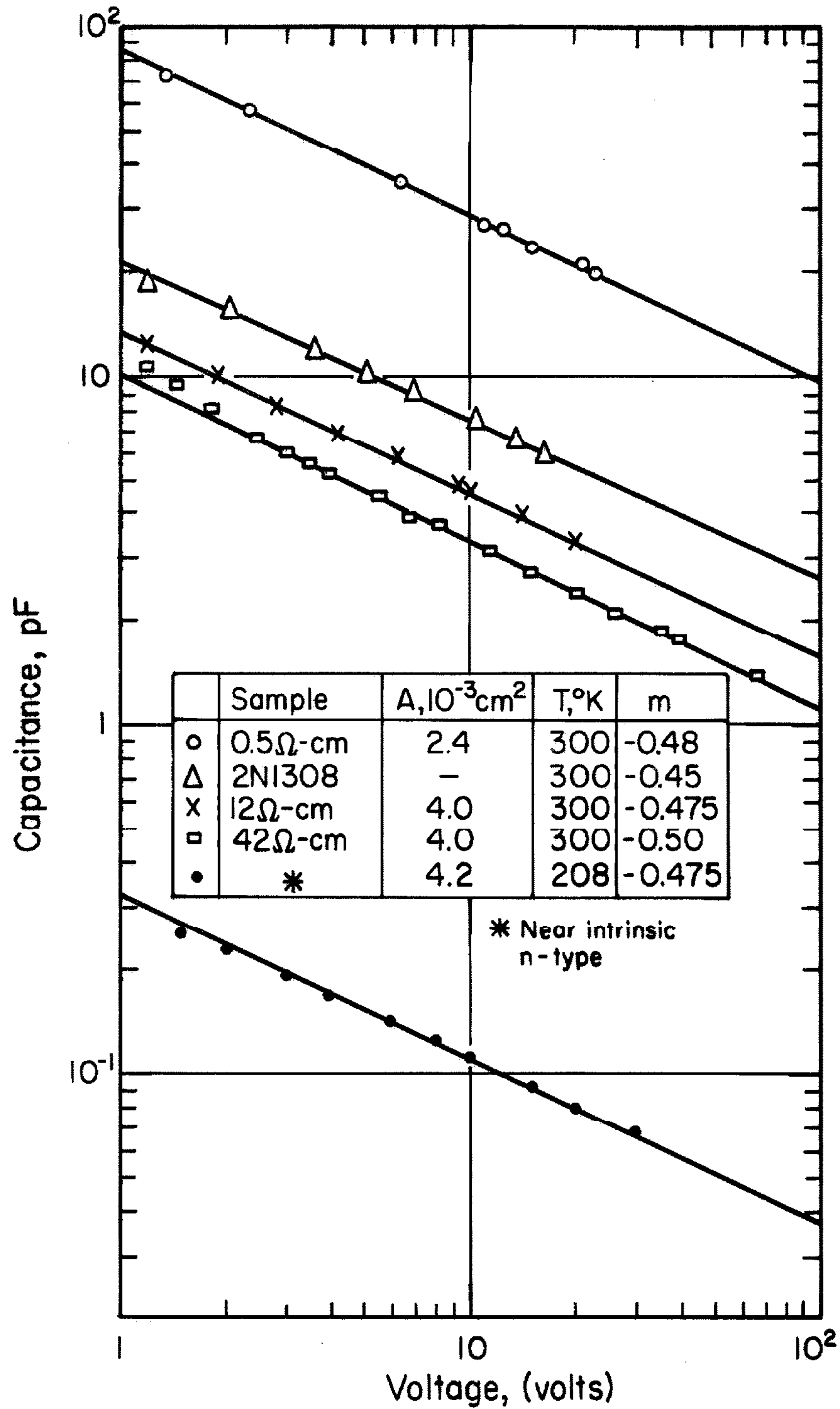


Figure 2.10. Reverse junction capacitance of alloyed germanium p-n junctions.

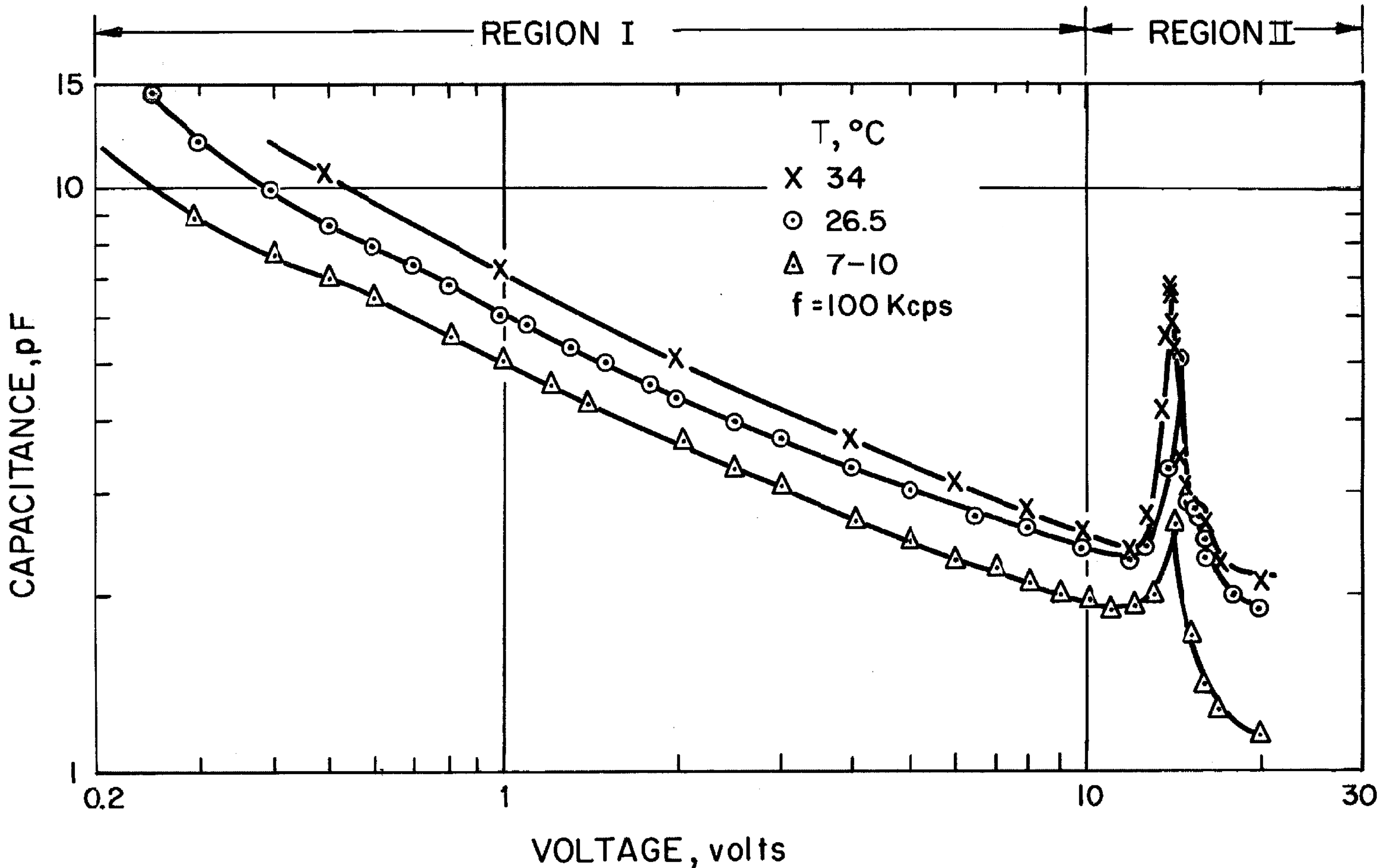


Figure 2.11. Reverse junction capacitance of an alloyed p-n-p structure ($V_{pt} \sim 13V$) with a floating junction configuration.

commercial samples (GE 2N1308 transistors) and it was observed that this effect is strongly dependent on temperature and frequency. It is clear that the effect is due to the interaction of the depletion layer with the transition region of the floating junction. The exact nature of this interaction, however, is not too well understood. The temperature dependence of the capacitance shown in region I of figure 2.11 is that discussed in the previous paragraph.

4.5 V-I Characterization of P-N Junctions. The V-I characterization of the junction is used as a yardstick for evaluating the fabrication process. Any defects in the junction structure and any surface leakage effects are very readily observed in the reverse junction characteristics. The former gives rise to low breakdown voltages and the latter reduces the reverse resistance of the junction. These effects are shown in figure 2.12a and 2.12b, respectively. Figure 2.12c depicts a reverse characteristic in which neither of these effects is present. This characteristic is typical for the average diodes fabricated, and such results were obtained with a high degree of reproducibility. Very few of the junctions showed breakdown voltages less than 150 V. If surface leakage effects were present, then the surface was retreated to remove them. The apparatus used to measure the V-I characteristic is described in appendix C.

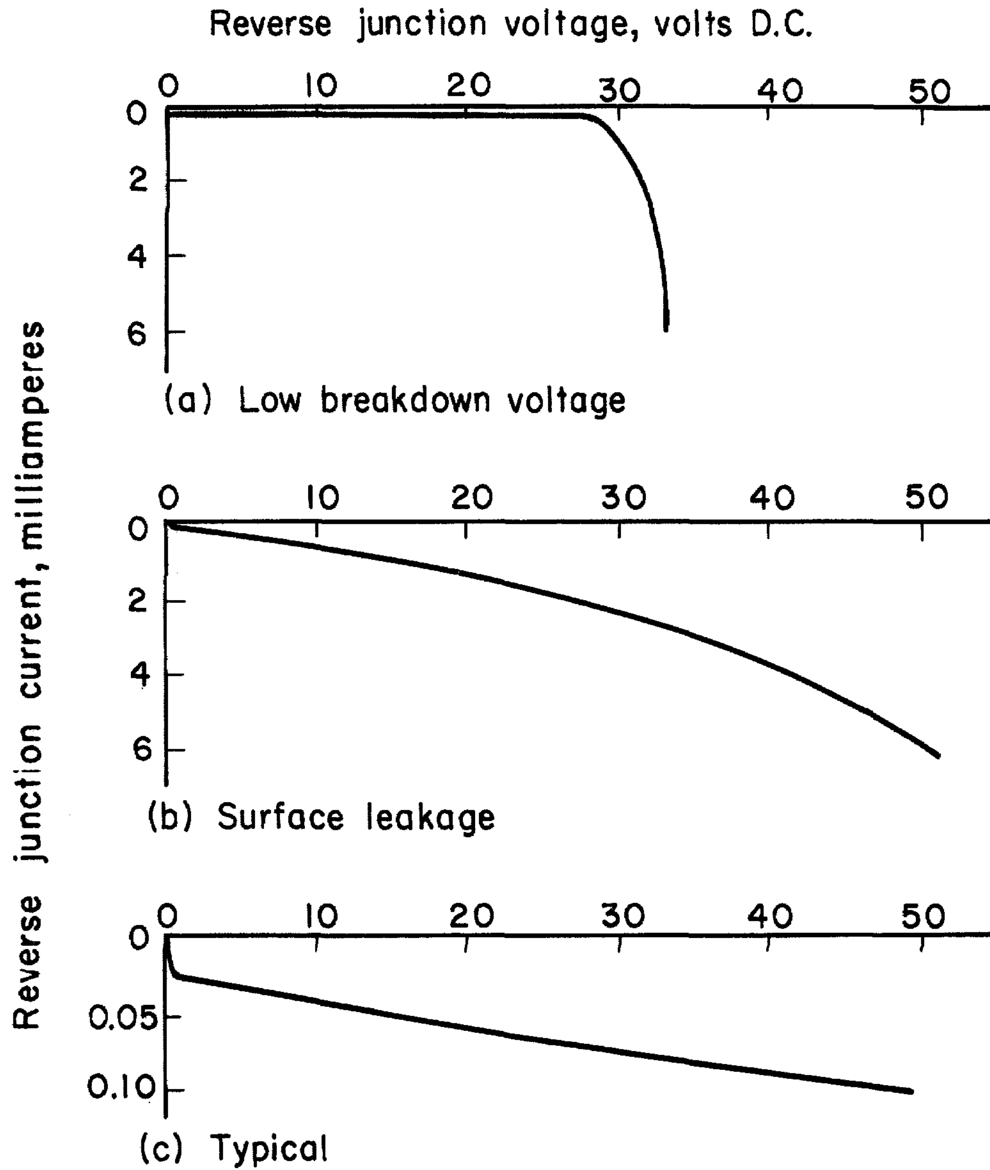


Figure 2.12. Reverse junction V-I characteristics

As a further check on the electrical rectifying properties of the junctions, the experimental V-I characteristic is compared with that predicted by theory. From theory the saturation current for an alloyed junction in which the p-region is much more highly doped than the n-region, is

$$I_s = q \left(\frac{D_p}{\tau_p}\right)^{1/2} p_n A \qquad (2.6)$$

where I_s is the saturation current, A the area of the junction, p_n the minority carrier (hole) concentration in the n-region, D_p the diffusion constant and τ_p the lifetime of the minority charge carriers. For a typical diode, at room temperature, $p_n = 2.1\ 10^{13}$ cm^{-3}, $D_p = 49$ cm^2 sec^{-1}, τ_p = 11 μs, A = 4 10^{-3} cm^2, and I_s = 28 μa. From equation 2.6 the calculated saturation current is 28.1 μa. The accuracy of the agreement is believed to be somewhat fortuitous.

According to the simple theory of p-n junctions, the saturation current should be constant for voltages greater than approximately 1 V. According to figure 2.12c, however, the reverse current increases from 28 μa at 1 V to 100 μa at 50 V. This increase is interpreted as due to the non-vanishing contribution of generation-recombination effects in the space charge region of the junction.

4.6 Junction Separation Distance in P-N-P Structures. The separation distance between the two junctions of the fabricated p-n-p structures is an important parameter whose value has to be known accurately in each sample. This value has been determined by three different, independent methods.

The first, and most accurate, method is that of a direct measurement of the base width by metallurgical techniques. Its disadvantage is that the sample is destroyed in this process and that it can therefore be applied only as a concluding experimental step. The method has been applied to all samples investigated and is described in section 4.1 of this chapter.

The second method uses the basic principles of a reverse-biased p-n junction in a p-n-p structure. For abrupt and strongly non-symmetrically doped junctions obtained by alloying, the width d of the depletion region established by the reverse-bias V is

$$d = \left(\frac{2\, \epsilon \epsilon_o\, (V + V_j)}{q N_D} \right)^{1/2} \qquad (2.7)$$

where the symbols have their conventional meaning. This depletion region will reach the boundary of that of the floating junction at a "punch-through" voltage whose value is given by

$$W = \left(\frac{2\,\epsilon\epsilon_o\,(V_{pt} + V_j)}{qN_D} \right)^{1/2} + \left(\frac{2\,\epsilon\epsilon_o\,V_j}{2N_D} \right)^{1/2} \qquad (2.8)$$

where the second term is due to the depletion region of the floating junction. For most p-n-p structures the punch-through voltage is usually large compared to the built-in potential V_j, and for such cases the base width W is proportional to the square root of V_{pt}.

A simple way to determine the value of the punch-through voltage is to apply a reverse bias in the form of a sawtooth across one junction and to measure the floating potential of the other p-side with respect to the first. The two potentials are displayed on a dual-trace oscilloscope (see appendix C for details). A typical result is shown in figure 2.13. As long as the depletion region does not extend across the full base width, the potential difference between the two p-sides increases (region I in figure 2.13). At punch-through, the depletion region has reached its fullest extent and the potential difference remains constant at the value V_{pt}.

This method is often used to determine base widths. The punch-through voltage has been measured on several samples. The results are shown in table 2.2. It is seen that the measured values depend upon the ambient temperature. The punch-through voltage increases for decreasing temperature. This variation cannot be accounted for by the

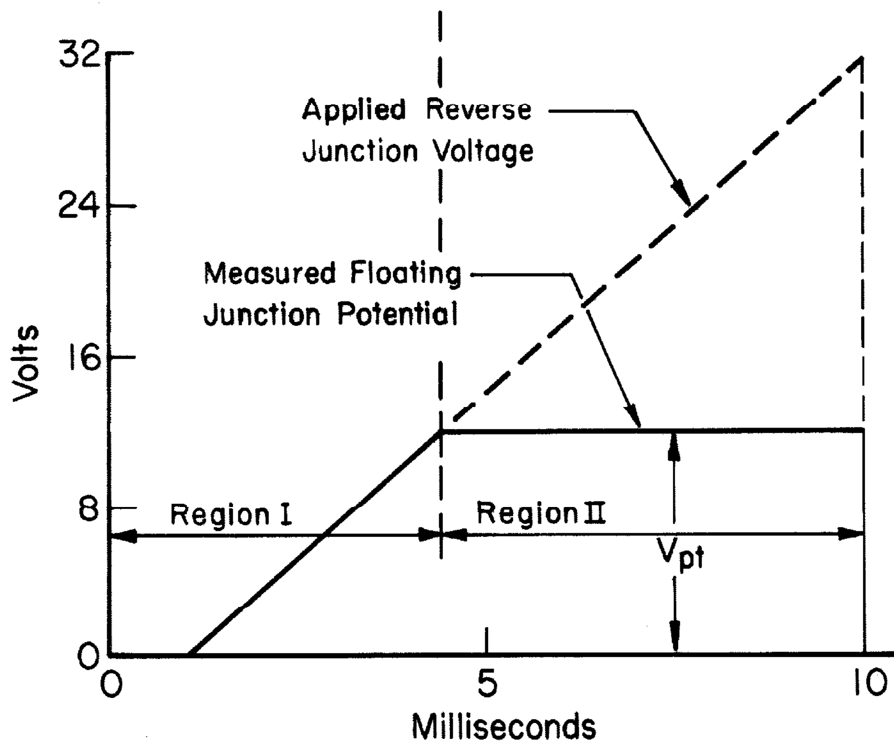


Figure 2.13. A punch-through voltage measurement for a typical fabricated p-n-p structure. All potentials are measured with respect to the p-region of the reverse-biased junction.

simple one-dimensional theory presented here, so that the interpretation of punch-through voltage measurements in terms of equation 2.8 is questionable. Base width measurements based on this method are therefore considered unreliable and have been discarded in the final analysis.

Table 2.2

Punch-through Voltage V_{pt} as a Function of Temperature for 4 Different Samples

Temperature °K	V_{pt} in Volts			
	1	2	3	4
300	20	40	4.0	10
195				11
78	23	45	5.6	
3	26			

The <u>third</u> method is based on an analysis in which the p-n-p structure is viewed as a transistor. A voltage is applied across the emitter and collector terminals with the base floating. If the value of the applied voltage is less than kT/q, then there is a linear relationship between the voltage and the current as shown in figure 2.14. The structure in this range of operation can be represented by an equivalent resistance R (see appendix B). The relationship between R and the base width W is

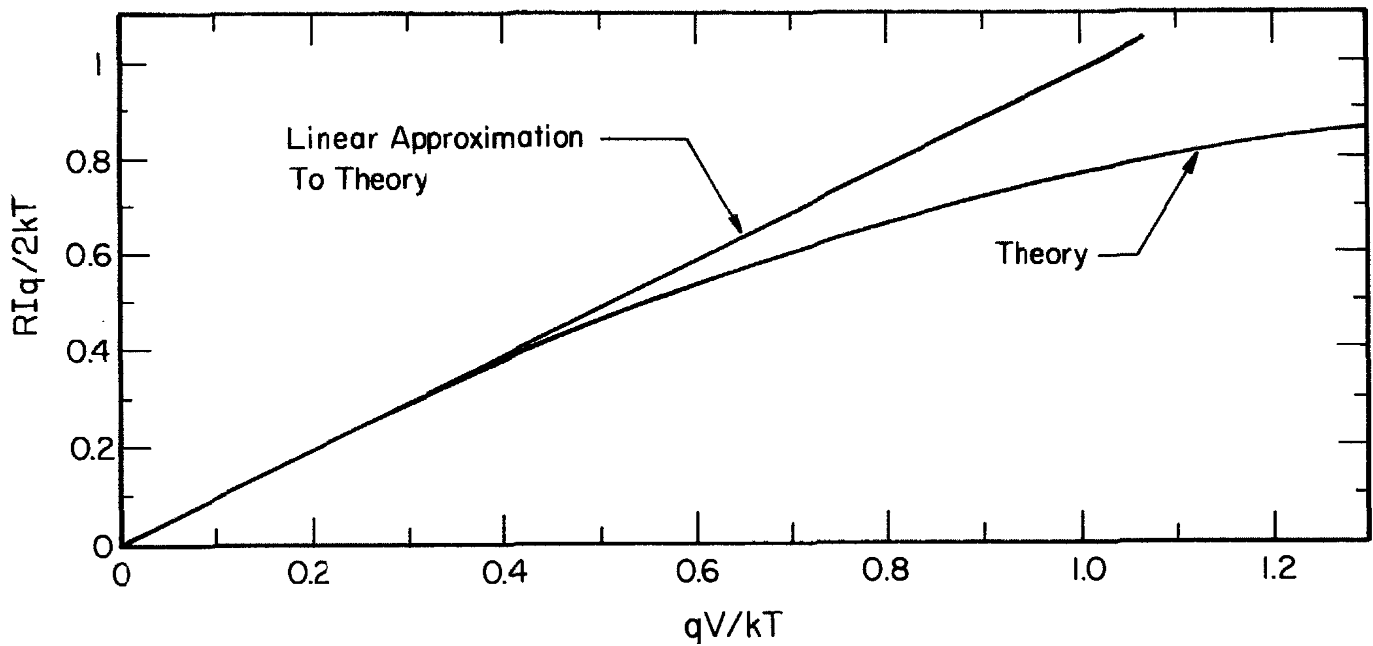


Figure 2.14. Normalized V-I characteristic of a p-n-p structure with the base floating.

$$W = q \mu_p p_n R A \tag{2.9}$$

where p_n is the minority carrier concentration in the base region, μ_p the mobility of the minority charge carriers, and A the junction area. The only restriction placed on this equation is that the base width be much less than the diffusion length of the minority charge carriers in the base region. This is not a severe restriction for any of the structures fabricated, since their base width is always much less than the diffusion length of the minority charge carriers.

The resistance R is determined from the linear current-voltage characteristic when a small voltage signal less than 0.1 kT/q is applied across the emitter and collector terminals. Typical numerical values at ambient temperature of 26.5° C are: $R = 0.75$ mV/8 μa $= 93.8\ \Omega$, $A = 4.31\ 10^{-3}$ cm^2, $\mu_p = 1900$ cm^2/Vs, $p_n = 2.1\ 10^{13}$ cm^{-3} and $W = 25.8\ 10^{-4}$ cm. The base width of this particular sample measured by the metallurgical method is $27.7\ 10^{-4}$ cm.

The base width of a structure as determined by this third method and by the metallurgical method are compared in figure 2.15. The scatter about the line $W_R = W_M$ is approximately 10%. Since the error in the metallurgical measurement is less than 2%, the error in W_R must be of the order of 10%. Each of the three methods described is used

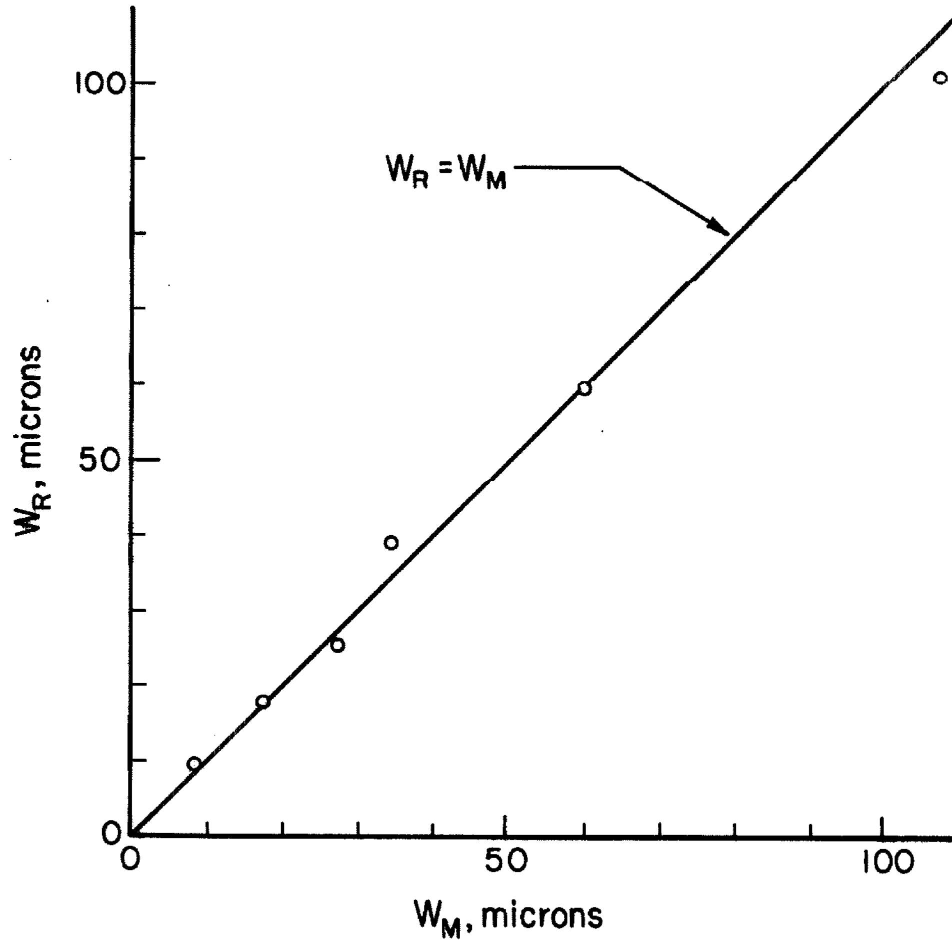


Figure 2.15. A comparison between the base width values determined by the metallurgical (W_M) and the electrical technique (W_R).

for specific purposes. The first method is used to measure accurately the junction separation distance in the p-n-p structure at the end of the electrical measurements. The second method is used to indicate qualitatively the punch-through voltage to be expected when scl current measurements are made. The third method is used to measure qualitatively the junction separation distance before scl current measurements are made, so as to allow for a preliminary evaluation of the results.

4.7 V-I Characterization of a P-N-P Solid-State Diode. The electrical measuring procedure is as follows. A solid-state diode is pulsed with a saw-tooth voltage signal and the resulting V-I characteristic is displayed on the screen of an oscilloscope. The repetition rate and the width of the saw-tooth signal are varied to observe if there are any transient or thermal effects. Although these effects are not observed over a wide range of pulse widths and repetition rates (duty cycle of 50 percent and pulse widths ranging from 10 μs to 10 ms), a duty cycle of 10 percent and a pulse width of 1 ms are used. The peak voltage that is applied is determined by the peak power that can be supplied from the electrical apparatus. This peak power is about 10 watts. A V-I characteristic of each solid-state diode is measured at liquid nitrogen temperature. For a few of the samples, these measurements are

also carried out at 195° K, 273° K, and 300° K. The voltage and the corresponding current are determined directly from the oscilloscope trace. A measurement error of about 5% is expected.

The electrical apparatus used to measure these V-I characteristics is described in appendix C.

APPENDIX A

IMPEDANCE OF SPACE-CHARGE-LIMITED CURRENTS WITH FIELD DEPENDENT MOBILITY

Introduction

The small-signal impedance presented by space-charge-limited currents in vacuum can be calculated in closed form for a planar structure (26). The solution shows that such an arrangement has an equivalent parallel capacitance which is 3/5 of the geometrical capacitance $C_0 = A\epsilon_0/d$ as long as the period of the sinusoidal perturbation is longer than about twice the dc transit time T_0 of the charge carrier. For frequencies higher than that, the value of this equivalent parallel capacitance is frequency dependent. In the limit of very high frequencies, its value approaches that of the purely geometrical capacitance $A\epsilon_0/d$. Recently, Shao and Wright (8) have analyzed the small-signal impedance presented by space-charge-limited currents in a dielectric medium. This case differs from the previous one by the modified relation which exists between the electric field E and the velocity v of the mobile charge carriers. These authors assume proportionality between v and E. Their solution shows that in this case, the equivalent parallel capacitance is 3/4 of the geometrical capacitance $C_0 = A\epsilon\epsilon_0/d$ for sinusoidal perturbations whose period is longer than about twice the dc transit time T_0 of the charge carriers.

Beyond this, the value of the equivalent parallel capacitance is again frequency dependent. At very high frequencies, its value again approaches that of the purely geometrical capacitance $A\varepsilon\varepsilon_o/d$.

Proportionality between charge carrier velocity v and electric field E implies a constant charge carrier mobility μ. It is a well established fact that in semiconductors, such as germanium, the mobility is not constant, but decreases with increasing field strength. Beyond a critical field E_c, the velocity obeys the relation (11) $v = \mu\sqrt{E_c E}$. It is the purpose of this investigation to determine how this modification affects the resultant small-signal impedance of space-charge-limited currents.

This problem is studied under the assumption that the period of the small-signal perturbation is long compared to the dc transit time of the charge carriers. This restriction is imposed by the appearance of integrals which can be evaluated only numerically for arbitrary frequencies. On the other hand, the generalization to a relationship of the form $v = \mu E_c(E/E_c)^{1/n}$ does not present major difficulties for this restricted range of frequencies. Such a dependence is relevant to very hot charge carriers (11). The analysis is therefore carried out for this general form of velocity-field relationship. Except for the change in the field-velocity relationship, the model is identical to that of references

(26) and (8). Its essential features are: a) planar geometry, b) carrier injection at $x = 0$ with zero initial velocity, c) collection of the charge carriers at $x = d$ and d) negligible diffusion processes.

Theory

The fundamental relations which govern the flow of space-charge-limited currents are the law of conservation of charge, Poisson's equation and the velocity-field relationship

$$\frac{\partial(\rho v)}{\partial x} = -\frac{\partial \rho}{\partial t} \qquad (1)$$

$$\frac{\partial E}{\partial x} = \frac{\rho}{\epsilon \epsilon_0} \qquad (2)$$

$$v = \mu E_c (E/E_c)^{1/n} \qquad (3)$$

With appropriate boundary conditions, these three equations determine the values of the electric field E, and of the density ρ and the velocity v of the charge carriers as a function of both the coordinate x and the time t. The continuity equation can be integrated once if the charge density ρ is eliminated by Poisson's equation to obtain

$$\epsilon \epsilon_0 \left(v \frac{\partial E}{\partial x} + \frac{\partial E}{\partial t} \right) = j(t) \qquad (4)$$

The constant of integration $j(t)$ represents the total current density of the arrangement and is independent of the coordinate x. If the velocity v is now interpreted as that of a

particular charge carrier, we have

$$v = \frac{dx(t)}{dt} , \tag{5}$$

where $x(t)$ is the location of that charge carrier as a function of time. The left-hand side of equation 4 then is a total differential for $E(x(t), t)$ and the equation can be integrated again

$$\epsilon\epsilon_o E(t,\bar{t}) = \int_{\bar{t}}^{t} j(t)dt \tag{6}$$

where it is assumed that the charge carrier under consideration is emitted at $x = 0$ with a zero velocity at an arbitrary instant of time $\bar{t}$. Substitution of the field-velocity relation 3 leads to

$$\left(\frac{\epsilon\epsilon_o}{\mu^n E_c^{n-1}} \right)^{1/n} \frac{dx}{dt} = \left(\int_{\bar{t}}^{t} j(t)dt \right)^{1/n} \tag{7}$$

from which the position of a charge carrier can be found through a final integration. Then

$$\left(\frac{\epsilon\epsilon_o}{\mu^n E_c^{n-1}} \right)^{1/n} x(t, \bar{t}) = \int_{\bar{t}}^{t} \left(\int_{\bar{t}}^{t} j(t)dt \right)^{1/n} dt. \tag{8}$$

To determine the impedance of space-charge-limited currents, the expression

$$\triangle V(t) = V(0,t) - V(x,t) = \int_0^x E(x,t)dx \qquad (9)$$

has to be evaluated at any given instant of time t. The desired function $E(x, t)$ can be derived from the known function $E(t, \bar{t})$ of equation 6. This expression gives the field strength at the point at which the charge carrier is located at time t if it was emitted at time $\bar{t}$. Equation 8 on the other hand, gives the location of the charge carrier at time t if it was emitted at time $\bar{t}$. Thus, the time of emission $\bar{t}$ of a charge carrier located at a point x at any instant of time t is obtained by solving equation 8 for $\bar{t}(x, t)$. This time of emission is substituted into the known function $E(t, \bar{t})$ to find the desired field distribution $E(t,x)$.

This program will be carried out for a dc current density j_o upon which a sinusoidally varying component $j_1 e^{i\omega t}$ is superimposed. Thus

$$j(t) = j_o + j_1 e^{i\omega t} \qquad (10)$$

and

$$E(t,\bar{t}) = j_o(t-\bar{t}) + \frac{j_1 e^{i\omega\bar{t}}}{i\omega}\left(e^{i\omega(t-\bar{t})} - 1\right) \qquad (6a)$$

and

$$\left(\frac{\epsilon\epsilon_o}{\mu^n\ E_c^{n-1}}\right)^{1/n} \frac{dx}{dt} = \left[j(t-\bar{t}) + \frac{j_1 e^{i\omega\bar{t}}}{i\omega} \left(e^{i\omega(t-\bar{t})} -1\right)\right]^{1/n} \tag{7a}$$

In this last equation, the complex notation is at fault unless the following considerations are restricted to a small sinusoidal perturbation, in which case the linear term in a binomial expansion is the only significant one. Then

$$\left(\frac{\epsilon\epsilon_o}{\mu^n E_c^{n-1}}\right)^{1/n} \frac{dx}{dt} = \left(j_o(t-\bar{t})\right)^{1/n} + \left[\frac{1}{n}\left(j_o(t-\bar{t})\right)^{(1-n)/n}\right] \cdot \left[\frac{j_1 e^{i\omega\bar{t}}}{i\omega} \left(e^{i\omega(t-\bar{t})} -1\right)\right], \tag{7b}$$

so that

$$\left(\frac{\epsilon\epsilon_o}{\mu^n\ E_c^{n-1}}\right)^{1/n} x(t,\bar{t}) = \frac{n}{n+1}\ j_o^{1/n}(t-\bar{t})^{(1+n)/n} + \frac{1}{n}\ j_o^{(1-n)/n}\ \frac{j_1 e^{i\omega\bar{t}}}{i\omega} \int_0^{t-\bar{t}} z^{(1-n)/n}\left(e^{i\omega z} -1\right) dz \tag{8a}$$

The integral cannot be evaluated in closed form for positive values of n unless $n = 1$ (case of Shao and Wright). It will therefore be assumed that the transit times $t - \bar{t}$ considered are sufficiently short compared to the period of perturbation so that a Taylor expansion of the integrand is justifiable. Then

$$\left(\frac{\epsilon\epsilon_o}{\mu^n E_c^{n-1}}\right)^{1/n} x = \frac{n}{n+1}\, j_o^{1/n}\, (t-\bar{t})^{(1+n)/n} +$$

$$+ j_o^{(1-n)/n}\, j_1 e^{i\omega\bar{t}} \left(\frac{1}{n+1}\, (t-\bar{t})^{(1+n)/n} + \right. \qquad (8b)$$

$$\left. + \frac{i\omega}{2!}\,\frac{1}{2n+1}\,(t-\bar{t})^{(1+2n)/n} + \frac{(i\omega)^2}{3!}\,\frac{1}{3n+1}(t-\bar{t})^{(1+3n)/n} + \ldots \right)$$

This equation is readily solved for $\bar{t}$ by an approximate procedure. Since the sinusoidal current density j_1 is but a small perturbation of the dc current density j_o, it may be expected that the time of emission $\bar{t}$ will deviate only little from that found in dc operation. If for this latter case a charge carrier needs a lapse of time t_o to reach a point x, the transit time with superimposed perturbation will be $t_o + t_1$, where $t_1 << t_o$. The time of emission then is

$$\bar{t} = t - (t_o + t_1). \qquad (11)$$

This expression is substituted into equation 8b. With $j_1 = 0$, it is found that

$$t_o = (ax)^{n/(n+1)} \qquad (12a)$$

where

$$a = \left(\frac{\epsilon\epsilon_o}{\mu^n E_c^{n-1}\, j_o}\right)^{1/n} \frac{n+1}{n} \qquad (12b)$$

With this, it then follows from perturbation terms of the first order only in j_1 and t_1 that

$$t_1 = -\frac{j_1 e^{i\omega t}}{j_o}\left(\frac{1}{n+1}\,t_o - \frac{i\omega}{2!}\,\frac{3n+1}{(n+1)(2n+1)}\,t_o^2\right) \qquad (13)$$

Expressions 11, 12 and 13 are now substituted into equation 6a and the exponentials are appropriately expanded, as is consistent with the assumption of sufficiently long perturbation periods. One then finds

$$\epsilon\epsilon_o E(x,t) = j_o t_o + j_o t_1 + j_1 e^{i\omega t}\left(t_o - \frac{i\omega}{2!}\,t_o^2\right), \qquad (14)$$

where the dependence upon x is expressed through t_o and t_1 of equations 12 and 13. The voltage drop ΔV can now be evaluated. Expressed in terms of t_o, the result is

$$\Delta V(t) = \frac{n+1}{2n+1}\,\frac{j_o t_o x}{\epsilon\epsilon_o} - \frac{j_1 e^{i\omega t}}{\epsilon\epsilon_o}\left(\frac{n}{2n+1}\,t_o x - i\omega\,\frac{n^2}{(2n+1)(3n+1)}\,t_o^2 x\right) \qquad (15)$$

If the total length of path for the space-charge-limited current is d and the corresponding dc transit time as given by equation 12 is T_o, the dc resistance R is

$$R = \frac{n+1}{2n+1}\,\frac{T_o d}{A\epsilon\epsilon_o} = \frac{n+1}{2n+1}\,\frac{T_o}{C_o} \qquad (16)$$

where A is the area of the current path and C_o is the geometrical capacitance of the structure. The small-signal impedance is

$$Z = \frac{n}{2n+1} \frac{T_o d}{A\epsilon\epsilon_o} - i\omega \frac{n^2}{(2n+1)(3n+1)} \frac{T_o^2 d}{A\epsilon\epsilon_o} \quad (17)$$

Expressed in terms of an equivalent parallel resistance R_1 and an equivalent parallel capacitance C_1, the impedance is given by

$$R_1 = \frac{n}{2n+1} \frac{T_o d}{A\epsilon\epsilon_o} = \frac{n}{2n+1} \frac{T_o}{C_o} \quad (18)$$

$$C = \frac{2n+1}{3n+1} \frac{A\epsilon\epsilon_o}{d} = \frac{2n+1}{3n+1} C_o$$

APPENDIX B

RESISTANCE - BASE WIDTH RELATIONSHIP: THEORY

For applied voltages less than the punch-through voltage, the theoretical expression for the current-voltage relationship of the germanium solid-state diode is essentially that of the floating base transistor. From transistor theory (27), the current I that will flow when a voltage V is applied across the solid-state diode, is

$$I = I_e = G_{11}\frac{kT}{q}\,(e^{qVe/kT}-1) + G_{1r}\,\frac{kT}{q}\,(e^{qVc/kT}-1) \qquad \text{(B.1)}$$

and is also equal to $-I_c$, where

$$I_c = G_{1r}\frac{kT}{q}(e^{qVe/kT}-1) + G_{11}\frac{kT}{q}\,(e^{qVc/kT}-1) \qquad \text{(B.2)}$$

According to the current and voltage convention as shown in figure B.1, $V = V_e - V_c$. These expressions can be considerably simplified if the reverse saturation electron current at the emitter and at the collector is assumed to be negligible compared with the reverse saturation hole current at these junctions. This simplification is possible because the resistivity of the n-region is much higher than that of the p-regions. For this case

$$G_{11} = q\,\mu_p p_n\,\frac{A}{L_p}\quad \coth(W/L_p)$$

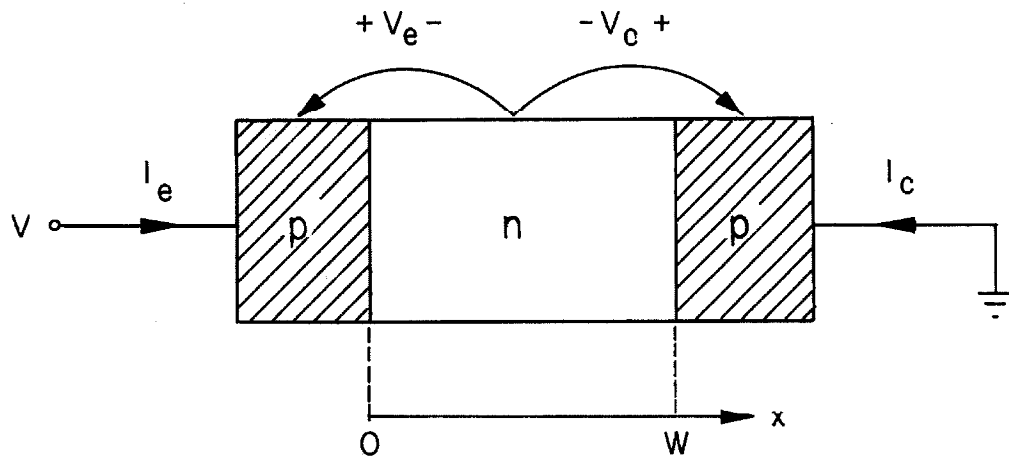


Figure B.1. A one-dimensional floating base transistor configuration.

and

$$G_{1r} = -q\, \mu_p \;\; p_n \; \frac{A}{L_p} \quad \frac{1}{\sinh(W/L_p)}$$

where p_n is the minority mobile charge carrier (hole) density in the n-region, L_p the diffusion length of the holes injected into the base, μ_p the hole mobility, W the base width, and A the junction area. Since I_e is equal to $-I_c$, then

$$e^{qV_e/kt} - e^{qV_c/kT} = 2$$

which reduces to

$$V_e = -V_c = -V/2$$

for $V << kT/q$. Hence equation B.1 can be expressed as

$$I = (G_{11} - G_{1r}) \quad V/2 \qquad (B.3)$$

where

$$G_{11} - G_{1r} = q\, \mu_p\, p_n \; \frac{A}{L_p} \; \frac{\cosh(W/L_p) + 1}{\sinh\,(W/L_p)} \qquad (B.4)$$

If we set $V/I = R$, then

$$R = 2/(G_{11} - G_{1r}) \qquad (B.5)$$

This signifies that the resistance R of the solid-state diode is constant for applied voltages much less than kT/q. If $W < L_p$ such that $(W/L_p)^2 << 1$, then equation B.4 can be

expressed as

$$G_{11} - G_{1r} = 2q\, \mu_p\, p_n\, A/W$$

Equation B.5 can now be written as

$$W = q\, \mu_p\, p_n\, AR \qquad \text{(B.6)}$$

This is an important result in that if the electrical properties of the base material are already known and if $W^2 << L_p^2$, then the base width W can be determined directly from the resistance measurement.

It should be noted that the measurement of R has been carried out at a temperature (273° K) at which the base material of the sample is near extrinsic. The above analysis, which is based on a low injection mode of operation, is not applicable, since even for very same applied voltages the sample operates in the high injection mode. It is well known, however, that a corresponding analysis in the high injection mode (28) leads to the same result as expressed in equation B.6. This dependence is thus assumed to be always valid.

APPENDIX C

ELECTRICAL MEASURING APPARATUS

The block diagram of the electrical measuring apparatus is shown in figure C.1. A saw-tooth voltage signal of fixed amplitude but of variable duty cycle and pulse width is generated by an externally triggered Tektronix oscilloscope Type 543. A high current two stage cathode follower is used to increase the power output. The V-I characteristic of the solid-state diode, which is maintained at a particular ambient temperature, is traced on the screen of a Tektronix oscilloscope Type 503.

In figure C.2 the circuit diagram of the apparatus is shown. The set of attenuators adjust the amplitude of the input signal to the cathode follower, while the d-c grid bias voltages minimize the d-c plate current. A set of protection resistors are connected at the output of the amplifier. The sample is placed across terminals A and B.

In figure C.3, a mounted sample is shown. To measure the V-I characteristic of a solid-state diode, the emitter lead is connected to terminal A, and the collector lead to terminal B. To measure the V-I characteristic of the p-n junction, the base lead is connected to terminal A and the collector lead to terminal B. This is the same connection as used for punch-through voltage measurement

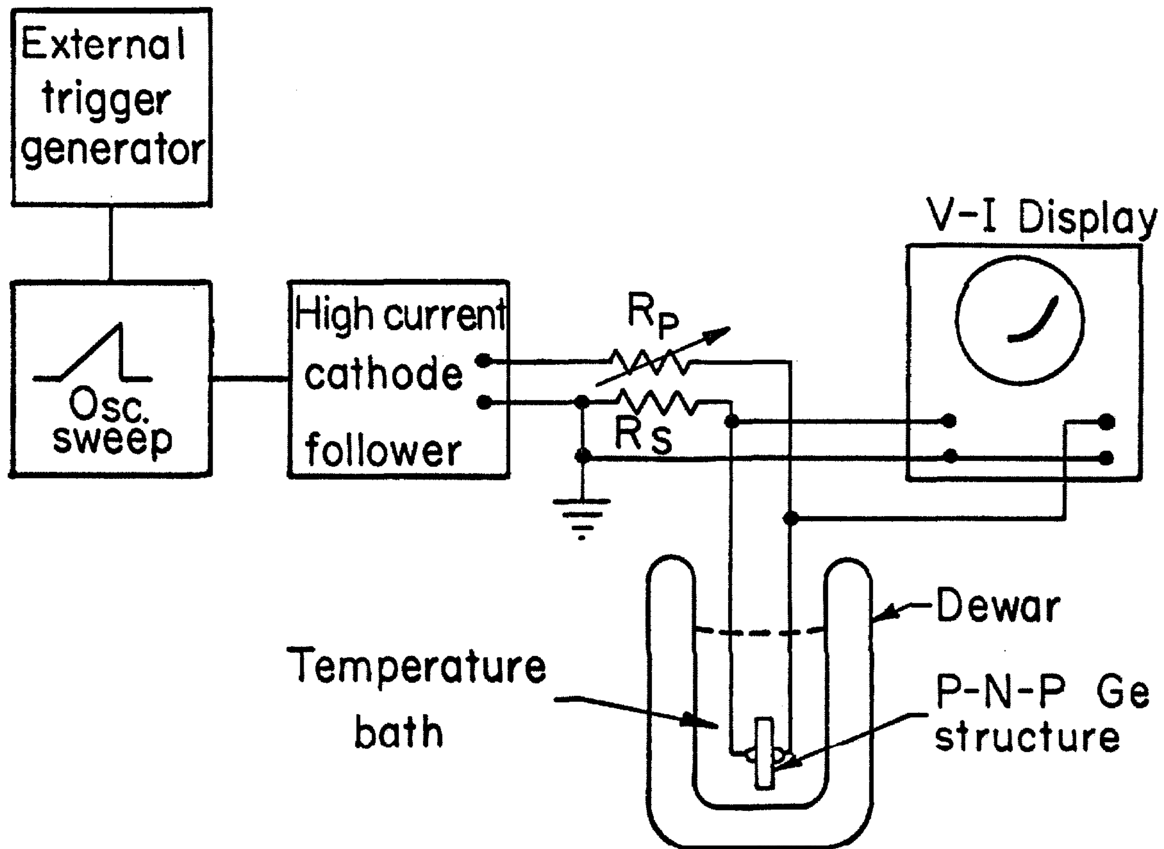


Figure C.1. Block diagram of the electrical measuring apparatus.

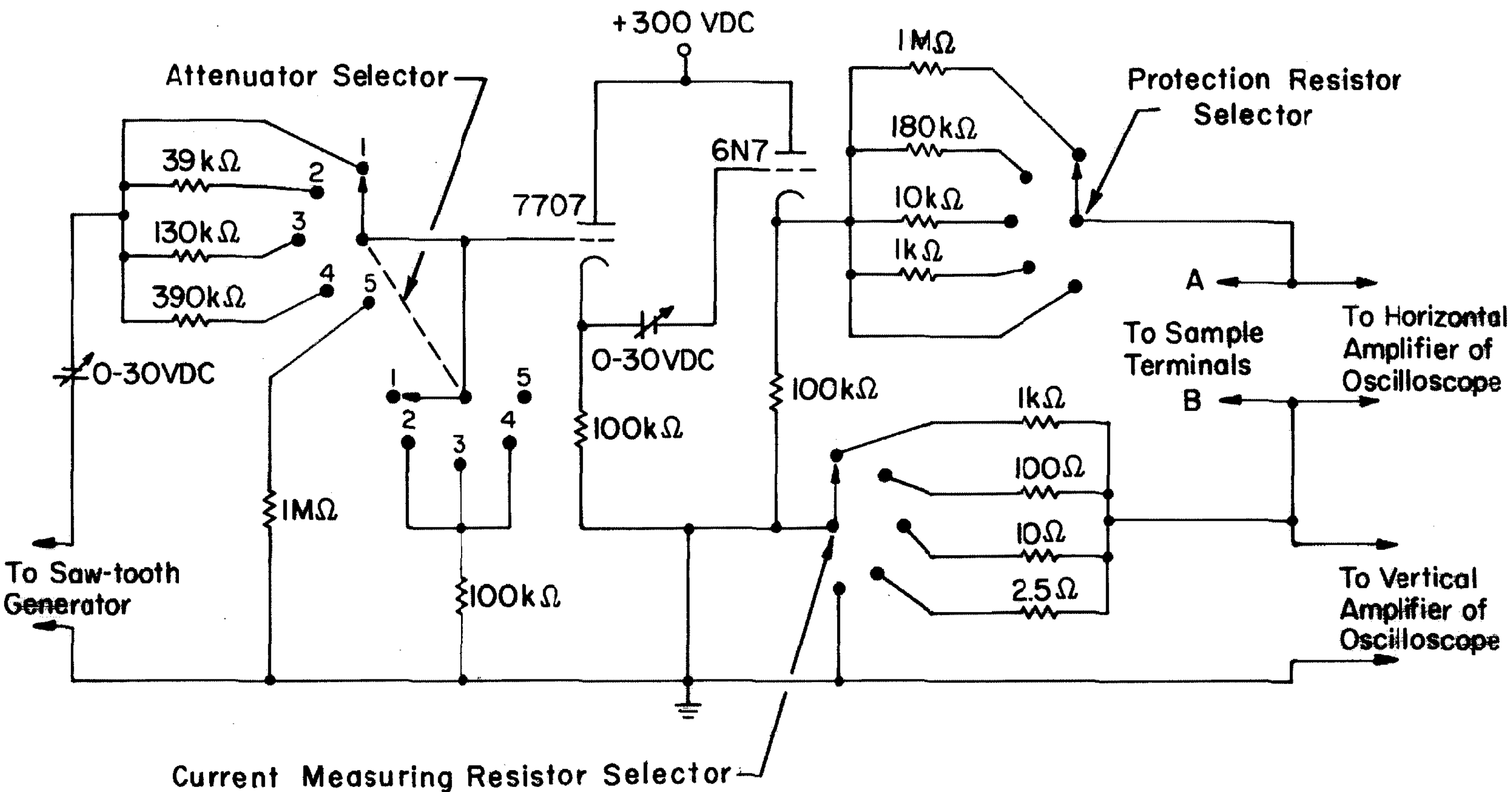


Figure C.2. Circuit diagram of the electrical measuring apparatus.

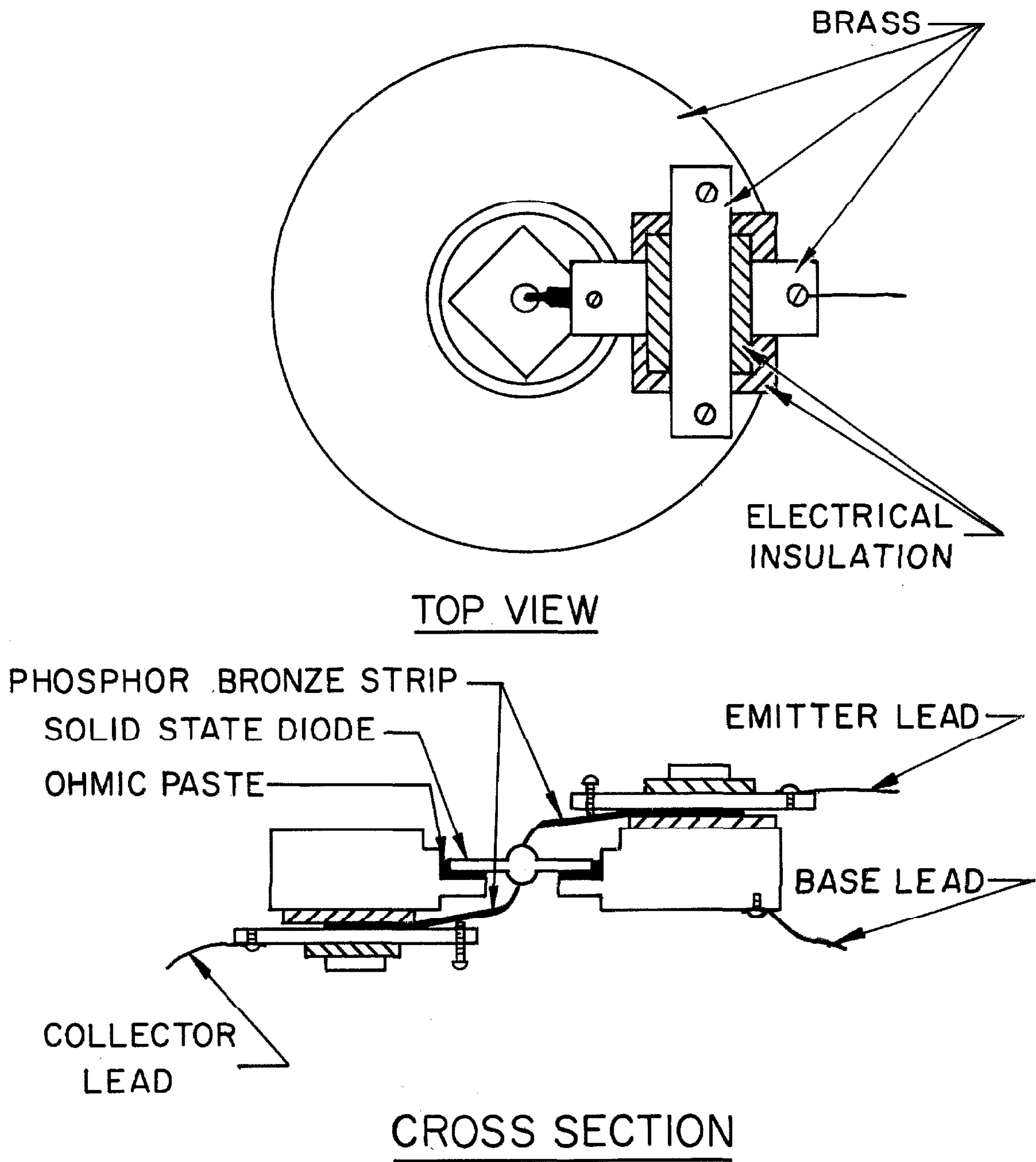


Figure C.3. A mounted solid-state diode.

except that in the latter case the current measuring resistors are shorted out. The voltage across the reverse-biased junction and the voltage of the floating junction are measured with respect to ground on the dual trace screen of the Type 543 oscilloscope.

For different ambient temperatures, the sample is placed in a temperature bath of liquid nitrogen for $T = 78^{o}K$ and of dry ice mixed with liquid pentane for $T = 195^{o}$ K. For $T = 273^{o}$ K a temperature bath of liquid pentane surrounded by an ice-water mixture is used.

REFERENCES

1. G. T. Wright, "Space-Charge-Limited Solid-State Devices",Proc. IRE, 61, 1642-1652 (1963).

2. N. F. Mott and R. W. Gurney, Electronic Processes in Ionic Crystals, Oxford University Press, London (1940); pp. 168-173.

3. W. Shockley and R. C. Prim, "Space-Charge-Limited Emission in Semiconductors", Phys. Rev. 90, 753-759 (1953).

4. G. C. Dacey, "Space-Charge-Limited Hole Current in Germanium", Phys. Rev. 90, 759-764 (1953).

5. A. Rose, "Space-Charge-Limited Currents in Solids", Phys. Rev. 97, 1531-1538 (1955).

6. A. Rose and R. W. Smith, "Space-Charge-Limited Currents in Single Crystals of Cadmium Sulfide", Phys. Rev. 97, 1531-1537 (1955).

7. G. T. Wright, "Space-Charge-Limited Currents in Insulating Materials", Nature 182, 1296-1297 (1958).

8. J. Shao and G. T. Wright, "Characteristics of the Space-Charge-Limited Dielectric Diode at Very High Frequencies" Solid-State Electron. 3, 291-303 (1961).

9. E. J. Ryder, "Mobility of Holes and Electrons in High Electric Fields", Phys. Rev. 90, 766-769 (1953).

10. C. T. Sah, R. N. Noyce and W. Shockley, "Carrier Generation and Recombination in P-N Junctions and P-N Characteristics", Proc. IRE. 45, 1228-1243 (1957).

11. W. Shockley, "Hot Electrons in Germanium and Ohm's Law", Bell Syst. Tech. J. 30, 990-1034 (1951).

12. M-A. Nicolet, "The Distribution of Free Charge Carriers, of Electric Field, and of Electrostatic Potential in a P-I Junction at Thermal Equilibrium", Calif. Inst. of Technology, Solid State Electronics Laboratories Report, (1963).

13. J. Lindmayer, J. Reynolds and C. Wrigley, "One-Carrier Space-Charge-Limited Current in Solids", J. Appl. Phys. 34, 809-812 (1963.

14. R. N. Hall, "Variation of the Distribution Coefficient and Solid Solubility with Temperature", J. Phys. Chem. 3, 63-73 (1957).

15. R. Dreiner and R. Garnach, "Precision Orientation of Germanium Crystals in the (111) Direction Using Alloy Pits", J. Appl. Phys. 33, 888-891 (1962).

16. R. A. Smith, Semiconductors, Cambridge University Press, (1959); section 5.4.3.

17. P. P. Debye and E. M. Conwell, "Electrical Properties of N-type Germanium", Phys. Rev. 93, 693-706 (1954).

18. F. J. Morin and J. P. Maita, "Conductivity and Hall Effect in the Intrinsic Range of Germanium", Phys. Rev. 94, 1525-1529 (1954).

19. M. B. Prince, "Drift Mobilities in Semiconductors I. Germanium", Phys. Rev. 92, 681-687 (1953).

20. R. H. Kingston, "Switching Time in Junction Diodes and Junction Transistors", Proc. IRE 42, 829-834 (1954).

21. G. A. Wolff, J. M. Wilbur Jas, and J. C. Clark, "Etching and Orientation Measurements of Diamond Type Crystals by Means of Light Figures", Z. Electrochem. 61, 101-106 (1957).

22. H. E. Bridgers, J. H. Scaff, and J. N. Shive, Transistor Technology, Vol. I, D. Van Nostrand (1958); p. 419.

23. J. I. Pankove, "Effect of Edge Dislocations on the Alloying of Indium to Germanium", J. Appl. Phys. 28 1054-1057 (1957).

24. D. Baker, "Methods of Sectioning and Etching Transistors for Microscopic Examination", Proc. Inst. Elec. Engrs. (London) 106 Part B Suppl. 13-18, 442-444 (1959).

25. J. V. King, "Liquid Alloy for Making Contacts to Metallic and Nonmetallic Surfaces", Rev. Sci. Instr. 32, 1407 (1961).

26. W. W. Harmon, Fundamentals of Electronic Motion, McGraw-Hill, New York (1953); section 6.5.

27. E. Spenke, Electronic Semiconductors, McGraw-Hill New York (1958); pp. 127-133.

28. R. W. Lade and A. G. Jordan, "On the Static Characteristics of High-Low Junction Devices", J. Electron. 13, 23-34 (1962).