Thin Film Silicon for Implantable Electronics

Thesis by

HSI-WEN LO

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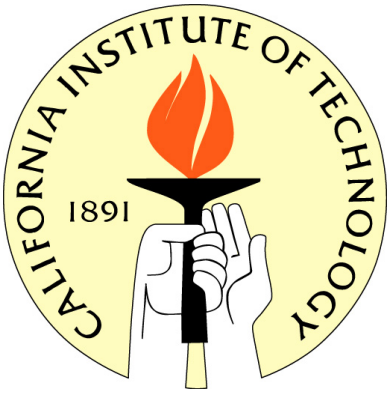
Doctor of Philosophy



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To LORD, Jesus Christ

To my family

Acknowledgements

The LORD was, is, and will always be with me wherever I go. He walked me through the darkest and hardest period of my life. His grace, love and support are the momentum advancing my life.

My studies at Caltech started with a letter to the admission committee. In that letter, I stated that I wanted to invent and build new devices that could change our life greatly and relieve all the lives on earth from pains and sweats, as James Watt did. The steam engine invented and improved by Watt relieved human beings and animals from providing limited amount of energy for productions in a pains taking sense. Before the advent of steam engines, human beings and animals such as horses and cows were widely used in industrial and agricultural productions. The steam engines eliminated the need of humans and animals as "tools and equipment" that provided energy for productions to support our daily life, opened the door to the use of fossil fuels and paved the way to the high living standards we are enjoying now. I hoped, at that time, I could invent something that would greatly change our daily life.

It was Dr. Yu-Chong Tai that moved my ambitions a step forward. In the past five years of working with him, I have gained a lot of knowledge and skills that help me become not only a good researcher but also an excellent leader of a research team. I have always been amazed by Dr. Tai's extensive and intensive knowledge, his keen intuitions for engineering problems, and his excellent management skills. His kindness and generosity add to his accomplishments. I have to thank Dr. Tai, for he has given me a lot of freedom to study whatever I think is interesting and fun. I could not be an independent researcher without the freedom I have enjoyed in the past five years.

I could never finish my Ph.D. studies without support of my family. During the last five years, my family helped me walk through my lows in research and shared my highs. In the third year of my Ph.D. studies, an angel came to my family. Elyse, my niece, was born in August 15, 2006. She has filled my life with happiness and laughters ever since. Although I am more than 6,000 miles away from her, I did not miss Elyse's first smile, first babbling, first stepping, first song, and first dance thanks to the marvelous modern technologies. Now at the edge of my graduation, Adalene, my second niece, is coming to enrich my life. These two angels make my life wonderful.

I would like to thank the current members and previous members of the Caltech Micromachining Laboratory who made my reseach life at Caltech a precious experience. Mr. Trevor Roper is an excellent engineer. He gave me a smooth working experience in the clean room. Mrs. Agnes Tong, Mrs. Christine Garske and Mrs. Tanya Owen are nice secretaries and have saved me a lot of troubles purchasing and traveling. Dr. Ellis Meng, Dr. Jun Xie, Dr. Qing He, Dr. Matthieu Liger, Dr. Justin Boland, Dr. Angela Tooker, Dr. Damien Rodger, Dr. Scott Miserendino, Dr. Changlin Pang, and Dr. Siyang Zheng have provided many precious advices to my research work. Dr. Victor Shih offered me more than help in my research. Victor and his lovely wife, Vanessa, provided me a lot of emotional support and helped me through my lows. I could not express my gratitude to this nice couple in words. My colleagues in the Caltech Micromachining Lab, Dr. Jason Shih, Dr. PJ Chen, Wen Li, Brandon Quach, Mike Liu, Luca Giacchino, Ray Huang, Jeffrey Lin, Monty Nandra, Justin Kim, Bo Lu, Yok Satsanarukkit, Wendian Shi, and Ying-ying Wang are outstanding and smart researchers. Dr. Futoshi Iwata from the Shizuoka University, Japan, shared the office with me in his six-month stay at Caltech and introduced me the beauty of the Japanese cultures. It would be difficult for me to obtain comparable memories elsewhere to what I have got in the past five years.

I would also like to thank the Keroro team, the vanguard of the Earth Invasion Force of the 58th planet, the Keron, in the Gamma Nebula. While they are working hard (?) to take over the Earth, these five frog-like aliens, Keroro, Giroro, Tamama, and Kururu, gave me a lot of fun and

kept me company through numerous lonely nights (Er ... ..., it seemed that I forgot someone ... ...). In addition, I am indebted to the great composer, Ludwig van Beethoven. His beautiful symphonies, concertos and many other works, together with excellent pieces from Antonin Leopold Dvorak, Wolfgan Amadeus Mozart, Bedrich Smetana, Pyotr Il'yich Tchaikovsky, Johannes Brahms, Johann Sebastian Bach, Joaquin Rodrigo Vidre, etc., have shielded me from the deafening noises of the mechanical pumps in the clean room and made pleasant my work in the clean room.

Finally, I thank my candidacy committee and thesis committee, Dr. Yu-Chong Tai, Dr. Ellis Meng, Dr. Changhei Yang, Dr. Sander Weinreb, Dr. James Weiland, and Dr. Marc Bockrath for their insights and advices to my Ph.D. research.

Abstract

The implantable electronic systems have changed our life greatly and provided crucial support for people who previously could not live an independent life otherwise. However, current implantable electronic systems are based on technologies more than 50 years old and more medical problems require advanced implantable electronic systems with small form factors and multiple electrodes. This work explores and evaluates possible alternatives of implantable electronic systems.

Parylene, a widely used MEMS/CMOS process compatible material, is the cornerstone of this work. Parylene has been an ISO10933 and USP Class VI certified biocompatible material. Parylene serves as the substrate and protective coating of the implantable electronic systems developed in this work.

Thin film pentacene is studied in this work and thin film pentacene transistors are developed. The thin film pentacene transistor uses Parylene as the flexible substrate, the gate insulator and the protective coating. Studies of parylene surface are carried out. And based on this study, pentacene hole mobility is improved using spin-cast smoothing layers and top-contact configurations. To evaluate the long term reliability and stability of the thin film pentacene transistors, saline soaking tests are performed. The results are less than satisfactory.

In addition, thin film amorphous silicon is studied and thin film amorphous silicon transistors are developed. This thin-film amorphous silicon uses Parylene HT®, a Parylene variant with high temperature stability, as the flexible substrate. To evaluate the long term reliability and stability of the thin film amorphous silicon transistor, room temperature saline soaking tests and 80°C accelerated saline soaking tests are carried out. The thin film amorphous silicon

transistors show excellent stability in saline soaking. The thin film amorphous silicon transitor shows no degradations after more than 90 days in 80°C saline solution.

In summary, thin film pentacene transistors and thin film amorphous silicon transistors are developed and their performances are optimized. The long-term stability and reliability of these transistors are evaluated via saline soaking tests. While thin film pentacene transistors show only less than satisfactory results, thin film amorphous silicon transistors exhibit stable and reliable performances.

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Chapter 1

Introduction to Implantable Electronic Systems

> "He has an iron hook instead of a right hand, and he claws with it."
>
> "Claws!"
>
> "I say, John," said Peter.
>
> *J.M. Barrie, "Peter Pan: Come Away, Come Away"*

A medical prosthesis is an artificial extension that replaces a missing body part. Perhaps the most famous medical prosthesis is the shining hook of Captain Hook in *Peter Pan*. Prostheses are typically used to replace body parts lost by injury, or missing from birth or to supplement defective body parts. With the advance of technology, the medical prostheses have evolved from a simple but scary hook to a complex, computer-aided, and thought-controlled biomimetic microelectronic system.

This work is to study the bio-implantable electronic systems and is aimed at finding novel alternative technologies that address problems current state of the art leave unsolved: small form factors, flexibility and interconnects. This thesis will address the pros and cons of current approaches of bio-implants, followed by evaluations of novel alternatives based on thin-film technology. Next, both the silicon-based approach and the pentacene-based approach will be investigated in detail. The MEMS/VLSI technologies used in the fabrication of these devices and the versatile material, Parylene, will be addressed in the appendix sections.

1.1 Medical Diseases and Implantable Electronic Systems

Today, a variety of diseases can be treated with implantable electronic systems such as artificial pacemaker, cochlear implants, cortical and spinal implants. These small electronic devices have greatly shaped our society as those consumer electronics. For some of the diseases, the implantable devices are the only cures available and for others, the implantable devices can help patients resume their daily life. The need for implantable devices is urgent and great. For example, according to the American Heart Association, an estimated 80,700,000 American adults (1 in 3) have one or more types of cardiovascular diseases. The estimated direct and indirect cost of cardiovascular diseases is $448.5 billion. Among these cardiovascular diseases, artificial pacemakers and implantable cardiac defibrillators (ICD) are currently the only cures for certain types of arrhythmia (irregular heartbeat). In 2005, 91,000 implantable cardiac defibrillators procedures and 180,000 pacemaker procedures were performed in the United States.

In addition to cardiac implants, cortical and spinal implants also have great influences. According to the National Spinal Cord Injury Statistical Center (Birmingham, Alabama), the number of people in the United States who are alive in 2007 and have spinal cord injury has been estimated to be approximately 255,702 and approximately 12,000 new cases occur each year. The average health care and living expenses per year for a patient with spinal cord injury ranges from $228,556 to $775,567 for the first year and $16,018 to $138,923 for each subsequent year. Neural implants can benefit these patients. Sacral nerve stimulators now help patients with paraplegia control their bladders. The brain-computer interfaces, or cortical and spinal implants combined with external equipment like robots and motors, can help these paralyzed patient live an independent life and thus reduce their reliance on other people and save huge healthcare expenses.

These are some examples of implantable electronic systems. Other implants such as retinal implants and cochlear implants can all help patients live an independent life and save the society an astronomical amount of money on medical expenses.

Conventional implants such as pacemaker are based on technologies that are invented more than 50 years ago. The electronics of these implants are housed in hermetically-sealed metal cases (mainly titanium). Because of this metal housing, these implants have large form factors. A typical pacemaker is approximately 40 mm by 40 mm by 8 mm. They are okay for subcutaneous implantations. However, there isn't enough room at certain locations. Retinal implants resides inside the eye and the eye has only a volume of 6 mL. The spinal canal that houses the spinal cord is only 11.5 mm in diameter. Small and flexible implantable systems are required for implantations at such regions. Not only small dimensions, flexibility is also needed for these implants. A flexible implant can reduce the size of the implantation incision and thus shorten the scar healing time and in some cases, only a small area is available for surgical insertion of such implants.

In addition, multi-electrode arrays are also desirable. The maximum number of electrodes of current implantable devices is 22 of the cochlear implants. Retinal implants requires at least 64×64 electrodes and the neuroprobes for cortical implants need more than 96 electrodes.

Small dimensions, flexibility and capability of multi-electrodes are a few new features that advanced neural implants need. Others properties such as better encapsulations, low power consumption, complex logics and high computing speed are also among the features of advanced neural implants.

Not only helping patients in need, neural implants can also improve our understanding of neural sciences. With the help of cortical implants, precise distributions of electrical signals of the brain are available and these data can help us understand how the parts of the brain collaborate with one another when we think. Signals recorded with retinal electrode arrays could help us further study the process of vision creation. In short, neural implants based on neural sciences in return advance neural sciences.

1.2 The State of the Art

Today, there are a variety of implantable electronic systems in our daily life, including artificial pacemakers, cochlear implants, and neural prosthesis and retinal prosthesis. A brief summary is given about artificial pacemakers, cochlear implants, and neural prosthesis and retinal prosthesis in the following section.

1.2.1 Artificial Pacemakers

A pacemaker or artificial pacemaker, is an electronic device that regulates the beating of the heart by stimulating the heart muscles with electrical pulses through the contact electrodes placed on the heart. The primary purpose of a pacemaker is to replace the malfunctioning native pacemaker of the heart.

Modern pacemakers are versatile. Cardiologists can externally program the pacemaker to suit individual patient's need. Some pacemaker systems combine a pacemaker and implantable defibrillator in a single implantable package. Some have multiple electrodes that can stimulate different positions of the heart to improve synchronization of all the heart muscles.

As early as 1889, McWilliam reported the results of stimulation of the human heart with electrical pulses [6]. Ventricular contractions were sucessfully elicited by stimulation of electrical pulses and a stable heart rhythm of 60 – 70 beats per minute was also demonstrated. McWilliam opened the door to the development of the artificial pacemakers. In 1932, Albert Hyman invented an electro-mechanical device dubbed as "artificial pacemaker". The term, "artificial pacemakers" has come into use since.

Numerous efforts were put into development of artificial pacemakers. In 1957, Earl Bakken built the first wearable external pacemaker based on silicon transistors. This pacemaker was contained in a small plastic box and had controls that adjusted electrical signals sent out to heart. The electrical pulses were transmitted to the heart via electrode leads that penetrated the skin of the patient and terminated with the contacts attached on the surface of the heart

muscle. In 1958, a fully-implantable pacemaker was first implanted into a human body.

At that time, the main concern of the development of the pacemakers was the continuous power supply. In early days, mechanical powering systems like springs were used. Later, pacemakers were powered by the short-life mercury batteries. In the late 1960s, nuclear battery powered pacemakers were developed. Not long, nuclear batteries were replaced by the lithium ion batteries. Wilson Greatbatch developed the first pacemaker powered by the lithium-iodide battery, which became today's standard design of pacemakers.

Another concern of the pacemaker development is how to protect the implanted system from corrosion. In early days, the pacemakers are encapsulated with epoxy resins and water of the body fluid can easily permeate through the epoxy resins. Telectronics of Australia in 1964 provided a solution to this problem. They developed a pacemaker that was housed within a hermetically sealed titanium case. The pacemaker was encapsulated in epoxy with a final dip coat of a mix of epoxy and titanium dioxide. 1974, Cowdery developed pacemakers contained in a titanium cases welded with tungsten-inert gas (TIG) welding process. Laser-welding processes were also developing in late 1980s.

A typical internal pacemaker has dimensions of 42 mm by 42 mm by 8 mm and comes with a electrode measuring between 50 and 60 cm long. The system consists of a power source, usually a lithium cell, a sensing circuitry to capture natural heart beats and computer logics that controls the pacing device, output circuity delivering electrical pulses to the electrodes, and electrodes that contacts the heart muscles.

A pacemaker is typically implanted below the subcutaneous fat at the chest wall and above the muscles and bones of the chest via an incision made in the left shoulder area below the collar bone. The stimulating leads are fed into the heart through a large vein.

1.2.2 Cochlear Implants

A cochlear implant is an implantable electronic device that stimulates the hearing nerves with electrical pulses. A cochlear implant system consists of an external system and an internal

system. The external system includes a microphone, a speech processor and n transmitter. The internal system contains a receiver and stimulator and a multi-electrode array.

Going back to the eighteenth century, Alessandro Volta, the developer of batteries, reported to hear sounds after stimulation of his own ears with a 50-volt circuitry. This is probably the first record of stimulation of the audio system with electrical pulses. In the 1950s, two French doctors, Djourno and Eyries, reported direct stimulation of an acoustic nerve. In the 1970s, Graeme Clark of University of Melbourne developed multi-channel cochlear implant systems that stimulate cochlea at different positions. Successful implantations of multi-channel cochlear systems have been reported since 1978.

The cochlear implants are based on the tonotopic organization, or frequency-to-place mapping, of the basilar membrane of the inner ear. Sounds are received by the microphone and processed by the speech processor. The transmitter sends out the processed sound signals via radio frequency electromagnetic wavers. The internal receiver and stimulator receives the transmitted signals and output electrical current pulses to the cochlea via the electrode array.

The electrode array is made of a special type of silicone rubber with platinum electrodes. One end of the electrode array is connected to the receiver/stimulator while the other end is extended into the cochlea. There are twenty-two electrodes on the multi-electrode arrays. Two electrodes sit outside the cochlea and function as ground electrodes: one is the ball electrodes that is placed underneath the skin and the other is a plate on the device.

The device is surgically implanted. A small incision is cut in the skin behind the ear and a hole is drilled on the skull into the mastoid bone and the inner ear. The electrode array is inserted into the cochlea.

By now, nearly 100,000 people worldwide have received cochlear implants.

1.2.3 Cortical Implants

A cortical implant is a direct brain interface that enables a primate, through the surgically implanted devices, to control external electromechanical devices with “thoughts” only. Figure 1.1

illustrates a system of cortical implants. Cortical implant systems can directly benefit those patients with spinal cord damages, peripheral nerve disease and amyotrophic lateral sclerosis (ALS, also known as Lou Gehrig's disease). In the United States, more than two million people suffer from some forms of paralysis.

The Caltech researchers, Andersen, Tai and others, developed a direct brain interface system that use high-level cognitive signals for controlling external prosthesis equipment. This system directly records the cortex signals when the subject is thinking of something, interprets the signals and send controlling signals to the controlled equipment.

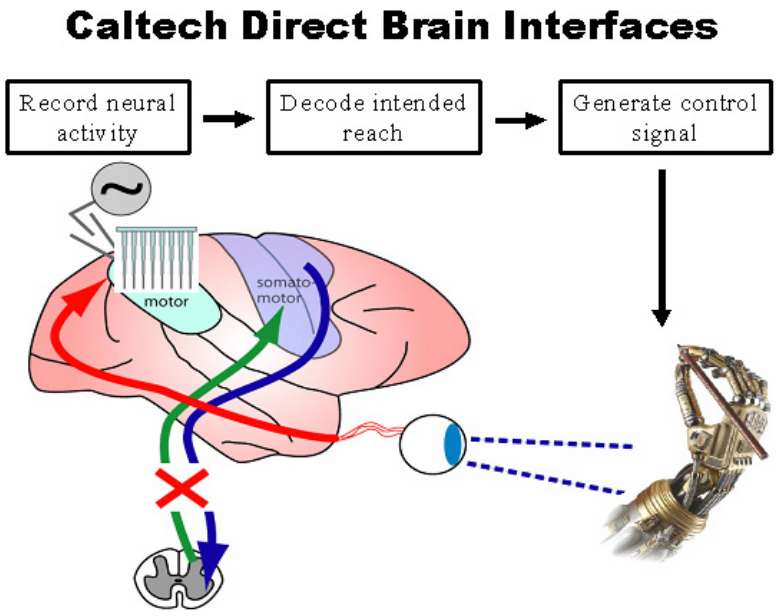


Figure 1.1: The Caltech direct brain interface. Courtesy of Dr. Changlin Pang.

Robots, computers, vehicles and other smart output devices are controlled by the signals sending out from the direct brain interface systems and complete the requested task by the subject. There are tons of cognitive signals available, including action, speech, and even emotional states and other higher cortical functions. The "expected value signals" used by the brain can also be employed by the direct brain interface system to interpret the subject's decisions and motivations. This cortical implant system can help a paralyzed patient interact with the world and facilitate his/her everyday life.

1.3 Retinal Prosthesis: A Special Problem

Among all these electronic prosthetic implantations, the retinal prosthesis is a special subject that posts additional challenges and constraints on the development of the implantable solution.

1.3.1 The Eye and Retinal Diseases

Vision occurs when the light enters the eye through the cornea and the pupil, is focused by the transparent crystalline lens, traverses the vitreous cavity of the posterior segment and finally hits the retina. At the retina, photoreceptors are activated by the incident photons and produce electrical signals that are carried to the visual cortex of the brain.

Because vision is created via a complex process signal transduction and transmission that requires the cooperation of numerous tissues and cells, the chances are high to break the process and blindness occur. Common blindness diseases includes cataracts, glaucoma, age-related macular degeneration (AMD), trachoma, cornea opacity and diabetic retinopathy. Some of these diseases result from blocking of the pathway of light to the retina, such as cataract, the disease of opacification of the lens. Some stem from loss of the retina's capability of converting light into electrical signals or some barriers to the transmission of the converted electrical signals to the visual cortex, for example optical nerve damage from glaucoma. In addition to the drug treatment and surgical operations, implantation of electronic systems can cure some blindness diseases and even restore the patient's damaged vision.

1.3.2 Electronic Implants in the Eye

A variety of electronic implants have been developed to be "placed inside the eye" so as to replace certain functions of the eye and restore patient's vision. In 1994, Humayun *et al* reported their results on stimulation of vertebrate retinas with bipolar electrical current. The conclusion was exciting and promising. They successfully elicit local retinal responses with electrical

signals on both the normal eye and the eye with outer retinal degeneration. This directed later interdisciplinary researches of medicine and MEMS to the field of ophthalmology. Later, the very same group led by Humayun demonstrated that visual responses could also be elicit by stimulating the retina with electrical signals [7].

Based on the concept of direct stimulation of retina, a complete implantation system is proposed as the treatment solution. Figure 1.2 illustrates the intraocular system of retina prothesis. In this system, an external camera captures the vision of the patient and sends the encoded signals to the intraocular system. The radio frequency coil of the intraocular system receives the data and the power. The silicon chip packaged within the system is powered by the RF coil and processes data received by the RF coil. The chip then sends out electrical signals to the corresponding electrodes via a flexible cable.

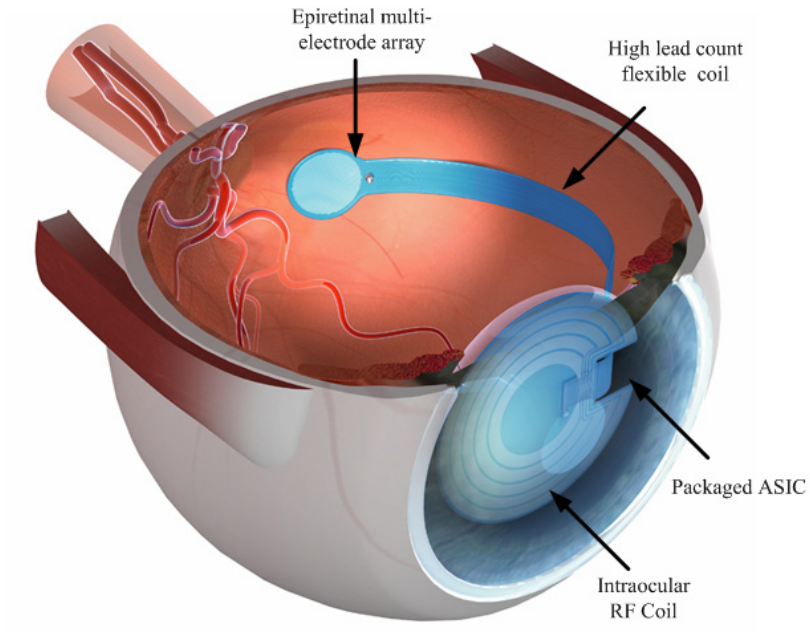


Figure 1.2: The intraocular system of retinal prothesis. Courtesy of Dr. Damien Rodger.

The silicon chip of the retina prosthetic system is a foundry-made ASIC. The chip is integrated into the retina prosthetic system via chip-level integrated interconnect (CL-I^2) technology [8]. Figure 1.3 shows a silicon chip packaged inside Parylene C along with electrode leads.

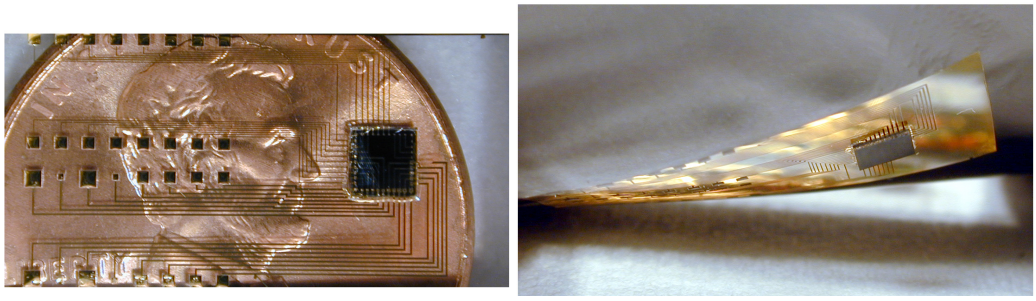


Figure 1.3: The chip-level integrated interconnect (CL-I^2) technology. Courtesy of Dr. Damien Rodger.

1.3.3 Limited Space in the Eye

This intraocular system is implanted inside the eye via surgical operations. As can been seen, the limited space in the eye places an additional contraint on the development of such intraocular systems. The dimensions of the eye vary only 1 – 2 mm among humans. The vertical diameter is 24 mm and the transverse is a little bit larger. The total volume of the eye is roughly 6.5 mL. Within such a small space, implants with huge and cumbersome metal cases are not possible. Meanwhile, the system is recommended to have a width of approximate 2 mm for the ease of surgical insertion. Eye incisions less than 2 mm long can readily self-healed without any sutures. How to protect the implant electronic systems with constraints of small dimensions is a challenge to the existing MEMS technologies.

1.4 Technology Challenges

1.4.1 Corrosive Physiological Environment

The first challenge an implantable electronic system faces is the corrosive physiological environment. The human body fluid is corrosive to silicon. Bare silicon wafers implanted on the cortical surface of adult rat brain are significantly corroded in as short as ten days [9]. The composition of the body fluids varies with the parts of the body. Take the aqueous humor and the vitreous humor for example. The aqueous humor is a thick watery substance that is between

the lens and the cornea. The aqueous humor is mainly composed of water (99%), ions (Cl^-, Na^+, K^+, Ca^{2+}, PO_4^{3-}, etc.), proteins (albumin, β-globulin), ascorbate, glucose, lactate and amino acids. The vitreous humor mainly consists of water (99%), salts, sugars, vitrosin, a network of collagen type II fibers and mucopolysaccharide hyaluronic acid. Among these compositions, water, oxygen and chloride ions are usually considered the culprits of corrosions of silicon and metal.

In addition to corrosions of the implants caused by the body fluids, the implant can elicit immune responses of the body, too. Silicon implanted on the cortical surface of the rat brain causes significantly elevated tissue and glial cell reactions [9]. Accordingly, it is mandatory that silicon be covered with some sort of protective and biocompatible coating if silicon is to be used in implantable systems.

1.4.2 Mechanical Bending And Stress Concentration

One major problem that the aforementioned devices do not address is the stress-caused damage when the devices are bent. During surgical implantation operations, the retina prosthetic devices are folded and bent to fit into the small incisions. Other implants such as spinal cord implants may be bent and under torsion after being implanted inside the subject's body. While the retina prosthetic devices based on Parylene are flexible, some points on the device may be the stress concentration points when the device is bent.

The retina prosthetic device is mainly a silicon chip encapsulated with Parylene and thus can be treated as a Parylene-silicon-Parylene sandwiched structure. This sandwiched structure can be modeled as a composite beam problem. The bending of the composite beam is can be analyzed via the following partial differential equations:

The moment-curvature relationship:

$$M = \kappa \left(2E_{Pa}I_{Pa} + E_{Si}I_{Si}\right) \ , \tag{1.1}$$

where M is the bending moment, κ is the curvature, the E_{Pa} and I_{Pa} are the Young's Modulus and moment of inertia of Parylene, and E_{Si} and I_{Si} are the Young's Modulus and moment of inertia of silicon.

The bending-moment equation:

$$\frac{\partial^2}{\partial x^2}\left\{(2E_{Pa}I_{Pa} + E_{Si}I_{Si})\frac{\partial^2 v}{\partial x^2}\right\} = -\frac{\partial^2 M}{\partial x^2}\,, \tag{1.2}$$

and the bending stress, or the flexural stress, is given by:

$$\sigma_x = -\frac{My}{I}\,. \tag{1.3}$$

As is the case of usual mechanical problems, this bending problem is too complicated and has no closed-form solutions. The computer software, COMSOL Multiphysics® is employed to solve the problem. Because of symmetry, the bending problem is modeled a composite beam with sandwiched material, which is fixed at one end and free at the other, as shown in Figure 1.5.

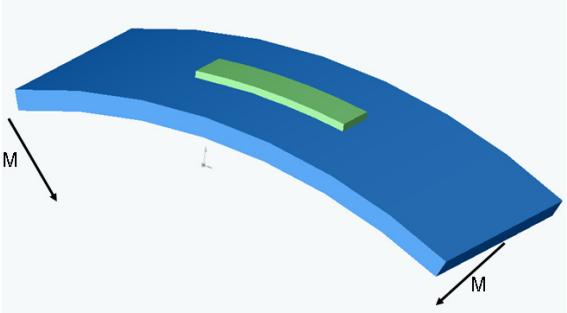


Figure 1.4: Illustration of The bending problem.

The thickness of the silicon chip ranges from 0.5 to 250 μm and it is 2.5 mm long. Both the substrate and top Parylene C are 10 μm thick. Figure 1.6 shows the stress inside the Parylene-silicon-Parylene structures. As the thickness of silicon reduces, the high stress area moves from the edge of the silicon chip to the fixed end of the beam and the high stress area switch from Parylene to silicon chip.

That is, for chip-integration technologies, the mechanical failure usually first comes from

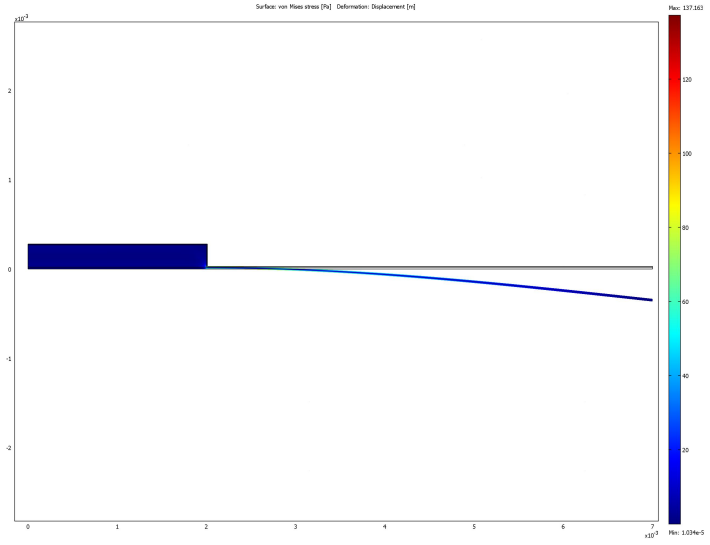
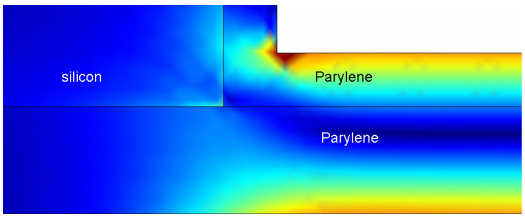
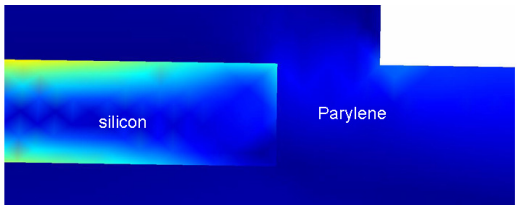


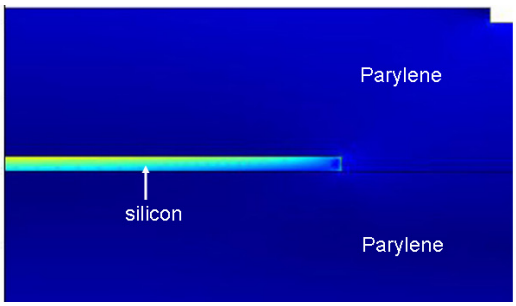
Figure 1.5: The bending problem.



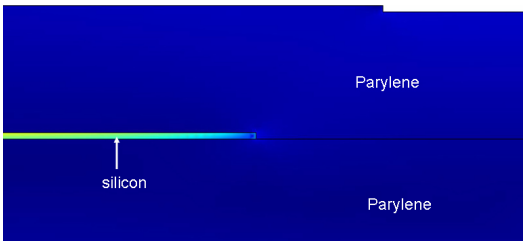
(a) 250 μm silicon



(b) 10 μm silicon



(c) 1 μm silicon

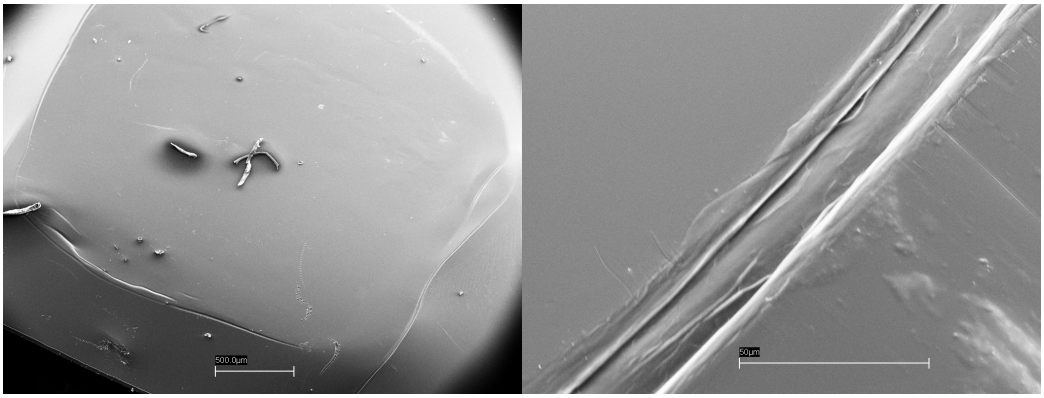


(d) 0.5 μm silicon

Figure 1.6: Stress concentrations of Parylene-silicon-Parylene structures.

the failure of Parylene while for thin-film transistor technology, it is the brittle silicon thin film that causes the mechanical failure.

A Parylene C film with a 250 μm silicon chip packaged inside is used for the mechanical bending test. After several bendings, the Parylene C film shows permanent deformation at the edges of the silicon chip. The Parylene surface shows clear cracks, as can be seen in the SEM images, Figure 1.7. Such cracks could lead to starting points of corrosion and increased water permeation. As a comparision, a blank Parylene C film, a Parylene C film with amorphous silicon transistors and a Parylene C film with pentacene transistors also undergo the same tests. Figure 1.8 shows these films after the bending test.

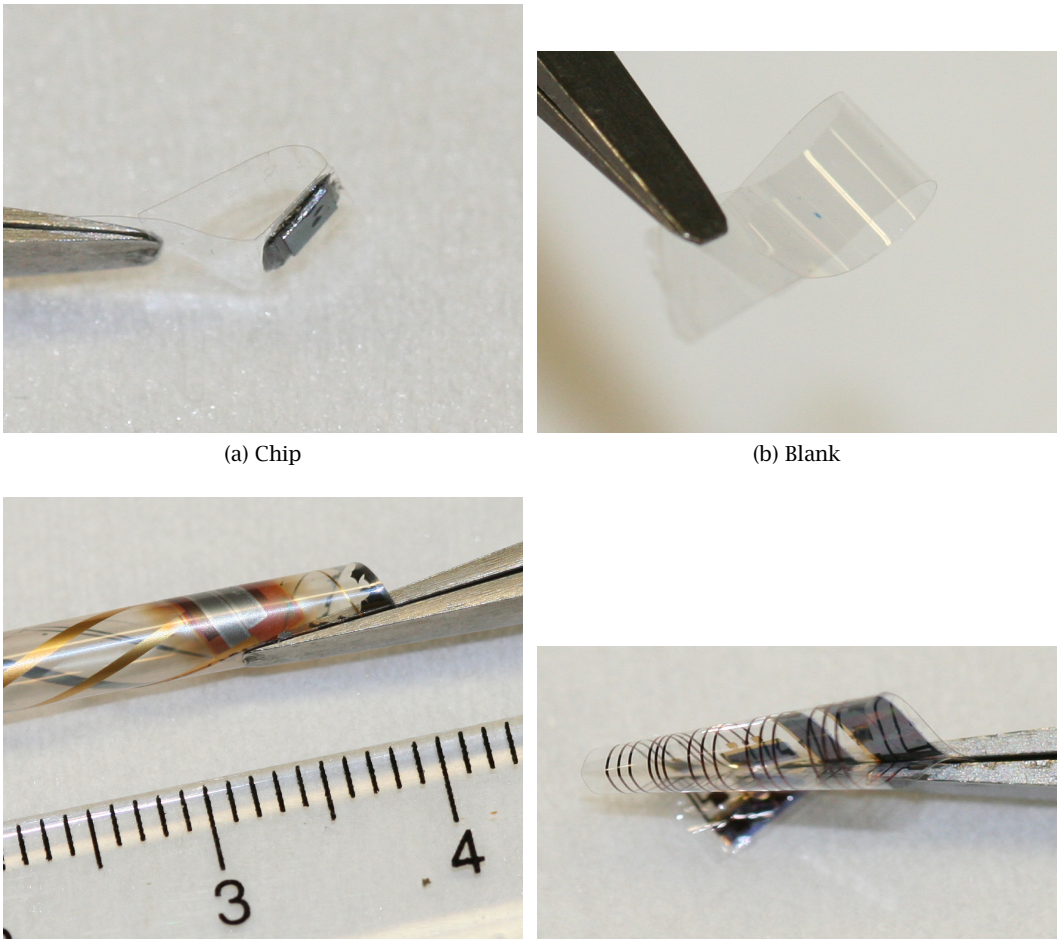


(a) The surface covering the whole chip (b) The crack

Figure 1.7: The SEM images of Parylene C film with a silicon chip inside after the mechanical bending test.

1.5 The Goal and Scope of This Study

This work is to search for and evaluate alternative approaches to bio-implantable systems. As a pioneering work, the devices presented in this work are by no means comparable to today's iPOD™ and Core 2 Duo™. However, the studies on these devices provide firm stepping stones to the future bio-implantable systems and solutions of some problems that are out of the reach of current state-of-the-art devices. Limited by existing facilities, some parts of this work only demonstrate feasibility without improvement of higher performance. But, in terms of a



(a) Chip

(b) Blank

(c) A-Si TFT

(d) Pentacene TFT

Figure 1.8: The bent Parylene C films.

pioneering work, such demonstrations provide valuable information.

Chapter 2

Thin-Film Electronics Approaches

2.1 Introduction

Although thin-film transistors seem new and novel in application of bio-implants, they are the building blocks of today's display industry. Recognized by Brody [10], Heil presented the first concept of the thin-film transistor in his 1935 British patent [11]. The first working thin-film transistor was demonstrated by Weimer [12]. His thin-film transistor is composed of micro-crystalline cadmium sulfide, CdS, as the semiconducting material, silicon oxide as the gate insulating dielectrics and gold as metal for source/drain contacts and interconnects. Since then, numerous researches on thin-film transistors have emerged. In the beginning, the target application and market of the thin-film transistor technology was the VLSI application. However, due to low mobilities and other poor device parameters and mainly the fast development of bulk silicon electronics, the thin-film transistor technology yield its place to single crystal MOSFET technology.

However, the thin-fim transistor technology revived in a new application, the display area. Brody *et al.* demonstrated the first active matrix LCD (AMLCD) based on CdSe thin-film transisotrs and the nematic liquid crystal [13].

Thin-film transistors made of various semiconducting materials, such as CdSe, Te, InSb and Ge were investigated in 1980's. However, the TFT technology did not take off until the advent of hydrogenated amorphous silicon thin-film transistors (a-Si:H TFT) and reports of

successful doping of hydrogenated amorphous silicon. Spear and Le Comber *et al.* reported successful doping of amorphous silicon with mixture of phosphine/diborane and silane [14][15] and subsequently fabricated the first a-Si:H thin-film transistors [15].

It is the commercial market of TFT LCD that spurs the development of thin-film transistors. According to iSuppli Corp., the global revenue for large-sized LCD panels, or those with diagonal dimensions of 10 inches or greater, rose up to $66 billion in 2007, up 22.2 percent from $54 billion in 2006. The rising trend will continue in the coming years. The large-sized LDC panel market will expand to 597.6 million units by 2011 and the revenue will reach $102 billion in 2011.

As is the case of other multidisciplinary researches, this research of bio-implantable electronics borrows the thin-film transistor technology from the display industry.

2.2 Design of Thin-Film Transistors

Unlike bulk transistors, thin-film transistors are built on insulating substrates such as glass, steel with insulating coating, and plastics. The structures of thin-film transistors are also different from those of bulk transistors. Figure 2.1 depicts four common structures of thin-film transistors according to the positions of the semiconductor layer, gate insulator, and source/drain electrodes. A staggered TFT has the gate and source/drain electrodes on the opposite sides of the semiconductor whereas a coplanar TFT has the gate and source/drain electrodes on the same side of the semiconductor. Both staggered TFTs and coplanar TFTs are top-gated thin-film transistors since the gates are on the top of the transistors. The other two, inverted staggered and inverted coplanar, have bottom gates. All the four structures are used in silicon thin-film transistors. In the fields of organic thin-film transistors, only inverted staggered and inverted coplanar structures are used. The inverted staggerted structure is usually referred to as “top contact” structures since the source/drain contacts are on the top of the semiconductor, while the inverted coplanar one is referred to as “bottom contact” structures.

There are ohmic contact layers between the source/drain electrodes and the semiconductor layer. The ohmic contact layers are to form ohmic contacts between the source/drain electrodes and the semiconductor and to reduce contact resistance. For silicon thin-film transistors, heavily-doped n^+ or p^+ silicon is used as the ohmic contact layers. For organic thin-film transistors, the ohmic contact layers are omitted. Instead, ohmic contact between the source/drain electrodes and the semiconductor is achieved througth proper selection of the metal type used as the soruce/drain electrodes. Generally, metals with work functions higher than 4.3 eV can form good contact with pentacene.

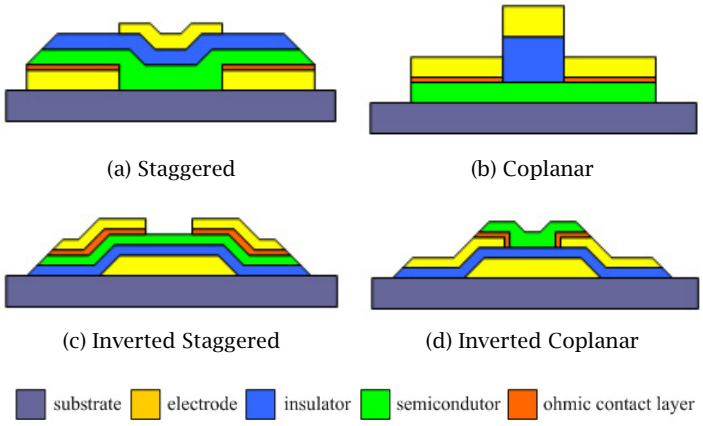


Figure 2.1: Common structures of thin-film transistors.

2.3 Thin-Film Semiconducting Materials

2.3.1 Inorganic Semiconductors

2.3.1.1 Silicon

Silicon has long been used in microelectronics. From a chip in a cell phone to a RFID in a baggage, silicon is everywhere in our daily life. However, silicon used in thin-film transistors is different from its siblings in VLSI industry.

Hydrogenated amorphous silicon (a-Si:H) is by far the most successful semiconducting ma-

terial used in applications of large-area electronics, for example flat-panel displays. In addition to amorphous silicon, silicon with other degrees of crystallinity can also be used for thin-film transistors. However, the research on semiconducting materials of thin-film transistors depends on mobility/grain sizes and process temperatures.

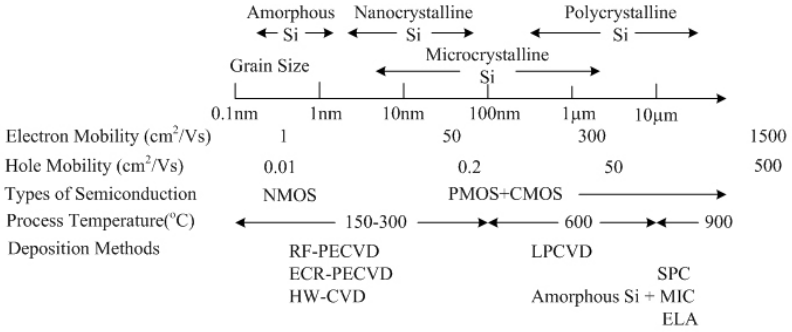
Silicon of various degrees of crystallinity can be either directly deposited on the substrates or be obtained from crystallization of amorphous silicon precursors. Generally, films of silicon are divided into four categories: amorphous silicon (a-Si), nanocrystalline silicon (nc-Si), microcrystalline silicon (μc-Si), and polycrystalline silicon (pc-Si). The mobility increases with grain sizes in general because grain boundaries are usually the sites of trapping and scattering for moving charge carriers. Figure 2.2 summarizes the mobilities, process temperatures, applications, and deposition methods of silicon with various degrees of crystallinity.

Amorphous Silicon The baseline deposition process of amorphous silicon is the radio frequency plasma-enhanced chemical vapor deposition (RF-PECVD). It is the most common deposition process to obtain amorphous silicon. The common process temperature is 250–300 °C. Typical electron field mobility of hydrogenated amorphous silicon is around 0.5 cm^2/Vs.

One of the advantages of RF-PECVD is that it is easy to lower the process temperatures from 250 – 300 °C to temperatures lower than 150 °C for flexible polymer substrates. Quality of amorphous silicon deposited at lower temperatures can be amended by increasing hydrogen content [16][17][18]. Similarly, the silicon nitride deposited with PECVD processes can also be deposited at lower temperatures with hydrogen enhancement. The source gases, such as silane, nitrogen and ammonia, are usually diluted in hydrogen for low-temperature processes. Amorphous silicon and nanocrystalline silicon deposited at lower temperature show comparable field mobility as deposited at typical temperatures [19][20][21][22].

In addition to PECVD processes, amorphous silicon can also be obtained by such low temperature processes as RF DC magnetron sputtering [23] and hot-wire chemical vapor deposition (HW-CVD) [24].

Figure 2.2: Properties of silicon with various grain sizes [1][2].



Abbreivation:
RF-PECVD: radio frequency plasma-enhanced chemical vapor deposition
ECR-PECVD: electron cyclotron resonance plasma-enhanced chemical vapor depositio
HW-CVD: hot-wire chemical vapor deposition
SPC: solid phase crystallization
MIC: metal-induced crystallization
ELA: excimer laser annealing

Nanocrystalline Silicon Nanocrystalline silicon (nc-Si) and hydrogenated amorphous silicon (a-Si:H) can be obtained by the same deposition process. A typical process temperatures of PECVD nc-Si is 250 – 300 °C. With hydrogen dilution of the source gases, the process temperature can be lowered, as is the case of amorphous silicon. Nanocrystalline silicon deposited at 150 °C by PECVD processes shows mobility of 40 cm^2/Vs [25]. Higher electron mobility up to 450 cm^2/Vs has also been demonstrated [26].

Mirocystalline and Polycrystalline Silicon Microcrystalline and polycrystalline silicon can be obtained by directly deposition or deposition of precursors followed by crystallization. Direct deposition of microcrystlline and polycrystalline silicon is usually done by low-temperature chemical vapor deposition (LPCVD). The typical processing temperature of LPCVD silicon is 600 °C. Likewise, such high process temperatures prevent fabrication of thin-film transistors on polymer substrates and glass substrates.

A popular deposition method of microcrystalline and polycrystalline silicon is the deposition of precursors followed by crystallization. The precursors are usually low-temperature amorphous silicon obtained by low-temperature PECVD processes and sputtering. The crystal-

lization process is usually done by solid-phase crystallization (SPC), metal-induced crystallization (MIC) or excimer laser annealing (ELA).

Solid phase crystallization (SPC) is a common method to obtain polycrystalline silicon from amorphous silicon. Amorphous silicon is a noncrystalline elemental solid and is considered to be at a metastable state. When amorphous silicon is annealed at high enough temeprature, the phase transformation from amorphous state to crystalline state takes place by a thermodynamic driving force. The transformation is typically carrried out with a simple furnace annealing at around 600 °C. It can also be done through a rapid-thermal annealing system at a higher temperature but shorter time. Thin-film transistors made of n-type pc-Si obtained through 650 °C annealing exhibit mobility of 64 cm^2/Vs [27]. However, the SPC annealing temperature is too high for flexible polymeric substrates.

Metal-induced crystallization (MIC) is a metal-induced transformation of amorphous silicon into crystalline silicon. Silicide, or Si-metal alloys are common materials in VLSI circuits. It is well known that the interactions between some metals, such as Al and Au, and amorphous silicon induce the crystallization of amorphous silicon at temperatures much lower than those of SPC processes. Though the kinetics of such a low temperature crystallization process has not been established, most of the experimental data show that addition of a small amount of metal impurities can dramatically enhance the crystallization of amorphous silicon at low temperatures. The reaction between a metal and amorphous silicon occurs at the interface and it lowers the crystallization temperature. Metal used as contact layers in metal/a-Si structures can be classified into two groups: silicide forming metals (Ni [28][29], Co, Cr, Pd [30], and Pt) and elemental metals that do not form silicides (Al [31][32], Ag, Au [33][34], and Sb). Thin-film transistors made of pc-Si crystallized via MIC processes show electron mobility of 121 cm^2/Vs [28].

Excimer laser annealing is to heat locally the amorphous silicon film and induce the crystallization of amorphous silicon film with pulsed excimer laser. The amorphous silicon can be deposited via low-temperature PECVD or room-temperature sputtering and later be converted

into polycrystalline silicon via laser annealing. By selectively deposit very large amounts of energy in the near-surface region of amorphous silicon in a very short time, pulsed excimer laser annealing shift the maximal process temperature from the crystallization step to other processing steps. Thin-film transistors made of polycrystalline silicon crystallized via ELA processes show electron mobility of 120 cm^2/Vs [35]. The development of excimer laser annealing permits fabrication of polycrystalline silicon thin-film transistors on low-temperature polymeric substrates such as PET and PEN [36][37].

Table 2.1 summarizes silicon materials for thin-film transistors.

Table 2.1: Properties of silicon materials for thin-film transistors [1].

Types of Silicon Films	**a-Si:H**	**nc-Si:H**	**μc-Si**
Standard deposition temperature (°C)	250	250	150-250 (precursor)
Highest process temperature (°C)	350	280	crystallization temperatures
Steps with highest process temperatures	nitride	heavily doped n, p	crystallization
Electron mobility (cm^2V^{-1} s^{-1})	0.5 – 1	40	300
Hole mobility (cm^2 V^{-1} s^{-1})	0.01	0.2	50
Conducitivity (S cm^{-1})	10^{-11}	10^{-7} – 10^{-2}	10^{-6}
Growth rate (Å s^{-1})	1 – 10	1	1 – 10
Source/drain configuration	Inverted staggered	staggered, coplanar	coplanar
Gate insulating dielectric	nitride	oxide	oxide

2.3.1.2 Other Inorganic Semiconductors

Transparent Oxides III-VI compound oxides, such as ZnO and its derivatives, provide another school of semiconducting materials for thin-film transistor applications. Such oxides are generally transparent and therefore allow unusual applications such as invisible electronics for head-up displays on windshields or cockpit enclosures. Such oxide films are usually obtained by room-temperature radio frequency magnetron sputtering and thus can be easily fabricated on flexible polymeric substrates. Thin-film transistors made of transparent ZnO exhibit electron mobility of 27 cm^2/Vs [38].

In addition to ZnO, ternary oxide derivatives of ZnO are also good semiconducting materials

for thin-film transistors. Amorphous $InGaO_3(ZnO)_5$ (a-IGZO) films with good properties can be formed on plastic substrates at room temperature [39]. The thin-film transistors with channel made of a-IGZO show electron mobility of 10 cm^2/Vs, an order higher than a-Si:H thin-film transistors and organic thin-film transistors [39].

Transparent thin-film transistors made of transparent oxides and transparent conductors, for example indium tin oxide (ITO), can be applied in a range of applications, such as backplanes for backlit LCD's and for some OLED's.

A Few Others In addition to silicon and transparent oxides, other materials, such as CdS and CdSe, are also used as the channel material of thin-film transistors. In fact, the first thin-film transistor, made by Weimer, was fabricated with a thin film of polycrystalline CdS [12]. Moreover, the first active-matrix liquid crystal display (AMLCD) had CdSe-based thin-film transistors as the pixel switch [13]. Not only on rigid substrates, CdS-based thin-film transistors has been fabricated on papers, Mylar®, Kapton® and other flexible substrates [40]. Unfortunately, the development of silicon-based electronics overturned the development of electronics based on chalcogenide compounds.

2.3.2 Organic Semiconductors

Organic semiconductors have been studied since 1940's. Recently, organic semiconductors have been used in light-emitting diodes and thin-film transistors. As is the case of inorganic semiconductors, organic semiconductors can function as either n-type or p-type materials. However, most of the organic semiconductors reported in literature are p-type organic semiconductors. Among those p-type organic semiconductors, pentacene is the most widely studied and has superior field effect mobility and environmental stability. Generally, organic semiconductors are conjugated polymer, oligomer and fused aromatics and thin films of organic semiconductors are generally prepared via either physical vapor deposition (PVD) processes or solution casting processes.

Organic semiconductor thin films can be deposited by physical vapor deposition. Heated up to the sublimation temperature, organic semiconductors are deposited in a variety of vacuum systems, such as organic molecular beam deposition (OMBD) systems, common bell-jar vacuum systems and simple glass-wall sublimation systems.

Organic semiconducting materials that can be deposited by PVD processes include: Cu-phthalocyanine [41][42][43], α-sexithiophene [44][45][46], pentacene [47] [48][49] and so on.

2.3.2.1 Pentacene

Pentacene is a polycyclic aromatic hydrocarbon consisting of 5 linearly-fused benzene rings. The extended conjugation and its crystal structures gives its semiconducting properties. However, pentacene generates excitons upon absorption of ultra-violet or visible light and makes itself sensitive to oxidation. This puts a great challenge in pentacene-based long-term applications.

Vapor-deposited pentacene-based thin-film transistors have been demonstrated with mobilities up to 3 cm^2/Vs [47], and 3–4 cm^2/Vs with surface treatments of self-assembly molecules and as high as 5 cm^2/Vs with polymeric surface treatment [50]. Field effect mobilty of 35 cm^2/Vs at room temperature was reported for purified single crystalline pentacene [51].

In addition to thin-film transistors, pentacene combined with buckminsterfullerene is used in applications of organic photovoltaic devices [52].

The solubility of organic semiconductors is the key factor for development of low-cost and large-area processing technologies, including spin-coating, inkjet printing and dip coating. But almost all small molecules are insoluble. A workaround method uses soluble precursors and later converts the precursors into the desired molecules via thermal processes. Pentacene has been fabricated in such a manner with mobilities ranging from 0.3 to 0.9 cm^2/Vs [53].

In addition, one of the major challenges for fabrication of pentacene thin-film transistors are the degradation of pentacene after exposure to organic solvents. This prevents patterning pentacene layers with conventional photolithography. Novel aqueous-based lithographical

processes to pattern pentacene films have been developed [54].

2.3.2.2 Other Organic Semiconductors

Polymers Most of the organic semiconducting polymers reported in literature are derivatives of thiophene. Because of high solubility, films of polymer organic semiconductors are often made with solution-based processes, like spin or drop casting. Although vapor-deposited organic semiconductors generally show better device performances, solution processed organic semiconductors have the potential for large-area and low-cost printing and rolling fabrication processes. Conventional photolithography and vacuum pumping systems can be eliminated with the use of soluble organic semiconductors. One of the first solution-processed organic semiconductors used in thin-film transistors is poly(3-hexylthiophene), or P3HT. The hexyl side chains may be replaced with other alkyl side chains without affecting the mobility much.

It is well known that performance of polymer thin-film transistors relies heavily on the chemical and structural order of the polymer [55]. Deposition of highly ordered polymer films depends on the regioregularity of the polymer and the molecular orientation on the substrate. The highest mobility of polymer thin-film transistors is 0.1–0.2 cm^2/Vs [56].

Other thiophene derivatives are used for thin-film transistors. Paul *et al.* fabricated thin-film transistors based on poly(9,9'-dioctyl-fluorene-co-bithiophene) (F8T2) and regioregular poly(thiophene) with ink-jet printing technologies [57].

Small Molecules In addition to pentacene, another small molecule dominates the literature of organic thin-film transistors made of small molecules: oligothiophene.

Oligothiophenes, either unsubstituted ones from terthiophene (3T) to octithiophene 8T, or substituted by alkyl chains are well studied. These oligothiophenes are most often deposited via vacuum evaporation because of their very low solubility.

Thin-film transistors made of 4T, 6T and 8T show hole mobilities ranging from 0.01 to 0.05 cm^2/Vs [58]. For substituted oligothiophenes, Halik *et al.* made α,α'-oligothiophenes thin-film

transistors with mobilities up to 0.5 cm^2/Vs [59].

Single Crystals The reports on thin-film transistors made of single crystalline organic semiconductors are rare. The major problem is the deposition of the single crystal semiconductor. Typical organic thin-film transistors are fabricated by depositing the semiconducting organics on a very flat gate insulating dielectric, either from vapor phase or by casting from a solution. Single crystal organics cannot be deposited this way. Carefully-controlled crystal growth is required for single crystal organics. Mobility of single crystal organics often suffers from the poor surface of the gate insulating dielectric. Thin-film transistors made of single crystalline sexithiophene show hole mobility of 0.075 cm^2/Vs [60].

The problem mentioned above is solved by depositing the gate insulator on top of the single crystal. By incorporating Parylene C as the gate insulator and using a top-gated paradigm, thin-film transistors based on single crystal organics have been demonstrated to have mobilities up to 8 cm^2/Vs for single crystal rubrene [61] and up to 0.3 cm^2/Vs for single crystal pentacene [62].

N-type Organic Semiconductors For inorganic semiconductor materials, the polarity is determined by doping of impurities. However, the polarity of organic semiconductors can be determined by 2 factors. The first is the ease of conduction. That is, the organic material is called n-type if its electron mobility is substantially higher than its hole mobility and p-type vice versa. In fact, in OLED area, their properties are termed with electron/hole transport. The other is charge injection. A n-type organic semiconductor is a material in which electrons are easily injected, and a p-type holes. Rather than the doping impurities, the types of organic semiconductors depends on the work functions of metal contacts and electron affinity of the organic material [63].

Little work on n-type organic semiconductors has been done. Thin-film transistors have been fabricated with derivatives of fullerene C_{60} [64], N, N'-dialkyl-3,4,9,10-perylene tetracarboxylic diimide [65] and hexadecafluorophthalocyaninato-copper (F_{16}PcCu) [66].

Among them, N, N'-dialkyl-3,4,9,10-perylene tetracarboxylic diimide has been reported to have electron mobilities up to 0.6 cm^2/Vs [65]. But N, N'-dialkyl-3,4,9,10-perylene tetracarboxylic diimide is sensitive to oxygen and water and the mobility decays fast after fabrication of the transistors.

A top-contact thin-film transistors based on N, N'-ditridecyl-3,4,9,10-perylene tetracarboxylic diimide is made with silicon dioxide as the gate insulating dielectric. The organic semiconductor film is deposited with the Denton evaporator under a pressure less than 1×10^{-6} Torr. Au is used as the source and drain contact. Figure 2.3 shows the SPM image of N, N'-ditridecyl-3,4,9,10-perylene tetracarboxylic diimide, Figure 2.4 shows the drain and gate characteristics of the thin-film transistor, and Table 2.2 summarizes the properties of this thin-film transistor.

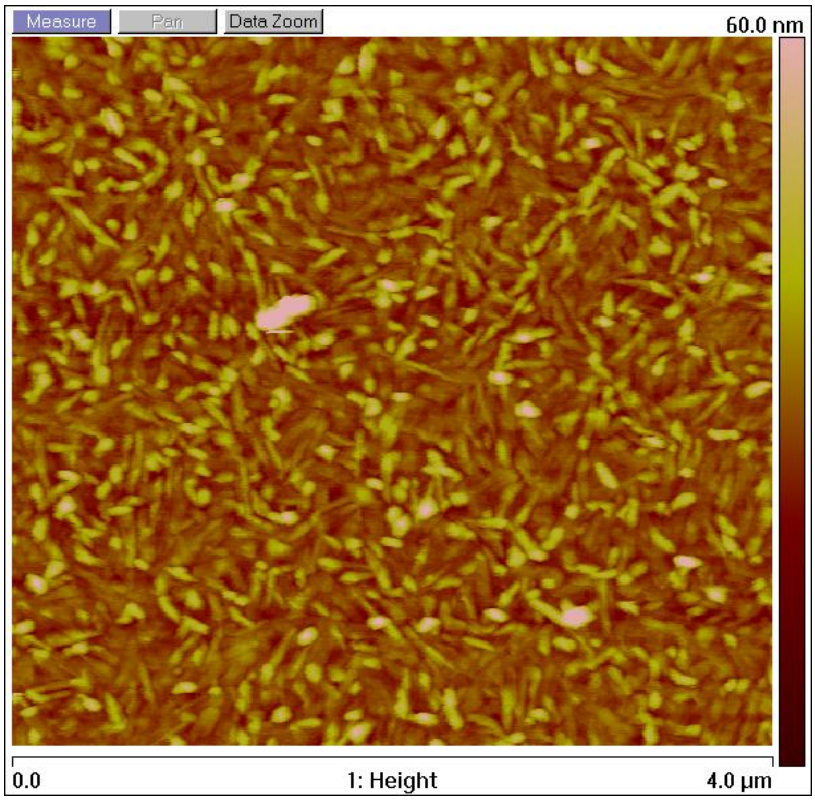
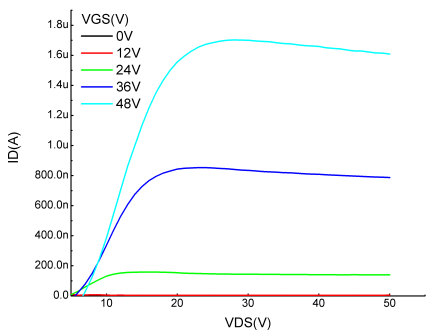
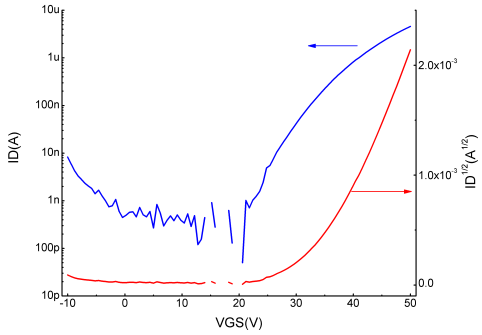


Figure 2.3: SPM image of N, N'-ditridecyl-3,4,9,10-perylene tetracarboxylic diimide.



(a) The drain characteristics



(b) The gate characteristics

Figure 2.4: The drain and gate characteristics of the thin-film transistor made of N, N'-ditridecyl-3,4,9,10-perylene tetracarboxylic diimide.

Table 2.2: Properties of the thin-film transistor made of N, N'-ditridecyl-3,4,9,10-perylene tetracarboxylic diimide.

Gate Insulator	1245Å oxide
W/L	3000/60
Source/Drain	500Å Au
Electron Mobility	0.016 cm^2/Vs
Threshold Voltage	33.38V
On/Off Ratio	10^5

2.4 Flexible Substrates

Flexible thin-film transistors are recently under much of research and industry interests, especially for applications of flexible displays. In TFT LCD display applications, a shift from glass substrates to flexible substrates is required in order to reduce the weight of the displays and produce flexible, conformal and rollable displays. Thin-film transistors have been fabricated on flexible substrates such as metal foils and polymer substrates. The deposition process of the semiconducting thin film seriously limits the choices of the flexible substrates. The most important factor of the deposition process is the maximal process temperature.

2.4.1 Metal Foils

The most common metal flexible substrate for thin-film transistors is steel foils. A widely-used and commercially available steel foil is American Iron and Steel Institute (AISI) Grade 304 stainless steel (Fe/Ni/Cr 72/18/10 wt.%). By tolerating temperatures of close to 1000 °C, steel substrates permit the adoption of many process used by the integrated circuit industry. Thus, all types of silicon thin-film transistors can be fabricated on steel foils. Polycrystalline silicon thin-film transistors have been fabricated on 200μm-thick steel substrates by Wu *et al.* with maximal process temperatures of 700 °C[67]. The achieved electron field effect mobility was 64 cm^2/Vs. Ma *et al.* fabricated amorphous silicon thin-film transistors on 3 – 200 μm steel foils with maximal process temperatures of 350 °C and achieved an electron field effect mobility of 0.6 cm^2/Vs [68]. Chen *et al.* demonstrated a flexible amorphous silicon TFT active-matrix display on 300-μm steel foil [69]. But the drawbacks of steel foils are their opaqueness and large parasitic capacitance.

2.4.2 Polymer Substrates

Although steel foils provide a solution of flexible substrates, they are relatively high-cost and opaque and not suitable for common display applications. To provide light weight and low-cost

Table 2.3: Properties of flexible substrates for thin film transistors.

Flexible Substrates	Maximum Allowable Process Temperature (°C)	Allowable Processes
Steel Foil	1000	LPCVD, PECVD, sputtering/ELA[1], organic[2]
Polyimide	400	PECVD, sputtering/ELA, organic
PEN/PET	150	Low-temperature PECVD, sputtering/ELA, organic

[1]Excimer laser annealing. [2]Spin-casting/thermal evaporation of organic semiconductors

solutions, thin-film transistors have been fabricated on polymeric substrates. Common polymeric substrates are polyimide (PI), polyethylene naphthalate (PEN) and polyethylene terephthalate (PET). One major difference between metal foils and these polymeric films is the maximal process temperatures the polymeric films can tolerate. Polyimide films, such as DuPont™ Kapton® has glass transition temperatures between 360 and 410 °C and thus are incapable of LPCVD processes. Instead, silicon-related PECVD processes are commonly applied to fabricate silicon thin-film transistors on polyimides [70]. However, polyimide films are opaque, yellow and thus have limited display-related applications. PEN and PET are both clear but with much lower temperature tolerances. DuPont™ Mylar® PET films have glass transistion temperature of 67 °C and DuPont™ Teonex® PEN films 120 °C. Silicon thin-film transistors are fabricated on these clear substrates with special low-temperatures PECVD processes [37][20] and room-temperature sputtering processes [71][72]. To no surprise, spin-cast or thermally evaporated organic semiconductors can be easily deposited onto the aforementioned polymeric substrates [73][74][49][75]. Table 2.3 lists some properties of common flexible substrates.

2.5 Parameter Extraction of Thin-film Transistors

In terms of electronic parameters such as drain current in the saturation regime or the linear regime, the thin-film transistors share the same equations with their siblings, the bulk transistors.

The threshold voltage of a thin-film transistors is given by

$$V_T = V_{FB} + 2\psi_B + \frac{2}{C_i}\sqrt{\epsilon_s q N \psi_B}\,, \tag{2.1}$$

where V_{FB} is the flat band voltage, $q\psi_B$ is the difference of the Fermi level and the intrinsic level of the semiconductor, N is the concentration of charge carriers and ϵ_s is the permittivity of the semiconductor and C_i is the capacitance of the gate insulating dielectric per unit area. C_i can usually be expressed with the expression $C_i = \epsilon_i/d$, where ϵ_i is the permittivity of the gate insulating dielectric, and d is its thickness. But in reality, C_i is measured directly due to process variations.

The drain current under a certain drain voltage, V_D and gate voltage, V_G is given by

$$I_D = \mu C_i \frac{W}{L} \times \{(V_{GS} - V_{FB} - 2\psi_B - 0.5V_{DS})V_{DS} - \frac{2}{3}\frac{\sqrt{2\epsilon_s qN}}{C_i}[(V_{DS} + 2\psi_F)^{3/2} - (2\psi_F)^{3/2}]\}\,. \tag{2.2}$$

For low drain voltages ($V_{DS} < V_{GS} - V_T$), or the linear regime, Equation 2.2 can be simplied as

$$I_D = \mu C_i \frac{W}{L}[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_D^2]\,. \tag{2.3}$$

The conductance of the transistor in the linear regime is

$$g = \frac{\partial I_D}{\partial V_{DS}} \simeq \frac{W}{L}\mu C_i (V_{GS} - V_T)\,. \tag{2.4}$$

For drain voltages, ($V_{DS} \geq V_{GS} - V_T$), or the saturation regime, the voltage across the gate insulator dielectric decreases near the drain and as a result, the channel becomes pinched off at the drain end and the current saturates. The saturation condition is given by $V_{DS,sat.} \simeq V_{GS} - V_T$. Thus, Equation 2.2 can be simplified to

$$I_{D,sat} = \frac{1}{2}\mu C_i \frac{W}{L}(V_{GS} - V_T)^2\,. \tag{2.5}$$

The transconduction in the saturation regime can be obtained by differentiating Equation 2.5 with respect to the gate voltage.

$$g_{m,sat} = \frac{\partial I_{D,sat}}{\partial V_{GS}} \simeq \frac{W}{L}\mu C_i(V_{GS} - V_T) \ . \tag{2.6}$$

In real world, it is often the case that a transistor is fabricated and we have to extract all the parameters from direct measurement results of the device. The HP4145B semiconductor parameter analyzer is often used to measure transistor characteristics. There are two kinds of transistor characteristics plots. The output characteristics plot the drain current as a function of the drain bias with gate bias as a parameter (Figure 2.4). On the other hand, the transfer characteristics plot the output drain current as a function of the input gate bias, for fixed drain bias (Figure 2.4).

To extract the carrier mobility μ and the threshold voltage V_T in the saturation region, we can plot the square root of I_D as a function of V_{GS}. By linear regression, we can get the threshold voltage from the intercept and and the mobility from the slope. By taking square root on both sides of Equation 2.5, we have

$$\sqrt{I_D} = \sqrt{\frac{C_i W}{2L}\mu}(V_{GS} - V_T) \ . \tag{2.7}$$

Solving this equation and use a definition of “k” as

$$k = \sqrt{\frac{C_i W}{2L}\mu} \tag{2.8}$$

$$\mu = \frac{2L}{WC_i}k^2 \ . \tag{2.9}$$

Equating the linear regression slope of the plot $\sqrt{I_D}$ versus V_G to “k” determines the mobility μ in the saturation regime. The threshold voltage can also be extracted from the same equation.

For short channel length MOSFETs, the threshold voltage and the mobility can be different from those in the linear regimes. But they are similar for long channel devices. For thin-film

transistors, this is not a serious problem since thin-film transistors often have long channel lengths.

2.6 Discussions

Before thin film transistors can be successfully applied in the field of the bio-implantable electronic, several issues must be investigated in detail, including flexibility, long-term reliability, biocompatibility and so on. Among all these issues, biocompatibility and long-term reliability are the most crucial. Biocompatibility ensures that the implantable devices do not elicit any detrimental effects to the human body and the long-term reliability keeps the implantable device functioning normally for a certain period of time in the physiological environment. The following chapters discuss development of thin-film transistors that are biocompatible and function reliably in the harsh physiological environment.

Chapter 3

Thin-Film Pentacene for Implantable Electronics

To develop flexible electronics for implantable applications, it is natural to look for electronics based on organic semiconductor since they are either polymers or small molecules and there is no problem bending these thin film organic semiconductors. This chapter discusses pentacene-based thin-film transistors for bio-implantable applications. The working principles behind the thin film pentacene transistors are presented and thin film pentacene transistors are developed. To have better devices performance, the process parameters, the properties of Parylene surfaces and the surface morphologies of pentacene are investigated in detail. Finally, soaking tests of thin film pentacene transistors are carried out to evaluate bio-implant reliability of thin film pentacene transistors.

3.1 Material

The bio-implantable thin film pentacene transistors have pentacene as the semiconducting material, gold-chromium as metal electrodes and interconnections, and Parylene C as the flexible substrate, the gate insulating dielectric and the top protection layer. The detailed properties of Parylene C and relevant applications are discussed in Appendix. While gold and chromium are common and well-known materials and will not be addressed here, the properties and preparation of pentacene are discussed in length.

3.1.1 Pentacene and Why It Is Selected

Pentacene is a polycyclic aromatic hydrocarbon consisting of 5 linearly-fused benzene rings. At room temperature, pentacene is in a form of purple-colored powders. Figure 3.1 illustrates the synthesis process of pentacene . The melting point of pentacene is greater than 300 °C and it sublimes at 372 – 374 °C. Because of oxidation, the color of pentacene powder slowly turns green after long exposure of air and light. Pentacene belongs to a family of linear acenes and its siblings include tetracene (four fused benzene rings) and hexacene (six fused benzene rings).

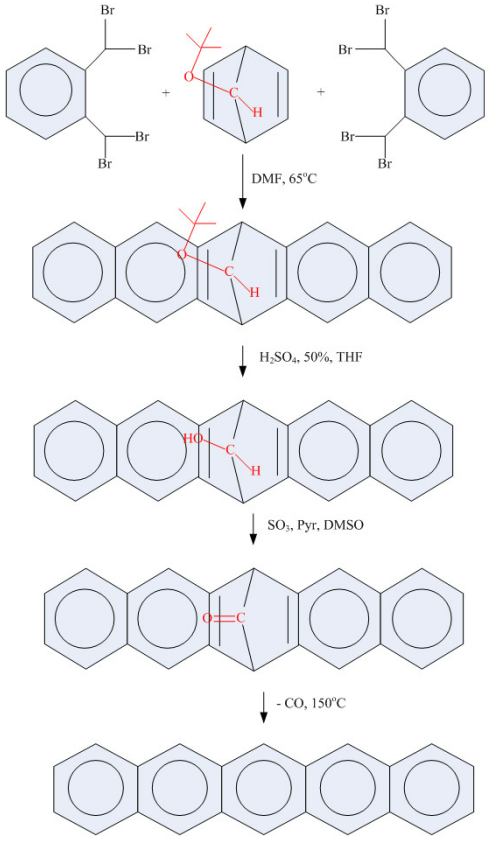


Figure 3.1: Synthesis of pentacene.

Pentacene is selected for this study because of its high mobility. Pentacene has the highest hole mobility ever reported, which is comparable to the electron mobility of amorphous silicon. In addition, the deposition of thin-film pentacene can be done by either vacuum vapor

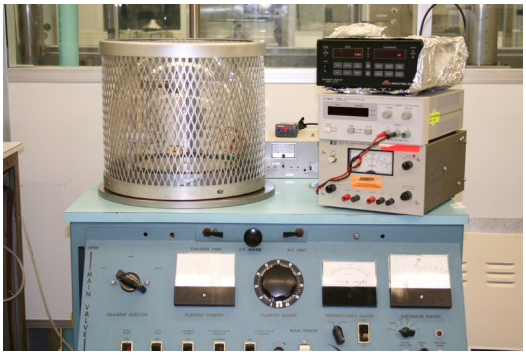
deposition or spin casting from precursor solutions followed by conversion reaction steps.

3.1.2 Deposition of Thin Film Pentacene

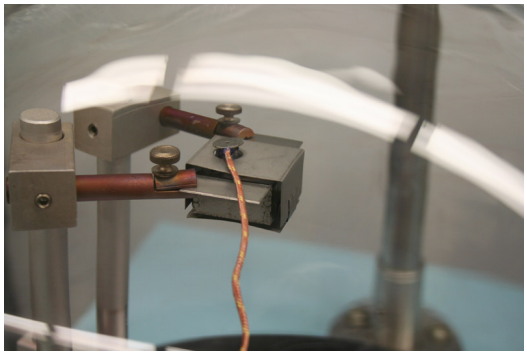
In general, thin film pentacene can be made by either depositing from vapor phase or casting from solution of precursors followed by synthesis reaction. Afzali *et al.* described a reflow method to synthesize pentacene from its precursor solution [53] and Yamada *et al.* demonstrated a photosynthesis process of pentacene from soluble precursors [76]. Casting from solution eliminates the need of sophisticated and expensive vacuum systems and thus reduces the cost of production. However, the devices made from solution casting show inferior performances to those made from vacuum deposition.

On the other hand, most of the best thin film pentacene transistors ever reported in literature were made through vacuum deposition. One of the key factors of vacuum deposition that influence device performances is the base pressure. The lower the base pressure is, the lower, the chances of oxidation are and thus the better quality of the pentacene thin film is. It ranges from less than 10^{-9} Torr of an organic molecular beam deposition system, to 10^{-7} Torr of a common high-vacuum bell jar system and up to 10^{-3} Torr of an home-made simple vacuum deposition system. In addition to direct physical vapor deposition, organic vapor phase deposition (OVPD), which consists of evaporating the molecular material into a stream of hot inert carrier gas that transports the vapors from the source to the cooled substrates where condensation of the organics occurs [77].

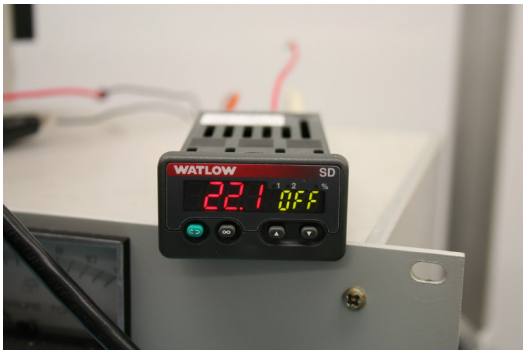
At the Caltech Micromachine Lab, pentacene thin films are deposited with the Denton evaporator (Figure 3.2). Pentacene, as purchased from Sigma-Aldrich, Inc, is loaded on a tungsten boat mounted inside the bell jar of the Denton evaporator. No purification process is carried out before deposition. The base pressure of the Denton is around 5×10^{-7} Torr. Pentacene deposition rate is maintained at 0.1 Å/s by controlling the temperature of the tungsten boat via a Watlow temperature controller. The substrate temperature is controlled in a similar way.



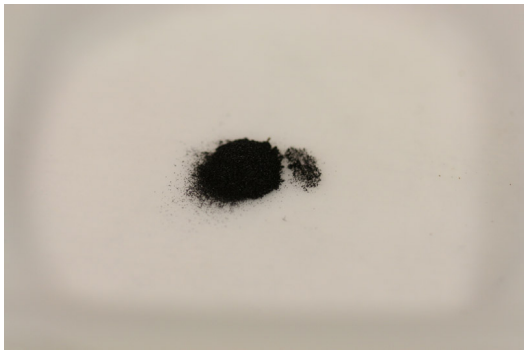
(a) The Denton evaporator



(b) The tungsten boat



(c) The Watlow controller



(d) Pentacene powder

Figure 3.2: The Denton evaporator system.

3.2 Thin-Film Pentacene Transistors in Theory

A typical thin film pentacene transistor consists of a thin semiconductor film, a insulator layer, and the gate and source/drain electrodes. Though both are dubbed as thin-film transistors, thin film pentacene transistors do not behave in the same way as amorphous silicon thin-film transistors.

3.2.1 Hole Injection into Pentacene

Figure 3.3 illustrates the band diagrams of Au and the highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO). When a positive voltage is applied on the gate electrode, negative charges builds up on the source electrodes. Because, the Fermi level of Au is far away from the LUMO level of pentacene, the electron injection into pentacene is very unlikey and thus, no current conduction occurs and the transistor is in the off state. On the other hand, when negative voltages are applied to the gate, positive charges accumulate on the source electrode and holes can be readily injected into pentacene because the Fermi level of gold is close to the HOMO level of pentacene. Thus, a conduction channel forms and charges can be driven from the source to the drain by a second bias applied between the source and the drain. Accordingly, pentacene is regarded as a p-type semiconductor. Unlike silicon, the n-type and p-type are determined by the impurity doping, the polarity of an organic semiconductor is determined by its HOMO/LUMO levels and the work function of the contact metal.

3.2.2 Thickness of Conduction Channel

The thickness of conduction channel of the thin film pentacene transistor plays an important role in understanding the thin film pentacene transistor and also determining the proper thickness of the souce/drain electrodes to reduce contact resistance.

The channel thickness can be derived from the total charge stored in a metal-insulator-semiconductor (MIS, or MOS) capacitors.

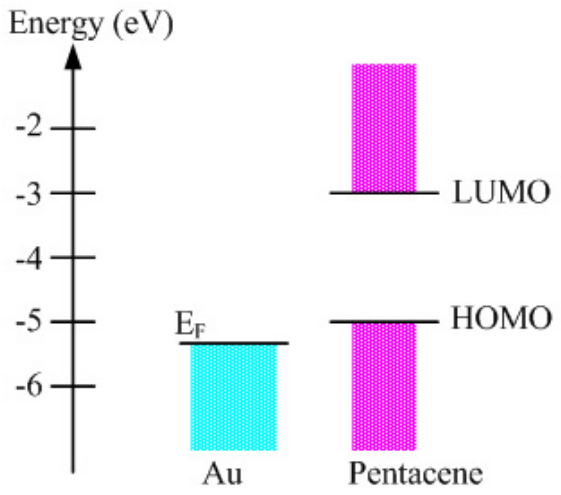


Figure 3.3: The band diagram of petacene and Au.

The derivation starts from the one-dimension Poisson equation:

$$\frac{\partial^2 \psi}{\partial x^2} = -\frac{\rho(x)}{\epsilon_s}, \tag{3.1}$$

where ψ is the potential at the position of distance x, normal to the insulator-semiconductor interface and $\rho(x)$ is the charge density and ϵ_s is the permittivity of the semiconductor.

The charge density at the point x can be expressed in terms of the surface charge density at the insulator-semiconductor interface ($x = 0$):

$$\rho(x) = qn_0 \cdot e^{\frac{q(\psi-\psi_0)}{kT}}, \tag{3.2}$$

where ψ_0 is the potential and qn_0 is charge density the at the insulator-semiconductor interface ($x = 0$)

Combining Equation 3.1 and Equation 3.2 gives:

$$\frac{\partial^2 \psi}{\partial x^2} = -\frac{qn_0}{\epsilon_s} \cdot e^{\frac{q(\psi-\psi_0)}{kT}}. \tag{3.3}$$

Integrating both sides of Equation 3.3 with respect to ψ gives:

$$E^2 = \frac{2kTn_0}{\epsilon_s} \cdot e^{\frac{q(\psi-\psi_0)}{kT}} , \tag{3.4}$$

where $E \equiv -\frac{\partial\psi}{\partial x}$, the electric field.

Then, the electric field, E, is given by:

$$E = -\frac{\partial\psi}{\partial x} = \sqrt{\frac{2kTn_0}{\epsilon_s}} \cdot e^{\frac{q(\psi-\psi_0)}{2kT}} . \tag{3.5}$$

Simplifying and integrating the above equation gives:

$$e^{\frac{q(\psi-\psi_0)}{kT}} = \left(1 + q\sqrt{\frac{n_0}{2\epsilon_s kT}}x\right)^{-2} = \left(1 + \frac{x}{\sqrt{2}L_D}\right)^{-2} , \tag{3.6}$$

where L_D is the debye length defined by:

$$L_D = \frac{1}{q}\sqrt{\frac{2\epsilon_s kT}{n_0}} . \tag{3.7}$$

By substituting Equation 3.6 back in Equation 3.2, the charge distribution is defined by:

$$\rho(x) = qn_0 \left(1 + \frac{x}{\sqrt{2}L_D}\right)^{-2} . \tag{3.8}$$

The total charge stored in the MIS capacitor under a gate bias V_G is $C_i(V_G - \psi_s) \simeq C_i V_G$ and is equal to the integration of Equation 3.8 with respect to x, from $x = 0$ to $x = \infty$.

By equating the above two values, the Debye length and the charge distribution are obtained as functions of the gate voltage:

$$L_D = \frac{\sqrt{2}kT\epsilon_s}{qC_i V_G} \tag{3.9}$$

$$\rho(x) = \frac{(C_i V_G)^2}{2kT\epsilon_s} \left(1 + \frac{x}{\sqrt{2}L_D}\right)^{-2} . \tag{3.10}$$

The conduction channel thickness can be defined as the layer of uniform charge density

of n_0 and the total charges of that layer equal the total charge stored in the MIS capacitor. By this definition, the conduction channel thickness is $\sqrt{2}L_D$. For a typical thin film pentacene transistor, the conduction channel thickness is approximately 15 Å. The monolayer of petacene molecules is 15 – 30 Å thick. Thus, it is considered that all the charge of the conduction layer lies in the first monolayer of the pentacene film.

3.2.3 Contact Resistance

The circuit model used in extraction of transistor parameters described in § 2.5 does not consider the contact resistance between the semiconductor and the source/drain contact. A circuit model incorporating contact resistance is depicted in Figure 3.4.

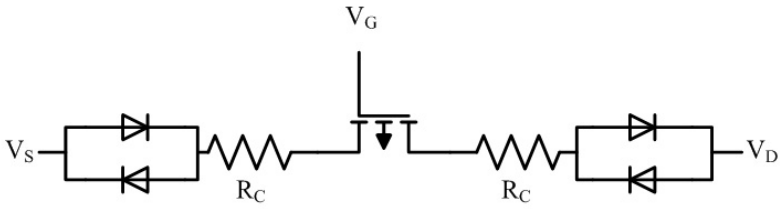


Figure 3.4: The circuit model of thin-film transistors with contact resistances. The diodes are included to account for nonlinearity of the contact resistance.

The contact resistance comes from the pentacene-Au interfaces. Kahn *et al.* did a study on orgainc-metal interfaces [3]. Figure 3.5 shows the band diagram of the pentacene-Au interface. Different from general cases of silicon semiconductors, the interface between pentacene and Au has interface-dipoles. The large difference between the vacuum levels of the two material, 1.05 eV, creates an interface dipole and makes the common Shottky-Mott model useless. The interface dipole introduces additional barrier height and makes the contact resistance larger than common metal-semiconductor interfaces. This 1.05 eV interface dipole barrier is measured from the device that has pentacene deposited atop Au. Kahn *et al.* also reported that the interface dipole barrier is reduced from 1.05 eV to 0.3 eV when Au is deposited on top of pentacene, i.e. the top-contact structure (see Figure 3.12). This explains why thin film pentacene

transistors with top contacts show better performance than those with bottom contacts (see Figure 3.12).

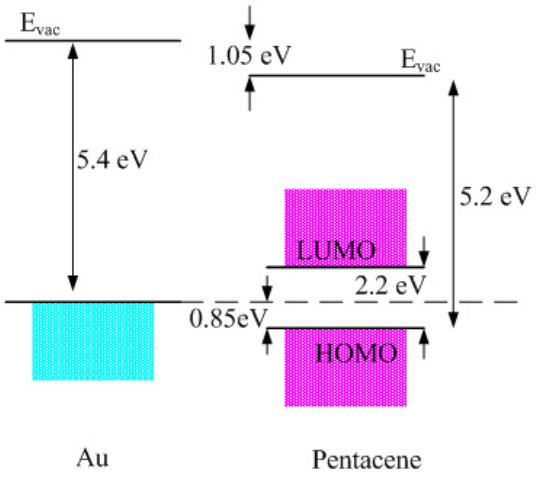


Figure 3.5: The band diagram of the pentacene-Au interface [3].

To include the contact resistance, the drain voltage, V_{DS}, used in § 2.5 has to be replaced with $(V_{DS} - I_D R_C)$ and the drain current in the saturation region becomes:

$$I_D = \mu C_i \frac{W}{L}(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} - \left((V_{GS} - V_T)I_D R_C - \frac{(I_D R_C)^2}{2}\right) . \tag{3.11}$$

However, with common testing equipment, for example, HP4145B, the contact resistance cannot be extracted. Instead, a technique that gives independent access to the channel resistance and contact resistance is needed for further analysis of contact resistance (see [78]).

For simplicity, parameters of pentacene transistors are all extracted with the circuit model without contact resistance (see § 2.5) and therefore, devices with top-contact structures will show higher mobilities than those with bottom-contact structures since the devices with top-contact structures have smaller contact resistance and thus larger on current than those with bottom-contact structures under the same bias voltages.

3.2.4 Mobility and Grain Sizes

Vacuum deposited pentacene films have polycrystalline structures. As a matter of course, the field effect mobility of thin film pentacene transistor correlates with the average sizes of the grains, since the grain boundaries are often the sites of scattering and trapping and thus slows down the holes moving inside the pentacene film. A simple way to calculate the effective mobility is to treat the film as grains and grain boundaries connected in series like the case of resistors in series [4].

The channel resistance is a series of grain resistance and grain boundary resistance:

$$\begin{aligned} R_{ch} &= \frac{L}{W\mu_{eff}Q_{inv}} = n(R_G + R_{GB}) \\ &= n\left(\frac{L_G}{W\mu_G Q_{inv}} + \frac{L_{GB}}{W\mu_{GB}Q_{GB}}\right), \end{aligned} \tag{3.12}$$

where

W	the channel width;
L	the channel length;
n	the number of grains inside the channel;
L_G	the average length of the grains;
L_{GB}	the average length of the grain boundaries;
μ_{eff}	the effective mobility;
μ_G	the mobility inside the grain;
μ_{GB}	the mobility inside the grain boundary;
Q_{inv}	the charge density of the inversion layer;
Q_{GB}	the charge density in the grain boundary.

And

$$L = n\,(L_G + L_{GB}) \tag{3.13}$$

$$Q_{GB} = Q_{inv} \cdot e^{-qV_b/kT} \tag{3.14}$$

if the barrier height of the grain boundary is qV_b.

Figure 3.6 illustrates the band diagram of polycrystalline material.

Then, the effective mobility of the polycrystalline pentacene film, μ_{eff} is given by:

$$\frac{L_G + L_{GB}}{\mu_{eff}} = \frac{L_G}{\mu_G} + \frac{L_{GB}}{\mu_{GB} \cdot e^{-\frac{qV_b}{kT}}} . \tag{3.15}$$

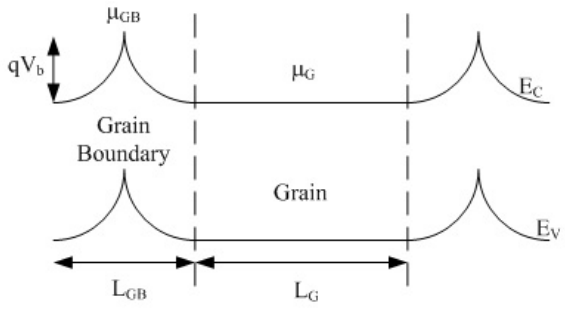


Figure 3.6: Illustration of the band diagram of polycrystalline material [4] .

Rewriting the above equation gives:

$$\frac{\mu_{eff}}{\mu_G} = \frac{L_G + L_{GB}}{L_G + L_{GB}\frac{\mu_G}{\mu_{GB} \cdot e^{-\frac{qV_b}{kT}}}} . \tag{3.16}$$

A plot of $\frac{\mu_{eff}}{\mu_G}$ as a function of L_G is given as an example in Figure 3.7 assuming $L_{GB} = 0.01$ μm and $\frac{\mu_G}{\mu_{GB} \cdot e^{-\frac{qV_b}{kT}}} = 100$ (arbitrary numbers, but close to real values). As can be seen, the effective mobility increases with grain sizes and saturates after the grain size reaches certain values. This leads to a series of experiments discussed in later sections.

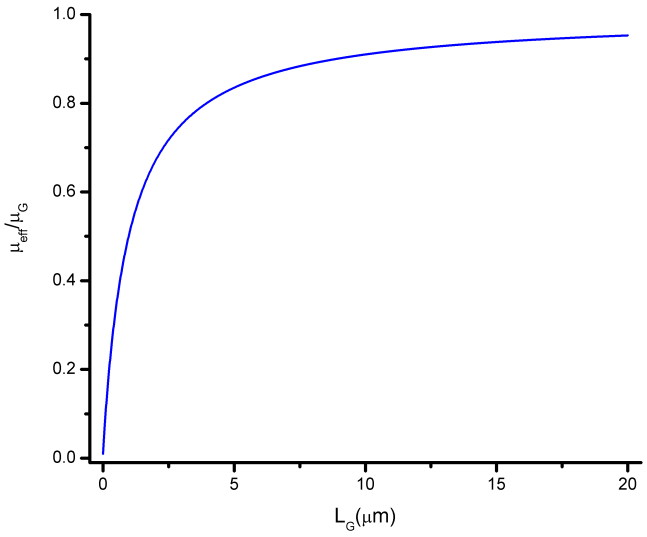


Figure 3.7: μ_{eff}/μ_G versus L_G.

3.3 In-House Thin-Film Pentacene Transistors

3.3.1 The Design

The thin film pentacene transistor takes an inverted-staggered structure, or bottom-gate bottom-contact structure, as shown in Figure 3.8. The substrate, the gate insulating dielectric and the top protection cover are made of Parylene C. The gate,and source/drain contacts are gold/adhesion metal dual layers.

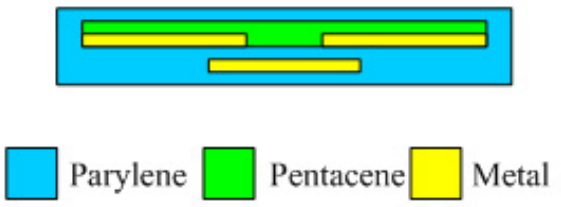


Figure 3.8: Illustration of the in-house design.

The channel length of the thin film pentacene transistor is defined by the gap between the source and the drain contacts due to the inverted-staggered configuration and the width of the

transistor is defined by the dimension of the source and drain contacts. The channel lengh, L, of the transistor is 20 μm, and the width of the transistor is 1000 – 4000 μm. The gate is 40 μm wide and 1500 – 4500 μm long. The overlap between the source/drain and the gate is 10 μm and thus makes the channel length of the transistor 20 μm. The gate and interconnects are 2000 Å gold with 200 Å chromium or titanium as the adhesion layer while the source and drain contacts are 500 Å Au only. The gate insulating dielectric is 1500 Å Parylene C.

3.3.2 The Fabrication Processes

The in-house fabrication process is to fabricate Parylene C encapsulated thin film pentacene transistors. The devices made by the in-house processes are used to compare with other devices made by modified or tuned processes. The in-house fabrication process is diagramed in Figure 3.9 and can be broken into 9 steps as follows:

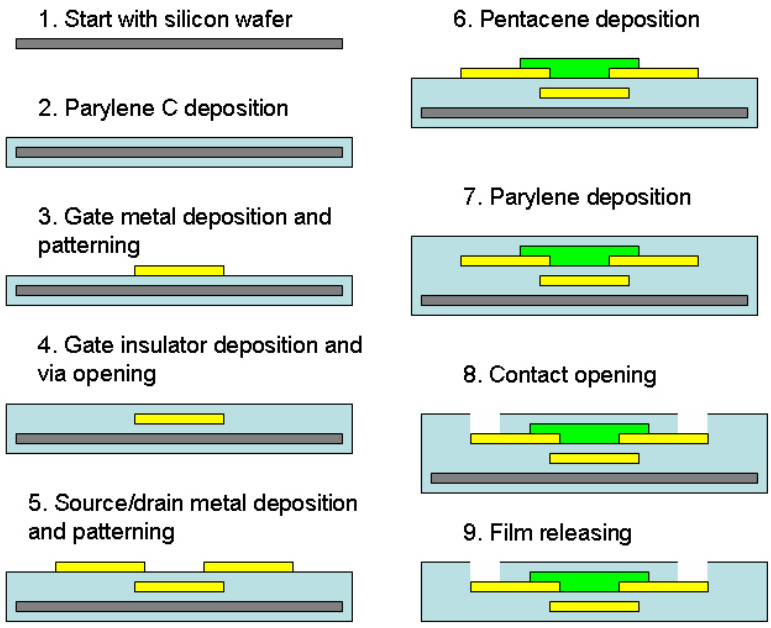


Figure 3.9: The illustrated process flow of the in-house thin film pentacene transistor.

1. Wafter Cleaning: The in-house fabrication process starts with cleaning a silicon wafer. The wafer is rinsed with DI water and purged dry with nitrogen. The native silicon oxide

on the wafer is intentionally retained. This native silicon oxide helps later releasing the thin film pentacene transistor from the wafer.

2. Parylene Deposition: a 10 μm Parylene C is deposited on the wafer. It costs around 15 g of Parylene C dimmers to deposit 10 μm Parylene with the SCS PDS Coater 2010. Detailed Parylene deposition processes are discussed in Appendix.

3. Gate Metal Deposition and Patterning: Before metal deposition, the Parylene surface is cleaned by dipping in diluted HF solution (1:10, DI water: 48% HF) for 30 seconds. This dipping removes particles and hydroxyl groups on Parylene and thus improves adhesion between Parylene and metal. A 2000/200 Å Au/Cr layer is deposited via thermal or e-beam evaporation. The Cr is used to improve adhesion between the Au and the Parylene surface. Metal patterning is achieved via wet etching processes. A 2 μm AZ1518 photoresist is spun on to the wafer and baked at 100 °C for 30 minutes. This layer of photoresist is then exposed and developed. After developing, a descum process is done by short exposure in oxygen plasma. Afterwards, the wafer is hard-baked at 120 °C for 30 minutes. The Au is etched with Transene Au Etch Type TFA and the Cr is etched with Cyantek CR-7. After etching, the photoresist is dissolved with ATMI ST-22 photoresist stripper. Next, the wafer is rinsed with ATMI PSR post-solvent rinse and DI water.

4. Gate Insulating Dielectric Deposition: Before deposition, the wafer is dipped in diluted HF solution (1:10, DI water: 48% HF) for 30 seconds. According to our previous experiences, this dipping improves adhesion between two Parylene layers. A 1500 Å Parylene C is deposited onto the wafer. The required dimmer weight is approximately 0.2 g. Detailed Parylene deposition processes are discussed in Appendix.

5. Via 1 Opening: After deposition of the gate insulating Parylene, contacts and interconnect of on the gate metal layer are opened with photolithography and plasma etching. A 2 μm AZ1518 photoresist is spun on to the wafer and baked at 100°C for 30 minutes. This layer of photoresist is then exposed and developed. Next, the gate insulating Parylene

is etched with oxygen plasma and thus the contacts and interconnects on the gate metal layer are opened. After etching, the photoresist is dissolved with ATMI ST-22 photoresist stripper. Next, the wafer is rinsed with ATMI PSR post-solvent rinse and DI water.

6. Source/Drain Metal Deposition and Patterning: Before metal deposition, the Parylene surface is cleaned by dipping in diluted HF solution (1:10, DI water: 48% HF) for 30 seconds. A 300 Å thin Au layer is deposited via thermal or e-beam evaporation. A 2 μm AZ1518 photoresist is spun on to the wafer and baked at 100 °C for 30 minutes. This layer of photoresist is then exposed and developed. After developing, a descum process is done by short exposure in oxygen plasma. Afterwards, the wafer is hard-baked at 120 °C for 30 minutes. The Au is etched with Transene Au Etch Type TFA. After etching, the photoresist is dissolved with ATMI ST-22 photoresist stripper. Next, the wafer is rinsed with ATMI PSR post-solvent rinse and DI water. The reason a thin pure Au layer without adhesion metal like Cr is used as source/drain contact is discussed in detail in § 3.4.3.2

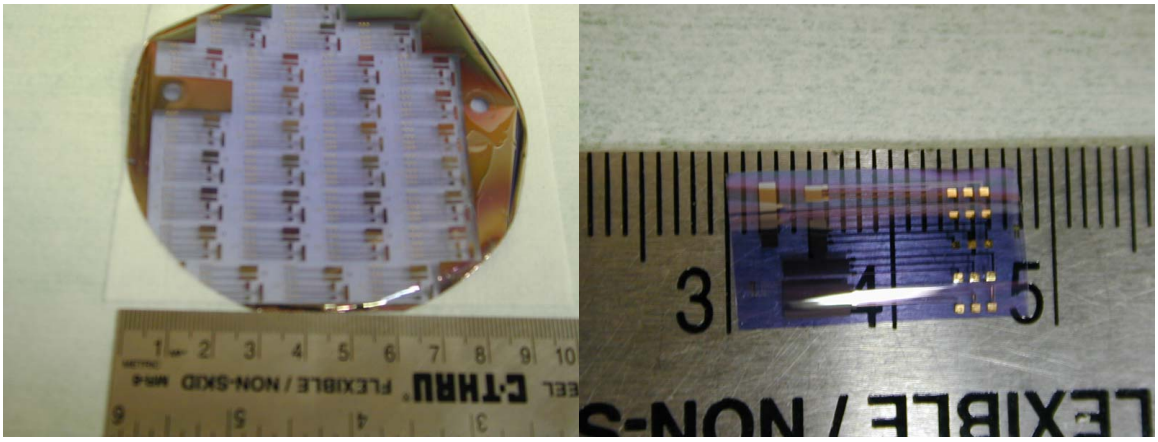
7. Pentacene Deposition: Before pentacene deposition, the wafer is dipped in diluted HF solution (1:10, DI water: 48% HF) for 30 seconds to clean the surfaces and convert the surfaces to hydrophobic ones. Pentacene, as purchased from Sigma-Aldrich, is thermally evaporated under 1×10^{-6} Torr using Denton Evaporator. The deposition rate is controlled at 1 Å/sec. The total thickness of pentacene is around 300 Å. Detailed pentacene deposition processes are discussed in § 3.1.2

8. Top Parylene Cover Deposition and Contact Opening: After pentacene deposition, a 1 μm Parylene is deposited on the wafer. Afterwards, a 3 μm AZ1518 photoresist is spun on to the wafer and baked at 100 °C for 30 minutes. This layer of photoresist is then exposed and developed. Next, the gate insulating Parylene is etched with oxygen plasma and thus the contacts and interconnects on the gate metal layer are opened. After etching, the photoresist is dissolved with ATMI ST-22 photoresist stripper. Next, the wafer is rinsed with ATMI PSR post-solvent rinse and DI water.

9. Transistor Film Releasing: Upon completion of all the process steps, the transistor film is released by cutting the Parylene film on the edge of the wafer and slowly lifting the film in DI water. Since there is native silicon dioxide in between Parylene and the silicon wafer, the adhesion of the Parylene film is good enough to sustain fabrication processes but not too strong to release the film. This method is much simpler and saves more time than traditional methods using photoresist sacrificial layers.

3.3.3 Characterization of the In-House Thin Film Pentacene Transistor

Figure 3.10 shows the pentacene transistors made by the in-house fabrication process described in § 3.3.2.

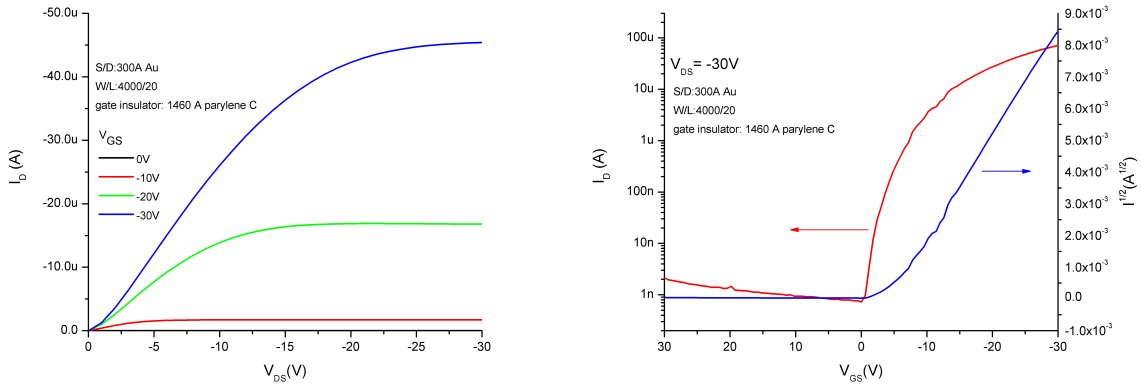


(a) The transistor film lifted from the wafer (b) A manually-cut film

Figure 3.10: The thin film pentacene transitor film.

The drain and gate characteristics are measured with a probe station and the HP4145B semiconductor parameter analyzer. The transistors are measured at room temperature. Figure 3.11 shows the drain characteristics and the gate characteristics of this thin film pentacene transistors. This thin film pentacene transistor has 1460Å Parylene C, measured with Tencor P15 surface profilometer, as the gate insulating dielectric and W/L = 4000 μm/20 μm.

The mobility of charge carriers, or holes, μ, and the threshold voltage in the saturation regime are extracted with the method mentioned in § 2.5.



(a) Drain Characteristics

(b) Gate Characteristics

Figure 3.11: Drain and gate characteristics of the thin film pentacene transistors.

The fabricated pentacene transistors shows a maximal mobilities of 0.0587 cm^2/Vs with an on-off ratio of 5×10^4. The threshold voltage is -4.556 V.

3.4 Improvements on Hole Mobility

The in-house devices with a hole mobility of 0.0587 cm^2/Vs leaves a lot of room for improvement. The following sections discuss the important factors affecting performances of pentacene transistors and how to improve them.

3.4.1 The Simplified Transistors for Process Tuning and Property Investigation

Generally, a device of the in-house design takes three weeks of processing time. In order to fabricate a lot of devices for process development and comparisons of properties, the simplified transistor design is proposed. Figure 3.12 depicts four types of simplified transistor designs. The first is the device using silicon as the gate and thermally grown oxide as the gate insulator. Depending on the top/bottom contact configurations, source/drain metals are deposited and patterned after/before pentacene deposition. These two designs are useful for calibration of

the pentacene deposition process. The other two using oxide wafers as the substrates. The gate metal is deposited and patterned on the oxide wafer. Polymer gate insulator is deposited atop the gate metal. The source and drain are deposited and patterned before or after pentacene deposition depending on the designs. These designs are useful for testing of polymer gate insulators.

As will be discussed in later sections, the source and drain electrodes of the devices using top contact configurations have to be patterned via shadow masks since no photolithography can be done after pentacene deposition.

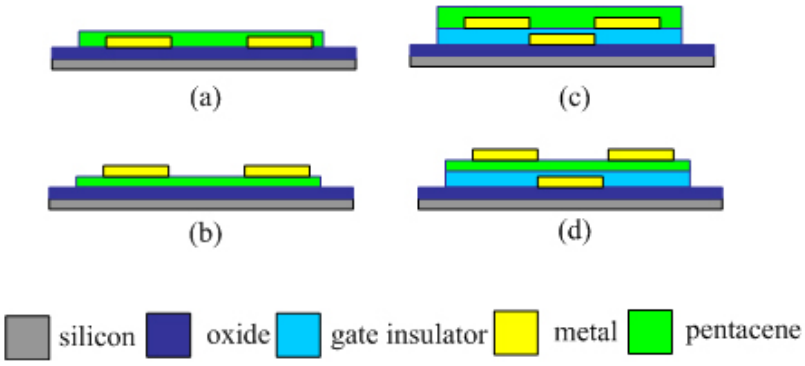


Figure 3.12: Illustration of the simplified transistor design. (a) silicon gate + silicon oxide gate insulator + bottom contact. (b) silicon gate + silicon oxide gate insulator + top contact. (c) metal gate + polymer gate insulator + bottom contact. (d) metal gate + polymer gate insulator + top contact.

While the in-house process described in § 3.3.2 takes a long time to complete and the devices made via the in-house process use bottom-contact configurations, it takes shorter time to fabricate the simplified transistors. This simplified fabrication process is described below.

1. Wafter Cleaning: The simplifed process starts with cleaning a wafer. The wafer could be either an oxide wafer or a glass wafer. The wafer is rinsed with DI water and purged dry with nitrogen. Piranha cleaning is carried out and followed by a 30-second dip in diluted HF.

2. Gate Metal Deposition and Patterning: A 2000/200Å Au/Cr layer is deposited via thermal or e-beam evaporation. The Cr is used to improve adhesion between the Au and the

Parylene surface. Metal patterning is achieved via wet etching processes. A $2\mu m$ AZ1518 photoresist is spun on to the wafer and baked at 100°C for 30 minutes. This layer of photoresist is then exposed and developed. After developing, a descum process is done by short exposure in oxygen plasma. Afterwards, the wafer is hard-baked at 120°C for 30 minutes. The Au is etched with Transene Au Etch Type TFA and the Cr is etched with Cyantek CR-7. After etching, the photoresist is dissolved with ATMI ST-22 photoresist stripper. Next, the wafer is rinsed with ATMI PSR post-solvent rinse and DI water. Depending on the actual devices, the silicon wafer itself can sometimes serve as the gate and this step can be omitted.

3. Deposition of Gate Insulating Dielectrics: The gate insulating dielectrics can be deposited via CVD processes (Parylene C and nitride), spin-coating (PMMA, PVP, and SU8-2) or thermal oxidation (Oxide).

4. Source/Drain Metal Deposition and Patterning: Before metal deposition, the gate insulator surface is cleaned by dipping in diluted HF solution (1:10, DI water: 48% HF) for 30 seconds. A 300 Å Au layer is deposited via thermal or e-beam evaporation. The patterning can be done by a mechanical mask during metal evaporation or conventional photolithography as described in § 3.3.2. The detailed discussion about the mechanical masks can be found in § 3.4.7.1.

5. Pentacene Deposition: Same as the step described in § 3.3.2. This deposition step will be carried out before the step of Source/Drain Metal Deposition and Patterning for top-contact devices and after that step for bottom-contact devices.

Depending on the actual needs, encapsulation of Parylene C is optional and the releasing step is omitted in the simplifed process.

3.4.2 Evaporation Process Parameters

Mobility of pentacene transistors depends on the quality of pentacene films and the quality of the vacuum deposited pentacene films depends on the rate of the deposition, the base pressure of the vacuum system and the substrate temperatures(see § 3.1.2).

The Denton evaporator is a more than 30 years old machine and needs some rejuvenation before it can deliver pentacene films of good quality. After long hours of services including replacing all O-rings and pipes/tubes, changing oils of the diffusion pump and the mechanical pump, and installing vacuum feedthroughs and the thickness monitor, the Denton evaporator can now give a base pressure in the range of 10^{-7} Torr.

As mentioned before, the deposition rate of pentacene is controlled by controlling the temperature of the evaporation boat. After numerous trials, it is found that deposition rate of pentacene can be maintained at 0.1 Å/s when the boat temperature is controlled at 205 – 210°C.

The substrate temperatures are controlled in similar ways and effects of substrate temperatures are discussed in § 3.4.4.1. Table 3.4 summarizes the effects of substrate temperatures.

3.4.3 Reduction of Contact Resistance

The aforementioned thin film pentacene transistors take bottom-contact configuration. Compared to top-contact configuration, a bottom-contact thin film pentacene transistor shows inferior performance. However, it is because of the relatively easy fabrication process that a thin film pentacene transistor of bottom-contact configuration is fabricated here. It is usually due to high contact resistance between source/drain metal and pentacene. Therefore, to improve device performance of thin film pentacene transistors with bottom-contact, it is important to reduce the contact resistance between the source/drain metal and pentacene.

3.4.3.1 Sizes of Source/Drain Contacts

To avoid device deficiency caused by large contact resistance and Schottky barriers between the source/drain metal and the organic semiconductor, large-area source/drain contacts are exploited. To test effects of source/drain contact area, transistors with different source/drain geometry are fabricated and mobilities are measured.

Table 3.1 shows the field effect mobilities of thin film pentacene transistors with different source/drain area. Figure 3.13 shows the fabricated thin film pentacene transistors with different source/drain contact area. All these transistors are fabricated via the in-house process describe in § 3.3.2. The data shown in Table 3.1 indicate that the mobility of pentacene does not vary a lot with the size of source/drain contacts. However, transistors with too small source/drain contacts (e.g., 100 μm $\times$ 100μm) show poor performance, according to previous observations.

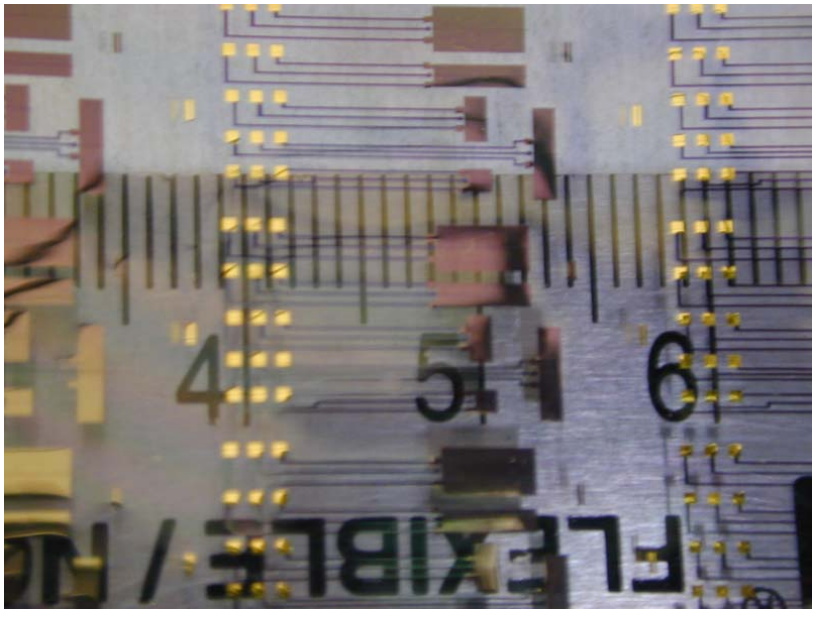


Figure 3.13: Pentacene TFT with difference source/drain contact area. From top to bottom: 4mm×2mm, 4mm×0.5mm, 1mm×1mm, 1mm×4mm, and 1mm×0.5mm.

Table 3.1: Mobilities of thin film pentacene transistors with different source/drain area (cm^2/Vs).

Chip\Area	4mm×2mm	4mm×0.5mm	1mm×1mm	1mm×4mm	1mm×0.5mm
Chip #1	0.05870	0.05208	0.04619	0.04948	0.05082
Chip #2	0.05067	0.05132	0.04785	0.05090	0.06286
Chip #3	0.06077	0.06577	0.06291	0.06725	0.06533
Chip #4	0.06093	0.06196	0.05769	0.05842	0.05104
Chip #5	0.04735	0.04582	0.04742	0.05072	0.04927
Chip #6	0.05089	0.04703	0.05061	0.04932	0.05598
Chip #7	0.04496	0.04293	0.04206	0.04905	0.04785

3.4.3.2 Source/Drain Metal and Thickness

To have thin film pentacene transistors with high mobilities, a proper metal must be selected as the source and drain electrodes that are in direct contact with pentacene. The contact resistance is a function of Schottky barrier, ψ_B at the metal-semiconduction interface. The Schottky barrier is the difference between the work function and and the ionization potential of the organic semiconductor. Previous studies have shown that the contact resistance heavily depends on the work function of the source and drain electrode metals [78][79]. Hole mobility of pentacene increases with work function of metals. If $\log(\mu)$ is plotted versus work function plot, there is a critical value, 4.3 eV, of work function. The mobility increase rapidly as the work function increases until it reaches 4.3 eV. The mobility increases slowly for work functions higher than 4.3 eV [79]. Thus choosing Au (work function 5.1 eV) as the source/drain contact promises optimal device performance.

In normal MEMS processes, a gold layer is accompanied by an auxiliary adhesion layer, usually Cr or Ti.

To measure the contact resistance, test structures are made on oxide wafers and pentacene is thermally evaporated onto the wafer. Figure 3.14 illustrates the testing structures of contact resistance measurement. Contact pads are 1500 Å Au with 200 Å Cr adhesion layer. The process used here is modified from the quick proccess as described in § 3.4.1. The I-V curves between the two metal pads are measured with HP4145B semiconductor parameter analyzer and total resistances are extracted from the I-V curves. The total resistance between two pads

are given in Equation 3.17.

$$R_{total} = 2R_c + \frac{\rho}{Wt} \times L \ , \tag{3.17}$$

where R_c is the contact resistance between the pad and pentacene, t the thickness of pentacene and L the gap length between two pads. R_c is extracted from the the plot of R_{total} by linear regression.

Table 3.2 lists the contact resistance between pentacene and Au/Cr. As can bee seen, the commonly used Au/Cr dual layer can have as high contact resistant as 150 MΩ. This is an enormous contact resistance that will render a poor thin-film transistor or even a failed transistor.

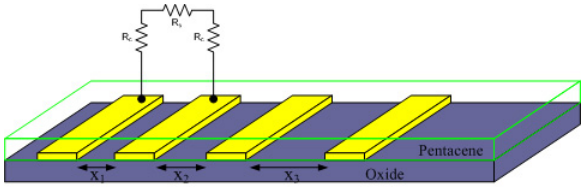


Figure 3.14: Testing structures for contact resistance measurement.

Table 3.2: Contact resistance between Au/Cr and pentacene.

Pad Sizes (μm^2)	**Metal**	**Contact Resistance**
1000×1000	1500 Å Au / 200 Å Cr	147.96 MΩ
800×800	1500 Å Au / 200 Å Cr	186.61 MΩ
600×600	1500 Å Au / 200 Å Cr	263.07 MΩ

The thickness of the Au layer and the existence of the adhesion layer are two factors rendering huge contact resistance. This adhesion layer could greatly increase the contact resistance and therefore hinder device performance. Yoneya *et al.* proposed a contact resistance model as shown in Equation 3.18 [80].

$$\begin{aligned} R_c W &= (t_{Au} + t_{ad} - t_{ch}) r_i^{-1} + (t_{ch} - t_{ad}) r_a^{-1}, \ t_{ad} < t_{ch} \\ &= t_{Au} r_i^{-1}, \ t_{ad} > t_{ch} \ , \end{aligned} \tag{3.18}$$

where the R_c is the total contact resistance, W the channel width, t_{Au}, t_{ad}, and t_{ch} the thicknesses of the Au, adhesion layer and the conducting channel layer, respectively. r_i is the resistance of the insulating pentacene layer. r_a is the resistance between the Au and layer and the conducting channels. Typically, the thickness of the conduction channel is less than 30 Å (see § 3.2.2), and Cr and Ti adhesion layers have thickness of around 150 to 200 Å. In this case where the adhesion metal layer is thicker than 30 Å, the contact resistance is determined by the thickness of Au and the resistance of the insulating pentacene, which also depends on the thickness of pentacene film. To lower the contact resistance, it is desired to have thin Au layer and the adhesion layer should be as thin as possible.

After performing several tests, it is found that Au can be deposited onto clean Parylene surface without any adhesion layer and be able to sustain later photolithographic and wet etching processes. A clean Parylene surface is one that goes through general cleaning processes and 30-second diluted HF dipping. However, such Au cannot survive common metal liftoff processes.

In all, 300 Å Au without any adhesion layer is chosen as the source and drain contact of the thin film pentacene transistors. As a comparison, thin film pentacene transistors with Au/Cr source/drain and pure Au source/drain are fabricated via the in-house process describe in § 3.3.2 and device parameters are listed in Table 3.3. Note that hole mobilities listed in Table 3.3 are extracted by the method described in § 2.5. The model does not incorporate contact resistance and therefore effects of contact resistance are included in the calculated hole mobilities.

It is clear that source and drain contacts made of thin Au without adhesion layers have much smaller contact resistances and the extracted field-effect hole mobility of such devices is one order of magnitude larger than that of transistors with source and drain contacts made of Au with adhesion layer.

Table 3.3: Hole mobilities of pentacene transistors with different source/drain contacts.

Source/Drain Contact	W/L	Hole Mobility (cm^2/Vs)
1500 Å / 200 Å Au/Cr	1000/25	5.18×10^{-3}
300 Å Au only	1000/25	4.62×10^{-2}

3.4.4 Annealing

As with the case of silicon, annealing can promote grain growth and thus hole mobility of pentacene. Two major annealing methods are available to improve device performance. One is raising the substrate temperature during pentacene deposition. The other is post-process annealing.

3.4.4.1 In-Situ Annealing

Raising the substrate temperature during deposition of pentacene films can increase the surface mobility of the pentacene molecules. The average grain size increases with the surface mobility of the deposited molecules and the field effect hole mobility increases with the grain size. Previous reports have shown that pentacene deposited on the substrates held at 60 – 100 °C has dendritic grains with diameters ranging from one micron to several microns [81][82].

To improve the performance of the thin film pentacene transistors and fine-tune the deposition process, pentacene transistors have been fabricated following the simplifed process described in § 3.4.1. These transistors uses silicon as the gate and thermally grown oxide as the gate insulator. The substrates are held at 50, 60, and 90 °C respectively during pentacene depositon. Table 3.4 summarizes performances of these transistors.

Table 3.4: Properties of pentacene transistors on oxide with different substrate temperatures during deposition (W/L=1000/20).

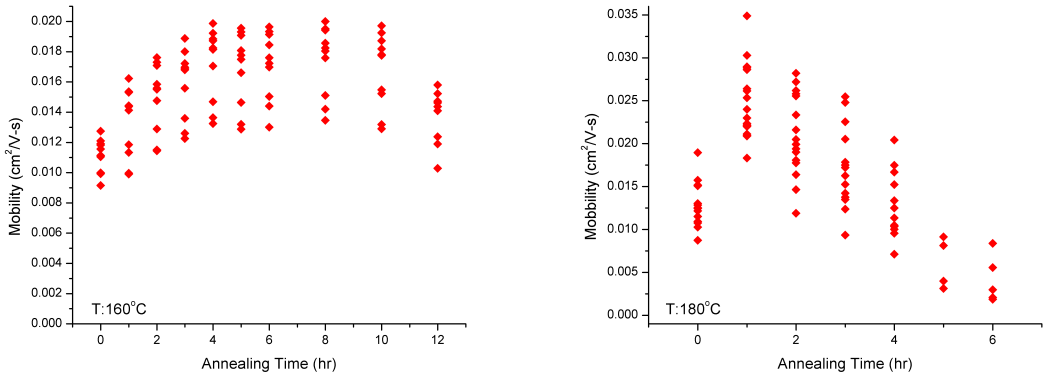
Substrate Temperature	Pentacene Mobility	Threshold Voltage	On/Off Ratio
Room Temperature (20 °C)	0.1269 cm^2/Vs	-4.701 V	10^6
50 °C	0.2315 cm^2/Vs	-5.798 V	10^5
60 °C	0.1150 cm^2/Vs	-5.029 V	10^4
90 °C	0.5609 cm^2/Vs	-14.82 V	10^4

The data show that with higher substrate temperatures, the hole mobility of pentacene transistors increases. However, the on/off ration decreases. And for samples of 90 °C, the threshold voltage increases up to -14.82 V. Though the grains are larger, pentacene films deposited at high substrate temperatures tend to have voids because of higher surface mobility. This might explain why the device performance decreases at higher substrate temperatures. Lin *et al.* proposed a solution of stacked layers of pentacene deposited at different substrate temperatures [82]. More data have to be collected to reach a solid conclusion.

3.4.4.2 Post-Process Annealing

Previous reports have shown some work on post-process annealing of thin film pentacene transistors [83][84]. However, these works used temperatures below 100 °C due to the temperature limitation of pentacene and other polymers used in the devices. The higher the annealing temperature is, the better effect the annealing will have. Therefore, it is desired to perform the annealing process with as high temperatures as possible. Although the melting temperature of pentacene is unknown, the evaporation temperature is around 185 °C. This places the upper limit of the annealing temperatures. With the help of Parylene C coating, it is possible to anneal thin film pentacene transistors at temperatures up to 180 °C. The pentacene films are fabricated by the in-house process described in § 3.3.2. After fabrication, the manually-cut pentacene transistor films (Figure 3.10) are placed in a nitrogen-back-filled vacuum annealing oven at various temperatures and duration. The pressure of the vacuum oven is 0.1 mTorr. The tested annealing temperatures are 160 °C, 180 °C and 200 °C. The annealing time ranges from 1 hour to 12 hours. Figure 3.15 shows the mobilties of thin film pentacene transistors annealed at 160 °C and 180 °C versus annealing time. No data is available for devices annealed at 200 °C since all the devices failed after annealing at 200 °C regardless of annealing time.

As Figure 3.15 shows, all transistors show higher mobilities after post-process annealing. However, there are optimal annealing hours. For the samples annealed at 180 °C, the samples annealed longer than one hour show decreased mobilities. But for the samples annealed at 160



(a) Annealing at 160°

(b) Annealing at 180°

Figure 3.15: Pentacene mobilities after post-process annealing.

°C, pentacene mobility increases, saturates and decreases after 12 hour-annealing. It seems no brainer that annealing could increase the pentacene mobilities since these pentacene transistors have pretty low mobilities. To serve as a control group, pentacene transistors are fabricated on oxide surface and have high mobilities. The same trend can be observed for pentacene transistors fabricated on oxide wafers with Parylene C top cover as shown in Figure 3.16.

Decrease of pentacene mobilities after certain hours of annealing may result from evaporation of pentacene. This can be seen from pentacene transistor films after annealing. Figure 3.17 shows as-fabricated and annealed pentacene transistor films. The film annealed at 180 °C for 8 hours loses almost all the pentacene and changes color. Pentacene might escape from the cut edges of the film since these films are manually cut and are not completely coated with Parylene. A quick amendment would be coating the films completely with Parylene C after fabrication.

3.4.5 Surface Modification

It is reported that pentacene has higher field effect mobility on surfaces treated with a layer of self-assembly molecules (SAM) [81]. Highly-ordered surfaces may help large grain growth. Common SAMs are hexamethyldisilazane (HMDS) and trichloro(octadecyl)silane $C_{18}H_{37}SiCl_3$

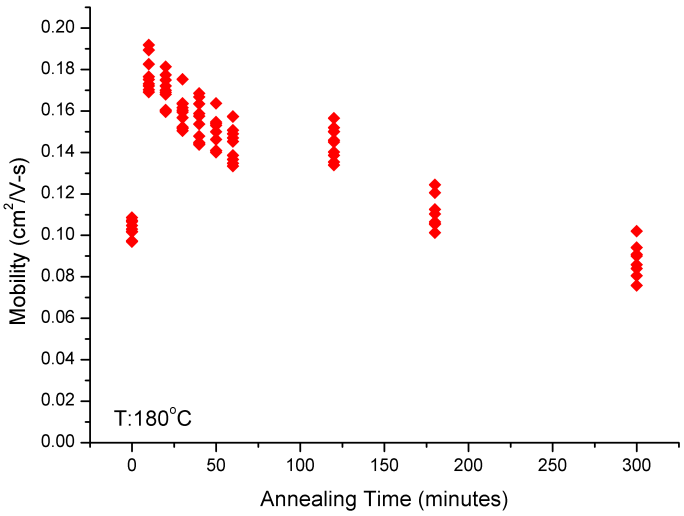
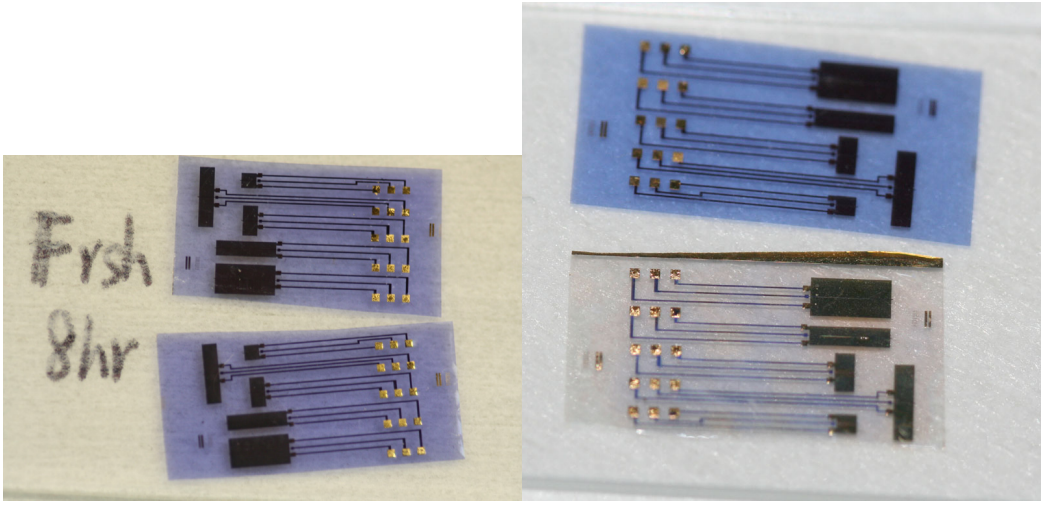


Figure 3.16: Mobilities of pentacene transistors on oxide after post-process annealing at 180 °C.



(a) 160 °C (b) 180 °C

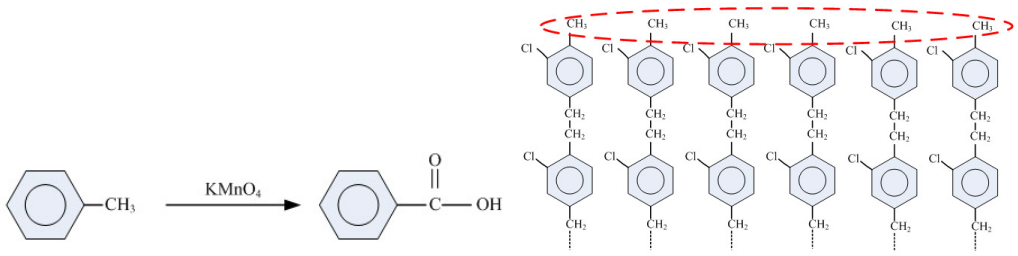
Figure 3.17: Comparison of pentacene transistor films as fabricated and annealed for 8 hours.

(OTS).

However, it requires additional treatment to apply OTS SAM layers on Parylene surfaces due to the lack of hydroxyl groups on Parylene surface. Parylene as deposited is hydrophobic and has a contact angle of 80°. Several ways add hydroxyl groups onto Parylene surfaces. Short exposure under low-power oxygen plasma can add hydroxyl group to parylene surfaces and reduce the contact angle to 30°. However, oxygen plasma treatment increases the surface roughness of Parylene films and this increased surface roughness will have detrimental influences on later device performances (see § 3.4.6).

To maintain surface roughness or at least not to increase, other chemical modifications have to be resorted to. Ozone treatment is a good candidate. The Parylene film after 30 minutes of ozone treatment show contact angles of 30°, same as the oxide surface and the surface roughness remains the same.

In addition to oxidation of free radicals, proper oxidizing agent can also serve the purpose. The oxidizing agent, Potassium Permanganate ($KMnO_4$) can oxidized the methyl group on a benzene ring into a carboxylic group. This chemistry can be applied to Parylene C, since Parylene C also has methyl groups on the benzene ring. Figure 3.18 illustrates the reaction of KMn_4 and the surface of Parylene C polymers.



(a) The $KMnO_4$ reaction (b) The surface of Parylene C

Figure 3.18: Illustration of $KMnO_4$ reaction and the surface of Parylene C.

The process of KMn_4 oxidation used here is dipping the Parylene C films into a 0.1 M $KMnO_4$ solution at 80 °C for 1 hour. $KMnO_4$ powder is purchased from Sigma-Aldrich Inc..

OTS is purchase from Sigma-Aldrich Inc. and the application of OTS is broken into the

following steps:

1. Dipping in isopropyl alcohol (IPA) for 10 minutes.
2. Dipping in toluene for 10 minutes.
3. Dipping in OTS/toluene solution (1 drop of OTS in 50 mL toluene) for 10 minutes.
4. Dipping in toluene for 10 minutes.
5. Dipping in IPA for 10 minutes.

In the above process, the sample is immersed in polar solution, non-polar solution and back to polar solution.

The contact angles of Parylene C surfaces are 80° after OTS treatment only and 105° after $KMnO_4$ oxidation followed by OTS treatment. It is clear that without adding hydroxyl groups, OTS SAM layers cannot be applied onto the Parylene C surfaces.

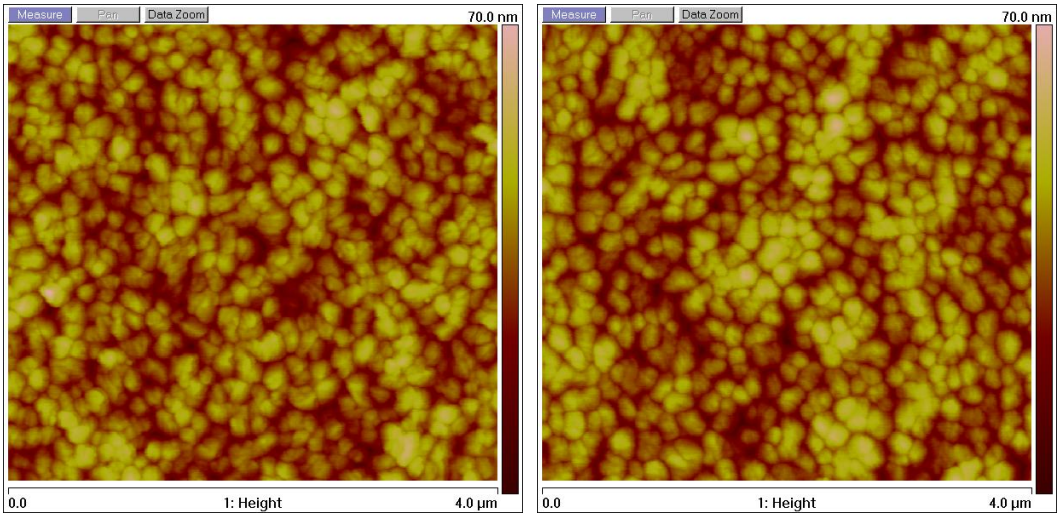
Table 3.5 summarizes contact angles of the Parylene C surfaces after various treatment.

Table 3.5: Contact angles of parylene surfaces after various treatments.

Treatment of Parylene Surfaces	**Contact Angle(°)**
As deposited	80
$KMnO_4$	30[1]
OTS	80
$KMnO_4$ + OTS	105[2]
Ozone	30[1]
Oxygen plasma	< 5

[1] Same as the contact angle of the oxide surface
[2] Same as the contacnt angle of the OTS-treated oxide surface

Oxidation of parylene surface with potassium permanganate solution followed by OTS treatment changes surface energy of parylene surfaces and thus might change the morphology of pentacene deposited on top. However, SPM images show no difference of surface morphology of pentacene deposited on these surfaces. Some other factors must have greater influences on pentacene grain growth than the difference of surface energy of Parylene C and oxide.



(a) Pentacene on Parylene treated with $KMnO_4$ followed by OTS.

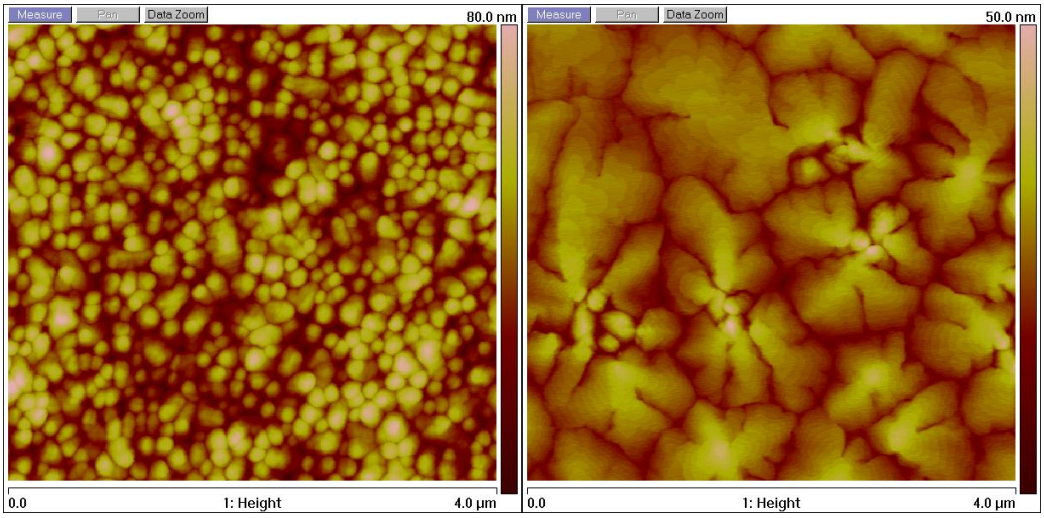
(b) Pentacene on Parylene treated with OTS only.

Figure 3.19: SPM images of pentene on Parylene surfaces treated with $KMnO_4$ and OTS.

3.4.6 Surface Roughness

By the data measured from previous devices, the pentacene transistors with oxide gate dielectrics have always higher mobilities than those with Parylene as gate dielectrics, at least one order of magnitude. The fabrication processes and conditions of the two transistors are the same. Figure 3.20 shows the SPM images of pentacene deposited on Parylene C and oxide. The morphologies of the two pentacene films are quite different and the difference must comes from the surface properties of Parylene and oxide. Pentacene grains are much smaller on the Parylene surface that on the oxide surface and smaller grains lead to lower field effect mobility (see § 3.2.4). Hydrophobicity and hydrophilicity do not play important roles since most thin film pentacene transistors deposited on OTS treatment oxide surfaces. OTS treatment makes the surface of the oxide as hydrophobic as the as-deposited Parylene C surface. As discussed in the previous section (§ 3.4.5), OTS treatment of Parylene C surfaces does not change the morphology of the pentacene films deposited on top. Another factor could affect the grain growth is surface roughness.

To study the surface roughness and surface morphology, scanning probe microscopy (SPM)



(a) Pentacene on As-deposited Parylene (b) Pentacene on As-deposited oxide

Figure 3.20: SPM images of pentacene on As-deposited Parylene and oxide.

or atomic force microscopy (AFM) is employed. The SPM equipment used here is the Veeco Digital Instrument Dimension 3100 Atomic Force Microscope. The surface roughness is evaluated by the built-in computer software. The arithmetic roughness, R_a is the the arithmetic average of the absolute values of the surface height deviations measured from the mean plane and is given by Equation 3.19. In addition, the root mean square roughness, R_q is the root mean square average of height deviations taken from the mean data plane and is given by Equation 3.20.

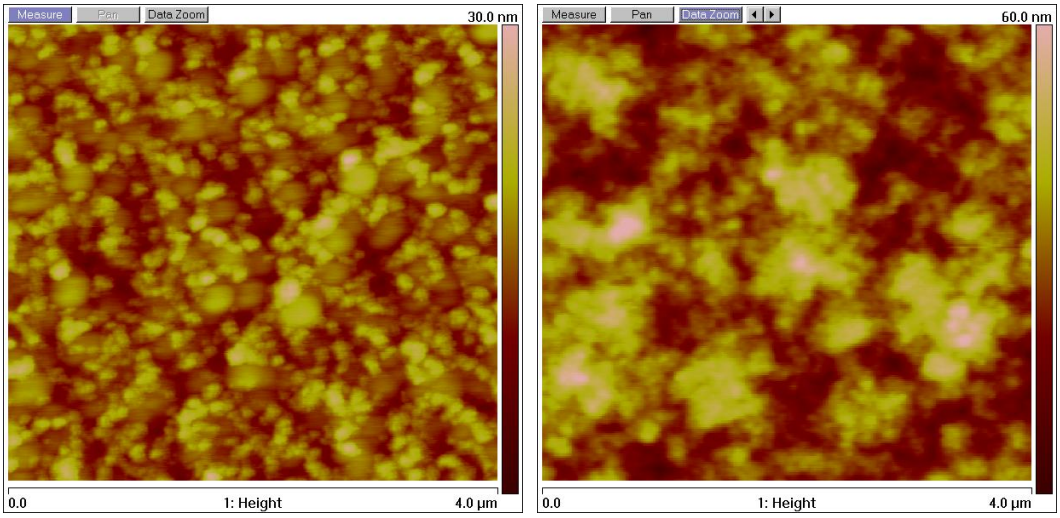
$$R_a = \frac{1}{N}\sum_{j=1}^{N}\left|Z_j\right| \tag{3.19}$$

$$R_q = \sqrt{\frac{\sum_{j=1}^{N}\left|Z_j\right|}{N}}, \tag{3.20}$$

where Z_j is the height deviation from the averaged plane height of the surface and N is the number of sample points.

Figure 3.21 shows the SPM images of as-deposited 0.3 μm and 10 μm Parylene C surfaces and Figure 3.22 shows the SPM image of a typical oxide surface. In fact, the flat and smooth oxide surface is beyond the resolution of the Dimension 3100 AFM. That is why the SPM image is

full of noises. The root-mean square surface roughness of as-deposited Parylene C are around 5 nm while that of a typical oxide surface is 0.115 nm.



(a) 0.3 μm Parylene C (b) 10 μm Parylene C.

Figure 3.21: SPM images of as-deposited Parylene C.

3.4.6.1 Surface Roughness, Film Thickness and Reflow Annealing

The mean-square-root surface roughness of Parylene C depends on the thickness of the film. Generally speaking, the thicker the film is, the rougher it is. Figure 3.23 shows the plot of surface roughness of Parylene C versus thickness.

Parylene C has melting point of about 270 – 290 °C and glass transition temperature of 80 °C. Parylene C starts reflowing at temperatures above its glass transition temperature. Therefore, it is possible to reduce the surface roughness of parylene C by reflowing the film. Figures 3.24, 3.25 and 3.26 show the plots of the surface roughness of Parylene C films versus annealing time.

Although reflow annealing does reduce the surface roughness of Parylene C but the resulting surface roughness is still too large, compared to that of oxide surfaces.

To further reduce the surface roughness of Parylene in the reflow process, Parylene C films are clamped with Al-coated Si wafers during reflow annealing. Because Parylene is thermoplas-

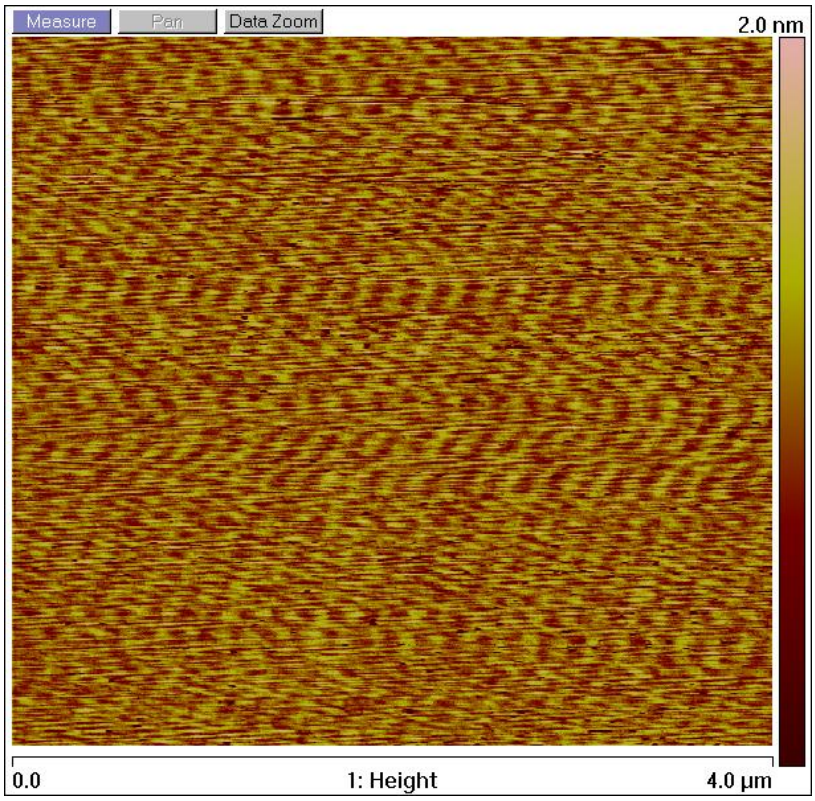


Figure 3.22: SPM image of an oxide wafer. It is beyond the resolution of the SPM.

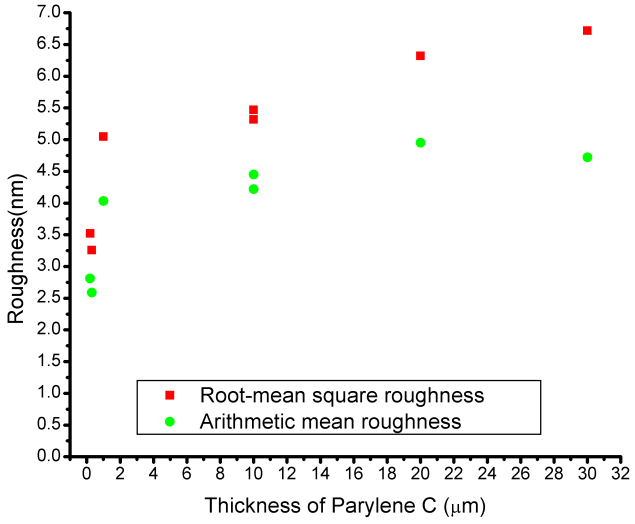


Figure 3.23: Surface roughness versus film thickness of as-deposited Parylene C.

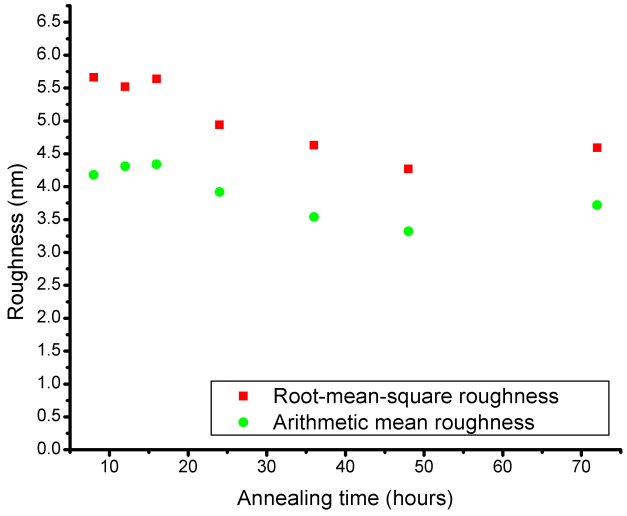


Figure 3.24: Surface roughness of 5 μm Parylene C after annealing at 180 °C.

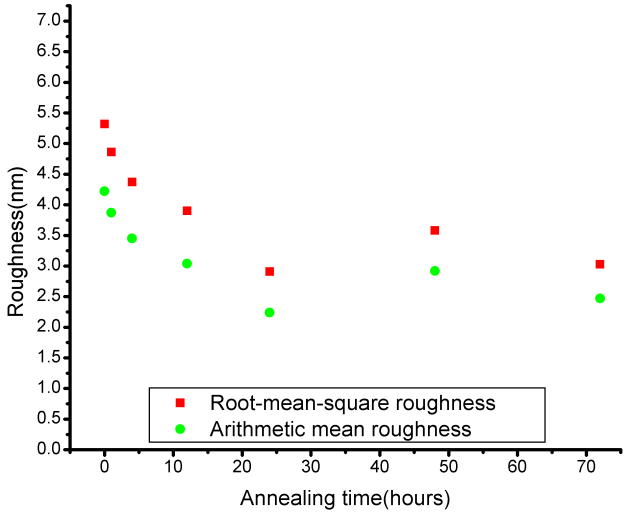


Figure 3.25: Surface roughness of 10 μm Parylene C after annealing at 200 °C.

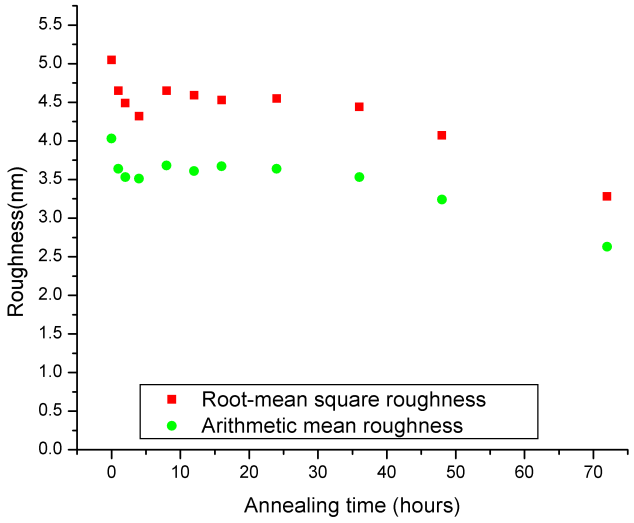


Figure 3.26: Surface roughness of 1 μm Parylene C after annealing at 200 °C.

tic, it can be deformed with high pressures and high temperatures. Here, the Parylene films are clamed with silicon wafers, pressed with heavy weights and baked in the vacuum oven. Table 3.6 lists the resulting surface roughness. Clamping with Al-coated wafers does not give better results than plain annealing.

Table 3.6: Surface roughness of Parylene C after annealing at 200°C.

Annealing time (hour)	R_q (nm)	R_a (nm)
As-deposited	5.04	3.96
2	4.76	3.68
24	4.53	3.57

(Samples are clamped with Al-coated wafers)

3.4.6.2 Flip-Parylene

Although reflow annealing can reduce surface roughness of parylene C, the film after reflow annealing is still not smooth enough for large pentacene grain growth. To produce a Parylene surface as smooth as oxide surfaces, a flip-Parylene film process is created. This process employs the conformal coating capability of Parylene C and the smooth surfaces of commercial

silicon or oxide wafers. The fabrication process start with a commercially available, single-side-polished prime wafers. After cleaning the wafer, Parylene C is deposited on the silicon wafer. Next a piece of silicon is attached on the Parylene C coated wafer. A second layer of Parylene C (30 μm thick) is deposited. After deposition of the second layer of Parylene C, the whole Parylene film, including the silicon piece is lifted from the substrate wafer. Figure 3.27 shows the illustrated process flow and the fabricated Parylene C film. The surface previously in contact with the bottom silicon wafer is now facing up and ready for further fabrication processes. This surface is named "flip-Parylene". The surface roughness of the flip-Parylene is R_q 0.279nm and R_a 0.211nm, approaching the values of oxide surfaces.

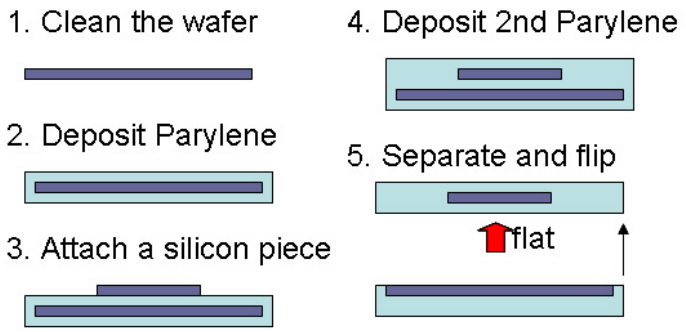
Pentacene is deposited onto the flip-Parylene C and Figure 3.28 shows the SPM image of pentacene. Compared to pentacene on as-deposited Parylene C (Figure 3.20a), pentacene deposited on Flip-Parylene has larger grains, as shown in Figure 3.28. However, compared to pentacene deposited on oxide (Figure 3.20b), the grains are still relatively small.

Although flip-Parylene provides smooth surfaces with root-mean-square roughness comparable to oxide surfaces. It is difficult to fabricated pentacene film transistors incorporating flip-Parylene.

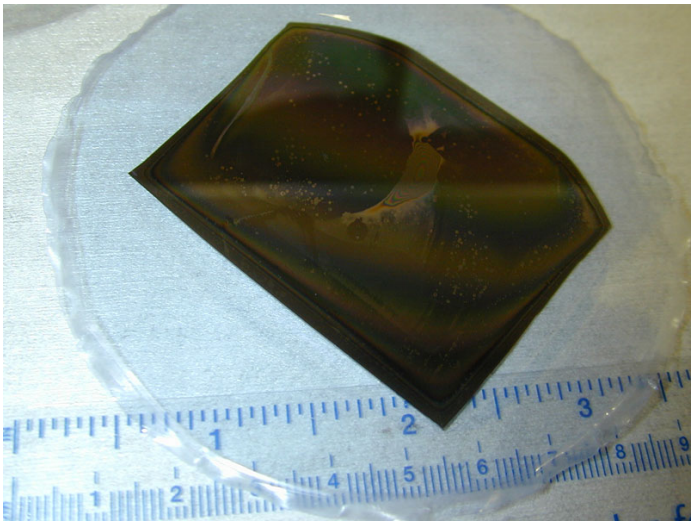
3.4.6.3 Spin-Cast Smoothing Layers

While Parylene is deposited via the room-temperature CVD process, some other dielectrics can be prepared via spin-casting processes.

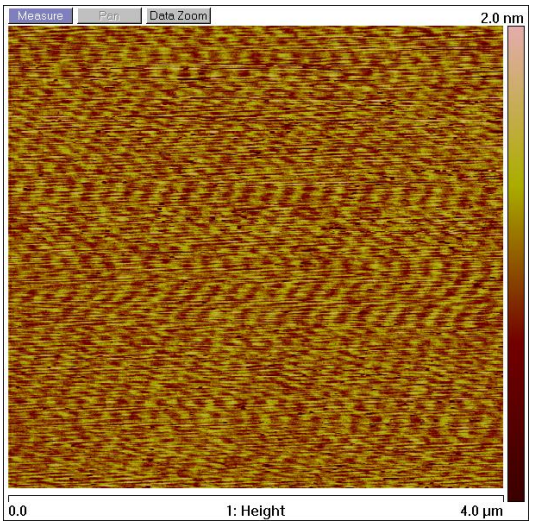
Several spin-cast dielectrics have been reported as the gate insulating dielectrics of thin film pentacene transistors. Among them, there are poly(4-vinylphenol) (PVP) and poly(methyl methacrylate) (PMMA). However, these spin-cast dielectrics have pretty low breakdown voltages and thus are not able to sustain high gate voltages. Meanwhile, Parylene C has a breakdown voltage of 200 V/μm. To preserve the high breakdown voltage of Parylene C and smoothness of spin-cast dielectric, a dual layer of spin-cast dielectric and Parylene C is employed as the gate insulating dielectrics. While Parylene C comprises most of the dielectric, a 1000 Å spin-cast



(a) Flip-Parylene process flow

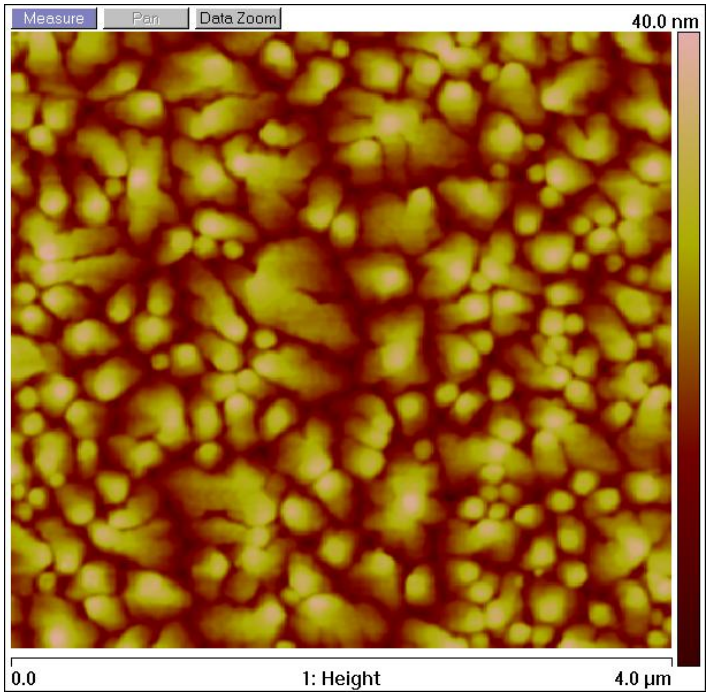


(b) Flip-Parylene film

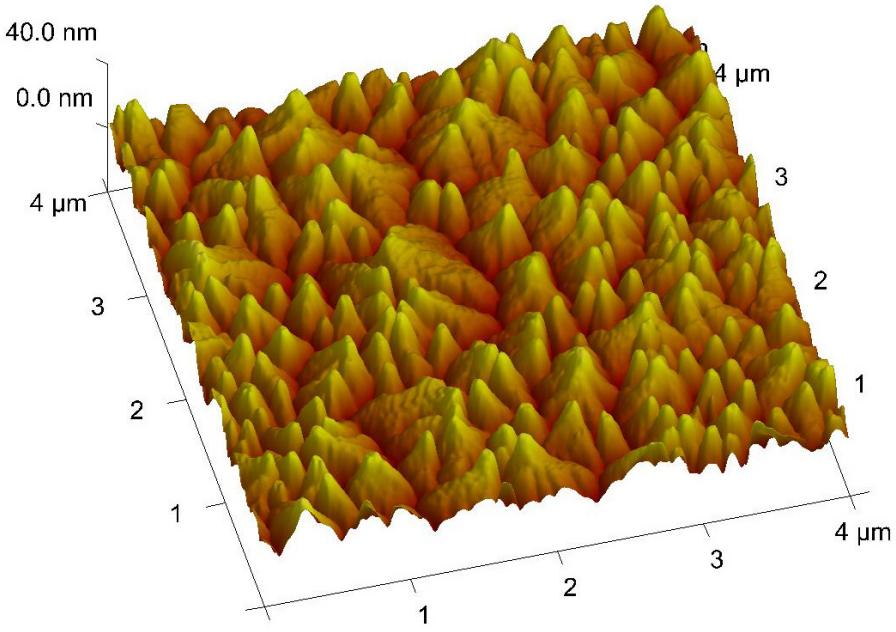


(c) SPM image

Figure 3.27: Flip-Parylene.



(a) Heigth view



(b) 3D view

Figure 3.28: SPM images of pentacene on Flip-Parylene.

dielectric is deposited on top as a smoothing layer.

The PVP solution is made of 5 to 10 wt.% of poly(4-vinylphenol) in propylene glycol monomethyl ether acetate (PGMEA). 5 to 10 wt.% crosslinking agent, (poly(melamine-co-formaldehyde) methylated/butylated, (55/45)) is added to the PVP solution to increase its chemical resistance. All these chemicals are purchased from Sigma-Aldrich Inc..

The PMMA solution is 495 PMMA A2 from MicroChem Corp. and the SU8-2 is also purchased from MicroChem Corp. Both solutions are applied as purchased without any dilution.

Table 3.7 summaries properties of the Parylene C surfaces smoothed with various spin-cast dielectrics.

Table 3.7: Surface roughness of Parylene C smoothed with various spin-cast dielectrics.

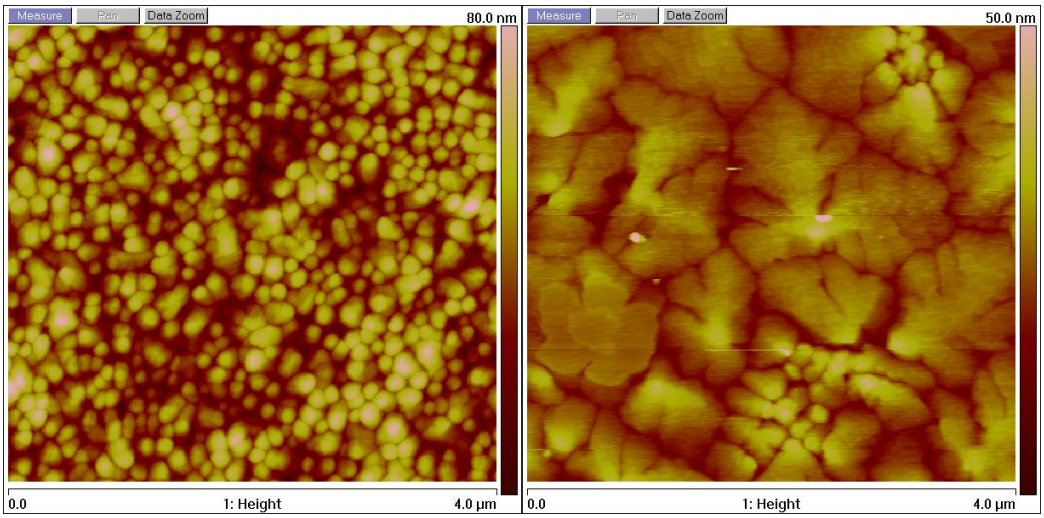
	Smoothing Layer	**Original Substrate**	**Smoothing Layer Thickness (Å)**
1.	None	0.2μm ParyleneC	0
2.	495 PMMA A2[1]	0.2μm Parylene C	967
3.	495 PMMA A2[2]	10μm Parylene C	1400
4.	PVP[3]	0.2μm Parylene C	1300
5.	PVP[4]	10μm Parylene C	5600
6.	SU8-2[5]	10μm Parylene C	9600

(continued)

	R_a (nm)	**R_q(nm)**	**Grain Diameter (μm)[6]**
1.	2.81	3.52	0.378
2.	0.52	0.65	0.852
3.	0.755	0.96	0.941
4.	0.984	1.23	0.559
5.	0.486	0.382	0.742
6.	0.325	0.409	0.68

[1] 1k rpm, 40-second spin coating
[2] 500 rpm, 40-second spin coating
[3] 5 wt.% PVP in PGMEA, 3k rpm, 40-second spin coating
[4] 10 wt.% PVP + 5 wt.% CLA in PGMEA, 1k rpm, 40-second spin coating
[5] 5k rpm, 40-second spin coating
[6] Grain diamerters are calculated via the method describe in § 3.4.7.3

Figure 3.29 shows SPM images of pentacene deposited on the Parylene C surfaces smoothed with various spin-cast dielectrics.



(a) As-deposited Parylene (b) PMMA

(c) PVP (d) SU8-2

Figure 3.29: SPM images of pentacene on Parylene surface smoothed with spin-cast dielectrics.

3.4.7 Source/Drain Contact Configuration

Organic thin-film transistors usually use bottom gates with top or bottom source and drain contacts. It is well known that transistors with top contact configurations show better performances than those with bottom contact configurations. The reason is believed to be smaller contact resistances of top contacts. However, the source and drain contacts of the transistors with top contact configurations must be deposited through mechanical masks. For transistors with top contact configurations, the organic semiconductor film is deposited before the source and drain contacts and no conventional photolithography can be carried out after deposition of organic semiconductor layers. Pentacene and other organic semiconductors are extremely sensitive to organic solvents used in the photolithographic processes. The organic solvents in the photoresist, for example, dissolve and damage the pentacene thin film. Therefore, the only way to have source and drain contacts is to evaporate metals through mechanical masks.

3.4.7.1 Mechanical Masks

Metal evaporation through mechanical masks can eliminate the need of photolithography. Common mechanical masks are made of metals, for example steel. However, metal mechanical masks are expensive and the resolution of the mechanical masks are not small. Once the mechanical masks are finished, there is no easy way to change the designs.

To have design flexibility and both time-saving and low cost processes, mechanical masks made of Parylene C and silicon are developed.

Parylene Mechanical Masks Parylene C with its particular mechanical properties has been widely used in MEMS applications as the structural material. With enough thickness, Parylene C can be used as the mechanical masks. The process releases the Parylene film with a Cr sacrificial layer and the Parylene C film is patterned with Al metal masking layer due to the unusual thickness. Before releasing, a stress-relieving annealing step is carried out. According to Harder *et al.*, as-deposited Parylene C films have compressive stress and after annealing at

temperatures above 100 °C, the stress becomes tensile [85]. The fabricating process of Parylene C mechanical masks is listed below:

1. Wafer Cleaning: The process starts with cleaning a wafer. The wafer could be either a silicon wafer or an oxide wafer. The wafer is rinsed with DI water and purged dry with nitrogen. Piranha cleaning is carried out and followed by a 30-second dip in diluted HF.

2. Deposition of Cr Sacrificial Layer: A 1000 Å Cr layer is deposited onto the wafer via thermal or e-beam evaporation.

3. Deposition of Parylene C: 30 to 40 μm Parylene C is deposited onto the wafer.

4. Deposition and Patterning of Al Patterning Mask Layer: A 1000 Å Al layer is deposited on top of the Parylene C layer by e-beam or thermal evaporation. Al patterning is achieved via wet etching processes. A 2 μm AZ1518 photoresist is spun on to the wafer and baked at 100 °C for 30 minutes. This layer of photoresist is then exposed and developed. After developing, a descum process is done by short exposure in oxygen plasma. Afterwards, the wafer is hard-baked at 120 °C for 30 minutes. Al is etched with Transene Al Etch Type A. After etching, the photoresist is dissolved with ATMI ST-22 photoresist stripper. Next, the wafer is rinsed with ATMI PSR post-solvent rinse and DI water.

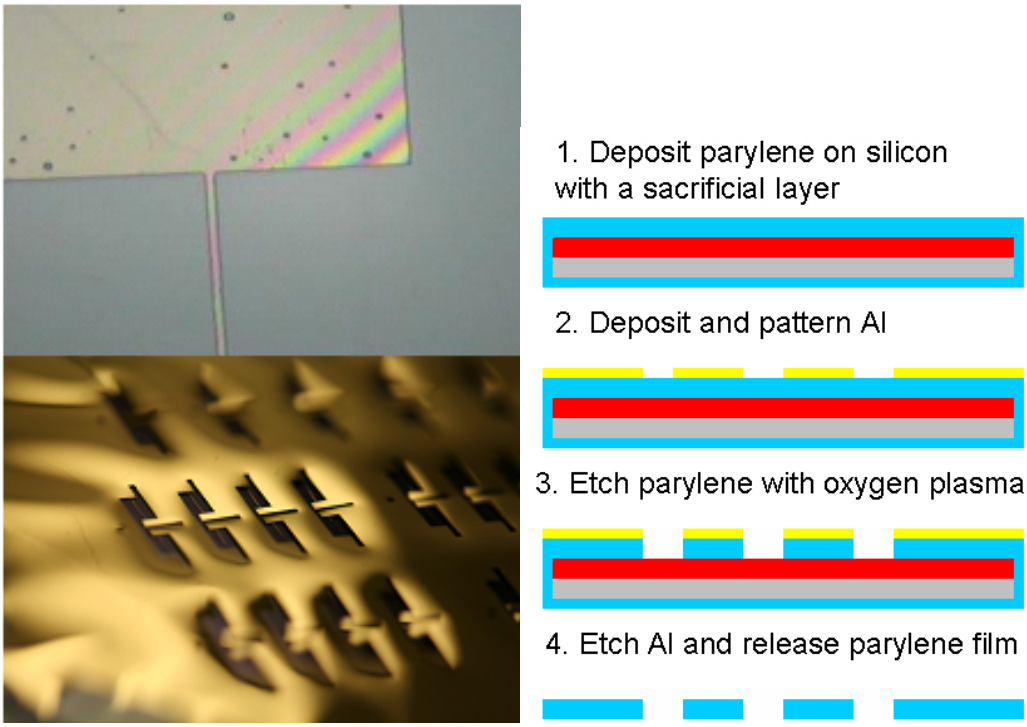
5. Patterning of Parylene C: The Parylene C layer is patterned with oxygen plasma in an reactive-ion etching system (RIE).

6. Removing Al Mask Layer: After RIE, the Al mask layer is removed with Al Etch.

7. Stress-relieving Annealing: Before releasing, the Parylene C film is annealed in a vacuum oven at 140 °C for 1 hour.

8. Releasing The Film: The last step is to release the Parylene C film with Cr-7.

Figure 3.30 shows the mechanical mask made of Parylene C. The smallest Parylene bridge is 50 μm and the final gap between metals evaporated through the Parylene C mask with 50 μm bridge is 40 μm.



(a) Parylene C mechanical mask (b) Illustrated Process

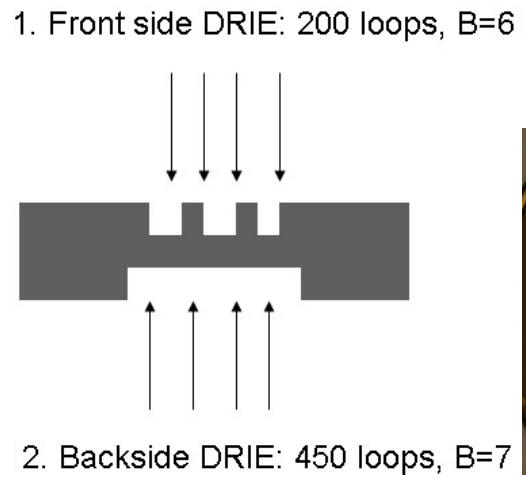
Figure 3.30: Parylene mechanical mask and the illustrated process.

Silicon Mechanical Masks Although Parylene mechanical masks offer a quick and economical alternative for conventional metal mechanical mask, the resolution of the evaporated metal is not enough. The minimum gap of metal evaporated through the Parylene C mechanical mask is around 40μm. To achieve higher resolutions, a mechanical mask made of silicon is developed.

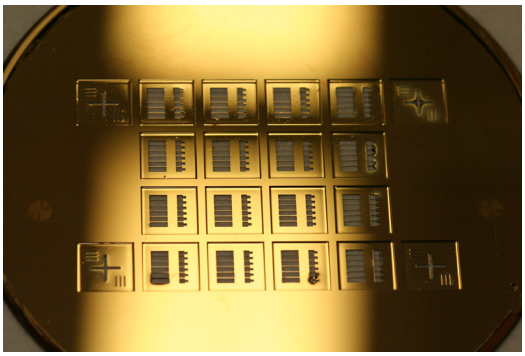
The silicon mechanical mask uses two-side DRIE processes. The front-side DRIE etching defines the patterns of the mechanical mask and the backside DRIE etching thins down the wafer and finishes the mechanical mask. Figure 3.31 shows the mechanical mask made of silicon. The smallest silicon bridge is 20 μm and the final gap between metals evaporated through the silicon mask with 20 μm bridge is 15 μm.

3.4.7.2 Top Contact versus Bottom Contact

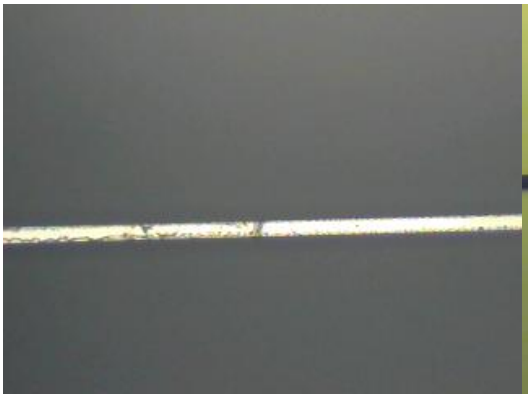
With the help of mechanical masks and smoothing layers, pentacene transistors with high performances can be made. Table 3.8 summarizes properties of thin film pentacene transistors



(a) Illustrated Process



(b) Silicon Mechnical Mask

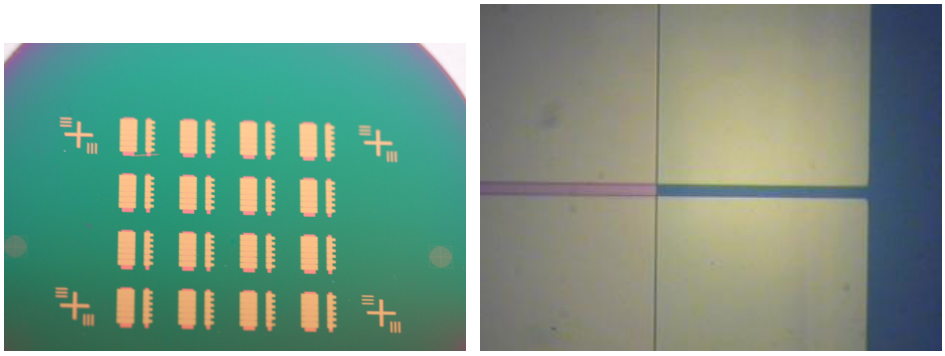


(c) The 20μm bridge of the mask

(d) The 15μm gap of the evaporated metal

Figure 3.31: Silicon mechanical mask and the illustrated process.

using smoothing layers and top/bottom contact configurations. All these transistors are fabricated by the simplifed process described in § 3.4.1. Figure 3.32 shows the pentacene transistors with the top-contact structure. The transistors with top contacts show significant higher hole mobility than those with bottom contacts. Besides, smoothing layers improves the mobility only for the transistors with top-contact configurations. For the transistors with bottom contact configuration, the smoothing layers do not have any effect on the hole mobility. This raises a new problem and the next section discusses this problem in details.



(a) The wafer (b) The transistor with a 40 μm long channel

Figure 3.32: The pentacene transistor using top-contact structures.

Table 3.8: Properties of thin film pentacene transistors using smoothing layers and top/bottom contact configurations.

Gate Insulating dielectric	2000Å Parylene C				
Contact Configuration	Bottom Contact		Top Contact		
Smoothing Layer	None	PVP[1]	None	PVP[2]	PMMA[3]
Mobility (cm^2/Vs)	0.02	0.02	0.04	0.2	0.2

[1] 10 wt.% PVP + 10 wt.% CLA in PGMEA, 3k rpm, 40-second spin coating
[2] 5 wt.% PVP in PGMEA, 3k rpm, 40-second spin coating
[3] 495 PMMA A2, 1k rpm, 40-second spin coating

3.4.7.3 Metal Supression of Pentacene Grain Growth

In the previous sections, pentacene transistors with bottom-contact and top-contact configurations are compared and discussed. Transistors with bottom-contact configurations are fab-

ricated in such a way that metal is deposited and patterned before pentacene deposition. This process makes it difficult to achieve flat and smooth enough surfaces to grow large pentacene grains since photolithographic and etching steps usually make surfaces rough. However, by comparing pentacene transistors fabricated on oxide surfaces with top-contact and bottom-contact source/drain electrode evaporated through shadow masks, bottom-contact transistors show much lower mobilities than top-contact ones, 2 orders of magnitude lower. Table 3.9 summarizes the properties of top-contact and bottom-contact pentacene transistors fabricated on the oxide wafer. Such small mobility results from small pentacene grains. Even on the same surface, pentacene tends to have smaller grains if metal is present. Figure 3.33 shows SPM images of pentacene inside the channels of the transistors described in Table 3.9.

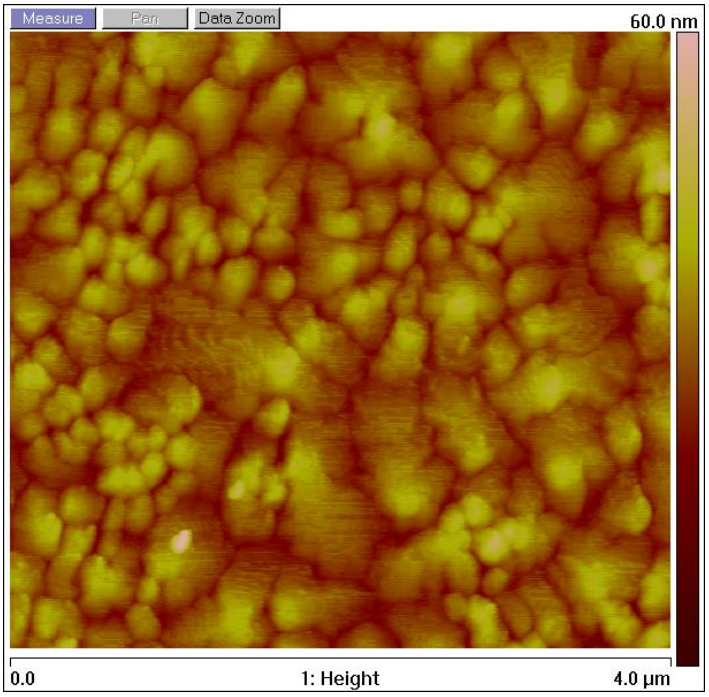
Table 3.9: Properties of top/bottom contact pentacene transistors on oxide (W/L=4000/20).

Contact Configuration	Top Contact	Bottom Contact
Gate Insulating Dielectric	900Å oxide	900Å oxide
Mobility (cm^2/Vs)	0.29802	0.0053563
Threshold Voltage (V)	-2.396	-1.339
On/Off Ratio	100	10^4

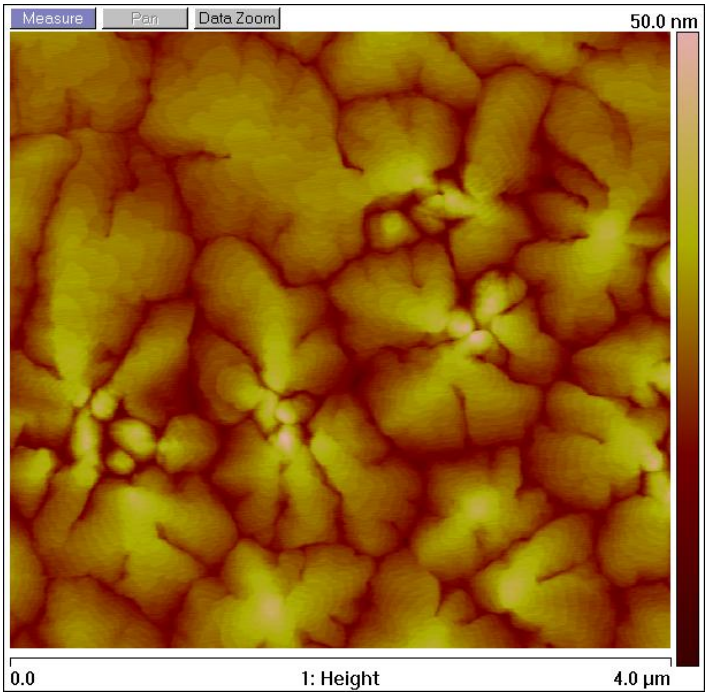
It is clear that pentacene has smaller grains near the metal, Au. Figure 3.34 shows the SPM images of pentacene on top of the metal, Au, and right at the edge of the metal, Au.

Estimation of Grain Sizes To fully study this phenomenon, a systematic algorithm of estimating pentacene grain sizes is required. Here, a simple and easy method is used. First, pentacen SPM images of the same area (4μm by 4μm) and same height color scales are taken. The colored SPM images are next converted into binary images with a fixed threhold values. The image processing application, Scion Image®, is next used to count particle numbers in the converted binary images. Once the number of particles is obtained, the average grain diameter is calculated assuming all grains are circular. Figure 3.35 illustrates this algorithm.

Different Substrates First, the dependence of substrates is studied. The preparation of samples start with prime silicon wafers. For oxide samples, silicon wafers first are cleaned with

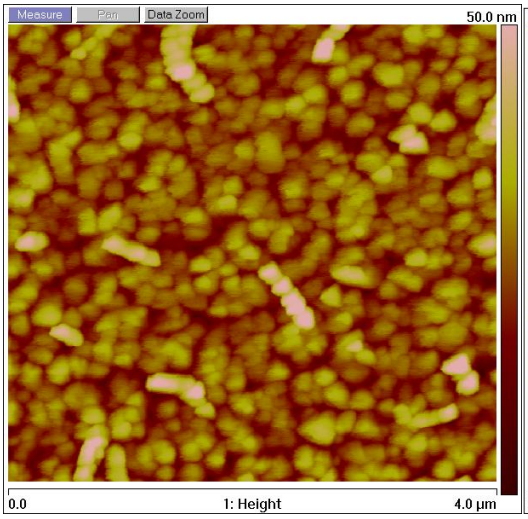


(a) Inside the bottom-contact channel

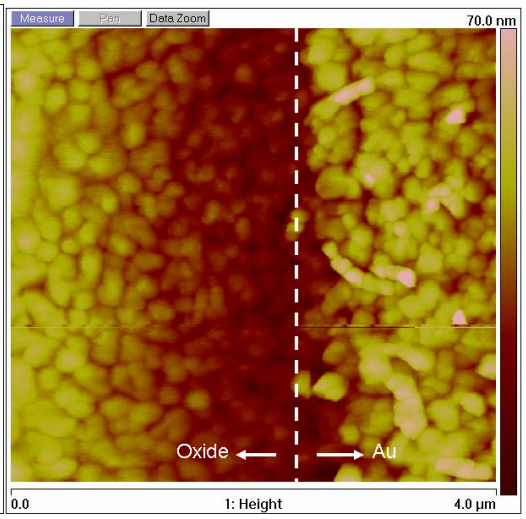


(b) Inside the top-contact channel

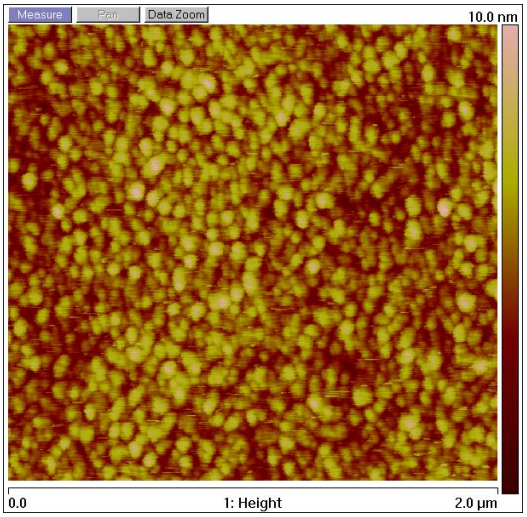
Figure 3.33: SPM images of pentacene on oxide.



(a) Pentacene on Au

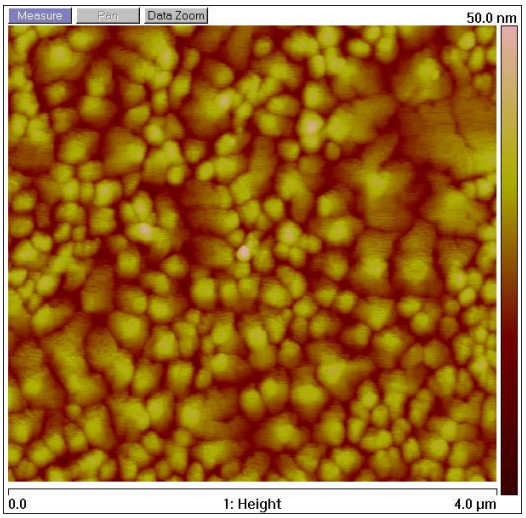


(b) Pentacene on Oxide-Au interface

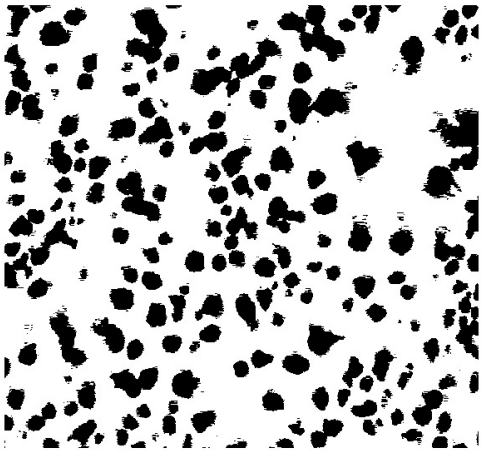


(c) Au surface

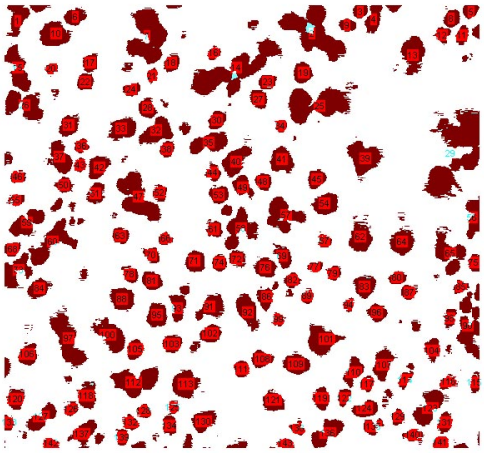
Figure 3.34: SPM images of pentacene on Au and oxide.



(a) Obtain SPM image



(b) Convert to a binary image



(c) Count particles with Scion Image®

$$2R = \sqrt{\frac{4\mu m \times 4\mu m}{N\pi}}$$

(d) Calculate average diameter

Figure 3.35: Illustration of the algorithm of grain sizes estimation (a) to (d).

piranha solution for 10 minutes and 1000 Å of silicon dioxide is then thermally grown on silicon surface. For PVP samples, poly-4-vinylphenol or PVP (from Sigma Aldrich), is dissolved in PGMEA to make 10 wt.% PVP solution. This 10 wt.% PVP solution is then spin-cast on silicon wafers at 3000 rpm for 40 seconds. After PVP spin-casting, PVP samples are baked at 100 °C for 30 minutes. SU8-2 samples preparation starts with dehydrating baking of silicon wafers at 100 °C for 5 minutes. SU8-2 from Microchem Corp. is spin-cast onto silicon wafers at 3000 rpm for 30 seconds. Soft-bake of SU8-2 samples is done on a hot plate for 1 minute at 60 °C, followed by 1 minute at 95 °C. UV exposure is carried out to cross-link SU8-2. Finally, the post exposure bake is done on the hot plate for 1 minute at 60 °C, followed by 1 minute at 95 °C, which completes the preparation of SU8 samples.

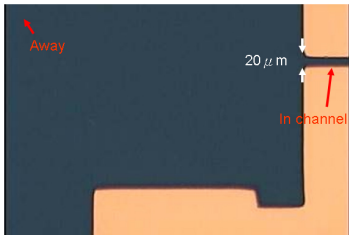
After sample preparation, 500 Å gold is thermally evaporated through shadow masks to avoid surface contamination from photolithographic pattern. Pentacene is then thermally evaporated at a rate of 0.1 Å/second under 10^{-7} Torr vacuum. During pentacene evaporation, all the samples are held at room temperature.

SPM images are taken and grain diameters are estimated by the method described in § 3.4.7.3.

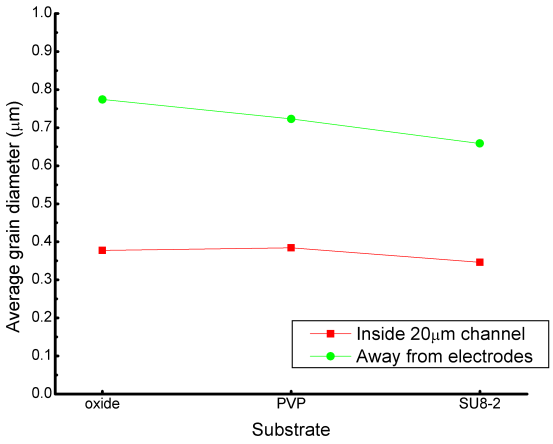
Figure 3.36 shows the results. Pentacene grains are smaller near Au and much larger away from Au, regardless of the types of the surfaces.

For these measurement results, one possible explanation is that there is trace amount of gold inside the channel that prohibits the grain growth of pentacene. However, this is ruled out by the measurement of energy dispersive X-ray spectroscopy (EDS/EDX). Figure 3.37 shows the result of EDS measurement, confirming that there is no gold inside the channel. This leads to a hypothesis that metal or at least gold can affect the grain growth of pentacene nearby.

Different Metals To further clarify whether other metals show the same effect as gold, the second series of experiments are performed. The second series of experiments is to investigate if other metals show the same suppressing effects as gold. All the samples use thermally grown silicon dioxide as substrates. First, silicon wafers are cleaned with piranha solution. 1000 Å



(a) Away and in-channel positions



(b) Grain diameter versus substrates

Figure 3.36: Pentacene grain diameter versus substrates.

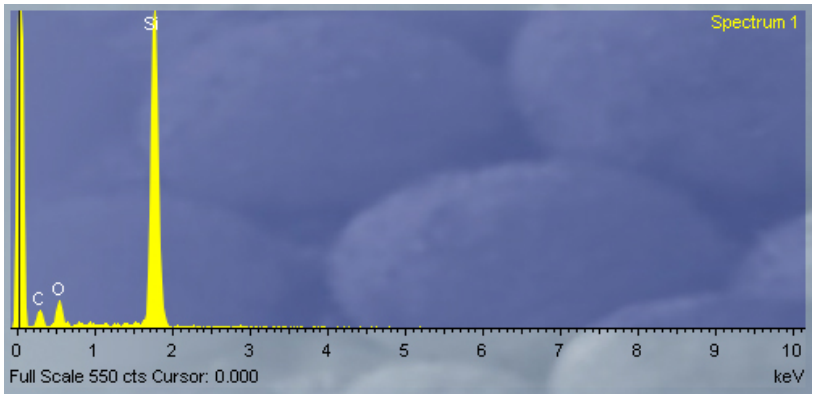
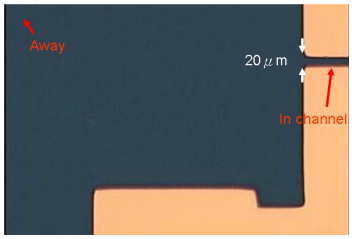


Figure 3.37: EDS spectrum inside the channel.

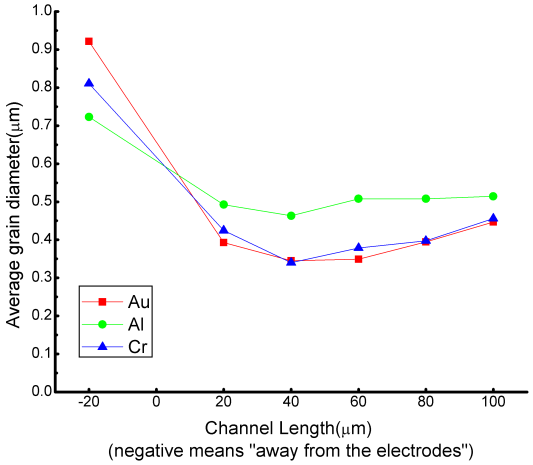
silicon dioxide is then grown in an oxidation furnace at 1050 °C. After oxidation, 500 Å gold, 500 Å chromium, and 500 Å aluminum are thermally evaporated through shadow masks. Again, photolithographic patterning processes are circumvented to prevent surface contamination of substrates.

Pentacene is then thermally evaporated at a rate of 0.1 Å/second under 10^{-7} Torr vacuum. During pentacene evaporation, all the samples are held at room temperature.

Figure 3.38 shows average pentacene grain diameters at positions "away" and "in-channel" of different channel widths for samples that have different metals but the same oxide substrates. Not only gold, but also aluminum and chromium show the suppressing effect. Grain sizes are larger at "away" positions than at "in-channel" positions, even when the channel width reaches 100 μm wide.



(a) Away and in-channel positions

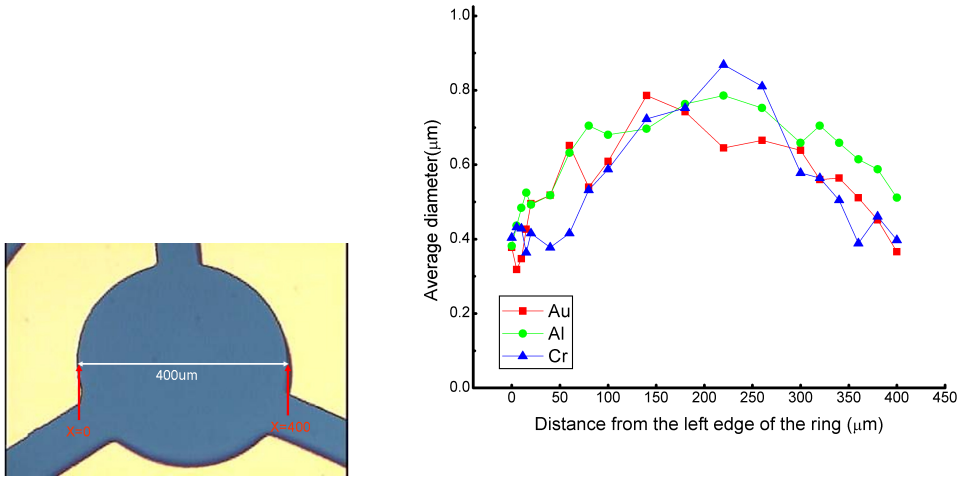


(b) Grain diameter versus channel lengths and metal types

Figure 3.38: Pentacene grain diameter versus channel lengths and metal types. (Negative values correspond to "away" positions.)

The channels used in this two series of experiments are rectangular, 20μm wide and 3000μm long. To eliminate the shape factors of metals, pentacene grain sizes across a circular region surrounded by different metals are measured. Figure 3.39 shows the microscopic picture of the circular region surrounded by metal, and the measurement results. The x-coordinate used

is also defined in Figure 3.39.



(a) The metal ring

(b) Grain diameter across the ring (from left to right)

Figure 3.39: Pentacene grain diameter across the ring made of different metals.

From these experiments, it is confirmed that pentacene grain growth is suppressed by metal nearby when pentacene is evaporated to substrates with metals. thin film pentacene transistors using bottom-contact configuration inevitably have smaller grains than those using top-contact configuration because bottom-contact configuration requires pentacene to evaporation onto substrates with metals. This is an additional support for the fact that thin film pentacene transistors with bottom-contact configuration have inferior performance.

The actual mechanism and theory behind these phenomena are still unknown. Development of models and theories are still underway to explain this suppressing effect of metal on pentacene grain growth.

3.4.8 Summary

In this section, key parameters influencing performance of thin film pentacene transistor, such as evaporation parameters, source/drain contacts, and surface roughness, are investigated in length. To have a thin film pentacene transistors with high performance, the gate insulator has

to be flat, spin-cast smoothing layer is needed, the source and drain contacts have to be thin and pure Au and the transistor has to use top-contact configuration.

3.5 Degradation of Thin Film Pentacene Transistors in Saline

One of the challenges that bio-implantable electronics face is the long-term reliability of the electronics immersed in the corrosive body fluids. Here, saline soaking is employed to evaluate long-term reliability and stability of the thin film pentacene transistors.

3.5.1 Degradation Mechanisms

The saline solution is 0.9 % w/v solution of sodium chloride with approximatedly 300 mOsm/L. Therefore, degradation of transistors can result from such agents as sodium ions, chloride ions, water and oxygen. Different agents could elicit degradations of transistors with different mechanisms. Meanwhile, the degradation of the transistors also depends on the material properties of the semiconductor the transistors use.

Sodium Ions Sodium ions mainly cause the changes of the threshold voltages of the transistors. Sodium ions go through the protective encapsulation layer and might causes short circuits when these ions stay inside the transistor channels. More significantly, sodium ions may be trapped within the gate insulating dielectric layer and change the threshold voltages of the transistors.

Chloride Ions Chloride ions are known as notorious culprits of many metal corrosions. The presence of chloride ions accelerates corrosion of metal immersed in water in an autocatalytic manner. The metal first is oxidized into positive metal ions. For charge neutrality, negatively charged chloride ions become concentrated at the corrosion site and form metal chloride compounds. Subsequently, water reacts with the metal chloride compounds and creates metal hydroxide, hydrogen ions, H^+, and chlorides. Now, the corrosion site becomes weakly acidic,

which in return accelerates the corrosion process. These chemical reactions are describe in the following reaction equations and Figure 3.40 depicts the corrosion process.

$$
\begin{aligned}
M &\rightarrow M^{n+} + ne^{-} \\
O_2 + H_2O + 4e^{-} &\rightarrow 4OH^{-} \\
M^{n+} \cdot (Cl^{-})_n + H_2O &\rightarrow M(OH)_n + H^{+} + Cl^{-}
\end{aligned}
$$

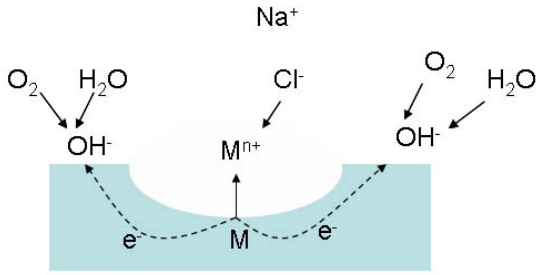


Figure 3.40: Metal corrosion in saline solution.

Oxygen Oxygen has a great influence on the electrical properties of the thin film pentacene transistor. Theories and calculations have revealed that oxygen readily forms stable chemical bond with the middle benzene ring of pentacene and pentacenequinone is generated as a result [86]. This molecule can become a scattering or trapping sites for charge carriers in the transistor channels and thus affect the performances of the transistor by reducing the on-current or mobility and the on-off ratio and by changing the threshold voltages.

Water Unlike other in-air applications such as organic LED and flexible displays, this implantable thin-film transistor has to stay in the saline solution or body fluids all the time. That is, the surface concentration of water of this device is much higher than that of in-air devices, which is only the humidity in air. Therefore, the process of water permeation is much more significant in the degradation of the transistors. Water molecules can dissociate and attach

to the grain boundaries of the pentacene thin film and to the dielectric interfaces due to electric fields induced by the operating voltages applied at the source/drain and the gate. On the ground boundaries, water molecules create trapping states and potential barriers and decrease mobility of charge carriers. In addition, water molecules can also cause drifts of threshold voltages when they accumulated at the dielectric interface.

3.5.2 Experimental and Results

To evaluate the bio-reliablity of the thin-film transistors, saline soaking tests are carried out. The thin film pentacene transistors are fabricated by the process described in § 3.3.2. After fabrication, these transistors are soaked in saline solution at room temperature. Figure 3.41 shows the transistors immersed in saline solution.

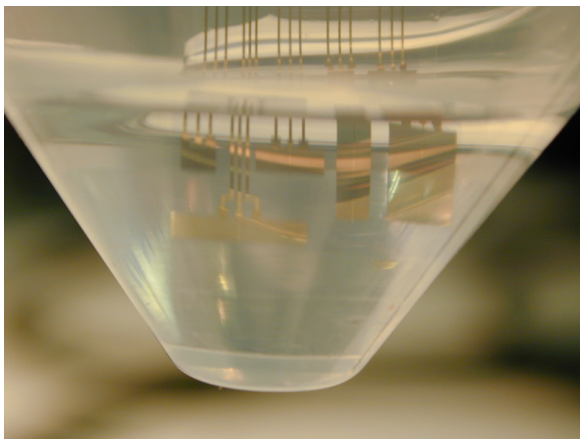


Figure 3.41: The thin film pentacene transistors immersed in saline solution.

Field effect mobility is monitored over a fixed period of time. Figure 3.42, Figure 3.43, and Figure 3.44 show mobility changes over time of the pentacene transistors encapsulated with 1 μm, 10 μm, and 20 μ Parylene C. The field effect hole mobility decays slower when Parylene thickness increases. After one hundred days, the field effect mobilities of the pentacene transistors encapsulated with 1 μm, 10 μm, and 20 μm Parylene C drop to 10 %, 30 %, and 30 % of initial values, respecitvely. Although 30 % seems like an okay value, the resulting field effect mobility is not high enough for any kind of application, since the initial mobility is low already.

Meanwhile, one hundred days at room temperature are too short a time for bio-implantable devices.

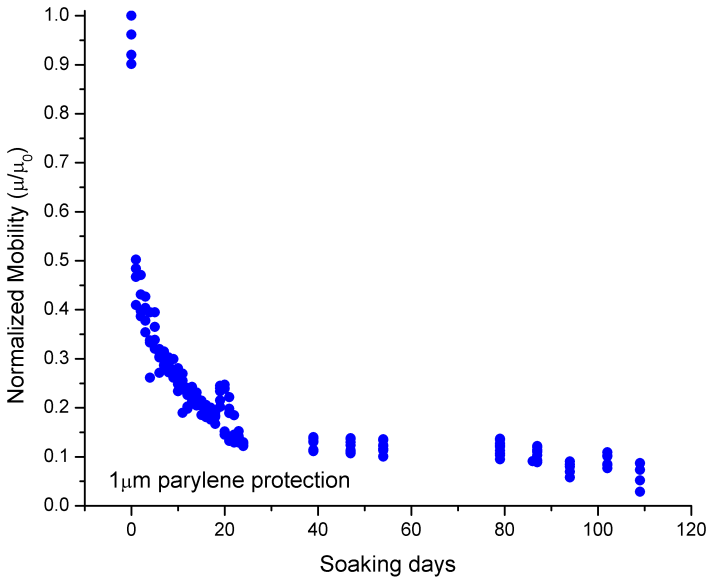


Figure 3.42: Evolution of the field effect mobility of thin film pentacene transistors soaking in room-temperature saline solution. 1-μm parylene C protection.

This shows only Parylene protection is not enough to ensure good encapsulation of thin film pentacene transistors. Unlike amorphous silicon, pentacene is sensitive to oxygen and moisture. Mobility of thin film pentacene transistors starts to drop in a few hours in air after fabrication if the devices do not have any kind of encapsulation. With Parylene coating, the device could last longer in air. But, for bio-implants, the devices are soaked in body fluids all the time. A better strategy of encapsulation, such as Parylene-metal-Parylene composite layers are needed to achieve reasonable performance and bio-reliablility.

3.6 Discussions and Future Work

Pentacene-thin-film transistors have been fabricated and their properties have been investigated in detail. This flexible thin-film transistor uses Parylene C as the substrate, the gate in-

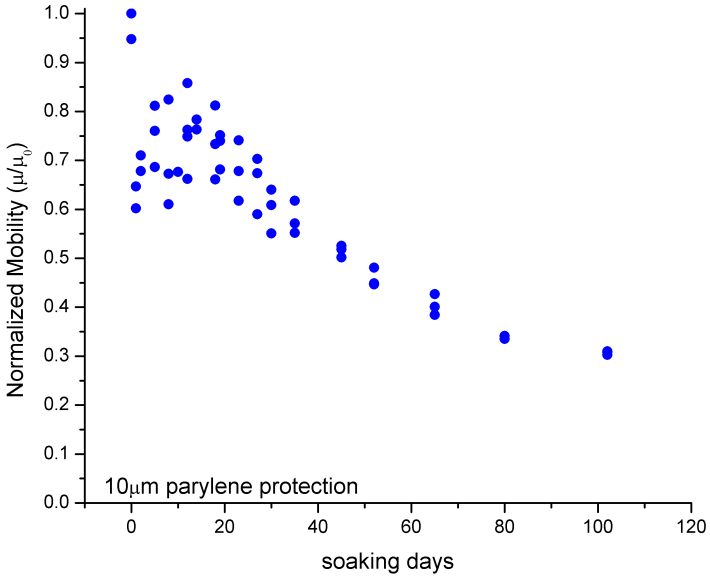


Figure 3.43: Evolution of the field effect mobility of thin film pentacene transistors soaking in room-temperature saline solution. 10-μm parylene C protection.

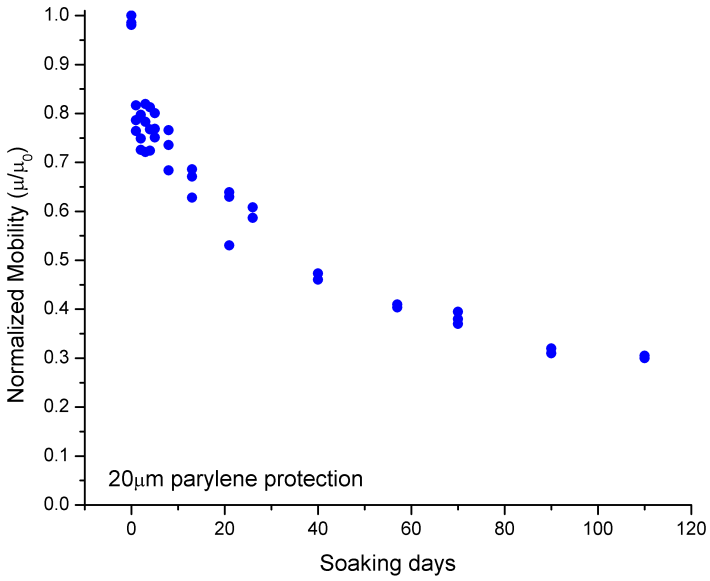


Figure 3.44: Evolution of the field effect mobility of thin film pentacene transistors soaking in room-temperature saline solution. 20-μm parylene C protection.

sulating dielectric, and the encapsulation layer. To achieve high performances of devices, the process paramaters have to be carefully controlled. The surface that pentacene is deposited on must be carefully prepared. Top contact structures make the transistors better but complicated the fabrication processes. For bioimplantation applications, pentacene transistors need special protections from water, oxygen and other corrosive agents in the body fluids. Parylene C along does not provide sufficient protection. Complex protection paradigms, such as Parylene-metal composite layers, have to be developed before bio-implantable systems made of thin film pentacene transistors can be used in real applications.

Chapter 4

Thin Film Silicon for Implantable Electronics

As can be seen from previous chapters, thin film pentacene transistors degrade fast when immersed in saline solution. This is mainly because pentacene is sensitive to water and oxygen. Pentacene degrades fast in air, not to mention soaking in saline solutions. As a result, we turn to thin film silicon since silicon does not degrade as fast as pentacene. This chapter discusses development of thin film silicon implantable electronics. Deposition processes of amorphous silicon are investigated in detail and the fabrication process of thin film amorphous silicon transistors is developed. Saline soaking tests are carried out to evaluate long-term reliability of thin film silicon transistors.

4.1 Flexibility of Thin Film Silicon

Before investigation of thin film silicon transistors, the flexibility of thin film silicon has to be examined. Intuitively, silicon is rigid and not flexible. But, in fact, thin silicon can be very flexible. In the following section, the relation between thickness and flexibility is studied. For elastic solids, the flexibility can be estimated by the radius of curvature. The curvature-strain relation is given by Equation 4.1 and the bending is depicted in Figure 4.1

$$\epsilon = \frac{y}{\rho}, \tag{4.1}$$

where ϵ is the strain, y is the distance from the neutral axis and ρ is the radius of curvature.

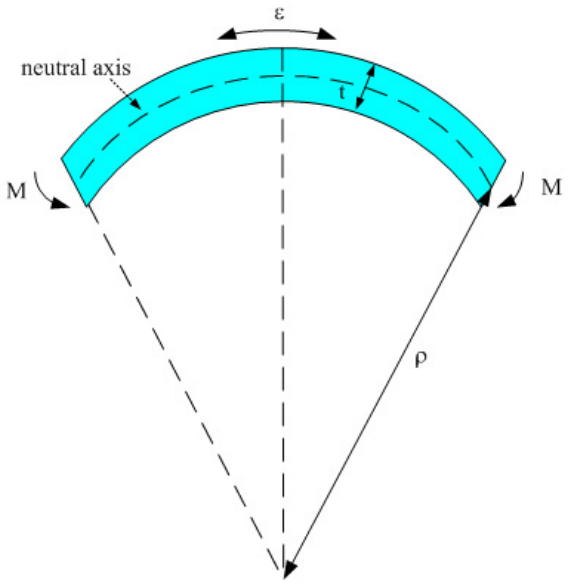


Figure 4.1: Illustration of a solid under bending moment.

For silicon chips or thin films, the neutral axis can be assume to be the middle of the solid. Therefore, the surface strain, or the maximum strain of silicon solid is given by Equation 4.2

$$\epsilon = \frac{t}{2\rho}\,, \tag{4.2}$$

where t is the thickness of the silicon solid.

Tai *et al.* studied fracture strains of thin film polysilicon with the help of surface micromachining techniques [87]. They reported a fracture strain of polysilicon of 1.72 %. From the same paper, it is found that the maximum fracture strain of single crystal silicon is approximately 2.6 %. Using these numbers, radii of curvatures of typical amorphous/polycrystalline silicon and single crystall silicon dies can be calculated. Table 4.1 shows the radii of curvature of thin film silicon and single crystal silicon dies of typical thickness.

The minimum radius of curvature of thin film silicon before fracture occurs is twenty times as small as that of silicon chips. Figure 4.2 depicts two arcs with two radii, one of which is twenty times as large as the other. As can be seen from this figure, the twenty times of difference of

Table 4.1: Radii of curvature of silicon.

Silicon Types	Single Crystal Die	Thin Film[1]
Fracture Strain	2.6 %	1.72 %
Thickness	250 μm	0.5 μm
Radius of Curvature	4807 μm	14.5 μm

[1] Polycrystalline and amorphous silicon

radii of curvature can result in enormous differences in terms of flexibility. Figure 4.3 shows bending of a silicon chip of 250 μm encapsulated with Parylene and a thin film amorphous silicon encapsulated with Parylene.

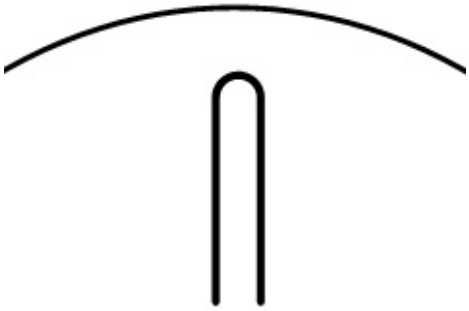


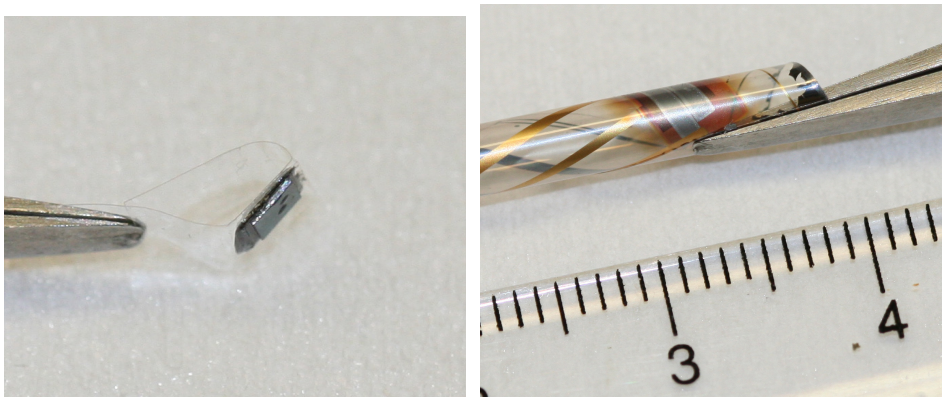
Figure 4.2: Two arcs with radii of curvature of 20× differences

As can be seen, thin film silicon can be very flexible and its radius of curvature can be as small as 14.5 μm before any fracture occurs.

4.2 Material

4.2.1 Process Equipment and Limitation

The development of thin film silicon implantable electronics is limited by the facilities of the Caltech Micromaching Lab. And limited by the temperature constraint of the polymer substrates, only PECVD processes and room-temperature deposition processes, such as sputtering, are the candidates for deposition of thin film silicon. For thin-film depositions (metal and silicon), the Caltech Micromaching Lab has the e-beam evaporator, the thermal evaporator and the



(a) silicon chip (b) thin film silicon

Figure 4.3: Bending of a silicon chip and thin film amorphous silicon.

PECVD processing equipment. For thin film silicon deposition, only a PECVD process equipment is available in the Caltech Micromaching Lab and there is no sputtering equipment available. Meanwhile the gases available to the PECVD process equipment are silane and ammonia. No phosphine, hydrogen, nor diborane is available. In short, with the current facilities at the Caltech Micromaching Lab, only amorphous silicon and silicon nitride are available. But with these limited capabilities, a lot of work can be done and valuable information can be obtained.

4.2.2 Amorphous Silicon and Silicon Nitride

Amorphous silicon (a-Si) is the non-crystalline allotropic form of silicon. Silicon is a four-fold coordinated atom that is normally tetrahedrally bonded to four neighboring silicon atoms. In crystalline silicon this tetrahedral structure is continued over a large range, forming a well-ordered lattice (crystal). In amorphous silicon this long range order is not present and the atoms form a continuous random network. Not all the atoms within amorphous silicon are four-fold coordinated. Due to the disordered nature of the material some atoms have dangling bonds. These dangling bonds are defects in the continuous random network, which cause electrical behaviour.

In unhydrogenated amorphous silicon, there are a large number of dangling bonds, typically around 10^{19} – 10^{20} cm^{-3}. However, the addition of hydrogen significantly reduces this such

that a high quality a-Si:H can have defect density as low as 10^{16} cm^{-3}. The hydrogen passivates the defects by forming a Si-H bond where the dangling bond would have been. Therefore as the hydrogen content of a-Si:H increases, the number of dangling bonds is reduced. Hydrogenated amorphous silicon of device quality usually has hydrogen content of 10%. Hydrogen is provided by either the products of the LPCVD and PECVD processes or addition of hydrogen gas during deposition.

Table 4.2 summarizes properties of device-quality a-Si:H.

Table 4.2: Properties of device-quality a-Si:H.

Activation Energy of Conduction	0.7 – 0.8 eV at 300K
Dark Conductivity	10^{-11} – 10^{-10} S cm^{-1}
Defect Density	10^{16} cm^{-3}
Electron Mobility	0.5 – 1 cm^2/Vs
Hole Mobility	0.001 – 0.02 cm^2/Vs
Hydrogen Content	5 – 15%[1]
Refractive Index	4.3

[1] percentage of numbers of atoms.

Almost all commercial TFT LCDs use thin-film transistors with amorphous silicon nitride as the gate insulating dielectric. The most wide-spread deposition method for amorphous silicon nitride is PECVD. The deposition sources are usually silane, ammonia and nitrogen. Silicon nitride has an amorphous structure and its properties depend on the relative atomic concentrations of silicon, nitrogen and hydrogen. For a-Si:H thin-film transistors of good electrical quality, PECVD deposited SiN_x is much more suitable than stoichiometric Si_3N_4. Silicon nitride deposited at 300 – 350 °C is quite a different material from Si_3N_4 produced by CVD at 700 – 900 °C.

Hydrogen in SiN_x passivates the traps and dangling bonds as in the case of a-Si:H. The defect density of SiN_x:H is therefore much less than that of CVD Si_3N_4. The interface charge density between a-Si:H and SiN_x:H is typically in the range of 2×10^{11} to 7×10^{12} $eV^{-1}cm^{-2}$, and it strongly depends on the deposition conditions: it increases with decreasing substrate temperature or decreasing RF power.

The ability to form good insulating film at low temepratures (< 350 °C) having a low interface state density with a-Si:H makes SiN_x:H a good gate insulating dielectric.

Table 4.3 summarizes properties of device-quality SiN_x:H.

Table 4.3: Properties of device-quality SiN_x:H.

Breakdown Voltage	10^7 V/cm
Hydrogen Content	< 25 %[1]
Dielectric Constant	7.5
Refractive Index	1.9 – 2.05
Resistivity at 300K	10^{10} Ωcm

[1] percentage of numbers of atoms.

4.2.2.1 Preparation of Amorphous Silicon and Silicon Nitride

When it comes to deposition of amorphous silicon, several methods are available: e-beam evaporation, sputtering, and PECVD processes. Sputtering is out of the question due to lack of facilities.

The lack of hydrogen gas renders e-beam evaporation not feasible. Silicon, deposited in a hydrogen-free environment, by sputtering or e-beam evaporation, has around 0.1 % of broken Si-Si bonds and this small fraction of broken bonds results on a density of electronic defects in the range of 10^{19} cm^{-3}. That is sufficient to kill any semicondutoring property. The workaround is supplying hydrogen in the deposition chamber or in post-process-annealing to amend the broken bond by forming Si-H. This could lower resulting electronic defect density to the 10^{16} cm^{-3}.

Therefore, we turn to the PECVD process for amorphous silicon preparation. It is desirable to lower the process temperature to accommodate plastic substrates and much work has been done to lower the process temperatures of PECVD silicon and silicon nitride. The key factor is to increase hydrogen content within deposited silicon/silicon nitride films. This is done by using hydrogen-diluted silane [17] [20] [88] [89] [90] or introducing hydrogen in the process chamber [91]. Or it is achieved by post-depostion processes, such as hydrogen plasma treatment [92] or

post-process annealing [93].

The deposition of amorphous silicon is done with the Technics Micro PD series 900, a one-chamber PECVD equipment. Figure 4.4 shows the RF matching network, the 13.56MHz RF generator and the processing unit.

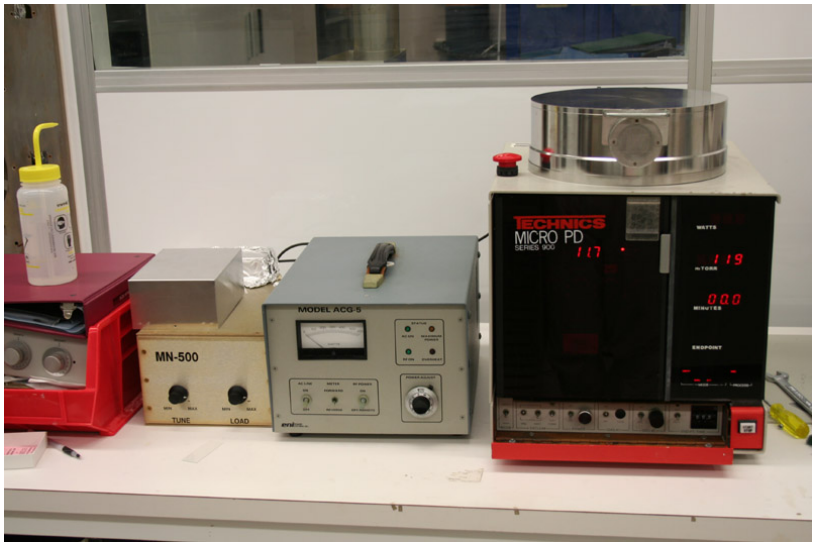


Figure 4.4: The PECVD process equipment, from left to right: the RF matching network, the 13.56 MHz RF generator and the processing unit.

Considering the current capability of the Caltech Micromaching Lab, post-process annealing in forming gas (5 % hydrogen and 95 % nitrogen) is employed to increase the hydrogen content and lower broken Si-Si bond density and thus device defect density.

For silane supply, two choices are available: pure silane and 5 % silane diluted in nitrogen. Figure 4.5 shows the EDS spectrums of PECVD amorphous silicon made out of 5 % silane diluted in nitrogen on the oxide wafer and Table 4.4 shows the content of nitrogen, oxygen and silicon. The nitrogen content of such amorphous silicon film is close to 10 % and thus render this film not semiconducting.

Meanwhile, the amorphous silicon film made out of pure silane shows no traces of impurity.

The deposition of silicon nitride is done in the PD900. The supply gases are ammonia and silane. No hydrogen nor nitrogen is added in the deposition processes.

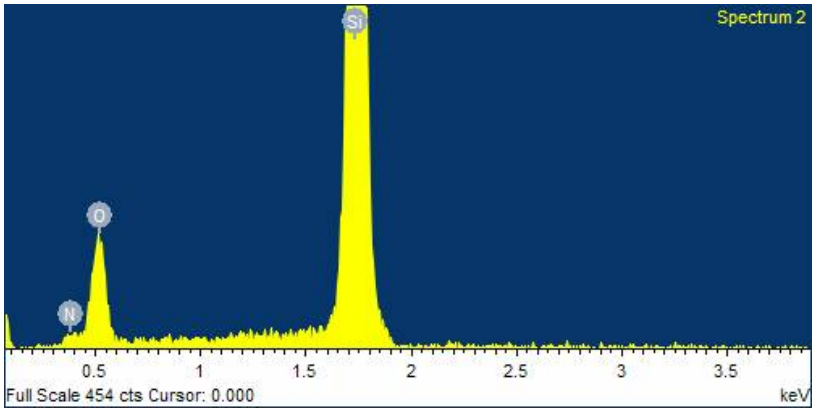


Figure 4.5: EDS spectrum of amorphous silicon on the oxide wafer, made out of 5 % silane diluted in nitrogen.

Table 4.4: Content of amorphous silicon on the oxide wafer, made out of 5 % silane diluted in nitrogen.

Element	Weigth %	Atomic %
N	5.81	9.60
O	20.33	29.45
Si	73.86	60.94

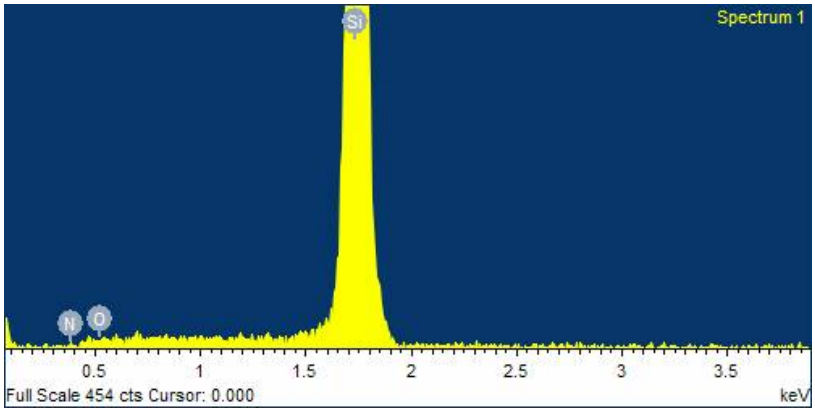


Figure 4.6: EDS spectrum of amorphous silicon on the silicon wafer, made out of pure silane.

Table 4.5: Content of amorphous silicon on the silicon and oxide wafer, made of pure silane.

On the oxide wafer

Element	Weigth %	Atomic %
N	0.09	0.16
O	14.96	23.58
Si	84.95	76.26

On the silicon wafer

Element	Weigth %	Atomic %
N	0.00	0.00
O	0.56	0.98
Si	99.44	99.02

4.2.3 Parylene HT®

Recently, a new variant of Parylene, Parylene HT® is introduced by Specialty Coating Systems. Parylene HT® replaces the alpha hydrogen atom of the parylene N dimmer with fluorine. Parylene HT® is useful in high temperature applications (short-time up to 450 °C). This unique high-temperature capability of Parylene HT® paves the way toward thin film amorphous silicon transistors.

The detailed properties and deposition process of Parylene HT® can be found in § B.1.

4.2.4 Metal

The metal used in development of thin film amorphous silicon transistors are common metals used in the MEMS field, such as Au, Cr, Pt, Al and Ti. We choose Au/Cr and Au/Ti as the metal interconnections and gate metals. These metals are deposited with e-beam evaporation and thermal evaporation.

Source And Drain Contacts A typical thin film amorphous silicon transistors have n^+ or p^+ regions to form ohmic contact with source/drain metals. These regions are formed by either ion-implantation after deposition of amorphous silicon or adding additional n^+ or p^+ amorphous silicon by PECVD process. The PECVD n^+ and p^+ amorphous silicon depositions require special gases of phosphine and diborane, respectively. Due to the lack of such gas

supply and the lack of ion-implantation capability, Al is selected as the source/drain metal since Al can form ohmic contact with silicon easily after proper post-process annealing.

In order to form ohmic contact between Al and amorphous silicon and to amend broken Si-Si bonds with hydrogen, a post-process annealing at 300 °C in forming gas (5 % hydrogen and 95 % nitrogen) is carried out.

4.3 Development of In-House Thin Film Amorphous Silicon Transistors

To implement a thin film amorphous silicon transistor, several process steps have to be investigated and established. The general process of thin film amorphous silicon transistors can be broken into the following steps:

1. Deposition of Sacrificial Layers
2. Deposition of Parylene HT®
3. Deposition and Patterning of the Gate Metal
4. Deposition and Patterning of the Gate Insulator
5. Deposition and Patterning of Amorphous Silicon
6. Deposition and Patterning of the Al Source And Drain Contacts
7. Forming Gas Annealing
8. Deposition and Patterning of Metal Interconnects
9. Deposition of Parylene as Protection Coating
10. Releasing of Amorphous Silicon Transistors

The detailed processes and problems are discussed in the following sections.

4.3.1 Tuning the Amorphous Silicon Deposition Process

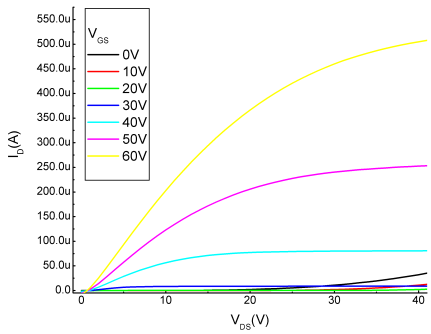
First, the properties of PECVD amorphous silicon films are investigated. A thin-film transistor is made using the silicon wafer as the gate, thermally-grown oxide as the gate insulating dielectric, PECVD amorphous silicon as the semiconductor, and Al as the source/drain contact. A post-annealing in forming gas is performed after fabrication of the transistors. The undoped amorphous silicon has bipolar behaviors. That is, it can act as a p-channel transistor and an n-channel transitor at the same time. However, the p-channel transisor has much worse performance than the n-type counterpart and the undoped amorphous silicon is more an n-channel transistor than a p-channel one. This dual behavior mainly stems from the lack of heavily-doped source/drain.

Figure 4.7 shows the drain characteristics and the characteristics of the amorphous silicon transistors and Table 4.6 lists properties of the amorphous silicon transistors.

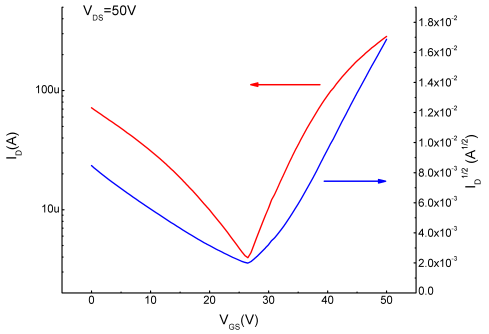
Table 4.6: Properties of the undoped thin film amorphous silicon transistor.

Properties	**n-channel**	**p-channel**
Gate	Silicon	Silicon
Gate Dielectric	1860 Å Oxide	
W/L	3000/60	
a-Si	PECVD 250 °C, 1000 Å	
S/D metal	1000 Å Al	
Annealing	350 °C, forming gas, 20 hours	
Mobility (cm^2/Vs)	1.183 (electron)	0.167 (hole)
Threshold Voltage (V)	26.98	-22.03
On/Off Ratio	10^3	10^3

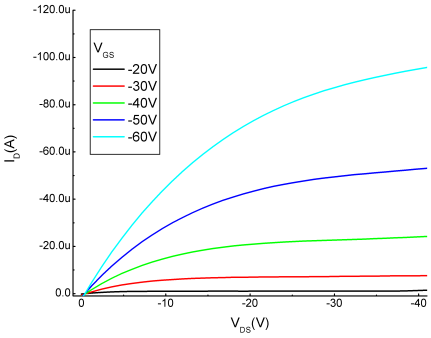
As can be seen, the undoped amorphous silicon acts more like an n-channel transistor than a p-channel transistor. One major problem with such an undope amorphous silicon is the low on/off ratio and high threshold voltages. High threshold voltages results mainly from the trapped charges between oxide and PECVD amorphous silicon due to exposure of plasma of the PECVD process.



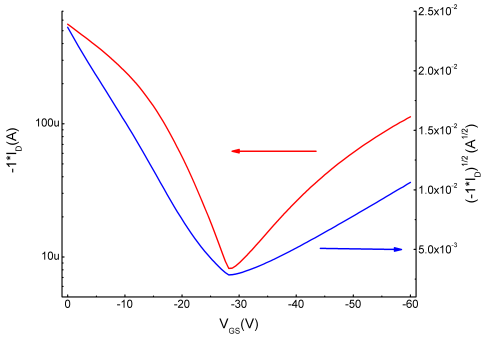
(a) n-channel Drain Characteristics



(b) n-channel Gate Characteristics



(c) p-channel Drain Characteristics



(d) p-channel Gate Characteristics

Figure 4.7: The drain and gate characteristics of undoped thin film amorphous silicon transistor on oxide.

4.3.2 Choosing the Gate Insulating Dielectric

Commonly, thin film amorphous silicon transistors use amorphous nitride as the gate insulating dielectric. In order to obtain optimal transistors, other materials are also tested. In addition to amorphous silicon nitride, Parylene C, Parylene N and Parylene HT® are used as the gate insulating dielectrics. The testing transistors are fabricated on glass wafers. The testing transistors use Au/Cr as the gate metal, the above materials as the gate insulating dielectrics. Table 4.7 lists resulting electron field effect mobilities of the aforementioned thin film amorphous silicon transistors.

Table 4.7: Electron field effect mobilities of thin film amorphous silicon transistors with Parylene as gate dielectrics.

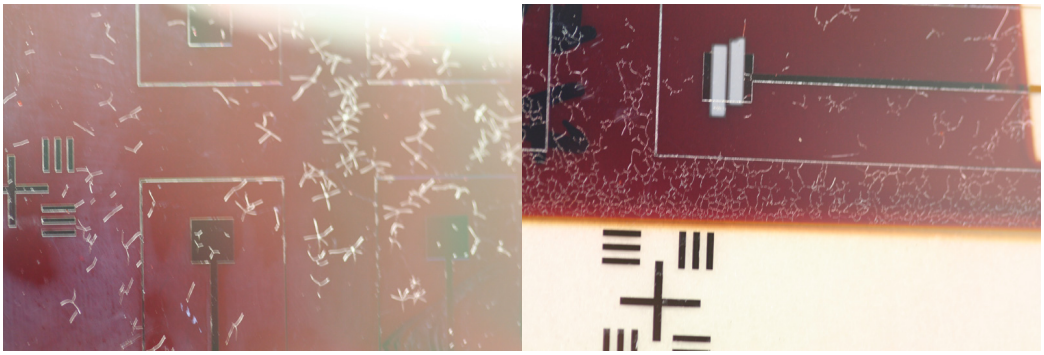
Gate Dielectrics	Thickness	Dielectric Constant	Electron Field Effect Mobility (cm^2/Vs)
Parylene C	1450 Å	3.10	N.A.[2]
Parylene D	N.A.[3]	2.82	N.A.[3]
Parylene N	6758 Å	2.65	0.37
Parylene HT®	4903 Å	2.20	0.27

[1] PECVD amorphous silicon is deposited at 250 °C.
[2] All transistors with Parylene C failed due to high process temperature.
[3] No transistors can be made due to difficulty of thickness control of parylene D deposition.

Although amorphous silicon transistors can be successfully made on Parylene N surfaces, cracks develop on the Parylene N right after the 250 °C PECVD processes. Figure 4.8 shows cracks on Parylene N and D after the 250 °C PECVD processes. No cracks appear on Parylene HT®.

Although transistors with Parylene HT® as the gate insulating dielectric show decent performances, the dielectric constant of Parylene HT® is way too small, only 2.2. In fact, the low dielectric constant makes Parylene HT® an excellent inter-metal dieletric material for VLSI applications.

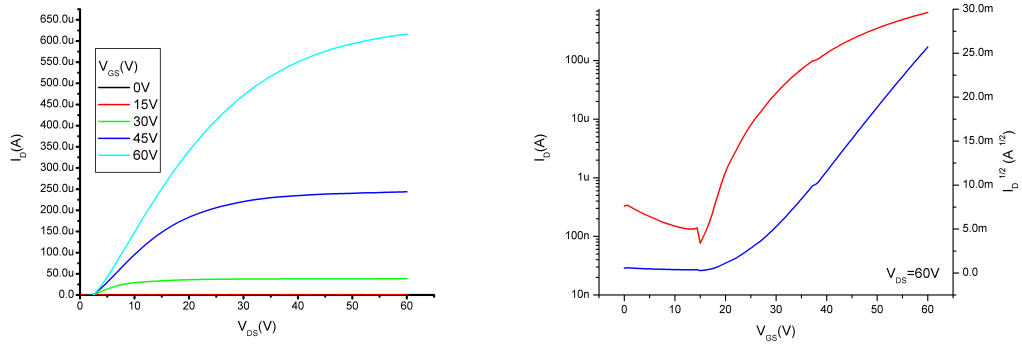
Meanwhile, amorphous silicon nitride has high dielectric constant, usually around 6 to 9 and it can be easily deposited with the available PECVD amorphous silicon process. In fact, most of amorphous thin-film transistors use amorphous silicon nitride as gate dielectric.



(a) Parylene D (b) Parylene N

Figure 4.8: Cracks of Parylene N and D after 250 °C PECVD processes.

Thin film amorphous silicon transistors are made on silicon wafers with silicon as gate, PECVD amorphous silicon nitride as gate dielectric. Figure 4.9 shows the gate characteristics and drain characteristics of the thin-film transistor, and Table 4.8 summarizes properties of the thin-film transistors.



(a) The drain characteristics (b) The gate characteristics

Figure 4.9: the gate characteristics and drain characteristics of the thin-film transistor with gate dielectric of amorphous silicon nitride.

4.3.3 Lifting off the Transistor Film

Now, we can build thin film amorphous silicon transistors with gate dielectric of amorphous silicon nitride on Parylene HT® films. A common process flow of Parylene liftoff technology

Table 4.8: Properties of the thin-film transistor with gate dielectric of amorphous silicon nitride.

Gate	Silicon
Gate Dielectric	300 °C PECVD nitride
Gate Dielctric Thickness	2000 Å
Source/Drain Metal	1000 Å Al
W/L	3000/60
Electron Mobility	0.7 cm^2/Vs
Threshold Voltage	23.42 V
On/Off Ratio	10^4

starts with coating the mechanical substrates, usually silicon wafers. After completing all fabrication processes, the Parylene C film is lifted off from the substrate via either dissolving sacrificial photoresists or mechanically lift-off. However, such techniques can never be applied to fabrication of thin film amorphous silicon transistors due to the plasma processes involved. Common photoresists cannot stand the process temperatures of the PECVD processes.

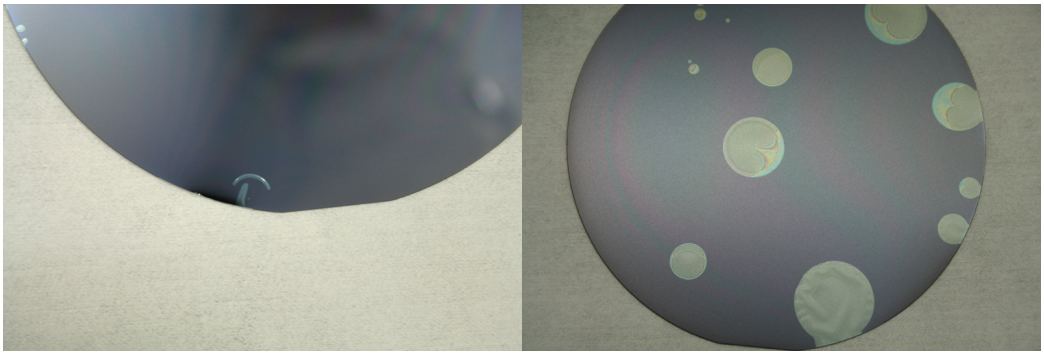
4.3.3.1 Poor Adhesion of Parylene HT®

From our past experiences, Parylene C has poor adhesion to silicon surface and extreme poor adhesion to hydrophilic surfaces, for example oxides. Deposition of Parylene C on oxide surfaces is always preceded by a step of adhesion promotion. A common adhesion promotor is A-174, which is a gamma methacryloxy propyltrimethyoxysilane.

Parylene HT® shows even poorer adhesion than Parylene C to either of silicon and oxide surfaces. Without any adhesion promotion, bubbles occur immediately after deposition of Parylene HT®, as shown in Figure 4.13. Thus, Parylene HT® cannot be processed in the same way as Parylene C (directly lifting off from a silicon wafer). Both sacrificial layers and adhesion promotion are necessary.

4.3.3.2 Metal as the Sacrificial Layer

The sacrificial layer must stand high temperatures up to 310 °C, the temperature of PECVD processes. Common photoresists are not qualified for this job due to the high temperature



(a) Front (b) Back

Figure 4.10: Delimination and bubbles of Parylene HT® on oxide immediately after Parylene deposition.

constraint. It is natural to try metal as the high temperature sacrificial layer.

A 1000 Å Cr layer is tested as the sacrificial layer. Silicon wafers are first cleaned by general cleaning procedures. Next, 1000 Å Cr is deposited on the silicon wafer. A-174 adhesion promotion is carried out before Parylene HT® coating. Then, 10 μm Parylene HT® is deposited. Finally, a-Si:H and SiN_x are deposited via PECVD processes at 310 °C. No transistors are made on the testing samples. After the PECVD processes, wafers are immersed in Cr-7, a common Cr etch from Transene.

However, the Parylene HT® film cannot be lifted off from the wafers after soaking in the Cr-7 for more than a week. A step-by-step process examination is done, as show in Table 4.9, and it is the plasma step that makes it impossible to release the Parylene HT® films. This effect not only happens to Cr but also to oxide sacrificial layers.

This effect might result from the fact that Parylene HT® is an excellent electret material and that the plasma in PECVE processes inevitably implants charges on the Parylene HT® film. Figure 4.11 shows the surface potential of Parylene HT® after the 310°C PECVD nitride process.

4.3.3.3 High-Temperature Photoresist as the Sacrificial Layer

Removing metal sacrificial layers requires metal etchants. Most of the etching mechanism of metal etchants depends on the negative ions of acids or oxidizing agents. The charges

Table 4.9: Process isolation: The PECVD processes make it impossible to release the Parylene HT® with metal sacrificial layers.

Substrates	Sacrificial Layer	A-174 Treatment	300 °C Heating	300 °C PECVD	Releasing
oxide	Cr	x		x	no
oxide	Cr	x	x		yes
oxide	none	x		x	no
oxide	none		x		yes
soda lime	Cr	x		x	no
soda lime	Cr	x			yes
silicon	Cr				yes
silicon	Cr		x		yes
silicon	Cr		x	x	no

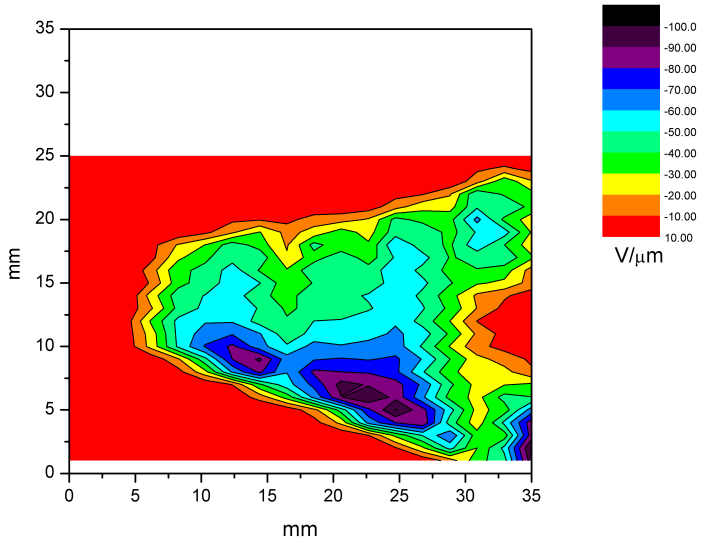


Figure 4.11: Surface potential of Parylene HT® after the 310°C PECVD nitride process.

implanted on the Parylene HT® film in the PECVD process might expel those negative ions away from the metal sacrificial layer beneath. Therefore, it is desirable to find a polymer sacrificial layer that is soluble in organic solvents. Thus no charged particles are involved in the releasing processes.

This polymer sacrificial layer must stand high temperatures of the PECVD processes up to 310 °C and must be able to be removed by organic solvents after the long high temperature processes. The PECVD deposition processes take around 30 minutes each time and the forming glass annealing is 24 hours long at 300 °C. These are harsh factors for a polymer sacrificial layer.

Polymethylglutarimide (PMGI) is chosen as the sacrificial layer because of its high temperature stability. PMGI is sold by MicroChem under the brand name of SF resists. Typically, PMGI is used as the underlying resist in bi-layer resist schemes because of its ability to produce a retrograde profile in lift-off processes. While PMGI is photosensitive, it has a significant unexposed development rate that allows PMGI to be used in applications without its own exposure step. PMGI does not intermix when used in combination with standard positive novolac resists. The glass transition temperature of PMGI is approximately 185 °C and it can be planarized at temperatures between 250 – 290 °C. PMGI is stable up to approximately 325 °C and therefore allows processes of higher temperatures than standard resists.

PMGI can be removed by tetramethyl ammonium hydroxide (TMAH), such as Shipley Microposit Developer CD26 (0.26 N) or N-methylpyrrolidone (NMP)-based photoresist stripper, for example ST-22 from ATMI.

The process using PMGI as the sacrificial layer starts with an oxide wafer. PMGI SF6 resist is spun onto the wafer (1k rpm, 40 seconds) and baked in a convection oven at 200 °C for 2 hours. 15 μm Parylene HT® is next deposited onto the wafer. 2000 Å Al is deposited via thermal evaporation and patterned as the gate electrode. Nitride and amorphous silicon films are deposited via PECVD. The processing temperature is lowered to 250 °C. The wafer looks fine after the PECVD processes. No wrinkles or cracks appear. Then, 1500 Å Al is deposited and patterned as the source and drain. 5 μm Parylene C is sequently deposited as the protection

coating.

Finally, the transistor film is released by immersing the wafer in 120 °C ST-22 solution. It takes 24 hours to completely release the Parylene HT® film. Figure 4.12 shows the transistor film.

Note that no forming gas annealing is carried out in this trial process.

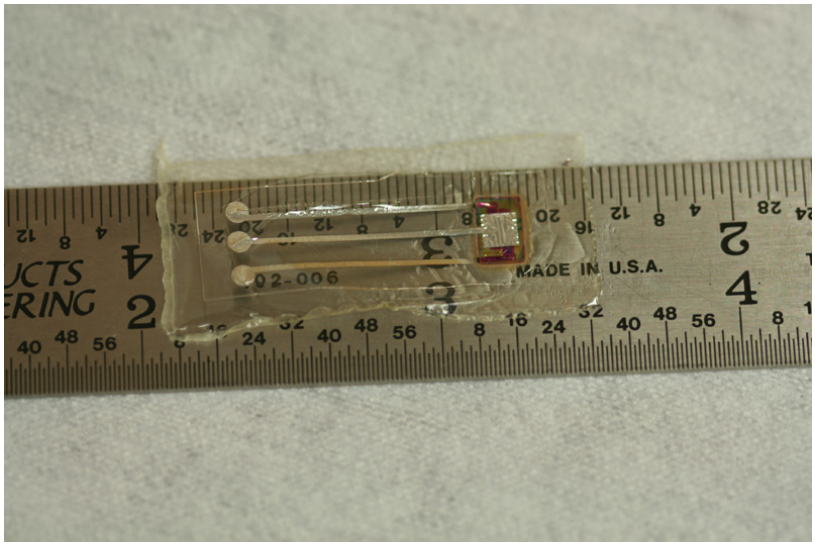


Figure 4.12: The thin film amorphous silicon transistor, lifted off with SF6 sacrificial layer.

Though the transitor shown in Figure 4.12 looks okay, it does not work. It is mainly because the low temperatures of the PECVD processes and the lack of forming gas annealing.

In addition to this problem, serious delamination between the two layers of Parylene occurs after the long and high-temperature releasing processes. Figure 4.13 shows the broken transistor film.

4.3.3.4 No Sacrificial Layer

In addition to polymer sacrificial layers, we also try fabricating the transistors without any sacrificial layers. The fact that the adhesion of Parylene HT® to silicon is a little bit better than that to oxide is exploited in this process.

This trial process start with dipping the silicon wafer in diluted HF solution to remove native

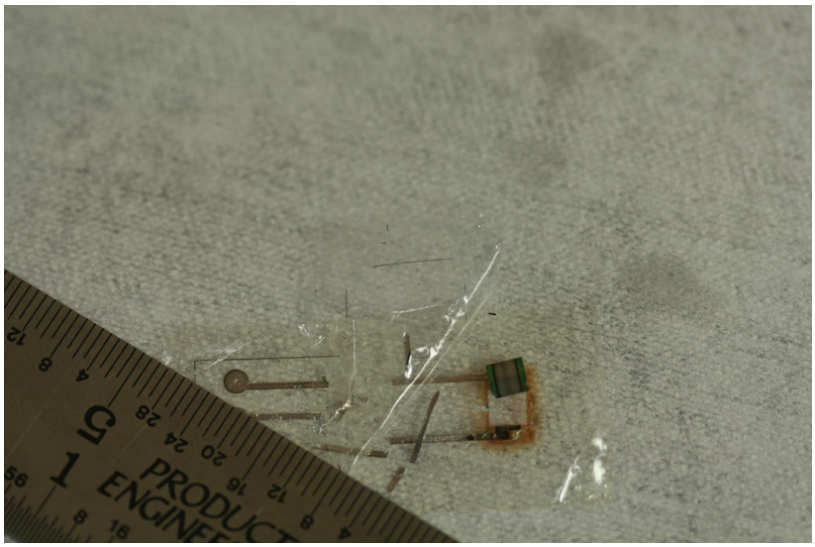


Figure 4.13: Delimination after soaking in ATMI ST-22 120 °C.

oxide. Next, 15 μm Parylene HT® is deposited. Because of the lack of native oxide, the adhesion of Parylene HT® to silicon is good enough to complete the process. After deposition of Parylene HT®, 1500 Å Al is deposited and patterned as the gate metal. Nitride and amorphous silicon is next deposited via PECVD at 310 °C. 1500 Å Al is subsequently deposited and patterned as the source and drain. Then, 300 °C forming gas annealing is carried out.

Upon completion of this process, the Parylene HT® film is manually lifted off from the wafer. Figure 4.14 shows the released Parylene HT® film. Although the transisors work well, the manual lift-off leaves a lot of wrinkles and stress marks on the Parylene HT® film. A better approach has to be developed.

4.3.3.5 Silicon Back Etching

After numerous trials and errors, we resort to the tranditional MEMS technique to solve the releasing problem, the silicon back etching. After fabricating transistors on the Parylene HT® with adhesion promotion, the substrate silicon is etched away by MEMS silicon etching processes.

The etching process used here is the hydrofluoric acid – nitric acid – acetic acid (HNA) etching system because of its fast and controllable etching rate. The silicon etching rate of the HNA

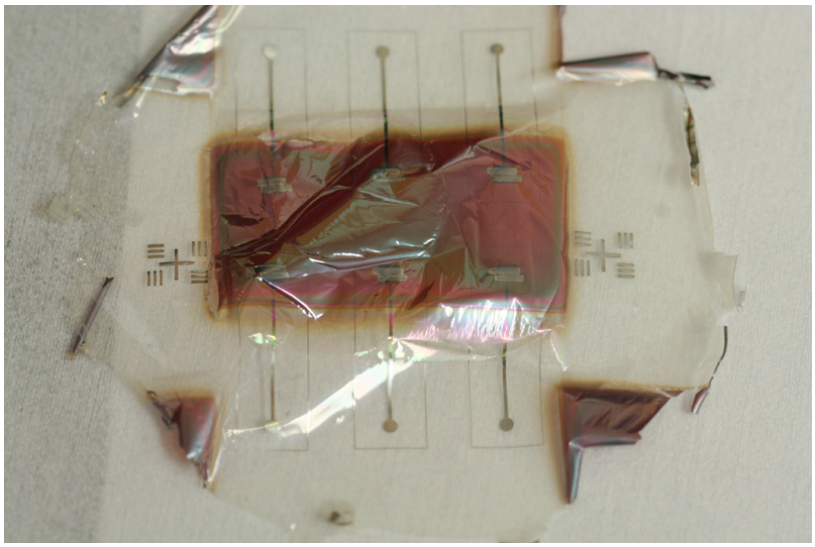


Figure 4.14: The transistor film, manually lifted off without sacrificial layers.

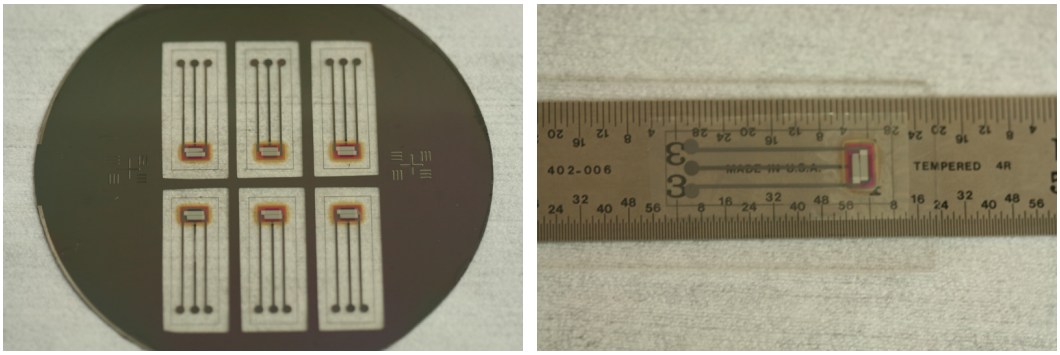
system is determined by the ratios of hydrofluoric acid, nitric acid and acetic acid. Besides, to avoid etching the whole wafer, approximately 550 μm, the backside of the wafer is first thinned down with TMAH etching solutions. Detailed information about HNA and TMAH can be found in § A.3.2. After fabrication of the transistors, the silicon substrate is then etched with the HNA system. Because all Parylene variants are chemically inert, the HNA etching system does not have any effect on the Parylene HT® film. After completely etching the silicon substrate, the transistor film is cut off the wafer.

Figure 4.15 shows the thin film amorphous silicon transistors fabricated in such a manner.

Figure 4.16 shows the drain and the gate characteristics of the transistors fabricated in this manner. The transistor have electron mobility of 0.3 cm^2/Vs, threshold voltage of 21 V and on/off ratio of 1000. Table 4.10 summarizes the properties of this transistor.

4.3.4 A Working Fabrication Process of In-House Thin Film Amorphous Silicon Transistors

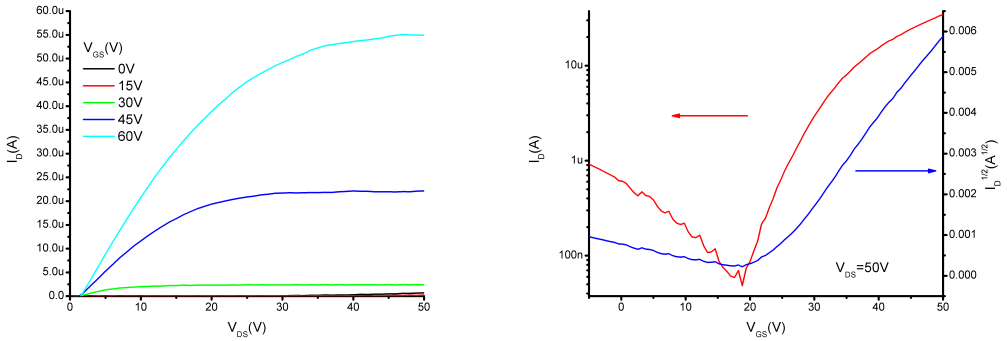
After much effort, the fabrication of process of the thin film amorphous silicon transistors is finally established. This a-Si TFT uses Parylene HT® as the substrate, whose adhesion to the



(a) Wafer (b) Released film

(c) Release film (d) Released film

Figure 4.15: The HNA-released thin film amorphous silicon transistors.



(a) The drain characteristics (b) The gate characteristics

Figure 4.16: the gate characteristics and drain characteristics of the HNA-released thin film amorphous silicon transistors.

Table 4.10: Properties of the HNA-released thin film amorphous silicon transistors.

Properties	
Gate	1500 Å Au / 200 Å Cr
Gate Dielectric	4000 Å SiN_x
W/L	3000/80
a-Si	PECVD 310 °C, 1000 Å
S/D metal	1000 Å Al
Annealing	300 °C, forming gas, 24 hours
Electron Mobility	0.3 cm^2/Vs
Threshold Voltage	21 V
On/Off Ratio	10^3

bottom wafer is promoted with chromium plus A-174 treatment, Au/Cr as the gate electrode and interconnects, PECVD SiN_x as the gate insulator, PECVD amorphous silicon as the channel material, and aluminum as the source/drain contacts. Forming gas annealing is carried out to passivate the amorphous silicon and improve interfaces between Al and a-Si:H. The whole device is coated with Parylene C. The transistor film is released from the wafer by HNA silicon etching. Before the front side transistor processes, the backside of the wafer is first thinned down with TMAH etching solution to reduce the etching time of the later HNA releasing step.

The process flow is illustrated in Figure 4.17 and is given below:

1. Oxidation: The process starts with a double-side-polished wafer. After piranha cleaning, 5000 Å oxide is thermally grown.

2. Backside Oxide Patterning: The oxide on the backside is patterned to open the window of later silicon wet etching. HMDS is applied on the oxide wafer before spinning the photoresist. A 2 μm AZ1518 photoresist is spun on to the wafer and baked at 100 °C for 30 minutes. This layer of photoresist is then exposed and developed. After developing, a descum process is done by short exposure in oxygen plasma. Afterwards, the wafer is hard-baked at 120 °C for 30 minutes. The oxide is then etched with Buffer-HF. After etching, the photoresist is dissolved with ATMI ST-22 photoresist stripper. Next, the wafer is rinsed with ATMI PSR post-solvent rinse and DI water.

3. TMAH Backside Silicon Etching: After pattering oxide, TMAH etching solution is used to

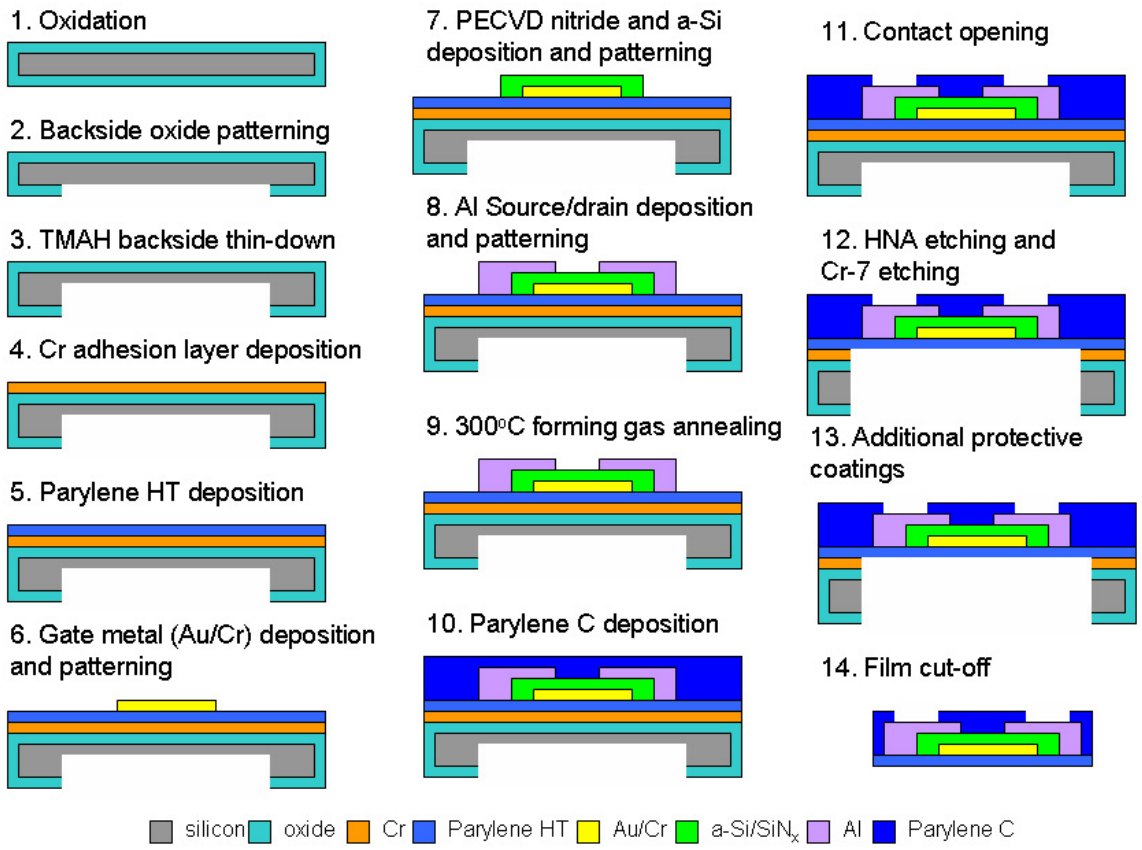


Figure 4.17: Illustrated process flow of the thin film amorphous silicon transistors.

thin-down the backside of the wafer. 15 % TMAH solution is made of the mixture of 25 % TMAH solution from Sigma-Aldrich, Inc., and DI water. The solution temperature is 90 °C. The wafer is dipped in the TMAH solution until the thickness of the wafer is reduced to 50 μm.

4. Deposition of Chromium Adhesion Layer: A layer of 1000 Å Cr is deposited via thermal or e-beam evaporation on the front side of the wafer as the adhesion layer of Parylene HT®.

5. Parylene HT® deposition: Prior to Parylene deposition, the wafer is treated with the A-174 adhesion promotor. Subsequently, 10 μm of Parylene HT® is deposited.

6. Gate Metal Deposition and Patterning: Before metal deposition, the Parylene surface is cleaned by dipping in diluted HF solution (1:10, DI water: 48 % HF) for 30 seconds. This dipping removes particles and hydroxyl groups on Parylene and thus improves adhesion between Parylene and metal. A 2000 Å / 200 Å Au/Cr layer is deposited via thermal or e-beam evaporation. The Cr is used to improve adhesion between the Au and the Parylene surface. Metal patterning is achieved via wet etching processes. A 2 μm AZ1518 photoresist is spun on to the wafer and baked at 100 °C for 30 minutes. This layer of photoresist is then exposed and developed. After developing, a descum process is done by short exposure in oxygen plasma. Afterwards, the wafer is hard-baked at 120 °C for 30 minutes. The Au is etched with Transene Au Etch Type TFA and the Cr is etched with Cyantek CR-7. After etching, the photoresist is dissolved with ATMI ST-22 photoresist stripper. Next, the wafer is rinsed with ATMI PSR post-solvent rinse and DI water.

7. PECVD SiN_x and a-Si:H Deposition: 4000 Å SiN_x and 1000 Å a-Si:H are deposited next onto the wafer via PD900, the PECVD processing equipment. The substrate is held at 310 °C during both depositions. The RF power is 50W for nitride and 10W for a-Si:H.

8. SiN_x and a-Si:H Patterning: A 2 μm AZ1518 photoresist is spun on to the wafer and baked at 100 °C for 30 minutes. This layer of photoresist is then exposed and developed. After

developing, a descum process is done by short exposure in oxygen plasma. Afterwards, the wafer is hard-baked at 120 °C for 30 minutes. The a-Si:H is first etched with SF6 plama and the SiN_x is next etched with Buffered HF. After etching, the photoresist is dissolved with ATMI ST-22 photoresist stripper. Next, the wafer is rinsed with ATMI PSR post-solvent rinse and DI water.

9. Al Deposition and Patterning: A 1500 Å Al layer is deposited via thermal or e-beam evaporation. Al patterning is achieved via wet etching processes. A 2 μm AZ1518 photoresist is spun on to the wafer and baked at 100 °C for 30 minutes. This layer of photoresist is then exposed and developed. After developing, a descum process is done by short exposure in oxygen plasma. Afterwards, the wafer is hard-baked at 120 °C for 30 minutes. The Al is etched with Transene Al Etch Type A. After etching, the photoresist is dissolved with ATMI ST-22 photoresist stripper. Next, the wafer is rinsed with ATMI PSR post-solvent rinse and DI water.

10. Forming Gas Annealing: After patterning the Al source/drain electrodes, the wafer goes through the forming gas annealing. The wafer is placed in the Minibrute furnace and annealed at 300 °C for 24 hours. 100 s.c.c.m. of forming gas (5 % H_2, balance N_2) is flowed into the furnace.

11. Parylene C Coating: After forming gas annealing, 10 μm Parylene C is deposited as the protection and moisture/gas permeation barrier.

12. Contact Opening: After Parylene C deposition, contacts are opened for later testing and connection. A 15 μm AZ9260 photoresist is spun on to the wafer and baked at 100 °C for 30 minutes. This layer of photoresist is then exposed and developed. After developing, a descum process is done by short exposure in oxygen plasma. Afterwards, the wafer is hard-baked at 120 °C for 30 minutes. The Parylene C layer is etched with RIE oxygen plasma. After etching, the photoresist is dissolved with ATMI ST-22 photoresist stripper. Next, the wafer is rinsed with ATMI PSR post-solvent rinse and DI water.

13. HNA Releasing: After contact opening, The transistor film is released with the HNA etching solution. The solution of HNA is composed of 48 % hydrofluoric acid: 70 % nitric acid : glacial acetic acid, 40:30:30 (wt. %). Hydrofluoric acid, nitric acid and glacial acetic acid are purchased from VWR. The HNA solution is applied onto the silicon wafer drop by drop with pipettes to control etching rates and etching areas. After silicon etching, the Cr layer is etched away with Cyantek Cr-7. Finally, the transistor film is cut from the wafer with a razor blade.

14. Parylene Bonding Annealing: After releasing, the transistor film is annealed at 200 °C in vacuum for 48 hours.

Figure 4.18 shows the thin film amorphous silicon transistor fabricated by this process, Figure 4.19 shows the drain and gate characteristics of this thin film amorphous silicon transistor and Table 4.11 summarizes its properties.

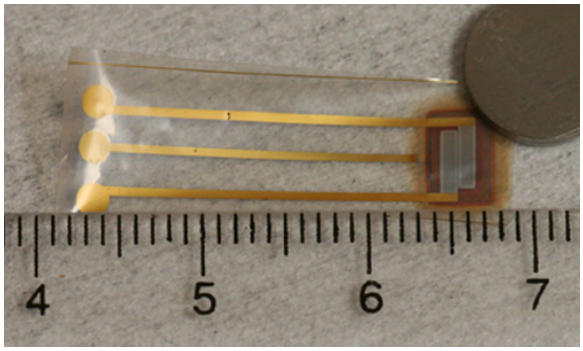
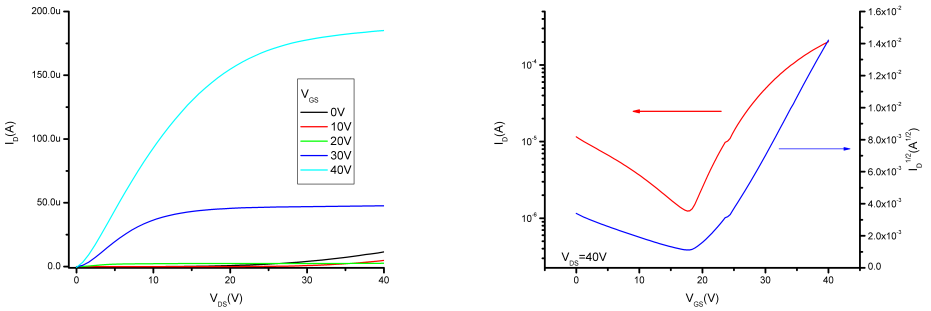


Figure 4.18: The thin film amorphous silicon transistor.

4.3.5 Discussions

Stress in the Film After HNA releasing, the free-standing Parylene film is manually cut off the wafer with a razor blade. During the manual cutting process, the film breaks easily during the cutting process, as shown in Figure 4.20. This may result from the residual stress of Parylene. Harder *et al.* reported that free standing Parylene films have an intrinsic compressive stress of 10MPa [85]. This intrinsic compressive stress cause damages during the cutting process.



(a) The drain characteristics (b) The gate characteristics

Figure 4.19: The drain and gate characteristics of the thin film amorphous silicon transistor.

Table 4.11: Properties of the thin film amorphous silicon transistor.

Properties	
Gate	1500 Å Au / 200 Å Cr
Gate Dielectric	4000 Å SiN_x
W/L	3000/80
a-Si	PECVD 310 °C, 1000Å
S/D metal	1500 Å Al
Annealing	300 °C, forming gas, 24 hours
Electron Mobility	2.0982 cm^2/Vs
Threshold Voltage	20.23 V
On/Off Ratio	10^3

But it can be amended. The residual stress of the free-standing Parylene film can be converted from compressive to tensile by annealing [85]. Therefore, an annealing process at 200°C is carried out after HNA releasing and before cutting. This annealing process not only relieves the compressive residual stress of Parylene but also improves the bonding strength between the two layers of Parylene.

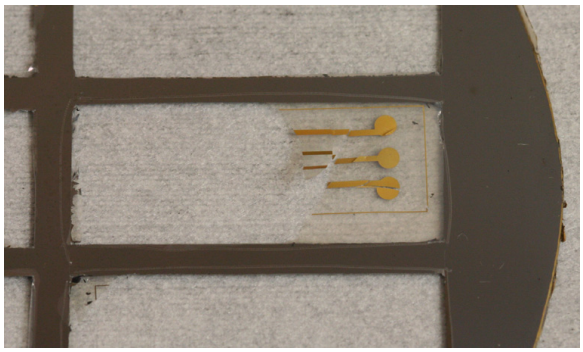


Figure 4.20: The broken film due to compressive stresses.

High Threshold Voltages Almost all the thin film amorphous transistors we made have threshold voltages of around 20V and the value is pretty consistent for all the devices. This high threshold voltage may stem from the PECVD process of amorphous silicon and amorphous silicon nitride. The potential distribution of a capacitively-coupled planar RF-plasma PECVD chamber is shown in Figure 4.21. The electric field points from the cathode to the anode and thus negatively charged particles, e.g. electrons, will be driven, by the electric field, to the anode, where the substrate is. Thus, negative charges may be trapped in the interface between the amorphous silicon and the silicon nitride and increase the threshold voltages. These trapped charges can be eliminated by long-time and high-temperature annealing.

In addition, the dangling bonds of the amorphous silicon nitride also contribute to the trapped charges within the gate insulator. To reduce the effect of the dangling bonds and thus the threshold voltage, the hydrogen content of the amorphous silicon nitride has to be raised. This can be done by adding hydrogen gas into the PECVD process chamber during the deposition of the amorphous silicon nitride. However, this is out of the question currently at

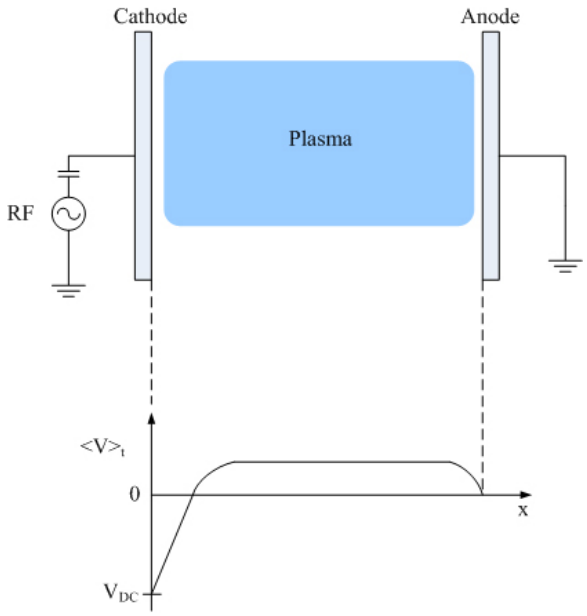


Figure 4.21: Distribution of time-average potential of the capacitively-coupled planar RF PECVD system.

the Caltech Micromachining Lab due to the lack of hydrogen supply.

High Off Current Figure 4.22 shows the magnified part of the drain characteristics of a thin film amorphous silicon n-channel transistor shown in Figure 4.19. The drain current rises when the drain voltage, V_{DS}, increase above certain voltages for the gate voltages lower than the threshold voltage. This drain current is also referred to as the off-current, since the transistor is in the off state. The increased off current is even more obvious in the case of the p-channel transistor (see Figure 4.7). In the gate characteristics shown in Figure 4.19, the drain current increase when V_{GS} decreases below the threshold voltage. This increased off current can be explained by threshold voltage shifts and high off conductivity.

The threshold voltage of an ideal thin film amorphous silicon n-channel should be approximately near zero. Figure 4.23 shows the gate characteristics of such a transistor. Note that the drain current increases when the gate voltage is the negative range. In our devices, the threshold voltage is around 20V and thus the whole curve of the gate characteristics shifts to the right. Figure 4.24 shows the resultant gate characteristics.

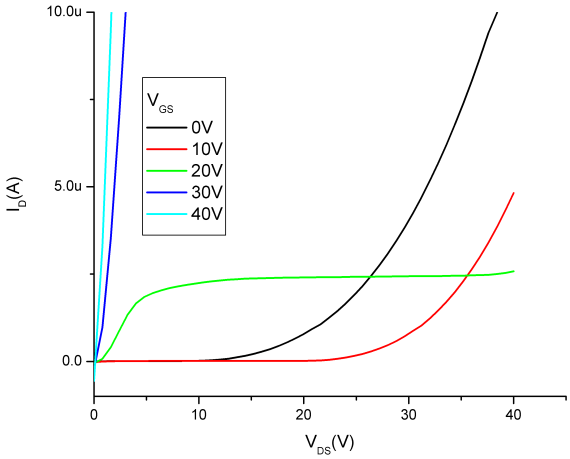


Figure 4.22: Magnification of part of the drain characteristics of Figure 4.19.

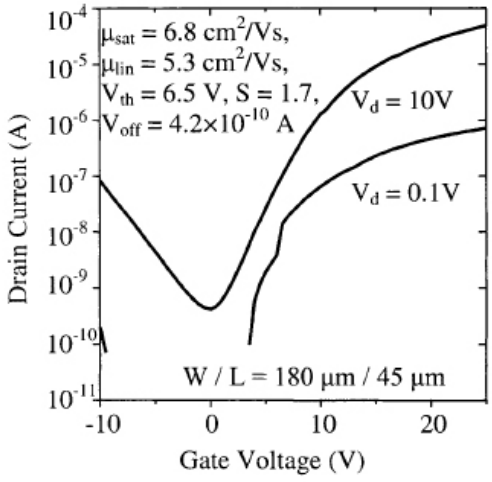


Figure 4.23: The gate characteristics of transistors with near zero threshold voltages. (Modified from [5].)

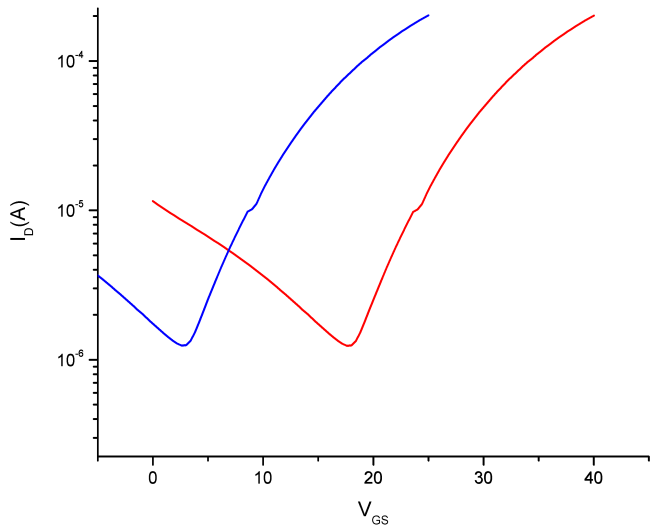


Figure 4.24: The gate characteristics of transistors with different threshold voltages. The red curve is the original gate curve and the blue curve is the shifted one.

The high off current originates from the thick amorphous silicon layer. According to Min *et al.* [5], the thickness-averaged film conductivity rises by around five orders of magnitude as the thickness of the amorphous silicon increases from 50 nm to 350 nm. Our devices use 1000Å thick amorphous silicon. Besides, the channel is undoped and there is no heavily doped source/drain region in our devices. The depletion region of the source/drain and the substrate can be large enough to interfere with each other and thus causing "punch through" leakage current. In addition, because of the low built-in voltage, the transistor is in the flat-band condition. It also has something to do with the large area of the source/channel and drain/channel junctions. All these factors increase the off current.

Several ways are available to reduce the off current. First, the threshold voltage can be reduced by increasing hydrogen content of the silicon nitride. The thickness of the amorphous silicon layer can be reduced. The flat-band electron density can be lowered by gettering oxygen and water from the source gases, by compensation doping, by depositing amorphous silicon in the presence of chlorine or SiF_4 [5].

In summary, the thin film amorphous silicon transistors made at the Caltech Micromachining Lab need to be optimized in the future. And due to limitation of processing equipment, certain optimization methods may not be available at the lab. Although the transistors are not perfect, they can provide useful information for bio-implant studies.

4.4 Degradation of Thin Film Amorphous Silicon Transistors in Saline

4.4.1 Degradation Mechanisms

Degradation of Semiconducting Properties In saline, the major corrosion agents are water, oxygen, sodium ions and chloride ions. Unlike pentacene, amorphous silicon has much stronger resistance to oxygen and water. At room temperature, silicon might form approximately 20Å thick native oxides only. Water and oxygen do not directly affect the semiconducting properties of amorphous silicon as much as those of pentacene. Of course, water might permeate into the interfaces between amorphous silicon and silicon nitride and cause shifts of threshold voltages. Likewise, sodium ions may cause shifts of threshold voltages too. Chloride ions could cause surface corrosions of amorphous silicon as in the case of metal corrosion. However, according to later data, degradation of silicon is not as significant as degradation of pentacene.

Metal Corrosion In saline, metal will be corroded by chloride ions and water. In the case of thin film pentacene transistors, the transistor degrades so fast that the effect of metal corrosion does not manifest. However, for thin film amorphous silicon, the lifetime of the transistor is long enough for the effect of metal corrosion to kick in.

Pitting Corrosion The source/drain contacts of the transistor are made of aluminum. It is well known that the pitting corrosion caused by chloride ions is the most destructive form of aluminum corrosions. Although the thin aluminum oxide serves corrosion barriers, ,the

corrosions developing at localised weak spots in the oxide barrier when contaminants (like the salts in sea air and inland dust, or in spray thrown up from asphalted surfaces) produce an active solution sufficient to destabilize the protective aluminum oxide film and attack the metal. In addition, the presence of chloride ions accelerates corrosion of aluminum immersed in saline in an autocatalytic manner. Aluminum first is oxidized into positive ions. For charge neutrality, negatively charged chloride ions become concentrated at the corrosion site and form aluminum chloride compounds. Subsequently, water reacts with the aluminum chloride compounds and creates metal hydroxide, hydrogen ions, H^+, and chlorides. Now, the corrosion site becomes weakly acidic, which in return accelerates the corrosion process.

Galvanic Corrosion In addition to pitting corrosion, galvanic corrosions also exist. Galvanic corrosion (sometimes called dissimilar metal corrosion) is the process in which the metals in contact with each other oxidizes or corrodes. There are three conditions required by the galvanic corrosion. First, there must be two electrochemically dissimilar metals present. Second, there must be an electrically conductive path between the two metals. Third, there must be a conductive path for the metal ions to move from the more anodic metal to the more cathodic metal. All these three conditions must be fulfilled before galvanic corrosion occurs. In the case of thin film amorphous silicon transistors, the source/drain electrodes are made of aluminum, which is in direct contact with chromium, the adhesion metal of the Au/Cr interconnect. The anodic indices of Au, Cr and Al are 0V, 0.6V and 0.9V. When in contact, the one with higher anodic index tends to be corroded while the other tends to remain. Factors such as relative size of anode (smaller is generally less desirable), types of metal, and operating conditions (temperature, humidity, salinity, etc.) will affect galvanic corrosion. The surface area ratio of the anode and cathode will directly affect the corrosion rates of the materials. In the case of the thin film amorphous silicon transistors, Al is in contact with Cr, which is in contact with Au. Therefore, Al tends to be corroded faster than Cr, which is corroded faster than Au, because of their relative values of anodic indices.

4.4.2 Experiments and Results

After establishment of fabrication processes of the thin film amorphous silicon transistors, the next step is to test how these transistors behave in physiological environments. Instead of placing the transistors inside real animal's body, saline solution is used as as an imitation physiological environment. The thin film amorphous silicon transistors are fabricated by the process described in § 4.3.4. After fabrication, the transistor films are immersed in saline solutions as shown in Figure 4.25.

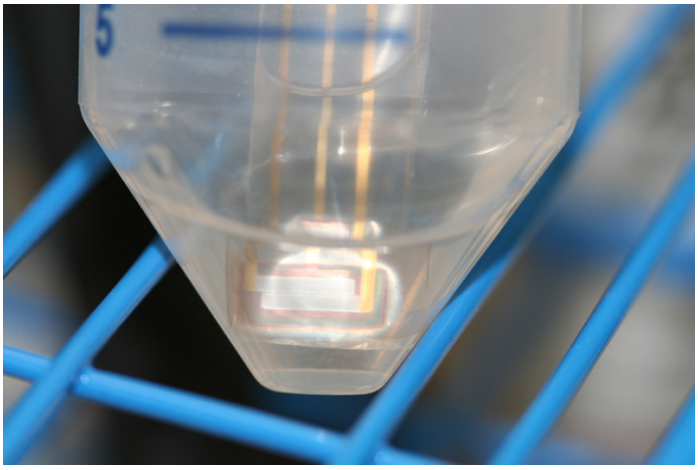
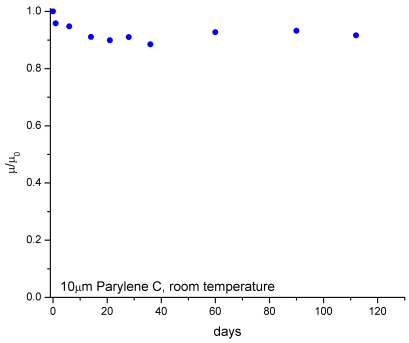


Figure 4.25: The thin film amorphous silicon immersed in saline solution.

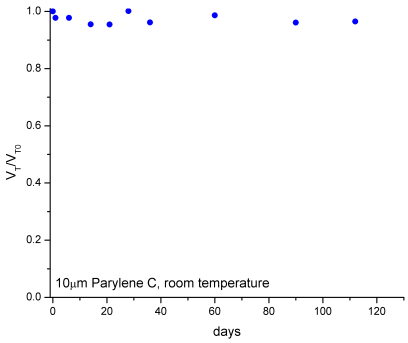
Figure 4.26, Figure 4.27, and Figure 4.28 show the mobility and threshold voltages change over time of transistors with 10, 20, 30 μm Parylene C coating immersed in saline solution at room temperature. The samples with 10 μm Parylene C coating is the thin film amorphous silicon transistors with 5 μm Parylene HT substrate and coated with 10 μm Parylene C. Samples with Parylene coating of other thicknesses are fabricated in similar ways. Therefore, the Parylene thickness on both sides of the transistor are not equal. This does not have crucial impacts on the conclusion of the soaking tests, since all samples use the same process.

After more than 100 days of soaking in saline at room temperature, the transistors do not exhibit significant changes in both mobility and threshold voltages.

To further investigate the soaking reliability and shorten the testing time, accelerated tests

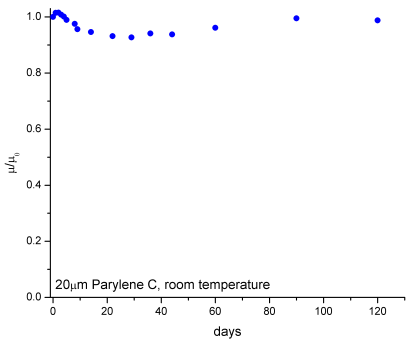


(a) mobility

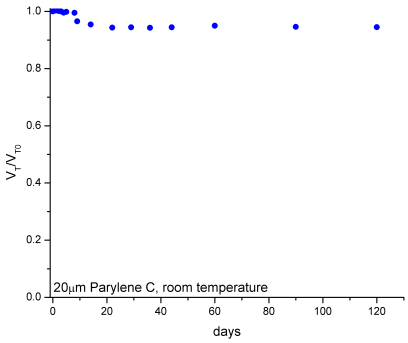


(b) threshold voltage

Figure 4.26: Mobility and threshold voltage of thin film amorphous silicon transistors in saline at room temperature (10 μm Parylene C).

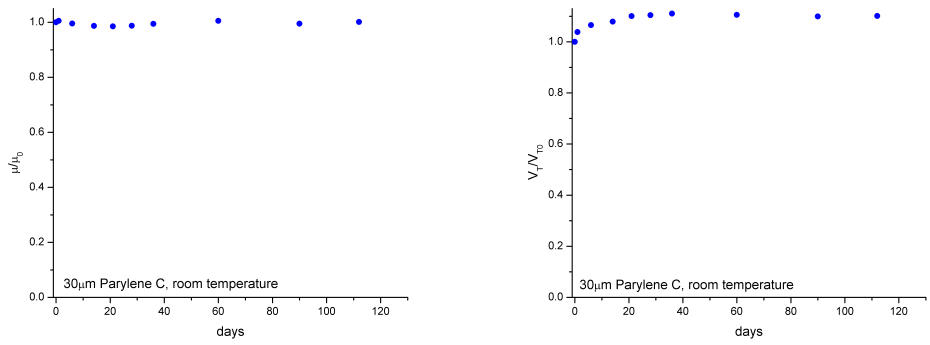


(a) mobility



(b) threshold voltage

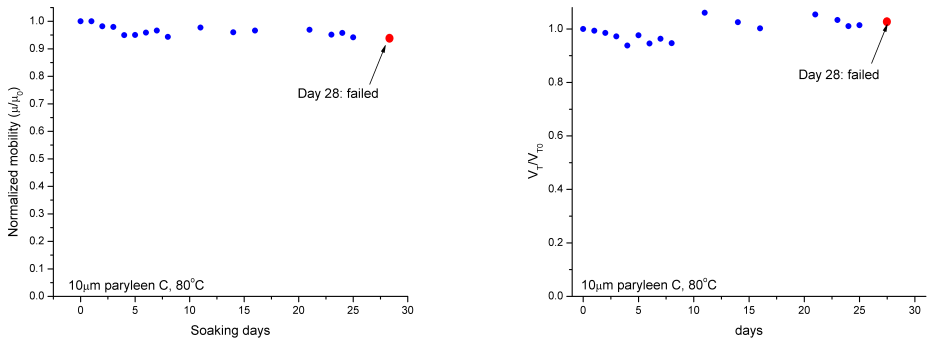
Figure 4.27: Mobility and threshold voltage of thin film amorphous silicon transistors in saline at room temperature (20 μm Parylene C).



(a) mobility (b) threshold voltage

Figure 4.28: Mobility and threshold voltage of thin film amorphous silicon transistors in saline at room temperature (30 μm Parylene C).

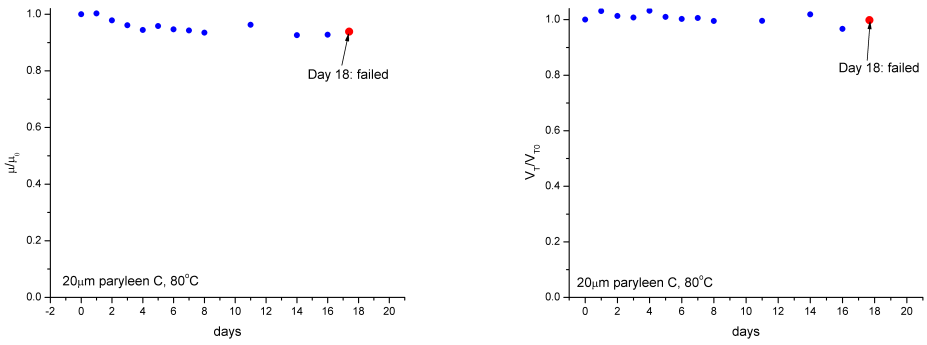
are carried out. Figure 4.29, and Figure 4.30 show the mobility and threshold voltages change over time of transistors with 10, 20, 30 μm Parylene C coating immersed in saline solution at 80 °C.



(a) mobility (b) threshold voltage

Figure 4.29: Mobility and threshold voltage of thin film amorphous silicon transistors in saline at 80 °C (10 μm Parylene C).

The transistor with 30 μm coating exhibits an interesting phenomenon and is worth discussion (Figure 4.31). This transistor failed after 3 days of soaking and luckily, transistor curves can be obtained by probing directly on the source and drain without damaging the devices. Figure 4.32 shows the drain and gate characteristics of this transistor. Although the transistor



(a) mobility (b) threshold voltage

Figure 4.30: Mobility and threshold voltage of thin film amorphous silicon transistors in saline at 80 °C (20 μm Parylene C).

shows poor turn-off features, this might come from the fact that the curves are measured by probing through the 30 μm Parylene C coating and good contacts might not be achieved.

From the fact that these 3 transistors failed randomly and the fact that the transistor still works even though no valid curves can be measured at the contact terminal, it is possible that the failure of the transistors results from metal to metal interconnection.

Figure 4.33 shows the optical images of the connection of the source/drain contact and the interconnect. Corrosion is significant. The SEM image of that area, Figure 4.34 shows no defects on the Parylene C surface, confirming that failure comes from inside.

Based on the information, it requires more than Parylene coating to protect the thin film amorphous silicon transistors from corrosion of saline solution. Parylene-metal-Parylene composited layers is thus proposed as an solution. To evaluate this approach, a thin film amorphous silicon transistor coated with 5 μm Parylene C, 1000 Å Pt, and 5 μm Parylene C has been fabricated and immersed in saline solution at 80 °C. Figure 4.35 shows the thin film amorphous silicon with Parylene-platinum-Parylene encapsulation and Figure 4.36 shows the mobility and threshold voltage changes over time.

The results are excellent. After more than 90 days of soaking in 80 °C saline solution, the transistors still show mobility of 99 % of the initial value and threshold voltage of 98 %

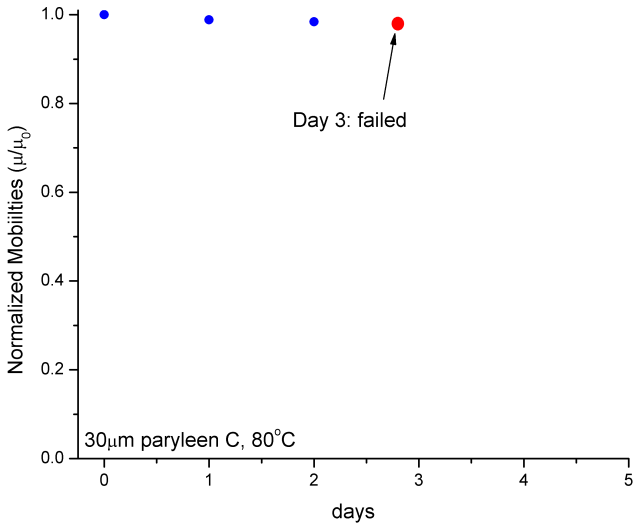
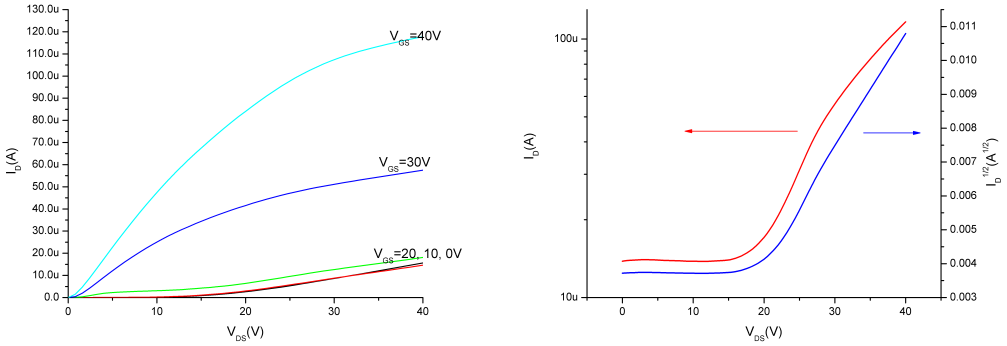


Figure 4.31: Mobility of thin film amorphous silicon transistors in saline at 80 °C (30μm Parylene C).



(a) the drain characteristics

(b) the gate characteristics

Figure 4.32: The drain and gate characteristics of the "failed" thin film amorphous silicon transistor after 3 days of soaking in 80 °C saline.

Figure 4.33: The optical microscopic images of the corroded metal junction.

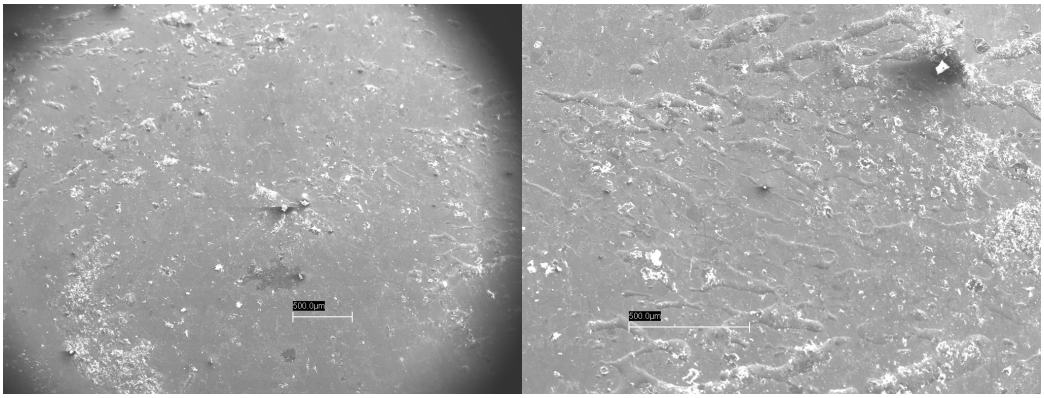
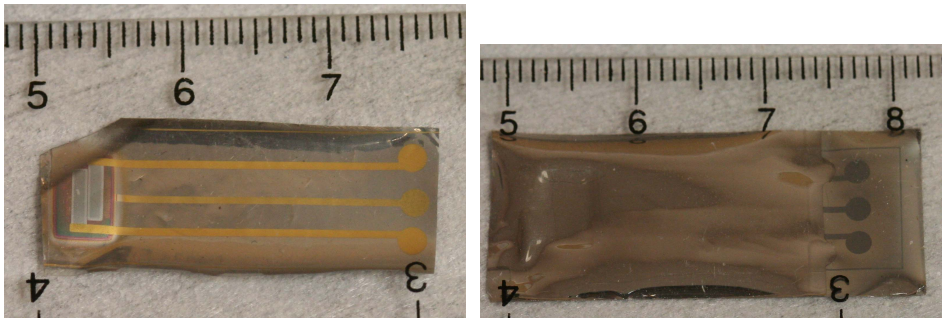


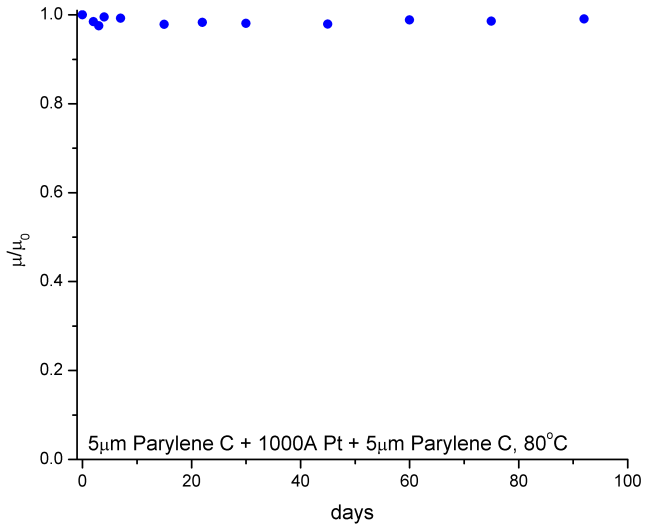
Figure 4.34: The SEM images of the surface of the Parylene covering the corroded metal junction.



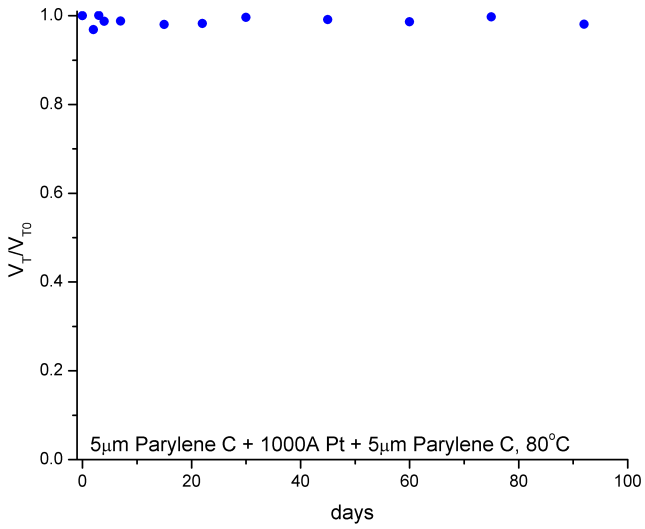
(a) Only the backside has Parylene-Pt-Parylene coating

(b) Both sides have Parylene-Pt-Parylene coating

Figure 4.35: The thin film amorphous silicon transistors with Parylene-Pt-Parylene encapsulation.



(a) mobility



(b) threshold voltage

Figure 4.36: Mobility and threshold voltage of thin film amorphous silicon transistors in saline at 80 °C (5 μm Parylene C, 1000 Å Pt, and 5 μm Parylene C).

of the initial value. It seems that the Parylene-metal-Parylene can stop the corrosion of saline solution effectively and can be applied to other bio-implantation applications requiring Parylene encapsulation.

4.5 Discussions and Future Work

Thin film amorphous silicon transistors are developed. The transistors uses Parylene HT®, a Parylene variant that stands high temperatures, as the substrate. PECVD amorphous silicon is used as the channel material. Because of its immunity to oxygen and moisture, amorphous silicon is an excellent material for bio-implantations, as demonstrated by the soaking tests.

However, the mobility of PECVD thin film amorphous silicon transistors is low, approximately around 1 cm^2/Vs. It is desirable to increase the mobility of the devices. In addition, the devices developed here are not optimized due to limited facilities. Therefore, several works have to be carried out in the future with better equipment and other manufacturing facilities.

High Mobility Instead of PECVD amorphous silicon, low-temperature polysilicon can be employed. As mentioned in previous chapters, low temperature polysilicon can be obtained by deposition of PECVD amorphous silicon followed by excimer laser annealing. By adding an additional step of excimer laser annealing into current fabrication processes, the channel material can be converted into polysilicon and will show higher mobilities, approximately 100 cm^2/Vs.

Heavy Doping of the Source and Drain The ohmic contact problem is circumvented using Al source/drain contact in the current processes. Although it works, but Al source/drain contact is not the optimal solution and the transistors fabricated in this manner shows amphipolarity, that is, behavior of both p-channel and n-channel. PECVD n^+ or p^+ amorphous silicon layers deposited from mixtures of silane and phosphine or diborane can be used to promote ohmic contacts and adjust the polarity of the channel. Ion implantation is another option for source/drain doping.

Elimination of High Temperature Processes Finally, it is desired to keep the temperatures of the fabrication processes low. Currently, the maximum process temperature is 310 °C of the PECVD amorphous silicon and silicon nitride. The PECVD steps can be replaced with room-temperature sputtering of amorphous silicon and silicon nitride. Using sputtered amorphous silicon and silicon nitride can lower the maximum process temperature down to 120 °C of the hard baking of photoresists in the photolithography steps. In addiiton, with such low temperatures, thin film amorphous silicon transistors can be fabricated on Parylene C, Parylene N and other Parylene variants.

In conclusion, the development and study of thin film amorphous silicon transistors shows promising initial results and bio-implantable electronic systems based on thin-film transistors can be realized in the foreseeable future.

Chapter 5

Conclusions and Future Directions

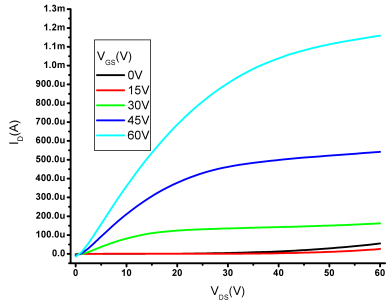
This research presents preliminary studies on implantable electronic systems based on thin film transistor technology. With the use of Parylene, a versatile MEMS/CMOS process compatible and USP Class VI and ISO10933 certified biocompatible material, thin film pentacene transistors and thin film amorphous transistors have been developed.

Fabrication processes of thin film pentacene transistors have been developed. The properties of thin film pentacene transistors have been investigated in detail and performances of thin film transistors have been studied and improved. The dependence of pentacene grains on surface roughness has been studied. It is found that the size of pentacene grains increases with the smoothness of the surfaces. The surface roughness of Parylene has been studied and the methods that smoothen Parylene surfaces have been developed. Long-term reliability of thin film pentacene transistors have been evaluated with room temperature saline soaking tests. With up to 30 μm thick Parylene coating, the thin film pentacene transistors still show significant degradations in room temperature saline solution in a short period of time. If thin film pentacene is to be good candidate for bioimplantable applications, more advanced protection schemes have to be developed.

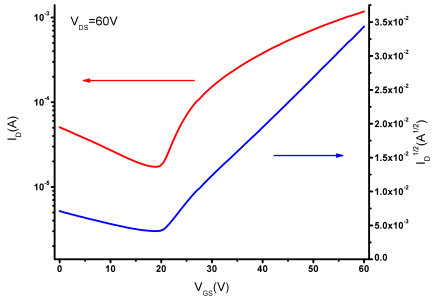
On the other hand, thin film amorphous silicon is chosen because of its relatively stronger resistance of water and oxygen. Unlike pentacene, which reacts fast with oxygen and water at room temperature, silicon remains quite inert at room temperature. With the help of Parylene HT®, a newly-released Parylene variant that has excellent high temperature stability, amorphous

silicon and silicon nitride can be deposited onto Parylene via a PECVD process with the process temperature up to 310 °C. Thin film amorphous silicon transistors have been developed and its long-term reliability has been studied. The soaking test of thin film amorphous silicon transistors in room temperature saline shows excellent results. No degradation of mobility and threshold voltages occurs. The accelerated saline soaking tests at 80 °C further shows that failures of thin film transistors mainly stem from corrosion of metals instead of degradation of amorphous silicon transistors. Parylene-metal-Parylene composite protective coatings have been developed and applied to the thin film amorphous silicon transistors. The accelerated saline soaking data confirm that thin film amorphous silicon transistors with Parylene-metal-Parylene coating remain stable in 80 °C saline solution for more than 90 days. No significant degradations of mobility and threshold voltages are observed. This promises thin film amorphous silicon is a good candidate for bio-implantable electronic systems as long as it is properly protected.

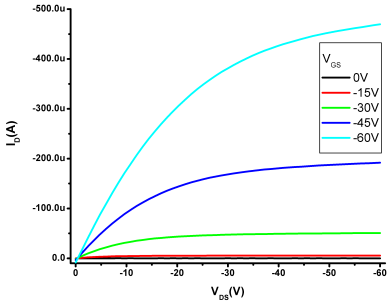
Finally, to conclude this work, an inverter composed of a thin film pentacene transistor and a thin film amorphous silicon transistor is demonstrated. This inverter is made in an assembly manner. The thin film pentacene transistor and the thin film amorphous silicon transistor are connected manually with the help of solder and conductive epoxy. Figure 5.1 shows the drain and gate characteristics of the thin film pentacene transistor and the thin film amorphous silicon transistor. Figure 5.2 shows the transfer curve of the inverter. The hole mobility of the thin film pentacene transistor is 0.56 cm^2/Vs and the electron mobility of the thin film amorphous silicon is 1.2 cm^2/Vs, and both transistors have W/L of 3000/60. The supply voltage is 60V. The high current for input voltage less than the threshold voltage is due to the high leakage current of the amorphous silicon transistor.



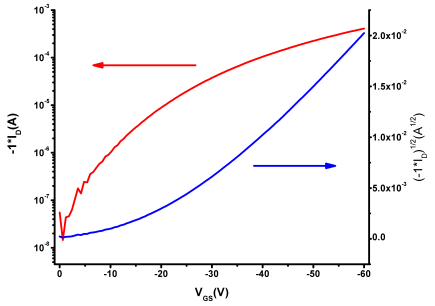
(a) The drain curve of the a-Si transistor



(b) The gate curve of the a-Si transistor



(c) The drain curve of the pentacene transistor



(d) The gate curve of the pentacene transistor

Figure 5.1: The drain and gate characteristics of the thin film pentacene transistor and the thin film amorphous silicon transistor.

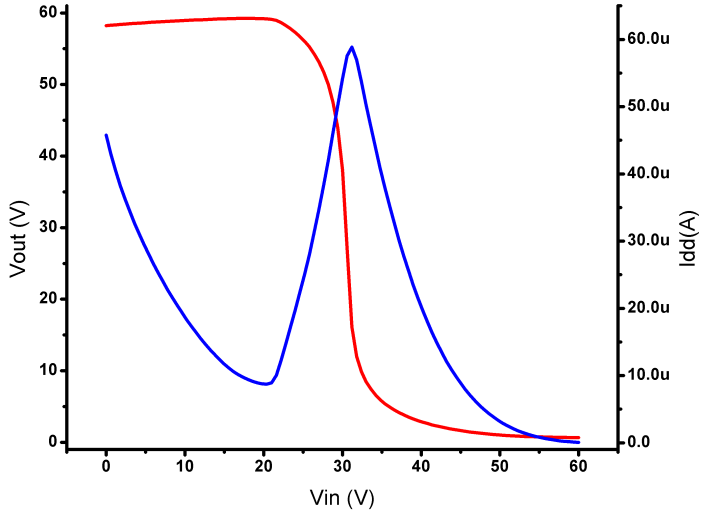


Figure 5.2: The transfer curve of the inverter made of thin film pentacene transistor and thin film amorphous silicon transistor.

Appendices

Appendix A

MEMS Processing Technology

A micro-electro-mechanical system (MEMS) is a micro-fabricated system that contains both electrical and mechanical components. The beginning of MEMS can be traced back to Richard Feynman's talk to the American Physical Society, "There's Plenty of Room at the Bottom", in 1959. Feynman argued the lack of research on "manipulating and controlling things on a small scale". He explained to scientists that this field "might tell use much of great interest about the strange phenomena that occur in complex situations...a lot of new things that would happen that represent completely new opportunities for design" and that "it would have an enormous number of technical applications".

Feynman's idea continues to inspire the research of MEMS community as well as the nano-techology field. Today, the MEMS community spreads all over the world and several terms are used to describe MEMS in different parts of the world: "MEMS" or "micromaching" in the US, "microsystems" in Europe and "micromachines" in Japan. Typical dimensions of MEMS devices range from several millimeters to 100 nm. The material and techniques used in MEMS are continuously evolving. MEMS technology is still based mostly on borrowed technologies from the VLSI industry. Some processes are identical, but others have been adapted to the specific needs of MEMS. The similarity of MEMS technologies and VLSI technologies inspires fusion of MEMS devices and microelectronics on the single silicon real estate and the difference between the two often remains a challenge that cannot be hurdled. Microelectronic devices are confined mainly within the top few microns of the wafer, while MEMS devices may claim

the entire substrate thickness, utilize both sides of the substrate and even require bonding multiple substrates together.

In general, MEMS technology produces devices that are smaller, better and cheaper. MEMS devices have significant smaller footprints than their conventional counterparts. By exploiting phenomena that are better or more efficient with downsizing, MEMS devices are often faster, consume less power and are more sensitive and selective.

The fabrication of Parylene flexbile electronics, either inorganic or organic, are carried out with the help of MEMS technologies. The basic MEMS technologies involved in fabrication of Parylene flexible electronics are :

1. Photolithography
2. Oxidation
3. Etching
4. Physical Vapor Deposition
5. Chemical Vapor Deposition

A.1 Photolithography

Photolithography is a key process that transfers design patterns to the substrates. By selectively initiating chemical reactions of the photoresist on the substrates, the design patterns are first transferred to the photoresist on the substrate. Subsequently, either etching or deposition steps are carried out and thus the design patterns are permanently transferred to the substrate. By repeating such procedures several times, complex MEMS/VLSI structures can be created.

A photolithography process consists of :

1. Spinning photoresist onto wafers and soft baking
2. UV exposure and post-exposure treatment

3. Development using developers

4. Removing residual photoresists (de-scumming) and hard-baking

5. Subsequent deposition or etching

6. Removing photoresists

FIgure A.1 illustrates the pattern transferring process via a photolithography process using positive and negative photoresists.

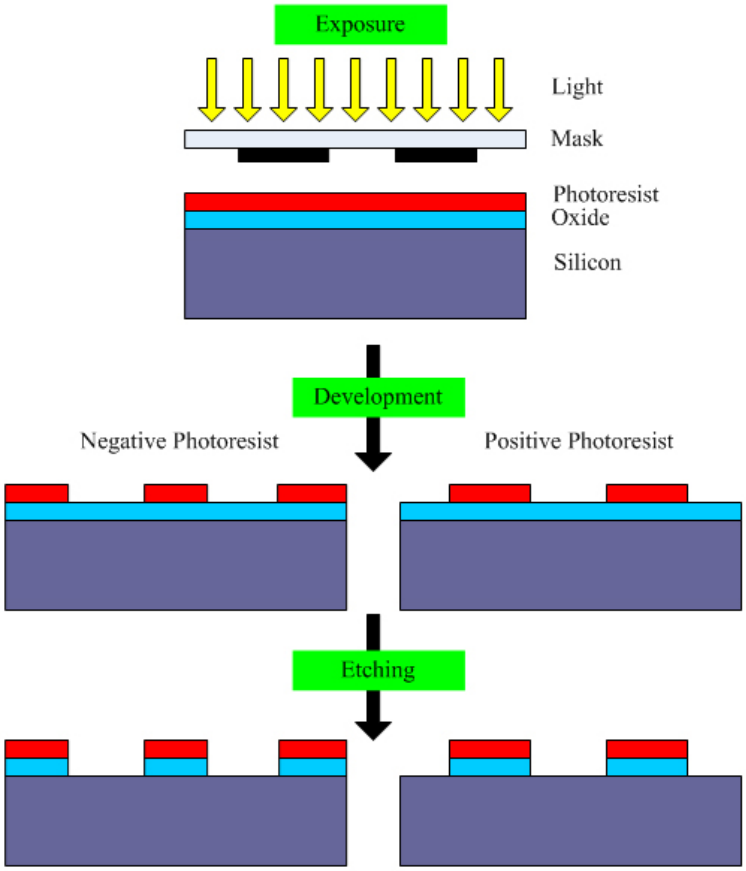


Figure A.1: Illustration of a pattern transferring process using both positive and negative photoresists.

Photoresists The main components of photoresists are a polymer (base resin), a sensitizer, and a casting solvent. The polymer undergoes chemical reactions when exposed to radiation.

The solvent allows spin-coating of the photoresist onto substrates. The sensitizer controls the chemical reactions in the polymer structure changes. For positive photoresists, the photochemical reaction during the exposure usually weakens the polymer by rupture or scission of the main and side polymer chains or by modifying the solubility of the polymer and the exposed photoresist becomes more soluble in developer solutions. While the photochemical reaction of negative resists strengthens the photoresist by cross-linking of the main chains and side chains, making the negative photoresist less soluble in developing solutions.

Soft Baking, Post-Exposure Baking and Hard Baking In a photolithography process, photoresists are usually baked for three times: soft baking, post-exposure baking and hard baking. Soft baking is carried out after spinning of photoresists. After spin coating, the photoresist still contains up to 15 wt.% solvent and may contain built-in stresses. Soft baking at 75 – 100 °C removes solvents and stress and promotes adhesion of the photoresist to the wafer. At the Caltech Micromachining Lab, soft baking is done at 100°C for 30 minutes in a convection oven. Figure A.2 shows the weight change of AZ4903 photoresist as a function of 100 °C soft baking time. 30-minute soft baking removes up to 90 % of solvent in the AZ4903 photoresist. Post-exposure baking is performed after exposure of photoresists. For chemically amplified photoresist, the post-exposure bake is critical. Although the catalysis reaction induced by the catalyst formed during exposure will take place at room temperature, the timing could be highly improved to a few seconds by post-exposure baking. Meanwhile, post-exposure baking can remove the standing wave effect of the photoresists by allowing diffusion of the catalysts inside the photoresist. Finally, after developing and before etching of the substrate or depositing new materials onto the substrate, the substrate goes through hard baking. Hard baking removes residual developing solvents and anneals the film to promote interfacial adhesion of the photoresist, which is weakened by developer penetration along the photoresist-substrate interfaces or by swelling of the photoresists. Hard baking also improves the hardness of the photoresist and increases the etching resistance of the photoresist in the following etching

steps. Hard baking is often carried out at 120 °C or higher temperatures.

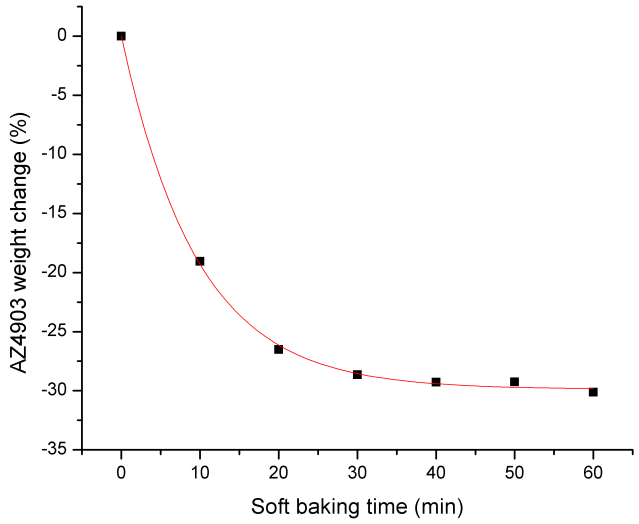


Figure A.2: Weigth changes of AZ4903 photoresist versus soft baking time, courtesy of Mr. Chun-Hui Lin at the Caltech Micromachining Lab.

A.2 Thermal Oxidation

Silicon dioxide (SiO_2, or oxide) is used in a variety of MEMS applications, including as a insulating material, a etching mask, a sacrificial material, etc.. Silicon readily oxidizes at room temperature forming thin naitve oxide approximately 20Å thick. Two main chemical reactions underly the thermal oxidation process:

$$Si + 2H_2O \rightarrow SiO_2 + H_2 \text{ (wet oxidation)}$$

$$Si + O_2 \rightarrow SiO_2 \text{ (dry oxidation)}$$

The quality of oxide depends primarily on its growth method. Dry oxidation at high temperatures betwee 900 and 1150 °C in pure oxygen produces a better quality than wet oxidation. Dry oxide is stoichiometric, has a higher density and is virtually free of pinholes. Wet oxidation

gives much higher growth rates but less quality oxide. Water in the wet oxidation makes the resulting oxide less dense and renders it more prone to impurity diffusion.

Both wet oxidation and dry oxidation are carried out in quartz tubes. Thermal oxidation give good oxides with thickness of a few thousand Angstroms. 1 to 2 μm is the upper limit of conventional thermal oxides.

The drawback of thermal oxidation is that silicon must be free of all metals or polymers, since these materials cannot generally withstand the high temperature and will interfere with the oxidation reaction. This limits the use of thermal oxide as a sacrificial layer.

A.3 Etching

The etching processes involved in MEMS technology can be divided into two categories: the wet etching and the dry etching. In general, the wet etching process is carried out by immersing the substrate in liquid etching solution while the dry etching process often involves plasma or gaseous etching chemicals. Although the wet etching process is generally faster and cheaper, it cannot generate pattern features smaller than 3 μm. In addition, for most wet etching chemicals, the etching profile is isotropic. On the other hand, dry etching requires less amount of etching chemicals and can provide both isotropic and anisotropic etching profiles, directional etching, high-resolution etching patterns and better process control. The shortcomings of dry etching are expensive and complicated processing equipment and slow etching rates.

A.3.1 Wet Etching

In MEMS fields, wet etching processes are carried out for patterning of thin films and bulk silicon. The thin films includes oxide, nitride and metals. The etching chemical basically consists of an oxidizer, an acid or base to dissolve the oxidized material, and a diluent. Most etching chemicals of thin films produce isotropic etching and only certain etching chemicals of silicon give anisotropic etching profiles. William *et al.* have published two papers with etching rates

of almost all wet etching chemicals used in MEMS [94][95].

A.3.2 Wet Etching of Silicon

Wet etching of silicon is very important in silicon bulk micromachining. In silicon micromachining, it is often necessary to etch silicon of hundreds of micrometers. Although dry etching technologies can provide high resolutions, the fast etching rates and simple equipment setup makes wet etching processes preferable in many applications.

Isotropic Wet Etching of Silicon The isotropic wet etching is carried out with the famous tri-acid system, hydrofluoric acid, nitric acid and acetic acid (HNA). Robbins and Schwartz published their studies on the etching rates of the HNA etching system with various ratios and under various temperatures [96]. The famous triangle of iso-etch curves is now a standard reference tool when performing an isotropic etching of silicon.

In acidic media, the silicon etching process involves hole injection into the Si valence band by an oxidant, an electrical field or photon. Nitric acids in the HNA etching system acts as an oxidant. Hydrofluoric acid removes the product of oxidation, or silicon dioxide, by forming water-soluble H_2SiF_6. The overall chemical reaction of the HNA etching system is:

$$Si + HNO_3 + 6HF \rightarrow H_2SiF_{6(\text{soluble})} + HNO_2 + H_2O + H_{2(\text{bubble})} \,.$$

The etching rate of the HNA system depends on the process temperature and the weight ratio of the HNA system. The etch rate of the HNA system ranges from several micrometers per minute up to 200 hundred micrometers per minute. One common mask material for the HNA system is silicon dioxide. Although silicon dioxide is also etched by the HNA system, the etching rate of silicon oxide is 300 to 800 Å/min and thick oxide can serve as a mask for shallow etching. A mask of nonetching Au or LPCVD silicon nitride is required for deeper etching. Etching masks made of Parylene C are developed recently as a easy and low-cost alternative of nonetching mask materials for the HNA etching system [97].

Anisotropic Wet Etching of Silicon A variety of chemicals have been used for silicon anisotropic wet etching, including alkaline aqueous solutions of KOH, NaOH, NH_4OH and quaternary ammonium hydroxides (for example tetramethyl ammonium hydroxide, TMAH). Alkaline organic solutions such as ethylene-diamine pyrocathechol (EDP) are employed as well.

The chemical reactions involved in alkaline anisotropic etching of silicon are complicated. Seidel proposed an model for this etching process [98] and the chemical reactions are given below:

$$Si + 2OH^- \rightarrow Si(OH)_2^{2+} + 2e^-$$

$$Si(OH)_2^{2+} + 2OH^- \rightarrow Si(OH)_4 + 2e^-$$

$$Si(OH)_4 + 4e^- + 4H_2O \rightarrow Si(OH)_6^{2-} + 2H_2$$

The anisotropy of these wet etching chemicals results from the different etching rates on silicon with different crystal orientation. The anisotropy ratio (AR) is defined by the ration of etching rates of silicon with different crystal orientations. For example, the AR of an 50 wt.% KOH solution at 85 °C is 400/200/1 for (110)/(100)/(111) silicon. By carefully controlling the crystal orientation of the substrate and designing special masks, various structures of silicon, such as v-shape trenches can be created (see Figure A.3).

Commonly used anisotropic etching solutions are KOH and TMAH. Due to its toxicity, EDP is now seldom used for silicon wet etching processes. The etching rate of KOH and TMAH are a few micrometers per minute. A common masking material is silicon oxide. The selectivity (silicon/oxide) of KOH is approximately 60 and that of TMAH is approaching infinity. To etching through a 550 μm thick wafer, thick oxides more than 1μm thick is required in KOH etching system while oxide of only a few thousand Angstroms is enough in TMAH etching solution.

In this work, the HNA isotropic etching system is later used in the releasing step of the fabrication of Parylene HT® - packaged amorphous thin-film transistors and the TMAH etching system is used to thin down the substrate of that process.

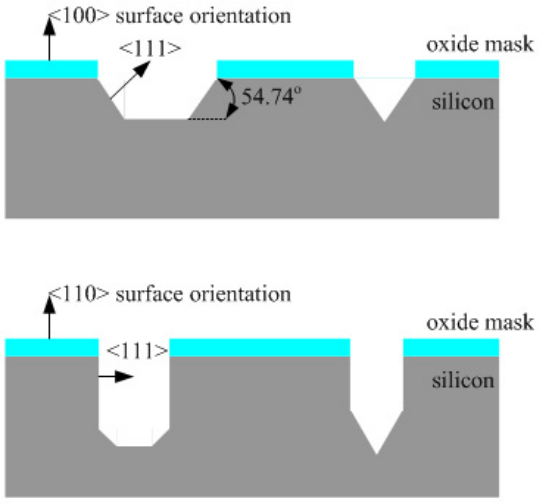


Figure A.3: Anisotropic wet etching of silicon (< 100 > and < 110 > surfaces).

A.3.3 Dry Etching

The dry etching process is a method by which a solid surface is etched in the gas phase, physically by ion bombardment, chemically by a chemical reaction with a reactive species at the surface, or combined physical and chemical mechanisms.

The plasma-assisted dry etching employs plasma to enhance the reactivity of chemicals or directional ion bombardment. Plasma is a partially or fully ionized gas, large enough and dense enough to interact with its own self fields. The plasma may contain electrons, positive ions and perhaps negative ions and neutral atoms and molecules, both excited and ground state. Plasma is generated by supplying energy to coupling electrodes. Electrons are thus accelerated, collide with the neutral molecules and produce new electrons and positive ions. Electrons and ions are annihilated via recombination. When the system reaches the steady state, a plasma is generated. The external energy can be either dc or radio-frequency energy. The industrial RF power usually has frequency of 13.56 MHz. Energy is transfered to the plasm via either capacitively coupling or inductively coupling mechanisms. Capacitively-coupled plasma is generated by a pair of parallel plates. Electric fields between the parallel plates accelerate electrons and ions and generate ionizations. Inductively-coupled plasma is generated by a helical coil combined with

an electrostatic shield. The electrons and ions are accelerated by the time-varying magnetic fields produced by currents passing through the helical coils. Inductive coupling can generate plasma of high density, low pressure, and low energy and thus high etch rate, high selectivity and high ion directionality.

In general, plasma-related dry etching can be divided into three categories: physical etching, chemical etching and physical-chemical etching.

A physical plasma etching employs plasma of inert gases, usually argon. The etching mechanism is mainly that the collision of high energy ions with the substrate material dislodges away the substrate material. Since it is a purely physical and impact-controlled process, physical plasma etching is completely directional and nonselective.

Meanwhile, chemical plasma etching substitutes reactive gas for the inert gas in physical plasma etching. The reactive neutral chemical species, such as chlorine or fluorine atoms and molecules generated in the plasma diffuse to the substrate where they form volatile products with the substrate. The only role of the plasma is to provide the gaseous and reactive etching atoms and molecules. Since it is a chemical process, chemical plasma etching is isotropic and selective.

Physical-chemical etching is the combination of physical plasma etching and chemical plasma etching. The ion bombardment of physical-chemical etching can make the substrate more reactive, removes film-forming reaction products and provide energy to drive surface reactions. Physical-chemical etching thus possess selectivity and directionality at the same time. Two types of physical-chemical plasma etching are widely used in MEMS: the reactive ion etching (RIE) and the deep reactive ion etching (DRIE). The plasma of a RIE system is either capacitively coupled or inductively coupled while that of a DRIE system is inductively coupled. The DRIE system uses additional polymer coating (the Bosch process) or chills the substrate wafer to low temperatures (the cryogenic process) to achieve large etching aspect ratios and vertical etching profiles.

A.4 Physical Vapor Deposition

Physical vapor (PVD) deposition is a process to deposit thin films in VLSI and MEMS fields. A PVD process includes 2 basic steps: dislodging the thin film material from the source, either by heating or ion bombardment and the dislodged source material attaching to the substrate and forming thin films. Depending on the dislodging methods, PVD can be divided into 2 schools: thermal evaporation, and sputtering.

Evaporation Thermal evaporation is one of the oldest thin film deposition techniques. Evaporation is based on the boiling off or sublimating of a heated material onto substrate in a vacuum. Depending on the size of the bell jar, a successful deposition of thermal evaporation requires a proper mean free path. The rule of thumb of mean free path is given by Equation A.1. In addition to mean free paths of particles, the oxygen partial pressure needs to be less than 10^{-8} Torr in order to avoid oxidation and other reaction at the boat.

$$\ell(\text{cm}) = \frac{5}{P\ (\text{Torr})}\ . \tag{A.1}$$

Thermal evaporation is usually carried out by either resistive heating or eletron-beam (e-beam) heating. In a evorator of resistive heating, metal is placed in a tungsten boat or filament and high current is passed through the tungsten boat or filament. A e-beam evaporator uses a high energy electron beam, usually 3 – 20 kV, focused on the target material that is placed in a crucible in a water-cooled copper hearth. The e-beam is directed by a magnetic field to the source crucible and locally melts the metal source. In this manner, the unmelted metal is too cool for any reaction and thus fewer contamination problem occur than in the case of resistive heating. One advantage of a evaporator of resistive heating over the e-beam evaporator is that a new charge of metal is used for each evaporation, as opposed to reusing of the source material for multiple depositions.

Sputtering Sputtering is preffered over evaporation in a variety of applications because of a wider choice of deposition material, better step coverage and better adhesion to the substrate. In a sputtering process, the target source, usually in the form a disc, is placed at a high negative voltage and bombarded by positive argon ions created in a plasma as a result. The plasma can be created with DC or RF power supply. The target material is dislodged as positively charged ions by momentum transfer and the expelled atoms are deposited on the substrate placed at the anode. During sputtering, the source is not heated and the vapor pressure is not concern as it is in thermal evaporation. Meanwhile, because sputtering is mainly a physical process, a lot of materials, especially insulators such as oxide and nitride, can be deposited in this manner. Sputtering provides a freedom of material choice in designing fabrication processes.

A.5 Chemical Vapor Deposition

A chemical vapor deposition (CVD) is a deposition process in which the constituents, which are in vapor phases and often diluted with an inert gas, reactions at the hot surface of the heated substrate to form a solid film. The CVD process works at both low pressure and atmospheric pressure, and at both low temperatures and high temperatures. Amorphous, polycrystalline and epitaxial films can be deposited via CVD processes. The CVD process is one of the key process in fabrication of Parylene-package amorphous silicon thin-film transistors.

Room Temperature Chemical Vapor Deposition Few materials are deposited via room temperature CVD processes. Parylene is one of them. The dimer of Parylene is vaporized and pyrolyzed to form monomers with free radicals. These highly-reactive Parylene monomers readily form polymers on the substrate at room temperature in a vacuum ranging from 1 – 100 mTorr.

Plasma Enhanced Chemical Vapor Deposition In a plasma-enhanced chemical vapor deposition (PECVD) process, the plasma provides the radicals that reacts with one another and form

the deposited films and ion impacts on the substrate provides energy required to arrived at the stable desired final products. Common processing temperatures of PECVD processes range from 250 – 350 °C and processing pressures are in the range of 10 to 100 mTorr.

Atmosphere Pressure Chemical Vapor Deposition Atmospheric to slightly reduced pressure CVD (approximate 750 mTorr) is used to primarily to grow epitaxial films of silicon and compound semiconductors and to deposit silicon oxide at high rates from oxygen and silane at lower temperatures of 300 – 450 °C.

Low Pressure Chemical Vapor Deposition Low pressure CVD at below 75 mTorr allows large numbers of wafers to be coated simultaneously with good wafer-towafer film uniformity. Oxide, nitride, and phosphosilicate glass (PSG) are often deposited via LPCVD processes. However, low deposition rates and relatively high temperatures are its two disadvantages.

Table A.1 summarizes the properties of CVD processes.

Table A.1: Properties of CVD processes.

Process	Pros	Cons	Applications
APCVD	Simple, high deposition rates, low temperature	Poor step coverage, particle contamination	Doped and undoped low-temperature oxide
LPCVD	Excellent purity and uniformity, conformable step coverage, large wafer capacity	High temperature and low deposition rate	Doped and undoped high temperature oxide, silicon nitrides, polysilicon, W, WSi_2
PECVD	lower substrate temperatures; fast, good adhesion; good step coverage; low pin hole density	Chemical (e.g. Hydrogen) and particulate contamination	Low-temperature insulators, passivation (nitride)

Process	Pressure (mTorr)	Temperature (°C)
APCVD	75 – 750	300 – 450
LPCVD	75	550 – 600
PECVD	10 – 100	250 – 350

A.6 Summary

The fabrication technologies that enables Parylene-packaged thin-film transistors are those common fabrication technologies in MEMS and VLSI industries. While sharing a lot with the VLSI industry, MEMS places its own unique stance on integration of mechanical and electrical components. From Feynman's talk, MEMS has evolved from a major research to a background technology that enables many applications in other disciplines, such as biology. The fast-growing MEMS market and potential MEMS applications have attracted not only academic researcher but also commercial venture capitals. While maintaining a market growth rate of 11 % per year (NEXUS, 2005), MEMS will claim more and more shares in our daily life.

Appendix B

Parylene and MEMS Applications

B.1 Parylene Background

Parylene, or poly(para-xylylene) is the generic name for a family of a unique room-temperature CVD thermoplastic polymers, discovered by Michael Szwarc in Machester, England [99]. Later, William Gorham of Union Carbide devised a relatively easy and simple deposition process of Parylene that involves vaporization of dimer powders, pyrolysis of dimer vapor and polymerization of monomers in vacuum at room temperature. However, Parylene was not commercially available until Donald Cram of UCLA developed a synthesis process of Parylene dimers in 1951. In 1965, Union Carbide released this vacuum deposition process dubbed as the Gorham process. Since then, over twenty types of Parylene have been developed. Not all members of the Parylene family are commercially available. Only Parylene N, the very first Parylene film deposited, Parylene C, the second commercially available, Parylene D, and Paryleen HT ® (recently released by Specialty Coating Systems, USA) are available in the market. Multiple companies all over the world provide Parylene. In the US, the company Speicalty Coating Systems sells Parylene dimers and Parylene dimers are sold under the brand name of diX (Daisankasei Co. Ltd.) in Japan. Figure B.1 shows the four commercially available Parylene variants.

Parylene polymers are deposited via a room-temperature CVD process in 25 – 35 mTorr vacuum. The Gorham process starts with evaporation of Parylene dimers in a vaporizer heated at approximated 120 – 150 °C. The dimer vapor then passes through a pyrolysis funace with

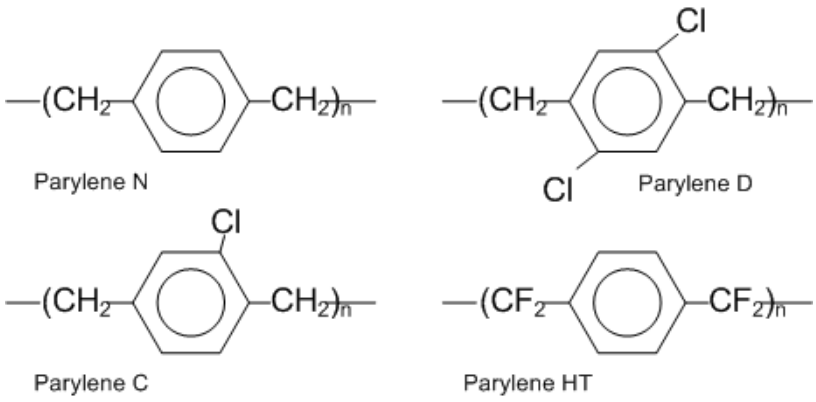
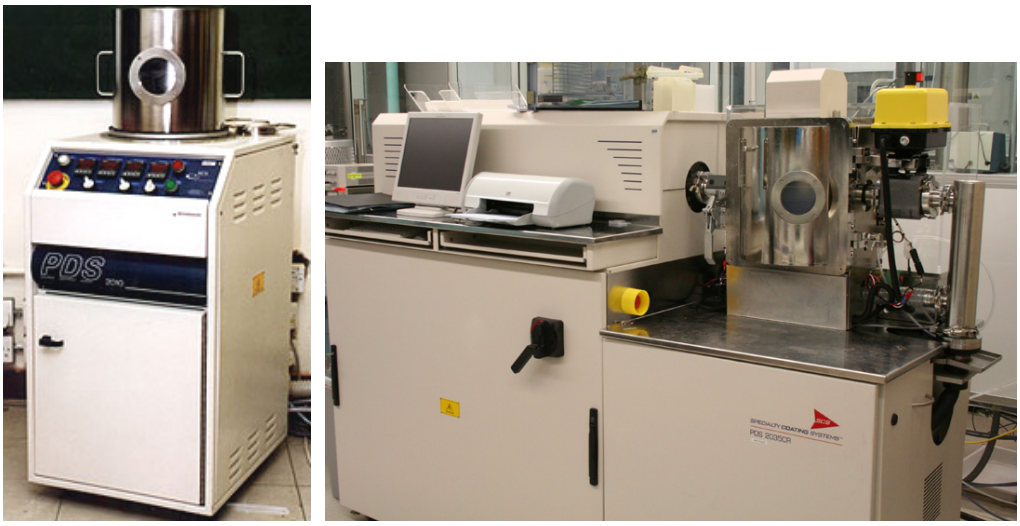


Figure B.1: Four commercially available Parylene variants.

temperatures of 650 – 750 °C. In the pyrolysis furnace, Parylene dimers go through thermal pyrolysis and split into monomers. Next the monomer enters a bell jar at room temperature with chamber pressures of approximately 12 – 22 mTorr. Polymerization of Parylene monomers occur on all the surfaces inside the bell jar and conformal coatings of Parylene are formed without pin holes. Residual Parylene monomers are collected by a coldtrap. General Parylene coating is carried out on the PDS 2010 Labcoater System, but the deposition of Parylene HT® has to be done with the new equipment, PDS 2035 (Figure B.2). Figure B.3 illustrates the Gorham process of Parylene.



(a) PDS2010 (b) PDS2035

Figure B.2: The Parylene coating equipment.

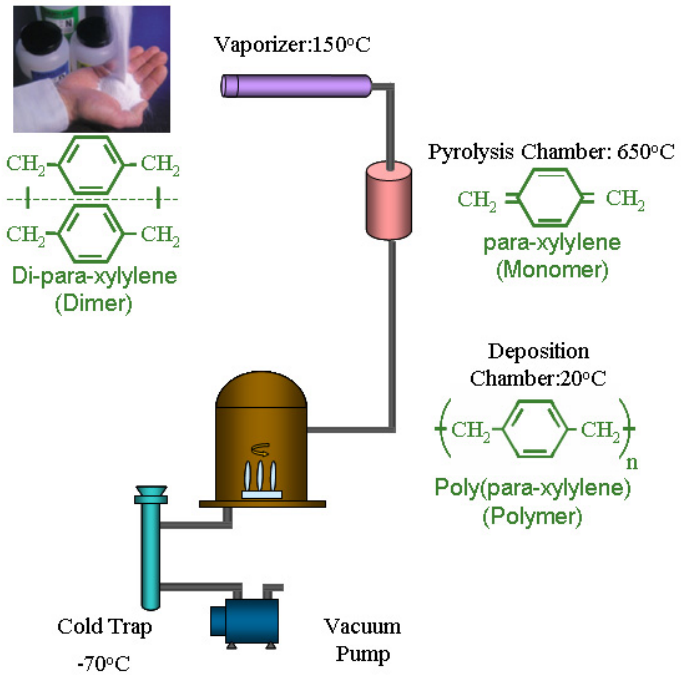


Figure B.3: Illustration of the Parylene deposition process.

Among all Parylene variants, Parylene C is the most widely used. Parylene C is an ISO10933, the United States Pharmacopeia (USP) Class VI material (the highest biocompatibility rating for plastics in the United States) and has low gas and moisture permeability. Optically, Parylene C is transparent above 300 nm and throughout the visible range.

Although Parylene C is excellent material for MEMS application, its low glass transition temperature and low melting points render it poor material choice for devices that need high-temperature processes such as PECVD. Parylene HT® is developed to cover this unaddressed range. Parylene HT® has a melting point greater than 500 °C and a short-term service temperature up to 450 °C. Parylene HT® has the lowest frictional coefficient of 0.15 and dielectric constant of 2.2. Parylene HT® is also ISO10993 certified biocompatible material. Table B.1 lists important properties of Parylene.

Table B.1: Properties of Parylene N, C, D, and HT®. (Modified from courtesy of Dr. Siyang Zheng at the Caltech Micromachining Lab.)

Property	**Parylene N**	**Parylene C**	**Parylene D**	**Parylene HT**
Dielectric Strength (V/mil), 1 mil film	7,000	5,600	5,500	5,400
Dielectric Constant				
60 Hz	2.65	3.15	2.84	2.21
1 kHz	2.65	3.10	2.82	2.20
1 MHz	2.65	2.95	2.80	2.17
Young's Modulus (psi)	350,000	400,000	380,000	–
Index of Refraction	1.661	1.639	1.669	–
Yield Strength (psi)	6,100	8,000	9,000	–
Elongation to break (%)	20 – 250	200	10	–
Coefficient of Friction				
Static	0.25	0.29	0.33	0.145
Dynamic	0.25	0.29	0.31	0.130
Density (g/cm^{-3})	1.10 – 1.12	1.289	1.418	–
Melting Point (°C)	420	290	380	>450
Service Temperature (°C)				
Short-Term	80	100	120	450
Continuous	60	80	100	350
Water Vapor Transmission Rate $(g \cdot mm)/(m^2 \cdot day)$	0.59	0.08	0.09	0.22
Oxygen Permeability at 25°C $(cc \cdot mm)/(m^2 \cdot day \cdot atm)$	15.4	2.8	12.6	23.5

B.2 Parylene and MEMS Applications

As mentioned in the previous sections, Parylene is deposited via a room temperature CVD process and it can be readily patterned with conventional MEMS/VLSI photolithographic processes and oxygen plasma etching with photoresist or metal masks. These properties, along with other mechanical properties, Parylene have been used in a variety of MEMS applications as a structural material. The conformal coating characteristics and the mechanical robustness of Parylene make it a excellent structural material for microfluidic applications. Parylene microfluidic devices such as channels, pumps [100], valves [101], filters and flow sensors [102], mass flow controllers [103], electrospray nozzles [104] and gas chromatography columns [105] have been demonstrated. Figure B.4 shows a few of these devices.

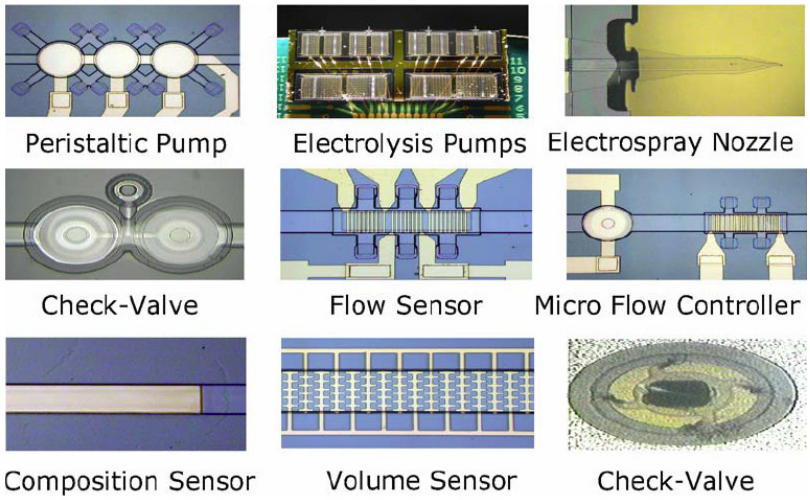


Figure B.4: Parylene microfluidic devices.

B.3 Parylene HT® and Power MEMS Applications

In addition to serving as a structural and packaging material, Parylene can also be used in power generation applications. This novel application wasn't feasible until the release of Parylene HT®.

B.3.1 Thin-Film Parylene HT® Electret

In 1980, Raschke and Nowlin from Union Carbide reported the first study on Parylenes as electret materials [106], in which Parylene HT® was referred to as Òpolymer AF-4Ó but limited results was available. Unfortunately, after [106] no research was reported on Parylene HT® as an electret material until this work, which is probably due to the unavailability of the material.

An electret is an insulating material that exhibits a net electrical charge or dipole moment. The net charge or dipole moment in the electret can be used to provide a biasing electric field such as for MEMS electret microphone [107][108]. Electrets are also useful for electrostatic generators. In fact, different electret materials have been studied for micro power generators. Boland et. al. made power generators with Teflon AF® as the electret [109][110][111]. Tsutsumino et. al. developed CYTOP®-based power generators [112][113]. Sterken et al demonstrated silicon oxide/silicon nitride electret micro power generators [114][115]. Among various electret materials, polymers such as Teflon and CYTOP® are of research interests because of their ease of processing. Although oxide/nitride electret could have higher charge densities [116], high-temperature processes often render them inferior to polymer counterparts in certain applications. In any case, the charge density is an important parameter for electrets. Table B.2 lists charge densities of common electret materials.

Table B.2: Charge densities of common electret materials.

Electret Material	Charge Density (mC/m^2)
Oxide/Nitride	11.51 [116]
Teflon AF	0.50 [117]
CYTOP®	1.37 [112]
Parylene HT®	3.69

To study the charge retention property of Parylene HT®, Parylene HT® is first deposited on soda lime wafers. Next, samples coated with Parylene HT® are implanted with electrons with corona discharge method. Distribution of surface potential of charged Parylene HT® is measured with an integrated system of Monroe Isoprobe® and computer-controlled x-y stage. Table B.3 lists the conditions of corona charging. Different from other literatures, constant

grid and base currents are employed, instead of constant needle and grid voltages. The corona charger is so controlled that the currents of the base and the grid is maintained at the values shown in Table B.3 by dynamically controlling the voltages of the needle and grid with PID controlling algorithms. Figure B.5 shows the space distribution of the charged sample. The highest surface potential observed is 204.58 V/μm, equivalent to a surface charge density of 3.69 mC/m^2. The surface potential of the electret depends on the thickness of the electret. Under the same corona charging conditions, the thicker electret can achieve higher surface potential. Therefore, it is meaningful only when we compare the electric field, volt/μm. The surface charge density can be calculated from this value. That is why the unit of volt/μm is shown in all surface potential plots.

Table B.3: Corona charging conditions.

Base Current	0.02 μA
Grid Current	0.2 μA
Sustrate Temperature	100 °C
Charging Time	60 minutes

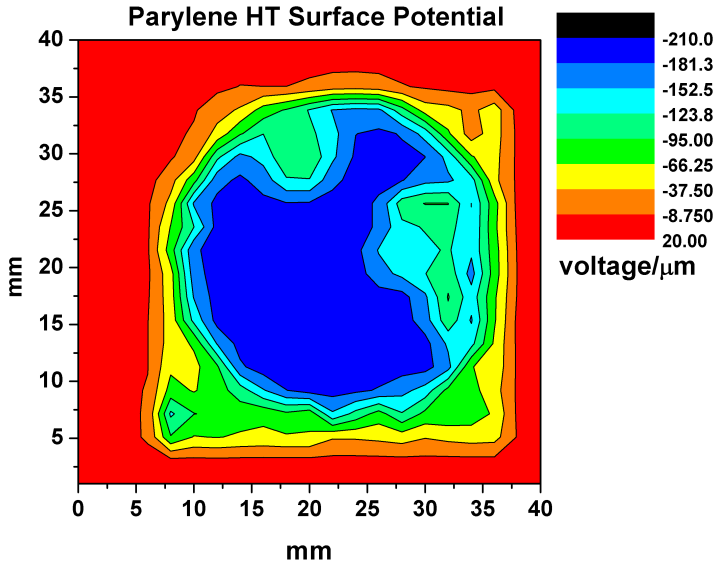


Figure B.5: The surface potential per μm of Parylene HT®.

To study the stability and long-term reliability of charged Parylene HT® films, Parylene HT® samples are first annealed in nitrogen ambient at 500 °C, 400 °C and 300 °C for 1 hour before charging and the change of surface potential over time were monitored. Samples are stored at the room temperature and 60 %RH. Figure B.6 shows the decaying of surface potential of Parylene HT® annealed at different temperature. The As-deposited Parylene HT® sample and the sample annealed at 500 °C show large initial drop of surface potential but maintain relatively stable values, around 65 % to 70 % of initial value. Meanwhile the surface charge density of the 400 °C-annealed sample dropped to 91 % of its initial value after 330 days. Since the measurement value scattered in a wide range, it is difficult to reach a solid conclusion of long-term reliability. However, this experiment still provides some information. To maintain as high power output as possible, 400 °C annealing may be a better choice since it could retain 91% of initial surface potential, although it shows continuous decreasing trend. In terms of stability and predictability, the As-deposited sample and 500 °C-annealed sample provide an edge over the other two. Although they have intial drops of surface potential, the As-deposited sample and the 500 °C-annealed sample show fairly stable surface potential after 75 days. From the viewpoint of engineering, it would be preferable to have devices generating a lower power but more stable in time than the opposite. In short, it requires more data to arrive at a clear and firm conclusion. Further testing and more accurate measurement are currently underway.

Thermally stimulated discharge (TSD) measurement are performed on charged Parylene HT® samples in order to understand their thermal stability and discharging mechanism. When an electret is heated, the dipoles and/or charges can be discharged at an accelerated rate depending on the temperature and the material. Therefore, during such a heat-stimulated discharge, an electret sandwiched between two electrodes can generate a discharging current that sometimes shows a number of peaks when recorded under a ramping temperature. The shape and peaks then reveal important information of the mechanisms by which the electret stores the charges. Here a modified TSD measurement is carried out. Both the discharging current and the surface potential are measured as a function of the ramping temperature. The measuring

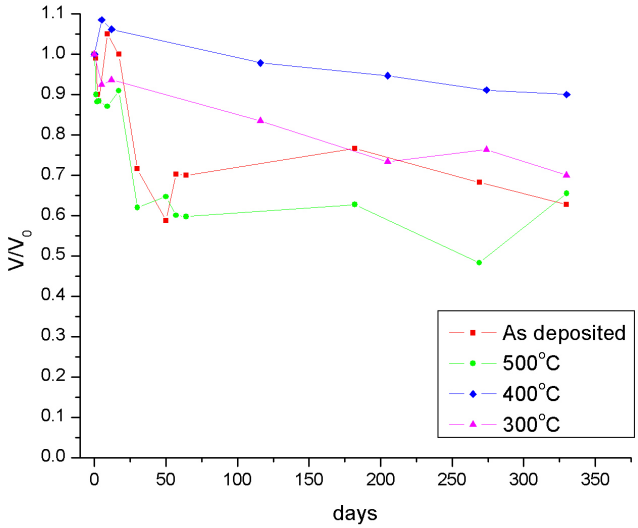
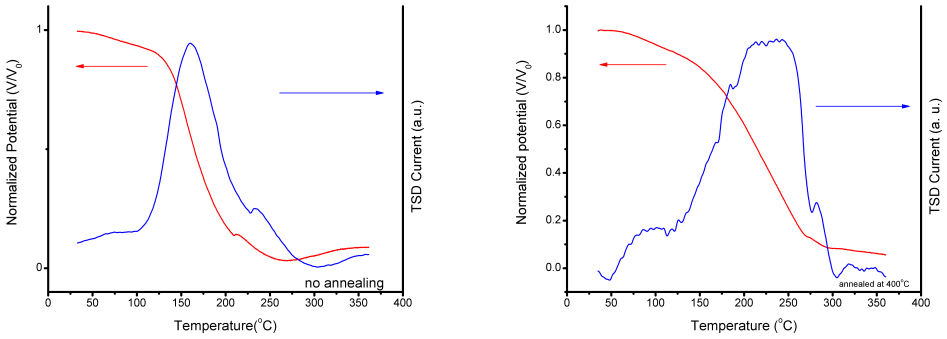


Figure B.6: Temporal change of surface potentials of Parylene HT® samples with different annealing treatment.

electrode is placed 1mm above the sample and current is measured with Keithley 485 autoranging picoammeter and surface potential is also monitored with Monroe Isoprobe. Samples are heated up at a rate of 1 °C/min. Figure B.7 shows the TSD current and surface potential of the non-annealed Parylene HT® sample and the Parylene HT® sample annealed at 400 °C for one hour before charging. The peak TSD current occurrs at around 160 °C for the Parylene HT® samples without annealing, and 230 °C for the samples annealed at 400 °C for one hour before charging. A higher TSD peak temperature means, a better the capability to withstand high temperature. It is found that pre-charging annealing improves high-temperature reliability of Parylene HT®. The mechanism is currently not well understood.

B.3.2 Parylene HT® Electret Power Generators

Generally, electrostatic power generators can be classified into 3 categories: variable in-plane overlap, variable in-plane gap and variable out-of-plane gap [2]. For micro electret power generators, a variable in-plane gap configuration (Figure B.8) has been widely used since the first



(a) As-deposited (b) Annealed at 400 °C

Figure B.7: Thermally stimulated discharge (TSD) measurement of Parylene HT® samples.

micro electret power generator[3]. The power output from such micro electret power generators is given by Equation B.1.

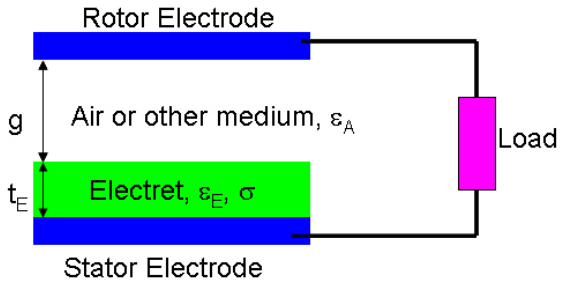


Figure B.8: Common design of micro electret power generators.

$$P_{MAX} = \frac{\sigma^2}{\frac{4\epsilon_0\epsilon_E}{t_E}\left(\frac{\epsilon_E g}{\epsilon_A t_E}+1\right)} \cdot \frac{\partial A}{\partial t}, \tag{B.1}$$

where σ is the surface charge density, ϵ_0 is the vacuum permittivity, ϵ_E is the dielectric constant of electret, ϵ_A is the dielectric constant of air (i.e., 1), g is the gap distance from the top electrode to the electret surface, t_E is the electret thickness, and A is the variable overlap area between the top and bottom electrodes.

From Equation B.1 , the power output of micro electret power generators depends on several factors, such as the gap distance, g, the thickness of electret material, t_E, etc. Typical values

of ϵ_E, the dielectric constant of polymer electrets are around 2 (2.2 for Parylene HT®, 2.1 for CYTOP, 1.9 for Teflon AF, and 2.1 for PTFE). Therefore, when the gap distance is larger than two times of the electret thickness, the gap distance plays a dominant role for the output power. To maximize the output power, it is desirable to have as small a gap distance relative to the thickness of the electret as possible. The largest state-of-the-art thickness of electrets is 20 μm of CYTOP, achieved by several consecutive spin-coatings [112]. With this constraint, the gap distance has to be controlled within around 50 μm. In [112], the gap distance is controlled to be 100 μm with precise x-y-z stages, while it is 500 nm in [114] with spin-coated polymer gasket, and 1000 μm in [111] with PDMS-formed chambers. The need for gap-controlling structures often complicates the generator design and fabrication.

A new design is used here. Different from the conventional variable in-plane gap design, this new design has both electrodes on the stator, as shown in Figure B.9. Figure B.9(a) is a device which uses a metal rotor and an electret-coated stator and Figure B.9(b) is a device using an electret-coated insulating rotor and a bare stator. Image charges on the electrodes are induced by the surface charges on the electret material. When the rotor moves from Figure B.10(a), (b) to (c), the final equilibrium image charges on the left electrode decrease, those on the right electrode increase, and a net current flows from the left electrode through the load to the right electrodes. Next, when the rotor moves from Figure B.10(c), (b) to (a), the current reverses and thus completes a power generation cycle. Based on this, two configurations are possible. One consists of a metal rotor and a stator covered with an electret, while the other is composed of an electret-coated rotor and a bare stator with output electrodes. Because the electret-coated rotor is made of insulators, the second configuration is expected to have larger power output since the induced charge density on the output electrodes is higher than that in the first configuration.

In these two designs, power is transduced into the load via charge induction and no gap control is required. Since no electrode is needed on the rotor, the rotor can be simply a moving object, made of metal or dielectric. One major advantage of this design is that thereÕs no

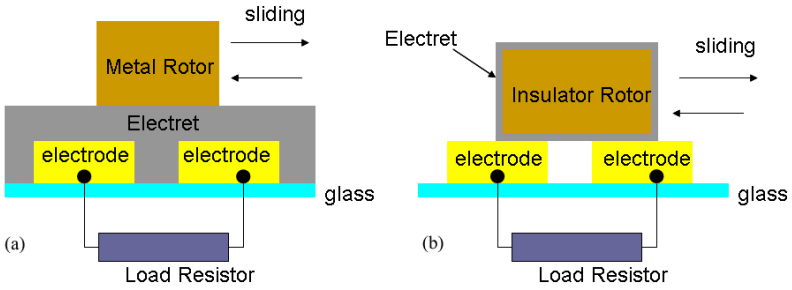


Figure B.9: New design of micro electret power generators.

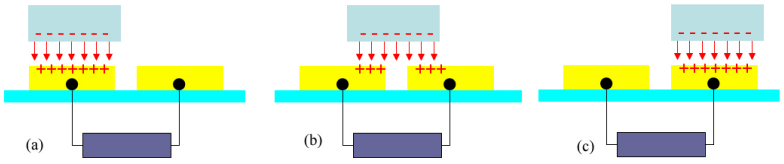


Figure B.10: Illustrated mechanism of power generation.

tethering spring attached to the rotor so there is not any mechanical resonance (i.e., resonant frequency near zero). This means that the generator can work at very low frequency as long as the relative motional force can break the frictional force induced by the attractive electrostatic force between the electret charges and their image charges on the electrodes.

To demonstrate the novel concept of electret power generation, we fabricated the prototypes with conventional machining processes, rather than microfabricating process. This facilitates us to conveniently and readily characterize the prototype devices and verify our theory of power generation. It is worth attention that future devices can be easily fabricated with microfabrication with little modification of the demonstrated prototype devices, although the prototype devices have large dimensions.

Fabrication of the generator using metal rotors started with soda lime glass wafers. 200 nm Au and 10 nm Cr were thermally evaporated and patterned as the power output electrodes via conventional photolithographic processes. The electrodes are 5 mm by 5 mm with 2 mm spacing for each cell. Next, the glass wafer was diced into 30-mm-by-30-mm stators. After dicing, 7.32 μm Parylene HT® is deposited on the stator. Similar to Parylene C and other Parylene

variant, Parylene HT® is deposited via the room temperature CVD process. After deposition, corona charging is done to implant electrons on Parylene HT®. Charging conditions are listed in Table B.3. The rotors are machined to be 4.5 mm by 4.5 mm by 2 mm (L by W by H) brass blocks. The container is also machined out of acrylic material. The final assembled device is shown in Figure B.11

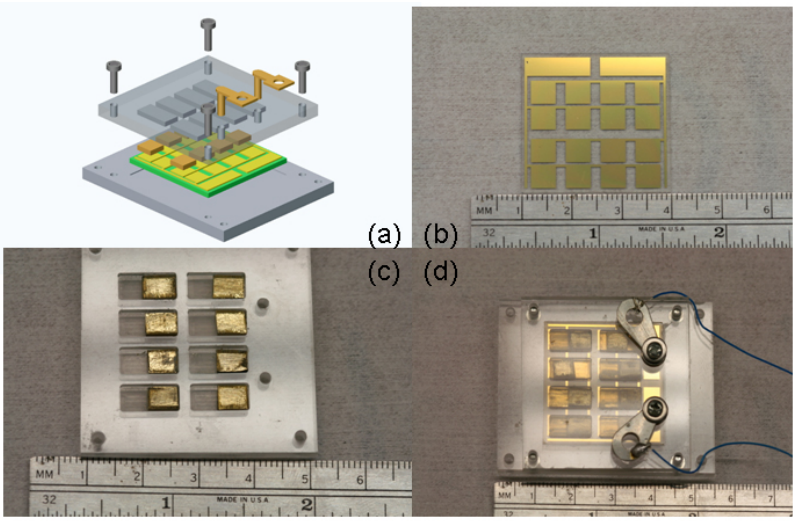


Figure B.11: The power generator with metal rotors.

The fabrication of the generator using PEEK rotors began with machining the polyetheretherketone (PEEK) rotor blocks. The dimensions of the rotor blocks are 5 mm by 6 mm by 9 mm (L by W by H). Same as the devices aforementioned, the stator is simply a piece of glass with patterned electrodes. 150 nm gold and 10 nm Chromium are deposited on soda lime wafers. The metal film is then patterned to be 5 mm by 5 mm square pads with conventional photolithography. A 7.32 μm of Parylene HT® is deposited onto the PEEK rotor, and then charged via corona charging. Charging conditions are also the same as in Table B.3. Figure B.12 shows the surface potential distribution of 8 pieces of PEEK rotor blocks after charging. An external acrylic packaging container was made to confine the movement of rotors. Figure B.13 shows the PEEK rotor block, the electrode stator and the device assembly.

The assembled generators were mounted onto a machined acrylic stage fixed to an electrodynamic shaker, as shown in Figure B.13(d). All necessary wires were soldered. Power generation

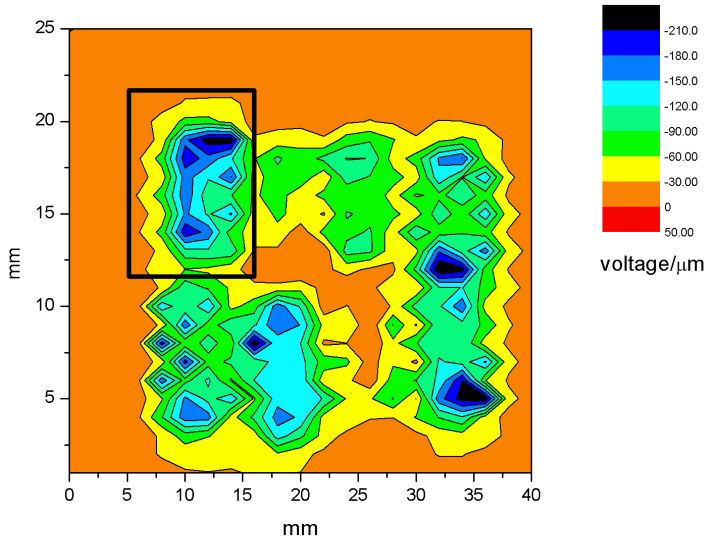


Figure B.12: The surface potential of Parylene HT® coated on PEEK rotor blocks. There are 8 PEEK blocks in the figure and one block is identified with a black rectangle frame.

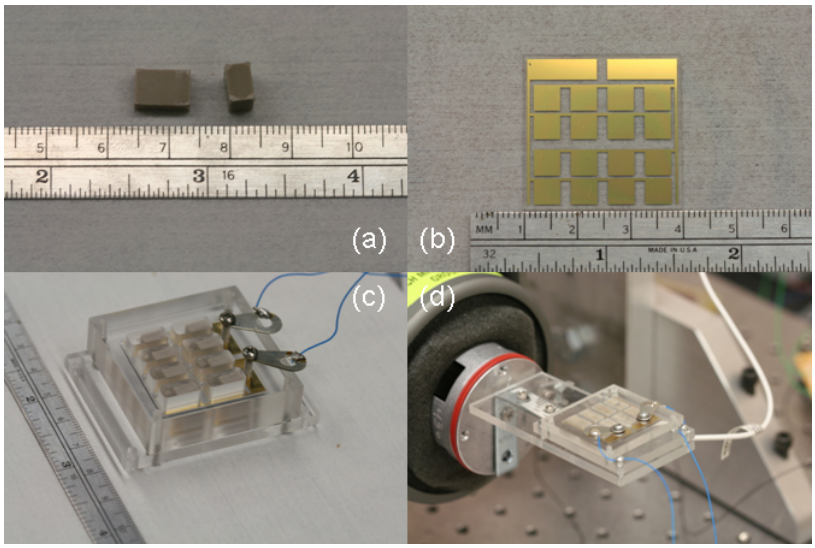


Figure B.13: The power generator with PEEK rotors.

experiments were performed using a Labworks Inc. ET-132-2 electrodynamic shaker, which was driven sinusoidally by a HP33120A function generator through a power amplifier. The acceleration of the power generator was measured with an Endevco256HX-10 accelerometer. The micro electret power generators were connected to resistive loads. In order to measure large output voltages, a simple two-resistor voltage divider was used as the load. The output voltage was measured through a National Semiconductor LF356N op-amp, a 1012-ohm input impedance voltage buffer. The maximal shaking amplitude, 5mm, was defined by the external packaging container. The frequency varied from 10Hz to 70Hz and the load resistance from 50 to 2,000 Mohm.

Figure B.14 and Figure B.15 show power outputs of both devices as a function of frequency. The maximum power output, 17.98 μW was obtained at 50Hz with an external load of 80 Mohm for the generator with Parylene HT®-coated PEEK rotors. As the devices are aimed to harvest power from natural vibrations, the low-frequency performance is of special interests. The generator with Parylene HT®-coated PEEK rotors can harvest 7.7 μW at 10Hz and 8.23 μW at 20Hz.

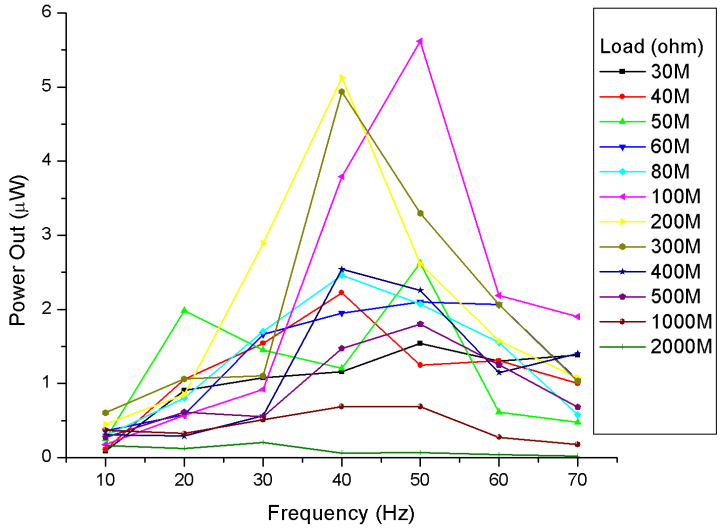


Figure B.14: The output power of the power generator with metal rotors.

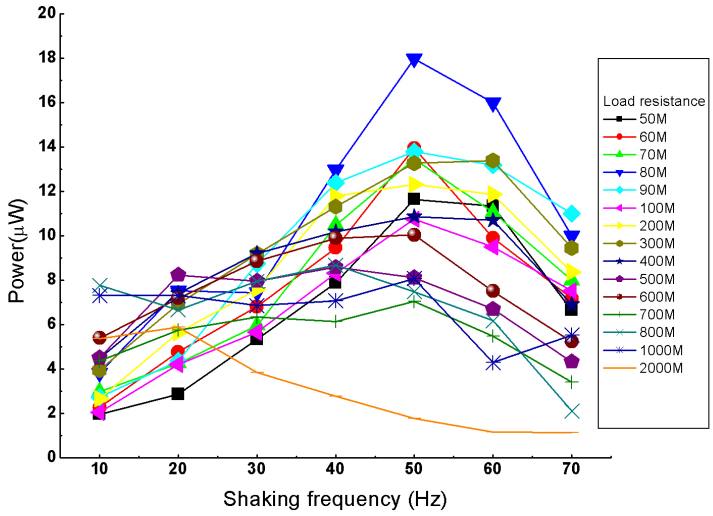


Figure B.15: The output power of the power generator with PEEK rotors.

As expected, the generator with PEEK rotors produces larger power than the one with metal rotors. The ratio is close to 4. This can be explained by the fact that the induced charge density on the electrodes of the generator with PEEK rotors is twice that of the generator with metal rotors. According to Equation B.1, power output is proportional to the square of charge density.

The device can fully deliver its power as designed only when the rotor moves completely from one electrode to the other, which is equivalent to the shaking amplitude of 5 mm. However, due to the limitation of the shaker, it was impossible to produce enough energy for the rotor to have 5 mm amplitudes at frequencies higher than 50Hz. According to the specifications of the ET-132-2 electrodynamic shaker, the maximum peak sine output force is 7 pound, equivalent to 31.136 Newton. The maximum acceleration the shaker could exert on the power generator assembly is around 576.6 m/s^2, since the power generator assembly has 54-gram mass. The maximum displacement of the shaker is 5.84 mm at 50 Hz, 4.05 mm at 60 Hz and 2.98 mm at 70 Hz (Displacement is calculated by assuming the shaking motion is ideal simple harmonic.) At higher frequencies, the rotor only moves in partially its supposed amplitude and hence the generator produces less power. Based on the information, we can say the shaker's failure to

provide enough shaking amplitude at frequencies higher than 50 Hz is at least a factor that the overall output power decreases in the frequency range higher than 50 Hz. This phenomenon results from the large dimensions of the rotors. It can be improved with smaller rotors, smaller confining chambers and thus smaller shaking amplitudes.

To correctly assess the capability of a micro power generator, power density should be used. For our devices, the total volume including the external container is 50 cm^3. Taking that into consideration, the power density of these devices is around 0.36 μW per cm^3 at 50Hz. It seemed very low. However, the first generation of these devices has a lot of unnecessary volume. Most of the unused volume comes from external package and the rotor blocks. To improve the power densities, one can carefully design an external packaging container that requires the least amount of volume. Besides, the PEEK rotors of the second device have a dimension of 5mm by 6mm by 9mm so that it has enough mass to overcome the electrostatic attraction forces between the rotor and stator electrodes during vibration. Choosing other insulating materials that have higher densities may further reduce the volume of the electret rotors and thus the total volume of the fabricated generator. Power density may further be improved. Large-area and stackable designs can also increase total power output.

Large optimal load resistance has always plagued electret-based power generators, preventing wide applications of such devices. Boland et al produced 25 μW with 7.6 MΩ [109], Tsutsumino et al produced 38 μW with 60 MΩ [112], and Sterken et al produced 5 μW with 40 MΩ [114]. It is the nature of electret power generators to produce outputs with large voltage but small current. We are currently actively looking for effective methods of power management that fits the special requirement of electret power generators. One possible and easy method would be connecting in parallel as many generator cells as possible to provide large enough current. There are only 8 cells in the prototype device. The more the cells are, the higher the power output is. Thus we can lower the load resistance while maintaining large enough power, although it is not optimal. Besides, shrinking the dimension of cells with microfabrication processes can increase the number of cells per devices and reduce the shaking amplitude,

generate higher current under the same condition, and thus lower the required load resistance while producing large enough power.

In short, a new electret based on the CVD Parylene HT® thin-film material is developed. The new Parylene HT® electret is studied in terms of process, stability, temperature reliability and optimization. The highest charge density observed of Parylene HT® was 3.69 mC/m^2, which is significantly higher than other polymer electrets. Annealing at 400 °C for 1 hour before charging greatly improved the long-term stability and high-temperature reliability of Parylene HT®. Two designs of electret generators were then fabricated and characterized. The maximum power output was 17.98 μW at 50 Hz with an external load of 80 Mohm. At low frequencies, this generator also produced decent power output such as 7.7μW at 10 Hz and 8.23μW at 20 Hz.

B.4 Conclusions

Parylene C and its other siblings of the Parylene family provide strong bases for Parylene surface micromachining technology. The Parylene micromachining technology has several advantages that result from its reliance on common MEMS/VLSI fabrication technologies.

Because this technology uses photolithography, devices made via this technology can be readily fabricated on large scales. Lithography also enables multi-layer processes without problems of alignments between layers. It is this capability of multi-layer processes that enables the Parylene surface micromachining technology to make a wide variety of devices of various complexity.

By sharing technologies with VLSI industries, devices made by the Parylene surface micromachining technology can be easily integrated into the current established fabrication processes of microelectronics. In addition, integration of various components made by this technology is no more difficult than fabrication of a single component.

One advantage that makes this technology unique and widely-used is the versatile properties

of Parylene. The low permeability, optical transparency, high mechanical strength, excellent dielectric properties, and biocompatibility of Parylene make it an perfect material for applications of MEMS and implantation.

References

[1] S. Wagner, H. Gleskova, I.-C. Cheng, and M. Wu, "Silicon for thin-film transistors," *Thin Solid Films, Proceedings of the Second International Conference on Cat-CVD (Hot Wire CVD) Process*, vol. 430, no. 1-2, pp. 15–19, Apr 2003.

[2] Y. Sun and J. A. Rogers, "Inorganic semiconductors for flexible electronics," *Adv. Mater.*, vol. 19, pp. 1897–1916, Jan 2007.

[3] A. Kahn, N. Koch, and W. Gao, "Electronic structure and electrical properties of interfaces between metals and π-conjugated molecular films," *Journal of Polymer Science*, Jan 2003. [Online]. Available: http://doi.wiley.com/10.1002/polb.10642

[4] Kamarinos, C. Angelis, C. Dimitriadis, and M. Miyasaka, "On-current modeling of large-grain polycrystalline silicon thin-film transistors," *Electron Devices*, Jan 2001. [Online]. Available: http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=915695

[5] R. Min and S. Wagner, "Nanocrystalline silicon thin-film transistors with 50-nm-thick deposited channel layer, 10 $cm^2v^{-1}s^{-1}$ electron mobility and 10^8 on/off current ratio," *Applied Physics A: Materials Science & Processing*, Jan 2002. [Online]. Available: http://www.springerlink.com/index/1BX2MQJ5Q8V1XQP4.pdf

[6] J. McWilliam, "Electrical stimulation of the heart in man," *British Medical Journal*, Jan 1889. [Online]. Available: http://www.pubmedcentral.nih.gov/articlerender.fcgi?artid=2154721

[7] M. Humayun, E. de Juan, G. Dagnelie, and R. Greenberg, "Visual perception elicited by electrical stimulation of retina in blind humans," *Archives of Ophthalmology*, Jan 1996. [Online]. Available: http://archopht.ama-assn.org/cgi/content/abstract/114/1/40

[8] D. Rodger and Y. Tai, "Microelectronic packaging for retinal prostheses," *Engineering in Medicine and Biology Magazine*, Jan 2005. [Online]. Available: http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=1511500

[9] A. Wang, P. Finlayson, J. Li, K. Brabant, and C. Black, "Is silicon suitable for making implantable biomedical devices," *AiChE 2005, Nanostructured Biomaterials*, Jan 2005. [Online]. Available: http://aiche.confex.com/aiche/2005/preliminaryprogram/abstract_15420.htm

[10] T. Brody, "The thin film transistor—a late flowering bloom," *Electron Devices, IEEE Transactions on*, vol. 31, no. 11, pp. 1614 – 1628, Jan 1984. [Online]. Available: http://ieeexplore.ieee.org/search/srchabstract.jsp?arnumber=1484047&isnumber=31908&punumber=16&k2dockey=1484047@ieeejrns

[11] O. Heil, "Improvements in or relating to electrical amplifiers and other control arrangements and devices," *British patent. BP439457*, 1935.

[12] P. Weimer, "The TFT – A new thin-film transistor," *Proceedings of the IRE*, vol. 50, no. 6, pp. 1462 – 1469, Jun 1962. [Online]. Available: http://ieeexplore.ieee.org/search/srchabstract.jsp?arnumber=4066878&isnumber=4066872&punumber=10933&k2dockey=4066878@ieeejrns

[13] T. Brody, J. Asars, and G. Dixon, "A 6 × 6 inch 20 lines-per-inch liquid-crystal display panel," *Electron Devices, IEEE Transactions on*, vol. 20, no. 11, pp. 995 – 1001, Jan 1973. [Online]. Available: http://ieeexplore.ieee.org/search/srchabstract.jsp?arnumber=1477437&isnumber=31717&punumber=16&k2dockey=1477437@ieeejrns

[14] P. L. Comber and W. Spear, "Electronic properties of doped amorphous Si and Ge," *AIP Conference Proceedings*, Jan 1976. [Online]. Available: http://link.aip.org/link/?APCPCS/31/284/1

[15] P. le Comber, W. Spear, and A. Ghaith, "Amorphous-silicon field-effect device and possible application," *Electron. Lett.*, vol. 15, no. 6, pp. 179–181, 1979. [Online]. Available: http://link.aip.org/link/?ELL/15/179/1

[16] C. Weber and J. Abelson, "Amorphous silicon buried-channel thin-film transistors," *Electron Devices*, Jan 1998. [Online]. Available: http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=658679

[17] M. Isomura, M. Kondo, and A. Matsuda, "Effects of hydrogen diluted silane plasma on amorphous silicon solar cells," *Jpn. J. Appl. Phys.*, vol. 39, no. 2000, pp. 4721–4726, Aug 2000. [Online]. Available: http://jjap.ipap.jp/link?JJAP/39/4721/

[18] S. Guha, J. Yang, A. Banerjee, B. Yan, and K. Lord, "High quality amorphous silicon materials and cells grown with hydrogen dilution." *Solar Energy Materials and Solar Cells*, Jan 2003. [Online]. Available: http://www.uni-solar.com/uploadedFiles/0.4.2_white_paper_6.pdf

[19] A. Sazonov and A. Nathan, "120°C fabrication technology for a-Si:H thin film transistors on flexible polyimide substrates," *Journal of Vacuum Science & Technology A: Vacuum*, Jan 2000. [Online]. Available: http://link.aip.org/link/?JVTAD6/18/780/1

[20] A. Sazonov, D. Striakhilev, C.-H. Lee, and A. Nathan, "Low-temperature materials and thin film transistors for flexible electronics," *Proceedings of the IEEE*, vol. 93, no. 8, pp. 1420–1428, Aug 2005. [Online]. Available: http://ieeexplore.ieee.org/search/wrapper.jsp?arnumber=1468597

[21] A. Sazonov and C. McArthur, "Sub-100°C a-Si:H thin-film transistors on plastic substrates with silicon nitride gate dielectrics," *Journal of Vacuum Science & Technology A: Vacuum*, Jan 2004. [Online]. Available: http://link.aip.org/link/?JVTAD6/22/2052/1

[22] I. Cheng and S. Wagner, "Hole and electron field-effect mobilities in nanocrystalline silicon deposited at 150°C," *Applied Physics Letters*, Jan 2002. [Online]. Available: http://link.aip.org/link/?APPLAB/80/440/1

[23] C. McCormick, C. Weber, J. Abelson, and S. Gates, "An amorphous silicon thin film transistor fabricated at 125°C by DC reactive magnetron sputtering," *Appl Phys Lett*, vol. 70, pp. 226–227, Jan 1997.

[24] J. Conde, P. Alpuim, and V. Chu, "Hot-wire thin-film transistors on PET at 100°C," *Thin Solid Films*, Jan 2003. [Online]. Available: http://linkinghub.elsevier.com/retrieve/pii/S0040609003001159

[25] I. Cheng and S. Wagner, "High hole and electron field effect mobilities in nanocrystalline silicon deposited at 150°C," *Thin Solid Films*, Jan 2003. [Online]. Available: http://linkinghub.elsevier.com/retrieve/pii/S0040609002012439

[26] C. Lee, A. Sazonov, A. Nathan, and J. Robertson, "Directly deposited nanocrystalline silicon thin-film transistors with ultra high mobilities," *Applied Physics Letters*, Jan 2006. [Online]. Available: http://link.aip.org/link/?APPLAB/89/252101/1

[27] M. Wu, K. Pangal, J. Sturm, and S. Wagner, "High electron mobility polycrystalline silicon thin-film transistors on steel foil substrates," *Applied Physics Letters*, Jan 1999. [Online]. Available: http://link.aip.org/link/?APPLAB/75/2244/1

[28] S.-W. Lee and S.-K. Joo, "Low temperature poly-Si thin-film transistor fabrication by metal-induced lateral crystallization," *Electron Device Letters, IEEE*, vol. 17, no. 4, pp. 160–162, 1996.

[29] A. Joshi and K. Saraswat, "High performance submicrometer CMOS with metal induced lateral crystallization of amorphous silicon," *Journal of The Electrochemical Society*, Jan 2003. [Online]. Available: http://link.aip.org/link/?JESOAN/150/G443/1

[30] S. Lee, Y. Jeon, and S. Joo, "Pd induced lateral crystallization of amorphous Si thin films," *Applied Physics Letters*, Jan 1995. [Online]. Available: http://link.aip.org/link/?APPLAB/66/1671/1

[31] L. Pereira, H. águas, P. Vilarinho, and E. Fortunato, "Metal induced crystallization: Gold versus aluminium," *Journal of Materials Science*, Jan 2005. [Online]. Available: http://www.springerlink.com/index/V7247W2G323137UH.pdf

[32] Y.-C. Her and C.-W. Chen, "Crystallization kinetics of ultrathin amorphous Si film induced by Al metal layer under thermal annealing and pulsed laser irradiation," *Journal of Applied Physics*, vol. 101, no. 4, p. 043518, Jan 2007.

[33] L. Pereira, "Polycrystalline silicon obtained by gold metal induced crystallization," *Journal of Non-Crystalline Solids*, vol. 338-340, pp. 178–182, Jun 2004.

[34] K. Lee, Y. Fang, and S. Fan, "Au metal-induced lateral crystallisation (milc) of hydrogenated amorphous silicon thin film with very low annealing temperature and fast milc rate," *Electron. Lett.*, vol. 35, no. 13, p. 1108, Jan 1999.

[35] K. Sera, F. Okumura, H. Uchida, S. Itoh, S. Kaneko, and K. Hotta, "High-performance TFTs fabricated by XeCl excimer laser annealing of hydrogenated amorphous-silicon film," *Electron Devices, IEEE Transactions on*, vol. 36, no. 12, pp. 2868–2872, 1989.

[36] S. Theiss, P. Carey, P. Smith, P. Wickboldt, T. Sigmon, Y. Tung, and T.-J. King, "Polysilicon thin film transistors fabricated at 100°C on a flexible plastic substrate," *Electron Devices Meeting, 1998. IEDM '98 Technical Digest., International*, pp. 257–260, 1998.

[37] P. G. Carey, P. M. Smith, S. D. Theiss, and P. Wickboldt, "Polysilicon thin film transistors fabricated on low temperature plastic substrates," *J. Vac. Sci. Technol. A*, vol. 17, no. 4, pp. 1946–1949, 1999. [Online]. Available: http://link.aip.org/link/?JVA/17/1946/1

[38] E. Fortunato, P. Barquinha, and A. Pimentel, "Wide-bandgap high-mobility ZnO thin-film transistors produced at room temperature," *Applied Physics Letters*, Jan 2004. [Online]. Available: http://link.aip.org/link/?APPLAB/85/2541/1

[39] K. Nomura, A. Takagi, T. Kamiya, H. Ohta, and M. Hirano, "Amorphous oxide semiconductors for high-performance flexible thin-film transistors," *Jpn. J. Appl. Phys.*, Jan 2006. [Online]. Available: http://jjap.ipap.jp/link?JJAP/45/4303/

[40] T. Brody, "The thin film transistor—a late flowering bloom," *Electron Devices*, Jan 1984. [Online]. Available: http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=1484047

[41] G. Heilmeier and L. Zanoni, "Surface studies of alpha-copper phthalocyanine films," *J. Phys. Chem. Solids*, Jan 1964. [Online]. Available: http://adsabs.harvard.edu/abs/1964JPCS...25..603H

[42] Z. Bao, A. Lovinger, and A. Dodabalapur, "Organic field effect transistors with high mobility based on copper phthalocyanine," *Applied Physics Letters*, Jan 1996. [Online]. Available: http://link.aip.org/link/?APPLAB/69/3066/1

[43] R. Zeis, T. Siegrist, and C. Kloc, "Single-crystal field-effect transistors based on copper phthalocyanine," *Arxiv preprint cond-mat*, Jan 2004. [Online]. Available: http://arxiv.org/abs/cond-mat/0409353

[44] A. Dodabalapur, L. Torsi, and H. Katz, "Organic transistors: Two-dimensional transport and improved electrical characteristics," *Science*, Jan 1995. [Online]. Available: http://www.sciencemag.org/cgi/content/abstract/sci;268/5208/270

[45] H. Katz, L. Torsi, and A. Dodabalapur, "Synthesis, material properties, and transistor performance of highly pure thiophene oligomers," *Chemistry of Materials*, Jan 1995.

[Online]. Available: http://pubs.acs.org/cgi-bin/abstract.cgi/cmatex/1995/7/i12/f-pdf/f_cm00060a007.pdf?sessid=6006l3

[46] D. Fichou, G. Horowitz, and F. Garnier, "Extended oligothiophenes: New materials for molecular electronics," *Molecular Crystals and Liquid Crystals*, Jan 1992. [Online]. Available: http://www.informaworld.com/index/757805099.pdf

[47] J. Schön, C. Kloc, and B. Batlogg, "On the intrinsic limits of pentacene field-effect transistors," *Organic Electronics*, Jan 2000. [Online]. Available: http://linkinghub.elsevier.com/retrieve/pii/S1566119900000100

[48] D. Knipp, R. Street, A. Völkel, and J. Ho, "Pentacene thin film transistors on inorganic dielectrics: Morphology, structural properties, and electronic transport," *Journal of Applied Physics*, Jan 2002. [Online]. Available: http://link.aip.org/link/?JAPIAU/93/347/1

[49] J. H. Lee, S. H. Kim, G. H. Kim, S. C. Lim, H. Lee, J. Jang, and T. Zyung, "Pentacene thin film transistors fabricated on plastic substrates," *Synthetic Metals*, vol. 139, no. 2, pp. 445–451, 2003. [Online]. Available: http://www.sciencedirect.com/science/article/B6TY7-48WB7H2-1/1/57852c25dadcec2fcbb1017d1035fd08

[50] D. Ender, D. Muyres, M. Haase, D. Vogel, and S. Theiss, "Recent progress in organic electronics: Materials, devices, and processes," *Chem. Mater*, Jan 2004. [Online]. Available: http://www.faculty.iu-bremen.de/course/c300442/Info/kelley%2520rfid.pdf

[51] O. Jurchescu, J. Baas, and T. Palstra, "Effect of impurities on the mobility of single crystal pentacene," *Applied Physics Letters*, Jan 2004. [Online]. Available: http://link.aip.org/link/?APPLAB/84/3061/1

[52] P. Sullivan and T. Jones, "Pentacene/fullerene (C_{60}) heterojunction solar cells: Device performance and degradation mechanisms," *Organic Electronics*, Jan 2008. [Online]. Available: http://linkinghub.elsevier.com/retrieve/pii/S1566119908000815

[53] A. Afzali, C. Dimitrakopoulos, and T. Breen, "High-performance, solution-processed organic thin film transistors from a novel pentacene precursor," *J. Am. Chem. Soc*, Jan 2002. [Online]. Available: http://pubs.acs.org/cgi-bin/abstract.cgi/jacsat/2002/124/i30/abs/ja0266621.html

[54] S. Wagner, S. Fonash, T. Jackson, and J. Sturm, "Flexible display enabling technology," *Cockpit Displays VIIIL Displays for Defense Applications*, Jan 2001. [Online]. Available: http://prism.princeton.edu/Sturm_publications/CP.188.SPIE.2001.pdf

[55] H. Sirringhaus, P. Brown, R. Friend, and M. Nielsen, "Two-dimensional charge transport in self-organized, high-mobility conjugated polymers," *Nature*, Jan 1999. [Online]. Available: http://www.nature.com/nature/journal/v401/n6754/pubmed/401685a0.html

[56] G. Wang, J. Swensen, D. Moses, and A. Heeger, "Increased mobility from regioregular poly (3-hexylthiophene) field-effect transistors," *Journal of Applied Physics*, Jan 2003. [Online]. Available: http://link.aip.org/link/?JAPIAU/93/6137/1

[57] K. Paul, W. Wong, S. Ready, and R. Street, "Additive jet printing of polymer thin-film transistors," *Applied Physics Letters*, Jan 2003. [Online]. Available: http://link.aip.org/link/?APPLAB/83/2070/1

[58] G. Horowitz, R. Hajlaoui, D. Fichou, and A. E. Kassmi, "Gate voltage dependent mobility of oligothiophene field-effect transistors," *Journal of Applied Physics*, Jan 1999. [Online]. Available: http://link.aip.org/link/?JAPIAU/85/3202/1

[59] M. Halik, H. Klauk, U. Zschieschang, G. Schmid, W. Radlik, S. Ponomarenko, S. Kirchmeyer, and W. Weber, "High-mobility organic thin-film transistors based on α,α'-didecyloligothiophenes," *J Appl Phys*, vol. 93, pp. 2977–2981, Jan 2003.

[60] G. Horowitz, F. Garnier, and A. Yassar, "Field-effect transistor made with a sexithiophene single crystal," *Chem. Phys*, Jan 1993. [Online]. Available: http://doi.wiley.com/10.1002/adma.19960080109

[61] V. Podzorov, S. Sysoev, E. Loginova, and V. Pudalov, "Single-crystal organic field effect transistors with the hole mobility ~ 8 cm^2/vs," *Applied Physics Letters*, Jan 2003. [Online]. Available: http://link.aip.org/link/?APPLAB/83/3504/1

[62] V. Butko, X. Chi, D. Lang, and A. Ramirez, "Field-effect transistor on pentacene single crystal," *Applied Physics Letters*, Jan 2003. [Online]. Available: http://link.aip.org/link/?APPLAB/83/4773/1

[63] G. Horowitz, "Organic thin film transistors: From theory to real devices," *Journal of Materials Research*, Jan 2004. [Online]. Available: http://www.mrs.org/s_mrs/bin.asp?CID=1655&DID=50233&DOC=FILE.PDF

[64] S. Kobayashi, T. Takenobu, S. Mori, and A. Fujiwara, "Fabrication and characterization of C_{60} thin-film transistors with high field-effect mobility," *Applied Physics Letters*, Jan 2003. [Online]. Available: https://dspace.jaist.ac.jp/dspace/bitstream/10119/3364/1/131-11.pdf

[65] P. Malenfant, C. Dimitrakopoulos, and J. Gelorme, "N-type organic thin-film transistor with high field-effect mobility based on a N,N-dialkyl-3, 4, 9, 10-perylene tetracarboxylic diimide derivative," *Applied Physics Letters*, Jan 2002. [Online]. Available: http://link.aip.org/link/?APPLAB/80/2517/1

[66] H. Klauk, U. Zschieschang, J. Pflaum, and M. Halik, "Ultralow-power organic complementary circuits," *Nature*, Jan 2007. [Online]. Available: http://www.fkf.mpg.de/oe/publications/pdfs/Klauk-Nature-2007-745.pdf

[67] M. Wu, K. Pangal, J. C. Sturm, and S. Wagner, "High electron mobility polycrystalline silicon thin-film transistors on steel foil substrates," *Applied Physics Letters*, vol. 75, no. 15, pp. 2244–2246, 1999. [Online]. Available: http://link.aip.org/link/?APL/75/2244/1

[68] E. Y. Ma and S. Wagner, "Amorphous silicon transistors on ultrathin steel foil substrates," *Applied Physics Letters*, vol. 74, no. 18, pp. 2661–2662, 1999. [Online]. Available: http://link.aip.org/link/?APL/74/2661/1

[69] Y. Chen, J. Au, P. Kazlas, A. Ritenour, H. Gates, and M. McCreary, "Electronic paper: Flexible active-matrix electronic ink display," *Nature*, vol. 423, no. 6936, pp. 136–136, 2003, 10.1038/423136a. [Online]. Available: http://dx.doi.org/10.1038/423136a

[70] P. I. Hsu, R. Bhattacharya, H. Gleskova, M. Huang, Z. Xi, Z. Suo, S. Wagner, and J. C. Sturm, "Thin-film transistor circuits on large-area spherical surfaces," *Applied Physics Letters*, vol. 81, no. 9, pp. 1723–1725, 2002, bending. [Online]. Available: http://link.aip.org/link/?APL/81/1723/1

[71] S. Theiss, P. Carey, P. Smith, P. Wickboldt, T. Sigmon, Y. Tung, and T.-J. King, "Polysilicon thin film transistors fabricated at 100°C on a flexible plastic substrate," *Electron Devices Meeting, 1998. IEDM '98 Technical Digest., International*, pp. 257–260, Dec 1998. [Online]. Available: http://ieeexplore.ieee.org/search/wrapper.jsp?arnumber=746349

[72] M. J. Lee, C. P. Judge, and S. W. Wright, "Thin film transistors for displays on plastic substrates," *Solid-State Electronics*, vol. 44, no. 8, pp. 1431–1434, 2000. [Online]. Available: http://www.sciencedirect.com/science/article/B6TY5-40NFSRX-G/1/80e455dbaf113d0af214794142efc3e9

[73] H. Klauk, M. Halik, U. Zschieschang, F. Eder, G. Schmid, and C. Dehm, "Pentacene organic transistors and ring oscillators on glass and on flexible polymeric substrates," *Applied Physics Letters*, vol. 82, no. 23, pp. 4175–4177, 2003. [Online]. Available: http://link.aip.org/link/?APL/82/4175/1

[74] G. H. Gelinck, T. C. T. Geuns, and D. M. de Leeuw, "High-performance all-polymer integrated circuits," *Applied Physics Letters*, vol. 77, no. 10, pp. 1487–1489, 2000. [Online]. Available: http://link.aip.org/link/?APL/77/1487/1

[75] F. Eder, H. Klauk, M. Halik, U. Zschieschang, G. Schmid, and C. Dehm, "Organic electronics on paper," *Applied Physics Letters*, vol. 84, no. 14, pp. 2673–2675, 2004. [Online]. Available: http://link.aip.org/link/?APL/84/2673/1

[76] H. Yamada, Y. Yamashita, M. Kikuchi, and H. Watanabe, "Photochemical synthesis of pentacene and its derivatives," *CHEMISTRY-WEINHEIM-EUROPEAN JOURNAL-*, Jan 2005. [Online]. Available: http://doi.wiley.com/10.1002/chem.200500564

[77] C. Rolin, S. Steudel, K. Myny, D. Cheyns, and S. Verlaak, "Pentacene devices and logic gates fabricated by organic vapor phase deposition," *Applied Physics Letters*, Jan 2006. [Online]. Available: http://link.aip.org/link/?APPLAB/89/203502/1

[78] L. Burgi, T. J. Richards, R. H. Friend, and H. Sirringhaus, "Close look at charge carrier injection in polymer field-effect transistors," *Journal of Applied Physics*, vol. 94, no. 9, pp. 6129–6137, 2003. [Online]. Available: http://link.aip.org/link/?JAP/94/6129/1

[79] S. C. Lim, S. H. Kim, J. H. Lee, H. Y. Yu, Y. Park, D. Kim, and T. Zyung, "Organic thin-film transistors on plastic substrates," *Materials Science and Engineering B*, vol. 121, no. 3, pp. 211–215, 2005. [Online]. Available: http://www.sciencedirect.com/science/article/B6TXF-4GBD6SR-1/1/7d5d6487fb2a915cd8f7937c485f149e

[80] N. Yoneya, M. Noda, N. Hirai, K. Nomoto, M. Wada, and J. Kasahara, "Reduction of contact resistance in pentacene thin-film transistors by direct carrier injection into a-few-molecular-layer channel," *Applied Physics Letters*, vol. 85, no. 20, pp. 4663–4665, 2004. [Online]. Available: http://link.aip.org/link/?APL/85/4663/1

[81] Y. Lin, D. Gundlach, S. Nelson, and T. Jackson, "High-mobility pentacene-based organic thin film transistors," *Device Research Conference Digest*, Jan 1997. [Online]. Available: http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=612475

[82] Y. Lin, D. Gundlach, S. Nelson, and T. Jackson, "Stacked pentacene layer organic thin-film transistors with improvedcharacteristics," *Electron Device Letters*, Jan 1997. [Online]. Available: http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=644085

[83] S. J. Kang, M. Noh, D. S. Park, H. J. Kim, C. N. Whang, and C.-H. Chang, "Influence of postannealing on polycrystalline pentacene thin film transistor," *Journal of Applied Physics*, vol. 95, no. 5, pp. 2293–2296, 2004. [Online]. Available: http://link.aip.org/link/?JAP/95/2293/1

[84] D. Guo, S. Ikeda, K. Saiki, H. Miyazoe, and K. Terashima, "Effect of annealing on the mobility and morphology of thermally activated pentacene thin film transistors," *Journal of Applied Physics*, vol. 99, no. 9, p. 094502, 2006. [Online]. Available: http://link.aip.org/link/?JAP/99/094502/1

[85] T. Harder, T. Yao, Q. He, C. Shih, and Y. Tai, "Residual stress in thin-film Parylene C," *Micro Electro Mechanical Systems*, Jan 2002. [Online]. Available: http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=984296

[86] J. Northrup and M. Chabinyc, "Gap states in organic semiconductors: Hydrogen- and oxygen-induced states in pentacene," *Physical Review B*, Jan 2003. [Online]. Available: http://link.aps.org/doi/10.1103/PhysRevB.68.041202

[87] Y. Tai and R. Muller, "Fracture strain of LPCVD polysilicon," *Solid-State Sensor and Actuator Workshop*, Jan 1988. [Online]. Available: http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=26440

[88] H. Gleskova and S. Wagner, "Amorphous silicon thin-film transistors on compliant polyimide foil substrates," *Electron Device Letters, IEEE*, vol. 20, no. 9, pp. 473–475, 1999.

[89] K. Pangal, J. C. Sturm, and S. Wagner, "Hydrogen plasma enhanced crystallization of hydrogenated amorphous silicon films," *Journal of Applied Physics*, vol. 85, no. 3, 1999.

[90] M. Kondo, M. Fukawa, L. Guo, and A. Matsuda, "High rate growth of microcrystalline silicon at low temperatures," *Journal of Non-Crystalline Solids*, Jan 2000. [Online]. Available: http://linkinghub.elsevier.com/retrieve/pii/S0022309399007449

[91] C. Weber and J. Abelson, "Amorphous silicon buried-channel thin-film transistors," *Electron Devices, IEEE Transactions on*, vol. 45, no. 2, pp. 447–452, 1998.

[92] D. Bernstein, S. Qin, C. Chan, and T. King, "Hydrogenation of polycrystalline silicon thin-film transistors by plasma ion-implantation," *Ieee Electr Device L*, vol. 16, pp. 421–423, Jan 1995.

[93] H. Jin, K. Weber, P. Deenapanray, and A. Blakers, "Hydrogen reintroduction by forming gas annealing to LPCVD silicon nitride coated structures," *Journal of The Electrochemical Society*, vol. 153, pp. G750–G754, Jan 2006.

[94] K. Williams and R. Muller, "Etch rates for micromachining processing," *Microelectromechanical Systems*, Jan 1996. [Online]. Available: http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=546406

[95] K. Williams, K. Gupta, and M. Wasilik, "Etch rates for micromachining processing - Part II," *Microelectromechanical Systems*, Jan 2003. [Online]. Available: http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=1257354

[96] B. Schwartz and H. Robbins, "Chemical etching of silicon," *Journal of The Electrochemical Society*, Jan 1976. [Online]. Available: http://link.aip.org/link/?JESOAN/123/1903/1

[97] H. Lo, W. Kuo, Y. Yang, and Y. Tai, "Recrystallized parylene as a mask for silicon chemical etching," *Nano/Micro Engineered and Molecular Systems*, Jan 2008. [Online]. Available: http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=4484464

[98] H. Seidel, "The mechanism of anisotropic, electrochemical silicon etching in alkaline solutions," *Solid-State Sensor and Actuator Workshop*, Jan 1990. [Online]. Available: http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=109827

[99] M. Szwarc, "Some remarks on the CH_2 [graphic omitted] CH_2 molecule," *Discussions of the Faraday Society*, Jan 1947. [Online]. Available: http://www.rsc.org/Publishing/Journals/DF/article.asp?doi=DF9470200046

[100] J. Xie, Y. Miao, J. Shih, Q. He, J. Liu, and Y. Tai, "An electrochemical pumping system for on-chip gradient generation," *Anal. Chem*, Jan 2004. [Online]. Available: http://pubs.acs.org/cgi-bin/abstract.cgi/ancham/2004/76/i13/abs/ac035188u.html

[101] X. Wang and Y. Tai, "A normally closed in-channel micro check valve," *Micro Electro Mechanical Systems*, Jan 2000. [Online]. Available: http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=838492

[102] E. Meng, S. Gassmann, and Y. Tai, "A mems body fluid flow sensor," *Micro Total Analysis Systems 2001*, Jan 2001. [Online]. Available: http://biomems.usc.edu/papers/2001_uTAS_flow_sensor.pdf

[103] J. Xie, J. Shih, and Y. Tai, "Integrated surface-micromachined mass flow controller," *Micro Electro Mechanical Systems*, Jan 2003. [Online]. Available: http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=1189677

[104] L. Licklider, X. Wang, A. Desai, Y. Tai, and T. Lee, "A micromachined chip-based electrospray source for mass spectrometry," *Analytical Chemistry*, Jan 2000. [Online]. Available: http://pubs.acs.org/cgi-bin/abstract.cgi/ancham/2000/72/i02/abs/ac990967p.html

[105] H. Noh, P. Hesketh, and G. Frye-Mason, "Parylene gas chromatographic column for rapid thermal cycling," *Microelectromechanical Systems*, Jan 2002. [Online]. Available: http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=1097792

[106] C. Raschke and T. Nowlin, "Polyparaxylylene electrets usable at high temperatures," *Journal of Applied Polymer Science*, vol. 25, pp. 1639–1644, 1980.

[107] W. Hsieh, T. Hsu, and Y. Tai, "A micromachined thin-film teflon electret microphone," *TRANSDUCERS '97, Solid-State Sensors and Actuators*, vol. 1, p. 2B2.02, 1997.

[108] W. Hsieh, T.-J. Yao, and Y.-C. Tai, "A high performance mems thin-film teflon electret microphone," *TRANSDUCERS '99 The 10th International Conference on Solid-State Sensors and Actuators*, vol. 2, pp. 1064–1067, 1999.

[109] J. Boland, Y. Chao, Y. Suzuki, Y. Tai, and Y. Suzuki, "Micro electret power generator," *Micro Electro Mechanical Systems, 2003. MEMS-03 Kyoto. IEEE The Sixteenth Annual International Conference on*, pp. 538–541, 2003.

[110] J. Boland and Y. Tai, "Liquid-rotor electret micropower generator," *Solid-State Sensor, Actuator, and Microsystems Workshop*, 2004.

[111] J. Boland, J. Messenger, H. Lo, and Y. Tai, "Arrayed liquid rotor electret power generator systems," *Micro Electro Mechanical Systems, 2005. MEMS 2005. 18th IEEE International Conference on*, pp. 618–621, 2005.

[112] T. Tsutsumino, Y. Suzuki, N. Kasagi, and Y. Sakane;, "Seismic power generator using high-performance polymer electret," *Micro Electro Mechanical Systems, 2006. MEMS 2006 Istanbul. 19th IEEE International Conference on*, pp. 98 – 101, Jan 2006. [Online]. Available: http://ieeexplore.ieee.org/search/srchabstract.jsp?arnumber=1627745&isnumber=34154&punumber=10836&k2dockey=1627745@ieeecnfs

[113] T. Tsutsumino, Y. Suzuki, N. Kasagi, Y. Suzuki, and N. Kasagi, "Electromechanical modeling of micro electret generator for energy harvesting," *Solid-State Sensors, Actuators and Microsystems Conference, 2007. TRANSDUCERS 2007. International*, pp. 863–866, 2007.

[114] T. Sterken, P. Fiorini, G. Altena, C. V. Hoof, R. Puers, P. Fiorini, and G. Altena, "Harvesting energy from vibrations by a micromachined electret generator," *Solid-State Sensors, Actuators and Microsystems Conference, 2007. TRANSDUCERS 2007. International*, pp. 129–132, 2007.

[115] T. Sterken, P. Fiorini, K. Baert, R. Puers, G. Borghs, P. Fiorini, and K. Baert, "An electret-based electrostatic μ-generator," *TRANSDUCERS, Solid-State Sensors, Actuators and Microsystems, 12th International Conference on, 2003*, vol. 2, pp. 1291–1294, 2003.

[116] H. Amjadi, "Charge storage in double layers of silicon dioxide and silicon nitride," *Electrets*, Jan 1996. [Online]. Available: http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=578033

[117] W. Hsieh, T. Hsu, and Y. Tai, "A micromachined thin-film teflon electret microphone," *Solid State Sensors and Actuators*, Jan 1997. [Online]. Available: http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=613676