Radial pn Junction, Wire Array Solar Cells

Thesis by
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To my father, Terence John Kayes, for instilling in me the curiosity that was necessary to get this far...

Acknowledgements

I was recently reminded of an email I sent to my parents way back in January 2003, in the core of which I wrote "I just spoke to Harry Atwater on the phone while he was driving to Boston from NYC, and him [sic] and Nate have put their heads together and cooked me up what looks like a beauty of a research project. Basically, Harry wants me to design and work out how to build and I guess hopefully build a third generation silicon cell which will take the manufacturing experience of his silicon lab and marry it with the exciting new possibilities afforded by recent work in chemical solar cells. So, apparently, truly somewhere in between Nate's and Harry's work, while still allowing me to keep my feet firmly planted in "Applied Physics" (and thus avoid that dirty world of Chemistry). He was talking [about] getting me an office, starting to review papers with me, learning semiconductor device physics over the summer, . . .I'm super excited". I make no claim to have worked on a "third generation" [1] device in this thesis, but other than that I'm struck by how little has changed since then (particularly with regards to Harry's ever-busy travel schedule).

First and foremost I would like to acknowledge the guidance and support of my two advisors, Harry Atwater and Nate Lewis. I don't even know where to begin, except to say that virtually everything I know about that which I'm now trying to make a career out of, namely semiconductors, solar energy conversion, etc. etc. etc., I owe it to these two men. Their encouragement, the challenges they have set for me, the insights, the opportunities - all have contributed to making me feel truly like a different person from who I was when I arrived at Caltech.

I would like to thank my candidacy and thesis committees, which, in addition to my advisors, have been composed of Marc Bockrath, Oskar Painter, Ken Pickar, and Rachid Yazami in various combinations. I would also like to thank all of the other Caltech faculty from whom I took classes while here. Particularly I would like to acknowledge the great teaching skills of Alan Weinstein, Oskar Painter, and Rob Phillips.

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Abstract

Radial pn junctions are potentially of interest in photovoltaics as a way to decouple light absorption from minority carrier collection. In a traditional planar design these occur in the same dimension, and this sets a lower limit on absorber material quality, as cells must both be thick enough to effectively absorb the solar spectrum while also having minority-carrier diffusion lengths long enough to allow for efficient collection of the photo-generated carriers. Therefore, highly efficient photovoltaic devices currently require highly pure materials and expensive processing techniques, while low cost devices generally operate at relatively low efficiency.

The radial pn junction design sets the direction of light absorption perpendicular to the direction of minority-carrier transport, allowing the cell to be thick enough for effective light absorption, while also providing a short pathway for carrier collection. This is achieved by increasing the junction area, in order to decrease the path length any photogenerated minority carrier must travel, to be less than its minority carrier diffusion length. Realizing this geometry in an array of semiconducting wires, by for example depositing a single-crystalline inorganic semiconducting absorber layer at high deposition rates from the gas phase by the vapor-liquid-solid (VLS) mechanism, allows for a "bottom up" approach to device fabrication, which can in principle dramatically reduce the materials costs associated with a cell.

This thesis explores the potential of this design, first theoretically and computationally, and then by exploring the growth of structures with the proposed morphology via methods with the potential for low cost, and finally by the experimental characterization of cells.

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Portions of this thesis have been drawn from the following publications:

Radial pn junction, wire array solar cells. B. M. Kayes, M. A. Filler, M. D. Henry, J. R. Maiolo, M. D. Kelzenberg, M. C. Putnam, J. M. Spurgeon, K. E. Plass, A. Scherer, N. S. Lewis, and H. A. Atwater, Conference Record of the Thirty-third IEEE Photovoltaic Specialists Conference (2008)

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Chapter 1

Introduction

This thesis concerns the description and exploration of a new solar cell design concept, namely the radial pn junction, wire array solar cell. This cell consists of arrays of semiconducting wires each with radial pn junctions, potentially enabling a separate optimization of the design requirements for light absorption and carrier extraction, which are two key necessary conditions for efficient energy conversion in a photovoltaic device. We will begin, in this chapter, by exploring the motivation for photovoltaics in general and for this design concept in particular, and proceed in later chapters to a detailed theoretical and experimental exploration of the proposed device design.

1.1   Energy, Climate Change, and Photovoltaics

There is much talk in the popular news media, as well as in technical journals, at present about energy supply and climate change. People's enthusiasm for the former topic is motivated largely by tangible factors such as the rising cost of gasoline, perceived to be caused by a diminishing supply of fossil fuels and/or political instability in the regions rich in supply of these fossil fuels. Concerns about fossil fuel supply have been brought into focus in discussions of "Hubbert's Peak" [2] [3] or "Peak Oil" - a Google search returns many hits on these subjects. The latter topic, climate change, was the subject of Al Gore's recent film, "An Inconvenient Truth", as well as numerous reports including the Stern Review on the economics of climate change released by the UK government in October 2006, [4] and the Intergovernmental Panel on Climate Change's Fourth Assessment Report released in 2007. [5]

In fact energy supply and climate change are inextricably linked, and while we can debate the relationship or lack thereof with regards to fossil fuel resources and gasoline prices, the evidence is becoming increasingly clear that we do face a problem with regard

to the increased concentrations of carbon dioxide in our atmosphere due to the combustion of fossil fuels. There are now large and growing social, political and economic drivers to generate energy in a way that is renewable and carbon-free. The scale of carbon-free energy required in order to stabilize carbon levels in the atmosphere is alarming. [5] [6] It is the magnitude of the required carbon-free power that provides a strong argument for pursuing solar energy conversion, in that no other renewable energy resource has the potential for generating energy on such a large scale [7] (nuclear power, while potentially able to generate energy at the required scale, is carbon-free but not renewable).

Photovoltaic (PV) devices convert incident photons of high-enough energy directly into electricity. As such they are one of a family of solar energy conversion devices, others include solar thermal (wherein sunlight is used to heat a liquid which is then used to drive a turbine to generate electricity) and photoelectrochemical cells (wherein a photoactive electrode(s) in the cell uses sunlight to directly drive an electrochemical reaction, generating fuel and/or electricity). PVs are favored for many applications because they are modular and can thus be deployed at arbitrarily small or large scales and in particular are well-suited to rooftop deployment (as opposed to solar thermal which requires large-scale deployment), and because of their relatively high efficiency and long-term (30 year) stability (as opposed to photoelectrochemical cells which at the time of writing are limited to lower efficiencies and suffer from stability issues). The PV industry has been growing rapidly, especially in recent years, due primarily to aggressive government-fostered market growth in Japan, Germany and, more recently, Spain. PVs are nearing cost-competitiveness with other sources of electricity, [8] [9] and the drive continues to reduce the cost per kilowatt-hour to increase the adoption of PVs.

Silicon (Si) is by far the most popular material choice in the terrestrial PVs market at the time of writing. [8] [9] This is for several reasons. Firstly, Si's bandgap is almost ideally matched to the solar spectrum. [10] Secondly, Si is abundant, indeed Si is the most abundant solid element on Earth, [11] and, at least in principle, cheap. Thirdly, by using Si the PV industry has been able to follow in the footsteps of the microelectronics industry, exploiting the wealth of knowledge that has grown up around the element. The microelectronics industry, in turn, favors Si because its oxide is easily-grown and water-stable, forms a dielectric with favorable electronic properties and low dislocation density at the Si-oxide interface, and because Si is more stable to thermal breakdown than is germanium. [12]

Furthermore, Si is nontoxic.

There are two broad approaches to reducing the cost per unit electrical energy generated by solar cell modules. Firstly, one can aim to increase the efficiency of the product, usually by pursuing new cell designs that can take full advantage of high-quality absorber material. Secondly, one can pursue cost reductions while maintaining the efficiency of the product, often done by exploring novel manufacturing approaches but also sometimes with new cell designs and perhaps by exploiting lower-quality, cheaper materials. There is good reason to believe that the record Si cell efficiency for unconcentrated sunlight, of 24.7%, set by UNSW in 1999, [13] will not be significantly exceeded. [14] Thus, in the case of Si, most research efforts have fallen into the second category, i.e., pursuing designs that approach this efficiency but that are more cost-effective at the manufacturing level. Notably, SunPower Corporation has recently announced a cell produced on an industrial pilot line with an efficiency of 23.4%. [15]

This latter approach is also broadly speaking the approach we have favored, through a cell design that has two key advantages over traditional, planar approaches. Firstly, the radial pn junction, wire array solar cell is predicted to exhibit superior tolerance to low material quality relative to a planar design (see Ch. 2). Secondly, this design, when combined with wire array "peel off" and substrate re-use, allows in principle for a manufacturing approach where the materials costs are greatly reduced because the relatively expensive Si wafers are used only as a (re-usable) growth template and not as the absorber material in the final cell.

1.2   Production of Si for Photovoltaics

The main expense in obtaining Si suitable for the manufacture of solar cells is in the refining and recrystallizing process. This is typically done by first obtaining Si from high-purity SiO_2 by reacting with carbon at high temperatures, via reactions like:

$$SiO_2 + 2C \longrightarrow Si + 2CO. \tag{1.1}$$
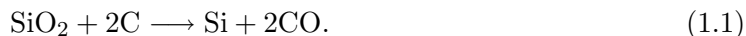
This creates so-called metallurgical-grade Si, which is approximately 98% pure and for most purposes in PVs requires further purification to be useful. After initial purification the Si is typically then brought to very high purity by the Siemens process, in which the Si is first

decomposed in reactions like

$$Si + 3HCl \longrightarrow SiHCl_3 + H_2 \qquad (1.2)$$

and then re-deposited onto high-purity Si rods at high temperature via reactions such as

$$2SiHCl_3 \longrightarrow Si + HCl + SiCl_4. \qquad (1.3)$$
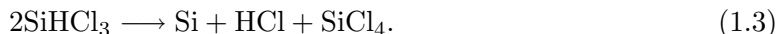
Si produced from this and similar processes is called polycrystalline silicon, or polysilicon. It is worth noting at this stage that $SiCl_4$ is a byproduct of both processes, in the latter case for example via the reaction written above, and in the former case through side reactions such as

$$Si + 4HCl \longrightarrow SiCl_4 + 2H_2. \qquad (1.4)$$

Overall, for each mole of Si converted to polysilicon, 3 to 4 moles are converted to $SiCl_4$. [16] Given the large amounts of energy required to convert the $SiCl_4$ back to $SiHCl_3$, $SiCl_4$ was until recently used to make fumed silica (silica nanoparticle powder used in fillers, coatings, and adhesives). However, as the demand for polysilicon has grown much more rapidly than the demand for fumed silica, more recently the $SiCl_4$ has had to be recycled. [17]

Liquid polysilicon is then solidified into large (~ 1 m^3) boules, typically either via the Czochralski Process (in which a Si seed crystal is pulled slowly out of a molten vat of Si, solidifying as it rises with the same crystal orientation as the seed), or by block-casting (simply cooling the Si at a controlled rate in a large crucible), depending on whether single-crystalline (in the former case) or multicrystalline (in the latter) material is required. These boules are then sawn into "wafers" which can then be processed into solar cells. Wafering induces additional losses in that a significant fraction of the boule simply becomes dust during the sawing process (called "kerf" loss).

Motivated by the potential for cost reductions in avoiding many or all of the above steps, many companies have been founded to create "thin film" solar cells, that is solar cells where the active material is deposited directly onto a foreign substrate from a liquid or gaseous precursor. Most notable, at the time of writing, is the company First Solar, which has become the largest PV manufacturer in the USA and one of the largest in the world on the

basis of its thin film CdTe-based product. There has also been much work on making thin film Si devices, on low cost substrates such as glass. However, with no crystalline "seed" to guide growth, these devices are inherently polycrystalline and efficiencies to date have been limited to less than 10%. [13]

1.3   Orthogonalizing Light Absorption and Carrier Transport

Despite a gradual but consistent decrease in the cost per kilowatt-hour of electricity generated by PVs, [18] the cost is still too high for widespread adoption of this technology. We have been motivated by the potential for radical redesign of the geometry of the PV cell to allow for the use of much lower quality material while retaining reasonable efficiencies, and therefore sharply reducing the cost per kilowatt-hour of PV electricity. Inexpensive candidate materials for use in PV applications generally have either a high level of impurities or a high density of defects, resulting in low minority carrier diffusion lengths. [19] Use of such low-diffusion-length material as the absorbing base in a conventional, planar pn junction solar cell geometry (Fig. 1.1) results in devices having carrier collection limited by minority carrier diffusion in the base region. In a solar cell, an incident photon creates an electron-hole pair which is then separated by a built-in electric field. To generate power, the carriers (electrons and holes) must be able to traverse the thickness of the cell. i.e., for a planar solar cell with a p-type base we want:

$$L_n > 1/\alpha \tag{1.5}$$

and

$$L > 1/\alpha, \tag{1.6}$$

where L_n is the diffusion length of electrons in the p-type base layer, L is the cell thickness (assuming a negligibly thin n-type emitter layer), and $1/\alpha$ is the "optical thickness" of the material (which is related to the wavelength-dependent absorption constant $\alpha(\lambda)$, integrated over all wavelengths λ). Optical thickness can be defined in a variety of ways. The definition that we use is that optical thickness is the thickness of material required to absorb 90% of the incident photons with energy above the band-gap energy (see also Ch. 2.2). With this
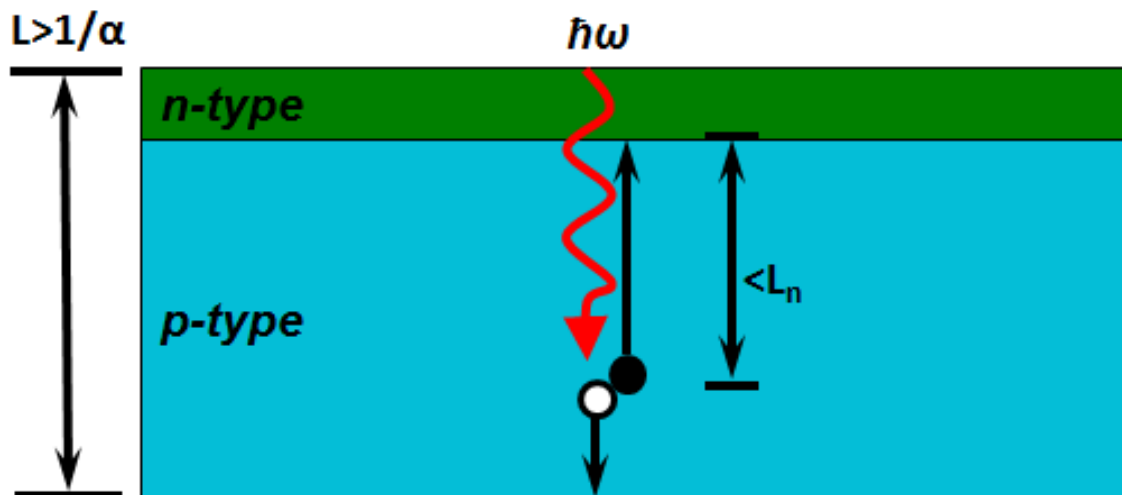
Figure 1.1. Schematic of a traditional planar solar cell design. Shown schematically are the device requirements that when a photon of energy $\hbar\omega$ generates an electron-hole pair in the p-type base of the cell, the cell thickness L must be greater than its optical thickness $1/\alpha$, and the minority-electron diffusion length L_n must be long enough that any optically-generated minority carrier can reach the pn junction before recombining.

definition, Si has an optical thickness of 125 μm. By employing light-trapping techniques, so that photons pass multiple times through the absorber material before leaving the device, the effective optical thickness of a material is reduced, but equations similar to those above will still apply. This sets a lower limit on the diffusion length that is acceptable for making high-efficiency solar cells from a given material in a traditional, planar pn junction geometry, and thus a lower limit on the material quality and materials costs in fabricating a high-efficiency solar cell. Given the limits to the extent to which light trapping can reduce the need for optically-thick material, [20] [21] [22] materials with diffusion lengths that are very low relative to their optical thicknesses cannot readily be incorporated into high energy conversion efficiency planar solar cell structures.

Decoupling the requirements for light absorption and carrier extraction into orthogonal spatial directions provides a potential solution to this device design and optimization issue. The first such proposal of orthogonalizing the direction of incident light and that of minority-carrier transport that we are aware of came in 1966 in the form of the so-called "vertical multijunction" (VMJ) solar cell of J. F. Wise. [24] [25] This device "employs the
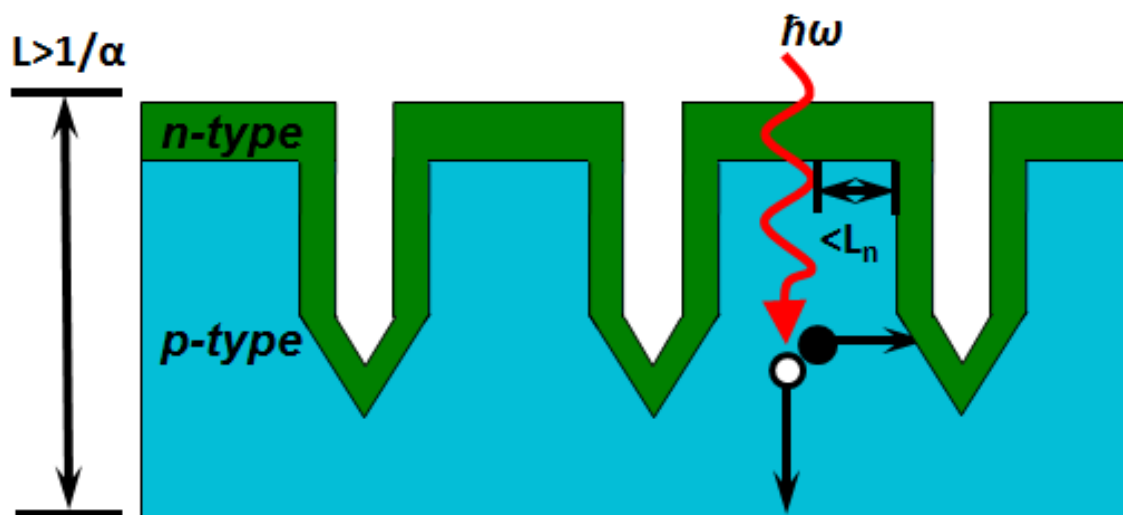
Figure 1.2. Schematic of the Vertical Multjunction (VMJ) solar cell design (after [23]). Shown schematically are the device requirements that when a photon of energy $\hbar\omega$ generates an electron-hole pair in the p-type "base" of the cell, the cell thickness L must be greater than its optical thickness $1/\alpha$, but that low minority-electron diffusion lengths L_n can be tolerated simply by tuning the groove pitch so that any optically-generating minority carrier is within a diffusion length of the pn junction.

concept of vertical junctions (parallel to incident light) rather than the conventional single horizontal junction (normal to incident light). The merit of such a device lies in the fact that many junctions vertically configured will enable photon-generated minority carriers to have a higher probability of reaching a junction thus increasing carrier collection efficiency and tolerance to radiation damage" (Fig. 1.2). At that time, the goal of the research was to engineer PV devices that were resistant to radiation damage, which is important for deployment in space, to power satellites for example. After a considerable amount of theoretical as well as experimental work in this area, including the demonstration of 15% efficient devices (see, for example, Ref. [26]), the field eventually died out as GaAs became the material of choice for space applications.

A similar idea surfaced in 1994 in the form of the "parallel multijunction" (PMJ) solar cell, [28] in which the solar cell consists of "alternating polarity n- and p-type layers, with like polarity layers connected in parallel" (Fig. 1.3). In contrast to the VMJ design, in this case the junctions are perpendicular to the direction of incident light, as for a traditional planar pn junction design. The PMJ and VMJ designs are however similar in that light-generated minority carriers can be made to be arbitrarily close to a charge-separating pn junction, even in an optically-thick cell with a low minority-carrier diffusion length absorber. With the PMJ design it was noted that, in theory, "with layers less than a minority carrier diffusion length thick, full collection of photogenerated carriers for arbitrary multijunction cell thickness is assured", and further that "as material quality decreases, single-junction performance drops to low values, while multilayer performance remains virtually unchanged, even for very poor material". The design was predicted to have superior tolerance to metallic impurities as well as to grain boundaries. [27] However, detractors claimed that, if one includes the effects of efficient light trapping, the parallel multijunction design is little better than a planar design, if at all. [29] It is not altogether clear from the literature why work on this design ceased, as relatively efficient ($\sim 13\%$) cells had been shown to be manufacturable with deposited Si in an industrial-like environment. [30] [31] However, it is likely tied to cost effectiveness, i.e., that the cell did not perform well enough to justify the expense of the single-crystalline growth substrate necessary for high quality Si device layers.
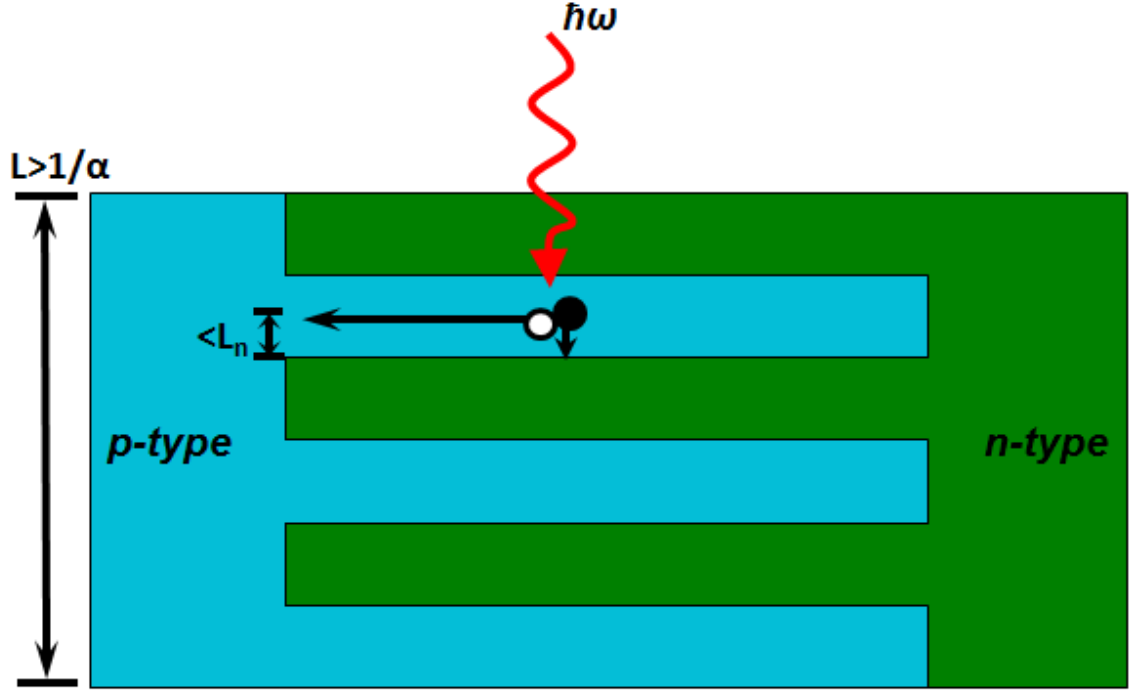
Figure 1.3. Schematic of the Parallel Multjunction (PMJ) solar cell design (after [27]). Shown schematically are the device requirements that when a photon of energy $\hbar\omega$ generates an electron-hole pair in a p-type layer in the cell, the cell thickness L must be greater than its optical thickness $1/\alpha$, but that low minority-electron diffusion lengths L_n can be tolerated simply by tuning the layer thicknesses so that any optically-generating minority carrier is within a diffusion length of the pn junction. Note that although the minority carrier transport and light absorption direction are parallel, this design shares the essential feature of the VMJ and radial junction wire array designs, namely that junction area is increased to boost the fraction of optically-generated minority carriers that are swept across the pn junction.

1.4 Nanowires and Vapor-Liquid-Solid Growth

Nanowires are ubiquitous in the scientific literature, and at the time of writing are being explored by many groups, for example, as potential building blocks for future microelectronic circuits as the demands on device size become ever-more demanding. They have also been used as a convenient structure with which to test the properties of very small objects such as quantum confinement and novel transport properties.

Because of these and many other applications, there is a similarly large body of literature on the many different methods of growing nanowires. The Vapor-Liquid-Solid (VLS) technique was first described by Wagner and Ellis in 1964 as a method for growing semiconductor "whiskers". [32] It quickly established itself as a convenient method for producing well-controlled nano- and microwires (where the latter is used to denote wire-like structures with diameters larger than 1 μm) of well-controlled dimensions and orientation, at rapid growth rates. It also has the interesting property that defects tend to be expelled out of the growing crystal, allowing for the growth of single-crystalline material. It is also noteworthy due to the wide variety of semiconductors and metals that can be grown via the same technique. [33]

In this method of wire growth, semiconductor atoms are introduced in the vapor phase over another semiconductor surface decorated with metal catalyst particles at elevated temperature. If the temperature is above the eutectic temperature of the metal-semiconductor alloy, the catalyst particle can act as a sink for semiconductor atoms. As the metal catalyst dissolves more and more of the semiconductor, it eventually becomes supersaturated, at which point solid semiconductor is "frozen" out of the alloy. As the gas continues to impinge on the catalyst, the semiconductor grows in one dimension only, in a direction determined by epitaxy with the substrate crystal orientation.

Interest in VLS was revived in the late 1990s as the nanowire research field began to pick up speed. While control of the position of microwires had already been demonstrated, [33] advances such as the precise control of the position of truly "nano" nanowires, [34] and the growth of core-shell [35] and axial heterojunction [36] [37] [38] structures generated tremendous excitement within the community. In the case of Si, and contrary to the previous work which had favored the use of $SiCl_4$ as the gaseous Si precursor, often at atmospheric pressures, this new group of researchers tended to use SiH_4 in low pressure chemical vapor
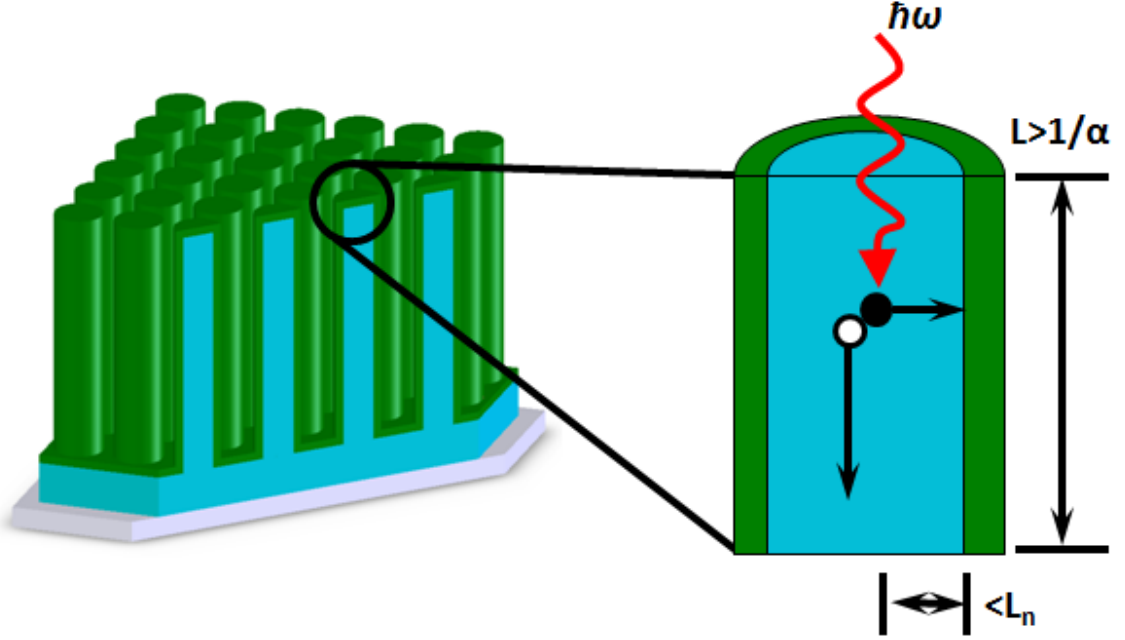
Figure 1.4. Schematic of the radial pn junction, wire array solar cell design (image credit: M. D. Kelzenberg). Shown schematically are the device requirements that when a photon of energy $\hbar\omega$ generates an electron-hole pair in the p-type core of a wire, the cell thickness (= wire length) L must be greater than its optical thickness $1/\alpha$, but that low minority-electron diffusion lengths L_n can be tolerated simply by tuning the wire radius so that any optically-generating minority carrier is within a diffusion length of the pn junction.

deposition (LPCVD) systems, which allowed for much lower processing temperatures ($\sim$ 500 °C rather than $\sim$ 1000 °C), and also allowed for smaller-diameter wires to be grown. [39] SiCl$_4$ did not disappear completely however, and it has been shown recently that the HCl that is formed in-situ when growing from SiCl$_4$ may make for much easier epitaxy than is possible with SiH$_4$ without significant effort. [40]

1.5   The Radial pn Junction, Wire Array Solar Cell

We proposed the radial pn junction, wire array solar cell, [41] that is, a PV device consisting of arrays of semiconducting wires each with radial pn junctions, (Fig. 1.4) as a way to potentially combine the PV device benefits of maintaining short minority-carrier transport distances in an optically thick cell, with the potential manufacturing benefits hinted at by the VLS-grown nanowire literature. An array of nano- or microwires with pn junctions

in the radial direction would enable decoupling the requirements for light absorption and carrier extraction into orthogonal spatial directions. Each individual pn junction wire in the cell could be long in the direction of incident light, allowing for optimal light absorption, but thin in another dimension, thereby allowing for effective carrier collection. The use of VLS-grown nano- or microwires as the active material potentially allows for the rapid growth of single-crystalline Si from low-cost vapor precursors. We recently discovered that the use of VLS-grown Si wires with radial pn junctions as photoconverters had previously been reported on in 1978, [42] but the detailed exploration of this structure for solar energy conversion was not contained in that earlier report, and the work contained herein was developed independently of that work. Theoretical and experimental exploration of the radial pn junction, wire array solar cell design is the topic of this thesis.

Chapter 2

Solar Cell Device Physics and the Radial Geometry

2.1 Introduction

In this chapter we will begin by providing motivation for the radial pn junction geometry, and follow with a detailed theoretical comparison of the performance of a PV device with a radial junction vs. one with a planar junction. The chapter concludes with a discussion of similar cylindrical structures with axial, rather than radial, pn junctions.

2.2 "To First Order": Salient Features

Solar cell efficiency, η, is defined as the ratio of electrical power out (at an operating condition of maximum power output), P_{out}, divided by total optical power in, P_{in}, typically under AM1.5G[1] illumination [43] (see Fig. 2.1) at an intensity of 0.1 W/cm^2, i.e.,

$$\eta = \frac{P_{out}}{P_{in}} \tag{2.1}$$

$$= \frac{V_{oc} \times J_{sc} \times FF}{P_{in}}, \tag{2.2}$$

where the open-circuit voltage V_{oc} is the voltage or bias across the cell when no current is flowing, the short-circuit current density J_{sc} is the current density at zero bias, and the fill

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[1]AM1.5G stands for Air Mass 1.5, Global illumination. "Air Mass 1.5" indicates that the sunlight has been attenuated by passage through the Earth's atmosphere a distance equal to 1.5 times the shortest path (which is when the sun is directly overhead). "Global" indicates that both direct and diffuse components of sunlight are included, "AM1.5D", where the D stands for "Direct" would indicate that only direct illumination is considered.

factor FF is the ratio of the maximum electrical power output to the product of V_{oc} and J_{sc}. As minority carrier diffusion length decreases, planar solar cell geometries lose efficiency due to losses in J_{sc}, V_{oc} and FF. Considering a solar cell as an ideal diode in parallel with a pure light-generated current source leads to the following expression for current generation in a planar pn junction solar cell: [44]

$$J = J_{sc} - J_0 \left[exp \left(\frac{qV}{k_B T} \right) - 1 \right]. \tag{2.3}$$

This in turn leads to the following expression for V_{oc}:

$$V_{oc} = \frac{k_B T}{q} ln \left[\left(\frac{J_{sc}}{J_0} \right) + 1 \right] \tag{2.4}$$

$$\approx \frac{k_B T}{q} ln \left(\frac{J_{sc}}{J_0} \right), \tag{2.5}$$

where $q = 1.602193 \times 10^{-19}$ C is the magnitude of the electronic charge, $k_B = 1.38073 \times 10^{-23}$ m^2 kg s^{-2} K^{-1} is Boltzmann's constant, and the temperature T is assumed to be 300 K.

For the purposes of this section, we will treat the minority carrier diffusion length, L_n (or L_p for holes), as the sole metric by which material quality is judged. This quantity is a measure of the average distance a carrier can move from the point of its generation before it recombines. Diffusion length is related to carrier mobility and lifetime by the following expressions: [45]

$$L_n = \sqrt{D_n \tau_n} \tag{2.6}$$

$$= \sqrt{\frac{k_B T}{q} \mu_n \tau_n}, \tag{2.7}$$

with similar expressions in the case of holes. As will be discussed in more detail below, for recombination processes dominated by recombination through mid-gap traps ("Shockley Read Hall" recombination [46] [47]), the minority carrier lifetime can also be related to trap density: [45]

$$\tau_{n0} = \frac{1}{\sigma_n N_r v_{th}}, \tag{2.8}$$

where σ_n is the cross section for electron capture, N_r is the density of recombination centers, and v_{th} is the thermal velocity, and again a similar expression applies for holes.
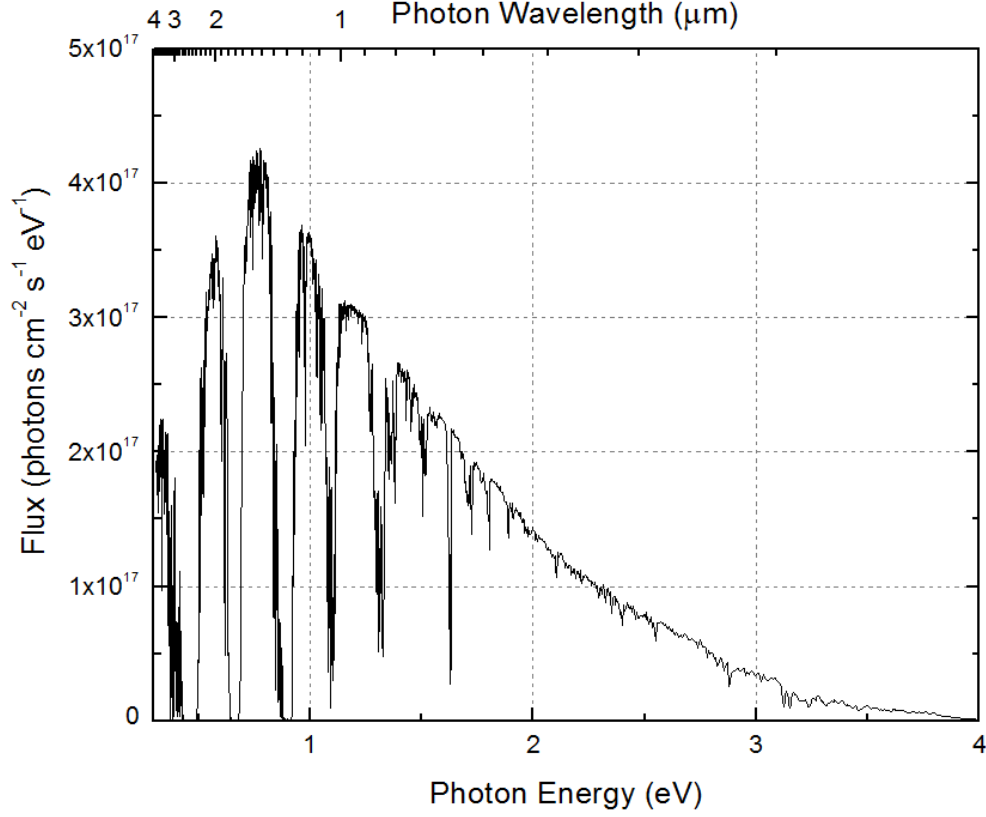
Figure 2.1. The AM 1.5 global (AM 1.5G) spectrum. [43]

J_{sc} can be considered a measure of the number of light-generated carriers that are swept across the pn junction per unit time, assuming ideal majority carrier transport and collection. We expect that J_{sc} will increase as L_n increases, until some limiting value, when either L_n becomes much larger than the cell thickness, or much larger than the "optical thickness" of the material.

Optical thickness denotes the thickness of material required to absorb all of the above-bandgap photons. Absorption is described by Beer's Law, which states that light is attenuated exponentially as a function of material thickness, at each wavelength. The strength of absorption, as a function of wavelength, is given by a material's absorption coefficient $\alpha(\lambda)$. To be more specific, given an incident photon flux $\Gamma_0(\lambda)$, the flux passing through a

material of thickness L is

$$\Gamma(L) = \int d\lambda \Gamma_0(\lambda) e^{-L/\alpha(\lambda)}. \tag{2.9}$$

Therefore, the total absorption of a piece of material of thickness L, neglecting all reflection effects, is

$$Abs(L) = \Gamma(0) - \Gamma(L) = \int d\lambda \Gamma_0(\lambda) \left[1 - e^{-L/\alpha(\lambda)} \right]. \tag{2.10}$$

It is tempting to define a wavelength-independent optical constant, say α, to define a wavelength-independent exponential attenuation of light into the semiconductor, i.e., such that

$$Abs(L) \approx \int d\lambda \Gamma_0(\lambda) \left[1 - e^{-L/\alpha} \right] = \left[1 - e^{-L/\alpha} \right] \int d\lambda \Gamma_0(\lambda). \tag{2.11}$$

This is, however, impossible, as displayed in Fig. 2.2, where the expressions 2.10 and 2.11 are compared. We therefore define the "optical thickness" of a material to be that thickness required to absorb 90% of the above-band-gap photons, and give this the loose designation "$1/\alpha$", with the understanding that this does not imply that a single, wavelength-independent, absorption coefficient can adequately describe light absorption in the material. This thickness is 125 μm for Si and is only 891 nm for GaAs (Fig. 2.3).

In the next few paragraphs we will motivate the potential benefits of a radial pn junction geometry with an intuitive model to describe the effects of reducing diffusion length in PV devices. Assume that we have an "optically-thick" (i.e., 125 μm thick) Si PV device with a p-type base, a negligibly thin emitter, insignificant surface recombination, and baseline parameters of the record Si solar cell (the UNSW PERL cell [13]), namely $V_{oc} = 0.706$ V, $J_{sc} = 0.0422$ A/cm^2, and $FF = 0.828$, so that $\eta = 24.7\%$. This means that $J_0 \approx 5.8 \times 10^{-14}$ A/cm^2 , from Eq. 2.3. Then consider the effect of reducing minority electron diffusion length L_n. Assume that carrier generation per unit volume is independent of depth into the cell (this is an oversimplification, with a more realistic description given above), and that all carriers generated within L_n of the pn junction are collected, while the rest are not (this is also an oversimplification, with a more realistic treatment given in the next section). i.e., For a planar geometry, assume that

$$J_{sc} = 0.0422 \times \frac{L_n}{L}, \qquad L_n \leq L \tag{2.12}$$

where J_{sc} is in A/cm^2, L_n is the minority electron diffusion length in the base, and L (=
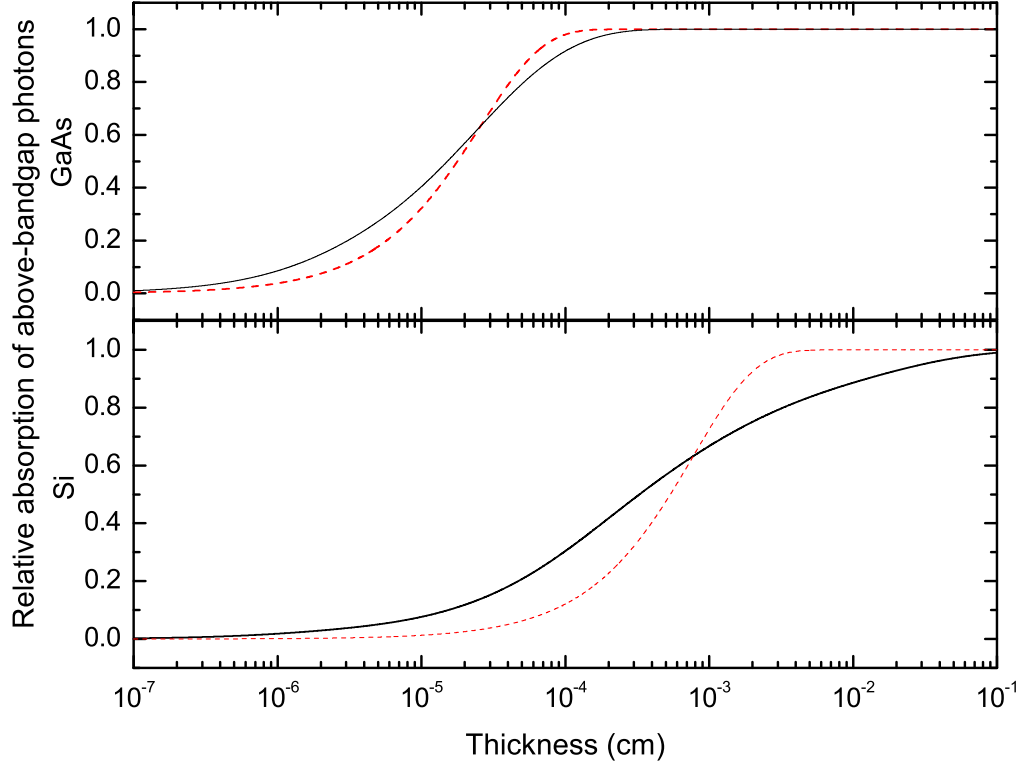
Figure 2.2. Comparison of a single exponential model for light absorption using a wavelength-independent α (the dotted red lines. See Eq. 2.11), with a more realistic model which integrates the absorption over all wavelengths of the AM1.5G spectrum [43] using a wavelength-dependent $\alpha(\lambda)$ (the solid black lines. See Eq. 2.10) [48]. These are plotted for both GaAs (top) and Si (bottom). Note that the wavelength-dependent and wavelength-independent models diverge more for the indirect bandgap material, Si.
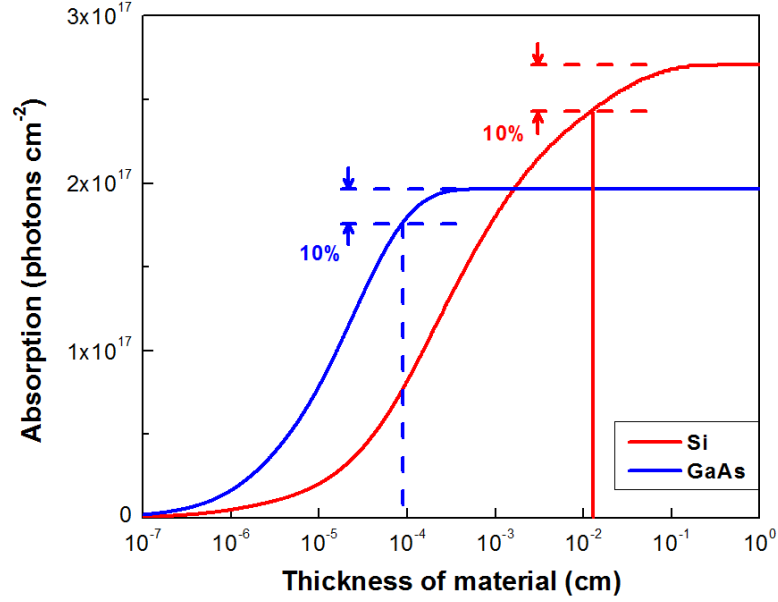
Figure 2.3. Absorption per unit area of Si and GaAs, of photons in the AM 1.5G solar spectrum [43] (at 0.1 W cm^{-2} intensity) with energy greater than each material's bandgap energy, as a function of thickness of material. The vertical lines indicate what we define to be the "optical thickness" of each material: 90% of the above-bandgap photons are absorbed within 891 nm in GaAs, while 125 μm of Si is required to achieve the same effect, due to Si's indirect band gap. Note also that because the band gap of GaAs is larger than that of Si, fewer total photons can be absorbed in optically-thick layers of GaAs than in optically-thick layers of Si.

125 μm) is the cell thickness. Then we can calculate V_{oc} from Eq. 2.5, and η from Eq. 2.1, assuming that FF is unaffected by changes in L_n.

In the radial pn junction geometry, assume that we again have a 125 μm thick device, this time in the shape of a cylinder, with an emitter layer on the top surface as well as on the side walls. Assume that the cylinder radius is set equal to the minority electron diffusion length L_n, so that, with the additional assumption that all carriers generated within L_n of the pn junction are collected, J_{sc} is independent of L_n. V_{oc} can then be calculated by assuming that J_0 scales with pn junction area, i.e., that

$$V_{oc} = \frac{k_B T}{q} ln \left[\left(\frac{J_{sc}}{J_0 \gamma} \right) + 1 \right], \tag{2.13}$$

where γ is the area of the junction in the cylindrical geometry relative to the area of the top surface of the cylinder (see, for example, [49]). Again, efficiency η can then be calculated from Eq. 2.1. The results of this simple comparison between what we might hope to expect in both geometries are given in Table 2.1.

Table 2.1. Comparison of the basic features of the planar and radial geometries

	L_n (μm)	125	100	10	1
Planar cell	J_{sc} (A/cm^2)	0.0422	0.0338	0.00338	0.000338
	V_{oc} (V)	0.706	0.700	0.641	0.581
	FF	0.828	0.828	0.828	0.828
	Efficiency (%)	24.7	19.6	1.8	0.2
Radial junction cell	Junction Area Increase	3	3.5	26	251
	J_{sc} (A/cm^2)	0.0422	0.0422	0.0422	0.0422
	V_{oc} (V)	0.678	0.674	0.622	0.563
	FF	0.828	0.828	0.828	0.828
	Efficiency (%)	23.7	23.5	21.7	19.7

The above analysis grossly oversimplifies solar cell principles, but demonstrates intuitively the potential benefits of the radial geometry for low-diffusion-length materials. There are many features of the above model that need to be changed in order to obtain quantitatively correct results, and this will be explored in the next section. The assumption of a linear dependence of J_{sc} on L_n overstates the loss in carrier collection as L_n decreases

in a planar geometry. In reality, carrier generation is highly non-uniform through the cell thickness and occurs much more strongly at the top of the cell, i.e., close to the pn junction. As stated above, in reality light is attenuated exponentially with material thickness, at each wavelength, with shorter wavelengths being absorbed most strongly. Furthermore, the model used above, that collection is guaranteed for carriers within a diffusion length of the junction, and zero for those further away, is not accurate either. Fill factor is also affected by changes in diffusion lengths, and no attempt was made to consider this in the above. Also, we have ignored any issues associated with the inevitably less-than-100 % packing fraction that we will have in the radial geometry (close-packed cylinders can fill at most $\pi/(2\sqrt{3}) \approx 90$ % of space) - this may have the effect of reducing the J_{sc} in the radial case although the details are far from trivial. Finally, we have neglected to treat the effects of the emitter, the wire surfaces, and the pn junction region, and the latter especially will prove to be extremely important as we shall see.

Nevertheless, this simple analysis does point to some of the key features we expect to see in the novel geometry. The radial junction is expected to exhibit a much higher tolerance to reduced diffusion lengths than the planar geometry, due to its ability to retain high carrier collection independent of diffusion length. This is paid for by a loss in V_{oc} as junction area increases, but because this is a logarithmic dependence it is a lesser effect. In the planar geometry we expect large losses in J_{sc} as L_n decreases, and that this will also affect V_{oc}, leading to intolerable losses in efficiency at low ($\lesssim 10$ μm for Si) diffusion lengths.

2.3   Transport Equations in the Radial Geometry

In order to gain a quantitative understanding of how the radial junction geometry should perform relative to a planar geometry, it is necessary to solve the carrier transport equations in a cylindrical coordinate system. A model for the radial pn junction solar cell was constructed by extending the analysis of the planar cell geometry [44] to a cylindrical geometry. The cell was divided schematically into four regions: the quasineutral part of the n-type emitter region (of width x_1), the depletion region of the n-type material (of width x_2), the depletion region of the p-type material (of width x_3), and the quasineutral part of the p-type base region (of width x_d) (Fig. 2.4).

The pn junction in each wire was assumed to be abrupt, and the depletion approxima-
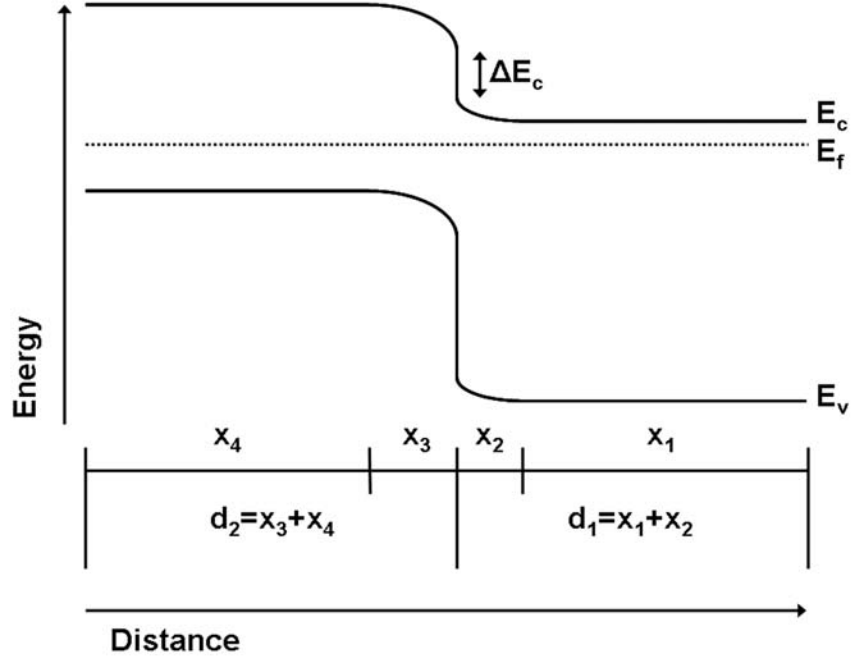
Figure 2.4. Generalized band structure for a pn heterojunction structure. Shown are the conduction and valence band energies, E_c and E_v, as well as the equilibrium Fermi energy E_f. ΔE_c is the discontinuity in the conduction band energy, which is typically nonzero for a heterojunction. The example cells in this paper are homojunctions, and so $\Delta E_c = 0$. The x axis shows the schematic division of the cell into four regions: the quasineutral part of the n-type material (of width x_1), the depleted part of the n-type material (of width x_2), the depleted part of the p-type material (of width x_3), and the quasineutral part of the p-type material (of width x_4).

tion was invoked. The emitter layer (i.e., the exterior "shell" of the wire) was assumed to be n-type, while the base (i.e., the interior "core" of the wire) was assumed to be p-type (see Fig. 2.5. The analogous schematic for the planar structure is shown in Fig. 2.6). Light was assumed to be normally incident on the top face of the wire, with no reflection losses. Recombination was assumed to be purely due to the Shockley-Read-Hall recombination from a single trap level at midgap; [47] other recombination processes, such as Auger recombination, were neglected. However, surface recombination effects were included, by assuming a minority carrier surface recombination velocity S at the $r = R$ surface.

To simplify the analysis and to allow for analytic solutions, the minority carrier transport in the wire structure was assumed to be purely radial. The approximation of one-dimensional carrier transport is valid when the variation in carrier concentration in the z direction occurs over a much longer length scale than that in the r direction. This is an appropriate assumption for a radial pn junction wire in a material that is collection limited, that is, one with an optical thickness (see Ch. 2.2) that is much greater than the diffusion length of minority carriers. In this case, the variation in carrier concentration in the axial direction is primarily due to light absorbtion and occurs over a large distance relative to the variation in carrier concentration in the radial direction, which occurs due to diffusion and drift resulting from the potential drop at the pn junction interface.

Although individual wires may have a high resistance, the IR drop in a wire can still be very low because of the very small current that will pass through each wire. Given a resistivity $\sim 10^{-2}$ Ω cm (appropriate for Si with doping $\sim 10^{18}$ cm^{-3}), [50] a wire length ~ 100 μm, and a current density ~ 0.05 A cm^{-2}, the IR drop in a wire due to series resistance is $\sim 10^{-5}$ V. Hence, it was reasonable to assume, as we did, that the exterior of the wire was an equipotential surface relative to the core of the wire.

The total photogenerated carrier flux was calculated by an integration that is equivalent to summing up the contributions at each value of z at a given bias, and the dark current was calculated for the entire junction area neglecting the ends. The bias was then varied, creating a current-density versus voltage $(J - V)$ curve (not shown), from which the open-circuit voltage, short-circuit current density, fill factor, and efficiency could be calculated.

Cell current density was normalized to the area of the top surface of the wire. This is equivalent to assuming a packing fraction of 100 %. In practice, light will not be incident truly normal on the top surface of the wires, but rather at some angle. At small angles from
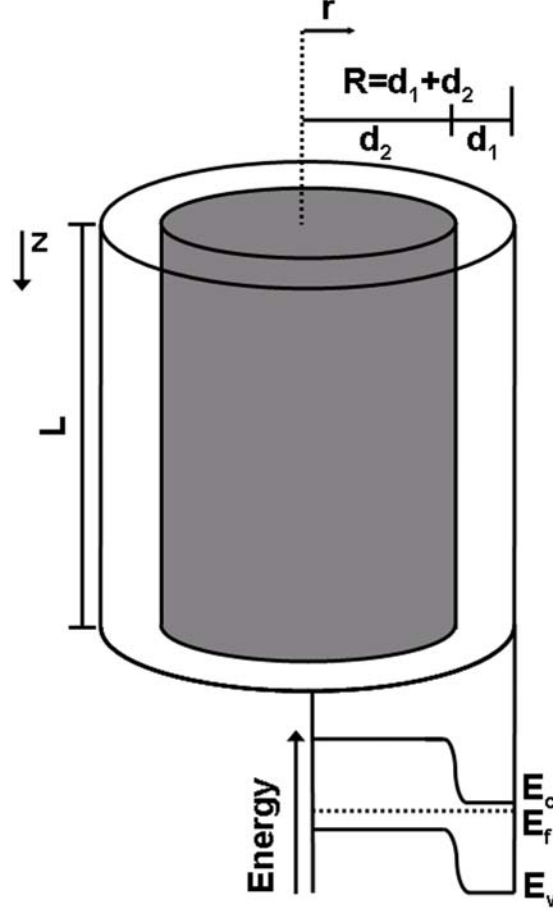
Figure 2.5. Schematic of a single wire from the radial pn junction cell, and its corresponding energy band diagram. Light is incident on the top surface. The external shell is n-type, the internal core is p-type. E_c is the conduction band energy, E_v is the valence band energy, and E_f is the Fermi energy. The n-type material forms an annulus of width d_1; the p-type material has radius d_2. The total cell radius $R = d_1 + d_2$, and its thickness is equal to the rod length L. Recombination at the top and bottom surfaces is neglected; i.e., it is assumed that minority-carrier diffusion in the vertical direction is negligible.
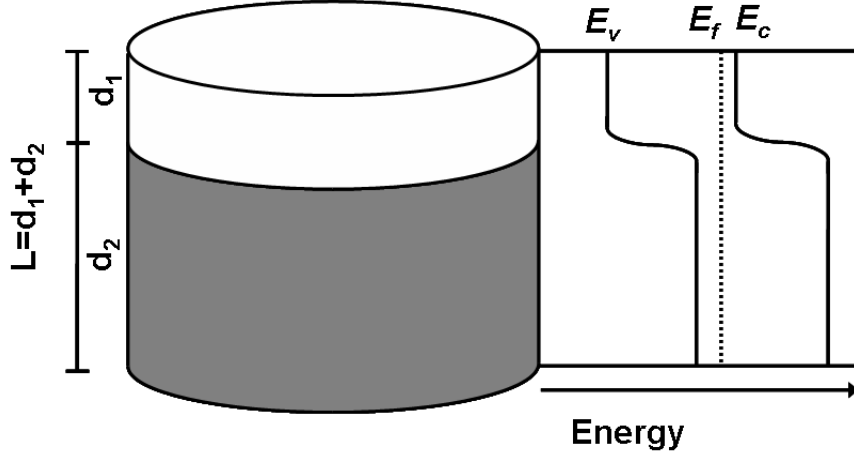
Figure 2.6. A conventional planar solar cell is a pn junction device. Light is incident on the top surface. The top surface ("emitter") is n-type, the base is p-type. E_c is the conduction band energy, E_v is the valence band energy, and E_f is the Fermi energy. The n-type material has thickness d_1; the p-type material has thickness d_2. The total cell thickness $L = d_1 + d_2$. Recombination at the sidewalls is neglected; i.e., it is assumed that lateral dimension of the cell is much greater than its vertical thickness L - the aspect ratio of the cell is greatly exaggerated in this schematic.

normal incidence, light that is incident on the top of a wire will remain within the wire due to total internal reflection, while light that is not incident on the top of a wire may pass through many rods while traversing the cell due to the high-aspect ratio of the wires. The details await further study.

2.3.1 Quasineutral Regions

In analogy to treatments of planar pn junctions, [44] the minority-carrier movement in the quasineutral region of the p-type base (i.e. core) material was assumed to be governed by the transport equation,

$$\nabla^2 n' - \frac{n'}{L_n{}^2} = \frac{\partial^2 n'}{\partial r^2} + \frac{1}{r}\frac{\partial n'}{\partial r} - \frac{n'}{L_n{}^2} = -\frac{\alpha_2 \Gamma_0}{D_n}e^{\alpha_2 z}, \tag{2.14}$$

where $n' = n - n_0$ is the excess minority-electron concentration with respect to the equilibrium value n_0, L_n is the diffusion length of minority electrons, α_2 is the absorption coefficient of the p-type material, Γ_0 is the incident photon flux, and D_n is the electron

diffusion coefficient. The boundary conditions are

$$n'(0) = \text{finite}, \tag{2.15}$$

$$n'(x_4) = n_0 \left(e^{qV/k_BT} - 1\right), \tag{2.16}$$

where V is the applied bias, and the temperature T is assumed to be 300 K. The current density in the p-type quasineutral region, J^p, is thus

$$J^p = \frac{2x_4 \int_0^L J^p(z)\, dz}{R^2}, \tag{2.17}$$

where

$$J^p(z) = -qD_n \left.\frac{\partial n'}{\partial r}\right|_{r=x_4}, \tag{2.18}$$

and R and L are the radius and length of the wire, respectively.

In the quasineutral region of the n-type emitter, the transport equation is

$$\frac{\partial^2 p'}{\partial r^2} + \frac{1}{r}\frac{\partial p'}{\partial r} - \frac{p'}{L_p{}^2} = -\frac{\alpha_1 \Gamma_0}{D_p} e^{\alpha_1 z}, \tag{2.19}$$

where $p' = p - p_0$ is the excess minority-hole concentration with respect to the equilibrium value p_0, L_p is the diffusion length of minority holes, α_1 is the absorption coefficient of the n-type material, and D_p is the minority-hole diffusion coefficient. The boundary conditions were

$$p'(R - x_1) = p_0 \left(e^{qV/k_BT} - 1\right), \tag{2.20}$$

$$S_p p'(R) = -D_p \left.\frac{\partial p'}{\partial r}\right|_{r=R}, \tag{2.21}$$

where S_p is the surface-recombination velocity of holes at the external surface of the wire. Hence, the current density in the n-type quasineutral region, J^n, is

$$J^n = \frac{2(R - x_1) \int_0^L J^n(z)\, dz}{R^2}, \tag{2.22}$$

where

$$J^n(z) = qD_p \left.\frac{\partial p'}{\partial r}\right|_{r=R-x_1}. \tag{2.23}$$

2.3.2 Depletion Region

The depletion region width was obtained by solving Poisson's equation in the depletion region, assuming that the electric field E was zero outside of the depletion region, that ϵE was continuous across the junction, where ϵ is the dielectric constant of the semiconductor, and that ionized donors and acceptors were the sole constituents of charge (i.e. the depletion approximation was invoked).

The light-generated current density in the depletion region, J_g^{dep}, was calculated by assuming that all incident light that was absorbed produced carriers that were collected, which is reasonable given the strength of the electric field within this region. Hence, in the p-type part of the depletion region

$$J_g^{dep,p}(V) = q\Gamma_0 \left(1 - e^{-\alpha_2 L}\right) \frac{d_2{}^2 - x_4{}^2}{R^2}, \tag{2.24}$$

whereas in the n-type part of the depletion region

$$J_g^{dep,n}(V) = q\Gamma_0 \left(1 - e^{-\alpha_1 L}\right) \frac{(d_2 + x_2)^2 - d_2{}^2}{R^2}. \tag{2.25}$$

The recombination current density in the depletion region was approximated by assuming that the potential in the depletion region was a linear function of r. The recombination current density for the entire depletion region was calculated by multiplying the maximum recombination rate by a small volume centered about this maximum recombination point, in analogy with the standard treatment of the planar case. [51]

2.3.3 Solution

Solving the above equations with the stated assumptions produced the following expression for the J-V behavior of the device:

$$J = (J_0^p + J_0^n)\left(e^{qV/k_B T} - 1\right) - J_l^p - J_l^n + J_r^{dep}(V) - J_g^{dep,p}(V) - J_g^{dep,n}(V), \tag{2.26}$$

where

$$J_0^p = -2qn_0L\frac{D_n}{L_p{}^2}\frac{\beta_5}{\beta_1{}^2}\frac{I_1(\beta_5)}{I_0(\beta_5)}, \tag{2.27}$$

$$J_0^n = -2qp_0L\frac{D_p}{L_p{}^2}\frac{\beta_2}{\beta_1{}^2}\left(\frac{f_1K_1(\beta_2) - f_2I_1(\beta_2)}{f_1K_0(\beta_2) + f_2I_0(\beta_2)}\right), \tag{2.28}$$

$$J_l^p = -2q\Gamma_0\frac{L_n{}^2}{L_p{}^2}\frac{\beta_5}{\beta_1{}^2}\frac{I_1(\beta_5)}{I_0(\beta_5)}\left(1 - e^{-\beta_6}\right), \tag{2.29}$$

$$J_l^n = -2q\Gamma_0\frac{\beta_2}{\beta_1{}^2}\left[\frac{K_1(\beta_2)(f_1 - \beta_4I_0(\beta_2)) - I_1(\beta_2)(f_2 + \beta_4K_0(\beta_2))}{f_1K_0(\beta_2) + f_2I_0(\beta_2)}\right]$$

$$\times\left(1 - e^{-\beta_3}\right), \tag{2.30}$$

$$J_g^{dep,p}(V) = -q\Gamma_0\frac{d_2{}^2 - x_4{}^2}{R^2}\left(1 - e^{-\beta_6}\right), \tag{2.31}$$

$$J_g^{dep,n}(V) = -q\Gamma_0\frac{(d_2 + x_2)^2 - d_2{}^2}{R^2}\left(1 - e^{-\beta_3}\right), \tag{2.32}$$

$$J_r^{dep}(V) = -qLU_{max}\frac{r_2{}^2 - r_1{}^2}{R^2}, \tag{2.33}$$

where $I_n(x)$ and $K_n(x)$, $n = 0$ or 1, represent modified Bessel's functions of the first and second kinds, respectively.

The dimensionless parameters are defined as

$$\beta_1 = \frac{R}{L_p}, \tag{2.34}$$

$$\beta_2 = \frac{R - x_1}{L_p}, \tag{2.35}$$

$$\beta_3 = \alpha_1 L, \tag{2.36}$$

$$\beta_4 = \frac{L_pS_p}{D_p}, \tag{2.37}$$

$$\beta_5 = \frac{x_4}{L_n}, \tag{2.38}$$

$$\beta_6 = \alpha_2 L, \tag{2.39}$$

$$f_1 = f_1(\beta_1, \beta_4)$$
$$= I_1(\beta_1) + \beta_4I_0(\beta_1), \tag{2.40}$$

$$f_2 = f_2(\beta_1, \beta_4)$$
$$= K_1(\beta_1) + \beta_4K_0(\beta_1). \tag{2.41}$$

Additionally,

$$U_{max} = \frac{n_{i,*}}{\sqrt{\tau_{n0}\tau_{p0}}} \sinh\left(\frac{qV}{2k_BT}\right). \tag{2.42}$$

$$r_1(V) = r(V) - \frac{(x_2(V) + x_3(V))}{2}\kappa, \tag{2.43}$$

$$r_2(V) = r(V) + \frac{(x_2(V) + x_3(V))}{2}\kappa, \tag{2.44}$$

$$r(V) = x_4 + \frac{\log\left(\frac{N_a}{n_{i,p}}\right)}{\log\left(\frac{N_aN_d}{n_{i,p}n_{i,n}}\right)}(x_2(V) + x_3(V)), \tag{2.45}$$

$$\kappa = \frac{\pi k_BT}{q(V_{bi} - V)}, \tag{2.46}$$

$$V_{bi} - V = \frac{qN_d}{2\epsilon_n}(d_2 + x_2)^2 \log\left(\frac{d_2 + x_2}{d_2}\right)$$
$$+ \frac{qN_d}{4\epsilon_n}\left[d_2^2 + (d_2 + x_2)^2\right] + \frac{qN_a}{2\epsilon_p}x_4^2 \log\left(\frac{x_4}{d_2}\right)$$
$$+ \frac{qN_a}{4\epsilon_p}\left(d_2^2 - x_4^2\right), \tag{2.47}$$

where N_a, $n_{i,p}$, ϵ_p, and τ_{n0} are the dopant (acceptor) density, intrinsic carrier concentration, dielectric constant, and lifetime in the depletion region, respectively, for the p-type material. N_d, $n_{i,n}$, ϵ_n, and τ_{p0} are the analogous quantities for the n-type material. Also, $n_{i,*} = n_{i,p}$ or $n_{i,n}$, depending on whether the maximum recombination point lies in the p-type or n-type material. From Eq. (2.47), $x_2(V)$ and $x_3(V)$ can be found numerically, given the built-in voltage V_{bi}:

$$V_{bi} = \frac{k_BT}{q}\log\left(\frac{N_aN_d}{n_{i,p}n_{i,n}}\right) + \frac{\Delta E_c}{q}, \tag{2.48}$$

where ΔE_c is the conduction-band offset ($= 0$ for homojunctions).

2.4   Numerical Assessment of Device Behavior in Si

To gain further insight into the behavior of the radial pn junction cell, current-density versus voltage (J-V) curves (not shown) were calculated for planar and radial pn junction cells for Si and GaAs homojunctions. This section will focus on Si while the next will discuss the results for GaAs. This set of simulations used the Air Mass 1.5 Global (AM 1.5G) spectrum [43] and measured optical-absorption coefficients as a function of energy, $\alpha(E)$,

for Si and GaAs. [48] The current density J was calculated by numerically integrating over wavelength, at each value of the forward bias V, to obtain a value for the total current density as a function of bias.

Two regimes were treated - (1) the trap density in the quasineutral region was assumed to be independent of the trap density in the depletion region, with the trap density in the depletion region set at a low level such that depletion region traps had negligible effect on cell performance, and (2) the trap density was assumed constant through the material, and thus the minority-carrier lifetimes in the quasineutral region and in the depletion region were identical. For a solid-state device the latter scenario is likely to be more realistic, but treating the two cases separately allowed us to gain insight into the different regimes of cell performance. Also, depending on the specific fabrication process used to make the radial pn junction cell, the former regime may also be realizable. The lifetimes in the depletion region are given by [45]

$$\tau_{n0} = \frac{1}{\sigma_n N_r v_{th}}, \tag{2.49}$$

$$\tau_{p0} = \frac{1}{\sigma_p N_r v_{th}}, \tag{2.50}$$

where σ_n and σ_p are the cross sections for electron and hole capture, respectively, N_r is the density of recombination centers, and v_{th} is the thermal velocity. To first order, $\sigma_n = \sigma_p$, so that $\tau_{n0} = \tau_{p0}$.

In case (2), the high doping levels we considered (10^{18} cm^{-3}) implies that [47]

$$\tau_n \approx \tau_{n0}, \tag{2.51}$$

$$\tau_p \approx \tau_{p0}, \tag{2.52}$$

so that $\tau_n = \tau_p = \tau_{n0} = \tau_{p0}$, where τ_n is the lifetime of minority electrons in the p-type quasineutral region, and τ_p is the lifetime of minority holes in the n-type quasineutral region. In turn, these lifetime values yield values for L_n and L_p through the relations [45]

$$L_n = \sqrt{\tau_n D_n}, \tag{2.53}$$

$$L_p = \sqrt{\tau_p D_p}, \tag{2.54}$$

where

$$D_{n,p} = \frac{k_B T}{q} \mu_{n,p}. \tag{2.55}$$

Hence, given values for μ_n and μ_p, [52] in this case only one parameter, i.e. τ_n, needs to be specified to determine the values of τ_n, τ_p, τ_{n0}, τ_{p0}, L_n, and L_p.

In case (1), the assumption that $\tau_n = \tau_p$ and $\tau_{n0} = \tau_{p0}$ was retained, but τ_{n0} was held fixed (at 1 μs, or, equivalently, trap density N_r was held fixed at 10^{14} cm^{-3}, while τ_n was allowed to vary independently. Then the above relations were used to relate L_n and L_p to τ_n. This set of conditions simulated the situation in which the impurity profile was not constant throughout the sample. Case (1) led to quasineutral region recombination always being the dominant recombination mechanism, while in case (2) quasineutral region recombination dominated for $\tau_n \gtrsim 40$ ns, with depletion region recombination dominating for shorter lifetimes.

2.4.1 Preliminary Observations

The behavior of the cells was first investigated as a function of doping levels in the emitter and base, emitter thickness, and wire radius. Some general conditions for an optimal cell thus became apparent. At a given value of the minority-electron diffusion length, radial junction cells favored high doping. Furthermore, smaller wire radii necessitated high doping to prevent full depletion of the wire core. Carrier mobility is coupled to the doping in a well known fashion in Si, [52] the lifetime is related to the trap density in (2.49) and (2.50) above, and the mobility, lifetime, and diffusion length are related in (2.53)-(2.55). At a fixed trap density, increasing the doping will decrease the mobility and hence decrease the diffusion length. On the other hand, increasing the doping level will increase the built-in voltage, through (2.48). And because carriers travel a mean distance of one diffusion length through a quasineutral region before recombining, setting the wire radius approximately equal to the minority-electron diffusion length allows carriers to traverse the cell radially even if the diffusion length is low, provided that the trap density is relatively low in the depletion region.

Further insight into the differences between the two cell geometries was obtained by evaluating the efficiency η, V_{oc}, and J_{sc}, versus L and R for a radial pn junction cell (Figs. 2.7, 2.8, and 2.9). J_{sc} increased with increasing wire length, plateauing when the

length of the wire became much greater than the optical thickness of the material. Also, J_{sc} was essentially independent of wire radius, provided that the radius was less than L_n. The value of J_{sc} decreased steeply for $R > L_n$. J_{sc} was essentially independent of trap density in the depletion region.

The open circuit voltage V_{oc} decreased with increasing wire length, and increased with increasing wire radius. The extent to which V_{oc} decreased with increasing wire length depended strongly on the trap density in the depletion region: as the trap density became high ($> \sim 3 \times 10^{15}$ cm^{-3} for Si) in the depletion region, the V_{oc} declined rapidly. The trap density in the quasineutral regions, on the other hand, had relatively less effect on V_{oc}.

We can thus identify two regimes. In the regime of low depletion region trap density ($\lesssim 3 \times 10^{15}$ cm^{-3} for Si), in which quasineutral region recombination dominates depletion region recombination, V_{oc} is lost through the geometric increase in pn junction interface area γ, and the subsequent decrease in light-generated current relative to dark current, per unit junction area, as described above in Ch. 2.2, as well as in [49]. In the regime in which depletion region recombination dominates ($N_r \gtrsim 3 \times 10^{15}$ cm^{-3} for Si), the high trap density effectively greatly increases the dark current, in addition to the geometrical effects.

The optimal wire dimensions are obtained when the wire radius R is between about 0.5 and 1 times the minority carrier diffusion length in the core of the wires (L_n for a p-type core) and a length that is determined by the specific trade-off between the increase in J_{sc} and the decrease in V_{oc} with length (Figs. 2.7, 2.8, and 2.9). If the trap density in the depletion region is relatively low (i.e., $< \sim 3 \times 10^{15}$ cm^{-3} for Si), the maximum efficiency occurs for wires having a length approximately equal to the optical thickness (~ 125 μm for Si). For higher trap densities in the depletion region, shorter wire lengths are optimal.

Because majority carrier transport issues are neglected, this model shows that in the planar case the efficiency reaches a limiting value as the thickness increases. In contrast, the efficiency of the radial pn junction cell attains a maximum as a function of thickness - if the thickness is increased further, the efficiency is reduced. This behavior can be understood by realizing that the light-generated current density goes as

$$J_l \sim (1 - e^{-\alpha L}), \tag{2.56}$$

where α is the absorption coefficient of the material, and L is the cell thickness, while dark
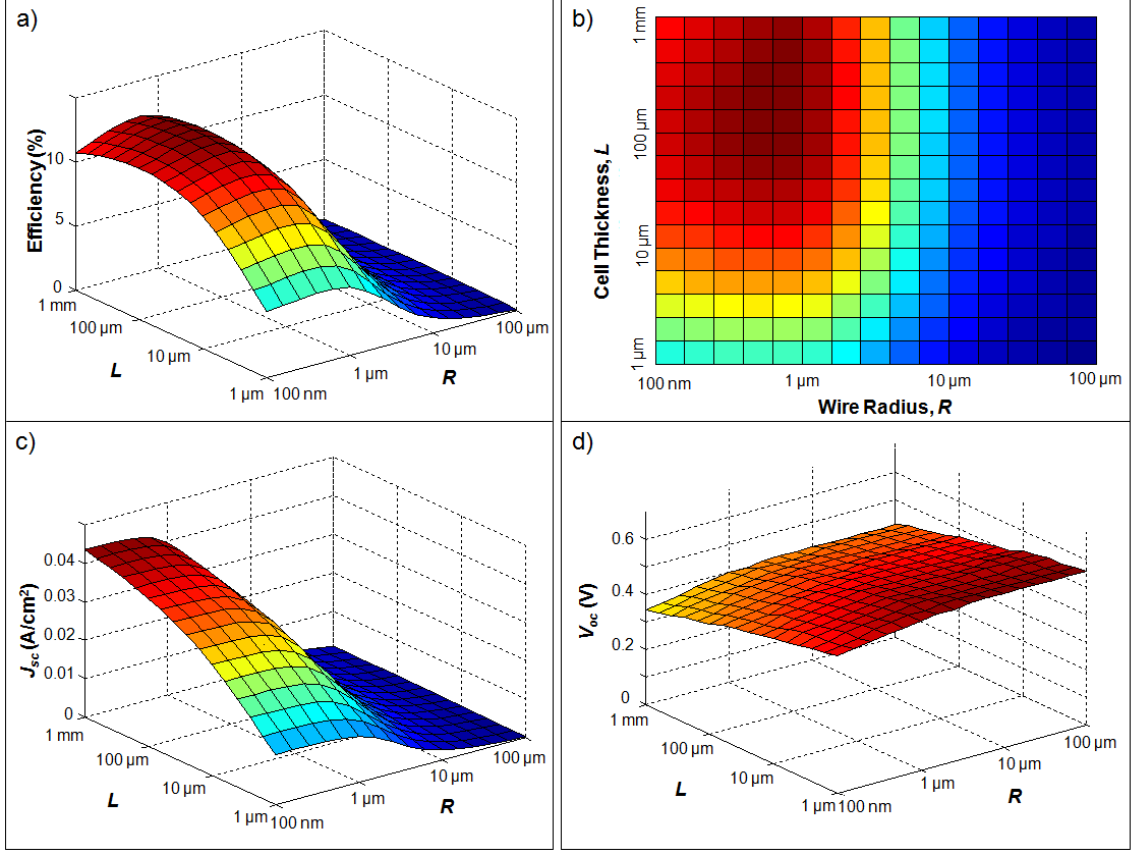
Figure 2.7. Example of (a) 3D and (b) plan views of efficiency η, and 3D views of (c) J_{sc}, and (d) V_{oc}, versus cell thickness L and wire radius R for a radial pn junction cell. This particular example is for a Si wire with $L_n = 1$ µm in the p-type core, with depletion region trap density fixed at 10^{14} cm^{-3}, and with surface recombination velocity S of 10^5 cm s^{-1} at the external surface of the wires. Note that peak efficiency is obtained when $L \approx 100$ µm and $R \approx 0.5$ - $1 \times L_n$.
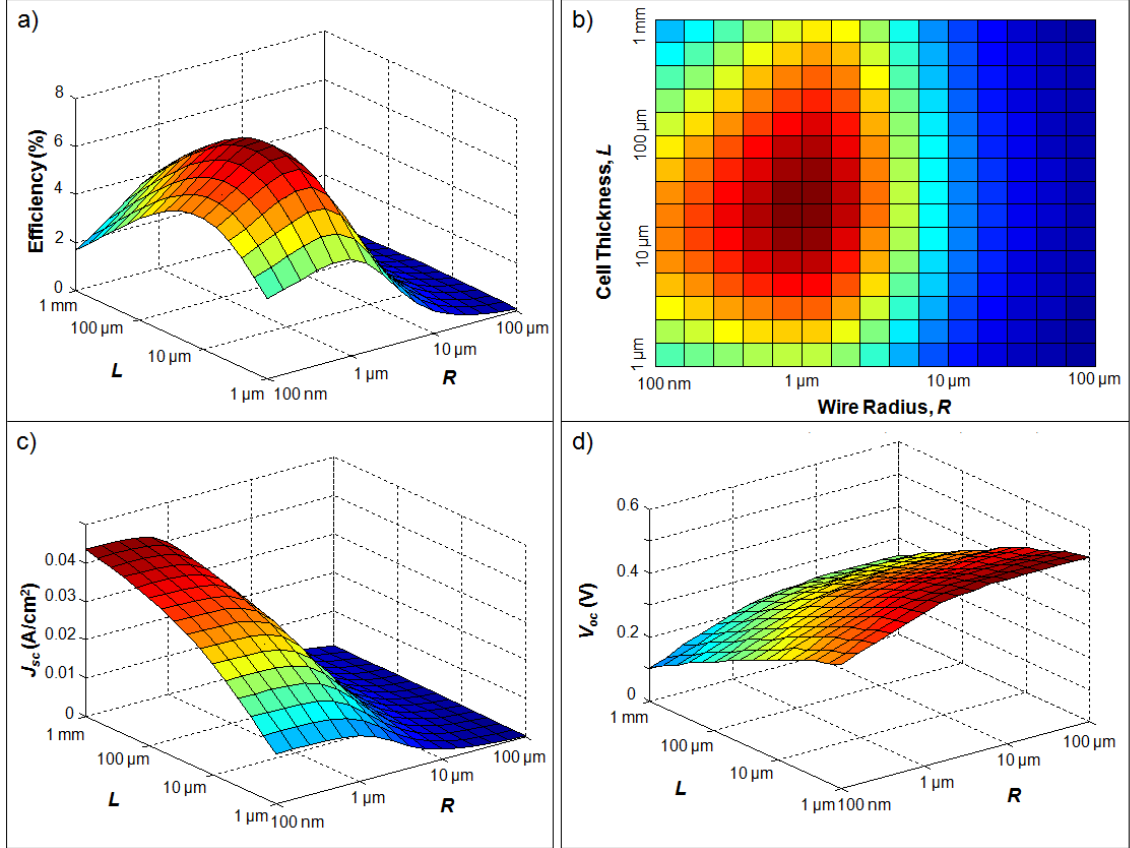
Figure 2.8. Example of (a) 3D and (b) plan views of efficiency η, and 3D views of (c) J_{sc}, and (d) V_{oc}, versus cell thickness L and wire radius R for a radial pn junction cell. This particular example is for a Si wire with $L_n = 1$ μm in the p-type core, with a homogeneous trap distribution, and with surface recombination velocity S of 10^5 cm s^{-1} at the external surface of the wires. Note that in this case of depletion region dominated recombination, optimal efficiency occurs at cell thicknesses of far less than 100 μm.
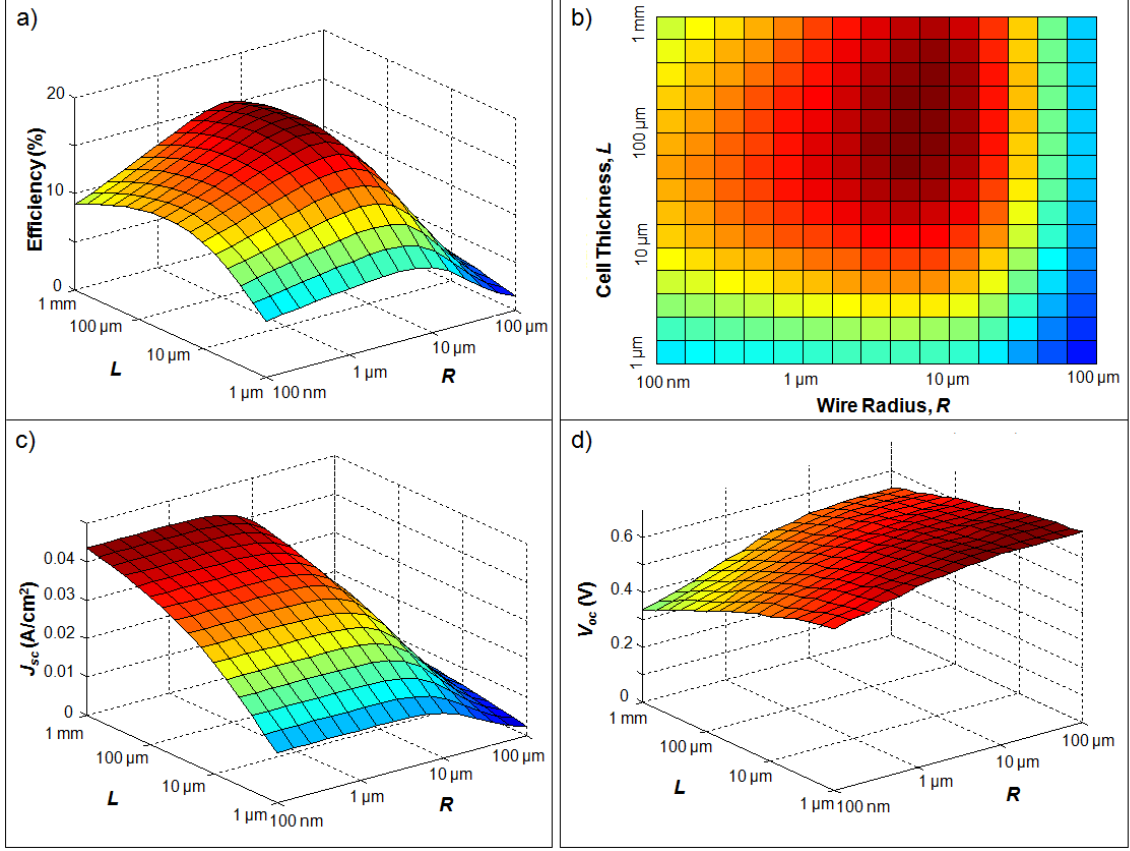
Figure 2.9. Example of (a) 3D and (b) plan views of efficiency η, and 3D views of (c) J_{sc}, and (d) V_{oc}, versus cell thickness L and wire radius R for a radial pn junction cell. This particular example is for a Si wire with $L_n = 10$ μm in the p-type core, with a homogeneous trap distribution, and with surface recombination velocity S of 1000 cm s^{-1} at the external surface of the wires. Note that peak efficiency is obtained when $L \approx 100$ μm and $R \approx 0.5$ - $1 \times L_n$.

current density goes as

$$J_0 \sim L. \tag{2.57}$$

The competition between these two effects determines the optimum thickness of the radial pn junction cell for maximum energy conversion efficiency.

2.4.2 Simulation Parameters

Given these observations, a comparison of the radial and planar junction geometries was undertaken in Si with the following parameters. An n^+ / p^+ structure was assumed, with the top layer and the external shell (the emitter) being n^+ in the planar and radial junction cells, respectively. The wire radius was set equal to the minority electron diffusion length L_n, a condition that was found to be near-optimal in all cases. In many cases the optimal radius was in fact less than L_n (with the optimal value tending to fall between 0.5 and 1 times the minority carrier diffusion length), but the difference in performance as R was varied in this range was small for our purposes (usually less than 0.5% absolute, whereas if R was increased significantly above L_n the drop in performance was much more significant). A fixed ratio between L_n and R simplified the analysis while allowing us to examine key features of the design. Other parameters were set as follows:

$$
\begin{aligned}
N_d &= 1 \times 10^{18} \text{ cm}^{-3}, \\
N_a &= 1 \times 10^{18} \text{ cm}^{-3}, \\
\mu_p &= 95 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}, \\
\Rightarrow D_p &= \frac{k_B T}{q} \mu_p = 2.46 \text{ cm}^2 \text{ s}^{-1}, \\
\mu_n &= 270 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}, \\
\Rightarrow D_n &= \frac{k_B T}{q} \mu_n = 6.98 \text{ cm}^2 \text{ s}^{-1}, \\
d_1 &= x_1 + x_2 \geq 1 \times 10^{-6} \text{ cm}, \\
S_p &= S_n = 1 \times 10^5 \text{ cm s}^{-1}, \\
\sigma_p &= \sigma_n = 1 \times 10^{-15} \text{ cm}^2, \\
v_{th} &= 1 \times 10^7 \text{ cm s}^{-1}, \tag{2.58}
\end{aligned}
$$

Figure 2.10. Short-circuit current density J_{sc} vs. cell thickness L and quasineutral region minority-electron diffusion length L_n for (a) a conventional planar pn junction Si cell and (b) a radial pn junction Si cell. In both cases the short-circuit current density is unaffected by decreasing the trap density in the depletion region. In the radial pn junction case, the cell radius R is set equal to L_n, a condition that was found to be near optimal.

where the $\geq$ symbol indicates that d_1 was set equal to 1×10^{-6} cm, unless this was too small to allow the full voltage drop V_{bi} to occur across the pn junction. In the latter case, d_1 was set equal to the minimum value required to achieve a voltage drop V_{bi}. The model assumes that the materials are not doped so heavily as to become degenerate; [45] also, the model does not account for Auger recombination. [53] Since these effects both become significant at higher dopings levels, the doping was not set to an even higher value.

2.4.3 Quasineutral Region Recombination Dominated Analysis

In the first analysis, the trap density in the quasineutral region was assumed to be independent of the trap density in the depletion region, with the trap density in the depletion region set at a low level (10^{14} cm^{-3}), such that depletion region recombination was included but had negligible effect on cell performance. This led to quasineutral region recombination dominated loss mechanisms at all parameters considered.

As shown in Fig. 2.10, the short-circuit current density J_{sc} in the Si wire cell is essentially independent of the trap density (recall, from Eqs. (2.49)-(2.54) above, that $L_n \propto 1/\sqrt{N_r}$), in stark contrast to the planar cell. For a 100-µm-thick silicon solar cell, J_{sc} in the radial pn junction geometry was ≈ 38 mA/cm^2 for thin (100 nm radius) wires, decreasing slightly

Figure 2.11. Open-circuit voltage V_{oc} vs. cell thickness L and quasineutral region minority-electron diffusion length L_n for (a) a conventional planar pn junction Si cell and (b) a radial pn junction Si cell. Depletion region trap density is held fixed at a relatively low level, $N_r = 10^{14}$ cm^{-3}, so that depletion region lifetime $\tau_{n0} = 1$ μs, leading to quasineutral region dominated recombination. In the radial pn junction case, the cell radius R is set equal to L_n, a condition that was found to be near optimal.

to ≈ 35 mA/cm^2 as the wire radius increased above 1 μm, whereas in the planar geometry J_{sc} dropped from 34 to 4 mA/cm^2 as τ_n decreased from 14 μs to 14 ps (so that L_n dropped from 100 μm to 100 nm in the quasineutral region of the p-type material). Note that a Si cell of thickness $L = 100$ μm is not optically thick, in that it absorbs less than 90% of the incident photons with energy above the bandgap (see 2.2 above). J_{sc} approached ~ 43 mA/cm^2 in both geometries as L_n approached 1 mm, in the limit of large L (> 1 mm). The radial pn junction design overcomes the problems of carrier collection that are present in the conventional planar geometry.

In this regime the open-circuit voltage could be relatively high even if the quasineutral-region trap density was large (Fig. 2.11). In the planar case, V_{oc} is nearly independent of cell thickness and decreases only mildly as the quasineutral region electron diffusion length decreases. In the radial pn junction case, V_{oc} decreases as the cell thickness increases because the junction area increases. Also, V_{oc} decreases as the electron diffusion length decreases in the quasineutral region, but again in a relatively mild fashion. For a 100-μm-thick silicon solar cell, the open-circuit voltage in the radial pn junction geometry only dropped from 0.58 to 0.38 V as τ_n in the quasineutral regions decreased from 1.4 μs to 14 ps, if τ_{n0} in
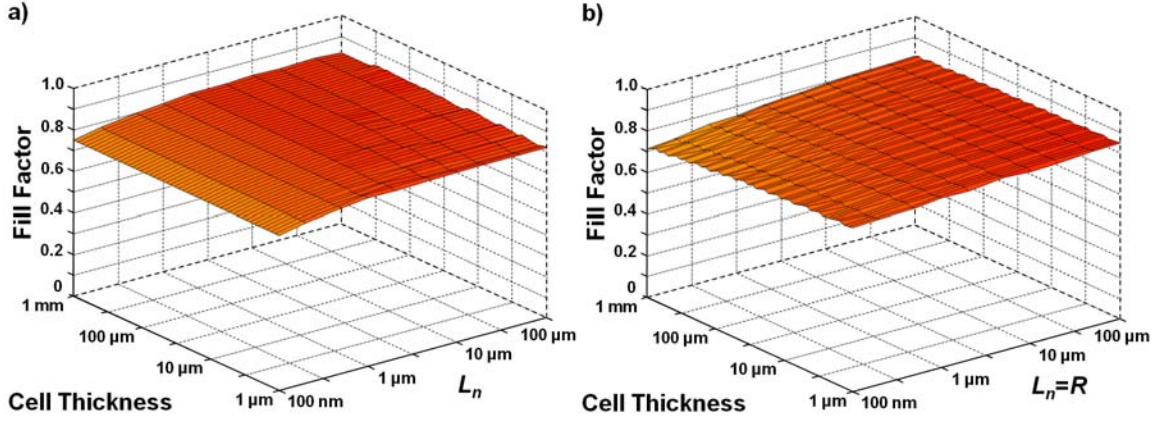
Figure 2.12. Fill factor FF vs. cell thickness L and quasineutral region minority-electron diffusion length L_n for (a) a conventional planar pn junction Si cell and (b) a radial pn junction Si cell. Depletion region trap density is held fixed at a relatively low level, $N_r = 10^{14}$ cm^{-3}, so that depletion region lifetime $\tau_{n0} = 1$ μs, leading to quasineutral region dominated recombination. In the radial pn junction case, the cell radius R is set equal to L_n, a condition that was found to be near optimal.

the depletion region was held fixed at 1 μs. In the planar geometry the open-circuit voltage dropped from 0.59 to 0.49 V over the same range.

The fill factor was nearly constant at ~ 0.8 as a function of L and L_n for both planar and radial geometries in this regime, reaching a maximum of ~ 0.84 within the range of L, R, and L_n considered (Fig. 2.12).

Taken together, the factors discussed above meant that the efficiency of the radial pn junction solar cell remained high despite a high quasineutral-region trap density (Fig. 2.13). In the planar geometry, a high quasineutral-region trap density led to a very low J_{sc}. This behavior inevitably results in a low efficiency for such systems (Fig. 2.13(a)). In contrast, for the radial pn junction, J_{sc} can attain high values even for very large trap densities in the quasineutral regions. V_{oc}, and thus the overall efficiency, can remain high.

For a Si solar cell with $L_n = 100$ nm (so that $\tau_n \approx 14$ ps) in the quasineutral regions and $\tau_{n0} = 1$ μs in the depletion region, the maximal efficiency of the radial pn junction geometry was 11%, compared with 1.5% in the planar geometry. This maximal efficiency occurred for a radial pn junction cell between 20 and 500 μm thick, whereas the efficiency saturated for a planar cell thicker than 450 nm. For a Si solar cell with $L_n = 1$ μm (so

Figure 2.13. Efficiency η vs. cell thickness L and quasineutral region minority-electron diffusion length L_n for (a) a conventional planar pn junction Si cell and (b) a radial pn junction Si cell. Depletion region trap density is held fixed at a relatively low level, $N_r = 10^{14}$ cm^{-3}, so that depletion region lifetime $\tau_{n0} = 1$ μs, leading to quasineutral region dominated recombination. In the radial pn junction case, the cell radius R is set equal to L_n, a condition that was found to be near optimal.

that $\tau_n \approx 1.4$ ns) in the quasineutral regions and $\tau_{n0} = 1$ μs in the depletion region, the maximal efficiency of the radial pn junction geometry was 13%, compared with 5% in the planar geometry. This maximal efficiency occurred for a radial pn junction cell between 100 and 240 μm thick, whereas the efficiency saturated in the planar geometry when thickness exceeded 5 μm.

2.4.4 Homogeneous Trap Distribution Analysis

The situation was also analyzed in the case that $\tau_{n0} = \tau_{p0} = \tau_n = \tau_p$, so that the trap density was assumed constant through the material. In this case, quasineutral region recombination was the dominant loss mechanism only until some critical value of depletion region trap density (or, equivalently, of τ_{n0} and τ_{p0}), and for trap densities above this, depletion region recombination began to dominate.

The results for J_{sc} are shown above in Fig. 2.10. These results, for both planar and radial pn junction cells, were unaffected by changing the trap density in the depletion region.

The degree to which V_{oc} varied with the trap density depended most strongly on the trap density in the depletion region, for both the radial pn junction case and for the planar
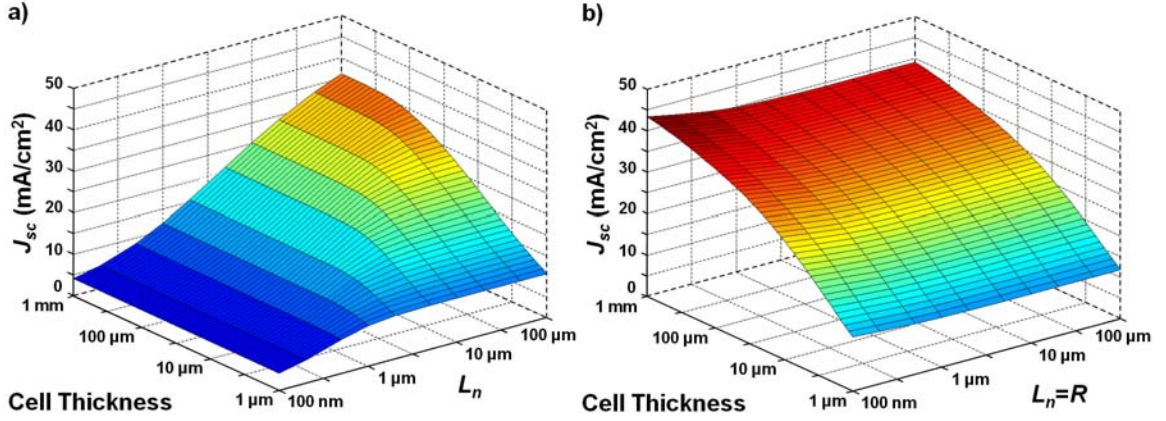
Figure 2.14. Open-circuit voltage V_{oc} vs. cell thickness L and quasineutral region minority-electron diffusion length L_n for (a) a conventional planar pn junction Si cell and (b) a radial pn junction Si cell. Depletion region trap density is set equal to quasineutral region recombination density, leading to depletion region dominated recombination at low values of L_n. In the radial pn junction case, the cell radius R is set equal to L_n, a condition that was found to be near optimal.

case (Fig. 2.14). In the planar case, the open-circuit voltage is independent of cell thickness and decreases as the quasineutral region electron diffusion length decreases - slowly until L_n dropped to ~ 2 µm, and more rapidly as L_n dropped below this value. In the radial pn junction case, the open-circuit voltage decreases as the cell thickness increases because the junction area increases. Also, the open-circuit voltage decreases as the electron diffusion length decreases in the quasineutral region - slowly until L_n dropped to a critical value, and more rapidly as L_n dropped below this value. What this critical value was depended on the thickness of the cell L. With $L = 100$ µm, this value was ~ 5 µm. For a 100-µm-thick Si solar cell, V_{oc} in the radial pn junction geometry dropped from 0.58 to 0.01 V as τ_n decreased from 1.4 µs to 14 ps. In the planar geometry, V_{oc} dropped from 0.59 to 0.24 V over the same range.

In this regime, the fill factor was nearly constant at ~ 0.8 as a function of L and L_n for both planar and radial geometries except for $L_n \leq 5$µm (i.e., for $\tau_n \lesssim 40$ ns), when the fill factor began to drop, steeply for the radial pn junction cell and more gradually for the planar cell (Fig. 2.15).

Taken together, the factors discussed above imply that depletion-region trap density

Figure 2.15. Fill factor FF vs. cell thickness L and quasineutral region minority-electron diffusion length L_n for (a) a conventional planar pn junction Si cell and (b) a radial pn junction Si cell. Depletion region trap density is set equal to quasineutral region recombination density, leading to depletion region dominated recombination at low values of L_n. In the radial pn junction case, the cell radius R is set equal to L_n, a condition that was found to be near optimal.
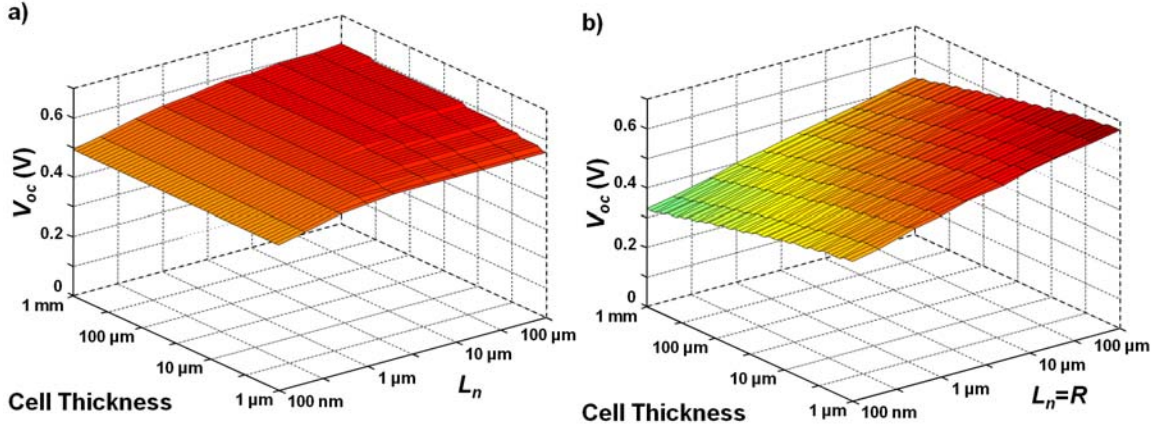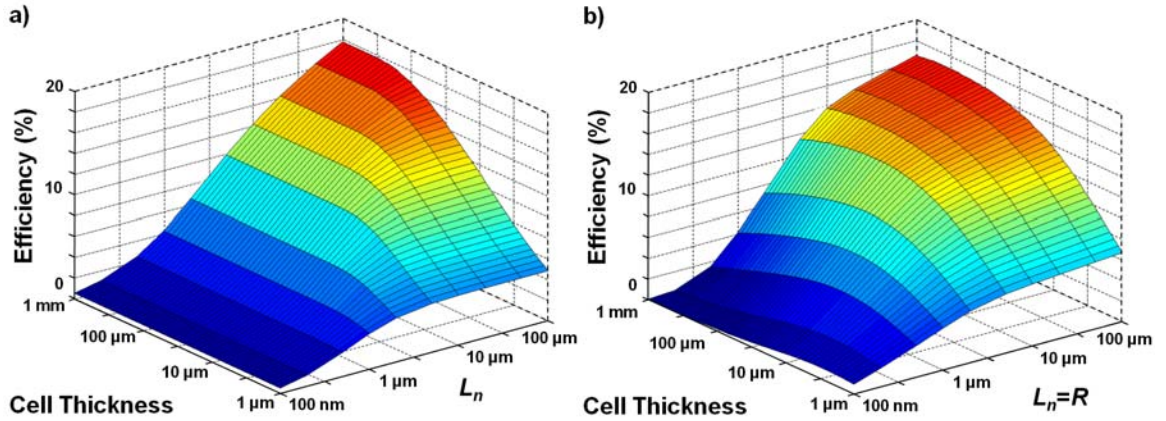

Figure 2.16. Efficiency η vs. cell thickness L and quasineutral region minority-electron diffusion length L_n for (a) a conventional planar pn junction Si cell and (b) a radial pn junction Si cell. Depletion region trap density is set equal to quasineutral region recombination density, leading to depletion region dominated recombination at low values of L_n. In the radial pn junction case, the cell radius R is set equal to L_n, a condition that was found to be near optimal.

limits the ability of the radial geometry to ameliorate the negative effects of low diffusion length. Specifically, for a radial junction Si cell of thickness $L = 100$ μm, a change in slope appears in the efficiency vs. L_n relationship at $L_n \approx 5$ μm (Fig. 2.16). As L_n drops below this value, depletion region recombination dominates, and efficiency drops much more rapidly with decreasing minority carrier lifetime.

For a Si solar cell with τ_n set to 14 ps throughout the cell, so that $L_n = 100$ nm, the maximal efficiency of the radial pn junction geometry was 1%, compared with 0.5% in the planar geometry. In this case, the maximal efficiency occurred for a radial pn junction cell between 1 and 30 μm thick, whereas the efficiency saturated for a planar cell thicker than 1 μm. For a Si cell with τ_n set to 1.4 ns throughout the cell, so that $L_n = 1$ μm, the maximal efficiency of the radial pn junction geometry was 7%, compared with 4% in the planar geometry. In this case, the maximal efficiency occurred for a radial pn junction cell between 5 and 100 μm thick, whereas the efficiency saturated for a planar cell thicker than 5 μm. For a Si cell with τ_n set to 36 ns throughout the cell, so that $L_n = 5$ μm, the maximal efficiency of the radial pn junction geometry was 13%, compared with 10% in the planar geometry. For a Si cell with τ_n set to 140 ns throughout the cell, so that $L_n = 10$ μm, the maximal efficiency of the radial pn junction geometry was 14%, compared with 12% in the planar geometry.

Note that these simulations were performed with a surface recombination velocity $S = 1 \times 10^5$ cm s^{-1} assumed throughout, and this limits the maximum efficiency attainable in the radial geometry when quasi-neutral region recombination dominates depletion region recombination. Also, setting $R = L_n$ was only approximately optimal. As seen in Fig. 2.9, the maximum efficiency observed when τ_n was set to 140 ns throughout the cell, so that $L_n = 10$ μm, with $S = 1000$ cm s^{-1}, was $\eta = 16.8$ %, when the wire radius $R = 5.5$ μm, and wire length $L = 90$ μm. In this case, $J_{sc} = 0.0369$ A cm^{-2}, $V_{oc} = 0.588$ V, and FF = 0.775. Decreasing S to 100 cm s^{-1} only increased the efficiency to 16.9 %. On the other hand, with $S = 1 \times 10^4$ cm s^{-1}, the maximum efficiency was 16.2 %, and with $S = 1 \times 10^5$ cm s^{-1}, the maximum efficiency dropped further to 14.9 %, all at optimal radii $R = 5.5$ μm.

Our group has recently reported the ability to grow Si wires with minority carrier diffusion lengths of ≈ 10 μm when using Ni as a growth catalyst, [54] by techniques that will be discussed in Ch. 4, which makes the above simulations potentially of great relevance

in anticipating performance limits in practical devices. With Au-catalyzed Si wires, our group has measured minority carrier diffusion lengths of $\approx$ 2 µm, [55] which is therefore a diffusion length worth considering in more detail also. Setting $\tau_n = 57$ ns throughout the cell, so that $L_n = 2$ µm, the maximal efficiency observed in the simulations was $\eta = 10.0$ %, when the wire radius $R = 1.5$ µm, and wire length $L = 30$ µm. In this, depletion region recombination dominated case, surface recombination effects are much less important, and the maximum efficiency was unchanged for S ranging from 100 cm s^{-1} up to 1×10^5 cm s^{-1}. In this case, $J_{sc} = 0.0324$ A cm^{-2}, $V_{oc} = 0.453$ V, and $FF = 0.684$. Under these conditions, increasing the wire length to 100 µm resulted in a drop in efficiency to 9.6 %.

In the case of homogeneous trap distributions, optically thick wires (i.e. with $L \approx 100$ µm) were optimal only when $L_n \gtrsim 10$ µm, i.e. $\tau_n \gtrsim 100$ ns. For lower lifetime material, the penalty associated with increased junction and surface area associated with increased wire length outweighed the benefits of increased light absorption. Insofar as we believe that the homogeneous trap density analysis is a more realistic model for what we are likely to see with solid state junctions in grown wire arrays, these results set targets for material quality as well as aspect ratio for this device geometry to be of relevance as a PV technology. Namely, in growing Si wires for use in a radial pn junction geometry, one would like to grow wires with microscopic rather than nanoscopic dimensions, and with diffusion lengths $L_n \gtrsim$ 10 µm (equivalently, lifetimes of $\gtrsim$ 100 ns).

2.5 Application to Direct Band Gap Semiconductors

The simulations were also performed for a gallium arsenide (GaAs) homojunction cell. GaAs was chosen because it is an archetypal direct band-gap semiconductor, whose transport and optical properties are well known. GaAs is also a good light absorber compared with Si (Fig. 2.3), in that the optical thickness of GaAs is 140 times less than that of Si (891 nm for GaAs compared with 125 µm for Si). Thus, Si and GaAs represent two extremes with regard to absorption.

The following parameters were taken as a baseline scenario for the GaAs cells: [56]
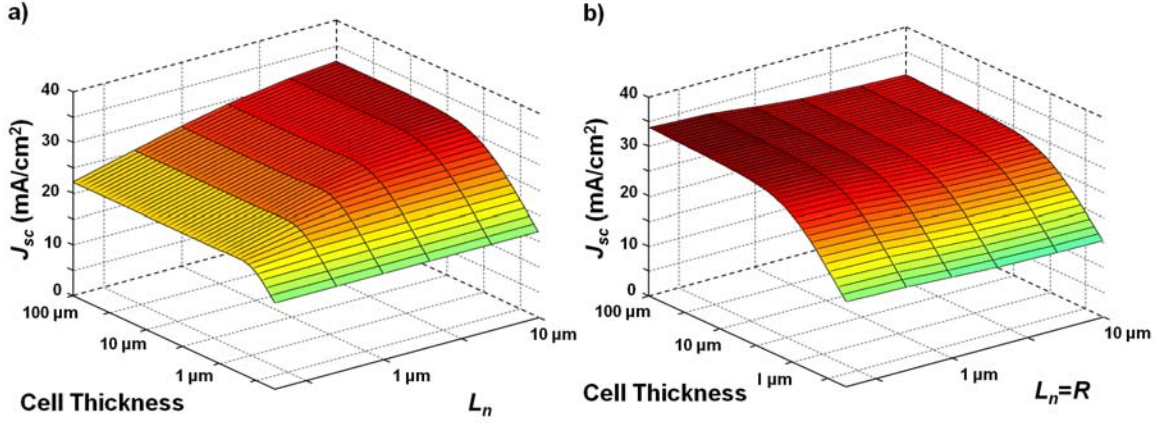
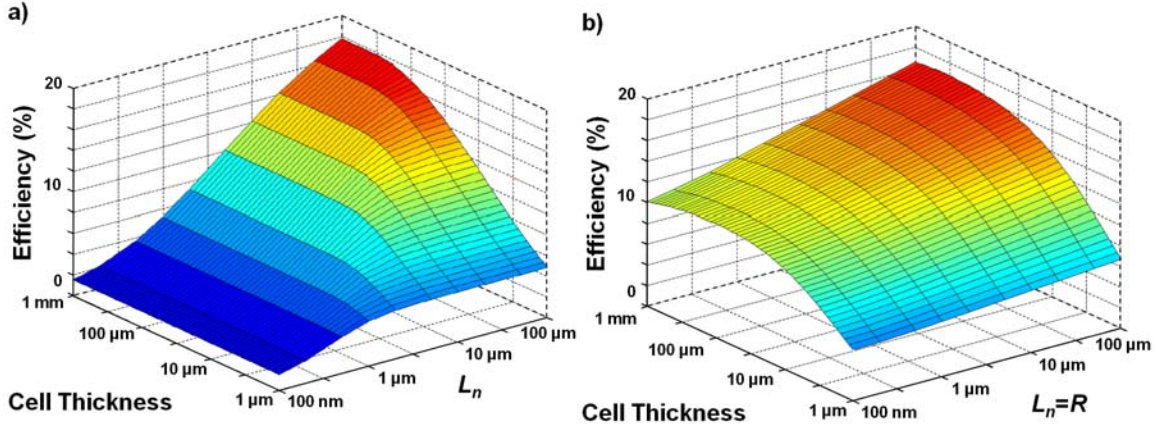Figure 2.17. Short-circuit current density J_{sc} vs. cell thickness L and quasineutral region minority-electron diffusion length L_n for (a) a conventional planar pn junction GaAs cell and (b) a radial pn junction GaAs cell. In both cases the short-circuit current density is unaffected by decreasing the trap density in the depletion region. In the radial pn junction case, the cell radius R is set equal to L_n, a condition that was found to be near optimal.

$$N_d = 1 \times 10^{17} \text{ cm}^{-3},$$

$$N_a = 1 \times 10^{17} \text{ cm}^{-3},$$

$$\mu_p = 320 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1},$$

$$\Rightarrow D_p = \frac{k_B T}{q} \mu_p = 8.27 \text{ cm}^2 \text{ s}^{-1},$$

$$\mu_n = 5000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1},$$

$$\Rightarrow D_n = \frac{k_B T}{q} \mu_n = 129 \text{ cm}^2 \text{ s}^{-1},$$

$$d_1 = x_1 + x_2 \geq 1 \times 10^{-6} \text{ cm},$$

$$S_p = S_n = 1 \times 10^5 \text{ cm s}^{-1},$$

$$\sigma_p = \sigma_n = 1 \times 10^{-15} \text{ cm}^2,$$

$$v_{th} = 1 \times 10^7 \text{ cm s}^{-1}, \tag{2.59}$$

As for Si, the maximum doping level was limited by the need to have a nondegenerate material, the recombination in which is not dominated by Auger processes. [57]

The results for J_{sc}, V_{oc}, and overall cell efficiency η for GaAs are presented in Figs. 2.17,
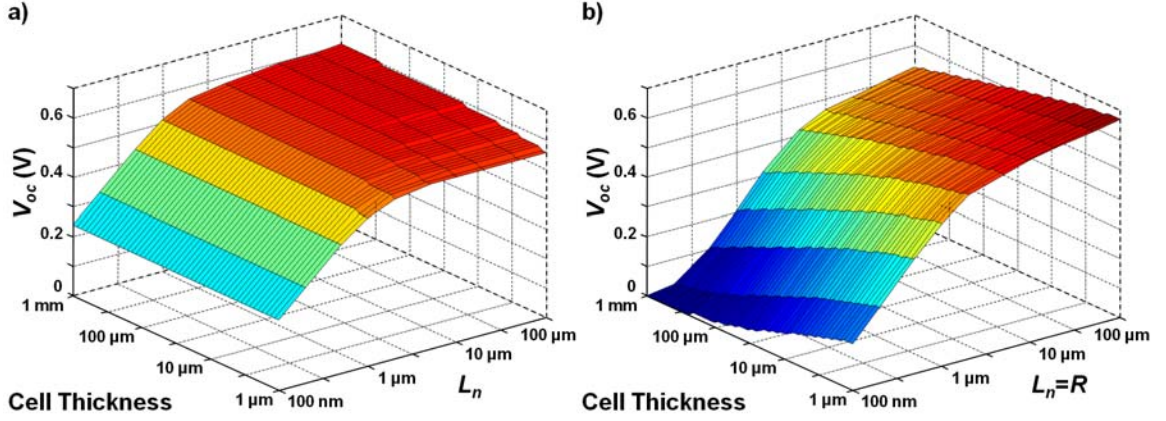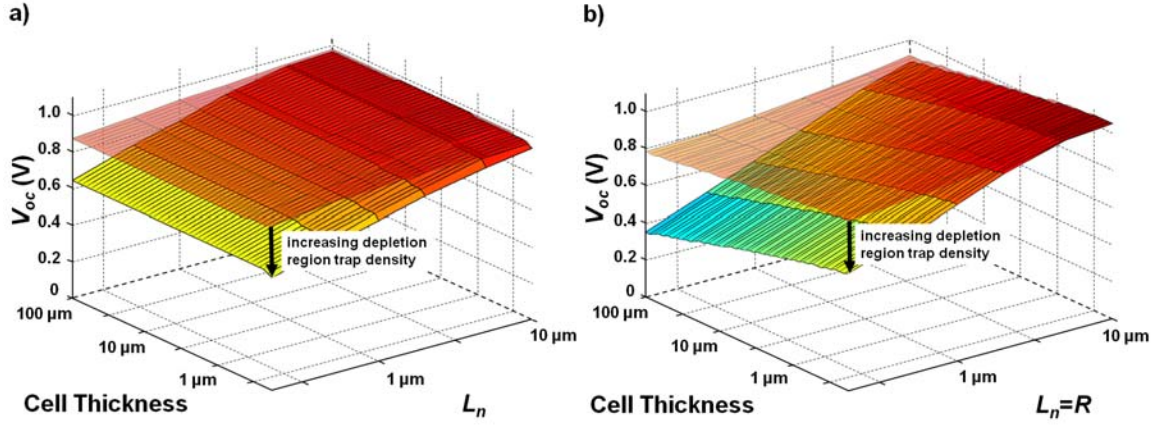
Figure 2.18. Open-circuit voltage V_{oc} vs. cell thickness L and quasineutral region minority-electron diffusion length L_n for (a) a conventional planar pn junction GaAs cell and (b) a radial pn junction GaAs cell. In both cases the top surface shown in the plot has a depletion region trap density fixed at 10^{14} cm^{-3}, while the bottom surface has a depletion-region trap density equal to the trap density in the quasineutral region, at each value of L_n. In the radial pn junction case, the cell radius R is set equal to L_n, a condition that was found to be near optimal.
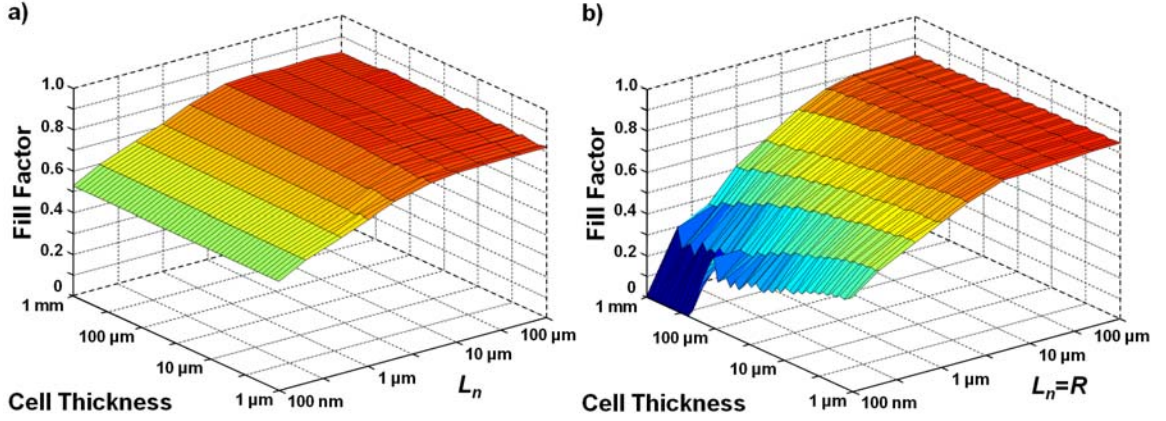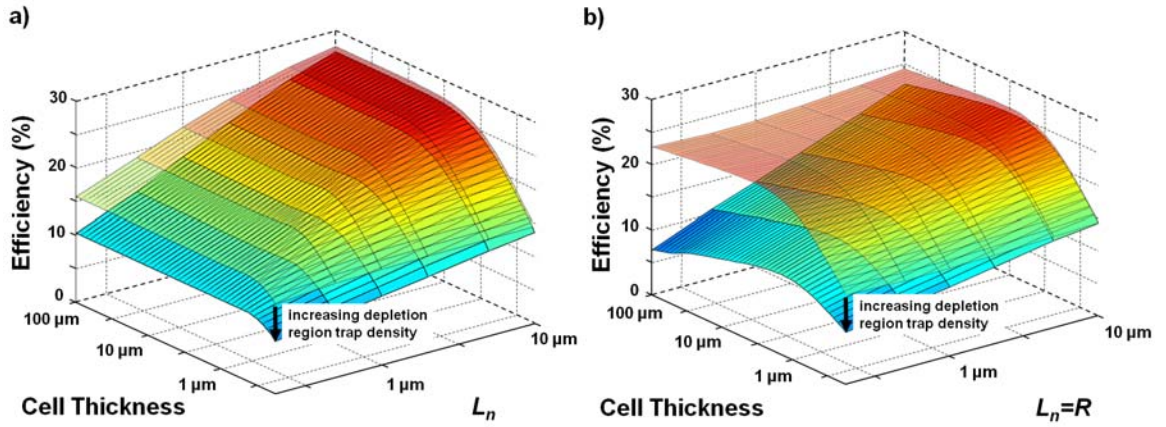

Figure 2.19. Efficiency η vs. cell thickness L and quasineutral region minority-electron diffusion length L_n for (a) a conventional planar pn junction GaAs cell and (b) a radial pn junction GaAs cell. In both cases the top surface shown in the plot has a depletion region trap density fixed at 10^{14} cm^{-3}, while the bottom surface has a depletion-region trap density equal to the trap density in the quasineutral region, at each value of L_n. In the radial pn junction case, the cell radius R is set equal to L_n, a condition that was found to be near optimal.

2.18, and 2.19, respectively. Clearly, the performance difference between the planar and radial pn junction structures for GaAs is not nearly as dramatic as that for Si. This is due simply to the change in the relative length scales involved with the direct band-gap material. As noted above, the optical thickness of GaAs is 891 nm. Therefore, severely collection-limited GaAs planar cells must have diffusion lengths much less than 891 nm, i.e., on the order of 100 nm or less. Recall also that the dopant density determines the depletion region width, with higher doping leading to thinner depletion regions. Nondegenerate doping implies that depletion regions in GaAs are on the order of hundreds of nanometers (191 nm for the planar case in our simulation). In the radial geometry the depletion region width depends upon the value of x_4, with 191 nm setting a lower bound. Making a radial pn junction with a radius equal to the minority-electron diffusion length, that is, less than $\sim$ 100 nm for severely collection-limited GaAs, would thus result in fully depleted pn junctions. This is a problem for several reasons. Firstly, a fully depleted cell cannot attain its full built-in voltage as given in Eq. 2.48, and the built-in voltage drops rapidly as the cell radius decreases further. Secondly, one might expect majority carrier transport to become more complicated in a fully-depleted wire because in this case the majority carriers are always in the presence of a strong electric field. One might expect that this could dramatically increase the effects of surface and junction recombination, and/or lead to other majority carrier transport issues not dealt with here. Thirdly, a fully depleted cell by definition has no quasineutral region; therefore, the concept of keeping the trap density in the depletion region low while the trap density in the quasineutral regions increases is meaningless. If the cell is fully depleted, then the lifetime in the depletion region, which needs to be high, is in fact the lifetime in the whole wire, and this defeats the whole concept of using lower lifetime material in the radial pn junction geometry. Finally, a fully depleted wire can no longer be adequately modeled by assuming purely radial minority carrier transport, because in this case the minority carriers are never swept into a quasineutral region in which they are majority carriers, and so ignoring majority carrier transport effects, as we have in the preceding analysis, may no longer be valid.

Note, however, that, as for the Si case, J_{sc} in the radial pn junction cell does not decrease with increasing trap density. This is not true in the planar geometry. Thus, it may be possible that degenerately doped GaAs wires with radial pn junction could exhibit some of the performance advantages seen in nondegenerately doped Si. This, however, is

left to the subject of a future study that deals explicitly with the transport and statistics of degenerately doped systems.

2.6   Axial pn Junction Wire Solar Cells

One can also envision forming a wire array solar cell with axial junctions. This may be of particular relevance if one is able to grow wire material with diffusion lengths that approach or exceed the optical thickness of the material, and/or if passivation of the external surfaces of the wires proves to be easier than the formation of a high-quality pn junction in the radial direction.

In the limit of negligible surface recombination at the external surface of the wires, the axial pn junction wire cell will behave identically to the planar cell (given that we are ignoring for now any optical absorption effects of the wire arrays, or potential loss of current density due to less than 100 % packing fraction of the wires). We therefore expect axial junction wires to behave similarly to the planar simulations, with an additional loss term due to surface recombination appearing when surface recombination velocity (S) becomes large enough.

Some general design principles then immediately become apparent. Even in the case that $S = 0$ cm s^{-1} on all surfaces, in the case where the minority carrier diffusion length is less than the optical thickness of the material, there will be little or no benefit to making the wires significantly longer than the diffusion length of minority carriers. i.e. the wire length should be comparable to the optical thickness of the material, or to the minority carrier diffusion length in the base, whichever is smaller. For $S > 0$ cm s^{-1} on the external ($r = $ R) surface of the wires, one might expect that the optimal length would tend to be decreased, for, as S increases the external surface of the wire acts as an increasingly strong "sink" for minority carriers relative to the pn junction.

Indeed, one might expect surface recombination at the external surfaces of the wires to be far more important in the axial junction case than in the radial. To the extent that the radial pn junction can shield minority carriers in the core of a wire from "seeing" the external surface of the wires, surface recombination is of relatively lesser importance compared with junction recombination, in the radial pn junction design. On the other hand, in an axial-junction wire of high aspect ratio, minority carriers within a diffusion length of

both the wire surface and the pn junction can potentially recombine at surface sites rather than be swept across the junction. For minority carriers within a diffusion length of the wire surface, but further than a diffusion length from the pn junction, recombination at the surface is a more likely fate. Therefore, another first-order design criterion would be to make the wire radii as large as possible. There is apparently nothing to be gained by going to smaller diameters in the axial pn junction geometry (except possibly in terms of advantageous light-trapping effects that may be possible with structures whose diameters are on the order of the wavelength of light).

Given that our primary interest in modeling this geometry was to determine an upper limit on acceptable surface recombination velocities for wire surfaces, we first identified a qualitative solution that demonstrates the effects of changing surface recombination. This was done solving the appropriate one-dimensional problems in the r and z directions in this geometry, and taking the carrier concentration as the square root of the product of these two solutions, at each value of r and z. While the solutions thus generated are not quantitatively correct, nevertheless they display many of the qualitative trends with respect to S that we would expect to see (not shown).

In order to obtain a more accurate solution, we then took the above qualitative solution as the input for a two-dimensional, finite element solver (the MatLab code for which is reproduced in Appendix A.3). Assuming an axial pn junction structure as shown in Fig. 2.6, with an n-type emitter of thickness d_1 and a p-type base of thickness d_2, this code calculates the minority carrier density at all values of r and z specified by the mesh chosen, in both p- and n-type quasineutral regions (the depletion region is ignored, which is more defensible here than in the radial pn junction case because depletion region volume is not a function of wire aspect ratio, and because for this geometry to be useful for indirect bandgap semiconductors, the lifetime, and therefore the diffusion length, of minority carriers will have to be relatively large in any case). The current density can then be calculated by integrating the carrier density gradient in the z-direction over the plane of the pn junction, for both carrier types. For example, the current density due to electrons in the p-type quasineutral region, J^p, is given by

$$J^p = \frac{2 \int_0^R r J^p(r)\, dr}{R^2},$$
(2.60)

where

$$J^p\left(r\right) = -qD_n \left.\frac{\partial n'}{\partial z}\right|_{z=d_1}, \tag{2.61}$$

and R and L are the radius and length of the wire, respectively.

Shown in Fig. 2.20 is the minority electron concentration in an axial junction wire as a function of z and r position, for a wire of radius 2.5 μm and 10 μm length, with S on the external ($r = 2.5$ μm) surface of (a) 10^5 cm s^{-1}, (b) 10^4 cm s^{-1}, and (c) 1000 cm s^{-1}. In all cases light is incident parallel to the wire axis on the $z = 0$ μm surface (and reflection effects are ignored), the emitter is negligibly thin, the minority electron diffusion length L_n = 10 μm, applied bias = 0 V, and $S = 1$ cm s^{-1} at the $z = 10$ μm surface. As S at the external surface is decreased, the calculated current density varies from 0.0052 A/cm^2 when $S = 10^5$ cm s^{-1}, to 0.011 A/cm^2 when $S = 10^4$ cm s^{-1}, 0.020 A/cm^2 when $S = 1000$ cm s^{-1}, and 0.024 A/cm^2 when $S = 100$ cm s^{-1} and when $S = 10$ cm s^{-1}. Similar trends were seen when the wire radius was set to 5 μm.

This and other preliminary studies indicate that we may need to aim for surface recombination velocities of $\lesssim 1000$ cm s^{-1} on wire sidewalls (however, the exact value presumably depends in detail on the wire length and radius, and the minority carrier diffusion length in the base). Notice in Fig. 2.20 that at higher values of surface recombination velocity the carrier density drops away significantly towards the wire surface. Also, the magnitude of minority carrier density even relatively far from the wire surface is dragged down, indicating that recombination at the external surface is interfering with carrier collection at the junction for carriers throughout the wire.

These results, while interesting, are very preliminary. Making the solver more robust to changes in step-size, tolerance, and spatial mesh size would be important steps to be taken, if this approach is to be pursued in the future.

2.7 Conclusion

In summary, the radial pn junction geometry has the potential to produce significant improvements in the efficiencies of PV cells made from materials that have diffusion lengths that are low relative to their optical thickness. It is crucial that the trap density near the pn junction is low enough that depletion region recombination does not dominate, otherwise large losses in V_{oc} are predicted to occur. In homogeneous materials this sets a limit on the
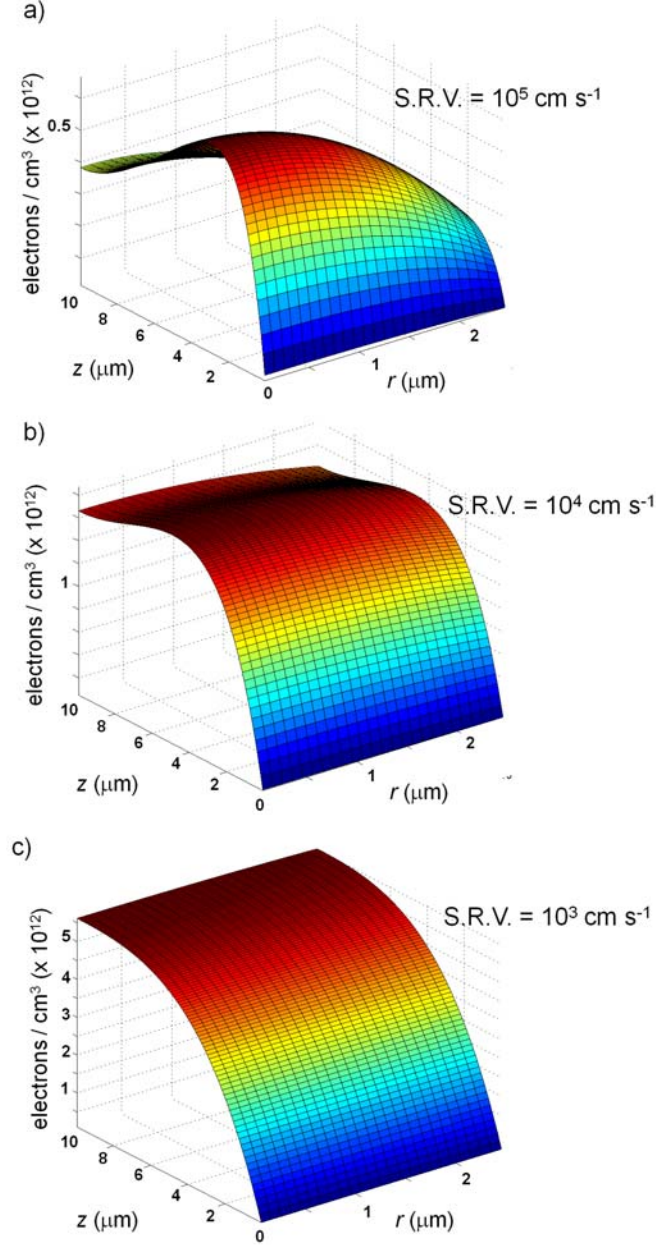
Figure 2.20. Minority electron concentration in an axial junction wire as a function of z and r position, for surface recombination velocities S on the external ($r = 2.5$ μm) surface of (a) 10^5 cm s^{-1}, (b) 10^4 cm s^{-1}, and (c) 1000 cm s^{-1}. In all cases light is incident parallel to the wire axis on the $z = 0$ μm surface (and reflection effects are ignored), the emitter is negligibly thin, the wire radius $= 2.5$ μm, the wire length $= 10$ μm, the minority electron diffusion length $L_n = 10$ μm, applied bias $= 0$ V, and $S = 1$ cm s^{-1} at the $z = 10$ μm surface.

extent to which the radial pn junction geometry can ameliorate the effects of poor material quality, and for Si we predict that minority carrier diffusion lengths of $\gtrsim$ 5 μm (equivalently, lifetimes of $\gtrsim$ 40 ns) will be required to fabricate a moderate efficiency PV device, even in the radial geometry. We predict that even larger diffusion lengths ($L_n \gtrsim$ 10 μm, or $\tau_n \gtrsim$ 100 ns) will be required to ensure that a cell can be optically thick without being penalized by the relatively large junction area that an optically-thick cell implies. Thus far it appears that this geometry will be of little benefit for direct bandgap semiconductors, primarily because in these materials the depletion region width will likely be comparable to the optical thickness of the material.

An optimally designed radial pn junction wire array cell should be doped as highly as possible in both n- and p-type regions (without producing additional reductions in diffusion lengths, or incurring significant losses due to Auger recombination or tunneling), and have a narrow emitter width, while ensuring that neither the n- nor the p-type regions are fully depleted. The wires that comprise the cell should have a radius between about 0.5 and 1 times the diffusion length of electrons in the p-type core (or of holes if the core is n-type), i.e.,

$$\frac{L_n}{2} \gtrsim R \gtrsim L_n, \tag{2.62}$$

(in qualitative agreement with [58]). The wire lengths should approximately equal the optical thickness of the material, i.e.,

$$L \approx 1/\alpha. \tag{2.63}$$

For Si that is not depletion region recombination dominated, this implies that an optimal cell should have $L_n \gtrsim$ 10 μm, $R \gtrsim$ 5 μm, and $L \approx$ 100 μm, i.e., microscopic, rather than nanoscopic, feature sizes are desired. Obviously, one would want the material to have as large a value for L_n as possible, and R tuned appropriately.

Axial junction wire cells may be of interest in the case that diffusion length can be made large enough (i.e., a significant fraction of the optical thickness of the material). In this case, surface recombination is expected to be of crucial importance in attaining an efficient device. Preliminary work suggests that surface recombination velocities of 1000 cm s^{-1} or lower may be required to reach the potential of this geometry (although this depends in detail on the wire length and radius, and the minority carrier diffusion lengths, and awaits

further study).

We anticipate that the results presented here can motivate the design of new types of radial junction and/or wire array solar cells that may enable efficient carrier collection in inorganic, organic, or dye-based solar absorber materials where minority-carrier transport limits cell performance. Future modeling work should target full 2D and 3D numerical simulation that includes the effects of majority carrier transport and deviations from 1D minority carrier transport. Commercial packages such as Sentaurus seem ideally suited to this task. Also, there is much scope for detailed optical simulations of these devices.

Chapter 3

Vapor Liquid Solid Growth of Si Wires from SiH$_4$

3.1 Introduction

In order to realize a radial pn junction wire array solar cell experimentally in Si, we are interested in exploring the fabrication of densely-packed, well-oriented arrays of Si wires, with diameters in the range ~ 1 μm and larger, and lengths of ~ 100 μm (potentially less with light trapping).

This chapter will outline our initial exploration of the growth of such arrays, exploiting the so-called "Vapor-Liquid-Solid" (VLS) growth mechanism, using SiH$_4$ as the Si precursor. The following chapter will continue to discuss this approach, but with SiCl$_4$ as the precursor.

3.2 The Vapor-Liquid-Solid (VLS) Process

While there are many approaches to the fabrication of micro- and nanowires, [59] of particular interest is the Vapor-Liquid-Solid (VLS) method. [32] [33] This has many desirable features for our purposes: wires formed by this technique tend to grow as single crystals; [60] under the right conditions, VLS-grown wires can inherit their growth orientation from the growth substrate; [61] VLS has been shown to be capable of high growth rates (up to several μm/s); [62] in the VLS approach, growth occurs from gas phase precursors, which in the case of Si can be of very high purity and/or inexpensive relative to alternative sources of Si, as well as allowing in principle for in-situ doping; [63] and the wide range of wire dimensions, and the high degree of control of wire diameter and position, that are possible with this technique. [64] [65]

In this technique, as it applies to Si growth, an impurity metal is used to form a liquid alloy droplet with Si, of relatively low freezing temperature, when Si is introduced from the gas phase via a Si-containing molecule such as SiH$_4$ or SiCl$_4$. The liquid droplet is a preferred

site for deposition from the vapor, which causes the liquid to become supersaturated with Si with continued exposure to the Si precursor molecule. A wire (or "whisker", or "rod") can then grow by precipitation of Si from the droplet. The metal has a high "accommodation coefficient" relative to a smooth solid surface, and is therefore the preferred deposition site, allowing for very selective growth, as well as accelerated growth rates relative to uncatalyzed deposition under the same conditions. [32] [61] Due to a low activation energy for nucleation at the crystal-melt interface, the wires grow by precipitation of Si from the supersaturated Si-metal alloy. [66]

3.3   Catalyst Selection

In searching for a catalyst one must take the following issues into account: (after [61])

1. Si should be highly soluble in the liquid catalyst

2. Wire growth must be thermodynamically favorable [66]

3. The catalyst-Si eutectic temperature should be compatible with the decomposition temperature of the gasesous Si precursor

4. The catalyst should have low solubility in solid Si

5. The catalyst should not form a deep-level trap state within the band-gap of Si

6. The catalyst should be readily available and inexpensive, lest it contribute significantly to the cost of overall PV device

7. The catalyst should not form an oxide, which would impede VLS wire growth

8. The catalyst should have a low vapor pressure at the eutectic temperature, so that catalyst is not lost to the vapor phase

9. The catalyst-Si binary phase diagram should not include solid intermediate phases, which could interfere with VLS growth of Si wires

10. The catalyst should be inert to the chemical reaction products

3.3.1 VLS Thermodynamics

For a metal to catalyze VLS growth, Si must first be soluble in the liquid metal. Wagner and Ellis argued that this then allows the catalyst to act as a preferred deposition site for Si out of the gas phase, due to the large "accommodation coefficient" of the metal droplet. [61] The argument points to the strong and nonlinear dependence of thin film deposition rate on the roughness of the deposition substrate, [67] and that the liquid surface presents an "ideally rough" interface for Si deposition.

Given a Si-metal liquid alloy particle, if it is thermodynamically favorable, solidification of solid Si from the supersaturated melt will occur, leading to one-dimensional Si growth. Nebol'sin and Shchetinin analyzed this situation in terms of the interfacial tensions α_L (liquid-vapor), α_S (solid-vapor), and α_{SL} (solid-liquid), at the point where liquid, solid, and vapor phases meet. [66] They then explore under what conditions it is favorable for solid Si to grow by a unit step with the liquid alloy riding on top of the Si post. They find that having an α_S/α_L ratio of $\lesssim 1.41$, and a relatively high value of α_L ($\gtrsim 0.9$), are necessary conditions for a metal to be a good VLS agent. And although they are not the first to observe that not all metals make good VLS catalysts, they note that "whisker growth with the use of Zn, Al, Ga ($\alpha_L = 0.650$ J/m^2), or In ($\alpha_L = 0.500$ J/m^2) as the solvent yields short, unoriented, tapering crystals, often with globules on their top and other imperfections, which is characteristic of unstable growth". They also state that "if α_L is low compared to α_S, a single (solid-liquid) interface is energetically more favorable than two (solid-vapor and liquid-vapor) interfaces". They observe experimentally that "the use of gold, nickel, platinum, and iron as growth leaders ensures steady-state (one-dimensional, oriented) whisker growth, while the process with the participation of silver, zinc, and aluminum is unstable: the liquid droplet breaks down, and the whisker branches and bends". Some of the practical consequences of their work are summarized in Table 3.1.

Historically, Ag, Au, Cu, Ni, Pd, and Pt have proven to be the most successful VLS catalysts for Si growth, [33] with Au and Pt generally favored because they do not form silicides. Later in this chapter and the next the results of our attempts to grow with various catalysts will be presented.

Table 3.1. Ability of various metals to catalyze VLS growth of Si, on the basis of thermo-dynamic predictions (after [66]).

Metal	Wire Growth Possible?
Al	Poor growth predicted
Au	Yes
Cu	Yes
Ga	Poor growth predicted
In	Poor growth predicted
Ni	Yes
Sn	No
Zn	Poor growth predicted

3.3.2 Temperature Requirements

The reaction chamber must be able to reach or at least get close to the eutectic temperature of the metal-Si binary alloy. Our SiH_4 LPCVD system was limited to temperatures of $\sim$ 600 °C or below[1]. This limited our catalyst selection from the above list to Al, Au, Ga, In, Sn, and potentially Zn (although we have not attempted the VLS growth of Si from Zn catalysts using SiH_4 to date). We subsequently constructed a $SiCl_4$ CVD system, able to reach temperatures of up to 1100 °C, which widened our catalyst search considerably, to include Cu, Fe, Mg, and Ni. This will be the subject of the next chapter.

3.3.3 Effect of Catalyst on Optoelectronic Properties of Si

Au is by far the most commonly used element to seed VLS growth of Si wires. [68] [33] In terms of almost all of the properties listed above, Au is more-or-less the ideal candidate for VLS growth of Si. In particular, the relatively low Si-Au eutectic temperature allows Au to be used for the low-temperature growth of wires using a SiH_4 Si precursor. However, Au

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[1]Note that there was a significant, namely up to 200 °C, and temperature-dependent difference between substrate temperatures, as measured by an instrumented Si wafer (SensArray), and set-point temperatures, as displayed on the Omega temperature display, with the substrate temperature being lower than the set-point temperature in all cases. In this chapter I have used the setpoint temperature and our calibration curves to estimate actual substrate temperatures - whenever a growth temperature is listed it is the estimated substrate temperature, not the setpoint temperature.
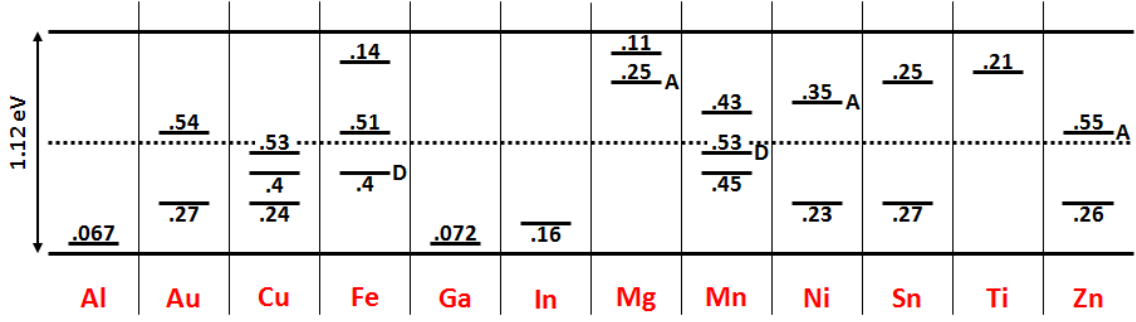
Figure 3.1. Measured ionization energies for various impurities in Si. The levels below the gap centers are measured from the top of the valence band and are acceptor levels unless indicated by D for donor level. The levels above the gap centers are measured from the bottom of the conduction-band level and are donor levels unless indicated by A for acceptor level. The bandgap of Si at 300 K is 1.12 eV (after [12]).

is known to form a deep-level trap state within the band-gap of Si. [12] If one is concerned with making minority-carrier devices, the effect that the VLS catalyst metal has on the optoelectronic properties of the grown semiconductor becomes important, since inevitably the catalyst will be soluble to some degree in the grown wires.

Carrier recombination via an energy level within the bandgap of a semiconductor is governed by Shockley-Read-Hall recombination statistics. [47] The rate of carrier capture by the trap state depends exponentially on the distance between the Fermi level of the material and the energy level of the trap state. Given that both carrier types must be captured in order for a free electron and a free hole to recombine, this means that impurities that form trap states at a given concentration near the middle of a semiconductor's bandgap tend to be exponentially worse in terms of their effect on the lifetime of minority carriers in the material than those that form trap states far from midgap. Fig. 3.1 illustrates this for a selection of metallic impurities in Si.

This does not, however, tell the whole story. Each trap level also has an associated cross-section with respect to each carrier type, and this must be multiplied by the aforementioned exponential energy level dependence in order to determine a rate of recombination associated with a given trap state. This is further complicated by the very different solubilities of different metals in Si, because obviously the concentration of an impurity material has an effect also.

The solubility of Au in bulk Si at a typical SiH_4 VLS growth temperature of 600 °C is $>$ 10^{14} cm^{-3}, and at a typical $SiCl_4$ VLS growth temperature of 1000 °C the solubility limit is almost 10^{16} cm^{-3}. [69] [70] A recent report which combined high-angle annular dark-field (HAADF) scanning transmission electron microscopy (STEM), local electrode atom probe (LEAP) tomographic analysis, and electron-beam-induced current (EBIC) microscopy, on individual Si nanowires grown by VLS from a SiH_4 Si precursor at 450 °C from Au catalysts, suggests that Au atoms may be present at levels of up to $\sim 2 \times 10^{17}$ cm^3, well in excess of the bulk solubility. [71] Another report, from our group, which used a secondary ion mass spectrometry (SIMS) instrument with nanoscale spatial resolution to study the Au concentration in individual Si wires of ~ 1 μm diameter, grown by VLS from a $SiCl_4$ Si precursor at 1000 °C from Au catalysts, found Au to be present inside the wires at a level of $\sim 1.7 \times 10^{16}$ cm^3, which is much closer to the bulk solubility. [72] In either case, Au concentrations this high can seriously degrade the electronic performance of Si. [73] [74]

A detailed empirical study of the effects of various metallic impurities in wafer-based Si PV devices was undertaken by members of the Westinghouse R&D center and others in the 1980s. [73] [75] [76] One key parameter that they identified was a "degradation threshold" in atoms cm^{-3}, which is the concentration below which solar cell performance is virtually unaffected, but above which solar cell performance drops off. A summary of the segregation (or "distribution") coefficients, solubilities, and degradation thresholds for various metallic impurities in Si is shown in Table 3.2.

One might think that it would then be enough to compare an element's solubility with its degradation threshold, and so long as the latter was greater than the former then this would be a good choice for a VLS catalyst. Unfortunately even still it is not that simple. Some metallic impurities, in addition to being soluble in Si, will form silicides, very stable crystallites of given stoichiometry and crystal properties and with the metal atom appearing at much higher concentrations than would be the case for the metal dissolved in the Si lattice. The Westinghouse experiments neglected this, except to say that "the model calculations are in good agreement with experimental values except for Cu, Ni, Fe, and to a lesser degree, carbon, which at high concentrations induce structural defects and precipitation effects and degrade the cells mainly by erratic junction defect mechanisms as opposed to the more usual base diffusion length loss". [75] This will be revisited in the next chapter.

Table 3.2. A summary of the segregation (or "distribution") coefficients (which is the ratio of the concentration of impurity atoms in the growing crystal to that in the melt from which it is growing, in thermodynamic equilibrium), solubilities, and degradation thresholds for various metallic impurities in Si, of potential relevance as Si VLS catalysts. [16] [44] [70] [73] [75] [77]

Metal	Segregation Coefficient	Solubility in Solid Si at 1000°C (cm^{-3})	Degradation Threshold
Al	2×10^{-3}	2×10^{19}	4×10^{15}
Au	3×10^{-5}	1×10^{16}	3×10^{13}
Cu	4×10^{-4}	3×10^{17}	4×10^{17}
Fe	8×10^{-6}	5×10^{15}	3×10^{14}
Ga	8×10^{-3}	3×10^{19}	
In	4×10^{-4}		
Mg	2×10^{-3}		
Mn	1×10^{-5}	2×10^{15}	2×10^{14}
Ni	8×10^{-6}	1×10^{17}	5×10^{15}
Sn	3×10^{-2}	5×10^{19}	
Ti	4×10^{-4}	3×10^{12}	3×10^{12}
Zn	1×10^{-5}	3×10^{15}	

3.3.4 Additional Effects of Catalysts Highly Soluble in Solid Si

Al, Ga, In, and Sn have all been explored as low-eutectic-temperature alternatives to Au for the VLS growth of Si wires, as will be detailed later in this chapter. All of these are predicted to have relatively benign effects on the properties of the grown Si. A major disadvantage of these catalysts (in addition to their inferior ability to catalyze growth, relative to Au) is their relatively high solubilities in solid Si (see Table 3.2). Up to a certain level this is not a problem, since a doped Si wire is ultimately desired and Al, Ga, and In form relatively shallow acceptor states near the valence band in Si. [12] However, as shall be demonstrated below for the case of Ga, if the solubility becomes too high the catalyst can actually shrink during wire growth, as more and more of the catalyst material is absorbed into the growing wire, leading to conical rather than wire-like structures. This limits the aspect ratio that is
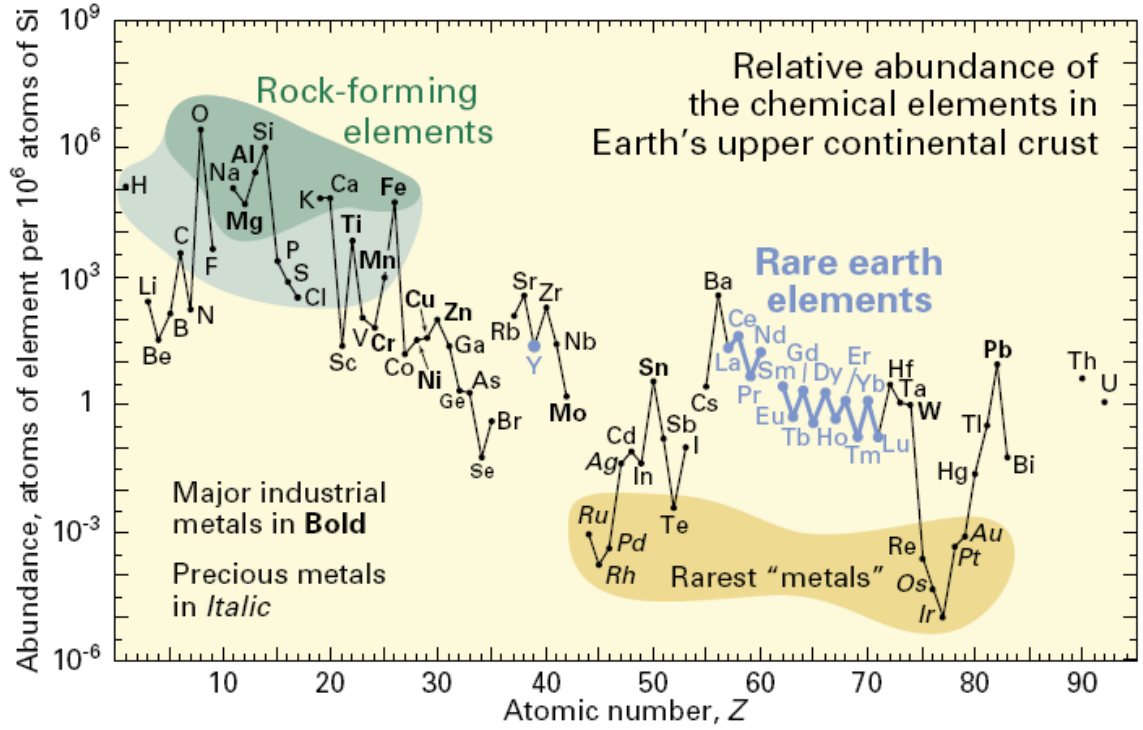
Figure 3.2. Abundance (atom fraction) of the chemical elements in Earth's upper continental crust as a function of atomic number. Many of the elements are classified into (partially overlapping) categories: (1) rock-forming elements (major elements in green field and minor elements in light green field); (2) rare earth elements (lanthanides, La-Lu, and Y; labeled in blue); (3) major industrial metals (global production $\gtrsim 3 \times 10^7$ kg/year; labeled in bold); (4) precious metals (italic); and (5) the nine rarest "metals" - the six platinum group elements plus Au, Re, and Te (a metalloid). (Taken, with permission, from [11]).

achievable, and also is likely indicative of a degenerate level of doping.

3.3.5 Cost and Availability of Catalyst

Another respect in which Au is not an optimal choice for VLS growth of wires for PV applications is in terms of its relative scarcity and expense. In fact, as shown in Fig. 3.2, Au is one of the rarest elements on Earth. This provides another motivation for searching for alternative catalysts. In particular, Al, Cu, Fe, Mg, Mn, Ni, Sn, and Zn are all Earth-abundant elements that are used on a large scale industrially.

3.3.6 Oxidation

Of the potential VLS catalyst choices shown in Fig. 3.1, the suitability of Al and Mg is reduced by the fact that both of these elements form extremely stable oxides. [78] This means that considerable care must be taken to have the Si precursor interact with the metal, rather than with the stable oxide that forms on the surface of the catalyst. [79] To date, this has meant that Al has been successfully demonstrated as a VLS catalyst only when deposited in-situ and the subsequent Si deposition done in UHV conditions, so that the Al is prevented from oxidizing. [80] Even in this study, however, the grown wires often were very tapered, and only lengths of less than 1 μm were demonstrated. Also, the relatively low growth rates, and low growth temperatures (down to ∼ 150 °C below the Al-Si eutectic temperature), suggests that possibly a vapor-solid-solid (VSS), rather than a VLS, process explains the results described there. To our knowledge, there are no reports of the successful use of Mg as a VLS catalyst.

3.4 Results from VLS Growth with SiH$_4$

Taking all of the above considerations into account, Al, Au, Ga, In, and Sn were explored as VLS catalysts with a SiH$_4$ precursor. As noted above, our catalyst search was limited in this case by the inability to reach temperatures higher than ∼ 600 °C in our SiH$_4$ LPCVD system.

A thermal Low Pressure Chemical Vapor Deposition (LPCVD) system was used, with silane (SiH$_4$) as the vapor-phase reactant, and, in some experiments, hydrogen (H$_2$) as a carrier gas. Metal seed particles were created either lithographically using a lift-off process, or simply by thermal evaporation of a thin (5 nm) layer of metal that dewetted from the substrate during deposition to form an array of nanoparticles.

As expected, Au was the best VLS catalyst of the group Al, Au, Ga, In, and Sn. Growth such as depicted in Fig. 3.3 could be achieved with little trouble.

Sn is apparently not thermodynamically favorable as a VLS catalyst for Si, [66] and we saw no wire growth with this catalyst (not shown).

Preliminary experiments with Al catalysts typically yielded thin shells at the edges of the seed particles rather than wires (see Fig. 3.4). Also, the growth rate was much slower than typically seen in the VLS process. This is potentially attributable to the aluminum
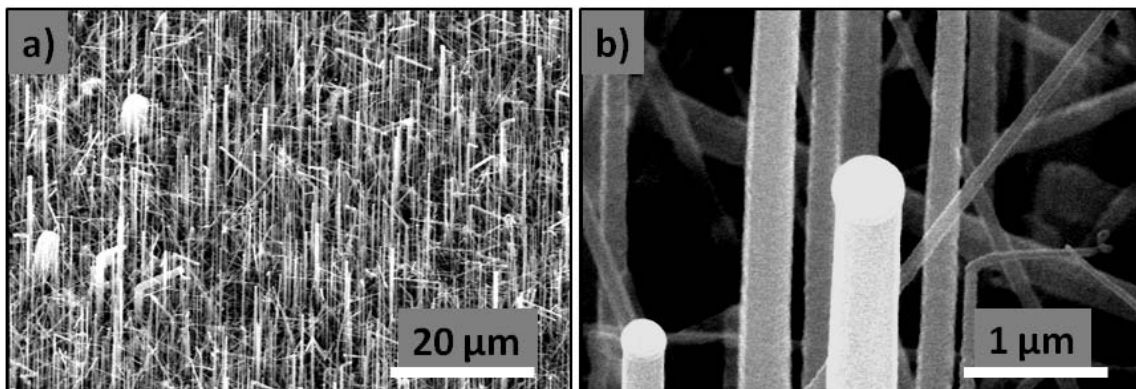
Figure 3.3. Typical example of Si wires grown from Au catalyst with SiH$_4$ precursor. In this case the growth occurred at a total pressure P = 1 Torr, flow rate of 100 sccm, using 5% SiH$_4$ in Ar (i.e., SiH$_4$ partial pressure of 50 mTorr), and temperature T $\approx$ 500 °C, for 180 mins. The catalyst was a 5 nm thick evaporated Au film, on a Si(111) substrate. Fig. (b) is a more detailed image of the same sample as shown in (a).

oxide that forms very rapidly on the Al surface and acts as a barrier to VLS growth. [79] Evaporation of a thick layer of In on top of the evaporated Al, without breaking vacuum, in an attempt to prevent the Al from oxidizing, did not produce better results (not shown). For these reasons Al was soon abandoned.

As noted above, Ga is extremely soluble in Si and wires grown with this catalyst were found to be extremely conical, presumably due to the catalyst particle dissolving as the wires grew (Fig. 3.5).

Of the catalysts tried with SiH$_4$, aside from Au we have achieved suitable wire morphologies only with In. Representative images of our fabrication results from In catalysts are shown in Fig. 3.6. The wire density as well as the range of wire diameters ($\sim$ 100 nm to > 1 µm) and lengths of many tens of µm to over 100 µm were in the size range desired for wire array solar cell applications - positive signs for the use of In as a catalyst for this application. However, as indicated in the figure, the uniformity of growth across a wafer from unpatterned In was extremely poor, with the In appearing to migrate on the Si(111) surface prior to initiation of wire growth. This typically results in clusters of dense wire growth with large areas of no wire growth in between.

We explored variations in pressure P, temperature T, SiH$_4$ flow rate, and catalyst thickness (deposited by thermal evaporation) in order to optimize growth conditions with
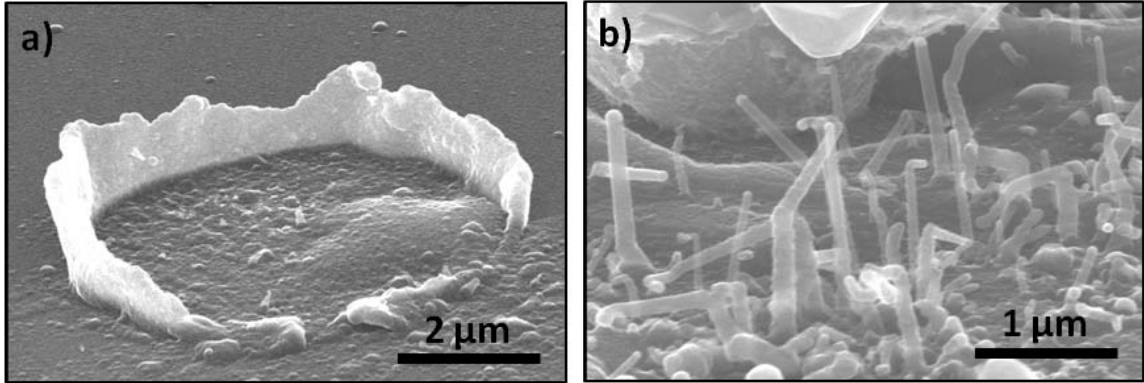
Figure 3.4. Example of Si wires grown from Al seed particles using a pure SiH$_4$ precursor. Growth was conducted at a temperature $T \approx 600$ °C, at pressure $P = 100$ mTorr, and (undiluted) SiH$_4$ flow of 40 sccm, for 60 mins. The catalyst was a 5 nm thick Al film, photolithographically defined to discs of various diameters. Shown are two typical growth morphologies, (a) mostly growth occurred in shells at the very edges of the Al discs, (b) in the few places where wire growth was observed, it was very patchy and the wires tended to be very short and kinked.
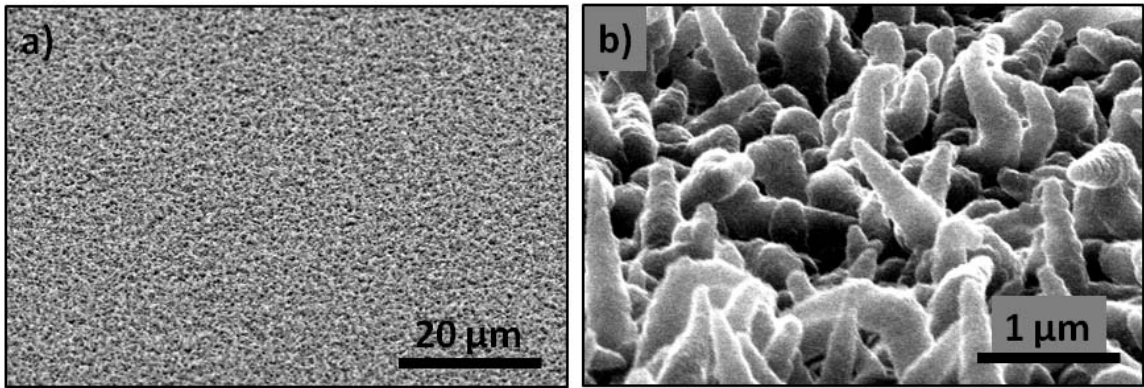
Figure 3.5. Typical example of Si wires grown from Ga catalyst with SiH$_4$ precursor. In this case the growth occurred at a total pressure of P $= 30$ Torr, at a flow rate ≈ 300 sccm with 5% SiH$_4$ in Ar (i.e. SiH$_4$ partial pressure of 1.5 Torr) and temperature T ≈ 500 °C, for 180 mins. The catalyst was a 5 nm thick evaporated Ga film, on a Si(111) substrate. Fig. (b) is a more detailed image of the same sample as shown in (a).
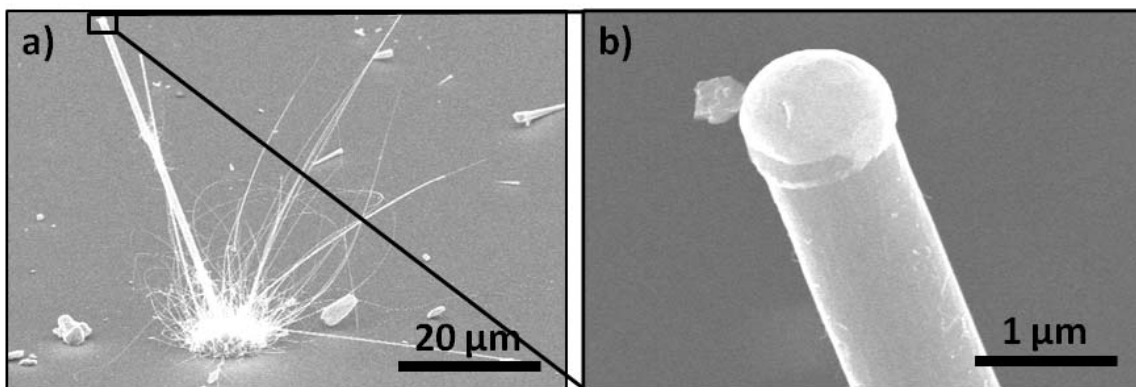
Figure 3.6. Typical example of Si wires grown from In catalyst with SiH$_4$ precursor. In this case the growth occurred at pressure P = 1 Torr, with a pure SiH$_4$ flow rate of 20 sccm, H$_2$ flow rate of 20 sccm, and temperature T = 500 °C, for 60 mins. The catalyst was a 5 nm thick evaporated In film, on a Si(111) substrate. Fig. (b) is a more detailed image of the same sample as shown in (a).

both Au and In as catalyst, using 5% SiH$_4$ in Ar as the growth precursor.

For the Au catalyst, wire morphology improved with increasing substrate temperature and decreasing SiH$_4$ partial pressure in the range T = 300 - 600 °C and SiH$_4$ partial pressure P = 0.05 - 1 Torr (in agreement with [39]). Best results were achieved with substrate temperatures of 600 °C and SiH$_4$ partial pressure of 0.05 Torr. Flow rate was varied between 40 and 200 sccm but this had relatively little effect on wire morphology. The thickness of the evaporated Au film also had relatively little effect.

Optimal growth was found to occur at lower T and higher P for In than for Au. For In, if we exceeded substrate temperatures of $\sim$ 500 °C we saw non-selective growth forming a very rough film, rather than wire growth. We attribute this to surface diffusion of the In particles upon the Si surface, as well as the high vapor pressure of In relative to Au, [81] [82] leading to substantial loss of In at high temperatures. When we grew at partial pressures significantly below 1 Torr we saw the growth rate drop and we saw negligible growth after three hours at partial pressures of 0.1 Torr and less. Best results were achieved with substrate temperatures of 500 °C and SiH$_4$ partial pressure of 1 Torr.

A phase diagram for In-catalyzed VLS growth of Si wires under these conditions is presented in Fig. 3.7. As already noted, the uniformity of growth across a wafer from unpatterned In was extremely poor. Despite this, the images show the most typical mor-
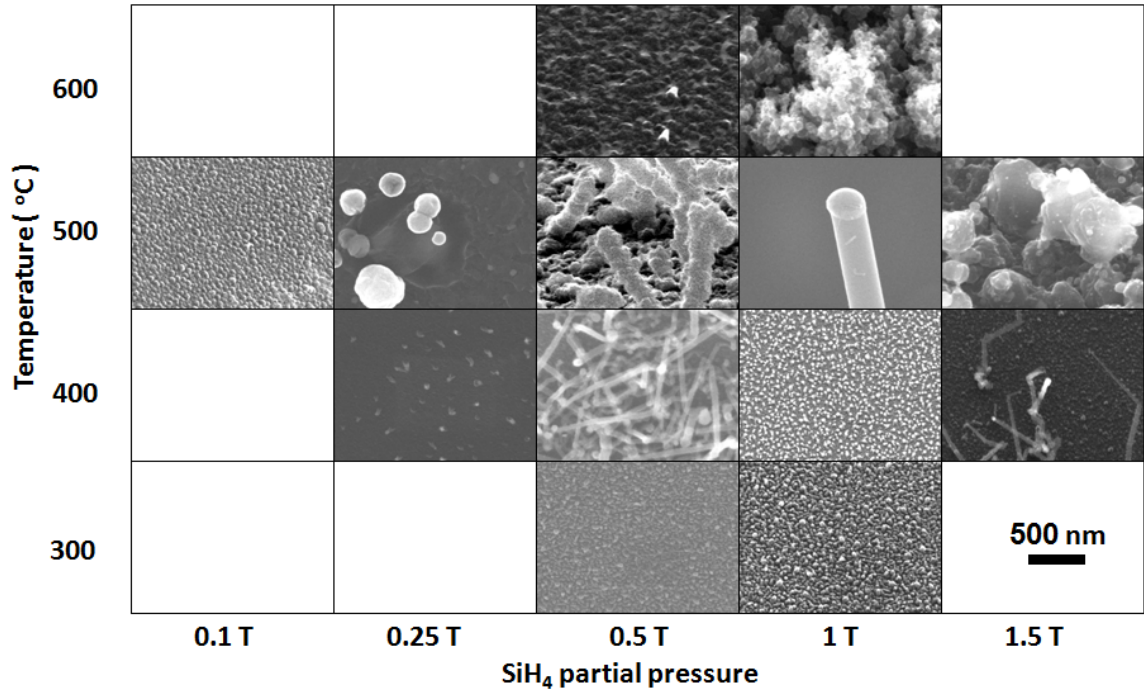
Figure 3.7. Partial phase diagram of growth of Si nanowires from In catalyst particles as a function of pressure and temperature. In all cases the growth was achieved with SiH_4 diluted to 5% concentration in Ar, with a flow rate of 100 sccm, for three hours. In most cases, catalyst particles were formed by the dewetting of a nominally 5 nm thick evaporated film of In, but the results of growth were found to be fairly relatively insensitive to catalyst layer thickness.

phology.

3.4.1 TEM of SiH_4-grown Wires

We have also performed transmission electron microscopy (TEM) on Au-catalyzed, SiH_4-grown wires. Firstly samples were grown by taking a p-Si(111) wafer (International Wafer Service), cleaning in RCA 1 solution (5:1:1 H_2O:H_2O_2:NH_4OH at 70 °C) [83] for 10 mins, etching in buffered HF (Transene), followed by thermal evaporation of 5 nm of Au. Growth was then performed in our LPCVD chamber, at 550 °C and a total pressure of 1 Torr, with a 100 sccm flow rate of 5% SiH_4 diluted in Ar, for 6 hours. A fragment of the grown sample was then sonicated in 100 µL of IPA for 1 min, and 7 µL of the resulting suspension was dropcast on a lacey carbon grid (SPI Supplies). TEM was then performed by Dr. Carol Garland using a Tecnai F30 transmission electron microscope.

We observed the expected VLS catalyst droplet at the tip of the wire, and smooth-walled wire with near-circular cross-section from the tip for several µm towards the base. However, beyond that we see the cross-section become hexagonal, and sawtooth "sub-facets" become increasingly prominent (Fig. 3.8). Also, there is a large amount of Au on the wire surfaces, as seen in Fig. 3.9. The wire cores do appear to be, however, single crystalline (Fig. 3.10).

3.5 Single Wire Electrical Measurements

Electrical measurements were performed on individual Au-catalyzed Si nanowires. Wires were removed from their growth substrate by sonicating the as-grown samples for 5 - 20 s in 5 - 50 µL of isopropanol (IPA) and drop-casting the resulting suspension in 5 µL increments on n+, ~ 0.01 Ω cm Si(100) wafers coated with 100 nm LPCVD silicon nitride (Si_3N_4) (International Wafer Service), spinning the wafer at ~ 300 RPM for 1 min between each dropcast in order that the isopropanol would evaporate and the wires be spread out on the surface. The nitride-coated wafers were then spin-coated with a double layer of PMMA, by applying 495K MW 4% PMMA in chlorobenzene (Microchem), spinning at 3000 RPM for 1 min, baking at 170 °C for 1 min on a hotplate, and then repeating with 950K MW 2% PMMA in chlorobenzene (Microchem). Contacts were then patterned in the PMMA by first locating a suitable wire (the wires were barely visible in the SEM through the PMMA), and then patterning a four-point probe assembly on top. Patterns were then developed by immersing the samples in 1:1 methyl isobutyl ketone (MIBK):IPA (Microchem) for 30 s, then 1:3 MIBK:IPA for 30 s, and then in just IPA for 1 min, and finally rinsing in H_2O and drying with N_2. 5 nm of Cr and 1 µm of Ag were evaporated and then lift-off was performed by soaking the samples in acetone. The Si wires being contacted were usually large enough in diameter that such a thick layer of Ag was required to prevent the Si wires from tearing through the metal contacts upon liftoff of the PMMA. We then wired-bonded these samples to 16-pin packages (Fig. 3.11) and performed two- and four-point I-V measurements (Fig. 3.12) as well as gate-bias-dependent two-point I-V measurements on the Si wires (not shown).

Wires characterized to date, grown from Au catalysts and 5% SiH_4 in Ar doped with 5 ppm phosphine, show resistivities of approximately 10^{-1} Ω cm, indicating a dopant density of approximately 10^{17} cm^{-3}, assuming n-type doping and bulk Si mobilities, giving rise
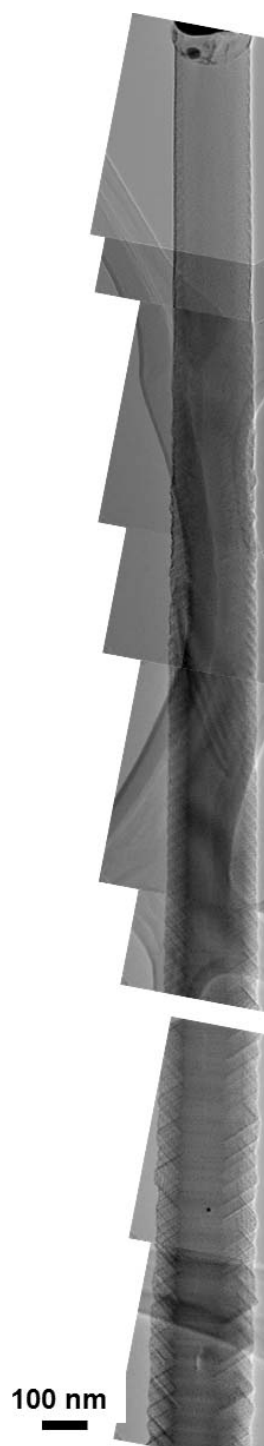
Figure 3.8. Composite TEM image of SiH$_4$ grown. The wire appears smooth-walled wire and with near-circular cross-section from the tip for several μm towards the base. However, beyond that the cross-section becomes hexagonal, and sawtooth "sub-facets" become increasingly prominent.
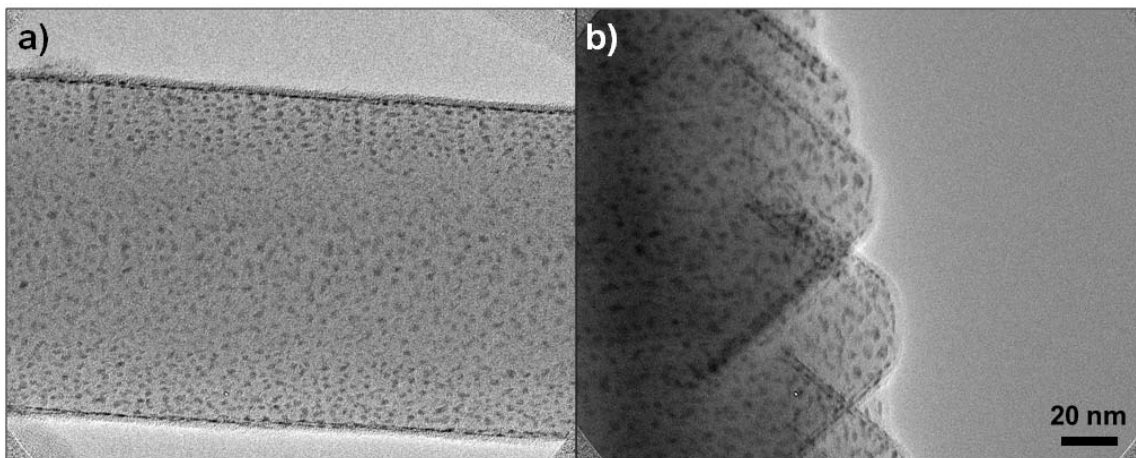
Figure 3.9. TEM images showing presence of Au on SiH$_4$-grown Si wire surface. Au is present in regions where the wire is (a) smooth, as well as (b) rough (i.e., with sawtooth "sub-faceting"). 20 nm scale bar applies to both images.

to the standard relationship between resistivity and dopant density for bulk silicon [50] (Fig. 3.12). Backgated I-V measurements (not shown) show no appreciable change in the conductivity of these nanowires for gate biases up to 50 V, which is somewhat surprising, and perhaps implies that the wires are in fact degenerately doped (which could be the case if, for example, bulk Si mobilities do not apply to these wires), or that the high concentration of Au at the surface, as observed by TEM, is shorting the device.

3.6 Patterned Growth

In order to fabricate the device pictured schematically in Fig. 1.4, control of wire density and orientation must be significantly improved relative to what was presented in Ch. 3.4. If precise control of wire position via a template-less growth mechanism proves challenging, this may be accomplished through the use of porous alumina to template VLS growth of a wire array. [49] [84] [85] [86] To do this, a porous alumina layer of the desired thickness could first be grown on top of silicon, then seed particles deposited within the pores, and then Si wires grown in the pores by the VLS process.

There are many reasons to favor a template-free approach to wire growth, among them being the additional processing steps that will be required if a physical template is used, the difficulty in achieving truly independent control of wire diameter and pitch over a large
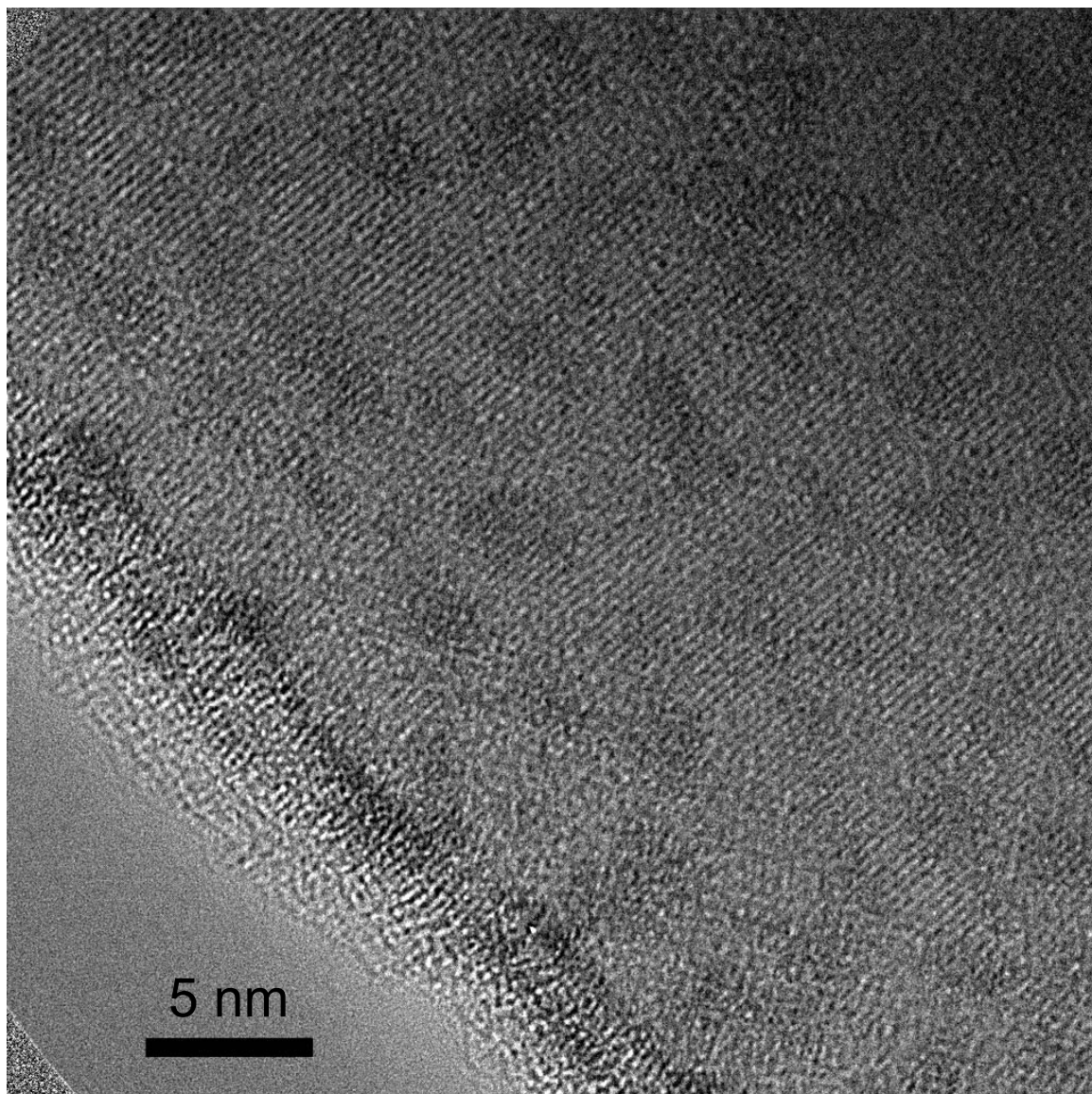
Figure 3.10. High resolution TEM image of Au-catalyzed, SiH$_4$-grown Si wire. Clearly visible are the lattice fringes indicating single-crystalline growth, as well as Au at the surface, which makes the wire appear mottled.
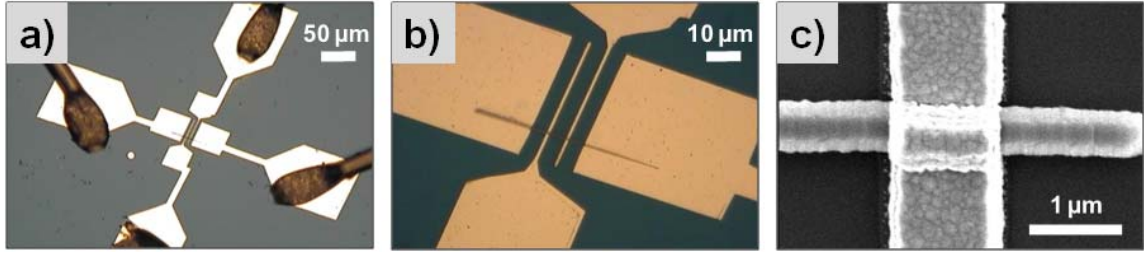
Figure 3.11. Illustration of electrical contacts to single Si wires. Fig. (a) is an optical micrograph showing the wire bonds to the contact pads. Fig. (b) is a close-up of the same device, showing the four-point electrical contacts to a Si wire. Fig. (c) is an SEM image of a single contact, showing that often the wire (which runs horizontally in the image) was found to be of large enough dimension to significantly distort or even break the deposited metal contact (which runs vertically).
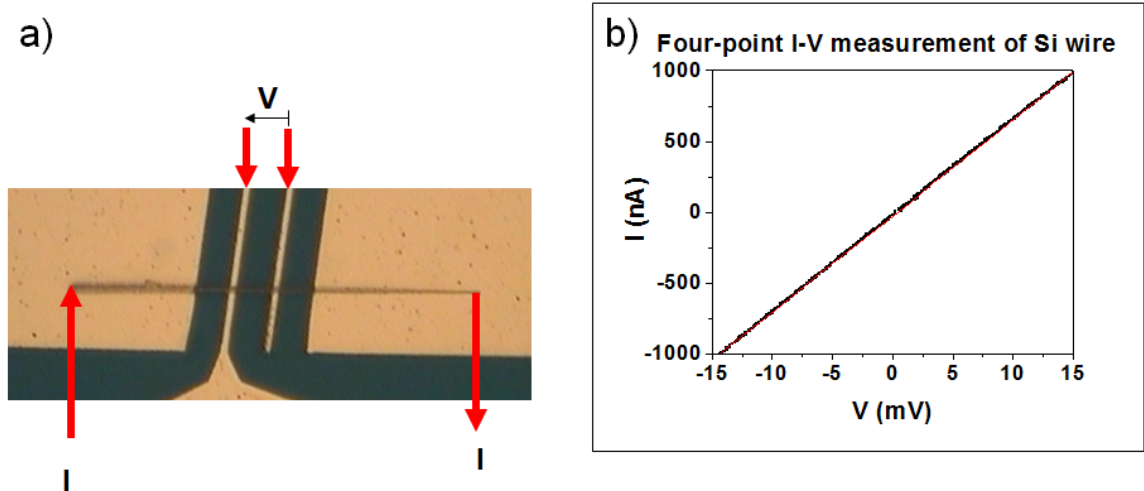
Figure 3.12. Illustration of a four-point probe measurement of a single Si wire. Fig. (a) shows schematically how the four-point measurement is performed, by sourcing a known current I between the external contacts and then measuring the potential drop V across the internal contacts. This allows one to make a measurement free from the effects of contact resistance. Fig. (b) shows the result of such a measurement on a phosphine-doped, SiH_4-grown Si wire, indicating a resistivity of approximately 10^{-1} Ω cm, indicating a dopant density of approximately 10^{17} cm^{-3}, assuming n-type doping and bulk Si mobilities.

range of values for many templates, [87] the potential for the template to interfere with the ability to grow single-crystalline material, [88] and the possible doping of the wires by the template. [89]

Therefore, we have explored the use of patterning, rather than physical templates such as porous alumina, to define wire growth. Specifically, we have used electron-beam lithography to control the catalyst particle size, spacing, and location. We took p+ Si(111) wafers, of ~ 0.01 Ω cm resistivity, and annealed in oxygen at 900 °C for 12 mins, after a 10 min RCA1 clean (1:1:5 H_2O_2:NH_4OH:H_2O at 80 °C) [83] and a 20 min etch in buffered HF (Transene). This formed a layer of SiO_2 approximately 10 nm thick, measured by spectral ellipsometry. The wafers were then spin-coated with a double layer of PMMA, and an electron beam (Hitachi S-4100 FESEM) was used to pattern various 100 μm × 100 μm arrays of circles, with diameter ranging from 100 nm to 5 μm, and pitch of either 1 or 10 μm. After developing the patterns with MIBK and isopropanol (IPA), the oxide was etched in the places from which the PMMA had been removed, by immersion in BHF. Then 10 nm of catalyst (either Au or In) was evaporated and acetone used to lift-off the remaining PMMA and unwanted catalyst, leaving an array of catalyst particles embedded in holes in the oxide. This was then placed in the CVD reactor and VLS growth was performed under various conditions. As in the case of unpatterned growth, optimal conditions were found to be different for the Au and In catalysts, but for each metal were similar for patterned and unpatterned growth. Results of this process are displayed for Au and In in Figs. 3.13 and 3.14, respectively.

These result were very encouraging, particularly in that they demonstrate the ability of a surface oxide to control catalyst position and prevent surface diffusion. This inspired the processing approach to be described in Ch. 4. On the other hand, in the case of In the growth rates observed were very low, apparently much lower than in the case of unpatterned growth, although the reason for this is unclear. Also, many wires tended to grow from each opening in the oxide, especially in the case of growth at 1 torr of SiH_4 partial pressure. Furthermore, a large fraction of wires did not grow normal to the growth substrate.

Morphology in the case of the Au catalyst was much better, with far higher growth rates observed, typically one wire growing per hole, and with a large fraction of the wires growing normal to the growth substrate. On the other hand, as shown in Fig. 3.13, the array fidelity is still far from perfect. Also, the wires grown to date have all had very small diameters, $\approx$
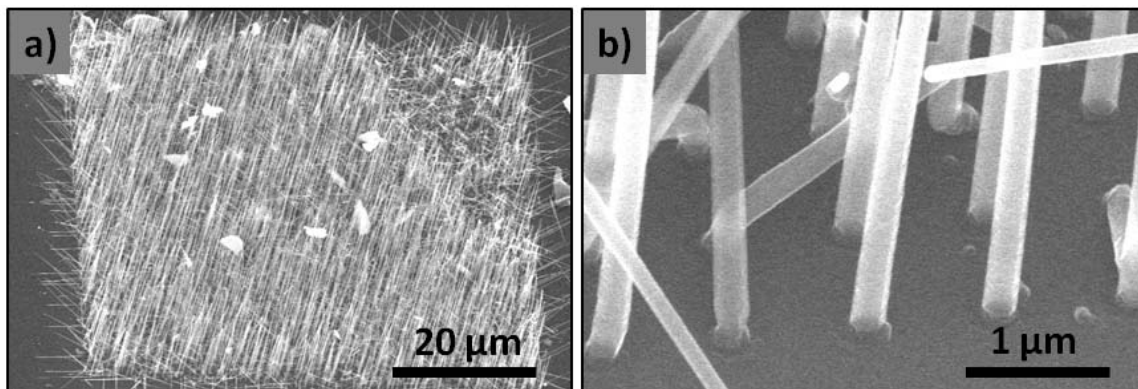
Figure 3.13. Si wires grown from Au catalyst, and patterned by electron beam lithography, at a total pressure P = 1 Torr, gas flow rate of 100 sccm, using 5% SiH_4 in Ar (i.e., SiH_4 partial pressure of 50 mTorr), and temperature T = 600 °C, for 180 mins. Fig. (b) is a more detailed image of the same sample as shown in (a).

100 - 200 nm, and attempts to grow larger, $\sim$ 1 μm-diameter wires by this approach have to date been unsuccessful (not shown). Furthermore, electron beam lithography is a rather time-consuming and expensive process, which is especially problematic if one is considering making large area (of many cm^2 areas, and larger) devices.

3.7   Axial Heterostructures

As noted in Ch. 2.6, axial pn homo- or heterojunctions may also be of interest for novel PV devices. Such structures have been demonstrated in a variety of materials systems. [36] [37] [38] This brief section is therefore just a demonstration that such structures are in principle achievable with our LPCVD setup also.

Preliminary work was undertaken into the growth of Ge on Si axial heterostructure nanowires (Fig. 3.15). In this case, growth was performed by cleaning a Si(111) wafer for 10 mins in an RCA1 etch, 20 mins in buffered HF, followed by thermal evaporation of 5nm Au. The sample was then introduced to the LPCVD chamber at $\sim$ 550 °C and $\sim$ 10^{-6} Torr base pressure. 5% SiH_4 in Ar was then introduced at a flow rate of 100 sccm to bring the chamber pressure up to 1 Torr, and Si deposition was continued for 90 mins. SiH_4 flow was then halted, and the temperature dropped to $\sim$ 300 °C. At the same time, 5% GeH_4 in Ar was then introduced at a flow rate of 100 sccm to bring the chamber pressure up to 1 Torr, and Ge deposition was continued for 90 mins.
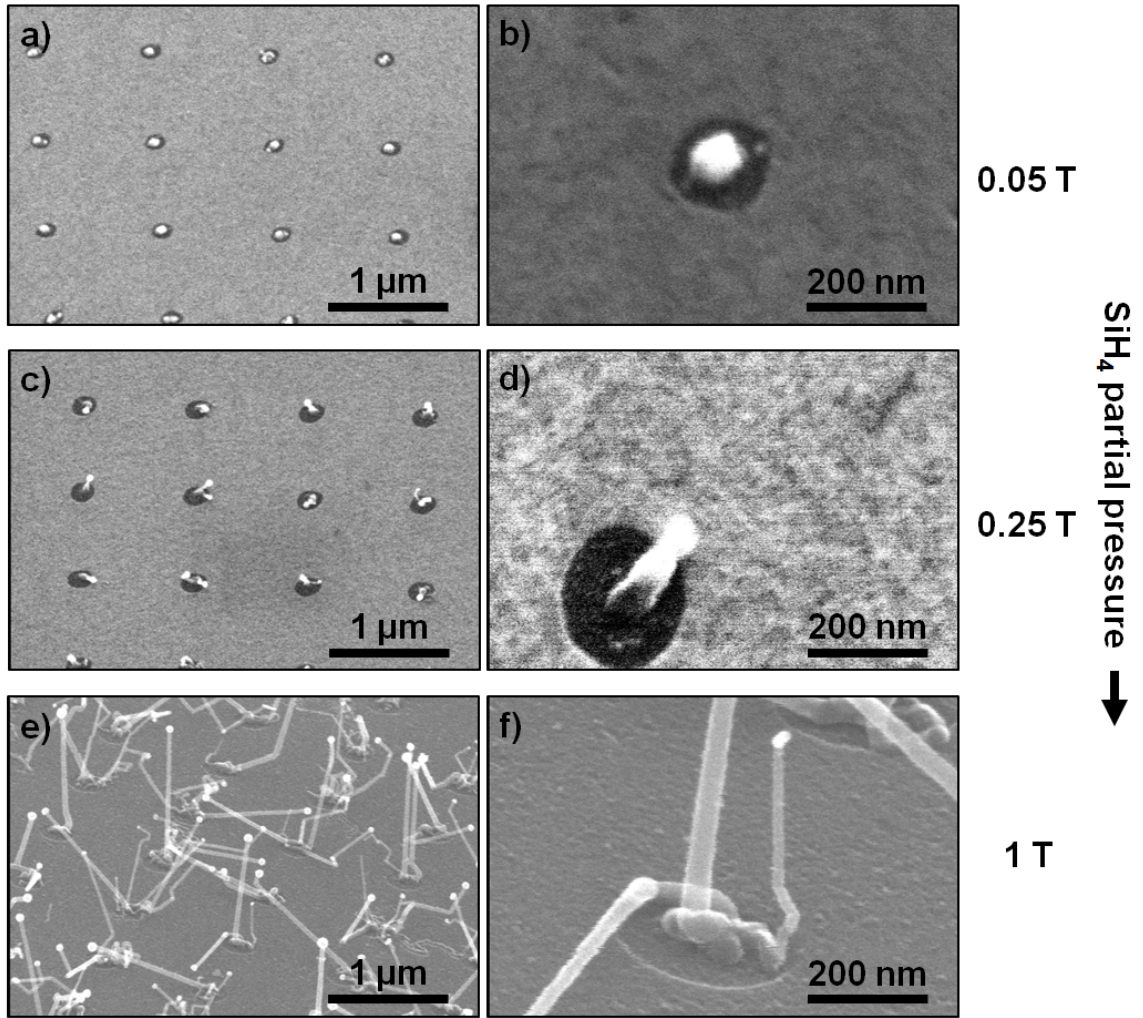
Figure 3.14. Si wires grown from In catalyst, and patterned by electron beam lithography, at various pressures, gas flow rate of 100 sccm, using 5% SiH_4 in Ar (i.e., total pressure = $20 \times SiH_4$ partial pressure), and temperature T = 500 °C, for 180 mins. Partial pressures were (a), (b) 0.05 T, (c), (d) 0.25 T, and (e), (f) 1 T. Figs. in the right column are more detailed images of the same samples as shown in the left column.
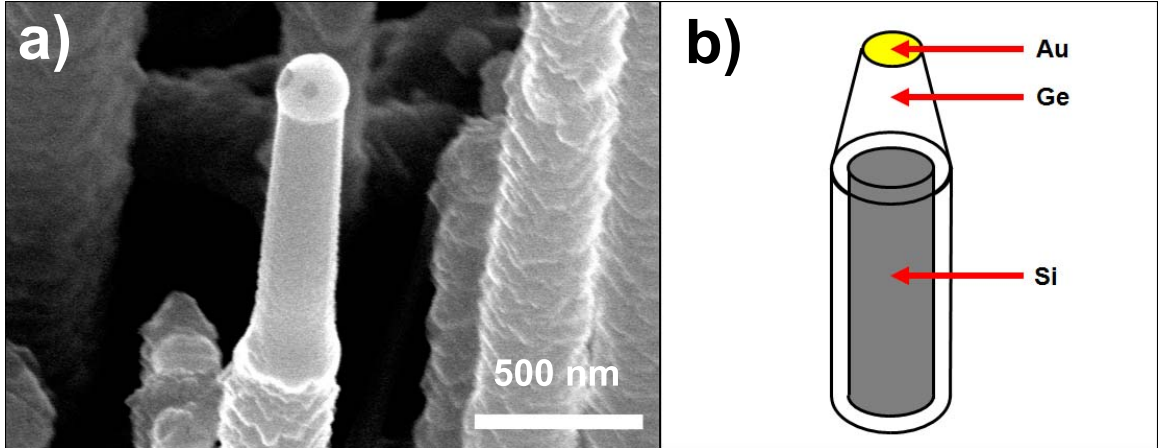
Figure 3.15. Example of preliminary work in growing Ge on Si heterostructures. Fig. (a) shows an SEM image of a Ge on Si structure, grown as described in Ch. 3.7. Fig. (b) illustrates the predicted composition of the structure, as suggested by Energy Dispersive X-Ray Spectroscopy (EDX/EDS).

Energy Dispersive X-Ray Spectroscopy (EDX/EDS) analysis suggests that the structure consists of axial Ge-on-Si growth, as well as a conformal shell of Ge around the Si wire core, as indicated in Fig. 3.15(b). VLS growth of Ge from GeH_4 conducted at lower temperatures than for Si from SiH_4 has been reported. [90] A two-step temperature profile, with an initial, higher temperature nucleation step, followed by a reduced temperature growth step, has also been reported, leading to reduced tapering in the Ge wires. [91] Our conditions were intended to simulate this effect, given the significant amount of time it took for the system to drop from 550 °C to 300 °C. However, the temperature profile was not very well controlled, and this is something that might be explored if there is a future need to increase or reduce deposition of Ge on the sidewalls of the Si wire core.

In addition to Si/Ge heterostructures, Si_xGe_{1-x} alloy wire structures may also be of interest, [92] in order to tune the bandgap of the absorber to more optimally match the solar spectrum in multijunction structures, [93] or for exploiting strain effects or for better crystalline lattice matching. [94] But these are left as the subject of future investigations.

3.8 Conclusion

Wire arrays are of interest in photovoltaic applications because of the potential for increased carrier collection in low diffusion length materials, the potential for rapid deposition of

single-crystalline material from low-cost precursors, and the potential for fabricating novel heterojunctions between non-lattice-matched materials. For a wholly inorganic, pn junction photovoltaic device design in Si, wires with diameters of at least a few hundred nm are required, so that the wires are able to sustain depletion regions. In addition, wire lengths of many tens of μms are desired so that the wires can absorb most of the incident above-bandgap photons. Such wires have been fabricated by the VLS method with both Au and In as a growth catalyst. In has the advantage of not forming a deep-level trap state within the bandgap of Si. However, without templating we have been unable to grow dense arrays of wires with In. Electron beam lithography is one example of an approach to formation of well-controlled dense array, and has been successfully demonstrated with both Au and In catalysts. We have identified optimal growth conditions for both catalysts. Wires made from Au catalysts and phosphine doped silane displayed metal-like conductivity properties when electrical measurements on single wires were performed. Finally, preliminary work demonstrating the potential for Ge-on-Si heterostructure wires has been performed.

Chapter 4

Growth of Si Wire Arrays from SiCl$_4$

4.1 Introduction

The successful production of large-area Si wire arrays involved the use of a SiCl$_4$ precursor gas, and a lithographically patterned oxide buffer layer to confine the VLS catalyst to the desired areas in the pattern. This approach produced nearly defect-free arrays that exhibited an extremely narrow diameter and length distribution, and highly controlled wire position. [95]

Inspired by Hochbaum et al.'s demonstration of the ability of a SiCl$_4$ precursor in the presence of H$_2$ to form in-situ HCl, that can etch any oxide layer than may be present on the Si growth substrate, allowing for epitaxial growth of Si wires normal to their [111] growth substrate, [40] we built a SiCl$_4$ tube furnace reactor capable of reaching temperatures up to 1100 °C[1]. For our present purposes, SiCl$_4$ has two key advantages to SiH$_4$ as a growth precursor. Firstly, the in-situ etching mechanism, as already mentioned, allows for much superior epitaxy between grown wires and the growth substrate, as the HCl etches through any native oxide that may be present on the growth substrate. Secondly, SiCl$_4$ is a significantly more stable molecule than SiH$_4$, and so requires higher temperatures to decompose. This allows us to perform growth at higher temperatures without excessive conformal (i.e., non-catalyzed) deposition of Si. This in turn allows us to use a wider range of catalysts, whose binary eutectic temperatures with Si are higher than of those considered in the previous chapter. Another benefit, that was alluded to in the first chapter, which may prove important looking ahead, is that SiCl$_4$ is currently a waste product of wafer-based

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[1]Note that there was a $\sim$ 50 °C difference between the temperature inside the tube, as measured by a thermocouple probe at atmospheric pressure under a N$_2$ ambient, and the set-point temperature, as displayed on the Omega temperature display, with the temperature inside the tube being lower than the set-point temperature. This was never quantified precisely, so in this chapter, whenever a growth temperature is listed it is the setpoint temperature.

Si production. It is therefore, at least for now and to our knowledge, plentiful and cheap relative to virtually any other source of Si.

4.2 SiCl$_4$ and Catalyst Choice

The higher growth temperatures required for the decomposition of SiCl$_4$ widens the pool for potential VLS catalyst candidates (see Ch. 3.3). While we were limited, primarily by our inability to reach high temperatures, to studying Al, Au, Ga, In, and Sn with our SiH$_4$ LPCVD, the ability to reach 1100 °C allowed us in principle to explore other metals mentioned in the previous chapter, such as Cu, Fe, Mg, Mn, Ni, and Ti.

To date, in our SiCl$_4$ atmospheric pressure chemical vapor deposition (APCVD) system we have experimented with the use of Al, Au, Cu, In, Mg, Ni, and Zn. Of these, Au, Cu, and Ni have been found to produce good results.

Fe has been demonstrated as a growth catalyst for Si wires, both for VLS, [96] and for solid-liquid-solid (SLS) growth, [97] but to our knowledge to date the morphologies achieved have not been particularly impressive. We have not attempted the VLS growth of Si from Fe catalysts using SiCl$_4$ to date.

Ti has also been explored, with considerable success, by Kamins and others. [98] [99] [100] [101] Again however, to our knowledge, and to date, the morphologies, and control of wire diameter, demonstrated have been far less impressive than with the more commonly used Au.

As listed in Table 3.2, this leaves Mn as an outstanding possibility that is potentially of interest (Co, omitted from Table 3.2, is another possibility), although the dearth of Si VLS literature with either Mn or Co may imply that these are not suitable catalysts, given the huge amount of work done in this area in the 1960s and 1970s.

4.3 Unpatterned VLS Growth

4.3.1 Catalyst Selection

Preliminary experiments were conducted by buffered HF (Transene, Inc.) etching of Si(111) wafers, followed by thermal evaporation of a metal, and subsequent introduction of the sample to the SiCl$_4$ APCVD system. Initial experiments explored a variety of growth pressures,
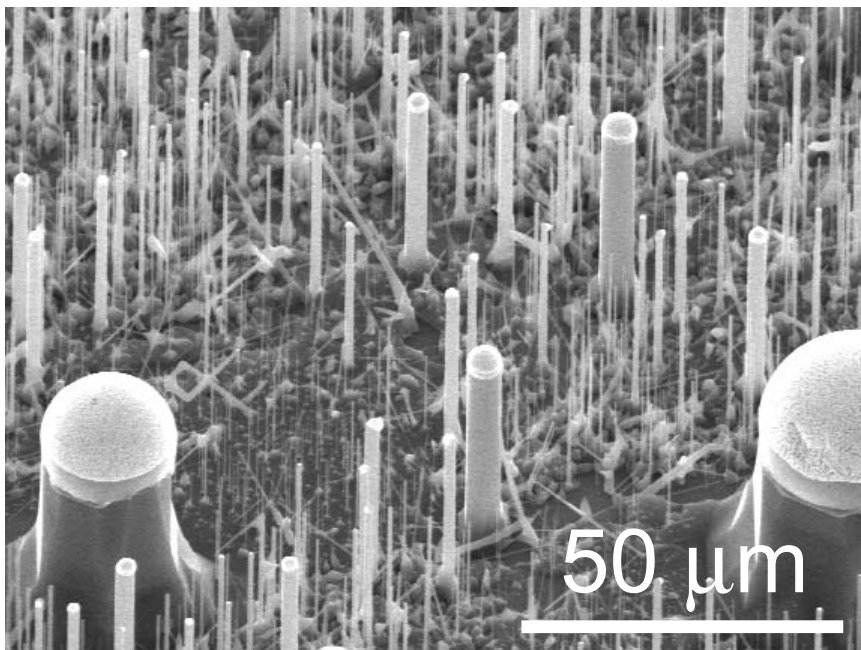
Figure 4.1. Representative SEM image of Au-catalyzed Si wire growth from $SiCl_4$ precursor and thermally evaporated film of Au. In this particular case, the sample consisted of a thermally evaporated, 100-nm-thick Au film on a Si(111) wafer. Growth was performed at 1050 °C and atmospheric pressure, by first annealing for 20 mins under H_2 at a flow rate of 1000 sccm, followed by wire growth under H_2 and $SiCl_4$, at flow rates of 1000 and 20 sccm, respectively, also for 20 mins.

using an MKS 640A pressure control system. However, growth at sub-atmospheric pressures was not successful (not shown), and subsequently the 640A was removed and all growth was conducted at atmospheric pressure. Typically growth was attempted at 1000 °C, by first annealing for 20 mins under H_2 at a flow rate of 1000 sccm, followed by wire growth under H_2 and $SiCl_4$, at flow rates of 1000 and 20 sccm, respectively, for varying lengths of time.

Initial growth attempts from evaporated Au films were successful, but led to poor uniformity in wire diameter (Fig. 4.1). Wires grew normal to the growth substrate so long as the temperature was high enough (see also Ch. 4.5). By correctly choosing the growth temperature, $SiCl_4$ flow rate, and Au film thickness, a much higher degree of uniformity on the wire diameter was observed (Fig. 4.2 (a)).

Growth from evaporated films of Cu and Ni were successful (Fig. 4.2). Note that
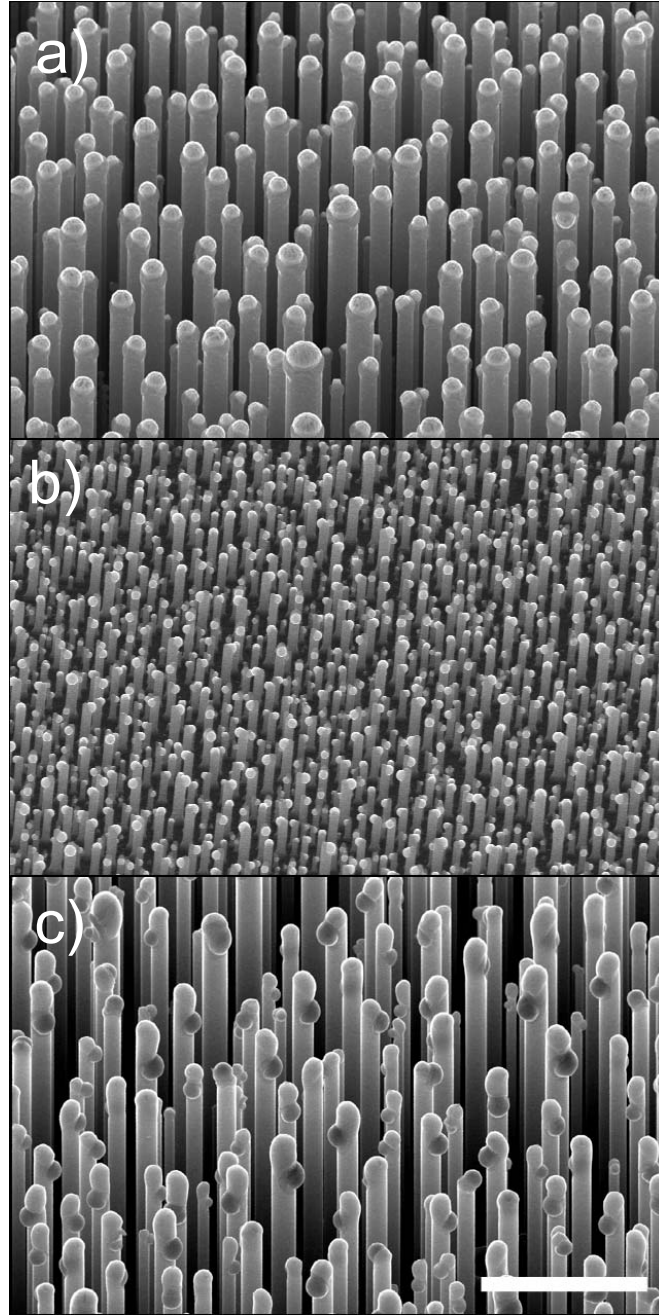
Figure 4.2. Representative SEM images of growth from evaporated (a) Au, (b) Cu, and (c) Ni films. In all cases 50 nm of the metal was thermally evaporated onto a Si(111) substrate that had been etched in buffered HF. Growth was undertaken by annealing in H_2 at a flow rate of 1000 sccm for 20 mins, followed by wire growth at H_2 and $SiCl_4$ flow rates of 1000 sccm and 20 sccm, respectively. In case (a) growth was at 1050 °C for 40 mins, in case (b) growth was at 1000 °C for 5 mins, and in case (c) growth was at 1050 °C for 20 mins. The scale bar is 20 μm and applies to all images.
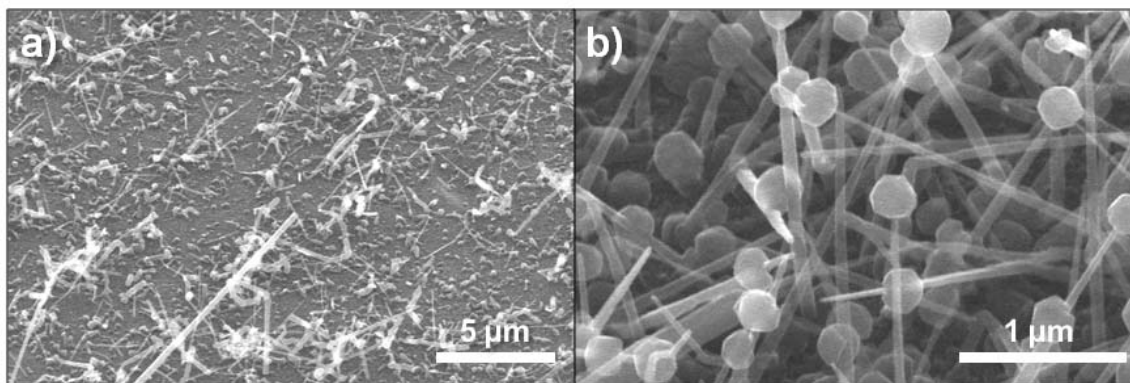
Figure 4.3. Representative SEM images of Al-catalyzed Si wire growth from $SiCl_4$ precursor. In this particular case, the sample consisted of a thermally evaporated, 33-nm-thick Al film on a Si(111) wafer. Growth was performed at 1000 °C and atmospheric pressure, by first annealing for 20 mins under H_2 at a flow rate of 1000 sccm, followed by wire growth for 5 mins under H_2 and $SiCl_4$, at flow rates of 1000 and 10 sccm, respectively. Two contrasting regions of the same sample are shown.

sometimes, and most often (but not solely) with Ni, we observed the VLS catalyst "dripping" off the side of the grown wire (Fig. 4.2 (c)). This presumably occurs after growth has finished, during evacuation and refilling of the growth tube with N_2, and/or cooling after removal of the wire array from the hot zone of the furnace. We infer this because grown wires can be straight for hundreds of μm, and yet have catalyst tips that are no longer atop the wire after removal from the growth chamber. Even with Ni this does not occur in all cases (see Fig. 4.11, for example).

Attempts to grow from evaporated thin films of Al did result in wire growth, although the results were far from ideal (Fig. 4.3). Given that Al is an abundant metal that forms a dopant rather than a trap level in Si, it is of considerable interest as a VLS catalyst of Si growth. If one wanted to pursue the use of Al for VLS from $SiCl_4$, further experimentation should first be done to ensure that Al is indeed catalyzing the growth, and that growth seen to date is not merely the result of Au contamination, for example.

Attempts to grow from Mg (not shown) led to no visible growth, probably related to its strong tendency to oxidize. In catalysts produced very rough, textured Si films, with a small number of wires (not shown), but in general the morphology was poor. Attempts to grow from Zn were similarly fruitless.
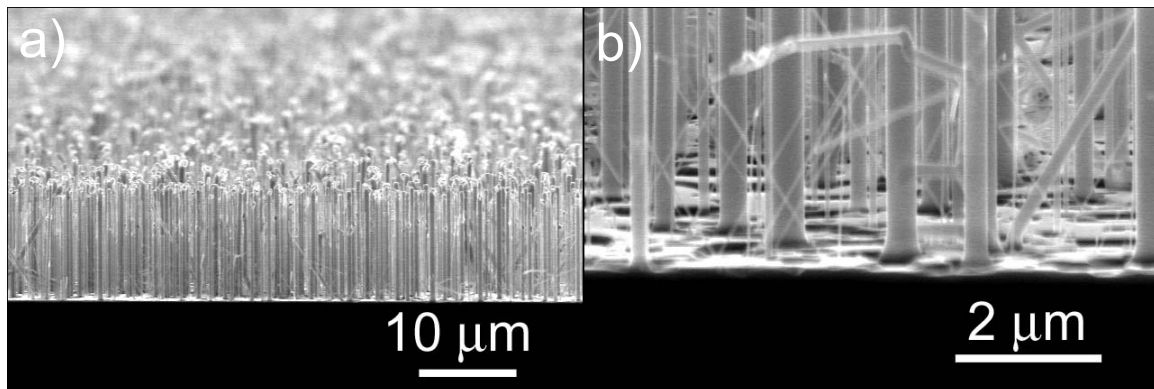
Figure 4.4. Result of growth using Au nanoparticles. The sample consisted of 200-nm-diameter Au nanoparticles, distributed on the surface of a Si(111) wafer as described in Ch. 4.3.2. Growth was performed at 1000 °C and atmospheric pressure, by first annealing for 20 mins under H_2 at a flow rate of 1000 sccm, followed by wire growth for 5 mins under H_2 and $SiCl_4$, at flow rates of 1000 and 10 sccm, respectively.

4.3.2   Growth from Nanoparticles

A greater degree of control on the wire diameter was introduced by depositing Au nanoparticles. This was done by using (3-Aminopropyl) Triethoxysilane (APTES) to immobilize Au nanoparticles on the surface of a wafer. Si(111) substrates were rinsed in acetone, isopropanol, and methanol, prior to being placed in a petri dish containing a mixture of 10 mL methanol and 0.1 mL APTES. APTES is extremely air sensitive, and therefore the mixture was prepared by using a syringe to extract 0.1 mL APTES from its bottle, and injecting the APTES into the methanol, beneath the surface of the methanol. The APTES and methanol were then mixed by stirring gently. After submerging the Si substrate in the APTES/methanol mixture, the petri dish was covered and left for 1 hour. The Si was then rinsed in methanol and in H_2O, making sure not to let the surface dry. After that, the Si was introduced to a second petri dish, which contained a well-mixed suspension of 200-nm-diameter Au nanoparticles in H_2O (Ted Pella). The sample was then removed, gently rinsed in H_2O and finally gently dried in N_2.

Samples prepared this way were introduced to the $SiCl_4$ APCVD chamber at 1000 °C and growth was conducted for 20 mins (Fig. 4.4).

4.3.3 TEM of SiCl$_4$-grown Wires

Si wires grown from SiCl$_4$ were examined under a transmission electron microscope (TEM). Samples were grown from a 100 nm Au nanoparticle colloid (deposited as described in the previous section), at 1000 °C, using H$_2$ and SiCl$_4$ at flow rates of 1000 sccm and 20 sccm, respectively. A fragment of the grown sample was sonicated in 100 µL of IPA for 2 mins, and 7 µL of the resulting suspension was dropcast on a lacey carbon grid (SPI Supplies). TEM was performed by Dr. Carol Garland using a Tecnai F30 transmission electron microscope.

In contrast to the SiH$_4$-grown wires (Ch. 3.4.1), wires did not appear to have sawtooth faceting. In fact the wires were quite smooth-walled over their entire lengths, and Au was not visible on the sidewalls of the wires. Also, the wires were single crystalline, with a lattice spacing of 0.307 ± 0.004 nm, consistent with growth in the [111] direction (Fig. 4.5).

Another feature of the wires was that the Au at the tips appeared to be embedded in a shell of silica (Fig. 4.6), which presumably occurred at the end of growth. At our growth temperature of 1000 °C, Si is soluble in liquid Au at concentrations approaching 50 atomic %, [102] far higher than the solubility of Si in solid Au at room temperature. This, combined with the driving force for oxidation of Si, [78], makes the observed structure perhaps unsurprising. It is also consistent with reports that Si can diffuse through Au even at room temperature, [103] and suggests that we need to expose the wires to a silica etch prior to a metal etch if we are to remove the catalyst particles (see Ch. 5).

4.4 Patterned VLS Growth

In order to achieve a higher degree of control of the size and position of the wires, as well as to enter the microwire rather than nanowire regime, we explored the use of photolithography to define the location of the catalyst. Attempts to grow Si wire arrays did not yield high pattern fidelity when the catalyst was not confined. Wires were grown by photolithographically patterning S1813 photoresist (Microchem) on a clean Si(111) wafer, then exposing it for 5 s to buffered HF(aqueous) (Transene, Inc., 9% HF, 32% NH$_4$F), followed by evaporation of 500 nm of Au and lift-off of the resist. This produced a square array of 3 µm diameter Au islands with a center-to-center pitch of 7 µm. Samples were then annealed in a tube furnace at 900 - 1000 °C for 20 mins under 1 atm of H$_2$ at a flow rate of 1000 sccm, followed by wire growth under 1 atm of H$_2$ and SiCl$_4$, at flow rates of 1000 and 20 sccm, respectively.
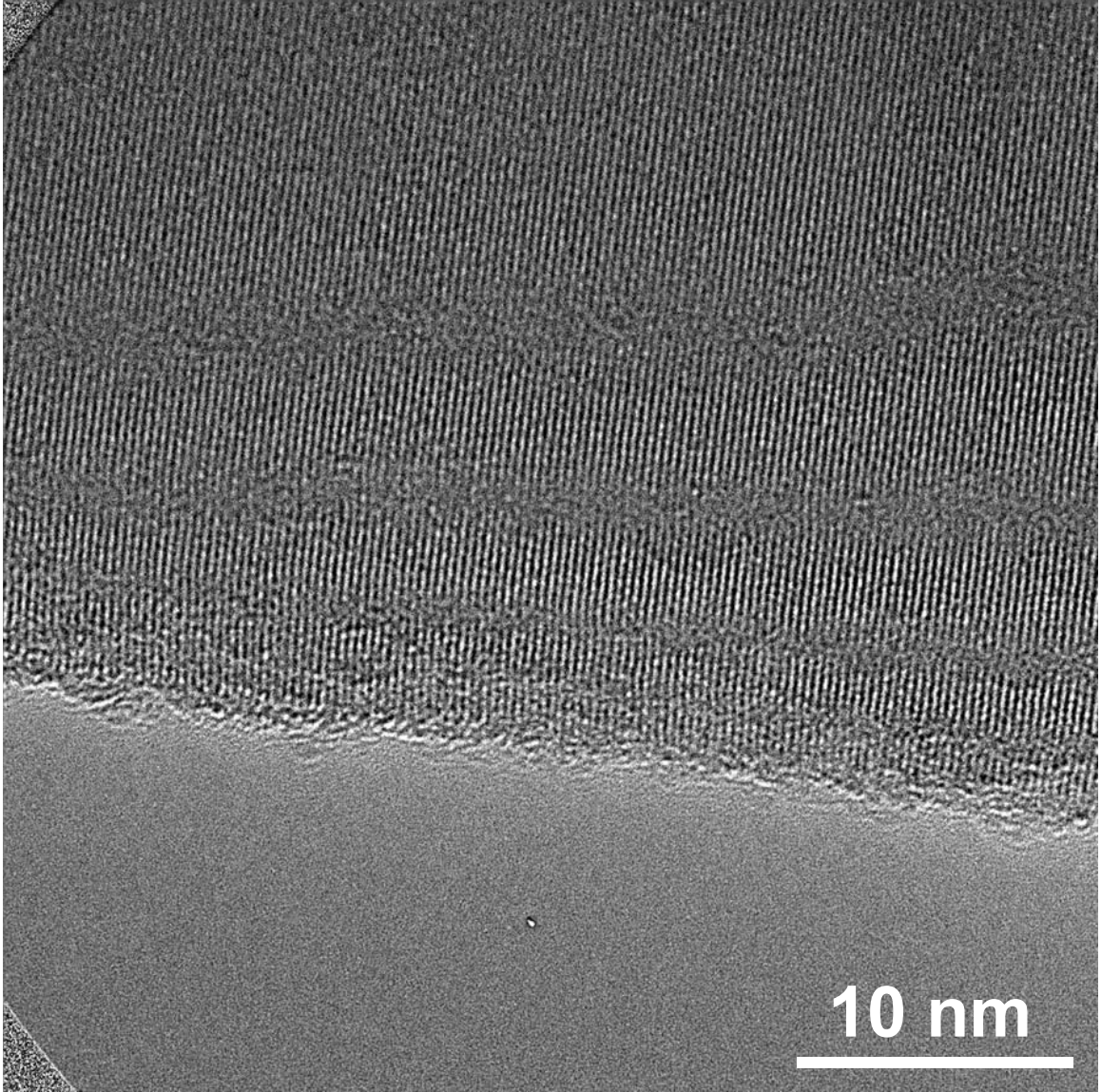
Figure 4.5. TEM image of a Au-catalyzed, SiCl$_4$-grown nanowire. The vertical lines are lattice fringes, and the horizontal bands are due to the curved surface of the wire causing interference fringes. From this image, we infer a lattice spacing of 0.307 $\pm$ 0.004 nm, consistent with growth in the [111] direction.
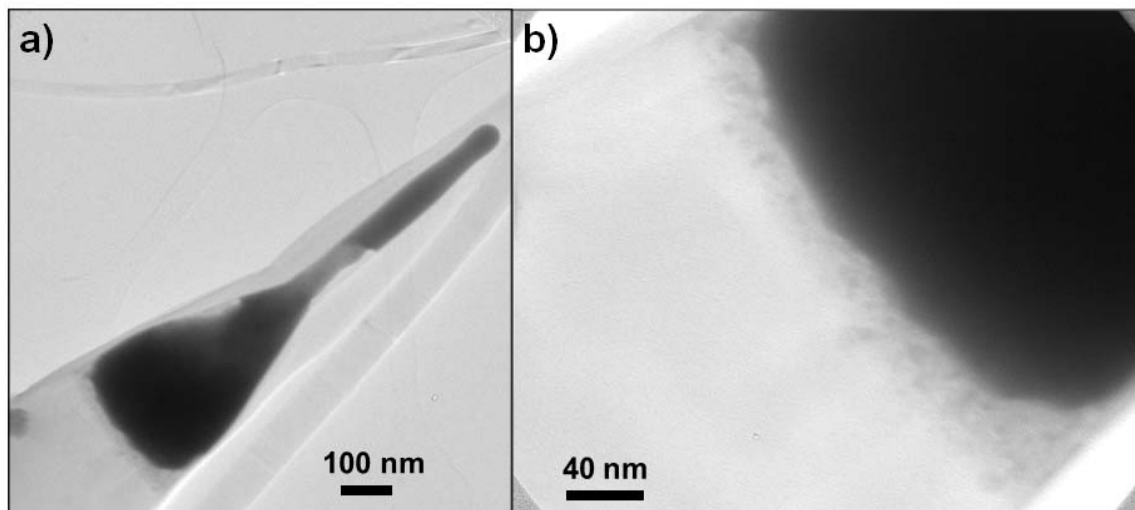
Figure 4.6. TEM images near the tip of a Au-catalyzed, $SiCl_4$-grown nanowire, showing segregation between the catalyst particle and SiO_x, leaving the metal apparently embedded in a shell of silica.

This produced arrays of low fidelity, with no control over the wire diameter or wire position (not shown). Examination of the samples after a 20 min H_2 anneal only revealed that this behavior was due to substantial agglomeration of the catalyst (Fig. 4.7).

The successful production of large-area Si wire arrays involved the use of an oxide buffer layer to confine the VLS catalyst to the desired areas in the pattern. To implement this approach, a 300 nm oxide was thermally grown on Si(111) wafers and then photolithographically patterned as described above. The oxide within the patterned resist holes was removed by immersion of the samples for 3 - 4 mins in buffered HF. The desired catalyst islands, now separated by a buffer oxide, were then formed by thermal evaporation of 300 - 500 nm of Au, followed by lift-off of the resist. These samples were then annealed in a tube furnace at 850 - 1100 °C for 20 mins under 1 atm of H_2 at a flow rate of 1000 sccm. Wires were then grown for up to 30 mins at 850 - 1100 °C with the same pressure and $SiCl_4/H_2$ flowrates as for the samples with no oxide.

This approach produced nearly defect-free arrays that exhibited an extremely narrow diameter and length distribution, and highly controlled wire position (Fig. 4.8). The wire growth was very uniform over areas > 1 cm^2, with the sample size currently limited by the diameter of our tube furnace. The growth uniformity declined within several hundred microns of the edges of the sample, presumably due to differences in temperature and/or
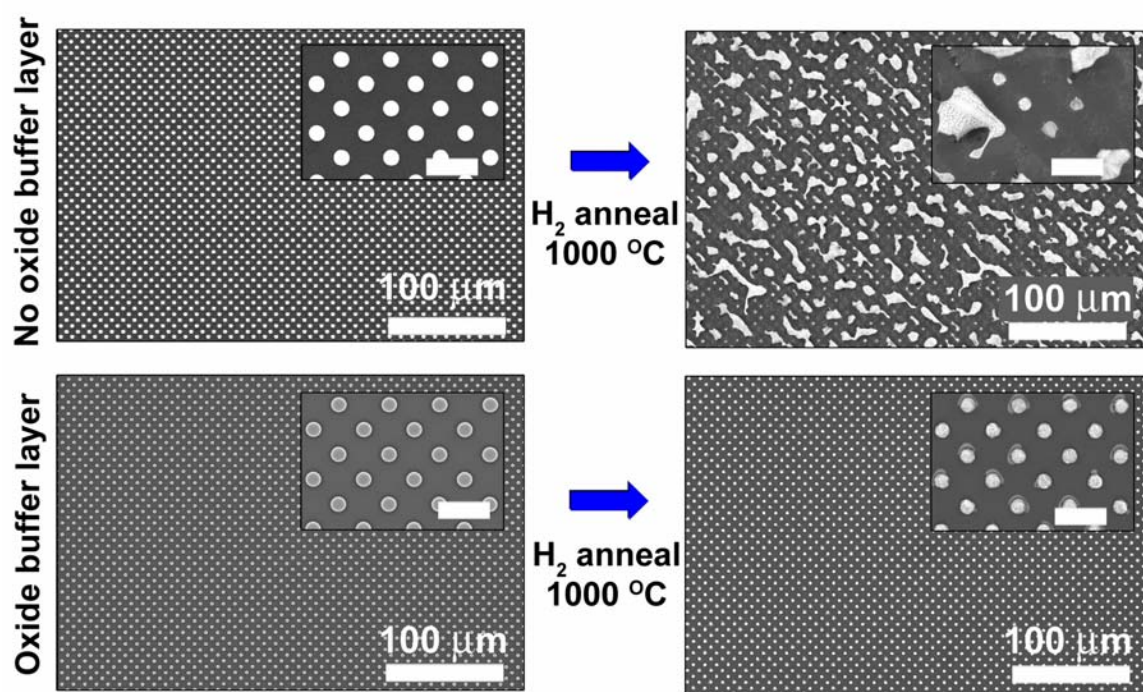
Figure 4.7. Effect of a 20 min anneal in H_2, at 1000 °C and atmospheric pressure, on Au arrays with and without a 300 nm oxide buffer layer, demonstrating the importance of the buffer oxide in maintaining the pattern fidelity. The scale bars in the insets are 10 μm.

gas flow at such locations.

The required thickness of catalyst is proportional to the diameter of the wires being grown, so 500 nm of catalyst material was required to produce 1.5 - 2 μm diameter Si wires. We believe that this relatively thick catalyst layer, and/or the higher growth temperatures, led to a significant problem with catalyst migration if a buffer oxide was not present on the surface, in contrast to earlier reports in which much thinner catalyst layers were used. [40] [104]

4.5   Effects of Temperature

Si nanowires have been grown previously at 800 - 900 °C with $SiCl_4/H_2$, [40] [104] but our optimal growth temperatures lie in the range 1000 - 1050 °C. At 950 °C and below, the wires either did not grow straight, grew intermittently straight with kinks, or grew straight but not aligned normal to the substrate (not shown). This difference in optimal growth temperatures between Si nanowires and Si microwires is not necessarily surprising because size-dependent effects have been observed for other aspects of VLS growth. [105] At 1075 °C and above, the wires grew straight and normal to the substrate, but significant destruction of the surface oxide was observed during the growth process, leading to a loss of the pattern fidelity (see Fig. 4.9).

4.6   Changing VLS Growth Catalyst

Chemical characterization of our Au-catalyzed Si wires, grown by VLS with $SiCl_4$ at 1000 °C, indicates Au concentrations of $\sim 1.7 \times 10^{16}$ cm^{-3} inside the "bulk" of each wire (surface concentrations were higher). [72] This is consistent with our work on the single-wire optoelectronic characterization of these wires, which indicates that minority hole diffusion lengths are ~ 2 μm in as-grown Si wires. [55] This is also consistent with the notion that the vapor-liquid-solid (VLS) catalyst is being incorporated into the growing crystal at its solubility limit at the growth temperature, [69] at least for wires of the size scale considered here, and under our growth conditions.

As stated in the previous chapter, we expect that Au concentrations this high will lead to additional degradation of V_{oc} separate from geometrical effects, and therefore greater loss in overall device performance than what should be achievable in a radial junction geometry
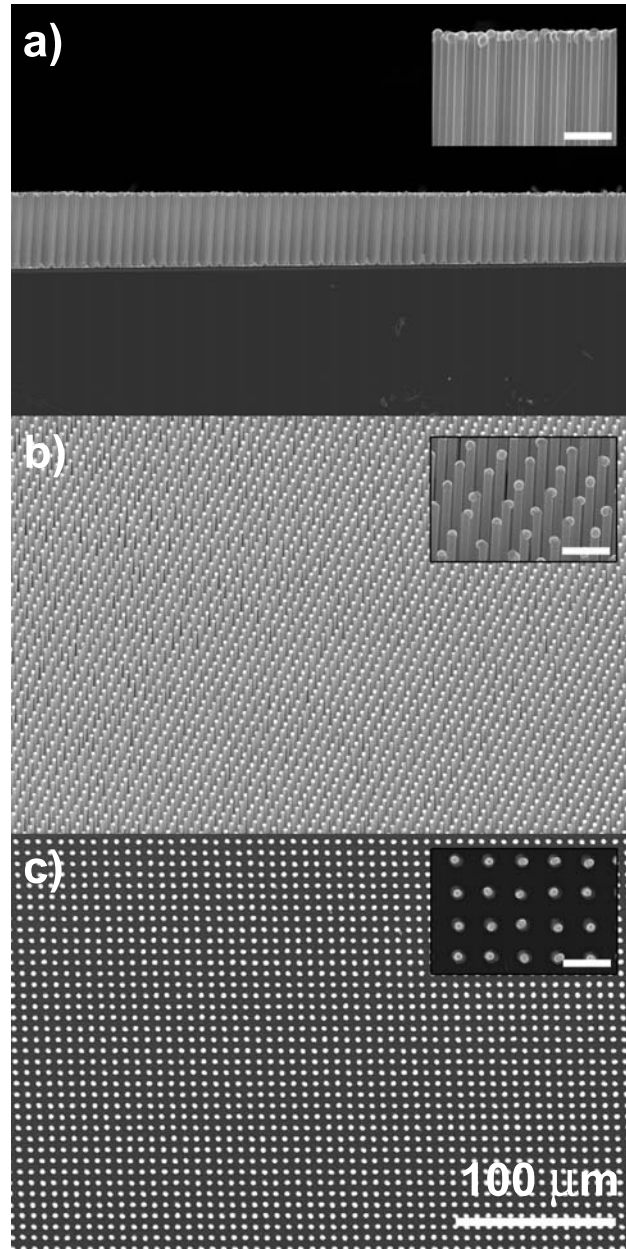
Figure 4.8. (a) Edge-on, (b) tilted, and (c) top-down SEM views of a Au-catalyzed Si wire array having nearly 100% fidelity over a large (> 1 cm^2) area. The 100 μm scale bar applies to all three panels, and in all cases the scale bar in the insets is 10 μm. Before wire growth, the sample consisted of 500-nm-thick, thermally-evaporated Au islands within 3 μm holes (in a square array with 7 μm pitch) in a 300-nm-thick oxide, on a Si(111) wafer. Growth was performed at 1000 °C and atmospheric pressure, by first annealing for 20 mins under H$_2$ at a flow rate of 1000 sccm, followed by wire growth for 30 mins under H$_2$ and SiCl$_4$, at flow rates of 1000 and 20 sccm, respectively.
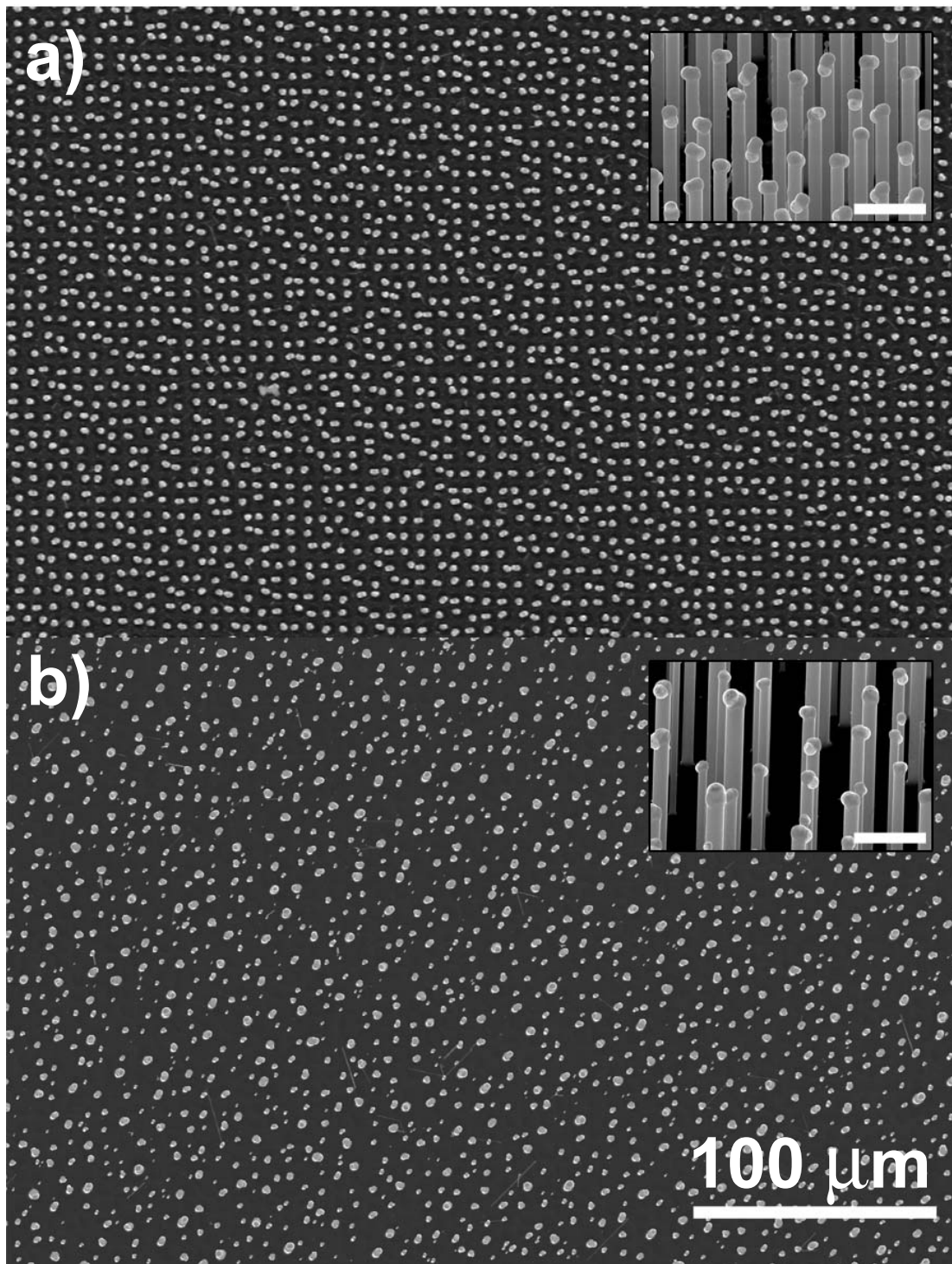
Figure 4.9. Top-down and (inset) tilted SEM views of the Au-catalyzed Si wire growth at (a) 1075 °C and (b) 1100 °C, showing the breakdown in pattern fidelity due to the destruction of surface oxide. The 100 µm scale bar applies to both panels, and the scale bars in the insets are 10 µm.

with longer diffusion lengths. The use of alternative catalysts may allow for the VLS growth of higher-quality Si than is possible with a Au catalyst.

Cu and Ni were found to be effective VLS catalysts, as shown above in Fig. 4.2, and are therefore potentially interesting as alternatives to Au. Cu has previously been reported as a VLS catalyst [33] [106] as well as a vapor-solid (VS) catalyst, [107] and Ni has previously been reported as a VLS catalyst. [33] [108]

The bulk solubilities of Cu and Ni at our growth temperature ($\sim$ 1000 °C) have been reported as $\sim$ 3 $\times$ 10^{17} cm^{-3} and $\sim$ 1 $\times$ 10^{17} cm^{-3}, respectively, [69] [77] which for the case of Cu at least is slightly below the concentration at which impurities have been seen to degrade solar cell performance, at least in the case of a p-type base. [109] Minority carrier lifetimes of $\sim$ 100 ns have been measured in Si which has had Ni diffused into it at 1000 °C. [110] Preliminary results from our group indicate effective hole diffusion lengths in n-type, Ni-catalyzed, Si wires to be $\sim$ 10 μm. [54] In the case of Cu, minority carrier diffusion lengths of $\sim$ 20 μm have been measured in n-type Si with Cu concentrations in the 10^{17} cm^{-3} range. [111] Also, Si with even larger minority carrier diffusion lengths ($>$ 30 μm) has been grown directly from a Si-Cu melt by liquid phase epitaxy at temperatures similar to our growth temperatures, and high-performance PV devices (with efficiency $>$ 15%) have been fabricated from this material. [112] Finally, both elements are far more diffusive in Si than is Au, [16] which could prove to be useful if additional gettering steps are required. [113] However, both Ni and Cu form silicides with Si which can potentially further degrade material quality. [114] [115] [116] [111] [117] Thus stricter processing control may be required in attempting VLS growth with these catalysts.

As discussed previously, Ni and Cu are also far more abundant, and inexpensive, than is Au, which provides another motivation for using them as catalysts (see Fig. 3.2).

Nominally identical wire arrays were produced, under similar growth conditions, when Cu or Ni was used as the VLS catalyst instead of Au (Figs. 4.10, 4.11).

4.7   Changing Wire Diameter and Pitch

As discussed in Ch. 2, control of wire diameter and wire packing fraction may prove extremely important in maximizing the conversion efficiency in our proposed cell design. This is for several reasons: conversion efficiency in radial pn junction devices is generally
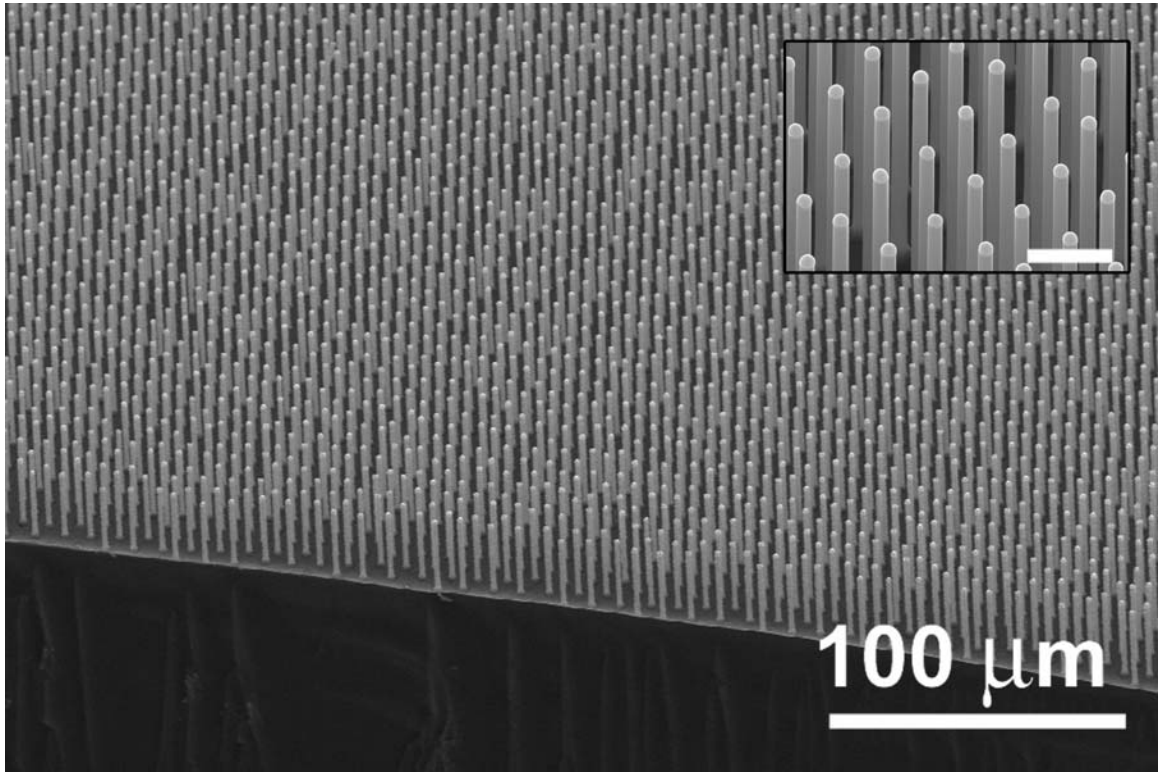
Figure 4.10. Tilted SEM views of a Cu-catalyzed Si wire array having nearly 100% fidelity over a large (> 1 cm^2) area. The scale bar in the inset is 10 µm. Before wire growth, the sample consisted of 500-nm-thick, thermally-evaporated Cu islands within 3 µm holes (in a square array with 7 µm pitch) in a 300-nm-thick oxide, on a Si(111) wafer. Growth was performed at 1000 °C and atmospheric pressure, by first annealing for 20 mins under H$_2$ at a flow rate of 1000 sccm, followed by wire growth for 10 mins under H$_2$ and SiCl$_4$, at flow rates of 1000 and 20 sccm, respectively.
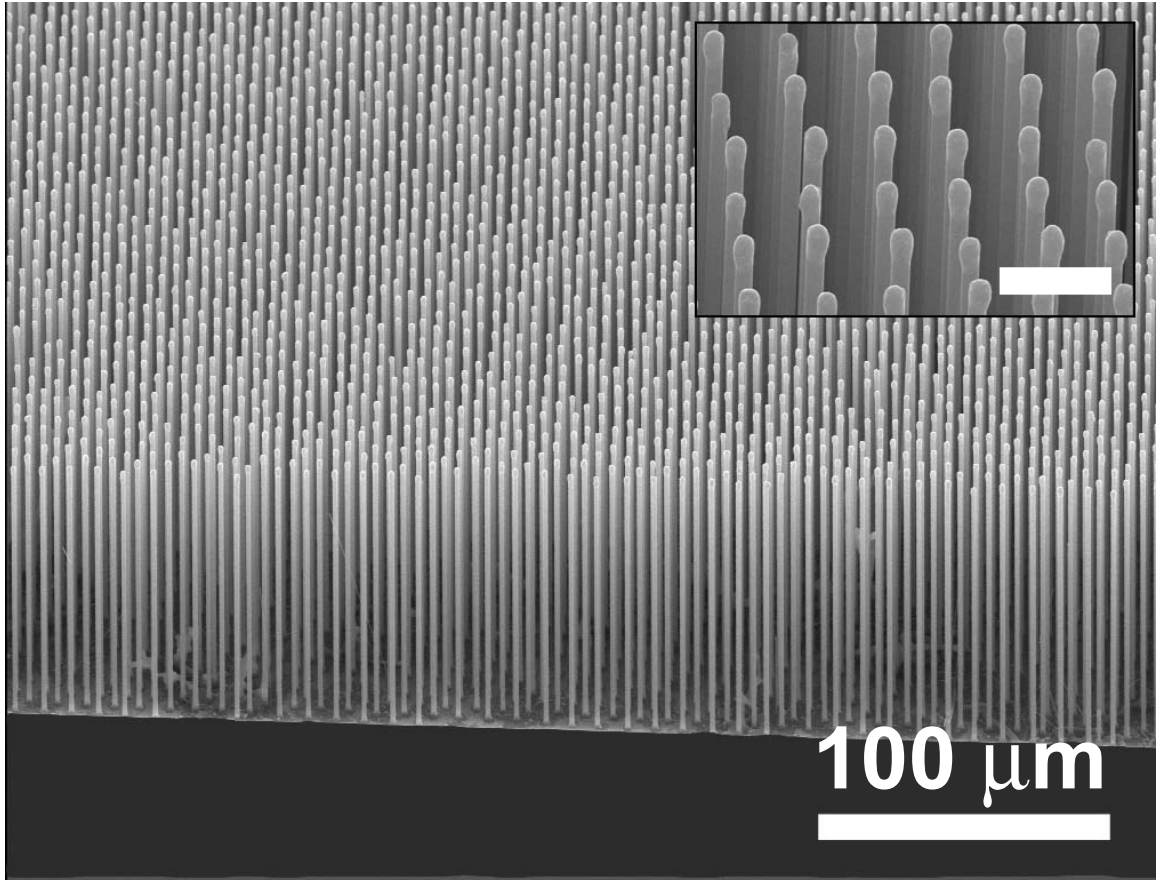
Figure 4.11. Tilted SEM views of a Ni-catalyzed Si wire array having nearly 100% fidelity over a large (> 1 cm^2) area. The scale bar in the inset is 10 µm. Before wire growth, the sample consisted of 300-nm-thick, thermally-evaporated Ni islands within 3 µm holes (in a square array with 7 µm pitch) in a 300-nm-thick oxide, on a Si(111) wafer. Growth was performed at 1000 °C and atmospheric pressure, by first annealing for 20 mins under H$_2$ at a flow rate of 1000 sccm, followed by wire growth for 20 mins under H$_2$ and SiCl$_4$, at flow rates of 1000 and 20 sccm, respectively.

maximized when wires have radii of 0.5 - 1 × the minority carrier diffusion length in the wire cores (as noted in Ch. 2), high wire packing fractions may be necessary in order to absorb a large fraction of the incident sunlight, and perhaps light trapping features enabled by periodic structures with features with dimensions on the order of the wavelength of visible light (i.e., photonic crystals) can be exploited to enhance the absorption of light in certain wavelength ranges. [118] We note briefly that the pitch of the growth template need not dictate the wire pitch in a final device. Our group has recently demonstrated the in-filling and peeling off of wire arrays with low-cost polymers, [119] as well as the shrinking of the in-fill polymer after peel off, to reduce the distance between wires as grown. Alternatively, increased wire diameter and packing fraction could be achieved by conformal deposition onto the grown wire array after catalyst removal, either to form abrupt, deposited junctions, or to epitaxially thicken the as-grown wires.

Nevertheless, control of wire diameter and pitch during growth could prove to be very useful and important. Wire diameter and pitch can be varied, within some limits, simply by changing the diameter and pitch of the circles in the photolithographic pattern, and then following the procedure outlined above in Ch. 4.4. A 2 μm minimum feature size was targetted as a comfortable limit on the resolution of our photolithography equipment. It is also a reasonable size scale for what might be achievable with pattern stamping in the future. Therefore, photolithographic masks were made with 2 μm diameter holes and 4 μm pitch, 5 μm diameter holes and 7 μm pitch, and 10 μm diameter holes and 12 μm pitch, all in hexagonal close packed arrangements. This unfortunately did not allow a clear comparison of the effect of changing the catalyst particle size with the previous studies on square arrays with 4 μm inter-hole spacing, as the reduction of the inter-hole spacing appeared to make the oxide barrier less effective in preventing catalyst migration. Nevertheless, this approach was pursued to form arrays of nominally 2 and 5 μm diameter wires using a Cu catalyst, as shall be discussed below in Ch. 4.7.1.

As already mentioned, we have seen that the diameter of the grown wires is approximately proportional to the thickness of the deposited catalyst islands, as might be expected if the volume of the catalyst island (plus some volume of Si, determined by the volume of metal and the solubility of Si in the liquid metal at the growth temperature) determines the volume of the catalyst hemisphere atop the growing wires. Therefore, if one is to grow dense arrays of 10-μm-diameter wires, one might expect that catalyst island thicknesses of

up to 2 µm will be required. This requires alternatives to the photolithography / wet etch / evaporation / lift off procedure outlined above. Preliminary results towards this goal, using a Cu catalyst, will be discussed in Ch. 4.7.2.

4.7.1 2 µm and 5 µm Patterns

The 2 µm and 5 µm patterns were approached as a simple extension of the procedure outlined in Ch. 4.4. Namely, Si(111) wafers coated with a 300 nm oxide were patterned photolithographically and the oxide was etched, and 300 nm of Cu catalyst was thermally evaporated, followed by lift off. Si wire growth was then conducted under nominally the same conditions as those outlined above. This proved successful (Fig. 4.12), but to date the areas of high fidelity wire growth achieved, particularly with the 5 µm pattern, have not been as large as those achieved with the original 3 µm diameter, 7 µm pitch square array (not shown).

Presumably the primary limitation in this case is the fact that the 2 µm oxide barrier between holes in our close packed arrays is less effective at preventing catalyst migration than the 4 µm barrier in the case of our square array. Perhaps this could be mitigated by using thicker oxide layers, and thus having the metal catalyst sitting deeper inside the patterned holes. It is also possible, but yet to be shown, that higher $SiCl_4$ flow rates will provide improved results, as the total volume of catalyst material per unit Si(111) surface is increased for these denser arrays, and so the surfaces can presumably tolerate higher fluxes of the Si precursor.

4.7.2 10 µm Pattern

As thick catalyst layers are required to seed densely-packed, large-diameter wire arrays, novel routes to sample preparation may need to be pursued. With a close-packed, 10 µm diameter hole pattern with 12 µm pitch, lift off proved to be difficult, simply due to the relatively small fraction of the photoresist area which is left behind after the pattern is developed. This is exacerbated by the fact that catalyst layers > 1 µm thick will likely be needed to seed dense arrays of such large diameter wires, a thickness which is non-trivial for lift off without specialized photoresists.

Furthermore, as our buffered HF wet oxide etch is isotropic this leaves the oxide mask with a bevelled cross-section relative to the underlying Si substrate (not shown). A thick
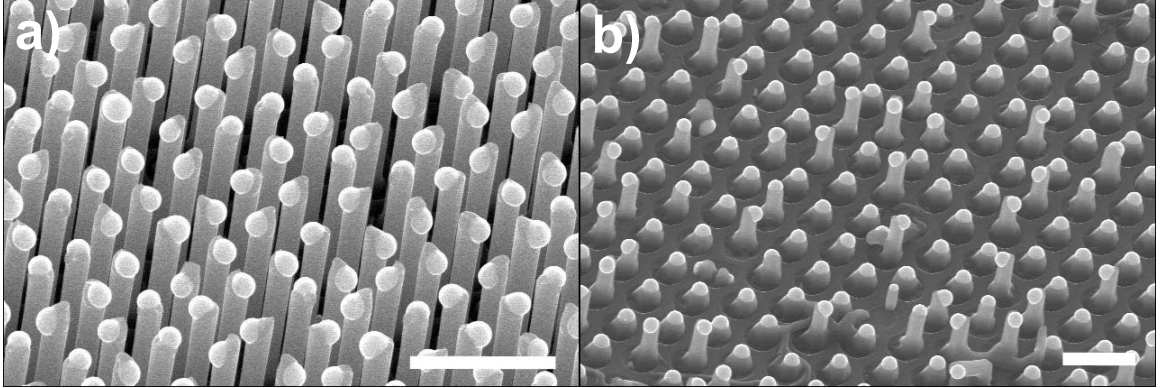
Figure 4.12. Representative SEM images of growth from (a) 2 μm and (b) 5 μm patterns. The scale bar is 10 μm in both images. In (a), before wire growth the sample consisted of 300-nm-thick evaporated Cu islands in 2 μm holes in a 300-nm-thick oxide, with a 4 μm pitch in a hexagonal close-packed array, on a Si(111) wafer. Growth was performed at 1050 °C and atmospheric pressure, by first annealing for 20 mins under H_2 at a flow rate of 1000 sccm, followed by wire growth for 5 mins under H_2 and $SiCl_4$, at flow rates of 1000 and 20 sccm, respectively. In (b), before wire growth the sample consisted of 300-nm-thick evaporated Cu islands in 5 μm holes in a 300-nm-thick oxide, with a 7 μm pitch in a hexagonal close-packed array, on a Si(111) wafer. Growth was performed at 1000 °C and atmospheric pressure, by first annealing for 20 mins under H_2 at a flow rate of 1000 sccm, followed by wire growth for 30 mins under H_2 and $SiCl_4$, at flow rates of 1000 and 20 sccm, respectively.

catalyst layer requires a thick oxide layer to contain the catalyst islands, and when the oxide thickness becomes comparable to the minimum feature spacing, the bevelled cross-section can reduce the effectiveness of the oxide in preventing catalyst migration. For example, isotropic wet etching of holes with a 2 μm spacing, in a 1 μm thick oxide, implies that when the bottom of the holes is reached, the tops of the sidewalls will also touch, as the vertical etch rate will be the same as the horizontal etch rate. This presents a problem for several reasons. Firstly, this sets a limit on how closely we can pack our catalyst islands for a given catalyst thickness, which poses problems for extending our general method to more closely packed arrays of wires with larger diameter. Secondly, this makes lift off difficult - if the oxide is almost entirely etched from beneath the photoresist prior to metal evaporation then the resist no longer will have the integrity to function. Thirdly, a triangular barrier will presumably not be as effective at preventing catalyst migration as a square one.

Attempting to pattern samples without a liftoff step, and observing that Si wires do not nucleate so readily on an oxide surface, [34] we therefore explored photolithography simply as a means to pattern thick ($\sim$ 1 μm) oxides on Si(111) (Fig. 4.13 (a)), after which we removed the photoresist and evaporated catalyst metal across the entire surface of the sample. Subsequent wire growth from samples of this kind showed this approach to be successful, but only to a limited extent. In some parts of the samples, wire growth was indeed confined by the oxide pattern (Fig. 4.13 (b)), but for the majority of the sample this was not the case, with wires of significantly larger diameters growing with no apparent relationship to the underlying oxide pattern (not shown).

We have explored the use of reactive ion etching (RIE - see also Ch. 5.5) to achieve oxide features with straight sidewalls. M. David Henry prepared samples by depositing a PECVD oxide layer, evaporating a 100 nm Cr hard mask, defining a pattern in the Cr by photolithography and wet etching, and then etching the pattern by RIE (Fig. 4.14 (a)). Cu was then thermally evaporated across the sample and APCVD growth of Si wires conducted. However, high-quality arrays have not been achieved from these patterns to date. This is for three primary reasons. Firstly, either the oxide as deposited was very rough or even porous, or the RIE process caused it to become so (Fig. 4.14 (b)). This prevented the oxide layer from acting as a barrier to Cu catalyst migration. Secondly, the RIE etching did not stop at the Si surface (Fig. 4.14 (b)), allowing other Si surfaces than the (111) to be exposed during growth. Finally, the selectivity of growth to Si rather than SiO_2 is
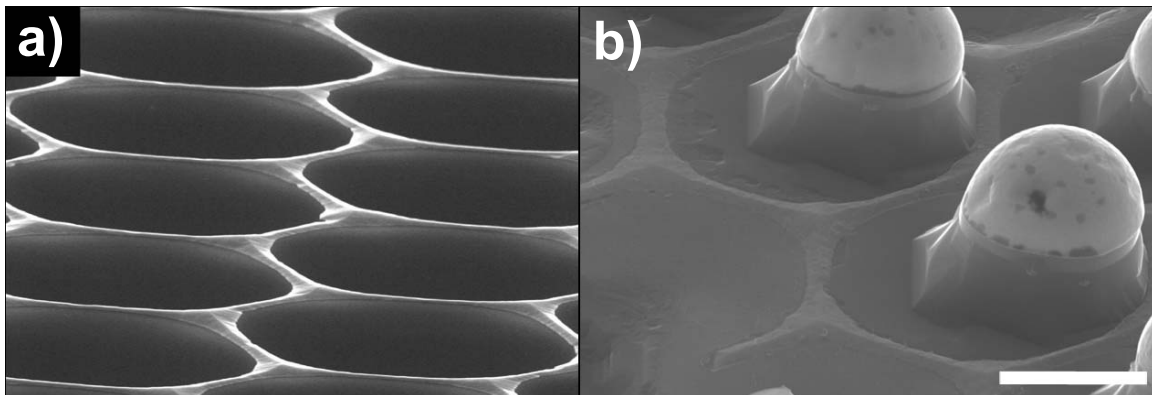
Figure 4.13. Representative SEM images of growth from 10 µm pattern, (a) before deposition of Cu, and (b) after deposition of 2 µm Cu and subsequent CVD growth. Before wire growth the sample consisted of a 2 µm-thick evaporated Cu layer on top of the 10-µm-diameter, 12-µm-pitch pattern shown in (a), on a Si(111) wafer. Growth was performed at 1000 °C and atmospheric pressure, by first annealing for 20 mins under H_2 at a flow rate of 1000 sccm, followed by wire growth for 15 mins under H_2 and $SiCl_4$, at flow rates of 1000 and 20 sccm, respectively. The scale bar is 5 µm and applies to both images.

not perfect, as mentioned above. This last point was exacerbated by the porosity of the oxide layer. RIE patterning of oxides may prove more effective when the initial oxide is a high-quality thermally-grown oxide.

These "lift-off-free" approaches may prove more successful if the catalyst is deposited selectively inside the pores, by electrodeposition for example.

4.8 Conclusion

In this chapter we have outlined a straightforward procedure to attain excellent control of the size, position, and uniformity of vertically aligned, large-area Si wire arrays, using VLS growth from a $SiCl_4$ precursor and an oxide mask to prevent catalyst migration on the growth substrate. Arrays of wires have been grown with wire diameters in the range 1 - 3 µm, and lengths controlled by the deposition time - wire lengths in the range from ~ 5 µm up to hundreds of µm have been demonstrated. We have shown that the method works equally well with Ni and Cu, as opposed to the more common VLS catalyst Au, which may have important technological implications. For technological applications where cost is a concern, such as in PV devices, it is possible that the control afforded by patterning of
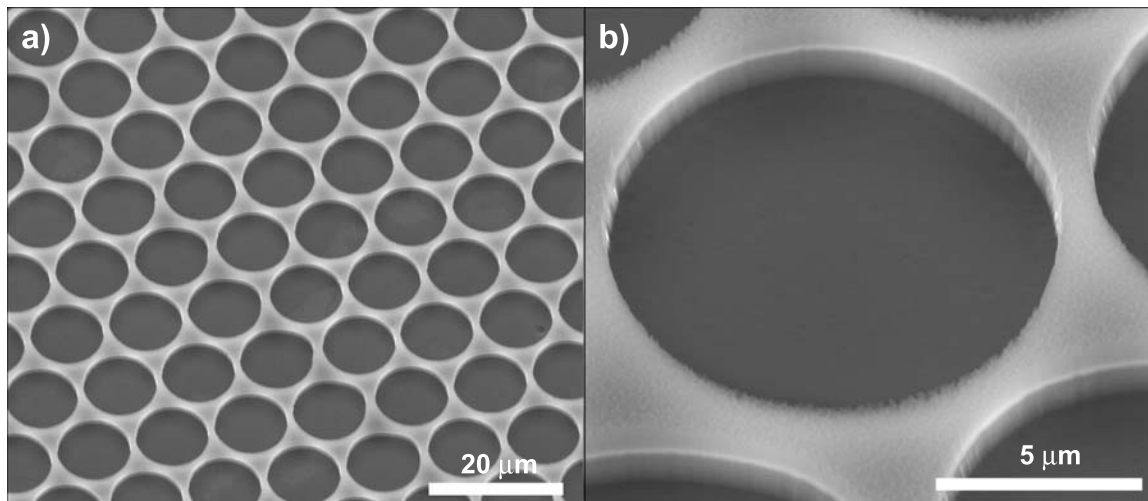
Figure 4.14. Representative SEM images of a 10 μm pattern, prepared by RIE on an oxide deposited by PECVD. The porosity of the oxide layer is visible in (b).

growth will be outweighed by the additional processing and cost that patterning requires, and therefore better understanding of unpatterned growth, as displayed for example in Fig. 4.2, may be important looking forward.

To illustrate the utility of these arrays in novel photovoltaic device designs, we have recently reported a Si wire photoelectrochemical cell. [120] We expect that these arrays may also be useful as photonic crystals, as well as in other novel energy conversion devices where a high surface area is desired. Finally, it should be possible to extend this methodology to alternative lithographic techniques, as well as to making wire arrays of materials that cannot currently be fabricated with top-down methods.

Chapter 5

Device Fabrication and Photovoltaic Measurements of Wire Arrays

5.1 Introduction

This chapter concerns initial experiments to investigate the viability of using VLS-grown Si wire arrays in solid state PV devices. We predicted in Ch. 2 that to attain high efficiency in this new geometry it is essential that the depletion region trap density remain relatively low. For Si with a homogeneous distribution of impurities, we expect that minority carrier lifetimes of > 40 ns will be required. We demonstrated in the previous chapter the growth of high-fidelity VLS-grown Si wire arrays using Cu and Ni as catalysts. This is an important alternative to the more commonly used Au, both from an economic point of view, but also, we expect, in terms of the effect of the catalyst on the optoelectronic properties of the Si.

In this chapter we will outline an approach to the fabrication of radial pn junction PV devices based on arrays of VLS-grown Si wires. This will be followed with results to date from the characterization of these structures. Finally, we discuss the use of reactive ion etching (RIE) to fabricate structures morphologically similar to the VLS-grown cells, which allows us to investigate any purely geometrical limitations to the radial pn junction design, free from issues related to material quality in grown wires, and difficulties associated with contacting devices from grown wires.

5.2 Fabrication of a Device Using Grown Wires

5.2.1 Catalyst Removal

After a wire array was grown by the method described in the previous chapter (and reproduced in Appendix B), the first step towards making a device involved removing the metal

catalyst particle at the tip as well as the near-surface of the wires. For gold the tip was removed the following way: [121]

1. 10:1 solution of DI water : 48% HF for 30 s to remove surface oxide on the Si.

2. 9:1 solution of TFA etchant (Transene): 38% HCl for 20 mins.

3. 10:1 solution of DI water : 38% HCl for 10 s to rinse.

4. Rinse in DI water, dry with N_2.

For Cu and Ni the following procedure was used:

1. Buffered HF (Transene) for 30 s.

2. RCA 2 clean (6:1:1 H_2O:H_2O_2:HCl at 70 °C) for 10 mins. [83]

3. Buffered HF (Transene) for 30 s.

4. Rinse in DI water, dry with N_2.

In some cases the RCA 2 cleaning step damaged the wire array, apparently by the physical impact of bubble formation on the wire surfaces and/or collisions between bubbles and wires. This was only noticed once, on an array whose wires were $\lesssim 1.5$ μm, and so may not be a problem for larger-diameter wires.

The Si at the near-surface was then removed by immersion of the sample in 60 wt.% KOH at 30 °C for 30 s. On a planar SOI control sample, with a Si(100) device layer (which is etched slightly less rapidly by KOH than is Si(110) [122]), this was found to remove 23 nm of Si per min. Seidel et al. give the etch rate under these conditions as 18 nm/min for Si(100), and 27 nm/min for Si(110). [122] Prior to doping, we ensured that the pattern oxide is fully removed (from the front side only) to ensure that the wire emitters are all connected. This was done by floating the sample, face down, on a drop of buffered HF (Transene) for about 4 mins.

5.2.2   Doping: Radial pn Junction Formation

The front side of the arrays were then doped n-type by stacking parallel to SiP_2O_7 diffusion wafers (PH-950, Saint-Gobain Ceramics), introducing to a tube furnace at 750 °C, ramping

up to 800 °C (over about 5 mins), holding at 800 °C for 40 mins, and then ramping back down, all under UHP N_2 at 5 lpm. The front surface was then exposed to buffered HF for 2 mins. This constitutes the n-type diffusion step. This approach, using post-growth dopant diffusion from source wafers, was taken simply for convenience, and future efforts in our group will look at the use of dopant gases during wire growth.

The samples were then re-introduced to the tube furnace, this time without the SiP_2O_7 diffusion wafers, at 750 °C under house N_2 bubbled through near boiling H_2O, ramped to 855 °C (over about 16 mins), and held at 855 °C for 20 mins, in order to create a high-quality surface oxide to prevent out-diffusion of the dopant atoms. The gas was then changed to dry house N_2, and the temperature ramped up to 1100 °C and held at this temperature for up to 23 hours in order to "drive in" the dopant atoms. Temperature was then ramped back down to room temperature, and the samples were not removed from the center of the furnace until the temperature there had at least dropped below 750 °C. The front surface was then exposed to buffered HF for long enough that the oxide was removed (determined by the time it took to change a planar control from hyrdophilic to hydrophobic). This constitutes the n-type drive step.

The front surface of the samples were then doped p-type by stacking parallel to BN diffusion wafers (BN-975, Saint-Gobain Ceramics), introducing to a tube furnace at 750 °C, ramping up to 950 °C, holding at 950 °C for 40 mins, and then ramping back down, all under UHP N_2 at 5 lpm. The front surface was then exposed to buffered HF for 2 mins. This was followed by a low temperature oxidation at 750 °C for 20 mins, under O_2 at 5 lpm. The front surface was again exposed to buffered HF for long enough that the oxide was removed (determined by the time it took to change a planar control from hyrdophilic to hydrophobic). This constitutes the p-type emitter diffusion step.

This procedure was developed to target a doping level of $\sim 10^{17}$ dopants/cm^3 in the wire cores, and a sheet resistance of 50 - 100 Ω cm in the emitter [123] (where the optimal emitter dose was determined empirically - diffusions at 900 °C or 1000 °C were found to reduce planar cell performance relative to a diffusions at 950 °C), and involved a combination of modeling using a spreadsheet tool developed by M. D. Kelzenberg, based on standard diffusion models as explained for example in [124] and on empirical data from [125] and [126], as well as 4 point probe resistivity measurements of planar control samples and well-established relationships between Si resistivity and dopant density. [50]

An SOI planar control doped by the same procedure as outlined above was sent to Solecon for spreading resistance depth profiling in order to assess the effectiveness of this procedure in attaining the doping profile we wanted. The results are shown in Fig. 5.1. We indeed see an n-type doping level of $\approx 10^{17}$ cm^3 throughout the base, and a highly doped p-type emitter, with surface concentration near the bulk solubility of B in Si at the emitter diffusion temperature, extending several hundred nm into the Si.

5.2.3 Metallization

Finally, the sample edges were cleaved off to prevent macroscopic shunting, oxide was removed from the entirety of the samples with buffered HF (Transene), and contact was made to the back surface by immediately rubbing Ga/In onto the back of the sample and the sample then bonded with Ag paste (SPI Supplies) to a piece of stainless steel to which electrical contact could be made with a probe tip. Contact was made to the front surface with a spot of Ga/In and an electrical probe tip. This led to the cell structure as depicted in Fig. 5.2. This method of contacting was used for convenience and was shown on homogeneously doped planar wafer samples to produce ohmic contacts of low resistivity (not shown).

5.3 Characterization of VLS-grown Samples

Samples were then tested in the light (under AM1.5D sunlight at 1 sun intensity, as calibrated with a BP Solar reference cell) and in the dark. This results in excitation of the wire array as well as the underlying Si and the adjoining planar regions. To date, our best cell, made from Cu-catalyzed, VLS-grown Si wire arrays, exhibited a J_{sc} of ≈ 12 mA/cm^2, V_{oc} of 213 mV, FF of 33 %, and overall efficiency of 0.87 % (Fig. 5.3). The J_{sc} was calculated by dividing the measured current by the total cell area, ≈ 0.42 cm^2, including the region where contact was made to the device. These results compare favorably with other published results for nanowire solar cells fabricated from VLS-grown wires, and tested over macroscopic areas. [127] [128]

Plotting V_{oc} vs. ln (J_{sc}) at close to 1 sun illumination intensity allows us to extract the diode quality factor of the cell, because

$$V_{oc} \approx \frac{nk_BT}{q} ln\left(J_{sc}\right) - \frac{nk_BT}{q} ln\left(J_0\right), \tag{5.1}$$
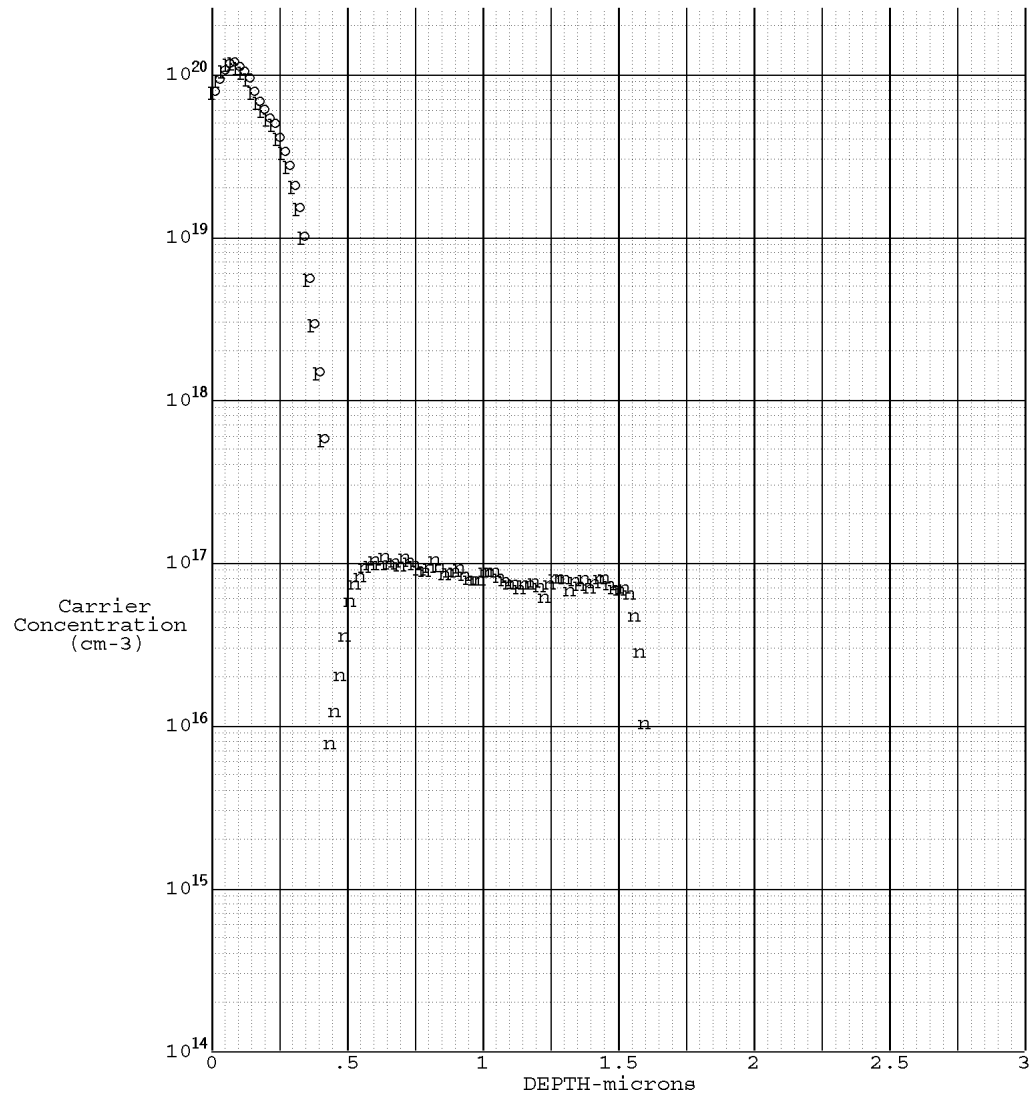
Figure 5.1. Spreading resistance depth profile of a control SOI wafer, indicating carrier concentration and type as a function of depth. Courtesy of Solecon Labs.
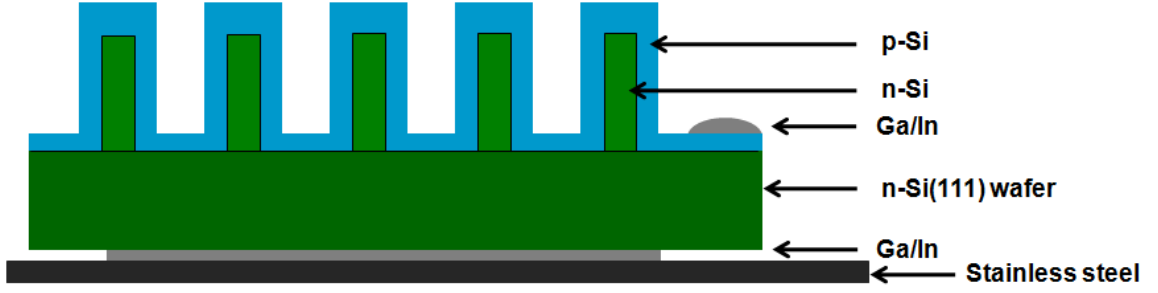
Figure 5.2. Schematic of VLS-grown wire cell, results from the characterization of which are presented in Fig. 5.3.
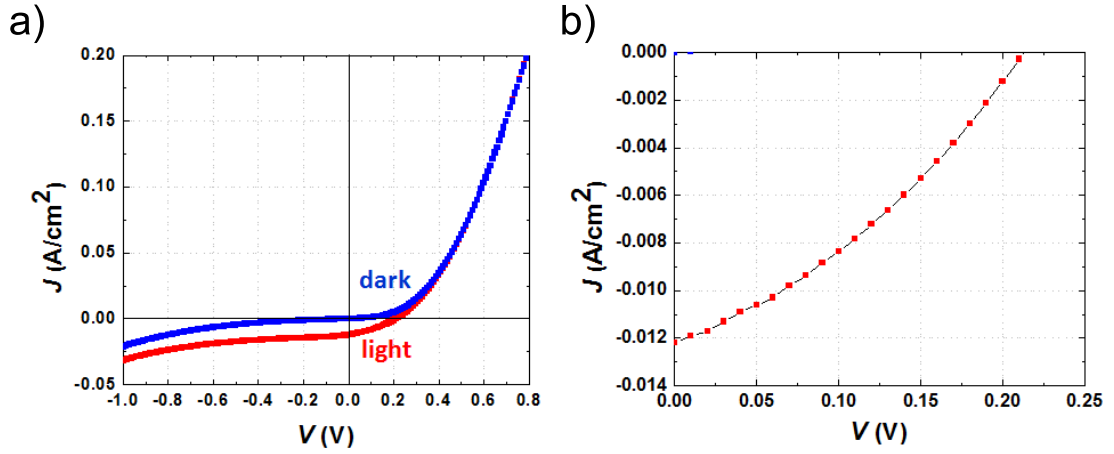
Figure 5.3. Light and dark J-V scans for a VLS-grown, diffusion-doped cell. In this case, the device was ≈ 0.42 cm^2 in area, and exhibited a J_{sc} of ≈ 12 mA/cm^2, V_{oc} of 213 mV, FF of 33 %, and overall efficiency of 0.87 %. Note that this measurement was made with the wires still attached to their growth substrate, so a significant amount of the photoresponse may be from the substrate itself. Fig. (a) shows the light and dark J-V response between -1 and +0.8 V. Fig. (b) is a more detailed look at the light J-V response in forward bias for the same cell.

where n is the diode quality factor. Doing this (not shown) yields $n = 1.81$ for this device. This can then be used, with the same equation, to calculate an effective J_0 - for this device $J_0 \approx 1.3 \times 10^{-4}$ A cm^{-2}.

This is a very high value for dark current density, and also the cells are clearly suffering from shunting (compare the large current density passed in reverse bias in Fig. 5.3 with a cell that is not suffering from shunting as in Fig 5.7). Unfortunately, results to date do not distinguish whether the observed shunting is simply the result of poor contact formation, or something more fundamental related to the VLS catalyst or other impurities shunting the junction. Answering this question would be a key step forward in determining whether Ni- or Cu-catalyzed, VLS-grown Si wires can make a viable absorber material in a PV device.

The wires in this cell had diameters of less than 2 μm. Given that they were grown in a pattern with 7 μm pitch, if the wire pattern were perfect and all the wires grew vertically, in a top-down view the wires would only fill 6.4 % of the plane. The wires are attached to a Si substrate of low enough doping that the substrate itself exhibits a photoresponse (which was necessary in order to avoid having the substrate shunt the entire device. Independent PV measurements of the substrate material were made but are not shown here), but the photoresponse of the substrate is presumably severely degraded by the diffusion of Cu and potentially other metal impurities during the growth, diffusion and drive-in steps. In the limit that J_{sc} can be attributed entirely to the wires, the reason that this is not higher than 12 mA/cm^2 may be due to the relatively low packing fraction of wires in this pattern. One might expect that in that case J_{sc} should be even lower, but recent measurements by M. D. Kelzenberg (unpublished) have shown absorption in wire arrays that is several times higher than one might expect based on their geometric packing fraction alone. Also, the fidelity of this wire array, which was not perfect to begin with, was degraded during cell processing, leaving some wires pointing at angles other than normal to the substrate. If these wires were still in good electrical contact with the substrate, they might potentially benefit from being at an angle relative to the incident light. However, there is clearly a need to deconvolute wire response from the response of the growth substrate, and our group has recently reported on a technique that will allow for the fabrication and testing of substrate-free devices in the future. [119]

Also, if Fig. 5.1 is truly representative of the doping profile throughout the length of the wires, the emitter may be as thick as 400 nm, in a shell around the n-type wire core. In

2 μm diameter wires, this would mean that the wire cores only fill $\approx$ 2.3 % of the top-down area of the plane. Given that the bulk of the photoresponse comes from the wire cores, given the high emitter doping, and presumably large surface recombination, this may be limiting the ability of the device to deliver a large photocurrent. Growing wires with larger diameters and/or more tightly controlled, thinner emitters should improve this. Deposited, rather than diffused emitters, may be useful in order to obtain abrupt junctions where the emitter is not quite so highly doped. Also, amorphous Si emitters may be useful for enhanced surface passivation and to build voltage.

The wires were subjected to extended periods at very high temperatures during cell processing, as described above. On the other hand, the bulk of our TEM, nanoSIMS, and single-wire optical and electrical characterization has been on as-grown wires. It is possible that the extended, high temperature processing is damaging or degrading our wires in unanticipated ways, either because it is somehow damaging the Si crystal lattice itself, or because it is leading to diffusion of additional impurities into the Si. Our group is now looking at in-situ doping (which could be used to dope the core of the wires during growth), as well as rapid thermal processing (which might be used to form an emitter with a far briefer diffusion than is possible in our current, tube furnace setup) to attempt to reduce these potential effects.

It would also be useful to characterize the Si wires after the cell processing has been completed. This could be done with nanoSIMS to see if additional impurity species are present after the processing, as well as to examine whether the pn junctions in the wires are really as we would expect from our SOI analogs. Also useful would be TEM analysis of processed wires, to look for damage to the crystal structure. In order to gain a thorough understanding of our device performance, independent of the difficulties associated with making robust contacts to large-area devices from grown wires, as well as to understand whether the observed shunting is intrinsic to the wires or simply the result of poor contact formation, PV measurements of single, radial pn junction wires could be invaluable. These measurements have recently been conducted by Tian et al. on wires grown from SiH_4 precursors, to great effect. [129]

An additional confounding factor is that these wire array devices, while ostensibly Cu-catalyzed, in fact have likely been affected by significant cross-contamination of metal catalyst types within our APCVD reactor. Until recently we had not taken enough care to

use separate tubes and sample boats for each catalyst type, and therefore it is likely that even in the Cu-catalyzed samples there is a significant amount of Au and Ni present. However, a first attempt at fabrication of cells from Ni-catalyzed wires with our new processing protocol, using separate growth tubes and boats for each catalyst, did not yield improved results (not shown).

Gettering may be useful to reduce the concentration of metallic impurities. Ni and Cu are both extremely diffusive in Si, and in high aspect ratio structures such as wires Au should be able to readily be gettered also. This could be achieved, for example, by performing an extended and controlled cool down in the growth furnace after wire growth, or perhaps by post-growth, post-catalyst-removal thermal oxidation of the wires, followed by an oxide etch. It may be possible for an emitter diffusion step to function also as a metal gettering step.

It will also be important, in the pursuit of high efficiency, to choose the doping type of the wire core on the basis of whether p- or n-type material is more tolerant to impurities of the VLS catalyst metal. P-type Si is apparently more tolerant of Cu and Ni impurities than is n-type. [109] However, the device described above was made with an n-type core. The reason for this is that historically our as-grown wires have been n-type. [55] Recent experiments with more care taken to reduce metal cross-contamination suggests that this n-type doping might be due to Au impurities, and therefore radial pn junction wires with p-type cores and n-type emitters should be revisited.

Finally, no attempt has been made in the above to passivate the surfaces of the wires, and thus the surfaces are likely strong sources of recombination. However, as discussed in Ch. 2, in the radial pn junction geometry the wire cores are shielded from the external surfaces, and it is unlikely that surface recombination alone can be blamed for the relatively poor performance of our devices to date.

Our group has also performed liquid electrolyte PV measurements on Au-catalyzed, VLS-grown Si wire array samples, [120] and V_{oc}s of up to ~ 400 mV have been recorded in this setup. Results with Ni- and Cu-catalyzed VLS-grown Si wire arrays tested in the same setup have to date performed worse than Au-catalyzed samples, surprisingly, but again this could simply be due to unintended Au contamination of these samples. The latter results could also be due to shunting by a surface phase, as no attempt to remove the surface Si was made on the Ni- and Cu-catalyzed samples.

5.4 Previous Fabrication Attempts

Prior to the achieving the results described above, we explored alternative contacting geometries for the fabrication of PV cells from VLS-grown Si wire arrays, as will now be described. While the approach described in Chs. 5.2 - 5.3 nominally used Cu as the VLS catalyst, the approaches to be described in this section involved the use of a Au catalyst for wire growth.

5.4.1 Previous Fabrication Attempts - I

As-grown, our Au-catalyzed Si wires have been found to be n-type. [55] Therefore it should be possible to form radial pn junctions simply by diffusing a p-type shell. We did this using BN wafer diffusion sources (Saint Gobain BN-975) under similar conditions to those described for the emitter diffusion in Ch. 5.2.2 above.

Arrays were then in-filled for structural support of the wires, as well to support a top contact, by using a spin-on glass (SOG). This was done by spin-coating Honeywell T-2027 SOG, at 600 RPM for 2s, then ramping to 1000 RPM for 20 s (with the spincoater's ACL setting at 200). Samples were then cured on a hotplate at 160 °C for 100 s, and then at 180 °C for a further 100 s. Samples were then allowed to cool. This process was repeated as necessary to completely in-fill the wire array. Each spin-coating filled to a depth of 15-20 μm, as determined by SEM.

After curing, the SOG was partially etched back by immersing samples in a heated piranha etch (3:1 H_2SO_4:H_2O_2), at 60 °C for 10 s. The etch rate of piranha solution on planar SOG controls was found to be $\sim$ 50 nm/s, as determined by spectral ellipsometry. For best results it was found that the initial SOG coating should just barely fill the array, and not fully submerge the wires, as the piranha etch was found to be fairly non-uniform across a sample surface, and also to lead to other problems in the SOG film (see below).

After this a transparent, conductive oxide (TCO), such as indium tin oxide (ITO) or indium zinc oxide (IZO), was deposited by magnetron sputtering, to make electrical contact to the tops of the exposed wires (Fig. 5.4). Prior to TCO deposition, samples were be dipped in buffered HF (Transene) to remove native oxide from the Si. ITO could then be deposited as follows (IZO deposition proceeded under similar conditions): Using a 0.125"-thick ITO target of 99.99% purity (Plasmaterials, Inc.), we pumped down the sputtering chamber for
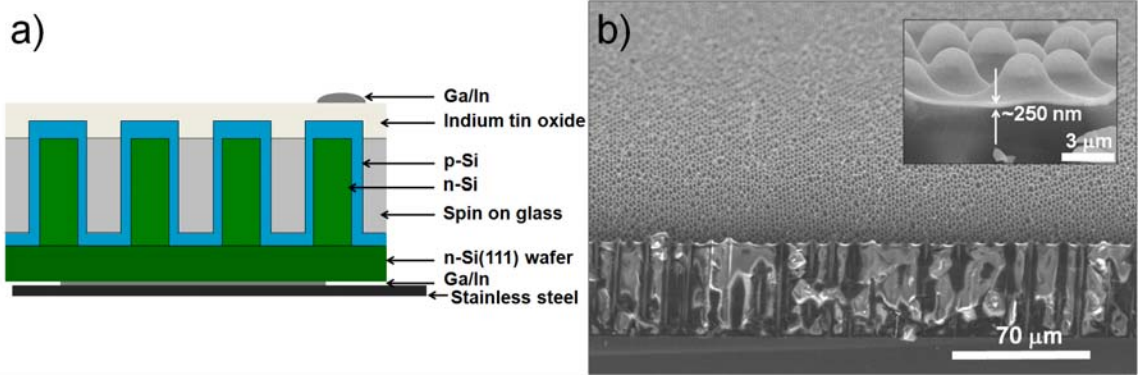
Figure 5.4. (a) Schematic of first attempt at VLS-grown wire cell. (b) SEM image of same, illustrating that in-filling wire arrays with very high-aspect ratios is possible with spin-on glasses (SOGs). (b, inset) Thin, conformal transparent, conductive oxides (TCOs), in this case indium tin oxide (ITO), can then be sputtered to contact the exposed ends of the wires. Results from the characterization of this approach to cell fabrication are presented in Fig. 5.5.

30 mins. Argon was then introduced into the chamber through a needle valve, leading to a chamber deposition pressure of 15 mtorr. The target was burned in for 10 mins at 40 W RF power in the Ar plasma. Deposition then proceeded for 30 mins at 40 W RF, with DC Bias $\approx$ 350 V. Under these conditions the deposited ITO layer was typically $\sim$ 250 nm thick, with a sheet resistance of $\sim$ 90 $\Omega/\square$.

To date we have measured V_{oc}s of up to 290 mV by this approach (Fig. 5.5), but these results are somewhat suspect. Firstly, the device does not display rectifying behavior, and passes approximately equal magnitudes of current density in forward or reverse bias. Secondly, the overall magnitude of current passed is very low (J_{sc} for the device in Fig. 5.5 was $\sim$ 0.15 mA/cm^2, about 100 times less than for the device in Fig. 5.3). Both of these issues make it unclear whether these J-V scans are probing the VLS-grown wires at all.

There were significant problems with the contacting scheme described. Firstly, testing ITO contacts directly on 200 Ω cm, as well as 0.01 Ω cm, p-type Si wafers demonstrated that the ITO contact itself was severely reducing current flow in forward bias (not shown). Secondly, during the piranha etch the SOG cracked (not shown), leading to poor contact between the wires and the TCO. Thirdly, the SOG itself is a significant absorber of light in visible wavelengths (not shown), and even if the cell contacting was robust the SOG itself is likely to reduce cell performance.
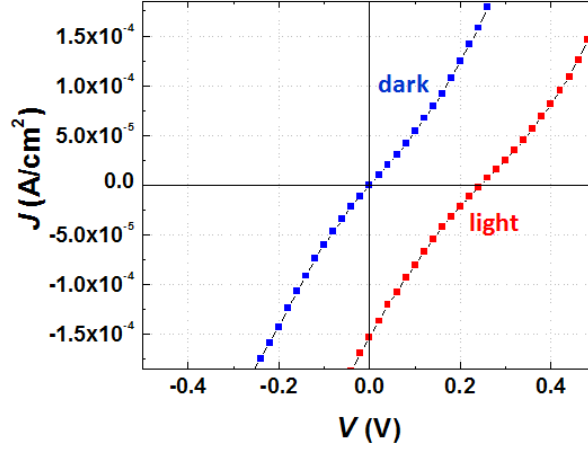
Figure 5.5. Typical result from light and dark J-V scans for our first attempt at a VLS-grown, diffusion-doped cell. This cell shows J_{sc} of ~ 0.15 mA/cm^2, V_{oc} of 245 mV, FF of 22%, and overall efficiency of 0.008%. Note that this measurement was made with the wires still attached to their growth substrate, so a significant amount of the photoresponse may be from the substrate itself.

5.4.2 Previous Fabrication Attempts - II

To avoid some of the issues associated with this first fabrication approach, we then switched to pursue cell designs that do not require the use of SOGs or TCOs. In the first attempt at doing this, we grew wire arrays in photolithographically-defined patches, leaving space for metal contacts so that series resistance in the emitter layer did not become limiting (Fig. 5.6 (b), (c)).

For other electrochemical experiments outside the scope of this thesis it is desirable for us to fabricate p-type Si wire arrays. Thus, this attempt at a large-area, solid-state radial pn junction solar cell measurement involved compensating our as-grown, Au-catalyzed wire arrays p-type, followed by the formation of an n-type shell. This followed an analogous procedure to that described in Ch. 5.2.2. The differences were that the initial diffusion was a p-type diffusion (using Saint Gobain BN-975 planar diffusion sources), at 850 °C for 40 mins, the drive step was only 5 hours long (at 1100 °C), and the emitter diffusion was an n-type diffusion (using Saint Gobain PH-950 wafers), at 850 °C for 60 mins.

Finally, metal contacts were thermally evaporated on the front and back sides (with
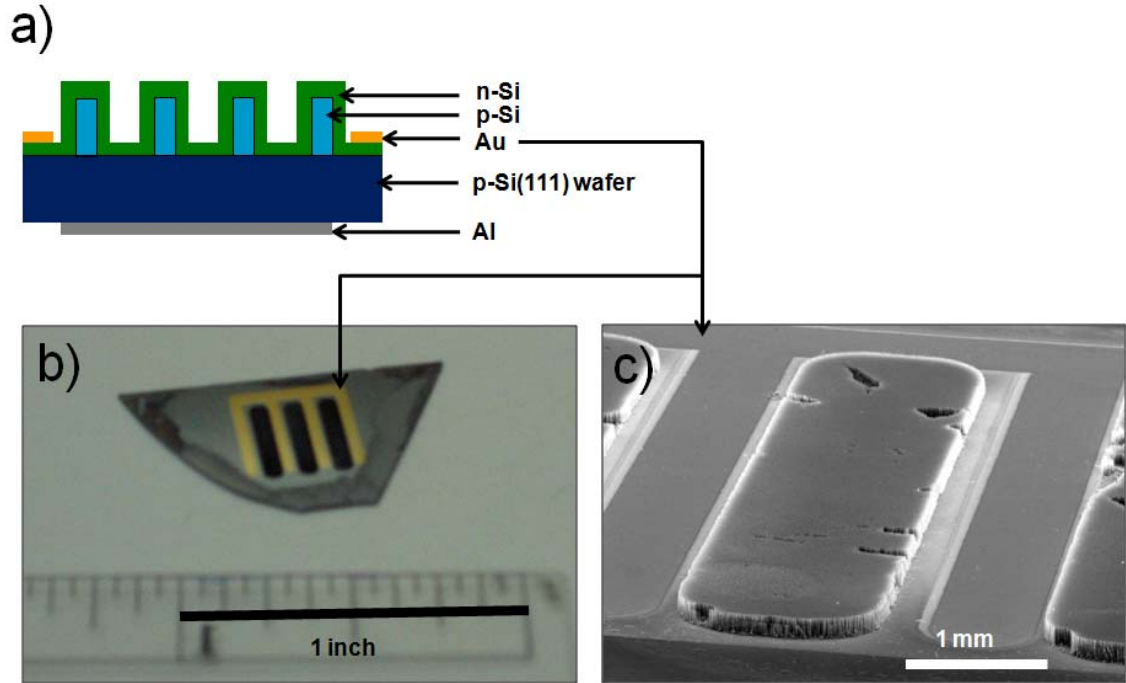
Figure 5.6. (a) Schematic of second attempt at VLS-grown wire cell. (b) Optical photograph of a finished device, showing dark patches of Si wires with radial pn junctions, and Au contact "fingers". (c) SEM image of the same showing one wire patch surrounded by a Au contact. It is evident that the wires are quite robust to the repetitive and aggressive chemical and thermal processing that is required to fabricate such a device.

metals, Au for the n-type contact and Al for the p-type contact, chosen such that low-resistance ohmic contact could be made to Si of the appropriate doping, as determined by planar controls (not shown)), which was sometimes followed by annealing under forming gas at up to 400 °C for up to 30 mins (Fig. 5.6).

Electrical characterization of these devices (not shown) not only exhibited a lack of diodic properties, in this case there was no photoresponse whatsoever. There may be many reasons for this. The initial diffusion step was likely too hot - 4 point electrical measurements of planar controls implied that p-type dopant densities of $\sim 10^{18}$ cm^{-3} may be present in the wires, given initial diffusions as described above, if the dopants were fully driven in. Also, the drive step was likely too short, leading to non-uniform dopant profiles within the wires and/or inadequate compensation of the as-grown n-type dopant species. Thirdly, the emitter diffusion may have benefited from being hotter - 4 point electrical measurements of

planar controls showed that the n-type emitter diffusion as described above leads to sheet resistances of $\sim 108 \ \Omega/\square$.

There was also a significant and unexpected difficulty introduced by limiting the catalyst placement to relatively small areas of the growth substrate. At the edges of the samples, conformal (uncatalyzed) deposition of rough Si films occurred, apparently on top of the oxide barrier layer. This could potentially lead to shunting of the device if the metal contacts on the top surface of the device were also contacting the uncatalyzed Si layer at any point, and if the uncatalyzed Si layer extended to the back side of the sample (which appeared to be the case in some instances).

An improved method that should produce homogeneously p-type wires with dopant densities on the order of 10^{17} cm^{-3} is as follows. The basic procedure is described in Ch. 5.2.2. However, to make p-type wires, the initial diffusion should be a p-type diffusion (using Saint Gobain BN-975 planar diffusion sources), at 800 °C for 40 mins. Then the drive step should be at least 10 hours long (at 1100 °C). This may be useful for related work on using wire arrays for water splitting, for example. [130]

5.5 Fabrication of a Device Using Reactive Ion Etching

To date, efforts to fabricate solid-state PV devices from Cu-catalyzed wire arrays have suffered from fabrication difficulties as outlined in the previous section, primarily associated with shunting. In order to more easily fabricate devices, as well as to probe the geometrical effects associated with this device design free from the convoluting effects of catalyst incorporation, we have also pursued reacive ion etching (RIE) [131] as a means to fabricate analogous wire arrays.

RIE was performed by M. D. Henry. N-type, P-doped Si(100) wafers of 2 - 8 Ω cm resistivity were first cleaned in acetone, isopropanol, and methanol, followed by a deionized (18 MΩ cm) (DI) H$_2$O rinse. Wafers were then soaked in buffered HF acid for 2 mins and then dried in an oven at 125 °C for 10 mins. Samples were spin-coated with AZ-5214E photoresist at 6000 RPM, baked at 95 °C, and patterned photolithographically, followed by another 95 °C bake. These patterned samples were then introduced to a plasma-enhanced chemical vapor deposition (PECVD) chamber for deposition of an SiO$_2$ etch mask. The oxide was deposited at a temperature T = 135 °C for 9 - 10 mins at a SiH$_4$ flow rate of

450 sccm, N_2O flow rate of 750 sccm, a total pressure P of 1 Torr, and an RF power of 15 W, leading to an SiO_2 deposition rate of 65 nm/min. Si etching was then performed using a SF_6 etchant. This was done at T = -110 °C, SF_6 flow rate of 70 sccm, O_2 flow rate of 6 sccm, and P = 10 mTorr. The inductively coupled plasma (ICP) power was 900 W at 56 MHz, with a forward power of 8 W, leading to an etch rate of 1.9-2.0 μm/min. The etching was done in 15 min increments with 10 min pumpdown in between, in order to prevent trapping of the etchant gas and/or reaction products within the bottoms of the etched structures.

In this way, wire arrays of a fixed packing fraction of 22.7% were fabricated. Four different wire diameters, 5 μm, 10 μm, 20 μm, and 50 μm, were considered, with pitch equal to twice the wire diameter, in a close-packed hexagonal arrangement. After array fabrication, samples were etched for 1 hour in piranha solution (3:1 H_2SO_4:H_2O_2 by volume) at room temperature, in order to remove bonding grease used for sample mounting in the RIE process. Any oxide was then removed in buffered HF. Samples were then oxidized at 850 °C for 1.5 hours in N_2 bubbled through near-boiling, H_2O at 3 lpm flow rate. Oxide on the front (device) surface was then removed with buffered HF. Samples were then annealed at 400 °C for 30 mins, under forming gas (5% H_2 in N_2) at 5 lpm. The front surface of the samples were then doped p-type by stacking parallel to BN diffusion wafers (BN-975, Saint-Gobain Ceramics), introducing to a tube furnace at 750 °C, ramping up to 950 °C, holding at 950 °C for 40 mins, and then ramping back down, all under N_2 at 5 lpm. The front surface was then exposed to buffered HF for 2 mins. This was followed by a low temperature oxidation at 750 °C for 20 mins, under O_2 at 5 lpm. Finally, oxide was removed from the entirety of the samples with buffered HF, and contact was made to the back surface by immediately rubbing Ga/In onto the back of the sample and the sample then bonded with Ag paste to a piece of stainless steel to which electrical contact could be made with a probe tip. Contact was made to the front surface with a spot of Ga/In and an electrical probe tip.
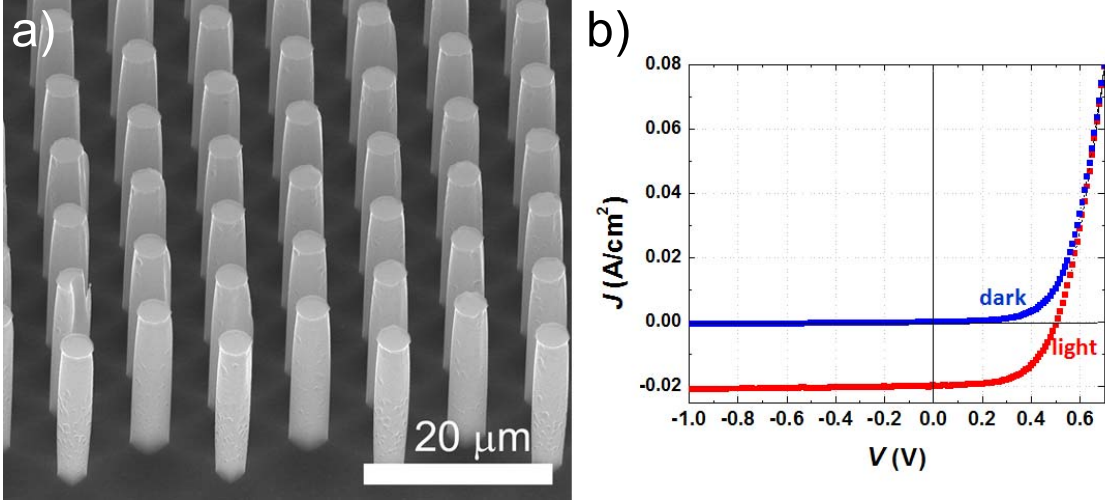
Figure 5.7. RIE-fabricated Si wire array PV cell. Fig. (a) shows an SEM image of a cell with 5-μm-diameter wires, and Fig. (b) shows the light (under AM1.5D sunlight at 1 sun intensity) and dark J-V response of the cell.

5.6   Characterization of Devices from Reactive Ion Etched Samples

Samples were then tested in the light (under AM1.5D sunlight at 1 sun intensity, as calibrated with a BP Solar reference cell) and in the dark. This results in excitation of the wire array as well as the underlying Si and the adjoining planar regions. In the best device, with 50 μm diameter wires, we observed an efficiency of 6.7%, with $V_{oc} = 537$ mV, $J_{sc} = 18.8$ mA/cm^2, and $FF = 66.1\%$ (not shown). For this sample, the total cell area was 22.9 mm^2 with a wire array area of 4 mm^2. In all cases, J_{sc} was calculated by normalizing to the total cell area. Even in the case of relatively small wires of 5 μm diameter, occupying a larger fraction of the sample (total cell area 12.9 mm^2, wire array area 4 mm^2), we saw an efficiency of 5.7%, with $V_{oc} = 507$ mV, $J_{sc} = 19.7$ mA/cm^2, and $FF = 57.7\%$ (Fig. 5.7).

The need to make contacts to the planar Si surrounding the wire arrays, and the fact that this planar Si is also photoactive, limited our ability to increase the junction area to only a factor of ~ 4. Nevertheless, initial results indicate a loss of V_{oc} of approximately 61 mV per factor of ten increase in junction area (Fig. 5.8), as well as a decrease in fill factor (FF) as junction area increases. As discussed in Ch. 2 (see also [49]), we expect that V_{oc} should drop by ~ 59 mV per factor of 10 increase in junction area, at 25 °C, for ideal ($n =$

a)

b)

$V_{oc} = 541 - 61.2 \; (J.A.E.)$
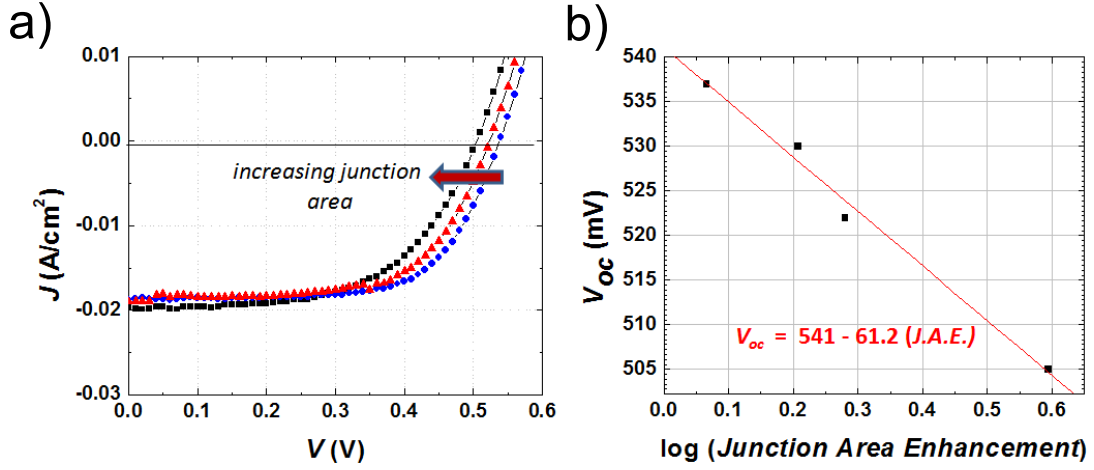
Figure 5.8. V_{oc} vs. junction area for solid-state PV cells made from RIE-fabricated Si wire arrays. Fig. (a) shows J-V curves for three cells of varying wire diameter, and therefore junction area. Fig. (b) plots the measured V_{oc} vs. the log of the pn junction area enhancement relative to a planar cell, for four cells of differing wire diameter, and therefore junction area.

1) diodes in the case that quasineutral region recombination is the dominant recombination mechanism, and that moderate or high efficiency devices should be possible in the radial pn junction geometry if we are in this recombination regime. [1]

Our RIE PV cell results are therefore important in that they support the notion that in high-enough quality Si, the recombination can be quasineutral-region-recombination-dominated, even in the radial pn junction geometry. Therefore there we expect that there is no fundamental, geometrical limitation to attaining moderate to high efficiencies in this geometry. In the quasineutral-region-recombination-dominated regime, losses in V_{oc} associated with purely geometrical effects in the radial pn junction design should be tolerable in the pursuit of efficient devices, which is consistent with other reports on analogous struc-

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[1]Performing V_{oc} / J_{sc} analyses, as in Ch. 5.3, indicates that these diodes are not in fact ideal, but that n ranges from ≈ 1.4 to ≈ 2, appearing to increase as wire radius decreases. However, these measurements were not made until several months after the original J-V curves were measured, and appeared to suffer greatly from series resistance in forward bias (not shown. Large series resistance was not observed when the cells were initially tested). This may be due to oxidation of the wires surfaces, and/or degradation of the Ga/In contact over time. Therefore it is not clear whether these measured diode ideality factors correspond to what the diode ideality factors were at the time the original J-V curves were measured.
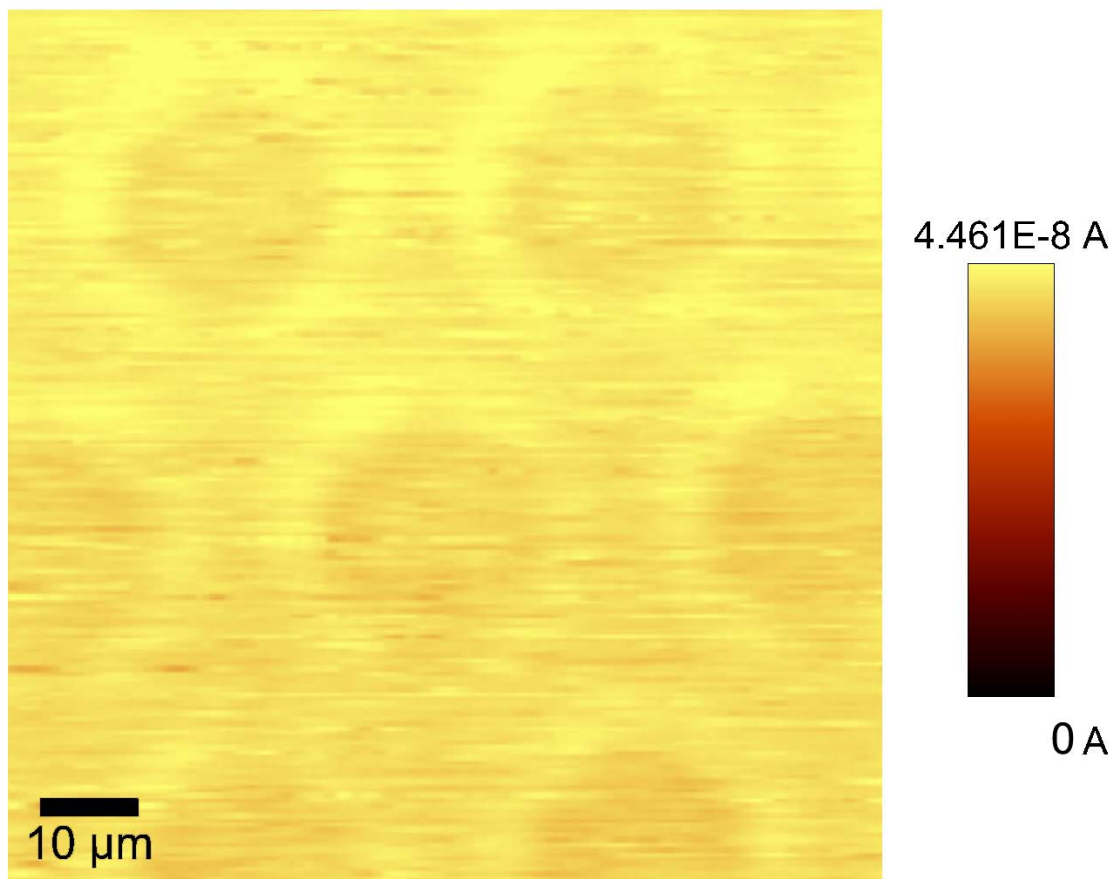
Figure 5.9. Scanning photocurrent map (SPCM) of RIE-fabricated wire array, showing current measured as a function of laser excitation position. The sample was held at a zero bias on both sides of the pn junction.

tures. [132] [133] [134] [135]

To verify that the RIE-fabricated wires were indeed contributing photocurrent to the device, we performed scanning photocurrent measurements using an excitation wavelength of 650 nm (which has an absorption depth $1/\alpha$ of ≈ 3 μm in Si), which showed that comparable photocurrent was generated in the wires and in the planar substrate (Fig. 5.9). This is important because it demonstrates that our RIE experiments were indeed probing an increase in active pn junction area, and it demonstrates that RIE followed by a surface cleaning (as outlined above) does not significantly degrade the Si, and therefore that RIE can be a useful tool for probing the utility of novel geometries in PV devices.

5.7 Conclusion

PV device measurements on VLS-grown wire arrays to date exhibit a large degree of shunting, and have been limited to a V_{oc} of 213 mV, and overall efficiency of 0.87%. It is not clear yet whether the observed shunting is simply the result of poor contact formation, or something more fundamental related to the VLS catalyst or other impurities shunting the junction. Answering this question would be a key step forward in determining whether Ni- or Cu-catalyzed, VLS-grown Si wires can make a viable absorber material in a PV device.

In addition to exploring fabrication and testing of cells based on arrays of VLS-grown wires, we have explored the use of RIE to fabricate morphologically similar structures. This allows us to investigate any purely geometrical limitations to the radial pn junction geometry, free from issues related to material quality in grown wires, and difficulties associated with making devices from grown wires. With these cells we observe a loss in V_{oc} of 61 mV per decade increase in junction area. This supports the notion that losses in V_{oc} associated with purely geometrical effects in the radial pn junction design should be tolerable in the pursuit of efficient devices.

Future efforts should target reduced shunting in the characterization of devices wherein the Si absorber layer has been grown by VLS using Cu or Ni as the growth catalyst. This should be coupled with independent experiments to determine the quality of the Cu- and Ni-catalyzed VLS-grown material. In addition to this, it will be important to pursue substrate-free device measurements, for example by exploiting a technique we have developed for embedding wire arrays in a polymer and removing them from their growth substrates. [119]

Chapter 6

Outlook

6.1 Towards a Solid-State, Flexible, Single-Crystalline Si PV Device

The radial pn junction, Si wire array cell is a compelling, novel approach to thin-film Si PV device design. The design is compelling less for its original intent to provide for moderate efficiency PV devices in material of arbitrarily low quality (for, as discussed in Ch. 2, depletion region effects begin to dominate when material quality becomes sufficiently poor), but rather for its potential to combine high-throughput, low-cost processing with the ability to generate single-crystalline Si device material. As discussed in Ch. 1, the Si precursor $SiCl_4$ is perhaps the cheapest source of high-purity Si currently available, and far cheaper per Si atom than Si wafers. Growth catalysts Cu and Ni are similarly abundant and inexpensive, and we have shown that using these catalysts the VLS growth method can produce single-crystalline Si at growth rates of many µm/min in well-controlled structures over potentially very large areas. Si is a very well understood PV material, and in principle all post-material-growth device processing can follow well established routes to doping and contacting.

Assuming that moderate-quality Si (which in this context means minority-carrier lifetimes of $\gtrsim 100$ ns, and mobilities equal to or close to those found in single-crystalline Si) can be confirmed in Si wires grown by the VLS technique with Cu and/or Ni catalysts, we believe that the path forward to making a manufacturable PV device lies in array "peel off" and subsequent re-use of the Si(111) growth substrate. Our group has recently demonstrated the infiltration of VLS-grown Si wire arrays with polymers such as polydimethylsiloxane (PDMS) and ethylene vinyl acetate (EVA), and the subsequent "peeling off" of the entire wire array, with the ability to leave both ends of the wires uncovered by the polymer. [119] This provides one with a substrate-free Si wire array, suitable for further experimentation

in order to study the properties of the grown wires without convolution with the properties of the growth substrate and/or the fabrication of substrate-free Si wire array devices, and a wire-free Si(111) handle, suitable for the growth of more wire arrays after a small amount of wet chemical processing to remove any remaining Si "stumps". Our group has also shown that the latter is possible, with the demonstration of the retention of a high degree of pattern fidelity after up to three substrate reuses. [136] There is a limit to how many times this can be repeated, as the oxide mask becomes increasingly defective with each re-use. However, by polishing back the wafer and re-oxidizing, the patterning process can be begun again. The latter study estimates that, in an optimized process, up to ~ 1000 wire arrays might be grown from a single Si(111) wafer, which in terms of a manufacturing process renders the cost of the high-quality growth substrate nearly insignificant.

One can then imagine growing wire arrays with an in-situ dopant, removing the metal catalyst particles and doping a thin emitter region into the wires, and then peeling off the arrays and contacting them to form substrate-free, flexible PV devices based on single-crystalline Si absorber material. This could potentially be of huge interest to the PV industry, as it has the potential to marry the best of thin film processing with the performance advantages of optically-thick, single-crystalline Si.

6.2   Other Applications of Si Wire Arrays

Outside of PV, there are many other exciting potential applications of Si wire arrays:

1. Si wire arrays as thermoelectric materials

   As described in [137] and [138], Si nanowires can make very efficient thermoelectric materials. If one could fabricate large arrays of vertically-aligned Si nanowires of the appropriate dimensions and with the appropriate surface morphology, one could imagine the possibility of large-area, efficient thermoelectrics based on this novel geometry.

2. Si wire arrays for enhanced catalysis

   As described in [139], catalysis, in particular the evolution of hydrogen at an electrode, is limited by maximum exchange current density of the catalyst material. One can imagine exploiting novel geometries with increased surface area relative to a planar electrode, such as afforded in a wire array geometry, in order to decrease the

current load on the catalyst metal. This may allow for less-efficient but cheaper and more abundant catalysts, such as Ni, to attain the high catalytic efficiencies currently reserved for the more commonly used Pt. In thinking about designing an efficient solar-powered water-splitting device utilizing low-cost catalyst material, [130] one can envision that Si nanowire arrays, decorated with Ni nanoparticles or coated conformally by a Ni thin film, are a potential way of realizing high photoelectrolytic efficiencies with low-cost materials.

3. Si wire arrays for enhanced Li-ion batteries

As described in [140], Li-ion batteries can maintain much higher potential energies when incorporating Si nanowires as the anode material. This is because, although Si has a high theoretical charge capacity, the Li ions tend to swell the anode material as they are incorporated into it, making bulk Si unsuitable for the task. Si nanowires grown over large areas but with little control have been successfully demonstrated in the aforementioned publication, but well-controlled nanowire arrays may prove even more beneficial, if one can optimize and control wire diameter, length, and packing density for this application.

4. Si wire arrays for enhanced Raman Spectroscopy

Si nanowires in close proximity to metals with plasmonic properties may be useful in the fabrication of novel plasmonic devices. Si wire arrays in particular may be useful for the realization of improved surface-enhanced Raman spectroscopy (SERS). This has been demonstrated at the single-wire level, exploiting a core-shell Si-metal geometry with VLS-grown wires and a Ag shell, SERS [141] as well as by using the Au VLS tip directly. [142] [143]

6.3   Conclusion

In this thesis, we have explored the ability of radial pn junctions to enable PV devices to maintain high efficiencies despite low minority-carrier lifetimes. In Ch. 2, it was found theoretically that there is a window of minority-carrier lifetimes over which the radial pn junction exhibits potential benefits relative to a planar geometry. It was found that for isotropic materials, losses in voltage become prohibitively high when depletion region recombination

dominates, and that therefore the radial pn junction geometry cannot ameliorate the effects of low diffusion lengths to an arbitrary degree, and that even within the window of material qualities over which we see improved performance the benefits of the radial pn junction geometry are relatively small (efficiency increases of up to $\sim$ a few % absolute). In the case of Si it was predicted that minority carrier lifetimes of > 40 ns will be required to avoid having depletion region recombination be the dominant recombination mechanism, which we predict will be required in the pursuit of moderate-to-high efficiency PV devices.

In Ch. 3 we explored the use of SiH_4 and the vapor-liquid-solid (VLS) process to fabricate Si nano- and microwires. We discussed key considerations when choosing a VLS growth catalyst, and demonstrated successful growth with Au and In catalysts. We also demonstrated a proof of principle approach to controlling wire position, by electron beam lithography followed by wet etching of an oxide layer.

In Ch. 4 we demonstrated a route to the fabrication of Si wire arrays over large areas (> 1 cm^2) with a high degree of control over wire diameter (albeit in the > 1 μm range) and pitch. This was done in an atmospheric-pressure tube furnace at high temperatures (~ 1000 °C), using a $SiCl_4$ precursor, and low-cost catalysts such as Cu or Ni, as well as the more commonly used Au, by the vapor-liquid-solid (VLS) growth technique. We extended the templating technique introduced in Ch. 3 to photolithography to allow for wires of microscopic diameters to be grown in arrays over macroscopic dimensions. The resulting wires where single-crystalline, and grew in the [111] direction. Wire length could be controlled simply by changing the deposition time, and aspect ratios well over 100 have been demonstrated.

In Ch. 5 we presented an initial exploration of the use of VLS-grown Si wire arrays in solid-state PV devices. So far our cells exhibit a large degree of shunting, and results to date do not distinguish whether this is simply the result of poor contact formation, or something more fundamental related to the VLS catalyst or other impurities shunting the junction. An additional confounding factor is potentially significant cross-contamination of metal catalyst types within our wire growth reactor. If large amounts of Au were present during growth this could also significantly impair device performance. We also presented the results of using reactive ion etching (RIE) to fabricate wire arrays from high-quality Si. This allowed us to investigate any purely geometrical limitations to the radial pn junction geometry, free from issues related to material quality in grown wires, and difficulties associated with making

devices from grown wires. These results support the notion that losses in voltage associated with purely geometrical effects in the radial pn junction design should be tolerable in the pursuit of efficient devices.

In conclusion, the demonstration of a rapid, potentially low-cost method of depositing single-crystalline Si that can then be embedded in a flexible substrate, removed from the growth substrate and the growth substrate reused, represents a potentially very interesting approach to reducing the cost per kilowatt-hour associated with materials in PV cells. Future work should seek to confirm the quality of the VLS-grown material, as well as the fabrication and testing of substrate-free PV devices.

Appendix A

MatLab Simulation Code

A.1 Radial pn Junction Simulation

This is the radial pn junction simulation code:

```
clear all
format short g
warning off MATLAB:fzero:UndeterminedSyntax
warning off MATLAB:divideByZero


load silicon_E_flux_alpha %silicon_E_flux_alpha.mat contains the vectors
flux, which is the solar flux in photons cm^-2 s^-1 eV^-1, and alpha, which is
the absorption coefficient of Si in cm^-1, as functions of the vector E,
which is an energy vector in eV
n=length(E)-1;
dE=(E(2:(n+1))-E(1:n));
alpha2=alpha(2:(n+1));
alpha1=alpha2; %alpha1 and alpha2 are the absorption coefficients of the n-
and p-type materials, respectively
gammaA=flux(2:(n+1));
gammaC=gammaA; %gammaA and gammaA are the photon fluxes incident on the top
of the n- and p-type quasineutral regions, respectively
matrix=[];


lengths=[1e-4,2e-4,5e-4,1e-3,2e-3,5e-3,1e-2,2e-2,5e-2,1e-1]; %lengths is a
vector containing the various cell thicknesses that will be considered, in cm
```

```
thing=length(lengths);


%dope=[1,10,1e2,1e3,1e4,1e5,1e6,1e7,1e8]*5e12;
%muele=[1500,1500,1500,1500,1000,400,150,100,100];
%muhol=[500,500,500,400,300,150,60,50,50]; %these lines indicate the maximum
electron and hole mobilities possible in Si at various doping levels, as
given by [52], for reference


%max Na = [>1e20, >1e20, 9e19, 4e19, 2e19, 9e18, 4e18, 2e18, 8e17, 3e17]
%vs Ln = [1e-5, 2e-5, 5e-5, 1e-4, 2e-4, 5e-4, 1e-3, 2e-3, 5e-3, 1e-2]
% => mun= [95, 95, 95, 100, 110, 130, 160, 195, 300, 540] %these lines
indicate the maximum electron diffusion length possible in Si at various
doping levels, as given by [53], for reference


%Define constants


q=1.60219e-19;
kB=1.3807e-23;
T=300;


%Silicon data
%Eg=1.12;
Nc=2.8e19;
Nv=1.04e19;
ni=1.4e10;


dopants=1e18;
Na=dopants;
mun=270;
Nd=dopants;
mup=95;
```

```
Dn=kB*T/q*mun;

Dp=kB*T/q*mup;


Sn=1e5;


sigman=1e-15;

sigmap=sigman;

vth=1e7;


if ni^2>=Na*Nd

    break

end


np0=ni^2/Na;

pn0=ni^2/Nd;

Vbi=kB*T/q*log(Na*Nd/ni^2);

epsilon0=8.85418e-14;

epsilonn=11.9*epsilon0; epsilonp=epsilonn; epsilons=epsilonn;


R=[1e-5,2e-5,5e-5,1e-4,2e-4,5e-4,1e-3,2e-3,5e-3,1e-2]; %R is a vector

containing the various cell radii that will be considered, in cm

N=length(R);

count=1:N;


for thingee=1:thing


   L=lengths(thingee)*ones(1,N);

   aspectratio=L./R;


   V=linspace(0,95/100*Vbi); %the program assumes that Voc < 0.95 Vbi

   NN=length(V);
```

```
x1=zeros(NN,N);

x2=zeros(NN,N);

x3=zeros(NN,N);

x4=zeros(NN,N);

J0A=zeros(NN,N);

J0C=zeros(NN,N);

J0=zeros(NN,N);

JlAperE=zeros(n,N,NN);

JlCperE=zeros(n,N,NN);

JlA=zeros(NN,N);

JlC=zeros(NN,N);

Jl=zeros(NN,N);

Jrdep=zeros(NN,N);

JdepAperE=zeros(n,N,NN);

JdepCperE=zeros(n,N,NN);

JdepA=zeros(NN,N);

JdepC=zeros(NN,N);

Jgdep=zeros(NN,N);

J=zeros(NN,N);

bias=zeros(NN,N);

VBI=zeros(NN,N);

Voc=zeros(1,N);

Jsc=zeros(1,N);

A1A=zeros(NN,N);

A1C=zeros(NN,N);

A2A=zeros(NN,N);

A2C=zeros(NN,N);

B1A=zeros(NN,N);

B2A=zeros(NN,N);


for i=1:N
```

```
disp(round(((thingee-1)/thing+i/(thing*N))*100)) %a counter, so that
the user doesn't think the program has crashed
for ii=1:NN


    Ln=R(i); %setting radius = minority electron diffusion length


    Nr=Dn/(Ln^2*sigman*vth);
    taun0=1/(sigman*Nr*vth);
    taup0=1/(sigmap*Nr*vth);
    taun=taun0;taup=taup0;
    %taun0=1e-6; taup0=taun0; %activate this line to set the depletion
    region minority electron lifetime τ_{n0} separately from the
    quasineutral region minority electron lifetime τ_n (similarly for
    holes)
    Lp=sqrt(taup*Dp);
    windowwidth=1e-6; %minimum emitter thickness, in cm


    bias(ii,i)=V(ii);
    [x1(ii,i),x2(ii,i),x3(ii,i),x4(ii,i),VBI(ii,i)]=depletionregion...
        (Nd,Na,R(i),epsilonp,epsilonn,ni,bias(ii,i),windowwidth);


    if bias(ii,i)>VBI(1,i)
        break
    end
    d1(ii,i)=x1(ii,i)+x2(ii,i);
    d2(ii,i)=x3(ii,i)+x4(ii,i);


%define dimensionless variables
    beta1(ii,i)=R(i)/Lp;
    beta2(ii,i)=(R(i)-x1(ii,i))/Lp;
    beta3=alpha1*L(i);
    beta4=Lp*Sn/Dp;
```

```
beta5(ii,i)=x4(ii,i)/Ln;

beta6=alpha2*L(i);

f1(ii,i)=besseli(1,beta1(ii,i))+beta4*besseli(0,beta1(ii,i));

f2(ii,i)=besselk(1,beta1(ii,i))-beta4*besselk(0,beta1(ii,i));


JlnperE(:,i,ii)=-2*q*gammaA*beta2(ii,i)/(beta1(ii,i))^2*...
   (-besseli(1,beta2(ii,i))*(f2(ii,i)+beta4*...
   besselk(0,beta2(ii,i)))+besselk(1,beta2(ii,i))*(f1(ii,i)-...
   beta4*besseli(0,beta2(ii,i))))/(f1(ii,i)*...
   besselk(0,beta2(ii,i))+f2(ii,i)*besseli(0,beta2(ii,i))).*
   (1-exp(-beta3)).*dE;
Jln(ii,i)=sum(JlnperE(:,i,ii));
J0n(ii,i)=2*L(i)*q*pn0/taup*beta2(ii,i)/(beta1(ii,i))^2*...
   (f2(ii,i)*besseli(1,beta2(ii,i))-f1(ii,i)*...
   besselk(1,beta2(ii,i)))/(f1(ii,i)*besselk(0,beta2(ii,i))+...
   f2(ii,i)*besseli(0,beta2(ii,i)));
JlpperE(:,i,ii)=2*q*gammaC*Ln^2/Lp^2*beta5(ii,i)/...
   (beta1(ii,i))^2*besseli(1,beta5(ii,i))/...
   besseli(0,beta5(ii,i)).*(1-exp(-beta6)).*dE;
Jlp(ii,i)=sum(JlpperE(:,i,ii));
Jlp(ii,i)=-Jlp(ii,i);
J0p(ii,i)=-2*L(i)*q*np0*Dn/Lp^2*beta5(ii,i)/(beta1(ii,i))^2*...
   besseli(1,beta5(ii,i))/besseli(0,beta5(ii,i));
JgdepnperE(:,i,ii)=-q*gammaA*((d2(ii,i)+x2(ii,i))^2-...
   (d2(ii,i))^2)/(R(i))^2.*(1-exp(-beta3)).*dE;
Jgdepn(ii,i)=sum(JgdepnperE(:,i,ii));
JgdeppperE(:,i,ii)=-q*gammaC*((d2(ii,i))^2-(x4(ii,i))^2)/...
   (R(i))^2.*(1-exp(-beta6)).*dE;
Jgdepp(ii,i)=sum(JgdeppperE(:,i,ii));


U(ii,i)=1/2*ni/sqrt(taun0*taup0)*2*sinh(q*bias(ii,i)/(2*kB*T));
kappa(ii,i)=pi*kB*T/(q*(VBI(ii,i)-bias(ii,i)));
```

```
        r(ii,i)=x4(ii,i)+(log(Na/ni))/(log(Nd/ni)+log(Na/ni))*(x2(ii,i)+...
            x3(ii,i));
        r2(ii,i)=r(ii,i)+(x2(ii,i)+x3(ii,i))*1/2*kappa(ii,i);
        r1(ii,i)=r(ii,i)-(x2(ii,i)+x3(ii,i))*1/2*kappa(ii,i);


        Jrdep(ii,i)=-q*L(i)*U(ii,i)*(r2(ii,i)^2-r1(ii,i)^2)/(R(i))^2;


    end
end

Jgdep=Jgdepn+Jgdepn;
Jgdep=[Jgdep;zeros(NN-length(Jgdep),N)];
Jl=Jln+Jlp;
Jl=[Jl;zeros(NN-length(Jl),N)];
J0=J0n+J0p;
J0=[J0;zeros(NN-length(J0),N)];
J=(J0.*(exp(q*bias/(kB*T))-1)-Jl-Jgdep+Jrdep);
temp=[J(1,:);zeros(NN-1,N)];
J(bias==0)=0;
J=J+temp;

P=J.*bias;
P(P<0)=0;

[maxP,posn]=max(P);
eff=maxP/(.1)*100;
Jsc=J(1,:);
b=sum(J>0);
for j=1:N;
    if b(j)~=0
        if b(j)==100
```

```
            Voc(j)=0;

        elseif bias(b(j)+1,j)==0

            Voc(j)=0;

        else

            Voc(j)=(bias(b(j),j)+bias(b(j)+1,j))/2;

        end

    else

        Voc(j)=0;

    end

end

ff=maxP./(Voc.*Jsc);


arshort=aspectratio(ff<0.9999&ff>0);

Lshort=L(ff<0.9999&ff>0);

Rshort=R(ff<0.9999&ff>0);

Vocshort=Voc(ff<0.9999&ff>0);

Jscshort=Jsc(ff<0.9999&ff>0);

ffshort=ff(ff<0.9999&ff>0);

effshort=eff(ff<0.9999&ff>0);


%disp(' Aspect Ratio L (cm) R (cm) Jsc (A/cm^2) Voc (V) ff Efficiency...
    (%)')

%disp([aspectratio', L',R',Jsc', Voc', ff', eff'])

matrix=[matrix; arshort', Lshort',Rshort',effshort', Jscshort',...
    Vocshort', ffshort'];


end


t1=num2str(Lp,4);

t2=num2str(Ln,4);

t3=num2str(Sn,4);

t6=num2str(mup,4);
```

```
t7=num2str(mun,4);

t8=num2str(Na,4);

t9=num2str(Nd,4);

t10=num2str(windowwidth,4);

t11=num2str(taun0,4);

t12=num2str(taup0,4);


name=sprintf('Radial_Silicon matrix Ln=%s, Lp=%s, Sn=%s, taun0=%s, taup0=...
   %s, Na=%s, Nd=%s, window_width=%s.txt', t2,t1,t3,t11,t12,t8,t9,t10);
save(name,'matrix','-ASCII','-TABS')


Rmin=min(matrix(:,3));

Rmax=max(matrix(:,3));

R=R((R>=Rmin)&(R<=Rmax));

nR=length(R);

Lmin=min(matrix(:,2));

Lmax=max(matrix(:,2));

L=lengths((lengths>=Lmin)&(lengths<=Lmax));

nL=length(L);

index=cumsum(ones(1,nR));

for i=1:nL
   temp=matrix(matrix(:,2)==L(i),4);

   temp=temp';

   tempJsc=matrix(matrix(:,2)==L(i),5);

   tempJsc=tempJsc';

   tempVoc=matrix(matrix(:,2)==L(i),6);

   tempVoc=tempVoc';

   tempff=matrix(matrix(:,2)==L(i),7);

   tempff=tempff';

   posR=(min(matrix(matrix(:,2)==L(i),3))==R)*index';

   matrix2(i,:)=[zeros(1,posR-1),temp,zeros(1,nR-length(temp)-posR+1)];

   matrixJsc(i,:)=[zeros(1,posR-1),tempJsc,zeros(1,nR-length(tempJsc)-...
```

```
      posR+1)];
    matrixVoc(i,:)=[zeros(1,posR-1),tempVoc,zeros(1,nR-length(tempVoc)-...
      posR+1)];
    matrixff(i,:)=[zeros(1,posR-1),tempff,zeros(1,nR-length(tempff)-posR+1)];
end
matrix2=[L',matrix2];
matrix2=[0,R;matrix2];
matrix2(:,2);
matrixJsc=[L',matrixJsc];
matrixJsc=[0,R;matrixJsc];
matrixVoc=[L',matrixVoc];
matrixVoc=[0,R;matrixVoc];
matrixff=[L',matrixff];
matrixff=[0,R;matrixff];


matrix(:,4:6)


maxeff=num2str(max(max(matrix2)),3);


    [junk, row]=max(matrix2);


    [junk, column]=max(max(matrix2));
row=row(column);


name2=sprintf('Radial_Silicon Eff Ln=%s, Lp=%s, Sn=%s, taun0=%s,...
    taup0=%s, Na=%s, Nd=%s, window_width=%s, maxeff=%s.txt',...
    t2,t1,t3,t11,t12,t8,t9,t10,maxeff);
name3=sprintf('Radial_Silicon Jsc Ln=%s, Lp=%s, Sn=%s, taun0=%s,...
    taup0=%s, Na=%s, Nd=%s, window_width=%s, maxeff=%s.txt',...
    t2,t1,t3,t11,t12,t8,t9,t10,maxeff);
name4=sprintf('Radial_Silicon Voc Ln=%s, Lp=%s, Sn=%s, taun0=%s,...
    taup0=%s, Na=%s, Nd=%s, window_width=%s, maxeff=%s.txt',...
```

```
    t2,t1,t3,t11,t12,t8,t9,t10,maxeff);
name5=sprintf('Radial_Silicon ff Ln=%s, Lp=%s, Sn=%s, taun0=%s,...
    taup0=%s, Na=%s, Nd=%s, window_width=%s, maxeff=%s.txt',...
    t2,t1,t3,t11,t12,t8,t9,t10,maxeff);
save(name2,'matrix2','-ASCII','-TABS')
save(name3,'matrixJsc','-ASCII','-TABS')
save(name4,'matrixVoc','-ASCII','-TABS')
save(name5,'matrixff','-ASCII','-TABS')


figure(1)
surf(log10(R),log10(L),matrix2(2:(nL+1),2:(nR+1)))
xlabel('log_{10}(R) (log_{10}(cm))')
ylabel('log_{10}(L) (log_{10}(cm))')
zlabel('Efficiency (%)')
name2a=sprintf('Radial cell Eff.  with Ln=%s, Na=%s, Nd=%s, Sn=%s,...
    maxEff=%s', t2,t8,t9,t3, maxeff);
title(name2a)


figure(2)
surf(log10(R),log10(L),matrixJsc(2:(nL+1),2:(nR+1)))
xlabel('log_{10}(R) (log_{10}(cm))')
ylabel('log_{10}(L) (log_{10}(cm))')
zlabel('Jsc')
name2b=sprintf('Radial cell Jsc with Ln=%s, Na=%s, Nd=%s, Sn=%s,...
    maxEff=%s', t2,t8,t9,t3, maxeff);
title(name2b)


figure(3)
surf(log10(R),log10(L),matrixVoc(2:(nL+1),2:(nR+1)))
xlabel('log_{10}(R) (log_{10}(cm))')
ylabel('log_{10}(L) (log_{10}(cm))')
zlabel('Voc')
```

```
name2c=sprintf('Radial cell Voc with Ln=%s, Na=%s, Nd=%s, Sn=%s,...

    maxEff=%s', t2,t8,t9,t3, maxeff);

title(name2c)


figure(4)

surf(log10(R),log10(L),matrixff(2:(nL+1),2:(nR+1)))

xlabel('log_{10}(R) (log_{10}(cm))')

ylabel('log_{10}(L) (log_{10}(cm))')

zlabel('ff')

name2d=sprintf('Radial cell ff with Ln=%s, Na=%s, Nd=%s, Sn=%s,...

    maxEff=%s', t2,t8,t9,t3, maxeff);

title(name2d)


beep
```

A.1.1   depletionregion.m

```
function [x1,x2,x3,x4,Vbi]=depletionregion(Nd,Na,R,epsilonp,epsilonn,ni,...

    bias,windowwidth) %depletionregion.m %calculates the thickness of each

    region of the pn junction in the cylindrical geometry, and the built in

    voltage, given certain dopant densities and a wire of a given radius and

    minimum emitter thickness, at a given bias


q=1.60219e-19;

kB=1.3807e-23;

T=300;


Vbi=kB*T/q*log(Na*Nd/ni^2);


if bias>=Vbi

    x1=0;

    x2=0;
```

```matlab
        x3=0;

        x4=0;

        Vbi=0;


        %disp('3')


elseif bias<Vbi


    x3guess=sqrt(2*Nd*epsilonn*epsilonp*(Vbi-bias)/(q*Na*(Nd*epsilonn+Na*...
        epsilonp)));
    x3old=0;
    x3new=sqrt(2*Nd*epsilonn*epsilonp*(Vbi-bias)/(q*Na*(Nd*epsilonn+Na*...
        epsilonp)));


    %disp('4')


    while abs(x3old-x3new)>1e-9
        x3old=x3new;
        x3new=FZERO(@depletion,x3old,[],Vbi-bias,0,epsilonp,epsilonn,Na,Nd);
    end
    x3max=x3new;
    x2max=sqrt(Na/Nd*x3max^2+x3max^2)-x3max;
    %VBI=q*Na/(4*epsilonp)*x3max^2+q*Nd/(4*epsilonn)*x3max^2-...
        q*Nd/(4*epsilonn)*R^2+q*Nd/(2*epsilonn)*R^2*log(R/x3max);


    if (x2max+x3max)>=R
        x4=0;
        x1=0;
        x2=x2max*R/(x2max+x3max);
        x3=x3max*R/(x2max+x3max);
        Vbi=(q*Na/(4*epsilonp)*x3^2-q*Nd/(4*epsilonn)*((x3+x2)^2-x3^2)+...
            q*Nd/(2*epsilonn)*(x3+x2)^2*(log((x3+x2)/x3)));
```

```
    %disp('5')


  elseif (x2max+x3max)<R
    x4old=1;
    x4new=0;
    while abs(x4old-x4new)>1e-9
      x4old=x4new;
      x3=FZERO(@depletion,x3guess,[],Vbi-bias,x4old,epsilonp,...
         epsilonn,Na,Nd);
      x2=sqrt(Na*((x3+x4old)^2-x4old^2)/Nd+(x3+x4old)^2)-x3-x4old;
      if x3>=(R-windowwidth)
        x1=R-x2-x3;
        x4new=0;
      elseif x3<(R-windowwidth)
        x1=max(0,windowwidth-x2);
        x4new=max(0,R-x1-x2-x3);
      end
    end
    x4=x4new;
  else
    disp('error 2')
  end
else
  disp('error 3')
end
```

A.1.2 depletion.m

```
function output=depletion(x3,V,x4,epsilonp,epsilonn,Na,Nd) %depletion.m
%is used to calculate the value of $x_3$ that self-consistently gives the
correct voltage drop across the pn junction, in the cylindrical geometry
```

```
q=1.60219e-19;
d2=x3+x4;
x2=sqrt(Na*(d2^2-x4^2)/Nd+d2^2)-d2;
if x4>0
    output=V-(q*Na/(4*epsilonp)*(d2^2-x4^2)-q*Na/(2*epsilonp)*x4^2*...
        log(d2/x4)-q*Nd/(4*epsilonn)*((d2+x2)^2-d2^2)+q*Nd/(2*epsilonn)*...
        (d2+x2)^2*(log((d2+x2)/d2)));
elseif x4==0
    output=V-(q*Na/(4*epsilonp)*d2^2-q*Nd/(4*epsilonn)*((d2+x2)^2-d2^2)+...
        q*Nd/(2*epsilonn)*(d2+x2)^2*(log((d2+x2)/d2)));
end
```

A.2   Planar pn Junction Simulation

This is the planar pn junction simulation code:

```
clear all
format short g
%warning off MATLAB:divideByZero


load silicon_E_flux_alpha %silicon_E_flux_alpha.mat contains the vectors
flux, which is the solar flux in photons cm^-2 s^-1 eV^-1, and alpha, which is
the absorption coefficient of Si in cm^-1, as functions of the vector E,
which is an energy vector in eV
n=length(E)-1;


%isthereadepletionregion=input('Depletion Region?  (1=yes, 0=no) ');
isthereadepletionregion=1; %gives the user the explicit option of turning
off depletion region recombination
```

```
L=[1e-4,2e-4,5e-4,1e-3,2e-3,5e-3,1e-2,2e-2,5e-2,1e-1]; %L is a vector
containing the various cell thicknesses that will be considered, in cm


matrix2=L';
matrixJsc=L';
matrixVoc=L';
matrixff=L';


%dope=[1,10,1e2,1e3,1e4,1e5,1e6,1e7,1e8]*5e12;
%muele=[1500,1500,1500,1500,1000,400,150,100,100];
%muhol=[500,500,500,400,300,150,60,50,50]; %these lines indicate the
maximum electron and hole mobilities possible in Si at various doping
levels, as given by [52], for reference


%max Na = [>1e20, >1e20, 9e19, 4e19, 2e19, 9e18, 4e18, 2e18, 8e17, 3e17]
%vs Ln = [1e-5, 2e-5, 5e-5, 1e-4, 2e-4, 5e-4, 1e-3, 2e-3, 5e-3, 1e-2]
% => mun= [95, 95, 95, 100, 110, 130, 160, 195, 300, 540] %these lines
indicate the maximum electron diffusion length possible in Si at various
doping levels, as given by [53], for reference


N=length(L);
count=1:N;
dE=(E(2:(n+1))-E(1:n));
alpha2=alpha(2:(n+1));
alpha1=alpha2; %alpha1 and alpha2 are the absorption coefficients of the
n- and p-type materials, respectively
gammaA=flux(2:(n+1)); %gammaA is the photon flux incident on the top of
the n-type quasineutral region


%Define constants
q=1.60219e-19;
kB=1.3807e-23;
```

```
T=300;
matrix=[];

%Silicon data
%Eg=1.12;
Nc=2.8e19;
Nv=1.04e19;
ni=1.4e10;

dopants=1e18;
Na=dopants;
mun=270;
Nd=dopants;
mup=95;

Dn=kB*T/q*mun;
Dp=kB*T/q*mup;

Sp=1e5;
Sn=Sp;
windowwidth=1e-6*ones(1,N); %minimum emitter thickness, in cm

sigman=1e-15;
sigmap=sigman;
vth=1e7;

Lns=[1e-5,2e-5,5e-5,1e-4,2e-4,5e-4,1e-3,2e-3,5e-3,1e-2];
for counter_Lns=1:length(Lns)

Ln=Lns(counter_Lns); Nr=Dn/(Ln^2*sigman*vth);
taun0=1/(sigman*Nr*vth);
taup0=1/(sigmap*Nr*vth);
```

```
taun=taun0;

taup=taup0;

%taun0=1e-6;taup0=taun0; %activate this line to set the depletion region

minority electron lifetime τ_{n0} separately from the quasineutral region

minority electron lifetime τ_n (similarly for holes)

Lp=sqrt(taup*Dp);


epsilon0=8.85418e-14;

epsilons=11.9*epsilon0;

epsilonp=epsilons;

epsilonn=epsilons;


np0=ni^2/Na;

pn0=ni^2/Nd;

Vbimax=kB*T/q*log(Na*Nd/ni^2);

V=linspace(0,99/100*Vbimax);

NN=length(V);

Vbi=zeros(NN,N);


if isthereadepletionregion==1


   x2maxmax=sqrt(2*epsilonn*epsilonp*Na*Vbimax/(q*Nd*(Na*epsilonp+...
      Nd*epsilonn)));
   x3maxmax=sqrt(2*epsilonn*epsilonp*Nd*Vbimax/(q*Na*(Na*epsilonp+...
      Nd*epsilonn)));
   windowwidth(windowwidth<x2maxmax)=x2maxmax;
   for i=1:N
      if (x2maxmax+x3maxmax)>=L(i)
         x2j(i)=x2maxmax*L(i)/(x2maxmax+x3maxmax);
         windowwidth(i)=x2j(i);
         x3j(i)=x3maxmax*L(i)/(x2maxmax+x3maxmax);
         Vbi(:,i)=q*Nd/(2*epsilonn)*x2j(i)^2+q*Na/(2*epsilonp)*x3j(i)^2;
```

```
elseif (x2maxmax+x3maxmax)<L(i)

    Vbi(:,i)=Vbimax;

end

for ii=1:NN

    bias(ii,i)=V(ii);

    x2max(ii,i)=sqrt(2*epsilonn*epsilonp*Na*(Vbi(ii,i)-bias(ii,i))/...

        (q*Nd*(Na*epsilonp+Nd*epsilonn)));

    x3max(ii,i)=sqrt(2*epsilonn*epsilonp*Nd*(Vbi(ii,i)-bias(ii,i))/...

        (q*Na*(Na*epsilonp+Nd*epsilonn)));

    if (x2max(ii,i)+x3max(ii,i))>=L(i)

        x4(ii,i)=0;

        x1(ii,i)=0;

        x2(ii,i)=x2j(i);

        x3(ii,i)=x3j(i);

        % Vbi(ii,i)=bias(ii,i)+q*Nd/(2*epsilonn)*x2(ii,i)^2+q*Na/...

            (2*epsilonp)*x3(ii,i)^2;

    elseif (x2max(ii,i)+x3max(ii,i))<L(i)

        if x2max(ii,i)>=windowwidth(i)

            x1(ii,i)=0;

            x2(ii,i)=x2max(ii,i);

        elseif x2max(ii,i)<windowwidth(i)

            x1(ii,i)=windowwidth(i)-x2max(ii,i);

            x2(ii,i)=x2max(ii,i);

        else

            disp('error')

            break

        end

        x3(ii,i)=x3max(ii,i);

        x4(ii,i)=L(i)-x1(ii,i)-x2(ii,i)-x3(ii,i);

    else

        disp('error')

        break
```

```
end

if bias(ii,i)>Vbi(ii,i)
    JOA(ii:NN,i)=zeros(NN-ii+1,1);
    JOC(ii:NN,i)=zeros(NN-ii+1,1);
    JlA(ii:NN,i)=zeros(NN-ii+1,1);
    JlC(ii:NN,i)=zeros(NN-ii+1,1);
    Jgdep(ii:NN,i)=zeros(NN-ii+1,1);
    Jrdep(ii:NN,i)=zeros(NN-ii+1,1);
    bias(ii:NN,i)=zeros(NN-ii+1,1);
    break
end
d1(ii,i)=x1(ii,i)+x2(ii,i);
d2(ii,i)=x3(ii,i)+x4(ii,i);
gammaC(:,i,ii)=flux(2:(n+1)).*exp(-alpha1*d1(ii,i)-...
    alpha2*x3(ii,i)); %gammaC is the photon flux incident on the
    top of the p-type quasineutral region

JlAperE(:,i,ii)=-(q*gammaA.*dE./(1-alpha1.^(-2)*Lp^(-2)).*...
    ((Sn./(alpha1*Dp)+ones(n,1)-exp(-alpha1*x1(ii,i)).*(Sn./...
    (alpha1*Dp)*cosh(x1(ii,i)/Lp)+1./(alpha1*Lp)*sinh(x1(ii,i)/...
    Lp)))./(ones(n,1)*(Sn*Lp/Dp*sinh(x1(ii,i)/Lp)+...
    cosh(x1(ii,i)/Lp)))-exp(-alpha1*x1(ii,i)))).*(ones(n,1));
JlCperE(:,i,ii)=-(q*dE./(1-alpha2.^(-2)*Ln^(-2)).*(1-1./(alpha2*...
    Ln).*(Sp*Ln/Dn*(ones(n,1)*cosh(x4(ii,i)/Ln)-exp(-alpha2*...
    x4(ii,i)))+ones(n,1)*sinh(x4(ii,i)/Ln)+alpha2*Ln.*...
    exp(-alpha2*x4(ii,i)))./(ones(n,1)*(Sp*Ln/Dn*sinh(x4(ii,i)/...
    Ln)+cosh(x4(ii,i)/Ln)))).*gammaC(:,i,ii)).*(ones(n,1));

JdepperE(:,i,ii)=-q*gammaA.*dE.*exp(-alpha1*x1(ii,i)).*(1-...
    exp(-alpha1*x2(ii,i)-alpha2*x3(ii,i)));
```

```
        J1A(ii,i)=sum(J1AperE(:,i,ii));

        J1C(ii,i)=sum(J1CperE(:,i,ii));

        Jgdep(ii,i)=sum(JdepperE(:,i,ii));


        J0A(ii,i)=-q*Dp*pn0/Lp*(Sn*Lp/Dp*cosh(x1(ii,i)/Lp)+...
            sinh(x1(ii,i)/Lp))./(Sn*Lp/Dp*sinh(x1(ii,i)/Lp)+...
            cosh(x1(ii,i)/Lp));
        J0C(ii,i)=-q*Dn*np0/Ln*(Sp*Ln/Dn*cosh(x4(ii,i)/Ln)+...
            sinh(x4(ii,i)/Ln))./(Sp*Ln/Dn*sinh(x4(ii,i)/Ln)+...
            cosh(x4(ii,i)/Ln));


        Jrdep(ii,i)=-q*ni*(x2(ii,i)+x3(ii,i))/sqrt(taun0*taup0)*(2*...
            sinh(q*bias(ii,i)/(2*kB*T))/(q*(Vbi(ii,i)-
            bias(ii,i))/(kB*T)))*pi/2;


    end

end


    J1=J1A+J1C+Jgdep;
    J0=J0A+J0C;
    J=(J0.*(exp(q*bias/(kB*T))-1)-J1+Jrdep);

elseif isthereadepletionregion==0


    for i=1:N
        Vbi(:,i)=Vbimax;
        for ii=1:NN
            bias(ii,i)=V(ii);
            x1(ii,i)=windowwidth(i);
            x4(ii,i)=L(i)-x1(ii,i);
            if bias(i)>Vbi(ii,i)

                J0A(ii:NN,i)=zeros(NN-ii+1,1);
```

```
        JOC(ii:NN,i)=zeros(NN-ii+1,1);

        JlA(ii:NN,i)=zeros(NN-ii+1,1);

        JlC(ii:NN,i)=zeros(NN-ii+1,1);

        Jgdep(ii:NN,i)=zeros(NN-ii+1,1);

        Jrdep(ii:NN,i)=zeros(NN-ii+1,1);

        bias(ii:NN,i)=zeros(NN-ii+1,1);

        break

    end

    d1(ii,i)=x1(ii,i);

    gammaC(:,i,ii)=flux(2:(n+1)).*exp(-alpha1*d1(ii,i)); %gammaC is
the photon flux incident on the top of the p-type quasineutral region


    JlAperE(:,i,ii)=-(q*gammaA.*dE./(1-alpha1.^(-2)*Lp^(-2)).*...
        ((Sn./(alpha1*Dp)+ones(n,1)-exp(-alpha1*x1(ii,i))).*(Sn./...
        (alpha1*Dp)*cosh(x1(ii,i)/Lp)+1./(alpha1*Lp)*sinh(x1(ii,i)/...
        Lp)))./(ones(n,1)*(Sn*Lp/Dp*sinh(x1(ii,i)/Lp)+cosh(x1(ii,i)/...
        Lp)))-exp(-alpha1*x1(ii,i)))).*(ones(n,1));
    JlCperE(:,i,ii)=-(q*dE./(1-alpha2.^(-2)*Ln^(-2)).*(1-1./...
        (alpha2*Ln).*(Sp*Ln/Dn*(ones(n,1)*cosh(x4(ii,i)/Ln)-...
        exp(-alpha2*x4(ii,i)))+ones(n,1)*sinh(x4(ii,i)/Ln)+alpha2*...
        Ln.*exp(-alpha2*x4(ii,i)))./(ones(n,1)*(Sp*Ln/Dn*...
        sinh(x4(ii,i)/Ln)+cosh(x4(ii,i)/Ln)))).*gammaC(:,i,ii)).*...
        (ones(n,1));


    JlA(ii,i)=sum(JlAperE(:,i,ii));
    JlC(ii,i)=sum(JlCperE(:,i,ii));


    JOA(ii,i)=-q*Dp*pn0/Lp*(Sn*Lp/Dp*cosh(x1(ii,i)/Lp)+...
        sinh(x1(ii,i)/Lp))./(Sn*Lp/Dp*sinh(x1(ii,i)/Lp)+...
        cosh(x1(ii,i)/Lp));
    JOC(ii,i)=-q*Dn*np0/Ln*(Sp*Ln/Dn*cosh(x4(ii,i)/Ln)+...
        sinh(x4(ii,i)/Ln))./(Sp*Ln/Dn*sinh(x4(ii,i)/Ln)+...
```

```
                cosh(x4(ii,i)/Ln));


        Jl=JlA+JlC;
        J0=J0A+J0C;


        J=(J0.*(exp(q*bias/(kB*T))-1)-Jl);


    end


  end


end


P=J.*bias;
P(P<0)=0;
[maxP,posn]=max(P);
eff=maxP/(.1)*100;
Jsc=J(1,:);
b=sum(J>0);
for j=1:N;
    if b(j)~=0
        if b(j)==100
            Voc(j)=0;
        elseif bias(b(j)+1,j)==0
            Voc(j)=0;
        else
            Voc(j)=(bias(b(j),j)+bias(b(j)+1,j))/2;
        end
    else
        Voc(j)=0;
    end
end
```

```matlab
ff=maxP./(Voc.*Jsc);


Lshort=L;
Lshort(~(ff<0.9999&ff>0))=0;
Vocshort=Voc;
Vocshort(~(ff<0.9999&ff>0))=0;
Jscshort=Jsc;
Jscshort(~(ff<0.9999&ff>0))=0;
ffshort=ff;
ffshort(~(ff<0.9999&ff>0))=0;
effshort=eff;
effshort(~(ff<0.9999&ff>0))=0;
%matrix=[matrix; Lshort',effshort',Jscshort', Vocshort', ffshort'];


%disp(' L (cm) Jsc (A/cm^2) Voc (V) ff Efficiency (%)')
%disp([Lshort',Jscshort', Vocshort', ffshort', effshort'])
matrix2=[matrix2,effshort'];
matrixJsc=[matrixJsc,Jscshort'];
matrixVoc=[matrixVoc,Vocshort'];
matrixff=[matrixff,ffshort'];


end


t1=num2str(Lp,4);
t2=num2str(Ln,4);
t3=num2str(Sn,4);
t6=num2str(mup,4);
t7=num2str(mun,4);
t8=num2str(Na,4);
t9=num2str(Nd,4);
t10=num2str(windowwidth,4);
t11=num2str(taun0,4);
```

```
t12=num2str(taup0,4);

maxeff=num2str(max(eff),3);

name=sprintf('GaAs Planar matrix Ln=%s, Lp=%s, Sn=%s, taun0=%s,...
    taup0=%s, Na=%s, Nd=%s, window_width=%s, maxeff=%s.txt', t2,t1,t3,...
    t11,t12,t8,t9,t10,maxeff);

name2=sprintf('GaAs Planar Eff Ln=%s, Lp=%s, Sn=%s, taun0=%s, taup0=%s,...
    Na=%s, Nd=%s, window_width=%s, maxeff=%s.txt', t2,t1,t3,t11,t12,t8,...
    t9,t10,maxeff);

name3=sprintf('GaAs Planar Jsc Ln=%s, Lp=%s, Sn=%s, taun0=%s, taup0=%s,...
    Na=%s, Nd=%s, window_width=%s, maxeff=%s.txt', t2,t1,t3,t11,t12,t8,...
    t9,t10,maxeff);

name4=sprintf('GaAs Planar Voc Ln=%s, Lp=%s, Sn=%s, taun0=%s, taup0=%s,...
    Na=%s, Nd=%s, window_width=%s, maxeff=%s.txt', t2,t1,t3,t11,t12,t8,...
    t9,t10,maxeff);

name5=sprintf('GaAs Planar ff Ln=%s, Lp=%s, Sn=%s, taun0=%s, taup0=%s,...
    Na=%s, Nd=%s, window_width=%s, maxeff=%s.txt', t2,t1,t3,t11,t12,t8,...
    t9,t10,maxeff);


nL=length(L);
nR=length(Lns);


figure(1)
surf(log10(Lns),log10(L),matrix2(:,2:(nR+1)))
xlabel('log_10(Ln) (log_10(cm))')
ylabel('log_10(L) (log_10(cm))')
zlabel('Efficiency (%)')
name2a=sprintf('Si Planar cell Eff. with Na=%s, Nd=%s, Sn=%s,...
    maxEff=%s', t8,t9,t3, maxeff);
title(name2a)


figure(2)
surf(log10(Lns),log10(L),matrixJsc(:,2:(nR+1)))
```

```
xlabel('log_10(Ln) (log_10(cm))')

ylabel('log_10(L) (log_10(cm))')

zlabel('Jsc')

name2b=sprintf('Si Planar cell Jsc with Na=%s, Nd=%s, Sn=%s,...
    maxEff=%s', t8,t9,t3, maxeff);

title(name2b)


figure(3)

surf(log10(Lns),log10(L),matrixVoc(:,2:(nR+1)))

xlabel('log_10(Ln) (log_10(cm))')

ylabel('log_10(L) (log_10(cm))')

zlabel('Voc')

name2c=sprintf('Si Planar cell Voc with Na=%s, Nd=%s, Sn=%s,...
    maxEff=%s', t8,t9,t3, maxeff);

title(name2c)


figure(4)

surf(log10(Lns),log10(L),matrixff(:,2:(nR+1)))

xlabel('log_10(Ln) (log_10(cm))')

ylabel('log_10(L) (log_10(cm))')

zlabel('ff')

name2d=sprintf('Si Planar cell ff with Na=%s, Nd=%s, Sn=%s,...
    maxEff=%s', t8,t9,t3, maxeff);

title(name2d)


beep
```

A.3   Axial pn Junction Wire Simulation

This is the radial pn junction simulation code:

```
clear all
```

```
format short g


%Define constants


q=1.60219e-19;

kB=1.3807e-23;

T=300;


%Silicon data

%Eg=1.12;

Nc=2.8e19;

Nv=1.04e19;

ni=1.4e10;


dopants=1e18;

Na=dopants;

mun=270;

Nd=dopants;

mup=95;


Snr=1e2;

Snz=1; %set the surface recombination velocities at the r=R surface, and
the top and bottom surfaces


%alpha=1e2;

alpha=1281.1; %the absorption coefficient for Si assuming a wavelength-
independent α, as in Fig.  2.2


gamma0=2.7e17; %flux of photons cm⁻² s⁻¹ with energy > 1.12 eV

%gamma0=4.4996e16 %flux of photons cm⁻² s⁻¹ with 1.12 eV > energy > 0.95 eV

%gamma0=4.5752e16 %flux of photons cm⁻² s⁻¹ with 0.95 eV > energy > 0.74 eV
```

```
R=5e-4; %wire radius, in cm

d1=0; %thickness of top quasineutral region, in cm

d2=1e-2; %thickness of bottom quasineutral region, in cm


V=0; %applied bias, in V


Ln=1e-3; %minority electron diffusion length in the bottom layer, in cm


tol=1e-11;
w=0.01; %numerical solver parameters


gridsizer=50; %number of grid points in each quasineutral region, in the
r-direction
gridsizez=50; %number of grid points in each quasineutral region, in the
z-direction


%[Jtop,gammaout1]=axialdifferencetop(Nc,Nv,ni,Na,mun,Nd,mup,Snr,Snz,...
    alpha,gamma0,R,d1,V,Ln,tol,w,gridsizer,gridsizez);
Jtop=0;


gammaout1=gamma0*exp(-alpha*d1); %solar flux hitting bottom layer is
filtered by top layer


[Jbottom,gammaout2]=axialdifferencebottom(Nc,Nv,ni,Na,mun,Nd,mup,Snr,Snz,...
    alpha,gammaout1,R,d2,V,Ln,tol,w,gridsizer,gridsizez);


Jbottom
J=Jtop+Jbottom
```

A.3.1   axialdifferencebottom.m

```
function [Jn,gammaout]=axialdifferencebottom(Nc,Nv,ni,Na,mun,Nd,mup,Snr,...
    Snz,alpha,gamma0,R,x4,V,Ln,tol,w,gridsizer,gridsizez)
```

```
%axialdifferencebottom.m is a finite element solver that determines the
    current contribution from the base of the axial cell, given the input
    parameters

%Define constants

q=1.60219e-19;
kB=1.3807e-23;
T=300;

Dn=kB*T/q*mun;
Dp=kB*T/q*mup;

sigman=1e-15;
sigmap=sigman;
vth=1e7;

np0=ni^2/Na;
pn0=ni^2/Nd;
Vbi=kB*T/q*log(Na*Nd/ni^2);
epsilon0=8.85418e-14;

beta=alpha*Ln;
taun=Ln^2/Dn;

r=linspace(0+R/(2*(gridsizer-1)),R-R/(2*(gridsizer-1)),gridsizer)'*...
    ones(1,gridsizez);
rho=r/Ln;
delrho=rho(2,1)-rho(1,1);
z=ones(gridsizer,1)*(linspace(0+x4/(2*(gridsizez-1)),x4-x4/...
    (2*(gridsizez-1)),gridsizez));
```

```
RRRA1=-Snr*alpha*gamma0*taun/(Snr*besseli(0,R/Ln)+Ln/taun*...
    besseli(1,R/*Ln))exp(-alpha*z);
RRR=RRRA1.*besseli(0,r/Ln)+alpha*gamma0*taun*exp(-alpha*z);


B3=-alpha*gamma0*taun/(alpha^2*Ln^2-1);


B1=np0*(exp(q*V/(kB*T))-1)-B3;
B2num=-B1*(Snz*cosh(x4/Ln)+Dn/Ln*sinh(x4/Ln))+B3*(alpha*Dn-Snz)*
    exp(-alpha*x4);
B2den=Snz*sinh(x4/Ln)+Dn/Ln*cosh(x4/Ln);
B2=B2num/B2den;


ZZZ=B1*cosh(z/Ln)+B2*sinh(z/Ln)+B3*exp(-alpha*z);


nprimeseed=sqrt(RRR.*ZZZ)/10;


nu=nprimeseed*Dn/(alpha*gamma0*Ln^2); %this is the seed solution, from
which the numerical solver generates a more accurate result
%nu=zeros(gridsizer, gridsizez);
%Y=zeros(gridsizer, gridsizez);
%Z=zeros(gridsizer, gridsizez);


zeta=z/Ln;
delzeta=zeta(1,2)-zeta(1,1);
%nuold=np0*Dn/(alpha*gamma0*Ln^2)*ones(gridsizer, gridsizez);
nuold=zeros(gridsizer, gridsizez);


small=eye(gridsizer-1, gridsizer-1);
upper1=[zeros(gridsizer-1,1),small];
uppereye=[upper1;zeros(1,gridsizer)];
lower1=[zeros(1,gridsizer-1);small];
lowereye=[lower1,zeros(gridsizer,1)];
```

```
A=lowereye-2*eye(gridsizer,gridsizer)+uppereye;


A1=A;


smallz=eye(gridsizez-1, gridsizez-1);
upper1z=[zeros(gridsizez-1,1),smallz];
uppereyez=[upper1z;zeros(1,gridsizez)];
lower1z=[zeros(1,gridsizez-1);smallz];
lowereyez=[lower1z,zeros(gridsizez,1)];
A2=lowereyez-2*eye(gridsizez,gridsizez)+uppereyez;


B=1./(2*rho(1:gridsizer,1)*ones(1,gridsizer)).*(uppereye-lowereye);
E=exp(-beta*zeta);


nu(:,1)=Dn*np0/(alpha*gamma0*Ln^2)*(exp(q*V/(kB*T))-1);


while max(max(abs(nuold-nu)))>tol; %this while loop is the core of the
solution method - iterate until the solution converges, while maintaining
the boundary conditions
    nuold=nu;
    nu=nuold+w*(A1*nuold+delrho*B*nuold+delrho^2*(1/delzeta^2*nuold*A2-...
        nuold+E));
    nu(gridsizer,:)=Dn/(Snr*Ln*delrho+Dn)*nu(gridsizer-1,:);
    nu(:,gridsizez)=Dn/(Snz*Ln*delzeta+Dn)*nu(:,gridsizez-1);
    nu(1,:)=nu(2,:);
    nu(:,1)=(2*Dn*np0/(alpha*gamma0*Ln^2)*(exp(q*V/(kB*T))-1)+nu(:,2))/3;
    % pause
end


figure(1)
nprime=nu/(Dn/(alpha*gamma0*Ln^2))+np0;
surf(r(:,1),z(1,:),nprime')
```

```
axis tight

colorbar

xlabel('r')

ylabel('z')


V1=axis;


nu=real(nu);

Jnr=q*alpha*gamma0*Ln*(nu(:,1)-nu(:,2))/delzeta;

Jn=2*Ln^2/R^2*delrho*sum(Jnr.*rho(:,1));

Jn=-Jn;


gammaout=gamma0*exp(-alpha*x4);


beep
```

A.3.2 axialdifferencetop.m

```
function [Jn,gammaout]=axialdifferencetop(Nc,Nv,ni,Na,mun,Nd,mup,Snr,...
    Snz,alpha,gamma0,R,x4,V,Ln,tol,w,gridsizer,gridsizez)
    %axialdifferencetop.m is a finite element solver that determines the
    current contribution from the top of the axial cell, given the
    input parameters

%Define constants

q=1.60219e-19;

kB=1.3807e-23;

T=300;


Dn=kB*T/q*mun;

Dp=kB*T/q*mup;
```

```
sigman=1e-15;

sigmap=sigman;

vth=1e7;


np0=ni^2/Na;

pn0=ni^2/Nd;

Vbi=kB*T/q*log(Na*Nd/ni^2);

epsilon0=8.85418e-14;


beta=alpha*Ln;

taun=Ln^2/Dn;


r=linspace(0+R/(2*(gridsizer-1)),R-R/(2*(gridsizer-1)),gridsizer)'*...
    ones(1,gridsizez);

rho=r/Ln;

delrho=rho(2,1)-rho(1,1);

z=ones(gridsizer,1)*(linspace(0+x4/(2*(gridsizez-1)),x4-x4/...
    (2*(gridsizez-1)),gridsizez));


RRRA1=-Snr*alpha*gamma0*taun/(Snr*besseli(0,R/Ln)+Ln/taun*...
    besseli(1,R/Ln))*exp(-alpha*z);

RRR=RRRA1.*besseli(0,r/Ln)+alpha*gamma0*taun*exp(-alpha*z);


B3=-alpha*gamma0*taun/(alpha^2*Ln^2-1);

B1num=np0*(exp(q*V/(kB*T))-1)-B3*(exp(-alpha*x4)+Ln*(Snz/Dn+alpha)*...
    sinh(x4/Ln));

B1den=cosh(x4/Ln)+Ln*Snz/Dn*sinh(x4/Ln);

B1=B1num/B1den;

B2=B3*Ln*(Snz/Dn+alpha)+B1*Ln*Snz/Dn;


ZZZ=B1*cosh(z/Ln)+B2*sinh(z/Ln)+B3*exp(-alpha*z);
```

```
nprimeseed=sqrt(RRR.*ZZZ)/10;


nu=nprimeseed*Dn/(alpha*gamma0*Ln^2); %this is the seed solution, from
which the numerical solver generates a more accurate result
%nu=zeros(gridsizer, gridsizez);
%Y=zeros(gridsizer, gridsizez);
%Z=zeros(gridsizer, gridsizez);


zeta=z/Ln;
delzeta=zeta(1,2)-zeta(1,1);
%nuold=np0*Dn/(alpha*gamma0*Ln^2)*ones(gridsizer, gridsizez);
nuold=zeros(gridsizer, gridsizez);


small=eye(gridsizer-1, gridsizer-1);
upper1=[zeros(gridsizer-1,1),small];
uppereye=[upper1;zeros(1,gridsizer)];
lower1=[zeros(1,gridsizer-1);small];
lowereye=[lower1,zeros(gridsizer,1)];
A=lowereye-2*eye(gridsizer,gridsizer)+uppereye;


A1=A;


smallz=eye(gridsizez-1, gridsizez-1);
upper1z=[zeros(gridsizez-1,1),smallz];
uppereyez=[upper1z;zeros(1,gridsizez)];
lower1z=[zeros(1,gridsizez-1);smallz];
lowereyez=[lower1z,zeros(gridsizez,1)];
A2=lowereyez-2*eye(gridsizez,gridsizez)+uppereyez;


B=1./(2*rho(1:gridsizer,1)*ones(1,gridsizer)).*(uppereye-lowereye);
E=exp(-beta*zeta);
```

```
nu(:,gridsizez)=Dn*np0/(alpha*gamma0*Ln^2)*(exp(q*V/(kB*T))-1);


while max(max(abs(nuold-nu)))>tol; %this while loop is the core of the
solution method - iterate until the solution converges, while maintaining
the boundary conditions
    nuold=nu;
    nu=nuold+w*(A1*nuold+delrho*B*nuold+delrho^2*(1/delzeta^2*nuold*A2-...
        nuold+E));
    nu(gridsizer,:)=Dn/(Snr*Ln*delrho+Dn)*nu(gridsizer-1,:);
    nu(:,1)=Dn/(Snz*Ln*delzeta+Dn)*nu(:,2);
    nu(1,:)=nu(2,:);
    nu(:,gridsizez)=Dn*np0/(alpha*gamma0*Ln^2)*(exp(q*V/(kB*T))-1);
    % pause
end


nu=real(nu);
Jnr=q*alpha*gamma0*Ln*(nu(:,gridsizez)-nu(:,gridsizez-1))/delzeta;
Jn=2*Ln^2/R^2*delrho*sum(Jnr.*rho(:,1));
Jn=-Jn;


gammaout=gamma0*exp(-alpha*x4);
```

Appendix B

Radial pn Junction, Wire Array Solar Cell Fabrication

B.1 Radial pn Junction, Wire Array Solar Cell Fabrication

For convenience, the "state of the art" radial pn junction, wire array solar cell fabrication is presented here in full, from array patterning to sample metallization.

B.1.1 Array Patterning

1. We start with 3", ~ 400 μm thick, n-type Si(111) wafers of 0.005 - 0.02 Ω cm resistivity, purchased from International Wafer Service with a 300 nm wet thermal oxide.

2. Place the wafer on the spinner and turn on the vacuum. Blow off any dust particles from the wafer surface with a N_2 gun. Coat the wafer surface with MCC Primer 80/20 (Microchem), wait for 10 s, and then spin dry for 30 s at 3000 rpm (acceleration index ACL = 100).

3. Coat the wafer with S1813 photoresist (Microchem), and then spin at 3000 rpm for 1 min (acceleration index ACL = 100).

4. Cure on a hotplate at 115 °C for 2 mins.

5. Photolithographically pattern the resist using the Karl Suss MA 6 mask aligner (aka "the new mask aligner"). For most of our masks the active area is less than the size of a 3" wafer, therefore to maximize the usable sample area it is best to cleave the sample into 4 - 6 pieces at this stage. Then a pattern can be transferred by exposing for ~ 10 s (exact time will vary with bulb age and should be recalibrated from time to time) in Hard Contact mode.

6. Place the sample in MF-319 developer (Microchem) for 60 s. Check with the optical microscope that the pattern has come out correctly, and if not adjust the exposure time accordingly for subsequent patterns.

7. Cure on a hotplate at 115 °C for 1 min.

8. After development of the pattern, the oxide within the patterned holes can be removed by immersion of the samples for 3 mins in buffered HF (Transene) (for the 3 μm diameter, 7 μm pitch pattern). It is important to use the slotted wafer holder to minimize resist lift-off / failure during the etch. Using this wafer holder the BHF etches the oxide at $\sim$ 2 nm/s.

9. Thermally evaporate 300 nm of either Au (Electronic Space Products International, 3N5 purity), Cu (Alfa Aesar, 5N purity) or Ni (Electronic Space Products International, 4N5 purity). Note that the liquid nitrogen cooled stage is required for best results with Ni. Start liquid nitrogen cooling 10 mins before starting to heat the metal to ensure the samples reach a low enough temp. Note also that with the cooled stage and a tooling factor of 148%, the quartz crystal monitor overestimates the thickness of the deposited metal film by $\sim$ a factor of 3).

10. Lift off the resist by submerging the sample in acetone and (if necessary) leaving overnight and/or (if necessary) sonication. Rinse sample in acetone, isopropanol, methanol, and finally H_2O before drying with nitrogen.

B.1.2   Wire Growth

11. Cleave the patterned samples to the desired size and transfer to the SiCl4 CVD system in Watson 255. Anneal the samples at 1000 °C for 20 mins under 1 atm of H2 at a flow rate of 1000 sccm. Wires are then grown under 1 atm of H_2 and $SiCl_4$, at flow rates of 1000 sccm and 20 sccm, respectively, for up to 30 mins. Growth rate varies depending upon catalyst, $\sim$ 2 - 3 μm/min for Au, $\sim$ 2 - 7 μm/min (or even faster) for Cu and Ni.

B.1.3 Catalyst Removal

12. After a wire array was grown, the first step towards making a device involved removing the metal catalyst particle at the tip as well as the near-surface of the wires. For gold the tip was removed the following way:

    (a) 10:1 solution of DI water: 48% HF for 30 s to remove surface oxide on the Si.

    (b) 9:1 solution of TFA etchant (Transene): 38% HCl for 20 mins.

    (c) 10:1 solution of DI water: 38% HCl for 10 s to rinse.

    (d) Rinse in DI water, dry with N_2.

    For Cu and Ni the following procedure appears to work well:

    (a) Buffered HF (Transene) for 30 s.

    (b) RCA 2 clean (6:1:1 H_2O:H_2O_2:HCl at 70 °C) for 10 mins.

    (c) Buffered HF (Transene) for 30 s.

    (d) Rinse in DI water, dry with N_2.

13. The Si at the near-surface was then removed by immersion of the sample in 60 wt.% KOH at 30 °C for 30 s. This should remove $\sim$ 10 nm of the wire surface. Prior to doping, we ensured that the pattern oxide is fully removed (from the front side only) to ensure that the wire emitters were all connected. This was done by immersion in buffered HF (Transene).

B.1.4 Doping: Radial pn Junction Formation

14. The front side of the arrays were then doped n-type by stacking parallel to SiP_2O_7 diffusion wafers (PH-950, Saint-Gobain Ceramics), introducing to a tube furnace at 750 °C, ramping up to 800 °C (over about 5 mins), holding at 800 °C for 40 mins, and then ramping back down, all under UHP N_2 at 5 lpm.

15. The front surface was then exposed to buffered HF for 2 mins.

16. The samples were then re-introduced to the tube furnace at 750 °C under house N_2 bubbled through near boiling H_2O, ramped to 855 °C (over about 16 mins), and held at 855 °C for 20 mins, in order to create a high-quality surface oxide to prevent out-diffusion of the dopant atoms. The gas was then changed to dry house N_2, and the temperature ramped up to 1100 °C and held at this temperature for up to 23 hours in order to "drive in" the dopant atoms. Temperature was then ramped back down to room temperature, and the samples were not removed from the center of the furnace until the temperature there had at least dropped below 750 °C.

17. The front surface was then exposed to buffered HF for 2 mins.

18. The front surface of the samples were then doped p-type by stacking parallel to BN diffusion wafers (BN-975, Saint-Gobain Ceramics), introducing to a tube furnace at 750 °C, ramping up to 950 °C, holding at 950 °C for 40 mins, and then ramping back down, all under UHP N_2 at 5 lpm.

19. The front surface was then exposed to buffered HF for 2 mins.

20. This was followed by a low temperature oxidation at 750 °C for 20 mins, under O_2 at 5 lpm.

21. The front surface was again exposed to buffered HF for long enough that the oxide was removed (determined by the time it took to change a planar control from hyrdophilic to hydrophobic).

B.1.5   Metallization

22. Finally, oxide was removed from the entirety of the samples with buffered HF, the sample edges were cleaved off to prevent macroscopic shunting, and contact was made to the back surface by immediately rubbing Ga/In onto the back of the sample and the sample then bonded with Ag paste (SPI Supplies) to a piece of stainless steel to which electrical contact could be made with a probe tip.

23. Contact was made to the front surface with a spot of Ga/In and an electrical probe tip.

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