PROBLEMS IN SWITCHED-MODE DC AND AC POWER CONVERSION

Thesis by

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Dedicated to my parents

Ali Hossein and Fakhri Barzegar

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ABSTRACT

Several issues in the field of Power Electronics are discussed in this thesis. Part I first reviews the method of state-space averaging to analyze steady state and small-signal behavior of switched-mode dc-to-dc converters. The approach is then generalized to encompass multiple inputs and a general form of feedback system. Since the method involves matrix manipulations it is well suited for computer computation. The Switching Converter Analysis Program is developed to implement the state-space averaging method, and requires computational power only of a small desktop computer. This, together with another program which performs frequency response measurement of the actual system, constitute a powerful design tool for power electronics engineers.

Part II extends the basic one-quadrant switching dc-to-dc converter to both current and voltage bidirectionality. The proposed "push-pull" power amplifier, being a four-quadrant converter, is capable of interfacing dc *and* ac ports. This special capability is then exploited to introduce a *single-stage ac Uninterruptible Power Supply* (UPS), which can process power from dc to ac or from ac to dc. Since with the form used only one of these accomplishments is required at a time, a single converter performs as a complete system. Hence, this UPS system is reliable and economical.

Finally, Part III further generalizes the switching power amplifier to polyphase operation in such a way that a minimal number of power converters is required. Then, through a set of steps a new polyphase

power amplifier is introduced. The idea is experimentally verified by a 1 hp variable-speed motor drive with regulated output voltages. The technique has many other advantages such as ease of paralleling, dc isolation, and voltage boost, etc. The generality of the technique makes it suitable for many other line related applications such as uninterruptible power supplies, unity power factor battery chargers, and battery-to-three-phase line interfaces.

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PART I

MODELLING AND MEASUREMENT OF SWITCHED-MODE DC-TO-DC CONVERTERS

CHAPTER 1

INTRODUCTION

A switched-mode dc-to-dc converter is a circuit which can convert a dc input at one voltage and current level to an output at a different voltage and current level, in an efficient and controllable manner. The efficiency is kept as close to the ideal 100% as possible while the control can provide constant output from an unregulated input source. There are four basic types of dc-to-dc converters, which are illustrated in Fig. 1.1. The switch periodically alternates between the two positions and enables the energy to be stored in the storage elements of the circuit and subsequently released to the output port. For example, in the boost converter of Fig. 1.1b, the inductor stores energy when the switch is in position 1, and releases that energy to the output RC network when the switch changes to position 2.

The energy storage element for the first three converters is the inductor. On the other hand, the Ćuk converter transfers energy via the C_1 capacitor. When the switch is in position 2, the current of inductor L_1 charges the capacitor C_1, and in position 1 of the switch this stored energy is transferred to the inductor L_2 and subsequently to the output and load.

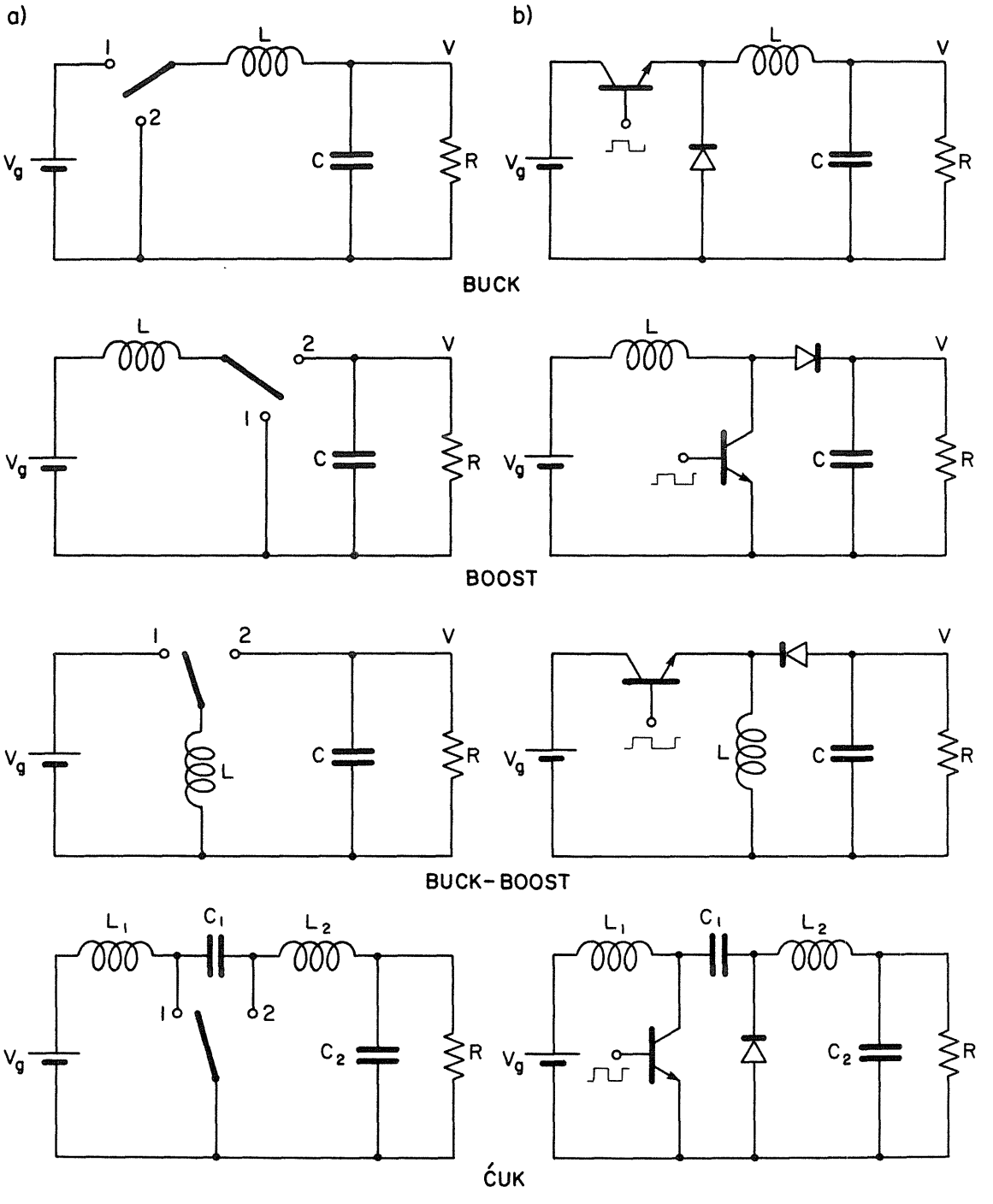


Fig. 1.1 *Four common switching dc-to-dc converters: (a) topological configuration (b) bipolar transistor implementation of the switch S.*

It can be noticed that the amount of the energy transfer depends on the time the switch spends in one position with respect to the time in the other position. One characterizing factor is the ratio of the time that the switch is in position 1, T_1, to the total switching period, T, denoted as the duty ratio, d:

$$d = \frac{T_1}{T} = \frac{T_1}{T_1 + T_2} \tag{1.1}$$

The more time spent in position 1 (large duty ratio), the more additional energy is stored in the converter and is then transferred to the output. Therefore, change of duty ratio is one way in which the output voltage and current levels can be varied. The output power is proportional to the number of energy transfers per second. That is, the output power is the product of the processed energy in each cycle and the switching frequency. Therefore, for a constant output power, the energy processing and thus the energy storage capability of the converter (sizes and values of the capacitors and inductors) are decreased as the switching frequency is increased. So, a higher switching frequency implies smaller sizes of the storage elements, and thus better utilization of the components of the converter. In practice, the chosen switching frequency is increased until second order (parasitic) effects become dominant.

Obvious advantages of switching converters are high efficiency and small size and weight. On the other hand, there are apparent difficulties in analysis of these inherently nonlinear systems

compared to their linear counterparts. Usually the switching converter is part of a larger system where some output quantity is to be regulated. The duty ratio and hence the output can be adjusted by a modulator. First, as shown in Fig. 1.2, an error signal is derived by comparison of an output quantity (along with other states) with a reference signal. Connection of this error signal to the modulator may be used to accurately regulate the output. Inside the regulator, there are two nonlinear subcircuits. One is the dc-to-dc converter and the other is the modulator. Analysis of the stability of the loop requires in-depth knowledge of both these parts. Until recently, there has been no analytical technique available. Chapter 2 is devoted to a review of the state-space averaging analysis of converters, which will provide a small-signal linear model for the converter upon which all the familiar linear circuit theories and techniques such as Nyquist Criterion, root locus, etc. can be applied. Chapter 3 develops extensions of the state-space averaging analysis method to allow more than one independent input source. This extension permits direct calculation of most transfer properties of the converters, as well as an increase in accuracy of the steady-state calculations. In another extension, generalized all-state feedback is discussed and the closed-loop responses are analytically obtained. With all-state feedback, it is possible to place the closed-loop poles at any location in the complex s-plane, while feedforward can be used to manipulate the zeros. The generalized state-space averaging method introduced in this chapter is the basis for a dedicated program

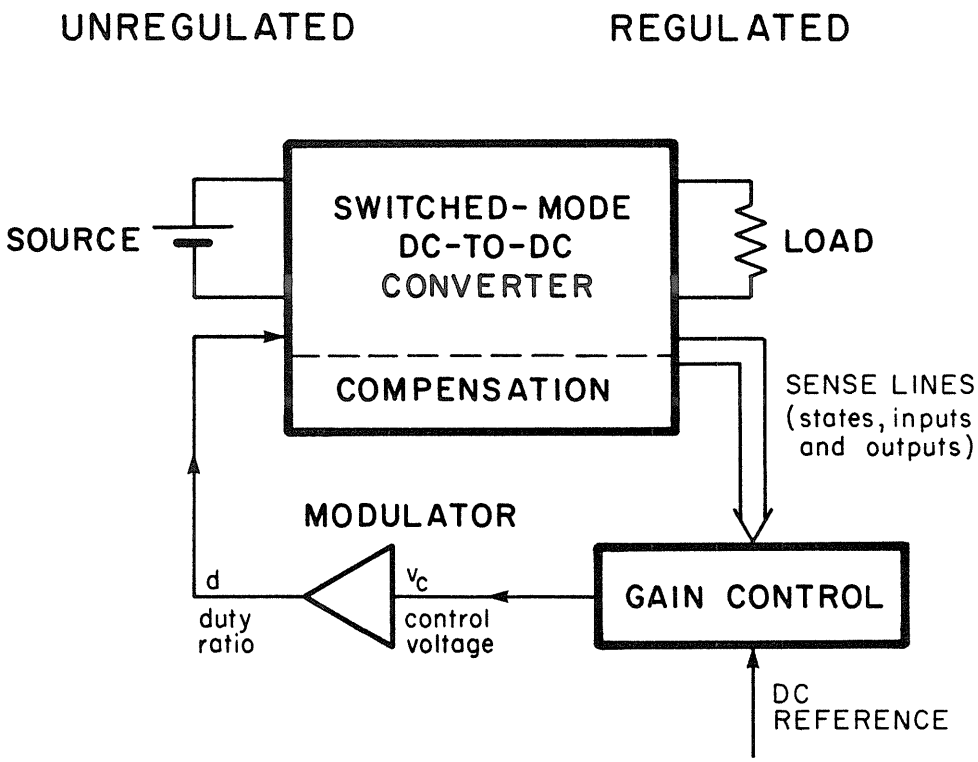


Fig. 1.2 Switching regulator: Full-state feedback regulation of the output.

which can include many second-order effects in the calculations. The powerful software is implemented on a desktop computer, and provides very accurate open-loop and closed-loop frequency response predictions verified by the measurements.

Proper design of switching regulators involves not only prediction from the model of various frequency responses, but also their verification by corresponding measurements. A section is dedicated to the frequency response measurement problem, and a solution wherein the measurement process is accelerated by a computer-controlled network analyzer. Finally, an example illustrates the accuracy of the calculations when compared with the measurement results.

Therefore, a small computer, through dedicated programs, is used to serve two functions. First, accurately calculate the frequency responses from the circuit element values and present the results in tabular or graphical form. Second, obtain the corresponding measurement results in either form from the actual hardware circuit.

These complementary analysis and measurement methods constitute extremely powerful tools in the design of switched-mode dc-to-dc converters and regulators, and yet they are also very fast and easy to use.

CHAPTER 2

REVIEW OF MODELLING TECHNIQUES

The emergence of switching converters in recent years and the continued increase in their popularity owing to their high efficiency and reliability has made the analysis of these systems a constantly demanding goal. Switching converters and regulators are inherently nonlinear, and the standard analysis techniques of linear systems do not apply. Many attempts have been made to develop modelling techniques for these circuits. The result has been the development of a series of modelling and analysis methods, each with its own advantages and disadvantages. One such technique, which has shown simplicity and effectiveness, is the state-space averaging method. The technique is used throughout this work and therefore its understanding is necessary.

2.1 State-Space Averaging Method

This technique can analyze any two-topology switching dc-to-dc converter and provide the result in the familiar form of frequency domain transfer functions and frequency responses. It is based on the state-space descriptions of the converter. In each position of the switch, the circuit is a linear time-independent system that can be analyzed by use of standard linear circuit theory.

The result is then converted to the state-space form:

$$\dot{x} = Ax + b\, v_g \tag{2.1}$$

where x is an n x 1 state vector, n is the order of the system (normally the number of the storage elements of the circuit), and v_g is the voltage source to power the converter. From the definition of the duty ratio, the switch time spent in position 1 of Fig. 1.1 is dT_s, where T_s is the switching period. The circuit constructed during the dT_s interval can be described as:

$$\dot{x} = A_1 x + b_1\, v_g \tag{2.2a}$$

$$Y = C_1^T x \tag{2.2b}$$

where Y is the output quantity in cases where the output does not coincide with one of the elements of the x vector. The remaining part of the switching cycle is denoted by $d'T_s$ where $d' \equiv 1 - d$, and

$$\dot{x} = A_2 x + b_2\, v_g \tag{2.3a}$$

$$Y = C_2^T x \tag{2.3b}$$

These descriptions correspond to two linear circuits generated by the switching action and at any moment only one is valid.

The state of the system changes according to the variation of the inputs v_g, d, and the load.

In order to predict the dynamics of the system and its response to perturbations of the inputs and the states, one must combine Eqs. (2.2) and (2.3) to dissolve the switching action. This will provide a description of the converter, over one switching period, by only one equation. This equation can then be used to obtain the essential properties of the converter. In order to generate this equation, one integrates Eqs. (2.2) and (2.3) over the corresponding time intervals to find an equation that relates the states of the converter at the end of a cycle to the states at the beginning of that cycle. A more informative form is obtained by introduction of some approximations. Finally, the equation is perturbed and linearized to find the small-signal transfer properties of the converter.

Consider the instant nT_s, at the beginning of the nth cycle when the converter states are $x(nT_s)$. The switch is turned ON and Eq. (2.2) governs the states of the converter. Then, by the techniques of linear algebra, one can exactly calculate the value of x at the end of the ON interval, at $nT_s + dT_s$:

$$x(nT_s + dT_s) = e^{A_1 dT_s} x(nT_s) + \int_0^{dT_s} e^{A_1(t-\tau)} b_1 v_g(\tau) d\tau \qquad (2.4)$$

At this instant the switch turns OFF to form the other circuit described by Eq. (2.3). With $x(nT_s + dT_s)$ as initial condition for the new differential equation, the state vector at the end of the

switching cycle is found to be:

$$x[(n+1)T_s] = e^{A_2 d'T_s} x(nT_s + dT_s) + \int_{dT_s}^{T_s} e^{A_2(t-\tau)} b_2 v_g(\tau)d\tau \quad (2.5)$$

One may combine Eqs. (2.4) and (2.5) to obtain an expression relating the $x(nT_s)$ to the $x[(n+1)T_s]$. This relation specifies the behavior of the system in the general case, but it is nonlinear and the exact solution (if it could be found) would reflect only the properties of a particular system denoted by the entries of (2.2) and (2.3). In other words, it would be a special solution for a special set of conditions. Owing to the nonlinearity of the expression, for any change in the input set, the process must be carried out again to find the new set of results. This causes the general form of solution to have a very limited use. Also, the difficulties and the generalities involved suggest computer simulation as a sensible way of solving the problem.

To extract more general information, one may introduce approximations. Suitable approximations, while still retaining reasonable accuracy, make the equations simple and attach physical interpretation to the individual terms. One such simplification involves the input voltage source v_g. Observation of practical low frequency limitation on $v_g(t)$ allows simplification of expressions (2.4) and (2.5) by the assumption that $v_g(t)$ is almost constant during one switching cycle. Equations (2.4) and (2.5) thus reduce

respectively to

$$x(nT_s + dT_s) = e^{A_1 dT_s} x(nT_s) + A_1^{-1} (e^{A_1 dT_s} - I)b_1 v_g \qquad (2.6)$$

$$x[(n+1)T_s] = e^{A_2 d'T_s} x(nT_s + dT_s) + A_2^{-1}(e^{A_2 d'T_s} - I)b_2 v_g \qquad (2.7)$$

substitute (2.6) into (2.7):

$$x[(n+1)T_s] = e^{A_2 d'T_s} e^{A_1 dT_s} x(nT_s) +$$

$$+ e^{A_2 d'T_s} A_1^{-1}(e^{A_1 dT_s} - I)b_1 v_g + A_2^{-1}(e^{A_2 d'T_s} - I)b_2 v_g \qquad (2.8)$$

The fundamental approximation results from the observation that the switching period is much shorter than the time constants of the converter, because of the inherent low-pass filtering action of the converter in which the corner frequency of the filter is much lower than the switching frequency. This point is mathematically expressed by:

$$e^{At} \simeq I + At \qquad (2.9)$$

This is the key approximation of the state-space averaging method, in which the higher order terms of the Taylor series for e^{At} are neglected. It leaves only the linear part which corresponds to the

linear form of changes of the x, that is, linear ripples. Substitution of (2.9) into (2.8) and neglect of the higher order terms gives

$$x[(n+1)T_s] \simeq [I + (dA_1 + d'A_2)T_s]\, x(nT_s) +$$

$$+ \ (db_1 + d'b_2)T_s\, v_g(nT_s) \tag{2.10}$$

Define

$$A \triangleq dA_1 + d'A_2$$

$$b \triangleq db_1 + d'b_2 \tag{2.11}$$

Therefore

$$x[(n+1)T_s] = (I + AT_s)\, x(nT_s) + bT_s\, v_g(nT_s) \tag{2.12}$$

Equation (2.12) is a difference equation to relate the states at the beginning of a cycle to the states at the beginning of the next cycle. So, the two equations (2.2) and (2.3) are replaced by a single equation and further information about the system may be obtained by manipulation of Eq. (2.12). The equation is linear with respect to the x and v_g, if the duty ratio is held constant.

However, on the contrary, variation of the duty ratio produces a difference equation with variable coefficients and thus the equation is generally nonlinear with respect to d.

One may solve Eq. (2.12) directly, by use of discrete techniques and the z-transform. On the other hand, one can dissolve the remaining switching action in Eq. (2.12) and convert it to a differential equation by means of the substitution

$$\dot{x} = \frac{x[(n+1)T_s] - x(nT_s)}{T_s} \tag{2.13}$$

so that

$$\dot{x}(t) = A(d)\, x(t) + b(d)\, v_g(t) \tag{2.14}$$

The direct result from Eq. (2.14), as well as (2.12) is the steady-state X vector

$$\dot{x}(t) = AX + bV_g = 0 \tag{2.15}$$

$$X = -A^{-1}\, bV_g \;;\; Y = C^T X \tag{2.16}$$

where $A \triangleq DA_1 + D'A_2$

$$b \triangleq Db_1 + D'b_2$$

$$C^T \triangleq DC_1^T + D'C_2^T \tag{2.17}$$

The next step is the perturbation of the variables according to:

$$v_g = V_g + \hat{v}_g \ , \ x = X + \hat{x} \ , \ y = Y + \hat{y} \tag{2.18}$$

$$d = D + \hat{d} \ , \text{ hence } d' = D' - \hat{d}$$

where capital letters denote steady-state values and carets represent superimposed ac perturbations. Substitution of Eq. (2.18) into (2.14) and elimination of the steady-state parts results in the following model:

$$\dot{\hat{x}} = A\hat{x} + b\hat{v}_g + [(A_1-A_2)X + (b_1-b_2)V_g]\hat{d} +$$

$$+ [(A_1-A_2)\hat{x} + (b_1-b_2)\hat{v}_g]\hat{d} \tag{2.19}$$

$$\hat{y} = C^T\hat{x} + (C_1^T-C_2^T)X\hat{d} + (C_1^T-C_2^T)\hat{x}\hat{d} \tag{2.20}$$

The last term in these equations, involve cross products of two input terms which explicitly exhibits nonlinearity. However, the nonlinearity may be avoided by putting a small-signal restriction on the perturbations such that the nonlinear terms become negligible compared with the other terms. Finally, a small-signal linear equation to describe the converter is obtained:

$$\dot{\hat{x}} = A\hat{x} + b\hat{v}_g + [(A_1-A_2)X + (b_1-b_2)V_g]\hat{d} \tag{2.21}$$

$$\hat{y} = C^T\hat{x} + (C_1^T - C_2^T)X\hat{d} \tag{2.22}$$

Equations (2.21) and (2.22) are the fundamental relations from which various transfer properties of switching converters can be derived. The Laplace transform of Eq. (2.21) is

$$s\hat{x}(s) = A\,\hat{x}(s) + b\hat{v}_g(s) + k\,\hat{d}(s) \tag{2.23}$$

where

$$k \triangleq (A_1 - A_2)X + (b_1 - b_2)V_g \tag{2.24}$$

Finally, the solutions for Eq. (2.23) are:

$$\frac{\hat{x}(s)}{\hat{v}_g(s)} = (sI - A)^{-1}\,b \tag{2.25}$$

$$\frac{\hat{x}(s)}{\hat{d}(s)} = (sI - A)^{-1}\,k \tag{2.26}$$

and

$$\frac{\hat{y}(s)}{\hat{v}_g(s)} = C^T(sI - A)^{-1}b \tag{2.27}$$

$$\frac{\hat{y}(s)}{\hat{d}(s)} = C^T(sI - A)^{-1}\,k + (C_1^T - C_2^T)X \tag{2.28}$$

Equation (2.27) is the input-voltage-to-output transfer function and Eq. (2.28) is the control-to-output transfer function. For regulation of the output, Eq. (2.28) is the transfer property of interest. A feedback loop around the converter contains the dynamics of both the converter and the compensation circuitry. The compensation is normally a linear circuit with no difficult analytical problems. So the problem of finding the loop gain of the regulator is essentially solved by calculation of the control-to-output transfer function of the converter.

2.2 Equivalent Circuit Representation

Equation (2.14) is the basis for the series of derivations leading to Eqs. (2.27) and (2.28). However, instead of the general mathematical route, one may use equivalent circuits; then, by treating each converter individually, considerable physical insight is achieved. The procedure is to construct an "averaged" circuit from the two linear circuits created by the switching action. So, one must take the steps to arrive at Eq. (2.14). This equation is the time-averaged model for the original two circuits, and a single equation governs the system. Then, the averaged circuit may be constructed from Eq. (2.14). Some manipulation may be necessary to put the equation in a suitable form. The next step is the perturbation and linearization of the model, all done on the equivalent circuit. The final result will be in a form from which many transfer properties of the converter can be obtained. In order to clarify the process, one simplified example

will be given. Figure 2.1a shows an ideal boost converter. Following the directions outlined in Section 2.1, one can easily find the averaged state-space equation for the circuit to be:

$$\begin{bmatrix} \frac{di}{dt} \\ \\ \frac{dv}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{d'}{L} \\ \\ \frac{d'}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i \\ \\ v \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ \\ 0 \end{bmatrix} v_g \qquad (2.29)$$

$$\dot{x} \qquad\qquad A \qquad\qquad x \quad + \quad b \quad v_g$$

In full, Eq. (2.29) becomes

$$V_g = L\frac{di}{dt} + d'v$$

$$d'i = C\frac{dv}{dt} + \frac{v}{R} \qquad (2.30)$$

Now, one reconstructs the average d circuit as in Fig. 2.1b. The circuit contains duty ratio-dependent voltage and current sources. The perturbation and linearization steps are next, done by separation of the sources into steady-state and small-signal ac sources. Figure 2.1c shows the resultant circuit in which the nonlinear parts are ignored. Notice the voltage source D'v and current source D'i. They represent a transformer action which, unlike the physical counterpart, retain operation even at dc. The basic function of a switching converter is this same dc transformation. After a few linear circuit transformations, the circuit of Fig. 2.1d is obtained. It comprises

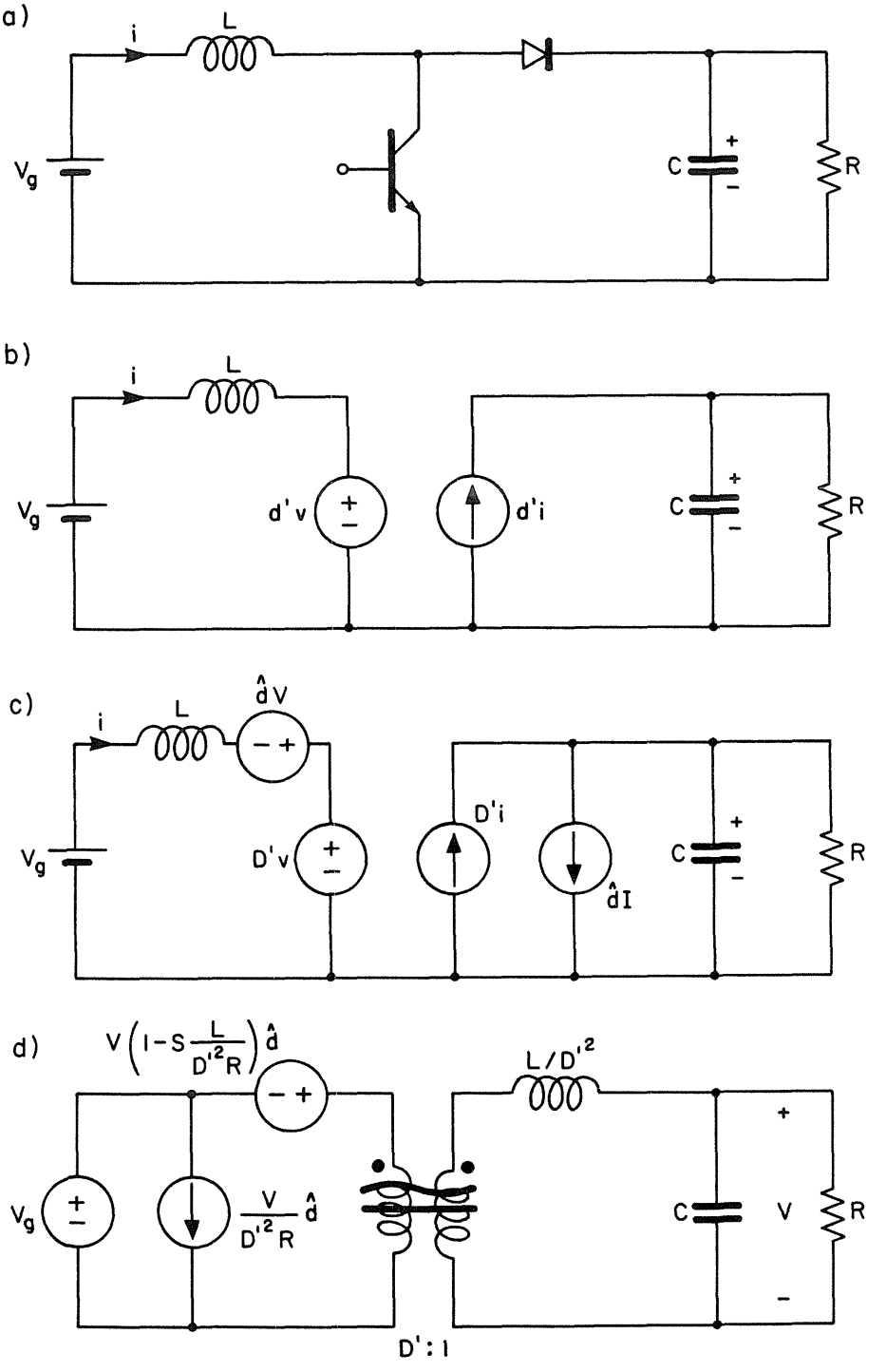


Fig. 2.1 *Equivalent circuit approach (a) ideal boost converter, (b) the averaged model, (c) perturbed and linearized model, (d) and the final form.*

the dc transformer, shown with the recently introduced transformer symbol with dc and ac signs; duty ratio-dependent sources to provide the control-induced perturbation; and a low-pass filter. It has been shown [1] that the small-signal equivalent for all dc-to-dc converters can be put into a form similar to Fig. 2.1d, with the same three-part structure. From Fig. 2.1d one can derive transfer properties such as input and output impedances, input-to-output transfer function, etc.

2.3 Modelling the Modulator

The other nonlinear part of the system is the modulator, where the disturbances in the control voltage are converted to duty-ratio modulations. As for converters, there are various types of modulators. The two most common versions are the "naturally sampled" modulator and the "sample-and-hold" modulator. The naturally sampled modulator is a comparator with one input connected to a sawtooth waveform while the other input is attached to the control voltage. The sample-and-hold modulator may be envisioned as a uniformly sampled modulator in which a sample-and-hold circuit is added between the control voltage and the comparator. This is done for noise reduction purposes or the cases where the signal is present in only a part of a cycle.

The frequency analysis of the modulators involves Fourier analysis of the output with a sine wave as control signal. This process, however, ignores inherent sampling effects present in both modulators. Now, if the control signal is in the following form:

$$\hat{v}_c = v_{cp} \sin(\omega t - \theta) \tag{2.31}$$

and the first harmonic of the duty ratio is

$$d = d_p \sin(\omega t - \theta - \phi_m) \tag{2.32}$$

the task becomes finding d_p and ϕ_m. The detailed derivation can be found in [3] and the results are summarized:

For the naturally sampled modulator: $$d_p = \frac{V_{cp}}{V_m} \tag{2.33}$$

where V_m is the height of the ramp and $$\phi_m = 0 \tag{2.34}$$

For the uniformly sampled modulator: $$d_p = \frac{V_{cp}}{V_m} \tag{2.35}$$

$$\phi_m = \omega D T_s = 2\pi D \frac{f}{f_s} \tag{2.36}$$

Equations (2.33) through (2.36) model the two types of modulators with respect to their small-signal first harmonic outputs by specifying their gain and phase. It shows the naturally sampled modulator to have a gain of $1/V_m$ and zero phase, whereas the uniformly sampled modulator, while having the same gain, exhibits a linear phase versus frequency and duty ratio. Therefore the small-signal transfer function of the modulator may be expressed in the

form

$$d = D + \hat{d} = \frac{V_c}{V_m} + \frac{\hat{v}_c}{V_m} e^{-j\phi_m} \tag{2.37}$$

where $\phi_m = 0$ for the naturally sampled modulator and $\phi_m = 2\pi D\, f/f_s$ for the uniformly sampled modulator.

With the assumption of a linear compensation circuit, this completes the modelling of the total regulator, since both the nonlinear parts of the loop are now characterized.

2.4 Review

Basic frequency domain analysis of switching converters is performed. The equations for the two switched circuits generated by the switching action are integrated to make a single equation that characterizes the dynamics of the system. The exact expression is then approximated to obtain a more revealing form. Finally, in a crucial averaging step, a simplified relation is obtained from which all the frequency domain transfer properties are extracted. Furthermore, the results can be worked out through a series of equivalent circuit transformations, wherein a physical understanding of the behavior of the converter is achieved. The modulator is also characterized by a simple gain function.

The total regulator system consisting of converter, modulator, and a linear compensation circuitry can therefore be analyzed very simply. Loop gain and any other transfer function of the regulator can be calculated, as will be demonstrated in the next chapter.

CHAPTER 3

GENERALIZED STATE-SPACE AVERAGING METHOD

So far, the state-space averaging method has been described in its original form. The method is simple enough to permit qualitative and quantitative evaluation of first-order effects upon the converter dynamics. Therefore, only the essential features, namely the dc-to-dc conversion, low-pass filtering, and the control function are present. On the other hand, the model is accurate enough to allow refinements through inclusion of second-order effects (parasitic resistances, switch nonidealities, etc.), which in some cases cause even large qualitative changes. However, the purpose of the analytical calculations — finding simple and revealing answers — can be quickly lost, as more second order effects are considered in the calculations. At this stage, one may resort to computerized implementation of the model.

This chapter will first describe the generalized state-space averaging method, whose general form of input and output vectors provides greater accuracies with direct calculations. One added feature is that accuracy of the small-signal ac performance is consistent with the increased accuracy of the dc results. The main features of the simpler model are still transparent as a check point for the refined model. The method is described in well defined steps

to lead to the final dc and ac results from the two original switched networks. The model is implemented on a computer by a dedicated program to analyze any switching dc-to-dc converter. This special purpose Switching Converter Analysis Program (SCAP) requires the computational power of only a small desktop computer, as opposed to large mainframes needed by general purpose programs. Still, the results of this program are in closed form (transfer functions, poles, zeros, frequency responses).

Next, the response of the converter along with the feedback compensation network is considered to predict the closed-loop behavior of regulators as well as various open-loop responses and loop gain. This feature is also included in the Switching Converter Analysis Program.

Frequency response measurements in the noisy environment of switching power supplies pose some difficulties which are treated next. A solution is introduced which relies on a computer-controlled network analyzer for quick and accurate results. An example clarifies the feature of these design methods.

3.1 Extended State-Space Averaging

The method of state-space averaging was introduced to characterize the steady-state dc and small-signal ac properties of switching converters. The technique has been verified to be accurate in describing duty ratio and input voltage transfer characteristics. In the simplified version presented in Chapter 2, the system contained

only one independent voltage source v_g. The general case, however, can include many independent voltage or current sources, some of them also being modulated and some not. For example, inclusion of transistor saturation voltage V_s and diode forward drop V_F, instead of the ideal switch model, would certainly lead to more accurate steady-state and dynamic results. Obviously they would not be modulated. However, addition of an ac current generator at the converter output, and evaluation of the output voltage as a response, would permit prediction of the converter's output impedance. Thus in general the input vector u can consist of several independent voltage and current sources. In addition, instead of a single output, one may be interested simultaneously in two or more different outputs such that $y = Cx$ where y is a vector and C is a matrix. Finally the output may have parts dependent on the input vector, and hence the output equations take the general form $y = Cx + Eu$.

The problem can be formulated as follows:

interval dT_s:

$$\dot{x} = A_1 x + B_1 u \tag{3.1}$$

$$y = C_1 x + E_1 u \tag{3.2}$$

interval $d'T_s$:

$$\dot{x} = A_2 x + B_2 u \tag{3.3}$$

$$y = C_2 x + E_2 u \tag{3.4}$$

in which the previous input vectors b_1 and b_2 became input matrices

B_1 and B_2. Note that unequal matrices C_1 and C_2 imply discontinuous entities such as pulsating currents.

A similar process as in Chapter 2 may be performed where the averaging step defined in Eq. (2.14) is still valid. The averaging process combines the Eqs. (3.1) to (3.4) and generates a single matrix differential equation, whose perturbation by

$$x = X + \hat{x} \qquad u = U + \hat{u}$$

$$d = D + \hat{d} \qquad y = Y + \hat{y} \tag{3.5}$$

results in the steady-state and small-signal ac characteristics as

steady-state:

$$X = - A^{-1}BU \tag{3.6}$$

$$Y = CX + EU \tag{3.7}$$

where

$$A = DA_1 + D'A_2$$

$$B = DB_1 + D'B_2$$

$$C = DC_1 + D'C_2$$

$$E = DE_1 + D'E_2 \tag{3.8}$$

small-signal ac:

$$\dot{\hat{x}} = A\hat{x} + B\hat{u} + [(A_1-A_2)X + (B_1-B_2)U]\hat{d} \tag{3.9}$$

$$\hat{y} = C\hat{x} + E\hat{u} + [(C_1-C_2)X + (E_1-E_2)U]\hat{d} \tag{3.10}$$

various duty ratio to state variables and input to state variable transfer properties can easily be derived as

$$\hat{x}(s) = (sI-A)^{-1}k\,\hat{d}(s) + (sI-A)^{-1}\,B\,\hat{u}(s) \qquad (3.11)$$

where

$$k = (A_1-A_2)X + (B_1-B_2)U \qquad (3.12)$$

Finally the output transfer functions are:

$$\frac{\hat{y}(s)}{\hat{d}(s)} = C(sI-A)^{-1}k + (C_1-C_2)X + (E_1-E_2)U \qquad (3.13)$$

and

$$\frac{\hat{y}(s)}{\hat{u}(s)} = C(sI-A)^{-1}B + E \qquad (3.14)$$

Note that in (3.14) $\hat{u}(s)$ is a vector consisting of individual perturbations $u^T(s) = [\hat{u}_1(s), \hat{u}_2(s), \ldots]$. Thus $\hat{y}/\hat{u}$ is a vector which contains transfer functions $\hat{y}/\hat{u}_1$, $\hat{y}/\hat{u}_2$ ..., which are the system's response to perturbation of each individual member $\hat{u}_i$ of the input vector.

The extended version is now demonstrated on a buck converter with a number of parasitic elements included such as transistor and diode voltage drops V_s, V_F, and parasitic resistance R_ℓ of the inductor as shown in Fig. 3.1a. The input vector now has three components, so the x and u vectors are defined as

$$x = \begin{bmatrix} i \\ \\ v \end{bmatrix} \qquad u = \begin{bmatrix} v_g \\ V_s \\ V_F \end{bmatrix} \qquad (3.15)$$

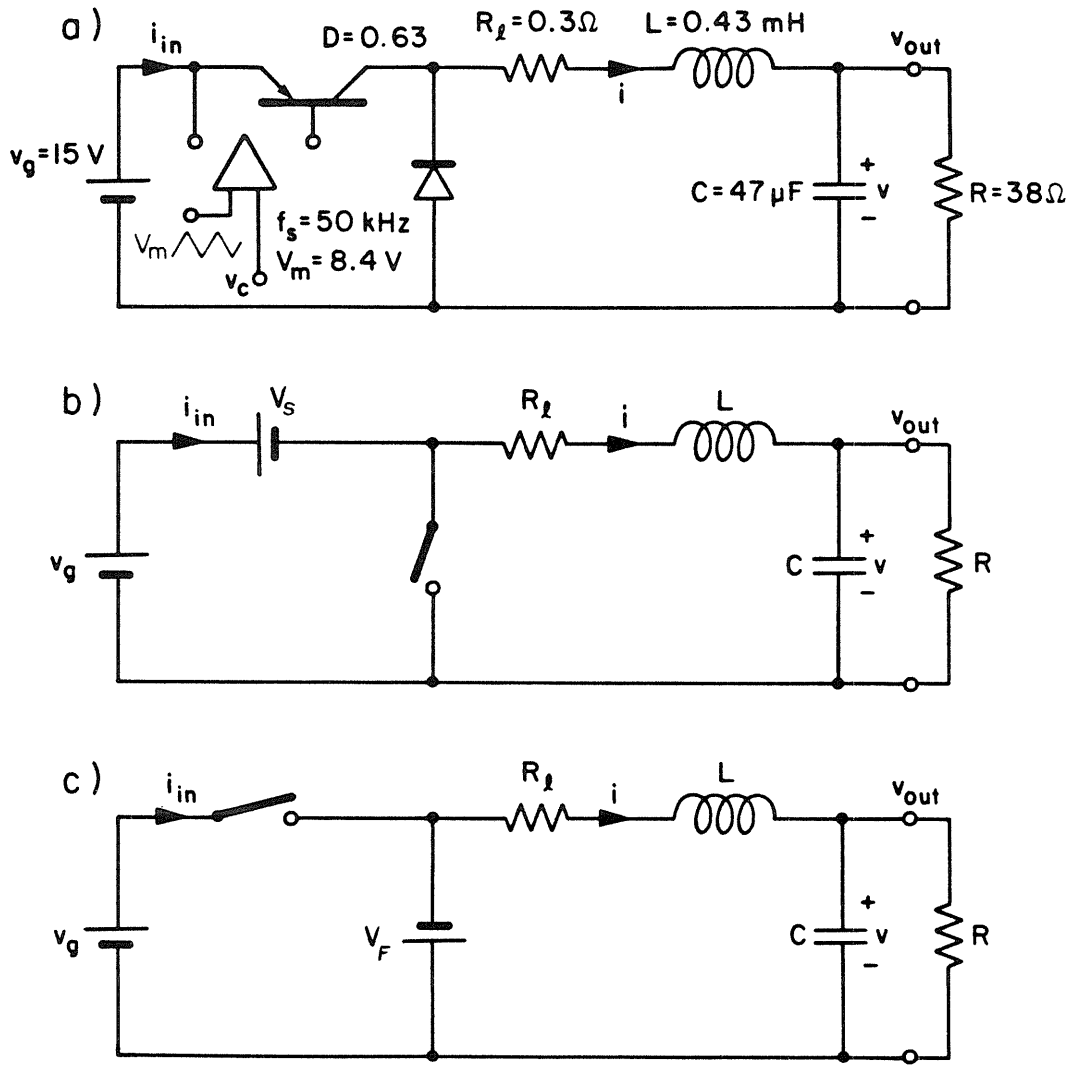


Fig. 3.1 *Use of generalized state-space averaging method. (a) The actual circuit, resultant circuit when transistor is (b) on, and (c) off.*

When the transistor is turned ON, Fig. 3.1b results in

$$\begin{bmatrix} \frac{di}{dt} \\ \\ \frac{dv}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_\ell}{L} & -\frac{1}{L} \\ \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i \\ \\ v \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & -\frac{1}{L} & 0 \\ \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_g \\ V_s \\ V_F \end{bmatrix} \tag{3.16}$$

$$\dot{x} = A_1 x + B_1 u$$

When the transistor is OFF, Fig. 3.1c results in

$$\begin{bmatrix} \frac{di}{dt} \\ \\ \frac{dv}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_\ell}{L} & -\frac{1}{L} \\ \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i \\ \\ v \end{bmatrix} + \begin{bmatrix} 0 & 0 & -\frac{1}{L} \\ \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_g \\ V_s \\ V_F \end{bmatrix} \tag{3.17}$$

$$\dot{x} = A_2 x + B_2 u$$

Averaging Eqs. (3.16) and (3.17) over one switching cycle and solving for steady state conditions gives the output voltage v as:

$$v = \frac{DV_g - DV_s - D'V_F}{1 + \frac{R_\ell}{R}} \tag{3.18}$$

The efficiency P_{out}/P_{in} is

$$\eta = \frac{1 - \frac{V_s}{V_g} - \frac{D'}{D}\frac{V_F}{V_g}}{1 + \frac{R_\ell}{R}} \tag{3.19}$$

which suggests low efficiencies at low duty ratios.

A more accurate calculation of dc quantities, as Eq. (3.13) suggests, can also result in a more precise prediction of the dynamics of the system. The final steady-state and dynamic models (3.6, 3.7) and (3.13, 3.14) are specified in terms of matrix and vector operations on the original converter descriptions (3.1 to 3.4). Therefore, all that is needed for a complete solution is the description of the two linear networks obtained for each position of the switch through quadruples (A_1, B_1, C_1, E_1) and (A_2, B_2, C_2, E_2). Next, a computer program is described which is used to do the mathematical operations.

3.2 The Switching Converter Analysis Program

Increased accuracy of the prediction requires incorporation of second-order parasitic circuit elements in the model. However, inclusion of these parasitics makes the analytical calculations rapidly grow tedious as the number of the parasitics and the order of the system get larger. Also, the final results are not easy to interpret. This section introduces a computer program, based on the generalized state-space averaging technique, which is capable of computing various open-loop and closed-loop characteristics of switching converters. The program is written for implementation on small computers, and is a compromise between a full nonlinear analysis of the system and oversimplified analytical methods. So far the program has been implemented on the HP 9845A and HP 9826 desktop computers. The Switching Converter Analysis Program (SCAP) provides increased accuracy,

yet, the results can be analytically checked with the simplified model by removal of the parasitics. It also provides capability of theoretically closing the loop around the converter. So, complex multiple-loop feedback and feedforward methods can be simulated and tested for the required specifications.

Section 3.1 described part of the mathematical techniques that are in the form of matrix operations and are suitable for numerical manipulations. The state-space matrices are the inputs of the program where, in order to simplify the format of the input data, the extended forms are used:

interval dT_s:

$$P\dot{x} = A_{11}x + B_{11}u \quad ; \quad A_1 = P^{-1}A_{11} \quad ; \quad B_1 = P^{-1}B_{11} \tag{3.20}$$

interval $d'T_s$:

$$P\dot{x} = A_{22}x + B_{22}u \quad ; \quad A_2 = P^{-1}A_{22} \quad ; \quad B_2 = P^{-1}B_{22} \tag{3.21}$$

where P usually consists of capacitance and inductance values, and A_{11}, A_{22}, B_{11}, and B_{22} now contain only resistive and dimensionless entities. This form provides less interaction of the circuit components on the matrix elements.

A flow chart of the SCAP is shown in Fig. 3.2. Note that the same program can be used for both the open-loop as well as the closed-loop response of converters. For open-loop considerations, the blocks denoted by asterisks are bypassed, since they are used only for closed-loop analysis. At the first block, the input data are read and A_1, A_2, B_1, and B_2 are calculated. The averaging process is performed

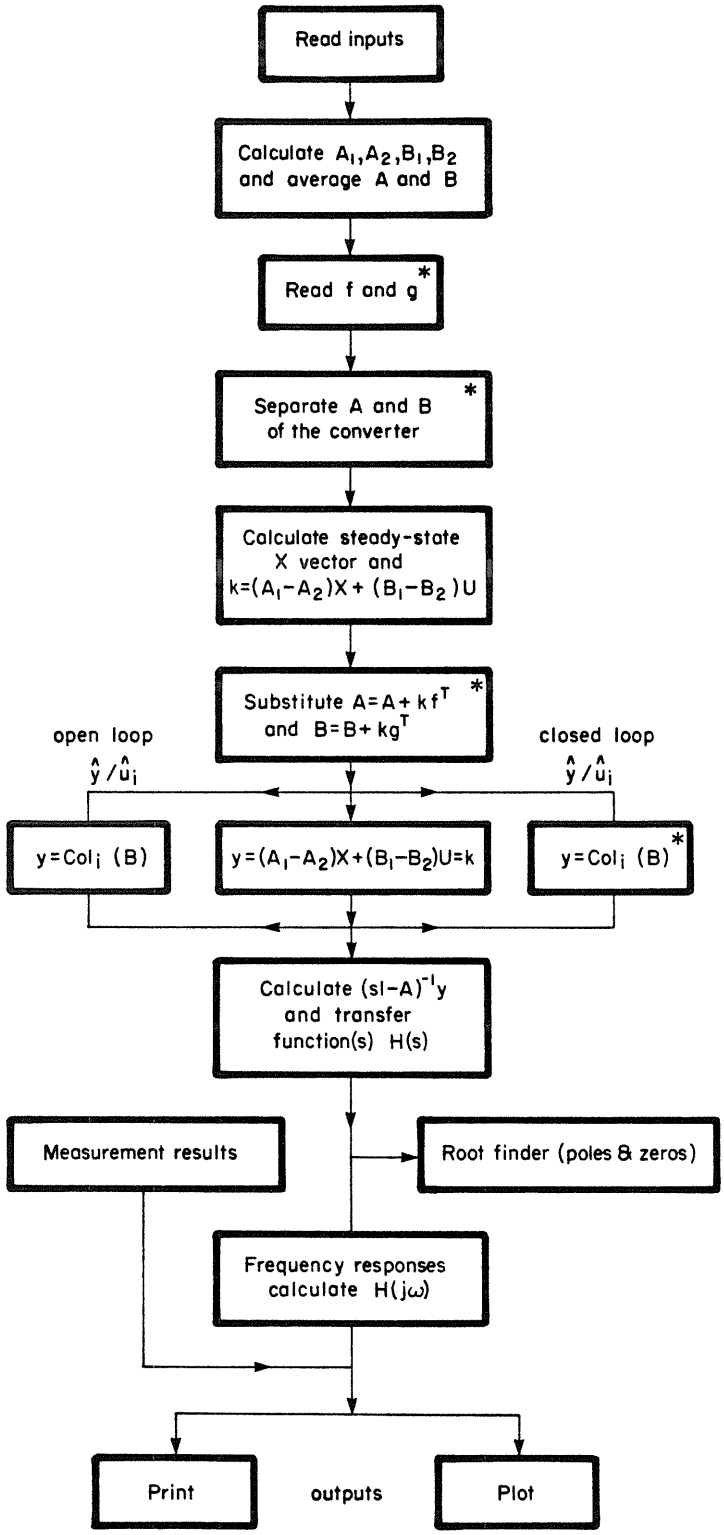


Fig. 3.2 Flowchart of Switching Converter Analysis Program (SCAP): blocks with asterisks are used in closed-loop calculations only.

and the average matrices of the system, A and B, are found. The next block finds the steady-state X vector by use of (3.6). Then, any of the $\hat{x}/\hat{d}$ or $\hat{x}/\hat{u}_i$ can be calculated by selection of different routes. The transfer functions are calculated via Leverrier's algorithm. The technique uses real n x n matrices $F_1, F_2, \ldots F_n$ and scalars $\theta_1, \theta_2, \ldots \theta_n$ as follows:

$$F_1 = I \qquad \theta_1 = - \text{ tr } AF_1/1$$

$$F_2 = AF_1 + \theta_1 I \qquad \theta_2 = - \text{ tr } AF_2/2 \tag{3.22}$$

$$F_n = AF_{n-1} + \theta_{n-1} I \qquad \theta_n = - \text{ tr } AF_n/n$$

Then

$$(sI-A)^{-1} = \frac{s^{n-1} F_1 + s^{n-2} F_2 + \ldots sF_{n-1} + F_n}{s^n + \theta_1 s^{n-1} + \ldots \theta_{n-1} s + \theta_n} \tag{3.23}$$

and

$$AF_n + \theta_n I = 0 \tag{3.24}$$

The last equation is used to check the method. As can be noted, the technique is not iterative and requires only n matrix multiplications and therefore, is well suited for small computer applications. However, due to inherent inaccuracy of the method, in cases of ill-conditioned matrices — those with widely separated eigenvalues — the method check can fail. Nevertheless, this is not usually so, and in the majority of cases very reasonable accuracies (better than 0.01%)

are obtained.

The general case of (3.23) requires a large storage. To reduce this requirement, the desired transfer functions are calculated during the process of (3.22) by immediate multiplication of F matrices to C matrix and a vector of k or a column of B matrix. Thus one of the transfer functions of Eq. (3.11) is obtained

$$\text{Transfer function} = \begin{bmatrix} (sI-A)^{-1}k \\ \\ (sI-A)^{-1}b_i \end{bmatrix} = \frac{g_{0i}+g_{1i}s+g_{2i}s^2 \ \cdots \ g_{n-1i}s^{n-1}}{b_0+b_1s+b_2s^2 \ \cdots \ b_ns^n}$$

$$b_i = \text{col}_i(B) \tag{3.25}$$

where

$$b_0 = \theta_n,\ b_1 = \theta_{n-1},\ \cdots\ b_n = 1 \quad \text{and} \quad g_0 = \begin{bmatrix} F_n & k \\ \\ F_n & b_i \end{bmatrix},$$

$$g_{1i} = \begin{bmatrix} F_{n-1} & k \\ \\ F_{n-1} & b_i \end{bmatrix}, \quad \cdots \quad g_{n-1i} = \begin{bmatrix} F_1 & k \\ \\ F_1 & b_i \end{bmatrix} \tag{3.26}$$

The final transfer functions calculated from one of Eqs. (3.13) or (3.14) and is in the form

$$H(s) = \frac{a_0 + a_1s + a_2s^2 + \ldots}{b_0 + b_1s + b_2s^2 + \ldots} \tag{3.27}$$

The poles of the system are the roots of the denominator polynomial. The roots of the numerator polynomials are the zeros of the specific output. A root finder is implemented which optionally determines the poles and zeros of the system. Finally, the frequency response in the desired frequency range is calculated, which can be outputed either numerically or as a Bode plot. Overlaying the plots to check different versions of a design or to compare theoretical and measurement results is also possible.

3.3 Closed-Loop Response Prediction

As discussed so far, the state-space averaging method has been used to predict the open-loop characteristics of converters. However, converters are usually used as controlled sources — regulators — with feedback loop(s) around them.

The feedback loop itself may contain some reactive components, hence increasing the order of the system. The input data for the closed-loop system, then, must be upgraded to include the additional state variables introduced by the compensation network. Therefore, the system will have modified state and input vectors

$$x = \begin{bmatrix} x_c \\ \\ x_L \end{bmatrix} \quad ; \quad u = \begin{bmatrix} u_c \\ \\ u_L \end{bmatrix} \tag{3.28}$$

where x_c is the original converter state variables and vector x_L contains the compensation network states. Similarly u_c is the input vector to

the converter and u_L is the optional reference voltages and reference currents of the loop. The A and B matrices are also upgraded to include dynamics of the loop, effect of the converter on the feedback network and vice versa.

The feedback determines the changes in the duty ratio in response to disturbances in the converter's states and the inputs to the system. The general format is

$$\hat{d} = f^T\hat{x} + g^T\hat{u} \tag{3.29}$$

where f is the feedback gain vector to determine the gains assigned to each of the states controlling the loop, which can of course be used in the analysis of total-state feedback systems. The g vector is the feedforward gain vector to provide direct access of the inputs of the system to duty ratio, which can be used to improve the overall performance. Substitution of Eq. (3.29) into the open-loop system characteristics of Eq. (3.13) results in:

$$\dot{\hat{x}} = (A + kf^T)\hat{x} + (B + kg^T)\hat{u} \tag{3.30}$$

and

$$\hat{y} = (C + zf^T)\hat{x} + (E + zg^T)\hat{u} \tag{3.31}$$

where

$$z = (C_1 - C_2)X + (E_1 - E_2)U \tag{3.32}$$

Laplace transformation and rearrangement yields

$$\frac{\hat{x}(s)}{\hat{u}(s)} = (sI - A - kf^T)^{-1} (B + kg^T) \tag{3.33}$$

and

$$\frac{\hat{y}(s)}{\hat{u}(s)} = (C + zf^T) (sI - A - kf^T)^{-1} (B + kg^T) + E + zg^T \tag{3.34}$$

Equation (3.34) describes the general small-signal closed-loop behavior of any switched-mode regulator with the f vector for the feedback gains, and g vector to describe the feedforward gains of the system. In the flowchart of Fig. 3.2 the blocks marked with asterisks are those which involve modifications necessary in calculation of the closed-loop response of switching converters. The f and g vectors must be supplied in addition to the rest of the input matrices. The loop may contain circuitry which is open-loop unstable (e.g. an integrator). Special precautions are taken for such cases and the steady-state X vector of the converter alone X_c is calculated. The A matrix is replaced by $A + k^T f$ and the B by $B + k^T g$. Finally the closed-loop transfer functions are calculated according to (3.34). The rest of the calculation is identical to the open-loop calculations. In the SCAP, the formulas are simplified by the assumption $E_1 = E_2 = E$.

From the system theory one can show that, by proper selection of the f vector, the poles of the closed-loop system can be placed anywhere in the complex s-plane, to create a highly flexible

closed-loop converter. However, the degree of validity of the approximation made so far, and practical constraints, limit the extent of this pole placement. Also, the feedforward vector g, can be used to manipulate the zeros of a designated transfer function.

3.4 Frequency Response Measurement Program

After a system is designed with the modelling technique, it is desired to accurately measure the response of the system to external perturbations to ensure that the system operates in accordance with the analytical prediction. Also, in case of a disagreement, results of the measurement will supply information upon which the design correction can be based. This section covers a practical method of measuring the transfer properties of open-loop and closed-loop systems. The same technique can be applied to measurement of loop gain of a feedback system by injection of a test signal into the closed-loop, as discussed in [2].

Transfer function and loop gain measurements are described in which a sophisticated network analyzer system is employed to give readouts of magnitude and phase directly, and which can be automated by computer control.

The measurement problem is considerably difficult in the switching regulators. Here, even a small-signal perturbation of control signal at a single frequency f generates an output which contains a multitude of frequencies: the fundamental signal at frequency f and its harmonics 2f, 3f, etc.; the switching ripple at the switching frequency

f_s and its harmonics $2f_s$, $3f_s$, etc.; and finally, output at frequencies which are sums and differences, such as $f_s + f$, $f_s - f$, etc. (side-bands).

For measurements on ordinary "linear" circuits, separate test signal oscillator and wideband voltmeter instruments can be used. However, for measurements on switched-mode converters and regulators, it is absolutely essential to have a narrowband voltmeter to avoid the small test signal being completely swamped by the switching noise. Although such voltmeters are available, it is considerably more convenient to use an instrument that combines the functions of test signal oscillator and narrowband voltmeter in such a way that the voltmeter bandpass automatically tracks the frequency of the oscillator output. This combination is a wave analyzer.

Use of the automatically tracking narrowband voltmeter enormously increases the available dynamic range for small-signal transfer function measurements, and makes possible measurement of the line-to-output and control-to-output transfer functions of switched-mode converters. Indeed, measurements can be made of the two components of the control transfer function, the control-to-duty ratio transfer function of the modulator, and the duty ratio-to-output transfer function of the power stage. This is accomplished by measurement of the pulse-width-modulated switching waveform of the modulator output: the voltmeter narrowband extracts the pwm test frequency, whose magnitude and phase can be determined by the described technique.

One such system is the HP3040A network analyzer, which is composed of an HP3330B waveform synthesizer and an HP3570A wave analyzer. The synthesizer generates sine waves with selected frequency and amplitude. The process is totally accomplished by digital means, and the selection of frequency and amplitude is made on the front panel keyboard. The analyzer has two inputs, each with a narrow-band tracking filter, which are used in amplitude measurement in noisy situations common to switching converters. The outputs of these filters are converted to dB (with respect to selectable references) and then subtracted to get the amplitude of the response.

Another section of the analyzer is an exclusive phase-meter that measures the phase difference between the two inputs by digital techniques. A digital display represents the magnitude of the response in dB and the phase in degrees. Fig. 3.3 shows the network analyzer system.

The task of frequency response measurement in the manual mode is now simplified to keying-in of the specified frequency with an acceptable amplitude and the reading out of the magnitude and the phase of the response. For complete measurement, this process is repeated for the entire desired frequency range. The improvement in speed and accuracy over conventional set-ups is quite remarkable.

Furthermore, in the automatic mode, a computer can be attached to the network analyzer as an active controller. The interactive program, Automatic Measurement System (AMS), first presets all the proper network analyzer parameters and then sweeps the desired frequency range

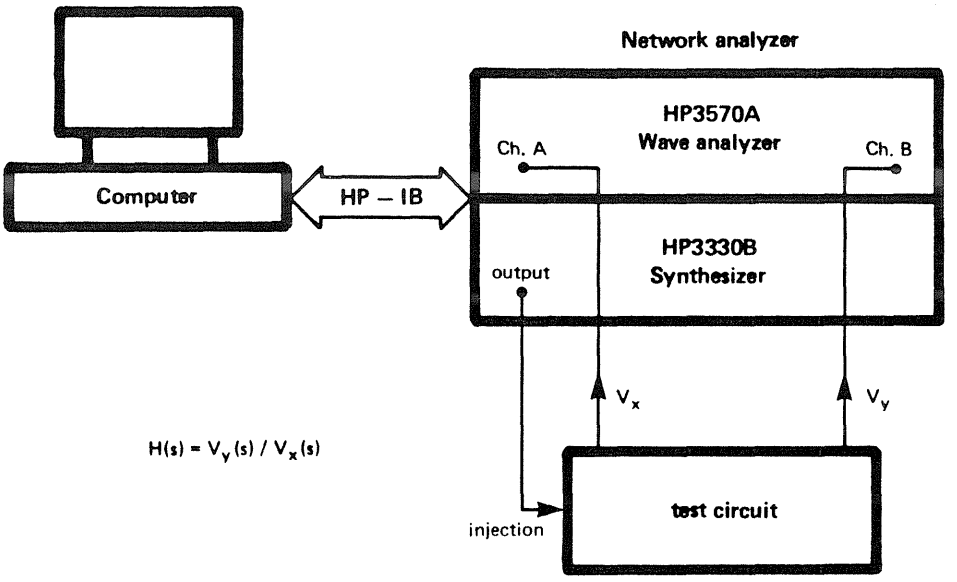


Fig. 3.3 *Automated frequency response measurement system composed of frequency synthesizer, wave anaylzer, and computer as controller.*

with steps which are equally spaced on a logarithmic scale. At each discrete frequency, the program waits for a specified time for the total system (network analyzer and circuit under test) to recover from transients and then measures each of the two inputs of the analyzer a given number of times. The measurements of the amplitude and phase are then averaged.

Many protective features are included. The output voltage of the synthesizer can be limited such that in open-loop measurements, the signal injection (duty ratio modulation) is controlled and hence possible damage to the system due to large perturbation is prevented. This injection voltage is altered subject to many other conditions. If either of the analyzer's inputs has magnitude below a specified value, the injection voltage is increased to improve the signal to noise ratio. In the same way, input magnitudes above given values cause a decrease of the injection voltage. This feature has been found very useful in limiting the perturbation level in closed-loop measurements. A phase reading in excess of $\pm$ 160 degrees causes a change of the phase reference, while the computer keeps track of the phase-jumps by adding or subtracting 180 degrees to or from the actual phase reading. This provides continuous phase readout.

At each frequency the magnitude and the phase of the response are averages of several measurements done by the analyzer. If the standard deviation of the readings is more than a given value (e.g. in the presence of excessive noise), then the results are rejected. The injection voltage is increased for improved signal to noise ratio and

the measurement is repeated until consistency is obtained. If in spite of increasing the injection to its maximum level, the desired consistency is not observed, a warning is issued by the computer and the measurement is continued at the next frequency. The measurement sequence can be interrupted at any time and some values can be changed interactively. The results are stored in the memory and can be printed, plotted, or stored on the tape for reference to this or other programs (such as theoretical prediction programs). The plotting routine allows multiple overlaying of the results of several measurements (as long as the plots are distinguishable), so that comparison of different versions of a design is possible. As an example of acquired speed, a typical automatic 50-point measurement takes only 25 seconds. Furthermore the interactive nature of the program makes it easy to use, and no special programming skills are necessary for operation.

3.5 Example: Closed-Loop Buck Converter

The input-to-output and input admittance transfer functions of the buck converter of Fig. 3.4 are examined, to clarify the generalized state-space averaging, and the capabilities of the SCAP. The result will be compared with the computer-controlled measurements performed on the actual hardware. The circuit comprises a damping network (r,C_2), and an integral feedback, and so the entire regulator has four states:

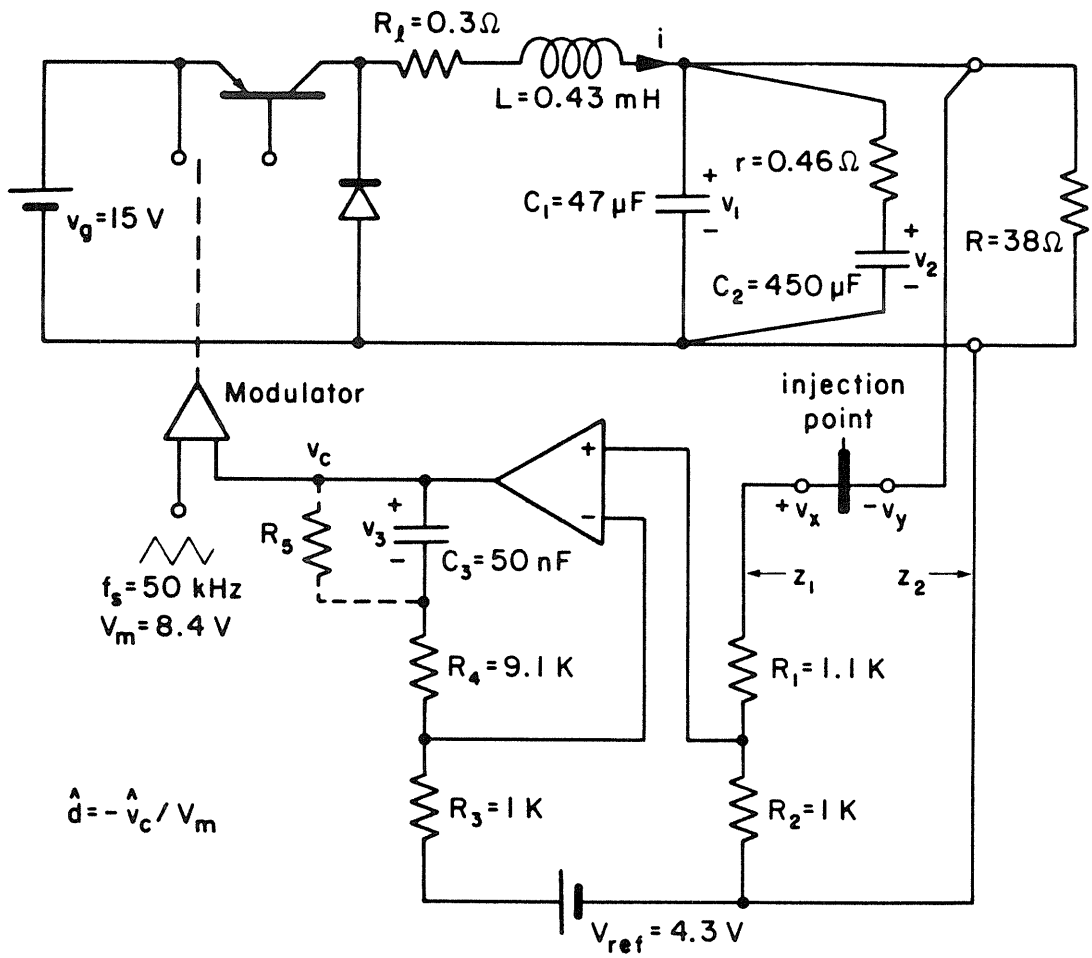


Fig. 3.4 Closed-loop buck example.

$$x = \begin{bmatrix} i \\ V_1 \\ V_2 \\ -- \\ V_3 \end{bmatrix} = \begin{bmatrix} x_C \\ \\ -- \\ x_L \end{bmatrix} \quad ; \quad u = \begin{bmatrix} v_g \\ \\ v_{ref} \end{bmatrix} \quad ; \quad y = \begin{bmatrix} V_{out} \\ \\ i_{in} \end{bmatrix} \tag{3.35}$$

During interval dT_s

$$V_g = R_\ell\, i + L\,\frac{di}{dt} + v_1 \tag{3.36a}$$

$$C_1\,\frac{dv_1}{dt} = i - \frac{v_1 - v_2}{r} - \frac{V_1}{R} \tag{3.36b}$$

$$C_2\,\frac{dv_2}{dt} = \frac{v_1 - v_2}{r} \tag{3.36c}$$

$$C_3\,\frac{dv_3}{dt} = \left(v_1\,\frac{R_2}{R_1 + R_2} - v_{ref}\right)/R_3 - \frac{v_3}{R_5} \tag{3.36d}$$

The modified state-space matrices are found to be

$$P = \begin{bmatrix} L & 0 & 0 & 0 \\ 0 & C_1 & 0 & 0 \\ 0 & 0 & C_2 & 0 \\ 0 & 0 & 0 & C_3 \end{bmatrix} \qquad A_{11} = \begin{bmatrix} -R_\ell & -1 & 0 & 0 \\ 1 & -\frac{1}{R\,||\,r} & \frac{1}{r} & 0 \\ 0 & \frac{1}{r} & -\frac{1}{r} & 0 \\ 0 & \frac{R_2}{R_3(R_1+R_2)} & 0 & -\frac{1}{R_5} \end{bmatrix}$$

$$B_{11} = \begin{bmatrix} 1 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & -\frac{1}{R_3} \end{bmatrix} \quad C_1 = \begin{bmatrix} 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 \end{bmatrix} \quad E_1 = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \tag{3.37}$$

Similarly during $d'T_s$, Eq. (3.36) holds except (3.36a) which becomes:

$$0 = R_\ell i + L\frac{di}{dt} + V_1 \tag{3.38}$$

Hence,

$$A_{22} = A_{11} \; ; \quad B_{22} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & -\frac{1}{R_3} \end{bmatrix} \; ; \quad C_2 = \begin{bmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}$$

$$E_2 = E_1 \tag{3.39}$$

Notice that the integral function of the feedback network provides very high gains at low frequencies. The effective finite open-loop gain of the operational amplifier is modelled by a large resistor R_5 in parallel with C_3. The feedback control output is

$$v_c = V_1 \frac{R_2}{R_1 + R_2}\left(1 + \frac{R_4}{R_3}\right) + V_3 - V_{ref}\frac{R_4}{R_3} \tag{3.40}$$

so that the f and g vectors are recognized as

$$f = -\frac{1}{v_m}\begin{bmatrix} 0 \\ \frac{R_2}{R_1 + R_2}\left(1 + \frac{R_4}{R_3}\right) \\ 0 \\ 1 \end{bmatrix} \quad ; \quad g = -\frac{1}{v_m}\begin{bmatrix} 0 \\ -\frac{R_4}{R_3} \end{bmatrix} \tag{3.41}$$

Proper numerical values are calculated from Fig. 3.4 and the data are fed to the SCAP. The thick lines of Fig. 3.5a indicate the outcome for v_{out}. The thin lines are the corresponding measurement results taken by use of the AMS (Automatic Measurement System), which confirm the theoretical predictions. The second output is the response of the input current due to disturbances of the input voltage, i.e. the closed-loop input admittance of the regulator. The theoretical and experimental results are superimposed as shown in Fig. 3.5b with thick and thin lines respectively. Notice that at low frequencies, the 180 degrees phase of the response indicates a *negative* input admittance. Connection of an LC filter to the input port of the closed-loop regulator — for current ripple and EMI reduction purposes — owing to this negative input admittance can cause the total system to oscillate. Special techniques must be employed to resolve this type of problem [14,15].

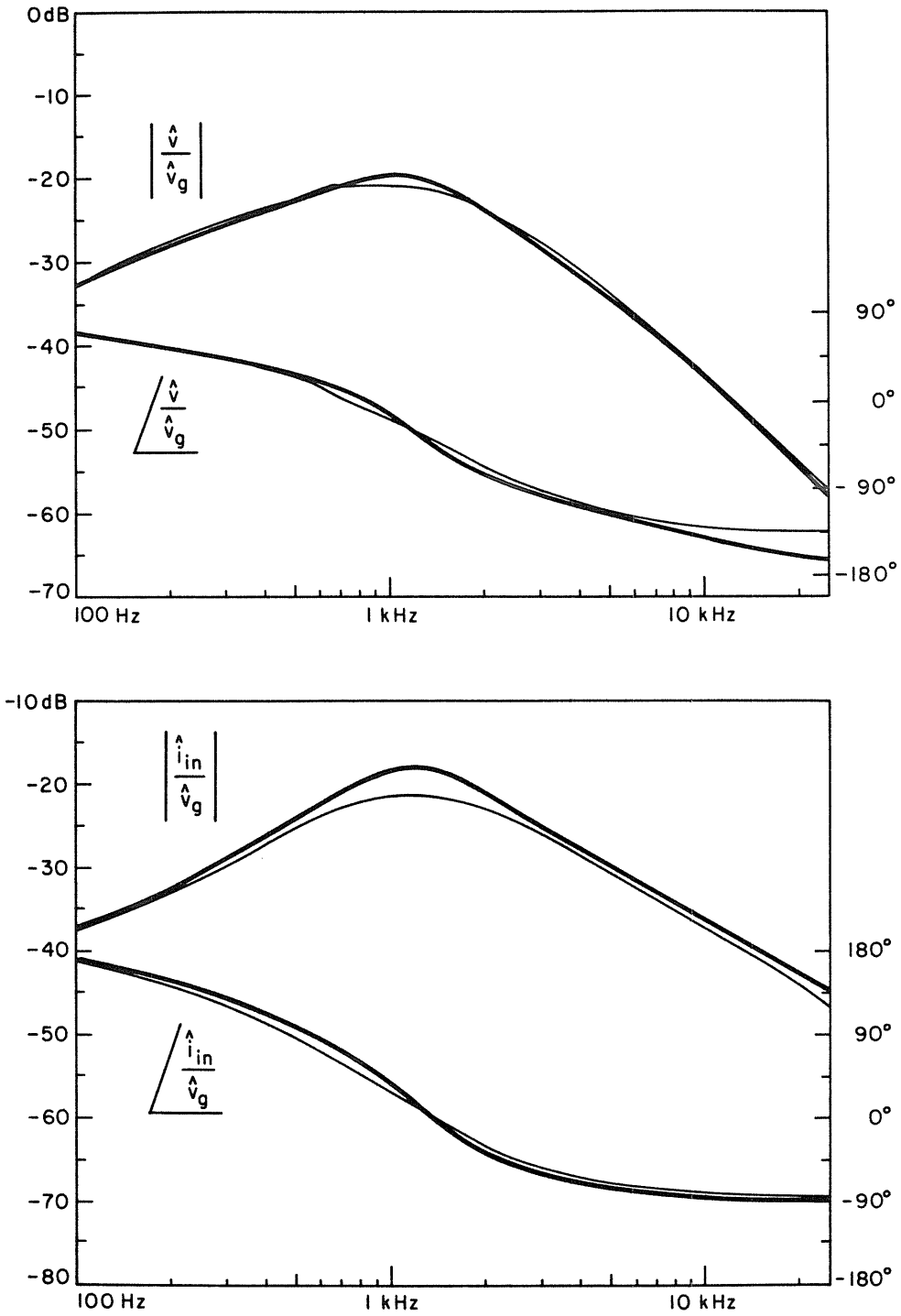


Fig. 3.5 *Comparison of the prediction (thick lines) and the measurement (thin lines) result on buck regulator of Fig. 3.4. (a) Closed-loop audio susceptibility, (b) closed-loop input admittance. Notice the phase-shift at low frequencies which denotes a negative impedance.*

Table 3.1. Poles and zeros of closed-loop $\hat{v}_{out}/\hat{v}_g$ and $\hat{i}_{in}/\hat{v}_g$ calculated by SCAP.

Poles		Zeros of $\hat{v}_{out}/\hat{v}_g$		Zeros of $\hat{i}_{in}/\hat{v}_g$	
F	Q	F	Q	F	Q
6.85 kHz	Real	888 Hz	Real	7.68 kHz	Real
1.17 kHz	0.89	3.18 Hz	Real	203 Hz	Real RHP
269 Hz	Real			114 Hz	Real

3.6 Review

The basic state-space averaging method was extended to handle more than one output. This generalization allows inclusion of many second-order effects to increase the accuracy of prediction of the steady-state dc as well as small-signal characteristics of switching converters. The output matrix is also put in a more general form to improve the flexibility of the technique. The output impedance and many other characteristics of the converter can now be directly calculated from the equations, as opposed to the original technique where, for the same task, only the equivalent circuits could have been used.

Next, a computer program was introduced that, thanks to the generalized state-space averaging technique, requires only the small processing power nowadays found in any small and even desktop computer. The state-space matrices of the two switched networks of the converter are fed to the program to find accurate steady-state conditions and many frequency transfer properties. The general form of the output allows calculation of the frequency response of even pulsating quantities.

The closed-loop behavior of the converter was analyzed and consideration of the total regulator enables prediction of various closed-loop transfer properties such as input and output impedances, input-to-output transfer function, and loop gain.

Next, another program was introduced to perform fast and accurate frequency domain measurements on the actual converter hardware by a

computer-controlled network analyzer. The results are used to experimentally verify the predicted performance and to provide clues for probable refinements of the original design. Close agreement of the prediction and the measurement of a buck regulator illustrated the accuracy and usefulness of the methods.

CHAPTER 4

CONCLUSION

In order to clarify the analysis to be done in the rest of this work, the state-space averaging approach to modelling of dc-to-dc converters was described. The technique can be used to analyze any two-topology converter via state-space descriptions of the linear circuits generated by the switching action. The state-space equations are integrated during each interval to find a single equation to relate the states at the beginning of a cycle to the states at the end of that cycle. By a series of approximations, the resultant equation is simplified to a nonlinear equation which describes the dynamics of the system. This equation has the same state-space form as the original two equations in which each matrix is the time average of the two original matrices. The steady-state condition of the converter is directly obtained from this equation. With the equation linearized by the small-signal restrictions, the dynamics of the system may now be analytically obtained by the usual Laplace transform techniques. The control-to-output transfer functions are those entering the feedback loop-gain calculations directly.

The model is simple enough to provide analytical results for an initial paper design, yet powerful enough to allow improvement of the accuracy by inclusion of second-order effects. However, analytical

prediction of the dynamics quickly becomes difficult as more parasitics are included in the model, or the order of the system is increased. The state-space averaging method is first generalized for utilization of many input sources and a general form of output. For dc steady states, more accurate results are obtained while now many ac transfer functions, previously derived only by the equivalent circuit approach, are obtained directly from the equations. Since it consists primarily of matrix algebra, the technique is suitable for computer implementation. Then, a program capable of calculation of steady-state dc and small-signal ac characteristics of *any* two-topology converter is introduced. Owing to the special-purpose nature of the program, it can be implemented on small or even desktop computers. Closed-loop systems are considered next, and the equations for the closed-loop frequency response of the converter are developed which are also incorporated into the SCAP (Switching Converter Analysis Program).

To verify the accuracy of the calculations, and thus the validity of the design, after breadboarding the hardware, actual frequency response measurements must be made. However, in order to prevent the switching noise from obscuring the results, a wave analyzer (narrow-band tracking voltmeter) is required. Another computer program was developed to use a wave analyzer to perform fast and accurate measurements under computer control. Results of the measurements supply information upon which refinements of the original design are based. Therefore, the Automatic Measurement System AMS, along with the SCAP, fulfill two very important steps of a design, namely prediction and measurement. Now,

a very accurate initial design of the complete closed-loop regulator is performed on the computer. After breadboarding, fast and accurate measurements are made. Owing to the high accuracy of the original design, fewer cycles of prediction-measurement-refinement are necessary and the design process becomes much faster.

In summary, the state-space averaging modelling technique along with important measurement methods such as measurement of the loop-gain without opening the loop, when coupled with the computerized implementation, result in an indispensable tool for the modern power supply engineer.

PART II

AC UNINTERRUPTIBLE POWER SUPPLY

CHAPTER 5

INTRODUCTION

Some services such as hospitals and high priority computers provide vital functions where no disruption of power is acceptable. Such systems usually rely on Uninterruptible Power Supplies (UPS) to ensure a continuous flow of power. To provide such service, these supplies incorporate some means of energy storage. The stored energy supports the load at times of main line power failure. The amount of the stored energy depends on the load and the particular application. Sometimes the supply must power the load just long enough to allow an orderly shutoff of the different stages of the load (normally in small computer systems). On the other hand, there are cases where the stored energy must be large enough to power the load during the time required to start and warm up an auxiliary diesel engine which, with an associated generator, will take over the task of energizing the load. When the power line recovers, by some preset procedure various parts of the load return to normal operation while the drained storage medium is recharged from the line.

Figure 5.1 demonstrates a typical ac uninterruptible power supply in which the storage medium consists of a bank of batteries. In normal line condition, the batteries are charged from the line by the battery charger, and the batteries in turn power an inverter which supplies the

load with ac power of suitable voltage and frequency. In case of a power failure, the charging current to the batteries is removed and the energy stored in the batteries keeps the inverter and the load running. The switches are for repair and are applicable in cases where the input and output voltages and frequencies are the same. The switches are normally open; in case of a failure in the UPS, the switches are closed to effectively remove the system from the line. In this condition, the load is of course unprotected.

So far in this work, only dc-to-dc conversion has been examined. However, the field of power electronics covers a much broader range: dc-to-ac, ac-to-dc, and finally ac-to-ac conversion. More specifically, these techniques are treated here as extensions of dc-to-dc conversion methods.

The first chapter of this part generalizes dc-to-dc converters in the "quadrant" sense, and various ways of generation of ac from dc sources are mentioned. The selected result is a four-quadrant converter hereafter referred to as an "amplifier", capable of delivering bipolar voltages and current to the load. It can well satisfy the requirements of the inverter part of the UPS of Fig. 5.1. Furthermore, the output voltage of a switched-mode amplifier is controllable, and by proper feedback, low distortion ac can be generated. However, the task of the battery charger is left unaltered. The battery charger is usually composed of a set of rectifier diodes or silicon controlled rectifiers (SCRs) and some large reactive elements to control the current. The combination, owing to the nonlinear nature of the devices, draws

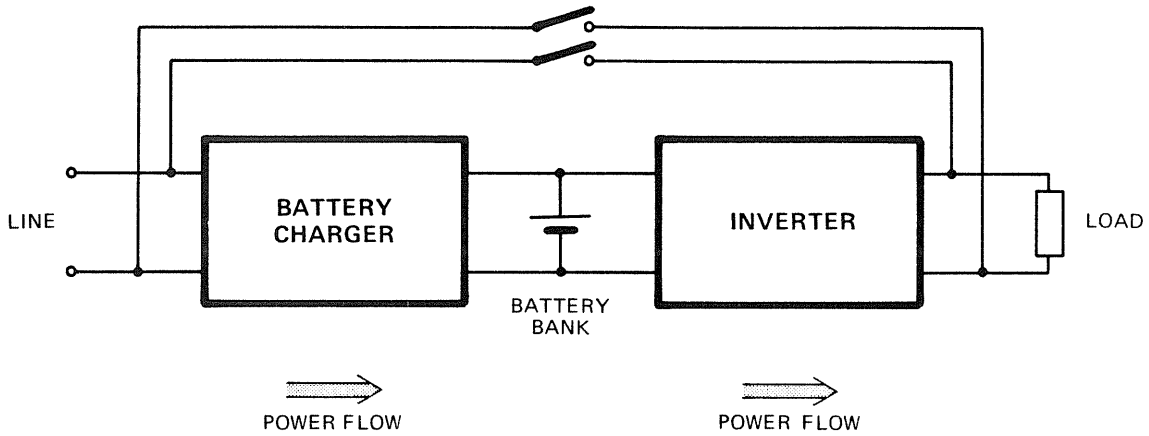


Fig. 5.1 A conventional ac Uninterruptible Power Supply.

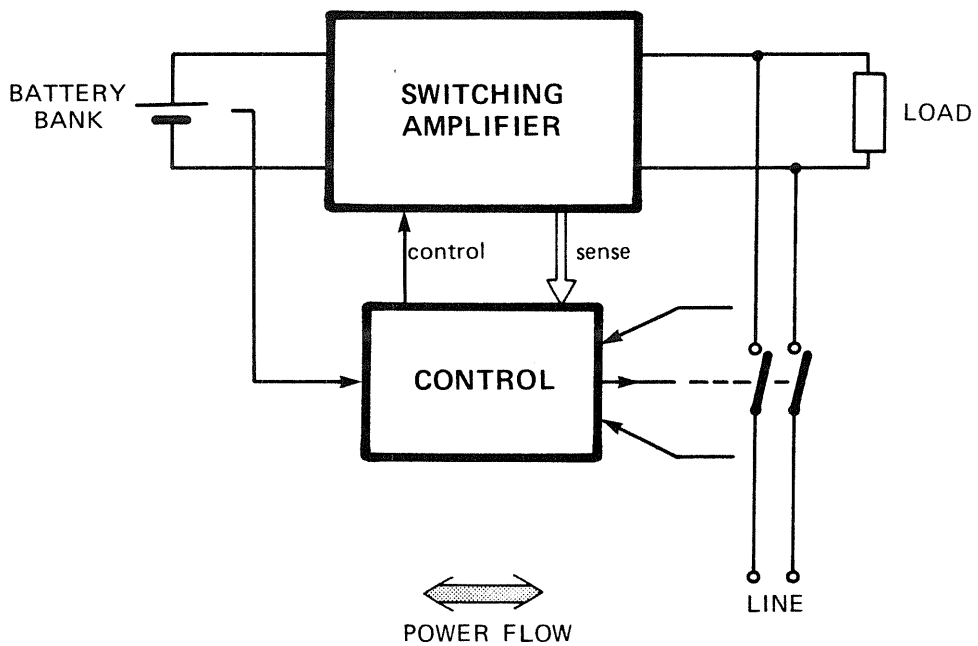


Fig. 5.2 Alternative UPS.

non-sinusoidal currents. Correction for this nonunity-power-factor load on the line requires low frequency filtering, which tends to be heavy, bulky, and expensive.

A more elegant and efficient solution is to use a unity power factor ac-to-dc battery charger. One implementation uses the above-described amplifier operating in the reverse direction: the switching amplifier, being a four-quadrant converter, is capable of processing power in both directions. In "forward" dc-to-ac operation, this permits reactive loads to be used where, in some part of the ac cycle, the voltage and current are out of phase and power is returned back to the dc source. However, if the load is replaced by an ac voltage source, the current waveforms become distorted due to lack of a proper control scheme. Such a scheme is based on current control to interface the two ac and dc voltage sources. Furthermore, with such control on current, it can be regulated to be proportional to the voltage, so it is sinusoidal and in phase with the voltage. Therefore, the amplifier functions as a unity power factor battery charger.

An alternative uninterruptible power supply is introduced here. The scheme is demonstrated in Fig. 5.2, which relies on the four-quadrant capability of the amplifier to permit bidirectional power processing. Notice that in Fig. 5.1 each unit processes power only in one direction, while in the UPS of Fig. 5.2 the switching amplifier is fully utilized to process power in both directions, since at any moment only one of the two functions is required. The system works as follows: when the line is up, the switches — controlled by the control circuit —

are closed. The load is then powered by the line. The control circuitry causes the amplifier to be a unity power factor battery charger, by constraining the ac input current to be of the same shape as and in phase with the ac input voltage. The battery bank is thus charged from the line, and the level of power flow depends on the amplitude of the current only since its shape and phase are predetermined. For a minimal charging time, the current is held at a maximum value until the batteries reach a preset voltage level, and operation is then switched to a low current level.

In case of a power failure, the control circuit immediately opens the switches while the amplifier converts to an inverter. The load is then energized from the battery bank to maintain a continuous operation. When the line power is restored, the control circuitry matches the phase and amplitude of the inverter to those of the line. The switches are then closed and the amplifier is converted back to a unity power factor battery charger to replenish the charge withdrawn, and the cycle repeats.

This alternative UPS reduces the number of power stages of the conventional UPS to one unit, since at any moment only one function is required. This reduction makes the new UPS simple, more reliable, and more economical. Furthermore, when the line is up, its unity power factor operation results in a more efficient line operation than does the ordinary UPS. However, there are some disadvantages associated with this technique: the load must have the same voltage and frequency ratings as the line, and the switches between the load and the line must respond quickly in case of power failure. It was mentioned that

after restoration of power, the battery bank will be charged at maximum level to get to the fully charged state, after which the operation is switched to a low-current mode. In the worst case of occurrence of a double failure at the voltage peak, it is required that the current going into the amplifier change sign immediately. Owing to the presence of reactive elements in the amplifier, an instantaneous reversal of current is not possible and will result in a "dip" in the voltage waveform. Nonetheless, the size and duration of this transition can be minimized by proper design. Also, the load is usually capable of recovering.

Chapter 6 extends the area of attention to ac generation. Two methods, the synthesis and the PWM methods, are reviewed. The synthesis method is primarily used in large power systems and the PWM method is more suitable for small to medium sized systems. Then, dc converters are classified according to their quadrant capability. Dc-to-dc converters, owing to the limitations set by the semiconductor switches, are usually capable of delivering only one polarity of voltage and one polarity of current, namely, one quadrant. By proper modification of the switch, current-bidirectionality and two-quadrant operation is obtained. Two such current-bidirectional dc converters may be used to provide bipolar currents *and* voltages. Thus, a true four-quadrant converter is obtained to permit generation of ac power from a single dc source.

Chapter 7 treats the dc-to-ac operation of push-pull power amplifiers. Owing to continuous large signal variation of the states

of the amplifier, the design techniques and criteria are different from those of conventional dc converters — constituent parts of the amplifier. Control of the output with feedback loop(s) requires careful attention to continuous change of dynamics due to large-signal modulation. The push-pull method is extensively examined for dc and ac characteristics, and the results are experimentally verified on an amplifier utilizing two Ćuk converters. A feedback algorithm is designed and the predicted and measured responses are compared.

The reverse mode of operation, ac-to-dc operation, is the subject of Chapter 8. Here the roles of input and output are also reversed such that input to the system is the ac source (line) while the dc source (battery) becomes the output. Unlike the dc-to-ac operation, this mode is forced upon the amplifier and application of feedback is mandatory. This is because the input impedance of the amplifier must be shaped to look *resistive* at low frequencies. Also, the input is connected to the line which completely changes the dynamics of the system. The control is performed on current, whose waveshape determines the quality of the charger. Again, the result of calculations on the Ćuk amplifier with multiple-loop feedback is compared to measurement data.

The same four-quadrant switching amplifier is used for both dc-to-ac inverter or ac-to-dc charger modes. Chapter 9 examines the process of switching between the two modes. In this region, the system may exercise a large variation of current while the voltages remain almost constant. The duty ratio saturates and the system behaves as an

open-loop converter. Finally the results are checked on the Ćuk UPS.

CHAPTER 6

CLASSIFICATION OF POWER CONVERTERS — AC GENERATION

The area of power electronics is not limited to dc-to-dc converters. Generation of ac from dc, dc from ac, and finally ac from ac are also required functions of power processing systems. High efficiency, reliability, low weight and volume, and controllability of the outputs make the switched-mode converters an attractive choice in all aspects of power electronics. Generation of ac is possible in several ways. In the past, inverter configurations have relied heavily on a large number of slow semiconductor devices to approximate sine waves by synthesis. On the other hand, the pulse width modulation approach, adopted here, inherently relies on a small number of generally faster devices to take full advantage of high operation frequencies.

Section 6.1 describes the synthesis method of sine wave generation and compares it with the pulse width modulation approach. The necessarily high switching frequency, owing to power device limitations, usually restricts the PWM method to low and medium power applications. The versatility and reliability of the technique makes PWM a better choice at low power levels.

Section 6.2 shows how dc-to-dc converters can be used as building blocks toward ac generation.

The output of the converter can be made to produce a full wave-rectified sine wave, which is "unfolded" to obtain sine waves on the output. However, owing to the unidirectional property of the semiconductor switches, the converter is capable of processing power in only one direction; the power can be only toward the ac side. This inverter type is capable of generation of in-phase bipolar voltages and currents (still two-quadrant) which can be used only in the case of unity power factor loads.

The problem is approached from another point of view by generalization of a dc-to-dc converter, in which the limitation imposed by the unidirectional switches is eliminated by a bidirectional switch. Then, the dc converter alone can process current and therefore power in both directions. Still, the output voltage is unipolar and techniques to generate bipolar output voltage are examined. Finally, the push-pull method is introduced which uses a single voltage source and two current-bidirectional dc-to-dc converters to power a load which is differentially connected to the outputs of the converters. Full four-quadrant ac operation is obtained which is capable of driving general loads, including reactive loads.

6.1 Synthesis Versus Pulse Width Modulation

This section reviews the synthesis technique and compares it with the PWM method.

Figure 6.1a shows a simplified waveform-synthesis power converter. The circuit is comprised of many voltage sources and switches

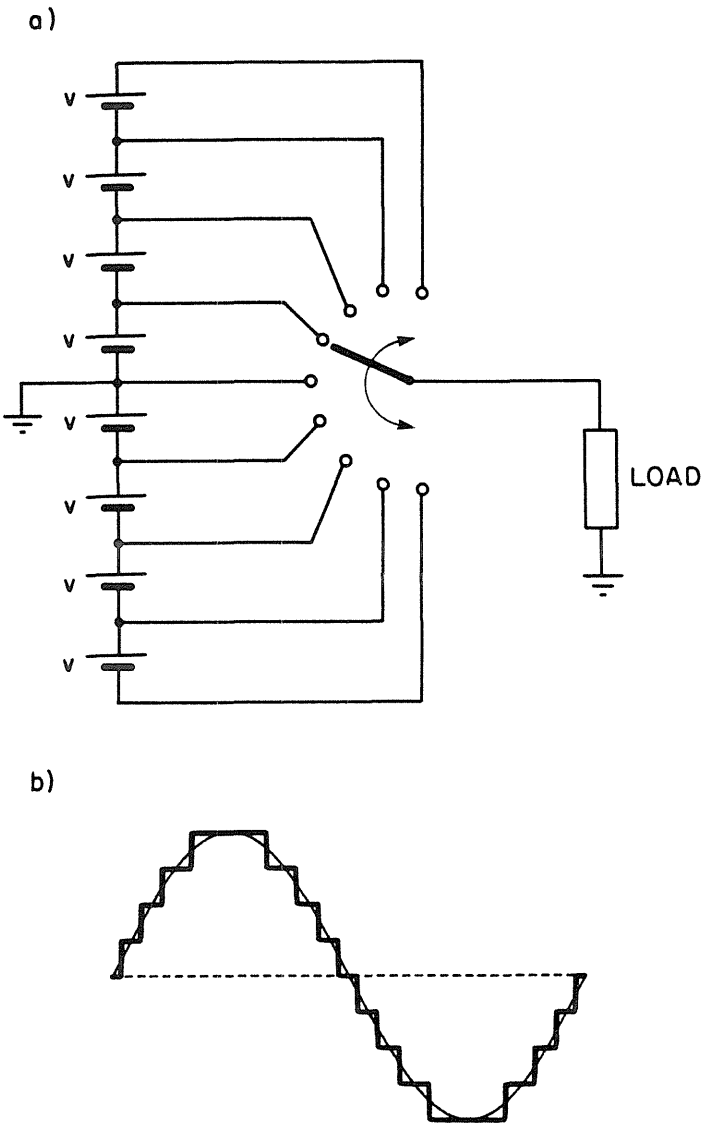


Fig. 6.1 Ac generation with synthesis method. (a) The hardware, (b) output waveform.

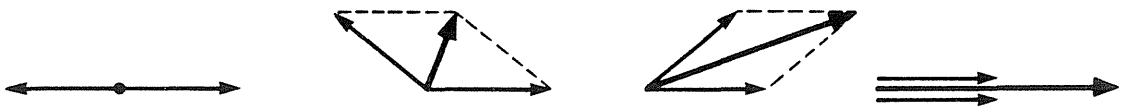


Fig. 6.2 Use of two synthesizers to vary the output amplitude.

(the 1 pole n-throw switch is realized by n single-pole, single-throw switches). A control circuit determines the instant when the switches are activated. The waveform of Fig. 6.1b illustrates the sequence of the switchings which leads to an almost sinusoidal voltage across the load. The greater the number of voltage sources and switches, the closer is the synthesized waveform to the original. So, in practice, one would like to use the minimum number of switches (steps), just enough to achieve the required distortion level. Still, some external filtering of the output might be necessary. One can notice that every switch is activated and deactivated only once during each cycle of the output frequency. So, for low-frequency line applications, the switching speeds of the switches are also low. This enables a collection of low-speed switches to generate a waveform on the output. High power switching devices are usually slow, and therefore this technique has application in high power inverter circuits.

However, there are some disadvantages associated with the synthesis technique. First is the complexity of the scheme: many voltage sources and switches are required. Also, improvement of the harmonic content of the output voltage demands a rapid increase in the number of steps and thus in the number of switches. This complexity can be justified only in the case of large systems. A second problem is that a very limited control of the output voltage is possible without a significant loss of purity of the output waveform. Owing to the limited number of switches and associated quantization errors, in order to minimize the harmonic content of the output it is desired always to use

the same shape of output. That is, a sine wave with an amplitude ¼ of that of Fig. 6.1b is quantized to a square wave! Therefore, the technique is usually used in fixed voltage applications. In cases where full control of the output voltage is required, two fixed-output synthesizers are used in series. By change of the relative phase between the outputs, various voltages in the range of zero to twice that of a single unit can be obtained, as illustrated vectorially in Fig. 6.2.

Now we consider the pulse width modulation (PWM) technique. Unlike the synthesizer, this method uses only one or two voltage sources and switches. The basic two-switch circuit is shown in Fig. 6.3a, where the switch connects the output to either a positive or a negative voltage at a high rate (frequency). The same amount of time spent on the positive and negative sides (duty cycle 0.5) generates a zero average voltage. Any waveform (average) can be generated on the output by pulse width modulation of the switch as shown in Fig. 6.3b. Compared with the synthesizer of Fig. 6.1a, the PWM approach is much simpler and more versatile. For example, by proper adjustment of the modulation index as illustrated in Fig. 6.3c, the output amplitude can be varied from average zero to the maximum. Usually a low-pass filter is placed on the output port of the inverter to retain the low frequency variations while disposing the high frequency components. The larger the separation of the switching frequency and the modulation frequency, the easier the task of the filter. However, in PWM systems, the switches operate at a much higher rate than those of a synthesizer to

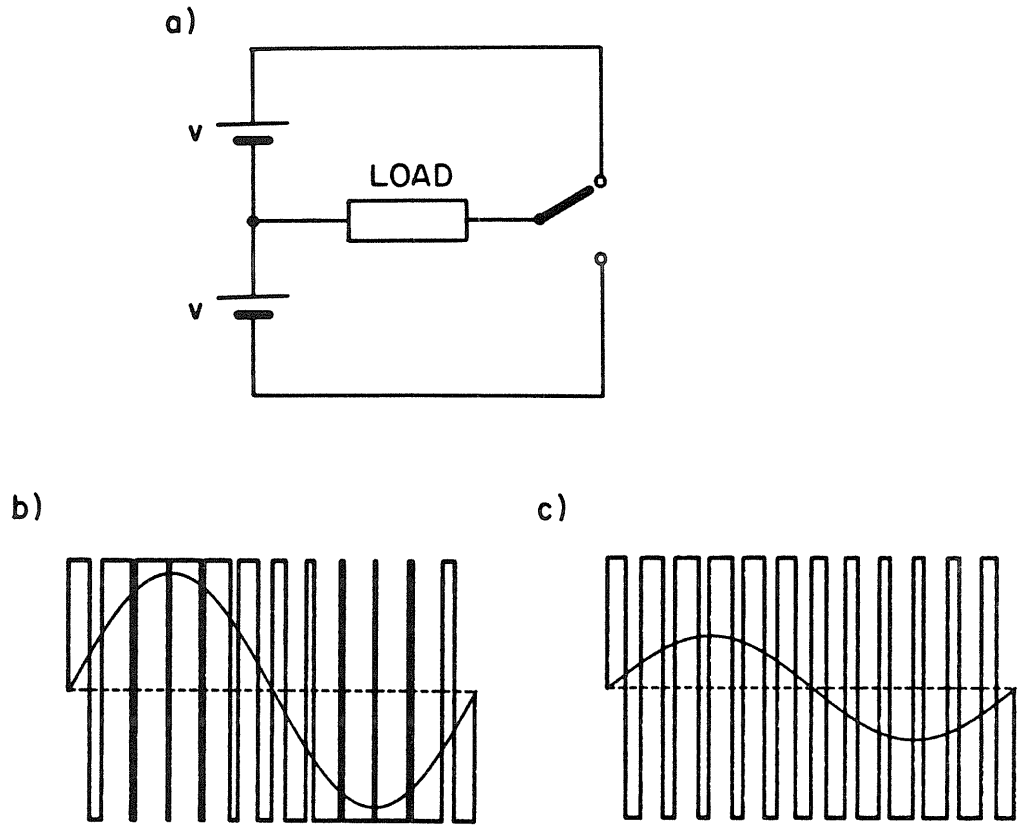


Fig. 6.3 Pulse Width Modulation technique. (a) The hardware, (b) high-level output, (c) low-level output.

produce the same output. Therefore, the limited availability of fast switches restricts the application of this method to low to medium power levels.

Next, the PWM technique is generalized to include the filter elements as parts of the system rather than add-on components to the final design.

6.2 General Pulse Width Modulation Techniques

Many switched-mode dc converters are PWM systems whose duty ratios are constant or change slightly to accommodate regulation. However, large ac voltages can be superimposed on the output of a properly configured dc converter if its duty ratio varies according to an input signal (e.g. the reference voltage of a regulator). This section analyzes ways of generation of ac voltages by special implementations of dc-to-dc converters.

6.2.1 Two-Quadrant Converter

An ordinary dc-to-dc converter such as one of those shown in Fig. 1.1b is considered a one-quadrant converter. The unidirectional capability is imposed upon the converter by the actual transistor-diode implementation of the switch. A unidirectional switch limits the operation to one direction of current, and because the unit is also capable of production of only unipolar voltages, the converter is limited to one quadrant. However, bipolar output voltages can be obtained by an "unfolding" circuit on the output of the converter.

Figure 6.4a illustrates the method. The duty ratio of the converter is varied to produce the full-wave rectified waveforms of Fig. 6.4b at the converter's output. Finally, the switches "unfold" the waveforms to those of Fig. 6.4c by change of position at each zero crossing. Although the combination produces bipolar voltages, the output is still limited to two quadrants because the output voltage and current must have a certain phase relation (0^0 or 180^0), which prohibits the inverter from driving reactive loads. This limits the applications of this inverter.

6.2.2 Differential Inverter

Ac power can be generated at a load if the load is placed between a variable dc source (converter) and a constant dc source. As can be seen in Fig. 6.5a, the load receives zero voltage if the supply and converter voltages are equal. Both polarities of voltage are produced by increase or decrease of the variable voltage source. The combination is realized by a load placed between output of a dc converter and its driving voltage source. Additionally, the load can be referenced to ground by swapping the variable source and the load as shown in Fig. 6.5b, provided that the output of the dc converter is isolated from the input.

Figure 6.6a shows an isolated version of the buck-boost converter, while Fig. 6.6b shows the series combination of the input and output according to Fig. 6.5b. The same figure is redrawn in Fig. 6.6c in which R, the load, receives bipolar voltages and currents. Note that the capacitor C may be placed around the load. This alters the

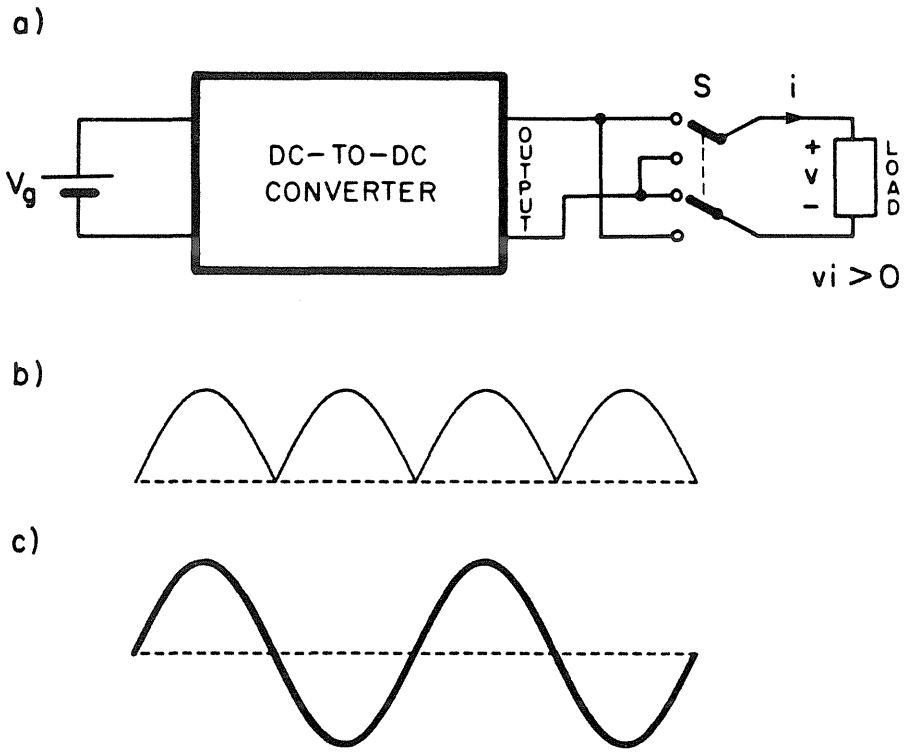


Fig. 6.4 Two-quadrant ac generation. (a) The basic method. The switches reverse the polarity of voltage. (b) Output voltage of the dc converter. (c) The load voltage.

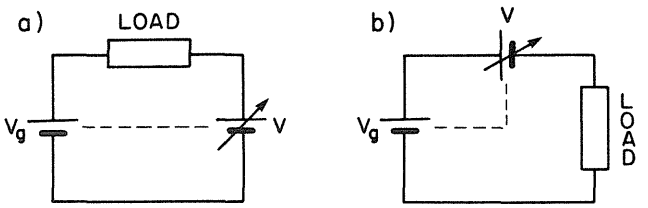


Fig. 6.5 *Differential generation of ac. (a) Floating load. (b) Output voltage is grounded on one side.*

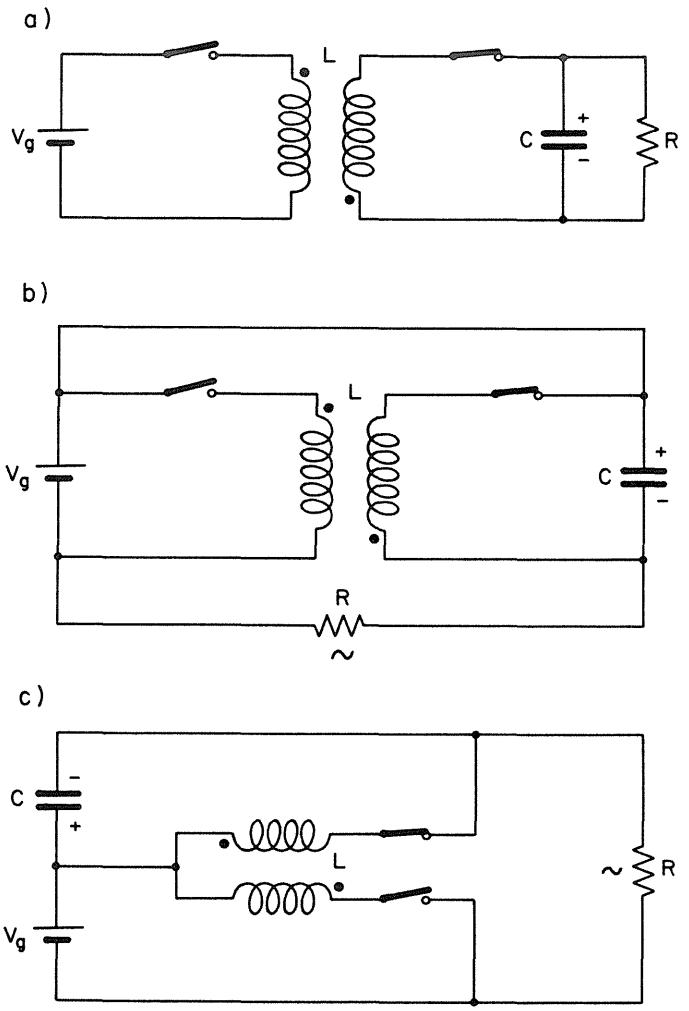


Fig. 6.6 *Buck-boost differential amplifier (a) isolated converter, (b) output in series with input, (c) the same as (b), but drawn differently.*

input/output waveforms and characteristics of the circuit, but the basic dc conversion property of the circuit remains intact.

The same procedure applied to a Ćuk converter results in the inverter shown in Fig. 6.7. The dc isolated version of other converters can also be used.

The technique is simple, and since it mostly uses the isolation property of the converters as a part of the inverter it becomes harder to implement a high frequency isolation between input and output ports. This, along with some slight nonsymmetry of the output, causes the scheme not to be as general as that to be introduced next.

6.2.3 Push-Pull Configuration

The one-quadrant limitation of dc converters is imposed by the practical implementation of the switch, illustrated by a Ćuk converter in Fig. 6.8a. By a simple addition of another transistor Q_2 and another diode D_2, as shown in Fig. 6.8b, the switch and therefore the converter becomes current-bidirectional. A simple change of the duty ratio makes the converter look either as a current source or as a current sink.

The problem of the generation of a bipolar voltage at the output is solved by the symmetrical push-pull method shown in Fig. 6.8c. The inverter comprises two current-bidirectional dc converters driven by a modulator with complementary outputs. At duty ratio D = 0.5, both converters are driven with the same pulse trains (despite the out of phase drive). Thus, the output voltages of the two converters with

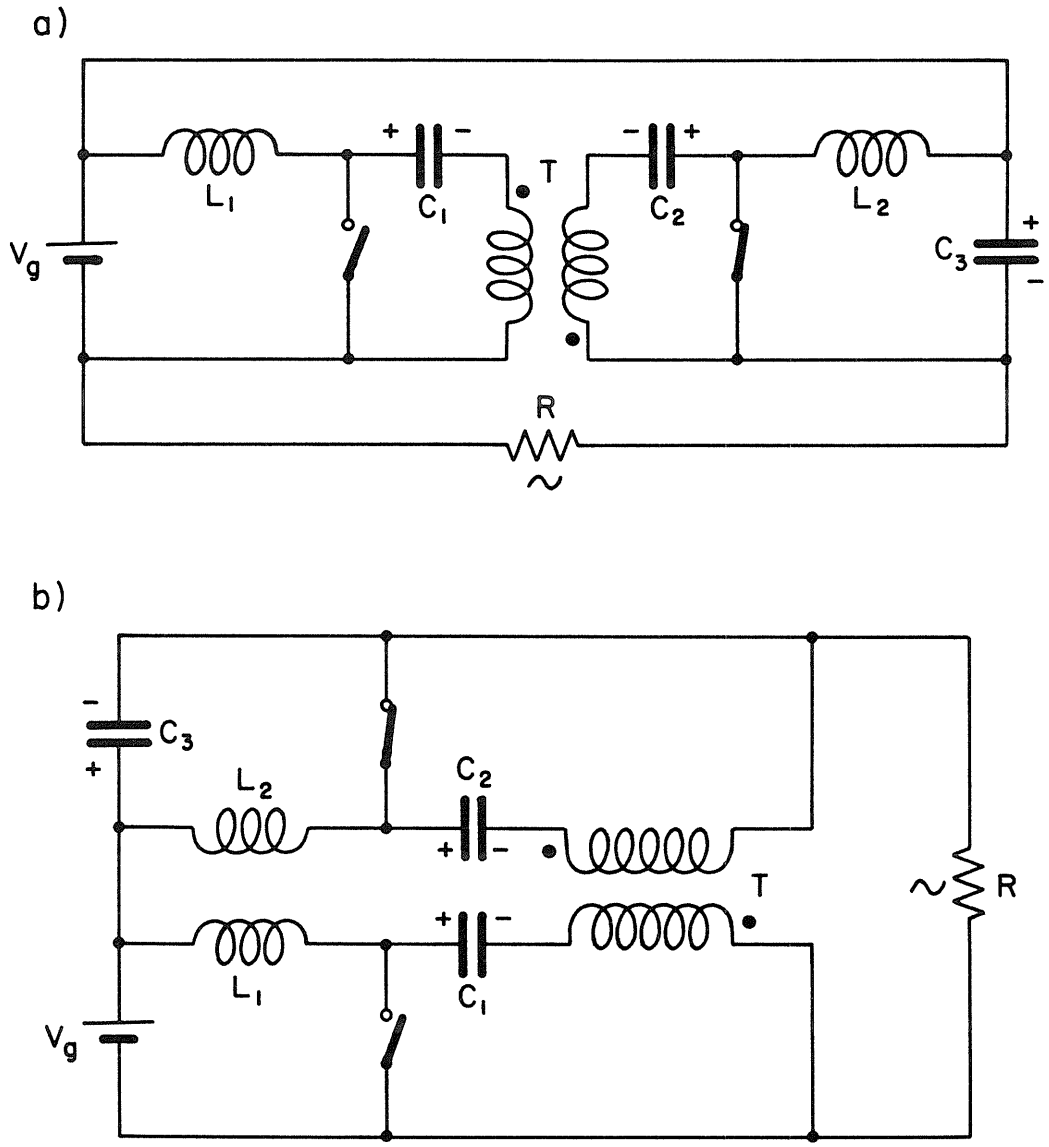


Fig. 6.7 Differential ac generation by use of a Ćuk converter. (a), (b) same amplifier drawn differently.

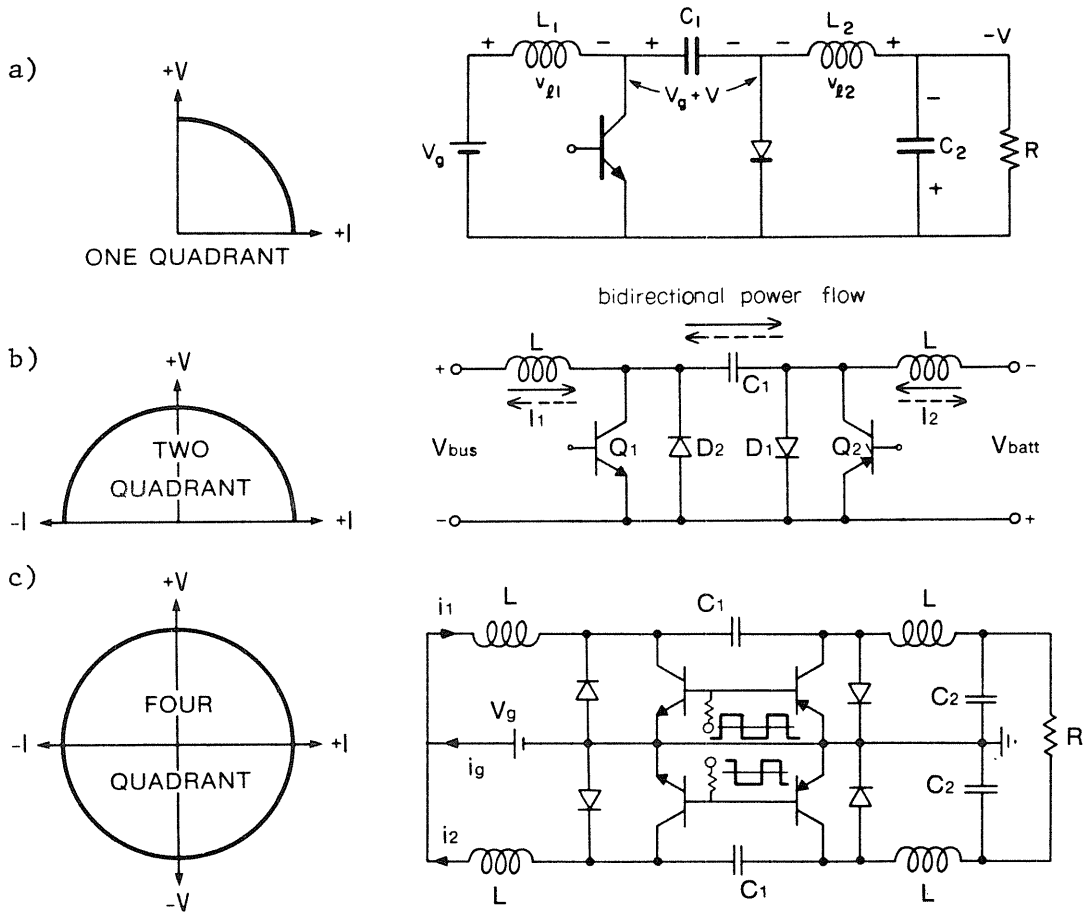


Fig. 6.8 *Generalization of dc-to-dc converters. (a) Single-quadrant, (b) current-bidirectional (2-quadrant), (c) push-pull amplifier (4-quadrant).*

respect to ground are the same. The load is differentially placed across the outputs and therefore sees zero voltage. Now, if the duty ratio of one converter is increased, its output voltage increases. However, by the complementary nature of the drive, the duty ratio of the other converter, and consequently its output voltage, decrease. Therefore, there is a net voltage across the load. By symmetry, reduction of duty ratio of the first converter from 0.5 causes the voltage across the load to reverse its polarity. Also, when the load draws current, one converter sources the current while the other sinks the current. For the other direction of current, the roles of the converters reverse, calling for current-bidirectional converters. Hence the name push-pull truly reflects its operation. This combination allows the polarities of the output voltage and current to be independently controlled, and thus demonstrates a true four-quadrant capability.

The push-pull structure of Fig. 6.8c is not limited to the particular converter, but is general and can be implemented with a bidirectional version of any dc-to-dc converter. Figure 6.9 shows the general push-pull amplifier where the blocks with double-headed arrows indicate bidirectional dc-to-dc converters. If an ac voltage is applied to the input of the modulator, the output is an ac voltage whose amplitude and shape depends on the specific converter and its dynamics.

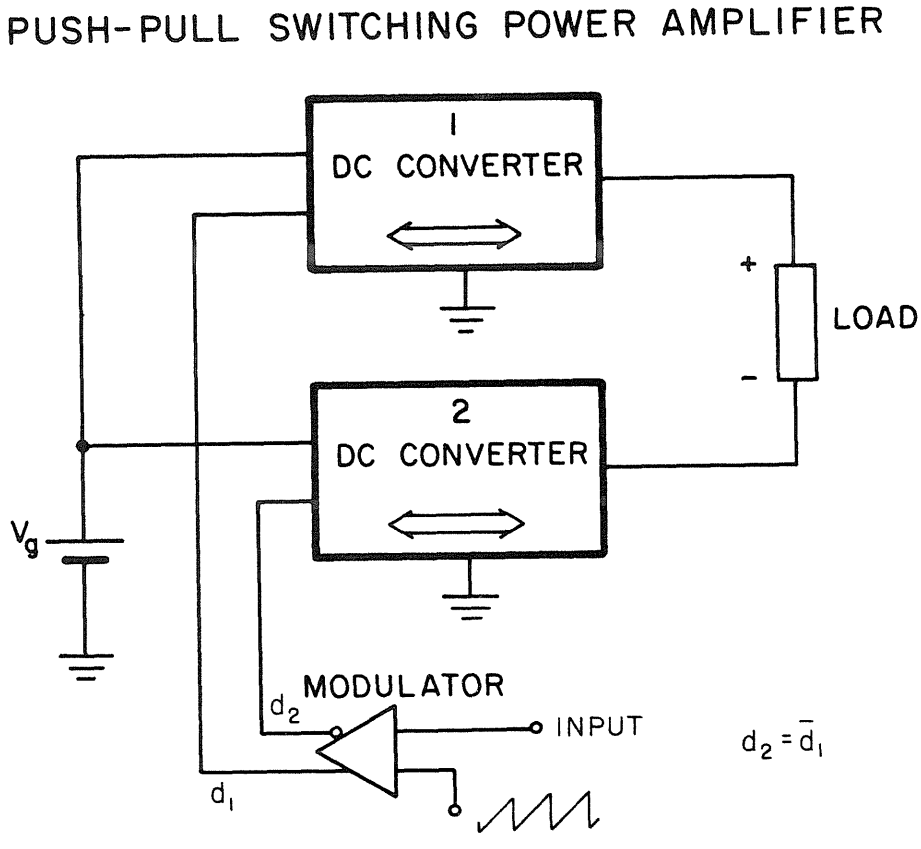


Fig. 6.9 *A general push-pull switching power amplifier. Arrows denote current-bidirectionality.*

6.3 Review

For small systems, comparison of the synthesis method and the pulse width modulation approaches quickly leads to the selection of the latter method for ac generation purposes. The technique employs a few fast switching devices to generate a low frequency output, after the switching frequency components are discarded by low-pass filters. A more general form of PWM involves PWM switching dc-to-dc converters, in which the filtering action is a part of the system to allow the better utilization of the components. Dual-supply converters were not mentioned because simple single-supply versions are achievable. The limitation of the switching devices dictate the unidirectional current and power flow. However, current-bidirectional, two-quadrant, converters are obtained by employment of a modified switch. First, the combination of a bidirectional dc converter and its driving voltage source is used to generate ac. Then, a more general form is obtained which incorporates two bidirectional dc converters. This last technique, referred to as the push-pull amplifier, is the basis of the work in the second part of this thesis.

CHAPTER 7

DC TO AC CONVERSION — INVERTER

Push-pull switching power amplifiers are counterparts of linear amplifiers, and have an ideal efficiency of 100%. However, the resemblance goes no further, and some fundamental differences separate the two methods. Two dc-to-dc switching converters and a modulator with complementary outputs are constituent parts of a switching push-pull amplifier, and Fig. 7.1 shows push-pull amplifiers employing basic converters. However, design of a linear amplifier is different from that of a dc converter, owing to different constraints and continuous large-signal variation of the states of the system. These differences, along with the low-frequency distortion caused by the nonlinear gain of some dc converters, are the subject of Section 7.1.

Commonly, it is desired to regulate the output of the amplifier and so feedback loop(s) are placed around the system, as in Fig. 7.2. The output voltage is sensed (and other states if necessary), and then compared with a reference signal. The error signal is processed through the compensation network and is used to keep the output as close to the reference as possible. If the reference signal is an audio signal and the converters have sufficient bandwidth, the system becomes a switched-mode audio amplifier. On the other hand, as in the case of the UPS if the input is restricted to sine waves, particularly to

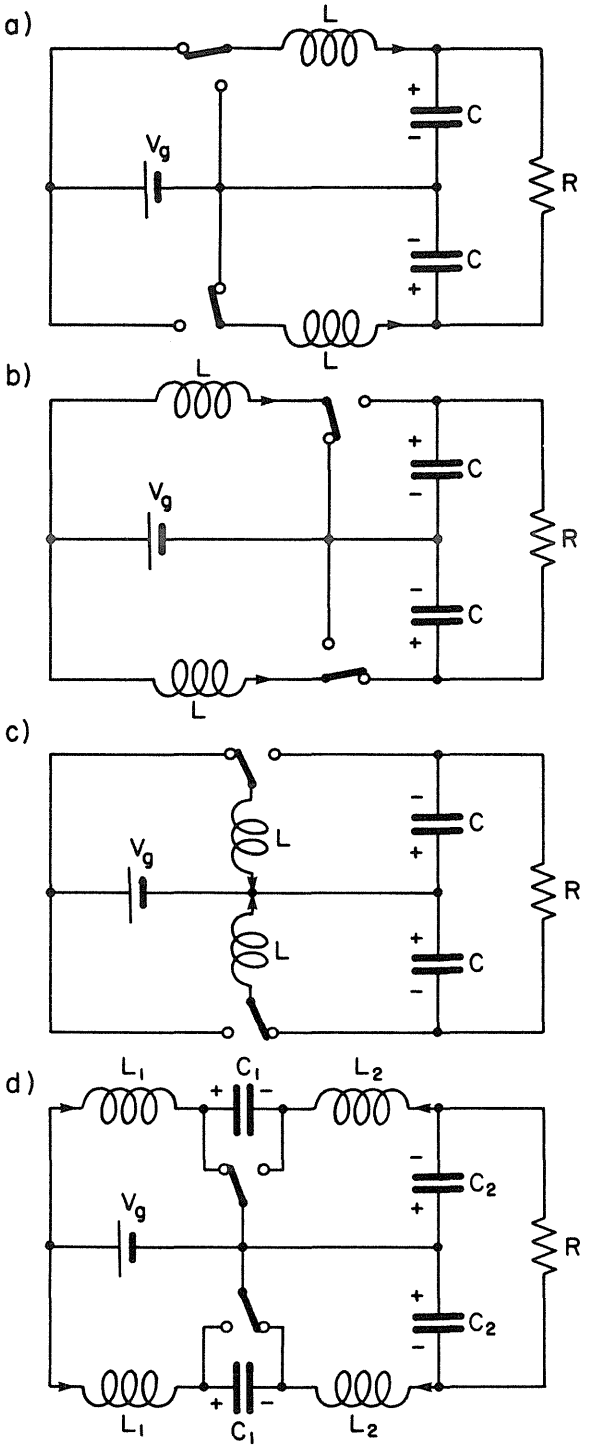


Fig. 7.1 *Four push-pull switching amplifiers each consisting of two current-bidirectional converters.*

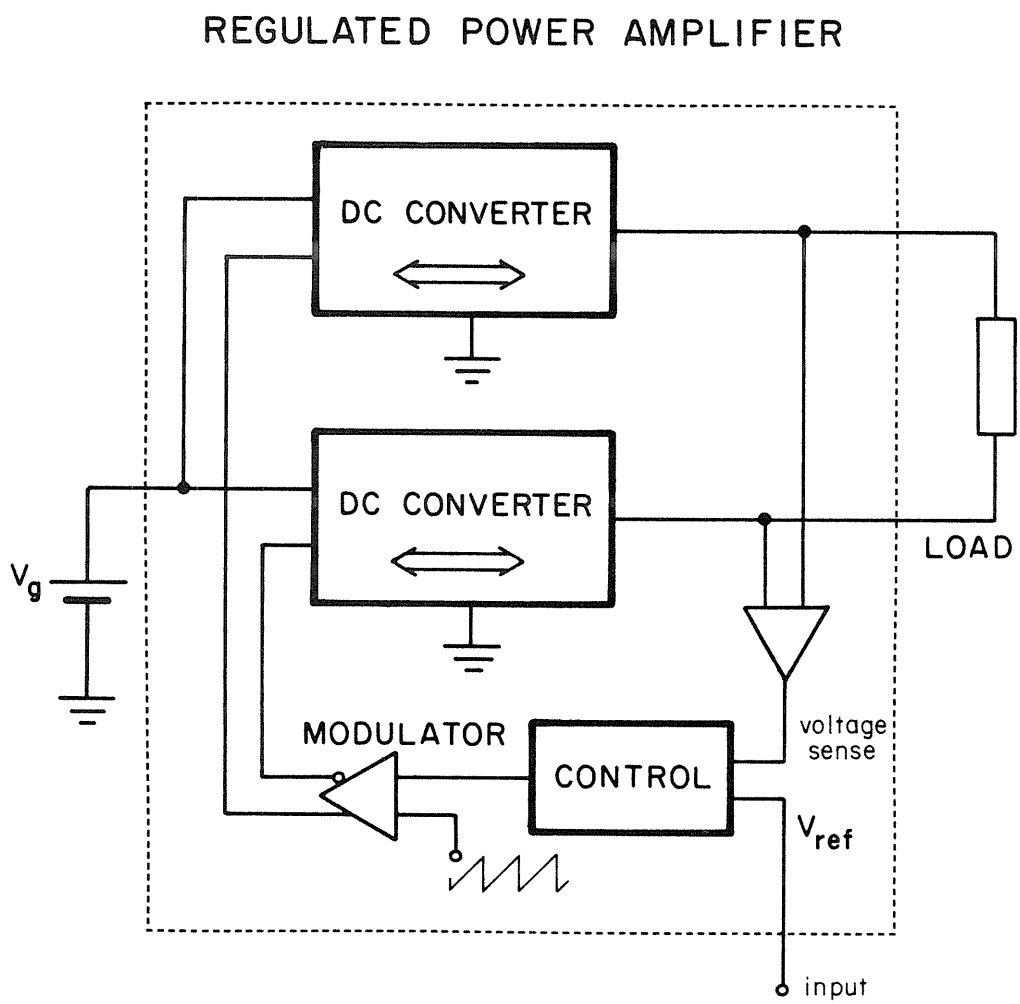


Fig. 7.2 *Output voltage regulation of a push-pull amplifier. The sensed output voltage is compared with the reference voltage and the error is kept minimal by the feedback loop.*

60(50) Hz sine waves, a dc-to-ac inverter is obtained. Regulation of the output allows tight control of the harmonics and therefore distortion of the output. Also, it desensitizes the output to variations of the input voltage, load, or other parameters of the system. Control aspects are discussed in Section 7.2. The results of control techniques are demonstrated in Section 7.3, through analysis and construction of a push-pull power amplifier comprising two Ćuk converters. The design includes the analysis of the complete amplifier, which is reduced to the analysis of a single constituent converter. A feedback loop is placed around the system, and finally the analytical and experimental results are compared.

7.1 Differences Between Dc and Ac Systems

The fundamental difference between a dc and an ac system is that, in a dc system, the operating point is set at a fixed point, except upon occasional disturbances when it changes to accommodate regulation (closed-loop); while, in an ac system, by its nature, the operating point experiences regular large variations. The ac system, therefore, must be able to tolerate these large variations.

These variations are not just in duty ratio and, for example in the case of the output voltage, the states of the system must handle a full scale variation over the desired frequency range. This immediately puts a constraint on the amplifier: the open-loop duty ratio-to-output frequency response must have a bandwidth at least as large as the maximum output frequency. Otherwise, if frequencies

higher than the bandwidth of the open-loop system are imposed on the duty ratio, the output cannot follow the maximum peak variations owing to the filtering effect of the converters. That is, the power bandwidth is less than the small-signal bandwidth. This is analogous to slew rate limit of conventional linear operational amplifiers.

If a feedback loop is placed around the amplifier, the crossover frequency may be set at a high frequency, but the full power bandwidth of the amplifier remains at the open-loop value. This problem is much less severe in dc converters where usually there is no need for the wide power bandwidth of 20 kHz or more as is required in audio amplifiers. The necessary high corner frequency of the filter in the amplifier dictates small values for inductances and capacitances of the converters. For applications such as audio amplifiers, the corner frequency is placed at the maximum audible frequency ($\simeq$ 20 kHz). While frequencies up to this limit must pass through the filter unaffected, the switching frequency must be attenuated as much as possible, and therefore the switching frequency must be much higher than the maximum bandwidth. Also, in order to lighten the task of the feedback loop around the complete amplifier, it is desired to make the open-loop system as close to ideal as possible. For example, for audio amplifiers, the open-loop frequency response of the amplifier is designed to be as flat as possible.

Another difference between dc and ac systems is in the "transfer ratio" from input to output of the amplifier. For an accurate large-signal reproduction of a signal at the output of an amplifier, the gain

characteristic (transfer ratio) must be linear. The transfer ratio is the dc gain (duty ratio-to-output) of the amplifier. Any nonlinearity of this characteristic is irrelevant in case of dc outputs, since the system is linearized around any operating point (for small perturbations), while in the case of the large variations in an ac system, it can cause severe distortion problems.

The calculation of the dc gain is simplified if all the parasitics of the circuit are neglected, whereby the dc loading effect of one stage upon the other becomes negligible. The load receives the difference between the two output voltages of two converters. If the duty ratio of one converter is D, the other converter, by the complementary nature of the drive receives D'. In the ideal case, one writes the output voltage as

$$\frac{V_0}{V_g} = M(D) - M(D') \tag{7.1}$$

where M is the ideal gain of one dc converter. At D = D' = 0.5, the output has zero voltage. The duty ratio is determined by the modulator, and with the normal linear sawtooth input, the duty ratio is directly proportional to the input voltage:

$$D = \frac{V_i}{V_{ramp}} \tag{7.2}$$

The transfer ratio V_0/V_i can be linear if the individual gains are formed such that Eq. (7.1) is linear versus D. This happens in the case

of a buck converter

$$M(D) = D \quad \frac{V_0}{V_g} \equiv D - D' = 2D - 1 \tag{7.3}$$

In the case of other basic converters, the individual and thus the overall gain is nonlinear

$$\text{boost:} \qquad \frac{V_0}{V_g} = \frac{1}{D'} - \frac{1}{D} = \frac{D - D'}{DD'} \tag{7.4}$$

$$\text{buck-boost:} \qquad \frac{V_0}{V_g} = \frac{D}{D'} - \frac{D'}{D} = \frac{D - D'}{DD'} \tag{7.5}$$

$$\text{\'Cuk}$$

However, as was mentioned before, Eq. (7.1) does not apply to nonideal cases. The loading effect of one converter in series with the load upon the other converter causes each individual dc gain to be different from that of a single, nonideal converter. For this reason, in general, the complete amplifier must be analyzed to find the input-to-output relationship. Consider the case of the boost amplifier of Fig. 7.3 with parasitic inductor resistance included. If by use of the state-space averaging method one calculates the overall gain from the individual converter gains, the following incorrect result is obtained by use of Eq. (7.1):

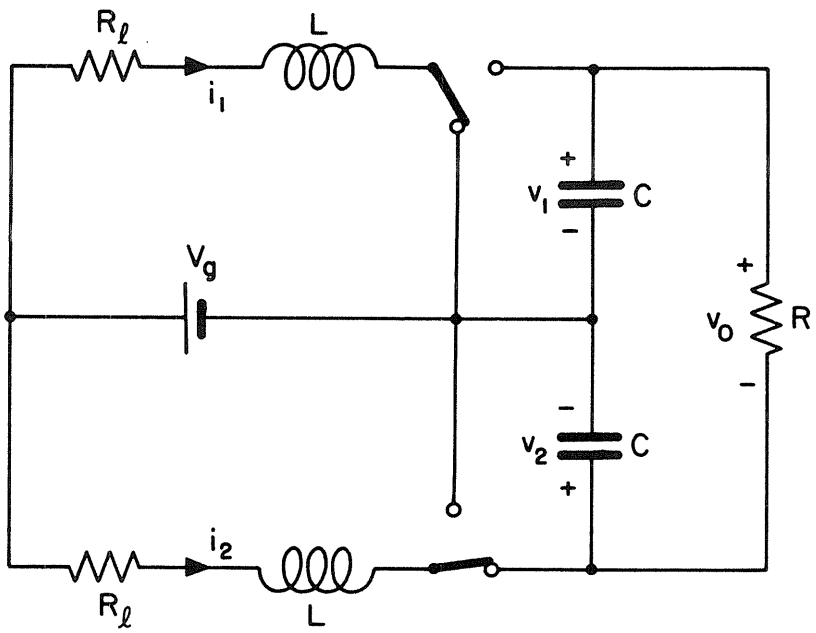


Fig. 7.3 Boost amplifier example with parasitics inductor resistances included.

$$\frac{V_0}{V_g} = \frac{1}{D'}\frac{1}{\left(1 + \alpha/D'^2\right)} - \frac{1}{D}\frac{1}{\left(1 + \alpha/D^2\right)} = \frac{D - D'}{DD'}\frac{1 - \frac{\alpha}{DD'}}{1 + \alpha\left(\frac{1}{D^2} + \frac{1}{D'^2}\right) + \alpha^2\left(\frac{1}{DD'}\right)^2} \tag{7.6}$$

where $\alpha \equiv \frac{R_\ell}{R}$.

However, if we calculate the dc gain of the complete amplifier, the correct expression is obtained as follows. For this purpose, we write the state-space equations during each switching interval.

during dT_s:

$$P\dot{x} = \begin{bmatrix} L\frac{di_1}{dt} \\ L\frac{di_2}{dt} \\ C\frac{dv_1}{dt} \\ C\frac{dv_2}{dt} \end{bmatrix} = \begin{bmatrix} -R_\ell & 0 & 0 & 0 \\ 0 & -R_\ell & 0 & -1 \\ 0 & 0 & -\frac{1}{R} & \frac{1}{R} \\ 0 & 1 & \frac{1}{R} & -\frac{1}{R} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ v_1 \\ v_2 \end{bmatrix} + \begin{bmatrix} 1 \\ 1 \\ 0 \\ 0 \end{bmatrix} v_g \tag{7.7}$$

$$A_{11} \qquad\qquad x \qquad\qquad b_{11}\ v_g$$

similarly during $d'T_s$:

$$P\dot{x} = \begin{bmatrix} -R_\ell & 0 & -1 & 0 \\ 0 & -R_\ell & 0 & 0 \\ 1 & 0 & -\frac{1}{R} & \frac{1}{R} \\ 0 & 0 & \frac{1}{R} & -\frac{1}{R} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ v_1 \\ v_2 \end{bmatrix} + \begin{bmatrix} 1 \\ 1 \\ 0 \\ 0 \end{bmatrix} v_g \tag{7.8}$$

$$A_{22} \qquad\qquad x \qquad\qquad b_{22}\ v_g$$

Notice that the equations are kept in the form $P\dot{x} = Ax + Bu$, whereby the dc solution immediately eliminates the reactive elements $P\dot{x} = 0$. Now we apply the averaging step of Eq.(2.14) to Eqs. (7.7) and (7.8) to obtain:

$$0 = \begin{bmatrix} -R_\ell & 0 & -D' & 0 \\ 0 & -R_\ell & 0 & -D \\ D' & 0 & -\frac{1}{R} & \frac{1}{R} \\ 0 & D & \frac{1}{R} & -\frac{1}{R} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ V_1 \\ V_2 \end{bmatrix} + \begin{bmatrix} 1 \\ 1 \\ 0 \\ 0 \end{bmatrix} V_g \tag{7.9}$$

Solution of Eq. (7.9) for the output voltage, that is $V_1 - V_2$, results in

$$\frac{V_0}{V_g} = \frac{D - D'}{DD'} \frac{1}{1 + \alpha\left(\frac{1}{D^2} + \frac{1}{D'^2}\right)} \tag{7.10}$$

This is the general result, and its comparison with Eq. (7.6) shows that the magnitude of the true output voltage is always larger than that predicted by Eq. (7.1) and, depending on the values of the X vector and D, the difference between the two equations may be large.

The same procedure may be applied to other amplifier configurations of Fig. 7.1 and the following results are obtained

$$\text{buck:} \qquad \frac{V_0}{V_g} = (D - D') \frac{1}{1 + 2\alpha} \qquad \text{linear}$$

$$\text{boost:} \qquad = \frac{D - D'}{DD'} \frac{1}{1 + \alpha\left(\frac{1}{D^2} + \frac{1}{D'^2}\right)}$$

$$\text{buck boost:} \qquad = \frac{D - D'}{DD'} \frac{1}{1 + \alpha\left(\frac{1}{D^2} + \frac{1}{D'^2}\right)} \tag{7.11}$$

$$\text{Ćuk:} \qquad = \frac{D - D'}{DD'} \frac{1}{1 + \alpha\left(\frac{D^2}{D'^2} + \frac{D'^2}{D^2}\right) + 2\beta} \quad ,$$

$$\alpha = \frac{R_{\ell 1}}{R} \qquad \beta = \frac{R_{\ell 2}}{R}$$

Equations (7.11) show that the gain functions of the nonlinear amplifiers are still nonlinear, except that the additional degree of freedom α may be used to shape the characteristic. The gain of the boost, buck-boost, and Ćuk amplifiers is considerably higher than that of the buck amplifier. Therefore, much less duty ratio variation is needed to produce a specific amplitude at the output. Also, α may be selected to produce a flat region on the gain curve to ensure minimum distortion. For example, for the same boost converter of Fig. 7.3 the

gain is calculated as Eq. (7.12). First shift the origin of duty ratio by the substitution D = 0.5 + a, so that a is the variation of the duty ratio from the quiescent operation point of 0.5. We get:

$$\frac{V_0}{V_g} = \frac{8a}{1 - 4a^2 + 8\alpha \dfrac{1 + 4a^2}{1 - 4a^2}} \tag{7.12}$$

Selection of $\alpha = 1/16$ causes the first order nonlinearity (coefficient of a^2) to vanish, and the gain becomes

$$\frac{V_0}{V_g} = \frac{8a}{1.5 + 16a^4 + \ldots} \tag{7.13}$$

A similar set of steps for the Ćuk amplifier shows that as expected $\beta \triangleq R_{\ell 2}/R$ is not important and maximum linearity is obtained at $\alpha = 1/14$. Of course, a β of zero yields the best efficiency. Figure 7.4 shows the dc gain characteristics of the basic converters. The ideal buck amplifier, ideal nonlinear amplifiers (described by Eqs. (7.4) and (7.5)), linearized boost and buck-boost, and the linearized Ćuk amplifier gains are illustrated which exhibit initial gains of 2, 8, 5.33, and 7 respectively. The sine waves of Fig. 7.5 are generated by a lossless boost, a linearized boost, and a linearized Ćuk amplifier. Table 7.1 contains pertinent results of these outputs.

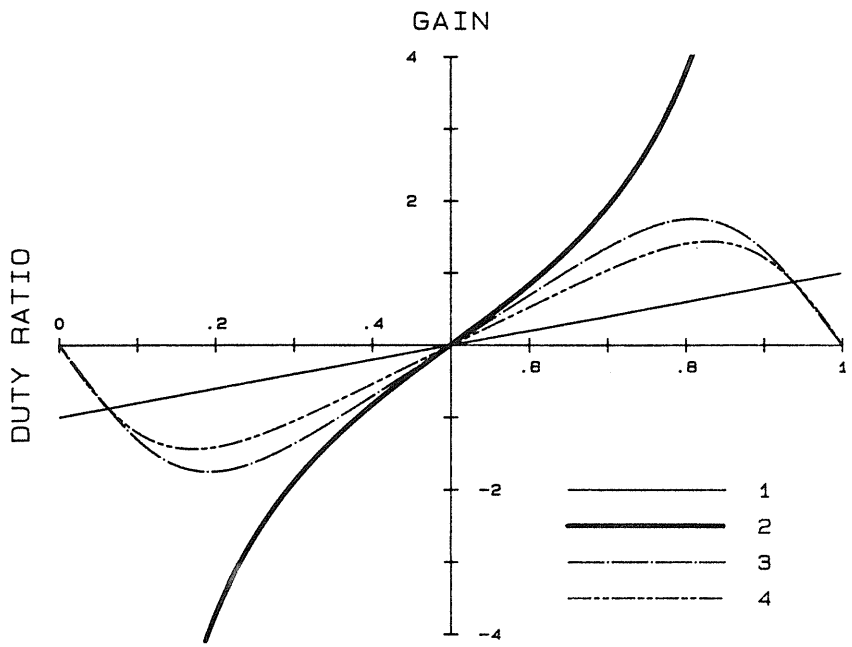


Fig. 7.4 Dc gain characteristics of various push-pull amplifiers. (1) Ideal buck, (2) ideal others, (3) linearized Ćuk, and (4) linearized boost and buck-boost.

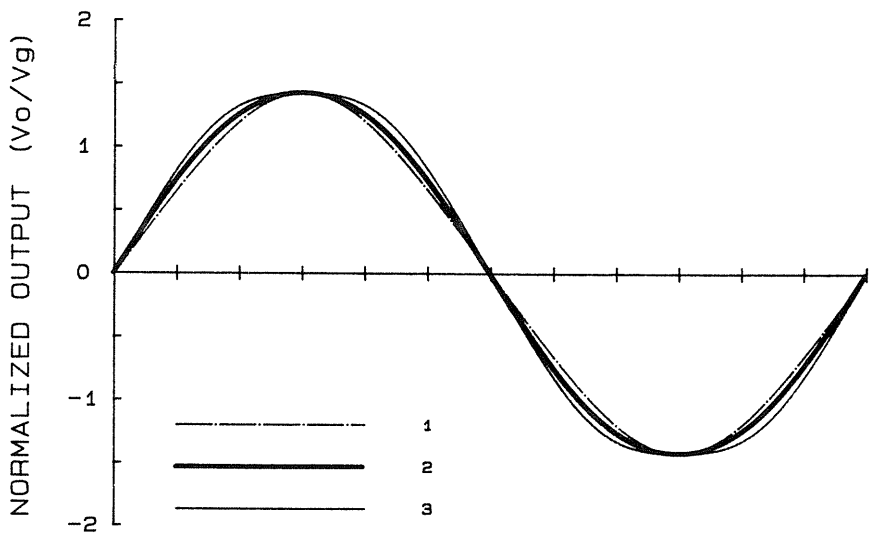


Fig. 7.5 Low frequency sine waves generated by nonlinear amplifiers. (1) Ideal (all), (2) linearized Ćuk, and (3) linearized boost and buck-boost.

Table 7.1

	ideal boost	linearized boost	linearized Ćuk
Duty ratio excursion	0.160	0.310	0.212
Peak gain	1.42	1.42	1.42
% Total harmonic distortion	2.70	4.90	1.25

There are other ways to linearize the gain function of the nonlinear amplifiers. One way is to purposely modify the modulator to have a nonlinear gain, that is, the ramp must be of the shape to cancel the nonlinearity in the gain of the amplifier by introduction of a distortion of exactly the opposite shape. In some converter configurations, it is possible to completely linearize the gain characteristics of the converter by addition of a third or more switching topology. A buck-boost example is illustrated in Fig. 7.6a. The timing of the switches are shown in Fig. 7.6b where the switch 1 is ON during $d_1 T_s$ while the others are OFF and so on. It can be shown that the gain function for such a converter is d_1/d_3. If d_3 is held constant, and d_1 and d_2 are modulated according to the input signal, the gain is linear whereby two of these converters constitute a linearized push-pull amplifier. Although the idea is very interesting, in case of the push-pull converters it requires addition of two generally four-quadrant switches to the circuit which have to have the same voltage and current capabilities as do the main switches. This increases the number of active switches, and hence the complexity of the system considerably. However, in the case of the differential amplifiers described in Section 6.2 it has potential applications.

One must notice that the nonlinearities and the linearization process so far spoken of refer to the dc gain characteristics of the amplifiers only. However, owing to the dynamics of the converters and their interaction with the load and source, the introduced distortion is also frequency dependent. For example, a sine wave input generates a

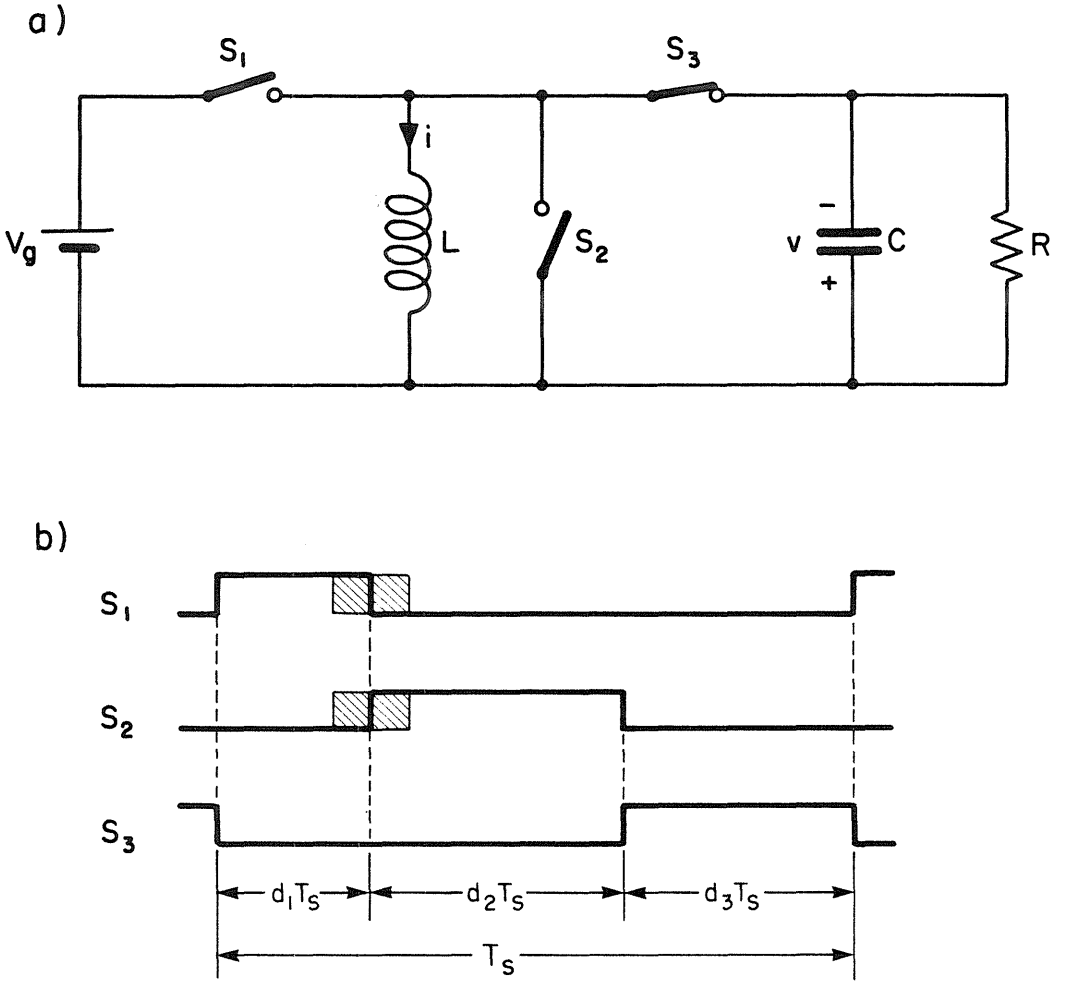


Fig. 7.6 *(a) Linearized buck-boost converter (b) timing for the switches.*

sinusoidal output plus a series of harmonics, and if the converter dynamics have a peak around one of these harmonic frequencies that component is magnified. This phenomenon happens only at certain frequencies where a harmonic of the input and the peak of the converter's response coincide. However, if the dynamics of the converter are wide enough, the output may be considered as a sequence of steady-state solutions of the system for which the foregoing distortion analysis remains valid.

7.2 Control Aspects

Analysis of an amplifier involves an understanding of the dynamics of the two constituent converters and their interactions with each other and the load. However, the main difference is the regular large variation of the operating point versus only occasional perturbation in dc-to-dc converters. The system is nonlinear and its dynamic is related to the operating point and duty ratio; hence the dynamic also experiences large variations. The control system must be designed in such a way as to consider all these facts.

As with the dc gain, in order to correctly include effects of all interactions of the various elements on the dynamics of the system, one must analyze the converter as a whole. The small-signal analysis verifies stability of the system at each operating point. One simplifies the analysis of the nonlinear amplifier to linearized small-signal analyses around each operating point that the converter encounters.

This is the case if the bandwidth of the converters is much larger than the large signal injection frequencies, whereby the output and the states of the system are on a trajectory corresponding to steady-state solutions of various duty ratios. This assumption is practical, very realistic, and simplifies the analyses to those of a series of linear circuits. At each duty ratio and its corresponding steady-state vector, the system may be analyzed by finding the associated small-signal dynamics. If the localized set of the resultant systems is stable, then the design is complete. Again, in analogy to its linear counterpart, the switching converters may be analyzed around the quiescent operating point to obtain design-oriented results. Then, the design is tested against the large-signal variation of the operating point. Therefore, the loop is designed for the small-signal amplifier model around the duty ratio of 0.5 for high performance, and then is checked to be acceptable at other duty ratios. In case of unacceptable performances, the original design is modified and the process continues until a satisfactory result is obtained.

There still are unmentioned a few fundamental differences between the dc and ac systems. In a dc system incorporating feedback loop(s), the output can be regulated to be very close to some preset value. This is possible by use of very high loop gains. One way of obtaining very high gains is to have an integrator in the feedback loop. For dc systems, the regulation is mainly at low frequencies and the integrator has an infinite ideal gain at dc. Therefore such a dc system can have

a theoretically perfect dc regulation. However, in an ac system, the output of interest contains frequencies other than zero, where the integrator has a finite gain. Therefore, a perfect regulation is not possible, but the error may be kept to a satisfactorily low level by proper design. A dc component on the output of an ac system is prohibited, and therefore use of an integrator is highly desirable in order to ensure a zero dc level at the output.

In case of multiple loop feedback systems, special attention must be paid to the development of the error signal. Again, the correct combination must be intensified in the frequency range of interest. For example, if the output voltage is the quantity to be regulated, and both the output voltage and input current are being sensed and returned, the output voltage must be highlighted to produce the correct form in the output. This can be done either by use of the output voltage integral or by insertion of a high-pass filter in the current path, or a combination of both. At the nominal output frequency (and preferably higher), the output voltage component of the error signal must be much greater than the other components. In nonlinear amplifiers, a sinusoidal variation of output does not imply sinusoidally varying states. An improperly derived error signal therefore can degrade the output impedance and other characteristics of the amplifier as well as introduce distortion.

With all these constraints in mind, one can start to analyze the system. As mentioned earlier, the analysis is performed around the quiescent point and then checked for other operating points. In

push-pull amplifiers the quiescent point is at duty ratio D = 0.5 where the system is symmetric. At D = 0.5, the two constituent converters do have exactly the same conditions, so they will have the same frequency characteristics at their outputs. That is, owing to the complete symmetry, one may be able to analyze the complete circuit by considering only one converter. However, at other duty ratios the loading of one converter by the other is such that the two cases are not exactly the same. So, in order fully to understand the dynamics of the amplifier, the total system must be considered.

The procedure is clarified by the example of the boost amplifier introduced in Section 7.1. The state equations are repeated here for convenience:

$$P\dot{x} = Ax + Bu$$

where

$$P = \begin{bmatrix} L & 0 & 0 & 0 \\ 0 & L & 0 & 0 \\ 0 & 0 & C & 0 \\ 0 & 0 & 0 & C \end{bmatrix}, \quad A = DA_{11} + D'A_{22} = \begin{bmatrix} -R_\ell & 0 & -D' & 0 \\ 0 & -R_\ell & 0 & -D \\ D' & 0 & -\frac{1}{R} & \frac{1}{R} \\ 0 & D & \frac{1}{R} & -\frac{1}{R} \end{bmatrix},$$

$$B = \begin{bmatrix} 1 \\ 1 \\ 0 \\ 0 \end{bmatrix} \qquad (7.14)$$

$$x = \begin{bmatrix} i_1 \\ i_2 \\ v_1 \\ v_2 \end{bmatrix}, \quad u = V_g, \quad A_{11} - A_{22} = \begin{bmatrix} 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & -1 \\ -1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \end{bmatrix},$$

$$B_{11} - B_{22} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

Perturbation and linearization of the first equation results in:

$$P\hat{\dot{x}} = A\hat{x} + B\hat{u} + [(A_{11} - A_{22})X + (B_{11} - B_{22})U]\hat{d} \tag{7.15}$$

and

$$(sP - A)\,\hat{x}(s) = B\hat{u}(s) + [(A_{11} - A_{22})X + (B_{11} - B_{22})U]\hat{d}(s) \tag{7.16}$$

Substitute Eq. (7.14) into Eq. (7.16) to find the control-to-output transfer functions

$$\begin{bmatrix} sL+R_\ell & 0 & D' & 0 \\ 0 & sL+R_\ell & 0 & D \\ -D' & 0 & sC+\frac{1}{R} & -\frac{1}{R} \\ 0 & -D & -\frac{1}{R} & sC+\frac{1}{R} \end{bmatrix} \begin{bmatrix} i_1(s) \\ i_2(s) \\ v_1(s) \\ v_2(s) \end{bmatrix} = \begin{bmatrix} V_1 \\ -V_2 \\ -I_1 \\ I_2 \end{bmatrix} \hat{d}(s) \tag{7.17}$$

At duty ratio D = 0.5, the steady state values are as follows:

$$I_1 = I_2 = 0 \tag{7.18a}$$

$$V_1 = V_2 = \frac{V_g}{D} = 2V_g \tag{7.18b}$$

The duty ratio-to-output transfer function $H(s) = \left(\hat{v}_1(s) - \hat{v}_2(s)\right)/\hat{d}(s)$ is then derived from Eq. (7.17) in which Eq. (7.18) is substituted

$$H(s) = 8V_g \frac{1 + 4R_\ell Cs + 4LCs^2}{\Delta} \tag{7.19a}$$

and

$$\Delta = \left(1 + 8\frac{R_\ell}{R}\right) + \left[8\frac{L}{R} + R_\ell C\left(32\frac{R_\ell}{R} + 8\right)\right] s + \left[LC\left(8 + 64\frac{R_\ell}{R}\right) + 16\,R_\ell{}^2C^2\right]s^2$$

$$+ \; 32LC\left(\frac{L}{R} + R_\ell C\right) s^3 + \; 16L^2C^2s^4 \tag{7.19b}$$

Notice that the denominator of Eq. (7.19) can be factorized as follows:

$$\Delta = \left(1 + 4R_\ell Cs + 4LCs^2\right)\left[1 + 8\frac{R_\ell}{R} + \left(8\frac{L}{R} + 4R_\ell C\right) s + 4LCs^2\right] \tag{7.20}$$

in which the first term exactly cancels out the numerator of Eq. (7.19a), resulting in

$$H(s) = 8V_g \frac{1}{1 + 8\frac{R_\ell}{R} + \left(8\frac{L}{R} + 4R_\ell C\right) s + 4LCs^2} \tag{7.21}$$

The cancellation of numerator may seem coincidental at first, but it is explained by the symmetry of the circuit and the fact that at duty ratio D = 0.5 the two converters do not load each other. However, the matching happens only at D = 0.5, and at other operating points current is drawn which changes the position of the zeros as well as the poles that are dependent on duty ratio. Since the feedback is designed around a duty ratio of 0.5, one may simplify the analysis by considering only one converter. However, owing to the strong dependence of the dynamics upon the steady-state X vector, the complete amplifier and the single converter substitute must have the same steady-state conditions. Thus, while the converter of Fig. 7.7a gives the wrong dynamics, the one shown in Fig. 7.7b with the steady-state X vector compensated for, generates the correct results for the quiescent operating point of the total amplifier. Therefore, the analysis of the total amplifier at D = 0.5 is reduced to that of a converter with proper conditions (to first order).

Although this simplifies the design phase of the system, a complete analysis requires verification of the dynamics around each duty ratio. The general analysis cannot be simplified because the converters have different dynamics at different duty ratios and each imposes its response on the load. Consequently, the complete amplifier must be considered. For example, at D = 0.5, Eq. (7.19), shows two poles and zeros which are exactly on top of each other and thus cancel. However, at duty ratios other than 0.5, the poles and zeros move to different locations. Since they are high Q poles and zero pairs, this movement causes a glitch in the response. Furthermore, at duty ratios other

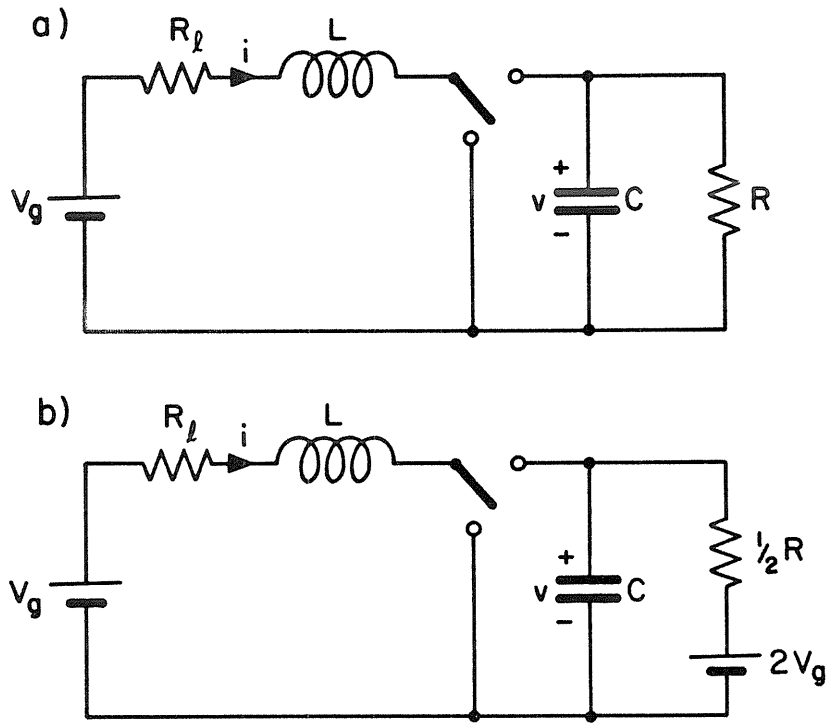


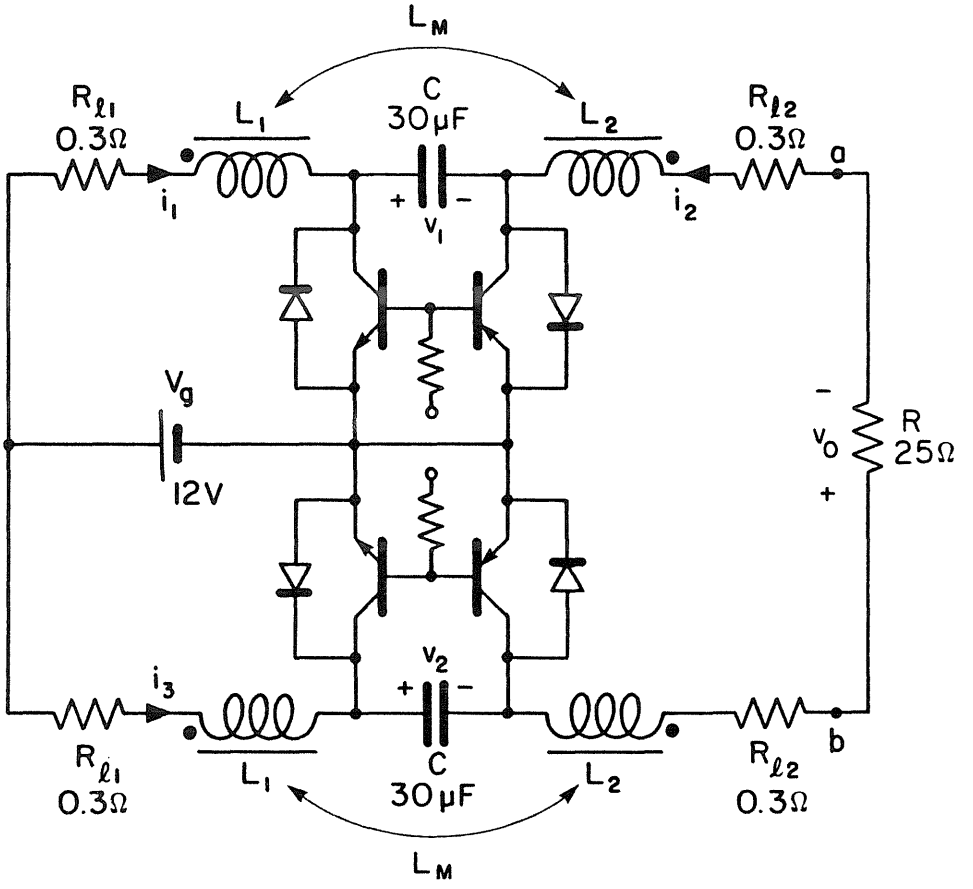
Fig. 7.7 *Analysis of amplifier considering one converter. (a) Wrong conditions, (b) correct conditions.*

than 0.5, another zero appears in the response whose position is again related to duty ratio. As excursion of duty ratio from 0.5 increases, one of these zeros may enter the right half-plane. If the feedback circuitry is not designed for this movement, the system may go unstable.

It must be noticed that the above discussion refers to nonlinear gain amplifiers. The buck amplifier is a simple case in which the positions of neither the poles nor the zeros are dependent on duty ratio or steady-state conditions. Therefore, the design, once made, is final and no further verifications are required. This, along with the linear dc gain characteristic of the power stage, makes the buck amplifier an attractive choice. Nonetheless, the nonlinear amplifiers have higher gains to allow reproduction of a certain output with much lower duty ratio excursions. With small excursions, the position of poles do not change considerably, while the zeros still can move in the s-plane over a wide range. To design the loop, one may first try an ordinary single loop system. If unsuccessful, multiple-loop feedback can be the answer.

7.3 Experimental Verification – Ćuk Amplifier

The design of a coupled-inductor Ćuk amplifier [7,11] is reviewed in this chapter. The topology is a nonlinear one and the coupled-inductor version provides a very low ripple on the output current. In fact, with proper design, one can completely cancel the output ripple, and with such a configuration one may eliminate altogether the capacitors on the output ports. Figure 7.8 shows the basic amplifier section with



$L_1 = L_M = 1\text{mH}$

$L_2 = 1.05\text{mH}$

Fig. 7.8 Experiment coupled-inductor Ćuk amplifier.

the output capacitors removed.

Despite the coupling of inductors, to first order, the dc analyses of this amplifier and the uncoupled version are the same (since for dc calculations, the ripples are generally ignored). For this reason, the dc analysis done in Section 7.1 is still valid and shows that for a maximally expanded region of linearity in the dc gain characteristic, one needs a total of 1/14 of the load resistance in series with the input inductance ($R_{\ell 1}/R = 1/14$). This approach, while improving the distortion problem, has an undesirable effect on efficiency. So, this method involves a compromise between distortion and efficiency. One way to minimize the problem is to keep the resistance $R_{\ell 1}$ as low as possible for better efficiency and stable dynamics and transfer the correction of the distortion to the feedback loop.

Analysis of the control-to-output transfer function of the amplifier starts with the state-space equations in each switching interval. When the upper npn transistor in Fig. 7.8 is on, it represents the DT_s interval while an inverse situation represents the $D'T_s$ interval. Each converter has three states, but owing to cancellation of one state at the output circuit, the amplifier has only five independent states. After writing state equations in each position of the switch and performing the averaging process, one obtains the following:

$$\begin{bmatrix} L_1 & L_M & 0 & 0 & 0 \\ 0 & -L_M & L_1 & 0 & 0 \\ L_M & 2L_2 & -L_M & 0 & 0 \\ 0 & 0 & 0 & C & 0 \\ 0 & 0 & 0 & 0 & C \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} -R_{\ell 1} & 0 & 0 & -D' & 0 \\ 0 & 0 & -R_{\ell 1} & 0 & -D \\ 0 & -R-2R_{\ell 2} & 0 & D & -D' \\ D' & -D & 0 & 0 & 0 \\ 0 & D' & D & 0 & 0 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ v_1 \\ v_2 \end{bmatrix} + \begin{bmatrix} 1 \\ 1 \\ 0 \\ 0 \\ 0 \end{bmatrix} v_g$$

$$P \qquad \dot{x} = \qquad A \qquad x \quad + \quad B\ u \qquad (7.22)$$

The Laplace transform is now taken, and steady-state conditions are substituted for the k vector. In order to simplify the algebra, we absorb $R_{\ell 1}$ and $R_{\ell 2}$ into $L_1 s$ and R respectively, that is, substitute $L_1 s$ for $L_1 s + R_{\ell 1}$ and R for $R + 2R_{\ell 2}$. Later in this section we recover the full result by making the reverse substitution. With this simplification, one gets:

$$\begin{bmatrix} sL_1 & sL_M & 0 & 0.5 & 0 \\ 0 & -sL_M & sL_1 & 0 & 0.5 \\ sL_M & 2sL_2+R & -sL_M & -0.5 & 0.5 \\ -0.5 & 0.5 & 0 & sC & 0 \\ 0 & -0.5 & -0.5 & 0 & sC \end{bmatrix} \begin{bmatrix} \hat{i}_1(s) \\ \hat{i}_2(s) \\ \hat{i}_3(s) \\ \hat{v}_1(s) \\ \hat{v}_2(s) \end{bmatrix} = \begin{bmatrix} 2 \\ -2 \\ 4 \\ 0 \\ 0 \end{bmatrix} V_g\, \hat{d}(s) \qquad (7.23)$$

One may find the control transfer function $H(s) = R\, \hat{i}_2(s)/\hat{d}(s)$ by use of Cramer's rule. The following is obtained:

$$H(s) = 8V_g \frac{1 + 2C(L_1 - L_M)s^2}{1 + 2\frac{L_1+2L_M+L_2}{R}s + 4L_1Cs^2 + 8\frac{C(L_1L_2-L_M^2)}{R}s^3} \qquad (7.24)$$

in which the common factor $(1 + 4L_1Cs^2)$ in numerator and denominator has been cancelled.

It turns out that the matching condition under which the zero ripple condition exists [11] can be modelled by $L_1 = L_M$. Then, with the definition $L_2 = L_M + L_e$, substitution into Eq. (7.24) results in

$$H(s) = \frac{8V_g}{1 + 2\frac{4L_M+L_e}{R}s + 4L_MCs^2 + 8\frac{CL_ML_e}{R}s^3} \qquad (7.25)$$

Provided that $R >> 2\sqrt{L_e/C}$, the denominator can be further approximated into two factors

$$H(s) \simeq \frac{8V_g}{\left(1 + 2\frac{L_e}{R}s\right)\left(1 + 8\frac{L_M}{R}s + 4L_MCs^2\right)} \qquad (7.26)$$

This shows the presence of a complex pole pair at moderate frequencies with another real pole at high frequencies. There are no zeros, and with the real pole being at high frequencies, the circuit behaves essentially as a two-pole system which can be regulated by use of classical control theory. With the actual values shown on Fig. 7.8, the approximate poles are found to be

f_{p1} = 39.8 kHz (39.4 kHz)

f_{p2} = 459 Hz (462 Hz) Q_{p2} = 1.08 (1.08)

The exact poles directly calculated from Eq. (7.25) are shown in parentheses beside each value to confirm the accuracy of the approximate results.

The calculations carried out so far neglect the parasitics. However, parasitics can be included by simple resubstitutions of $L_1 s + R_{\ell 1}$ for $L_1 s$ and $R + 2R_{\ell 2}$ for R in Eq. (7.24):

$$H(s) = H_0 \frac{1 + 2R_{\ell 1}Cs}{1 + \frac{2R_{\ell 1}}{R+2R_{\ell 2}} + \left(\frac{4L_M+L_e}{R+2R_{\ell 2}} + 4R_{\ell 1}C\right)s + \left(4L_M+8\,\frac{R_{\ell 1}}{R+2R_{\ell 2}}\,L_2\right)Cs^2 + 8\,\frac{CL_ML_e}{R+2R_{\ell 2}}\,s^3}$$

where

$$H_0 = 8V_g \frac{R}{R + 2R_{\ell 2}} \tag{7.27}$$

Comparison of Eq. (7.27) with the previous result of Eq. (7.25) shows that the parasitics have lowered the gain, slightly modified the position of the poles and their Q, and finally have created a new zero by interaction with the energy transfer capacitor C. Also, change of R only modifies the Q of the resonance. The thick lines in Fig. 7.9 show the control-to-output transfer function of Eq. (7.27) superimposed on the measurement results shown by thin lines. The close agreement shows the degree of accuracy of the calculations. Since the system is

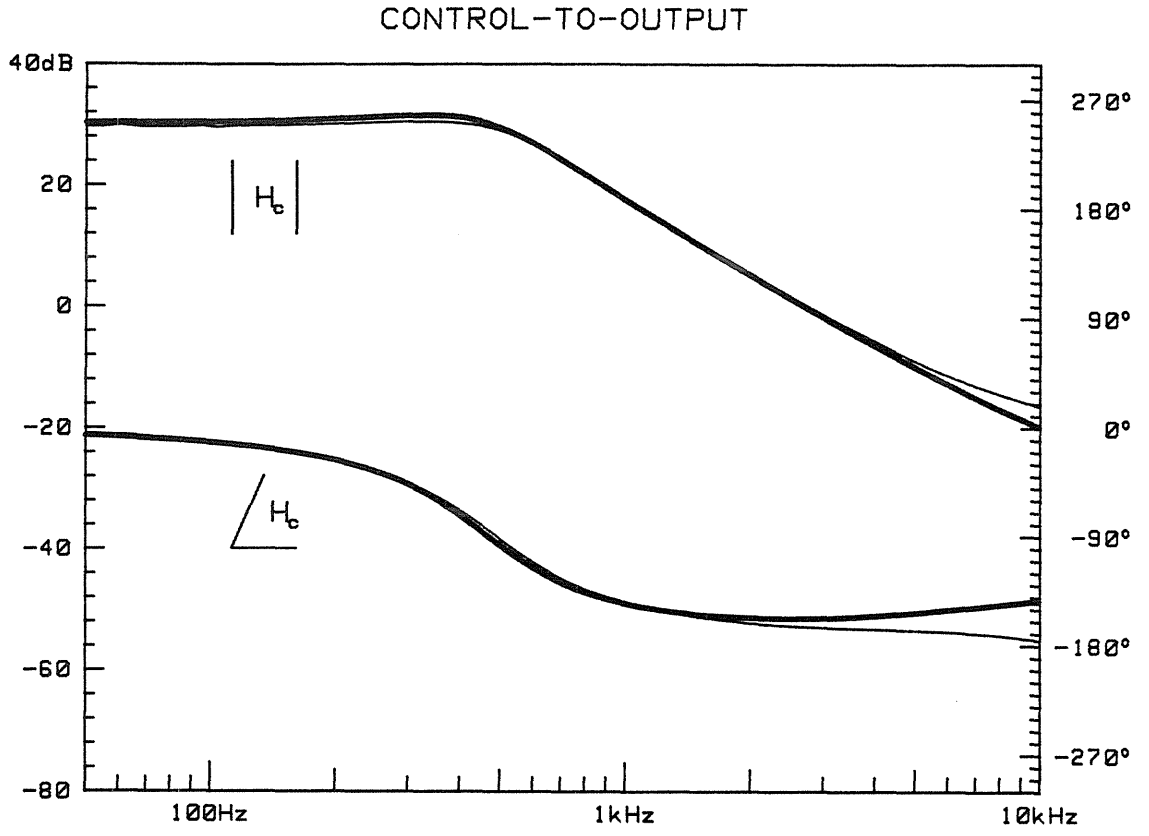


Fig. 7.9 Predicted (thick lines) and measured (thin lines) control-to-output transfer function of the Ćuk amplifier.

essentially second-order, design of the feedback loop is simple and is done by insertion of a zero in the loop. Figure 7.10 shows the simple feedback compensation network used in the actual circuit, in which V_e is the error which passes through the compensation network to the modulator, v_c. The lead-lag network comprised of R_1, R_2, and C_1 generates a zero and a pole for phase correction purposes, and C_2 is the integrator capacitor. The resistor around C_2 is for simulation of the limited gain of the operational amplifier and is not physically present. Although there will be some output error owing to the finite loop gain, the integrator can null the dc part of the output voltage completely. The integrator can also be used to boost the loop gain at low frequencies to reduce the error and thus improve the distortion problem. However, in this case, the duty ratio deviation from the quiescent value of 0.5 must be small (0.1 max).

The addition of a moderate amount of loop gain improves the distortion to an acceptable point, and the integrator in this case was used solely for dc cancellation (see Chapter 9). Figure 7.11 shows the result of theoretical calculations (thick lines) and actual measurement (thin lines) superimposed. The calculated phase margin is 67 degrees. The phase discrepancy arises because the capacitor C_3 in Fig. 7.10, which was added to reduce noise, was not considered in the calculations.

All that remains to be checked is the sensitivity of the loop gain to the operating point. In this case, only the control transfer function need be checked, because the remaining poles and zeros are due to the compensation network and are not duty ratio dependent. The

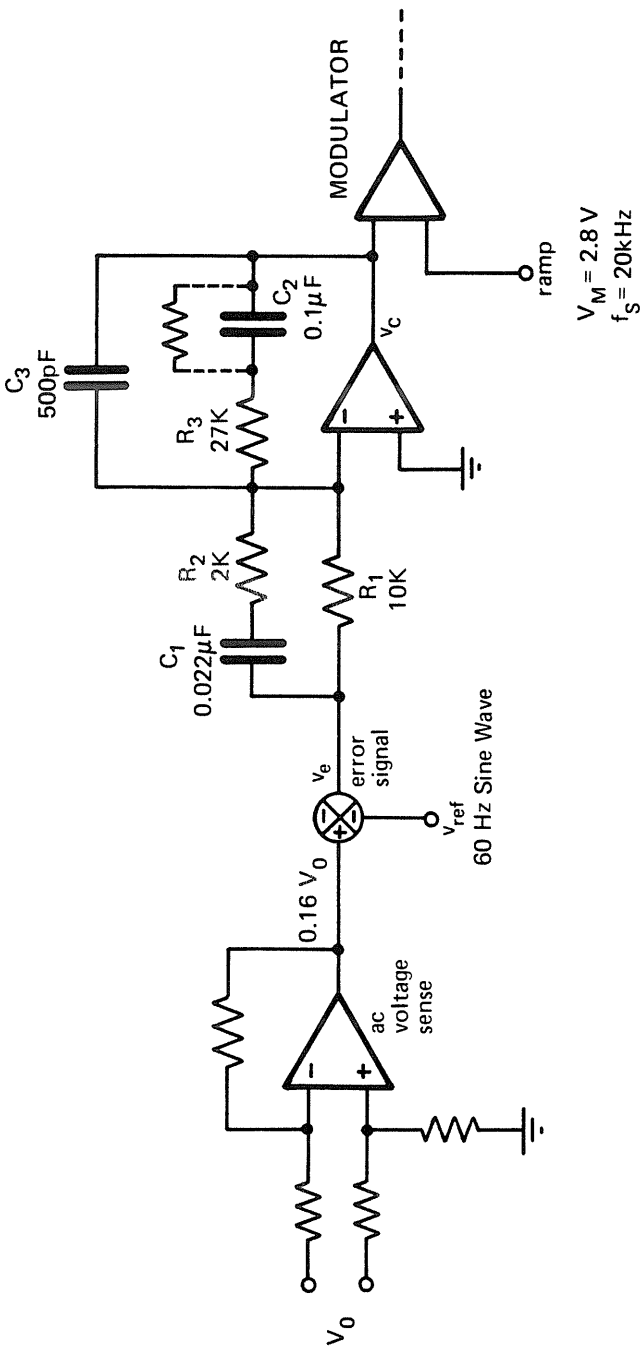


Fig. 7.10 Complete control circuitry of the Ćuk inverter.

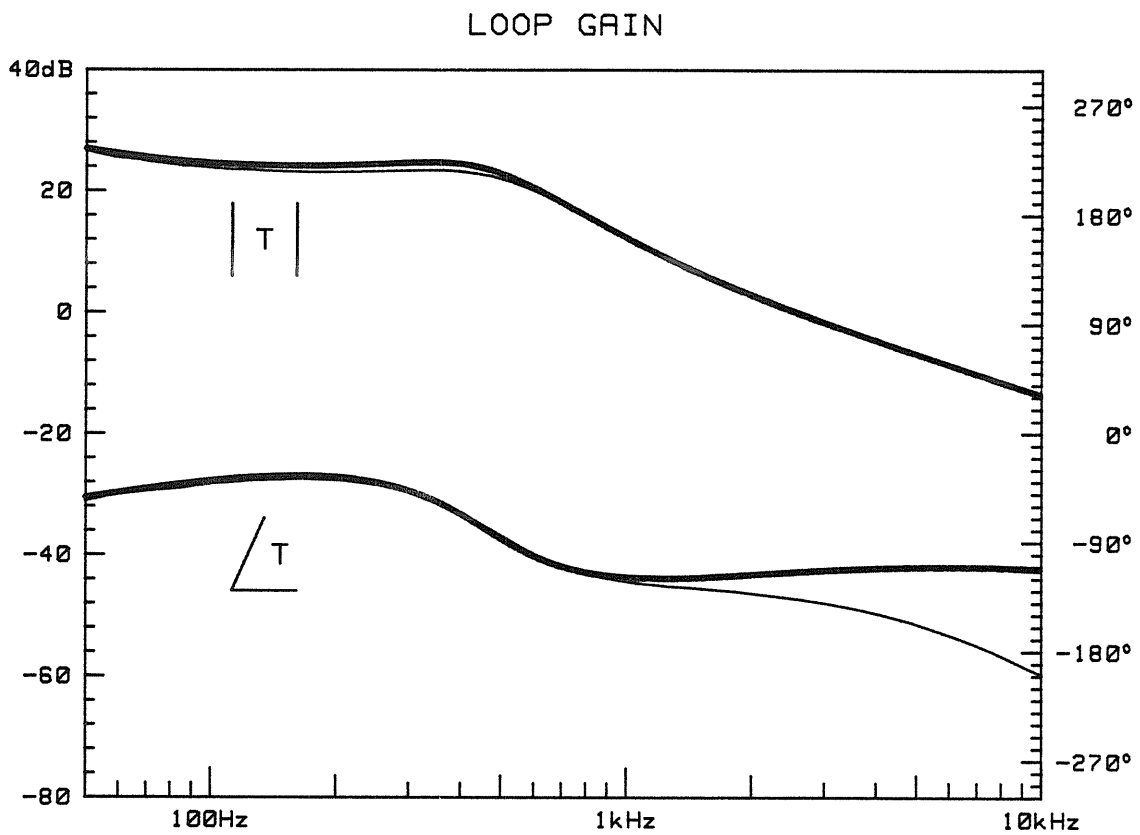


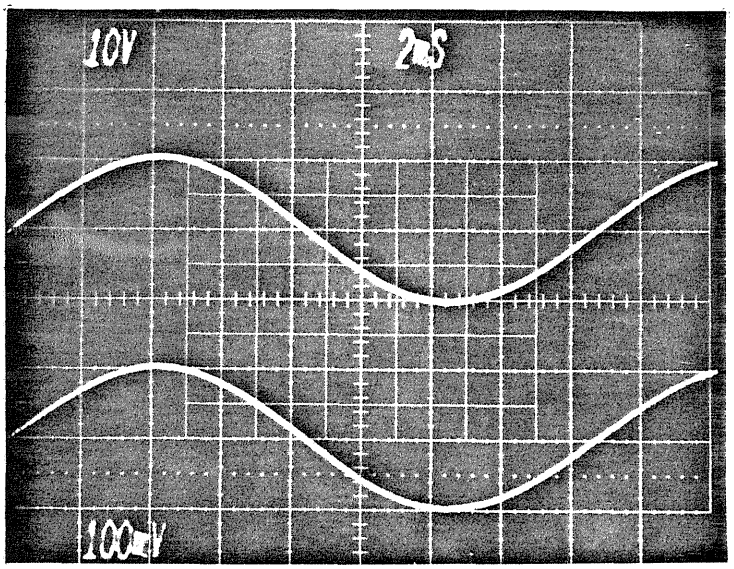
Fig. 7.11 Loop gain. Thick lines: Prediction. Thin lines: Measurement.

calculation shows a strong dependence of the control transfer function zeros upon the parasitics. For example, at a duty ratio of 0.5, Eq. (7.24) shows a pair of zeros on the imaginary axis if $R_{\ell 1}$ and $R_{\ell 2}$ are ignored. At any duty ratio other than 0.5, these zeros move to the right half-plane, which makes design of the control much more difficult. However, this movement is very small, and addition of a very small amount of parasitic $R_{\ell 1}$ solves the problem. The common factor in the numerator and denominator, $1 + 4L_1Cs^2$, changes to $1 + 4R_{\ell 1}Cs + 4L_1Cs^2$, giving a negative real part to poles and zeros. If $R_{\ell 1}$ is large enough, the changes of duty ratio over the whole range can bring the zeros closer to the imaginary axis, but the zeros will never cross it. In the present example, the inherent parasitics of the circuit $R_{\ell 1} = R_{\ell 2} = 0.3\ \Omega$ were enough to keep the zeros in the left half-plane.

Owing to symmetry of the amplifier around duty ratio of 0.5, the conditions at duty ratios of D = 0.5 + a and D = 0.5 - a are the same, so excursions on only one side need be considered. Table 7.2 shows the placement of the poles and zeros of the loop gain and the two extremes of duty ratio. Calculation of the loop gain at duty ratio of 0.6 (D_{max}) shows a phase margin of 56 degrees. Therefore, all the design steps have been correct and the design of the inverter is complete. Figure 7.13 shows an oscillogram of the output voltage and current of the amplifier taken from the actual circuit. The duty ratio was extended beyond the normal limit of 0.6, and the circuit still exhibited a good degree of stability.

Table 7.2

D = 0.5		D = 0.6	
i_1 = 0		i_1 = 0.568 A	
i_2 = 0		i_2 = 0.377 A	
i_3 = 0		i_3 = -0.252 A	
v_1 = 24 V		v_1 = 29.6 V	
v_2 = 24 V		v_2 = 20.1 V	
Poles			
459 Hz	Q = 9.62	485 Hz	Q = 3.56
461 Hz	Q = 1.01	421 Hz	Q = 1.15
41.3 kHz	Real	41.3 kHz	Real
Zeros			
459 Hz	Q = 9.62	466 Hz	Q = 32
8.84 kHz	Real	28.8 kHz	Real



0.4A/div.

Fig. 7.12 Output voltage and current waveforms of the amplifier.

7.4 Review

Switched-mode *push-pull* power amplifiers are discussed in detail. The amplifier module contains two current-bidirectional dc-to-dc converters and a modulator with complementary outputs. The load is placed differentially on the outputs of the converters. The ideal 100% efficiency is not the only difference between switching amplifiers and their linear counterparts. A full-power sine wave can be generated at the load as long as the open-loop amplifier is capable of doing so. That is, the power bandwidth of the system is equal to its *open-loop* bandwidth. Furthermore, a system with a power bandwidth much larger than its input signal frequency, is assumed to pass through a series of steady-state conditions. It was shown that except for the buck amplifier, the other types of converters have nonlinear dc gain characteristics which produce an overall nonlinear gain. However, the gain is much higher, and addition of small parasitics was shown to linearize the dc gain characteristic to a considerable extent. Furthermore, the large-signal variations of duty ratio and states of the system results in movement of the poles and zeros of the control transfer function. As an analogy to the linear amplifiers, the feedback loop is designed around a nominal quiescent operating point and then is checked for stability at the maximum excursions. At a duty ratio of 0.5 (the quiescent operating point) the two constituent converters of the system are exactly at the same conditions. The system's control response can then be analyzed by examination of only one converter provided the same steady state and loading conditions are preserved. It

was shown that the usual right half-plane zeros of the converters *do not* appear in the response since they are generated by currents which are in this case zero. Since no dc is allowed in the ac output, a very high loop-gain at dc is mandatory. The feedback design is performed following the preceding simplifications and guidelines. Then, the loop gain is tested for possible variations caused by dependence of the amplifier dynamics on the operating point. Finally, these points were experimentally verified by an amplifier composed of two coupled-inductor Ćuk converters. The amplifier has a bandwidth of about 500 Hz which is much higher than 60 Hz (which it is intended to amplify). In this case, little attempt was made to linearize the dc gain. A thorough examination of the dynamics showed an effective two-pole response for the control characteristic of the amplifier, and the feedback loop was then easily designed. The importance of the parasitic shows up in analysis of the system at non-quiescent operating conditions. It was shown that even small values of parasitic resistances are enough to prevent movement of some zeros to the right half-plane. Thus the parasitics, even though undesirable from the efficiency point of view, can improve both the dc and ac performances of an amplifier. This completes the design of the inverter. However, being part of the single-stage UPS, the same amplifier is used in the ac-to-dc conversion as well. The requirements of the latter mode of operation may impose some additional constraints on the power stage such that a refinement of the inverter design becomes necessary.

CHAPTER 8

AC TO DC CONVERSION — BATTERY CHARGER

A switched-mode amplifier is a four-quadrant converter, capable of having bipolar voltages *and* currents on its output. At any moment, one constituent converter of the amplifier is processing power from dc to ac side, while the other converter does the reverse. In the last chapter, the inverter case was considered where the output is attached to a passive load. Then the direction of the net power is from the dc side to the ac side, since more power is processed toward the ac side than the returning power and the difference is dissipated by the load. This is the "normal" or "inverter" mode of operation.

However, the direction of power flow is not limited to that of an inverter. This is because the direction of the voltage and the current on the ac side do not necessarily have to have a prescribed relationship and can be independent of each other. When a passive load is connected to the ac side, it determines this relationship. So, for example, when a reactive load is sinusoidally excited, in part of the cycle it consumes power while in the rest of the cycle, it returns some power back to the amplifier and thus to the battery. The difference is dissipated in the load, so the net power is still toward the ac side. If now instead of the load (power sink), one uses a power source, it is possible to change the net flow of power from the ac side to the dc side.

This is the "reverse" or "charger" mode of operation. In this part, the amplifier refers to the general circuit shown in Fig. 6.9, and the terms "inverter" and "charger" simply refer to the modes of operation from dc to ac and from ac to dc, respectively. The ac and dc sides are referred to as ports because the bidirectionality of the amplifier makes the usual input and output definitions ambiguous.

The first section describes various aspects of the "charger" mode of operation. The roles of input and output change, and the amplifier is converted to an ac-to-dc charger. However, the conversion process is fully controllable. Then, the current is shaped to be proportional to the voltage and hence *unity power factor* conversion is performed.

Section 8.2 examines the circuit from the control point of view since the dynamics of the system experience a drastic change from the inverter mode. The results are experimentally demonstrated in Section 8.3, where the same Ćuk amplifier of Section 7.3 is analyzed for the reverse mode of operation. The mandatory feedback is designed around the system and the comparison of the measurements and predictions concludes this section.

8.1 Description of the Method

This section describes the behavior of a push-pull amplifier when its load is replaced by an ac voltage source. Without the added ac voltage source, output of the amplifier (ac port) is practically a voltage source. The output impedance of the amplifier is generally very low and especially at low frequencies, it is determined by the parasitic

resistances of the amplifier's components. At higher frequencies, the converter dynamics mostly determine the impedance. Therefore, when the ac voltage source is added to the ac port, there will be a low impedance voltage source in parallel with another one. The result will be very large currents in case of small voltage mismatches between the two sources. Furthermore, the smaller the parasitics get, the more intensified this problem becomes. An ideal amplifier with no parasitic resistances is open-loop marginally stable. This makes incorporation of a feedback network in the amplifier mandatory. The feedback must change the ac port impedance of the amplifier to a high value such that the interaction of the ac voltage source and the amplifier is reduced. Ideally, if this impedance is infinite — a current source — there will be no interactions between the two sources, and the controllable source, namely the amplifier, determines the amount of current. The feedback, as illustrated in Fig. 8.1, must then tightly regulate the ac *current* of the amplifier to make it follow a reference signal. Having an adjustable current provides many capabilities previously not possible. For example, if as illustrated in Fig. 8.1, the reference signal of the feedback loop is tied to the ac voltage source, the feedback forces the current to be proportional to the voltage. The line (ac source) therefore, interprets the amplifier as a resistor. The circuit now becomes a unity power factor battery charger. The thick line of Fig. 8.2a shows the ac voltage, while the thin line denotes the current (determined by the feedback). The dash-dot line is the instantaneous power input and therefore, by the assumption of 100% efficiency, is

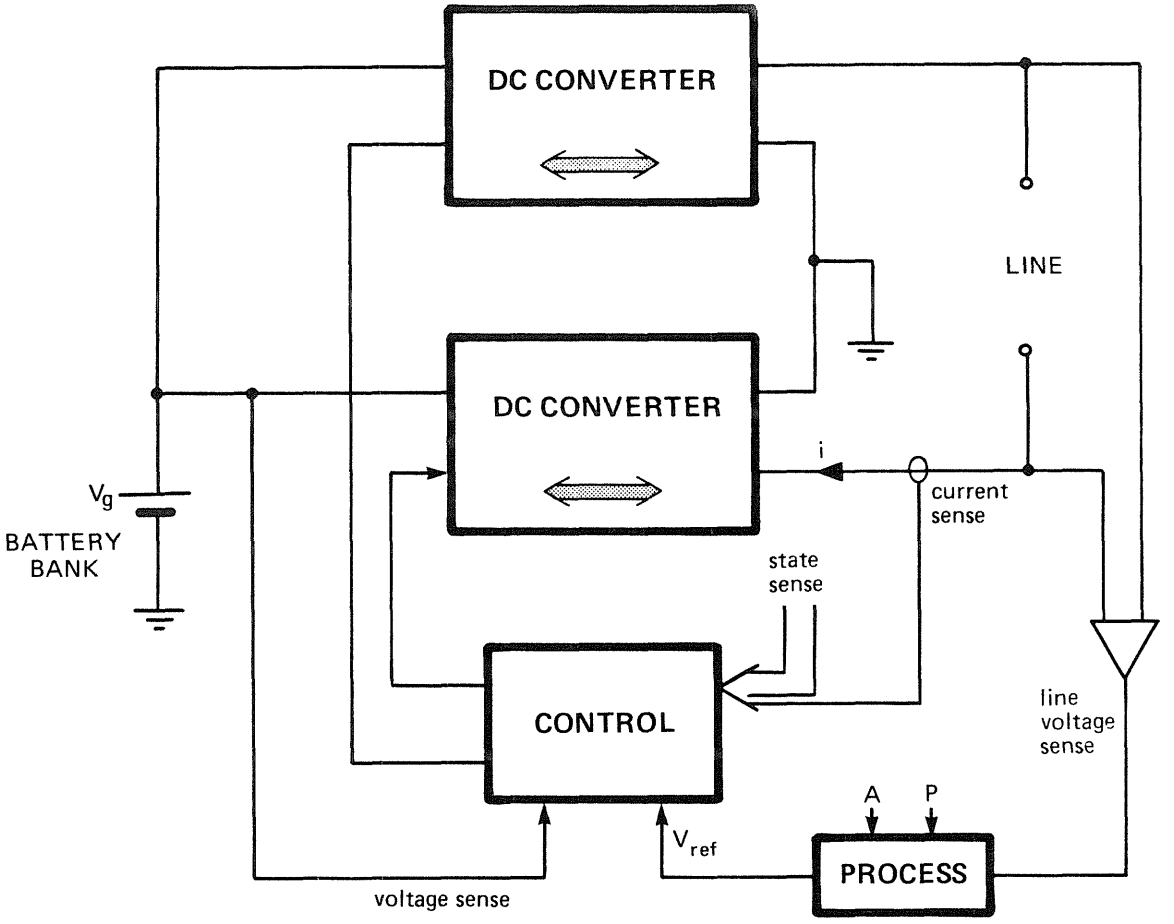


Fig. 8.1 *Basic structure of the battery charger. The control circuit causes current to be proportional to the reference signal which itself is an amplitude-phase adjusted replica of the input voltage.*

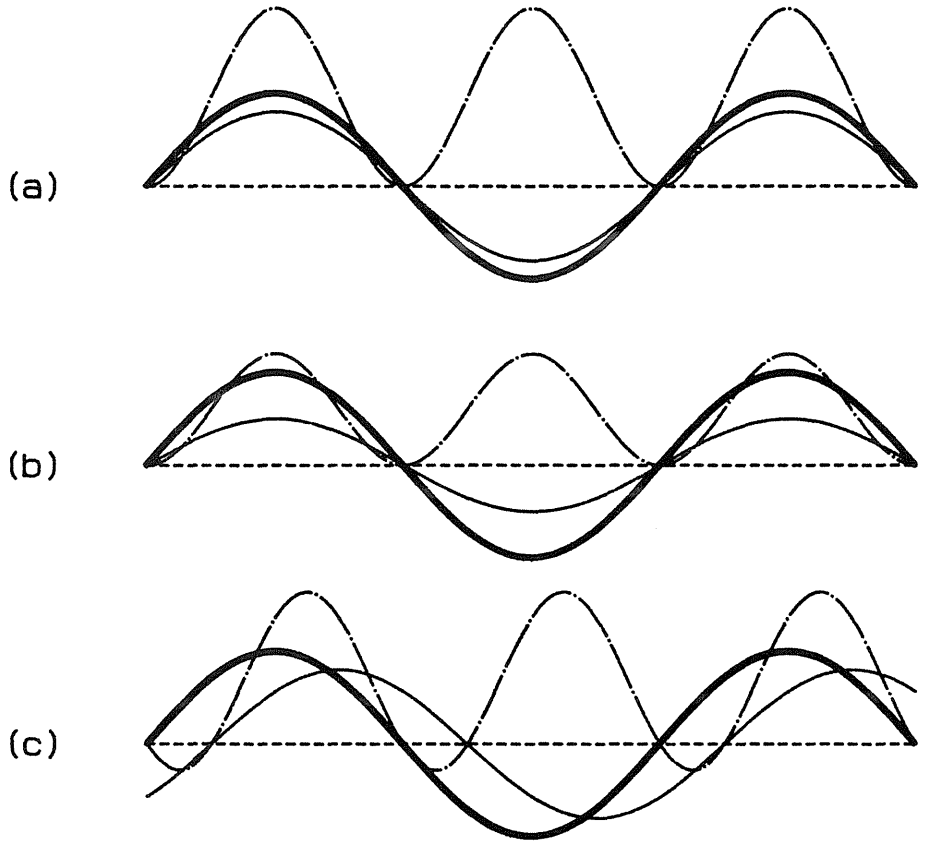


Fig. 8.2 Modes of operation of the battery charger. (a) High power resistive, (b) low power resistive, and (c) inductive. The voltages, currents, and powers are represented by thick, thin, and dash-dot lines, respectively.

also the charging current of the battery. The amount of power processed depends on the magnitude of the current. Less current amplitude shown in Fig. 8.2b causes delivery of less power to the battery. On the other hand, if the feedback's reference is phase-shifted with respect to the ac voltage, the current drawn from the ac line will also have a phase displacement with the line voltage. This allows simulation of inductive or capacitive loads on the line. In Fig. 8.2c the inductive example is shown; negative instantaneous power during part of the cycle signifies the fact that the battery is being discharged during this portion of the cycle. The control on phase and amplitude of the reference signal versus the ac voltage is modelled by the process box in Fig. 8.1 with A (amplitude) and P (phase) inputs. The throughput power is varied by exercising either of these controls. Therefore, these controls may be used inside a larger (and slower) feedback loop, when a control of the battery charging process is required.

In UPS applications, in order to charge the battery fast, the current level is set at its maximum level. When the battery is charged, the current level is reduced to a minimum level, just enough to overcome the losses of the circuit and the battery. The phase control method may be used to compensate for the other non-unity power factor devices on the line, such that it compensates their reactive currents and the total load on the line becomes a unity power factor. The phase-shift may be continued to $\pm$ 90 degrees where the amplifier behaves as a pure inductance or capacitance with applications in power factor correction facilities. At this phase angle, the net power flow is zero, while

increase of the angle beyond 90 degrees changes the sign of the power flow direction. That is, now the power flows from the battery to the line. The amplifier functions as an interface between the ac line and the battery.

One may remove the battery completely, and insert a parallel combination of a capacitor and a load. This is a unity-power-factor ac-to-dc converter. However, owing to the fact that the input power is pulsating (battery currents in Fig. 8.2), the added capacitor must be very large. The capacitor must absorb the current ripple whose frequency is twice that of the line frequency. At best, the current peak is twice the average current rendered to the load. The output will have a twice-the-line-frequency ripple whose amplitude depends on the capacitor, load, current and the load voltage.

8.2 Control Aspects

Unlike the inverter case, the charger must regulate the ac current rather than voltage. This section discusses ways to control this current. This is not the only difference between the two modes of operation and, there are some distinct properties which characterize the charger mode.

As was described in Section 8.1, the open-loop characteristics (ac port impedance) of the amplifier is far from the desired shape for the charger mode while closely resembling the desired shape for the inverter mode. Therefore, the charger owing to the large discrepancy between the open and closed loop performances, requires large loop gains

and, except in very special cases, cannot operate open-loop.

The current control also permits a variable rate of exchange of power. That is, the closed-loop characteristics of the system will be adjustable. In the inverter, the ac voltage is set by the converter and the load determines the current, while in the charger, the voltage is predetermined and the converter — acting as a load — must have variable characteristics to be able to control the amount of current and power (Fig. 8.2).

First the steady-state currents are examined. Here, the open-loop currents can be found only if the parasitic resistances are included. Absence of resistive elements causes the interaction between the stages to be higher than that of the inverter mode. In order to include all the interaction of various components on the dynamics of the system, the total amplifier must be analyzed to find out the relation between the output current, dc and ac source voltages, and duty ratio. In general, one expects a nonlinear dependence of output current on duty ratio and a linear dependence on dc and ac voltages. To be consistent, consider the boost converter of Fig. 8.3 with the parasitic resistances of inductor and capacitor included. The ESR of the capacitors are included to remove ambiguity that will arise later in the ac calculations. Also, for this analysis the ac output voltage is slowly varying and considered constant. Assuming $x^T = [i_1 \; i_2 \; v_1 \; v_2]$ and $u^T = [v_g \; v_s]$, the extended state-space averaging results in:

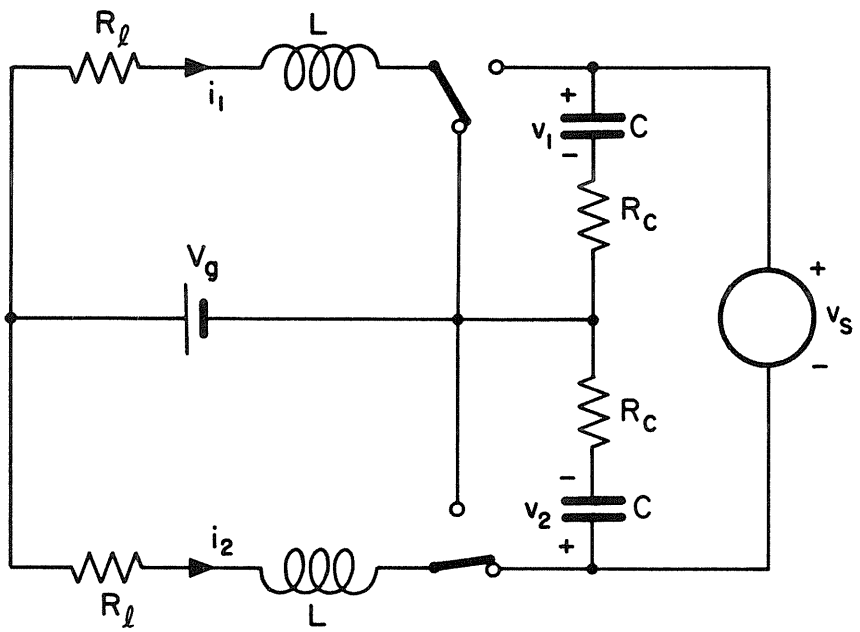


Fig. 8.3 *Boost amplifier example with inductor and capacitor resistive parasitics.*

$$P\dot{x} = Ax + Bu$$
$$y = Cx + Eu \tag{8.1}$$

where:

$$P = \begin{bmatrix} L_1 & 0 & 0 & 0 \\ 0 & L_2 & 0 & 0 \\ 0 & 0 & C_1 & 0 \\ 0 & 0 & 0 & C_2 \end{bmatrix} \quad A = \begin{bmatrix} -R_\ell - D'\frac{R_c}{2} & 0 & -\frac{D'}{2} & -\frac{D'}{2} \\ 0 & -R_\ell - D\frac{R_c}{2} & -\frac{D}{2} & -\frac{D}{2} \\ \frac{D'}{2} & \frac{D}{2} & -\frac{1}{2R_c} & \frac{1}{2R_c} \\ \frac{D'}{2} & \frac{D}{2} & \frac{1}{2R_c} & -\frac{1}{2R_c} \end{bmatrix},$$

$$B = \begin{bmatrix} 1 & -\frac{D'}{2} \\ 1 & \frac{D}{2} \\ 0 & \frac{1}{2R_c} \\ 0 & -\frac{1}{2R_c} \end{bmatrix}$$

$$C = \begin{bmatrix} \frac{D'}{2} & -\frac{D}{2} & \frac{1}{2R_c} & -\frac{1}{2R_c} \end{bmatrix}, \qquad E = \begin{bmatrix} 0 & -\frac{1}{2R_c} \end{bmatrix} \tag{8.2}$$

owing to the dependence of i_s to all of the states, the steady-state value values for each state must be calculated by AX + BU = 0, and then

$I_s = CX + EU$ gives the final result:

$$I_s = \frac{V_g \frac{D - D'}{DD'} - V_s}{\frac{R_c}{2DD'} + R_\ell \left(\frac{1}{D^2} + \frac{1}{D'^2} \right)} \tag{8.3}$$

Equation (8.3) determines the output current to be difference of the ideal output voltage of the amplifier (no load) and the ac supply voltage divided by an equivalent resistor. As parasitic resistances R_ℓ and R_c are reduced, the current becomes more sensitive to small deviations in the two terms of the numerator of Eq. (8.3). The open-loop system will be indeterminate as parasitics vanish completely.

The same procedure, when applied to other converters results in the following expressions:

buck:
$$I_s = \frac{V_g(D - D') - V_s}{2R_\ell} \tag{8.4a}$$

boost:
$$I_s = \frac{V_g \frac{D - D'}{DD'} - V_s}{\frac{0.5R_c}{DD'} + R_\ell \left(\frac{1}{D^2} + \frac{1}{D'^2} \right)} \tag{8.4b}$$

buck-boost:
$$I_s = \frac{V_g \frac{D - D'}{DD'} - V_s}{\frac{0.5R_c}{DD'} + R_\ell \left(\frac{1}{D^2} + \frac{1}{D'^2} \right)} \tag{8.4c}$$

Ćuk:
$$I_s = \frac{V_g \frac{D - D'}{DD'} - V_s}{R_{\ell 1}\left(\frac{D^2}{D'^2} + \frac{D'^2}{D^2}\right) + 2R_{\ell 2}} \tag{8.4d}$$

where $R_{\ell 1}$ and $R_{\ell 2}$ in the Ćuk amplifier correspond to the parasitic resistances of the two inductors in each converter. Also, Eq. (8.4) shows that the direction of current may be reversed by a small change in one of the two numerator terms. Furthermore, in converters with pulsating output currents, the ESR of the input capacitor is included in the effective resistance.

So far, the dc solution for the output current versus various parameters of the amplifier has been found. In order to control this current to the desired form a feedback scheme must be employed. The complete form of the closed-loop solution is given by Eq. (3.34). However, in case of a single-loop feedback, this equation is greatly simplified. Then, the output current is influenced by two factors, namely the duty ratio and the ac voltage. Small-signal ac wise, this relation may be written by

$$\hat{i}_s = \hat{d}\, G_{id} - \frac{\hat{v}_s}{Z_0} \tag{8.5}$$

To be consistent with Chapter 7, the direction of i_s is selected as shown in Fig. 8.3. This is the reason for the negative sign in Eq. (8.5) and should not be misinterpreted as the negative resistance. The entity G_{id} denotes the duty ratio-to-output current transfer function $\hat{i}_s/\hat{d}$ and Z_0 is the open-loop output impedance, as seen by the V_s

(or $\hat{v}_s/\hat{i}_s$). In a single-loop system, the output current is compared to a reference current and the error signal is used to control the duty ratio. That is,

$$\hat{d} = (\hat{i}_{ref} - \hat{i}_s)\, H \tag{8.6}$$

where H(s) is the transfer function of the compensation network. Substitute Eq. (8.6) in (8.5):

$$\frac{i_s}{v_s} = \frac{\frac{\hat{i}_{ref}}{\hat{v}_s} G_{id}\, H - \frac{1}{Z_0}}{1 + G_{id}\, H} \tag{8.7}$$

The quantity $G_{id}\, H$ is the loop gain of the system. Furthermore, in a unity power factor system the reference current will be proportional to the output voltage such that $\hat{v}_s/\hat{i}_{ref} = -R$, where R is the desired output resistance of the closed loop system, such that:

$$\frac{i_s}{v_s} = -\frac{\frac{G_{id}\, H}{R} + \frac{1}{Z_0}}{1 + G_{id}\, H} \tag{8.8}$$

As $G_{id}\, H$ goes to infinity, the output impedance of the amplifier approaches the ideal R. Therefore, the quantity to be regulated must be emphasized by increase of its gain in the frequency range of interest to generate a correct error signal. In such a system, on the ac side,

no dc current is allowed; therefore, very high loop gains at dc are desirable. It will be shown later that the current gain of the amplifier in the charger mode is large and heavily dependent on parasitics. Being one of the components of the loop gain, it can be improved upon by an integrator in the compensation network. Here with the ideal infinite gain of the integrator at dc, the absence of dc current on the ac port is ensured. Furthermore, it increases the overall loop gain at line frequency where it provides a better control of the ac impedance. In a multiple-loop system, G_{id} and H will be vectors of gains.

The frequency response analysis of the system involves a few assumptions. As with the inverter case, the amplifier must have enough bandwidth to allow large-signal variations of the current. Also, it is considered that the frequency of the ac voltage source is low enough such that the circuit has enough time to follow it.

In general, the control transfer functions vary with steady-state values. Again, one performs the required transfer function calculations and the loop design at the quiescent operating point D = 0.5, and then checks the results against various operating conditions to ensure the stability. The dynamics of the system, owing to the removal of the load changes dramatically. At the quiescent operating point, the two converters of the amplifier again share the same overall conditions, however, in general, reduction of the analysis to that of a single converter is not quite as simple. As an example, the control-to-output current transfer function of the boost amplifier of Fig. 8.3 is analyzed:

$$P\dot{\hat{x}} = A\hat{x} + k\hat{d} \tag{8.9a}$$

$$\hat{y} = C\hat{x} + \left[(C_1 - C_2)\, X + (E_1 - E_2)U\right]\hat{d} \tag{8.9b}$$

where P and A matrices are found in Eq. (8.2) and with $D = D' = 0.5$ and $V_s = 0$ the steady-state X vector is found to be $[0,0,2,2]^T V_g$. Then

$$k = (A_{11} - A_{22})X + (B_{11} - B_{22})U = [2 \;\; -2 \;\; 0 \;\; 0]^T V_g \tag{8.10}$$

and the last two terms of Eq. (8.9b) null out to reduce it to:

$$\frac{\hat{i}_s}{\hat{d}} = \frac{1}{4}\,\frac{\hat{i}_1}{\hat{d}} - \frac{1}{4}\,\frac{\hat{i}_2}{\hat{d}} + \frac{1}{2R_c}\,\frac{\hat{v}_1}{\hat{d}} - \frac{1}{2R_c}\,\frac{\hat{v}_2}{\hat{d}} \tag{8.11}$$

Therefore all the transfer functions of the system's states versus duty ratio must be calculated. Carrying all the calculation with the resolution of R_ℓ in Ls results in the final answer of:

$$\frac{\hat{i}_s}{\hat{d}} = \frac{4V_g}{R_c}\;\frac{1 + R_c C s}{1 + \left(R_c C + 4\,\frac{L}{R_c}\right) s + 4LCs^2} \tag{8.12}$$

in which the common factor of $(1 + R_c C s + 4LCs^2)$ in numerator and denominator cancel out. Equation (8.12) simplifies even further to

$$\frac{\hat{i}_s}{\hat{d}} = \frac{4V_g}{R_c} \frac{1}{1 + 4\frac{L}{R_c}s} \tag{8.13}$$

Substitute $R_\ell + Ls$ for Ls in Eq. (8.13) to get the final answer:

$$\frac{\hat{i}_s}{\hat{d}} = \frac{V_g}{R} \frac{1}{1 + \frac{L}{R}s} \quad \text{and} \quad R = R_\ell + \frac{1}{4}R_c \tag{8.14}$$

Equation (8.14) shows a few important points. First, the output current has a simple one-pole response versus the duty ratio. Such response allows very high loop gains and thus good regulations. Second, the corner frequency is determined by the parasitics. Without the resistive parasitics, a pole at zero frequency exhibits an indeterminant system, as previously verified by other methods. Third, exact cancellation of poles and zeros at the quiescent operating point, signals the interaction of the two converters of the amplifier whose conditions are exactly the same (as discussed in Chapter 7). However, if the same analysis is done on a single converter, the results are not the same, even if correct steady-state conditions are imposed upon the converter (it results in $R = R_\ell$ in Eq. (8.14)). So, one must be careful to avoid probable inaccuracies by the short cut to analysis of a single converter. Nevertheless, the discrepancy which is generated by interaction of the pulsating output current and the ESR of the capacitor, is minimal and practically is ignored in the feedback loop design procedure. The same

difference can be verified to exist in the inverter mode too, but, since the parasitics are much smaller than the load, they were ignored.

At duty ratios other than 0.5, and at different current levels, the poles and zeros move to different locations and the pole-zero cancellation does not occur. These poles and zeros are of high Q type whose movement away from each other generates a glitch in the response. Feedback design must consider the undesirable possibility of placement of zeros in the right half-plane. One may analyze these movements and properly modify the parasitics to ensure confinement of the zeros to the left half-plane for various operating conditions. A single or multiple loop feedback may then be placed around the system.

Again, the buck amplifier is exempt from the above discussion, since its single-pole duty ratio-to-output current transfer function does not depend on operating conditions. A more difficult case is considered next in the experimental verification of a coupled-inductor Ćuk amplifier.

8.3 Experimental Verification — Ćuk Battery Charger

The same amplifier of Section 7.3 is treated as a battery charger. Figure 8.4 illustrates the power stage. The dc analysis was done on the Ćuk amplifier and the results of Eq. (8.4d) are still valid. The inverter mode was analyzed for the maximum load of 25 Ω. For the battery charger, the currents are also selected to simulate a maximum of 25 ohm load on the line (to take advantage of the current capability of the hardware). However, this resistance is variable and will be

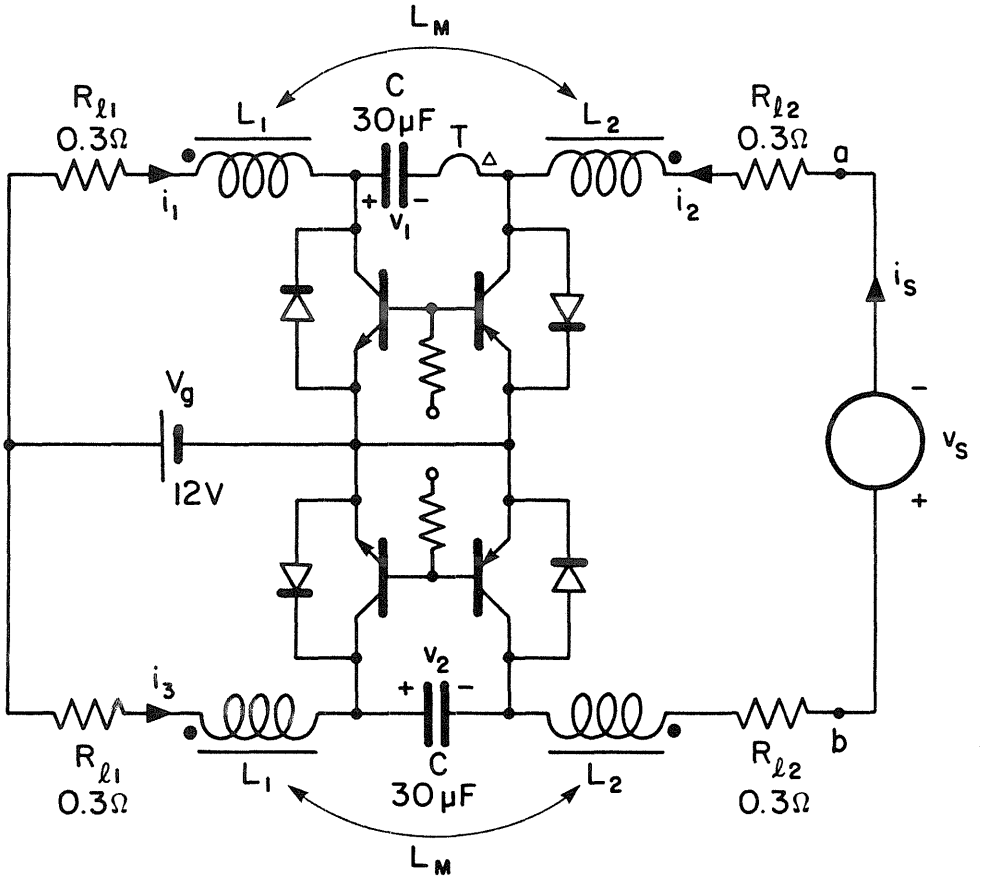


Fig. 8.4 Experimental Ćuk battery charger. The current transformer T is used to sense i_1 and i_2.

switched to a high value when the voltage on the battery has reached a preset value.

The generalized state-space averaging step results in:

$$P\dot{x} = Ax + Bu \tag{8.15}$$

where $x = [i_1, i_2, i_3, v_1, v_2]^T$ and $u = [v_g, v_s]^T$ and

$$P = \begin{bmatrix} L_1 & L_M & 0 & 0 & 0 \\ 0 & -L_M & L_1 & 0 & 0 \\ L_M & 2L_2 & -L_M & 0 & 0 \\ 0 & 0 & 0 & C & 0 \\ 0 & 0 & 0 & 0 & C \end{bmatrix} \tag{8.16}$$

$$A = \begin{bmatrix} -R_{\ell 1} & 0 & 0 & -d' & 0 \\ 0 & 0 & -R_{\ell 1} & 0 & -d \\ 0 & -2R_{\ell 2} & 0 & d & -d' \\ d' & -d & 0 & 0 & 0 \\ 0 & d' & d & 0 & 0 \end{bmatrix} \quad \text{and} \quad B = \begin{bmatrix} 1 & 0 \\ 1 & 0 \\ 0 & -1 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}$$

Then

$$G(s) = C(sP - A)^{-1}k \tag{8.17}$$

where

$$C = [0, 1, 0, 0, 0] \quad \text{and} \quad k = [2, -2, 4, 0, 0]^T V_g.$$

The final result is found to be

$$\frac{\hat{i}_2}{\hat{d}} = 4 \frac{V_g}{R_{\ell 2}} \frac{1 + 2C(L_1 - L_M)s^2}{1 + \frac{L_1 + 2L_M + L_2}{R_{\ell 2}} s + 4L_1 Cs^2 + \frac{4C\left(L_1 L_2 - L_M^2\right)}{R_{\ell 2}} s^3} \tag{8.18}$$

where common factor of $(1 + 4L_1Cs^2)$ has exactly cancelled out in numerator and denominator and reduced the original fifth order system to a third order one. Now resubstitute $R_{\ell 1} + sL_1$ and $L_1 = L_M$ for the zero ripple conditions in Eq. (8.18). Define $L_2 \equiv L_M + L_e$ and

$$\frac{\hat{i}_2}{\hat{d}}(s) = \frac{4V_g}{R_{\ell 1} + R_{\ell 2}} \frac{1 + 2R_{\ell 1}Cs}{\Delta}$$

$$\Delta = 1 + \left(\frac{4L_M + L_e}{R_{\ell 1}+R_{\ell 2}} + 4\left(R_{\ell 1} \,||\, R_{\ell 2}\right)C\right)s + 4C\left(L_M + \frac{R_{\ell 1}}{R_{\ell 1}+R_{\ell 2}} L_e\right)s^2 + 4C\, L_M \frac{L_e}{R_{\ell 1}+R_{\ell 2}} s^3$$

(8.19)

With the actual numerical values, one may approximately factorize the denominator as

$$\frac{\hat{i}_2}{\hat{d}(s)} \cong \frac{4V_g}{R_{\ell 1} + R_{\ell 2}} \frac{1 + 2R_{\ell 1}Cs}{\left(1 + \frac{4L_M}{R_{\ell 1} + R_{\ell 2}} s\right)\left[1 + C\left(R_{\ell 1} + R_{\ell 2}\right)s + L_e Cs^2\right]}$$

(8.20)

provided that $4L_M >> L_e$. Equation (8.20) shows a single pole at low frequencies approaching zero Hertz as the resistive parasitics vanish. Also, there is a high frequency pole pair due to interaction of the capacitors and the leakage inductance. The Q of this resonance depends on the parasitics which can cause problems for the feedback. The zero of the transfer function is also at high frequency. This leaves the transfer function with a single pole at low frequencies. The thick lines of Fig. 8.5 demonstrate the result of the calculations performed on SCAP, while thin lines correspond to the measurement of the actual hardware taken by AMS. The phase discrepancy is partly due to the

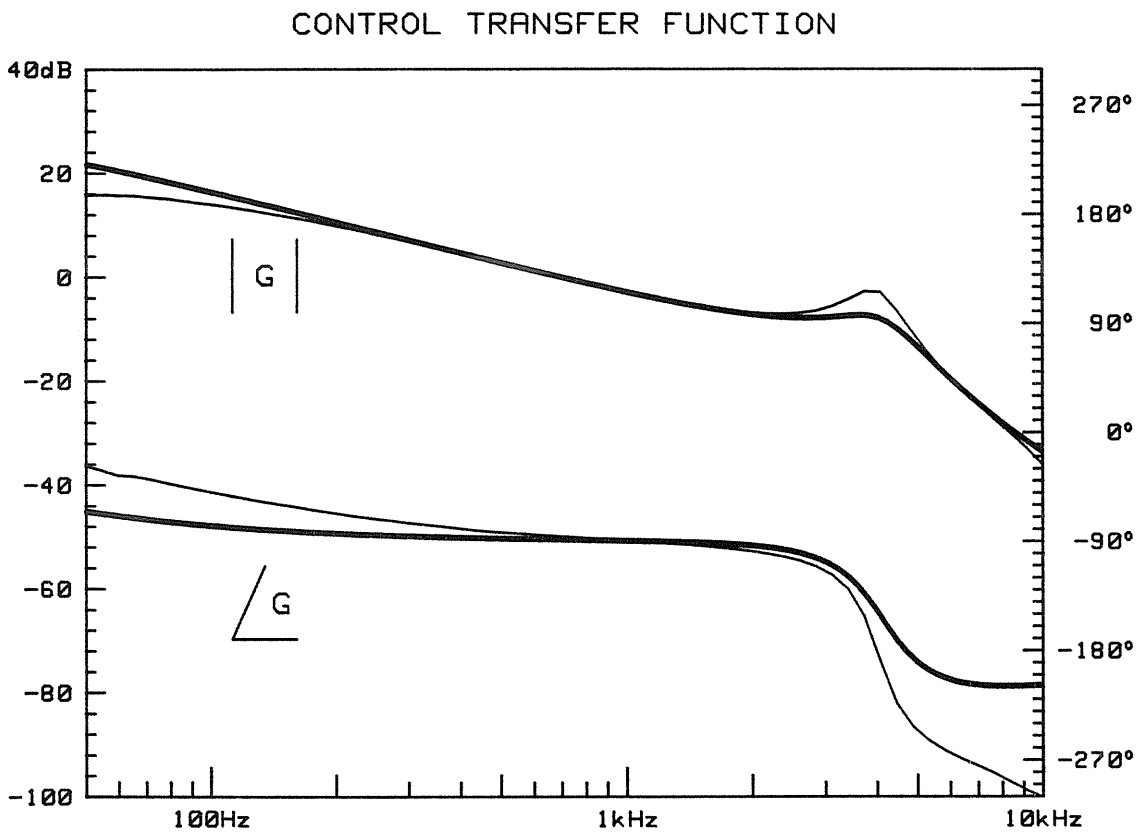


Fig. 8.5 *Control-to-output current transfer function of the Ćuk battery charger. Thick and thin lines correspond to predicted and measured results.*

sensing technique where a sample and hold circuit was used. The reason for this choice will be discussed later.

Unlike the buck, boost, or the buck-boost stages, this response alone cannot constitute a feedback loop with very high loop gains since the other poles will degrade the phase with an eventual instability with further increase of the gain. However, the multiple-loop feedback option is still available. A prime candidate to correct the loop gain is the input current i_1. Similar to the i_2 calculations, the $\hat{i}_1/\hat{d}$ transfer function is found in Eq. (8.17) except with C = [1, 0, 0, 0, 0]. After simplifications described earlier, the final transfer function is found to be

$$\frac{\hat{i}_1(s)}{\hat{d}(s)} \cong \frac{4V_g}{R_{\ell 1} + R_{\ell 2}} \frac{1 + 2R_{\ell 2}Cs + 2CL_e s^2}{\left(1 + \frac{4L_M}{R_{\ell 1} + R_{\ell 2}} s\right)\left[1 + C\left(R_{\ell 1} + R_{\ell 2}\right)s + L_e Cs^2\right]} \tag{8.21}$$

where in Eq. (8.21) the denominator is approximated from the form in Eq. (8.19) to this factorized form. One simple check shows that

$$\frac{\hat{i}_1}{\hat{d}} + \frac{\hat{i}_2}{\hat{d}} \cong \frac{4V_g}{R_{\ell 1} + R_{\ell 2}} \frac{1 + 2R_{\ell 1}Cs + 1 + 2R_{\ell 2}Cs + 2L_e Cs^2}{\left(1 + \frac{4M}{R_{\ell 1}+R_{\ell 2}} s\right)\left[1 + C\left(R_{\ell 1}+R_{\ell 2}\right)s + L_e Cs^2\right]} =$$

$$= \frac{8V_g}{R_{\ell 1} + R_{\ell 2}} \frac{1}{1 + \frac{4M}{R_{\ell 1} + R_{\ell 2}} s} \tag{8.22}$$

The sum of two currents exhibits an approximate single-pole response ideal for high loop-gain systems. Exact calculation of the sum of the transfer function gives the following results:

Exact				Approximate	
poles		zeros		poles	zero
23.6 Hz	real			23.9 Hz	real
4.13 kHz	Q = 2.14	4.11 kHz	Q = 2.15		

Figure 8.6 shows the three transfer functions $\hat{i}_1/\hat{d}$, $\hat{i}_2/\hat{d}$, and $(\hat{i}_1 + \hat{i}_2)/\hat{d}$. However, as mentioned earlier, the sum of i_1 and i_2 transfer functions of Eq. (8.22) cannot directly be used to close a feedback loop, since $i_1 + i_2$ will be the regulated quantity instead of i_2. The quantity i_2 must then be highlighted such that at the line frequency, only the output current i_2 is compared with the reference. At higher frequencies, i_1 may be added to remove the pole pair as suggested by Eq. (8.22). Figure 8.7 shows the control circuitry for the battery charger. Current sensing is performed by a current transformer T on the capacitor, in Fig. 8.4. In this figure, when the upper npn transistor is ON, the capacitor carries i_2. In the rest of the cycle the current will be $-i_1$. Therefore, two sample and hold circuits activated at the correct times can select either of the two waveforms from the capacitor current waveform. This is a simple way of sensing i_2 *and* i_1, however, it introduces some additional phase shift due to the sampling

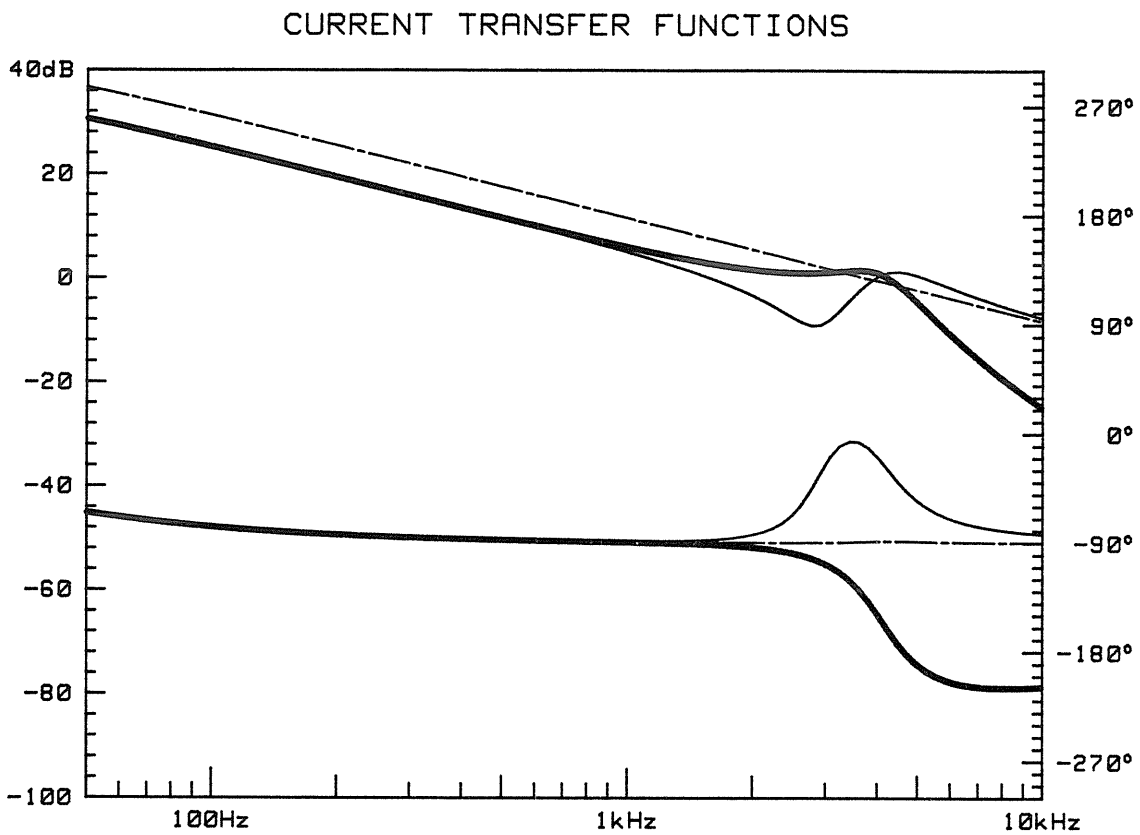


Fig. 8.6 *Current transfer functions of the Ćuk battery charger. Thick lines are for* $\hat{i}_2/\hat{d}$, *thin lines are for* $\hat{i}_1/\hat{d}$, *and dash-dot lines are for* $(\hat{i}_1 + \hat{i}_2)/\hat{d}$.

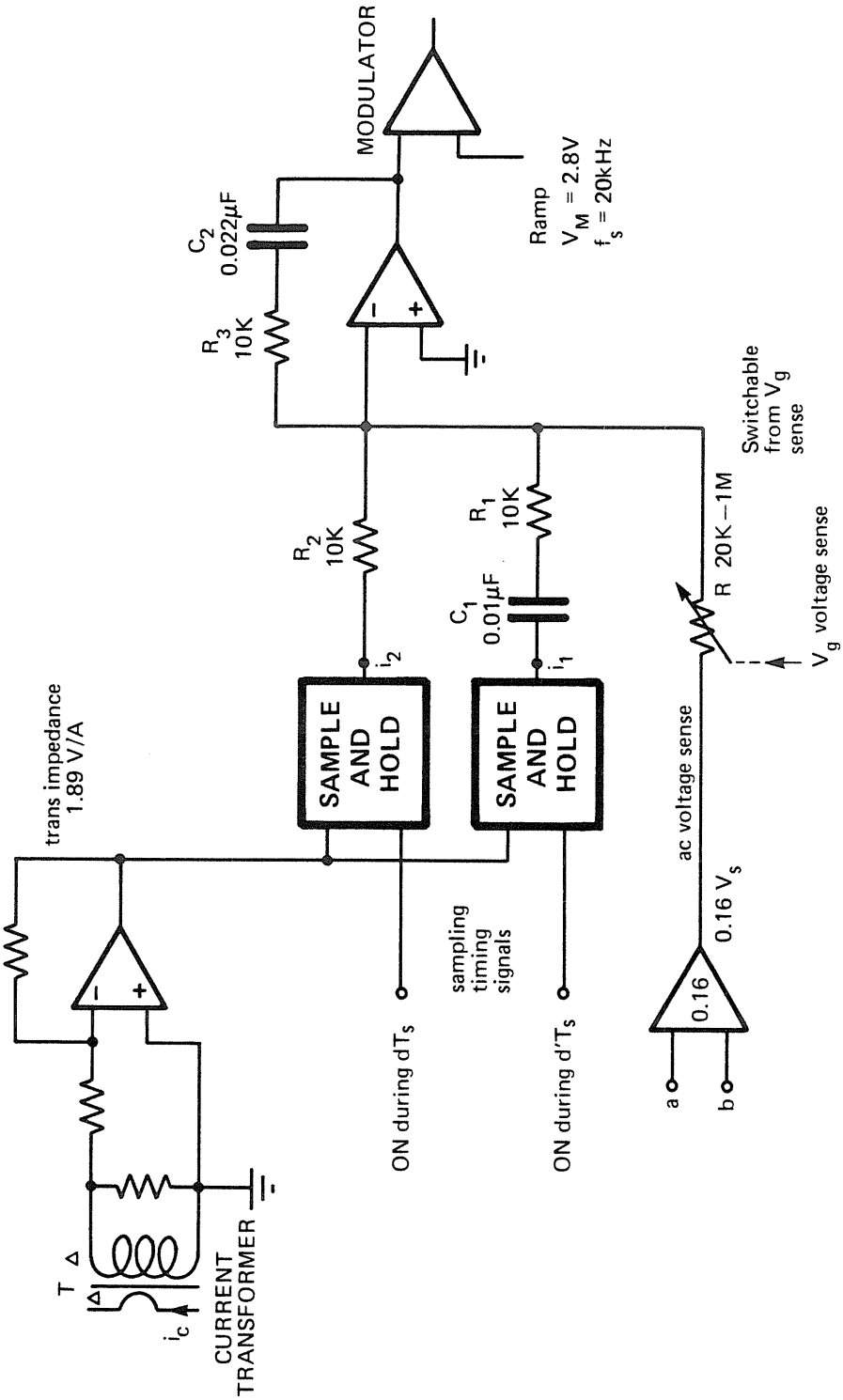


Fig. 8.7 Control circuit of the Ćuk battery charger.

effect (Section 3.4).

Capacitor C_1 along with R_1 removes i_1 signal at low frequencies, and C_2 is the integrator capacitor to improve the loop gain and remove any dc from i_2. The variable resistor R determines the amplitude of the current. For example, with the numerical values shown, and for the output impedance of 25 Ω, the R must be

$$\frac{0.16\ V_s}{R} = \frac{1.89\ i_2}{R_2} \quad \text{or} \quad R = 21.2\ \text{k}\Omega \quad (847\ \text{ohms/ohm})$$

Figure 8.8 compares the prediction of the loop gain (thick lines) with those taken experimentally (thin lines). Notice the glitch in the response, since the high pass filter on i_1 sense produces a phase shift which prevents a complete cancellation of the pole and zero pair as in Eq. (8.22).

The most important aspect of the battery charger, namely its ac port admittance, can also be analyzed. From equations, one can analytically obtain the open-loop ac port admittance of the charger:

$$-\frac{\hat{i}_2}{\hat{v}_s} \cong \frac{1}{2(R_{\ell 1} + R_{\ell 2})} \frac{1 + 4R_{\ell 1}Cs + 4L_M Cs^2}{\left(1 + \dfrac{4L_M}{R_{\ell 1} + R_{\ell 2}}\, s\right)\left[1 + (R_{\ell 1} + R_{\ell 2})Cs + L_e Cs^2\right]} \tag{8.23}$$

Figure 8.9a shows a Bode plot of Eq. (8.23). A very low and uncontrollable admittance (open-loop) will cause high currents while

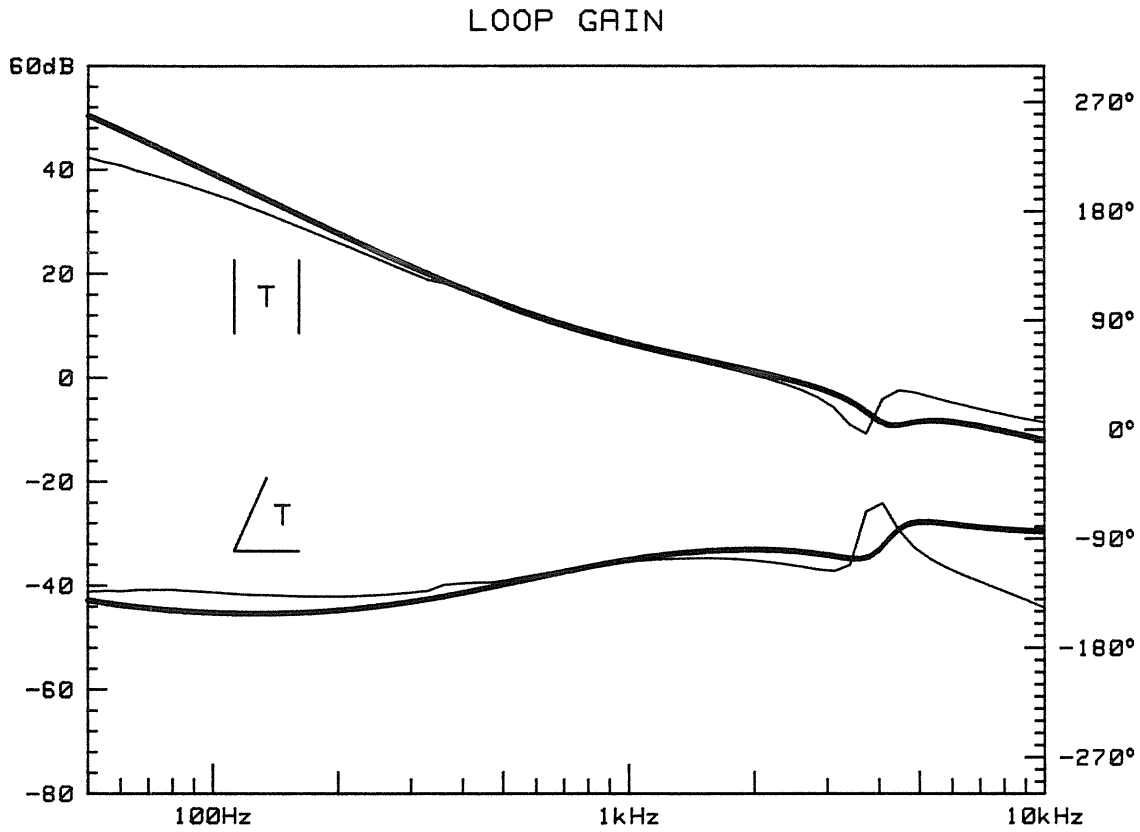


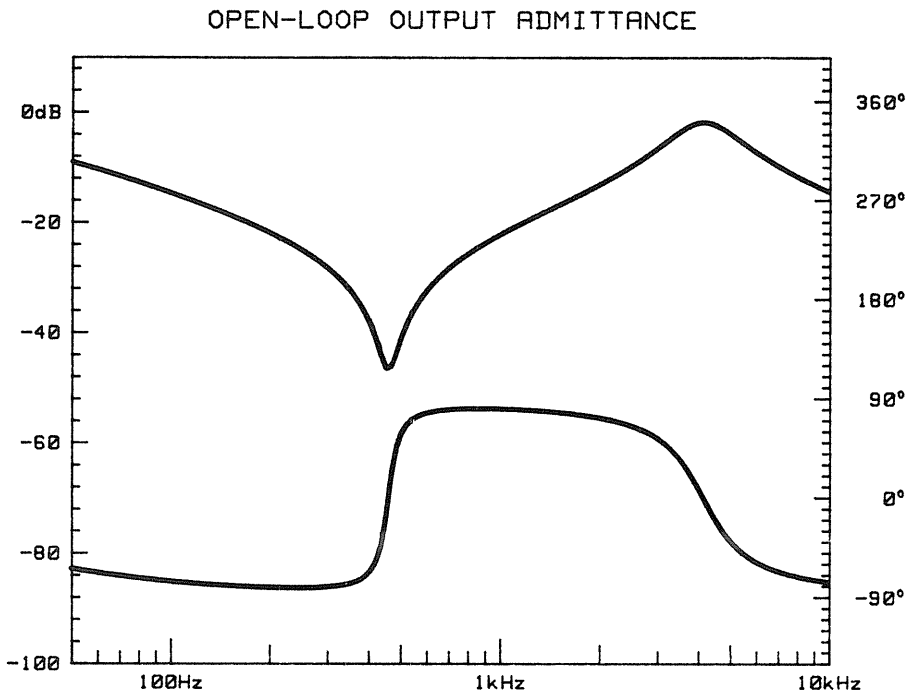
Fig. 8.8 Predicted and measured loop gain of the battery charger. (Thick and thin lines respectively).

Fig. 8.9b is the closed-loop output admittance (prediction and measurement) for the 25 ohm resistance case. The high degree of matching shows the accuracy of the calculations. At 60 Hz, the actual magnitude of the output impedance is 28.06 dB(0dB = 1Ω) = 25.3 Ω with 1.5^0 phase shift. So, the output impedance is satisfactory at the frequency of the line (up to nearly 400 Hz). Figures 8.10a and 8.10b show families of calculated closed-loop output admittance for differed levels of power transfer. While in the first one power flows from ac to dc, the second figure is for dc to ac cases.

To complete the design, one must check the movement of the poles and zeros of the loop gain to ensure stability at various operating conditions. The design was done around D = 0.5, where the unity power factor requirement dictates zero current (zero voltage). This design allows for maximum duty ratios of 0.6 (0.4). At maximum duty ratio (and the peak ac voltage), the current will be at its maximum too. However, its value depends on the selected output impedance. For maximum resistance, the current will still be zero, while for minimum resistance, the current will reach to its maximum. Table 8.1 shows the poles and zeros of loop gain at different conditions.

With the conditions in Table 8.1, all the zeros stay in the left half-plane. The calculated phase margins are also included. The last column in Table 8.1 is for the case of negative input admittance or when the power is flowing from the battery to the line. This is easily realized by a simple change of sign in the ac voltage sense in Fig. 8.7. Therefore, the design is completely stable at all the possible operating

a)



b)

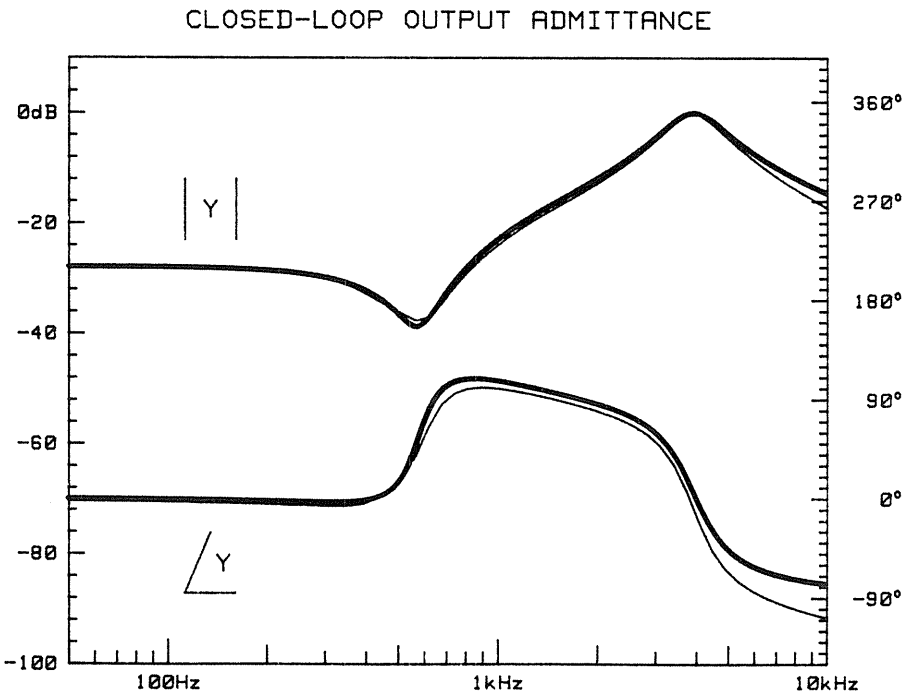
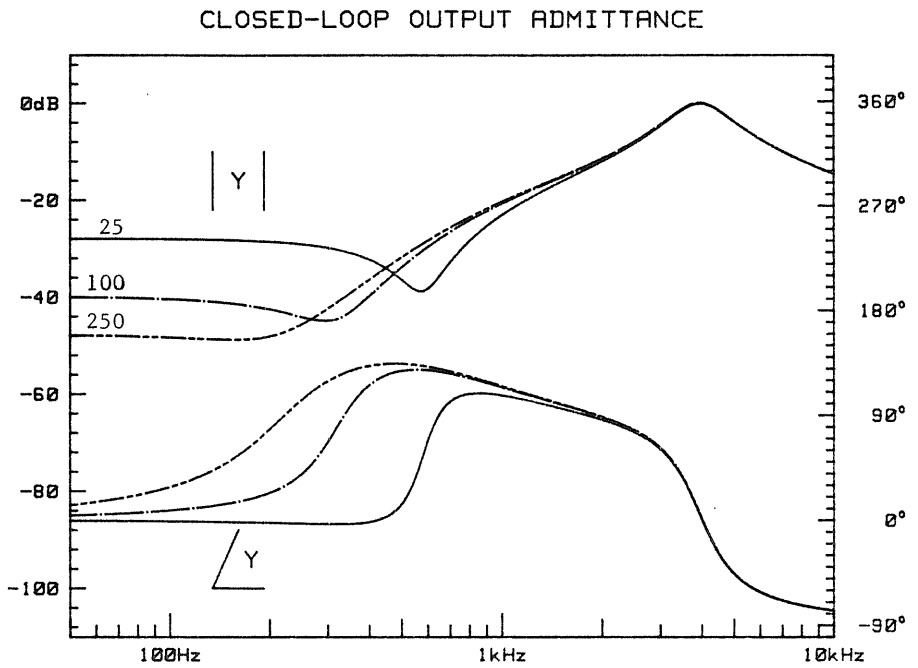


Fig. 8.9 *Output admittance, (a) theoretical, open-loop; (b) theoretical (thick lines) and measurement (thin lines) results for closed-loop admittance of* 25Ω *nominal. Zero dB corresponds to* 1Ω (1 mho).

a)



b)

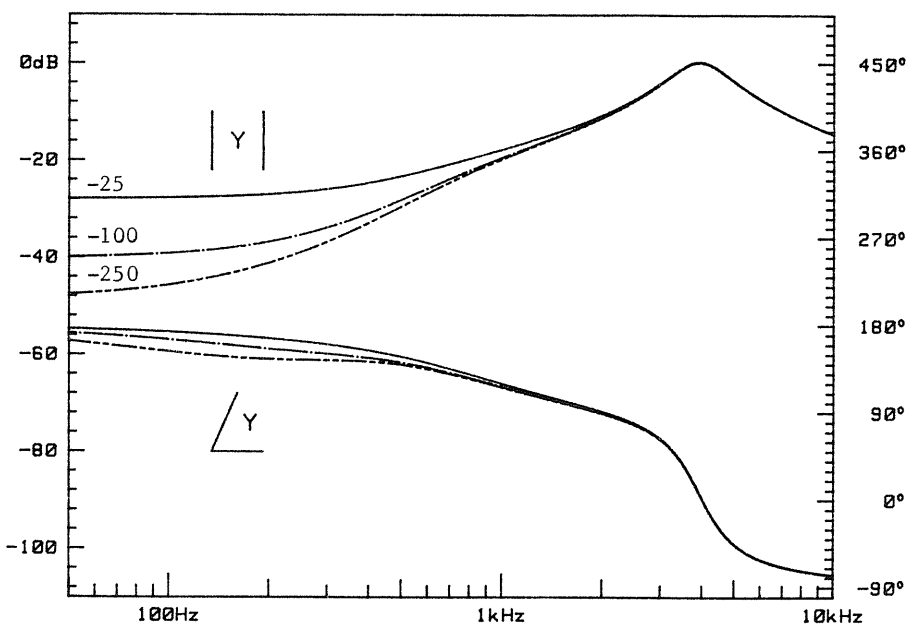


Fig. 8.10 *Families of output admittance transfer functions. (a) Battery charger: Cases of 25Ω, 100Ω, and 250Ω, (b) battery discharger: Cases of -25Ω, -100Ω, and -250Ω. Zero dB corresponds to 1Ω (1 mho).*

D = 0.5	D = 0.6		
$v_s = 0$ $i_2 = 0$	$v_s = 10$ $i_2 = 0$	$v_s = 10.597$ $i_2 = 0.424$	$v_s = 9.467$ $i_2 = -0.379$
poles	poles	poles	poles
4.13 kHz Q = 2.14	4.13 kHz Q = 2.14		
1.59 kHz real	1.59 kHz real		
459 Hz Q = 9.62	468 kHz Q = 9.80	→ same	→ same
23.5 Hz real	24.5 Hz real		
7.23 Hz real	7.23 Hz real		
zeros	zeros	zeros	zeros
4.18 kHz Q = 3.66	4.17 kHz Q = 3.22	4.28 kHz Q = 3.25	4.07 kHz Q = 3.21
459 Hz Q = 9.62	469 Hz Q = 10.02	495 Hz Q = 11.6	446 Hz Q = 10.34
766 Hz real	614 Hz real	523 Hz real	714 Hz real
730 Hz real	730 Hz real	730 Hz real	730 Hz real
Phase Margin: 86°	Phase Margin: 96°	Phase Margin: 97°	Phase Margin: 96°
Any R_{out}	$R_{out} = \infty$	$R_{out} = 25\ \Omega$	$R_{out} = -25\ \Omega$

Table 8.1

conditions (even in the reverse flow mode!) and the feedback design is complete.

One notices that a system with the correct initial condition stays stable and an incorrect initial condition may cause unwanted movement of zeros to the right half-plane. However, since this mode is exactly controllable (its occurrence is determined by the system), the correct set of initial conditions can be used for assured stability. Figure 8.11 shows the actual ac voltage (V_s) and the current drawn by the closed-loop battery charger (i_2).

8.4 Review

The idea of battery charging by use of a switched mode power amplifier was introduced. Instead of load, ac lines are connected to the ac port of the amplifier (now input). A feedback system controls the ac current, otherwise, the voltage source-like ac port of the amplifier and the line will be paralleled causing very large currents. Since the currents are controllable, it can make the amplifier a superior performance load on the line, as opposed to the ordinary rectifiers with uncontrollable currents. The control is exercised to make the current proportional to the ac voltage. Now the amplifier functions as a unity power factor battery charger. The amount of power transferred during one complete cycle depends on current. Also, the current may be deliberately phase-shifted with respect to the voltage to make the charger appear inductive or capacitive.

To control the system, essentially the same approximations as in

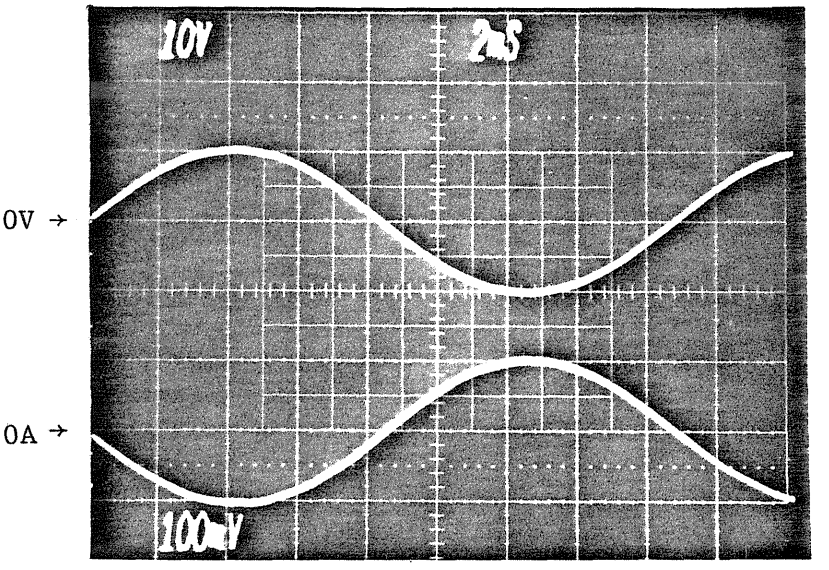


Fig. 8.11 *Oscillogram of the ac voltage and current of the battery charger* (R_{out} = 25Ω).

the case of the inverter are made. For example, the system must have bandwidth much larger than the operating (line) frequency. Open-loop steady-state currents of the system are totally determined by the resistive parasitics such that an ideal lossless amplifier is indeterminate. Dynamics of the amplifier, owing to the effective short circuit (line) on the output, experience a large change with a dominant pole at low frequencies. This pole whose position is determined by the parasitics will move to zero frequency in a lossless amplifier.

Feedback design is performed around the quiescent operating point and then is checked for various duty ratio and current excursions. At the quiescent operating point, buck, boost, and buck-boost amplifiers exhibit only a single-pole response while the Ćuk amplifier, owing to the additional reactive components, will have more complex dynamics. As could be expected, larger loop gains are necessary to convert the undesirable open-loop output impedance of the amplifier to an adjustable, resistive one. No dc current on the line is allowed, so a very high loop gain at dc is mandatory. After the design is finished, the stability must be checked at various operating points, since the open-loop poles and zeros are duty ratio and current dependent. Calculation of the closed-loop output impedance of the battery charger and verification of the result with the desired specifications, and also with the practical setup, finalizes the design. The experimental battery charger was verified on the coupled-inductor Ćuk amplifier for which a double-loop feedback was designed and tested. The next chapter analyzes the switching process between the modes and the total UPS.

CHAPTER 9

THE COMPLETE UPS SYSTEM

Use of a switched-mode power amplifier as an inverter and a unity-power factor battery charger was analyzed in the last two chapters. A conventional UPS as shown on Fig. 5.1 can now be realized by use of two switching amplifiers, one as a battery charger and the other as the inverter. This would be useful in cases where the input and output voltages and frequencies are not the same with some obvious advantages. The alternative UPS of Fig. 5.2 utilizes the amplifier in both modes, however, some precautions are required for an orderly transition from one mode of operation to another.

So far the power amplifier and the control circuitries of the two modes have been examined separately. The analysis will be completed when the transitions are considered and the necessary refinements are performed. When both modes of operation are utilized on a single amplifier, one may merge the two control circuits and produce a single control unit which changes its response to the desired forms by a set of switches, or keep two separate control circuits. Figure 9.1 demonstrates the complete single-unit ac UPS in a more expanded form. Here, the two control circuits are kept separate and the switches are used to connect output of the proper control circuit to the modulator. For example, the switches of Fig. 9.1 are shown for the inverter mode.

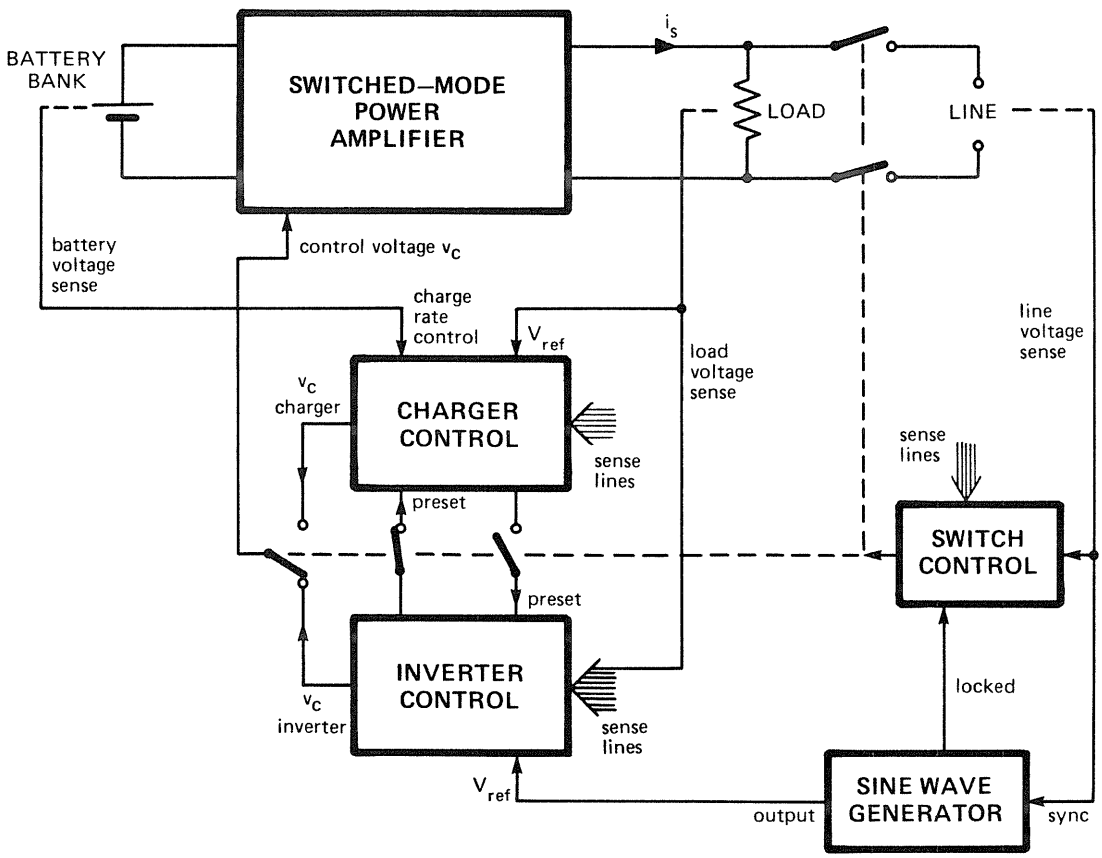


Fig. 9.1 *The complete single-unit uninterruptible power supply. Switches are set for inverter mode.*

For the battery charger mode, the state of each switch is inverted by the switch control circuit.

The requirements for smooth transition calls for communication between the control circuitries as illustrated in Fig. 9.1 as well as some possible modifications in the control circuits to meet the design specifications.

9.1 Transition from Inverter Mode to the Battery Charger Mode

This transition is controllable and can be carefully planned for. As long as the power is down, the switches are in the states shown in Fig. 9.1 (inverter). The amplifier is controlled by the inverter control circuitry and has a stable operation. The reference sine wave is supplied by a high quality sine wave generator. The amplified sine wave appears around the load, drawing power from the batteries.

When the line power is restored, an immediate reversal of switch states is not a good solution, since the sine wave developed around the load, and that of the line, may differ in phase (or slightly in frequency). Therefore, the sine wave generator of the system must be very slowly phase (and amplitude) locked to the line such that the two voltages are the same in phase and amplitude to minimize the transient. Still, the transition can be difficult if the correct state conditions are not met. As an inverter, at any time, the output power is non-negative, that is, the output voltage and current are in phase. On the other hand, the battery charger always has zero or negative output power, so, the output voltage and current are 180^0 out of phase. Since the

output voltage is predetermined, switching from the inverter mode to the battery charger mode means reversal of the direction of current in the amplifier. Notice that the state voltages of the amplifier are almost at the correct levels (differ only in parasitic resistive levels).

The reversal of current in the amplifier, however, need not be immediate and a gradual change of sign of the reference voltage in the charger mode may be used to solve the problem. Instead, a much simpler approach would be to switch the modes at the voltage cross over time. Since the output voltage and current are proportional, the current is at zero too. The amplifier now has the correct initial conditions for the charger mode and, the switching process will happen smoothly since no resistance is shown by the inductors of the circuit to the immediate reversal of the currents (zero current reversal!). This process is shown in Fig. 9.2.

The preceding argument considers only the amplifier; however, the feedback circuit also has dynamics and those states must also have the correct initial conditions. As long as the system is in the inverter mode, the inverter control circuit is active and its states have the correct values, but the control circuit for the charger has been deactivated by the switch action (even though it still senses all the required states). This circuit, owing to the no dc requirements, contains an integrator. Since the output of the control circuit does not correct for the errors, the integrator, accumulating these errors, quickly takes off and owing to the practical limitation of the OP Amps of the circuit, saturates at one and the circuits' voltage limits.

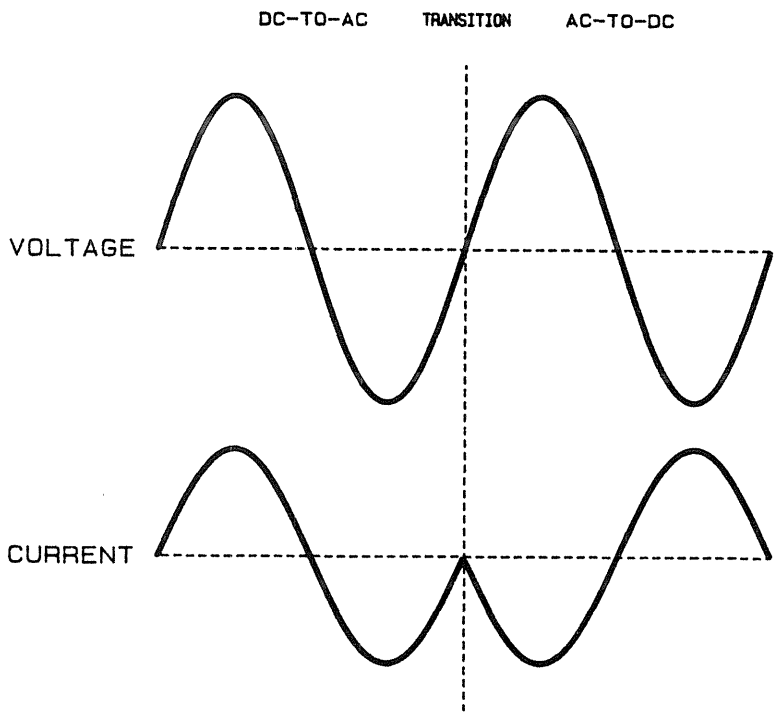


Fig. 9.2 Transition from the inverter mode to the charger mode.

At the time of switchover, even if the power stage is held at correct initial conditions, the integrator is at a wrong state. This imposes a wrong condition, and during the time it takes the system to return to correct conditions, large duty ratios and large currents will be generated.

The remedy for this case, of course, is to put correct initial voltage in the integrator of the charger control circuit. But, what is the correct voltage? To answer this question one must refer to equations describing the output current in each mode of operation. Define ideal voltage gain of the amplifier (no resistive parasitics) to be M(D). For example, for the boost converter $M(D) = (D - D')/DD'$. Also, define $\alpha(D)$ and $\beta(D)$ as representative of parasitic losses as follows:

in the inverter mode:

$$i_s = \frac{V_{out}}{R} = \frac{V_g\, M(D)}{R[1 + \alpha(D)]} = \frac{V_g\, M(D)}{R + \beta(D)} \tag{9.1}$$

in the charger mode:

$$i_s = \frac{V_g\, M(D) - V_s}{\beta(D)} \tag{9.2}$$

Equation 9.1 can be rewritten as

$$i_s = \frac{V_g\, M(D) - V_{out}}{\beta(D)} \tag{9.3}$$

Since at the time of switching the output voltages must be equal ($V_s = V_{out}$), then as expected, by keeping the same duty ratio, the current will continue unchanged. A reversal of current requires a minute change of D in Eq. (9.2), because $\beta(D)$ is a parasitic quantity and very small, while both the numerator quantities are large. Nonetheless, at the duty ratio of 0.5 (zero output voltage), when the switching occurs, both currents are equal to zero and no change of duty ratio is required.

Therefore, in order for the charger circuit to have correct voltages, an auxiliary circuit is required to keep the charger controller at such a level to produce the same ratio as the inverter controller. This level can be fixed at the value corresponding to D = 0.5, however, forcing the charger controller to follow the inverter is simpler and more accurate. For example, the circuit used in the experimental Ćuk battery charger of Fig. 8.7 is modified to that of Fig. 9.3 to hold the deactivated integrator of the charger at the correct level. The second amplifier, through a feedback circuit, injects enough voltage in the integrator capacitor C_2 to make the control voltage of the charger equal to that of the active inverter controller. Thus at D = 0.5, where the switchover command is given, the charger will have the exact initial condition leading to a completely smooth transition.

9.2 Transition from the Charger Mode to the Inverter Mode

Unlike the transition from inverter to charger mode, this transition is not controllable, since the power line failure can happen randomly.

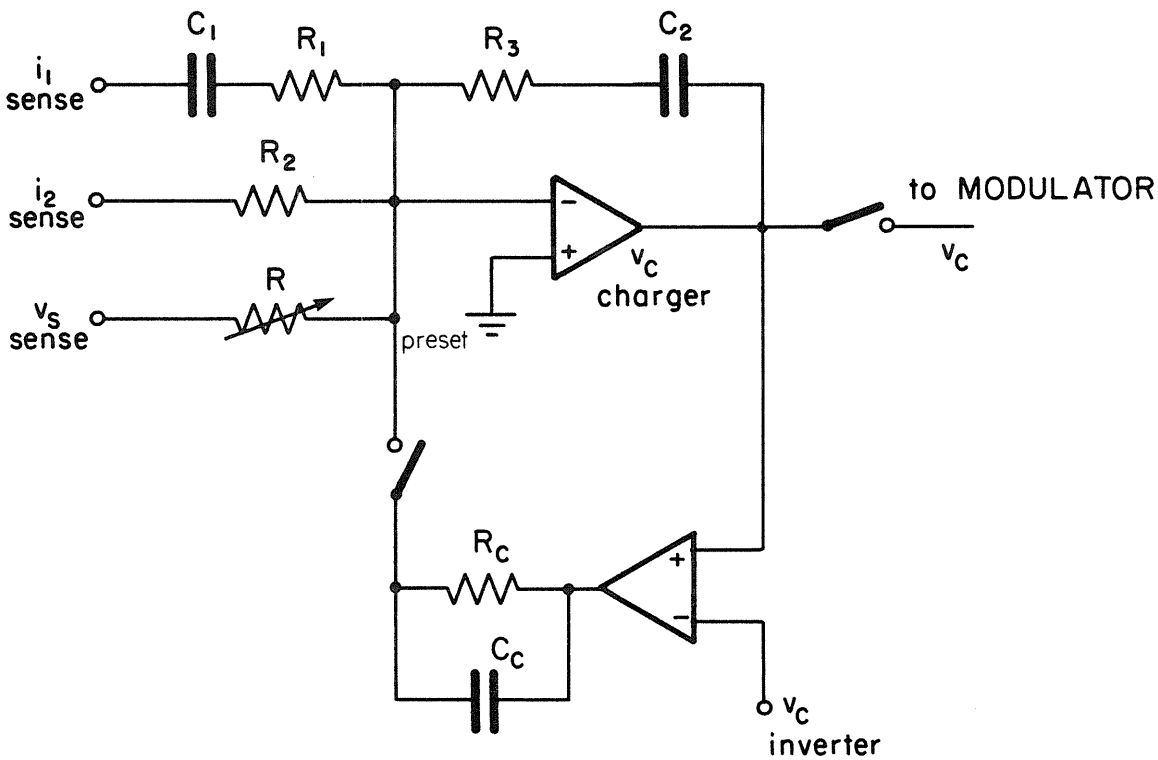


Fig. 9.3 Active circuit to preset the correct voltage in the integrator capacitor of charger controller. (States of the switches are the same as those of Fig. 9.1).

During the charger mode, the sine wave generator is phase-locked to the line such that the output voltage produced by the combination of the generator and the amplifier is exactly in phase with the line. This ensures proper continuation of the output voltage in case of a failure. Again, the output power of the charger is always non-positive. At the instant of line failure, the switches are immediately ordered open by the switch control circuit. Also, the inverter control is activated. The task of the inverter is to provide continuation of the line cycle with "positive power", even though most loads can tolerate a missing cycle.

If the switching occurs when the line had a non-zero voltage, to furnish the load with continuous power means the output power and, therefore, the output current of the amplifier must reverse direction immediately. However, the dynamics of the amplifier prohibit instantaneous changes of current. Therefore, during the period for the current to change from one level inward to another level outward, the load will not have proper current, and the voltage will have a "dip". The following conditions lead to the worst case: consider a power line failure has already happened. The system is in the inverter mode to supply the load with ac power (drawn from the battery). When the power is restored, with a proper sequence (Section 9.1), the system is switched to the battery charger mode. The batteries are drained, so the control circuit uses maximum current level to recharge the batteries as soon as possible. The worst case is, while in the heavy charger mode, at the peak of the current (voltage), the power fails again. The current must

reverse its direction from maximum level in one direction to the peak level of the other direction. Figure 9.4a illustrates this condition. On the other hand, an easy case is when the failure occurs at zero voltage as shown in Fig. 9.4b. Here, the amplifier draws no current; also the inverter need not supply current. This, as was the case with the inverter to charger mode, implies a perfect initial condition match and a smooth transition is possible.

Again, the correct initial condition must be provided for the amplifier states, as well as the feedback network states. A good approximation for the correct integrator voltage is one which produces the same duty ratio as the charger does. Although this value is not 100% accurate, it provides almost exact values around the D = 0.5 duty ratio where the transition is smooth. Figure 9.5 shows the circuit employed to modify Fig. 7.10 of the practical inverter control circuit to preset the initial condition in the integrator capacitor C_2.

At other duty ratios, the current must change sign while the voltages remain almost the same. The inductors of the circuit prevent an instantaneous reversal of current and thus the output voltage starts to drop. The control circuit increases the duty ratio to avoid this drop. However, an increase in voltage will not happen before this current transition has finished. Thus, the duty ratio will further increase and it may hit one of its limits. The circuit behaves as an open-loop circuit until the voltage comes close to its correct value, and the control circuit again takes over. In order to make the transition smoother, the following conditions must be considered:

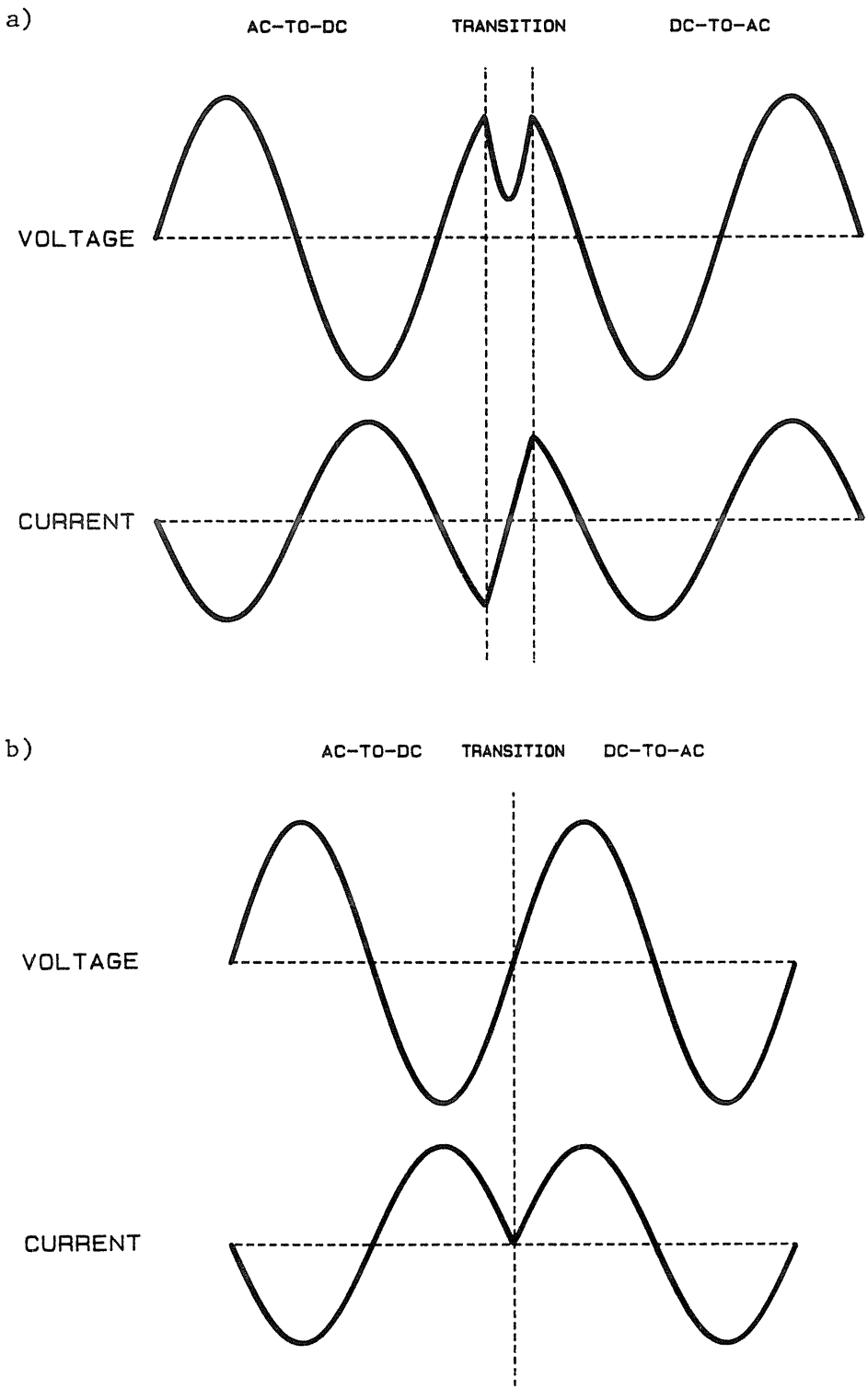


Fig. 9.4 *Transition from charger to inverter mode. (a) Worst case, (b) an easy case!*

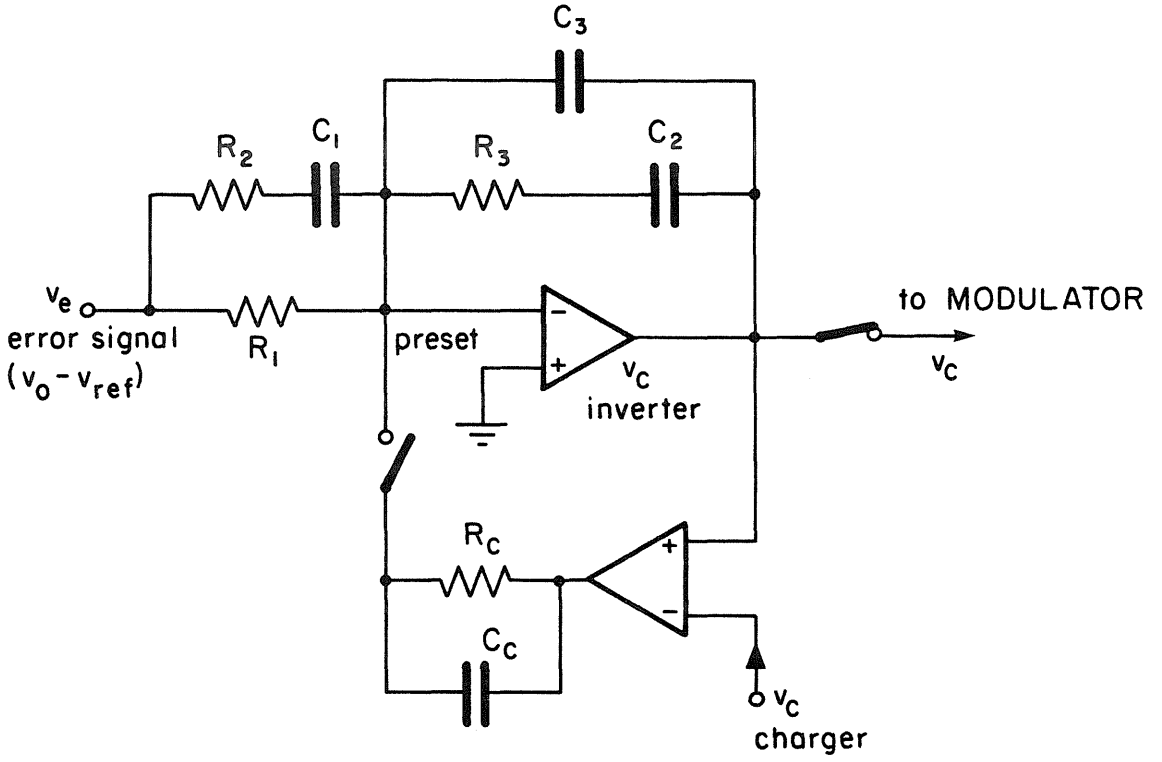
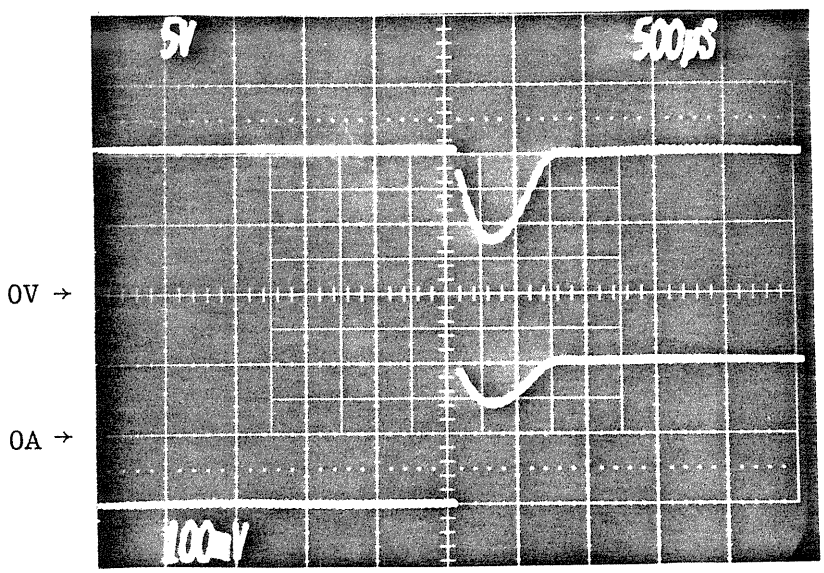


Fig. 9.5 *Voltage preset circuit for the inverter control circuit. (States of the switches are the same as those of Fig. 9.1).*

The duty ratio limits must be controlled to avoid extra large voltage and or currents. Also, as long as the duty ratio is at its limits, the circuit behaves as open-loop. During this time, the control circuit cannot compensate for the errors, and they accumulate in the integrator (although with the correct initial condition). So, when the circuit returns to normal condition, the integrator is slightly off, causing a larger duration of voltage mismatch. To reduce this additional mismatch, one may add another circuit to temporarily disable the integrator. However, a simpler remedy was used in the actual case, that is a low corner frequency to deactivate the integrator ($1/R_3C_2$). Here, the integrator capacitor requires a long time to change considerably, before which, the circuit reaches the correct conditions. Figure 9.6 shows the actual transition of the Ćuk UPS from the charger mode to the inverter mode. The worst case transition is shown where the voltage is at the maximum level and peak current is drawn inward and after transition peak current is drawn outward. It shows a 0.7 msec completion time for the worst case transition ($D_{limit} = 0.65$).

9.3 Review

The complete UPS consists of a switched-mode power amplifier, two control circuits, one for each mode of operation, reference signals, and switches with the associated control. In order for transitions to be smooth, the final condition of states in one mode, must be equal to the initial condition of states in the other mode. It was shown that in the inverter to charger transition, this condition is met at the time of



0.4A/div.

Fig. 9.6 *Output voltage and current waveforms for the worst case transition from the inverter mode to the charger mode.*

output voltage (current) cross-over (with the help of an auxiliary circuit to provide correct initial condition in the compensation network). Therefore, this transition is controllable and by switching the modes at the cross-over time, smooth transition is obtained.

The instant of charger to inverter transition, on the other hand, is unpredictable. The failure can happen at non-zero current conditions. The initial condition criterion is not met and the transition (in this case) is not smooth and will be dictated by the dynamics of the circuit (even with the controller presetter). To control the worst case, i.e. the peak power inward to peak power outward transition, some precautions must be taken. The duty ratio is limited to a maximum to prevent large voltage changes and the integrator is controlled to reduce the effect of accumulated error during the duty ratio saturation.

There are other possibilities to improve the performance of the system. The most important one is the power bandwidth of the amplifier. If this power bandwidth is increased, the inherent speed of the system will also increase. This will not only decrease the size and weight of the amplifier but also permits faster transition between the modes, in addition to higher loop-gains and better closed-loop behavior of the overall system. However, increase in the bandwidth, usually corresponds to an increase in the switching frequency, and practical considerations soon prohibit very high switching frequencies and bandwidths.

CHAPTER 10

CONCLUSION

This part has considered another aspect of power processing, namely the ac. Two general approaches to the generation of ac power: waveform synthesis and pulse width modulation were compared. The synthesis method uses many voltage sources and many slow switches to approximate sine waves with a number of steps. The degree of complexity of the method is justified only for large systems. On the contrary, the PWM method uses one or two voltage sources and a number of fast switches. The simplicity of the power stage makes it an attractive choice for low power applications. Many dc-to-dc converters are PWM systems with the filter as an inherent part; they are natural extensions of ordinary PWM inverters. First dc-to-dc converters are generalized for bidirectional current capability. In order to produce bipolar voltages, a few alternatives were considered. The push-pull technique was discussed where the load is differentially placed between outputs of two current-bidirectional dc-to-dc converters. The converters are fed from a common voltage source and from a modulator with complementary output. Zero voltage appears across the load at the duty ratio of 0.5, while $D > 0.5$ produces a non-zero voltage. By symmetry the $D < 0.5$ generates a voltage of opposite polarity. The push-pull technique is capable of providing independently controllable bipolar voltage and currents on

the ac side, a true four-quadrant power converter.

This four-quadrant capability is the basis for an alternative to conventional ac uninterruptible power supplies. Having a bank of batteries as the energy storage elements calls for interfaces between the dc batteries and the ac line and the ac load. Conventionally, a battery is charged from the ac line by a battery charger and is used to power the ac load through an ac inverter. The flow of power is always from the line to the battery and to the load. The alternative way of interfacing the dc battery to the ac line and load is the use of a switched-mode amplifier. Now, there is only one power stage with dc (battery) on one side and ac (line and load) on the other side. With the power up, the line powers the load directly, and the amplifier behaves as a unity power factor battery charger (ac-to-dc). With the power disrupted, the amplifier is converted to an inverter to power the load (dc-to-ac). Therefore, the amplifier can be referred to as a complete dc-ac interface since it works in either direction.

The dc-to-ac inverter was analyzed in detail from the large signal dc transfer ratio to small-signal ac characteristics. The analysis was performed by use of the state-space averaging method. The method was shown to be valid for cases where the operating frequency (line frequency) is much smaller than the power bandwidth of the amplifier. This constraint is very realistic since high power bandwidth means smaller sizes of storage elements of the amplifier. To meet this criterion simplifies the calculations, because one can assume large-signal variation of the states of the system to be a series of steady-state

solutions for the circuit. Dc behavior of the inverter can now be easily characterized by interaction of the two constituent converters of the amplifier with the load. Nonlinear transfer characteristics of converters are transferred to the amplifier comprising those converters. It was shown that a small amount of parasitics can reduce this nonlinearity to a reasonable value. Assumption of quasi- steady-state at each operating point, simplifies the ac analysis by consideration of each operating point and its associated small-signal dynamics. Therefore, the analysis of large-signal variation of the system is approximated by a series of small-signal analyses for which powerful analytical techniques already exist. Very often it is required to regulate the output of the inverter to desensitize the output to variations of various system parameters, reduce harmonics, remove dc, etc. The loop design was performed around the quiescent operating point, and then checked at various operating conditions for possible degradation of stability. It was shown that owing to the complete symmetry of the system, dynamics of the system at the quiescent operating point can be analyzed by examination of only one converter, provided the correct steady-state and other conditions are met. However, at any other point, this symmetry is not valid and the complete amplifier must be analyzed. An experimental amplifier comprising two coupled-inductor Ćuk converters was then carefully examined. A feedback loop was designed, and was checked against operating points to verify stability. The design may be refined later to meet the requirement of transition between the modes.

The battery charger mode of operation is different for the inverter mode in the sense that it is forced upon the amplifier by a mandatory feedback around the system. In this case, the amplifier has an ac voltage source on its ac port (instead of a dissipative load). In this case, with the amplifier being a nonideal voltage source, the outputs of two voltage sources are paralleled, which can cause large currents. The output impedance of the amplifier is very low at low frequencies and a current feedback is required to convert this open-loop impedance to the desired form. For example, for unity power factor application, one prefers to have resistive impedance for the amplifier ac port to draw a current proportional to the voltage. Also one wants to vary the value of this effective resistance to be able to control the rate of power flow. Again, the feedback is designed around the quiescent operating point, and then checked against various operating points encountered. The control parameter is output current, and the dynamics of the system experience a large change owing to the replacement of the load by a voltage source. It was shown that with some precautions, at the quiescent operating point, the dynamics of the amplifier can be approximated from that of a single converter. Experimentally, the Ćuk amplifier was analyzed and a two-loop feedback was designed and checked for various operating conditions.

Finally, the complete UPS system was checked that has a single power amplifier and two control circuits for each mode of operation. The transition from inverter to charger mode is the controllable one where a smooth change of mode is possible. The reason is that the

requirement of equality of the final state conditions of one mode to the initial state condition of another mode can be exactly fulfilled. This includes incorporation of additional circuitry to preset the compensation network to the correct value too. The charge to inverter transition, however, can happen randomly and thus, there is no guarantee for a smooth transition. Still, the requirements on equality of initial and final states, suggest a circuit similar to the charger, to preset the correct voltages in the compensation network of the inverter. The worst case of this transition was found and some remedies to improve the situation were given. The experimental system was also checked for the worst case transition.

Therefore, the design of our UPS alternative starts with an appropriate power amplifier for which two separate control circuits are designed, one for the inverter, and one for the charger. At last these designs are refined to be able to improve the transition capabilities.

PART III

A NEW POLYPHASE SWITCHING POWER AMPLIFIER

CHAPTER 11

INTRODUCTION

Ac systems are widely used in almost all commercial and industrial applications where they operate on power obtained from the ac distribution networks. One of the advantages of distribution of power in ac form results from the use of polyphase systems. Polyphase operation and transmission allows substantial savings in the total cost of the network owing to the cancellation of return currents and consequent omission of return wires. Also, it is a cheap and reliable method of generation of a rotating magnetic field, which is the basic principle of operation of all ac motors. The area of electronic processing of polyphase power is a relatively new one, and is receiving more attention owing to advances in power device technology. Polyphase systems are mainly used in the high power range, and limitations of the power processors are generally dictated by those of the power switching devices.

Part II of this work focused on pulse-width-modulated ac systems. By being a generalized PWM system, switching dc-to-dc converters were specifically treated as building blocks of ac networks. Such extensions became possible by observation of the behavior of dc-to-dc converters, and by proper modifications to expand their *quadrant* capabilities. Single-phase ac generation was then performed by use of two modified

dc-to-dc converters.

This part generalizes the principle of operation of switched-mode single-phase ac systems toward their polyphase versions. Again, the dc-to-dc converters, and more advanced single-phase power amplifiers, are used as modules of polyphase power processors. However, among many ways to accomplish this task, the one with the simplest configuration and minimum count of elements is more desirable. So, the generalization process is steered to a form where a simultaneous reduction of elements and improvement of performance coincide in a switched-mode polyphase power amplifier.

Chapter 12 examines a few techniques of extension from single-phase ac systems to the polyphase systems. A brute-force method is discussed and its properties are enumerated. A closer look at this method provides some clues to improve the performance by advancement of the ordinary push-pull amplifier to a more general form, which is then extended to polyphase operation and to a new polyphase power amplifier. The amplifier comprises three current-bidirectional dc-to-dc converters with the load differentially placed among the outputs. Similar to the single-phase amplifier, this technique is capable of delivering high-quality regulated polyphase power to the load. The excellent quality of the polyphase voltages generated makes this amplifier suitable for almost all the line-related applications.

Chapter 13 demonstrates feasibility of the idea by an experimental one-horsepower variable-frequency variable-amplitude motor drive based on this concept. The drive is used to efficiently energize a

three-phase induction motor for variable speed operation of a general-type load. Owing to sinusoidal output waveforms, many problems associated with common motor drives such as harmonic heating and torque pulsation are eliminated. The drive uses three buck converters and its output is regulated to make it insensitive to variations of the input voltage, load, and other parameters of the system. The system is a general multiple-input multiple-output control network. However, by proper strategy, it is approximated to three identical non-interacting systems, for which feedback loops are designed.

Finally, owing to the general nature of the technique, a number of other interesting applications for the polyphase amplifier have also emerged. They include: uninterruptible power supplies, unity power factor ac-to-dc converters and battery chargers, fixed-frequency to variable-frequency converters and others as discussed in Chapter 14.

CHAPTER 12

NEW POLYPHASE POWER AMPLIFIER

This chapter examines ways to generate polyphase ac power by simple extensions of ordinary single-phase systems. There are numerous approaches to the problem, among which the simplest one is the most desirable scheme. Thus, the search is toward simpler configurations. For example, first, a brute-force method is examined and its salient features are pointed out. Then, by careful attention the remedy is offered. The push-pull configuration is modified toward a more flexible form to which another converter is added to obtain a polyphase amplifier. This polyphase amplifier consists of three current-bidirectional dc-to-dc converters and offers dramatic advantages when compared with the brute-force method. The technique uses practically half as many components with the outputs in the general form to allow conventional connection of the load.

Many capabilities of dc-to-dc converters are readily built into this system. For example, high gains can be obtained by nonlinear converters while isolation between input and output can be easily implemented by use of high-frequency transformers. The output (voltage, current, or a combination) can be regulated by use of feedback to obtain high quality outputs.

The general form of the output creates a family of new applications

for the method which will be discussed in Chapter 14.

12.1 Polyphase Operation

In the previous part, it was shown that the push-pull amplifier can be used as a single-phase inverter. The inverter may be extended for use in three-phase power generation by employing three separate inverters, one for each phase.

As customary with three-phase systems, one might want to put the outputs in a star or delta connection. However, because the outputs of the inverters may not be electrically isolated from the input, these connections are not possible in general and would cause uncontrollable currents to flow among the inverters. Nevertheless, there is a special case where the use of three separate inverters is possible. Three power amplifiers may be utilized as illustrated in Fig. 12.1 to generate a three-phase motor drive. The only requirement is that the three reference voltages constitute a three-phase system with the usual 120^0 phase displacement among them. The electrical isolation is provided by the windings of the motor, which are in this case used separately. This scheme works, but its application is severely limited. Although it is a rather straightforward implementation of power amplifiers to three-phase systems, a major drawback is that this technique requires six bidirectional power converters, two per amplifier in Fig. 12.1.

The goal, then, is to find an inverter with fewer converters and a general form of output which permits regular three-phase load connections. The general form of output connection, however, can be

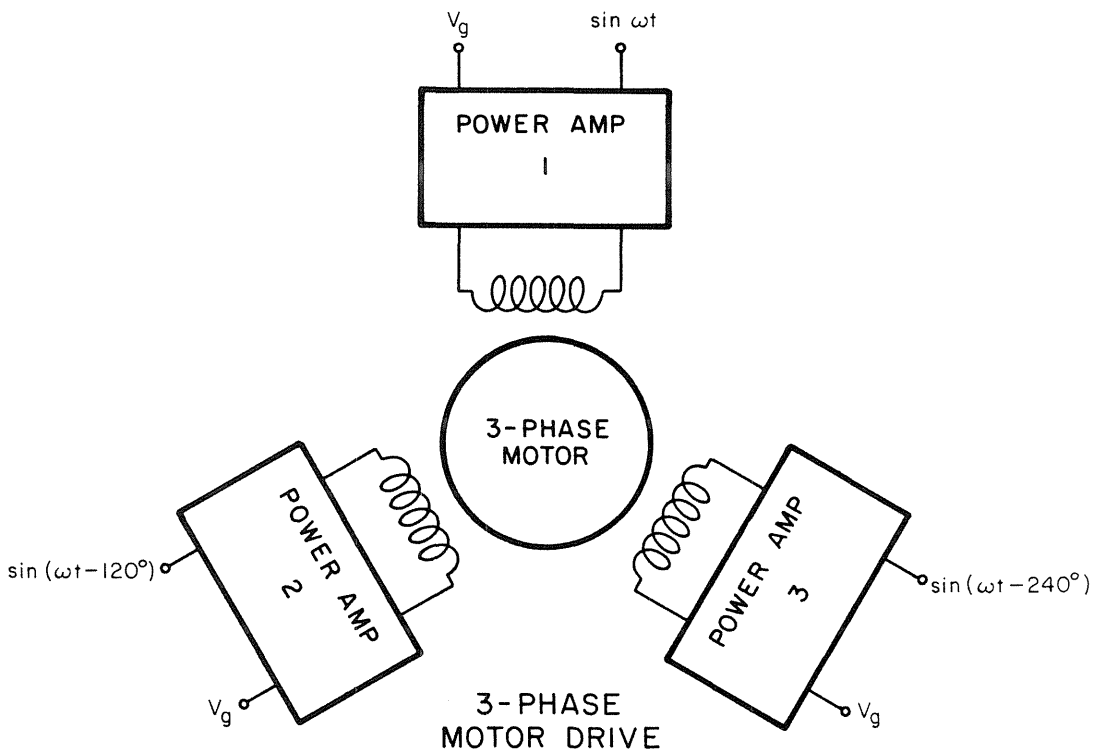


Fig. 12.1 Three-phase motor drive employing three regulated switching power amplifiers.

obtained by the same technique, but with the isolated version of the converters as demonstrated in Fig. 12.2. Each converter of the amplifier behaves as a controlled quasi-voltage source which provides voltages according to its inherent gain.

A conventional amplifier is shown in Fig. 12.2a where the converters are modelled as variable-voltage sources and share the same ground with the source V_g. Figure 12.2b models the isolated version in which the ground of v_g and the converter's outputs are separated. In order to provide the conventional load (3 or 4 wires), three isolated inverters may be put in a delta connection as shown in Fig. 12.2c, where d_1, d_2, and d_3 are determined by a set of three-phase sine waves. However, the outputs of the converters are all parallelled through the outer loop and, unless prevented by very accurate feedback systems, a large current can be generated between the converters.

Figure 12.2d, on the other hand, illustrates use of three isolated inverters in a star connection. This technique permits the general form of the output and the common point of the amplifiers can be utilized as the neutral connection for the load. It can be noticed that the unisolated version of the amplifiers, when employed in the star connection as in Fig. 12.2d, cause uncontrollably large currents since three semi-voltage sources are parallelled whose control signals are different. This is the result of control of six converters with three signals.

Next, we generalize the single-phase amplifier.

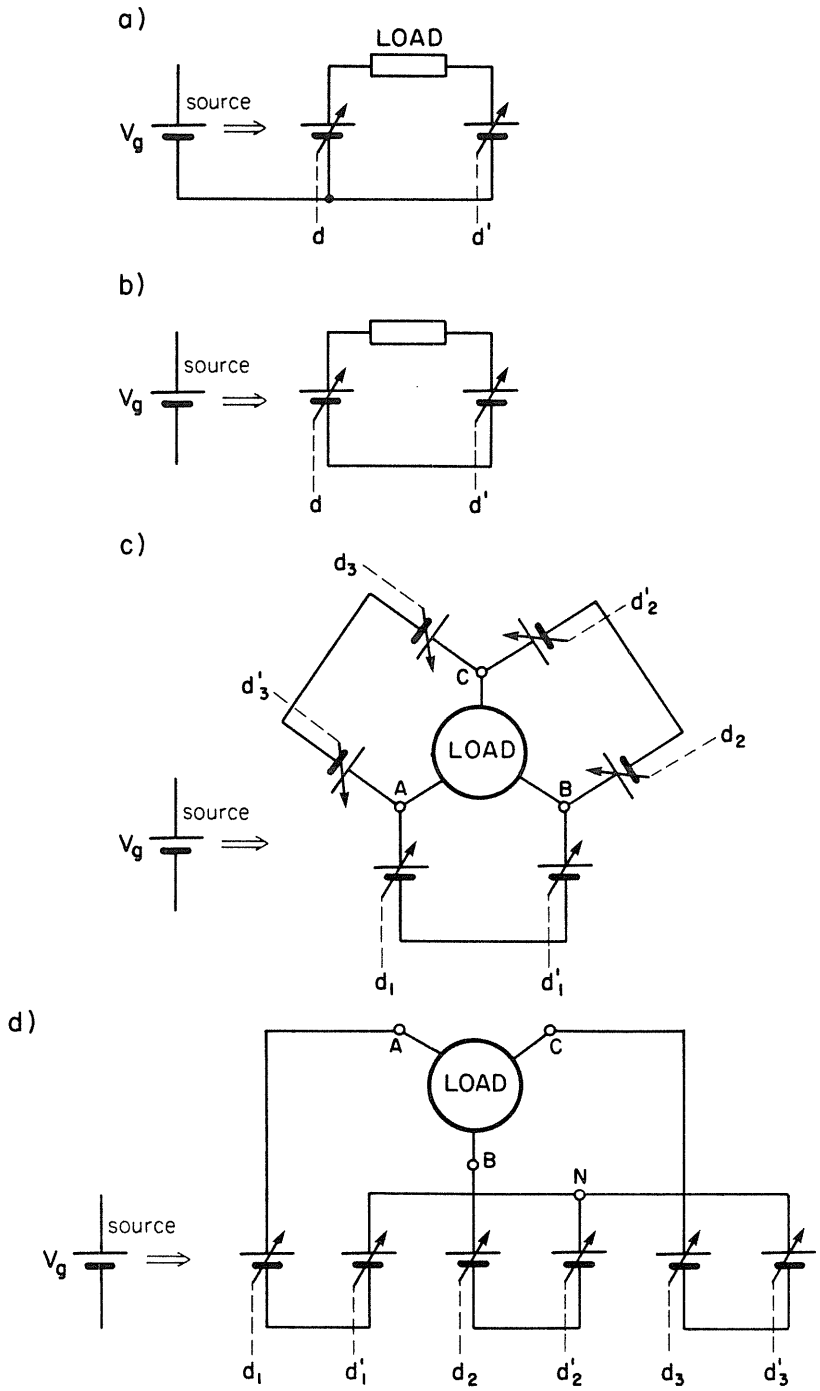


Fig. 12.2 *General three-phase connection: (a) a single-phase power amplifier, (b) isolated single-phase inverter, (c) delta connection of inverters, (d) star connection of inverters.*

12.2 New Polyphase Amplifier

The key to operation of the push-pull amplifier of Fig. 6.9 is the cancellation of the dc component of the output in the differential load. This was automatically provided at duty ratio D = 0.5 in the original amplifier, but this cancellation effect can be assured at *any* steady state duty ratio and corresponding output voltage, provided that two independent modulators as in Fig. 12.3a are used.

If two equal voltages are applied to the modulator inputs, the outputs of the two converters will be at the same dc potential, leading to zero voltage across the load. Therefore, even if the voltages of Fig. 12.3b (equal sine waves) are applied to the inputs, the differential output voltage remains at zero. This clearly illustrates that the quiescent operating point of the amplifier can be set to values other than 0.5 as well.

Nevertheless, it is easy to produce some useful ac power by implementing waveforms of Fig. 12.3c as inputs to the modulators — that is, by shifting the sinusoidal components of the signals to be 180^0 out of phase. As in the original push-pull amplifier, the output is the difference between two out-of-phase sine waves with equal dc components. Hence, a pure sine wave can be obtained and the previous push-pull output reproduced (Fig. 6.9), but now with an arbitrary quiescent operating point and arbitrary dc component.

Even the special 180^0 phase shift can be dispensed with. With the two separate modulators, an arbitrary phase shift between the two reference sine waves may be implemented and still result in a sine wave

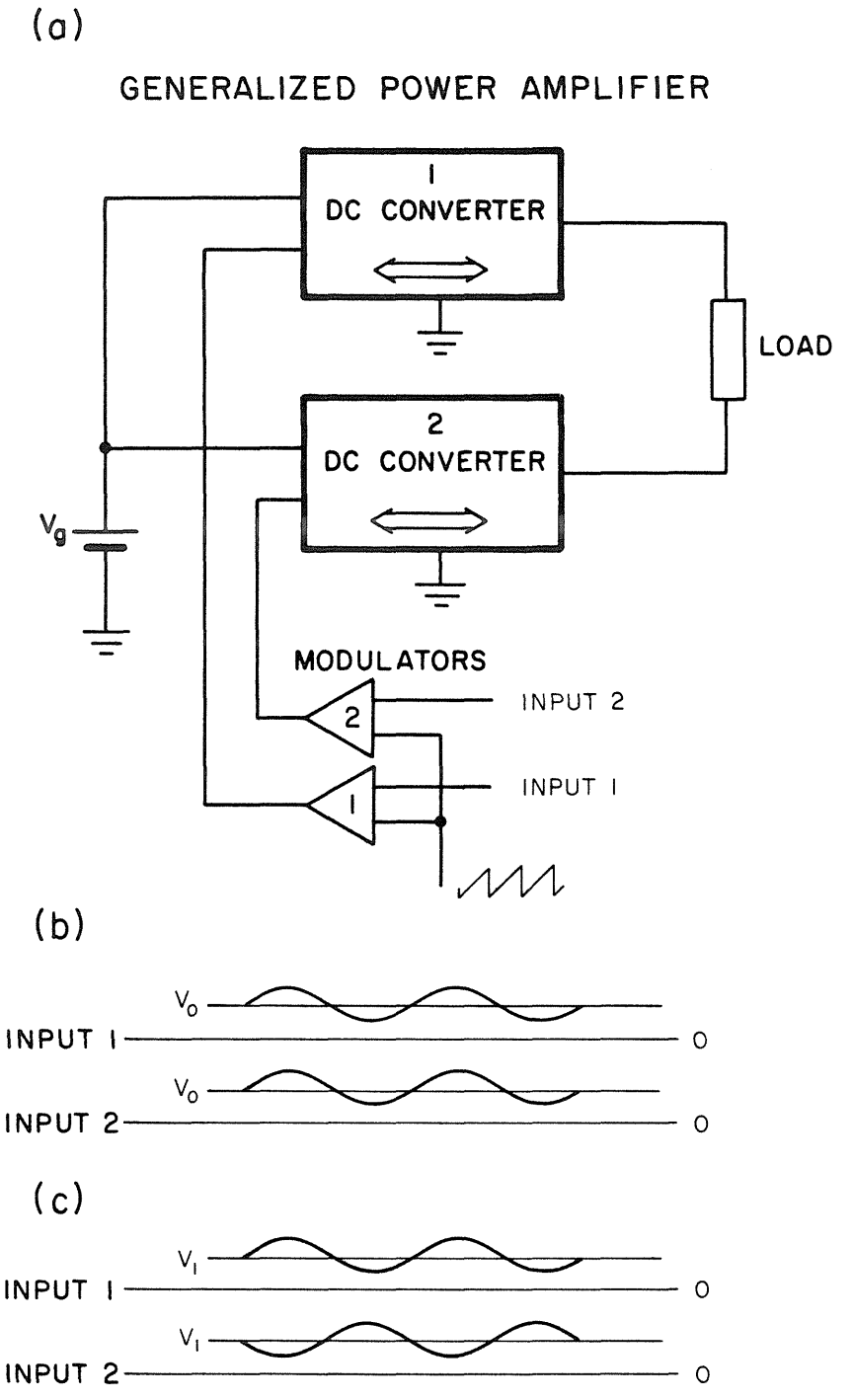


Fig. 12.3 *Generalized push-pull amplifier: (a) each converter has its own modulator, (b) equal inputs generate zero output and (c) a sine wave is generated with the set of inputs.*

output. This is, of course, owing to the unique nature of sinusoidal quantities, whose addition even when phase-shifted, yields sinusoidal outputs. A non-sinusoidal quantity, when phase shifted and subtracted from the original, can result in output changed in its form, although the dc parts are still eliminated.

For the sinusoidal case, there is a particular phase shift which is of more interest than any other. Consider the case where the sine waves are 120^0 out of phase and nonlinearities of the converters are neglected. The load voltage becomes:

$$[DC + \sin\omega t] - [DC + \sin(\omega t - 120^0)] = \sin\omega t - \sin(\omega t - 120^0) =$$

$$= \sqrt{3}\,\sin(\omega t + 30^0) \qquad (12.1)$$

It now seems quite natural to add a third converter with its own modulator, driven with a 240^0 phase-shifted sine wave, to the circuit as shown in Fig. 12.4. This is the new polyphase sine amplifier [13,22]. The modulators are driven by a set of three-phase sine waves:

$$\text{input } 1 = V_1 + V_2 \sin\omega t$$

$$\text{input } 2 = V_1 + V_2 \sin(\omega t - 120^0) \qquad (12.2)$$

$$\text{input } 3 = V_1 + V_2 \sin(\omega t - 240^0)$$

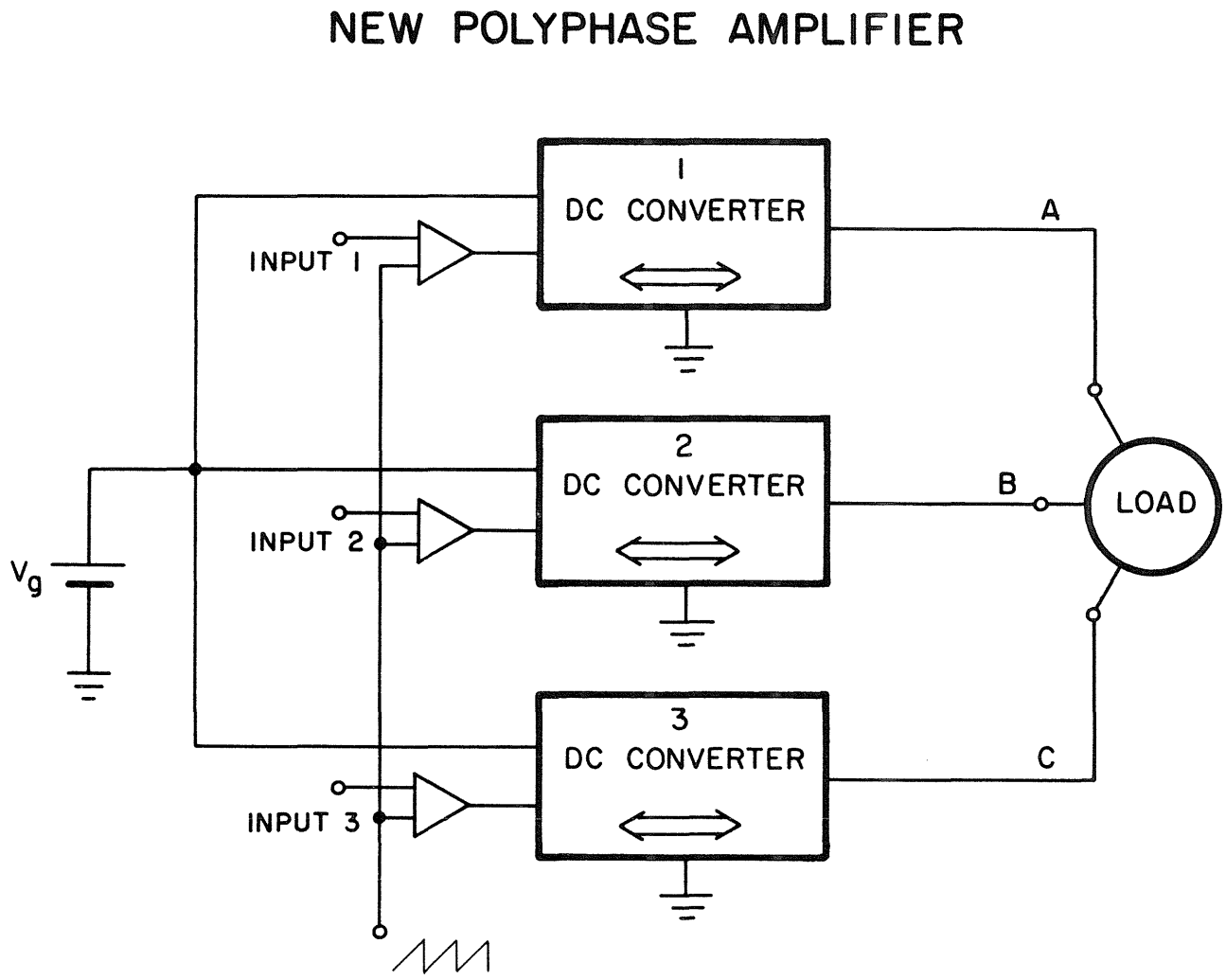


Fig. 12.4 *New three-phase switching amplifier. Three bidirectional dc-dc converters, with their own modulators, driven by a set of three-phase sine waves, constitute three phase voltages around the differential load.*

This set of inputs results in the following output voltages (with respect to ground):

$$V_{AG} = V_{DC} + V_m \sin(\omega t + \gamma)$$

$$V_{BG} = V_{DC} + V_m \sin(\omega t - 120^0 + \gamma) \qquad (12.3)$$

$$V_{CG} = V_{DC} + V_m \sin(\omega t - 240^0 + \gamma)$$

where G refers to ground and γ is the phase of the control transfer function at the frequency ω. The voltage V_{DC} corresponds to a steady-state duty ratio (representing V_1). Figure 12.5a shows these line-to-ground voltages. The differential load actually receives the difference of these voltages which are line-to-line voltages and again constitute a balanced three-phase system:

$$V_{AB} = \sqrt{3}\, V_m \sin(\omega t + 30^0 + \gamma)$$

$$V_{BC} = \sqrt{3}\, V_m \sin(\omega t - 90^0 + \gamma) \qquad (12.4)$$

$$V_{CA} = \sqrt{3}\, V_m \sin(\omega t - 210^0 + \gamma)$$

The line-to-line voltages are shown in Fig. 12.5b.

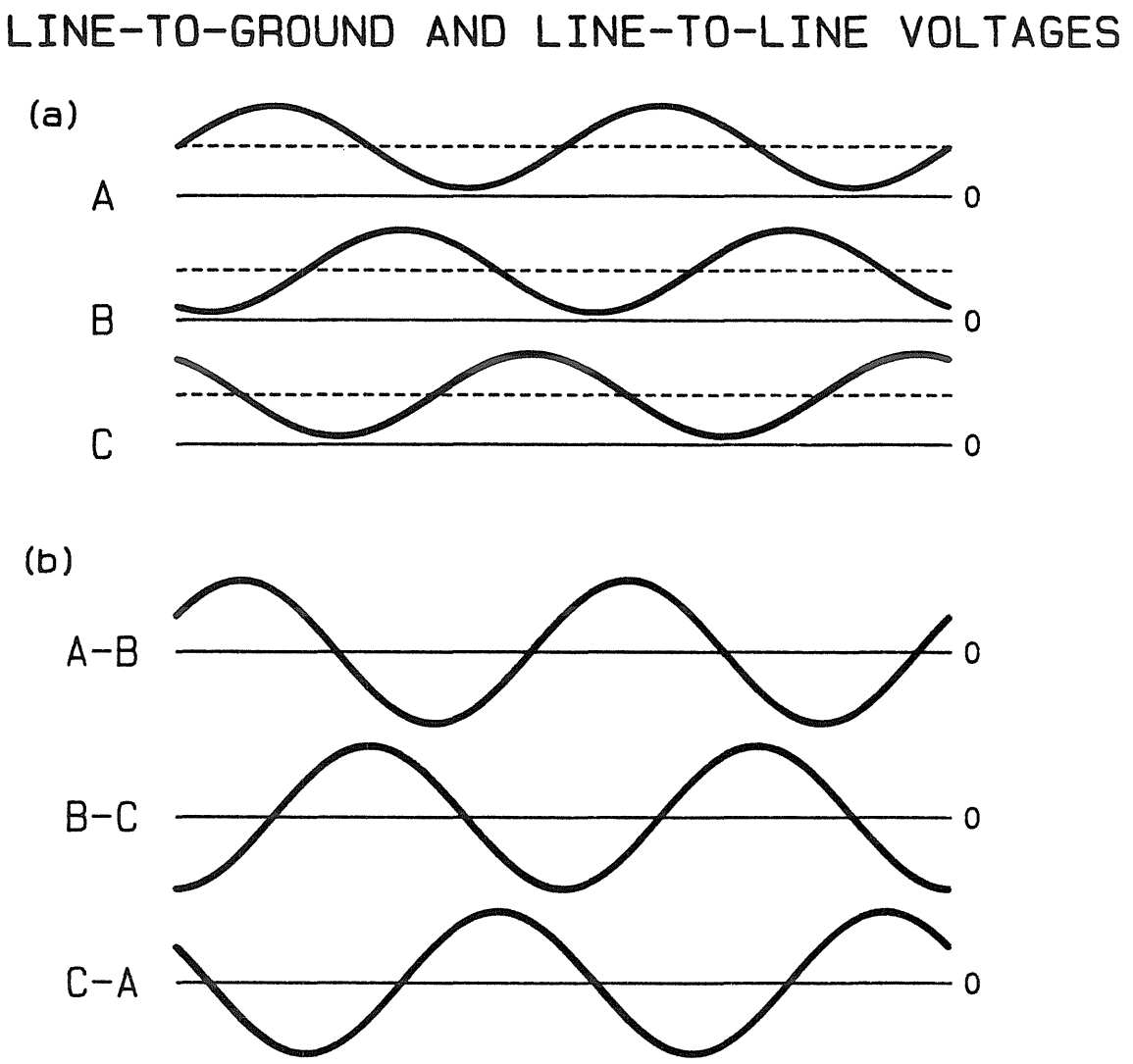


Fig. 12.5 *(a) Line-to-ground and (b) line-to-line voltages generated by the new three phase power amplifier. The dc component of the line-to-ground voltages automatically disappears in line-to-line voltages which are pure ac.*

Note that the dc potential present in line-to-ground voltages has automatically vanished in line-to-line voltages. However, any difference in the dc potentials of each phase, V_{DC}, would directly lead to presence of dc voltage (and consequently dc current) in the line-to-line voltages and the load. This could have serious implications for an ac motor, which cannot take even small dc currents, owing to saturation and torque pulsation problems. In fact, in open loop operation, special care must be devoted to ensure equality of the dc potentials of the phases. However, as shown later in Chapter 13, this problem is easily solved by closing feedback loops around the converters and employing integral compensation. Also, it may be noted that in Fig. 12.4, the modulators need not necessarily share the same ramp. As a matter of fact, phase-shifted ramps may be applied to the converters to improve the overall input and output current waveforms.

Comparison of the new amplifier with the brute-force method of Fig. 12.1 shows that the number of converters has been significantly reduced from six to three, and also that the output is in a more general form and can drive loads which are in delta or star connections (no null connections). Figure 12.6 shows implementation of the new polyphase amplifier using three bidirectional Ćuk converters (modulators are not shown). Also, the operation is not limited to three-phase systems and can be easily expanded to N phases. Figure 12.7 illustrates an N-phase inverter employing N bidirectional dc-to-dc converters, N modulators assumed inclusive to the converters, and a set of N-phase sinusoidal inputs. Again the outputs are all floating on the same dc level which

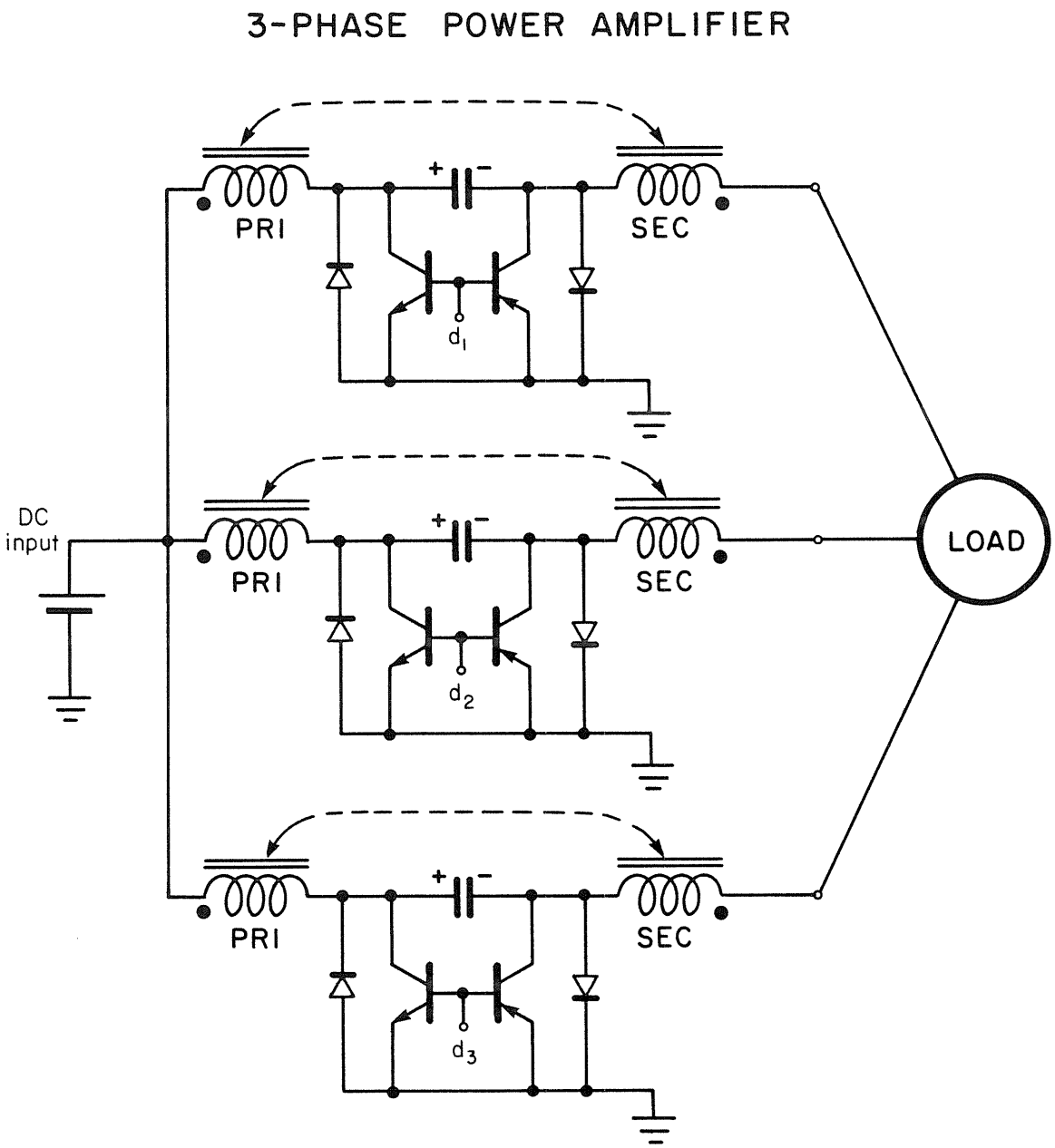


Fig. 12.6 Three-phase switching amplifier employing three Ćuk converters. The d_1, d_2, and d_3 are connected to the modulators.

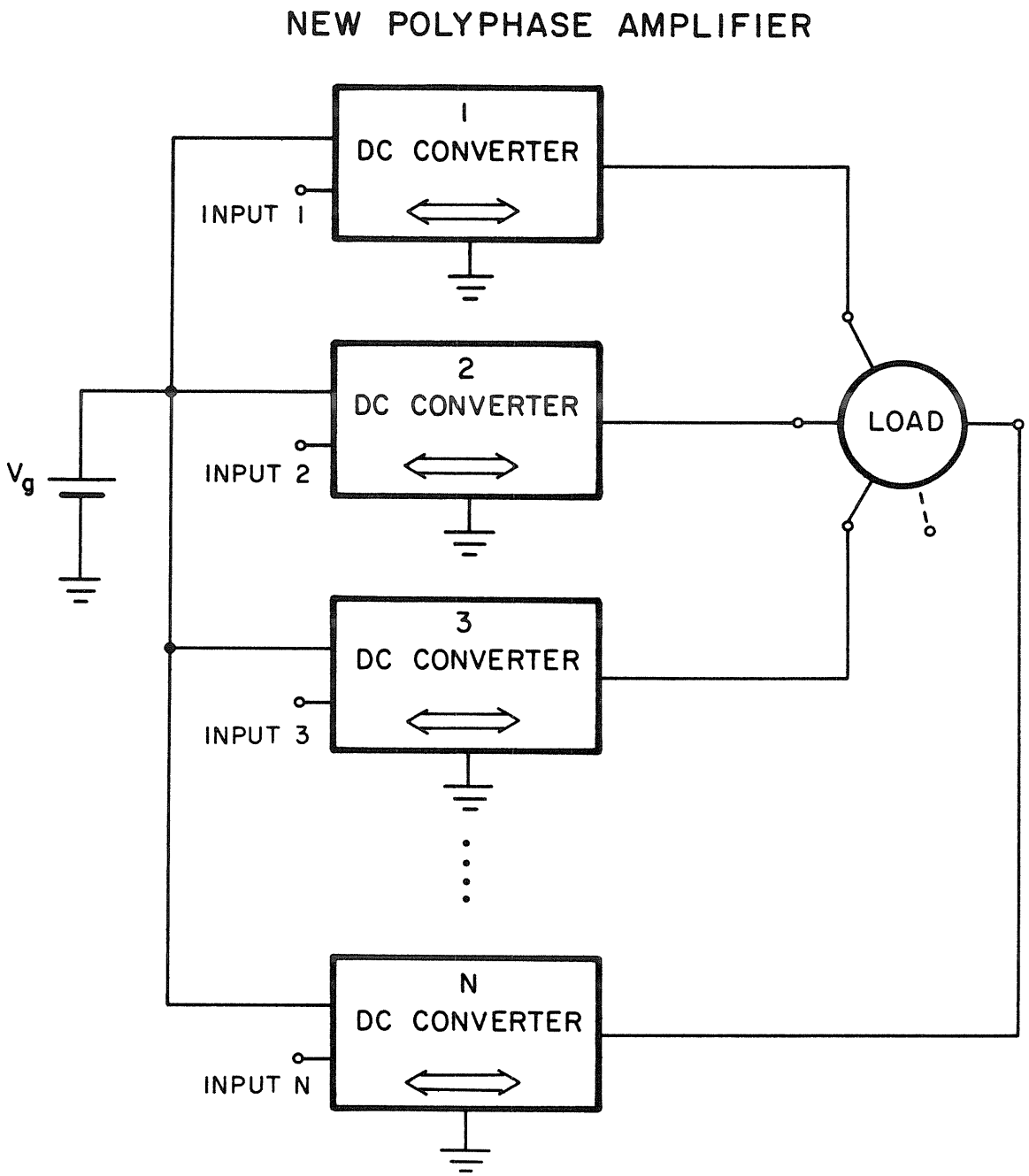


Fig. 12.7 *Extension of three-phase converter of Fig. 12.4 to a general polyphase amplifier. Modulators are inclusive to the converters and a set of polyphase sine waves drives the inputs.*

is cancelled out in the differential load.

Overall, the polyphase switching amplifier has the following advantages:

1. *Sinusoidal voltage and current waveforms.*
   In the area of motor drive this eliminates harmonic heating and torque pulsation. EMI is also significantly reduced. Finally the design of the speed-control loop can be simplified owing to the absence of switching noise on the sense signals.
2. *Generality.* Owing to the amplifier's consisting primarily of dc-to-dc converters, all advances made in the dc converter area can be directly applied to this amplifier. For example, in the case of requirement for galvanic isolation between input and output, the dc isolated version of the converters can be employed to eliminate bulky 60 Hz transformers. The same high frequency transformers in the isolated versions can also be used to increase or decrease the output voltage, although some converters inherently have this capability. Paralleling of converters to increase the output power is also simple.
3. *Versatility.* Sinusoidal outputs create many line related applications for the polyphase amplifier. Also, the four quadrant capability of the original push-pull amplifier is still retained, which generates a whole line of new applications. These applications, some of which will be discussed in Chapter 14, include:

Uninterruptible power supplies (UPS), unity power factor (UPF) battery chargers, electronic capacitors, and battery to three-phase line interfaces.

A comparison of the new polyphase amplifier and that of Fig. 12.2d reveals that now the isolation is not necessary and the converters 2, 4, and 6 of Fig. 12.2d have been eliminated and replaced by short circuits. This may also be viewed as the two converters of each amplifier replaced by a single one, cutting the complexity in half while raising the null's dc level. The outputs of the new amplifier are all floating on a dc level, so that connection of the null to the ground is not possible. However, if the load requires a grounded null connection, another bidirectional dc-to-dc converter may be added to the circuit. Unlike in the main converters, the output of this converter is held constant and is set at the same dc level of the other converters and is used as the null connection. Thanks to the polyphase idea, this converter must be able to handle only the current produced by asymmetry of the load. The required power capability of additional converter is thus a fraction of that of the main converters, and the additional converter is of course unnecessary for a symmetric load.

As was mentioned earlier, each of the converters in the new amplifier replaces two converters (in series) in the brute-force method. Although dc equilibrium is obtained, now each converter must produce the complete voltage swing generated by the original two converters. That is, each converter while handling the same current, must provide on the order of twice the voltage swing on the output than that of each

converter of Fig. 12.2d.

12.3 Discussion

The polyphase amplifier is a generalized push-pull system and all the differences between converters of the amplifier and those of a dc system have already been discussed in Part II. For example, full power is available as long as the output frequency is below the open-loop bandwidth of the converters. Restriction of the signal frequency (line frequency) to much lower than the converter bandwidth greatly simplifies the dc and small-signal ac analysis of the system by the approximation of the states to follow a series of steady-state trajectories. The dc analysis is reduced to finding the steady-state solution of the system, while the ac analysis is performed at each operating point defined by the associated steady state quantities.

The dc and low-frequency transfer characteristics of the amplifier become nonlinear if the gain characteristic of each individual converter of the system is nonlinear. An open-loop buck amplifier theoretically can produce distortion-free low frequency sine waves at the load, while open-loop outputs provided by other types of amplifier will have some distortion. However, owing to the inherent high gain of the nonlinear amplifiers, they can be of great help in simplification of the system (by avoiding transformers). Also, feedback may be applied to reduce the distortion appreciably.

The dc analysis is different from that of a single-phase push-pull amplifier because there is another degree of freedom, the quiescent

operating point D. The transfer characteristic in the sense defined in Part II is meaningless since it is double-valued, hinting at the existence of even harmonics. A better form is to find the output (line-to-line) when the input is excited by a set of three-phase sine waves,

$$d_1 = D + a \sin\omega t$$

$$d_2 = D + a \sin(\omega t - 120^0) \tag{12.5}$$

$$d_3 = D + a \sin(\omega t - 240^0)$$

where D is the quiescent duty ratio, and a is the depth of modulation limited by

$$a = \text{Min } (D,D') \tag{12.6}$$

If the lossless gain of each converter is M(d), then

$$\frac{V_{12}}{V_g} = M(d_1) - M(d_2) \tag{12.7}$$

For example, for a three-phase boost amplifier,

$$\frac{V_{12}}{V_g} = \frac{1}{\frac{1}{d_1}} - \frac{1}{\frac{1}{d_2}} = \frac{1}{D' - a\sin\omega t} - \frac{1}{D' - a\sin(\omega t - 120^0)} = \tag{12.8a}$$

$$= \frac{\sqrt{3}\, a \sin(\omega t + 30^0)}{[D' - a\sin\omega t]\,[D' - a\sin(\omega t - 120^0)]} \tag{12.8b}$$

The same gain for the buck converter is

$$\frac{V_{12}}{V_g} = d_1 - d_2 = \sqrt{3}\, a \sin(\omega t + 30) \tag{12.9}$$

The expression for the buck-boost and Ćuk amplifiers, even though different from Eq. (12.8a), results in Eq. (12.8b). Equation (12.9) indicates an open-loop pure sinusoidal output for the buck amplifier with maximum line-to-line voltage of $\sqrt{3}/2\ V_g$, since the maximum of a is 0.5 (at $D = D' = 0.5$).

However, Eq. (12.8b) indicates a sine wave output with low distortion if in the denominator the nonlinear terms are kept small, i.e. $a/D' \ll 1$. The values for a and D are determined from the peak output voltage requirements, which are not unique. At small a/D' cases, the maximum gain is almost

$$\frac{V_{12}}{V_g}_{\text{peak}} \simeq \frac{\sqrt{3}\, a}{D'^2} \tag{12.10}$$

which illustrates lower distortions at higher D (lower D'), because to deliver the same peak voltage, at lower D' values, smaller values of a/D' are needed. Figure 12.8 shows the sinusoidal outputs for the same peak value of 1 but at two sets of a and D values. The thick lines are for (D,a) = (0.8, 0.0228) and the thin lines indicate the output for (D,a) = (0.3, 0.243). Clearly the higher duty ratio delivers a better quality open-loop output. If one calculates the total harmonic distortion for the line-to-line voltages of three-phase boost, buck-boost, and Ćuk amplifiers, the following is obtained:

$$\text{Total Harmonic Distortion} = \left[\frac{\left(1 + \sqrt{1 - r^2}\right)^2}{4\sqrt{1 - r^2}\left(1 - \frac{r^2}{4}\right)} - 1 \right]^{\frac{1}{2}}, \quad r = \frac{a}{D'} \tag{12.11}$$

which predicts respectively 5.7% and 17.9% distortion for the first and second cases of Fig. 12.8. Figure 12.9 shows the distortion versus the ratio a/D'. Equation (12.11) can be modified for the single-phase amplifier too. In an ordinary push-pull amplifier D' is restricted at 0.5 and, for maximum gain, only one value of a is available. However if the generalized amplifier of Fig. 12.3a is used, much higher quality waveforms are obtained at higher D values (for the same gain).

The dc analysis of the system has a procedure close to the single-phase version, however, interaction of the three converters upon each other — through the load — needs careful attention. Chapter 13 treats this problem in detail.

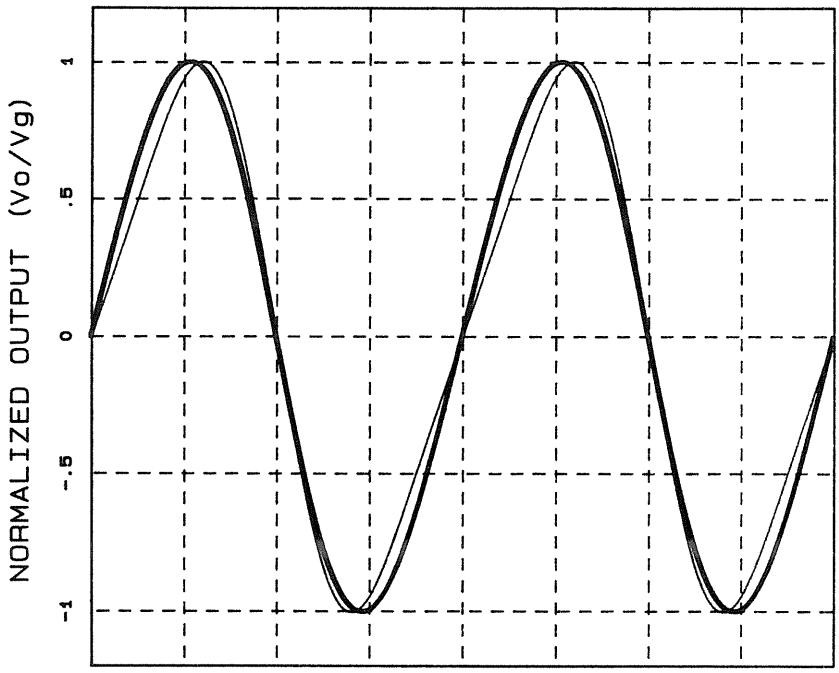


Fig. 12.8 *Production of sine wave with gain of* 1. *Thick lines:* D = 0.8, a = 0.0228. *Thin lines:* D = 0.3, a = 0.243.

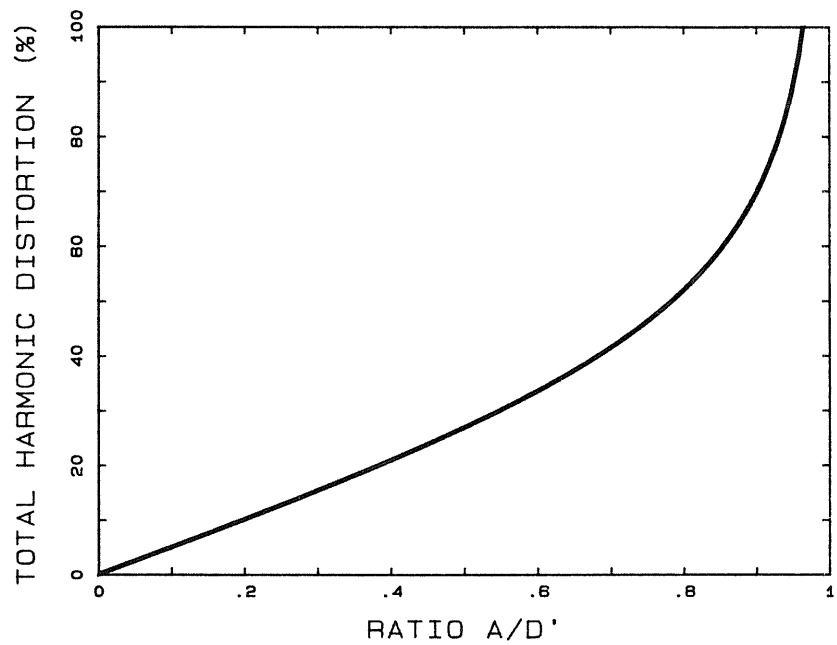


Fig. 12.9 *Total harmonic distortion for boost, buck-boost, and Ćuk three-phase amplifiers.*

12.4 Review

High power ac systems are almost all designed to operate from polyphase ac power. A few possibilities exist to extend a single-phase system to a polyphase one and among these methods, that with a simpler and more general form is preferred. The brute-force method, consisting of three single-phase systems was tested and was shown to have a very limited use. A closer examination of the method gave clues to generalize the conventional push-pull amplifier to a form upon which other converters may be added to construct a polyphase amplifier. The new amplifier, then, has three (N) bidirectional dc-to-dc converters each with its own modulator, feeding from a single dc source. The load is placed differentially on the outputs. A set of three (N)-phase sine waves applied to the modulators produces sinusoidal polyphase voltages around the load. Many advances made in the area of dc-to-dc converters are applicable to this amplifier, as well as a line of new applications introduced by the technique. For the dc analysis, it was shown that even though the buck type is essentially distortion free, the nonlinear converters can simplify a design owing to inherent high gains to produce larger output voltage swing. The results of these calculations can also be applied to single-phase mode to improve the output waveforms.

CHAPTER 13

EXPERIMENTAL VERIFICATION — VARIABLE-SPEED MOTOR DRIVE

So far, the idea of a polyphase power amplifier has been introduced, and the theoretical background has been established. A practical example of its implementation is now provided. The block diagram of Fig. 12.4 is realized by a set of three buck-type converters to create a variable-voltage variable-frequency 1 hp motor drive.

An ac induction motor works on the rotating magnetic field principle. A polyphase voltage set on its stator winding (with the similar spatial phase displacement) generates a rotating magnetic field inside the motor. This field crosses the rotor which has shorted windings and, by transformer action, produces currents in those windings. The current in the rotor in turn produces another field whose interaction with the original stator field produces a net torque and mechanical movement. Usually an induction motor rotates almost but not quite, at the speed of the rotating magnetic field (synchronous speed). The difference between the synchronous and actual speed is called slip speed. The slip is normally very small, and therefore for normal line applications the induction motor practically is a constant speed machine. Varying the input voltage of the motor alone has some limited effect on the speed with certain types of load.

Much better performance is obtained if the input frequency is changed as well as voltage or current levels. This causes the rotational speed of the magnetic field to vary, and the rotor to very closely follow these changes, resulting in a high performance speed controller. Note that the magnetizing field of the motor depends on both the voltage and frequency. At lower frequencies, in order to prevent saturation, the input voltage must be reduced almost proportionally such that $V/f \simeq$ constant. Therefore, a variable-voltage variable-frequency drive is required for speed control purposes. The polyphase power amplifier has a good potential for this type of application.

13.1 Drive

The purpose of the following hardware development is to demonstrate the new polyphase amplifier concept at a 1 hp level. A brief description of the practical hardware follows.

Figure 13.1a shows the power stage of the motor drive. Three current-bidirectional buck converters are shown which are fed from a single voltage source and the outputs are connected to the stator winding of a 1 hp induction motor. The drives for the transistors also include: modulator, dead time control to prevent the transistors from conducting at the same time, soft start, and current protection circuits. The drive must provide up to 120 V_{rms} (line-to-ground) voltage around the load with peak current of close to five amperes. This corresponds to a nearly 340V swing on each output. In the case of the buck converter, the maximum gain of each stage is unity and therefore V_g must be more

than 340 volts; for simplicity it was selected to be 500 volts.

If the input voltage is obtained from the rectified line, it is almost 300 volts, not enough for the maximum power requirement. The remedy can be either to change to nonlinear high gain converters (Section 12.3) or, after reaching the limit of maximum output swing, change to nonsinusoidal output waveforms (higher rms value with the same peak). This last method, however, can be used only for loads such as motors where at high speeds they can tolerate nonsinusoidal voltages even though it causes some additonal torque pulsation and harmonic heating. Also, the open-loop amplifier does not generate distortion, and so in order to generate maximum output swing, the quiescent duty ratio was selected to be 0.5 during the output cycle, and varies between ideal values of 0.16 and 0.84.

Each of the switches (S_1 to S_6 in Fig. 13.1a) of the converter is realized as shown in Fig. 13.1b. As can be seen, the cascode or emitter cutoff technique has been used to ensure fast and reliable switching. The upper transistor, Q_1, is a high voltage, high current transistor and the lower transistor, Q_2, is a low voltage, high current one. When the switch is ON, both transistors are ON. At turn off Q_2, which is fast, turns off quickly, while Q_1 is still ON. The emitter of Q_1, then, is opened and so Q_1 is turned off. The turn-off process is thus fast and reliable.

The driver is activated by the logic circuit shown in Fig. 13.2a. Only half the logic is shown while the modulator is common to two switches (e.g. S_1 and S_2). A dead-time circuit ensures that ON times

BUCK TYPE 3-PHASE VARIABLE SPEED MOTOR DRIVE

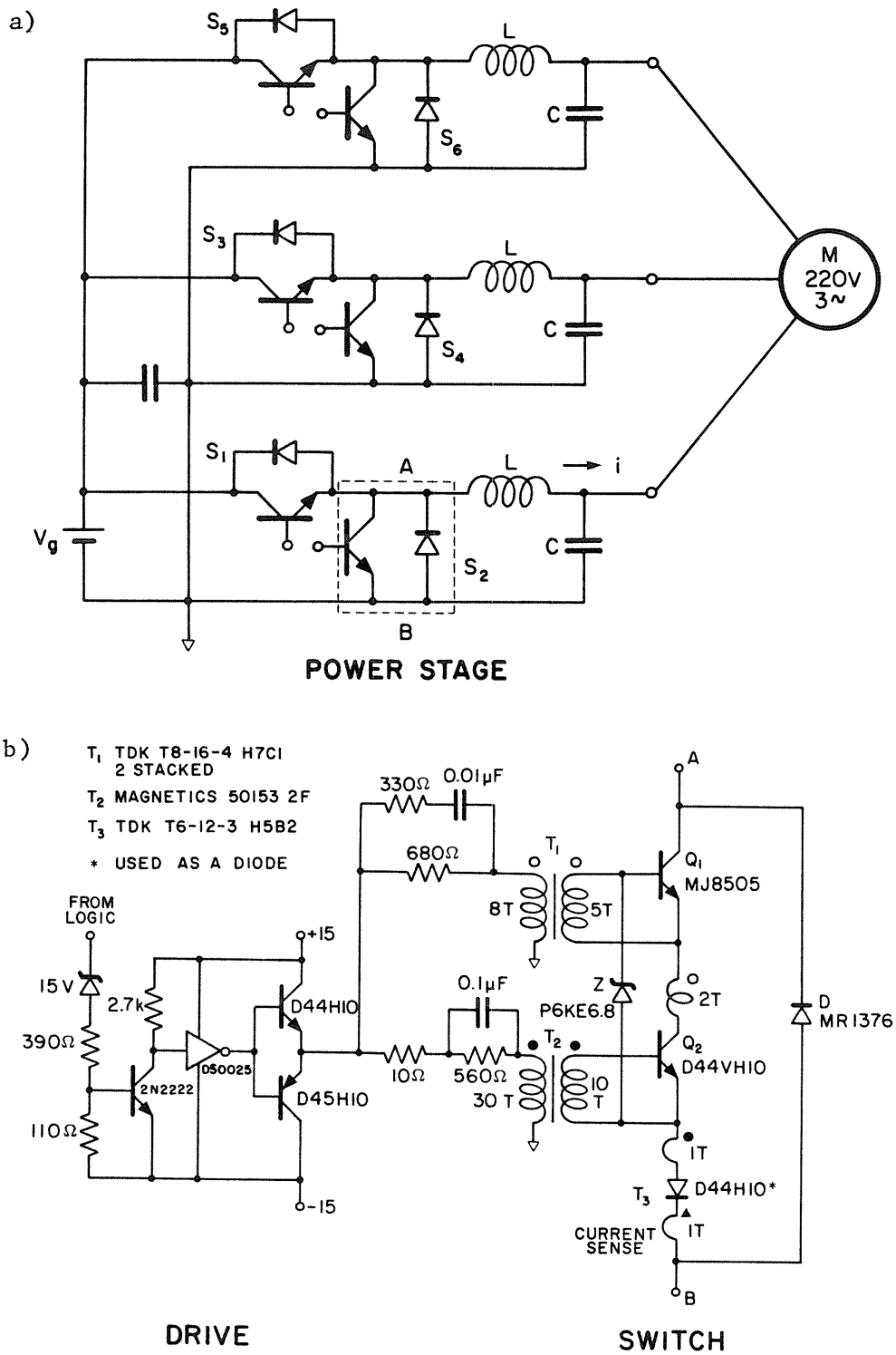


Fig. 13.1 (a) Buck three-phase variable speed motor drive. (b) Practical implementation of one switch and its drive.

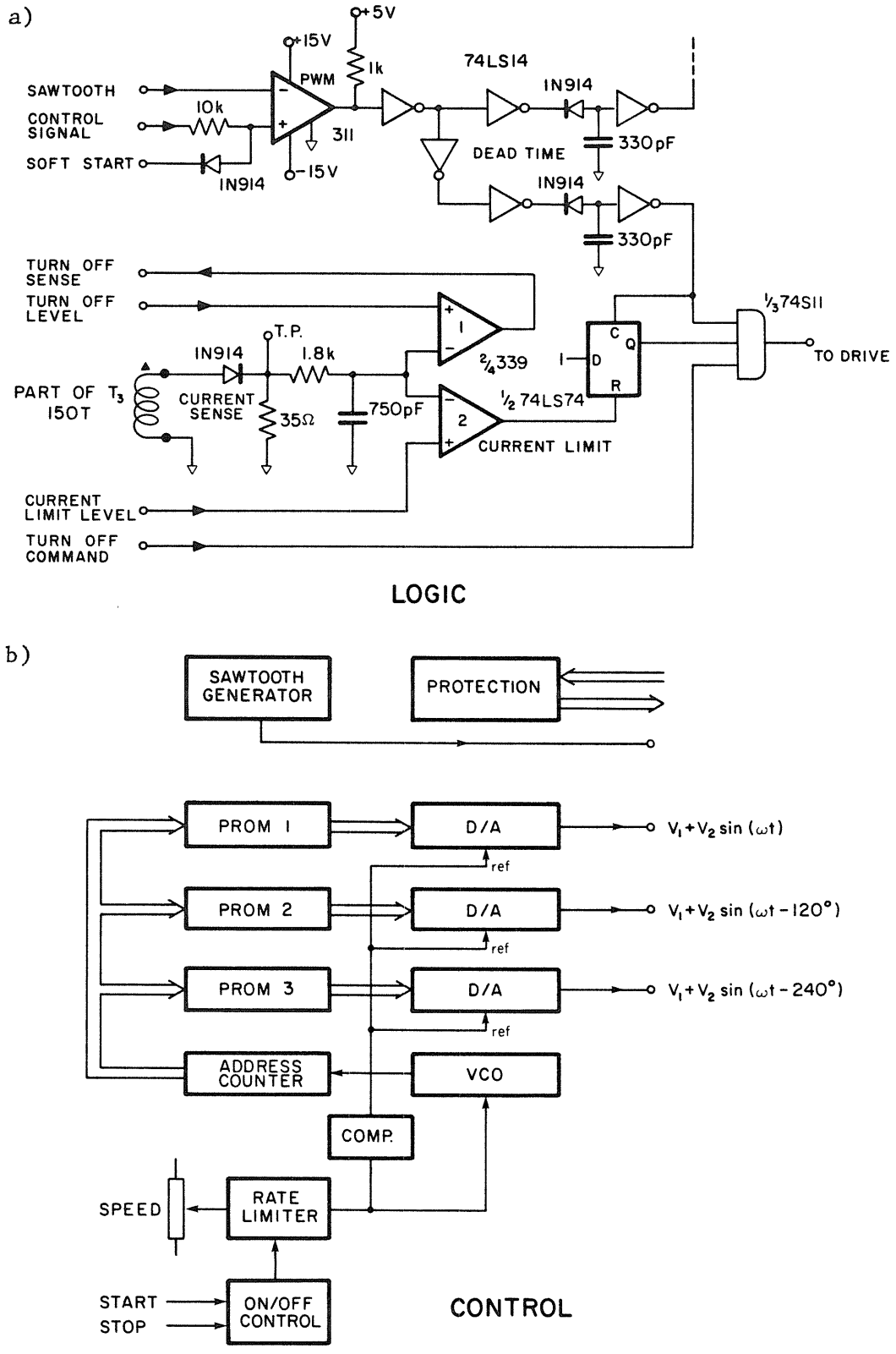


Fig. 13.2 (a) Logic board to control the switches. (b) Main control.

of the two switches will not overlap. The remaining circuitry is for current sensing and current limiting. Comparator 2 is used to shut the switch OFF immediately after sensing high currents (set by current limit level). In cases such as short circuits, the turn-off speed of the switch may not be fast enough, and then comparator 1 senses higher current levels than comparator 2 and shuts the whole system off.

The control board provides various reference signals and is responsible for supervisory functions. This board provides current protection levels, soft start, and other protective features. The 20 kHz sawtooth for the modulators and a set of three-phase sine waves are generated as shown in Fig. 13.2b. The sine waves are generated digitally by storing the numerical values of sine functions in PROMs as lookup tables. By successively addressing the PROMs, a sequence representing polyphase sine waves is generated which is converted to analog signals by three D/A converters. Variation of the rate of addressing the PROMs changes the frequency of the sine waves while adjusting the reference currents of the D/A's control their amplitude. The speed control signal is connected to a balanced voltage controlled oscillator (VCO) and through a compensator to the D/A references, which provide the reference sine waves with nearly constant V/f. The quiescent operating point of the converters is determined by the amount of dc voltage added later to these sine waves. For open loop operation, these sine waves can be directly applied to the "control signal" inputs of the logic boards (Fig. 13.2a) which modulate the duty ratios and subsequently produce polyphase voltages on the motor. In

practice, one regulates the output voltages to desensitize the drive to variations of line, load, and other parameters.

13.2 Regulation of the Output

Large variations of input voltages and/or load current can produce substantial changes in the output voltages of the amplifier. Also, converters with nonlinear characteristics may not reproduce good large-signal sine wave outputs when excited with sinusoidal inputs (Section 12.3). This effect in conjunction with parasitics, may be intensified by reactive and nonlinear loads where the output voltages and currents are not in phase, further increasing the distortion. These, together with the requirements to eliminate dc from the load, calls for feedback regulation of the outputs. However, one must clearly distinguish this regulation from speed or torque or any other type of low frequency control technique that is ordinarily applied in motor drives. Usually the motor drives provide some voltage on their outputs which are not regulated (open-loop) and any regulation is done in a larger and slower loop around the whole system which consists of the drive and the motor. The regulation of voltage is just to control the output voltages of the converter and to maintain a low distortion output. This is performed in high speed control loops centered around the electrical quantities (i.e. voltage) of the drive. A speed control loop can then be applied to the total drive and motor combination.

So far we have separated the task of voltage regulation from the normal and sometimes optional speed control loops. For the output

voltage regulation one must consider that unlike the single-phase version of Fig. 7.2, the polyphase amplifier has many controlling inputs. Also, any change in one output will affect the other outputs through the differential loads, and therefore, the circuit is a multiple-input multiple-output feedback system. For such systems, the general form of feedback is as shown in Fig. 13.3. Compensation networks sense the output voltages of the stages as well as all other states of the system and adjust the duty ratios appropriately. However, this general form is very complicated and one would prefer to break the task into several smaller portions. To do this, the first step is to break the circuit into three separate non-interacting converters. Next, we analyze one converter assuming that the loop is closed around the other two converters. Then, we design the loop and finally go back and check the validity of the original assumption of non-interaction.

For each section, the equivalent circuit model for the motor is required, so let us start with the motor. The motor is of a nonsalient squirrel-cage rotor type, where the electrical characteristics have a slight dependence on the rotor position. These characteristics, however, depend on the input frequency and slip of the motor which means that they change with variation of speed of the rotor. Based on a series of transformations of the rotor to stator circuit [16], the equivalent circuit for one phase of the motor is found to be as illustrated in Fig. 13.4a. The model is a steady-state model suitable for speed control application. However, it can be used for high frequency perturbation modelling necessary for voltage regulation purposes.

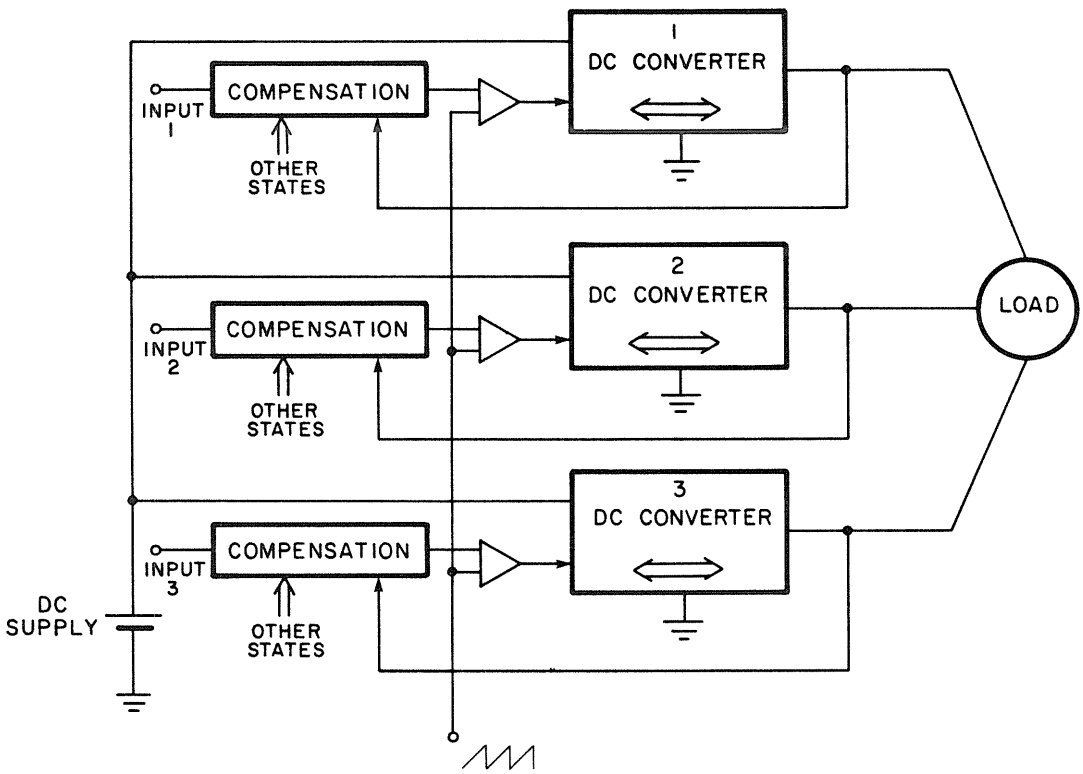


Fig. 13.3 General form of output voltage regulation of the three-phase amplifier.

Notice the variable resistor inversely proportional to slip r_2/S, by which the dependence of the characteristics on slip is modelled. Elements L_1 and L_2 are leakage inductances of the stator and the rotor (reflected to the stator circuit), where L_M denotes the magnetizing inductance. The current in L_M represents the flux, and thus it is easy to see that in order to keep a constant flux, the ratio V/f must be held almost constant (at low frequencies the resistive drop upsets this balance). This is an analogy to constant excitation field in a dc motor controller. Consider that nominal three-phase voltage is applied to the motor and that it is running at a speed very close to its synchronous speed. Slip with respect to the synchronous speed is very small. Now, if small-signal high frequency signals are injected into the motor, corresponding synchronous frequencies will be very high and slip with respect to these frequencies is essentially unity as if the rotor were at a standstill. So, for the high frequency injection, the r_2/S will be r_2 and also L_M is very large and practically open. At very low frequency — near mechanical rotational frequency — the slip varies with change of perturbation frequency, but then the converter is at its low frequency flat region where variation of the load is not very important. The loop is usually closed at high frequencies and except for radical changes, the low frequency behavior of the motor does not affect the stability of the loop. Therefore, for frequency response calculation purposes, the equivalent circuit of Fig. 13.4a simplifies to that of Fig. 13.4b, where frequency dependence of the resistance shown is ignored according to the preceding discussion.

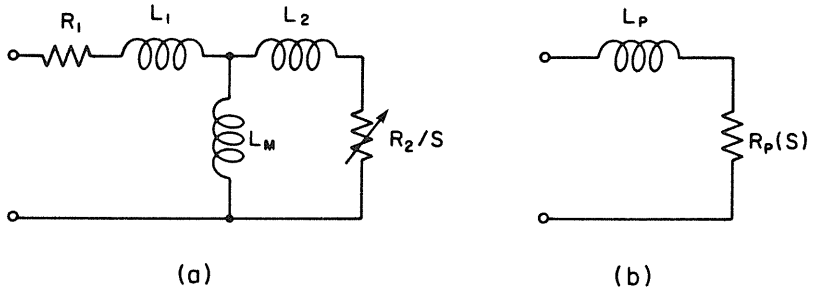


Fig. 13.4 (a) Steady-state model for one phase of an inductor motor. (b) Simplified version for modelling purposes.

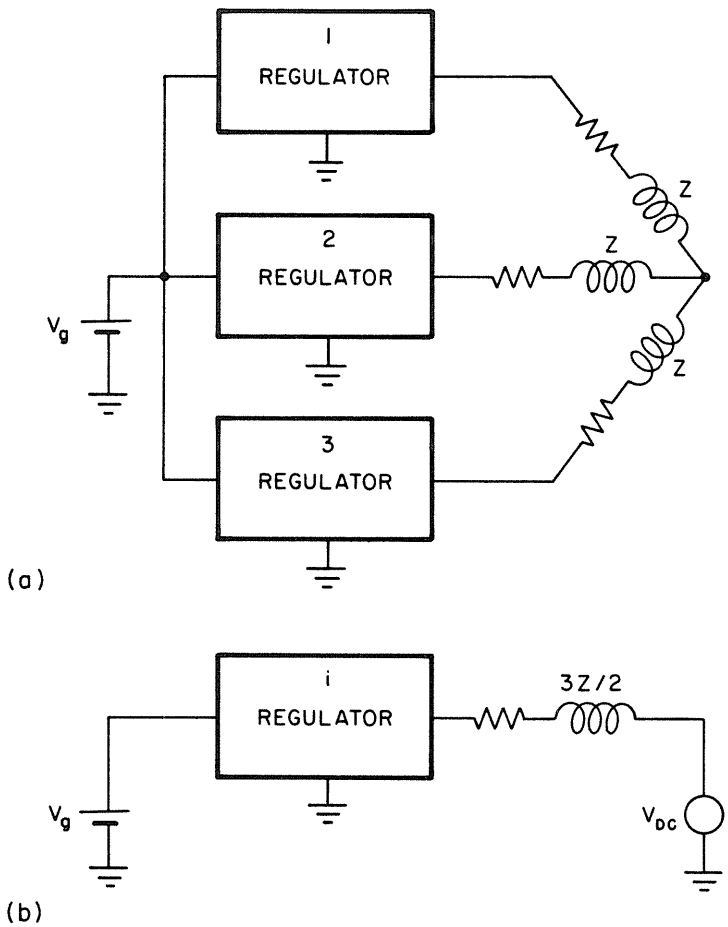


Fig. 13.5 (a) Model of the amplifier and the motor. (b) Simplified model for one phase.

The simplified model is employed in the closed-loop amplifier of Fig. 13.3 to obtain the form shown in Fig. 13.5a. The separation of the converters starts when it is assumed that two stages of the polyphase amplifier, for example stages 2 and 3, already contain a feedback loop and stage number 1 does not. A reasonable voltage feedback on stages 2 and 3 ensures very low output impedance for those stages, and for design purposes, the output impedances are ignored (small compared with the load impedances). The feedback design then simplifies to analysis and closing the loop around the converter of Fig. 13.5b. After the design is finished, one must check the validity of the initial assumption of negligible output impedances and do the necessary readjustments in case of a mismatch. Figure 13.6 shows implementation of Fig. 13.5b on one converter where $L_e = 3/2\ L_p$ and $R_e = 3/2\ R_p$. The other converters are assumed regulated. The voltage source is to model the dc generated by the other stages at their quiescent operating point D = 0.5. It simulates correct steady-state conditions.

Open-loop characteristics for the circuit of Fig. 13.6 can be found by use of the state-space averaging technique which after necessary manipulation results in the duty ratio-to-output transfer function of Eq. (13.1)

$$\frac{\hat{v}}{\hat{d}} = \frac{1 + \frac{L_e}{R_e} s}{1 + \frac{L_e + L}{R_e} s + LCs^2 + \frac{L_e}{R_e} LCs^3} \qquad (13.1)$$

R_e is small and thus the circuit is essentially a resonant network

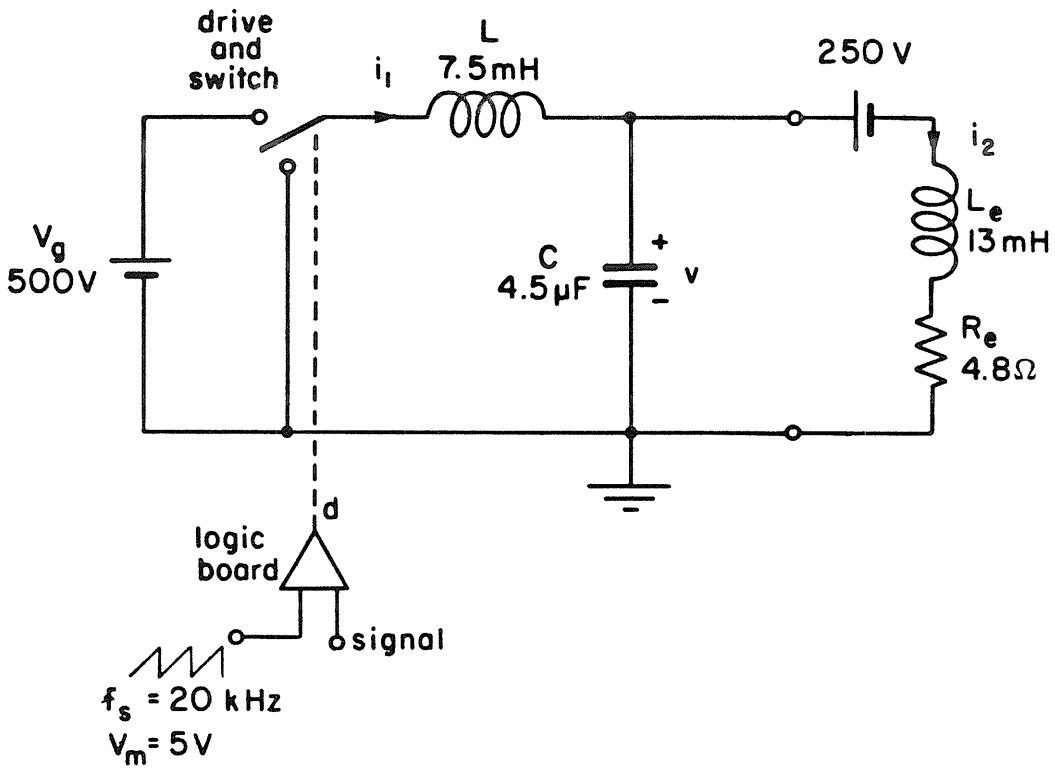


Fig. 13.6 Open-loop model of one stage with the other stages regulated.

consisting of C and parallel combination of L and L_e. For small values of R_e the denominator can be analytically approximated into two factors as

$$\frac{\hat{y}}{\hat{d}} \simeq \frac{1 + \frac{L_e}{R_e} s}{\left(1 + \frac{L_e + L}{R_e} s\right)\left[1 + \left(\frac{L}{L + L_e}\right)^2 R_e C s + \left(L_e \,||\, L\right) C s^2\right]} \tag{13.2}$$

provided that $R_e^2 << (L + L_e)^3/L^2C$. This shows a pole and a zero at low frequency which are close together and a pair of high-frequency poles. The Q of these poles is high with low R_e values, which is actually the case, and this high Q resonant circuit causes rapid phase shift in the control transfer function, making the loop design more difficult.

In order to improve the conditions, one may damp the power stage [15] by use of a series combination of a resistor and a capacitor in parallel with the load to essentially smooth out the open-loop frequency characteristics of the converter. As in the case of the original power amplifier, in order to have a high bandwidth, highly efficient circuit, the damping network must be calculated very differently from those designed for dc-to-dc converters. Owing to wide regular changes in voltage levels, a damping circuit not carefully designed can dissipate too much power as well as significantly reduce the power bandwidth of the converter. The design becomes a compromise between the amount of damping and bandwidth reduction and losses. This suggests a small value for the damping capacitor. In order to use the results of [15], R_e is approximated to be zero. Then, the circuit as mentioned earlier converts

to a normal LC filter with the value of $L \,||\, L_e$ for the inductor. The damping resistor and capacitor are denoted by R_d and C_d respectively. The damping capacitor value was selected to be of approximately the same value as the converter capacitor (C_d = 4 μF).

$$n = \frac{C_d}{C} = \frac{4\mu}{4.5\mu} = 0.89$$

and

$$R_d = R_0 \sqrt{\frac{(1 + n)(2 + n)}{2n^2}} \quad , \quad R_0 = \sqrt{\frac{L \,||\, L_e}{C}} \tag{13.3}$$

The circuit is not a pure LC network and a numerical trial and error value for the R_d was found to be about 50 ohms (there is no single solution and lower values of R_d are preferred). At maximum frequency of 60 Hz and 120 V ac operation there will be almost 1.6 watts loss for each damping circuit (4.8 watts total). Introduction of this damping network reduces the Q of the resonant circuit from a theoretical value of 48 to 2.5, which is much more acceptable for loop closure.

With the converter damped, the loop can be closed in several ways. The one selected is the simplest, having a lead-lag network to shape the loop gain and improve the phase margin. No dc is allowed on ac loads, especially for motors where the load is mostly inductive and the resistance is parasitic and by design kept low. Any dc on the motor causes a stationary field to be created inside the motor which, when added to the desired rotating magnetic field, creates a variable torque. Depending on the size of the dc component, it may even cause

severe mechanical shaking, dc losses and, finally, possible saturation of the motor. To avoid this, dc levels of the outputs must be kept exactly the same. This makes the use of an integrator type compensation very desirable. It must be noted that many motor drives produce this torque pulsation either inherently (non-sinusoidal fields) or due to open-loop operation of mismatched switching circuits.

Figure 13.7 shows the complete feedback circuitry for one phase of the power amplifier. Damping is done by R_d and C_d and the single-loop feedback consists of R_3, R_4, and C_4 forming a lead-lag network where C_2 is the integrating capacitor ensuring negligible dc error. With the numerical values shown in Fig. 13.7, one can evaluate the loop gain of the circuit as shown by the thick lines on Fig. 13.8; the thin lines are the results of computer-controlled measurement taken from the actual amplifier. The good agreement between the two graphs confirms the accuracy of the analysis. Small deviation around the resonant frequency is due to variation of parameters of the system and can actually be verified to vanish with more accurate characterization of the components. One may also notice that the practical circuit, owing to the ESR of the output capacitor and various other losses, exhibits an improved phase at high frequencies such that higher loop gains are obtainable. However, the output is quite satisfactory and there is no need for further increase of the loop gain. The output dc level is tightly regulated to the dc level of the reference voltage. That is, the input reference voltages must be exactly a replica of the outputs. To do this, the outputs of the three-phase sine generators

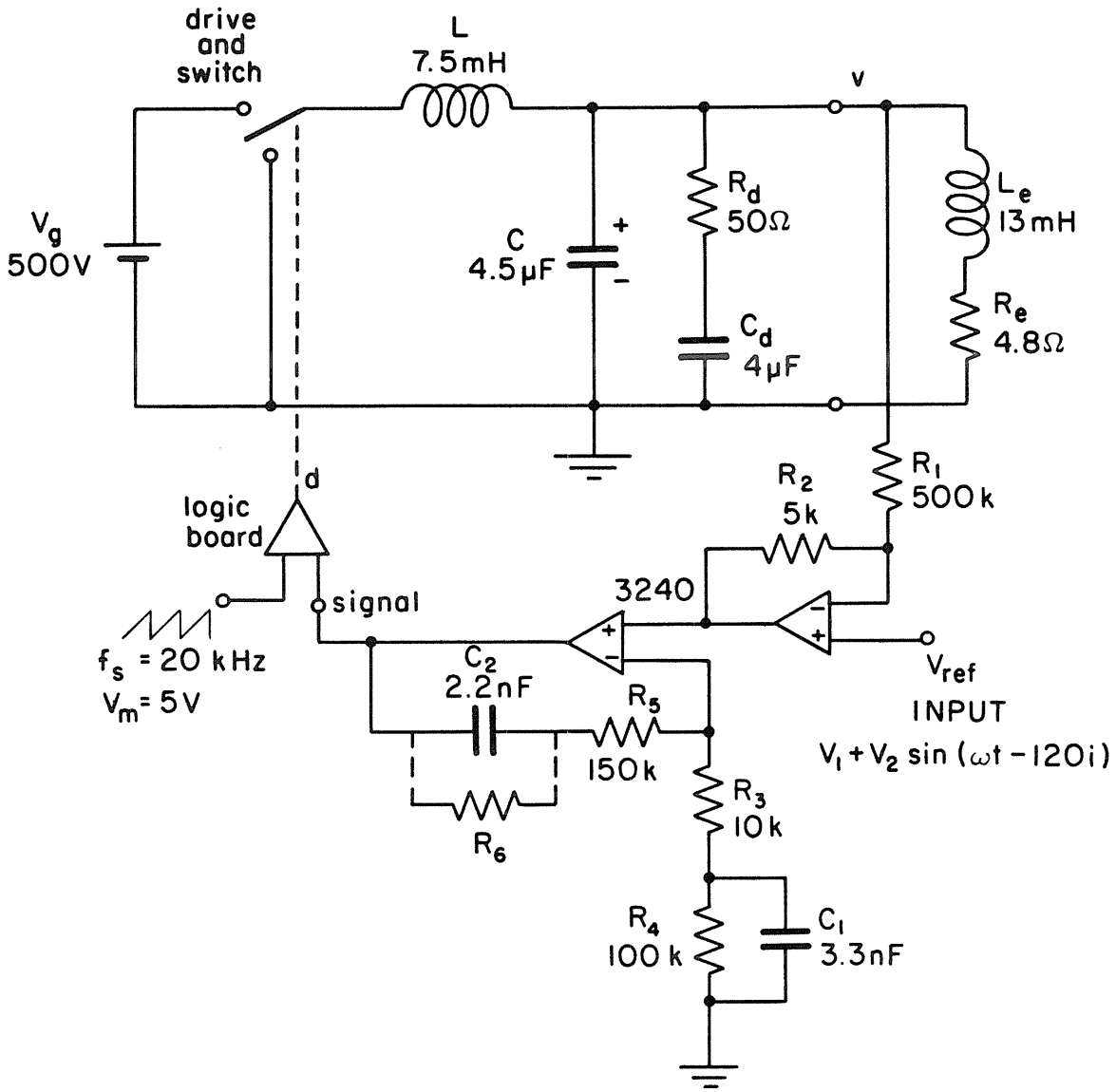


Fig. 13.7 Complete closed-loop schematic of one phase of the amplifier.

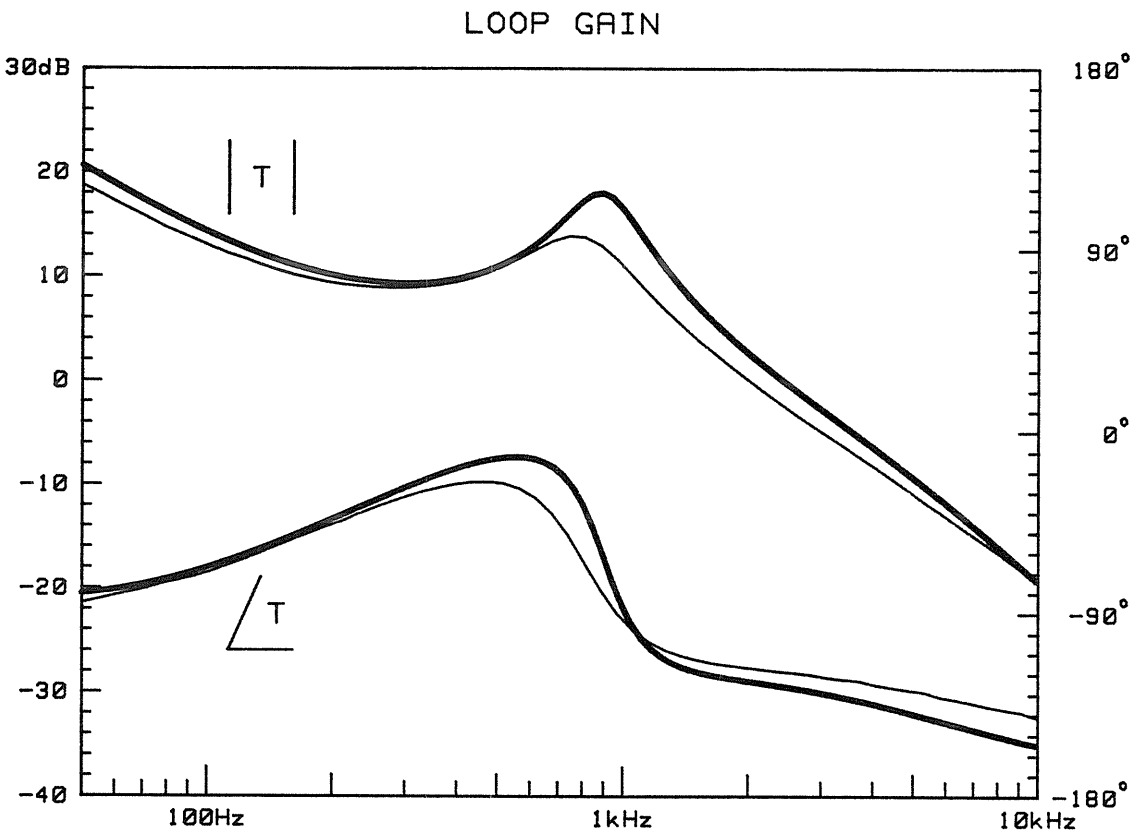


Fig. 13.8 *Comparison of theoretical prediction (thick lines) and practical measurement (thin lines) of the loop gain of one converter.*

as mentioned in Section 13.1 ought to be added to a dc level which sets the output dc levels. This initial design has been performed around the quiescent operating point. It must be checked for other operating conditions. However, since the dynamic of the buck converter is independent of the operating point, no further modifications are necessary. One must return to check the initial assumptions of non-interaction. The verification may be done in many ways, one of which is to find a condition for compensation gain, $H(s) = \hat{d}/\hat{v}$ (Fig. 13.7). It is started with the actual loop gain, T, and the approximated loop gain by the assumption of negligible output impedance for other stages, T_∞. The condition to satisfy is to show that T and T_∞ are almost the same. That is, if

$$\frac{T}{T_\infty} = 1 + \varepsilon(s) \tag{13.4}$$

then $|\varepsilon(s)| << 1$. This ensures minor modification of the real loop gain. From Eq. (13.4), one can work backward to find ε which is related to H(s). By setting $|\varepsilon| << 1$, a constraint for H(s) is found.

Start with the linearized equivalent circuit model for any dc-to-dc converter. The output can be represented by a Thevenin equivalent circuit which consists of a duty ratio-dependent voltage source $V_0(s)$ and an output impedance Z_0 (all open-loop). If the load impedance is denoted by Z_L, then if $G(s) = \hat{v}/\hat{d}$ and $A(s) = \hat{v}_0/\hat{d}$

$$G(s) = A(s) \frac{Z_L}{Z_0 + Z_L} \tag{13.5}$$

A(s) can be viewed as the *no load* duty ratio-to-output gain of the converter. The load as can be seen in Fig. 13.9 is

$$Z_L = \frac{3}{2} Z_p + \frac{1}{2} \frac{Z_0}{1 + T} \tag{13.6}$$

and $T(s) = G(s)\, H(s)$. The equation for $T_\infty(s) = G_\infty(s)\, H(s)$ assumes large loop gain such that $T \to \infty$. Then

$$G_\infty(s) = A(s) \frac{\frac{3}{2} Z_p}{Z_0 + \frac{3}{2} Z_p} \tag{13.7}$$

and

$$G(s) = A(s) \frac{\frac{3}{2} Z_p + \frac{1}{2} \frac{Z_0}{1 + T}}{Z_0 + \frac{3}{2} Z_p + \frac{1}{2} \frac{Z_0}{1 + T}} \tag{13.8}$$

Now find ε

$$\varepsilon = \frac{T}{T_\infty} - 1 = \frac{G}{G_\infty} - 1 \tag{13.9}$$

With substitution of Eqs. (13.7) and (13.8) and the definition $\alpha \equiv Z_p/Z_0$, Eq. (13.9) reduces to

$$\varepsilon = \frac{2}{3\alpha[(3\alpha + 2)(1 + T) + 1]} \tag{13.10}$$

Find T = GH from Eq. (13.10) and by a few approximations get

$$H \simeq \frac{2}{9A\alpha^2\varepsilon} \tag{13.11}$$

or, since $\varepsilon << 1$,

$$H >> \frac{2}{9A\alpha^2} \tag{13.12}$$

substitution of actual expressions for the various terms in Eq. (13.12) gives the condition to be:

$$\frac{R_2}{V_m R_1} \frac{1 + [(R_3 + R_4 + R_5)C_2 + R_4C_1]s + (R_3 + R_5)R_4C_1C_2s^2}{(R_3 + R_4)C_2s + R_3R_4C_1C_2s^2} >>$$

$$>> \frac{2}{9V_g} \frac{\left(\frac{L}{R_p}s\right)^2}{\left(1 + \frac{L_p}{R_p}s\right)^2} \frac{1 + R_dC_ds}{1 + R_dC_ds + L(C + C_d)s^2 + LCR_dC_ds^3} \tag{13.13}$$

If one draws Bode plots of the magnitudes of both sides of Eq. (13.13) as shown in Fig. 13.10, it is seen that the condition is satisfied and the original assumption is indeed correct. In fact, numerical simulation of the complete motor drive shows that T and T_∞ are not more than 0.3 dB apart and cannot be distinguished if plotted on Fig. 13.8. Figure 13.11 shows the oscillograms of the output voltage and current of one phase of the power amplifier. The 20 Hz output, shown in Fig. 13.11a, causes the

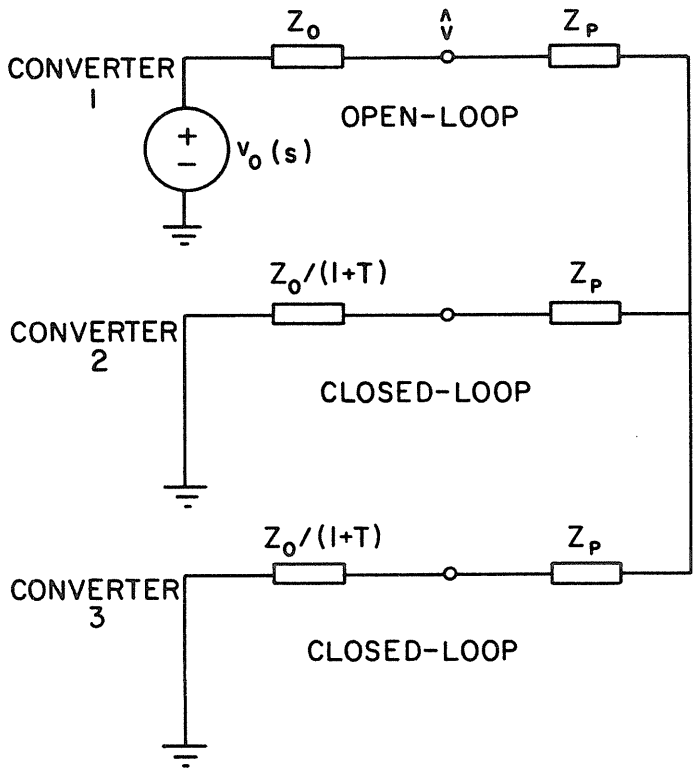


Fig. 13.9 *Load impedance for one converter with the other converters regulated.*

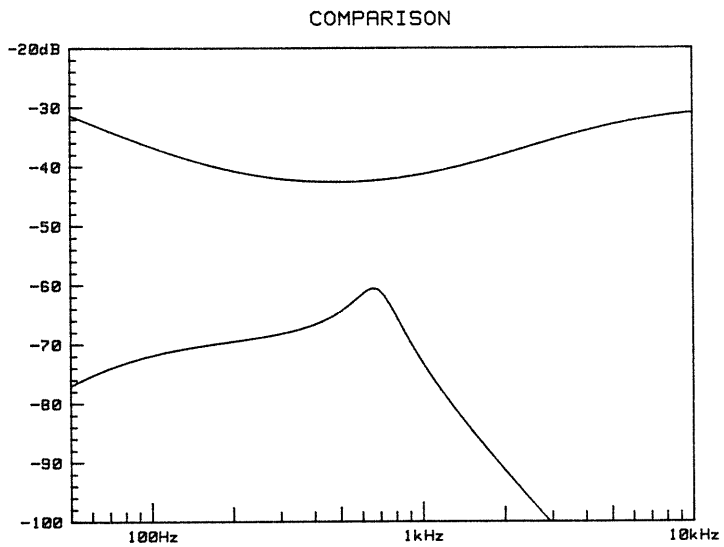


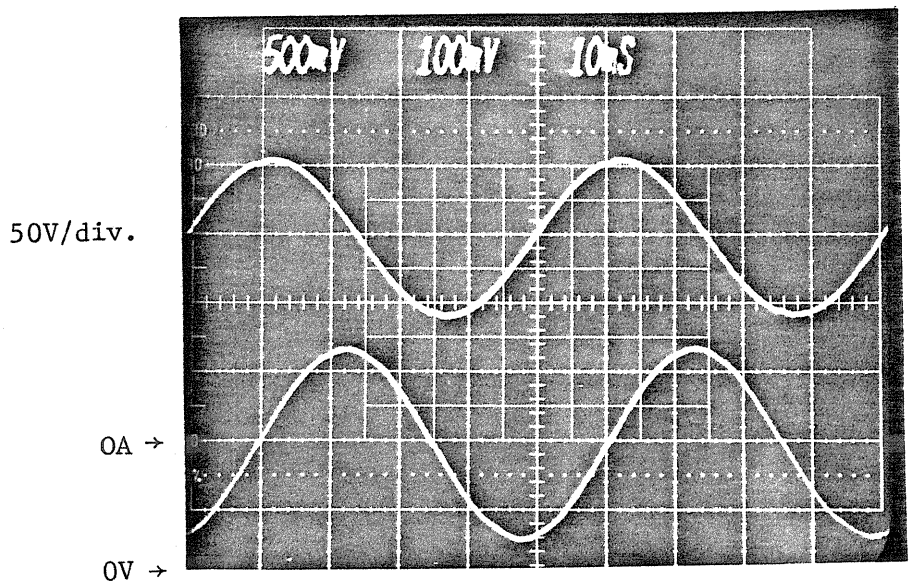
Fig. 13.10 *Comparison of the two sides of Equation (13.13). Upper graph is the magnitude of* $H(s)$ *and the lower one is for* $2/9\alpha^2 A$.

motor to rotate at about a third of its normal speed ($\simeq$ 600 RPM) and Fig. 13.11b shows the case of 60 Hz output with 0.8 hp mechanical load on the motor. The voltages and currents are almost pure sinusoids, which relieves the motor from absorbing extra harmonic currents; thus harmonic overheating problems are prevented. Having the electrical feedback completed, one may add larger and slower loops around the entire system to control position, torque, or speed of the motor.

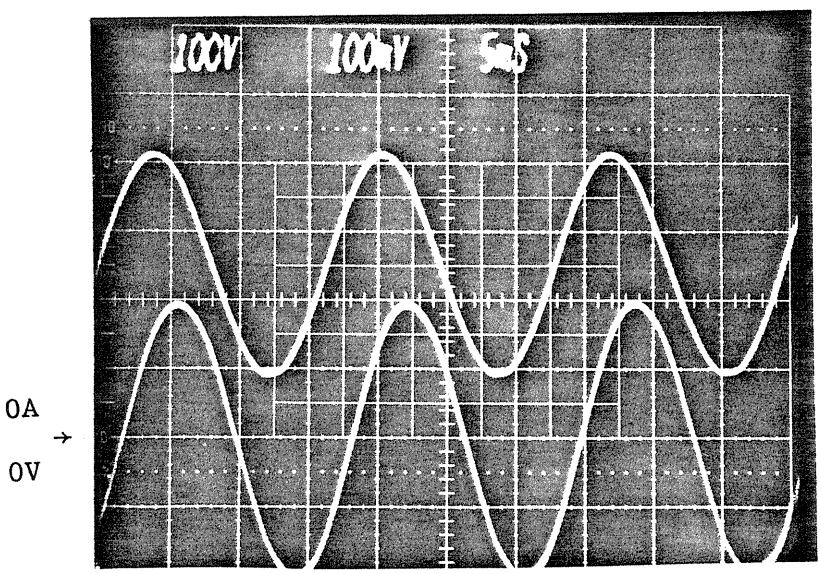
13.3 Review

An experimental variable-speed induction motor drive was constructed comprising three bidirectional buck converters. The drive provides variable-voltage variable-frequency polyphase power required by the motor for high performance and efficient operation. The voltage and frequency can be independently controlled, but in order to keep the air gap flux constant, the ratio of voltage to frequency is held almost constant (no speed regulation loop).

The drive was built with cascode type switches for reliable operation, in which a low-voltage transistor is used to turn a high-voltage transistor off. The regulation of the output voltages was extensively covered, whereby use of an integrator the possibility of dc on the load is eliminated. First, the motor model was simplified to a series connection of a resistor and an inductor. The complete system, owing to differential connection of the load to the converters outputs, constitutes an interacting multiple-input multiple-output system.



(a)



(b)

Fig. 13.11 *Current and line-to-ground voltage waveforms of the motor drive, (a) output at 20 Hz with no load. (b) 60 Hz operation with more than 0.8 hp mechanical load. Current scales: 2A/div.*

However, the interaction is weak and design of the feedback is performed with the assumption of noninteraction. Three separate converters were analyzed, and after damping the converters feedback loops were designed. In the general case these designs must be checked against variations imposed upon the system at various operating conditions. The buck converters, however, are exempt since their dynamic is fixed.

Finally after the design is completed the noninteraction assumption is checked. It was shown that even the small amount of feedback was enough to very well satisfy the noninteraction condition.

In addition to the electronic feedback, one may put a speed control loop around the total system consisting of the motor and the drive.

CHAPTER 14

OTHER APPLICATIONS

Applications for the polyphase power amplifier are not limited to motor drives. Owing to its high quality sinusoidal output voltages, the amplifier has an excellent potential for three-phase line applications as extensions of the single-phase amplifier.

For example, consider a typical ac uninterruptible power supply (UPS) as shown in Fig. 14.1. The battery charger converts the ac line power to dc to charge the battery bank which is the storage medium. Then, the dc power is converted to three-phase sine waves by the inverter. In case of a power failure, the incoming flow of power to the battery bank is removed, but the stored energy will keep the inverter and the load running; thus, the power flow to the load is uninterrupted. The inverter part of this UPS is a very good application for the new power amplifier which is capable of producing high quality sine waves with low harmonic content. In cases where the power lines are very noisy, this technique may be used to filter the line, since the battery essentially separates the load from the ac line.

It can be easily seen from Fig. 12.4 that the polyphase amplifier is a four-quadrant converter and its bidirectionality allows polarity reversal of both currents and voltages. Furthermore, the reversal of signs for the voltage and the current are also independent of each other,

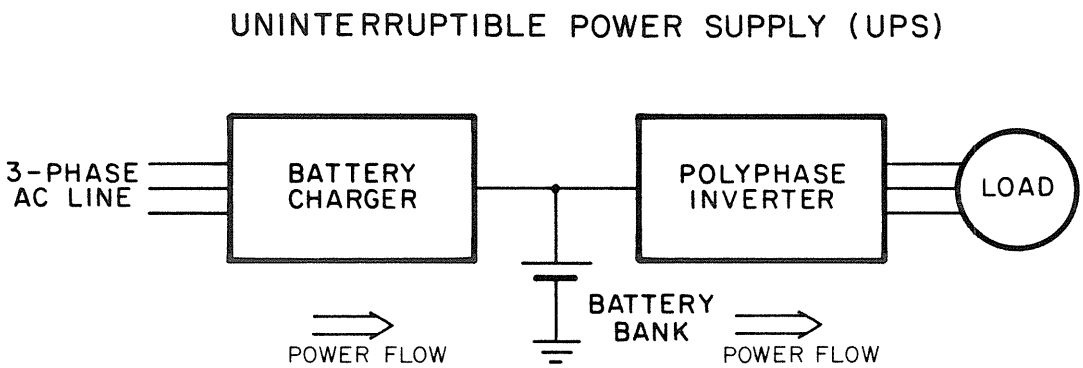


Fig. 14.1 A three-phase uninterruptible power supply utilizing a polyphase amplifier.

which enables the power flow to be in either direction: from dc to ac or vice versa. Non-unity power factor loads, such as the motor in Chapter 13 draw currents which are not necessarily of the same polarity as the voltage. So in portions of the ac cycle, the power is returned back to the amplifier. In this type of dc to ac generation, the average power is flowing to the load. The reverse mode is generation of dc from ac power. If the ac side is connected to a motor which is mechanically driven, by making the slip of the operation negative, one can make the net average power flow from the ac to the dc side. This feature is known as regenerative braking, which returns the mechanical energy stored in the inertia of the load back to the battery. A particular use for this feature is in electric vehicles where not only is energy saved but the mechanical brakes are relieved from heavy duty work.

It should be emphasized that since the voltages and currents of the amplifier can be controlled independently, the amplifier is capable of bidirectional power flow. Controlled rectification is a promising application of this feature. That is, if the ac side is connected to the three-phase ac line as illustrated in Fig. 14.2, the power flows from the line to the battery and charges it. The major advantage of this ac-to-dc converter is that unlike the simple bridge rectifiers, the line currents can be controlled to be of a desired shape, namely sinusoidal [22].

The control loops of Fig. 14.2 illustrate the technique. There are three separate current control loops in the system which control the output currents and make them proportional to the corresponding

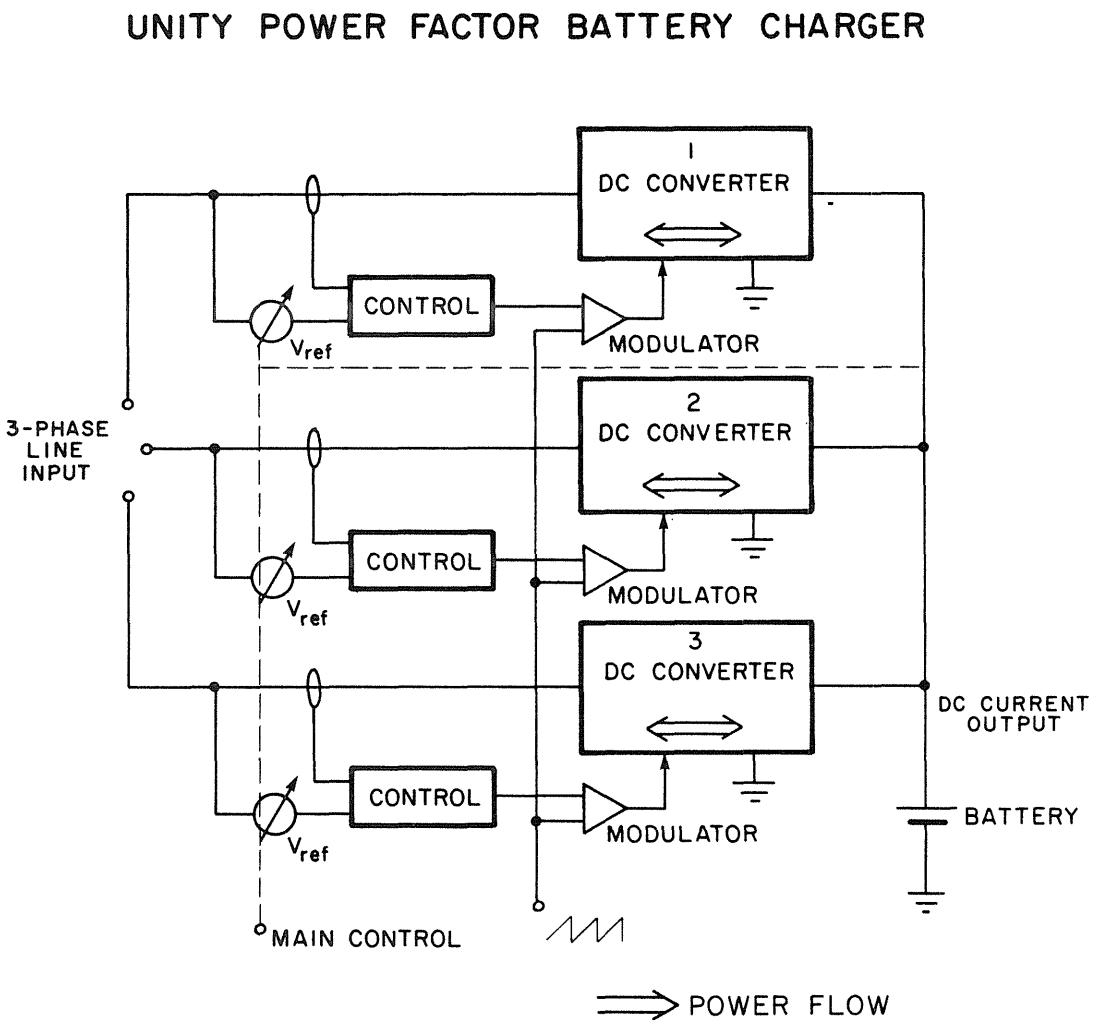


Fig. 14.2 A unity power factor battery charger.

reference voltages. If as shown in Fig. 14.2, the reference voltages are connected to the line voltages, the current and voltage of each phase are proportional, sinusoidal and in phase with each other. Now the circuit is a unity power factor battery charger. The amount of charging current can be controlled by varying the amplitude of the reference voltage with a multiplier.

If one uses a phase shifter between each line voltage and reference voltage, the currents can be phase-shifted with respect to the voltages and therefore the power factor can be varied. The power factor can thus be adjusted to compensate for the non-unity power factor of other loads, to result in a total system with unity power factor. If the phase shift is set at -90^0, the net power through the system is zero and it becomes an "electronic variable polyphase capacitor" useful for power factor correction purposes. The phase shift may further increase to 180^0, where the power flows from the battery to three-phase line interface capable of working in either direction.

For applications in which the power is generated from sources such as solar cell arrays or other dc sources, the amplifier may be used as an interface between the dc and the ac lines. Thus, in an installation which uses solar cells as an alternative power source, this technique allows the sale of unused energy back to the power company.

Application of bidirectional power flow can considerably simplify the conventional UPS of Fig. 14.1 to that of Fig. 14.3. In this form [22], only one polyphase amplifier is used. As long as the ac line is up, the switches are closed and the line powers the load. The control

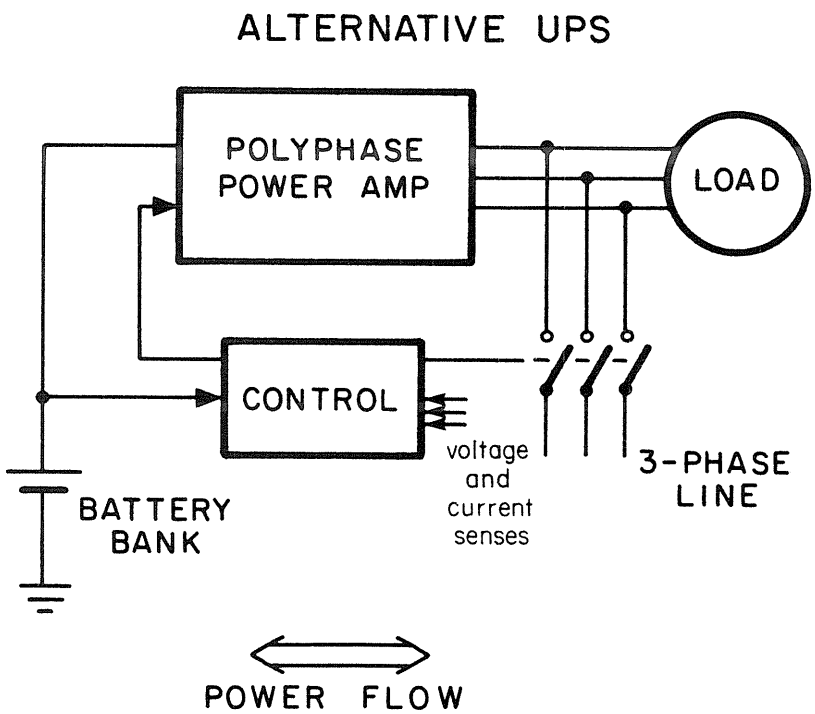


Fig. 14.3 *Alternative three-phase UPS comprising only one polyphase power amplifier.*

circuitry monitors the line and converts the amplifier to a unity power factor battery charger. It charges the batteries to a preset level and then the charging current is reduced to a low level. In case of a power failure, the control circuit opens the switches and converts the amplifier to a dc-to-ac inverter similar to Fig. 12.4 which powers the load from the battery for continuous operation. At the time when the line power is restored, after the phase matching procedure, the switches are closed and the circuit is converted back to a battery charger to replenish the lost energy of the battery. This technique simplifies the power processing part to a single unit as opposed to two in Fig. 14.1, so that the overall system is simpler, more efficient, more reliable, and more economical.

The battery in Fig. 14.1 may be replaced by a parallel combination of a load and a capacitor. However, analysis of this system, owing to the high degree of interaction of the states is considerably complicated. Nevertheless, (unlike the single-phase version) since the input currents as well as voltages constitute a three-phase system, the instantaneous input power is constant. Thus the current supplied to the dc load is also dc, which eliminates the need for very large capacitors. The capacitor must be only large enough to absorb the switching frequency ripple current and the load transients. In the simple rectifier circuit, the input power (current) is pulsating requiring a large capacitor to hold the energy for a fraction of a line period. The load can be another polyphase amplifier and the combination is a three-phase to three-phase converter, with applications in motor drives and line

filters, In the latter case, the input and output voltages are isolated from each other by the dc link in such a way that a disturbance in one side does not propagate to the other side. Other applications for this converter are in variable-frequency to constant-frequency operations. This is very useful in cases such as wind and dam generators where the unregulated input must be interfaced to the line network.

CHAPTER 15

CONCLUSION

High power applications mostly utilize polyphase systems for their economy of production and distribution as well as many other advantages. There are many ways to electronically produce polyphase power. It was shown that the brute-force way to produce polyphase power using many single-phase push-pull power amplifiers is not an efficient use of components and has only limited applications. The problem is approached from a different angle by generalization of the original push-pull amplifier. Instead of a single modulator, two are used to make the two constituent converters of the amplifier completely independent. This additional degree of freedom allows the amplifier to have an arbitrary quiescent operating point rather than operation around the duty ratio of 0.5 imposed by the use of a single modulator. Also, for the same reason, the ac components of the outputs do not need to have 180^0 phase shift but can have any phase relations.

A new polyphase switching power amplifier is then introduced by addition of a third bidirectional dc-to-dc converter to this amplifier. Therefore, the three-phase sine amplifier is comprised of three current-bidirectional dc-to-dc converters with their own individual modulators, where the three-phase load is connected differentially across the outputs. At quiescent operating points, all the outputs

have the same dc voltage. Applying a set of three-phase sine waves to the modulator inputs produces ac components on the outputs. A three-phase ac is generated on the load, while the equal dc output voltages are cancelled automatically. The technique produces clean output voltages with considerably fewer components than the brute-force method.

All the advances made in the area of dc converters are directly applicable to this amplifier — the analysis of the circuit becomes a refinement of existing methods rather than a search for new ones. Galvanic isolation of input and output can be obtained by the use of isolated versions of the converters. The transformers then operate at high frequencies and bulky 60 Hz transformers are eliminated. Also, the same transformers can be used to boost the voltage (in addition to inherent boosting capability of some converters) to power a high voltage load from a low voltage source. In order to increase the output power, the polyphase power amplifiers can be paralleled.

Feasibility of the idea was demonstrated by a 1 hp three-phase variable-speed motor drive employing the sine amplifier. High performance motor operation requires variable-amplitude variable-frequency voltages which are easily generated by the amplifier. The clean sinusoidal voltages eliminate torque pulsation and harmonic heating and some other problems encountered with ordinary motor drives. Switching at 20 kHz, the amplifier employs three bidirectional buck converters to drive a 4 pole induction motor. The power switches are realized by a cascode technique, in which a low voltage transistor is used to open

the emitter of a high voltage transistor for a fast turn-off process. Unlike in ordinary motor drives, the output voltages are electronically regulated to reduce the sensitivity of the drive to variations of the line, load, and various other parameters of the system. Owing to interaction of the converters via the differential three-phase load, special attention must be paid to design the fast feedback loops around the converters.

Smooth, controllable output voltages make this amplifier suitable for many line applications. Independent bidirectionality of currents and voltages allows reversal of the power flow to create dc-to-ac or ac-to-dc conversion capability. The proper control of currents can even provide unity power factor ac-to-dc conversion. The long list of applications for the polyphase power amplifier includes: Single-stage uninterruptible power supplies, unity power factor battery chargers, electronic capacitors, battery to three-phase line interfaces, and many others.

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APPENDIX

Listing of the Switching Converter Analysis Program (SCAP)

This listing of the Switching Converter Analysis Program is written in Basic 1.0 for the HP9826 computer. Each subroutine includes comments to clarify its function. The data file, when called, is automatically inserted in the program starting at line 20000.

Three subprograms, Decomp, Solve, and Siljak are slightly modified versions of those in the HP98821A BASIC Numerical Analysis Library. The library is copyrighted by the Hewlett-Packard Company and the above named subprograms' listings are included with their permission.

```
10   !
20   !   Switching Converter Analysis Program
30   !
40   !
50   !
60   !              Farhad Barzegar
70   !
80   !       Version 2.6    Dec. 12, 1982
90   !
100  !
110  !
120  ! This program calculates the transfer
130  ! function coefficients of a switching
140  ! converter and then evaluates the frequency
150  ! response by use of complex arithmetic.
160  !
170  !
180  ! PROGRAM Main
190  OPTION BASE 1
200  COM /Mem/ Yy(10,400),Title$(5)[40]
210  COM /Coeff/ A(15,16),B(16)
220  COM /A/ N,M,L,D,Loop,Mm,Nc,Nf
230  COM /B/ Fmin,Fmax,Nn,Count(5)
240  COM /C/ INTEGER Plt,Graph,Offset(5,0:1)
250  COM /D/ Aa(15,15),Ad(15,15),Ba(15,6),Bd(15,6)
260  COM /D/ Ca(5,15),Cd(5,15),E(5,6),X(15),U(6)
270  COM /D/ F(15),G(15)
280  COM /Alt/ Alt,Err
290  INTEGER Prt,I
300  !
310 Init: !
320  PRINTER IS 1
330  GRAPHICS OFF
340  ALPHA ON
350  Plt=705      ! HP9872 PLOTTER
360  Prt=702      ! HP2671 PRINTER
370  DUMP DEVICE IS Prt
380  !
390  DEG
400  ON KEY 0 LABEL "OPEN_LP" RECOVER Start
410  ON KEY 10 RECOVER Repeat
420  ON KEY 1 LABEL "CLOSE_LP" RECOVER Close
430  ON KEY 11 RECOVER Open
440  ON KEY 2 LABEL "LoopGain" RECOVER Loopgain
450  ON KEY 3 LABEL "Data_In" RECOVER Diskin
460  ON KEY 4 LABEL "DataFile" RECOVER Restart
470  ON KEY 14 GOTO Data
480  PRINT FNPage$
490  PRINT FNLin$(8),TAB(7),"SWITCHING CONVERTER ANALYSIS PROGRAM",FNLin$(5)
500  IF FNMem(Out) THEN Output
510 Idle: GOTO Idle
520  !
530 Data: OUTPUT 2;"%P%#EDIT 20000%X";
540       GOTO Idle
550  !
560 Restart: PRINT FNPage$
570  PRINT FNLin$(8),TAB(7),"SWITCHING CONVERTER ANALYSIS PROGRAM",FNLin$(8)
580  Edit("Enter the name of the data file",File$)
590  ON ERROR GOTO Dataerror
600  ASSIGN @P TO File$
610  ASSIGN @P TO *
620  OFF ERROR
630  GET File$,20000,640
640  Alt=0
650  Err=0
660  GOTO Init
```

```
670  !
680 Dataerror:  !
690  BEEP
700  PRINT "PROBLEM IN LOADING THE ";File$
710  WAIT 2
720  GOTO Init
730  !
740 Start:Loop=0
750  GOTO 820
760 Open:Loop=1
770  GOTO 820
780 Close: Loop=2
790  GOTO 820
800 Loopgain: Loop=3
810  !
820  CALL Read_data(Title$(*))
830  !
840  ! All matrices averaged.
850  !
860  CALL Transfer
870  !
880  CALL Print_trans(Prt,Title$(*))
890  !
900  CALL Polezero(Prt,Title$(*))
910  !
920 Repeat:  CALL Response
930  GOTO Output
940  !
950 Diskin:  CALL Measure_in
960  !
970  ! output routines
980  !
990 Output:  GRAPHICS OFF
1000 IF FNMem(Out)=0 THEN Idle
1010 PRINT FNLin$(2);"Memory contains the following data:";FNLin$(1)
1020 FOR I=1 TO 5
1030  IF Count(I) THEN PRINT "#"&VAL$(I)&": "&Title$(I)
1040 NEXT I
1050 PRINT FNLin$(2)
1060 DISP "Use the soft keys"
1070 ON KEY 5 LABEL " PRINT" GOTO Print
1080 ON KEY 15 GOTO Prt_print
1090 ON KEY 6 LABEL "  PLOT" GOTO Plot
1100 ON KEY 16 GOTO Plt_plot
1110 ON KEY 7 LABEL "OVER_LAY" GOTO Over
1120 ON KEY 17 GOTO Erase
1130 OFF KEY 9
1140 IF Err>1.E-4 THEN
1150  IF Alt=0 THEN ON KEY 9 LABEL "ACCURATE" GOTO Accu
1160  IF Alt=1 THEN ON KEY 9 LABEL "STANDARD" GOTO Stan
1170  END IF
1180 GOTO Idle
1190 !
1200 Stan: Alt=0
1210 GOTO Output
1220 Accu: Alt=1
1230 GOTO Output
1240 !
1250 Prt_print: PRINTER IS Prt
1260 Print: GRAPHICS OFF   ! print on CRT
1270 IF FNMem(Out)>1 THEN INPUT "Enter the output number",Out
1280 IF FNCheck(Out) THEN CALL Print(Out,Yy(*),Title$(Out))
1290 GOTO Output
1300 !
1310 Erase: GRAPHICS OFF   ! CRT eraser
```

```
1320 IF Graph<>1 THEN Output
1330 CALL Bode_plot(Out,3,Yy(*),Title$(Out))
1340 GOTO Output
1350 !
1360 Over: GRAPHICS OFF    ! overlay
1370 IF FNMem(Out)>1 THEN INPUT "Enter the overlay output number",Out
1380 IF FNCheck(Out) THEN CALL Bode_plot(Out,2,Yy(*),Title$(Out))
1390 GOTO Output
1400 !
1410 Plt_plot: Graph=2     ! plot on plotter
1420 GOTO 1440
1430 Plot: Graph=1         ! plot on CRT
1440 GRAPHICS OFF
1450 IF FNMem(Out)>1 THEN INPUT "Enter the output number",Out
1460 IF FNCheck(Out) THEN CALL Bode_plot(Out,1,Yy(*),Title$(Out))
1470 GOTO Output
1480 !
1490 END
1500 !
1510 !
1520 DEF FNCheck(Out)
1530 COM /B/ Fmin,Fmax,Nn,Count(*)
1540 IF Out>0 AND Out<6 THEN
1550  IF Count(Out) THEN
1560   RETURN 1    ! Out is valid
1570  END IF
1580 END IF
1590 BEEP
1600 DISP "NON-EXISTING OUTPUT !"
1610 WAIT 2
1620 RETURN 0     ! Out is invalid
1630 FNEND
1640 !
1650 DEF FNMem(Out)
1660 COM /B/ Fmin,Fmax,Nn,Count(*)
1670 J=0
1680 FOR I=1 TO 5
1690  IF Count(I)=0 THEN 1720
1700  J=J+1
1710  K=I
1720 NEXT I
1730 IF J=1 THEN Out=K
1740 RETURN J     ! Returns number of the outputs
1750 FNEND
1760 !
1770 SUB Mm_mul(A(*),B(*),C(*),N,M,L)
1780 INTEGER I,J,K
1790 FOR I=1 TO N
1800  FOR K=1 TO L
1810   C(I,K)=0.
1820   FOR J=1 TO M
1830    C(I,K)=C(I,K)+A(I,J)*B(J,K)
1840   NEXT J
1850  NEXT K
1860 NEXT I
1870 SUBEND
1880 !
1890 SUB Mv_mul(A(*),B(*),C(*),N,M)
1900 INTEGER I,J
1910 FOR I=1 TO N
1920  C(I)=0.
1930  FOR J=1 TO M
1940   C(I)=C(I)+A(I,J)*B(J)
1950  NEXT J
1960 NEXT I
1970 SUBEND
```

```
1980 !
1990 SUB Mm_add(A(*),B(*),C(*),N,M)
2000 INTEGER I,J
2010 FOR I=1 TO N
2020  FOR J=1 TO M
2030   C(I,J)=A(I,J)+B(I,J)
2040  NEXT J
2050 NEXT I
2060 SUBEND
2070 !
2080 SUB Mm_sub(A(*),B(*),C(*),N,M)
2090 INTEGER I,J
2100 FOR I=1 TO N
2110  FOR J=1 TO M
2120   C(I,J)=A(I,J)-B(I,J)
2130  NEXT J
2140 NEXT I
2150 SUBEND
2160 !
2170 SUB Ms_mul(S,A(*),B(*),N,M)
2180 INTEGER I,J
2190 FOR I=1 TO N
2200  FOR J=1 TO M
2210   B(I,J)=A(I,J)*S
2220  NEXT J
2230 NEXT I
2240 SUBEND
2250 !
2260 SUB Mm_eq(A(*),B(*),N,M)
2270 INTEGER I,J
2280 FOR I=1 TO N
2290  FOR J=1 TO M
2300   B(I,J)=A(I,J)
2310  NEXT J
2320 NEXT I
2330 SUBEND
2340 !
2350 SUB Vv_eq(A(*),B(*),N)
2360 INTEGER I
2370 FOR I=1 TO N
2380  B(I)=A(I)
2390 NEXT I
2400 SUBEND
2410 !
2420 SUB Vs_mul(S,A(*),B(*),N)
2430 INTEGER I
2440 FOR I=1 TO N
2450  B(I)=A(I)*S
2460 NEXT I
2470 SUBEND
2480 !
2490 SUB Vv_add(A(*),B(*),C(*),N)
2500 INTEGER I
2510 FOR I=1 TO N
2520  C(I)=A(I)+B(I)
2530 NEXT I
2540 SUBEND
2550 !
2560 SUB Vv_sub(A(*),B(*),C(*),N)
2570 INTEGER I
2580 FOR I=1 TO N
2590  C(I)=A(I)-B(I)
2600 NEXT I
2610 SUBEND
2620 !
```

```
2630 SUB Inv(N,A(*),Ainv(*),Det)
2640 !
2650 ! Puts inverse of A matrix (n*n) in Ainv
2660 ! matrix.  The Det is the determinant of A.
2670 !
2680 OPTION BASE 1
2690 ALLOCATE Lu(N,N),B(N),X(N),INTEGER Ips(N)
2700 INTEGER I,J,Oops
2710 CALL Decomp(N,A(*),Lu(*),Ips(*),Oops)
2720 IF Oops THEN
2730  Det=0.
2740  SUBEXIT
2750 END IF
2760 Det=1.
2770 FOR J=1 TO N
2780  FOR I=1 TO N
2790   B(I)=0.
2800  NEXT I
2810  B(J)=1.
2820  CALL Solve(N,Lu(*),B(*),X(*),Ips(*),Oops)
2830  IF Oops THEN
2840   Det=0.
2850   SUBEXIT
2860  END IF
2870  FOR I=1 TO N
2880   Ainv(I,J)=X(I)
2890  NEXT I
2900  Det=Det*Lu(Ips(J),J)
2910 NEXT J
2920 FOR J=1 TO N-1
2930  FOR I=1 TO N-J
2940   IF Ips(I)<Ips(I+1) THEN 2990
2950   Temp=Ips(I)
2960   Ips(I)=Ips(I+1)
2970   Ips(I+1)=Temp
2980   Det=-Det
2990  NEXT I
3000 NEXT J
3010 SUBEND
3020 !
3030 DEF FNDet(N,A(*))
3040 ! finds determinant of A matrix
3050 OPTION BASE 1
3060 ALLOCATE Lu(N,N),INTEGER Ips(N)
3070 INTEGER I,J,Oops
3080 CALL Decomp(N,A(*),Lu(*),Ips(*),Oops)
3090 IF Oops THEN RETURN 0
3100 Det=1.
3110 FOR J=1 TO N
3120  Det=Det*Lu(Ips(J),J)
3130 NEXT J
3140 FOR J=1 TO N-1
3150  FOR I=1 TO N-J
3160   IF Ips(I)<Ips(I+1) THEN 3210
3170   Temp=Ips(I)
3180   Ips(I)=Ips(I+1)
3190   Ips(I+1)=Temp
3200   Det=-Det
3210  NEXT I
3220 NEXT J
3230 RETURN Det
3240 FNEND
3250 !
3260 SUB Solve(N,Lu(*),B(*),X(*),INTEGER Ips(*),Oops)
3270 !
```

```
3280 !   © Copyright (1982) Hewlett-Packard Company.
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3290 !
3300 OPTION BASE 1
3310 INTEGER I,J,Ip
3320 Oops=0
3330 Ip=Ips(1)
3340 X(1)=B(Ip)
3350 FOR I=2 TO N
3360  Ip=Ips(I)
3370  Sum=0
3380  FOR J=1 TO I-1
3390   Sum=Sum+Lu(Ip,J)*X(J)
3400  NEXT J
3410  X(I)=B(Ip)-Sum
3420 NEXT I
3430 Ip=Ips(N)
3440 IF Lu(Ip,N)<>0 THEN 3470
3450 Oops=1
3460 SUBEXIT
3470 X(N)=X(N)/Lu(Ip,N)
3480 FOR I=N-1 TO 1 STEP -1
3490  Ip=Ips(I)
3500  Sum=0
3510  FOR J=I+1 TO N
3520   Sum=Sum+Lu(Ip,J)*X(J)
3530  NEXT J
3540  IF Lu(Ip,I)<>0 THEN 3570
3550  Oops=1
3560  SUBEXIT
3570  X(I)=(X(I)-Sum)/Lu(Ip,I)
3580 NEXT I
3590 SUBEND
3600 !
3610 SUB Decomp(N,A(*),Lu(*),INTEGER Ips(*),Oops)
3620 !
3630 !   © Copyright (1982) Hewlett-Packard Company.
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3640 !
3650 OPTION BASE 1
3660 ALLOCATE Scales(N)
3670 INTEGER I,J,K,Ip,Kp
3680 Oops=0
3690 FOR I=1 TO N
3700  Ips(I)=I
3710  Rowrm=0
3720  FOR J=1 TO N
3730   Lu(I,J)=A(I,J)
3740   IF Rowrm-ABS(Lu(I,J))>=0 THEN 3760
3750   Rowrm=ABS(Lu(I,J))
3760  NEXT J
3770  IF Rowrm<>0 THEN 3800
3780  Oops=1
3790  SUBEXIT
3800  Scales(I)=1/Rowrm
3810 NEXT I
3820 FOR K=1 TO N-1
3830  Big=0
3840  FOR I=K TO N
3850   Ip=Ips(I)
3860   Size=ABS(Lu(Ip,K))*Scales(Ip)
3870   IF Size-Big<=0 THEN 3900
3880   Big=Size
3890   Idxpiv=I
3900  NEXT I
3910  IF Big<>0 THEN 3940
3920  Oops=1
```

```
3930  SUBEXIT
3940  IF Idxpiv-K=0 THEN 3980
3950  J=Ips(K)
3960  Ips(K)=Ips(Idxpiv)
3970  Ips(Idxpiv)=J
3980  Kp=Ips(K)
3990  Pivot=Lu(Kp,K)
4000  FOR I=K+1 TO N
4010   Ip=Ips(I)
4020   Em=-Lu(Ip,K)/Pivot
4030   Lu(Ip,K)=-Em
4040   FOR J=K+1 TO N
4050    Lu(Ip,J)=Lu(Ip,J)+Em*Lu(Kp,J)
4060   NEXT J
4070  NEXT I
4080 NEXT K
4090 Kp=Ips(N)
4100 IF Lu(Kp,N)<>0 THEN SUBEXIT
4110 Oops=1
4120 SUBEND
4130 !
4140 DEF FNLin$(A)
4150 X=INT(A+.5)
4160 IF X=0 THEN RETURN CHR$(13)
4170 Eol$=CHR$(13)&CHR$(10)
4180 IF X<0 THEN Eol$=CHR$(10)
4190 ALLOCATE R$[X*LEN(Eol$)]
4200 R$=""
4210 FOR I=1 TO X
4220  R$=R$&Eol$
4230 NEXT I
4240 RETURN R$
4250 FNEND
4260 !
4270 SUB Transfer
4280 !
4290 ! This subroutine finds the final transfer
4300 ! functions for open/close loop operations.
4310 ! The resultant coefficients are in A(*) and
4320 ! B(*) arrays. If not successful it calls
4330 ! an alternative routine.
4340 OPTION BASE 1
4350 COM /Coeff/ A(*),B(*)
4360 COM /A/ N,M,L,D,Loop,Mm,Nc,Nf
4370 COM /D/ Aa(*),Ad(*),Ba(*),Bd(*),Ca(*),Cd(*),E(*),X(*),U(*),F(*),G(*)
4380 COM /In/ In
4390 COM /Alt/ Alt,Err
4400 ALLOCATE Y(N),Z(L),Af(N,N),Zz(N)
4410 INTEGER I,J
4420 IF Loop=2 THEN
4430  IF M>1 THEN
4440   INPUT "Input for closed-loop transfer function? (1 to M)",Mm
4450  IF Mm<1 OR Mm>M THEN 4440
4460  ELSE
4470   Mm=1
4480  END IF
4490 ELSE
4500  IF Loop<>3 THEN INPUT "Control(0) or Input (1 to M) transfer function?",Mm
4510  IF Mm>M THEN 4500
4520 END IF
4530 Inv(Nc,Aa(*),Af(*),Det)
4540 IF Det AND Mm>=0 THEN
4550  Mv_mul(Ba(*),U(*),Zz(*),Nc,M)
4560  Mv_mul(Af(*),Zz(*),X(*),Nc,Nc)
4570  Vs_mul(-1.,X(*),X(*),Nc)
```

```
4580                    ! X = -inv(A) B U
4590 ELSE
4600  BEEP
4610  IF Det=0 THEN PRINT "A MATRIX SINGULAR !"
4620  PRINT "Given ";
4630 END IF
4640 PRINT "Steady-State X Vector:",FNLin$(1)
4650 FOR I=1 TO Nc
4660  PRINT "X("&VAL$(I)&")=";FNRound(X(I),-5)
4670 NEXT I
4680 PRINT
4690 !                      -1
4700 !   H(s)  = Ca(sI-Aa)  Y+Z
4710 !
4720 IF Mm>0 AND Loop<>2 THEN     ! open-loop x/u
4730  FOR I=1 TO N
4740   Y(I)=Ba(I,Mm)
4750  NEXT I
4760  FOR I=1 TO L
4770   Z(I)=E(I,Mm)
4780  NEXT I
4790  ! Ca=C , Aa=A , Y=B , Z=E
4800 ELSE
4810  Mv_mul(Ad(*),X(*),Y(*),N,N)! open-loop x/d
4820  Mv_mul(Bd(*),U(*),Zz(*),N,M)
4830  Vv_add(Y(*),Zz(*),Y(*),N)
4840  Mv_mul(Cd(*),X(*),Z(*),L,N)
4850  ! Ca=C , Aa=A , Y=k , Z=(C1-C2)X
4860  !
4870  IF Loop=2 THEN              ! closed-loop x/u
4880   FOR J=1 TO N
4890    FOR I=1 TO N
4900     Aa(I,J)=Aa(I,J)+Y(I)*F(J)
4910    NEXT I                    ! Aa=A+kf
4920    FOR I=1 TO L
4930     Ca(I,J)=Ca(I,J)+Z(I)*F(J)
4940    NEXT I                    ! Ca=C+(C1-C2)Xf
4950   NEXT J
4960   IF In=0 THEN CALL Vs_mul(0.,G(*),G(*),M)
4970   FOR I=1 TO N
4980    Y(I)=Ba(I,Mm)+Y(I)*G(Mm)
4990   NEXT I                    ! Y=B+kg
5000   FOR I=1 TO L
5010    Z(I)=E(I,Mm)+Z(I)*G(Mm)
5020   NEXT I                    ! Z=E+(C1-C2)Xg
5030  END IF
5040 END IF
5050 !
5060 Transfer: IF Alt THEN
5070  ON ERROR GOTO 5090
5080  CALL Alternative
5090  OFF ERROR
5100  IF ERRN=7 THEN
5110   PRINT FNLin$(2);"Install the POWER ELECTRONICS disk";FNLin$(2)
5120   DISP "When done press CONT"
5130   PAUSE
5140   DISP
5150   LOADSUB ALL FROM "ALT"
5160  END IF
5170  DEALLOCATE Af(*),Zz(*)
5180  CALL Alternative(Ca(*),Aa(*),Y(*),Z(*))
5190  ! Generalized eigenvalue program
5200  SUBEXIT
5210 ELSE
5220  CALL Leverrier(Aa(*),Y(*),A(*),B(*))
```

```
5230  DISP
5240  IF Alt THEN Transfer
5250  ! A(*) and B(*) contain coefficients of
5260  ! numerator and denominator of Inv(sI-Aa)y
5270  ! respectively.
5280  ! Err contains the Leverrier test results.
5290  N1=N+1
5300  Mm_mul(Ca(*),A(*),Af(*),L,N,N)
5310  Ms_mul(0.,A(*),A(*),L,N1)
5320  FOR I=1 TO L
5330   FOR J=1 TO N1
5340    A(I,J)=Z(I)*B(J)
5350    IF J<=N THEN A(I,J)=A(I,J)+Af(I,J)
5360   NEXT J
5370  NEXT I
5380                ! ^     ^     ^            ^
5390                ! y = C x + E u + (C1-C2)X d
5400                !
5410  Det=B(1)            ! Det=|A|
5420  IF Det=0. THEN Det=1.
5430  Vs_mul(1./Det,B(*),B(*),N1)
5440  Ms_mul(1./Det,A(*),A(*),L,N1)
5450 END IF
5460 SUBEND
5470 !
5480 SUB Leverrier(A11(*),Y(*),A(*),B(*))
5490 !
5500 ! Routine to find the transfer functions
5510 ! by the Leverrier algorithm.  The result
5520 ! is the coefficients of Inv(sI-A11)*Y in
5530 ! the A matrix and b vector.  Err returns
5540 ! the accuracy of the method.
5550 !
5560 DISP "Calculating the transfer functions"
5570 OPTION BASE 1
5580 COM /A/ N,M,L,D,Loop,Mm,Nc,Nf
5590 COM /Alt/ Alt,Err
5600 ALLOCATE F(N,N),Z(N),Af(N,N)
5610 INTEGER I,J,K,N1,Nr
5620 N1=N+1
5630 Ms_mul(0.,Af(*),Af(*),N,N)  ! Af=0
5640 B(N+1)=1.
5650 FOR K=1 TO N
5660  Nr=N-K+1
5670  FOR I=1 TO N
5680   FOR J=1 TO N
5690    F(I,J)=0.
5700   NEXT J
5710   F(I,I)=B(Nr+1)             ! F = b I
5720  NEXT I
5730  Mm_add(F(*),Af(*),F(*),N,N)
5740                             ! F = Af + b I
5750  Mv_mul(F(*),Y(*),Z(*),N,N)
5760  FOR I=1 TO N
5770   A(I,Nr)=Z(I)      ! Numerator coefficients
5780  NEXT I
5790  Mm_mul(A11(*),F(*),Af(*),N,N,N)
5800                             ! Af = A11 * F
5810  B(Nr)=0.
5820  FOR I=1 TO N
5830   B(Nr)=B(Nr)-Af(I,I)/K     ! b = -Tr(Af)/K
5840  NEXT I             ! Denominator coefficients
5850 NEXT K
5860 !
5870 !   test for the method's accuracy
```

```
5880 !
5890 IF FNDet(N,A11(*))=0. THEN
5900  BEEP
5910  PRINT "WARNING: The A matrix is singular; accuracy check"
5920  PRINT "is cancelled.";FNLin$(1)
5930  SUBEXIT
5940 END IF
5950 !
5960 Test=0.
5970 FOR I=1 TO N
5980  FOR J=1 TO N
5990   IF I=J THEN 6010
6000   IF Test<ABS(Af(I,J)) THEN Test=ABS(Af(I,J))
6010  NEXT J
6020 NEXT I
6030 Err=ABS(Test/B(1))    ! maximum error
6040 IF Err>1.E-4 THEN
6050  BEEP
6060  PRINT "NUMERICAL ERROR OF THE STANDARD CALCULATIONS IS";FNRound(Err*100,-2
);"PERCENT."
6070  PRINT
6080  PRINT "However, an alternative is available.  This"
6090  PRINT "routine may take a long time."
6100  INPUT "Continue(C, ) or Alternative(A) ?",Q$
6110  IF Q$[1,1]="A" OR Q$[1,1]="a" THEN Alt=1
6120 END IF
6130 SUBEND
6140 !
6150 SUB Print_trans(INTEGER Prt,Title$(*))
6160 COM /Coeff/ A(*),B(*)
6170 COM /A/ N,M,L,D,Loop,Mm,Nc,Nf
6180 COM /Alt/ Alt,Err
6190 INTEGER G1,N1,I
6200 !
6210 N1=N+1
6220 INPUT "No transfer functions(1), on CRT(2), on printer(3)",G1
6230 IF G1<1 OR G1>3 THEN G1=2
6240 ON G1 GOTO 6490,6300,6250
6250 PRINTER IS Prt
6260 IF Alt=0 AND Err>1.E-4 THEN
6270  PRINT FNLin$(1);"Numerical error of the calculations is";FNRound(Err*100,-
2);"percent."
6280  PRINT
6290 END IF
6300 IF Loop=0 OR Loop=1 THEN
6310  A$="Control"
6320  IF Mm THEN A$="Input#"&VAL$(Mm)
6330  PRINT "Open-loop "&A$&"-to-Output transfer functions"
6340 END IF
6350 IF Loop=2 THEN PRINT "Closed-loop Input#"&VAL$(Mm)&"-to-Output transfer fun
ctions"
6360 PRINT
6370 PRINT "Denominator's coefficients:",FNLin$(1)
6380 FOR I=1 TO N1
6390  PRINT USING 6400;"B";I-1;B(I)
6400  IMAGE A,DD,"=",MD.5DE
6410 NEXT I
6420 FOR J=1 TO L
6430  PRINT FNLin$(1);"Numerator of "&Title$(J);FNLin$(1)
6440  FOR I=1 TO N1
6450   PRINT USING 6400;"A";I-1;A(J,I)
6460  NEXT I
6470 NEXT J
6480 PRINT
6490 PRINTER IS 1
6500 SUBEND
```

```
6510 !
6520 SUB Polezero(INTEGER Prt,Title$(*))
6530 OPTION BASE 1
6540 COM /Coeff/ A(*),B(*)
6550 COM /A/ N,M,L,D,Loop,Mm,Nc,Nf
6560 INTEGER G2,N1,I
6570 !
6580 ALLOCATE Rcoef(0:N),Icoef(0:N),Rroot(N),Iroot(N)
6590 PRINTER IS 1
6600 INPUT "No poles and zeros(1), on CRT(2), on printer(3)",G2
6610 IF G2<1 OR G2>3 THEN G2=2
6620 ON G2 GOTO 6860,6650,6630
6630 PRINTER IS Prt
6640                ! find order of the polynomial
6650 N1=N+1
6660 FOR Ii=0 TO L
6670  FOR Order=N1 TO 1 STEP -1
6680   IF Ii=0 THEN
6690    IF B(Order)<>0 THEN 6770
6700   ELSE
6710    IF A(Ii,Order)<>0 THEN 6770
6720   END IF
6730  NEXT Order
6740  BEEP
6750  PRINT Title$(Ii)&" is null !",FNLin$(1)
6760  GOTO 6850
6770  Order=Order-1
6780  FOR I=0 TO Order
6790   IF Ii=0 THEN Rcoef(I)=B(I+1)
6800   IF Ii THEN Rcoef(I)=A(Ii,I+1)
6810   Icoef(I)=0.
6820  NEXT I
6830  Siljak(Order,Rcoef(*),Icoef(*),1.E-6,1.E-6,100,Rroot(*),Iroot(*))
6840  Print_root(Ii,Order,Rroot(*),Iroot(*),Title$(*))
6850 NEXT Ii
6860 PRINTER IS 1
6870 SUBEND
6880 !
6890 SUB Siljak(N,Rcoef(*),Icoef(*),Tola,Tolf,Itmax,Rroot(*),Iroot(*))
6900 !
6910 ! Subroutine to find roots of a polynomial
6920 ! with complex coefficients Rcoef+jIcoef.
6930 ! The results are in form of Rroot+jIroot.
6940 !
6950 !   © Copyright (1982) Hewlett-Packard Company.
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6960 !
6970 ALLOCATE Xsiljak(0:N),Ysiljak(0:N)
6980 !
6990 ON ERROR GOTO 7830
7000 IF N=0 THEN SUBEXIT
7010 DISP "Calculating the poles and zeros"
7020 FOR I=1 TO N
7030 Rroot(I)=9.999999E+99
7040 Iroot(I)=9.999999E+99
7050 NEXT I
7060 N2=N
7070 IF N=1 THEN 7760
7080 DATA 1,1,1,.1,.1,0,0
7090 RESTORE 7080
7100 READ Y,Xsiljak(0),Ysiljak(1),X,Xsiljak(1),Ysiljak(0),L
7110 GOSUB Siljak
7120 G=F
7130 M=0
7140 Q=0
7150 P=0
7160 L=L+1
```

```
7170 ! *** Z=(DU/DX)^2+(DV/DX)^2.
7180 FOR K=1 TO N
7190  P=P+K*(Rcoef(K)*Xsiljak(K-1)-Icoef(K)*Ysiljak(K-1))
7200  Q=Q+K*(Rcoef(K)*Ysiljak(K-1)+Icoef(K)*Xsiljak(K-1))
7210 NEXT K
7220 Z=P*P+Q*Q
7230 ! *** Deltax AND Deltay ARE THE RESPECTIVE CHANGES IN X AND CHANGES IN Y.
7240 Deltax=-(U*P+V*Q)/Z
7250 Deltay=(U*Q-V*P)/Z
7260 ! INCREMENT SUCCESSIVE QUARTERING COUNTER.
7270 M=M+1
7280 !
7290 !
7300 ! *** NEW ROOT APPROXIMATIONS X,Y LOADED
7310 ! *** INTO Xsiljak(1) AND Ysiljak(1).
7320 !
7330 Xsiljak(1)=X+Deltax
7340 Ysiljak(1)=Y+Deltay
7350 ! *** RECOMPUTE SILJAK COEFFICIENTS.
7360 GOSUB Siljak
7370 IF F>=G THEN 7430
7380 IF (ABS(Deltax)<Tola) AND (ABS(Deltay)<Tola) THEN 7550
7390 IF L>Itmax THEN 7560
7400 X=Xsiljak(1)
7410 Y=Ysiljak(1)
7420 GOTO 7120
7430 IF M>20 THEN 7470
7440 Deltax=Deltax/4
7450 Deltay=Deltay/4
7460 GOTO 7270
7470 IF (ABS(U)<=Tolf) AND (ABS(V)<=Tolf) THEN 7550
7480 PRINT FNLin(2);"ERROR IN SUBPROGRAM Siljak."
7490 PRINT "THE INTERVAL SIZE HAS BEEN QUARTERED 20 TIMES AND "
7500 PRINT "THE TOLERANCE FOR FUNCTIONAL EVALUATIONS IS STILL NOT MET."
7510 PRINT "Tolf=";Tolf,"U=";U,"V=";V,FNLin(2)
7520 PRINT "MAXIMUM # OF ITERATIONS HAS BEEN EXCEEDED."
7530 PRINT "L=";L,"Itmax=";Itmax,FNLin(2)
7540 GOTO 7830
7550 Rroot(N)=Xsiljak(1)
7560 Iroot(N)=Ysiljak(1)
7570 A=Rcoef(N)
7580 B=Icoef(N)
7590 Rcoef(N)=0
7600 Icoef(N)=0
7610 X=Xsiljak(1)
7620 Y=Ysiljak(1)
7630 FOR K=N-1 TO 0 STEP -1
7640  C=Rcoef(K)
7650  D=Icoef(K)
7660  U=Rcoef(K+1)
7670  V=Icoef(K+1)
7680  Rcoef(K)=A+X*U-Y*V
7690  Icoef(K)=B+X*V+Y*U
7700  A=C
7710  B=D
7720 NEXT K
7730 N=N-1
7740 ! *** REDUCE NUMBER OF COEFFICIENTS AND BEGIN AGAIN.
7750 IF N<>1 THEN 7070
7760 A=Rcoef(0)
7770 U=Rcoef(1)
7780 B=Icoef(0)
7790 V=Icoef(1)
7800 T=U*U+V*V
7810 Rroot(1)=-(A*U+B*V)/T
```

```
7820 Iroot(1)=(A*V-U*B)/T
7830 N=N2
7840 DISP
7850 SUBEXIT
7860 !
7870 ! *** SUBROUTINE TO COMPUTE SILJAK COEFFICIENTS.
7880 Siljak: Z=Xsiljak(1)*Xsiljak(1)+Ysiljak(1)*Ysiljak(1)
7890 T=2*Xsiljak(1)
7900 FOR K=0 TO N-2
7910  Xsiljak(K+2)=T*Xsiljak(K+1)-Z*Xsiljak(K)
7920  Ysiljak(K+2)=T*Ysiljak(K+1)-Z*Ysiljak(K)
7930 NEXT K
7940 U=0
7950 V=0
7960 FOR K=0 TO N
7970  U=U+Rcoef(K)*Xsiljak(K)-Icoef(K)*Ysiljak(K)
7980  V=V+Rcoef(K)*Ysiljak(K)+Icoef(K)*Xsiljak(K)
7990 NEXT K
8000 F=U*U+V*V
8010 RETURN
8020 SUBEND
8030 !
8040 !
8050 SUB Print_root(Ii,N,Rroot(*),Iroot(*),A$(*))
8060 !
8070 ! Subroutine to print the outputs of the
8080 ! siljak.
8090 !
8100 ALLOCATE B$[50]
8110 ON ERROR GOTO 8140
8120 IF N=0 THEN
8130  PRINT A$(Ii)&" has no zeros",FNLin$(1)
8140  SUBEXIT
8150 END IF
8160 IF Ii=0 THEN PRINT "Poles",FNLin$(1)
8170 IF Ii<>0 THEN PRINT "Zeros of "&A$(Ii),FNLin$(1)
8180 PRINT USING "4X,2(4A,7X),1X,4A,9X,A";"Real","Imag","Freq","Q"
8190 Vs_mul(1/(2*PI),Rroot(*),Rroot(*),N)
8200 Vs_mul(1/(2*PI),Iroot(*),Iroot(*),N)
8210 !    convert radian to frequency
8220 FOR I=1 TO N
8230  Type$=""
8240  F$="0.00000  Hz"
8250  Q$="   REAL  "
8260  Pow$="um kMG"         ! initial values
8270  IF Rroot(I)>0 THEN Type$="RHP"
8280  IF (Ii=0) AND (Type$="RHP") THEN Type$="UNSTABLE"
8290  F=SQR(Iroot(I)^2+Rroot(I)^2)
8300  ON 1+(F>1.E-6)+(F>1.E+11)+(F>1.E+99) GOTO 8490,8350,8310,8330
8310  OUTPUT F$ USING "D.2DE,3A";F," Hz"
8320  GOTO 8420
8330  PRINT B$&"Root #";I;"was not calculated"
8340  GOTO 8540
8350  OUTPUT F$ USING "D.5DE";F
8360  P=VAL(F$[9])+9
8370  F$=F$[1,1]&F$[3,7]
8380  F$=F$[1,P MOD 3+1]&"."&F$[P MOD 3+2]&" "&Pow$[P DIV 3;1]&"Hz"
8390  IF Rroot(I)<>0 THEN 8420
8400  Q$=" INFINITY"
8410  GOTO 8490
8420  Q=F/(2*ABS(Rroot(I)))
8430  IF Q<.50005 THEN 8490
8440  K=3-INT(LGT(Q))
8450  OUTPUT Q$ USING "D.3DE";Q
8460  IF K<0 THEN 8490
8470  Q$="   "&VAL$(FNRound(Q,-K))&"  "
```

```
8480                ! content-dependent image
8490  B$="2(MD.3DE,1X),1X,11A,1X,9A"
8500  IF Type$="" THEN B$=B$&",A"
8510  IF Type$="RHP" THEN B$=B$&",3X,3A"
8520  IF Type$="UNSTABLE" THEN B$=B$&",20X,8A"
8530  PRINT USING B$;Rroot(I),Iroot(I),F$,Q$,Type$
8540 NEXT I
8550 PRINT
8560 SUBEND
8570 !
8580 !
8590 SUB Response
8600 !
8610 ! This part finds the frequency response of
8620 ! the transfer functions and puts the results
8630 ! in the memory.
8640 !
8650 OPTION BASE 1
8660 COM /Mem/ Yy(*),Title$(*)
8670 COM /Coeff/ A(*),B(*)
8680 COM /A/ N,M,L,D,Loop,Mm,Nc,Nf
8690 COM /B/ Fmin,Fmax,Nn,Count(*)
8700 INTEGER I,J,K,Jj
8710 !
8720 N1=N+1
8730 ALLOCATE Temp(L),A360(L),S(N1,2),Num(L,2)
8740 INPUT "Enter Fmin, Fmax, and number of calculations",Fmin,Fmax,Nn
8750 IF Nn<2 OR Nn>400 OR Fmin<1.E-4 OR 2*PI*Fmax>=10^(200/N) OR Fmin>=Fmax THEN
 8740
8760 Deltaf=EXP(LOG(Fmax/Fmin)/(Nn-1))
8770 F=2*PI*Fmin
8780 FOR I=1 TO L
8790  Temp(I)=0.
8800  A360(I)=0.
8810  Count(I)=Nn
8820 NEXT I
8830 S(1,1)=1.
8840 S(1,2)=0.
8850 ON ERROR GOTO Problems
8860 FOR K=1 TO Nn
8870  DISP "Calculating",K
8880  P=0.
8890  Q=F
8900  FOR I=2 TO N1
8910   S(I,1)=P
8920   S(I,2)=Q
8930   W=-F*Q
8940   Q=F*P
8950   P=W
8960  NEXT I
8970 !         2  3
8980 ! S=[1,s,s ,s ,......]  &  s=jw
8990 !
9000  V=0.
9010  W=0.
9020  FOR I=1 TO N1
9030   W=W+B(I)*S(I,1)
9040   V=V+B(I)*S(I,2)
9050  NEXT I
9060                          ! Den. calculated
9070  Mag2=W*W+V*V            ! denominator^2
9080  Mm_mul(A(*),S(*),Num(*),L,N1,2)
9090                          ! Num. calculatad
9100                          ! service for each output
9110  FOR Jj=1 TO L
```

```
9120   P=Num(Jj,1)
9130   Q=Num(Jj,2)
9140 E1: Real=(P*W+Q*V)/Mag2
9150   Imag=(Q*W-P*V)/Mag2
9160   Mag=Real*Real+Imag*Imag    ! Magnitude^2
9170 E2: Phs=ATN(Imag/Real)       ! Phase
9180   IF Real<0. THEN Phs=Phs+180.
9190 !
9200 ! This part fixes discountinuities in phase.
9210 !
9220 R2:Phs=Phs-A360(Jj)
9230   IF Phs-Temp(Jj)-200.<=0. THEN Chk2
9240   A360(Jj)=A360(Jj)+360.
9250   Phs=Phs-360.
9260   GOTO Formal
9270 Chk2:IF Temp(Jj)-Phs-200.<=0. THEN Formal
9280   A360(Jj)=A360(Jj)-360.
9290   Phs=Phs+360.
9300 Formal: Temp(Jj)=Phs
9310   Yy(2*Jj-1,K)=10.*LGT(Mag)! magnitude in dB
9320   Yy(2*Jj,K)=Phs            ! corrected phase
9330 Nextjj: NEXT Jj
9340  F=F*Deltaf
9350  ! logarithmic increase of the frequency
9360 NEXT K
9370 DISP
9380 OFF ERROR
9390 SUBEXIT
9400 !
9410 Problems: !  Calculation problems
9420  IF ERRN=31 THEN
9430   IF ERRL(E2) THEN
9440    Phs=90*SGN(Imag)
9450    IF Phs THEN R2
9460    BEEP
9470    PRINT "calculation problem on ";Title$(Jj)
9480    PRINT "point #";K
9490    Yy(2*Jj-1,K)=0.
9500    Yy(2*Jj,K)=0.
9510    GOTO Nextjj
9520   END IF
9530   IF ERRL(E1) THEN 9460
9540  END IF
9550  BEEP
9560  PRINT "Error number ";ERRN
9570  STOP
9580  !
9590 SUBEND
9600  !
9610 SUB Measure_in
9620 !
9630 ! Reads the measurement results in.
9640 !
9650 COM /Mem/ Yy(*),Title$(*)
9660 COM /B/ Fmin,Fmax,Nn,Count(*)
9670 INTEGER I,Out
9680 Edit("Enter the name of the measurement file",Measure$)
9690 FOR Out=5 TO 1 STEP -1
9700  IF Count(Out)=0 THEN 9800
9710 NEXT Out                ! find an output #
9720 BEEP
9730 INPUT "Memory is full.. Select one output to over-write",Out
9740 IF Out>5 OR Out<1 THEN
9750  BEEP
9760  DISP "NOT A VALID NUMBER"
9770  WAIT 1
```

```
9780  GOTO 9730
9790 END IF
9800 ON ERROR GOTO Read_error
9810 ASSIGN @Q TO Measure$
9820 ENTER @Q;Q$,Q$,W,W,W,W,W,W,W,V,W,Tfmin,Yy(2*Out-1,1),Yy(2*Out,1)
9830 Count(Out)=-V
9840 FOR I=2 TO V
9850  ENTER @Q;Tfmax,Yy(2*Out-1,I),Yy(2*Out,I)
9860 NEXT I
9870 ASSIGN @Q TO *
9880 OFF ERROR
9890 IF Tfmin<>Fmin OR Tfmax<>Fmax THEN
9900  BEEP
9910  PRINT "Frequency bounds mismatch.. Following limits are"
9920  PRINT "in effect now:"
9930  PRINT FNLin$(2);"Fmin=";Tfmin;", Fmax=";Tfmax;FNLin$(1)
9940  Fmin=Tfmin
9950  Fmax=Tfmax
9960 END IF
9970 Title$(Out)="MEASUREMENT;"&Measure$
9980 P=POS(Measure$,":")
9990 IF P THEN Title$(Out)=Title$(Out)[1,11+P]
10000 SUBEXIT
10010!
10020 Read_error:!
10030 PRINT "ERROR IN ";Measure$
10040 BEEP
10050 SUBEND
10060!
10070!
10080 SUB Print(Out,Yy(*),Title$)
10090!
10100! Subroutine to print the results.
10110!
10120 COM /B/ Fmin,Fmax,Nn,Count(*)
10130 ALLOCATE A$[50]
10140 N=ABS(Count(Out))
10150 PRINT FNPage$;Title$
10160 PRINT
10170 PRINT USING "9A,8X,9A,8X,6A,/";"FREQUENCY","AMPLITUDE"," PHASE"
10180 Df=EXP(LOG(Fmax/Fmin)/(N-1))
10190 F=Fmin
10200 FOR I=1 TO N
10210 ! image changes according to frequency
10220 !
10230  A$=",8X,M4D.DD,7X,M5D.DD"
10240  IF F>10 AND F<1.E+7 THEN A$="7D.D"&A$
10250  IF F>=1.E+7 THEN A$="D.3DE"&A$
10260  IF F<=10 THEN A$="3D.5D"&A$
10270  PRINT USING A$;F,Yy(2*Out-1,I),Yy(2*Out,I)
10280  F=F*Df
10290 NEXT I
10300 PRINT FNLin$(3)
10310 PRINTER IS 1
10320 SUBEND
10330 !
10340 !
10350 SUB Bode_plot(Out,Type,Yy(*),A$)
10360 !
10370 ! Bode plot of the results
10380 !
10390 COM /B/ Fmin,Fmax,Nn,Count(*)
10400 COM /C/ INTEGER Plt,Graph,Offset(*)
10410 COM /P/ Amin,Amax,Pmin,Pmax
10420 COM /P/ INTEGER Overl,Pen2,Mode,Flag
```

```
10430 INTEGER Line,Pen,Amp,Phs,I,J,K
10440 DIM Title$[30]
10450 OFF KEY
10460 ON KEY 9 LABEL "Exit" GOTO Exit
10470 Phs=2*Out
10480 Amp=Phs-1        ! pointers to the memory
10490 Line=1
10500 Pen=1
10510 Ex=(Count(Out)<0)*Out
10520 N=ABS(Count(Out))
10530!
10540! overlay
10550!
10560 IF Type=2 THEN
10570  IF Flag=0 THEN SUBEXIT
10580  INPUT "Enter the LINE TYPE",Over1
10590  Line=Over1
10600  IF Out=Ex THEN INPUT "Enter amplitude and phase offset",Offset(Out,0),Off
set(Out,1)
10610  IF Graph=1 THEN
10620   GRAPHICS ON
10630   ALPHA OFF
10640  ELSE
10650   INPUT "Enter the pen number",Pen2
10660   Pen=Pen2
10670  END IF
10680  GOTO Plain
10690 END IF
10700!
10710! plot eraser ( CRT only )
10720!
10730 IF Type=3 THEN
10740  IF Graph<>1 THEN SUBEXIT
10750  Pen=-1
10760  GRAPHICS ON
10770  ALPHA OFF
10780  GOTO Plain
10790 END IF
10800!
10810 Amx=Yy(Amp,1)
10820 Amn=Amx
10830 Pmx=Yy(Phs,1)
10840 Pmn=Pmx
10850 FOR I=1 TO N
10860  IF Yy(Amp,I)>Amx THEN Amx=Yy(Amp,I)
10870  IF Yy(Amp,I)<Amn THEN Amn=Yy(Amp,I)
10880  IF Yy(Phs,I)>Pmx THEN Pmx=Yy(Phs,I)
10890  IF Yy(Phs,I)<Pmn THEN Pmn=Yy(Phs,I)
10900 NEXT I
10910   ! max. and min. of amplitude & phase
10920 PRINT "Plot for "&A$,FNLin$(2)
10930 PRINT "Amin=";FNRound(Amn,-2);TAB(20);"Pmin=";FNRound(Pmn,-2)
10940 PRINT "Amax=";FNRound(Amx,-2);TAB(20);"Pmax=";FNRound(Pmx,-2),FNLin$(1)
10950 Amn=Amn+Offset(Out,0)
10960 Amx=Amx+Offset(Out,0)
10970 Pmn=Pmn+Offset(Out,1)
10980 Pmx=Pmx+Offset(Out,1)
10990 IF Type=1 THEN
11000  IF Out=Ex THEN INPUT "Enter amplitude and phase offset",Offset(Out,0),Off
set(Out,1)
11010 END IF
11020 Title$=A$[1,30]
11030 Edit("Title of the plot",Title$)
11040 INPUT "Enter AMPmin,AMPmax ( 0,0 for auto-scaling)",Amin,Amax
11050 IF Amin>=Amax THEN Auto
```

```
11060 INPUT "Enter PHASEmin,PHASEmax ( 0,0 for auto-scaling)",Pmin,Pmax
11070 IF Pmin>=Pmax THEN Auto
11080 INPUT "Plot : Plain(1), with scaling(2), or Full graph(3)",Mode
11090 IF Mode<1 OR Mode>3 THEN Mode=3
11100 Flag=1
11110 GINIT
11120 IF Graph=1 THEN
11130  PLOTTER IS 3,"INTERNAL"
11140  GRAPHICS ON
11150  ALPHA OFF
11160 ELSE
11170  PLOTTER IS Plt,"HPGL"
11180  OUTPUT Plt USING "K";"VS3"
11190  INPUT "Enter the pen number",Pen2
11200  Pen=Pen2
11210 END IF
11220 !
11230 ON Mode GOTO Plain,Scaling,Full
11240 ! labels
11250 Full:LINE TYPE 1
11260 FRAME
11270 WINDOW 0,100,0,100
11280 CSIZE 4
11290 LORG 5
11300 MOVE 50,95
11310 LABEL USING "K";Title$
11320 CSIZE 3
11330 LORG 2
11340 MOVE 3,97
11350 LABEL USING "4A,/,4A";"Amp.","(dB)"
11360 MOVE 5,3
11370 LABEL USING "K";"Fmin="&VAL$(Fmin)&"Hz"
11380 MOVE 95,3
11390 LORG 8
11400 LABEL USING "K";"Fmax="&VAL$(Fmax)&"Hz"
11410 MOVE 98,97
11420 LABEL USING "6A,/,5A";"Phase ","(deg)"
11430 !
11440 Scaling:FRAME
11450 Xmin=LGT(Fmin)
11460 Xmax=LGT(Fmax)
11470 L=100*RATIO
11480 C=-(10*Xmax-(L-10)*Xmin)/(L-20)
11490 D=((L-10)*Xmax-10*Xmin)/(L-20)
11500 IF Mode=3 THEN WINDOW C,D,-12.5,112.5
11510 IF Mode=2 THEN WINDOW Xmin,Xmax,0,100
11520 Y=Xmax-Xmin
11530 Coef=10^(INT(Xmin)-1)
11540 Space=1-(Y<=1)*.5-(Y<=.5)*.4-(Y<.04)*.08
11550 FOR I=INT(Xmin) TO 20
11560 Coef=Coef*10
11570 FOR J=1 TO 10-Space STEP Space
11580  F=J*Coef
11590  IF Fmin>F THEN 11720
11600  IF F>Fmax THEN 11740
11610  X=LGT(F)
11620  MOVE X,2+2*(J=1)+(J=2)+(J=5)
11630  DRAW X,0
11640  PENUP
11650  LORG 6
11660  IF Space<>1 AND INT(J)=J THEN 11680
11670  IF J<>1 AND J<>2 AND J<>5 THEN 11720
11680  IF Mode=3 THEN
11690   MOVE X,-2
11700   LABEL USING "D";J ! tics and labels
```

```
11710  END IF
11720 NEXT J
11730 NEXT I
11740 FOR K=1 TO 2
11750  IF K=1 THEN
11760   P=Amin
11770   Q=Amax
11780   X=Xmin
11790   Tip=(Xmax-Xmin)/100
11800   Ad=Q-P
11810   Tic=.4+.6*(Ad>25)+(Ad>50)+2*(Ad>100)+4*(Ad>200)
11820   Space=Tic*5
11830  ELSE
11840   P=Pmin
11850   Q=Pmax
11860   Y=Q-P
11870   X=Xmax
11880   Tip=-Tip
11890   Tic=1+(Y>40)+3*(Y>80)+5*(Y>200)+10*(Y>800)
11900   Space=9*Tic
11910  END IF
11920  IF Mode=3 THEN WINDOW C,D,-(10*Q-90*P)/80,(90*Q-10*P)/80
11930  IF Mode=2 THEN WINDOW Xmin,Xmax,P,Q
11940  I=INT((INT(Q/Space)+1)*Space)
11950  FOR Jj=I TO P STEP -Tic
11960   IF Jj>Q THEN Con
11970   IF Jj<P THEN 12120
11980   PENUP
11990   MOVE X,Jj
12000   IF INT(ABS(Jj/Space)+1.E-6)*Space=FNRound(ABS(Jj),-2) THEN
12010    LORG 14-6*K
12020    MOVE X+Tip*2,Jj
12030    DRAW X,Jj
12040    IF Mode=2 OR Turn=1 THEN Con
12050    IF K=1 THEN LABEL USING "M3D,X";Jj
12060    IF K=2 THEN LABEL USING "M4D";Jj
12070   ELSE
12080    DRAW X+Tip,Jj
12090    PENUP
12100   END IF
12110 Con:NEXT Jj
12120 NEXT K
12130 IF Mode=3 THEN
12140 VIEWPORT 10,100*RATIO-10,10,90
12150 FRAME
12160 END IF
12170 ! plot of the data
12180 !
12190 Plain:PENUP
12200 GRAPHICS ON
12210 ALPHA OFF
12220 LINE TYPE Line
12230 PEN Pen
12240 WINDOW 1,N,Amin,Amax
12250 FOR I=0 TO 1         ! offset for measurement
12260  MOVE 1,Yy(Amp+I,1)+Offset(Out,I)*(Ex=Out)
12270  FOR J=1 TO N
12280   DRAW J,Yy(Amp+I,J)+Offset(Out,I)*(Ex=Out)
12290  NEXT J
12300  WINDOW 1,N,Pmin,Pmax
12310  PENUP
12320 NEXT I
12330 PEN 0
12340 PAUSE
12350 SUBEXIT
12360 !
```

```
12370 ! auto-scaling
12380 !
12390 Auto:IF Amx>Amn THEN 12420
12400 Amn=Amn-5
12410 Amx=Amx+5
12420 Amin=(.95*Amn-.51*Amx)/.44
12430 Amax=(Amx-.05*Amin)/.95
12440 IF Pmx>Pmn THEN 12470
12450 Pmn=Pmn-30
12460 Pmx=Pmx+30
12470 Pmin=(.49*Pmn-.05*Pmx)/.44
12480 Pmax=(Pmx-.51*Pmin)/.49
12490 Digit=0
12500 IF Amax-Amin<10 THEN Digit=-1
12510 Amin=FNRound(Amin,Digit)
12520 Amax=FNRound(Amax,Digit)
12530 P=(Pmax-Pmin>100)
12540 Pmin=FNRound(Pmin,P)
12550 Pmax=FNRound(Pmax,P)
12560 GOTO 11080
12570 !
12580 Exit:  PEN 0
12590 SUBEND
12600 !
12610 DEF FNMax(A,B)                    ! MAX
12620 Max=A
12630 IF B>A THEN Max=B
12640 RETURN Max
12650 FNEND
12660                                   ! MIN
12670 DEF FNMin(A,B)
12680 Min=A
12690 IF B<A THEN Min=B
12700 RETURN Min
12710 FNEND
12720                                   ! ROUND
12730 DEF FNRound(A,B)
12740 C=10^B
12750 R=INT(A/C+.5)*C
12760 RETURN R
12770 FNEND
12780                                   ! EDIT
12790 SUB Edit(Prompt$,A$)
12800 DISP Prompt$;
12810 OUTPUT 2;A$;
12820 LINPUT "",A$
12830 SUBEND
12840                                   ! PAGE
12850 DEF FNPage$
12860 OUTPUT 2;"*K";
12870 RETURN ""
12880 FNEND
12890 !
12900 SUB Read_data(A$(*))
12910 !
12920 ! Subroutine to read input data and through
12930 ! averaging, find A, B, and other matrices
12940 ! of the system.
12950 !
12960 OPTION BASE 1
12970 COM /A/ N,M,L,D,Loop,Mm,Nc,Nf
12980 COM /D/ Aa(*),Ad(*),Ba(*),Bd(*),Ca(*),Cd(*),E(*),X(*),U(*),F(*),G(*)
12990 COM /In/ In
13000 ON ERROR GOTO Err
13010 RESTORE
13020 READ N,M,L,D,Tsw
```

```
13030 In=(Tsw<0)
13040 IF N<2 AND N>15 AND M<1 AND M>6 AND L<1 AND L>5 THEN
13050  BEEP
13060  PRINT "ERROR IN ONE OF THE FOLLOWINGS:";FNLin$(1);"N=";N,"M=";M,"L=";L
13070  STOP
13080 END IF
13090 Nc=N
13100 ALLOCATE A1(N,N),A2(N,N),B1(N,M),B2(N,M),Xt(N),Ut(M)
13110 ALLOCATE P(N,N),Pinv(N,N),C1(L,N),C2(L,N)
13120 ALLOCATE A(N,N),B(N,M),C(L,N)
13130 IF Loop THEN
13140  INPUT "Enter the order of the feedback network",Nf
13150  IF Nf<0 OR Nf>N THEN 13140
13160  Nc=N-Nf
13170 END IF
13180 DISP "Reading and processing data"
13190 IF D<0 OR D>1 THEN
13200  BEEP
13210  PRINT "WARNING: D=";D
13220 END IF
13230 FOR I=1 TO L
13240  A$(I)="Output # "&VAL$(I) ! Default titles
13250 NEXT I
13260 !
13270 READ P(*)
13280 Inv(N,P(*),Pinv(*),Det)
13290 IF Det=0. THEN
13300  DISP "P MATRIX IS SINGULAR !"
13310  BEEP 200,1
13320  STOP
13330 END IF
13340 READ A1(*),A2(*),B1(*),B2(*),Xt(*),Ut(*)
13350 Vv_eq(Xt(*),X(*),N)
13360 Vv_eq(Ut(*),U(*),M)
13370 Mm_mul(Pinv(*),A1(*),A(*),N,N,N)
13380 Mm_eq(A(*),A1(*),N,N)
13390 Mm_mul(Pinv(*),A2(*),A(*),N,N,N)
13400 Mm_eq(A(*),A2(*),N,N)
13410 Mm_mul(Pinv(*),B1(*),B(*),N,N,M)
13420 Mm_eq(B(*),B1(*),N,M)
13430 Mm_mul(Pinv(*),B2(*),B(*),N,N,M)
13440 Mm_eq(B(*),B2(*),N,M)
13450                    ! Aa = D A1 + D'A2
13460                    ! Ad = A1 - A2
13470 FOR I=1 TO N
13480  FOR J=1 TO N
13490   Aa(I,J)=D*A1(I,J)+(1-D)*A2(I,J)
13500   Ad(I,J)=A1(I,J)-A2(I,J)
13510  NEXT J
13520                    ! Ba = D B1 + D'B2
13530                    ! Bd = B1 - B2
13540  FOR J=1 TO M
13550   Ba(I,J)=D*B1(I,J)+(1-D)*B2(I,J)
13560   Bd(I,J)=B1(I,J)-B2(I,J)
13570  NEXT J
13580 NEXT I
13590 Out: READ C1(*),C2(*)
13600 Ms_mul(0.,E(*),E(*),L,M)  ! E=0
13610 IF In THEN
13620  FOR I=1 TO L
13630   FOR J=1 TO M
13640    READ E(I,J)     ! E
13650   NEXT J
13660  NEXT I
13670 END IF
13680                    ! Ca = D C1 + D' C2
```

```
13690                    ! Cd = C1 - C2
13700 FOR I=1 TO L
13710  FOR J=1 TO N
13720   Ca(I,J)=D*C1(I,J)+(1-D)*C2(I,J)
13730   Cd(I,J)=C1(I,J)-C2(I,J)
13740  NEXT J
13750 NEXT I
13760 IF Loop=3 THEN     ! LOOP GAIN
13770  L=1
13780  Mm=0
13790  A$(1)="LOOP GAIN"
13800  FOR I=1 TO N
13810 Loopgain: READ C1(1,I)
13820   Ca(1,I)=-C1(1,I)          ! Ca = -f
13830   Cd(1,I)=0.                ! Cd = 0
13840  NEXT I
13850  DISP
13860  SUBEXIT
13870 END IF
13880 IF Loop=2 THEN             ! closed loop
13890  Vs_mul(0.,F(*),F(*),15)
13900  Vs_mul(0.,G(*),G(*),15)
13910  FOR I=1 TO N
13920 Fread:  READ F(I)          ! f vector
13930  NEXT I
13940  IF In THEN
13950   FOR I=1 TO M
13960 Gread:  READ G(I)          ! g vector
13970   NEXT I
13980  END IF
13990 END IF
14000 DISP
14010 SUBEXIT
14020 Err:  ! error conditions
14030 IF ERRN=32 AND ERRL(Out) THEN
14040  FOR I=1 TO L
14050   READ A$(I)               ! read titles
14060  NEXT I
14070  GOTO Out
14080 END IF
14090 BEEP
14100 IF ERRL(Fread) OR ERRL(Loopgain) THEN
14110  DISP "f vector missing !"
14120  STOP
14130 END IF
14140 IF ERRL(Gread) THEN
14150  DISP "g vector missing !"
14160  STOP
14170 END IF
14180 DISP "Error in data    #";ERRN
14190 STOP
14200 !
14210 !
14220 !

data for the program


20000 SUBEND
```