Silicon Heterojunctions

Thesis by

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To Krista

Acknowledgments

I am happy to have had the opportunity to work with Tom McGill. He stayed out of the way of the experiments while giving critical guidance when necessary. In addition, he taught me some of the most important skills needed in today's environment – communication, presentation, marketing, and fund raising skills.

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List of Publications

Work related to this thesis has been, or will be, published under the following titles:

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P.O. Pettersson, R.J. Miles, and T.C. McGill, *J. Appl. Phys.* **76**, 7328 (1994).

Temperature dependence of surface morphology of silicon grown on CaF_2/Si by electron beam assisted MBE,
P.O. Pettersson, R.J. Miles, and T.C. McGill, Mat. Res. Soc. Symp. Proc. Vol. **367**, 305 (1995).

Sb-Surfactant-Mediated Growth of $Si/Si_{1-y}C_y$ Superlattices by Molecular-Beam Epitaxy,
P.O. Pettersson, C.C. Ahn, T.C. McGill, E.T. Croke, and A.T. Hunter, Appl. Phys. Lett. **67**, 2530 (1995).

Characterization of $Si/Si_{1-y}C_y$ Superlattices Grown by Surfactant Assisted Molecular Beam Epitaxy,
P.O. Pettersson, C.C. Ahn, T.C. McGill, E.T. Croke, and A.T. Hunter, Accepted for publication, J. Vac. Sci. Technolog. **B** (1996).

Dependence of the I/V curve of a Metal Insulator Semiconductor Switch on insulator thickness - an experimental and theoretical investigation,

P.O. Pettersson, A. Zur, E.S. Daniel, H.J. Levy, O.J. Marsh, and T.C. McGill, To be submitted, IEEE Electron Devices (1996).

Abstract

The three topics presented in this thesis all concern silicon heterojunction growth and device applications. We developed growth techniques for two relatively immature material systems, silicon/calciumfluoride (Si/CaF_2) and silicon/silicon-carbon ($Si/Si_{1-y}C_y$), and fabricated devices which take the mature silicon/silicon dioxides (Si/SiO_2) material system to new limits in terms of oxide thickness.

We applied novel growth techniques in the undeveloped material systems with the ultimate goal of producing device quality material suitable for quantum device fabrication. In the Si/CaF_2 material system, we used a new technique known as Electron Beam Assisted Molecular Beam Epitaxy to improve the morphology of silicon grown on calciumfluoride. The result was a decrease in roughness of the silicon overlayer. In the silicon/silicon-carbon material system, we employed Surfactant Assisted Molecular Beam Epitaxy to grow smooth high carbon content silicon-carbon on silicon. Here, the result was a greatly improved surface morhology and the technique looks promising for applications requiring high carbon concentrations.

In the mature and extremely important (from a technological and commercial point of view) Si/SiO_2 material system, we fabricated Metal Insulator Semiconductor Switches devices in a study of the dependence of the I/V curve on the insulator thickness. While the primary objective of this study was to optimize the I/V curve, we learned that this material system is not very well understood, neither from a theoretical nor experimental standpoint, when the oxide is extremely thin.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

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In the mature and extremely important (from a technological and commercial point of view) Si/SiO_2 material system, we fabricated Metal Insulator Semiconductor Switches devices in a study of the dependence of the I/V curve on the insulator thickness. While the primary objective of this study was to optimize the I/V curve, we learned that this material system is not very well understood, neither from a theoretical nor experimental standpoint, when the oxide is extremely thin.

The uniting theme of these studies is that they all involve silicon heterojunc-

tions and that they embody the spirit of *applied* physics in the sense that they all drive toward making useful devices.

1.1 Overview of Thesis

The three related topics are presented in chapters 3, 4, and 5. The first two topics, silicon overgrowth on CaF_2/Si and surfactant assisted growth of $Si_{1-y}C_y$/Si, are introduced in this chapter. The final topic, fabrication of a Metal Insulator Semiconductor Switch and study of the influence of the oxide thickness on the I/V curve of the device, is introduced in chapter 2.

1.2 The Si/CaF$_2$ Material System

1.2.1 Background

This material system had been investigated extensively by the time we started working in the area. CaF_2 had been grown on silicon about ten years earlier[1] and many studies of this material system had subsequently been reported. For a review of the field, see Schowalter[2]. Interestingly, only a few reports had been published on the silicon overgrowth on CaF_2. For some examples, see Isiwara[1], Asano[3], and Fathauer[4]. One reason for this is that while it is easy to grow high quality CaF_2 on silicon, the quality of a silicon overlayer, when grown on CaF_2, is poor.

Some methods for improving the silicon overlayer quality had been proposed, but they relied on growing a poor quality (low growth temperature) initial layer of silicon and then annealing it. One would then grow a thick silicon (high growth temperature) layer where the quality improved as the thickness increased[3]. Unfortunately, this method would not work in our application as we needed an extremely thin high quality silicon layer. Thus, we had to apply another method

to improve the silicon quality. We chose to apply a novel technique, known as Electron Beam Assisted MBE, that had previously been used to improve Ge [2] and GaAs [3] overgrowth on CaF_2. Before we continue to describe the details of the experiment, we will take a moment to motivate our interest in this material system by pointing out some of the interesting device applications.

1.2.2 Potential Applications

If the silicon/calciumfluoride material system could be made to work, it might be one way to integrate quantum devices with standard CMOS electronics on a single silicon chip. The reason for wanting to integrate these devices is that the support electronics necessary to make an interesting, commercially viable, circuit could then easily be built using the surrounding silicon. One envisions making ultra dense digital memory circuits, neural networks, ultra high speed analog to digital converters and other high speed electronic circuits. In addition to making quantum devices, this material system could also be used to provide silicon on insulator technology and 3D electronics, which could be used to speed up standard devices in integrated circuits and allow for more complicated circuits respectively.

Quantum Devices

In Fig. 1.2a, we show a resonant tunneling diode (RTD). This device was invented some 24 years ago[7] and demonstrated shortly thereafter[8]. The device had since been built with great success in many configurations in III-IV material systems[9], but the efforts to make them work in silicon had been less fruitful. For instance, these devices had been built in the Si/SiGe material system, but the peak-to-valley ratio was only 1.2 for n-type RTDs[10] and 1.5 for p-type[11] RTDs at room temperature. For a generic I/V curve of these devices with the peak-to-valley ratio defined, see Fig. 1.2b.

While tunneling and device theory are beyond the scope of this thesis, we

Resonant Tunneling Diode
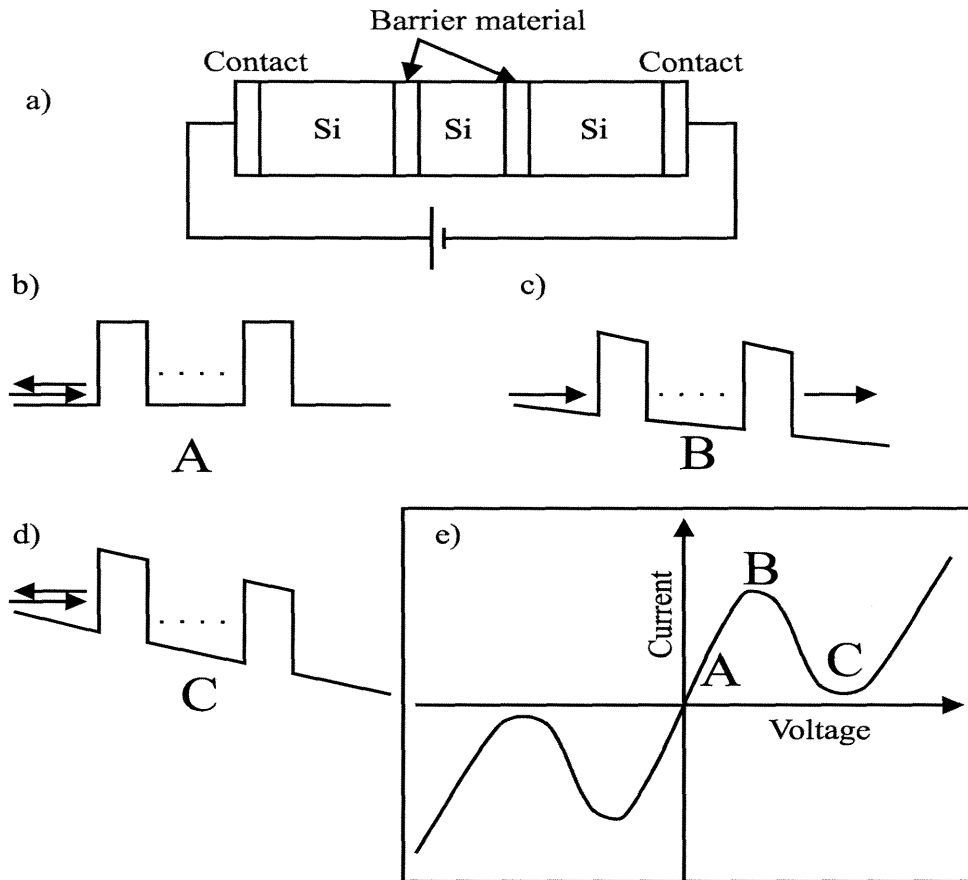
Figure 1.1: (a) RTD. (b) Schematic band diagram of an RTD. An electron incident from the left (at low bias) will have a very low transmission coefficient through the structure, as there is no state available in well region between the two barriers. (c) By biasing the device, one can line up the energy of the incident electrons with one of the semi-bound state of the well. (d) By increasing the bias further, the incident electron energy no longer is lined up with the semi-bound state in the well. (e) The resulting I/V curve.

provide a simple explanation for how these devices work here. In Fig. 1.1b we show a schematic band diagram of an RTD. An electron incident from the left (at low bias) will have a very low transmission coefficient through the structure, as there is no state available in well region between the two barriers. The result is that the current increases slowly with the voltage. This region of the I/V curve in Fig. 1.1e is denoted by A. By biasing the device, one can line up the energy of the incident electrons with one of the semi-bound state of the well (see Fig. 1.1c). In this case the electron is easily transmitted through the device. This corresponds to point B in the I/V curve shown in Fig. 1.1e. If the energy of the incident electron is increased further (see Fig. 1.1d), the transmission coefficient becomes smaller as there is no state in the well that can transmit the electron (point B in Fig. 1.1e). Thus, the current through device decreases as the voltage increases giving rise to negative differential resistance shown in the I/V curve as a downward slope. In order to achieve good confinement of the semi-bound states in the well, the conduction band offset has to be at least an order of magnitude larger than kT. The negative resistance region of the I/V curve can be used to make ultra fast amplifiers and memory circuits.

1.2.3 Growth

Having described a possible application of the material system, we now turn back to fabrication issues. From a growth point of view, the important thing to notice is that in order to build this device, one has to grow the structure using two different materials (see Fig. 1.2a). As one can see in the figure, the barrier material has to be grown on the substrate material and then the well/substrate material has to be grown on top of the barrier material. Given that we want to use a silicon substrate, we are constrained to materials that match silicon in several respects. The list below show some, but by all means not all, of the constraints that have to be met:

a)   RTD Device Structure   **b)   RTD I/V Curve**

| Metal Contact |
| Silicon Cap |

Barrier Mat.

Silicon Well

Barrier Mat.

| Silicon buffer/wafer |
| Metal Contact |

Peak-to-valley-ratio = I_{peak} / I_{valley}

Current

I_{peak}
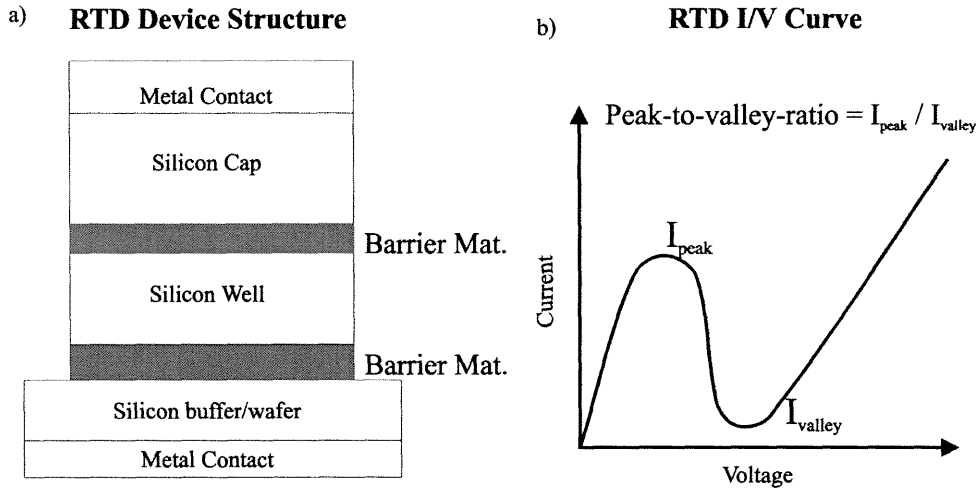
I_{valley}

Voltage

Figure 1.2: RTD device structure and I/V curve with definition of peak-to-valley voltage.

- Lattice constant match

- Appropriate band alignments

- Thermal stability up to normal silicon processing temperatures

- Thermal expansion coefficient match

- Surface free energy match

From a practical point view, we also had to be able to evaporate the material in our MBE machine.

Calcium fluoride meet the first three requirements. The lattice match is pretty good (only 0.6% mismatch) and the band offsets are large in both the conduction and valence bands. The high melting temperature of CaF_2 also leads one to believe that it would remain stable during silicon processing temperatures. Unfortunately, the thermal expansion coefficients are very different. In fact, at the growth temperature, the lattice mismatch increases to about 2.5%. This mismatch is probably still small enough to maintain good crystal quality, provided that the barriers are

kept thin enough (below critical thickness). In contrast, we believe that the surface free energy mismatch turns out to be fatal.

CaF$_2$ Growth on Silicon

Thanks to the favorable matches mentioned above, CaF$_2$ grows nicely on silicon(111)[2]. We used LEED to characterize the CaF$_2$ and it shows the expected 1x1 reconstruction signifying good ordering of the surface. This is partially due to the low free energy (350 ergs/cm^2) of the CaF$_2$(111) surface, as compared to the high (1200 ergs/cm^2) free energy of the silicon(111) surface. If the growth process is close to thermal equilibrium, the system will strive to reach the state of lowest Helmholtz surface free energy. Since the CaF$_2$ has a much lower surface free energy, the thermodynamic driving force would tend to maximize the low surface free energy CaF$_2$ surface and completely cover up the high energy silicon surface.

Silicon Overgrowth

Here, the difficulties begin. AFM micrographs show that the silicon does not wet the CaF$_2$ surface. Instead, the silicon forms hexagonal islands and defects are generated as these islands coalesce. One possible reason for the silicon to islands is that the system reaches its lowest free energy by minimizing the silicon surface area and maximize the CaF$_2$ surface area.

1.2.4 Experiment

In order to alleviate the islanding, we modified the CaF$_2$ surface prior to silicon overgrowth by irradiating the surface with low energy electrons. It has been shown that low energy electron radiation desorbs fluorine as F$^+$ from CaF$_2$(111), creating a calcium rich surface with an ordered array of surface F-centers[6]. This array of F-centers will have a higher surface free energy than the normal CaF$_2$ surface and should thus favor 2D growth or at least lower the contact angle in 3D growth of

silicon on CaF_2.

We then studied the surface morphology of silicon, grown on top of the modified CaF_2/Si surface, using atomic force microscopy (AFM), x-ray photoelectron spectroscopy (XPS) and low energy electron diffraction (LEED). We found an optimal range of electron beam exposure for high temperature (650°C) growth of the silicon overlayer that minimizes the roughness of the silicon overlayer. The observed hexagonally shaped microcrystals formed by the silicon during high temperature growth were explained by a simple model based on thermodynamics.

We observed a similar optimal range of exposures that minimized the surface roughness of the silicon overlayer during medium (575°C) and low (500°C) temperatures growth. We explained this based on kinetics.

1.2.5   Summary

In summary, we improved the surface morphology of silicon grown on calciumfluoride in an effort to make the silicon/calciumfluoride material system a basis for quantum device integration on silicon substrates. We reduced the roughness of silicon grown on CaF_2/Si using electron beam assisted molecular beam epitaxy. We found that the roughness of the silicon overlayer was minimized by exposing the CaF_2 to an electron dose of 1.0 mC/cm^2 in the high temperature case (650°C) before growing the epitaxial silicon overlayer. The medium (575°C) and low (500°C) temperature samples showed smoother surfaces at the cost of crystalline quality. The AFM results were consistent with the LEED and XPS data. We presented a simple model based on thermodynamics which explained the data well in the high temperature case. An explanation based on kinetics was put forward for the low and medium temperature cases.

Although these results indicate that it is currently impractical to manufacture RTDs, which require thin smooth films of silicon on CaF_2 through electron irradiation of the CaF_2 surface and kinetic constraints, there is some hope for this

material system. The most fruitful approach would probably be to find a substance that could either lower the Si−CaF$_2$ interface free energy or passivate the silicon surface during the growth. Hydrogen and antimony might be interesting candidates.

1.3 The Si/Si$_{1-y}$C$_y$ Material System

1.3.1 Background

Looking at column IV of the periodic system (C, Si, Ge, Sn, Pb), we see that one might consider alloys of the first two (C, Si) with one of the larger atoms (Ge, Sn, and perhaps Pb) a potential material system that would be suitable for silicon based electronics. Here, we consider the first three (C, Si, and Ge). Since the crystal structure is the same for these elements (diamond) and lattice constants increase monotonically (a_C=0.3567 nm, a_{Si}=0.543 nm, and a_{Ge}=0.5658 nm), it might be possible to generate device quality alloys that would be perfectly lattice matched to a silicon substrate.

Unfortunately, carbon does not easily mix with the other materials. The C-Ge phase diagram shows that the mutual solubilities are negligible and there is no evidence of germanium carbide formation[13]. Similarly, the solid solubility for carbon in silicon is in the range of 10^{-3} to 10^{-4} atomic %. However, in this case there is formation of silicon carbide and its many poly types. In contrast to the carbon alloys, the silicon germanium phase diagram shows no such miscibility gap. Thus, it is no surprise that while SiGe alloys with a wide range of composition have been grown on silicon substrates[15], high crystal quality Si$_{1-y}$C$_y$ alloys have been grown only for small y[14].

1.3.2 Potential Applications

In addition to the RTDs mentioned earlier, the SiGe/Si material system has produced devices such as HJBTs and p-channel FETs using the valence band offset. For a recent review of these devices, see Whall[15]. One of the main limitations of the system is that strain always have to be taken into account since SiGe alloys will have larger lattice constants than silicon. Another limitation is that while the valence band offset is large enough for device applications, the conduction band offset is negligible. The reason for this is that the compositional shift of the conduction band cancels the shift due to strain, when SiGe is grown coherently strained to silicon. While conduction band offsets can be achieved in the $Si/Si_{1-x}Ge_x$ system by growing tensile-strained layers on relaxed $Si_{1-x}Ge_x$ buffer layers, the incorporation of carbon may provide this desirable feature without the substantial defect densities and complicated processing inherent for growth on relaxed buffer layers.

By introducing carbon into the system, the cancellation mentioned above could perhaps be removed. The carbon could be used to increase the lattice constant of a SiGeC alloy to match the silicon and thus reduce the strain in the system. This would remove the shift in the conduction band due to strain and leave the system with a compositional shift in the conduction band which could lead to a significant conduction band offset. This offset would then open up the possibilities for electron, as opposed to hole, based devices such as n-RTDs without having to use strained layers.

1.3.3 Growth

As mentioned earlier, the miscibility gap in the C-Si binary alloy phase diagram make it difficult to grow these alloys with the carbon concentration required to obtain a substantial conduction band offset. We have found that surface of the growth roughens during MBE growth of $Si_{1-y}C_y$ on silicon(100) for carbon concentrations larger than 2%. To eliminate this roughening we employed a technique

called surfactant assisted MBE.

Surfactant Assisted Growth of $Si_{1-y}C_y$

In surfactant assisted MBE one adds an adsorbate, the surfactant, either before or during the growth. In general, the surfactant could play many roles. It could change the surface free energies of the materials at the growth front, relieve strain, or change the growth kinetics as to improve the growth. I think it is fair to say that the atomic level processes are not yet well understood. In our case we used Sb as a surfactant to reduce the roughening mentioned above.

To test the effectiveness of the Sb as a surfactant, we grew $Si/Si_{0.97}C_{0.03}$ superlattices on Si(001) substrates by surfactant assisted molecular beam epitaxy (MBE) and characterized them by *in situ* reflection high energy electron diffraction (RHEED), atomic force microscopy (AFM), transmission electron microscopy (TEM), and high resolution x-ray diffraction (HRXRD). The RHEED showed that, in absence of Sb, the growth front roughens during $Si_{0.97}C_{0.03}$ growth and smoothens during subsequent Si growth.

In contrast, when Sb was present, the growth front remained smooth throughout the growth. We confirmed this observation by cross-sectional (TEM) which revealed that for samples grown without the use of Sb, the $Si/Si_{0.97}C_{0.03}$ interfaces ($Si_{0.97}C_{0.03}$ on Si) were much more abrupt than the $Si_{0.97}C_{0.03}/Si$ interfaces. In the case of Sb assisted growth, there were no observable difference in abruptness between the two types of interfaces. AFM micrographs of the $Si_{0.97}C_{0.03}$ surface revealed features that could be the source of the roughness observed by RHEED and TEM.

Although our experiment gave no direct evidence on exactly what goes on at the growth front, we think that the surfactant changed the growth kinetics rather than energetics in this case. This is the case in the Sb assisted growth of germanium on silicon[6]. The reason for this is that the change in surface free

energy due to the carbon probably is fairly small considering that the carbon concentration was only about 3%. Furthermore, a reduction in the surface free energy of the $Si_{0.97}C_{0.03}$ layer would lead to increased islanding, contrary to our observation. Instead, we think that one or more of the species in the carbon flux disrupted the epitaxial growth of $Si_{0.97}C_{0.03}$ on Si. These species formed surface nucleation centers where diffusing adatoms could incorporate in competition with surface steps, resulting in 3D growth.

All of the multiple carbon species, which remained undissociated on the surface, are potential candidates for having nucleated the rough growth. The diffusion length of these dimers and trimers is expected to be negligible compared to that of the monomers because of the large activation energy due to the bond bending and stretching required for a dimer or trimer to move on the surface. Thus, while the monomers might diffuse to a step and thus contribute to step flow growth, the dimers or trimers will incorporate at the site of impingement and form nucleation centers.

The nucleation center density generated by the dimers and trimers was large enough for 3D growth to dominate over 2D step flow growth. We speculate that in the case of Sb assisted growth, where the surface stayed smooth throughout the growth, the surfactant assisted growth mechanism prevented the dimers and trimers from forming effective nucleation centers. The primary role of the Sb was to ride as a surface layer burying the carbon dimer and trimers. Although there was some Sb incorporation during growth, as measured by Rutherford backscattering spectrometry[1], the concentration of the incorporated Sb was too small to provide significant strain relief for the $Si_{0.97}C_{0.03}$ layers. Instead the growth kinetics was most likely modified. An impinging silicon adatom diffused on the Sb-layer until it reached a proper site. At that site, the adatom underwent an exchange with a surfactant atom and incorporated. Again, the carbon clusters did not diffuse on the

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[1]We would like to thank Maggie Taylor for the RBS measurement and analysis.

surface, rather they were incorporated immediately by some exchange mechanism. Since direct contact between Si adatoms and the carbon clusters was reduced, the clusters no longer served as effective nucleation centers and the growth stayed relatively smooth as shown by AFM and the streaked RHEED pattern.

1.3.4 Summary

In order to grow smooth layers of high carbon content (larger than 2% carbon) silicon carbon on silicon, we employed surfactant assisted molecular beam epitaxy using Sb as the surfactant. The silicon/silicon carbon, like the silicon/calciumfluoride material systems could be used to integrate quantum devices like RTDs on standard silicon substrates. We grew $Si/Si_{0.97}C_{0.03}$ superlattices on Si(001) substrates and characterized them by *in situ* RHEED, AFM, TEM, and HRXRD. The RHEED showed that, in absence of Sb, the growth front roughened during $Si_{0.97}C_{0.03}$ growth and became smooth again during subsequent Si growth.

In contrast, when Sb was present, the growth front remained smooth throughout the growth. We confirmed this observation by TEM which revealed that for samples grown without the use of Sb, the $Si/Si_{0.97}C_{0.03}$ interfaces ($Si_{0.97}C_{0.03}$ on Si) were much more abrupt than the $Si_{0.97}C_{0.03}/Si$ interfaces. In the case of Sb assisted growth, there were no observable difference in abruptness between the two types of interfaces. AFM micrographs of the $Si_{0.97}C_{0.03}$ surface revealed features that could be the source of the roughness observed by RHEED and TEM.

Thus, the surfactant assisted growth method worked well for $Si_{0.97}C_{0.03}$ growth on silicon(100). This result, if it can be extended to higher carbon concentrations, could greatly extend the reach of the SiGeC material system.

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Chapter 2

Introduction to the SRAM/MISS

2.1 Introduction

In this chapter, we introduce the third topic of the thesis – the static random access memory (SRAM) based on a memory cell consisting of a metal insulator semiconductor switch (MISS) in series with a resistor. This SRAM was originally proposed by Harold Levy[2]. We provide background and motivation for the theoretical and experimental study of the influence of oxide thickness on the I/V of the MISS device presented in chapter 5. We will motivate the research by describing current limitation of the conventional SRAM architecture and describe Harold's new approach based on the memory cell mentioned above. In addition to describing the device and the cell, we will also discuss the appropriate reading and writing addressing schemes. Finally, we will provide an overview of the detailed oxide thickness study.

2.1.1 Background

The standard static random access memory (SRAM) cell is large and fast. As you can see in Fig. 2.1, it takes at least four transistors to make the cell itself and then another transistor to address the cell. The addressing transistor is necessary as
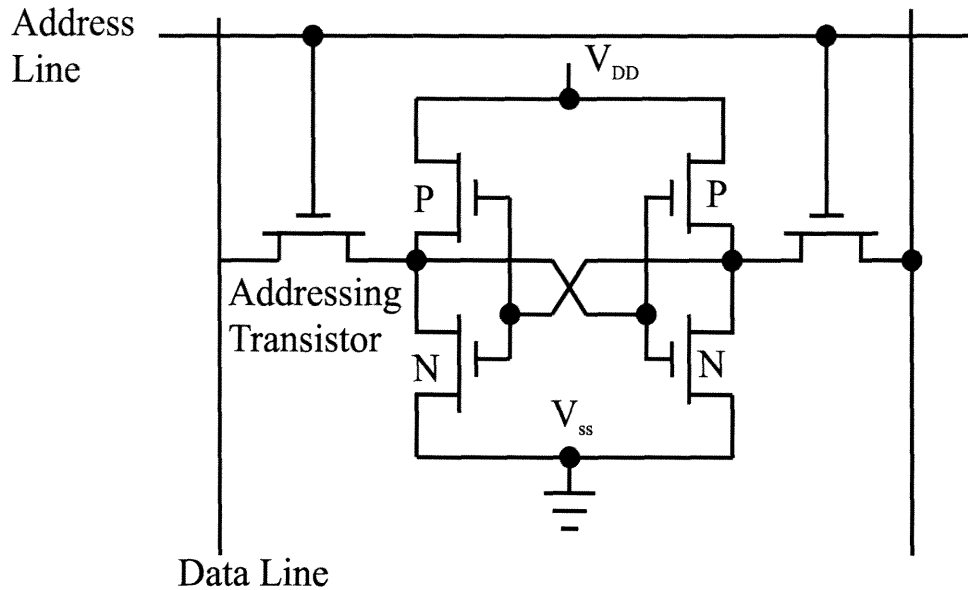
Figure 2.1: The conventional SRAM cell consists of a bistable flip-flop made of four transistors. The two extra addressing transistors serve to isolate the cell from the other cells in the memory. A bit is sensed by detecting a certain amount of charge (around 100fC). As the memory cell can source a large amount of current through the saturated transistors, it is fast.

the bit is stored as a voltage state of a bistable flip-flop and thus would short out, unless isolated. A bit is sensed by detecting a certain amount of charge (around 100fC). Thus, the time it takes to detect whether the bit is one or zero is inversely proportional to the current sourced by the memory cell. As the memory cell can source a large amount of current through the saturated transistors, it is fast.

A dynamic random access (DRAM) memory cell is, *au contraire*, small and slow. The design consists of a capacitor and an isolation transistor (see Fig. 2.2). The reason for the cell being slow is that the current is limited by the discharge characteristics of a capacitor; i.e., the current decays exponentially. Another problem with this design is that the cell has to be refreshed as the capacitor slowly leaks out the stored charge.
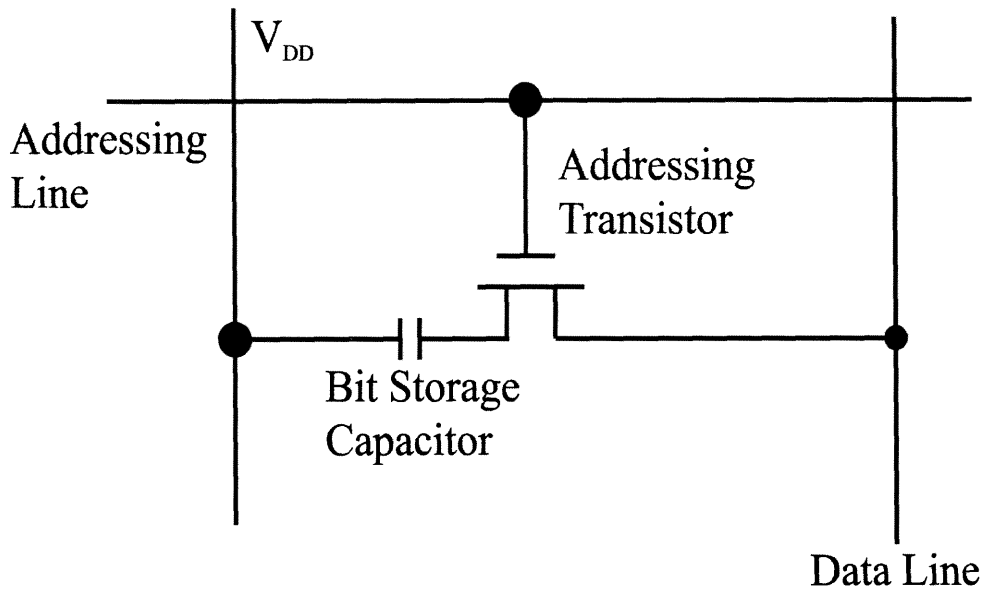
Figure 2.2: The conventional DRAM cell consists of a capacitor and a transistor. The addressing transistor isolates the cell from the other cells in the memory. The cell is small, but slow due to the discharge characteristics of the capacitor.

Given the need for large amounts of fast memory, current memory architecture relies on fast, but expensive, on-CPU-chip SRAM cache memory and off-chip large and relatively cheap DRAM memory. This way, most of the CPU reads and writes are serviced fast while a large amount of memory is available. The benefit of our approach is that the SRAM density can be increased by a factor of about 20. This would allow up to 5MB of SRAM cache on a CPU instead of today's 256kB. Or, one could decrease the area now used for SRAM which is up to 50% now to less than 5%. If our revolutionary memory design could be fabricated at a cost similar to that of standard SRAM, there could be an immediate worldwide commercial demand for the product.
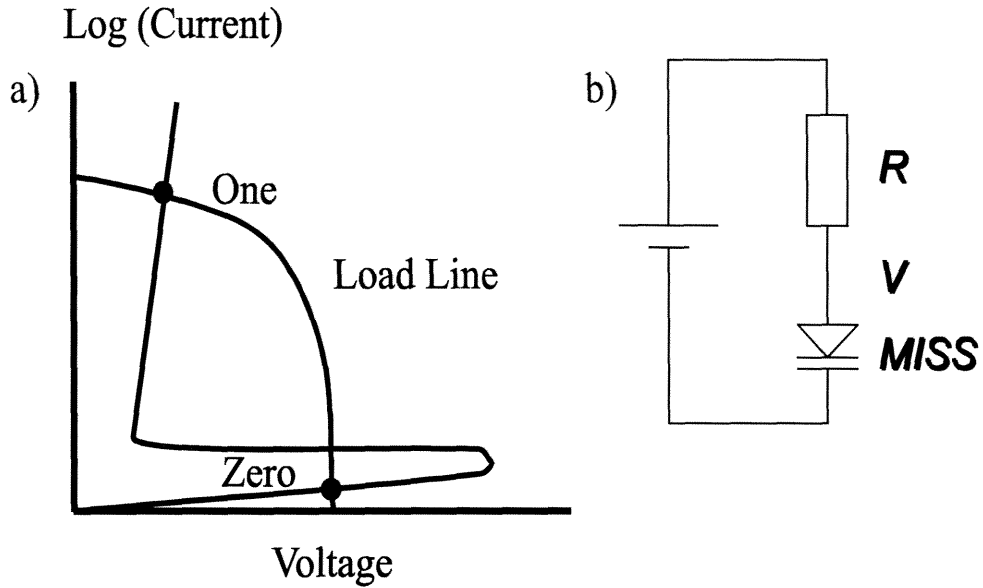
Figure 2.3: The SRAM memory cell based on a MISS.

2.1.2 The Memory Cell

The basic memory cell in our scheme is a metal insulator semiconductor switch (MISS) in series with a resistor where the bit is stored in current state rather than a voltage state. This allows for a transistor less addressing scheme leading to a fast memory with a small footprint.

The MISS, invented some 24 years ago by Yamamoto[1], is a two terminal device with an current-voltage (I/V) curve which exhibits a high and a low impedance state, as seen in Fig. 2.3a. The simple memory cell is shown in Fig. 2.3b with the load line solution depicted in Fig. 2.3a. The low current state would correspond to a "zero" and the high current state to a "one." The memory would be built by arranging these cells in a grid with proper addressing electronics along the sides of the grid.

a)

b)

Log (I)

$V_s+\delta$

V_s

Voltage
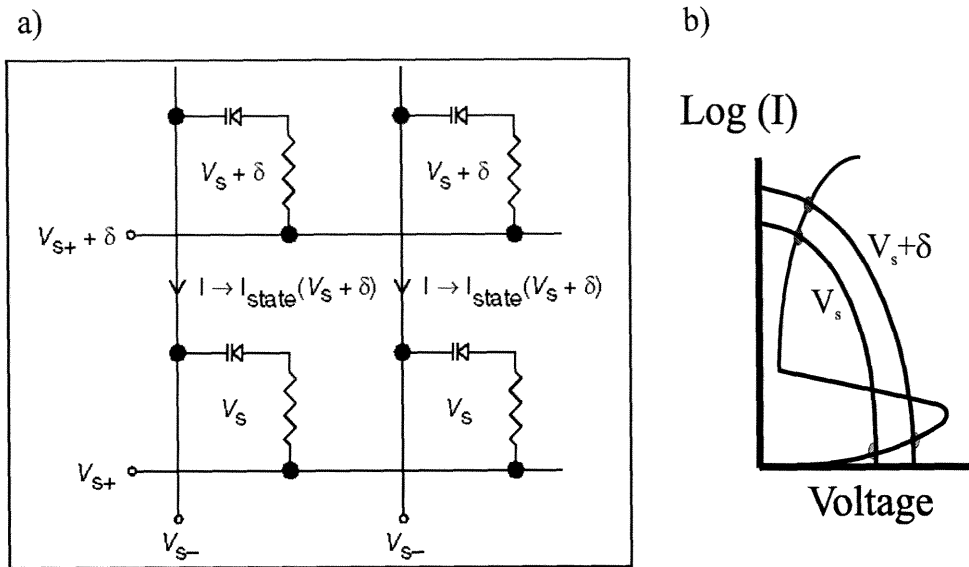
Figure 2.4: Reading the memory cell.

2.1.3   Addressing Scheme

Read

To read the cell, say the one in the upper left corner in Fig. 2.4, one would bias the corresponding horizontal line slightly higher than the quiescent bias required to maintain the state and then measure the current in the left vertical line. If the state were a "one," then the slight increase in voltage would result in a large increase in the current and thus a large amount of charge delivered to the sense amplifier which would read a "one". On the other hand, if the state were a "zero," the current would hardly increase, leading to a zero state being read. The time it would take to read the state would be determined by the charge necessary to detect a "one" divided by the amount of current sourced in the "one" state.

Write

To write a "one" to the upper right cell in Fig. 2.5, one would bias the corresponding horizontal and vertical lines positively ($+\Delta$) and negatively ($-\Delta$) respectively.

a)

b)
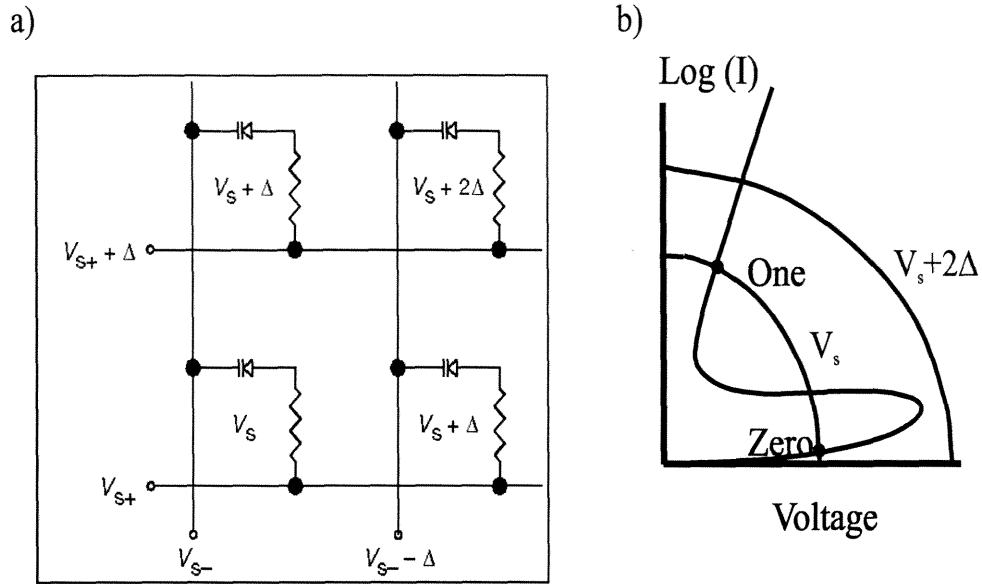
Figure 2.5: Writing to the memory cell.

The cell would see a 2Δ increase in bias, which would be large enough to switch the state from a "zero" to a "one." The other cells on the vertical and horizontal lines in question would only see a bias of Δ which would not be enough to change their states. To write a "zero" the biases would be reversed.

2.2 MISS Experiment

The device consists of a metal/SiO_2/Si(n)/Si(p$^+$)/metal structure (see Fig. 2.6, where the insulator is thin enough to pass a direct tunnel current, but not so thin that holes cannot accumulate at all.

Although the metal insulator semiconductor switch had been investigated for quite some time, there had been no systematic report on the influence of the oxide thickness on the I/V curve. In chapter 5 we describe our experiment determining this dependence both experimentally and by simulation.

We fabricated four types of metal insulator semiconductor switches where the

Device Structure

Aluminum
Tunnel oxide - SiO$_2$
n-type Silicon
p-type Silicon substrate
Aluminum

Figure 2.6: The MISS device consists of a thin insulator layer on an n-p (or p-n) junction. The top and back contacts are made of aluminum. The figure is not drawn to scale.

only intentional difference was the thickness of the oxide. There were three processing steps. First, we cleaned a silicon chip consisting of n-type Si epi on a p-type Si substrate. Next, we grew the oxide by rapid thermal oxidation. Finally, the contacts were sputtered and defined by photolithography.

The I/V curve showed the expected switching behavior although the details such as switching currents and voltages did not agree with simulations. Despite the disagreement between the experiment and the theory, we found that the simulation provided some insight to how the device operates. We observed that the I/V curves of these devices are very sensitive to the oxide thickness. The onset of the negative resistance region in the curve is so sensitive to the electron and hole tunneling currents that these devices could be used to characterize ultra thin oxides.

Another important observation was that the I/V curve changed after the first switching event and then remained fairly constant. Extremely high current densities (10^3 A/cm^2) could be driven through the ultra thin oxides without changing the device characteristics. We believe this is the highest, non-destructive current density through an oxide reported to date.

2.3   Summary

In this chapter, we introduced a static random access memory (SRAM) concept in which a Metal Insulator Semiconductor Switch (MISS) device is the basis for the memory cell. We showed that this device, in series with a resistor, could be used with a transistor less addressing scheme to increase the SRAM density by a factor of 20 compared to current technology.

The influence of the oxide thickness on the I/V curve of the MISS device was studied both experimentally and by simulation, and we found that the I/V curve showed the expected switching behavior although the details such as switching currents and voltages did not agree with simulations. Despite the disagreement between the experiment and the theory, the simulation provided some insight into how the device operates. We observed that the I/V curves of these devices are very sensitive to the oxide thickness.

Another important observation was that the I/V curve changed after the first switching event and then remained fairly constant. Extremely high current densities (10^3 A/cm^2) could be driven through the ultra thin oxides without changing the device characteristics. We believe this is the highest, non-destructive current density through an oxide reported to date.

Although the fabricated devices still need to be refined in order to serve as the basis for an SRAM with acceptable specifictions in terms of power consumption and speed, we have showed that this approach to increasing SRAM density is promising.

Bibliography

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[2] T. Yamamoto and M Morimoto, *Appl. Phys. Lett.* **20,** 269 (1972).

Chapter 3

Surface Morphology of Silicon Grown on CaF$_2$/Si By Electron Beam Assisted MBE

3.1 Introduction

3.1.1 Chapter Abstract

The surface morphology of silicon, grown on epitaxial CaF$_2$/Si by electron beam assisted MBE, is studied using atomic force microscopy (AFM), x-ray photoelectron spectroscopy (XPS) and low energy electron diffraction (LEED). We find an optimal range of electron beam exposure for high temperature (650°C) growth of the silicon overlayer that minimizes the roughness of the silicon overlayer. The observed hexagonally shaped microcrystals formed by the silicon during high temperature growth are explained by a simple model based on thermodynamics.

We observe a similar optimal range of exposures that minimizes the surface roughness of the silicon overlayer during medium (575°C) and low (500°C) temperatures growth. We present an explanation for this based on kinetics.

3.1.2 Motivation and Background

As discussed in chapter 1, one way of realizing ultra dense digital memory circuits, neural networks, and high speed electronics is to integrate quantum devices such as resonant tunneling diodes which exhibit negative differential resistance with standard VLSI silicon circuitry. The Si/CaF_2 material system is a promising candidate for this integration effort since the lattice mismatch is small (0.6% at room temperature) and the crystalline structures are similar. Another application of this material system is as the insulator in silicon on insulator. Consequently, the system has been studied extensively and it has been found that while CaF_2 grows in a two dimensional epitaxial fashion on silicon (111), silicon islands on CaF_2 [1]. In this chapter, we report on our efforts to reduce the tendency of the silicon to island by using a technique known as electron beam assisted molecular beam epitaxy (EB MBE). This technique has been used to improve growth of both Ge [2] and GaAs [3] on CaF_2, but as far we know, there has not been any reports, apart from our own [4][5], on its use in growth of silicon on CaF_2.

In EB MBE, the CaF_2 surface is exposed to electrons to desorb fluorine from the CaF_2, prior to silicon overgrowth. It has been shown that low energy electron radiation desorbs fluorine as F^+ from $CaF_2(111)$, creating a calcium rich surface with an ordered array of surface F-centers[6]. A detailed mechanism for the desorption process which involves excitations of the Ca $3p$ core level has been proposed by Chakarian [7]. The array of F-centers will have a higher surface free energy than the normal CaF_2 surface and should thus favor 2D growth or at least lower the contact angle in 3D growth of silicon on CaF_2.

3.1.3 Outline of Chapter

In the experimental section we describe the sample structure and growth. LEED, AFM, and XPS data is presented in the characterization section, and in the discussion section we explain these results using a simple thermodynamical model for

the high growth temperature case and an argument based on kinetics for the low temperature results. In the final section, we summarize the results and suggest future directions for research is this area.

3.2 Experiment

3.2.1 Sample structure

The samples consist of three layers: 50 nm silicon on 10 nm CaF_2 on a 100 nm thick silicon buffer grown on a silicon (111) wafer. The reason for choosing a thick CaF_2 layer is to prevent the electron beam from penetrating it. Early TEM studies showed that 10 nm is sufficient for this purpose. Since the AFM measurements were performed in air, we chose a relatively thick (50 nm) silicon overlayer to ensure that the surface features due to oxidation are about a factor of 10-50 times smaller than the features due to the electron beam exposure.

3.2.2 Sample preparation

MBE Growth

Before growth, we degreased the 2 inch (boron doped, 3×10^{18} cm^{-3}) silicon wafer and dipped it in a 25% HF solution in order to remove the contaminated native oxide and terminate the surface with hydrogen. Samples were grown at three different substrate temperatures during silicon deposition. The high temperature sample was grown at 650°C, the medium temperature sample at 575°C, and the low temperature sample was grown at 500°C. During CaF_2 deposition, the substrate temperature was kept at 700°C for all samples. Each wafer was exposed to the electron beam at four different locations in order to reduce scatter in the data due to variations in surface preparation and growth conditions. The total time required for the 4 exposures was about 1.5 hours for each sample. The background

pressure in the MBE machine was about 10^{-9} Torr during electron beam exposure and 10^{-8} Torr during growth. The deposition rates were 0.05 nm/s for the silicon growth and 0.04 nm/s during CaF_2 growth.

Electron Beam Exposure

The buffer layer exhibited the customary sharp 7x7 LEED pattern. This pattern changed to the expected 1x1 pattern after the CaF_2 had been deposited. To expose the surface, we defocused the LEED beam to a spot diameter of about 4 mm and set the dose rate to 0.85 $\mu A/cm^2$ for the samples with doses ranging from zero to 1.0 mC/cm^2 and 12 $\mu A/cm^2$ for the samples with doses ranging from 0.5 to 50 mC/cm^2. The dose rate was measured by shuttering the electron beam and measuring the current from the shutter to ground. The LEED pattern remained the same during the exposure (except the spots were larger due to the defocusing) for the doses up to 1.0 mC/cm^2. The unchanging LEED pattern shows that the surface remains ordered, indicating that the F-centers created by fluorine desorption form an ordered array [6]. For higher doses the LEED pattern lost contrast, which we interpret as a disordering of the CaF_2 surface by the electron irradiation. The low temperature silicon overlayer exhibited a weak 1×1 whereas the medium and high temperature silicon overlayers exhibited strong 1x1 patterns. In all cases, the spot size was larger than that of the silicon buffer layer.

3.3 Characterization

3.3.1 Atomic Force Microscopy

Figure 3.1 shows a 3D view of the surface morphology (as measured by AFM) of the silicon overlayer grown at high temperature with zero electron dose (since there are electron guns in the MBE system, there is a background of electrons, but this dose is compared to the doses used in this experiment). As you can see in the
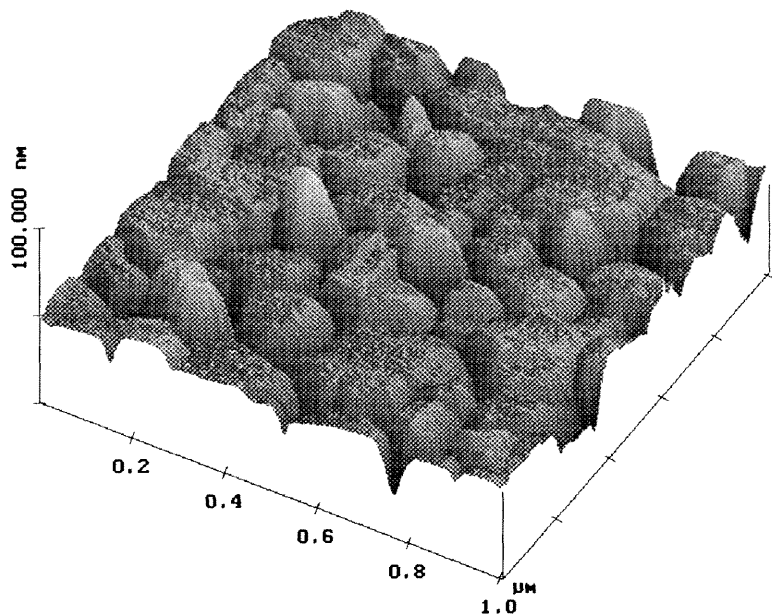
Figure 3.1: AFM micrograph of silicon grown on $CaF_2(111)$ by standard MBE at high temperature (650°C). This 3D view emphasizes the roughness of the silicon layer; note that the scale along the x and y axes are 10 times that of the z axis. Given that the nominal thickness of the silicon overlayer is 50 nm, one sees that the silicon is not wetting the CaF_2; there are islands and the coverage is incomplete. The 2D view of the same sample, shown in figure 3.2, emphasizes the hexagonal shape of the islands.

2D view (figure 3.2), the islands are about 100-300 nm in diameter and many are hexagonal. The sides of the islands are aligned along what we believe to be the {011} directions of the substrate.

The contact angles (defined in figure 3.8c) of the islands vary over a large range (0°-50°). This variation is probably due to the fact that the islands are in various stages of coalescing at the Si/CaF_2 interface. Experimentally we see that, in general, the stronger the coalescence, the lower the contact angle. "Free standing faces," faces that are comparatively far from other islands, have a contact angle of 39° ± 5°.

The surface morphology of the zero electron dose medium temperature sample is similar to that of the zero dose high temperature sample, except that the typical
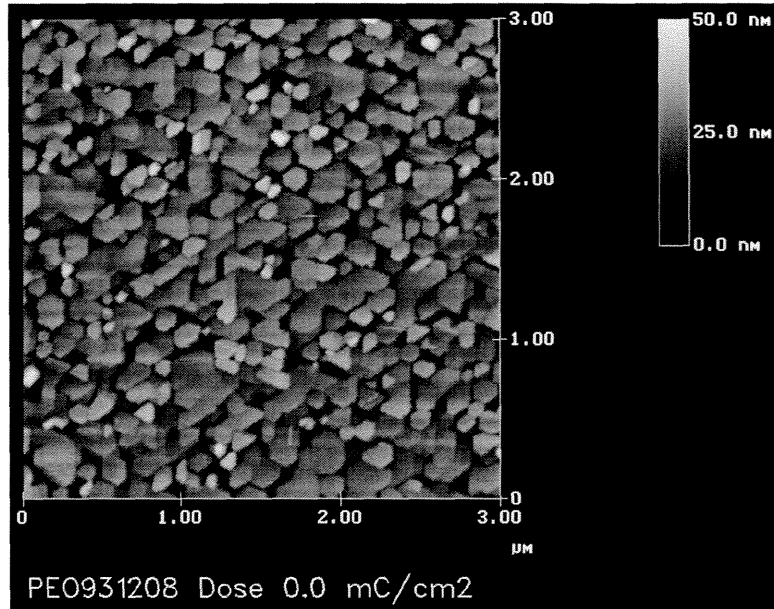
Figure 3.2: AFM micrograph of silicon grown on $CaF_2(111)$ by standard MBE at high temperature (650°C). This 2D view shows that many of the islands are hexagonal and that sides of the islands are aligned along what we believe to be the {011} directions of the substrate.

island size is smaller (100 - 200 nm diameter).

Figure 3.3 shows the morphology of the silicon overlayer grown at low temperature with zero electron dose. Unlike the high and medium temperature samples, this sample has no well defined islands and the silicon overlayer appears to cover the CaF_2 completely.

The surface morphology of the high temperature sample irradiated with a dose of 1.0 mC/cm^2 is shown in figure 3.4. The islands have the same general shape and size distribution as in the high temperature zero dose case, as you can see in figure 3.5, but they have coalesced to a large degree and the surface is much smoother than that of the zero dose. There are fewer islands that are comparatively far from other islands and thus the contact angles are smaller; for the "free standing faces" the contact angles are 32° ± 5°.

The island shape changes in the medium temperature case with an electron dose
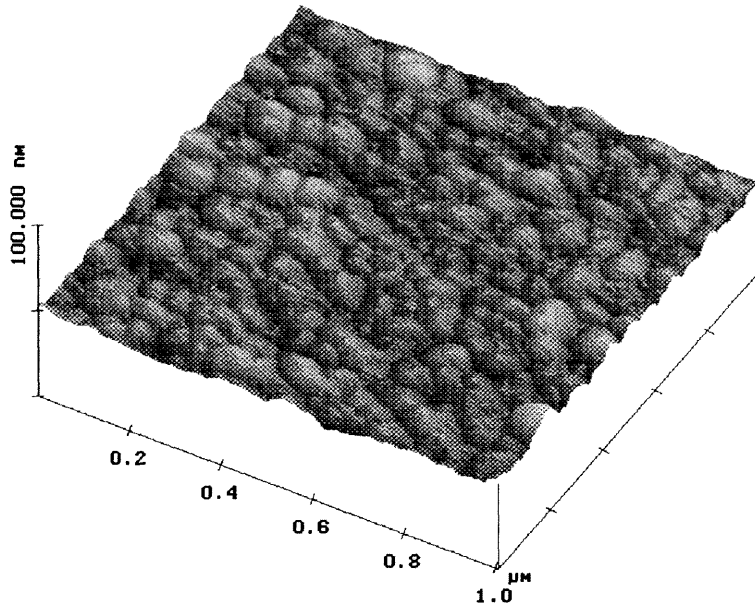
Figure 3.3: AFM micrograph of silicon grown on $CaF_2(111)$ by standard MBE at low temperature (500°C). In contrast to the high temperature case (figure 3.1), there are no well defined islands and the surface is relatively smooth.
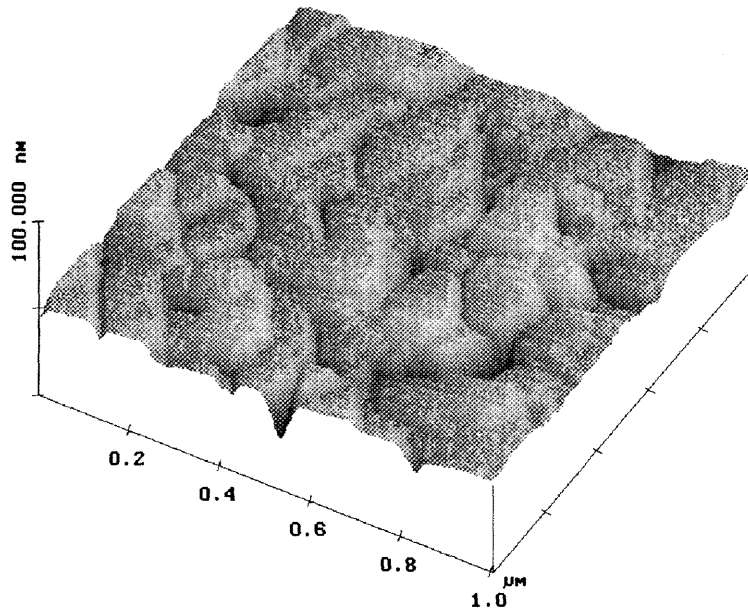
Figure 3.4: AFM micrograph of silicon grown on $CaF_2(111)$ by EB MBE at 650°C. Dose 1.0 mC/cm^2. Compared to the zero dose case (figure 3.1), this sample appears smoother although it still is islanded.
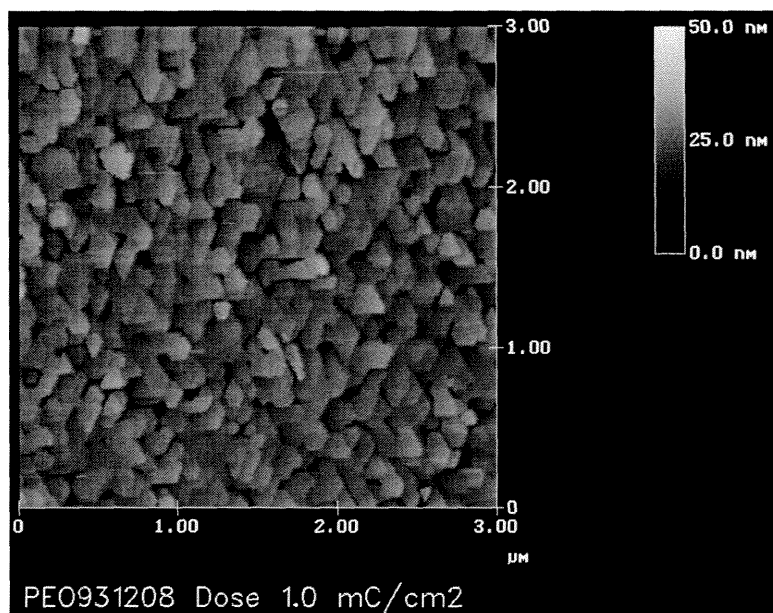
Figure 3.5: AFM micrograph of silicon grown on $CaF_2(111)$ by EB MBE at high temperature (650°C). Dose 1.0 mC/cm^2. This 2D view shows that the islands have the same hexagonal shape as the non irradiated high temperature sample (figure 3.2).

of 1.0 mC/cm^2. As you can see in figure 3.6, the islands have lost their hexagonal shape. The triangular shapes are due to the morphology of the underlying CaF_2. The smoothest overlayer was obtained with an electron dose of 0.5 mC/cm^2 in the low temperature case, but the difference in roughness and morphology between this case and the zero dose case is small.

The high temperature and high electron dose cases can be characterized as follows. At a dose of 10 mC/cm^2, the islands are shapeless, tall and spaced far apart. The islands do not to seem to have any specific crystal faces, instead their shape appears to be flattened spheres. In general, they stand about 50 nm tall with base diameter of about 200 nm and the spacing between them is about 2.5 μm. All of these values are rough means with large (50% of mean) standard deviations. The surface between the islands does not show any specific crystalline faces either. The reason for this change in surface morphology is probably due to the CaF_2
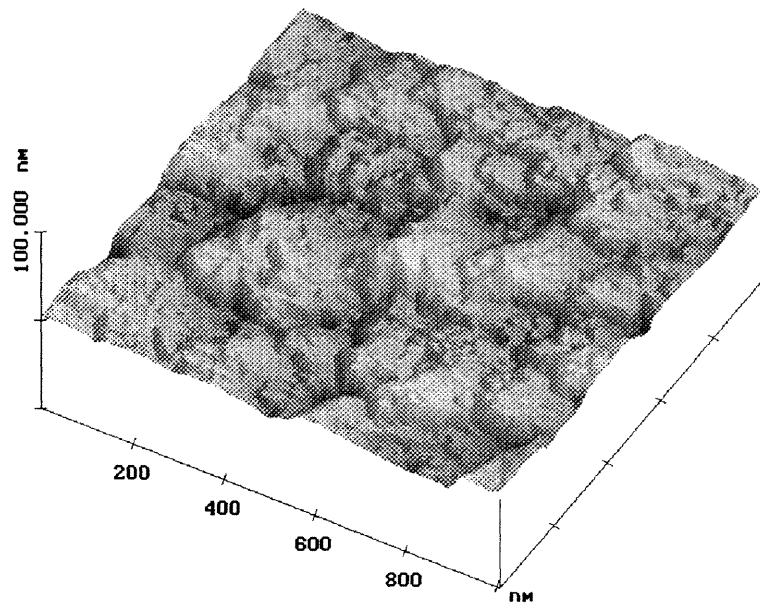
Figure 3.6: AFM micrograph of silicon grown on $CaF_2(111)$ by EB MBE at medium temperature (575°C). Dose 1.0 mC/cm^2. At this temperature, the silicon surface seems to be continous (the hexagonal islands have disappeared). The triangular shapes are due to the morphology of the underlying CaF_2 layer.

surface being randomized by the electron beam as indicated by the LEED. At a dose of 50 mC/cm^2, there are 40 nm deep triangular pinholes spaced about 1 μm apart instead of islands. The surface between the holes also shows triangular features. Again, we think that the damage done to the CaF$_2$ during the electron beam exposure is the reason for this change in surface morphology.

Since the histograms of the AFM micrographs acquired in the constant force mode are unimodal and gaussian-like, the root mean square (RMS) of the data is a good measure of the surface roughness. The measured roughness depends not only on the surface morphology, but also on the magnitude of the force, the scanning rate, and the condition of the tip. Thus, to ensure that the measurements were quantitatively comparable, we used a small repulsive force (8 - 25 nN) and a slow scan rate (15 min/image). To check for tip modification, we scanned a calibration sample between each roughness measurement. Figure 3.7 shows that the roughness is significantly lower for the irradiated samples in the high temperature case (the lines drawn in the picture are there only to guide the eye). The roughness exhibits a broad minimum followed by an increase in roughness at 10 mC/cm^2. In the medium temperature case, the roughness also decreases with increased electron dose. In the low temperature case, the roughness has a broad but shallow minimum around 1.0 mC/cm^2.

3.3.2 X-ray Photoemission Spectroscopy

The CaF$_2$/Si XPS peak ratios for the high temperature case, shown in table 3.1, support the notion that the silicon nearly covers the CaF$_2$ in the 1.0 mC/cm^2 case whereas the coverage is incomplete in the zero dose case. The fluorine/silicon ratio is largest in the zero dose and diminishes significantly for the 1.0 mC/cm^2 surface. After sputtering about 3 nm, the calcium and fluorine peaks vanish in all but the zero dose case. This is consistent with the model that the zero dose morphology consists of tall islands with valleys between whereas the CaF$_2$ surface in the 1.0

Surface roughness versus electron dose
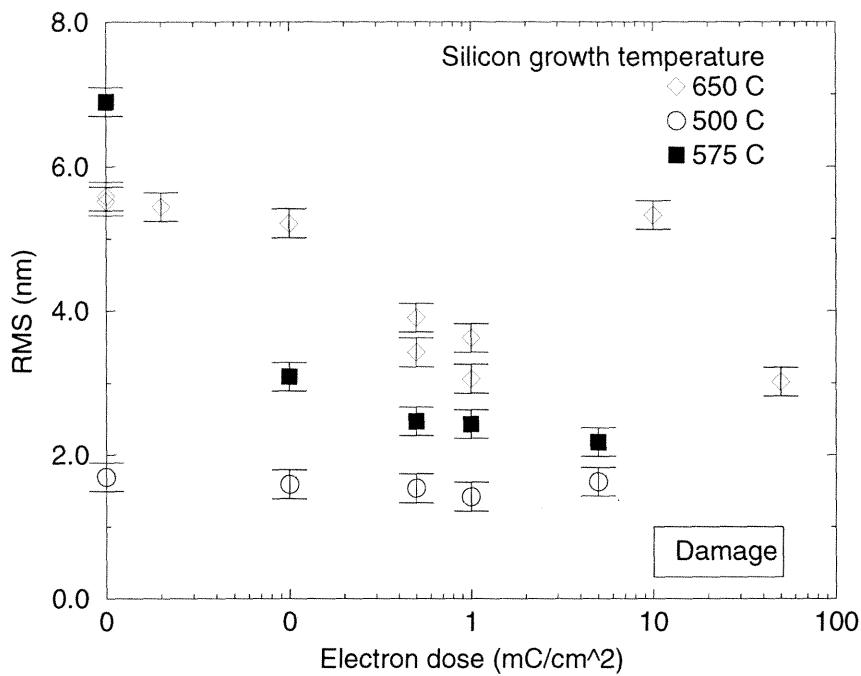
Figure 3.7: In this figure, we show RMS of the silicon overlayer versus the electron dose used in the EB MBE growth step for three different substrate temperatures. For the high and medium temperature cases, we see that there is a large improvement in terms of roughness for electron doses around 1 mC/cm^2. The roughness increases at a dose of 10 mC/cm^2 due to damage to the CaF$_2$ layer caused by the electron dose. At 50 mC/cm^2, the damage is more severe and the surface morphology is completely different. The surface is relatively smooth in the low temperature case and there is no significant change in surface morphology due to the electron dose.

Table 3.1: Calcium to silicon and fluorine to silicon XPS peak ratios of silicon grown on CaF_2 using electron assisted MBE (EB MBE) at high temperature (650°C). The dose refers to the electron dose used in the EB MBE growth. The samples were sputtered about 3 nm; the table shows the ratios both before and after the sputtering.

Dose	Ca/Si		F/Si	
(mC/cm^2)	pre sputter	post sputter	pre sputter	post sputter
0	0.45	0.07	0.45	0.13
1	0.30	0	0.07	0
10	0.33	0	0.14	0
50	0.33	0	0.04	0

mC/cm^2 case is nearly completely covered with silicon. The tall islands might shield the CaF_2 during sputtering, thus only the zero dose case shows calcium and fluorine peaks after sputtering. The calcium to silicon ratio is about the same for all samples before sputtering which is explained by the fact that calcium is known to surf on top of silicon [8]. The AFM micrographs show that there are valleys that probably reach down to the CaF_2 layer in the zero dose case, but not in the 1.0 mC/cm^2 case. Since this agrees well with the model explaining the XPS data, we conclude that the silicon almost covers the CaF_2 completely in the 1.0 mC/cm^2 case whereas the coverage is incomplete in the zero dose case.

At 10 mC/cm^2, in the high temperature case, the pre sputter fluorine to silicon XPS peak ratio increased from the value at 1 mC/cm^2. Since we expect the fluorine to silicon ratio to decrease monotonically with increased electron dose in the absence of shadowing effects, the increase in the ratio is most likely due to less complete coverage. This is supported by the extraordinary islanding observed by AFM. At 50 mC/cm^2, the pre sputter fluorine to silicon XPS peak ratio decreases. This is probably due to the large electron dose having desorbed most of the fluorine.

3.4 Discussion

In the high temperature case, we can explain the observed crystal shape and roughness with a simple model based on thermodynamics. In this model, the electron dose creates an ordered array of F-centers that increases the surface free energy, favoring lower contact angles and a smoother surface morphology. If one assumes that the growth process is close to thermodynamic equilibrium and that the shear stress is small near the interface, the surface morphology can be determined by two conditions. The first one is that the Helmholtz surface free energy is minimized and the second one is the contact angle between the surface and the epilayer is determined by the force balance of the respective surface tensions [9]. The minimization condition determines the shape of the silicon islands, and the contact angle force balance allows us to estimate the surface tensions of the interface and the irradiated CaF_2.

The measured surface free energies are approximately $1240\,ergs/cm^2$ and $450\,ergs/cm^2$ for Si(111) and CaF_2(111) respectively [10]. Thus, in the case of CaF_2 growth on silicon, the surface free energy is minimized by the CaF_2 covering the silicon in a 2D fashion. On the other hand, in the case of silicon growth on CaF_2, the free energy is minimized by 3D growth of the silicon on the CaF_2.

The shape of the resulting microcrystal is determined by the directional dependence of the surface free energy. Using the Wulff construction [9] to minimize the Helmholtz surface free energy, one finds that a silicon crystal should be bound by the {111} and {100} faces. However, the common crystal habit of silicon also shows {113} faces (see figure 3.8a). The presence of this face can be explained by a surface reconstruction lowering the energy of the {113} surfaces [11]. Thus, we expect the shape of a silicon microcrystal on a (111) substrate to be hexagonal (see figure 3.8b).

As one can see in figures 3.2 and 3.5, silicon does indeed form hexagonally shaped microcrystals when grown both on electron irradiated and non-irradiated

Silicon Crystal

a. Silicon crystal habit.

b. Silicon microcrystal on 111 surface.

c. Cross section of microcrystal showing contact angle θ.
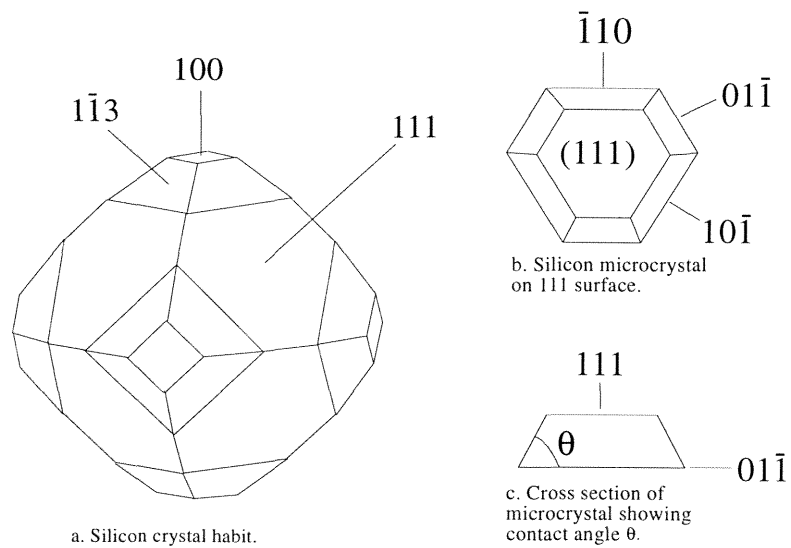
Figure 3.8: In (a) we show the silicon crystal habit which is bound by three types of faces: {111}, {100}, and {113}. Looking down the [111] direction (b), we see that a microcrystal on a (111) surface then forms an hexagonal shape. In (c) we show our definition of the contact angle.

CaF_2.

The contact angle (defined in figure 3.8c) between the microcrystal and the substrate is determined by the force balance at the bottom of the edge of the crystal.

$$\gamma_{e,v}(\theta)\cos\theta = \gamma_{s,v} - \gamma_{s,e} \tag{3.1}$$

In the above equation $\gamma_{s,v}$ represents the free energy of the substrate/vacuum surface, $\gamma_{e,v}(\theta)$ is the free energy of the epilayer/vacuum surface, and $\gamma_{s,e}$ is the free energy of the interface between the substrate and the epilayer. We approximate the silicon epilayer free energy as $\gamma_{e,v}(\theta) = \gamma_{111}\sin\theta + \gamma_{01\bar{1}}\cos\theta$, where γ_{111} and $\gamma_{01\bar{1}}$ are the free energies of the (111) and (01$\bar{1}$) silicon surfaces respectively; by comparing the number of broken bonds on the surfaces, we find that $\gamma_{01\bar{1}} = \frac{4}{3}\gamma_{111}$. Note that we ignore any passivating effect that the "surfing" calcium might have on the silicon surface.

Using the free energies given above and the measured contact angle for the high temperature zero dose case, equation 3.1 yields an interface free energy of $\gamma_{s,e}$=-1100 $\pm$ 60 ergs/cm^2. Since the interface bonding has been determined to be dominated by the Si$-$Ca bonds [1], this implies that the Si$-$Ca bond energy at the interface is 2.5 $\pm$ 0.3 eV. This value is reasonable considering that a rough estimate based on the average of the Si$-$Si and Ca$-$Ca bond energies with corrections for the differences in electronegativity puts the Si$-$Ca bond energy at 2.6 eV [12]. If we interpret the lower contact angle in the 1.0 mC/cm^2 case as an increase in the surface free energy of the CaF$_2$ surface ($\gamma_{s,v}$) due to induced F-centers and assume that the Si/CaF$_2$ interface free energy ($\gamma_{s,e}$) remains the same as in the zero dose case, then equation 3.1 yields an F-center-CaF$_2$ surface free energy of 520 $\pm$ 95 ergs/cm^2, in the high temperature case. As expected, this energy is larger than the free energy of the normal CaF$_2$ surface. The large confidence interval is due to the compounding of the substantial uncertainty in the measured contact angles.

Sasaki [8] thought that the increase in roughness of silicon epilayers on CaF$_2$

with increased silicon growth temperature was due to a chemical reaction between silicon and calcium. However, we observed that the roughness is smallest for an electron dose of 1 mC/cm^2 in the high temperature case. If a chemical reaction between the silicon and calcium was responsible for the 3D growth mode, one would expect the electron irradiated areas to be rougher due to the excess calcium available. Thus, the chemical reaction theory seems to be inconsistent with our experimental results whereas our simple model explains the data well.

We do not see the predicted hexagonally shaped islands neither on the irradiated medium temperature samples nor on any of the low temperature samples. For the low temperature samples, the assumption that the growth process is close to thermodynamic equilibrium probably breaks down; in these cases the mobility is too low. Instead of forming well defined islands, the silicon forms an overlayer of polycrystalline nature as shown in figure 3.3. A possible explanation for the smoothening of the medium temperature irradiated sample is that defects caused by the radiation decreases the mobility of the silicon atoms to the point where they cannot form the islanded surface of the zero dose case.

In conclusion, our model correctly predicts the observed hexagonal islands and decrease in surface roughness due to decrease in the contact angle in the high temperature cases and the medium temperature zero dose case. Furthermore, the model gives reasonable values for the Si−Ca bond energy and the free energy of the F-center-CaF$_2$ surface. At the low and medium growth temperatures the mobility of the silicon atoms is too low to form well defined microcrystals. This would explain why the resulting surfaces appears to be polycrystalline in the AFM micrographs and why the LEED patterns for the low temperature case indicates that the surface might be amorphous.

3.5   Chapter Summary

We studied the surface morphology of silicon, grown on epitaxial CaF_2/Si by electron beam assisted MBE, at three different growth temperatures, using atomic force microscopy (AFM), x-ray photoelectron spectroscopy (XPS) and low energy electron diffraction (LEED). We found that the roughness of the silicon overlayer was minimized by exposing the CaF_2 to an electron dose of 1.0 mC/cm^2 in the high temperature case (650°C) before growing the epitaxial silicon overlayer. Contact angle measurements yielded a $Si-Ca$ interface bond strength of 2.5 ± 0.3 eV and a free energy of 520 ± 95 $ergs/cm^2$ of the irradiated CaF_2 surface. The medium (575°C) and low (500°C) temperature samples showed smoother surfaces at the cost of crystalline quality. The AFM results were consistent with the LEED and XPS data. We presented a simple model based on thermodynamics which explained the data well in the high temperature case. An explanation based on kinetics was put forward for the low and medium temperature cases.

Although these results indicate that it is currently impractical to manufacture devices that require thin smooth films of silicon on CaF_2 through electron irradiation of the CaF_2 surface and kinetic constraints, there is some hope for this material system. The most fruitful approach would probably be to find a substance that could either lower the $Si-CaF_2$ interface free energy or passivate the silicon surface during the growth.

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Chapter 4

Si/Si$_{1-y}$C$_y$ Superlattices Grown by Surfactant Assisted Molecular Beam Epitaxy

4.1 Introduction

4.1.1 Chapter Abstract

Si/Si$_{0.97}$C$_{0.03}$ superlattices grown on Si(001) substrates by Sb surfactant assisted molecular beam epitaxy (MBE) are characterized by *in situ* reflection high energy electron diffraction (RHEED), atomic force microscopy (AFM), transmission electron microscopy (TEM), and high resolution x-ray diffraction (HRXRD). The RHEED shows that, in absence of Sb, the growth front roughens during Si$_{0.97}$C$_{0.03}$ growth and becomes smooth during subsequent Si growth. In contrast, when Sb is present, the growth front remains smooth throughout the growth. This observation is confirmed by cross-sectional (TEM) which reveals that for samples grown without the use of Sb, the Si/Si$_{0.97}$C$_{0.03}$ interfaces (Si$_{0.97}$C$_{0.03}$ on Si) are much more abrupt than the Si$_{0.97}$C$_{0.03}$/Si interfaces. In the case of Sb assisted growth, there is no observable difference in abruptness between the two types of interfaces. AFM

micrographs of the $Si_{0.97}C_{0.03}$ surface reveal features that could be the source of the roughness observed by RHEED and TEM.

4.1.2   Introduction and Background

Introduction of carbon into the Si/Ge material system could increase the flexibility in the design of electronic structure in a Si-based electronics technology. Carbon, in SiGe alloys, may provide a useful conduction band offset for layers grown coherently strained to Si. As discussed in chapter 1, this offset might allow fabrication of novel n-type devices such as n-type resonant tunneling devices (RTDs) or high-electron-mobility transistors (n-HEMTs) which are compatible with VLSI processing lines. In addition, due to the smaller lattice constant of diamond ($a_0=0.357$ nm vs. $a_0=0.543$ nm for Si and $a_0=0.566$ nm for Ge), carbon could be used for strain compensation of SiGe structures, resulting in alloy layers which are lattice-matched to Si and therefore in devices that are stable during high temperature processing steps.

When $Si_{1-x}Ge_x$ is grown coherently strained to Si(001), the compressive strain causes the four-fold-degenerate Δ_4 band to become the lowest conduction band state. The combination of strain splitting and compositional shift cancel for this band, resulting in almost no conduction band offset for $Si_{1-x}Ge_x$ alloys grown strained to Si [1].

While conduction band offsets can be achieved in the $Si/Si_{1-x}Ge_x$ system by growing tensile-strained layers on relaxed $Si_{1-x}Ge_x$ buffer layers, the incorporation of carbon may provide this desirable feature without the substantial defect densities and complicated processing inherent for growth on relaxed buffer layers. Since $Si_{1-x-y}Ge_xC_y$ alloys can be grown lattice matched to Si, the strain splitting of the conduction band can be eliminated and a useful conduction band offset might be provided by a compositional shift in band gap. According to estimates [1], the band gap for $Si_{1-y}C_y$ alloys strained to Si decreases only slightly with y. Therefore, it is

essential to develop growth techniques that allow the introduction of substantially more than 1% carbon to achieve band gap differences and band offsets that are larger than $k_B T$ at room temperature.

Our experiments show that for carbon concentrations in excess of 2%, the normal, two-dimensional layer-by-layer growth of Si(100) [2] is disrupted, resulting in a rough surface. This roughness manifests itself in RHEED as "spottiness" in the pattern, rather than the normally streaked, $(2\times1)+(1\times2)$ pattern associated with growth on atomically smooth, two-domain-reconstructed Si(001) surfaces.

In this chapter, we report a study of surfactant-mediated growth of $Si/Si_{0.97}C_{0.03}$ superlattices through the use of RHEED, TEM and AFM. The RHEED and TEM results were reported in [3] and the RHEED analysis was explained in detail and correlated the previous results with AFM measurements in [4]. Actual composition and layer thicknesses were confirmed using high resolution x-ray diffraction (HRXRD). We demonstrate that through the use of a surfactant, the tendency for the $Si_{1-y}C_y$ surface to roughen during growth can be reduced or eliminated, allowing layers with even higher carbon concentrations to be grown. This technique has be used previously with encouraging results to suppress Stranski-Krastanov islanding during the growth of Si/Ge superlattices [5] and $Ge_{1-y}C_y$ alloy layers [6] on Si substrates.

4.1.3 Outline of Chapter

First, the sample growth is described. Details of the superlattice structure and post-growth compositional analysis by HRXRD is presented. We then present an analysis of digitized RHEED data taken during growth of the samples and discuss the findings in comparison with cross-sectional TEM micrographs and AFM images of the sample surfaces. Finally, we put forward an explanation as to how the surfactant might suppress the islanding.

4.2 Experiment

4.2.1 Sample Growth

The samples used in this experiment consisted of two 15 -period, 26.1 nm Si/4.4 nm $Si_{0.97}C_{0.03}$ superlattices grown at 525°C on 100 nm thick Si buffer layers. Prior to growth, 2000 Ω-cm Si(001) substrates were degreased in trichloroethane and acetone for 2 mins each, followed by rinses in methanol for 10 mins and de-ionized H_2O. A 15 s dip in 5% HF just prior to loading into the MBE system (Perkin-Elmer Model 430S) was used to hydrogen passivate the wafer surfaces. *In situ*, the wafers surfaces were cleaned at 875°C under the influence of a slight Si flux (about 0.1 Å/s) until the RHEED pattern consisted of the usual $(2\times1)+(1\times2)$ streaked pattern indicative of a clean, reconstructed Si(001) surface.

After deposition of a 100 nm undoped Si buffer layer, approximately one monolayer (6.8×10^{14} atoms/cm^3) of Sb was deposited on the surface of sample SL-Sb. Sample SL received no such Sb pre-deposition. The superlattices were then grown on each sample using growth rates of approximately 1.8 Å/s and 0.015 Å/s for Si and C, respectively, evaporated from electron beam sources. The $Si_{0.97}C_{0.03}$ layer was grown with both shutters opened, so the growth rate for this layer was 1.815 Å/s. Closed-loop control of the flux was accomplished for Si through the use of a Sentinel III deposition controller and for C by monitoring the amplitude of amu 36 (C_3) with a residual gas analyzer (RGA) and adjusting the power to the electron gun to maintain a predetermined signal.

4.2.2 Characterization

HRXRD

Growth rates, layer thicknesses, and compositions were determined later by matching simulated curves with measured HRXRD curves. From the superlattice peak positions, the average carbon concentration and superlattice period were measured

and, together with a knowledge of the shutter opening times, used to calculate individual layer thicknesses and the carbon content of the $Si_{1-y}C_y$ layer. Using this method, we only detect the amount of substitutional carbon. In addition, there could be interstitial carbon.

RHEED

During superlattice growth, images of the RHEED patterns were digitized and captured for later analysis. The setup consisted of a standard RHEED system (Perkin-Elmer), a black and white CCD camera (SONY CCD-IRIS), and an S-VHS VCR (Panasonic AG 7355). Data were recorded on S-VHS videotape and digitized at a resolution of 512×512 pixels with a 256 level grayscale using a computer (Sun Sparc 2) and a video capture board (Data Cell S2200). In order to filter out some of the background due to stray light from the e-gun sources, we inserted a green filter between the camera and the RHEED screen.

AFM and TEM

The AFM measurements were performed in laboratory ambient without any surface preparation using a Nanoscope III from Digital Instruments. The TEM cross-sections were prepared by mechanical polishing and ion milling and the micrographs were acquired at an acceleration voltage of 300 kV on a Philips EM430 electron microscope.

4.3 Results

4.3.1 Analysis of RHEED Video

The RHEED pattern from both samples prior to growth of the Si buffer layer exhibited the usual $(2 \times 1) + (1 \times 2)$ streaked pattern typical of a clean Si(001) surface. During growth of sample SL, immediately upon opening the carbon shutter, the

a) Streaked RHEED pattern

c) Spotted RHEED pattern

b)

$R\sim0.4$

d)

$R=1$
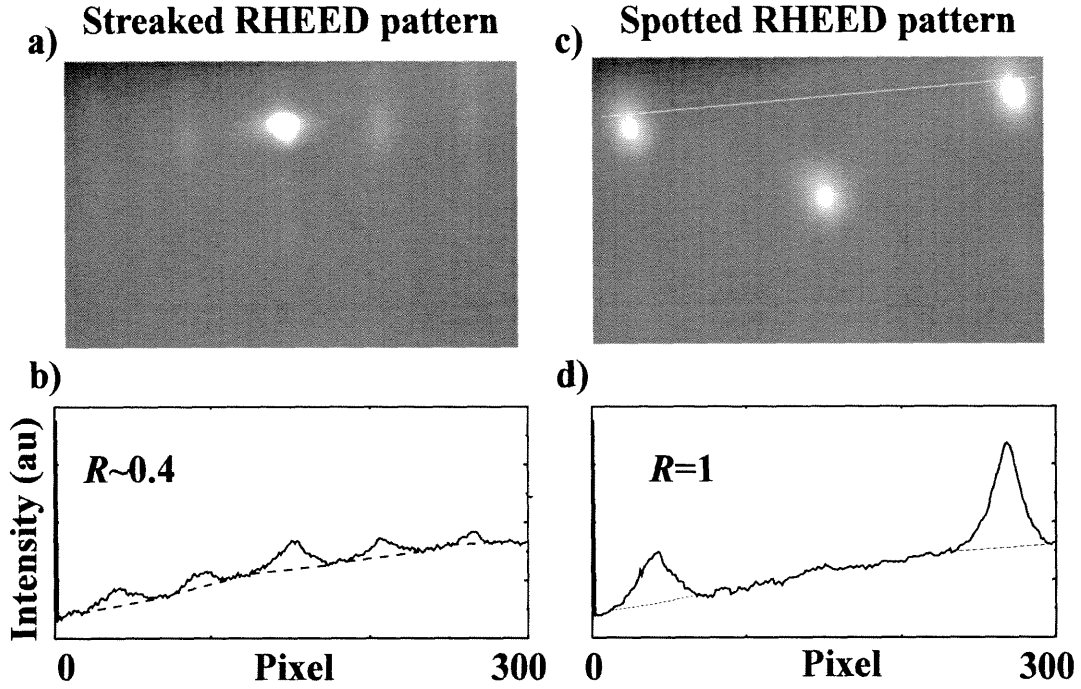
Figure 4.1: Analysis of the RHEED pattern. The amplitudes of the intensity along the line (marked in white in (a) and (c)) are shown in (b) and (d). The areas enclosed by the solid curves and the dotted lines in (b) and (d) represent the total intensity associated with that streak or spot. By calculating the ratio of the spot intensity to the total intensity of the pattern, we obtain a qualitative measure of the roughness of the surface R (see Eq. 4.1). This ratio can be used as a qualitative measure of surface roughness since, for a spotty pattern (c), the areas associated with the spots will dominate, making $R \approx 1$. On the other hand, when the RHEED pattern is streaked (a), all the areas are comparable, giving an R of about $\frac{2}{5} = 0.4$.

pattern became spotty in appearance, indicative of a rough surface. Each subsequent Si layer caused the pattern to return to the (2×1)-reconstructed pattern, suggesting that the Si deposition caused the surface to become smooth again. This alternating behavior of roughening followed by smoothing persisted throughout the growth of this sample. For sample SL-Sb, the half-order streaks originally visible in the pattern diminished in intensity after Sb deposition due to a realignment of the surface reconstruction [7]. The observed (1×1) pattern exhibited no spottiness during the subsequent growth of the superlattice and remained streaked (smooth).

To study the differences between the spotted and streaked patterns observed in the growth of sample SL, we employed the following analysis of the digitized RHEED data. First, the intensity along a line (marked in white in Figs. 4.1(a) and 4.1(c)) perpendicular to the streak direction and intersecting the $(\bar{1}0)$ and (10) spots was digitized. The amplitude of the intensity along the line is shown in Figs. 4.1(b) and 4.1(d). Then, the intensity associated with a certain spot or streak $(n0)$ was integrated along the line, to take into account the intensity from the full width of the streak or spot, to give the quantity I_{n0}. The background intensity due to light from the e-gun sources was subtracted as indicated by the dotted lines in Figs. 4.1(b) and 4.1(d). Finally, we calculated the ratio, R, of the spot intensity to the intensity of the whole pattern (see Eq. 4.1). This ratio can then be used as a qualitative measure of surface roughness since, for a spotty pattern, $I_{\bar{1}0}$ and I_{10} will dominate, making $R \approx 1$. On the other hand, when the RHEED pattern is streaked (see Figs. 4.1(a) and 4.1(b)), all the terms are of comparable magnitude, giving an R of about $\frac{2}{5} = 0.4$.

$$R = \frac{I_{\bar{1}0} + I_{10}}{I_{\bar{1}0} + I_{\frac{\bar{1}}{2}0} + I_{00} + I_{\frac{1}{2}0} + I_{10}} \qquad (4.1)$$

In Fig. 4.2(d), the ratio, R, is plotted as a function of time during growth of the two samples (C shutter opens at $t = 0$ seconds). For sample SL (no Sb pre-deposition), immediately upon opening the C shutter, the ratio is shown to increase rapidly, saturating at a value near 1. During subsequent growth of the Si layer, the RHEED pattern slowly recovered its original $(2 \times 1) + (1 \times 2)$, streaked pattern and the ratio returned to approximately 0.4 (smooth). From Fig. 4.2, we note that fully half (≈ 13 nm) of the Si layer thickness was required to completely recover the original pattern. During growth of sample SL-Sb, the RHEED pattern remained unchanged from the (1×1), streaked pattern observed immediately following Sb pre-deposition. Data was not available for SL-Sb during $Si_{0.97}C_{0.03}$ deposition because stray light from the e-guns washed out the pattern. Nevertheless, it was
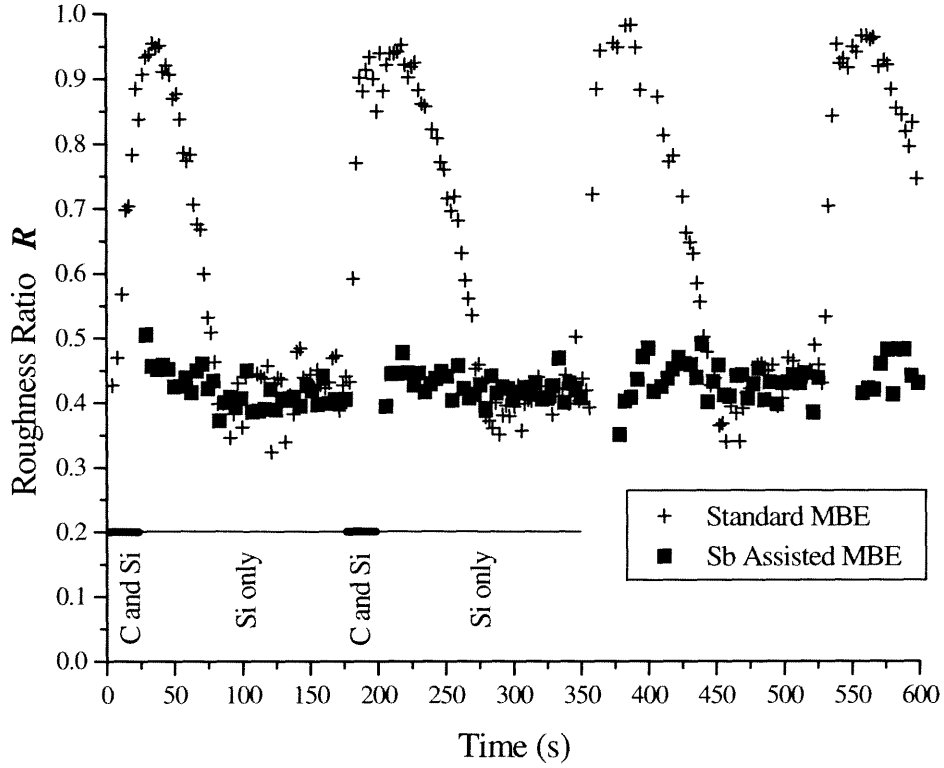
Figure 4.2: Roughness ratio R versus growth time (d). See Fig. 4.1 for the derivation of R. An R of 1 indicates a spotted RHEED pattern and an R of 0.4 indicates a streaked pattern. For sample SL (no Sb pre-deposition), immediately upon opening the C shutter the ratio is shown to increase rapidly, saturating at a value near 1. Half ($\approx$ 13 nm) of the Si layer thickness was required to completely recover the original pattern. During growth of sample SL-Sb, the RHEED pattern remained unchanged from the (1×1), streaked pattern observed immediately following Sb pre-deposition.

possible to view the pattern visually during these periods and no spottiness was observed.

4.3.2   Analysis of TEM Micrographs

In Fig. 4.3, we present cross-sectional TEM images of the samples which show features consistent with the RHEED observations. Fig. 4.3(a) is an image taken from sample SL, showing alternating thick and thin layers corresponding to the Si and $Si_{0.97}C_{0.03}$ layers, respectively. The surface of the superlattice is marked A near the top of the figure. Clearly, the interfaces which are formed when $Si_{0.97}C_{0.03}$ is grown on Si are much more abrupt than the interfaces formed when Si is grown on $Si_{0.97}C_{0.03}$. In the case of sample SL-Sb (Fig. 4.3(b)), both interfaces appear equally abrupt. In comparison with sample SL, they appear more abrupt than the case for which Si is grown on $Si_{0.97}C_{0.03}$ and less abrupt than the case for which $Si_{0.97}C_{0.03}$ is grown on Si. Sample SL was terminated with a $Si_{0.97}C_{0.03}$ layer resulting a rough surface morphology evident in the TEM and AFM micrographs (see Fig. 4.5). Sample SL-Sb was terminated with a Si layer which gives the superlattice a smooth surface morphology.

4.3.3   Analysis of HRXRD Data

In Fig. 4.4, we display HRXRD of the two samples. The peaks associated with sample SL are larger in magnitude and have narrower widths than those of sample SL-Sb. One reason for this could be that the $Si_{0.97}C_{0.03}/Si$ interfaces (when $Si_{0.97}C_{0.03}$ is grown on Si) in sample SL are more abrupt than the $Si/Si_{0.97}C_{0.03}$ interfaces in sample SL-Sb as seen in the TEM image (see Fig. 4.3). Another reason might be that there is a higher density of defects that look like stacking faults in sample SL-Sb as compared to sample SL. These defects could reduce the lateral coherence of the superlattices and thus broaden the HRXRD peaks. The defects are discussed in more detail below. As mentioned above, the superlattice
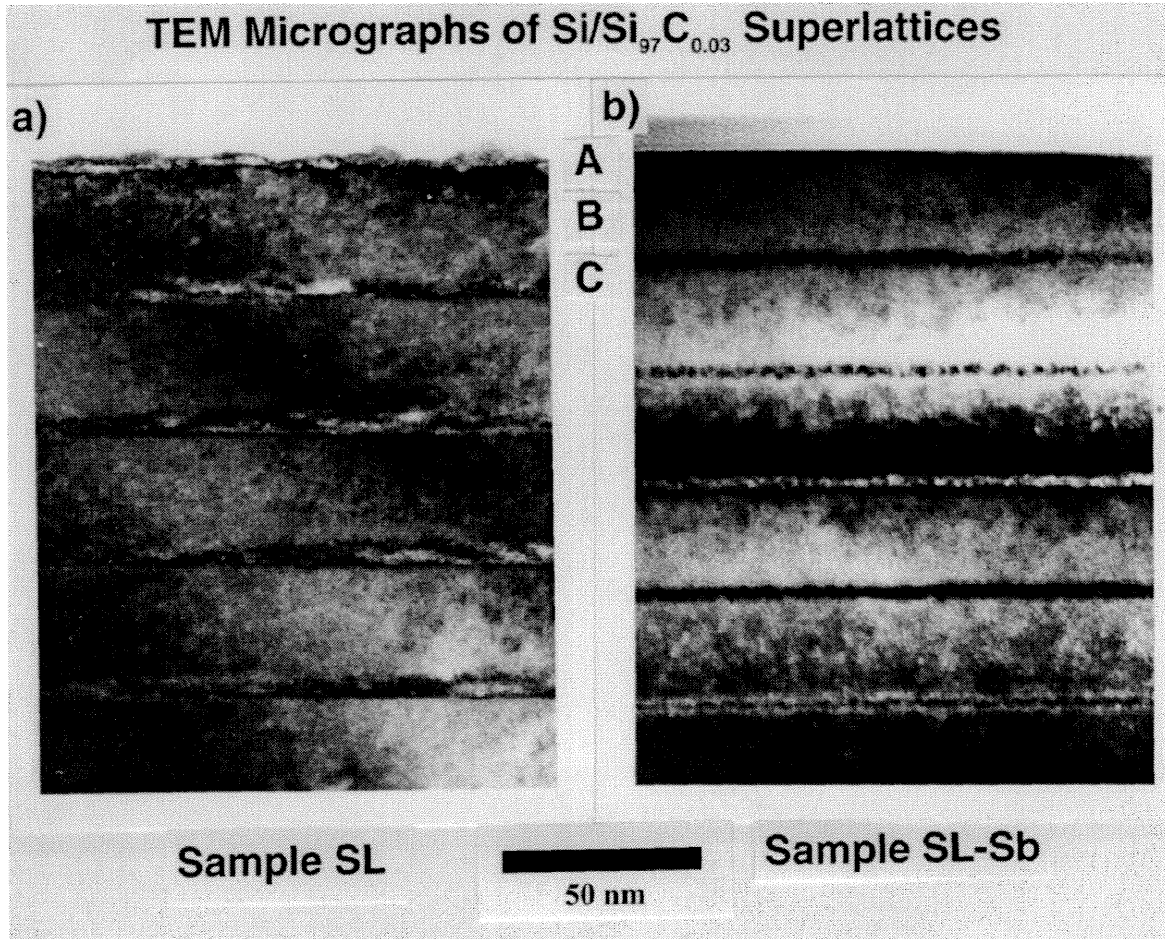
Figure 4.3: Cross-sectional TEM images of the superlattice samples. Fig (a) is an image taken from sample SL, showing alternating layers of thick and thin bands corresponding to the Si (B) and $Si_{0.97}C_{0.03}$ (C) layers, respectively. The surface of the superlattice is marked A near the top of the figure. Sample SL (a) was terminated with a $Si_{0.97}C_{0.03}$ layer resulting in rough surface morphology (see Fig. 4.5). Sample SL-Sb (b) was terminated with a Si layer. Clearly, the interfaces which are formed when $Si_{0.97}C_{0.03}$ is grown on Si are much more abrupt than the interfaces formed when Si is grown on $Si_{0.97}C_{0.03}$. In the case of sample SL-Sb (b), both interfaces appear equally abrupt. In comparison with sample SL, they appear more abrupt than the case for which Si is grown on $Si_{0.97}C_{0.03}$ and less abrupt than the case for which $Si_{0.97}C_{0.03}$ is grown on Si.

HRXRD of Si/Si$_{1-y}$C$_y$ superlattices
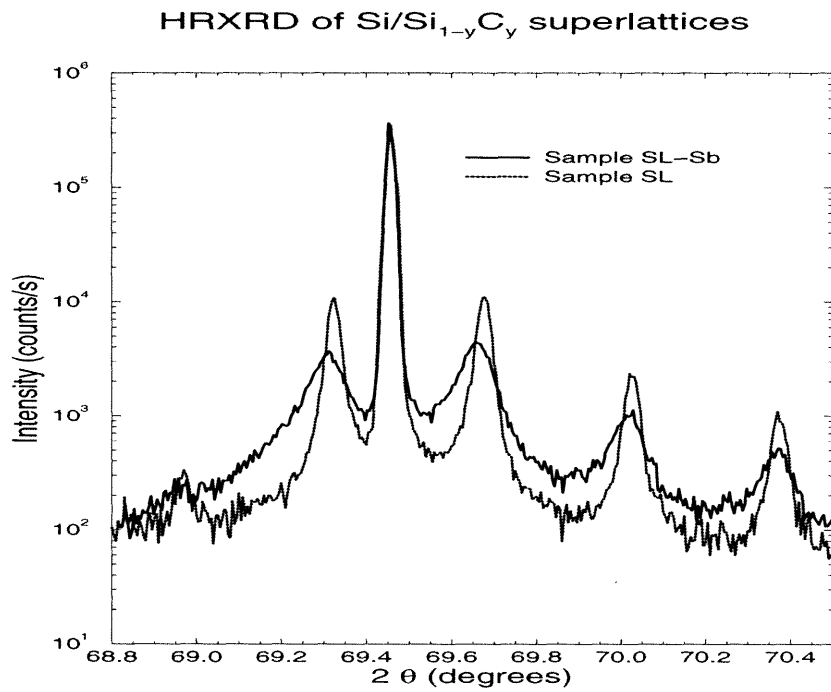
Figure 4.4: HRXRD of a 15 period Si/Si$_{0.97}$C$_{0.03}$ superlattices grown by standard MBE (sample SL) and by Sb assisted MBE (sample SL-Sb). The sample SL superlattice peaks are sharper than those of sample SL-Sb. The reason for this might be that there is a higher density of defects that look like stacking faults in sample SL-Sb as compared to sample SL. These defects could reduce the lateral coherence of the superlattices and thus broaden the HRXRD peaks.

AFM micrograph of $Si_{0.97}C_{0.03}/Si$
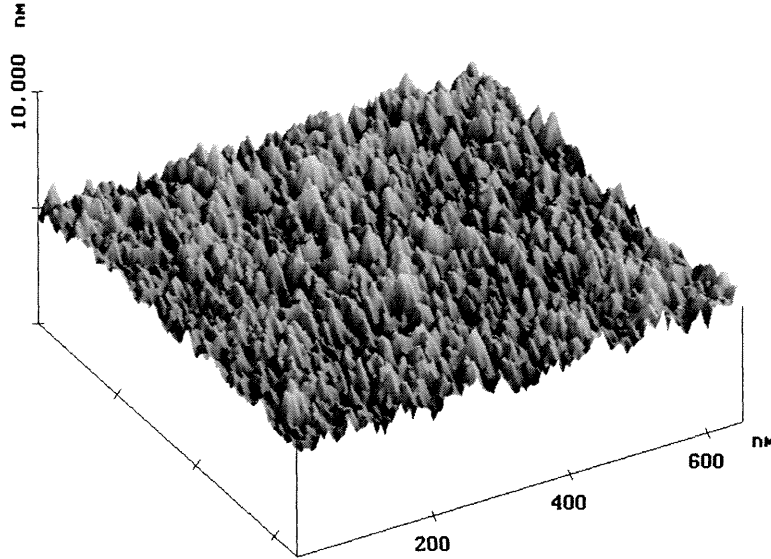
Figure 4.5: AFM micrograph of the top layer ($Si_{0.97}C_{0.03}$) of a 15 period $Si/Si_{0.97}C_{0.03}$ super-lattice grown by standard MBE (sample SL). The features are on the order of 1.4 nm tall and 40 nm on the side. These surface features apparently give rise to the spotty RHEED pattern observed (see Fig 4.1(c)) and the variation in thickness seen in the TEM (see Fig 4.3).

peak positions were measured to calculate the layer thicknesses and carbon content of the samples.

4.3.4 Analysis of AFM Micrographs

In Fig. 4.5, we show an AFM micrograph taken from the surface of sample SL, terminated with $Si_{0.97}C_{0.03}$. The figure shows features on the order of 1.5 nm peak-to-valley perpendicular to the surface and 40.0 nm laterally. There does not appear to be any directional dependence to the features. The RMS roughness of this surface was measured to be approximately 0.36 nm. These features are apparently responsible for the spotted pattern observed in the RHEED image of Fig. 4.1(c), since additional samples we have studied, for which Si in one sample and Sb-terminated $Si_{0.985}C_{0.015}$ in another were grown on Si(001), lack

these features and have streaked RHEED patterns. The feature height observed in the AFM micrograph agrees with the thickness variation seen in the TEM image (see Fig. 4.3(a)).

4.3.5   Large Scale Defects

In addition to the interface structure, the TEM images also reveal that here are defects that look like stacking faults, possibly originating from point defects such as C dimers or trimers in the SL-Sb sample. These defects are also present without Sb in the SL sample albeit at a lower density. Most of the defects in sample SL-Sb originate in the region between superlattice layer 7 and 10 (counting up from the bufferlayer). Only a small fraction (0.4%) of the volume of the superlattice is enclosed by these defects.

4.4   Discussion

The data presented in the above section suggest that one or more of the species in the carbon flux disrupts the epitaxial growth of $Si_{0.97}C_{0.03}$ on Si (sample SL). These species form surface nucleation centers where diffusing adatoms can incorporate in competition with surface steps, resulting in 3D growth. Residual gas analysis of the growth flux shows that it primarily consists of monomers (C), dimers (C_2), and trimers (C_3). In principle, any of carbon species could act as nucleation centers. We expect the monomers to be the most mobile on the surface, and hence, the most likely to simply be incorporated in step flow growth. Of multiple carbon species the dominant is the dimers.

All of the multiple carbon species, however, are potential candidates for nucleating the rough growth. First, the C$-$C bond is 1.8 times stronger than the Si$-$Si bond and based on the observation that the Si dimer is stable up to 600 K [9], one expects the C dimer and trimers to be stable up to 1100 K or about 800°C. Since

the growth temperature used in this experiment was 525°C, the carbon dimers and trimers impinging on the surface remain undissociated.

Second, the diffusion length of these dimers and trimers is expected to be negligible compared to that of the monomers because of the large activation energy due to the bond bending and stretching required for a dimer or trimer to move on the surface. Thus, while the monomers might diffuse to a step and thus contribute to step flow growth, the dimers or trimers will incorporate at the site of impingement and form nucleation centers.

Third, the nucleation center density generated by the dimers and trimers is large enough for 3D growth to dominate over 2D step flow growth. To show one possibility for how this could occur, we need to consider this probability of an adatom attaching to a dimer or trimer rather than to a step. To assess the relative probability, we follow Mo's *et al.* argument [9]. Adapting his argument, we consider a square with the side aligned with a step on a slightly miscut substrate. We set the length of the side equal to the average terrace width W of the steps which is given by the degree of miscut of the substrate. Under the conditions of our experiment, this square is the area from which this portion of the step accumulates adatoms. Let us say that the square has a dimer at the center and assume that both the step and the dimer are perfect sinks for adatoms. According to the 2D random walk theory, the number of hops required for an adatom impinging at a random site in the square to reach the dimer is on average $\sim (W/a)^2$ where a is the length of a hop. The number of hops required for the adatom to find the step is also on average $\sim (W/a)^2$. In this case then, both island growth and step flow growth will take place. For both sample SL and SL-Sb, the fluxes of the dimers and trimers were about 10% and 5% of the monomer flux respectively. These fluxes yield a dimer and trimer density of about 10^{12} molecules/cm^2 in the time required to complete a monolayer of Si$_{0.97}$C$_{0.03}$ growth. Given a limiting case of a wafer miscut of about 0.5°, the terrace width is $W \approx 2 \times 10^{-6}$ cm. At the density calculated above, we get 4 dimers per square so 3D nucleation should compete effectively with 2D step-flow

growth.

We speculate that in the case of sample SL-Sb, where the surface stays smooth throughout the growth, the surfactant assisted growth mechanism prevents the dimers and trimers from forming effective nucleation centers. Although there is some Sb incorporation during growth, as measured by Rutherford backscattering spectrometry[1], the concentration of the incorporated Sb is too small to provide significant strain relief for the $Si_{0.97}C_{0.03}$ layers. Instead, we believe that the primary role of the Sb is to ride as a surface layer burying the carbon dimer and trimers. An impinging silicon adatom diffuses on the Sb-layer until it reaches a proper site. At that site, the adatom undergoes an exchange with a surfactant atom and incorporates. Again, the carbon clusters do not diffuse on the surface, rather they are incorporated immediately by some exchange mechanism. Since direct contact between Si adatoms and the carbon clusters is reduced, the clusters no longer serve as effective nucleation centers and the growth stays relatively smooth as shown by AFM and the streaked RHEED pattern.

The TEM picture in Fig. 4.3 shows that the interface between the Si and $Si_{0.97}C_{0.03}$ on the substrate side is slightly rougher on sample superlattice grown with Sb than it is on sample grown without Sb. One possible reason for this is that, in our case, a perfectly ordered Sb terminated Si(001) surface was not achieved (RHEED pattern was (1×1) as opposed to (2×1)). The unordered surface could prompt the exchange to occur at sites other than steps thus creating a less abrupt growth front. A highly-ordered Sb-terminated (2×1)-reconstructed surface could be expected to aid in the formation of perfectly flat interfaces.

In conclusion, the Sb prevents the carbon dimers and trimers from serving as effective nucleation centers for 3D growth and, as a consequence, the surface stays smooth during growth of $Si_{0.97}C_{0.03}$ on sample grown with Sb, whereas the surface roughens during $Si_{0.97}C_{0.03}$ growth on the sample grown without Sb.

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[1]We would like to thank Maggie Taylor for the RBS measurement and analysis.

4.5 Chapter Summary

We studied the effect of adding Sb as a surfactant in the MBE growth of $Si/Si_{0.97}C_{0.03}$ superlattices. Our analysis of reflection high energy electron diffraction, transmission electron microscopy, x-ray diffraction, and atomic force microscopy data shows that Sb induces 2D growth of $Si_{0.97}C_{0.03}$ under conditions in which standard MBE yields 3D growth. Epitaxial growth on the 2×1 Si(001) surface could be easily disrupted by carbon dimers and trimers which introduce additional sites for incorporation of Si adatoms. The Sb-terminated Si surface could prevent direct contact between the carbon dimers and the silicon, and hence suppresses the tendency of the surface to roughen. In conclusion, the use of Sb as a surfactant during growth of high-carbon-content $Si_{0.97}C_{0.03}$ alloys was shown to result in sharper film interfaces and appears useful for achieving carbon contents in excess of what would normally be possible for growth on bare Si(001).

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Chapter 5

Dependence of the I/V Curve of a Metal Insulator Semiconductor Switch on Insulator Thickness

5.1 Introduction

5.1.1 Chapter Abstract

Although the metal insulator semiconductor switch (Al/SiO$_2$/n-Si/p-Si) has been investigated for quite some time, there has been no systematic report on the influence of the oxide thickness on the I/V curve. We fabricated four types of metal insulator semiconductor switches where the only intentional difference was the thickness of the oxide. We observed, both experimentally and by simulation, that the I/V curves of these devices are very sensitive to the oxide thickness. While the simulated curves do not agree with the measured ones, the simulation provides some insight to the operation of the device. The onset of the negative resistance region in the curve is so sensitive to the electron and hole tunneling currents that these devices could be used to characterize ultra thin oxides. Extremely high current densities (10^3 A/cm^2) have been driven through the ultra thin oxides without

Device Structure

Aluminum
Tunnel oxide - SiO_2
n-type Silicon
p-type Silicon substrate
Aluminum

Figure 5.1: The MISS device consists of a thin insulator layer on an n-p (or p-n) junction. The top and back contacts are made of aluminum. The figure is not drawn to scale.

significantly changing the device characteristics. We believe this is the highest, non-destructive, current density through an oxide reported to date.

5.1.2 Motivation and Background

The Metal Insulator Semiconductor Switch (MISS), first reported by Yamamoto 24 years ago [1], is a two terminal device with a current-voltage (I/V) curve which exhibits a high and a low impedance state, as seen in figure 5.2. Recently, renewed interest has been generated in this device, thanks to Levy'[2] novel static random access memory design in which a MISS is used in series with a resistor as the memory cell [3][4].

The device consists of a metal/SiO_2/Si(n)/Si(p^+)/metal structure (see Fig. 5.1), where the insulator is thin enough to pass tunnel current, but not so thin that holes cannot accumulate at all. While this device has been investigated to a large extent, there has not been many reports on how the I/V curve depends on the oxide thickness. In this paper, we report both experimental and simulated I/V curves of four types of MISS devices where the only intentional difference between the types was the insulator thickness.

In addition to the variation in the I/V curves with oxide thickness, we ob-

served the following. The I/V curve for a particular device changed after the first switching event, but then remain essentially the same after subsequent switching events. While this "forming" behavior has been reported by other groups[5], we could drive current densities on the order of 10^3 A/cm^2 through the ultra thin oxides without further changing the device characteristics. We believe this is the highest, non-destructive, current density through an oxide reported to date.

We observed, both experimentally and by simulation, that the I/V curves of these device are sensitive to the oxide thickness. Since the onset of the negative resistance (V_{peak}, I_{peak}) depends both on the electron and hole tunneling currents, the MISS can be used to study tunneling properties of ultra thin oxides, given proper simulation of the semiconductor part of the device. Precise knowledge of these oxide parameters will become increasingly important to the design of standard CMOS devices as the oxide thickness enters the ultra thin regime.

In comparing the measured curves with simulations based on the work of Habib and Simmons[6] and Zolomy[7], we find that while there is no direct agreement between the experiment and our simulation; the simulation still provides some insight to the operation of the device.

The chapter is organized in the following fashion. The device structure, fabrication process, and the procedure for estimating the insulator thickness are described in the experiment section below. Next, the experimental I/V curves are presented and discussed briefly. A brief overview of how the device works, the details of the simulation and calculated curves are presented in the simulation section. In the discussion section, we discuss the measured curves in detail and compare them to calculated results.
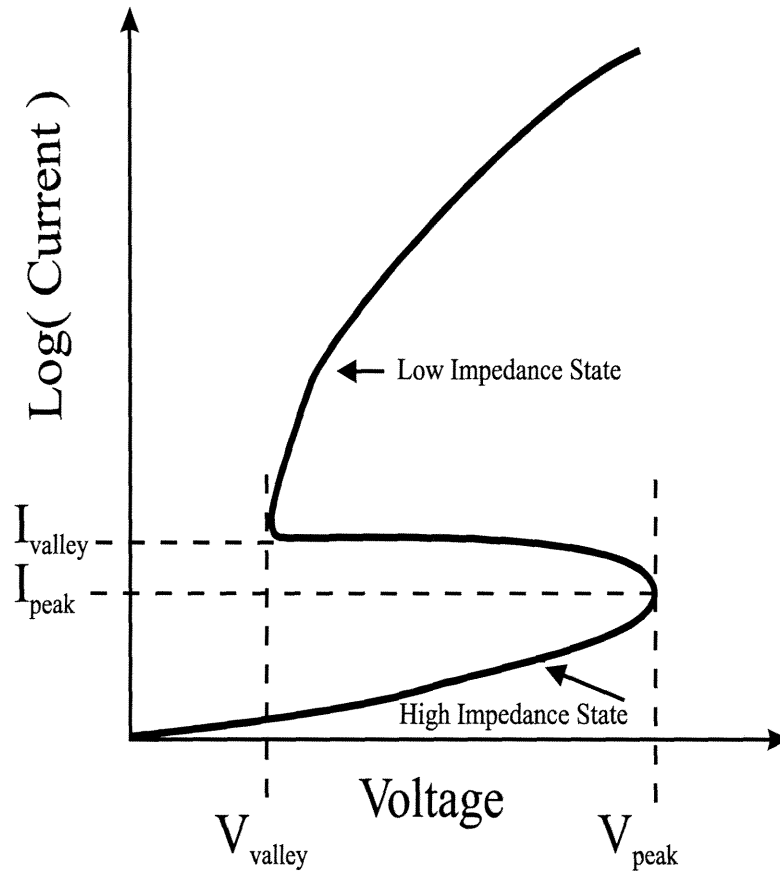
Figure 5.2: The generic MISS I-V curve has two impedance states as indicated in the figure. Since the current scale is logarithmic, the I/V curve has the desirable feature (for memory applications) that the high impedance state currents are orders of magnitude lower than those of the low impedance state. The definitions of peak and valley voltages as well as currents are shown in the figure.

5.2 Experiment

5.2.1 Device Structure

The fabrication process used in this experiment consisted of three major steps following the process developed by Levy[2]. First, a sample was cleaved from an epi wafer and cleaned using a modified RCA process followed by HF passivation. Second, the sample was oxidized in a rapid thermal processor. Third, aluminum was deposited and patterned to form top and back contacts.

A 1×1.5 cm sample was cleaved from a commercially obtained wafer[1], consisting of an n-type epi layer on a p-type substrate. The sample was degreased for 30 s (ultrasound) in Acetone, 2-Propanol, and de-ionized (DI, 18 MΩ-cm resistivity) water. Next, the sample was cleaned using a modified RCA procedure[8]. The sample was immersed in $NH_4OH:H_2O_2:H_2O$ 1:4:20 (with 1 ppm of Ethylenediaminetetraacetic acid) at 80°C for 10 minutes followed by an overflow rinse in DI water for another 10 minutes. Then, the sample was spun dry and immersed in $HCL:H_2O_2:H_2O$ 1:1:5 at 80°C for 5 minutes. To remove the chemically grown oxide, the sample was dipped in 10% 10-1 BHF followed by a dip in DI water.

Immediately following the DI water dip, the sample was introduced into the rapid thermal processor[2] (RTP), and the temperature was ramped to 900°C at 200 °C/s in Ar ambient. After a 15 s hold at 900°C in Ar, the ambient was switched to O_2 for 60 s to grow a sacrificial oxide, and then switched back to Ar for a 45 s anneal. The sample was removed at 250°C and dipped in 10% 10-1 BHF to remove the sacrificial oxide. After a brief dip in DI water, the tunnel oxide was grown in a similar fashion, except that oxygen flow time (60 s in case of the sacrificial oxide) was varied according to the type of device fabricated (see table 5.1). In all cases the total time at 900°C was 120 s.

[1]Silicon Quest, Inc.

[2]Heatpulse Minipulse 310, AG Associates, Inc.

Table 5.1: Device types.

Type	O$_2$ Flow Time (s)	Estimated SiO$_2$ Thickness (nm)	Measured Devices
A	15	1.5	10
B	30	1.8	11
C	45	2.1	8
D	60	2.5	7

Immediately after the tunnel oxide growth, the sample was transferred into a sputtering machine for metal deposition. To form the top contact, a 75 nm thick aluminum layer was deposited by magnetron sputtering in 4.6×10^{-3} Torr Ar ambient. The contacts were defined by standard photolitography. Finally, an Al back contact was deposited in the same fashion.

5.2.2 Electrical Measurements

The I/V curves were acquired at room temperature using an HP 4145A Semiconductor Parameter Analyzer. For these measurements, the current was sourced and the voltage measured. We noticed that the I/V curve changed as the device switched for the first time, but that subsequent switching events had little effect on the curve. In order to compare the results, each device was switched continually at 60 Hz to a maximum current of 100 mA for a few seconds before the I/V curve was acquired. The C-V measurements were obtained at a frequency of 1 MHz using a HP 4192 Impedance Analyzer. To capture the variation across the sample, about 10 devices were probed on each sample.

5.2.3 SiO$_2$ Thickness Estimate

In order to estimate the thickness of the insulator layers, we employed the following method. We fabricated metal-oxide-semiconductor devices using the process described above, but substituting the n-p substrate with a plain heavily doped p-type silicon (100) wafer. Then, we measured the thickness of the insulator using the standard capacitance-voltage technique.

For the 60 s oxygen flow sample, we measured a thickness of 2.5 nm, assuming that the dielectric constant of the thin SiO$_2$ takes on the bulk value of 3.9. Comparing this value with published calibration curves (SiO$_2$ thickness, as measured by *ellipsometry*, versus oxygen flow time in RTP oxidation), we see that our measurement yields a value that is about 1 nm less than published values[9],[10]. Given that Duzelier *et al.*[11] have observed a constant offset of 0.9 nm when comparing C/V thickness measurements with that of high resolution transmission electroscopy and ellipsometry, we find our measurement in good agreement with the calibration curves. They suggest that the constant offset could be attributed to the aluminum reacting with the SiO$_2$ layer thus decreasing the effective thickness as measured by C/V techniques.

While the C/V technique worked well for the 60 s sample, the tunneling currents were too large for the thinner oxides – the MOS structure could not accumulate charges in the normal fashion. To estimate the insulator thickness for samples B, C, and D, we used the measured thickness for the 60 s device and then extrapolated down to the shorter oxidation times using an average slope of 0.023 nm/s based on the previously mentioned published calibration curves. The resulting estimated effective insulator thicknesses are shown in table 5.1.

5.3   Results

In figure 5.3, we show the measured I/V curves for the four types of devices. For each type of device, we measured curves of about ten devices (see table 5.1 for the actual number of measured devices) and then calculated the mean curve and the standard error in the mean. This average curve is plotted with error bars displaying the standard error. The details and trends of these curves will be explained in the discussion section, so we will only point out the most important features here.

All the devices, except for type A, show a negative differential resistance region. In the case of type A, we believe that the oxide is too thin to serve as an effective barrier for the holes resulting in an I/V curve showing no negative resistance region. The peak voltage (see figure 5.2 for definitions) increases with increasing insulator thickness while the peak current remains the same. These trends are in disagreement with our simulation. It is worth noting that the current densities in the low impedance state are on the order of 10^3 A/cm^2, if the current density is assumed to be uniform. As far as we can tell, this is the highest reported, non destructive, current density through an ultra thin oxide (see the discussion section).

5.4   Simulation

5.4.1   Simulation Description

Before we discuss the details of the simulation, we will briefly describe how the device works. In the high impedance regime, i.e., for low currents, the device can be thought of as a reversed biased MOS barrier (the metal oxide semiconductor junction) in series with a forward biased n-p junction (see Fig. 5.4a for the band diagram). Most of the voltage drop is across the reversed biased junction and the behavior is dominated by this junction. When the voltage is such that the n^- region is fully depleted, any additional voltage will be dropped across the n-p
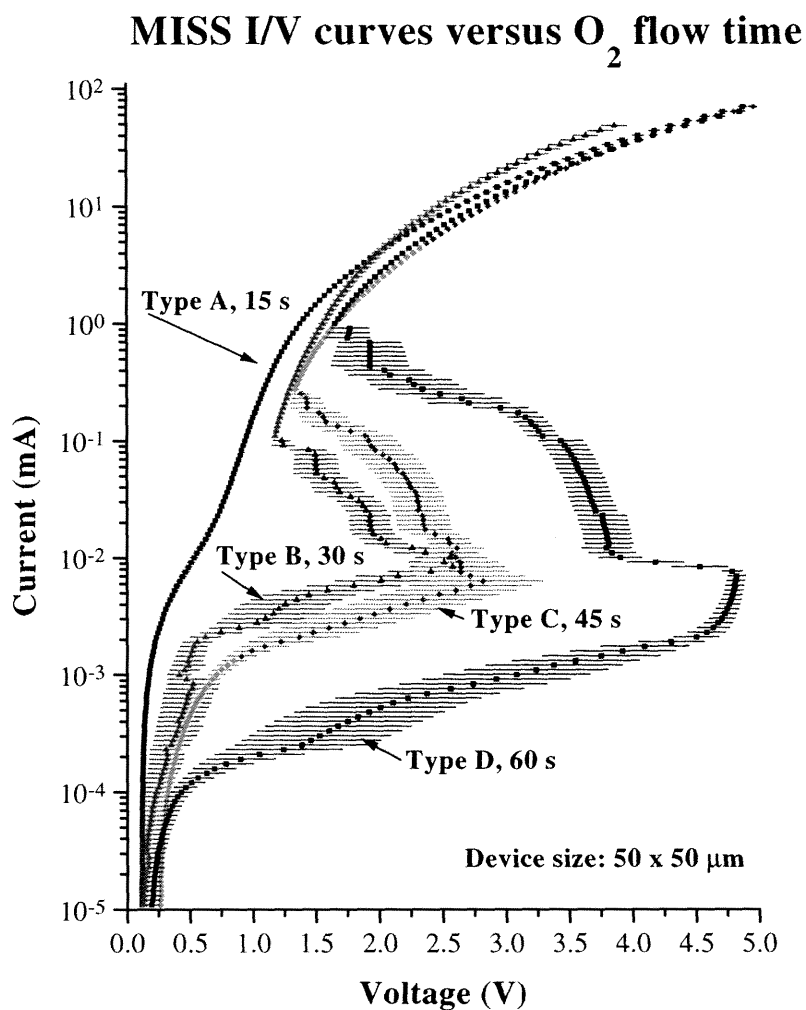
Figure 5.3: I-V curves of the MISS devices as a function of oxygen flow time. See table 5.1 for estimated thickness. For each type of device, we measured the I/V curve of about ten devices (see table 5.1 for the actual number of measured devices) and calculated the mean curve and the standard error. The error bars displayed represent this standard error.

junction, which causes it to become forward biased. We call this mode of operation punch through (PT) mode. The increasing forward bias of the n-p junction leads to injection of a large number of holes into the surface region. The holes accumulate under the oxide and thus lower the barrier for electrons to tunnel into the surface region, which in turns increases the forward bias of the n-p junction. Thus, a positive feedback loop is created and the device switches into the low impedance state characterized by high injection.

Our simulation closely follows previously published simulations by Habib and Simmons[6] and Zolomy[7], with minor modifications[12]. In this section, we describe the simulation in enough detail to explain what we did - most of the formalism can be found in the original papers[6, 7] and will not be reproduced here.

The simulation is described in three parts. We start with the variables and then move on to the assumptions and details of the model which are discussed in the order of the layers of the device, from left to right, as drawn in Fig. 5.4a. Finally, we mention the equations and the solution method.

The Variables

The variables and the important parameters of the simulation are seen in Fig. 5.4a. The five variables of the model are listed below:

- The voltage across the oxide, V_i, as seen in the inset in Fig. 5.4a.

- V_s is the magnitude of the band bending across the surface region.

- $2V_r$ is the difference between the electron quasi Fermi level and its equilibrium position [12]; this variable is set to zero, unless the device is in punch-through mode.

- $2V_p$ is the separation between the quasi Fermi levels within the surface depletion region.

MISS Device simulation band diagram

a) Non-Punch-Through (non-PT) mode

b) Punch-Through (PT) mode
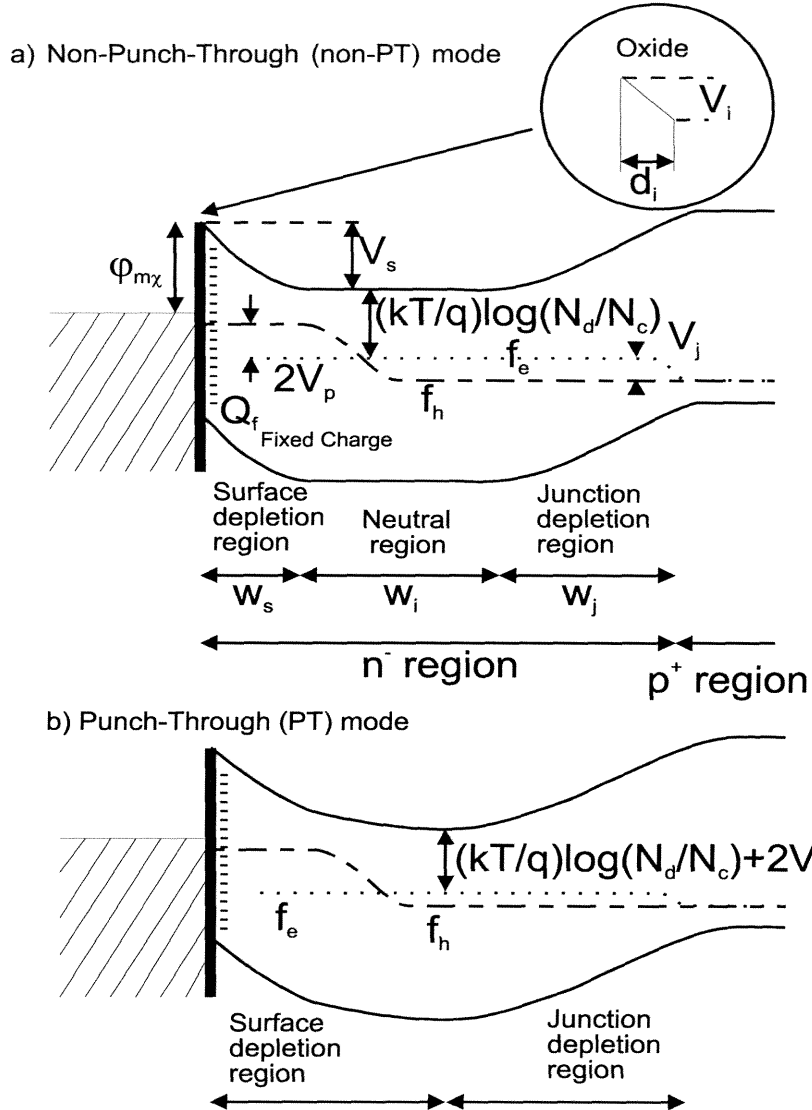
Figure 5.4: Band diagram for the simulation. From left to right, the device consists of a metal contact, tunnel oxide, a lightly n-type doped region, followed by a heavily doped p-type substrate. In a), we show the band diagram used in the non punch through (non-PT) mode of the simulation. The punch through (PT) mode is shown in b). The difference is that there is no "Neutral Region" and the electron quasi Fermi level is offset by $2V_r$ in the PT mode. The five variables of the model are: V_i, V_s, $2V_r$, V_p, and V_j. For a list of the parameters used in the model, see table 5.2.

- V_j is the separation between the quasi Fermi levels within the junction depletion region.

The Metal

The metal is described by one parameter, namely $\phi_{m\chi}$, the relative band lineup between the metal and the semiconductor.

The Oxide

The oxide is assumed to be uniform, having a dielectric constant of ϵ_i and a fixed charge density Q_f located between the oxide and the semiconductor. The carrier tunneling through the thin oxide follows a Richardson model (see eq. (1a) in [6]) with a tunneling probability that is assumed independent of the field across the oxide, and exponentially decaying with the oxide thickness d_i. Any carrier recombination or generation within the oxide or at the oxide-semiconductor interface is neglected, so the quasi-Fermi levels at that interface are floating.

The Semiconductor

The semiconductor is modeled using the full-depletion – charge neutrality approximation, i.e., the n^- region of the semiconductor was divided into three parts as shown in Fig. 5.4a from left to right: the surface region next to the oxide, which is assumed fully depleted, thus having a parabolic band bending.

Next comes an intermediate region which is assumed neutral, i.e., having flat bands. The intermediate (neutral) region may or may not exist. When there is no neutral region, i.e., the entire n^- region is depleted, the device is said to be in "punch-through" (PT) mode. In PT mode, shown in Fig. 5.4b, the electron quasi Fermi level is lower than the equilibrium Fermi level.

The final part of the semiconductor is the n^- part of the n–p junction, which is also assumed fully depleted, thus also having parabolic bands.

An important approximation is that the device operates in low-injection mode. This implies that the quasi-Fermi levels are nearly flat within the depletion regions, and that the band-bending in the depletion regions remains parabolic regardless of the current density. This assumption becomes inaccurate as the current density goes up. Consequently, there is an upper bound for the current, above which there is no solution to the model (the junction depletion width, w_j, becomes negative). Assuming low injection, a single number (V_p, V_j) describes the separation of the quasi Fermi levels within each of the depletion regions (i.e., this separation is position independent).

The Equations

Having discussed the assumptions, we now turn our attention to the equations. Four equations are used as constraints on the five variables: (1) Electron current continuity at the oxide-silicon interface (OSI), (2) Hole current continuity at the OSI, and (3) Electric field discontinuity according to the charge at the OSI. (4) This equation is different depending on whether the device is in the punch-through mode or in the non-punch-through mode. In PT mode, the sum of the surface- and the junction depletion widths is equal to the n^- region width, while $V_r \leq 0$. In non-PT mode, $V_r = 0$, while the sum of the two depletion widths is less than the n^- width. The formulas connecting the currents, field and depletion widths to the five variables can be found elsewhere[7, 12].

The Solution

To solve the four equations, the following formalism was used. The equations were solved at a single point, namely, the equilibrium point at which the electron and hole current vanish. The algebraic equations were then converted to a vector differential equation using the implicit-function theorem, and solved using a 4th-order Runge-Kutta method, followed by Newton-Raphson corrections after each

integration step.

Despite the inherent inaccuracies in the above-mentioned approximations, this model is appealing in the sense that it is rather straightforward to solve it, and does not suffer from the numerical problems associated with a self-consistent solution of the diffusion-drift equations of the device. Within the assumptions of this model, some useful observations about the operation of the device could be made and compared to experimental results, as well as a qualitative understanding of how a change in the device parameters would affect the J/V curve. The model is, however, too crude to yield accurate numerical agreement with experiment, as will be discussed in the next section.

5.4.2   Simulation Results

The parameters used in our simulations are listed in table 5.2.

A typical result of the simulation is given in Fig. 5.5, where we plot the current density vs voltage for several oxide thicknesses. The J/V curves in Fig. 5.5 all exhibit some characteristic behaviors. The negative resistance regime is rather flat in current, i.e., J_{peak} is very close to J_{valley}. This was not observed in our experiments; instead the experimental curves (see Fig. 5.3) show that I_{valley} is 1-2 orders of magnitude larger than I_{peak}. Another disagreement with experiment is that J_{peak} (current density at the onset of the negative resistance region) changes rapidly with oxide thickness, roughly by an order of magnitude for every 0.4 nm. Again, this was not seen in the experiment. The simulated curves all exhibit cusps at the peak voltage (V_{peak}). This is an artifact of this model and results from the transition from PT to non-PT modes.

Some of the important observations that could be made using this simple model are as follows:

- Negative resistance is observed only when the tunneling probability is neither too high, nor too low. This agrees with our experimental results; device type

Table 5.2: The parameters used in the simulations.

Param.	Value	Description
T	$300\ ^\circ K$	Ambient Temperature
ϵ_s	$11.7\ \epsilon_0$	Silicon Dielectric Constant
τ_p, τ_n	2×10^{-5}	Hole, electron lifetimes
N_v	$1.02 \times 10^{19}\ \text{cm}^{-3}$	Hole desity
N_c	$2.8 \times 10^{19}\ \text{cm}^{-3}$	Electron density
A_h, A_e	$0.66A_0, 0.38A_0$	Richardson coefficients
μ_p, μ_n	$450, 1500 \frac{cm^2}{V \cdot sec}$	Hole, electron mobility
$\varphi_{m\chi}$	$-0.11V$	Aluminum - Silicon band lineup
N_d	$2 \times 10^{15}\ \text{cm}^{-3}$	n^- doping
N_a	$3 \times 10^{18}\ \text{cm}^{-3}$	p^+ doping
W_{n^-}	1.2μ	n^- epi-layer width
d_i	$1.6, 2.0, 2.4$ nm	Oxide thickness
η_h, η_n	$7d_i$[6], $9.22d_i$[21]	Hole, electron tunneling exponent
Q_f	-7×10^{12} q/cm^2	Fixed interface charge
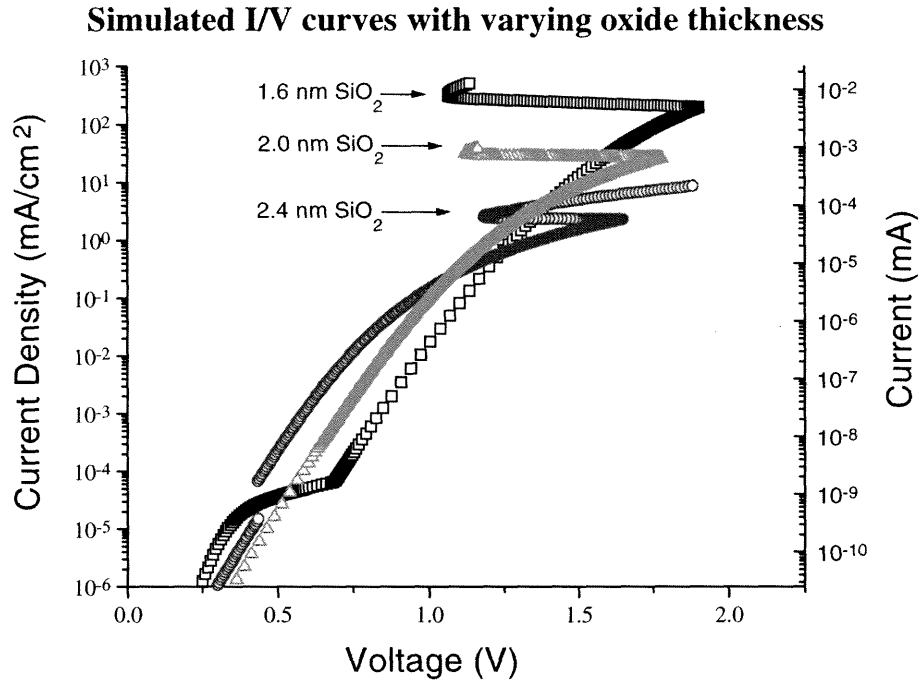
Figure 5.5: Calculated J/V curves of the MISS devices as a function of oxide thickness. We assumed a 50×50μm device size to calculate the current scale shown on the right axis. The negative resistance regime is rather flat in current, i.e., J_{peak} is very close to J_{valley}, in disagreement with experiment (see Fig. 5.3). The negative-resistance current density (J_{peak}) changes rapidly with oxide thickness, roughly by an order of magnitude for every 0.4 nm. Again, this was not observed in the experiment. The simulated curves exhibit all exhibits cusps at the peak voltage (V_{peak}). This is an artifact of this model and results from the transition from PT to non-PT modes.

A (oxide too thin) shows no negative resistance as the holes tunnel out of the surface region, instead accumulating under the oxide.

- The negative-resistance region is characterized by accumulation of holes near the silicon-oxide interface.

- The low-current regime is almost entirely hole current, but both carrier types are important in the high-current regime.

- The high-current regime should scale like the tunneling probability, i.e., like a negative exponent of the oxide thickness. (Disagrees with our experimental results.)

- The peak voltage is sensitive to the n^- region thickness and doping (increases with both).

Some of the obvious limitations of the model are as follows:

- The high-current regime is characterized by high injection, thus inadequately modeled.

- The turn-off point (V_{peak}) is always at the exit from the PT mode. Since the PT mode is an artifact of the model, this point cannot be accurate.

5.5   Discussion

Currently, we cannot accurately compare experimental to theoretical results. The model is both too crude in its assumptions and requires oxide parameters that are not easily obtained from experiment. Below we will first discuss several observations that could be made despite the quantitative disagreement. Next, we will elaborate on the lack of experimental data on the oxide parameters and the futility of a first principles approach to theoretical calculations of such parameters.

Finally, we will point to a new promising approach that involves measuring the oxide parameters using the MISS device and proper modeling of the semiconductor part of the device.

The most important feature of this device is its negative resistance. It has been observed by us, and by several researchers previously[13], that this negative resistance requires a tunneling barrier resulting in tunneling probability which is neither too low nor too high. In the experiments, one can change the tunneling probability by varying the oxide thickness. Indeed, devices with too thin or too thick oxides do not result in negative-resistance regions in the I/V curves. The same result is predicted by the model. The existence of a negative-resistance region indicates that a tunneling barrier exists. This is important since we passed very large currents through some of these devices, and observed "forming," i.e., a change in the characteristics the first time a high current was passed through the device. Even after the forming, the devices still exhibited negative-resistance regions, indicating that the oxide integrity was maintained.

According to the model, a significant fraction of the voltage is dropped across the oxide, in the low impedance state. This results in an electric field on the order of $10^6 - 10^7$ V/cm. Although such a high field is normally considered to cause a dielectric breakdown, our devices continue to operate in this regime. It should be noted, though, that the high field is a result of dividing a moderate voltage, on the order of a couple of volts or less, by a very thin oxide thickness and, as a result, the energy that any particular carrier could impart to the oxide is relatively small. It should also be noted, that the low impedance state is not adequately described by the model, and that significant disparities between our experimental results and the predictions of the model exist.

Due to difficulties in measuring and modeling the thin oxide, it is unrealistic to have a theoretical calculation agree with the measured I/V curve at this stage. Experimentally, we would like to know the oxide thickness, composition, and density of charged and chargeable states at the silicon-oxide interface, as well as a

measure of uniformity of these quantities. None of these is known at this stage within the precision required for modeling.

Furthermore, the atomic structure of the oxide is not well understood. It is probably amorphous with varying composition, being more Si-rich in the first 1 nm, as suggested by some experimental[14] and theoretical[15] studies of oxidized silicon. The precise atomic structure could be processing-dependent, and could change after metalization and after passing strong current through it ("forming"). In particular, the possibility of aluminum atoms diffusing into the oxide cannot be ruled out[16].

Lateral variation in thickness and composition are also very important, as localized regions with higher carrier transmission probability could contribute to conductance much more than their proportion in the total conducting area[17]. There could be non uniformity of a very fine scale, such as a slight variation in the oxide thickness near a substrate step, or a particular configuration of oxide atoms resulting in an unoccupied localized state within the oxide band gap. Our AFM studies indicate that the oxide is uniform on a 1 nm (vertical) scale, but this scale is obviously not fine enough.

Having discussed the experimental difficulties, we now consider the theoretical models, which are in no better shape. First-principles models limit themselves to one dimension, neglecting lateral variations, then proceed with the WKB approximation (far beyond its range of applicability) to integrate k_x across the oxide. k_x is obtained from the complex band structure of the oxide, typically using a 1-band[18] or a 2-band[19] model for the energy bands of the oxide[20]. To perform the integration one has to know the silicon-oxide band offsets as well as the effective masses of holes and electrons in the oxide. In view of how poorly we understand the atomic structure of the oxide, and its amorphous state, this process is highly questionable. Our model uses the numbers calculated by Habib and Simmons[6], namely, tunneling exponents of 0.92/Å and 0.93/Å for electrons and holes respectively. In the simulation results shown in Fig. 5.5, we used a hole

tunneling probability of $7d_i$ as in Faigon and Campabadal[21].

Given the difficulties associated with a first principles approach, a semi empirical approach seems much more promising. Faigon and Campabadal[21] used a semi empirical fit to the data, leading to a tunneling exponent is closer to 0.7/Å. The modeling is done by fitting the I/V curves of MOS structures, thus limited to majority carriers. The MISS device offers the possibility to obtain fits to both majority and minority carriers at the same time. This approach, however, requires a much better model of the silicon, taking into account high injection. Such modeling of the MISS has not yet been reported.

5.6   Summary

In summary, we measured the I/V curves of four types of MISS devices where the only intentional difference was the thickness of the oxide. We observed, both experimentally and by simulation, that the I/V curves of the devices are sensitive to the oxide thickness. While the simulated curves do not agree with the measured ones, the simulation provides some insight to the operation of the device. We found that the onset of the negative resistance region in the curve (V_{peak}, I_{peak}) is so sensitive to the electron and hole tunneling currents that the MISS devices could be used to characterize ultra thin oxides, given that the semiconductor part of the device could be simulated properly. The I/V curve for a particular device changed after the first switching event, but then remain essentially the same after subsequent switching events. Current densities on the order of 10^3 A/cm^2 could be driven through the ultra thin oxides without further changing the device characteristics. We believe this is the highest, non-destructive, current density through an oxide reported to date.

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