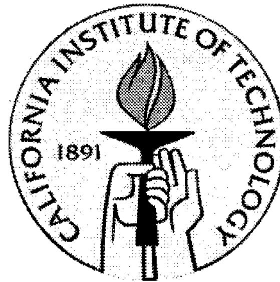
Integrated Parylene Micro Electro Mechanical Systems (MEMS)

Thesis by

Xuan-Qi Wang

In Partial Fulfillment of the Requirements

For the Degree of Doctor of Philosophy



California Institute of Technology

Pasadena, California

2000

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To my parents

my wife

and my children

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Abstract

One important goal of micro electro-mechanical systems (MEMS) development is to seamlessly interface microelectronics with the non-electronic world in an integrated manner. In the mean time, integrated micro fluidic devices and systems are expected to extract biomedical information in ways similar to how IC-chips process electrical current. Therefore, functional integration and fabrication process integration are the keys and challenges to MEMS development.

This work is first devoted to developing novel low-temperature MEMS fabrication technologies that use Parylene as a micro-structural material. A bromine trifluoride (BrF_3) gas phase silicon etching method for micromachining is then developed. Combining with the Parylene processes, BrF_3 etching method plays important roles in bulk silicon etching, the release of Parylene freestanding structures and silicon surface treatment.

The developed technology facilitates wafer scale post-CMOS integration and integrated micro fluidic systems. Using this technology, a Parylene-based electro-spray chip for protein mass spectrometry, a single chip micro check valve, an in-channel normally closed check valve, and a fully integrated shear stress sensor are successfully designed, fabricated, and tested.

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Chapter 1

Parylene as a MEMS Material

1.1 Introduction of Micro-Electro-Mechanical-Systems (MEMS)

In the last forty years, there have been three constantly asked questions for scientists and engineers, “How can we make things small?”, “How do we put small things together?” and “What are the applications?” To address these questions, a fascinating speech entitled "There is plenty of room at the bottom"[1] was given by Richard Feymann, a physicist and Nobel Laureate at Caltech, in 1959.

In the microelectronic arena, those questions have been remarkably well answered with the invention of transistor [2] and integrated circuits (IC) [3]. The complexity of ICs has doubled every two to three years since 1970. The minimum dimension of ICs has decreased from 20 μm to today’s sub-micron levels. IC-based microprocessors and microcomputers have revolutionized every aspect of our lives from dishwashers to the Space Shuttles. Moreover, the success of microelectronics industry has brought us the incredible economies of scale.

In general, integrated microsystems are being called upon to interact with the information technology and physical world. They can be used to sense and actuate, to read and write, to heat and cool, to reflect and refract, and to control fluid flows. To realize these functions, small devices, such as microelectronics, sensors, actuators, opto-electromechanical devices, etc., have to be made and assembled together. Such integrated microsystems are expected to play important roles in the areas of health care, information technology, environmental monitoring, manufacturing, and defense [4].

Since the late 1980s when a spinning micromotor made from polycrystalline silicon was fabricated on a silicon ship by researchers at the University of California at Berkeley [5], Micro-Electro-Mechanical Systems (MEMS) have gained great interests from many diverse research and engineering fields. MEMS technology has spawned from integrated circuits technology in terms of the materials and processes involved. In the last decade, numerous MEMS devices have been developed [6].

Development of MEMS devices often requires the fabrication of micromechanical structures (e.g., diaphragm, plate, cantilever beam, tip, post, cavity, channel, and nozzle). IC materials such as silicon, silicon nitride, silicon dioxide, and metals have been widely used to fashion these micromechanical parts. Many techniques have been developed based on silicon micromachining [7], such as bulk micromachining [8] and surface micromachining [9]. Bulk micromachining designates the techniques that the bulk of the silicon substrate is etched away to leave behind desired micromechanical elements. In surface micromachining, silicon substrate is primarily used as a mechanical support upon which the micromechanical elements are fabricated. Over the years, other specific MEMS technologies, such as LIGA (German acronym for X-ray lithography, electro-deposition, and molding) [10], bonding [11], molding [12], plating [13], micro stereolithography [14], micro electrical discharge machining (EDM) [15], and laser micromachining [16] have also been developed.

Although many MEMS devices are fabricated using standard IC materials and processes, most of them require chip-to-chip bonding, gluing, clamping, and other manual assembly steps to achieve a specific function. Very few of them are integrated monolithically, especially with microelectronics. This aspect poses significant technical challenges to the on-going development of BioMEMS and distributed MEMS sensing and control systems.

A "lab-on-a-chip" or a "handheld" biomedical analysis system requires integration of various micro fluidic handling functions, such as valving, pumping, heating, cooling, mixing, separation and detection. Due to the diverse methodology involved in chemical/biochemical analyses and the wide range of samples used, a self-contained, mass-produced "lab-on-a-chip" system with the same economies of scale as microelectronic components has yet to be realized. What has been reported are numerous types of discrete micro fluidic devices, such as micro valves, channels, mixers, reservoirs and pumps. Currently, to form a micro fluidic device, not only is the chip assembly process cumbersome, but the fluidic dead volume and sample contamination caused by inter-chip gluing and tubing become intolerable. Likewise, discrete multi-chip assembly will not allow MEMS devices to enjoy the same economies of scale as microelectronics. Therefore, a critical requirement for realizing these miniaturized systems is to develop an integrated microfluidic chip that contains valves, pumps, chambers and other micro fluidic components within a channel network. Such an integrated fluidic handling system is the key to a successful BioMEMS. It could be used as a general platform for specific applications, such as DNA detection, cell manipulation, and drug delivery. An integrated microfluidic chip will process fluidic samples to extract bio/medical information the way similar to IC-chip processes electronic current.

In general, functional integration and fabrication process integration are the keys to future MEMS development. Currently, the limiting factor in achieving the goal of complete on-cnip integration has been the lack of feasible technologies. One consideration of MEMS integration technology is that it has to take full advantage of mature IC technology, namely industrial IC capabilities and infrastructures.

The aim of this work is to first develop a novel micromachining technology that using Parylene as the micro structural material and gas phase bromine trifluoride (BrF_3) as the silicon etching method. The developed technology is used to make integrated micro fluidic devices and Post-CMOS fabricated micro sensors. More specifically, an electrospray ionization chip for mass spectrometry, a single chip micro check valve, an integrated micro check valve and an integrated shear stress sensor have been developed. Several novel processing techniques, such as room temperature vacuum sealing of micro cavities by Parylene deposition, silicon surface roughening by BrF_3, and several novel micro structure designs, such as twist-up tether, vacuum collapsing chamber, overlapping etching holes are also developed and can be used in making other MEMS devices.

This thesis is organized as follows:

- Chapter 1 discusses the motivations of the work and introduces Parylene material, process and previous works.
- Chapter 2 focuses on the design, setting-up and testing of gas-phase bromine trifluoride silicon etching system.
- Chapter 3 attacks the difficulties in fabricating overhanging micro capillaries and demonstrates the design and fabrication of Parylene based electrospray nozzle for mass spectrometry.
- Chapter 4 develops a single chip Parylene micro check valve that has a significant low forward flow resistance, non-detectable reverse leakage and robust performance.
- Chapter 5 demonstrates the first normally closed micro check valve that is within a micro channel network and on a monolithic chip.

- Chapter 6 realizes the successful integration of a shear stress sensor with its bias circuits on a single chip by developing Post-CMOS MEMS fabrication techniques.

1.2 Parylene as a MEMS Material

Parylene [17] and the Parylene coating process were developed in the 1950's by William F. Gorham. It was then commercialized in 1965 by the Union Carbide Corporation and widely used to protect components and assemblies in medical, electronic and automotive applications, and to preserve cultural materials and delicate antiquities. Only recently, it has been used in MEMS field [18,19,20]. This section will introduce the material properties and deposition process of commercially available Parylene.

1.2.1 Parylene

Parylene is the generic name for members of a unique family of thermoplastic polymers that are deposited by using the dimer of para-xylylene (di-para-xylylene, or DPXN). Parylene is deposited from vapor phase at room temperature and under a vacuum condition. There are three types of commercially available Parylene as shown in Fig.1-1. The basic member of the series, is poly-para-xylylene, a completely linear, and highly crystalline polymer called Parylene N. It is a dielectric material that exhibits a very low dissipation, high dielectric strength. The second type, Parylene C, has the same monomer except a chlorine atom replaces one of the aromatic hydrogens. Parylene C has a useful combination of electrical and physical properties. It also has very low permeability to moisture and other corrosive gases. Parylene D, third member of the series, has two of the aromatic hydrogens replaced by chlorine atoms at its

monomer. Parylene D has similar properties to Parylene C with the ability to withstand higher use temperatures.

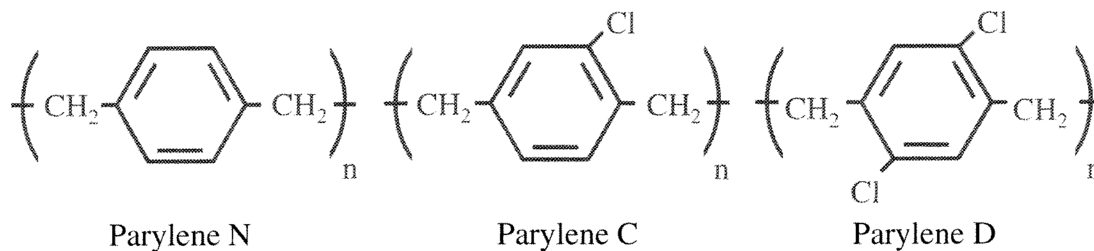

Figure 1-1 Chemical structures of Parylene

1.2.2 Parylene Deposition

The most common method of applying polymers to a substrate is by spin coating. Although simple, it always involves pinholes and intrinsic stresses. Moreover, it is inefficient for large area substrates, and leads to environmental, health, and safety issues. The most significant advantage of the Parylene process is that it is deposited at room temperature in vapor phase under a medium vacuum. There is no liquid-phase in the deposition process and the wafer temperature remains near ambient. In addition, no catalysts or solvents are involved, and no foreign substances that could contaminate coated surfaces are introduced. As a result, Parylene has many advantages over the spin-coated polymers.

The deposition process consists of three distinct steps as shown in Fig.1-2. The first step is sublimation in which Parylene is vaporized from its solid dimer form. This is accomplished by the application of heat under vacuum. The typical temperature range for this sublimation is 140°C ~ 170°C. The second step is pyrolysis, where gaseous form of dimer is cleaved into a monomer. The pyrolysis chamber is heated to above 650°C for this process. The third step is polymerization of the gaseous monomer that occurs at room temperature in the deposition chamber. The first and second steps are achieved by controlled temperatures, while

the final deposition rate is controlled by the pressure inside the deposition chamber. The typical deposition pressure is between 20 to 30 mTorr.

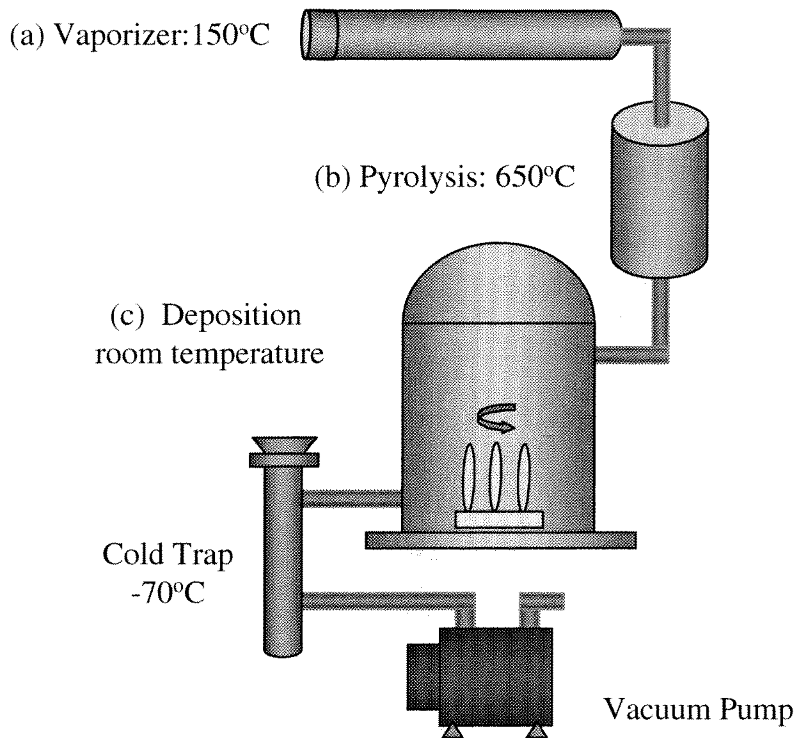

Figure 1-2 Parylene deposition system

1.2.3 Parylene Patterning

Oxygen containing plasma etching has been used in removal of organic thin films in the microelectronics industry. The applications include photoresist stripping and descumming. The etching is usually done in a plasma etcher that electrically isolates the wafers from the cathode of the plasma chamber. The etching can also be achieved by reactive ion etching (RIE), in which the wafers are placed on the powered cathode. In generating Parylene openings to make microstructures, photoresist or metals (e.g., Al, Au) are frequently used as masking materials for the etching. In the case of photoresist as a mask, the etching rates of Parylene and photoresist are found to be similar. There are other methods of etching deposited Parylene.

For example, laser micromachining has been used to expose Parylene at the tip of a fine needle [21]. In another report, openings without conventional patterning and etching has been achieved by creating localized hot spots by heated resistors during parylene deposition [22].

1.2.4 Properties of Parylene

The electrical, mechanical, thermal, optical, and other properties of Parylene N, C, and D are listed in Table 1-1 [17].

	Parylene N	Parylene C	Parylene D
Dielectric Strength (V/μm)	275	220	220
Dielectric Constant	2.6	3.1	2.8
Young's Modulus (GPa)	2.5	2.8	2.7
Yield Strength (MPa)	42	55	62
Elongation to Break (%)	20-250	200	10
Density (g/cm3)	1.10-1.12	1.29	1.42
Index of Refraction	1.66	1.64	1.67
Melting Point (°C)	420	290	380
Glass Transition (°C)	>300	240	240
Linear Coef. Of Expan. /°C	$6.9x10^{5}$	$3.5x10^{5}$	$3\text{-}8x10^{5}$
Specific Heat at 20°C (cal/g°C)	0.20	0.17	-
Thermal Conductivity at 20°C (cal/cm°Cs)	$3.0x10^{-4}$	$2.0x10^{-4}$	-

Table 1-1 Properties of Parylene N, C, and D

Since Parylene thin films are formed at a medium vacuum of approximately 20 to 30 mTorr, under these conditions the mean free path of the gas molecules in the deposition chamber is in the order of 0.1 cm. This length is much shorter than the case of metal

evaporation. As a result, Parylene thin film has high degree of conformity, which implies that it is deposited on any exposed surfaces at the same rate.

As one type of polymers, Parylene thin films are long-chain macromolecules with repeating monomers. As the monomers link together during polymerization, the macromolecules may align parallel to the substrate, leading to anisotropic properties. Cross-linking between Parylene chains provides higher rigidity.

Chemically, Parylene is inert, non-toxic and non-hazardous. It emits no volatile organic compounds during storage, handling or deposition. Parylene resists room temperature chemical attack and are insoluble in all organic solvents up to 150°C. They are also resistant to permeation by most solvents.

1.2.5 Parylene Integration Technology

The most significant feature of the technology discussed below is that every processing step involved is achieved below 120°C. In particular, Parylene, the main structural material, is deposited at room temperature. Using this approach, complicated microstructures can be fabricated by using composite multi-layers, such as Parylene, photoresist, metals (e.g., Al, Au), and amorphous silicon. In general, any one of these materials can be deposited before or after other materials. Consequently, the overall process is suitable for POST-CMOS and microfluidic integration. The major depositions and etching processes involved in the developed low temperature process are shown in Fig.1-3.

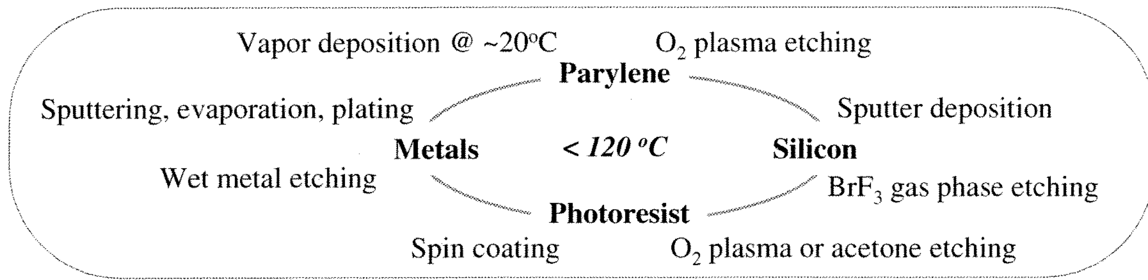

Figure 1-3 Low temperature (<120°C) MEMS technology

Parylene is not only used as micro structural material, it can be used to seal both bulk micromachined cavities (chapter 6) and surface micromachined chambers (chapter 5). Photoresist is used as a sacrificial layer material [18] and a structural layer material, such as a spacer [23]. Thermal evaporated Al and Au are used in the process as sacrificial layer (chapter 3), surface stiction reduction layer (chapter 5), and the electrode layers for electrostatic actuation. The wafer surface temperature, which is well controlled to be less than 120°C during evaporation, is the most important factor in the thermal evaporation process. Metals, such as Al, can also be sputtered on top of a Parylene surface. However, in order to achieve a good adhesion, the Parylene layer must be roughened by oxygen plasma treatment before the sputtering process. Metals can also be electroplated on top of Parylene to achieve high-aspect-ratio structure [20]. Both polysilicon and amorphous silicon can be deposited and used as sacrificial layer material by BrF_3 etching. However, due to the high deposition temperature (~800°C) of LPCVD polysilicon deposition, polysilicon must be deposited before the rest of the layers.

The developed bromine trifluoride (BrF_3) gas phase silicon etching method [24] plays an important role in bulk silicon etching, the release of Parylene free standing structures and silicon surface roughening. BrF_3 gas-phase silicon etching has been found to be crucial in Parylene micromachining. Unlike most wet-etching methods, BrF_3 does not attack the

parylene/substrate interface. Therefore, stiction issues caused by meniscus force after wet etching are avoided. This etching method is also free of plasma. Thus, plasma-induced damages to the microelectronic circuitry can be eliminated. By combining BrF_3 silicon etching with Parylene micromachining, several novel MEMS devices, such as electrospray ionization chip, micro check valves, and integrated shear stress sensors, have been successfully fabricated and demonstrated. In fabricating these devices, the developed BrF_3 silicon-surface-roughening technique has greatly improved the adhesion at Parylene and silicon interface.

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Chapter 2

Gas-Phase Silicon Etching with Bromine Trifluoride

2.1 Introduction

Silicon etching is the one of the most important steps in silicon micromachining. Many silicon-etching techniques have been developed from the matured IC fabrications. However, in order to make complex MEMS microstructures, specific silicon etching techniques are required. A crucial step in micromachining is to choose the right silicon etching method to achieve the desired structures while keeping the rest of the features undamaged.

There are several ways to categorize the etching methods. The first way is to separate the etching techniques into bulk etching [1] and surface layer etching [2]. Bulk etching targets substrate silicon, while surface etching targets polysilicon or amorphous-silicon thin layers. In terms of the states of the etchants, there are three categories of methods: wet, plasma, and vapor etching. Furthermore, as silicon-etching rates may also be different with crystal orientations, they can be separated into isotropic and anisotropic etching. In some cases, only one etching method can be applied, while in the majority of cases, the etching method employed is a matter of tradeoffs among etching quality, cost, and time. There are also cases that unique structures can only be achieved by combining two or more etching methods in certain procedures.

Bromine trifluoride (BrF_3) is a member of a family of fluorine-containing interholagens that etch silicon spontaneously in a vapor phase. Such chemicals include ClF_3, BrF_3, BrF_5, IF_5, and XeF_2 [3]. XeF_2 was first used to study the mechanisms of fluorine etching chemistry on silicon [4] and first to be used in silicon micromachining [5]. The study of pure BrF_3 [6] gas for silicon micromachining has not been reported before. BrF_3 is attractive as an etchant, as it

is in a liquid phase and has a high vapor pressure at room temperature, implying ease of use and high etching rate. Also BrF_3 is commercially available and much less expensive than XeF_2. Like the other fluorine-containing interholagens, the disadvantage of BrF_3 is that it is highly toxic and corrosive. Extreme caution and care should be taken when working with BrF_3. The physical properties [7] of BrF_3 are listed in Table 2-1.

Molar Mass	Liquid Density	Melting Point	Boiling Point	Vapor Pressure
137	2.8 kg/L	8.8°C	125°C	7 Torr

Table 2-1 Physical properties of BrF_3

In the following section, the features of gas phase BrF_3 silicon etching for micromachining are compared to other methods.

Wet (liquid-phase) chemical etching always involves surface tension effects, which can be significant when the feature dimensions are small. The meniscus force during drying can induce direct mechanical damage on fragile structures, or, cause surface stiction of large overhanging structures. Hence, there is a general need to release microstructures by silicon etching in dry phase.

BrF_3 gas-phase silicon etching has been also found to be crucial in the Parylene micromachining. Unlike most wet silicon etching methods (KOH, TMAH), gas-phase BrF_3 does not attack the Parylene/substrate interface. Thus, it is an ideal method to release Parylene freestanding structures from silicon.

Most common dry-phase silicon etching methods are plasma and reactive ion etching (RIE), which developed from IC technology. Although widely used, plasma etching has several constrains. First, plasma silicon etching has limited selectivity to silicon dioxide and

nitride and it can not provide large undercut when used to release microstructures. Since ion bombardments are more directed into the vertical direction, the vertical etching rate is therefore much faster than lateral etching rate. Moreover, the ion bombardment and associated plasma radiation can induce damages to any microelectronic circuitry that might be on an etching substrate. It is, therefore, advantageous to have a pure gas-phase silicon etchant that is both selective and tension-free, such as BrF_3, which can etch silicon spontaneously in the gas phase. The BrF_3 etching is isotropic, and thus can provide much larger undercuts than plasma etching. It also offers very high selectivity for aluminum, silicon dioxide, silicon nitride, Parylene, and photoresist. The etching is achieved without plasma. Therefore, there is no plasma-induced damage to microelectronic circuits nor need of a plasma source. These properties make it an extremely useful etchant for post-CMOS fabrication.

2.2 Etching Chemistry

The etching mechanism of BrF_3 with silicon is believed to be the same as that of other fluorine-containing interholagens reported in [3,4]. It is described by the following sequence of steps:

(1) nondissociative adsorption of gas-phase species at the surface of the solid etched.

(2) dissociation of this absorbed gas.

(3) reaction between adsorbed atoms and the solid surface to form an adsorbed product molecule (SiF_4);

(4) desorption of the products molecule into the gas phase.

Although the physics and chemistry of this reaction are still not fully understood, the final volatile products of the etching are confirmed to be SiF_4 and Br_2 [6].

$$BrF_3 + Si \rightarrow Br_2 + SiF_4 \quad (2.1)$$

2.3 Etching Apparatus and Operation

The etching system [8] shown in Fig. 2-1 consists of a reaction chamber, a vapor reservoir, nitrogen purge, xenon dilution and a vacuum subsystem. The volume of the reaction chamber and expansion chamber is 2200 cm^3 and 350 cm^3 respectively. Gases flow is controlled by switching the corresponding valves. Pressures in the reservoir and reaction chamber are monitored by a Baratron and a pressure gauge. The construction materials are stainless steel and brass. For safety reasons, the whole system is set up inside a fume hood with plenty of ventilation. Etching experiments are conducted in pulses instead of continuous BrF_3 flow etching for the following two reasons. First, continuous flow of BrF_3 vapor through the system etches silicon too fast, making the etching difficult to control. Second, continuous BrF_3 flow has a low etching efficiency. Unconsumed BrF_3 vapor can enter the pump system and generate safety concerns and cause pump failure.

The process starts with loading the wafers into the reaction chamber. Both the reaction chamber and vapor reservoir are pumped down below 10 mTorr. The chamber separation valve is then closed, and a fixed amount of BrF_3 is introduced into the vapor reservoir. The chamber separation valve is then opened to allow BrF_3 vapor to enter the reaction chamber. Enough time is given to make sure the entire BrF_3 vapor inside the reaction chamber is consumed. Finally, the chamber separation valve is opened and both the chamber and reservoir are pumped down. The above procedure is then defined as one pulse of the etching. At room temperature and 6 Torr of pressure in the vapor reservoir, the number of BrF_3 molecules in one pulse is calculated to be 1.29 x 10^{-4} mole. When balanced with the reaction chamber, there

will be 1.1 x 10^{-4} mole of BrF_3 in the chamber and theoretically up to 2.3 mg of silicon will be etched away according to equation 2-1.

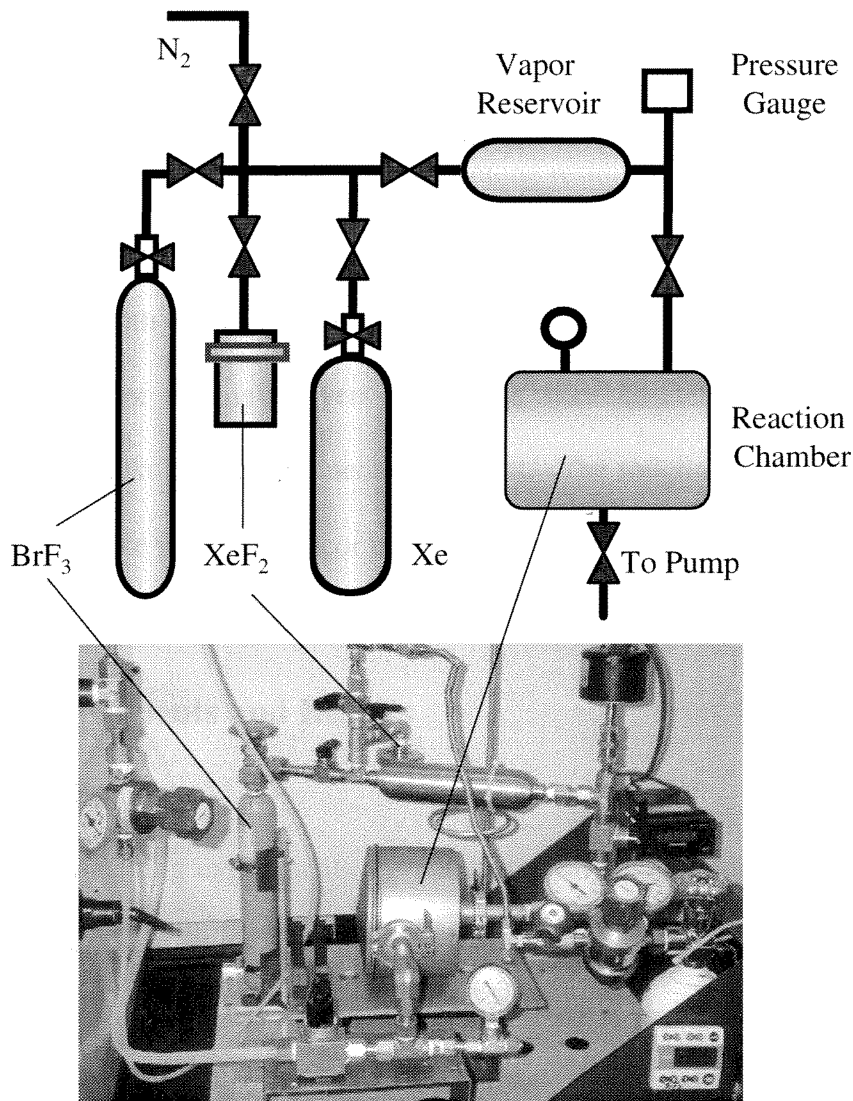

Figure 2-1 BrF_3 silicon etching apparatus

Sample Preparation

Silicon etching experiments are conducted on silicon die with edges covered by hard baked photoresist, which is shown later to have a very low etching rate. To remove the native oxide on the silicon surface, all the samples are etched in buffered hydrofluoric acid for 10 seconds followed by deionized water rinse and nitrogen drying before etching. Samples are

then loaded into the reaction chamber and pumped down to 10 mTorr. Samples are kept in the vacuum for at least 10 minutes before starting the first BrF_3 pulse. The experiments show that N_2 drying is enough to produce reliable and repeatable etching, and baking the sample at high temperature is not necessary. Acetone cleaning should be avoided; otherwise, a white polymer like film will form on the silicon surface when acetone residue is exposed to BrF_3 vapor. This white film will stop further etching.

The etching depth and the undercut are measured under a microscope with a calibrated focus. The thickness of the mask layers before and after the etching is determined using a Nanospec thin-film thickness measurement instrument. The roughness of the silicon surface is measured using a surface profiler (Tencor α-step 200).

2.4 Etching Experiments and Results

2.4.1 Bulk Silicon Etching

Bulk silicon etching experiments are conducted on silicon chips with various opening sizes. Different masking materials such as thermal oxide, LPCVD silicon nitride, hard baked photoresist (AZ4400 and AZ1518) and Parylene are used as the mask materials to study the etching rate and etching selectivity. Checkerboard openings of 800μm $\times$ 800μm made using several masking materials on a silicon wafer are tested to study the etching selectivity. The etching selectivity of silicon to other materials is found to be greater than 3000:1 for LPCVD silicon dioxide, and 1000 to 1 for hard baked AZ 4400 and AZ1518 photoresists. The etching rate of silicon nitride depends on the quality and silicon concentration of the nitride layer and results in a selectivity range of 400:1 to 800:1. In the case of most metals, like aluminum, copper, gold, and nickel, once exposed to BrF_3, a passivated non-volatile metal fluoride layer is

formed on the metal surfaces and further reaction is stopped. The silicon etching selectivity to these metals is greater than 1000 to 1.

To characterize the etching rate, etching depths of samples with 800 μm circular windows are measured at various gas pressures by using constant etching pulse duration of 10 minutes. Fig. 2-2 shows the vertical etching depth as a function of the number of pulses at the different BrF_3 pressures. For this particular window opening, the etching rate ranges from 10 μm/pulse up to 140 μm/pulse, corresponding to an average etching rate range from 1 μm/min up to 14 μm/min.

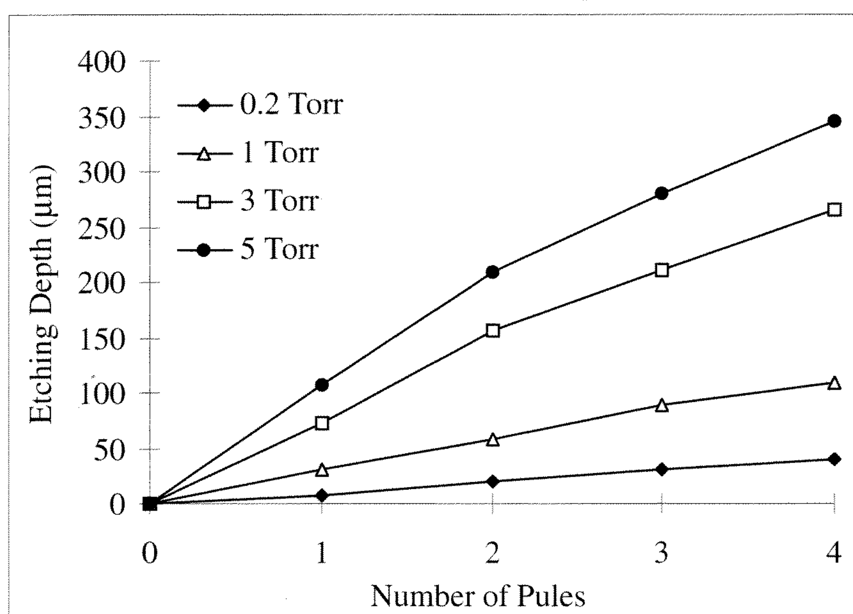

Figure 2-2 Etching rate vs. BrF_3 gas pressures

using a sample with a 800 mm circular opening

Second, at a constant BrF_3 pressure of 1 Torr, etching rates of different pulse duration are measured. The pulse duration time is varied from 20 seconds to 20 minutes. Fig. 2-3 shows the silicon mass etched away versus pulse duration time at different window opening

areas. The samples with different openings are tested separately. For each data point, a new silicon sample is used.

Fig. 2-3 shows that not only the etching rate but also the system etching efficiency is a function of exposed silicon area. Assuming all the BrF_3 gases in the reaction chamber are consumed by silicon etching, then 2.3 mg is etched away. The efficiency of the etching system is defined as the ratio of the silicon mass loss in real case to the ideal value (2.3mg). The maximum efficiency from Fig. 2-4 is 80% for the 4-inch bare silicon wafer (160 cm^2).

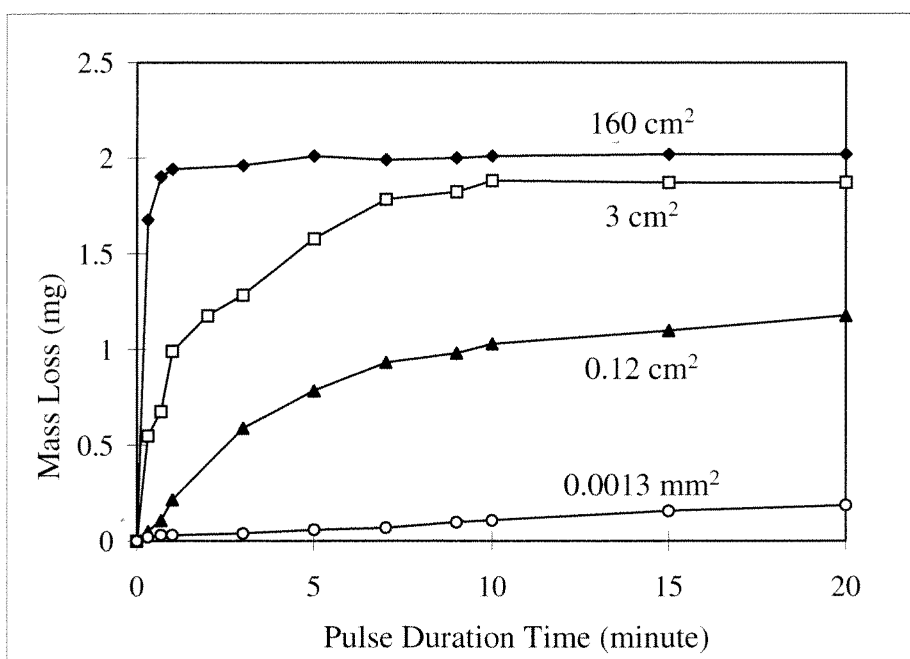

Figure 2-3 Si mass loss vs. pulse duration time for different exposed Si areas

Third, etching rates of various opening areas are investigated. Circular openings with diameters from 4 μm to 4 mm are used. Note that in this case all the samples are etched in the same load. The etching is conducted under 1 Torr of BrF_3 gas pressure and 15 minutes of pulse duration. The etched depth and undercut of these samples versus the mask opening area are plotted in Fig. 2-4.

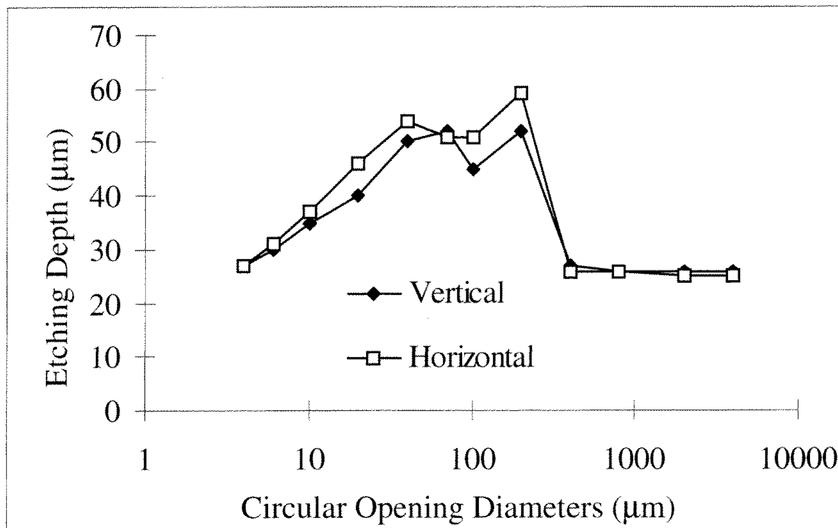

Figure 2-4 Vertical and horizontal etching depth vs. opening size

with diameters from 4 μm to 4 mm

Fig. 2-4 indicates that the etching depths of the samples having 40μm to 200μm window openings are about 50% more than the samples of larger openings. For the samples with opening diameters under 40 μm, the etching depths are reduced with decreasing opening sizes. To confirm the data, another series of experiments are done with the same type of samples using 500 mTorr, and 15 consecutive pulses (1min/pulse). All the samples are etched at the same time. The results are shown in Fig. 2-5. Compared to the last experiment, the etching depth differences of the various samples have not been reduced significantly, even though BrF_3 is refreshed 15 times to achieve similar etching depths.

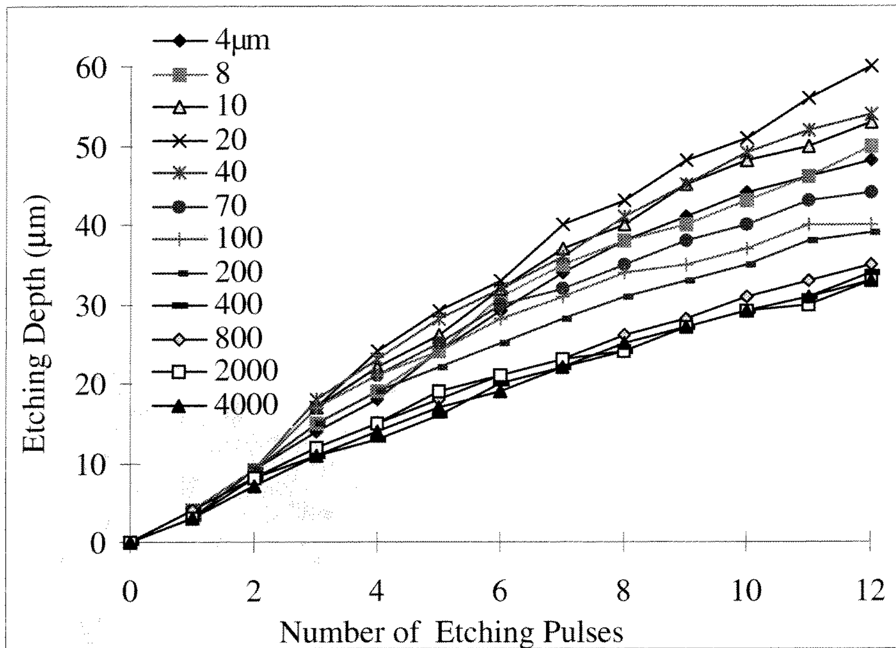

Figure 2-5 Vertical etching depth vs. number of pulses

Fig. 2-6 shows bulk silicon etching though a 40μm SiO_2 mask opening. The buckling of overhanging SiO_2 thin film caused by compressive stress is obvious.

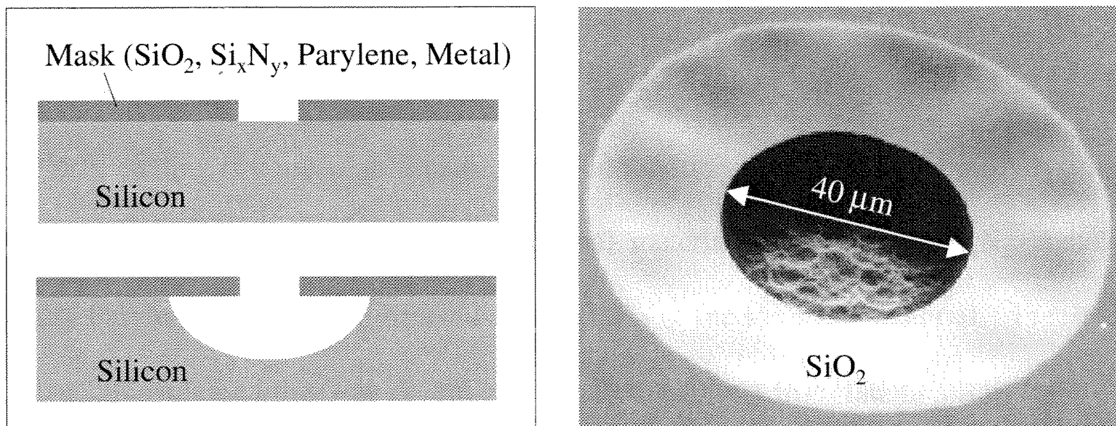

Figure 2-6 Gas phase BrF_3 bulk silicon etching

Also notice from Fig. 2-6, the BrF_3 etched silicon surface is very rough. For example, the surface roughness is about ± 0.2 μm after 2 μm thick silicon removal. To reduce the etched surface roughness, inert gas, such as Xe can be added into the reaction chamber to increase the

gas pressure during etching. In this case, the mean free path of the reactant gas molecules can be significantly reduced by Xe dilution, thus the etched surface is less rough. The compromise is that by adding the dilution gas, the etching rate and efficiency is reduced. Fig. 2-7 shows the etched silicon surface with and without Xe gas dilution.

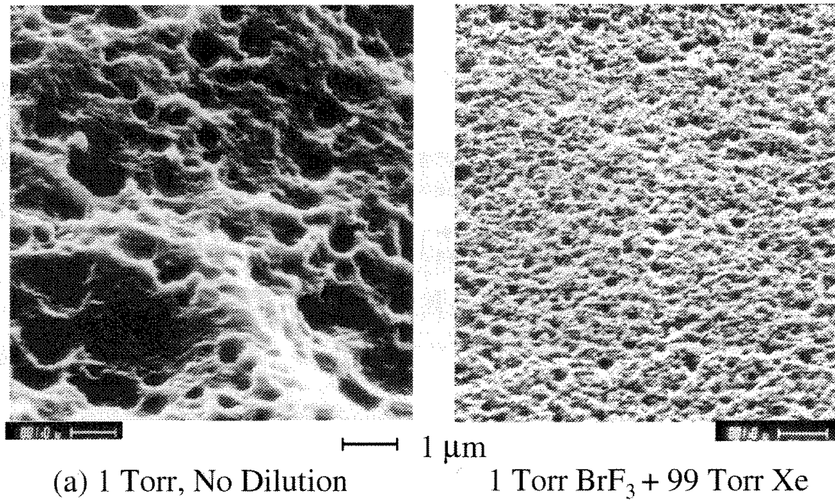

Figure 2-7 BrF_3 etched silicon surfaces

2.4.2 Surface micromachining with BrF_3

BrF_3 etching is a useful releasing technique for surface micromachining. Polysilicon or amorphous silicon can be used as the sacrificial materials, while SiO_2, Si_xN_y, metal, and especially Parylene thin film can be used as the masks or the structural material. Freestanding microstructures released this way do not have stiction resulting from the meniscus force and/or cracking that takes place in wet etching.

Shown in Fig. 2-8 are the surface micromachined channels and membranes with 0.5 μm silicon nitride and 1 μm Parylene as the structural layer and polysilicon as the sacrificial layer material. An interesting phenomenon is noticed when the polysilicon is etched to create the

Parylene channels and chambers, whereby the etching rate along the edges of the internal sidewall of the channels and chambers is faster. The reason has yet been further investigated. The channel etching rates of microchannels with a variety of widths are plotted in Fig. 2-9. Note that there are not significant etching rate differences.

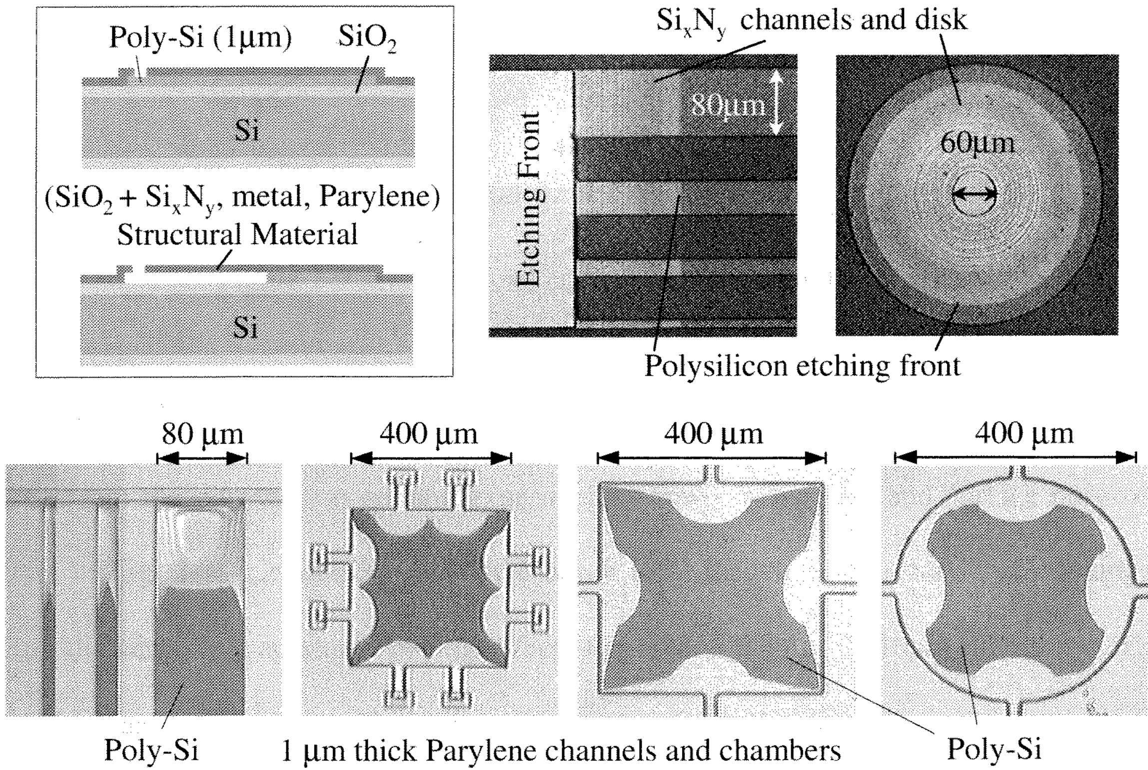

Figure 2-8 Si surface micromachining using polysilicon as sacrificial layer

Si_xN_y and Parylene as structure layers

Notice the interesting phenomenon that etching along the Parylene sidewalls are faster.

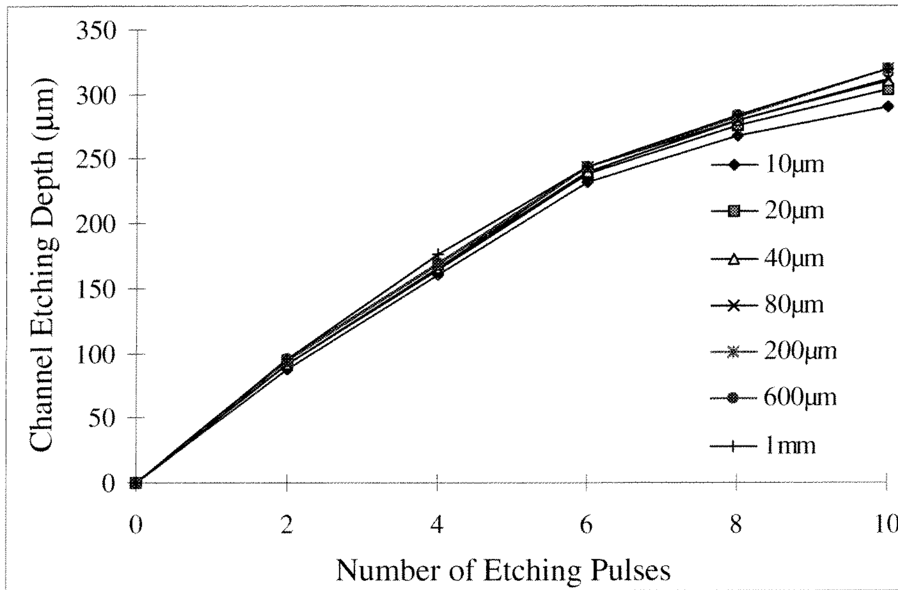

Figure 2-9 Microchannel etching depth vs. number of pulses

2.5 Etching Process Analysis

From the bulk silicon etching experiments shown in Fig. 2-4 and surface polysilicon etching in Fig. 2-9, it is noticed that there exists local loading effects for large openings (> 200μm diameter) and aperture opening effects for small openings (< 10μm diameter). These two effects are caused by the formation of a local BrF_3 depletion region. Consequently, the overall etching rate of the system is diffusion limited.

Silicon etching with gas phase BrF_3 belongs to a heterogeneous reaction sequence. In such a sequence, mass transfer of reactants first takes place from the bulk gas to the external surface of the wafer. The reactants then diffuse into the mask openings and reach the silicon-etching front. These two diffusion steps can be described as external diffusion and internal diffusion, respectively. They limit the rates of reaction at different mask opening sizes. The two ranges, in which these two effects limit the reaction rates accordingly, can be qualitatively described by the Knudsen's number,

$$K_n = \frac{\lambda}{L} \tag{2.2}$$

where λ is the mean free path and L is the charateristic length. The mean free path is the average distance between two concecutive collision of gas molecules. L can be choosen from the smallest dimension of the mask opening. In bulk silicon etching, L is the diameter of a circular opening or the short side of a rectangular opening. In polysilicon sacrificial layer etching, L is usually the channel height. λ [9] for air at 300K can be calculated as

$$\lambda = kT/[\sqrt{2}\pi\xi^2 P] \approx \frac{50}{P(Torr)}(\mu m) \tag{2.3}$$

where T = *300K*, ξ is the molecular diameter, and P is the reaction pressure. In this case, for 1.0 Torr of reaction pressure, λ is 50 μm.

If $K_n \rightarrow 0$ ($L >> \lambda$) the etchant gas is in the viscous flow range, the etching in this case is external diffusion dominated. If K_n close or larger than 1, then the gas is in free moleculor flow range, the etching is then internal diffusion doninated. As shown in Fig. 2-10, the microchannel etching and small hole bulk etching are limited by the internal diffusion, where a gas molecule collides with the internal channel surface much more frequently than with another gas molecule. This kind of mass tranfer or etching rate is independent of the gas pressure. This phenomenon is confirmed by the channel etching experiment which conducted etching at different pressure from 200 mTorr to 6 Torr. When the etchant gas molecules have to tranvel a long distance to reach the silicon etching front, the overall etching rate is reduced as shown in Fig. 2-9. Moreover, the etching efficiency can also be reduced in the case of internal diffusion limited case. This implies the BrF_3 gas are more likely to be consumed by attacking the reaction chamber materials and masking materials.

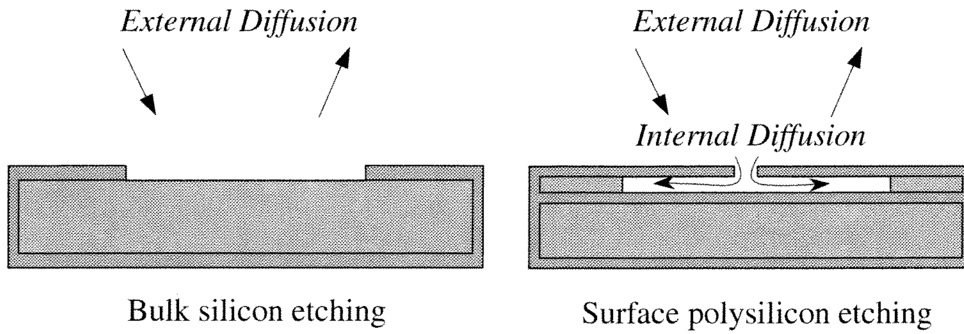

Figure 2-10 Diffusion limited etching (External and internal diffusion)

The external diffusion time can be approximated in a simplified one-dimensional case. According to the one-dimensional diffusion equation [10]

$$\frac{\partial C(x,t)}{\partial t} = D_e \frac{\partial^2 C(x,t)}{\partial^2 x} \tag{2.4}$$

where $C(x, t)$ is the concentration of BrF_3 and D_e is diffusion coefficient, which has a typical value for gas as follows:

$$D_e \approx 10^{-1}\, cm^2/sec \tag{2.5}$$

Assuming no convection, and fast reaction at $x = 0$, which implies

$$C(0,t) = 0 \tag{2.6}$$

while at $x = 10\ cm$, the boundary condition can be assumed as

$$C(10cm,0) = C_0 \tag{2.7}$$

The solution of diffusion equation (2.4) is a error function:

$$C(x,t) = C_0[\,erf(\frac{x}{2\sqrt{Dt}})] \tag{2.8}$$

Considering the BrF_3 concentration at $x = 10\ cm$, which is the length of the reaction chamber, the concentration vs. time data from equation (2.8) are plotted in Fig. 2-11.

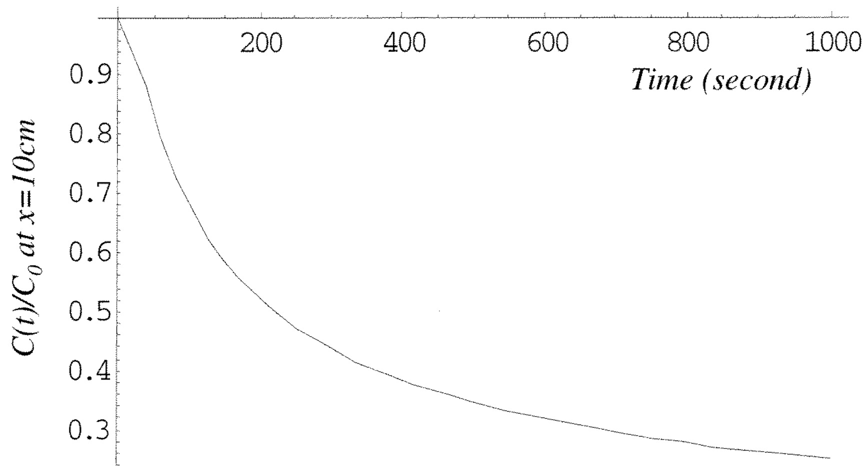

Figure 2-11 BrF_3 concentration vs. time in the one-dimensional diffusion model at x = 10 cm

As in Fig. 2-11, it takes more than 10 minute to reach a concentration ratio of $(C(t)/C_0)>80\%$ at $x = 10$ *cm*. On the other hand, as shown in Fig. 2-3, the etching can be finished with in one minute if the exposed silicon area is large (4-inch diameter wafer). Therefore, the external diffusion, meaning the mass transfer from the bulk gas to the substrate surface, is an important factor that can affect the silicon etching rate and system etching efficiency. In practice, in order to increase the etching efficiency by reducing the time of external diffusion, we designed a small reaction chamber that can just accommodate a 6-inch wafer.

2.6 Summary

A gas phase BrF_3 silicon etching system is designed, built and characterized. Silicon bulk micromachining and surface micromachining are achieved by this isotropic room temperature etching method. In many applications, it has tremendous advantages over wet etching and plasma etching. Consistent high etching rate is achieved with using various masking materials. The etching is conducted in a pulse mode, in which external and internal diffusions are the rate-limiting step of the etching.

Overall, gas-phase BrF_3 silicon micromachining is simple, fast, maskable, and repeatable. It plays important roles in Post-CMOS MEMS fabrication as detailed in chapter 6.

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Chapter 3

A Parylene MEMS chip for Electrospray Ionization Mass Spectrometry

3.1 Introduction

A central problem in protein biochemistry is that many of the medically important proteins are present in amounts that are too little to permit isolation and analysis. Current biochemical analysis of proteins require microgram (hundreds of picomoles) of sample, amounts that preclude the analysis of many proteins.

Over the past decade there has been increasing interest in the development of miniaturized chemical analysis systems using MEMS technology. The goal is to create micro scale total analytical systems (μTAS) [1] that would combine sample handling and measurement into a single package with a high level of automation [2]. MEMS technology will have a great impact on the field of protein biochemistry than any other biomedical technology currently being developed. It will offer the following advantages:

(1) Reducing the minimum sample requirements of biochemical analysis.

(2) Increasing the analysis sensitivity, efficiency and speed.

(3) Reducing the costs by reducing the labor time and offering disposable chips.

(4) Opening new areas of biomedical research and medical diagnosis.

However, due to the diversified process of chemical/biochemical analysis and a wide range of samples involved, a self-contained, mass produced "lab-on-a-chip" with the same economy of scale as electronic components has yet to be realized. Although such a μTAS or a

"lab-on-a-chip" is not a commercial product today, the vital components such as MEMS chromatographs, and MEMS capillary electrophoresis required for such a system, have been under extensive development. In the meantime, there are still numerous connections to macroscopic components such as power supplies, computers, and laser light sources. Consequently, an important task then, is to use MEMS based components and integrate them with commercially available macroscopic instrumentation. MEMS integrated in larger analytical systems are valuable both in terms of developing the technology and as practical interim solutions to real world problems.

Electrospray Ionization Mass Spectrometry (ESI-MS) is a powerful analytical tool that has been broadly applied to biomolecular structure analysis [3-6]. Since the most dangerous invaders of the human body- notably viruses – are protein-based. To synthesize effective drugs, we first need precise information on the make-up and structure of the proteins that they will be acting against. This analysis has traditionally been done by chemically breaking off constituent amino acids one by one and sequencing the entire protein in this way. Since the relative mass of a protein may be many hundreds of thousands and the mass of an individual amino acid as low as 75, this represents a rather painstaking way of sequencing and analysis. With ESI-MS, detailed information about molecular weights and structures can be derived from extremely small sample quantities. Applications include the sequencing and analysis of peptides and proteins; studies of noncovalent complexes and immunological molecules; DNA sequencing; and the analysis of intact viruses.

3.1.1 Mass Spectrometry (MS)

The history of mass spectrometry began with J. J. Thomson (University of Cambridge), who constructed the first mass spectrometer (then called a parabola spectrograph) in the 1910s.

In the last thirty years, mass spectrometers dramatically proliferated both in terms of new types developed and number of applications in scientific research and industry. They have been used in the discovery of isotopes, the exact determination of atomic weights, the characterization of new elements, quantitative gas analysis, identification of trace pollutants and drugs, and the characterization of molecular structure. Mass spectrometry expanded into biomedical applications in the 1970s.

A mass spectrometer is an analytical device that determines the molecular weight of chemical compounds by separating the molecular ions in magnetic and electric fields according to their mass-to-charge ration (m/z). Fig. 3-1 is an illustration of the basic components of a mass spectrometry system used in biochemical analysis.

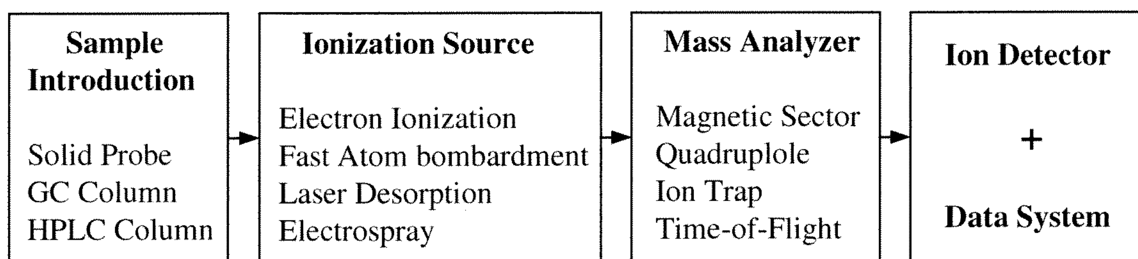


Figure 3-1 Mass spectrometry system

Biochemical samples can be introduced to mass spectrometer directly via solids probe, or in the case of mixtures, by the column of gas chromatography, high performance liquid chromatograph, capillary electrophoresis, etc. Samples from these devices are transported into the gas phase, achieve ionization by various ionization techniques, and then directed into the inlet of mass spectrometer with some kinetic energy. The heart of a mass spectrometer is its mass analyzer, in which ions with different mass, velocity, and charge are moved differently and separated by the controlled electromagnetic fields. Different kind of analyzers can be used, magnetic, quadruplole, ion trap time of light, etc.

As an example, a typical ion trap mass analyzer [5] is illustrated in Fig. 3-2.

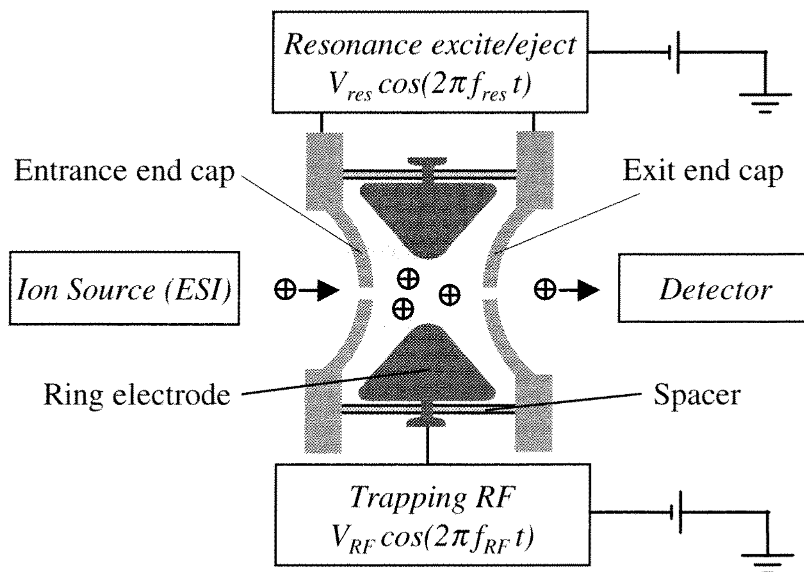


Figure 3-2 A quadrupole ion trap [5]

It is a three-electrode device; a doughnut-shaped central ring electrode is sandwiched between two identical end cap electrodes. A negative DC offset is applied to all three electrodes to inject positive ions (from electrospray, as detailed in the following section). A three-dimensional quadrupole field is formed when a suitable RF voltage V_{rf} is applied to the ring electrode. At certain RF quadrupole field, all ions above a specified m/z ration are strapped within the volume described by the electrodes. When the RF voltage is increased and a dipole signal V_{res} is applied to the end caps, resonance excitation and / or resonance ejection of the ions occurs. Ions of higher m/z ratios become sequentially unstable and exit through perforations in the end cap electrode. An ion detector is placed outside the end cap to detect the ejected ions and the signal is registered.

The result of such a process is a mass spectrum that can provide molecular weight or even structural information. The primary advantage of an ion trap mass analyzer is that tandem mass spectrometry (MS/MS, MS^n) can be performed without multiple analyzers. It also offers high scan speed, high ion transmission, low cost, small size and simple operation.

3.1.2 Electrospray Ionization (ESI)

Electrospray Ionization (ESI) is a technique used to produce gas phase ions from a liquid solution at around atmospheric pressure. As a method of electrostatic dispersion of liquids, electrospray existed long before its application to MS. A schematic representation of process [5] in ESI is illustrated in Fig. 3-3. When a strong electric field is applied between a capillary tip and a ground plate, positively charged droplets begin to leave the capillary orifice through what is known as a "Taylor cone"[7-9]. In the absence of solution, the electric field at the tip is given by [5, pp. 9]

$$E_c = \frac{2V_c}{r_c} ln^{-1}(\frac{4d}{r_c}) \tag{3.1}$$

where r_c is the radius of the capillary, d is the distance from the tip to the planar counter electrode, and V_c is the potential applied. To form a Taylor cone and initiate a droplet spray, a typical value for E_c is in the order of $10^6 V/m$.

A charged-residue model was proposed by Molcolm Dole [8]. The fine spray formed by the ejected droplets is electrostatically attracted to the ground electrode (MS inlet). Dry gas, heat, or both are applied to the droplets before they reach the ground electrode (enter MS inlet) to enhance the evaporation of solvent from the droplets. As a droplet decrease in size, its surface-charge density increases. This results in reaching the Rayleigh limit [5, pp. 20]:

$$q_R = 8\pi(\varepsilon_0 \gamma R^3)^{1/2} \tag{3.2}$$

where q_R is the charge carried by the droplet with a radius R. The Rayleigh equation gives the condition at which the electrostatic repulsion becomes equal to the force due to the surface tension γ, which holds the droplet together. Above this limit, coulomb repulsion overcomes surface tension and the droplet breaks up into offspring droplets.

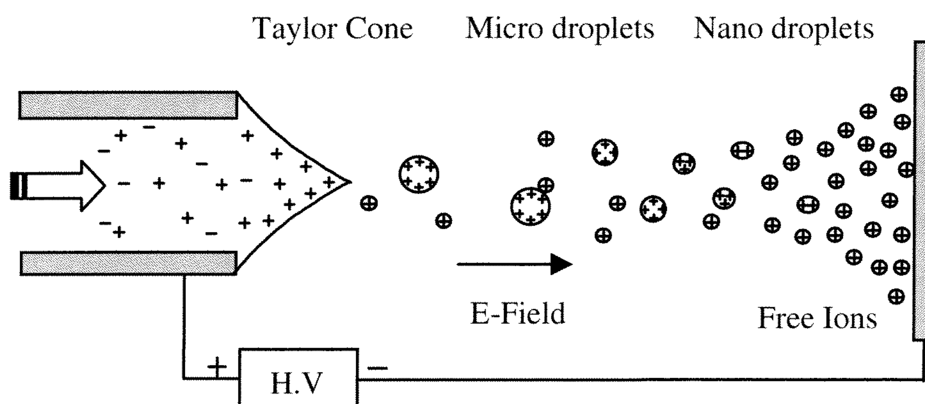


Figure 3-3 Schematic of major processes occurring in electrospary [5]

Each offspring droplet would repeat this sequence, ultimately producing droplets containing only one solute molecule. Such a molecule is a free ion retains some droplet charge after all solvent had evaporated. This process usually takes less than 1msec before a free ion reaches the MS inlet. The charged droplet stream leads to an electrical current *I*, which is generally less than 1μA.

The voltage or electric field required to onset electrospray depends on the surface tension of the solvent and the concentration of electrolyte ions (usually larger than 10^{-6} mol/L). If the applied electric field is too high, corona discharge between the ES capillary and its counter electrode will take place and partially suppress the ES process. Some discharge-suppressing gases, such O_2 and SF_6 have been used around the tip to suppress the discharge by capture of electrons.

3.1.3 ESI-MS

The revolution in the analysis of biomolecules by mass spectrometry began with the discovery of fast atom bombardment (FAB) in 1980. Since then two ionization techniques have had a major impact on the ability to use MS for the study of large biomolecules: Electrospray ionization (ESI) and matrix-assisted laser desorption / ionization (MALDI) [4].

They have made it possible for large biomolecules to be analyzed by low-cost instruments such as quadrupole, ion trap, and TOF mass spectrometers with high sensitivity, specificity, and speed. Four features of electrospray ionization set it apart from other mass-spectrometric ionization techniques.

The first unique feature of ESI is its ability to create of highly charged forms of very high molecular weight compounds. Such large multiply charged ions could be analyzed on virtually all types of mass spectrometers.

Secondly, it is possible to use ESI-MS to analyze mixtures of proteins in a single experiment. On the other hand, a protein that has been fragmented into pieces will result in a spectrum which shows a series of peaks, each one differing by the mass of one amino acid, allowing the whole protein to be sequenced in a single experiment, with a high degree of accuracy.

A third unique feature is the extreme "softness" or “mildness” of the ESI process, which allows noncovalent interactions between molecules in solution to be preserved in the gas phase. Since a large portion of organic chemistry and biochemistry involves ions in solution, the fourth unique advantage of ESI is its ability to transfer ions from solution to the gas for mass spectrometric analysis. Therefore, ESI is naturally compatible with many types of separation techniques, particularly those most suitable for separations of mixtures of larger molecules, such as various categories of liquid chromatography (LC), as well as capillary electrophoresis (CE).

In recent years, significant advances have been made with respect to various aspects of the capillary LC-MS technology. ESI is widely used to connect LC to MS. Under normal

operating conditions (using sheath gases or sheath liquids), ions are dispersed throughout a large volume in front of the orifice to the mass spectrometer (Fig. 3-4(a)).

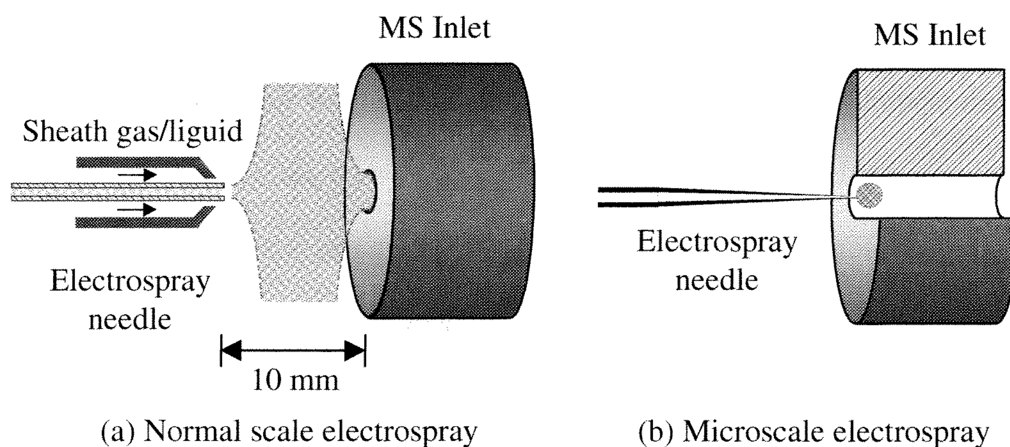


Figure 3-4 Schematics of ESI to MS interface

Wilm et al. [10] demonstrated that using very small needle dimensions, it was possible to generate ions within the vortex of gas flow into the mass spectrometer (Fig. 3-4). The result is a dramatic increase in the efficiency of ion transport into the mass spectrometer. For very small electrospray needle dimensions (5μm ID), the voltage required for stable spray is greatly reduced (<1000V) and stable electrospray conditions can be achieved at very low flow rates (<20 nl/min). Davis, *et al* [11] have succeeded in combining capillary chromatography with micro electrospray. They have discovered that stable electrospray operation can be achieved over a broad range of flow rates (20-200nl/min) and solvent compositions (0% -100% aqueous) without the use of sheath gases and sheath liquids. As a consequence, the micro electrospray source is the ideal interface for on-line, gradient LC-MS analyses.

3.2 Microchip based ESI-MS

3.2.1 Motivation

Some progress has been made to scale down the dimensions of ion trap mass analyzers [12, 13], and a serious effort has been made to create a chip based quadrupole mass analyzer [14, 15]. However, the complexity and capabilities of modern tandem mass spectrometer systems will not be achievable in a micromachined format any time soon.

Because of the nature of the electrospray ionization process, sample preparation is a major consideration. The presence of buffer salts suppresses sample ionization and increases spectral complexity. Many applications require working with complex mixtures that necessitate some degree of separation prior to mass analysis. Proteins, in particular, require enzyme digestion to readily access the sequence information that forms the basis for proteomic research. Sample preparation would benefit greatly from MEMS devices that would integrate multi-step processes in a single low cost disposable unit. There has already been considerable progress in achieving electrophoretic separations in planar chip formats. Consequently, there is great interest in developing an effective electrospray ionization source on a chip to couple these processes to mass spectrometry.

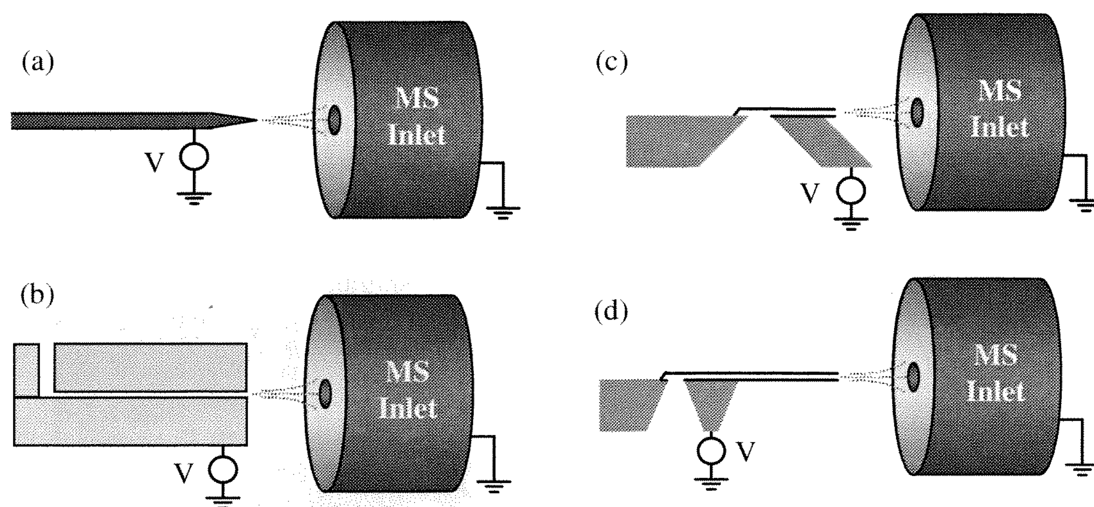
3.2.2 Recent Works of Microchip Based ESI-MS

Typical micro-fluidic structures in microchips are micro-channels produced in planar silicon or glass substrates. Photolithography techniques are used to first pattern the surface of the substrate and then selectively etch channels [16,17]. A cover is applied to complete the micro-capillary structure. Karger and co-workers [18] and Ramsey and co-workers [19] have electrosprayed directly from a channel opening at the edge of a chip (Fig. 3-5(b)). With a high

voltage differential between the chip and the mass spectrometer, a Taylor cone is formed in the surface of the liquid emitting a spray of charged droplets. The principal drawback to this approach is the tendency for the liquid to spread out over the surface of the chip. Once this happens, the volume of the liquid pool supporting the Taylor cone can easily exceed the total volume of the channels on the chip. This would preclude coupling to any on-chip separation. Confinement of the liquid to the channel opening can be achieved provided a sufficient hydrophobicity difference exists between the surface of the chip and the sample solution [18]. Another approach is to attach a conventional capillary emitter to a chip [20-23]. This is difficult to do without introducing a certain amount of void volume and precludes mass production using batch processes. Recently, Henion and co-workers reported micromachining electrospray nozzles in the surface of planar glass chips that yielded good electrospray spectra [24]. The design is well suited for batch processing although the very short length of the nozzle, formed by etching away the surrounding surface material, may prove problematic if solvent flow rates are not carefully controlled. Finally, Foret and co-workers have demonstrated a microfabricated electrospray source that utilizes an integrated gas nebulizer to atomize liquid flow from a port on the side of a chip [23]. This design effectively prevents droplet formation at the port and is compatible with on chip separations. The CE separation of a simple peptide mixture with subsequent mass analysis was demonstrated with this device.

An overhanging capillary that extends away from the bulk of the chip can provide two obvious advantages for ESI over the blunt-edged orifice [25]. (Fig. 3-5) It minimizes the wetted surface area at the tip, which becomes important for reducing the volume of the Taylor cone size. An overhanging capillary also minimizes interference with the electric field required for electrospray.

Previously a chip based electrospray source was first reported by Desai *et al.* (Fig. 3-5(c)) at Caltech [25, 26]. ESI-MS using the fabricated device was successfully demonstrated. Layers of silicon nitride were used to construct hollow needles projecting beyond the edge of a silicon wafer. Although suitable spectra could be obtained using these devices, considerable difficulties were encountered in optimizing the fabrication process, particularly with respect to creating longer channel and needle structures [26, 27]. The fabrication technology has since changed and made the ESI chip (Fig. 3-5(d)) practical [27, 28]. The new micromachining process [27] is far less complicated and the resulting devices are much more versatile and robust.



(a) Conventional Fused Silica Capillary (c) MEMS Overhanging Si_xN_y ESI Nozzle [25]

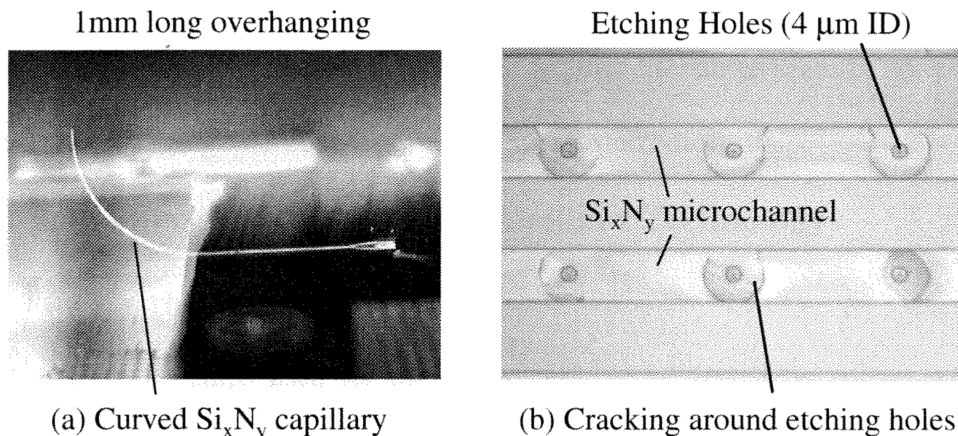
(b) Bonded Glass Slides [18] (d) 2.5mm Parylene Capillary [27]

Figure 3-5 Recent works in ESI for MS

3.3 Fabrication Challenges of MEMS ESI-MS Interface Chip

3.3.1 Problems of the Previous Si_xN_y Nozzle

As a first step in investigating the feasibility of a MEMS interface between the chip and the MS, our group previously developed a micron-sized electrospray nozzle and demonstrated its application for ESI-MS. But the Si_xN_y ESI capillary suffered from numerous disadvantages. For example, the total length of the microchannel (including the overhanging part) is limited to less than 500 μm, due to the prolonged time of sacrificial material (PSG or Polysilicon) etching. In the meantime, the outward sloping sidewall combined with the short length of the silicon nitride nozzle limited the tip to inlet distance as well as interfering with the electric field profile at the tip (Fig. 3-5(c)). Furthermore, it is well known that fabrication of mm-long silicon nitride overhanging structures pose significant challenges. Si_xN_y capillaries longer than a few hundred microns curved significantly as shown in Fig. 3-6(a) due to film stress gradients (typically 200MPa for LPCVD Si_xN_y).



(a) Curved Si_xN_y capillary (b) Cracking around etching holes

Figure 3-6 Intrinsic stress caused curving and cracking in Si_xN_y overhanging capillary structures [26, 27]

To achieve channels longer than a few hundred microns long, etching holes on Si_xN_y channels were needed and had to be sealed after sacrificial layer etching. These etch holes not only complicated the process, but the resulting stress concentration around the etching holes caused the released microchannels to crack as shown in Fig. 3-6(b). Finally, the fragile silicon nitride capillaries could shatter with the slightest contact with MS inlet during handling.

3.3.2 Other MEMS Overhanging Capillary Technologies

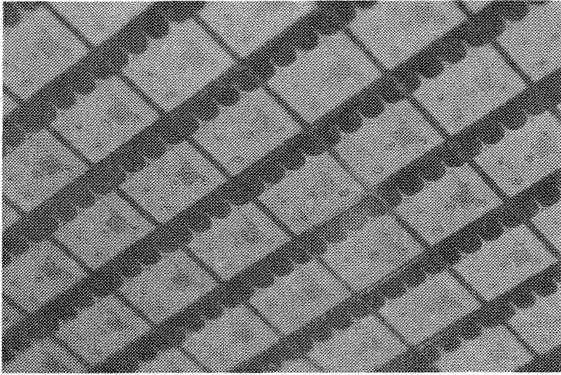
There are other micromachining techniques of constructing microcapillaries, but they suffer similar problems in comparison with this low temperature polymer process. Talbot and Pisano [29] demonstrated a two-wafer polymolding process to make polysilicon microcapillary. It is not easy to integrate these needles with microchannels and other microfluidic components on chip. Papaustky *et al.* [30] reported a low temperature process to fabricate surface micromachined overhanging metallic microchannels. The metallic structure material makes it difficult to perform some of the on-chip separation methods (such as electrophoresis), and to visualize the liquid flow in the channels. In the literature search, no polymer-based electrospray overhanging microcapillary has been reported before.

3.4 Mm-long Parylene Overhanging Capillary Technology

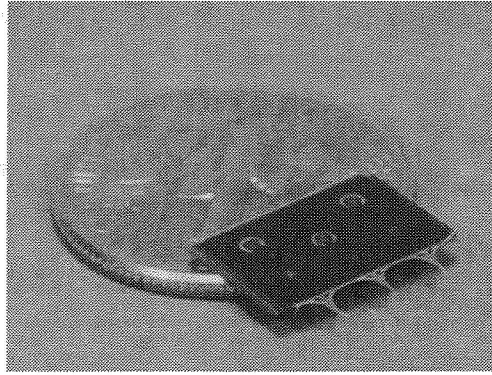
3.4.1 Parylene Overhanging Capillary Chip

The prototype chips used for these studies were fabricated on silicon wafers (Fig. 3-7(a)). Each individual unit was 1 square centimeter (Fig. 3-7(b)) and contained three different sets of ports, chambers, channels, and needles. The ports are square pyramidal holes in the silicon wafer formed by isotropic etching. The remaining structures are formed entirely from two polymer (parylene) layers deposited on the surface of the wafer with a sacrificial layer in

between to create the voids that become channels and chambers. Forming channels by removing a sacrificial layer eliminates the need to use a cover plate and makes it easier to do the fabrication as a single batch process.



(a) ESI chips batch-fabricated on a 4-inch Silicon wafer



(b) A fabricated chip with overhanging Parylene capillary

Figure 3-7 Fabricated Parylene ESI chip

Many of the drawbacks of the Si_xN_y ESI capillary are eliminated with this new overhanging Parylene technology.

The most important advantage is using thin film Parylene is used as the structure layers of the mcirochannels and overhanging capillary. In contrast to the high temperature Si_xN_y process, Parylene is deposited at room temperature. The intrinsic stress in Parylene film is less than 100 MPa.

The second advantage is to use photoresist as the sacrificial material. Photoresist readily dissolves in acetone and can be easily removed from channels a few cm long. Unlike PSG etching, this photoresist sacrificial etching (with acetone) does not require any etch holes along the channel, and thus, structures that are orders of magnitude longer can be easily fabricated.

The next advantage is contributed by the mechanical property of Parylene. The Young's modulus of Parylene (~3 GPa) is only about one hundredth of Si_xN_y. As a result, the

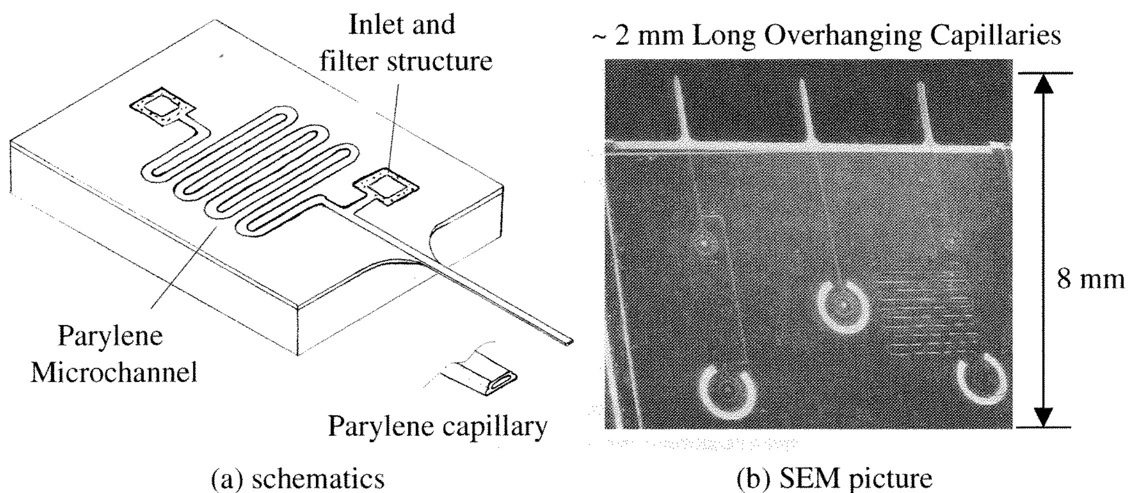
overhanging capillary is straight and much more flexible, therefore robust, compare to the case of Si_xN_y.

At last, Parylene is chemically inert and is compatible with water and a broad range of organic solvents. It is also transparent, which makes it possible to observe fluid flows during testing.

3.4.2 The Chip Structure Design and Fabrication Process

(1) General Chip Structure:

The channels used on these prototype chips were 100 μm wide by 5 μm high. During the fabrication process, the silicon support under the ends of channels extending to the side of the chip was removed to create needle-like structures. A portion of the silicon wafer in front of the needles (guardrail) was left in place during fabrication to protect against mechanical damage. The guardrail was removed prior to use. At the end of the needles, the channel width was reduced to 10 μm resulting in a nozzle with a rectangular opening 5 μm by 10 μm.

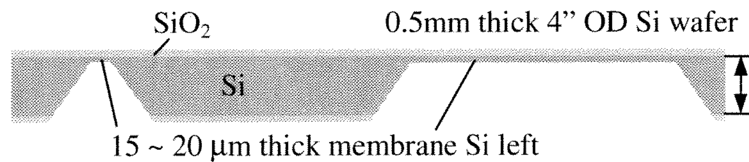


(a) schematics (b) SEM picture

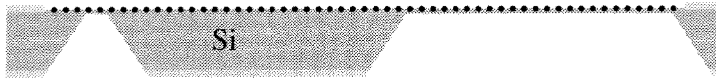
Figure 3-8 ESI Chip with Parylene Capillaries

(2) Major Fabrication Process:

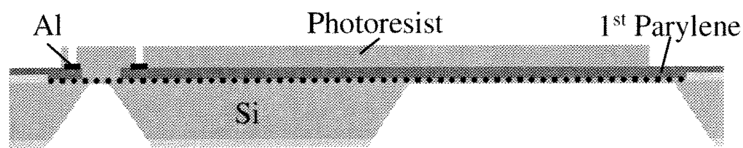
The major fabrication process is shown in Fig. 3-9.



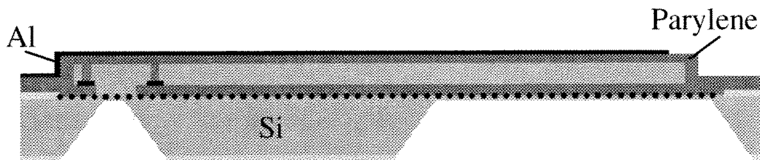
(a) Thermal Oxidation (1.5 μm)
Backside SiO_2 patterning and etching with BHF
Backside KOH etching



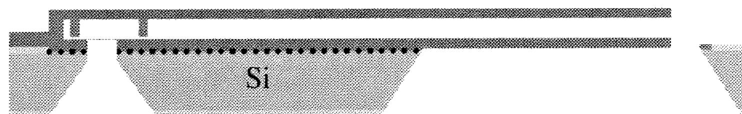
(b) Front side SiO_2 patterning and etching with BHF
BrF_3 front Si surface roughening



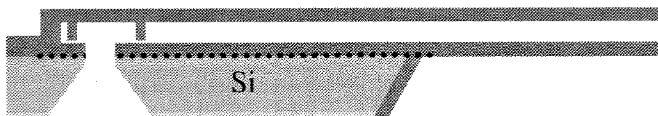
(c) 1st Parylene deposition (1.5 μm)
Parylene patterning with O_2 Plasma
Sacrificial Al (0.1 ~0.2 μm) evaporation and patterning
Photoresist sacrificial layer (~5μm) lithography



(d) 2nd Parylene deposition (1.5μm)
Mask layer (0.1μm Al or 10 μm Photoresist) pattern
Patterning with O_2 plasma



(e) Wafer dicing
BrF_3 backside Si etching to free the needles and open the inlets
Sacrificial layer etching (Al etchant, Acetone)



(f) Chip cleaning with acetone, alcohol, DI water
3rd layer Parylene deposition

Figure 3-9 Major fabrication steps

First, windows are opened on backsides of silicon wafers that coated with 1.5 μm silicon dioxide on both sides. Next, the backside cavities are etched by KOH to leave a 10 μm silicon membrane left using SiO_2 as a mask layer. The SiO_2 layer on wafer top side is patterned and etched by BHF. BrF_3 gas phase etching follows to roughen the silicon surface for adhesion enhancement. Next, a 3 μm thick Parylene-C is deposited on the wafer front side only. After patterning the Parylene with oxygen plasma, a 5000Å thick Al layer is evaporated and patterned to form the filter region. Photoresist layer of 5μm thick is spun and patterned. The wafer is then hard baked at 120°C for 10 minutes to evaporate the solvent in the photoresist. This step is important, otherwise the channel will tend to buckle and burst if heat is applied later on. A 3 μm thick Parylene-C layer is then deposited on the front side only followed by 0.1 μm Al evaporated and patterned as a masking layer. Afterwards, oxygen plasma etching defines the microcapillary tip. Next, the wafer is diced, and the thin silicon membrane is etched away by BrF_3 to open up the backside inlet holes and release the overhanging polymer structure. Finally, the photoresist layer is dissolved away with acetone to open the channels. The chips are then rinsed and immersed in alcohol and deionized water for several hours.

(3) In-channel Micro Filter Structures:

To minimize tip clogging, particle filters (Fig. 3-10) are also incorporated in several other designs by employing a double sacrificial material method. Filter structures can be formed by using sub-micron channel heights in the filter areas, and larger channel heights for the remaining microchannel length. To achieve this type of bi-level sacrificial structure, careful control of both thickness' are essential. Therefore, in the process a sub-micron thick Al layer is use for the filter region and thicker photoresist for the rest of the structure. The

flexibility of polymer must also be taken into account when designing structures that are subject to mechanical pressure. For example, fluidic pressure can cause deformation in the sub-micron filter area and nullify its effectiveness as a sub-micron filter. To address this deformation problem, polymer anchor structures are fabricated in this region to hold the top and bottom of the channel together.

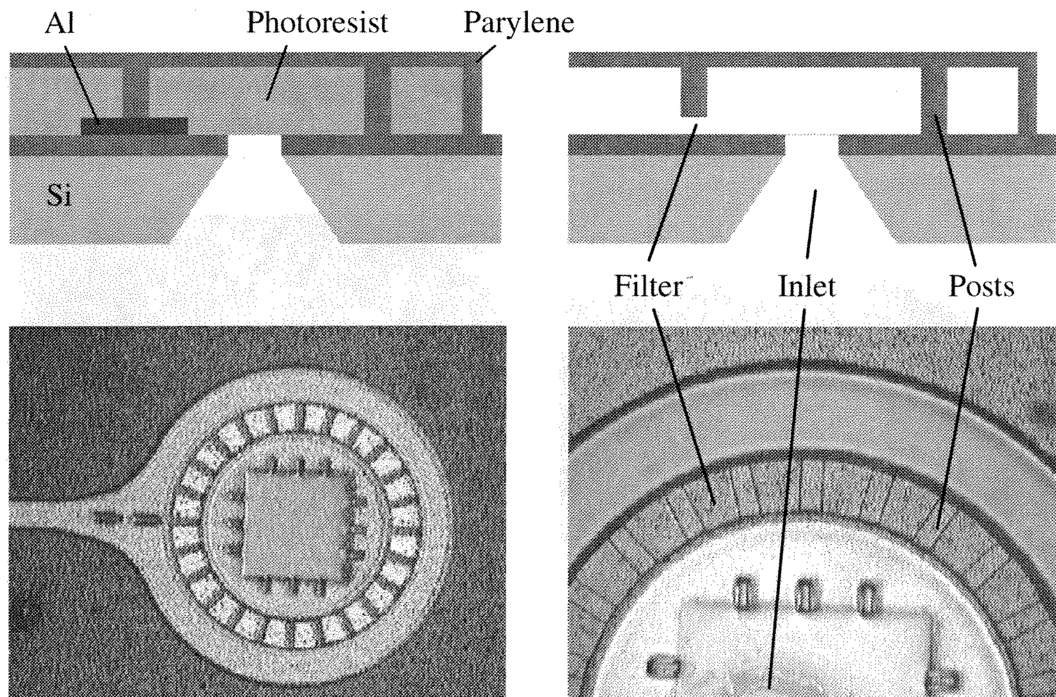


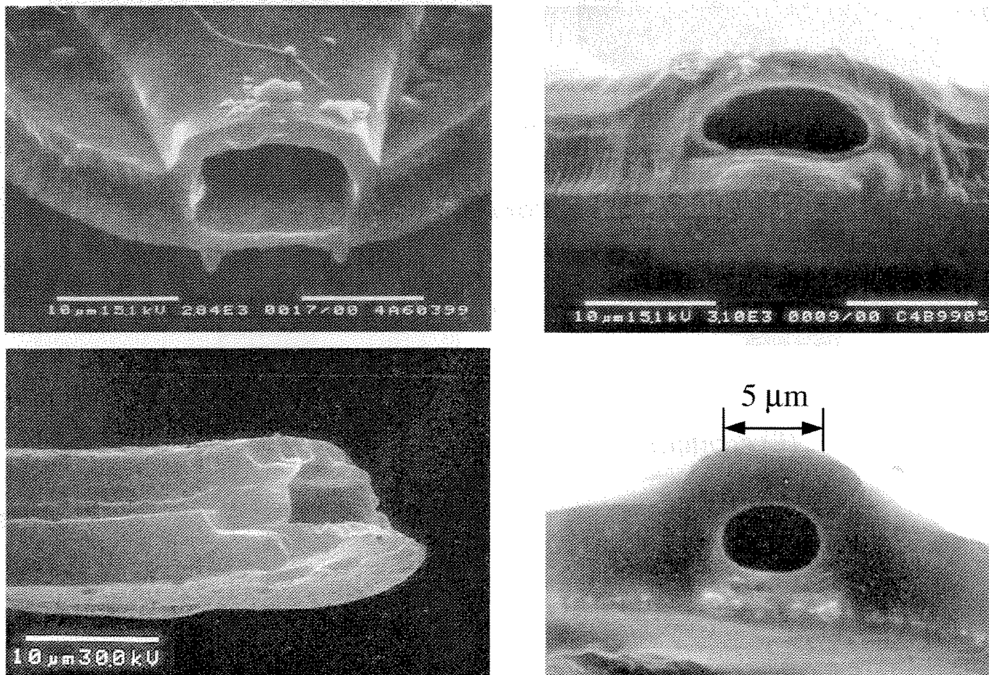
Figure 3-10 Inlet microfilter structures made by composite Al/PR sacrificial layers

Gas phase silicon etchant BrF_3 [Chapter 2] is used to release the microcapillaries. This etching method serves two purposes in this process: (1) to partially roughen the silicon surface for increased adhesion to the Parylene, and (2) to release the microcapillaries from silicon substrate in the last fabrication step. Compared to other silicon etching methods, plasma etching offers much less silicon undercutting and tends to damage the Parylene film on the chip. Even though KOH or TMAH do not attack Parylene at low temperature, they do attack the Parylene-silicon interface significantly and cause Parylene to peel off from the substrate.

In contrast, the gas phase silicon isotropic etchant, BrF_3, can etch silicon spontaneously at room temperature and maintain the integrity of Parylene-silicon interface.

(4) Various Tip Design and Process:

Various tip shapes and geometry can be achieved by using different processing conditions and / or different mask design. If the sacrificial photoresist is only soft baked (90°C, 20 min.) before add on the second Parylene layer, the final tip opening is rectangular (Fig. 3-11(a)). On the other hand, if the photoresist is re-flowed (hard baked 90°C, 20 min.), the final tip opening can be oval or circular (Fig. 3-11(b)) depending on the aspect ratio.



(a) Soft baked photoresist (90°C 20 min) (b) Hard baked photoresist (120°C 20 min)

Figure 3-11 Capillary tip variations (1)

The actual shape of the tip could also be varied depending on the pattern for the mask used to protect the channel during the plasma-etching step. If the cut is made perpendicular to the channel axis, a blunt tip with a roughly rectangular opening is created (Fig.12(a)). Alternatively, if a V-shaped cut is made, then triangular sections of the upper and lower

parylene layers extend beyond the channel orifice (Fig.12(b)). These are referred to as sharp tip emitters.

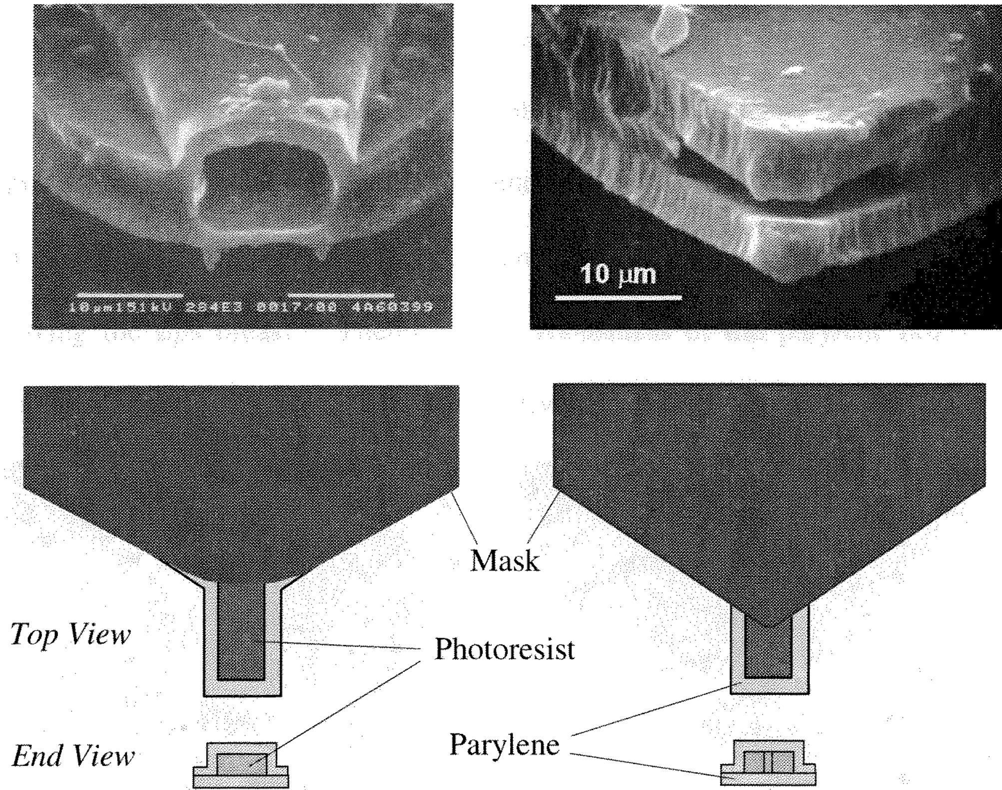


Figure 3-12 Capillary tip variations (2)

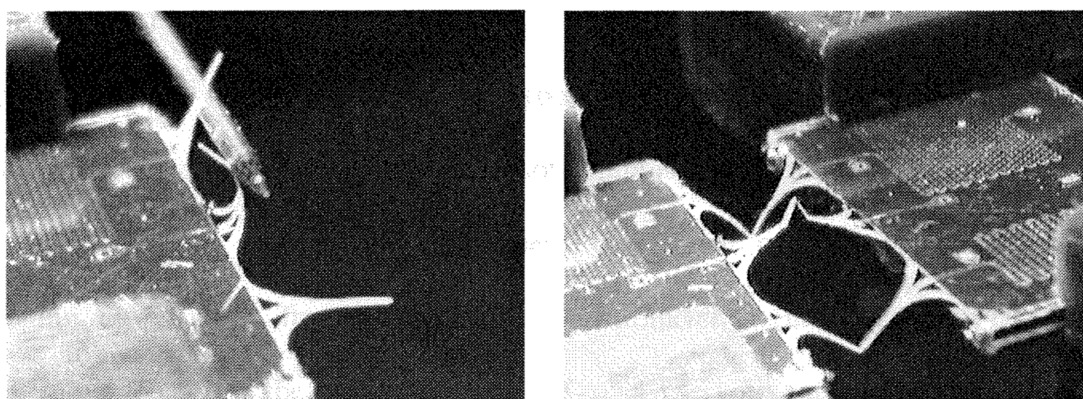
(5) Inlet Considerations:

At the connection with the ports on the chip, the channels expand to form circular chambers approximately 700 μm across. A circular array of posts was placed within each chamber and served to strengthen the roof and provide a filter for any debris entering the chip. A portion of the silicon wafer around the outside perimeter of the chamber was left exposed to provide an anchor point for a layer of epoxy or polyimide that might be needed to further strengthen the roof of the chamber. This was not necessary for any of the experiments described here. Pressures of larger than 15 psi were needed to rupture the 3 μm parylene films.

3.5 Testing

3.5.1 The Robustness Test

In terms of robustness, Si_xN_y capillaries can shatter easily with the slightest contact with other objects, but the Parylene capillaries although 600 times longer, flex and return to their original shape. Fig. 3-13 illustrates the Parylene ESI tips' amazing plasticity. In spite of the long overhanging structure, quite a few chips can even survive table-top falls and mishandling without having the tips break. Therefore, the robustness of the parylene nozzles, and the simple process makes this technology most attractive.



(a) Deflection by Probe Tip (b) Bending on a Mirror Surface

Figure 3-13 Robustness demonstration of the overhanging Parylene capillary

3.5.2 The Testing Jig and Setup

Customized chip holders were used to facilitate handling the chip and to make the necessary sample and electrical connections. To visualize the Taylor cone at Caltech, a plexiglass chip holder that consists of two plates and O-rings were designed and made. The MEMS ESI chip was mounted between the two plexiglass plates to sit against three alignment pins. The whole assembly was held together with three screws. PEEK tubing (150 μm ID,

1.6 mm OD) was then inserted into the access holes of the back plate. The PEEK material had previously been shaped to fit by holding it in liquid N_2 for a few minutes and then pressing it into the access hole. This connection allowed for easy removal and replacement of the tubing and was able to withstand applied pressures larger than 20 psi. This method eliminated the tedious backside gluing required to connect the MEMS ESI chips to the "macro" world.

To do the ESI-MS testing at Beckman Research Institute of City of Hope, Dr. Larry Licklider designed a customized chip holder that consisted of two chlorotrifluoroethylene polymer (Kel-F) plates (2.16 cm x 2.16 cm x 0.31 cm) and an elastomer (polydimethysiloxane, PDMS) gasket (Fig. 3-14). For convenience, the chip holder was assembled upside down. The plate in contact with the top of the chip (bottom plate in Fig. 3-14) was cut out so that it contacted only the edges of the chip and did not compress any of the parylene structures. This also facilitated using a microscope to observe movement of fluid in the channels and positioning the chip in front of the mass spectrometer. Holes in the PDMS gasket corresponding to ports in the bottom the chip served as reservoirs for loading sample solutions. To make the gasket, Sylgard 184 (Dow Corning, Midland, MI) was prepared according to manufacturers instructions and polymerized on a flat surface to a thickness of 1.4 mm. The reservoir was formed using a piece of 1.6 mm o.d. PEEK tubing. The tubing was positioned on top of one end of a 40 μm diameter Ni/Cr wire. Removing the tubing after the elastomer hardened, left a portion of the wire within the reservoir opening. The elastomer was cut to the dimensions of the chip and positioned so that the reservoirs aligned with the ports in the chip. The second Kel-F plate containing access holes (made with a 0.055 inch drill bit) was positioned over the gasket. The whole assembly was held together with three screws.

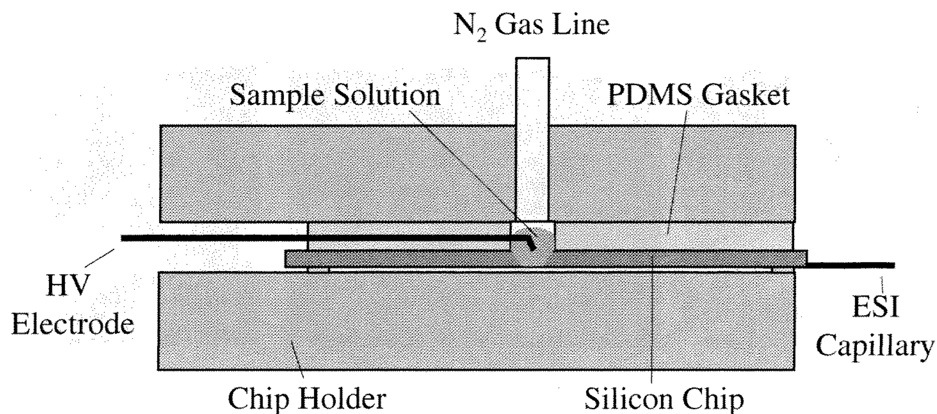


Figure 3-14 Chip holder for sample loading and ESI [28]

3.5.3 The Taylor Cone Visualization

With a high magnification lens, the Taylor cone formation at the orifice of the polymer micro-capillaries was video-taped [27]. The test solution consisted of 1% acetic acid (by volume) added to 1:1 MeOH:Water. The sequence of snapshots below clearly indicates how size of the Taylor cone is governed by the tip orifice geometry and the formation of the cone is governed by electrical potential. In fact, the cone size and shape is also related to flow rate and the distance between the tip and MS inlet. It is also important to note, that the view of the ESI is taken from a top view through a microscope, and that the "cone" most likely is not circular but flattened in the vertical dimension because the tip orifice is rectangular. In Fig. 3-15(a) and Fig. 3-15(b), although the electric field is applied the meniscus forces are strong enough to create the curvature. Subsequently, as the potential increases to 1250 V, the generation of a sharp and stable cone is visible (Fig. 3-15(c)). The distance from the tip to the inlet was roughly 500 μm. No plume is visible from the point of the cone, because droplet size is likely to be below 100 nm [5].

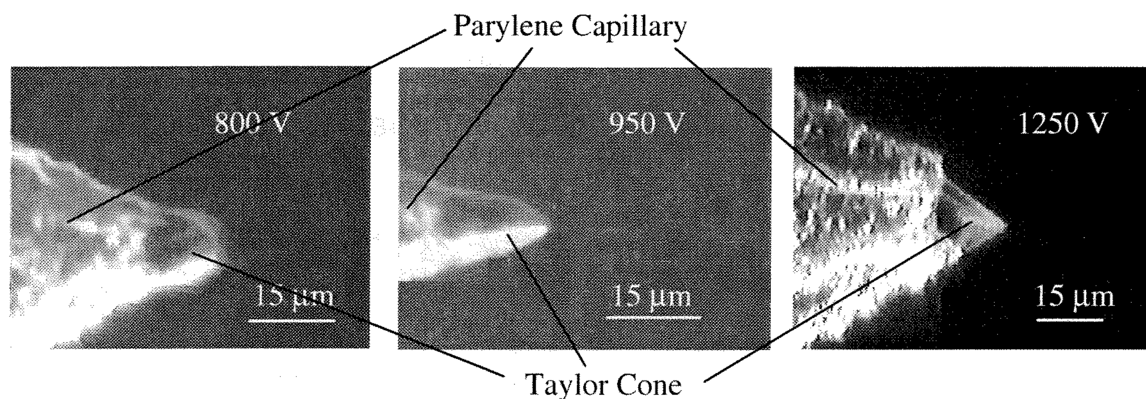


Figure 3-15 Video snapshots of formation of Taylor cones at the tip overhanging Parylene capillary as voltage increased [26, 27]

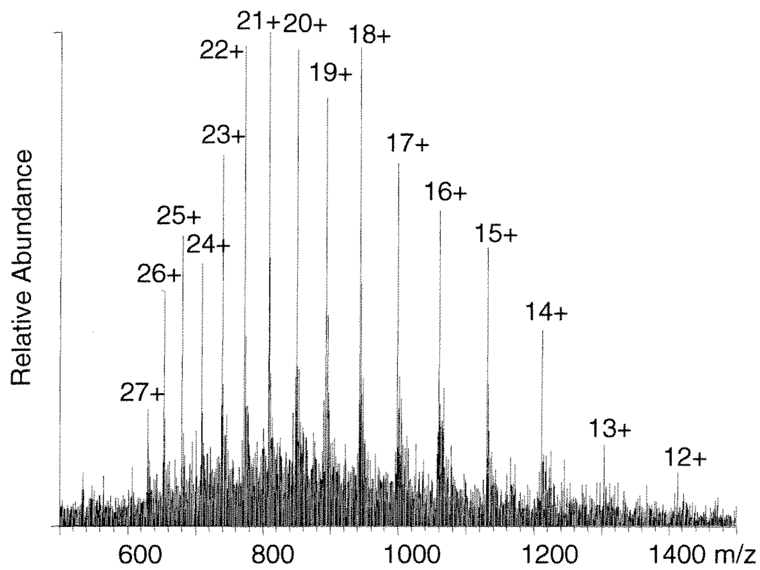
Solution: 1% Acetic Acid, 49.5% Methanol, 49.5% Water

Distance: 500 μm from electrode

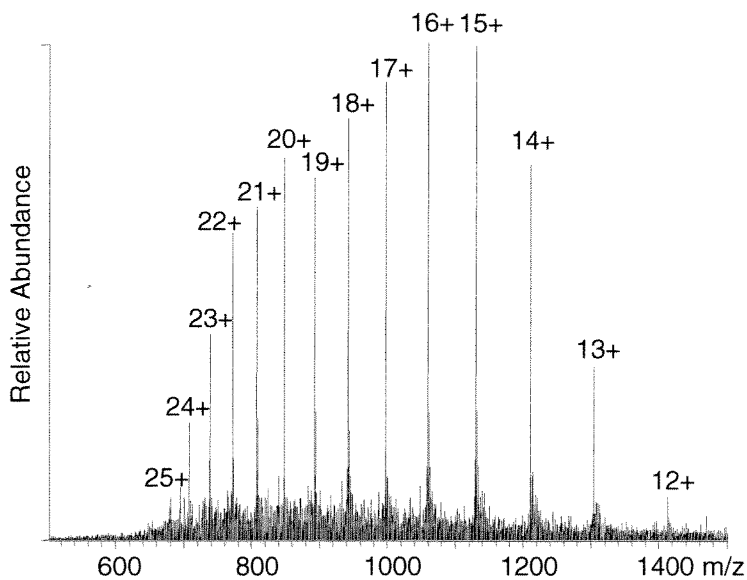
3.5.4 Testing Results

Using the fabricated chip, the ESI-MS testing was successfully done by Dr. Larry Licklider and Dr. Terry D. Lee at Division of Immunology, Beckman Research Institute of the City of Hope.

Samples (2-5 μL) were loaded by inserting a micro-pipette tip or syringe needle through the access hole into the elastomer reservoir. PEEK tubing was then inserted into the access hole after taking out from liquid N_2. Ar gas was supplied via the tubing and a 0 – 15 psi regulator. A standardized 200 nM Myoglobin solution was continually infused with a reservoir pressure of 2 psi and 1.6 kV potential. Fig. 3-16 shows the similarity of a mass spectrum analysis of myoglobin using the Parylene micro capillary vs. conventional silica capillary. Both MS scans were performed using 15 attomoles of sample.



(a) ES-MS Spectrum of Myoglobin
15 amole consumed, pulled Fused silica needle



(b) ES-MS Spectrum of Myoglobin
15 amole consumed, micromachined Parylene needle

Figure 3-16 MS scans of Myoglobin

using conventional fulsed silica needle and on-chip Parylene needle. [27]

3.5.5 Discussion

The ability to fabricate precise micrometer-sized tip geometry introduces further opportunities to examine micro-electrospray phenomena. Although a lot of experimental data and understanding have been acquired by various groups such as Fenn [6] and Wilm [9] regarding electrospray, mathematical models exist for only special cases.

$$re = \left(\frac{\rho}{4\pi^2 \gamma \left[\left(\frac{Ua}{Ut} \right)^2 - 1 \right] tan(\frac{\pi}{2} - \upsilon)} \right)^{1/3} \cdot \left(dV/_{dt} \right)^{2/3}$$

For instance, the previous mathematical model developed by Wilm and Mann [9] models a circular cone with a specific cone tip angle, where r_e represents the radius of the emission region at the tip of the Taylor cone, γ the surface tension of the liquid, ρ the density of the liquid, U_a the applied voltage, U_t the voltage at which the cone is formed, ν the cone angle, and dV/dt the flow rate. The equation below predicts that $r_{e,}$ the emission radius can be reduced with a reduction in flow rate. For the microcapillary, the orifice is rectangular and initial measurements of the cone angle show significant deviation from that of a circular capillary Taylor cone (~49°). Experiments are in progress to determine the extent to which ESI-MS performance is affected by the shape of the ES nozzle.

3.6 Summary

This work demonstrates the feasibility of creating chip-based micro-scale electrospray sources using MEMS technology. It represents vital and significant improvements in MEMS process technology and MS functionality with respect to the silicon-nitride ESI nozzles reported before. Many of the drawbacks of the previous generations of Si_xN_y ESI tips were eliminated with the overhanging polymer technology, and has made this MEMS device more robust and practical than ever before. It is validated here, the tremendous advantages and viability of Parylene polymer technology combined with gas phase etching for mm-long rugged freestanding structures. In addition, fluid visualization of the Taylor cone formation from the tips unearths new issues in the study of electrospray phenomena. As an example of MEMS technology for chemical analysis systems, the work presented here has made the MEMS electrospray chip more practical.

3.7 References

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Chapter 4

A Single Chip Parylene Micro Check Valve

4.1 Introduction

4.1.1 Fluid Rectification

Analogous to a diode used to rectify current flow in an electric circuit, a check valve is a passive device to rectify liquid or gas flows in a fluidic system. It is opened by a forward fluid flow and closed by a reverse one. Micro check valves are widely used in micro fluidic systems, such as micro reciprocating pumps, to direct flows.

It is important to note that a check valve can only work in a specified flow rate range. In this chapter, a novel micro check valve that works for both gases and liquids is present.

4.1.2 Recent MEMS Check Valves

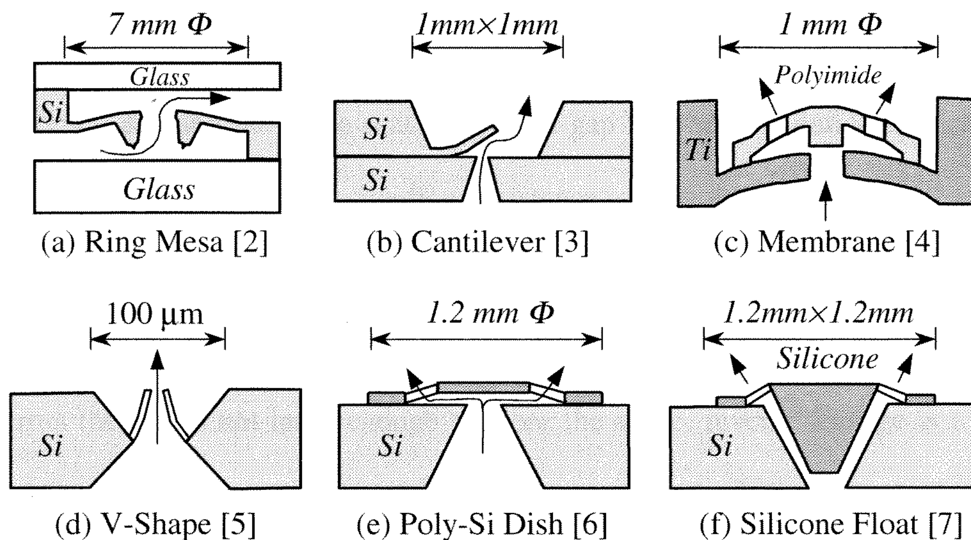


Figure 4-1 Schematics of the reported micro check valves in forward flow position

Recent developments in micro check valves are reviewed by S. Shoji [1]. Some of the reported micro check valves are shown in Fig. 4-1

Structures such as ring mesas, cantilevers, float, gates, and membranes fabricated from silicon, silicone, polyimide and metal, have been used to form the deflectable sealing elements (caps) of check valves [2-7]. The valve seats and orifices were often made of KOH-etched trapezoidal structures on a silicon substrate.

4.1.3 Technical Challenges

Some of the check valves (Fig. 4-1) used more than two bonded chips. They are not batch-fabricated and require considerable packaging. Moreover, multi-chip bonding creates a large fluid dead volume within the check valve package. It is desirable from the fabrication point of view to have the whole check valve contained in a single chip.

There are also several general performance issues associated with micro check valves. Most developed check valves appear to have deteriorated performance with decreasing pressure and flow rate. For example, small forward pressures make it difficult to facilitate large cap (the deflectable element) deflection, while small reverse pressure can not eliminate the fine gap between the rigid cap and the valve seat. The small gap between the deflected membrane cap and valve seat often causes an excessive flow resistance and leads to large pressure losses in the forward flow direction. Thus, minimizing the flow resistance caused by the sealing cap is important for a successful check valve design. On the other hand, if the reverse pressure applied across the cap is not large enough to close the valve, reverse leakage is a significant problem. Moreover, the small sizes of micro valves imply that stiction and surface tension effects between the valve seat and membrane cap often need to be carefully addressed. Here, the cracking pressure, the minimum pressure to open the check valve for forward fluid flow, is commonly used to gauge stiction effects. A good micro check valve, therefore, should have low

cracking pressure, low cap-induced flow resistance, small reverse leakage and large operational reverse pressure. These parameters can qualitatively defined (Fig. 4-2) in the same way as characterization of a diode in an electric circuit.

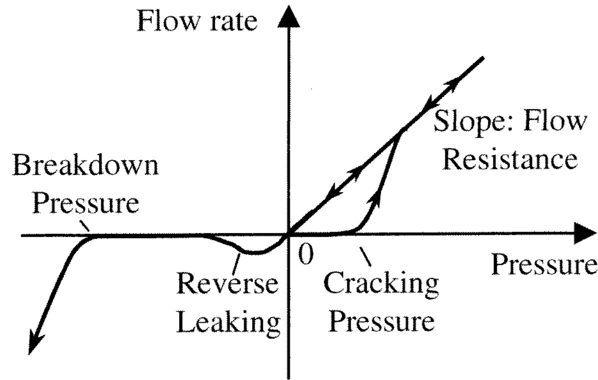


Figure 4-2 Schematic description of the characteristics of a check valve

4.2 Design

The single chip micro check valve consists of a bulk-micromachined orifice, a valve seat with roughened surface, and a Parylene sealing cap anchored to the valve seat. A pressure differential across the sealing cap either causes the cap to lift up, allowing fluid to flow though orifice or pushes it down, sealing the cap to the valve seat (closed), as shown in Fig. 4-3.

Parylene has been selected for its elasticity, which provides large open gap in the forward direction and good sealing in the closed position. A special structure designed is made to maximize the forward cap deflection in order to minimize flow resistance caused by the cap. In the check valve, the Parylene sealing cap is tethered by four S-shape Parylene beams. This is advantageous, as the sealing cap is self-aligned with respect to the orifice as the arms are symmetrical. Under forward flow, the cap and tethers will rotate and twist up. With this design, the vertical displacement of the cap is determined by the length and shape of the tethers. Since Parylene has a very low Young's modulus (~2.8 GPa) and the thickness of the S-shaped beams

is on the order of microns, the twist-up tethers exert a very small resistance to the upwards movement of the membrane. Therefore, they produce negligible resistance in response to forward fluid flow.

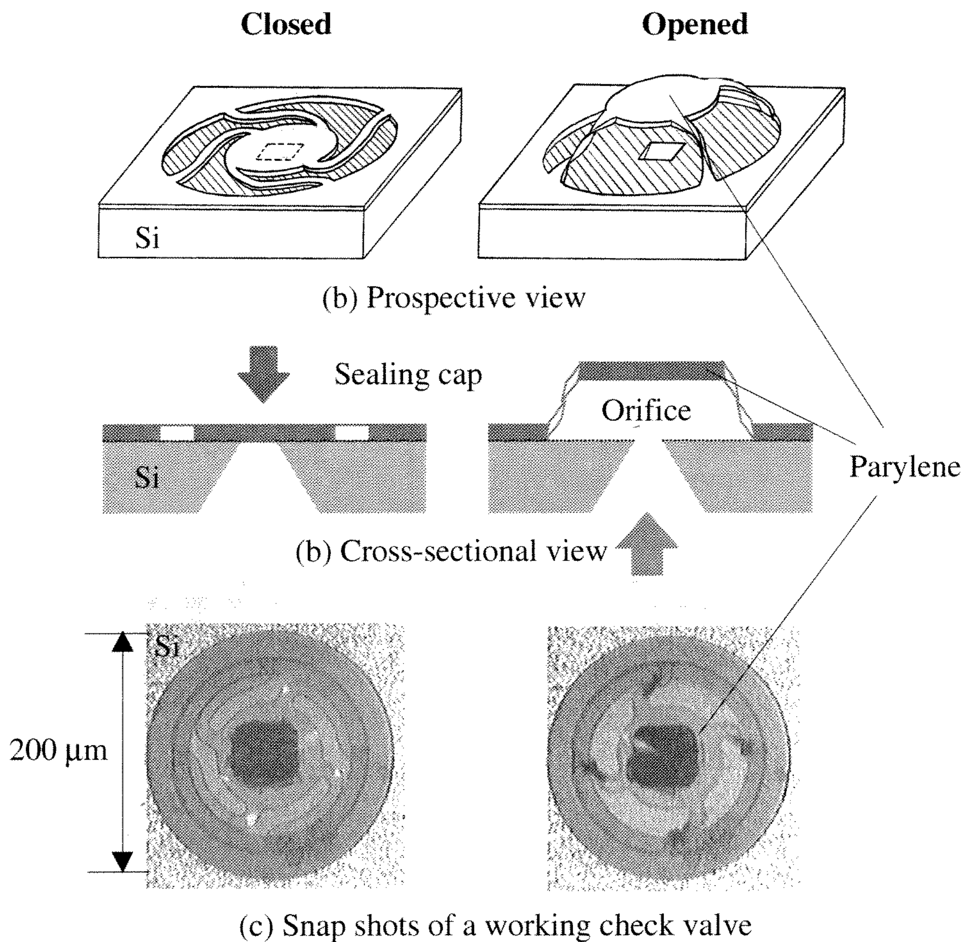


Figure 4-3 Schematics and photos of a single chip Parylene micro check valve

4.3 Fabrication

The fabrication process is shown in Fig. 4-4. First, a 1.5-μm thick silicon dioxide layer is thermally grown on the wafers at 1050°C. The silicon dioxide layer on the back side of the wafer is patterned and etched by buffered hydrofluoric acid (BHF) to expose silicon while the front side of the wafer is protected by photoresist.

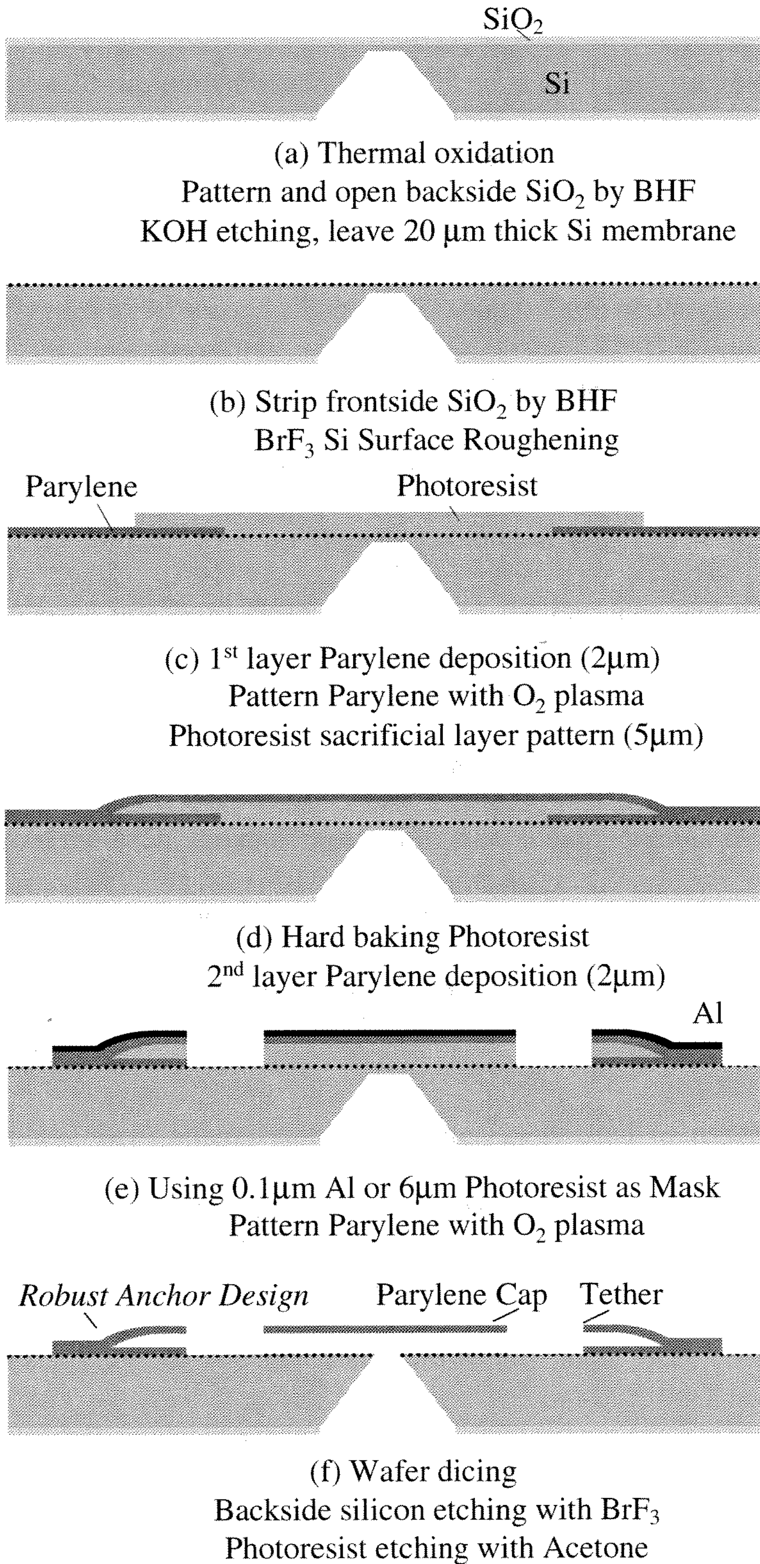


Figure 4-4 Major fabrication steps

After removal of the photoresist, the wafers are immersed into KOH to etch the silicon substrate until about a 20-μm thick membrane of silicon is left. The silicon dioxide is removed from the front side by BHF, followed by a 3-minute BrF_3 gas phase etching to roughen the silicon surface. The wafers are then immersed in the 0.5% A-174 adhesion promoter for 20 minutes followed by a 15 to 30 second alcohol rinse. Next, 2 μm of Parylene-C is deposited on only the front side of the wafer. After patterning the Parylene with oxygen plasma, a 5-μm thick photoresist (AZ4400) layer is spun and patterned on the front side. The wafers are then baked at 120°C for 20 minutes to form smooth photoresist edges. The front of the wafer is etched in oxygen plasma briefly to clean and roughen the Parylene and photoresist surfaces. Another Parylene layer with a thickness of more than 2μm is deposited followed by a 0.1 μm Al evaporation. The Al layer is patterned and used as a mask to etch the Parylene layer with oxygen plasma. From the back, the underneath thin silicon diaphragm is etched away by BrF_3 to expose the photoresist sacrificial layer. Following wafer dicing, the micro check valve diaphragm is released after photoresist etching in acetone at room temperature, followed by alcohol and DI water rinse.

Here, gas phase BrF_3 silicon etching [chapter 2] is used to roughen the valve seat surface. This reduces stiction and surface tension in the valve by minimizing effective contact area between the mating surfaces. The roughened valve seat surface also leads to enhancement of the adhesion of the Parylene anchors. Exposure to gas phase BrF_3 under 1 Torr at room temperature generates ± 0.2 μm of roughness on a polished silicon surface as shown in Fig. 4-5.

For forward flow, the robustness of the tether anchors determines the maximum pressure the check valve can withstand.

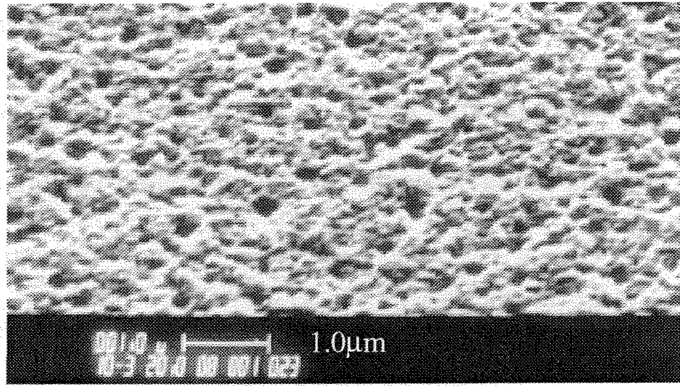


Figure 4-5 Silicon surface after BrF_3 roughening

The anchors have therefore been improved by three means: First, the substrate surface is roughened to enhance Parylene adhesion. Next, an initial layer of Parylene is deposited and patterned after applying the A-174 adhesion promoter to the substrate surface. This step is necessary since the A-174 adhesion promoter dissolves the photoresist sacrificial layer if used afterwards. Finally, the patterned photoresist sacrificial layer is reflowed by hard baking to form smooth edges as shown in Fig. 4-6.

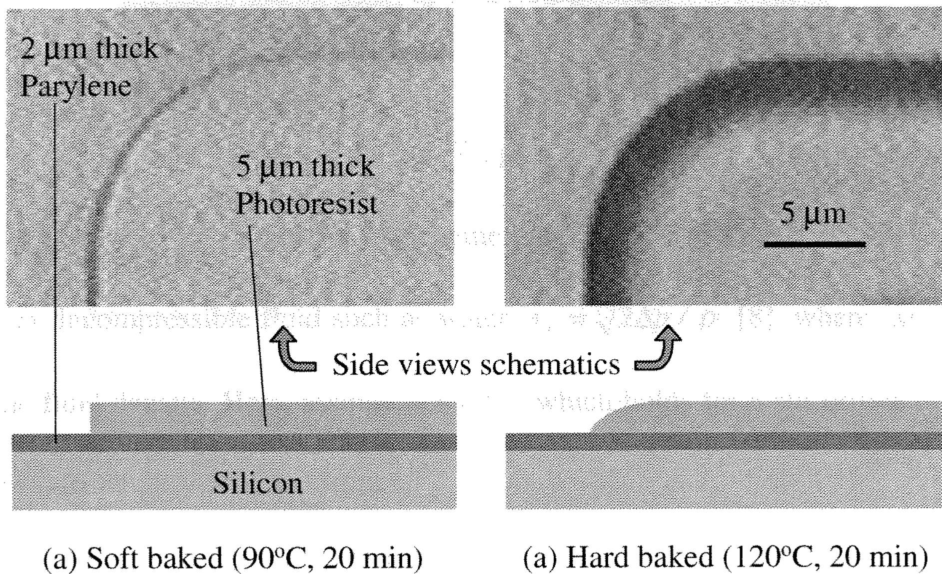


Figure 4-6 Photoresist (5μm AZ4400) edges before and after hard bake

4.4 Analysis of Orifice Flows

This section analyzes of liquid and gas flows through the micro valve. Such analysis is important for a fundamental understanding of valve operation, and can be a valuable tool for optimizing valve designs.

First consider the flow across the orifice in the absence of the membrane cap, as illustrated in Fig. 4-7. Due to a pressure difference, a jet discharges from a reservoir (with pressure p_0) through an orifice (with area A) into the atmosphere (with pressure p_{atm}). Upon exiting the orifice the jet first contracts to a minimum region (called the vena contracta), achieving a velocity v_e. The jet then expands downstream. The area vena contracta is $A_e = \phi A$, where $\phi < 1$ is a contraction coefficient and A is the area of the orifice.

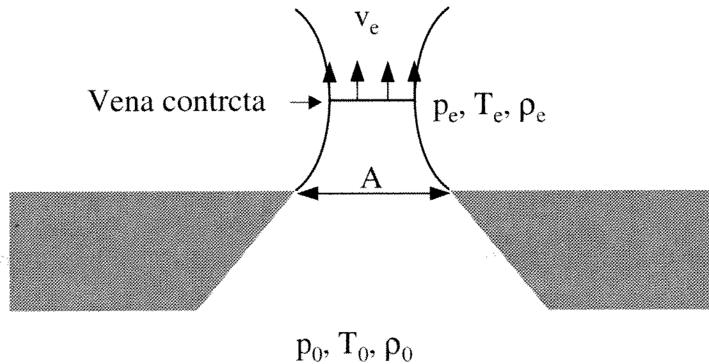


Figure 4-7 A jet emerging from an orifice

For an incompressible fluid such as water, $v_e = \sqrt{2\Delta p / \rho}$ [8], where $\Delta p = p_0 - p_{atm}$ and ρ is the fluid density. Here, assume $\phi = 0.61$, which holds for a slit orifice [9]. Then, the volume flow rate can be calculated from

$$Q = v_e A_e . \tag{4.1}$$

For a compressible fluid, the assumption of an isentropic flow leads to [9],

$$v_e = \sqrt{[2\gamma R/(\gamma-1)][1-(p_e/p_0)^{(\gamma-1)/\gamma}]T_0} \tag{4.2}$$

where T_0 is the absolute temperature in the reservoir, p_e is the fluid pressure at the vena contracta, R is the gas constant, and γ is the ratio of the constant-pressure to constant-volume specific heats of the gas. The fluid density at the vena contracta is

$$\rho_e = \rho_0(p_e/p_0)^{1/\gamma} \tag{4.3}$$

where $\rho_0 = p_0/RT_0$ is the gas density in the reservoir. To estimate the contraction coefficient, the following formula [8] can be used,

$$\phi = \frac{\pi}{\pi + 2(p_e/p_0)^{1/\gamma}}. \tag{4.4}$$

Although this expression only holds for a slit orifice, Brower [8] has indicated that it yields a reasonable estimation in the case of a circular orifice. Finally, the mass flow rate is given by

$$\dot{m} = \rho_e v_e A_e \tag{4.5}$$

The value of p_e is next to be determined. It can be shown [9] that $p_e = p_{atm}$ when $p_{atm}/p_{0>} > \lambda^* = (2/(\gamma+1))^{\gamma/(\gamma-1)}$, and $p_e = \lambda^* p_0$ when $p_{atm}/p_{0>} \leq \lambda^*$. The phenomenon in the latter case is called choking, where the jet velocity reaches the speed of sound (i.e., the Mach number equals unity), and the mass flow rate becomes linear with the absolute reservoir pressure.

In the presence of a membrane cap, the above analysis ceases to hold, unless the displacement of the cap from the orifice is sufficiently large. In this case the ambient pressure will still equal the atmospheric pressure, and the bare-orifice analysis may be used. Testing shows that the tethered membrane cap introduces negligible flow resistance, and the preceding

equations can be used to fit the experimental data. This will be demonstrated in the next section.

4.5 Testing

This section presents results from testing of the check valve. The testing setup is first described. And then the testing results on some important valve characteristics are presented.

4.5.1 Testing setup

A special acrylic jig is made for the testing setup as shown in Fig. 4-8. The check valve chip can be easily clamped between two O-rings to prevent leakage from the package. Using this setup under the microscope, the check valve operation is readily monitored.

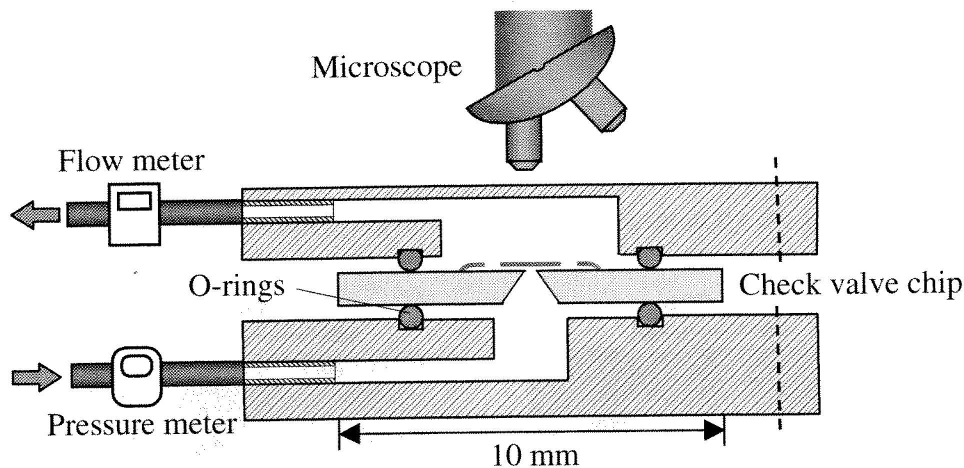


Figure 4-8 Check valve testing setup

4.5.2 Forward Cracking Pressure

The cracking pressure of the valve is discussed first. Theoretically, the cracking pressure (Fig. 4-2) is a threshold value such that any applied pressure difference that is greater than this value will generate a flow rate. In practice, measured cracking pressures generally differ because of variations in measurement instrument sensitivities. For the micro check valve,

a nitrogen flow is detected at a pressure reading of 0.5 kPa, which is also the sensitivity of the pressure measurement. It follows that the cracking pressure is less than 0.5 kPa for gases. However, if wetted prior to the testing, the valve has a cracking pressure of 1 kPa (±0.5 kPa). In comparison, the tests with a smooth valve seat indicate a cracking pressure higher than 620 kPa. It can be concluded that the roughened top surface of the valve seat drastically reduces stiction and surface tension effects, and consequently to reduces the cracking pressure.

4.5.3 Forward Flow Resistance

The measured membrane cap deflections and its implications on membrane-induced flow resistance are discussed next. The membrane cap in Fig. 4-9(a) is anchored by four twist-up arms, while the one in Fig. 4-9(b) is anchored by tree straight arms. The load deflection data of the two types is shown in Fig. 4-10. It can be seen that deflection of the twist-up membrane is roughly four times as large as that of the straight-arm anchored membrane. Thus the twist-up tether design is advantageous since large membrane deflections generally allows a larger flow rate for a given pressure difference. This is further demonstrated by the following testing data.

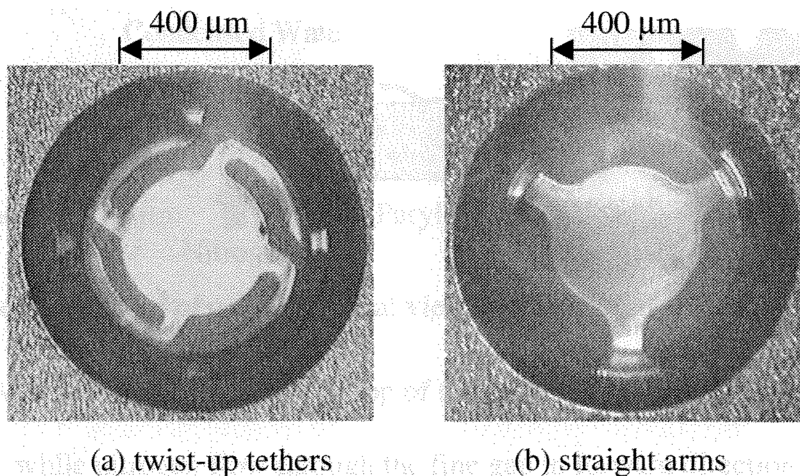


Figure 4-9 Two types of Parylene arm design

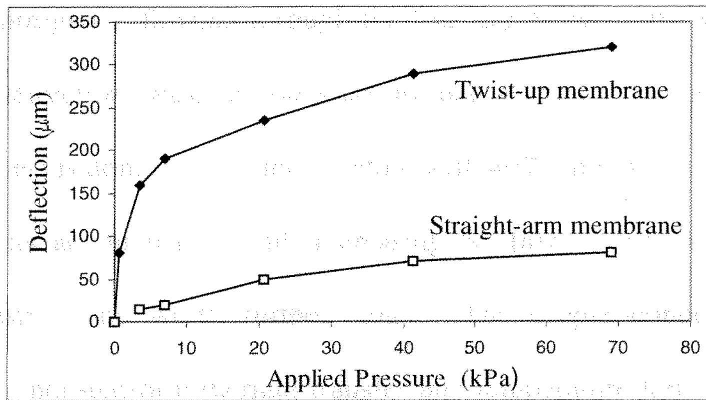


Figure 4-10 Membrane deflection tests

An interesting phenomenon was observed during testing the check valve that has four straight arms, as shown in Fig. 4-11.

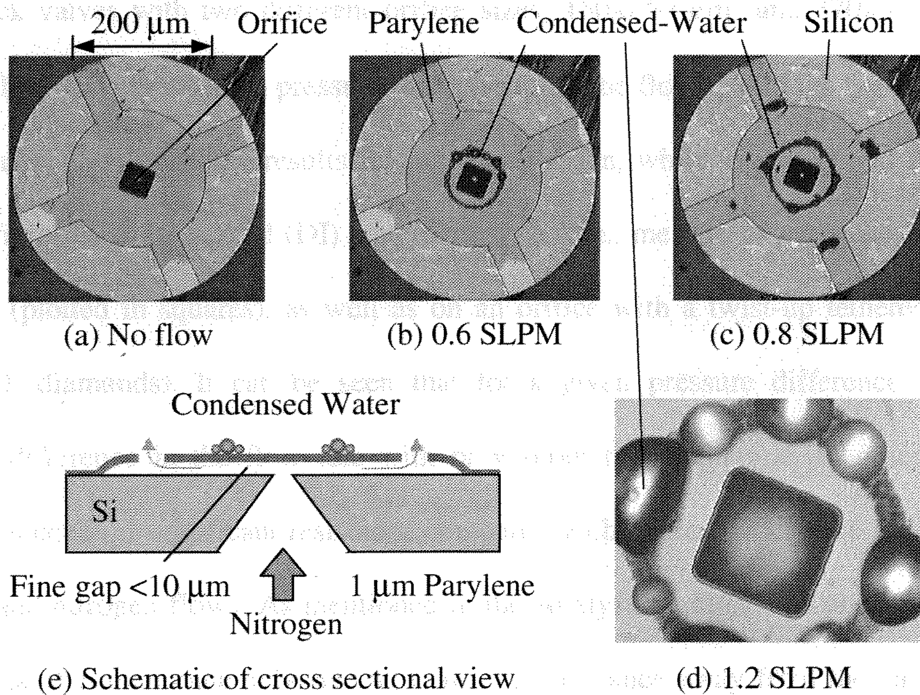


Figure 4-11 Water condensation on top of the Parylene sealing cap with straight-arm while nitrogen flow through the fine gap in forward direction.

(SLPM: standard liter per minute)

When dry nitrogen is flowing through the fine gap between the sealing cap and valve seat in the forward direction, water droplets are formed at top of the Parylene sealing cap by condensation. The test is done at room temperature with 40% humidity. The amount and sizes of the water droplets are increased with increasing N_2 flow. The locations of the water droplets are interesting and worth further study. The droplet-condensation at particular locations indicates a non-uniform thermal transfer and temperature field distribution from the N_2 flow to the sealing cap and valve seat. On the other hand, it is in evidence that with a straight-arm design, the fine gap between the cap and valve seat affects the fluidic flow much more significantly than the twist-up design.

Check valves with two different orifice sizes, 150×150 μm^2 and 370×370 μm^2, have been tested by applying a fluidic pressure and measuring the flow rate in the forward direction. Fig. 4-12 and Fig. 4-13 are the results from using nitrogen, while Fig. 4-14 and Fig. 4-15 are the results from using Deionized (DI) water. In those tests, measurements are performed on a bare orifice (plotted in squares), as well as on an orifice with a twist-up tethered membrane (plotted with diamonds). It can be seen that for a given pressure difference, there is no appreciable difference in the flow rate with or without the membrane. In other words, the membrane induced no significant resistance compared with that caused by the orifice itself for both water and nitrogen flows. As mentioned in the Analysis section, this phenomenon is due to the fact that the membrane deflected to a sufficient distance away from the valve seat such that the pressure at the orifice exit remained close to atmospheric. In comparison, for the valve that employed a straight-arm tethered membrane (see Fig. 9(b)), the flow rate in the presence of the membrane (as shown with triangles in Fig. 4-12), is considerably smaller than the bare orifice data. It follows that the relatively large stiffness of the straight-arm tethers resulted in

significant flow resistance by the membrane. In conclusion, the check valve with a twist-up membrane can be modeled similar to the bare orifice in analytical analysis.

The fluid flow models presented in the Analysis section are examined here with respect to the experimental data. In Fig. 4-12, 13, 14, 15, the solid curves present the theoretical predictions of flow characteristics. Compared with experimental results, it can be seen that the models correctly predict the trend of flow characteristics. Quantitatively, the models give a flow rate that is smaller than actually measured (off by 20-30%). The reason for this deviation is not clear, and calls for further research.

Despite the inaccuracy, the current analysis does provide important insight into the characteristics of the valves. It is also interesting to see that, by scaling up the models by a factor of 1.2 to 1.3, the theory can match the experimental data very well, as shown in those figures using dashed curves.

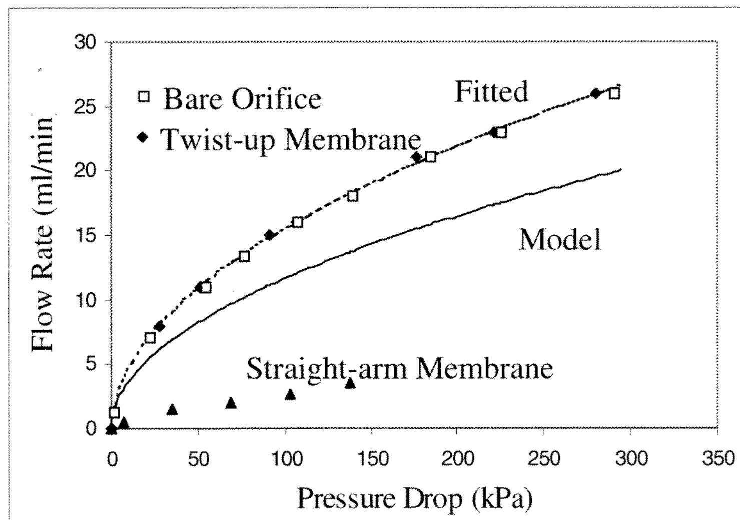


Figure 4-12 Water flow rate vs. pressure drop across a 150 150 μm^2 orifice valve

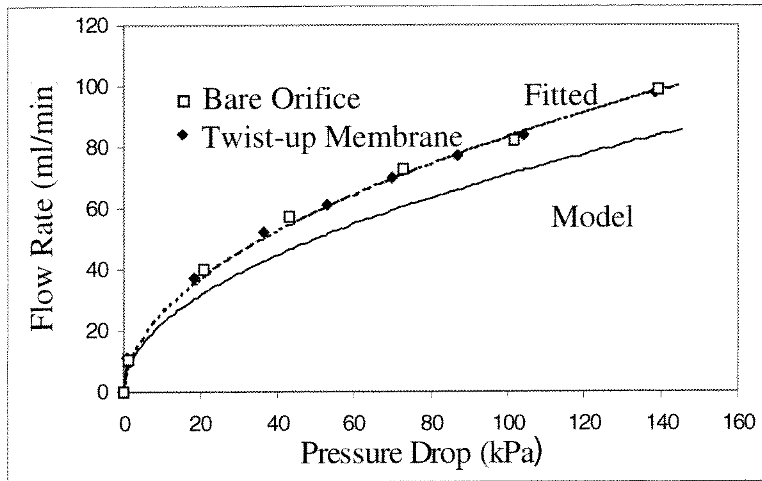


Figure 4-13 Water flow rate vs. pressure drop across a 370 370 μm² orifice valve

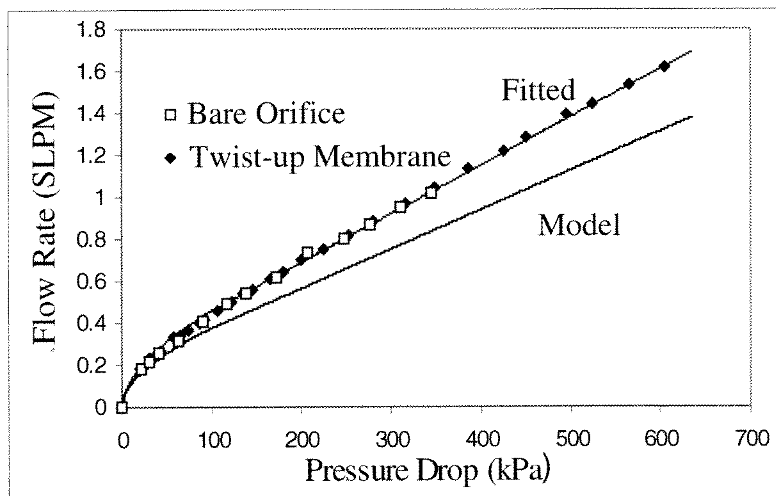


Figure 4-14 Nitrogen flow rate vs. pressure drop across a 150 150 μm² orifice valve

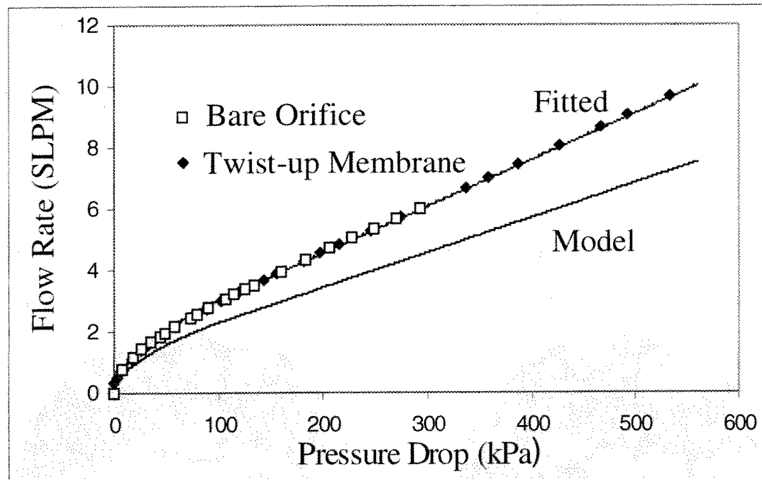


Figure 4-15 Nitrogen flow rate vs. pressure drop across a 370 370 μm² orifice valve

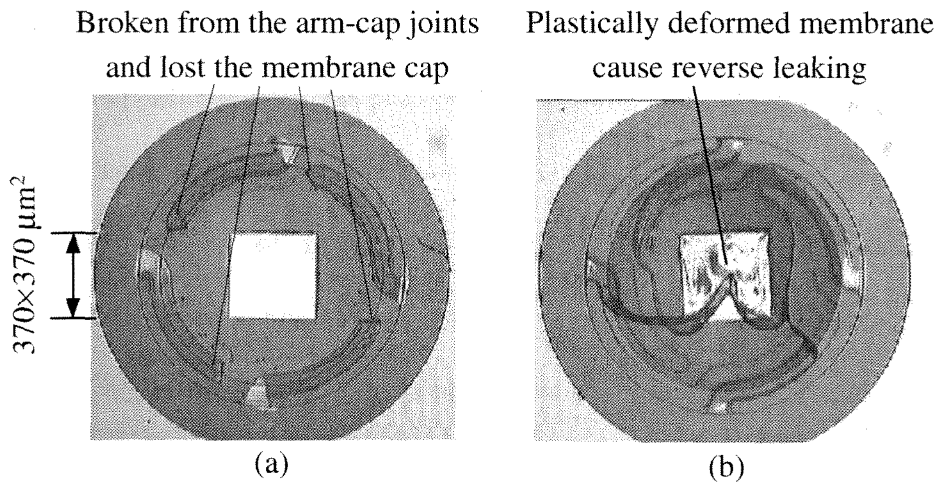
4.5.4 Reverse pressure and leakage

For orifice sizes up to 370×370 μm² and a membrane thickness of 8 μm, the valve can withstand 600 kPa of reverse pressure without structural damage. Meanwhile, the valve has very low leakage under the reverse flow condition. For valve orifice sizes in the range of 60×60 μm² to 980×980 μm², no leakage of nitrogen can be detected, using a flow meter with a resolution of 0.2 ml/min, under reverse pressure up to 100 kPa.

4.5.5 Failure Modes

The check valves are robust in the flow and pressure range specified by the valve design. Here the failure modes are studied to further optimize the valve design. Check valve failures occur when an abrupt burst pressure of 400kPa is applied in the forward direction or an excessive pressure greater than 600kPa is applied in the reverse direction. As shown in Fig. 4-16(a), in the forward flow direction, the check valve failed by the tearing off of the sealing cap

at arm-cap joints. In the reverse direction (Fig. 4-16(b), the 1mm thick Parylene sealing cap yielded and caused leakage by plastic deformation.



Failed Parylene micro check valve due to excessive
(a) abrupt forward pressure ~400kPa, (b) reverse pressure > 600 kPa

Figure 4-16 Failure modes of a check valve

4.6 Summary

This chapter has reported a single chip Parylene micro check valve that exhibits excellent performance compared to check valves in the literature. The valve consists of a micromachined silicon valve seat with a roughened top surface, to which a membrane cap is anchored by twist-up tethers. BrF_3 gas phase silicon etching and Parylene deposition have been combined to enable a low temperature fabrication process.

Analytical modeling of liquid and gas flows through a micro orifice has been performed, and testing data has shown that the models correctly predict the qualitative characteristics of the valve. Testing results also show that the check valve has a low cracking pressure (less than 0.5 kPa for nitrogen), high reverse pressure (greater than 600 kPa) and low reverse leakage (undetectable with a 0.2 ml/min flow meter resolution), and negligible membrane-induced flow resistance.

In term of application, a reciprocating micro pump was successfully demonstrated using the developed micro check valve by Ellis Meng *et al.* [10]

4.7 References

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Chapter 5

A Normally Closed In-Channel Micro Check Valve

5.1 Introduction

As described in last chapter, a micro check valve is a passive device used to rectifying fluidic flows. It is opened by a forward fluid flow and closed by a reverse flow. Most of the check valves [1] consist of a bulk micromchined orifice, and a deflectable sealing element. They usually require chip to chip bonding to form the two-element structure, including the most recent "in-plane" micro check valves [2]. Even though the previous Parylene micro check valve [3] (chapter 4) is made by a single chip, it still requires off chip fluidic coupling (tube connection) when used in a micro fluidic system. The fluidic coupling can include bonding, gluing, and clamping the inlet and outlet to the rest of micro fluidic system. The overall cumbersome manual assembly and interconnection process can bring in intolerable fluidic dead volumes, contamination from glue and tubing, low yield and high cost. Therefore, an integrated micro check valve, which is built inside a microchannel to rectify channel flows, is a crucial component needed in an integrated micro fluidic system. It is ideal that micro check valves could be placed anywhere inside the microchannel during the formation of the microchannel network. They can be used individually to isolate channel flows according to their directions, or can be used in pairs to direct flows in an integrated micro reciprocating pumps. Analogous to electronics, such an in-channel micro check valve is similar to a diode, which is a basic building block to realize digital and logical functions in an integrated circuit.

Most importantly, many micro fluidic systems require liquid flow rate in the order of nL/min. However, around this flow rate, none of the reported check valves are perfectly closed normally, which implies intolerable reverse leakage.

In an interesting approach, Man *et al.,* [4] reported an in-channel stop valve that uses the liquid/gas surface-tension interface to provide the stopping force. However, multiphase fluid (gas/liquid) operation is problematic. Gas bubbles are to be avoided in many micro fluidic systems, due to fact that gas bubbles bring in extra flow resistance and difficulties of flow control.

Consequently, the goal of the work in this chapter is to develop a check valve that is in-channel, normally closed, monolithically fabricated and can be used in two-phase (gas, liquid or mixture) integrated microfluidic system. The targeting liquid flow rate is in the range of nL/min.

5.2 Normally Closed Mode Design

5.2.1 The Need of a Normally Closed Mode

Most reported micro check valves operate in a normally opened mode, which means the valve is expected to be closed by a reverse flow or an applied reverse pressure. Two in-channel micro check valves are initially designed and fabricated as shown in Fig. 5-1. The fabrication process will be described in detail in Section 5.4. Basically, Parylene is used as a structural layer and photoresist is used as a sacrificial layer in forming the valves and channels. As shown in the cross-sectional view, the check valve consists of a two level flow channel with an opening in between and a thin flap on top the opening. There exists a fine gap (1.5μm) after the photoresist layer removal. Forward flow, as indicated, can pass through the check valve

with non-detectable flow resistance. However, there is no stop for the reverse channel flow when a minimum of 30kPa reverse pressure is applied. As a result, the sealing flap can not be closed by the reverse pressure or flow.

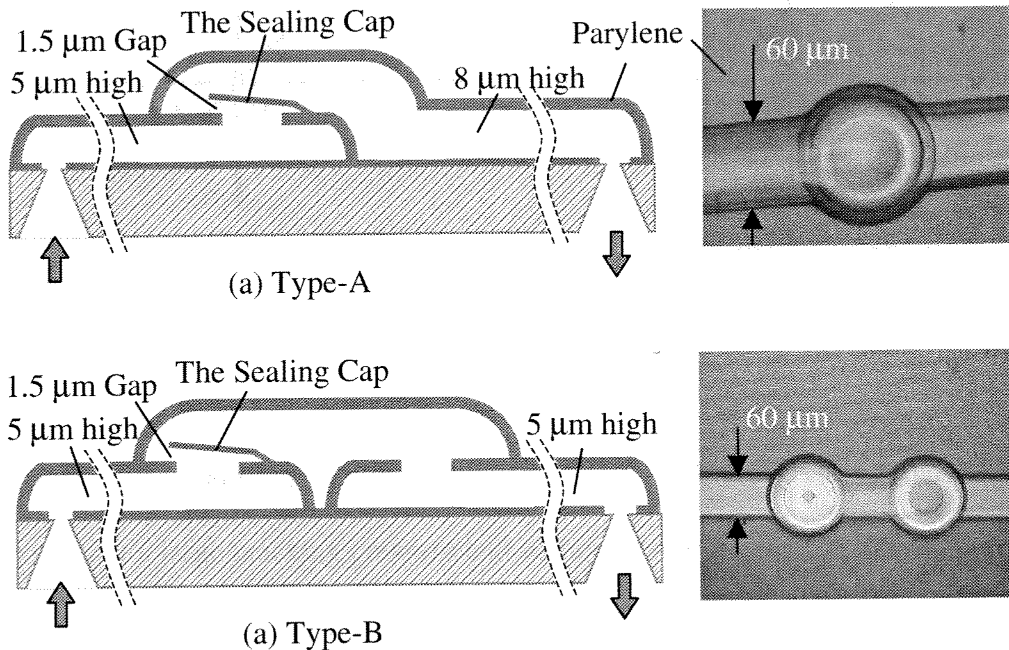


Figure 5-1 Schematics and picture of normally open, in-channel micro check valves

The normal pressure-flow curves for a normally open mode (NO) and a normally closed mode (NC) are shown in Fig. 5-2. The intrinsic problem of a NO operation mode is that if there is not enough reverse pressure or reverse flow rate, the valve fails to work in the shaded region as shown. Unfortunately, the in-channel check valve operates in this region and the minimum reverse pressure to close the valve in the reverse direction could not be detected. The most interested on-chip flow rates are below 100nL/min, which is too small to create adequate pressure difference across the sealing plate to force it close when flow reverses. On the other hand due to the surface effect dominant microfluidic behavior, the liquid has tendency to wick

into fine gaps from relatively larger geometry, which will make plate closing more difficult in an normally open mode.

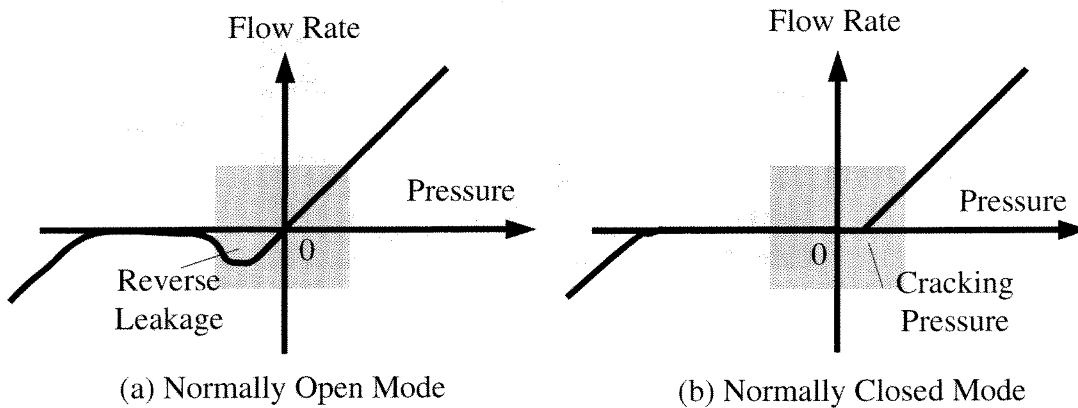


Figure 5-2 Normal Flow rate vs. Pressure of check valves

Therefore, for many micro flow applications, we need check valves that are normally closed but without a large cracking pressure and without a significant spring force to reduce the pressure drop in the forward direction.

5.2.2 Vacuum-Collapsed Sub-chamber Design

The essential element of realizing a normally closed mode is to create a spring force on the sealing plate. The entire valve construction, including the microchannels, is designed to use the developed Parylene process. The operating structure of the check valve is a circular sealing plate on top of a ring-shaped valve seat as shown in Fig. 5-3. The sealing plate is center-anchored on top of a chamber diaphragm that is vacuum-collapsed to the bottom of the chamber in order to achieve a normally closed position.

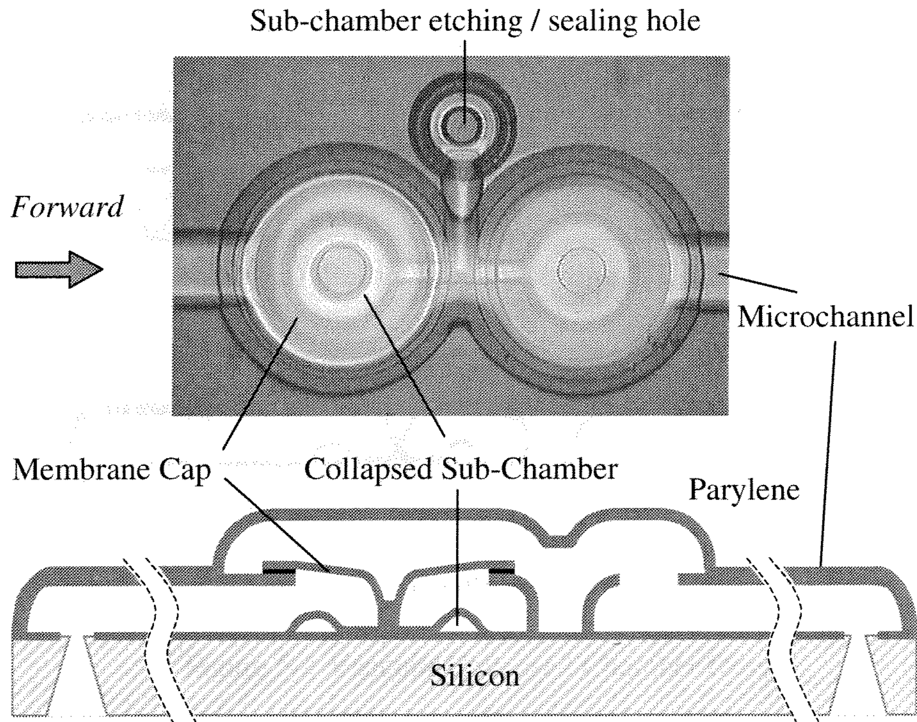


Figure 5-3 A normally close, in-channel Parylene micro check valve

In this novel design, notice the sub-chamber is isolated to the fluid flow channel. After the sacrificial layer (2.5μm thick) etching, as usual, there is a fine gap with a height of h_1 between the valve seat and the sealing plate. However, the sealing plate is center-anchored on top of a sub-chamber with a height of h_2, where h_2 is larger than h_1. After the release from sacrificial layer etching, the etching hole of the sub-chamber is sealed by room temperature Parylene deposition. Since the deposition occurs in vacuum (20~30 mTorr), after taking out to atmosphere, the sub-chamber diaphragm is collapsed to the bottom of the chamber due to the pressure difference across diaphragm. Fig. 5-4 shows the check valve structure before and after vacuum sealing of the etching hole.

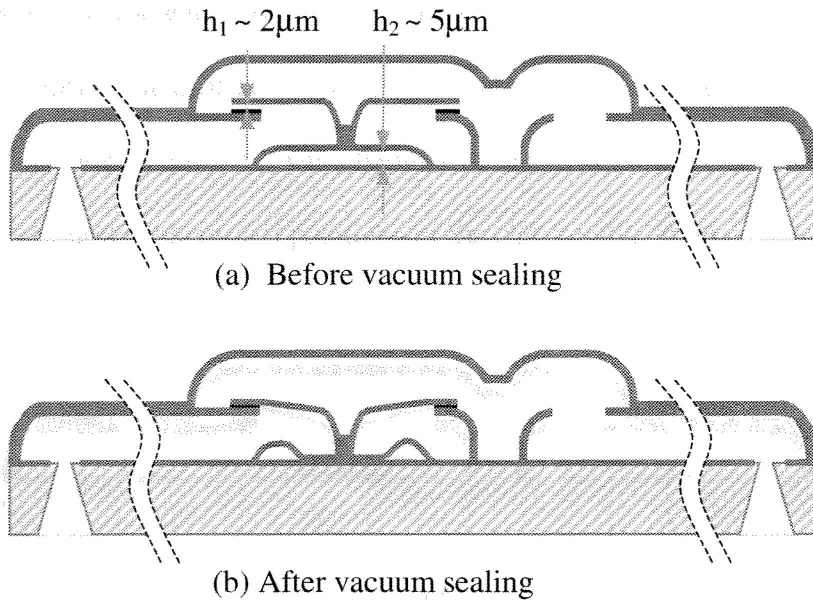


Figure 5-4 Vacuum-Collapsed Chamber Design

The sealing is verified by the existence of Newton rings as shown in Fig. 5-5. The sub-chamber sealing process is tested separately to optimize the design parameters.

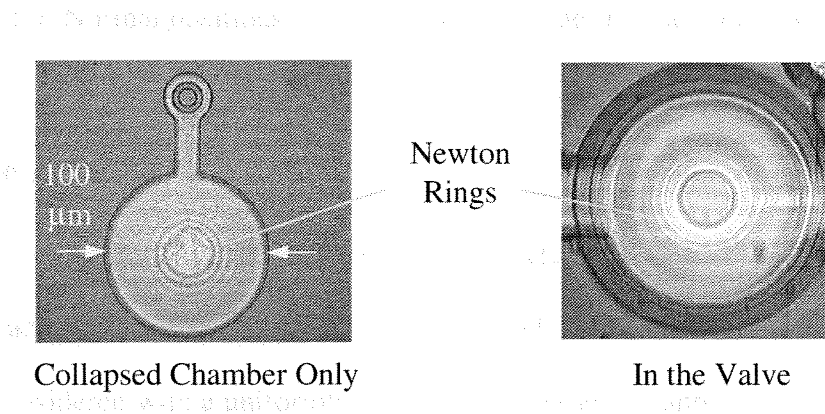


Figure 5-5 Vacuum sealed micro-chambers

Because of the small Young's Modulus of parylene (~3 GPa), the Parylene chamber diaphragm is easily collapsed with about 1 atm pressure difference even for diaphragm sizes

smaller than 100μm in diameter. As a result, the sealing plate is brought down to completely eliminate the gap initially and offers a spring force when the check valve operates. Therefore, by adding this vacuum collapsed sub-chamber a normally closed mode is successfully achieved. Fig. 5-6 shows the normal positions of the check valve in open and in close.

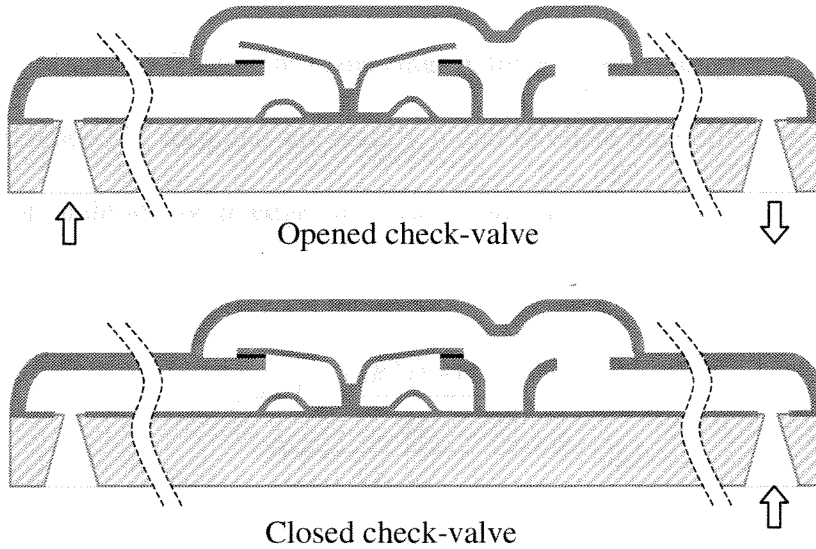


Figure 5-6 Normal positions of the sealing cap under forward and reverse pressure

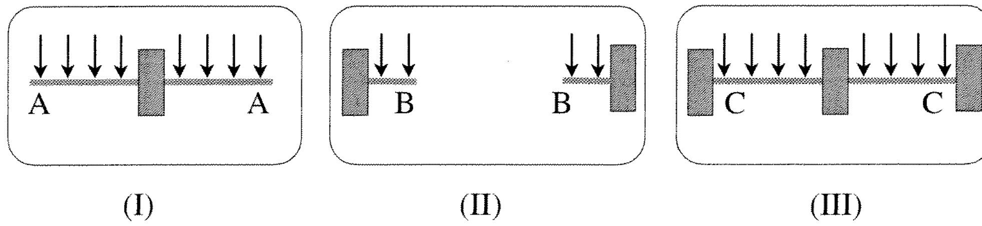
5.3 Structure Analysis

In order to made reasonable parameter choices, it is important to study the load-deflection characteristics of both the sealing plate and the circular valve seat. Here three structures are considered with a uniformly distributed pressure *(q)* applied.

(I) The sealing plate is represented as an outer edge free, inner edge fixed circular plate as shown in Fig. 5-7(a).

(II) The valve seat is represented as an inner edge free, outer edge fixed circular plate as shown in Fig. 5-7(b).

(III) The sticking sealing plate is represented as a both outer and inner edge fixed circular plate as shown in Fig. 5-7(c).



(I) (II) (III)

Figure 5-7 Circular plate, rings at three fixed edges positions

From reference [5], formulas are readily found to relate the deflection and loading. The general expression of deflection at edges for case (I) and (II) is:

$$y = \underbrace{\left[K_y \frac{12R^4(1-v^2)}{Et^3} \right]}_{k_A^{-1},\ k_B^{-1}} q \tag{5.1}$$

where the Poisson ratio (v) of Parylene is about 0.3. The unit shear force (force per unit of circumferential length) in case (III) at the edge is expressed as:

$$Q_C = \underbrace{\left[K_Q r - \frac{(R^2 - r^2)}{2R} \right]}_{k_C^{-1}} q \tag{5.2}$$

where the values of R, r, and t are listed in Table 5-1. And the corresponding K coefficient at three position, A, B, C are listed in Table 5-2. Notice, k_A and k_B are actually the spring constants of the sealing plate and the circular valve seat at position A and B. Their calculated values are also listed in Table 5-2. On the other hand, in equation (5.2), the unit shear force can be related to the surface energy when q is the minimum value to delaminate the sealing plate from the valve seat.

R_I	r_I	t_I	R_{II}	r_{II}	t_{II}
60	15	0.75	60	55	2.5

Table 5-1 Inner, outer diameters and thickness (μm)

K_{yA}	K_{yB}	K_{QC}	k_A (N/m^3)	k_B (N/m^3)	k_C $(1/m)$
-0.0318	-0.00032	0.0006	$-5.8\text{x}10^8$	$-2.8\text{x}10^{10}$	$4.4\text{x}10^4$

Table 5-2 Spring constants of case (I), (II) and unit shear force in case (III)

From Table 5-2, it is noticed that the spring constant of the valve seat is two orders larger than the sealing plate. For example, in order to generate 5 μm bending at outer edge of the sealing plate, it requires about 2 kPa uniformly distributed pressure. While with a pressure of 200 kPa, the inner edge of the valve seat only deflects less than 1μm. Therefore, it can safely assume that the valve seat is normally fixed while the sealing plate deflected under the interested pressure range. It can concluded from the above analysis that ideally it only requires approximate 2 kPa (cracking pressure) to bend the sealing plate to allow fluid flow. Consequently, the pressure drop caused by the deflected plate during flow should also be approximate 2 kPa.

Stiction Reduction

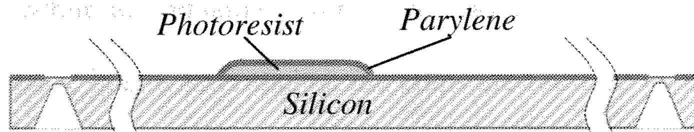
Unfortunately, surface stiction force between the sealing plate and the valve seat is quite large in micro systems. And the experimentally measured cracking pressure is much larger than 2kPa. Therefore, minimization of the cracking pressure by reducing the surface stiction requires much more attention in the fabrication process. In the design, the overlap of the valve

seat and sealing plate to a 10 μm narrow ring is first reduced. We also roughened the valve seat surface and applied a thin gold layer to effectively reduce the stiction. The testing results will be shown in later sections.

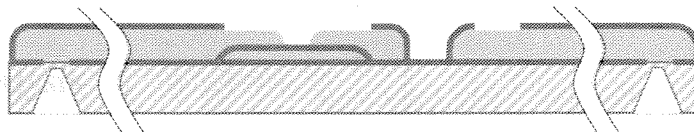
5.4 Fabrication

The major fabrication steps are shown in Fig. 5-8. The entire check valve and channels are constructed using Parylene-C, while photoresist is used as the sacrificial layers. In general, all the photoresist sacrificial layers are hard baked (120°C) for 20 minutes immediately after the lithography. This is necessary for baking out all the solvent to prevent structure deformation later on. On the other hand, hard baking also offers smoother sidewalls of the structures. As a standard process, all the Parylene layers are deposited on the front wafer side only and patterned in oxygen plasma of 400 W and 400 mTorr oxygen pressure.

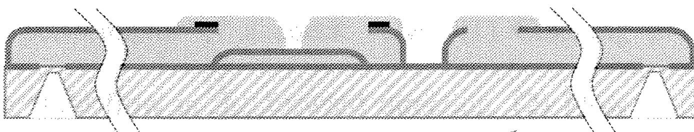
The process starts with a 4-inch silicon wafer with a 1.5 μm thick thermal oxide. The inlet/outlet cavities are created by KOH etching while leave a 10~20 μm silicon layer. The front side silicon is exposed and roughened by gas phase BrF_3 etching for the purpose of Parylene adhesion enhancement. A-174 adhesion promoter is also applied before the deposition of the 1st Parylene layer. A 4 μm AZ4400 layer and 1.5 μm AZ1518 layer are spun and patterned to form the sub-chamber and its etching path for ease of sealing later on. A 2 μm thick 2nd Parylene layer is deposited to form the roof of the sub-chamber and patterned with the 1st Parylene to expose the inlet/outlet. 5 μm thick channel photoresist is spun and patterned followed with a 3 μm thick 3rd Parylene layer deposition. The Parylene surface is treated in oxygen plasma for 1 minute and followed by a thin Cr/Au layer (100A/200A) on top. The valve seat is created by patterning the 3rd layer Parylene. Then a 2 μm AZ1518 photoresist and 0.7 μm 4th Parylene are layered on and patterned to form the sealing plate.



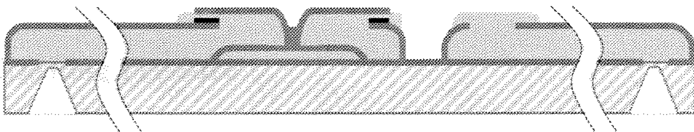
- 1.5 μm thermal oxide
- Back side KOH etching
- BrF_3 Si surface roughening
- 1 μm Parylene-C deposition
- 5.5 μm hard-baked PR
- 1μm Parylene deposition/patterning



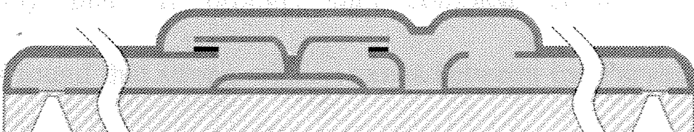
5 μm hard-baked PR & 3 μm Parylene-C deposition



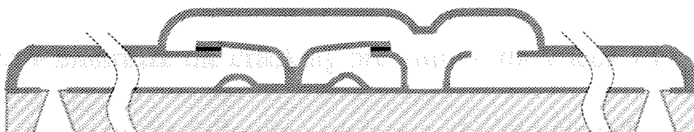
- Evaporation of 100A Cr & 200A Au
- 2 μm hard-baked PR



0.7 μm Parylene deposition and patterning



8 μm hard-baked PR & 3 μm Parylene deposition



- BrF_3 back side Si etching / Acetone PR etching
- Vacuum sealing by Parylene deposition

Figure 5-8 Major Process Flow

An 8 μm thick AZ4620 photoresist layer and 3 μm 5th Parylene layer are formed to encapsulate the check valve. This Parylene layer is patterned to expose the etching hole of the

sub-chamber on top, while the remaining thin silicon layer is remove by BrF_3 to expose the inlet/outlet from the back side. After dicing, the chips are released by an acetone photoresist removal. Finally, 2 μm thick Parylene layer is deposited to seal the sub-chamber etching holes.

5.5 Test and Analysis

In rectification of fluid flow, as shown in Fig. 5-3(b), there are four parameters associated with the performance of a check valve. (1) Cracking pressure: The minimum pressure required for fluid flow in the forward direction. (2) Flow resistance in the forward direction. (3) Leakage in the reverse direction, and (4) the maximum reverse blocking pressure.

Stiction Test and Cracking Pressure

After photoresist sacrificial layer etching and the vacuum sealing of the collapsed sub chamber, the sealing plate is brought into complete contact with the valve seat. Experimentally, it is found that strong stiction exists between the Parylene surfaces. Cracking pressure is then defined as the minimum pressure required to allow the forward liquid flow. The goal of the stiction test is to characterize the surface energy between following contacting surfaces and eventually minimize the cracking pressure of the check valve. Parylene cantilever beams are fabricated on top of the following surface with sandwiched photoresist layer.

A: As deposited Parylene bottom surface;

B: Cr/Au (200A/100A) on top of Parylene surface of A;

C: Parylene surface treated in O_2 Plasma (400 mTorr, 400W) for 1minute;

D: Cr/Au (200A/100A) on top of Parylene surface of C.

After photoresist sacrificial layer being etched in acetone, a portion of the beams are found attached to the bottom Parylene surface. Fig. 5-9 shows a cross section of a Parylene cantilever beam of lengths 20 μm to 400μm, detachment length *L*, width *w* (20μm), thickness *t* (2μm), gap *h* (3μm), and Young's Modulus *E* (3GPa).

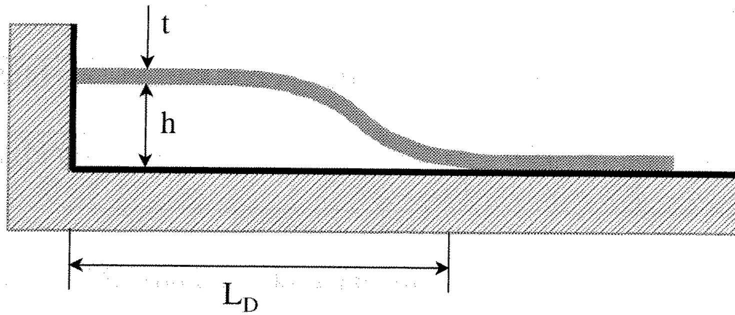


Figure 5-9 Cantilever beam adhesion test

The measured detachment lengths are listed in Table 5-3.

The surface energy per unit area γ_s is calculated by using the following equation. [6]

$$\gamma_s = \frac{3}{2}\frac{Et^3h^2}{L^4} \tag{5.3}$$

	A	B	C	D
L (mm)	30	35	55	60
γ_s(N/m)	2.4	1.3	0.2	0.15

Table 5-3 Measured detachment length, calculated surface energy

From the table, it is noticed while L_D is more than twice as large as L_A, the surface energy is 16 times lager than the L_A case. This also corresponds to the experimentally measured cracking pressure shown in Table 5-4.

	A	B	C	D
P_c(kPa)	200~270	200~240	35~60	20~40
Q_C(N/m)	4.7~6.3	4.7~5.4	0.7~1.4	0.4~0.9

Table 5-4 Measured cracking pressure and calculated peeling force per unit circumferential length.

With the measured cracking pressure, the pealing force per unit circumferential length Q_C can be also approximated by using equation (2) with the assumptions of rigid plate and small deflection. It is also noticed that Q_C has the same unit as the surface energy (J/m^2). From the calculated results shown in Table 3 and 4, the surface energy calculated by the cantilever detachment length and the peeling force calculated by the cracking pressure are in the same order of magnitude. The conclusion is that the O_2 plasma treated Parylene surface with a thin Cr/Au layer can reduce the surface stiction and the cracking pressure effectively.

Flow Resistance

An important characteristic of a check valve is the flow resistance caused by the deflected plate. On the same chip, there are two independent fluid paths with identical channel and inlet/outlet geometry. The check valve structures are also identical except that one has a missing plate. Using this chip, the flow resistance caused by the deflected plate can be measured. As shown in Fig. 5-10, the DI water volume flow rate is plotted against the pressures applied at the channel inlets for both channels. For less than 12.4 kPa, the pressure is

applied by a water column with a specified height, while compressed air is applied on top of a water column to generate pressure between 12.4 kPa to 41 kPa.

It is noticed first, without the plate, the liquid flow rate is quite linear, with a flow resistance about 16nl/min/psi. With the plate, above the cracking pressure (20kPa), we can see a similar flow resistance, but the pressure required to generate a typical flow rate is about 7kPa larger, this is the range for the fluid to overcome the restoring force of the deflected plate.

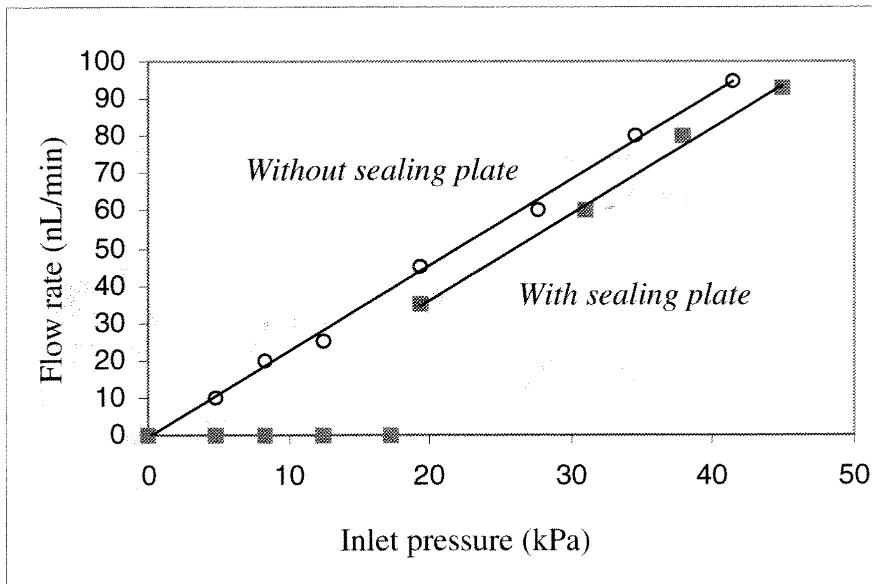


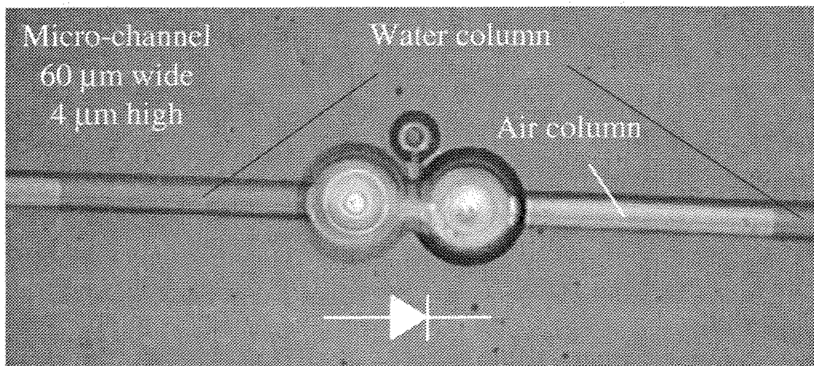
Figure 5-10 Forward flow rate vs. increasing inlet pressure

Due to the difficulties of small flow rate measurement, the measured data has an error about 10% to 20% where Fig. 5-9 shows only averaged results. Another thing worth mentioning is that even though the check valve can work for liquid and liquid/gas mixture, the gas bubbles usually have large effects on the flow characteristics. Gas bubbles are normally trapped within the microchannels upon liquid introduction. They disturb of the dynamics of the micro check valve for two reasons. First, the damping properties of the gas bubbles require larger forward pressure to facilitate a certain liquid flow rate. Second, the surface tension of

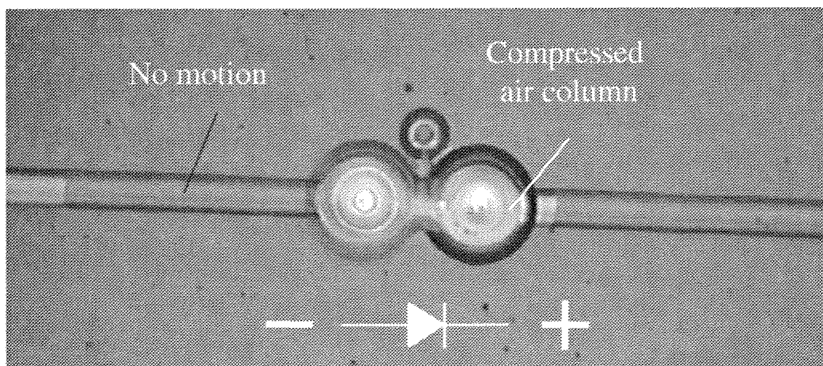
gas bubbles leads to a significant increase of the cracking pressure. Therefore, gas bubbles are avoided as much as possible during test and operation.

From the above test, the importance of reducing the cracking pressure is realized. Because of the existence of the cracking pressure, once the valve opened, the flow immediately starts with a flow rate larger than 50nL/min. In other words, the minimum initial flow rate is 50nl/min, while lower flow rates can only achieved afterwards.

Lastly, an interesting experiment of a working check valve is in Fig. 5-11.



(a) No pressure applied



(b) ~ 55 kPa Reverse pressure applied

Figure 5-11 Video snap shots when reverse pressure applied

In Fig. 5-11(a) there is an air column in between two water columns fed in from the forward flow. Fig. 5-11(b) shows the same structure under a reverse 55 kPa pressure. One can see that the left water column has no motion at all, while the air column is greatly compressed (so that the right water column does advanced toward the check valve). The reverse pressure can be progressively increased up to 270kPa, before the check valve fails. A novel inlet design (Fig. 5-12) with reinforced posts contributes to tolerating the higher inlet pressure.

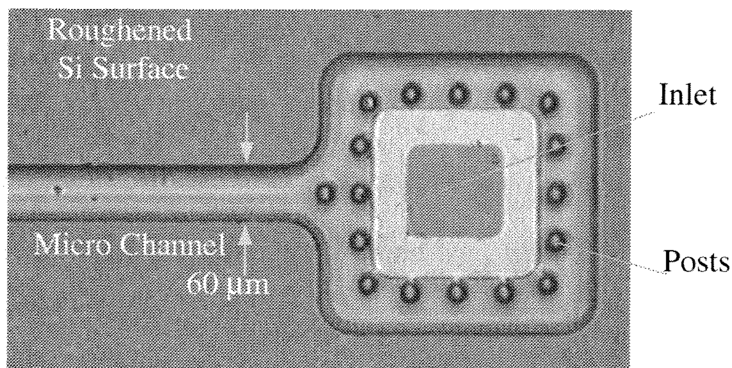


Figure 5-12 Inlet / Outlet of the microchannel

5.6 Summary

A surface-micromachined, normally closed, in-channel micro check valve is presented for using in integrated micro fluidic systems. This device is fabricated monolithically on silicon substrate using a multi-layer Parylene process. The main structure of the check valve is a circular sealing plate on top of a ring-shaped valve seat. The sealing plate is center-anchored on top of a chamber diaphragm that is vacuum-collapsed to the bottom of the chamber so as to achieve a normally closed position. Moreover, a thin gold layer on the roughened valve seat surface is used to reduce stiction between the sealing plate and the valve seat. As a result, an in-channel check valve with a cracking (opening) pressure of 25 kPa under the forward bias and without any measurable leakage under the reverse bias up to 270 kPa has achieved. This valve performs in two-phase microfluidic systems, i.e., microchannel flows containing gas, liquid, or gas/liquid mixture. The vacuum enforced sub-chamber design and Parylene surface stiction reduction techniques are useful in making other integrated micro fluidic components.

5.7 References

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Chapter 6

A Post-CMOS Integrated Shear Stress Sensor

6.1 Introduction

6.1.1 Drag reduction

Drag reduction is of great interest [1] in the continuous efforts of having airplanes and other man-made vehicles moving faster using less energy. There are many sources of drag on an object moving through a fluid. One type is the pressure or form drag, which results from the negative pressure differential between the front and the back of a moving object. A fluid flow past an object may separate from the object and form a wake behind the object. The flow separation leads form drag. Another type of drag is viscous or skin-friction drag, which exists within a thin region (i.e., a boundary layer) adjacent to the object. Form drag reduction is considered in the shape design of a moving object, while friction drag exists at any surface moving through a fluid. Friction drag is especially high in turbulent flow and is practically important to study and reduce skin friction drag.

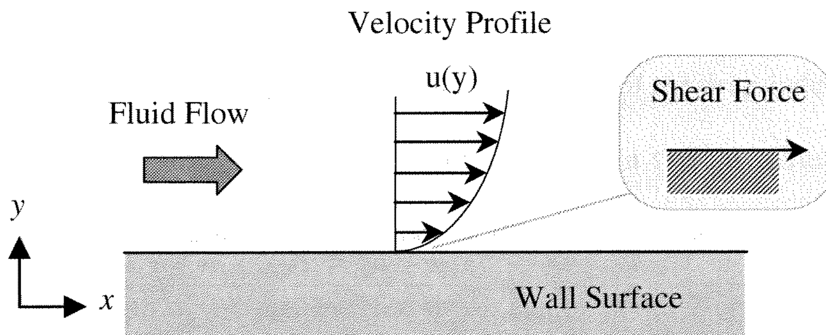


Figure 6-1 Schematic description of flow velocity profile and shear stress on a surface

In general, an object exposed to a flow experiences a shear force on its surface, due to the viscosity of the fluid as shown in Fig. 6-1.

If a no slip boundary condition is applied to the flow field immediately adjacent to the solid surface, the tangential velocity of fluid flow at the surface is zero. Within the boundary layer, the velocity increases in a very short distance from zero to the free-stream velocity. The shear force per unit area is the shear stress τ_w, which is related to the flow velocity profile by

$$\tau_w = (\mu \frac{\partial u}{\partial y})_{y=0} \tag{6.1}$$

Where μ is the viscosity of the fluid evaluated at the surface temperature, u is the streamwise fluid velocity, and y is the axis normal to the surface.

The drag force (F_d) caused by this skin friction is the shear stress integrated over an area (A), can be expressed as follows:

$$F_d = \int_A \tau dA \tag{6.2}$$

High skin friction drag has been linked to the vortex structure [2] formed with in the turbulent boundary layer. These structures consist of counter-rotating vortex pairs that travel downstream. As shown in Fig. 6-2, between these vortex pairs, faster moving fluid is brought down to the surface and result in a higher velocity gradient, thus high shear stress. Such local increase of shear stress can contribute to a large friction. These vortex structures are quasi-random in space and have a finite lifetime. The statistical size of the drag-inducing vortex pair streak decreases with the Reynolds number of the flow. For a typical airflow of 15 m/s in UCLA wind tunnel tests, and a Reynolds number of 10^4, the vortex streaks have a mean width of about 1mm. The length of a typical vortex streak can be about 2 cm, giving the streaks a 20:1 aspect ratio. The frequency of appearance of the streaks is approximately 100 Hz. The lifetime is about 1 ms [3]. Consequently, a logical drag reduction approach is to detect and interact with these vortices at similar spatial and temporal scales. In other words, it requires

distributed sensing, actuation and control that can only be implemented with a large number of MEMS devices and control circuitry. Hardware wise, wafer-scale integration of these MEMS devices with IC (integrated circuit) electronics is believed to be the only way to achieve this goal.

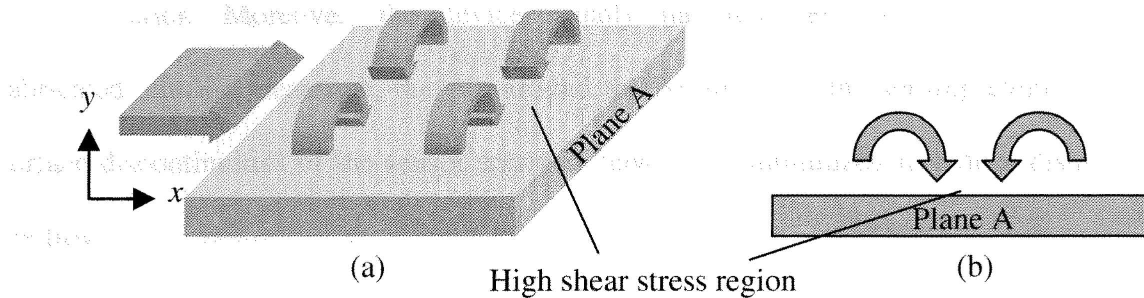


Figure 6-2 Simplified (a) perspective and (b) side views of a counter-rotating vortex pair [1]

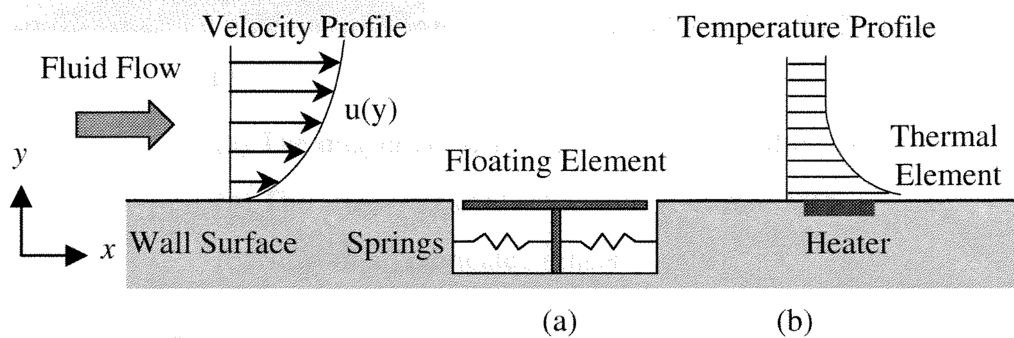
6.1.2 The shear stress measurement

The measurement of shear stress is of primary importance in a drag reduction system. It provides the basic experimental information for the modeling, simulation and active control of turbulence flow. The basic requirements for a shear stress sensor are its spatial and temporal resolution and the feasibility to be integrated with microelectronics and micro actuators.

The wall shear stress (tangential stress) measurement is much more difficult than the normal stress measurement. Over the years many techniques [4] have been developed. However, there is no universal solution exists for accurate determination of wall shear stress for every situation. The techniques can be categorized into direct and indirect methods. Fig. 6-3(a) is a schematic representation of the floating-element method of direct shear stress measurement [5]. The shear force exerted by the fluid flow on the surface of the floating element is balanced by the restoring force of the spring. The spring force or the small displacement of the floating element is measured to determine the wall shear stress.

The advantage of such a direct measurement is that no assumptions have to be made to relate the shear stress to the measured quantities. However, the sensitivity and shear stress range of the measurement are determined by the spring constant of the system and the area of the floating element. In other words, there is a trade off between sensitivity and miniaturization. Moreover, the device usually has relatively complex structures to be fabricated. In the meantime, the gap around the perimeter of the sensing element and other surface discontinuities of the sensor structure have to be minimized to reduce disturbances to the flow.

In indirect methods, the shear stress information is extracted from other related physical parameters, such as pressure and temperature. The techniques include Stanton tube/razor blades, Preston tubes, heated-films/wires, and liquid surface tracing [4]. Among them, measurements based on thermal transfer principles have been widely used, especially with MEMS technology [6,7]. The operating principle of the sensor is to relate the rate of heat loss of the sensor to the velocity profile in the fluid boundary layer (Fig. 6-3(b)).



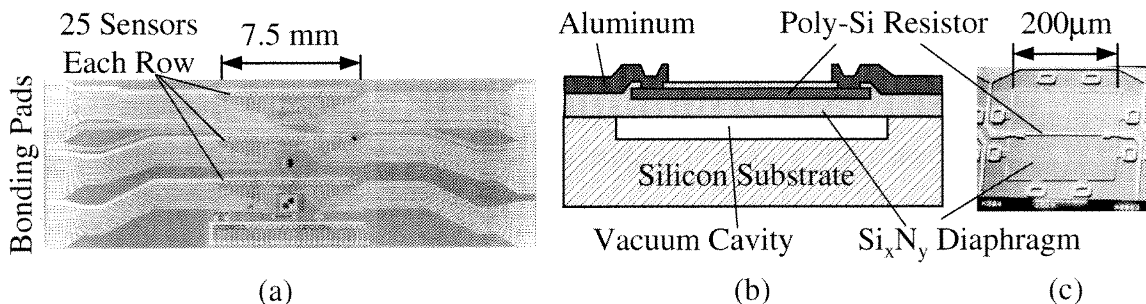
(a) Direct measurement using a floating element

(b) Indirect measurement using a thermal element

Figure 6-3 Schematic description of shear stress measurements

According to Ohm's Law, as a voltage is applied to a polysilicon resistor, the current flow in the resistor is inversely proportional to the resistance. A physical property of polysilicon is that as the operating temperature increases, the resistance increases. Therefore, we can either relate the heat loss rate to the resistance measurement while maintaining a constant current (CC mode), or to the current measurement while maintaining a constant sensor temperature (CT mode).

A MEMS hot-film/wire shear stress imager (Fig. 6-4) was developed for use in the drag-reduction system by Jiang *et al.* [7] at the Caltech Micromachining Group. The imager consists of multiple rows of shear stress sensors with a 300 μm pitch. Each sensor consists of a polysilicon resistor sitting atop a silicon-nitride diaphragm with a sealed vacuum cavity underneath it for thermal isolation.



(a) The imager consists of 3 rows of shear stress sensors

(b) The cross-sectional schematic of each sensor

(c) SEM of an fabricated sensor

Figure 6-4 Previous caltech shear stress imager, [3] *Jiang et al. MEMS 1996*

Many features of the fabricated sensor are detailed in Jiang's Ph.D thesis [7]. For example, compared to other sensing methods, it has negligible interference with the flow; the size to the sensor can be smaller than 0.5 mm; the possibility of measuring fluctuations in the

wall shear stress as well as the time average makes them particularly attractive for turbulent flow measurement. Compared to conventional metal film resistors, it offers high sensitivity in low thermal conductivity fluids such as air. The general disadvantages for this kind of thermal method are the complicated sensor calibration process and susceptibility to environmental temperature fluctuations.

6.1.3 Challenges of integrated shear stress sensors

The capability of the above mentioned hot-wire shear stress sensor for imaging surface shear stress distributions was successfully demonstrated. However, the greatest technical challenge is how to integrate the sensors with necessary microelectronic circuitry and micro actuators on a monolithic chip [8]. The next task would be to seamlessly interface microelectronics with the non-electronic world in an integrated manner. The concept of integration has two tasks: fabrication process integration by using compatible materials and micromachining techniques; and functional integration to realize integrated sensing, actuating, calculation and control.

The integration needs for drag reduction systems are obvious. Any system designed to reduce the drag caused by the turbulent vortices should be distributed and should have localized control. First, only integration can greatly reduce the total number of external electrical leads. This is especially important for a distributed system where a large number of sensor arrays are involved and shown in Fig. 6-4(a). Second, it can reduce the electromagnetic noise caused from outside sources and parasitic effects if many external leads were used. Finally, only integration can realize a batch fabrication process to save time and reduce production cost.

The integration of shear stress sensors with microelectronics is not trivial [8]. It is important to take advantage of matured IC fabrication processes to ensure robust integration with the MEMS device. However, the desirable LPCVD silicon nitride (with controllable thickness and stress) for the above shear stress sensor is not available from standard IC processes and no IC foundry could accommodate the fabrication process. On the other hand, due to the non-IC MEMS materials, processing steps, and contamination concerns, extremely few IC facilities allow pre-processed wafers to enter their production line. As a result, a practical approach to achieve this goal is to fabricate MEMS devices onto IC-foundry-finished wafers. This method, first developed in university laboratories, is called a post-IC process [9,10,11]. Since about 80% of industrial IC manufacturing is performed in CMOS (complementary metal-oxide-semiconductor) technology, this approach is also called a post-CMOS process.

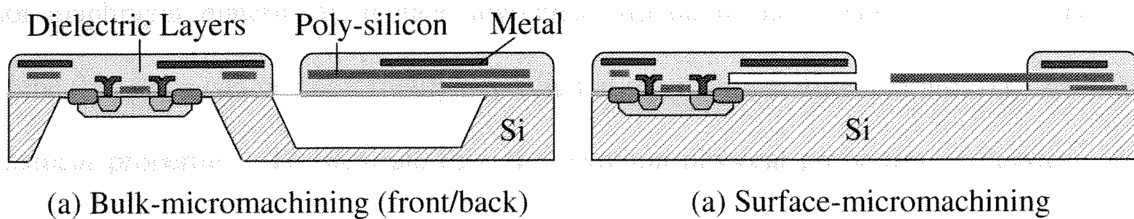
6.2 Post-CMOS MEMS technology

6.2.1 The advantages and limitations of Post-CMOS MEMS

One primary advantage of the post-processing approach is that silicon foundry-based IC processing is a mature technology and there are many choices of IC foundries that can provide wafer-level electronics, which are fast, reliable, repeatable, and economical. Such wafers are then subjected to MEMS processing, which can be carried out outside of the VLSI fabrication line. In this step, non-IC materials and micromachining techniques can be added on. However, to ensure the functionality and integrity of electronic circuit, there are many limitations on the add-on MEMS processes. One obvious limitation is on the processing temperature, i.e., all post-IC processing should be performed below 450°C, which is about the temperature that the

aluminum used for electronic connections can withstand. This limitation rules out the application of LPCVD silicon nitride and polysilicon that we would like to deposit on the wafer to form the sensor structure layers, because they are typically deposited at around 800°C.

Due to above temperature concerns, a logical approach is to use CMOS materials as the MEMS structural materials (to make bridges, membranes, diaphragms, etc) and sacrificial layers. The existing CMOS materials include bulk silicon, doped polysilicon, dielectrics (silicon oxide, silicon nitride, passivation), and metal (mainly aluminum). Over the years, many integrated MEMS devices [11] have been reported using this approach. They can be categorized to post CMOS bulk micromachining and surface micromachining as shown in Fig. 6-5.



(a) Bulk-micromachining (front/back) (a) Surface-micromachining

Figure 6-5 Schematics of post-CMOS micromachining techniques

There are many problems that one can encounter when using CMOS materials for MEMS. For example, freestanding MEMS structures made by CMOS materials often curl out of the substrate plane or even crack spontaneously. The reason is that the primary concern for CMOS foundries is producing films with reliable electrical properties, and optimized for these, not mechanical properties. As a result, such CMOS material based microstructures can suffer from large residual stresses and stress gradients, which may vary from run to run. These stress gradients can also be vertical if composite layers are used to form freestanding microstructures.

In addition, the thickness of the layers of such materials are always fixed for the sake of IC optimization, which greatly limits their use for many MEMS devices that require high-aspect-ratio structures.

Consequently, it is decided to change the strategy and develop a low-temperature post-IC process. In this process, a new MEMS structure material is added to the CMOS wafers with corresponding etching techniques to create microstructures, such as diaphragm-cavity type for the integrated shear stress sensor.

6.2.2 Post-CMOS Parylene MEMS

A CMOS-add-on process is developed using Parylene N (poly-para-xylylene) as the sensor diaphragm material to replace low-stress silicon nitride. This is because not only Parylene thin films can be conformally deposited at room temperature, but also they have good mechanical properties. To illustrate this, the common physical properties of Parylene N are compared with LPCVD silicon nitride in Table 7-1. Since the designed operation temperature of the sensor is 120°C, Parylene-N is therefore chosen as the diaphragm material because it has highest melting temperature among the three types of Parylene. The thermal conductivity of Parylene is about an order of magnitude less than that of silicon nitride; therefore, the heat conduction loss through the diaphragm to the substrate is significantly reduced. Although the linear thermal expansion coefficient is much larger than that of nitride, the internal stress of a parylene film caused by thermal effects is low due to its small Young's modulus.

	Young's Modulus (GPa)	*Intrinsic Stress (MPa)*	*Thermal Conductivity (W/cmK)*	*Thermal Expansion (1/°C)*	*Melting Point (°C)*
PA-N	*3*	*20*	*0.0013*	*7×10^{-5}*	*420*
Si_xN_y	*300*	*200*	*0.032*	*8×10^{-7}*	$>10^3$

Table 6-1 Comparison of mechanical properties of silicon nitride and Parylene-N (PA-N)

The Post-CMOS approach is to use the 1st layer CMOS poly-Si as the sensor element. In order to minimize the heat loss to the substrate, a diaphragm-cavity structure is needed. Here, it is achieved by the combination of Parylene deposition and BrF_3 [12,13] gas-phase etching. All the dielectric layers around the sensor element are to be removed and replaced by a post-deposited Parylene layer and then create a diaphragm-cavity structure as shown in Fig. 6-6.

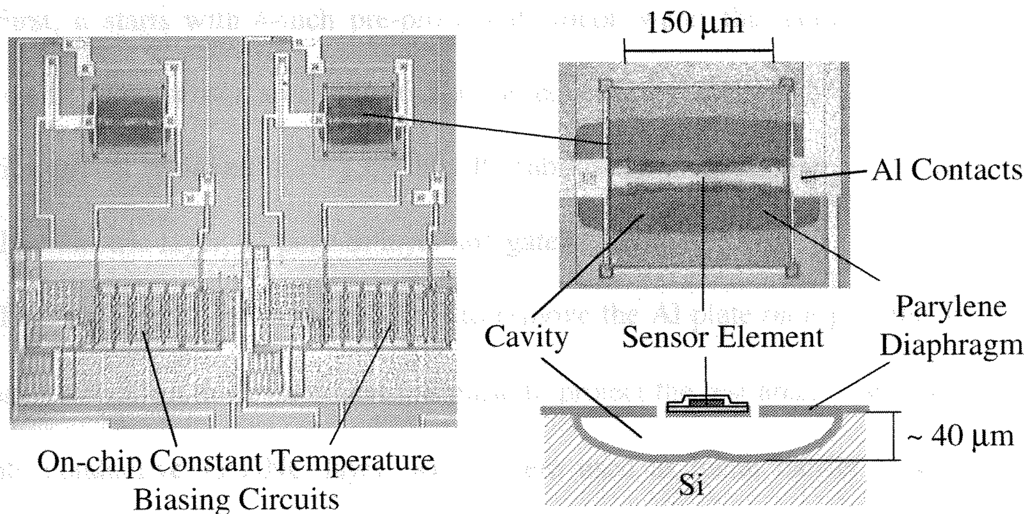


Figure 6-6 Fabricated shear stress sensors with on chip circuits

6.3 Design and Fabrication of integrated shear stress sensor

6.3.1 Design and CMOS fabrication

The on-chip CMOS circuit contains the sensing element, biasing circuit and operational amplifier. The circuit layout was done by V. Koosh from Professor R. Goodman's group at Caltech. While the CMOS fabrication was achieved by using the Mitel Semiconductor [14] standard 2 μm double-poly, double-metal process. The sensing element is made of the first polysilicon, which has a thickness of 3200A, a sheet resistance of 20 Ω/square, and the temperature coefficient of resistance (TCR) of 0.1%/°C. Under the first polysilicon is a 300A thick gate oxide layer.

6.3.2 Post-CMOS sensor fabrication

To make an effective diaphragm-cavity Parylene structure in the post-CMOS process, the most important consideration is to choose compatible micromachining techniques.

The major post-CMOS fabrication steps are shown in Fig. 6-7.

First, it starts with 4-inch pre-processed silicon wafer that contains all the necessary circuits on it. The sensor area (Fig. 6-7(a)) is covered by metal 1 and metal 2 layers with passivation layers removed during the last IC fabrication step. Under the metal plate is the inter-poly dielectric layer, 1st poly-Si layer and gate oxide layer.

The first step of the post-process is to remove the Al plate on top of the sensor area by Al etchant using 3 μm thick photoresist as mask to protect the rest area. Underneath the Al is a composite conductive Ti/TiNC layer, which were used as metal barrier between metal and polysilicon. This layer is removed by SF_6 plasma etching. Buffered HF is then used to etch away the inter-poly layer and gate oxide layer to expose bulk silicon as shown in Fig. 6-7(b).

A 1-μm-thick film of Parylene is then deposited at room temperature after applying Parylene adhesion promoter (A-174). The next step is to create etching slots on Parylene for cavity etching. A 3-μm-thick photoresist is used for the oxygen plasma etching with oxygen pressure of 400 mTorr and power of 400 W. The Parylene plasma etching has loading effects with a non-uniform etching rate of 0.1~0.5 μm/min. In order to keep the etching openings of parylene diaphragm as small as possible for ease of sealing, 4 μm wide slots are opened and overlap with the edge of the sensor-bridge. This way, the actual etching slot has a width of about 2 μm. Smaller etching slots have less interference to the fluid flow and make the later on sealing process easier.

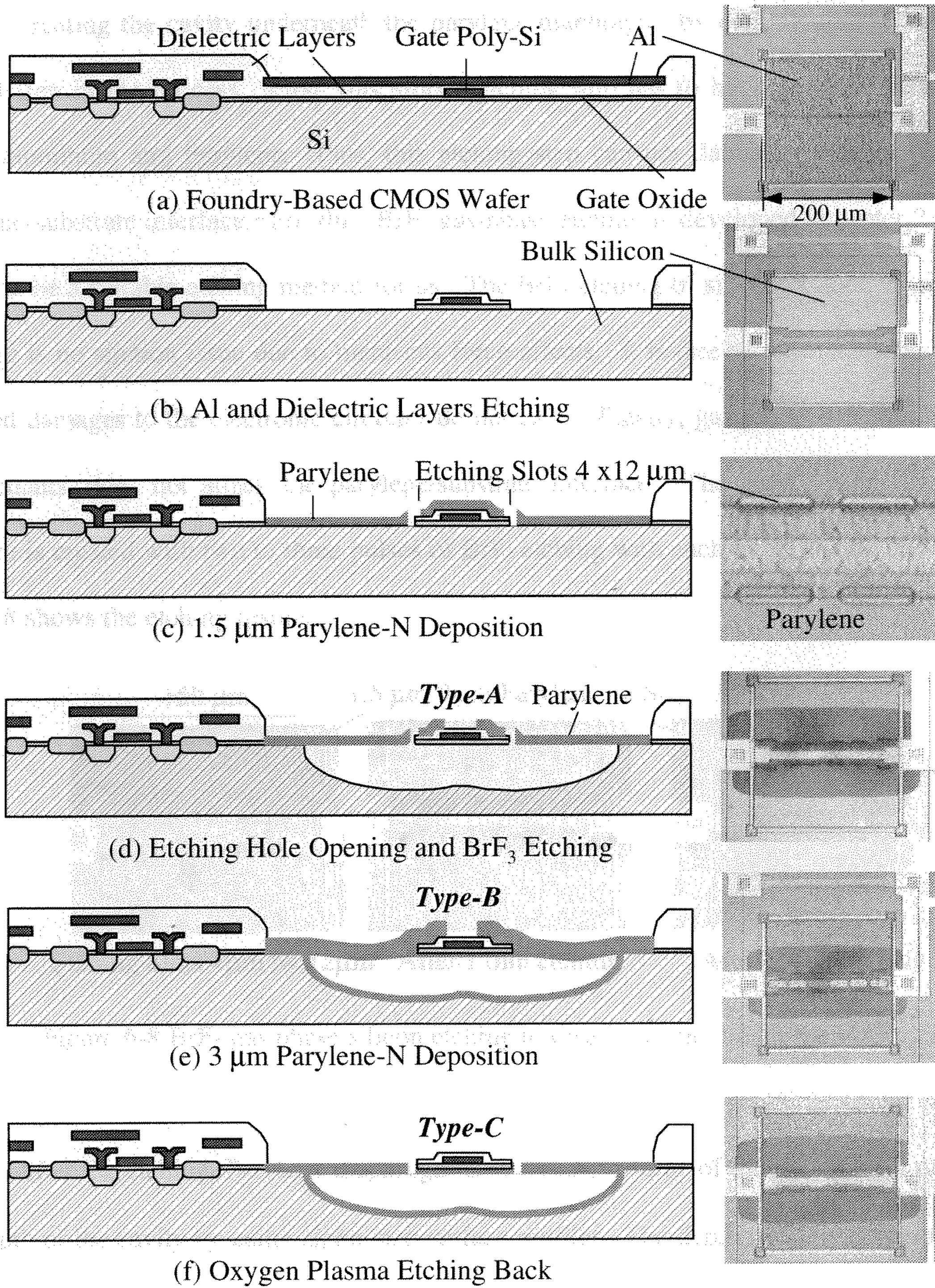


Figure 6-7 Major Post-CMOS processing steps and top views of the sensor area

Creating the cavity underneath the parylene diaphragm (by etching silicon away) is a crucial step in the process. First, this silicon-etching step has to have good selectivity over LTO, aluminum and Parylene. Plus, this etching step can not damage the integrity of the parylene-substrate interface. For this, BrF_3 gas-phase etching is developed 9chapter 2), and is found to be a suitable etching method for us. The BrF_3 etching of silicon is done in gas phase so there is no stiction issue due to meniscus force effects. It is free of plasma so the plasma-induced damages to the electronic circuitry do not exist. Finally, gas phase BrF_3, unlike most wet echants, does not attack the parylene/substrate interface. The cavity under the sensor element is created with two to three pulses of BrF_3 etching with each pulse lasting one minute. Fig. 6-8 shows the etching results.

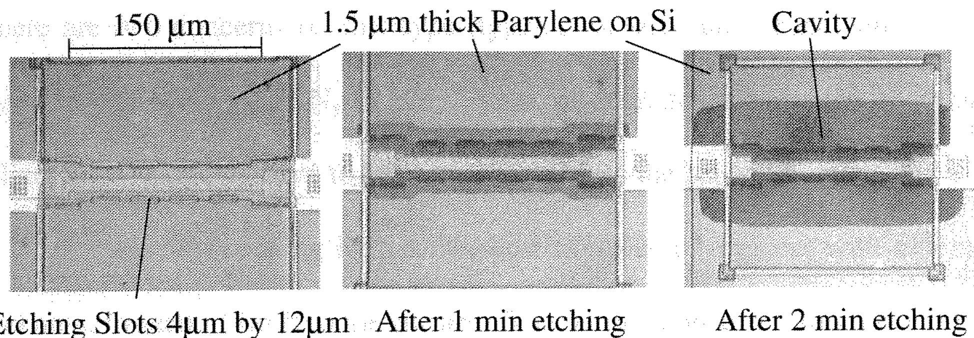


Figure 6-8 BrF_3 gas phase silicon etching to create a cavity under the sensor

After the etching, Parylene diaphragm is stripped off some of the sensors and measured the depth of the cavity by using alpha-step surface profiler. The depth range is between 30 μm to 40 μm as shown in Fig. 6-9.

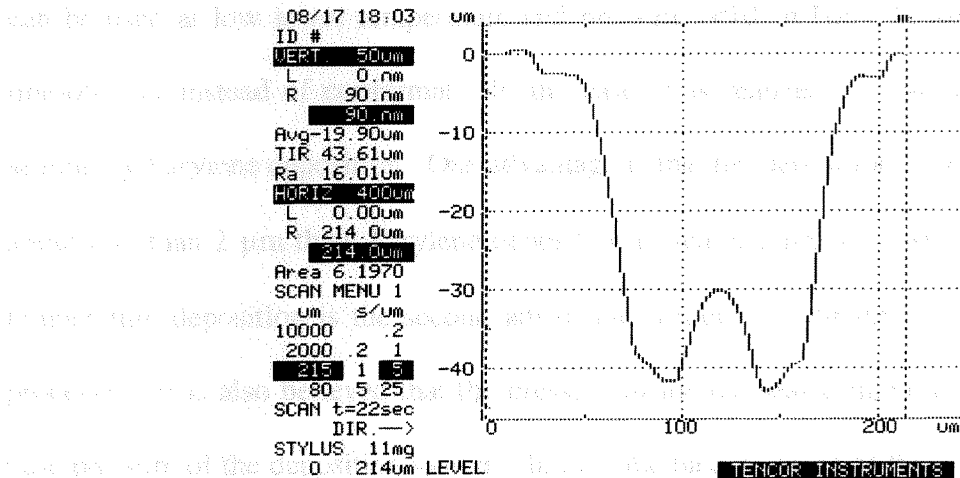


Figure 6-9 Profile of BrF_3 etched cavity, measured by alpha-step profiler

As shown in Fig. 6-7(d), a basic shear stress sensor structure has been achieved. However, there are two concerns on this type (type-A) of structure. First, since the thermal conductivity is less than 5% of Si_xN_y or polysilicon, in order to measure the heat dissipation rate to the fluid flow, windows have to be opened to expose the sensor element. However, the trade-off of such a window opening is that the sensor resides in a recess with a depth of the Parylene thickness, instead of flush to the surface. The second concern is that since it has an air cavity underneath the sensor element, the amount of heat loss through the "dead" air to the substrate is significant, which will be shown in detail in the thermal transfer experiment and analysis section. Therefore, the next step is to seal the etching slots to create a micro vacuum cavity.

Vacuum sealing of a micromachined cavity is an important process that has many MEMS application. Over the years many sealing techniques have been developed. For example, LPCVD S_xN_y, LTO, polysilicon deposition [15] can seal micro cavities with a deposition temperature above 400°C and pressure around 200 mTorr. Metal evaporation [16]

can be used at low lower temperature and pressure (<10^6 mTorr), however the deposition is line-of-sight instead of conformal. In the case, it is realized that the micro vacuum cavity sealing by Parylene deposition. One advantage is that the deposition is conformal, which takes about less than 2 μm thick Parylene deposition to seal a 2 μm wide slot. Furthermore, room temperature deposition is the second advantage, which is compatible with the subsequent of processes. It is also believed that the pressure inside the sealed micro cavity is much less the base pressure of the deposition system. In fact, the base pressure of the system after deposition is significantly less than the base-pressure (6 mTorr) before the deposition. The reason is that all the monomers are eventually deposited on the internal wall of the micro cavity of the system. Since a conventional rotary mechanical pump and a Baratron pressure gauge are used in the Parylene deposition system, the real vacuum pressure after deposition is not measurable but should be in the range of 0.1 mTorr to 1 mTorr.

In the process, 2 μm thick Parylene is deposited to seal the etching slots. In the mean time, about 0.5-1μm of Parylene is deposited on the backside of the sensor-bridge and internal wall of the micro cavity. Windows are then opened on top of the sensor-bridge again to expose the sensor. Shown in Fig. 6-7(e) is a type-B sensor with a vacuum cavity underneath. However, Type-B has 3.5 μm thick Parylene diaphragm over a vacuum-sealed cavity, and the sensing element resides inside a deeper recess (total Parylene thickness) than type-A. Nevertheless, the Parylene diaphragm is deformed and sagged down by more than 5 μm due the pressure difference across it. This overall structure is undesirable since it decreases the sensor sensitivity.

Finally, a plasma etch-back process is adopted to eliminate the recess and reduce the diaphragm thickness to a sub-micron level. A time controlled oxygen plasma etching is done

with 300 mTorr of oxygen pressure and 300 W of plasma power. The total etching time is 10 ~ 12 minutes with four times wafer rotation to eliminate the effects of non-uniformity of the Parylene film and plasma etching. During the etching, the sealed etching slot are reopened but with the opening size (<1μm wide) smaller than before the sealing (as shown in Fig. 6-10 SEM).

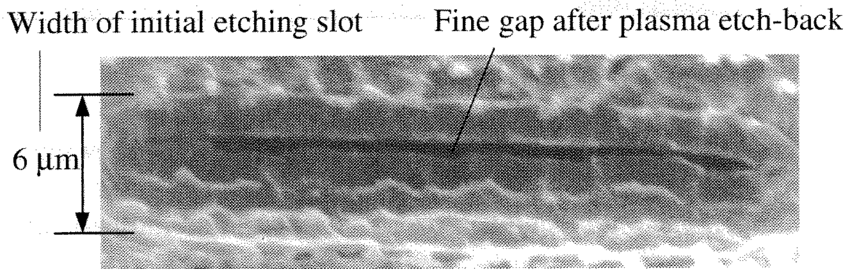


Figure 6-10 SEM of a etched-back slot on Parylene diaphragm

As a result, type-C sensor has an air-filled cavity that coated with thin layer of Parylene internally and a flat diaphragm of 0.7 μm on top.

6.4 Shear stress sensor testing and analysis

6.4.1 The thermal transfer testing and analysis

The sensitivity and power consumption of a hot film/wire shear stress sensor depend on the heat dissipation rates from the sensor to the ambient in several terms. Since the silicon substrate has a high thermal conductivity and a large thermal mass compared to the sensor material and size, it can be treated as a heat sink. In another words, we can always assume the silicon substrate has a constant temperature of Ts, which can be different from the fluid temperature in the main stream.

The total heat dissipation of a heated element includes thermal conduction, convection and radiation through the wire, the diaphragm, the air and the substrate. If the sensor

temperature is kept constant during the measurement, the heat dissipation rate is represented in the following terms as shown in Fig. 6-11.

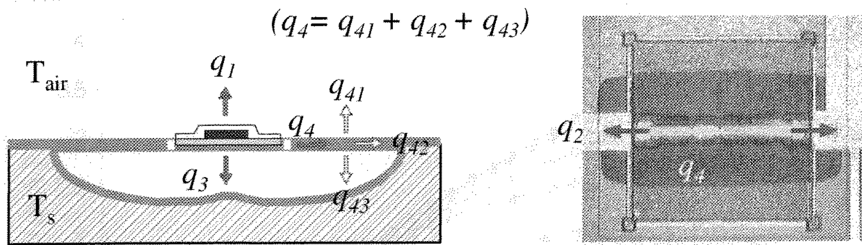


Figure 6-11 Heat transfer characteristics

(1) q_1: the direct convective heat transfer from the heated sensor element to the fluid flow to be measured, with the assumption of constant substrate temperature and negligible heat convection through the etching slot opening.

(2) q_2: the conductive heat transfer to the substrate from the metal leads and anchors of the sensor bridge.

(3) q_3: the direct convective heat transfer from the heated sensor element to air underneath. This then completely dissipates to the cavity wall, which has same temperature of the substrate.

(4) q_4: the conductive heat transfer from the sensor element to the Parylene diaphragm. This term can be separated to three parts: Convective heat loss from the diaphragm to the air (q_{41}, q_{43}) and the conductive loss from the diaphragm to the substrate (q_{42}). It can be assumed that q_4 is then completed dissipate to the air at both side of the diaphragm ($q_4 = q_{41} + q_{43}$).

To study the heat transfer characteristics experimentally, I-V curve measurements of a sensor resistor with and without the Parylene diaphragm have been conducted in still air and in vacuum (~30mTorr). Without a cavity underneath the sensor resistor, the I-V curve of the sensor is a straight line, which indicates that there is no resistance or temperature change with the changing sensor power consumption. On the other hand, with a cavity underneath the

sensor, the non-linearity of the I-V curves in Fig. 6-12 indicates the heating effects of the sensor.

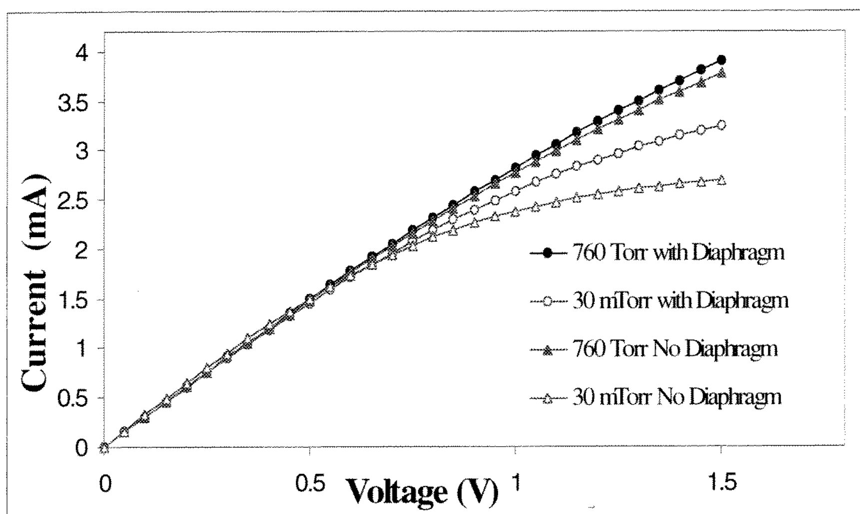


Figure 6-12 I-V curves of the sensor element in air and vacuum

Since the TCR of the sensor is a constant (~0.1%/°C), the I-V curves are converted to a series of plots of power consumption against sensor temperature, as shown in Fig. 6-13.

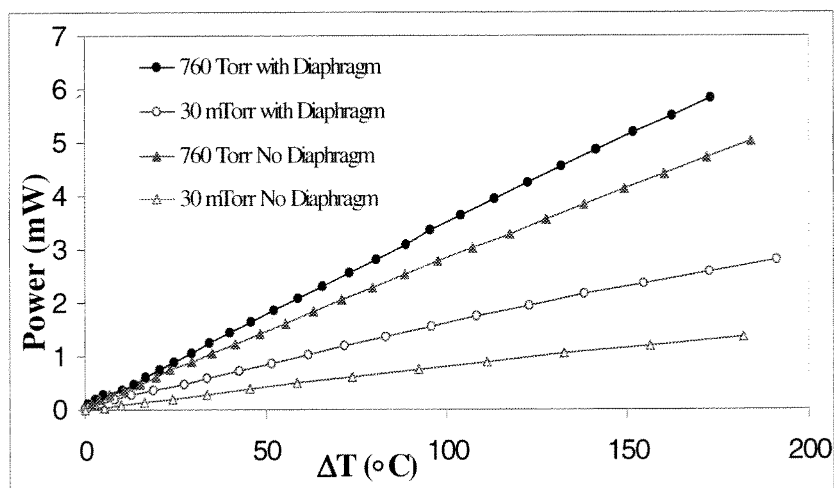


Figure 6-13 Power required to heat up the sensor element

The reciprocals of the slopes of these curves represent the thermal resistance R_{th}. The differences of the thermal resistance in the four cases reflect the contribution of heat losses from above four terms. In Fig. 6-12, the power consumption of various sensors for keeping

them at 120°C temperature in a static flow condition can be compared. These values are shown in table 6-2.

	Without diaphragm 30 mTorr	With diaphragm 30 mTorr	Without diaphragm 760 Torr	With diaphragm 760 Torr
Power	$P_1 = 0.81$ mW	$P_2 = 1.91$ mW	$P_3 = 3.36$ mW	P_4=4.16 mW

Table 6-2 Power consumption to keep sensors at 120°C in static airs with various pressures

The previous described q values can be related to the P values in Table 6-2.

$$q_2 = P_1 = 0.81mW\ (20\%) \tag{6.3}$$

$$q_{42} = P_2 - P_1 = 1.1\ mW\ (25\%) \tag{6.4}$$

$$(q_1 + q_{41}) + (q_3 + q_{43}) = P_4 - P_2 = 2.25\ mW\,(55\%) \tag{6.5}$$

$$q_4 = q_{41} + q_{43} = P_4 - P_3 = 0.8\ mW\,(20\%) \tag{6.6}$$

$$q_1 + q_3 = P_4 - P_3 = 2.25 - 0.8 = 1.45\ mW\ (35\%) \tag{6.7}$$

It is obvious that the sensitivity of a shear stress sensor depends on the value of $(q_1+q_{41})/(i^2R)$. From the tests, it is not able to extract the value of (q_1+q_{41}) from above calculations. However, we realize that there is a 20% conductive loss through the two anchors, 25% conductive loss through the membrane to the substrate, 20% convective loss through the diaphragm to the air, and 35% direct convective loss to the air. Notice, here the convective losses to the air include both sides of the diaphragm. These values are very useful in the optimization of sensor structure designs.

6.4.2 Constant temperature operation mode and its Frequency response:

The sensors in this design are biased in a constant temperature mode. As governed by equation (6.8), if the sensor temperature is kept at a constant value that higher than room temperature, we can also achieve a constant resistance that higher than its value at room temperature.

$$R_{sensor} = R_o + \alpha(T - T_o) \tag{6.8}$$

where α is known as the temperature coefficient of resistance (TCR). Note that this equation assumes a linear dependence between the temperature and the resistance. In practice, higher order terms have to be taken into account [7]. Using Ohm's law we can then relate the resistance changes to the power change (equation 6.9), which measures the heat loss rate.

$$P_{sensor} = I_{sensor} R_{sensor}^2 \tag{6.9}$$

The constant temperature circuit has the sensor as one arm in a Wheatstone bridge configuration (Fig. 6-14). The operational amplifier (op-amp) output terminal is connected to the top of the bridge, which converts the output voltage to a current. The current passes through both sides of the bridge. The op-amp (open-loop gain ~500, gain-bandwidth product ~5 MHz) is used to force the two sides of the bridge to be balanced through the use of feedback at the top of the bridge.

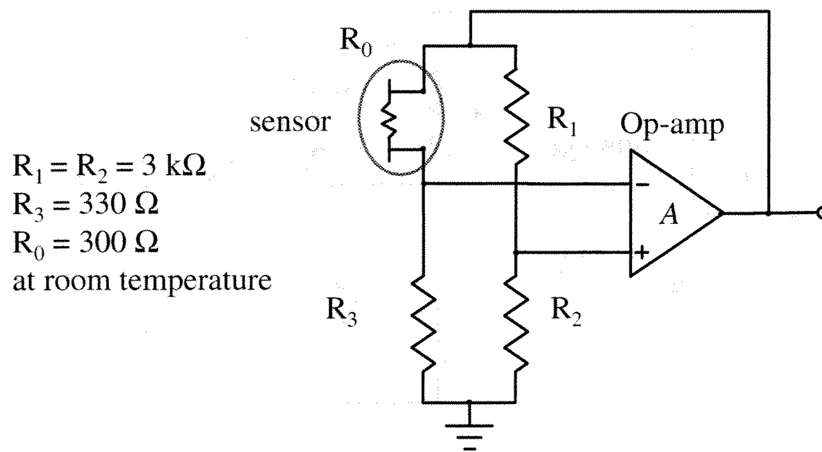


Figure 6-14 Constant temperature biasing circuit

As in Fig. 6-14, in a constant temperature mode, the sensor temperature is preset to a value by the three bridge resistors, R_1, R_2, and R_3. Since these three resistors are in direct contact with the substrate, they will not be heated up by electrical current, if we assume the substrate is an ideal heat sink. When the circuit is off, the sensor has a cold resistance of R_0, and the ratio of R_3 over R_{sensor} is 1.1. When the circuit operates, the ratio of R_3 over R_{sensor} is forced to be balanced with the ratio of R_2 over R_1, by heating up the sensor. Therefore, the value of R_3 is designed to be equals to the desired operating resistance of the sensor. The ratio between the desired operating resistance and the cold resistance of the sensor is called the over heat ratio, which is 1.1 in this design. Since the TCR of the polysilicon resistor is 0.1%/°C, the sensor temperature is kept at 120°C when the circuit operates as design.

According to [4], the frequency response of the sensor with the CT circuit can be measured by feeding a square wave into the circuit at point A as shown in Fig. 6-15.

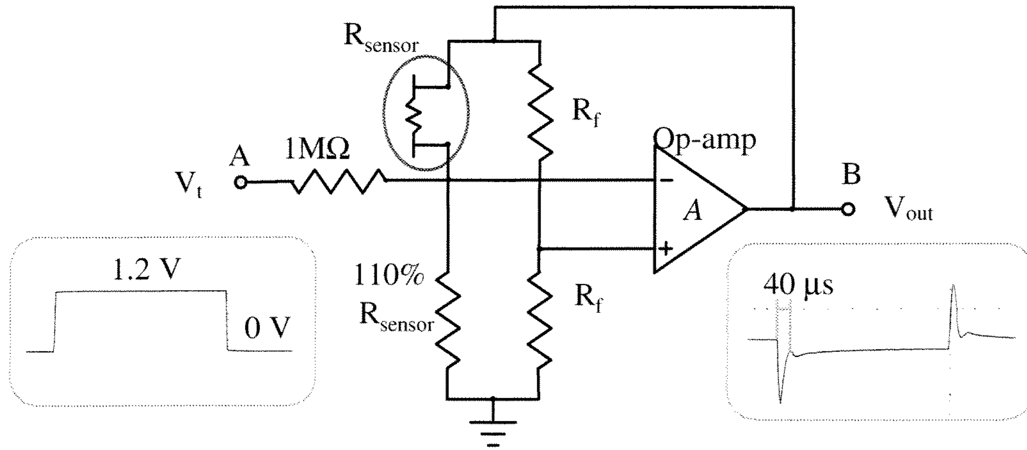


Figure 6-15 Frequency response of the sensor and its CT biasing circuit

At point B of Fig. 6-15, the measured peak width of the response curve is τ = 40 μs. The cutoff frequency of the system is approximately 19 kHz, which is calculated by equation 7.10 [4].

$$f_{cutoff} = \frac{1}{1.3\tau} = 19kHz \tag{6.10}$$

6.4.3 Wind tunnel tests

The fabricated sensors with their integrated CT circuits are calibrated in a wind tunnel with fully developed channel flow. The time-averaged voltage outputs in steady-state flow condition are calibrated against known wall shear stress levels, which are obtained from the centerline velocity using the following relationship [3],

$$\tau = 0.00826 R_e^{-0.178} U_\infty^2 \rho \tag{6.11}$$

Where $R_e = (U_\infty d / v)$ is the Reynolds number, d is the half height of the windtunnel, v is the kinematic viscosity, ρ is the density of air and U_∞ is the free stream mean velocity (5-25 m/s).

The sensors are packaged on a PC board with a recess in the center so that the chip can be flush-mounted into the wall of the windtunnel. A 6V DC is applied to the integrated chip. The output voltage from the on-chip CT circuit is monitored by a 12-bit data acquisition system. In order to calibrate the on-chip sensors more flexibly, an off-chip 2-stage amplifier to connect to the sensors in CT mode is also used.

6.4.4 Temperature compensation of the wind tunnel tests

The shear-stress sensor is inherently sensitive to the airflow and the substrate temperature variations. When the shear stress value is ramped up and down by changing the airflow velocity in a wind tunnel, we notice non-repeatable sensor output voltages with known shear stress. Fig. 6-17 shows the plot of sensor output voltage against the shear stress without considering temperature compensation. However, the airflow and substrate temperature variations during the measurement are monitored. A thermocouple temperature sensor suspended in the windtunnel is used to measure airflow temperature, while the resistance of a polysilicon resistor (TCR = 0.1%/^{o}C) on the substrate is measured by a precision ohmmeter to provide the temperature variation of the substrate. The two temperature variations against the shear stress are plotted in Fig. 6-18. It is obvious that temperature measurement and compensation are crucial to the shear stress measurements.

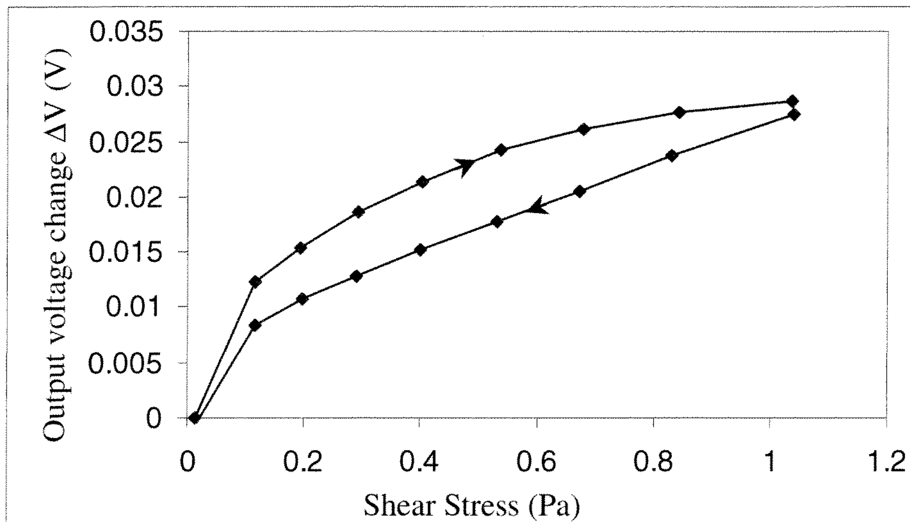


Figure 6- 16 Output voltage change vs. shear stress without temperature compensation

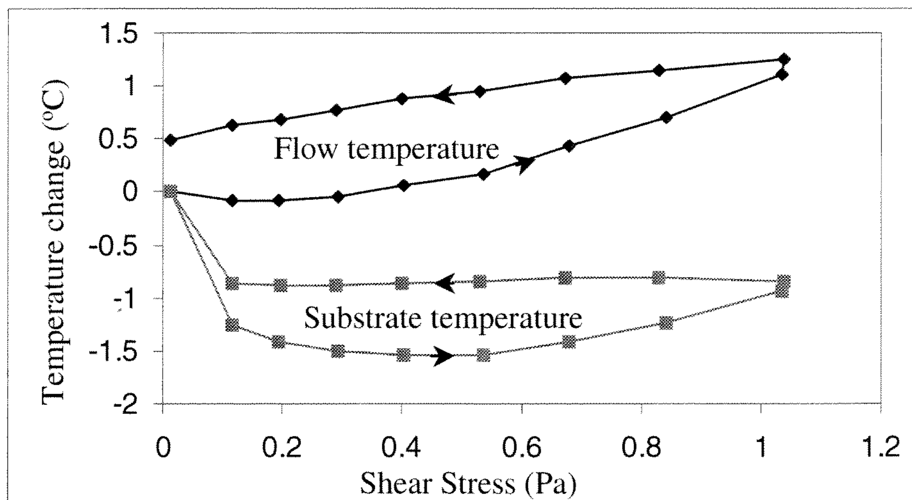


Figure 6-17 Temperature variation of substrate and air flow

From Reference [7, pp. 69], the temperature sensitivity for the on-chip Wheatstone bridge and CT circuit is shown to be of the form

$$\frac{\partial V}{\partial T} = \alpha_R V_0 \tag{6.12}$$

where α_R is the TCR (0.1%/°C for the polysilicon resistor). However, the question is what temperature should be used to compensate the results of shear stress measurement. Both temperature compensation are done independently and plotted the compensated curves in Fig. 6-18 and Fig. 6-19. It is obvious that the substrate temperature compensated data is much more repeatable. Therefore the temperature variations at the substrate are believe to have more influence on the shear stress measurement than in the airflow.

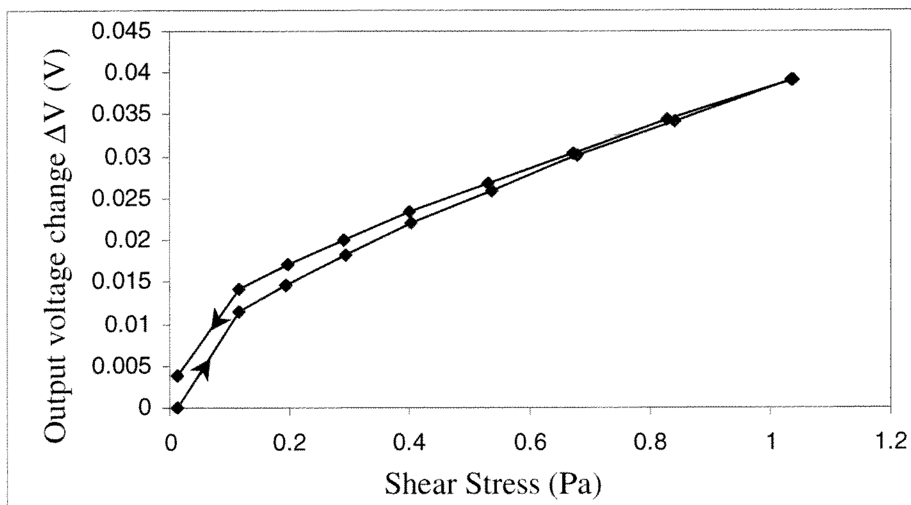


Figure 6-18 Shear stress measurement with flow temperature compensation

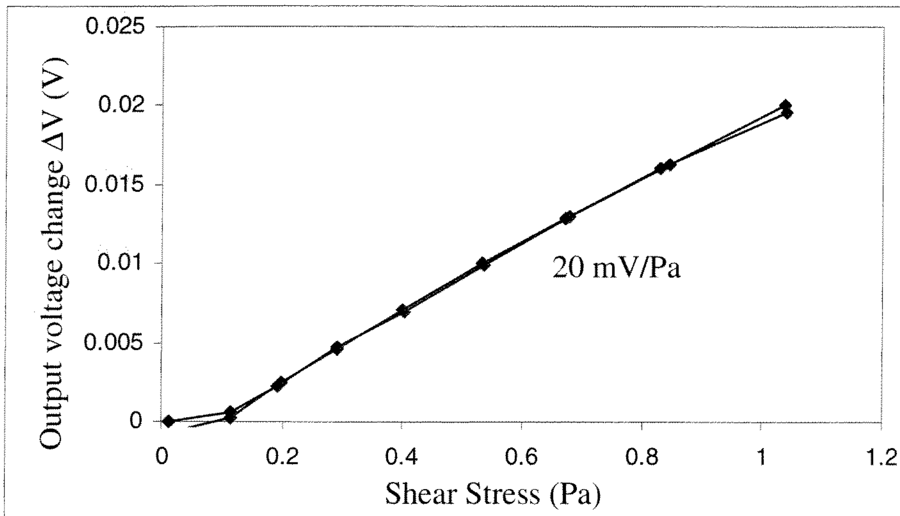


Figure 6-19 Shear stress measurement with substrate temperature compensation

As shown in Fig. 6-19, when shear stress is larger than 0.1 Pa, we have two straight lines that almost overlap each other. The wind tunnel test also shows a 20 mV/Pa sensitivity of shear stress measurement for this particular sensor.

6.4.5 Discussion

The operation principle of this shear stress measuring method is to relate the power (*P*) required maintaining the sensor at a constant temperature to the wall shear stress (τ). According to classical heat transfer theory [4],

$$P - P_0 \propto \tau^{1/3} \tag{6.13}$$

where $P_0 = P|_{\tau=0}$. Since the power P is proportional to the square of the output voltage *V*, and if $\Delta V << V_o$, which is true in most cases, then the following linear relationship have been reported [7],

$$\Delta V \propto \tau^{1/3} \tag{6.14}$$

In Fig. 6-20, we plot the output voltage change of one of the sensors against the one-third power of shear stress.

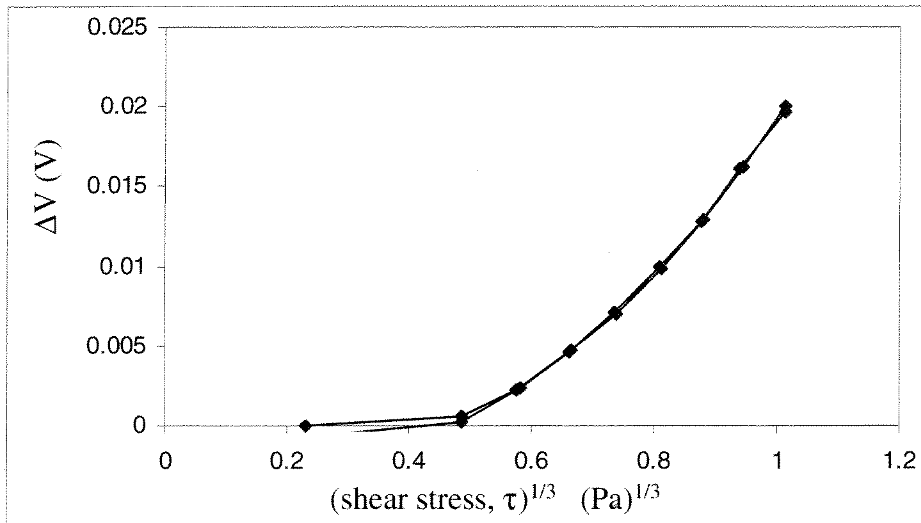


Figure 6-20 Sensor output voltage change vs. (shear stress)$^{1/3}$

Clearly, we see a non-linear relationship, which contains considerable deviation from the above theory. This interesting phenomenon was first studied by Lin *et al.* at Caltech, who reported a new MEMS shear stress theory [17].

6.5 Summary

A fully integrated shear-stress sensor has been developed using a post-IC process that is added to 4-inch foundry-processed CMOS wafers. The shear-stress sensor uses a gate-polysilicon hot-wire as the sensing element that sits on a freestanding Parylene diaphragm suspended over a cavity. A special Parylene vacuum sealing and etch-back process is used to achieve better thermal isolation and overall sensitivity. The integrated shear-stress sensor is made of a wheatstone bridge (sensor as one arm) with an amplifier connected into a constant-temperature mode. The sensor is designed to have an overheat ratio of 10%. The calibration of the shear stress sensor is conducted in a windtunnel and the results show a sensitivity of 20~30 mV/Pa and a measured bandwidth of 18 kHz. The Post-CMOS technology developed in this work may be used in many other MEMS integration applications.

6.6 References

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