Appendix A

Description of Fabrication Processes

The detailed description of each fabrication process developed in the thesis is presented in this appendix.

A.1 Micromachined Hot-Wire Anemometer

1. Start with 4" (100) Si wafers with 70 μm epitaxial layer and 8 μm heavily boron-doped layer.
2. LPCVD low stress silicon nitride.
   2.1 Standard piranha wafer cleaning.
   2.2 Silicon nitride deposition: 835 ^{o}C, DCS 65 sccm, NH3 16 sccm, 30 min.. Target: 0.2 μm.
3. LPCVD LTO.
   3.1 Standard piranha wafer cleaning (omitted if immediately follow step #2).
   3.2 LTO deposition: 450 ^{o}C, SiH_4 42.8 sccm, O_2 62 sccm, 200 min.. Target thickness: 2 μm.
4. LPCVD polysilicon.
   4.1 Standard piranha wafer cleaning (omitted if immediately follow step #3).
   4.2 Polysilicon deposition: 560 ^{o}C, SiH_4 80 sccm, 170 min.. Target thickness: 0.55 μm.
5. Dope and anneal polysilicon.
   5.1 Boron ion implantation: energy 80 keV, dose 1×10^{16} cm^{-2}.
   5.2 Standard piranha wafer cleaning.

5.3 Annealing: 1050 ^{o}C, 1 hr..

6. Pattern polysilicon.
   6.1 Standard photolithography.
   6.2 RIE etching: SF_6 65 sccm, O_2 15 sccm, 600 W, 4 min. for both front and back side.
   6.3 Remove photoresist with acetone followed by plasma ashing.
7. Deposit metals.
   7.1 Standard piranha wafer cleaning.
   7.2 Evaporate 1 μm Cr/Au.
8. Pattern Cr/Au.
   8.1 Standard photolithography.
   8.2 Etch Au with gold etchant.
   8.3 Etch Cr with chrome etchant.
9. LPCVD LTO.
   9.1 TCE wafer cleaning.
   9.2 LTO deposition: 450 ^{o}C, SiH_4 42.8 sccm, O_2 62 sccm, 400 min.. Target thickness: 4 μm.
10. Pattern front side.
   10.1 Standard photolithography.
   10.2 Etch LTO with BHF: 0.2 μm/min.
   10.3 Plasma-etch nitride (from step #3): CF_4/O_2, 200 mT, 200 W, 4 min.. Target etching depth: 0.4 μm.
   10.4 Etch thermal oxide (from step #2) with BHF: 80 nm/min..
   10.5 Remove photoresist with acetone followed by plasma ashing.
11. Pattern backside.
   11.1 Standard piranha wafer cleaning.
   11.2 Standard photolithography on backside.
   11.3 Plasma-etch nitride (from step #3): CF_4/O_2, 200 mT, 200 W, 4 min.. Target etching depth: 0.4 μm.

11.4 Etch thermal oxide (from step #2) with BHF: 80 nm/min..

11.5 Remove photoresist with acetone followed by plasma ashing.

12. EDP etching.

12.1 Standard piranha wafer cleaning with 5% HF dip.

12.2 EDP etching: 95 ^{o}C, 10 hrs.

13. Boron layer, nitride and LTO removal.

13.1 TCE wafer cleaning.

13.2 RIE etching on wafer backside: SF_6 65 sccm, O_2 15 sccm, 600 W, 16 min..

13.3 BHF etching: 40 min..

A.2 Micromachined Shear Stress Sensor

1. Start with 4" single-side polished Si wafers.
2. LPCVD low stress nitride deposition.
   2.1 Standard piranha wafer cleaning.
   2.2 Silicon nitride deposition: 835 ^{o}C, DCS 65 sccm, NH3 16 sccm, 70 min.. Target: 0.5 μm.
3. Pattern nitride.
   3.1 Standard photolithography.
   3.2 Plasma etching: CF_4/O_2, 200 mT, 200 W, 6 min.. Target etching depth: 0.9 μm.
   3.3 Remove photoresist with acetone followed by plasma ashing.
4. Local oxidation (LOCOS).
   4.1 Standard piranha wafer cleaning.
   4.2 Thermal oxidation: 1050 ^{o}C, O_2 0.5 liter/min., DI water 10 drops/min., 12 hrs.. Target thickness: 2.1 μm.
   4.3 Planarization: BHF etches back.
5. LPCVD PSG.
   5.1 Standard piranha wafer cleaning.

5.2 PSG deposition: 450 ^{o}C, SiH_4 20 sccm, O_2 62 sccm, PH_3 10 sccm, 60 min.. Target thickness: 0.4 μm.

5.3 Anneal PSG: 950 ^{o}C, 30 min..

6. Pattern PSG.

6.1 Standard photolithography.

6.2 BHF etch PSG: 2.5 min..

6.3 Remove photoresist with acetone followed by plasma ashing.

7. Anneal PSG.

7.1 Standard piranha wafer cleaning.

7.2 Anneal PSG: 1050 ^{o}C, 30 min..

8. LPCVD low stress silicon nitride.

8.1 Standard piranha wafer cleaning (omitted if immediately follow step #8).

8.2 Nitride deposition: 835 ^{o}C, DCS 65 sccm, NH3 16 sccm, 180 min.. Target: 1.3 μm.

9. Pattern nitride to open etch holes.

9.1 Standard photolithography.

9.2 RIE etching: SF_6 65 sccm, O_2 15 sccm, 600 W, 20 min.. Target etching depth: 1.5 μm.

9.3 Remove photoresist with acetone followed by plasma ashing.

10. Sacrificial layer etching.

10.1 Standard piranha wafer cleaning.

10.2 High concentrion HF (49%) etches PSG and thermal oxide: 25 - 30 min..

10.3 DI water rinse: 20 min.. Spin dry.

11. Seal cavities in vacuum.

11.1 Standard piranha wafer cleaning.

11.2 Bake at 600 ^{o}C for 30 min..

11.3 LPCVD LTO deposition: 450 ^{o}C, SiH_4 42.8 sccm, O_2 62 sccm.Target thickness: 1 μm.

11.4 LPCVD low stress nitride deposition: 835 ^{o}C, DCS 65 sccm, NH3 16 sccm, 70 min.. Target: 0.5 μm.

12. Pattern sealing materials.
    12.1 Standard photolithography.
    12.2 Plasma-etch nitride: CF_4/O_2, 200 mT, 200 W, 6 min.. Target etching depth: 0.6 μm.
    12.3 BHF-etch LTO: 6 min..
    12.4 Remove photoresist with acetone followed by plasma ashing.
13. LPCVD polysilicon.
    13.1 Standard piranha wafer cleaning.
    13.2 Polysilicon deposition: 560 ^{o}C, SiH_4 80 sccm, 170 min.. Target thickness: 0.55 μm.
14. Dope and anneal polysilicon.
    14.1 Boron ion implantation: energy 80 keV, dose 1×10^{16} cm^{-2}.
    14.2 Standard piranha wafer cleaning.
    14.3 Annealing: 1050 ^{o}C, 1 hr..
15. Pattern polysilicon.
    15.1 Standard photolithography.
    15.2 RIE etching: SF_6 65 sccm, O_2 15 sccm, 600 W, 4 min..
    15.3 Remove photoresist with acetone followed by plasma ashing.
16. LPCVD low stress silicon nitride deposition.
    16.1 Standard piranha wafer cleaning.
    16.2 Nitride deposition: 835 ^{o}C, DCS 65 sccm, NH3 16 sccm, 30 min.. Target: 0.2 μm.

A.3 M^3 System

1. Start with p-type (100) Si wafer with resistivity of 8-12 Ω·cm.
2. Grow 0.1 μm SiO_2.

3. Define N well {CWN}.
4. Implant phosphorus with dose of $5\times10^{12}/cm^2$ at energy of 150 keV.
5. Drive-in well to 3.4 μm.
6. Grow 30nm SiO_2 (pad ox)
7. Deposit 0.1 μm silicon nitride.
8. Pattern silicon nitride to define active area (PR1) [Active] and LOCOS {CAA}.
9. Define p-field (PR2).
10. Implant boron with dose of $1.5\times10^{13}/cm^2$ at energy of 70 keV.
11. Grow LOCOS 0.65-0.7 μm.
12. Remove silicon nitride (from step #7).
13. Remove oxide (from 6 - pad ox).
14. Grow sac. oxide 20 nm.
15. Implant boron $1.7\times10^{12}/cm^2$ at energy of 30 keV.
16. Remove sac. oxide (from step #14).
17. Grow gate oxide 30nm.
18. Deposit 0.450 μm gate polysilicon [Poly].
19. Pattern gate polysilicon {CPG}.
20. Deposit cap. oxide 80 nm.
21. Deposit 0.45 μm cap. polysilicon [Poly2].
22. Pattern cap. polysilicon {CEL}.
23. Define N+ source and drain.
24. Implant arsenic with dose of $5\times10^{15}/cm^2$ at energy of 160 keV.
25. Anneal N+ source and drain.
26. Deposit 0.7 μm PSG.

*** Back to Caltech at this point ***

27. Pattern PSG (from step #26) [fberk_psg] {FEP}.

28. Deposit 0.4 μm PSG at 450 ^{o}C (SiH_4 20 sccm, O_2 62 sccm, PH_3 10 sccm).
29. Deposit 1 μm polysilicon at 620 ^{o}C (SiH_4 80 sccm, 140 A/min.).
30. Pattern polysilicon [tpoly] {TNP}.
31. Pattern PSG (from step #28) [fcaltech_psg] {NG}.
32. Deposit 1.3 μm low stress silicon nitride at 835 ^{o}C (DCS 64.7 sccm, NH3 15.6 sccm).
33. Pattern nitride to open etch holes [fhole_etch] {NS}.
34. Sacrificial layer (PSG and oxide) etching with 49% HF.
35. Deposit 1 μm LTO at 450 ^{o}C (SiH_4: 42.8, O2: 62 sccm).
36. Deposit 0.4 μm low stress silicon nitride at 835 ^{o}C.
37. Pattern silicon nitride [fseal_pad_nitride].
38. Etch LTO (from step #35).
39. Deposit 0.55 μm polysilicon at 560 ^{o}C (SH4 80sccm)
40. Implant boron on polysilicon with dose of 1×10^{16} cm-2 at energy of 80 keV;
41. Anneal polysilicon at 900 ^{o}C for 1 hour.
42. Pattern polysilicon [fpoly].
43. Deposit 0.2 μm low stress silicon nitride.
44. Pattern silicon nitride [fcontact] {NC}.
45. Pattern silicon nitride (from step #32) [fnitride] {FN}.
46. Define contact holes for electronics.
47. Etch contact holes (Berkeley).
48. Sputter 0.6 μm aluminum (Berkeley).
49. Define aluminum (Caltech).
50. Etch aluminum (Lam/plasma) [Metal1] {CMF} (Berkeley).
51. Sintering (Berkeley).
52. Pattern aluminum (wet etch) [fberk_metal] {NM}.
53. Pattern silicon nitride (from step #32) [tnitride_etch] {TNC}.
54. Deposit 2 μm LTO.

55. Pattern LTO [tlto_etch] {TNG}.
56. Evaporate 0.4 μm Cr/Au.
57. Pattern Cr/Au [tmetal1+] {TNM}.
58. Deposit o.5 μm LTO.
59. Pattern LTO [tlto2_etch] {TLYRL} <add to over sensor like LTO1>
60. Evaporate 0.4 μm Cr/Au.
61. Pattern Cr/Au [tmetal2+] {TNMS}.
62. Evaporate Cr/Cu seed layer.
63. Pattern seed layer [tplating] {TNS}.
64. Plate NiFe.
65. Protect NiFe [tcr_protect] {TLYRR}.
66. Remove seed layer.
67. Release actuators by TMAH and BrF_3 etching.

A.4 Flexible Shear Stress Sensor Array

1. Start with 4” double-side polished (100) Si wafers.
2. Make double-side alignment marks.
   2.1 Spin-coat and soft-bake 3 μm photoresist on both sides of wafers.
   2.2 Mount wafers on the double-side alignment jig. Flush-expose each side of a wafer under UV light.
   2.3 Develop photoresist.
   2.4 RIE etching: SF_6 65 sccm, O_2 15 sccm, 600 W, 15 min. for each side.
   2.5 Remove photoresist with acetone followed by plasma ashing.
3. LPCVD low stress nitride deposition.
   3.1 Standard piranha wafer cleaning.
   3.2 Silicon nitride deposition: 835 ^{o}C, DCS 64.7 sccm, NH3 15.6 sccm, 70 min.. Target: 0.5 μm.
4. Pattern nitride.

4.1 Standard photolithography.

4.2 Plasma etching: CF_4/O_2, 200 mT, 200 W, 6 min.. Target etching depth: 0.9 μm.

4.3 Remove photoresist with acetone followed by plasma ashing.

5. Local oxidation (LOCOS).

5.1 Standard piranha wafer cleaning.

5.2 Thermal oxidation: 1050 ^oC, O_2 0.5 liter/min., DI water 10 drops/min., 12 hrs.. Target thickness: 2.1 μm.

5.3 Planarization: BHF etches back.

6. LPCVD PSG.

6.1 Standard piranha wafer cleaning.

6.2 PSG deposition: 450 ^oC, SiH_4 20 sccm, O_2 62 sccm, PH_3 10 sccm, 60 min.. Target thickness: 0.4 μm.

6.3 Anneal PSG: 950 ^oC, 30 min..

7. Pattern PSG.

7.1 Standard photolithography.

7.2 BHF etch PSG: 2.5 min..

7.3 Remove photoresist with acetone followed by plasma ashing.

8. Anneal PSG.

8.1 Standard piranha wafer cleaning.

8.2 Anneal PSG: 1050 ^oC, 30 min..

9. LPCVD low stress silicon nitride.

9.1 Standard piranha wafer cleaning (omitted if immediately follow step #8).

9.2 Nitride deposition: 835 ^oC, DCS 64.7 sccm, NH3 15.6 sccm, 180 min.. Target: 1.3 μm.

10. Pattern nitride to open etch holes.

10.1 Standard photolithography.

10.2 RIE etching: SF_6 65 sccm, O_2 15 sccm, 600 W, 20 min.. Target etching depth: 1.5 μm.

10.3 Remove photoresist with acetone followed by plasma ashing.

11. Sacrificial layer etching.

11.1 Standard piranha wafer cleaning.

11.2 High concentrion HF (49%) etches PSG and thermal oxide: 25 - 30 min..

11.3 DI water rinse: 20 min.. Spin dry.

12. Seal cavities in vacuum.

12.1 Standard piranha wafer cleaning.

12.2 Bake at 600 ^{o}C for 30 min..

12.3 LPCVD LTO deposition: SiH_4 42.8 sccm, O_2 62 sccm. Target thickness: 1 μm.

12.4 LPCVD low stress nitride deposition: 835 ^{o}C, DCS 64.7 sccm, NH3 15.6 sccm, 70 min.. Target: 0.5 μm.

13. Pattern sealing materials.

13.1 Standard photolithography.

13.2 Plasma-etch nitride: CF_4/O_2, 200 mT, 200 W, 6 min.. Target etching depth: 0.6 μm.

13.3 BHF-etch LTO: 6 min..

13.4 Remove photoresist with acetone followed by plasma ashing.

14. LPCVD polysilicon.

14.1 Standard piranha wafer cleaning.

14.2 Polysilicon deposition: 560 ^{o}C, SiH_4 80 sccm, 170 min.. Target thickness: 0.55 μm.

15. Dope and anneal polysilicon.

15.1 Boron ion implantation: energy 80 keV, dose 1×1016 cm^{-2}.

15.2 Annealing: 1050 ^{o}C, 1 hr..

16. Pattern polysilicon.

16.1 Standard photolithography.

16.2 RIE etching: SF_6 65 sccm, O_2 15 sccm, 600 W, 4 min. for both front and back side.

16.3 Remove photoresist with acetone followed by plasma ashing.

17. LPCVD low stress silicon nitride deposition.
    17.1 Standard piranha wafer cleaning.
    17.2 Nitride deposition: 835 ^{o}C, DCS 64.7 sccm, NH3 15.6 sccm, 30 min.. Target: 0.2 μm.
18. LPCVD LTO and low stress silicon nitride.
    18.1 Standard piranha wafer cleaning (omitted if immediately follow step #17).
    18.2 LTO deposition: SiH_4 42.8 sccm, O_2 62 sccm. Target thickness: 1 μm.
    18.3 Nitride deposition: 835 ^{o}C, DCS 64.7 sccm, NH3 15.6 sccm, 100 min.. Target: 0.7 μm.
19. Pattern backside.
    19.1 Plasma-etch nitride: CF_4/O_2, 200 mT, 200 W, 9 min.. Target etching depth: 0.9 μm.
    19.2 BHF-etch LTO: 6 min..
    19.3 Standard photolithography (6 μm photoresist).
    19.4 RIE-etch nitride: SF_6 65 sccm, O_2 15 sccm, 600 W, 14 min.. Target etching depth: 0.9 μm.
    19.5 BHF-etch LTO: 6 min..
    19.6 RIE-etch nitride: SF_6 65 sccm, O_2 15 sccm, 600 W, 30 min.. Target etching depth: 1.9 μm.
    19.7 Remove photoresist with acetone followed by plasma ashing.
20. KOH etching.
    20.1 Standard piranha wafer cleaning with 5% HF dip.
    20.2 KOH etching: 58 ^{o}C, 20 hrs. Monitor remaining thickness closely after 16 hr. etching. Stop when it is 80 μm.
21. Remove nitride and LTO on the front side.
    21.1 Standard piranha wafer cleaning.
    21.2 Plasma-etch nitride: 9 min..

21.3 BHF-etch LTO: 6 min..

22. Evaporate aluminum.

22.1 Standard piranha wafer cleaning.

22.2 Evaporate 0.5 μm pure aluminum.

23. Pattern aluminum.

23.1 Standard photolithography.

23.2 Etch aluminum with aluminum etchant: 35 ^{o}C, 2 min..

23.3 Remove photoresist with acetone followed by plasma ashing.

24. Polyimide processing

24.1 TCE wafer cleaning.

24.2 Spin diluted VM-651 polyimide adhesion promoter water solution (0.5% - 1%) at 5 krpm/min..

24.3 Bake at 130 ^{o}C for 10 min..

24.4 Spin-coat polyimide PI-2808 at 4 krpm/min..

24.5 Bake at 130 ^{o}C for 15 min..

24.6 Standard photolithography. Polyimide etched during developing.

24.7 Remove photoresist by butyl acetate.

24.8 Cure polyimide: Ramp up from room temperature to 200 ^{o}C at a rate less than 4 ^{o}C/min.; Stay at 200 ^{o}C in air for 30 min.; ramp up to 350 ^{o}C at a rate less than 2.5 ^{o}C/min.; Stay at 350 ^{o}C with 10 liter/min. nitrogen purging for 1 hr.; Ramp down to room temperature at a rate less than 3 ^{o}C/min..

25. Open contact holes.

25.1 TCE wafer cleaning.

25.2 Standard photolithography.

25.3 RIE-etch nitride: SF_6 65 sccm, O_2 15 sccm, 600 W, 4 min.. Monitor closely.

25.4 Remove photoresist with acetone.

26. Metallization.

26.1 TCE wafer cleaning.

26.2 Evaporate 2.5 μm aluminum.

26.3 Standard photolithography.

26.4 Etch aluminum with aluminum etchant: 35 ^{o}C, 6 min..

26.5 Remove photoresist with acetone.

26.6 TCE wafer cleaning.

26.7 Evaporate 1 μm aluminum.

26.8 Standard photolithography.

26.9 Etch aluminum with aluminum etchant: 35 ^{o}C, 3.5 min..

26.10 Remove photoresist with acetone.

27. Polyimide processing (repeat step #24).

28. Form aluminum mask on backside.

28.1 TCE wafer cleaning.

28.2 Evaporate 0.5 μm pure aluminum on backside.

28.3 Standard photolithography (focus on Si diaphragm).

28.4 Etch aluminum with aluminum etchant: 35 ^{o}C, 2 min..

28.5 Remove photoresist with acetone.

29. Form Si islands.

29.1 TCE wafer cleaning.

29.2 RIE etching: SF_6 65 sccm, O_2 15 sccm, 600 W, 240 min.. Target etching depth: 80 μm. Monitor closed after 120 min. etching.

30. Strip aluminum on backside.

30.1 Spin-coat and bake 6 μm photoreist on front side.

30.2 Etch aluminum with aluminum etchant: 35 ^{o}C, 2 min..

31. Polyimide processing on backside (repeat steps #24.1-24.5 and #24.8, spin speed 2.0 krpm).

32. Cut finished skins from Si wafer frame using a razor blade.