

# Efficient Precise Computation with Noisy Components: Extrapolating From an Electronic Cochlea to the Brain

Thesis by  
Rahul Sarpeshkar

In Partial Fulfillment of the Requirements  
for the Degree of  
Doctor of Philosophy



California Institute of Technology  
Pasadena, California

1997

(Submitted April 3, 1997)

© 1997

Rahul Sarpeshkar

All Rights Reserved

Dedicated to my parents,  
Nalini and Pandi Sarpeshkar

## Acknowledgements

I would like to gratefully acknowledge the contribution of the following people to my thesis:

- Carver Mead, my mentor, adviser, and friend. Carver has always been a constant source of inspiration and encouragement. I will be indebted to Carver for teaching me that imagination, intuition, and common sense were more important than formal education.
- Richard F. Lyon, my "hearing mentor" at Caltech. Dick's keen intelligence and outspokenness served to clarify many of my muddier thoughts. My thesis has built on the strong foundation that Dick pioneered.
- The other members of my thesis committee, Yaser Abu-Mostafa, John Allman, Richard Andersen, and Christof Koch for their interest and their help in my work.
- Lloyd Watts for the use of figures from his thesis in my oral presentation.
- Dave Kewley for his extremely generous and extensive help with various aspects of my thesis.
- The people at Caltech who've helped me on numerous occasions: Ben Arthur, Kwabena Boahen, Prista Charuworn, Geoff Coram, Chris Diorio, Tobi Delbrück, Jeff Dickson, Paul Hasler, John Klemic, Jörg Kramer, Boug Kustsza, Mike Levene, Shih-Chii Liu, Sanjoy Mahajan, Sunit Mahajan, Bradley Minch, Lena Peterson, Sam Roweis, John Wyatt, Orly Yadid-Pecht.
- Candace Schmidt and Donna Fox who made Carverland a fun and efficient place to work in.
- Lyn Dupre for her careful editing of my manuscript.

## Abstract

Low-power wide-dynamic-range systems are extremely hard to build. The cochlea is one of the most awesome examples of such a system: It can sense sounds over 12 orders of magnitude in intensity, with an estimated power dissipation of only a few tens of microwatts.

We describe an analog electronic cochlea that processes sounds over 6 orders of magnitude in intensity, while dissipating less than 0.5mW. This 117-stage, 100Hz–10Khz cochlea has the widest dynamic range of any artificial cochlea built to date. This design, using frequency-selective gain adaptation in a low-noise traveling-wave amplifier architecture, yields insight into why the human cochlea uses a traveling-wave mechanism to sense sounds, instead of using bandpass filters.

We propose that, more generally, the computation that is most efficient in its use of resources is an intimate hybrid of analog and digital computation. For maximum efficiency, the information and information-processing resources of the hybrid form of computation must be distributed over many wires, with an optimal signal-to-noise ratio per wire. These results suggest that it is likely that the brain computes in a hybrid fashion, and that an underappreciated and important reason for the efficiency of the human brain, which only consumes 12W, is the hybrid and distributed nature of its architecture.

# Contents

<b>Acknowledgements</b>	<b>iv</b>
<b>Abstract</b>	<b>v</b>
<b>1 Overview</b>	<b>1</b>
1.1 White Noise in MOS Transistors and Resistors . . . . .	1
1.2 A Low-Power Wide-Linear Range Transconductance Amplifier . . . . .	1
1.3 A Low-Power Wide-Dynamic-Range Analog VLSI Cochlea . . . . .	2
1.4 Efficient Precise Computation with Noisy Components: Extrapolating from Electronics to Neurobiology . . . . .	3
1.5 A New Geometry for All-Pole Underdamped Second-Order Transfer Functions	5
1.6 Publication List . . . . .	5
1.7 The Use of We . . . . .	6
<b>2 White Noise in MOS Transistors and Resistors</b>	<b>7</b>
2.1 Shot Noise in Subthreshold MOS Transistors . . . . .	8
2.2 Shot Noise vs. Thermal Noise . . . . .	12
2.3 The Equipartition Theorem and Noise Calculations . . . . .	14
2.4 Conclusion . . . . .	16
<b>Bibliography</b>	<b>18</b>
<b>3 A Low-Power Wide-Linear-Range Transconductance Amplifier</b>	<b>24</b>
3.1 Introduction . . . . .	25
3.2 First-Order Effects . . . . .	27
3.2.1 Basic Transistor Relationships . . . . .	27
3.2.2 Transconductance Reduction Through Degeneration . . . . .	28
3.2.3 Bump Linearization . . . . .	30
3.2.4 Experimental Data . . . . .	32
3.3 Second-Order Effects . . . . .	33

3.3.1	Common-Mode Characteristics . . . . .	33
3.3.2	Bias-Current Characteristics . . . . .	35
3.3.3	Gain Characteristics . . . . .	35
3.3.4	Offset Characteristics . . . . .	36
3.4	Follower-Integrator Characteristics . . . . .	38
3.4.1	Linear and Nonlinear Characteristics . . . . .	39
3.5	Noise and Dynamic Range . . . . .	41
3.5.1	Theoretical Computations of Noise in the Amplifier and Follower-Integrator . . . . .	41
3.5.2	Theoretical Computations of Dynamic Range . . . . .	45
3.5.3	Experimental Noise Curves . . . . .	47
3.5.4	Capacitive-Divider Techniques . . . . .	48
3.6	Conclusions . . . . .	50
	<b>Acknowledgements</b>	<b>52</b>
	<b>Bibliography</b>	<b>53</b>
3.7	Appendix A . . . . .	79
3.7.1	The Effects of Changes in $\kappa$ . . . . .	79
3.7.2	The Effects of the Parasitic Bipolar Transistor . . . . .	81
<b>4</b>	<b>A Low-Power Wide-Dynamic-Range Analog VLSI Cochlea</b>	<b>85</b>
4.1	Introduction . . . . .	85
4.2	The Single Cochlear Stage . . . . .	88
4.2.1	The WLR . . . . .	89
4.2.2	The Offset-Adaptation Circuit . . . . .	90
4.2.3	The Second-Order Filter . . . . .	91
4.2.4	The Tau-and- $Q$ Control Circuit . . . . .	95
4.2.5	The Inner Hair Cell and Peak-Detector Circuits . . . . .	96
4.2.6	The Properties of an Entire Cochlear Stage . . . . .	98
4.3	Properties of the Cochlea . . . . .	101
4.3.1	Low-Frequency Attenuation . . . . .	101
4.3.2	Offset Adaptation . . . . .	104

4.3.3	Frequency Response . . . . .	104
4.3.4	Noise, Dynamic Range, and SNR . . . . .	106
4.3.5	Spatial Characteristics . . . . .	110
4.3.6	Dynamics of Gain and Offset Adaptation . . . . .	110
4.3.7	The Mid-Frequency and High-Frequency Cochleas . . . . .	110
4.4	Analog Versus Digital . . . . .	111
4.4.1	The ASIC Digital Cochlea . . . . .	111
4.4.2	$\mu$ P Cochlea . . . . .	113
4.4.3	Comparison of Analog and Digital Cochleas . . . . .	113
4.5	The Biological Cochlea . . . . .	114
4.5.1	Traveling-Wave Architectures Versus Bandpass Filters . . . . .	116
4.6	Applications to Cochlear Implants . . . . .	117
4.7	Conclusions . . . . .	117
<b>Bibliography</b>		<b>119</b>
<b>5</b>	<b>Efficient Precise Computation with Noisy Components: Extrapolating From Electronics to Neurobiology</b>	<b>162</b>
5.1	Introduction . . . . .	162
5.2	Analog Versus Digital: The Intuitive Picture . . . . .	165
5.2.1	Physicality: Advantage Analog . . . . .	167
5.2.2	Noise and Offset: Advantage Digital . . . . .	168
5.3	Analog Versus Digital: The Quantitative Picture . . . . .	169
5.3.1	Noise in MOS Transistors . . . . .	169
5.3.2	Noise in Analog Systems . . . . .	171
5.3.3	The Costs of Analog Precision . . . . .	174
5.3.4	The Costs of Digital Precision . . . . .	175
5.3.5	Precision Costs: Analog Versus Digital . . . . .	176
5.3.6	A Clarification . . . . .	176
5.3.7	The Meaning of the Quantitative Analysis . . . . .	177
5.4	The Best of Both Worlds . . . . .	177
5.4.1	Distributed Analog Computation . . . . .	178
5.4.2	Hybrid Computation . . . . .	180



5.4.3	Distributed and Hybrid Computation . . . . .	185
5.5	Extrapolating to Neurobiology . . . . .	185
5.5.1	Why Neuronal Information Processing is Distributed . . . . .	186
5.5.2	Information Processing in the Brain is Hybrid . . . . .	186
5.5.3	How Signal Restoration May be Implemented . . . . .	188
5.5.4	Noise in Biological Devices . . . . .	190
5.5.5	Noise in Neurobiological Systems . . . . .	192
5.6	Other Reasons for the Brain's Efficiency . . . . .	193
5.6.1	Technology . . . . .	193
5.6.2	Signal Processing . . . . .	195
5.6.3	Computational Strategies . . . . .	195
5.7	Summary . . . . .	196
<b>Bibliography</b>		<b>199</b>
5.8	Appendix A: The Efficiency of Cortical Computation . . . . .	202
5.8.1	The Operational Throughput of Cortical Computation . . . . .	202
5.8.2	The Power Consumption of the Brain . . . . .	203
5.9	Appendix B: Noise in MOS Transistors . . . . .	204
5.10	Appendix C: Noise in Analog Systems—Further Details . . . . .	207
<b>6</b>	<b>A New Geometry for All-Pole Underdamped Second-Order Transfer Functions</b>	<b>217</b>
6.1	Introduction . . . . .	217
6.2	The Usual Geometry . . . . .	217
6.3	Transforming to the New Geometry . . . . .	218
6.4	The Geometry of Gain . . . . .	219
6.4.1	Relationship to Other Geometries . . . . .	221
6.5	The Geometry of Phase . . . . .	222
6.6	How to Remember the Mapping From Algebra to Geometry . . . . .	223
6.7	The Geometry of Group Delay . . . . .	224
6.8	Conclusions . . . . .	225
6.9	Acknowledgements . . . . .	225



## Chapter 1 Overview

This thesis is a compilation of five journal papers. Some of them have been published, some of them are currently under review, and some of them are in press. Although each chapter is self contained and may be read without reference to others, there is a natural bottom-up progression from issues of noise in single transistors (Chapter 2) to issues of noise and computation in the brain (Chapter 5). Each of these chapters provides an important step in understanding how to compute efficiently with noisy components.

Chapter 6 is a diversion on the theory of second-order filters used in cochleas. We have included Chapter 6 in this thesis because it provides useful geometric techniques for future work on the cochlea.

### 1.1 White Noise in MOS Transistors and Resistors

Chapter 2 is a discussion of noise in single transistors. To minimize or exploit the effects of noise in computation, it is important to know what causes noise. Thus, Chapter 2 delves into the physical origins of noise in subthreshold MOS transistors. We present the first experimental measurements of noise in subthreshold MOS transistors, and also the deep relationship between two forms of white noise, shot noise and thermal noise. We show that thermal noise in transistors or resistors is shot noise due to internal diffusion currents in the device. We do not assume that the reader has any background in noise and begin our discussion from first principles.

### 1.2 A Low-Power Wide-Linear Range Transconductance Amplifier

In Chapter 3 we show how to build a lowpass filter with a wide dynamic range of operation by widening the linear range of operation of a conventional subthreshold amplifier. Various novel circuit and feedback techniques were used in the design of our amplifier. The amplifier has been patented. We show that if the dominant form of noise in the amplifier is

thermal noise, then widening the linear range of the amplifier increases its dynamic range of operation. If the dominant form of noise in the amplifier is  $1/f$  noise (nonthermal noise due to impurities in traps in transistors), then widening the linear range of the amplifier has no effect on the filter's dynamic range. Since our dominant form of noise is thermal noise, we attain an improvement in the filter's dynamic range. This improvement in dynamic range is crucial in the design of our wide-dynamic-range cochlea, which is built with 234 such filters.

If we want to maintain the same bandwidth of operation in the filter, an increase in its dynamic range is attained at the price of a proportionate increase in its power consumption. We encounter, for the first time in this thesis, a relationship between resource consumption (power) and the precision of the computation (as measured by the dynamic range of operation). Precise computation requires averaging over the incoherent motions of a large number of electrons per unit time in order to minimize noise. The flow of a large number of electrons per unit time implies a large current, and consequently a large power consumption.

### 1.3 A Low-Power Wide-Dynamic-Range Analog VLSI Cochlea

In complex systems like cochleas, where there are a large number of filters arranged in a cascade, noise accumulation and amplification severely degrade the dynamic range of operation. To attain a wide dynamic range of operation without an excessive consumption of power or area, it is necessary to have a strategy that adapts the gain of cochlea to the intensity of the incoming sound. The adaptation enables the cochlea to have a dynamic range of operation with varying lower and upper limits. At any given time, the dynamic range of operation is moderate ( $\approx 30\text{dB}-40\text{dB}$ ), thus limiting power consumption. Over time scales that are long compared to the adaptation time, the dynamic range is large ( $> 60\text{dB}$ ) because the system adapts its upper and lower limits to be suited to the intensity range of the input. The adaptation is almost instantaneous (one cycle of the input frequency) for soft-to-loud changes in intensity, and slow (100msecs to a few seconds depending on parameters) for loud-to-soft changes. The automatic gain control (AGC) is performed in a frequency-dependent way such that loud sounds at one frequency do not mask the effect of soft sounds at another frequency. In addition to adaptation, we use a low-noise filter topology, and an architecture called *overlapping cascades*. This architecture restores good

signal-to-noise ratios for low-frequency inputs. In prior designs, such inputs had poor signal-to-noise ratios.

The design of the silicon cochlea yields insight into why nature uses a traveling-wave mechanism to hear instead of using a bank of bandpass filters. We show that the filter cascade, that models the properties of a traveling-wave medium, results in a very efficient construction of a bank of high-order wide-dynamic-range filters with properties that are relatively invariant with input intensity. It requires a lot more circuitry to accomplish the same feat with a bank of bandpass filters.

The problem of noise accumulation and amplification in a filter cascade is solved by successive lowpass filtering in a graded exponential fashion, and by limiting the length of the filter cascade. The problem of parameter sensitivity in a filter cascade is solved by collective regulation of the filter gains by the AGC circuits of the cochlea. The cochlea is a great example of a front end that uses adaptive, distributed, and collective strategies to compute efficiently and precisely in spite of the presence of noise.

We show that our analog cochlea is more efficient than a custom digital cochlea by two orders of magnitude in power consumption; for noncustom digital cochleas, our analog cochlea is five orders of magnitude more efficient. The comparison of analog and digital cochlear efficiencies provides a starting point for a more general analysis of efficiency issues between analog and digital computation.

## 1.4 Efficient Precise Computation with Noisy Components: Extrapolating from Electronics to Neurobiology

We begin by reviewing issues of efficiency with respect to the use of physical resources like energy, time, and space for general analog and digital systems. We rederive a well-known result for particular systems, namely, that analog systems are more efficient than digital systems at low signal-to-noise ( $S_N$ ) ratios and vice versa. The basic reason for this behavior is that physical primitives are more efficient at computing than are logical primitives as long as we do not attempt to compute with low noise on one wire. At high  $S_N$ , however, the multiwire representation of information by digital systems divides the information processing into independent bit parts that many simple processing stages can collectively handle more efficiently than can one precise single-wire analog processing stage.

This intuition is mathematically expressed by a logarithmic scaling of digital computation with  $S_N$ , and a power-law-like scaling of analog computation with  $S_N$ . Furthermore, the lack of signal restoration in analog systems causes the noise accumulation for complex analog systems to be much more severe than that for complex digital systems.

It is then attractive to wonder if a hybrid paradigm that combines the best of both worlds can do better than either. We suggest that computation that is most efficient in its use of resources is neither analog computation nor digital computation, but rather is an intimate mixture of the two forms. We propose a hybrid architecture that combines the advantages of discrete-signal restoration with the advantages of continuous-signal continuous-time analog computation. The tradeoffs between resources spent on computation versus those spent in signal restoration reveal that, for maximum efficiency, an optimum amount of continuous processing must occur before a restoring discrete decision is made. The tradeoffs between resources spent on computation versus those spent on communication reveal that, for maximum efficiency, the information and information-processing resources of the computation must be distributed over many wires, with an optimal signal-to-noise ratio per wire. Thus, we arrive at the conclusion that hybrid and distributed systems are very efficient in their use of computational resources.

Efficient computation is important in complex systems to ensure that the resource consumption of the system remains within reasonable bounds. Thus, it would appear that there is a great advantage to building complex systems with a hybrid and distributed architecture.

The human brain is one of the most efficient and complex systems ever built. The entire brain consumes only 12 W of power. The devices that the brain is built out of are noisy just like physical devices used in artificial computation. The brain is known to be a massively distributed system with a constant alternation between continuous nonspiking representations and spiking representations of information. The brain appears to compute with a hybrid and distributed architecture. However, the mere presence of spikes does not necessarily imply the encoding of discrete states. We suggest how discrete states may be encoded, and how signal restoration may be performed in networks of neurons. We do **NOT** claim that this is how signal restoration in the brain works but merely offer our suggestion as a possible way that it might work in the hopes of stimulating further work and discussion on the subject.

We have made many simplifying assumptions such as treating computation and restora-

tion as distinct entities, and similarly treating computation and communication as separate entities. It is likely that such entities are more deeply intertwined in the brain. It is likely that the rather sharp digital restorations that we propose are really soft restorations in the brain, such that a more accurate description would need to involve the language of complex nonlinear dynamical systems. However, in spite of our simplifications, we suggest that the brain is hybrid in nature. We propose that the hybrid-and-distributed architecture of the brain is one of the major reasons for its efficiency, and that the importance of this point has generally been underappreciated.

## 1.5 A New Geometry for All-Pole Underdamped Second-Order Transfer Functions

We present a geometry in which many of the relationships of a cochlear-filter transfer function become transparent and obvious. In particular, in this geometry the gain of the transfer function depends on one length, and the phase corresponds to one angle. In the standard  $s$ -plane geometric interpretation, the gain depends on the product of two lengths, and the phase is the sum of two angles.

## 1.6 Publication List

We provide an index of the Chapter Number and the associated journal publication.

- **Chapter 2:** R. Sarpeshkar, T. Delbrück, and C. A. Mead, “White Noise in MOS Transistors and Resistors”, *IEEE Circuits and Devices*, Vol. 9, No. 6, pp. 23–29, Nov. 1993.
- **Chapter 3:** R. Sarpeshkar, R. F. Lyon, and C. A. Mead, “A Low-Power Wide-Linear-Range Transconductance Amplifier”, to appear in *Analog Integrated Circuits and Signal Processing*, 1997.
- **Chapter 4:** R. Sarpeshkar, R. F. Lyon, and C. A. Mead, “A Low-Power Wide-Dynamic-Range Analog VLSI Cochlea”, to appear in *Analog Integrated Circuits and Signal Processing*, 1997.

- **Chapter 5:** R. Sarpeshkar, “Efficient Precise Computation with Noisy Components: Extrapolating from Electronics to Neurobiology”, under review in *Neural Computation*.
- **Chapter 6:** R. Sarpeshkar, S. Mahajan, and R. F. Lyon, “A New Geometry for All-Pole Underdamped Second-Order Transfer Functions”, under review in *IEEE Transactions in Signal Processing*.

## 1.7 The Use of We

Throughout this thesis I use 'We' instead of 'I'. This is partly because of style, and partly because some of the work was done jointly with other authors. However, more than 90% of the work in each chapter paper, including the creative idea aspects and the actual labor, was done by me. I am the first author on all the chapter papers and bear responsibility for any errors and omissions in these papers.



## Chapter 2 White Noise in MOS Transistors and Resistors

### Abstract

Shot noise and thermal noise have long been considered the results of two distinct mechanisms, but they aren't.

We live in a very energy-conscious era today. In the electrical engineering community, energy-consciousness has manifested itself in an increasing focus on low-power circuits. Low-power circuits imply low current and/or voltage levels and are thus more susceptible to the effects of noise. Hence, a good understanding of noise is timely.

Most people find the subject of noise mysterious, and there is –understandably–much confusion about it. Although the fundamental physical concepts behind noise are simple, much of this simplicity is often obscured by the mathematics invoked to compute expressions for the noise.

The myriads of random events that happen at microscopic scales cause fluctuations in the values of macroscopic variables such as voltage, current and charge. These fluctuations are referred to as noise. The noise is called “white noise” if its power spectrum is flat and “pink noise” or “flicker noise” if its power spectrum goes inversely with the frequency. In this article, we shall discuss theoretical and experimental results for white noise in the low-power subthreshold region of operation of an MOS transistor. A good review of operation in the subthreshold region may be found in Mead [2]. This region is becoming increasingly important in the design of low-power analog circuits, particularly in neuromorphic applications that simulate various aspects of brain function [2]- [4].

A formula for subthreshold noise in MOS transistors has been derived by Enz [6] and Vittoz [18] from considerations that model the channel of a transistor as being composed of a series of resistors. The integrated thermal noise of all these resistors yields the net thermal noise in the transistor, after some fairly detailed mathematical manipulations. The expression obtained for the noise, however, strongly suggests that the noise is really “shot noise”, conventionally believed to be a different kind of white noise from thermal noise.

We solve the mystery of how one generates a shot-noise answer from a thermal-noise derivation by taking a fresh look at noise in subthreshold MOS transistors from first principles. We then rederive the expression for thermal noise in a resistor from our viewpoint. We believe that our derivation is simpler and more transparent than the one originally offered in 1928 by Nyquist, who counted modes on a transmission line to evaluate the noise in a resistor [5]. Our results lead to a unifying view of the processes of shot noise (noise in vacuum tubes, photo diodes and bipolar transistors) and thermal noise (noise in resistors and MOS devices).

In subthreshold MOS transistors, the white-noise current power is  $2qI\Delta f$  (derived later) where  $I$  is the d.c. current level,  $q$  is the charge on the electron,  $f$  is the frequency and  $\Delta f$  is the bandwidth. In contrast, the flicker-noise current power is approximately  $KI^2\Delta f/f$  where  $K$  is a process and geometry-dependent parameter. Thus, white noise dominates for  $f > KI/2q$ . For the noise measurements in this paper, taken at current levels in the  $100fA - 100pA$  range, white noise was the only noise observable even at frequencies as low as 1Hz. Reibold [8] and Schutte [9] have measured noise for higher subthreshold currents ( $> 4$  nA), but have reported results from flicker-noise measurements only.

Our results (to our best knowledge) are the first reports of measurements of white noise in subthreshold MOS transistors. We will show that they are consistent with our theoretical predictions. We also report measurements of noise in photoreceptors (a circuit containing a photo diode and an MOS transistor) that are consistent with theory. The photoreceptor noise measurements illustrate the intimate connection of the equipartition theorem of statistical mechanics with noise calculations.

The measurements of noise corresponding to miniscule subthreshold transistor currents were obtained by conveniently performing them on a transistor with  $W/L \approx 10^4$ . The photoreceptor noise measurements were obtained by amplifying small voltage changes with a low-noise high-gain on-chip amplifier.

## 2.1 Shot Noise in Subthreshold MOS Transistors

Imagine that you are an electron in the source of an MOS transistor. You shoot out of the source, and if you have enough energy to climb the energy barrier between the source and the channel, you enter it. If you are unlucky, you might collide with a lattice vibration,

surface state, or impurity and fall right back into the source. If you do make it into the channel, you will suffer a number of randomizing collisions. Eventually, you will actually diffuse your way into the drain. Each arrival of such an electron at the drain contributes an impulse of charge.

Similarly, electrons that originate in the drain may find their way into the source. Thus, there are *two independent* random processes occurring simultaneously that yield a forward current  $I_f$ , from source to drain and a reverse current  $I_r$ , from drain to source. Since the barrier height at the source is less than the barrier height at the drain, more electrons flow from the source to drain than vice versa and  $I_f > I_r$ .

$$\begin{aligned}
 I &= I_f - I_r \\
 I_r &= I_f e^{-\frac{V_{ds}}{U_T}} \\
 \Rightarrow I &= I_f \left(1 - e^{-\frac{V_{ds}}{U_T}}\right) \\
 &= I_{sat} \left(1 - e^{-\frac{V_{ds}}{U_T}}\right)
 \end{aligned} \tag{2.1}$$

where  $I$  is the measured channel current,  $V_{ds}$  is the drain-to-source voltage, and  $I_f = I_{sat}$  is the saturation current of the transistor, and  $U_T = kT/q$  is the thermal voltage.

Because the forward and reverse processes are independent, we can compute the noise contributed by each component of the current separately and then add the results. Thus, we first assume that  $I_r$  is zero, or equivalently that  $C_D$ , the concentration of electrons at the drain end of the channel, is zero. The arrival of electrons at the drain may be modelled by a Poisson process with an arrival rate  $\lambda$ . A small channel length  $L$ , a large channel width  $W$ , a large diffusion constant for electrons  $D_n$ , and a large concentration of electrons at the source  $C_S$  all lead to a large arrival rate. Because the current in a subthreshold MOS transistor flows by diffusion, the electron concentration is a linear function of distance along the channel, and the forward current  $I_f$  and arrival rate  $\lambda$  are given by

$$I_f = qD_n W \frac{C_S}{L} \tag{2.2}$$

$$\lambda = I_f/q. \tag{2.3}$$

Powerful theorems due to Carson and Campbell, as described in standard noise textbooks such as [10], allow us to compute the power spectrum of the noise. Suppose we have

a Poisson process with an arrival rate of  $\lambda$ , and each arrival event causes a response,  $F(t)$ , in a detector sensitive to the event. Let  $s(t)$  be the macroscopic variable of the detector that corresponds to the sum of all the  $F(t)$ 's generated by these events. Then, the mean value of  $s(t)$  and the power spectrum,  $P(f)$ , of the fluctuations in  $s(t)$  are given by

$$\overline{s(t)} = \lambda \int_{-\infty}^{\infty} F(t) dt \quad (2.4)$$

$$\overline{(s(t) - \overline{s(t)})^2} = \lambda \int_{-\infty}^{\infty} F^2(t) dt \quad (2.5)$$

$$= \int_0^{\infty} P(f) df \quad (2.6)$$

$$= 2\lambda \int_0^{\infty} |\psi(f)|^2 df \quad (2.7)$$

where  $\psi(f) = \int_{-\infty}^{+\infty} F(t) e^{-j2\pi ft} dt$  is the Fourier transform of  $F(t)$ . Each electron arrival event at the drain generates an impulse of charge  $q$  that corresponds to  $F(t)$ . Thus, we obtain

$$\overline{I} = q\lambda \quad (2.8)$$

$$\overline{(I - \overline{I})^2} = 2q^2\lambda \int_0^{\Delta f} df \quad (2.9)$$

$$= 2q\overline{I}\Delta f. \quad (2.10)$$

where  $\Delta f$  is the bandwidth of the system. Eq. (2.10) is the well-known result for the shot-noise power spectrum. Thus, the noise that corresponds to our forward current is simply given by  $2qI_f\Delta f$ . Similarly, the noise that corresponds to the reverse current is given by  $2qI_r\Delta f$ . The total noise in a given bandwidth  $\Delta f$  is given by

$$\begin{aligned} \Delta I^2 &= 2q(I_f + I_r)\Delta f \\ &= 2qI_f(1 + e^{-\frac{V_{ds}}{U_T}})\Delta f \\ &= 2qI_{sat}(1 + e^{-\frac{V_{ds}}{U_T}})\Delta f. \end{aligned} \quad (2.11)$$

where  $I_{sat} = I_f = I_0 e^{\frac{\kappa V_g - V_s}{U_T}}$  corresponds to the saturation current at the given gate voltage. Note that as we transition from the linear region of the transistor ( $V_{ds} < 5U_T$ ) to the saturation region, the noise is gradually reduced from  $4qI_{sat}\Delta f$  to  $2qI_{sat}\Delta f$ . This factor of two reduction occurs because the shot-noise component from the drain disappears in

saturation. A similar phenomenon occurs in junction diodes where both the forward and reverse components contribute when there is no voltage across the diode; as the diode gets deeply forward or reverse biased, the noise is determined primarily by either the forward or reverse component, respectively [11].

The flatness of the noise spectrum arises from the impulsive nature of the microscopic events. We might expect that the flat Fourier transform of the microscopic events that make up the net macroscopic current would be reflected in its noise spectrum. Carson's and Campbell's theorems express formally that this is indeed the case. The variance of a Poisson process is proportional to the rate, so it is not surprising that the variance in the current is just proportional to the current. Further, the derivation illustrates that the diffusion constant and channel length simply alter the arrival rate by Eq. (2.3). Even if some of the electrons recombined in the channel – corresponding to the case of a bipolar transistor or junction diode –, the expression for noise in Eq. (2.11) is unchanged. The arrival rate is reduced because of recombination. A reduction in arrival rate reduces the current and the noise in the same proportion. The same process that determines the current also determines the noise.

Experimental measurements were conducted on a transistor with  $W/L \approx 10^4$  for a saturation current of 40nA (Fig. 1). A gigantic transistor size was used to scale up the tiny subthreshold currents to 10nA-1uA levels and make them easily measurable by a low-noise off-chip sense amplifier with commercially available resistor values. The shot noise scales with the current level, so long as the transistor remains in subthreshold. The noise measurements were conducted with a HP3582A spectrum analyzer. The data were taken over a bandwidth of 0-500 Hz. The normalized current noise power,  $\Delta I^2/(2qI_{sat}\Delta f)$ , and the normalized current  $I/I_{sat}$  are plotted. The lines show the theoretical predictions of Eqs. (2.1) and (2.11). Using the measured value of the saturation current, the value for the charge on the electron, and the value for the thermal voltage, we were able to fit our data with no free parameters whatsoever. Notice that as the normalized current goes from 0 in the linear region to 1 in the saturation region, the normalized noise power goes from 2 to 1 as expected. Fig. 2 shows measurements of the noise power per unit bandwidth,  $\Delta I^2/\Delta f$ , in the saturation region for various saturation currents  $I_{sat}$ . Since we expect this noise power to be  $2qI_{sat}$ , we expect a straight line with slope  $2q$  which is the theoretical line drawn through the data points. As the currents start to exceed  $1\mu\text{A}$ - $10\mu\text{A}$  for our

huge transistor, the presence of  $1/f$  noise at the frequencies over which the data were taken begins to be felt. The noise is thus higher than what we would expect purely from white noise considerations.

## 2.2 Shot Noise vs. Thermal Noise

We have taken the trouble to derive the noise from first principles even though we could have simply asserted that the noise was just the sum of shot-noise components from the forward and reverse currents. We have done so to clarify answers to certain questions that naturally arise:

- Is the noise just due to fluctuations in electrons moving across the barrier or does scattering in the channel contribute as well?
- Do electrons in the channel exhibit thermal noise?
- Do we have to add another term for thermal noise?

Our derivation illustrates that the computed noise is the total noise and that we don't have to add any extra terms for thermal noise. Our experiments confirm that this is indeed the case. The scattering events in the channel and the fluctuations in barrier crossings all result in a Poisson process with some electron arrival rate. Both processes occur simultaneously, are caused by thermal fluctuations and result in white noise. Conventionally, the former process is labelled "thermal noise" and the latter process is labelled "shot noise". In some of the literature, the two kinds of noise are often distinguished by the fact that shot noise requires the presence of a dc current while thermal noise occurs even when there is no dc current [12]. However, we notice in our subthreshold MOS transistor, that when  $I_f = I_r$ , there is no net current but the noise is at its maximum value of  $4qI_f\Delta f$ . Thus a two-sided shot noise process exhibits noise that is reminiscent of thermal noise. We will now show that **thermal noise is two-sided shot noise**.

Let us compute the noise current in a resistor shorted across its ends. Since there is no electric field, the fluctuations in current must be due to the random diffusive motions of the electrons. The average concentration of electrons is constant all along the length of the resistor. This situation corresponds to the case of a subthreshold transistor with  $V_{ds} = 0$ ,

where the average concentrations of electrons at the source edge of the channel, drain edge of the channel and all along the channel, are at the same value.

In a transistor, the barrier height and the gate voltage are responsible for setting the concentrations at the source and drain edges of the channel. In a resistor, the concentration is set by the concentration of electrons in its conduction band. The arrival rate of the Poisson process is, however, still determined by the concentration level, diffusion constant and length of travel. This is so because, in the absence of an electric field, the physical process of diffusion is responsible for the motions of the electrons. Thus, the power spectrum of the noise is again given by  $2q(I_f + I_r)$ . The currents  $I_f$  and  $I_r$  are both equal to  $qDnA/L$  where  $D$  is the diffusion constant of electrons in the resistor,  $n$  is the concentration per unit volume,  $A$  is the area of cross section and  $L$  is the length. Einstein's relation yields  $D/\mu = kT/q$ , where  $\mu$  is the mobility. Thus, the noise power is given by

$$\begin{aligned}
 \Delta I^2 &= 4qI_f\Delta f \\
 &= 4q \times \frac{qDnA}{L}\Delta f \\
 &= 4q \times \mu kTn \frac{A}{L}\Delta f \\
 &= 4kT(q\mu n) \frac{A}{L}\Delta f \\
 &= 4kT(\sigma) \frac{A}{L}\Delta f \\
 &= 4kTG\Delta f
 \end{aligned} \tag{2.12}$$

where  $G$  is the conductance of the resistor and  $\sigma$  is the conductivity of the material. Thus, we have re-derived Johnson and Nyquist's well-known result for the short circuit noise current in a resistor! The key step in the derivation is the use of the Einstein relation  $D/\mu = kT/q$ . This relation expresses the connection between the diffusion constant  $D$ , which determines the forward and reverse currents, the mobility constant  $\mu$ , which determines the conductance of the resistor, and the thermal voltage  $kT/q$ .

It is because of the internal consistency between thermal noise and shot noise that formulas derived from purely shot noise considerations (this paper) agree with those derived from purely thermal noise considerations [6].

## 2.3 The Equipartition Theorem and Noise Calculations

No discussion of thermal noise would be complete without a discussion of the equipartition theorem of statistical mechanics, which lies at the heart of all calculations of thermal noise: Every state variable in a system that is not constrained to have a fixed value is free to fluctuate. The thermal fluctuations in the current through an inductor or the voltage on a capacitor are the ultimate origins of circuit noise. If the energy stored in the system corresponding to state variable  $x$  is proportional to  $x^2$ , then  $x$  is said to be a degree of freedom of the system. Thus, the voltage on a capacitor constitutes a degree of freedom, since the energy stored on it is  $CV^2/2$ . Statistical mechanics requires that if a system is in thermal equilibrium with a reservoir of temperature  $T$ , then each degree of freedom of the system will have a fluctuation energy of  $kT/2$ . Thus, the mean square fluctuation  $\Delta V^2$ , in the voltage of a system with a single capacitor must be such that

$$\begin{aligned}\frac{C\Delta V^2}{2} &= \frac{kT}{2}, \\ \Rightarrow \Delta V^2 &= \frac{kT}{C}.\end{aligned}\tag{2.13}$$

This simple and elegant result shows that if all noise is of thermal origin, and the system is in thermal equilibrium, then the total noise over the entire bandwidth of the system is determined just by the temperature and capacitance [13]. If we have a large resistance coupling noise to the capacitor, the noise per unit bandwidth is large but the entire bandwidth of the system is small; if we have a small resistance coupling noise to the capacitor, the noise per unit bandwidth is small but the entire bandwidth of the system is large. Thus, the total noise – the product of the noise per unit bandwidth  $4kTR$  and the bandwidth of the circuit  $\frac{1}{RC}$  is constant, independent of  $R$ . We illustrate, for the particular circuit configuration of Fig. 3, how the noise from various devices interact to yield a total noise of  $kT/C$ .

Fig. 3 shows a network of transistors all connected to a capacitor,  $C$  at the node  $V_s$ . We use the sign convention that the forward currents in each transistor flow away from the common source node, and the reverse currents flow toward the common source node.<sup>1</sup> The

<sup>1</sup>Our sign convention is for carrier current, not conventional current. Thus, in an NFET or a PFET, the forward current is the one that flows away from the source irrespective of whether the carriers are electrons or holes. This convention results in a symmetric treatment of NFETs and PFETs.



gate and drain voltages,  $V_{gi}$  and  $V_{di}$ , respectively are all held at constant values. Thus,  $V_s$  is the only degree of freedom in the system. Kirchoff's current law at the source node requires that in steady state

$$\sum_{i=1}^n I_f^i = \sum_{i=1}^n I_r^i. \quad (2.14)$$

The conductance of the source node is given by

$$g_s = \sum_{i=1}^n \frac{I_f^i}{U_T}. \quad (2.15)$$

The bandwidth,  $\Delta f$ , of the system is then

$$\Delta f = \frac{1}{2\pi} \times \frac{\pi}{2} \times \frac{g_s}{C} = \frac{g_s}{4C} \quad (2.16)$$

where the factor  $1/2\pi$  converts from angular frequency to frequency and factor  $\pi/2$  corrects for the rolloff of the first-order filter not being abrupt<sup>2</sup>. Thus, the total noise is

$$\begin{aligned} \Delta I^2 &= \sum_{i=1}^n 2q (I_f^i + I_r^i) \frac{g_s}{4C} \\ &= \sum_{i=1}^n 4q I_f^i \frac{g_s}{4C} \end{aligned} \quad (2.17)$$

where we have used Eq. (2.14) to eliminate  $I_r$ . The voltage noise is just  $\Delta I^2/g_s^2$  or

$$\begin{aligned} \Delta V_s^2 &= \frac{q \sum_{i=1}^n I_f^i}{\sum_{i=1}^n \frac{I_f^i}{U_T}} \\ &= \frac{kT}{C}. \end{aligned} \quad (2.18)$$

The fact that the total noise equalled  $kT/C$  implies that this circuit configuration is a system in thermal equilibrium. Typically, most circuit configurations yield answers for total voltage noise that are proportional to  $kT/C$ .

We obtained direct experimental confirmation of the  $kT/C$  result from our measure-

$$\int_0^\infty \frac{df}{1 + \left(\frac{f}{f_c}\right)^2} = \frac{\pi}{2} f_c$$

ments of noise in photoreceptors: Fig. 4 shows a source-follower configuration which is analogous to the case discussed previously with two transistors connected to a common node. The lower current source is a photo diode which has current levels that are proportional to light intensity. The voltage noise is measured at the output node,  $V_s$ . The voltage  $V_g$  is such that the MOS transistor shown in the figure is in saturation and its reverse current is zero. The photo diode contributes a shot-noise component of  $2qI\Delta f$ . Thus, we obtain equal shot-noise components of  $2qI\Delta f$  from the transistor and light-dependent current source, respectively. The theory described above predicts that, independent of the current level, the total integrated noise over the entire spectrum must be the same. We observe that, as the current levels are scaled down (by decreasing the light intensity), the noise levels rise but the bandwidth falls by exactly the right amount to keep the total noise constant. The system is a low pass filter with a time constant set by the light level. Thus, the noise spectra show a low pass filter characteristic. The voltage noise levels,  $\Delta V_s^2$ , are proportional to  $\Delta I^2/g_s^2$  or to  $1/I$  and the bandwidth is proportional to  $g_s$  and therefore to the photo-current  $I$ . Thus, the product of the noise per unit bandwidth and the bandwidth is proportional to the total noise over the entire spectrum and is independent of  $I$ . Thus, the area under all three curves in Fig. 4 is the same. The smooth lines in Fig. 4, are theoretical fits using a temperature of 300K and a value of capacitance estimated from the layout.

It is possible to extend our way of thinking about noise to the above-threshold region of MOS operation as well. However, the mathematics is more difficult because the presence of a longitudinal electric field causes non-independence between the noise resulting from forward and reverse currents. Further, the modulation of the surface potential by the charge carriers results in a feedback process that attenuates fluctuations in the mobile charge concentration—an effect that is referred to as space-charge smoothing.

## 2.4 Conclusion

The key ideas of our article begin with the derivation of a formula for noise, Eq. (2.11), that is valid in the subthreshold region of operation of the MOS transistor. The noise is essentially the sum of shot-noise components from the forward and reverse currents. This noise is the total thermal noise, and no further terms need be added to model thermal noise.

This view of thermal noise as a two-sided shot noise process is fundamental, and we showed that Johnson and Nyquist's well-known expression for thermal noise in a resistor may be viewed in the same way. Thus, this article developed a unifying view of thermal noise and shot noise.

The predictions of the formula were confirmed by experimental measurements. We discussed the equipartition theorem of statistical mechanics and its relation to noise calculations. We showed how our theoretical calculations agreed with noise measurements in a photoreceptor. Finally, we concluded with a brief discussion of the considerations involved in extending our ideas to above-threshold operation in order to develop a single comprehensive theory of noise for the MOS transistor.

## **Acknowledgements**

This work was supported by grants from the Office of Naval Research and the California Competitive Technologies Program. Chip fabrication was provided by MOSIS. We thank Dr. Michael Godfrey for his helpful suggestions regarding this manuscript.

## Bibliography

- [1] C.A. Mead, *Analog VLSI and Neural Systems*, pp. 33-36, Addison-Wesley, 1989.
- [2] A. G. Andreou, "Electronic Arts Imitate Life", *NATURE*, **354** (6354), p. 501, 1991.
- [3] C. Koch *et al.*, "Computing Motion Using Analog VLSI Vision Chips: An Experimental Comparison Among Four Approaches", In: *Proceedings of the IEEE Workshop on Visual Motion*, Princeton, NJ, Oct. 7-9, 1991.
- [4] M.D. Godfrey, "CMOS Device Modeling for Subthreshold Circuits", *IEEE Transactions on Circuits and Systems II- Analog and Digital Signal Processing*, **39** (8), pp. 532-539, 1992.
- [5] H. Nyquist, "Thermal Agitation of Electric Charge in Conductors", *Physical Review*, Vol. 32, 1928, pp. 110-113.
- [6] Enz, "*High Precision CMOS Micropower Amplifiers*", PhD Thesis No. 802, pp. 50-59, EPFL, Lausanne, 1990.
- [7] E. Vittoz, "*MOS transistor*", Intensive Summer Course on CMOS VLSI Design, EPFL, Lausanne, 1990.
- [8] G. Reimbold, "Modified 1/f Trapping Noise Theory and Experiments in MOS Transistors Biased from Weak to Strong Inversion —Influence of Interface States", *I.E.E.E. Transactions on Electron Devices*, Vol. ED-31 (9), 1984.
- [9] C. Schutte and P. Rademeyer, "Subthreshold 1/f Noise Measurements in MOS Transistors Aimed at Optimizing Focal Plane Array Signal Processing", *Analog Integrated Circuits and Signal Processing*, Vol. 2(3), 1992, pp. 171-177.
- [10] A. Van der Ziel, **Noise: Sources, Characterization, Measurement**, pp. 171-173, Prentice-Hall, 1970.
- [11] F.N. Robinson, "Noise and Fluctuations in Electronic Devices and Circuits", pp. 92-94, Oxford University Press, 1974.

- [12] P.R. Gray and R. G. Meyer, "Analysis and Design of Analog Integrated Circuits", 2nd. ed., pp. 635-637, John Wiley, 1984.
- [13] A. Rose, *Vision Human and Electronic*, Plenum Press, 1977.

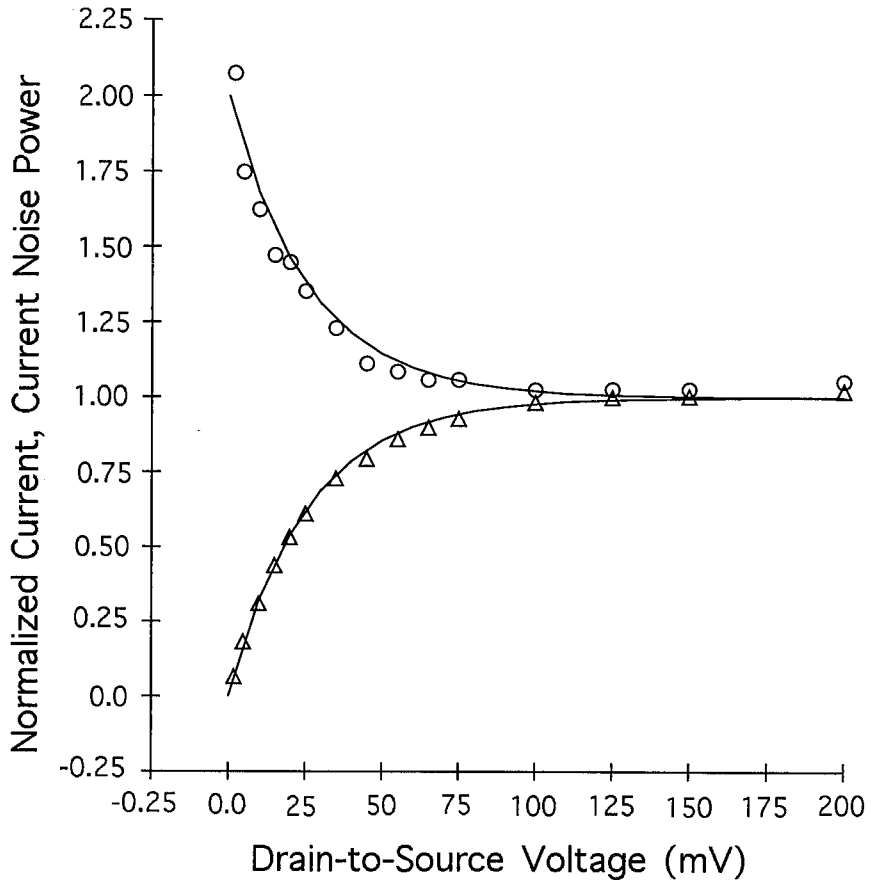


Figure 2.1: Measured current and noise characteristics of a subthreshold MOS transistor. The lower curve is the current, normalized by its saturation value  $I_{sat}$ , so that it is 1.0 in saturation and zero when  $V_{ds}$  is 0. The upper curve is the noise power,  $\Delta I^2$ , normalized by dividing it by the quantity  $2qI_{sat}\Delta f$ , where  $\Delta f$  is the bandwidth and  $q$  is the charge on the electron. We see that as the transistor moves from the linear region to saturation, the noise power decreases by a factor of two. The lines are fits to theory using the measured value of the saturation current and the value for the charge on the electron  $q = 1.6 \times 10^{-19}$  C.

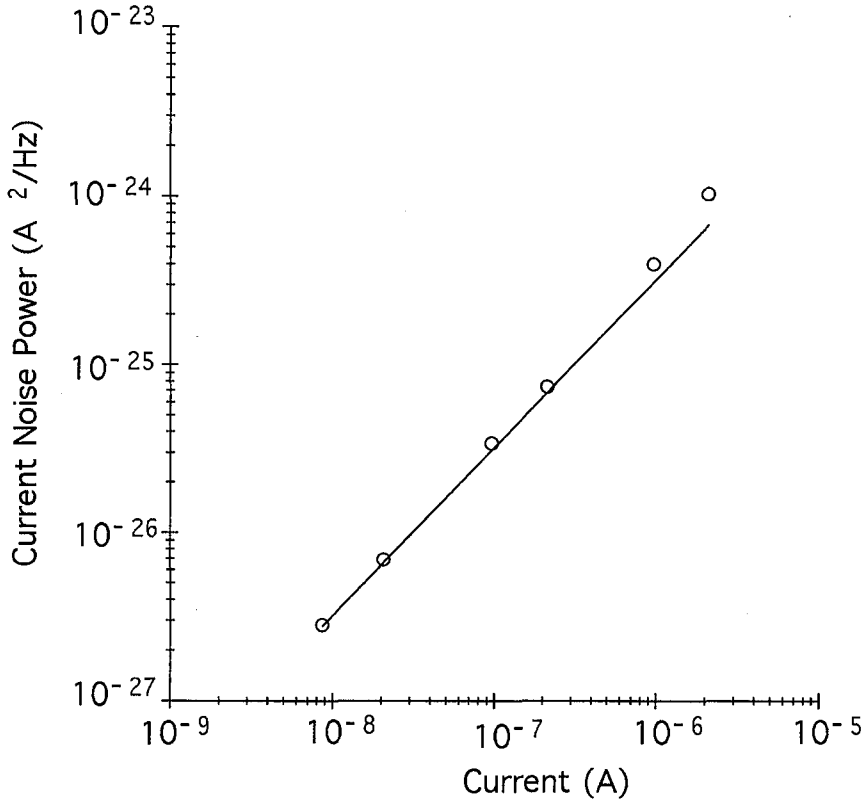


Figure 2.2: The noise power per unit bandwidth,  $\Delta I^2/\Delta f$ , plotted vs. the saturation current,  $I_{sat}$ , for different values of  $I_{sat}$ . The MOS transistor is operated in saturation. Theory predicts a straight line with a slope of  $2q = 3.2 \times 10^{-19}$  C, which is the line drawn through the data points. The small but easily discernible deviations from the line increase with higher levels of  $I_{sat}$  due to the increasing levels of  $1/f$  noise at these current values.

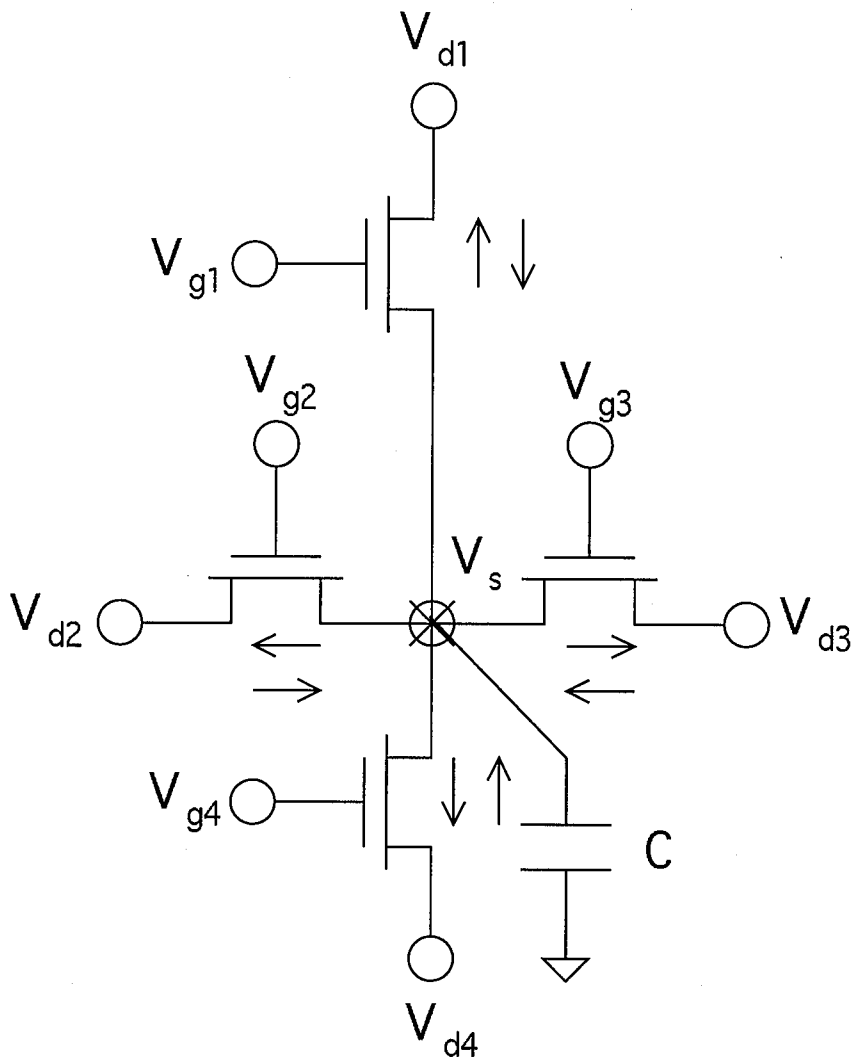


Figure 2.3: A circuit with four transistors connected to a common node with some capacitance  $C$ . By convention, the common node is denoted as the source of all transistors, and the forward currents of all transistors are indicated as flowing away from the node while the reverse currents of all transistors are indicated as flowing towards the node. Only the voltage  $V_s$  is free to fluctuate, and all other voltages are held at fixed values, so that the system has only one degree of freedom. The Equipartition theorem of statistical mechanics predicts that if we add the noise from all transistors over all frequencies to compute the fluctuation in voltage,  $\Delta V_s^2$ , the answer will equal  $kT/C$  no matter how many transistors are connected to the node, or what the other parameters are, so long as all the noise is of thermal origin. We show in the text and in the data reported in Figure 4 that our expressions for noise yield results that are consistent with this prediction.



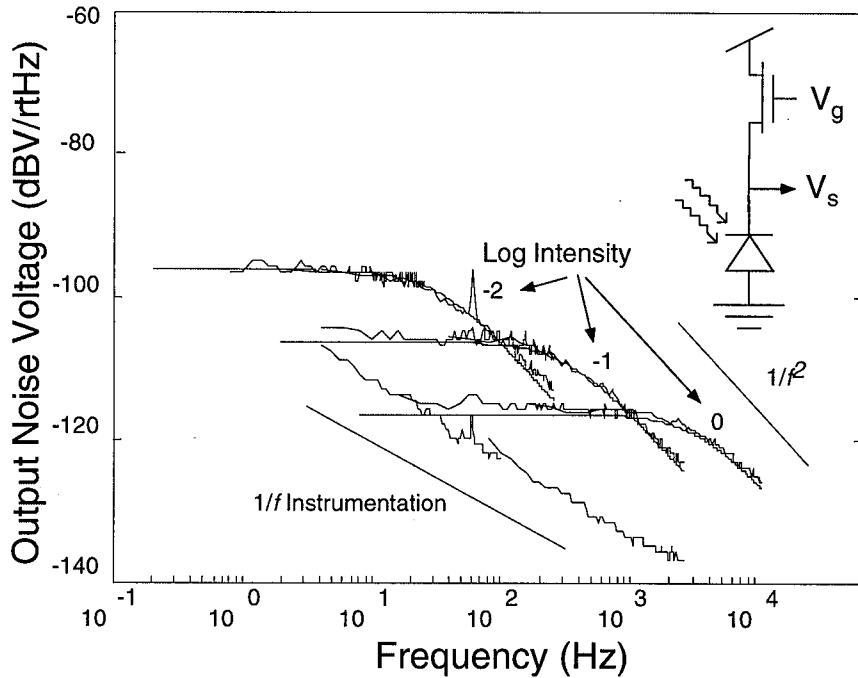


Figure 2.4: Measured noise spectral density in units of dBV/rtHz (0 dBV = 1V, -20dB = 0.1V) for the voltage  $V_s$  in the circuit above. The current source is light-dependent and the curves marked 0, -1 and -2 correspond to bright light (high current), moderate light, and dim light (low current) respectively. The intensity levels were changed by interposing neutral density filters between the source of the light and the chip to yield intensities corresponding to  $1.7 \text{ W/m}^2$ ,  $0.17 \text{ W/m}^2$ , and  $0.017 \text{ W/m}^2$  respectively. The  $1/f$  instrumentation noise is also shown and reveals that its effects were negligible over most of the range of experimental data. We observe that the noise levels and bandwidth of the circuit change so as to keep the total noise constant, i.e., at low current levels, the voltage noise is high and bandwidth low and the converse is true for high current levels. Thus, the area under the curves marked 0, -1 and -2 stays the same. The theoretical fits to the low-pass filter transfer functions are for a temperature of 300K and a capacitance of 310 fF, estimated from the layout. These results illustrate that the  $kT/C$  concept, derived from the equipartition theorem in the text is a powerful one.

## Chapter 3 A Low-Power Wide-Linear-Range Transconductance Amplifier

### Abstract

The linear range of approximately  $\pm 75$  mV of traditional subthreshold transconductance amplifiers is too small for certain applications—for example, for filters in electronic cochleas, where it is desirable to handle loud sounds without distortion and to have a large dynamic range. We describe a transconductance amplifier designed for low-power ( $< 1\mu\text{W}$ ) subthreshold operation with a wide input linear range. We obtain wide linear range by widening the tanh, or decreasing the ratio of transconductance to bias current, by the combination of four techniques. First, the well terminals of the input differential-pair transistors are used as the amplifier inputs. Then, feedback techniques known as source degeneration (a common technique) and gate degeneration (a new technique) provide further improvements. Finally, a novel bump-linearization technique extends the linear range even further. We present signal-flow diagrams for speedy analysis of such circuit techniques. Our transconductance reduction is achieved in a compact 13-transistor circuit without degrading other characteristics such as dc-input operating range. In a standard  $2\mu\text{m}$  process, we were able to obtain a linear range of  $\pm 1.7\text{V}$ . Using our wide-linear-range amplifier and a capacitor, we construct a follower-integrator with an experimental dynamic range of 65 dB. We show that, if the amplifier's noise is predominantly thermal, then an increase in its linear range increases the follower-integrator's dynamic range. If the amplifier's noise is predominantly  $1/f$ , then an increase in its linear range has no effect on the follower-integrator's dynamic range. To preserve follower-integrator bandwidth, power consumption increases proportionately with an increase in the amplifier's linear range. We also present data for changes in the subthreshold exponential parameter with current level and with gate-to-bulk voltage that should be of interest to all low-power designers. We have described the use of our amplifier in a silicon cochlea [1, 2].

### 3.1 Introduction

In the past few years, engineers have improved the linearity of MOS transconductor circuits [3]–[12]. These advances have been primarily in the area of above-threshold, high-power, high-frequency, continuous-time filters. Although it is possible to implement auditory filters (20Hz–20kHz) with these techniques, it is inefficient to do so. The transconductance and current levels in above-threshold operation are so high that large capacitances or transistors with very low  $W/L$  are required to create low-frequency poles, and area and power are wasted. In addition, it is difficult to span 3 orders of magnitude of transconductance with a square law, unless we use transistors with ungainly aspect ratios. However, it is easy to obtain a wide linear range above threshold.

In above-threshold operation, identities such as  $(x - a)^2 - (x - b)^2 = (b - a)(2x - a - b)$  are used to increase the wide linear range even further. In bipolar devices where the non-linearity is exponential, rather than second-order, it is much more difficult to completely eliminate the nonlinearity. The standard solution has been to use the feedback technique of emitter degeneration, which achieves wide linear range by reducing transconductance, and is described by Gray [39]. A clever scheme for widening the linear range of a bipolar transconductor that cancels all nonlinearities up to fifth order, without reducing the transconductance, has been proposed by Wilson [14]. A method for getting perfect linearity in a bipolar transconductor by using a translinear circuit and a resistor has been demonstrated by Chung [15]. Both of the latter methods, however, require the use of resistors, and ultimately derive their linearity from the presence of a linear element in the circuit. Resistors, however, cannot be tuned electronically, and require special process steps.

Various authors have used an MOS device as the resistive element in an emitter-degeneration scheme to make a BiCMOS transconductor—for example, the scheme proposed by Sanchez [16]. Another BiCMOS technique, reported by Weimin [5], uses an above-threshold differential pair to get wide linearity, and scales down the output currents via a bipolar Gilbert gain cell, to levels more appropriate for auditory frequencies. Above-threshold differential pairs, however, result in lower open-loop gain and higher voltage offset, and techniques such as cascode mirrors are required to improve these characteristics. Cascode mirrors, however, degrade dc output-voltage operating range and consume area. In addition, above-threshold operation results in higher power dissipation.

Subthreshold MOS technology, like bipolar technology, is based on exponential nonlinearities. Thus, it is natural to employ source-degeneration techniques. Methods for getting wider linear range that exploit the Early effect in conjunction with a source-degeneration method are described by Arreguit [19]. The Early voltage is, however, a parameter with high variance across transistors; thus, we cannot expect to get good transconductance matching in this method. Further, such schemes are highly offset prone, because any current mismatch manifests itself as a large voltage mismatch due to the exceptionally low transconductance.

The simple technique of using a diode as a source-degeneration element extends the linear range of a differential pair to about  $\pm 150$  mV, as described by Watts [6]. However, it is difficult to increase this linear range further by using two stacked diodes in series as the degeneration element—the wider linear range that is achieved is obtained at the expense of a large loss in dc-input operating range. If we operate within a 0 to 5V supply, the signal levels remain constrained to take on small values, because of the inadequate dc input operating range.

Three techniques for improving the linear range of subthreshold differential pairs have been described in [17]. The authors define the linear range to be the point where the transconductance drops by 1%. By that definition, the linear range of a conventional transconductance amplifier described by  $I_{out} = I_B \tanh(x/V_L)$  is  $V_L/5$ . Their best technique achieved a value of  $V_L = 584$  mV, and involved expensive common-mode biasing circuitry. In contrast, our technique yields a  $V_L$  of 1.7 V, and involves no additional biasing circuitry.

In [21], a 21-transistor subthreshold transconductance amplifier is described. From visual inspection of their data, the amplifier has a  $V_L$  of about 700 mV. They estimate from simple theoretical calculations that the effective number of shot-noise sources in their circuit is about 20. In contrast, our 13-transistor circuit has a  $V_L$  of 1.7 V, and the effective number of shot-noise sources in our circuit is around 5.3 (theory) or 7.5 (experiment).

We can solve the problem of getting wider linear range by interposing a capacitive divider between each input from the outside world and each input to the amplifier. Some form of slow adaptation is necessary to ensure that the dc value of each floating input to the amplifier is constrained. This approach, as used in an electronic cochlea, is described in [14]; it did not work well in practice because of its sensitivity to circuit parasitics. As we shall see later, capacitive-divider schemes bear some similarity to our scheme. We shall

discuss capacitive-divider techniques in Section 3.5.4.

To get low transconductance, we begin by picking an input terminal that is gifted with low transconductance from birth: the well. We reduce the transconductance further by using source degeneration, and a new negative-feedback technique, which we call gate degeneration. Finally, we use a novel technique, which we call bump linearization, to extend the linear range even more; bump circuits have been described in [23]. The amplifier circuit that incorporates all four techniques is shown in Figure 3.1.

In Section 3.2, we present all the essential ideas and first-order effects that describe the operation of the amplifier. We describe second-order effects, such as the common-mode and gain characteristics, in Section 3.3. We discuss the operation of this amplifier as a follower-integrator filter in Section 3.4. We elaborate on noise and dynamic range in Section 3.5. In Section 3.6, we conclude by summarizing our contributions. Appendix A contains a quantitative treatment of common-mode effects on the amplifier's transconductance. Section 3.7.1 describes the effects of changing transconductance; Section 3.7.2 is on the effects of parasitic bipolar transistors present in our well-input amplifier. Normally, the amplifier operates in the 1V to 5V range, where these bipolar transistors are inactive.

## 3.2 First-Order Effects

We begin by expressing basic transistor relationships in a form that will be useful in our paper. We use standard IEEE convention for large-signal ( $i_{DS}$ ), dc ( $I_{DS}$ ), and small-signal ( $i_{ds}$ ) variables.

### 3.2.1 Basic Transistor Relationships

The current in a subthreshold MOS well transistor in saturation is given by

$$i_{DS} = I_0 \exp\left(-\frac{\kappa v_{GS}}{U_T}\right) \exp\left(-\frac{(1-\kappa)v_{WS}}{U_T}\right), \quad (3.1)$$

where  $v_{GS}$  and  $v_{WS}$  are the gate-to-source and well-to-source voltage, respectively;  $\kappa$  is the subthreshold exponential coefficient;  $I_0$  is the subthreshold current-scaling parameter;  $U_T = kT/q$  is the thermal voltage; and  $v_{DS} \gg 5U_T$ .

Eq. (3.1) illustrates that the gate affects the current through a  $\kappa$  exponential term,

whereas the well affects the current through a  $1-\kappa$  exponential term. Thus, when the gate is effective in modulating the current, the well is ineffective, and vice versa. By differentiating Eq. (3.1), we can easily show that the gate, well, and source transconductances are

$$\begin{aligned} g_{gt} &= \frac{\partial i_{DS}}{\partial v_G} = \frac{i_{ds}}{v_g} = -\kappa \frac{I_{DS}}{U_T}, \\ g_{wl} &= \frac{\partial i_{DS}}{\partial v_W} = \frac{i_{ds}}{v_w} = -(1-\kappa) \frac{I_{DS}}{U_T}, \\ g_s &= \frac{\partial i_{DS}}{\partial v_S} = \frac{i_{ds}}{v_s} = \frac{I_{DS}}{U_T}, \end{aligned} \quad (3.2)$$

respectively. Thus if and only if  $\kappa > 0.5$ —which is almost always the case—then the well transconductance has a lower magnitude than the gate transconductance, and the well is preferable over the gate as a low-transconductance input.

It is convenient to work with dimensionless, small-signal variables: If  $i_d$  and  $v_d$  are arbitrary small-signal variables, and we define the dimensionless variables  $i = i_d/I_D$ ,  $v = v_d/U_T$ , then a relation such as  $i_d = g_d v_d = \kappa I_D v_d/U_T$  takes the simple form  $i = \kappa v$ . We notice then that  $\kappa$  plays the role of a dimensionless transconductance; that is,  $\kappa = g_d/(I_D/U_T)$  is the dimensionless transconductance that we obtain by dividing the real transconductance  $g_d$  by  $I_D/U_T$ . We shall use the dimensionless variable forms to do most of our calculations, and then shall convert them back to the real forms. For convenience, we denote the dimensionless variable by the same name as that of the variable from which it is derived. Thus, Eq. (3.2) when converted to its dimensionless form, simply reads  $g_{gt} = -\kappa$ ,  $g_{wl} = -(1-\kappa)$ , and  $g_s = 1$ .

Figure 3.2 shows a well transistor, its small-signal-equivalent circuit, and a signal-flow diagram that represents its small-signal relations. In this paper, we shall ignore the capacitances that would be represented in a complete small-signal model of the transistor.

### 3.2.2 Transconductance Reduction Through Degeneration

The technique of source degeneration is well known, and was first used in vacuum-tube design; there it was referred to as *cathode degeneration*, and was described by Landee [24]. Later, it was used in bipolar design, where it is referred to as *emitter degeneration* [39]. The idea behind source degeneration is to convert the current flowing through a transistor into a voltage through a resistor or diode, and then to feed this voltage back to the emitter or source of the transistor to decrease its current.

*Gate degeneration* has never been reported in the literature to our knowledge. This lacuna probably occurs because most designs use the gate as an input and thus never have it free to degenerate. The vacuum-tube literature, however, shows familiarity with a similar concept, called *screen degeneration*, as described in Landee [24]. The idea behind gate degeneration is to convert the current flowing through a transistor into a voltage through a diode, and then to feed this voltage back to the gate of the transistor to decrease its current.

Figure 3.3a shows a half-circuit for one differential arm of the amplifier of Figure 3.1, *if we neglect the B transistors for the time being*. The source-degeneration diode is the *p*FET connected to the source of the well-input transistor; the gate-degeneration diode is the *n*FET connected to the drain of the well-input transistor. The gate-degeneration diode is essentially free in our circuit, because it is part of the current mirror that feeds the differential-arm currents to the output. The voltage  $V_C$  represents the common-node voltage of the differential arms. In differential-mode ac analysis, the common-node voltage is grounded, as explained in the following paragraph.

In Figure 3.1, if  $v_+ = v_-$ , and the amplifier is perfectly matched, then a quiescent current of  $I_B/2$  flows through each branch of the amplifier and  $i_{OUT}$  will be 0. If we now vary the differential voltage,  $v_d = v_+ - v_-$ , by a small amount, the current changes by  $i_{out} = gv_d$ , where  $g$  is the transconductance of the amplifier. We would like to compute  $g$ . If we apply  $v_d$ , such that  $v_+$  changes by  $+v_d/2$  and  $v_-$  changes by  $-v_d/2$ , then the common node of the two differential halves (the source of the S transistors) does not change in voltage. For the purposes of small-signal analysis, we can treat the common node as a virtual ground. Thus, if  $g_h$  is the transconductance of the half-circuit shown in Figure 3.3a, the output current is  $g_h \frac{v_d}{2} - (-g_h \frac{v_d}{2}) = g_h v_d$ . Hence, the transconductance of the half-circuit, biased to the current level of  $I_B/2$ , is the transconductance of the amplifier.

The circuit of Figure 3.3a yields the small-signal circuit of Figure 3.3b: The source-degeneration diode is represented by a dimensionless resistor of value  $1/\kappa_p$ , the gate-degeneration diode is represented by a dimensionless resistor of value  $1/\kappa_n$ , the gate-controlled current source of Figure 3.2 is represented by a dimensionless resistor of value  $1/\kappa$  (the gate is tied to the drain), and the well-controlled current source of Figure 3.2 is represented by a dependent source, as shown.

The left half of Figure 3.3c represents the signal-flow diagram for the well-input transistor, as derived in Figure 3.2. The right half of Figure 3.3c represents the blocks due to

the source or gate degeneration diodes feeding back to the source or gate. Thus, we have two negative-feedback loops acting in parallel to reduce the transconductance. One loop feeds back the output current to the source via a  $-1/\kappa_p$  block; the other loop feeds back the output current to the gate via a  $1/\kappa_n$  block. Since the magnitude of the loop gains of the source-degeneration and gate-degeneration loops are  $A_s = \frac{1}{\kappa_p}$  and  $A_g = \frac{\kappa}{\kappa_n}$  respectively, the well transconductance is attenuated by  $\frac{1}{1+A_s+A_g}$ ; that is to say, the transconductance is

$$g = \frac{1 - \kappa}{1 + \frac{1}{\kappa_p} + \frac{\kappa}{\kappa_n}}. \quad (3.3)$$

We multiply the dimensionless transconductance thus computed by  $\frac{I_B}{2U_T}$  to get the actual transconductance, since  $I_{DS}$  in each differential arm is  $\frac{I_B}{2}$ .

The  $W$ ,  $S$ , and  $G$  transistors of each differential arm may be regarded as a single transistor with I-V characteristics given by

$$I \propto e^{-(v_S - gv_W)/U_T}. \quad (3.4)$$

By following the steps outlined by Mead [2], we can easily derive that

$$i_{OUT} = I_B \tanh\left(\frac{g(v_+ - v_-)}{2U_T}\right), \quad (3.5)$$

where  $g$  is given by Eq. (3.3).

### 3.2.3 Bump Linearization

Bump linearization is a technique for linearizing a tanh and extending the linear range of a subthreshold differential pair [26]. We shall first explain how it works for the simple differential pair; then, we shall extend this explanation to our amplifier in a straightforward fashion.

A bump differential pair has, in addition to its two outer arms, a central arm containing two series-connected transistors [23]. The current through the transistors in the central arm is a bump-shaped function of the differential voltage, so we call these transistors *bump transistors*. Thus, the differential output current from the outer two arms,  $I$ , is the usual tanh-like function of the differential voltage,  $V$ , except for a region near the origin, where the bump transistors steal current. By ratioing the  $W/L$  of the bump transistors to be



$w$  with respect to the transistors in the outer arms, we can control the properties of this I–V curve. A small  $w$  will essentially leave it unchanged. A large  $w$  will cause a flat zone near the origin, where there is current stealing. The larger the  $w$ , the larger the width and flatness of the zone. At intermediate values of  $w$ , the expansive properties of the curve due to the bump compete with the compressive properties of the curve due to the tanh, and a curve that is more linear than is a tanh is obtained. At  $w = 2$ , the curve is maximally linear.

For a simple subthreshold bump amplifier with bump scaling  $w$ , the differential output current can be shown to be

$$i_{out} = \frac{\sinh x}{\beta + \cosh x}, \quad (3.6)$$

where

$$\beta = 1 + \frac{w}{2}, \quad (3.7)$$

$$x = \frac{q\kappa(v_+ - v_-)}{kT}. \quad (3.8)$$

The bias current is assumed to be 1, without loss of generality. Simple calculus shows that the first and second derivatives of Eq. (3.6) are

$$\frac{di_{out}}{dx} = \frac{1 + \beta \cosh x}{(\beta + \cosh x)^2}, \quad (3.9)$$

$$\frac{d^2i_{out}}{dx^2} = \frac{\sinh x (\beta^2 - \beta \cosh x - 2)}{(\beta + \cosh x)^3}. \quad (3.10)$$

If we require that the  $i_{out}$ -vs.- $x$  curve have no points of inflection in it except at the origin, then it must always be convex or concave in the first or third quadrant; this requirement is necessary to ensure that there are no strange kinks in the I–V curve. In Eq. (3.10), we must then have

$$(\beta^2 - \beta \cosh x - 2) \leq 0 \quad (3.11)$$

for all  $x$ . Note that in deriving Eq. (3.11), we have used the facts that the denominator term of Eq. (3.10) is always positive, and that  $\sinh x$  changes sign at only the origin. The worst possible case for not meeting the constraint given by Eq. (3.11) occurs when  $\cosh x$  is at its minimum value of 1 at  $x = 0$ . If we set  $\cosh x = 1$  and solve the resulting quadratic

for  $\beta$ , we obtain

$$\beta \leq 2, \quad (3.12)$$

$$\Rightarrow w \leq 2. \quad (3.13)$$

Thus, at  $w = 2$ , we are just assured of satisfying this constraint. At  $w = 2$ , the  $i_{out}$ -vs.- $x$  curve is maximally linear: If we Taylor expand Eq. (3.6) at  $\beta = w = 2$ , we find that it has no cubic-distortion term. In comparison, the function  $\tanh x/2$ , which is to what Eq. (3.6) reduces when  $w = 0$  or  $\beta = 1$ , has cubic distortion.

$$\tanh \frac{x}{2} = \frac{x}{2} - \frac{x^3}{24} + \frac{x^5}{240} - \frac{17x^7}{40320} + \dots \quad (3.14)$$

$$\frac{\sinh x}{2 + \cosh x} = \frac{x}{3} - \frac{x^5}{540} + \frac{x^7}{4536} - \frac{x^9}{77760} + \dots \quad (3.15)$$

At  $x = 1$ , the  $\tanh$  function has cubic distortion of approximately 8%, as compared to the linearized  $\tanh$  function which has no cubic distortion whatsoever, but has only fifth-harmonic distortion of less than 1%. Thus, we have linearized the  $\tanh$ . We shall show later, in Section 3.5, that bump linearization is a particularly useful technique because it increases the linear range of an amplifier without increasing that amplifier's noise.

Our circuit topology in Figure 3.1 implements a wide-linear-range bump differential pair by ratioing the  $W/L$  of the the  $n$ FET B transistors to be  $w$  with respect to the  $W/L$  of the  $n$ FET GM transistors. However, the mathematical analysis of the circuit is identical to that of a simple bump differential pair if we replace the  $\kappa$  of Eq. (3.8) with the  $g$  of Eq. (3.3).

### 3.2.4 Experimental Data

In summary, from Eqs. (3.3) and (3.5), we get the transfer function of the amplifier *with the B transistors absent*:

$$I_{out} = I_B \tanh(V_d/V_L), \quad (3.16)$$

$$V_d = V_+ - V_-, \quad (3.17)$$

$$V_L = (2kT/q) \left( \frac{1 + 1/\kappa_p + \kappa/\kappa_n}{1 - \kappa} \right). \quad (3.18)$$

From Eqs. (3.3), (3.5), (3.6), (3.7), and (3.8), the transfer function of the overall amplifier has the form

$$I_{out} = I_B \frac{\sinh(2x)}{1 + w/2 + \cosh(2x)}, \quad (3.19)$$

where  $x = V_d/V_L$ . The  $W/L$  of the B transistors is  $w$  times the  $W/L$  of the GM transistors.

We fabricated our transconductance amplifier in a standard  $2\mu\text{m}$  CMOS  $n$ -well process, and obtained data from it. We have also used the amplifier in a working silicon cochlea [1,2]. Figure 3.4a shows experimental data for our amplifier for values of  $w = 0, 1.86,$  and  $66$ , fitted to Eq. (3.19). Note that, even at rather large  $w$ , the nonlinear characteristics are still gentle. This property ensures that even fairly large mismatches in  $w$  do not degrade the operation of the amplifier significantly. For  $w \approx 2$ , Figure 3.4b shows that the simple tanh fit of Eq. (3.16) is a good approximation to Eq. (3.19) if  $V_L \rightarrow (3/2)V_L$ —that is to say, from 1.16 V for  $w = 0$  to 1.7 V for  $w = 2$ . Considering the leading-order terms of Eqs. (3.14) and (3.15), the factor of  $3/2$  seems natural. However, we shall show, from the follower–integrator data of Section 3.4, that the tanh approximation is inadequate for large differential inputs, because the curve is more linear than is that of a tanh.

We verify Eq. (3.18) experimentally in Section 3.7.1. Since  $\kappa$  varies with the well-to-gate voltage, and consequently with the common-mode voltage, the verification is involved; we have relegated the details to the appendix.

### 3.3 Second-Order Effects

We shall now discuss several second-order effects in our amplifier. We begin by describing the common-mode characteristics.

#### 3.3.1 Common-Mode Characteristics

Below an input voltage of 1V, the well-to-source junction becomes forward biased, and the parasitic bipolar transistors, which are part of every well transistor, shunt the current of the amplifier to ground. Thus, as Figure 3.5a shows, the output current of the amplifier falls. Figure 3.5b illustrates the same effects, but from the perspective of varying the differential-

mode voltage, while fixing the common-mode voltage. In this figure, we can see that changes in  $\kappa$  increase the transconductance of the amplifier as the common-mode voltage is lowered. The increase is exhibited as a rise in the slope at the origin. At very low common-mode voltages, at a particular differential voltage, the input voltage for one arm or the other falls below 1V, and the bipolar transistors in that arm begin to shunt the current to ground. The lower the common-mode voltage, the smaller the differential voltage at which shunting begins. Thus, at low common-mode voltages the current starts to fall at small magnitudes of differential voltage.

We clarify the bipolar effect in Figure 3.6: Figure 3.6a shows a vertical crosssection of a well transistor in an  $n$ -well process; Figure 3.6b shows that the equivalent circuit of this well transistor contains two parasitic bipolar transistors. Typically, the well-to-source and well-to-drain junctions are always reverse biased, so that these bipolar transistors are turned off. For our amplifier, and in most cases, the source-to-drain voltage is sufficiently positive that the bipolar transistor at the source is the one that is turned on, if any is, whereas the one at the drain is hardly turned on. Thus, in Figure 3.6c, we have indicated the bipolar transistor at only the source. The bipolar effect is described in quantitative detail in Section 3.7.2.

Typically, we operate the amplifier at a common-mode voltage of about 3V, where small dc offsets do not significantly affect its transconductance, and where the action of the bipolar transistors is negligible. When the bipolar transistors do turn on, there is no danger of latchup, because the current that is fed to the substrate is at most the tiny subthreshold bias current of the amplifier. Our input operating range of 1V to 5V is about the same as that of a simple subthreshold  $n$ FET differential amplifier. These amplifiers also show transconductance changes, due to  $\kappa$  changes, that are most abrupt at low common-mode voltages.

As the common-mode input voltage of our amplifier is decreased, the well-to-gate voltage falls, the depletion region beneath the channel of the transistor shrinks,  $\kappa$  decreases, the transconductance of the amplifier rises from Eq. (3.3), and, at a given differential voltage, there is more current. Thus, the data of Figure 3.5a show that the current rises as the common-mode voltage is decreased from 5V to 1V. Note also that the transconductance changes are greatest near 1V where the depletion region is thin, and are least near 5V, where the depletion region is thick. The  $\kappa$  changes are described in quantitative detail in

## Section 3.7.1.

### 3.3.2 Bias-Current Characteristics

Figure 3.7a shows the bias-current characteristics of our amplifier as a function of the bias voltage  $V_B$ . The amplifier is capable of operating with little loss in common-mode range from bias currents of pA to  $\mu\text{A}$ . Figure 3.7b illustrates that the linear range begins to increase at above-threshold current levels, because of an increase in the  $I/g_m$  ratio of a transistor at these levels. That is to say, the characteristic scaling voltage in Eq. (3.18) begins to increase above  $2kT/q$ .

Note that the changes in  $\kappa$  observed with bias current and common-mode voltage are not unique to our amplifier: They occur in every subthreshold MOS transistor. By measuring the slope of the I–V curve in a simple  $n\text{FET}$  differential pair, we obtained changes in  $\kappa$  with common-mode voltage and with bias current. Figure 3.8 shows these data. Note that  $\kappa$  changes are most abrupt at low common-mode voltages—that is to say, at low gate-to-bulk voltages;  $\kappa$  also decreases with increasing bias current.

### 3.3.3 Gain Characteristics

The voltage gain of the amplifier is determined by the ratio of its transconductance  $g_m$  to its output conductance  $g_o$ . When  $w = 0$ , the transconductance is  $I_B/V_L$ . The output conductance is  $I_B/2V_0$ , where  $V_0$  is the effective Early voltage of the output M transistors in Figure 3.1. The effective Early voltage of the output M transistors is the parallel combination  $V_0^n V_0^p / (V_0^n + V_0^p)$ , where  $V_0^n$  and  $V_0^p$  are the Early voltages of the  $n$  and  $p$  output transistors, respectively. When  $w = 2$ ,  $g_m$  is given by  $I_B/(3/2V_L)$ , since the linear range increases by a factor of  $3/2$ . The value of  $g_o$  is given by  $I_B/3V_0$ , as the output current in each arm falls from  $I_B/2$  to  $I_B/3$ . Thus, effectively, the  $w = 2$  case corresponds to the  $w = 0$  case, with  $I_B$  being replaced by  $2I_B/3$ . So the gain is unchanged, because  $g_m$  and  $g_o$  change proportionately. Independent of whether  $w = 0$  or  $w = 2$ , the gain is  $2V_0/V_L$ . Figure 3.9a shows that the conclusions of the previous paragraph are borne out by experimental data. As the common-mode voltage is lowered, the gain increases because of the increasing transconductance, or decreasing  $V_L$ . The  $w = 0$  and  $w = 2$  amplifiers have almost identical gain. Figure 3.9b illustrates that, as a function of bias current, the gain initially rises, because the Early voltage increases with current. As the bias current starts

to go above threshold, however,  $V_L$  drops faster than  $V_0$  increases, and the gain starts to fall. From Figure 3.7b and Figure 3.9b, we see that the location of the gain peak is at a bias current (10 nA) where the linear range starts to change significantly, as we would expect. Figure 3.9b shows, however, that the  $w = 0$  and  $w = 2$  cases do not have identical gains at all bias currents, although the gains are similar. We attribute these small differences to differences in  $g_m$  and  $g_o$  at bias-current levels of  $I_B/2$  versus  $I_B/3$ .

For the amplifier for which data were taken, the output transistors had a channel length of  $16\mu\text{m}$  in a  $2\mu\text{m}$   $n$ -well Orbit analog process. If higher gain is desired, these channel lengths should be increased, or the positive and negative output currents can be cascoded via  $p$ FET and  $n$ FET transistors respectively.

### 3.3.4 Offset Characteristics

A current offset of  $i_k$  can be compensated for by a voltage offset of  $v_l = i_k/g_m$ , where  $g_m$  is the transconductance of the  $i_K - v_L$  relation ( $i_K$  and  $v_L$  are arbitrary variables). Therefore, if the fractional current offset caused by a threshold or geometry mismatch is  $i_k/I_K = \delta$ , then the voltage offset  $v_l$  is  $i_k/g_m = (I_K/g_m)(i_k/I_K) = (I_K/g_m)\delta$ . The  $I_K/g_m$  ratio is thus the scale factor that converts percentage mismatches to voltage offsets. A transconductance amplifier has an  $I_B/g_m$  ratio of  $2U_T/g$ . Thus, the same percentage mismatch results in a larger voltage offset for an amplifier with a lower  $g$ . This general and well-known result causes the lowering of transconductance to be associated with an increase in voltage offset. However, we show next that, although this increase in voltage offset is fundamental and unavoidable, certain transistor mismatches matter more than do others. By designing the amplifier carefully, such that more area is expended where mismatches are more crucial, we can minimize the offset. In our amplifier, mismatches may arise in the two  $n$ FET GM-M mirrors, in the  $p$ FET M mirror, or between the W, S, and GM transistors in the two arms. In a first-order analysis, the B transistors do not affect the voltage offset, except that  $g$  is replaced by  $(2/3)g$ . We shall therefore start our analysis with the case of  $w = 0$ , and then extend our analysis to the  $w = 2$  case.

Suppose the net mismatch due to all mirror mismatches is such that  $i_+/i_- = \frac{I_B}{2}(1 + \frac{\delta_M}{2})/\frac{I_B}{2}(1 - \frac{\delta_M}{2}) \approx 1 + \delta_M$ . The mismatch in currents may be referred back to the input as a voltage offset of  $+V_M/2$  on one input, and a voltage offset of  $-V_M/2$  on the other input:

$$\begin{aligned} \frac{V_M}{2} &= \left( \frac{I_K}{g_m} \right) \frac{\delta_M}{2} = \left( \frac{\frac{I_B}{2}}{\frac{g I_B}{2 U_T}} \right) \frac{\delta_M}{2} \\ \Rightarrow V_M &= \delta_M \frac{U_T}{g}. \end{aligned} \quad (3.20)$$

Since  $\frac{U_T}{1-\kappa}$  is the  $I_K/g_m$  ratio of the W transistors, a mismatch of  $\delta_W$  between those transistors introduces a voltage offset of  $\frac{U_T}{1-\kappa} \delta_W$  on the well inputs. Because  $\frac{U_T}{\kappa_n}$  is the  $I_K/g_m$  ratio of the S transistors, a mismatch of  $\delta_S$  between those transistors results in a voltage offset of  $\frac{U_T}{\kappa_p} \delta_S$  on their gates. This voltage offset is fed back to the sources of the W transistors and is amplified by  $1/(1-\kappa)$  when referred back to the those transistors' well-inputs. Similarly, a mismatch of  $\delta_G$  between the G transistors causes a voltage offset of  $\frac{U_T}{\kappa_n}$  on the gates of the GM transistors that is amplified by  $\kappa/(1-\kappa)$  when referred back to the well inputs. The total offset,  $V_{of}$ , is just the sum of the voltage offsets introduced by all the mismatches, and is given by

$$\begin{aligned} V_{of} &= U_T \left( \frac{1}{g} \delta_M + \frac{1}{1-\kappa} \delta_W + \frac{1}{\kappa_p} \frac{1}{1-\kappa} \delta_S \right) + \\ &U_T \left( \frac{1}{\kappa_n} \frac{\kappa}{1-\kappa} \delta_G \right). \end{aligned} \quad (3.21)$$

If we use the expression from Eq. (3.3) to substitute for  $g$ , then

$$\begin{aligned} V_{of} &= \frac{U_T}{1-\kappa} \left( \left( 1 + \frac{1}{\kappa_p} + \frac{\kappa}{\kappa_n} \right) \delta_M + \delta_W \right) + \\ &\frac{U_T}{1-\kappa} \left( \frac{1}{\kappa_p} \delta_S + \frac{\kappa}{\kappa_n} \delta_G \right). \end{aligned} \quad (3.22)$$

We notice that the greatest contributor to the offset is the mirror mismatch  $\delta_M$ . Thus, it is important that all mirror transistors in the amplifier be big. The matching of the S transistors is more important than is the matching of the W transistors since  $1/\kappa_p > 1$ . The matching of the GM transistors is more important than is that of the W transistors if  $\kappa/\kappa_n > 1$ , which is usually the case; for  $\kappa/\kappa_n$  ratios exceeding  $1/\kappa_p$ , it is also more important than the matching of the S transistors. The amplifier is thus laid out with big

$p$ FET M transistors, moderate GM transistors, moderate  $n$ FET M transistors (to match the GM transistors), moderate S transistors and small W transistors. It is interesting that the transistors that matter the least for matching are the input transistors.

If the B transistors are present, a similar analysis shows that the matching of the M transistors becomes even more important, because the  $g$  in Eq. (3.21) is replaced by  $(2/3)g$ . In Eq. (3.22), we then have  $\delta_M \rightarrow (3/2)\delta_M$ .

The sizes of the transistors that we used for the amplifier were 12/12 for the W transistors, 12/12 for the bias transistor, 29/12 for the S transistors, 14/16 for the GM and  $n$ FET M transistors, and 26/16 for the  $p$ FET M transistors. The total dimensions of the amplifier were  $85\mu\text{m} \times 190\mu\text{m}$  in a  $2\mu\text{m}$  process. Our random offset is about 5 to 10 mV.

Due to Early voltage effects, the cascaded gains of the GM–M mirror and the  $p$ FET M mirror in the positive-output-current path, exceed those of the GM–M mirror in the negative-output-current path. Hence, with  $V_{OS} = V_{DD}$ , the amplifier typically has a systematic positive voltage offset that is on the order of 10 to 20 mV. The voltage  $V_{OS}$  is operated approximately 0.5 mV below  $V_{DD}$ , to cancel this offset. We have also built automatic offset-adaptation circuits to control the offset of our amplifiers; we shall not elaborate on those schemes here.

The data of Figure 3.10a show the offset voltage of a follower built with this amplifier as a function of the  $V_{OS}$  voltage. The two current curves correspond to two different common-mode voltages. The slope of the input–output relation is the ratio of the source transconductance at the  $V_{OS}$ -input  $g_s$  to the transconductance of the overall amplifier  $g$ . At high common-mode voltages, the offset is more sensitive to the  $V_{OS}$  voltage, because  $g$  decreases with common-mode voltage. Figure 3.10b shows that the offset voltage is less sensitive to the  $V_{OS}$  voltage at high bias-current levels, because  $g_s$  decreases faster than does  $g$  with bias current.

### 3.4 Follower–Integrator Characteristics

One of the most common uses of transconductance amplifiers is in building filters. Thus, it is important to study the properties of a follower–integrator. The follower–integrator is the simplest filter that can be built out of a transconductance amplifier; it is a first-order, lowpass filter. Figure 3.11a shows the basic configuration. The voltage  $V_T$  is identical to  $V_B$



in Figure 3.1, and, with the capacitance  $C$  determines the corner frequency (CF) of the filter. Figure 3.11b shows the dc characteristics of such a filter built with our amplifier. Except for very low input voltages, where the parasitic bipolar transistors shunt the amplifier's current to ground, the output is a faithful replica of the input. Figure 3.12 reveals the effects of the parasitic bipolar transistors in detail. At input voltages that are within the normal range of operation of the amplifier (1V to 5V), such as those shown in the top portion of the figure, the output of the follower is a simple lowpass-filtered version of the input. In the bottom portion of the figure, we see that, as long as the input voltage is below about 0.7 V, the amplifier's bias current is shunted to ground, and the output voltage barely changes. The constancy of the output voltage occurs because there is no current at the output of the amplifier to charge or discharge the capacitor such that it barely changes. When the input voltage is outside this range, the output voltage tries to follow the input voltage by normal follower action. We show these data to illustrate the consistency of our earlier results with the behavior of the follower-integrator; we do *not* recommend operation of the filter in this regime. We shall now describe more useful linear and nonlinear characteristics of the follower-integrator in detail.

### 3.4.1 Linear and Nonlinear Characteristics

Figure 3.13a and Figure 3.13b show data for the gain and phase characteristics of a follower-integrator. The phase curve is much more sensitive to the presence of parasitics than is the gain curve, which remains ideal for a much wider range of frequencies. The higher sensitivity of the phase curve to parasitics is reasonable, because the effect of a parasitic pole or zero on the gain is appreciable only at or beyond the pole or zero frequency location. The effect of the same pole or zero on the phase is significant a full decade before the frequency location of the pole or zero.

We have studied the origin of the parasitic capacitances in detail, but we shall not delve into this subject here. The parasitics are caused by the large sizes of transistors that we use to reduce our  $1/f$  noise and offset; the dominant parasitics are the well-to-drain capacitance of the W transistor, which causes a right-half-plane zero, and the gate-to-bulk capacitance of the GM transistors, which causes a left-half-plane pole. Rather than make detailed models of the parasitics, we model their effect by simply having a different corner frequency (CF) for the gain and phase curves. As Figure 3.13a and Figure 3.13b show, the phase CF is

slightly lower than the gain CF, because of the excess phase due to the parasitics.

It is possible to reduce the influence of parasitics in our amplifier by having the  $n$ FET GM-M mirrors be attenuating. Then, the differential-arm parasitics are at higher frequencies, compared with the CF of the filter. Another alternative is to use a larger output capacitor. However, for cochlear-filtering applications, for which this amplifier is mainly intended, there is a steep amplitude rolloff beyond the CF of the lowpass filter, and fine phase effects are not important at these frequencies. In addition, the second-order filter, of which this filter is a part, is only an approximation to the more complicated filtering that occurs in a real cochlea. Thus, we have not expended energy optimizing the parasitics to get an ideal first-order filter.

Figure 3.13c shows the first, second, and third harmonic rms output amplitudes when the input rms amplitude is 1V (peak-to-peak of 2.8V). The data were collected with an EGG3502 lockin amplifier. Because of the wide linear range of our amplifiers, there is little distortion even at these large amplitudes. At frequencies that are within a decade of the CF, the second harmonic is less than  $4 \times 10^{-2}$  the amplitude of the first harmonic. The third-harmonic distortion is negligible at these frequencies. The total harmonic distortion is less than 4%.

Figure 3.14 plots the relative amplitude distortion—that is to say, the ratio of the magnitude of the second and third harmonic amplitude to that of the first. Note that the  $X$ -axis is plotted in multiples of the CF, and that we are uninterested in effects more than a decade beyond the 1 point. The chief features of interest are that the addition of the bump transistors reduces third-harmonic distortion as we expect from Eq. (3.14) and Eq. (3.15). However, it also increases the second-harmonic distortion at frequencies just below the CF, for reasons unknown to us. Usually, second-harmonic distortion occurs along with dc shifts. Figure 3.15 shows these shifts for an input signal with an rms input amplitude of 1V. These shifts exert only a mild influence in cochlear designs, because input-signal amplitudes far beyond the CF are small due to successive filtering from prior stages. The dc shifts are not significant for small inputs. The dc shifts are observed in OTA-C follower-integrators as well; they are typically positive for amplifiers with  $n$ FET differential pairs and negative for amplifiers with  $p$ FET differential pairs.

Figure 3.16a shows the shifts in gain and phase CF for the  $w = 0$  and  $w = 2$  cases as a function of the input rms amplitude. Note that the gain and phase CF shifts are similar.

The addition of the  $B$  transistors decreases the amount of CF shift due to the linearization of the  $\tanh$ . Figure 3.16b shows the shifts in CF as a function of the input dc voltage to the follower–integrator. As we expect from prior data on the amplifier (Figure 3.5a), the CF shifts track the shifts in transconductance with dc input voltage. The tracking is seen for gain and phase CF curves, and for the  $w = 0$  and  $w = 2$  cases.

## 3.5 Noise and Dynamic Range

The largest signal that a filter can process without excessive distortion is determined by the linear range of that filter. The smallest signal that a filter can process is one whose rms amplitude is just above the filter’s input-referred noise. The dynamic range of a filter is given by the ratio of the power of the largest signal to the power of the smallest signal. We have already discussed linear range and distortion in the follower–integrator. Now, we focus on the other half of the story: noise in the follower–integrator. After we compute and measure the noise, we can tell whether there has been an improvement in the dynamic range of the follower–integrator. Since there are no free lunches in nature, we also want to discover what price we have paid in our design, in terms of the increase in power and area. We shall discuss noise and dynamic range in our design in Sections 3.5.1–3.5.3. We shall discuss the dynamic range of capacitive-divider schemes in Section 3.5.4, since those schemes bear similarity to our technique of using the well as an input.

### 3.5.1 Theoretical Computations of Noise in the Amplifier and Follower–Integrator

We now compute the noise in a follower–integrator built with our amplifier. We tie the  $v_+$  and  $v_-$  to a common constant voltage source, and the output to another constant voltage source. Then, we replace each of the 13 transistors in Figure 3.1 with its small-signal equivalent circuit. We introduce a noise current source between each transistor’s drain and source terminals in the small-signal equivalent circuit. For each noise source, we compute the ac transfer function between its current and the differential output current. We sum the noise contributions from each of the 13 sources incoherently; that is to say, the square of the net output current noise is the sum of the squares of the current noise from each source. The input-referred voltage noise per unit bandwidth is the output current noise per unit

bandwidth divided by the transconductance of the amplifier. The total voltage noise is the voltage noise per unit bandwidth integrated over the bandwidth of the follower–integrator. The bandwidth of the follower–integrator is determined by the transconductance of the amplifier and the capacitance. If the amplifier is used in a system, where the bandwidth is determined by some other part of the system, then this bandwidth determines the interval of integration. The parasitic capacitances in the amplifier set an upper bound on the maximum possible bandwidth.

Although there are 13 transistors in Figure 3.1, we do *not* get 13 transistors' worth of current noise at the output. Our calculations will show that we get about 5.3 transistors' worth of current noise. This figure is only slightly higher than the 4 transistors' worth of noise obtained from a 5-transistor ordinary transconductance amplifier (OTA). The reduction in noise occurs for three reasons. First, for each noise source, there is a total or partial cancellation of its noise current at the output, due to opposing contributions from the two circuit arms. As an example, the noise current from the bias transistor in Figure 3.1 (with gate voltage  $V_B$ ) makes no contribution to the output noise current, because it branches into equal portions in the two differential arms, which cancel each other at the output. Similarly, other noise sources, such as those from the B transistors, contribute no noise. The sources from the GM transistors have a partial noise cancellation. Second, some of the noise current from each source is prevented from contributing to the output by local shunting circuit impedances. As an example, the noise currents from the W transistors contribute only 0.16 transistors' worth of current noise to the output because most of the noise current gets shunted by the W transistors themselves. Third, when we compute the incoherent noise average across many sources, a given source's contribution to the net noise is proportional to the square of its fractional current gain; that is to say, to the square of the output noise current divided by source current. Therefore, weak contributions are weakened further.

If we define  $\alpha_B$ ,  $\alpha_S$ ,  $\alpha_W$ ,  $\alpha_G$ , and  $\alpha_M$  to be the current gain between the output current of the amplifier and the input drain-to-source noise current of a B,S,W,G, or M transistor, respectively, we can show that

$$\alpha_B = 0, \tag{3.23}$$

$$\alpha_S = \frac{\kappa_n}{\kappa_n + \kappa_n \kappa_p + \kappa \kappa_p}, \quad (3.24)$$

$$\alpha_W = \frac{\kappa_n \kappa_p}{\kappa_n + \kappa_n \kappa_p + \kappa \kappa_p}, \quad (3.25)$$

$$\alpha_G = \frac{\kappa_n + \kappa_n \kappa_p}{\kappa_n + \kappa_n \kappa_p + \kappa \kappa_p}, \quad (3.26)$$

$$\alpha_M = 1. \quad (3.27)$$

Since each transistor has the same dc current flowing through it (i.e.  $I_B/2$  in the  $w = 0$  case, or  $I_B/3$  in the  $w = 2$  case), the magnitude of the noise current source across each transistor is the same. Thus, the output-current noise of the amplifier is the noise current due to one transistor times an effective number of transistors  $N$ , where,  $N$  is given by

$$N = 2\alpha_S^2 + 2\alpha_W^2 + 2\alpha_G^2 + 4\alpha_M^2. \quad (3.28)$$

For our amplifier with  $\kappa \approx 0.85$ ,  $\kappa_n \approx 0.7$ , and  $\kappa_p \approx 0.75$ , the numbers work out such that  $N = 5.3$ . The dominant contribution to  $N$  comes from the four M transistors which contribute a whole transistor each. The two G transistors contribute 0.865 transistors. The two S transistors contribute 0.28 transistors. The two W transistors contribute 0.16 transistors. The B transistors and the bias transistor contribute no noise. The most noise-free linearization techniques, in decreasing order of merit, are bump linearization, the use of the well as an input, source degeneration, and gate degeneration. Bump linearization is the only technique of the four that adds no noise whatsoever. Note that, depending on the circuit configuration, the relative noise efficiencies of the use of the well as an input, source degeneration, and gate degeneration may vary. For example, in a well-input amplifier with source degeneration but no gate degeneration,  $\alpha_W = \alpha_S = \kappa_n/(\kappa + \kappa_n)$ . In the latter case, the use of the well as an input and gate degeneration each contribute 0.41 transistors' worth of noise.

The magnitudes of the individual noise current sources depend on the dc current flowing through the transistor, and are well described by a white-noise term for low subthreshold currents [1]. At high subthreshold currents, there is also a  $1/f$ -noise term. Our experimental data in Section 3.5.3 reveal the amount of the  $1/f$  contribution; we shall model this term empirically, because no satisfactory theory for  $1/f$  noise currently exists.

In the first paragraph of this section, we explained the procedure for calculating the

noise. We shall now perform the calculations. As usual, we begin by analyzing the case for  $w = 0$  and then extend our analysis to the  $w = 2$  case. The output-current noise of the amplifier  $\overline{i_o^2}$  is given by

$$\overline{i_o^2} = \int_{f_l}^{\infty} N \left( 2q \left( \frac{I_B}{2} \right) + \frac{K(I_B/2)^2}{f} \right) df, \quad (3.29)$$

where the first and second terms in the integral correspond to white noise and  $1/f$  noise, respectively;  $I_B$  is the bias current, and  $K$  is the  $1/f$  noise coefficient. We also assume that there is low-frequency adaptation in the amplifier, so that frequencies below  $f_l$  are not passed through. This assumption is necessary if we are to prevent the  $1/f$  noise from growing without bound at low frequencies. In our amplifier, we have an offset-adaptation circuit that keeps  $f_l$  around 1 Hz. Also, typically the  $K$  for  $p$ FETs is smaller than is that for  $n$ FETs, and scales inversely with the channel area of the transistor. However, we assume a transistor-invariant  $K$ , for simplicity.

The corner frequency of the follower-integrator  $f_c$  is

$$f_c = \frac{I_B}{2\pi CV_L}, \quad (3.30)$$

so from Eq. (3.29), the input-referred voltage noise  $\overline{v_i^2}$  is

$$\begin{aligned} \overline{v_i^2} &= \int_{f_l}^{\infty} \frac{N \left( qI_B + \frac{KI_B^2}{4f} \right)}{(I_B/V_L)^2} \left( \frac{1}{1 + (f/f_c)^2} \right) df \\ &= \left( \frac{NqV_L^2}{I_B} \right) \frac{\pi f_c}{2} + \frac{NKV_L^2}{8f} \ln \left( 1 + (f_c/f_l)^2 \right) \\ &= \frac{NqV_L}{4C} + \frac{NKV_L^2}{8} \ln \left( 1 + \left( \frac{I_B}{2\pi f_l CV_L} \right)^2 \right). \end{aligned} \quad (3.31)$$

In evaluating Eq. (3.31), we computed two integrals:

$$\int_0^{\infty} \frac{dx}{1+x^2} = \frac{\pi}{2}, \quad (3.32)$$

$$\int_{f_i}^{\infty} \frac{dx}{x(1+x^2)} = \frac{1}{2} \ln\left(1 + \frac{1}{f_i^2}\right). \quad (3.33)$$

Note that the  $1/f$  noise rises with bias current because of the increasing bandwidth. The magnitude of the  $1/f$  noise depends on the bandwidth; that is to say, it depends on  $I_B/CV_L$ . The white noise is current invariant, because the noise per unit bandwidth and the bandwidth scale as  $1/I_B$  and  $I_B$ , respectively. The white noise increases linearly with  $V_L$ , whereas the  $1/f$  noise increases quadratically with  $V_L$ .

### 3.5.2 Theoretical Computations of Dynamic Range

The dynamic range  $D_R$  is defined to be the ratio of rms input power in a signal with amplitude  $V_L$  to the input-referred noise power; this definition is implicitly based on our willingness to accept the distortion present at this amplitude, which from Figure 3.13 is seen to be reasonable. If we want to be more conservative with respect to distortion, then we simply scale  $V_L$  by the necessary fractional amount. So, we have from Eq. (3.31) that

$$\begin{aligned} D_R &= \frac{V_L^2/2}{v_i^2} \\ &= \frac{V_L^2/2}{\frac{NqV_L}{4C} + \frac{NKV_L^2}{8} \ln\left(1 + \left(\frac{I_B}{2\pi f_i CV_L}\right)^2\right)} \\ &= \frac{1}{\frac{Nq}{2CV_L} + \frac{NK}{8} \ln\left(1 + \left(\frac{I_B}{2\pi f_i CV_L}\right)^2\right)}. \end{aligned} \quad (3.34)$$

In Eq. (3.34), the white-noise term is typically much larger than the  $1/f$  term, because of the small value of  $K$  in our large, mostly  $p$ FET transistors, because frequencies below 1Hz are filtered out by offset adaptation, and because white noise is still relatively high at the low subthreshold current levels. Even at high bias currents, where the  $1/f$  noise appears to be important on a log-log plot of noise amplitude versus frequency, the net area under the plot is dominated by white noise on a linear-linear plot. Thus, from Eq. (3.34), the dynamic range is nearly

$$D_R = \frac{2CV_L}{Nq}. \quad (3.35)$$

We see from Eq. (3.31) that the white-noise power increases like  $V_L$ . The maximum signal

power increases like  $V_L^2$ . Thus, if white noise dominates, wide linear range implies more dynamic range, as Eq. (3.35) predicts. The noise per unit bandwidth scales like  $V_L^2$ , but the bandwidth scales like  $1/V_L$  such that the overall noise scales like  $V_L$ . If bandwidth is to be preserved, then power proportional to  $V_L$  has to be expended, according to Eq. (3.30). After the bandwidth has been restored to its original value, however, the noise still remains at a value proportional to  $V_L$ . The noise remains at the same value because thermal noise is current invariant. The current invariance arises because the noise per unit bandwidth and the bandwidth scale like  $1/I_B$  and  $I_B$ , respectively. The extra dynamic range has been earned at the price of an increase in power.

We see from Eq. (3.31) that the  $1/f$ -noise power increases like  $V_L^2$ . The maximum signal power increases like  $V_L^2$ . Thus, if  $1/f$  noise dominates, wide linear range does not affect the dynamic range. The noise per unit bandwidth scales like  $V_L^2$ , and the bandwidth scales like  $1/V_L$ . If bandwidth is to be preserved, then power proportional to  $V_L$  has to be expended, according to Eq. (3.30). After the bandwidth has been restored to its original value, however, the noise increases like  $V_L^2$  because  $1/f$  noise is not current invariant, but rather is bandwidth invariant. The bandwidth invariance arises because the noise per unit bandwidth depends on only  $V_L^2$  and is current invariant. So, the total noise over a given bandwidth depends on only that bandwidth. The advantage of linearity in such a situation is merely that the signal and noise levels have been scaled to be suited to inputs that themselves have a higher noise floor and large amplitudes. There is also an area cost associated with extra dynamic range: To reduce  $1/f$  noise and offset, we must use transistors with large areas.

If  $w = 2$ , the analysis for  $\overline{v_i^2}$  and  $D_R$  proceeds similarly. For the currents through the transistors,  $I_B/2 \rightarrow I_B/3$ . For the bandwidth and linear range,  $V_L \rightarrow (3/2)V_L$ . If a  $w = 0$  and a  $w = 2$  follower-integrator have the same bandwidth, then we can show that they have identical input-referred noise spectra. For the bandwidths for the  $w = 2$  and  $w = 0$  cases to be equal, however, the bias current for the  $w = 2$  case has to be increased by a factor of  $(3/2)$  over that for the  $w = 0$  case. Theoretically, the dynamic range of the  $w = 2$  case is  $(3/2)^2$  times the dynamic range of the  $w = 0$  case because of the increase in linear range. In practice, however, if the linear range is already large in the  $w = 0$  case, the increased linearity in the  $w = 2$  case does not reduce distortion further. The distortion is typically limited by some other mechanism. For example, in our amplifier the dominant distortion is due to  $\kappa$  shifts caused by the nonlinear well-to-channel capacitance.



Nevertheless, the increased linearity does reduce third-harmonic distortion and CF shifts with input amplitude, as shown in Figure 3.14b and Figure 3.16b.

### 3.5.3 Experimental Noise Curves

Figure 3.17a shows noise spectra at low bias-current levels for a follower-integrator with a capacitance  $C = 1.02$  pF. The data were taken with a HP3582A spectrum analyzer. From Eq. (3.29), we would expect white or thermal noise to be dominant at low bias currents. We observe from the figure that, even at the lowest frequencies, no  $1/f$  noise is visible. We were able to fit the data with lowpass-filter transfer functions as shown. Note that, for the low bias currents of Figure 3.17a, where  $1/f$  noise is hard to discern, we did not use any  $1/f$  terms in our fit. The terms in the integral of Eq. (3.31) predict that the noise spectra reveal relatively more  $1/f$  noise at high bias current levels because the white-noise term decreases and the  $1/f$  term remains roughly constant. The data of Figure 3.17b illustrates that this prediction is approximately borne out. However, we were able to empirically fit the voltage noise per unit bandwidth  $\overline{v_{if}^2}$  more accurately by a term of the form

$$\overline{v_{if}^2} = \left( \frac{K_B}{f^n} + A \right) \left( \frac{1}{1 + (f/f_c)^2} \right). \quad (3.36)$$

Figure 3.18a shows a typical fit to the data in more detail. From the first line of Eq. (3.31), we would expect  $K_B = V_L^2 K/4$ ,  $n = 1$ , and  $A = V_L^2 Nq/I_B$ . Since  $K_B$  and  $n$  are empirical, they do not yield substantial theoretical information, although they are useful practically. In the following paragraph, we show how to extract the value of  $N$  of Eq. (3.35) from the value of  $A$ .

From the value of  $f_c$  obtained from the fit to the data, from our knowledge of  $C$ , from measurements of  $I_B$ , and from Eq. (3.30) we obtain  $V_L$ . Given  $V_L$  and the fit parameter  $A$ , we obtain  $N$ , the effective number of transistors contributing shot noise. Figure 3.18b shows a plot of  $N$  versus the bias current  $I_B$ . We observe that  $N$  is roughly 7.5 in subthreshold, and decreases as the bias current goes above threshold and space-charge smoothing sets in. The value of  $N$  in subthreshold is within a factor of 1.4 of our theoretical prediction of 5.3. Above threshold, the space-charge smoothing, that is to say, the modulation of the mobile charge concentration by the mobile charges themselves, reduces the noise to a value below what we would expect from shot noise.

Figure 3.19 shows a plot of how the  $K_B$  and  $n$  of Eq. (3.36) vary with bias current  $I_B$ . Since  $K_B = KV_L^2/4$ , part of the increase in  $K_B$  arises from the increase in  $V_L$  and part of it arises from the increase in  $K$ . It is also interesting that, as the bias current increases, the  $1/f$  noise power systematically rises from about 0.67 to about 0.95.

The noise measurements of Figure 3.17 through 3.19 were taken for an amplifier with  $w = 0$ . We also experimentally confirmed that the noise in a  $w = 2$  amplifier was identical to that in a  $w = 0$  amplifier of the same bandwidth.

### 3.5.4 Capacitive-Divider Techniques

Our use of the well as an input implicitly involves a capacitive-divider technique: The gate, surface potential, and well form three terminals of a capacitive divider. We chose the well as an input because coupling ratio of the well to the surface potential,  $1 - \kappa$ , is smaller than the coupling ratio of the gate to the surface potential,  $\kappa$ . The advantage of this implicit capacitive-divider scheme is that the divider is inherently part of the transistor; so, we exploit a parasitic capacitance rather than avoiding one. Also, no additional floating-gate adaptation circuits or control voltages are needed. The disadvantage of the technique is that the capacitive-divider ratio is fixed by the physical parameters of the process, and is slightly nonlinear. If the divider ratio is not as small as desired, we must use other circuit techniques like source degeneration, gate degeneration or bump linearization to obtain wider linear range. Luckily, in our circuit, the additional transistors used to widen the linear range do not increase the noise greatly, but they do cost more area. It is logical to ask whether we can do better in area consumption with circuits that have explicit capacitive dividers.

We shall discuss two simple schemes where capacitive dividers are explicitly used around OTA's. We assume that any floating-gate inputs of the amplifiers are held at a proper dc value by low-frequency adaptation circuits. We further assume that the adaptation circuits do not affect noise in the amplifier's transistors or in the circuit. In practice, this assumption may not be true of certain adaptive schemes.

Figure 3.20a shows a simple scheme. The voltage  $V_T$  determines the bias current in the OTA. In practice, parasitic capacitances between the output and input terminals of the OTA can hurt the design significantly. If  $V_L$  is the linear range of the OTA, and  $N$  is the effective number of noise-contributing transistors in the OTA, then it can be shown that the dynamic range  $D_R$  is

$$D_R = \frac{2 \left( C_{out} + \frac{C_1 C_2}{C_1 + C_2} \right) \left( \frac{C_1 + C_2}{C_1} \right) V_L}{Nq}. \quad (3.37)$$

The analysis leading to the previous equation is similar to that preceding Eq. (3.35). We assume that thermal noise dominates. From Eq. (3.37), we see that  $C_{out}$  needs to be moderately large. If not, any improvement in dynamic range over that of an OTA-C follower-integrator arises only at the expense of an extremely large value of  $C_2$ . For example, if  $C_{out}$  were 0, we would need  $C_2$  to be approximately 15 pF to get a dynamic range improvement of 15 over that of an OTA-C follower-integrator with 1pF.

Similarly, for the inverting configuration of Figure 3.20b, we get

$$D_R = \frac{2 \left( C_{out} + \frac{C_2(C_{in} + C_1)}{C_2 + C_{in} + C_1} \right) \left( \frac{C_2 + C_{in} + C_1}{C_2} \right) V_L}{Nq}. \quad (3.38)$$

Once again, we observe that  $C_{out}$  must be moderately large. If not, any improvement in dynamic range arises only at the cost of an extremely large value of  $(C_{in} + C_1)$ . This configuration also introduces an RHP zero. If the effects of this zero are to occur at frequencies well past the CF of the follower-integrator, then

$$C_{out} \left( \frac{C_2 + C_{in} + C_1}{C_2} \right) + C_{in} + C_1 \gg C_2. \quad (3.39)$$

Parasitic capacitances can also hurt this design significantly, especially if the explicit capacitors in the circuit are small.

Actually, the circuit of Figure 3.20b does not even need an OTA, as the reference input of the OTA is not really used. The OTA can be replaced by a two-transistor amplifier, but, in that case,  $V_L$  also should be replaced by  $V_L/2$ . Thus, from Eq. (3.35), as in a normal OTA,  $N$  is still effectively 4.

Theoretically, by making capacitive-divider ratios appropriately small, and by spending power, the dynamic range may be increased to values beyond that attained in our design. A floating-gate adaptation scheme combined with a two-transistor version of Figure 3.20b is being explored [30,31].

## 3.6 Conclusions

We conclude by summarizing our key findings:

1. If the amplifier's noise is predominantly thermal, then an increase in its linear range increases the follower-integrator's dynamic range. If the amplifier's noise is predominantly  $1/f$ , then an increase in its linear range has no effect on the follower-integrator's dynamic range. To preserve follower-integrator bandwidth, power consumption increases proportionately with an increase in the amplifier's linear range according to Eq. (3.30).
2. In subthreshold, the noise is predominantly due to thermal noise, even at high bias currents, where some  $1/f$  noise is present. The theory described in [1] accurately modeled our thermal noise. Empirical expressions in the paper modelled our  $1/f$  noise.
3. In subthreshold circuits where thermal noise dominates, a simple formula for the dynamic range of a follower-integrator is  $D_R = 2CV_L/Nq$ . The capacitance of the follower-integrator is  $C$ , the linear range of the amplifier is  $V_L$ , the charge on the electron is  $q$ , and the effective number of noise-contributing transistors in the amplifier is  $N$ . A more complicated formula that includes  $1/f$  noise is given by Eq. (3.34).
4. Experimentally, we obtained a dynamic range of 65.2 dB in a follower-integrator with a capacitance of 1pF. A signal with an input rms amplitude of 1V yielded 4% total harmonic distortion. The total measured noise of the follower-integrator was 0.55 mV. A simple OTA-C follower-integrator has a theoretical linear range of 75 mV, and a theoretical noise floor of 110  $\mu$ V. Thus, we obtained a dynamic range improvement of at least 8.5 dB over the OTA-C follower-integrator. In practice, due to offchip noise floors on the order of 0.5-1 mV, the improvement can be as much as 20 dB.
5. Bump linearization is our most efficient linearization technique, because it increases the linear range of our amplifier without increasing its noise.
6. Gate degeneration is a useful transconductance-reduction technique. It can be generalized to the notion of the current increase from one input degenerating another input. The technique could be useful in multiple-gate-input circuits [32].

7. When the well is used as an input, the gate must be operated at as low a voltage as possible in order to obtain maximum dc-input operating range.
8. Capacitive-divider techniques that widen the linear range bear similarity to our technique of using the well as an input. If appropriate attention is paid to capacitor sizing, parasitic capacitances, and floating-gate adaptation in these techniques, then they may yield dynamic range improvements similar to ours.
9. Changes in  $\kappa$ , the subthreshold exponential parameter, are due to changes in dc current and to changes in well-to-gate voltage. These two effects may be studied separately through the techniques described in the paper.

## Acknowledgements

We thank Lena Peterson for providing the data of Figure 3.8. We thank Paul Hasler and Bradley Minch for useful discussions. This work was supported by the Beckman Hearing Center, and by the Center for Neuromorphic Systems Engineering as part of the National Science Foundation Engineering Research Center Program.

## Bibliography

- [1] R. Sarpeshkar, R. F. Lyon, and C. A. Mead, "An Analog VLSI Cochlea with New Transconductance Amplifiers and Nonlinear Gain Control", *Proceedings of the IEEE Symposium on Circuits and Systems*, Atlanta, Vol. 3, pp. 292–295, May 1996.
- [2] R. Sarpeshkar, R. F. Lyon, and C. A. Mead, "Nonvolatile Correction of Q-offsets and Instabilities in Cochlear Filters", *Proceedings of the IEEE Symposium on Circuits and Systems*, Atlanta, Vol. 3, pp. 329–332, May 1996.
- [3] H. Khorramabadi and P.R. Gray, "High Frequency CMOS continuous time filters", *I.E.E.E. J. Solid State Circuits*, SC-19(6), pp. 939–948, 1984.
- [4] A. Nedungadi and T.R. Viswanathan, "Design of linear CMOS transconductance elements", *I.E.E.E. Trans.*, CAS-31(10), pp. 891–894, 1984.
- [5] Y. Tsvividis, Z. Czarnul, S.C. Fang, "MOS transconductors and integrators with high linearity", *Electronics Letters*, 22(5), pp. 245–246, 1986.
- [6] Z. Wang, and W. Guggenbuhl, "A voltage-controllable linear MOS transconductor using bias offset technique", *I.E.E.E. J. Solid State Circuits*, SC-22(3), pp. 357–365, 1987.
- [7] F. Krummenacher and N. Joehl, "A 4 MHz CMOS continuous time filter with on-chip automatic tuning", *I.E.E.E. J. Solid-State Circuits*, SC-23, pp. 750–758, 1988.
- [8] B. Nauta, and E. Seevinck, "Linear CMOS transconductance element for VHF filters", *Electronics Letters*, 25, pp. 448–450, 1989.
- [9] S. T. Dupuie and M. Ismail, "High Frequency CMOS Transconductors", in *Analogue IC Design: the current mode approach*, eds. C. Toumazou, F.J. Lidgley and D.G. Haigh, Peter Peregrinus Ltd. on behalf of IEEE, 1990.

- [10] P. Wu, R. Schaumann, "Tunable Operational Transconductance Amplifier with Extremely High Linearity over Very Large Input Range", *Electronics Letters*, 27(14), pp. 1254–1255, 1991.
- [11] M.C.H. Cheng, and C. Toumazou, "Linear Composite MOSFETs (COMFETs)", *Electronics Letters*, 27(20), pp. 1802–1804, 1991.
- [12] S. Szczepanski, J. Jakusz, and A. Czarniak, "Differential Pair Transconductor Linearisation via Electronically Controlled Current-Mode Cells", *Electronics Letters*, 28(12), pp. 1093–1095, 1992.
- [13] P.R. Gray and R.G. Meyer, *Analysis and Design of Analog Integrated Circuits*, pp. 183–186, John Wiley and Sons, New York, 1987.
- [14] G. Wilson, "Linearised Bipolar Transconductor", *Electronics Letters*, 28(4), pp. 390–391, 1992.
- [15] W. Chung, K. Kim, and H. Cha, "A Linear Operational Transconductance Amplifier for Instrumentation Applications", *IEEE Trans on Instrumentation and Measurement*, 41(3), pp. 441–443, 1992.
- [16] J. Ramirez-Angulo and E. Sánchez-Sinécio, "Programmable BiCMOS Transconductor for Capacitor-Transconductor Filters", *Electronics Letters*, 28(13), pp. 1185–1187, 1992.
- [17] W. Liu, *An Analog Cochlear Model: Signal Representation and VLSI Realization*, PhD. Thesis, John Hopkins University, Baltimore, Maryland, 1992.
- [18] L. Watts, D. A. Kerns, R. F. Lyon, and C.A. Mead, "Improved Implementation of the silicon cochlea", *IEEE Journal of Solid-State Circuits*, 27(5), pp. 692–700, May 1992.
- [19] X. Arreguit, "Compatible Lateral Bipolar Transistors in CMOS Technology: Model and Applications", *Ecole Polytechnique Federale de Lausanne DSc thesis*, These no. 817, 1989.
- [20] P. Furth and A.G. Andreou, "Linearised differential transconductors in subthreshold CMOS," *Electronics Letters*, 31(7), pp. 545–547, 30th March 1995.



- [21] I. E. Opris and G.T.A. Kovacs, "Large-signal subthreshold CMOS transconductance amplifier", *Electronics Letters*, 31(9), pp. 718–720, 27th April 1995.
- [22] R. F. Lyon, "Analog Implementations of Auditory Models", *DARPA Workshop on Speech and Natural Language*, Morgan Kaufmann Publishers:San Mateo CA, 1991.
- [23] T. Delbrück, "Bump Circuits for computing similarity and dissimilarity of analog voltages", CNS Memo 26, California Institute of Technology, May 24, 1993.
- [24] R. W. Landee, D. C. Davis, and A. P. Albrecht, *Electronic Designers Handbook*, pp. 3-18, pp. 3-34 to 3-38, McGraw-Hill Book Co.: N.Y., 1957.
- [25] C.A. Mead, *Analog VLSI and Neural Systems*, pp. 33-36, 67-82, Addison-Wesley Publishing Co.: Reading, MA, 1989.
- [26] R. F. Lyon, T. Delbrück, and C. A. Mead, "Circuits for Wide Input Range Analog Rectification and Correlation", U.S. Patent 5,319,268, June 7th. 1994.
- [27] R. Sarpeshkar, T. Delbrück, and C. Mead, "White Noise in MOS Transistors and Resistors", *IEEE Circuits and Devices*, 9(6), pp. 23–29, November 1993; contained in chapter 2 of this thesis.
- [28] R.F. Lyon and C.A. Mead, "The CMOS Grounded-Substrate Convention", *Caltech Computation and Neural Systems Memo #27*, 1993.
- [29] Y. Tsvividis, *Operation and Modeling of the MOS Transistor*, pp. 136–140, McGraw-Hill Book Company, New York, 1987.
- [30] P. Hasler, B. A. Minch, C. Diorio, and C. A. Mead, "An Autozeroing Amplifier Using pFET Hot-Electron Injection", *Proceedings of the IEEE Symposium on Circuits and Systems*, Vol. 3, pp. 325–328, Atlanta, May 1996.
- [31] P. Hasler, Personal Communication.
- [32] B. A. Minch, C. Diorio, P. Hasler, and C. A. Mead, "Translinear Circuits Using Subthreshold Floating-Gate MOS Transistors", *Analog Integrated Circuits and Signal Processing*, 9(2), pp. 1–13, 1996.

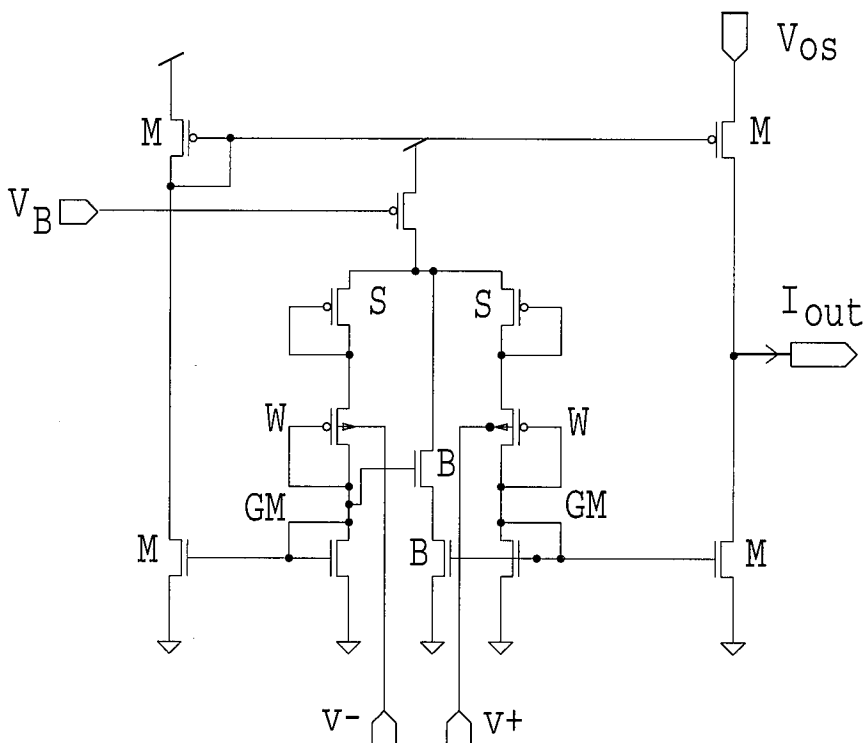


Figure 3.1: The Wide Linear Range Transconductance Amplifier. The figure shows the transconductance amplifier with  $v_+$  and  $v_-$  well-input voltages and the  $I_{out}$  current output. The voltage  $V_B$  sets the bias current of the amplifier and the voltage  $V_{os}$  allows a fine adjustment of its offset if necessary. The S transistors reduce the transconductance of the differential-pair W transistors through source degeneration. The GM transistors reduce the transconductance of the W transistors through gate degeneration. They also serve to mirror the differential-pair currents to the output of the amplifier. The B transistors implement bump linearization. The M transistors form parts of the current mirrors in the circuit.

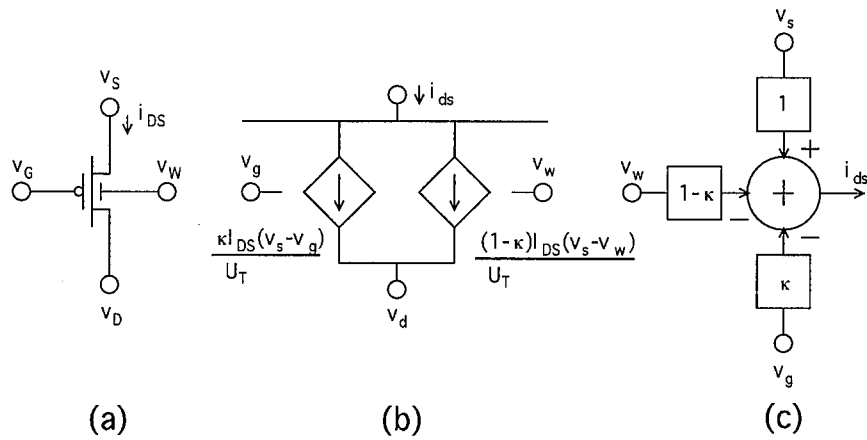


Figure 3.2: Signal-Flow Diagram for a Saturated Well Transistor. (a) A well transistor with marked voltages and currents. (b) The small-signal equivalent circuit for the well transistor. (c) The signal-flow diagram represents the dimensionless relationships between the small-signal variables of the transistor. In our paper it shall prove to be the most useful and insightful way of analyzing transconductance relationships, rather than the more conventional circuit representation shown alongside it. In the signal-flow diagram, it is understood that all currents are normalized by  $I_{DS}$ , all voltages are normalized by  $U_T$ , and all transconductances are normalized by  $I_{DS}/U_T$ . Thus, the small-signal relationship of the transistor takes the simple form  $i_{ds} = v_s - \kappa v_g - (1 - \kappa)v_w$ .

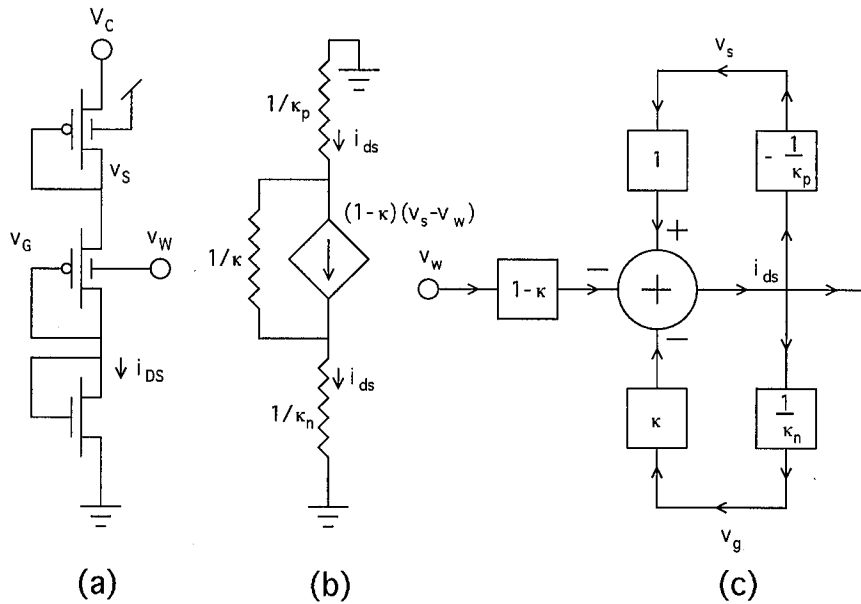


Figure 3.3: Transconductance Reduction through Degeneration. (a) A half circuit for one differential arm of our amplifier, if we ignore the B transistors of Figure 3.1 for now. (b) A small-signal equivalent circuit for this configuration. (c) A signal-flow diagram for this configuration. The signal-flow diagram shows that the transconductance reduction is achieved through two parallel feedback loops. The top loop is due to source degeneration and the bottom loop is due to gate degeneration. A more detailed description of the feedback concepts associated with transconductance reduction may be found in Section 3.2.2.

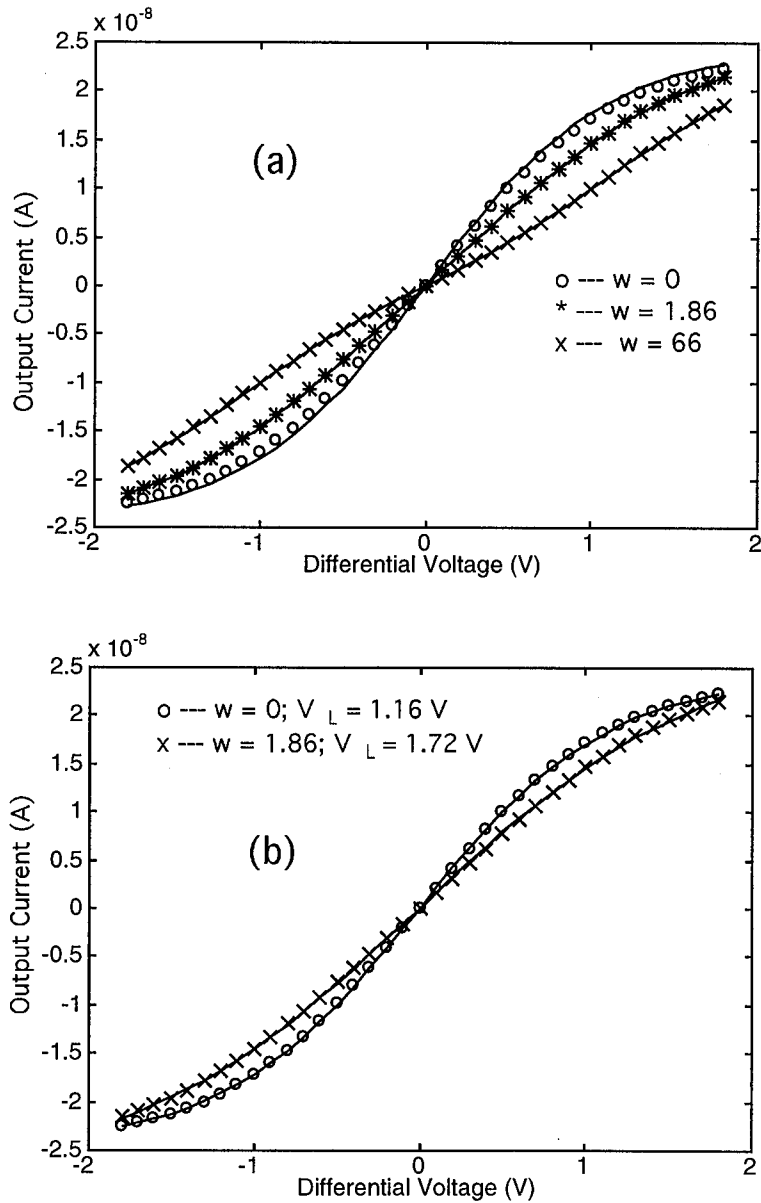


Figure 3.4: I-V curves for the Amplifier. (a) Experimental data for our amplifier for values of  $w = 0, 1.86,$  and  $66$ , fitted to Eq. (3.19). (b) For  $w \approx 2$ , the simple tanh-fit of Eq. (3.16) is a good approximation to Eq. (3.19), if  $V_L \rightarrow (3/2)V_L$

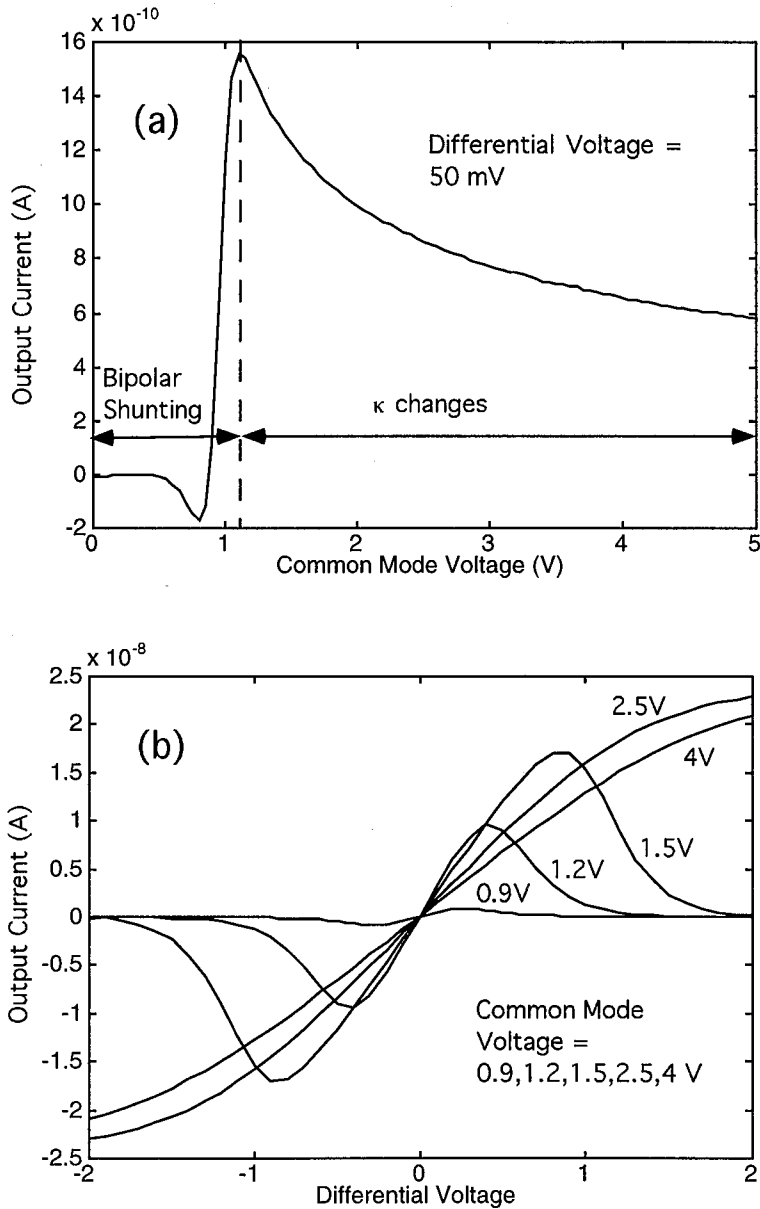


Figure 3.5: Differential and Common-Mode Curves. (a) The data shows that the current rises as the common-mode voltage is decreased from 5V to 1V, because changes in  $\kappa$  increase the transconductance of the amplifier. Below 1V, the well-to-source junction becomes forward biased, and the parasitic bipolar transistors, which are part of every well transistor, shunt the current of the amplifier to ground. (b) The same effects as in (a) but from the perspective of varying the differential-mode voltage, while fixing the common-mode voltage. Further details may be found in Section 3.3.1.

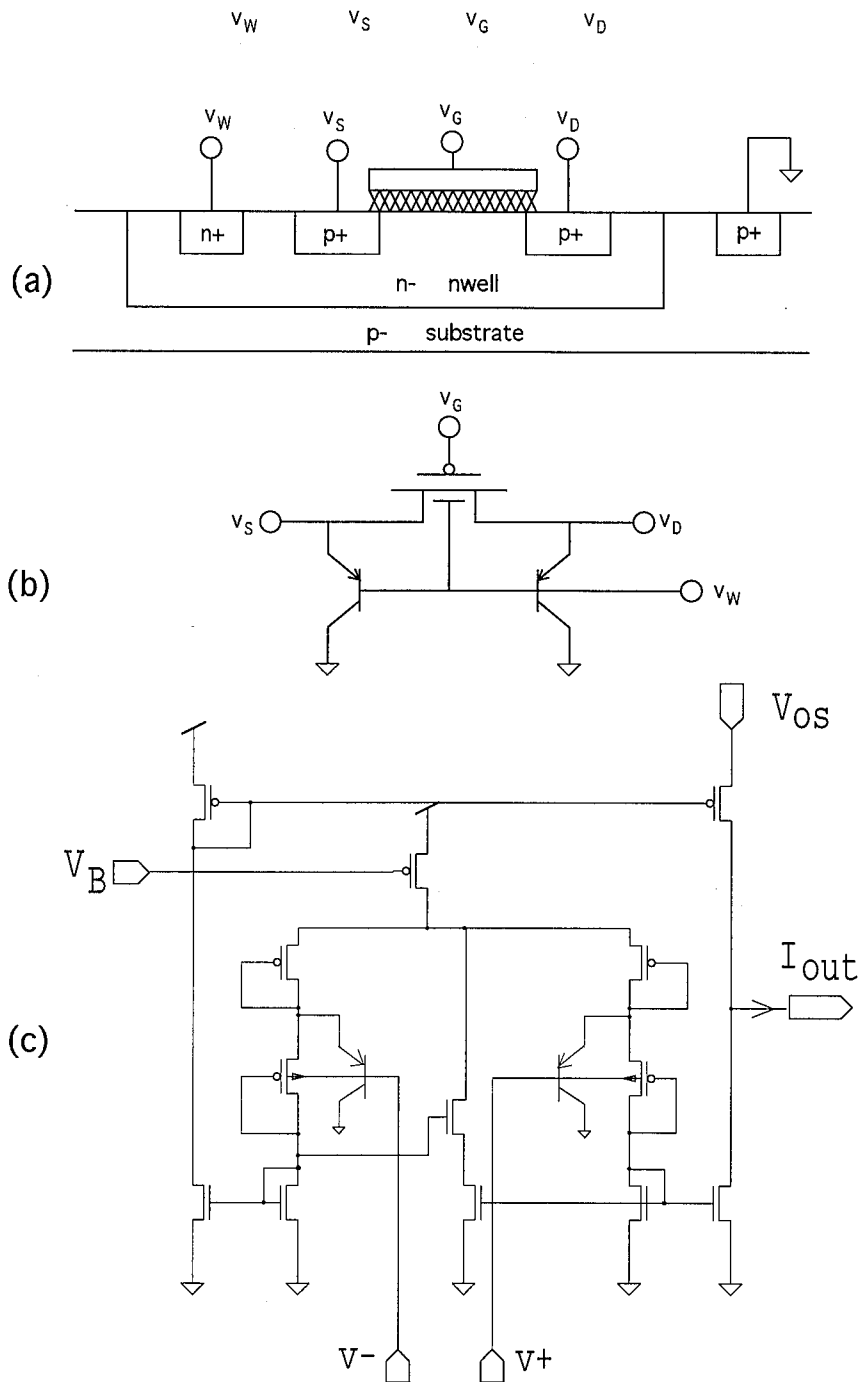


Figure 3.6: The effect of the parasitic bipolar transistor. (a) A vertical crosssection of a well transistor in an  $n$ -well process. (b) The equivalent circuit of this well transistor contains two parasitic bipolar transistors. (c) The bipolar transistor at the source is responsible for shunting the amplifier's current to ground at low common-mode voltages, while the bipolar transistor at the drain plays a negligible part.

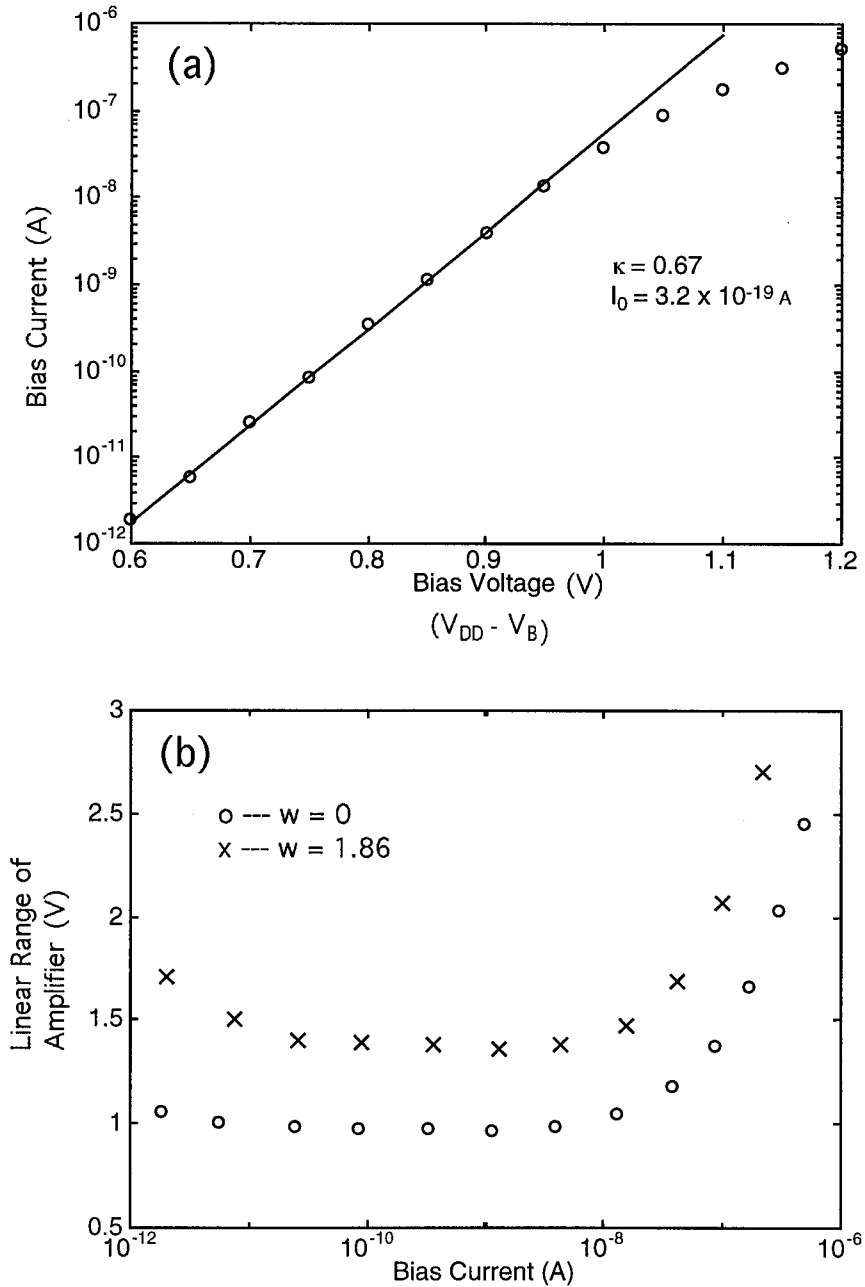


Figure 3.7: Linear Range vs. Bias Current. (a) The bias current  $I_B$  as a function of the bias voltage  $V_B$ . (b) The linear range of the amplifier  $V_L$  as a function of the bias current  $I_B$ .



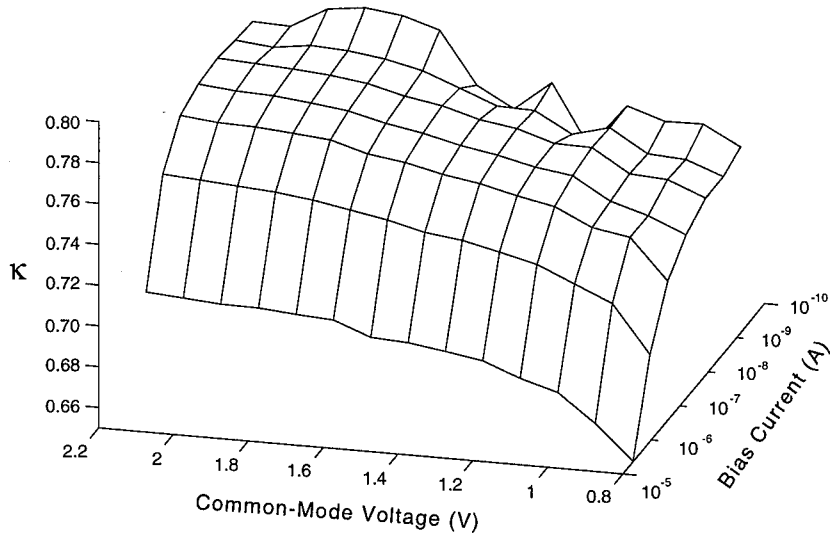


Figure 3.8: The changes in  $\kappa$  in a simple  $n$ FET differential pair. The changes in  $\kappa$  are most abrupt at low common-mode voltages, i.e., at low gate-to-bulk voltages;  $\kappa$  also decreases with increasing bias current.

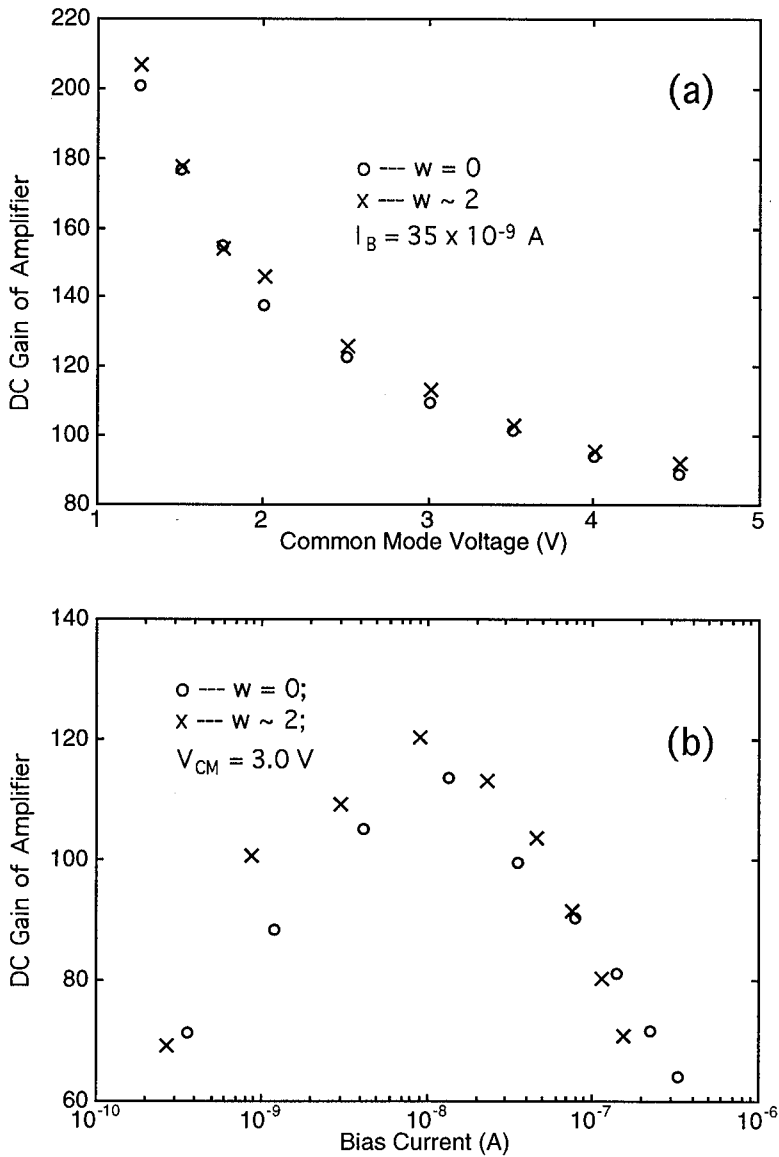


Figure 3.9: Gain Characteristics. (a) The gain of our amplifier as a function of the common-mode voltage. At low common-mode voltages, the gain increases because of the rising transconductance of the amplifier. (b) The gain of our amplifier as a function of the bias current. Initially, the gain rises because of the increasing Early Voltage of the amplifier, and then falls because of the increasing linear range. A more detailed discussion may be found in Section 3.3.3.

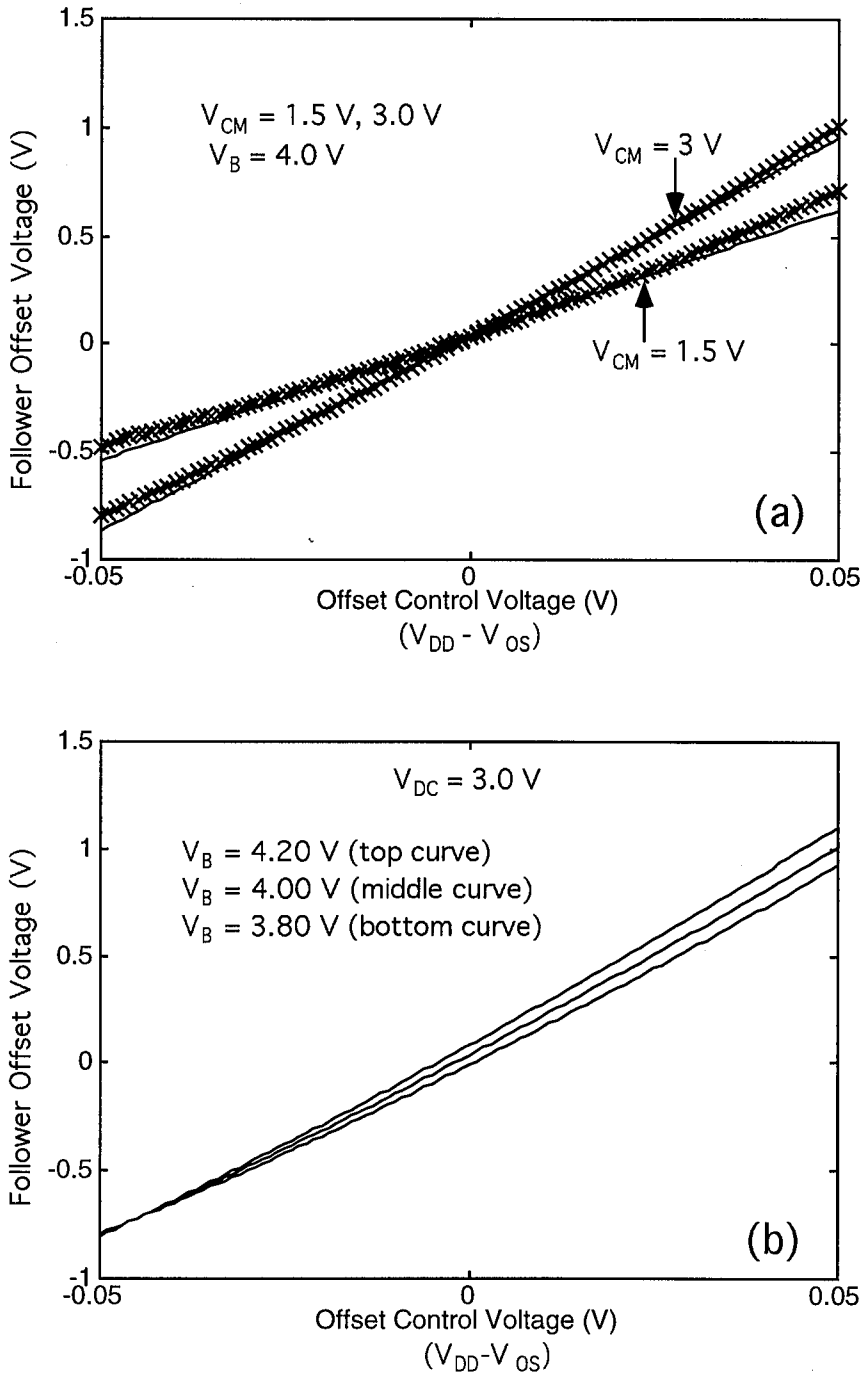


Figure 3.10: Offset Characteristics. (a) The offset characteristics of the amplifier at two different common-mode voltages. (b) The same characteristics at three different bias currents. More details may be found in Section 3.3.4.

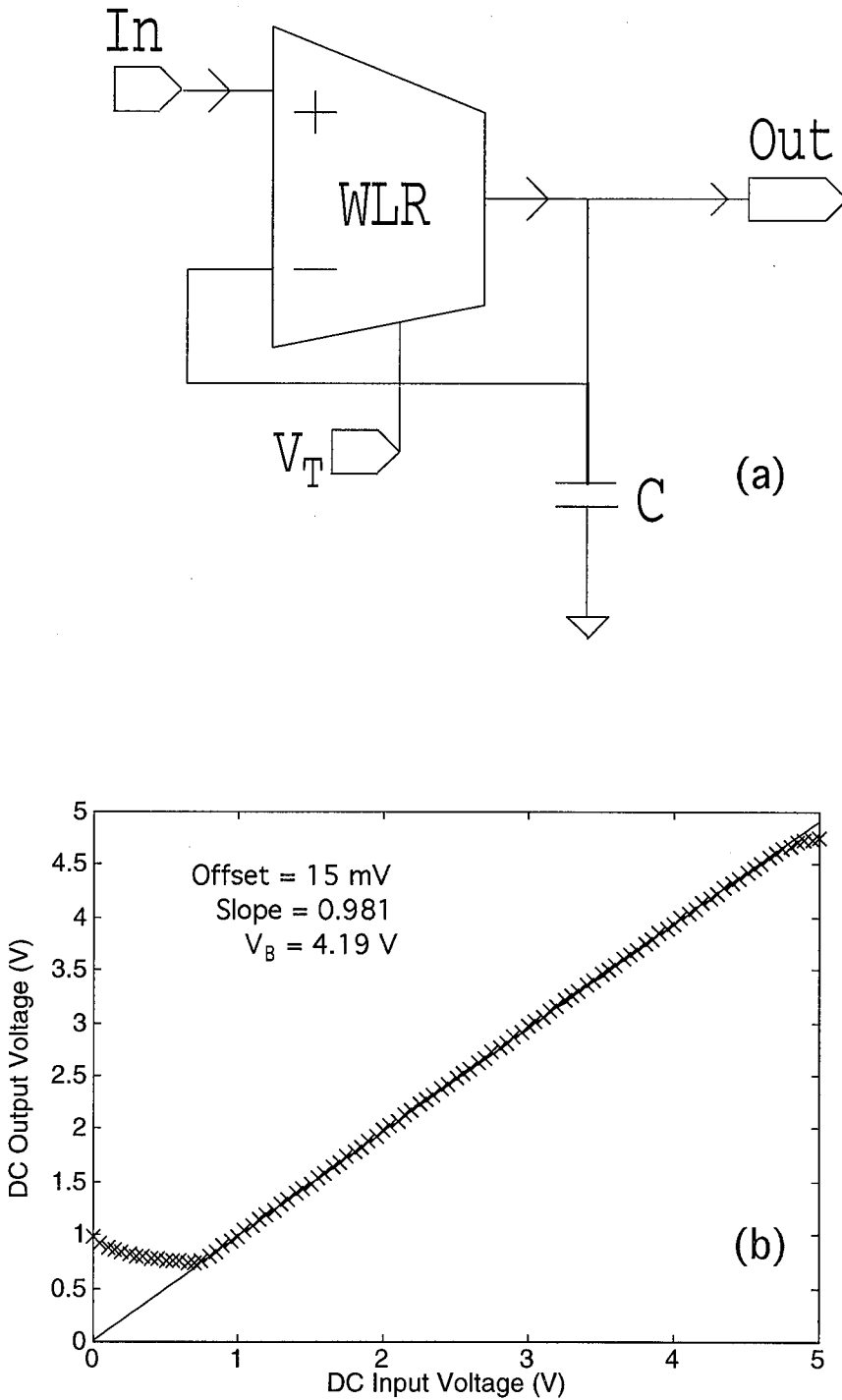


Figure 3.11: Follower DC Characteristics. (a) The basic circuit for a follower-integrator. (b) The output is a faithful replica of the input except at very low input voltages.

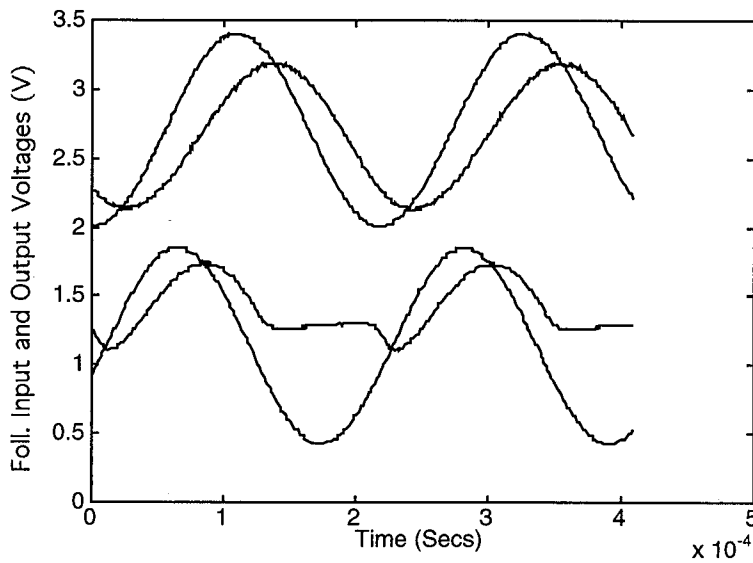


Figure 3.12: Bipolar Effects in the Follower-Integrator. The top portion of the figure shows normal follower-integrator operation, i.e., the filtering of a sinewave input. The output waveform is attenuated and phase-shifted with respect to the input waveform. The bottom portion of the figure shows operation of the filter at low input voltages. An explanation for the strange output curve is given in Section 3.4, and is due to the effects of the parasitic bipolar transistors in our amplifier.

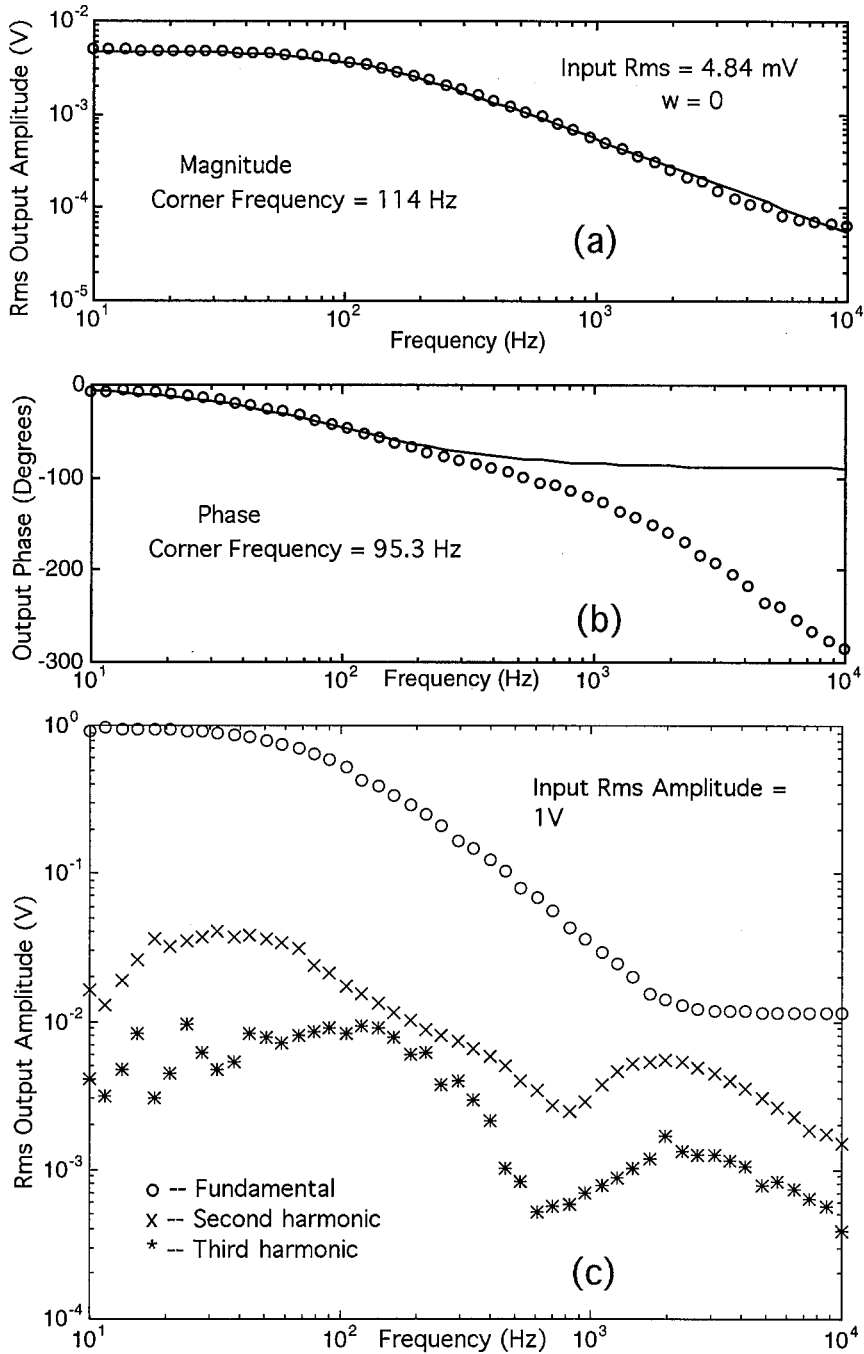


Figure 3.13: Follower-Integrator Frequency Response at a dc-input voltage of 3V. (a) and (b) show the gain and phase characteristics of the follower-integrator along with fits to lowpass filter transfer functions. The phase characteristics are more sensitive to parasitics and we model their effect by fitting the phase curves to a different corner frequency than the gain curves. (c) The first, second, and third harmonic rms output amplitudes at an input rms amplitude of 1V (2.8 V peak-to-peak). Because of the wide linear range of the amplifier, the total harmonic distortion is low even at this amplitude.

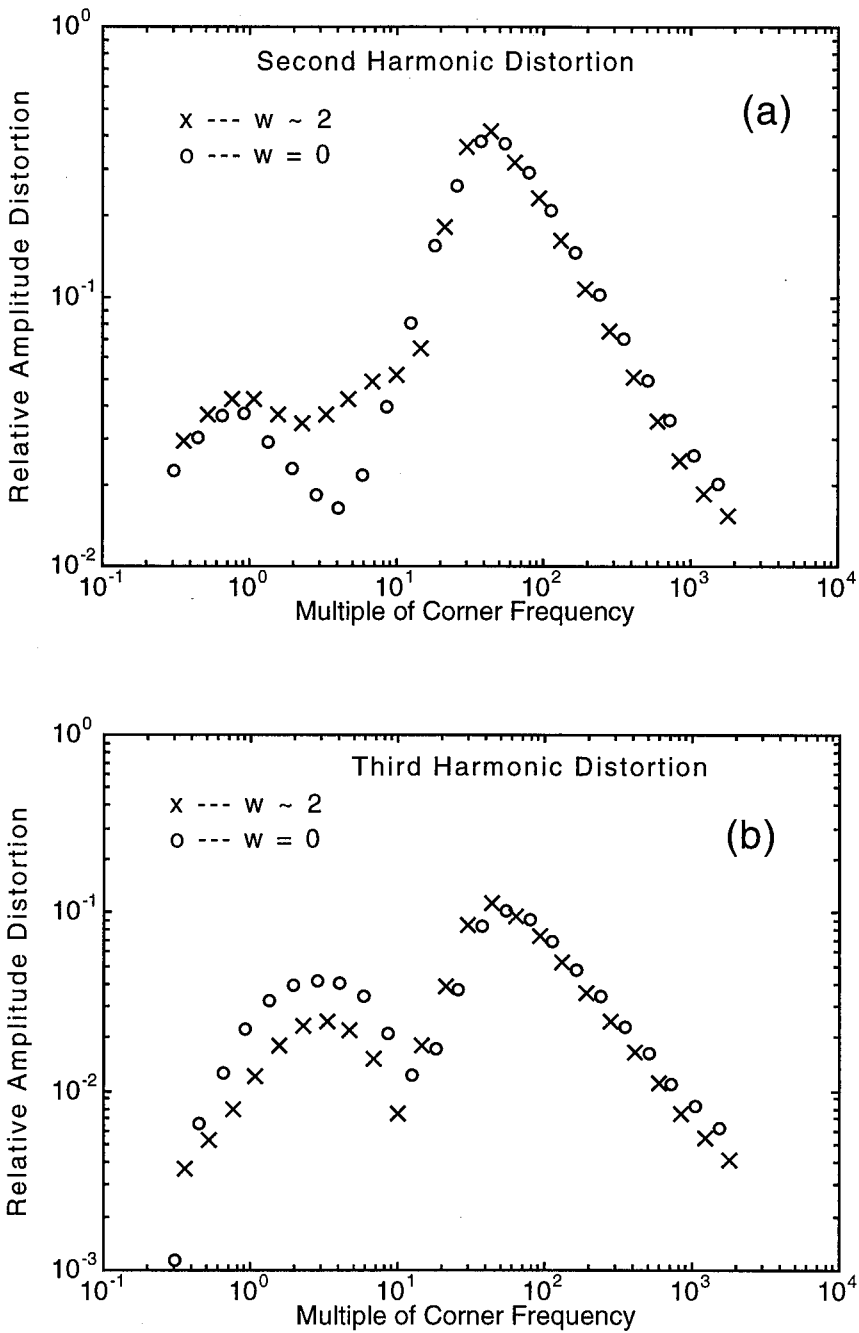


Figure 3.14: Follower-Integrator Distortion Characteristics. (a) The ratio of magnitude of the second harmonic to that of the first harmonic vs. normalized frequency, i.e., frequency normalized by the CF. (b) The same as (a) except that the third harmonic is plotted instead. Note that the addition of the  $B$  transistors decreases third harmonic distortion but increases second harmonic distortion.

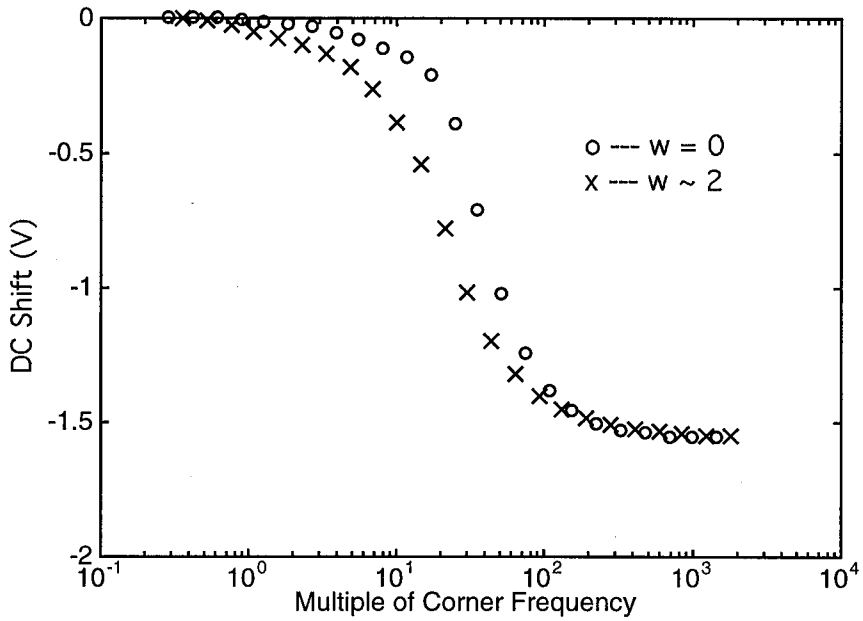


Figure 3.15: DC Shifts in the Follower-Integrator. The shifts are shown at an input rms amplitude of 1V. These shifts exert only a mild influence in cochlear designs. See Section 3.4.1 for details.



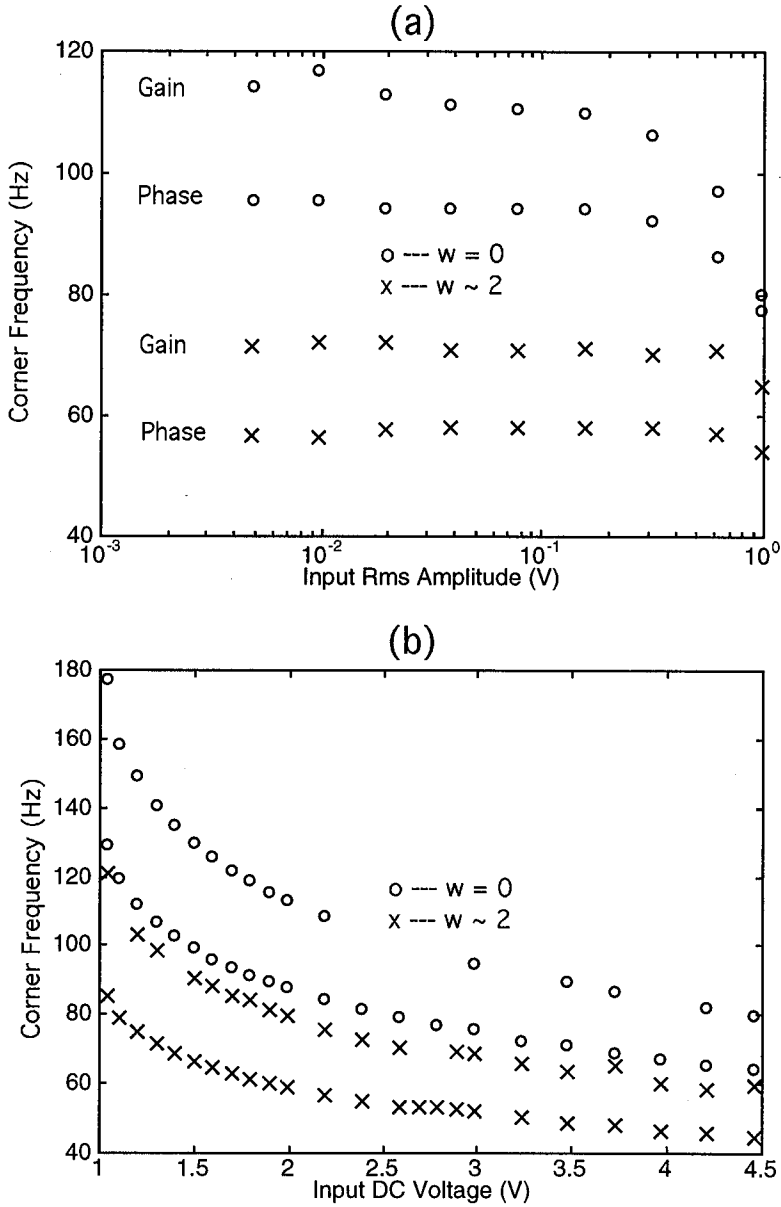


Figure 3.16: Corner-Frequency Shifts in the Follower-Integrator. (a) CF-shifts vs. input rms amplitude and (b) CF-shifts vs. input dc voltage. The lower curve is the phase CF for the  $w = 0$  and the  $w = 2$  cases.

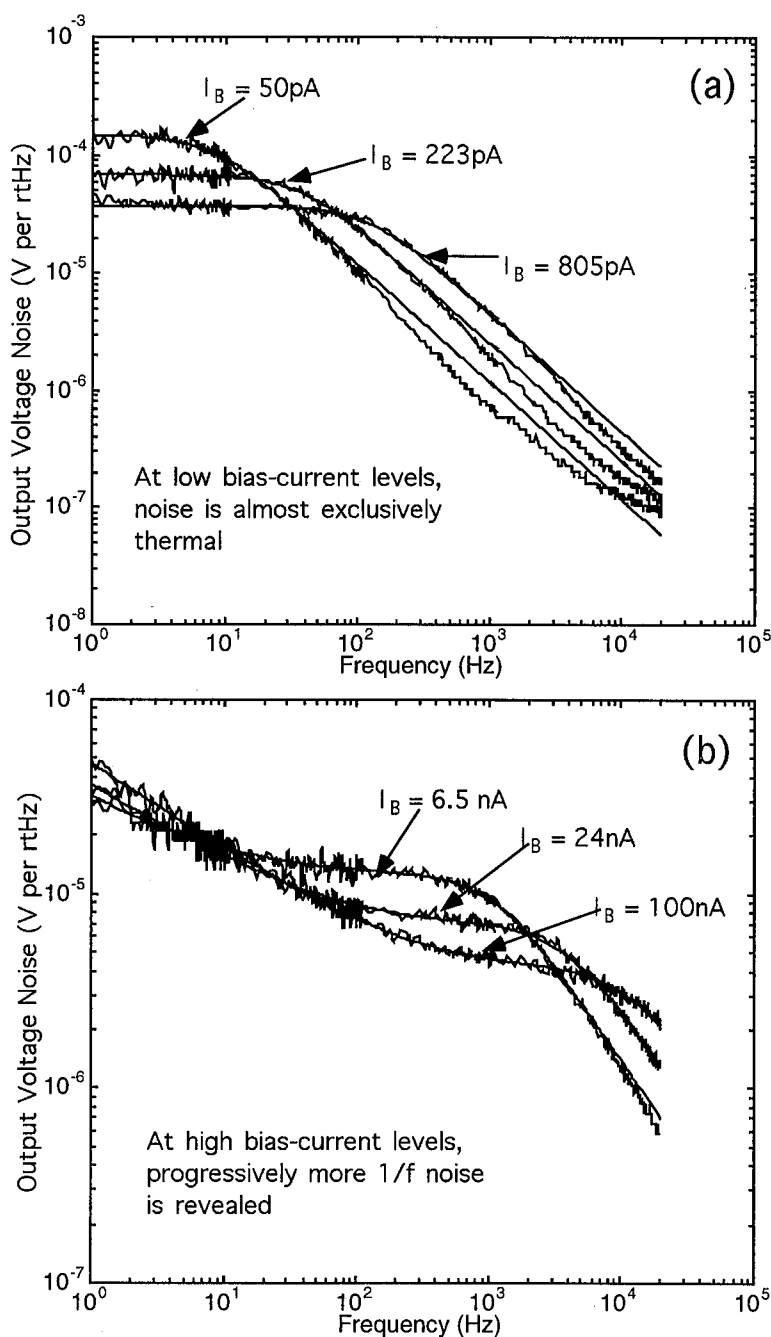


Figure 3.17: Noise Spectra at Various Current Levels. (a) At low bias currents the noise is almost solely white or thermal. The bold lines are lowpass-filter fits to the data. (b) At high bias currents, there is relatively more  $1/f$  noise. Nonetheless, the dominant contribution to the noise, which is the area under this curve in a linear-linear plot, remains thermal. The bold lines are fits to the sum of a  $1/f$  term and a white-noise term.

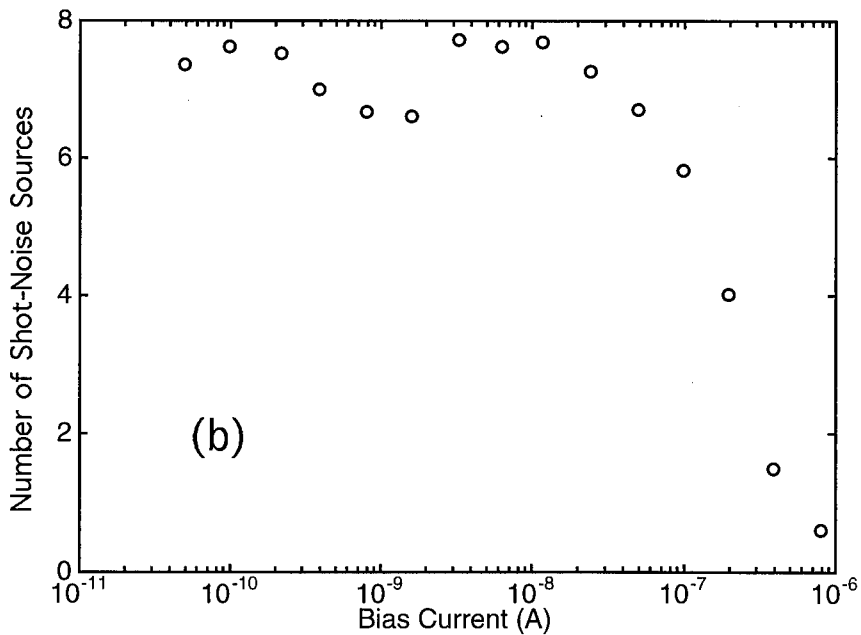
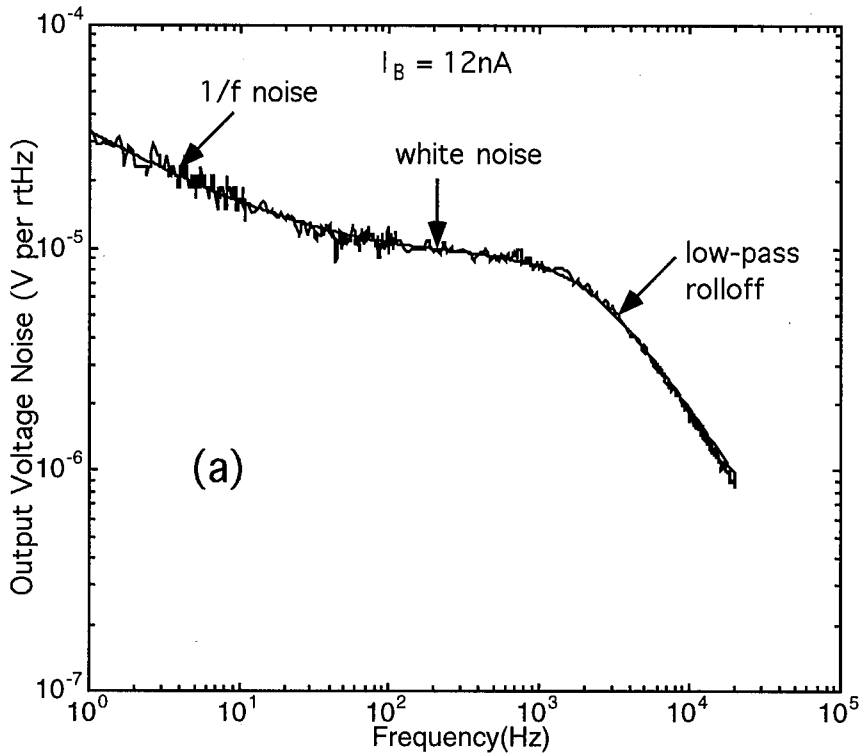


Figure 3.18: Basic Noise Characteristics. (a) A typical noise spectrum. (b) The effective number of transistors contributing shot noise in our circuit as a function of the bias current. As the bias current goes above threshold, the effective number of transistors contributing shot noise decreases because of space-charge smoothing.

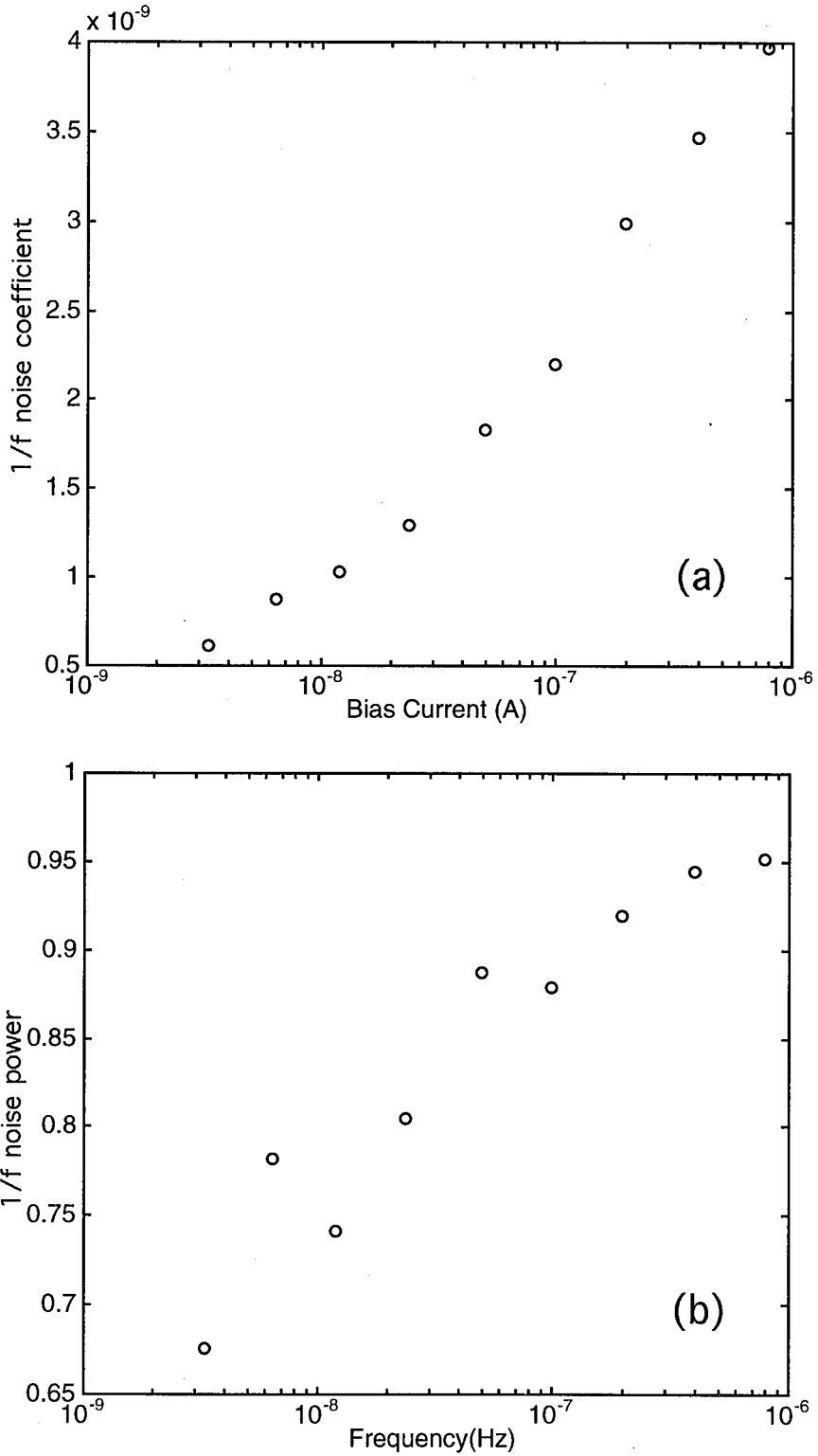


Figure 3.19: Characteristics of  $1/f$  noise. (a) The  $1/f$  noise coefficient  $K_B$ , used in Eq. (3.36), as a function of the bias current  $I_B$ . (b) The  $1/f$  noise power  $n$  as a function of the bias current  $I_B$ .

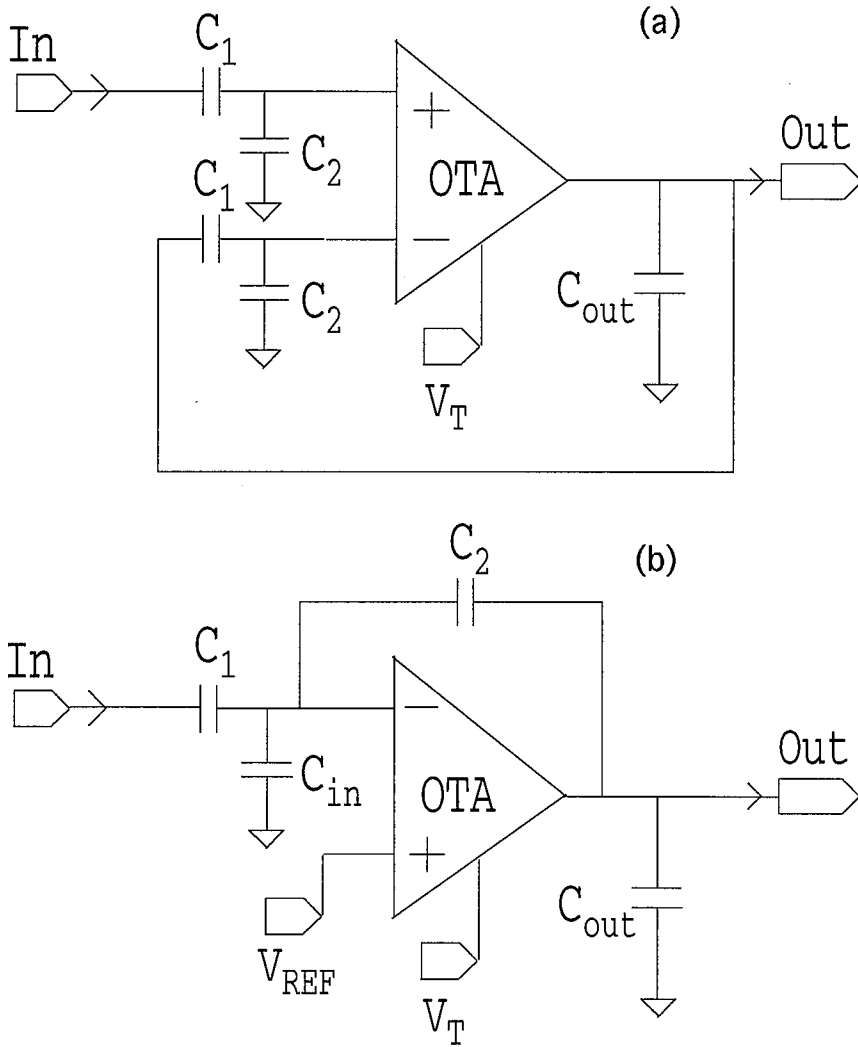


Figure 3.20: Capacitive-Divider Schemes for Widening the Linear Range. (a) and (b) show two different schemes. Section 3.5.4 contains further details.

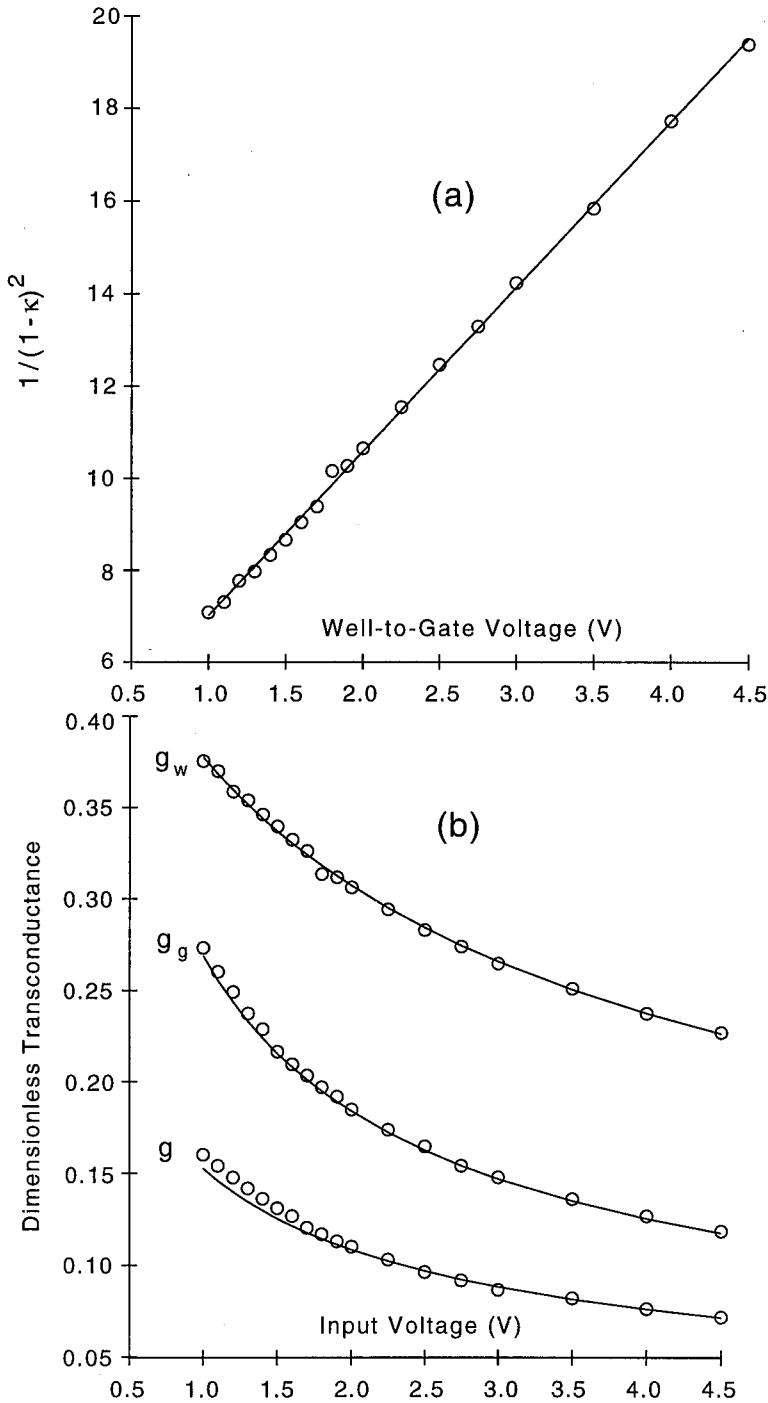


Figure 3.21: The effects of changes in  $\kappa$ . (a) The changes in  $\kappa$  with well-to-gate voltage may be used to extract the body-effect parameter  $\gamma$  and the flatband voltage  $V_{FB}$ . The slope of the graph yields information about  $\gamma$ , and the intercept then yields information about  $V_{FB}$ . See Section 3.7.1 for details. (b) Data for the change in transconductance of well-input amplifiers with no degeneration ( $g_w$ ), with gate degeneration ( $g_g$ ), and with gate and source degeneration ( $g$ ). The solid lines are fits to theory.

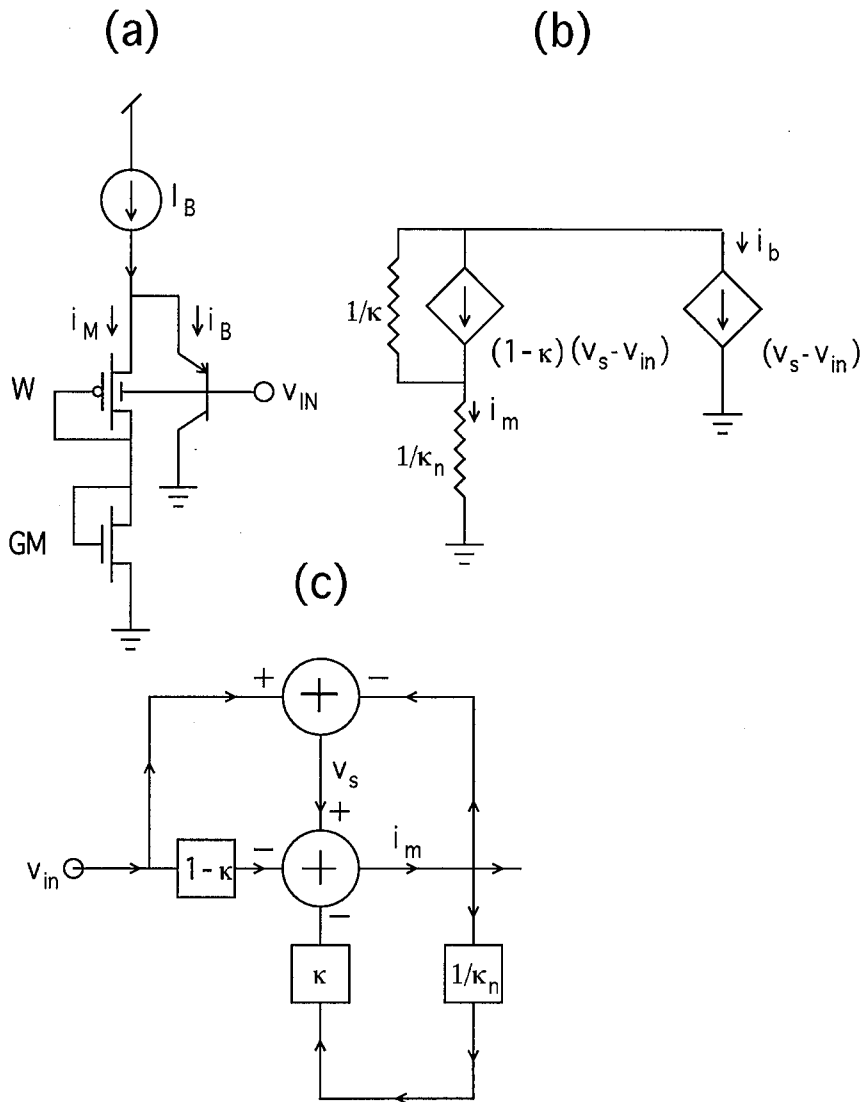


Figure 3.22: The parasitic bipolar half circuit. (a) A simplified half circuit for our amplifier that is important for understanding the bipolar–mos interaction in it. (b) The small-signal equivalent circuit for (a). (c) A signal-flow diagram for the small-signal equivalent circuit.

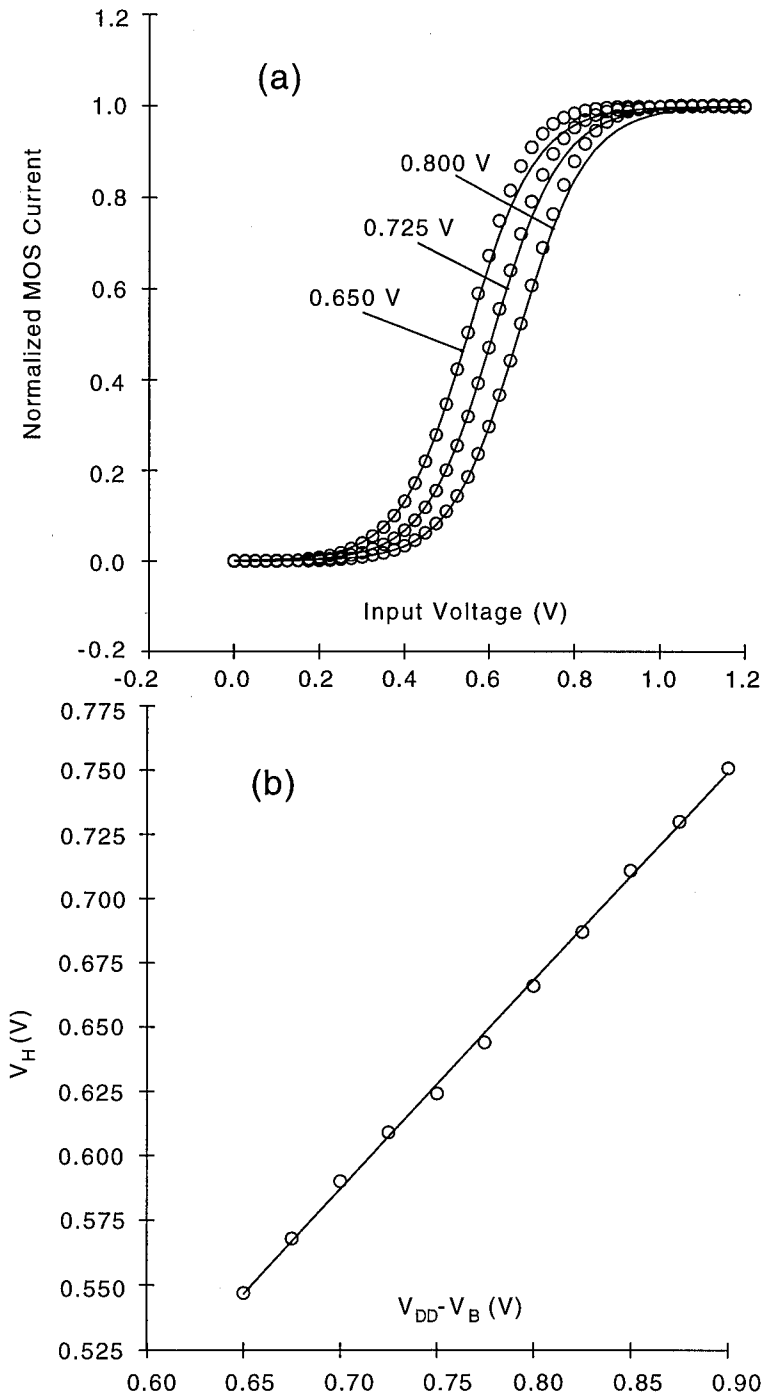


Figure 3.23: The Bipolar-MOS Characteristics. The sigmoid-like competition between the MOS and bipolar transistors as the input voltage is varied. The three parametric voltages refer to the value of the bias voltage  $V_B$  of Figure 3.1. (b) The threshold point of this sigmoid varies with  $V_B$ .



### 3.7 Appendix A

This appendix contains a quantitative discussion of the common-mode effects in our amplifier. The data in the appendix were taken for a  $w = 0$  amplifier built in a  $p$ -well process, as opposed to the data in the rest of the paper, which were taken in an  $n$ -well process. The  $\kappa$  for the  $p$ -well process is lower, and consequently the linear range is near 0.6 V, rather than 1V. We also use the grounded-substrate convention [12]. This convention enables us to present the data as though they were from an  $n$ -well process, as in the rest of the paper. The grounded-substrate convention implements the following transformation from  $n$ -well space to  $p$ -well space:  $V \rightarrow -V$ ,  $n$ -channel  $\rightarrow p$ -channel, and  $p$ -channel  $\rightarrow n$ -channel. Note that the transformation is applied to all voltages implicitly defined in terms of the gate, source, drain, or well voltages in addition. For example, the flatband voltage is defined in terms of  $v_G - v_W$ , and changes sign as we move from  $n$ -well space to  $p$ -well space. Thus, if the flatband voltage is quoted as  $-0.75$  V for an  $n$ -channel transistor, it's taken as  $-0.75$  V for a native transistor in  $n$ -well space and as  $+0.75$  V for a well transistor in  $p$ -well space.

#### 3.7.1 The Effects of Changes in $\kappa$

In our amplifier, the gates of the W transistors are near ground. As we lower the voltages of the well inputs, the well-to-gate voltage decreases; consequently  $\kappa$  decreases; the transconductance, which is proportional to  $1 - \kappa$ , increases. We now analyze this effect more quantitatively.

The parameter  $\kappa$  is a function of the gate-to-well voltage. We can show that

$$\kappa = 1 - \frac{\frac{\gamma}{2}}{\sqrt{\frac{\gamma^2}{4} - (v_G - v_W - V_{FB})}}, \quad (3.40)$$

where  $\gamma$  is the body-effect parameter and  $V_{FB}$  is the flatband voltage.

A well-input amplifier that has no source degeneration or gate degeneration has a transconductance of magnitude  $g_w$ , given by  $g_w = (1 - \kappa)$ . By computing the transconductance at the origin for various common-mode voltages  $V_C$ , we measured  $g_w$  as a function of  $V_C$  at a bias current corresponding to  $V_{DD} - V_B = 0.77$  V. From Eq. (3.40), if we plot

$1/(1 - \kappa)^2$  versus  $v_W$ , i.e.,  $1/g_w^2$  versus  $v_C$ , we get

$$\frac{1}{g_w^2} = \left( \frac{1}{\frac{\gamma^2}{4}} \right) v_C + \left( 1 + \frac{V_{FB} - V_G}{\frac{\gamma^2}{4}} \right), \quad (3.41)$$

which is a straight line. Thus, we can compute  $\gamma$  and  $V_{FB}$  from the slope and y-intercept of this line, if we know  $V_G$ . For our experiment, we grounded the gate to allow maximum dc input operating range, so  $V_G$  was 0. From the data shown in Figure 3.21a, we computed  $\gamma = 1.06V^{\frac{1}{2}}$  and  $V_{FB} = 0.68$  V. In comparison, the SPICE parameters from the MOSIS sheets quoted  $\gamma = 1.05V^{\frac{1}{2}}$  and  $V_{FB} = 0.75V$ . The actual flatband voltages are negative; since the data were taken in a  $p$ -well process, we use the positive values as explained in the first paragraph of this appendix.

A well-input amplifier with gate degeneration has a transconductance of magnitude  $g_g$ , given by

$$g_g = \frac{1 - \kappa}{1 + (\kappa/\kappa_n)}. \quad (3.42)$$

For such an amplifier, we can determine the functional variation of  $\kappa$  with  $V_C$  from Eq. (3.40), using the previously determined values of  $V_{FB}$  and  $\gamma$ , and with  $V_G$  being the amount of diode drop on a G transistor. By using measured well and native transistor parameters we estimate  $V_G = 0.69$  V given that  $V_{DD} - V_B = 0.77$  V, and also that  $\kappa_n = 0.714$ . By using these parametric values in Eq. (3.42) and Eq. (3.40), we predicted the dependence of  $g_g$  with  $v_C$ . The middle curve of Figure 3.21b shows that changes of  $g_g$  with  $V_C$  were in good agreement with the theory of Eq. (3.42) and Eq. (3.40). The uppermost curve of Figure 3.21b is that of  $g_w$  versus  $V_C$  and is also plotted for reference; it is simply a different way of plotting Figure 3.21a.

A well-input amplifier with source and gate degeneration has a transconductance  $g$  given by Eq. (3.3). By using the functional variation of  $\kappa$  versus  $V_C$ , the values of  $\kappa_n$ , the value of  $V_G$  estimated in the previous paragraph, and  $\kappa_p = 0.753$ , we were able to predict the variation of  $g$  with  $V_C$ , as shown by the lowest curve of Figure 3.21b. The data begin to deviate from theory at the lower input voltages, probably because of the change in  $\kappa_p$  with increasing well-to-gate voltage.

### 3.7.2 The Effects of the Parasitic Bipolar Transistor

To understand exactly when the parasitic bipolar transistor present in every MOS well transistor becomes significant, we find it instructive to analyze the interaction between the bipolar and MOS modes of operation for a well transistor: The subthreshold saturation current of an MOS transistor situated in a well, which is assumed to be an  $n$ -well without loss of generality, is given by

$$i_M = I_M e^{\left(\frac{v_S - \psi}{U_T}\right)}, \quad (3.43)$$

where  $\psi$  is the surface potential, and  $I_M$  is a constant pre-exponential factor. The constant  $I_M$  does have a weak dependence on  $\psi$ , described in [29], that we neglect for simplicity. If  $I_{T0}$  is the threshold current of the transistor, and if, at this point, the surface potential is below the source potential by an amount  $2\phi_F$ , then

$$I_M = I_{T0} e^{-2\phi_F/U_T}. \quad (3.44)$$

The constant  $I_{T0}$  is typically near  $\mu C_{ox}(W/2L)(U_T/\kappa)^2$ .

If all voltages are referenced to the well (i.e.,  $v_W = 0$ ), and we define  $\bar{\psi} = -\psi$  and  $\bar{v}_F = -(v_G - V_{FB})$ , then we can show that

$$\bar{\psi} = \left( \sqrt{\bar{v}_F + \frac{\gamma^2}{4}} - \frac{\gamma}{2} \right)^2. \quad (3.45)$$

We introduce the definitions of  $\bar{\psi}$  and  $\bar{v}_F$  because it is more convenient to work with  $-\psi$  and  $-(v_G - V_{FB})$  when dealing with transistors in the well.

The source current of a well transistor is split into an MOS component, called  $i_M$ , which reaches the drain of the transistor and a bipolar component, called  $i_B$ , which is shunted away to ground. The bipolar current is given by

$$i_B = I_B e^{\left(\frac{v_S - v_W}{U_T}\right)}, \quad (3.46)$$

where  $I_B$  is the saturation current of the bipolar. The MOS current is given by Eq. (3.43).

The question that we now ask is this: When does the MOS current exceed the bipolar current ( $i_M \geq i_B$ )? The answer to this question provides insight into how a well transistor

must be operated if it is to have as wide a range of MOS operation as possible. We notice that the MOS and bipolar transistors have the same dependence on the source voltage,  $v_S$ . Thus, in subthreshold, the answer is independent of the source voltage. The MOS pre-exponential factor,  $I_M$ , is usually 1000 to 10000 times smaller than the bipolar pre-exponential factor  $I_B$ . Thus, if the MOS transistor is to have any hope of competing with the bipolar transistor, its surface potential must be below that of the well by the amount that compensates for its pre-exponential handicap. Hence, the gate-to-well voltage must be below the flatband voltage by an amount needed to generate an adequate depth of depletion region. We now compute exactly how much this amount must be.

If  $i_M \geq i_B$ , then, from Eqs. (3.46) and (3.43), we must have

$$\begin{aligned} v_W - \psi &\geq U_T \ln \left( \frac{I_B}{I_M} \right) \\ &\geq V_{BM}, \end{aligned} \quad (3.47)$$

where  $V_{BM}$ , defined as in the previous equation, is a voltage that yields a measure of by how much the bipolar's pre-exponential constant exceeds the MOS's. Thus, if we reference all voltages to the well, Eq. (3.47) yields

$$\begin{aligned} -\psi &\geq V_{BM}, \\ \bar{\psi} &\geq V_{BM}, \\ \left( \sqrt{v_F + \frac{\gamma^2}{4}} - \frac{\gamma}{2} \right)^2 &\geq V_{BM}. \end{aligned} \quad (3.48)$$

After we perform simple manipulations on the previous equation, we finally obtain the criterion for the MOS transistor to dominate over the bipolar transistor:

$$(v_G - v_W) \leq V_{FB} - \sqrt{V_{BM}} \left( \sqrt{V_{BM}} + \gamma \right), \quad (3.49)$$

$$\leq V_{CT} \quad (3.50)$$

where we define  $V_{CT}$  to be the RHS of Eq. (3.49). If we require  $i_M \geq 100i_B$ , for robust operation, we must increase  $V_{BM}$  by  $U_T \ln 100$  before using Eq. (3.50). We now have a recipe for operating well transistors in subthreshold: As long as we ensure that the gate is

sufficiently below the well, we are in no danger of turning on the bipolar transistor. *Thus, if the range of MOS operation is to be as wide as possible, the gate voltage must be set to as low a value as circuit requirements will allow.* The well is then free to operate from low values near the gate voltage to  $V_{DD}$ . Therefore, when the well is being used as an input, the gate should be at ground or near ground. In our amplifier, it is one diode drop above ground.

To understand the effects of the parasitic bipolar transistor in our amplifier, we need only to understand the half-circuit shown in Figure 3.22a, because the bipolar transistor(s) in the arm(s) of our amplifier is (are) activated if the voltage of either input gets too low. It is thus simpler to analyze the effects of the bipolar transistor in a single arm of the amplifier, and to extend the analysis to the case where the bipolar transistors in both arms are activated. Hence, we tie one input to  $V_{DD}$  to turn off completely one arm of the amplifier, and we concentrate on the turned-on arm.

The circuit of Figure 3.22a is one half of the differential pair of the amplifier with the S transistor omitted, and the bipolar transistor drawn explicitly. The S transistor is omitted because it affects the drain voltage of the bias transistor (the bias-current transistor not shown), but has no effect on the currents  $i_B$  and  $i_M$ , which are our primary concern. Figure 3.22b and Figure 3.22c show the small-signal model and corresponding signal-flow diagram that describe the half-circuit of Figure 3.22a.

When the well-input voltage  $v_{IN}$  is in the 1V to 5V range, the gate voltage,  $v_G$ , which is one diode drop above ground, is sufficiently below the well voltage that all the bias current is carried by the MOS transistor. As the well voltage begins to drop, it starts to get close to the gate voltage and the bias current starts to be diverted to the bipolar transistor. The data of Figure 3.23a show that a differential-pair-like competition between the MOS and bipolar transistors yields a sigmoid curve in output current versus input voltage. The data curves of Figure 3.23 were normalized by their saturation current values, and were fit by sigmoid equations of the form

$$i_N = \frac{1}{1 + e^{-0.326(v_{IN} - V_H)/U_T}}, \quad (3.51)$$

with differing values of  $V_H$  for the three curves.

The input voltage at which the bipolar and MOS currents become equal,  $V_H$ , depends on

the bias current. Higher bias currents drop larger voltages across the GM transistor, increase the gate voltage of the W transistor, and consequently cause the well-input voltage to approach the gate voltage at higher values. The data of Figure 3.23b show our measurements of this effect, and also show that

$$V_H = 0.81 (V_{DD} - V_B) + 0.019. \quad (3.52)$$

Given the theory that we have developed for the bipolar-mos interaction (Eq. (3.50)), and the effects of changes in  $\kappa$  (Eq. (3.40)), we can predict what Eqs. (3.51) and (3.52) should be by analyzing the circuit of Figure 3.22a. Using measured values for the constants  $V_{FB}$ ,  $\gamma$ ,  $\kappa_n$ ,  $\kappa_b$  (the  $\kappa$  of the bias-current transistor), and  $V_{BM}$  (determined by measurements of the bipolar and MOS pre-exponential constants), we were able to obtain reasonable agreement between theory and experiment. From the signal-flow diagram of Figure 3.22c, we can show that the constant 0.326 of Eq. (3.51) is nearly

$$\alpha = 2 \frac{(\kappa/2)\kappa_n}{\kappa/2 + \kappa_n}. \quad (3.53)$$

Note that we evaluated  $\kappa$  with the surface potential at a value that was  $V_{BM}$  below the well voltage. We found that it was 0.467. Using Eq. (3.50) and elementary reasoning, we can show that Eq. (3.52) is derived from

$$V_H = \frac{\kappa_b}{\kappa_n} (V_{DD} - V_B) + \frac{U_T}{\kappa_n} \ln \left( \frac{I_0^B}{2I_0^N} \right) - V_{CT}, \quad (3.54)$$

where  $I_0^B$  and  $I_0^N$  are the subthreshold scaling parameters for the bias-current transistor and for the G transistor respectively. We found that  $\kappa_b = 0.5615$ ,  $\kappa_n = 0.714$ ,  $I_0^B = 1.12 \times 10^{-17}$  A,  $I_0^N = 1.40 \times 10^{-16}$  A,  $I_B = 2.12 \times 10^{-16}$  A,  $I_{T0} = 1.8 \times 10^{-7}$  A,  $2\phi_F = 0.749$  V,  $V_{BM} = 0.2165$  V,  $\gamma = 1.05V^{\frac{1}{2}}$ ,  $V_{FB} = 0.75$  V. The most interesting finding is that  $V_{BM} = 0.26$  V, which implies that the MOS transistor's pre-exponential constant  $I_M$  is about 4000 times as weak as the bipolar transistor's pre-exponential constant  $I_B$ .

## Chapter 4 A Low-Power Wide-Dynamic-Range Analog VLSI Cochlea

### Abstract

Low-power wide-dynamic-range systems are extremely hard to build. The biological cochlea is one of the most awesome examples of such a system: It can sense sounds over 12 orders of magnitude in intensity, with an estimated power dissipation of only a few tens of microwatts. In this paper, we describe an analog electronic cochlea that processes sounds over 6 orders of magnitude in intensity, and that dissipates 0.5mW. This 117-stage, 100Hz-to-10Khz cochlea has the widest dynamic range of any artificial cochlea built to date. The wide dynamic range is attained through the use of a wide-linear-range transconductance amplifier, of a low-noise filter topology, of dynamic gain control (AGC) at each cochlear stage, and of an architecture that we refer to as *overlapping cochlear cascades*. The operation of the cochlea is made robust through the use of automatic offset-compensation circuitry. A BiCMOS circuit approach helps us to attain nearly scale-invariant behavior and good matching at all frequencies. The synthesis and analysis of our artificial cochlea yields insight into why the human cochlea uses an active traveling-wave mechanism to sense sounds, instead of using bandpass filters. The low power, wide dynamic range, and biological realism make our cochlea well suited as a front end for cochlear implants.

### 4.1 Introduction

The dynamic range of operation of a system is measured by the ratio of the intensities of the largest and smallest inputs to the system. Typically, the dynamic range is quoted in the logarithmic units of decibel (dB), with 10dB corresponding to 1 order of magnitude. The largest input that a system can handle is limited by nonlinearities that cause appreciable distortion or failure at the output(s). The smallest input that a system can handle is limited by the system's input-referred noise floor.

At the *same* given bandwidth of operation, a low-current system typically has a higher noise floor than does a high-current system: The low-current system averages over fewer

electrons per unit time than does the high-current system, and, consequently, has higher levels of shot or thermal noise [1]. Thus, it is harder to attain a wide dynamic range in low-current systems than in high-current systems. A low-voltage system does not have as wide a dynamic range as a high-voltage system because of a reduction in the maximum voltage of operation.<sup>1</sup>

Low-power systems have low-current or low-voltage levels; consequently, it is harder to attain a wide dynamic range in low-power systems than in high-power systems. The biological cochlea is impressive in its design because it attains an extremely wide dynamic range of 120dB (at 3kHz), although its power dissipation is only about  $14\mu\text{W}$ . The power dissipation in the biological cochlea has been estimated from impedance calculations to be about  $0.4\mu\text{W}/\text{mm} \times 35\text{mm} = 14\mu\text{W}$  [2].

The dynamic range of the cochlea at various input frequencies has been measured by psychophysical and physiological experiments [3]. The biological cochlea has a wide dynamic range because it has an adaptive traveling-wave amplifier architecture, and also because it uses a low-noise electromechanical technology.

The electronic cochlea models the traveling-wave amplifier architecture of the biological cochlea as a cascade of second-order filters with corner frequencies that decrease exponentially from 20kHz to 20Hz (the audio frequency range) [4]. The exponential taper is important in creating a cochlea that is roughly scale invariant at any time scale; it is easily implemented in subthreshold CMOS, or in bipolar technology.

Prior cochlear designs have paid little or no attention to dynamic range. The reports do not give their dynamic ranges [4]–[18]. However, we know that low-power cochlear designs that pay no attention to noise or gain control, like our own initial designs, have a dynamic range of about 30dB to 40 dB (1mV to 70mV rms) at the small-signal peak frequency (BF) of a typical cochlear stage. The lower limit of the dynamic range is determined by the input signal level that results in an output signal-to-noise ratio (SNR) of 1. The upper limit of the dynamic range is determined by the input-signal level that causes a total harmonic distortion (THD) of about 4%. Typically, the upper limit is a strong function of the linear range of the transconductance amplifiers used in the cochlear filter.

A single follower-integrator filter in one of our recent designs [9] had a dynamic range

---

<sup>1</sup>We are assuming that the supply voltage limits the range of operation of the system. If there is some other voltage that limits the range of operation of the system, then power is wasted through an unnecessarily high supply voltage. We choose not to operate the system in this nonoptimal situation.



of 65dB (0.55mV–1000mV rms) because of the use of a wide-linear-range transconductance amplifier (WLR) [10]. However, even if the first filter in a cochlea has a wide dynamic range, the dynamic range at the output of a typical cochlear stage is reduced by the accumulation and amplification of noise and distortion from stages preceding it. Nevertheless, the constant reduction in the bandwidth of the cochlear stages along the cascade ensures that the total noise or distortion eventually becomes invariant with the location of the cochlear stage: Noise or distortion accumulates along the cascade, but it is also reduced constantly by filtering. However, the asymptotic noise is high enough that, in our design [9], the dynamic range for a cochlear stage with a BF input was only about 46 dB (5mV to 1000mV rms). In that design, the use of nonlinear gain control helped to decrease the small-signal  $Q$  with increasing input amplitude, and thus mitigated the effects of distortion; however, the design's filter topology was not low-noise, and the nature of the nonlinear gain-control circuit was such that the circuit increased the noise further. Thus, the effects of noise accumulation and amplification limited our ability to attain a wide dynamic range.

In this paper we describe a cochlea that attains a dynamic range of 61dB at the BF of a typical cochlear stage by using four techniques:

1. The previously described WLR
2. A low-noise second-order filter topology
3. Dynamic gain control (AGC)
4. The architecture of *overlapping cochlear cascades*

In addition, we use three techniques that ensure the presence of a robust infrastructure in the cochlea:

1. Automatic offset-compensation circuitry in each cochlear filter prevents offset accumulation along the cochlea.
2. Cascode circuitry in the WLRs increase the latter's DC gain, and prevent low-frequency signal attenuation in the cochlea.
3. Translinear bipolar biasing circuits provide  $Q$ s that are approximately invariant with corner frequency, and allow better matching. Bipolar biasing circuits were first used in cochlear designs by [18].

We shall discuss all of these preceding techniques in this paper.

The organization of this paper is as follows: In Section 4.2 we discuss the architecture and properties of a single cochlear stage. In Section 4.3 we discuss the architecture and properties of the cochlea. In Section 4.4 we compare analog and digital cochlear implementations with respect to power and area consumption. In Section 4.5, we discuss the relationship between our electronic cochlea and the biological cochlea. In Section 4.6, we discuss possible applications of the electronic cochlea for cochlear implants. In Section 4.7, we summarize our contributions.

## 4.2 The Single Cochlear Stage

Figure 4.1 shows a schematic for a single cochlear stage. The arrows indicate the direction of information flow (input to output). The second-order filter (SOS) is composed of two WLR amplifiers, two capacitors, and offset-compensation circuitry (LPF and OCR). The corner frequency  $1/\tau$  and quality factor  $Q$  of the filter are proportional to  $\sqrt{I_1 I_2}$  and  $\sqrt{I_1/I_2}$ , respectively, where  $I_1$  and  $I_2$  are the bias currents of the WLR amplifiers. The tau-and- $Q$  control circuit controls the values of the currents  $I_1$  and  $I_2$  such that the value of  $1/\tau$  depends on only the bias voltage  $V_T$ , and the small-signal value of  $Q$  depends only on the bias voltage  $V_Q$ . An AGC correction current  $I_A$  attenuates the small-signal value of  $Q$  at large-signal levels in a graded fashion.

The inner-hair-cell circuit (IHC) rectifies, differentiates, and transduces the input voltage to a current  $I_{hr}$ . The voltage  $V_A$  controls the value of an internal amplifier bias current in the IHC. The voltage  $V_{HR}$  controls the transduction gain of the IHC. The peak detector (PD) extracts the peak value of  $I_{hr}$  as a DC current  $I_{pk}$ . The current  $I_{pk}$  becomes the AGC correction-current input ( $I_A$ ) to the tau-and- $Q$  control circuit. The bias voltage  $V_{PT}$  determines the time constant of the peak detector, and thus the response time of the AGC. The peak detector is designed such that it can respond to increases in input intensity within one cycle of a sinusoidal input at  $V_{in}$ ; its response to decreases in input intensity is much slower and is determined by  $V_{PT}$ .

The offset-compensation circuit is composed of a lowpass filter (LPF) whose time constant is determined by  $V_{OT}$ . The LPF extracts the DC voltage of the filter's intermediate node, and compares this voltage with a global reference voltage  $V_{RF}$  in the offset-correction

block (OCR). The OCR applies a correction current to the intermediate node to restore that node's voltage to a value near  $V_{RF}$ . The DC voltage of the output node is then also near  $V_{RF}$ , because the systematic offset voltage of a WLR amplifier is a small negative voltage. The maximal correction current of the OCR scales with the bias current  $I_1$ ; the bias voltage  $V_{OF}$  controls the scaling ratio. Since the restoration is performed at every cochlear stage, the output voltage of each stage is near  $V_{RF}$ , and offset does not accumulate across the cochlea. If there were no offset adaptation, a systematic offset voltage in any one stage would accumulate across the whole cochlea.

Since the gain-control topology is feedforward, rather than feedback, we avoid instabilities or oscillations in the  $Q$ . However, since raising  $Q$ s lowers the DC voltage, and the DC voltage does have a mild influence on the  $Q$ , the DC and AC output-voltage dynamics are weakly dependent on each other.

We shall now describe the details of each of the circuits in Figure 4.1. In Section 4.2.1 we discuss the WLR circuit. In Section 4.2.2, we describe the offset-adaptation circuit. In Section 4.2.3, we examine the filter topology. In Section 4.2.4 we present the translinear tau-and- $Q$  control circuit. In Section 4.2.5, we describe the circuits in the IHC and PD blocks. In Section 4.2.6, we discuss the overall properties of an entire cochlear stage.

### 4.2.1 The WLR

The WLR has been described in great detail [10]. The version of the WLR that we use in our cochlea, however, has been slightly modified, so we shall describe it briefly. Figure 4.2 shows the circuit of the transconductance amplifier. The inputs  $v_+$  and  $v_-$  are the wells of the W transistors; we use the well, instead of the gate, to lower amplifier transconductance and consequently to widen the linear range of the amplifier. The linear range is further widened through the novel technique of gate degeneration via the GM transistors, and through the technique of bump linearization via the B transistors [10]. The GM-M mirrors are attenuating, with a 1:3 ratio, to avoid parasitic-capacitance effects in the differential pair. The CP and CN transistors function as cascode transistors; they ensure that the DC gain of the amplifier is high such that there is no significant low-frequency attenuation in the cochlea (See Section 4.3.1 for further details.). We use CP and CN transistors on both arms of the amplifier to avoid any systematic offsets. The CP and CN transistors do not alter the noise performance of the amplifier, since their noise currents contribute little to the

output current of the amplifier. The  $p$ FET M transistors implement current mirrors. The bias current of the amplifier  $I_B$  is provided by bipolar transistors in the tau-and- $Q$  biasing circuit. The extra mirror necessary to convert NPN bipolar collector currents to  $p$ FET bias currents does not alter the noise performance of the amplifier. The offset-correction circuit adds two correction currents at the  $V_{ol}$  and  $V_{or}$  nodes. In the filter of Figure 4.1, only the left amplifier has correction-current inputs from the OCR.

## 4.2.2 The Offset-Adaptation Circuit

Figure 4.3 shows the offset-adaptation circuit. The LPF is a simple 5-transistor  $n$ FET OTA-C filter operated in the subthreshold regime. The DC value of the  $V_1$  input is extracted by the LPF and is compared with  $V_{RF}$  in the  $p$ FET differential pair. The currents in the arms of the differential pair are steered via mirrors to the  $V_{ol}$  and  $V_{or}$  inputs of the left WLR in Figure 4.1, such that the sign of the feedback is negative. The cascoding of the offset-correction currents prevents the offset-correction circuitry from degrading the DC gain of the amplifier. The  $V_B$  gate voltage of the left WLR, as revealed in Figure 4.2, is also the  $V_B$  gate voltage in the offset-adaptation circuit, such that the offset-correction current scales with the bias current of the WLR. The scaling ratio is controlled by the source control  $V_{OF}$ .

The value of  $V_{OF}$ , which determines the loop gain of the offset-adaptation loop, and the value of  $V_{OT}$  determine the closed-loop time constant of the offset-adaptation loop. A high loop gain speeds up the closed-loop response such that the influence of low-frequency inputs is adapted away. Thus, there is a tradeoff between strong offset control (high loop gain), which implies some ringing and overshoot as well, and coupling of low-frequency inputs into the cochlea. Since our lowest-frequency input is 100Hz, we have been able to maintain a good control of the DC offset in the cochlea without attenuating any frequencies of interest.

Note that the offset-correction circuitry can correct offsets to only a resolution that is limited by its own offsets. Since we use subthreshold circuitry with small linear ranges in the OCR and LPF, these offsets are on the order of 5mV to 15mV; they are small compared with the 1V linear range of the WLR. The offset-correction scheme would have been useless if we had used WLRs to sense and correct the offset of other WLRs.

### 4.2.3 The Second-Order Filter

Figure 4.4 shows representations of our second-order filter. The block-diagram form of part (b) is convenient for doing noise calculations. For the purposes of doing noise calculations we list 12 algebraic relationships:

$$g_{m1} = \frac{I_1}{V_L}. \quad (4.1)$$

$$g_{m2} = \frac{I_2}{V_L}. \quad (4.2)$$

$$\tau_1 = \frac{C_1}{g_{m1}}. \quad (4.3)$$

$$\tau_2 = \frac{C_2}{g_{m2}}. \quad (4.4)$$

$$\tau = \sqrt{\tau_1 \tau_2}. \quad (4.5)$$

$$I_1 = \frac{C_1 V_L}{\tau_1}. \quad (4.6)$$

$$I_2 = \frac{C_2 V_L}{\tau_2}. \quad (4.7)$$

$$Q = \sqrt{\frac{\tau_2}{\tau_1}}. \quad (4.8)$$

$$\tau_1 = \frac{\tau}{Q}. \quad (4.9)$$

$$\tau_2 = \tau Q. \quad (4.10)$$

$$C_R = \frac{C_2}{C_1}. \quad (4.11)$$

$$C = \sqrt{C_1 C_2}. \quad (4.12)$$

The currents  $I_1$  and  $I_2$  are the bias currents of the amplifiers,  $V_L$  is the linear range of these amplifiers, and the transconductance  $g_{mi}$  of amplifier  $i$  is given by  $g_{mi} = I_i/V_L$ . The noise source  $v_{ni}$ , shown in Figure 4.4(b), represents the input-referred noise per unit bandwidth of amplifier  $i$ . From [10], we know that

$$v_{ni}^2 = NqV_L^2/I_i, \quad (4.13)$$

where  $N$  is the effective number of shot-noise sources in the amplifier, and  $q$  is the charge on the electron. For our amplifiers,  $N$  is typically 4.8, whereas the amplifiers reported in [10] have  $N = 5.3$ .

From Figure 4.4(b) and the preceding algebraic relationships, it may be shown that the

output noise per unit bandwidth  $v_{no}$  is given by

$$v_{no} = \frac{v_{n1} + v_{n2}(\tau s/Q)}{\tau^2 s^2 + \tau s/Q + 1}, \quad (4.14)$$

$$v_{no}^2 = \frac{v_{n1}^2 + |\tau^2 s^2/Q^2| v_{n2}^2}{|\tau^2 s^2 + \tau s/Q + 1|^2}. \quad (4.15)$$

In Eq. (4.15) we have used the fact that the noise sources  $v_{n1}$  and  $v_{n2}$  are uncorrelated, so there are no cross terms of the form  $v_{n1}v_{n2}$ . From the algebraic relationships of Eqs. (4.1) through (4.12), by substituting  $s = \omega\tau$  and  $\omega = 2\pi f$ , and by using the normalized frequency  $x = \omega\tau$ , we can show that

$$v_{no}^2(f)df = \frac{(NqV_L/QC_1) \left(1 + \frac{\omega^2\tau^2}{C_R}\right)}{(1 - \omega^2\tau^2)^2 + \frac{\omega^2\tau^2}{Q^2}} df, \quad (4.16)$$

$$v_{no}^2(x)dx = \left(\frac{NqV_L}{2\pi QC_1}\right) |H(x)|^2 \left(1 + \frac{x^2}{C_R}\right) dx, \quad (4.17)$$

where  $H(x)$  represents the normalized transfer function of a second-order filter,

$$H(x) = \frac{1}{1 - x^2 + jx/Q}, \quad (4.18)$$

and  $j$  is the square root of -1. To get the total noise over all frequencies, we integrate the LHS and RHS of Eq. (4.17) from 0 to  $\infty$ . It can be shown by contour integration that

$$\int_0^\infty |H(x)|^2 dx = \frac{\pi}{2} Q, \quad (4.19)$$

$$\int_0^\infty x^2 |H(x)|^2 dx = \frac{\pi}{2} Q. \quad (4.20)$$

$$(4.21)$$

The total output noise over all frequencies  $\langle v_{no}^2 \rangle$  is then given by

$$\langle v_{no}^2 \rangle = \frac{1}{2\pi} \left(\frac{NqV_L}{QC_1}\right) \left(\frac{\pi}{2} Q + \frac{\pi}{2} Q \left(\frac{1}{C_R}\right)\right), \quad (4.22)$$

$$= \left(\frac{NqV_L}{4C_1}\right) \left(1 + \frac{1}{C_R}\right), \quad (4.23)$$

$$= \left(\frac{NqV_L}{4C}\right) \left(\sqrt{C_R} + \frac{1}{\sqrt{C_R}}\right). \quad (4.24)$$

Note that the total output noise is independent of  $Q$  for this topology: The noise per unit bandwidth scales like  $1/Q$ , and the integration of the noise over all bandwidths scales like  $Q$ , so that the total output noise is independent of  $Q$ . These relationships are reminiscent of an LCR circuit where the total output current noise depends on only the inductance, the total output voltage noise depends on only the capacitance, and neither of these noises depends on  $R$ ; only the noise per unit bandwidth and the  $Q$  of the LCR circuit are influenced by  $R$ . In fact, it can be shown that this topology has a transfer function and noise properties that are similar to those of an LCR circuit if we make the identifications

$$\tau_1 = L/R, \quad (4.25)$$

$$\tau_2 = RC. \quad (4.26)$$

For a given value of  $C$  (the geometric mean of  $C_1$  and  $C_2$ ), the total output noise is minimized if  $C_R = 1$ —that is, if  $C_1 = C_2$ .

Figure 4.5 shows the noise spectral density versus frequency and the total integrated noise at the output over all frequencies. The data were obtained from a test chip that contained a second-order filter with amplifiers identical to those in our previous report [10]. The lines are fits to theory. As we expect, the total integrated noise is quite constant with  $Q$ . The parameters used in the fits were  $N = 5.3$ ,  $V_L = 1\text{V}$ ,  $C_R = 1.43$ ,  $q = 1.6 \times 10^{-19}$ , and  $C = 697\text{fF}$ . The values of  $N$  and  $V_L$  were obtained from measurements on our transconductance amplifiers [10]. The value of  $C_R$  was obtained from least-squares fits to the data. We obtained the value of  $C$  by having the noise measurements be consistent with values of  $C$  expected from the layout.

In filter topologies that have been used in prior cochlear designs e.g. [4] or [9], the noise per unit bandwidth increases with  $Q$ : The  $Q$  is obtained through the addition of positive-feedback currents. These currents contribute additional shot noise and thus increase the noise per unit bandwidth; in these topologies, the integrated noise over all frequencies also increases with  $Q$ , so both factors contribute to the increase in noise with  $Q$ . Although we have performed extensive experimental and theoretical analysis of noise in these filter topologies as well, we shall present only key findings here: For the topology presented in [4], at  $Q$ s near 2.5, the rms noise power at the output is 9 times higher than it is for our topology. For  $Q$ s near 0.707, the rms noise power at the output is about 0.8 times

lower than it is for our topology. For  $Q$ s near 1.5, which is where we typically operate, the rms noise power at the output is about 2 times higher than it is for our topology. The effects of increased noise per unit bandwidth in a single second-order filter are greatly amplified in a cochlear cascade. Factors of 2 in noise reduction in a single stage can make a significant reduction in the output noise of a cochlear cascade. Thus, using our filter topology contributes significantly to reducing noise in a cochlear cascade.

Although the noise properties of the filter of Figure 4.4 are superior to those of other second-order topologies, this filter's distortion at large amplitudes is significantly greater, especially for  $Q$ s greater than 1.0: Distortion arises when there are large differential voltages across the transconductance-amplifier inputs in a filter. The feedback to the first amplifier of Figure 4.4 arises from  $V_2$ , rather than from  $V_1$ , in contrast to the topology of [4]. Consequently, the accumulation of phase shift from two amplifiers, as opposed to that from one amplifier used in earlier topologies, causes greater differential voltages and greater distortion in the first amplifier. Also, the transfer function of the intermediate node  $V_1$  is such that the magnitude of voltage at this node is greater than that in other topologies for  $Q$ s greater than 1.0. Consequently, the differential voltage across the second amplifier is larger, and the distortion from the second amplifier is also greater.

It is instructive to find the largest input signal at the BF of a filter for which the total harmonic distortion (THD) is about 3%–5%. The amplitude of this signal,  $v_{mx}$ , is a good measure of the upper limit of dynamic range for a filter, in the same way that the input-referred noise is a good measure of the lower limit of dynamic range. Figure 4.6 shows the rms amplitude  $v_{mx}$  at a BF of 140Hz for the filter of Figure 4.4. We observe that, as the  $Q$  increases, the distortion increases, and the value of  $v_{mx}$  falls. The data were obtained for a THD level of 3.3% (30dB attenuation in intensity). The data were *empirically* fit by the equation

$$v_{mx}(Q) = 128 - 161 \ln \left( \frac{Q}{1.75} \right). \quad (4.27)$$

The preceding discussion illustrates why an AGC is essential for attaining a wide dynamic range with our filter topology: The noise properties of the topology are favorable for sensing signals at small amplitudes, and with high  $Q$ s. However, when the signal levels are large, if the distortion is to be kept under control, the  $Q$ s must be attenuated. The AGC ensures that the  $Q$ s are large when the signal is small, and are small when the signal is



large.

#### 4.2.4 The Tau-and- $Q$ Control Circuit

In Figure 4.7, we make the following definitions:

$$I_\tau = I_s e^{V_T/2U_T}, \quad (4.28)$$

$$Q_0 = e^{V_Q/2U_T}, \quad (4.29)$$

where  $U_T = kT/q$  is the thermal voltage, and  $I_s$  is the bipolar preexponential constant. The current  $I_A$  is a place holder for an AGC correction current from the IHC and peak-detector circuit, and  $I_1$  and  $I_2$  are output currents that bias the first and second amplifiers of Figure 4.4, respectively. A simple translinear analysis and the solution of the quadratic equation reveal that, if we define  $\eta$  to be a normalized AGC correction current, according to

$$\eta = \left( \frac{I_A}{2I_\tau/Q_0} \right), \quad (4.30)$$

then

$$Q = \sqrt{\frac{I_1}{I_2}}, \quad (4.31)$$

$$= Q_0 \sqrt{\left( \frac{\sqrt{1+\eta^2} - \eta}{\sqrt{1+\eta^2} + \eta} \right)}. \quad (4.32)$$

Independent of the value of  $I_A$ , the translinear circuit always ensures that

$$\sqrt{I_1 I_2} = I_\tau. \quad (4.33)$$

Thus, it is an effective tau-and- $Q$  biasing circuit for the filter in Figure 4.4, since it ensures that the AGC affects the  $Q$  but not the corner frequency of the filter. If we let

$$\theta = \arctan \eta, \quad (4.34)$$

then trigonometric manipulations of Eq. (4.32) reveal that

$$Q = Q_0 \tan \left( \frac{\pi}{4} - \frac{\theta}{2} \right). \quad (4.35)$$

If there is no AGC correction current, then  $\theta = 0$  and  $Q = Q_0$ . In the limit of an infinite AGC correction current,  $\theta/2 = \pi/4$  and  $Q = 0$ .

Figure 4.8(a) shows the corner frequency of the filter in Figure 4.4 as a function of the bias voltage  $V_T$ . As we expect from Eq. (4.28) and (4.33), and from the equations of the filter (Eqs. 4.1 to (4.12)), the corner frequency is an exponential function of the bias voltage  $V_T$ . The exponential preconstant yields a thermal voltage of 26.7mV, which is fairly close to the expected thermal voltage of 26mV at a room temperature of 300K.

Figure 4.8(b) shows the  $Q$  of the filter in the absence of any AGC correction current. As we expect from Eq. (4.29) and Eq. (4.35) with  $\eta = 0$  (no AGC current), the  $Q$  is an exponential function of the bias voltage  $V_Q$ . The exponential preconstant yields a thermal voltage of 26.3mV, which is fairly close to the expected thermal voltage of 26mV at a room temperature of 300K.

#### 4.2.5 The Inner Hair Cell and Peak-Detector Circuits

Figure 4.9 shows the IHC and PD circuits. The amplifier in the IHC is a simple 5-transistor  $n$ FET OTA with a fairly high gain (500 to 1000). The bias current of the OTA is determined by the voltage  $V_A$ . The bias current should be sufficiently high that the dynamics of the node  $V_h$  are much faster than the dynamics of the node  $V_n$ , for all input frequencies and amplitudes of interest. Since the OTA is connected in a follower configuration, the voltage  $V_n$  is very nearly a copy of  $V_{in}$ , except for very weak signals, where the bipolar transistor BA or the MOS transistor PA are not sufficiently turned on. In practice, the signals or noise at the cochlear output taps are sufficiently high that BA or PA may be assumed always to be sufficiently turned on. When  $V_{in}$  or  $V_n$  are rising, the capacitor  $C_{HR}$  is charged primarily by the bipolar transistor BA. When  $V_{in}$  or  $V_n$  are falling, the capacitor  $C_{HR}$  is charged primarily by the MOS transistor PA. Thus, during the phases of the signal when the derivative of the signal is negative, the current  $I_{hr}$  is an amplified copy of  $C_{HR}dV_{in}/dt$ . The amplification factor is given by  $\exp(V_{HR}/U_T)$ . Thus, the IHC differentiates, rectifies, amplifies, and transforms the input voltage  $V_{in}$  into an output current  $I_{hr}$ .

The output current  $I_{hr}$  is fed into the peak detector. The peak detector consists of a slow source follower, composed of PF, PT, and  $C_{PT}$ , and the feedback transistor PI. The transistor PO outputs a copy of the current in PI as  $I_{pk}$ . The source follower can follow descending signals in  $V_f$  rapidly because of the exponential dependence of the current of

PF on its gate voltage. However, the voltage  $V_{PT}$  is set near  $V_{DD}$  so that the current source formed by the transistor PT is slow in charging the capacitor  $C_{PT}$ ; consequently, during ascending signals in  $V_f$ , the voltage  $V_s$  is slow to respond. Because of the feedback nature of the circuit, and the asymmetry in the time constants of the source follower,  $V_s$  will equilibrate at a value such that the average current through PI is slightly below the peak value of  $I_{hr}$ . As  $I_{hr}$  alternately reaches its peak and moves below that peak, the voltage  $V_f$  will undergo large swings due to the high gain of the input node of the peak detector. In contrast, the voltage  $V_s$  will have only small variations from its DC value; they constitute the ripple of the peak detector.

Figure 4.10 shows the waveforms  $V_{in}$ ,  $V_n$ ,  $V_h$ ,  $V_f$ , and  $V_s$ . The labeled voltages in the figure indicate the DC voltage values that correspond to the horizontal location of the arrow. As we expect,  $V_{in}$  and  $V_n$  are very nearly equal to each other. The voltage  $V_h$  undergoes abrupt transitions during changes in the sign of the input derivative; these changes correspond to a transition from BA being turned off to PA being turned on or vice versa. The voltages  $V_f$  and  $V_s$  in the peak detector undergo rapid downward transitions that are phase locked to the downward-going zero crossings of the input waveform where the peak value of  $I_{hr}$  occurs. The upward transitions in  $V_f$  and  $V_s$  are slow because of the sluggishness of the current-source transistor PT. The data were taken with  $V_{in}$  being a 102mV rms input at 1kHz, with  $V_A = 1.0V$ , with  $V_{PT} = 4.039V$ ,  $V_{DD} = 5.0V$ , and with  $V_{HR} = 100mV$ . Typically, we operate  $V_{PT}$  near 4.25V, which results in no discernible ripple in  $V_s$ , but these data were taken specifically to illustrate better the workings of the peak detector. The transistor PT was fabricated as a poly2 transistor. Thus, at the same current level, the bias voltages on  $V_{PT}$  are higher than those corresponding to bias voltages on a poly1 transistor.

From the preceding discussion, we expect that the value of  $I_{pk}$  will be near the peak value of  $C_{HR}dV_{in}/dt$  amplified by the factor of  $\exp(V_{HR}/U_T)$ . Thus, if the input amplitude were given by

$$V_{in} = a_{in} \sin(2\pi f_{in}t), \quad (4.36)$$

then the value of  $I_{pk}$  would be given by

$$I_{pk} = 2\pi f_{in} C_{HR} a_{in} e^{V_{HR}/U_T}. \quad (4.37)$$

In conformance with Eq. (4.37), Figure 4.11 shows that the response of  $I_{pk}$  is linear with the amplitude and with the frequency of the input. The data were taken for  $V_A = 1.0\text{V}$ , and  $V_{PT} = 4.3\text{V}$ . The experimental slopes for Figure 4.11(a) and Figure 4.11(b) yielded values for  $C_{HR} = 335\text{fF}$  and  $C_{HR} = 313\text{fF}$ , respectively. However, the linear fits to the data reveal that an offset in amplitude of about  $77.5\text{mV rms}$  in the case of Figure 4.11(a), and an offset in frequency of about  $276\text{Hz}$  in the case of Figure 4.11(b), needs to be subtracted from  $a_{in}$  or  $f_{in}$ , respectively. These offsets imply that there is a minimum amount of input current  $I_{hr}$  that is required for the peak detector to output a current  $I_{pk}$ . Through experimentation, we have found that this minimum value scales approximately linearly with frequency such that the offset for  $a_{in}$  always lies somewhere in the  $50$  to  $100\text{mV rms}$  region (for a  $V_{HR}$  of about  $100\text{mV}$ ). At this time, we do not have a good explanation of what causes these offsets; we suspect that they are due to the short-channel length and small Early Voltage of transistor PI.

Figure 4.12 shows that the relationship between  $I_{pk}$  and  $V_{HR}$  is described by an exponential, as Eq. (4.37) predicts. The thermal voltage  $U_T$  was determined to be around  $29.9\text{mV}$ . This voltage is somewhat higher than the  $26\text{mV}$  expected from theory. The data were taken with  $V_{PT} = 4.30\text{V}$ , and  $V_A = 1.15\text{V}$ .

The current  $I_{pk}$  is mirrored by the bipolar transistors BP and BO in Figure 4.9 to function as the AGC correction current  $I_A$  in Figure 4.7. From Eqs. 4.1 to (4.12), we know that  $I_\tau$  is given by  $2\pi f_c C V_L$ , where  $f_c = 1/\tau$  is the corner frequency (CF) of the filter. Thus,  $\eta$  in Eq. (4.30) is given by

$$\eta = \frac{I_A}{2I_\tau/Q_0}, \quad (4.38)$$

$$= Q_0 e^{V_{HR}/U_T} \left( \frac{f_{in}}{f_c} \right) \left( \frac{C_{HR}}{2C} \right) \left( \frac{a_{in}}{V_L} \right). \quad (4.39)$$

Thus, the voltage  $V_{HR}$  serves to strengthen or weaken the normalized AGC correction factor  $\eta$ .

#### 4.2.6 The Properties of an Entire Cochlear Stage

Figure 4.13 shows the frequency-response characteristics of the filter of Figure 4.4 for different input amplitudes. In the absence of an AGC, large input amplitudes generate large

amounts of distortion in the filter; thus, in Figure 4.13(a), it was impossible to obtain smooth frequency responses beyond an input rms amplitude of 250mV. In contrast, in Figure 4.13(b), we could easily obtain smooth frequency responses up to (and even beyond) input amplitudes of 1V rms, because of the presence of an AGC. If the frequency-response curves are fitted with the transfer function of a second-order section,

$$H(s) = \frac{1}{\tau^2 s^2 + \tau s/Q + 1}, \quad (4.40)$$

then we find that the CF ( $1/\tau$ ) is reduced with input amplitude, and the  $Q$  is reduced by the AGC as well. In Figure 4.13(b), the CF is reduced from 147Hz at small signals to 112Hz at large signals; the  $Q$  is reduced from 2.22 at small signals to about 0.52 at large signals. These numbers are valid for  $V_{HR} = 65\text{mV}$ , and  $V_{PT} = 4.25\text{V}$ . Given that we designed Eq. (4.33) in our translinear biasing circuit to keep the CF constant, it may seem surprising that the CF changed with input amplitude. However, we must realize that we are fitting the frequency-response curves of a nonlinear system with a linear approximation given by Eq. (4.40) at each rms input amplitude. According to Eqs. (4.39) and (4.32), for the same input rms amplitude, the “ $Q$ ” is lower at high frequencies than at low frequencies. The frequency dependence of the  $Q$  results in disproportionately more attenuation of the input at high frequencies than at low frequencies, such that the CF, as measured by the amplitude curves, appears to shift.

If we plot the  $CF_{90}$ —that is to say the frequency at which the the second-order filter has a phase lag of 90 degrees—versus rms input amplitude, then the data of Figure 4.14 reveal that  $CF_{90}$  is approximately constant. At low input amplitudes, the AGC has no effect, because  $I_{pk}$  provides no correction until the input amplitude is above a certain threshold, as we discussed in Section 4.2.5. Even if there were no offset, the AGC correction in this regime would be small. Thus, the system is linear at low amplitudes. Consequently, at these amplitudes, the  $CF_{90}$  is identical with  $1/\tau$  and with the CF measured by gain curves. Since the AGC is designed not to affect the parameter  $\tau$ , the  $CF_{90}$  remains approximately invariant with input amplitude, even at high amplitudes where the AGC is active. In fact, Figure 4.14 shows that a strong AGC (higher values of  $V_{HR}$ ) improves the constancy of the  $CF_{90}$  with amplitude, because it prevents static nonlinear shifts in  $CF_{90}$  that increase at high  $Q$ s. The  $CF_{90}$  is the frequency near which center-surround schemes, e.g., those

that perform spectral extraction on cochlear outputs for use in implants [11], generate their maximum output. Thus, the fact that the  $CF_{90}$  is approximately invariant with amplitude makes our AGC cochlea attractive as a front end for center-surround postprocessing.

Figure 4.15(a) shows data for  $Q$  versus  $a_{in}$  measured for three different values of  $V_{HR}$  for the second-order filter. From Eqs. (4.30), (4.34), and (4.35) we would expect the curves to be fit by a function of the form

$$Q = Q_0 \tan \left( \frac{\pi}{4} - \frac{\arctan(Ga_{in})}{2} \right). \quad (4.41)$$

However, from the discussion of Section 4.2.5, we know that  $a_{in}$  in Eq. (4.41) should be replaced by 0 below some threshold value  $a_0$ , and by  $a_{in} - a_0$  above this threshold value. The fits in Figure 4.15(a) are functional fits to Eq. (4.41) with the free parameter  $G$ , and the additional free parameter  $a_0$ . For  $V_{HR} = 3\text{mV}$ ,  $32\text{mV}$ , and  $65\text{mV}$ , we found  $G = 1.93, 2.5, 4$ , and  $a_0 = 0.164, 0.095, 0.06$ , respectively;  $Q_0$  was 2.05 for all curves,  $a_{in}$  and  $a_0$  are in units of V. We took data by measuring the gain of the filter at  $f_{in} = f_c = CF_{90} = 1/\tau$ , which, for a second-order filter, is  $Q$ . Figure 4.15(b) plots the output amplitude,  $Q(a_{in}) \times a_{in}$ , rather than  $Q(a_{in})$ , at this frequency. We observe that, before the AGC turns on ( $a_{in} < a_0$ ), the relationship between the input and output amplitudes is linear. After the AGC turns on ( $a_{in} > a_0$ ), the relationship between the output and input amplitudes is compressive, although not as compressive as theory would predict. Since  $a_0$  is large for small values of  $V_{HR}$ , the range of linearity is large for small values of  $V_{HR}$ .

Figure 4.15 suggests that, at large amplitudes, the static nonlinearities in the filter increase the  $Q$  slightly. Since the  $Q$  of the filter is given by  $\sqrt{\frac{\tau_2}{\tau_1}}$ , we deduce that the static nonlinearity is causing  $\tau_2$  to increase faster with  $a_{in}$  than  $\tau_1$ ; this deduction is in accordance with the intuition that the second amplifier in Figure 4.4 is subject to greater differential voltages, and, consequently, to more saturation and slowing than the first amplifier. One way to avoid, or even to reverse, the nonlinear shift toward higher  $Q$ s is to have the linear range of the first amplifier be smaller than the linear range of the second amplifier.

The nature of Eq. (4.41) is such that, independent of the value of  $G$ ,  $Q(a_{in})a_{in}$  is a monotonically increasing function of  $a_{in}$ . This property guarantees that the input-output curve at the BF of a cochlear stage is always monotonically increasing, as confirmed by the data of Figure 4.15.

Figure 4.16 shows that the harmonic-distortion levels at 1V rms with an AGC are comparable with the harmonic-distortion levels at 250mV rms without an AGC. The AGC data were taken with  $V_{hr} = 65\text{mV}$ . Figure 4.17 shows that a strong AGC (large value of  $V_{HR}$ ) reduces harmonic distortion due to the lowering of  $Q$ .

Figure 4.18 illustrates the dynamics of  $Q$  adaptation: The stimulus is a pure tone at the BF of the filter that turns on suddenly after a period of silence, persists for a while, and then abruptly decreases in intensity to a quieter tone. At the onset of the tone, a transient response is seen at the output. The transient causes the peak detector to overadapt instantly within one cycle. The overadaptation is corrected by the slow capacitive charging of the peak-detector current source, which restores the  $Q$ , and thus the output amplitude, to an equilibrium value. When the tone transitions from loud to soft, the initial response to the soft tone is moderate due to the low  $Q$  caused by adaptation to the preceding loud tone. Eventually, the slow capacitive charging of the peak-detector current source restores the  $Q$ , and thus the output amplitude, to an equilibrium value.

### 4.3 Properties of the Cochlea

In this section, we shall discuss the properties of the cochlea. We shall begin with a discussion of low-frequency attenuation because the discussion will motivate the introduction of our overlapping-cascades architecture.

#### 4.3.1 Low-Frequency Attenuation

If the open-loop gains of the amplifiers in Figure 4.4 are  $A_1$  and  $A_2$ , then we can show that we obtain the low-frequency gain of the filter of Figure 4.4 by simply replacing  $\tau_1 s$  and  $\tau_2 s$  with  $1/A_1$  and  $1/A_2$  in the transfer function. Thus, from Eq. (4.40) the low-frequency gain  $H_0$  is given by

$$H_0 = \frac{1}{1 + \frac{1}{A_1} + \frac{1}{A_1 A_2}} \quad (4.42)$$

$$\approx \frac{A_1}{A_1 + 1}. \quad (4.43)$$

Although  $H_0$  is very close to 1, it is not exactly 1. A low-frequency input that travels through  $M$  stages of a cochlea will suffer a net attenuation,  $H_M$ , given by

$$H_M = \left( \frac{A_1}{A_1 + 1} \right)^M, \quad (4.44)$$

$$\approx e^{-M/A_1}, \quad (4.45)$$

where the exponential approximation is valid if  $A_1$  is a large number. Now,  $A_1 = 2V_0/V_L$ , where  $V_L$  is the linear range of the amplifier and  $V_0$  is its effective Early voltage at the output of the amplifier [10]. In the  $1.2\mu\text{m}$  *n*well Orbit MOSIS process used to fabricate our circuits,  $V_0$  is around 20V for wide-linear-range amplifiers that do not have cascode transistors at the output;  $V_L = 1\text{V}$ , and  $A_1$  is about 40. Thus, we can expect an attenuation of almost one e-fold across a 39-stage cochlea built with cascodeless amplifiers.

Figure 4.19 shows the low-frequency attenuation of a 40Hz 50mV input to a 39-stage cochlea tuned from 900Hz to 100Hz for different values of the parameter  $A_1$ . For these experiments, we operated the cochlea with a very low  $Q$  ( $V_Q = -80\text{mV}$ ) so that we could focuss on just the effects of low-frequency attenuation. We varied the value of  $A_1$  by varying the bias of the cascode transistors  $V_{CN}$  and  $V_{CP}$ , in the amplifier of Figure 4.2. We explored the effects of turning off the cascode transistors by biasing them as switches. Thus, to turn off the CN cascode transistors, we would set  $V_{CN}$  to 5V; to turn off the CP cascode transistors we would set  $V_{CP}$  to 0V. Figure 4.19 shows the low-frequency attenuation for the four cases of both cascodes on, both cascodes off, only N cascodes off, or only P cascodes off. We observe from the data that the P cascodes are more helpful in reducing low-frequency attenuation than are the N cascodes, because the *p*FETs in our process have a lower Early voltage than do the *n*FETs. With both cascodes on, a 39-stage cochlea has a net attenuation that is less than 0.8. We normally operate the cochlea with both cascodes on, with  $V_{CN} = 1.2\text{V}$ , and with  $V_{CP} = 3.8\text{V}$ . These bias values permit operation of our amplifiers over the entire frequency range of the cochlea without any saturation effects for input rms amplitudes that exceed 1V rms.

The attenuation of the gain of signals at other frequencies is by the same factor  $H_M$ . In contrast, the output noise (or distortion) at a cochlear tap is accumulated through addition over successive stages, as shown in Figure 4.20. The noise that is added at the input is attenuated by the same amount as the signal, but the amounts of noise that are added at



stages successively closer to the output tap of interest are attenuated by successively smaller amounts. Thus, the output SNR is degraded by low-frequency attenuation.

To limit the degradation of the SNR of the cochlea through low-frequency attenuation, and noise-and-distortion accumulation, we use the architecture of overlapping cascades shown in Figure 4.21. Rather than having one large cochlea, we use a few small cochleas whose frequency ranges overlap by one octave. All such cochleas process the input in parallel. The filters in the overlapping octave serve to mimic the effects of the infinite cascade prior to the stages of interest; the outputs of these filters are not used. Since most of the effect of the infinite cascade occurs within an octave of the corner frequency of a cochlear stage, we do not sacrifice much in the way of cochlear modeling, but we do gain significantly in limiting our SNR degradation. In general, the amount of overlap between cochleas, and the number of stages per cochlea can be varied to suit the nature of the cochlear application.

Although the thermal noise in an infinite cascade converges to an equilibrium where noise accumulation is matched by noise filtering, the  $1/f$  noise in an infinite cascade does not converge and continues to grow in the cascade. The  $1/f$  noise is significant for only those high-frequency cochlear stages that have amplifiers with large bias currents [10]. The overlapping-cascades architecture helps to limit the accumulation of  $1/f$  noise.

A cochlear cascade that is composed of all-pole second-order filters overestimates the group delay of the biological cochlea. The overlapping-cascades architecture also helps to reduce the group delay of the silicon cochlea.

The architecture of overlapping cascades may be viewed as a hybrid of an architecture that has many parallel filters in a filter bank and of one that has one filter cascade with all the filters in serial.

The cochlea that we discuss in this paper was built out of three 39-stage overlapping cochlear cascades: The low-frequency cochlear cascade was tuned to operate in the 100Hz to 900Hz region. The mid-frequency cochlear cascade was tuned to operate in the 450Hz to 4050Hz region. The high-frequency cochlear cascade was tuned to operate in the 2000Hz to 18,000Hz region. Thus, each of the cochlear cascades had about 11.2 filters per octave, ensuring a fairly sharp cochlear rolloff slope. The  $Q$ s of the cochleas were tuned to be approximately 1.5. The voltage gradients in  $V_T$  corresponding to the three frequency gradients of the low-frequency, mid-frequency, and high-frequency cochlear cascades were 1.040 to 0.9V, 1.130 to 0.990V, and 1.210 to 1.070V respectively. The value of  $V_Q$  that

was suitable for operating all three cochleas was  $-52\text{mV}$ . For the remainder of the paper, we shall focus on the operation of the low-frequency cochlear cascade, which we shall call the cochlea. The operation of the other cochlear cascades follows by straightforward generalization. The other parameters that we used for operating our cascades were  $V_{OL} = 4.93\text{V}$ ,  $V_{HR} = 120\text{mV}$ ,  $V_{PT} = 4.25\text{V}$ ,  $V_{CN} = 1.2\text{V}$ ,  $V_{CP} = 3.8\text{V}$ ,  $V_{OT} = 0.3\text{V}$ ,  $V_{RF} = 3.0\text{V}$ , and the DC value of  $V_{in} = 3\text{V}$ . To conserve power, we operated  $V_A$  at  $0.995\text{V}$  in the low-frequency cochlea, at  $1.05\text{V}$  in the mid-frequency cochlea, and at  $1.15\text{V}$  in the high-frequency cochlea. It is possible to reduce the power dissipation even further by having a tilt in the values of  $V_A$  in each cochlea. Through experimentation, we found that  $V_Q = -44\text{mV}$ ,  $-52\text{mV}$ , and  $-65\text{mV}$  yielded the best performance for the low-frequency, mid-frequency, and high-frequency cochleas, respectively. We could also speed up the gain adaptation in the mid-frequency and high-frequency cochleas by setting  $V_{PT}$  in the  $4.10\text{V}$  to  $4.15\text{V}$  range. We used standard shift-register and clocking circuitry to multiplex the outputs from the different cochlear taps onto a common output tap.

### 4.3.2 Offset Adaptation

Figure 4.22 shows the DC output voltage across the cochlea as we scan from tap 1 to tap 39. In the absence of any offset adaptation ( $V_{OF} = 4.76\text{V}$ ), each cochlear stage has a systematic negative offset of about  $42\text{mV}$ ; by 39 stages the DC output voltage has dropped from  $3\text{V}$  to  $1\text{V}$ . As we strengthen the offset adaptation by raising the value of  $V_{OF}$ , the offset degradation improves. At  $4.96\text{V}$ , there is little offset accumulation, and there is an almost flat DC response across the whole cochlea. Typically, we operate the cochlea at  $V_{OF} = 4.93\text{V}$  and tolerate some offset in return for reduced ringing in the offset-adaptation loop, and for a lower adaptation corner frequency.

### 4.3.3 Frequency Response

Figure 4.23(a) shows the frequency response of the cochlea at different input amplitudes ranging from  $5\text{mV}$  to  $1000\text{mV}$  rms at cochlear tap 30. The adaptation in  $Q$  with increasing input amplitude is evident. Figure 4.23(b) plots the gain versus frequency such that the curve with the highest gain corresponds to the lowest input amplitude of  $5\text{mV}$ . The gain adapts from about 30 for the  $5\text{mV}$  rms case to about 0.7 at  $1000\text{mV}$  rms. Figure 4.24 shows that the output is approximately linear in the input at frequencies before the BF,

is compressive at the BF, and is even more compressive after the BF. These compression characteristics are seen in the biological cochlea as well [12]; they arise because of the accumulated effects of gain adaptation over several cochlear stages.

Figure 4.25(a) illustrates that the harmonic distortion is greatest about one octave before the BF. This effect occurs because the second-harmonic distortion is amplified by the high gain at the BF when the input frequency is 1 octave before the BF. When the input frequency is at the BF, the second-harmonic distortion drops sharply because 1 octave after the BF there is great attenuation. These effects imply that nonlinearities in the cochlea cause masking in the perception of harmonic frequencies; that is, the threshold for the detection of a  $2f$  tone is higher in the presence of a  $1f$  tone than in the absence of one. Psychophysical experiments reveal this effect in humans as well [13].

Figure 4.25(b) illustrates the growth and filtering of harmonic distortion as the signal travels through the cochlea. The input is a 1V rms signal with frequency 162Hz that corresponds to the BF at tap 30. As the signal travels from tap 15 to tap 30, the second-harmonic distortion builds until it is at its peak value about 1 octave before tap 30 (tap 20). After tap 20, however, it is gradually filtered away because the second-harmonic frequency begins to fall in the cutoff region of the cochlear filters. By the time that the signal is at tap 30, there is only a small amount of distortion left. Thus, the sharp cochlear rolloff ensures that each tap does not suffer much distortion at its BF.

Figure 4.26 illustrates that, at the BF, the output amplitude and harmonic distortion barely change with amplitude for amplitudes beyond about 40mV or 50mV. The second harmonic is 25dB smaller than the first harmonic for a wide range of input amplitudes. The reduction in harmonic distortion is due to the accumulated effects of the action of the AGC at each cochlear stage, and to the sharp cochlear rolloff. Note that, in the corresponding harmonic-distortion plots for a single cochlear stage (Figure 4.17(b)), the second harmonic distortion at BF is only down a factor of 8 at 1V rms, and there is continued growth of all harmonics with input amplitude.

Although the CF as measured by amplitude curves (Figure 4.13(b)), shifts, the  $CF_{90}$  as measured by phase curves (Figure 4.14) does not change appreciably. These findings for a single cochlear stage are echoed in the cochlea as well: At cochlear tap 30, as Figure 4.27 shows, the phase curves have a relatively invariant CF, although the gain curves (shown in Figure 4.23(b)) shift with amplitude. The kinks and rising parts of the phase curves of

Figure 4.27 are due to parasitic capacitances in the cochlear filters.

#### 4.3.4 Noise, Dynamic Range, and SNR

Figure 4.20 illustrates that the noise at the output of a cochlear tap has contributions from the input-referred noise of each cochlear filter preceding that tap. To evaluate the total noise at the output we need to evaluate the noise per unit bandwidth of each of these sources, to evaluate the transfer function from each source to the output, to accumulate the contributions from the various sources, and then to integrate over all frequencies.

If there are  $N_{oct}$  filters per octave, then the frequency ratio  $r$  between the  $\tau$  of any filter and the  $\tau$  of the filter just to the right of that one is given by

$$r = 2^{-1/N_{oct}}, \quad (4.46)$$

$$= e^{-1/(N_{oct}/\ln(2))}, \quad (4.47)$$

$$= e^{-1/N_{nat}}. \quad (4.48)$$

Thus if  $x = \omega\tau$  is the normalized frequency corresponding to the output tap of interest, then the filtering effects of the filters preceding the output filter are represented by  $H(x)$ ,  $H(rx)$ ,  $H(r^2x)$ ,...as shown in Figure 4.20. Similarly, if  $I$  were the bias current at the output cochlear tap (corresponding to  $\sqrt{I_1 I_2}$  at each tap), the bias current of the  $k_{th}$  preceding filter would be given by  $I/r^k$ .

From Eqs. (4.12) and (4.17), the normalized input-referred noise per unit bandwidth is given by

$$v_0^2(x)dx = \left( \frac{NqV_L}{2\pi QC} \right) \left( \sqrt{C_R} + \frac{x^2}{\sqrt{C_R}} \right) dx. \quad (4.49)$$

It is then easy to show that the input-referred noise per unit bandwidth for the  $k_{th}$  filter preceding the output tap is given by

$$v_k^2(x)dx = \left( \frac{NqV_L r^k}{2\pi QC} \right) \left( \sqrt{C_R} + \frac{x^2 r^{2k}}{\sqrt{C_R}} \right) dx, \quad (4.50)$$

since  $x \rightarrow r^k x$  and  $I \rightarrow I/r^k$ . If there are  $M$  preceding taps, then the total output noise per unit bandwidth  $v_{out}^2(x)dx$  is given by

$$\frac{NqV_L}{2\pi QC} \sum_0^M r^n \left( \sqrt{C_R} + \frac{x^2 r^{2n}}{\sqrt{C_R}} \right) \prod_0^n |H(r^k x)|^2 dx. \quad (4.51)$$

We obtain the total output noise at the cochlear tap of interest by integrating Eq. (4.51) over all  $x$  from 0 to  $\infty$ . Although the expression for the output noise at a cochlear tap can be written down, it is hard to solve in closed form. But it can be measured easily with a SR780 Spectrum Analyzer. Figure 4.28 shows what the noise spectrum of a cochlear tap looks like at tap 31 of our cochlea. It has a form predicted by Eq. (4.51) except for the second and third harmonic peaks; these peaks are due to nonlinearities in the filters.

Figure 4.29 illustrates that the dynamic range at the output of tap 30 of our cochlea is greater than 60 dB at the BF of that tap (162Hz): Figure 4.29(a) shows the noise spectrum of the background noise at tap 30 which yields a total integrated noise of 50mV rms. When a BF sinusoidal signal (162Hz) of 0.907mV rms magnitude is applied to the input of the cochlea, it is amplified up by a factor of 57.1 to 51.8mV. Thus, the rms power of the signal and noise at tap 30 is about 72mV rms ( $\sqrt{(51.8^2 + 50^2)}$ ). Now, at an output SNR ratio of 1, we would expect the signal and noise to have an rms power of  $50\sqrt{2} = 70.7$ mV rms. The fact that the rms power is 72mV means that our minimum detectable signal, which corresponds to an output SNR of 1, is actually below 0.907mV. In fact, since the system is linear at small input amplitudes, the minimum detectable signal is  $50\text{mV}/57.1 = 0.875$ mV. Figure 4.29(b) shows that the harmonic distortion at a 1V rms input is about  $\sqrt{(11.85^2 + 2.82^2 + 1.11^2 + 0.245^2)}/315.8 = 3.87\%$ . This value is less than 4% which is commonly used as a measure of the upper limit of dynamic range of measuring-amplifier systems. Thus, at BF, we can process input signals over a ratio of  $1000/0.875 = 1143$  in amplitude, or  $1.306 \times 10^6$  in intensity. This range of intensity corresponds to a dynamic range of  $10\log_{10}(1.306 \times 10^6) = 61.1$ dB.

At large signals, the SNR at BF improves for two reasons: The signal amplitude gets larger—though not in a linear fashion, because of the AGC—and the noise amplitude drops, because of the lowering of  $Q$ . Figure 4.30(a) illustrates this effect for a 1V input and for a 0.9mV input. Figure 4.30(b) shows a plot of the signal amplitude and the noise amplitude for various input levels. The signal amplitude was evaluated as the square root of the power at the BF in spectral plots like those in Figure 4.30(a); the power at the harmonic peaks was ignored, although the power at these peaks also is due to the signal. We evaluated

the noise power by integrating the power over all frequencies in the noise spectrum. The noise spectrum was obtained by removing all signal and harmonic peaks in the spectrum. We interpolated the noise spectrum in the regions where we removed the peaks. The noise amplitude was the square root of the noise power.

Figure 4.31 shows a plot of the SNR (signal power/noise power) as a function of input amplitude. As the input rms amplitude changes by a factor of about 61dB in intensity (0.9mV to 1V rms), the SNR changes by a factor of about 31dB (1 to 1241).

Figure 4.32 shows how our AGC cochlea extends the dynamic range of a hypothetical linear low- $Q$  cochlea. The linear low- $Q$  cochlea can be viewed as being representative of just the passive basilar membrane, with no outer hair cells [4]. Thus, we call our AGC cochlea with amplification (high- $Q$ ) an *active cochlea*, and the linear low- $Q$  cochlea a *passive cochlea*. Some silicon cochleas have been built with a passive cochlea acting as a front end to a bank of bandpass filters [5].

Suppose that the passive cochlea has the same gain, and the same low  $Q$ , as the active cochlea at the largest input levels of 1V rms. Both cochleas will then have the same low- $Q$  noise floor of 8.96mV at 1V. Since the passive cochlea maintains the same 0.315 gain at all intensities, its minimum detectable signal is given by  $8.96\text{mV}/0.315 = 28.4\text{mV}$ . The active cochlea has a high  $Q$  at small input levels such that it amplifies the input signal and the noise. At BF, however, it amplifies the signal significantly more than the noise. In fact, its minimum detectable signal occurs when a 0.82mV input at BF has been amplified up by a factor of 59 to be just above the noise floor, which has now increased to  $48.4\text{mV}$ .<sup>2</sup> Thus, the active cochlea extends the dynamic range of the passive cochlea by having the minimum detectable signal decrease by  $20\log_{10}(28.4/0.82)$  dB = 31dB! It is known that outer hair cells in the biological cochlea extend the lower end of our dynamic range of hearing by about 40dB.

Figure 4.33(a) shows the noise spectra of various taps from tap 1 to tap 37. The corner frequency of the noise spectra successively decrease from tap 1 to tap 37, while the noise per unit bandwidth successively increases. The peak height increases and converges to an asymptotic limit as we traverse the cochlea. Note that, because of offsets in the cochlea,

<sup>2</sup>These numbers (gain of 59, noise of 48.4mV, and minimum detectable signal of 0.82mV) are slightly different from the numbers that we quoted earlier (gain of 57.1, noise of 50mV, and minimum detectable signal of 0.875mV) because of the interpolation procedures used in our data processing algorithm, and because of the different times at which the data were collected.

there is an abrupt reduction in corner frequency between taps 21 and 25. This abrupt reduction in bandwidth lowers the noise below the theoretical value that we would expect for taps close to and beyond this region. The total integrated noise over all frequencies is shown in Figure 4.33(b). The noise increases due to accumulation and amplification as we traverse the filters of the cochlea. However, the successive lowpass filtering limits this growth, until, in the asymptotic limit, there is an equilibrium between noise accumulation and noise filtering, and the noise ceases to grow. The discontinuities in the curve around tap 21 to tap 25 are due to the abrupt reductions in bandwidth around this region. The eventual convergence of the noise is due to the exponential taper of the cochlea: The exponential taper results in an accumulation of noise terms with coefficients that are determined by the terms of a geometric series with geometric ratio  $r$  (Eq. (4.51)). Since  $r < 1$ , the geometric series converges. Note that, as we increase the number of filters per octave, by Eq. (4.46), we increase  $r$ , and the noise increases. There is thus a tradeoff between the sharpness of the rolloff slope of the cochlea, which increases with  $N_{oct}$ , and noise reduction. The noise is also extremely sensitive to the value of  $Q$  because of the sensitive dependence of the  $H(r^k x)$  terms of Eq. (4.51) on  $Q$ . We used  $Q = 1.5$ , and  $N_{oct} = 11.2$  as a good compromise between not having too much noise at the output of the cochlear taps, and not having broad filters with shallow rolloff slopes.

Figure 4.34(a) shows the minimum detectable signal and maximum undistorted input at the BF of each tap in the cochlea. The minimum detectable signal was measured as described earlier in this section. The maximum undistorted input was measured by finding the input rms value at which the second harmonic (by far the dominant harmonic) was attenuated by 25 dB when compared with the first harmonic. We observe that the maximum undistorted input is nearly constant at 1V rms, except for the first few taps, where the action of the strong AGCs at each tap have not accumulated sufficiently to reduce the distortion.<sup>3</sup> Figure 4.34(b) shows the dynamic range at various taps. The dynamic range varies from about 59dB to 64dB. The early taps have little accumulation of noise or gain, in contrast with the late taps, which have large accumulation of noise and gain. The effect of gain regulation in the AGC causes the accumulation of noise and of gain to be approximately

---

<sup>3</sup>We were able even to apply a 1.4V input rms signal and to keep the distortion under 25 dB (due to the strong AGC), but we refrained from doing so because the input signal then would be just at the edge of our DC operating range; operating the cochlea at this extreme is possible, but we chose not to so as to leave a safety margin.

in balance, so the dynamic range does not suffer a huge variation across taps. However, as we would expect, Figure 4.35 shows that the maximum output SNR at BF (the SNR at 1V rms input) falls as we traverse the cochlea. It is maximum at tap1 ( $6.74 \times 10^4$  or 48.3dB) where there is the least noise, and minimum at tap 37 where there is the most noise (649 or 28.1dB). The discontinuities, due to the CF offset of the cochlea around taps 21 to 25, are evident in Figure 4.34 and Figure 4.35.

### 4.3.5 Spatial Characteristics

Figure 4.36(a) shows the spatial response of various taps of the cochlea to a 162Hz input, for various amplitudes. To understand the similarity of Figure 4.36(a) to Figure 4.23(a), we can view the cochlea as performing a frequency-to-place transformation with  $\log(f) \rightarrow x$  [4]. Even the harmonic-distortion plot of Figure 4.36(b) is quite similar to that of Figure 4.25(a). The most severe distortion occurs at a place that corresponds to a corner frequency that is 1 octave higher than the corner frequency at the best place (BP). Figure 4.37 shows the shift in BP for two different frequency inputs to the cochlea.

### 4.3.6 Dynamics of Gain and Offset Adaptation

Figure 4.38(a) shows the attack response of cochlear tap 30 to the abrupt onset of a tone at the tap's BF (162Hz). After a transient at the first cycle, the envelope of the response adapts quickly to the new intensity, corresponding to the quick onset adaptation of the peak detector. The offset correction has a slower rate of adaptation and continues to adapt with some ringing even after the envelope adaptation is complete.

Figure 4.38(b) shows the release response of cochlear tap 30 to an abrupt decrease in the intensity of the BF tone. The adaptation of the envelope is much slower than that shown in Figure 4.38(a) because of the slow adaptation of the peak detector to inputs of decreasing intensity. The DC offset adaptation continues to have a rate of adaptation that is slower than the rate of envelope adaptation.

### 4.3.7 The Mid-Frequency and High-Frequency Cochleas

So far, we have dwelled almost entirely on the properties of the low-frequency cochlea; the properties of the other cochleas are similar. Figure 4.39 shows the variation in  $Q$  versus



corner frequency due to bias-current differences in a cochlear filter. There is a variation in  $Q$  as we go from subthreshold behavior at low frequencies to above-threshold behavior at high frequencies. However, our high-frequency circuits operate just at the beginning of the transition from subthreshold to above threshold, and thus the change in  $Q$  is not significant. Figure 4.40 shows that, consequently the “sounds of silence”, that is, the noise spectra at the various taps in the low, mid, and high-frequency cochleas are similar in shape across the entire frequency range (100Hz to 10kHz).

## 4.4 Analog Versus Digital

The total resting current consumption of all three of our cochlear cascades was measured to be  $95\mu\text{A}$ . Playing microphone speech through our cochleas increased the power consumption to about  $99\mu\text{A}$ . Thus, the total power consumption of our cochlea is about  $100\mu\text{A} \times 5\text{V} = 0.5\text{mW}$ . Our area consumption was  $1.6\text{mm} \times 1.6\text{mm} \times 3 = 7.7\text{mm}^2$  in a  $1.2\mu\text{m}$  process. The pitch of a single cochlear stage, including all scanning circuitry and with a conservatively large number of power buses (to prevent unwanted coupling through the supplies), was  $102\mu\text{m} \times 444\mu\text{m}$ .

The high-frequency cochlea consumes more than 3/4 of this power. We can easily cut our power dissipation to 0.2mW by having a tilt on the  $V_A$  voltages, although we did not implement this tilt on our current design. If only telephone bandwidth is required, we can do away with the high-frequency cochlea and cut our power dissipation to 0.125mW. If we implement the tilt on the  $V_A$  voltages and do not use the high-frequency cochlea, then our power consumption reduces to  $50\mu\text{W}$ .

We next compare the power and area consumption of our analog cochlea, an ASIC digital cochlea, and a noncustom microprocessor ( $\mu\text{P}$ ) cochlea. We begin by describing the design of the ASIC digital cochlea.

### 4.4.1 The ASIC Digital Cochlea

Figure 4.41 shows a block-level schematic of a digital cochlea, similar to our analog cochlea, and described in [14]. Second-order recursive digital filters with tapering filter coefficients model the basilar membrane. Half-wave rectification circuits (HWR) perform MSB lookup to model the inner hair cells. Automatic-gain-control circuits (AGC) with cross talk model

the olivocochlear efferent system. The multiscale AGC is modeled over 4 time scales.

This is a custom cochlea, designed to be as efficient in power and area consumption as possible. A digital input, clocked at 50 KHz, forms the input to the cochlea; that frequency is slightly over the Nyquist frequency of 36kHz for the highest-frequency location of the cochlea, and is necessary to obtain robust behavior with the filtering and nonlinear operations in the cochlea. It is possible to implement a multirate sampling system, but calculations show that the bandwidth needed to implement 95 stages of the cochlea from 18KHz to 100Hz (as in the analog cochlea) is equivalent to the bandwidth needed to implement 17 stages at 18kHz. Thus, a multirate system can help only by a factor of 5.6. If the overhead in circuitry and complexity needed for a multirate system is factored in, there may be no advantage whatsoever. Thus, we shall confine ourselves to a system with only one rate of sampling. Note that we need only 95 stages in the digital cochlea (as opposed to 117 stages), since we do not need the redundancy of the overlapping-cascades architecture. To handle the input dynamic range of 60dB, (i.e., 10 bits), it is necessary to do fixed-point operations at a precision of approximately 24 bits; otherwise, overflow errors and round-off-error accumulation can seriously jeopardize the computation.

The system shown in Figure 4.41 is implemented most efficiently with a bit-serial representation, where the bits are processed serially, and each filter, HWR, and AGC block is reused 95 times to compute the effect of the entire cascade. The reuse of circuitry results in tremendous savings in area and power, and makes a digital cochlear implementation feasible on a single chip. There is, of course, overhead in the storage that is necessary to implement these computations.

The proposed ASIC digital cochlea was never built. However, we can estimate what its power dissipation would have been. The Clock Rate is  $50 \text{ kHz} \times 95 \text{ stages} \times 24 \text{ bits} = 114.0 \text{ Mhz}$ . The power supply would need to be about 2.0 V to attain a 114.0MHz clock rate. Let's assume that the technology is  $0.5 \mu\text{m}$ . The number of gates needed for the computation is roughly  $40$  (number of gates for 1 multiply operation, including storage overhead)  $\times 24$  (number of bits)  $\times 7$  (3 multiplies in filter and 4 in the AGC) = 6720 gates + RAM and ROM. The 13 add operations comprising 5 adds in the filters and  $4 \times 2$  adds in the AGC are treated as being essentially free in fixed-point computations. The  $\text{gate.Hz} = 6720 \times 114 \text{ Mhz} = 0.77 \times 10^{12} \text{ gate Hz}$ . The gate capacitance =  $(0.5 \mu\text{m} \times 0.5 \mu\text{m} \times 10$  (transistors per gate)  $\times 2 \text{ fF}$  (cap. per unit area) = 50 fF. The switching energy per gate

Table 4.1: Cochleas

	ANALOG	ASIC DIGITAL	DEC $\alpha$
TECH.	1.2 $\mu$ m	0.5 $\mu$ m	0.5 $\mu$ m
$V_{DD}$	5V	2V	3.3V
POWER	0.5mW	150mW	50W
AREA	7.7mm <sup>2</sup>	25 mm <sup>2</sup>	299 mm <sup>2</sup>

= 50 fF x (2.0)<sup>2</sup> =  $2.0 \times 10^{-13}$ J. The power dissipation is therefore  $0.77 \times 10^{12}$  gate.Hz  $\times$   $2.0 \times 10^{-13}$  = 0.154W, which we shall round down to **0.15W**. The area we would need to build this chip is estimated to be 5 mm  $\times$  5 mm (in 0.5  $\mu$ m tech.) = **25 mm<sup>2</sup>**.

#### 4.4.2 $\mu$ P Cochlea

In FLOPS, we need about 50 KHz (bandwidth)  $\times$  95 (number of stages)  $\times$  20 (7 multiplies and 13 adds) = 95 MFLOPs to implement our cochlea. Note that adds cannot be treated as free in floating-point operations. On the specP92 Ear program, the DEC 21164 running on an Alpha server 8200 5/300 does about 1275 times better than a Vax 11/780. The Vax 11/780 is specified at 0.1 MFLOPS. Thus, the DEC  $\alpha$  is capable of  $1275 \times 0.1 = 127.5$  MFLOPS which is enough for our computation, The DEC  $\alpha$  consumes **50 W** and has an area of 16.5 mm  $\times$  18.1 mm = **299 mm<sup>2</sup>**.

#### 4.4.3 Comparison of Analog and Digital Cochleas

Table 4.4.3 compares the power and area consumption of the various cochleas. Note that our analog cochlea would be more efficient in area by about a factor of 2 to 4 if it were also implemented in a 0.5 $\mu$ m technology like the digital designs. However, we have not scaled down the analog numbers; we have just shown them for our current 1.2 $\mu$ m technology.

The analog implementations are more efficient in power than are custom digital implementations by a factor of 300, and than are noncustom  $\mu$ P implementations by a factor of  $1 \times 10^5$ . The analog cochlea can run on 1Ah batteries for more than a year (with 100 $\mu$ A current consumption), whereas the best digital cochlea would be able to run for only less than 1 day (with 75mA current consumption).

The area comparisons show that, even in an inferior technology (1.2  $\mu$ m vs. 0.5  $\mu$ m), the analog cochlea is about 3 times more efficient than is the custom ASIC cochlea, and is about 40 times more efficient than is the microprocessor implementation.

The cochlear comparisons were generous to digital implementations: We used a better technology (0.5  $\mu\text{m}$  versus 1.2  $\mu\text{m}$ ), operated with a power-saving supply voltage (2.0 V versus 5.0 V), used an efficient bit-serial implementation, did not include the cost of the 10-bit or 13-bit A/D converter, and were more conservative in our cost estimates. Nevertheless, the analog implementations were two to five orders of magnitude more efficient than the digital implementations. To compete with digital systems, the analog systems had to be designed with wide-dynamic-range circuitry, and had to compensate for their offsets. In fact, most of the analog cochlea's resources in area were expended in filter linearization, low-noise transduction, and offset-compensation circuitry. Most of the analog cochlea's resources in power were expended in low-noise sensing circuitry. The number of devices needed to do the actual computation was nevertheless so small that 117 stages could be implemented easily on one chip, with room to spare.

By contrast, the digital cochlea's resources in area and power were not primarily consumed in maintaining precision, although extra bits were necessary to prevent overflow and roundoff errors. Rather, the actual computation was so expensive in digital that only one stage of the cochlear cascade was feasible on a single chip. That stage had to be reused 95 times in succession, at a fast rate of 114MHz, to finish the computation in real time. In other words, the analog implementation was slow per computational stage, cheap, and completely parallel. The digital implementation was fast per computational stage, expensive, and fully serial. We might wonder—if the digital implementation were slow and fully parallel just like the analog one, would the comparisons in efficiency seem less drastic? The answer is yes for power consumption because it could be reduced by turning down the power-supply voltage and clock frequency. The answer is no for area consumption, because it would be 95 times worse. In this particular case, however, the size of the chip required for the parallel digital implementation would be totally unfeasible. In other words, there is no free lunch: the inefficiency of using a transistor as a switch will always show up somewhere.

## 4.5 The Biological Cochlea

The biological cochlea is far more complex than is our electronic cochlea, and it is surprising that we can replicate much of its functionality with just our simple circuits. Our aim is not to replicate its functions exactly, as computer modeling attempts to do, but rather

to exploit its clever computational ideas to build more efficient electronic architectures for artificial hearing. Such architectures may enable the design of superior hearing aids, cochlear implants, or speech-recognition front ends. In addition, as we shall show in Section 4.5.1, the synthesis of an artificial cochlea can help us to improve our understanding of how the biological cochlea works.

The functions of the biological cochlea that we can replicate are:

1. The frequency-to-place transformation, as implemented by the amplification and propagation of traveling waves
2. A compressive nonlinearity at and beyond the BF of a cochlear tap. Like the biological cochlea, our response is linear for frequencies well below the BF. Our compression is achieved through an AGC. In the biological cochlea, it is still a matter of debate as to how much of the compression arises from a dynamic AGC and how much from a static nonlinearity. We have reported on cochleas where the compression arises solely from a static nonlinearity as well [9].
3. An asymmetric attack and release response to transient inputs.
4. The extension of dynamic range due to active amplification. Our dynamic range is extended from 30dB to about 60dB. In the biological cochlea, it is believed that amplification by outer hair cells extends the dynamic range of the cochlea by about 40dB.
5. The broadening of the pattern of excitation as the input intensity is increased. The dual effect, which we can also model, is the broadening of the frequency-response curves as the input intensity is increased.
6. The shift of the peak frequency towards lower frequencies as the input intensity is increased. The dual effect, which we can also model, is the shift of the peak place of excitation toward the input of the cochlea as the intensity is increased.
7. A sharp cochlear roll-off slope.
8. Masking of adjacent frequencies and harmonics due to the effects of the AGC and nonlinearity, respectively. However, our dominant harmonic is the second harmonic. In the biological cochlea, the dominant harmonic is the third harmonic.

### 4.5.1 Traveling-Wave Architectures Versus Bandpass Filters

Why did nature choose a traveling-wave architecture that is well modeled by a filter cascade instead of a bank of bandpass filters? We suggest that nature chose wisely, for the following three reasons:

1. To adapt to input intensities over a 120dB dynamic range, a filter bank would require a tremendous change in the  $Q$  of each filter. To compress 120dB in input intensity to about 40dB in output intensity the filter  $Q$ s must change by 80dB; a dynamic-range problem in the input is merely transformed into a dynamic-range problem in a parameter. In contrast, in a filter cascade, due to the exponential nature of gain accumulation, enormous changes in the overall gain for an input can be accomplished by small distributed changes in the  $Q$  of several filters.
2. Large changes in the  $Q$  of a filter are accompanied by large changes in the filter's window of temporal integration. Thus, in filter banks, faint inputs would be sensed with poor temporal resolution, and loud inputs would be sensed with good temporal resolution. In contrast, in a filter cascade, the shifts in temporal resolution with intensity change only in a logarithmic fashion with intensity, as opposed to in a linear fashion as in the filter bank.
3. A sharp rolloff slope in a filter is extremely useful in limiting distortion, and in enhancing spectral contrasts. A sharp rolloff slope arises naturally in the cochlear filter cascade. To accomplish such a rolloff slope in a filter bank requires very high-order filters, and consequently an enormous amount of circuitry at each tap. In contrast, in the filter cascade, the burden of creating a high-order rolloff is shared collectively, so only one new filter needs to be added for each new desired corner frequency.

There are two problems that need to be addressed in a filter cascade:

1. A filter cascade is prone to noise accumulation and amplification. The solution to this problem is either to have an exponential taper in the filter time constants such that the output noise converges (the solution found at high CFs in the biological cochlea), or to limit the length of the cascade (the solution at low CFs in the biological cochlea). The exponential taper also results in elegant scale-invariant properties.

2. The overall gain is quite sensitive to the value of each filter's  $Q$ . The solution to this problem is to have gain control regulate the value of the  $Q$ 's in the cascade. If the gain control is sufficiently strong, then the collective adaptation in  $Q$  across many filters will compress a wide input dynamic range into a narrow output dynamic range.

## 4.6 Applications to Cochlear Implants

Front-end modules in current cochlear implant devices make use of parallel banks of independent bandpass filters. For example, the front-end module of a state-of-the-art commercial multichannel cochlear implant devices consists of 20 fourth-order bandpass filters with center frequencies between 250Hz and 10kHz. The filters are implemented using switched-capacitor techniques. The total power dissipation of such implementations is on the order of several milliwatts, and the dynamic range is only 35 to 40 dB.

Our neuromorphic approach mimics several aspects of the biological cochlea, as described in Section 4.5. In addition, our dynamic range exceeds 60dB. Our power dissipation for a 117-stage cochlea with a roll-off slope corresponding to a high-order filter (10th order to 16th order) is 0.5mW. If we use fewer stages and fewer filters per octave to correspond to current values in implant front ends, we could, we estimate, cut our power dissipation to 50  $\mu$ W. This power dissipation is about 20–100 times lower than that in current front ends.

Thus, in terms of biological realism, dynamic range, and power we can do much better than current implant front ends. Previously [11], we described how a nonlinear center-surround operation on the outputs of the cochlear taps can convert cochlear lowpass information into bandpass information without degrading the temporal resolution at that tap. A neuromorphic front-end module like ours satisfies the fundamental requirements of future cochlear-implant speech processors [15].

## 4.7 Conclusions

We described a 117-stage 100Hz-to-10kHz cochlea that attained a dynamic range of 61dB while dissipating 0.5mW of power. The wide dynamic range was attained through the use of a wide-linear-range transconductance amplifier, of a low-noise filter topology, of dynamic gain control (AGC), and of an overlapping-cascades architecture. An infrastructure

of automatic offset adaptation, small amounts of low-frequency attenuation, and scale-invariant BiCMOS circuit techniques provided robust operation. The low power, wide dynamic range, and biological realism suit our cochlea to be used as a front end for cochlear implants. The design of our electronic cochlea suggests why nature preferred an active traveling-wave mechanism over a bank of bandpass filters as a front end for hearing.



## Bibliography

- [1] R. Sarpeshkar, T. Delbrück, and C. Mead, “White Noise in MOS Transistors and Resistors”, *IEEE Circuits and Devices*, Vol. 9, No. 6, pp. 23–29, Nov. 1993; contained in chapter 2 of this thesis.
- [2] B. M. Johnstone, “Genesis of the Cochlear Endolymphatic Potential”, *Current Topics in Bioenergetics*, Vol. 2, pp. 335–352, 1967.
- [3] B. C. J. Moore, *An Introduction to the Psychology of Hearing*, Third Edition, pp. 47–83, Academic Press Limited, London, 1989.
- [4] C.A. Mead, *Analog VLSI and Neural Systems*, pp. 179–192, 279–302, Addison-Wesley Publishing Co., Reading, MA, 1989.
- [5] W. Liu, *An Analog Cochlear Model: Signal Representation and VLSI Realization*, PhD. Thesis, John Hopkins University, Baltimore, Maryland, 1992.
- [6] L. Watts, D. A. Kerns, R. F. Lyon, and C.A. Mead, “Improved Implementation of the silicon cochlea”, *IEEE Journal of Solid-State Circuits*, 27(5), pp. 692–700, May 1992.
- [7] N. Bhadambkar, “A variable resolution nonlinear silicon cochlea”, Technical Report CSL-TR-93-558, Stanford University, 1993.
- [8] A. van Schaik, E. Fragniere, and E. Vittoz, “Improved Silicon Cochlea using Compatible Lateral Bipolar Transistors”, *Advances in Neural Information Processing Systems 8*, pp. 671–677, edited by D. Touretzky, et al., MIT Press, Cambridge, MA 1996.
- [9] R. Sarpeshkar, R. F. Lyon, and C. A. Mead, “An Analog VLSI Cochlea with New Transconductance Amplifiers and Nonlinear Gain Control”, *Proceedings of the IEEE Symposium on Circuits and Systems*, Atlanta, Vol. 3, pp. 292–295, May 1996.

- [10] R. Sarpeshkar, R. F. Lyon, and C. A. Mead, "A low-power wide-linear-range transconductance amplifier", to appear in *Analog Integrated Circuits and Signal Processing*, special issue on neuromorphic engineering, expected publication date 1997; contained in chapter 3 of this thesis.
- [11] R. J. W. Wang, R. Sarpeshkar, M. Jabri, and C. Mead, "A Low-Power Analog Front-end Module for Cochlear Implants", presented at the XVI World Congress on Otorhinolaryngology, Sydney March 1997.
- [12] M. A. Ruggero, "Response to Sound of the Basilar Membrane of the Mammalian Cochlea", *Current Opinion in Neurobiology*, Vol. 2, pp. 449–456, 1992.
- [13] T. D. Clack, J. Erdreich, and R. W. Knighton, "Aural Harmonics: The Monoaural Phase Effects at 1500Hz, 2000Hz, and 2500Hz Observed in Tone-on-Tone Masking When  $f_1 = 1000\text{Hz}$ ", *Journal of the Acoustical Society of America*, Vol. 52, Number 2 (Part 2), pp. 536–541, 1972.
- [14] C. D. Summerfield and R.F. Lyon, "ASIC Implementation of the Lyon Cochlea Model", *Proc. IEEE International Conference on Acoustics, Speech, and Signal Processing*, San Fransisco, March 1992.
- [15] G. Clark, "Cochlear Implants: Future Research Directions", *Annals of Otology, Rhinology, and Laryngology*, Vol. 104, No. 9, Part 2, pp. 22–27, 1995.

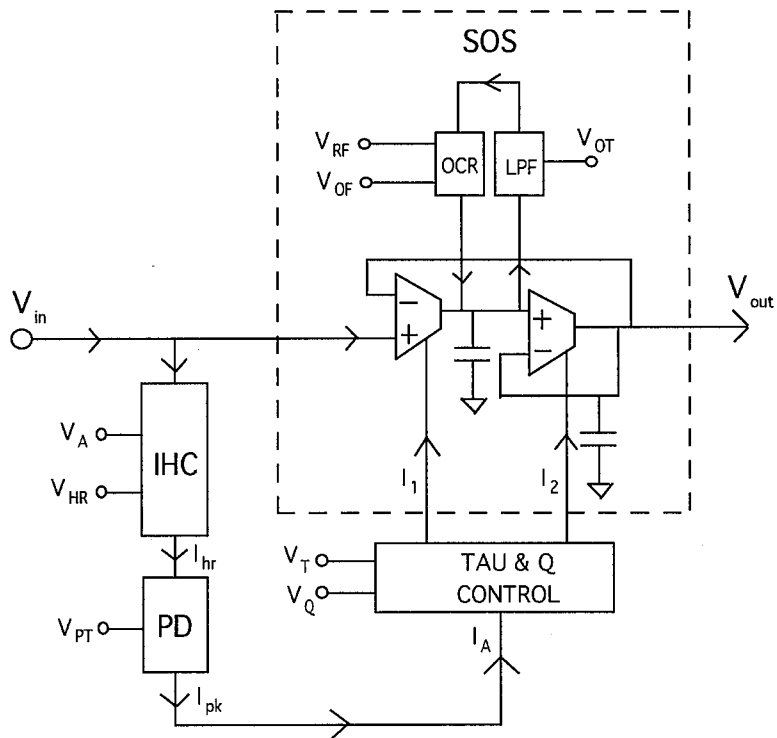


Figure 4.1: Schematic for a Cochlear Stage. A single cochlear stage is composed of a filter (SOS) with offset-adaptation circuitry (LPF and OCR), an inner-hair-cell and peak-detector circuit (IHC and PD), and a tau-and- $Q$  control circuit.

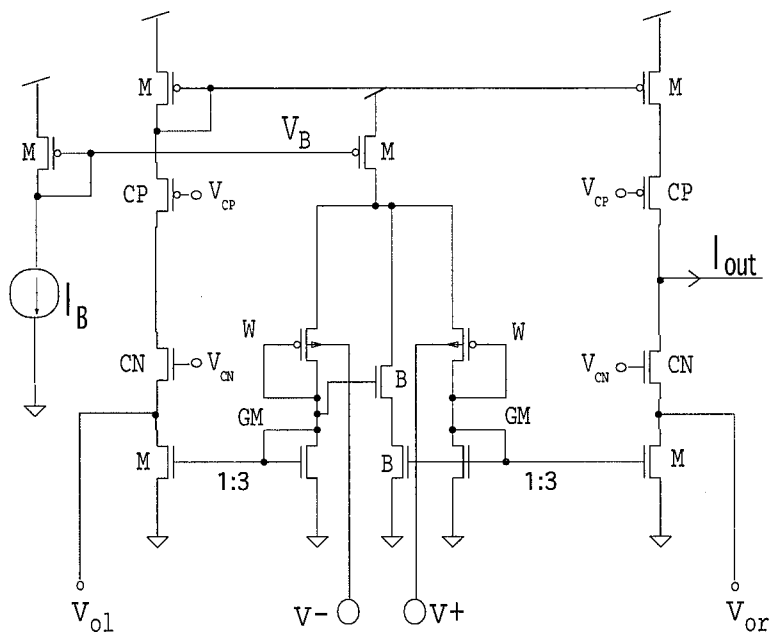


Figure 4.2: The Wide-Linear-Range Transconductance Amplifier. The inputs to the amplifier are  $v_+$  and  $v_-$ , and the output is the current  $I_{out}$ . The bias current is  $I_B$ . The voltages  $v_{ol}$  and  $v_{or}$  represent inputs from the offset-adaptation circuitry.

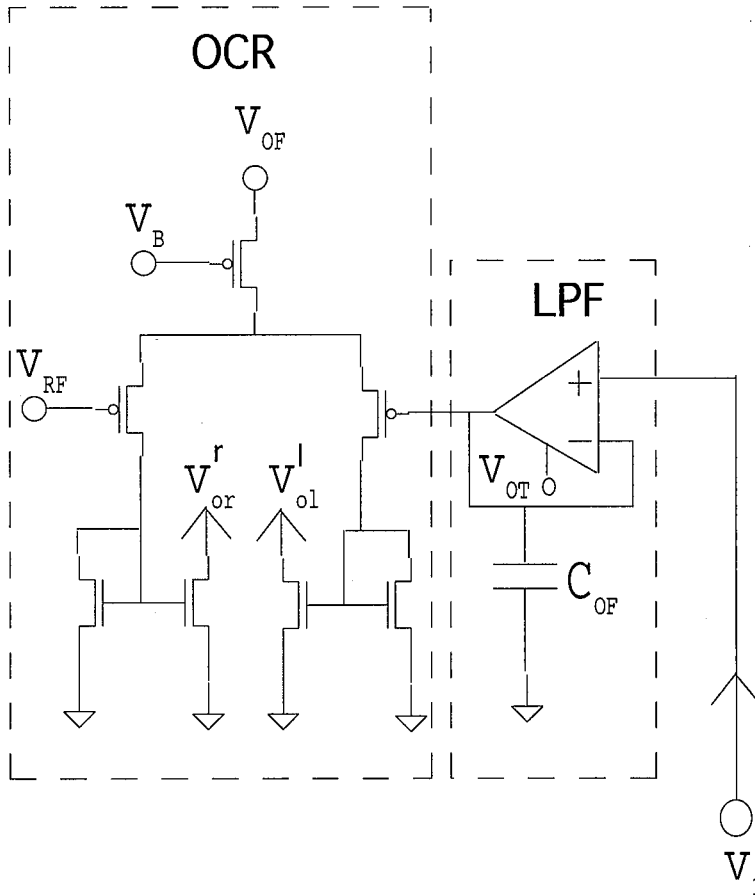


Figure 4.3: The Offset-Adaptation Circuit. The input to the circuit is the output of the first amplifier of the SOS,  $V_1$ . The outputs  $v_{ol}^1$  and  $v_{or}^1$  connect to the corresponding inputs of the first amplifier of the SOS.

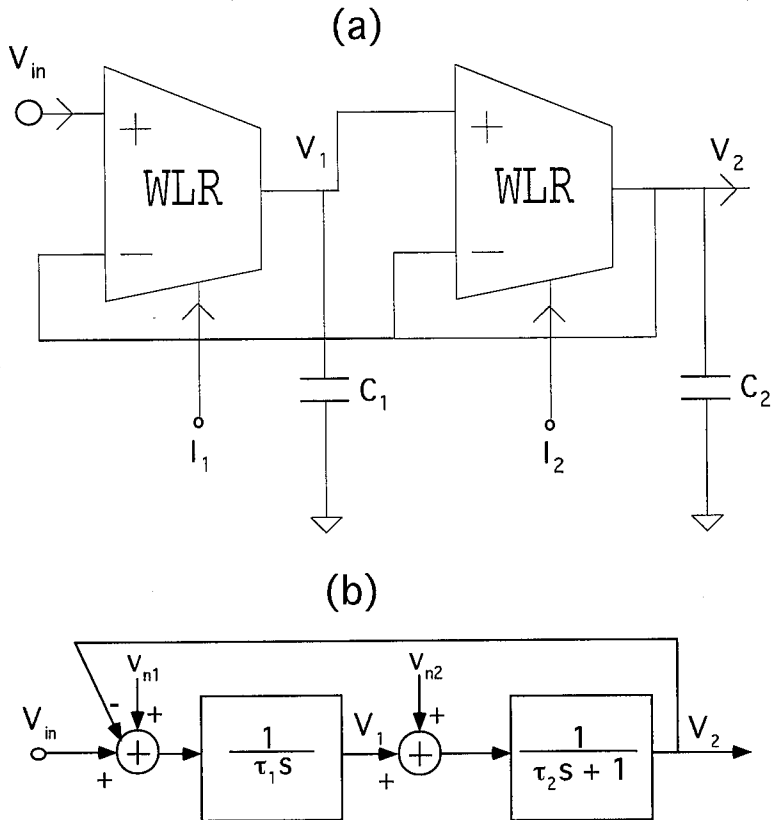


Figure 4.4: The Second-Order Filter Circuit. (a) The input is  $V_{in}$ , the output is  $V_2$ , and the bias currents of the first and second amplifiers are  $I_1$  and  $I_2$ . (b) The block-diagram equivalent of the filter is useful for making noise calculations. The voltages  $v_{n1}$  and  $v_{n2}$  represent the input-referred noise sources of the first and second amplifier respectively.

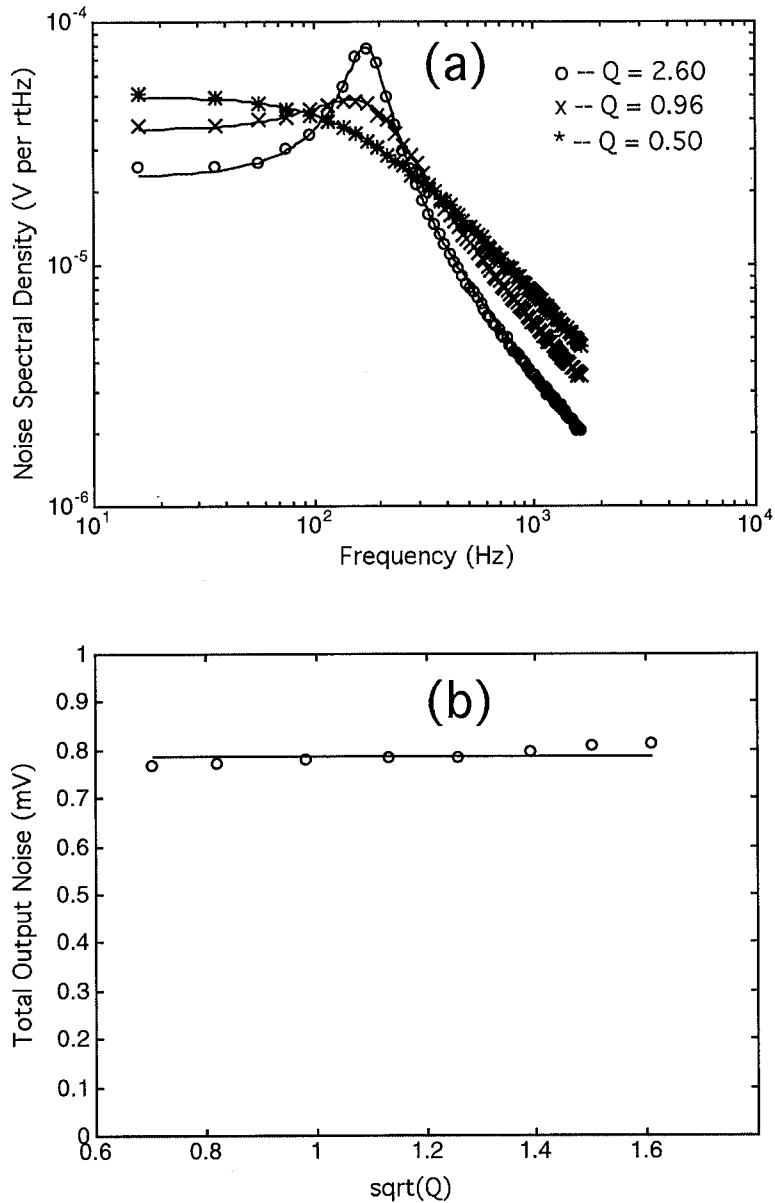


Figure 4.5: Noise in the Second-Order Filter Circuit. (a) The noise spectrum changes shape as the  $Q$  of the filter is changed. (b) The total output noise integrated over all frequencies is approximately invariant with  $Q$  for this filter.

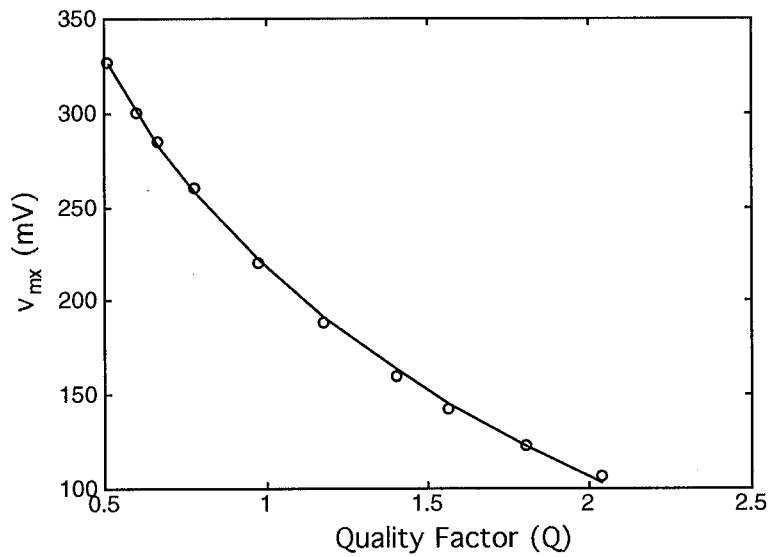


Figure 4.6: Maximum Undistorted Signal in the Filter. The input amplitude at which the total harmonic distortion at the output is attenuated by 25dB with respect to the fundamental is plotted versus  $Q$ . The fundamental frequency is at the BF of the filter. The line is an empirical fit.



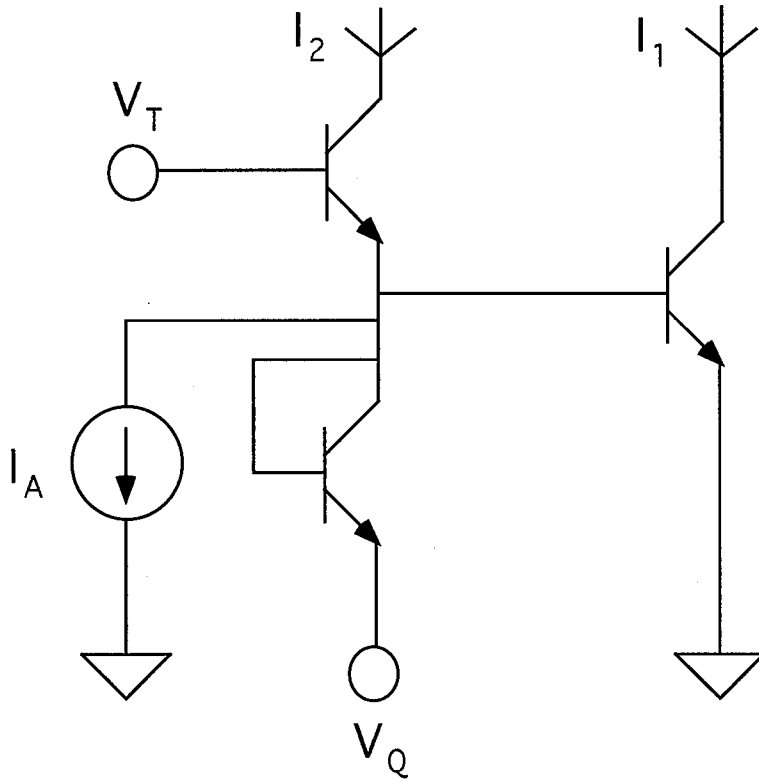


Figure 4.7: Translinear tau-and- $Q$  Biasing Circuit. The voltage  $V_T$  sets the  $\tau$  of the filter, and the voltage  $V_Q$  sets the small-signal  $Q$ . The current  $I_A$  is a placeholder for a gain-control-correction current. The currents  $I_1$  and  $I_2$  are the bias currents of the first and second amplifiers of the filter.

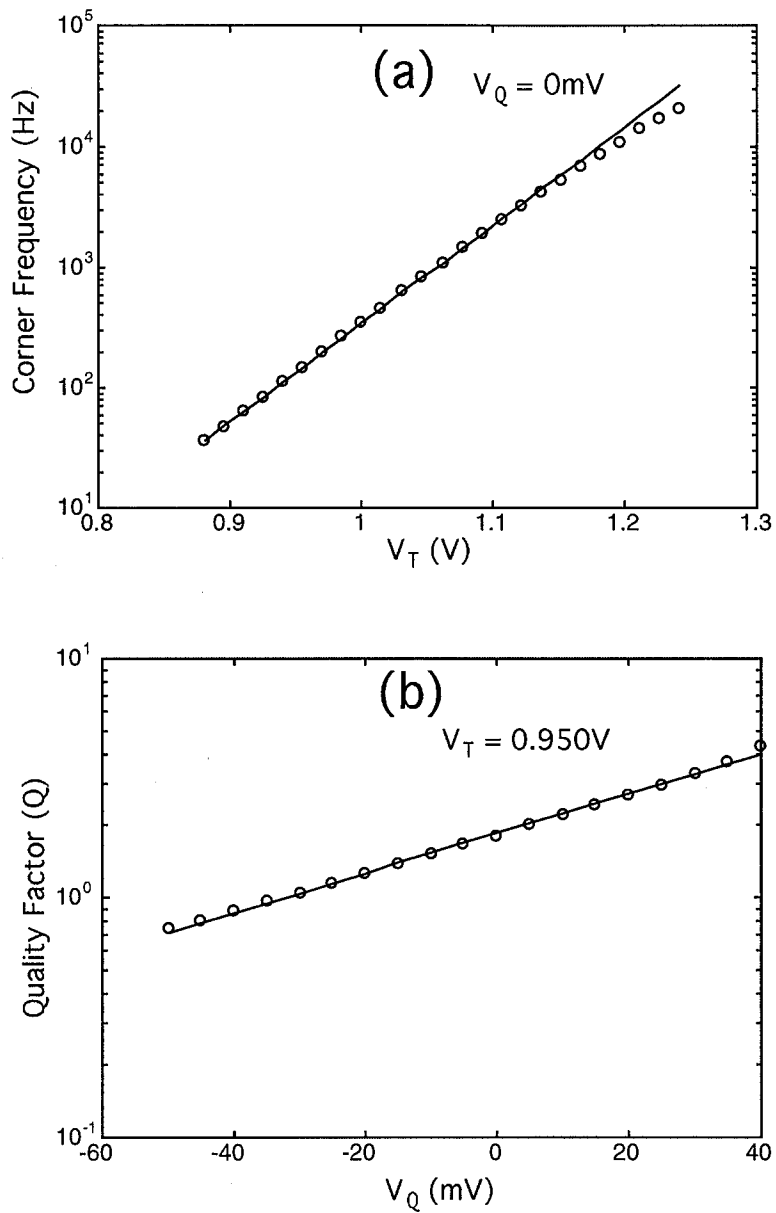


Figure 4.8: Tau-and-Q Control Circuit Characteristics. (a) The corner frequency has an exponential dependence on the voltage  $V_T$ . (b) The quality factor  $Q$  has an exponential dependence on the voltage  $V_Q$ .

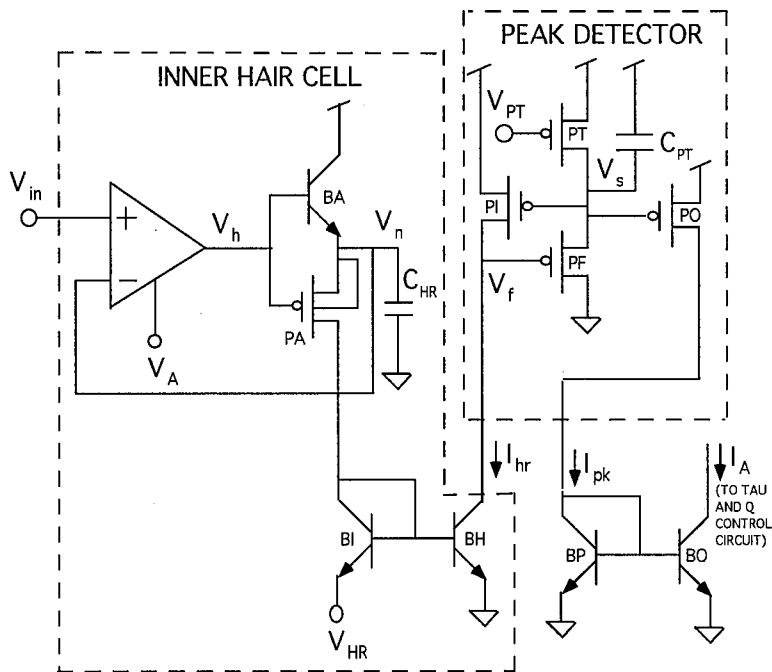


Figure 4.9: The IHC and PD Circuits. The inner hair cell transduces its input  $V_{in}$  to a current  $I_{hr}$  that is then fed to the peak detector. The output of the peak detector  $I_{pk}$  is mirrored to the tau-and-Q control circuit as a gain-control-correction current.

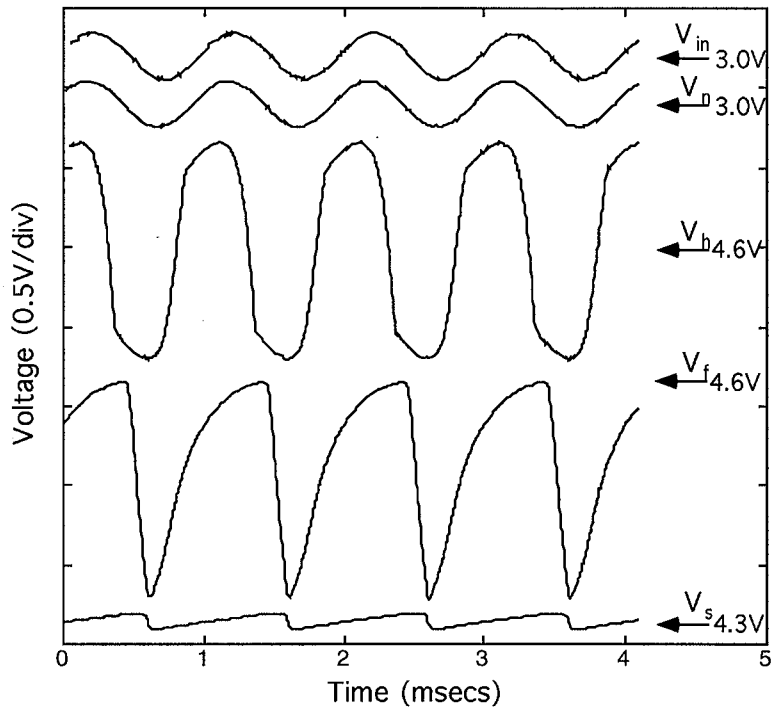


Figure 4.10: The IHC and PD Circuit Waveforms. The waveforms for the voltages  $V_{in}$ – $V_s$  illustrate the operation of the circuits of Figure 4.9.

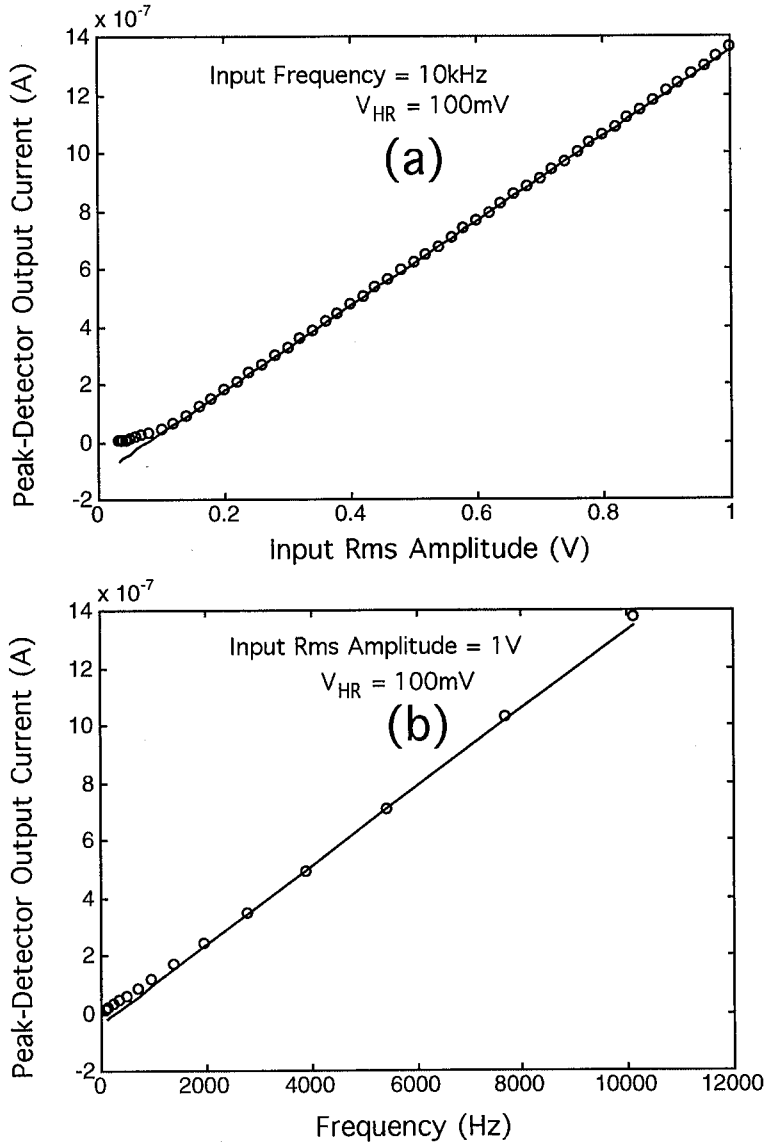


Figure 4.11: IHC and PD Amplitude and Frequency Characteristics. (a) The current  $I_{pk}$  has a linear dependence on the input rms amplitude. (b) The current  $I_{pk}$  has a linear dependence on the the input frequency.

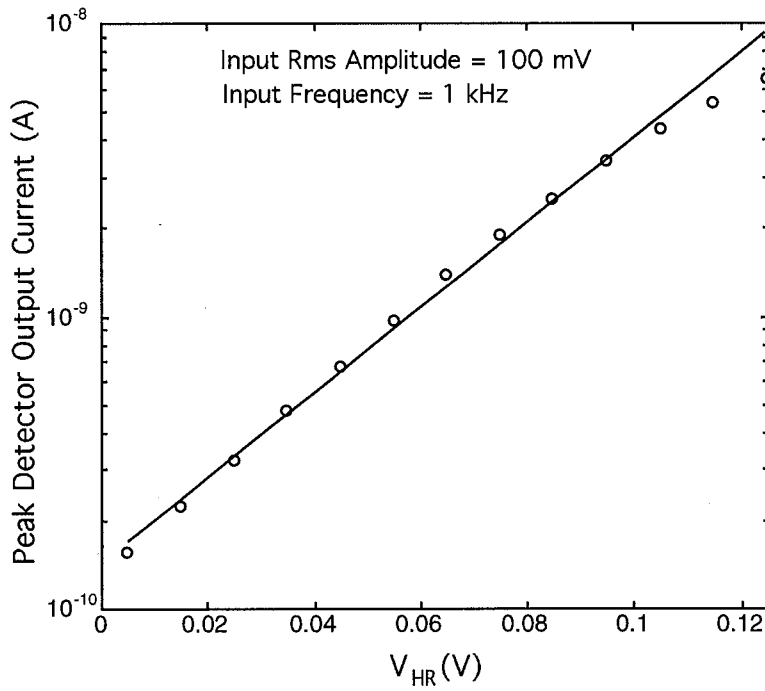


Figure 4.12: Dependence of  $I_{pk}$  on  $V_{HR}$ . The current  $I_{pk}$  has an exponential dependence on the voltage  $V_{HR}$ .

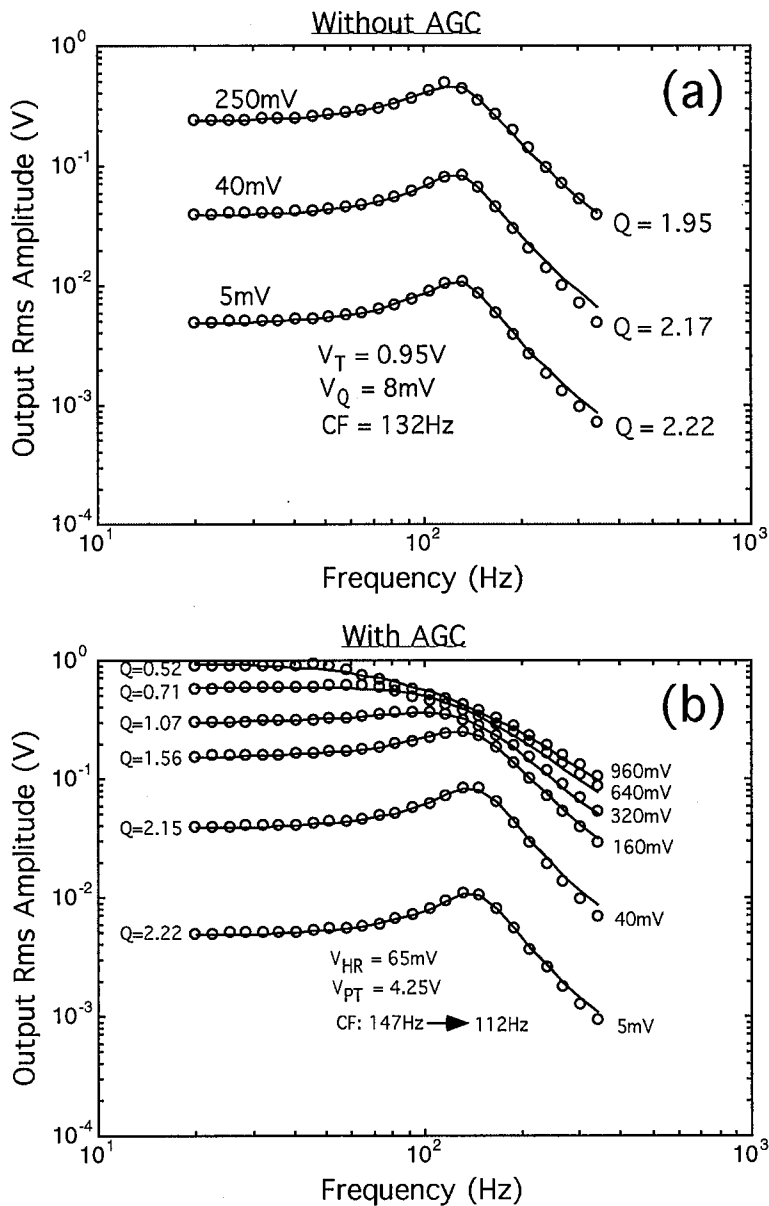


Figure 4.13: Frequency-Response Characteristics of a Stage. (a) Without an AGC, it is impossible to obtain smooth and continuous data beyond an input rms amplitude of 250mV. (b) With an AGC, it is easy to obtain smooth and continuous data up to and beyond a 960mV rms input amplitude.

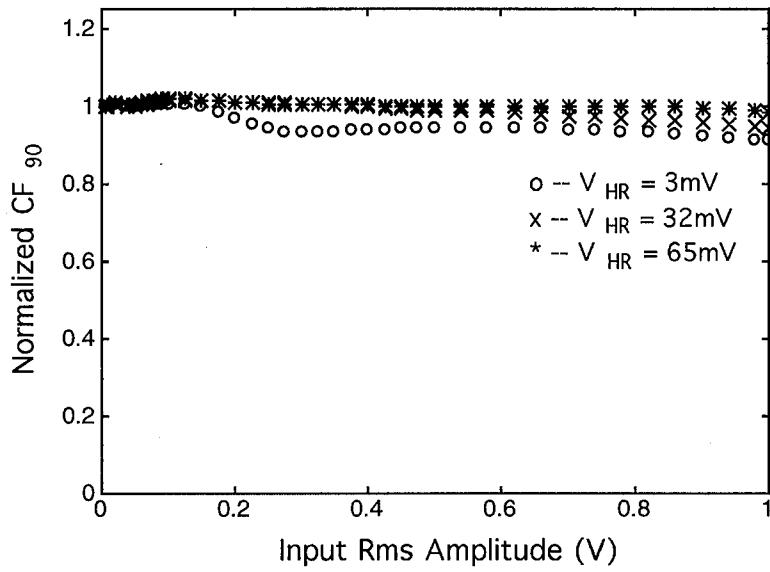


Figure 4.14:  $CF_{90}$  Characteristics. The frequency at which the phase lag of the filter is 90 degrees is relatively invariant with input rms amplitude.



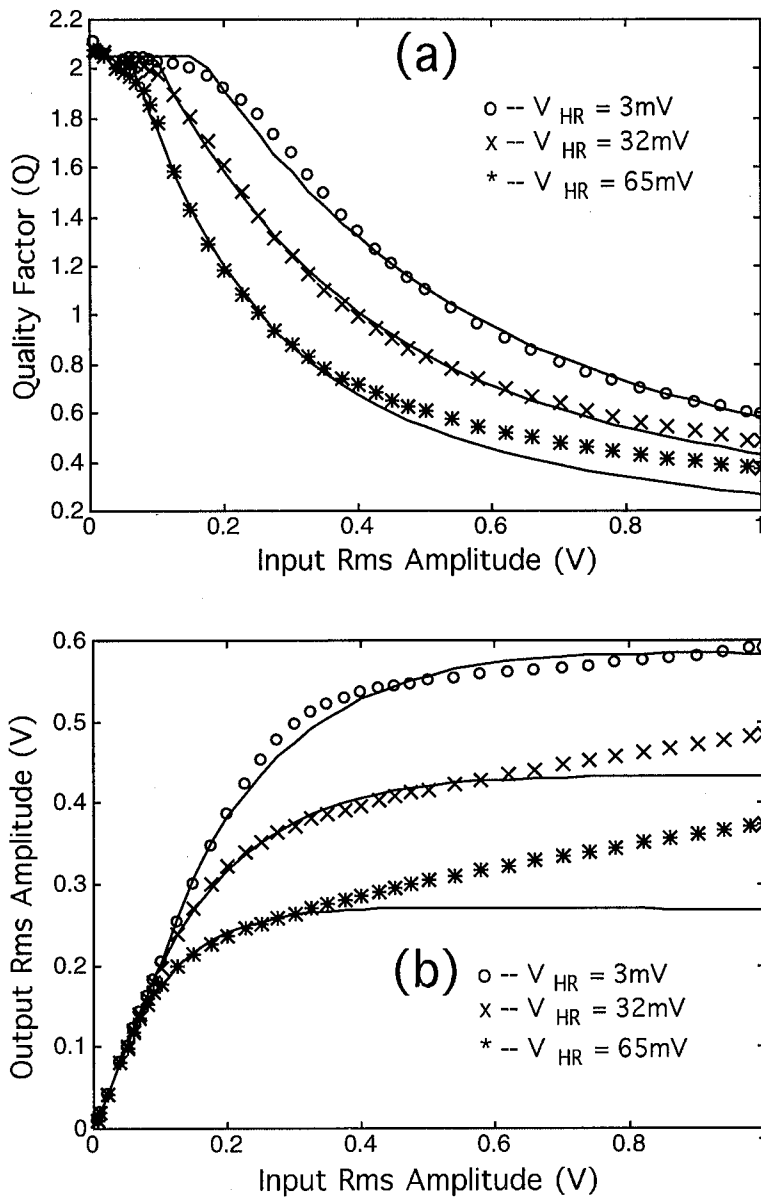


Figure 4.15:  $Q$ -Adaptation Characteristics. (a) The  $Q$  adaptation due to the AGC is well fit by theory, except at large input rms amplitudes, and for strong AGC corrections (large  $V_{HR}$ ). (b) The same data as in (a) except that we plot the output rms amplitude, instead of the  $Q$ .

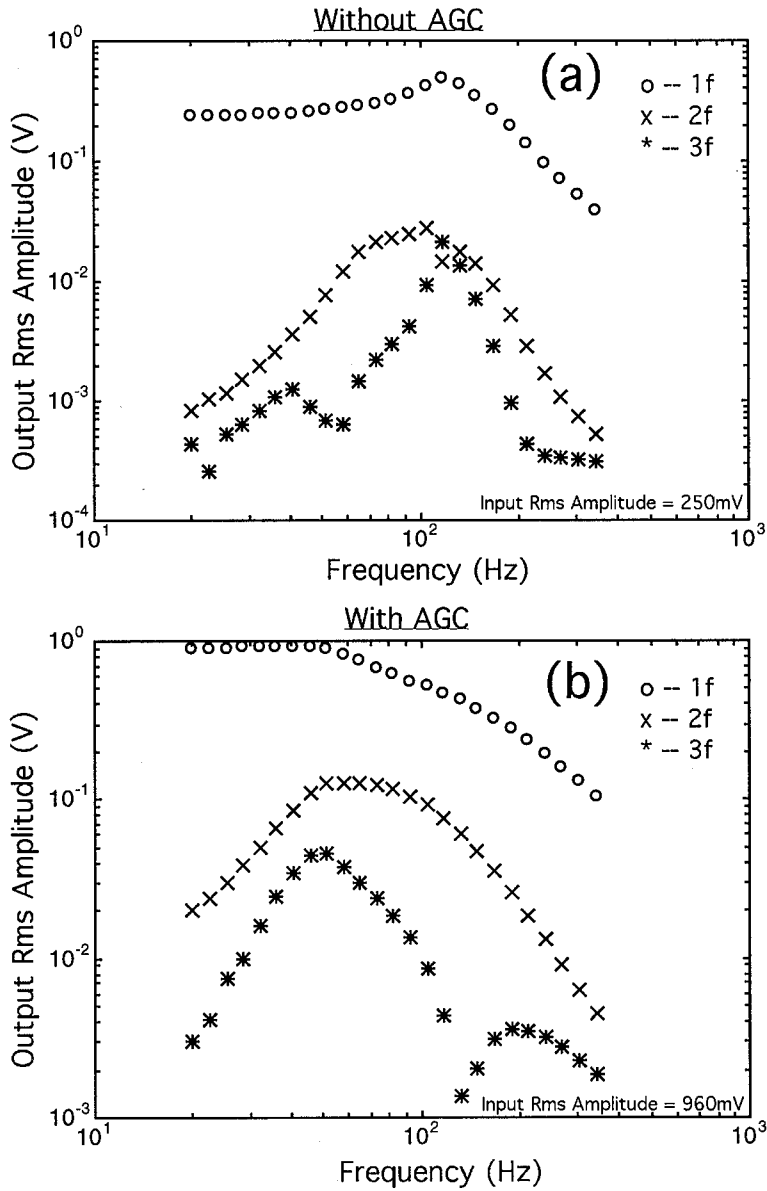


Figure 4.16: Distortion Characteristics of the Filter. (a) Without an AGC, the distortion is already fairly high at a 250mV input rms amplitude. (b) With a strong AGC ( $V_{HR} = 65\text{mV}$ ), the distortion is comparable to that in (a) at only a 1V rms input amplitude.

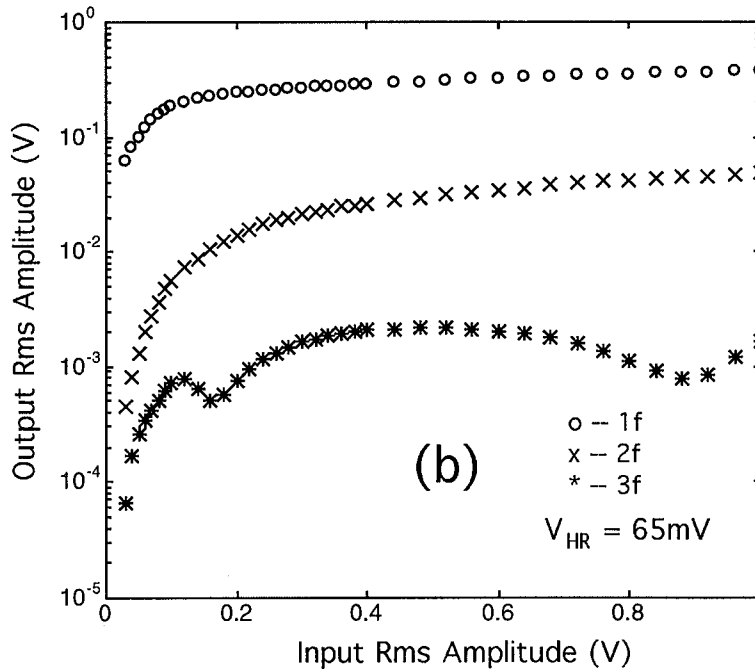
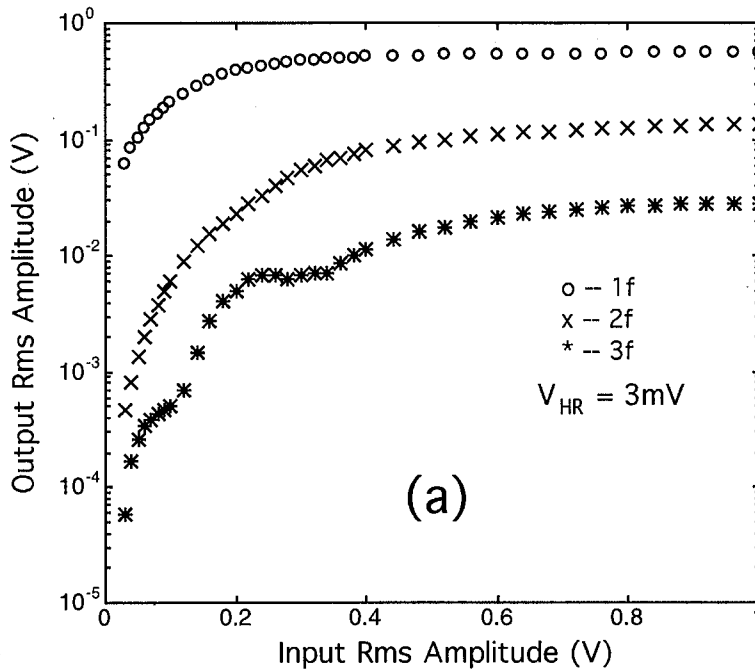


Figure 4.17: Distortion Characteristics at BF. (a) With a weak AGC ( $V_{HR} = 3mV$ ), the distortion levels are significant at a 250mV input rms amplitude. (b) With a strong AGC ( $V_{HR} = 65mV$ ), the distortion levels are smaller than are those in (a) even at a 1V input rms amplitude.

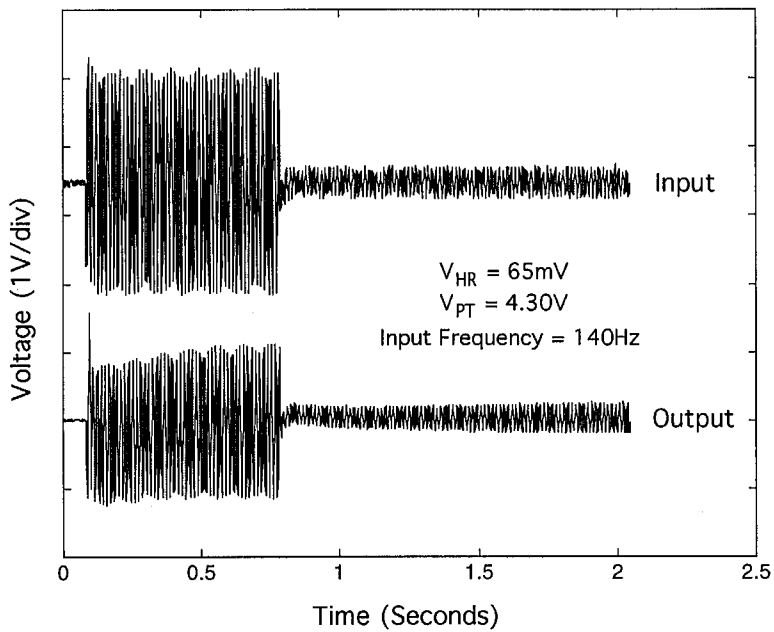


Figure 4.18: Dynamics of  $Q$ -adaptation. The onset of a loud tone at BF preceded by a period of silence causes a brief transient on the first cycle, followed by a restoration to equilibrium. The reduction in intensity of the same tone from a loud to a soft value causes a gradual buildup in the output response as the gain of the AGC adapts.

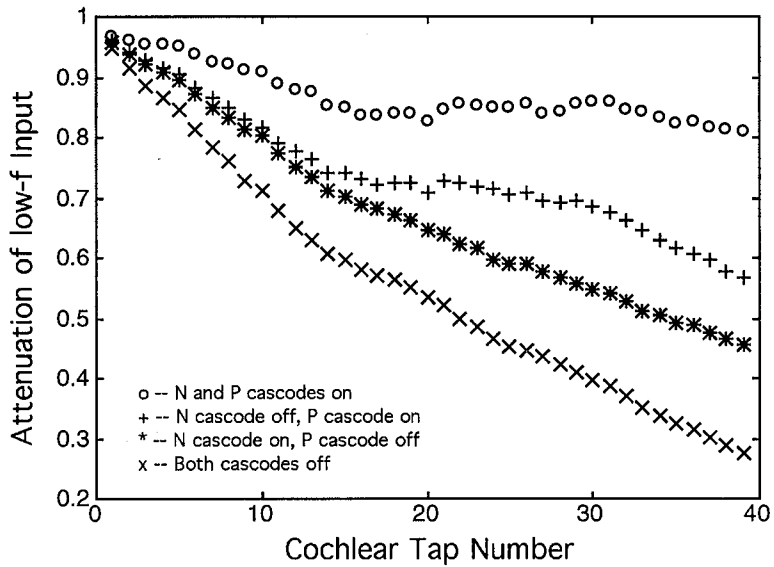


Figure 4.19: Low-Frequency Attenuation in the Cochlea. The low-frequency attenuation for various conditions of open-loop amplifier gain are shown.

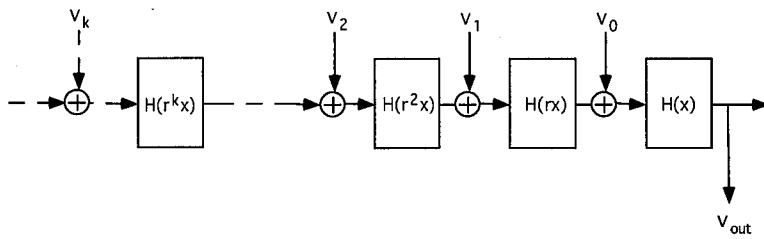


Figure 4.20: Noise Accumulation in the Cochlea. The noise at the output tap of a cochlea,  $v_{out}$  is due to the accumulation, amplification, and filtering of noise from taps preceding that tap.

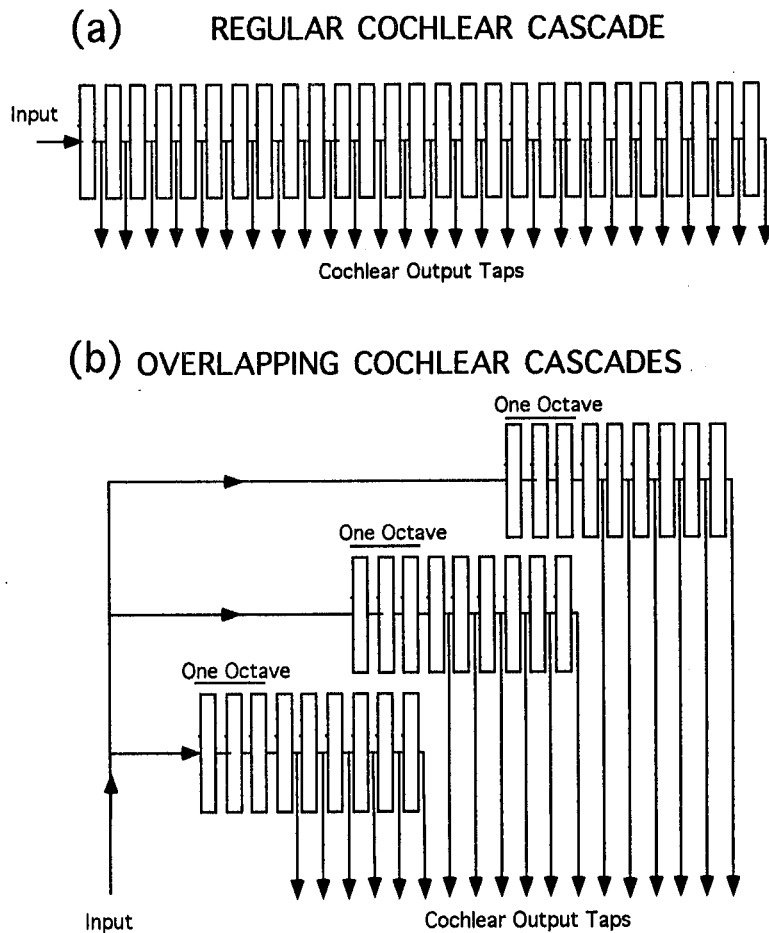


Figure 4.21: Architecture of Overlapping Cascades. (a) In a regular cochlear cascade, the input is fed serially to all stages. (b) In an overlapping cochlear cascade, the input is fed in parallel to tiny cochlear cascades whose corner frequencies overlap by 1 octave.

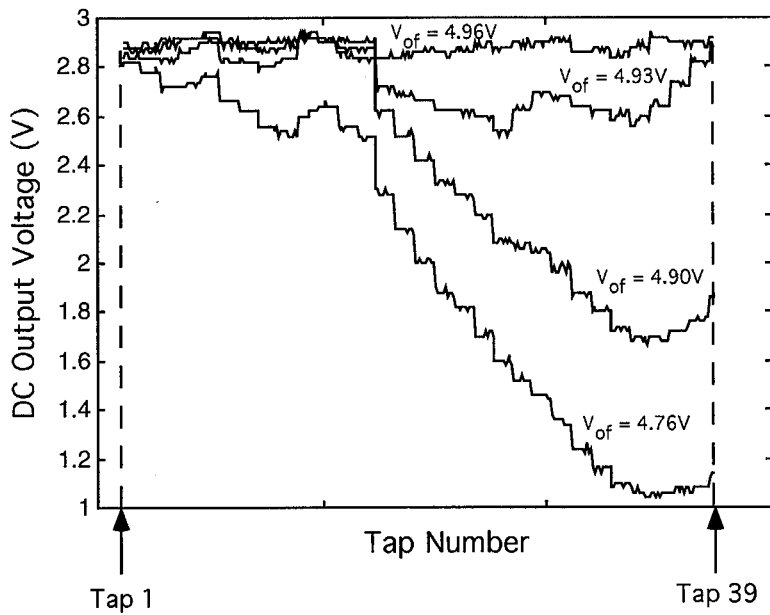


Figure 4.22: Offset Adaptation in the Cochlea. As the loop gain of the offset-adaptation loop, controlled by  $V_{OF}$ , is increased, the offset accumulation across the taps of the cochlea is reduced.



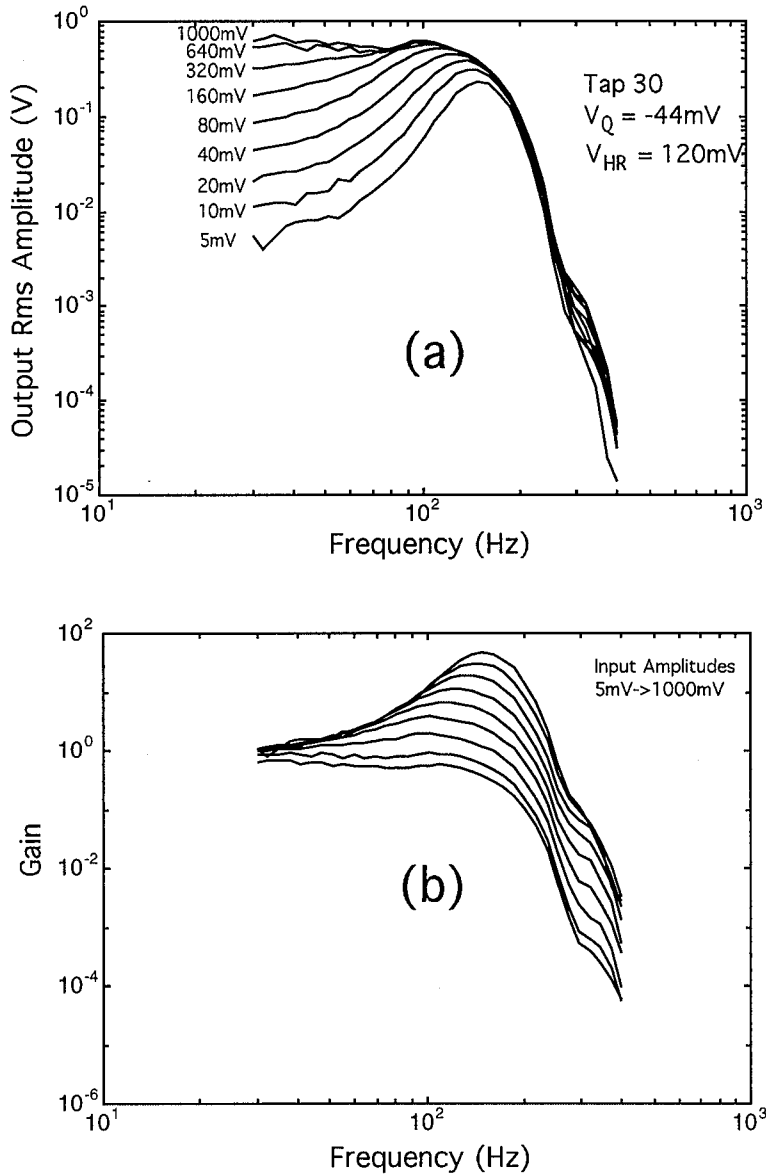


Figure 4.23: Frequency-Response Curves of the Cochlea. (a) The frequency response for various input rms amplitudes is shown. (b) The same data as in (a) except that we plot the gain, instead of the output rms amplitude.

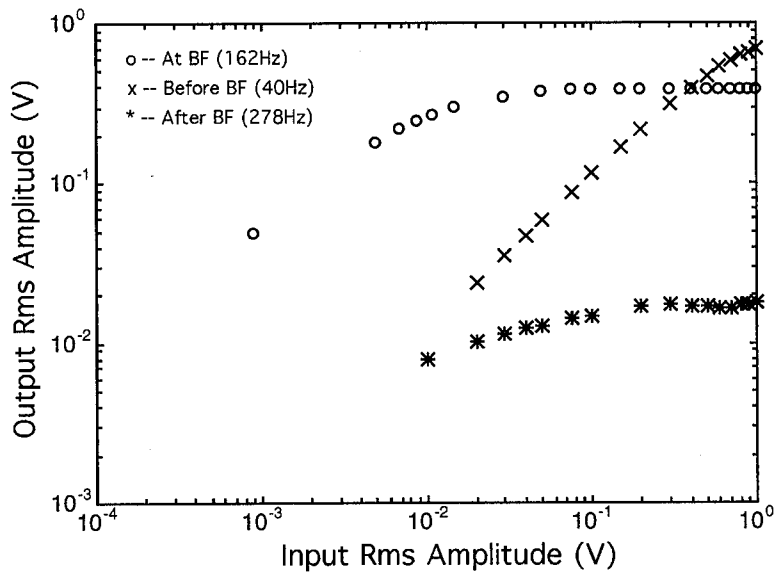


Figure 4.24: Compression Characteristics of the Cochlea. The compression at a cochlear tap occurs primarily at and beyond the BF, whereas the response at frequencies below the BF is linear.

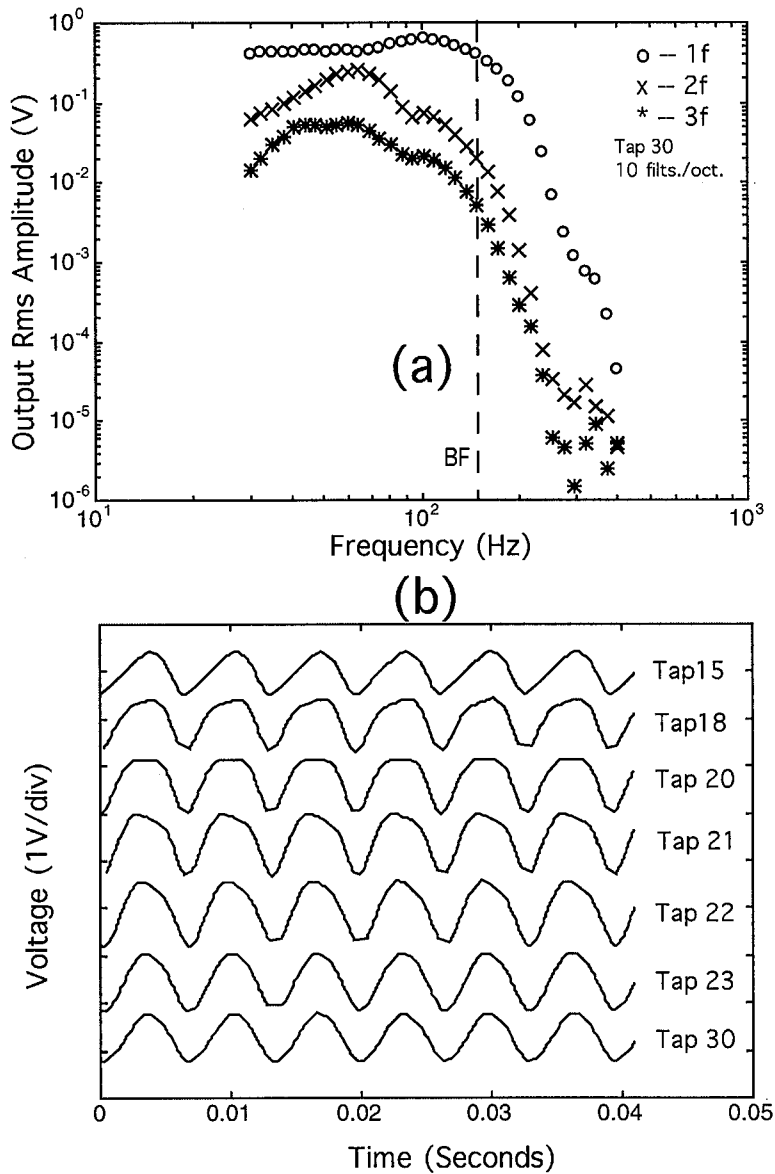


Figure 4.25: Harmonic Distortion Characteristics of the Cochlea. (a) The harmonic distortion is most pronounced 1 octave before the BF, but is sharply attenuated at the BF. (b) The dual effect in space reveals that harmonic distortion is most pronounced 1 octave before tap 30 (at tap 20), but is filtered away by tap 30.

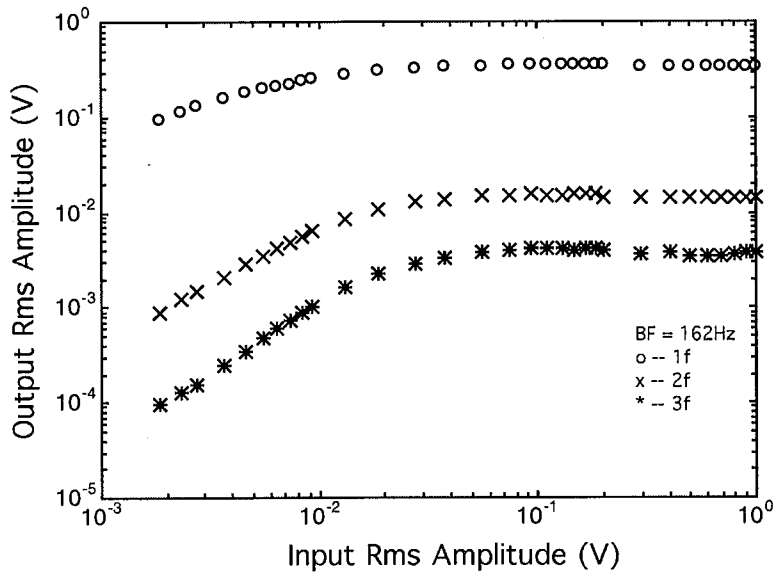


Figure 4.26: Harmonic Distortion at BF in the Cochlea. The total harmonic distortion at BF is at least -30dB for all input rms amplitudes.

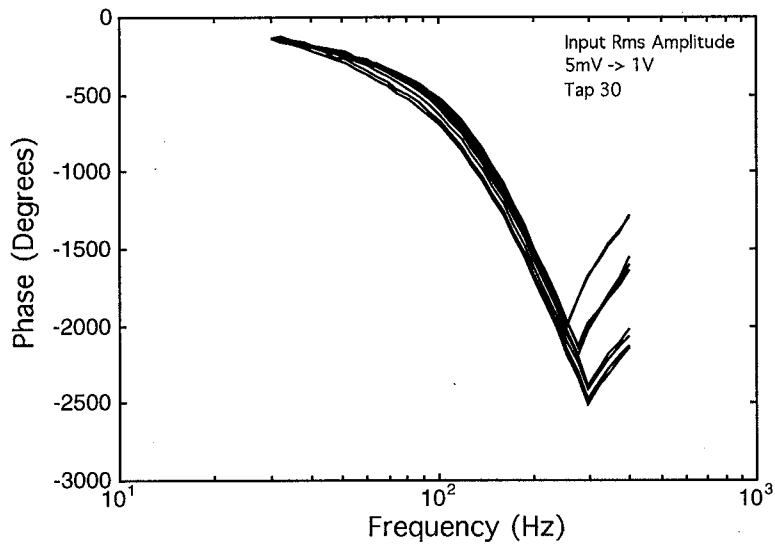


Figure 4.27: Phase Characteristics of the Cochlea. Because the AGC corrects  $Q$ , but not  $1/\tau$ , there is relatively little shift in the phase curves with input rms amplitude. The discontinuous parts of the phase curves are due to parasitic effects.

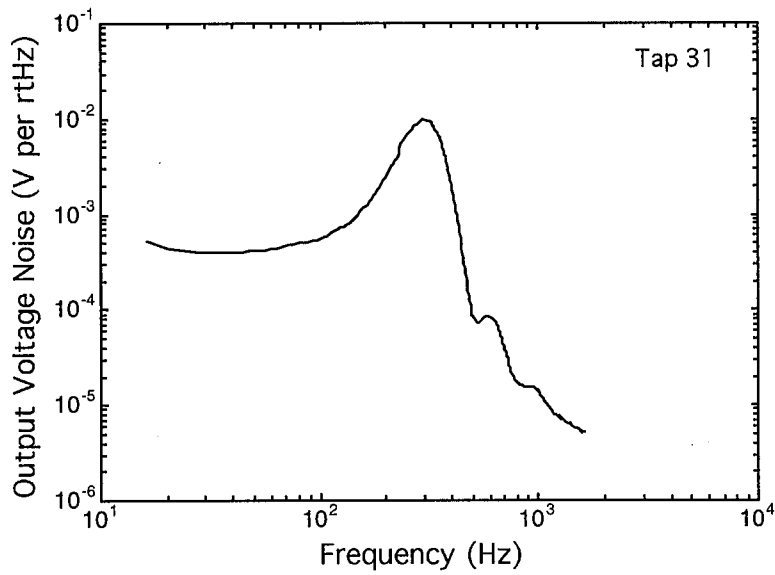


Figure 4.28: Typical Noise Spectrum of a Cochlear Tap. The secondary peaks at the high frequencies are at multiples of the primary peak frequency and are due to nonlinearities.

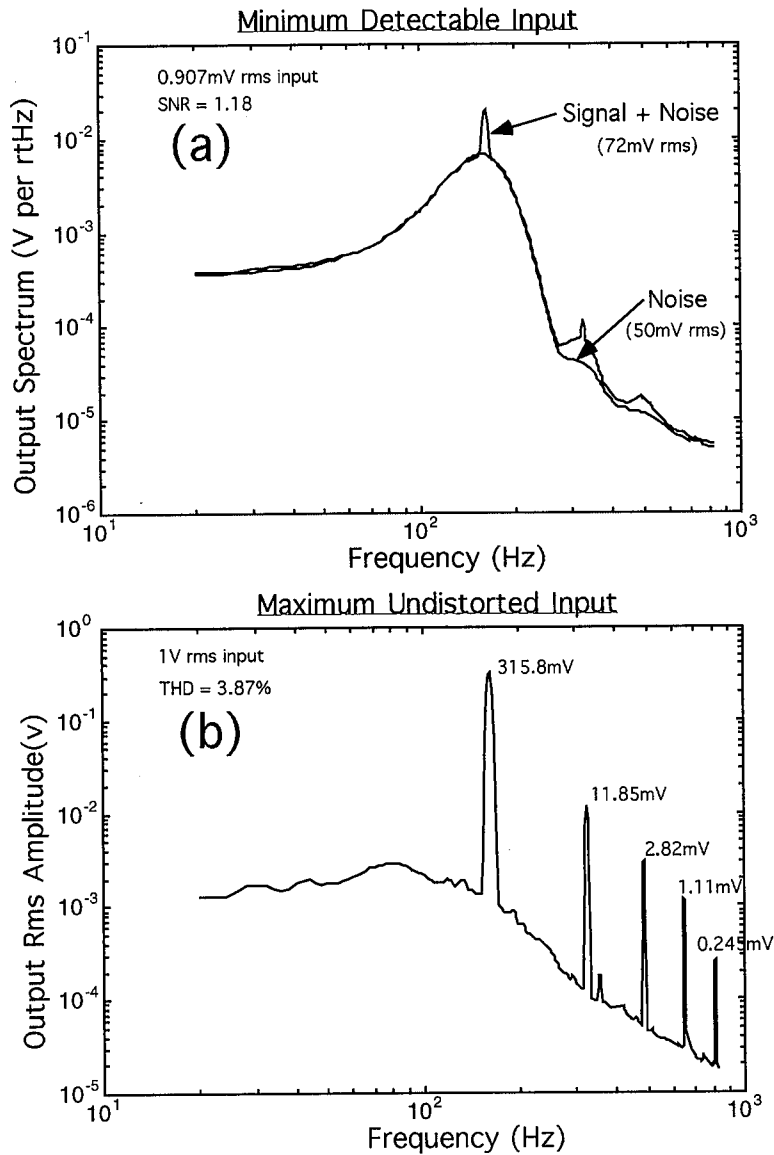


Figure 4.29: Dynamic Range of a Cochlear Tap. (a) The spectra of tap 30 when there is no input present, and when a BF signal that is just above the threshold of audibility is present, are shown. The minimum detectable input at BF was found to be 0.875mV. (b) The total harmonic distortion from all harmonics for a 1V rms input at BF was less than 4%. The maximum undistorted input is thus 1V.

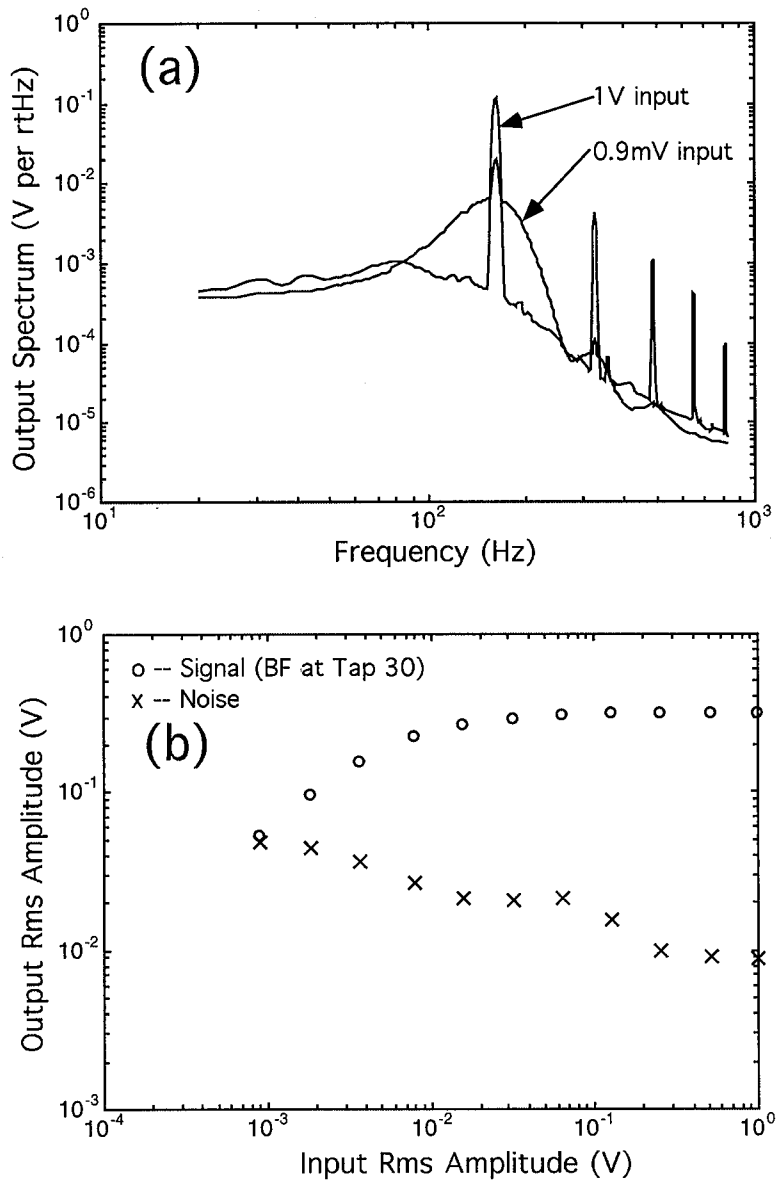


Figure 4.30: Signal-and-Noise Amplitude Characteristics. (a) The output spectrum of tap 30 for a 1V rms and 0.9mV rms input at BF shows the adaptation in  $Q$  and consequent reduction in noise. (b) The output rms amplitude of the signal and of the noise at different input rms amplitudes are shown.



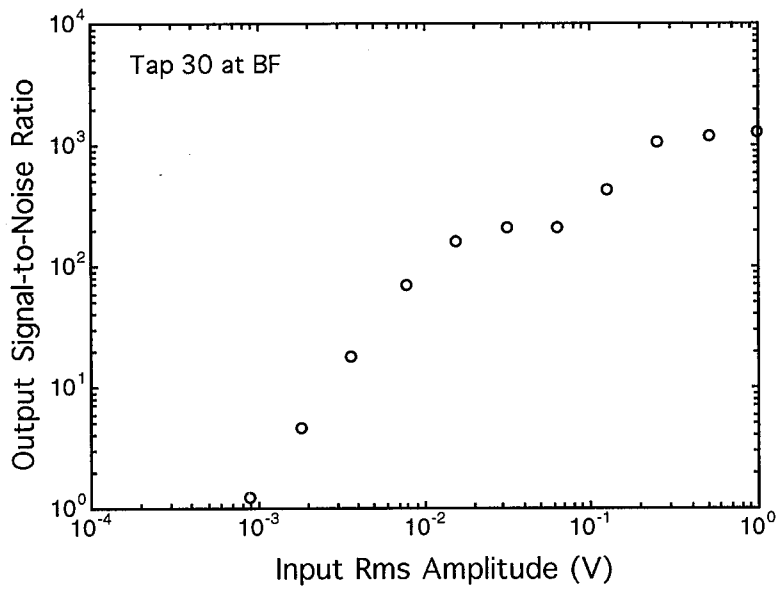


Figure 4.31: SNR Amplitude Characteristics. The output SNR improves by about 30dB (1 to 1241) as the signal changes intensity by about 60dB (0.9mV to 1V)

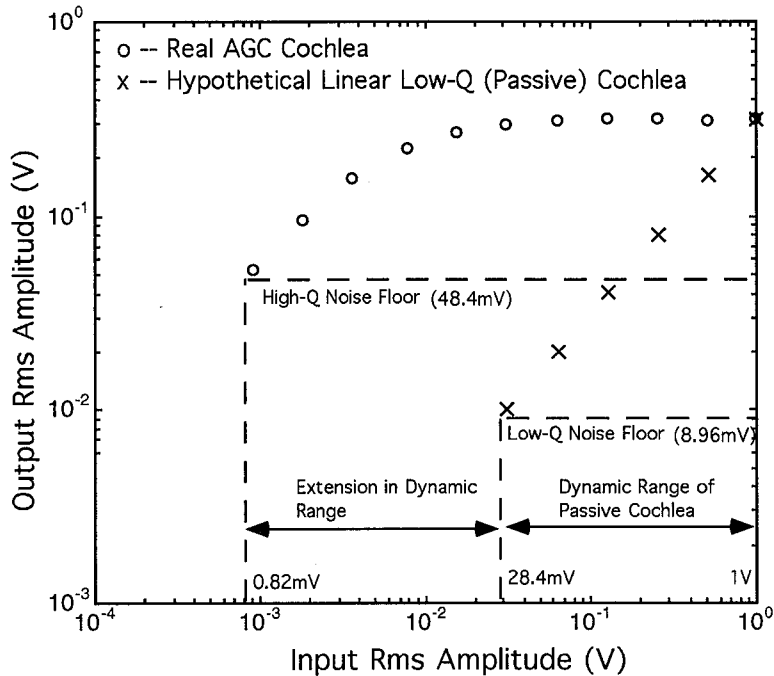


Figure 4.32: Extension of Dynamic Range. A hypothetical low- $Q$  cochlea that is completely linear would have a dynamic range of only 30dB due to the uniformly low gain of 0.315 at all amplitudes; such a cochlea is analogous to the passive biological cochlea with no outer hair cells. Our AGC cochlea has a dynamic range of 60dB because faint signals at 0.82mV are amplified by a factor of 59 to be just above the noise floor of 48.4mV, whereas loud signals at 1V rms amplitude are attenuated by a factor of 0.315 to prevent distortion; such a cochlea is analogous to the active cochlea with outer hair cells.

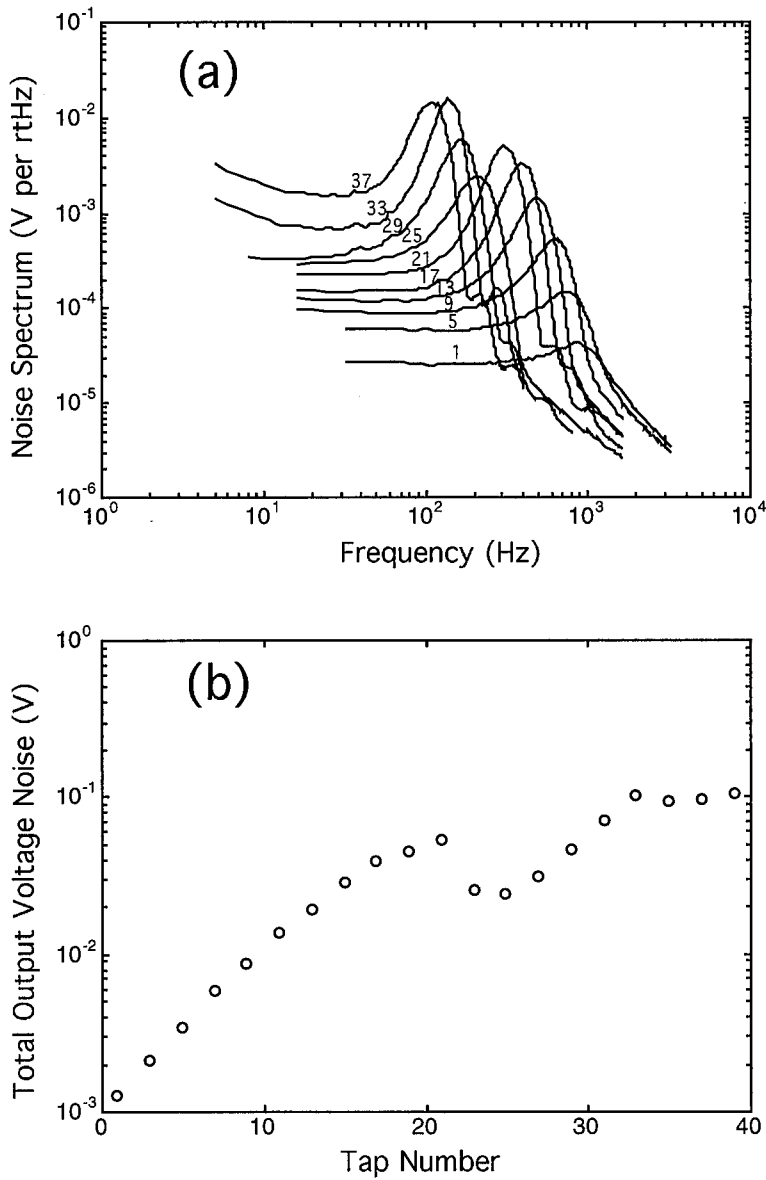


Figure 4.33: Noise Accumulation Across Cochlear Taps. (a) The noise spectra at various cochlear taps are shown. (b) The total output noise integrated over all frequencies asymptotically converges due to the exponential taper of the cochlea. The discontinuities in the curve are due to the discontinuous reduction in bandwidth, in turn due to chip offsets, between taps 21 and 25 in (a)

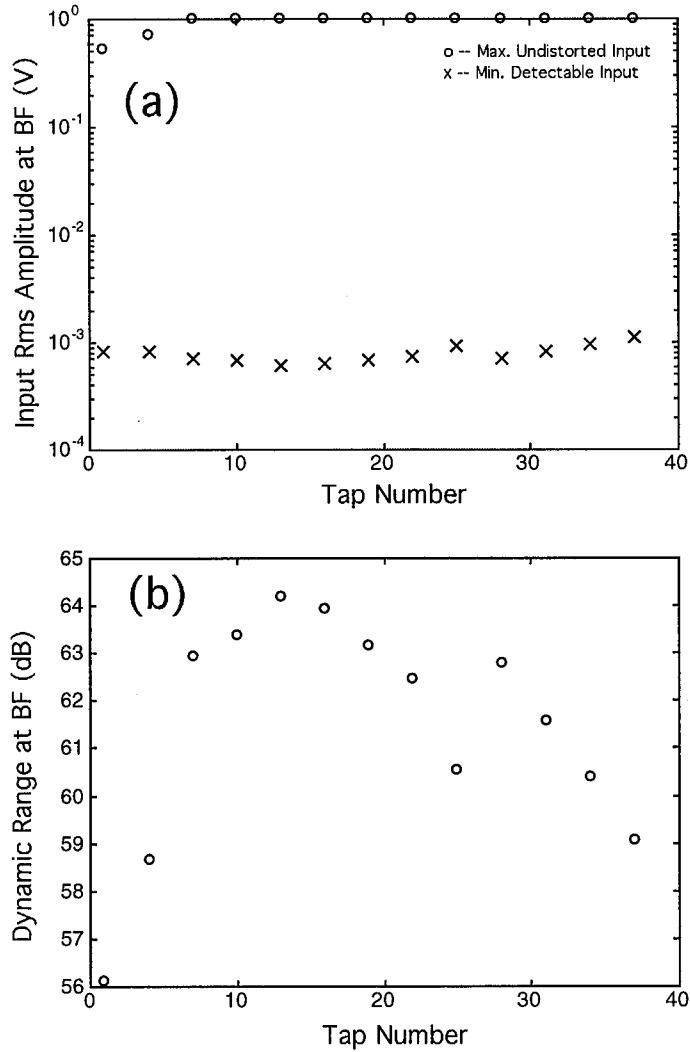


Figure 4.34: Dynamic Range Across Cochlear Taps. (a) The minimum detectable input and maximum undistorted input at various cochlear taps are shown. (b) The dynamic range at BF at various cochlear taps are shown.

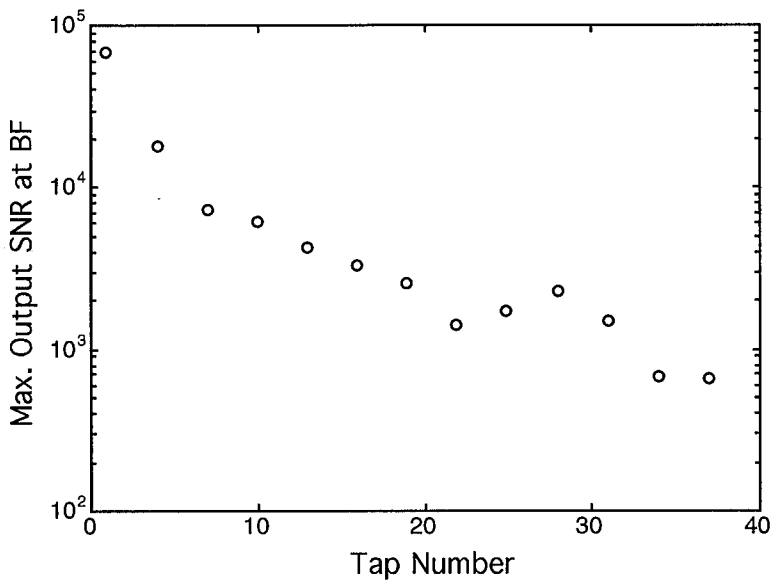


Figure 4.35: SNR Across Cochlear Taps. The maximum output signal-to-noise ratio progressively decreases as we travel down the cochlea due to the accumulation of noise. The numbers represent the ratio of the signal power to the noise power, that is  $10^5$  corresponds to 50dB.

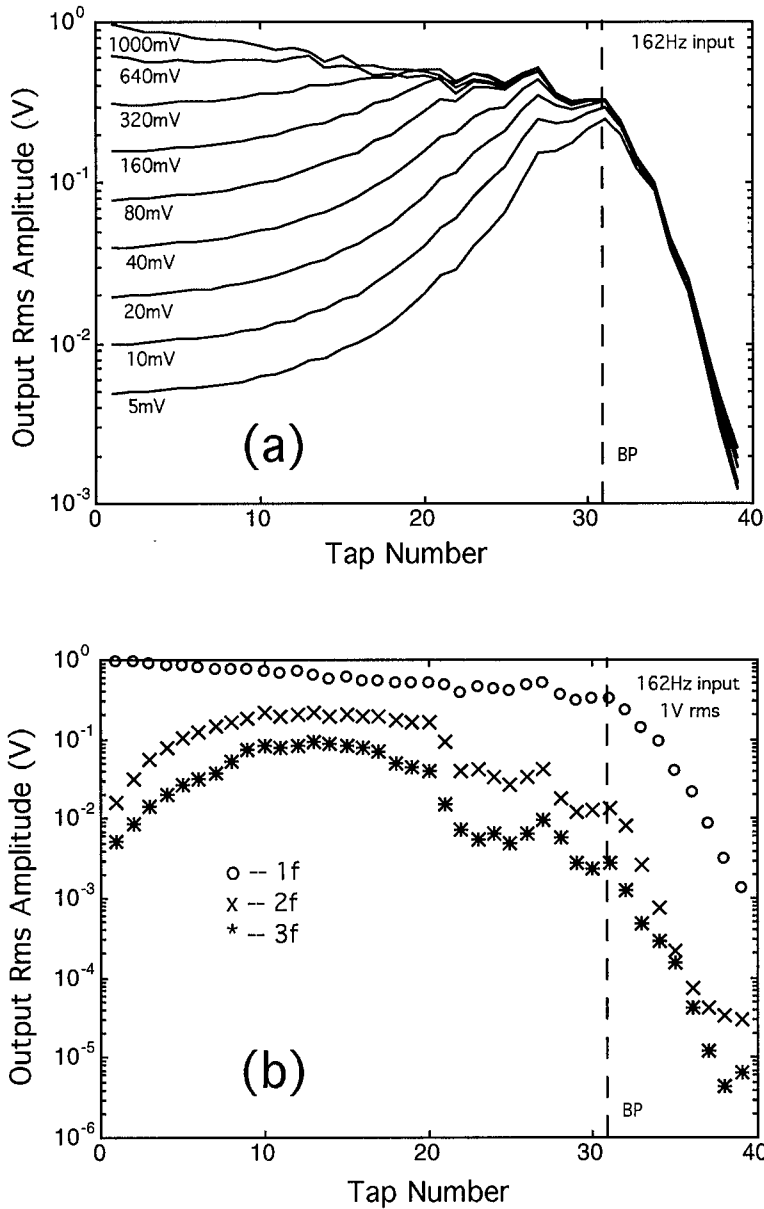


Figure 4.36: Spatial-Response Characteristics. (a) The spatial response at various input amplitudes is remarkably similar to the frequency response at various input amplitudes because of the cochlear frequency-to-place transformation ( $\log(f) \rightarrow x$ ). (b) The harmonic distortion is filtered sharply at the best place (BP); it is at its worst at a place that has a corner frequency that is 1 octave above that of the best-place corner frequency.

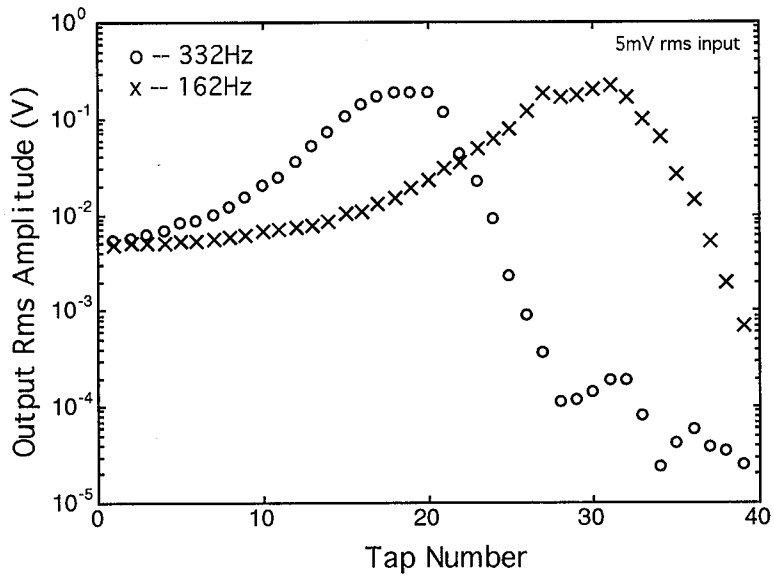


Figure 4.37: The Frequency-to-Place Transformation. The best place for high frequencies occurs earlier than that for low frequencies.

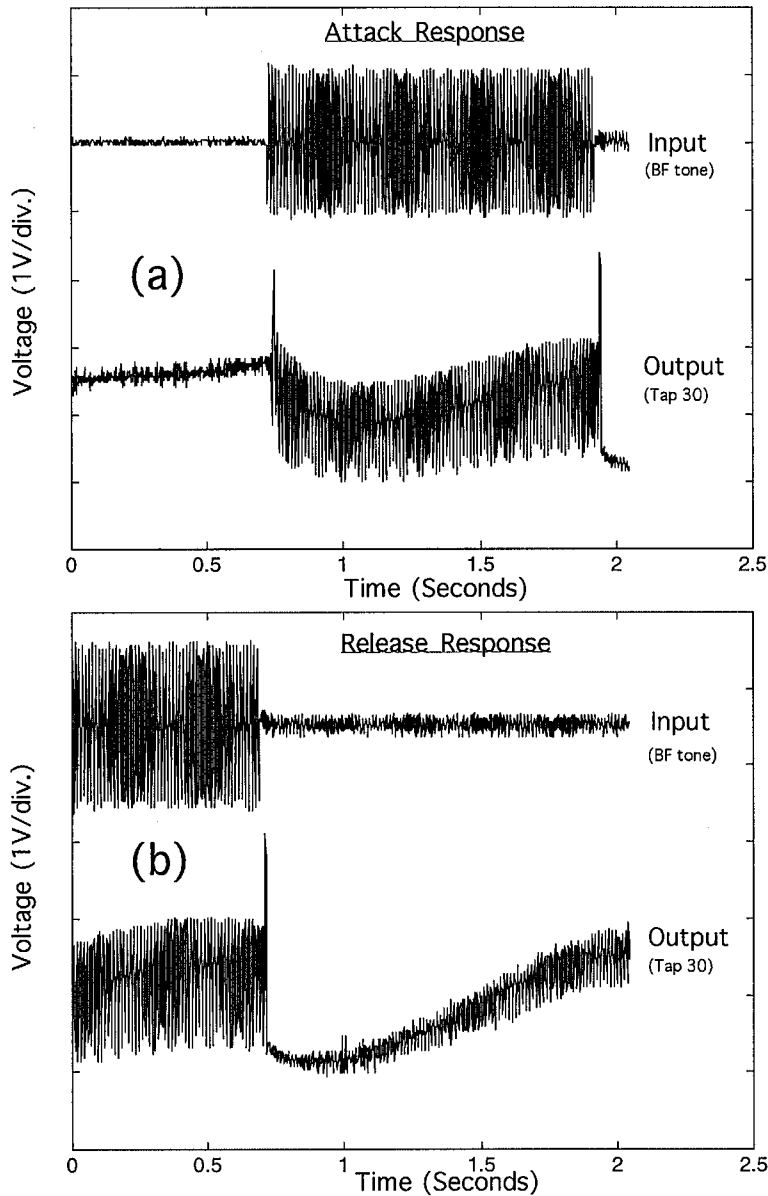


Figure 4.38: AGC and Offset Adaptation. (a) At the onset of a loud input tone after a period of silence, there is a brief output transient followed by quick adaptation of the envelope. The offset adaptation occurs in parallel with the envelope adaptation, which happens on a much slower time scale. (b) The reduction in the intensity of a loud input tone causes a gradual adaptation in the envelope of the signal. The offset adaptation is still slower than the envelope adaptation, but the time scales are more comparable.



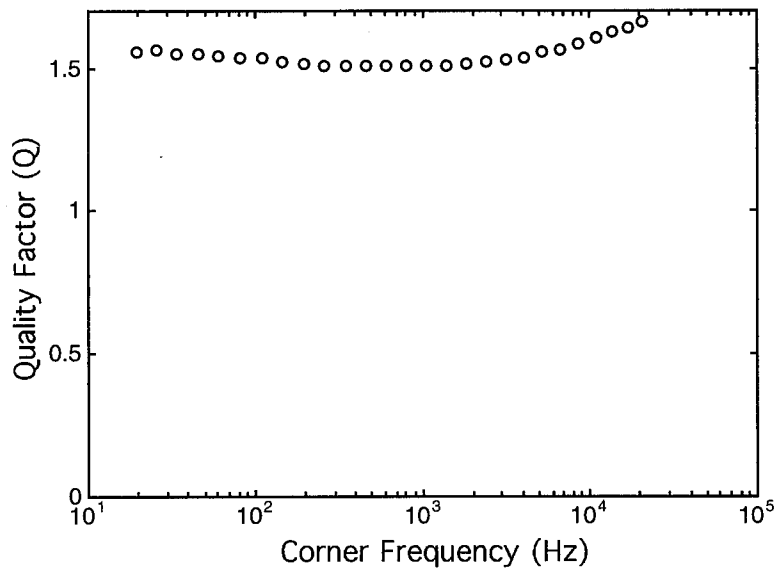


Figure 4.39: The  $Q$  across Cochlear Filters. The  $Q$  across various cochlear taps is fairly well matched.

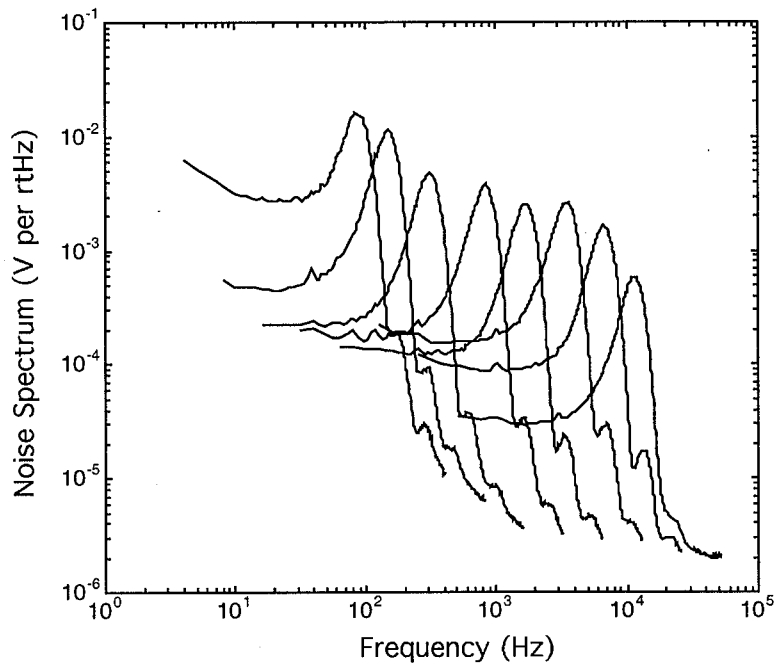


Figure 4.40: The Sounds of Silence. The noise spectra at various cochlear taps from the low, mid, and high-frequency cochleas are fairly similar in shape.

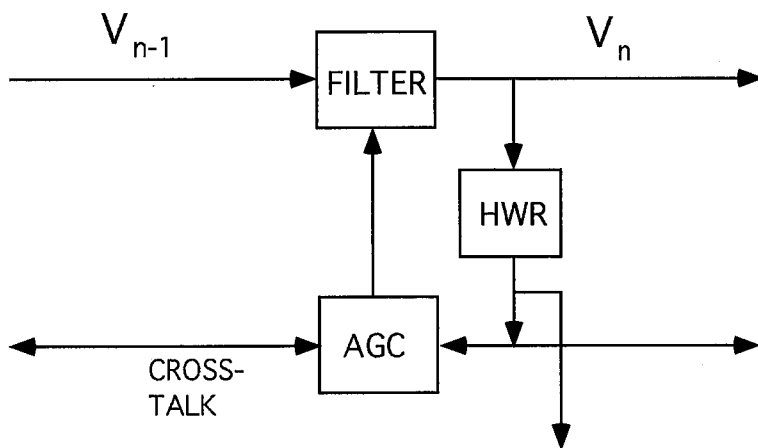


Figure 4.41: The ASIC Digital Cochlea

## Chapter 5 Efficient Precise Computation with Noisy Components: Extrapolating From Electronics to Neurobiology

### Abstract

We review the pros and cons of analog and digital computation. We propose that computation that is most efficient in its use of resources is neither analog computation nor digital computation, but rather is an intimate mixture of the two forms. For maximum efficiency, the information and information-processing resources of the hybrid form must be distributed over many wires, with an optimal signal-to-noise ratio per wire. Our results suggest that it is likely that the brain computes in a hybrid fashion, and that an underappreciated and important reason for the efficiency of the human brain, which only consumes 12W, is the hybrid and distributed nature of its architecture.

### 5.1 Introduction

We estimate that the human brain performs on the order of  $3.6 \times 10^{15}$  synaptic operations per second (see Appendix 5.8.1). From measurements of cerebral blood flow and oxygen consumption, it is known that the brain consumes only 12 W (see Appendix 5.8.2). Its efficiency of computation is thus about  $3 \times 10^{14}$  operations per joule. Our brain is capable of doing tremendously complex computation in real time despite the slow and noisy components in our heads and bodies.

An extremely fast microprocessor such as the DEC Alpha 21164 performs about  $255 \times 10^6$  floating-point operations per second, and consumes 40 W.<sup>1</sup> Its efficiency is thus about  $6.25 \times 10^6$  operations per joule. It is incapable of solving even relatively simple behavioral tasks in real time in spite of its blazingly fast and precise transistors.

---

<sup>1</sup>On the specfp92 Ear Program, which performs auditory computations similar to those in the human ear, the DEC 21164 running on an Alpha Server 8200 5/300 is 1275 times as fast as a VAX 11/780, which would run at about 0.2 MFLOPS for our computation. Thus, we estimate that it is equivalent to about  $1275 \times 0.2 = 255$  MFLOPS. These numbers are for 1995.

If we compare the computing efficiency of the human brain with that of a digital microprocessor, we observe that the brain is at least seven orders of magnitude more efficient.<sup>2</sup> Mead was the first scientist to point out the great discrepancy in the computational efficiencies of neurobiology and electronics [1]; he also pioneered the field of neuromorphic computation—electronic computation inspired by and similar to that performed by neural systems [2].

How is efficient and complex computation with noisy components achieved in neurobiological systems? Mead attributed the enormous efficiency of neurobiological systems to their clever exploitation of the physics of the medium that they were built in, to their local wiring strategies, and to their enormous capabilities to adapt and learn. In this paper we will focus on the tradeoffs involved in using physics to do computation.

At first, it is strange to imagine that physics might have anything to do with computation. However, information is encoded in physical state variables, and information processing is accomplished with the use of physical devices. Thus, questions about what we can compute and how efficiently we can compute are deeply linked to the way the physical world works [3]– [4]. The Universal Turing machine helped us to understand that a language with an extremely minimal vocabulary is sufficient for expressing almost any concept. However, it helped to obscure that a language with a rich vocabulary can express, in a few sentences, concepts that would take several paragraphs to express in an impoverished language. Proposals for molecular computing [5] and quantum computing [6], [7] have suggested that problems that take an exponential number of resources in conventional digital computing may be reduced to problems that take a polynomial number of resources in these paradigms of computing. So far, neither of these proposals has been made to work for large-scale systems. However, they have both reminded us of the importance of the underlying physical substrate in computation.

The three resources that a machine uses to perform its computation are also ultimately physical: time, space, and energy. Computer scientists have traditionally treated energy as

---

<sup>2</sup>It may be argued that our comparisons have not been fair since the floating-point computations that a microprocessor performs are more complex than are those that a synapse performs, and are also more precise. However, in addition to multiplication, synaptic computations involve temporal filtering and adaptation, which are fairly complex operations in digital computation. We have also neglected several complex spatiotemporal correlations and additions that are performed in the dendrite of a neuron. Thus, for simplicity, we have chosen to just compare the efficiency of an “elementary operation” in digital computation and in neurobiology. There are so many orders of magnitude of discrepancy between neurobiology and electronics that such concerns will not alter our conclusions.

a free resource, and have focused mostly on time (the number of clock cycles required for the computation to terminate) and space (the amount of memory needed or the number of devices needed to perform the computation). However, energy cannot be treated as a free resource when we are interested in systems of vast complexity, such as the brain. With the current efficiencies of digital computation, it would take us tens of megawatts (the power of about 10,000 furnaces!) to build a system like the brain, assuming we could do so at all. If we wanted to make this system portable as well, energy constraints would be very important indeed. Energy has clearly been an extremely important resource in natural evolution. For an interesting discussion on energy constraints in biology and evolution see [9] and [10]. On a smaller scale, today, energy constraints are important in all portable applications such as radio telephony, laptop computing, and hearing aids.

Biological systems typically compute constantly, rather than episodically, with the resource of time fixed by the computational requirements of the task. For example, for a sensorimotor task we may need to respond within a few hundred milliseconds, whereas for the task of hearing a 1Khz tone, we will need to respond to cycle by cycle variations on a one 1msec time scale. Thus, throughout this paper, we will assume that the bandwidth of the computational task is fixed and that the resource of time is not a degree of freedom (it will be a parameter in our equations but will not be a variable). The other two resources (energy and space) will be degrees of freedom; we shall use the more natural resources of power (energy per unit time) and area (the spatial resource in a two-dimensional substrate such as nerve membrane or in VLSI) as our degrees of freedom.

*Suppose that we are given two systems, A and B, that do a computation at the same bandwidth, at the same output information rate, and with the same input. Then, A is more efficient than B if it consumes less power (and/or area) in doing this computation. In this paper, we shall be interested in understanding the reasons for the efficiency of one system over another.*

Electronic systems are far simpler to understand and analyze than are biological systems. So, in Sections 5.2 and 5.3, we begin by analyzing electronic systems. In Section 5.4, we use the insights gained by this analysis to outline how efficient precise computation can be achieved by hybrid and distributed electronic architectures. In Section 5.5 we extrapolate our ideas for electronic systems to neurobiological systems. In Section 5.6 we describe other reasons for the efficiency for the brain, besides its hybrid and distributed architecture. In

Section 5.7 we conclude by summarizing our contributions.

## 5.2 Analog Versus Digital: The Intuitive Picture

Electronic systems operate with continuous signals (CS) or discrete signals (DS), and in continuous time (CT) or discrete time (DT). Thus, there are four classes of systems: CSCT, CSDT, DSCT, DSDT. Figure 5.1 shows examples of systems, either electronic or biological, in each class. Typically, continuous-signal systems are referred to as analog, and discrete-signal systems are referred to as digital, irrespective of their representation in the time domain. In this paper, we shall first concentrate on those analog systems that are continuous in both the signal and time domains (CSCT), and on those digital systems that are discrete in both the signal and time domains (DSDT). Such systems are the most common examples of analog and digital systems respectively, and are also the most disparate from each other. Later, in Section 5.4, we shall discuss why an alternation between the CSCT and DSCT domains can be advantageous over operation in the DSDT or CSCT domain alone. We shall ignore the CSDT domain in this paper because its relevance to neurobiology is generally believed to be small.

We now tabulate some of the pros and cons of analog (CSCT) and digital (DSDT) systems from a signal-processing viewpoint. The tabulation reflects our own biases on what we believe to be of importance in the context of this paper. It is by no means a comprehensive and exhaustive list of all the differences between analog and digital systems. For example, we completely omit all discussion of programmability and learning in these systems, although these issues are very important; also, we omit all discussion of temporal aliasing, which is an important source of distortion in discrete systems.

### ANALOG

1. Compute with continuous values of physical variables in some range, typically between Gnd and Vdd.

### DIGITAL

1. Compute with discrete values of physical variables, typically Gnd and Vdd, denoted by 0 and 1 respectively.
2. Primitives of computation arise

from the physics of the computing devices:

physical relations of NFETs, PFETs, capacitors, resistors, floating-gate devices, Kirchoff's current and voltage Laws etc.

The use of these primitives is an art form, and does not lend itself easily to automation.

The amount of computation squeezed out of a single transistor is high.

3. One wire represents many bits of information at a given time.
4. Computation is offset-prone since it's sensitive to the parameters of the physical devices. The degradation in performance is graceful.
5. Noise is due to thermal fluctuations in physical devices.
6. Signal is not restored at each stage of the computation.
7. In a cascade of analog stages, noise starts to accumulate. Thus, complex systems with many stages are difficult to build.

from the mathematics of Boolean logic:

logical relations like AND OR, NOT, NAND, XOR.

The use of these primitives is a science, and lends itself easily to automation.

The transistor is used as a switch, and the amount of computation squeezed out of a single transistor is low.

- One wire represents 1 bit of information at a given time.
- Computation is not offset-prone since it's insensitive to the parameters of the physical devices. However, a single bit error can result in catastrophic failure.
- Noise is due to roundoff error.
- Signal is restored to 1 or 0 at each stage of the computation.
- Roundoff-error does not accumulate significantly for many computations. Thus, complex systems with many stages are easy to build.



### 5.2.1 Physicality: Advantage Analog

Items 1 through 3 show that analog computation can be far more efficient than digital computation because of analog computation's repertoire of rich primitives; For example, addition of two parallel 8-bit numbers takes one wire in analog circuits (using Kirchoff's current law) whereas it takes about 224 transistors in CMOS digital circuits. The latter number is for a cascade of 8 full adders. Similarly an 8-bit multiplication of two currents in analog computation takes 4-8 transistors, whereas a parallel 8-bit multiply in digital computation takes approximately 3000 transistors. Although other digital implementations could make the comparisons seem less stark, the point here is simply that exploiting physics to do computation can be powerful. The advantage of an analog machine over a digital machine is especially great when there is a straightforward mapping between the operations needed in the computation and the primitives of the technology. For large-scale systems, e.g. in the implementation of silicon cochleas [8], depending on the nature of the digital implementation, the advantage can range from a factor of 300 to  $10^5$  in power consumption.

Because the number of devices required to perform a computation is greater in digital systems, there is more wiring and communication overhead. The presence of more devices and more communication overhead cause digital circuits to have typically higher area consumption than that of analog circuits. The switching-energy dissipation due to the large number of devices and the communication overhead also causes the power consumption to be higher in digital circuits. If the number of devices switching per clock cycle is  $N$ , the clock frequency is  $f$ , the average load capacitance that a device has to drive is  $C$ , and the power-supply voltage is  $V_{DD}$ , then the power consumption  $P_D$  of digital circuits is given by the simple formula

$$P_D = NfCV_{DD}^2. \quad (5.1)$$

Unlike digital CMOS circuits, whose power dissipation occurs only during switching and is entirely dynamic, many analog circuits have standby or static power dissipation and little or

no dynamic power dissipation.<sup>3</sup> Thus their power dissipation is given by the simple formula

$$P_A = NV_{DD}I, \quad (5.2)$$

where  $N$  is the number of computational stages,  $V_{DD}$  is the power-supply voltage, and  $I$  is the average bias current flowing through each computational stage.

We can make digital circuits more efficient in area and power by using bit-serial implementations, by lowering power-supply voltages, by reducing clock frequency, and by using more parallelism [11]– [12]. The net effect of these improvements is that the efficiency gap between analog and digital computation shrinks, although analog computation still retains its advantage.

### 5.2.2 Noise and Offset: Advantage Digital

Although the use of physics made analog systems much more efficient than digital systems, items 4 through 7 reveal that the very same physics causes analog systems to be much more sensitive to noise and offset than digital systems. *The use of continuous signal variables precludes analog systems from having any discrete attractor state to which they can be restored.* Thus, for a sufficiently complex computation the noise accumulation in analog systems becomes severe, not enough precision can be maintained at the output of the system, and analog systems clearly emerge as the losers.

Adaptation can help to compensate for offset in analog systems. However, performance is still ultimately limited by residual offsets due to the finite loop gains of the compensating circuits, and by the offsets introduced by the compensating circuits themselves. If the compensation of offset is done periodically or continuously, such that it remains bounded throughout the computation, then the presence of offsets can cease to be a problem in analog systems. Care must be taken to ensure that the feedback loops do not cause unwanted dynamics due to interactions with the rest of the analog system.

We can attenuate noise to an arbitrarily low amount if we are willing to spend an arbitrarily large amount of power (and/or area resources). However, as we shall show in Section 5.3, by this point a digital solution would be more efficient than is an analog solution.

---

<sup>3</sup>Of course, Class AB analog systems have dynamic power dissipation but we are focusing on only general trends.

It is interesting to note that components in digital computation have not always been reliable. In the early days of digital computation, vacuum tubes had failure probabilities of one part in a thousand, and very complex computations could simply not be performed without resulting in large errors. One of the pioneers of digital computation, John Von Neumann, gave an entire set of lectures devoted to the problem of correcting errors in digital circuits through the use of redundant signal representations and signal-restoration components[13]. Von Neumann also speculated, with the limited knowledge that was available at the time, on the possibilities for analog computation in the nervous system.

### 5.3 Analog Versus Digital: The Quantitative Picture

In this section we quantify the intuitive picture of Section 5.2. To make progress, we need to have an understanding of what causes noise in the devices with which we compute, and of how the noise accumulation from the various devices in a system degrades the output signal-to-noise ratio of an analog system.

#### 5.3.1 Noise in MOS Transistors

Appendix 5.9 contains a detailed discussion of noise in MOS transistors. Here, we discuss only the most important ideas.

We usually treat current as though it is the flow of a continuous fluid, although it is the flow of discrete charged electrons. Due to thermal fluctuations, these electrons have random, diffusive motions that are uncoordinated with one another. These incoherent motions give rise to shot-noise currents and cause white noise in the device. The noise is called *white* because its power spectrum is flat. Intuitively, by simple  $\sqrt{N}$  law-of-large-numbers arguments, we might expect that shot noise would be less important at larger current levels because we average over the motions of more electrons per unit time. This intuition is indeed borne out. For further details of shot noise in transistors, see [14]. White noise is fundamental, and is present in all physical devices at room temperature. The input-referred white noise of an MOS transistor is given by

$$v_n^2 = \frac{K_w(p)}{I^p} \Delta f, \quad (5.3)$$

where  $p = 1.0$  in the subthreshold region of operation of the MOS transistor, and  $p = 0.5$  in the above-threshold region of operation of the MOS transistor;  $I$  is the DC current through the transistor; and  $\Delta f = f_h - f_l$  is the bandwidth of operation, with  $f_h$  and  $f_l$  being the highest and lowest frequencies of operation; the technology-dependent parameter  $K_w(p)$  increases with temperature and with thick gate oxides, and is given by

$$K_w(1.0) = \frac{4kTU_T}{2\kappa^2} \quad (5.4)$$

in the subthreshold regime, and by

$$K_w(0.5) = \frac{4kT(2/3)}{\sqrt{(2\mu C_{ox} \frac{W}{L})}} \quad (5.5)$$

in the above-threshold regime. The parameter  $\kappa$  is the subthreshold exponential coefficient;  $kT$  is a unit of thermal energy;  $U_T = kT/q$  is the thermal voltage where  $q$  is the charge on the electron;  $\mu$  is the mobility of the electron;  $C_{ox}$  is the oxide capacitance; and  $W$  and  $L$  are the width and length of the transistor, respectively. Note that  $K_w$  is independent of transistor geometry in the subthreshold regime, but is dependent on the transistor geometry in the above-threshold regime. The parameter  $K_w(p)$  is an important parameter of MOS technology.

Another kind of noise in the transistor is called  $1/f$  noise because its power spectrum varies inversely with the frequency. It is widely believed that this form of noise arises from electrons in the channel going into and out of surface states, and into and out of impurities or defect traps in the gate oxide of the transistor. It is known that the mean-square  $1/f$  noise voltage at the gate input of the transistor scales inversely with the area of the transistor  $A = WL$ . The offset voltage of a transistor also scales inversely with the area of the transistor, because it is also caused primarily by impurities and traps in the gate oxide of the transistor. The inverse scaling with area is intuitive and relies on simple  $\sqrt{N}$  law-of-large-numbers arguments, as espoused in Appendix 5.9. The  $1/f$  noise is approximately independent of the current flowing through the transistor. The input-referred  $1/f$  noise of a transistor  $v_{nf}^2$  is given by

$$v_{nf}^2 = \frac{K_f}{A} \ln \left( \frac{f_h}{f_l} \right), \quad (5.6)$$

where  $K_f = B/C_{ox}$ . The parameter  $B$  is a measure of the number of surface states, impurities, and defects in the gate oxide.

Thus, we observe that the noise and offset (or 1/f noise) in an MOS transistor decrease with an expenditure of power and area resources in the transistor, respectively. The total input-referred noise is given by

$$v_n^2 = \frac{K_w(p)}{I^p} \Delta f + \frac{K_f}{A} \ln(f_h/f_l). \quad (5.7)$$

We call such an equation a *noise-resource equation* for the transistor. In any technology, each device will have its own noise-resource equation that illustrates how the noise in the device decreases with an increase in the resources consumed by the device. In this case, we consume the resource of power (current) to reduce thermal noise, and the resource of area to reduce 1/f noise (or offset).

### 5.3.2 Noise in Analog Systems

Figure 5.2 shows a cascade of  $M$  analog computational stages with an input  $V_{in}$  and output  $V_{out}$ . Each stage  $i$  has a certain number of devices  $n_i$ , has a gain  $g_i$ , consumes a current  $I_i$ , consumes an area  $A_i$ , and adds a certain amount of noise  $v_{ni}$ . The cascade is representative of many analog computations that involve distributed-gain amplification. In neurobiology, distributed-gain amplification occurs in the dendrites of neurons or in the traveling-wave-amplifier architecture of the cochlea.

The complexity of the computation sets a lower bound on the number of devices in each stage  $n_i$ , and on the total number of stages  $M$ . The ingenuity of the analog designer determines how close to the bound a realization of this system is. Depending on the details of the computation, the bound may be on  $M \times \Sigma n_i$ , on all the  $n_i$ , on  $n_1$  and  $M \times \Sigma n_i$ , and so on. We assume that the power-supply voltage  $V_{DD}$  is fixed and is less than or equal to the linear voltage range of the system, because otherwise power is unnecessarily wasted with no increase in output signal-to-noise ratio. So, we choose not to operate the system in this nonoptimal situation. We also make two simplifying assumptions. We assume that the current  $I_i$  and area  $A_i$  of stage  $i$  are divided equally among all the  $n_i$  devices in the stage. We also assume that each of the  $n_i$  devices contributes equally to the noise of the stage  $v_{ni}$ . In practice, the circuit topology of a stage determines the amount of current through

a device. The circuit topology also determines the noise contribution of that device to the noise of the stage. In spite of our simplifying assumptions, our model captures the general trend of the noise in each stage to increase with increasing  $n_i$ , and the noise at the output of the cascade to increase with increasing  $M$ .

The total mean-square noise at the output of the cascade,  $v_{no}^2$ , is made up of noise from each of the computational stages. The noise at the first stage is amplified by the cascaded gain of all the stages, whereas noise at the output of the  $i$ 'th stage is amplified by the cascaded gain of all stages from  $i$  to  $M$ . *Therefore, the early computational stages typically contribute more noise than do the later stages.* We define the noise gain from stage  $i$  to the output as  $G_i$ , with

$$G_i = \prod_{k=i}^{k=M} g_k. \quad (5.8)$$

Then from Eq. (5.7), the assumptions of the previous paragraph, and Figure 5.2 we have the total noise at the output given by

$$\begin{aligned} v_{no}^2 &= \sum_{i=1}^{i=M} v_{ni}^2 G_i^2 \\ &= \sum_{i=1}^{i=M} \left( n_i \frac{K_w(p)}{(I_i/n_i)^p} \Delta f + n_i \frac{K_f}{(A_i/n_i)} \ln(f_h/f_l) \right) G_i^2. \end{aligned} \quad (5.9)$$

The nature of the computational task determines the requirements on  $f_l$  and  $f_h$ . The bandwidth of the system,  $\Delta f = f_h - f_l$ , is the overall bandwidth of the system at the output. Any individual computational stage may have a bandwidth higher than this, but that is not the bandwidth that is relevant for noise calculations at the final output.

Suppose that we have a total amount of current  $I_T$ , or equivalently power  $P_T = V_{DD}I_T$ , at our disposal; suppose also that we have a total amount of area  $A_T$ . That is,

$$\begin{aligned} \sum_{i=1}^{i=M} I_i &= I_T, \\ \sum_{i=1}^{i=M} A_i &= A_T. \end{aligned} \quad (5.10)$$

We now ask how should we distribute our current and area resources among the various stages to minimize the output noise given by Eq. (5.9)? The answer to this question is a simple exercise in multivariable minimization through a Lagrange-multiplier technique. We

find that the currents  $I_i$  and areas  $A_i$  should be distributed such that

$$I_i = \frac{w_i I_T}{\sum w_i}, \quad (5.11)$$

$$w_i = G_i^{2/(1+p)} n_i, \quad (5.12)$$

$$A_i = \frac{z_i A_T}{\sum z_i}, \quad (5.13)$$

$$z_i = G_i n_i. \quad (5.14)$$

With the optimal allocation of resources, the total noise at the output is given by

$$v_{no}^2 = \frac{\left(\sum_{i=1}^M w_i\right)^{1+p} K_w(p) \Delta f}{I_T^p} + \frac{\left(\sum_{i=1}^M z_i\right)^2 K_f \ln(f_h/f_l)}{A_T}. \quad (5.15)$$

This equation is the noise–resource equation for our system. We find that the noise–resource equation for the device Eq. (5.7) and the noise–resource equation for the system Eq. (5.15) are very similar. The noise–resource equation for the device modeled the technology with the  $p$ ,  $K_w(p)$ , and  $K_f$  parameters. The noise–resource equation for the system added the effects of the complexity of the task and the ingenuity of the analog designer in the  $\sum w_i$  and  $\sum z_i$  terms. Both equations reveal that power and area resources lower thermal noise and 1/f noise (or offset) respectively. Further subtleties of noise in analog systems are discussed in Appendix 5.10.

*To first order, Eq. (5.15) quantitatively captures all the intuitive ideas about noise and offset that we expressed in items 4–7 of our analog-versus-digital table.* Eq. (5.15) reveals how noise accumulates in analog systems; if  $M$  and/or  $n_i$  are large, as would be the case for a complex computation, then the output noise can be large indeed. Eq. (5.15) also illustrates that if we are willing to compute slowly ( $\Delta f$  and  $f_h/f_l$  are both small), then we can keep the output noise low without consuming too much power or area. Thus, Eq. (5.15) also captures tradeoffs between maintaining low noise with few resources and maintaining bandwidth. Finally, Eqs. (5.12), (5.14) and (5.15) show that, if noise is to be minimized, more resources should be distributed to the parts of a system that affect all other parts of it (the initial stages) and to those parts of it that are complex (high  $n_i$ ). Note that, above threshold, the weighting of power resources towards the early stages is more severe than is that for subthreshold ( $G_i^{4/3}$  versus  $G_i$ ).

It is convenient to rewrite Eq. (5.15) as

$$v_{no}^2 = \frac{C_w}{P_T^p} + \frac{C_f}{A_T}, \quad (5.16)$$

where  $P_T = V_{DD}I_T$ . The parameter  $C_w$  is simply the numerator of the first term of Eq. (5.15) multiplied by  $V_{DD}^p$ , and the parameter  $C_f$  is the numerator of the second term of Eq. (5.15).

### 5.3.3 The Costs of Analog Precision

In an analog system, the maximum possible amplitude of an output sinusoidal signal  $Y$  is  $V_{DD}/2$ . The power of this signal is  $V_{DD}^2/8$ . For such a signal, the maximum possible signal-to-noise ratio is given by

$$S_N = \frac{V_{DD}^2}{8v_{no}^2}, \quad (5.17)$$

where  $v_{no}^2$  is the noise power at the output. The parameter  $S_N$  is important because the information  $H(Y)$  that we can observe at the output of our system is a monotonically increasing function of  $S_N$ . The larger the value of  $S_N$ , the more finely can we distinguish among states at the output, and the greater is the output precision. The exact form of the function depends on the amplitude distribution of the output signal, and on the amplitude distribution of the output noise. For many practical situations,  $H(Y) \approx (\log_2(1 + S_N))/2$  is a good approximation to the number of bits of information present at the output. The information at the output is an upper bound on the mutual information between the function of the input implemented by the computation and the output [15].

By using the expression for system-level noise from Eq. (5.16) in Eq. (5.17), and inverting the resulting equation to solve for  $P_T$  and  $A_T$  respectively, we get,

$$P_T = \left( \frac{C_w S_N}{V_{DD}^2/8 - (C_f/A) S_N} \right)^{\frac{1}{p}}, \quad (5.18)$$

$$A_T = \left( \frac{C_f S_N}{V_{DD}^2/8 - (C_w/P_T^p) S_N} \right). \quad (5.19)$$

We refer to these equations as the *resource-precision* equations for analog computation; they tell us how the resource utilization is a function of  $S_N$ , the variable that determines the output precision. For small values of  $S_N$ , the denominator is constant in both expressions



and  $P_T \propto S_N^{1/p}$ , while  $A_T \propto S_N$ . Since  $p = 1.0$  in the subthreshold regime, and  $p = 0.5$  in the above-threshold regime, the scaling laws of power versus  $S_N$  are  $P_T \propto S_N$  in the subthreshold regime, and  $P_T \propto S_N^2$  in above-threshold regime. The scaling laws for area,  $A \approx S_N$ , are similar in both regimes. The power cost  $P_T$  diverges when  $S_N$  is limited by 1/f noise (or offset); we must spend area in this situation to reduce 1/f noise (or offset). Similarly, the area cost  $A_T$  diverges when  $S_N$  is limited by thermal noise; we must spend power in this situation to reduce the thermal noise. Actually, these conclusions of divergence are true only for the subthreshold regime, where we cannot trade the power and area resources of a transistor to obtain a certain value of  $S_N$ . Appendix 5.10 shows how we can trade between power and area in the above-threshold regime.

### 5.3.4 The Costs of Digital Precision

In typical digital systems, the power and area costs are proportional to the number of bits  $b$  used in the computation. Thus, a 12-bit computation consumes one-half as much area and one-half as much power as does a 24-bit computation if all parameters—such as clock frequency  $f$ , average switching capacitance  $C$ , and power-supply voltage—remain fixed. If we do allow the clock frequency and power-supply voltage to scale with the number of bits, as in a bit-serial implementation, then the power costs scale as a polynomial function of the number of bits. Some computations like multiplication have power and area costs that scale like the square of the number of bits. In general, most tractable computations scale as a polynomial function of the number of bits. For simplicity, we assume that the power and area costs are proportional to the number of bits. It is straightforward to extend the arguments that follow to the polynomial-scaling case, although a quantitative solution may not be possible for any general polynomial. Thus, the resource–precision equations for digital computation are given by

$$P_T = L_p \log_2(1 + S_N), \quad (5.20)$$

$$A_T = L_a \log_2(1 + S_N), \quad (5.21)$$

where  $b$  is defined from the relationship  $b \approx (\log_2(1 + S_N))/2$ . The parameters  $L_p$  and  $L_a$  would depend on the task, technology and ingenuity of the digital designer. For example,  $L_a$  would scale like  $NWL$  where  $W$  and  $L$  are the widths and lengths of a small transistor,

and  $N$  represents the complexity of the task and the ingenuity of the digital designer. The parameter  $L_p$  would scale like  $NfCV_{DD}^2$ .

### 5.3.5 Precision Costs: Analog Versus Digital

Figure 5.3 shows power and area resource–precision curves for subthreshold analog computation (Eq. (5.18) and Eq. (5.19) with  $p = 1$ ) and for digital computation (Eq. (5.20) and Eq. (5.21)). We see that analog computation is cheaper than digital computation at low values of  $S_N$ , and is more expensive than digital computation at high values of  $S_N$ . Note also the divergence in power and area costs when  $S_N$  is limited by  $1/f$  noise (area) and thermal noise (power), respectively. The exact location of the crossover point will depend on the task, technology, and ingenuity of the analog and digital designers. We have chosen values for  $C_w$ ,  $C_f$ ,  $L_p$ , and  $L_a$  such that the crossover happens near 10 bits (60 dB in  $S_N$ ). For many common computations in today’s CMOS technology, the crossover happens near 8 bits.

Curves such as the ones in Figure 5.3 were first proposed for comparisons of delay operations in a seminal paper [16]. Recently, there has been additional work on comparing analog and digital systems for delay operations [17]. The work of [18] compared filtering operations in analog versus digital systems. The work of [19] compared analog and digital systems for their performance on the tasks of comparing two  $N$ -bit numbers, and also for the construction of delay lines. To our knowledge, the comparison presented in this paper is the first comparison to generalize the prior results to a broad class of analog and digital systems, and to include the effects of  $1/f$  noise and offset along with the effects of thermal noise.

### 5.3.6 A Clarification

It is worth making a clarification: A/Ds and D/As are analog systems and the costs of operating these systems at high precision (high  $S_N$ ) are high. In a digital system that does a lot of high-precision processing, the precision costs of the A/D and D/A are paid once at the front end and once at the back end, respectively. The cost of the high-precision processing between the front end and back end is determined by the digital system in between. Thus, the total cost of the overall system is made up of an analog part for the A/D and D/A, and a digital part for the rest of the processing. Our comparisons between analog and digital

computation ignored the additional A/D and D/A costs of a digital system. In a sufficiently complex computation, the A/Ds and D/As represent a small fraction of the total cost of the computation. In an analog system doing the same high-precision processing, the high-precision analog costs are paid throughout all parts of the system, rather than only at the front end and back end; that is why, for a sufficiently complex task, a digital system with an A/D and D/A would still be more efficient than an analog system.

### 5.3.7 The Meaning of the Quantitative Analysis

The analog constants  $C_w$  and  $C_f$  and the digital constants  $L_p$  and  $L_a$  are such that the analog curves lie below the digital curves at low  $S_N$ . The basic reason for this behavior is that physical primitives are more efficient at computing than are logical primitives as long as we do not attempt to compute with low noise on one wire. At high  $S_N$ , however, the multiwire representation of information by digital systems divides the information processing into independent bit parts that many simple processing stages can collectively handle more efficiently than can one precise single-wire analog processing stage. This intuition is mathematically expressed by a logarithmic scaling of digital computation with  $S_N$ , and a power-law-like scaling of analog computation with  $S_N$ . Furthermore, the lack of signal restoration in analog systems causes the noise accumulation for complex analog systems to be much more severe than that for complex digital systems. Thus, we have large values of  $C_w$  and  $C_f$  for complex analog computations (large  $M$ ,  $w_i$ , or  $z_i$  in Eq. (5.15)), whereas  $L_p$  and  $L_a$  remain of reasonable size for the equivalent complex digital computation.

## 5.4 The Best of Both Worlds

It is attractive to combine the best of both computing paradigms to make a hybrid paradigm that is better than either one. In this section, we suggest a framework for such a paradigm: In Section 5.4.1 we show that analog computation that distributes its precision and processing resources over many wires is maximally efficient at a certain signal-to-noise ratio per wire. In Section 5.4.2, we propose a hybrid architecture that combines the advantages of discrete-signal restoration with the advantages of continuous-signal continuous-time analog computation. In Section 5.4.3 we describe a computing architecture that illustrates the simultaneous workings of distributed and hybrid computation.

### 5.4.1 Distributed Analog Computation

Figure 5.4(a) shows an example that illustrates the idea behind distributed analog computation. Instead of the usual analog paradigm that represents 8 bits of information on one wire, or the usual digital paradigm that represents 8 bits of information on 8 wires, in distributed analog computation, we represent 8 bits of information on two wires that carry analog signals. Also, instead of one analog processor maintaining 8 bits of precision on its output wire, we now have two processors that interact with each other, and that maintain 4 bits of precision on their respective output wires. The analog signals each have a signal-to-noise ratio of 24 dB in order to encode 4 bits of information. Note that the information encoded on the pair of wires does not necessarily represent the amplitude information for some other 8-bit signal. For example, two wires carrying outputs from a cochlea represent information in two different frequency bands of the sound input. In this example, we have assumed that the two wires carry 4 independent bits of information each, such that the pair of wires encodes 8 bits of information. In general, there may be correlations between the information carried by two wires.

Because each analog processor operates at a low precision, its power-consumption and area-consumption requirements are low. We are interested in knowing whether the total costs in power consumption and area consumption are lower for two 4-bit processors than for one 8-bit processor. We therefore ask the following question. Suppose we want to output  $N$  bits of information by outputting  $b$  bits of information from  $N/b$  analog processors on  $N/b$  wires. What is the optimal number of bits  $b$  on each wire such that the total power or area consumption of all circuitry is minimized? In general, because there are correlations in the information amongst wires or because we intentionally want redundancy (to provide insurance against transmission noise, or to simplify the computation in subsequent stages) we shall assume that there is also a redundancy factor  $R > 1$ . Thus, we have  $RN/b$  processors and  $RN/b$  wires, instead of  $N/b$  processors and  $N/b$  wires.

To answer the question posed in the previous paragraph, we will have to take the costs of wiring (communication) and computation into account. Wires cost area and add capacitance. In order to keep the bandwidth of the system constant as capacitance is added, the power consumption in the system rises. The wiring costs for area increase in

linear proportion to the number of wires.<sup>4</sup> If bandwidth is to be maintained, the power consumption must rise in linear proportion to the total capacitance in the analog processor. Thus, the power costs of wiring also increase in linear proportion to the number of wires. In neurobiological systems, the power costs of wiring include the costs of active restoring circuitry in axons as well. Thus, wiring costs are a function of the technology.

From Eq. (5.18) and Eq. (5.19), for relatively small  $S_N$  where analog computation is more effective than digital computation, the power consumption and area consumption are power-law functions of  $S_N$  in the subthreshold and above-threshold regimes. Thus, the analog cost function for computation per processor is well described by  $cS_N^l$ , where  $l = 2$  for above-threshold power consumption, and  $l = 1$  in all other cases of interest; here,  $c$  is a computation-cost constant. We will discuss only the case for  $l = 1$  since the  $l = 2$  case follows by straightforward extension. The cost function for wiring is given by a constant cost of  $w$  per wire. The number of bits per wire  $b = (\log_2(1 + S_N)) / 2$ . Thus the total cost function for computation and communication is given by

$$\begin{aligned} \text{Cost} &= (cS_N + w) \left( \frac{RN}{b} \right) \\ &= (cS_N + w) \left( \frac{RN}{0.5(\log_2(1 + S_N))} \right). \end{aligned} \quad (5.22)$$

Figure 5.4(b) shows plots of the total cost of computation and communication as a function of  $S_N$  in each wire, for  $c = 1$ , and for various  $w/c$  ratios. We see that, when wiring is expensive ( $w/c = 10$ ), the optimal signal-to-noise ratio is high,  $b$  is high, and we have few wires. When wiring is cheap ( $w/c = 0.1$ ), the optimal signal-to-noise ratio is low,  $b$  is low, and we have many wires.

By simple calculus, we can show that the optimal  $S_N$  occurs when

$$\ln(1 + S_N) = \left( \frac{S_N + w/c}{1 + S_N} \right). \quad (5.23)$$

---

<sup>4</sup>The linear proportionality of area cost with the number of wires accounts for only the area occupied by the wires themselves. In practice, area costs for wiring will involve the area between wires, and the area between computational elements as well. Such considerations cause the area cost function to be supralinear in the number of wires. For simplicity, we assume a linear function as the supralinear case will not alter the basic nature of our conclusions.

The optimal value  $S_N^o$  has the following limiting solutions:

$$S_N^o = \sqrt{w/c} \text{ if } w/c \ll 1, \quad (5.24)$$

$$S_N^o \ln S_N^o = w/c \text{ if } w/c \gg 1. \quad (5.25)$$

At the optimal value, the total cost of computation and communication is  $2NRc \ln 2(1+S_N)$ . For the case where  $w/c \ll 1$ , the cost is  $2NRc \ln 2$ . The cost of outputting all  $N$  bits from one single analog processor is  $c2^N$ . Thus, if  $N$  is sufficiently big,  $2NRc \ln 2 \ll c2^N$  even if  $R$  is large. Therefore, even in cases where there is a lot of redundancy, if the amount of output information is large, it is better to distribute the information and information processing on many wires.

## 5.4.2 Hybrid Computation

Noise always accumulates in a cascade of analog processing stages. If a computation is sufficiently complex, then at some point, an analog system simply cannot maintain enough precision at its output to do anything useful. Even if we require the system to maintain only 1 bit at its output it will be unable to do so. We now show how to use a building block called the A/D/A, and an architecture that uses A/D/As for solving the noise accumulation problem in analog systems. The A/D/A is an A/D converter that is immediately followed by a D/A converter. However, its most efficient circuit implementation does not involve explicit implementation of an A/D converter and a D/A converter. The A/D/A has been proposed as a useful building block for various analog and digital storage and processing applications [20].

The basic ideas are illustrated in Figure 5.5. A *hybrid link* is a set of analog processing stages (denoted  $A_i$  in the figure) followed by an A/D/A that restores the analog signal to one of  $M$  discrete attractor states. A *hybrid chain* is composed of a sequence of hybrid links. Each chain can maintain analog information to a precision of  $\log_2(M)$  bits with a low probability of error, provided that we meet the following constraint: *The net input-referred noise of the A/D/A, due to all processing stages in a link and the restoration circuits in the A/D/A, must be significantly lower than the minimum distance between attractor states.* In Section 5.4.2, we show that an error probability of  $10^{-4}$  can be achieved in a hybrid link if the input-referred noise has a precision of about  $N + 3$  bits. To keep the error probability

low in a hybrid chain composed of many links, the requisite precision before restoration only needs to grow very slowly with the number of links in the chain (like the  $\log(\log(\text{size of the chain}))$ ).

Thus, a hybrid chain can do an extremely large amount of analog processing, and still maintain a precision of  $\log_2(M)$  bits at its output. Effectively, we can operate with the precision and complexity characteristic of digital systems, while doing efficient analog processing. If we assume that we do not want to have to maintain more than 8 bits of precision at the input to the A/D/A, then the best A/D/A that we can build would restore a signal to 5 bits of precision. However, such a A/D/A would require too much circuitry. Using A/D/As is probably not a good technique for maintaining anything more than 3 to 4 bits of precision on an analog input. As we shall discuss in Section 5.4.3, the main use for A/D/As is in distributed analog computation, where it is unnecessary to maintain too much precision on one wire.

To maximize the efficiency of information processing in a hybrid chain, there is an optimal amount of analog processing that must occur before signal restoration in a hybrid link; that is, hybrid links should not be too long or short. If the link is too long, we expend too much power (and/or area) in each analog stage to maintain the requisite precision at the input of the A/D/A. If the link is too short, we expend too much power (and/or area) in frequent signal restorations. In Section 5.4.2, we analyze the optimal length of a hybrid link quantitatively. Needless to say, if we are unconcerned about efficiency, then the link can be as long or as short as we like, as long as we meet the A/D/A constraint.

### The A/D/A

To restore a signal, we must have discrete attractor states. In digital signal restoration, the input signal is compared with a threshold, and high-gain circuits restore the output to an attractor state that is a function of the input attractor state. The input may deviate by a fairly large amount from its attractor state, and the output will still be very close to its attractor state. The noise immunity of digital circuits arises because the typical distance in voltage space between an input attractor-state level and a threshold level is many times the variance of the noise or the offset in the circuit. We can generalize this two-state restoration to an  $M$ -state restoration by having  $M - 1$  input threshold levels and  $M$  output-state levels. The input signal is compared with  $M - 1$  threshold levels and is

rounded off to that attractor-state level that it is closest to. Systems like these have been proposed for multistate logic systems. Figure 5.6(a) shows the threshold levels  $V_{Ti}$  and restoration levels  $V_{Li}$  for a four-state or two-bit system. The arrows converge on restoration levels and diverge from threshold levels.

The A/D/A modifies the digital-restoration scheme for  $M$  states to an analog-restoration scheme for  $M$  states. In the analog-restoration scheme,  $M$  can be arbitrary and does not have to be 1, 2, 4, 8, 16, 32, and so on. It can be any arbitrary number that we choose because, *unlike multistate logic, we do not do any digital computation with our inputs or outputs*. The input  $V_{in}$  is an analog signal that may have been processed by many analog stages. The output  $V_{out}$  is a restored and filtered analog signal that can serve as an input to future analog-processing stages. Figure 5.6(b) shows a circuit for one possible implementation of a 4-state A/D/A.<sup>5</sup> The analog signal is compared with three thresholds, and 0, 1, 2, or 3 currents are switched onto a resistor, whose voltage then equilibrates at  $V_{L1}$ ,  $V_{L1} + IR$ ,  $V_{L1} + 2IR$ , or  $V_{L1} + 3IR$  respectively. The RC circuit acts as a filter and removes sharp edges in the signal. The capacitance is chosen such that  $1/RC$  is at or near the desired bandwidth of the input. Figure 5.6(a) shows that, if an input analog signal happens to be exactly at a threshold level  $V_{Ti}$ , then it will be constantly restored at random to the attractor state above or below it. However, since we are always within half a bit of the analog input, this random restoration still preserves the input information to within one bit, as desired. All other analog inputs are restored to within half bit of their input values as well. Thus, we preserve information in the analog signal to a precision of  $\log_2 M$  bits like an A/D followed by a D/A of  $\log_2 M$  bits. Interestingly, an explicit A/D/A approach has been proposed for use in various applications [20].

Now we analyze how large the input noise and offset of the A/D/A can be if we need to preserve a precision of  $\log_2 M$  bits in the output analog signal. Suppose that, because of noise and offsets, the input signal is described by a Gaussian probability distribution with variance  $\sigma^2$ , as shown in Figure 5.6(c). If the analog input is situated at a threshold level  $V_{Ti}$ , then it needs to deviate by a full 1-bit distance from this level for a bit error to occur. If, on the other hand, the analog input is situated at a restoring level  $V_{Li}$  that is not at the extremes such as  $V_{L1}$  or  $V_{L4}$ , but rather is midway such as  $V_{L1}$  and  $V_{L2}$ , then a deviation

---

<sup>5</sup>There are vastly more efficient circuit representations that we can use to construct a A/D/A. However, we do not discuss these here because they are of a more technical nature, and would require that the reader have a background in analog circuit design.



from this level by half-bit distance is sufficient for a bit error to occur. Thus, we analyze this worst-case situation for the input situated at  $V_{L2}$ .

Let the variance of the noise be  $\sigma^2$ . The distance between a threshold level and a restoration level is  $b_d/2$ , where  $b_d$  is a bit distance given by  $(V_{LM} - V_{L1})/(M - 1)$  in an  $M$ -state A/D/A. The probability of a bit error  $P_e$  is then given by the area under the Gaussian tails in Figure 5.6(c); that is, to the left of  $V_{T1}$  and to the right of  $V_{T2}$ . Thus,  $P_e$  is given by

$$P_e = \operatorname{erfc}\left(\frac{b_d/2}{\sigma\sqrt{2}}\right), \quad (5.26)$$

where  $\operatorname{erfc}(x)$  is defined by

$$\operatorname{erfc}(x) = \frac{2}{\sqrt{\pi}} \int_x^\infty e^{-u^2} du \approx \frac{e^{-x^2}}{\sqrt{\pi}x}. \quad (5.27)$$

Now  $P_e = 1 \times 10^{-4}$  if  $b_d/(2\sigma\sqrt{2}) = 2.75$ . Thus,  $b_d = 2\sqrt{2} \times 2.75\sigma = 7.77\sigma$ .

Hence, to restore the signal faithfully, with a low bit-error rate, an  $N$ -bit A/D/A requires that the precision at its input be  $\approx N + 3$  bits ( $\log_2(7.77) \approx 3$ ).

### The Optimal Length of a Hybrid Link

For simplicity, assume that our computation is a cascade of  $N$  identical analog processing stages, as in a many-pole filter. By the reasoning of the third paragraph of Section 5.4.2, if the stages are not identical, we can show that an optimal length still exists. However, the closed-form solution is hard to obtain. Thus, we shall discuss only the case with identical stages to avoid complexity that does not add much insight. For similar reasons, we shall analyze only the simple case of current (power) optimization assuming that the  $1/f$  (or offset) terms in the resource-noise Eq. (5.7) are negligible. Other simplifying assumptions also include that  $p = 1$  (subthreshold), and that we pay a fixed cost in power per A/D/A restoration stage<sup>6</sup>.

Suppose that there are  $M$  computational stages and 1 A/D/A in every hybrid link. Then, there will be  $N/M$  links with a total of  $N$  computational stages, and  $N/M$  A/D/As in the chain. Suppose that the complexities of the A/D/A stage and of each computational stage correspond to  $n_r$  and  $n_c$  devices respectively. By Eq. (5.26), corresponding to whatever

<sup>6</sup>There is a possible variant of the problem, where we simultaneously optimize the power allocated between the A/D/A stages and the computation stages, as well as the number of stages per link.

error criterion we pick, the input-referred noise  $\sigma$  at every A/D/A must be less than or equal to some value  $\sigma_t$ . The value of  $\sigma_t$  depends on only  $b_d$ , the distance between attractor states in the A/D/A, which is fixed by the precision desired for a given hybrid chain.

Thus from Eq. (5.15), Eq. (5.12), and Eq. (5.14), with  $n_i = n_c$  for all  $i$ , and  $G_i = G$  for all  $i$ , the noise due to the computational stages in a link is given by

$$v_c^2 = \frac{(MGn_c)^2 K_w(1) \Delta f}{I_C}, \quad (5.28)$$

where  $I_C$  is the total power consumption in the computational stages. Similarly, the noise due to a A/D/A stage in a link is given by

$$v_r^2 = \frac{(n_r)^2 K_w(1) \Delta f}{I_R}, \quad (5.29)$$

where  $I_R$  is the fixed current consumption of the restoration stage. The A/D/A constraint gives us

$$v_c^2 + v_r^2 = \sigma_t^2. \quad (5.30)$$

Algebraic manipulation of Eq. (5.28), Eq. (5.29), and Eq. (5.30) then yields

$$I_C = M^2 \left( \frac{G^2 n_c^2 K_w(1) \Delta f}{\sigma_t^2 - \frac{n_r^2 K_w(1) \Delta f}{I_R}} \right), \quad (5.31)$$

$$= M^2 C_c, \quad (5.32)$$

where  $C_c$  is defined by the preceding equations. The total current consumption due to  $N/M$  links in the entire chain is then given by,

$$\begin{aligned} I_{CH} &= \left( \frac{N}{M} \right) (I_C + I_R), \\ &= N \left( C_c M + \frac{I_R}{M} \right). \end{aligned} \quad (5.33)$$

Figure 5.7 shows a plot of the current consumption for differing values of  $C_c = 2.06$  pA, 5.11 pA, 9.52 pA, and 15.34 pA;  $I_R$  is fixed at 100 pA. The parameter  $C_c$  was changed by varying  $\sigma_t$  in Eq. (5.31). Thus, as we increase the precision of the hybrid link, the costs of computation rise with respect to the costs of signal restoration, and the optimal length of the link decreases. The mathematics is in accord with the intuition expressed in the third

paragraph of Section 5.4.2. The curves in Figure 5.7 were drawn for  $G = 1$ ,  $\Delta f = 100$  Hz,  $K_w(1) = 4.38 \times 10^{-22}$ ,  $n_r = 3$ , and  $n_c = 150$ . It is easy to show that the location of the optimum in Eq. (5.33) is given by

$$M = \sqrt{\frac{I_R}{C_c}}. \quad (5.34)$$

### 5.4.3 Distributed and Hybrid Computation

Figure 5.8 combines the ideas of Sections 5.4.1 and section 5.4.2. The information from a single-wire analog input is encoded onto many wires by an analog encoder. Typically, the encoder might be more redundant and thus might distribute the information over many more wires, but for simplicity, we have shown a nonredundant encoder. A cochlea, retina, and A/D are all good examples of encoders that distribute information from one wire onto many wires. In this example, we have an analog encoder, so if we used an A/D, we would have to follow it with a D/A. Encoding is a computation with costs. In many cases, these costs can be paid once, right at the frontend, and never paid again, as long as the information is always distributed. In the example of Figure 5.8, the distributed information is preserved in the first stage of processing by 2-bit A/D/As. In the next stage of processing, the analog processors and/or the A/D/As make decisions based on the information and reduce the output information to 1 bit. Thus, the analog circuits in the second half can afford to be noisier, since the A/D/A restoration has a precision of only one bit. The use of distributed analog computation and low-precision A/D/A signal restoration makes this architecture ideal for efficient precise computation.

## 5.5 Extrapolating to Neurobiology

Our analysis for electronic systems suggests

1. Why neuronal information processing is distributed.
2. That information processing in the brain is hybrid.
3. How signal restoration in neurons **may** be implemented.

In Sections 5.5.1 through 5.5.3 we shall discuss these suggestions in more detail. In Sections 5.5.4 through 5.5.5 we shall discuss how our arguments about noise in electronic systems can be extrapolated to neurobiology.

### 5.5.1 Why Neuronal Information Processing is Distributed

Information processing in networks of neurons is accomplished in a tremendously distributed fashion. It has often been pointed out that this distribution results in fault-tolerant behavior, since the destruction of any one neuron or synapse hardly affects the operation of the overall network. However, we suggest that the primary reason for the distributed nature of neuronal information processing is not fault tolerance, but rather is efficiency. We showed, in Section 5.4.1, that the costs of computation force information to be as distributed as possible across many information-processing resources and many wires. However, the costs of communication force the information-processing and information to be as localized as possible. The tradeoff between these two constraints, as revealed in Eq. (5.22), results in an optimal signal-to-noise ratio per wire, as revealed in Figure 5.4. In neurobiological systems, where communication costs are relatively low compared with communication costs in silicon, the optimal signal-to-noise ratio is lower than that in silicon.<sup>7</sup> Thus, we believe that nature was smart to distribute her computational resources over many noisy neurons (dendrites and somas), and communicate that information between neurons over many noisy fibers (axons). The noisiness of the brain is due to the wisdom of millions of years of evolution, and is not a reflection of the incompetence of biology. We believe that the “use” of neuronal noise in phenomena such as stochastic resonance, or in phenomena that prevent trapping in a local minima, may be valuable in certain special cases, but the primary reason for the noisy nature of the brain is efficiency.

### 5.5.2 Information Processing in the Brain is Hybrid

Action potentials are all-or-none discrete events that usually occur at or near the soma or axon hillock. In contrast, dendritic processing usually involves graded synaptic computation, and graded nonlinear spatiotemporal processing. The inputs to the dendrites are caused by discrete events. Thus, in neuronal information processing, there is a constant alternation between spiking and nonspiking representations of information. This alternation is reminiscent of the constant alternation between discrete and continuous representations of information in Figure 5.5. Thus, it is tempting to view a single neuron as a “D/A/D”.

---

<sup>7</sup>In today’s electronic technology, it would be unthinkable to even dream of wiring on the scale of neurobiology. For example, the million fibers of the optic nerve, or the 35,000 fibers of the auditory nerve would simply be too expensive to implement.

However, although the firing of a spike is a discrete event it does not imply that it encodes information about a discrete state. The information encoded by a spike is meaningful only in relation to spikes in different neurons, or in relation to earlier or later spikes in the same neuron. If these relationships are analog, then all-or-none events do not imply the encoding of discrete states. So how do we know whether the brain is analog (continuous-signal) or digital (discrete-signal) or hybrid (both)? Almost everybody accepts that the brain does a tremendous amount of analog processing. The controversy lies in whether there is anything digital about it.

We know, from the arguments of this paper, that the noise accumulation in complex systems is simply too high for purely analog processing to be efficient in such systems. Given that the brain is made up of a large number of physical devices that exhibit noise at room temperature, and is yet extremely efficient (12W power consumption and 300ms response time for complex tasks), we may hypothesize that it must be mixing continuous-signal and discrete-signal processing to compute in a hybrid fashion. In Section 5.5.4 we review noise in biological devices, and in Section 5.6.1 we review numbers on the interconnectivity and complexity of the brain's architecture. These reviews suggest that, although it is theoretically possible that the brain's complexity is small enough that a purely analog brain could be efficient, a purely analog brain seems unlikely. However, more quantitative studies need to be done on noise in biological devices and on the architecture of the brain before we can conclusively rule out the possibility of a purely analog brain. Thus, at the present time, our suggestion that the brain is hybrid is only a hypothesis supported by our quantitative arguments from electronics, and by some qualitative facts from our current knowledge of neurobiology.

Experimental evidence and theoretical work suggest that discrete states are encoded in the crosscorrelated firing patterns of neurons in a network [22], [23]. We already know that the brain's information processing is tremendously distributed. We have shown how distributed and hybrid systems combine the best of the continuous and discrete worlds to create a world that is more efficient than either. Thus, we suggest that a major reason for the tremendous efficiency of the brain is that its architecture is not only distributed but also hybrid. We explore other reasons for the efficiency of the brain in Section 5.6.

### 5.5.3 How Signal Restoration May be Implemented

To implement signal restoration there must be a set of discrete states that the continuous signal is periodically restored to. How are the discrete restorative states of neurons encoded in the firing of action potentials? Conceptually, at the level of a single neuron, the discrete states of a spike train may be encoded in the number of spikes that occur in a given window of time (the mean-firing-rate code), or in a discrete set of firing patterns that occur within that same window of time (the timing-pattern code). Such codes are scalar codes since they involve only one neuron. As experimental [22] and theoretical [23] work indicate, it is more likely that discrete states involve a vector code that is implemented in a collective fashion across many neurons. The window of time over which we count spikes or detect temporal patterns within the spikes is determined by the integration time constants of the neurons.

The mean-firing-rate and timing-pattern scalar codes have direct analogies in vector codes: In the mean-firing-rate case, instead of counting the number of spikes in one neuron within a window of time, we count the number of spikes across many neurons that are present within some time window. In the timing-pattern case, instead of a discrete set of firing patterns of one neuron that occur within some time window, we have a discrete set of crosscorrelated firing patterns of many neurons within some time window. For simplicity, we shall assume that our time window is short enough such that each neuron contributes at most one spike within that time window. It is easy to generalize our ideas to multiple spikes within one time window.

The key building block of our electronic signal-restoration schemes was the A/D/A, which was basically an A/D followed by a D/A. In the signal-representation scheme of neurons how might we build a A/D/A? We shall only discuss signal-restoration for vector codes.

#### VonNeumann Restoration for Spike Counting

Suppose we have  $3N$  neurons. We group them into  $N$  sets of 3 each. For each of the  $N$  sets we perform a simple majority vote, and regenerate 3 signals, each of which encodes the result of the majority vote. Thus, if we have (spike, spike, no spike) across the three neurons, we restore this signal to (spike, spike, spike). If we have (no spike, spike, no spike) across the three neurons, then we restore this signal to (no spike, no spike, no spike). Thus,

we restore the original  $3N + 1$  possible states (ordering of neurons does not matter) into  $N + 1$  possible states. Just as in the A/D/A, if we want to have low rates of error, we must compute with more redundancy ( $20N$  instead of  $3N$ ). The majority-vote scheme was first proposed by John Von Neumann [13] as a way for doing signal restoration. Note that, in this scheme we are really restoring a fine-grained discrete quantity to a coarse-grained discrete quantity. In the A/D/A, we restore a continuous analog quantity with a fine-grain size determined by analog noise into a coarse-grained discrete quantity.

### Restoration for Spike Timing

Here, we detect the presence of a discrete timing pattern by building suitable delays in the dendrites or synapses or input axons of a “matched-filter” neuron such that the inputs from the  $N$  neurons that encode the timing pattern arrive in synchrony at the axon hillock [24]. The matched-filter neuron regenerates the timing pattern by fanning out collaterals to a set of  $N$  output neurons with appropriate axonal or synaptic delays such that the timing pattern is regenerated. The restoration in pattern timing will occur if the matched-filter neuron is configured to respond to inputs with somewhat-skewed timing patterns; this is accomplished by setting its threshold to not be too high. If we want to restore  $M$  timing patterns that are encoded on  $N$  input axons, then we need  $M$  matched-filter neurons and  $N$  output neurons. Each of the  $N$  output neurons could receive inputs in parallel from the  $M$  matched-filter neurons, as, in a good design, only one of the  $M$  matched-filter neurons would be active at any given time. As in the A/D/A, if we want to ensure low error rates,  $M$  should be significantly less than the possible number of timing patterns encoded amongst the  $N$  neurons. It is also crucial that the delays involved in regeneration be precise enough to maintain a precision that is a few bits above  $\log_2(M)$  bits.

In digital electronic circuits, an inverter performs restoration and computation at the same time: It inverts its input (1 goes to 0, and 0 goes to 1), but it is also restorative since a “bad 1” is restored to a “good 0”. Similarly, in a time-delay restoration scheme we could have the regenerated pattern be a different timing pattern such that a somewhat-skewed input temporal pattern is restored to a clean temporal pattern. In a pattern-recognition computation, such as that performed by an associative memory, computation and restoration are intermingled because the nature of the computation inherently requires a discrete set of outputs.

## Caveats

We have made many simplifying assumptions such as treating computation and restoration as distinct entities, and similarly treating computation and communication as separate entities. It is likely that such entities are more deeply intertwined in the brain. It is likely that the rather sharp digital restorations that we propose are really soft restorations in the brain, such that a more accurate description would need to involve the language of complex nonlinear dynamical systems. The processing of information in a single dendrite, let alone the whole brain is enormously complex. It is possible the tree-like structure and nonlinear processing of dendrites enables them to perform classification of an exponentially large number of input combinations with linear resources in dendritic area [32]. Such processing could be enormously useful in performing signal restoration within the level of the dendrite itself.

*Thus, we do not, by any means, claim that the brain is implementing the particular architectures, and the particular restorative schemes that we have proposed. We have merely offered our schemes as a possible way in the hopes that it will stimulate further discussion and work on the subject. However, in spite of our simplifications, we suggest that the brain is hybrid in nature. We propose that the hybrid-and-distributed architecture of the brain is one of the major reasons for its efficiency, and that the importance of this point has generally been underappreciated.*

### 5.5.4 Noise in Biological Devices

In any technology, the starting point for an analysis of the information costs of computing is the noise–resource equation of that technology. It was the noise–resource equation for MOS technology (Eq. (5.7)) that enabled us to construct a set of resource–precision equations (Eq. (5.18) and Eq. (5.19)). The resource–precision equations evaluated the costs of a computation as a function of the output information or precision. What might the noise–resource equations for neurobiological devices look like? Due to the great diversity of biological devices, and the incomplete knowledge that we have about their functioning, a quantitative theory for the technology of neurobiology seems premature. However, we can make qualitative statements that reveal how the noise can be decreased with an increase in resource consumption.



The limiting form of noise in biological devices are typically the randomness in ion channel openings and closings [27], and the unreliability of synaptic vesicle release [28]. Channels transition between discrete closed and open states with certain finite probabilities per unit time. The transition probabilities depend on the membrane voltage or on the chemical concentration of a substance. For a good discussion of the kinetics of ion channels, see [29]. The noise can be reduced by  $\sqrt{N}$  law-of-large-numbers averaging over several ionic channels, (i.e., through the increase of ion channel densities). Similarly, the noise of synaptic transmission may be reduced through the use of averaging over many vesicles, many synaptic contacts and so on. Such averaging costs area, and also turns up power consumption, since the power per unit channel, vesicle, or contact is approximately constant. It is intuitive to expect that averaging over large areas of membrane would improve offsets and  $1/f$  noise, but we are unaware of any actual experimental measurements that address whether they do. Interestingly, as in electronics, the magnitude of the  $1/f$  noise in biology is highly unpredictable. It is dependent on the concentrations in the cellular environment of substances that alter transport properties of nerve membrane [27]. In electronics,  $1/f$  noise is also strongly dependent on the concentrations of impurities in an insulating membrane, the gate oxide.

Averaging strategies were at the root of a reduction in noise in electronic systems as well. In electronics, we averaged over more electrons per unit time (to reduce thermal noise by increasing power), or over more traps and impurity defects (to reduce  $1/f$  noise and offset by increasing area). In biology, we average over more ion channels or over larger stretches of membrane. Indeed, a simple  $\sqrt{N}$  averaging would yield noise-resource equations that are similar to Eq. (5.7), with  $p = 1$ . However, there are suggestions that neurobiological systems may be even smarter, and may attain noise reductions that scale like  $1/N$  rather than like  $1/\sqrt{N}$  [30]; such scaling laws require the use of interactions between channel kinetics and membrane kinetics through the use of membrane-voltage feedback.

In situations where it is important to maintain reliability and precision, such as at a neuromuscular junction, there is a lot of averaging over numerous synaptic connections and/or synaptic vesicles. In situations where it is not that important to be very reliable, such as in the highly distributed architecture of cortex, there is little averaging over synapses or vesicles [25]. When timing must be precise, synapses are typically large [26]. From numerous examples, it is qualitatively clear that the reduction of noise is accomplished through

resource consumption in neurobiology, as it is in electronics. *Neurobiology and electronics behave similarly because physical and mathematical laws like the laws of thermodynamics and the law of large numbers do not change with technologies.* It is such laws that, along with a few technology-dependent parameters, determine noise–resource equations. Since our conclusions depend on only general properties of noise–resource equations, such as a polynomial reduction in noise with resource consumption, we suggest that our extrapolation from electronics to neurobiology is correct to leading order.

### 5.5.5 Noise in Neurobiological Systems

In Section 5.3.2, we abstracted the mapping from computational task to circuit topology in the parameters  $M$ ,  $n_i$ . We stated that the exact mapping would depend on the task, technology, and ingenuity of the designer. The ingenuity of the designer lies in mapping the task to the primitives and architecture of the technology, so that  $M$  and/or  $n_i$  are as small as possible. Consequently, when function is well mapped to structure, noise is minimized; the wiring of the architecture also is more efficient. Computational architectures where function and structure are well matched amplify the computational information above the noise in the components. This amplification is analogous to the way a matched filter amplifies the signal above the background noise.

Two topologies that may be completely equivalent functionally may have markedly different noise properties: For example, suppose that in topology A we take the difference between a large positive current and a large negative current to output a small differential current; in topology B we just output a small differential current. The noise of topology A will be much higher than that of topology B even though the two topologies may be indistinguishable as far as outputs go. Thus, the mapping from function to structure must be done with care.

It is clear that natural structures have evolved to match structure and function. The architectures of the cochlea, the retina, the hippocampus, the cerebellum, the neocortex and various other regions have patterns of connectivity, cellular organization, and cell differentiation that indicate a close relationship between structure and function. Cells of various anatomical types are specialized to have certain functional characteristics. For a good review see [31].

For noise minimization, resource allocation should be increased in the initial and complex

stages of a computation, as discussed in Sections 5.3.2.

## 5.6 Other Reasons for the Brain's Efficiency

In this paper, we have emphasized that the hybrid and distributed nature of the brain's signal processing is important for its efficiency. Now we shall list all the reasons that contribute to the brain's efficiency. We shall group them under the three categories of technology, signal processing, and computational strategies.

### 5.6.1 Technology

The brain has an awesome technology. It is composed of at least 50–100 kinds of one-terminal ion-channel elements, and 100–200 two-terminal synaptic elements. The synaptic elements are made out of varying combinations of neurotransmitter, receptor, and postsynaptic ion channel(s). The most common ion channels are the delayed-rectifier potassium, inactivating sodium, calcium, and chloride channels. The most common neurotransmitters are glutamate, with excitatory effects on NMDA and non-NMDA receptors, and GABA, with inhibitory effects on  $GABA_A$  and  $GABA_B$  receptors. In addition, every neuron is capable of elaborate spatiotemporal processing, due to the distributed resistances and capacitances in dendritic cables. The treelike structure and nonlinear processing of dendrites may allow for pattern classification of an exponential number of input combinations with linear resources in dendritic area [32]. The power supply is regenerated locally through the action of ion pumps, and thus noise accumulation via a global power supply is avoided. The technology is a symbiotic mix of chemistry and electronics allowing ion channels to be made as needed, power supply distribution to be adapted as needed (mitochondrial expression), and extensive wiring and synaptic modification to take place. The molecular specificity of chemistry is exploited such that many information channels can coexist in the same space, analogous to the way that radio stations with different broadcast frequencies share the same airspace. The technology is impressive in terms of its miniaturization and connectivity as well [25]. An ion pore is a few Å; the nerve membrane is about 50 Å; the synaptic cleft is about 200 Å; there may be 1–50 vesicle-release sites on a presynaptic membrane that is about half micron; dendrites can vary from a few  $\mu\text{m}$  to 4 mm; the soma is about 10  $\mu\text{m}$ ; there are an average of 6000 synaptic connections per neuron; there are  $10^5$  neurons per

$\text{mm}^3$  in a cortical sheet that is only about  $1000 \text{ cm}^2$  in area, when spread out, and of 2.4 mm average thickness; there are about  $4 \times 10^{10}$  neurons, and about  $2.4 \times 10^{14}$  synapses. The synapses of the brain may be thought of as being arrayed on a 3D  $1.1 \mu\text{m}$  lattice [25].

In comparison with electronics, the brain's technology is rather noisy. It was the noisiness of the brain that caused us to emphasize the noise-management techniques of hybrid and distributed computation as being of paramount importance. In comparison with digital electronics, the brain is also slow (a time scale of 10–100 ms. vs 1–10 ns), and yet it can routinely solve sensory tasks in 300 ms. that no supercomputer can do in an eon. However, electronic technology is impoverished in other ways: The number of transistor types is 4 in the very best BiCMOS processes; spatiotemporal processing through structures analogous to dendrites are expensive to create on a neuron-to-neuron basis; the geometry is most often rigidly rectangular with two-dimensional wiring; locally generated power supplies are expensive to create and are rarely ever implemented; chemistry and electronics are not integrated, with chemistry being involved during fabrication, and never during processing, thus preventing adaptation on a very fine scale; and the lack of molecular specificity provided by chemistry prevents the multiplexing of information in the same physical space.

If we collapse the 3D architecture of cortex into a 2D architecture on silicon, maintain the same area of  $1000 \text{ cm}^2$ , replace every synapse with a single transistor, *ignore the costs of wiring (we are being generous to silicon)*, and extrapolate today's design rules for fabrication, we would need a technology whose feature size was about  $50 \text{ \AA}$  and a square 12-inch  $\times$  12-inch wafer! Today's feature lengths are about  $0.35 \mu\text{m}$ , and  $300 \text{ \AA}$  is about the limit at which discrete and quantum effects start to be of importance [33]; the wafer sizes are about 8 inches in diameter. Alternatively, if we keep today's feature sizes, we would need our square silicon wafer to 64-ft  $\times$  64-ft! In conventional digital computing paradigms, the costs for fabricating a wafer without any defects grows exponentially in the size of the wafer. Thus, the difference in costs between a 64-ft.  $\times$  64-ft. wafer and a 8-inch diameter wafer is enormous. It is a tribute to nature that she created a structure that is still way ahead of the finest technology we possess in the world today: the technology of microelectronics.

Nevertheless, there is nothing that the brain can do that we cannot do in electronics, in principle. For example, adaptation can be well mimicked at the level of a single device through the use of floating gates, and networks of transistors can simulate the resistive-grid computation of a dendrite. Our technology will be less efficient than neurobiology because

it is relatively impoverished; however, we can exploit the electronic advantages of lower noise, and higher speed to improve that efficiency.

### 5.6.2 Signal Processing

Apart from the hybrid and distributed nature of the neurobiological signal processing, nonlinearity and adaptation are extremely important as well. Nonlinearity is exploited, rather than avoided. For example, the nonlinear negative damping in the ear is responsible for that organ's instantaneous gain control in response to transient sounds. The clever use of nonlinearity in the outer hair cell allows us to extract information in transients without introducing deleterious distortion or saturating the auditory system. Similarly, adaptation optimizes the gain of the ear for different listening conditions over a long time scale. We would not have a dynamic range of 120 dB in our auditory system if it did not have nonlinear and adaptive properties. It is likely that dendrites have nonlinear and adaptive-gain-control mechanisms as well, so that they can "listen" to and process a variety of input conditions in an optimal way. An adaptive threshold is the simplest example of such a mechanism. Adaptation is built into all levels of the nervous system, from ion channels that are sensitive to the level of calcium to massive cortical reorganization of wiring patterns. *For reasons similar to those outlined in Section 5.4.1, it is efficient to distribute the adaptation in small amounts throughout the system, rather than to do it all in one place.* Distributed adaptive systems are less prone to oscillation because of the low loop gains throughout the system; nevertheless, the overall system has a large loop gain from the accumulated adaptation through all levels of the system. Systems with large loop gain are insensitive to fluctuations at their outputs, because their powerful adaptation compensates for these fluctuations.

### 5.6.3 Computational Strategies

It is possible to do a behavioral task by processing lots of useless information. Neurobiological systems are efficient at processing only the information that is useful for solving the task. Any neurobiology textbook is replete with examples on this subject, and we shall not discuss it further here.

## 5.7 Summary

We conclude by reviewing the main points of the paper:

1. Analog computation is efficient at low-precision processing, and digital computation is efficient at high-precision processing. The resource-precision equations for analog computation (Eq. (5.18) and Eq. (5.19)), and the resource-precision equations for digital computation (Eq. (5.20) and Eq. (5.21)) quantify the costs of computing at a certain precision in MOS technology. Figure 5.3 shows a plot of the costs of analog and digital computation at different levels of precision. The noise-resource equation of a technology (Eq. (5.7) for MOS technology) determines the form of the resource-precision curves for that technology.
2. The advantages of analog computation arise from its exploitation of the physical primitives for computation. The advantages of digital computation arise from its multi-wire representation of information and information processing, and from its signal-restoration properties.
3. Analog computation that distributes its precision and processing resources over many wires is maximally efficient at a certain signal-to-noise ratio per wire, due to the trade-offs between computation and communication. Eq. (5.22) and Figure 5.4 illustrate this fact in more detail.
4. We proposed a hybrid architecture that combines the advantages of discrete-signal restoration with the advantages of continuous-signal, continuous-time analog computation. The key building block of such a hybrid scheme is a restoration circuit called a A/D/A, which is described in Section 5.4.2. Figure 5.5 and Figure 5.6 illustrate the workings of the hybrid scheme. For maximum efficiency in a computation, there is an optimal amount of continuous analog processing that must be done before a discrete signal restoration; Figure 5.7 and Eq. (5.33) illustrate how this optimum can be determined.
5. We described a computing architecture that illustrates the simultaneous working of distributed and hybrid computation in Section 5.4.3 and Figure 5.8. Distributed and hybrid computation combines the best of the analog and digital worlds to create a world that is more efficient than either.

6. In neurobiological systems, where communication costs are relatively low compared with communication costs in silicon, the optimal signal-to-noise ratio per wire is lower than that in silicon. Thus, we believe that nature was smart to distribute her computational resources over many noisy neurons (dendrites and somas), and communicate information between neurons over many noisy wires (axons).
7. The brain uses hybrid representations, because that is the most efficient way for massively complex systems to compute.
8. Experiments suggest that discrete states in the brain are encoded in the crosscorrelated firing patterns of neurons in a network [22]. Neuronal information processing is thus most likely to involve vector signal restoration. In Section 5.5.3, we discussed how signal-restoration in networks of neurons may be implemented using A/D/A-like schemes.
9. From numerous examples, it is qualitatively clear that, in neurobiology, the reduction of noise is accomplished through resource consumption as it is in electronics. Neurobiology and electronics behave similarly because physical and mathematical laws such as the laws of thermodynamics and the law of large numbers do not change with technologies. It is such laws that, with a few technology-dependent parameters, determine noise-resource equations. Since our conclusions depend only on general properties of noise-resource equations such as a polynomial reduction in noise with resource consumption, we suggested that our extrapolation from electronics to neurobiology is correct to leading order.
10. We have emphasized the hybrid and distributed nature of the brain's signal processing as being of paramount importance for its efficiency. However, the brain's great technology, (Section 5.6.1), its nonlinear and adaptive signal processing (Section 5.6.2), and its computational strategies (Section 5.6.3) are also important for its efficiency.

### Acknowledgements

We acknowledge useful discussions with Carver A. Mead, John Allman, Christof Koch, Yaser Abu Mostafa, Kwabena Boahen, Sanjoy Mahajan, Mike Levene, and David Kewley. We thank Lyn Dupre for her detailed editing of our manuscript, and Shih-Chii Liu for a

thorough review of our work. Funding for this work was provided by the Beckman Hearing Center.



## Bibliography

- [1] C. A. Mead, "Neuromorphic Electronic Systems", Invited Paper, Proceedings of the IEEE, Vol. 78, No. 10, pp. 1629–1636, October 1990.
- [2] C.A. Mead, *Analog VLSI and Neural Systems*, pp. 33–36, Addison-Wesley, Reading, Massachusetts, 1989.
- [3] C. A. Mead and L. Conway, *Introduction to VLSI Systems*, pp. 333–371, Addison Wesley, Reading, Massachusetts, 1980.
- [4] R. Landauer, "Information is Physical", *Physics Today*, pp. 23–29, May 1991.
- [5] L. A. Adleman, "Molecular Computation of Solutions to Combinatorial Problems", *Science*, Vol. 266, No. 11, pp. 1021–1024, November 1994.
- [6] D. Deutsch, *Proceedings of the Royal Society of London, Ser. A* 400, p. 97, 1985.
- [7] P. W. Shor, *Proceedings of the 35th Annual Symposium on the Foundations of Computer Science*, p. 124., edited by S. Goldwasser, IEEE Computer Society, Los Alamitos, CA. 1994. Expanded version in LANL quantph archive, preprint 9508027.
- [8] R. Sarpeshkar R. F. Lyon and C. A. Mead, "A Low-Power Wide-Dynamic-Range Analog VLSI Cochlea", to appear in *Analog Integrated Circuits and Signal Processing* Special Issue on Neuromorphic Engineering, expected date of publication: 1997; contained in chapter 4 of this thesis.
- [9] J. Allman, "Evolution of Neocortex", *Cerebral Cortex*, Vol. 8A, pp. 269–283, Edited by E. G. Jones and A. Peters, 1990.
- [10] L. C. Aiello and P. Wheeler, "The Expensive-Tissue Hypothesis: The Brain and Digestive System in Human and Primate Evolution", *Current Anthropology*, Vol. 36, No. 2, pp. 199–221, April 1995.
- [11] Denyer and Renshaw, "VLSI Signal Processing: A Bit Serial Approach", Addison Wesley, 1985.

- [12] R. F. Lyon, "Cost, Power, and Parallelism in Speech Signal Processing", Proceedings of the IEEE 1993 Custom Integrated Circuits Conference, pp. 15.1.1– 15.1.9, San Diego CA, May 9-12, 1993.
- [13] J. Von Neumann, "Lectures on Probabilistic Logics and the Synthesis of Reliable organisms from Unreliable Components", delivered by J. Von Neumann at the California Institute of Technology, Pasadena, January 4–15, 1952; notes by R. S. Pierce.
- [14] R. Sarpeshkar, T. Delbrück, and C. Mead, "White Noise in MOS Transistors and Resistors", *IEEE Circuits and Devices*, pp. 23–29, Nov. 1993; contained in chapter 2 of this thesis.
- [15] T. Cover and J. Thomas, *Elements of Information Theory*, p. 20, John Wiley and Sons, Inc., New York, 1991.
- [16] B. J. Hosticka, "Performance Comparison of Analog and Digital Circuits", Proceedings of the IEEE, Vol. 73, No. 1, pp. 25-29, January 1985.
- [17] P. M. Furth and A. G. Andreou, "Bit-energy comparison of discrete and continuous signal representations at the circuit level", Proceedings of the Physics of Computation Conference, 1996; also see <http://gauss.nmsu.edu:8000/pfurth/>.
- [18] E. A. Vittoz, "Future of Analog in the VLSI Environment", Proceedings of the International Symposium on Circuits and Systems, Vol. 2, pp. 1347-1350, 1990.
- [19] D.A. Kearns, "Experiments in Very Large-Scale Analog Computation", Electrical Engineering PhD thesis, California Institute of Technology, 1993.
- [20] G. Cauwenberghs, "A Micropower CMOS Algorithmic A/D/A Converter", G. Cauwenberghs, *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, Vol. 42, No. 11, pp. 913–919, 1995.
- [21] M. T. T. Wong–Riley, "Cytochrome Oxidase: An endogenous metabolic marker for neuronal activity", *TINS*, Vol. 12, No. 3, pp. 94–101, 1989.

- [22] M. Abeles, H. Bergman, I. Gat, "Cortical Activity flips among quasi-stationary states", Proceedings of the National Academy of Sciences of the United States of America, Vol. 92, No. 19, pp. 8616–8620, September 1995.
- [23] J. Hopfield and A. V. M. Herz, "Rapid Local Synchronization of Action Potentials: Toward computation with coupled integrate-and-fire neurons", Proceedings of the National Academy of Sciences, Vol. 92, pp 6655–6662, July 1995.
- [24] M. Abeles, *Corticonics*, pp. 227–259, Cambridge University Press, Cambridge, 1991.
- [25] C. Koch, *Biophysics of Computation: Information Processing in Single Neurons*, Personal draft of book from the author; book to be published in 1997.
- [26] S. Zhang and L. O. Trussell, "A Characterization of excitatory postsynaptic potentials in the avian nucleus magnocellularis", Journal of Neurophysiology, Vol. 72, pp. 705–718, 1994.
- [27] L. J. DeFelice, *Introduction to Membrane Noise*, pp. 371–453, Plenum Press, New York, 1981.
- [28] C. Allen and C. F. Stevens, "An evaluation of causes for unreliability of synaptic transmission", Proceedings of the National Academy of Sciences, Vol. 91, pp. 10380–10383, Oct. 1994.
- [29] T. F. Weiss, *Cellular Biophysics*, Vol. 2, pp. 331–467, MIT Press; Vol. 1., pp. 449–533, Cambridge, Massachusetts, 1996.
- [30] H. Salman, Y. Soen, E. Braun, "Voltage Fluctuations and Collective Effects in Ion-Channel Protein Ensembles", Physics Review Letters, Vol. 77, No. 21, pp. 4458–4461, 1996.
- [31] G. M. Shepherd, *The Synaptic Organization of the Brain*, Oxford University Press, Oxford, 1990.
- [32] C. A. Mead, personal communication.
- [33] C. A. Mead, "Scaling of MOS Technology to Submicrometer Feature Sizes", Analog Integrated Circuits and Signal Processing, Vol. 6, No. 1, pp. 9–25, Jul. 1994.

- [34] B. K. Siesjo, *Brain Energy Metabolism*, John Wiley and Sons, p. 42, p. 95, p. 267–268, New York, 1978.
- [35] H. S. Bachelard, “Energy Utilized by Neurotransmitters”, in *Brain Work*, pp. 79–81, Alfred Benzon Symposium VIII, Munksgaard, 1975.
- [36] O. D. Creutzfeldt, “Neurophysiological Correlates of Different Functional States of the Brain”, pp. 21–47, in *Brain Work*, Alfred Benzon Symposium VIII, Munksgaard, 1975.
- [37] C. Koch, M. Rapp, and I. Segev, “A Brief History of Time (Constants)”, *Cerebral Cortex*, Vol. 6, pp. 93–101, March/April 1996.
- [38] S. G. Hasselbalch, P. L. Madsen, L. P. Hageman, K. S. Olsen, N. Justesen, S. Holm, O. B. Paulson, “Changes in cerebral blood flow and carbohydrate metabolism during acute hyperketonemia”, *American Journal of Physiology Endocrinology and Metabolism*, Vol. 33, No. 5, pp. E746–E751, May 1996.
- [39] P.R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 2nd. edition, pp. 635-702, John Wiley, New York, 1984.
- [40] R. Sarpeshkar, R. F. Lyon, and C.A. Mead, “A low-power wide linear range transconductance amplifier”, to be published in *Analog Integrated Circuits and Signal Processing*, Special Issue on Neuromorphic Engineering, expected date of publication: 1997; contained in chapter 3 of this thesis.

## 5.8 Appendix A: The Efficiency of Cortical Computation

We first compute the number of synaptic operations that the brain executes per second, and then we discuss the brain’s power consumption.

### 5.8.1 The Operational Throughput of Cortical Computation

From the numbers of the first paragraph of Section 5.6.1, we know that there are about  $2.4 \times 10^{14}$  synapses in each cortex of the brain. The average firing rate of cortex is about 5–10 Hz [25]—we shall use 7.5 Hz. Assuming that each synapse is always operational and

constantly computing, then the number of synaptic operations per second is  $2 \times 2.4 \times 10^{14} \times 7.5 = 3.6 \times 10^{15}$ .

### 5.8.2 The Power Consumption of the Brain

Most of the power consumption of the brain is believed to go into the maintenance of concentration gradients by ion pumps. Estimates of ion-pump power consumption vary from 25–100% [34]; consistent quantitative results are as yet unavailable in this neglected area of research. The ion pumps are the batteries that power all the brain's electrical activity. The power consumed by ion pumps may be accounted for by the ATP-related activity at the pumps, or by adding up the power dissipated in all the resistive ion channels of the brain. Both forms of accounting must yield the same answer by energy conservation. The situation in neurobiology is analogous to one in electronics: We can account for the total power consumption of an electronic chip by measuring the current provided by its power supplies or by adding up the power dissipated in all the resistive circuits to which it supplies power. Ion pumps do not power activity such as neurotransmitter synthesis, uptake, and packaging, synthesis of cellular and vesicular material, axoplasmic transport, and glial-cell activity. The synthesis of neurotransmitter has been shown to consume a negligible amount of energy due to its small turnover rate [35]. Mitochondrial distribution reveals little power dissipation in glial cells [21]. It is an open question whether the energy consumption due to neurotransmitter uptake also is negligible.

The amount of energy consumption due to spiking activity in the brain has been shown to be small from calculations and measurements of heat generated by spiking nerve [36]; the small value is also consistent with mitochondrial distribution [21]. Thus, nonspiking active and passive currents account for most of the brain's electrical power dissipation. However, it is erroneous to conclude that the firing rates of the brain are irrelevant in determining its power consumption: If the firing rates of neurons in the brain were increased globally, all the nonspiking activity of the brain also would have to increase, to keep up with the higher information bandwidth, which is given by the average number of bits per spike times the average spike firing rate.

The total power consumption of the brain hardly changes from its normal value during arithmetic problem solving, during fatigue, during sleep, or during hypoxia and hyperoxia. Even, in an epileptic seizure it increases by only 60 %. During deep anaesthesia or in a coma,

it reduces by 50% [34]. However, regional changes in power consumption could potentially be large, because the conductances of neurons can easily change by more than an order of magnitude due to activity [37]. Thus, we reach the inescapable conclusion that regional changes in power consumption due to activity at one location must be compensated for by a reduction in power consumption at other locations. Given that the power consumption of the brain is one sixth of the total power consumption of the body [10], it is not surprising that evolution did not allow drastic changes in brain power consumption; drastic increases in overall power consumption would have to be accompanied by drastically increased rates of cooling, which don't seem plausible. Generally, in the body, power-hungry organs—such as the kidneys, liver, and brain—have high resting power consumptions that change little with activity. The brain is the neurobiological equivalent of many analog electronic circuits that have high static power dissipation, and little dynamic (signal-dependent) power dissipation. In contrast, most CMOS digital circuits have high dynamic power dissipation and almost no static power dissipation (see Section 5.2.1).

The global power consumption of the brain has been measured numerous times by the Kety–Schmidt technique, and the measurements have generally been fairly consistent, even over 40 years. A recent measurement [38] yielded an oxygen uptake of  $144 \mu\text{mol}\cdot 100\text{g}^{-1}\cdot\text{min}^{-1}$ . The glucose reaction yields, in in-vitro reactions, about  $60 \text{ kJ/mol} \times 38 \text{ ATP}/6 = 380 \text{ kJ/mol}$  of oxygen consumed. The  $60 \text{ kJ/mol}$  value was obtained from [29]. The weight of the brain is about  $1.3 \text{ kg}$  [10]. Thus, the power consumption in watts is computed to be  $11.8 \text{ W}$ , a value that we shall round off to  $12 \text{ W}$ . Some measurements that were performed in the 1970's and used in the studies of [10] yielded  $15 \text{ W}$ . We shall use the more recent measurements of  $12 \text{ W}$  in our paper. Note also that  $12 \text{ W}$  is for both cortices of the brain. Most of the power in the brain is consumed in cortex.

## 5.9 Appendix B: Noise in MOS Transistors

If  $I$  is the mean DC current flowing through a saturated MOS transistor,  $kT$  is an amount of thermal energy,  $f_l$  and  $f_h$  are the lowest and highest frequencies of operation, and  $\Delta f = f_h - f_l$  is the bandwidth of operation, then the mean-square white-noise voltage at the gate input of the transistor,  $v_n^2$ , is given by

$$v_n^2 = \frac{4kT}{2\kappa g_m} \Delta f, \quad (5.35)$$

$$g_m = \frac{\kappa I}{U_T} \quad (5.36)$$

in the subthreshold region of operation, and by

$$v_n^2 = \frac{4kT(2/3)}{g_m} \Delta f, \quad (5.37)$$

$$g_m = \sqrt{2\mu C_{ox} \frac{W}{L}} \sqrt{I} \quad (5.38)$$

in the above-threshold region of operation.<sup>8</sup> In Eqs. (5.35)–(5.38),  $U_T$  is the thermal voltage  $kT/q$ ,  $\mu$  is the mobility of electrons,  $C_{ox}$  is the oxide capacitance,  $W$  is the width of the transistor,  $L$  is the length of the transistor, and  $\kappa$  is the subthreshold exponential coefficient of the transistor.

For later use, it will be convenient to write the white noise for subthreshold and above-threshold regimes as

$$v_n^2 = \frac{K_w(p)}{I^p} \Delta f \quad (5.39)$$

where  $p = 1.0$  for the subthreshold regime, and  $p = 0.5$  for the above-threshold regime. The parameter  $p$  is the exponent in the  $g_m$ -versus- $I$  relation of the transistor, and is an important parameter in MOS technology. We define  $K_w(p)$  such that

$$K_w(1.0) = \frac{4kTU_T}{2\kappa^2} \quad (5.40)$$

in the subthreshold regime, and

$$K_w(0.5) = \frac{4kT(2/3)}{\sqrt{(2\mu C_{ox} \frac{W}{L})}} \quad (5.41)$$

in the above-threshold regime. Note that  $K_w$  is independent of transistor geometry in the subthreshold regime, but is dependent on the transistor geometry in the above-threshold regime. The parameter  $K_w(p)$  is an important parameter of MOS technology.

Another kind of noise in the transistor is called 1/f noise because its power spectrum varies inversely with the frequency. It is widely believed that this form of noise arises from

---

<sup>8</sup>These expressions represent a lower bound on the noise in the transistor. If the transistors are in their linear region of operation, the noise is higher by a small amount. We ignore such factors in this paper, since they are inconsequential to our conclusions.

electrons in the channel going into and out of surface states, and into and out of impurities or defect traps in the gate oxide of the transistor. It is known that the mean-square  $1/f$  noise voltage at the gate input of the transistor  $v_{nf}^2$  scales inversely with the area of the transistor  $A = WL$ . The noise is approximately independent of the current flowing through the transistor.

$$\begin{aligned} v_{nf}^2 &= \frac{K_f}{A} \int_{f_l}^{f_h} \frac{df}{f}, \\ &= \frac{K_f}{A} \ln \left( \frac{f_h}{f_l} \right). \end{aligned} \quad (5.42)$$

The parameter  $K_f$  is given by

$$K_f = \frac{B}{C_{ox}}, \quad (5.43)$$

where  $B$  is a measure of the number of surface states, impurities, or defects in the gate oxide.

The electronic fluctuations just described dynamically modulate the surface potential and thus the threshold voltage of the transistor. Hence,  $1/f$  noise can be viewed as noise due to a dynamically varying threshold voltage. Since the current in a transistor depends on the difference between the gate voltage and its threshold voltage, independent of where the transistor is operating, the input-referred  $1/f$  noise is independent of current. The larger the area of the transistor, the greater the oxide capacitance of the transistor, and the smaller the effect of any one fluctuating electronic charge on the transistor's threshold voltage. However, since the trap and defect densities are approximately constant, the larger the area of the transistor, the greater the number of fluctuating charges. The increased-capacitance effect reduces the noise power like  $1/A^2$ , and the increased total-charge effect increases the noise power like  $A$ , such that the input-referred noise scales like  $1/A$ .

The parameter  $B$  also determines the magnitude of typical offsets in MOS technology: Offsets between transistors are mainly due to mismatches in threshold voltage caused by charges in impurities, surface states, defect traps and so on. By applying the reasoning of the previous paragraph, we can show that offsets scale inversely with the area of the transistor as well. Thus, the RHS of Eq. (5.42) that models the magnitude of  $1/f$  noise in MOS technology, also models the magnitude of the typical offsets in this technology. Actually, the total  $1/f$  noise would be affected by  $f_l$  and  $f_h$ , but the offsets would not be.



So, to model offsets, we should add another term proportional to  $K_f$  but independent of  $f_l$  and  $f_h$ . However, this added complication neither affects nor adds to our conclusions. Thus, we model 1/f noise and offsets with one term.

In summary, the total input-referred noise in a transistor can be written as

$$v_n^2 = \frac{K_w(p)}{I^p} \Delta f + \frac{K_f}{A} \ln(f_h/f_l). \quad (5.44)$$

The first term on the RHS of Eq. (5.44) tells us that thermal noise can always be reduced by increasing  $I$  or equivalently by increasing power consumption. The second term on the RHS of Eq. (5.44) tells us that 1/f noise and offsets can always be lowered by increasing  $A$  or area consumption. Thus, noise reduction is not free but rather is obtained by spending power and/or area resources. In the above-threshold regime,  $K_w(0.5)$  depends on the transistor geometry according to Eq. (5.41). Thus, unlike in the subthreshold regime, in the above-threshold regime we can reduce thermal noise by expending area as well. In both regimes, 1/f noise can only be reduced by spending area. Note that our conclusions assume that  $f_l$  and  $f_h$  are constant and are determined by the requirements of the computation. We discuss how these constraints are implemented, in Section 5.10.

## 5.10 Appendix C: Noise in Analog Systems—Further Details

In the above-threshold regime, we can increase the W/L ratio of a transistor to decrease the thermal noise as seen from Eq. (5.15), Eq. (5.16), and Eq. (5.41) (The dependence of thermal noise on area is hidden in the constant  $K_w$  in Eq. (5.15)). Thus, in the above-threshold regime, if we are limited by thermal noise, we can reduce it by expending area, and consequently can increase  $S_N$ . Furthermore, in the above-threshold regime, if we have the freedom to scale the power-supply voltage in proportion to the  $I/g_m$  ratio of a transistor, then increasing  $I$  and  $V_{DD}$  simultaneously can increase  $S_N$  by increasing the maximum voltage of operation. Thus, in the above-threshold regime, power and area resources can be traded against each other to obtain a certain value of  $S_N$ . In the subthreshold regime no such trade can be made, because, first,  $g_m$  is independent of the geometry of the transistor and depends on only the current level, and, second, because the  $I/g_m$  ratio is invariant with current level.

In Section 5.3.2, we did not take into account the cost of capacitances. When we increased the value of  $I_i$  in stage  $i$ , we asserted that  $f_h$  and  $f_l$  somehow remained constant. However, to keep  $f_l$  and  $f_h$  constant, some area has to be expended in increasing the value of capacitances that determine  $f_l$  and  $f_h$ . If filtering operations represent a small part of a large analog system, then the area resources devoted to these capacitances are negligible. Our analysis implicitly assumed that they were. However, in systems where filtering is a large part of the overall computation, and it is important that the bandwidths of each filtering stage stay constant as  $I_i$  is changed, the area costs of capacitances may no longer be negligible. In the latter case, there is an area capacitance cost of  $aI_i^p/f_i$  associated with stage  $i$ , where  $a$  is a parameter of the technology, and  $f_i$  is the desired corner frequency of the stage. The optimal allocation of resources is then a problem considerably more difficult to solve in closed form, since there is an interaction between the allocations of power resources and area resources. We can provide only intuition for such cases.

The thermal noise levels still decrease with an increase in power consumption. However, the  $1/f$  noise (and offset) levels increase with increasing power consumption, because transistor area is sacrificed for capacitor area. Thus, if we wish to minimize the total noise, for a given amount of area consumption, there is an optimal amount of power consumption. Hence, we can think of area as being the only true independent resource of the system. The low-frequency stages must have their current levels and capacitances reduced, compared with cases where capacitance costs are negligible. The high-frequency stages must have their current levels and capacitances, increased compared with cases where capacitance costs are negligible. In systems built with transconductance–capacitor filters, we can also use circuit tricks, such as transconductance reduction [40], to keep the bandwidths constant. In this case,  $n_i$  becomes a function of  $I_i$ ; there is then an interaction between the complexity of the circuit and the power resources used. The net result is that the total noise at the output is a more complicated function of the power and area resources and has the form

$$v_{no}^2 = \frac{C'_w}{f(P_T)} + \frac{C'_f}{g(A_T - h(P_T))}, \quad (5.45)$$

where  $f(x)$ ,  $g(x)$ , and  $h(x)$  are smooth monotonically increasing functions of  $x$ , built out of power-law-like and polynomial-like component functions; and  $C'_w$  and  $C'_f$  are constants that depend on the task, technology, and ingenuity of the designer.

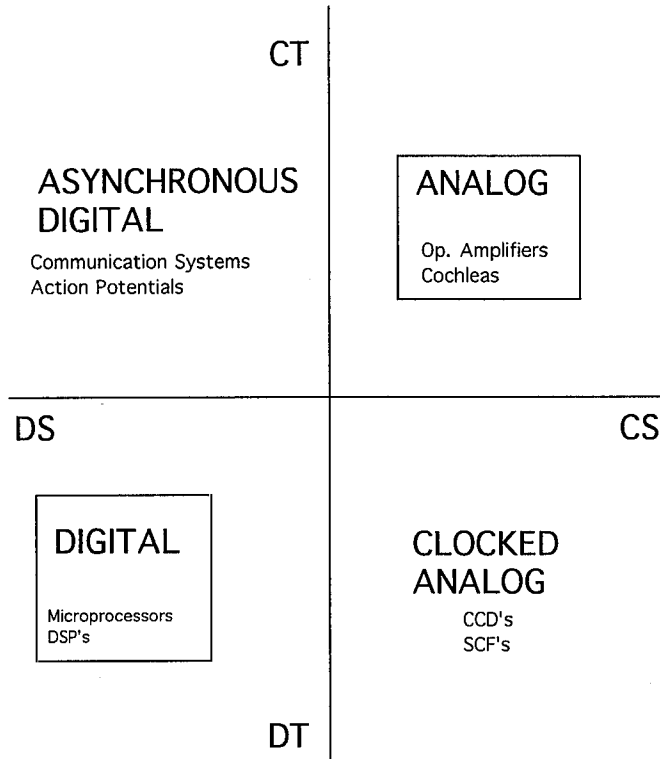


Figure 5.1: The Four Types of Systems. Systems operate with continuous (CS) or discrete signals (DS), and in continuous (CT) or discrete time (DT). Thus, there are four classes of systems—CSCT, CSDT, DSCT, DSDT. The figure shows examples of electronic and biological systems in each class. The acronym SCF stands for Switched Capacitor Filter. The acronym CCD stands for Charge Coupled Device. Typically, continuous-signal systems are referred to as analog, and discrete-signal systems are referred to as digital, irrespective of their representation in the time domain. Analog systems that are continuous in both the signal and time domains and digital systems that are discrete in both the signal and time domains have been boxed in the figure. Such systems are the most common examples of analog and digital systems respectively, and are also the most disparate from each other.

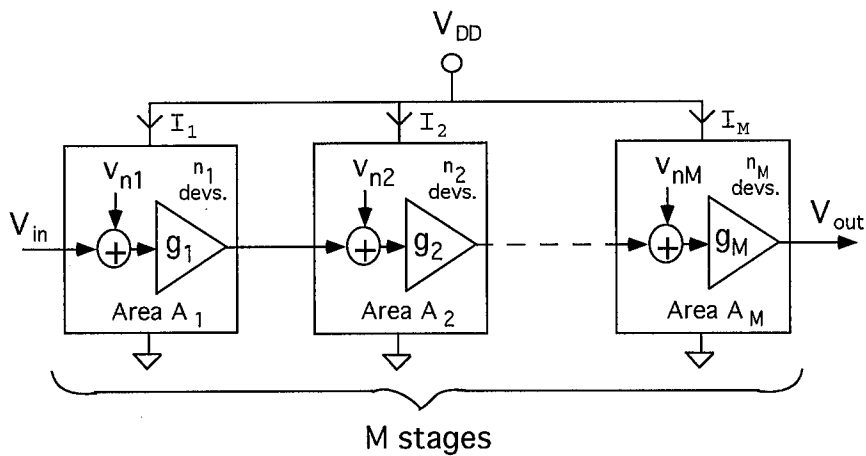


Figure 5.2: Noise Accumulation in an Analog System. The figure shows a cascade of  $M$  analog computational stages. Each stage consumes a current  $I_i$ , consumes an area  $A_i$ , has  $n_i$  devices, has a gain  $g_i$ , and contributes a noise  $v_{ni}$ . The common power supply is represented by  $V_{DD}$ . If we want to minimize noise at the final output,  $V_{out}$ , subject to fixed constraints on total current consumption and total area consumption, then Eq. (5.8), Eq. (5.12), and Eq. (5.14) show that the complex stages (with large numbers of devices) and the early stages (with large amounts of accumulated gain) should get most of the system's resources of current and area.

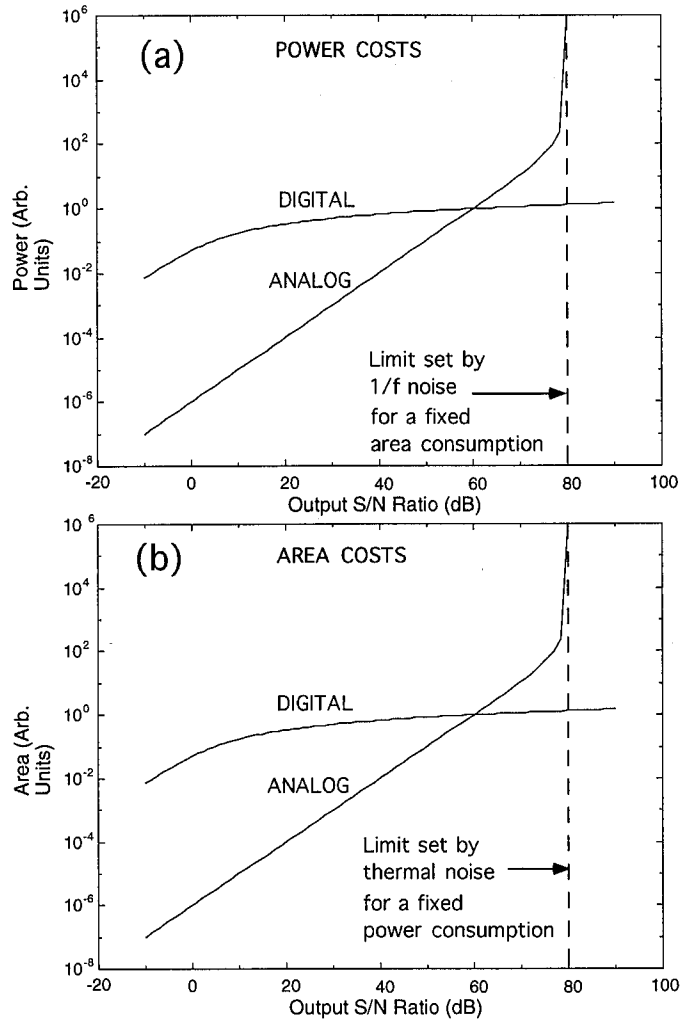


Figure 5.3: Resource–Precision Curves—Analog Versus Digital. The figure shows plots of the *resource–precision* equations for analog computation (Eq. (5.18) and Eq. (5.19)) and digital computation (Eq. (5.20) and Eq. (5.20)) for subthreshold technology ( $p = 1$ ). The plots show how the resource utilization (power in (a) or area in (b)) is a function of  $S_N$ , the output signal-to-noise ratio (a measure of precision). Analog computation is cheap because of its use of physical primitives, but, at high precision, the costs of maintaining low noise and offset on one wire make it expensive. Digital computation is costly because of its use of logical primitives; nevertheless, at high precision, its multiwire representation of information and information processing makes it efficient. In (a), the power cost for analog computation diverges when  $S_N$  is limited by 1/f noise (or offset); we must spend area in this situation to reduce 1/f noise (or offset). Similarly, plot (b) shows that the area cost  $A_T$  diverges when  $S_N$  is limited by thermal noise; hence, we must spend power to reduce the thermal noise. Actually, these conclusions of divergence are only true for the subthreshold regime where the power and area resources of a transistor may not be traded against each other to obtain a certain value of  $S_N$ . Appendix 5.10 contains a discussion that shows how we may trade between power and area in the above-threshold regime.

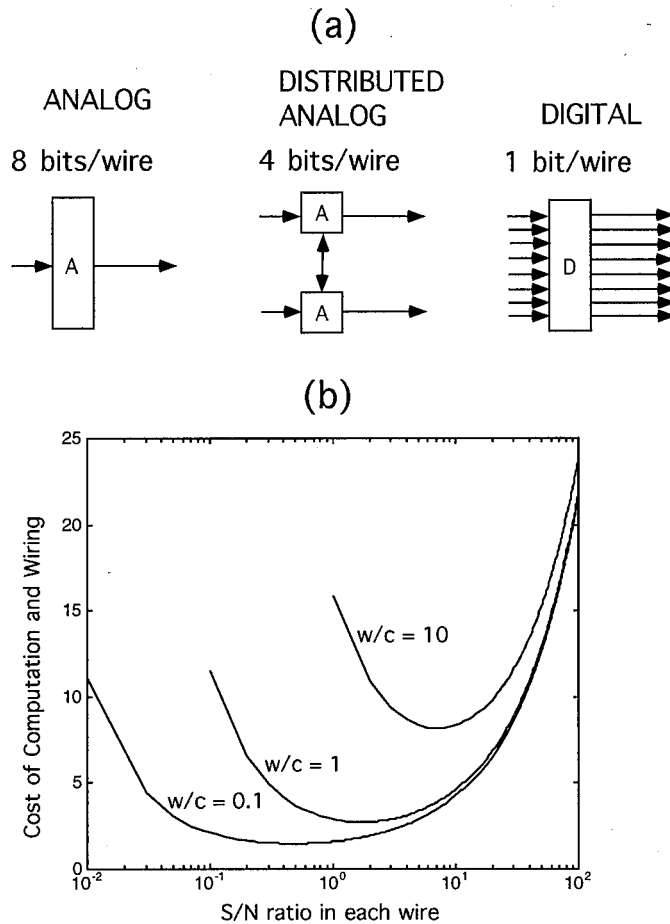


Figure 5.4: Distributed Analog Computation. (a) The idea behind distributed analog computation is illustrated with an example. Instead of the usual analog paradigm that represents 8 bits of information on one wire, or the usual digital paradigm that represents 8 bits of information on 8 wires, in distributed analog computation we represent 8 bits of information on two wires that carry analog signals. Also, instead of one analog processor maintaining 8 bits of precision on its output wire, we now have two processors that interact with each other, and maintain 4 bits of precision on their respective output wires. In general, there may be correlations between the information carried by the two wires. (b) Plots of the total cost of computation and communication as a function of  $S_N$  in each wire, for  $c = 1$ , and for various  $w/c$  ratios in Eq. (5.22) are shown. We see that when wiring is expensive with respect to computation ( $w/c = 10$ ), the optimal signal-to-noise ratio is high, and we have few wires. When wiring is cheap ( $w/c = 0.1$ ), the optimal signal-to-noise ratio is low, and we have more wires. In neurobiological systems, where wiring costs (due to axons) are relatively low compared with wiring costs in silicon, the signal-to-noise ratio per wire is lower than that in silicon.

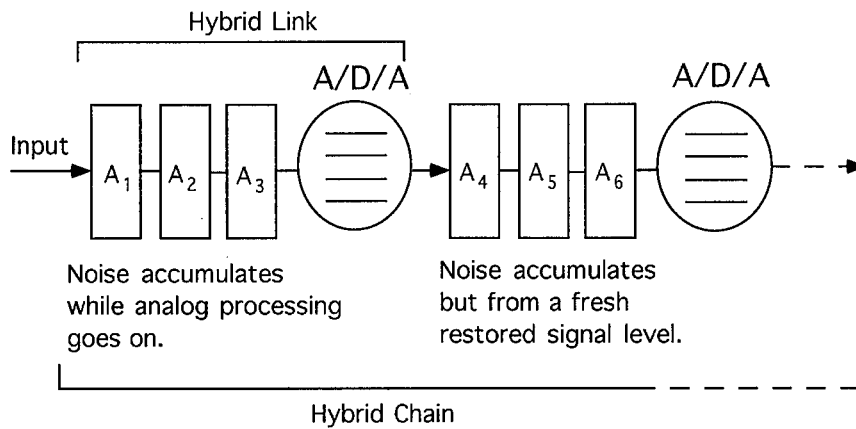


Figure 5.5: Hybrid Computation. A *hybrid link* is a set of analog processing stages (denoted  $A_i$  in the figure) followed by an A/D/A that restores the analog signal to one of  $M$  discrete attractor states. A *hybrid chain* is composed of a sequence of hybrid links. Each chain can maintain analog information to a precision of  $\log_2(M)$  bits with a low probability of error provided we meet the following constraint: The net input-referred noise of the A/D/A, due to all processing stages in a link and the restoration circuits in the A/D/A, must be significantly lower than the minimum distance between attractor states. In Section 5.4.2 we quantify this constraint. Effectively, we can operate with the precision and complexity characteristic of digital systems, while doing efficient analog processing.

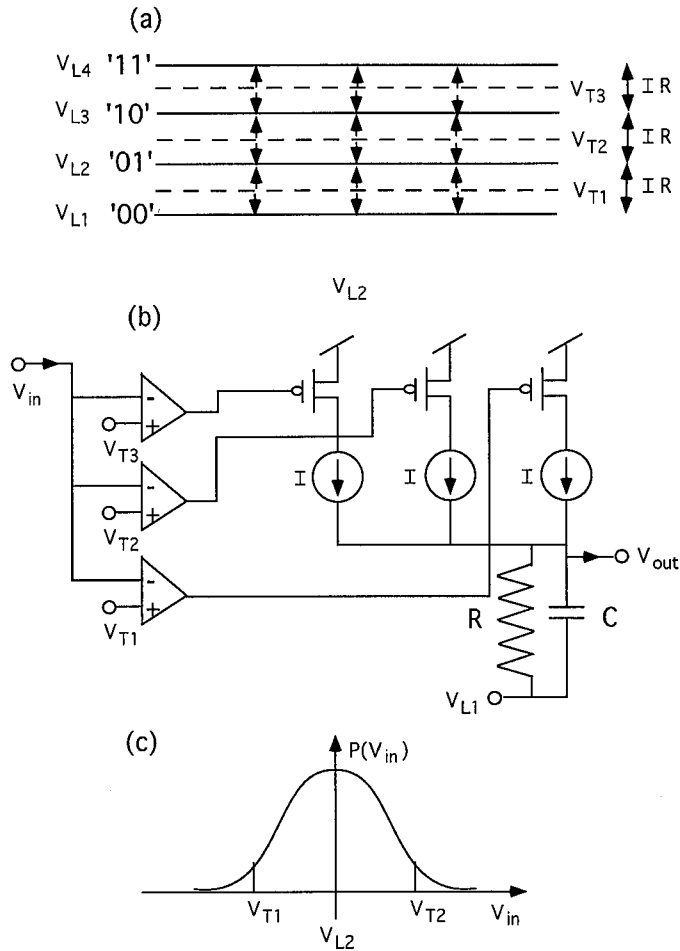


Figure 5.6: The A/D/A. (a) The input signal is compared with  $M - 1$  threshold levels and rounded off to the restoration level that it is closest to. The threshold levels  $V_{T_i}$  and restoration levels  $V_{L_i}$  for a four-state or two-bit system are shown. The arrows converge on restoration levels and diverge from threshold levels. (b) A circuit for one possible implementation of a 4-state A/D/A is shown. The analog signal is compared with three thresholds and 0, 1, 2, or 3 currents are switched onto a resistor, whose voltage then equilibrates at  $V_{L1}$ ,  $V_{L1} + IR$ ,  $V_{L1} + 2IR$ , or  $V_{L1} + 3IR$  respectively. The RC-circuit acts as a filter and removes sharp edges in the signal. The capacitance is chosen so that  $1/RC$  is at or near the desired bandwidth of the input. (c) The probability of a bit error for a worst-case situation when the input is at  $V_{L2}$  is given by the area under the Gaussian tails, i.e., to the left of  $V_{T1}$  and to the right of  $V_{T2}$ . Section 5.4.2 provides further details.



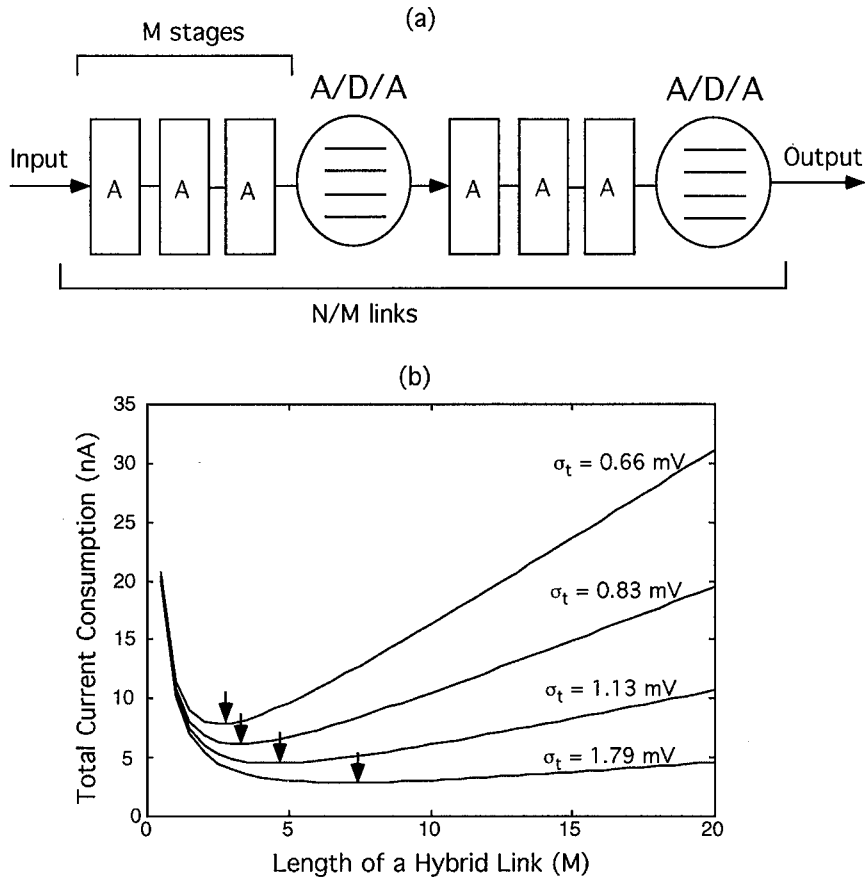


Figure 5.7: The Optimal Length of a Hybrid Link. (a) To maximize the efficiency of information processing in a hybrid chain, there is an optimal amount of analog processing that must occur before signal restoration in a hybrid link, i.e., hybrid links should not be too long or short. If the link is too long we spend too much power (and/or area) in each analog stage in order to maintain the requisite precision at the input of the A/D/A. If the link is too short, we spend too much power (and/or area) in frequent signal restorations. (b) The figure shows a plot of the current consumption (obtained from Eq. (5.33)) versus link length ( $M$ ) for differing values of precision, parametrized by  $\sigma_t$ , the input-referred noise at the A/D/A. Section 5.4.2 provides further details. As the precision increases, the optimal length of the hybrid link is shortened.

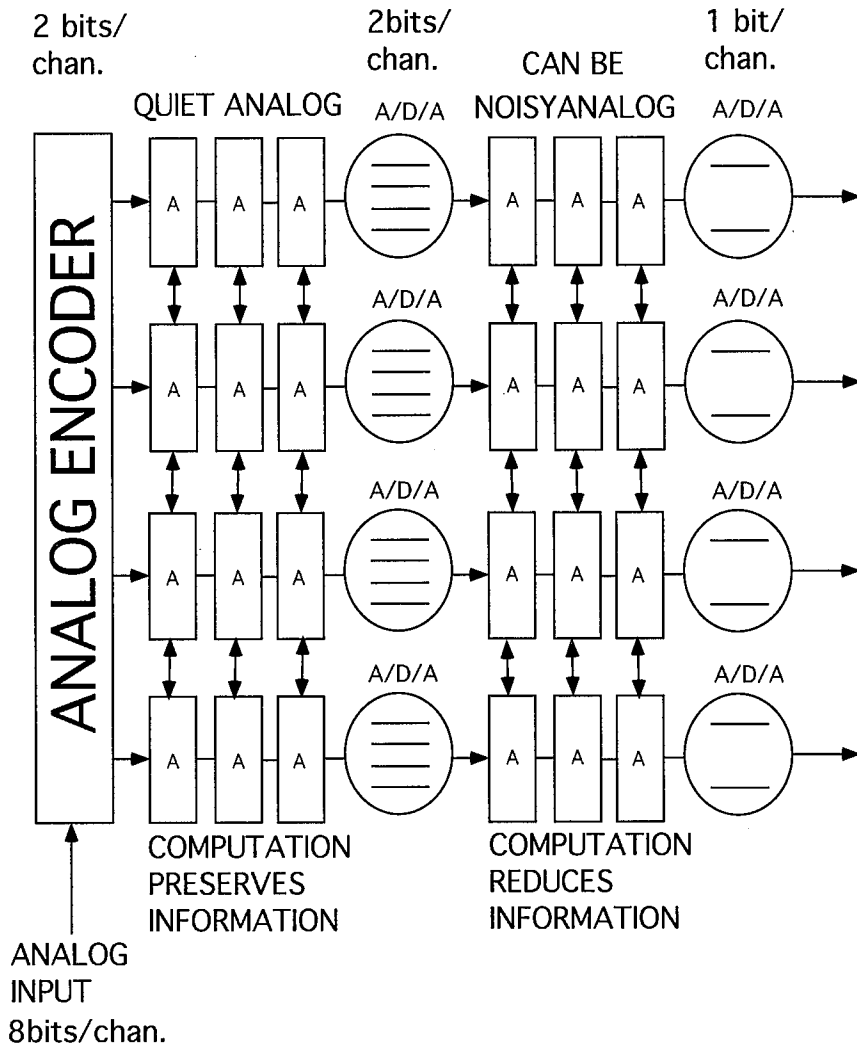


Figure 5.8: Distributed and Hybrid Computation. This scheme combines the best of the analog and digital worlds to create a world that is more efficient than either. The information from a single-wire analog input is encoded onto many wires by an analog encoder such as a cochlea, retina or A/D. In the example of the figure, the distributed information is preserved in the first stage of processing by 2-bit A/D/As. In the next stage of processing, the analog processors and/or the A/D/As make decisions based on the information and reduce the output information to 1-bit. Thus, the analog circuits in the second half can afford to be noisier since the A/D/A restoration only has a precision of one bit. The use of distributed analog computation and low-precision A/D/A signal restoration make this architecture ideal for efficient precise computation.

## Chapter 6 A New Geometry for All-Pole Underdamped Second-Order Transfer Functions

### Abstract

In the standard  $s$ -plane geometric interpretation of a second-order transfer function with two complex poles and no zeroes (the frequently occurring transfer function of underdamped oscillators), the gain depends on the product of two lengths, and the phase is the sum of two angles. This construction obscures the overall frequency response, hiding important quantities such as the gain peak and the corner frequency. We present an alternate “one-pole” geometry in which the gain depends on one length, and the phase corresponds to one angle. In this space, many relationships in the transfer function become obvious; quantities such as the group delay and bandwidth have simple forms and geometric interpretations.

### 6.1 Introduction

Because Newton’s law is a second-order differential equation, and damped oscillators are ubiquitous, second-order transfer functions with two complex poles abound in nature. Examples include springs, pendula, elastics, RLC and active-filter circuits, lasers, atomic vibrations, acoustics, and audition. In this article we discuss a geometric view of these transfer functions that makes their behavior intuitive.

### 6.2 The Usual Geometry

The transfer function of a second-order system with two poles is given by [1]

$$H(s) = 1 / \left( 1 + \frac{\tau s}{Q} + \tau^2 s^2 \right), \quad (6.1)$$

where  $H$  is the transfer function,  $s$  is the Laplace transform variable,  $Q$  is the quality factor of the resonant circuit, and  $\tau$  is the time constant of the system. We will only discuss

the common case of underdamped second-order transfer functions, *i.e.*, systems for which  $Q > 0.5$ , and both poles are complex. The value  $Q = 0.5$  corresponds to a critically damped system with coincident poles just about to leave the real axis in the  $s$  plane. Our results may be trivially generalized to signal-processing filters that have two complex zeroes, by reciprocating gains and negating phases.

With  $s = j\omega$ , the gain and phase are given by

$$|H(j\omega)| = \frac{1}{\sqrt{(1 - \omega^2\tau^2)^2 + \omega^2\tau^2/Q^2}}, \quad (6.2)$$

$$\text{Arg } H(j\omega) = -\arctan\left(\frac{\omega\tau/Q}{1 - \omega^2\tau^2}\right), \quad (6.3)$$

$$= -\arccos\left(\frac{1 - \omega^2\tau^2}{\sqrt{(1 - \omega^2\tau^2)^2 + \omega^2\tau^2/Q^2}}\right). \quad (6.4)$$

Figure 6.1 shows the usual geometric interpretation of these equations for the underdamped case where both poles are complex. To calculate the gain at the frequency point,  $F$ , measure the distances,  $d_1$  and  $d_2$ , from  $F$  to the two poles,  $P_1$  and  $P_2$ . The gain is  $1/d_1d_2$ . To calculate the phase, add the signed angles made by  $\overline{P_1F}$  and the  $x$ -axis, and by  $\overline{P_2F}$  and the  $x$ -axis. In a double-zero system, this sum is the phase, whereas in a double-pole system, you negate this sum to get the phase. For example, at DC ( $\tau s = 0$ ), these two angles are equal and opposite, and the phase is zero. At infinite frequency ( $\tau s \rightarrow +i\infty$ ), both angles are  $90^\circ$ , and the phase is  $-180^\circ$  for a double-pole system.

### 6.3 Transforming to the New Geometry

In eq. (6.2), we notice that the important variable of interest is the square of the normalized frequency,  $\omega^2\tau^2$ . Thus, it's natural to first define a simpler variable,

$$x = \omega^2\tau^2. \quad (6.5)$$

With this substitution, we expand squares in eq. (6.2) to get

$$|H(x)| = \frac{1}{\sqrt{1 - 2x(1 - 1/2Q^2) + x^2}}. \quad (6.6)$$

Now we define an angle  $\theta$  such that

$$\sin \theta = 1 - \frac{1}{2Q^2}, \quad (6.7)$$

or equivalently,

$$\theta = \arcsin\left(1 - \frac{1}{2Q^2}\right). \quad (6.8)$$

For eq. (6.8) to be valid, the argument of the arcsin must be within  $\pm 1$ , which means that  $0.5 \leq Q \leq \infty$ . So our substitution works for the underdamped cases that we're interested in. Actually, the construction also works for  $-\infty < Q \leq -0.5$ , *i.e.*, for negatively damped systems with complex poles; the results for positive  $Q$  carry over, except that we negate the phase.

We may now simplify eqs. (6.2)–(6.8) to obtain

$$|H(x)| = \frac{1}{\sqrt{(x - \sin \theta)^2 + \cos^2 \theta}}, \quad (6.9)$$

$$\text{Arg } H(x) = -\arctan\left(\frac{\sqrt{x}/Q}{1-x}\right), \quad (6.10)$$

$$= -\arccos\left(\frac{1-x}{\sqrt{(x - \sin \theta)^2 + \cos^2 \theta}}\right). \quad (6.11)$$

*Eqs. (6.5) and (6.8) are the key equations of our paper.. We will show how they enable us to construct simple geometric interpretations of our transfer function.*

## 6.4 The Geometry of Gain

We can interpret eq. (6.9) as saying that the magnitude transfer function  $|H(x)|$  is the reciprocal of the Euclidean distance between the point  $(x, 0)$  and the point  $(\sin \theta, \cos \theta)$ . A pictorial representation of eq. (6.9) is shown in Figure 6.2: The  $x$  axis in the figure represents  $x = \omega^2 \tau^2$ ; that is, it is proportional to the square of the normalized frequency. The negative  $x$  axis is meaningless in this geometry (squares are always positive), and is therefore shown with dotted lines. *To plot the magnitude frequency response, we move along the  $x$  axis from 0 to  $+\infty$ , and compute the reciprocal of our distance from a fixed point that lies on a semicircle of radius 1 at  $(\sin \theta, \cos \theta)$ .* The angular location of the fixed point on

the semicircle is determined by  $Q$  according to eq. (6.8); consequently, we call the fixed point the  $Q$  point. For  $Q = 0.5$ , the phase is  $\theta = -90^\circ$ , and the  $Q$  point is located at  $(-1,0)$ . For  $Q = \infty$ , the phase is  $\theta = +90^\circ$ , and the  $Q$  point is located at  $(1,0)$ . For  $Q \in [0.5, \infty]$ , the angular location of the  $Q$  point varies between  $-90^\circ$  and  $+90^\circ$ . Some important  $Q$  points are  $Q = 1/\sqrt{2} = 0.707$ ,  $(0,1)$ , where  $\theta = 0$ ;  $Q = 1$  where  $\theta = 30^\circ$ ; and  $Q = 1.93$  where  $\theta = 60^\circ$ . If we define  $\phi = 90^\circ - \theta$ , then

$$Q = \frac{1}{\sqrt{2}(\cos(\theta/2) - \sin(\theta/2))}, \quad (6.12)$$

$$= \frac{1}{2\sin(\phi/2)}. \quad (6.13)$$

We now itemize a list of relationships that are obvious from the geometry:

- At low frequencies, the distance from the  $Q$  point is approximately the radius of the semicircle, and thus the gain is near 1.
- As we move away from the origin the gain rises, because the distance from the  $Q$  point decreases. The gain peaks at  $x = \sin\theta$ , when we are directly underneath the  $Q$  point. As we move past the peak, the distance increases and the gain falls.
- In  $x$  space, the transfer function is symmetric about the peak for  $x \leq 2\sin\theta$ ; at  $x = 2\sin\theta$ , the distance is again 1 (The first time that the distance was 1 was at  $x = 0$ ).
- Since the peak gain is at  $x = \sin\theta$ , and the place where the gain is unity is at  $x = 2\sin\theta$ , the unity-gain and peak-gain frequencies are a factor of two apart in  $x$  space, or are one-half an octave apart in frequency space. The algebraic proof of this result is tedious with the original transfer function eq. (6.2).
- The value of the peak gain,  $1/\cos\theta$ , is evident in the geometry.
- We can determine the critical value of  $Q$  at which there is a gain peak in the transfer function: To have a gain peak, the  $Q$ -point must be on the right half of the semicircle; otherwise, the distance from it will always increase with frequency, eliminating the gain peak. Thus,  $Q = 0.707$  is the critical value. The geometry divides the space into a left quadrant without a gain peak and a right quadrant with a gain peak. When

there is a gain peak, the gain is greater than 1, because the distance to the  $Q$  point at the peak is always less than the radius of the semicircle.

Thus, we observe that various relationships in the magnitude transfer function become transparent in our one-pole construction.

### 6.4.1 Relationship to Other Geometries

For the benefit of readers, we tabulate expressions for useful quantities in various representations:

- Rectangular representations in the usual geometry that use the  $a$  and  $b$  parameters of Figure 6.1. This representation is often used in audition and speech-recognition literature, e.g. in [2].
- Polar representations in the usual geometry that use  $\omega_n = 1/\tau$  and  $Q$  parameters. This representation is often used in physics literature, e.g. in [3];  $\omega_n$  is determined by nondissipative energy storage elements, and  $Q$  is determined by dissipative damping elements.
- Polar representations in the usual geometry that use  $\omega_n$  and  $\Theta$ , where  $\Theta$  is marked in Figure 6.1.
- Our polar representation that uses  $\omega_n$  and  $\theta$ . Note that we implicitly use  $\omega_n$  when we work with the square of the normalized frequency  $x = (\omega/\omega_n)^2$ .

The latter two representations are closely related. It may be shown that  $\Theta$  of the third representation, is related to  $\phi$  and  $\theta$  of our representation through

$$\phi = \pi/2 - \theta = 2\Theta = 2 \arcsin(1/2Q). \quad (6.14)$$

Eq. (6.14) is extremely useful in converting between the representations. Figure 6.3 shows that, because the angle subtended at the center is half the angle subtended at the circumference [4], the  $x$  plane represents  $\Theta$  as well; also, because the angle subtended at the circumference by a semicircle is  $90^\circ$  [5], and the angle between perpendiculars to lines is equal to the angle between lines,  $\Theta$  is also the angle marked at the  $Q$  point in the figure. Figure 6.4 shows a more detailed comparison of our representation vs. that of the  $\omega_n$  and  $\Theta$

representation. Note the warping of the symmetric gain curve in  $x$  space to the asymmetric gain curve in  $s$  space and the representation of  $\theta$  in  $s$  space. The  $\theta$  values are marked with tickmarks in both spaces.

Expressions for useful quantities in all four representations are summarized in Table 6.4.1. It is sometimes more convenient to use  $\phi$ , that is,  $(\pi/2 - \theta)$  instead of  $\theta$ , in our representation, but, for the sake of consistency, we've used only  $\theta$  in all the tabulated expressions.

Table 6.1: Useful Quantities in the Four Representations

	$a$ and $b$	$\omega_n$ and $Q$	$\omega_n$ and $\Theta$	$\omega_n$ and $\theta$
Underdamped Region	$a > 0, b > 0$	$0.5 < Q < \infty$	$0 < \Theta < \pi/2$	$-\pi/2 < \theta < \pi/2$
Gain > 1 Region	$0 < a < b$	$1/\sqrt{2} < Q < \infty$	$\pi/4 < \Theta < \pi/2$	$0 < \theta < \pi/2$
Damping	$a/\sqrt{a^2 + b^2}$	$1/(2Q)$	$\sin \Theta$	$\sin(\pi/4 - \theta/2)$
Peak Frequency	$\sqrt{b^2 - a^2}$	$\omega_n \sqrt{1 - 1/(2Q^2)}$	$\omega_n \sqrt{\cos 2\Theta}$	$\omega_n \sqrt{\sin \theta}$
Peak Gain	$(a^2 + b^2)/2ab$	$Q/(\sqrt{1 - 1/(4Q^2)})$	$1/(\sin 2\Theta)$	$1/(\cos \theta)$
$-90^\circ$ Frequency	$\sqrt{a^2 + b^2}$	$\omega_n$	$\omega_n$	$\omega_n$
$-90^\circ$ -Frequency Gain	$\sqrt{1 + b^2/a^2}/2$	$Q$	$1/(2 \sin 2\Theta)$	$1/(2 \sin(\pi/4 - \theta/2))$
Unity Gain Frequency	$\sqrt{2(b^2 - a^2)}$	$\omega_n \sqrt{2 - 1/(Q^2)}$	$\omega_n \sqrt{2 \cos 2\Theta}$	$\omega_n \sqrt{2 \sin \theta}$
3dB Frequencies	$\frac{b^2 - a^2 \pm 2ab}{a^2 + b^2}$	$(1 - \frac{1}{2Q^2}) \pm (\sqrt{1 - \frac{1}{4Q^2}})/Q$	$\omega_n (\cos 2\Theta \pm \sin 2\Theta)$	$\omega_n (\sin \theta \pm \cos \theta)$

## 6.5 The Geometry of Phase

A pictorial interpretation of eqs. (6.10) and (6.11) is shown in Figure 6.5. *The angle  $\psi$  is the negative of the phase.* The distance  $d$  is the reciprocal of the gain and is the distance from  $x$  to the  $Q$  point, as we discussed in section 6.4. With the point  $x$  as center, we draw an arc of radius  $d$  that intersects the vertical line  $x = 1$  at the *phase point*. If we draw a *phase vector* from  $x$  to the phase point, then the angle between the phase vector and the positive  $x$  axis is  $\psi$ . To plot the phase of the frequency response, we move along the  $x$  axis and compute  $\psi$ .

We have a symmetry—to compute gain, we measure distances from our current location on the  $x$  axis to the  $Q$  point on the semicircle; to compute phase, we measure angles between the phase vector and the positive  $x$  axis. However, the gain construction is simpler to visualize than is the phase construction, because the phase construction requires drawing an arc for each frequency. We can avoid this difficulty if we simply realize that the phase point is  $(1, \sqrt{x}/Q)$  because of the consistency of eqs. (6.10) and eq. (6.11); therefore, it moves up the vertical line  $x = 1$  as  $x$  moves to the right on the  $x$  axis. Hence, we may



imagine a ladder with its foot at  $(x, 0)$ , and with its length being the reciprocal of the gain, sliding against the wall  $x = 1$ ; then, the angle that the ladder makes with the floor (the positive  $x$  axis) is the negative of the phase.

At low frequencies, the point  $(1, \sqrt{x}/Q)$  is near the  $x$  axis and the angle  $\psi$  is nearly zero. As we increase  $x$ , the angle  $\psi$  increases as we decrease  $1 - x$  and increase  $\sqrt{x}/Q$ . At  $x = 1$ ,  $\psi$  is  $90^\circ$ , with the phase point located at  $(1, 1/Q)$ . Note that  $1/Q$  is also the distance from  $(1, 0)$  to  $(\sin \theta, \cos \theta)$ , because of our arc construction.<sup>1</sup> As  $x$  increases beyond 1, the phase point moves up the vertical line  $x = 1$  at a rate given by  $1/(2Q\sqrt{x})$ ; that rate is always less than the horizontal rate of motion of  $x$  (*i.e.*, 1) for  $Q \geq 0.5$ . If  $Q$  is large,  $\psi$  is small for all  $x$  except those  $x$  near 1, since  $\sqrt{x}/Q$  remains small even while  $x$  changes by a large amount; as we cross  $x = 1$ ,  $\psi$  increases above  $90^\circ$  and quickly heads toward  $180^\circ$  as the  $1 - x$  distance rapidly overtakes the slow motion of the phase point. Thus, we may infer that the slope of the phase curve around  $90^\circ$  increases with  $Q$ . In fact,  $d\psi/dx$  is  $Q$  at  $x = 1$ .

Figure 6.6 shows how we can make an alternate construction that also yields  $\psi$ , by drawing  $\sqrt{x}/Q$  versus  $x$ . Then, at any point  $x$ , the ratio of the curve height to the distance of  $x$  from 1 (*i.e.*,  $1 - x$ ) is  $\tan \psi$ . By eq. (6.10),  $\psi$  is the negative of the phase of the transfer function. The construction of Figure 6.6 is identical to that of Figure 6.5, except that, in the former case, the phase-point computation is performed on a curve, whereas, in the latter case, it is done by an arc construction.

## 6.6 How to Remember the Mapping From Algebra to Geometry

Eqs. (6.5) and (6.8) were responsible for mapping the transfer-function algebra into geometry, and for all of the resulting simplifications. Eq. (6.5) is easy to remember since it merely states that we work with the square of the normalized frequency. Eq. (6.8) is more painful on the memory. One way to avoid this pain is to simply remember the following fact: The gain of a second-order transfer function is always  $Q$  at its corner frequency; thus, the distance from the  $Q$  point  $(\sin \theta, \cos \theta)$  to the corner-frequency point  $(1, 0)$  is  $1/Q$ . By

<sup>1</sup>There is an easier way to show that the distance from  $(1, 0)$  to  $(\sin \theta, \cos \theta)$  is  $1/Q$ . This distance is the reciprocal of the gain at  $x = 1$ . At  $x = 1$ , the gain is  $Q$ , so the distance must be  $1/Q$ . It may also amuse you to show that the distance from  $(\sin \theta, 0)$  to  $(1, 0)$  is  $1/2Q^2$ , and that from  $(\sin \theta, \cos \theta)$  to  $(\sin \theta, 0)$  is  $\sqrt{1 - 1/4Q^2}/Q$ .

computing the Euclidean distance between the latter two points, eq. (6.8) is then easily rederived.

## 6.7 The Geometry of Group Delay

The group delay of a filter,  $T_g$ , is defined as the negative of the derivative of phase with respect to angular frequency  $\omega$ . The group delay is useful in estimating quantities like the delay and dispersion of the filter's impulse response.

$$T_g = -\frac{\partial(\arg H)}{\partial\omega} = \frac{\partial\psi}{\partial\omega}, \quad (6.15)$$

where  $\psi$  is the negative of the phase, as defined earlier in section 6.5.

Rather than work with the formula for phase eq. (6.3), which would require differentiating, it is possible to differentiate phase graphically. Consider the standard  $s$ -plane plot of the pole locations and the angles  $\psi_1$  and  $\psi_2$  from the horizontal to the point  $j\omega$ , as shown in Figure 6.7. Since these are poles,  $\psi = -(\psi_1 + \psi_2)$ , and

$$T_g = \frac{\partial\psi_1}{\partial\omega} + \frac{\partial\psi_2}{\partial\omega} \quad (6.16)$$

The trick is to get simple algebraic expressions for the derivatives of the angles, while avoiding the angles themselves. The rate of change of an angle with respect to a moving point is inversely proportional to the distance to the point, which we label  $d_1$  in Figure 6.7. The rate is also proportional to the "direction cosine" that describes how the point is moving relative to the "tangential" direction that would most affect the angle. This direction cosine is just the ratio  $d_2/d_1$  in Figure 6.7. The fact that  $d_1$  comes into the denominator twice is convenient, since it is a hypotenuse.

$$\frac{\partial\psi_1}{\partial\omega} = \frac{d_2}{d_1^2} = \frac{a}{a^2 + (\omega - b)^2} \quad (6.17)$$

$$\frac{\partial\psi_2}{\partial\omega} = \frac{a}{a^2 + (\omega + b)^2} \quad (6.18)$$

We have used the rectangular description of the pole locations in the  $s$ -plane due to their obvious simple relationship to the geometric differentiation. We now express the sum over a common denominator and convert to the "polar" parameters  $\omega_n^2 = a^2 + b^2$ ,  $Q = \omega_n/2a$ ,

where  $\omega_n = 1/\tau$  is the corner frequency; also, we define  $x = \omega^2\tau^2$  to be the square of the normalized frequency, as per our earlier definitions. Then,

$$T_g = \frac{2a(a^2 + b^2) + 2a\omega^2}{(a^2 + b^2)^2 + 2(a^2 - b^2)\omega^2 + \omega^4} \quad (6.19)$$

$$\begin{aligned} \omega_n T_g &= \frac{1+x}{Q(1 + (1/Q^2 - 2)x + x^2)} \\ &= \left(\frac{1+x}{Q}\right) |H|^2 \\ \Rightarrow T_g &= \frac{\tau}{Q} (1+x) |H|^2 \end{aligned} \quad (6.20)$$

Notice that the group delay is closely related to the gain magnitude  $|H|$ . In particular, from the form of eq. (6.20) we can make a direct construction for group delay in the geometry that we used for gain and phase.

If we have two “poles” at the  $Q$  point and at the symmetrically located point on the bottom of the circle, as shown in Figure 6.8, and a “zero” at  $x = -1$ , then the product of the distances,  $d_z/d_p^2$  yields the group delay of eq. (6.20) apart from the constant  $\tau/Q$  scale factor. Thus, we can visualize the dependence of group delay on  $x$  by a two-pole/one-zero construction. This construction is not as simple as the one-pole construction for gain or phase. Yet it is a vast simplification over eq. (6.19). Note that unlike the gain or squared gain, the group delay is not symmetric in  $x$ , and that the effect of the zero shifts the group-delay peak to a somewhat higher frequency than the gain peak.

## 6.8 Conclusions

The new geometry described in this paper clarifies the properties of a second-order transfer function with two complex poles. We hope that others will find it useful in working with these transfer functions as we have.

## 6.9 Acknowledgements

We thank L. M. Peterson for useful suggestions and enthusiasm regarding this work. This work is supported by a Beckman Hearing Grant. S.M. is supported by a Hertz fellowship.

## Bibliography

- [1] Mead, C. A., *Analog VLSI and Neural Systems*, pp. 179—186, Addison Wesley, New York, 1989.
- [2] Flanagan, J. L., “Models for approximating basilar membrane displacement”, *Bell Sys. Tech. J.* **39**, pp. 1163–1191, 1960.
- [3] Bekefi, G., and Barrett, A.H., *Electromagnetic Vibrations, Waves and Radiation*, Chapt. 1 “The Oscillator”, pp. 1—116, M.I.T. Press, Cambridge 1987.
- [4] Euclid, *The Thirteen Books of the Elements*, translated by T.L. Heath, Vol. **2**, Proposition 20, pp. 46–49, Dover Publications, New York, 1956.
- [5] Euclid, *The Thirteen Books of the Elements*, translated by T.L. Heath, Vol. **2**, Proposition 31, pp. 61–65, Dover Publications, New York, 1956.

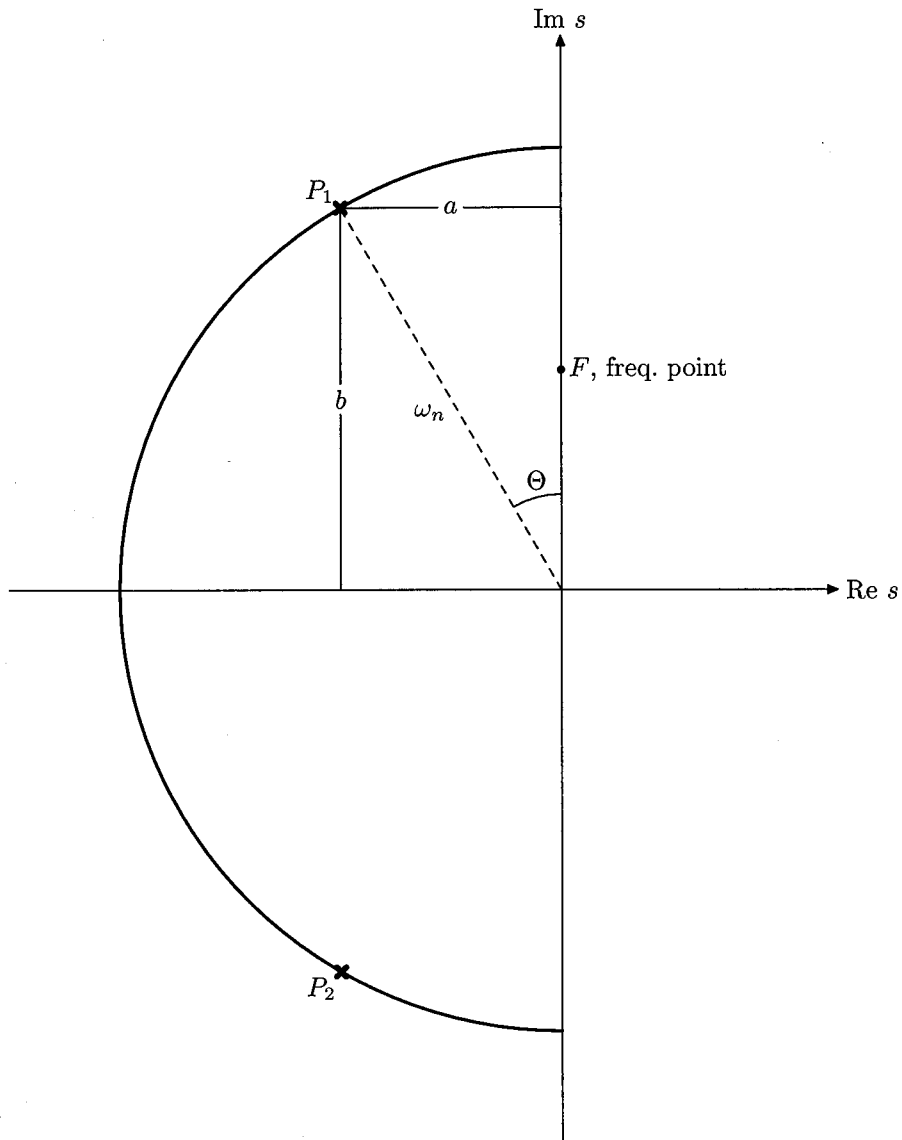


Figure 6.1: The usual geometric interpretation of a two-pole system. You need distances and angles from two poles,  $P_1$  and  $P_2$ , to calculate the gain and phase at  $F$ .

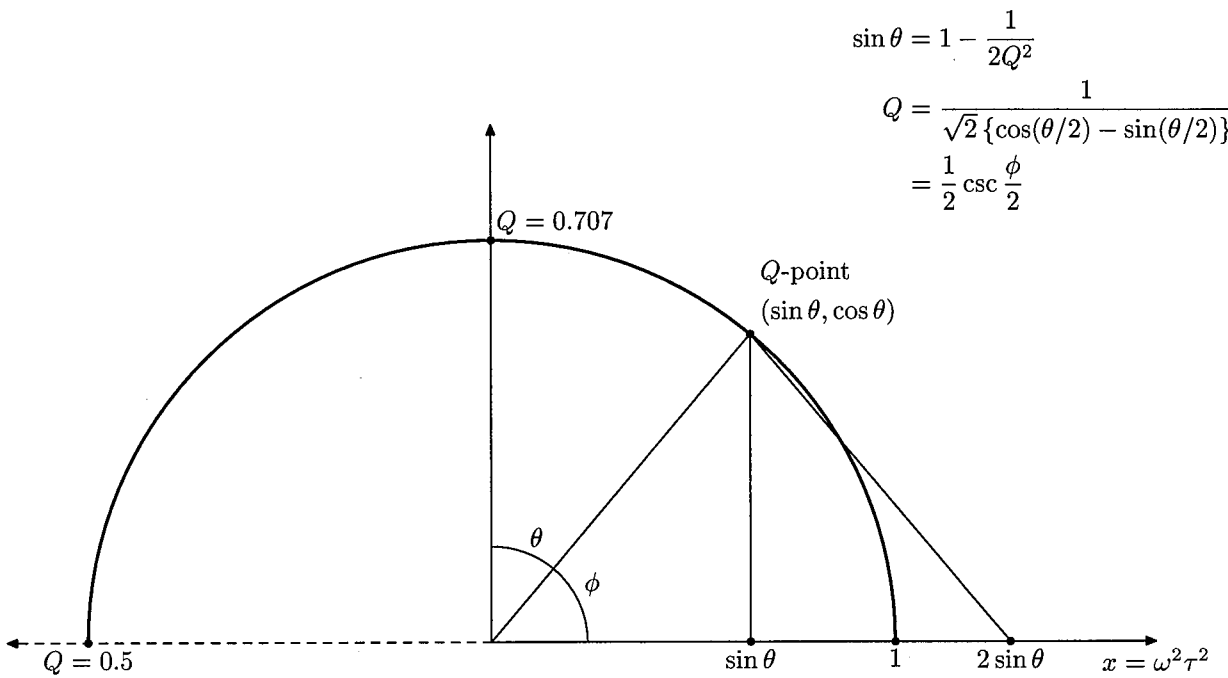


Figure 6.2: The geometry associated with finding the gain of a second-order transfer function. The  $x$  axis represents the square of the normalized frequency  $\omega\tau$ , where  $1/\tau$  is the corner frequency of the transfer function (see eq. (6.1)). The  $Q$  point  $(\sin \theta, \cos \theta)$  lies on a semicircle of radius 1. Different values of  $\theta$  correspond to different values of  $Q$ —the angle  $\theta = -90^\circ$  corresponds to  $Q = 0.5$ ,  $\theta = 0^\circ$  corresponds to  $Q = 0.707$ , and  $\theta = +90^\circ$  corresponds to  $Q = \infty$ . The relationship between  $\theta$  and  $Q$  is shown in the equations at the top of the figure. The gain at the frequency corresponding to  $x$  is the reciprocal of  $d$ , the distance from the frequency point  $(x, 0)$  to the  $Q$  point. The zero-frequency gain is unity; the gain peaks at  $x = \sin \theta$  with a value of  $1/\cos \theta$ , and is unity again at  $x = 2 \sin \theta$ . The gain is symmetric around the peak for  $x \leq 2 \sin \theta$  in  $x$  space. For  $x > 2 \sin \theta$ , the gain is less than 1 and decreases monotonically with  $x$ .

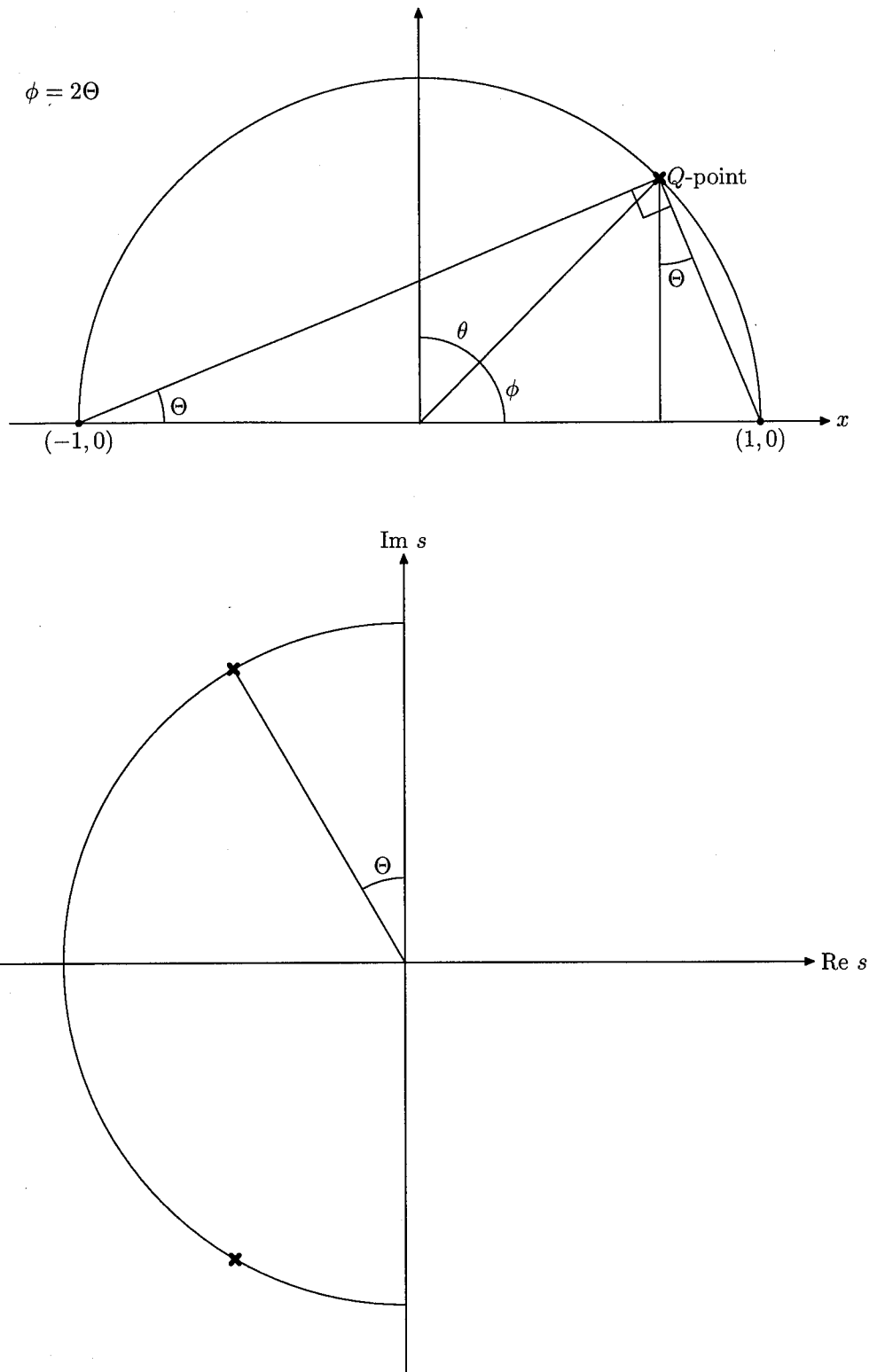


Figure 6.3: The relation between angles in the  $x$  plane (top figure) and the  $s$  plane (bottom figure). The angle  $\phi$  in the  $x$  plane is twice the angle  $\Theta$  which is represented in the  $s$  plane and  $x$  plane as shown. The angle  $\theta$  in the  $x$  plane is  $\pi/2 - \phi$ , that is,  $\pi/2 - \Theta/2$ .





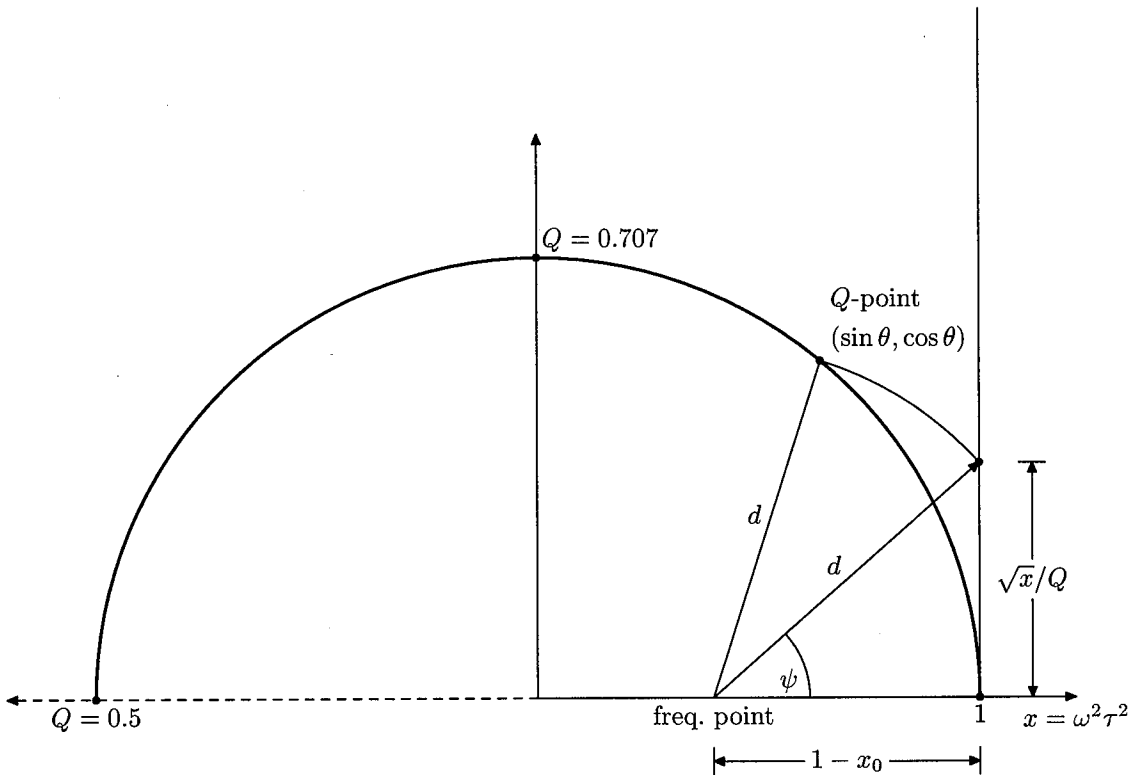


Figure 6.5: The geometry associated with finding the phase of a second-order transfer function. The normalized  $x$  axis,  $Q$  point, and semicircle are identical to those of Figure 6.2. The distance  $d$  is the reciprocal of the gain at the point  $x_0$ . The *phase point*  $(1, (x_0/Q)^{0.5})$  is located at the intersection of an arc of radius  $d$ , centered at the point  $(x_0, 0)$ , and the line  $x = 1$ . The *phase vector* is the vector from  $(x_0, 0)$  to the phase point. The angle  $\psi$  between the positive  $x$  axis and the phase vector is the negative of the phase of the transfer function.

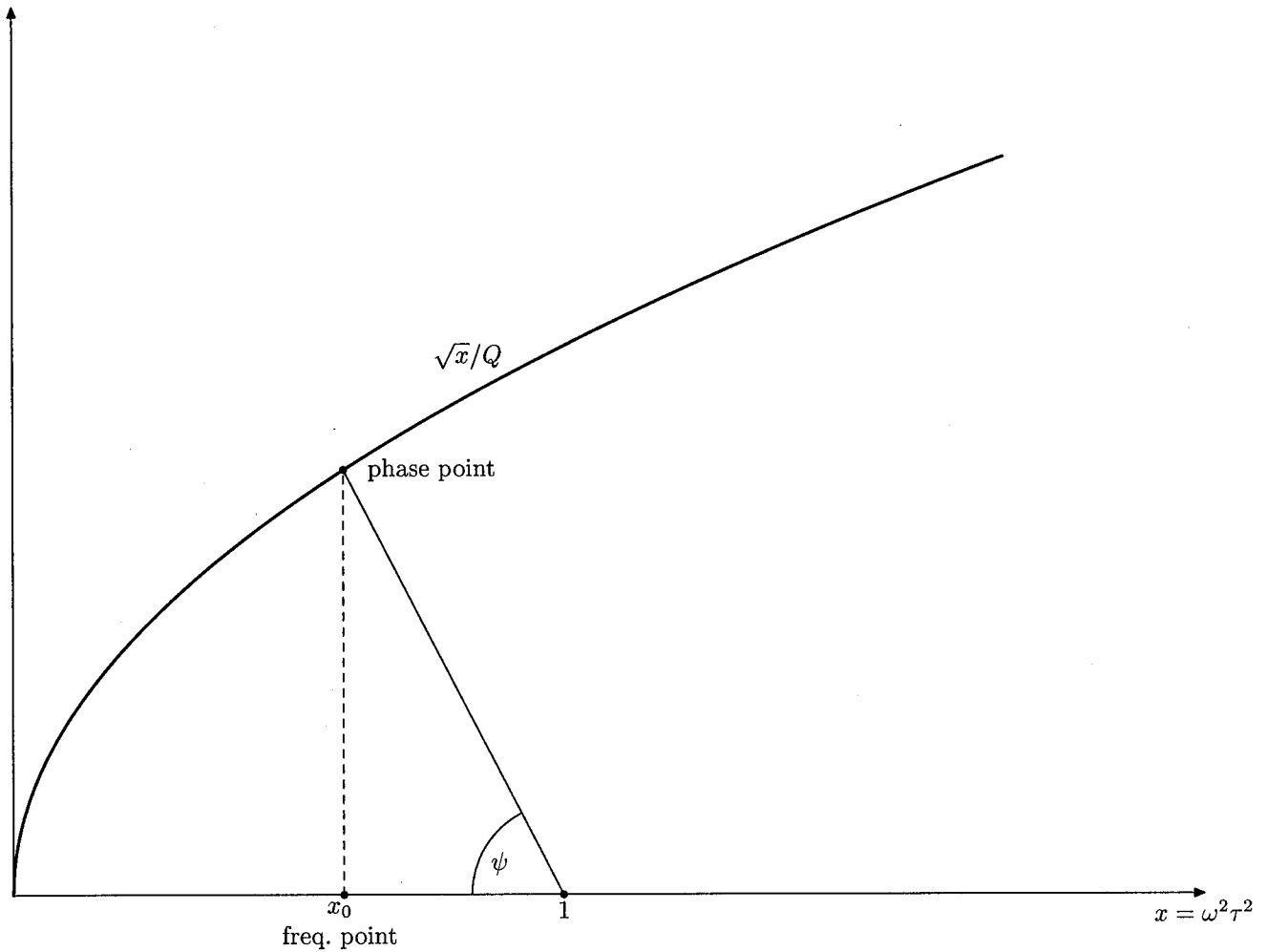


Figure 6.6: An alternate construction that we can use to find the phase of a second-order transfer function by drawing  $(x/Q)^{0.5}$  versus  $x$ . At any point  $x_0$ , the ratio of the curve height to the distance of  $x_0$  from 1 (i.e.,  $1 - x_0$ ) is  $\tan \psi$ , where  $\psi$  is the negative of the phase of the transfer function. The construction of Figure 6.6 is identical to that of Figure 6.5, except that, in the former case, the phase-point computation is performed on a curve; in the latter case, it is done by an arc construction. Note that varying  $Q$  simply scales  $\tan(\psi)$ .

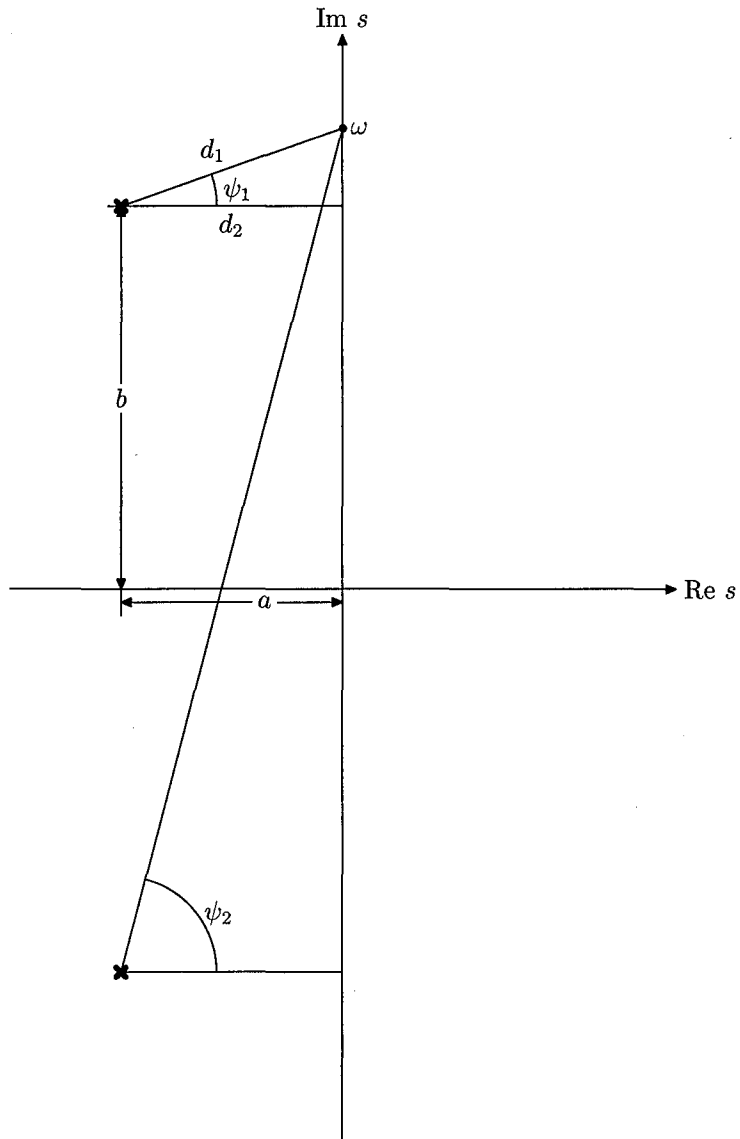


Figure 6.7: The determination of group delay. The group delay is the rate of change of the quantity  $\psi_1 + \psi_2$  with  $\omega$ .

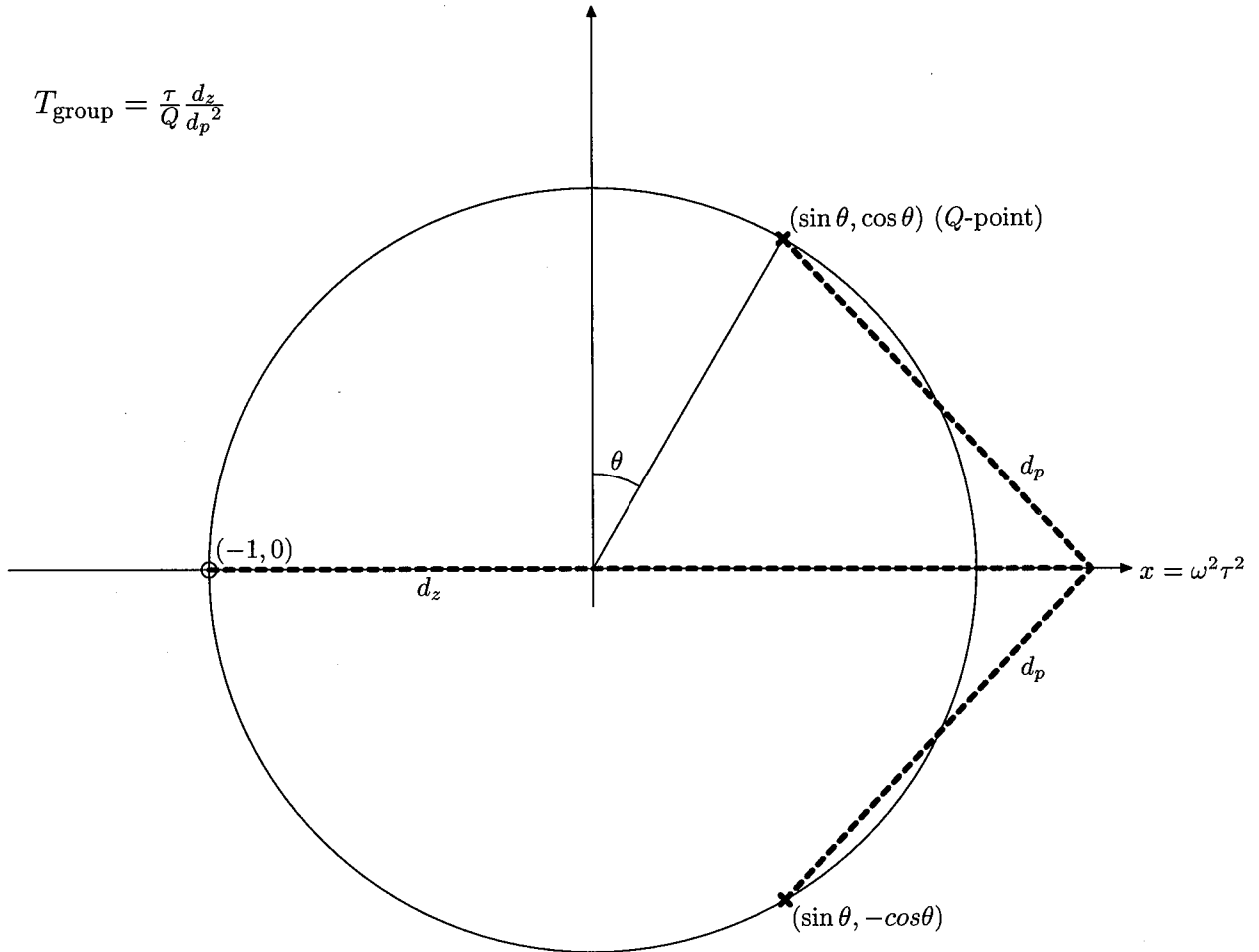


Figure 6.8: The representation of group delay in the  $x$  plane by a two-pole/one-zero construction. The group delay is the product of  $\tau/Q$ , a scale factor, and  $d_z/d_p^2$ ;  $d_z$  is the distance from the “zero” at  $(-1, 0)$  to the point  $(x, 0)$ , and  $d_p^2$  is the product of the distances from the two “poles” at  $(\sin \theta, \cos \theta)$  (the  $Q$  point) and  $(\sin \theta, -\cos \theta)$ .