Signal Integrity Issues in High-Speed Wireline Links: Analysis and Integrated System Solutions

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To

Yadollah Analui and Ashraf Kamali

for their unconditional love.

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Abstract

This work focuses on the basic signal integrity issues of high-speed wireline links. It bridges the gap between optimum system design and circuit design for such links by: (1) understanding the effects of the system parameters on the bit error rate (BER), (2) introducing circuit architectures for the realization of systems that minimize the BER, and (3) demonstrating integrated circuit prototypes that verify the solutions.

First, we develop a theory that analytically relates the data link BER to the system characteristics, *e.g.*, the channel response, the pre-amplifier bandwidth, and the transmitter clock jitter. We generate the BER contours to find the optimum receiver bandwidth as well as the optimum sampling point and its associated timing margin. We also develop the theory of the data-dependent jitter (DDJ), which is a significant component of the timing jitter in high-speed links. We provide an analytical distribution function for the DDJ of an arbitrary linear time-invariant system and include the impact of the DDJ on the BER.

Second, we propose a bandwidth enhancement method for wideband amplifiers. This is useful for the realization of high-speed links in technologies that suffer from large parasitic components. The method leverages two-port broadband matching to enable amplifier stages to achieve their maximum gain-bandwidth product. We demonstrate a 10Gb/s CMOS 0.18μm amplifier with this technique that has 2.4 times the bandwidth improvement over a design that does not apply the technique.

Third, we develop an eye-opening monitor (EOM) that enables full integration of adaptive equalizers. The EOM evaluates the signal eye diagram quality and reports a quantitative measure, which is correlated to the signal integrity. We demonstrate a prototype in 0.13μm standard CMOS that operates up to 12.5Gb/s and has 68dB error dynamic range.

Finally, we introduce an instantaneous clockless demultiplexer for burst-mode communication applications. We propose a clockless finite state machine that recovers and demultiplexes the received burst of data instantaneously. The architecture consists of a combinational logic structure and a bit-period-delayed feedback loop. We demonstrate a 1:2 clockless demultiplexer based on this concept in SiGe BiCMOS technology that operates at 7.5Gb/s.

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