Low-Temperature Hot-Wire Chemical Vapor Deposition of Epitaxial Films for Large-Grained Polycrystalline Photovoltaic Devices

Thesis by

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In Partial Fulfillment of the Requirements

for the Degree of

Doctor of Philosophy

California Institute of Technology
Pasadena, California
2006
(Defended June, 2006)

Acknowledgements

This has been the hardest part of my thesis to write, to do it properly would take an entire thesis in and of itself, but I will try my best. The past four years have been incredibly rewarding both personally and professionally, and I have many people to thank for this. I am incredibly grateful for the time I have spent in the Atwater Group. I could not have hoped for a better match in an advisor. Harry was kind enough to spend a lot of time with me during my first year to help me understand the specifics of the project and its larger context in the field of photovoltaics. He then allowed me free range to explore, but was always there when I got stuck. He has supported my attendance at countless meetings, conferences, and workshops, a rare opportunity for most graduate students.

Of course, this research would not have been possible without the financial support of several organizations. The National Renewable Energy Lab funded the early stages of this project and Dave Carlson at BP Solar was instrumental in ensuring that this project continued to have funding through the Future Technology Program at BP Solar. I would also like to thank the National Science Foundation and Corning Inc. through the National Physical Science Consortium for their graduate fellowships.

I was fortunate enough to inherit this project from Maribeth Mason, who helped me get off to a quick start. Young-Bae Park is an incredible resource of silicon technology, and discussions with him motivated the chapter on the surface evolution of silicon thin-films. Brendan Kayes and I risked life and limb together in the pursuit of higher silicon photovoltaic knowledge and because of his critical eye, he became my sounding board. Matt Dicken and Melissa Griggs generously allowed me to hijack their chambers and their time for RHEED measurements. Katsu Tanabe and Robb Walters set up the photovoltaic efficiency measurements.

Learning how to prepare samples for and to use a TEM is never an easy feat and Carol Garland and Channing Ahn worked to make this as painless for me as possible. David Michalak

tried with several of my SURF students to do lifetime measurements and was a valuable resource on lifetime measurement techniques and ohmic contacts to silicon. Liz Miura generously ran all of the Raman measurements. David Boyd and Eugene Mahmoud helped me, and several of my undergrads, with the FTIR. Chi Ma runs an incredibly tight ship in the geology microscopy facility, and Ali Ghaffari manages the nano/micro facility in Watson, in which I heavily used the AFM, profilometer, and spinner. I would also like to thank all of the undergrads who did research with me at Caltech: Chloe Lepomme, Jacqueiline Greene, Josue Martinez, Joanne Yim, Kavita Raghavan, and Neliza Leon. I learned a lot about managing both people and projects by working with them. Thanks also to the members of my candidacy and thesis committees: Harry Atwater, David Goodwin, Nate Lewis, Rob Phillips, and Kerry Vahala.

One reason photovoltaics research is such a rewarding and pleasant area to work in is due to the scientists at the National Renewable Energy Lab. The low-temperature HWCVD epitaxial Si work of Howard Branz, Eugene Iwaniczko, and Chaz Teplin led to many interesting and helpful discussions. They generously ran several depositions to try and passivate my films grown by graphite filament HWCVD with a *p*+ amorphous emitter grown at NREL. Qi Wang provided help early on in discussing the combinatorial approach and HWCVD design, and Robert Reedy analyzed an incredible number of SIMS samples for me when I was trying to solve a large and mysterious contamination problem.

Stefan Gall at the Hahn-Meitner-Institut provided aluminum induced large-grained polycrystalline templates on glass. I also benefited from discussions with Jens Schneider on large-grained polycrystalline templates, and with Bjoern Rau on low temperature epitaxial growth and post-deposition treatments. In addition, Corning generously provided both institutes with novel high-temperature glass substrates with coefficients of thermal expansion close to that of silicon. Thank you also to Magnus Wagener and George Rozgonyi at NCSU for the near-field photocurrent mapping of several samples.

Even before my arrival at Caltech, I was fortunate to have a great number of fantastic mentors. Jeremy Martin at Advanced Micro Devices first encouraged me to consider Caltech and I'm incredibly glad that I did. Peter Searson and Tim Weihs at the Johns Hopkins University have served as great sources of advice and inspiration, not to mention writing recommendations for me years after I graduated.

Personally, I would like to thank Julie Biteen, who gets the best office-mate ever award. Her personal and professional support over the past few years cannot be underestimated. Jennifer Ruglovsky was my instant family, and after being out of school for two years, was nice enough to explain to me how to solve an integral without laughing, at least not to my face. Jimmy Zahler has been an entertaining source of knowledge about both the photovoltaic industry and life in general. I have also enjoyed the camaraderie of Julie and Rhett Brewer, Ken Diest, Jen Dionne, Tao Feng, Krista Langeland, Gerald Miller, Anna Fontcuberta i Morral, Ben Kaufmann, Carrie Ross, and Luke Sweatlock. Outside of the group, I (and my marriage) also owe many thanks to Eric Johnsen, Joe Klamo, and Amy Zahler for their baby-sitting services.

Melissa Griggs, Michael Haverty, Maribeth Mason, Josh Richardson, and especially Julie Biteen and Brendan Kayes deserve special thanks for reading and correcting drafts of my thesis. Thank you to Eleonora Chetverikova, Irene Loera, Mary Metz, Cierina Marks, and April Neidholt for placing purchase orders, supplies, processing travel receipts, and all the other behind-the-scenes activities that keep the Applied Physics department and the Atwater group running.

Finally, and most importantly, I would like to thank my entire extended family. My parents, Ken and Terri Esber, have always been a great source of encouragement, support, and love. My husband, Josh, who first fostered my sense of social responsibility, has not only withstood two cross-country moves to pursue my interest in photovoltaic research and this degree, but has also picked up most of the cooking and cleaning duties so that when I get home I can enjoy our two beautiful boys, Aiden and Dillon. They definitely help me remember what is important in life. Thanks.

Abstract

Large-grained polycrystalline silicon thin-films on low-cost substrates are an interesting area of research for photovoltaic devices. Such devices, with grain sizes larger than the thickness of the cell, have the potential to achieve multicrystalline-like efficiencies of 15%, but at a much lower cost by taking advantage of thin-film manufacturing techniques. In this thesis, low-temperature epitaxial growth, by hot-wire (or catalytic) chemical vapor deposition, is investigated for the epitaxial thickening of large-grained polycrystalline silicon templates formed by metal-induced crystallization on low-cost substrates. Low-temperature hot-wire chemical vapor deposition allows for the deposition of epitaxial silicon with polycrystalline breakdown and with open-circuit voltages close to that of monocrystalline silicon. This is possible due to the incorporation of hydrogen into the silicon lattice, at temperatures below 350°C, for internal surface and defect passivation. In addition with hot-wire chemical vapor deposition, the critical epitaxial thickness actually increases, with a decrease in the substrate temperature down to temperatures of 270°C. Epitaxial growth of 5.5 μm thick films at 300°C and twinned epitaxial silicon growth of 6.8 μm thick films at 230°C have been achieved, along with arbitrarily thick crystalline films at low temperatures. Since epitaxial and high-quality crystalline silicon can be deposited at such low deposition temperatures, low-cost substrates, such as ordinary soda lime glass and many polymers are possible. In order to work towards achieving an epitaxially-thickened large-grained polycrystalline device, this work studies the mechanisms that lead to epitaxial growth during hot-wire chemical vapor deposition on silicon (100) substrates under various growth regimes, examines the surface evolution of crystalline thin-films grown via hot-wire chemical vapor deposition and their growth mechanisms (including the unusual rough epitaxial growth and arbitrarily thick crystalline films at low temperatures), and concludes by presenting the optical and electrical characteristics of these films and their resultant devices. This

thesis demonstrates that low-temperature epitaxial silicon growth by hot-wire chemical vapor deposition is a promising material for low-cost thin-film silicon photovoltaic devices.

List of Related Publications

1. **C. E. Richardson,** Y.-B. Park, and H. A. Atwater, "Surface Evolution during Low Temperature Epitaxial Silicon Growth by Hot-wire Chemical Vapor Deposition: Structural and Electronic Properties." *Proceedings of the 4th IEEE Photovoltaics Specialists Conference.* Waikoloa, HI. (2006) **Chapters 4 and 6.**

2. **Christine Esber Richardson,** Y.-B. Park, and H. A. Atwater. "Surface Evolution during Crystalline Silicon thin film growth by Low-temperature Hot-wire Chemical Vapor Deposition on Silicon Substrates." Phys. Rev. B **73** (24) 2006. **Chapters 4 and 5.**

3. **Christine E. Richardson**, M.S. Mason and Harry A. Atwater. "Hot-wire CVD Grown Epitaxial Films and a Model of Epitaxial Breakdown." *Thin Solid Films* **501** (1-2), 332 (2006). **Chapters 2 and 3.**

4. Maribeth S. Mason, **C. E. Richardson**, Harry A. Atwater, R.K. Ahrenkiel. "Microsecond Minority Carrier Lifetimes in HWCVD-Grown Films and Implications for Thin Film Solar Cells." *Thin Solid Films* **501** (1-2), 288 (2006). **Chapters 6 and 7.**

5. **Christine E. Richardson**, J. K. Holt, and Harry A. Atwater. "Epitaxial Silicon and Silicon Nitride Growth by Hot-wire Chemical Vapor Deposition for Photovoltaic Devices." *Proceedings of the 15th Workshop on Crystalline Si Solar Cells.* Vail, CO. (2005) **Chapters 2 and 3.**

6. **Christine Esber Richardson**, B.M. Kayes, M.J. Dicken, and Harry A. Atwater. "A Phase Diagram of Low Temperature Epitaxial Silicon Grown by Hot-wire Chemical Vapor Deposition for Photovoltaic Devices" in *Amorphous and Nanocrystalline Silicon Science and Technology*-2005, (Mater. Res. Soc. Symp. Proc. 862, Warrendale, PA, 2005). **Chapters 1 and 3.**

7. **Christine Esber Richardson**, M.S. Mason and Harry A. Atwater. "A Phase Diagram for Morphology and Properties of Low Temperature Deposited Polycrystalline Silicon Grown by Hot-wire Chemical Vapor Deposition." *Proceedings of the 31st IEEE Photovoltaics Specialists Conference.* Lake Buena Vista, FL. (2005) **Chapters 2 and 3.**

8. Brendan M. Kayes, **C.E. Richardson**, N.S. Lewis, and H.A. Atwater. “Radial PN Junction Nanorod Solar Cells: Device Physics Principles and Routes to Fabrication in Silicon.” *Proceedings of the 31st IEEE Photovoltaics Specialists Conference*. Lake Buena Vista, FL. (2005) **Chapters 7 and 8.**

9. **Christine E. Richardson**, Maribeth S. Mason, and Harry A. Atwater. "A Phase Diagram of Hot-wire CVD Epitaxial Si Films on Si (100) Substrates and Large-grained Polycrystalline Templates." *Proceedings of the 14th Workshop on Crystalline Si Solar Cells.* Winterpark, CO. (2004) **Chapters 3 and 7.**

10. **Christine E. Richardson**, Maribeth S. Mason, and Harry A. Atwater. "A Phase Diagram for Morphology and Properties of Low Temperature-Deposited Polycrystalline Silicon Grown by Hot-wire Chemical Vapor Deposition" in *Amorphous and Nanocrystalline Silicon Science and Technology*— 2004, (Mater. Res. Soc. Symp. Proc. 808, Warrendale, PA, 2004). **Chapters 3 and 7.**

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Chapter 1

Introduction

"Sooner or later we shall have to go directly to the sun for our major supply of power. This problem of the direct conversion from sunlight into power will occupy more and more of our attention as time goes on, for eventually it must be solved."

— Edison Pettit, Wilson Observatory, 1932

1.1 Thin-Film Si Photovoltaics: Motivation

The worldwide demand for photovoltaic power modules has grown by over 30% per year for the last six years.[1,2] This is a time of incredible opportunity for the growth of photovoltaics into a mainstream technology as well as the commercialization of novel technologies, as shown by the initial public offering of several solar companies including (in millions of US dollars) SunTech Power Holdings at $395.7 and SunPower Corporation at $138.6.[3] Venture capital firms in the United States have more than doubled their investment in solar energy in 2005 over 2004 by investing $67.6 million during its first three quarters.[4] The solar energy industry generated an estimated $12 billion in revenue in 2005 and is estimated to generate more than $36 billion in 2010.[5] "This is not just the most attractive space in the energy sector, but probably the most attractive space across equity markets, period," says Michael Rogol, global solar market analyst for CLSA Asia Pacific Markets.[4,5]

The main factor that limits the future growth and the mainstream acceptance of solar generated electricity is the cost per kilowatt hour (¢/kWh). While the cost per peak Watt ($/$W_P$) is the most commonly used metric for solar energy, the cost per kilowatt hour is the most demanding metric since it allows direct comparison between the cost of solar electricity and more traditional forms of residential electricity. A 1 kW_P system, which receives an average 5.5 hours of sunlight per day in a sunny location (*e.g.* Los Angeles) and an average of 2.5 hours of sunlight

per day in a cloudy location (*e.g*. Hamburg, Germany), would generate 1,600 and 750 kWh/year respectively.[6] The average retail price of electricity for residential use in February 2006 in the United States was 9.81¢/kWh up from the 8.97¢/kWh average in 2004, while in California the cost in February 2006 was 12.98 ¢/kWh, up from 11.75 ¢/kWh in 2005, and continues to rise almost monthly.[7] Currently, solar modules in the US retail at an average of $\$5.37/W_P$.[1] This is up from $\$4.96/W_P$ in April of 2004, due primarily to the limited amount of silicon feedstock. A solar module at $\$5.37/W_P$ in its 20 year lifetime[8,9] would generate electricity at 16.78 ¢/kWh in a sunny location as defined above, or at a cost of 3.8 ¢/kWh more than the average residential electricity rate in California, not including installation costs or subsidies. The silicon supply issue should resolve itself during the next few years. This will allow retail prices to drop to 2004 values or below,[5] and drop the cost of solar generated electricity to 15.5 ¢/kWh. However, to increase demand beyond markets such as Germany and Japan, which have liberal feed-in subsidies in place,[10] the cost per peak watt, not including the installation and the balance of systems costs, needs to decrease down to $\$1.00/W_P$. At this module price, a solar installation, including installation and balance of systems costs, could pay for itself in approximately 5 years without subsidies.[11]

The solar industry can get to $\$1.00/W_P$ by either increasing efficiency or by decreasing manufacturing costs. Solar cell efficiency records for silicon devices as of the end of 2005 are listed in Table 1.1.[12] Because of the large knowledge and experience base of working with silicon, most competitive cell designs are based upon this material.[13] The thermodynamic detailed balance model[14,15] calculates the maximum efficiency for a single junction solar cell using AM1.5 radiation at 31% and a band-gap of 1.35 eV. Si is almost ideally matched to the solar spectrum, with a band-gap of 1.1 eV and a theoretical maximum efficiency of 29%. The current record for silicon technology is almost 25% (Table 1.1). If additional forms of losses are included in the calculation of the theoretical efficiency limit such as the bulk recombination, surface recombination, losses at the contacts, and optical losses, then the practical limit of silicon

appears to be an efficiency of 25%, which the photovoltaic community has already achieved at the research level.[16] Therefore, the cost of manufacturing solar cells must be decreased. One method of doing this is through thin-film crystalline silicon technology. This route has the potential to blend the high efficiency of crystalline silicon with the low-cost of thin-film technology.

Si Classification	Si Thickness	Efficiency (%)	Area (cm^2)	V_{oc} (mV)	J_{sc} (mA/ cm^2)	FF (%)	Description
Crystalline	260 μm	24.7±0.5	4.00	706	42.2	82.8	UNSW PERL[17]
Multicrystalline	99 μm	20.3±0.5	1.002	664	37.7	80.9	FhG-ISE[18]
Thin-film Transfer	45 μm	16.6±0.4	4.017	645	32.8	78.2	University of Stuttgart [19]
Large-grained Polycrystalline	2-10 μm	15%	-	550-650	30-35	80	Target values
Nanocrystalline	2 μm	10.1±0.2	1.199	539	24.4	76.6	Kaneka[20]
Amorphous	i-layer ~250 nm	9.5±0.3	1.070	859	17.5	63	U. Neuchatel[21]

Table 1.1: Silicon solar cell efficiency records of various silicon technologies, along with the target values for an epitaxially thickened large-grained polycrystalline Si device.

Thin-film technologies allow one to separate the electrically active and mechanically supportive material by depositing the active silicon thin-film onto a low-cost substrate. With this technology, the greatest reduction in cost is due to the reduction in silicon. Half of the costs associated with traditional crystalline silicon solar cells, which currently account for 93% of the market,[1] are due to the silicon wafer itself. Scrap silicon from the semiconductor industry, the main source of silicon for the photovoltaic industry up until a few years ago, was available for $25/kg in 2003. But with demand increasing, the photovoltaics industry now pays for non-scrap Si at $50/kg.[22] Moreover, even though the Si feedstock capacity has increased by 12% over the last year, because of the increase in demand for silicon due to the growing photovoltaic industry,

prices have still increased by 25%.[23] In contrast, a thin-film silicon cell can be fabricated from a gas precursor such as silane. Silane formation is an intermediate step in the production of solar-grade material and so is less expensive than solar-grade silicon. Silane may also be recycled, increasing the material utilization and decreasing the manufacturing cost.[24] Moreover, a traditional silicon cell is typically 20 to 100 times thicker than a thin-film device deposited on a non-Si substrate due to the need for some form of mechanical support. By depositing a thin-film of silicon on a low-cost substrate, one can decrease the material costs even further, and perhaps even take advantage of this step by depositing on building materials, such as window glass or roofing tiles, to decrease installation and material costs.

The lowest-priced modules currently on the market are thin-film modules, either a-Si or CdTe based. For example, in April 2006, the lowest retail price for a monocrystalline module was \$4.16/W_P; the lowest retail price for a multicrystalline silicon module was \$4.05/W_P; and the lowest thin-film module price was \$3.80/W_P.[1] However, there are several advantages to pursuing a large-grained polycrystalline silicon device over other types of thin-film solar cells. Due to the cadmium in the CdTe cells, they are currently facing heavy regulation in the European Union.[25] Currently, United Solar LLC has a commercial a-Si based tripe junction module (a-Si and a-SiGe of two different Ge contents) with 9.5% module efficiency.[26] Large-grained polycrystalline silicon solar cells on glass, with grain sizes greater than the thickness of the cell, have the potential to have efficiencies on par with multicrystalline silicon efficiencies of 15% (Table 1.1).

There are several strategies to pursuing crystalline Si thin-films on glass substrates. One involves the crystallization of the entire amorphous silicon device by metal induced crystallization. With this technique, the metal reduces the energy and temperature necessary to crystallize the film. Typically, the grain-size is determined by the distance between nucleation sites. This method has recently been commercialized by CSG Solar.[27] They have achieved small module efficiencies of 9.4% for a 95 cm^2 module.[27]

Currently the Hahn-Meitner-Institut[28] and the University of New South Wales[29] are working on large-grained templates crystallized by aluminium. This provides the cell with a *p*+ doped template, since aluminum acts as an acceptor in silicon. With this type of template, the aluminium and amorphous silicon layers exchange places, leaving a crystalline silicon film with an Al/Si layer on top.[30] This layer must be removed and polished by a chemical or mechanical method. The template is then epitaxially thickened at deposition temperatures between 580-600°C, which is still compatible with a low-cost glass substrate.[29,31] The University of New South Wales has achieved a 3% efficient un-textured cell with a maximum open-circuit voltage of 441 mV.[31] Current limits to the efficiency of this class of devices include contact design;[16] the intra-granular defects of the template;[32] the passivation of defects, interfaces, and surfaces;[33,34] and light trapping which will be discussed in detail in Chapters 5 and 6.[27]

The strategy pursued in this thesis begins with a large-grained polycrystalline template formed by nickel induced crystallization fabricated on low-cost substrates, such as glass (Fig. 1.2). This gives the added flexibility of being able to have an *n*+-type template and does not require any further smoothening steps after crystallization. The layer is then epitaxially thickened with an *n*-type layer grown by hot-wire CVD. With this technique, twinned epitaxial films greater than 6 μm thick have been grown on Si (100) substrates at substrate temperatures of 230°C.[35] Then a *p*+ emitter can be deposited by HWCVD or formed by an Al anneal (Fig. 1.2).

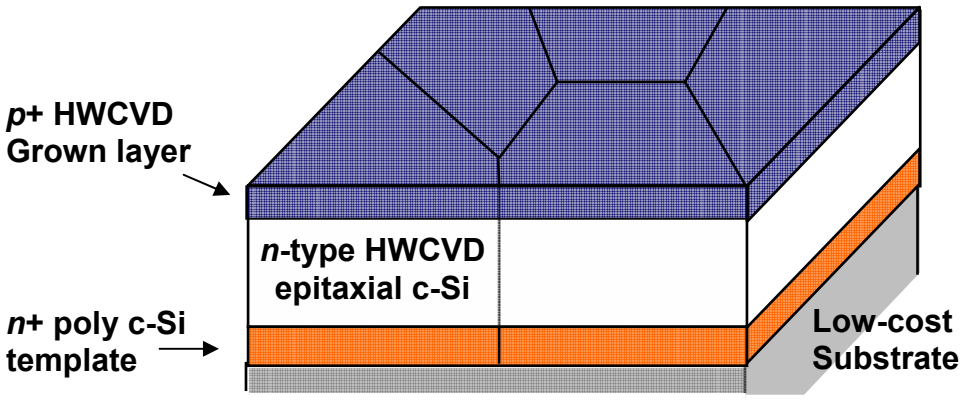

Figure 1.1 Schematic of a large-grained polycrystalline thin-film photovoltaic device.

1.2 Organization of this Thesis

This thesis is organized first with a brief introduction into the photovoltaics market, the drive for thin-film solar cells, and the current status of large-grained polycrystalline devices. Chapter 2 is a summary of hot-wire chemical vapor deposition, including the advantages and disadvantages of using this technique. Chapter 3 follows with the interesting low-temperature epitaxial growth regime that HWCVD enables under conditions of high hydrogen dilution. The possible mechanisms for this growth regime are then discussed by looking at the unique surface morphology and structural evolution of these films in Chapter 4. Chapter 5 is a brief introduction into photovoltaic devices, including specific design concerns for thin-film devices. Chapter 6 discusses the optical and electrical properties of HWCVD epitaxial films. Chapter 7 discusses the electrical results of devices made from epitaxially thickened large-grained polycrystalline templates. Future research directions that would take advantage of the unique film morphologies and structures, along with a brief conclusion of this thesis are in Chapter 8.

1.3 References

1. www.solarbuzz.com, (April 2006).

2. Strategies Unlimited, Global Analysis of Photovoltaic Markets - 2000 - Applications, Geographic Distribution, and Growth Patterns, 2001.

3. www.ipohome.com.

4. Solar Electric Power Association, www.solarpowerconference.com, (2006).

5. M. Rogol and B. Fisher, Sun screen II: Investment opportunities in Solar, 2005.

6. www.solarbuzz.com, (2002).

7. Energy Information Administration, Electric Power Annual with data for 2004, 2005.

8. Solar modules are guaranteed for at least 20 yrs. The efficiency of the modules degrades on average 0.5% per year. Other components included in the balance of systems may fail at a more frequent rate.

9. J. H. Wohlgemuth, D. W. Cunningham, P. Monus, J. Miller, and A. Nguyen, Proceedings of the 4th IEEE WCPEC, Waikoloa, HI, 2006.

10. V. Jimenez, (Earth Policy Institute, 2004).

11. Lewis M. Fraas, *Path to Affordable Solar Electric Power & the 35% Efficient Solar cell*. (2003).

12. M. A. Green, Progr. Photovolt. **14** (1), 45 (2006).

13. M. A. Green, Proceedings of the 4th IEEE WCPEC, Waikoloa, HI, 2006.

14. W. Shockley and H. J. Queisser, J. Appl. Phys. **32** (3), 510 (1961).

15. C. H. Henry, J. Appl. Phys. **51** (8), 4494 (1980).

16. R. M. Swanson, Proceedings of the 31st IEEE PVSC, Lake Buena Vista, FL, 2005.

17. J. Zhao, A. Wang, M. A. Green, and F. Novel Ferrazza, Appl. Phys. Lett. **73**, 1991 (1998).

18. O. Shultz, S. W. Glunz, J. C. Goldschmidt, H. Lautenschlager, A. Leimenstoll, E. Scheiderlochner, and G. P. Willeke, Proceedings of the 19th European Photovoltaic Solar Energy Conference, Paris, 2004.

19. R. B. Bergmann, T. J. Rinke, C. Berge, J. Schmidt, and J. H. Werner, Proceedings of the 12th PVSEC, Chefju Island, Korea, 2001.

20. K. Yamamoto, M. Toshimi, T. Suzuki, Y. Tawada, T. Okamoto, and A. Nakajima, Proceedings of the Materials Research Society Spring Meeting, San Francisco, 1998.

21. J. Meier, J. Sitznagel, U. Kroll, C. Bucher, S. Fay, T. Moriarty, and A. Shah, Thin Solid Films **451-452**, 518 (2004).

22. M. S. Keshner and R. Arya, Study of Potential Cost Reductions Resulting from Super-Large-Scale Manufacturing of PV Modules, 2004.

23. Solar Buzz LLC, (2006).

24. M. S. Keshner and R. Arya, Study of Potential Cost Reductions Resulting from Super-Large-Scale Manufacturing of PV Modules.

25. E. Iritani, *Europe Pushes Tech Into Detox* in the Los Angeles Times Issue, Date.

26. United Solar LLC, Technical Brief, 2004.

27. P. A. Basore, Proceedings of the 4th IEEE WCPEC, Waikoloa, HI, 2006.

28. W. Fuhs, S. Gall, B. Rau, M. Schmidt, and J. Schneider, Solar Energy **77**, 961 (2004).

29. A. G. Aberle, A. Straub, P. I. Widenborg, A. B. Sproul, Y. Huang, and P. Campbell, Prog. Photovolt: Res. Appl. **13**, 37 (2005).

30. J. Schneider, J. Klein, A. Sarikov, M. Muske, S. Gall, and W. Fuhs, MRS Proceedings **A2.2** (2005).

31. A. G. Aberle, Proceedings of the 4th IEEE WCPEC, Waikoloa, HI, 2006.

32. Claudine M. Chen, "*Polycrystalline Silicon Thin Films for Photovoltaics,*" California Institute of Technology, 2001.

33. C. E. Richardson, Y.-B. Park, and H. A. Atwater, Proceedings of the 4th IEEE WCPEC, Waikoloa, HI, 2006.

34. B. Rau, I. Sieber, B. Selle, S. Brehme, U. Knipper, S. Gall, and W. Fuhs, Thin Solid Films **451-452**, 644 (2004).

35. C. E. Richardson, B. M. Kayes, M. J. Dicken, and H. A. Atwater, Amorphous and Nanocrystalline Silicon Science and Technology. Symposium A. (Materials Research Society Symposium Proceedings Vol. **862**), 171 (2005).

Chapter 2

Hot-Wire Chemical Vapor Deposition

2.1 Advantages of HWCVD

Hot-wire chemical vapor deposited (HWCVD), or catalytic-CVD, is a thin-film growth technique in which gaseous precursors, i.e., silane and hydrogen, catalytically and thermally decompose on a hot filament at 1200-2000°C. The precursors are then deposited onto a substrate typically heated by an external heat source or by the hot filament itself to temperatures between 200-600°C (Fig. 2.1). This technique is a low-cost alternative to the current standard in thin-film deposition, plasma-enhanced CVD (PECVD). HWCVD has several advantages over more traditional deposition techniques like PECVD and MBE: in addition to costing less, HWCVD causes less ion-induced damage than PECVD.[36,37] The thermal radical species decomposed by HWCVD have energies of only ~0.2 eV, while in PECVD, ions are produced and then are often accelerated towards the substrate. HWCVD also offers high deposition rates of up to 5 nm/s,[38] and the uniformity of the deposited film can be increased by increasing the number of filaments. The catalytic filament dissociates precursors very efficiently,[39] and creates a growth in a high H atmosphere, which makes it a great tool for the surface and bulk passivation of films. The hydrogen can also aide in the growth of low-temperature crystalline and epitaxial films as discussed in Chapters 3 and 4. A survey of recent work on the passivation of solar cells by HWCVD films has covered HWCVD H-rich SiN, which passivated defects in silicon more effectively than PECVD SiN by acting as a hydrogen source;[40] HWCVD amorphous silicon used as a surface passivation layer and emitter in the HIT cell;[41] and short HWCVD hydrogen treatments for the passivation of surfaces before junction formation[41] and for the passivation of

defects in the bulk and at the grain boundaries.[42,43] The beneficial passivation properties of HWCVD films are due to the high-H content resulting from the high gas utilization of HWCVD. By depositing Si at temperatures below 350°C, hydrogen can be incorporated into the bulk to passivated defects and grain boundaries.[31,44] This chapter addresses several important issues in optimizing HWCVD for low-temperature epitaxial growth of silicon films including filament material and filament temperature choice, contaminant minimization, gas precursors and deposition species, and doping efficiency.

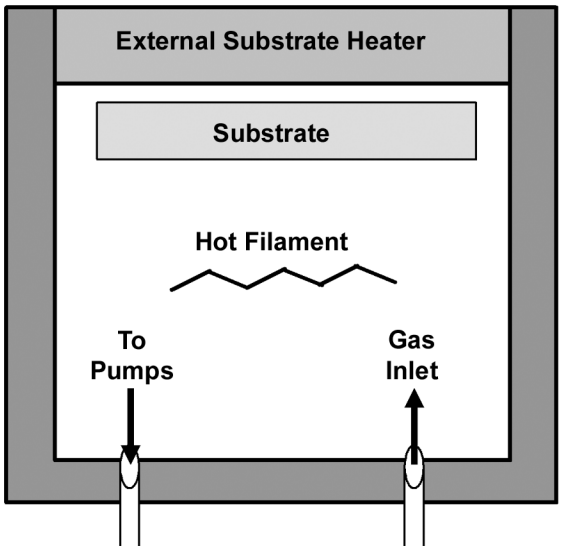

Figure 2.1 Schematic of HWCVD chamber used for Si deposition.

2.2 Choice of Filament Material and Temperature

The choice of filament is critical for HWCVD as the technique involves catalytic decomposition of the precursors. Several materials have been investigated as possible hot-wire candidates. The tradition material of choice is tungsten. Above ~1500°C, W has a high cracking coefficient of 0.7 for SiH_4, which provides for high gas utilization.[45] More recently, other materials have come into favor, such as tantalum and graphite in order to access a wider range of filament temperatures[46] and decrease contamination from the filament respectively. Groups such as the Silicon Materials and Devices group at NREL recently switched to tantalum wires because

tantalum filaments produced larger critical epitaxial film thicknesses than tungsten filament-grown films under the same deposition conditions.[46] This is most likely due to the fact that the tungsten silicide is more stable than the tantalum silicide at higher temperatures.[46] The silicide reduces the reactivity of the filament; and when the silicide cannot form, the cracking coefficient does not decrease during silane exposure. The drawbacks of tantalum filaments are that tantalum is more expensive per meter than tungsten and that tantalum wires begin to sag when heated, causing additional complications for the design of a hot-wire assembly, including shorting and trouble maintaining a constant wire-to-substrate distance.

The temperature of the filament is also very important, because it determines the species coming off the filament, and hence the deposition species. Above ~1500°C, the dominant species off of the filament is Si.[47,48] Most of our depositions are above this temperature in order to ensure the efficient dissociation of precursors, and also to prevent a silicide from forming on the filament and decreasing the deposition rate.[49] At lower temperatures and with aged wires, SiH_3 and SiH_2 begin to dominate.[39,47,50] This decreases the deposition rate, and increases the mobility of atoms on the surface and will be discussed in more detail in Chapter 4.

The choice of filament temperature and material is also extremely influential in determining the amount of contamination in the film. There appears to be a trade off in terms of higher filament temperatures and the high dissociation of precursors, with lower filament temperatures and lower contamination levels.

2.2.1 Graphite filaments

Graphite filaments are relatively new to the hot-wire CVD community. They have been used to grow columnar (220) polycrystalline films, which have greater stability than comparable films grown with tantalum wires.[51,52] Moreover, secondary ion mass spectrometry (SIMS) measurements illustrate that at equivalent wire temperatures, substrate temperatures, and wire-to-substrate spacings, graphite filaments do not contaminate the film with more carbon than do tungsten filaments; both have a carbon concentration between $2x10^{20}$ and $10x10^{20}$ atoms/cm^3

(Fig. 2.2). Moreover, if contamination from the filament does occur, C does not have as much of a detrimental effect on the efficiency of a solar cell as do more traditional materials like Ta and W (Fig. 2.3).

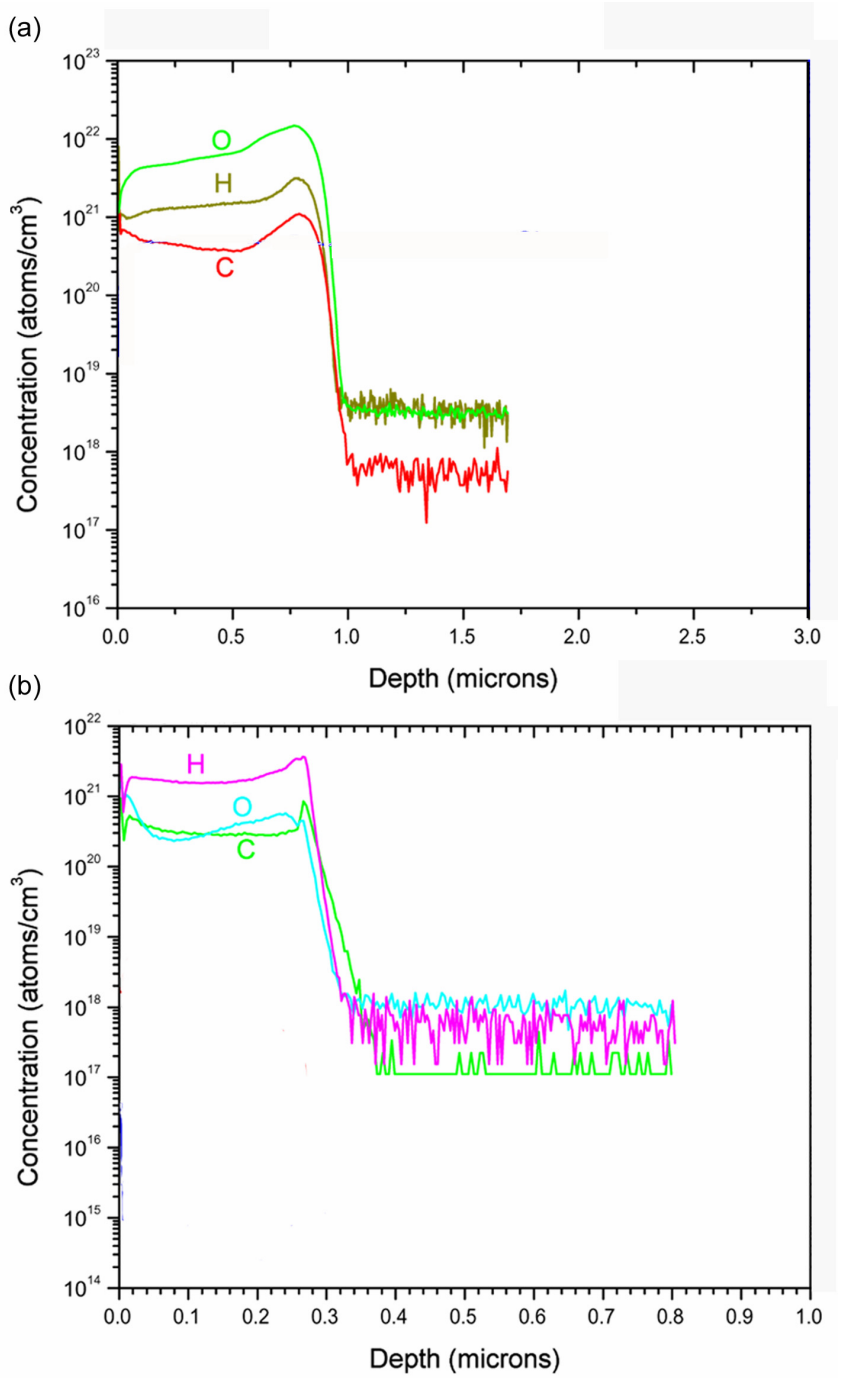

Figure 2.2 SIMS analysis of (a) Si film deposited with two tungsten wires. (b) Si film deposited with two graphite wires. Both depositions used a wire temperature of 1500°C, substrate-to-wire spacing of 5.5 cm, and substrate temperature set to 400°C. The carbon content in both films is equivalent.

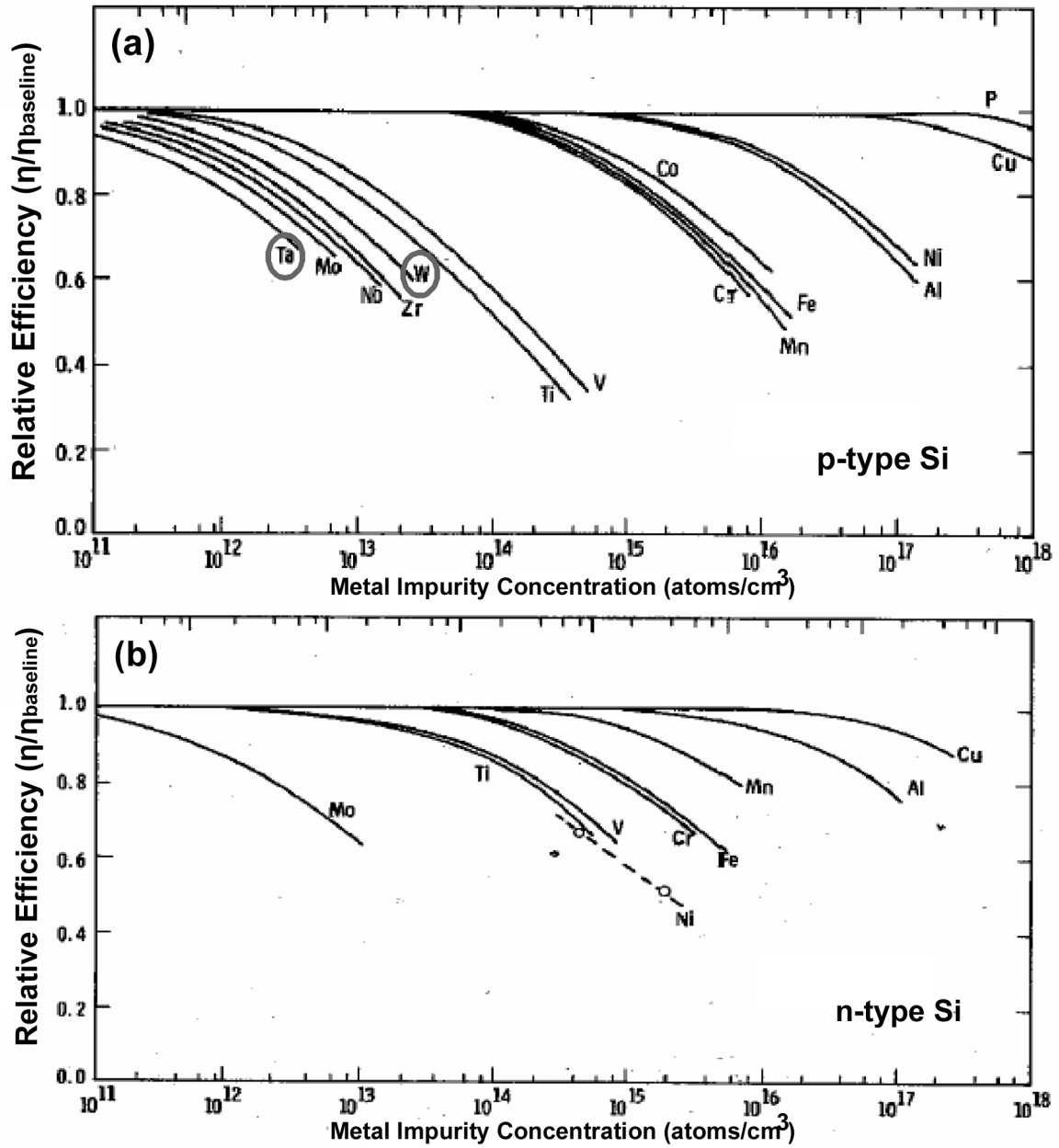

Figure 2.3 The relative efficiency of silicon solar cells contaminated with increasing concentrations of metallic impurities for (a) *p*-type Si and (b) *n*-type Si from Davis *et al.*[59]

However, there are several potential drawbacks to using graphite filaments. One potential drawback of using graphite filaments is that their higher resistivities require more power to bring the wires up to the same current and temperature as W and Ta filaments. This high power requires that the chamber be conditioned by a short deposition to coat all of the stainless steel and ceramic parts of the assembly in order to minimize the contaminants from these

components incorporating into the film. However, a conditioning step is often the standard procedure with metallic filaments as well, since their composition and precursor cracking efficiencies change during their useful lifetime.[39]

The most significant drawback of using graphite filaments is that within the deposition regime of high hydrogen dilution and low wire temperatures, after a critical thickness, the deposition rate decreases dramatically. Table 2.1 summarizes the experimental data of three HWCVD films growths using two graphite filaments at a total gas pressure of 100 mTorr and a wire to substrate spacing of 5.5 cm. With increasing deposition time, the film thickness does not increase, but the open circuit voltage and hence, the device quality, increases (Table 2.1). Figure 2.4 is a transmission electron microscopy (TEM) cross-sectional image at a magnification 614 kx of the films from Table 2.1 with run numbers 213 (751 min.) and 214 (1323 min.). It is difficult to draw definitive conclusions from these micrographs. The twinned epitaxial regions of these films appear to grow with increasing deposition time, possibly through a restructuring method similar to the abstraction and redeposition growth mechanism discussed in detail in Chapter 4. The dramatic decrease in deposition rate is most likely due to the changing filament chemistry during deposition, especially at low filament temperatures such as 1400°C. At this temperature, SiC can form on the graphite filament, especially near the wire clamp which is much cooler than the center of the filament (Fig. 2.5). The formation of SiC is confirmed by energy dispersive X-ray spectroscopy (EDS) where almost equal amounts of Si and C were detected on the surface of the graphite filament near the wire clamp. This coating would decrease the cracking efficiency of the graphite filament or reduce the filament temperature even further. Growths at higher filament temperatures may prevent a SiC layer from forming, but investigations into this regime are currently limited by the power supply on the deposition chamber. Because of these reasons, tungsten filaments are predominantly used in our HWCVD depositions. However, graphite filaments should not be discounted. Studies need to occur at higher filament temperatures in order to accurately assess the technology.

2.2.2 Tungsten filaments

There has been a wide acceptance of tungsten wires as the heated catalyzer in HWCVD. This is primarily due to encouraging results in the a-Si community for dense, well-passivated, device quality amorphous and microcrystalline silicon thin-films.[39,53-56] However, there is little written about large-grained polycrystalline films and even less about epitaxial HWCVD grown films. The main groups working on this subject are at the National Renewable Energy Laboratory (NREL) and the California Institute of Technology (Caltech). Each group deposits epitaxial films in a unique deposition regime dictated in large part by the partial silane pressure during growth[57] of epitaxial growth with amorphous or with polycrystalline breakdown respectively.[46,52,58]

Run no.	Substrate Set Temp (°C)	Wire Temp (°C)	5ppm PH_3 in 5.12% SiH_4 in Ar (sccm)	H_2 (sccm)	R = H_2/ SiH_4	Dep Time (min)	Film thickness (nm)	Dep rate (nm/ min)	V_{oc} (mV)
211	350	1400	10.1	100.2	194	280	150	0.54	202
213	400	1400	10.2	100.1	192	751	100	0.13	256
214	350	1425	10.1	100.1	194	1323	150	0.11	365

Table 2.1: Process conditions and experimental results from three films grown using graphite filaments using a low filament temperature to reduce contamination.

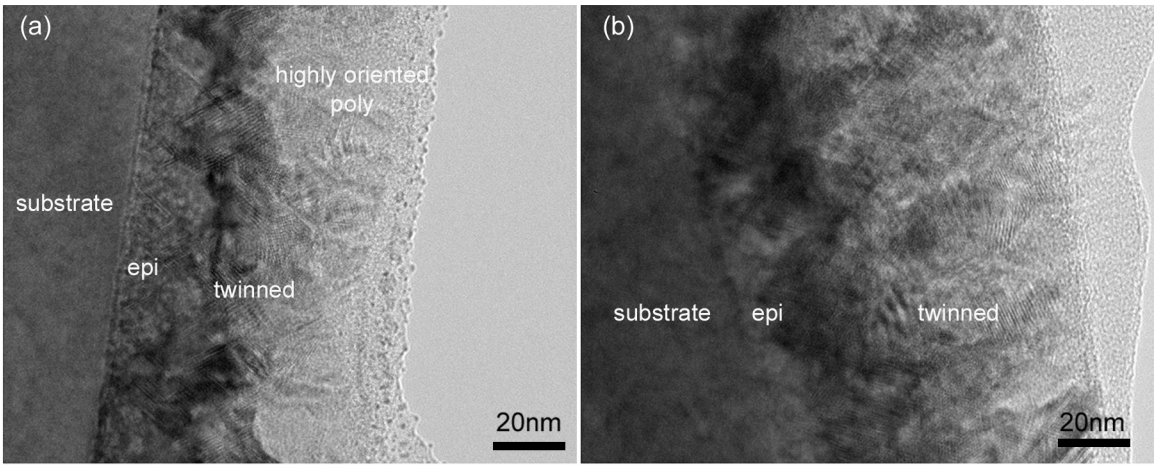

Figure 2.4 TEM cross-sectional images at 614 kx magnification of HWCVD graphite filament grown films at deposition times of (a) 751 minutes and (b) 1323 minutes corresponding to run numbers 213 and 214 of Table 2.1.

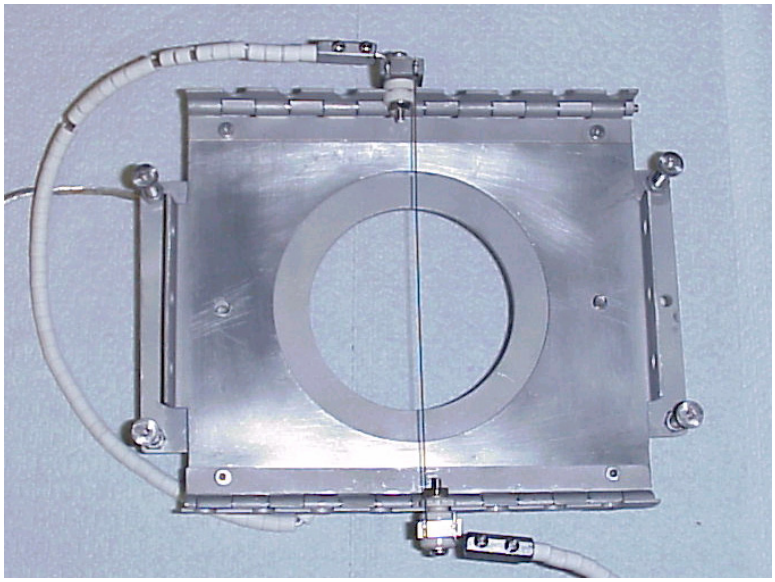

Figure 2.5 Photograph of the HWCVD wire assembly. Two electrical leads are passed through a vacuum feed-through into the chamber. The electrical leads are then isolated by ceramic spacers. The lead is then locked into a double clamp with the filament. The clamp is electrically isolated from the base plate with ceramic spacers.

2.3 Sources of Contamination in HWCVD

An unexpected source of contamination in our system was the filament assembly itself (Fig. 2.5). High levels of Fe, Cr, Ni, W, and Ta were found in silicon films deposited with both W and Ta filaments at levels of $1x10^{16}$ to $2x10^{21}$ cm^{-3} at surprisingly low filament temperatures of 1450-2000°C, and wire-to-substrate spacings between 2.5 and 6 cm. Figure 2.6 compares the contamination in films grown with W and Ta filaments in a stainless steel assembly at 1600-1700°C. The amount of W or Ta in these films is enough to drop the efficiency in a silicon solar cell to near zero (Fig. 2.3).[59] In fact, these contaminants can ruin a device at contamination levels below the detection limit of SIMS.[60] To decrease the amount of W and Ta in the film, the substrate to wire distance was set to 5 cm; and the filament temperature decreased to approximately 1500°C.

Even at lower filament temperatures, a high amount of Fe, Cr, C, and Ni were incorporated into the film. The source of these contaminants is predominantly the wire clamps which were also at high temperatures (Fig. 2.5). In order to eliminate this source of

contamination, any stainless steel part which carried current and was not shielded by a ceramic spacer was replaced with a Ta or Mo replica due to the low vapor pressure of these materials at high temperatures (Fig. 2.7).[61] Ta foil shields were also effective at preventing contamination, but were not very robust. Tungsten would have been the material of choice, however it is extremely difficult to machine.

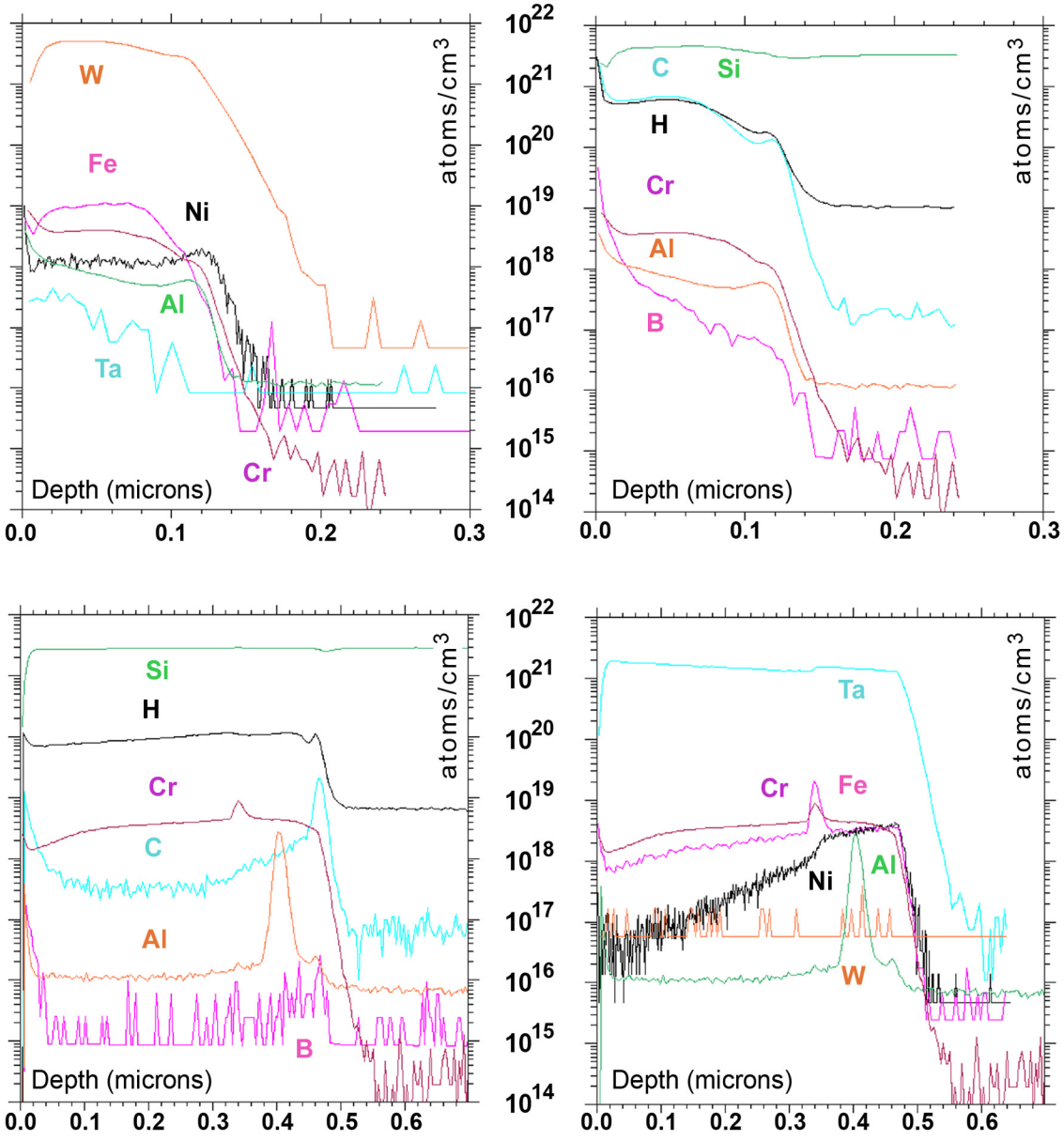

Figure 2.6 SIMS data of two samples (top) grown with a tungsten filament at 1700°C and (bottom) grown with a tantalum filament at 1600°C at a wire to substrate distance of 2.5 cm. Note the high levels of W and Ta along with the elements that compose stainless steel.

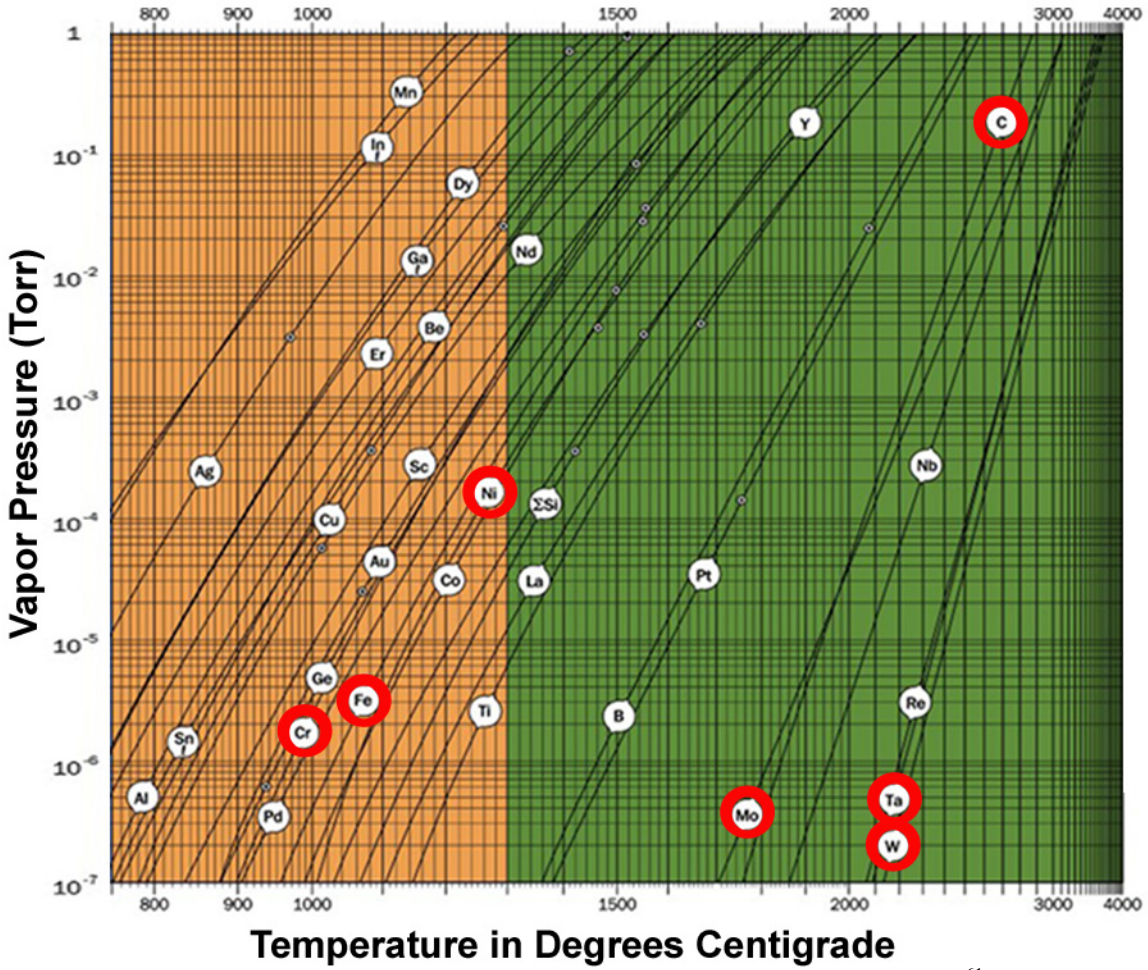

Figure 2.7 Vapor pressures of the elements at high temperatures from Honig.[61] Materials of interest, W, Ta, C, Mo, Ni, Fe, and Cr, are circled in red.

2.4 Gas Precursors and Deposition Species

We have targeted the growth regime of high hydrogen dilution conditions that lead to epitaxial growth with a breakdown to polycrystalline growth. The main species desorbed from the wire at wire temperatures above ~1400-1500°C is Si.[47,48] At low total pressures, Si diffuses un-reacted to the surface; however, at higher total pressures above several mTorr and under deposition conditions of hydrogen dilution, gas phase reactions into the deposition species of SiH_3 and SiH occur[36] and SiH_3 becomes the primary deposition species.[36,39] The sticking probability of atomic Si is near unity and leads to the surface roughening of most films. SiH_3 can diffuse on a hydrogenated surface, like Si (100) at temperatures of 350°C and below, before being

incorporated, which gives rise to smoother surfaces.[62] These effects will be discussed further in Chapter 4. In addition, under conditions of high hydrogen dilution at low-temperatures, the deposition rate, or throughput, does not decrease with decreasing substrate temperature or increased hydrogen dilution, improving the manufacturability of the HWCVD process.

2.5 Dopants

Previous studies have shown that the crystallinity of a silicon thin-film decreases when boron-containing precursors are added, but that the addition of phosphine increases the crystallinity.[63] Low-temperature epitaxial films have a much larger process window and greater epitaxial thicknesses when grown *n*-type rather than *p*-type.[64] This could be due to the faster deposition rate of films with boron dopants as opposed to phosphorous dopants, which increases the disorder in the film.[65] Table 2.2 summarizes the deposition parameters for two films grown by HWCVD. The growth rate for films grown with 5% silane in argon containing 5 ppm trimethylboron (TMB) was three times faster than that for films grown with 5ppm phosphine (PH_3). The difference in growth rate is most likely due to the difference in the adsorption mechanisms of PH_3 and B_2H_6 on Si (100) surfaces. Yu *et al.* found that phosphine adsorbs non-dissociatively while B_2H_6 dissociates into an amorphous layer of B on the surface.[66] The non-dissociative adsorption of phosphine is believed to block growing species from the silicon growth surface.[67,68] Moreover, the sticking coefficient of phosphine is near unity, so this would increase the effect of the blocking mechanism of phosphine for incoming Si deposition species. For a good review of quenched and enhanced growth due to dopant incorporation, see Mehta and Tao.[69]

In addition, it is easier to activate *n*-type dopants than *p*-type dopants. The doping efficiency of PH_3 is much higher than that of TMB for HWCVD at low-temperatures.[70] For example, the resistivity of a *p*-type film grown with TMB at a wire temperature of 1500°C with a hydrogen dilution ratio close to 100 is too high to measure the carrier concentration by spreading

resistance. Therefore, the carrier concentration must be less than 10^{12} cm^{-3}. In contrast, an *n*-type film grown with PH_3 has a carrier concentration of 10^{14} cm^{-3} ± 20% under the same deposition conditions (Fig. 2.4). Note, however, that since these films are sometimes polycrystalline, the resistance is an inclusive property of the grains and the bulk and therefore, the actual doping concentration may not be accurate.

To increase boron activation, additional hydrogen and a higher filament temperature are needed.[63,70] High filament temperatures may cause an increase in the incorporation of tungsten from the hot filament into the film. This is a problem, since the film will serve as the active region of our solar cell device and tungsten is a major lifetime killer in silicon (Fig. 2.6).[59,60] This is another reason to pursue devices with *n*-type active regions over those with *p*-type regions; *n*-type silicon is more resilient to defects than *p*-type silicon.[59]

The concentration of active dopants versus the concentration of all dopant atoms is low in our HWCVD grown films due in part to the relatively low wire temperatures used to grow these films, 1350-1500°C, as opposed to typical wire temperatures of 2000°C. However, these low temperatures are required to minimize the metal contamination in the growing film from the hot filament (Fig. 2.5). The dopant activation can be increased by post-deposition dopant anneals.[71]

Run no.	Substrate Set Temp (°C)	Wire Temp (°C)	5ppm TMB in 5.11% SiH_4 in Ar (sccm)	5ppm PH_3 in 5.12% SiH_4 in Ar (sccm)	H_2 (sccm)	R = H_2/ SiH_4	Dep Time (min)	Film thickness (nm)	Dep rate (nm/ min)
204	400	1475	-	19.8	100.4	99	279	500	1.79
206	400	1500	20.7	-	100.4	95	316	1700	5.38

Table 2.2: Process conditions and experimental results of two films grown using tungsten filaments with different dopants introduced during deposition.

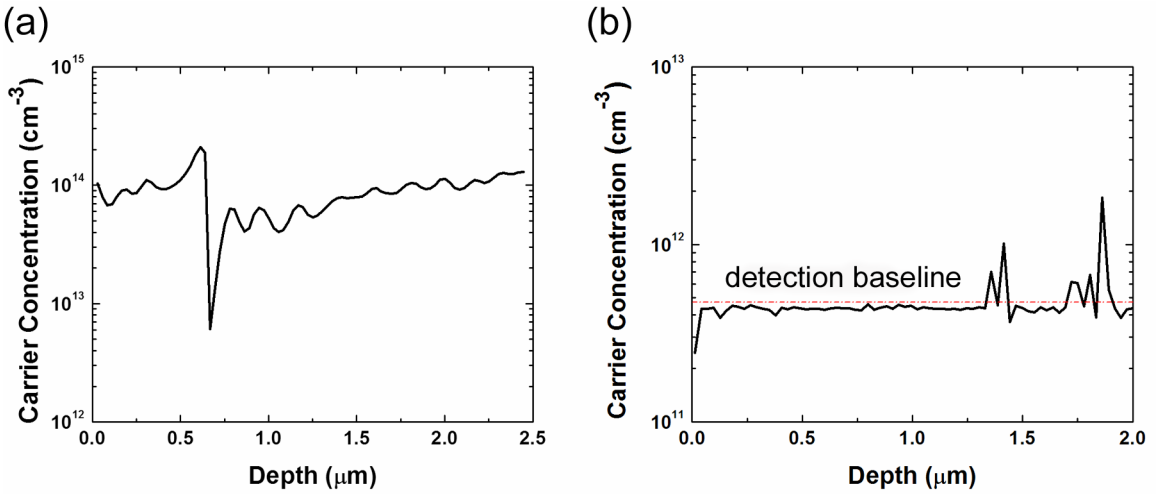

Figure 2.8 Spreading resistance of films grown under the same deposition conditions with (a) PH_3 (sample 204) and (b) TMB (sample 206). Note the resistance of sample 206 is too low to measure.

Dopant segregation during epitaxial growth has traditionally been a problem in molecular beam epitaxy (MBE) grown films due to low incorporation probabilities.[72] However, at temperatures below 500°C,[73] the ability of the dopants to segregate decreases and results in a more uniform dopant incorporation preferable for photovoltaic devices.[74] We find higher levels of activation with lower deposition pressures consistent with previous results for very low pressure chemical vapor deposition.[75]

2.6 Conclusions

HWCVD is an interesting technique for the low-temperature growth of thin-film silicon. It offers efficient use of precursors, fast deposition rates, and high hydrogen passivation of defects. The choice of filament and its temperature are critical to the determination of the deposition environment and appropriate precautions must be taken in order to achieve high quality, contamination-free films. For the deposition regime of interest, low-temperature epitaxial growth, tungsten was the most reliable catalyst filament. Tungsten offers a large process window for *n*-type epitaxial films with high hydrogen dilution ratios of 0 to 480, but filament temperatures must be kept below 1600°C to prevent contamination in this system. Films with *n*-

type doping are easier to grow than *p*-type films at lower temperatures due in part to the high deposition rates of the latter. Moreover, during low-temperature growth, dopant non-uniformity issues observed during higher temperature growths are avoided.

2.7 References

1. R. E. I. Schropp, Thin Solid Films **451-52**, 455 (2004).

2. H. Matsumura, Jpn. J. Appl. Phys. **37**, 3175 (1998).

3. J. K. Rath, A. J. Hardeman, C. H. M. van der Werf, P. A. T. T. van Veenendaal, M. Y. S. Rusche, and R. E. I. Schropp, Thin Solid Films **430** (1-2), 67 (2003).

4. J. K. Holt, "*Hot-Wire Chemical Vapor Deposition of Silicon and Silicon Nitride for Photovoltaics: Experiments, Simulations, and Applications,*" California Institute of Technology, 2003.

5. M. Stavola et al., Proceedings of the 14th Workshop on Crystalline Si Cells and Modules, 2004.

6. T. H. Wang et al., Proceedings of the Proceedings of the 31st IEEE Meeting, 2005.

7. R. Brendel, R. B. Bergmann, B. Fischer, J. Krinke, R. Plieninger, U. Rau, J. Reiss, H. P. Srunk, H. Wanka, and J. H. Werner, Proceedings of the 26th PVSC, Anaheim, CA, 1997.

8. J. K. Rath, A. Barbon, and R. E. I. Schropp, J. Non-crys. Sol. **227**, 1277 (1998).

9. A. G. Aberle, Proceedings of the 4th IEEE WCPEC, Waikoloa, HI, 2006.

10. B. Rau, J. Schneider, E. Conrad, and S. Gall, Proceedings of the Mat. Res. Soc. Sym., San Francisco, 2006.

11. M. Swiatek J.K. Holt, D.G. Goodwin, R.P. Muller, W.A. Goddard III, Harry A. Atwater, Thin Solid Films **395**, 29 (2001).

12. C.W. Teplin, E. Iwaniczko, K. M. Jones, R. Reedy, B. To, and H. M. Branz, Mater. Res. Soc. Symp. Proc. **862**, A2.3 (2005).

13. K. Inoue, S. Tange, K. Tonokura, and M. Koshi, Thin solid Films **395**, 42 (2001).

14. H. Matsumura, Jap. J. Appl. Phys. **37**, 3175 (1998).

15. Jason K. Holt, Maribeth Swiatek, David G. Goodwin, and Harry A. Atwater, Journal of Applied Physics **92** (8), 4803 (2002).

16. J. J. C. Doyle, J. App. Phys. **64** (6), 3215 (1988).

17. M.B. Schubert K. Bruhne, C. Kohler, J.H. Werner, Thin Solid Films **395**, 163 (2001).

18. C. W. Teplin, Qi Wang, E. Iwaniczko, K. M. Jones, M. Al-Jassim, R. C. Reedy, and H. M. Branz, J. Crys. Growth **287** (2), 414 (2006).

19. K. F. Feenstra, R. E. I. Schropp, and W. F. Van der Weg, J. Appl. Phys. **85** (9), 6843 (1999).

20. R. E. I. Schropp, K. E. Feenstra, E. C. Molenbroek, H. Meiling, and J. K. Rath, Philos. Mag. B **76** (3), 309 (1997).

21. E. C. Molenbroek, A. H. Mahan, and A. Gallagher, J. Appl. Phys. **82** (4), 1909 (1997).

22. A. Gallagher, Thin Solid Films **395** (1-2), 25 (2001).

23. C.E. Richardson, Y.-B. Park, and H. A. Atwater, Phys. Rev. B **73** (24) (2006).

24. C. E. Richardson, M. S. Mason, and H. A. Atwater, Mater. Res. Soc. Symp. Proc. **808**, A8.11 (2004).

25. J. R. Davis, A. Rohatgi, R. H. Hopkins, P. D. Blais, P. Raichoudhury, J. R. McCormick, and H. C. Mollenkopf, IEEE Trans. Electr. Dev. **27** (4), 677 (1980).

26. S. Baumann, in *Outsourcing of Analysis: Choosing the Right Technique* (Evans Analytical Group).

27. R. E. Honig and D. A. Kramer, RCA Review **30**, 285 (1969).

28. T. Karabacak, Y.P. Zhao, G.C. Wang, and T. M. Lu, Phys. Rev. B **66** (7), 075329 (2002).

29. P. Brogueira, V. Chu, A. C. Ferro, and J. P. Conde, J. Vac. Sci. Technol. A **15** (6), 2968 (1997).

30. B. Rau, K. Petter, S. Brehme, I. Sieber, M. Stoger-Pollach, P. Schattschneider, K. Lips, S. Gall, and W. Fuhs, Proceedings of the 31st IEEE Photovoltaic Specialists Conference, Orlando, FL, 2005.

31. J. Thiesen, H. M. Branz, and R. Crandall, Appl. Phys. Letters **77** (22), 3589 (2000).

32. M. L. Yu, D. J. Vitkavage, and B. S. Meyerson, J. Vac. Sci. Technol. A **3** (3), 861 (1984).

33. Ming L. Yu and B. S. Meyerson, J. Vac. Sci. Technol. A **2** (2), 446 (1984).

34. F. Gao, D. D. Huang, J. P. Li, Y. X. Lin, M. Y. Kong, D. Z. Sun, J. M. Li, and L. Y. Lin, J. Crys. Grwth **220**, 461 (2000).

35. B. Mehta and M. Tao, Journal of the Electrochemical Society **152** (4), G309 (2005).

36. E. Iwaniczko (*personal communication*).

37. S. Lourdudoss, Appl. Phys. Lett. **64** (25), 3461 (1994).

38. H.-J. Gossmann, E. F. Schubert, D. J. Eaglesham, and M. Cerullo, Appl. Phys. Lett. **57** (23), 2440 (1990).

39. C. B. Arnold and M. J. Aziz, Physical Review B **72** (19) (2005).

40. E. Suvar, H. H. Radamson, and J. V. Grahn, Materials Science And Engineering B-Solid State Materials For Advanced Technology **89** (1-3), 314 (2002).

41. M. Sarret, A. Liba, O. Bonnaud, F. Le Bihan, B. Fortin, L. Pichon, and F. Raoult, IEE Proc.-Circuits devices Syst. **141** (1), 19 (1994).

Chapter 3

Low-Temperature HWCVD Epitaxial Growth

3.1 Epitaxial Growth – An Overview

Low-temperature silicon epitaxial growth is of great importance in thin-film technology, but it is often riddled with problems such as the breakdown of epitaxial growth to an amorphous phase and amorphous inclusions above a critical thickness.[76] Most of the literature on low temperature epitaxial growth stems from studies of molecular beam epitaxy (MBE). Eaglesham found that in MBE growth of epitaxial silicon films that the critical epitaxial thickness, h_{epi}, increases with substrate temperature as

$$h_{epi}=h_o\exp(E_{act}/k_BT) \qquad (3.1)$$

where T is the substrate temperature and breakdown is into an amorphous phase.[77]

Ever since, the low temperature epitaxial growth community has been working under the assumption that the critical epitaxial thickness increases with the substrate temperature and that epitaxial breakdown to an amorphous phase occurs for all growth techniques. However, in 2004 Mason *et al.* showed that the epitaxial thickness during low temperature HWCVD growth with H dilution *increases* with decreasing substrate temperature down to 300°C as determined by from reflection high energy electron diffraction (RHEED)[78,79] (Figs. 3.1 and 3.2) or by cross-sectional transmission electron microscopy (TEM).[78] Moreover, under these H dilution conditions, breakdown is always into a polycrystalline phase with micron size grains, in contrast to the results for HWCVD growth with pure silane.[80]

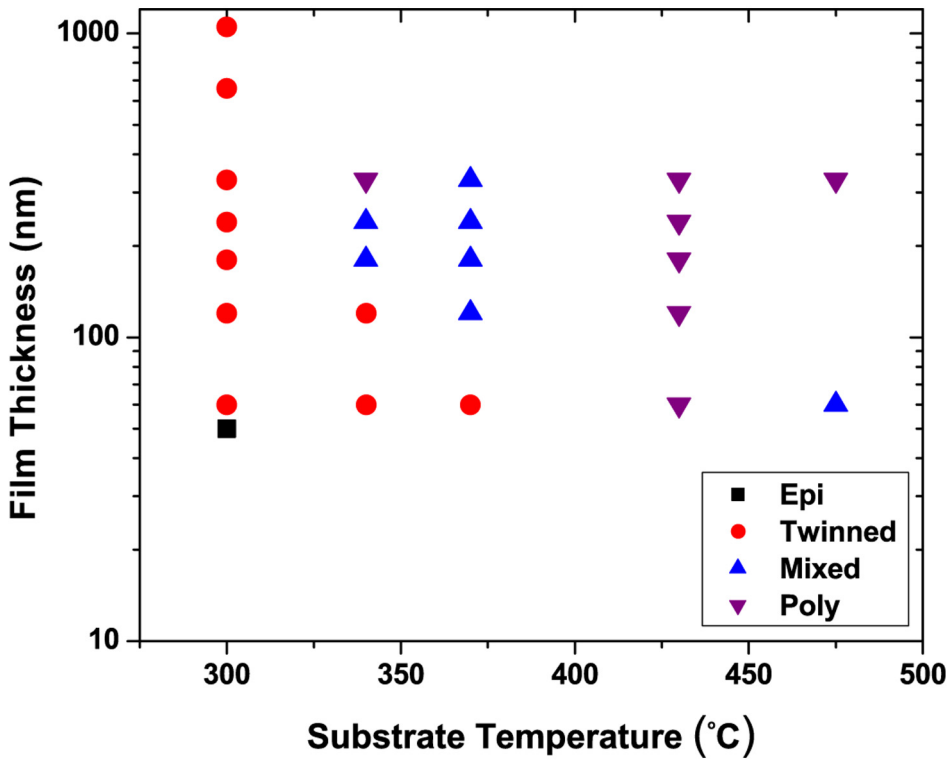

Figure 3.1 Phase diagram of the structure of HWCVD grown crystalline films with substrate temperature and thickness from Mason.[58,78]

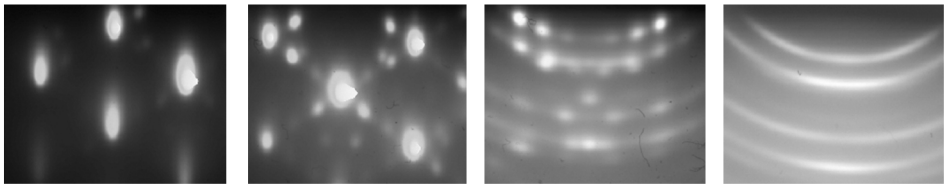

Figure 3.2 RHEED patterns demonstrating the definitions of epitaxial, twinned epitaxial, mixed, and polycrystalline films.

Epitaxial growth with HWCVD was first reported in 1997 by Theisen, with 100 nm of epitaxial growth on Si (100) at 250°C substrate temperature with epitaxial breakdown into an amorphous phase.[81] In 2000, Watahiki *et al.*[82] reported a critical epitaxial thickness of ~10 nm for HWCVD growth with substrate temperatures from 200-600°C evolving into a twinned epitaxial phase. At 15 mTorr SiH_4 partial pressure, they reported that the epitaxial quality increased with

decreasing substrate temperature for a set of 100 nm thick samples. However, no discussion was made of the optimal conditions for epitaxial growth or of growth mechanisms.[83]

Epitaxial growth with breakdown into a polycrystalline phase has also been seen in other growth techniques such as electron-cyclotron resonance chemical vapor deposition (ECRCVD) and pulsed magnetron sputtering. Using ECRCVD with a hydrogen to silane ratio, R, equal to 1 and a substrate temperature of 560°C, epitaxial growth on a variety of substrate orientations was studied.[34] On Si (311) substrates, epitaxial growth with conical polycrystalline regions of disorder at the substrate/film interface occurs; while for growth on Si (111) substrates, breakdown to a polycrystalline film occurred immediately.[34] At lower deposition temperatures of 325°C with R = 3, the same group found epitaxial breakdown to occur on Si (311) at 60 nm and on Si (111) at 35 nm.[76] The critical epitaxial thickness increases with a decrease in substrate temperature for the homoepitaxial growth of Si on (311) and (111) substrate orientations during ECRCVD.

In the sputtered films, the highest quality epitaxial films were deposited at substrate temperatures between 375 to 400°C, with more disorder occurring at higher and lower substrate temperatures.[84] However, the films remain epitaxial below 400°C, down to a substrate temperature of 100°C, and are completely polycrystalline at higher substrate temperatures of 450°C. The critical epitaxial thickness in these experiments could not be determined since the disorder increased monotonically with thickness and there was no abrupt critical epitaxial breakdown thickness.[84]

Although the deposition mechanisms in ECRCVD and pulsed magnetron sputtering are quite different than in HWCVD, the success of low-temperature epitaxial growth with polycrystalline breakdown means that both techniques are able to prevent amorphous inclusions from forming in the film by either physical or chemical methods.

This thesis deliberately focuses on conditions of high hydrogen dilution, which lead to epitaxial growth with polycrystalline breakdown. Table 3.1 summarizes the HWCVD growth conditions that have led to epitaxial or polycrystalline growth[85,86] and compares them to the

deposition conditions that lead to amorphous films[85,87] or epitaxial breakdown to an amorphous phase[46] on Si (100) substrates. Note that the shift from crystalline to amorphous films occurs with increasing silane partial pressure, and that epitaxial films with breakdown to any phase typically have a lower growth rate.

The role of hydrogen dilution in thin film Si chemical vapor deposition is not fully understood. Many studies have shown that hydrogen increases the crystallinity in films regardless of the deposition technique.[88,89] Robertson concluded that crystallinity originates through a direct solid state transformation, in microcrystalline Si (μc-Si) deposition, that causes crystalline nuclei to form due to the higher stability of the crystalline phase.[89] Hydrogen is also thought to play a substantial role in low-temperature epitaxy through its coverage of the growth surface.[90] In addition, hydrogen dilution plays an important role in the surface evolution of Si thin films as it increases the roughness of the growing surface in microcrystalline silicon[91], in amorphous silicon,[92] and in epitaxial silicon.[57]

The two most important deposition parameters in low-temperature epitaxial growth with breakdown to a polycrystalline phase are the substrate temperature and the hydrogen dilution ratio. A simple contamination probability model relates the epitaxial thickness to the oxygen contamination in the first monolayer of growth.[78,90] The growth of epitaxial films is experimentally observed by monitoring the structure of the evolving film by RHEED, TEM, and Raman spectroscopy.

3.2 Experimental Details

Epitaxial silicon thin films were deposited on Si (100) substrates. Before growth, the substrates were placed in a UV-ozone cleaning system for 10 minutes, then briefly immersed for ~30s in a dilute HF solution in water. Once in the chamber, the substrates were heated by both the substrate heater and by the radiant heat from the wires for 30 minutes to remove any residual

hydrocarbons[93] and to bring the wafers to the growth temperature. The substrate temperature was calibrated with a SensArray thermocouple wafer under vacuum, with the wires set at the growth temperature; this has an error of ± 50°C.

	Silane precursor	$PSiH_4$ mTorr	R = H_2/ SiH_4	P_{tot} mTorr	Ts °C	Wire to Substrate distance	Wire type/ current/ temp	Growth rate nm/min
C.E. Richardson *et al.*[57] : epitaxial growth with polycrystalline breakdown and polycrystalline films	1% in He	0.21 to 1.2	0 to 480	120	230 to 350	5 cm	W 14A 1450°C	1 to 5
C.E. Richardson: epitaxial growth with polycrystalline breakdown and polycrystalline films	5% in Ar	0.45 to 1.4	50 to 200	100	350 to 450	5.5 cm	C 1400°C	1
C.E. Richardson *et al.*[86]: epitaxial growth with polycrystalline breakdown	100%	2	10	20	380	3.5 cm	C 2100°C	9
R.E.I. Schropp[85]: polycrystalline	100%	5	15	75	500	4 cm	W 1800°C	30
C.W. Teplin *et al.*[46]: epitaxial growth with amorphous breakdown	100%	10	0	10	175 to 480	5 cm	Ta 11.5A	12
C.E. Richardson: amorphous	100%	11	0	11	380	3.5 cm	C 2000°C	24
E.C. Molenbroek *et al.*[87]: amorphous	1% in He	30	0	300	280	1.1 cm	W 2000°C	84
R.E.I. Schropp[85]: amorphous	100%	15	0	15	250	5 cm	Ta 1700°C	60

Table 3.1: Deposition parameter comparison for HWCVD grown films on crystalline Si substrates.[57]

3.2.1 Dilute silane growth – Substrate temperature effects

Crystalline silicon thin films were grown on Si (100) substrates by HWCVD. The dilution ratio, $R=H_2/SiH_4$ was set to ~240 for a mixture of 1% SiH_4 in He. Total pressure ranged from 75 to 120 mTorr. Two tungsten wires with diameters of 0.5 mm were positioned between 3.5 and 5 cm from the substrate for a growth rate of ~1 Å/s. The wire temperature was set to 1350-1550°C, as measured by optical pyrometry, and substrate temperatures ranged from 230°C

to 350°C. Films with thicknesses in the range of 100 nm to 6.8 μm were grown. The crystal orientation is determined by RHEED.

3.2.2 Pure silane growth – Hydrogen dilution and pressure effects

The effect of the dilution ratio on the microstructure of silicon thin films was studied using a pure silane system. The substrate temperature was held constant at 380°C, while the graphite filaments were set to 2100°C by optical pyrometry and placed 3.5 cm from the substrate. The H_2 to SiH_4 ratio ranged from 10 to 50, total pressure ranged from 20 to 50 mTorr. The crystal orientation is determined by TEM selective area diffraction patterns, while the crystallinity is determined by Raman spectroscopy. The crystalline fraction is calculated by integrating the Raman intensity under the a-Si peak at 480 cm^{-1} and the c-Si transverse optical mode peak at 520 cm^{-1}.[94,95]

$$X_c = I_{520} / (I_{520} + I_{480}) \qquad (3.2)$$

3.3 Microstructure

3.3.1 Dilute silane growth – Substrate temperature effects

RHEED was used to characterize the crystallinity of 100 nm to 7 μm thick films, grown at a 240:1 hydrogen dilution and temperatures between 230°C and 350°C. An epitaxial phase was observable by RHEED for film thicknesses at and below 1.5 μm, while twinned epitaxial and mixed polycrystalline phases were observed for film thicknesses above 1.1 μm (Fig. 3.3). A general trend toward thicker critical epitaxial thicknesses at lower substrate temperatures is observed. The decrease in epitaxial thickness as substrate temperature increases is believed to be due to interplay between surface hydrogenation at low temperatures and surface oxidation at high temperatures that reduces the epitaxial thickness. This is possibly related to the higher hydrogen content in HWCVD as compared to PECVD or MBE along with the oxygen contamination in the deposition chamber with base pressures between $1x10^{-7}$ and $1x10^{-6}$ torr.[90,96,97]

Figure 3.3 also suggests that a greater substrate to wire spacing contributes to a higher quality, larger epitaxial thickness, of film growth. This could be due to the decrease in deposition rate as the substrate moves further away from the wires. The use of diluted silane also contributes to a higher quality film growth due to the lower partial pressure of silane in the chamber (Table 3.1). Deposition rates in this study vary for each film and average between 0.9 and 4.5 nm/min; however, the growth rate for each phase within each film is not known.

The thickest observed twinned epitaxial layer was 6.8 μm and was grown at a substrate temperature of 230°C (Figs. 3.3 and 3.4). At this temperature, very low-cost materials may be considered as potential substrate materials. The softening points of many inexpensive glass and polymeric materials (soda lime glass, 550°C; borosilicate glass, 500°C; polyimide, 320°C; polyetheretherketone, 250°C) lie above this prospective 230°C growth temperature. The thickest observed epitaxial layer was 5.5 μm and was grown at a substrate temperature of 300°C and R=60. This sample is discussed in Section 6.3.

As the films evolve from epitaxial to twinned epitaxial to polycrystalline, the texture evolves from (100) to predominantly the {121} orientations, as seen by electron backscattered diffraction (EBSD) (Fig. 3.5). The mechanism for this is not fully understood, but discussion of the surface morphology and evolution is contemplated in more detail in Chapter 4. At breakdown the dense single-crystalline films becomes more porous and faceted. However, this is not a condition for breakdown, as epitaxial films with varying degrees of porosity and texture are seen.[57]

Figure 3.6 shows the structural evolution of an epitaxial film grown by HWCVD with a substrate to wire distance of 4.2 cm with two tungsten filaments at 350°C using 1% silane in He. The TEM cross-section shows a dense epitaxial and twinned phase evolving into a rough porous twinned structure. However, the RHEED patterns show that the film is epitaxial with a typical SEM pattern for an epitaxial film grown under conditions of low silane partial pressures (Fig.

3.7). This discrepancy could be due to the inhomogeneous nature of the films and the fact that the amount of film probed during TEM is extremely small.

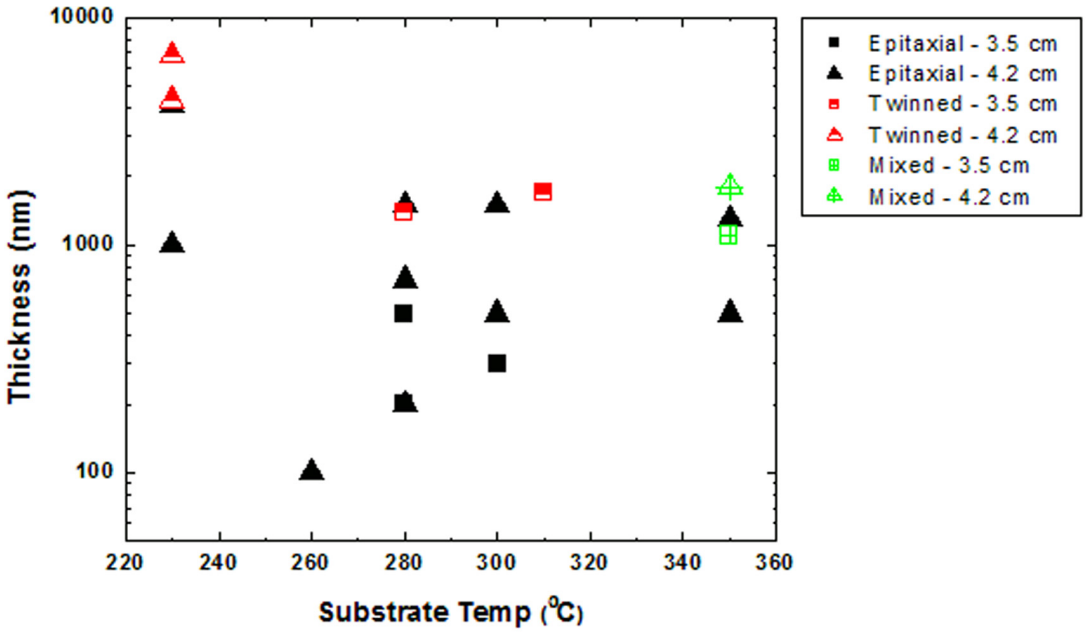

Figure 3.3 Phase diagram of epitaxial Si growth on a Si (100) substrate for 1% SiH_4 in He with R = 240, for substrate-to-wire separations of 3.5 cm and 4.2 cm. Total pressures ranged from 75 to 120 mTorr.

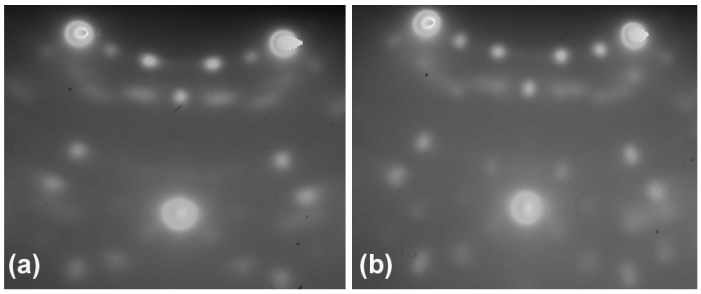

Figure 3.4 RHEED patterns of thick twinned epitaxial films grown at 230°C and R=240 (a) 4.2 μm (b) 6.8 μm.

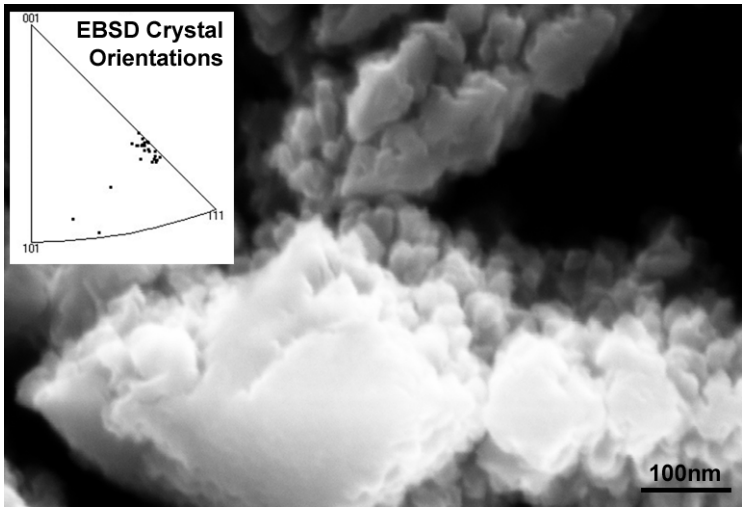

Figure 3.5 SEM image and (inset) EBSD pattern of 1.7 μm film after epitaxial breakdown. This films was grown at 260°C and R=120. The predominant textures of the polycrystalline film are {121}.

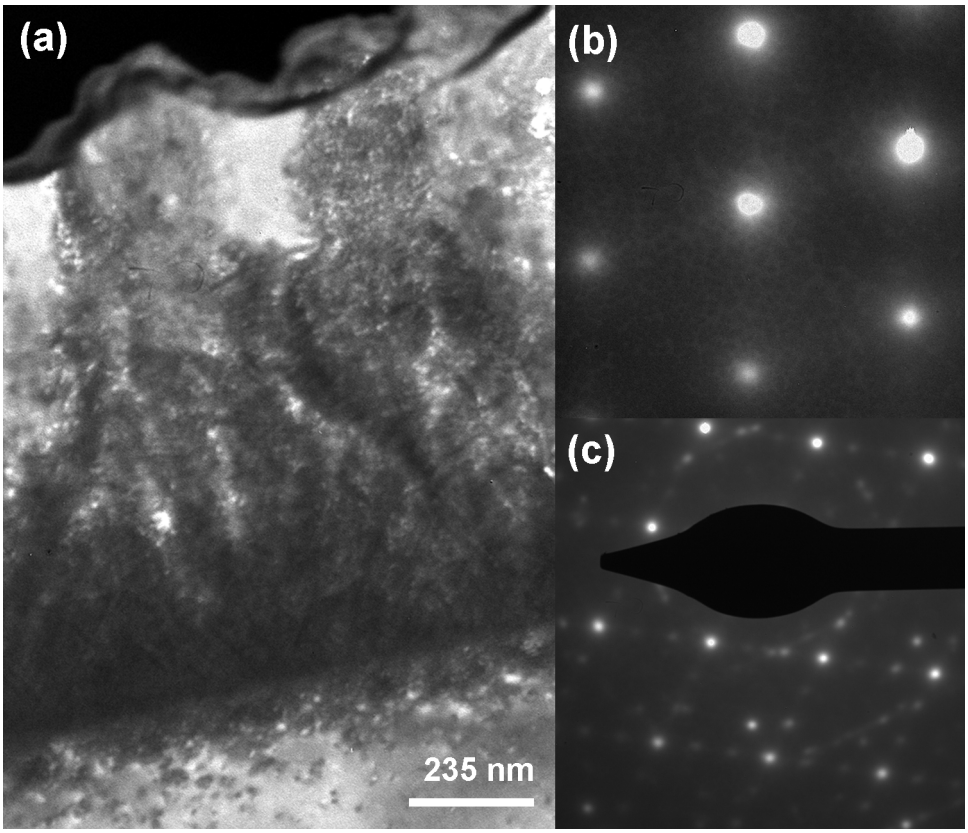

Figure 3.6 TEM images of film grown with a substrate to wire distance of 4.2 cm with 2 W filaments at 350°C. (a) TEM cross-section of film with a dense epitaxial and twinned phase evolving into a more porous twinned structure. (b) Selective area diffraction (SAD) pattern of the epitaxial film/substrate interface. (c) SAD pattern of the top 500 nm of the film showing heavily twinned region.

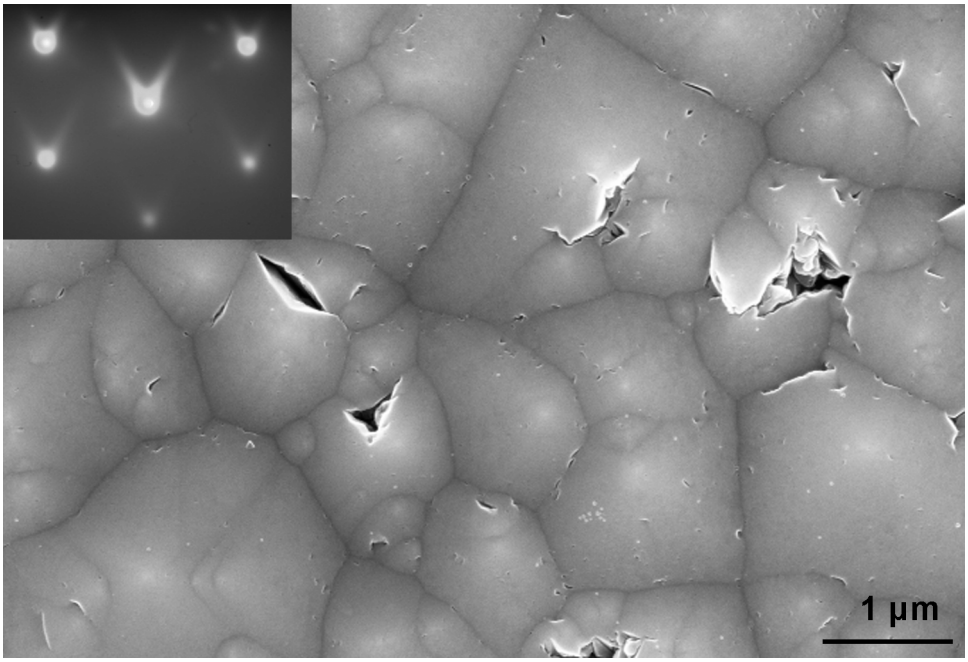

Figure 3.7 SEM image of film shown in Fig. 3.6 with the epitaxial RHEED pattern shown in the inset.

3.3.2 Pure silane growth – Hydrogen dilution and pressure effects

Transmission electron microscopy (TEM) was used to determine the structure of Si thin films grown at 380°C with graphite wires at 2100°C by selective area diffraction of the film or the film/substrate interface using a 0.5 µm aperture (Fig. 3.8). Raman Spectroscopy was used to calculate the degree of crystallinity in each film (Fig. 3.9). The degree of crystallinity did not increase with hydrogen dilution as expected.[78] Instead, an amorphous/protocrystalline (amorphous starting to nucleate crystallites) structure was observed at intermediate dilution ratios of R=20 and R=30 (Fig. 3.10), while at both R=10 and 40 epitaxial growth with polycrystalline breakdown occurred. These are the first known epitaxial results for HWCVD using graphite filaments (Table 3.2 and Fig. 3.8). These results suggest a complex interaction between pressure and dilution, which may be explained by a contamination probability model.

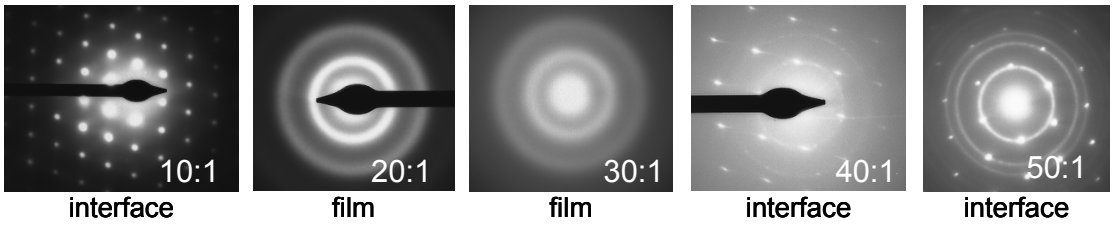

Figure 3.8 TEM selective area diffraction patterns of HWCVD growth with pure silane at 380°C substrate temperature and at 2100°C graphite filament temperature with 3.5 cm spacing. The hydrogen dilution ratio is in the lower right corner while the area selected is underneath each image.

Hydrogen Dilution Ratio	Pressure (mTorr)	Deposition Rate (nm/min)	Raman Crystallinity %	Phase
50:1	50	4	83	Poly
40:1	27	5	84	Epi/poly
30:1	20	3	9	a-Si/Proto
20:1	20	6	10	a-Si/Proto
10:1	20	9	96	Epi/poly

Table 3.2: Results of HWCVD growth with pure silane at 380°C substrate temperature and at 2100°C graphite filament temperature with 3.5cm spacing.

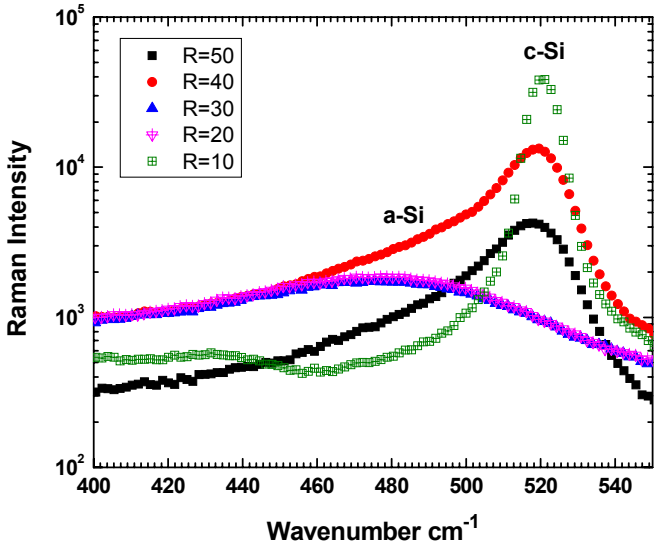

Figure 3.9 Raman spectroscopy of HWCVD films grown with graphite filaments at 380°C and R=0, 10, 20, 30, 40, and 50.

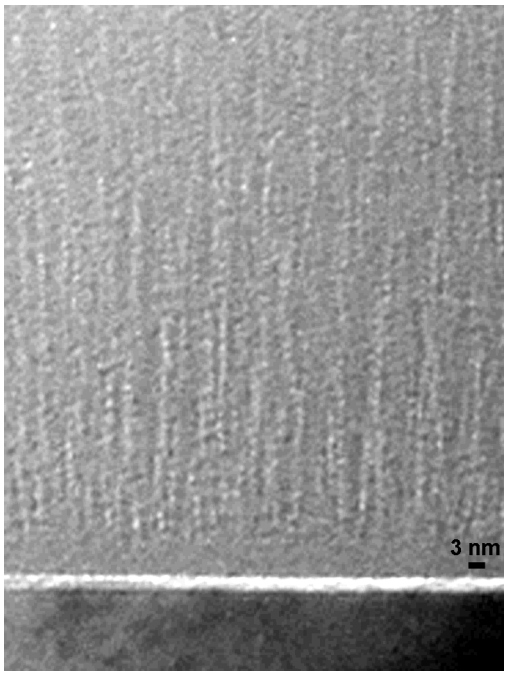

Figure 3.10 TEM cross-section off-axis of the protocrystalline film grown at R=30 and a 380°C substrate temperature.

3.4 Oxygen Contamination Probability Model

In our HWCVD experiments, the critical epitaxial thickness decreases with an increase in substrate temperature unlike in growth with MBE and PECVD.[96] This is most likely due to the high hydrogen content generated during HWCVD growth. Silane decomposes with 70% efficiency and hydrogen decomposes with 14% efficiency. Mason[78] first proposed a probability model to help explain low-temperature HWCVD epitaxial breakdown in terms of oxygen incorporation. Details of the model along with changes to the Mathematica code are included in Appendix A.

The epitaxial growth and the breakdown trends described above are consistent with a simple probability model correlating the critical epitaxial thickness with surface oxidation. Starting with an initial hydrogen surface coverage dependent only on the substrate temperature determined from temperature programmed desorption (TPD) data,[98] the model determines the steady-state hydrogen surface coverage, Θ, by balancing the thermal desorption of surface hydrogen with the adsorption and abstraction of surface hydrogen by atomic hydrogen produced

by the hot-wire along with the oxidation of the surface. The change in hydrogen coverage on a Si (100) surface at a given temperature is given by

$$\frac{\partial \Theta}{\partial t} = \frac{\partial \Theta}{\partial t}_{adsorption} - \frac{\partial \Theta}{\partial t}_{abstraction} - \frac{\partial \Theta}{\partial t}_{desorption} - \frac{\partial \Theta}{\partial t}_{oxidation} \qquad (3.2)$$

An oxygen atom is allowed to deposit into any empty site, while a silicon atom can deposit in any site regardless of site occupation. The model then determines the amount of oxygen deposited during the growth of the first monolayer of silicon for a given growth temperature as a function of dilution ratio R ($R=H_2/SiH_4$) at constant pressure, by assuming that all silicon atoms incident on the substrate contribute to growth and the sticking probability of Si is near unity.[78,90] Figure 3.11 shows that the maximum silicon to oxygen ratio calculated from the model decreases with an increase in substrate temperature from 380°C to 520°C. This may explain the decrease in epitaxial thickness with temperature during HWCVD epitaxial growth (Fig. 3.1). In addition, the peak of the Si/O curve shifts towards higher R at lower temperatures. In other words, higher H dilutions are necessary at lower substrate temperatures in order to achieve high quality films.

The dependence of the measured epitaxial thickness on the calculated silicon to oxygen ratio is difficult to quantify since many assumptions are made as to the gas phase chemistry and reactions. However, it is known that, during MBE crystal growth, impurities at the growing interface lead to surface roughening and subsequent epitaxial breakdown through the formation of voids that may lead to twinning and surface facets.[99] For our dilute silane experiments, a decrease in the maximum silicon to oxygen deposition ratio with temperature, which agrees with the contamination model prediction, may explain the observed decrease in epitaxial thickness with temperature by considering oxygen as the roughening contaminant (Fig. 3.12).

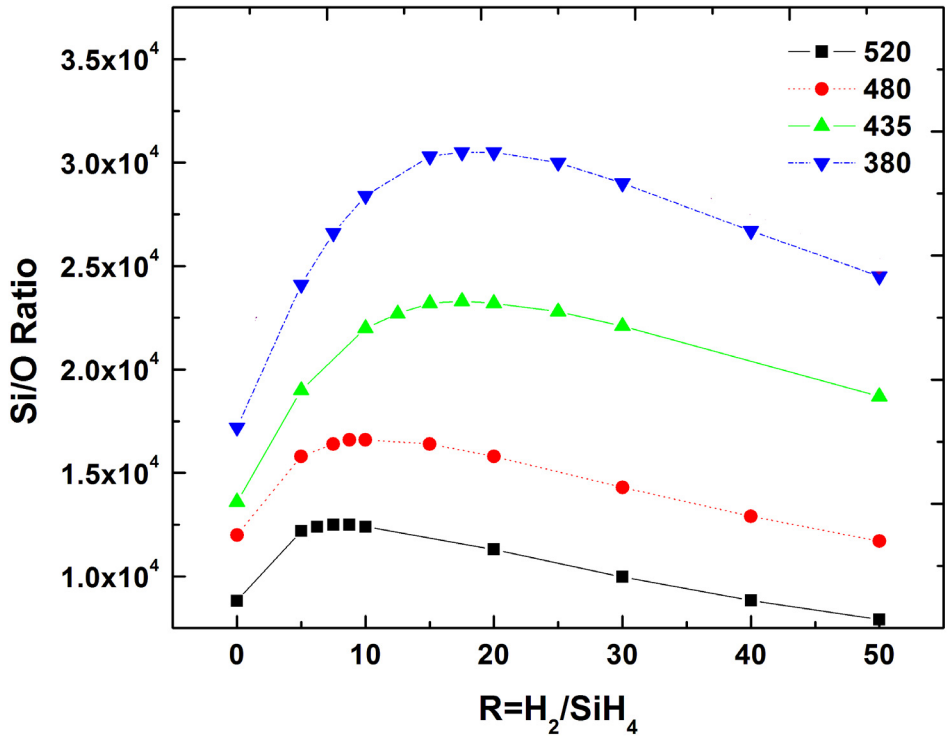

Figure 3.11 Calculated Si/O ratio versus H dilution at various substrate temperatures in °C. The largest Si/O ratio shifts towards higher H dilution at lower substrate temperatures.

Figure 3.13 provides some qualitative insight into the amorphous/protocrystalline peak at intermediate dilution for growth with pure silane. In this simulation, the deposition pressure is changed along with the dilution ratio in order to match the deposition conditions in Table 3.2. The Si/O ratio is highest at the two extremes of the deposition conditions: low dilution ratio, low pressure; and high dilution ratio, high pressure. The high Si/O ratio correlates with less contamination a higher degree of crystallinity. A low Si/O ratio leads to the amorphous and ultimately protocrystalline film due to a higher amount of contamination incorporated into the films. Through these experiments and simulations, we are working toward determining and understanding the optimal deposition parameters for epitaxial growth with polycrystalline breakdown.

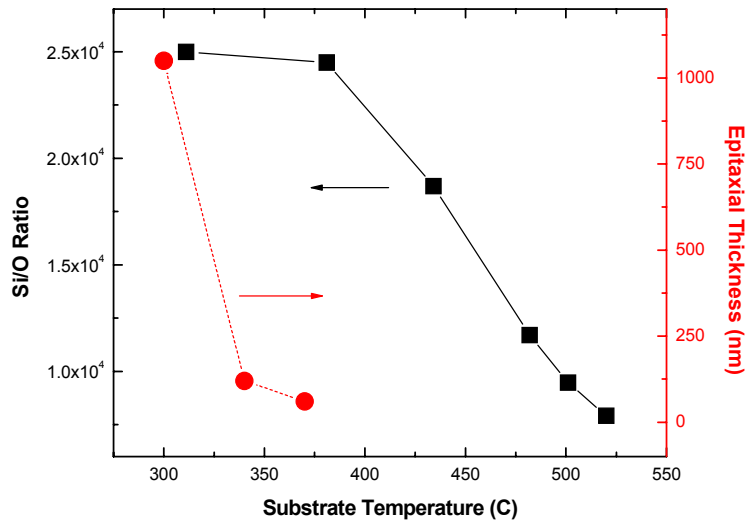

Figure 3.12 The calculated silicon to oxygen ratio in the first monolayer of growth and the measured epitaxial thickness determined by RHEED as a function of substrate temperature for dilute silane growth at 50:1 hydrogen.

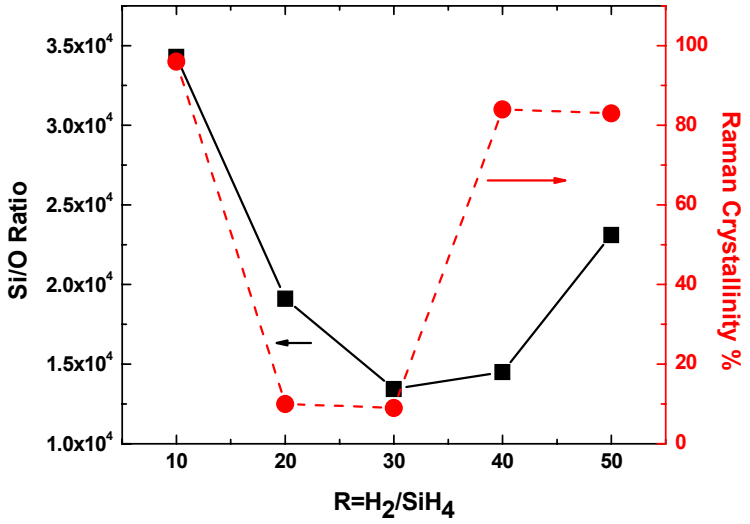

Figure 3.13 The calculated silicon to oxygen ratio in the first monolayer of growth as a function of R for pure silane growth using the deposition conditions in Table 3.2 along with the experimental Raman crystalline fraction.

3.5 Experimental Evidence for the Oxygen Incorporation Model

In order to evaluate the effects of both the substrate temperature and the hydrogen to silane dilution ratio on oxygen contaminant incorporation, a set of 300 nm thick films were grown

and measured by RHEED and Fourier transform infrared spectroscopy (FTIR) for structural and chemical evaluation. The films are epitaxial at high dilutions shifting to a polycrystalline structure at no dilution (Fig. 3.14). This is thought to be due to the ability of hydrogen to abstract contaminants from the film and is discussed in detail in Chapter 4. By comparing the FTIR scans at each dilution with substrate temperature, the effect of the H surface coverage on contaminant incorporation can be examined experimentally. Because all of the films are approximately the same thickness, the absorbance of each can be compared directly. In FTIR, the region between 1800 to 2200 nm^{-1} is typically associated with H content in Si films.[53,100,101] The hydrogen content of these films increases with a decrease in substrate temperature. The hydrogen could be passivating point defects, grain boundaries and possibly even the phosphorous dopants.

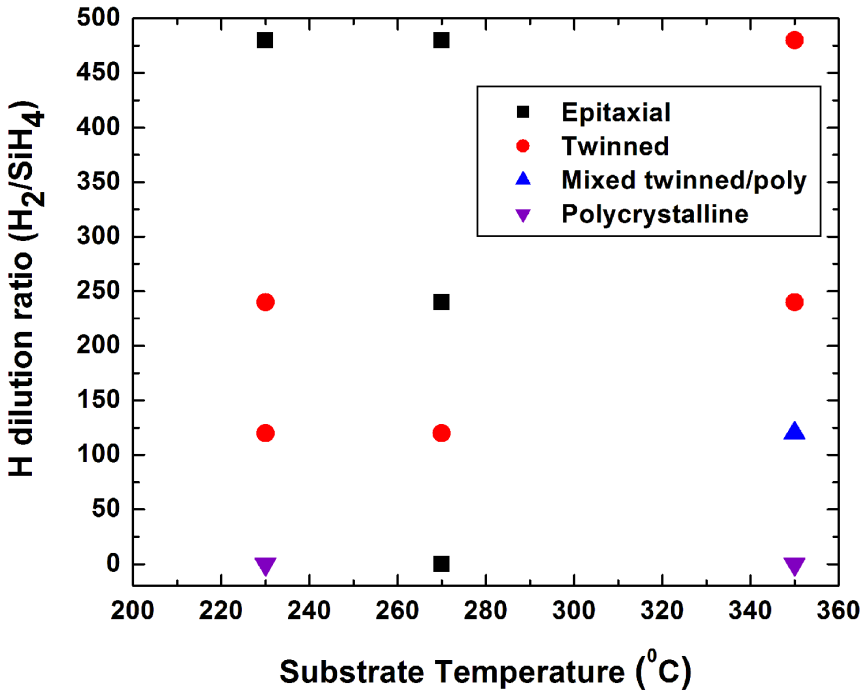

Figure 3.14 Phase diagram for 300 nm thick HWCVD grown crystalline films with substrate temperature and hydrogen dilution ratio.

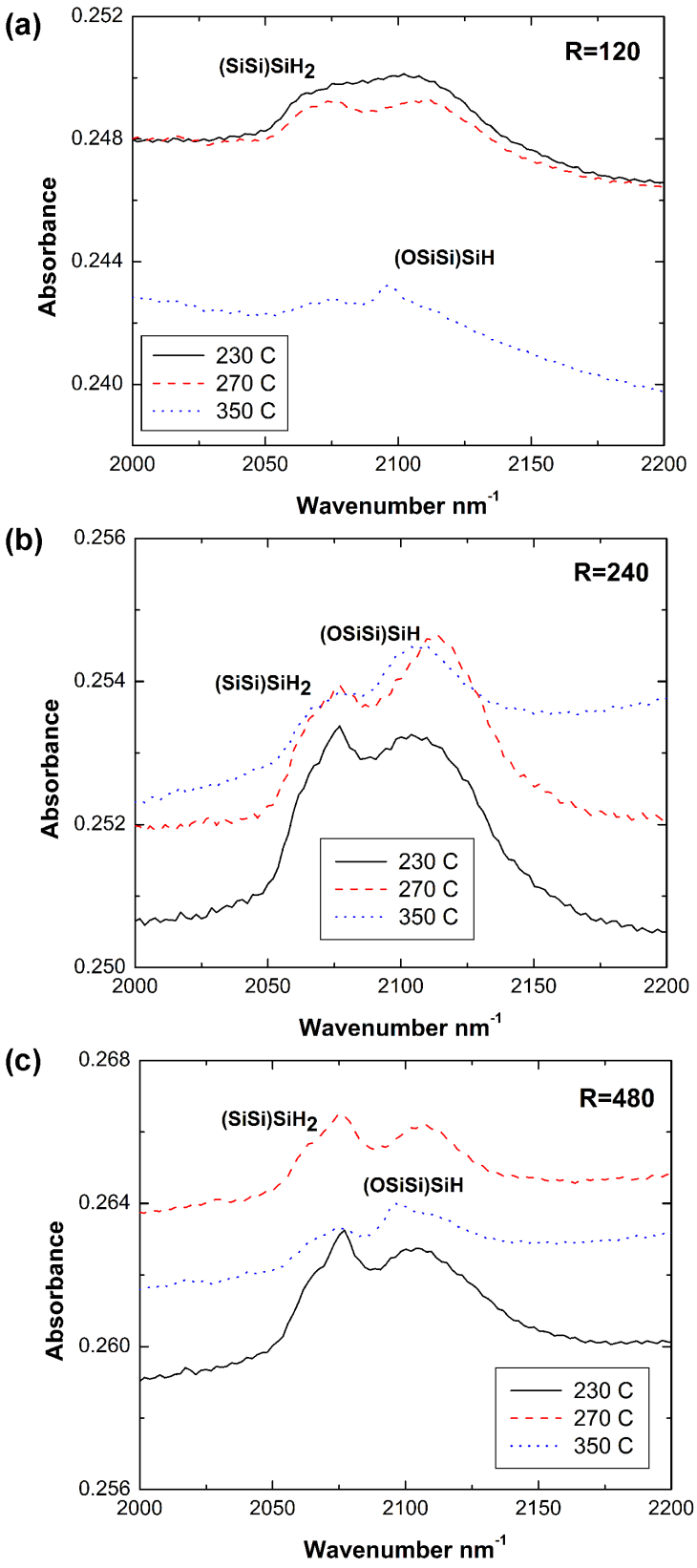

Figure 3.15 FTIR absorbance measurements for 300 nm thick samples grown with a hydrogen to silane ratio of (a) R=120 (b) R=240 and (c) R=480 with substrate temperature.

Moreover, the appearance of an oxygen bond-centered peak at 2096 nm^{-1} with an increase in substrate temperature at a given dilution gives credence to the oxygen contamination model and is likely due to a decrease in the H coverage of the Si (100) surface (Fig. 3.15).[100] It appears that there may also be an O contribution to the hydrogen peaks at 230°C. This would strengthen the hydrogen coverage argument, as below ~300°C the hydrogen coverage cannot increase any further. Therefore, surface mobility will begin to play a more important role and contaminants could be incorporated into the films at low temperatures. This would also explain the shift from epitaxial to twinned epitaxial films for R=480 with a decrease in temperature.

3.6 Conclusions

Hot-wire chemical vapor deposition is a unique technique that allows the regime of low-temperature growth of epitaxial films with polycrystalline breakdown to be investigated. While low growth rates are characteristic of an initial epitaxial phase, deposition under conditions of low silane partial pressure lead to epitaxial breakdown to a polycrystalline phase instead of to an amorphous phase. Under these conditions, arbitrarily thick crystalline films can be grown at low temperatures enabling the use of low-cost substrates, such as glass and many polymers. We have demonstrated the ability to grow a twinned epitaxial silicon layer of 6.8 μm at 230°C. Moreover, as the substrate temperature decreases, the critical epitaxial thickness increases down to a deposition temperature of 270°C. This is due to the high hydrogen content during HWCVD, and can be explained by a contamination probability model. The contamination probability model describes the complex relationship between hydrogen dilution, substrate temperature, and pressure and points to the direction of higher H dilution at low substrate temperature for high quality epitaxial growth.

3.7 References

1. J. Platen, B. Selle, I. Sieber, S. Brehme, U. Zeimer, and W. Fuhs, Thin Solid Films **381** (1), 22 (2001).

2. D. J. Eaglesham, Appl. Phys. Rev. **77** (8), 3597 (1995).

3. Maribeth S. Mason, "*Synthesis of Large-Grained Polycrystalline Silicon by Hot-Wire Chemical Vapor Deposition for Thin Film Photovoltaic Applications,*" California Institute of Technology, 2004.

4. C. E. Richardson, M. S. Mason, and H. A. Atwater, Amorphous and Nanocrystalline Silicon Science and Technology-2004 (Materials Research Symposium Proceedings Vol.808), 227 (2004).

5. C. W. Teplin, Qi Wang, E. Iwaniczko, K. M. Jones, M. Al-Jassim, R. C. Reedy, and H. M. Branz, J. Crys. Grwth **287**, 414 (2006).

6. C. E. Richardson, M. S. Mason, and H. A. Atwater, Mater. Res. Soc. Symp. Proc. **808**, A8.11 (2004).

7. Jack H. Thiesen, "*Low-temperature Epitaxial Silicon Using Hot-wire Chemical Vapor Deposition,*" University of Colorado, 1997.

8. T. Watahiki, A. Yamasa, and M. Konagai, J. Crys. Grwth **209**, 335 (2000).

9. T. Watahiki, K. Abe, H. Tamura, S. Miyajima, A. Yamada, and M. Konagai, Materials Science And Engineering B-Solid State Materials For Advanced Technology **89** (1-3), 328 (2002).

10. B. Rau, I. Sieber, B. Selle, S. Brehme, U. Knipper, S. Gall, and W. Fuhs, Thin Solid Films **451-452**, 644 (2004).

11. P. Reinig, F. Fenske, B. Selle, W. Bohne, J. Rohrich, I. Sieber, and W. Fuhs, Appl. Surf. Sci. **227**, 114 (2004).

12. R. E. I. Schropp, Thin Solid Films **451-452**, 455 (2004).

13. C. E. Richardson, M. S. Mason, and H. A. Atwater, Proceedings of the 31st IEEE PVSC, Lake Buena Vista, Fl, 2005.

14. E. C. Molenbroek, A. H. Mahan, E. J. Johnson, and A. C. Gallagher, J. App. Phys. **79** (9), 7278 (1996).

15. C.W. Teplin, E. Iwaniczko, K. M. Jones, R. Reedy, B. To, and H. M. Branz, Mater. Res. Soc. Symp. Proc. **862**, A2.3 (2005).

16. H.R. Moutinho, C.-S. Jiang, J. Perkins, Y. Xu, B.P. Nelson, K.M. Jones, M.J. Romero, and M.M. Al-Jassim, Thin Solid Films **430**, 135 (2003).

17. J. Robertson, J. App. Phys. **93** (1), 731 (2003).

18. Christine E. Richardson, M. S. Mason, and Harry A. Atwater, Thin Solid Films **501** (1-2), 332 (2006).

19. R. Bruggemann and F. Houze, Proceedings of the 16th European Photovoltaic Solar Energy Conference, Glasgow, 2000.

20. D. Levi, B. Nelson, J. Perkins, and H. Moutinho, Proceedings of the NCPV Program Review Meeting, Lakewood, CO, 2001.

21. C.E. Richardson, Y.-B. Park, and H. A. Atwater, Phys. Rev. B **73** (24) (2006).

22. M. K. Sanganeria, M. C. Ozturk, K. E. Violette, G. Harris, A. Lee, and D. M. Maher, Appl. Phys. Lett. **66** (10), 1255 (1994).

23. J. E. Smith Jr., M. H. Brodsky, B. L. Crowder, M. I. Nathan, and A. Pinczuk, Physical Review Letters **26** (11), 642 (1971).

24. Toshiki Kaneko, Masatoshi Wakagi, Ken-ichi Onisawa, and Tetsuroh Minemura, Applied Physics Letters **64** (14), 1865 (1994).

25. H. Fujiwara Michio Kondo, and Akihisa Matsuda, Thin Solid Films **430**, 130 (2003).

26. M. S. Mason, C. E. Richardson, H. A. Atwater, and R. K. Ahrenkiel, Thin Solid Films **501** (1-2), 288 (2006).

27. N.B.H. Jonathon M.C. Flowers, Y. Liu, and A. Morris, Journal of Chemical Physics **99**, 7038 (1993).

28. D. J. Eaglesham, Journal of Applied Physics **77**, 3597 (1995).

29. T. S. Shi, S. N. Sahu, G. S. Oehrlein, A. Hiraki, and J. W. Corbett, Phys. Stat. Sol. **74**, 329 (1982).

30. K. F. Feenstra, R. E. I. Schropp, and W. F. Van der Weg, J. Appl. Phys. **85** (9), 6843 (1999).

31. M. H. Brodsky, M. Cardona, and J. J. Cuoma, Phys. Rev. B **16** (8), 3556 (1977).

Chapter 4

Surface Evolution of Crystalline Silicon Thin Films by Low-Temperature HWCVD on Silicon Substrates

4.1 Introduction to Surface Evolution

The properties of thin-films can vary substantially depending upon growth conditions. The microstructure and surface evolution are particularly important because all other properties: optical, electrical, and mechanical, stem from these. Previously, many researchers have reported on the roughness evolution of amorphous Si films with substrate temperature[102,103] and thickness[104] and of epitaxial films grown by molecular beam epitaxy (MBE)[105], ion assisted MBE,[106] and hyperthermal Si beams.[107] This study addresses the surface evolution of hot-wire chemical vapor deposited (HWCVD) crystalline Si thin-films: epitaxial, twinned epitaxial, and polycrystalline; with temperature, thickness, and hydrogen dilution; and discuss the resulting growth regimes and structures.

HWCVD is an unusual epitaxial film deposition process in which the critical epitaxial thickness actually increases with decreasing substrate temperature when breakdown is to a polycrystalline phase[58,78] and down to a substrate temperature of 380°C when breakdown is to an amorphous phase.[46] In silicon HWCVD, gas precursors are catalytically decomposed by a hot filament and silane is decomposed with 70% efficiency.[108] Thus, the substrate temperature can be at a much lower temperature than in MBE or traditional CVD processes and one can still achieve high quality films.[109]

During the last decades, many theoretical and numerical simulations of vapor deposited surfaces in conditions far away from equilibrium have been investigated using various continuum models.[110-116] However, experimental results show the scaling parameters vary from case to case

and strongly depend upon the growth conditions and methods, even for the same material. Rather than attempt to compare the present experimental results with particular models for surface growth, a scaling analysis of surface evolution during HWCVD is developed in order to gain insight about the factors that affect the surface morphology, such as substrate temperature and hydrogen dilution, and to use these insights in turn to deduce general observations about how growth kinetics and structure change with these parameters.

The self-affine scaling nature of surfaces during thin-film growth was first introduced by Family and Vicsek.[117] The growing surface can be characterized as either self-affine or self-similar by its fractal dimension and rms roughness, defined at position r and thickness or deposition time t as $\sigma_r(M)=[\Sigma_i(h_i- h(M))^2]^{1/2}$, where $h(M)$ is the mean height. The rms roughness and the correlation between points can be described by the height-height correlation function G(r) defined at r = m*d by the function

$$G(md)=\left[\frac{1}{N-m}\sum_{i=1}^{N-m}(\delta_{i+m}-\delta_m)^2\right]^{1/2} \qquad (4.1)$$

where d is the distance between two neighboring points.[118] This equation examines the correlations between the distances $\delta_i=\delta(y_i)$ at different positions along the scan direction y_i, i=1,…,N, and N is the total number of equidistant points on y.[118]

In our study, surface height data from atomic force microscopy (AFM) were obtained for a 10 μm x 10 μm scanning size window, unless otherwise noted. Morphologies such as ours have been successfully described in terms of the self-affine scaling model given by $G(r)\sim r^{\alpha}$, where α is the static scaling coefficient (or Hurst parameter).[103,118] Self-affine means that the surface remains statistically the same when it is stretched anisotropically in different directions.[118] At long length scales, the height-height correlation function, G(r), approaches the value $\sqrt{2}\sigma$. The correlation length, ξ, is defined at

$$G(\xi)=\sqrt{(1-\frac{1}{e})}\sqrt{2}\sigma \qquad (4.2)$$

At length scales much greater than ξ, $\sigma_{sat} \sim t^{\beta}$. β is known as the dynamic scaling coefficient.

This study investigates the evolution of the surface roughness for HWCVD grown crystalline Si thin-films: epitaxial, twinned, and polycrystalline; that are of increasing importance to the photovoltaic and semiconductor industries. We consider specifically the influence of substrate temperature and hydrogen dilution upon the surface morphology and structure of the Si thin-films.

4.2 Experimental Details

Crystalline silicon thin-films were grown on Si (100) substrates by hot-wire chemical vapor deposition (HWCVD). The dilution ratio of H_2 to SiH_4 was varied from 0 to 480 by varying the H_2 flow rate with a mixture of 1% SiH_4 in He. Total pressure ranged from 75 to 120 mTorr. Two tungsten wires with diameters of 0.5 mm were positioned between 3.5 and 5 cm from the substrate for a growth rate of ~1 Å/s. The wire temperature was set to 1350-1550°C, as measured by optical pyrometry, and substrate temperatures ranged from 230°C to 350°C.

Before growth, substrates were placed in a UV-ozone cleaning system for 10 minutes, and then briefly immersed in HF. Once in the chamber, the substrates were heated by the substrate heater and by the radiant heat from the wires for 30 minutes to remove any residual hydrocarbons and to bring the wafers up to growth temperature. The substrate temperature was calibrated with a SensArray thermocouple wafer under vacuum, with the wires set at the growth temperature, and has an error of ±50°C due to the calibration of the wires. Films with thicknesses ranging from 100 nm to 6.8 μm were grown.

AFM measurements were made on each sample over an appropriate size widow (40, 10, or 5 μm) and then analyzed for scaling behavior using a Matlab code expanding the arguments of Constantoudis[118] into 2-D by averaging the height-height correlation functions in the x and y directions. Surface morphology was also investigated by scanning electron microscopy (SEM) to

complement the AFM measurements. In order to study the crystallinity of the films, Raman spectra were collected using 514.5 nm excitation, reflection high energy electron diffraction (RHEED) measurements were performed to characterize the crystallographic structure of the film surface, and cross-sectional transmission electron microscopy (TEM) is used to image the evolution of the structure and morphology in the films.

4.3 Results

4.3.1 Thin-film structure and crystallinity

Unlike other reports of the effect of hydrogen dilution on crystallinity,[88] we do not observe a change in crystalline fraction with H dilution (Fig. 4.1a-c), but there is a change in structure from epitaxial to twinned to polycrystalline Si with decreasing H fraction (Fig. 4.2). All of the samples are fully crystalline as measured by Raman spectroscopy with crystalline silicon peaks at 521.5 cm^{-1}. Despite an apparently porous structure as seen in Fig. 4.3 for H_2/SiH_4 ratio, R=120 to 240; we find no detectable SiO_2 fraction as indicated by the absence of SiO_2 peaks at 465 and 800 cm^{-1} during the Raman measurements taken 70 days after deposition with storage in an air ambient (Fig. 4.1). The lack of an internal oxidized surface indicates that these films do not show the instabilities associated with some reports of microcrystalline Si.[119] This is likely due to the large grain sizes in the polycrystalline films and a small fraction of networked porosity.

4.3.2 Surface roughness and evolution

AFM and SEM were used for real space imaging of deposited Si thin-films with various H_2/SiH_4 ratios, R, and substrate temperatures as shown in Figs. 4.3 and 4.4. If we look at films of average thickness 300 nm deposited under a pressure of 120 mTorr with a 5 cm wire to substrate spacing, the rms roughness and lateral correlation length generally increase with substrate temperature at each dilution (Figs. 4.5 and 4.6). This is in contrast to results for both crystalline and amorphous Si seen by molecular beam epitaxy[120] and plasma-enhanced CVD (PECVD)[103]

and is more akin to the increase in surface roughness with increasing substrate temperature seen in HWCVD grown amorphous silicon.[121] If we assume as in Mason,[78,90] that H coverage prevents contaminants such as C and O from depositing onto the surface, but does allow Si to deposit, then at higher substrate temperatures increased hydrogen desorption leads to higher contaminant incorporation which would increase the surface roughness with increasing substrate temperature.[86,90,122] Moreover, given that the H coverage of the Si (100) surface at high H dilutions is large and temperature independent below 300°C,[123] then as we lower the substrate temperature from 270°C to 230°C, we suggest that film growth becomes surface mobility-limited and there is an increase in the film roughness once more.

Consistent with previous results, the roughness at each temperature increases with increasing H dilution. This could be due to a decrease in Si surface diffusion due to the lower amount of H at higher substrate temperatures[120] or could be due to the H-mediated chemical abstraction of surface amorphous species back into the vapor phase causing an increase in the surface roughness.[124] This last point will be discussed in more detail in the discussion section.

Interestingly, by comparing Fig. 4.2 with Fig. 4.5, it is found that epitaxial growth is possible on the highest RMS roughness surfaces under conditions of high hydrogen dilution. Roughness during growth under most conditions is believed to cause epitaxial breakdown.[77,106,125] However, under extreme conditions of high hydrogen dilution, as we find in our experiments, the hydrogen actually improves the preferential growth of epitaxial species by removing amorphous adatoms and defects. This H etching effect increases the roughness of the films, but allows an epitaxial film to continue to deposit onto the rough surface.

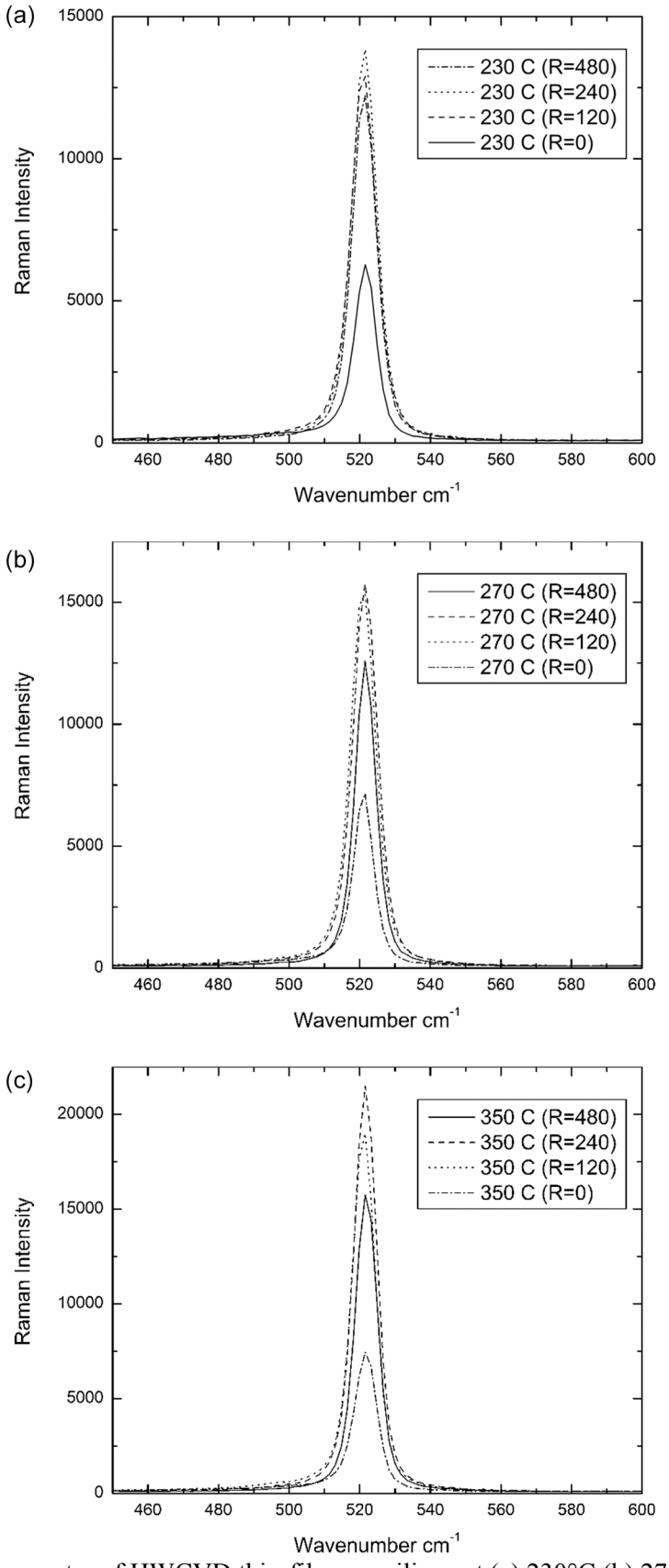

Figure 4.1 Raman spectra of HWCVD thin-films on silicon at (a) 230°C (b) 270°C (c) 350°C.

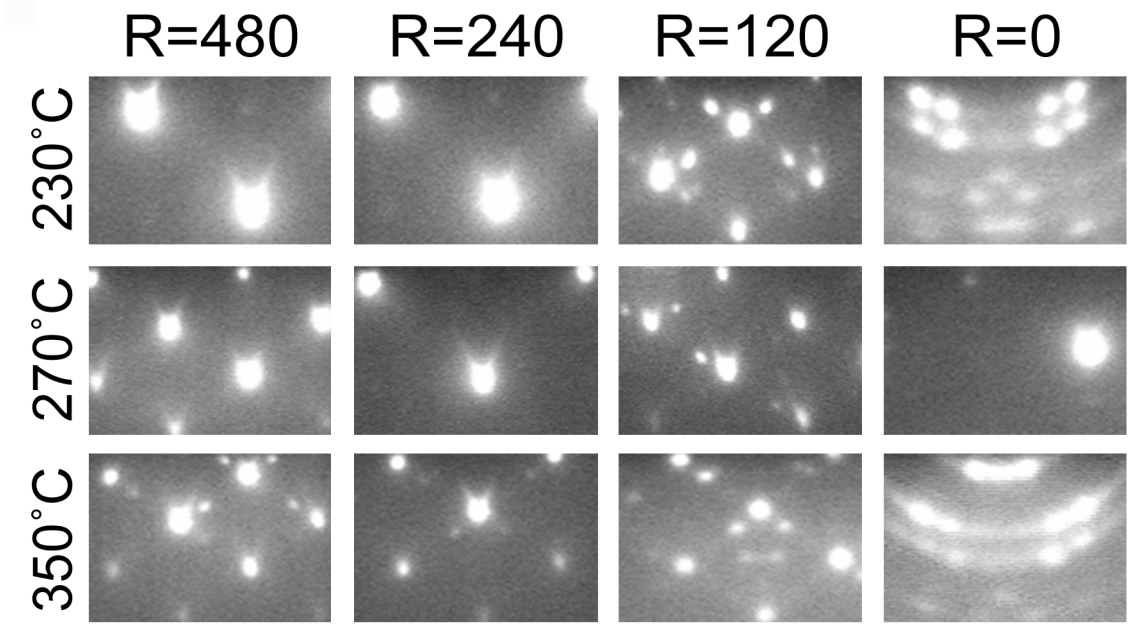

Figure 4.2 RHEED patterns of HWCVD grown Si films at various substrate temperatures versus hydrogen dilution.

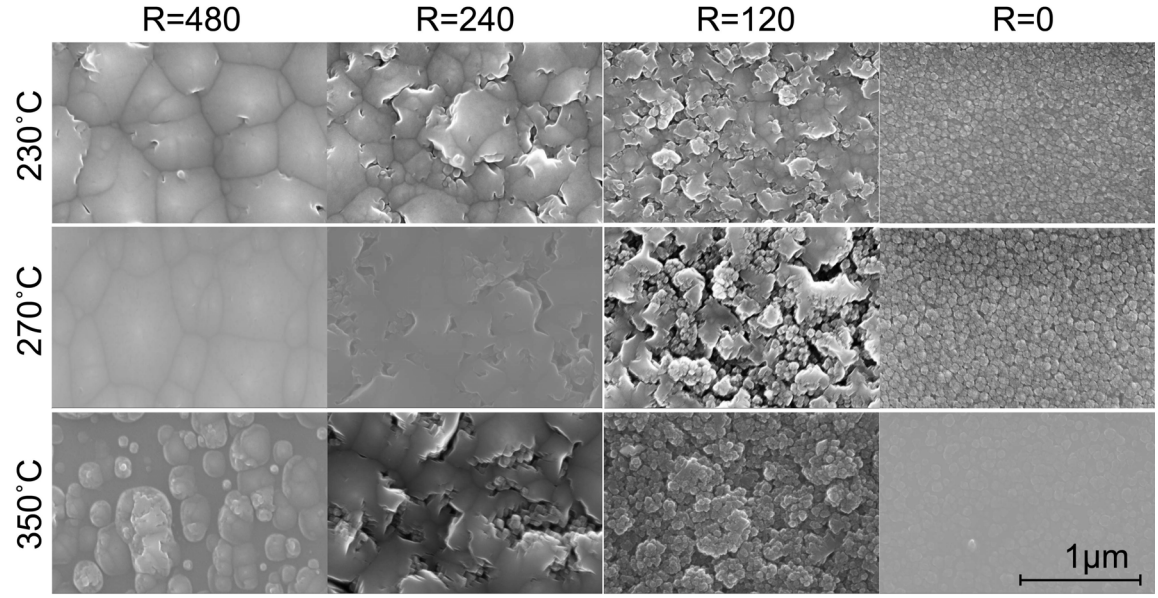

Figure 4.3 Scanning electron microscopy images of HWCVD grown Si films at 50kX. Images correspond to the RHEED patterns in Fig. 4.2 and the atomic force micrographs in Fig. 4.4.

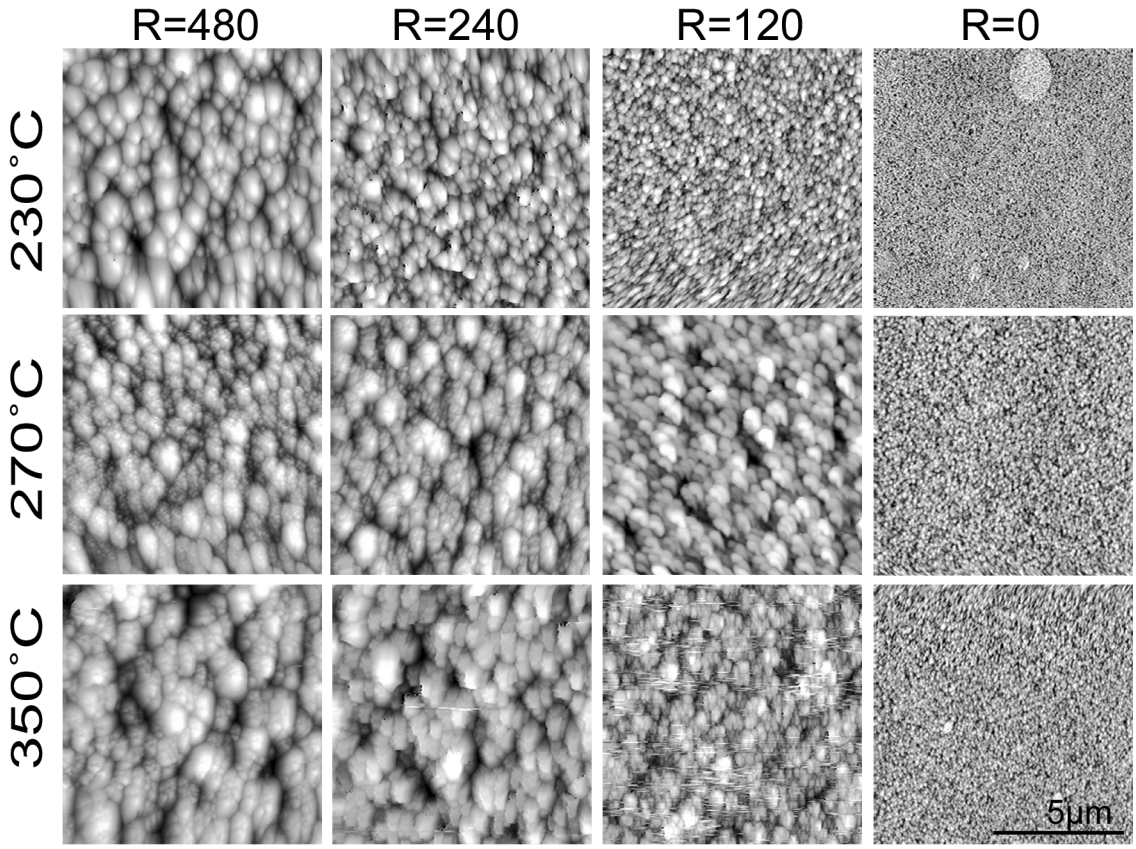

Figure 4.4 Atomic force micrographs of Si film surfaces for various substrate temperatures and hydrogen dilution ratios taken in contact mode with 10 x 10 μm^2 area. Micrographs correspond to the SEM images in Fig. 4.3.

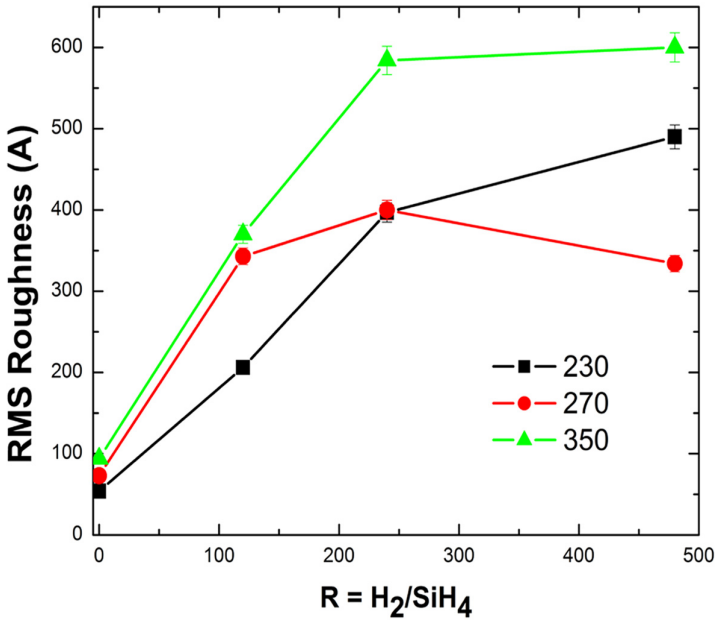

Figure 4.5 RMS roughness of films at various substrate temperatures versus hydrogen dilution taken from 10 μm x 10 μm scans.

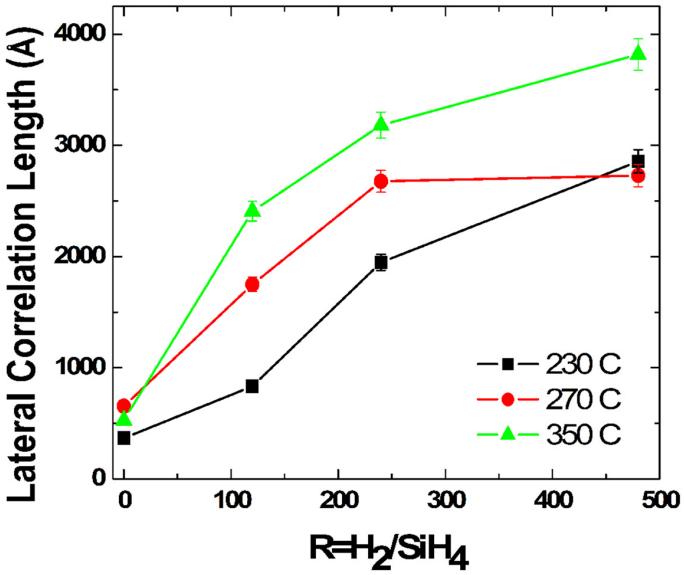

Figure 4.6 Lateral correlation length of films at various substrate temperatures versus hydrogen dilution taken from 10 μm x 10 μm scans.

Figure 4.7 shows TEM images in cross-section of films grown at R=480, 240, and 120. The porosity seen in Fig. 4.3 correlates well with the structural evolution shown in the TEM images. A decrease in hydrogen dilution corresponds to a more porous structural evolution. Contrary to Raman however, each porous region appears to originate in the film and grow perpendicular up to the surface and should be susceptible to oxidation.

The RMS roughness was obtained from the height-height correlation function plots generated using equation (4.1). Each height-height correlation function in Fig. 4.8 consists of two regimes, which are separated by the correlation length, ξ. At length scales $r<\xi$, the slope of G(r) increases as $G(r)\sim r^{\alpha}$, where α is the static scaling coefficient. At length scales much greater than ξ, the saturation RMS value is reached and there is no further increase in σ with increasing length scale. The rms value also increases with thickness as β, the dynamic scaling coefficient. The RMS roughness value and ξ, represent the vertical and lateral sizes of the mountains or valleys in the rough surface, respectively.

The static scaling coefficient is correlated to the local surface fractal dimension and is indicative of the surface texture in the short scaling range, $r<\xi$.[118] The static scaling coefficients

in this series range from 0.42 to 0.86 (Fig. 4.9) and are associated with a local fractal dimension, D_F, by the relation $D_F=3-\alpha$. The fractal dimensions obtained range from $D_F=2.14$ to 2.58 and indicate that the surface roughens quickly. One would expect Si to be the main deposition species due to its large sticking probability of ~1. Although Si is the most prevalent species desorbed from the wire,[114,39,50,126] in this pressure and hydrogen dilution regime the predominant growth species should be SiH_3.[39,56] SiH_3 can also diffuse on a hydrogenated surface before being incorporated, like our Si (100) substrates at temperatures 350°C and below.[62] This allows for a much smaller, but important smoothening effect on the deposition and is seen by the slope of the high frequency portion of the power spectral density function (PSD) ranging from -3.67 at R=120, Ts=350°C and above with the highest slopes at R=0. All of the slopes in the high frequency region of the PSD are near -4 (Fig. 4.8d), which is the theoretical value normally associated with surface diffusion.[103,127]

The Schwoebel effect is the asymmetrical nature of the sticking coefficient of adatoms to steps and its consequences on the surface evolution. A diffusing atom along an upper ledge sees a barrier, the Schwoebel energy barrier, toward going to a lower ledge. A positive Schwoebel effect causes the surface roughness to increase with deposition time. A negative barrier would cause the surfaces to smoothen during growth.[128] As shown in Fig. 4.1, the majority of these films are epitaxial, and so one would expect that most of the step edges and faces are in the <100> directions. However, because these films are so rough, there are additional growth directions, presumably with each having a different Schwoebel barrier.[129] The Schwoebel energy at each possible surface step is not addressed, as this would be too complicated in the current system and would give little additional insight. Moreover, the surface diffusion effect is thought to be less important than the effect H etching in determining the surface roughness, as evidenced by the increase in roughness being more dependent on the H dilution than the substrate temperature.

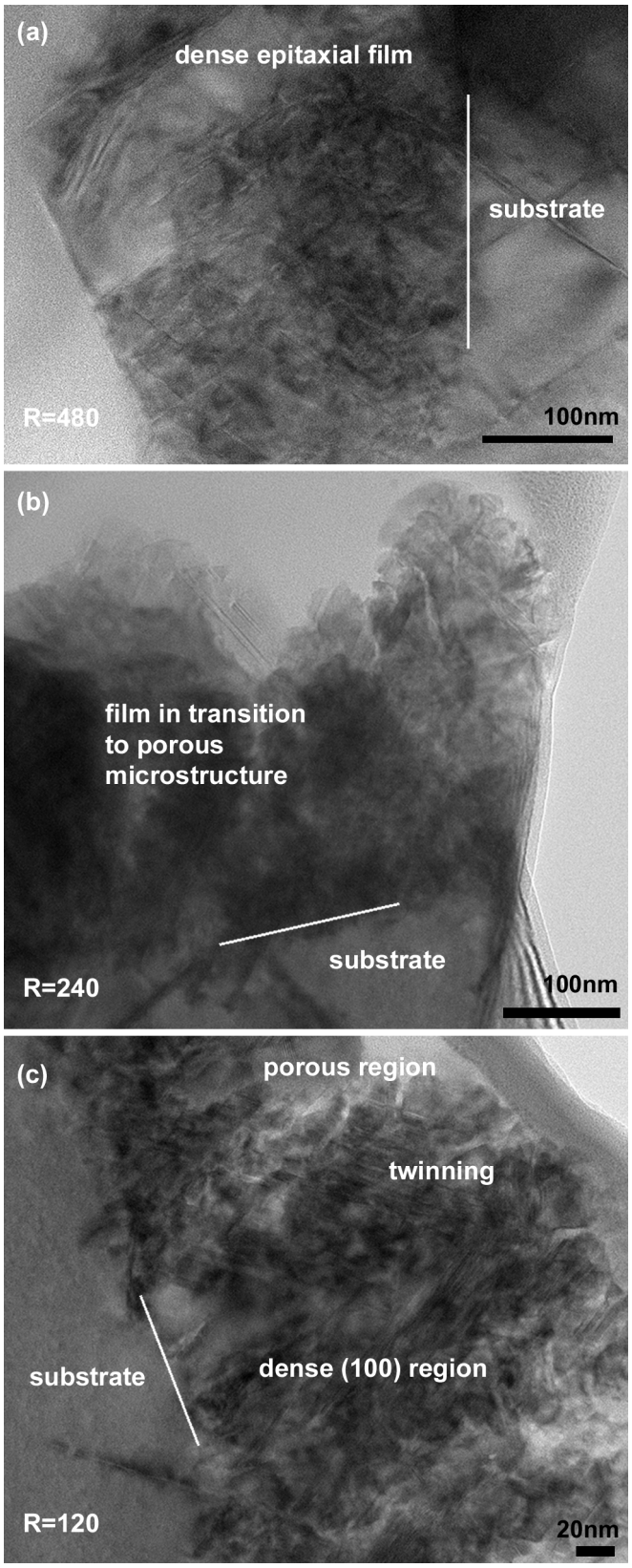

Figure 4.7 Cross-sectional TEMs of HWCVD grown epitaxial and twinned films at 350°C and dilution ratios, R, of (a) 480 (b) 240 (c) 120. The films get porous more quickly as R decreases.

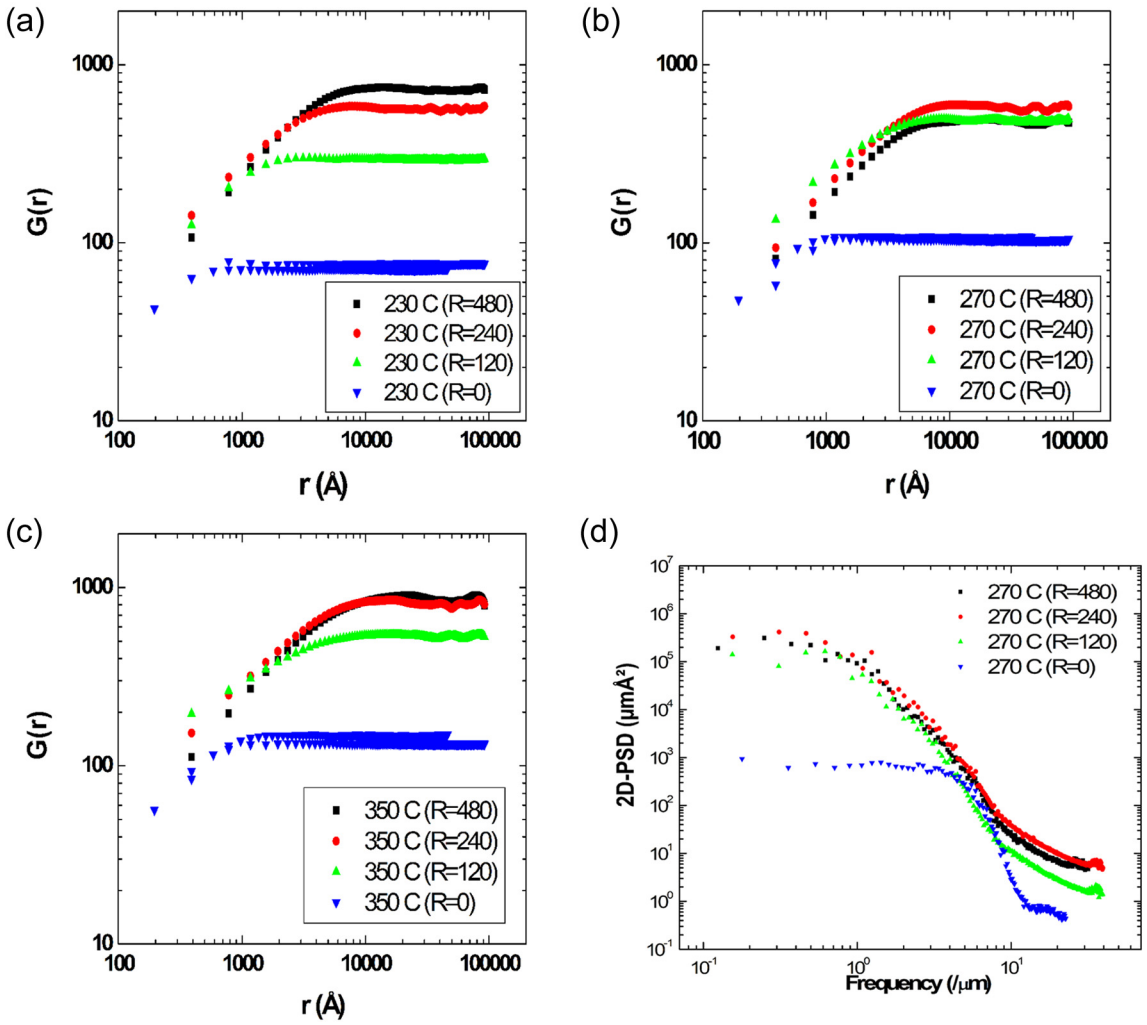

Figure 4.8 (a), (b) and (c) Effect of dilution ratio (R) and substrate temperature on the height-height correlation functions of Si thin-films. The average film thickness is 300 nm. For R=0 scans at both 5 and 10 μm are displayed. (d) Representative PSD for 270°C.

However, this energy barrier is thought to be small and positive for most crystallographic directions found in silicon growth and would be consistent with the roughening of our surfaces during growth (Figs. 4.10 and 4.11).[129] It is also possible that the roughness of these films does not allow the growth of [111] facets, typical during epitaxial growth by most other methods. This may also contribute to the breakdown of the epitaxial or twinned phase into a polycrystalline phase, rather than an amorphous phase.[77,129]

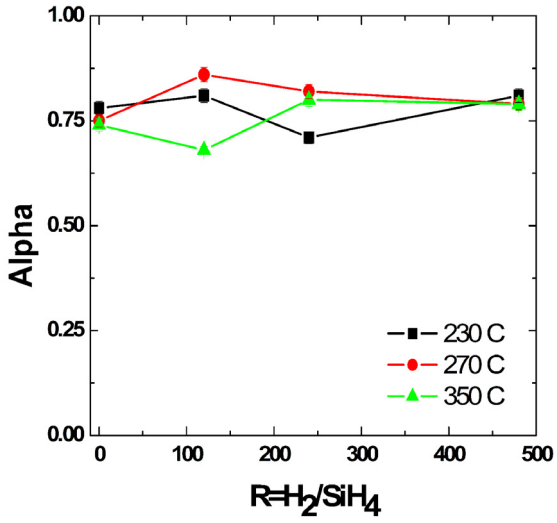

Figure 4.9 (a) Static scaling coefficient exponent, α, at different substrate temperatures as a function of hydrogen dilution.

As mentioned earlier, there is a general increase in the saturated RMS roughness with thickness (Figs. 4.10 and 4.11). These films are categorized by dilution, but for each dilution the films were deposited under a range of substrate temperatures (230-350°C), pressures (75-120 mTorr), wire to substrate distances (3.5-5 cm), and wire temperatures (1350-1550°C). The scatter in Fig. 4.10 reflects the wide range of deposition conditions. For example, the data for R=240 includes depositions at several experimental settings described above. The entire set of data at R=240 has a beta value of 0.82±0.20 for r<1500 nm, while the subset of films grown at 270°C and R=240 have a beta value of 0.78±0.03 (Fig. 4.10b).

4.4 Discussion

We suggest that aside from the thickness, under the deposition conditions described above, hydrogen dilution is the most important factor that determines the surface evolution of a HWCVD grown crystalline film. As a starting point, at R=240 and all substrate temperatures and deposition conditions, β=0.82±0.20 and α=0.78±0.06. The high values of the static and dynamic scaling coefficients of these HWCVD grown films at R=240 are more akin to those observed in

sputter deposition process, than in other CVD methods.[102,111] Shadowing growth has been observed in sputtered amorphous silicon[130] and modeled by Monte Carlo simulations[110,131] with growth coefficients of β=1. For shadowing models, the morphology of neighboring points can result in shadowing where the valleys of the surface grow less than the hills around them despite the fact that there is an extended source. Relaxing this model to allow for surface diffusion, in the present case of SiH_3, decreases the growth exponent β to between 0.5 and 1. This modified model fits well for the above data for R=240 and is confirmed by the SEM images in Fig. 4.3 where surface roughness is characterized by a bimodal feature size distribution indicating some porosity from a shadow growth. We suggest that this is due to a shadowed etch of the incoming H atoms, rather than a more traditional shadowed growth. This would also offer an explanation as to how epitaxial films are able to grow on such rough surfaces. Hydrogen could preferentially etch those atoms which are defects, and consequently at a lower bond energy, than those that are in the epitaxial structure.

By comparing the SEM images and RMS roughness of Figs. 4.3 and 4.4, we conclude that a similar deposition mechanism must contribute to growth at R=120 and at R=480 as in R=240. At R=120, the RMS roughness and correlation lengths are less than those at R=240, and there are additional smaller surface features. Because of the decrease in H available for etching defective adatoms under the R=120 regime as opposed to R=240, these films at 300 nm are twinned rather than epitaxial at low temperatures. Moreover, hydrogen etching of silicon is known to be less effective at higher temperatures, and so at 350°C, the etching mechanism is insufficient to quench the polycrystalline breakdown of this film. Films with R= 20 also had the highest deposition rates in this study of up to 5 nm/min and so one would expect the dynamic scaling coefficient to be close to 1.

As shown in Table 3.1, the deposition rates of films grown at R=0 versus R=480 vary at most by a factor of 5 and do not increase monotonically as a function of silane partial pressure. Moreover, the morphology of an etched surface as in R=120 and 240 is not evident at R=480.

This could mean that the deposition species come from another source aside from the precursors off the hot filament. One explanation for this is that at R=480, it is important to consider growth species re-emission and deposition following the re-emission model presented by Karabacak *et al.* who found experimentally β=0.41 and α=0.83.[130] In this model, each atom has a finite sticking probability depending on how many times it has been re-emitted.[132] Surface diffusion and a directional incident flux on the growing surface are also considered and are consistent with deposition conditions in the HWCVD experiments. The additional hydrogen is also thought to minimize the shadowing etch found at lower dilution, to a more universal etch and deposition mechanism that is predominantly redeposition or reemission dominated, which with a high abstraction rate of SiH_4 from H and Si, is produced and available for redeposition.[39,133] The redeposition of species usually occurs at peaks or crests on the surface. This would increase the film roughness quickly consistent with the observed large static and dynamic scaling coefficients.

It is also possible that the steady state surface coverage of hydrogen limits reactive adsorption and thus is the growth limiting step in this study.[134] In this case, the growth rate is determined by a balance between abstraction, desorption and adsorption of hydrogen on the surface of the substrate. All of these effects are temperature dependent while the abstraction and adsorption of hydrogen are also hydrogen dilution dependent. Hydrogen abstraction should dominate at conditions of high hydrogen dilution.

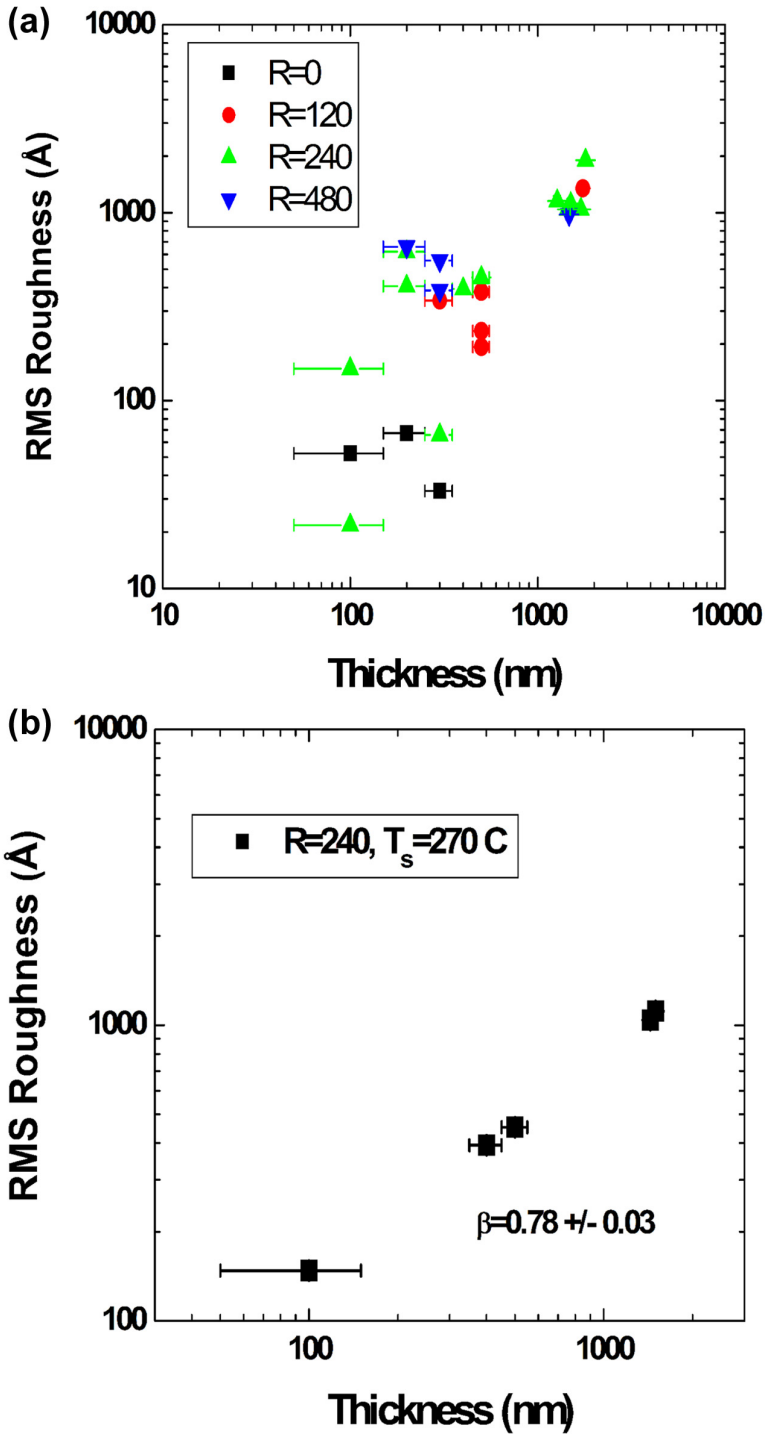

Figure 4.10 (a) The effect of thickness on rms roughness at several dilutions. Substrate temperatures vary from 230-350°C, pressures from 75-120 mTorr, wire to substrate spacings of 3.5 to 5 cm, and wire temperatures from 1350-1550°C. (b) RMS roughness as a function of thickness for films deposited at R=240 and T_s=270°C and less than 1500 nm.

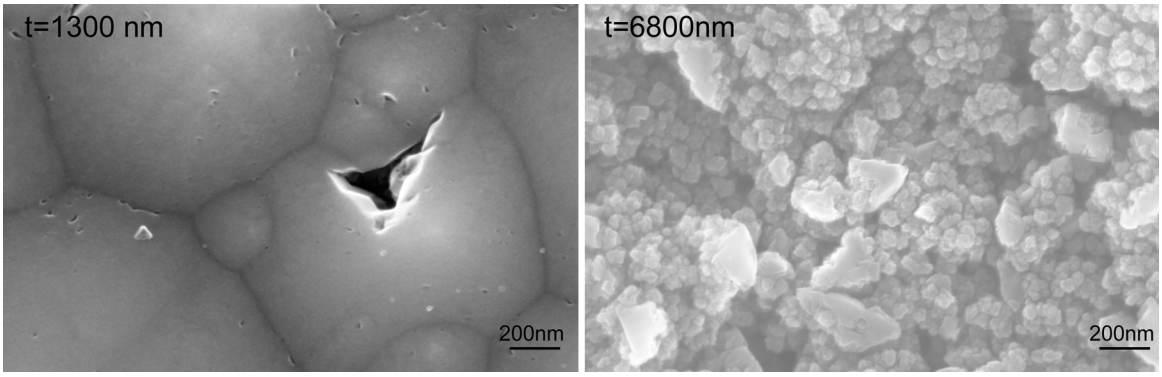

Figure 4.11 SEM images of the surface evolution of a film grown at R=240, T_s = 350°C, 4.2 cm wire to substrate spacing, and 120 mTorr at 1300 nm and 6800 nm at 50kx.

In these growths, the H etching or abstraction mechanism is thought to be extremely important. Otobe *et al.*[135] found that the roughness of H etched Si increased with increasing substrate temperature, consistent with our results. Other possible explanations for the role of hydrogen have been put forth by a number of authors: Nakata *et al.* suggest that the atomic hydrogen coverage or the growing surface enables surface species to have a higher mobility,[84,136] explaining the decrease in roughness with decreasing substrate temperature. Another possible mechanism at high dilutions is the chemical annealing effect.[137,138] The chemical annealing mechanism has been used to explain the low-temperature crystallization of silicon[138] by the insertion of H atoms into the strained Si-Si bonds.[139] The subsequent relaxation of the bonds as the H diffuses through the Si results in the crystallization of the structure. The hydrogen content of our films increases with increasing temperature at a given dilution and with increasing dilution at a given temperature, so that films with more H incorporation appear to have a larger rms roughness. However, there is no immediate correlation with structure, as our films become more epitaxial at higher dilutions and *lower* substrate temperatures.

Although the specific growth mechanism cannot be determined through ex-situ surface studies, given the surface morphology analysis and the fact that the growth rate and the flux of growth species are approximately the same under all discussed growth conditions; hydrogen appears to be the predominant species in determining the growth regime of HWCVD grown

crystalline Si films. At zero hydrogen dilution (R=0), growth is primarily due to the species coming from the wire. At mid-range dilutions (R=120 to 240), growth is still mainly from the wire, but a shadow dominated etch occurs simultaneous with growth which roughens the deposition surface. At the highest hydrogen dilutions (R=480), it is possible that the growth is dominated by the re-deposition of previously H-abstracted and desorbed surface species; i.e., we suggest that at high R, most growth species have been 'recycled' through the sequence of growth →abstraction→desorption→redeposition more than once. The high hydrogen dilution provides a unique deposition environment and growth regime for epitaxial films to grow on rough surfaces.

4.5 Conclusions

It has been shown in this chapter that rms roughness increases with increasing substrate temperature and with increasing hydrogen to silane dilution ratio for crystalline silicon films on silicon substrates. This is similar to the trend seen in amorphous films, but not in other crystalline systems, particularly in the high H dilution regime. This trend is due to the large amount of atomic hydrogen involved in the HWCVD process and allows epitaxial growth to continue, even on the roughest surfaces. Hydrogen dilution is thus found to be the most important factor in determining the growth regime. Films grown without additional hydrogen grow in the random deposition with relaxation regime, while increasing hydrogen leads to shadowing and finally the etching and re-emission growth regime. By varying the deposition parameters, one can control the morphology and structure of these HWCVD epitaxial silicon films and hence tailor each material for a particular device structure.

4.6 References

1. A. H. M. Smets, W. M. M. Kessels, and M. C. M. van de Sanden, App. Phys. Lett. 82 (6), 865 (2002).

2. K. R. Bray and G. N. Parsons, Phys. Rev. B 65, 035311 (2001).

3. D. M. Tanenbaum, A. L. Laracuente, and A. Gallagher, Phys. Rev. B 56 (7), 4243 (1997).

4. D.J. Eaglesham, App. Phys. Rev. 77 (8), 3597 (1995).

5. M. V. R. Murty, "*Ion-surface Interactions and Limits to Silicon Epitaxy at Low Temperatures,*" California Institute of Technology, 1994.

6. N.-E. Lee, David G. Cahill, and J. E. Greene, Phys. Rev. B 53 (12), 7876 (1996).

7. Maribeth S. Mason, "*Synthesis of Large-Grained Polycrystalline Silicon by Hot-Wire Chemical Vapor Deposition for Thin Film Photovoltaic Applications,*" California Institute of Technology, 2004.

8. C. E. Richardson, M. S. Mason, and H. A. Atwater, Mater. Res. Soc. Symp. Proc. 808, A8.11 (2004).

9. C.W. Teplin, E. Iwaniczko, K. M. Jones, R. Reedy, B. To, and H. M. Branz, Mater. Res. Soc. Symp. Proc. 862, A2.3 (2005).

10. J.K. Holt, M. Swiatek, D.G. Goodwin, R.P. Muller, W.A. Goddard III, and Harry A. Atwater, Thin Solid Films 395, 29 (2001).

11. R. E. I. Schropp, K. F. Feenstra, E. C. Molenbroek, H. Meiling, and J. K. Rath, Phil. Mag. B 76 (3), 309 (1997).

12. J. T. Drotar, Y.-P. Zhao, T.-M. Lu, and G.-C. Wang, Phys. Rev. B 62 (3), 2118 (2000).

13. F. Family, J. Phys. A 19, L441 (1986).

14. G. S. Bales, A. C. Redfield, and A. Zangwill, Phys. Rev. Lett. 62 (7), 776 (1989).

15. D. D. Vvedensky, A. Zangwill, C. N. Luse, and M. R. Wilby, Phys. Rev. E 48, 852 (1993).

16. J. Yu and J. G. Amar, Phys. Rev. E 65, 060601(R) (2002).

17. C. H. Horowitz, R. A. Monetti, and E. V. Albano, Phys. Rev. E 63, 066132 (2001).

18. A. Mazur, D. J. Srolovitz, P. S. Hagain, and B. G. Bukiet, Phys, Rev. Lett. 60 (5), 424 (1988).

19. F. Family and T. Vicsek, J. Phys. A 18, L75 (1985).

20. V. Constantoudis, G. P. Patsis, A. Tserepi, and E. Gogolides, J. Vac. Sci. Technol. B 21 (3), 1019 (2003).

21. H.R. Moutinho, C.-S. Jiang, J. Perkins, Y. Xu, B.P. Nelson, K.M. Jones, M.J. Romero, and M.M. Al-Jassim, Thin Solid Films 430, 135 (2003).

22. F. Finger, R. Carius, T. Dylla, S. Klein, S. Okur, and M. Gunes, J. Opt. Adv. Mat. 7 (1), 83 (2005).

23. D.J. Eaglesham, F. C. Unterwald, H. Luftman, D.P. Adams, and S.M. Yalisove, J. Appl. Phys. 74 (11), 6815 (1993).

24. S. Gupta, G. Morell, and B.R. Weiner, J. Non-Crys. Sol. 343, 131 (2004).

25. Christine E. Richardson, M. S. Mason, and Harry A. Atwater, Thin Solid Films 501 (1-2), 332 (2006).

26. G. Ganguly and A. Matsuda, Phys. Rev. B 47, 3661 (1993).

27. C. E. Richardson, M. S. Mason, and H. A. Atwater, Proceedings of the 31st IEEE PVSC, Lake Buena Vista, Fl, 2005.

28. M. Fehrenbacher, J. Spitzmuller, M. Pitter, H. Rauscher, and R. J. Behm, Jpn. J. Appl. Phys. 36, 3804 (1997).

29. K. Sasaki and T. Takada, Jpn. J. Appl. Phys. 37, 402 (1998).

30. D. J. Eaglesham, Appl. Phys. Rev. 77 (8), 3597 (1995).

31. O. P. Karpenko, S. M. Yalisove, and D. J. Eaglesham, J. Appl. Phys. 82 (3), 1157 (1997).

32. J. J. C. Doyle, J. App. Phys. 64 (6), 3215 (1988).

33. Shinya Tange, Keisuke Inoue, Kenichi Tonokura, and Mitsuo Koshi, Thin Solid Films 395 (1-2), 42 (2001).

34. J. K. Holt, "*Hot-Wire Chemical Vapor Deposition of Silicon and Silicon Nitride for Photovoltaics: Experiments, Simulations, and Applications,*" California Institute of Technology, 2003.

35. A. Gallagher, Thin Solid Films 395 (1-2), 25 (2001).

36. T. Karabacak, Y.P. Zhao, G.C. Wang, and T. M. Lu, Phys. Rev. B 66 (7), 075329 (2002).

37. B. A. Sperling and J. R. Abelson, App. Phys. Lett. 85 (16), 3456 (2004).

38. J. Villain and I. Elkinant, J. Phys. I France 4, 949 (1994).

39. T. A. Wagner, "*Low temperature silicon epitaxy: Defects and electronic properties,*" University of Stuttgart, 2003.

40. T. Karabacak, Y.-P. Zhao, G.-C. Wang, and T.-M. Lu, Phys. Rev. B 64, 085323 (2001).

41. J. H. Yao and H. Guo, Phys. Rev. E 47, 1007 (1993).

42. J. T. Drotar, Y.-P. Zhao, T.-M. Lu, and G.-C. Wang, Phys. Rev. B 61, 3012 (2000).

43. A. Masuda, K. Kamesaki, A. Izumi, and H. Matsumura, Mat. Res. Soc. Sym. Proc. 664, A4.5 (2001).

44. K. Werner, S. Butzke, S. Radelaar, and P. Balk, J. Crys. Grwth 136, 338 (1994).

45. M. Otobe, M. Kimura, and S. Oda, Jap. J. Appl. Phys. 33 (7B), 4442 (1994).

46. M. Nakata, A. Sakai, T. Uematsu, T. Namikawa, H. Shirai, J-I Hanna, and I. Shimizu, Phil. Mag. B 63 (1), 87 (1991).

47. P. Reinig, F. Fenske, B. Selle, W. Bohne, J. Rohrich, I. Sieber, and W. Fuhs, Appl. Surf. Sci. 227, 114 (2004).

48. K. Nakamura, K. Yoshino, S. Takeoka, and I. Shimizu, Jpn. J. Appl. Phys. 34, 442 (1995).

49. H. Shirai, D. Das, J-I Hanna, and I. Shimizu, App. Phys. Lett. 59 (9), 1096 (1991).

50. S. Sriraman, S. Argarwal, E. S. Aydil, and D. Maroudas, Nature 418, 62 (2002).

Chapter 5

Thin-film Photovoltaics: Design Issues

5.1 Introduction to Thin-film Photovoltaics

As discussed in Chapter 1, thin-film silicon photovoltaics is a promising device class that has the opportunity to take advantage of the wide literature surrounding silicon technology, while capitalizing on the reduced cost of manufacturing thin-film silicon relative to silicon wafers.[27,31,140] However, it is important to understand the limitations and special design concerns of thin-film devices. This chapter explores the effect of various solar cell parameters and then examines several cases by using a one-dimensional photovoltaic simulation program to determine the expected efficiencies of thin-film large-grained polycrystalline silicon solar cells on glass.

5.2 Design Concerns

When a semiconductor is exposed to solar radiation, photons with energy above the band gap of the material are absorbed. The energy of the photon can excite an electron from the valence band into the conduction band of the semiconductor, creating an electron-hole pair. In a *p*-*n* junction, which exists in a solar cell device, the electric field generated by the difference in the doping levels of the *p*-type and *n*-type layers causes the carriers to separate and accelerates them to the opposite sides of the junction. There they become majority carriers and are collected at the metal contacts of the device.

Figure 5.1 is an equivalent circuit of a solar cell device, which includes the generated current, *p*-*n* diode, shunt resistance, R_{sh}, and the series resistance, R_S, due to the contacts. The diode current under illumination, I, for the solar cell shown in Fig. 5.1 is

$$I = I_L + I_S\left[1-\exp\left(\frac{V+R_sI}{m_{id}V_{th}}\right)\right]-V/R_{sh} \qquad (5.1)$$

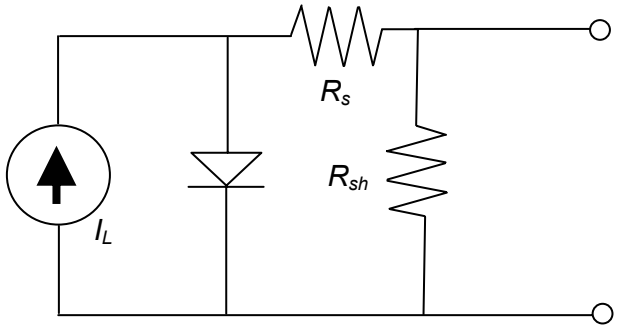

Figure 5.1 Equivalent circuit of a solar cell adapted from Shur.[141]

I_L is the light generated current, I_S is the dark saturation current, V is the applied voltage, m_{id} is the diode ideality factor, and V_{th} is the thermal voltage equal to kT/q where k is Boltzmann's constant, T is the temperature in Kelvins, and q is the charge of an electron. The current-voltage curve for this device in the dark and under illumination is shown in Fig. 5.2. I_{SC} is the short-circuit current and is defined as the current when the voltage is equal to zero. V_{OC} is the open-circuit voltage defined when I=0. For a *n*+/*p* solar cell, I_S for very pure material dominated by Auger recombination[141] is given by Equation 5.2

$$I_S = qSn_i^2\left(D_nC_p\right)^{1/2}\coth\left(W_p/L_n\right) \qquad (5.2)$$

where S is the surface recombination velocity, n_i is the intrinsic carrier concentration, D_n is the electron diffusion coefficient, C_p is the Auger coefficient equal to $9.9\text{x}10^{-32}$ cm^6/s for *p*-type Si,[142] W_p is the width of the *p*-type region, and L_n is the electron diffusion length.[141] Then the open circuit voltage is given by Equation 5.3 below.

$$V_{oc} = m_{id} V_{th} \left\{ \ln \left[\frac{I_L}{qSn_i^2 (D_n C_p)^{1/2} \coth(W_p / L_n)} + 1 \right] + \ln \frac{V_{oc}}{R_{sh}} \right\} \quad (5.3)$$

V_{oc} is the most demanding material characteristic for a solar cell as it accounts for surface recombination, material diffusion lengths, the shunt resistance, the generation of carriers, and the ideality of the junction without the device-related complications of contact formation and current collection. The magnitude of the current collected from the solar cell is governed by the absorption and the carrier recombination characteristics of the material, as well as by the contact design.

The fill factor of a solar cell captures the effect of the series and shunt resistance on the illuminated current-voltage curve (Fig. 5.2) and is defined by

$$FF = \frac{P_{\max}}{I_{sc} V_{oc}} \quad (5.3)$$

and is always less than 1. At the maximum power point, the current and the voltage are defined as I_{max} and V_{max}. The efficiency of a photovoltaic device is then defined by the ratio of the maximum power output to the power in:

$$\eta = \frac{P_{\max}}{P_{in}} = \frac{I_{sc} V_{oc} FF}{P_{in}} \quad (5.4)$$

5.2.1 Optical absorption

Because crystalline silicon is an indirect band gap semiconductor, the device must be thick enough to absorb enough incident photons to generate the device current. To absorb over 85% of the incident photons at or above the band gap, the active layer of a silicon photovoltaic device must be at least 30 μm thick.[143] In a thin-film device, a 30 μm effective thickness can be achieved in a thinner cell by increasing the optical path length by using textured surfaces,[144-146] an anti-reflective coating,[144] and/or a back-reflecting surface (Fig. 5.3), where the path length due to a textured surface increases the optical thickness by $1/\cos\theta$.[141,147]

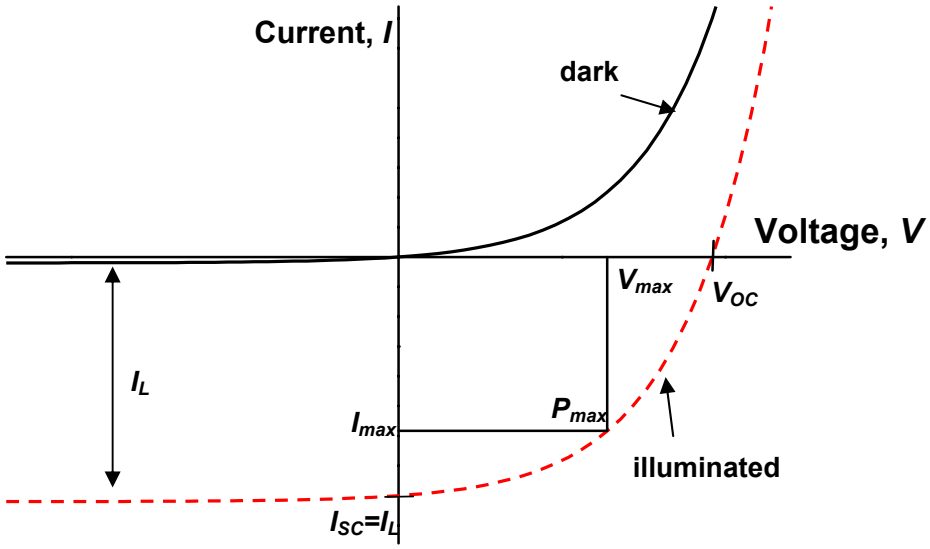

Figure 5.2 Current-voltage characteristics of a *p-n* diode under dark (solid) and illuminated (dashed) conditions.

The enhancement in absorption due to light trapping depends on the structure of the surface texture. The goal is to decrease the reflectance of the front surface as much as possible while internally reflecting all of light for rays reflected from the back surface. A random surface texture gives near optimal light trapping to a solar cell.[144-146,148]

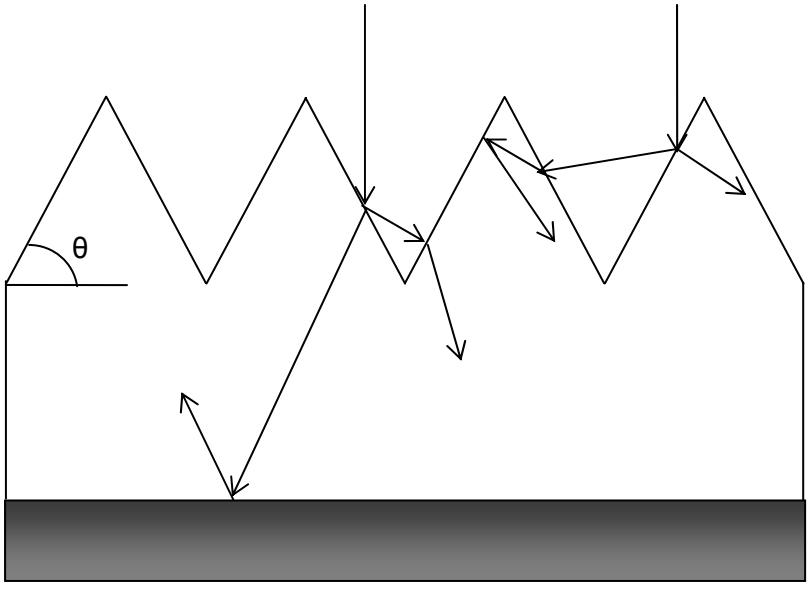

Figure 5.3 Light trapping due to scattering and total internal reflection in a textured cell with a reflective back surface.[141]

5.2.2 Grain boundaries

Grain boundaries decrease the efficiency of carrier collection by acting as recombination sites. To minimize the presence of grain boundaries, it is important to have grain sizes greater than the thickness of the device, which is the maximum distance carriers must travel in order to be collected. To decrease the electrical activity of the dangling bonds in the grain boundaries, hydrogen can be introduced either during low-temperature deposition[43] or by post-deposition techniques.[31,42,44] A hydrogen atom can occupy the dangling silicon bond, thereby passivating the grain boundary.

For the large-grained polycrystalline devices of concern in this thesis, there are several sources of grain boundaries. One is the polycrystalline template, which has grain boundaries from the crystallization process. These grains are then grown into the epitaxial layer. Aside from the grains present in a polycrystalline template, even more grains will develop with the breakdown of epitaxial growth on a template. If breakdown occurs more quickly for a certain crystallographic texture, there will be more grains in the material of that texture.[34,76] For example in films deposited under the same conditions by electron-cyclotron resonance CVD, the critical epitaxial thickness was greatest for films grown on a (100) surface, less for films on a (311) surface, and even less for those grown on a (111) surface.[34] This is also most likely true of HWCVD, as shown by the drastically different surface morphologies (Figs. 5.4-5.6), however the orientation dependence of the critical epitaxial thickness has not been studied.

5.2.3 Crystallographic orientation

Intra-granular defects within individual grains are problematic in low-temperature polycrystalline silicon thin-film devices and are also substrate orientation dependent.[149] Epitaxial growth on (111) surfaces by low-temperature methods results in films with more stacking faults than those grown on (100) surfaces and hence lower diffusion lengths.[149,150] Consequently, polycrystalline templates with a preferred texture in the (100) orientation are desired.

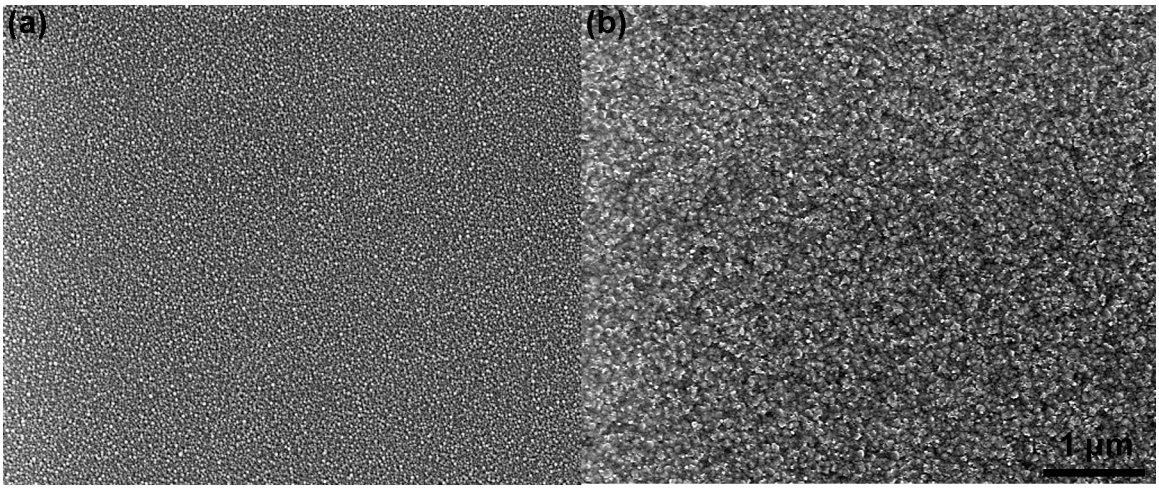

Figure 5.4 Surface morphologies at 10kx magnification of a 135 nm film grown at 270°C and R=90 on (a) Si (111) and (b) Si (100).

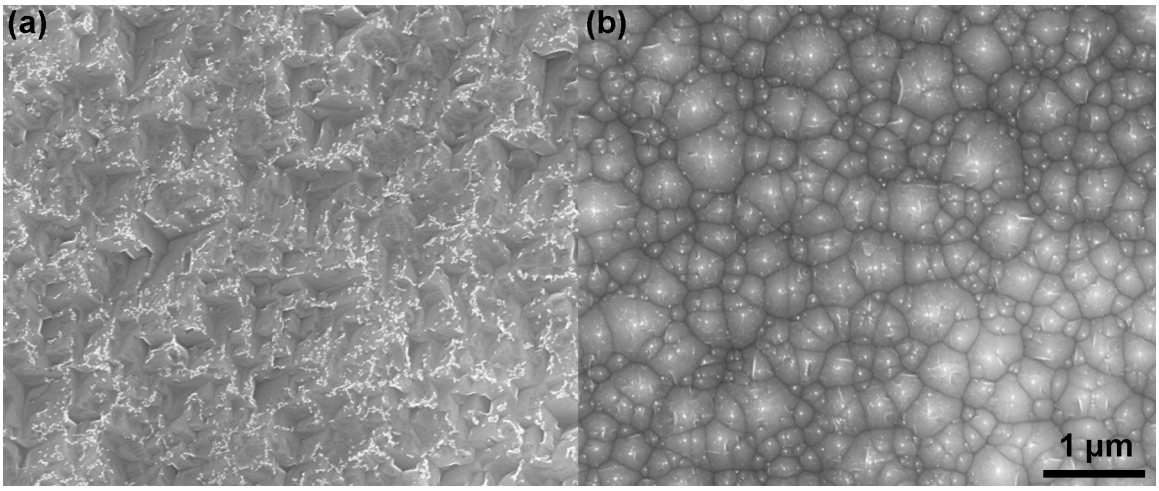

Figure 5.5 **S**urface morphologies at 10kx magnification of a ~250 nm film grown at 270°C and R=340 on (a) Si (111) and (b) Si (100).

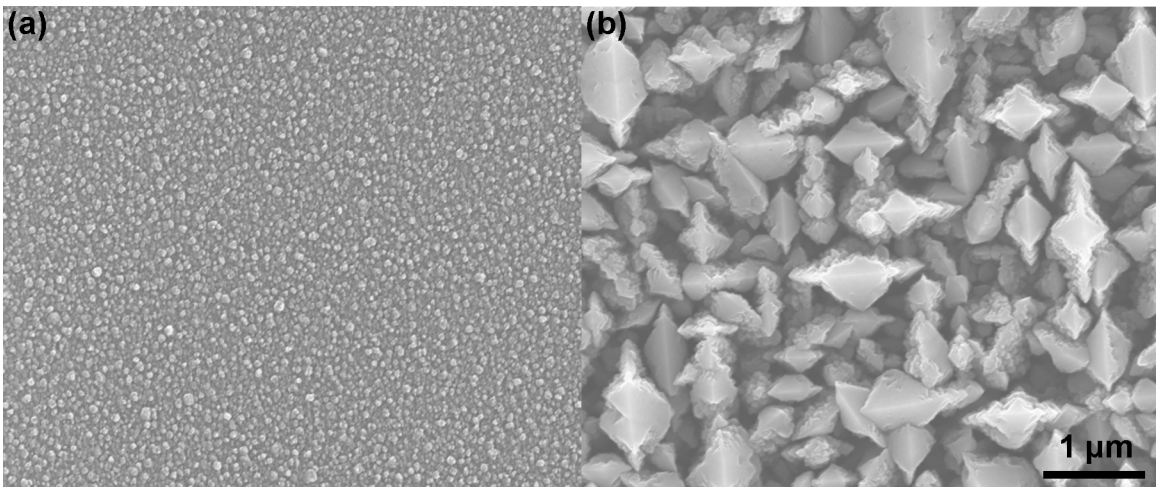

Figure 5.6 Surface morphologies at 10kx magnification of a 2 µm film grown at 270°C and R=180 on (a) Si (111) and (b) Si (100).

5.2.4 Bulk passivation

Low temperature depositions and epitaxy on most templates require a post-deposition hydrogenation treatment to decrease the electrical activity of grain boundaries, dislocations,[151] and point defects within the bulk. Poor minority carrier diffusion lengths and device properties are improved with hydrogenation.[31,42,44,150,152]

5.2.5 Gettering

Gettering is the process of moving a metallic impurity into an appropriate sink where it cannot electrically interact with carriers in the active area of the device. $POCl_3$ phosphorus diffusion is often used as both a getter and a back surface field (see 5.2.6).[153]

5.2.6 Surface passivation

Due to the smaller bulk-to-surface ratios of thin-films, surface recombination plays an extremely important role in the quality of a thin-film device. The surface recombination velocity is dependent on the energy levels of the surface states, the density of states, the capture cross-section, the doping level, and the carrier injection level.[154] Surface recombination can be reduced by depositing a dielectric film, such as silicon dioxide or silicon nitride, on the surface, which not only decreases the surface trap density, but also leads to a field-effect passivation due to the fixed oxide charges.[155,156] Silicon nitride (SiN) appears to be the most effective anti-reflective coating (ARC) and surface passivation layer and is the industry standard.[154,156] Nitride films are often deposited with an excess of hydrogen so that hydrogen passivation of the bulk can occur by diffusion of this excess hydrogen during contact firing at elevated temperatures, giving SiN a competitive advantage over an oxide passivation.[40,156] The surface recombination velocity for a nitride-passivated Si surface is higher at grain boundaries than in the bulk, 500 versus 30 cm/s, another motivator for large grain sizes.[153] The surface recombination velocity is reduced by including a built-in back surface field by heavily doping the region near the surface. This heavily

doped region reflects minority carriers away from the surface and is often done in conjunction with a gettering step as mentioned in Section 5.2.5.[154]

5.3 Ideal Efficiency

PC-1D is a valuable one-dimensional modeling tool for understanding how material properties and device design affect the solar cell device quality.[157] It includes useful tools, which account for such properties as the effect of texture, back reflectors, series resistance, and shunt resistance for ease in modeling thin-film devices.

A 5 μm thick absorber grown on a 100 nm *n*+ template with a <111> faceted 100 nm thick amorphous silicon emitter (*p*+ type $1x10^{19}$ cm^{-3}), would have an expected ideal efficiency of 15.2%, assuming perfect internal reflectance, a perfect back reflector, no surface recombination, and a diffusion length of 25 μm in the bulk[149] (Fig. 5.7). *Note that because PC-1D is a one-dimensional program, grain boundaries and grain boundary recombination must be considered as an effective medium layer with the bulk. In this case the grain boundaries are included through the diffusion length or lifetime of the material.* With a crystalline silicon emitter, the efficiency rises to 16.7%. However, this calculation neglects carrier recombination at the junction. Grain boundaries at the junction are especially deleterious to solar cell performance.[42] Therefore, it is advantageous to have an amorphous emitter. The amorphous layer decreases the number of grain boundaries on the highly doped side of the junction. And, since the recombination velocity at the *p/n* junction in a real system is not zero, the amorphous layer serves as an passivation layer at the crystalline surface.[158,159] Efficiencies of 20.8% have been achieved for a *p*+-type amorphous Si emitter on a *n*-type monocrystalline solar cell.[160]

A thickness of 5 μm is chosen as a balance between the optical thickness and the cost of depositing a thin-film. While ideally one would want the thickness to be on the order of the diffusion length (Fig. 5.8), there are other throughput limits to the thickness one can achieve.

Currently the highest deposition rate for the films of interest is ~15 nm/min, the average growth rate is closer to 5 nm/min. With the highest growth rate, it would take 5.56 hrs to deposit a 5 µm thick film, the average growth rate would take 16.67 hrs. Because of the low growth rates, HMI[44] and UNSW[31] have limited their films to a thickness of 2 µm. We have chosen to target a 5 µm thick absorber layer, in the expectation that the growth rates of epitaxial HWCVD grown films can be increased with further optimization.

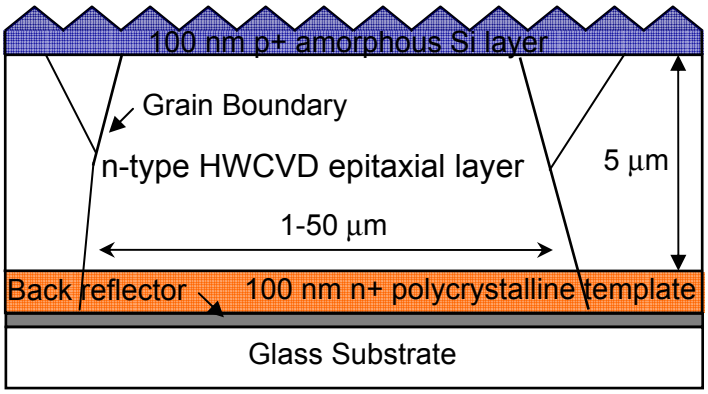

Figure 5.7 Example of a solar cell made from epitaxially thickening a polycrystalline template.

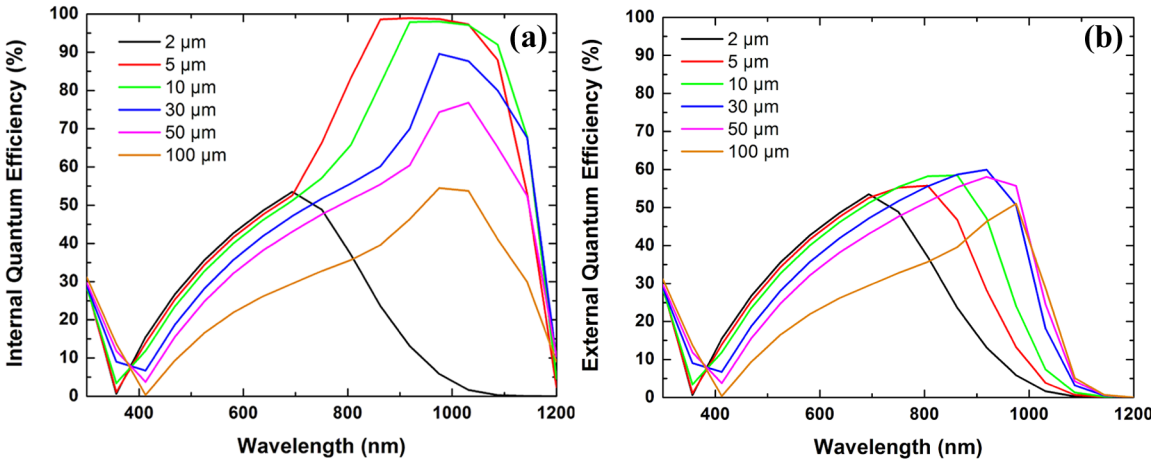

Figure 5.8 (a) Internal and (b) External quantum efficiencies of *p+/n/n+* silicon device shown in Fig. 5.4 with varying *n*-layer thicknesses for a layer with a 25 µm diffusion length as calculated by PC-1D.

5.4 Deviations from Ideality

In an actual solar cell device, there is some series resistance due to the contacts. The target resistance of the contacts in order to minimize their effects is on the on the order of 0.010

Ωcm^2, which is extremely low.[161] Moreover, the contacts may not be perfectly ohmic, which could create a small tunneling barrier and an electric field in the semiconductor attracting minority carriers to the contact and creating a surface recombination site.

Furthermore, there will be a parallel shunt resistance due to carrier mobility along the grain boundaries. The effect of the shunt resistance depends upon whether or not the grain boundaries are decorated with contaminants[162] or are passivated,[42] which would decrease and increase the shunt resistance, respectively. If the PC-1D device model is adjusted for more realistic conditions and we assume that recombination at the grain boundaries decreases the diffusion length in the absorber layer to 5 μm,[31,149] that the surface recombination velocities on the front and back of $1x10^4$ cm/s, that there is a cell with shallow texturing of 15° on the front surface (Fig. 5.3),[57] non-ideal reflectance of 10% at the front surface, 50% reflectance at the back surface, and 50% internal reflectance (reflectance of light rays reaching the front surface from inside the cell), then the expected efficiency of a device with an amorphous emitter, described above in Section 5.3, is 8.5%, down from 15.2% for an ideal cell, as modeled by PC-1D. In summary, one must be extremely careful with the device and the material process design in order for a large-grained polycrystalline thin-film device to reach an ideal 15% efficiency.

5.5 Present Limitations to Efficiency

The record efficiency for an epitaxially thickened large-grained polycrystalline solar cell is currently 3%, which was achieved for a 2 μm device with an *n*-type absorber layer fabricated at the University of New South Wales by ion-assisted deposition.[31] This device was without texture, which decreased the optical thickness of the cell and the number of absorbed photons.[31] With optimized doping and texturing, and the assumptions made earlier for a practical efficiency limit, this device could get to ~6% efficiency, as calculated by PC-1D, without any improvements in the material properties. By optimizing the deposition parameters, the post-deposition

treatments, the contact structure, and the texture of the cell; expected efficiencies improve to over 10%.[31] This is lower than the ideal 15% efficiency for the devices developed in this thesis due to the thinner absorber layer thickness.

5.6 Conclusions

Thin-film crystalline silicon photovoltaics on glass offer a novel path to decrease manufacturing costs; however, because of their smaller dimensions and high surface to bulk ratio, extra consideration must be taken in designing a device. Sources of loss in a polycrystalline thin-film device are grain boundaries, intra-granular defects, junction recombination, and limited absorption; while most thin-film devices are dominated by surface recombination and high losses due to the shunt and series resistance. These limitations can be overcome by hydrogen passivation, dielectric anti-reflection coatings, amorphous emitters, and light trapping. A 5 μm thick target for the epitaxial active layer of the device is chosen as a balance between the deposition time and the optical thickness. The current record efficiency for an epitaxially thickened large-grained polycrystalline solar cell is 3%. This is due to the main sources of loss expressed above and reinforces the need for careful device and material design in order to obtain a 15% efficient device.

5.7 References

1. A. Slaoui, R. Monna, J. Poortmans, T. Vermeulen, O. Evrard, K. Said, and J. Nijs, Journal of Materials Research **13** (10), 2763 (1998).

2. A. G. Aberle, Proceedings of the 4th IEEE WCPEC, Waikoloa, HI, 2006.

3. P. A. Basore, Proceedings of the 4th IEEE WCPEC, Waikoloa, HI, 2006.

4. M. Shur, *Physics of Semiconductor Devices*. (Prentice-Hall, 1990).

5. J. Dziewior, Applied physics letters **31** (5), 346 (1977).

6. T. H. Wang, T. F. Ciszek, C. R. Schwerdtfeger, H. Moutinho, and R. Matson, Solar Energy Materials And Solar Cells **41-2**, 19 (1996).

7. E. Yablonovitch, J. Opt. Soc. Am. **72** (7), 899 (1982).

8. D. Thorp and S. R. Wenham, Sol. Ener. Mat. and Sol. Cells **48**, 295 (1997).

9. M. A. Green, Progress in photovoltaics **10** (4), 235 (2002).

10. A. Goetzberger, Proceedings of the 15th IEEE Photovoltaic Specialists Conference, Orlando, Fl, 1981.

11. R. Brendel, *Thin-Film Crystalline Silicon Solar Cells: Physics and Technology*. (Wiley-VCH, 2003).

12. J. K. Rath, A. Barbon, and R. E. I. Schropp, J. Non-crys. Sol. **227**, 1277 (1998).

13. R. Brendel, R. B. Bergmann, B. Fischer, J. Krinke, R. Plieninger, U. Rau, J. Reiss, H. P. Srunk, H. Wanka, and J. H. Werner, Proceedings of the 26th PVSC, Anaheim, CA, 1997.

14. B. Rau, J. Schneider, E. Conrad, and S. Gall, Proceedings of the Mat. Res. Soc. Sym., San Francisco, 2006.

15. B. Rau, I. Sieber, B. Selle, S. Brehme, U. Knipper, S. Gall, and W. Fuhs, Thin Solid Films **451-452**, 644 (2004).

16. J. Platen, B. Selle, I. Sieber, S. Brehme, U. Zeimer, and W. Fuhs, Thin Solid Films **381** (1), 22 (2001).

17. T. A. Wagner, L. Oberbeck, R. B. Bergmann, and J. H. Werner, Sol. State Phen. **80-81**, 95 (2001).

18. D. H. Neuhaus, Sol. Ener. Mat. and Sol. Cells **74** (1-4), 225 (2002).

19. M. Kittler and W. Seifert, in *Gettering And Defect Engineering In Semiconductor Technology* (2004), Vol. 95-96, pp. 197.

20. Z. C. Liang, Solar energy materials and solar cells **80** (2), 181 (2003).

21. O. Palais, M. Lemiti, J. F. Lelievre, and S. Martinuzzi, in *Gettering And Defect Engineering In Semiconductor Technology Xi* (2005), Vol. 108-109, pp. 585.

22. A. G. Aberle, Solar Energy Materials and Solar Cells **65** (1-4), 239 (2001).

23. M. Kunst, F. Wunsch, O. Abdallah, and G. Citarella, Sold State Phenomena **108-109**, 327 (2005).

24. A. G. Aberle, Progr. Photovolt. **8** (5), 473 (2000).

25. M. Stavola et al., Proceedings of the 14th Workshop on Crystalline Si Cells and Modules, 2004.

26. P. A. Basore, IEEE Transactions on Electron Devices **37** (2), 337 (1990).

27. T. H. Wang, E. Iwaniczko, M. R. Page, D. H. Levi, Y. Yan, V. Yelundur, H. M. Branz, A. Rohatgi, and Q. Wang, Proceedings of the 31st IEEE PVSC Meeting, Lake Buena Vista, FL, 2005.

28. T. H. Wang, E. Iwaniczko, M. R. Page, Q. Wang, D. H. Levi, Y. Yan, Y. Xu, and H. M. Branz, Mater. Res. Soc. Symp. **862**, A23.5.1 (2005).

29. H. Sakata, T. Nakai, T. Baba, M. Taguchi, S. Tsuge, K. Uchihashi, and S. Kiyama, Proceedings of the IEEE Photovoltaic Specialist Conference, Anchorage, 2000.

30. L. M. Porter, A. Teicher, and D. L. Meier, Sol. Ener. Mat. and Sol. Cells **73**, 209 (2002).

31. T. Yamazaki, Japanese Journal of Applied Physics. Parts 1 & 2 **45** (4A), 2441 (2006).

32. C.E. Richardson, Y.-B. Park, and H. A. Atwater, Phys. Rev. B **73** (24) (2006).

Chapter 6

Optical and Electrical Properties of Low-Temperature HWCVD Epitaxial Films

6.1 The Properties of Epitaxial films on Si (100) Substrates

In order to separate the properties of HWCVD epitaxial grown films from the device properties and design issues of HWCVD epitaxially thickened large-grained polycrystalline templates; epitaxial films on Si (100) substrates were evaluated. The first device discussed in this chapter is an epitaxial *n*-type emitter layer grown on a *p*-Si (100) substrate (Fig. 6.1a). In this design, the quality of HWCVD grown epitaxial film is harder to decouple from the properties of the substrate because of the relative thicknesses, however the device is easiest to fabricate. The second device is an *n*-type absorber grown on an *n*+-type Si (100) substrate with a HWCVD grown *p*-type amorphous Si emitter layer (Fig. 6.1b). In this design, the entire active region of the device is grown with HWCVD, and in theory, this is a much better indicator of the potential of these films. However, difficulties with the emitter layer may prevent an accurate audit on the potential of this device. Both of these devices are evaluated for their optical and electrical properties using several methods including the reflectance, photocurrent contrast microscopy, quasi-steady state open circuit voltage measurements, efficiency measurements, and one-dimensional photovoltaic modeling.

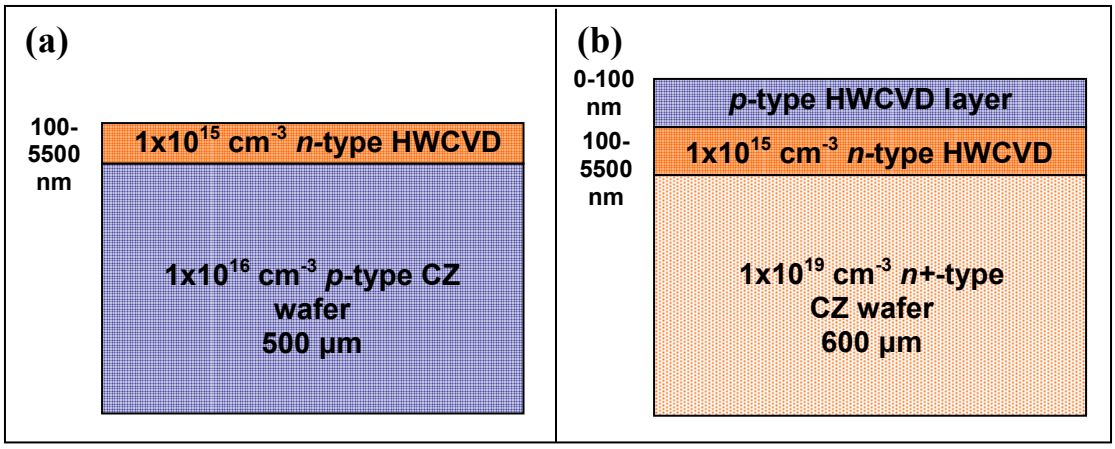

Figure 6.1 Devices fabricated with a HWCVD *n*-type epitaxial layer (a) *p-n* junction with thin-film as the emitter. (b) *n+/n/p+* device with thin-film as the absorber.

6.2 Optical Properties

The as-grown texturing of epitaxial and polycrystalline films grown on Si (100) substrates was evaluated using reflectance data collected through a spectroscopic ellipsometer. For the films discussed in detail in Chapter 4, grown at substrate temperatures between 230 and 350°C and R=H_2/SiH_4 ratios of 0 to 480, a representative reflectance measurement for films grown at 270°C is compared to a bare Si (100) wafer and is shown in Fig. 6.2.[33] The reflectance for all films is decreased relative to that of the silicon substrate. The roughest films, grown at 350°C under high hydrogen dilution, have the lowest reflectance.[33,57]

Figure 6.3 shows an atomic force microscope (AFM) line scan for a representative film grown at 270°C and R=240. Although the AFM tip is too large, between 10 and 40 nm with a 35° front angle,[163] to have enough resolution to determine the crystallographic texture of the growth facets (Figs. 4.2, 4.3), the angles calculated from this scan can be considered minimums. If we consider a 5 µm *n+/n/p+* device discussed in Chapter 5, the efficiency increases by 10% with a 20° texture, which is 50 nm deep, when compared to a flat film as modeled by PC-1D. Moreover, because the surfaces are porous[164] and rough[145] as characterized by SEM and TEM (Figs. 6.4, 6.5), Lambertian light trapping,[146] which is near optimal for a thin-film photovoltaic device,[148] may apply.

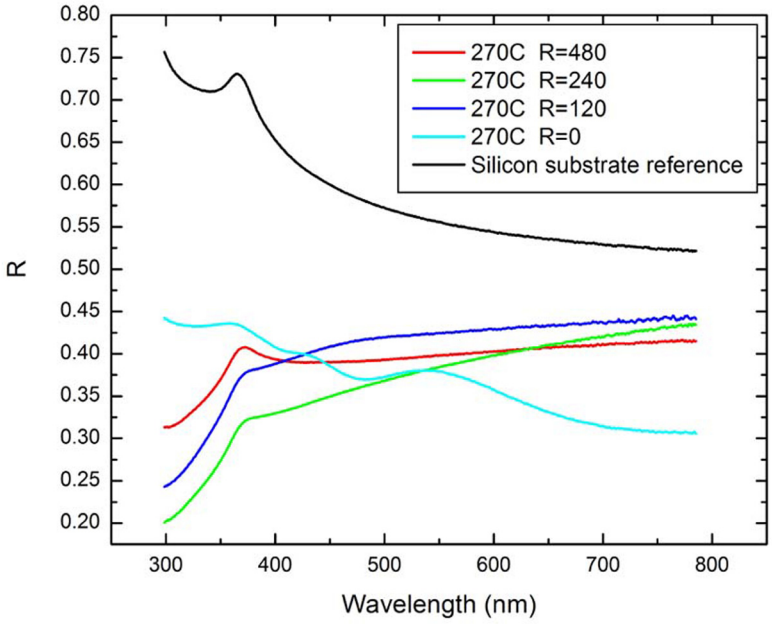

Figure 6.2 Representative reflectance spectrum of epitaxial and crystalline Si thin-film samples grown on a silicon substrate compared with a bare silicon substrate at 270°C and H_2/SiH_4 ratios of R=0, 120, 240, 480.

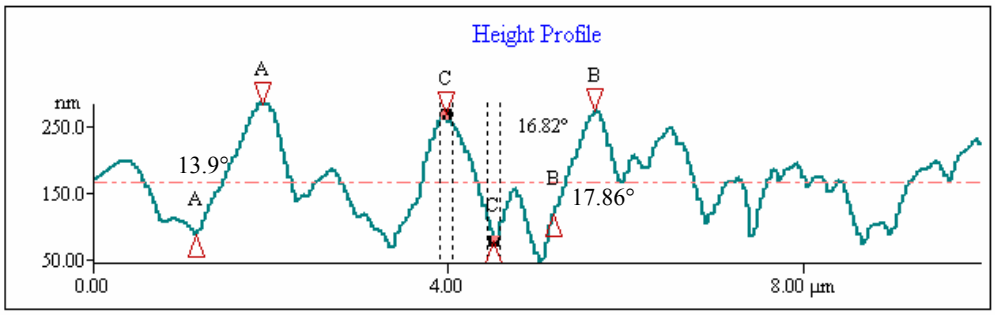

Figure 6.3 AFM line scan of film grown at 230°C, R=240 with typical angles of the surface structures.

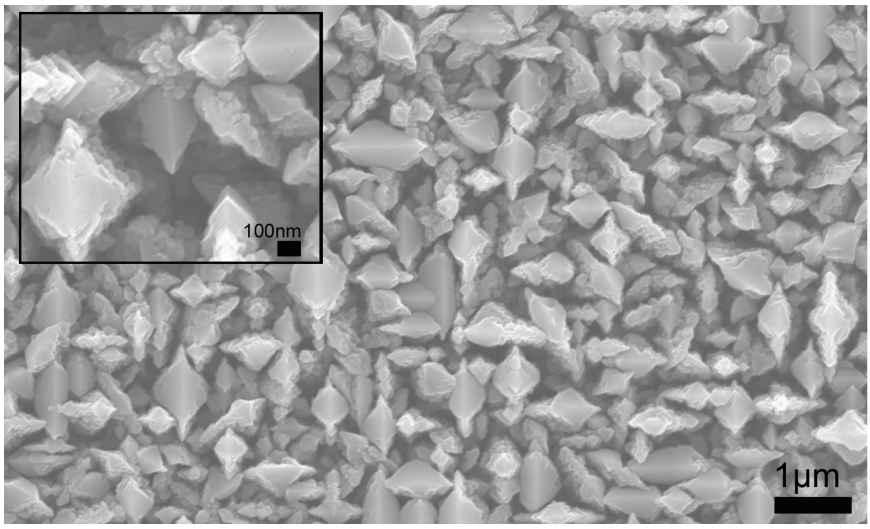

Figure 6.4 SEM image of 2 μm thick film grown at 270°C and R=180 showing large angle facets.

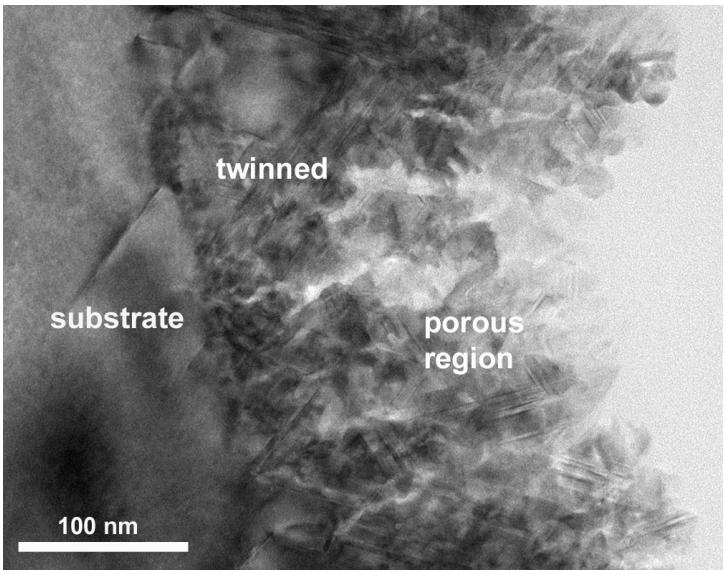

Figure 6.5 TEM cross-section of film grown at 350°C and R=120.

6.3 Near-Field Photocurrent Contrast Microscopy

Because of the rough surfaces of the HWCVD epitaxial films grown under the conditions of high hydrogen dilution shown in Chapter 4, there is the possibility that dislocation and twin boundary recombination will follow the morphology of the surface features. Defects along these morphological structures would be detrimental to the device, as they would be a low shunt resistance path for carriers. To help determine the electric nature of these features, several

samples were scanned and analyzed using near-field photocurrent contrast microscopy (NPC) (Fig. 6.6) by Magnus Wagener and George Rozgonyi at North Carolina State University.

During the NPC measurements, an optical probe with an aperture of roughly 100 nm is scanned at a constant height of approximately 20 nm across the sample surface, a much smaller distance than the wavelength of light, 632 nm. Under near-field conditions, the excitation source produces an excitation volume localized within a wavelength below the surface. It is therefore anticipated that most of the generation will take place within the measured 5.5 μm thick epitaxial silicon film (Fig. 6.7). The reflected light is also measured during the NPC measurement in order to aid in interpretation of the NPC image.

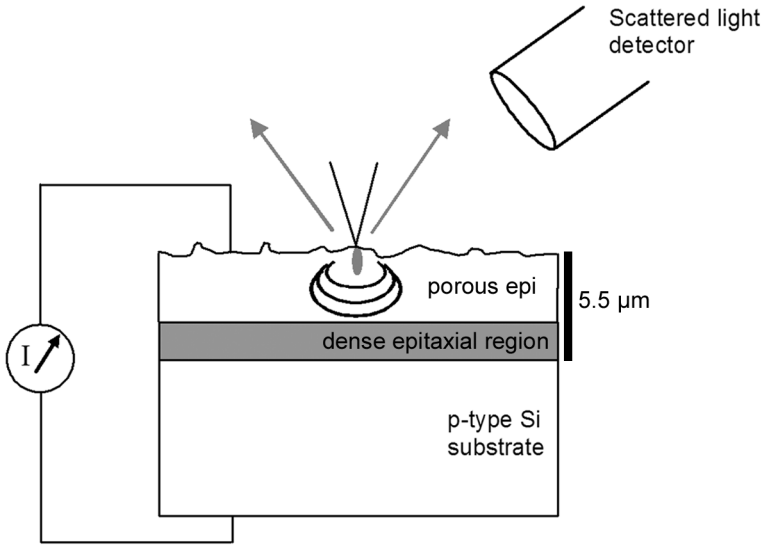

Figure 6.6 Schematic of the near-field photocurrent experiment using an *n/p* junction from Wagener et al.[165] The NPC image is obtained by moving the tip with respect to the sample.

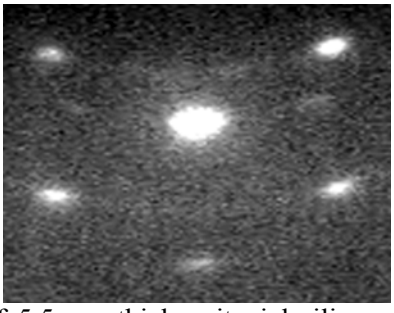

Figure 6.7 RHEED pattern of 5.5 μm thick epitaxial silicon film under investigation in this section. From this image it appears that the film is starting to twin.

Figure 6.8 depicts the morphology, near-field photocurrent contrast map, and reflectance map of a 5.5 μm *n*-type film grown on a *p*-type substrate at ~300°C, R=60, and a total pressure of 75 mTorr measured by Near-Field Scanning Optical Microscopy (NSOM) and a scattered light detector. The surface features appear to be slightly elongated, with the feature size typically around 500 nm. The corresponding NPC map shows some correlation between the NPC images and the surface morphology, but the regions in the photocurrent and reflectance maps appear to be larger than the surface morphological structures. This could be due to the roughness of the film, which would cause a non-uniform absorption, a non-uniform surface passivation.[166] The low total current is due to the evolution of hydrogen during the contact anneal. Although these results are somewhat inconclusive, NPC will be a valuable tool in the future to understand the carrier recombination mechanisms in HWCVD grown films and in decreasing the inhomogeneity of the electrical properties of these films.

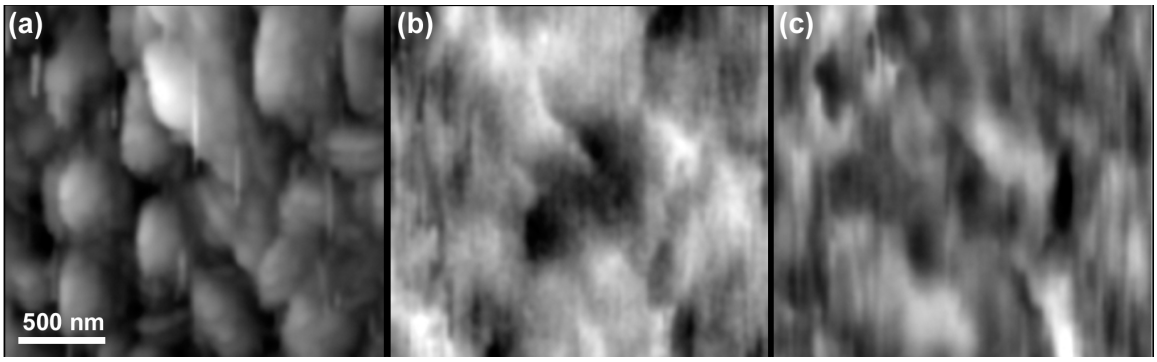

Figure 6.8 (a) Morphology as measured by NSOM, (b) corresponding photocurrent and (c) reflectance maps of a 5.5 μm *n*-type HWCVD film on a *p*-type substrate grown at ~300°C and R=60. The gray scale represents a 320 nm height variation, a 5% change in photocurrent, and a 54% change in reflectance (increasing from black to white). The maximum current is ~2 nA.

6.4 HWCVD Epitaxial Emitters on Si Substrates

As seen above, an epitaxial film does not necessarily ensure good electrical or device properties, so a key criterion for characterization is needed. Here, we correlate the morphology and structure with a key cell performance parameter, the open-circuit voltage, V_{oc}. For electrical testing, *n*-type films with active doping concentrations of 1 x 10^{15} cm^{-3} were grown on CZ-grown

p-type Si (100) with doping concentrations of 1 x 10^{16} cm^{-3} and the open circuit voltages were evaluated with a Sinton Consulting Suns-V_{oc} system.[167] With this method, one can evaluate the material quality without contact metallization, thereby simplifying the study of photovoltaic materials without the complications of forming an ohmic contact. With the open-circuit voltage and the device structure, one can then model the device in PC-1D to determine the effective properties of the HWCVD grown emitter including the shunt resistance, surface passivation, the generation of carriers, and the ideality of the junction. Although the doping concentrations are not ideal for such a device, the measurements and subsequent modeling provide valuable information about the device quality of low-temperature HWCVD epitaxial films.

6.4.1 Quasi-steady-state open-circuit voltage measurements

By simultaneously measuring the open-circuit voltage of a solar cell and the incident light intensity of a slowly varying flash lamp, one can determine the open circuit of a device at any point in the solar cell fabrication process after the junction formation. This method is called the quasi-steady-state open-circuit voltage method (qss-V_{oc}), and is described in detail by Sinton and Cuevas.[167]

6.4.2 As-deposited films

The estimated maximum achievable V_{oc} for devices made from growing an *n*-type emitter on a *p*-type substrate is 438 mV for 125 nm films and 439 mV for 885 nm films as modeled by PC-1D. The maximum V_{oc} is limited by the non-optimal doping concentrations of the layers. Figure 6.9 illustrates the surface morphology of 125 nm twinned films grown at 270°C under different hydrogen dilutions (R = 45, 90, 180). The initial measured open circuit voltages and voltages measured after one week are shown in Figures 6.10 and 6.11. Since all of these 125 nm thick films are twinned epitaxial layers, the surface morphology and evolution likely plays a role in the differences in V_{oc}, probably due to enhanced light trapping and/or increased surface area. The highest stabilized V_{oc}, 350 mV, was observed for 885 nm thick films deposited at R=90 (Fig.

6.11). This is probably due to its denser structure compared to the other films as seen in Fig. 6.9, which leads to less surface recombination due to the smaller surface area.

6.4.3 PC-1D modeling of HWCVD emitter devices

The open-circuit voltage of films grown at R=45 and a substrate temperature of 270°C were measured with the Suns-V_{oc} system as-deposited and then after one week (Fig. 6.12). The one week open-circuit voltages were then modeled with PC-1D to determine the quality of the HWCVD emitter layers and paths for improvement in the HWCVD films and devices.

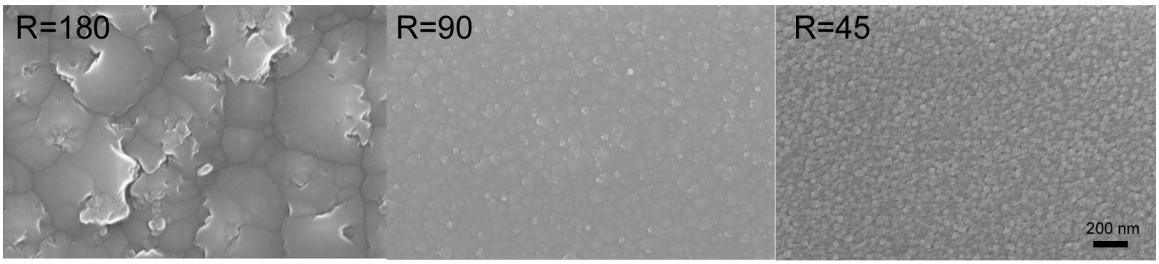

Figure 6.9 SEM Micrographs of 125 nm thick twinned epitaxial films grown at 270°C and under different hydrogen dilutions (R).

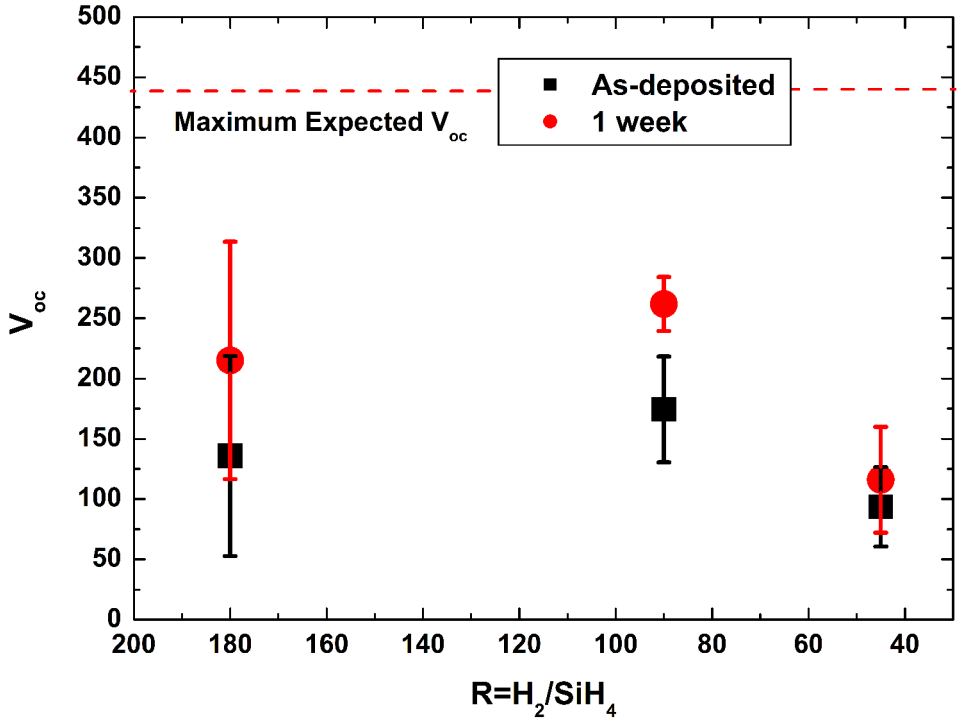

Figure 6.10 Open-circuit voltages of *n*-type 125 nm thick twinned films shown in Fig. 6.6 on a *p*-type substrate as-deposited and after one week.

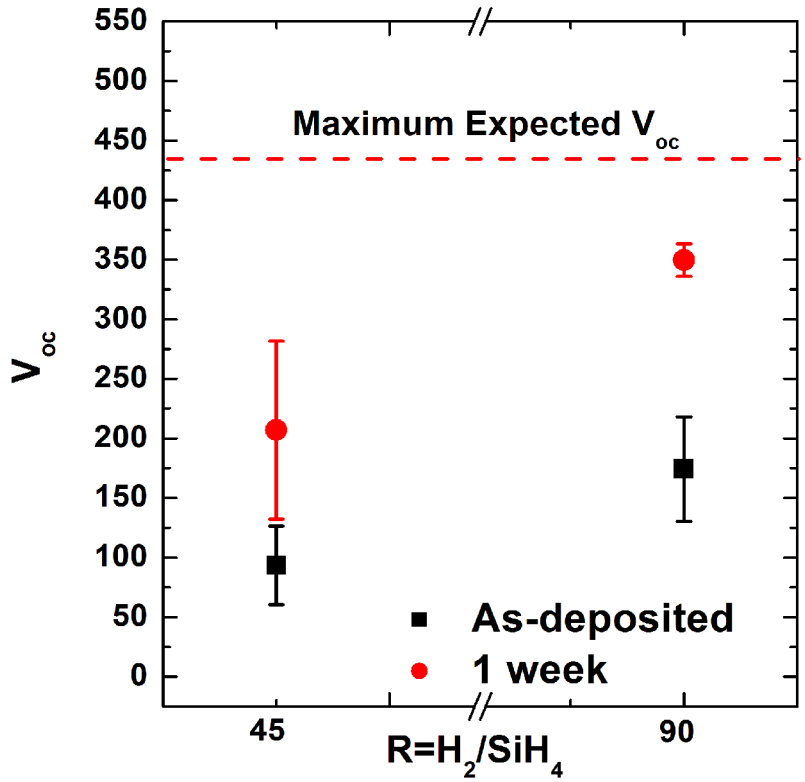

Figure 6.11 Open-circuit voltages for *n*-type 885 nm thick films twinned films on a *p*-type substrate as-deposited and after one week.

Several assumptions are made in order to model the device. There is no front, rear, or internal reflectance and no series resistance. The 500 μm CZ-silicon substrate is assumed to have a lifetime of 30 μs,[168] with a back surface recombination velocity, S_B, of $1x10^4$ cm/s. The front surface recombination velocity, S_F, of the native oxide passivated HWCVD is assumed to also be $1x10^4$ cm/s and includes the texture of the film as estimated by SEM and comparing it to similar AFM measurements (Table 6.1).

A low shunt resistance path had to be added to the model, in order to decrease the open-circuit voltages to the measured values. This shunt resistance could arise from defects at the junction due to the vacuum break before deposition of the HWCVD layer or could be due to low resistance paths following the surface morphology as discussed in section 6.3.

The efficiency of each device is then calculated for these films without a series resistance contribution. The efficiencies for the films grown at 270°C and R=45 are calculated with the

above assumptions by PC-1D to be ~3.8%, with an I-V curve that looks very resistive. Post-deposition hydrogen passivation treatments and SiN surface passivation layers and anti-reflective coatings are expected to improve the device properties of these films.

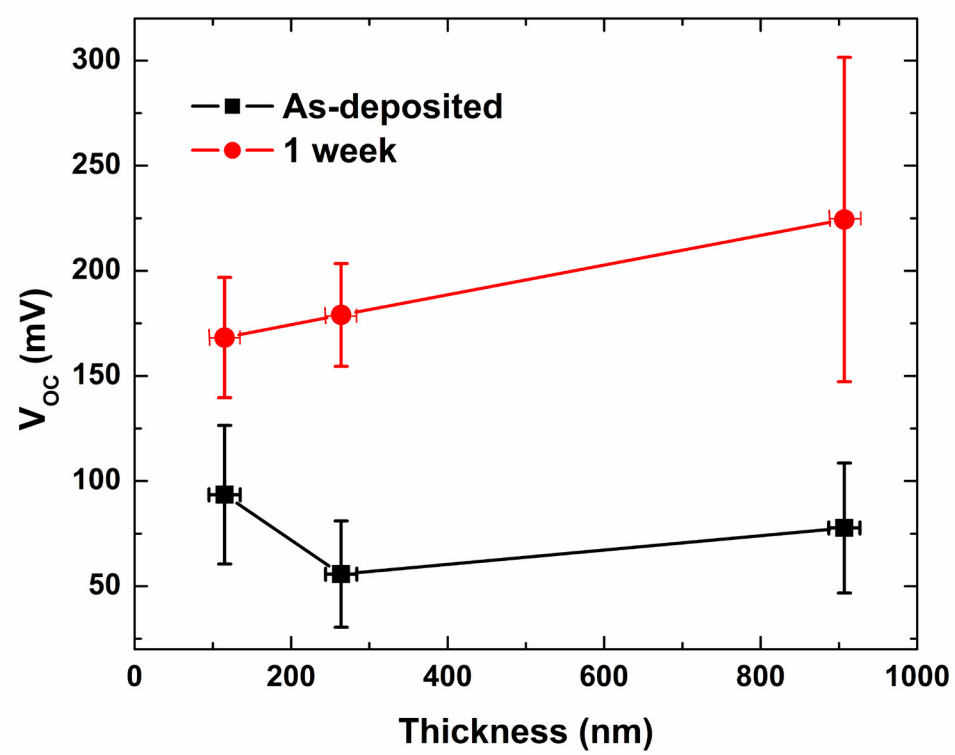

Figure 6.12 Measured open-circuit voltages as-deposited and after one week for films grown at R=45 and various thicknesses.

Thickness (nm)	Measured V_{oc} (mV)	Texture Angle	Texture Depth (nm)	R_{sh} (Ω)	Film lifetime (μs)	S_F and S_B (cm/s)	Substrate lifetime (μs)	Calculated η (%)
115	168	5	5	4.35	<0.1	$1x10^4$	50	1.63
264	180	5	5	4.65	<0.1	$1x10^4$	50	1.74
907	224	15	35	5.78	<0.1	$1x10^4$	50	2.17

Table 6.1 Measured thickness and V_{oc} and fitting parameters from PC-1D for $1x10^{14}$ *n*-type HWCVD grown epitaxial emitter on a $1x10^{16}$ *p*-type substrate for samples measured in Fig. 6.13.

6.4.4 Post-deposition treatments

The open-circuit voltages of junctions deposited under all conditions increased over time (Figs. 6.10-6.12). This is due to the decrease in the surface recombination velocity with the

growth of a native oxide layer. Modeling of these devices with PC-1D reveals that the lower operational voltages are dominated by the surface recombination and a shunt resistance, possibly due to the vacuum break at the device junction. The observed porous microstructure (Fig. 6.5) and electrical property evolution with time illuminates the need for post-deposition treatments which could decrease the surface recombination velocities even better than a native oxide[169] and passivated defects that contribute to the parallel shunt path.

6.4.4.1 Heat treatments and bulk passivation

Heat treatments for the activation of dopants[170] and the reduction of point defects[171] is necessary in most low-temperature epitaxial growth processes.[31,172] However, these treatments cause an evolution of hydrogen from passivated defects and decrease the open-circuit voltage (Figs. 6.13, 6.14).[172,173] Because of the low-strain points of the low-cost substrates, the time and temperature at which the samples can be exposed are limited. This has motivated research into the rapid thermal anneals (RTA) of films on low-strain point substrates.[172,174] Results of V_{oc}=425 mV have been achieved for a 10s treatment at 1000°C with a natural cool-down to 575°C in a nitrogen atmosphere.[172] This heat treatment was followed by a remote hydrogen plasma passivation at 625°C for 15 min and then a slow ramp down with the plasma on to 325°C.[172] Heat treatments above 350°C introduce the need for subsequent hydrogen passivation to increase the open-circuit voltage.[31,44] Typical hydrogen treatments are done by remote plasma CVD in order to decrease the amount of ionic damage.

6.4.4.2 Hydrogen passivation

Hydrogen treatments alone typically improve the open-circuit voltage to a value over half that of a sample that has been both heat treated and hydrogen passivated.[172] The results of the atomic hydrogen treatment, shown in Figures 6.13 and 6.14 were performed in a HWCVD system. The time of 5 minutes, the substrate temperature of 200°C, and the hydrogen pressure of 26 mTorr during hydrogenation were all too low to improve the open-circuit voltage of most of these films. Remarkably however, the short hydrogenation was reasonably effective on the films

grown under conditions of R=45, most likely due to the nature of the pores and the surface of these films which would allow a fast path for H to diffuse into the film and to passivate defects (Figs. 6.9, 6.13, and 6.14). These varying results exemplify the need to tailor post-treatments for each deposition condition and/or regime.

6.4.4.3 Surface passivation

An RCA oxidation, in a solution with a 5:1:1 ratio of water to hydrogen peroxide to ammonium hydroxide for a duration of 15 minutes, was done at 80°C and passivated the surfaces without evolving hydrogen from the films due to the low temperature. Because this clean generates only 3-6Å oxide,[175] the resulting open-circuit voltages for the RCA oxidation were comparable to results with a 1-2 nm native oxide that grew over the course of a week.

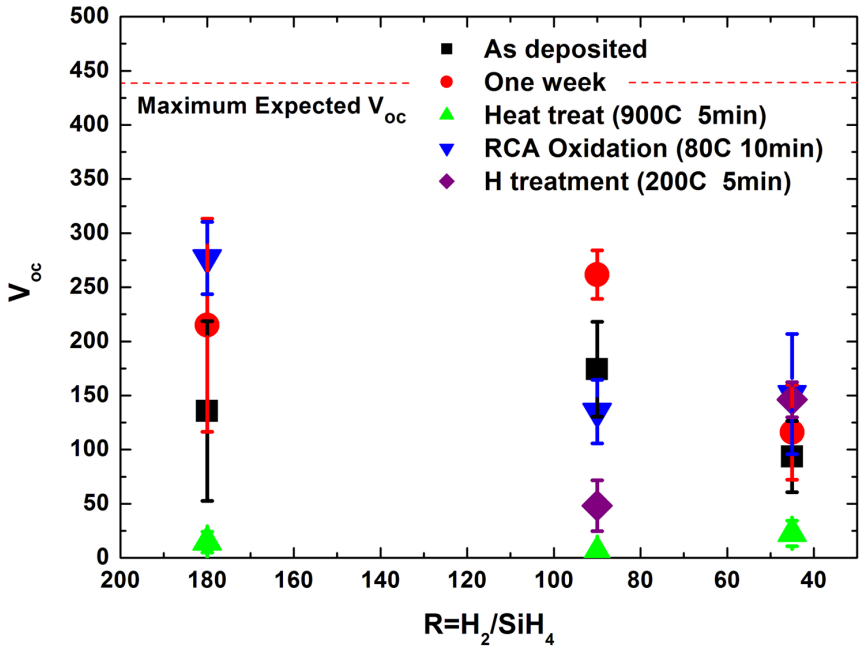

Figure 6.13 Effect of post-deposition treatments for 125 nm thick *n*-type films grown on a *p*-type substrate at different hydrogen dilutions.

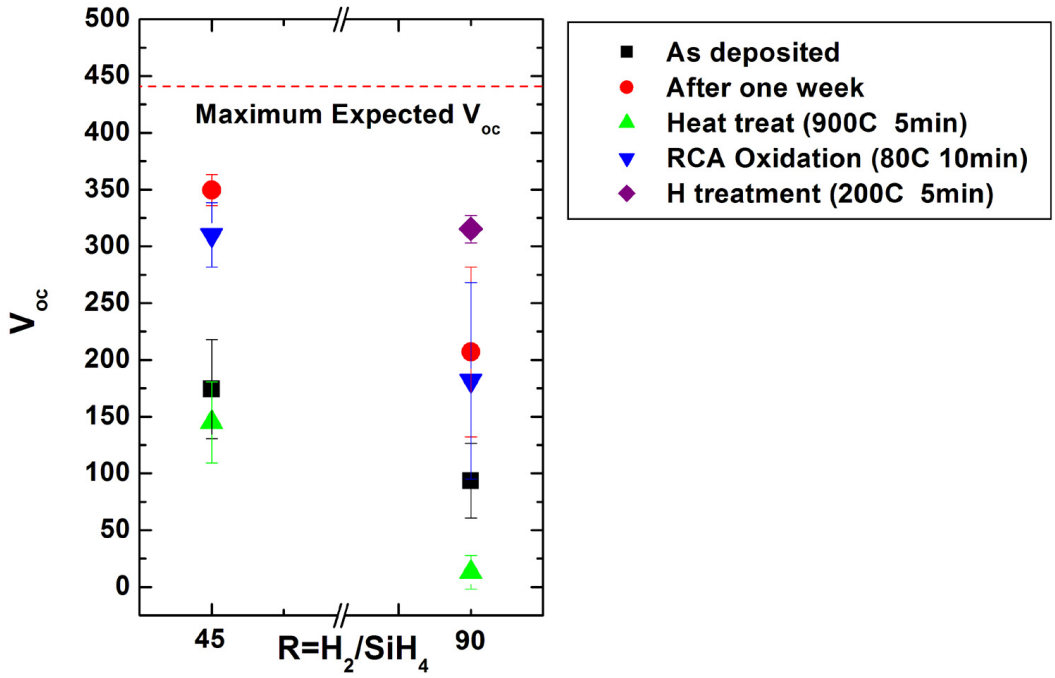

Figure 6.14 Effect of post-deposition treatments described in the text for 885 nm thick *n*-type films grown on a *p*-type substrate at different hydrogen dilutions.

6.4.5 Contact formation

6.4.5.1 Al contacts

Although aluminum makes a near-ohmic contact with silicon as-deposited, heat treatments are necessary in order to improve the contact quality. This is because the contact resistance decreases with an increase in the doping concentration and metals, such as Al, are *p*-type dopants in silicon and heating can lead to a diffusion doping of the Si.[176,177] Unfortunately, the possibility of having a non-continuous metallic film with a heat treatment exists, so contact formation must occur within a certain thermal budget.[176]

Figures 6.15 and 6.16 illustrate the importance of understanding the origin of the series resistance which have a much higher effect on the current-voltage properties of a device than the shunt resistance.[178] The efficiencies of these devices as-deposited, after a 450°C 15 min anneal after Al deposition, and after a 450°C 30 min anneal after Al deposition, are 0.047%, 0.045% and 0.0058%, respectively under AM1.5 illumination with Al and Ag contacts. All of the samples

were ~1 cm^2, so the current is also the current density. Incidentally, the V_{oc} as measured by the Suns-V_{oc} system was the same as that measured with the more traditional current-voltage apparatus. The decrease in efficiency with an increase in annealing time is probably due to the migration of Al and/or Ag into the film causing the contact to be discontinuous (Fig. 6.17).

The short-circuit current, I_{sc}, versus solar irradiation intensity for a 5.5 μm *n*-type HWCVD film on a *p*-type substrate grown at ~250°C, R=60, total pressure of 75 mTorr, and with two tungsten filaments. The non-ideal curvature in the I_{SC}-Suns curve is due to the high series resistance (Fig. 6.16). In this case, the detrimental effect on the device properties is due to the discontinuity of an evaporated Al film after a 30 min anneal at 450°C (Fig. 6.17) and possibly the evolution of hydrogen out of the film. Another possible source of the resistive nature of the device could be the film itself and is discussed in Section 6.4.3.

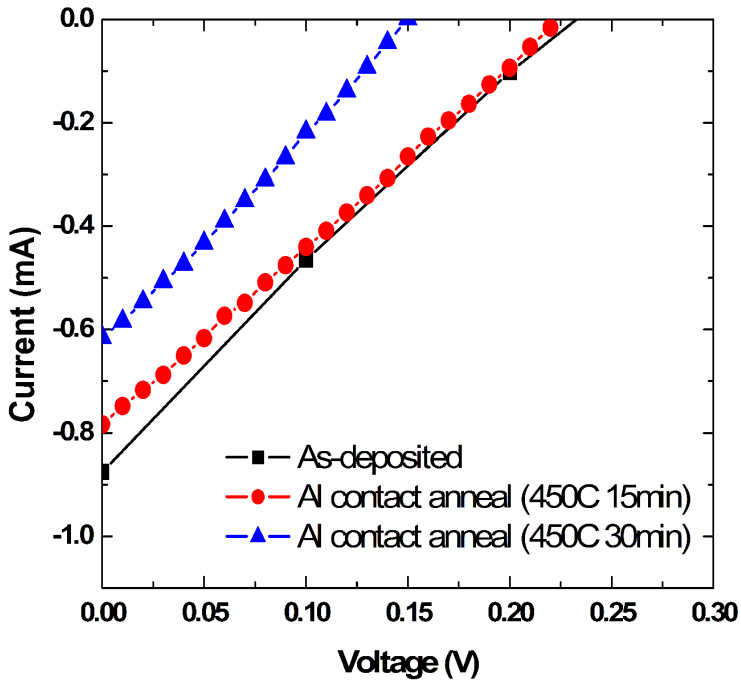

Figure 6.15 Efficiency measurements of a 5.5 μm thick *n*-type HWCVD film on a *p*-type substrate grown at ~250°C and R=60 subjected to various heat treatments. The efficiencies of these devices as-deposited, after a 450°C 15 min anneal after Al deposition, and after a 450°C 30 min anneal after Al deposition, are 0.047%, 0.045% and 0.0058%, respectively under AM1.5 illumination with Al and Ag contacts.

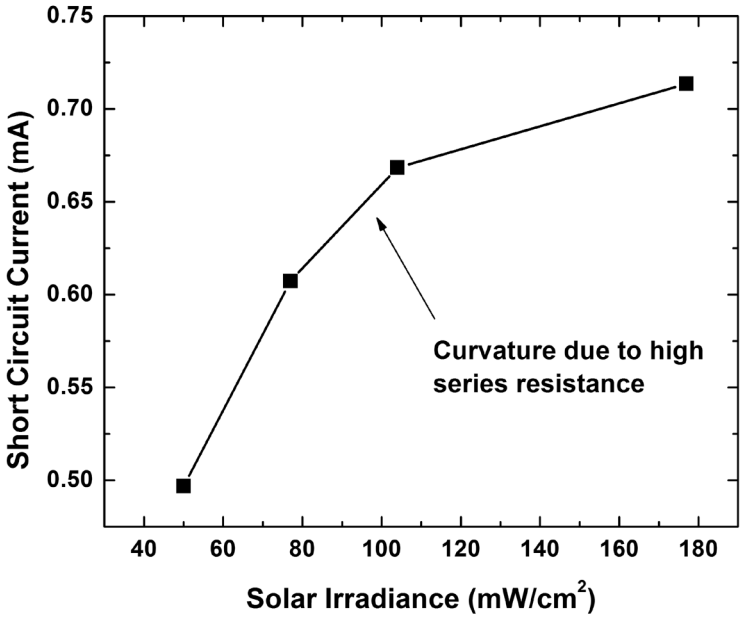

Figure 6.16 Short-circuit current versus solar irradiance for a 5.5 μm thick *n*-type HWCVD film on a *p*-type substrate grown at ~250°C and R=60.

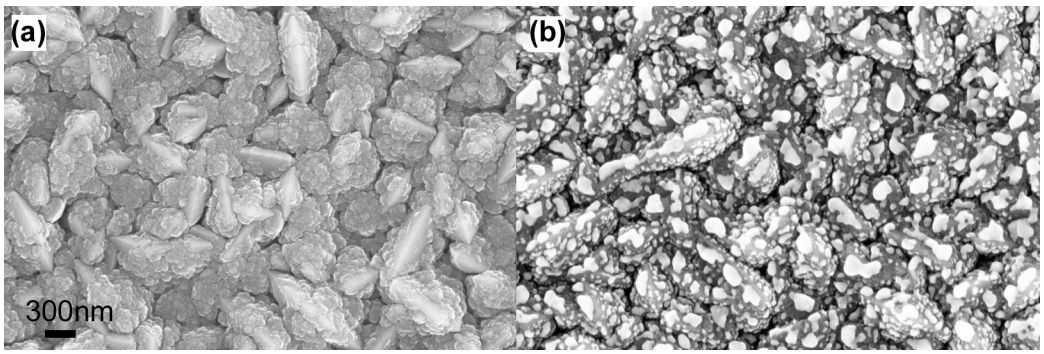

Figure 6.17 SEM images of a film after heat treatment in an area (a) without Ag metallization (b) with Ag metallization. The Ag film appears to be non-continuous.

6.4.5.2 Ag contacts

In the photovoltaic industry, it is common to use a screen printed silver paste for ohmic contacts to the *n*-type region in a crystalline Si cells. These can be phosphorous-doped for improved current collection[161] and are typically fired at temperatures around 700°C.[179] In the devices discussed above, the silver was evaporated onto the *n*-type region after the Al contact anneal in order to ensure that Ag would not migrate along pores in the HWCVD grown film and short the device.

6.5 HWCVD Grown *p/n* Junctions

Films on *n*+ substrates were grown in order to better evaluate the properties of the *n*-type epitaxial layer. Unfortunately these were, in effect, high-low *n*+/*n* junctions rather than the *n*+-type CZ Si wafer/1 μm *n*-type epitaxial layer/100 nm *p*-type a-Si heterojunction device originally envisioned due to the "history" of the chamber; *i.e.* *n*-type dopants from the chamber walls compensated the *p*-type dopants in the gas precursors. The as-deposited films had open-circuit voltages of 2 mV. By depositing Al and Ag contacts without a heat treatment, but with a post-deposition hydrogen treatment at low temperature for 45 minutes, the open-circuit voltage increased to 41±1mV.

6.6 Conclusions

The optical and electrical properties of low-temperature epitaxial films grown by HWCVD are discussed. The rough surface structure is shown to decrease the surface reflectance most likely due to light trapping. Near field photocurrent contrast microscopy of a 5.5 μm thick epitaxial film shows that the electrical properties of the epitaxial films are inhomogeneous suggesting that improvements in the bulk need to be made, perhaps through post-deposition treatments. The electrical properties of as-deposited and post-deposition treated devices are discussed and the need for a good surface passivation is illuminated. The highest stabilized open-circuit voltage of 350 mV out of an expected maximum efficiency of 439 mV for an 885 nm thick *n*-type film on a *p*-type substrate is achieved. The highest efficiency measured was 0.06% for a 300 nm $1x10^{15}$ *n*-type HWCVD grown epitaxial film on a $1x10^{16}$ *p*-type CZ-grown wafer. With optimized post-deposition treatments and surface passivation, we are optimistic that these films can be competitive with traditional silicon photovoltaics.

6.7 References

1. C. E. Richardson, Y.-B. Park, and H. A. Atwater, Proceedings of the 4th IEEE WCPEC, Waikoloa, HI, 2006.

2. C.E. Richardson, Y.-B. Park, and H. A. Atwater, Phys. Rev. B **73** (24) (2006).

3. Veeco Probes, (2006).

4. H. Seel and R. Brendel, Thin Solid Films **451-52**, 608 (2004).

5. D. Thorp and S. R. Wenham, Sol. Ener. Mat. and Sol. Cells **48**, 295 (1997).

6. M. A. Green, Progress in photovoltaics **10** (4), 235 (2002).

7. R. Brendel, *Thin-Film Crystalline Silicon Solar Cells: Physics and Technology*. (Wiley-VCH, 2003).

8. M. C. Wagener, J. K. L. Peters, Y. Park, and G. A. Rozgonyi, Proceedings of the NREL Contract Review Meeting, Denver, CO, 2005.

9. M. Wagener (*personal communication*).

10. R. A. Sinton and A. Cuevas, Proceedings of the 16th European Photovoltaic Solar Energy Conference, 2000.

11. S. Rein and S. W. Glunz, Applied Physics Letters **82** (7), 1054 (2003).

12. E. Yablonovitch, D. L. Allara, C. C. Chang, T. Gmitter, and T. B. Bright, Physical Review Letters **57** (2), 249 (1986).

13. N. Kasai and N. Endo, Journal of the Electrochemical Society **139** (7), 1983 (1992).

14. P. Asoka-Kumar, H.-J. Gossmann, F. C. Unterwald, L. C. Feldman, T. C. Leung, H. L. Au, V. Talyanski, B. Nielson, and K. G. Lynn, Phys. Rev. B **48** (8), 5345 (1993).

15. M. L. Terry, D. Inns, and A. G. Aberle, Proceedings of the 4th IEEE WCPEC, Waikoloa, HI, 2006.

16. A. G. Aberle, Proceedings of the 4th IEEE WCPEC, Waikoloa, HI, 2006.

17. C. H. Seager, D. J. Sharp, J. K. G. Panitz, and R. V. D'Aiello, J. Vac. Sci. Technol. **20** (3), 430 (1982).

18. M. L. Terry, A. Straub, D. Inns, D. Y. Song, and A. G. Aberle, Applied Physics Letters **86** (17), 172108 (2005).

19. B. Rau, J. Schneider, E. Conrad, and S. Gall, Proceedings of the Mat. Res. Soc. Sym., San Francisco, 2006.

20. D. Rouchon, N. Rochat, F. Gustavo, A. Chabli, O. Renault, and P. Besson, Surface and Interface Analysis **34** (1), 445 (2002).

21. O. Nast Hartley, R. Russell, K. C. Heasman, N. B. Mason, and T. M. Bruton, Proceedings of the 29th IEEE PVSC, New Orleans, 2002.

22. C. Y. Chang, Y. K. Fang, and S. M. Sze, Solid-State Electronics **14** (7), 541 (1971).

23. M. B. Prince, J. Appl. Phys. **26** (5), 534 (1955).

24. L. M. Porter, A. Teicher, and D. L. Meier, Sol. Ener. Mat. and Sol. Cells **73**, 209 (2002).

25. Z. Swiatek, E. Beltowska, W. Maziarz, and F. Krok, Materials Science and Engineering B-Solid State Materials for Advanced Technology **101** (1-3), 291 (2003).

Chapter 7

Large-grained Polycrystalline Photovoltaic Devices

7.1 Large-Grained Polycrystalline Silicon Templates

Large-grained polycrystalline silicon templates are formed by crystallizing an amorphous silicon film in contact with a metallic particle at elevated temperatures. The driving force for crystallization process is a reduction in the Gibbs free energy when the amorphous silicon goes through a phase transition into crystalline silicon. Metals forming silicides (Ni, Pd, Cu) and eutectics (Al, Au, Ag, In) with silicon are common. In addition, electrically active dopants in silicon improve the crystallization rate and suppress homogeneous nucleation.[180,181]

7.1.1 Nickel nanoparticle induced crystallization: Caltech

In the Ni/Si system, a silicide is formed when Ni is in contact with the Si at elevated temperatures. The chemical potential for Ni is lower at the $NiSi_2$/a-Si interface than at the $NiSi_2$/c-Si, therefore Ni diffuses to the a-Si side at temperatures as low as ~480°C.[182,183] This allows the silicide to move through the a-Si silicon laterally, crystallizing the silicon as it diffuses in the <111> direction.[184] The density of the nickel on the a-Si film is the main determinant of the resulting crystalline silicon structure (Fig. 7.1).[185] Needle-like growth is the dominant morphology under most conditions (Fig. 7.2),[181] however under with the application of an electric field,[186] by a nitride filter,[182] or another type of Ni reduction,[187] disk-like growth can occur.

Nickel-induced crystallization (NIC) in this work is achieved by the spin-on coating of Ni particles in solution on an amorphous silicon film.[180] Removal of the native oxide is not necessary

in order to nucleate the crystallization process. The effect of the oxide layer on grain size and orientation was not studied.

Nickel is an attractive metal to use because there is only a 0.4% difference in the lattice parameter of c-Si and $NiSi_2$ at room temperature.[184] Moreover, the nickel appears to be stable in the large-grained polycrystalline template after low-temperature epitaxial thickening of the template.[79] The $NiSi_2$ and the a-Si/c-Si phases also remain immiscible during the process, the solid solubility at the crystallization temperature of 600°C is only $3x10^{-14}$ cm^{-3}, and Ni does not contribute to the contamination of the template (Fig. 7.3).[188,189] In addition because Ni is not a dopant in Si, *n*-type or *p*-type templates can be fabricated by the NIC method.[181]

The templates are found to have a (110) preferred orientation.[180] And although the grain sizes can be relatively large, on the order of 10 μm, there is a high density of intra-granular defects.[79,180]

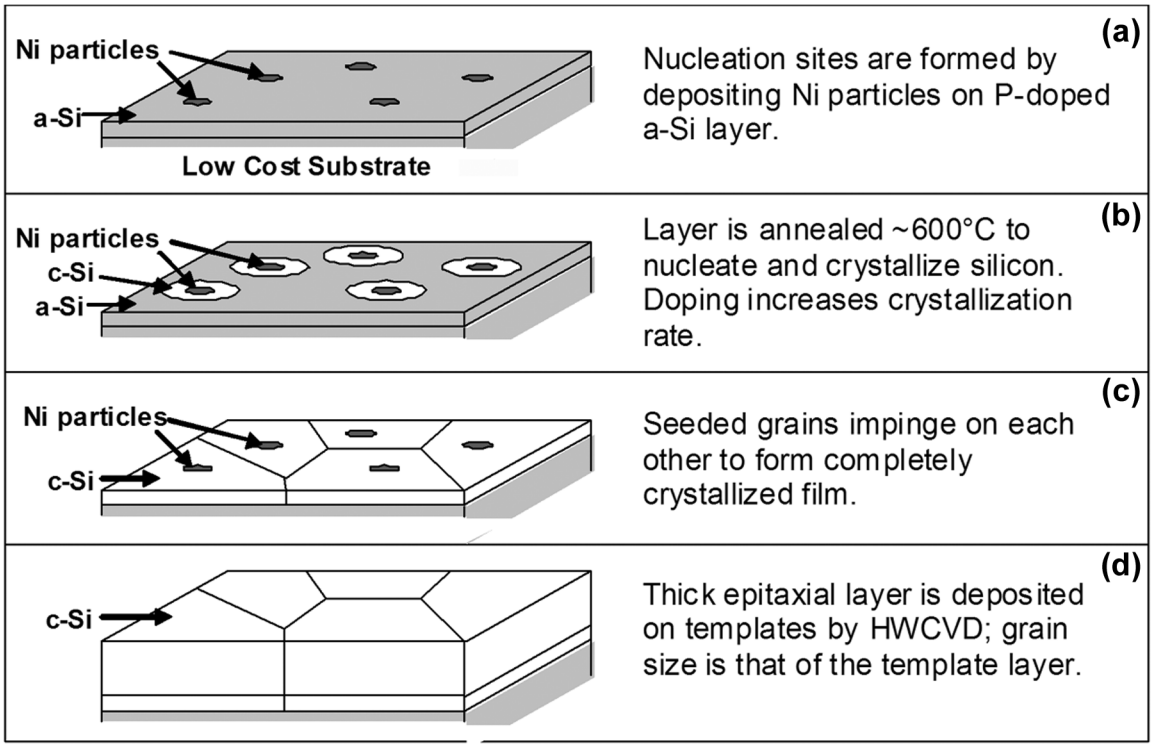

Figure 7.1 Metal induced crystallization of a-Si by Ni nanoparticles adapted from Chen.[180] (a) Randomly distributed Ni nanoparticles on an a-Si film. (b) Crystallization by Ni at 600°C. (c) Grain growth ends when the individual grains coalesce. (d) Excess Ni is then removed and the template is epitaxially thickened.

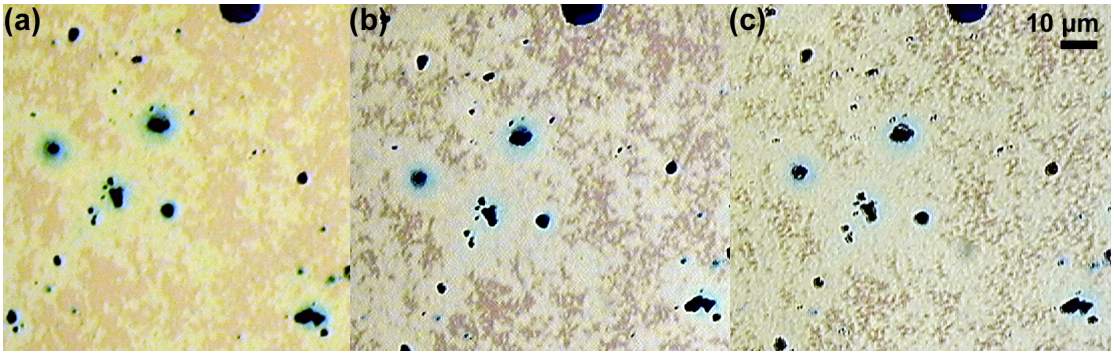

Figure 7.2 Crystallization of 100 nm thick amorphous film on 100 nm SiO_2 on Si after an anneal at 600°C for (a) 9 hrs. (b) 11 hrs. and (c) 13 hrs. The pink regions are amorphous; the green and yellow regions are crystalline; and the dark regions are nickel. Needle-like growth between nucleation sites can be seen.

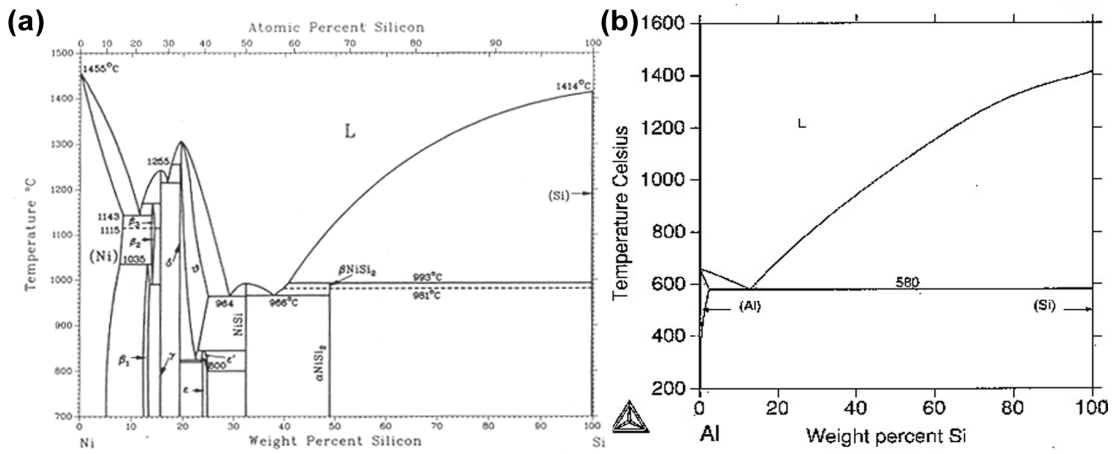

Figure 7.3 Binary phase diagrams of (a) Ni-Si (b) Al-Si. The Ni-Si diagram has a large number of line compounds so the system is often in equilibrium between two phases. Al is up to 1% soluble in silicon and is incorporated into the Si lattice as a dopant during crystallization.

7.1.2 Silane assisted NIC: Caltech

It was found that by flowing silane over the a-Si/metal device during the crystallization anneal that the crystallization time can decrease up to 5-fold as compared to traditional metal-induced crystallization. It also effectively decreases the annealing temperature, further enabling the use of low-cost glass substrates.

A low flow rate of 2.5 sccms of silane was flowed over NIC samples of 100, 200, and 500 nm thicknesses during an anneal at 485°C and compared to those annealed at the same temperatures in vacuum. The anneal conditions and resulting crystallinity as measured by Raman

spectroscopy are listed in Table 7.1 and the Raman spectra for the 100 and 200 nm samples are shown in Figs. 7.3 and 7.4 calculated from the spectra by the method described in Chapter 3. Anneals with forming gas decreased the crystallization rate due most likely to the additional H in the films.[190]

The greater crystalline fraction in the silane-enhanced NIC (SENIC) process is akin to the vapor-liquid-solid mechanism of nanowire growth, but vapor-solid-solid in this case.[191,192] In the SENIC method, the incoming silane molecules appear to react with the Ni nanoparticle depositing a crystalline film on the surface. The Ni reaction with the incoming silane and the a-Si substrate continues laterally until the film coalesces. This would allow one to form an extremely thin polycrystalline template, which may be beneficial for defect minimization in a solar cell (Fig. 7.5). However, the rms roughness of the NIC films annealed in a silane atmosphere was an order of magnitude rougher than those annealed in vacuum. The additional roughness could have a negative impact on the growth of epitaxial films on the SENIC templates.

a-Si Thickness (nm)	Annealing Atmosphere	485°C Anneal Length (min)	Raman Crystallinity%
100	2.5 sccms SiH_4	215	27.98
200	2.5 sccms SiH_4	315	88.57
500	2.5 sccms SiH_4	315	23.77
100	Vacuum	237	8.2
200	Vacuum	335	0
500	Vacuum	335	14.27

Table 7.1 Annealing conditions and resulting Raman crystallinity for a-Si NIC samples annealed in a silane and a vacuum ambient.

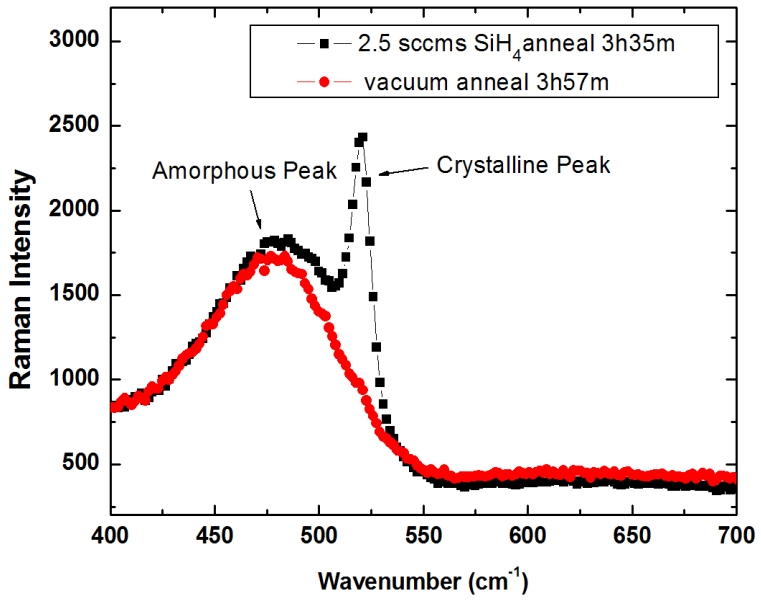

Figure 7.4 Raman spectroscopy of a 100 nm thick a-Si film spun with Ni nanoparticles and annealed. This graph shows the greater crystallinity of the sample annealed in a SiH_4 ambient for 3 hrs and 35 min versus the sample annealed in vacuum for 3 hrs and 57 min.

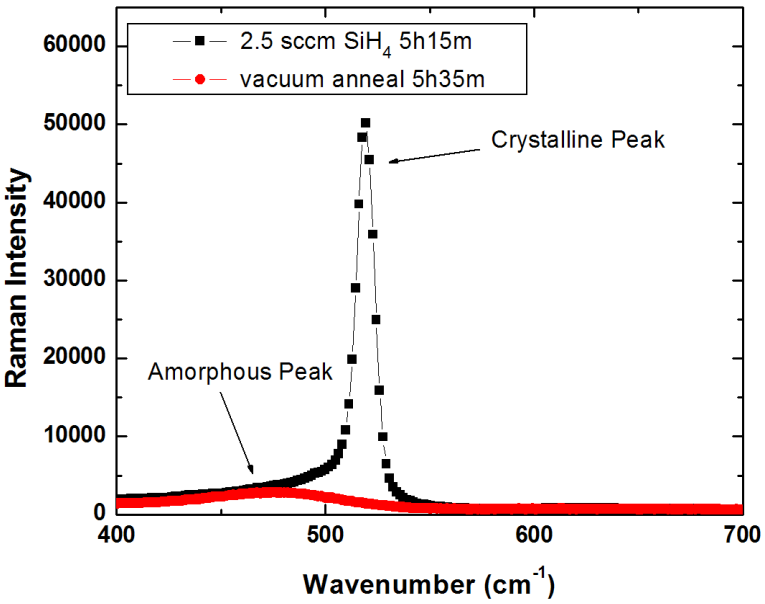

Figure 7.5 Raman spectroscopy of a 200 nm thick a-Si film spun with Ni nanoparticles and annealed. This graph shows the full crystallinity of the sample annealed in a SiH_4 ambient for 5 hrs and 15 min versus the vacuum anneal for 5 hrs and 35 minutes.

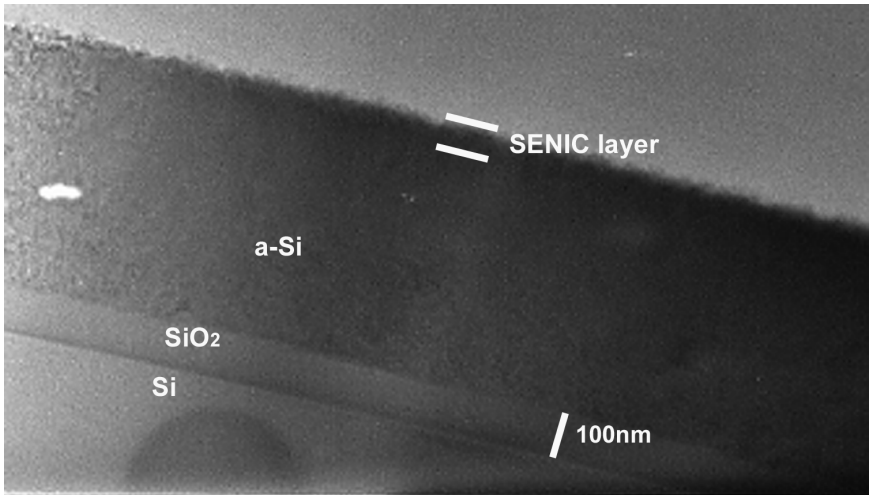

Figure 7.6 Cross-sectional TEM image of thin crystalline layer on an a-Si film grown by the SENIC process.

7.1.3 Aluminum induced crystallization: Hahn-Meitner-Institut

Aluminum induced crystallization (AIC) for photovoltaic devices have been studied extensively at the University of New South Wales[193-199] and the Hahn-Meitner-Institut (HMI).[197,198,200-205] With an anneal below the eutectic temperature (Fig. 7.2), layer exchange between the Al film and the a-Si film will occur leaving a c-Si film with an Al/Si film on top (Fig. 7.6).[199] The mostly Al film on top is then removed with a chemical etch or mechanical polish.[206]

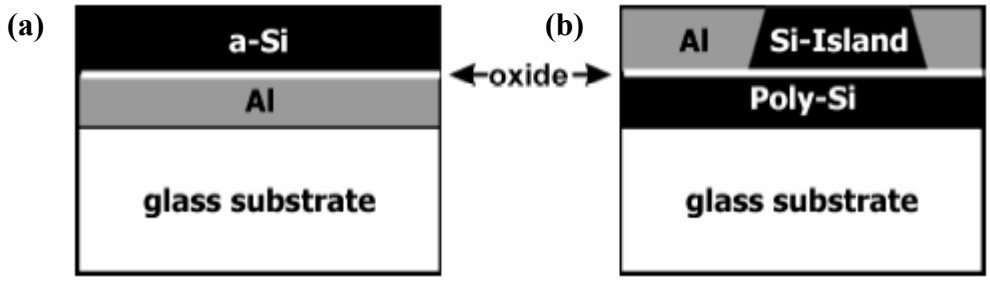

Figure 7.7 Schematic of the AIC process from Shneider[206] (a) before and (b) after crystallization.

7.1.4 Aluminum nanoparticle induced crystallization: Caltech

Samples were fabricated with aluminum nanoparticles instead of nickel nanoparticles in the hopes of reducing the annealing temperature of the templates. The nucleation of crystallites

was unable to occur at temperatures lower than 500°C, due most likely to the oxidation of the aluminum nanoparticles.

Figure 7.7 is a comparison of 200 nm thick films annealed at 600°C in a vacuum furnace for 3 hours with nickel and aluminum nanoparticles. The green areas are crystallized, the pink area amorphous. The nickel induced films preferentially crystallized laterally from the nickel particle, where as the aluminum induced films seemed to spread locally and nucleate homogeneously. The aluminum could be crystallizing through the depth of the 200 nm thick film as in the layer transfer process. Also, the Al spreading as compared to the Ni particle is due to the lower melting point and higher vapor pressure of Al. The Ni nanoparticles have much more consistent and favorable results, so the Al nanoparticle crystallization was abandoned.

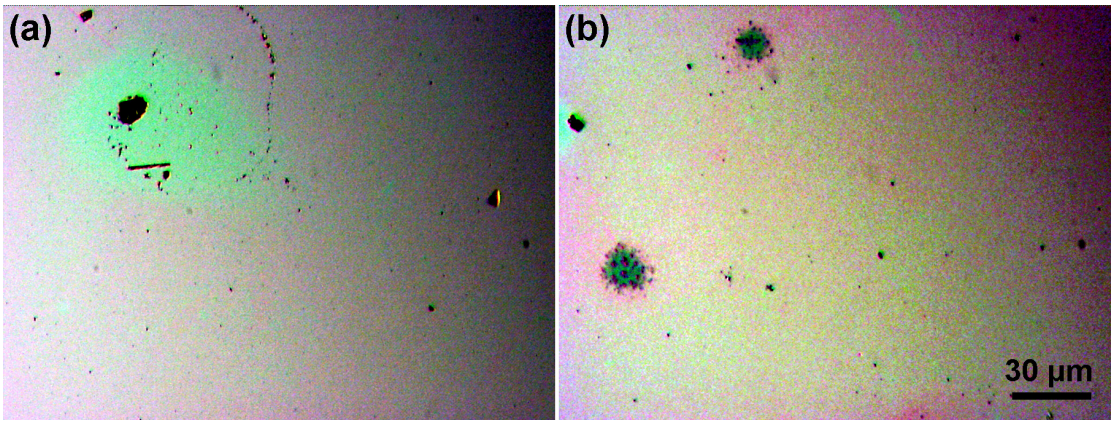

Figure 7.8 Comparison of nanoparticle induced crystallization of 200 nm thick a-Si films with (a) Nickel and (b) Aluminum after 3 hours at 600°C.

7.2 Epitaxial Films on Templates

Several growths were completed on both Caltech NIC and HMI AIC templates and Si (100) substrates for comparison (Table 7.2 and Fig. 7.8). The highest open-circuit voltage for an as-deposited film was for a 5.5 µm thick *n*-type epitaxial film grown on a *p*+-type HMI AIC template as measured with the Suns-V_{oc} system.[167] The devices on HMI templates were illuminated from the film side; as a rear junction device. The film on the NIC template as-deposited is a hi-low junction and does not have a true emitter layer. The highest open-circuit

voltage for an as-deposited device made by epitaxially thickening a large-grained polycrystalline template is 284 mV by Rau *et al.* at HMI for films grown at 600°C.[207] With un-optimized anneal and hydrogen passivation steps, the open-circuit voltage was increased to 378 mV.[207]

As seen in Fig. 7.9, the 5.5 µm thick film with the greater epitaxial thickness on Si (100) had a higher V_{oc} on the HMI templates, which are predominately (100) oriented.[208] The high-angled surface texture of this film is also advantageous for light trapping (Fig. 7.10).

The 3 µm thick films on the NIC (46 mV) and AIC (32 mV) templates allow for a direct comparison of the two templates. The NIC device appears to perform better, however this could be due to the *n+/p/p+* device structure with a back surface field as opposed to the *p+/n* device structure of the AIC device.

After the Al contact anneal at 450°C for 30 minutes the V_{oc} of all of the devices dropped due to the evolution of hydrogen from the films. This anneal is done not only to make contact to the p+-layers in the HMI stack, but to dope the *n*-type epitaxial layer for the film grown on the Ni template. Figure 7.11 shows the depth in which the Al contact diffused into the *n*-type epitaxial layer. It does not appear that a short is made through the thin-film device.

The largest open-circuit voltage measured on a NIC device was 249 mV for a 4 µm thick film grown at 200°C and R=380 with two graphite filaments. However, this film was incredibly non-uniform and open-circuit voltages as low as 3 mV were also measured on the same device without metallization.

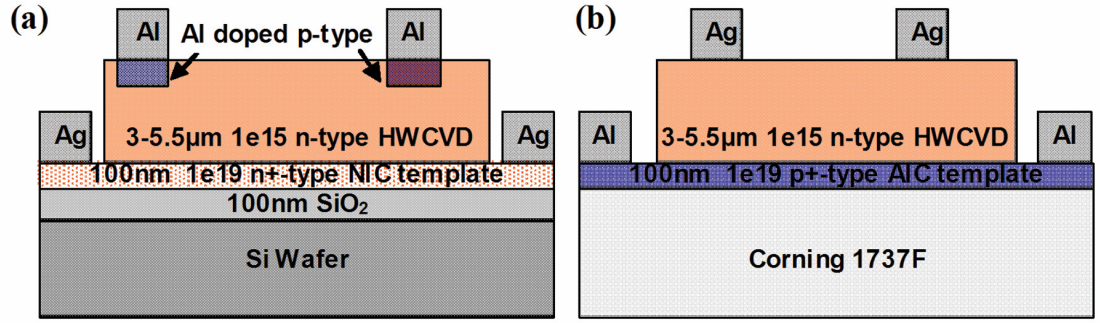

Figure 7.9 Schematic of devices fabricated on (a) NIC templates and (b) AIC templates.

Thickness (μm)	Template Type	Substrate Temp (°C)	R= H_2/ SiH_4	Pressure (mTorr)	Dep rate (nm/min)	RHEED on Si (100)	V_{oc} [a] (mV)	V_{oc} [b] (mV)
3	NIC Caltech	330	115	120	2.2	Poly	46	9
3	AIC HMI	330	115	120	2.2	Poly	32	3
5.5	AIC HMI	300	60	75	4.5	Epi	90	2

Table 7.2 Deposition parameters and open-circuit voltages for epitaxial films on large-grained polycrystalline templates. [a] as-deposited, [b] after metallization and H desorption anneal.

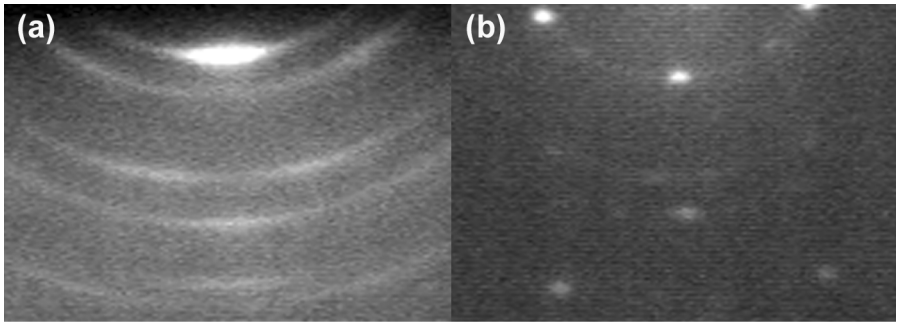

Figure 7.10 RHEED patterns for depositions on Si (100) substrates for (a) a 3 μm thick polycrystalline film and (b) a 5.5 μm thick polycrystalline/twinned epitaxial mixed film.

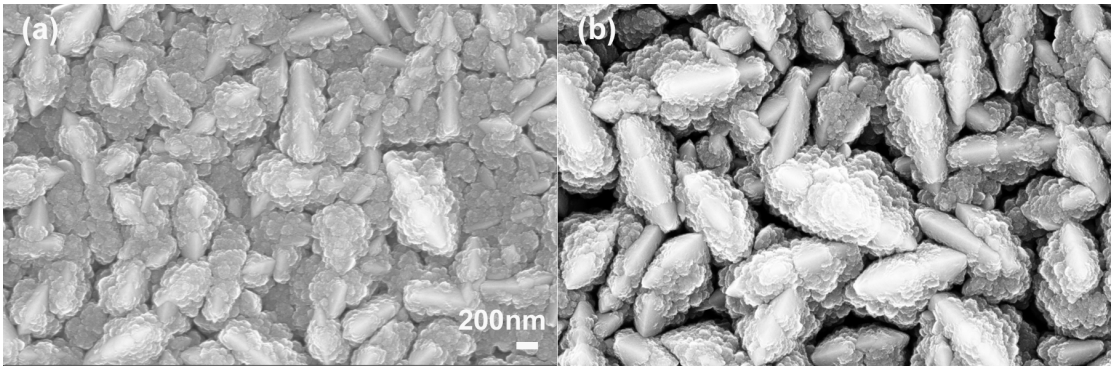

Figure 7.11 SEM images for depositions on Si (100) substrates (a) 3 μm thick polycrystalline film and (b) 5.5 μm thick polycrystalline/epitaxial mixed film. Note the higher angle facets for light trapping in the thicker film.

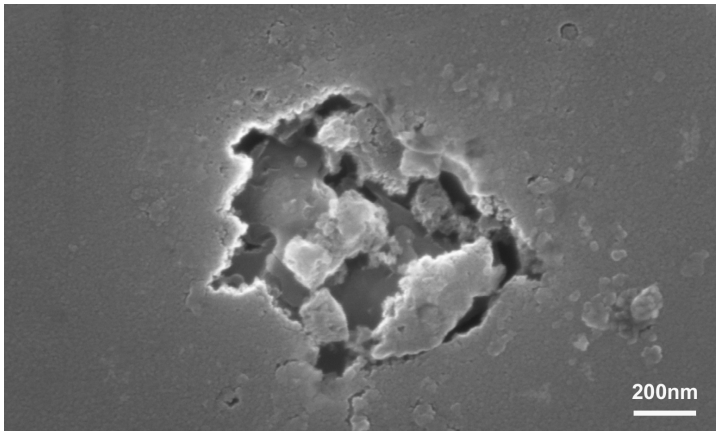

Figure 7.12 SEM image taken after a metal etch on the contact region of a 3 μm thick polycrystalline film grown on NIC template after Al metallization and heat treatment showing the extent of the Al diffusion into the film.

7.3 Integration of Glass Substrates with Semiconductor Processing

Previous work in the area of NIC with nanoparticles had been on oxidized silicon wafers because of their smoothness and for ease in TEM preparation.[78,79,180] Therefore, it was not clear whether or not variations to the process would need to be made when using glass substrates in order to achieve the same grains sizes, due to the possibility of a rough surface acting as a nucleation site. The roughness of the glass substrates used in this study had an rms roughness of 30 Å, and order of magnitude more than an oxidized Si substrate. Figure 7.12 shows the NIC of a films on glass and oxide coated silicon. The grain sizes are greater in the crystallized films on glass. This is probably due to the initial oxide layer between the Ni and the a-Si, which effectively reduced the amount of Ni available for crystallization just as the oxide layer in the AIC process.[209] The optical microscope image in Fig. 7.12 also shows small pinholes. Crystallization on an indium tin oxide (ITO)-coated glass substrate was also successful (Fig. 7.13), although the ITO itself was incompatible with the HF template oxide removal.

Samples on glass are incompatible with an HF dip to remove the native oxide layer. The adhesion of the a-Si to the glass is not strong enough and causes the films to peel or bubble. However, removal of the native oxide layer on the crystallized template must occur in order to

have epitaxial growth. This can be done either by placing the sample on a spinner, pippetting HF onto the a-Si surface for 30 seconds and then spin-drying the sample, or by drying with a N_2 gun. The ITO-coated glass was incompatible with this step, with the ITO immediately peeling the entire template off the glass even with extremely dilute HF solutions.

Ideally, the glass would be coated with a SiN anti-reflective coating prior to deposition of the amorphous silicon film and the NIC. The SiN layer would not only aid in light trapping in a superstrate configuration,[31] but would also prevent the diffusion of ions from the low-cost glass during the crystallization anneal and improve adhesion.[210,211] Although contaminants from the glass or the ITO, did not appear to inhibit crystallization, hydrogen is known to decrease the crystallization speed and increase the disorder of the crystallized film, and it can be inferred that larger point defects would have an even greater effect.[190] Point defects in crystallized samples are notoriously difficult to remove and/or accommodate even after long high-temperature anneals.[171,172]

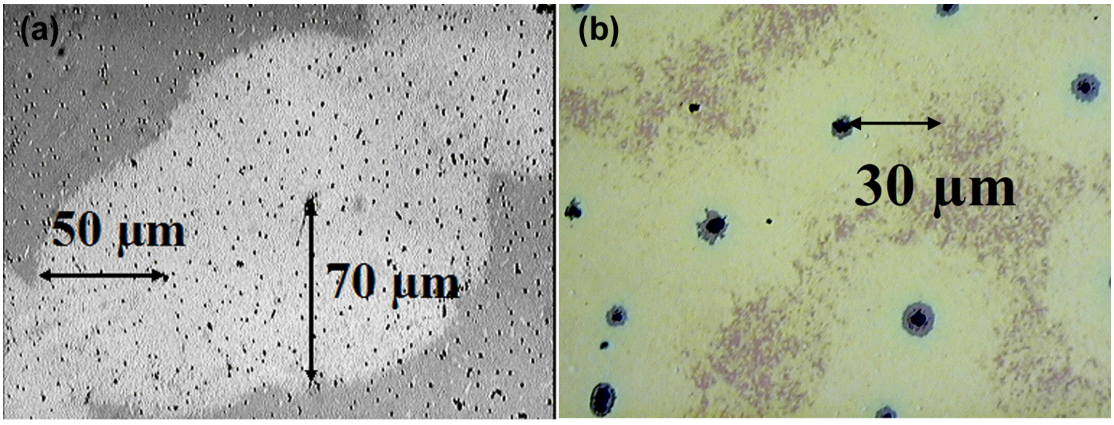

Figure 7.13 NIC films on (a) glass after 17 hrs at 600°C with small pinholes. (b) SiO_2/Si after 10 hrs at 600°C.

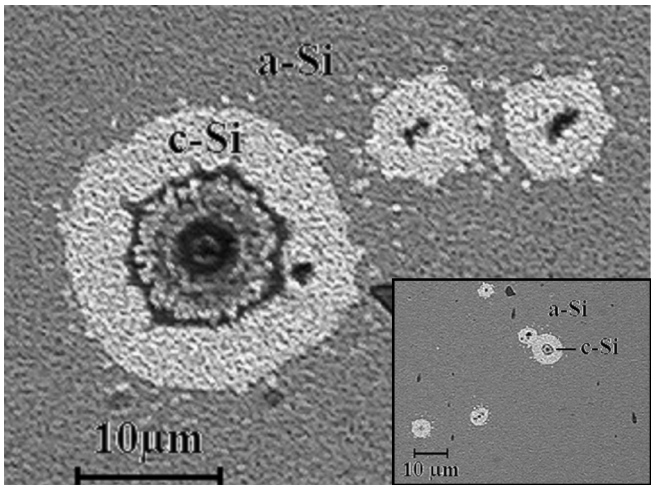

Figure 7.14 NIC of a-Si on an ITO coated glass substrate from BP Solar. Contaminants from the ITO do not appear to inhibit crystallization.

The next modification would be a very thin highly doped polycrystalline template, perhaps with the SENIC process, so that the conductivity through this layer is high enough to allow for collecting carriers without a conductive transparent oxide. The doping concentration needs to be higher in a polycrystalline film than in a monocrystalline film due to the larger number of grain boundaries, which decrease the conductivity of the layer. The epitaxial thickening of the template would then occur via HWCVD, most likely at a temperature closer to 600°C since any post-deposition treatments remove the intrinsic hydrogen from the films and since higher temperature allows for a denser growth.[212] An amorphous emitter would then be deposited in a separate chamber via HWCVD or a crystalline emitter could be made by the diffusion of Al into the epitaxial Si from the metallization through an annealing step. A conformal Al deposition would also serve as a back reflector to enhance light-trapping in the device (Fig. 7.14).

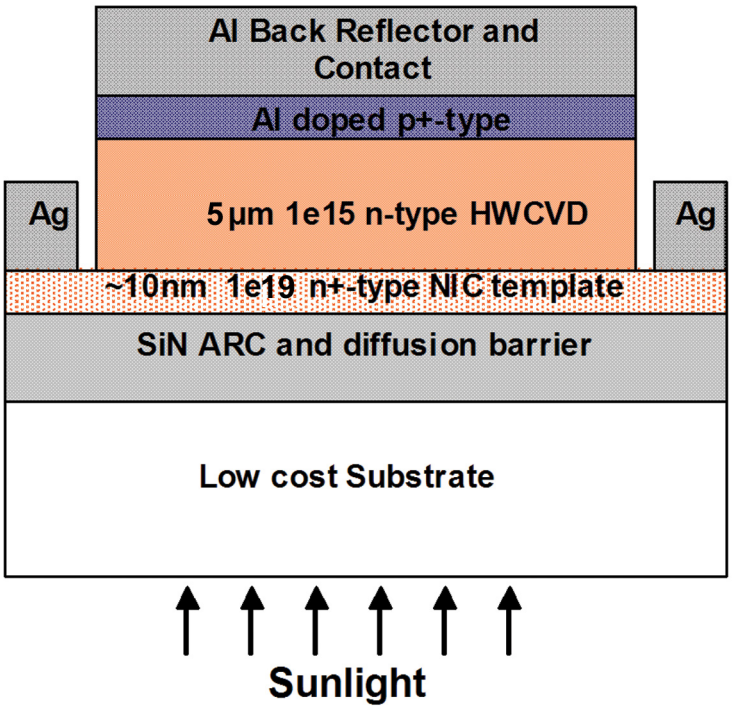

Figure 7.15 Proposed thin-film polycrystalline silicon photovoltaic device structure for future work.

7.4 Conclusions

HWCVD epitaxial thickening of large-grained polycrystalline templates is a novel and interesting processing scheme with the potential for achieving low-cost 15% efficient solar cells. Epitaxial films were grown on NIC templates and AIC templates from the Hahn-Meitner-Institute. The highest open-circuit voltage measured for an as-deposited film with epitaxial thickening was 90 mV for a 5.5 μm epitaxial film on an AIC HMI template. However, more studies need to be done in order to compare the advantages and disadvantages of NIC and AIC templates. Post-deposition treatments are necessary for the improvement of these devices. Possible modifications in the processing sequence to improve the device properties of these films in the future include starting with SiN coated glass, thin, highly-doped templates, and a back reflector for the superstrate configuration.

7.5 References

1. C. M. Chen, "*Polycrystalline Silicon Thin Films for Photovoltaics,*" California Institute of Technology, 2001.

2. J. S. Ahn, Y. G. Yoon, and S. K. Joo, Journal Of Crystal Growth **290** (2), 379 (2006).

3. W. S. Sohn, J. H. Choi, K. H. Kim, J. H. Oh, and S. S. Kim, J. Appl. Phys. **94** (7), 4326 (2003).

4. C. Hayzelden and J. L. Batstone, J. Appl. Phys. **73** (12), 8279 (1993).

5. C. Hayzelden, J. L. Batstone, and R. C. Cammarata, Appl. Phys. Lett. **60** (2), 225 (1992).

6. J. H. Choi, S. S. Kim, J. H. Oh, J. H. Cheon, and J. Jing, J. Appl. Phys. **96** (6), 3574 (2004).

7. H. Kanno, A. Kenjo, T. Sadoh, and M. Miyao, Thin Solid Films **508** (1-2), 40 (2006).

8. K. Makihira, H. Nozaki, T. Asano, and M. Miyasaka, Solid State Phenomena **93**, 207 (2003).

9. C. E. Richardson, M. S. Mason, and H. A. Atwater, Amorphous and Nanocrystalline Silicon Science and Technology-2004 (Materials Research Symposium Proceedings Vol.808), 227 (2004).

10. Z. Jin, A. B. Gururaj, M. Yeung, H. S. Kwok, and M. Wong, J. Appl. Phys. **84** (1), 194 (1998).

11. Eicke R. Weber, Applied Physics A: Materials Science & Processing **30** (1), 1 (1983).

12. A. H. Mahan, S. P. Ahrenkiel, B. Roy, R. E. I. Schropp, H. Li, and D. S. Ginley, Proceedings of the 4th IEEE WCPEC, Waikoloa, HI, 2006.

13. R. S. Wagner and W. C. Ellis, Appl. Phys. Lett. **4** (5), 89 (1964).

14. B. M. Kayes, C. E. Richardson, N. S. Lewis, and H. A. Atwater, Proceedings of the 31st IEEE Photovoltaics Specialist Conference, Lake Buena Vista, FL, 2005.

15. A. G. Aberle, Journal Of Crystal Growth **287** (2), 386 (2006).

16. A. Straub, D. Inns, M. L. Terry, R. Gebs, and A. G. Aberle, Journal Of Applied Physics **98** (2) (2005).

17. A. Straub, D. Inns, M. L. Terry, Y. Huang, P. I. Widenborg, and A. G. Aberle, Journal Of Crystal Growth **280** (3-4), 385 (2005).

18. A. Straub, P. I. Widenborg, A. Sproul, Y. Huang, N. P. Harder, and A. G. Aberle, Journal Of Crystal Growth **265** (1-2), 168 (2004).

19. O. Nast and A. J. Hartmann, Journal Of Applied Physics **88** (2), 716 (2000).

20. O. Nast, S. Brehme, D. H. Neuhaus, and S. R. Wenham, Ieee Transactions On Electron Devices **46** (10), 2062 (1999).

21. O. Nast, T. Puzzer, L. M. Koschier, A. B. Sproul, and S. R. Wenham, Applied Physics Letters **73** (22), 3214 (1998).

22. J. Schneider, A. Sarikov, J. Klein, M. Muske, I. Sieber, T. Quinn, H. S. Reehal, S. Gall, and W. Fuhs, Journal Of Crystal Growth **287** (2), 423 (2006).

23. J. Schneider, R. Heimburger, J. Klein, M. Muske, S. Gall, and W. Fuhs, Thin Solid Films **487** (1-2), 107 (2005).

24. W. Fuhs, S. Gall, B. Rau, M. Schmidt, and J. Schneider, Solar Energy **77** (6), 961 (2004).

25. B. Rau, I. Sieber, J. Schneider, M. Muske, M. Stoger-Pollach, P. Schattschneider, S. Gall, and W. Fuhs, Journal Of Crystal Growth **270** (3-4), 396 (2004).

26. J. Schneider, J. Klein, M. Muske, S. Gall, and W. Fuhs, Journal Of Non-Crystalline Solids **338-40**, 127 (2004).

27. S. Gall, M. Muske, I. Sieber, O. Nast, and W. Fuhs, Journal Of Non-Crystalline Solids **299**, 741 (2002).

28. J. Schneider, "*Nucleation and growth during the formation of polycrystalline silicon thin films,*" Technical University of Berlin and the Hahn-Meitner-Institut, 2005.

29. R. A. Sinton and A. Cuevas, Proceedings of the 16th European Photovoltaic Solar Energy Conference, 2000.

30. B. Rau, J. Schneider, E. Conrad, S. Gall, and W. Fuhs, Proceedings of the 15th International PVSEC, Shanghai, China, 2005.

31. A Straub, NP Harder, YD Huang, and AG Aberle, JOURNAL OF CRYSTAL GROWTH **268** (1-2), 41 (2004).

32. Maribeth S. Mason, "*Synthesis of Large-Grained Polycrystalline Silicon by Hot-Wire Chemical Vapor Deposition for Thin Film Photovoltaic Applications,*" California Institute of Technology, 2004.

33. J. Schneider, J. Klein, A. Sarikov, M. Muske, S. Gall, and W. Fuhs, Proceedings of the Materials Research Society Spring Meeting, San Francisco, CA, 2005.

34. A. G. Aberle, Proceedings of the 4th IEEE WCPEC, Waikoloa, HI, 2006.

35. R. C. Reedy, E. Iwaniczko, Q. Wang, Y Xu, and D. Young, Proceedings of the 15th Workshop on Crystalline Silicon Solar Cells and Modules: Materials and Processes, Vail, CO, 2005.

36. W. H. Teh, A. Trigg, C. H. Tung, R. Kumar, N. Balasubramanian, and D. L. Kwong, Applied Physics Letters **87** (7) (2005).

37. M. L. Terry, D. Inns, and A. G. Aberle, Proceedings of the 4th IEEE WCPEC, Waikoloa, HI, 2006.

38. P. Asoka-Kumar, H.-J. Gossmann, F. C. Unterwald, L. C. Feldman, T. C. Leung, H. L. Au, V. Talyanski, B. Nielson, and K. G. Lynn, Phys. Rev. B **48** (8), 5345 (1993).

39. C.W. Teplin, E. Iwaniczko, Q. Wang, K. M. Jones, R. Reedy, B. To, D. Levi, H. Moutinho, and H. M. Branz, Proceedings of the Materials Research Society, San Francisco, 2006.

Chapter 8

Conclusions and Future Directions

8.1 Low-Temperature HWCVD Epitaxial Films for Photovoltaic Devices

This thesis demonstrates that low-temperature epitaxial silicon growth by hot-wire chemical vapor deposition (HWCVD) is an interesting and flexible material for photovoltaic devices. The epitaxial thickening of large-grained polycrystalline templates are a promising avenue of research for next-generation photovoltaic devices. Such devices, with grain sizes larger than the thickness of the cell, have the potential to achieve multicrystalline-like efficiencies of 15%, but at a much lower-cost by taking advantage of thin-film manufacturing techniques. The surface morphology and structural evolution of low-temperature epitaxial films can be tailored for different device designs. Variations in the physical properties of these HWCVD grown films are achieved through variations in the silane partial pressure, the hydrogen dilution of silane, and the substrate temperature. The partial pressure of silane determines whether epitaxial growth will breakdown into a polycrystalline or an amorphous phase, with silane partial pressures below ~10 mTorr allowing for breakdown into a polycrystalline phase. While a low-growth rate dictates the initial epitaxial phase. The critical epitaxial thickness has previously been shown to increase with a decrease in the substrate temperature down to temperatures of 300°C. This is due to the high hydrogen content during HWCVD, and can be explained by a contamination probability model. The contamination probability model describes the complex relationship between hydrogen dilution, substrate temperature, and pressure. In this thesis, epitaxial growth of 5.5 μm thick films at 300°C and twinned epitaxial silicon growth of 6.8 μm thick films at 230°C have been achieved. Since epitaxial and high-quality crystalline silicon are

deposited at such low deposition temperatures, there is an opportunity to deposit high quality films on low-cost substrates.

The rms roughness of HWCVD low-temperature crystalline films increases with increasing substrate temperature and with increasing dilution ratio for crystalline silicon films on silicon substrates. This trend is also due to the large amount of atomic hydrogen involved in the HWCVD process and allows epitaxial growth to continue even with roughest morphologies. Under conditions of low silane partial pressure, hydrogen dilution is found to be the most important factor in determining the growth regime, and arbitrarily thick crystalline Si films can be grown at low-temperatures under high H dilution. Films grown without additional hydrogen grow in the random deposition with relaxation regime, while increasing hydrogen leads to shadowing, and finally the etching and reemission of growth species.

Because of the larger surface and interface to bulk ratios of thin-film photovoltaics, extra consideration must be taken in designing a device. Sources of loss in a polycrystalline thin-film device are grain boundaries, intra-granular defects, and limited absorption, with the main losses coming from surface and junction recombination. These potentially damaging issues can be mitigated with hydrogen passivation, dielectric anti-reflection coatings, amorphous emitters, and light trapping through texturing and reflective back surfaces.

A stabilized open-circuit voltage of 350 mV out of a maximum, doping limited, expected efficiency of 439 mV is achieved for an *n*-type 885 nm film on a *p*-type substrate. Epitaxial films were also grown on NIC and AIC templates. The highest open-circuit voltage for an as-deposited film with epitaxial thickening was for a 5.5 μm epitaxial film on an AIC HMI template. With optimized post-deposition treatments and surface passivation, these films can be competitive with traditional silicon photovoltaics. Other modifications necessary to the processing sequence in order to improve the device properties of these films include starting with SiN coated glass and a back reflector for the superstrate configuration.

8.2 Future Avenues of Research

8.2.1 HWCVD apparatus

Many elements of HWCVD are not well understood manufacturable. The most problematic, to my mind, is the actual apparatus itself. There are many source of contamination when metallic species are heated above 1000°C, including all the materials in the filament circuit itself and the deposition shutter. Moreover, since the wire chemistry changes during the course of a deposition, the results of a deposition, even under the same deposition condition, can be dramatically different. In-situ treatments for cleaning wires without having to vent the chamber should be investigated to increase the filament lifetime along with ensuring wafer-to-wafer uniformity, in order to make HWCVD a manufacturable technique.

8.2.2 Large-grained NIC templates

The NIC templates have a high density of intra-granular defects due to the dendritic crystallization front.[1,2] In order to minimize the carrier recombination at these low-angle grain boundaries which are grown into the epitaxial active layer of the device, further research must be carried out into growing higher quality templates and/or post-deposition treatments to decrease the defect density. This would include looking at the effect of the temperature, including temperature ramps, the nanoparticle concentration during the spin-on process, the native or grown silicon oxide on the surface before spin-on of the nickel, the nickel removal etch, and the resulting roughness and grain size of the large-grained polycrystalline templates.

Moreover, it may be more desirable from a device, and from a manufacturing standpoint, to have a template with uniform grain sizes, rather than a low-cost template with a random distribution of grain-sizes as are formed with the spin-on technique and should be considered during future investigations. Perhaps a thin-film of nickel is more desirable than nanoparticles for sample to sample uniformity reasons.

8.2.3 Post-deposition treatments and device design modification

Chapters 6 and 7 illuminated the need for post-deposition treatments in order to increase the efficiencies of low-temperature HWCVD epitaxial films. Further studies into the heat treatments (RTA and furnace), hydrogen passivation, and metallization are needed, especially since the low-temperature films discussed in this thesis are almost 400°C less than those being investigated by other groups.[3,4] Their effect on dopant activation, defect reduction, and bulk and surface passivation are not well understood. This could include easy solutions like halting a deposition every ~100 nm to do an H treatment, but *in-situ* and *ex-situ* post-deposition treatments need to be explored. In addition, HWCVD SiN has shown great promise as a H source for bulk passivation.[5] The addition of SiN:H coated glass substrates to the process flow would help greatly with light trapping and passivation and would work as a diffusion barrier for impurities from the glass to get into the active region of the device. In addition, optimization of the actual contact structure and dimensions are needed in order to efficiently collect carriers out of the device.

8.2.4 New deposition regimes of epitaxial growth

Films with high hydrogen dilutions (R=480) were found to be very dense even at temperatures of 350°, however, further studies into thicker films of this morphology would be necessary in order to ascertain their potential for epitaxially thickening large-grained templates. The other route would be to increase the deposition temperature (450-600°C) to allow for higher surface diffusion and denser films at intermediate dilutions. This may be the more attractive method if a post-deposition treatment is found to be necessary.

8.2.5 Porous silicon emitter layers

Porous silicon (PS) has recently been gaining a lot of attention due to the band-gap modification of the effective medium and its light trapping capabilities and their applications towards silicon on insulator technologies in microelectronic and optoelectronic applications.[6-8]

The exciting difference in the work of this thesis versus those of other researchers is the low-temperature deposition of the PS. Typically, PS is a post-deposition treatment to an increasingly expensive silicon wafer,[6] while in this thesis porous epitaxial silicon is deposited at 230-350°C by HWCVD, at a potentially much lower cost. Investigations into grown PS emitters for light trapping could prove to be very interesting.

8.2.6 Porous epitaxial films as a template for nanostructured devices

The last potential application discussed in this thesis is the use of porous epitaxial silicon as a manufacturable method of achieving nanostructured photovoltaic devices. One could imagine etching the porous regions of the *n*-type PS and then subsequently depositing a p+ film into the pores, or alternatively, seeding nanowire growth in the pores via VLS growth,[9] similar to the work done with VLS growth in alumina templates (Fig. 8.1).[10] This device would take advantage of the uncoupling of the absorbing thickness and the carrier collection length, similar to radial junction solar cells[11] and parallel multi-junction solar cells,[12] but would provide a more robust template for manufacturing and metallization than traditional nanowire growth.

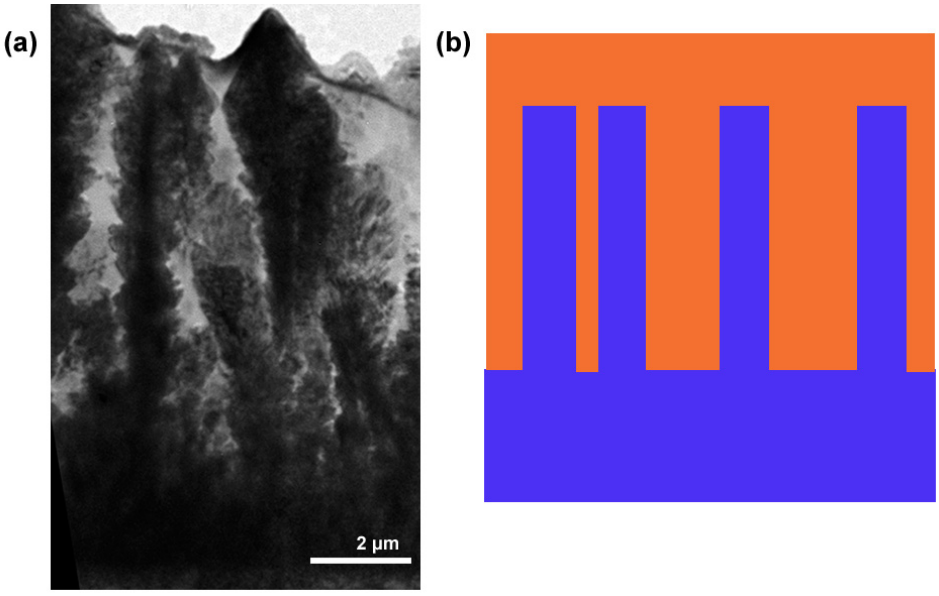

Figure 8.1 (a) TEM cross-sectional image of a crystalline porous film with columnar grains and pores. (b) Schematic of nanostructured solar cell using columnar porous silicon.

8.3 References

1. C. M. Chen, "*Polycrystalline Silicon Thin-films for Photovoltaics,*" California Institute of Technology, 2001.

2. C. E. Richardson, M. S. Mason, and H. A. Atwater, Amorphous and Nanocrystalline Silicon Science and Technology-2004 (Materials Research Symposium Proceedings Vol.808), 227 (2004).

3. B. Rau, J. Schneider, E. Conrad, and S. Gall, Proceedings of the Mat. Res. Soc. Sym., San Francisco, 2006.

4. A.G. Aberle, A. Straub, P.I. Widenborg, A.B. Sproul, Y. Huang, and P. Campbell, Prog. Photovolt: Res. Appl. 13, 37 (2005).

5. J. K. Holt, "*Hot-Wire Chemical Vapor Deposition of Silicon and Silicon Nitride for Photovoltaics: Experiments, Simulations, and Applications,*" California Institute of Technology, 2003.

6. W. Liu, X. Xie, M. Zhang, Q. Shen, C. Lin, L. Wang, and P. K. Chu, J. Vac. Sci. Technol. 21 (1), 168 (2003).

7. A. V. Chemakin, I. G. Neizvestny, N. L. Shwartz, Z. Sh. Yanovitskaja, and A. V. Zverev, Phys. Low-Dim. Struct. 9-10, 7 (2002).

8. A. P. Vasilenko, A. V. Kolesnikov, E. M. Trukhanov, L. V. Sokolov, A. A. Federov, O. P. Pchelyakov, and S. I. Romonov, Inst. Phys. Conf. Ser. 166 (Ch. 3), 173 (2000).

9. B. M. Kayes, C. E. Richardson, N. S. Lewis, and H. A. Atwater, Proceedings of the 31st IEEE Photovoltaics Specialist Conference, Lake Buena Vista, FL, 2005.

10. B. M. Kayes, J. Spurgeon, T. Sadler, N. Lewis, and H. A. Atwater, Proceedings of the 4th IEEE WCPEC, Waikoloa, HI, 2006.

11. Brendan M. Kayes, Harry A. Atwater, and Nathan S. Lewis, Journal of Applied Physics 97 (11), 114302 (2005).

12. S. A. Edmiston, A. B. Sproul, M. A. Green, and S. R. Wenham, Progress in Photovoltaics 3 (5), 330 (1995).

Appendix A

Contamination Probability Model

A.1 Introduction

In HWCVD experiments, the critical epitaxial thickness decreases with an increase in substrate temperature unlike MBE and PECVD.[1] This is most likely due to the high hydrogen content generated during HWCVD growth. Silane decomposes with 70% efficiency and hydrogen decomposes with 14% efficiency.[2] A model that considers the oxygen incorporation into the first monolayer of Si growth on an H-passivated Si (100) surface is proposed to help explain epitaxial breakdown. The Si/O ratio in the first monolayer of growth increases with a decrease in the substrate temperature, and a maximum in the Si/O ratio is seen at a different hydrogen dilution for each substrate temperature. These results help us to understand the optimal conditions for epitaxial growth during HWCVD.

A.2 Probability Model for Epitaxial Growth

The epitaxial growth and growth breakdown trends described above are consistent with a simple model correlating epitaxial growth breakdown with surface oxidation. Starting with an initial hydrogen surface coverage dependent only on the substrate temperature determined from TPD data (Table A.1),[3] the model determines the steady-state surface hydrogen coverage by balancing thermal desorption of surface hydrogen with adsorption and abstraction of surface hydrogen by atomic hydrogen produced by the hot wire. Oxygen atoms can be incorporated into the film at any empty sites. We used the model to determine the amount of oxygen deposited during the growth of the first monolayer of silicon for a given growth temperature as a function of

dilution ratio R ($R=H_2/SiH_4$) at constant pressure, assuming that all silicon atoms incident on the substrate contribute to growth.[4]

Ts (K)	TPD Flowers *et al.*[3]
584	1.41
613	1.4
632	1.36
654	1.27
671	1.17
685	1.12
707	1.04
717	1.02
736	0.98
755	0.88
769	0.79
774	0.71
778	0.64
781	0.6
785	0.53
793	0.44
795	0.36
802	0.27
807	0.18
814	0.11
821	0.06
835	0.02
847	0.01
868	0

Table A.1: Table of the fractional surface coverage of H on a Si (100) surface at different substrate temperatures from summing Flowers data.[3]

We consider a model for the thermal desorption of hydrogen proposed by Flowers *et al*.[5] in which the overall rate of change of the fractional coverage, Θ, of the Si (100) surface during temperature-programmed desorption (TPD) can be determined by considering the Si (100) surface as an ensemble of 1×1 and 2×1 lattice sites which are occupied by indistinguishable hydrogen atoms. θ_{00}, θ_{10}, θ_{11}, and θ_2 represent the fractional coverages of unoccupied dimers, singly occupied dimers, doubly occupied dimers, and dihydride species, respectively. It must be true that both

$$\theta_{00} + \theta_{10} + \theta_{11} + \theta_2 = 1 \quad \text{(A.1)}$$

$$\frac{1}{2}\theta_{10} + \theta_{11} + 2\theta_2 = \Theta \quad \text{(A.2)}$$

To define the distribution of surface species, but not the mechanism by which they are established, then the quasi-equilibrium state for the reactions

$$\text{H-Si-Si-H + Si=Si} \leftrightarrow \text{2H-Si-Si} \quad \text{(A.3)}$$

$$\frac{3}{2}\,\text{H-Si-Si-H} \leftrightarrow \text{H-Si-Si}\cdot + \text{H-Si-H} \quad \text{(A.4)}$$

are assumed. If the only significant differences in the vibrational partition functions for the surface groups are due to Si-H vibrations, then the equilibrium between surface species can be described by the vibrational partition functions

$$\frac{\theta_{10}^2}{\theta_{00}\theta_{11}} = \frac{4Q_{10}^2}{Q_{11}} \exp\left(-\frac{\varepsilon_1}{kT}\right) \quad \text{(A.5)}$$

$$\frac{\theta_{10}\theta_2}{\sqrt{\theta_{11}^3(1+\theta_2)}} = \frac{Q_{10}Q_2}{Q_{11}^{3/2}} \exp\left(-\frac{\varepsilon_2}{kT}\right) \quad \text{(A.6)}$$

where the Q's represent the vibrational partition functions for surface species

$$Q = \prod_i \frac{\exp\left(-\frac{\nu_i}{kT}\right)}{\sum_j \exp\left(-\frac{\nu_i}{kT}\right)} \quad \text{(A.7)}$$

and the Si-H vibrational frequencies can be obtained from published data and is listed in Table A.2.

The rate of change of the surface hydrogen coverage on Si (100) during HWCVD growth at a specific temperature is given by

$$\frac{\partial\Theta}{\partial t} = \frac{\partial\Theta}{\partial t}_{adsorption} - \frac{\partial\Theta}{\partial t}_{abstraction} - \frac{\partial\Theta}{\partial t}_{desorption} - \frac{\partial\Theta}{\partial t}_{oxidation} \quad \text{(A.8)}$$

where

$$\left(\frac{\partial \Theta}{\partial t}\right)_{adsorption} = \Phi_H P_{ads} \exp\left(-\frac{E_{ads}}{kT}\right)(2-\Theta) \qquad \text{(A.9)}$$

$$\left(\frac{\partial \Theta}{\partial t}\right)_{abstraction} = \Phi_H P_{abs} \exp\left(-\frac{E_{abs}}{kT}\right)(\Theta) \qquad \text{(A.10)}$$

$$\left(\frac{\partial \Theta}{\partial t}\right)_{desorption} = \nu_a \theta_{11} \exp\left(\frac{-E_a}{kT}\right) + \nu_b \theta_2^2 \exp\left(\frac{-E_b}{kT}\right) \qquad \text{(A.11)}$$

and

$$\left(\frac{\partial \Theta}{\partial t}\right)_{oxidation} = \Phi_{O2} P_{ox} (\theta_{00} + \frac{1}{2}\theta_{10}) \qquad \text{(A.12)}$$

The flux of hydrogen at the wire, $\Phi_{H,}$ can be determined from:

$$\Phi_H = \frac{0.14 P_H}{\sqrt{2\pi mkT}} \qquad \text{(A.13)}$$

where P_H is the hydrogen partial pressure, 0.14 is the cracking coefficient of hydrogen, m is the mass of a hydrogen atom, k is Boltzmann's constant and T is the temperature of a wire.

The partial pressure of oxygen in the chamber is assumed to be approximately 1×10^{-7} Torr at a base pressure of 5×10^{-7} Torr. The oxidation rate at the equilibrium surface coverage for a given temperature is given by equation A.12 where $P_{ax} = 0.01$, the sticking coefficient of oxygen, is roughly temperature independent.[6]

The distribution of these surface species can be calculated from their vibrational partition function which can be obtained from published data. By solving Equations A.1, A.2, and the vibrational partition functions for a particular hydrogen coverage and surface temperature, the equilibrium distributions of all surface species on Si (100) can be calculated.

By setting equation A.8 equal to zero, we can determine the equilibrium surface coverage of Si (100) during HWCVD growth under various growth conditions. We hypothesize that the incorporation of contaminants, *i.e.*, oxygen adsorption, contributes to epitaxial breakdown. When

the ratio of silicon to oxygen deposition is highest, the greatest h_{epi} may be achieved, although the exact correspondence between h_{epi} and the silicon to oxygen ratio is unknown.

A.3 Changes to the original model

The original model is discussed in Maribeth Mason's thesis.[7] Several changes to the model were made including the absorption probability and starting value for the code. This model starts with the hydrogen surface coverage fraction from Flowers' TPD data[3] as opposed to starting with a hydrogen only pretreat at the deposition conditions. The limits of the fractional coverage also changed to be less than or equal to one and greater than or equal to zero.

	Value	Reference
Density of Si atoms on Si(100) surface	6.8×10^{14} cm^{-2}	3
P_{ads}	0.6	8
P_{abs}	0.18	5
P_{ox}	0.01	6
E_{ads}	0.1 kcal/mol	9
E_{abs}	2 kcal/mol	5
ε_1	6 kcal/mol	3
ε_2	19 kcal/mol	3
v_a	2e15 s^{-1}	3
E_a	57.2 kcal/mol	3
v_b	3.2e13 s^{-1}	3
E_b	43 kcal/mol	3
Cracking probablility H_2	0.14	10
Cracking probability SiH_4	0.7	10
H-SiSi stretch	2093 cm^{-1}	3
H-SiSi bend	621 cm^{-1}	11
H-SiSi-H sym. Stretch	2088 cm^{-1}	12
H-SiSi-H asym. stretch	2099 cm^{-1}	12
H-Si-H deformation	637 cm^{-1}	11
H-Si-H sym. Stretch	2091 cm^{-1}	13
H-Si-H asym. Stretch	2104 cm^{-1}	13
H-Si-H scissors	910 cm^{-1}	14
TPD data		3

Table A. 2: Values used in the contaminant incorporation model.

A.4 Mathematica Model

```
(*Temperatures are in degrees Kelvin*)
Tsube=584
Twire=2073;
theta0=1.41; (*theta 0 is determined by adding Flowers' data, sum is given in table
below*)
R=25; (* R=H2/SiH4 ratio *)
Ptot=75*10^(-3); (*pressure in Torr*)
PSiH4=Ptot/(R+28);
(*R+28 or 4% dilute silane
  R+0 for 100% silane
  R+23 for 5% silane
  R+99 for 1% silane*)

PSiH4inHe=25*PSiH4;
PH2=Ptot-PSiH4inHe;
O2flux=2.558*10^(13)*N[Sqrt[573/Tsub]];

NN=6.8*10^14; (*density of atoms on Si(100) surface*)

PstickH=0.6*Exp[-6.94*10^(-22)/(k*Tsub)];
(*energy converted to J/atom from 0.1 kcal/mol*)
Pabs=0.18*Exp[-1.39*10^(-20)/(k*Tsub)];
(*energy converted to J/atom from 2 kcal/mol*)
PstickO=0.01;

h=6.626*10^(-34);
c=3*10^10;
k=1.38*10^(-23);
epsilon1=6.0*4184/(6.022*10^23);
epsilon2=19*4184/(6.022*10^23);
nua=2*10^(15);
Ea=57.2*4184/(6.022*10^23);
nub=3.2*10^(13);
```

```
Eb=43*4184/(6.022*10^23);
mh=1.7*10^(-27);
dh=1.06*10^(-10);
dsi=2.2*10^(-10);
rwire=.025; (*wire radius in cm*)
dwsub=2.5; (*wire to substrate distance cm*)

Fluxatwire=(PH2*133*0.14)/(100^2*Sqrt[2*Pi*mh*k*Twire]);
Fluxnocoll=Fluxatwire*rwire/dwsub;
(*assumes cylindrical distribution around the wire*)
fluxin=Fluxnocoll;
FluxSiH4wire=(PSiH4*133*0.7)/(100^2*Sqrt[2*Pi*28*mh*k*Twire]);
FluxncSiH4=FluxSiH4wire*rwire/dwsub;
fluxinSi=FluxncSiH4;
Fluxratio=(fluxin+fluxinSi)/fluxinSi;
T=Tsub;

Print["T = ",Tsub];
Print["Ptot = ",Ptot];
Print["R = ",R];
Print["PSiH4 in He = ",PSiH4inHe];
Print["PSiH4 = ",PSiH4];
Print["PH2 = ",PH2];
Print["fluxin = ",fluxin];
Print["flux silicon in = ",fluxinSi];
Print["flux ratio = ",Fluxratio];

Q10=Exp[-h*c*(2093)/2/k/T]*Exp[-h*c*(621)/2/k/T]/(1-Exp[-h*c*(2093)/k/T])/(1-Exp[-
h*c*(621)/k/T]);
Q11=Exp[-h*c*(2088)/2/k/T]*Exp[-h*c*(2099)/2/k/T]/(1-Exp[-h*c*(2088)/k/T])/(1-Exp[-
h*c*(2099)/k/T]);
Q2=Exp[-h*c*(637)/2/k/T]*Exp[-h*c*(2091)/2/k/T]*Exp[-h*c*(2104)/2/k/T]*Exp[-
h*c*(910)/2/k/T]/(1-Exp[-h*c*(637)/k/T])/(1-Exp[-h*c*(2091)/k/T])/(1-Exp[-
h*c*(2104)/k/T])/(1-Exp[-h*c*(910)/k/T]);
```

```
VerboseDthetadt[Theta_]:=Module[{theta00,theta10,theta11,theta2,eqn3,sol3,theta11A,t
heta11B,eqn4,eqn4A,eqn4B,sol4A,sol4B,sols,solns,realsolns,n,t10,t11,t00,t2,dThetadtd
es,dThetadtads,dThetadtabs,dThetadt},
    theta00=1-theta10-theta11-theta2; (*solve for theta00*)
     theta10=2 (Theta-theta11-2 theta2); (*solve for theta100*)
     eqn3={theta10^2/theta00/theta11==4 Q10^2/Q11*Exp[-epsilon1/k/T]};
   sol3=Solve[eqn3,theta11]; (*gives 2 answers for theta11, equation from Flowers,
then expands them*)
     theta11A=Expand[theta11/.sol3[[1]]];
     theta11B=Expand[theta11/.sol3[[2]]];


eqn4={theta10^2 theta2^2/theta11^3/(1+theta2)==Q10^2 Q2^2/Q11^3 Exp[-2 epsilon2/(
k T)]};
     eqn4A=eqn4/.{theta11→theta11A};
     eqn4B=eqn4/.{theta11→theta11B};
     sol4A=Solve[eqn4A,theta2];
     sol4B=Solve[eqn4B,theta2];
     sols={};

For[n=1,n<=Length[sol4A],n++,sols=Append[sols,Union[sol3[[1]]/.sol4A[[n]],sol4A[[n]]]]];

For[n=1,n<=Length[sol4B],n++,sols=Append[sols,Union[sol3[[2]]/.sol4B[[n]],sol4B[[n]]]]];
(* Solutions must be between zero and one with the imaginary part equal to zero*)
     solns={theta00,theta10,theta11,theta2}/.sols;
     realsolns=solns;
     realsolns=Select[realsolns,Im[#[[1]]]==0&];
     realsolns=Select[realsolns,Im[#[[2]]]==0&];
     realsolns=Select[realsolns,Im[#[[3]]]==0&];
     realsolns=Select[realsolns,Im[#[[4]]]==0&];
     realsolns=Select[realsolns,Re[#[[1]]]>=0&];
     realsolns=Select[realsolns,Re[#[[2]]]>=0&];
     realsolns=Select[realsolns,Re[#[[3]]]>=0&];
     realsolns=Select[realsolns,Re[#[[4]]]>=0&];
     realsolns=Select[realsolns,Re[#[[1]]]<=1&];
     realsolns=Select[realsolns,Re[#[[2]]]<=1&];
     realsolns=Select[realsolns,Re[#[[3]]]<=1&];
     realsolns=Select[realsolns,Re[#[[4]]]<=1&];
```

```
    Print["Theta = ",Theta];
    Print[realsolns];
    If[Length[realsolns]>0,t00=realsolns[[1]][[1]];
     t10=realsolns[[1]][[2]];
     t11=realsolns[[1]][[3]];
     t2=realsolns[[1]][[4]];
     dThetadtdes=(-nua*t11*Exp[-Ea/k/T]-nub*t2^2*Exp[-Eb/k/T]);
     Print["dTheta/dt (desorption) = ",dThetadtdes];
     dThetadtads=fluxin*PstickH*(2-Theta)/2/NN;
     Print["dTheta/dt (adsorption) = ",dThetadtads];
     dThetadtabs=-fluxin*Pabs*(Theta)/2/NN;
     Print["dTheta/dt (abstraction) = ",dThetadtabs];
     dThetaox=O2flux*(2-Theta)*PstickO/2/NN;
     Print["dTheta/dt (oxidation) = ",dThetaox];
     dThetadt=dThetadtdes+dThetadtads+dThetadtabs+dThetaox;
     Print["dTheta/dt = ",dThetadt];
     dThetadt,0]];


Dthetadt[Theta_]:=Module[{theta00,theta10,theta11,theta2,eqn3,sol3,theta11A,theta11B
,eqn4,eqn4A,eqn4B,sol4A,sol4B,sols,solns,realsolns,n,t10,t11,t00,t2,dThetadtdes,dThet
adtads,dThetadtabs, dThetadt},theta00=1-theta10-theta11-theta2;
    theta10=2 (Theta-theta11-2 theta2);
    eqn3={theta10^2/theta00/theta11==4 Q10^2/Q11*Exp[-epsilon1/k/T]};
    sol3=Solve[eqn3,theta11];
    theta11A=Expand[theta11/.sol3[[1]]];
    theta11B=Expand[theta11/.sol3[[2]]];
    eqn4={theta10^2 theta2^2/theta11^3/(1+theta2)==Q10^2 Q2^2/Q11^3 Exp[-2
epsilon2/(k T)]};
    eqn4A=eqn4/.{theta11→theta11A};
    eqn4B=eqn4/.{theta11→theta11B};
    sol4A=Solve[eqn4A,theta2];
    sol4B=Solve[eqn4B,theta2];
    sols={};

For[n=1,n<=Length[sol4A],n++,sols=Append[sols,Union[sol3[[1]]/.sol4A[[n]],sol4A[[n]]]]];
```

```
For[n=1,n<=Length[sol4B],n++,sols=Append[sols,Union[sol3[[2]]/.sol4B[[n]],sol4B[[n]]]]];
    solns={theta00,theta10,theta11,theta2}/.sols;
    realsolns=solns;
    realsolns=Select[realsolns,Im[#[[1]]]==0&];
    realsolns=Select[realsolns,Im[#[[2]]]==0&];
    realsolns=Select[realsolns,Im[#[[3]]]==0&];
    realsolns=Select[realsolns,Im[#[[4]]]==0&];
    realsolns=Select[realsolns,Re[#[[1]]]>=0&];
    realsolns=Select[realsolns,Re[#[[2]]]>=0&];
    realsolns=Select[realsolns,Re[#[[3]]]>=0&];
    realsolns=Select[realsolns,Re[#[[4]]]>=0&];
    realsolns=Select[realsolns,Re[#[[1]]]<=1&];
    realsolns=Select[realsolns,Re[#[[2]]]<=1&];
    realsolns=Select[realsolns,Re[#[[3]]]<=1&];
    realsolns=Select[realsolns,Re[#[[4]]]<=1&];
    If[Length[realsolns]>0,t00=realsolns[[1]][[1]];
      t10=realsolns[[1]][[2]];
      t11=realsolns[[1]][[3]];
      t2=realsolns[[1]][[4]];
      dThetadtdes=(-nua*t11*Exp[-Ea/k/T]-nub*t2^2*Exp[-Eb/k/T]);
      dThetadtads=fluxin*PstickH*(2-Theta)/2/NN;
      dThetadtabs=-fluxin*Pabs*(Theta)/2/NN;
      dThetaox=O2flux*(2-Theta)*PstickO/2/NN;
      dThetadt=dThetadtdes+dThetadtads+dThetadtabs+dThetaox;
      dThetadt=N[dThetadt];
      ClearAll[theta00,theta10,theta11,theta2];
      dThetadt,0]];

ClearAll[theta];
theta=theta0;
Odeposit=0;
Sideposit=0;
stepsize=0.002;
dthdt=9999;
```

```
n=0;
While[Sideposit<6.8*10^14,t=n*stepsize;
   Print["t = ",n*stepsize];
   Print["theta = ",theta];
   Print["deposited Oxygen atoms = ",Odeposit];
   Print["deposited Silicon atoms = ",Sideposit];
   If[Abs[dthdt]>10^(-7),dthdt=Dthetadt[theta],dthdt=0];
   Print["Dtheta/Dt = ",dthdt];
   Print[];
   theta=theta+dthdt*stepsize;
   Odeposit=Odeposit+dThetaox*stepsize*2*NN;
   Sideposit=Sideposit+ fluxinSi*stepsize;
   n=n+1];
```

A.5 References

1. Michio Kondo, H. Fujiwara, and Akihisa Matsuda, Thin Solid Films **430**, 130 (2003).

2. J. K. Holt, "*Hot-wire Chemical Vapor Deposition of Silicon and Silicon Nitride for Photovoltaics: Experiments, Simulations, and Applications,*" California Institute of Technology, 2003.

3. M.C. Flowers, N.B.H. Jonathon, Y. Liu, and A. Morris, Journal of Chemical Physics **99**, 7038 (1993).

4. Christine E. Richardson, M. S. Mason, and Harry A. Atwater, Thin Solid Films **501** (1-2), 332 (2006).

5. M.C. Flowers, N.B.H. Jonathon, Y. Liu, A. Morris, and S. Wright, Surface Science **396**, 227 (1998).

6. M.P. D'evelyn, M.M. Nelson, and T. Engel, Surface Science **186**, 75 (1987).

7. Maribeth S. Mason, "*Synthesis of Large-Grained Polycrystalline Silicon by Hot-Wire Chemical Vapor Deposition for Thin Film Photovoltaic Applications,*" California Institute of Technology, 2004.

8. U. Hansen and P. Vogl, Phys. Rev. B **57** (20), 57 (1998).

9. D. D. Koleske, S. M. Gates, and B. Jackson, **101** (4), 3301 (1994).

10. J.K. Holt, M. Swiatek, D.G. Goodwin, R.P. Muller, W.A. Goddard III, and Harry A. Atwater, Thin Solid Films **395**, 29 (2001).

11. H. Froitzheim, U. Koler, and H. Lammering, Surface Science **149**, 537 (1985).

12. Y. J. Chabal and K. Raghavachari, Phys. Rev. Letters **53**, 282 (1984).

13. Y. J. Chabal and K. Raghavachari, Phys. Rev. Letters **54**, 1055 (1985).

14. P. Gupta, V. L. Colven, and S. M. George, Phys. Rev. B **37**, 8234 (1988).

Appendix B

Silane System Safety Procedures

B.1 Basic Operating Procedures

1. Only trained personnel should operate the system.
2. Ensure that silane and air are not mixed.
3. Ensure that the gate valves are not opened unless each MPZ chamber has been evacuated and flushed after processing.
4. Check that the turbo molecular pumps and rotary vane pumps are functional.
5. Check that the gas cabinets are in the appropriate state.
6. Check that the Thermal Combustion System (TCS) is properly working.
7. Always store cylinders in a secure fashion.
8. Be mindful of the gauges inside the gas cabinets to ensure the purge is proceeding correctly.

B.2 Gas Cabinet Procedures: Automatic Cabinet

This is for bottle changes, MFC changes, and any other time you need to purge the gas cabinet. There should always be two people around for safety reasons in order to double check the procedures. Always wear gloves and eye protection.

1. Check to make sure N_2 above gas cabinet is above 90 psi (Venturi vacuum and valve operation).
2. Check that N_2 gas cylinders inside cabinet for dilution are set to 25 psi and are open.
3. Make sure the N_2 flow meter inside the phosphine gas cabinet (all the way to the right) is set to between 16-20 scfm. This allows a trickle purge to dilute the line up the entire stack.
4. Make sure CGA fitting is tight (have buddy double check).
5. Start automatic purge offline/online – display will prompt when to open/close silane gas cylinder and when to adjust flow rate regulator.
6. If purging offline make sure to remove restrictive flow orifice (RFO) from CGA connection on the cylinder.

7. If purging online make sure restrictive flow orifice (RFO) is in CGA connection on the cylinder.
8. ***Only do one purge at a time!*** There is not enough Nitrogen to support two purges.

B.3 Manual Gas Cabinet Offline Purge

1. Close gas cylinder (have buddy double check)
2. Close LPI (low pressure inlet) and ESV (emergency shut-off valve)
3. Open VGV (Vacuum Generator Valve)
4. Open LPV (Low Pressure Vent) and HPI (High Pressure Inlet) for 20s (this purges out the process line)
5. Close LPV and HPI
6. Repeat steps 3 and 4, 10 times
7. Open ESV(Emergency Shut-Off Valve) and HPV(High Pressure Vent) for 20s
8. Close HPV
9. Open PGI (Purge Gas Inlet) for 20s allows bottle nitrogen into the manifold
10. Close PGI
11. Repeat 6-9, 20 times
12. Close all valves: VGV, LPV, HPI, ESV, HPV, and PGI
13. Double check that the regulator is empty.
14. Take off cylinder at CGA valve.
15. Remove restricting flow orifice (RFO).

B.4 Manual Gas Cabinet Online Purge

1. Attach cylinder at CGA valve with RFO in it (have buddy double check)
2. Close regulator on the manifold
3. Open VGV
4. Open ESV and HPV for 20s
5. Close HPV
6. Open PGI for 20s allows bottle nitrogen into the manifold
7. Close PGI
8. Repeat 4-7, 20 times
9. Close ESV, HPV, and PGI
10. Keep VGV open
11. Open LPV and HPI for 20s (this purges out the process line)

12. Close LPV and HPI
13. Repeat 11 and 12, 10 times
14. Close VGV, LPV, and HPI
15. Make sure CGA fitting is tight
16. Open cylinder
17. Open ESV and HPI
18. Adjust regulator to 5-10 psi.
19. Open LPI (low pressure inlet)
20. Process flow is open

B.5 Gas Line Purge Procedure

This is for a Mass Flow Controller change or any other valve change in the line between the gas cabinet and the deposition chamber. You will need to ***purge all of the lines*** since they are all connected where they go into the chamber.

1. Make sure the TCS is on.
2. Close the cylinder valve on the line to be purged.
3. Purge gas cylinder offline using above procedures.
4. Ensure that the pumps exhibit normal operating conditions.
5. Ensure that the throttle valve (to the pumps) is open.
6. Set the flow for all the appropriate gas lines to 100 sccm.
7. Open flow to the pumps. (MFC, on/off and gate valves).
8. Wait for the gas flow to show zero.
9. Wait for the regulator to show negative pressure.
10. Continue to pump on the lines.
11. Put the gas cabinets into manual mode.
12. Open LPI
13. Open LPV
14. Open PGI (make sure N2 is really flowing through the line by looking at the regulator gauge.
15. Watch flow through MFCs increase.
16. Allow to flow for several minutes.
17. Close PGI
18. Close LPV

19. Close LPI
20. Continue to pump on line till MFC reads zero flow.
21. Close MFC, on/off gas and gate valve.

B.6 System Interlocks

1. If the chamber pressure is too high (above the setpoint on the pressure controller) then process gasses will not flow.
2. If the main gas inlet valve is open in the chamber, the chamber gate valve will not open.
3. The external hydride monitoring system has 2 levels of alarms.
    a. Level 1 actuates a light outside of the lab in the hallway and occurs at 5ppm.
    b. Level 2 actuates a light and an audio alarm outside of the lab in the hallway and occurs at 10 ppm.
    c. Other error may occur that cause the system to beep inside room 249. These are most often due to the chemcassette tape running out.
4. If the gas cabinet is rocked, it will alarm and go into standby mode.
5. EMO's are located:
    a. On the system front panel
    b. On each gas cabinet
    c. On the electrical manifold
    d. On the thermal combustion unit
6. In case of power failure all valves default into closed position.

B.7 Emergency Off Procedure

1. Put the cabinets into standby mode.
2. Leave the room if there is any danger.
3. Assure that it is safe to re-enter the room and that there is no damage to the nitrogen or vent lines.
4. Purge the cylinder offline.
5. Turn off the electricity at the EMO on the electrical manifold (will need to be reset on the inside).

B.8 Vacation Shutdown Procedure

If the system will be idle for a week or longer, please use the vacation shutdown procedure.

1. Purge silane cylinders off line.

2. Turn off Thermal Combustion System.
3. Turn off hydride detector.

B.9 Accidental Release Procedures

1. Personal precautions
    a. Wear self-contained breathing apparatus when entering area unless atmosphere is proved to be safe.
    b. Evacuate area.
    c. Ensure adequate air ventilation.
    d. Eliminate ignition sources (look at hydride monitor to see where it is alarming from).
2. Clean up methods
    a. Ventilate area.
    b. Dust deposited may be vacuum cleaned or the area hosed down with water.

B.10 Figures

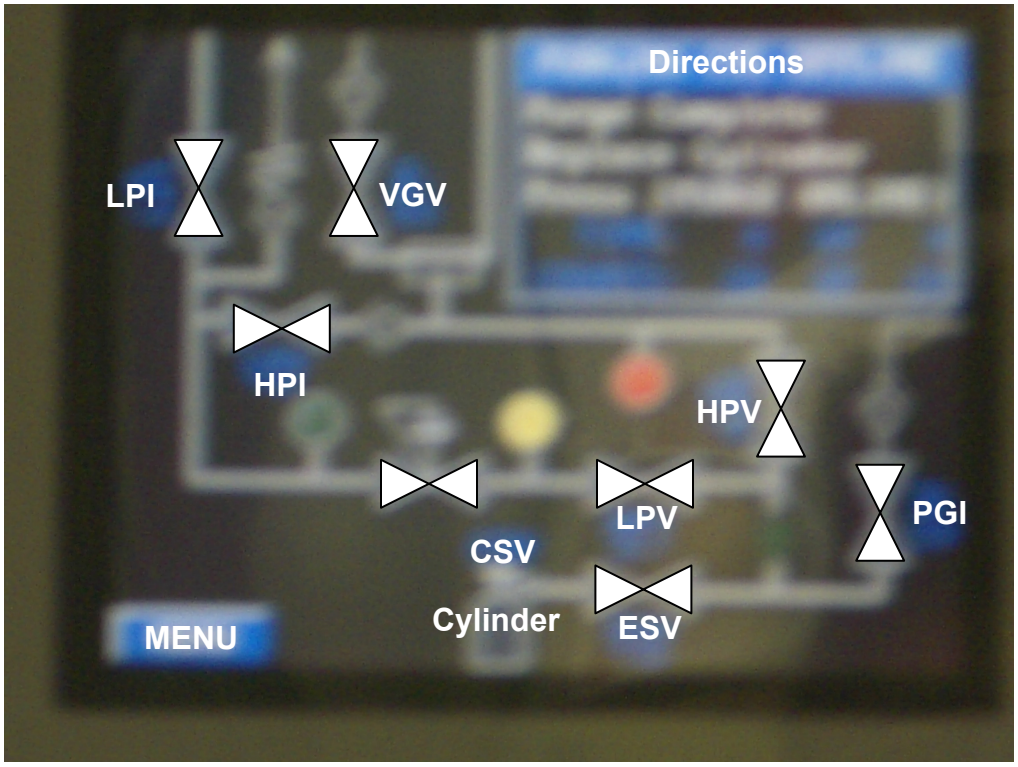

Figure B.1 Automatic Gas Cabinet Display

1. Valves are black when closed.
2. Valves are green when open.
3. The code to get into manual mode is 2000.

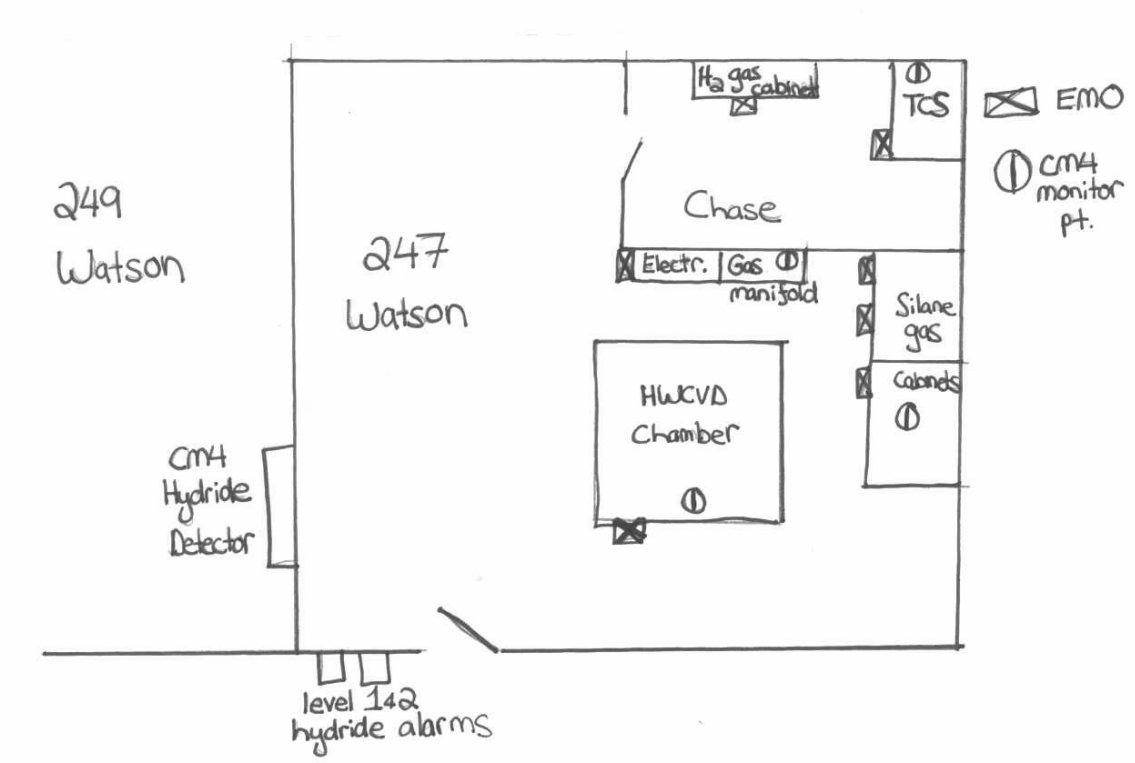

Figure B.2 Silane System Physical Schematic: Gases flow from the cabinets to the gas manifold into the chamber and then out to the TCS. During bottle changes gas flows from the cabinet to the exhaust on the roof.

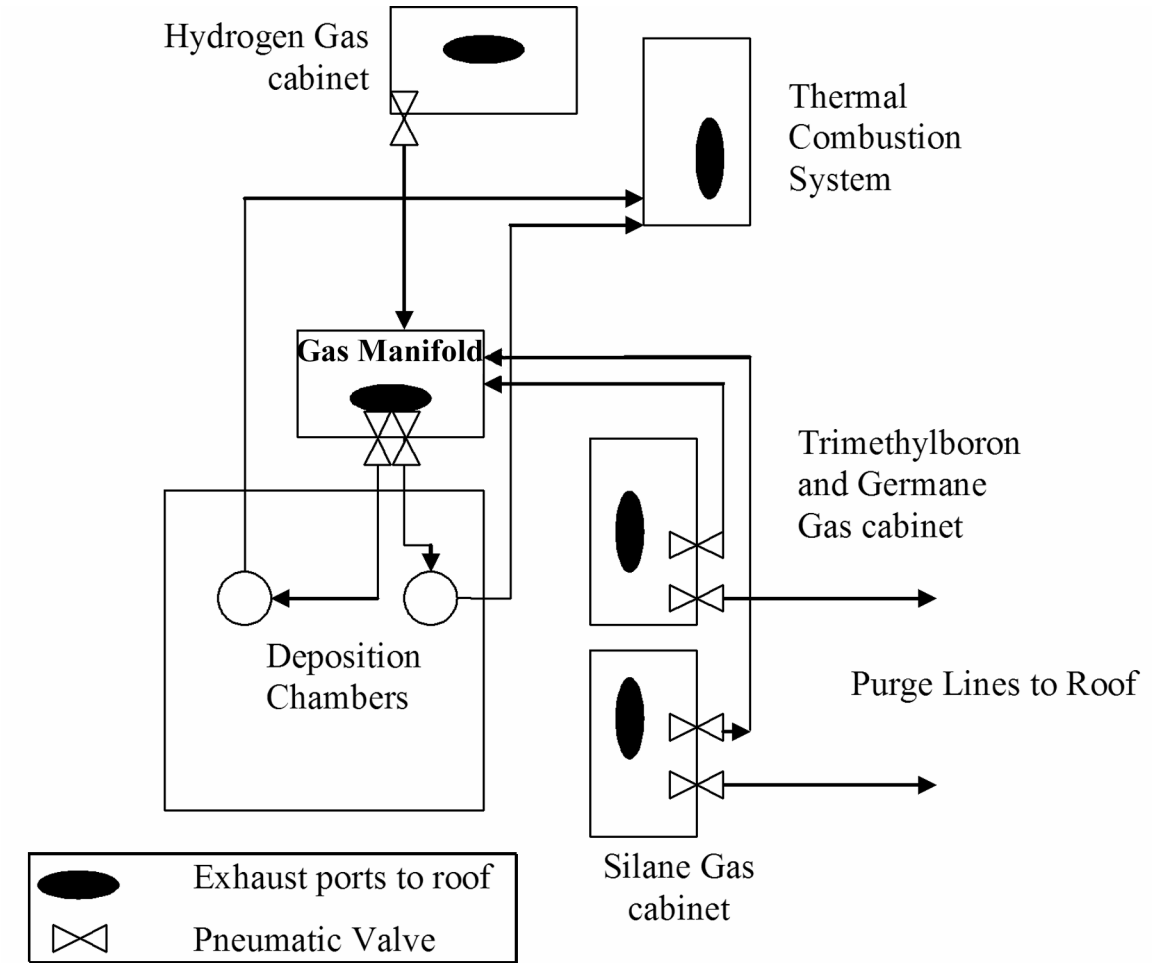

Figure B.3 Schematic of silane system in 247 Watson. Gases flow from the cabinets to the gas manifold into the chamber and then out to the TCS. During bottle changes gas flows from the cabinet to the exhaust on the roof.

Appendix C

Procedure for Fabricating Large-grained Polycrystalline Templates with Nickel Nanoparticles

1. Ni nanoparticles of 20-200 nm are mixed in isopropanol to a nanoparticle concentration of 20 μg/ml.
2. The solution is subjected to an ultrasonic treatment for 30 minutes in order to evenly distribute the particles before use.
3. Wait ~1 hour till the larger nanoparticles sink to the bottom of the solution.
4. Deposit 100 nm of a-Si by any method. *Note: The HWCVD amorphous films did not yield good results probably due to the high H content of the films grown at low temperatures. The amorphous Si recipe needs to be optimized for the 5% silane mixture with 5ppm PH_3 currently in use.*
5. Dope *in-situ* or by ion-implantation to an *n*-type phosphorous carrier concentration of $1x10^{19}$ cm^{-3}. Implantation doses can be found in C. Chen, *Ph.D. Thesis, Caltech* (2001).
6. Spin on approximately 90 μl per 1 in^2 sample for 20 seconds at 1500 rpm immediately following deposition of the film, after oxide formation, or after an HF dip depending on the desired results and the substrate type (Fig. C.1).

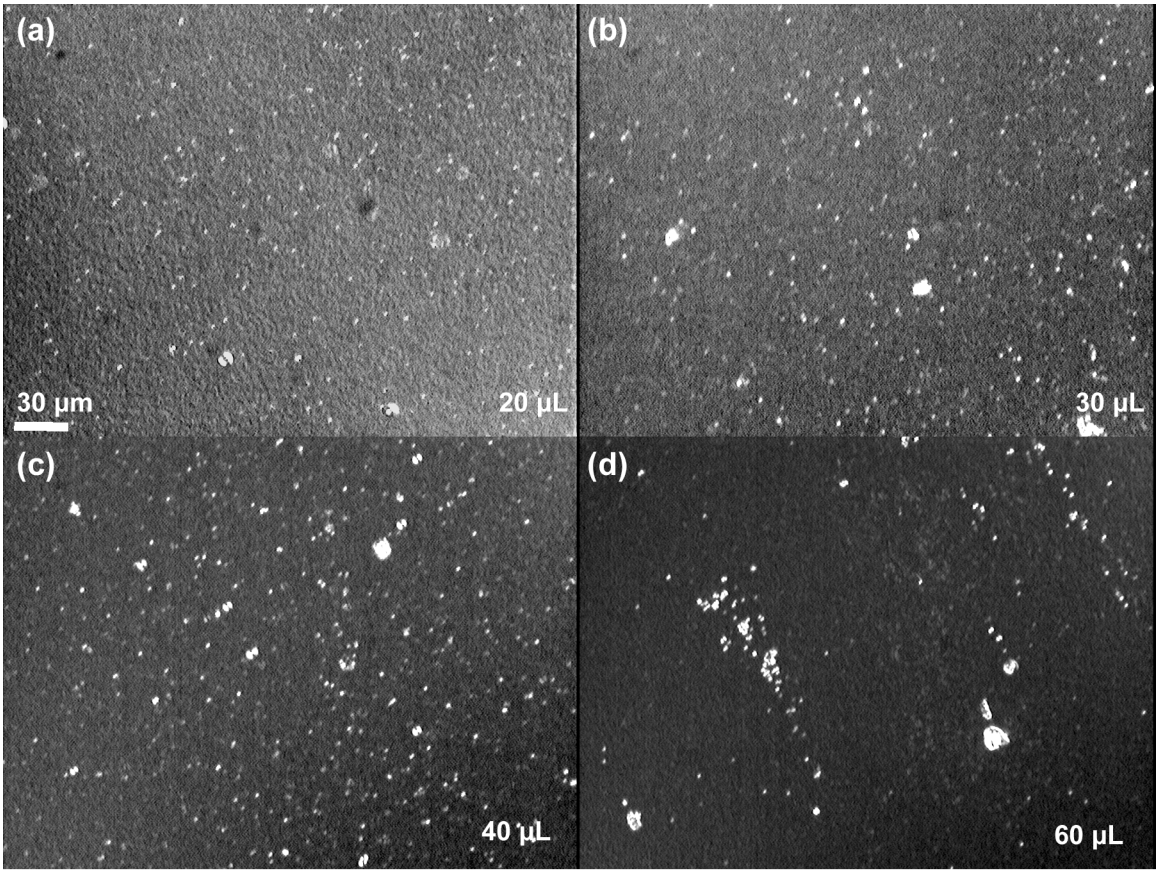

Figure C.1 The effect of the amount of Ni ink on the interparticle spacing of the Ni nanoparticles on a 1 cm^2 sample. (a) 20 µL (b) 30 µL (c) 40 µL and (d) 60 µL. Too much ink appears to cause the Ni to cluster and streak on the substrate. Smaller amounts appear to have no effect on the Ni interparticle distance

7. Anneal at 600°C for ~18 hours under vacuum.

8. Templates on low-temperature glass must be fully supported on a Si wafer or quartz holder in order for the sample to remain flat during the high temperature anneal.

9. After ~24 hours, the temperature can be increased to between 700-900°C in order to fully crystallize the template.

Appendix D

Porous Amorphous Silicon Films for Nanostructured Photovoltaics

Porous amorphous Si thin films are an interesting area of research for nanostructured photovoltaic devices. One can imagine filling the pores with amorphous or crystalline Si and Si_xGe_{1-x} or a calcogenide material; for either a homo- or hetero-junction device. The pores could be opened and widened by a chemical etch and then filled either by a chemical vapor deposition process, such as HWCVD, by Vapor-Liquid-Solid growth, or by electrodeposition.

Depending upon the deposition condition, the pores can be aligned in the growth direction or at some angle to it (Figure D.1). The reason for the off angle is not understood. The pores are a significant fraction of the total volume of the film, with the color of the film changing dramatically with an HF dip. An SiO_2 signature can be seen in Raman spectroscopy with peaks at 460 cm^{-1} and 800 cm^{-1} (Fig. D.2).

These films were all grown with pure silane at a wire to substrate distance of 2.5 cm and two tungsten wires. To deposit these films with 5% silane dilute in argon may take some work due to the higher total pressures that are necessary to have a high enough silane flow rate. It will be much easier to grow porous crystalline films of the type described in Chapter 4.

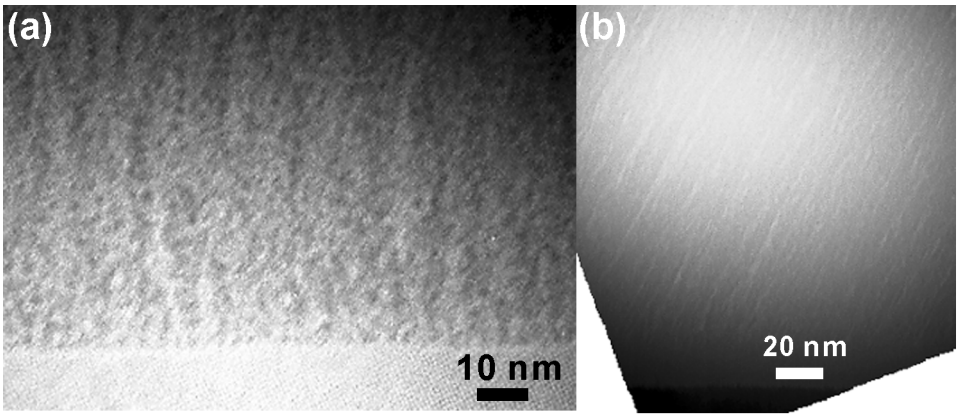

Figure D.1 Porous amorphous Si TEM cross-sectional micrographs of films grown with HWCVD using pure silane. (a) Film grown at 360°C at R=1 and 6 mTorr with pores perpendicular to the interface. (b) Film grown at 270°C at R=0 and 6 mTorr with pores at an angle to the growth direction.

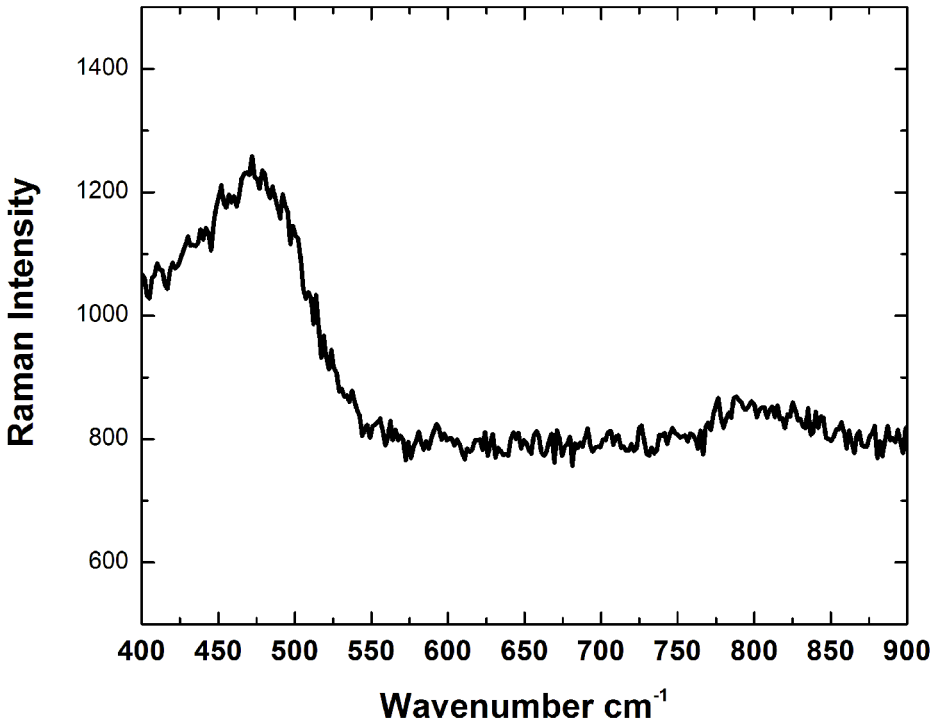

Figure D.2 Raman spectroscopy of a porous a-Si film. The scan shows signature SiO_2 peaks at 460 cm^{-1} and 800 cm^{-1} and an a-Si peak at 480 cm^{-1}.