

# **SILICON NANOWIRES AND SILICON/MOLECULAR INTERFACES FOR NANOSCALE ELECTRONICS**

Thesis by

Bonnie Ann Sheriff

In Partial Fulfillment of the Requirements

For the Degree of

Doctor of Philosophy

CALIFORNIA INSTITUTE OF TECHNOLOGY

Pasadena, California

2009

(Defended June 11, 2008)

© 2009

Bonnie Ann Sheriff

All Rights Reserved

*To my best friend and husband,*

*Bryan*

## Acknowledgements

---

I am so grateful to the many people who enriched my experiences at Caltech. First, I would like to thank my advisor, Professor Jim Heath, whose dedication to the pursuit of scientific understanding has been truly inspirational. I am indebted to his support and guidance over the last 5 years. I also would like to thank my thesis committee for their support and insights into my graduate research: Prof. Mitchio Okumura, Prof. Pat Collier, and Prof. Bill Goddard.

I was blessed to be surrounded by many excellent colleagues. I would like to acknowledge the support and assistance of several current and past Heath group members: Dunwei Wang, whom I learned so much from; Yi Luo, a true mentor for so many; and Johnny Green, Erica DeIonno, Gabe Kwong, Rosemary Rohde, Heather Agnew Akram Boukai, Habib Ahmad, Kris Beverly, Ryan Bailey, Mike McAlpine, and John Nagarah, for their friendship, guidance, and for making going to work so much fun. I also would like to thank Rosemary Rohde and Heather Agnew for their help with surface chemistry techniques and acknowledge Will Dichtel, Jason Spruell, and Dorota Rozkiewicz for their contributions with the microcontact printing project. Thanks to Ruo-Gu Huang, Peigen Cao, and Clara Ji-Hyun Cho for continuing the logic and microcontacting printing projects. I owe a big thanks to Diane Clark-Robinson for running the group efficiently and for keeping things interesting, and Kevin Kan, the guardian of the cleanroom and its equipment.

When I was an intern at Intel, I had the pleasure of working with several friendly and extremely helpful colleagues. In particular, I would like to thank Juanita Kurtin,

Janice Lee, Keith Bowman, Ravi Pillarisetty, and Tanay Karnik. I would also like to acknowledge the Intel Foundation for providing financial support during the last two years here in the form of a Ph.D. Fellowship.

I would like to acknowledge my friends at Caltech who made my experiences here so much better. In particular, I would like to thank Heather Wiencko, Christina Vizcarra, and Amie Boal for their support and friendship.

Finally, I would like to thank my husband, Bryan, who has been a source of unlimited love, friendship, laughter, support, and motivation.

## **Abstract of the thesis**

---

The thesis describes the realization of high-performance silicon nanowire (Si NW) logic circuits and a novel surface modification technique for nanoscale electronics applications. First, doped Si NWs were generated via the superlattice nanowire pattern transfer (SNAP) process, forming aligned, uniform, ultra-dense NW arrays. The NWs served as the channel material for field-effect transistors. NWs could be doped n- or p-type using a diffusion doping process and both n-FETs and p-FETs could be fabricated simultaneously on the same substrate.

Individual p-FETs exhibited excellent performance metrics compared to other NW and carbon nanotube (CNT) transistors, including high on/off ratios, low off currents, high mobilities, and low subthreshold swings. The n-type devices also had good characteristics, although they did not perform as well as the p-FETs. A comparison of nanowire and microwire device performance revealed that the NW FET performance was dominated by the high surface-area-to-volume ratio. These devices were integrated into complementary symmetry (CS) inverter circuits, which showed a consistent performance and a gain (a measure of performance) of  $\sim 5$ .

Circuit performance was optimized by utilizing a methodology that combined prototype devices with circuit simulations. First, prototype devices were fabricated and their DC and AC characteristics were tabulated into a look-up-table model. This model was accessed by a circuit simulator, which could predict the performance of arbitrary circuits utilizing these devices and provide feedback into the device design. Circuits could then be fabricated from the optimized devices resulting in increased performance.

This methodology was demonstrated by optimizing the gain of the CS inverter circuit from an initially measured value of 8 to a gain of 45.

A novel microcontact printing method was developed to functionalize gold and silicon surfaces. The copper<sup>I</sup>-catalyzed azide-alkyne cycloaddition (CuAAC) reaction was used to covalently attach molecules containing an alkyne functional group to azide-terminated monolayers on gold or silicon. The copper<sup>I</sup> catalyst in the ink solution (homogeneous catalyst) was replaced by coating the elastomer stamp with copper metal (heterogeneous catalyst). The copper-coated stamp was shown to catalyze the reaction to completion within 1 hour with a zero-order reaction rate. In comparison, the homogeneous catalyzed stamp reaction took ~ 30 minutes to complete with a pseudo first-order reaction rate. No pattern diffusion was observed, suggesting that free copper ions are not responsible for the catalysis. It is proposed that this method can be used to sequentially synthesize electronically active molecules directly onto gold or silicon electrodes.

## Table of Contents

---

Acknowledgements .....	iv
Abstract of the thesis .....	vi
Table of contents .....	viii
List of figures .....	xii
<b>Chapter 1: Thesis overview .....</b>	<b>1</b>
1.1 Introduction to nanoelectronics .....	1
1.2 Organization of the thesis .....	5
1.2.1 Summary of Chapter 2 .....	5
1.2.2 Summary of Chapter 3 .....	6
1.2.3 Summary of Chapter 4 .....	7
1.2.4 Summary of Chapter 5 .....	7
1.3 References .....	9
<b>Chapter 2: High-performance nanowire field-effect transistors .....</b>	<b>13</b>
2.1 Introduction .....	13
2.1.1 The SNAP technique .....	15
2.1.2 Conducting Si nanowire arrays .....	18
2.1.3 Organization of the chapter .....	19
2.2 Nanowire field-effect transistor fabrication .....	20
2.2.1 Substrate doping process .....	20
2.2.2 SNAP technique experimental details .....	25
2.2.3 Fabrication and measurement of the FET structure .....	28
2.3 Development of high-performance NW p-FETs .....	31
2.4 Comparison of nanowire and microwire performance .....	37
2.5 Development of high-performance nanowire n-FETs .....	41
2.6 Conclusions .....	43



2.7 References .....	44
<b>Chapter 3: Fabrication and characterization of nanowire logic circuits .....</b>	<b>48</b>
3.1 Introduction .....	48
3.1.1 Overview of logic functions .....	49
3.1.2 Organization of the chapter .....	51
3.2 The pattern doping technique .....	52
3.3 Electrostatic force microscopy characterization .....	56
3.4 Diode fabrication and characterization .....	59
3.5 SNAP nanowire alignment system .....	62
3.6 Nanowire logic circuit fabrication .....	65
3.7 DC characterization of fabricated FETs and circuits .....	68
3.7.1 Demonstration of other logic gates .....	69
3.8 Conclusions .....	71
3.9 References .....	72
<b>Chapter 4: In silico design optimization of nanowire circuits .....</b>	<b>75</b>
4.1 Introduction .....	75
4.1.1 Organization of the chapter .....	77
4.2 Large-area nanowire transistors .....	78
4.2.1 Fabrication of large-area nanowire transistors .....	78
4.2.2 DC and AC electrical characterization of large-area devices .....	80
4.2.3 Calculation of performance metrics .....	82
4.3 Setup of the device look-up-table model and simulations .....	85
4.3.1 The look-up-table format .....	86
4.3.2 Circuit simulation setup .....	89
4.4 Initial DC circuit simulation results .....	91
4.5 Transient analysis circuit simulation results .....	94
4.6 Optimized DC circuit simulation results .....	95
4.7 MEDICI simulations .....	97

4.8 Fabrication of improved n-FETs and inverter circuit performance .....	101
4.9 Potential directions for simulation methodology .....	103
4.10 Conclusions .....	104
4.11 References .....	105
4.12 Appendix A: Example DEW file .....	109
4.13 Appendix B: MEDICI code .....	110
<b>Chapter 5: Microcontact printing methods for molecular electronics                   applications .....</b>	<b>116</b>
5.1 Introduction .....	116
5.1.1 Application for high-density molecular circuits .....	118
5.1.2 Organization of the chapter .....	121
5.2 Generation of azide-terminated monolayers on Au .....	122
5.3 CuAAC reaction conditions in solution and in stamping .....	122
5.3.1 Solution CuAAC conditions .....	123
5.3.2 Microcontact printing CuAAC conditions using a homogeneous catalyst ..	123
5.3.3 Microcontact printing CuAAC conditions using heterogeneous catalyst ....	124
5.4 Surface characterization experimental procedures .....	125
5.4.1 XPS measurements .....	125
5.4.2 Contact angle measurements .....	126
5.4.3 Infrared spectroscopy measurements .....	126
5.4.4 Frictional force microscopy measurements .....	126
5.4.5 Electrochemical measurements .....	127
5.5 $\mu$ CP results using homogeneous and heterogeneous catalysts .....	128
5.5.1 Contact angles .....	128
5.5.2 Grazing angle infrared spectroscopy .....	129
5.5.3 X-ray photoelectron spectroscopy .....	131
5.5.4 Frictional force microscopy .....	132
5.5.5 Electrochemistry .....	134
5.6 Stamp kinetics comparison .....	136

5.7 The <i>StampCat</i> mechanism .....	139
5.8 $\mu$ CP on silicon surfaces .....	142
5.8.1 Generation of azide-terminated alkane monolayers on Si(111) .....	142
5.8.2 Generation of direct azide-terminated silicon surfaces .....	144
5.8.3 Stamping results on azide monolayers formed via hydrosilylation .....	146
5.8.4 Stamping results on direct azide-terminated silicon .....	148
5.9 Conclusions .....	151
5.10 References .....	152

## List of figures and tables

---

### Chapter 1

Table 1.1	Summary of nanoscale material challenges .....	4
-----------	--	---

### Chapter 2

Figure 2.1	The SNAP process .....	16
Figure 2.2.	Scanning electron micrographs of the SNAP SL and the Si NWs .....	17
Figure 2.3.	NW resistance normalized to the bulk-scaled resistance .....	18
Figure 2.4.	Boron concentration as a function of Si depth .....	22
Figure 2.5.	Doping levels of boron (p-type) and phosphorous (n-type) under various diffusion temperatures .....	24
Figure 2.6.	Scanning electron micrographs of Si NW arrays before and after surface treatment .....	27
Figure 2.7.	Scanning electron micrograph of EBL-patterned electrodes on NWs ..	28
Figure 2.8.	NW FET structure .....	29
Figure 2.9	Performance characteristics of Si NW FETs for different processing conditions and device configurations .....	32
Figure 2.10.	$I_{DS}$ - $V_{GS}$ curves with both top gate ( $V_{GS}$ ) and back gate ( $V_{BG}$ ) modulation .....	34
Figure 2.11.	High-performance, top-gated, p-type Si NW FETs .....	36
Figure 2.12.	Comparison of NW and $\mu$ W FET performance .....	39
Figure 2.13.	N-FET performance metrics .....	42

### Chapter 3

Figure 3.1.	Truth tables and logic symbols for the fundamental Boolean functions .....	50
Figure 3.2.	Schematic of pattern doping technique .....	53
Figure 3.3.	Scanning electron micrographs of surface damage from pattern doping .....	54

Figure 3.4.	Depiction of doping windows checkerboard pattern and the EFM technique .....	56
Figure 3.5.	EFM images of pattern doped substrate .....	58
Figure 3.6.	Diode curves from devices fabricated from patterned doped substrates .....	60
Figure 3.7.	IV characteristics of fabricated Si diode .....	61
Figure 3.8.	Pictures of SNAP alignment system .....	63
Figure 3.9.	Scanning electron micrographs of SNAP NWs dropped from the SNAP alignment system .....	64
Figure 3.10.	The NW inverter circuit .....	65
Figure 3.11.	Scanning electron micrograph of SNAP NWs at the interface of n- and p-type Si .....	66
Figure 3.12.	Example of the NW 2-bit full adder circuit .....	67
Figure 3.13.	Inverter performance metrics .....	69
Figure 3.14.	Demonstration of a NW XOR logic gate .....	70
 <b>Chapter 4</b>		
Figure 4.1.	Fabrication of NW large area device .....	79
Figure 4.2.	Representative DC data from a large-area p-type NW FET .....	80
Figure 4.3.	Representative capacitance data of NW FET devices .....	82
Figure 4.4.	Comparison of conventional MOSFET to buried-channel (BC) MOSFET structures .....	83
Figure 4.5.	Threshold and subthreshold characteristics of NW p-FET .....	84
Figure 4.6.	The format of the Device Exploration Workbench file .....	87
Figure 4.7.	Comparison of simulated and experimental device parameters .....	91
Figure 4.8.	DC simulation results of the inverter and XOR logic gates .....	93
Figure 4.9.	Simulated transient plot of inverter .....	95
Figure 4.10.	DC characteristics of simulated and experimental CS inverters .....	96
Figure 4.11.	Graphical representation of MEDICI modeled NW FET with overlaid grid points .....	98

Figure 4.12.	NW device potential contours for different gate biases .....	99
Figure 4.13.	Semilog plot of $I_{DS}$ versus $V_{GS}$ for MEDICI modeled n-FET with Ti gate metal and Pt gate metal .....	100
Figure 4.14.	Fabrication and characterization of improved n-FETs .....	101
Figure 4.15.	Input versus output voltage characteristics of fabricated CS inverter with Pt-gate n-FET .....	103
Figure 4.16.	Screen shot of DEW file .....	109
 <b>Chapter 5</b>		
Figure 5.1.	Schematic of microcontact printing .....	116
Figure 5.2.	Molecular structure of amphiphilic, bistable [2]rotaxane .....	118
Figure 5.3.	Schematic of proposed [2]rotaxane synthesis .....	120
Figure 5.4.	Molecular structures from the azido-terminated monolayers and the stamp inks: ferrocene alkyne and pentafluorophenylether alkyne .....	128
Figure 5.5.	Grazing angle IR spectra of azide-terminated and stamped surfaces ...	130
Figure 5.6.	XPS data of azide-, 3-, and 4-terminated surfaces .....	131
Figure 5.7.	FFM and fluorescence characterization of patterned surfaces .....	133
Figure 5.8.	Electrochemistry of 3 patterned using the <i>HomoCat</i> and <i>StampCat</i> methods .....	135
Figure 5.9.	Kinetics plot of the StampCat and HomoCat techniques with 3 .....	137
Figure 5.10.	Elucidating the mechanism of <i>StampCat</i> using electrochemistry .....	140
Figure 5.11.	Schematic of azide-terminated monolayer on Si via hydrosilylation of 1-chloro-11-undecene and subsequent substitution to the azide .....	143
Figure 5.12.	Schematic of synthesis of direct azide-termination on Si(111) .....	145
Figure 5.13.	XPS data for CuAAC reactions on azide-terminated surfaces made via hydrosilylation .....	147
Figure 5.14.	XP spectra of azide-terminated Si(111) surfaces .....	150
Table 5.1.	Contact Angle measurements for various modified Au surfaces .....	129