Chapter 3

Fabrication and characterization of nanowire logic circuits

3.1 Introduction

Complementary symmetry logic gates involve both p- and n-type transistors. Such logic gates outperform structures based upon pure p- or n-type technology with a key characteristic of low static power consumption, implying significant advantages for ever-denser circuit integration.[1] In fact, beginning in the early 1980s, there was a forced move from NMOS to complementary technology despite the increased fabrication complications. Today, a similar trend is occurring in the field of semiconducting nanowires (NWs). These promising building blocks for electronics are not dependent upon existing lithographic limitations.[2, 3] Si NWs, in particular, are appealing because they are relatively straightforward to prepare,[4, 5] the Si/SiO_2 interface is attractive, and Si NWs exhibit some compatibility with more traditional Si-based technologies.[6, 7] Si NW logic gates have been largely based upon p-FETs because they have been historically

more reliable to fabricate.[6, 8, 9] A few complementary NW devices have been reported, including p-type Si/n-type Si or GaN heterojunctions for diode logic,[10, 11] or carbon nanotube (CNT) based inverters.[12, 13] These systems are limited by both the stochastic chemical nature of the NW formation and doping and by the very challenging issues involving the assembly of devices into even the most basic circuits.[6, 10, 12, 14]

For NW electronics to have practical applications, both p- and n-type devices must be integrated onto the same substrate using a technique that is controllable, scalable, and that permits increasingly complex functionalities to be implemented. This chapter presents techniques for combining both p- and n-type Si NWs within a single, ultrahigh-density, highly aligned NW array. By combining traditional diffusion doping and lithographic techniques with the superlattice nanowire pattern transfer (SNAP) process,[15, 16] spatial control over the doping profiles can be achieved within a single NW or in adjacent NWs. Both n-type and p-type Si NW FETs can be co-prepared, and those FETs exhibit consistent and good performance metrics. These concepts are combined to demonstrate statistical numbers of a simple complementary logic circuit: a power-efficient Si NW inverter that exhibits voltage gain.

3.1.1. Overview of logic functions

The foundation of logic circuit operation is Boolean algebra. The Boolean algebraic equations are represented by logic gates. The NOT gate, which inverts the input signal, and either the AND or OR logic gate can be used to synthesize any Boolean alegebraic function (De Morgan's Laws).[17] The common logic functions also include the NAND, NOR, and XOR functions.

The most fundamental logic gate is the NOT function, or inverter. Its function is to invert the state of an input. The logic symbol and truth table appear in Figure 3.1. The CMOS inverter circuit is the most basic logic gate (consisting of 1 p-FET and 1 n-FET) and will be discussed further in this and the next chapter.

The AND and NAND gates are also fundamental logic gates. The AND gate will only output a **1** if both inputs are **1**. The NAND gate is the inverse of the AND gate. Similarly, the OR gate only outputs a **0** if the inputs are both **0** and the NOR is the inverse of the OR gate (see Figure 3.1 for the truth tables and the associated logic symbols). The CMOS AND/OR logic gates require 2 p-FETs and 2 n-FETs to operate and the NAND/NOR gates can be generated by coupling the AND/OR gate to the inverter. Lastly, the XOR, or exclusive OR gate, only outputs a **1** if the inputs are different. The XOR can be synthesized using the other fundamental logic gates and requires a minimum of 6 p-FETs and 6 n-FETs to implement for CMOS.

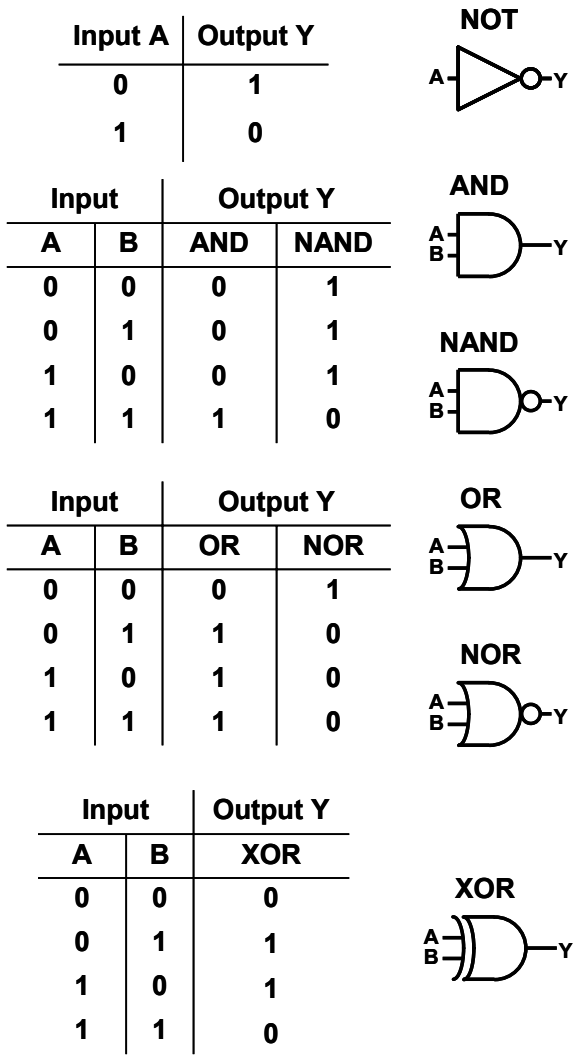

Figure 3.1. Truth tables and logic symbols for the fundamental Boolean functions

Complex logical operations, such as addition and multiplication, can be implemented by connecting these gates together to satisfy the correct Boolean algebraic equations. The level of complexity that can be achieved using these simple logic gates is staggering. For instance, current Intel microprocessors have 500–800 million transistors.[18] However, the implementation of these logic circuits from individual devices is not straightforward and requires the optimization of several performance metrics.

3.1.2 Overview of the chapter

The next section describes the development of a pattern doping technique that allowed for the side-by-side production of NW n- and p-FETs. These surfaces were characterized using electrostatic force microscopy and by measured I-V curves from fabricated diodes. Next, a SNAP master alignment system, which allowed for precise alignment of the SNAP-generated Pt NWs and the pattern-doped substrate, is described. Lastly, the fabrication of characterization of complementary inverters and other logic circuits are presented

3.2 Pattern doping technique

The realization of complementary symmetry (CS) logic circuits requires a method to fabricate adjacent n- and p-type NW FETs. The original method for fabricating SNAP-generated NW FETs involved a single doping step to dope the entire substrate (see Section 2.2.1). To pattern both n- and p-type regions on the same substrate, a pattern doping technique was developed to achieve spatial control over dopant profiles across a substrate. Once the substrate contains both n- and p-type regions, a SNAP master alignment system was implemented to pattern NWs over the desired regions with 1 μm precision. In this section, the development of the patterned doping technique is discussed. In the following sections, the characterization of the doped regions using electrostatic force microscopy (EFM) and by the I-V characteristics from fabricated diodes is discussed.

In order to achieve both n- and p-type regions on the same SOI region, a sequential diffusion doping process was implemented (Figure 3.1).[19] Intrinsic silicon-on-insulator (SOI) substrates (34 nm <100> Si on 250 nm oxide) (Simgui, Shanghai, China) were cleaned using the standard RCA process (see Section 2.2.1 for details). Alignment markers were first formed using photolithography and 20 nm Si evaporation, followed by thorough RCA cleaning. The substrates were then coated with a ~ 180 nm thick undoped spin-on-glass (SOG) film (Accuglass 214, Honey Electronic Materials, Sunnyvale, CA) followed by a photoresist bilayer consisting of a layer 3% PMMA (in chlorobenzene), spun at 4000 RPM for 30 seconds and baked at 130°C for 1 minute, and followed by 3612 (Shipley Corporation) spun on at 3000 RPM for 30 seconds (Figure 3.2i).

To define the p-type regions, windows were opened in the photoresist using optical lithography and the exposed SOG was removed by exposure to buffered oxide etch (BOE) (6:1 NH_4F:HF) (Figure 3.2ii). The etched regions were examined under an optical microscope after every 10 s exposure to monitor the etching process. The process was stopped when a slight undercut was observed which was typically after ~ 25s of etch time. If the etch process occurred too quickly to control, the BOE solution was diluted with DI H_2O.

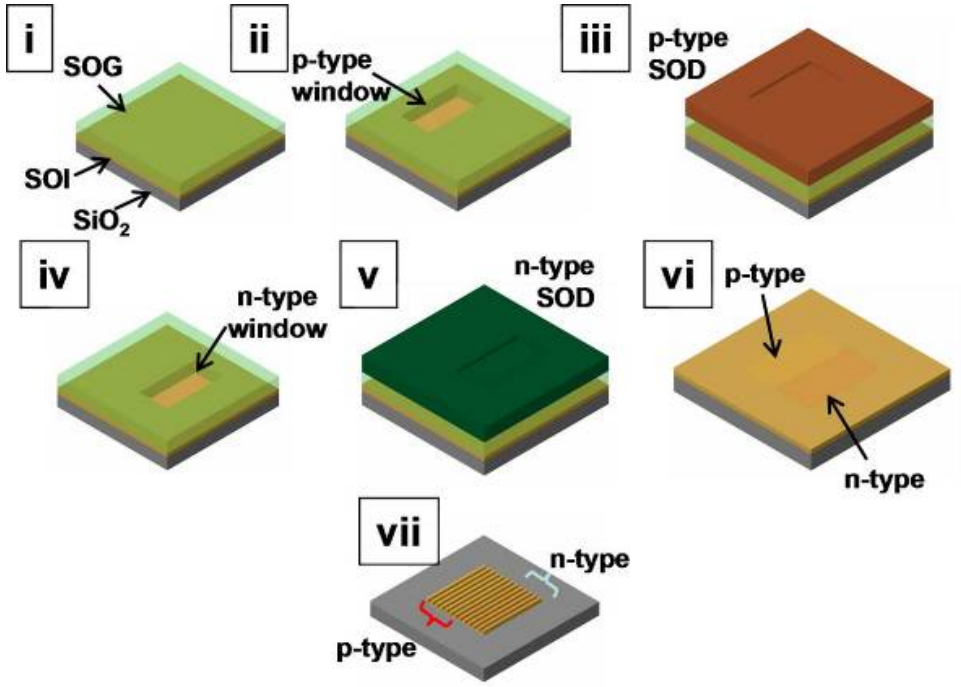

Figure 3.2. Schematic of pattern doping technique. **(i)** Undoped spin-on glass (SOG) is applied to SOI wafer. **(ii)** Electron beam or optical lithography is used to open windows in the SOG film. **(iii)** P-type SOD is applied on the SOG and the substrate is annealed. The only regions of the SOI substrate that are doped p-type are where the windows were patterned. **(iv–v)** The same process is repeated to pattern the n-type regions, resulting in a substrate containing both n- and p-type regions **(vi)**. **(vii)** Lastly, NWs are formed over the patterned doped areas.

The photoresist was then removed using an acetone soak and the p-type SOD (Boron A, Filmtronics, Inc., Butler, PA) was applied to the substrate (Figure 3.2iii). The film was annealed using rapid thermal processing (RTP). The dopants diffuse into the

SOI only where the SODs are directly in contact with the substrate. The SOG/SOD films were then removed using BOE, acetone, and DI H_2O in a process described in Section 2.2.1.

The substrate was cleaned using an additional RCA clean and the process was repeated to form the n-type doped regions, using n-type SODs (1:10 phosphorosilicafilm:CH_3OH, Emulsitone Company, Whippany, NJ) (Figure 3.2iv–v). The resulting substrate contained both n- and p-type regions (Figure 3.2vi). SNAP-generated NWs were patterned over the desired regions (Figure 3.2vii) to form n- and p-type NW FET channels.

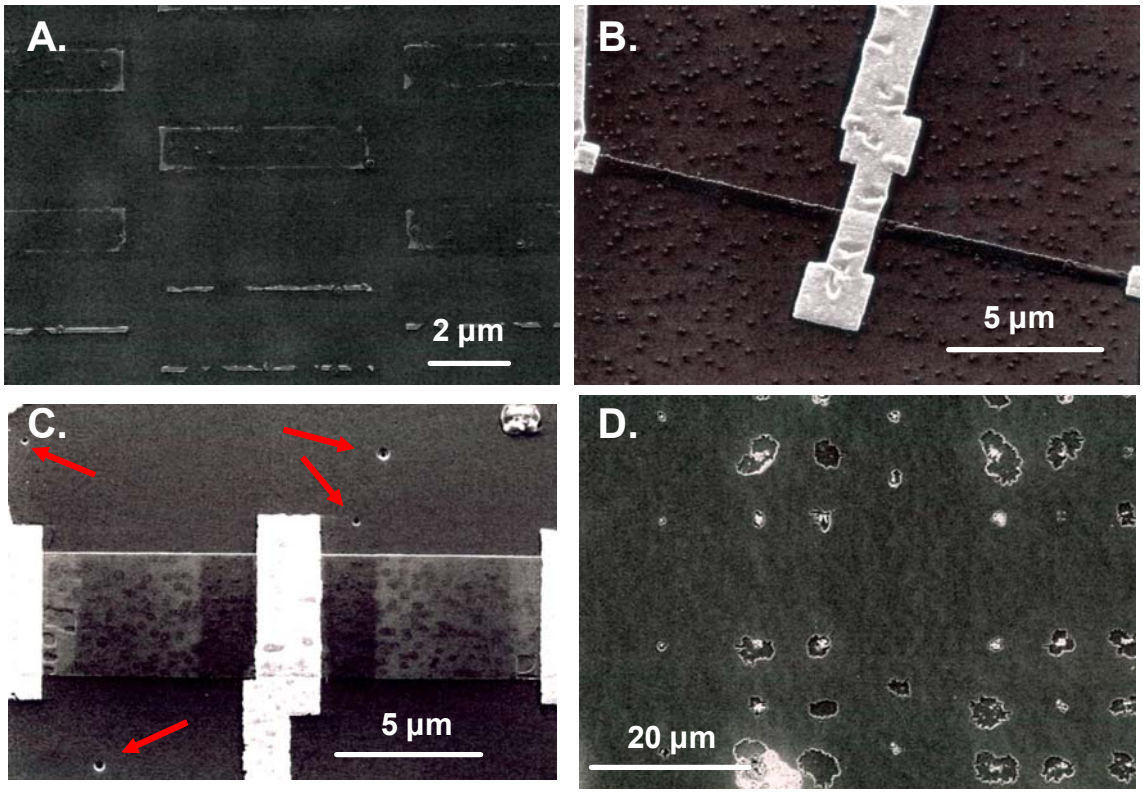

Figure 3.3. Scanning electron micrographs of surface damage from pattern doping. **A.** Reaction between the n- and p-type SODs lead to surface contamination. **B.** Bubbles suspended in the SOD can manifest as contamination on the surface, especially if there was no RCA cleaning. **C.** Etch pits in the underlying SiO_2 layer (denoted by red arrows) and a pitted texture on the Si epilayer can occur from BOE overetching. **D.** The reaction of the BOE with metal alignment markers causes severe etch pits on the surface.

The development of this process required several advancements. First, the use of an undoped SOG as a sacrificial layer was crucial. Studies were performed where n-type regions were patterned in a p-type SOD layer or vice versa. This scheme was attractive because it would only require a single annealing step. However, the n- and p-type SODs would react with each other during the anneal step, creating a contaminated surface that could not be cleaned (Figure 3.3A).

Next, the RCA cleaning process was important for reducing the contamination and Si etch pits on the devices. If contamination was present on the surface after the annealing step, inconsistent BOE etching occurred, leaving small contaminants (Figure 3.3B) or etch pits (Figure 3.2C) on the surface. If it took a significantly longer time than usual to render the surface hydrophobic with BOE, it was very likely that the surface was contaminated and that these microscopic defects would be present.

Lastly, the use of photolithography combined with Si alignment markers was important. Initially, metal alignment markers were used, which were easy to identify for EBL. However, during the BOE etching process, the BOE would react with the exposed metal markers, creating etch pits in the Si (Figure 3.3D). Etched trenches were also tested but were not compatible with the etching process and were not observable using scanning electron microscopy.

3.3 Electrostatic force microscopy characterization

Before NW devices were fabricated, the diffusion doping technique was characterized by electrostatic force microscopy (EFM) using a standard doping pattern consisting of dopant windows in a checkerboard pattern (Figure 3.4A).

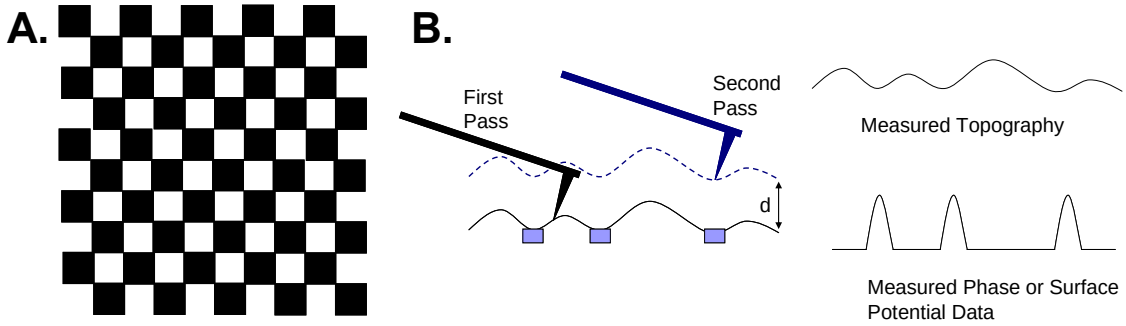

Figure 3.4. Depiction of doping windows checkerboard pattern and the EFM technique. **A.** Schematic of doping windows checkerboard pattern. The alternating black and white squares represents alternating areas of n- and p-type doping. **B.** Schematic of EFM technique. The cantilever scans over the surface twice. The first scan generates the topographical image (upper-right image) and the second scan, which is performed at a set distance, d, above the surface, produces the electric field gradient in response to electric fields (depicted as light blue boxes) on the surface.

EFM is a scanning probe technique, similar to tapping-mode atomic force microscopy (AFM), which allows the mapping of electric field gradients above a sample. The technique uses two scan passes per line (a trace and retrace) to record both topology and the force gradients. First, the scanning probe cantilever scans across the surface while oscillating at the probe tip's resonant frequency. Once the probe reaches the end of the scan, it lifts up by a set distance, d, and retraces the scan line, following the recorded topology (Figure 3.4B). On this retrace step, a voltage is applied across the tip to make it more sensitive to surface electric fields. If the tip is attracted to the surface due to electrostatic interactions, the cantilever resonance frequency will reduce. Conversely, a repulsive interaction will increase the cantilever resonance frequency. The phase shifts

can then be mapped into a two-dimensional image to illustrate the electric field gradients on a surface. EFM is a powerful technique for simultaneously probing the morphology and the electrical characteristics of surfaces, and has been used to explore interesting phenomena in organic heterojunction solar cells,[20] molecular films,[21, 22] nanoscale devices,[23] and semiconductor device failure.[24]

To study the fidelity of the pattern doping technique, a checkerboard pattern of alternating n- and p-type regions was formed on SOI substrates (Figure 3.4A). These checkerboard patterns were originally generated using EBL and PMMA resist. Various sized squares were patterned with areas ranging from 36 μm^2 to 1 μm^2. Once these samples were generated, they were characterized using a Multimode Nanoscope IIIA (Veeco Instruments, Santa Barbara) atomic force microscope and a Nanoscope Extender^{TM} electronics module. The module allowed for phase detection, which improves the instrument's sensitivity to the surface's electric fields. Pt/Ir-coated tapping-mode etched Si probes were used (SCM-PIT from Veeco Instruments). The Pt/Ir coating provides an electrical path from the cantilever to the apex of the tip, which is necessary to provide a DC bias on the probe tip. The AFM hardware and software was configured for phase detection EFM measurements as described in the user's manual.[25]

The topology and associated EFM image of a checkerboard pattern consisting of 3 μm squares is shown in Figure 3.5A and 3.5B. The n-type regions were doped 3×10^{17} cm^{-3} and the p-type regions were doped 9×10^{17} cm^{-3}. The topography image reveals a surface with ~ 5 nm average height variation but no obvious checkerboard pattern. The associated EFM image was taken by a 5 V biased tip lifted 20 nm off of the surface. The scan rate was 0.5 Hz and 512 scans lines were taken per image. Here, the n-type regions

appear darker than the p-type regions due to the differing phase shifts of each region. The n- and p-type squares are not uniform due to overetching of the p-type windows during the lithography steps. The phase shift between the n- and p-type regions was approximately 4°.

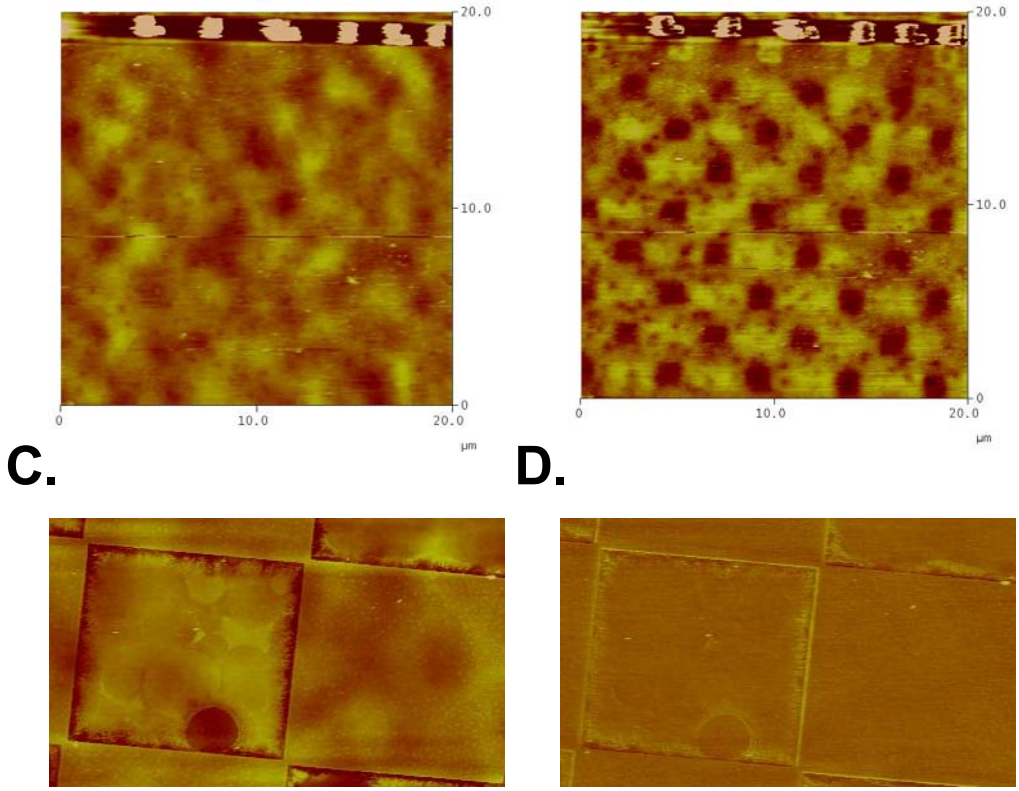

Figure 3.5. EFM images of pattern doped substrate. **A.** Topography image of SOI substrate doped with a checkerboard pattern of 3 μm^2 squares. **B.** EFM image of same area, showing the alternating squares. The darker regions represent the n-type regions and the lighter regions are doped p-type. **C.** Close-up of a topography image of a "control" checkerboard, where the squares are undoped but etched to form topographical variations. **D.** EFM image of the same area, showing negligible phase shifts within each square

A control sample was also characterized with EFM to ensure that the EFM signal was not due to slight changes in the topography (vertical overetching of the n- or p-type regions). A checkerboard pattern was made where alternating squares were etched into undoped Si (Figure 3.5C). The average height variation was ~ 10 nm. The associated EFM image (Figure 3.5D) shows no variation in the phase shift between adjacent

squares. The phase does change at the interface at each square, which is typical in EFM. This is due to the fact that sharp features on a surface concentrate the local force gradient.

The EFM technique allows for the characterization of the Si surface prior to device formation. Since NW devices require the Si epilayer of an SOI wafer to be removed, this technique is the best method for seeing the entire doping pattern and also to easily characterize issues such as SOG overetching.

3.4 Diode fabrication and characterization

To characterize the interface between n- and p-doped regions, thin film diodes were fabricated. The devices consisted of a 0.5 μm x 2.5 μm wire patterned using EBL. At the center of the wire was a pn junction. Fifty-four devices were fabricated and approximately half showed rectification. The device structure and representative pn junction curves are presented in Figure 3.6. The first I-V curve is from a diode biased from the electrode contacting the n-type side (Figure 3.6C) and the second curve is another device biased from the electrode contacting the p-type side (Figure 3.6D). Both curves show the correct rectifying behavior.

A semilog plot of the absolute value of the current versus voltage for the first curve shown in Figure 3.7A indicates correct diode characteristics.[26] Four regions of the semilog plot are labeled A–D and can be related to typical diode behavior: (A) generation-recombination current; (B) diffusion current; (C) high-injection coupled to

series resistance effects; and (D) reverse bias (breakdown not observed). The minima are shifted from zero volts due to miscalibration of the IV software. The curve shape and measurement repeatability provides evidence that the sharp change in current is due to the device turning on and not breakdown.

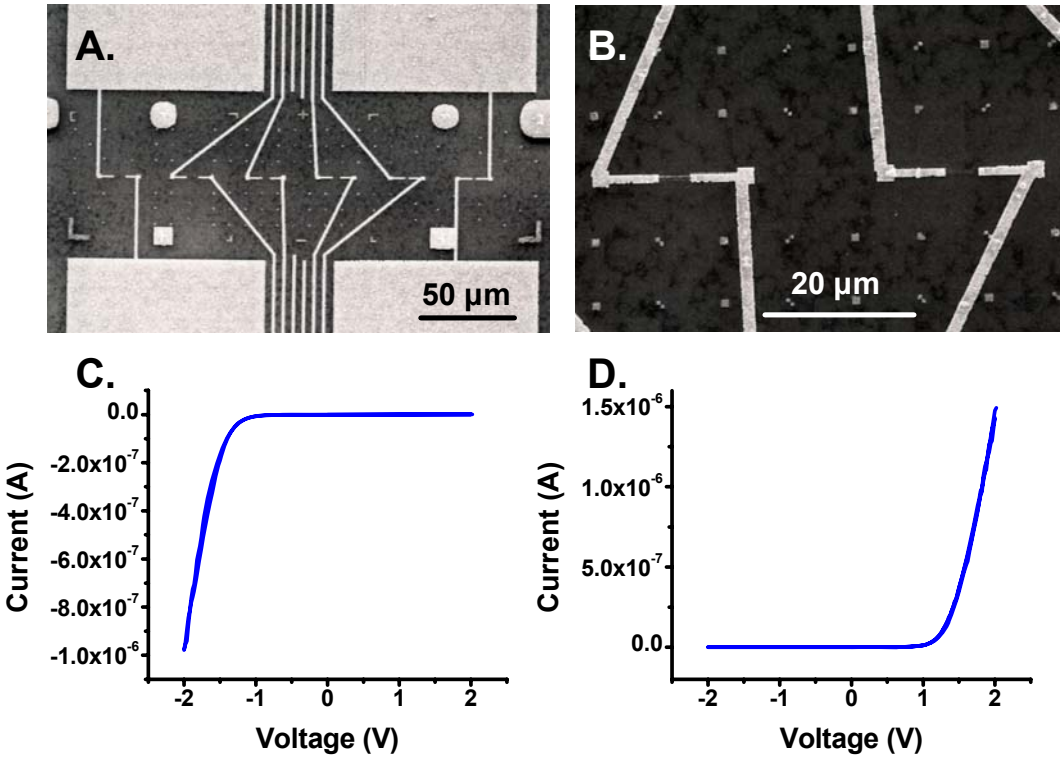

Figure 3.6. Diode curves from devices fabricated from patterned doped substrates. **A.** Diode biased from n-type side. **B.** Diode biased from p-type side.

The semilog plot can be used to perform simple device modeling. Diode behavior can be modeled using the ideal diode equation:[26]

$$I = I_S\left(e^{\frac{qV}{nkT}} - 1\right) \tag{3.1}$$

where I_S is the generation current and n is the ideality factor. The ideal diode equation assumes several conditions: (1) an abrupt depletion layer, (2) that the Boltzmann approximation is valid within the depletion layer, (3) low minority carrier injection, and

(4) no generation current within the depletion layer. Therefore, the ideal diode equation would match the slope of region B in the semilog plot.

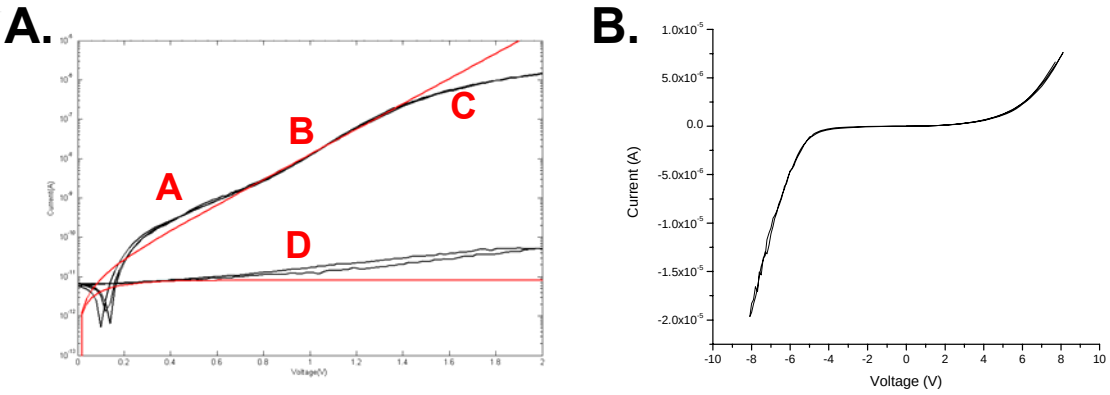

Figure 3.7. IV characteristics of fabricated Si diode. **A.** Semilog plot of IV characteristics of diode with ideal diode equation fitted to the slope in region B. **B.** IV characteristics of diode showing rectifying behavior in the +V direction and diode breakdown in the –V direction.

The fitted plot is shown in red over the semilog plot in Figure 3.7A. The ideality factor n equals 2 in ideal diodes where the diffusion current dominates. For the measured device, n = 5.2. Deviations from the ideality factor are due to surface leakage current, generation/recombination of carriers within the depletion layer, carriers tunneling through the bandgap, high-injection of minority carriers at low forward bias, and/or series resistance. Therefore, the ideal diode equation only gives qualitative agreement for actual silicon diodes. However, because the semilog curve shape matches the shape for typical silicon diodes and the ideality factor is within the same order of magnitude for ideal diodes, the devices are exhibiting normal diode behavior. Figure 3.7B shows a device with a positive turn-on voltage and a breakdown event (indicated by a sharper slope) at high negative voltage, also indicating correct device behavior.

3.5 SNAP nanowire alignment system

In order to produce logic circuits from pattern doped surfaces, it was essential to develop a method to align the SNAP Pt NWs over the appropriate region. Originally, the SNAP masters were placed on the wafer manually, using tweezers. This method was sufficient for homogeneous doped samples. For samples containing pattern doping or existing features (alignment markers, other devices, etc), a high control over the placement of the NWs to within a few μm becomes necessary. Therefore, an SNAP NW alignment system was built and is described here.

The basic concept of the SNAP alignment system is that both the substrate and the SNAP master are aligned to a stationary reference point (in this case, a specific point on a reticle that is projected on a monitor). Photos of the alignment system with individual components labeled are shown in Figure 3.8. The substrate is aligned by positioning it so that the vertical reticle line (Figure 3.8B) is aligned to the appropriate alignment markers on the surface. The SNAP master is affixed to a custom designed holder (Figure 3.8G) using simple suction and brought 0.5–1 mm over the substrate. On the top of the SNAP master holder is a lithographically patterned grid. The holder is moved until the vertical and horizontal reticle lines are aligned to a specific grid point, as determined by calibrations. Both the SNAP master holder and the substrate platform can be moved independently in the x, y, z, and θ directions using high-quality optical stages. The suction is released and the SNAP master drops onto the substrate, which is coated in epoxy. The heat stage (Figure 3.8E) is turned on and the epoxy is heat-cured. At this point, the substrate can be removed from the alignment system.

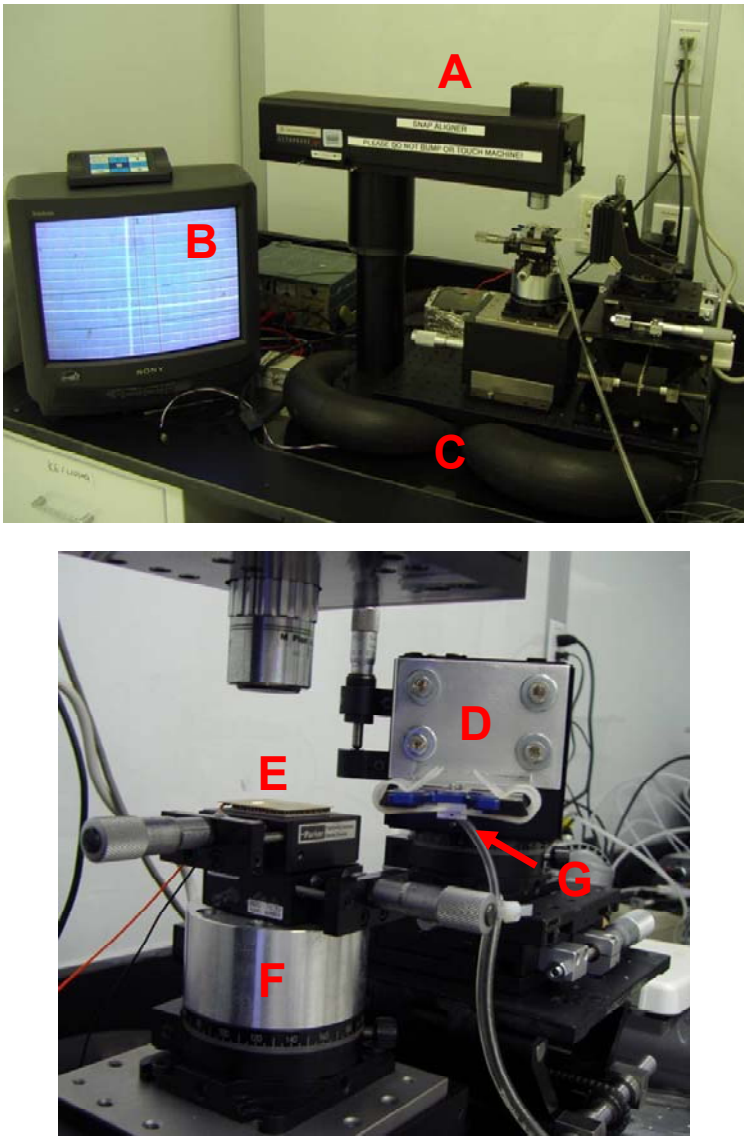

Figure 3.8. Pictures of SNAP alignment system. Individual components are labeled A–G. **A.** Microscope system with 200× objective with a working distance of ~ 0.5 inches. **B.** Monitor that displays the microscope view with a reticle overlay. **C.** Alignment system is attached to an optics board that is placed on 4 inflated inner tubes. The inner tubes suppress room vibrations. **D.** Arm that holds SNAP master holder. It can be moved in the x,y,z, and θ directions using optics stages. **E.** Substrate platform. The platform is a heat stage so that epoxy on the substrate can be heat-cured after the SNAP masters are placed on the surface. **F.** The substrate holder sits on three optics stages, which can move it in the x,y,z, and θ directions. **G.** The SNAP master holder. It holds the SNAP master by suction until it is properly aligned over the substrate. A fine grid is lithographically patterned on the top of the holder. To align the SNAP master and the substrate to each other, the reticle is first aligned to the appropriate alignment markers on the substrate. The SNAP master holder is brought over the substrate and is also aligned to the reticle.

Once the alignment system was built, it was tested for accuracy. 15 μm metal target squares were patterned onto Si substrates, flanked by two 5 × 5 μm alignment markers. The center of each alignment marker was positioned on the correct reticle line. Figure 3.9A and 3.9B show the results of one SNAP NW transfer. The alignment of the NWs was accurate to within 1 μm on several samples.

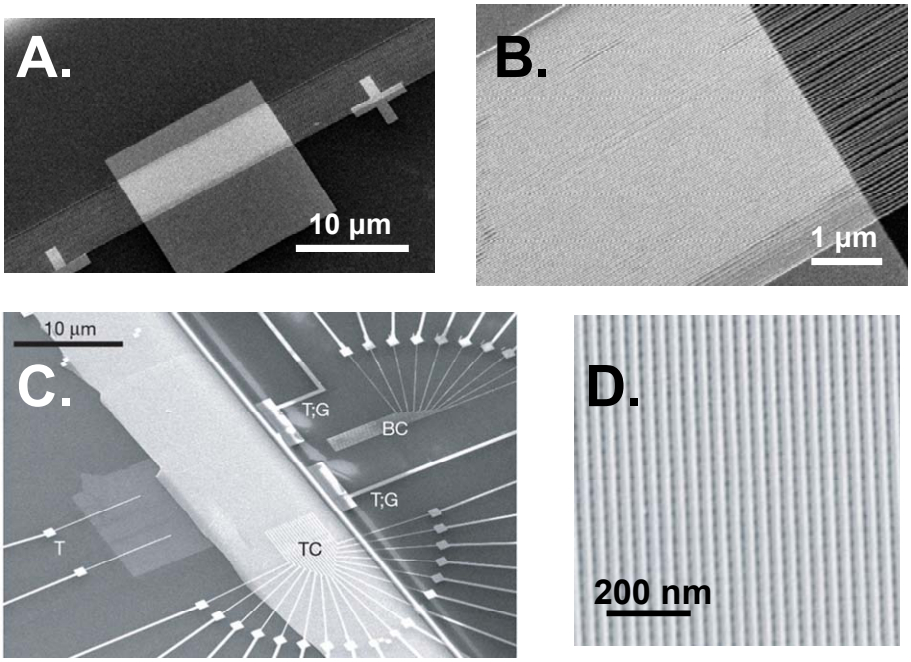

Figure 3.9. Scanning electron micrographs of SNAP NWs dropped from the SNAP alignment system. **A.** SNAP NWs on the target square. The cross-shaped alignment markers were used to line up the reticle. **B.** Close-up of the NWs on target. **C.** A 160 kbit crossbar array memory circuit patterned at 10^{11} bits/cm^2 using two sets of NW arrays. The top plane of NWs were dropped using the alignment system. **D.** Close-up of the SNAP NW crossbar array.

In addition to being used for the logic circuit fabrication, this alignment system was also an enabling technology for the development of a 160 kbit molecular memory circuit patterned at 10^{11} bits/cm^2 (Figure 3.9C).[27] This architecture density was achieved by overlapping two sets of perpendicular SNAP NW arrays, forming a crossbar array (Figure 3.9D). Without the development of the alignment system, the formation of NW circuits would have been significantly more difficult.

3.6 Nanowire logic circuit fabrication

Once the pattern doping process was optimized and the SNAP alignment system was completed, the NW logic circuit fabrication process could be developed. First, new Ti/Pt alignment markers were patterned around the NW array. The Si alignment markers from the pattern doping were used to map out the patterned doped regions on the NW array. As for single devices (see Section 2.2.3), the continuous NW array was divided into discrete sections. Next, Ti/Pt input and output wires were patterned using EBL, using the map of the doped areas to guide the placement of the n- and p-FETs. The Al_2O_3/Ti/Pt top gates were fabricated and the circuits were ready to characterize. The circuits were tested in a probe stations using three Keithley 2400 SourceMeters and custom LabVIEW software.

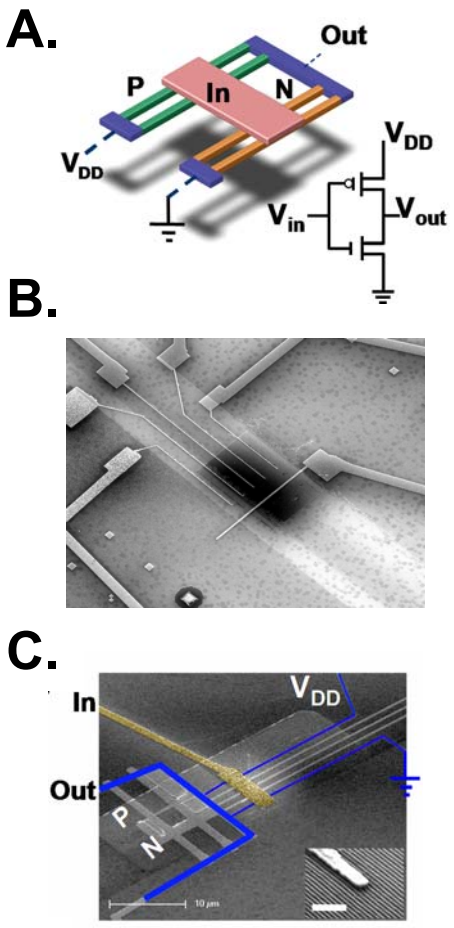

Figure 3.10. The NW inverter circuit. **A**. Schematic of the NW inverter circuit. **B.** Scanning electron micrograph of NWs with EBL-patterned power supply and output wires. **C.** Micrograph of completed inverter circuit with top gate supplying input signal

Figure 3.10 shows the schematic and the scanning electron micrographs of a complementary inverter circuit patterned from a SNAP NW array. A complementary inverter involves a p-FET and n-FET in series (see the circuit diagram in Figure 3.10A), with a shared gate as the input and a shared contact

as the output. The advantage of the complementary symmetry architecture is that there is minimal current flowing from the power supply (V_{DD}) to the ground, whether the input is high (the p-FET is "off") or low (the n-FET is "off"). Therefore, the power consumption is minimized, which is why complementary logic gates comprise an important component in modern digital technology.

During the circuit fabrication, it was interesting to observe that the n- and p-type NWs were distinguishable using scanning electron microscopy. Figure 3.11 shows a micrograph of the NWs at the interface of n- and p-type regions. The p-type NWs appear brighter than the n-type NWs. This is due to the difference in the Fermi energies of the p- and n-type materials. Although the contrast was noticeable, it was still necessary to explore the pattern doping quality using EFM and to carefully map the pattern doped areas using the doping alignment markers.

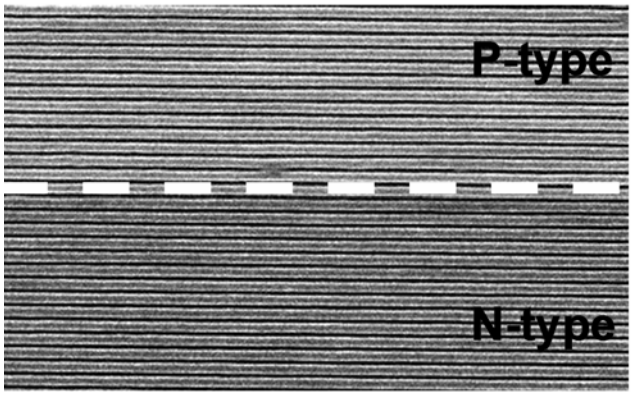

Figure 3.11. Scanning electron micrograph of SNAP NWs at the interface of n- and p-type Si

Prototypes of more complex logic functions were also fabricated, although not electrically characterized, in order to understand the fabrication challenges associated with integrating several n- and p-type FETs. These circuits utilized a design feature called monolithic contacts.[28] Monolithic contacts are formed by patterning Pt microwire contacts by EBL prior to the NW transfer into Si. The NWs, along with the patterned microwires, are transferred in the Si epilayer simultaneously to form both NWs and Si

bars. These bars are then used to route signals to the NWs, analogous to standard metal microwire contacts. The strength of this technique is that the monolithic contacts eliminate any issue of contact resistance to the NWs. The metal contact pads are ohmically contacted to the monolithic contacts, which are large and typically highly doped.

Figure 3.12A shows a scanning electron micrograph of a NW full adder circuit consisting of 14 n-FETs and 14-FETs. The monolithic contacts appear as the dark microwires in the image and the metal top gate. The interface between the NWs, the monolithic contacts and the metal contacts are shown in Figure 3.12B.

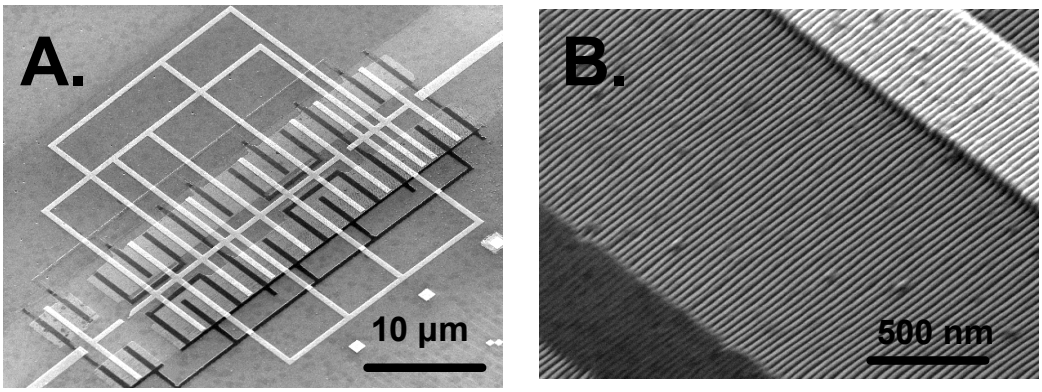

Figure 3.12. Example of the NW 2-bit full adder circuit consisting of 28 NW FETs. **A.** Scanning electron micrograph of adder circuit. The bright microwires are patterned using Ti/Pt and the dark microwires are monolithic contacts. **B.** Close-up of NWs showing comparison of monolithic wire and metal wire

Although these circuits were not tested, their fabrication was a useful exercise for learning more about the fabrication processes involved for complex circuits.[28]

3.7 DC characterization of fabricated FETs and circuits

Several complementary inverter circuits were fabricated and characterized. For the measured inverters, the contact electrode width was 150 nm (which contacted 4–5 Si NWs) and the channel length was 2 μm. P- and n-FETs were first characterized separately (Figure 3.13A). This step helped determine the appropriate power supply voltage (V_{DD}) and the input signal range. For all of the inverters measured in this study, $V_{DD} = 3$ V. Under this condition, both p- and n-FETs are saturated and show symmetrical performance. The input versus output of the inverter is plotted in Figure 3.13B: when the input is low, the output is high, and vice versa. Therefore, a "NOT" logic gate is achieved.

The gain of the inverter, which is defined as the maximum slope during the transition between the output low and output high levels, characterizes the noise margins of the circuit. This yields a metric for how robust the circuit is to signal variation. A gain greater than unity is a minimum requirement and a high gain is desired. The gain can be obtained by taking the first-order derivative of the input/output plot and the result is shown in Figure 3.13C. Out of the 7 devices measured, a gain of ~ 5 was consistently obtained (Figure 3.13D), further suggestive of uniformly performing p- and n-FETs.

In Chapter 4, the optimization of the inverter circuit using device and circuit simulations is discussed and provides more in-depth information about the relevant performance metrics.

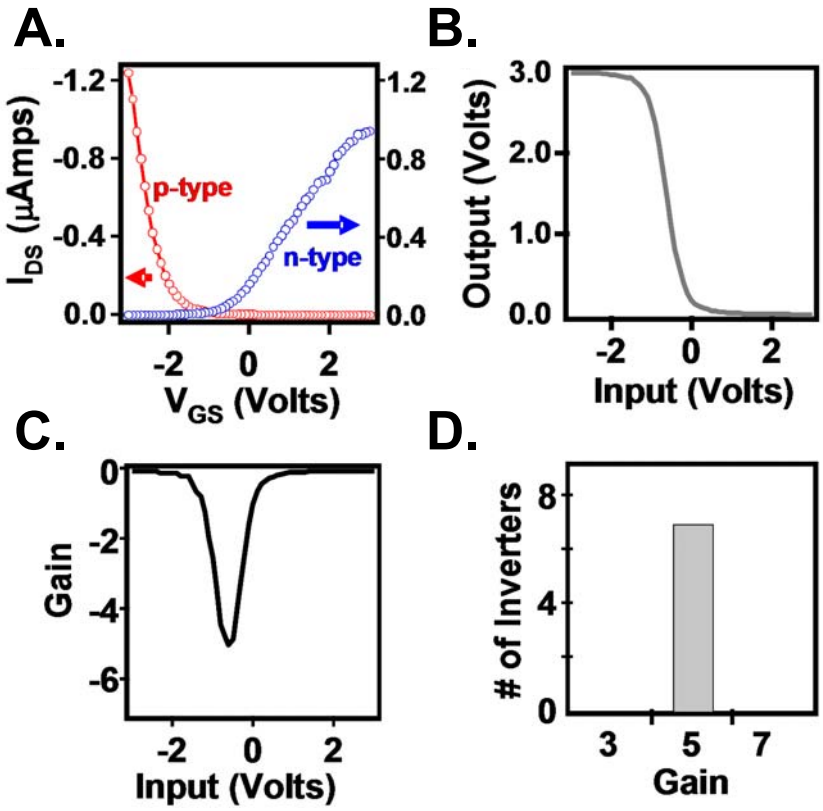

Figure 3.13. Inverter performance metrics. **A.** I-V_{GS} characteristics of p- and n-FETs in the same array. V_{DS}=- 1.5 V for p- and + 1.5 V for n-FETs. **B.** Output versus input signal of the complementary NW inverter. **C.** The gain of the inverter versus input. **F.** Histogram of the gain of 7 measured inverters

3.7.1 Demonstrations of other logic gates

Since the development of the inverter circuit, the rest of the basic logic gates have been fabricated and tested by a colleague.[29] This was a significant achievement since it required several NW FETs to have consistent performance. These circuits were enabled by the SNAP, the in-plane routing, and the pattern doping techniques developed in this chapter.

Figure 3.14 shows a demonstration of a NW XOR circuit, which required 6 n-FETs and 6 p-FETs. Two NW CS inverters are first utilized to create complementary

inputs $\overline{A}$ and $\overline{B}$ from inputs A and B. All four of these logic values are then utilized to drive a circuit of 8 NW FETs, with each input utilized to drive a p-FET and an n-FET.

When all 12 FETs operated consistently, a functional XOR gate was achieved.[29] This circuit utilized the in-plane routing technique, which allowed for the construction of highly doped, NW-to-NW signal routing pathways within the same single-crystal Si epilayer from which the NWs are formed. Without this nanofabrication advancement, it is unlikely that the NW CS XOR gate would have achieved full signal restoration.

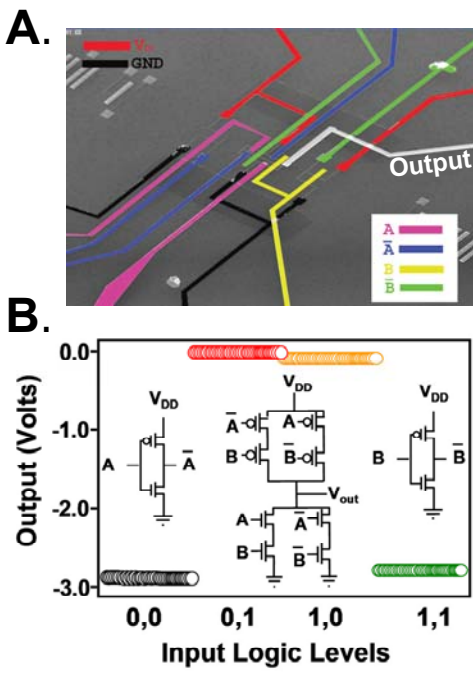

Figure 3.14. Demonstration of a NW XOR logic gate. **A.** SEM of XOR gate. **B.** Output versus input of XOR gate, reproducing the correct truth table.

The yield of working n- and p-FETs was likely near 100%. However, the requirement that the NW n- and p-FETs be well matched with each other so that a CS logic gate exhibits full signal restoration is a very stringent one. 15 XOR gates were tested and it was found that only 5 exhibited full signal restoration. If a single NW FET performed out-of-range within an XOR gate, the XOR gate would fail. This is likely the dominant failure mode. There were 180 FETs tested in the 15 XOR gates, and the 33% yield in XOR gates implies an approximately 93% yield in working and matched FETs.

3.8 Conclusions

Spatially selective doping and a SNAP alignment system were developed, and this allowed for the fabrication of both p- and n-type devices within a single, ultra-high-density Si NW array. The pattern doping method was characterized using electrostatic force microscopy and by characterizing fabricated pn diodes. Complementary Si NW inverters were constructed and demonstrated to exhibit uniform performance. This laid the foundation to generate the other Boolean logic functions.

3.9 References

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