Chapter 2

High-performance nanowire field-effect transistors

2.1 Introduction

Semiconductor nanowires (NWs)[1, 2] have attracted significant interest because of their potential for a variety of different applications, including logic and memory circuitry, photonics devices, and chemical and biomolecular sensors.[3–6] Although many different types of semiconductor NW have been investigated, silicon NWs have become prototypical nanowires because they can be readily prepared, the Si/SiO_2 interface is chemically stable, and Si NWs are utilized in a number of device demonstrations that have well-known silicon-technology-based counterparts.[3, 7, 8] Various techniques have been developed to synthesize semiconductor NWs, including the materials method known as vapor-liquid-solid (VLS) growth,[3, 7] and the templating method known as superlattice nanowire pattern transfer (SNAP).[9, 10] Each method has its advantages. The VLS technique can produce bulk quantities of semiconductor NWs, but those NWs are

characterized by a distribution of lengths and diameters, and they also must be assembled into the appropriate device structure (or the device structure must be constructed around the nanowire[11]). However, VLS NWs may be prepared with various doping configurations,[12] and they may be studied on a variety of different substrates.[13]

The SNAP process, which will be described in detail in the next section, can be applied to the production of both metal and semiconductor NWs. Those NWs are characterized by extremely narrow width distributions, they can possess aspect ratios of up to 10^6, and they are prepared as highly defined arrays with near atomic control over NW width and pitch.[9, 10] In addition, the growth of VLS Si NWs relies upon a metal particle to seed the growth, and that particle can also serve as an impurity dopant.[7] SNAP Si NWs, by contrast, are prepared from thin film materials, and so the purity of the NW is limited only by the purity of the thin film. In any case, the ultimate test of the quality of a NW is based upon its electronic properties. For VLS Si NWs, field effect transistors (FETs) with high mobilities and low subthreshold swings have been reported.[8, 13] The DC transport characteristics of heavily doped SNAP Si NWs have been reported, and those wires exhibited bulk-like conductivity characteristics.[14] A key toward achieving that result was the use of spin-on-dopants (SODs). SODs, which have found uses in devices such as thin film transistors,[15, 16] provides a means for controlling doping levels while avoiding the damage that can occur through alternative methods, such as ion implantation.

In this chapter, the doping and fabrication processes were optimized for the production of SNAP Si NW FETs. P-type FETs exhibited high carrier mobilities, high on-current, excellent on/off ratios, and a low subthreshold swing of hole carriers. N-type

FETs showed consistent performance and also exhibited good performance metrics. These results reveal that the SNAP Si NWs have low defects, low surface and interface states, and can operate as high-performance FETs.

2.1.1 The SNAP technique

The key enabling technology for high-performance nanowire logic is the superlattice nanowire pattern transfer (SNAP) technique developed by Melosh et al. in 2003.[9] In this technique, Si NWs are formed from silicon-on-insulator (SOI) substrates using a template-mediated, top-down fabrication process. In this section, the process for generating SNAP NWs is qualitatively described and the full experimental details appear in Section 2.2.2.

First, superlattices (SLs) consisting of alternating GaAs and $Al_xGa_{(1-x)}As$ layers are grown via molecular-beam epitaxy (MBE). The SL wafer is carefully cleaved to form an atomically flat edge. The SLs are then diced into small pieces called "masters" (Figure 2.1A). Each master is carefully cleaned to remove any dust particles from the cleaved edge and then immersed in an etch solution that selectively etches back the $Al_xGa_{(1-x)}As$ layers, leaving behind GaAs ridges (Figures 2.1B, 2.2A, and 2.2B). Metal is then anisotropically deposited onto the cleaved edge of the master, forming metal NWs along the GaAs ridges (Figure 2.1C). The SL containing the metal NWs are transferred onto the SOI substrate and adhered via an epoxy layer (Figure 2.1D). The SL is removed using a chemical etch process, leaving behind the metal NWs on the substrate (Figure 2.1E). The metal NWs act as a physical etch mask and the pattern is transferred into the Si epilayer using a reaction-ion-etching process (Figure 2.1F). Lastly, the metal NWs are

removed by dissolving them in acid. The resulting substrate consists of Si NWs on an insulating layer (Figure 2.2C and 2.2D).

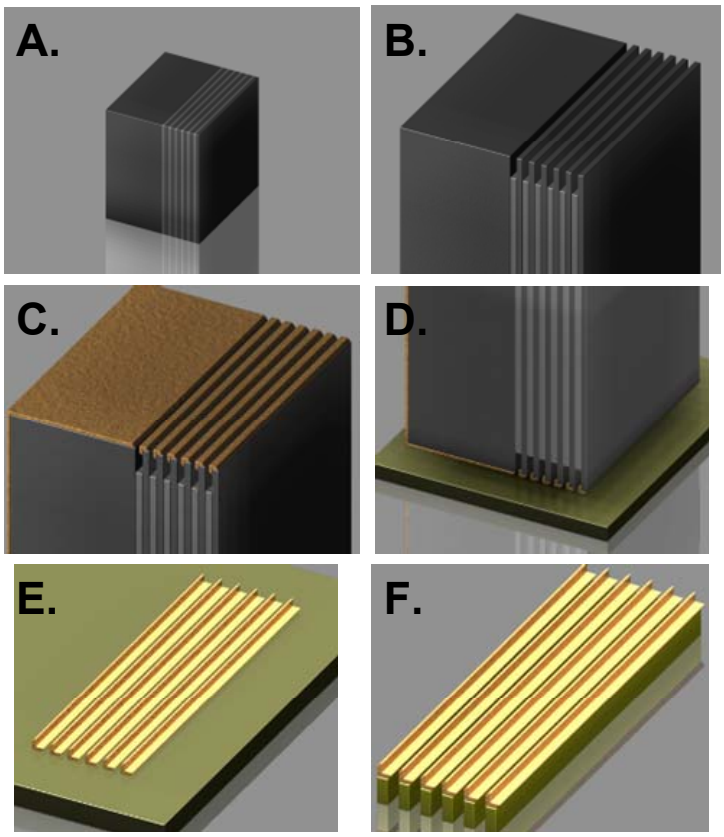

Figure 2.1. The SNAP process. **A.** First, the MBE-grown superlattice (SL) is cleaved, exposing the alternating GaAs/$Al_xGa_{(1-x)}As$ layers. **B.** Next, $Al_xGa_{(1-x)}As$ layers are selectively etched, leaving behind GaAs ridges. **C.** Metal is then anisotropically deposited onto the surface of the SL, forming metal NWs on the GaAs ridges. **D.** The metallized surface of the SL is then put in contact with an SOI substrate. **E.** The metal NWs are transferred using a wet-etch process. **F.** The NW pattern is transferred into the underlying Si epilayer using a reactive-ion etch and the metal NWs are removed

Metal and semiconducting NWs have been generated using this technique with NW widths and full-width pitches down to 8 nm and 16 nm, respectively.[9] Each NW can be as long as several millimeters. Arrays of up to 1400 NWs have been fabricated, however, SLs that generated 400 NW arrays with a 33 nm pitch were used for all of the devices in this thesis. The key strength of this technique is that the formation and the alignment of the NWs occur in a single step. Other methods of non-lithographic NW

formation (such as VLS) require a separate alignment step that all but precludes the fabrication of ordered, highly dense arrays. Another key advantage to this technique is that NW doping can be performed by doping the SOI substrate prior to NW formation. Additional details are discussed in the following section.

Si NWs produced by the SNAP technique have been used in several applications beyond logic circuits, including crossbar molecular memory circuits,[17] a binary-tree demultiplexing scheme,[10] biomolecular[18] and chemical[19] sensors, thermoelectrics,[20, 21] and superconductivity studies.[22] They are currently being used for novel photovoltaic applications.

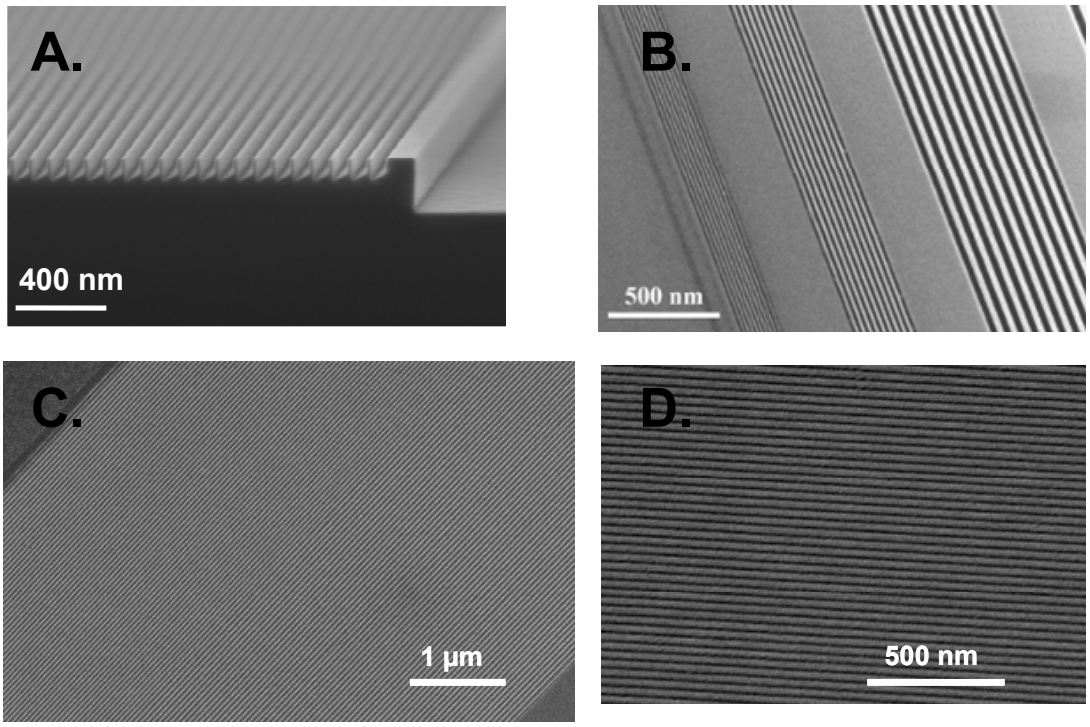

Figure 2.2. Scanning electron micrographs of the SNAP SL and the Si NWs. **A.** Side view of an etched SNAP master. **B.** Top view, highlighting the control over NW width and pitch. **C.** 128 Si NW array produced using the SNAP technique. **D.** Close-up of a 400 Si NW array

2.1.2 Conducting Si nanowire arrays

To fully utilize the SNAP-generated Si NW arrays, it is necessary that they have conductivity comparable to bulk Si. In 2004, Beckman et al. investigated optimizing the choice of substrate, substrate doping, and NW etching steps to maximize NW conductivity.[14] First, the choice of substrate proved to be a critical factor. Si NWs were produced from 4- and 8-inch SIMOX SOI wafers and their conductivities were compared to NWs produced from a high-quality MBE-grown wafer containing a p-type Si epilayer. 10 to 20 nm wide NWs were formed from each substrate using the same fabrication process. Figure 2.3 shows the NW resistance normalized to the bulk-scaled resistance for each substrate.

The 8 inch SOI wafer, which is more commonly used in the semiconductor industry, was shown to match the performance of the NWs generated from the MBE-grown substrate, which had bulk-like conductivity.

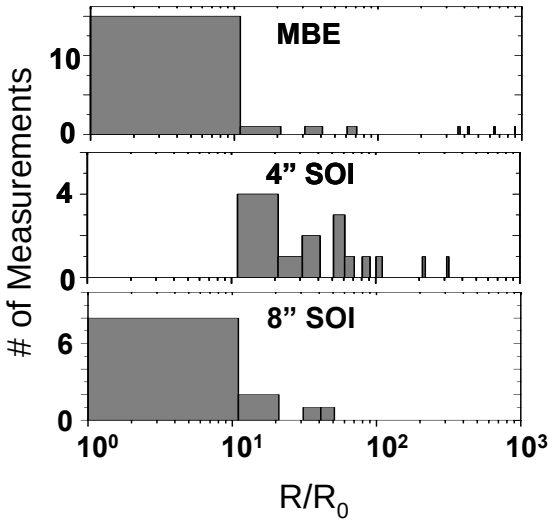

Figure 2.3. NW resistance normalized to the bulk-scaled resistance for NWs formed on 4- and 8-inch SIMOX SOI wafers and on an MBE-grown wafer

An additional factor that contributed to achieving bulk-like conductivity in SNAP-generated NWs was the method used to dope the substrate. Commercially available ion-implanted wafers produced NWs with degraded conductivity when their widths were below 50 nm. This conductivity improved substantially by utilizing diffusion doping. It is hypothesized that ion implantation causes irreversible damage to the Si epilayer lattice, which directly influences carrier transport in nanoscale devices.

Lastly, it was determined that the method to etch the Si NWs was important for maintaining high conductivity. As described in the previous section, reactive-ion etching is employed to transfer the metal NW pattern into the Si epilayer. A RIE system utilizing a high-frequency power supply enables stable plasma formation at low DC bias. This was shown to produce smooth NW sidewalls with no noticeable undercut. The optimizations done for this paper were a key foundation for producing high-performance nanowire transistors and, later, logic circuits.

2.1.3 Organization of the chapter

The next section describes the full fabrication process for the NW FETs. Details are provided on the diffusion doping, SNAP, and device fabrication processes. This information is also used as the foundation for the circuits discussed in Chapters 3 and 4. Next, the results of the p-FET characterization are discussed. Transistor metrics such as mobility and subthreshold swing are defined and calculated for several devices, and the role of surface states on device performance is explored. Lastly, the performance characteristics of NW n-FETS are discussed. The n-FETs did not perform as well as their p-FET counterparts but exhibited consistent performance. A side-by-side comparison of nanowires and microwires was done to determine the cause of this behavior discrepancy.

2.2 Nanowire field-effect transistor fabrication

The fabrication of high-performance Si NW field-effect transistors (FETs) is described in this section. Although FETs using SNAP NWs as the channel material had been previously demonstrated,[10, 14] these devices were not optimized for performance or for use in logic circuits. Several parameters were explored to optimize performance: the substrate doping process, the device fabrication process, and methods to reduce surface states. The first two parameters are discussed in the next two sections. The last parameter is discussed in Section 2.3.

2.2.1 Substrate doping process

As discussed in Section 2.1.2, diffusion doping gave superior NW conductivity results over ion implantation.[14] The diffusion doping process involves exposing the surface of the Si substrate to a high concentration of dopant atoms at an elevated temperature (usually close to 1000°C). The high temperature creates vacancies in the crystal lattice and the impurity atoms diffuse into the Si lattice by hopping into these vacancies.[23] In comparison, ion implantation involves accelerating a beam of dopant ions to high kinetic energies towards the Si surface. The dopant ions come to rest within the Si lattice. The advantage of this technique is that the dopant profile within the Si substrate can be well controlled. However, ion implantation causes lattice damage and a subsequent thermal anneal is needed to restore the lattice. For decreasing device size, the effect of these lattice defects becomes magnified and for nanoscale structures, ion implantation becomes an unsuitable technique.

For the diffusion doping, spin-on dopants (SODs) were used as the dopant source, which consists of a high concentration of dopant ions within a silica matrix. The SODs are diluted in a solvent and are spin-coated onto the surface. The solvent is removed by heating the Si substrates to 100–200°C, which causes the silica matrix to densify. The coated substrates are then annealed via a tube furnace or a rapid thermal processor (RTP). Lastly, the SODs are removed post-anneal using HF or buffered oxide etch (BOE) (6:1 NH_4F:HF).

Eight inch SIMOX SOI wafers were purchased (Simgui, Shanghai, China) consisting of a 32 nm epilayer of intrinsic Si in the <100> orientation and a 150 nm buried oxide layer on a ~ 0.5 mm thick Si substrate. The best method for cleaning the substrate prior to diffusion doping is the RCA cleaning method, which consists of immersing the substrates in three solutions: 5:1:1 H_2O: H_2O_2: NH_4OH at 80°C for 10 minutes; 1:10 BOE: H_2O at room temperature for 30 seconds; and 5:1:1 H_2O: H_2O_2: HCl at 80°C for 10 minutes. Cleaning the substrates with heated ALEG-355 (Mallinckrodt Baker, Phillipsburg, NJ) or heated acid "piranha" (3:1 H_2SO_4: H_2O_2) also yields good results. It is important that the cleaned substrates be hydrophilic prior to applying the SOD.

Several commercially available SODs were tried and recipes that correlated anneal times and temperatures to measured substrate resistivities were tabulated. To guide the development of RTP recipes, the 1-D diffusion model was used to calculate the dopant profile in Si, *C(d,t,T)*:[24]

$$C(d,t,T) = C_S erfc\left(\frac{d}{2\sqrt{D(T)t}}\right). \tag{2.1}$$

Here, *erfc* is the complementary error function, C_S is the concentration of dopant atoms on the silicon surface, *D(T)* is the diffusivity coefficient, and *t* is the anneal time. *D(T)* is empirically determined for each type of dopant atom. The calculated dopant profiles for boron diffusion at 1000°C ($D = 2 \times 10^{-14}$ cm^2/s)[25] for various anneal times are shown in Figure 2.4. Since *D(T)* has an exponential dependence on *T*, *C(d,t,T)* varies more as a function of *T* than anneal time, and thus the RTA recipes were developed more as a function of anneal temperature than anneal time.

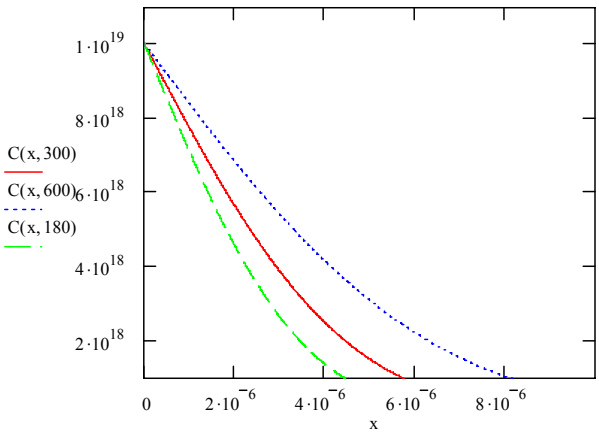

Figure 2.4. Boron concentration as a function of Si depth, for an anneal temperature of 1000°C and for 180, 300, and 600 second anneal times

The two commercially available SODs that yielded the best results were Emulsitone (Whippany, NJ) phosphorosilicafilm 5×10^{20} (the number denotes the phosphorous ion concentration in cm^{-3}), diluted 10-fold in cleanroom-grade methanol, and Filmtronics, Inc. (Butler, PA) Boron A, used without any modification. The SODs can be filtered prior to application but this step is not necessary. The SODs were spin-coated onto the substrates at 4000 RPM for 30 seconds and the substrates were then placed on a pre-heated hotplate set to 100°C. The hotplate temperature was increased to 200°C and the samples were heated for 10 minutes. This temperature ramp is an neccessary step to ensure gas bubbles do not get trapped in the densified SOD.

The substrates were annealed using a tube furnace or a rapid thermal processor (RTP) (RTP 600s System, Modular Process Technology Corp.). The RTP was vastly

superior to use in terms of its temperature control, programmability, sample loading, user interface, consistent performance, and in its ability to anneal under various gas compositions. To anneal using the RTP, substrates were placed on a clean Si wafer and loaded into the RTP chamber. The temperature was monitored by a pyrometer that monitored the temperature of the backside of the Si wafer. Samples were annealed under a flow of N_2. Once the chamber temperature cooled to below 100°C, the samples could be safely unloaded.

The final and most difficult step in the diffusion doping process is removing the SOD post-anneal. During the high-temperature anneal, the SOD matrix densifies further, and for SODs containing organic species such as Boron A, difficult to remove organic films can develop on the Si surface. The best method for removing the SOD and any organic contaiminants without damaging the Si epilayer was the following sequence: 30 seconds BOE immersion, brief DI H_2O immersion, vigorous H_2O rinse using a high-pressure spray gun, immersion in acetone accompanied by surface swabbing, acetone rinse, and another vigorous H_2O rinse. By repeating this sequence, most SODs will be removed without damaging the surface with at most ~ 2 minutes of total BOE exposure.

The impurity concentration of doped substrates was calculated from a four-point resistivity measurement. In this measurement, four aligned metal probe tips with a few mm spacing are brought into contact with the doped substrate. A constant current is passed between the two outer probes and the voltage is measured between the two inner probes. This setup effectively counteracts any probe contact resistance and for thin wafers (where the length and width of the substrate is much larger than the thickness), the sheet resistance, R_S, can be calculated as:[26]

$$R_S = \frac{V}{I} CF \,. \tag{2.2}$$

CF is the correction factor and can be approximated as 4.54 for wafers much larger than the spacing between the probe tips.

To obtain the resistivity, ρ, of the wafer, the sheet resistance is multiplied by the thickness of the Si epilayer:

$$\rho = R_S W \,. \tag{2.3}$$

The resistivity can be used to determine the impurity concentration in the substrate by applying an empirical formula that relates to the two parameters or by a look-up table.[26] Note that this technique does not give any information on the dopant profile through the Si epilayer and that this technique is measuring impurity concentration, not carrier concentration (which are only equal in the case that 100% of the impurities are ionized). However, this method does provide a quick and easy measurement for approximating doping levels.

The four-point measurements were performed using a probe card or a home-built system and a Keithly 2400 SourceMeter (Keithley Instruments, Inc.) operating in four-point mode. The typical current sourced was 100 μA and a minimum of three areas on each substrate were measured, to verify homogeneous doping.

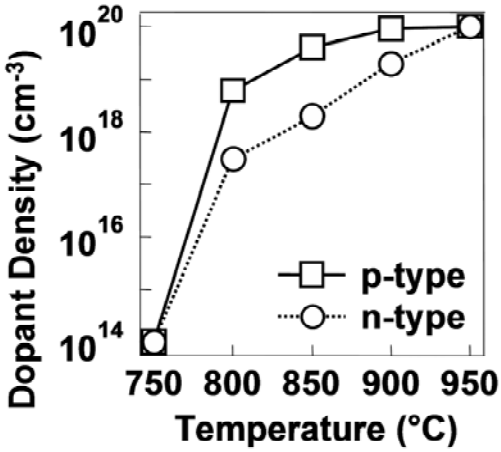

Figure 2.5. Doping levels of boron (p-type) and phosphorous (n-type) under various diffusion temperatures. For all processes, the diffusion time is fixed at 3 minutes.

Samples were annealed for 3 minutes

at temperatures between 750–950°C. The resistivity results were compiled into a graph (Figure 2.5). For various applications, the appropriate doping conditions can be looked up in this plot and selected accordingly.

2.2.2 SNAP technique experimental details

The SNAP technique, qualitatively described in Section 2.1.1, was performed on the doped SOI substrates. A custom-made superlattice (SL) consisting of 800 layers of alternating GaAs and $Al_{0.8}Ga_{0.2}As$ layers grown on top of a (100) GaAs substrate (IQE, Ltd. Cardiff, UK). The superlattice was cleaved in the {110} or {001} plane, forming an atomically flat edge, and diced into ~ 2 mm wide and ~ 5 mm long pieces, referred to as the SNAP masters. The cleaving and dicing processes generate GaAs particles that contaminate the SL. The SNAP masters were sonicated in cleanroom-grade methanol and the cleaved plane was swabbed to remove any contamination visible under 160× magnification.

Once the majority of the particles are removed from the cleaved edge, the SNAP masters were immersed in $NH_4OH/H_2O_2/H_2O$ (1:20:750 v/v) for ~ 10 seconds to selectively etch the $Al_{0.8}Ga_{0.2}As$ regions, followed by an immersion in 30% H_2O_2 for ~ 5 seconds. This second immersion removes residual Ga particles that form on the SL after the etching process.[27] After the etching process, the resulting SL etch consists of GaAs ridges separated by $Al_{0.8}Ga_{0.2}As$ recessions. Pt metal was deposited using e-beam evaporation onto the edge of the GaAs ridges, with the edge of the superlattice held at a 45° angle to the incident flux of Pt atoms. The angle of 45° prevents the Pt from filling in the $Al_{0.8}Ga_{0.2}As$ recessions and determines the Pt NW width.

The doped substrates were prepared by first removing any particles by swabbing the surface in methanol and drying with N_2. The cleaned substrates were coated with a heat-curable epoxy film via spin-coating at 6000–8000 RPM for 30 seconds. The epoxy formulation used is modified from a commercially available epoxy formulation, Epoxy Bond 110 (Allied High Tech, Rancho Dominguez, California). The formulation that yielded the best results was: 5 drops of Epoxy Bond part A, 1 drop of Epoxy Bond part B, and 2 drops of dibutyl phthalate (used as a plasticizer) in 10 mL of anhydrous tetrahydrofuran (THF). The spin-coating speed varies depending on the size of the substrate (large substrates required slower speeds) and is a critical parameter for ensuring successful SNAP results.

Immediately following the spin-coating process, the cleaved edge of the SNAP master was brought into contact with the substrate. The SL/epoxy/SOI assembly was dried on a hot plate (85°C, 30 minutes) and the SL was then released by a selective etch in a concentrated H_3PO_4: 30% H_2O_2: DI H_2O (5:1:50 v/v) solution or a commercially available Au etch solution (containing KI and I_2 in H_2O), leaving a highly aligned array of 400 Pt NWs on the surface of the SOI substrate.

The Pt nanowires served as masks for a reactive ion etch (RIE) process to produce aligned, single-crystal Si NWs. To remove the residual epoxy, the samples were exposed to an O_2/Ar plasma (60 W, 5 mTorr), produced by a 40 MHz Unaxis SLR parallel-plate RIE system. The Si epilayer was then etched using a CF_4/He plasma at 40 W and 5 mTorr for approximately 4 minutes (interferometry can be used to determine the etch time). This plasma recipe generates smooth NW sidewalls with no observable undercutting and no degradation in conductivity. Finally the Pt nanowires were then

removed using aqua regia (4:1 conc. HCl: conc. HNO_3) at 120°C for 10 minutes to produce a ultra-dense array 400 Si NWs at a pitch of 34 nm and width of 17 nm. Residual epoxy can be removed by soaking the substrates in hot ALEG for 30 minutes.

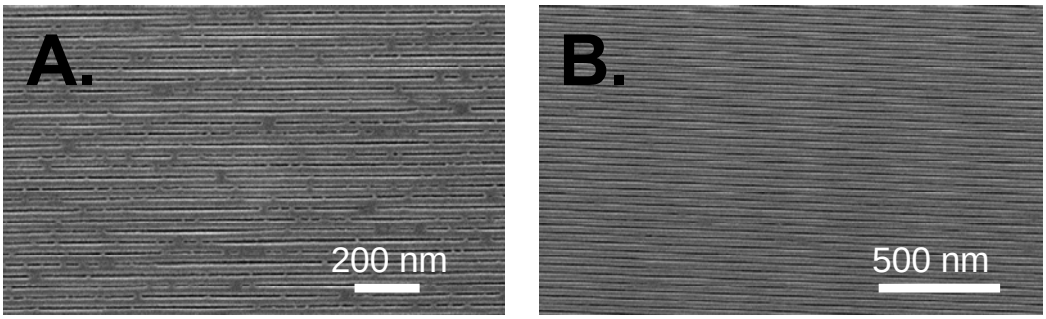

Figure 2.6. Scanning electron micrographs of Si NW arrays before and after surface treatment. **A.** Micrograph of NW array that is shorted together due to problems in the epoxy consistency. **B.** Treatment with an O_2 plasma oxidation and diluted BOE dip removes shorts.

Typically several SNAP masters will be used during the SNAP process to produce several NW arrays on multiple substrates. The typical yield of usable arrays from all the SNAP masters used is 50–80%. The loss of usable arrays was due to a variety of reasons. One common failure is that the SNAP master falls off the substrate during the Pt NW transfer, and no NWs are transferred to the substrate. This is due to particulates between the SNAP master and substrate, which prevents the master from making good contact with the thin epoxy layer. Another failure mode is when the NWs are transferred into the Si epilayer but are shorted together. This is due to a problem in the epoxy consistency. However, this failure can be corrected in some cases. Figure 2.6A shows an example of a NW array containing several shorts. These shorts are significantly narrower than the NWs themselves. After a brief oxidation using an O_2 plasma, followed by a brief dip in 1:100 BOE:H_2O, these shorts are removed (Figure 2.6B) and these NWs are recovered.

2.2.3 Fabrication and measurement of the FET structure

The SNAP process yields a continuous array of NWs that extends over a few millimeters. The first step in fabricating useful devices was to separate the NW arrays into discrete sections. Separated arrays of NWs that are 10–20 μm long were formed by patterning Al sections over portions of the NWs using electron beam lithography (EBL) and electron beam metal deposition. The Al protected the wires underneath from an SF_6 plasma (20 mTorr, 10 W) that removed any exposed Si NWs. The Al was subsequently removed using PAE (80% H_3PO_4 5% CH_3COOH 5% HNO_3 10% H_2O). Alignment markers were carefully patterned around each NW array section, which were then used to pattern source (S) and drain (D) electrodes over the NW sections.

Several different metals were investigated to obtain an ohmic contact to the NWs, such as Ti, Al, Cr, Ni, and Pt. The contacts material that yielded the best results was 10–20 nm Ti (used as an adhesion layer) and 50 nm Pt. Figure 2.7 shows ~ 0.5 μm wide Ti/Pt contacts on Si NWs. The NWs appear brighter between the metal contacts due to their conductivity. Ti/Al/Pt, Cr/Al/Pt, and Ni yielded very poor contacts that could not improved by annealing. Prior to metal deposition, the EBL exposed areas were briefly dipped in 100-fold diluted BOE, which flushes out organic contaminants and removes the native SiO_2. This step was crucial for obtaining ohmic contacts. Several device widths and channel lengths were also explored.

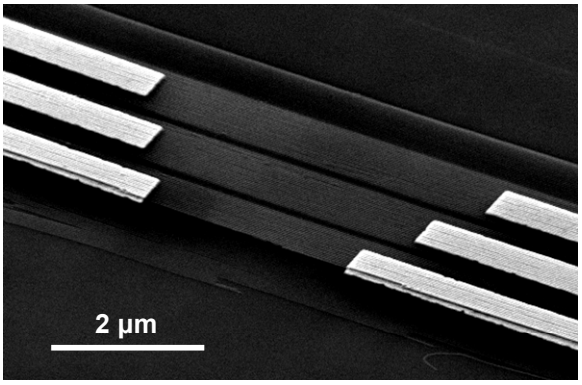

Figure 2.7. Scanning electron micrograph of EBL-patterned electrodes on NWs. NW conductivity is indicated by the brighter areas between the contacts.

On a typical ~ 13 μm wide section of NWs, three S/D electrodes can be patterned to form three FETs with a shared top-gate electrode. Because of the patterning limitations of EBL, the best devices were fabricated from contacts that were over 100 nm wide and with channel lengths of at least 500 nm.

After the S/D contacts were formed, the devices were annealed in the RTP at 475°C for 5 minutes in forming gas (95% N_2 5% H_2). This anneal helped improve the ohmic contacts and reduced the number of surfaces states on the NW channel. The effect of this anneal, which proved to be invaluable for obtaining good device metrics, is discussed further in Section 2.3.

To fabricate the top gate dielectric, 10 nm of Al_2O_3 was deposited at a rate of 0.1Å/s by electron beam evaporation using an Al target in the presence of O_2. The measured dielectric constant of the oxide is ~ 3.7 (see Section 4.2.2 for more details), which is well below the expected value for Al_2O_3. Attempts to improve the dielectric by investigating film thickness, O_2 flow rate, and chamber pressure did not yield any significant improvements. A low chamber pressure (5×10^{-7} Torr) with a moderate-to-high flow rate (+5 to +9 sccm) gave the best results. Increasing the chamber pressure decreased the quality of the Al_2O_3 (as monitored by device on/off ratio) and increasing both chamber pressure and O_2 flow

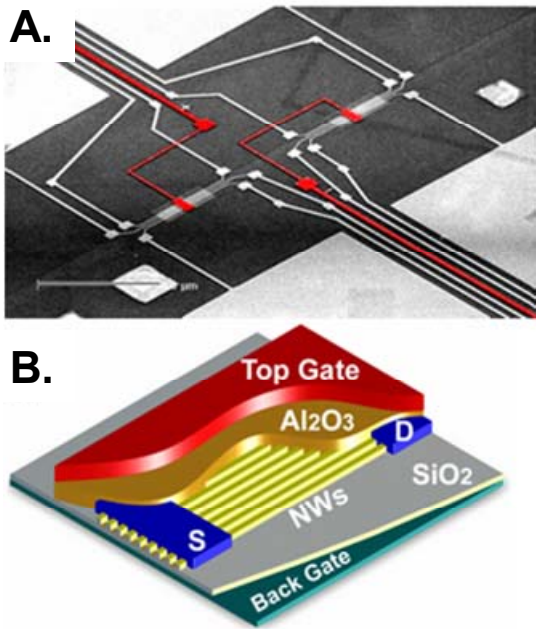

Figure 2.8. NW FET structure. **A.** SEM image of a few devices with top gate color-coded red. Scale bar: 50 μm. **B.** Schematic drawing of the active area of a Si NW FET, with the electrodes labeled.

rate resulted in significant current leakage through the oxide. HfO_2 films were also attempted using electron beam evaporation. All deposited HfO_2 films exhibited significant current leakage.

The last step in the NW FET fabrication process was the formation of the top gate electrode. For the majority of NW FETs, the top gate electrode was patterned using EBL and deposited with 10 nm Ti and 50 nm Pt. The final fabricated FET structure is shown in Figure 2.8A and the idealized device structure is depicted in Figure 2.8B.

To make external electrical contact to the fabricated devices, each electrode fanned out to a 50 × 50 μm contact pad. Devices were contacted using probe tips in a grounded probe station. The S/D contact pads could be contacted through the deposited Al_2O_3 by gently scratching away the oxide using the probe tip. Source to drain current was measured as a function of gate to source and drain to source voltage using using Keithley 2400 SourceMeters and LabVIEW programs (National Instruments).

2.3 Development of high-performance nanowire p-FETs

Once the doping, SNAP, and device fabrication processes were optimized, high-performance NW p-FETs were developed.[28] NW p-FETs consisting of ~ 8 NWs were fabricated with a channel length of 4 μm and a doping level of ~ 10^{18} cm^{-3}. At this doping level, the mobility for bulk Si is ~ 100 cm^2/V-s.[29] Higher doping levels lead to lower mobilities and less gate modulation, and lower doping levels lead to reduced on-current values.

These devices were characterized by utilizing the underlying Si wafer as a bottom gate electrode (Figure 2.9A and 2.9B). Large variations in on-current and on/off switching amplitudes characterized these devices, suggesting the possible presence of defects within the Si lattice or on the surface. Defects can damage performance in a number of ways: they can act as scattering centers that reduce carrier mobilities (leading to lower transconductance and lower on-current values) and they can also serve as charge traps that degrade gating efficiency (poorer on/off ratios and large subthreshold swings).[26]

The performance of the NW p-FETs could be improved significantly with a forming gas (FG) anneal (Figure 2.9A and 2.9C).[29] Prior to gate formation, the NW devices were annealed in FG at 475°C for 5 minutes in the RTP. Prior to annealing, surface adsorbed H_2O could be removed by spin-coating 3% PMMA onto the devices and baking at 130°C for 30 minutes.[28] This was done to eliminate oxidation and charge traps caused by the H_2O.[30] Another method to ensure dry surfaces to simply bake them on a hotplate set to a temperature higher than 100°C for at least 10 minutes. This method can

be used prior to FG anneals and also prior to applying the SOD (but ensure that the wafer has cooled back to RT first).

Once the FG anneal is performed, back-gate FET performance of as-fabricated and annealed devices was compared. Significant improvement in the on/off ratio and the on-current was observed in the annealed devices (Figure 2.9A and 2.9C). This behavior was consistent for over 20 devices made. It was observed that the off-current remained low (~ 100 pA) for all of the measured devices. Longer annealing times did not improve the performance further and high anneal temperatures (650°C) resulted in device degradation. Annealing in pure N_2 yielded at best a marginal improvement in device performance.

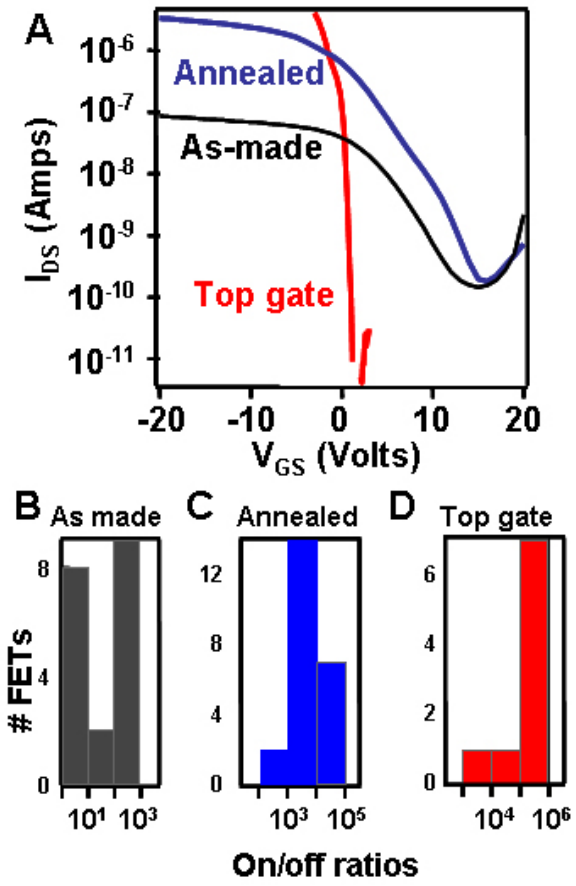

Figure 2.9. Performance characteristics of Si NW FETs for different processing conditions and device configurations. **A.** Source-to-drain (I_{DS}) current values versus applied gate voltages for an as-prepared, back-gated FET (black trace), a back-gated FET post-forming gas anneal (red trace), and a top-gated FET post-forming gas anneal. **B.–D.** Histograms for each of the device parameters shown in A, but representing statistical numbers of device measurements. Relatively fewer top-gate devices were measured due to the fabrication yield of the top-gate processing steps.

The observed improvement of the Si NW FETs following the annealing step can originate from either the removal of Si/SiO_2 interfacial states, or through the promotion of an ohmic contact at the S/D electrodes. It is well known that an FG anneal can reduce defects in Si MOSFETs.[26, 29]

During annealing, Si/SiO_2 interface dangling bonds are terminated by hydrogen from the forming gas and charge traps diffuse out, directly leading to increased on-current and improved on/off ratios.

The effect of promoting an ohmic contact at the NW/contact interface would be a decreased Schottky barrier height. This would typically be manifested as an improved on-current. It is unlikely, however, to significantly reduce off-current. It was observed that similar device performance enhancements (i.e., higher on-current and higher on/off ratios) could be obtained by carrying out the forming gas anneal of the SNAP Si NWs prior to metal contact deposition. Therefore, it is speculated that the charge trap removal plays the most important role. However, since surface states also reside at the NW/contact interface, it is predicted that there is an improvement in electrical contact as well. Cui et al. have also reported on the effectiveness of a much higher temperature forming gas anneal on VLS grown Si NW FETs.[8]

Annealed devices were next characterized after the fabrication of the top gate (see Section 2.2.3 for experimental details). In comparison to the bottom gate devices, the off-current of top-gated devices is greatly decreased, hence increasing the on/off ratios by more than one order of magnitude (Figures 2.9A and 2.9D). This originates not only from an improved gating efficiency through the thin Al_2O_3 dielectric, but also from the diffusion-based SOD doping process. As described in Section 2.2.1, the distribution of dopants through the thickness of the NWs follows the 1D diffusion model.[10, 26, 29] Therefore, most of the carriers reside near the top surface of the NWs, making a gate modulation from the top more effective. This is in accordance with the observations of

improved top-gated devices (Figure 2.9A) and indicates that the SOD doped Si NWs are ideal for a top-gated high-performance FET device.

Another way to illustrate this point is to compare the NW FET I_{DS}-V_{GS} curves using both top-gate and back-gate modulations. V_{GS} sweeps were performed for various back-gate biases and it was observed that the back gate had a negligible effect on the transistor curves (Figure 2.10). Since the buried oxide layer is significantly thicker than the Al_2O_3 layer (150 nm as opposed to 10 nm) and the dopants have the highest concentration on the surface of the NWs, the relative weakness of the back gate was expected.

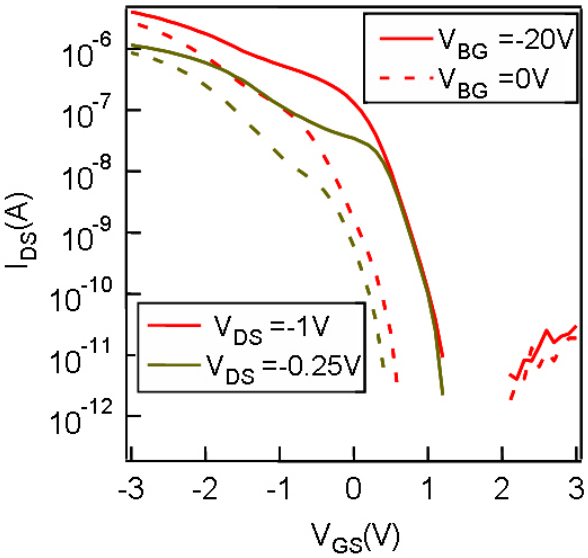

Figure 2.10. I_{DS}-V_{GS} curves with both top-gate (V_{GS}) and back-gate (V_{BG}) modulation

Typical drain current versus gate voltage (I_{DS}-V_{GS}) and I_{DS} versus drain voltage (V_{DS}) data are plotted in Figure 2.11. Several transistor metrics can be extracted from these plots. First, the on-current of the devices is high. As shown in Figures 2.9A and 2.9B, 5 μA on-current through an individual device consisting of ~ 8 NWs was measured. Considering each NW is ~ 17 nm wide × 30 nm high in cross section, the current density equals ~ 1.3 mA/μm^2. Note that this does not represent a fully saturated current value since the V_{DS} values were kept below a certain voltage to prevent any breakdown events in the channel. Furthermore, the 30 nm height does not account for the doping gradient through the thickness of the NWs. This implies that the current density should represent

a lower limit that could easily be increased through, for example, the incorporation of high-κ gate dielectrics through atomic layer deposition.[31] A second positive characteristic was the large on/off current ratios measured—typically 10^5–10^6 (Figure 2.9D). In addition, the measured on-current levels exhibited less than 2-fold variations from device to device. These results confirm the statistical significance of the high-performance characteristics of SNAP Si NW FETs. Mobilities of all devices were extracted in the linear triode regions with V_{DS} = -0.25 V. In this region,[26]

$$\mu = \frac{dI_{DS}}{dV_{GS}} \times \frac{L^2}{C_{ox}} \times \frac{1}{V_{DS}} \tag{2.4}$$

where $\frac{dI_{DS}}{dV_{GS}}$ is the transconductance and a typical value for our devices is ~ 1 μA/V; L is the device length and is 4 μm; C_{ox} is the gate capacitance and is ~ 5×10^{-15} F; and V_{DS} = 0.25 V. The calculated mobility values are summarized in Figure 2.11C. The mean value ~ 100 cm^2/V-s is close to bulk Si value with a doping level of ~ 10^{18} cm^{-3}.

An additional figure of merit is the subthreshold swing (**S**), which is defined as:[26]

$$S = \frac{kT}{q} \ln 10 \cdot \left[1 + \frac{C_G}{C} \right] \tag{2.5}$$

where C is the entire gate capacitance and C_G includes the component of the capacitance that arises from interface states and parasitic capacitance: when C_G = 0, ideal behavior is obtained. A low **S** is desired for low power operation and can only be obtained with low-defect-density devices.

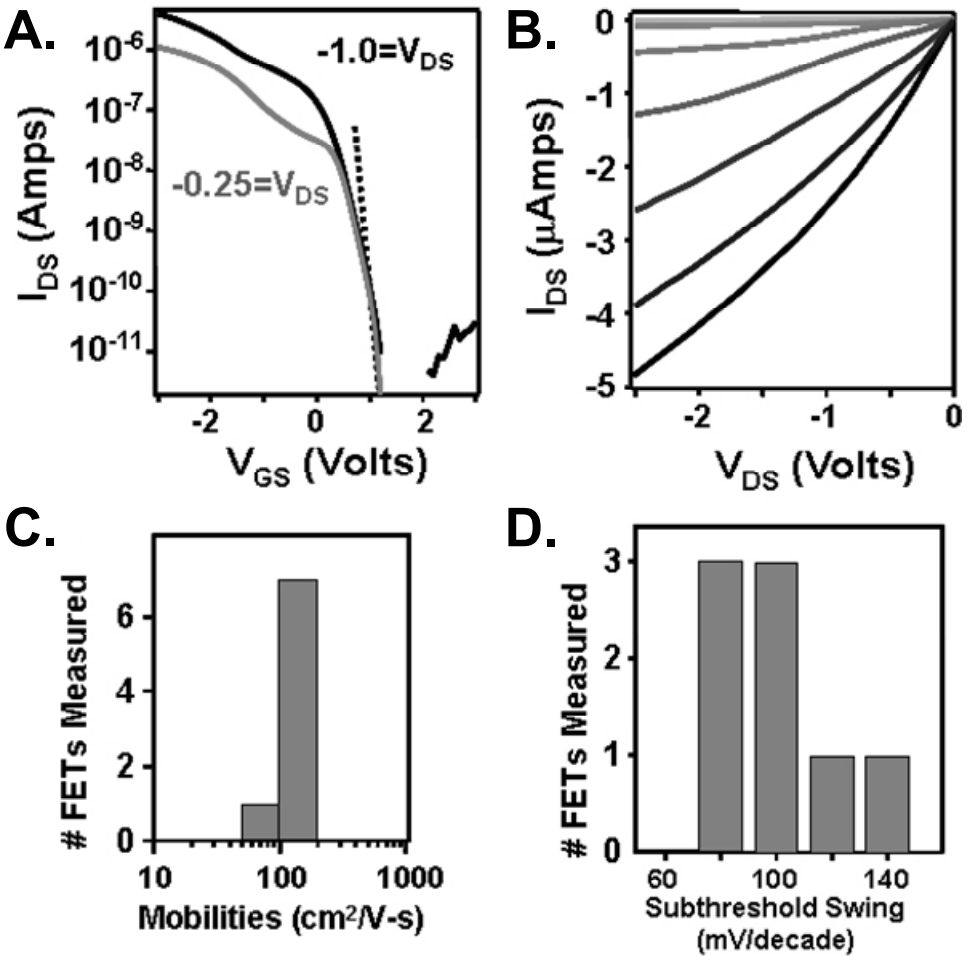

Figure 2.11. High-performance, top-gated p-type Si NW FETs. **A.** I_{DS}-V_{GS} characteristics at different bias source-drain biases. The dashed line represents the fitted sub-threshold slope value of 83 mV/decade. **B.** I_{DS} versus V_{DS} at different gate voltages, from -3 V (darkest colored trace) to 1 V (lightest colored trace), at 0.5 V/step. At least 5 μA current can be driven through a single device (consisting of ~ 8 NWs) without noticeable degradation while the experiments are carried out under ambient conditions without precautions to prevent oxidation. **C. and D.** Statistics from top-gated Si NW FETs for both carrier mobilities and for subthreshold swing values

S was extracted from I_{DS}-V_{GS} curves at current levels below 10^{-10} A using the relationship: [32, 33]

$$S = \frac{dV_{GS}}{d\log\left(I_{DS}\right)}. \tag{2.6}$$

Those values are summarized in Figure 2.11D. The highest performing device yielded an **S** of ~ 80 mV/decade and the poorest performing device yielded **S** = 130 mV/decade.

The 80 mV/decade value represents the lowest subthreshold swing of any p-type NW FET to date, although ~ 70 mV/decade has been reported for n-type (CdS) NW FETs.[34] The record for an n-type Si NW FET is ~ 80 mV/decade.[33] The lowest **S** value previously reported for a Si NW p-type FET was 135 mV/decade.[13] Given the low **S** values and property uniformity of the devices discussed here (Figure 2.9D), these results indicate that the SNAP process can yield very high-quality transistors at device dimensions and circuit densities that far exceed what can be produced using more traditional patterning methods.

2.4 Comparison of nanowire and microwire performance

Initial attempts to produce NW n-FETs with performance metrics comparable to the NW p-FETs were not successful. The n-FETs were fabricated exactly like the p-FETs but using substrates that were doped n-type at a concentration of ~ 10^{18} cm^{-3}. Typical performance metrics included on/off ratios of ~ 5000 and much larger **S** values than their p-type counterparts.

Low dimensional semiconductor materials are characterized by high surface-area-to-volume ratios.[35, 36] Recent studies have shown that the electronic properties of extremely thin (~ 10 nm) SOI films can be dominated by surface states.[37] Similar results have also been demonstrated on Ge NWs as well.[38] In the semiconductor industry, n-type Si devices have been more challenging to develop due to their enhanced sensitivity to surface states over p-type devices.[39] In the NW community, few literature reports exist of

NW n-FETs with high performance metrics.[40] To understand how the high characteristic surface area impacts the performance of Si NW FETs, Si NW FETs and Si microwire (μW) FETs were prepared side-by-side on the same SOI substrate using the SNAP method for the NW FETs and more traditional lithographic patterning for the μW FETs. The device structures are schematically depicted in Figure 2.12C.

A SOI substrate was first doped using either p- or n-type spin-on-dopants (SODs). The SNAP process was then carried out to place a Pt NW array onto the SOI surface. Afterwards, a stripe of ~ 10 μm wide and 10 nm thick Pt thin film was patterned adjacent to the SNAP Pt NWs by e-beam lithography (EBL) and metal deposition. The Pt NWs or microstructures served as masks for a reactive ion etching (RIE) process to transfer the Pt NWs and stripes patterns to form analogous Si NWs and stripes.[9] The resulting structure consisted of an array of Si NWs adjacent to a thin film of Si, both on a SiO_2 dielectric (Figure 2.12C). Ti/Pt (20 nm/50 nm) S/D contacts were patterned by EBL to be 150 nm wide and separated 2 μm apart. Al_2O_3 (10 nm) was then deposited as a gate dielectric, and a Ti top gate electrode was deposited to conclude the fabrication process, as shown in Figure 2.12C.

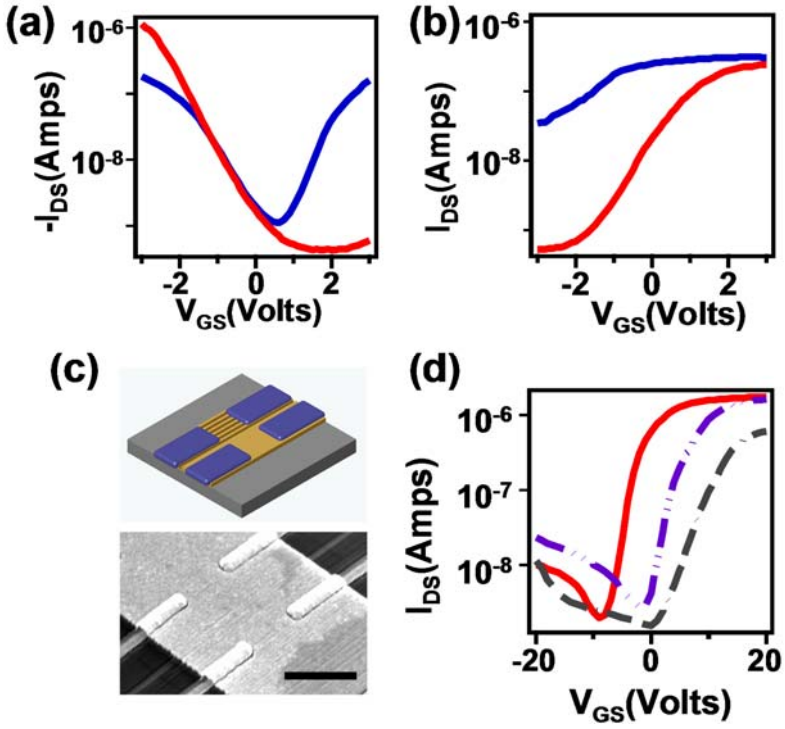

Figure 2.12. Comparison of NW and µW FET performance. I_{DS}-V_{GS} curves of **A.** P-type and **B.** n-type NW FETs (red) and µW FETs (blue). **C.** Device structure with µW NW FETs side by side. Scale bar: 2 µm. **D.** I_{DS}-V_{GS} curves of NW n-FETs after different treatments. Solid red trace: as-fabricated; purple broken line: after O_2 plasma; gray broken line: after H_2 plasma. For all devices, V_{DS}=1.5 V for n-type and -1.5 V for p-type.

In this experiment, four types of devices were characterized and compared, namely NW p- and n-FETs, and µW p- and n-FETs. The as-fabricated NW p-FETs exhibited similar characteristics as those described in the previous section,[28] i.e., high on-current at high negative gate potentials and low off-current at high positive gate potentials (Figure 2.12A). The µW p-FETs, however, were typified as ambipolar: a high on-current was observed at both positive and negative gate potentials and a low off-current was only seen at low gate potentials (Figure 2.12A). This suggests that for µW p-FETs, both hole (at negative gate potentials) and electron carriers (at positive gate potentials) are important for the conductance, whereas in NW p-FETs only hole carriers are significant. Given that the NW and µW FETs are fabricated side by side on the same

substrate and have undergone the same processing sequences, the doping levels, crystal orientations and electrical contacts should be identical. The only difference should be the increased surface-area-to-volume ratio for the NWs. It is therefore reasonable to suspect that the difference in device characteristics is mainly a result of the surface effects. Similar differences were also observed on n-FETs: NW n-FETs could be turned off easily while neighboring μW n-FETs that have identical parameters exhibited a noticeably weaker gate response (Figure 2.12B). It appears that the μW n-FETs have a higher electron carrier concentration than the analogous NW devices.

Considering that all of the measurements were conducted in ambient air, it is suspected that the surfaces of NWs tend to p-dope the channel, hence the hole carriers are enhanced and electrons are suppressed. Similar effects have been widely reported for CNT and organic-material devices.[41–43] To better understand this, systematic surface treatments on all devices were performed and the corresponding changes of transport characteristics were compared. Taking NW n-FETs as an example, the as-fabricated devices were measured with a bottom gate (i.e., using the underlying Si wafer of the SOI substrate as a gate electrode). These devices were then subjected to gentle O_2 and H_2 plasma treatments (Figure 2.12D). Such treatments constitute standard cleaning processes that are often employed during FET fabrication. After the O_2 plasma treatment, the clear trend was that the p-channel was enhanced and n-channel suppressed (purple curve in Figure 2.12D). This may arise because surface-adsorbed O_2 p-dopes the NW channels. By contrast, both the p- and n-channels were suppressed by the H_2 plasma treatment (gray curve in Figure 2.12D). This universal effect likely arises from surface damage that results from the reaction of H_2 or H-atoms with the Si native oxide, and thus

introduces surface states that can trap both holes and electrons. Similar experiments were also carried out on NW p-FETs and μW FETs. And for all devices, O_2 treatments enhanced p-channel and suppressed n-channel while H_2 suppressed both p- and n-channels. Importantly, the effects were always more pronounced for the NW FETs. NW FET performance metrics were clearly more dependent upon the surface treatments that were employed.

2.5 Development of high-performance nanowire n-FETs

The fabrication of the n-FETs was similar to the p-FETs but special care was taken to ensure the surface was clean after every step. The RCA cleaning process was done prior to applying the SOD and after the NWs were formed. Also, the substrate was annealed in N_2 at 450°C for 1 minute to fix surface states. As shown in Figures 2.13A and 2.13B, as-fabricated devices exhibited good n-type characteristics, with on/off ratios $> 10^3$, high on-current (> 1 μA), and acceptable transconductance (~ 1 μS). Equally important was that the n-FET performance was uniform over more than 15 measured devices (Figure 2.13C).

The RCA cleaning and 450°C annealing are important to this result. Devices without these treatments typically showed large variations in performance parameters. Different annealing conditions were explored and it was found that higher temperatures (e.g., 800°C) resulted in lower on-currents, and no working devices were obtained for 900°C annealing. On the other hand, lower annealing temperatures (e.g., 300°C) resulted in less-consistent device performance metrics.

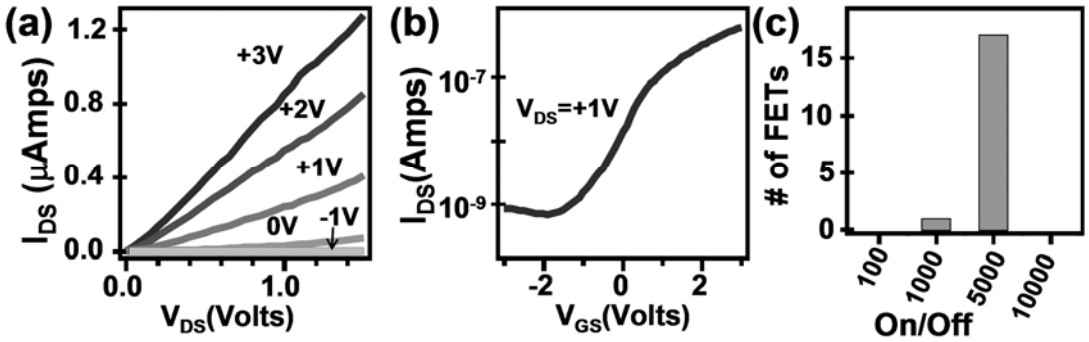

Figure 2.13. N-FET performance metrics. **A.** and **B.** I_{DS}-V_{DS} and I_{DS}-V_{GS} characteristics of NW n-FETs. Device dimensions: 150 nm wide with 2 μm channel length. The underlying Si bottom gate is grounded for all measurements. **C.** Histogram of on/off ratios of 17 measured devices

It is worth pointing out that the n-FETs in this study are non-optimized. The gate dielectric was e-beam evaporated Al_2O_3, the poor quality of which may be responsible for the large subthreshold swings (Figure 2.13B). Chapter 4 discusses the significant improvement of the n-FET devices by using in silico design feedback. Nevertheless, these results are significant in that this fabrication process reliably and consistently produced good n-FETs (Figure 2.13C). Moreover, when taken together with the much higher quality p-FETs that were obtained using similar protocols, an opportunity to integrate both p- and n-FETs within the same NW array to produce complementary-symmetry NW logic devices is presented.

2.6 Conclusions

The SNAP method, coupled with spin-on doping techniques and forming gas annealing, was utilized to produce high density arrays of 17 nm wide, 34 nm pitch Si NWs doped at 10^{18} cm^{-3}. FETs fabricated from small groups of these NWs exhibited extremely good performance characteristics, including high on-current, high on/off ratios and low subthreshold swings. In particular, the unprecedented S ~ 80 mV/decade for p-type Si NWs FETs reveals that the SNAP process can produce high-quality Si NWs with negligible numbers of defects. These results were valid for statistical numbers of devices, and provide a compelling argument for the reproducibility of this process.

In addition, it was demonstrated that Si NW FETs are sensitive to the surface properties, and that information was used as feedback to improve the nanofabrication techniques to achieve consistent performance from n-type Si NW FETs. These results opened up the opportunity to produce complementary logic circuits within ultra-high-density NW arrays.

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