GROWTH AND CHARACTERIZATION OF Si-BASED ELECTRONIC MATERIALS FOR NOVEL DEVICE APPLICATIONS

Thesis by
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To the two Pattis in my life

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Abstract

The material presented in this thesis concerns the growth and characterization of Si-based electronic materials through the use of molecular beam epitaxy (MBE). In particular, the $Si_{1-x}Ge_x/Si$ and $V_{1-x}Si_x/Si$ material systems are studied because of their potential application in novel, heteroepitaxial device structures grown on crystalline Si substrates. Our work with the $Si_{1-x}Ge_x/Si$ material system involves a study of the kinetics of strain relaxation for coherently strained $Si_{1-x}Ge_x$ alloys grown on (100) Si at extremely low temperatures. In addition, we measure the strain dependence of the (100) Si/Ge valence band offset through the use of x-ray photoelectron spectroscopy (XPS). Further study of $Si_{1-x}Ge_x$ alloys reveals a previously unreported (2×8) surface reconstruction, and for highly metastable alloys, the occurrence of chemical segregation during growth. We also report the successful nucleation and growth of superconducting V_3Si on (111) Si, the first step toward the realization of epitaxial superconductor/semiconductor heterostructures. Finally, we make use of the knowledge gained in our preliminary studies and present the first electrical characterization of p-$Si_{1-x}Ge_x$/n-Si heterojunction interband-tunnel (HIT) diodes, demonstrating an enhancement of negative differential resistance (NDR) as a function of Ge concentration in the p-type $Si_{1-x}Ge_x$ layer.

In Chapter 2, we present a study of strain relaxation in metastable $Si_{1-x}Ge_x/Si$ superlattices and $Si_{1-x}Ge_x$ alloys. The samples prepared for this study are grown at unusually low growth temperatures ($\sim 365\,^\circ$C) to thicknesses significantly in excess of previously established critical thicknesses for growth at higher temperatures. θ-2θ x-ray diffraction (θ-2θ XRD) is used to study the relaxation process as the samples are annealed in a sequence of isochronal anneal steps. Significant relaxation is observed at anneal temperatures as low as $370\,^\circ$C.

In addition, we compare the relaxation behavior of $Si_{1-x}Ge_x/Si$ superlattices and $Si_{1-x}Ge_x$ alloys designed to possess the same average properties and report that the superlattices relax to a lesser extent than the corresponding alloys. Finally, alloy relaxation is described as a thermally activated, first-order kinetic process described by a single activation energy of approximately 2.0 eV.

In Chapter 3, the strain dependence of the (100) Si/Ge valence band offset is measured through the use of XPS. Coherently strained Si, strained Ge, and symmetrically strained Si/Ge superlattices are grown on relaxed $Si_{1-x}Ge_x$ buffer layers and transferred in ultrahigh vacuum (UHV) to the XPS chamber. Si $2p$ and Ge $3d$ core level to valence-band edge, and core level to core-level energy separations are measured as a function of in-plane lattice constant. High resolution x-ray diffraction (HRXRD) is used to measure the strain in these samples. For the valence band offset, we measure 0.83 ± 0.11 eV for Ge strained to (100) Si and 0.22 ± 0.13 eV for Si strained to (100) Ge.

High-quality, coherently strained $Si_{1-x}Ge_x$ alloy layers are studied in Chapter 4 using HRXRD and *ex situ* transmission electron diffraction (TEM). Several samples are grown at extremely low temperatures (310 – 330 °C) by MBE. Sample thicknesses and alloy concentrations are chosen to span a range beginning just below to significantly above critical thicknesses previously reported for this system. HRXRD observations demonstrate a high degree of coherency in the as-grown structures, since measurements of the lattice constant parallel to the sample surface ($a_{\parallel}$) consistently yield the value for the (100) Si substrate. HRXRD from (004) planes used to measure $a_{\perp}$ typically yield a spectrum with several peaks for growths in excess of the critical thickness and single peaks for those below the critical thickness. The high degree of coherency observed in these samples suggests that chemical segregation is responsible for the observed x-ray peaks.

In Chapter 5, the surfaces of $Si_{1-x}Ge_x$ alloys are studied using reflection high-energy electron diffraction (RHEED) and low-energy electron diffraction (LEED) techniques. $Si_{1-x}Ge_x$ films are grown on Si (100) substrates by MBE at temperatures between approximately 230 and 550 °C, with alloy compositions ranging from $x = 0.11$–0.30. RHEED and LEED patterns from samples within this compositional range and at temperatures between 350 °C and 550 °C exhibit the usual Si-like (2×1) surface reconstruction patterns modified by the appearance of new, $n/8$-order diffracted beams. The $n/8$-order beams are observed for both coherently strained and unstrained films. Upon annealing and recooling, they appear to degrade reversibly within the temperature range 600–700 °C. The additional fractional orders are interpreted as an 8-fold-periodic modulation in electron scattering factor, which is due to spatial correlation (ordering) of Ge atoms along the dimer chains of a (2×1) surface reconstruction. Possible physical origins of the Ge ordering are discussed.

A study of the growth parameters governing the nucleation of metastable superconducting $A15$ V_3Si on Si and Al_2O_3 is presented in Chapter 6. Nominally, 500 Å films of $V_{1-x}Si_x$ are produced through codeposition of V and Si onto heated (111) Si and $(1\bar{1}02)$ Al_2O_3 substrates. Samples are prepared in a custom-built UHV chamber containing dual *e*-beam evaporation sources and a high-temperature substrate heater. V and Si fluxes are adjusted to result in the desired average film composition. $V_{0.75}Si_{0.25}$ films prepared at temperatures in excess of 550 °C on Si show significant reaction with the substrate and are nonsuperconducting, while similar films grown on Al_2O_3 exhibit superconducting transition temperatures (T_c) approaching bulk values for V_3Si (16.6 – 17.1 K). Codeposition at temperatures between 350 and 550 °C results in superconducting films on Si substrates, while growth at lower temperatures results in nonsuperconducting films. Lowering the growth temperature to 400 °C is shown through *ex situ* TEM and Auger compositional profiling to minimize the reaction with

the Si substrate while still activating the surface-migration processes needed to nucleate $A15$ V_3Si. Variation of film composition about $x = 0.25$ is shown to result in nonsuperconducting films for high x and superconducting films with T_c approaching the bulk V value (5.4 K) for low x. Finally, lowering the $V_{0.75}Si_{0.25}$ deposition rate is shown to raise T_c.

In Chapter 7, we present an electrical characterization of the first p-$Si_{1-x}Ge_x/n$-Si HIT diodes. Equilibrium band-bending calculations are used to predict qualitatively an enhancement of NDR as a function of Ge concentration in the $Si_{1-x}Ge_x$ alloy layers. Experimentally, measurements of I–V curves from HIT diodes compared with a Si interband-tunnel diode confirm the enhancement effect. Finally, differentiation of the current-voltage relationship through the use of inelastic electron tunnelling spectroscopy (IETS) reveals previously unobserved phonon peaks in the HIT diodes. The possible origin of these features is discussed.

List of Publications

Parts of this thesis have been, or will be, published under the following titles:

Chapter 2:

Strain Relaxation Kinetics in $Si_{1-x}Ge_x/Si$ Heterostructures,

R. J. Hauenstein, B. M. Clemens, R. H. Miles, O. J. Marsh, E. T. Croke, and T. C. McGill, *J. Vac. Sci. Technol. B* **7**, 767 (1989).

Relaxation of Coherent Strain in $Si_{1-x}Ge_x/Si$ Superlattices and Alloys,

R. J. Hauenstein, R. H. Miles, E. T. Croke, and T. C. McGill, *Thin Solid Films* **183**, 79 (1989).

Chapter 3:

Measurement of the Valence Band Offset in Strained Si/Ge (100) Heterojunctions by X-ray Photoelectron Spectroscopy,

E. T. Yu, E. T. Croke, and T. C. McGill, *Appl. Phys. Lett.* **56**, 569 (1990).

Measurement of the Valence Band Offset in Novel Heterojunction Systems: Si/Ge (100) and AlSb/ZnTe (100),

E. T. Yu, E. T. Croke, D. H. Chow, D. A. Collins, M. C. Phillips, T. C. McGill, and J. O. McCaldin, *J. Vac. Sci. Technol. B* **8**, 908 (1990).

Measurement of the Strain Dependence of the Si/Ge (100) Valence Band Offset,

E. T. Yu, E. T. Croke, T. C. McGill, and R. H. Miles, *SPIE Vol. 1285 Growth of Semiconductor Structures and High-T_c Thin Films on Semiconductors*, 214 (1990).

Chapter 4:

Evidence of Segregation in (100) Strained $Si_{1-x}Ge_x$ Alloys Grown at Low Temperature by Molecular Beam Epitaxy,

E. T. Croke, T. C. McGill, R. J. Hauenstein, and R. H. Miles, *Appl. Phys. Lett.* **56**, 367 (1990).

Chapter 5:

Observation of Reconstruction Periodicity on Surfaces of $Si_{1-x}Ge_x$ Alloys Grown on Si (100) by Molecular Beam Epitaxy,

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Observation of a (2×8) Surface Reconstruction on $Si_{1-x}Ge_x$ Alloys Grown on (100) Si by Molecular Beam Epitaxy,

E. T. Croke, R. J. Hauenstein, T. C. Fu, and T. C. McGill, presented at the Eighteenth Conference on the Physics and Chemistry of Semiconductor Interfaces, Long Beach, CA, January 29 - February 1, 1991.

Chapter 6:

Growth of Superconducting V_3Si on Si by Molecular Beam Epitaxial Techniques,

E. T. Croke, R. J. Hauenstein, and T. C. McGill, *Appl. Phys. Lett.* **53**, 514 (1988).

Growth and Characterization of Superconducting V_3Si on Si and Al_2O_3 by Molecular Beam Epitaxial Techniques,

E. T. Croke, R. J. Hauenstein, C. W. Nieh, and T. C. McGill, *J. Elec. Mat.* **18**, 757 (1989).

Contents

5 Observation of a (2 × 8) Reconstruction on Surfaces of (100) $Si_{1-x}Ge_x$ Alloys 90

6 Growth of Superconducting V_3Si on Si 116

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Introduction to Thesis

The work presented in this thesis primarily addresses issues pertaining to the growth and characterization of Si-based electronic materials prepared through the use of molecular beam epitaxy (MBE). Our effort is motivated by the belief that future processing technology will be able to integrate many different types of electronic devices on a single chip of semiconducting material. Realization of this goal requires the development of materials and processing technologies resulting in high-quality device structures, free from defects and performance-destroying impurities. Since typical MBE growth temperatures are much lower than conventional, chemical vapor deposition (CVD) techniques, high-quality device structures with monolayer abruptness can be fabricated. The best candidate for substrate material currently appears to be Si, since Si substrates are relatively inexpensive to manufacture, generally can be made defect-free, and are available in n- or p-type with resistivities varying from intrinsic to degenerate. For these reasons, we have preferred to investigate material systems suitable for integration with existing Si-device technologies. In particular, we have focused upon the

$Si_{1-x}Ge_x/Si$ and $V_{1-x}Si_x/Si$ material systems.

To introduce the work presented in this thesis, Chapter 1 has been organized as follows. Most of the chapter has been dedicated to providing a strong technical base for many of the ideas presented in later chapters. Section 1.2 gives an overview of the fundamental concepts necessary for understanding the MBE growth technique. Attention is given to describing a typical Si MBE growth chamber, sample preparation, *in situ* characterization techniques, and doping. Section 1.3 introduces the concepts of strain and critical thickness as they apply to growth of thin layers on crystalline substrates. Several theories of critical thickness are discussed and $Si_{1-x}Ge_x/Si$ is offered as the model, strained-layer material system. In addition, the measurement of strain through the use of high-resolution x-ray diffraction (HRXRD) and θ-2θ x-ray diffraction (θ-2θ XRD) is described. Section 1.4 discusses the use of x-ray photoelectron spectroscopy (XPS) for measuring valence band offsets in strained semiconductor systems. Section 1.5 introduces several electrical techniques used to characterize p-$Si_{1-x}Ge_x/n$-Si heterojunction interband-tunnel (HIT) diodes including 2, 3, and 4-point I–V measurements and inelastic electron tunnelling spectroscopy (IETS). Finally, presented in Section 1.6 is an overview of the remaining chapters of the thesis.

1.2 Fundamentals of Si MBE

1.2.1 The Si MBE Growth Chamber

The term molecular beam epitaxy* typically refers to the technique of depositing a flux of atoms or molecules onto a heated crystalline substrate under

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*Strictly speaking, epitaxy usually refers to the growth of crystalline material oriented preferentially on a crystalline substrate.

ultrahigh-vacuum (UHV) conditions. Achieving and maintaining UHV is essential for producing high-quality thin films. Commercial UHV systems employ stainless steel chambers and generally contain parts fabricated from refractory metals and "UHV compatible" ceramics (copper is also a common material). UHV-compatible parts are degreased *ex situ*, and contain insignificant quantities of absorbed gases. Current vacuum technology is capable of producing pressures on the order of 5×10^{-11} Torr through the use of ion pumps, cryopumps, and Ti sublimators.

All of the samples studied in this thesis were grown in vacuum systems specifically designed for Si epitaxy. Two independent systems were employed here. One is a custom-built, Si-silicide deposition chamber capable of simultaneous evaporation of two elements from a Thermionics, dual *e*-beam source. Examples of elements which we have coevaporated with Si in this system are Co, Ni, Ge, and V. A tungsten heating element is used to radiatively heat a 2 inch substrate to temperatures exceeding 850 °C. Typical growth temperatures for Si homoepitaxy range from 300 to 700 °C. Several LN_2 cryopanels and H_2O cooling shrouds protect the walls of the chamber from excessive heat load from the *e*-beam source and the substrate heater; otherwise, outgassing of heated parts would introduce contaminants into the vacuum and ultimately, onto the substrate. Also included in the system is a quadrupole mass analyzer used to analyze residual gases in the vacuum. Finally, a Princeton Instruments reverse view LEED (low-energy electron diffraction) optical system is mounted on a 6 inch flange to the side of the substrate heater for *in situ* surface analysis. A more detailed description of the Si-silicide MBE chamber is described elsewhere.[1]

Most of the $Si_{1-x}Ge_x/Si$ samples prepared for this thesis were grown in a Perkin-Elmer (Model 430S) Si MBE system. A schematic of the system is shown in Fig. 1.1. The Perkin-Elmer system holds several important advantages over the

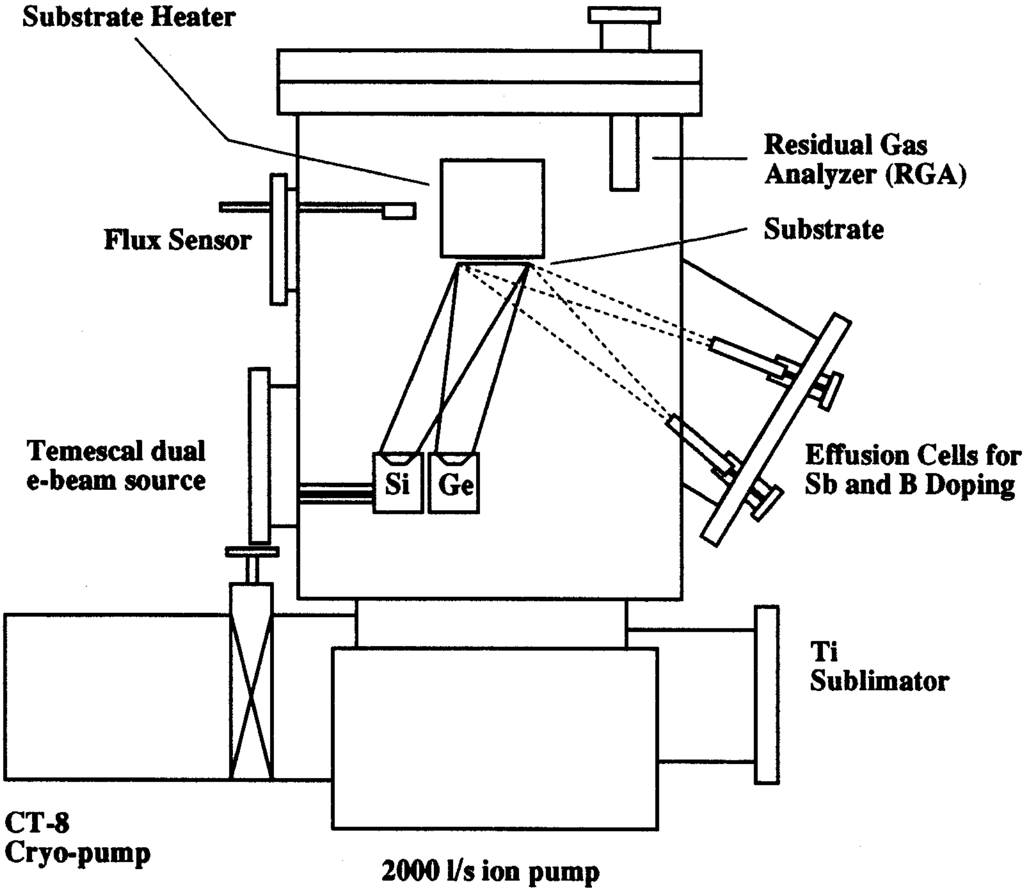


Figure 1.1: Schematic of the Perkin-Elmer (Model 430S) Si MBE system. Visible in the figure is a dual, *e*-beam evaporator for Si and Ge evaporation, a cathodoluminescent flux sensor, a graphite filament substrate heater for radiative heating of the substrate, several effusion cells for doping, a residual gas analyzer (RGA) and a pumping system consisting of a 2000 l/s ion pump, a model CT-8 cryopump, and a titanium sublimation pump.

Si-silicide chamber. For example, the dual *e*-beam source can be loaded with more than 40 cc of material, compared with only 2 cc for each crucible in the Si-silicide chamber. As a result, the vacuum chamber does not need to be vented as often. Also, the *e*-beam flux is monitored with a cathodoluminescent flux sensor (Inficon, Sentinel III), allowing deposition rates to be controlled down to 0.01 Å/s. In addition, the substrate heater uses a serpentine, graphite heating element which gives excellent temperature uniformity across the substrate while minimizing any chance of metallic contamination. In contrast to the Si-silicide system, the Perkin-Elmer Si MBE machine uses reflection high-energy electron diffraction (RHEED) for *in situ* surface analysis. Both RHEED and LEED analysis techniques will be discussed further in Section 1.2.3. In addition, a residual gas analyzer (RGA) identical to the one used in the Si-silicide chamber is included in the system for leak-testing and characterization of the UHV environment.

1.2.2 Substrate Preparation

The preparation of a clean Si starting surface is just as important to successful growth as maintaining the sample in UHV. For instance, carbon contamination is known to produce deep levels,[2] and particulates contribute significantly to defect formation and poor crystalline quality.[3] Most cleaning procedures begin with an HF etch to remove SiO_2, followed by the growth of a "clean" oxide using one of several chemical oxidation procedures. For example, Ishizaka and Shiraki[4] refined the standard RCA[5] cleaning procedure for Si to include repeated oxidation in hot HNO_3:H_2O and oxide removal in HF:H_2O. A final passivating oxide is grown in HCl:H_2O_2:H_2O (3:1:1) prior to loading into the growth chamber. Once inside the growth chamber, thermal cleaning procedures can be employed to remove the passivating oxide. These procedures purport to reduce carbon contamination by trapping it in the oxide layers and subsequently eliminating it once the oxide is removed.[6] Some workers,[7] however, suspect that contamination may increase during the course of these chemical procedures and that cleaner samples would result simply by etching the oxide in dilute HF prior to *in situ* cleaning.

The procedure we have developed is based upon the latter suspicion. (100) Si substrates are first degreased at 50 °C in (1,1,1) trichloroethane, acetone, and methanol solvents. After degreasing, the substrates are rinsed in de-ionized water and etched in a 50% HF solution to remove any native oxide. Once the oxide layer is removed, the substrate is rinsed again in de-ionized water and removed slowly, eliminating the need for blow-drying since the bare Si surface is hydrophobic. We suspect that through elimination of the blow-drying step, we can reduce the amount of particulates needlessly introduced onto the surface of the substrates. Immediately after these *ex situ* cleaning procedures are completed, the substrates are loaded into the MBE growth chamber.

Once inside the growth chamber, SiO_2 can be desorbed through a variety of techniques. Following the original work of Streit and Allen,[8] we apply a 0.1 Å/s Si flux to the substrate held at a temperature of approximately 850 °C. A slightly higher temperature is needed for (111) Si substrates. At this temperature, SiO_2 is reduced by the incident Si flux and forms SiO, which immediately leaves the surface. After approximately two minutes, a (2×1) surface reconstruction is observed with RHEED,[9, 10] and the Si flux is removed. Our experience has proven that it is imperative to shut off the Si flux immediately after the (2×1) reconstruction appears, since further deposition of Si at these temperatures has resulted in hazy surfaces. Furthermore, the Si flux must be low; otherwise Si will build up on the oxide faster than it is removed, again resulting in poor surface morphology. Once the oxide has been removed, we typically grow a Si buffer layer as the substrate temperature is ramped down from 700 °C to 500 °C. In this way, clean, (2 × 1)-reconstructed Si surfaces can be produced rather routinely.

1.2.3 *In situ* Characterization Techniques

Through the use of reflection high-energy electron diffration (RHEED) and low-energy electron diffraction (LEED) techniques, sample surfaces can be characterized *in situ*. In this section, the experimental setup and the interpretation of LEED and RHEED diffraction patterns are discussed. In RHEED, a high-energy electron beam with typical energies of 10 – 40 keV is diffracted at glancing incidence off the sample surface and across the growth chamber where it produces a pattern on a phosphor screen (see Fig. 1.2). RHEED patterns from flat, crystalline surfaces show sharp streaks (zeroth-order Laue zone) and spotted rings (higher-order Laue zones) centered about a specular spot produced from reflection. Patterns from different azimuths produce different patterns; therefore, the sample must be rotated to determine surface symmetries. The origins of the pattern will be discussed later. In the Perkin-Elmer system, we can use RHEED to monitor the sample surface during growth, although in practice this is difficult since interaction of the RHEED beam with the fields produced in the e-beam sources causes the pattern to appear fuzzy. Still, the technique allows us to monitor surface periodicities and to verify surface cleanliness. For example, clean (100) and (111) Si surfaces are well known to exhibit (2 × 1) and (7 × 7) superstructures,[11] respectively, in their diffraction patterns.

On the Si-silicide chamber, we have mounted a Princeton Instruments (Model RVL-6-120), reverse-view LEED optical system. A schematic diagram describing the technique is presented in Fig. 1.3. With LEED, a 30-100 eV electron beam is incident normally to the sample surface. Elastically scattered electrons are

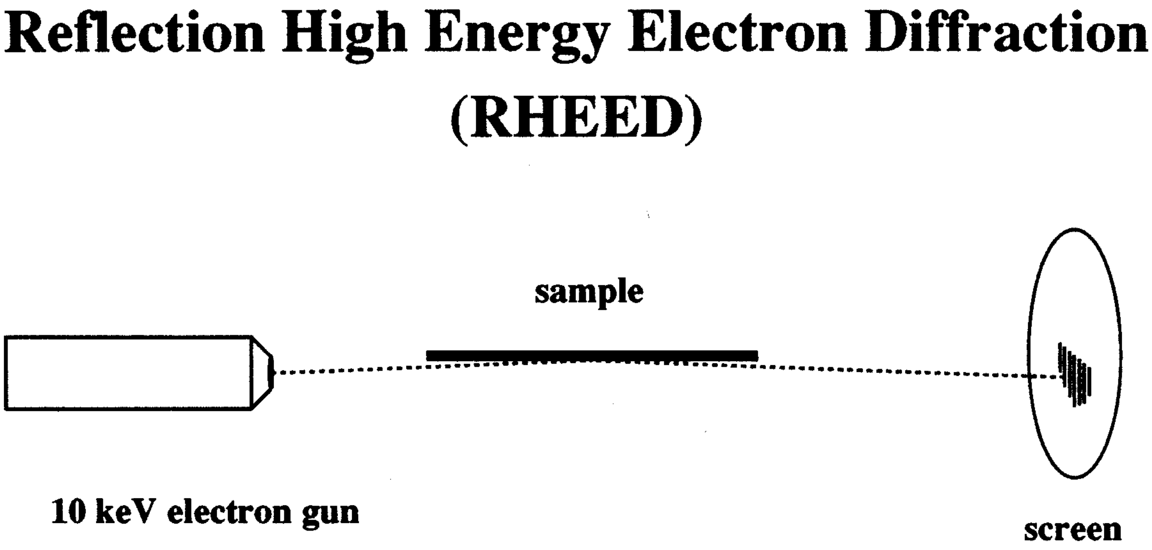
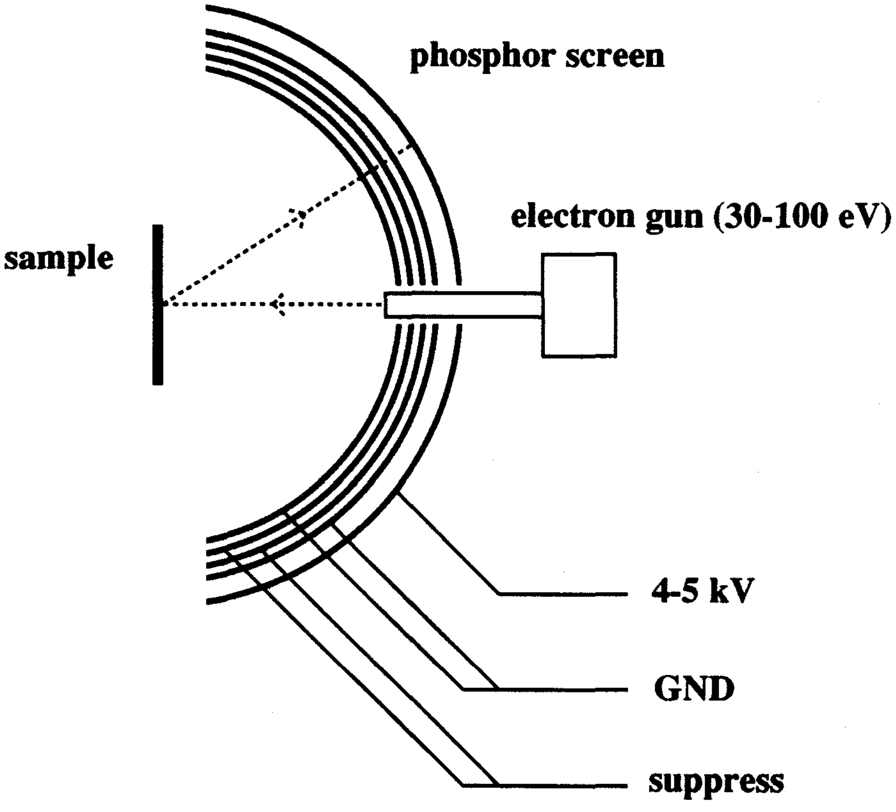


Figure 1.2: RHEED configuration in the Perkin-Elmer (Model 430S) Si MBE system. A 10 keV electron beam is incident at glancing angle on the surface of the sample. Diffracted beams strike a phosphor screen positioned on the opposite side of the chamber to the electron gun. The resulting pattern can be used to identify surface symmetries and otherwise provide *in situ* sample characterization.



Low Energy Electron Diffraction (LEED) (reverse view)

Figure 1.3: LEED configuration in the Si-silicide MBE system. A 30-100 eV electron beam is incident normally to the substrate surface. Elastically scattered electrons are accelerated into a phosphor screen and produce a pattern. Surface symmetries can be readily determined from the patterns. Unfortunately, the geometry of the reverse-view technique does not allow simultaneous deposition and characterization like RHEED.

selected and accelerated into a phosphor screen located around the snout of the electron gun. Since the beam energy in LEED is so low, considerable care is taken to shield the optics from stray magnetic fields. In contrast with RHEED, LEED patterns from clean, crystalline surfaces show sharp spots. Although simultaneous deposition and characterization are not possible with reverse-view LEED, surface symmetries are readily determined without rotation of the sample, as required by RHEED.

Although a detailed theoretical analysis of RHEED and LEED patterns is beyond the scope of this thesis, a summary of the most important ideas is presented here. For a more complete treatment of the theory of electron diffraction, the reader is encouraged to refer to Refs. [12] and [13]. Following Ashcroft and Mermin,[14] we define $\vec{k}$ such that

$$\vec{k} = \vec{k}_{out} - \vec{k}_{in} \tag{1.1}$$

where $\vec{k}_{out}$ and $\vec{k}_{in}$ are the wave vectors of the incoming and outgoing electrons, respectively. The diffraction condition for elastically scattered electrons requires that $|\vec{k}|$ must be equal to a reciprocal lattice vector, $\vec{G}$. Suppose we draw the vector $\vec{k}_{in}$ properly oriented in reciprocal space, locating its tail at the origin. Now, the intersection of the reciprocal lattice with a sphere centered about the tip of $\vec{k}_{in}$ of radius $|\vec{k}_{in}|$ satisfies the diffraction condition. This construction is due to Ewald.[14]

To understand the origins of RHEED and LEED patterns, remember that since these techniques are extremely surface-sensitive, the reciprocal lattice is the three-dimensional extension of the two-dimensional surface, reciprocal lattice. As a result, the reciprocal lattice must be thought of as a two-dimensional array of rods. In RHEED, since the electrons are incident on the sample at glancing angle, the intersection of the reciprocal lattice with the Ewald Sphere produces a streaked pattern. Variations in intensity along a particular streak yield information on the planarity of the surface. For instance, rough surfaces have spotty RHEED patterns. In LEED, the Ewald Sphere intersects reciprocal space perpendicular to the elongated rods of the reciprocal lattice. For this reason, LEED produces patterns of spots from which considerable information can be obtained.[15]

1.2.4 Doping

Unfortunately, doping with Si MBE is a significant problem. If the substrate temperature, T_g, is above a critical value dependent on the Si growth rate, doping can be adequately described by first-order kinetic theory. Following Allen and Kasper,[16] the rate of change of the dopant surface concentration is governed by the equation

$$\frac{dN_D}{dt} = F_D - K_d N_D - K_i N_D, \tag{1.2}$$

where F_D is the incoming doping flux and K_d and K_i are coefficients describing desorption and incorporation of the dopant. If we define the sticking coefficient, S, by

$$S = \frac{K_i}{K_i + K_d} \tag{1.3}$$

and the residence time, τ, by

$$\tau = (K_i + K_d)^{-1}, \tag{1.4}$$

then the steady-state dopant concentration in the growing crystal, N_{bulk}, is given in terms of the Si flux, F_{Si}, and the number density of atoms in the crystal, N_0, by the equation

$$N_{bulk} = S\frac{F_D}{F_{Si}}N_0. \tag{1.5}$$

If the dopant flux is shuttered off, Eq. 1.2 becomes

$$\frac{dN_D}{dt} = -\frac{N_D}{\tau} \tag{1.6}$$

and $N_D(t)$ decays exponentially at a rate proportional to $e^{-\frac{t}{\tau}}$. Therefore, to produce sharp profiles with high dopant densities, we need to keep S high and τ low. Unfortunately, residence times for the typical n-type Si dopants (Ga and Sb) are too long and sticking coefficients are too low to produce the desired profiles. Doping a semiconductor p-type with elemental boron apparently does not suffer from these problems, as recent results have demonstrated 100% activation for doping levels up to $2 \times 10^{20}\,\mathrm{cm}^{-3}$ with a profile abruptness of 20 Å/decade.[17]

Fortunately, several approaches have been at least partially successful in circumventing the problems with n-type doping. One approach is based upon the hope that the equilibrium state can be quickly reached, once growth of a new layer begins.[18] When switching to an n-type layer, a predeposit of dopant is applied prior to opening the Si shutter. Determination of the amount of surface concentration necessary to result immediately in steady-state growth is difficult since the amount is strongly dependent on growth temperature, growth rate, and desired doping concentration. When growth of the n-type layer is complete, both dopant and Si flux are interrupted and the temperature of the sample is taken high enough to "flash off" the dopant remaining on the surface. Then, the growth temperature is reduced and the next layer can begin. From a practical point of view, this technique does not allow complicated structures to be grown since each n-type layer would take approximatedly 20 min just to predeposit and flash off the dopant.

Recently several authors have reported success with n-type doping at low growth temperatures.[19, 20] Segregation of dopants to the growth surface is suppressed at low temperatures since atoms cannot diffuse a great distance before the next monolayer of Si is deposited. Unfortunately, low-temperature growth also inhibits the crystallization of Si, producing defective material. As a result, crystal quality is sacrificed at the expense of hyperabrupt doping profiles. Nonetheless, useful devices can still be fabricated.[21]

Lastly, high doping levels and abrupt profiles have been demonstrated through the use of low-energy ion implantation (I^2 MBE). For example, Houghton *et al.*[22] have reported 100% activation of As, implanted as As^+ in Si at energies between 500 and 1000 keV with doping levels as high as $10^{20}\,cm^{-3}$ and profile abruptness near 100 Å/decade. The technique avoids problems associated with segregation since the dopants are implanted a few monolayers into the growing film. At high doping levels, some crystal damage may occur, requiring a high-temperature anneal to restore crystalline quality. Although the technique appears promising, the necessary equipment is expensive and must be made more reliable before it comes into widespread use.[23]

1.3 Strain and the Concept of Critical Thickness

1.3.1 Theories of Critical Thickness

Through the use of MBE, strained epitaxial structures consisting of lattice mismatched materials can be grown. If the lattice constant parallel to the surface of the epitaxial film ($a_\parallel$) is equal to that of the substrate, the growth is said to be commensurate, and the interface between the film and the substrate is described as coherent. This behavior has been observed for the $GaAs_{1-x}P_x/GaAs$,[24]-[27] $Si_{1-x}Ge_x/Si$,[28, 29] and $In_xGa_{1-x}As/GaAs$[27] strained-layer systems. Because of the increasing importance of Si-based devices and the relatively well-understood nature of Si-based chemistry, the $Si_{1-x}Ge_x/Si$ strained-layer material system has recently emerged as the model system for studying relaxation behavior.[30]-[32] For $Si_{1-x}Ge_x$ alloys on Si, the mismatch varies roughly linearly with Ge concentration up to 4.18%. In Fig. 1.4, schematic diagrams depicting the structural effect upon the crystalline lattice of $Si_{0.5}Ge_{0.5}$ coherently strained to an infinitely thick (100) Si substrate and a relaxed Ge film on an identical substrate are presented. The unit cell of the $Si_{0.5}Ge_{0.5}$ layer is compressed biaxially so that the lattice constant parallel to the interface, $a_{\parallel}$, has decreased, relative to its relaxed value, and takes on the value of the substrate. Conversely, the lattice constant perpendicular to the interface, $a_{\perp}$, increases, relative to its relaxed value producing a tetragonal distortion of the unit cell. Therefore, measurement of $a_{\parallel}$ and $a_{\perp}$ reveals information about the nature of the strain distribution in the epilayer. An introduction to the measurement of $a_{\parallel}$ and $a_{\perp}$ from <100>-oriented films on (100) substrates is presented in Section 1.3.2.

Previous studies of commensurate growth of a crystalline film on a lattice mismatched substrate have led to the concept of a "critical thickness," with critical thickness being loosely defined as the thickness where strain relaxation by dislocation formation becomes dramatically accelerated. In practice, however, the process of relaxation in these structures depends upon a large number of parameters, resulting in a variety of relaxation behaviors varying from very abrupt to quite gradual transitions. Initial theories of critical thickness were evaluated on the basis of simple energy considerations and assumed that the as-grown structure would relax to the thermal equilibrium state. Ideally, the relaxed film would contain a concentration of misfit dislocations dependent upon the lattice mismatch between the film and the substrate. Van der Merwe[33] bases his theory upon the idea that the areal strain energy of a strained epitaxial layer will increase until it becomes energetically favorable for the film to relax. As a

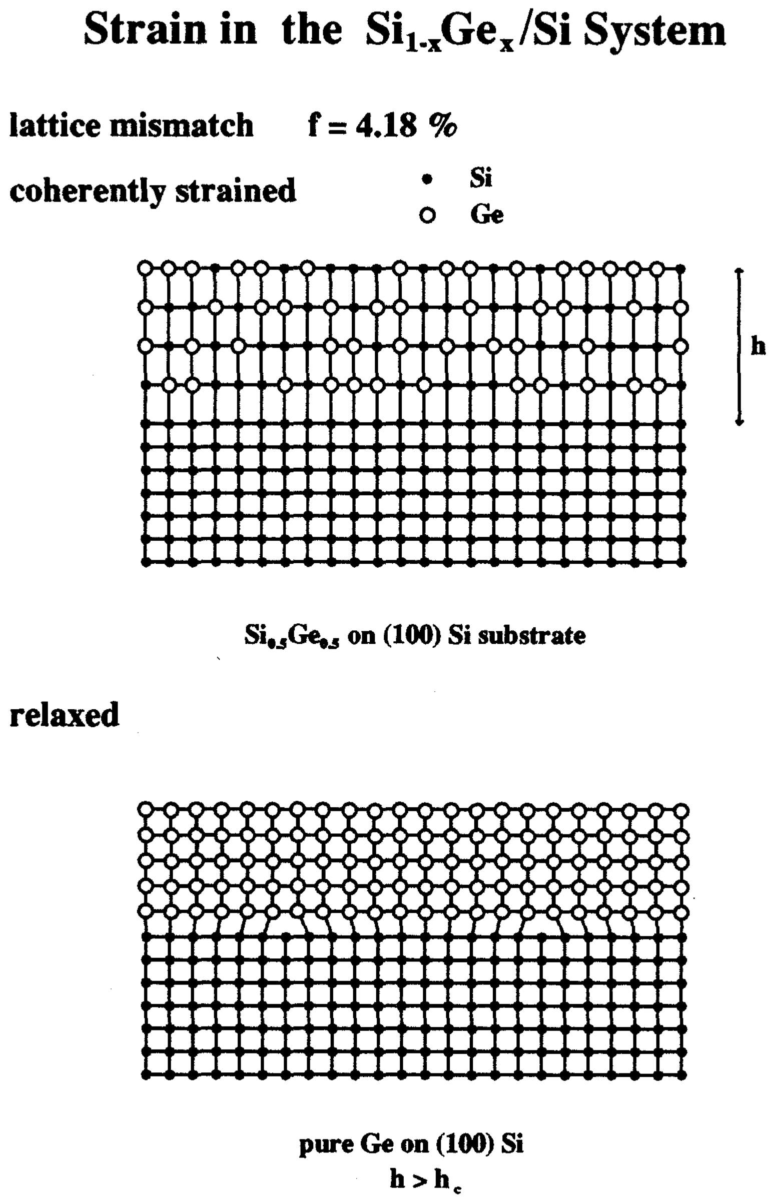


Figure 1.4: (a) Schematic diagram showing the tetragonal distortion resulting from commensurate growth of $Si_{0.5}Ge_{0.5}$ on an infinitely thick (100) Si substrate. The epilayer is said to be coherently strained. (b) Situation for a Ge film grown on (100) Si to a thickness $h > h_c$. Two misfit dislocations are present in the figure and contribute to strain relaxation.

function of thickness, h, the expression for the areal strain energy based upon continuum elastic theory is given by[34, 35]

$$E_S = 2G\left(\frac{1+\nu}{1-\nu}\right) f^2 h. \tag{1.7}$$

In this equation, f is the mismatch, G is the shear modulus, and ν is Poisson's ratio. The areal energy associated with a relaxed film containing strain-relieving dislocations is given in terms of the energy per unit length of a misfit dislocation,*

$$E_d = \frac{Gb^2}{4\pi}\left(\frac{1-\nu\cos^2\beta}{1-\nu}\right)\ln\left(\frac{\rho h}{b}\right), \tag{1.8}$$

by

$$E_D = \left(\frac{2f}{b\sin\beta\cos\gamma}\right) E_d. \tag{1.9}$$

The variable ρ is actually a constant of integration and is generally taken to be 4.[34] If we equate the expressions in Eqs. 1.7 and 1.9, the critical thickness is given implicitly by

$$f = \frac{b(1-\nu\cos^2\beta)}{4\pi h_{c1}(1+\nu)\sin\beta\cos\gamma}\ln\left(\frac{\rho h_{c1}}{b}\right). \tag{1.10}$$

A slightly different approach was employed by Matthews and Blakeslee.[36] This theory assumes that grown-in threading dislocations already exist in the epitaxial layer, and if the tension on a dislocation line is greater than the force exerted on the line by misfit stress, then the threading arm will propagate and the misfit dislocation line will extend, causing relaxation. The thickness at which this occurs is equated with the critical thickness. The expression[30]

$$f = \left(\frac{b}{h_{c2}}\right)\left(\frac{1}{4\pi(1+\nu)}\right)\left(\ln\left(\frac{h_{c2}}{b}\right)+1\right) \tag{1.11}$$

---

*The parameters b, β, and γ describe the magnitude of the Burger's vector, the angle between the Burger's vector and the dislocation line, and the angle between the interface and the plane in which the dislocation moves (the glide plane), respectively.

is obtained under these assumptions and results in critical thicknesses approximately equal to those of Van der Merwe[33] ($h_{c1} \approx h_{c2}$).

Unfortunately, neither of these theories adequately describes observed critical thicknesses. To account for this discrepancy, a third theory was proposed by People and Bean.[30] In their theory, the film is initially assumed to be free of threading dislocations. Interfacial misfit dislocations are "spontaneously" generated when the areal strain-energy density exceeds the self-energy of an isolated dislocation. Values for the critical thickness were calculated for both screw and edge-type dislocations. Assuming a value for Poisson's ratio, $\nu \sim 0.3$, and the magnitude of the Burger's vector, $b \sim 4\,\text{Å}$, People and Bean derive

$$h_{c3} = \left(\frac{1.9 \times 10^{-2}\,\text{Å}}{f^2}\right) \ln\left(\frac{h_{c3}}{4\,\text{Å}}\right) \tag{1.12}$$

for screw dislocations. For comparison, Eqs. 1.10, 1.11, and 1.12 are plotted in Fig. 1.5 against experimental results for $\mathrm{Si}_{1-x}\mathrm{Ge}_x$ on Si(100).[37] The values for the parameters $b = 3.84\,\text{Å}$, $\beta = 60\,°$, $\gamma = 35.3\,°$, and $\nu = 0.3$ were chosen for edge-type dislocations in Si.[34] Although the theory of People and Bean appears successful, it does not account for the mechanism that generates these strain-relieving dislocations. Even today, the point is still a controversial matter.

1.3.2 Measuring Strain with X-ray Diffraction

We have used high-resolution x-ray diffraction (HRXRD) and θ-2θ x-ray diffraction (θ-2θ XRD) to measure $a_\perp$ and $a_\parallel$ in $\mathrm{Si}_{1-x}\mathrm{Ge}_x$ alloys and superlattices strained to (100) Si in order to determine strain distributions in the epilayers. The measurements are straightforward for <100>-oriented cubic crystals. As indicated previously, biaxial stress arising from the requirement that atoms in the epilayer must be in registry with the substrate forces a tetragonal distortion on the cubic unit cell. As a result, for Bragg planes at an angle to the surface, both

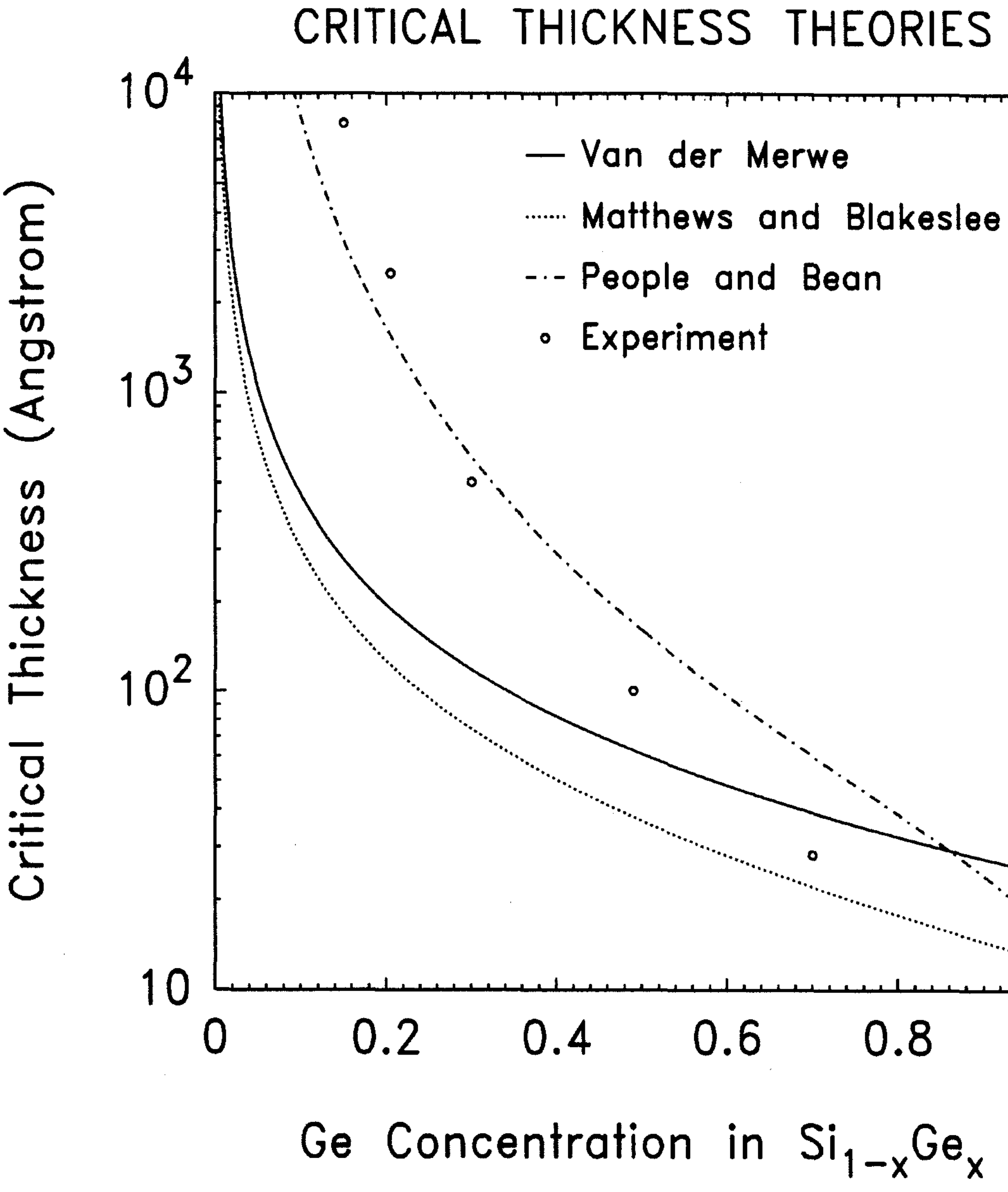


Figure 1.5: Plot of critical thickness as a function of Ge concentration according to several theoretical models. Early models attributed to Van der Merwe[33] and Matthews and Blakeslee[36] were based on equilibrium arguments and severely understated observed critical thicknesses. The more recent model of People and Bean[30] agrees well with experiment but has questionable physical basis.

the spacing between planes, d, and the angle with respect to the surface of these planes, ϕ, will differ from their corresponding values in the substrate. In practice, d is determined by Bragg's Law

$$2d\sin\theta = n\lambda, \tag{1.13}$$

where λ is the x-ray wavelength and θ is the angle of incidence measured with respect to the diffracting planes. Two angular measurements are required from which the two lattice constants can be calculated.

The reciprocal lattice vector, $\vec{G}$, corresponding to (hkl) planes in <100>-oriented crystals is given by

$$\vec{G} = 2\pi\left[\frac{h}{a_\perp}\hat{h} + \frac{k}{a_\parallel}\hat{k} + \frac{l}{a_\parallel}\hat{l}\right]. \tag{1.14}$$

Since the interplanar spacing is given by $\frac{2\pi}{|\vec{G}|}$, it can be expressed through the use of Eq. 1.14 in terms of $a_\parallel$ and $a_\perp$ by

$$d = \frac{a_\parallel a_\perp}{h\sqrt{k^2+l^2}}\frac{1}{\sqrt{\left(\frac{a_\perp}{h}\right)^2 + \frac{{a_\parallel}^2}{k^2+l^2}}}. \tag{1.15}$$

As indicated earlier, the diffracting plane (hkl) makes an angle, ϕ, with respect to the surface. Now, consider the projection of $\vec{G}$ on the surface. Since $\vec{G}$ is perpendicular to the diffracting plane, the angle between $\vec{G}$ and its projection onto the surface, $\vec{P}$, is exactly ϕ. From the dot product, $\vec{P}\cdot\vec{G}$, expressions for $\sin\phi$ and $\cos\phi$ can be easily derived in terms of $a_\perp$, $a_\parallel$, and d. First, $\vec{P}$ is given by

$$\vec{P} = 2\pi\left[\frac{k}{a_\parallel}\hat{k} + \frac{l}{a_\parallel}\hat{l}\right]. \tag{1.16}$$

In terms of the dot product, $\sin\phi$ can be written as

$$\sin\phi = \frac{\vec{P}\cdot\vec{G}}{|\vec{P}|\,|\vec{G}|}. \tag{1.17}$$

Also,

$$\vec{P} \cdot \vec{G} = (2\pi)^2 \left[\frac{k^2 + l^2}{{a_{\parallel}}^2} \right] \tag{1.18}$$

and

$$\left|\vec{P}\right| \left|\vec{G}\right| = \frac{(2\pi)^2 \sqrt{k^2 + l^2}}{a_{\parallel} d}. \tag{1.19}$$

Substitution of Eqs. 1.18 and 1.19 into Eq. 1.17 yields

$$\sin\phi = \frac{d\sqrt{k^2 + l^2}}{a_{\parallel}} \tag{1.20}$$

and

$$\cos\phi = \frac{dh}{a_{\perp}}. \tag{1.21}$$

From these equations and Bragg's Law, $a_{\perp}$ and $a_{\parallel}$ are derived in terms of ϕ and θ, the two unknowns:

$$a_{\perp} = \frac{\lambda h}{2\sin\theta\cos\phi} \tag{1.22}$$

$$a_{\parallel} = \frac{\lambda\sqrt{k^2 + l^2}}{2\sin\theta\sin\phi}. \tag{1.23}$$

Since there are two unknowns, two measurements are needed to determine $a_{\perp}$ and $a_{\parallel}$ uniquely. Let α and β equal $\theta + \phi$ and $\theta - \phi$, respectively. In practice, a diffracting plane is chosen (typically (422) or (440) in $\mathrm{Si}_{1-x}\mathrm{Ge}_x$) and the two quantities, α and β, are measured for the epilayer with respect to the substrate. In the so-called forward-scattering geometry, one measures

$$\Delta\alpha \equiv \alpha_{\mathrm{SUB}} - \alpha_{\mathrm{EPI}} \tag{1.24}$$

and in the reverse geometry,

$$\Delta\beta \equiv \beta_{\mathrm{SUB}} - \beta_{\mathrm{EPI}}. \tag{1.25}$$

A diagram elucidating the two geometries is shown in Fig. 1.6. Once $\Delta\alpha$ and $\Delta\beta$ have been measured, θ and ϕ can be calculated from

$$\theta_{\mathrm{EPI}} = \theta_{\mathrm{SUB}} - \frac{\Delta\alpha + \Delta\beta}{2} \tag{1.26}$$

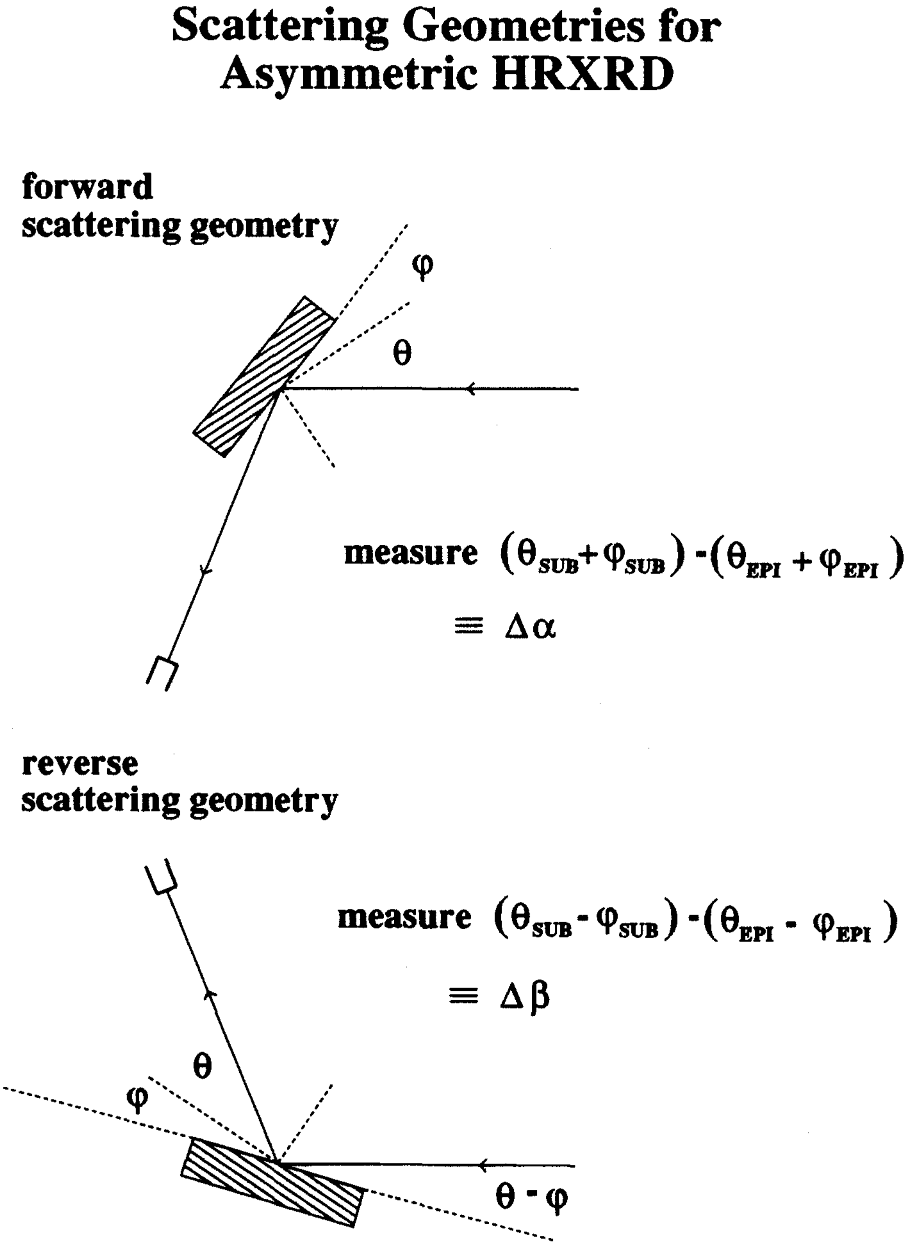


Figure 1.6: Forward and reverse scattering geometries for asymmetric measurements of $a_\perp$ and $a_\parallel$ through the use of high-resolution x-ray diffraction (HRXRD). In the forward (reverse)-scattering geometry, the difference of the angle $\theta + \phi$ $(\theta - \phi)$ between the substrate (SUB) and the epilayer (EPI) is measured. From these data, θ_{EPI} and ϕ_{EPI} can be calculated from the known values of θ_{SUB} and ϕ_{SUB}.

and

$$\phi_{\rm EPI} = \phi_{\rm SUB} - \frac{\Delta\alpha - \Delta\beta}{2}. \qquad (1.27)$$

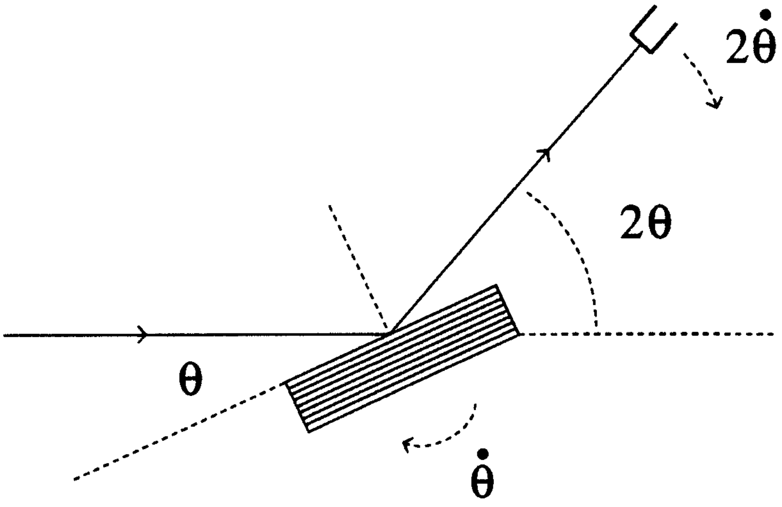
Finally, $a_\perp$ and $a_\parallel$ are obtained using Eqs. 1.22 and 1.23. $a_\perp$ can also be measured using the symmetric (400) Bragg reflection. In this case, $\phi = 0$ and the epilayer must be assumed to be coherently strained (*i.e.*, $a_\parallel \equiv a_0$); therefore, $\theta_{\rm SUB} - \theta_{\rm EPI}$ is directly measured and $a_\perp$ can be calculated from Bragg's Law.

Actual measurements of angles in the two techniques differ considerably and should be addressed. In HRXRD, a detector is placed near the expected angle (with respect to the incident beam) for the $n = 1$ Bragg reflection from the substrate, and the sample is rotated through the correct Bragg condition. Both symmetric and asymmetric measurements can be made with this technique. For the case of θ-2θ XRD, the incident beam remains fixed, while the sample rotates at $\dot{\theta}$ and the detector scans at $2\dot{\theta}$. In principle, θ-2θ XRD can be used to perform both symmetric and asymmetric measurements; however, for the samples we studied, accurate measurements of the lattice constants required the higher resolution of the HRXRD technique. The geometry for symmetric θ-2θ XRD is shown in Fig. 1.7.

1.4 Determining Band Offsets by XPS

In Chapter 3, we measure the strain dependence of the (100) Si/Ge valence band offset using x-ray photoelectron spectroscopy (XPS), otherwise known as electron spectroscopy for chemical analysis (ESCA). Samples are irradiated in UHV with a monoenergetic beam of Al K_α x-rays ($h\nu = 1486.6$ eV) to induce electron emission from the first few tens of Angstroms into the surface (see Fig. 1.8(b)). The emitted electrons are subsequently analyzed with an electron spectrometer to measure their kinetic energies. Our present capabilities allow UHV

Geometry for Symmetric
θ-2θ XRD



sample rotated at $\dot{\theta}$

detector scanned at $2\dot{\theta}$

$\Delta\theta \equiv \theta_{SUB} - \theta_{EPI}$ is measured directly

Figure 1.7: Scattering geometry for θ-2θ x-ray diffraction (θ-2θ XRD). The substrate is rotated at $\dot{\theta}$ while the detector is scanned at $2\dot{\theta}$. The difference in scattering angle between the substrate and the epilayer is measured directly, immediately giving θ_{EPI} if θ_{SUB} is known.

transfer of samples grown in one of three MBE growth chambers. As a result, atomically smooth semiconductor heterojunctions, free from atmospheric contamination, can be studied *in situ*.

The kinetic energies of emitted electrons depend upon the binding energy of the electron state from which they were scattered according to the equation[38]

$$E_{\text{kinetic}} = h\nu - E_{\text{binding}} - \phi_s, \tag{1.28}$$

where ϕ_s is defined as the spectrometer work function. A spectrum obtained by plotting counts as a function of binding energy can be compared to standard spectra[38] for each of the elements of the periodic table, allowing the constituents of the surface to be identified. In addition, surface states can be identified from any shifts in the binding energies of the atomic core levels. Finally, for semiconductor materials, the valence-band edge can be determined through a careful analysis of electrons with binding energies near the band-gap energy.*

In practice, the valence-band edge must be measured with respect to a core level since the spectrometer work function is not well known. Fig. 1.8(a) diagrams the relative positions of the valence-band edges and core levels for a heterojunction between two semiconductors, A and B. If the samples are lattice-matched, a single thin sample of material A on B or material B on A would suffice, and the valence band offset could be determined from a single scan. Since most of the semiconductor heterojunctions in which we are interested are lattice-mismatched, any measurement of the valence band offset must consider strain effects on the core levels. In practice, the offset is measured as a function of strain, requiring a large number of samples to be grown. Fig. 1.8(c) summarizes the sample set needed for this measurement.

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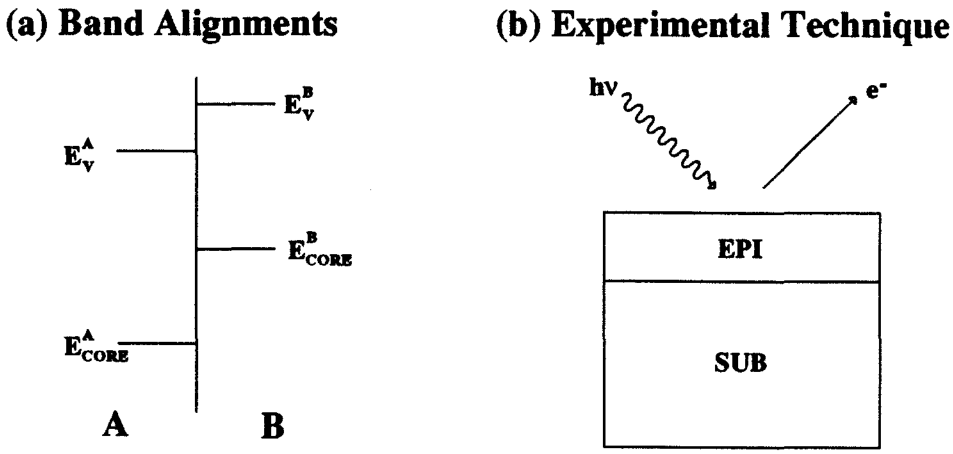
*In general, the binding energy of an electron emitted from the top of the valence band would roughly equal the Fermi energy measured with respect to the valence-band edge.

Measuring Band Offsets with XPS

(for semiconductors A and B with lattice mismatch f)



(c) Required Sample Set

I. Strained A on A-rich $A_{1-x}B_x$ buffers
Measure $E^A_{CORE} - E^A_V$

II. Strained B on B-rich $A_{1-x}B_x$ buffers
Measure $E^B_{CORE} - E^B_V$

III. Strain-symmetrized A/B superlattices on $A_{1-x}B_x$ buffers
Measure $E^A_{CORE} - E^B_{CORE}$

$$\Delta E_V = (E^B_{CORE} - E^B_V) + (E^A_{CORE} - E^B_{CORE}) - (E^A_{CORE} - E^A_V)$$

Figure 1.8: (a) Valence-band and core-level alignments at a heterojunction between semiconductors A and B. (b) Experimental technique of x-ray photoelectron spectroscopy (XPS). Incident x-rays of energy $h\nu$ scatter electrons from the epilayer and into a spectrometer which measures their kinetic energy. (c) For heterojunctions between two lattice-mismatched semiconductors, three sets of samples are needed to consider strain effects on the band structures properly. From the data, the valence band offset, ΔE_v, can be calculated.

First, thin ($h < h_c$) films of material A are grown coherently strained to unstrained, A-rich, $A_{1-x}B_x$ substrates (or relaxed buffer layers). From these samples, the strain dependence of the energy of a core level is measured with respect to the valence-band edge in material A ($E^{A}_{\mathrm{CORE}} - E^{A}_{v}$). Similarly, $E^{B}_{\mathrm{CORE}} - E^{B}_{v}$ is determined as a function of strain from samples of material B grown coherently strained to B-rich, $A_{1-x}B_x$ substrates. The strain distribution in each of the samples is determined through HRXRD, using techniques previously discussed in Section 1.3 Finally, strain-symmetrized A/B superlattices grown on $A_{1-x}B_x$ substrates are used to determine the strain dependence of the energy separation between the core levels of the two constituent materials. The top layer of the superlattice is chosen to be thinner than the electron-escape depth so that electrons emitted from both materials can be analyzed simultaneously. The total thickness of the superlattice is chosen to be several thousand Angstroms to facilitate strain measurements by HRXRD. With this technique, the valence band offset as a function of strain is calculated from

$$\Delta E_v = (E^{B}_{\mathrm{CORE}} - E^{B}_{v}) + (E^{A}_{\mathrm{CORE}} - E^{B}_{\mathrm{CORE}}) - (E^{A}_{\mathrm{CORE}} - E^{A}_{v}). \qquad (1.29)$$

1.5 Characterization of Electronic Devices

Two-terminal devices consisting of mesa structures fabricated from some of the samples grown for this thesis were studied to determine their electrical properties. DC I–V curves and $\frac{d^2I}{dV^2}$-V inelastic electron tunnelling spectra (IETS) were obtained for the structures studied in Chapter 7. Presented here is an introduction to these measurements. Emphasis is placed on describing the techniques.

1.5.1 *I–V* Measurements

The DC *I–V* measurement is a useful characterization of two-terminal electronic devices. For instance, the quality of a *p-n* junction can be characterized through a study of the breakdown voltage and the reverse-bias, leakage current obtained from the *I–V* curves.[39] Our *I–V* measurements were performed with a Hewlett Packard (Model 4145) parametric analyzer. The unit contains four stimulus/measurement units (SMUs), two voltage sources, and two voltage monitors. The SMUs are capable of simultaneously sourcing and sensing currents and voltages of ±100 mA or ±100 V up to a maximum power of 2 Watts. In addition, the data can be stored digitally and analyzed later with a computer.

I–V curves from two-terminal devices are typically measured through the use of the 2, 3, and 4-point contacting schemes outlined in Fig. 1.9. A thin metallic layer (usually Au or Au/Ge alloy) is evaporated onto the sample and mesa structures are fabricated using standard photolithograpic techniques and wet chemical etching (see Section 7.3.2). In the 2-point measurement (Fig. 1.9(a)), two contacts are used. The sample is secured on an 8-pin header with silver paint to contact the backside. Then, a thin (25 μm) Al wire is bonded between the device and a post, making contact with the top of the device. For the 2-point measurement to be accurate, the device resistance must be much larger than the total series resistance of the circuit; otherwise, the measured voltage drop will reflect these additional resistances. In the 3-point measurement (Fig. 1.9(b)), contact to a second device eliminates any series resistance that is due to the substrate, since the voltage across the active device can be measured with respect to the second device. Finally, in the 4-point measurement, a second contact (Fig. 1.9(c)) added to the active device eliminates any series resistance between the device and the voltage or current source. We found significant effects that were due to series resistances in our devices could be minimized through the use of the 4-point contacting scheme.

1.5.2 Inelastic Electron Tunnelling Spectroscopy

Features visible in the I–V curves of tunnelling devices can be enhanced through the process of taking derivatives. Unfortunately, numerical differentiation of the I–V curves also enhances noise, which tends to be relatively high in DC measurements. One solution to this problem is to use modulation techniques. Following Ref. [40], a small AC voltage, $v_\omega \sin\omega t$, superimposed on a DC voltage, V_0, is applied across a device having a nonlinear current-voltage characteristic given by $I(V)$. Expanding into a Taylor series, the current, $I(t)$, becomes

$$I(t) = I(V_0) + \frac{dI}{dV}(V_0)v_\omega \sin\omega t + \frac{1}{2}\frac{d^2I}{dV^2}(V_0)v_\omega^2 \sin^2\omega t + \cdots. \tag{1.30}$$

From Eq. 1.30, the amplitude of the current at the fundamental frequency is just

$$\frac{dI}{dV}(V_0)v_\omega \tag{1.31}$$

from which $\frac{dI}{dV}$ at V_0 can be obtained. By expanding the $\sin^2\omega t$ in Eq. 1.30, we can see that the amplitude of the second harmonic contribution to the current is given by

$$-\frac{1}{4}\frac{d^2I}{dV^2}(V_0)v_\omega^2. \tag{1.32}$$

In practice, however, it is not possible to apply a pure frequency to the sample. As a result, the Fourier spectrum of the voltage actually applied may contain components at frequencies ω, 2ω, 3ω, etc. Therefore, the total contribution to the amplitude of the current at frequency 2ω is the sum of the second harmonic contribution from v_ω and the first harmonic contribution from $v_{2\omega}$

$$I_{2\omega} = -\frac{1}{4}\frac{d^2I}{dV^2}v_\omega^2 + \frac{dI}{dV}v_{2\omega}. \tag{1.33}$$

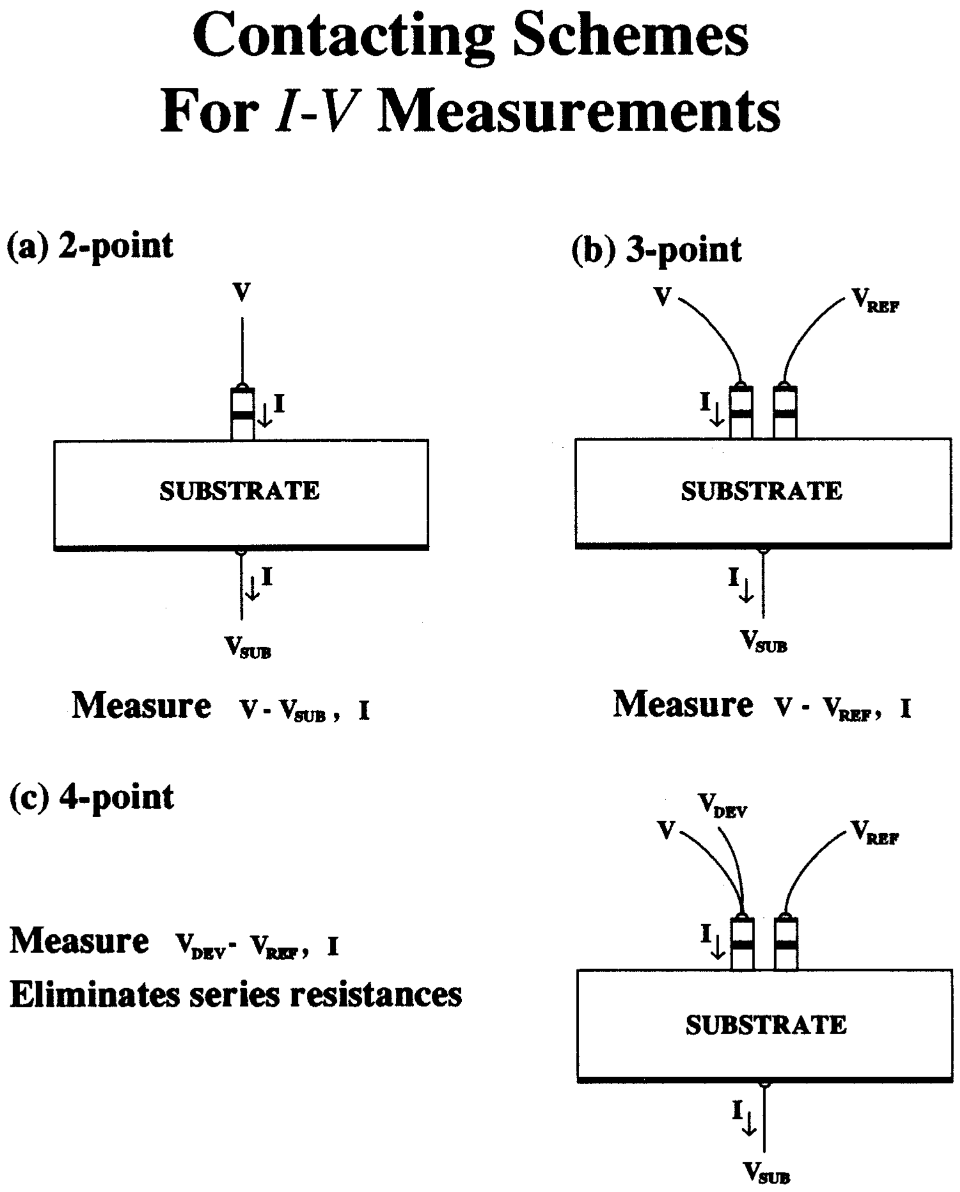


Figure 1.9: (a) Contacting scheme for the 2-point *I–V* measurement. The 2-point measurement should be used only if the device resistance is large compared to any series resistances. (b) The substrate series resistance can be eliminated if a second device is contacted and the voltage is measured with respect to this device. (c) A fourth contact can be used to eliminate any series resistances between the device and the current or voltage source.

Since $v_{2\omega}$ is also being applied across the linear elements in the circuit, which are in parallel with the device,

$$I_{2\omega} = -\frac{v_{2\omega}}{Z}, \tag{1.34}$$

where Z is the impedance of the rest of the circuit. Finally, the circuit is tuned so that at 2ω, Z becomes infinite and the amplitude of the signal becomes

$$v_{2\omega} = \frac{1}{4}\frac{dV}{dI}\frac{d^2I}{dV^2}v_{\omega}^2. \tag{1.35}$$

If $\frac{dI}{dV}$ does not vary significantly over the range of voltages observed, then we can obtain $\frac{d^2I}{dV^2}$ from a measurement of $v_{2\omega}$, using Eq. 1.35, since we know v_{ω}. In this way, we were able to obtain the second derivative spectra presented in Chapter 7.

1.6 Outline of Thesis

The remainder of the thesis is organized as follows. In Chapter 2, $Si_{1-x}Ge_x$ alloys and $Si_{1-x}Ge_x/Si$ superlattices, grown at extremely low temperatures ($\approx$ 365 °C) and coherently strained to (100) Si substrates, are studied using θ-2θ XRD as a function of *ex situ* anneal treatment. Significant relaxation is observed to occur at temperatures as low as 400 °C. A 2 h anneal at a temperature of 700 °C, considered long enough to allow for complete relaxation, reveals that alloys relax more fully than superlattices of the same average composition. In addition, we have determined that the process of relaxation can be described by first-order kinetics and have experimentally determined the activation energy for the process to be approximately 2.0 eV.

Chapter 3 describes a study of the strain dependence of the (100) Si/Ge valence band offset, providing the most definitive measurement to date on this important device parameter. Si 2*p* and Ge 3*d* core-level energy separations and core level to valence-band edge energies are measured as a function of strain. Strain configurations are determined *ex situ* through the use of HRXRD. From our results, the valence band offset for Ge strained to (100) Si and Si strained to (100) Ge is calculated to be 0.83 ± 0.11 eV and 0.22 ± 0.13 eV, respectively.

In addition, two studies pertaining to segregation and ordering effects in $Si_{1-x}Ge_x$ alloys are presented in Chapters 4 and 5. First, Chapter 4 reports the observation of segregation in $Si_{1-x}Ge_x$ alloys through the use of HRXRD. In the study, $Si_{1-x}Ge_x$ alloys grown coherently strained on (100) Si to thicknesses exceeding the critical thickness for growth at 550 °C[30] are shown to have segregated into several layers of different composition. Chapter 5 describes the first observation of a (2×8) surface reconstruction on (100) $Si_{1-x}Ge_x$, using RHEED and LEED surface-analysis techniques. The reconstruction is observed as a function of temperature to be a thermodynamically stable phase in which Ge dimers may be ordering along the direction of the (2×1) reconstruction normally seen on (100) Si surfaces.

Presented in Chapter 6 is a study of the growth of superconducting V_3Si on (111) Si through the use of MBE techniques. Si and V are codeposited on clean (111) Si surfaces at various temperatures. Growth at 400 °C is shown to minimize reaction with the Si substrate while still allowing nucleation of the superconducting *A*15 phase of V_3Si. Auger sputter-depth profiling and transmission electron microscopy (TEM) are used to confirm this result. In addition, structural analysis of superconducting films with TEM demonstrates that the superconducting films consist of columnar, polycrystalline grains approximately 200 Å in diameter.

Finally, we report an electrical characterization of the first p-$Si_{1-x}Ge_x$/n-Si heterojunction interband-tunnel (HIT) diodes in Chapter 7. Equilibrium band-bending calculations predict a decrease in the tunnelling distance as a function of Ge concentration in the $Si_{1-x}Ge_x$ alloy layers. At fixed doping levels, the current-voltage relationship obtained from two-terminal p-Si$_{1-x}$Ge$_x$/n-Si diodes show enhanced negative differential resistance (NDR) with increasing Ge concentration, in support of our band-bending calculations. In addition, $\frac{d^2I}{dV^2}$ spectra from these samples reveal previously unobserved phonon peaks. An interpretation of the origin of these features is presented.

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Chapter 2

Kinetics of Strain Relaxation in $Si_{1-x}Ge_x$ Alloys and $Si_{1-x}Ge_x/Si$ Superlattices

2.1 Introduction

2.1.1 Background

The $Si_{1-x}Ge_x/Si$ material system has recently emerged as the model for studying relaxation behavior in strained-layer heterostructures, which is due to its moderate lattice mismatch ($\approx 4.18\%$ for Ge/Si pseudomorphic growth) and relatively simple growth dynamics. Epitaxial $Si_{1-x}Ge_x/Si$ heterostructures[1]-[3] have been reported to grow coherently strained on (100) Si with thicknesses exceeding theoretical predictions based upon equilibrium arguments.[4, 5] In particular, some authors have reported that the onset of relaxation in $Si_{1-x}Ge_x/Si$ strained-layer superlattices (SLS) is strongly dependent on growth temperature.[6, 7] These results suggest that a significant amount of excess strain can be metastably "frozen" into a strained-layer heterostructure before the microscopic mechanisms of relaxation become active. Considerable work remains to be done before an adequate description of relaxation is achieved.

Substantial effort in recent years has focused on understanding the microscopic mechanisms of strain relaxation through defect formation. For example, Fiory *et al.*[8] have investigated relaxation in metastable $Si_{1-x}Ge_x$ films through the use of ion channeling and transmission electron microscopy (TEM). Dislocation formation near the epilayer/substrate interface was shown to cause local strain reduction after a 30 min anneal at 750 °C. Subsequently, Hull *et al.*[9] have observed motion of misfit dislocations in $Si_{1-x}Ge_x$ alloys annealed *in situ* with the aid of TEM. In a later paper, Hull and Bean[10] reported that the relaxation rate of metastable $Si_{1-x}Ge_x$ alloy samples depends strongly on Ge concentration and provide an explanation based upon interactions between dislocations as the films relax. In a related study of $Si_{1-x}Ge_x/Si$ superlattices, Tuppen *et al.*[11] report that interactions between dislocation half-loops and the alternating strain fields in the superlattice provide a further impediment to dislocation formation. These results are used to explain differences in the extent of relaxation between superlattices and alloys.

The preceding results were all obtained from samples grown at higher temperatures (550 – 600 °C) than those used in the present work, and significant relaxation was not observed until the annealing temperature was taken above 650 °C. Our samples were grown at a temperature of approximately 365 °C and relaxed considerably upon annealing at only 370 °C. Through the use of x-ray diffraction (XRD), we have followed the relaxation process as a function of anneal time for both single-layer $Si_{1-x}Ge_x$ alloys and $Si_{1-x}Ge_x/Si$ superlattices. Our results[12, 13] demonstrate that relaxation can be described as a thermally activated, first-order kinetic process with an activation energy close to 2.0 eV, regardless of composition or detailed strain distribution. Interestingly enough, previous studies[14] describe dislocation glide in Si as a thermally activated process and also measure an activation energy near 2.0 eV, suggesting that glide may be the mechanism responsible for limiting strain relaxation. We have also investigated the extent of relaxation in single-layer $Si_{1-x}Ge_x$ alloys and $Si_{1-x}Ge_x/Si$ superlattices with the same average composition after a 2 h anneal at 700 °C. We report that the alloys relax $\sim$ 84% of their coherent strain, while the corresponding superlattices relax only $\sim$ 43%. These results are consistent with the studies performed by Tuppen *et al.*[11]

2.1.2 Outline of Chapter

In this chapter, we report the first quantitive study of strain relaxation kinetics in single-layer $Si_{1-x}Ge_x$ alloys and $Si_{1-x}Ge_x/Si$ superlattices grown at unusually low growth temperatures (365 °C). In Section 2.2, we describe the experimental details pertaining to this work focusing on sample preparation, *ex situ* annealing procedures, and the determination of strain relaxation using XRD. A description of the sample set studied here is presented in Table 2.1. Single-layer $Si_{1-x}Ge_x$ alloys and $Si_{1-x}Ge_x/Si$ superlattices having the same average composition were grown to allow qualitative comparison of relaxation behavior. The results of this work are presented in Section 2.3. The extent of relaxation for a $Si_{0.8}Ge_{0.2}$ alloy film and a $Si_{0.6}Ge_{0.4}/Si$ superlattice both having average composition, $\overline{x} = 20\%$, is presented in Section 2.3.1. In Section 2.3.2, relaxation of a 5000 Å $Si_{0.8}Ge_{0.2}$ alloy is studied as a function of *ex situ* anneal treatment through the use of θ-2θ XRD. Significant relaxation is observed at temperature of only 414 °C. In addition, we describe relaxation as a thermally activated, first-order kinetic process and measure the activation energy for several $Si_{1-x}Ge_x$ alloy layers and a $Si_{1-x}Ge_x/Si$

superlattice in Section 2.3.3. Finally, our results are discussed in detail in Section 2.4, and a chapter summary is given in Section 2.5.

2.2 Experimental

2.2.1 Sample Growth

The samples prepared for this study were grown in a Perkin-Elmer (Model 430S) MBE system. Ge and Si are codeposited from a dual *e*-beam source onto a radiatively heated, Si substrate in an ultrahigh-vacuum (UHV) environment (base pressure $< 8\times10^{-11}$ Torr). For a more detailed description of the deposition system, please refer to Section 1.2.1. All samples were grown at a temperature of 365 °C, measured with the aid of a thermocouple seated against a reflector located inside the heater. Thermocouple temperature was calibrated with an optical pyrometer (Ircon, W-series) and through the *in situ* observation of Au/Si and Al/Si eutectic reactions. Growth temperature is assumed to be accurate to ±20 °C.

Ex situ substrate preparation consisted of chemical degreasing followed by a rinse in de-ionized water. Subsequently, the substrate was dipped in a 50% HF solution and rinsed again just prior to loading into the MBE growth chamber. To prepare an atomically smooth Si starting surface, the substrate temperature was raised to 850 °C, and a slight Si flux (0.1 Å/s) was applied until a (2×1) reconstruction was observed with reflection high-energy electron diffraction (RHEED).[15]-[17] This procedure was used to facilitate the removal of any native oxide remaining on the substrate surface. Finally, a 1000 – 2000 Å thick, pure Si buffer was grown after the substrate temperature was lowered to 700 °C. A sharp (2×1) reconstruction indicative of a clean, atomically smooth, Si starting surface was observed with RHEED after this step.[18]

The $Si_{1-x}Ge_x/Si$ sample set prepared for this study is shown in Table 2.1. Average sample composition and thickness were chosen to place the samples above the empirical critical thickness curve of People and Bean[2] (see Section 1.3.1) for growth at 550 °C. The superlattices, SL1 and SL2, were designed to have the same average properties as sample A2 and to this end, consist of alternating layers of 72 Å $Si_{0.6}Ge_{0.4}$ and 73 Å Si (36 periods). Although our samples would relax considerably during growth at 550 °C,[2] high-resolution x-ray diffraction (HRXRD) and TEM indicate that they remain coherently strained at a growth temperature of 365 °C.

2.2.2 *Ex situ* Annealing Procedure

Strain relaxation was accomplished by annealing pieces of the samples in a conventional quartz-tube furnace flooded with N_2 gas. Furnace temperatures were measured with the aid of a thermocouple and controlled to within ±1 °C. A pre-warmed quartz boat was used to support the sample during the anneal and also served to minimize errors associated with warm-up transients. Even so, a slight correction was needed to account for these effects, although this correction did not affect E_a. Immediately after each annealing step, the samples were quenched in water to bring them quickly back to room temperature.

2.2.3 Determination of Strain Relaxation Using XRD

Measurements of $a_\perp$ and $a_\parallel$ with HRXRD (resolution $<$ 5 arcsec) confirm that the samples were all grown coherently strained. In our setup, Cu $K_{\alpha 1}$ x-ray radiation is selected with a Ge four-crystal monochromator and collimated onto the sample. A detector is placed near the expected angle for the $n = 1$ reflection

Sample	h (Å)	$\overline{x}$	η_0^{exp} (%)	E_a (meV)
A1	5040	23	17	⋯
A2	4990	21	16	2.0±0.1
A3	2900	26	17	2.0±0.1
A4	900	37	34	⋯
A5	3500	21	47	2.3±0.3
SL1	5220	20	57	⋯
SL2	5220	18	57	1.9±0.3

Table 2.1: $Si_{1-x}Ge_x/Si$ sample set studied for this chapter. Average Ge concentration, $\overline{x}$, and residual strain, η_0^{exp}, were determined through the use of θ-2θ XRD.

corresponding to diffraction from (400), (422), or (440) Bragg planes. For the alloy samples (A1-A5), analysis was straightforward since only a single peak corresponding to the alloy and a substrate peak appear in the scans. In this case, the angular separation between the alloy and substrate peaks is measured. The lattice constants, $a_\perp$ and $a_\parallel$, are determined from the equations derived in Section 1.3.2. For the superlattices, several peaks are visible in the scans because of the long wavelength periodicity present in the structure. As a result, only average properties can be determined. In practice, the angular separation between the substrate and the $m = 0$ superlattice peak[19] is used to calculate $\overline{a}_\perp$ and $\overline{a}_\parallel$.

In a coherently strained film, alloy composition fixes the angle of incidence, θ, and hence the spacing between Bragg planes, d, through

$$\lambda = 2d \sin\theta. \tag{2.1}$$

For (400) diffraction, we define the fraction of coherent strain, η, in terms of the tetragonal distortion,[1] $\epsilon_{\mathrm{T}} = -\epsilon_\perp/\epsilon_\parallel = 0.76$, and the mismatch, $f = 0.0418$, by[12]

$$d_{(400)}(\eta) = \frac{a_\perp}{4} \approx d_{\mathrm{Si}} \left[1 + f\left[1 + \eta\epsilon_{\mathrm{T}}\right] x\right]. \tag{2.2}$$

Therefore, we can fix $\eta = 1$ since the samples are coherently strained and determine average composition, $\overline{x}$, from Eq. 2.2 and a measurement of $\overline{a}_\perp$.

After each annealing step, (400) θ-2θ scans were used to measure η as a function of annealing time. Since the average composition remains fixed throughout the annealing sequence, η can be determined from Eq. 2.2 and a measurement of $d_{(400)}$. For these measurements, Cu K_β as opposed to Cu K_α x-ray radiation was selected through the use of a graphite, monochromating filter, eliminating the need to perform a Rachinger correction on the data. Data were acquired digitally and peak positions were determined through the use of a numerical, peak-finding algorithm.[20]

2.3 Results

2.3.1 Comparison of Residual Strain in $Si_{1-x}Ge_x$ Alloys and $Si_{1-x}Ge_x/Si$ Strained-layer Superlattices

After pieces of the samples were annealed at 700 °C for 2 h, the extent of relaxation was determined with θ-2θ XRD. While significant interdiffusion did not occur at this temperature, the treatment was seen as being sufficient to allow complete relaxation. In Fig. 2.1, we compare the amount of residual strain remaining in the single-layer, alloy sample A2 and the superlattice SL1. Recall, both samples were designed to have the same average properties, and therefore, according to equilibrium critical thickness theories, should relax to the same degree.[3]-[5] In the figure, a single peak corresponding to the (400) reflection from the alloy and a family of peaks corresponding to the (400)-like reflections from superlattice are visible. A comparison of the scans taken before (solid) and after (dotted) reveal that significant relaxation has occurred. The peak at $2\theta = 61.68\,^\circ$ is from the substrate, and its position does not change. In (a), the d-spacing between (400) planes in the alloy sample has relaxed by $(0.55\%)d_{\mathrm{Si}}$ which, according to Eq. 2.2, corresponds to relaxation of $\sim$ 84% of coherent strain. Similar analysis of the (400)-like, zeroth-order superlattice peak[19] in (b) indicates that the superlattice relaxes only $\sim$ 43% of its coherent strain.

2.3.2 Relaxation Behavior of $Si_{1-x}Ge_x$ Alloys

In Fig. 2.2, we study the relaxation behavior of sample A2 following a sequence of anneal steps at a temperature of 414 °C. In the figure, the peak marked COH corresponds to the θ-2θ scan prior to annealing. The peaks 1-4 reveal that each annealing step causes the sample to relax further as indicated by the move-

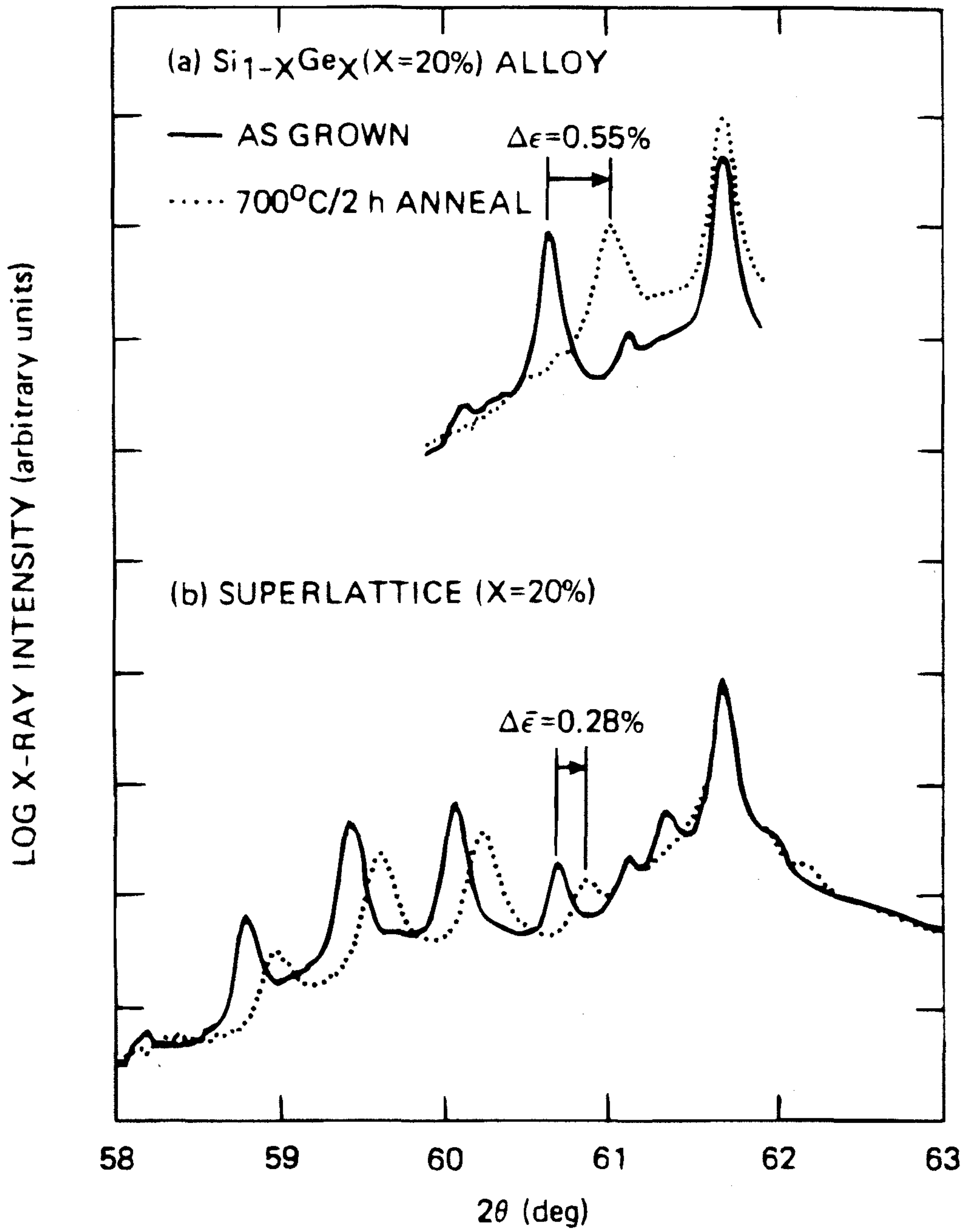

Figure 2.1: (a) Symmetric (400) Bragg reflections from sample A2 showing the full extent of relaxation after a 2 h anneal at 700 °C. (b) For a superlattice with the same average composition (sample SL1), the average strain measured from the (400)-like, $m = 0$ superlattice reflection[19] relaxes considerably less. (From Ref. [13].)

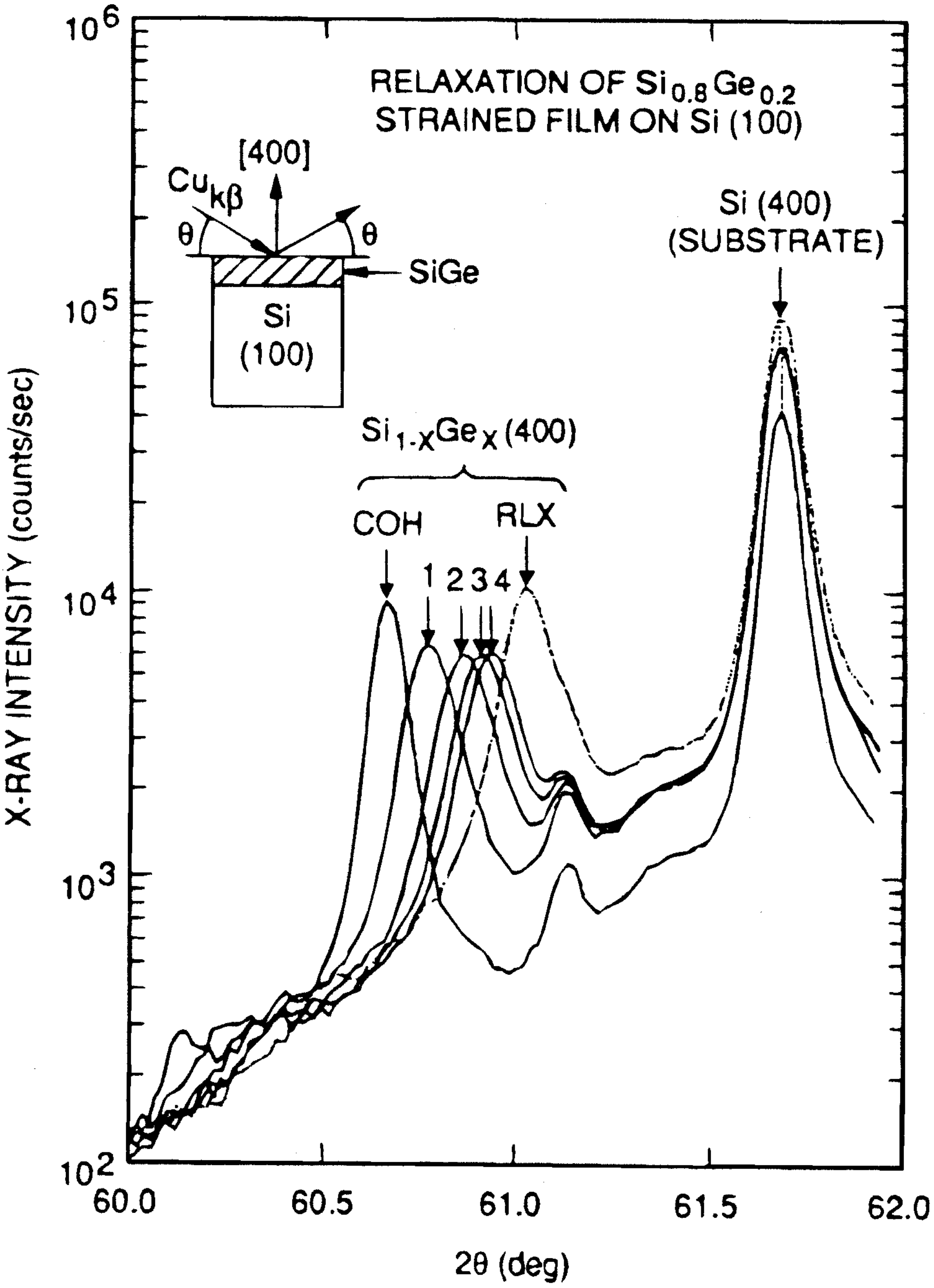

Figure 2.2: θ-2θ XRD scans of the (400) Bragg reflection from sample A2 as a function of anneal time. Initially strained coherently to (100) Si (COH), the sample is shown to relax significantly after several 35 min anneals at only 414 °C (1-4). A scan from a fully relaxed piece of A2 is included for comparison (RLX). (From Ref. [12].)

ment of the peak position toward increasing 2θ (decreasing $d_{(400)}$). Notice that the width of the alloy peak is observed to broaden after the first anneal suggesting that the relaxation is not homogeneous (compare the peaks labeled "COH" and "1"). Data taken from Fig. 2.1(a) are also included in the figure to allow comparison with a fully relaxed piece of the sample (RLX). Analysis of the peak positions indicates that the strain decays exponentially with anneal time toward a residual value.

2.3.3 Strain Relaxation Kinetics

In Fig. 2.3 we plot η, the fraction of coherent strain, as a function of *ex situ* anneal time for sample A3. Pieces of the sample were annealed at various temperatures between 369 and 437 °C in a series of isochronal anneal steps. After each step, θ-2θ XRD was used to determine the fraction of coherent strain remaining in the epilayer. In (a), we show that relaxation proceeds to a residual value, η_0, exponentially, regardless of the anneal temperature. Values for η_0 were determined in all our samples after a 2 h anneal at 700 °C and are displayed in Table 2.1. In (b), $\ln(\eta - \eta_0)$ is plotted as a function of anneal time and a linear fit is made to the data at each temperature assuming first-order kinetics. The strain relaxation rate is determined from the slope of the fit. The error bars at each point reflect the uncertainty in η arising from the finite resolution of the diffractometer used to measure the x-ray peak positions. A slight, systematic deviation from first-order kinetics is observed as the relaxation proceeds, perhaps indicating that interactions between dislocations become more significant. From the decay rates, an activation energy can be obtained. In Fig. 2.4, we plot strain relaxation rate vs. $1/kT$ for each sample. Regardless of composition or anneal temperature, each sample is observed to relax with an activation energy near 2.0

eV.

2.4 Discussion

The results presented in this chapter describe the relaxation process in $Si_{1-x}Ge_x/Si$ heterostructures in quantitative detail. We find that structures can be grown coherently strained to (100) Si at a growth temperature of 365 °C to thicknesses considerably in excess of previous experimental values for growth at higher temperatures (550 – 600 °C).[1] Furthermore, we have observed significant relaxation in our samples during anneals at temperatures as low as 370 °C, far below temperatures employed in previous studies of relaxation.[8, 9, 26] In a series of isochronal anneals, relaxation is observed to proceed roughly exponentially toward a residual value at a rate dependent upon the detailed strain distribution in the sample. It was pointed out in Section 2.3.3 that as the relaxation proceeds, a systematic deviation from first-order kinetics is observed. Also, the observed broadening of the alloy peak from sample A2 after the first anneal (see Fig. 2.2) suggests that the actual relaxation mechanism may be more complicated. In fact, a complete picture of relaxation may require a sequence of events to occur, each having different activation energies.[21]-[24]

On the basis of our results, we can attempt to determine which microscopic properties might be important. In Section 2.3.1, we compared the relaxation behavior between a $Si_{0.8}Ge_{0.2}$ alloy and a superlattice having similar average properties. In contrast with the predictions of equilbrium, critical thickness theories,[3]-[5] the two samples do *not* relax to the same extent. Apparently, the detailed structure in the superlattice serves as impediment to the microscopic mechanisms of relaxation. These results suggest that any microscopic theory of relaxation must involve mechanisms that allow interaction of disloca-

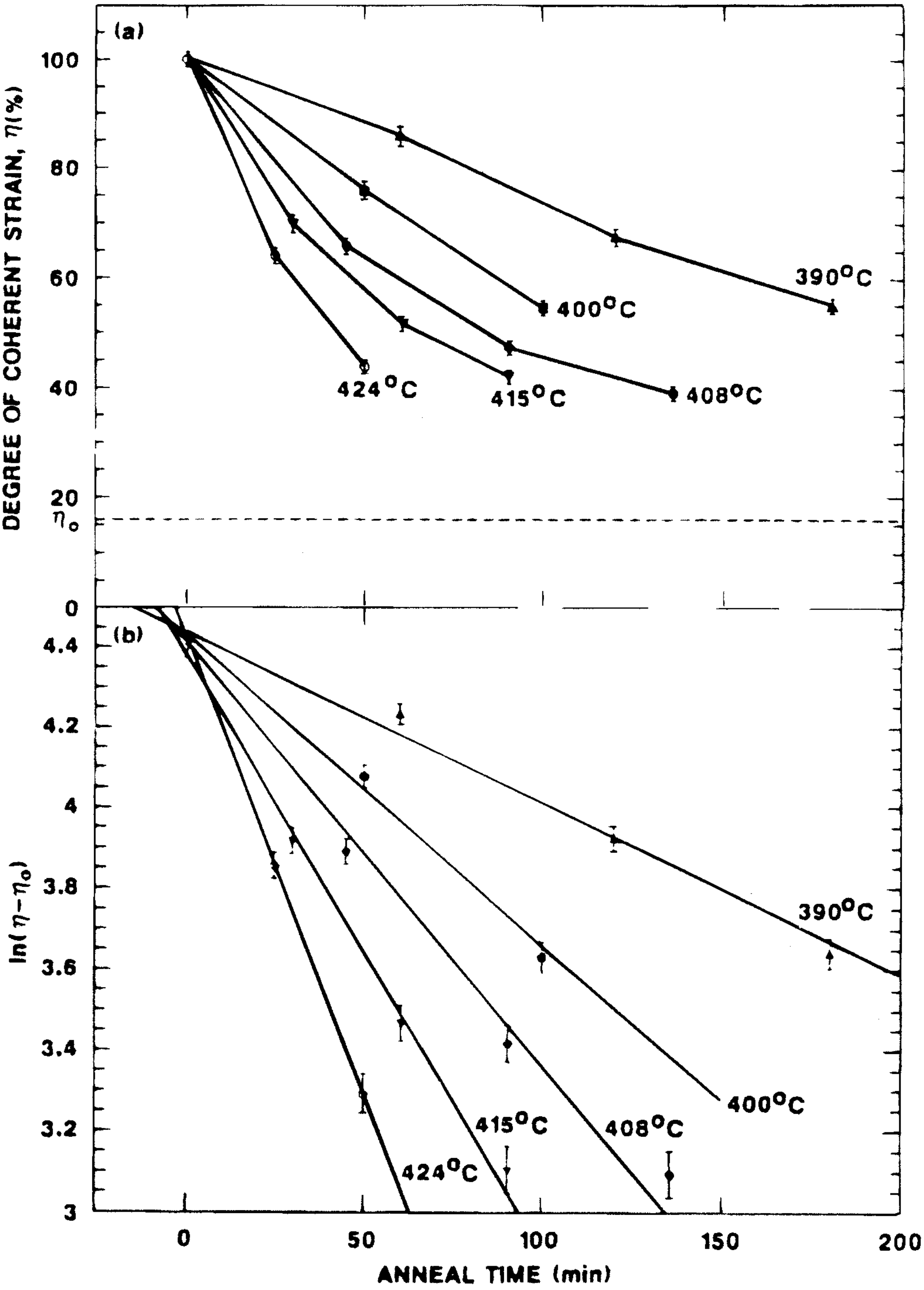

Figure 2.3: (a) η, the fraction of coherent strain, is plotted as a function of anneal time for sample A3 at various temperatures. (b) Assuming first-order kinetics, strain relaxation rate is determined at each temperature from a linear fit to the data displayed in semilog form. (From Ref. [13].)

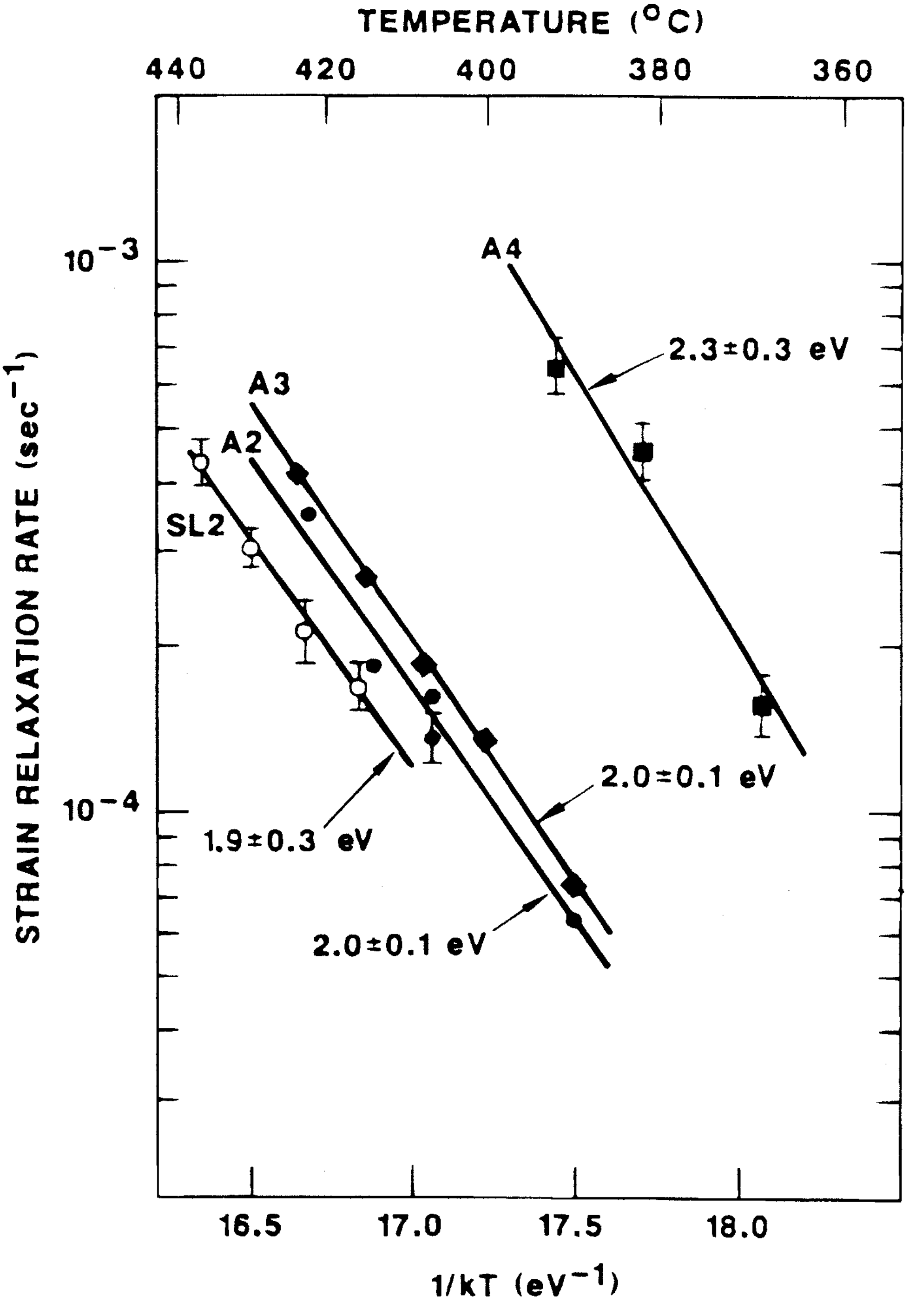

Figure 2.4: Strain relaxation rate vs. $1/kT$ for several of the samples studied. The activation energy for relaxation is measured to be approximately 2.0 eV regardless of composition or annealing temperature. (From Ref. [13].)

tions with the alternating strain fields of a superlattice, in agreement with the work of Tuppen *et al.*[11] Indeed, previous work with GaAsP on GaAs suggests that superlattices may bend dislocations toward the sample edge,[25] decreasing the density of threading dislocations in the heteroepitaxial layers.

2.5 Chapter Summary

In this chapter, we have presented results from a quantitative study of strain relaxation in $Si_{1-x}Ge_x$ alloys and $Si_{1-x}Ge_x/Si$ superlattices initially grown coherently strained to (100) Si substrates. Alloys and superlattices designed to have the same average properties were compared to determine the extent of relaxation after a 2 h anneal at 700 °C. From θ-2θ XRD, a $Si_{0.8}Ge_{0.2}$ alloy was shown to relax approximately $\sim 84\%$ of its initial strain compared with only $\sim 43\%$ for the corresponding superlattice. Interactions between dislocations and the alternating strain fields of the superlattice appear to be responsible for the observed differences. In addition, the kinetics of relaxation was investigated quantitatively for several samples. Significant relaxation is observed as the samples were annealed at temperatures as low as 370 °C, considerably *below* growth temperatures typically employed in previous studies.[1, 11, 26] In each case, relaxation can be described as a single, thermally activated, first-order kinetic process having an activation energy near 2.0 eV. Since an activation energy of 2.0 eV is also attributed to the glide of misfit dislocations in Si,[14] glide may be the rate-limiting mechanism for strain relaxation in our samples.

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Chapter 3

Measurement of the Strain Dependence of the (100) Si/Ge Valence Band Offset

3.1 Introduction

3.1.1 Background

In general, heterojunction devices fabricated from dissimilar semiconductors possess discontinuities in their valence and conduction bands; therefore, since the band gaps of most semiconductor materials are well known,[1] a measurement of the valence band offset reveals much about the potential behavior of any electronic devices[2, 3] fabricated from the materials. Often, the valence band offset can be affected by strain, causing shifts in the heavy-hole, light-hole, and spin-orbit energies, complicating the picture considerably.[4] Theoretical calculations[5] and recent experimental results[6, 7] confirm the strong influence of strain in these systems. Consequently, meaningful measurements of band offsets must address the various effects of strain.

Earlier in this thesis, the $Si_{1-x}Ge_x$/Si material system was indicated to possess a moderate lattice mismatch, $f = 4.18\%$, thereby requiring a careful study of strain effects in any measurement of the valence band offset. In this chapter, we present the first *in situ* measurement of the strain dependence of the (100) Si/Ge valence band offset. Samples prepared by molecular beam epitaxy (MBE) and maintained in an ultrahigh-vacuum environment (UHV) were transferred to an attached, surface-analysis chamber capable of performing x-ray photoelectron spectroscopy (XPS). There, Si $2p$ and Ge $3d$ core level to valence-band edge and core level to core-level energy separations were measured as a function of strain. Since our samples were never exposed to atmosphere, our results do not suffer from doubts related to the cleanliness of our surfaces. In fact, both oxygen *and* carbon contamination were confirmed to be absent down to the sensitivity of the XPS technique (< 0.5 atomic percent).

Three sets of samples were grown for this measurement. First, Si films grown coherently strained to relaxed Si-rich $Si_{1-x}Ge_x$ buffer layers were studied with XPS to determine the energy difference between the Si $2p$ core level and the Si valence-band edge. Similarly, the Ge $3d$ core level to Ge valence-band edge energy separation was measured for strained Ge films grown on relaxed, Ge-rich $Si_{1-x}Ge_x$ buffers. Lastly, the separation between the Si $2p$ and Ge$3d$ core levels was measured by XPS from strain-symmetrized Si/Ge superlattices. For these measurements, strain was measured independently through the use of high-resolution x-ray diffraction (HRXRD) from the (422) Bragg reflections in the strained epilayers and relaxed, $Si_{1-x}Ge_x$ buffer layers.

3.1.2 Outline of Chapter

The remainder of this chapter is organized as follows. In Section 3.2, the sample set grown for this study is described. Motivation for choosing the structures and the methods used are discussed. In addition, this section focuses on sample preparation, growth of relaxed, $Si_{1-x}Ge_x$ buffer layers, and the determination of strain through HRXRD. We present our results in Section 3.3. Section 3.3.1 contains an introduction to the expected band alignments for strained Ge on Si and strained Si on (100) Ge. Also included in Section 3.3 are typical XPS spectra from each type of sample studied. We also describe the use of model functions in determining the position of the valence-band edge from our data. Results of our measurements including a plot of separation energy vs. in-plane lattice constant ($a_{\parallel}$) are presented in Section 3.3.4. The chapter concludes with a discussion of these results and a summary in Sections 3.4 and 3.5, respectively.

3.2 Experimental

3.2.1 Sample Set

In Section 1.4, the method used here to measure strain effects on the valence band offset in lattice-mismatched heterostructures was discussed. Three sets of samples consisting of strained Si, strained Ge, and Si/Ge superlattices grown coherently to nearly fully relaxed* $Si_{1-x}Ge_x$ buffer layers were studied *in situ* with XPS. Since the $Si_{1-x}Ge_x$/Si material system possesses a moderate lattice mismatch, care must be taken to ensure that the samples are indeed strained. Consequently, epilayer thicknesses were chosen, keeping in mind several impor-

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*In most cases, HRXRD measurements of $a_{\perp}$ and $a_{\parallel}$ confirm that the buffer layers were more than 80% relaxed.[8, 9]

tant considerations. First, total layer thickness should not exceed the empirical, critical thickness curve for growth at 550 °C attributed to People and Bean.[10] Second, the strained Si and strained Ge epilayer thicknesses were chosen to be as close to the People and Bean curve as possible since thicker films are more easily detectable with HRXRD. As a result, these layers were between 300 and 1000 Å in thickness. Lastly, the Si/Ge superlattices were chosen to have the same average composition as the buffer layer, so if the individual layer thicknesses did not exceed the critical thickness curve, the entire structure could be grown to arbitrary thickness (symmetrically strained case). Superlattice thicknesses were typically 2000 Å, producing strong x-ray signals from which $a_{\parallel}$ could be easily measured. Furthermore, we wished to obtain XPS data from both the Si and Ge layers of the superlattice; therefore, the top-layer thickness had to be below the electron-escape depth for XPS (typically a few tens of Angstroms).[11] For this reason, superlattice layer thicknesses ranged between 20 and 60 Å. Si-rich superlattices were topped with 30 Å Si. The sample set studied for this chapter is presented in Table 3.1.

Growth of each sample took place in the Perkin-Elmer (Model 430S) Si MBE system previously described in Section 1.2.1. Si and Ge were coevaporated from a Temescal, dual *e*-beam source onto radiatively heated, 3 inch, (100) Si substrates typically doped with phosphorus to 0.02 – 0.60 Ωcm. Deposition rates were monitored through the use of a cathodoluminescent flux sensor and verified with HRXRD from $Si_{1-x}Ge_x/Si$ superlattices and transmission electron microscopy (TEM). Buffer layers were grown typically at 500 °C at a deposition rate of approximately 5 Å/s. During the growth of the strained epilayers, the deposition rate was decreased to 1 Å/s, and a lower growth temperature[12] was used.[†]

[†] Some strained epilayers were also grown at 500 °C (see Table 3.1).

Sample	Buffer Layer(s)	Superlattice	Top Layer
Strained Si			
A1	...	...	5000 Å Si*
A2	5500 Å $\mathrm{Si}_{0.91}\mathrm{Ge}_{0.09}$ on 5000 Å Ge	...	1000 Å Si*
A3	5100 Å $\mathrm{Si}_{0.81}\mathrm{Ge}_{0.19}$ on 5000 Å Ge	...	500 Å Si*
A4	5000 Å $\mathrm{Si}_{0.72}\mathrm{Ge}_{0.28}$ on 5000 Å Ge	...	400 Å Si
Strained Ge			
B1	...	...	5000 Å Ge*
B2	5000 Å $\mathrm{Si}_{0.04}\mathrm{Ge}_{0.96}$	...	1000 Å Ge*
B3	5100 Å $\mathrm{Si}_{0.16}\mathrm{Ge}_{0.84}$	...	500 Å Ge*
B4	5000 Å $\mathrm{Si}_{0.26}\mathrm{Ge}_{0.74}$	...	500 Å Ge
B5	5000 Å $\mathrm{Si}_{0.30}\mathrm{Ge}_{0.70}$	...	400 Å Ge
Superlattices			
C1	5000 Å $\mathrm{Si}_{0.76}\mathrm{Ge}_{0.24}$ on 2500 Å Ge	20 Å Ge on 60 Å Si (25 periods)	30 Å Si
C2	5000 Å $\mathrm{Si}_{0.60}\mathrm{Ge}_{0.40}$	20 Å Ge on 30 Å Si (40 periods)	30 Å Si
C3	5000 Å $\mathrm{Si}_{0.41}\mathrm{Ge}_{0.59}$	20 Å Si on 30 Å Ge (40 periods)	20 Å Si
C4	5000 Å $\mathrm{Si}_{0.24}\mathrm{Ge}_{0.76}$	20 Å Si on 60 Å Ge (25 periods)	20 Å Si

Table 3.1: Strained Si/Ge sample set. Strained epilayers were grown at 350 °C except for those marked with a (*), which were grown at higher temperatures (500 °C). Buffer layers were grown at 500 °C and annealed for 30 min at 700 °C to ensure full relaxation.

Temperatures were measured *in situ* with the aid of a thermocouple calibrated against an optical pyrometer (Ircon, W-series) and corroborated through observations of Au/Si and Al/Si eutectic reactions. Quoted temperatures are believed to be accurate within ±20 °C.

3.2.2 Sample Preparation

Prior to deposition, substrates were degreased *ex situ* in (1,1,1)-trichloroethane, acetone, and methanol solvents at a temperature of 50 – 60 °C. After a brief rinse in de-ionized water, surface SiO_2 was removed in a 50% HF solution, and the substrates were rinsed again. After about 30 s, the substrates were removed slowly from the rinse and quickly loaded into the deposition chamber. *In situ* oxide desorption involved heating the substrate in UHV to 800 °C under a slight Si flux (0.1 Å/s) until a sharp (2 × 1) reconstruction was observed with reflection high-energy electron diffraction (RHEED).[13, 14] Finally, a 1200 Å, pure Si buffer layer was grown as the substrate temperature was ramped from 700 to 530 °C. Substrate surfaces prepared in this way appear mirror-smooth and have sharp (2 × 1) RHEED patterns indicative of a clean surface.[15]

3.2.3 Growth of Relaxed $Si_{1-x}Ge_x$ Buffer Layers

For this study, relaxed $Si_{1-x}Ge_x$ buffer layers prepared by MBE were grown for the purpose of varying the in-plane lattice constant in the subsequent epitaxial layers (of course, edge- and screw-type dislocations are present in the relaxed layers; however, their densities should not be high enough to affect the XPS measurements). Practical considerations required the growth of a relaxed, Ge buffer layer prior to the growth of the Si-rich buffers since the critical thickness for these layers exceeds several thousand Angstroms for epitaxy on Si. In the case of Ge-rich buffers, 5000 Å deposited directly on Si was seen to be sufficient to produce a relaxed layer. Following the deposition of each buffer layer, the substrate temperature was increased over 10 min to 700 °C and held there for 30 min. Annealing the samples at this temperature allowed for substantial relaxation, while at the same time, prevented significant interdiffusion with the substrate.[8, 9]

3.2.4 Study of Strain Distributions Through the Use of HRXRD

The lattice constants, $a_\perp$ and $a_\parallel$, in the strained Si and strained Ge samples were measured through HRXRD of the asymmetric (422) Bragg reflections in the buffer layers and heteroepitaxial films. Recall from Section 1.3.2, that two measurements are needed to determine $a_\perp$ and $a_\parallel$ with this technique. In the forward (reverse) scattering geometry, we measure the angular separation of $\theta + \phi$ ($\theta - \phi$) between the substrate and the epilayer. Unfortunately, the strained Si and strained Ge epilayers were too thin to allow an accurate measurement to be made in the reverse geometry. The measurement could be made in the forward geometry, however, so we calculated the angular separation expected in the reverse geometry (and hence $a_\perp$ and $a_\parallel$), since we knew the composition of the epilayers and the elastic constants. Similarly, the composition of the buffer layers was calculated from direct measurements of the two lattice constants and the elastic constants. These measurements indicated that on average, the buffer layers were approximately 80% relaxed.

The strain configurations in the superlattices were measured through the use of a Phillips θ-2θ powder diffractometer. Superlattice period and average composition were calculated from the position of the (400)-like $m = 0$ superlattice reflection[16] and the spacing between superlattice peaks. These measurements, in conjunction with the known rates for Si and Ge deposition, were consistent with our contention that the superlattices were coherently strained to the underlying $Si_{1-x}Ge_x$ buffer layers.

3.3 Results

3.3.1 Band Alignments for Strained (100) Si/Ge

In Fig. 3.1, a schematic diagram, showing the energy-band diagrams for strained Ge on (100) Si and strained Si on (100) Ge, is presented. Strain in the epilayer results in a shift of the light-hole, heavy-hole, and spin-orbit energy levels in addition to a shift in the core level to valence-band edge, energy separation. A meaningful measurement of the valence band offset, therefore, requires these effects to be taken into account. From XPS spectra, we measure the Si $2p$ core level to valence-band edge, the Ge $3d$ core level to valence-band edge, and the Si $2p$ core level to Ge $3d$ core-level, energy differences as a function of strain and calculate the strain dependence of the valence band offset using

$$\Delta E_v = (E^{\mathrm{Ge}}_{\mathrm{Ge}3d} - E^{\mathrm{Ge}}_v) + (E^{\mathrm{Si}}_{\mathrm{Si}2p} - E^{\mathrm{Ge}}_{\mathrm{Ge}3d}) - (E^{\mathrm{Si}}_{\mathrm{Si}2p} - E^{\mathrm{Si}}_v). \qquad (3.1)$$

3.3.2 Typical XPS Spectra

After sample growth was completed and the substrate returned to room temperature, the samples were transferred in UHV into the XPS analytical chamber. XPS measurements were performed through the use of a Perkin-Elmer 5100 analysis system equipped with a monochromatic Al K_α x-ray source ($h\nu = 1486.6$ eV). Earlier in the thesis (Section 1.4), the technique of XPS was discussed. A monochromatic x-ray source incident on the surface interacts with the atoms

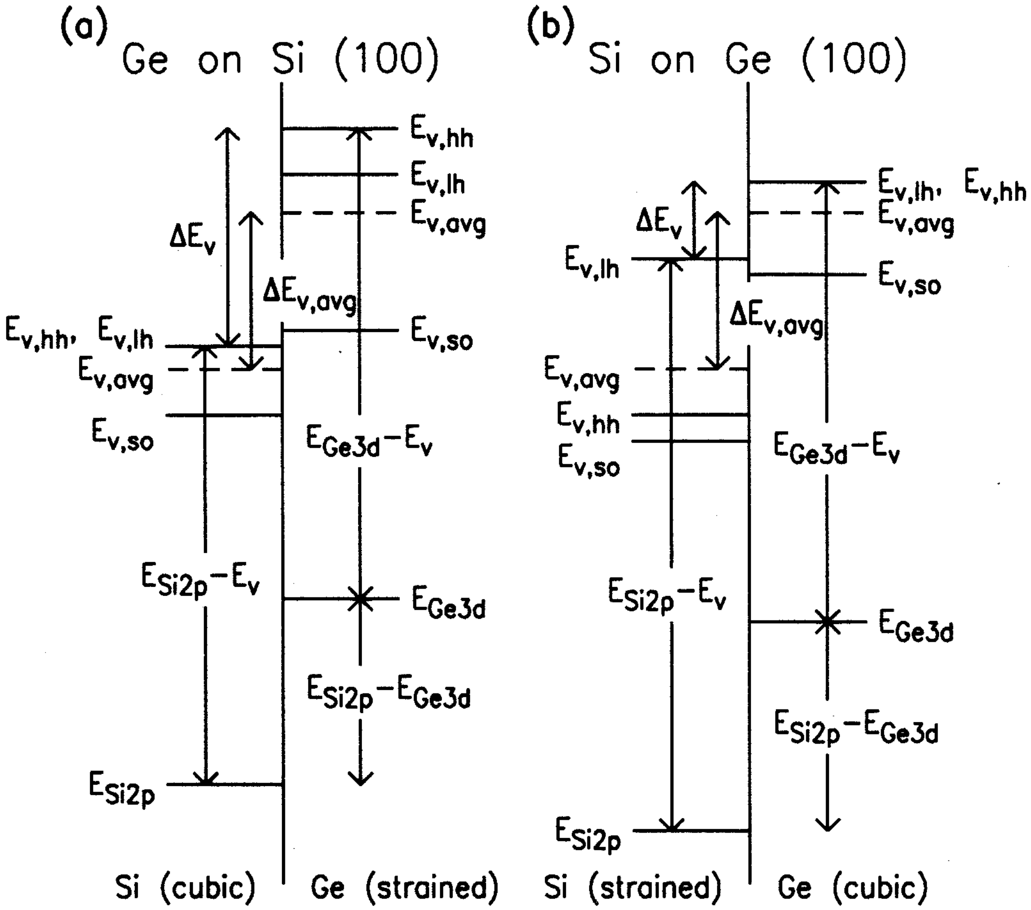

Figure 3.1: (a) Schematic band diagram for Ge strained to (100) Si. (b) Same diagram for Si strained to (100) Ge. The energies $E^{\mathrm{Si}}_{\mathrm{Si}2p} - E^{\mathrm{Si}}_{v}$, $E^{\mathrm{Ge}}_{\mathrm{Ge}3d} - E^{\mathrm{Ge}}_{v}$, and $E^{\mathrm{Si}}_{\mathrm{Si}2p} - E^{\mathrm{Ge}}_{\mathrm{Ge}3d}$ are measured and ΔE_v is calculated from Eq. 3.1. (From Refs. [17]-[19].)

in the sample, inducing electrons to leave their atomic orbitals. With the XPS technique, the kinetic energy of the emitted electrons can be analyzed and their binding energies can be determined. A study of the binding-energy spectra from these electrons necessarily reveals a great deal about the nature of the electronic states in the sample. Although the x-ray source penetrates several microns into the sample, only electrons emitted from the first 30 Å or so escape the surface and are analyzed.

In Fig. 3.2, we show some XPS spectra representative of the data obtained from our samples. In (a), a strained Si sample was studied from which we determined the Si $2p$ core level to valence-band edge, energy separation. Visible in the figure is the Si $2p$ peak and the valence-band edge. To improve signal-to-noise, sampling times in the vicinity of the valence-band edge were typically four times longer than near the core levels. The valence-band edge also appears in the figure plotted on an expanded scale. In (b), we plot a similar spectrum for strained Ge. Finally, a representative spectrum from one of our superlattice samples is shown in Fig. 3.2(c). From these data we measure the Si $2p$ to Ge $3d$ core level to core-level energy separation in several samples strained to various degrees on relaxed $Si_{1-x}Ge_x$ buffer layers.

3.3.3 Determining the Positions of Core-Level Peaks and Valence-Band Edges

The core-level peak positions were determined to be the average of the two energies at half maximum after subtracting a background function proportional to the integrated, photoelectron intensity from the original data. The core-level position proved to be reproducible to better than 0.01 eV. Following Kraut *et al.*,[20] the position of the valence-band edge was determined by fitting the XPS data to

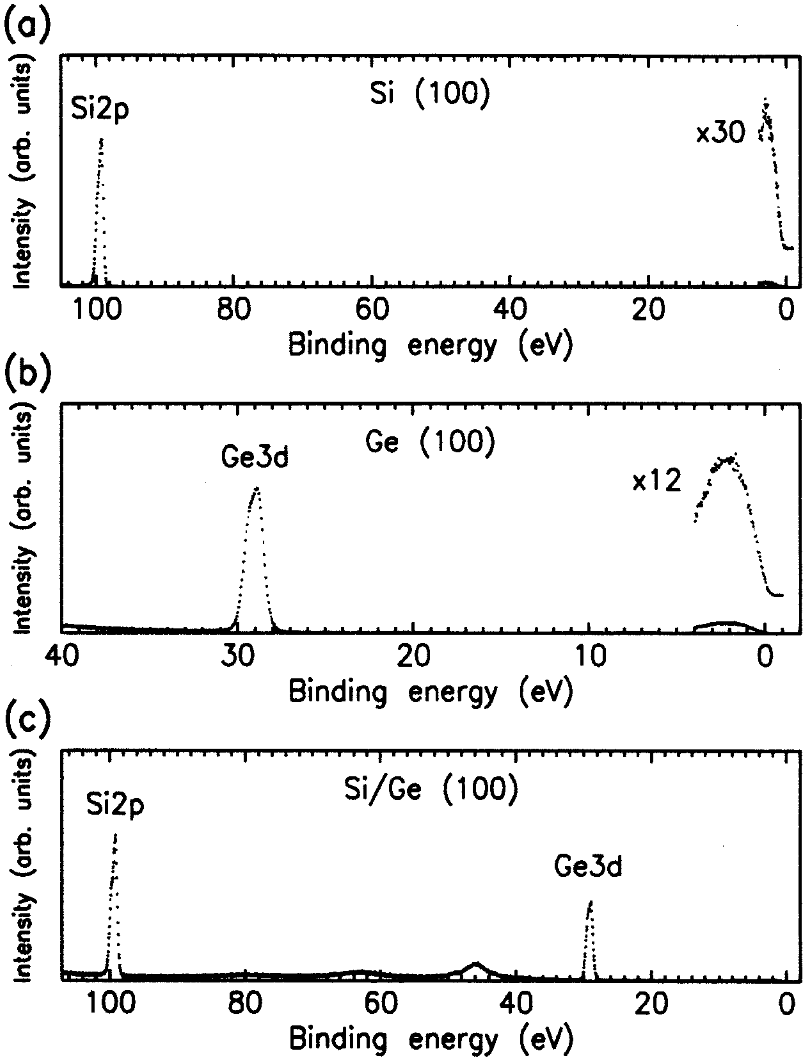

Figure 3.2: XPS data from (100) Si (a), (100) Ge (b), and a (100) Si/Ge superlattice (c). Sampling times near the valence-band edge in (a) and (b) are four times longer than at the core level positions. For clarity, these data are also plotted on an expanded scale. (From Refs. [17]-[19].)

a model function calculated from a convolution of a theoretical density of states and an experimentally determined, XPS-instrumental resolution function. The empirical pseudopotential method[21] including spin-orbit interactions[22] and a nonlocal electron mass parameter[23] were used to calculate the electron densities of states. Strain effects were included through the use of a Pikus-Bir transformation on the Hamiltonian[24] and a fit of the resulting splitting of the valence bands to known deformation potentials for Si and Ge.[25] Our estimate of the uncertainty in the valence-band edge position was taken to be 0.04 eV, although the results were found to be reprodicible to better than 0.01 eV. In Fig. 3.3, we show represenative XPS spectra from the vicinity of the valence-band edge for strained Si and strained Ge. The solid curve in the figure represents the fit of the model function to the data. Inset in the figure are the calculated valence-band density-of-states functions used in the model.

3.3.4 Summary of Results

Results from these measurements are tabulated in Table 3.2. In Fig. 3.4, we plot the energy separation of the Si $2p$ core level to valence-band edge, Ge $3d$ core level to valence-band edge, and Si $2p$ core level to Ge $3d$ core level as a function of in-plane lattice constant, $a_\parallel$. The solid lines represent the results of a least-squares fit to the data. From these fits, we obtain the core-level binding energies and core-level energy separations to be

$$E^{\mathrm{Si}}_{\mathrm{Si}2p} - E^{\mathrm{Si}}_{v} = 98.95 + 1.96(a_\parallel - 5.431), \tag{3.2}$$

$$E^{\mathrm{Ge}}_{\mathrm{Ge}3d} - E^{\mathrm{Ge}}_{v} = 29.41 - 1.24(a_\parallel - 5.658), \tag{3.3}$$

$$E^{\mathrm{Si}}_{\mathrm{Si}2p} - E^{\mathrm{Ge}}_{\mathrm{Ge}3d} = 70.09 + 0.526(a_\parallel - 5.431). \tag{3.4}$$

In these equations, energy is measured in eV, and $a_\parallel$ is given in Angstroms. We can calculate the valence band offset from these equations and Eq. 3.1.

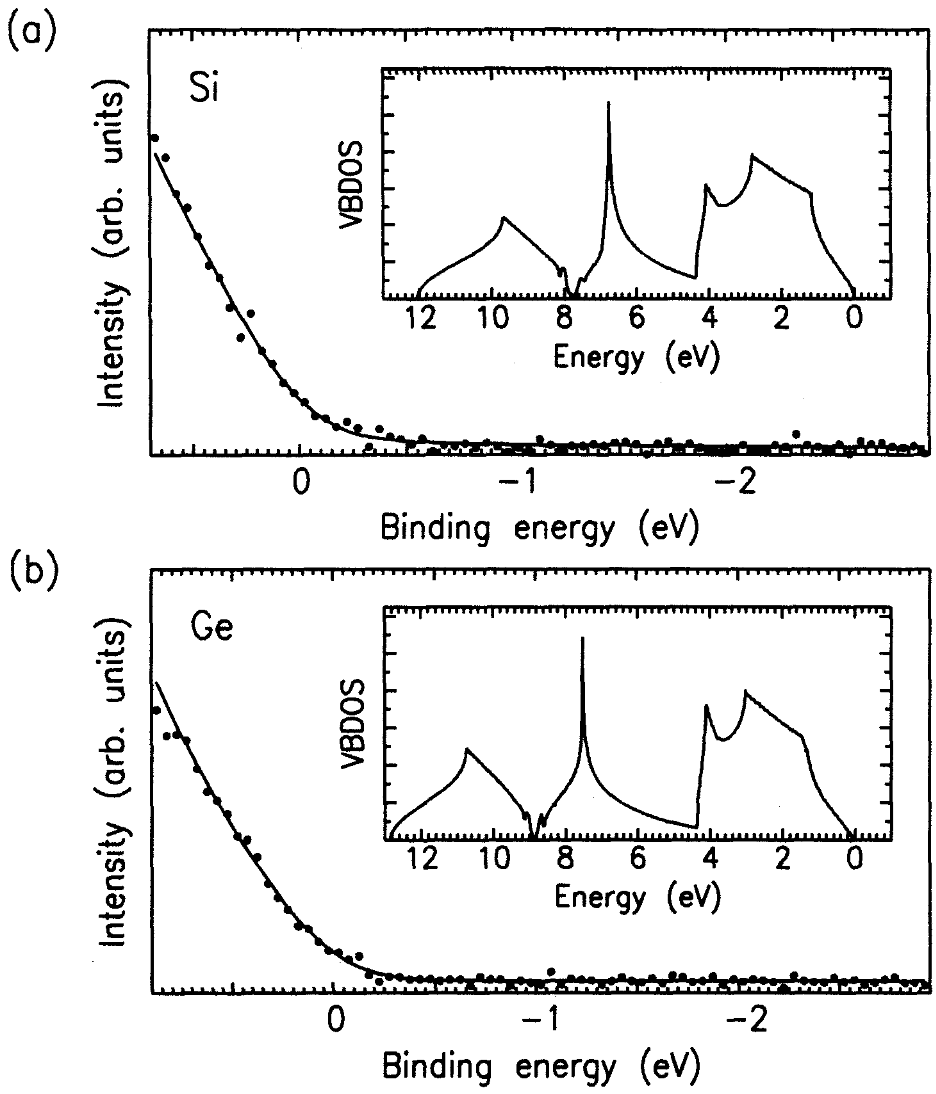

Figure 3.3: XPS spectra from the valence-band edge of unstrained (100) Si (a) and unstrained (100) Ge (b). Inset in the figure are the theoretical density-of-states functions used to fit the data (see text). (From Refs. [18, 19].)

Sample	Buffer Layer Composition (% Ge)	$a_{\parallel}$ (Å)	Energy Separation (eV)
Strained Si			$E^{\mathrm{Si}}_{\mathrm{Si}2p} - E^{\mathrm{Si}}_{v}$
A1	0	5.431	98.951
A2	9	5.447	98.964
A3	19	5.463	99.027
A4	28	5.492	99.065
Strained Ge			$E^{\mathrm{Ge}}_{\mathrm{Ge}3d} - E^{\mathrm{Ge}}_{v}$
B1	100	5.658	29.415
B2	96	5.652	29.410
B3	84	5.628	29.457
B4	74	5.611	29.473
B5	70	5.601	29.475
Si/Ge Superlattices			$E^{\mathrm{Si}}_{\mathrm{Si}2p} - E^{\mathrm{Ge}}_{\mathrm{Ge}3d}$
C1	24	5.483	70.121
C2	40	5.516	70.136
C3	59	5.556	70.165
C4	76	5.597	70.178

Table 3.2: Results obtained from HRXRD and XPS of samples described in Table 3.1. Relaxed, alloy buffer-layer composition, x, and parallel-lattice constant, $a_{\parallel}$, measured with HRXRD, appear in columns 2 and 3. Si $2p$ and Ge $3d$ core level to valence-band edge and core level to core-level energy separations are shown in column 4.

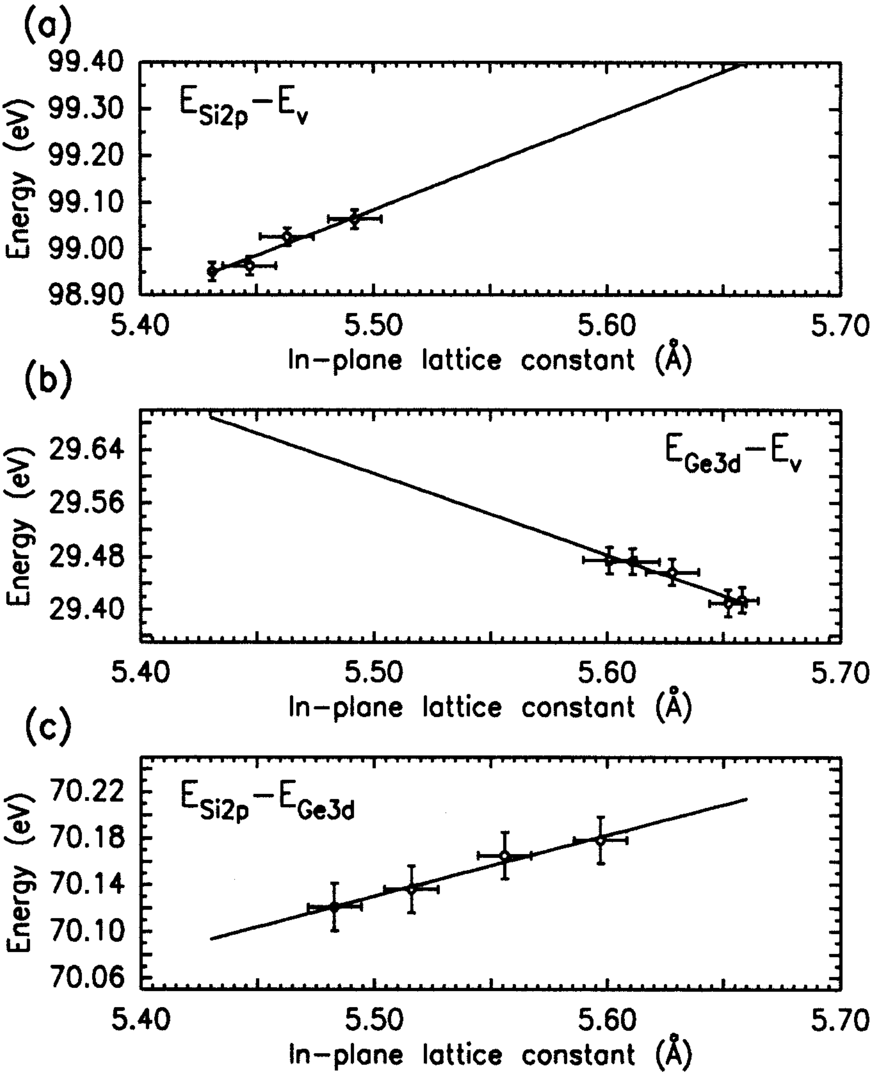

Figure 3.4: Core level to valence-band edge separation energies for strained Si (a) and strained Ge (b). (c) Strain dependence of the core-level energy differences determined from XPS data from strained Si/Ge superlattices. The strain dependence of the valence band offset was calculated from a linear fit to these parameters and Eq. 3.1. (From Refs. [17]-[19].)

Substituting $a_\parallel = 5.431$, we obtain the valence band offset for Ge strained to (100) Si to be 0.83 ± 0.11 eV. Similarly, for Si strained to (100) Ge, we substitute $a_\parallel = 5.658$ eV into Eqs. 3.1-3.4 and obtain a valence band offset of 0.22 ± 0.13 eV. Uncertainties in the core level to valence-band edge and core level to core-level energy separations were calculated in the fit, assuming an uncertainty of 0.02 eV in binding energy between samples and 0.01 Å in $a_\parallel$ for each sample. In addition, 0.04 eV was calculated as the strain-independent estimate of the core-level, binding-energy uncertainty. The total uncertainty reflected in these results were added in quadrature from the individual uncertainties.

3.4 Discussion

Calculations of the valence band offset due to Van de Walle and Martin[5] are in good agreement with our results. These authors obtain a value of 0.84 eV for Ge on (100) Si and 0.31 eV for Si on (100) Ge. In addition, Schwartz *et al.*[6] have measured shifts in the core level binding energies and core-level energy separations through XPS on strained Ge on (100) Si and strained Si on (100) Ge and obtained offsets of 0.74 ± 0.13 eV and 0.17 ± 0.13 eV, respectively. Our results are also in good agreement with modulation doping experiments of People *et al.*[26] and Abstreiter *et al.*[27] for heterojunctions involving $Si_{1-x}Ge_x$ alloys in intermediate strain configurations. These comparisons were based upon calculations using the interpolation scheme of Van de Walle and Martin.[5] Measurements obtained through other means involving samples in which the strain distributions were not well known yield slightly different results. Kuech *et al.*[28] find $\Delta E_v = 0.39 \pm 0.04$ eV for Ge on (100) Si from reverse-bias capacitance measurements. Through the use of photoemission spectroscopy, Margaritondo *et al.*[29] obtain 0.2 eV for Ge on Si (100) and Mahowald *et al.*[30] measure 0.4 ± 0.1 eV for strained Si on (111)

Ge.

3.5 Chapter Summary

In this chapter, we have described a measurement of the strain dependence of the (100) Si/Ge valence band offset through the use of XPS. Samples were analyzed *in situ*, eliminating uncertainties related to contamination and surface-oxide formation. Si $2p$ and Ge $3d$ core level to valence-band edge and core level to core-level binding energies were determined as a function of in-plane lattice constant, $a_{\parallel}$. Strain configurations in Si and Ge samples grown on relaxed $Si_{1-x}Ge_x$ buffer layers were measured through the use of HRXRD from the asymmetric (422) Bragg reflection. Values for $a_{\perp}$ and $a_{\parallel}$ confirm that these films were grown coherently strained to the buffer layers. In addition, θ-2θ XRD was used to confirm the coherency of the Si/Ge superlattice samples used to measure core level to core-level energy separations. From these techniques, we have obtained the valence band offset for Ge on (100) Si to be 0.83 ± 0.11 eV, and for Si on (100) Ge, we measure 0.22 ± 0.13 eV. These values are in excellent agreement with theoretical predictions[5] and previous experimental results.[6, 26, 27]

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Chapter 4

Study of Segregation in $Si_{1-x}Ge_x$ Alloys

4.1 Introduction

4.1.1 Background

Strained-layer heteroepitaxial semiconductor systems have attracted considerable interest in recent years primarily because of their potential use in novel, high-mobility, electronic devices.[1, 2] Consequently, the processes required to produce high-quality, defect-free material, are being studied extensively. As discussed earlier in this thesis, theoretical calculations[3]-[5] have shown that coherently strained epilayers can be grown to a critical thickness before misfit dislocations appear at the substrate interface and accommodate the strain, causing relaxation. Experimentally, the (100) $Si_{1-x}Ge_x/Si$ material system has recently emerged as the model strained-layer semiconductor system. Most studies of this system have involved samples grown by molecular beam epitaxy (MBE) at temperatures above 400 °C,[6]-[8] with only a few examples of growth at lower temperatures.[9]-[13]

The results presented here were obtained for samples grown coherently strained to (100) Si substrates at temperatures between 310 and 330 °C, and therefore, represent extremely low-temperature growths.

In this chapter, we report results of high-resolution x-ray diffraction (HRXRD) measurements of $a_\perp$ and $a_\parallel$ for $Si_{1-x}Ge_x$ alloys grown on (100) Si. Sample characteristics were chosen to place the samples within a range spanning the empirical critical thickness curve of People and Bean[5] ($h_c(x)$) for growth at 550 °C. Several of these samples, however, were grown at a temperature of only 310 °C and therefore could be grown thicker than h_c, yet still remain coherently strained.[11]-[13] In these cases, HRXRD from the symmetric (400) and asymmetric (422) and (440) Bragg reflections reveals several peaks near the position where one would normally expect to see only a single peak from the alloy. For samples with $h < h_c$, only single peaks are observed. Since HRXRD measurements of $a_\parallel$ corresponding to each peak yield the value for the Si substrate ($a_\parallel = 5.431\,\text{Å}$), we conclude that as h exceeds h_c, compositional segregation may be occurring during growth. We also present results from a simulation, suggesting that this segregation may be occurring in the growth direction.

4.1.2 Outline of Chapter

The remainder of this chapter is organized as follows. In Section 4.2, we describe the sample set prepared for this study and focus on the growth procedure. In addition, the characterization of the samples through the use of HRXRD is discussed. In Section 4.3.1, results from this characterization are tabulated. The data clearly confirm our contention that the films were grown coherently strained and suggest that compositional variation may be occurring for films grown thicker that h_c. In Section 4.3.2, (400) HRXRD scans from two representative samples are presented. Several peaks are shown for the sample grown above h_c while only a single peak is present in the scan from the sample grown thinner than h_c. Results from a third sample are discussed in Section 4.3.3 and are compared with a simulation, assuming that compositional variation is occurring in the growth direction. Finally, our conclusions are given in the Chapter Summary, Section 4.4.

4.2 Experimental

4.2.1 Sample Growth

Table 4.1 summarizes the samples prepared for this study. Samples are given the designation A-B, where A is the intended Ge fraction and B distinguishes them in order of decreasing, intended thickness (column 2). Samples were grown on *n*-type (100) Si substrates (P doped to $1 - 10\,\Omega$-cm) degreased at $50 - 70$ °C in (1,1,1)-trichloroethane (TCA), acetone, methanol, and then rinsed in de-ionized water. The substrates were subsequently etched in a 50% HF and de-ionized water solution and immediately loaded into the Perkin-Elmer 430S Si MBE system (base pressure $< 10^{-10}$ Torr). To desorb SiO_2 and prepare the substrate surface to be atomically smooth, wafers were heated to approximately 800 °C and exposed to a 0.1 Å/ s Si flux until a clear (2×1) reconstruction was observed using *in situ* reflection high-energy electron diffraction (RHEED).[14, 15] A 1200 Å Si buffer layer was grown as the substrate temperature slowly decreased from 700 °C to 530 °C. Finally, the substrate temperature was lowered to the desired growth temperature and the $Si_{1-x}Ge_x$ alloy layer was grown. During this phase, Si and Ge were codeposited from an Edwards/Temescal, dual *e*-beam evaporation source with fluxes monitored by a cathodoluminescent flux sensor (Inficon, Sentinel III). Si and Ge deposition rates were calibrated by measuring the periods of $Si_{1-x}Ge_x/Si$ superlattices with θ-2θ x-ray diffraction (θ-2θ XRD) and verified with cross-sectional transmission electron microscopy (TEM). Wafer temperatures were calibrated using an optical pyrometer (Ircon, W-series accurate between 300 and 800 °C) and corroborated through *in situ* observations of Au/Si and Al/Si eutectics. The temperatures quoted are estimated to be accurate to ±20 °C.

4.2.2 Sample Characterization Using HRXRD

Strain measurements were obtained through HRXRD from the symmetric (400) and asymmetric (422) and (440) Bragg reflections in the substrate and heteroepitaxial film. Cu K_α radiation was selected using a Ge four-crystal monochromator and collimated onto the sample. A detector was placed near the expected angle (with respect to the incident beam) for the $n = 1$ Bragg reflection from the substrate, and the sample was subsequently rotated through the correct Bragg condition. Asymmetric measurements of $a_\parallel$ on samples 40-1, 25-1, 25-2, 25-3, 20-1, and 20-3, all yielded the value for unstrained Si (5.431 Å) to within 0.001 Å. As a result, the samples were generally assumed to be coherently strained and the Ge fraction, x, was calculated from HRXRD measurements of $a_\perp$, using the expression[12]

$$d_x(\eta) = d_{\mathrm{Si}}\,[1 + (4.18\%)(1 + \eta\epsilon_{\mathrm{T}})x] \tag{4.1}$$

with η, the fraction of coherent strain, set equal to 1. The derivation of Eq. 4.1 assumes that the tetragonal distortion parameter, ϵ_{T}, relates the strains parallel and perpendicular to the interface through[6]

$$\epsilon_\perp/\epsilon_\parallel = -\epsilon_{\mathrm{T}}, \tag{4.2}$$

with ϵ_{T} set equal to 0.76 for the present study. The Ge fraction, x, obtained in this way appears in column 3 of Table 4.1. Six samples were observed to have several peaks in their x-ray spectrum. Since the peaks have been observed to be coherently strained, we conclude that the most likely explanation is a chemical segregation has occurred. As a result, a range of compositions appears in the table for each.

In addition to the film thickness and Ge fraction, Table 4.1 contains other important characteristics of the samples. The empirical 550 °C critical thickness, h_c, calculated from the expression[2]

$$h_c \cong \left(\frac{1.9 \times 10^{-2}\,\text{Å}}{f^2}\right) \ln\left(\frac{h_c}{4\,\text{Å}}\right) \tag{4.3}$$

appears in column 4 of the table. Incorporated into the misfit, f, is the Ge fraction described above. Using these values for h_c, the value h/h_c appears in column 5 and is used for qualitative comparison between samples. Finally, the growth temperature of each sample is recorded in the sixth column. Note, all samples that have multiple peaks in their x-ray spectrum have ranges associated with their Ge fractions and therefore will also have ranges associated with any parameters calculated from the samples.

4.3 Results and Discussion

4.3.1 HRXRD Measurements of $a_\perp$ and $a_\parallel$

Table 4.2 contains the results of measurements of $a_\perp$ and $a_\parallel$ using HRXRD. Sample thicknesses (h) and alloy compositions (x) were chosen to span a range varying from below to above the empirical, critical thickness. Symmetric (400) HRXRD shows that samples with $h > h_c$ typically have multiple peaks (with the only exception being sample 40-1), while samples grown below critical thickness are singly peaked. Furthermore, the observed peaks are extremely sharp and yield film thicknesses in excellent agreement with intended thickness; however,

Sample	h (Å)	x (%Ge ±0.2)	h_c(Å)	h/h_c	T_g (°C)
40-1	900	36.6	392	2.30	310
25-1	5000	20.4-24.9	1024-1659	3.01-4.88	310
25-2	2900	25.6-26.4	888-957	3.03-3.27	310
25-3	2000	21.4-23.4	1192-1479	1.35-1.68	310
20-1	5000	20.0-21.2	1513-1740	2.87-3.30	330
20-2	5000	20.4-20.3	1495-1659	3.01-3.34	310
20-3	5000	16.8-17.4	2424-2634	1.90-2.06	310
20-4	1200	18.4	2123	0.57	500
20-5	1200	19.6	1826	0.66	330
15-1	2500	15.3	3283	0.76	500
15-2	2500	15.5	3185	0.78	310

Table 4.1: Growth characteristics of the $Si_{1-x}Ge_x/Si$ sample set. Quoted ranges span the entire multiple-peak spectrum for relevant samples.

this may simply be a fortuitous result of interference between neighboring regions of different composition.

4.3.2 Representative HRXRD Scans

X-ray data from two representative samples analyzed using HRXRD are shown in Figs. 4.1 and 4.2. Data displayed in Fig. 4.1 are from sample 20-1 ($h > h_c$) grown at 330 °C. Four peaks are clearly visible and are seen to be extremely sharp in comparison with the substrate peak. Inset for clarity, the multiply peaked alloy spectrum is shown (solid curve) with a theoretical x-ray spectrum (dashed curve) for a 5000 Å $Si_{0.793}Ge_{0.207}$ film. The peak widths are almost equal. It should be noted here that since the full width at half maximum (FWHM) of the (400) reflection for sample 40-1 is approximately 4.5 times that of sample 20-1, we suspect that any segregation present in 40-1 would be obscured. The observed broadening in the samples can be easily shown to be consistent with finite-film thickness effects. In Fig. 4.2, the x-ray spectrum for sample 15-1 is shown. The spectrum is dominated by a single peak corresponding to a 15.3% Ge fraction in a 1500 Å film grown at 500 °C. The spectrum from 15-2 is nearly identical. The sharp peak is accompanied by Pendelossung[16] thickness fringes, indicative of exceptional crystalline quality. Samples 15-1 and 15-2 demonstrate that pathological fluxuations in Si or Ge fluxes are probably not responsible for the observed multiple peak spectra.

4.3.3 Simulation of Multiple-Peak HRXRD Data

HRXRD data from (400) planes of a third sample, 25-1, intended to be grown at $x = 0.25$ to about $5h_c$ are presented in Fig. 4.3 (solid curve). Several peaks are observed and HRXRD from (422) planes shows the entire spectrum to be coher-

Sample	$a_\perp$ (400)	$a_\perp$ (422)	$a_\parallel$ (422)	$a_\perp$ (440)	$a_\parallel$ (440)
40-1	5.577	5.578	5.431	...	...
25-1	5.512-5.530	5.513-5.531	5.431	...	...
25-2	5.533-5.536	5.534-5.538	5.430-5.431	5.534-5.537	5.431
25-3	5.517-5.524	5.519-5.524	5.429-5.430	5.519	5.430
20-1	5.511-5.516	5.514	5.431	...	...
20-2	5.513-5.516	...	...	...	...
20-3	5.498-5.500	5.497-5.498	5.431-5.432	...	...
20-4	5.504	...	...	...	...
20-5	5.509	...	...	...	...
15-1	5.492	...	...	...	...
15-2	5.493	...	...	...	...

Table 4.2: Results from HRXRD measurements of $a_\perp$ and $a_\parallel$ performed on the sample set prepared for this study. Values quoted are accurate to within 0.001 Å.

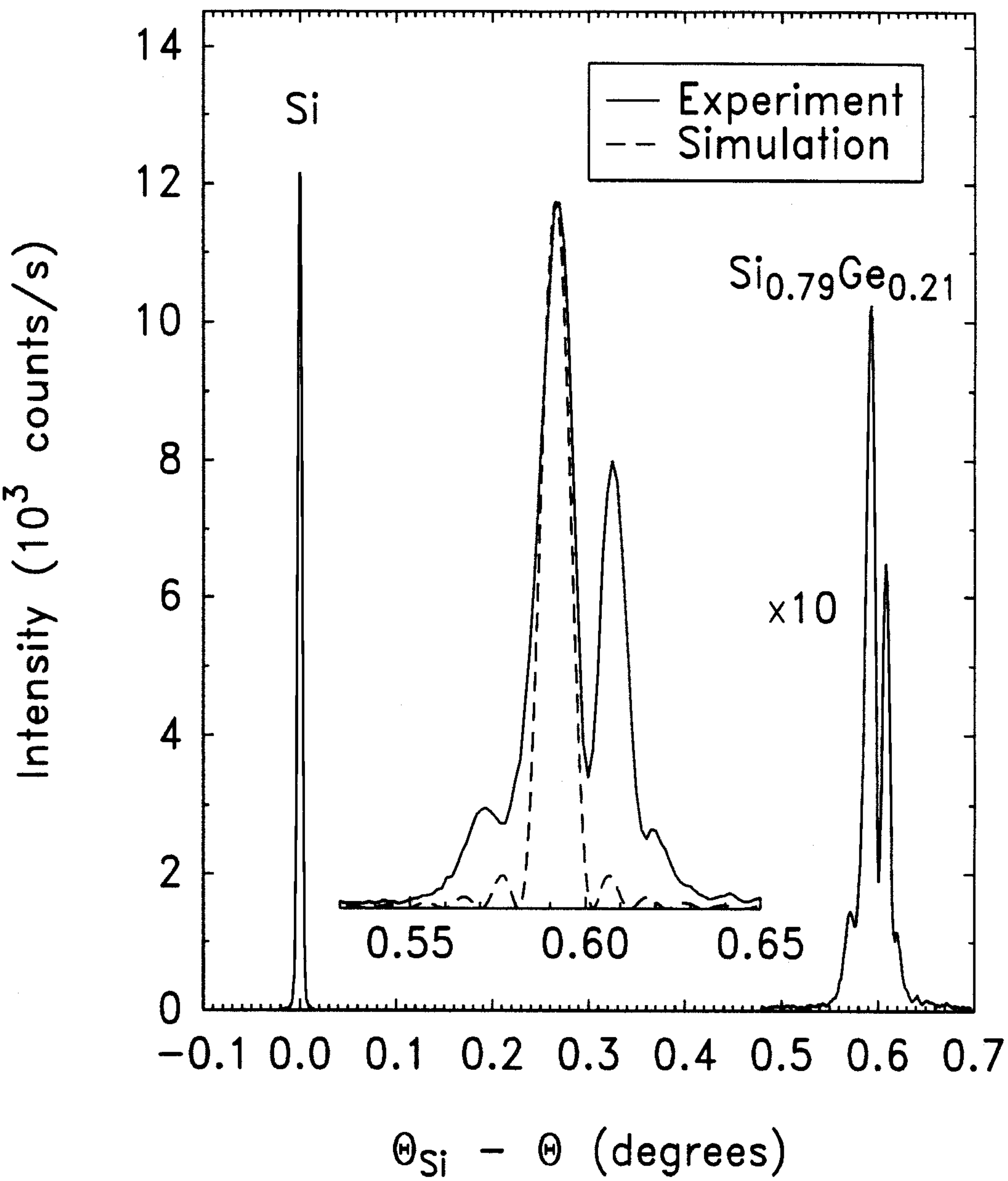

Figure 4.1: (400) HRXRD from sample 20-1. Diffraction from the alloy layer is shown to be composed of four distinct peaks. The alloy peaks are inset against a simulated x-ray spectrum from a 5000 Å $Si_{0.793}Ge_{0.207}$ layer. Note that the width of the strongest alloy peak is comparable to the simulation.

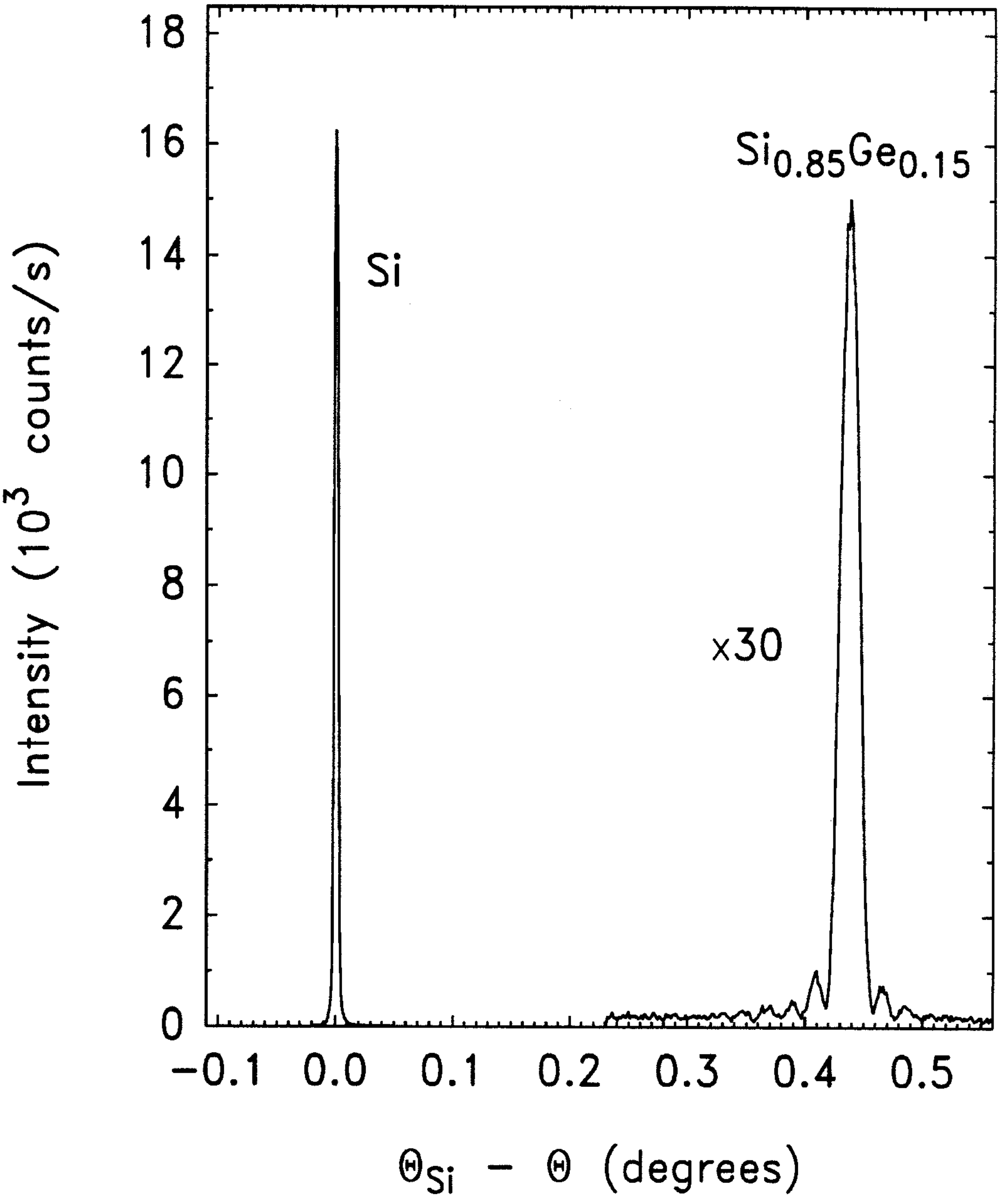

Figure 4.2: (400) HRXRD from sample 15-1. The alloy peak is extremely sharp with Pendelossung thickness fringes. The film thickness calculated from these fringes agrees well with intended thickness.

ently strained. The peaks correspond to compositions ranging from 20.4 – 24.9% Ge. These data present considerable difficulty when one attempts to understand their origin. Since the film has been shown to be coherently strained to the substrate, one is led to the conclusion that chemical segregation is taking place in the sample. Since only samples grown in excess of the critical thickness show this effect, we believe it to be due to the presence of excess strain, although preliminary calculations have not yet supported this contention. Attempts to observe such an effect in sample 20-1 (the sample analyzed for Fig. 4.1) with TEM have been unsuccessful thus far, since the thicknesses of the samples have been so large that segregation cannot be distinguished from bend contours produced during the preparation of the TEM specimen. Therefore, at present, conclusions cannot be made concerning the microscopic details of the segregation that we have apparently observed.

If we assume that segregation occurs in layers parallel to the interface, we can approximately reproduce the results from sample 25-1 through simulation. The dashed curve of Fig. 4.3 is the simulated (400) x-ray spectrum from a 5000 Å sample containing 3 layers with the Ge fraction varying from 20.6 – 25.2%. The layer structure is shown in the figure. Although we realize that this particular structure is not the only one that reproduces the results from 25-1, we present it simply to suggest that it is possible for the segregation to occur parallel to the interface.

4.4 Chapter Summary

In summary, high-quality, coherently strained $Si_{1-x}Ge_x$ alloy layers have been grown on (100) Si at extremely low temperatures. Samples grown in excess of the critical thickness show multiple peaks in HRXRD and those below h_c are singly

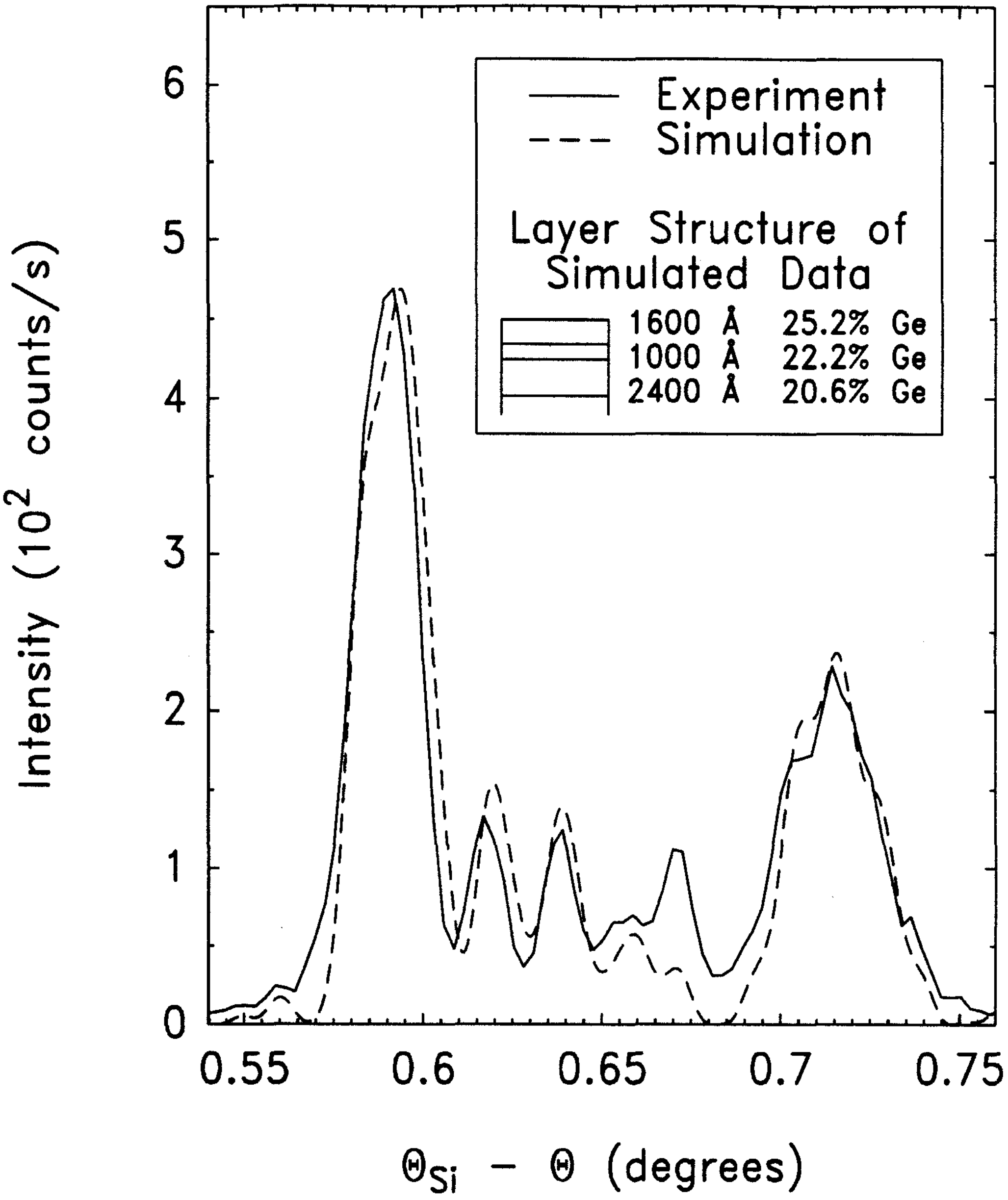

Figure 4.3: (400) HRXRD from sample 25-1. Several peaks are visible in the actual data (solid curve). The dashed curve shows how results from a simulation incorporating three layers of varying alloy composition compare with the data. Although this is not the only structure that approximately reproduces the data, we present it simply to suggest that compositional variation perpendicular to the interface may be occurring.

peaked. Since the samples are shown to be highly coherent, chemical segregation has been identified as the most likely explanation for this observation. Attempts to observe this with TEM have been unsuccessful thus far. Further study will, it is hoped, determine the microscopic details of this effect.

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Chapter 5

Observation of a (2×8) Reconstruction on Surfaces of (100) $Si_{1-x}Ge_x$ Alloys

5.1 Introduction

5.1.1 Background

Interest in the $Si_{1-x}Ge_x/Si$ material system has increased dramatically in recent years primarily because of the enormous potential for fabricating novel heterojunction devices compatible with existing, Si-based processing technologies. Recent results[1, 2] point to material quality as the single most important factor in determining device performance; therefore, a study of the physical mechanisms of epitaxial growth is extremely timely. Once these mechanisms are understood, growth conditions can be adjusted to produce the highest-quality material possible. To this end, the study presented here focuses on surfaces of $Si_{1-x}Ge_x$ alloys grown epitaxially on (100) Si substrates by molecular beam epitaxy (MBE).

In this chapter, reflection high-energy electron diffraction (RHEED) and low-energy electron diffraction (LEED) techniques are used to study the surface reconstruction of $Si_{1-x}Ge_x$ alloys grown on (100) Si substrates. Most of the samples studied were grown below the 550 °C empirical, critical thickness curve of People and Bean[3] with the exception of one, which was deliberately relaxed through the use of a high-temperature anneal. RHEED and LEED patterns from these surfaces indicate the presence of a (2×8) surface reconstruction with the "8" direction aligned perpendicular to the dimerization direction. $(2 \times n)$ reconstructions have been observed previously on clean (100) Si after a quenching from high temperatures[4, 5] and on (100) Si contaminated with Ni[6] and Cu[7] impurities. Our samples have been determined through the use of secondary ion mass spectroscopy (SIMS) to be free of such metallic impurities.

We present experimental evidence suggesting that the (2×8) reconstruction is a thermodynamically favored arrangement of Ge dimers ordering in a direction perpendicular to the dimerization direction of a (2×1) Si-surface reconstruction. Similar models have been proposed previously to explain the (100) Si $(2 \times n)$ reconstructions. Martin *et al.*[5] concluded that these reconstructions result from ordered phases of missing-dimer defects, a conclusion based on an earlier treatment by Pandey.[8] Further refinements to this model made by Aruga *et al.*[9] detail a mechanism for ordering arising from lattice strain surrounding the defects. In our model, Ge dimers play the same role as the missing-dimer defects. Local strains surrounding each Ge dimer drive the reconstruction toward the ordered phase. Presumably, an optimal configuration exists when Ge dimers are located at every eighth site. To support our conclusions, we present simulated diffraction patterns from one-dimensional atomic chains. The calculated patterns are consistent with the interpretation that fractional order peaks observed experimentally are due to ordered Ge dimers on the surface. Finally, simulations including strain effects are shown to predict qualitatively the relative intensities of the fractional order peaks.

5.1.2 Outline of Chapter

The chapter has been organized along the same lines as preceding chapters. First, experimental details are discussed in Section 5.2, concentrating on the growth procedures employed in the fabrication of the samples and the *in situ* characterization techniques used to study surface reconstructions. In Section 5.3, we present the results of the study and suggest a model for the structure of the (2×8) reconstruction we have observed. Here, RHEED and LEED observations are summarized in Sections 5.3.1 and 5.3.2. In addition, Section 5.3.3 surveys the range of growth parameters necessary for the formation of the (2×8) reconstruction. In Section 5.3.4, we present results from a kinematical calculation of diffraction from an ordered, linear chain consistent with our contention that Ge dimers are ordering in a direction parallel to the dimer chains normally seen on clean, (100) Si surfaces. Finally, our conclusions are summarized at the end of the chapter, in Section 5.4.

5.2 Experimental

5.2.1 Sample Preparation by MBE

Single-crystal $Si_{1-x}Ge_x$ alloys were grown for this study on (100) Si (±1 °) substrates by molecular beam epitaxy (MBE). Substrates were degreased in (1,1,1)-trichloroethane (TCA), acetone, methanol, and de-ionized water prior to etching in a 50% HF solution for the purpose of removing any SiO_2 present on the surface. After the etch, the substrates were again rinsed in de-ionized water and removed slowly, eliminating the need to dry the samples with nitrogen, since the etched Si is hydrophobic. Recently, we have used this technique since we felt that blow-drying the substrates needlessly introduces particulates on the surface. Subsequently, the substrates were loaded into one of two ultrahigh-vacuum (UHV)-deposition chambers in which *in situ* growth and characterization of the alloy surfaces were performed.

Samples prepared for study using the RHEED technique were grown in the Perkin-Elmer (Model 430S) Si MBE system. LEED analysis was performed in the Si-silicide deposition system. Both growth chambers were discussed previously in Section 1.2.1. Prior to alloy-layer growth, the substrate temperature was taken to approximately 860 °C and exposed to a 0.1 Å/s Si flux in order to remove any remaining oxide.[10, 11] Then, a several-hundred-Angstrom thick Si buffer was grown while the temperature was ramped from 700 °C to approximately 500 °C. RHEED and LEED patterns from surfaces prepared in this way are extremely sharp incoherent superpositions of the (2×1) and (1×2) patterns expected for pure, reconstructed (100) Si surfaces containing a roughly equal mixture of (2×1) and (1×2) domains.[12] Although it is possible to form preferentially one type of domain through the use of off-axis substrates,[12, 13, 14] such an attempt was not undertaken here. Henceforth, references to $(n \times m)$ surface symmetries should be interpreted as incoherent superpositions of $(n \times m)$ and $(m \times n)$ symmetries.

5.2.2 *In situ* Surface Analysis Techniques

The surface periodicities of our samples were analyzed *in situ* through the use of RHEED and LEED analytical techniques. As indicated above, LEED patterns were obtained from samples grown in a custom-built MBE growth chamber. The apparatus consists of a Princeton Research Instruments, reverse-view LEED optical system mounted on a 6 inch flange to the side of the sample heater. Typical beam energies ranged from 30 – 100 eV. Patterns appearing on the phosphor screen were photographed with a Nikon (Model F3/T) 35 mm camera loaded with 3200 ASA film. RHEED patterns were obtained from samples grown in the Perkin-Elmer Si MBE growth chamber. In this case, a 10 keV electron beam was diffracted from the sample at glancing incidence. Patterns were recorded digitally through the use of a Cohu, solid-state, charge-coupled device (CCD) camera, an S-VHS video recorder, an Analogic (Model DASM) frame grabber, and a Sun SPARC$^{\mathrm{TM}}$station. Each image consists of a 512 × 512 array of single-byte data (1 MB/frame). Recording the images in this way allows a great deal of flexibility in analyzing the data. For instance, several rows of data can be selected and averaged together to improve signal to noise and can accurately measure the separation between streaks in a RHEED pattern.

5.3 Results and Discussion

5.3.1 RHEED Observations

Summarized in Table 5.1 are the growth and anneal sequences of three representative samples prepared for this study. Each of these samples exhibits new, fractional-order, surface periodicities in their RHEED or LEED patterns under certain growth conditions. In Fig. 5.1, we present digitally acquired data taken from the RHEED pattern of sample A. Prior to acquiring the data, the sample was briefly annealed to 700 °C and cooled to 450 °C (step 5). We found that this procedure significantly improves the sharpness of the observed patterns. Clearly visible in the figure are the usual (00), ($\frac{1}{2}$0), and (10) diffraction orders characteristic of a Si-like (2 × 1) reconstruction. However, additional, fractional-order

Sample	Step	Description	Technique	Symmetry
A	1	200 Å $Si_{0.80}Ge_{0.20}$ at 450 °C	RHEED	(2 × 8)
	2	anneal *in situ* at 700 °C for 30 min	RHEED	diffuse (2 × 1)
	3	200 Å $Si_{0.80}Ge_{0.20}$ at 230 °C	RHEED	spotty
	4	anneal *in situ* at 700 °C for 30 min	RHEED	diffuse (2 × 1)
	5	cooldown to 450 °C	RHEED	sharp (2 × 8)
	6	5000 Å $Si_{0.80}Ge_{0.20}$ at 450 °C	RHEED	diffuse (2 × 8)
	7	anneal *in situ* at 700 °C for 3 h	RHEED	diffuse (2 × 1)
	8	cooldown to room temperature	RHEED	diffuse (2 × 8)
B	1	200 Å $Si_{0.89}Ge_{0.11}$ at 540 °C	LEED	(2 × 1)
	2	200 Å $Si_{0.80}Ge_{0.20}$ at 540 °C	LEED	(2 × 8)
	3	100 Å $Si_{0.70}Ge_{0.30}$ at 540 °C	LEED	diffuse (2 × 1)
C	1	500 Å Si at 550 °C	LEED	(2 × 1)
	2	200 Å $Si_{0.82}Ge_{0.18}$ at 550 °C	LEED	(2 × 8)

Table 5.1: Growth sequences for the $Si_{1-x}Ge_x/Si$ sample set used in this study. Surface symmetries were determined after each step, using the indicated technique. The diffraction patterns from these samples actually exhibited a two-domain pattern for which the symmetries are related by a 90 ° rotation.

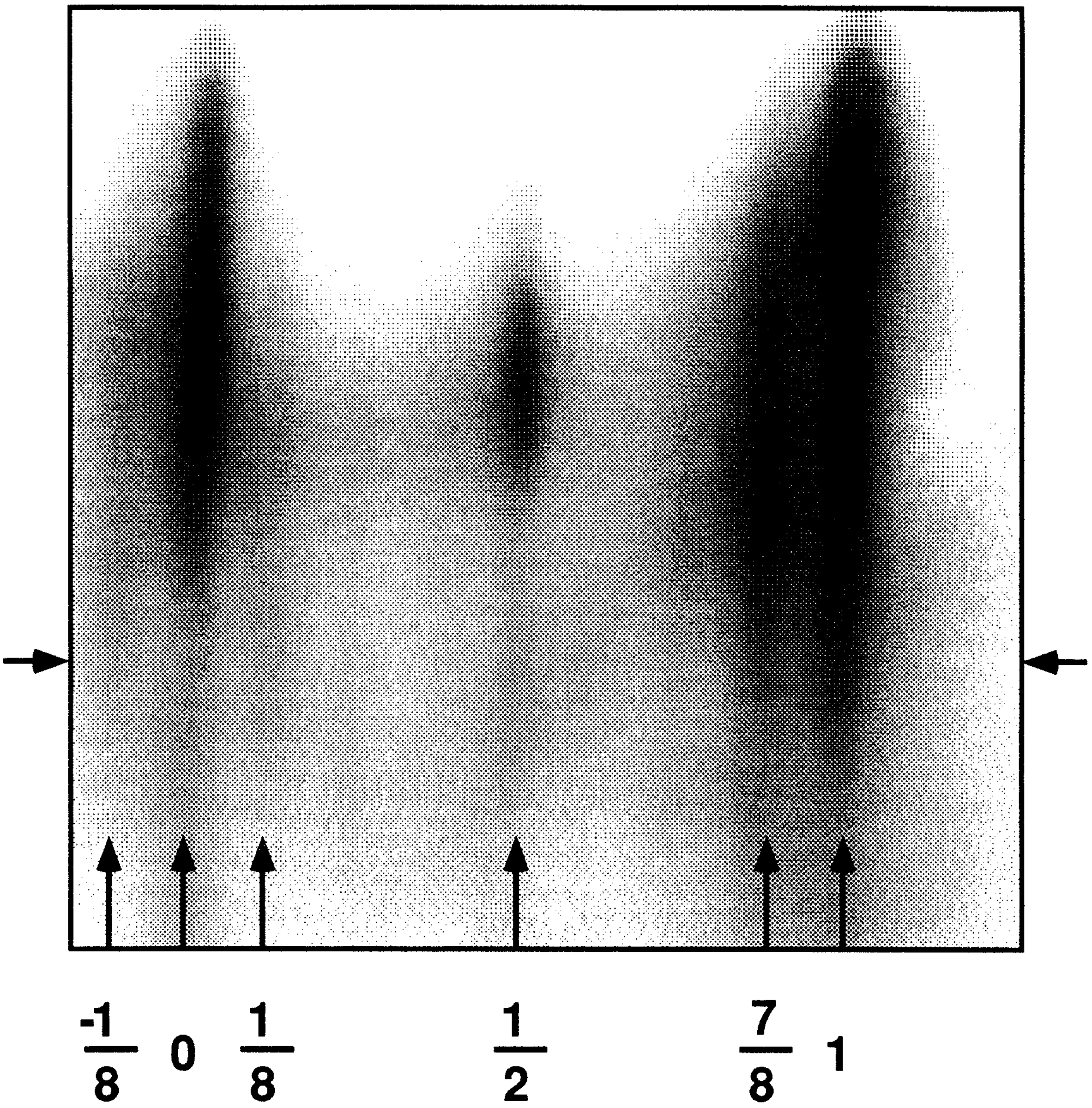

Figure 5.1: Gray-scale image of the RHEED pattern from sample A after completion of step 5, shown slightly off from a <011> azimuth. In the image, white represents low, and black represents high intensities. Visible in the figure are the (00), ($\frac{1}{2}$0), and (10) streaks usually seen for pure, reconstructed (100) Si surfaces. In addition, several fractional orders are also distinguishable.

streaks, corresponding to $(\pm\frac{1}{8}0)$ and $(\frac{7}{8}0)$ diffraction orders, are also evident. These extra streaks are absent from the diffraction patterns of pure Si, and the diffraction patterns of more Ge-rich films are qualitatively different.[15]

A closer inspection of the RHEED pattern is required to resolve the fractional-order streaks not clearly distinguishable by the eye in Fig. 5.1. For this purpose, 15 lines of data were taken from the position marked by the arrows and averaged together to improve signal to noise. The resulting "linescan" is shown in Fig. 5.2. As a result of the signal-to-noise improvement, the $(\frac{1}{4}0)$, $(\frac{3}{8}0)$, and $(\frac{3}{4}0)$ streaks can be resolved in addition to the $(\frac{1}{8}0)$ and $(\frac{7}{8}0)$ streaks. Using a standard numerical peak-finding algorithm,[16] the positions of each of the streaks can be plotted as a function of streak order. Since there are seven equally spaced, fractional-order peaks between each integer order, we conclude that the reconstruction is eight-fold-periodic. The plot shown in Fig. 5.3 thereby validates the $n/8$ indexing scheme used here.

5.3.2 LEED Observations

As discussed earlier, samples for this study were grown on (100) Si substrates that were degreased and etched in a 50% HF solution prior to loading into the UHV deposition chamber. Once inside the growth chamber, an atomically clean Si surface was prepared through the use of an *in situ* oxide-desorption procedure followed by growth of a pure Si buffer layer. The LEED pattern from a substrate prepared in this way is shown in Fig. 5.4. Integer and half-integer order spots are clearly visible in the figure. After we obtained a clean (2×1) Si surface, 200 Å $Si_{0.82}Ge_{0.18}$ were deposited onto the substrate at a temperature of approximately 550 °C (sample C). The LEED pattern from this sample is shown in Fig. 5.5. Visible in the figure are additional fractional-order diffraction spots located near

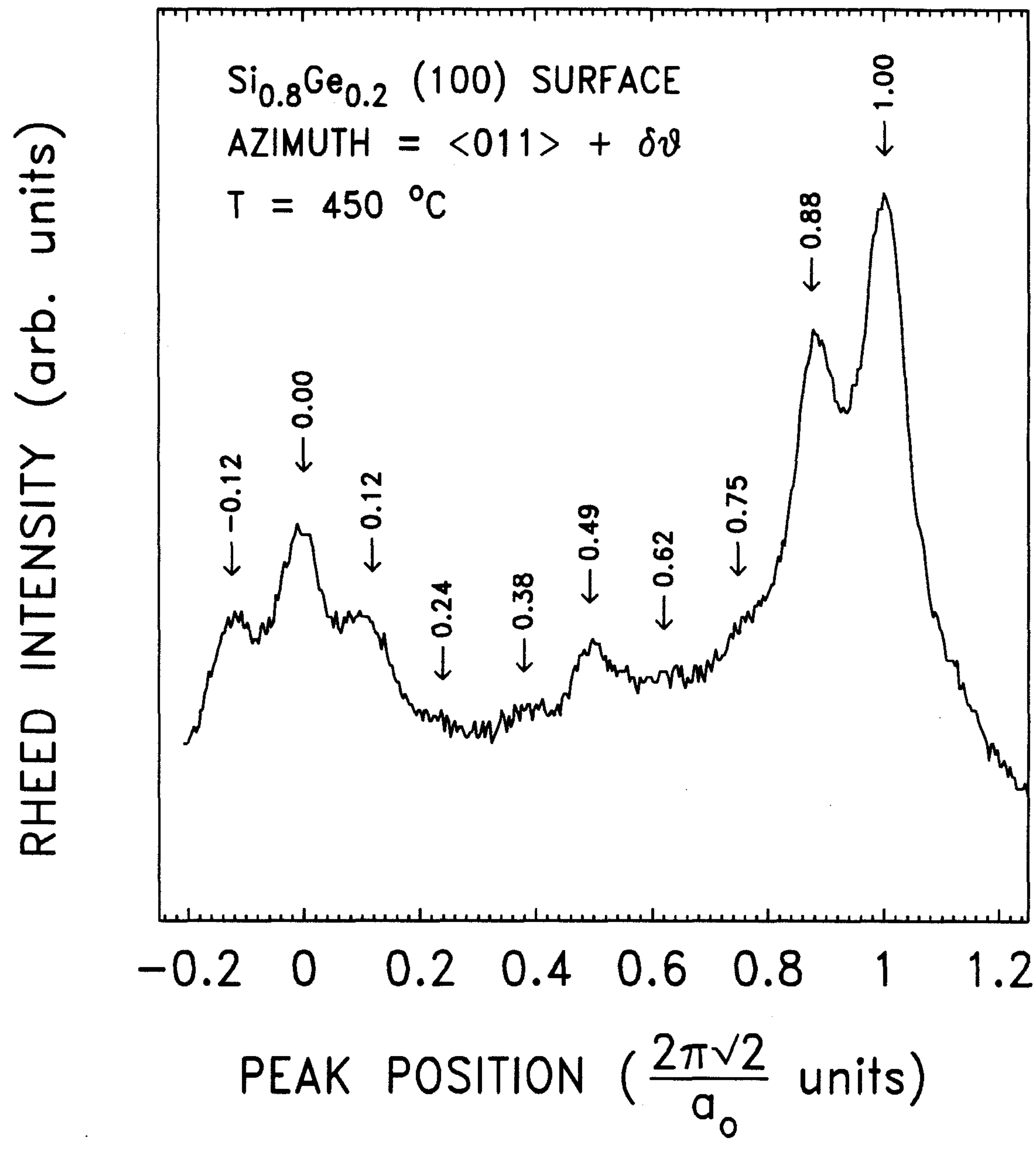

Figure 5.2: Linescan of 15 averaged pixel rows taken from the location indicated in Fig. 5.1 above. The resulting signal-to-noise improvement reveals the presence of additional fractional orders. Peak positions, indicated, were identified with the aid of a numerical peak-finding algorithm.[16]

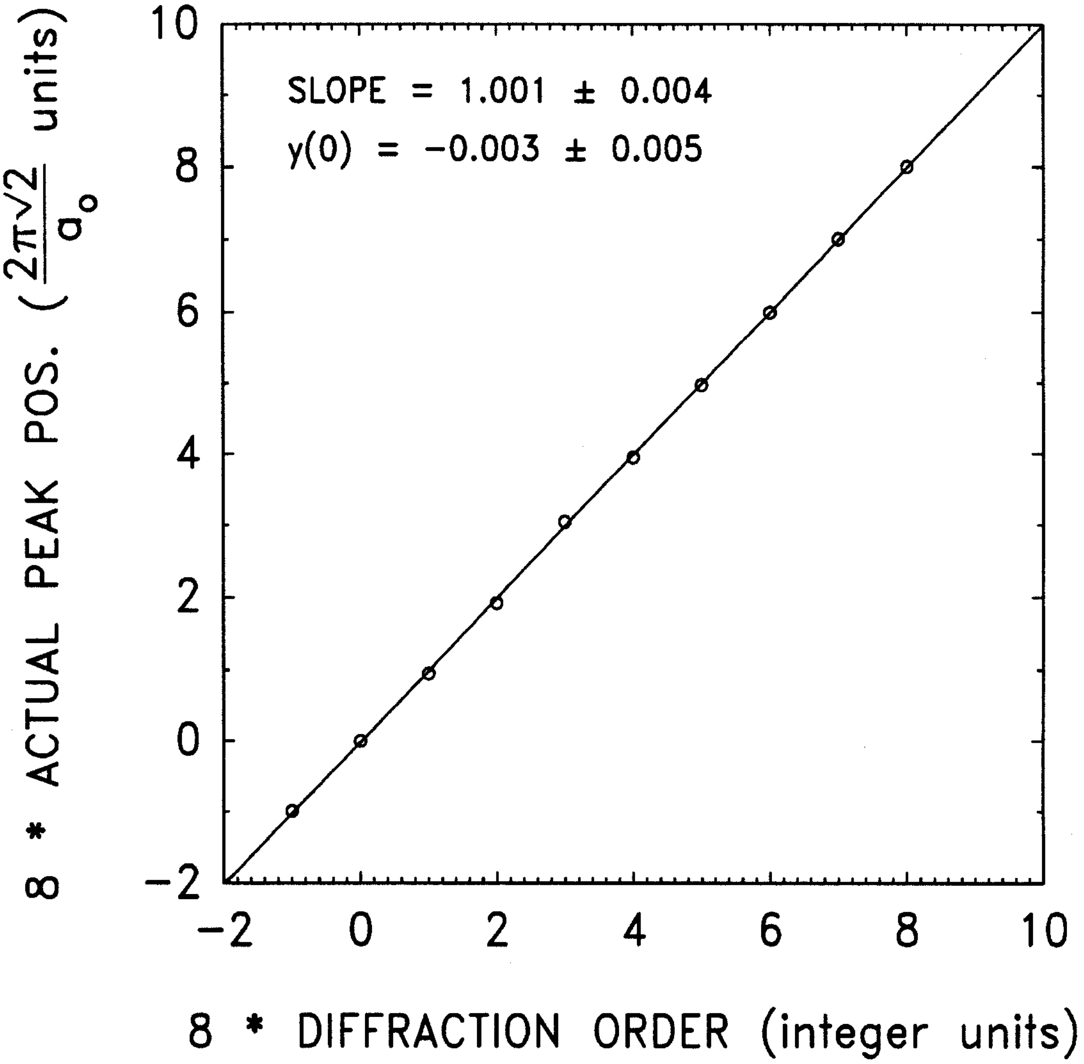

Figure 5.3: Peak Position vs. Diffraction Order for the peaks identified in Fig. 5.2. The data strongly support the $n/8$ indexing scheme used here.

integer and half-integer spots of the (2 × 1) reconstruction. The presence of fractional-order spots suggests that a long-range periodicity is present on the surface.

The fact that only one set of fractional order spots occurs near each half-integer spot indicates the long-range periodicity is aligned with the direction of the dimer chains of a pure Si (2 × 1) reconstruction.[15] Therefore, we conclude that the pattern we have observed results from an incoherent superposition of patterns associated with (2 × 8) and (8 × 2) domains. The schematic diagram shown in Fig. 5.6 elucidates the above conclusion. In the figure, (2 × 1) spots (large circles) are associated with $n/8$-order satellite peaks (small circles) along the long direction of the reciprocal unit cell. Such additional peaks are what one might expect if, for example, every 8th position along the dimer chains is occupied by a Ge atom. Additionally, $n/8$-order peaks will result even if the ordering is imperfect, so long as the pair-correlation function of surface Ge atoms exhibits an 8-fold periodicity which extends for a distance of at least the order of one LEED/RHEED coherence length.

5.3.3 Dependence on Growth Parameters

In an attempt to establish the importance of growth conditions on the (2 × 8) reconstruction, several issues were addressed. For example, $n/8$-order diffracted beams are observed only on $Si_{1-x}Ge_x$ surfaces for which x lies in the range 0.11–0.30. LEED studies of the surface of sample B demonstrate this compositional dependence. For $x \leq 0.11$, (2 × 1) symmetry is observed, consistent with what has been observed for pure Si (100). Samples for which $x \geq 0.30$ exhibit a diffuse (2 × 1) symmetry, and for higher Ge concentrations, become faceted.[15] For x between 0.11 and 0.30, $n/8$ fractional-order spots are observed in LEED

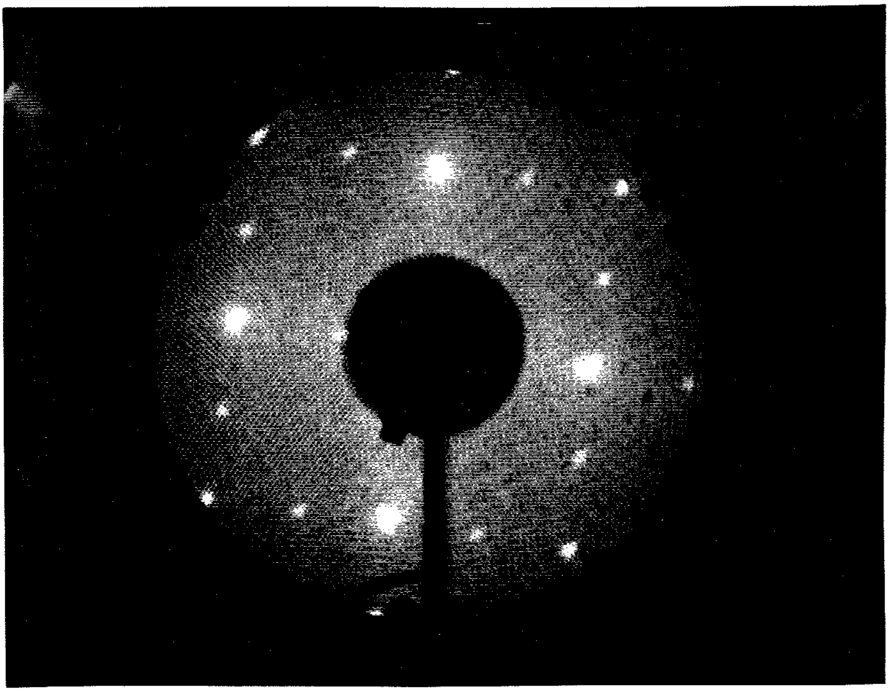

Figure 5.4: LEED pattern from a clean (100) Si surface. Integer and half-integer diffraction spots are visible because of the usual (2×1) reconstruction. $E_{\mathrm{beam}} \approx 47$ eV.

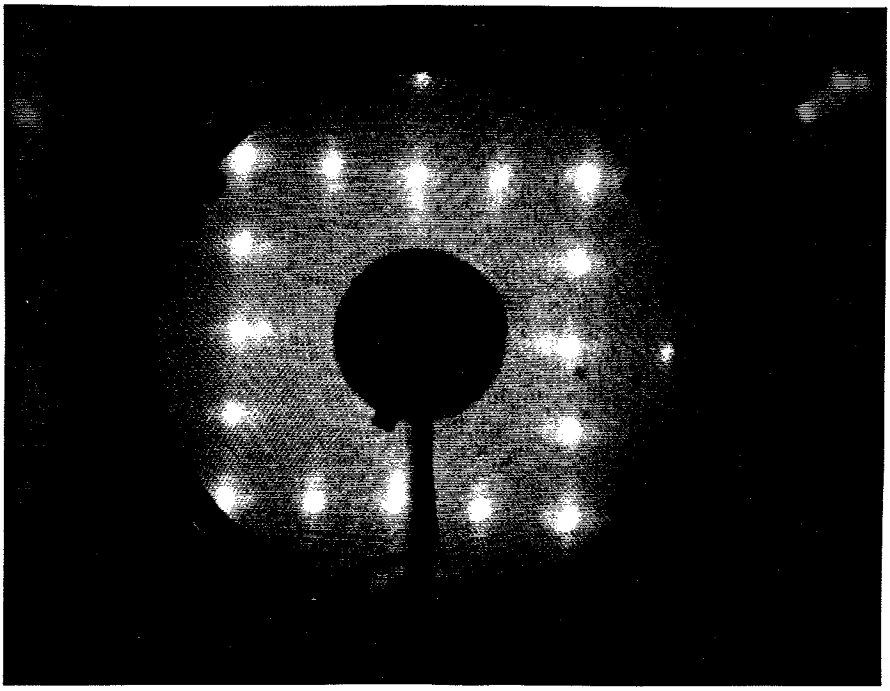

Figure 5.5: LEED pattern from a 200 Å $Si_{0.82}Ge_{0.18}$ alloy grown at 550 °C (sample C). Clearly visible are the $n/8$-order diffraction beams also seen in the RHEED patterns taken from samples grown under similar conditions. The pattern suggests the presence of an 8-fold-periodic modulation in electron-scattering factor across the surface. $E_{\text{beam}} \approx 47$ eV.

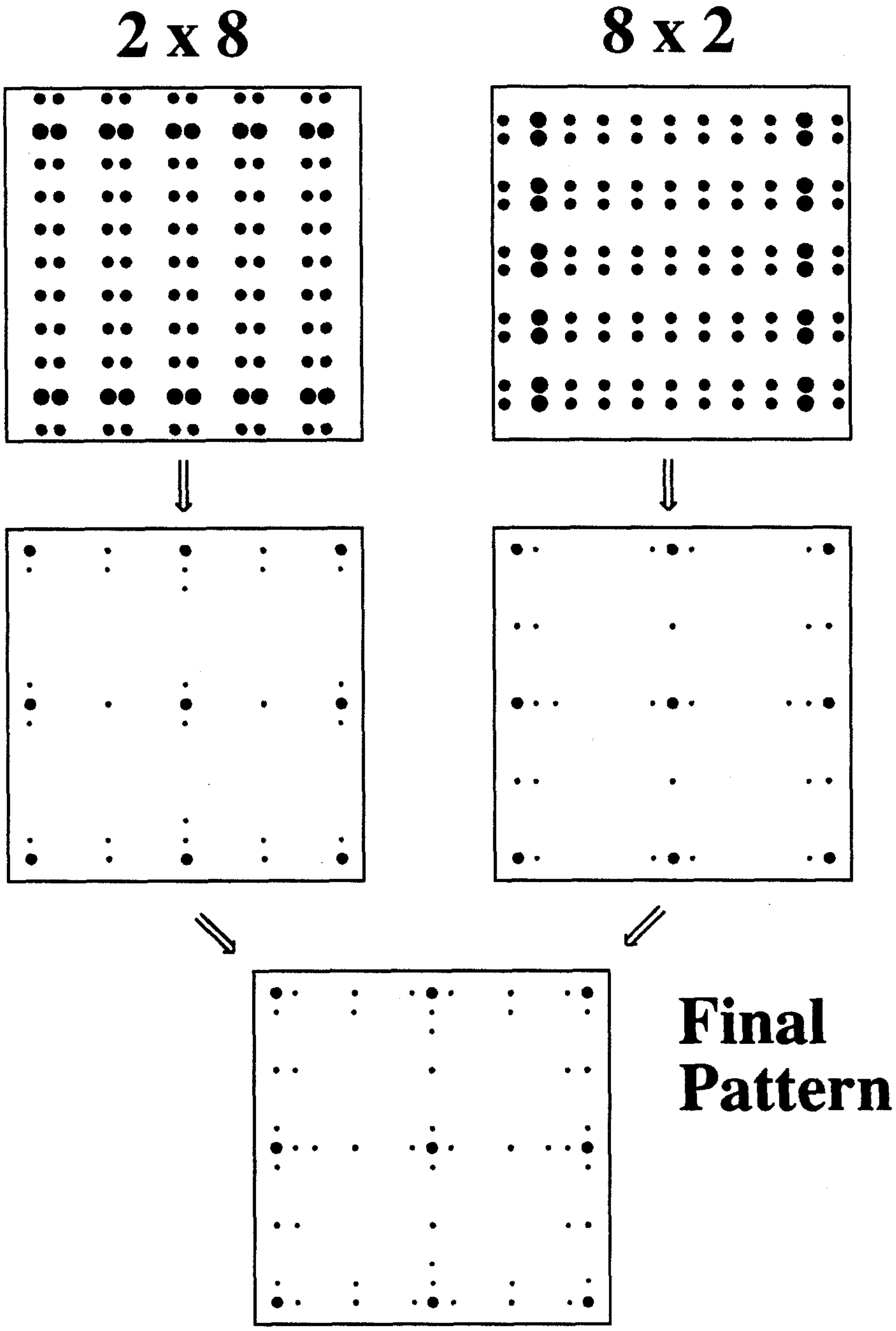

Figure 5.6: Schematic of the LEED pattern expected for a real-space (2 × 8) scattering-factor modulation imposed on a (2 × 1) domain. A similar pattern (rotated by 90 °) is associated with a (1 × 2) domain. The mixed-domain LEED pattern in Fig. 5.5 corresponds to an incoherent superposition of the two patterns.

patterns, entirely consistent with the $n/8$ fractional-order streaks observed in RHEED patterns for sample A. Although the spacing of fractional-order spots does not appear to change with composition, some variation in the sharpness and intensity of these beams has been observed. The sharpest patterns were obtained on samples with compositions between 10 and 20% Ge.

In addition to composition, growth temperature has also been observed to affect the appearance of the (2×8) reconstruction. As the growth temperature is reduced below 350 °C, the (2×8) symmetry observed in RHEED patterns immediately after growth of the alloy layer becomes diffuse and eventually turns spotty, suggesting that surface mobility plays a crucial role in the formation of the reconstruction. The surfaces of samples grown at higher temperatures ($\sim$ 500 °C) routinely exhibit (2×8) symmetry. As a result, most of our samples were grown at temperatures within the range 450–550 °C.

Sample A was intentionally grown at low temperature in order to determine the thermal stability of the (2×8) reconstruction. The RHEED pattern from a 200 Å $Si_{0.80}Ge_{0.20}$ alloy layer grown at 230 °C is shown in Fig. 5.7. As indicated by the spots in the pattern, the sample surface immediately after growth was very rough. The sample was subsequently heated to 700 °C in 10 minutes. As the temperature climbed above 450 °C, the RHEED pattern improved considerably. The spots were replaced by sharp streaks, indicating that the surface had become smooth once again. Also, fractional-order streaks became visible. At 700 °C, the fractional-order peaks became difficult to see, perhaps because of thermal diffuse scattering. After the anneal, the heater power was cut off and the sample temperature was allowed to "freefall" back to room temperature. The RHEED pattern taken after the anneal is shown in Fig. 5.8. The fractional-order streaks were sharper after the anneal than while the temperature was rising to the anneal temperature. Since a high-temperature anneal did not destroy the ordering in

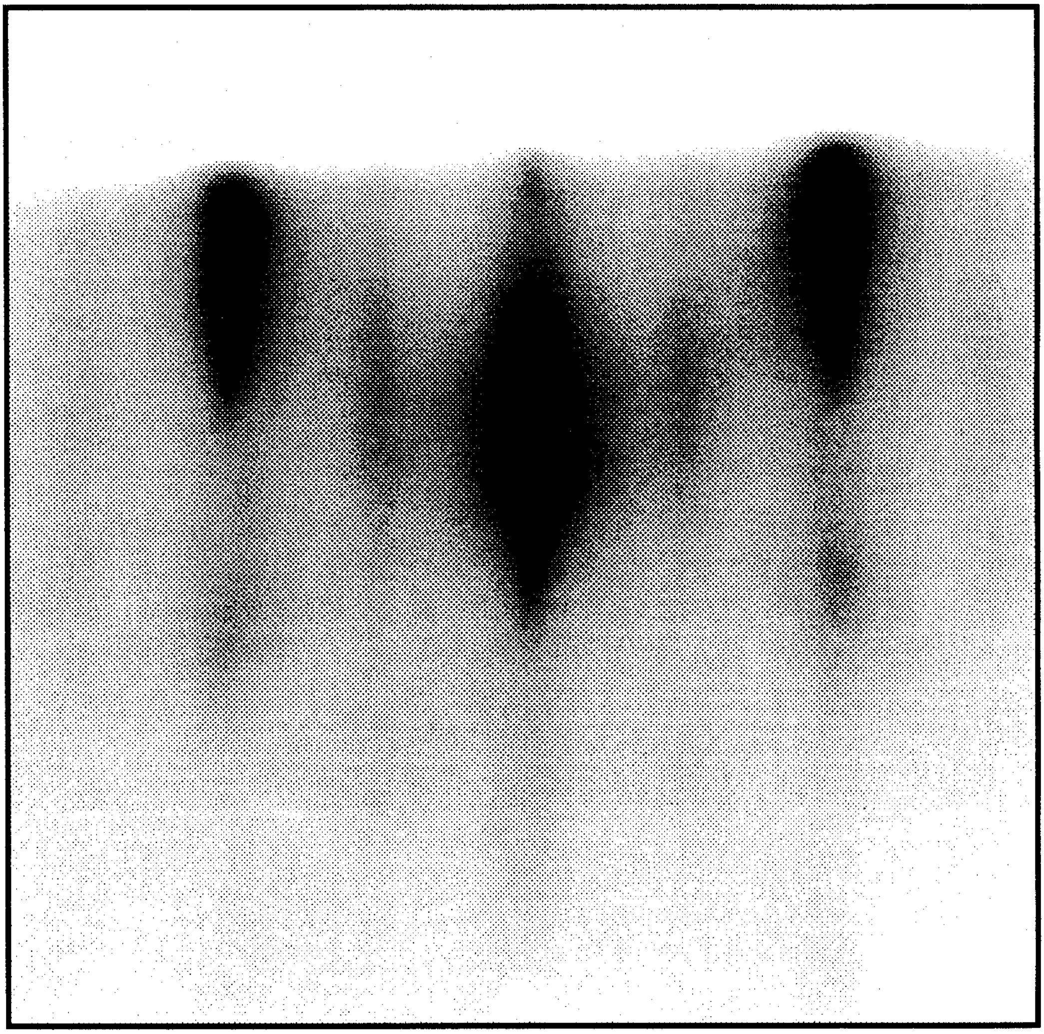

Figure 5.7: RHEED pattern from Sample A immediately after growth of 200 Å $Si_{0.80}Ge_{0.20}$ at 230 °C. Growth at low temperature has resulted in a rough surface, producing a spotty pattern.

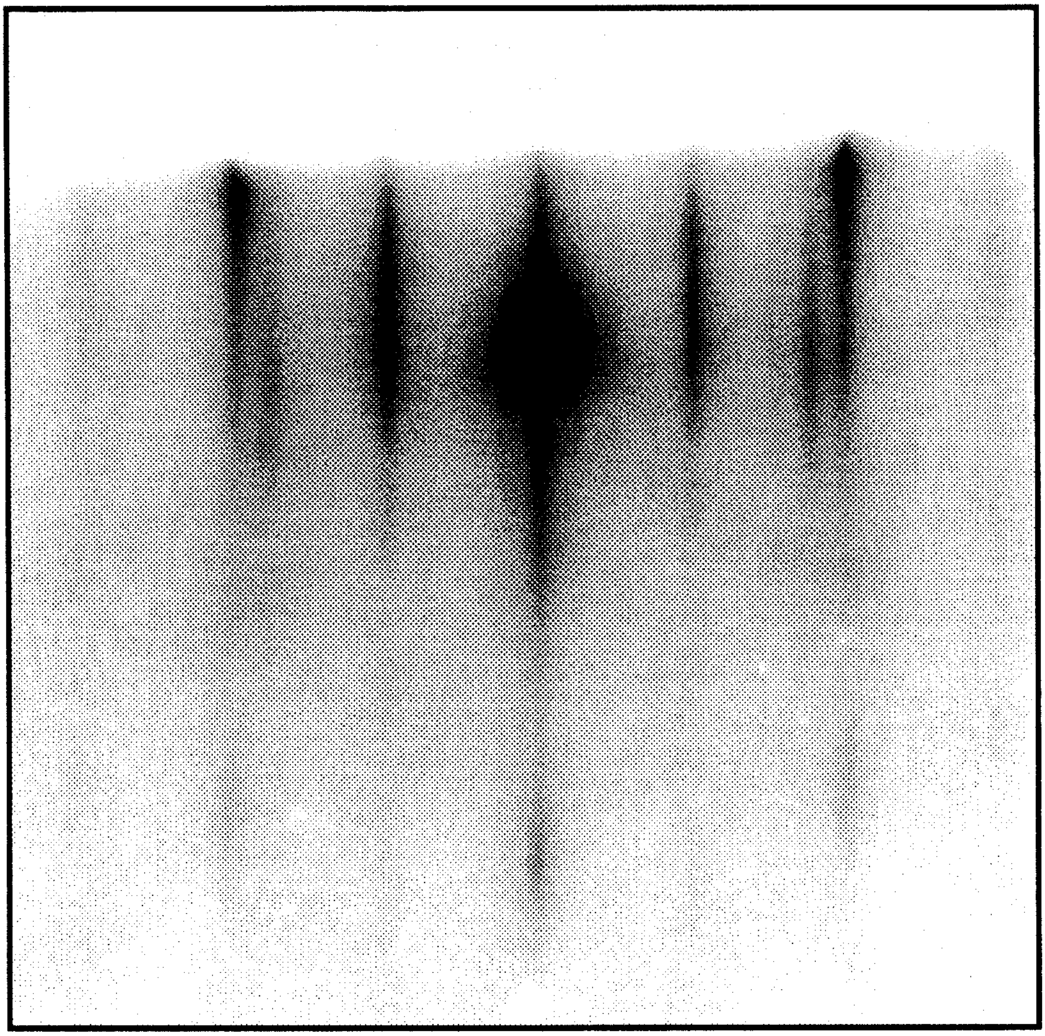

Figure 5.8: RHEED pattern from the same sample as in Fig. 5.7 after a brief anneal to 700 °C. The sharp streaks in the pattern indicate that the sample surface has become smooth. Atoms have rearranged on the surface, reproducing the same ordering phenomena observed with LEED.

the reconstruction, we can conclude that it is thermodynamically stable.

The final three steps in the growth of sample A were intended to determine the dependence of strain on the reconstruction. A 5000 Å $Si_{0.80}Ge_{0.20}$ was grown to place the sample in the relaxed region of the 550 °C empirical, critical thickness curve of People and Bean.[3] Immediately after growth, the sample surface was observed to possess (2×8) symmetry, although its RHEED pattern appeared diffuse. After annealing the sample for three hours at 700 °C and allowing it to return to room temperature, the (2×8) reconstruction reappeared. Similar films have been reported previously[17, 18] to relax $\sim$ 84% of coherent strain; therefore, since the pattern reappeared, we can conclude that bulk strain is not responsible for the reconstruction. It should be pointed out, however, that the pattern after annealing was not as sharp as before but this is probably due to disorder created by the introduction of large numbers of threading dislocations during the relaxation process.

We have also observed the evolution of the RHEED pattern on a (100) Si substrate under a slight Ge flux. First, a sharp (2×1) pattern was obtained through the use of the usual desorption procedure and subsequent Si buffer layer growth. Then, at a temperature of 500 °C, the surface was exposed to a 0.01 Å/s Ge flux. After about 160 s (1 monolayer), the reconstruction changed from (2×1) to (2×8). The ordered reconstruction persisted until a total of approximately 5 monolayers of Ge were deposited. At this point, the reconstruction became faceted, possibly because of the formation of Ge islands. Interestingly enough, a further deposition of Si reversed the process exactly. The faceted pattern reverted to (2×8) and then, after nearly 10 monolayers of Si, became (2×1). It is interesting to note that several monolayers were necessary to cause the reconstructions to change, suggesting that some segregation had taken place during growth. The behavior described above demonstrates that Ge plays a very important role in the formation of the (2×8) reconstruction. Indeed, the reconstruction can be created, and destroyed, simply by changing the surface concentration of Ge.

5.3.4 Kinematical Calculation of Diffraction from an Ordered Linear Chain

We propose the following model for the (2×8) $\mathrm{Si}_{1-x}\mathrm{Ge}_x$ surface reconstruction based on the ordered defect model proposed by Martin *et al.*[5] to explain the origin of $(2 \times n)$ reconstructions observed on (100) Si. In our model, ordering of Ge dimers in a direction perpendicular to the dimerization direction locates them approximately eight atoms apart. Arranging these ordered dimer chains by lining up the Ge dimers in the "2" direction yields the required (2×8) symmetry. Composition can be adjusted as necessary without affecting the symmetry by randomly substituting one type of atom for the other. To evaluate the validity of this model, we have approximated the ordered dimer chain as an ordered linear chain of individual scattering sites. Finally, we have simulated electron diffraction from such a chain through the use of the kinematic approximation.[19]

Each atom in the chain is defined by a position, $\vec{r}_n$, and a form factor, f_n, describing the relative strength of interaction with the incident electron beam. Si atoms are arbitrarily assigned a form factor of 1. Ge atoms, however, receive a value of 2.3 since the form factor is known to vary approximately linearly with atomic number.[19, 20] Also, since the diffracting electrons are coherent over a distance of several hundred Angstroms,[20] we have limited the number of atoms involved in the calculation to 160. The intensities of the diffracted beams are a function of the difference in wave vector between the scattered electrons and the incident electrons. Hence, we define $\vec{k}$ such that

$$\vec{k} = \vec{k}_{out} - \vec{k}_{in}. \tag{5.1}$$

In our model, each scatterer contributes a phase multiplied by its form factor to the overall scattering intensity, $I(\vec{k})$, which can be written

$$I(\vec{k}) = |\sum_n f_n e^{i\vec{k}\cdot\vec{r}_n}|^2. \qquad (5.2)$$

Using Eq. 5.2, we have calculated $I(\vec{k})$ for an ordered, linear chain to study the effect of strain on the relative intensities of the fractional-order peaks.

In the unstrained case, each scatterer is located exactly 1 unit apart. The calculated diffraction pattern appears in Fig. 5.9. Intensity has been normalized so that at $\vec{k} = 0$, it takes on a value of 1. It should be pointed out that each fractional-order peak is exactly the same intensity. The strained case is shown in Fig. 5.10. Here, the Si-Si bond length has been decreased, while the Si-Ge bond length has been increased. The eight-atom, unit-cell length, of course, was preserved. In the figure, notice that the intensity of the $\frac{7}{8}$-order peak has increased relative to the $\frac{9}{8}$-order peak. This is consistent with our experimental results. In the unphysical case where the Si-Ge bond length is made to be *shorter* than the Si-Si bond length, the intensity of the $\frac{7}{8}$-order peak increases relative to the $\frac{9}{8}$-order peak. These results support our contention that Ge dimers are ordering along the direction of the dimer chains of a (2×1) reconstruction.

5.4 Chapter Summary

In conclusion, we have observed a (2×8) surface reconstruction on surfaces of $Si_{1-x}Ge_x$ alloys grown on (100) Si for compositions, x, between approximately 0.10 and 0.30. Outside this compositional range, RHEED and LEED patterns exhibit a (2×1) Si-like reconstruction. We have also investigated the thermal stability of the reconstruction and found it to persist even after a high-temperature anneal, suggesting that it is thermodynamically stable. Bulk strain apparently

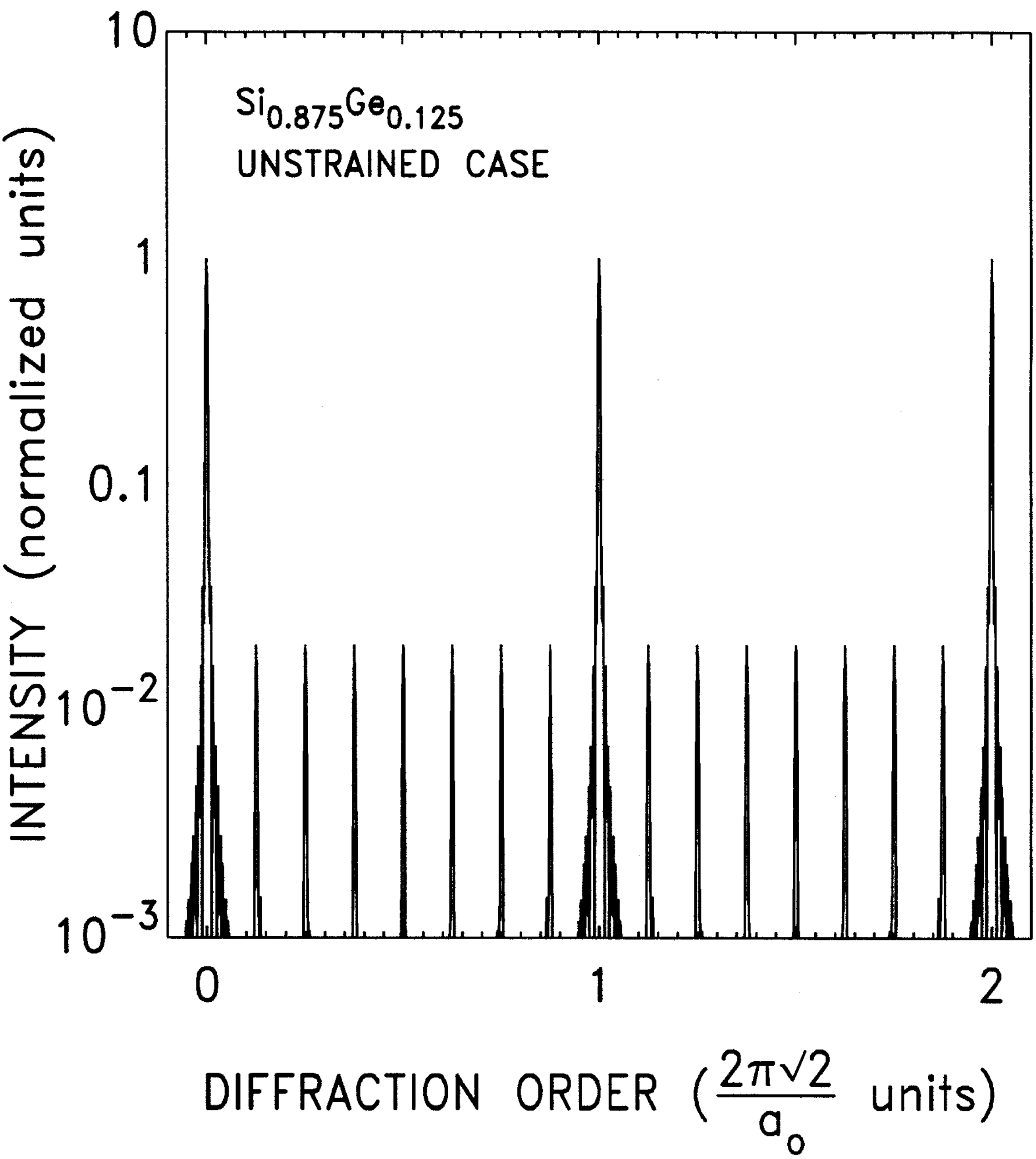

Figure 5.9: Simulated diffraction pattern from an ordered chain of Si and Ge atomic scatterers in which Ge atoms are located every eight atomic positions. Visible in the figure are fractional-order diffraction peaks of equal intensity.

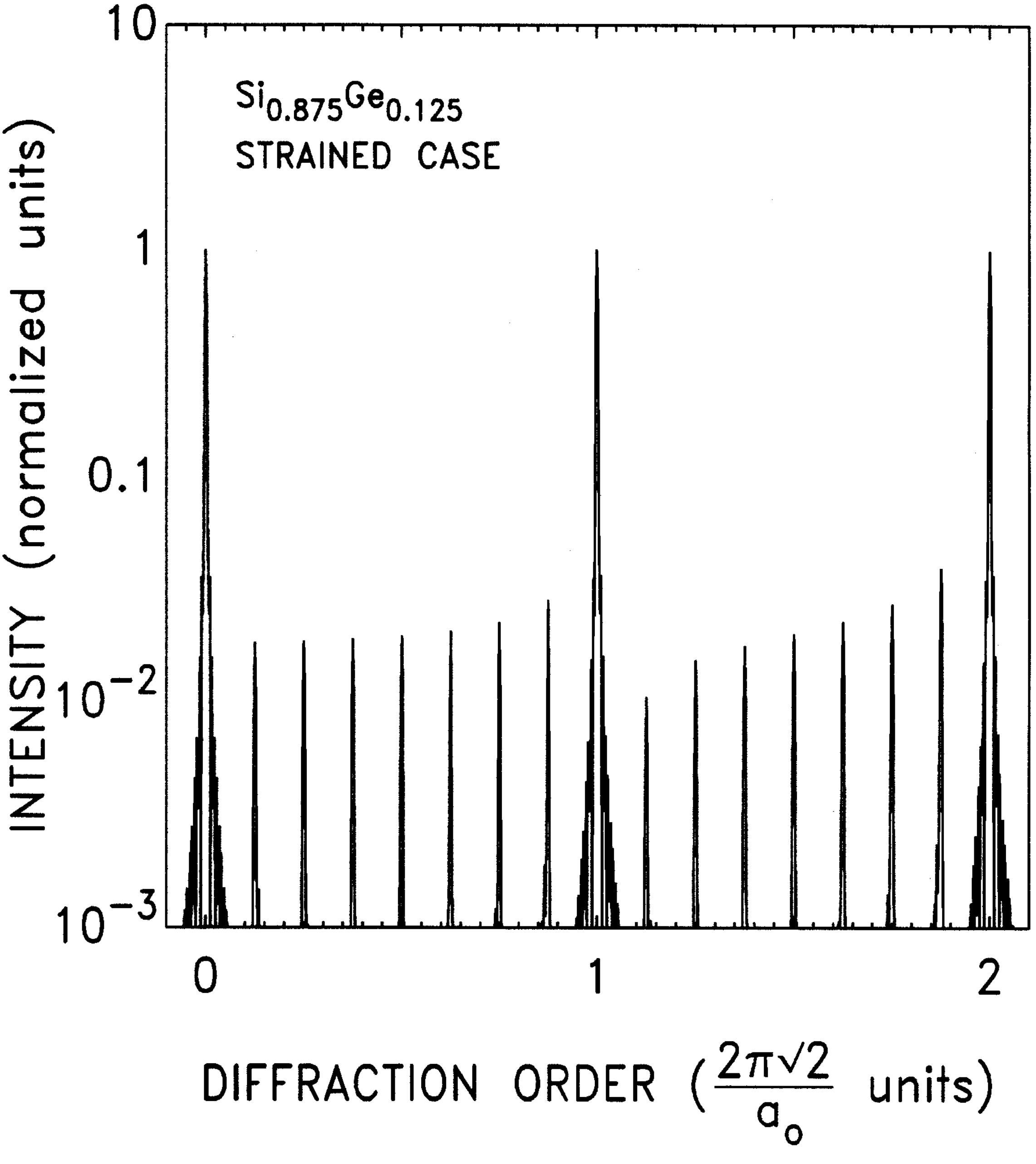

Figure 5.10: Diffraction from a similar chain of atoms in which Si-Ge bond lengths were chosen to be slightly larger than Si-Si bond lengths. The increase in $\frac{7}{8}$-order peak intensity relative to $\frac{9}{8}$-order intensity is consistent with RHEED and LEED observations.

is not responsible for the formation of the (2 × 8) phase, since an intentionally relaxed sample also exhibited the reconstruction. Furthermore, our results demonstrate that simply changing the surface concentration of Ge influences the type of reconstruction present. These results lead us to conclude that Ge is ordering on the surface. We suspect that the Ge atoms are arranging themselves in dimers that order in a direction perpendicular to the dimerization direction. A repulsive force that is due to local lattice strains between Ge dimers may be responsible for the observed ordering phenomenon. This conclusion is similar to the model proposed by Aruga and Murata[9] to explain the mechanism of missing-dimer defect ordering on (100) Si. Finally, results from our simulation are consistent with this model since the intensity of the $\frac{7}{8}$-order peak increases relative to that of the $\frac{9}{8}$-order peak for atomic chains, including strain effects.

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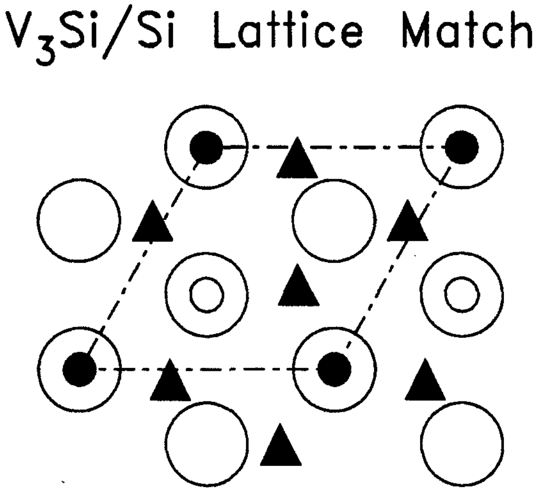
Chapter 6

Growth of Superconducting V_3Si on Si

6.1 Introduction

6.1.1 Introduction to Chapter

Materials that crystallize in the $A15$ structure have long been of interest for their superconducting properties. One of these $A15$ materials, V_3Si, has been shown to exhibit a close geometrical lattice match to (111)-Si.[1] The lattice match between V_3Si and Si is shown in Fig. 6.1. There we see that the (1×1) surface unit cell of (111)-V_3Si coincides in size almost exactly ($< 0.4\%$) with a $(\sqrt{3} \times \sqrt{3})R\,30^\circ$ surface cell of (111)-Si.[2] The nature of the chemical bonds at such an interface appears favorable to epitaxy, although a significant amount of reconstruction may be necessary. As a result, the question of whether or not V_3Si can be grown epitaxially on Si is important from both a physical and a technological point of view. This lattice match, along with the recent advances in Si molecular beam epitaxy (MBE), which have made possible the fabrication of



Symbol	Atomic Layer	Layer #
◯	(111)-Si : Si	0
●	(111)-V_3Si : Si	1
▲	(111)-V_3Si : V	2
○	(111)-V_3Si : Si	3

Figure 6.1: Illustration of the lattice match between (111)-V_3Si and (111)-Si structures. For clarity, only one atomic layer of the Si and three of the V_3Si are shown. The fundamental surface unit cell of V_3Si is almost exactly the same size as the $(\sqrt{3} \times \sqrt{3})R30^\circ$ surface cell on (111)-Si. However, since only 1/3 of the Si atoms lie under the Si atoms in V_3Si (corners of the rhombus), there are three translationally equivalent lattice matches, and for each of these, a pair of 180° rotation twins, making a total of six possible epitaxial matches of V_3Si to a given (111)-Si surface.

epitaxial, single-crystal metal[3] ($NiSi_2$ and $CoSi_2$) and insulating[4] (CaF_2) films on Si, invites the possibility of growth of multilayered, device structures based on various combinations of epitaxial superconductors, semiconductors, normal metals, and insulators, on Si.

Recently, much excitement has been generated in the scientific community because of the discovery of materials that exhibit high superconducting transition temperatures. It is now well known that these materials possess a highly layered structure resembling, to a certain extent, a superconductor/insulator superlattice. Our work with the V_3Si/Si system[5, 6] has been motivated by the possibility of fabricating such a structure, and perhaps, gaining control over the structural considerations governing T_c in the new superconductors. In addition, superconductor/semiconductor epitaxial structures may be of considerable interest in novel electronic-device applications.

Unfortunately, it has been previously impossible to stabilize growth of V_3Si films directly on crystalline Si. Studies have shown that the thermodynamics[7]-[10] and (in some cases) kinetics[8] instead favor the formation of the most Si-rich vanadium silicide phase, VSi_2, on a crystalline Si substrate. In particular, the V-Si phase diagram contains several V_xSi_y compounds, none of which exhibits superconductivity except V_3Si, the most V-rich (and in the presence of excess Si the least stable) phase.[11] This previous work was based on solid-phase reaction (SPR) of thin V films with Si substrates[7, 10] and also on SPR of sequentially deposited Si-V diffusion couples onto SiO_2 or Al_2O_3 substrates.[8, 9]

In this chapter, we report the first successful fabrication of superconducting V_3Si films directly on a crystalline Si substrate. Our V_3Si films were fabricated by molecular beam codeposition of V and Si (3:1 flux ratio) in an ultrahigh-vacuum (UHV) chamber. Simultaneous growth on Si and Al_2O_3 substrates at temperatures in excess of 550 °C result in nonsuperconducting films on Si, while the corresponding films on Al_2O_3 exhibit superconductivity with T_c approaching the bulk value for V_3Si (16.6 – 17.1 K[12]). Further analysis of the growth-temperature dependence of T_c for depositions on Si indicate the presence of a plateau region of superconductivity between 350 and 550 °C. Auger compositional profiling and transmission electron microscopy (TEM) have been used to characterize the quality of the films and to identify the superconducting material. Studies of the dependence of T_c on Si concentration, x, reveal that a maximum occurs near $x = 0.25$. In addition, for high x, films prepared on Si are nonsuperconducting, and for low x, T_c approaches the bulk value for pure V (5.4 K). In addition, decreasing the growth rate is shown to result in improved film quality and the highest T_c observed for a 500 Å V_3Si film on Si (13.5 K). While all the films studied here proved to be polycrystalline, we believe that this work takes the first step toward achieving an epitaxial superconductor on Si.

6.1.2 Potential Device Applications

Most useful applications of superconducting materials in electronic devices take advantage of a remarkable property studied in the early 1960's by B. D. Josephson.[13] Josephson considered the problem of electron-pair tunnelling through a thin (< 10 Å) insulating layer between two superconductors (see Fig. 6.2). As a direct result of the quantum-mechanical nature of superconductivity, electron transport through such a structure (now known as a Josephson junction) can be made to exhibit counter-intuitive behavior. Although a thorough treatment of the so-called Josephson Effect is beyond the scope of this thesis, the main result will be presented here.

Following Feynman,[14] the current through a Josephson Junction is described in terms of the phase difference between the electron wave functions in the two

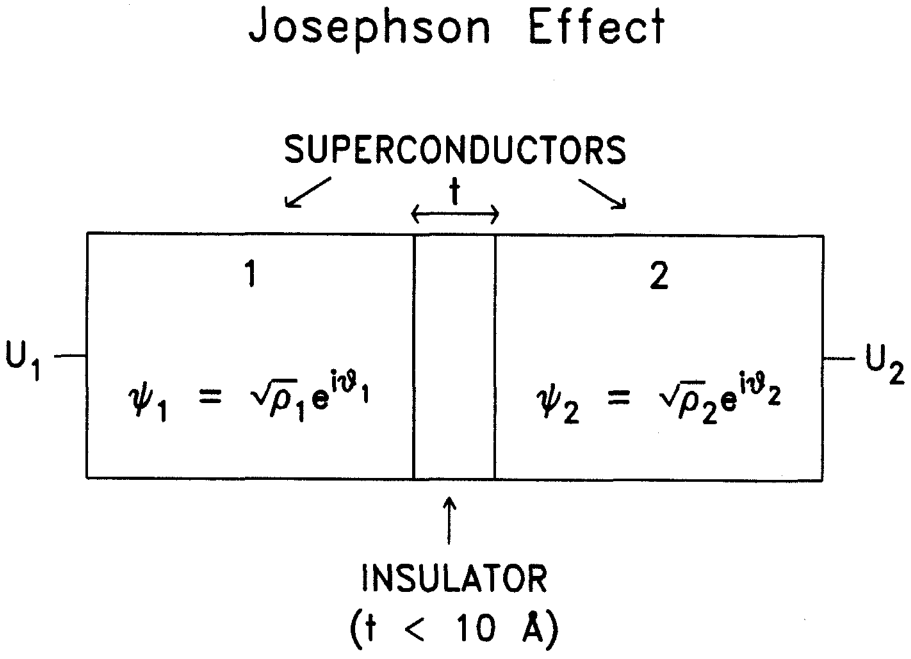


Figure 6.2: Situation studied by B. D. Josephson[13] in 1962. Two superconductors are separated by a thin (< 10 Å) insulating layer. Quasi-particle tunnelling through the insulator produces a coupling between the two sides of the junction. Many modern, superconducting, electronic devices are based on the resulting behavior.

superconductors, $\delta \equiv \theta_2 - \theta_1$. The phase difference, in turn, arises from the vector potential, $\vec{A}$, and the expression for the total current through the device is just

$$J = J_0 \sin\delta = J_0 \sin\left(\delta_0 + \frac{2q_e}{\hbar}\int \vec{A}\cdot d\vec{s}\right), \tag{6.1}$$

where the integral is taken across the junction. The quantity $2q_e$ appears in this equation, since we are considering tunnelling of pairs of electrons.

Armed with this result, consider what happens when two Josephson junctions are combined in parallel. The phase difference between the two parallel flowing currents in such a circuit is calculated, using Eq. 6.1. The change in phase of the current flowing through junction 1 is given by taking the integral in Eq. 6.1 over a path through that junction. Similarly, integration over a path through junction 2 yields the change in phase through that junction. Subtracting the change in phase through junction 2 from that of junction 1 yields the phase difference between the two paths:

$$\delta_2 - \delta_1 = \frac{2q_e}{\hbar}\underbrace{\oint_{loop} \vec{A}\cdot d\vec{s}}_{\Phi}. \tag{6.2}$$

But the integral in Eq. 6.2 is just the magnetic flux, Φ, through the loop formed by the two junctions. Summing the contribution to the total current, J, from each junction yields

$$J = J_1 + J_2 = J_0 \sin\delta_0 \cos\frac{q_e\Phi}{\hbar}, \tag{6.3}$$

which is a maximum whenever the flux through the loop is an integral multiple of $\frac{\pi\hbar}{q_e}$. If the area of the loop is $1\,\mathrm{mm}^2$, each maximum in the total current is separated by as little as 2.1×10^{-5} gauss! Devices exploiting this interference phenomenon have been studied extensively in recent years and are now used as sensitive detectors of magnetic field. They are most often referred to as superconducting quantum-interference devices (SQUIDs). An excellent report on some recent attempts to fabricate reliable, high-performance, Josephson tunnel junctions is given in Ref. [15].

In addition to SQUIDs, several other applications for superconductor devices have been proposed. Examples include a variety of three-terminal devices based on nonequilibrium superconductivity such as the Gray-effect transistor (GET[16]) and QUITERON.[17] Other devices[18, 19] replace the base of a conventional bipolar transistor with superconducting material, resulting in a device that is limited in performance by the transit time of quasi-particles (electrons and holes) through the superconducting base layer. Unfortunately, the fabrication of these devices has been hampered by the inability to find a suitable material system. Clearly, an epitaxial superconducting material on Si would be an excellent combination.

6.1.3 Outline of Chapter

So far, we have presented background information and motivation for choosing the V_3Si/Si materials system for this study. The remainder of the chapter focuses on the experimental details and results of this work. In Section 6.2, the growth procedures used to fabricate the samples is discussed. In particular, we summarize the growth process from sample preparation through V_3Si growth and describe the purpose of each sample in the sample set. In Section 6.3, the results of this work are presented. In particular, we have investigated the dependence of T_c on growth temperature, studied the reaction between the V_3Si and the Si substrate with Auger compositional depth-profiling and TEM, and describe the effects of composition and growth rate on the microstructure of our superconducting V_3Si films. Finally, the last section of the chapter concludes with a brief summary of the work and suggests ideas for follow-up experiments.

6.2 Sample Preparation

The samples prepared for this study were codeposited from a Thermionics, dual *e*-beam source in a custom-built UHV chamber with a base pressure $< 8 \times 10^{-11}$Torr and typical growth pressures of approximately 5×10^{-9}Torr. The growth system has been adequately described in Section 1.2.1. Two Inficon (model XTC) controllers were independently used to maintain closed-loop control over the V- and Si-deposition rates. Rates were calibrated using a Tencor Instruments alpha-step 200 stylus profiler. Nominally, 1000 Å V or Si were deposited on Al_2O_3 substrates, and the thicknesses were measured at four different spots on the wafer. The spread in the measurements indicated an uncertainty of about 5 percent in the final thicknesses. The deposition-rate ratio, r_V/r_{Si}, was calculated from the expression

$$\frac{r_V}{r_{Si}} = \frac{1-x}{x} \frac{\rho_{Si} M_V}{\rho_V M_{Si}}, \tag{6.4}$$

where x is the molar fraction in $V_{1-x}Si_x$, ρ_{Si} and ρ_V are the densities, and M_{Si} and M_V are the molecular weights of Si and V, respectively. For $x = 0.25$ (the Si concentration appropriate for V_3Si growth), the ratio, $r_V/r_{Si} = 2.07$, was calculated from Eq. 6.4. This ratio changed, of course, when we varied the Si concentration in the depositing film. In practice, accurate rate control over a few Angstroms was difficult to achieve, especially at low deposition rates, since instantaneous rate fluctuations in the e-beam process could be as large as 0.3 Å/ s; however, at the growth temperatures used in this study, the atoms have sufficient thermal energy to blur the effect of these fluctuations. As a result, we have chosen to calculate our compositions using the final thicknesses of the constituents in Eq. 6.4 instead of the rates. Propagating through the uncertainty in the thicknesses, the calculation results in an uncertainty in average Si concentration of about 1%.

Depositions were made onto heated (111) Si and $(1\bar{1}02)$ Al_2O_3 substrates which had been first degreased in trichloroethylene, acetone, methanol, and then rinsed in de-ionized water. After this degreasing procedure, the Si substrates were etched in a 50% HF solution to remove SiO_2, rinsed once again in de-ionized water, and immediately loaded into the UHV chamber. Samples prepared for the study of growth temperature versus T_c were outgassed *in situ* at approximately 800 °C. Growth temperatures were calibrated through observation of Au/Si and Al/Si eutectic reactions *in situ*, and correlated to heater power levels, assuming a T^4 dependence. At the eutectic points, calibration is exact, assuming that the eutectic reactions occurred at the correct temperatures (363 °C for Au/Si and 577 °C for Ai/Si). We estimate our substrate temperature calibration to be accurate within ±25 °C. Other factors are also present that may affect actual substrate temperature. For instance, thermal drift that is due to heating of the substrate heater itself could cause the wafer temperature to change during deposition. We have attempted to address these factors by carefully reproducing heater power levels and temperature-ramping times from run to run.

Once we determined that we could consistently grow superconducting V_3Si on Si, we discontinued use of the Al_2O_3 substrates. Prior to growth of the samples used in the study of growth rate versus T_c, the substrates were heated to approximately 860 °C and were exposed to a 0.1 Å/s Si flux for 2 min.[20, 21] Subsequently, a 200 Å Si buffer layer was grown at 760 °C. Changes in substrate cleaning procedure were intended to improve the Si starting surface, with the objective of obtaining an atomically clean surface. Low-energy electron diffraction (LEED) from (111) Si substrates prepared in this way show sharp (7×7) patterns indicative of a clean surface.[22]

The sample set described in this study is presented in Table 6.1. In the table, we have indicated the substrate type, thickness of the $V_{1-x}Si_x$ layer, h, deposition rate, r, composition, x, growth temperature, T_g, and superconducting transition temperature, T_c. Samples 1-9 were grown for the purpose of determining the dependence of growth temperature on transition temperature. Samples 5 and 10-13 were grown to study the effect of Si composition, x, on T_c. Finally, preliminary results from four samples (5, 14, 15, and 16) suggest that T_c increases with increasing film thickness and decreasing growth rate.

6.3 Results and Discussion

6.3.1 Dependence of T_c on Growth Temperature

Our films were codeposited on Si and Al_2O_3 substrates at temperatures between room temperature and approximately 600 °C. Films grown on Si at temperatures in excess of 550 °C have a cloudy appearance and show no evidence of superconductivity. Growths on Si at lower temperatures have surfaces that appear mirror-smooth and have superconducting transition temperatures closer to 10 K. Fig. 6.3 shows the ρ vs. T profile for a 1000 Å V_3Si film grown at 400 °C (sample 14). The data indicate that the sample undergoes a superconducting transition at $T_c = 12.5\,\mathrm{K}$ with a transition width of about 0.2 K.

To determine the dependence of growth temperature on T_c, growth rates and final thicknesses were chosen to result in a 500 Å V_3Si film at a rate of about 2.6 Å/s. Fig. 6.4 shows the dependence of T_c on T_g observed in this study. Samples prepared at temperatures in excess of 550 °C are nonsuperconducting on Si and have T_c approaching the bulk value for V_3Si (16.6 – 17.1 K) on Al_2O_3 substrates. (Presumably we might obtain a higher T_c on Al_2O_3 if we chose to investigate growth at higher temperatures. Higher growth temperature would give the depositing atoms more energy and freedom to nucleate larger grains.

Sample[a]	Substrate(s)	h (Å)	r (Å/s)	x (%Si)	T_g (°C)	T_c (K)
1(a)	(111) Si	5000	2.6	0.25	25	···
1(b)	(1$\bar{1}$02) Al_2O_3	5000	2.6	0.25	25	···
2	(111) Si	500	2.6	0.25	305	···
3	”	500	2.6	0.25	350	8.4
4	”	500	2.6	0.25	380	9.8
5	”	500	2.6	0.25	400	9.8
6(a)	(111) Si	500	2.6	0.25	500	9.6
6(b)	(1$\bar{1}$02) Al_2O_3	500	2.6	0.25	500	10.6
7(a)	(111) Si	500	2.6	0.25	530	9.9
7(b)	(1$\bar{1}$02) Al_2O_3	500	2.6	0.25	530	9.8
8(a)	(111) Si	500	2.6	0.25	565	···
8(b)	(1$\bar{1}$02) Al_2O_3	500	2.6	0.25	565	13.1
9(a)	(111) Si	525	2.6	0.25	640	···
9(b)	(1$\bar{1}$02) Al_2O_3	525	2.6	0.25	640	14.6
10	(111) Si	500	2.6	0.20	400	5.4
11	”	500	2.6	0.22	400	7.0
12	”	500	2.6	0.27	400	11.1
13	”	500	2.6	0.30	400	···
14	”	1000	5.2	0.25	400	12.5
15	”	500	1.3	0.25	400	12.2
16	”	500	0.8	0.25	400	13.5

[a] **Sample pairs denoted by (a) and (b) involve simultaneous deposition onto Si and Al_2O_3 substrates.**

Table 6.1: $V_{1-x}Si_x/Si$ sample characteristics. Samples 1-9 were used in the study of T_c vs. T_g. The dependence of T_c on composition, x, was determined through a study of samples 5 and 10-13, and samples 5, 15, and 16 were used to investigate the effect of deposition rate on T_c.

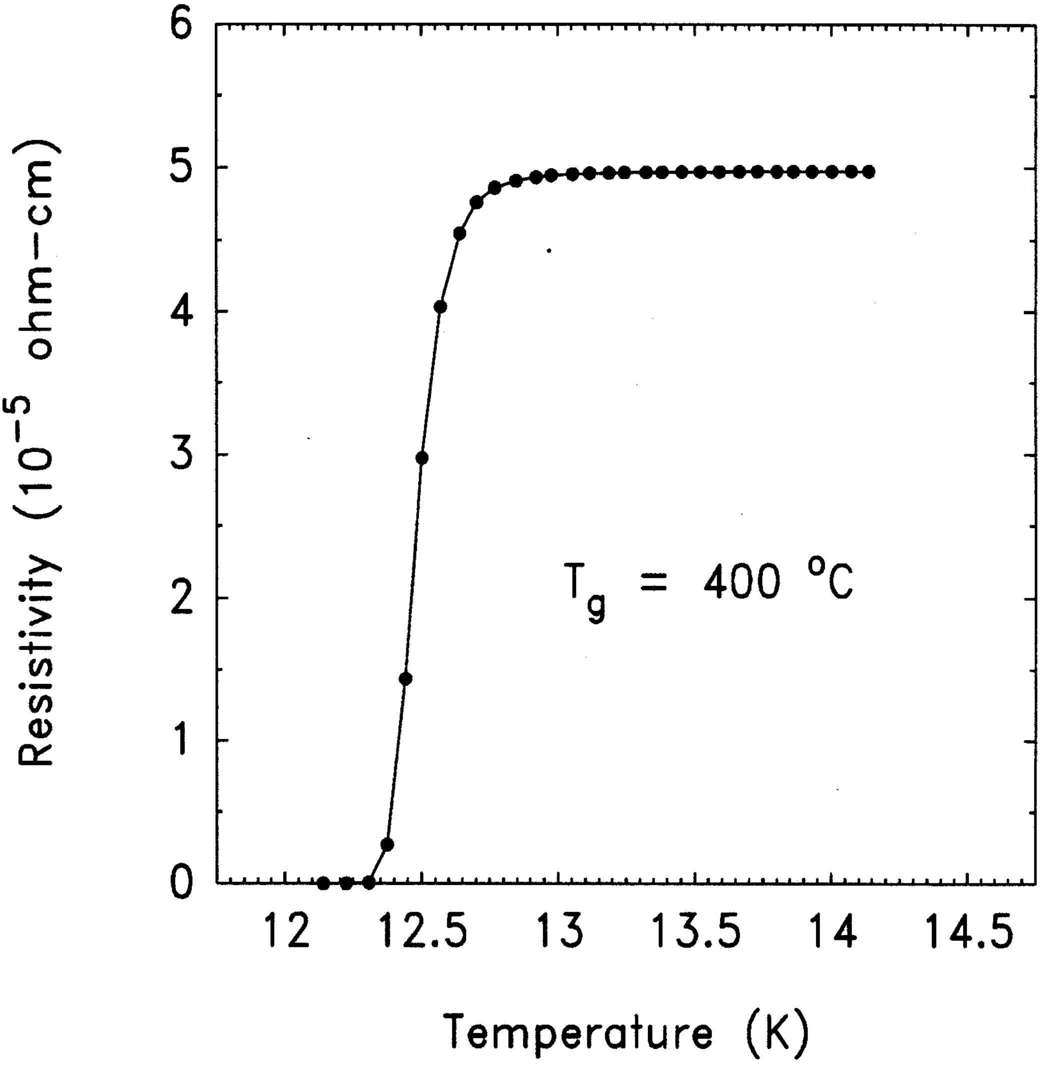


Figure 6.3: Resistivity vs. temperature data for Sample 14. The film shown becomes superconducting at $T_c = 12.5\,\mathrm{K}$, with a transition width (10%–90%) of approximately 0.2 K. Resistivity was measured using the Van der Pauw method and calculated, assuming a film thickness of 1000 Å.

Our purpose here, however, is to study growth on Si.) Films grown on Si do not superconduct unless the growth temperature is between 350 and 550 °C. Room-temperature depositions do not superconduct on either substrate, presumably because the surface migration of the depositing atoms is insufficient to form the $A15$ structure. Therefore, we find a plateau region between 350 and 550 °C, where $A15$ V_3Si can be grown directly on a (111) Si substrate with T_c near 10 K.

6.3.2 Auger Compositional Profiling Results

Seemann-Bohlin x-ray diffraction measurements on two similar, 500 Å-thick superconducting samples, one grown at 400 °C and the other grown at 530 °C (samples 5 and 7(a)), indicate in both cases the presence of a polycrystalline film of $A15$ V_3Si. These samples were selected for further analysis using Auger compositional profiling. Calibration was achieved by defining the surface layer to be accurately V_3Si. The results are presented in Fig. 6.5. In Fig. 6.5(a), the film grown at 400 °C is shown to be composed entirely of V_3Si. The diffuse nature of the interface with the Si substrate is due to instrumental broadening. Fig. 6.5(b) suggests that significant reaction with the substrate has occurred for the sample grown at 530 °C, producing an intermediate layer composed of V and Si in a 1:1 average composition. It is interesting to note that the binary-phase diagram[11] for the V-Si system does not include a "VSi" phase and that although a V_6Si_5 phase does exist, it is not stable below 1160 °C. Hence, the chemical identity of the intermediate layer is unclear at present, though it could conceivably be metastable V_6Si_5.

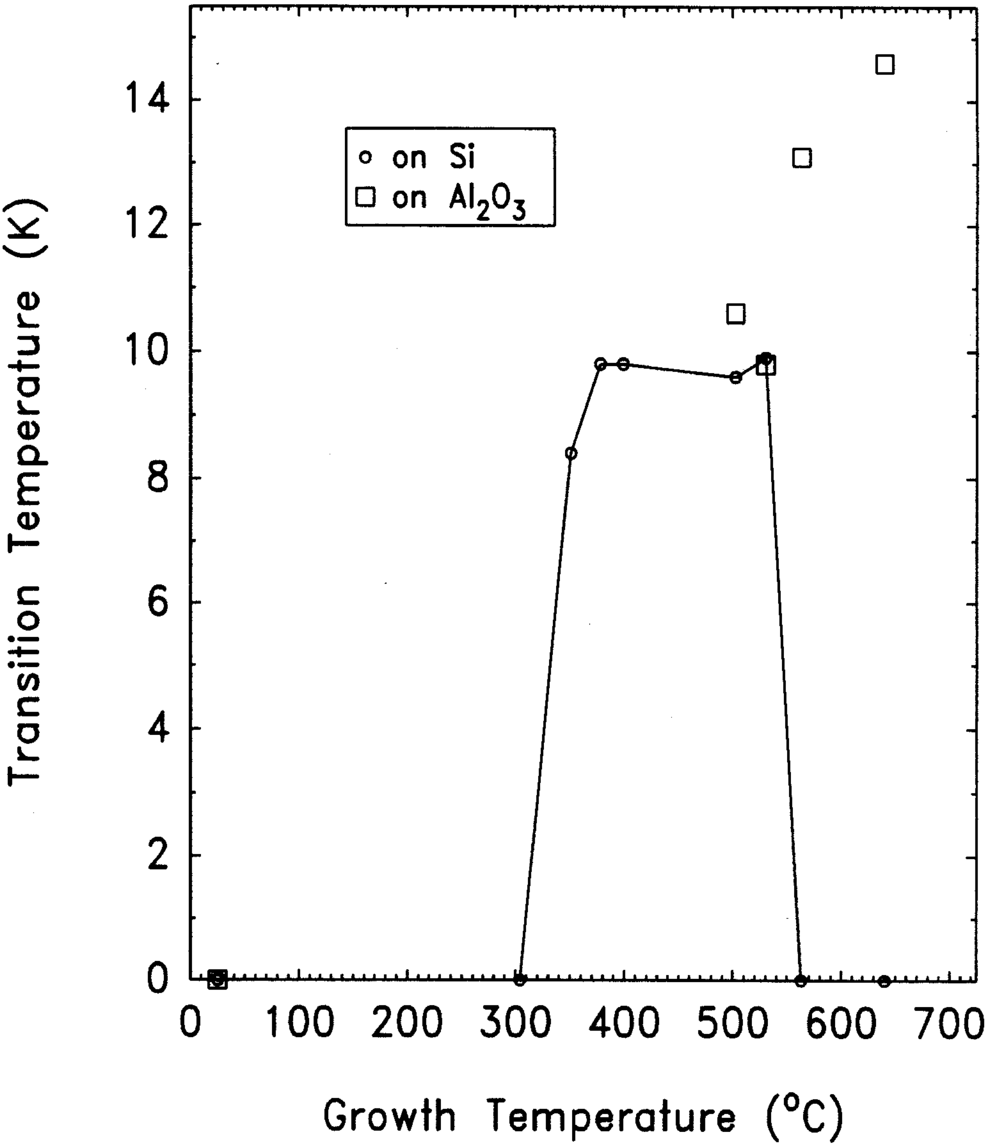


Figure 6.4: Results from T_c measurements on 500 Å $V_{0.75}Si_{0.25}$ films grown on (111) Si and $(1\bar{1}02)$ Al_2O_3 substrates. Samples grown on Al_2O_3 at high temperature have T_c approaching the bulk value for V_3Si (16.6 – 17.1 K). Growths on Si react considerably with the substrate at growth temperatures in excess of 550 °C, yet between 350 and 550 °C, superconducting *A*15 V_3Si is nucleated with a T_c typically near 10 K. Films grown at room temperature do not superconduct on either substrate.

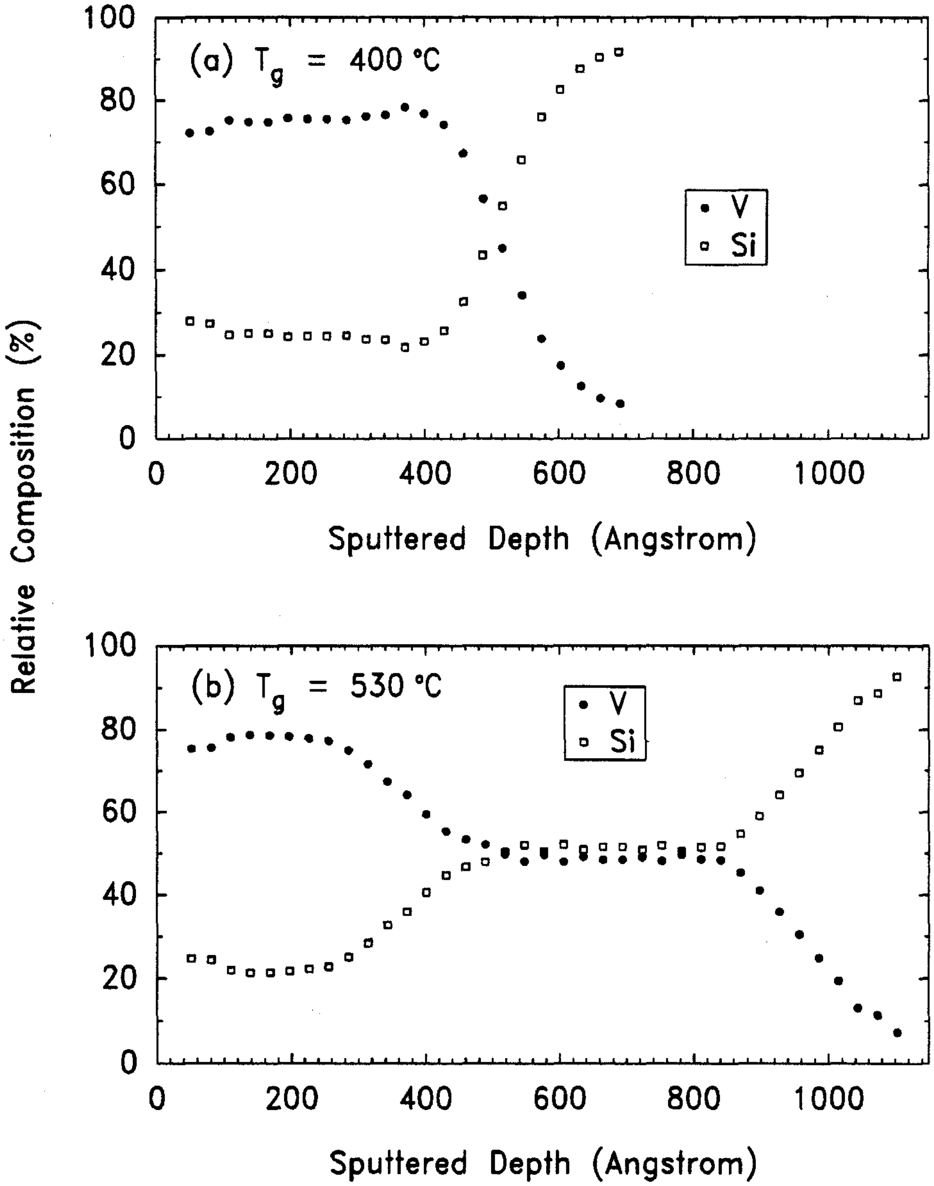


Figure 6.5: Auger compositional profiles from two nominally 500 Å V_3Si samples grown on (111) Si (samples 5 and 7(*a*)). (a) The sample grown at 400 °C has a sharp interface with the Si substrate, indicating that minimal reaction has taken place. The diffuse nature of the interface is due entirely to limitations associated with instrumental resolution. (b) A growth temperature of 530 °C is shown to result in significant reaction with the substrate producing an intermediate layer with a 1:1 V:Si average composition.

6.3.3 TEM Results

Transmission electron diffraction (TED) and plan-view TEM have confirmed the presence of polycrystalline $A15$ V_3Si in our samples. Fig. 6.6 is a plan-view TEM of sample 5. The polycrystalline nature of the surface layer is clearly evident in the image, and the grain diameter is estimated to range from 100 – 200 Å. Further evidence of the presence of polycrystalline V_3Si is presented in Fig. 6.7. This image is the electron diffraction pattern from the sample analyzed for Fig. 6.6, with the electron beam aligned along the (111) zone axis normal to the surface. The rings surrounding the transmitted beam (central spot) have been indexed and are due to V_3Si. Multiple diffraction is responsible for the rings observed around the Si substrate diffraction spots. It is apparent from this pattern that the V_3Si grains are randomly oriented with respect to the substrate.

Cross-sectional TEM was also performed on samples 5 and 7(a), and the results are presented in Figs. 6.8 and 6.9. In Fig. 6.8, the Si buffer layer and the polycrystalline V_3Si overlayer from the sample grown at 400 °C are clearly visible. The buffer layer is indeed epitaxial despite the contrast present in the image. Unfortunately, it appears to contain a higher than desired density of extended defects (spaced by several thousand Angstroms). However, since the V_3Si grain size is only about 100 Å, we can safely assume that buffer-layer quality is not the limiting factor in our attempt to obtain epitaxial V_3Si. In addition, the image shows no evidence of reaction with the substrate, since the interface appears very sharp. The 530 °C sample shown in Fig. 6.9 has obviously reacted with the Si substrate. One can clearly distinguish two polycrystalline layers in this image, thereby corroborating the result presented in Fig. 6.5(b). The crystallites appear columnar in these images, with typical grain diameters between 100 and 200 Å, in agreement with our plan-view image presented in Fig. 6.6. Therefore, we

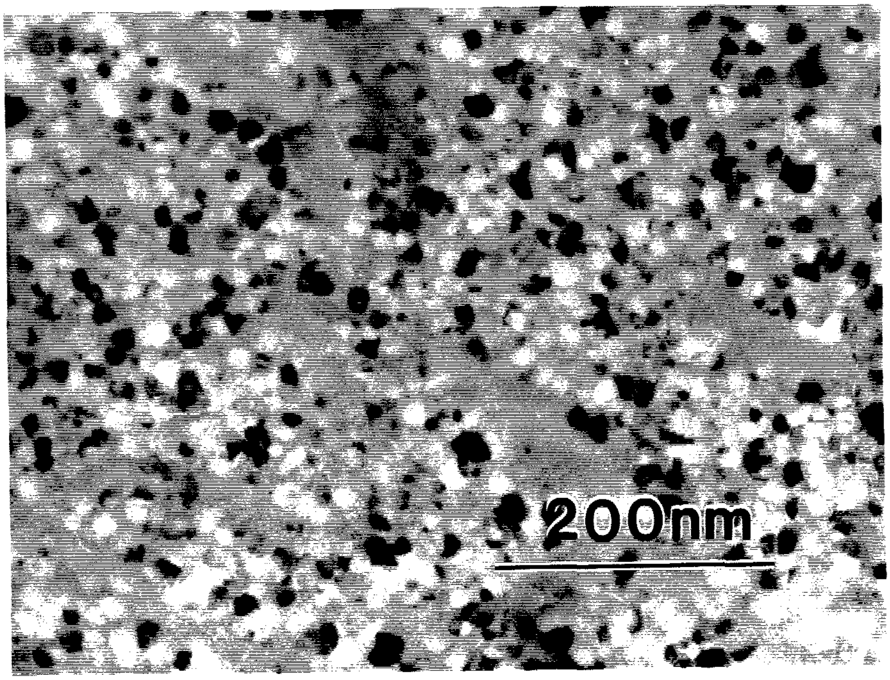


Figure 6.6: Plan-view TEM showing randomly oriented grains from a 500 Å V_3Si film grown on (111) Si at 400 °C (sample 5). The grain size is estimated to range between 100 and 200 Å in the plane of the interface.

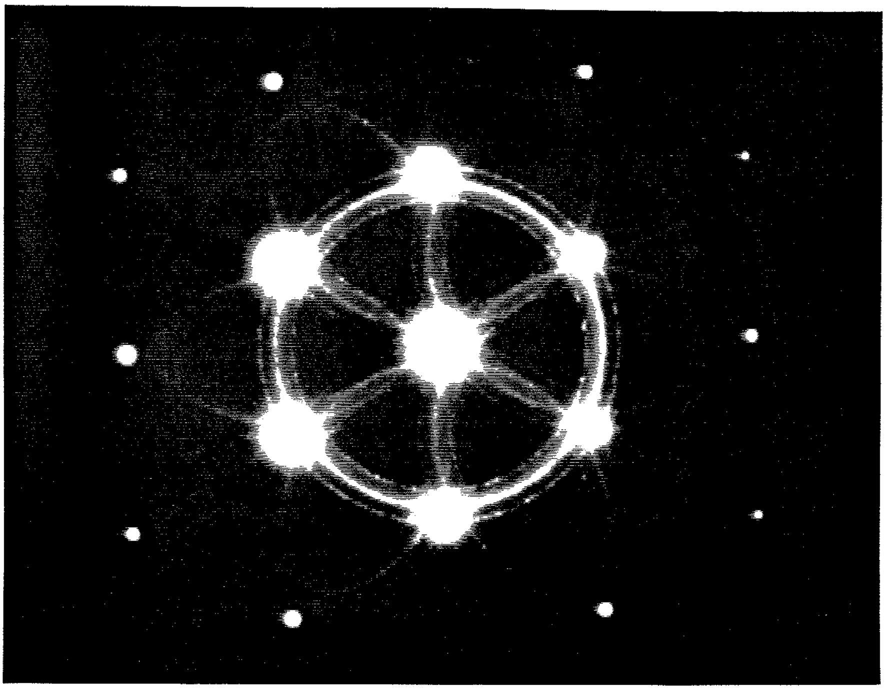


Figure 6.7: Transmission electron diffraction pattern along the (111) zone axis normal to the surface of the sample studied in Fig. 6.6. Rings surrounding the transmitted beam (central spot) were indexed and are due to polycrystalline *A*15 V_3Si. Rings surrounding diffraction spots that are due to the substrate result from multiple scattering from the film and the substrate.

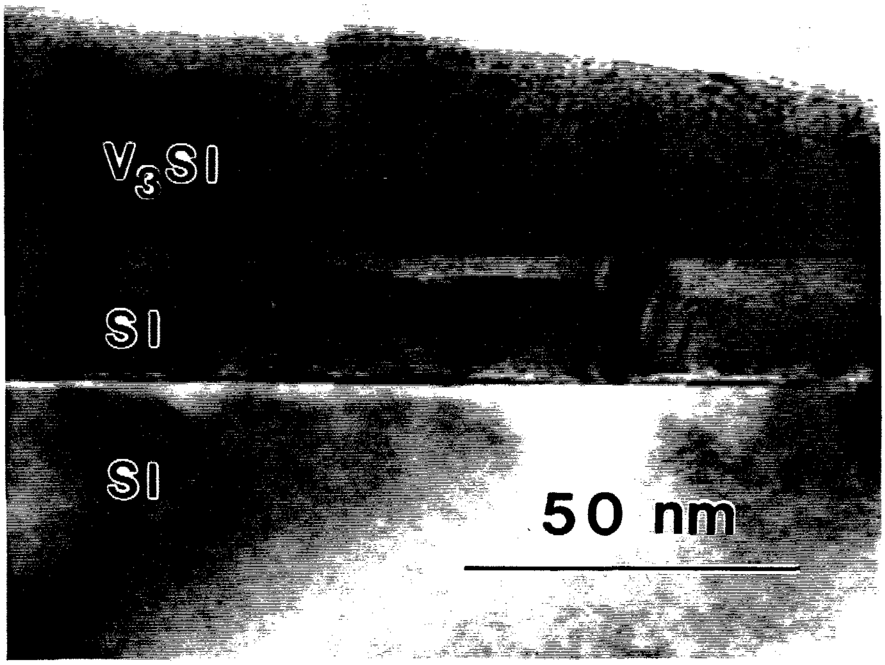


Figure 6.8: Cross-sectional TEM performed on the sample presented in Figs. 6.5(a), 6.6, and 6.7. A crystalline Si buffer layer and a polycrystalline V_3Si overlayer is shown to form a sharp interface if the sample is grown at 400 °C.

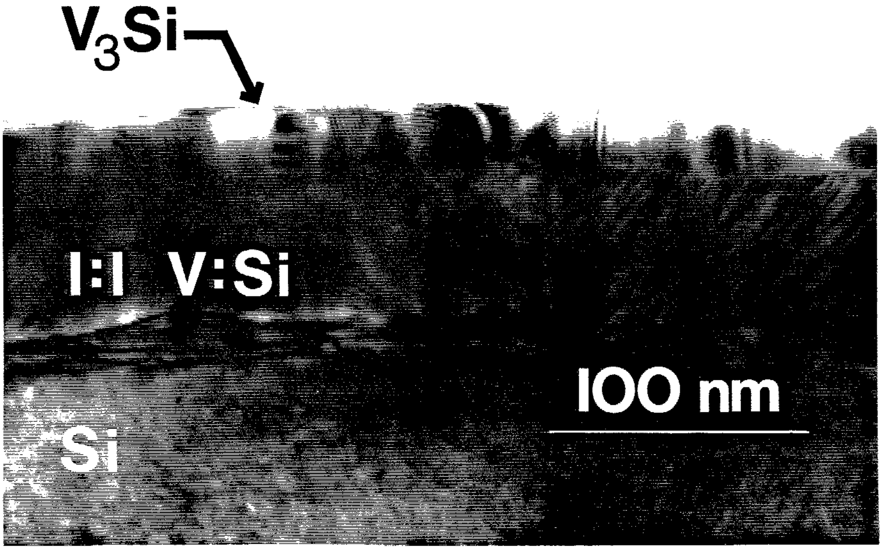


Figure 6.9: Cross-sectional TEM from Sample 7(*a*). At a growth temperature of 530 °C, reaction with the Si substrate has produced a polycrystalline intermediate layer. The grains visible here and in Fig. 6.8 appear to be columnar with typical diameters ranging from 100 – 200 Å.

conclude, by lowering the growth temperature to about 400 °C, a polycrystalline, superconducting V_3Si film can be grown metastably, directly on crystalline Si, with minimal reaction with the substrate.

6.3.4 Dependence of T_c on Other Parameters

Si Composition

During the course of our studies, we have also investigated the effect of film composition on T_c. Depositions were made at our previously determined, optimal growth temperature of 400 °C, and deposition rates were modified to provide a V:Si flux ratio that varied from 4:1 to 7:3 (20% to 30% Si). Fig. 6.10 shows that for high V concentrations, T_c drops to about 5.4 K, the accepted value for pure V, suggesting that pure V has segregated out of the depositing layer. As the Si concentration is increased, we see a maximum in the T_c occurring near $x = 0.25$ as might be expected. For $x \geq 0.30$, samples are typically nonsuperconducting, indicating that a nonsuperconducting $V_{1-x}Si_x$ phase has segregated out of the Si-rich films in the same way that pure V segregated out of the V-rich films. So far, TEM specimens have not been prepared to verify this conclusion. This study has shown that a Si composition of approximately $x = 0.25$ results in the highest-quality superconducting V_3Si material.

Growth Rate and Film Thickness

Several V_3Si samples have been grown at 400 °C (samples 14-16) in an attempt to study the effect of growth rate on T_c. Deposition rates for V_3Si growth were varied between 5.2 and 0.8 Å/s. Unfortunately, strict stoichiometric control was difficult to obtain at low growth rates because of fluctuations. Nevertheless, a comparison of samples 5, 15, and 16, reveals a systematic increase in T_c as the

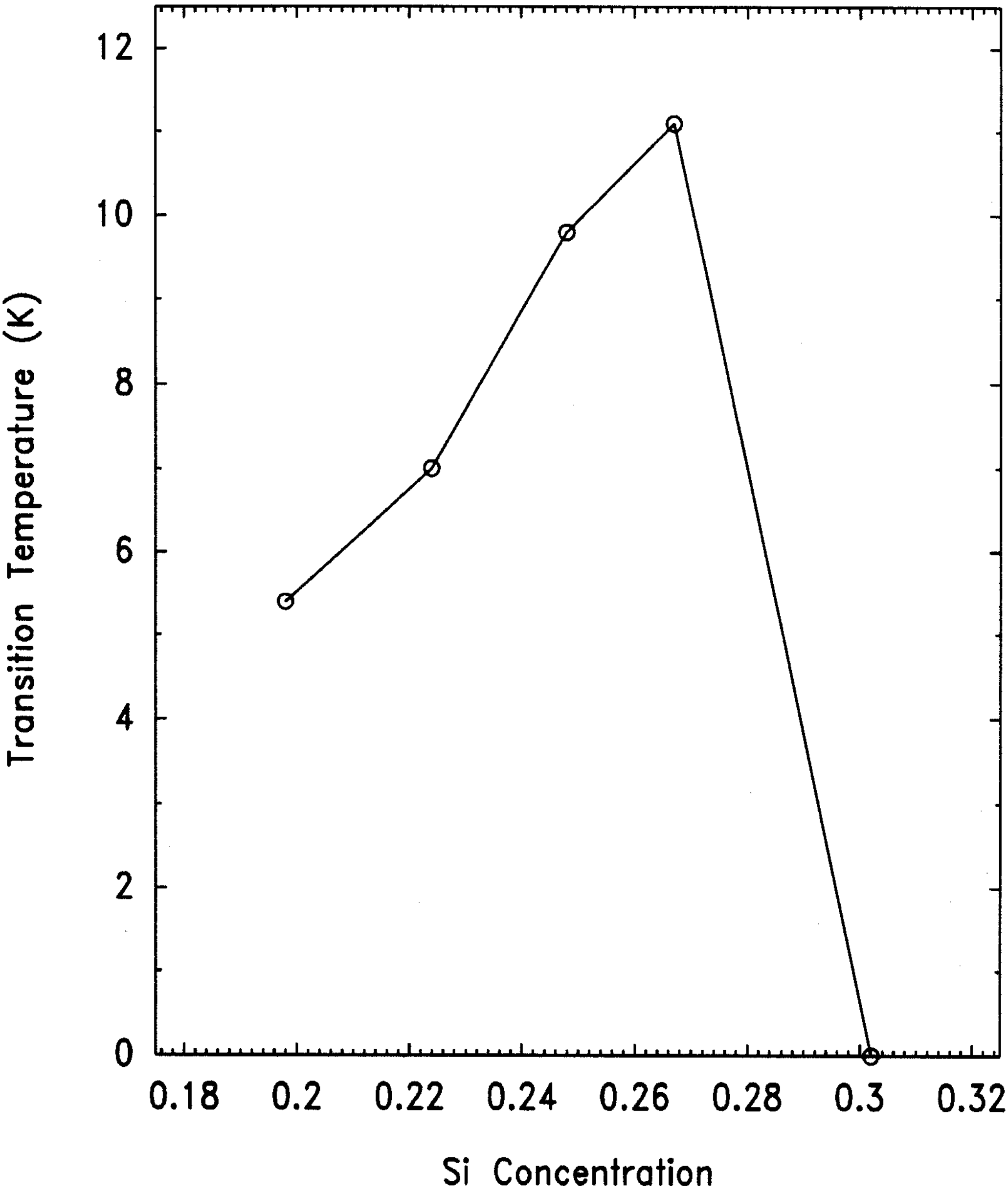


Figure 6.10: Effect of Si concentration, x, on T_c for 500 Å $V_{1-x}Si_x$ films. As x is varied about the value, 0.25, T_c degrades considerably. For V-rich films, V segregates out and the T_c begins to approach the bulk V value (5.4 K). For Si-rich films, nonsuperconducting material segregates out, causing superconductivity to vanish for $x \geq 0.30$.

growth rate is decreased. Possibly, the lower growth rate has allowed nucleation of larger V_3Si grains, resulting in the higher T_c. Our best sample shows a T_c of 13.5 K for a 500 Å V_3Si film grown at 400 °C with a deposition rate of only about 0.8 Å/s. Finally, since T_c for sample 14 was higher than for sample 5, we can conclude that T_c also increases with increasing film thickness.

6.4 Chapter Summary

Through the use of modern, molecular beam epitaxial growth techniques, superconducting V_3Si films have been successfully grown directly on a crystalline Si substrate. A study of the growth parameters governing nucleation of V_3Si on (111) Si has also been conducted. Growth temperature has been shown to affect the nature of the deposited film strongly. A temperature of 400 °C seems to produce the highest-quality V_3Si while minimizing reaction with the Si substrate. Additionally, for Si concentrations different from $x = 0.25$, T_c begins to degrade because of segregation of inferior materials from the $A15$ V_3Si. Lowering the growth rate has been shown to increase T_c, although strict stoichiometric control has been difficult to obtain. Even though we have not yet been able to achieve epitaxy, the results obtained here suggest that the appropriate growth template coupled with the appropriate substrate-surface preparation may result in epitaxial growth of (111)-V_3Si on (111)-Si in the future.

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Chapter 7

Electrical Characterization of p-$\mathrm{Si}_{1-x}\mathrm{Ge}_x/n$-Si Heterojunction Interband Tunnel Diodes

7.1 Introduction

7.1.1 Motivation

The studies presented in previous chapters of this thesis have been motivated by the possible application of the $\mathrm{Si}_{1-x}\mathrm{Ge}_x$/Si and $\mathrm{V}_{1-x}\mathrm{Si}_x$/Si material systems into novel, heteroepitaxial-device structures. Our studies of the $\mathrm{Si}_{1-x}\mathrm{Ge}_x$/Si material system, in particular, suggest that through the use of low-temperature growth techniques, coherently strained structures with abrupt doping profiles can be fabricated to thicknesses considerably in excess of previously established equilibrium[1, 2] and empirical[3] critical thickness curves based upon growth at higher temperatures. In this chapter, we culminate our study of $\mathrm{Si}_{1-x}\mathrm{Ge}_x$/Si heterostructures with an electrical characterization of the first $\mathrm{Si}_{1-x}\mathrm{Ge}_x$/Si heterojunction interband-tunnel (HIT) diodes.

Recent experiments involving molecular beam epitaxy (MBE) of $Si_{1-x}Ge_x/Si$ heteroepitaxial devices have led to the demonstration of negative differential resistance (NDR) in *p*-type, unipolar double-barrier structures based upon resonant tunnelling of holes.[4, 5] In addition, several schemes have been proposed for *n*-type, resonant tunnel structures.[6] Unfortunately, NDR has not yet been observed in the *n*-type structures, possibly because of the relatively small conduction band offset in the $Si_{1-x}Ge_x/Si$ system. Originally proposed by Esaki and co-workers in 1958,[7, 8] the classic, interband-tunnel diode does not suffer from this limitation. The basic structure of the device is a degenerate *p*-*n* junction. Band-to-band quantum mechanical tunnelling of electrons can occur if the degenerate portion of the bands overlap. Since the operation of this device does not depend upon the existence of a band offset, NDR can be observed even in a homoepitaxial device. The operation of these devices will be addressed further in Section 7.2. With the development of techniques for controlling doping and composition, a novel, heteroepitaxial version of the so-called Esaki diode can now be fabricated.

In this chapter, we present preliminary results from the electrical characterization of $Si_{1-x}Ge_x/Si$ heterojunction interband-tunnel (HIT) diodes. In contrast with the Si interband-tunnel diode, we have replaced the *p*-side of the device with a degenerate, *p*-type $Si_{1-x}Ge_x$ alloy layer. At constant doping levels, equilibrium band-bending calculations qualitatively predict an enhancement of NDR with Ge concentration that is due to the valence-band discontiuity present at the *p*-*n* interface. A schematic diagram detailing the structure of the device is shown in Fig. 7.1. In the figure, a *p*-$Si_{1-x}Ge_x$ alloy layer is shown coherently strained to a *p*-type Si substrate. Both the substrate and alloy layers are doped heavily with B ($p \sim 1 \times 10^{20}$ cm^{-3}). Care must be taken so that the alloy layer is grown thicker

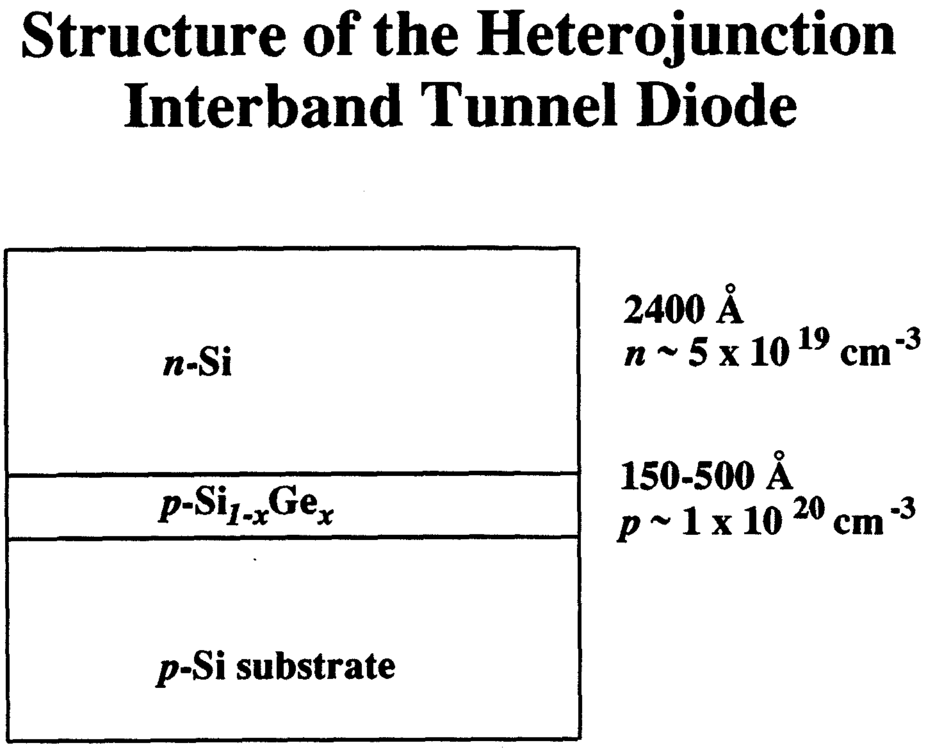

Figure 7.1: Schematic diagram of the $Si_{1-x}Ge_x/Si$ heterojunction interband-tunnel (HIT) diode. A layer of degenerate p-$Si_{1-x}Ge_x$ is grown coherently strained to a p-Si substrate followed by a degenerate n-type Si capping layer.

than the depletion layer and thinner than the critical thickness, in order for the layer to be relatively defect-free. Generally, this limits the composition of the alloy to less than 50% Ge. Following alloy layer growth, a degenerate, n-type Si capping layer, doped to 5×10^{19} cm^{-3} with Sb, is grown on the $Si_{1-x}Ge_x$, forming the n-side of the degenerate p-n junction. Here, we report successful fabrication of $Si_{1-x}Ge_x/Si$ HIT diodes and present an electrical characterization of these devices through the use of I–V measurements and inelastic electron tunnelling spectroscopy (IETS).

7.1.2 Outline of Chapter

In Section 7.2, we introduce concepts pertaining to the basic operating principle of the Si interband-tunnel diode. The physics of this device is discussed and a qualitative picture of the effect of a heterojunction interface is presented. Section 7.3 describes the experimental details of this work, including sample growth and device fabrication. Samples are prepared through the use of low-temperature MBE, and standard photolithographic techniques are used to fabricate the devices. Measurements of current-voltage curves and IETS spectra are presented and discussed in Section 7.4. The principal result is an enhancement of NDR as a function of Ge concentration in the p-$\mathrm{Si}_{1-x}\mathrm{Ge}_x$ layer. In addition, we report previously unobserved peaks in the phonon spectra of our devices and speculate on the possible origin of these features. Finally, our conclusions are summarized in Section 7.5.

7.2 Background

7.2.1 Physics of the Interband-Tunnel Diode

Consider the situation of an interband-tunnel diode consisting of a degenerate p-n junction. The degree of degeneracy (V_n or V_p) is defined by the position of the Fermi level with respect to the band edge. In thermal equilibrium, carriers are exchanged across the junction, creating a depletion layer less than 100 Å in thickness. In general, the total current through the device under bias is a combination of three components. In reverse bias, the total current is dominated by a component that is due to tunnelling. In forward bias and at low voltages, the total current is also dominated by tunnelling. Tunnelling will occur as long as an empty state and a filled state exist at the same energy on opposite sides of the depletion layer. In forward bias, the tunnelling component increases roughly linearly as the degenerate bands begin to overlap, reaches a maximum at $I_{peak} = I(V_{peak})$, and decreases as the bands separate. Once the applied bias exceeds the sum of the Fermi degeneracies $(V_n + V_p)$, the tunnelling component becomes negligible.

Ideally, at this point we would expect that the total current through the device would decrease identically to zero; however, this is not the case. Tunnelling can also occur through states localized in the band gap, producing considerable "excess" current. As a result, the total current will decrease from I_{peak} down to a minimum at $I_{valley} = I(V_{valley})$. At still higher biases, thermal current over the bands becomes important. Empirically, the total current density is described by relation[9]

$$\begin{aligned} J_{total} &= J_{tunnel} + J_{excess} + J_{thermal} \qquad (7.1) \\ &= J_{peak}\left(\frac{V}{V_{peak}}\right)\exp\left(1-\frac{V}{V_{peak}}\right) \\ &\quad + AJ_{valley}\left(V - V_{valley}\right) \\ &\quad + J_0 \exp\left(\frac{qV}{kT}\right). \qquad (7.2) \end{aligned}$$

Following Sze,[10] we consider the tunnelling component to be composed of a contribution from electrons tunnelling from the n-side to the p-side $(I_{n\rightarrow p})$ and a contribution from electrons tunnelling from the p-side to the n-side $(I_{p\rightarrow n})$:

$$\begin{aligned} I_{tunnel} &= I_{n\rightarrow p} - I_{p\rightarrow n} \qquad (7.3) \\ &= A\int_{E_c}^{E_v} F_c(E) n_c(E) P_t \left[1 - F_v(E)\right] n_v(E) dE \end{aligned}$$

$$+A\int_{E_c}^{E_v} F_v(E)n_v(E)P_t\left[1-F_c(E)\right]n_c(E)dE \tag{7.4}$$

$$= A\int_{E_c}^{E_v}\left[F_c(E)-F_v(E)\right]P_t n_c(E)n_v(E)dE. \tag{7.5}$$

In these equations, A is a constant, $F_v(E)$ and $F_c(E)$ are the Fermi filling functions, $n_v(E)$ and $n_c(E)$ are the electron density of states, and P_t is the tunnelling probability. In the Wentzel-Kramers-Brillouin (WKB) approximation,[11] the tunnelling probability is written as

$$P_t = \exp\left[-2\int_0^W |k(x)|\,dx\right], \tag{7.6}$$

where the integral is taken over the depletion layer and k is the wave vector of the tunnelling electron.

Ideally, we would like to calculate the tunnelling current in Eq. 7.5 as a function of voltage, V. To accomplish this, we need to calculate the one-dimensional band profile of the device, then use Eq. 7.6 to compute the tunnelling probability as a function of energy, and evaluate the integral in Eq. 7.5 at each voltage. Unfortunately, a calculation of this complexity is well beyond the scope of this thesis. We shall assume that the tunnelling probability, and hence the tunnelling current, roughly vary as e^{-CW}, where C is a constant. Therefore, qualitatively, we conclude that the tunnelling current should increase as the depletion layer thickness decreases.

7.2.2 Influence of a Heterojunction

Now, we consider the effect of introducing a p-type $\mathrm{Si}_{1-x}\mathrm{Ge}_x$ alloy into the device structure. In Chapter 3, we determined the valence band offset for strained Si on (100) Ge and for strained Ge on (100) Si to be 0.22 and 0.83 eV, respectively. Using the interpolation scheme of Van de Walle and Martin,[12] we calculate from our measured values, the average valence band offset for a $Si_{1-x}Ge_x/Si_{1-y}Ge_y$ heterojunction coherently strained to a relaxed $Si_{1-z}Ge_z$ substrate to be[13]

$$\Delta E_{v,avg}(Si_{1-x}Ge_x/Si_{1-y}Ge_y) = (y-x)[0.55(1-z)+0.43z]. \tag{7.7}$$

To calculate the actual values for the valence band offsets, we must also compute the spin-orbit splitting, deformation potential, and elastic constants for the $Si_{1-x}Ge_x$ alloy layer. A complete description of this procedure can be found in Ref. [13].

In Section 7.2.1, we concluded that the tunnelling current should increase as the width of the depletion layer decreases. In this section, we calculate the depletion layer width for a Si interband-tunnel diode and compare it to a HIT diode in which the *p*-side of the homojunction device has been replaced with $Si_{0.6}Ge_{0.4}$. In both cases, we have taken the carrier concentrations to be 1×10^{20} cm^{-3} and 5×10^{19} cm^{-3} in the *p* and *n*-sides of the devices, respectively. Our simulation involves solving Poisson's Equation in one dimension through the use of the Thomas-Fermi approximation and requiring charge neutrality across the entire device structure. A numerical solution is obtained through the use of relaxation techniques.[14] The resulting band diagram includes the effect of electrostatic band bending from which the depletion-layer width can be compared for the two cases. The program code has been supplied, courtesy of E. T. Yu and is discussed in detail in his Ph. D. thesis.[13]

In Fig. 7.2 we present the results of our calculations. The solid curve represents the energy of the conduction and valence bands in the homojunction device as a function of position. The bands corresponding to the $Si_{0.6}Ge_{0.4}/Si$ heterojunction device are shown in dotted line type. All calculations were carried out assuming a temperature of 4.2 K for devices in thermal equilibrium; therefore, the Fermi level is flat and has been defined as the zero-point energy (dashed-dot

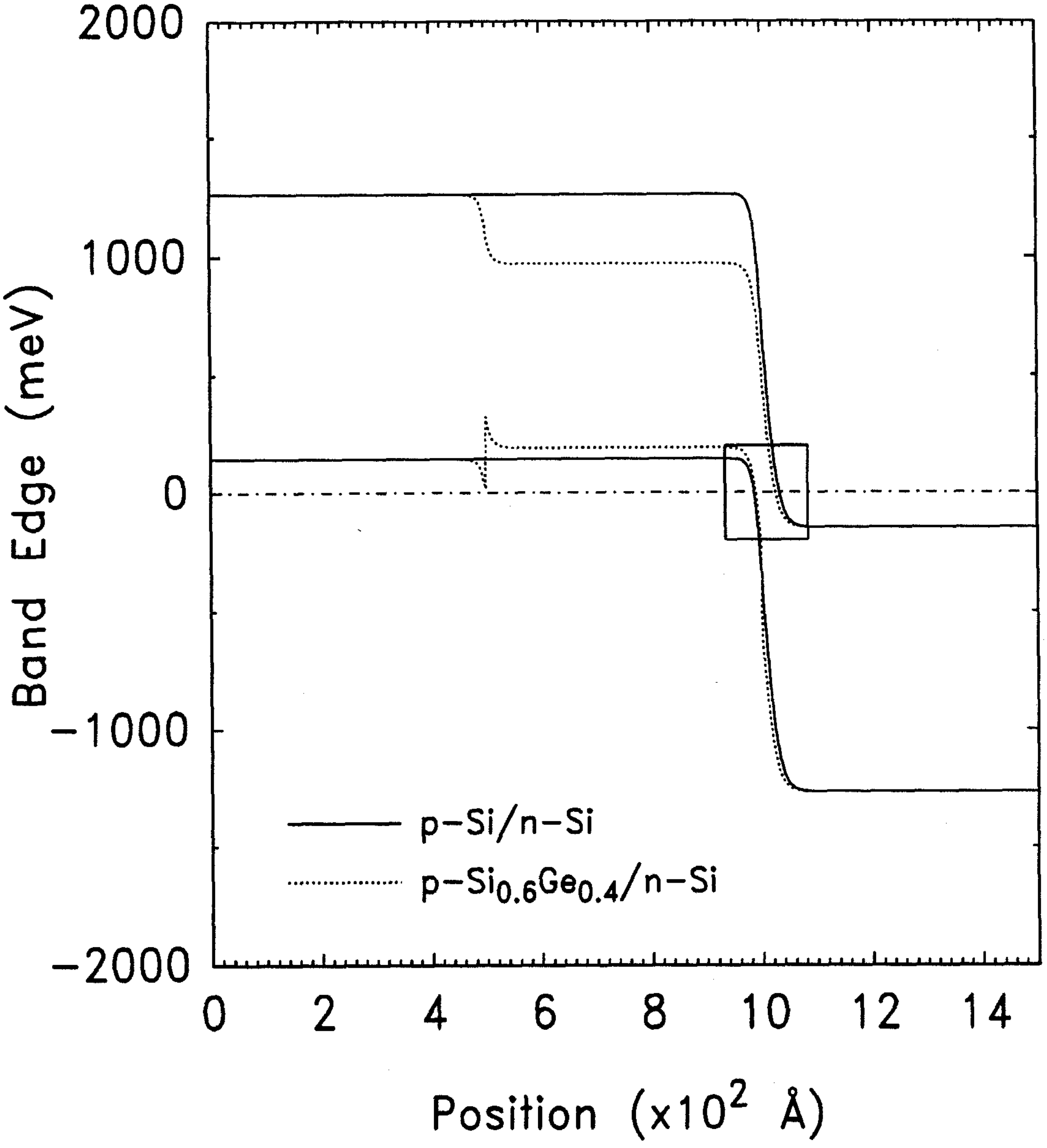

Figure 7.2: Band diagram for 500 Å n-Si/500 Å p-Si$_{1-x}$Ge$_x$/500 Å p-Si heterojunction interband-tunnel diodes at 4.2 K. Electrons in the conduction band on the n side of the degenerate p-n junction tunnel across the barrier region (boxed) to the valence band on the p-side (and vice-versa). Two cases are shown for comparison. The solid curve represents the homojunction case ($x = 0$), while the dotted curve represents the case where $x = 0.4$.

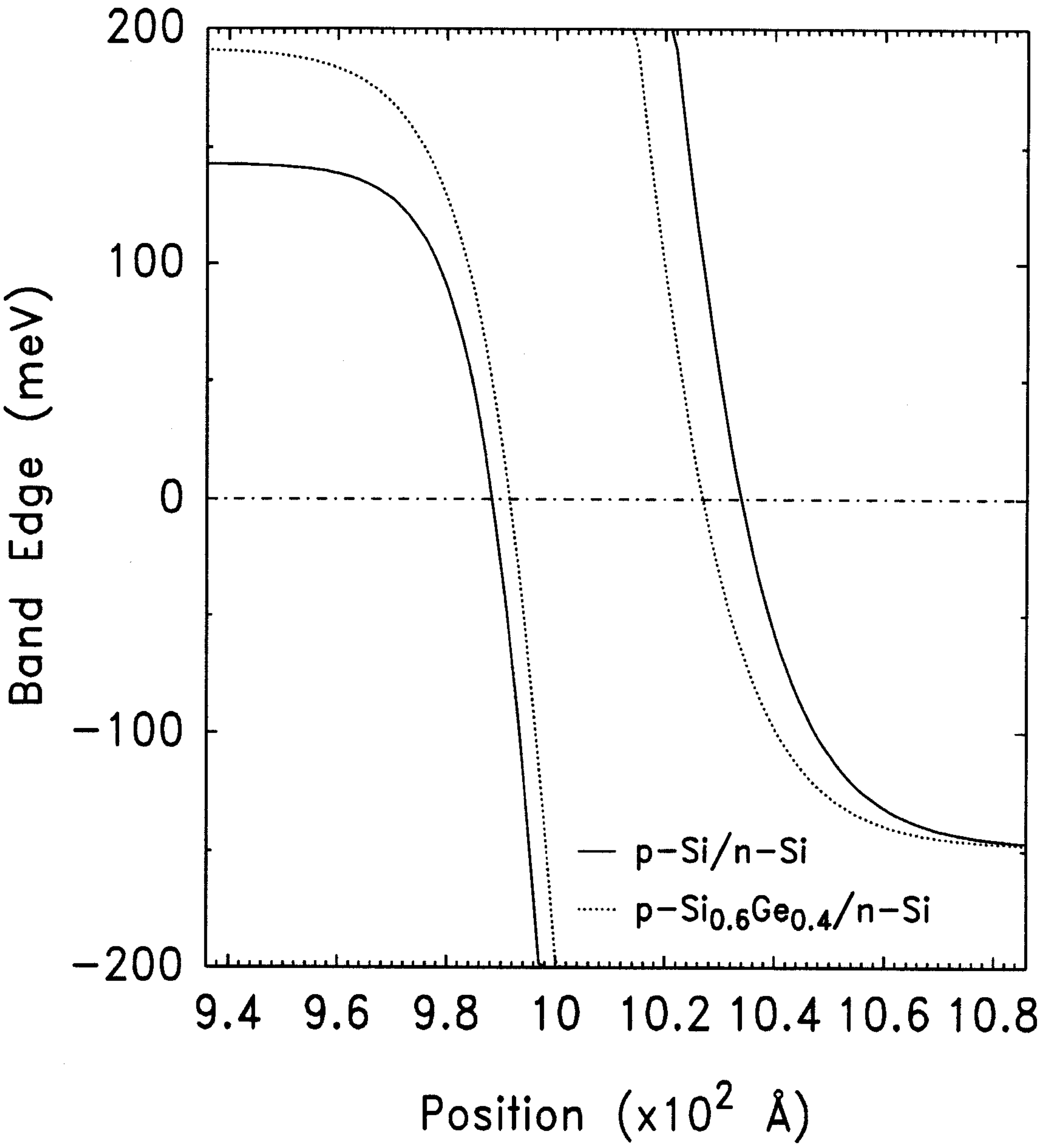

Figure 7.3: Expanded view of the boxed region of Fig. 7.2. As shown in the figure, the tunnel distance (band-to-band separation at $E_F = 0$) becomes measurably shorter for the heterojunction case (dotted curve) as compared with the homojunction case (solid curve), given identical doping profiles.

line type). An expanded view of the boxed region of Fig. 7.2 is shown in Fig. 7.3. Here, we can clearly see that the depletion layer in the heterojunction case is considerably less than for the homojunction case. As a result, Eq. 7.6 suggests that the tunnelling current component should be larger for the HIT device structure. Assuming that the excess and thermal contributions to the total current do not change, we predict an enhancement of NDR as the concentration of Ge in the HIT diode structure is increased.

7.3 Experimental

7.3.1 Sample Growth

Several HIT diode structures were fabricated for this study through the use of MBE growth techniques. The samples were grown in the Perkin-Elmer Si MBE machine described previously in Section 1.2.1. Si and Ge were coevaporated from a dual *e*-beam source onto radiatively heated, 3 in, (100) Si substrates nominally doped to 1×10^{20} cm^{-3} with B. Subsequent layers were doped through the use of elemental B and Sb effusion cells. The sample set studied here is described in Table 7.1. Prior to loading into the vacuum chamber, substrates were degreased *ex situ* and etched in a 50% HF solution similar to the procedure described in previous chapters of this thesis. After an *in situ* oxide desorption, 100 Å of intrisic Si were grown at 700 °C, followed by a 1200 Å *p*-type, Si contact layer. Each *p*-type layer was doped to 1×10^{20} cm^{-3} with B, and *n*-type layers were doped to 5×10^{19} cm^{-3} with Sb. The temperatures of the B and Sb sources during growth of the doped layers were 1840 °C and 440 °C, respectively.

The actual device structure consists of a *p*-type, $\mathrm{Si}_{1-x}\mathrm{Ge}_x$ alloy layer grown at 500 °C followed by an *n*-type Si capping layer grown at 420 °C. The thickness of

Sample	p-$Si_{1-x}Ge_x$ Alloy Layer		I_{peak}/I_{valley}
	x (% Ge)	Thickness (Å)	
A	0	500	···
B	10	1000	···
C	20	1000	···
D	30	500	1.033
E	40	250	1.055
F	50	130	···

Table 7.1: $Si_{1-x}Ge_x/Si$ HIT diode sample characteristics. Each sample was grown on a p-type, (100) Si substrate doped to 1×10^{20} cm^{-3} with B. Subsequent p-type layers were also doped to 1×10^{20} cm^{-3} with B. Following a 100 Å intrinsic Si buffer layer, a 1200 Å p-Si contact layer was grown prior to the p-$Si_{1-x}Ge_x$ alloy layer described in the table. After the alloy layer, a 2400 Å n-Si cap doped to 5×10^{19} cm^{-3} with Sb was grown. The peak-to-valley-ratio at 4.2 K for samples in which NDR is observed appears in column 4. We do not observe NDR for sample F, since critical thickness considerations required the $Si_{1-x}Ge_x$ layer to be grown too thin.

the $Si_{1-x}Ge_x$ alloy layer was chosen to place the layer below the empirical, critical thickness curve of People and Bean for growth at 550 °C.[3] The composition and thickness of the alloy layers are given in the table. The Si deposition rate was kept at 1.0 Å/s and the Ge rate was adjusted to result in the desired concentration. In practice, we have experienced little difficulty doping with B, as the sticking coefficient is approximately unity.[15] Doping with Sb, however, is more difficult. Sharp doping profiles are impossible to obtain at typical Si MBE growth temperatures (500 − 600 °C) because of surface segregation of the dopant. We have slightly modified the procedure of Jorke *et al.*[16] and Gossmann *et al.*[17] to obtain high doping levels without sacrificing crystalline quality. First, a 10 min predeposit of Sb resulting in a surface concentration of 6.0×10^{14} cm^{-2} (88% surface coverage) is deposited after the growth of the alloy layer was complete and the substrate temperature was lowered to 420 °C. Then, we deposited Si at 2.0 Å/s while the Sb flux was still on, resulting in a 2400 Å thick n-type Si capping layer. Under these conditions, doping takes place in the kinetically limited regime, producing an abrupt doping profile.

7.3.2 Device Fabrication

Two-terminal, mesa-diode devices were fabricated using standard photolithography and wet chemical etching techniques. First, a Au contact layer, approximately 2000 Å in thickness, was evaporated onto each sample. Then, 70 − 250 μm diameter mesas were patterned using standard photolithographic techniques and etched in commercial Au etch and 3:1:0.4 HNO_3:CH_3COOH:HF. Samples were mounted on an 8-pin header with In-Ga amalgam and silver paint. Contacts were wire-bonded to 116 μm diameter devices using the 4-point contacting scheme described in Section 1.5. A slight modification to this scheme was necessary since it was not possible to place two wire bonds onto a single device. Instead, a single connection was made between a device and a post; then, two contacts were made to the post.

7.4 Results and Discussion

7.4.1 *I–V* Measurements

I–V measurements were recorded digitally with the aid of a Hewlett-Packard (Model 4145) Semiconductor Parametric Analyzer for the samples shown in Table 7.1. Devices were characterized at both room temperature and 4.2 K. In these devices, NDR is observed only in forward bias, so we limited our data to this regime. In Fig. 7.4, we compare the current-voltage characteristics of a Si interband-tunnel diode and a $Si_{0.6}Ge_{0.4}/Si$ HIT diode (samples A and E). Since the structures of these samples are identical to the structures studied in Section 7.2.2, we expect to observe an enhancement of NDR for sample E over sample A. In the figure, the *I–V* curve for sample E shows a region of NDR, whereas for sample A, NDR is not observed. The shape of *I–V* curves, however, suggest that tunnelling *is* taking place in both samples, since at about 100 mV, the curvature of $I(V)$ changes sign, indicating that the maximum in the tunnelling component has been reached. Apparently the excess and thermal current components are too large in the homojunction device to allow the current to decrease at this point. Our results demonstrate an enhancement of NDR that is due to the decreased tunnelling distance in HIT diodes in comparison with their homojunction counterpart.

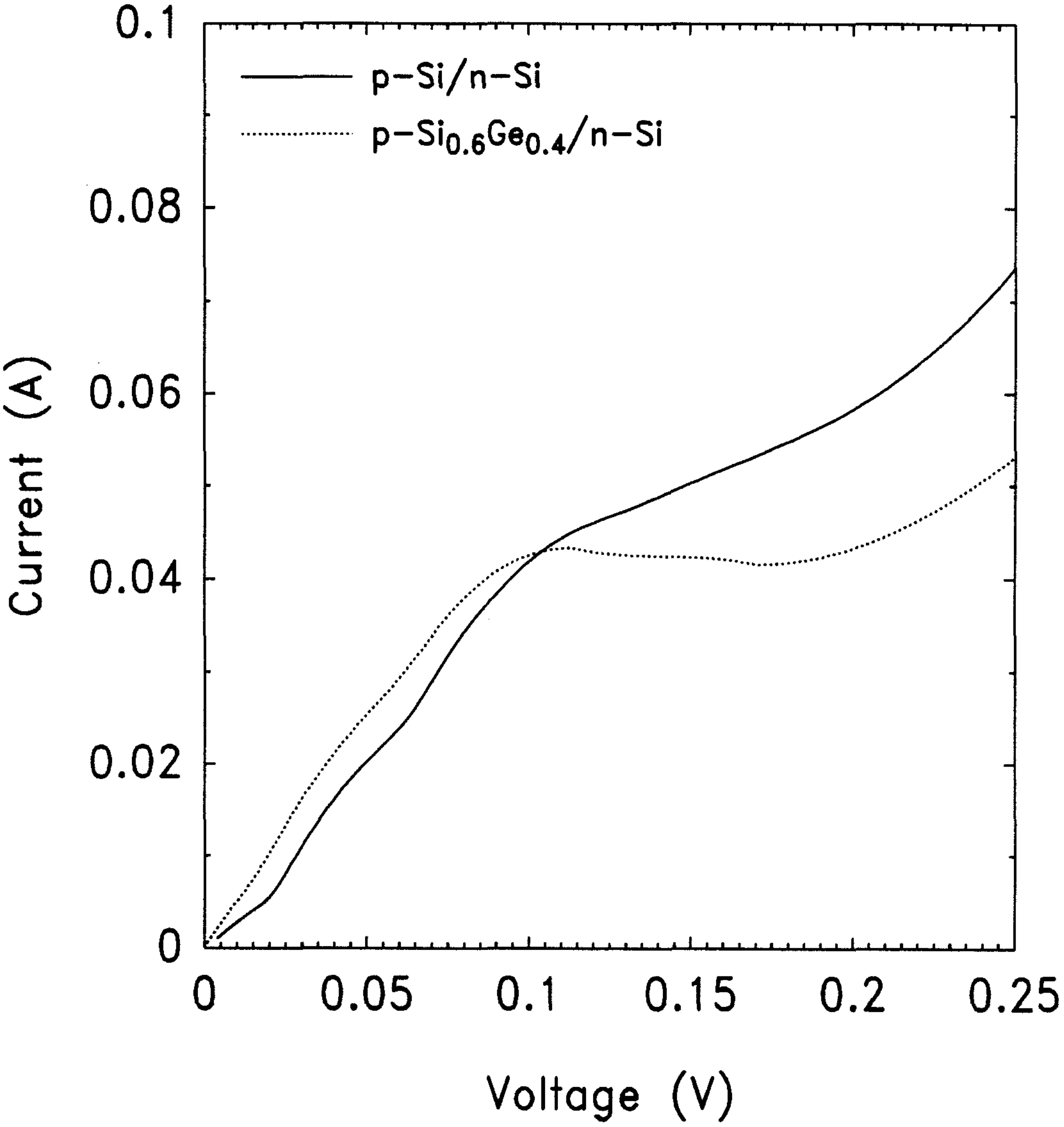

Figure 7.4: *I–V* characteristics for two devices made from samples A and E. At approximately 100 mV, the *I–V* curves for both devices begin to curve down, indicating the onset of negative differential resistance (NDR). Actual NDR is observed only in the heterojunction case, possibly because of the shorter tunnelling distance as compared with the homojunction case. The variation from nonlinearity for voltages less than 100 mV are due to phonons (see Fig. 7.5).

7.4.2 IETS Results

Because of the indirect nature of the band gap for both Si and $Si_{1-x}Ge_x$ alloys, conservation of momentum requires the emission of a phonon during the tunnelling process. Since the phonon carries energy, energy conservation forces the process to be inelastic. As the energy of the tunnelling electrons surpasses the energy of a particular phonon mode, the current-voltage relationship for the device undergoes a change in slope. An examination of the I–V curves presented in Fig. 7.4 reveals several "wiggles" associated with the excitation of phonon modes which are due to inelastic electron tunnelling. The onset of phonon excitation can be more clearly observed by taking derivatives of the I–V curves. The technique of inelastic electron tunnelling spectroscopy (IETS) used here measures $\frac{d^2I}{dV^2}$ as a function of voltage. A more detailed description of the technique is described by R. T. Collins in his Ph. D. thesis[18] and in Section 1.5.2.

In Fig. 7.5, we present inelastic electron tunnelling spectra from samples A and E at 4.2 K. Low temperatures are necessary to observe phonon interactions since at high temperature, the distribution of available phonon states becomes too diffuse. The solid curve in the figure represents the IETS spectra from a 116 μm mesa device fabricated from sample A, a Si interband-tunnel diode. The peak in the curve near 20 meV is due to the transverse acoustic phonon, while the peak located near 60 meV is associated with the transverse optical phonon.[19] In addition, the weaker, longitudinal phonon modes are also expected to appear near 60 meV. In the heterojunction case (sample E), several additional phonon modes are observed (dotted curve). The phonons responsible for the observed peaks have not been identified as yet, since a detailed study of phonon modes in a strained $Si_{1-x}Ge_x$/Si heterojunction is required. One might expect phonons associated with the strained $Si_{1-x}Ge_x$ alloy, the bulk Si, and/or interfacial modes to contribute. Since the phonons are emitted as the electrons tunnel across the junction region, interfacial phonon modes might be dominating the observed spectra.[20]

7.5 Chapter Summary

Through the use of modern MBE growth techniques, we have demonstrated successful operation of the first p-$Si_{1-x}Ge_x$/n-Si HIT diodes. The structures consist of a degenerate p-n junction composed of p-type, $Si_{1-x}Ge_x$ alloy and n-type Si grown coherently strained to a degenerate p-type, (100) Si substrate. Electrostatic band-bending calculations predict an enhancement of NDR because of the considerable valence band offset between Si and $Si_{1-x}Ge_x$. Measurements of I–V curves from HIT diodes compared with a Si interband-tunnel diode (homojunction case) confirm the enhancement effect. Finally, IETS spectra taken from these samples reveal additional phonon peaks in the heterojunction case, possibly associated with interfacial phonon modes. A more detailed description of phonon modes in strained $Si_{1-x}Ge_x$/Si is necessary to characterize fully the nature of the observed peaks.

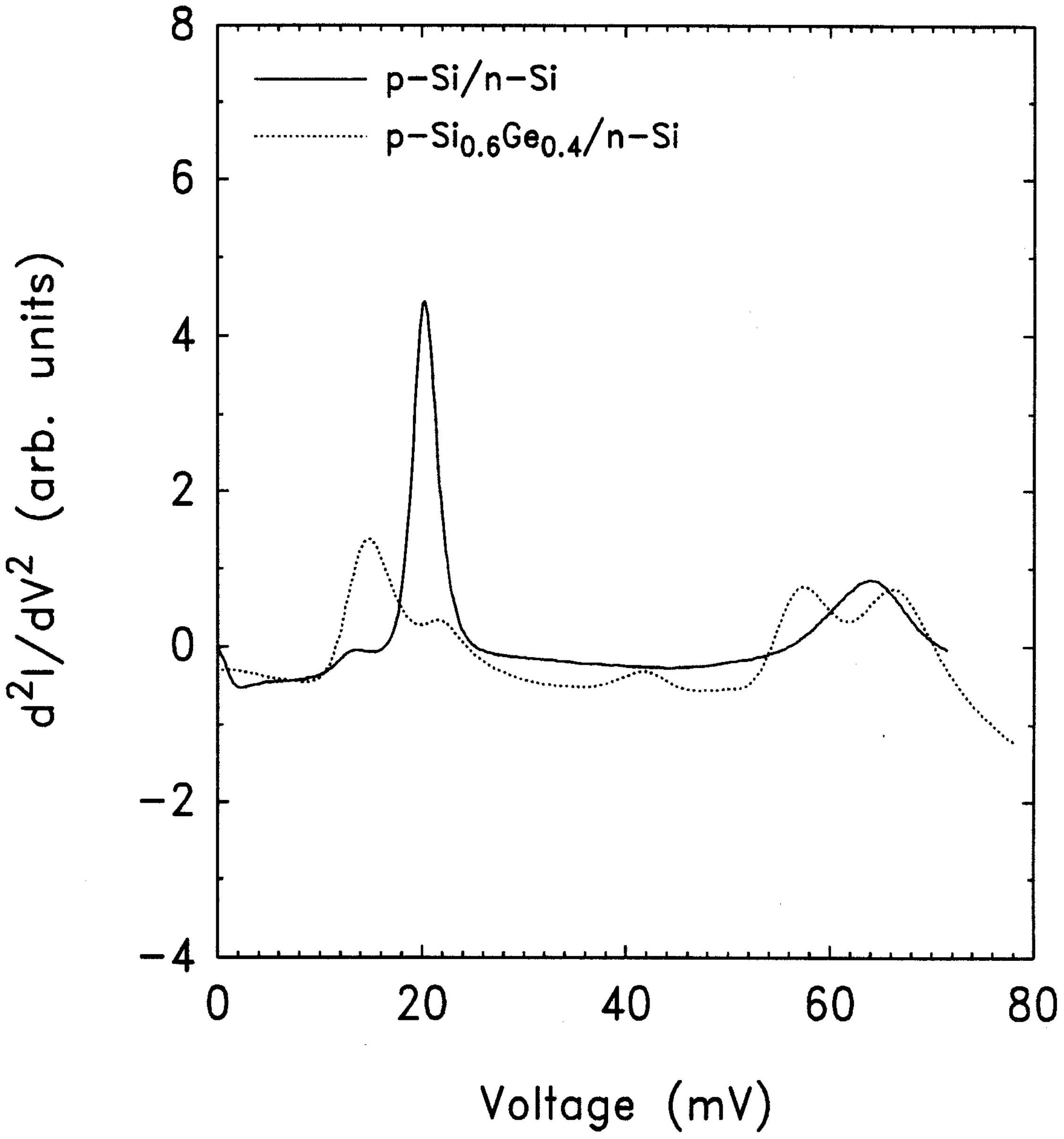

Figure 7.5: Inelastic electron tunnelling spectra ($\frac{d^2I}{dV^2}$ vs. V) for the two HIT diode structures previously discussed in this chapter. Two peaks identified with the transverse acoustic and transverse optical phonons are observed for the homojuction case (solid curve). Additional peaks are visible in the heterojunction case (dotted curve). The origin of these peaks is currently under investigation.

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Appendices

Appendix A

Considerations for the Design and Construction of a UHV STM / MBE System

A.1 Introduction

A.1.1 Scanning Tunnelling Microscopy

Since its invention in 1981 by Binnig and co-workers,[1, 2] the scanning tunnelling microscope (STM) has become a powerful tool for the purpose of studying surface electronic structure and topography. In recent years, the STM has been used to examine surfaces in air, in vacuum, and in liquids. Although just about any conducting material may be imaged, most studies have focused on semiconductor surfaces in order to understand the mechanisms of epitaxial growth. A few examples of semiconductor surfaces studied extensively include (100) Si,[3]-[6] (111) Si,[7]-[9] and (110) GaAs.[10]

With the STM, the surface-electronic properties of a conducting sample are imaged by scanning a sharp metallic tip (usually tungsten) across the sample surface at atomic distances. Precise control of the tip position with respect to the sample is achieved through the use of ceramic, piezoelectric transducer (PZT) elements. As the electronic wave functions of the tip overlap those of the sample, significant quantum-mechanical tunnelling current will begin to flow. In this regime, the current, I, is described by the equation[11]

$$I \propto \left(\frac{V}{d}\right) e^{-A\Delta\phi^{\frac{1}{2}}d}, \tag{A.1}$$

where V is the voltage across the tunnelling gap, d is the gap distance, $\Delta\phi$ is the average barrier height between the tip and the sample ($\sim$ 4 eV), and A is a constant roughly equal to 1.025 $(\text{eV})^{-\frac{1}{2}}\,\text{Å}^{-1}$. From the equation, the tunnelling current is predicted to increase by a factor of 60 for a decrease in the tunnelling gap of only 1 Å. The tunnelling current, therefore, is a sensitive function of gap distance.

The STM is capable of recording both topographic and spectroscopic information about the surface under study. In the topography mode, the gap distance is adjusted through the use of a negative feedback loop in order to maintain a constant tunnelling current. Images obtained in this way actually reflect the density of electronic states at the sample surface, and therefore, are only roughly related to topography. The spectroscopy mode involves decreasing the gain on the feedback loop and measuring the current-voltage relationship at a fixed gap distance. Some commercially available software packages allow the feedback loop gain to be changed from point to point in a scan, allowing approximately simultaneous topography and spectroscopy data to be obtained. In this way, spectroscopic information can be correlated to the features imaged in the topography mode of operation.

A high-performance STM should be capable of imaging surfaces with atomic resolution. Specifically, the resolution perpendicular to the surface (z-direction) must be better than 0.1 Å, and the lateral resolution (x- and y-directions) must be better than 1 Å.[12] These conditions require the STM to be isolated from the numerous noise sources present in a laboratory environment. Examples of noise sources include building vibrations, acoustic noise, electrical noise, thermal effects, and hysteresis of the PZT elements. In addition, coupling the STM to a molecular beam epitaxy (MBE) system seriously complicates the design. Not only must STM parts be compatible with the ultrahigh-vacuum (UHV) environment of an MBE growth chamber; in addition, special consideration must be given to the issues of damping high-amplitude, low-frequency vibrations and the handling of large samples.

A.1.2 Outline

In this appendix, we discuss the issues pertaining to the implementation of a UHV STM / MBE system. In particular, several issues are discussed at length in Section A.2. These include rigidity and vibration isolation, thermal drift stability, sample and tip manipulation, control electronics, and the computer hardware and software necessary for successful operation of the STM. Emphasis is placed on describing the complications associated with the integration of a UHV STM with an MBE chamber, and some possible solutions are suggested. The appendix concludes in Section A.3.

A.2 Design Specifications for the UHV STM / MBE System

A.2.1 Rigidity and Vibration Isolation

Adequate isolation of the STM from external vibrations is, perhaps, the most important aspect of a good design. The goal is to prevent excitation of modes resulting in the fluctuation of the tunnelling gap (δz) and the lateral position (δx, δy) of the tip with respect to the sample. In a well-designed microscope, the tip-position control should be an order of magnitude better than the desired resolution; therefore, the tolerances on δx, δy, and δz are[12]

$$\delta x, \delta y \leq 10 \text{ pm and} \tag{A.2}$$

$$\delta z \leq 1 \text{ pm.} \tag{A.3}$$

The overall scheme for vibration isolation of an STM involves restricting the resonant frequencies of the microscope and eliminating any external excitation of these resonances. Since the scan rate of an STM is limited by the minimum resonant frequency of the microscope, the design should attempt to make this frequency as high as possible, requiring the STM to be made small and rigid. In particular, the microscope should use a cylindrical PZT scanning element (tube scanner) as opposed to the tripod version because of its higher minimum resonance frequency. Several commercial STMs employing tube scanners are now available with a minimum resonance greater than 20 kHz.

To eliminate external sources of vibration, STMs are typically mounted on a dampening mechanism acting as a low-pass filter, preferably filtering excitations above 1 Hz. The most successful mechanisms currently employed include spring-dashpot arrangements, magnetic eddy-current damping, and Viton-spaced metal plates. Practical designs utilizing spring-dashpot arrangements are capable of suppressing vibrations to 2-5 Hz, as an example. In addition, many designs place the entire vacuum chamber on air supports, providing further protection from building vibrations.

Unfortunately, the high-amplitude, low-frequency vibrations generated by the cryopumps on an MBE machine require extraordinary measures to meet the design criteria. Originally, we discussed placing the STM in a separate vacuum chamber and isolating it from the MBE chamber with a bellows. Although the bellows should be capable of damping low frequencies, we concluded that significant high-frequency excitations would be transmitted, making this arrangement impractical. One alternative involves passing the sample through a separately pumped transfer stage located between the STM chamber and the MBE chamber. Once the sample transfer is complete, the transfer stage could be detached, physically separating the two chambers. After analysis, the transfer tube could then be reconnected to the STM chamber, pumped down, and the sample removed. Ideally, this approach should be successful; however, good STM images require the samples to be relatively contamination-free. As a result, samples must be transferred in UHV at all times, requiring a few days for the transfer stage to be baked out each time a new sample is studied.

A.2.2 Thermal Drift Stability

As the temperature of the STM changes, perhaps as a result of the introduction of a hot sample, different parts will expand and contract at different rates, causing the relative position of the tip and sample to change during a scan. Often referred to as thermal drift, this phenomenon can be as large as 1000 Å/ K and can occur in any direction. Some designs have taken into consideration certain drift-minimization schemes. In the x- and y-directions, thermal drift can be minimized using a PZT tube scanner and locating the tip along the tube axis. To further compensate drift in the x- and y-directions, the sample should be scanned near the center, since at this location, thermal gradients are at a minimum. To compensate drift in the z-direction, some designs incorporate concentric PZT tubes.[13] One tube controls the movement of the tip, while the other serves as a stage on which the sample is located. In this arrangement, the tip and sample move together in the z-direction as the temperature changes, compensating for temperature gradients along the tubes. As thermal drift cannot be totally eliminated, most commercial software packages are capable of performing drift correction.

A.2.3 Sample and Tip Manipulation

One of the more complicated aspects of integrating an STM with an MBE chamber involves designing a sample transfer scheme compatible with the MBE samples and sample holders. Most MBE machines use sample holders capable of carrying wafers two inches or larger in diameter. To prevent sample vibration from limiting the scan speed of the STM, samples should be as small as possible, since a large sample could decrease the minimum resonant frequency of the STM. As a result, the sample holder may need to be redesigned to accept a smaller sample. Unfortunately, modifying the size of the sample holder will make the task of calibrating growth temperatures more difficult. Another approach involves clamping the sample in the STM, effectively increasing the minimum resonant frequency. Once the sample is clamped in place, the STM tip can be lowered onto the sample surface, and tunnelling may proceed normally.

Practical operation of a UHV STM requires spare tips located inside the vacuum system to be exchanged *in situ*; otherwise, the chamber would have to be vented each time it was necessary to replace the tip. Tips are frequently destroyed by crashing into the sample or by picking up debris on the sample surface during the scan. Often, the sharpness of the tip may be recovered by raising the voltage on the tip and tunnelling against a tungsten sample. Tips may also be regenerated through the use of ion-sputter cleaning.

A.2.4 Control Electronics

Controlling the tip position in an STM is accomplished through the use of a negative feedback loop between the tunnelling current and the z-PZT. In the topography mode of operation, the feedback loop adjusts the gap distance to maintain a constant tunnelling current. The tunneling current is sent immediately to a preamplifier (and possibly, a logarithmic amplifier, to improve dynamic range) and compared with the desired current level. Subsequently, an error signal is sent to either a digital feedback amplifier or an analog version consisting of an integrator and proportional amplifier. In general, analog circuitry works faster than digital; however, some applications may require the added flexibility offered by digital feedback. Ultimately, the feedback signal is sent to the high-voltage amplifier that drives the z-PZT.[11] In any STM, the preamplifier should be located as close as possible to the tunnelling junction to minimize the shunt capacitance and to decrease noise amplification.[14] For the UHV STM, this means locating the preamplifier inside the vacuum system.

A.2.5 Computer Hardware and Software

Most commercial STM systems use a 386-based personal computer for data storage and analysis. Faster computers are not necessary, since the scan speed of the STM is limited by the response of the feedback circuit and/or the mechanical resonances of the microscope. When simultaneous topography and spectroscopy are performed, extremely large amounts of data are generated; therefore, the memory of the computer system must be quite large. A typical scan may produce, for example, a 512×512 array of single-byte data (0.26 MB). Assuming that only 10 points of an I–V curve are taken at each point in the trace of a spectroscopy run, as much a 2.9 MB of data will be generated. Data generation at this rate would require large memory capacity in the computer system and immense disk storage-space capability. A conservative estimate would place the requirements on RAM at about 4 MB and hard-disk capability at 50-100 MB. In addition, most software packages have the capability of performing some limited drift correction as well, assuming that the drift can be approximated as being linear. Standard display modes for the data include gray scale plots, contour plots, and linescans. Finally, the more advanced software packages can perform surface rendering on the data, including three-dimensional shading and two-dimensional Fast Fourier Transform (FFT) filtering, for example. In the ideal STM system, one would like the capability of generating all of these various displays and rendering options.

A.3 Summary

In conclusion, we have discussed the design considerations for the integration of a UHV STM with an MBE chamber. The most important problems we foresee involve vibration isolation of the microscope from the low-frequency, high-amplitude vibrations generated by cryopumps and the practical considerations of manipulating large samples. We conclude that the STM must be located in a separate chamber accessible to the growth chamber through the use of a detachable transfer stage. Finally, the samples should be clamped so that the resonances associated with the sample do not limit the performance of the microscope.

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Appendix B

Instructions for Maintaining and Operating the MBE Systems

B.1 Introduction

The purpose of this appendix is to describe some of the procedures and precautions necessary for the proper maintenance and operation of the two molecular beam epitaxy (MBE) systems used to grow the samples studied for this thesis. In particular, the custom-built Si-silicide and the Perkin-Elmer (Model 430S) Si MBE systems are discussed. Proper maintenance of MBE systems requires periodic access to the components inside the vacuum chamber. When dealing with vacuum parts, care must be taken to avoid introducing particulates and oils into the ultrahigh-vacuum (UHV) environment. For example, a single fingerprint will outgas considerably, limiting the ultimate system pressure and contaminating the samples. Clean latex gloves are typically employed for this reason and should be changed frequently when their cleanliness becomes in doubt. Remember, the price of gloves is insignificant compared with the cost of a new chamber. The following procedures are undoubtedly incomplete; therefore, the operator should exercise extreme caution and common sense when performing each step.

B.2 The Si-Silicide MBE System

B.2.1 Venting the System

Venting of the system should be avoided if at all possible, since the system will be down for several days. Most often, the system will need to be vented to replace sources. The *e*-beam sources for the Si-silicide system are located in the bottom half of the growth chamber. To gain access, the top part of the chamber (bell jar) must be removed. The following steps detail the procedure used to replace the source material in preparation for a system bakeout.

1. Remove the water lines and blow out any liquid water remaining in the shrouds. During the bakeout, the temperature of the system will exceed 100 °C, causing any remaining water to vaporize and potentially damage the shrouds.

2. Remove the electrical connections to the system. These include connections to the *e*-beam evaporators, the substrate heater, the heater thermocouple, the Inficon (Model XTC) crystal sensors, the residual gas analyzer (RGA), the ionization gauge, and the low-energy electron diffraction (LEED) optics.

3. Remove the LN_2 buckets from the heater and *e*-beam cooling shrouds. Do not vent the system until the LN_2 shrouds have returned to room temperature.

4. Remove the shield on the transfer rod.

5. Adjust the heater position with the manipulator so that the bellows is compressed. Avoid compressing the bellows completely since this may cause

a leak. Also, do not allow the heater to contact the LN_2 shroud. The shroud is very fragile, and leaks may develop in the welds if it is bent.

6. Detach the shutter actuators from the magnets internal to the system. This will avoid damage when the bell jar is removed.
7. Close the valve to the load-lock ion pump. Leave the gate valve to the growth chamber closed.
8. Vent the load lock by opening the dry N_2 line to the manifold and subsequently opening the valve between the load lock and the manifold.
9. Remove the bolts connecting the load lock to the gate valve and pull the load lock slightly to the side. Blank off the 6-inch flange on the load lock and pump down to a rough vacuum with an oil-free mechanical pump. Protect the gate valve from contamination by covering it with Al foil.
10. Close the pop-it valve located under the *e*-beam LN_2 shroud and shut off the main ion-pump controller.
11. Vent the chamber by opening the metal seal valve located just above the manifold.
12. If the substrate heater is to be removed, it is necessary to remove the LEED optics first. Be sure to protect it with Al foil after removal. Always unbolt the 8 inch flange of the substrate heater, **not** the 6-inch flange, since the LN_2 shroud will need to be rewelded to reseal the flange.
13. Remove the 18 bolts surrounding the Wheeler flange connecting the bell jar to the bottom of the chamber.

14. Attach the Al collars to the bell jar and use the crane to remove it. Set aside.

15. Remove the shutter assembly by removing the three Au-coated allen-head screws connecting it to the LN_2 shroud. Place it on a clean cloth suitable for vacuum parts.

16. Vacuum the inside of the chamber as necessary. A hollow tube works well as an attachment. Be sure it is clean.

17. Degrease the shaped Si charge and W crucible in trichloroethylene (TCE), acetone, methanol, and de-ionized water. Etch the charge in 3:1:0.4 HNO_3:CH_3COOH:HF and load it into the W crucible and place in an *e*-beam hearth. Load the second *e*-beam hearth with an appropriately cleaned, pure material. Previously, we have evaporated Ni, Co, V, and Ge in addition to Si.

18. Replace the shutter assembly.

19. Remove the old Cu wire seal gasket surrounding the Wheeler flange and replace.

20. Lower the bell jar onto the wire seal. Be sure to align the position of the bell jar properly. Use a pencil mark to aid in this process.

21. Close the shutter actuators and verify proper operation of the shutter mechanism.

22. Reseal the Wheeler flange. Make three passes with a torque wrench set at 40, 60, and 75 ft-lbs. Alternate back and forth from one side of the chamber to the other when tightening the bolts.

23. Replace all remaining vacuum parts. Be sure to use a new Cu gasket for each seal.
24. Open the gate valve, reach in, and reseat the LEED shield and the Si mirror. Try to avoid touching the inside of the system with your sleeve. Al foil may be used to prevent contact with the interior of the chamber.
25. Replace the 6-inch Cu gasket and rebolt the load lock onto the gate valve.
26. Leave the gate valve open, rough out the chamber and load lock simultaneously, first with the oil-free mechanical pump, then with the sorption pumps. Open the pop-it valve.
27. When the pressure reads less than 1×10^{-3} Torr, replace the electrical connection to the ionization gauge and monitor the pressure.
28. Close the gate valve, open the valve to the load lock ion pump, and turn on the main ion-pump controller once the pressure falls below 3×10^{-4} Torr. Reseal the metal seal valve on the manifold with a torque wrench set at 25 ft-lbs.

B.2.2 Baking the System

After pumping overnight, the system pressure should be in the 10^{-7} Torr range or below. At this point, the ultimate system pressure is limited by the slow release of gases such as N_2 and water vapor trapped in the walls of the chamber. To bring the pressure down to the 10^{-11} Torr range, it is necessary to "bakeout" the chamber by heating the walls to a temperature of 160 °C through the use of external heating elements. At this temperature, the absorbed gases are released into the vacuum and pumped away. The following steps detail the bakeout procedure.

1. Complete steps 1-5 of the venting procedure described in Section B.2.1.

2. Close the shutter actuators.

3. Remove the Al collars used to raise the bell jar.

4. Wipe down the chamber with propanol and cover the quartz windows with Al foil to prevent cracking.

5. Position the two black panels on the system frame. Try to minimize any openings to the bottom of the chamber.

6. Wrap the transfer rod, the load lock, and the gate valve with heating tape. Cover with Al foil.

7. Place a thermocouple (type K) on the 8-inch flange connecting the gate valve to the bell jar. The bakeout is interlocked, so this temperature does not exceed 160 °C.

8. Position the two bakeout shrouds around the bell jar. The two shrouds should abut the gate valve on one side and join together on the other side.

9. Use Al foil to cover any openings to the system. Try to create an enclosure surrounding the chamber. Plug the bakeout shrouds into the sockets located to the left of the pumpwell LN_2 bucket.

10. Open the gate valve slightly to prevent deformation of the viton seal during heating.

11. Connect a Keithley (Model 230) programmable voltage source to the IEEE bus. The voltage source is controlled by the Hewlett Packard personal computer to output 30 V when the temperature is too low and 0 V when

it is too high. The voltage signal is sent to a relay connected in series with the bakeout controller located next to the main ion-pump controller.

12. Connect the output of the voltage source to the relay.

13. Send the thermocouple signal to the Eurotherm controller and the "PROG OUT" signal to the Keithley (Model 195A) digital multimeter. Be sure to depress the red button on the back side of the multimeter.

14. Set the temperature setpoint on the Eurotherm controller to 160 °C.

15. Use variable transformers to power the heating tapes. Do not exceed 30% power at 140V.

16. Begin running the program "BAKEOUT" on the HP computer. If the interlock is set up properly, the relay should open as soon as the program begins to run.

17. Switch on the bakeout controller. The switches corresponding to the pump and the manifold should be in the down position, whereas the bell jar and chamber switches should be up. The pressure interlock is set so that the heater turns off when the pressure rises above 1×10^{-5} Torr and turns on when the pressure falls below 2×10^{-6} Torr.

18. Once the temperature reaches 160 °C and the pressure has fallen below about 5×10^{-7} Torr, the bakeout is complete (usually after a day or so).

19. Turn off the bakeout control and the variable transformers. Let the system cool to room temperature.

20. Remove the Al foil, heating tape, thermocouple, bakeout shrouds, and black panels from the system.

21. Close the gate valve.

22. With steel wool, remove CuO from the Cu electrodes for the e-beam evaporators and the substrate heater. Attach all electrical and water-cooling connections. Connect the LN_2 buckets to the shrouds.

23. Degas the ionization gauge for approximately 1/2 h. Degas the RGA and LEED gun filaments, as well.

24. Replace the shield on the transfer rod.

25. Flash the titanium sublimation pump (TSP) for 2 min at 47 A. Do not exceed 47 A or the filament may break. The pressure should begin to fall quickly through the 10^{-10} Torr range after the TSP is shut off.

B.2.3 Running the System

Once the system has been properly baked out, the pressure should be below 1×10^{-10} Torr. The following procedure describes how to outgas the newly loaded e-beam sources and grow a sample.

1. Keeping the gate valve closed, vent the load lock. Be sure to close the valve to the ion pump first.

2. Degrease a substrate in TCE, acetone, methanol, and de-ionized water and etch in 50% HF if the substrate is Si. Rinse again in de-ionized water, place the substrate in the substrate holder, and screw the holder into the nosepiece at the end of the transfer rod.

3. Rough out the load lock with the oil-less mechanical pump and the sorption pumps.

4. Open the ion pump valve **slowly** and let the load lock pump into the 10^{-7} Torr range.

5. Position the substrate heater so that it is free to rotate. Set the z-direction (out of the system) to align the zero on the moving piece with 26.5 mm on the fixed piece. The vertical position should be set at 4.6 mm, and the horizontal position should be set to 7.0 mm. **FAILURE TO POSITION THE SUBSTRATE HEATER PROPERLY PRIOR TO ROTATION MAY RESULT IN DAMAGE TO THE LEED OPTICS AND A COSTLY REPAIR PROCESS.**

6. Rotate the substrate heater so that the Si mirror is facing toward the *e*-beam sources (*i.e.*, down). Open both shutters.

7. Turn on the water cooling. The *e*-beam power supplies will not operate unless the flow rate to the hearths exceeds 0.5 gal/min. Fill the LN_2 buckets and wait until ice is observed on the return side of the shrouds.

8. Turn on the *e*-beam power supplies and the high voltage. Turn on the Tektronics (Model TM 5006) power module. Set the Inficon (Model XTC) controllers to manual mode. The power to the *e*-beams can now be operated with the manual switches.

9. Carefully raise the *e*-beam power levels to 25%. Be sure that the pressure does not exceed 10^{-7} Torr. Raise the power on one of the guns until the source begins to glow red. Record the power level at which this occurs as "SOAK PWR 1." Slowly increase the power level again until the source material begins to melt. Avoid causing the material to spit or flow out of the crucible. If for any reason you think the source is empty, **STOP HEATING IMMEDIATELY**. A potentially catastrophic failure mode

exists if the *e*-beam melts through the hearth to the cooling water. Carefully increase the power level until the desired deposition rate is reached. Record the power level as SOAK PWR 2. Cut the power to the e-beam source. Repeat with the second *e*-beam source.

10. Program the Inficon controllers for automatic operation. Set RISE TIME 1 to 2 min, SOAK TIME 2 to 3 min, RISE TIME 2 to 5 min, and SOAK TIME 2 to 3 min. Set MAX PWR to SOAK PWR 2 + 2%. Set the IDLE PWR to 0% and the IDLE RAMP TIME to 5 min. Also set the density, thickness, and tooling factor as desired. The tooling factor is used to calibrate the controller. A calibration sample should be grown, and the thickness of the sample should be measured independently. Set the new tooling factor to the value of the old tooling factor multiplied by the measured thickness divided by the expected thickness.

11. Open the gate valve and load the substrate onto the substrate heater. Rotate the substrate down to the growth position. Locate the substrate inside the LN_2 shroud.

12. The substrate temperature has been calibrated to the heater power level through the observation of Au/Si and Al/Si eutectic reactions, assuming a T^4 dependence. Use programs "T_to_P" and "P_to_T" to determine the substrate temperature.

13. Turn on the Lamda power supply for the substrate heater.

14. Use the third Inficon controller to program the substrate temperature. Maximum power (100%) corresponds to 15 V. For most applications, the heater power level should not exceed 83% (12.5 V).

15. Begin increasing the substrate to the desired temperature. This should take at least 15 min. Open the shutters halfway. After 2 min, begin ramping up the *e*-beam sources. Once the deposition rate has settled down to the setpoint value and the substrate has reached the desired temperature, open the shutters fully.

16. When the deposition is complete, close the shutters halfway, shut off the *e*-beam sources, and allow the substrate to return to room temperature.

17. Turn off the *e*-beam and substrate heater power supplies, the Tektronics power module, and the water cooling. Remove the substrate through the load lock.

B.3 The Perkin-Elmer Si MBE System

B.3.1 Venting the System

Maintaining the Perkin-Elmer Si MBE machine proceeds similarly to maintaining the Si-silicide machine. In this section, we outline the steps necessary for venting the Perkin-Elmer growth chamber in preparation for a bakeout.

1. Bring the effusion cells down from idle temperature (200 °C) to room temperature.

2. Shut off the water flow to the cooling lines and flush with 4 psi N_2 to remove any liquid water. Disconnect the water lines to the *e*-beam sources and the crystal sensor. It is not necessary to disconnect the water lines to the substrate heater unless the heater is to be removed.

3. Remove the LN_2 cooling lines and close the valve on the return to prevent any LN_2 from flowing back from the phase separator. Do not close this

valve when the LN_2 lines are connected to the chamber, since the pressure will build up too high when the shrouds begin to warm up. A 20 psi relief valve is used to limit the maximum pressure in the shrouds.

4. Detach the electrical connections to the *e*-beam source (Amphenol connector), RHEED gun, and flux monitor. Remove the photomultipliers and related electrical connections. Place the filters in dessicant vials and cover the apertures with Al foil. Remove the electrical connections to the crystal sensor.

5. Trip the main circuit breaker inside the *e*-beam power supply. Carefully remove the covers to the four high-voltage connections and short the electrodes to ground. **BE SURE TO CONNECT THE GROUND STRAP TO GROUND FIRST, TO AVOID DANGEROUS VOLTAGES**. Disconnect the high-voltage cables.

6. Remove the manual, transfer-rod control handle and set aside.

7. Leave the N_2 pressure attached to the shutter actuators to allow easy access to the sources.

8. Leave the thermocouple and substrate heater power cables attached unless the substrate heater is to be removed.

9. Remove the pyrometer, cover the aperture with Al foil, and set aside.

10. Check the cryopump (CT-8) valve to make sure it is closed. Close the ion-pump valve.

11. Disconnect the pump cart from the load-lock manifold, blank off the fitting, and connect the cart to the chamber manifold. Open the green valve on the cart to flood the manifold with dry N_2.

12. Vent the chamber by opening the Au seal valve located between the manifold and the chamber.

13. Remove the bolts on the bottom half of the *e*-beam flange and attach the support. Remove the remaining bolts and withdraw the *e*-beam source flange from the chamber. Be careful not to let the flange roll off the tracks.

14. Remove the old source material and vacuum the hearths as necessary. Replace the sources with properly cleaned and etched Si and Ge.

15. Replace the wire seal around the *e*-beam flange and rebolt the flange onto the system, reversing the procedure described in step 13.

16. Pump out the chamber with the sorption pumps, beginning with the one on the far right. When the pressure falls below 10^{-3} Torr, begin monitoring it with the ionization gauge. When the pressure falls below 10^{-4} Torr, open the ion-pump valve and close the Au seal valve with a torque wrench set at 45 in-lbs. The pressure should come down into the 10^{-8} Torr range overnight.

B.3.2 Baking the System

The Perkin-Elmer Si MBE chamber also requires a bakeout to reach an ultimate pressure of 1×10^{-10} Torr. The procedure is outlined below.

1. Ramp the effusion cells to 200 °C over 30 min. See the Micristar manual for instructions.

2. Wipe down the chamber walls with propanol or spray cleaner. Cover the quartz windows with Al foil to prevent cracking.

3. Cover the chamber with the bakeout blanket. The blanket should fit snugly around the *e*-beam source flange and the dopant source flange. Avoid uneven heating of the flanges, as differences in thermal expansion may cause leaks.

4. Ramp the substrate temperature to 400 °C in 20 min.

5. Remove the tabletop and pull out the bakeout interlocks, as they tend to get stuck.

6. Turn on the three circuit breakers and switch the bakeout power on. Reach inside the blanket to verify that the heaters are working properly. The bakeout temperature is interlocked automatically at 200 °C, and the pressure interlock is set to 2×10^{-6} Torr (SPT 3 on the Perkin-Elmer (Model DGC III) ionization gauge controller).

7. After a day or so, the pressure should be in the 10^{-7} Torr range, and the bakeout can be shut off. Let the system cool for 24 h before removing the bakeout blanket and the Al foil covering the quartz windows.

8. Degas the RGA filament, ionization gauge, and flux monitor. Flash the TSP for 2 min. Leave the effusion cell temperatures idling at 200 °C. Turn off the substrate heater. The pressure should fall well into the 10^{-10} Torr range overnight.

9. Reattach all electrical connections, water, and LN_2 cooling lines. Once the pyrometer has been connected and the tabletop has been replaced, the system should be ready to run.

B.3.3 Running the System

In this section, the procedure used to grow a $Si_{1-x}Ge_x$ alloy layer on (100) Si is described. The photomultiplier gain constants and tooling factors are assumed to be calibrated previously. Refer to the Micristar and Inficon (Model Sentinel III) manuals for the details concerning the operation of these instruments.

1. Degrease a (100) Si substrate at 50 °C in (1,1,1)-trichloroethane (TCA), acetone, and methanol. Rinse in de-ionized water and etch in 50% HF. Rinse again in de-ionized water prior to loading into the substrate holder.

2. Vent the load lock, position the substrate holder in the cassette, and rough out with the sorption pumps. When the pressure has fallen below 5×10^{-4} Torr, close the butterfly valve and open the cryopump (CT-100) valve.

3. Once the pressure in the load lock has fallen below 10^{-7} Torr, open the valve to the transfer tube and lower the cassette.

4. Move the substrate down the transfer tube and into the growth chamber. Be sure to close the gate valve between the chamber and the transfer tube only after the transfer rod has been fully retracted.

5. Open the cryopump (CT-8) valve. Begin cooling the LN_2 shrouds. Start supplying cooling water to the various parts of the chamber. Be sure to open the return valves first, before opening the supply valves.

6. Turn on the reflection high-energy electron diffraction (RHEED) power supply and carefully increase the filament current to 3.1 A at 0 kV.

7. Check the operation of the shutters and adjust the N_2 flow rate accordingly. Don't allow the shutters to open and close too abruptly, or they may be damaged.

8. Turn on the Inficon (Model Sentinel III) deposition controller and set the parameters to ramp the *e*-beam sources to SOAK PWR 2 in 20 min. Set the deposition rates to 0.1 Å/s for both the Si and Ge sources. Turn on the *e*-beam power supply. Turn on the heater power supply and increase the substrate temperature to 860 °C in 30 min. Start the Inficon program 10 min later.

9. As soon as the substrate temperature reaches 860 °C, open the RHEED shutter and turn on the high voltage. Adjust the RHEED controls as necessary to obtain a sharp pattern. Open the Si shutter until a (2×1) reconstruction is observed (about 2 min). Turn off the high voltage and close the RHEED shutter.

10. Ramp the substrate temperature to 500 °C in 25 min. Ramp the Si deposition rate to 1.0 Å/s.

11. Turn on the substrate rotation to 15 rpm. Open the Si shutter when the substrate temperature reaches 700 °C. After 1200 Å of Si have been deposited, close the shutter. The substrate surface should be atomically smooth at this point in the deposition.

12. Set the Ge deposition rate to result in the desired Ge concentration. Open the Si and Ge shutters simultaneously and deposit $Si_{1-x}Ge_x$ to the desired thickness. A coherently strained film can be grown below the critical thickness at a substrate temperature of 500 °C.

13. When the deposition is complete, stop the substrate rotation, close the shutters and ramp the *e*-beam sources back to room temperature. Turn off the power supply.

14. Ramp the substrate back to room temperature and turn off the heater power supply.

15. Open the RHEED shutter and turn on the high voltage. Adjust the controls to obtain a sharp pattern. For compositions between 10 and 30% Ge, we have observed a (2 × 8) reconstruction on the (100) $Si_{1-x}Ge_x$ alloy surface (see Chapter 5).

16. Once the substrate has returned to room temperature, it can be removed from the growth chamber.

17. Be sure to shut off the LN_2, close the cryopump valve (CT-8), and turn off the RHEED power supply and the water cooling before leaving the room. The water flow to the chamber and the manipulator may be left permanently in the "on" position.