Resonant Power Processing at a Fixed Frequency Using a Controllable Inductance

Thesis by

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Dedicated to My Parents, Jay and Gayle Vollin

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Abstract

Power processing at high frequencies often involves the use of resonant conversion techniques. Most of these techniques require the use of a variable switching frequency to provide control over the output voltage or current. In many applications this variable switching frequency is not tolerable and another method of regulation is required. A novel device called a magnetic regulator can be used in conjunction with a resonant DC-to-DC converter to provide regulation of the output voltage or current at a fixed switching frequency. This device resembles an ordinary transformer except with an additional winding which provides control over the input-output conversion ratio.

Prior to the use of the magnetic regulator, suitable resonant DC-to-DC converters are identified and partitioned into a resonant inverter which converts the incoming DC energy into high frequency AC energy and into a rectifier circuit which converts the AC back to DC. The candidate inverters used include the Class E and Class D Zero-Voltage-Switched circuits. Since the rectifier circuit must be compatible with the choice of the inverter, the design details of such a rectifier are presented.

The magnetic regulator is modeled using the reluctance concept exposing the true nature of the regulation mechanism. The control current changes the permeability of a portion of the core of the device which results in a current-controlled leakage inductance.

The magnetic regulator may be inserted into the forward power path of a resonant DC-to-DC converter. In the process, it is possible to integrate the resonant inductor and a matching inductor into the basic structure of the magnetic regulator. The result is a high frequency, resonant converter with only one or two magnetic components which can be controlled by a low-level control signal without resorting to a variable switching frequency.

The inclusion of a variable inductance poses special problems in the design and modeling of the control loop which regulates this family of converters. The small-signal model of the magnetic regulator is derived and verified with experimental results. This model is then incorporated into a model for the DC-to-DC converter. The converter model is presented with three levels of complexity beginning with a very simple model which exposes the contribution of the magnetic regulator to the overall response of the converter. The model is further refined to include a bilateral model for a resonant rectifier with a final bilateral model for the inverter.

The model of the complete DC-to-DC converter is compared against simulated data from the computer program SPICE and also against measured data on a typical converter. The model is shown to contain low frequency dynamics dominated by the input and output filters on the converter, and high frequency dynamics associated with the resonant circuit elements. The models developed are continuous-time average models which are conveniently represented using equivalent circuits.

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Chapter 1

Introduction

Motivation for the Research

The field of power electronics is concerned with the art and science of converting electrical energy from one form to another, emphasizing the minimization of the power lost by the processing circuitry. The minimization of the volume, weight, and cost of this processing circuitry are also important factors which have driven the development of many different approaches to the problem. One industry in particular has motivated the search for better circuits and methods of power conversion, and that is aerospace. The need for electronic systems to operate in airborne environments has driven the power processing circuitry to ever-increasing levels of sophistication.

One application of airborne electronics which motivated the developments described in this thesis is that of the airborne radar. A typical radar consists of a transmitter and a receiver along with various signal and data processing functions. The radar transmitter has very stringent requirements for signal purity which translate into ripple and noise requirements on the transmitter's power processing circuitry. Most aircraft radar transmitters employ vacuum tube microwave devices such as magnetrons, klystrons and traveling wave tubes (TWT's). These devices have been used because of their ability to produce large amounts of microwave energy. The TWT is popular because of its inherent wide bandwidth in addition to its high power.

In order to operate, the TWT requires several bias voltages which range up to 100 kV in some high power systems. A more common requirement would be 20 kV. This high voltage is produced by a high voltage power supply (HVPS) which often is a significant portion of the entire radar in relation to its weight, volume and cost. Additionally, the HVPS is frequently the least reliable subassembly in the entire radar. These facts have driven power supply designers to search for better methods of generating and regulating high voltages. Significant gains in this area have been made possible by the advent of the high-frequency switching power supply. In most power processing applications, the switching frequency is a free parameter which the designer can manipulate to optimize the design. Unfortunately, this is usually not the case in the radar HVPS.

In a radar the TWT acts as a modulator, converting any signals on the bias electrodes into modulation of the amplitude and phase of the transmitted signal. Any power supply for these bias voltages will produce some residual ripple as a result of the power conversion process. This ripple will modulate the microwave carrier signal with sidebands which are spaced above and below the carrier signal by the frequency of the ripple. Many modern radar designs use the doppler shift of the target to determine the velocity of the target. In these systems, the receiver is effectively a spectrum analyzer which scans for any signals near the microwave carrier frequency. The typical velocities of airborne targets place the doppler-shifted return signals from the radar between zero and several kilohertz. If the ripple out of the high voltage power supply has frequency components in this range, the receiver may mistake these signals for real target returns. One technique that is used to combat this problem is to synchronize the switching frequency of the HVPS to the pulse repetition frequency of the radar. This will place any modulation of the transmitted signal by the power supply coincident with the pulse spectrum of the radar and causing it to be irrelevant. This means that a HVPS for a radar may require a specific switching frequency. To accommodate modern radar requirements, HVPS's capable of greater than 1 MHz switching frequency are necessary. The only practical way to operate a HVPS at this frequency is to use one of the resonant topologies [1]. The great difficulty with this approach is that most resonant converters operate by using a variable switching frequency, becoming unsuitable for this application. This dilemma motivated the invention of a device which can provide regulation over the output voltage or current in a resonant converter at a fixed switching frequency. This device together with its application to resonant power processing is treated in the following chapters in the general context of the DC-to-DC converter. The high voltage aspects of this problem are discussed in an example application of this technique of power processing.

Organization of the Thesis

The following chapters are broadly divided into two parts. Part I deals with the development of the resonant DC-to-DC converter and its steady-state operation. Chapter 2 begins with a discussion of several types of converters all of which regulate the output variables by using a variable switching frequency. The design and operating characteristics of these converters is presented for the case of steady-state operation. The magnetic regulator is introduced and analyzed in Chapter 3. The analysis reveals that the magnetic regulator is similar to a conventional transformer with a leakage inductance that is proportional to the current in an auxiliary control winding. In Chapter 4 the magnetic regulator is combined with the DC-to-DC converters developed in Chapter 2 to yield a new, efficient method of processing power at a fixed switching frequency.

Before a practical power supply can be built, a method for the regulation of the output voltage must be designed. This regulation requires that a dynamic model of the power supply be used to design a suitable compensation network which will render the closed-loop feedback system stable. Part II of this thesis focuses on this problem in the case of the resonant converter with a magnetic regulator. Since the magnetic regulator is new, Chapter 5 is devoted exclusively to developing a model for this device in a carefully controlled experiment.

The complete model of the resonant power supply with the magnetic regulator is complex, so the development of this model follows several steps. In Chapter 6, the resonant inverter and the rectifier circuit are modeled very simply and the magnetic regulator is included into the model. This chapter makes several restrictive assumptions about the inverter and rectifier which are not well satisfied in practice. This investigation is useful to gain insight into the operation of the complete power supply. Chapters 7 and 8 relax these assumptions resulting in more complete and realistic models for the power supply. In Chapter 7 the inverter switches are treated as a stiff voltage source with the focus on a complete rectifier model. This model predicts some of the behavior of the complete power supply, but the inverter model precludes the calculation of the input impedance or the input-output transfer function. Chapter 8 completes the model development of the inverter and provides predictions of the dynamic performance of the input impedance, output impedance, control-to-output and input-output transfer functions. In each of the chapters, the model predictions are compared to experimental data from one of the applications discussed in Chapter 4.

During the course of the model developments, intermediate results were often checked by using the circuit simulation program SPICE. Several of the quantities predicted by the models are inaccessible or difficult to measure in the practical hardware. In these cases as well as others, the computer simulation proved to be a valuable tool to confirm the validity of the analytical models. Often computer modeling is considered only when a very complex design must be evaluated prior to entering production. The work here illustrates how computer modeling can play a significant role in the analytical stages of a circuit's design.

Nonetheless, in the use of computer modeling, it is very important to maintain a healthy skepticism regarding the results. The computer program will only account for the effects explicitly included in the model and even then can actually produce incorrect results. It is common that a complex computer model will not converge to a solution. In this case the user knows not to trust the answer because none exists. It is also possible for the computer to return results which look reasonable at first glance, but are incorrect. Modern simulation programs often fool the user into thinking the answers are absolute by hiding the error controls inside obscure menus which the novice user never sees. These error controls place limits on the numerical errors associated with the circuit simulation, and an inappropriate choice of values of these error controls can make a solution invalid.

Power supplies pose a difficult problem for SPICE since the time constants associated with the model are widely separated. It is not unusual for a power supply simulation to have output filter dynamics with time constants less than 100 Hz, but at the same time the switching transistors may have dynamics in the 100's of MHz. Through the course of the thesis, the models in which SPICE can be useful are demonstrated as are the places where the computer model is inappropriate.

While computer simulations are helpful tools, the final result of the thesis is an analytical model of the DC-to-DC converter with the magnetic regulator as the control element. The solution of this model is difficult using hand computations; therefore, a computer is used to plot the final results. The model is based on equivalent circuits which reduce all the nonlinearities to voltage and current sources, so the usual methods of circuit analysis can be used to work out the consequences of the models. While a specific topology is used in the model development, the nature of the model readily accommodates modifications to the basic circuitry.

Part I

The Steady-State Solution

Chapter 2

Resonant DC-to-DC Converters of Conventional Design

Introduction

This chapter will introduce a family of switching DC-to-DC converters that are suitable for operation at high switching frequencies (> 500 kHz). The motivation for operation at such high switching frequencies comes from several factors:

1. The energy-storage capacitances are smaller in value, volume, and mass at higher switching frequencies. The magnetic components are also smaller in value but may not be smaller in mass or volume due to large core losses and skin effects in the conductors.
2. The switching noise in some applications can be more readily tolerated if it is known to occur at a specific frequency such as the frequency of a master clock in a digital communications system. Often this master clock frequency is higher than the optimal switching frequency of the power supply.
3. Resonant operation may make certain kinds of switching devices practical for the main switch since it is possible to arrange zero switch current at turn-off. Devices such as SCR's fit into this category.
4. In converters with high conversion ratios, the parasitics associated with the main transformer may force the circuit to operate as a resonant converter

even if the intended design is non-resonant (this often occurs in high voltage designs).

5. Capacitively-coupled voltage multipliers can replace high voltage transformers in high voltage power supplies thus greatly reducing cost, weight, and volume and increasing reliability.

For these reasons, the high-frequency resonant DC-to-DC converter is of considerable interest.

One approach to the problem of the high-frequency resonant converter is to use a quasi-resonant converter, derived from a parent pulse-width-modulated converter (PWM). These converters are especially attractive since the parasitics associated with the switching elements may be absorbed into the natural topology of the circuit. This approach has been explored thoroughly by other authors [2].

A second family of high-frequency converters are the full resonant converters such as the parallel and series resonant converters [3]. These converters can operate efficiently when faced with the non-idealities associated with high voltage transformers [4] and therefore satisfy one of the requirements of interest; however, neither the series resonant nor the parallel resonant converter account for the possibility of parasitic capacitance in parallel with the main power switch. Since the high frequencies discussed here almost always necessitate the use of power MOSFET switches which have very large shunt capacitances, any topology which does not inherently account for the shunt capacitance may be subject to large switching losses and inefficiency. (If the voltage across the switch is not zero at the instant the switch closes, the shunt capacitance will be dissipated in the switch according to $CV^2f/2$ where f is the switching frequency. At high switching frequencies, this loss is intolerable.)

The family of converters that are of interest in this work are those which use a suitable zero-voltage-switched (ZVS) DC-to-AC inverter such as the Class E [5] or Class D ZVS [6] circuit together with a suitable rectifier [7] or [8]. The elements of a suitable rectifier will be explained below. In this family of converters it is convenient to separate the problem into that of the inverter and that of the rectifier. In this way, a large number of DC-to-DC converters can be synthesized using various inverters and rectifiers in combination. This chapter will reference several key relationships for the Class E converter from the literature and then use similar methods to develop those same relationships for the Class D ZVS converter. These latter relationships have not been previously published.

After the development of the inverter circuits, the resonant rectifier will be addressed. First, the conditions for any rectifier to be compatible with its source of energy will be discussed briefly. The bridge rectifier with a capacitive input filter will then be examined and its salient features identified. Finally, the inverter and rectifier will be combined into a complete DC-to-DC converter and the steady-state operating conditions will be established. This step is a prelude to both the development of the new fixed-frequency DC-to-DC converter in Chapter 4 and the dynamic model of this family of resonant converters in Part II of the thesis.

2.1 The Resonant Inverter

The inverter portion of the circuit is responsible for the conversion of the input DC power into high-frequency AC power which can then be used by the rectifier circuit directly or transformed to lower or higher voltage using a transformer. This conversion is necessary since it is impossible to regulate DC power without power loss in dissipative elements. By using reactive elements in an AC circuit, it is possible to regulate power flow without the use of dissipative elements.

2.1.1 The Class E Circuit

One circuit well suited to this application is the Class E circuit shown in Fig. 2.1. This circuit was originally invented as a high efficiency alternative to the Class C RF power amplifier [5]. Since the circuit was intended for use in RF applications, the circuit is capable of efficient operation well into the megahertz region.

Circuit Description

The Class E circuit operates in ZVS mode if the components C_1, C_2, L_1, and the drive to MOSFET Q_1 are properly chosen. The drive duty cycle may be other than 50%, but this is the most common choice. The inductor L_{RFC} is chosen to be large compared to the other impedances in the circuit and therefore can be modeled as a constant-current input source. The value for C_2 must be selected to be larger than the shunt capacitance of MOS-

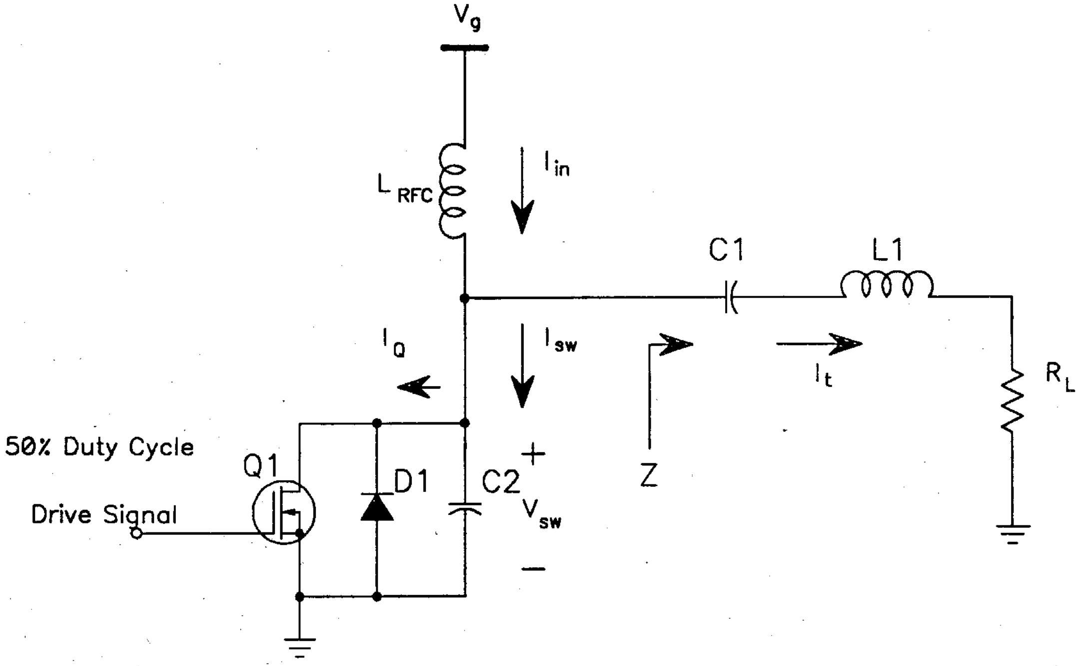


Figure 2.1: The Basic Class E Inverter. This circuit can operate at high efficiency because the main power switch closes when V_{sw} is zero. The input drive may have a duty cycle other than 50%.

FET switch Q_1 in parallel with antiparallel diode D_1 since C_2 represents the total capacitance at V_{sw}. (The capacitance of the MOSFET and diode in Fig. 2.1 has been absorbed into C_2.) The choice of the tank components, C_1 and L_1, is a trade-off between low harmonic distortion on the tank current and high voltage stresses on the components. The resonant frequency of C_1 and L_1 is chosen to be below the switching frequency of Q_1, and the resonant frequency of C_1 in series with C_2 (= C_s) together with L_2 is chosen to be above the switching frequency. If $f_1 = \sqrt{C_1L_1}$ and $f_2 = \sqrt{C_sL_1}$, the tank current rings at a frequency f_1 when Q_1 or D_1 is on, and at a frequency f_2 when both are off. If C_2 is much larger than C_1, then f_1 and f_2 are nearly the same and the current in the tank current closely resembles a true sine wave. On the other hand, if C_1 is larger than C_2, the two frequencies are substantially different, and the waveform in the tank circuit is distorted. This will have consequences in the rectifier circuit which will be described below. Since the inverter will be designed for a specific power level, the choice of the value for C_1 will not change the current in it and therefore the larger its value, the lower will be its peak voltage stress. The applied voltage stress on the tank circuit components and the distortion of the tank current are the major trade-offs that must be made in this inverter's design. A quantitative design procedure for the Class E inverter may be found in [5]. The waveforms in an idealized Class E inverter are shown in Fig. 2.2. These waveforms occur if the tank current I_t is assumed to be a sine wave. The voltage across the switch, V_{sw}, rises when Q_1 turns off then returns to zero at which point the diode D_1 conducts. The MOSFET turns on again while the current I_Q is either negative or zero thus achieving zero-voltage-switching.

The waveforms in an actual converter can be significantly different from those shown in Fig. 2.2. Figure 2.3 is an example of the waveforms obtained in actual practice. The waveforms shown are from a SPICE simulation which accounts for the non-sinusoidal current that results when the true inverter topology is used. Even though the actual wave-

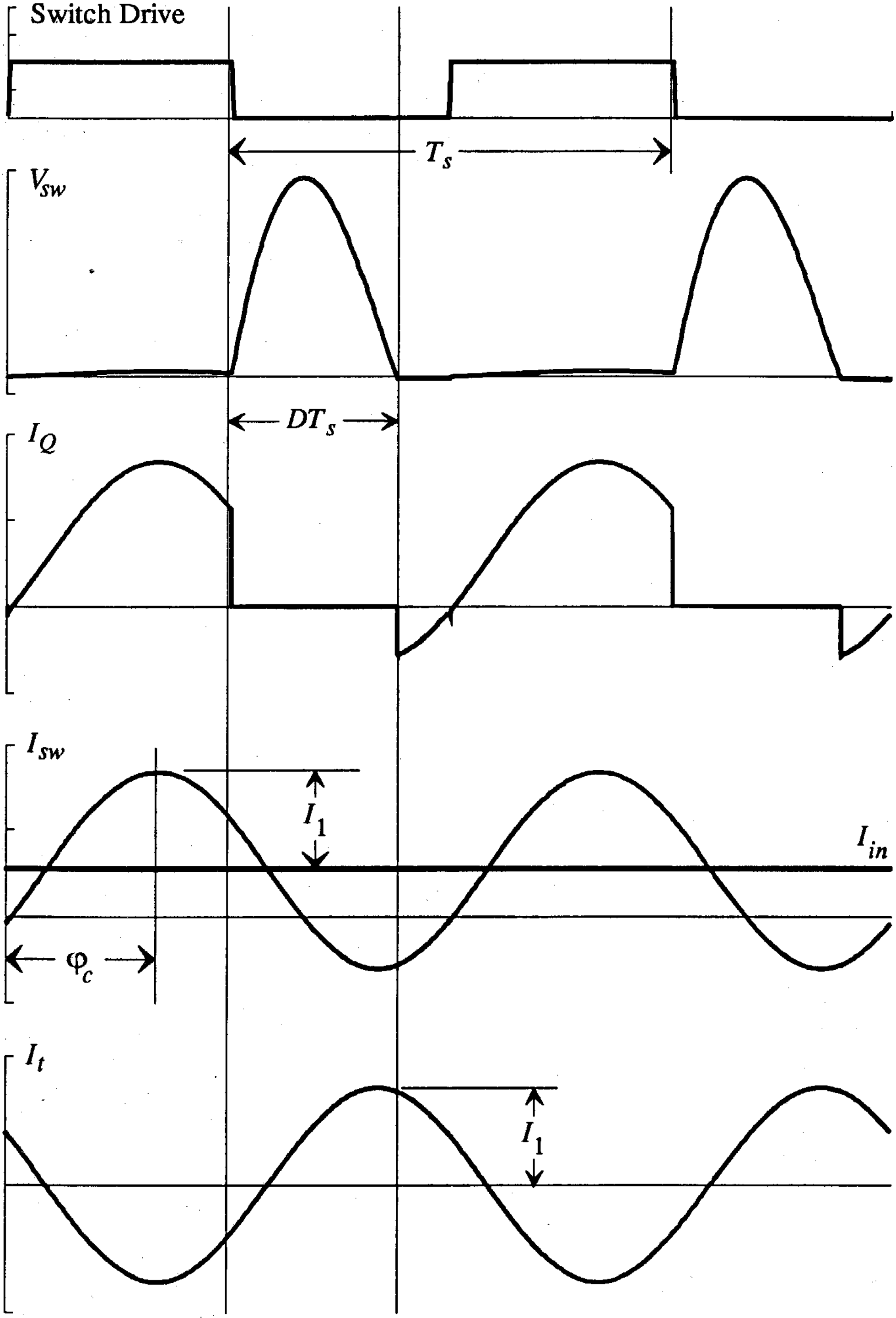


Figure 2.2: Waveforms in an Idealized Class E Inverter. The assumption that the tank current (I_t) is a sine wave makes the analysis of this circuit tractable.

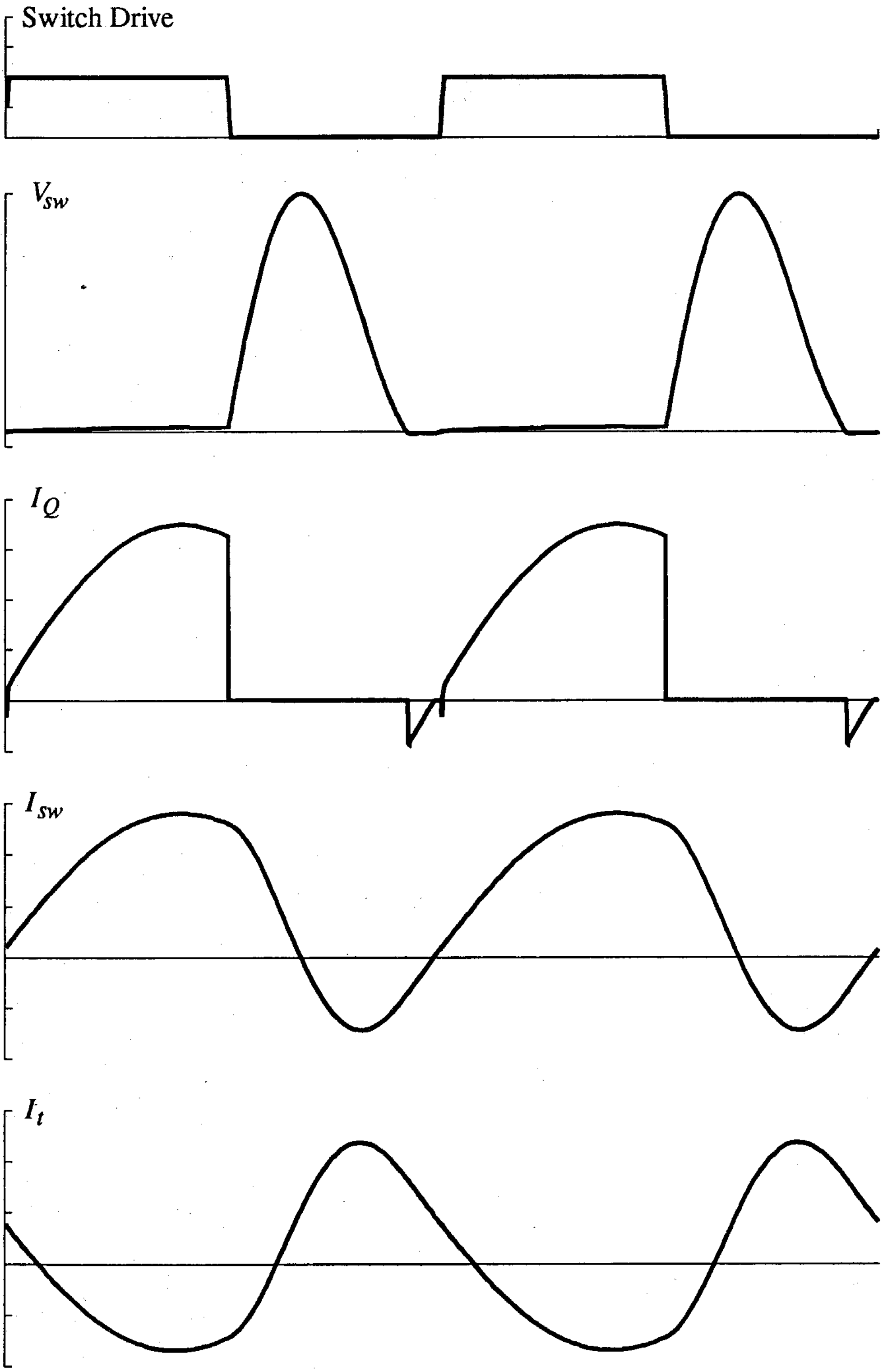


Figure 2.3: Waveforms in a Nonideal Class E Inverter. This SPICE simulation accounts for the true nature of the inverter tank current, I_t.

forms in the Class E circuit are distorted, the assumption of a sinusoidal tank current is analytically useful.

Analysis

One of the important limitations of the Class E inverter is that the voltage applied to the switch is much larger than the DC input voltage. Since the input voltage is connected to the switch through an inductor, the average voltage applied to the switch must equal the DC input voltage. Therefore, if the switch duty cycle is small, the peak voltage applied to the switch is large. An approximate formula for the maximum switch voltage is [9]:

$$V_{MAX} = \frac{1.65V_{DC}}{D} \tag{2.1}$$

In a typical case, the switch duty cycle is 35% which implies that the maximum voltage applied to the switch is 4.7 times the DC input voltage. This fact limits the Class E inverter to low voltage, low power applications.

The design of the Class E inverter amounts to selecting the proper components to achieve ZVS for a given load. This problem has been solved in many papers, and one which is particularly useful is [9]. The problem is solved by defining a normalized load impedance, $z'_y = z_y/X_{C_2}$, as shown in Fig. 2.1 and then plotting the locus of z'_y which results in ZVS operation. This analysis will not be done here but a similar analysis for the Class D ZVS inverter will be presented in the next section. The region in the z'_y plane which results in lossless switching is shown in Fig. 2.8 (b). The use of this plot will be deferred until after the resonant rectifier load is discussed.

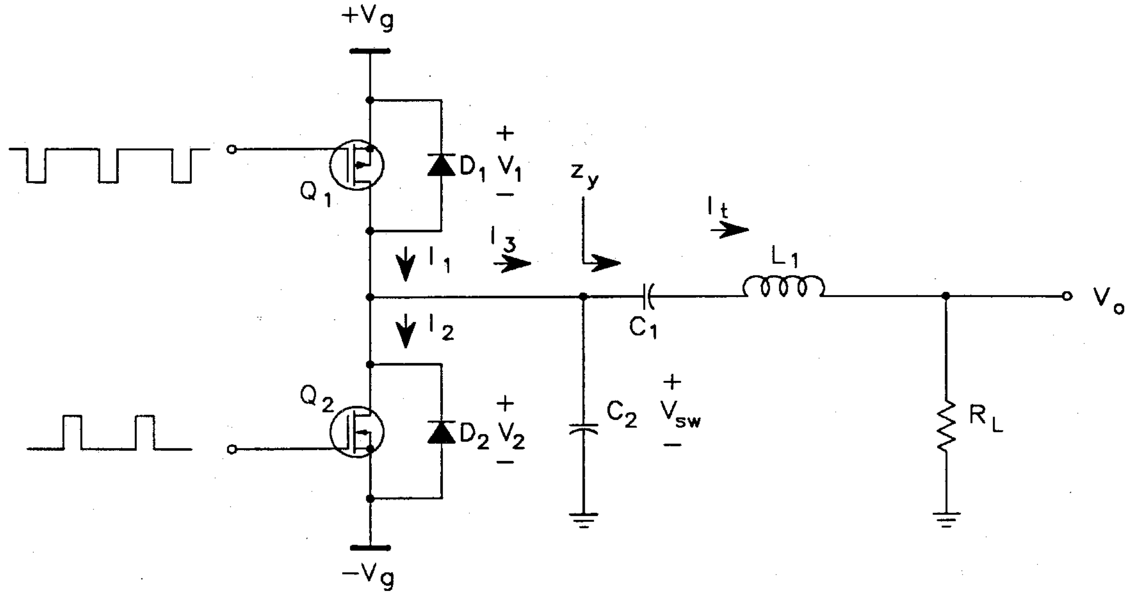


Figure 2.4: Basic Class D ZVS Inverter. The drives for Q_1 and Q_2 are interlaced with some dead time.

2.1.2 The Push-Pull Circuit

The Class E inverter examined in the previous section has a serious disadvantage: the voltage applied to the power switch is many times larger than the DC input voltage. This restricts the use of this topology to low voltage and low power applications. An alternative topology which has better switch utilization is the Class D ZVS circuit. A typical example of this topology is shown in Fig. 2.4. In this circuit the voltage across the power switches never exceeds the power supply rails (i.e., each switch will see $2V_g$ maximum).

Circuit Description

The Class D ZVS circuit consists of two MOSFET switches and two antiparallel diodes arranged in a totem pole configuration driving a resonant circuit with a shunt capacitor at the input. The purpose of the capacitor is to account for the output capacitance of the MOSFETs and the junction capacitance of the diodes. The MOSFETS are driven with a non-overlapping drive signal which alternately turns on each switch for some duty cycle which must be less that 50%. Figure 2.5 shows the basic waveforms associated with Fig. 2.4. The waveform V_{sw} shows the voltage across the capacitor C_2. At time t_2, Q_1 is turned on just as the voltage across Q_1 is approaching zero. The voltage remains near zero as long as Q_1 is on. When Q_1 is turned off, the current in the tank circuit charges capacitor C_2 toward the lower supply rail. (The voltage across C_2 was equal to the upper supply rail while Q_1 was on.) The voltage on C_2 must be at the lower supply rail prior to the turn-on of Q_2 to achieve the zero-voltage-switching condition. Normally, the antiparallel diode D_2 will conduct briefly before Q_2 is switched on. At the moment when Q_2 closes (t_3), the voltage across Q_2 will be zero since $V_{sw} = -V_g$ as shown in the fig 2.5. The narrowband nature of C_1 and L_1 will select out the fundamental of the waveform V_{sw}. In most high-frequency applications the transition time of V_{sw} is substantial, so the drive duty cycle to each of the switches is well below 50%, typically around 25%. Note the phase shift between the current in the tank circuit, I_t, and the voltage into the tank circuit, V_{sw}. The voltage is leading the current which implies the impedance looking into the tank circuit and the load is inductive. This is one of the necessary conditions for ZVS. Only certain values of the load impedance can be tolerated. The possible failures of the circuit to operate in the ZVS mode are illustrated in Fig. 2.6. If the tank current is too small or has too much phase lag, then the voltage across C_2 will not charge to the opposite rail before the closure of the power switch (Fig. 2.6 (a)). The jump in this waveform is indicative of large switching loss. If the current is large enough to charge C_2 but leads the proper phase angle by too much, then the current in the diode reverses and the voltage across the switch pulls away from the supply rail. When the switch closes, C_2 will discharge into the switch again resulting in switching loss and inefficiency.

Analysis

The design of the Class D inverter amounts to choosing values for the components C_1, C_2, and L_1 that will result in the ZVS mode of operation for a given load impedance. The

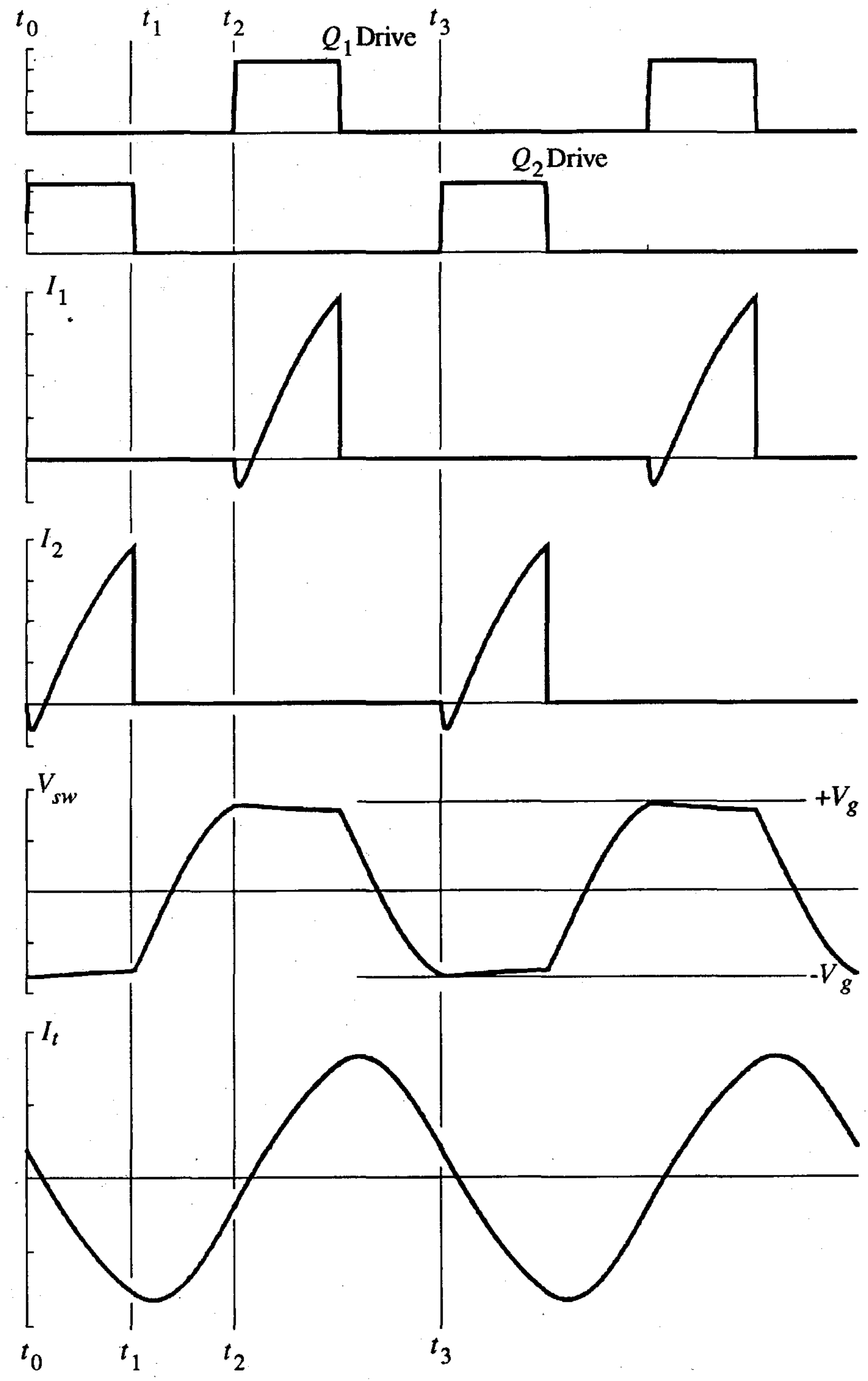
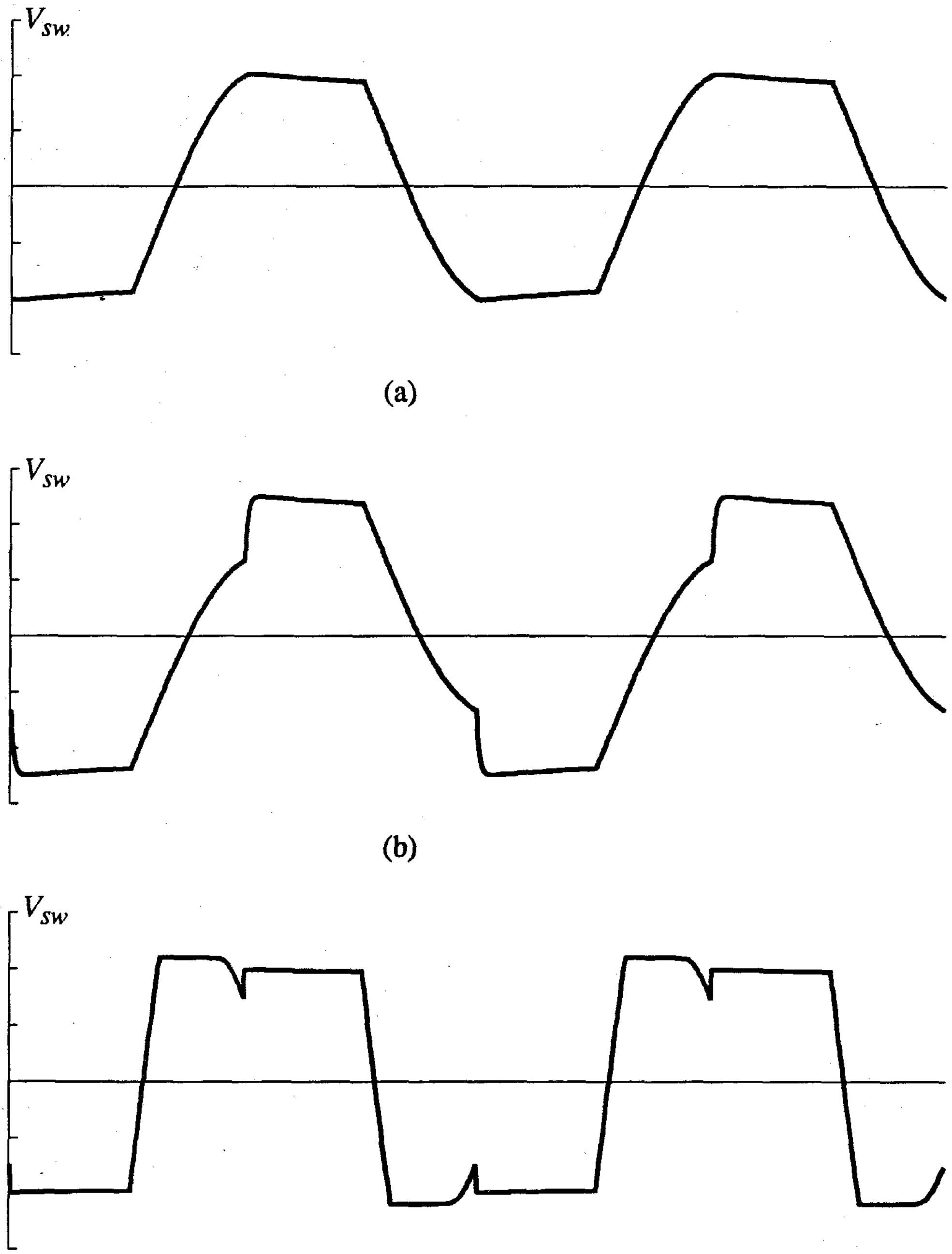


Figure 2.5: Basic Waveforms in the Class D ZVS Inverter. The load components and the drives are chosen so that the voltage across either switch is zero at turn-on (times t_2 and t_3).



(a)

(b)

(c)

Figure 2.6: Class D ZVS Inverter Waveforms. The waveform V_{sw} is shown in proper ZVS mode (a). In (b) the tank current is insufficient to charge C_2 to the opposite supply rail. In (c) the tank current has too much phase lead ahead of the switch drives.

impedance z_y in Fig. 2.4 must be chosen to provide the proper magnitude and phase for the tank current. The analysis of this circuit closely parallels that in [9], which solved the same problem for the Class E circuit.

The first condition for lossless switching is for the current into capacitor C_2 to charge it from one supply rail to the opposite supply rail. (Refer to Fig. 2.7 for the waveforms and notation used in the following analysis.) The charge required to do this is illustrated in the figure by the shaded area under the I_{C_2} curve. Lossless switching will occur if:

$$\Delta V_{sw} \geq 2V_g \quad \text{(rising edge)}$$
$$\Delta V_{sw} \leq -2V_g \quad \text{(falling edge)}$$

Because of the symmetry of the circuit, either condition is equivalent so consider the falling edge:

$$\Delta V_{sw} = -\frac{1}{\omega C_2} \int_{\pi D}^{\pi D + \Gamma} I_t(\theta)\, d\theta \tag{2.2}$$

where ω is the angular frequency of the drive signal. The tank current I_t is

$$I_t = i_t \sin(\theta - \phi) \tag{2.3}$$

Carrying out the integration and simplifying the result gives

$$\Delta V_{sw} = \frac{i_t}{\omega C_2} [\cos(\pi D + \Gamma - \phi) - \cos(\pi D - \phi)] \tag{2.4}$$

For the common case of $D = 0.5$, (i.e., each switch on for 25% of the *total* switching cycle) 2.4 becomes

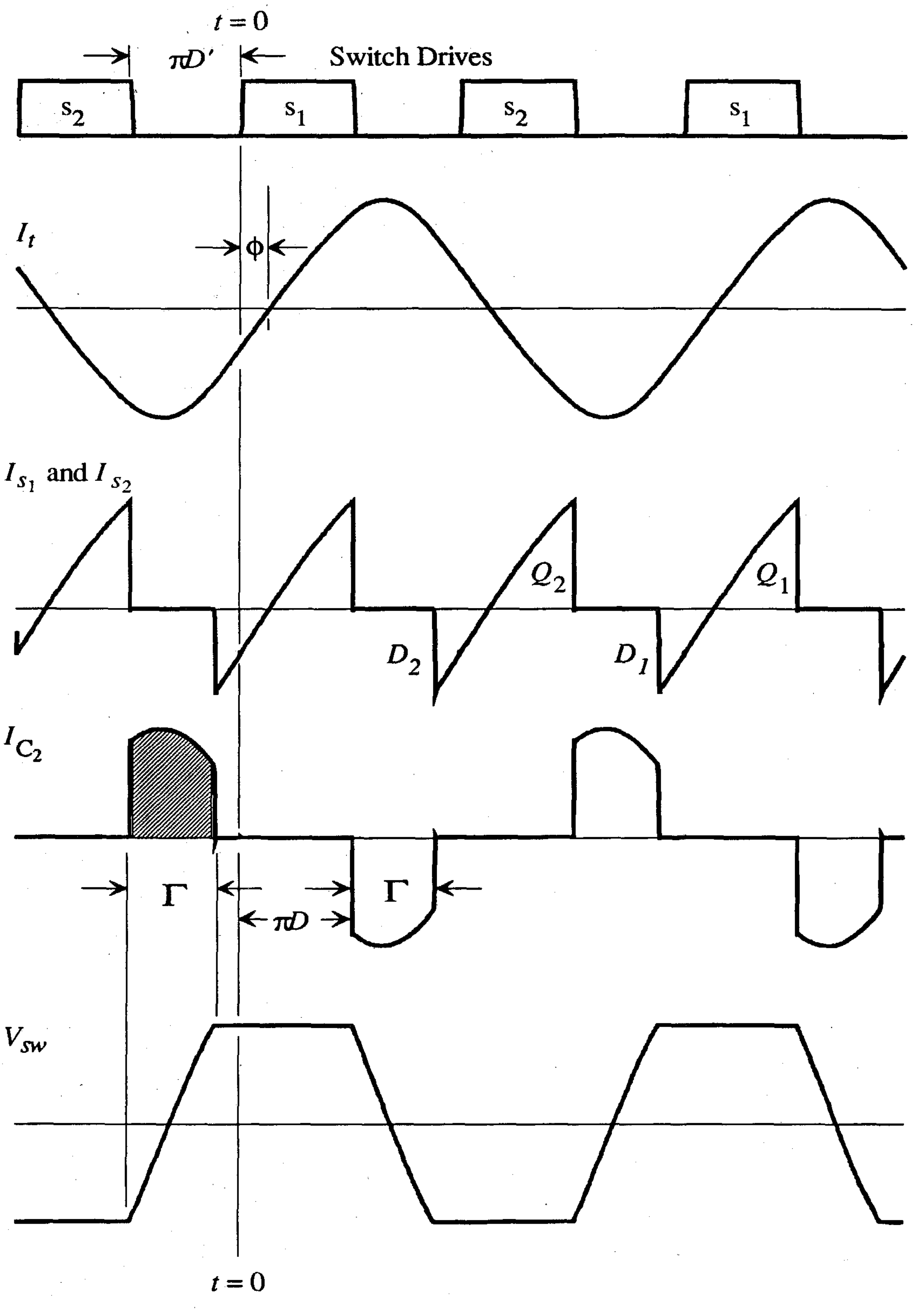


Figure 2.7: Waveforms used in the Analysis of the Class D ZVS Converter. The switches refer to the parallel combination of a MOSFET and antiparallel diode.

$$\Delta V_{sw} = \frac{i_t}{\omega C_2}\left[-\sin(\Gamma-\phi)-\sin\phi\right] \tag{2.5}$$

At the boundary of ZVS, $\Delta V_{sw} = -2V_g$ which implies

$$\frac{2V_g\omega C_2}{i_t} = \sin(\Gamma-\phi)+\sin\phi \tag{2.6}$$

The next step is to calculate z_y in Fig. 2.4. A clever method used in [9] is to calculate the fundamental of the current in C_2 and then calculate the voltage across C_2 from the result. The impedance z_y is equal to the fundamental of the voltage across C_2 divided by the current in the tank circuit, I_t. The fundamental of the current in C_2 is

$$\begin{aligned} I_{tF} &= \frac{1}{\pi}\int_0^{2\pi} I_{C_2}(\theta)\,e^{-j\theta}d\theta \\ &= \frac{1}{\pi}\int_{\pi D}^{\pi D+\Gamma}(-I_t)\,d\theta + \frac{1}{\pi}\int_{\pi+\pi D}^{\pi+\pi D+\Gamma}(-I_t)\,d\theta \end{aligned} \tag{2.7}$$

Equations 2.3 and 2.7 give:

$$I_{tF} = \left(\frac{e^{j(\phi-2\pi D)}}{2\pi}(1-e^{-j2\Gamma}) + \frac{e^{-j\phi}\Gamma}{j\pi}\right)i_t \tag{2.8}$$

The fundamental of the capacitor voltage can now be obtained easily by using $V_{C_2} = -jX_{C_2}I_{tF}$. The fundamental of the tank current is

$$
\begin{aligned}
I_{tF} &= \frac{1}{\pi}\int_{0}^{2\pi} i_t \sin(\theta - \phi)\, e^{-j\theta} d\theta \\
&= -j i_t e^{-j\phi}
\end{aligned}
\tag{2.9}
$$

The normalized impedance z'_y is:

$$
z'_y \equiv \frac{z_y}{X_{C_2}} = \frac{V_{C_2}}{X_{C_2} I_{tF}} = \frac{1}{\pi}\left[j\Gamma + \frac{e^{j2(\phi - \pi D)}}{2}\left(e^{-j2\Gamma} - 1\right) \right] \tag{2.10}
$$

In the special case of $D = 0.5$, this simplifies to,

$$
z'_y = \frac{1}{\pi}\left[j\Gamma - \frac{e^{j2\phi}}{2}\left(e^{-j2\Gamma} - 1\right) \right] \tag{2.11}
$$

To map the region of lossless operation, the acceptable values for ϕ and Γ must be determined. One condition for lossless operation is that the voltage across C_2 transitions from $+V_g$ to $-V_g$ before the switch closes. This is equivalent to $0 \le \Gamma \le \frac{\pi}{2}$. It is necessary to maintain positive or zero forward current in the diodes prior to the switch closure. This will occur so long as $\phi \ge 0$. These conditions define the boundary of the ZVS region in the z'_y plane. To trace the locus of the boundary, set $\Gamma = \pi/2$ and sweep ϕ from zero upward and set ϕ = zero and sweep Γ across its range. The resulting region is plotted in Fig.2.8 (a) together with a similar region corresponding to the Class E circuit from [9] in Fig. 2.8 (b). It is clear from the figures that only inductive loads will provide lossless switching in either the Class E or Class D ZVS inverter.

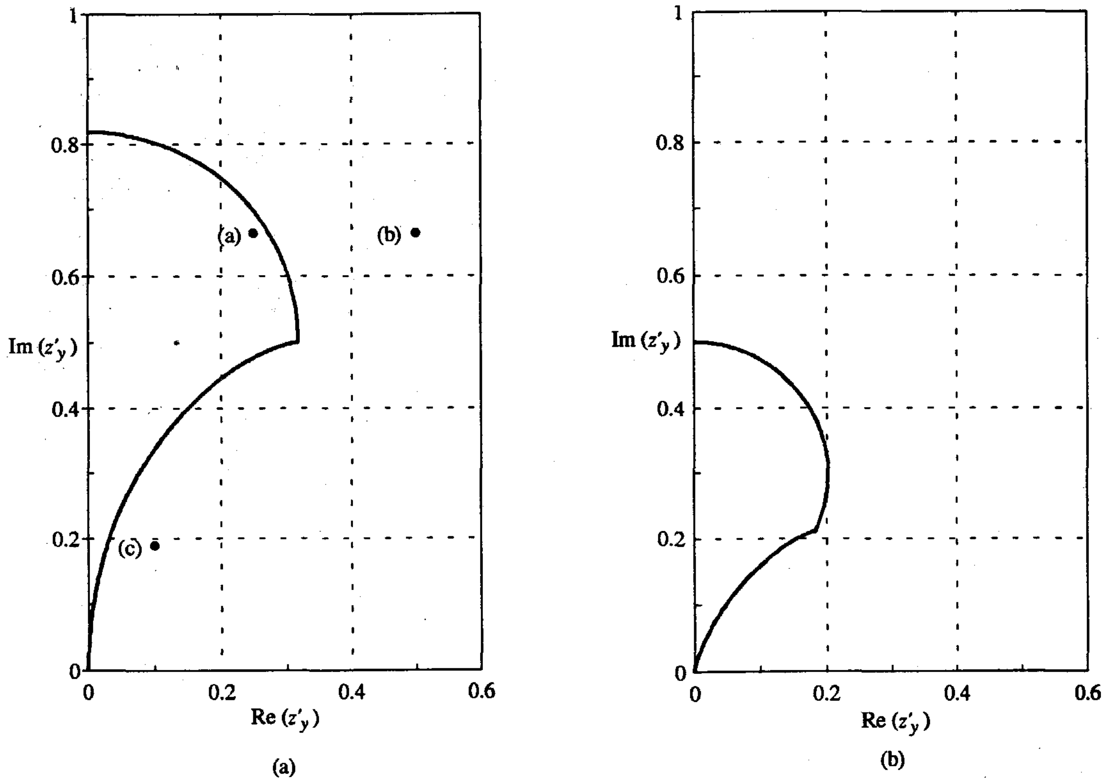


Figure 2.8: Region of Lossless Operation of the Class D ZVS Inverter (a) and the Class E Inverter (b). The points plotted in (a) correspond to the waveforms shown in Fig. 2.6. Points (b) and (c) are outside the lossless region and therefore have large switching losses. The point (a) is inside the region and has no switching loss.

2.2 The Resonant Rectifier

Rectifier circuits are some of the most common circuits in all of power electronics and the most often neglected. This section is concerned with the conditions necessary for a rectifier and its source to be "compatible." What compatibility means in this context is that the rectifier and the source function together without causing any impulsive voltages or currents. The reason this compatibility is desirable is that the presence of impulsive voltages or currents inevitably leads to power loss and electromagnetic interference. The former problem is due to the fact that an impulse has an average to RMS ratio which approaches zero as the width of the pulse approaches zero. In the mathematical limit, this means that the power loss in the interconnections of a circuit which contains impulses will consume all the available power, with none left for the load. This point is best illustrated with a simple example. Consider the *RC* circuit in Fig. 2.9. The resistance R represents a small parasitic resistance in the branch of a circuit with an impulsive current which feeds a capacitor filter and resistive load R_L. The current source at the input provides rectangular pulses of current whose amplitude is I_0/D and whose width is DT_s. T_s is the period of the current pulse train. This input current has an average value of I_0 independent of the value of D. Therefore, if the capacitor is large, the output voltage will be mostly DC equal to $R_L I_0$. The output power into the load is $P_o = I_0^2 R_L$. The input pulse train is assumed to be very narrow so that the input voltage to the circuit is much larger than the output voltage. In this case the input power is $P_i = (I_0/D)^2 \cdot R \cdot D$. The efficiency of this circuit is $\eta \equiv P_o/P_i = (DR_L)/R$. As the duty cycle goes to zero, the efficiency of this circuit also goes to zero for any finite ratio of the load resistance to the parasitic resistance. In actual practice this means that circuits with impulsive currents will have poor efficiency even with good components.

The best example of an incompatible circuit is the most familiar rectifier circuit, the capacitive input rectifier used in 60 Hz applications. In these circuits, the action of the

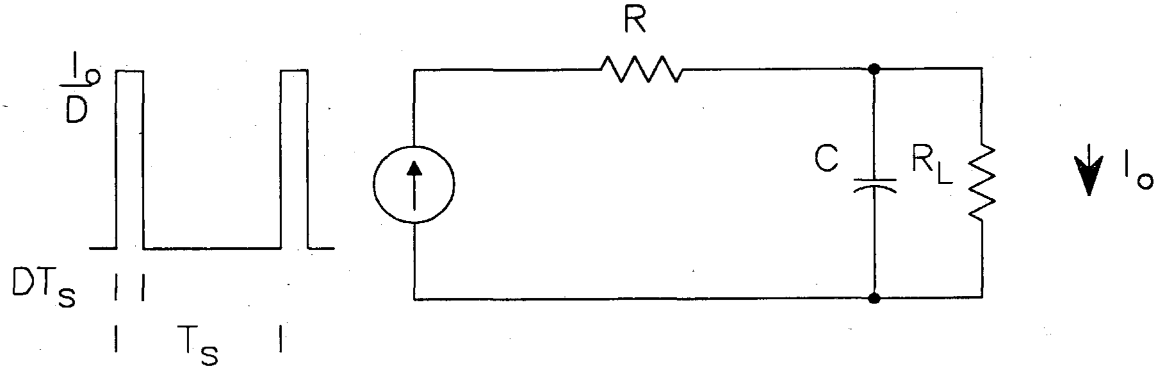


Figure 2.9: Current Impulse Applied to an RC Filter. The presence of R, no matter how small, makes the efficiency of this circuit low.

capacitor causes the currents in the input rectifier diodes to flow in narrow pulses with conduction occurring at the top of the input voltage waveform. The main problem here is the lack of compatibility; the capacitively-filtered rectifier circuit requires a *current* drive to be efficient. Likewise, the inductively-filtered rectifier requires a *voltage* drive to be efficient. Figures 2.10 and 2.11 are examples of compatible and incompatible combinations of rectifiers and sources. Any combination which results in an impulse of either voltage or current is considered incompatible.

The reason that the capacitive input filter works in 60 Hz applications is that modern diodes are designed with large peak current handling capabilities and the parasitic resistances in real circuits will limit the peak current delivered to the rectifier. Finite filter capacitance also acts to limit the width of the impulse so that some reasonable efficiency can be maintained. However, this approach fails when high frequencies are used. The diode switching losses become excessive, and consequently the diode junction temperature also becomes excessive. The appropriate design technique is to choose a rectifier topology which is inherently compatible with the source of energy. The sine wave inverters described in this chapter all function as current sources of sine waves, so the capacitive-input rectifier is the topology of choice. Several candidate rectifiers can be used, but the common bridge rectifier will be analyzed below. The analysis will follow [9] closely. (The voltage doubler circuit was analyzed in this reference.)

2.2.1 Resonant Bridge Rectifier Analysis

As discussed above, the bridge rectifier circuit is inherently compatible with the resonant inverters discussed in this chapter. However, this compatibility is somewhat limited when the locus of acceptable loads for the Class D ZVS or Class E circuit is considered as in Fig. 2.8. It is clear from the figure that only certain loads can be tolerated if the ZVS

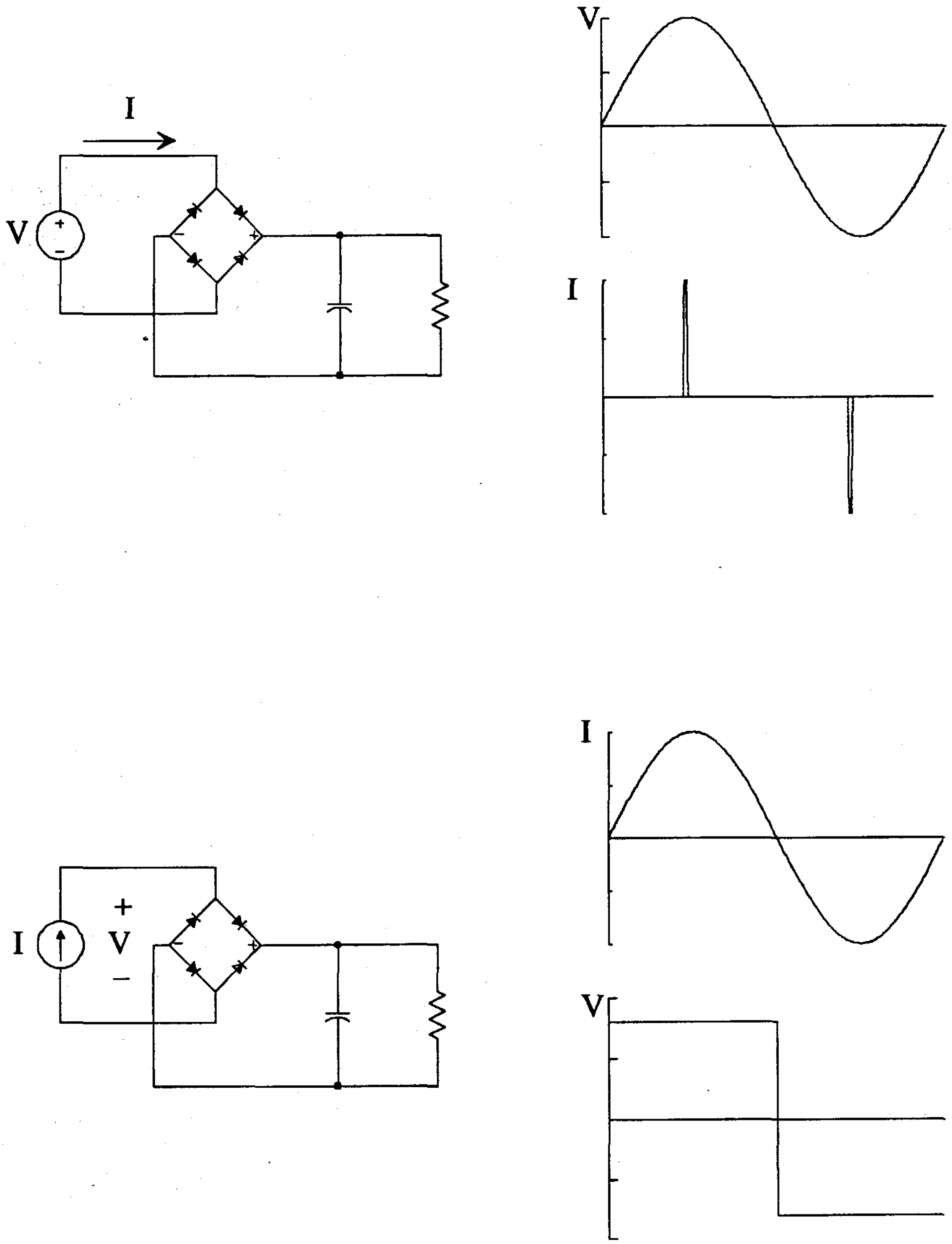


Figure 2.10: Examples of Capacitive-Input Rectifiers. The upper example is the familiar case for many 60 Hz applications. In this case, the rectifier and source are *incompatible*. The rectifier and source are compatible in the lower example.

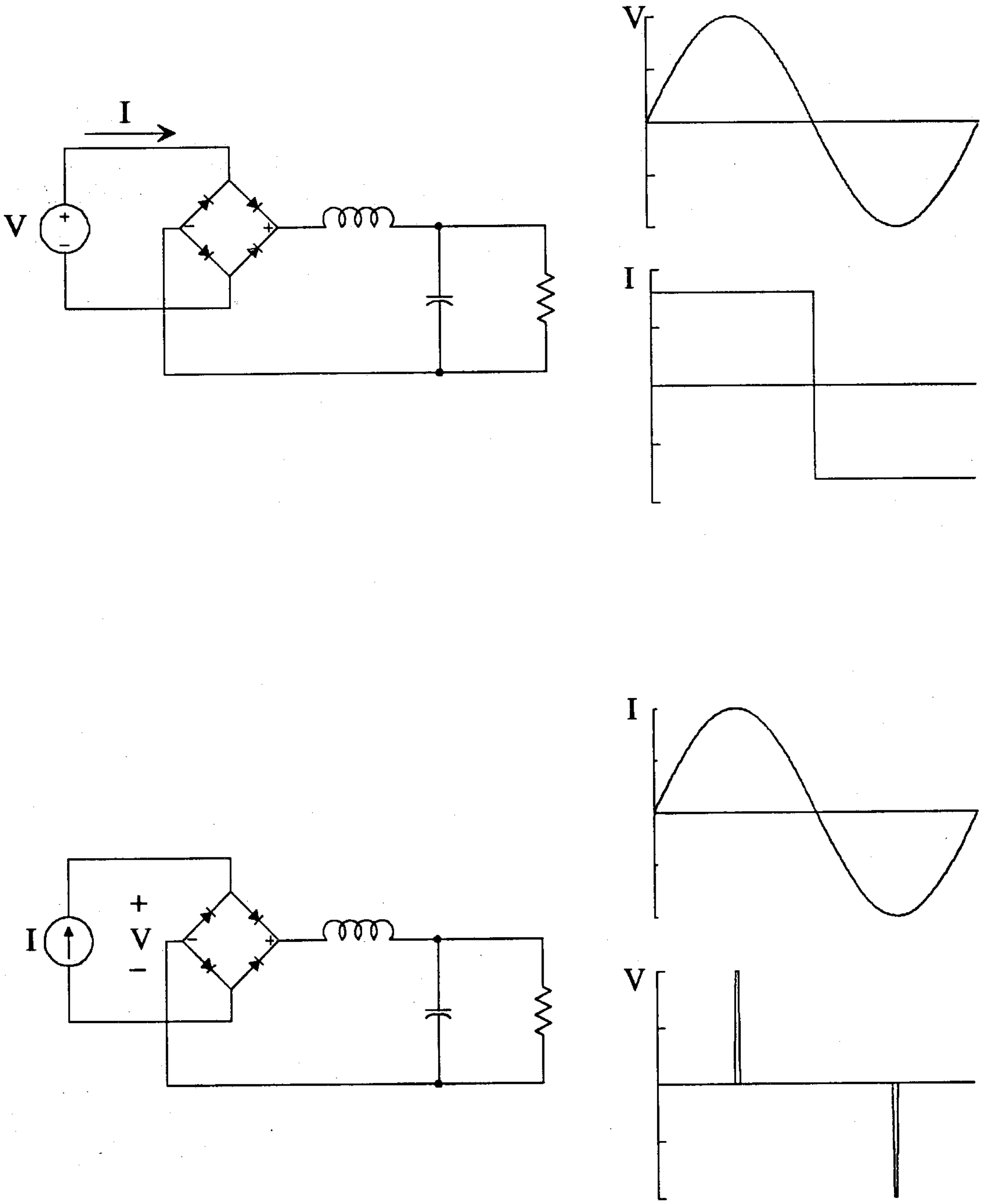


Figure 2.11: Examples of Inductive-Input Rectifiers. The upper example is commonly used for many 60 Hz applications. In this case, the rectifier and source are *compatible*. The rectifier and source are incompatible in the lower example.

condition is to be maintained. In particular, if the load resistance on the output of the bridge rectifier is removed, the input impedance to the rectifier becomes infinite which is well outside the range of acceptable loads. The input impedance to the rectifier is clearly a quantity of interest since it will determine if the overall circuit can function efficiently.

Rectifier Input Impedance Analysis

The input impedance to a bridge rectifier such as in Fig. 2.10 cannot be defined in general terms since the circuit is nonlinear. However, in a resonant DC-to-DC converter, the high impedance of the tank circuit at frequencies other than resonance means that the behavior of the load on the inverter is only important near the resonant frequency. The switching frequency of the inverter is sufficiently close to the resonant frequency of the tank circuit that the switching frequency alone may be considered in the analysis of the load. Therefore, the input impedance to the rectifier can be defined as the ratio of the fundamental of the input voltage to the fundamental of the input current. If the input current is assumed to be a sine wave of amplitude I_0, then the input voltage will be a bipolar square wave, switching between $+V_o$ and $-V_o$ where V_o is the DC output voltage (the forward voltage drops of the diodes have been neglected). Since the average input current must equal the average output current, the current into the DC load resistance is $(2/\pi)\ I_0$. The DC output voltage is therefore $(2/\pi)\ I_0 R_L$. The fundamental of a square wave with peak value V_o is $(4/\pi)\ V_o$. The equivalent AC input impedance to the bridge rectifier is

$$z_{AC} \equiv \frac{V_{\text{fundamental}}}{I_0} = \frac{8}{\pi^2} R_L \tag{2.12}$$

This impedance is purely real which means that the bridge rectifier cannot be used alone as a load on either of the inverters discussed above unless some inductance is placed in series. This is equivalent to saying that the inverter switching frequency must be above the resonant frequency of the tank circuit since at resonance the inductive and capacitive reactances in the tank circuit cancel each other out. Above resonance, some of the inductive reactance will remain which can move the load impedance into the allowable region in the z_y-plane.

Further examination of Fig. 2.8 shows that even with series inductance, there is a very limited range of load resistances that will operate acceptably on the inverter. This problem was solved in [9] by placing an inductor in parallel with the input to the rectifier. This adds a "pre-load" to the rectifier so that the load impedance does not go to infinity as the output load is removed. In addition, the inductor modifies the current into the rectifier so that the current rises slowly at first (while the diodes are experiencing reverse recovery) and then rises more quickly later in the cycle. The rectifier circuit that will be analyzed is shown in Fig. 2.12. Figure 2.13 shows the basic waveforms in this circuit. The input current to the rectifier is

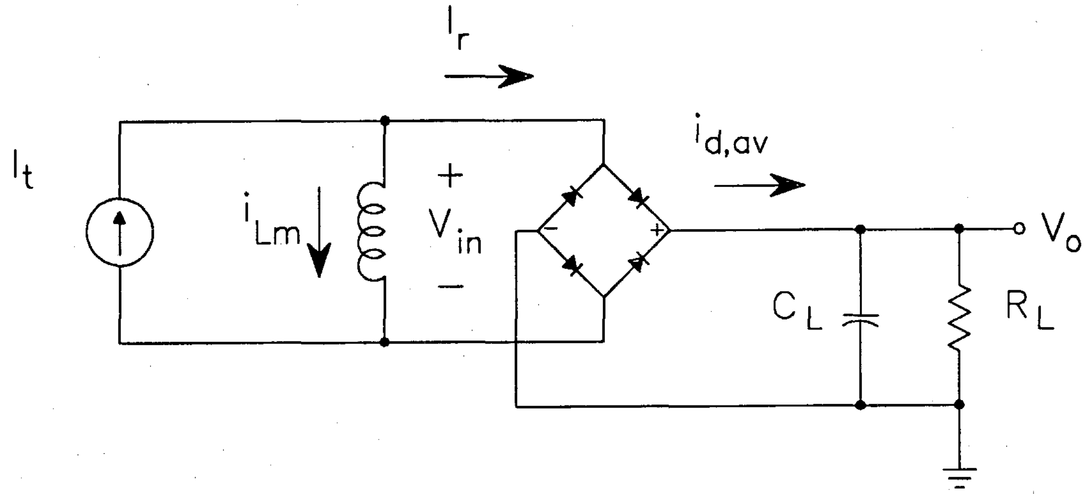


Figure 2.12: Schematic Diagram of the Resonant Rectifier Circuit. The inductor across the input acts as an impedance matching component.

$$I_t = i_t \cos\theta \tag{2.13}$$

The current in inductor L_m is (refer to Fig. 2.13)

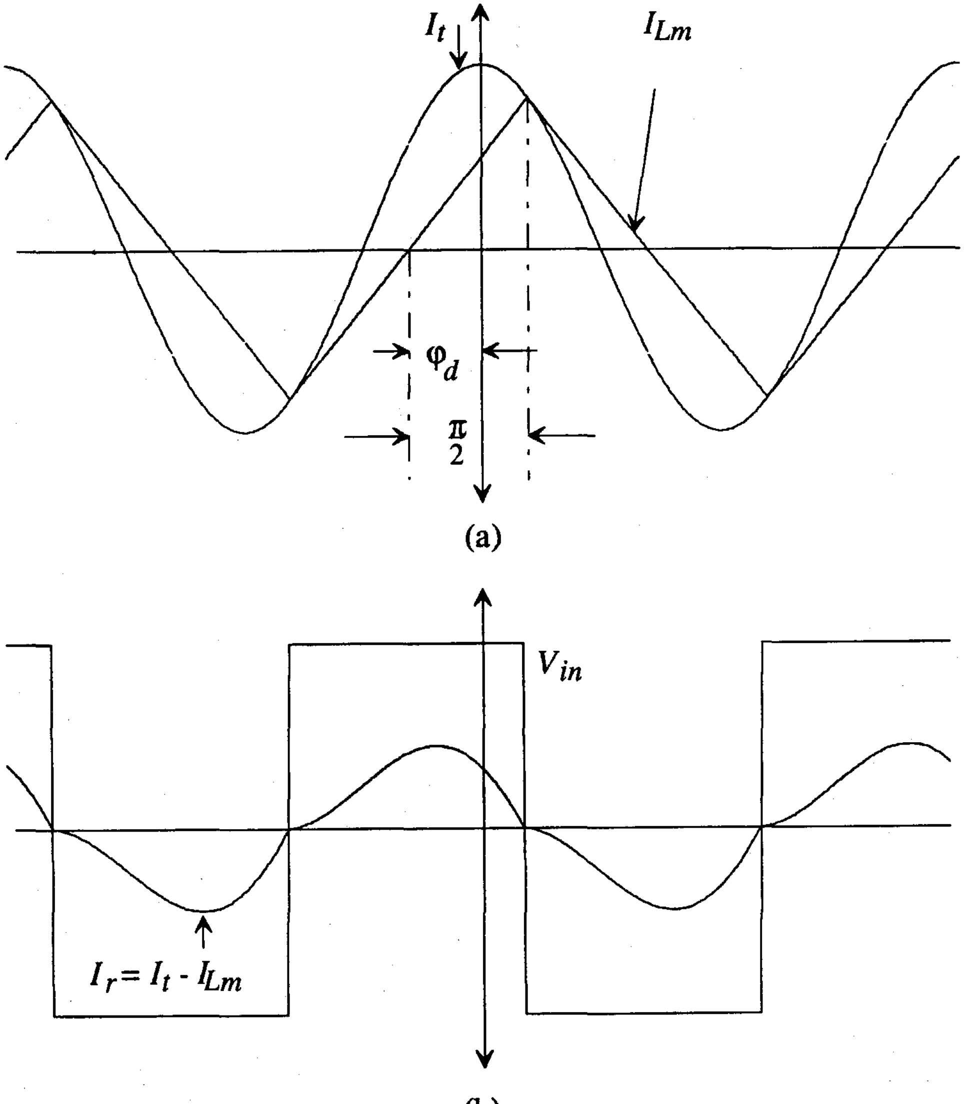


Figure 2.13: Basic Waveforms Associated with the Resonant Rectifier in Fig. 2.12. This example has relatively little load current compared to the current in L_m.

$$I_{L_m} = i_t\left(\frac{2}{\pi}\right)(\theta - \varphi_d)\,\sin\varphi_d \tag{2.14}$$

The average current out of the diode bridge is

$$i_{d,av} = \frac{1}{\pi}\int_{-\frac{\pi}{2}-\varphi_d}^{\frac{\pi}{2}-\varphi_d} (I_t - I_{L_m})\,d\theta \tag{2.15}$$

The equations 2.13 and 2.14 simplify this to

$$i_{d,av} = \frac{2}{\pi} i_t \cos\varphi_d \tag{2.16}$$

The average current out of the diode bridge equals the current into the load resistor, so

$$I_{d,av} = \frac{V_o}{R_L} \tag{2.17}$$

Therefore, the amplitude of the tank current is given by

$$i_t = \frac{\pi}{2}\frac{V_o}{R_L}\frac{1}{\cos\varphi_d} \tag{2.18}$$

From the figure, it is clear that the input voltage is a bipolar square wave with a peak amplitude of V_o. The fundamental of such a waveform is $(4/\pi)\,V_o$ with a phase shift of φ_d. The input current from 2.18 together with the input voltage fundamental define the input impedance,

$$z_{in} = \frac{\frac{4}{\pi} V_o e^{j\varphi_d}}{\frac{\pi}{2} \frac{V_o}{R_L \cos\varphi_d}} = \frac{8}{\pi^2} \cos\varphi_d e^{j\varphi_d} R_L \tag{2.19}$$

The relationship between the voltage and current in an inductor is

$$V_o = \omega L_m \frac{d}{d\theta} (I_{L_m}) \tag{2.20}$$

which together with 2.14 gives

$$\frac{V_o}{i_t} = X_{L_m} \frac{2}{\pi} \sin\varphi_d \tag{2.21}$$

Equations 2.18 and 2.21 can be used together to solve for the phase angle,

$$\tan\varphi_d = \frac{R_L}{X_{L_m}} \tag{2.22}$$

Equation 2.22 allows the input impedance to be normalized to the shunt inductive reactance,

$$\frac{z_{in}}{X_{L_m}} = \frac{8}{\pi^2} \sin\varphi_d e^{j\varphi_d} \tag{2.23}$$

This can be further simplified by using the complex form of the sine function,

$$\sin\varphi_d = \frac{e^{j\varphi_d} - e^{-j\varphi_d}}{2j} \tag{2.24}$$

which results in

$$\frac{z_{in}}{X_{L_m}} = \frac{4}{\pi^2}\left(j - je^{2j\varphi_d}\right) \tag{2.25}$$

The above derivation is valid so long as the diodes remain in continuous conduction. If the load resistance is large enough, there will be an interval when none of the diodes are on. This is the discontinuous conduction mode. The boundary between discontinuous and continuous conduction mode occurs when the inductor current slope and the input current slope are equal at the point of tangency. The point of tangency is $\theta = -\frac{\pi}{2} - \varphi_d$. If the phase associated with the boundary between continuous and discontinuous conduction is called φ_{cr}, then 2.13 and 2.14 give

$$\frac{d}{d\theta}(I_t) = \frac{d}{d\theta}(I_{L_m}) \tag{2.26}$$

$$i_t \sin\left(-\frac{\pi}{2} - \varphi_{cr}\right) = i_t\left(\frac{2}{\pi}\right)\sin\varphi_{cr} \tag{2.27}$$

$$\varphi_{cr} = \tan^{-1}\left(\frac{\pi}{2}\right) \tag{2.28}$$

A plot of the normalized input impedance is a portion of a circle in the normalized z-plane for φ_d between zero and approximately 65° (see Fig. 2.14). The impedance follows an unknown path to the point $0 + j1$ in the normalized z-plane which is the impedance when the output load is completely removed.

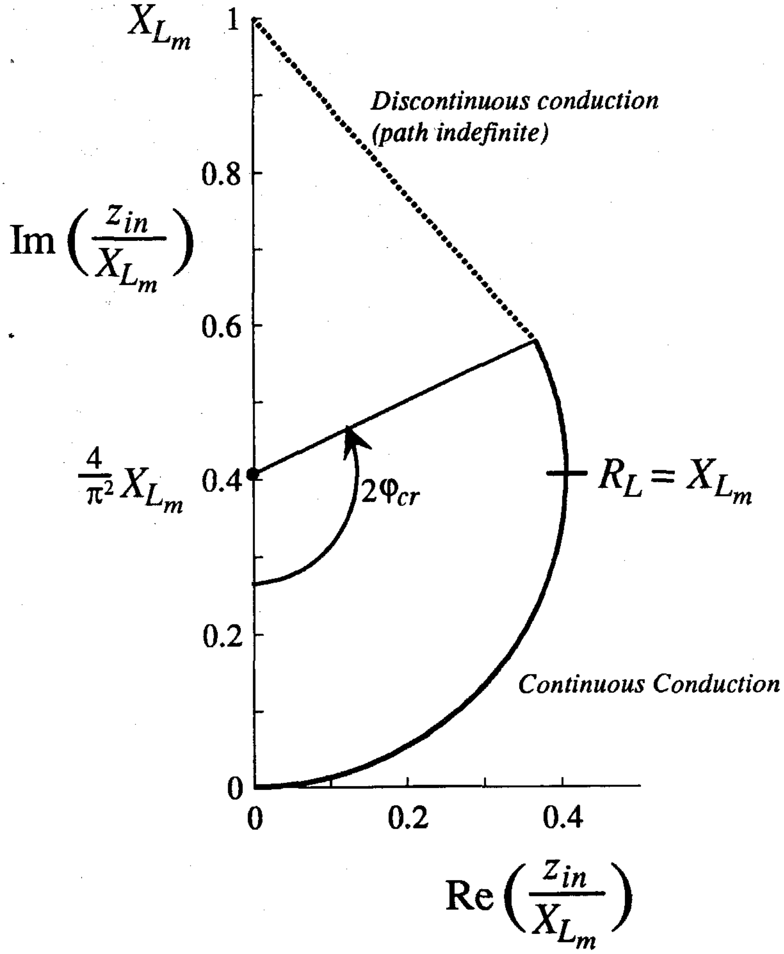


Figure 2.14: Normalized Input Impedance to the Resonant Bridge Rectifier. This plot has the same shape as in the case of the voltage doubler [9] because of the normalization. The load resistance that corresponds to the angle φ_d changes so that $\varphi_d = \pi/2$ occurs for $R_L = X_{Lm}$.

2.3 The Resonant DC-to-DC Converter

The resonant rectifier can now be combined with the inverter, and with a suitable choice of components, it is possible for the inverter to operate in the ZVS mode for all values of load resistance. Since the ZVS region for either the Class E or the Class D ZVS inverter is extremely small near the origin in the z-plane, some series inductance is necessary between the inverter and the rectifier. This is equivalent to operating the switching frequency above the resonant frequency of the tank circuit. It is convenient to break the tank circuit into an LC circuit which is resonant at the switching frequency plus whatever residual inductance remains. This inductance is termed L_{res}. The design task is to choose values for L_m, L_{res} and C_2 together with the tank circuit elements L_1 and C_1 that meet all the design goals. In the final implementation, L_1 and L_{res} will be combined as a single inductance. A few of the trade-offs in the choices for these components are as follows:

1. The smaller the value for L_m, the larger the range of R_L that results in ZVS operation. At some value for L_m, *all* values of R_L result in ZVS operation (when Fig. 2.14 fits entirely inside Fig. 2.8). Low values of L_m result in large circulating current in the tank circuit, even at no load. This is a trade-off between efficiency and wide load range.

2. If the load can be restricted to some minimum value, then the entire z_{in} curve is not traversed. This will result in less L_{res} used to displace the z_{in} curve vertically or a larger value for L_m. This is also an efficiency versus load range trade-off.

3. Since the tank circuit elements are assumed to exactly cancel at the switching frequency, any values will work such that $f_s = 1/2\pi\sqrt{L_1 C_1}$. The larger the characteristic impedance of these values, the larger the applied voltage stress to the components. It is not difficult to choose values for C_1 that result in applied voltages beyond 600 V even at moderate power levels. The lower the characteristic impedance, the larger the harmonic distortion in the tank current. This problem can be particularly difficult in the Class E circuit since it has even harmonics in its spectrum. Large even harmonic distortion can result in asymmetrical current flow in the diodes which then causes increased power loss. The Class D ZVS inverter is less sensitive in this regard due to the lack of even harmonic distortion. This is

a trade-off between component stress and efficiency (and potentially harmonically-related noise).

4. The value for C_2 must be chosen to be larger than the shunt capacitance of the MOSFET(s) and the diode(s) in the power switch. The shunt capacitance of a MOSFET is both nonlinear and variable from unit-to-unit. This means that C_2 should be several times larger than the switch capacitance to dominate the characteristics of the switch capacitance. Larger values of C_2 result in greater harmonic distortion and the resulting problems with the rectifier. This is a trade-off between the consistency of the inverter in manufacturing and efficiency.

5. Larger Values of L_{res} result in larger voltage stresses on the combination $(L_{res} + L_1)$ and lower output voltage for a given input supply voltage. This is a trade-off between output voltage and load dynamic range.

This last trade-off is addressed in the next section.

2.3.1 Resonant DC-to-DC Power Supply Conversion Ratio

It is convenient to divide the converter into stages for the conversion ratio analysis. Figure 2.15 shows a converter using a Class D ZVS inverter with a bridge rectifier. With the circuit partitioned as shown in the figure, the tank components are resonant at the switching frequency and therefore represent a short circuit to the tank current. The residual inductance, L_{res}, forms a voltage divider with the input impedance of the rectifier circuit. The voltage (fundamental) at the input to the rectifier is

$$V_r = \frac{z_{in}}{z_{in} + sL_{res}} V_{swf} \tag{2.29}$$

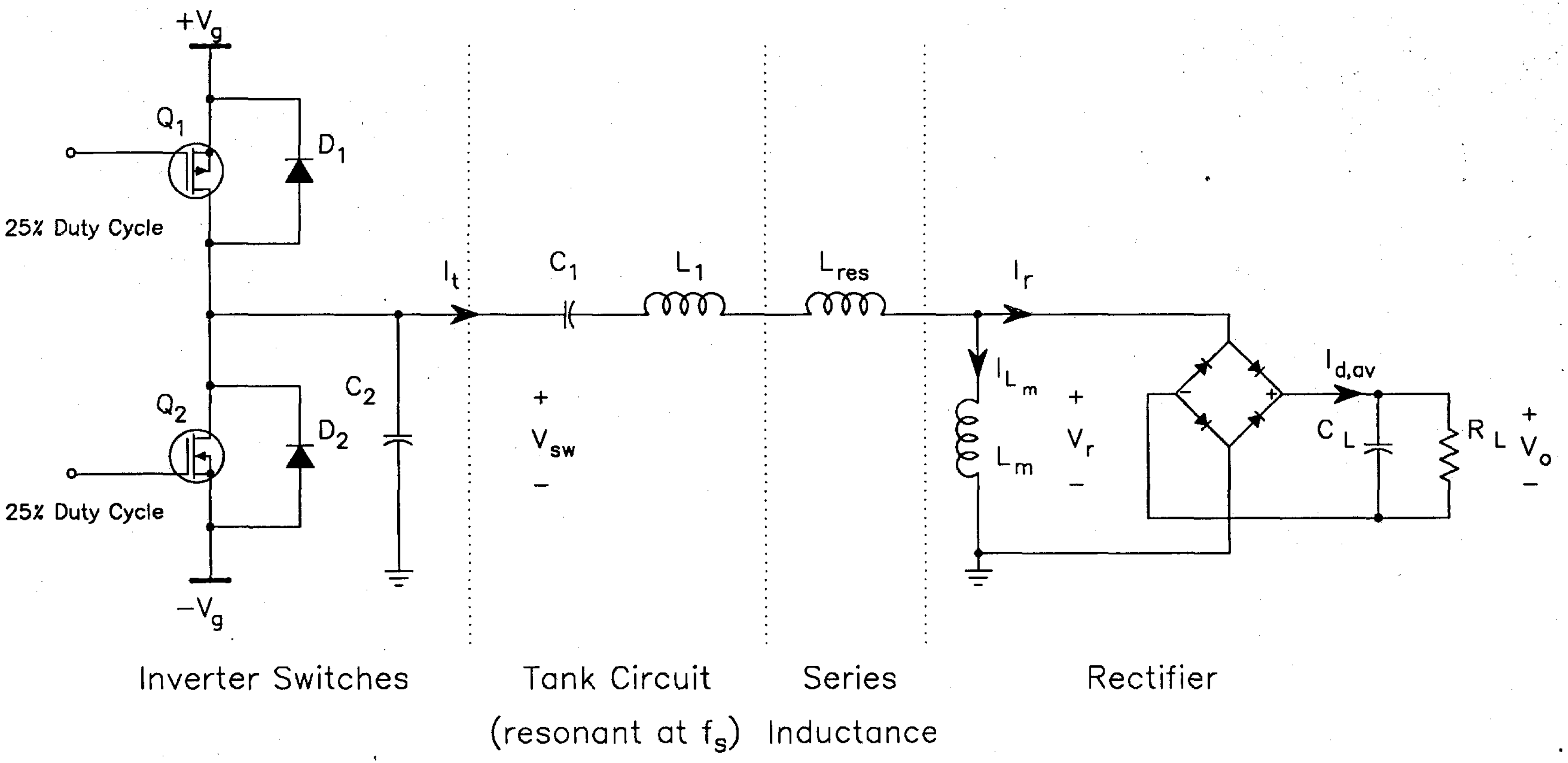


Figure 2.15: Functional Diagram of the DC-to-DC Converter using a Class D ZVS Inverter with a Bridge Rectifier. For analytical purposes, it is convenient to partition the circuit as shown.

where V_{swf} is the fundamental voltage at the output of the inverter switches. The output voltage from the rectifier is

$$V_o = \frac{\pi}{4} V_r \tag{2.30}$$

To complete this picture, it is necessary to calculate the fundamental of the voltage out of the inverter switches. This waveform is a bipolar quasi-trapezoidal waveform which switches between $+V_g$ and $-V_g$. The actual transitions are segments of sine waves but a reasonably good approximation is to use straight lines as illustrated in Fig. 2.16. The fundamental of this waveform is

$$V_{swf} = \frac{1}{\pi} \int_0^{2\pi} V_{sw}(\theta)\, e^{-j\theta} d\theta \tag{2.31}$$

Since $V_{sw}(\theta - \pi) = -V_{sw}(\theta)$ and $e^{j(\theta - \pi)} = -e^{j\theta}$, the integral simplifies to

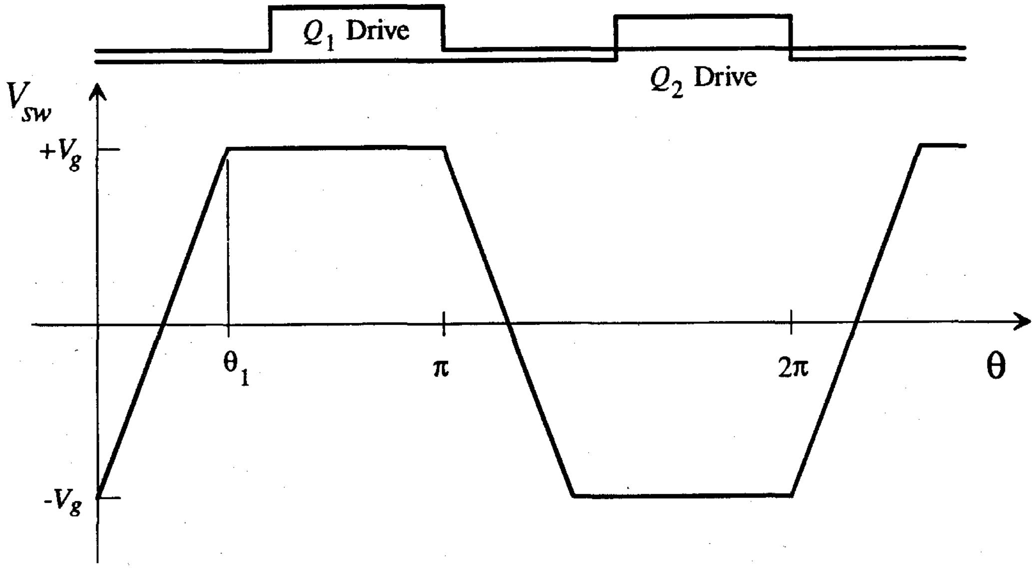


Figure 2.16: Idealized Waveform for the Class D ZVS Inverter. The fundamental of this waveform propagates through the resonant tank circuit to the rectifier.

$$V_{swf} = \frac{2}{\pi}\int_{0}^{\pi} V_{sw}(\theta)\, e^{-j\theta} d\theta \tag{2.32}$$

$$V_{swf} = \frac{2}{\pi}\int_{0}^{\theta_1} V_g \left(\frac{2}{\theta_1}\theta - 1\right) e^{j\theta} d\theta + \frac{2}{\pi}\int_{\theta_1}^{\pi} V_g e^{j\theta} d\theta \tag{2.33}$$

This integral simplifies to

$$V_{swf} = \frac{4\left(e^{-j\theta_1} - 1\right)}{\pi\theta_1} V_g \tag{2.34}$$

The magnitude of the fundamental varies from $1.15V_g$ for $\theta_1 = \pi/2$ to $1.27V_g$ for $\theta_1 = 0$ so a reasonable approximation is that $V_{swf} = 1.2V_g$. The transfer ratio from the DC input voltage to the DC output voltage can now be found from 2.29 and 2.30 to be

$$\frac{V_o}{V_g} = \frac{\pi}{4} \frac{1.2 \cdot z_{in}}{z_{in} + j\omega_s L_{res}} \tag{2.35}$$

where z_{in} is given in 2.19.

2.3.2 Resonant DC-to-DC Converter Control

The circuit discussed so far is only a converter since the output is proportional to the input. For practical application, it is necessary to control such a converter to regulate the output voltage against variations in the input DC source and against changes in the load and the converter itself. The conventional method to control a resonant converter of the type discussed in this chapter is to vary the switching frequency. This will cause the conversion ratio to change since the inductance L_{res} is the residual inductance that remains in the tank circuit after the capacitive reactance of the resonant capacitor has been subtracted from the inductive reactance of the tank inductor. A typical frequency variation would be plus or minus 10 - 15%. This variation in frequency is small compared to some other resonant topologies but is still unacceptable in some applications such as the power supply in a radar transmitter. In this application it is necessary that the switching frequency of the power supply remain fixed so that the switching ripple on the output also remains at a fixed frequency. It is this consideration that motivated the invention of a controllable transformer, named a magnetic regulator by the inventors [10]. In this device, which resembles a two-winding transformer, the input-output conversion ratio can be modified by the application of a DC control signal. This device is analyzed in the next chapter and then applied to the DC-to-DC converter problem in Chapter 4.

Chapter 3

Magnetic Regulator Modeling

Introduction

In the area of high voltage power supply (HVPS) design, many significant improvements have been made in recent years with respect to weight and size by utilizing high frequency switching techniques. In areas where weight and size are at a premium such as aircraft or missile radar, the switching frequencies have been driven above 300 kHz in designs utilizing square wave switching techniques. Often the requirement to operate at such high switching frequencies comes not from a consideration of the power supply's weight or volume, but from a system requirement to synchronize the switching frequency of the power supply to a system clock, thus reducing the harmful effects caused by the switching frequency and its many harmonics. In these supplies, the switching losses in the semiconductors and particularly the high voltage diodes become excessive. The designer then finds that the efficiency (and therefore the internal device temperatures) must be sacrificed to operate at these high frequencies. One way to alleviate some of the problems associated with these high switching frequencies is to use one of the many resonant switching techniques.

While resonant switching techniques allow higher frequency power supplies to operate efficiently, conventional designs have several disadvantages. One of the major disadvantages is the fact that regulation of the output voltage is accomplished by varying the switching frequency. Obviously, a variable switching frequency cannot be synchronized to a fixed system clock, so another mechanism is needed to accomplish the regulation.

Recently a novel device called a magnetic regulator (MR) was proposed in [10], in which control over a sinusoidal output voltage, at a fixed frequency, is possible in response to a controlling current. This device appears at first glance to be a transformer with an electronically-adjustable turns ratio. In fact, as shown below, the MR will function as a transformer if the control current that drives it is fixed. Further, if one varies the control current, the input to output conversion ratio is modified. Since the device is ideally lossless (real devices suffer from conductor loss in the windings and core loss in the core), the MR can function as a kind of 'control valve' for sinusoidal power signals. This suggests that a power supply with high efficiency could be constructed using an MR in a similar way to the pass element in a linear power supply.

By embedding this device into a resonant DC-to-DC converter such as described in [9], regulation of the output voltage is still possible but at a fixed switching frequency. A simple block diagram is shown in Fig. 3.1 to illustrate the idea.

While the converter described above works well, there is no theory available to describe its operation. This chapter will take the MR as a separate device and develop an

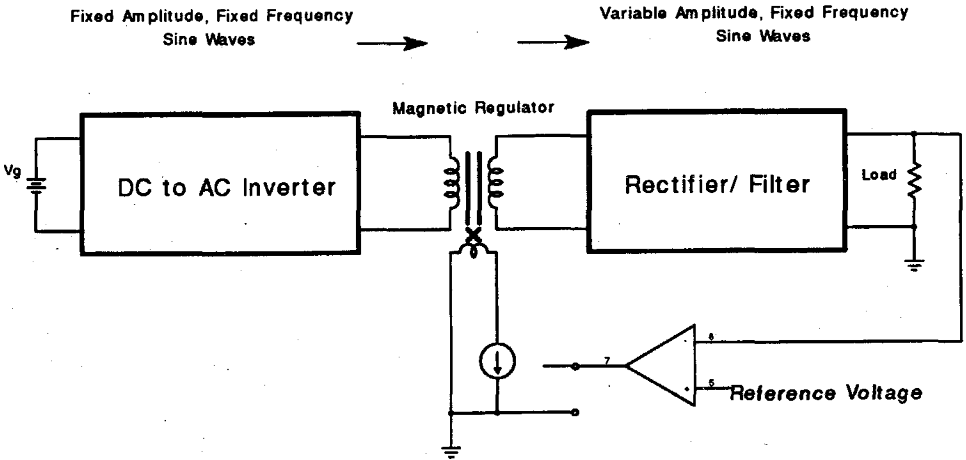


Figure 3.1: Block Diagram of a DC-to-DC Power Converter with Fixed Frequency Regulation Using a Magnetic Regulator.

equivalent circuit model based upon the actual physical structure of the magnetic device. In the model, each of the components can be directly related back to physical properties of the device. This results in a circuit model which provides both an intuitive feel for the device's operation and a quantitative model suitable for calculations. Once the modeling method is established, another structure is introduced and its shortcomings identified. This leads naturally to a new structure with significant advantages.

3.1 Physical Operation

The physical structure of one type of magnetic regulator is illustrated in Fig. 3.2. The core is similar to an EI core except with four legs instead of three. The legs are numbered one through four from left to right. A winding we shall call the primary or input winding is wound around leg number three and another winding, the secondary, is wound around leg number four. These windings can have different numbers of turns. Legs 1 and 2 each

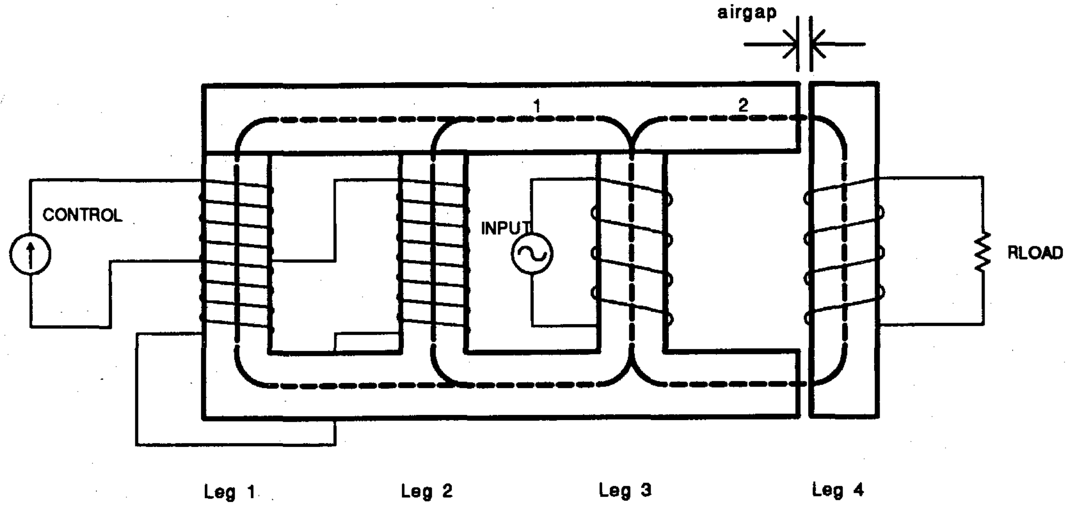


Figure 3.2: Physical Structure of the Four-Leg Magnetic Regulator. The flux generated by the input winding divides between paths 1 and 2 according to the reluctance of each path. The reluctance of path 1 can be modified by the current in the control winding.

have windings wound around them with equal numbers of turns and then series-connected in such a way that the flux produced by the primary will cancel in the series combination of these windings. A DC current source is connected to the series combination of coils 1 and 2 and thereby controls the DC flux density in the left half of the structure. For this reason, these windings are referred to as the control windings. Leg 4 has a small intentional air-gap.

If an AC source is connected to the primary terminals, then the flux generated by the primary winding will flow in leg 3 and then divide between the left and right paths according to the reluctance associated with each path. If there is no DC current in the control windings, the path to the left will have much lower reluctance than the path to the right owing to the air-gap placed in leg 4. In this case very little flux will flow into leg 4 and therefore very little AC voltage will be induced in the secondary windings. Further, there will be no AC voltage developed at control winding terminals because of the series-opposing connection of the windings.

Now if a DC current large enough to saturate legs 1 and 2 is driven into the control windings, the reluctance of the path to the left of the primary increases greatly forcing the AC flux from the primary to 'steer' to the secondary leg through the air-gap. In this case the voltage induced on the secondary will be equal to the primary voltage times the turns ratio of the secondary to the primary, less the voltage lost due to the inevitable leakage of some of the primary flux into the air surrounding the core.

The above describes the extremes of the control range. Between zero and maximum control current, the permeability is varied continuously so that the conversion ratio is varied continuously. In addition, the core material is usually soft ferrite which provides a smooth variation in the conversion ratio. Regulation can then be easily obtained using linear feedback concepts. The next section will quantify the concepts developed above to calculate the flux distribution in the core and therefore the input-output behavior of the device.

3.2 Modeling

3.2.1. The Reluctance Model

Since a knowledge of the flux distribution in the core of the MR is necessary to calculate the terminal voltages, the first problem to attack is that of the magnetic circuit. A method used on a very different problem in power electronics is directly applicable here. In [11], the problem of the design of an integrated coupled inductor was solved by using the reluctance concept to generate a magnetic equivalent circuit which then could be used to design an appropriate inductor. The AC waveforms in [11] were square waves and the operation of the power processing system was quite different; however, the reluctance model used there applies equally well to this case.

To model a magnetic device using the reluctance concept, one first identifies the important magnetic paths which make up the device. Each of these paths is assigned a 'magnetic resistance' or, more precisely, a reluctance. Each of the windings of the device will appear as magnetic 'voltage sources' whose voltage is equal to the ampere-turns product. The unknown quantity is the magnetic 'current' which is the flux in the actual device. The flux is solved for using standard electric circuit analysis techniques. An equivalent circuit for the magnetic device which will model its terminal characteristics can be directly obtained from the magnetic equivalent circuit. This is accomplished by recognizing that the inductance is inversely proportional to the reluctance and that terminal currents are proportional to the *voltage* sources in the magnetic equivalent circuit. Similarly, the 'currents' (flux) in the magnetic equivalent circuit are proportional to the voltage in the electric circuit. This implies that the electric circuit model can be derived from the magnetic circuit model using duality, where the reluctances are replaced by inductances. To properly account for the constants involved, each winding in the actual device appears in the electric equivalent circuit as an ideal transformer. A more complete description of this method is described in [12].

Figure 3.3 illustrates the various reluctance elements that make up the MR superimposed on the core geometry to emphasize the relationship between the elements in the reluctance model and the actual physical structure. The diagram is based upon the experimental four-leg MR which was assembled from six pieces of ferrite material. While this model is specific to the experimental device, it will be simplified in Fig. 3.4 to a more general model which is common to all the MR's designed to date. The primary and secondary windings are illustrated as magnetomotive force sources N_1I_1 and N_2I_2 respectively.

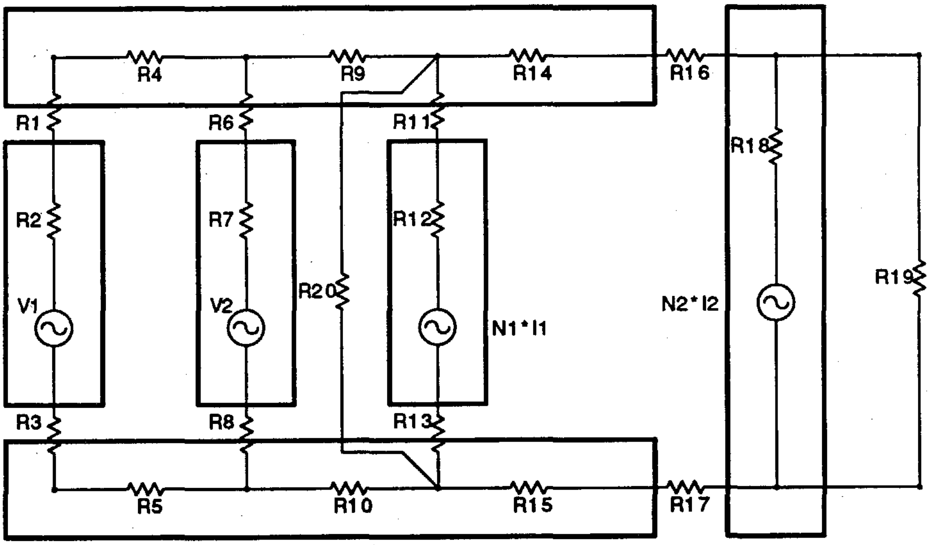


Figure 3.3: Reluctance Model for the Four-Leg Magnetic Regulator. Each reluctance in this model corresponds to a physical element in the MR.

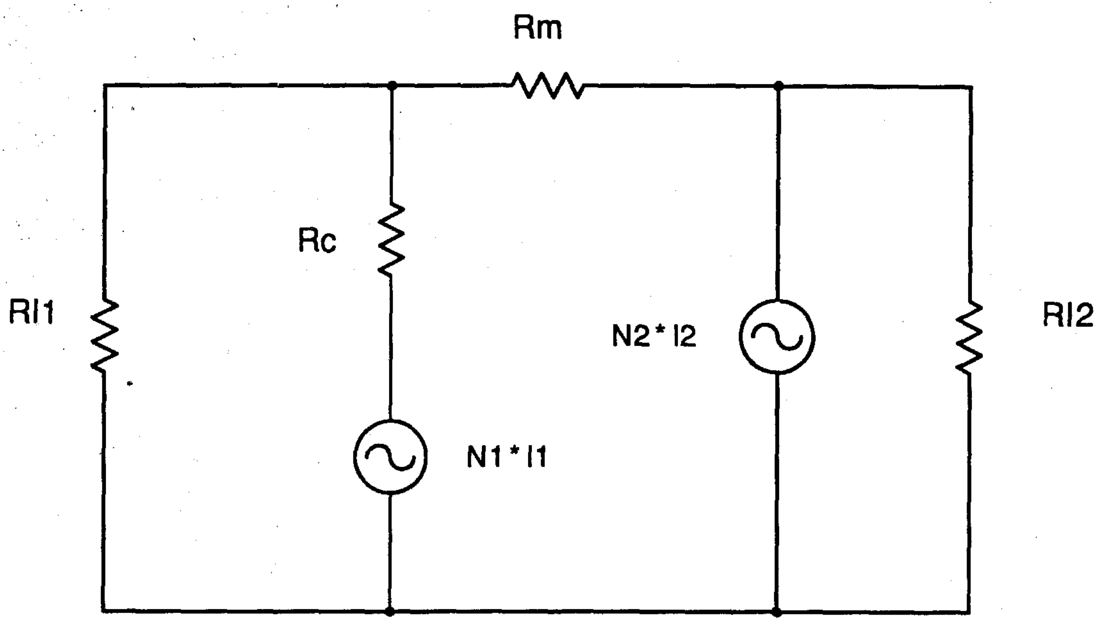


Figure 3.4: Simplified Reluctance Model for the Four-Leg Magnetic Regulator.

Several of the reluctances in this case are physically identical which will simplify the calculations considerably. Reluctances R1, R3, R6, R8, R11, and R13 represent the residual air-gap that inevitably results when separate pieces of ferrite are used. This gap is as small as possible and is estimated to be 2.54 μm (.0001 in). Reluctances R2, R7, and R12 are all the same being made from identical pieces of core material. Similarly, R4, R5, R9, R10, R14, and R15 are identical ferrite paths. R16 and R17 represent the intentional air-gap introduced into the structure for control purposes. Each gap is 190 μm (.0075 in). Reluctance R18 is unique due to the geometry used for leg 4. This reluctance is neglected as small in the final model. R19 and R20 are the leakage fluxes in air and therefore quite large (but measurable).

Figure 3.3 can be simplified to Fig. 3.4 by straightforward combinations of the elements in Fig. 3.3. Reluctance R_{l1} is the sum total of all of the flux which does not pass through the intentional air-gaps. This is the total primary leakage flux. R_{l2} is the secondary leakage flux path and is equal to R19. The coupling flux path is modeled by R_m. Reluctance R_c is the combination of all the reluctances which carry the common flux of both the leakage and coupling paths. The values are:

$$\begin{aligned}
R_{l1} &= R20 \left\| \left(R9 + R10 + \left(\frac{(R1 + R2 + R3 + R4 + R5) + (R6 + R7 + R8)}{2} \right) \right) \right. \\
R_c &= R11 + R12 + R13 \\
R_m &= R14 + R15 + R16 + R17 \\
R_{L2} &= R19
\end{aligned} \tag{3.1}$$

The reluctance R_c is usually quite small and would normally be neglected when compared to other elements in the model. It will be shown in the measurements section, however, that this element will be required to properly account for the measured behavior. Note that there is no DC source shown for the control winding mmf. The effect of the control windings is to modulate the permeability of the control legs so the reluctances R2, R4, R5 and R7 are functions of the control current from the general definition of the reluctance:

$$R = \frac{l}{\mu S} \tag{3.2}$$

Where R is the reluctance of a bar of length l, cross-sectional area S, and permeability μ.

Since the permeability is a function of the control current, so is the reluctance. Note that the flux paths through each of the control legs have substantially different reluctances owing to the greater distance of leg 1 from the primary (leg 3) than leg 2. This would cause an AC voltage to appear across the series-opposing connection of the control windings. This is undesirable since the control current source is usually a transistor collector which should not be reverse biased. To prevent the AC voltage from appearing across the control winding terminals, a capacitor is used which effectively shorts the AC voltage. This places the control windings in parallel thus forcing equal AC voltage on each. This implies that the flux through legs 1 and 2 are forced to be equal at a cost of some circulating current in the control windings. Therefore, the voltage sources V1 and V2 in Fig. 3.3 are equal in magnitude and opposite in polarity. R_{l1} is computed with this in mind in (3.1). In computing R_{l1} the dependent sources V1 and V2 are accounted for, so no AC ampere-turns are needed to represent the control windings in the simplified model.

3.2.2. The Inductance Model

The next step in modeling the MR is to transform the equivalent magnetic circuit into a circuit model for the inductances. By using the duality of the electric and magnetic fields as described above, the equivalent electric circuit in Fig. 3.4 is transformed to that shown in Fig. 3.5. The same subscripts are used in each figure with all the R's replaced by L's. The L's are calculated as follows:

$$L_i = \frac{N^2}{R_i} \tag{3.3}$$

where N is chosen to be the number of turns on the primary winding. (This choice is arbitrary; in general each mmf source is replaced by a pair of terminals and an ideal transformer whose turns ratio is N_a:N_b where N_a is a reference number of turns and N_b is the number of turns of the mmf source winding. Using N_a=N_b inserts a 1:1 transformer at the primary terminals which is then neglected. This choice of N_a amounts to referencing all the inductances in the model to the primary.)

The model shown in Fig. 3.5 is very similar to the usual model of a two-winding transformer with the exception of the element L_c. As stated above, L_c is actually present in a

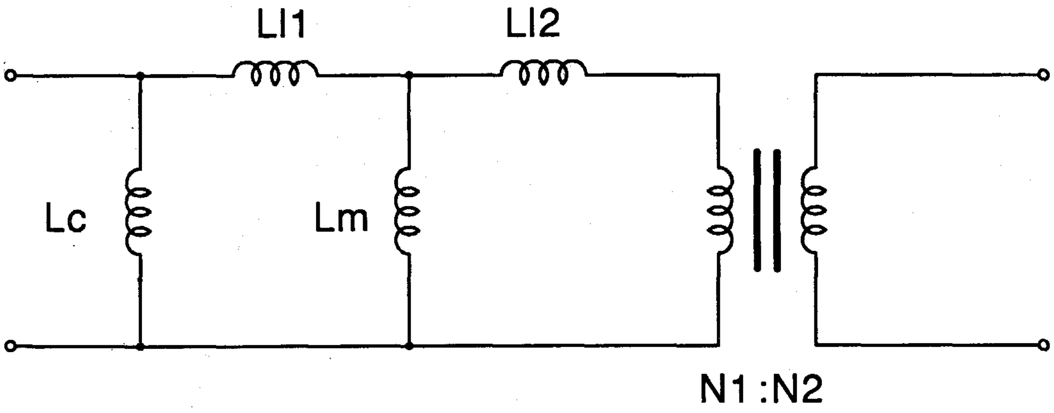


Figure 3.5: Inductance Model for the Four-Leg Magnetic Regulator. This circuit follows directly from Fig. 3.4.

conventional transformer, but is usually neglected. The most significant prediction from the model is that the turns ratio of the ideal transformer is fixed as are the inductances, except for L_{l1}. L_{l1} is proportional to the permeability of the control legs and hence would decrease with increasing control current. Measurements done below show this behavior clearly.

3.3 Experimental Verification

An experimental magnetic regulator was constructed using the dimensions shown in Table 3.1. The measurements were done using a computer-controlled network analyzer to measure the AC quantities and a computer-controlled power supply to sweep the control current during the measurement. The individual inductances must be extracted from the data measured at the terminals of the device. Since the magnetic regulator is being treated as a two port device, there are four parameters which can be determined from terminal

Table 3.1: Dimensions of the Four-Leg Magnetic Regulator

Element	Length (cm)	Area (cm^2)	Reluctance (1/H)
Top, Bottom Bar	75.9	0.87	116 k
Legs 1,2,3	27.4	1.18	92.4 k
Leg 4	27.4	0.87	126 k
Residual air-gap	0.00025	1.18	17.1 k
Intentional air-gap	0.019	0.87	1.75 M

measurements. Further, the magnetic regulator is a reciprocal device so only three of the parameters are independent. Since the model for the magnetic regulator has four elements, they cannot be uniquely determined by terminal measurements alone. This means only a three-inductor equivalent circuit can be uniquely specified by measurements and, therefore, the equivalent circuit of Fig. 3.6 can be used as a basis. The measurements are

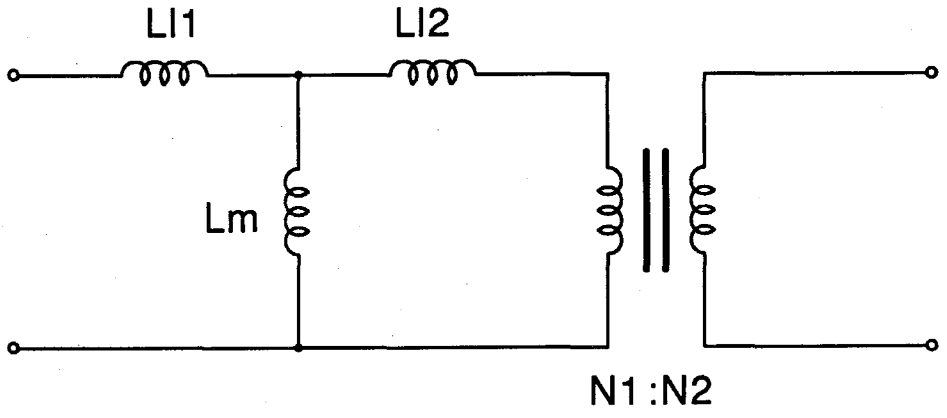


Figure 3.6: Minimum-Inductance Equivalent Circuit for a Two-winding device.

of three types: 1) Input inductance with the secondary open ($L_{11,open}$). 2) Output inductance with the primary open ($L_{22,open}$). 3) Secondary / primary ratio, driving the primary with the secondary open($R_{21,open}$). The model quantities in Fig. 3.6 can be obtained from the measured quantities as in (3.4).

$$\begin{aligned} L_{l1} &= R_{21,open} L_{11,open} \\ L_m &= L_{11,open} - L_{l1} \\ L_{l2} &= L_{22,open} - L_{l1} \end{aligned} \tag{3.4}$$

The ideal transformer's turns ratio is obtained from the winding information and is assumed to be 1:1 for simplicity in the present context.

Figure 3.7 shows the measurements for the case where L_c is ignored as is described by the above equations. From Fig. 3.7 it is apparent that the inductances L_m and L_{l2} are not independent of control current as was postulated above. The reason for this behavior is that the inductance L_c was ignored. Even though this inductor cannot be directly measured from terminal measurements, its presence is very real and it disturbs the measurements of the other inductances. To account for L_c, the approach taken was to calculate L_c from the geometry of the center leg and use that value as an input into the measurement routine. If the value for L_c is correct, and the proposed model is also correct, then the inductances L_m and L_{l2} should become independent of control current *at the same time.* The equations for the magnetic regulator model parameters with L_c included now become:

$$\begin{aligned} L_x &= \frac{L_c L_{11,open}}{L_c - L_{11,open}} \\ L_m &= R_{21,open} L_x \\ L_{l1} &= L_x - L_m \\ L_{l2} &= L_{22,open} - L_m \| (L_{l1} + L_c) \end{aligned} \tag{3.5}$$

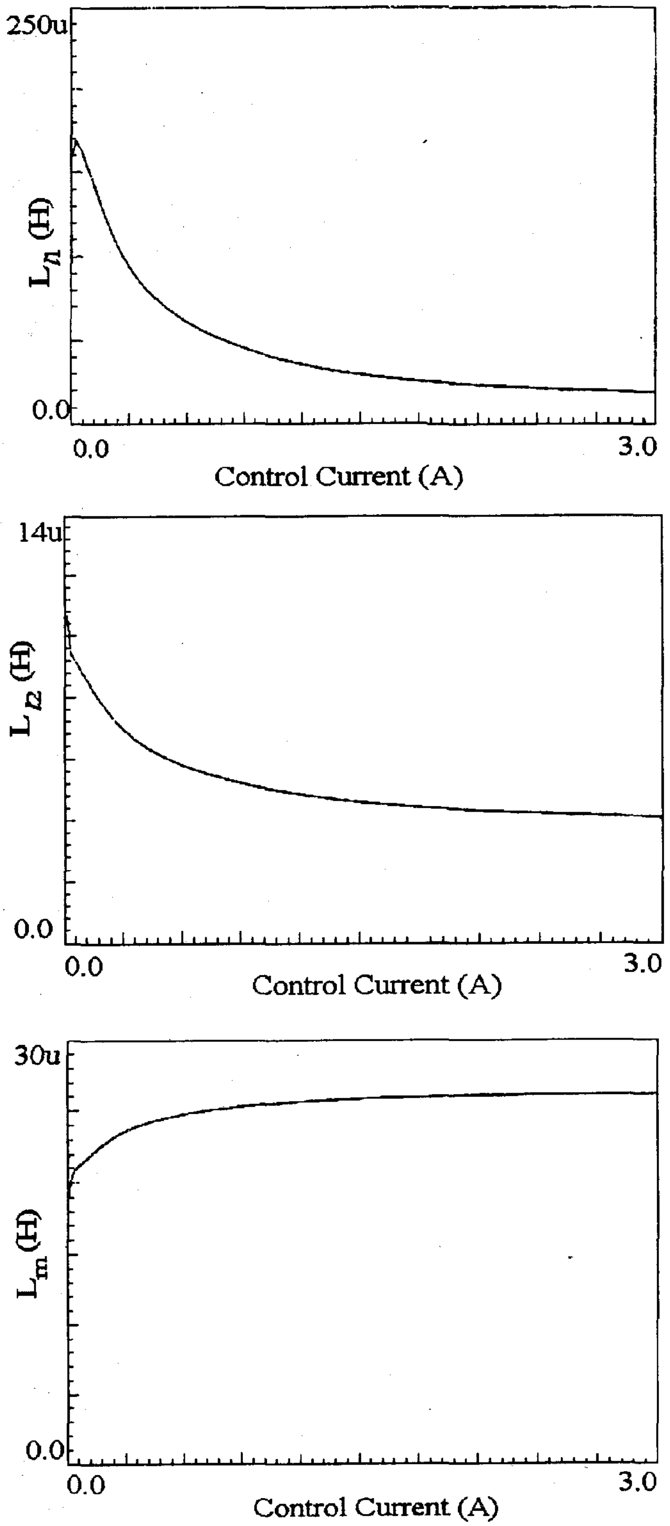


Figure 3.7: Magnetic Regulator Inductances. These curves were extracted from measurements and then calculated excluding inductor L_c.

Using the dimensions of the center leg from Table 3.1, the reluctance of the center leg is 92.4 k plus the air-gap reluctance of 34.2 k which gives a total value for R_c of 126.6 k. The corresponding inductance is 790 μH. Using this value for L_c, the other inductances can be recalculated as shown in fig 3.8. As predicted, the same value that gave a flat curve for L_m also gave a flat curve for L_{l2}. The fact that a single value for L_c makes both L_m and L_{l2} independent of control current is proof that the model is correct.

The reluctance concept also predicts values for the other elements in the model. The value for L_{l1} takes on a range of values from the value for the zero-bias ferrite permeability of approximately 2000, down to a value determined by the leakage fluxes in the air. The air leakage flux can be estimated from the measured value for L_{l2}. This value of inductance yields a reluctance value for a winding on a single leg, R19, as suggested in Fig. 3.3. This reluctance value, $27.9\text{x}10^6$ 1/H, can then be divided by three to obtain a rough value for R20 which is $9.3\text{x}10^6$ 1/H. This translates to an inductance of 10.8 μH. This assumes that the saturated reluctance of R2 and R7 go to infinity which is of course not realistic. Nevertheless, the predicted value could be taken as a lower bound on the estimate for L_{l1} at high control currents. The predicted values for the model elements are summarized in Table 3.2

Table 3.2: Predicted Versus Measured Values for the Magnetic Regulator.

Element	Predicted (μH)	Measured (μH)
L_{l1}	283-10.8	225-20
L_m	26.8	28
L_{l2}	-	3.58
L_c	790	Provides flat L_m and L_{l2}

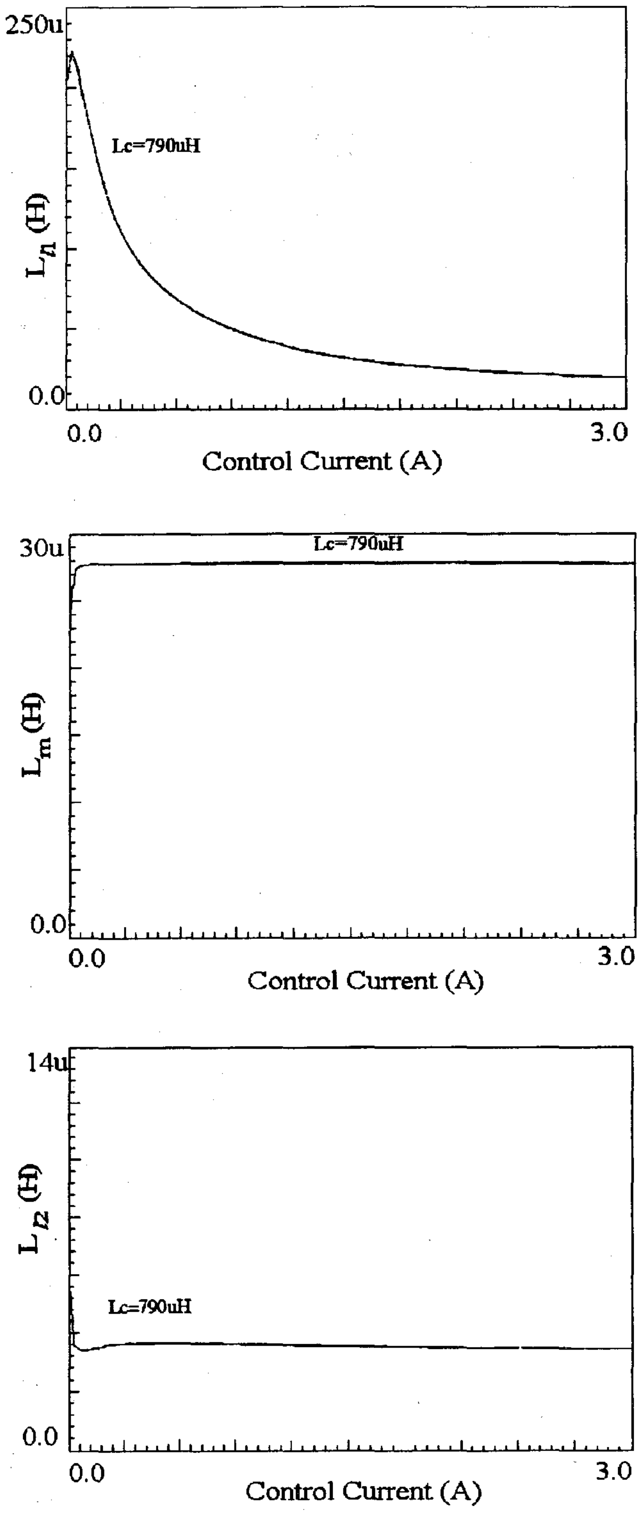


Figure 3.8: Extracted Inductance Values for the Four-Leg Magnetic Regulator after Accounting for the Inductance L_c.

3.4 Other Magnetic Regulator Structures

The magnetic regulator discussed above is one of several possible structures for this device. In [10], another possible structure is described which uses two E-I cores side-by-side. The control windings are wound around one of the outer legs of each core separately, then the two cores are placed side-by-side and the primary wound around the center legs of both cores. Similarly, the secondary is wound around the unused outer legs of both cores. Figure 3.9 shows two views of the device along with the path of the control flux.

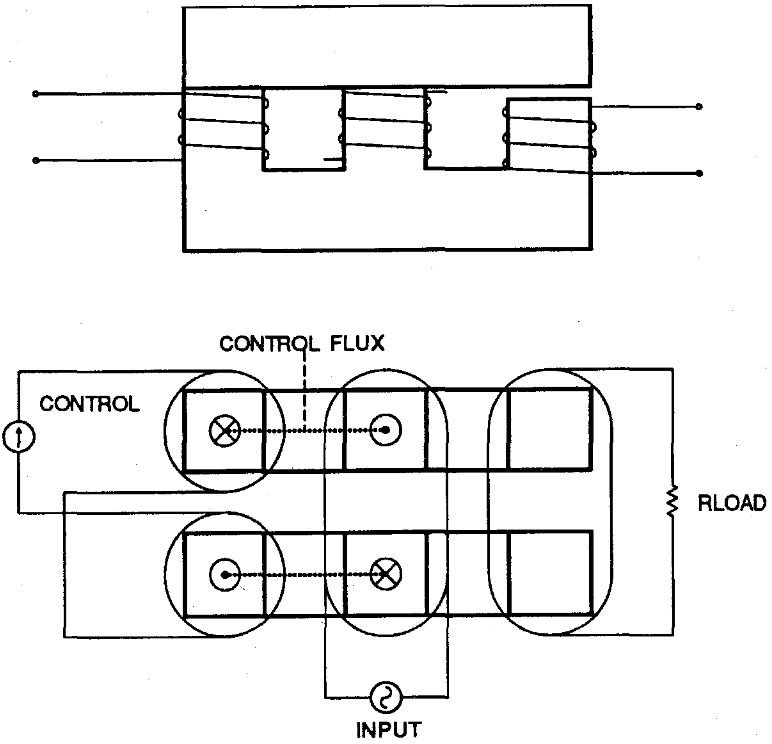


Figure 3.9: Top View of the Three-Leg Magnetic Regulator, Showing the Core and Winding Configuration and the Control Flux Path.

In this structure, the control legs are equidistant from the primary so there is no circulating current in the control winding as was present in the four-leg magnetic regulator described above. The reluctance model for this device is very similar to the previous case with one less leg. The magnetic circuit is shown in Fig. 3.10. Note the absence of the

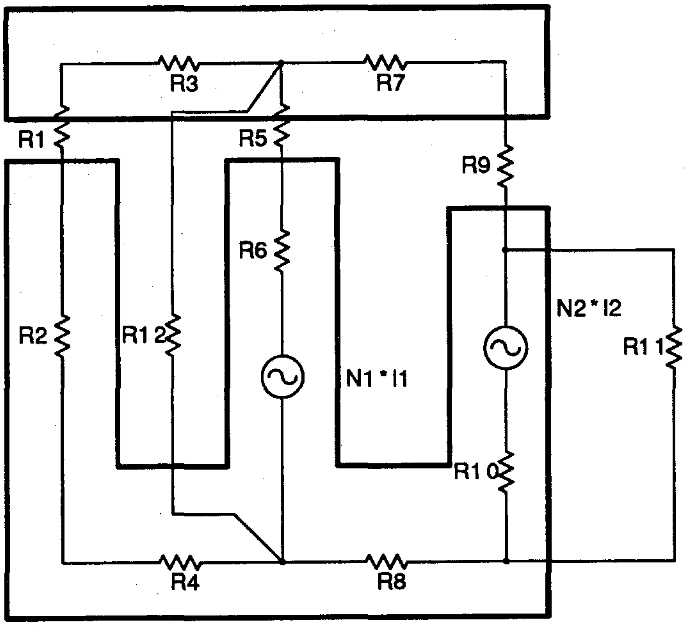


Figure 3.10: Reluctance Model for the Three-Leg Magnetic Regulator.

voltage sources in the control leg as compared to Fig. 3.3. This is due to the fact that the flux divides equally between the two control legs naturally, without any circulating current in the control windings. The complete reluctance model in Fig. 3.10 can be reduced to the simplified model shown in Fig. 3.4 by straightforward circuit manipulations. In this case, however, R_{l1} is not the only reluctance that is a function of control current; this time R_c is also dependent upon the control current since the DC control flux travels through it. The practical implication of this is that it is no longer possible to specify a single value for L_c and then extract the other inductances with a measurement. Also, as shown in [13], the core loss in ferrite which contains a DC bias is greater than that in unbiased ferrite. This means that the core loss in the primary leg would be greater than that in the four-leg structure.

These two shortcomings were the motivation for a new structure described in detail in [14]. In this device, the core is a custom-made core which resembles an E-I core with a longitudinal slot cut in one of the outer legs. A sketch of the device is shown in Fig. 3.11.

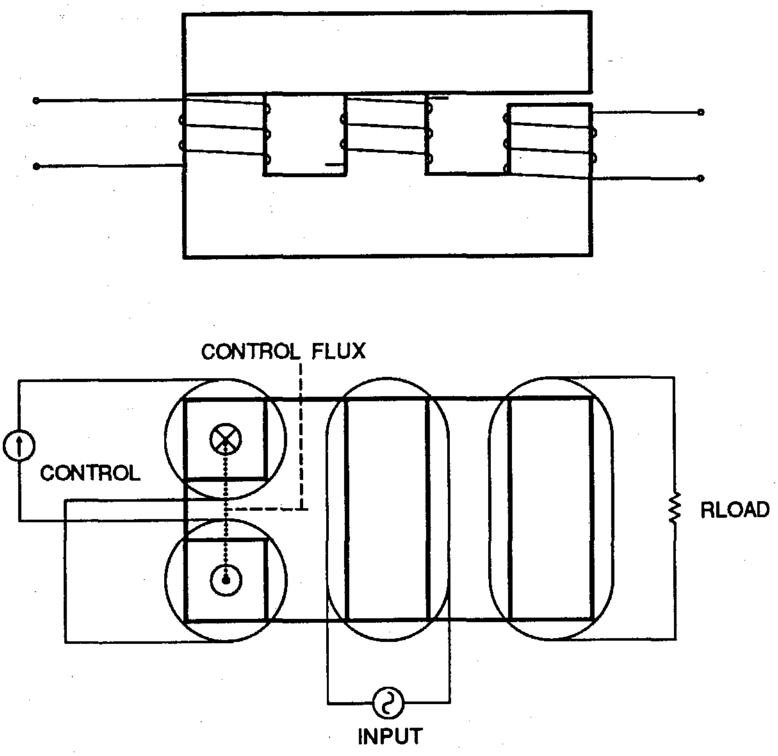


Figure 3.11: The basic structure of an improved three-leg magnetic regulator

The windings are wound as in the case of the three-leg magnetic regulator. The absence of a central gap confines the DC control flux to just the control legs of the core. This eliminates the variation of R_c and (therefore) L_c so the inductance values can easily be extracted from measurements as in the four-leg case. In addition, the DC flux occupies much less of the total volume of the core as compared to the three-leg magnetic regulator, yielding lower core losses. Therefore, this new device combines the best features of each of the devices from [10] without the undesirable features. A photograph of an experimental model of the improved magnetic regulator is shown in Fig. 3.12.

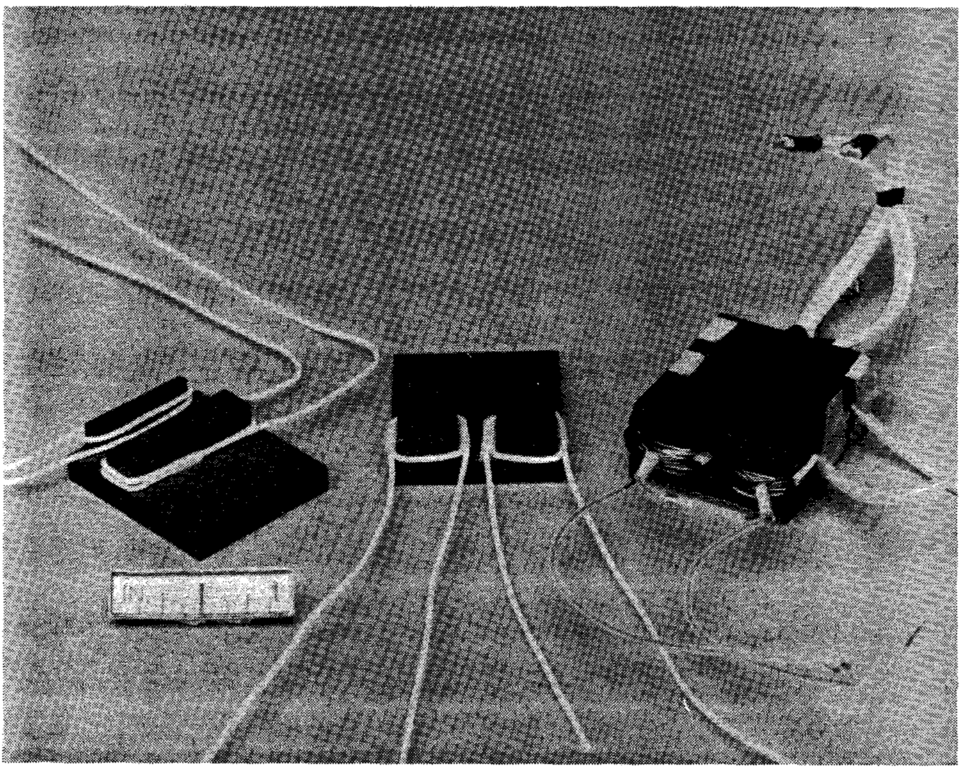


Figure 3.12: Experimental Model of the Improved Magnetic Regulator. The completed device is on the right. One half of the core containing the primary and secondary windings is on the left. The other half of the core containing the control windings is in the center. The windings on the latter two core halves are for illustration purposes only. This model was designed for a 10V, 1A power supply with 10kV primary-to-secondary isolation.

3.5 Conclusion

In this chapter a magnetic regulating device has been characterized which is capable of operation within a resonant converter to regulate the output voltage at a fixed frequency. The device resembles a transformer with an electronically-controlled leakage inductance. An equivalent circuit for the device is developed which both qualitatively and quantitatively describes the performance of the device. Measurements made on one particular design of the magnetic regulator verify the validity of the model.

The simplified reluctance model for the magnetic regulator presented in Fig. 3.4 contains all the important elements needed to describe the behavior of the magnetic regulator and also maintains a relationship between the equivalent circuit model and the physical structure of the device. This model is simple enough to be included in a larger analysis of the operation of a power processing system using the magnetic regulator as a regulating element. Such an analysis could be used to design an appropriate compensation network for the feedback loop in the system.

The first magnetic regulator analyzed in this chapter has one disadvantage in that a circulating current in the control windings exists in order that the AC voltage across the winding is zero. A second structure was discussed which eliminates the circulating current but at a cost of increased core loss and an equivalent circuit with two variable elements rather than one. The problems with these structures motivated the invention of a new structure which captures the desirable features of the previous devices without the disadvantages.

Chapter 4

Regulation of the Resonant DC-to-DC Converter at Fixed Switching Frequency

Introduction

Chapter 2 pointed out several advantages to resonant DC-to-DC converters which make them attractive in many applications. One serious drawback to a resonant converter is the fact that output voltage control is accomplished through variation of the switching frequency. There are applications where a high switching frequency is desirable, but a variable switching frequency is unacceptable. The observation that the magnetic regulator can control the amplitude of a sine wave in response to a low-power control signal and to do so with high efficiency suggests a means of designing a resonant power converter without the disadvantage of a variable switching frequency.

4.1 The Magnetic Regulator as a Control Device

To achieve output-voltage regulation at a fixed switching frequency, the basic idea is to insert the magnetic regulator in the forward power path as shown in Fig. 4.1. Since specific impedance conditions must be met at the interface between the inverter and the rectifier, it may be necessary to include matching components before and after the magnetic regulator. This approach was first used by the inventors of the magnetic regulator [10] before the true nature of the magnetic regulator was understood. While this approach works, the goal in most power supply designs is to maximize efficiency while minimizing volume and mass. The matching circuits in Fig. 4.1 must pass the full forward power of

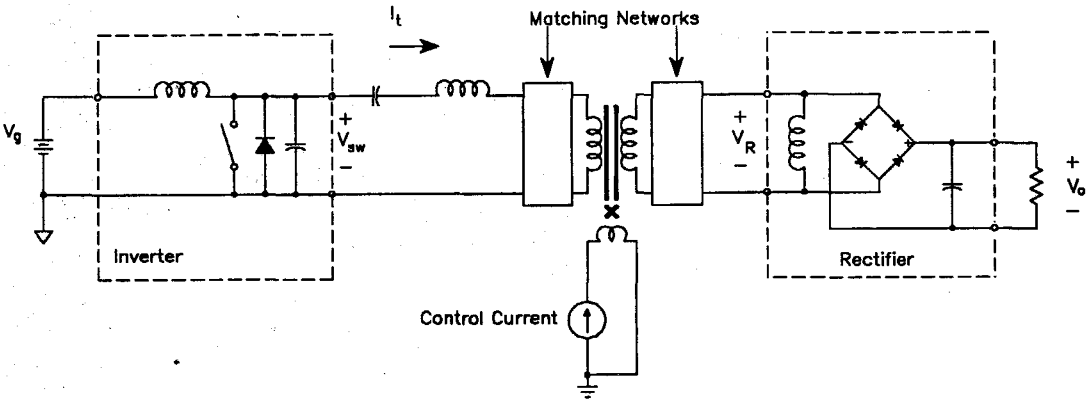


Figure 4.1: Resonant DC-to-DC Converter Using a Magnetic Regulator for Fixed-Frequency Control. Matching networks may be required to preserve the compatibility between the rectifier and the inverter.

the converter; therefore, these components can be quite large and will inevitably result in power loss. The magnetic regulator model developed in Chapter 3 provides the means to simplify this topology to a minimum number of magnetic components.

4.1.1 Integration of the Magnetics into the Magnetic Regulator

The first step toward the simplification of Fig. 4.1 is to insert the equivalent circuit for the magnetic regulator into the forward power path as in Fig. 4.2. The model shown for

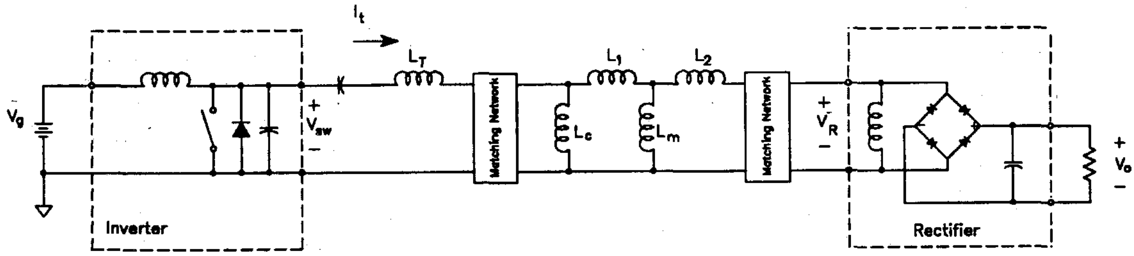
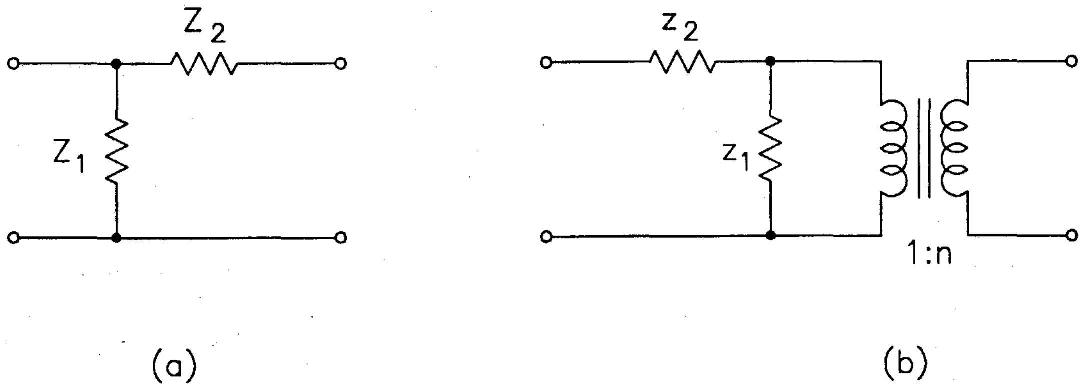


Figure 4.2: DC-to-DC Converter with the Magnetic Regulator Equivalent Circuit Inserted into the Power Path. The magnetic regulator equivalent circuit also contains an ideal transformer which has been omitted for clarity.

the magnetic regulator is the general model. In nearly all practical cases the inductance L_c is much larger than all the other inductances in the circuit and can be neglected. The inductance L_2 is usually much smaller than all the other inductances in the model and could be replaced by a short circuit. In the case where L_2 is not negligible, it is still possible to eliminate it with a simple transformation as outlined in Fig. 4.3. This transformation can be applied to L_m and L_2 which will reverse their order and add an ideal transformer. The new series inductance can be absorbed into L_1. If this transformation is used, the results will be a new value for L_m which is smaller than the original, an ideal transformer with a turns ratio near one, and a slightly larger value for L_1. In either case, the new model for the converter is shown in Fig. 4.4. At this point it is clear that the matching networks will be unnecessary if the inductances in the magnetic regulator can be freely chosen. If the primary leakage inductance of the magnetic regulator can be designed to be equal to the resonant inductor in the inverter, then no impedance matching circuit is needed at the input of the magnetic regulator. Similarly, if the magnetizing



$$z_1 = \frac{Z_1^2}{Z_1 + Z_2} \quad z_2 = Z_1 \| Z_2 \quad n = \frac{Z_1 + Z_2}{Z_1}$$

Figure 4.3: Transformation from a Shunt-Series Impedance to a Series-Shunt Impedance.

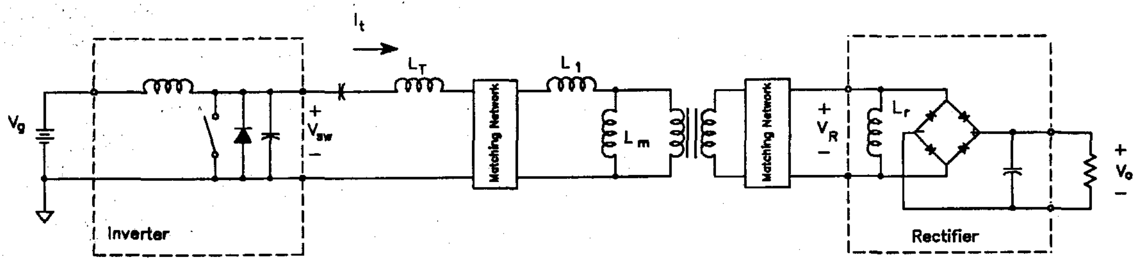


Figure 4.4: DC-to-DC Converter Using a Simplified Magnetic Regulator Model. The ideal transformer may have a turns ratio slightly different from the physical turns ratio of the magnetic regulator if the secondary leakage inductance L_2 is accounted for.

inductance of the magnetic regulator can be made equal to the shunt input inductor into the rectifier, then no matching circuits are required at the output of the magnetic regulator.

The next question to answer is if the magnetic regulator inductances can be designed to meet the necessary conditions. The magnetizing inductance of the magnetic regulator is determined by the intentional air-gap placed in the core so this value can be chosen by the designer. In most magnetic circuits, the leakage inductance is not well controlled. In the magnetic regulator, the leakage inductance is actively controlled by the control current so a feedback loop can be designed to maintain $L_1 = L_T$. In most instances, the feedback will be designed to monitor the output voltage and adjust the control current to stabilize it. In this topology, the regulation is accomplished by changing the resonant tank circuit rather that the frequency of the current in the tank. The final circuit for the converter is shown in Fig. 4.5. This power supply topology is the subject of a patent application [15]. This configuration has several advantages:

1. There is only one high-frequency magnetic component. This component will usually be much more compact than the separate inductors used in the conventional design.

2. In the conventional design, a significant amount of current flows in the shunt inductor at the rectifier input. In the integrated design, this current

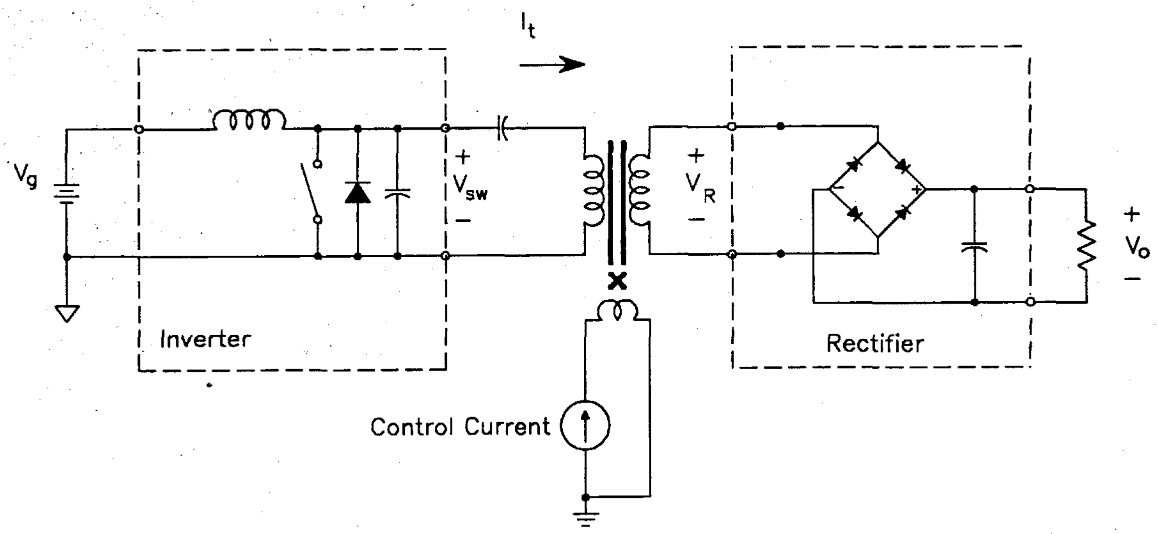


Figure 4.5: DC-to-DC Converter after Integrating the Resonant Inductor and Matching Inductor into the Magnetic Regulator.

flows only in the primary and not in the secondary. This results in lower loss in the conductors compared to a design using a normal transformer with the shunt inductor on the secondary side.

3. The control signal is isolated from either the input or the output ground. This allows the feedback circuits to be located exclusively at the output ground with no violation of the primary-secondary isolation.

4. The circuit will operate normally even with a large leakage inductance in the magnetic regulator. This allows a large physical separation between the primary and secondary windings which provides high voltage isolation.

5. Multiple secondaries can be wound on the magnetic regulator if tight cross-regulation is not required.

6. This design provides natural current limiting since some impedance will always be present between the load and the inverter. (This is in contrast to

the PWM converters where an output short will quickly destroy the semiconductors if some current limit is not built-in.)

Nonetheless, there are some disadvantages with this configuration. The main disadvantage is that the input voltage to the magnetic regulator terminals is very high since it is the sum of the voltage into the rectifier plus the voltage across the resonant inductor. The primary winding of the magnetic regulator will need many turns to keep the flux density in the core at an acceptable level. The required number of turns may make the realization of the desired magnetizing inductance difficult. In some cases, it may be necessary to add the rectifier matching inductor externally. Choosing a low value for the resonant inductor will minimize this problem. Under some circumstances it is possible for the magnetic regulator and its control current supply to oscillate open loop. This would appear to be caused by excessive flux swing in the control legs of the magnetic regulator. If the flux swing in the magnetic regulator is too large, the impedance looking into the control winding can have a negative real part. This effect imposes another design constraint on the magnetic regulator.

4.2 Applications

The best way to demonstrate the usefulness of this new power supply approach is to design some useful prototype circuits. Two such designs will be pursued in this chapter. The first application is a filament power supply for a traveling wave tube (TWT). In this application, 10 V are required at 1 A to heat the filament which is connected to the cathode of the TWT. The cathode of the TWT is at a high negative voltage (-3000 V) which requires a large input-output voltage isolation. This application takes advantage of the large voltage isolation that is possible using the new power supply technique.

The second application is the high voltage power supply for the TWT cathode. This supply must provide -2000 V to the cathode plus 1225 V with respect to the cathode for the TWT collector. This supply must provide 150 W of total output power with the bulk of the power in the collector supply. This application will illustrate the use of this power supply technique in a high power and high input voltage application. Additionally, the ability to drive a voltage multiplier will be demonstrated. This is a significant departure from the usual application of the voltage multiplier to low-power applications such as CRT displays. The fact that the voltage multiplier can produce significant output power in a reasonable volume is a consequence of the high operating frequency of this design.

4.2.1 The Filament DC-to-DC Converter

The main requirements for the filament DC-to-DC converter are:

1. Input Voltage, 20 to 32 V.
2. Output Voltage, 10 V regulated within 5% @ 1 A.
3. Input-Output isolation, 3000 V
4. 1 MHz switching frequency. (This choice was arbitrary; the purpose here is to demonstrate operation at some high switching frequency for reasons discussed in Chapter 1.)

The large input-output isolation voltage would normally dictate a transformer with a large leakage inductance because of the physical separation between the primary and secondary. The insulation is often solid encapsulating material to minimize this distance. Solid encapsulated transformers are expensive to produce and often suffer reliability problems. To avoid these problems, this example design will use high voltage wire for the secondary winding. This wire can withstand quite high voltages due to thick polyethylene insulation. The thick insulation means that the secondary winding will have a poor fill factor and large leakage inductance. The new power supply design will naturally incorporate the leakage inductance, and the fill factor problem can be mitigated by using a minimum number of turns of secondary wire. Since high voltage wire is used for the secondary winding, it is inconvenient to use the center-tapped full-wave rectifier circuit which would normally be used in a low-voltage application such as this. Instead, a bridge rectifier circuit was used. This choice sacrifices some efficiency for ease of manufacturing.

The low power and low input voltage in this application indicate that the Class E circuit would be an appropriate inverter. This inverter is preferred over the Class D ZVS inverter since it has ground-referenced drive circuits for the power switch and uses only one active switch. The topology has a basic input-output conversion ratio that is given by [9]:

$$\frac{V_{out}}{V_{DC}} = 1.6K\frac{|Z_A|}{|Z_A + jX_1|} \tag{4.1}$$

where

Z_A = input impedance to the rectifier

X_1 = reactance of the tank circuit at f_s

K = rectifier conversion factor $= \pi/4$

The upper bound on the conversion ratio is 1.25. Given that the minimum input voltage is 20 V, the maximum output voltage possible would be 25 V. This would require a large value for X_1 to maintain regulation so a turns ratio in the magnetic regulator is indicated. A turns ratio of 0.5 results in a maximum output voltage at a minimum input voltage of 12.5 V.

The Rectifier Design

The rectifier design involves the selection of appropriate diodes and the matching inductor. The diodes used in this example are Schottky diodes to take advantage of their fast switching characteristics and also the low forward voltage drop. The magnetizing inductance of the magnetic regulator serves the purpose of the matching inductor.

The magnetizing inductance is chosen so that under nominal load conditions, the input impedance to the regulator has a maximum real part as shown in fig. 2.14. This implies that $R_L = X_{L_m}$. R_L is slightly larger than the actual load resistance to account for the diode drops in the bridge rectifier. The effective load resistance is (10 V +2 V_d)/ 1 A = 11 Ω. All calculations will be done by reflecting the loads to the primary side of the magnetic regulator so the value used for R_L is 44 Ω. The design value for L_m is therefore 7.0 μH.

The Inverter Design

The first step in the inverter design is to select a value for the shunt capacitance of the power switch. This capacitance must be larger than the internal capacitance of the MOSFET and diode used as the power switch. This capacitance is chosen to place the input impedance of the rectifier inside the region of ZVS switching as shown in Fig. 2.8 (b). The real part of the rectifier input impedance normalized to X_{C_2} must be less than 0.2 to satisfy this condition. The imaginary part of the rectifier input impedance is not important since the resonant tank circuit will be in series. The input impedance to the rectifier at the nominal operating point is $(4/\pi^2)\,(R_L + X_{L_m}) = 17.8 + j17.8\ \Omega$ from Fig. 2.14. To provide some design margin, the operating point in the normalized z_y-plane in Fig. 2.8 (b) was chosen to be $0.18 + j0.25$. By equating the real part of the input impedance to the rectifier and the desired value of z'_y, the value of C_2 is found to be 1600 pF.

The next components to select are the resonant tank components. In Chapter 2 it was noted that the choice of the resonant capacitor's value is a trade-off between large distortion of the tank current for large values of C_1 versus high voltage-stress on the tank components for small values of C_1. An initial choice of C_1 = 1600 pF caused an open-loop oscillation of the control current source due to the high voltage impressed on the magnetic regulator primary. The value of C_1 was then changed to 3900 pF which was stable open loop under all operating conditions. For C_1 = 3900 pF the resonant inductor is 6.5 μH. In addition to this inductance (which exactly cancels the reactance of the resonant capacitor), there is additional inductance needed to move the load on the inverter into the ZVS region. The normalized reactance z'_y has an imaginary part of 0.25 at the desired operating point. This translates to an inductance of 1.75 μH. This inductance is added to the resonant inductance for a total series inductance of 8.25 μH.

The tank current can be calculated from Equation 2.18 to be approximately 1.1 A. This implies the peak voltage across the resonant capacitor is 45 V, and across the resonant inductor the peak voltage is 57 V. Since the voltage into the rectifier is 22 V scaled to the primary of the magnetic regulator, the voltage across the series combination of the series inductance and the rectifier input is 78 V. This is the primary input voltage of the magnetic regulator.

The Magnetic Regulator Design

A reasonable number of turns for the secondary winding of the magnetic regulator was chosen to be two. The design example uses a switching frequency of 1 MHz which will dictate an acceptable maximum flux swing consistent with reasonable core loss. The value chosen was B_{peak} = 0.04 Tesla. This choice of maximum flux density was based upon the manufacturer's data on core losses at 1 MHz. (In hindsight this choice was too high because the efficiency was lower than expected.)

The secondary number of turns, N_s, together with a maximum flux density, B_{peak}, and a known secondary voltage, V_{out}, determine the size of the secondary leg of the magnetic regulator. The voltage waveform applied to the secondary is a square wave making the appropriate relationship for the area of the secondary leg,

$$A_s = \frac{V_{out}}{4B_{peak}N_s f_s} \tag{4.2}$$

The resulting value for A_s is 0.34 cm^2. The voltage waveform applied to the primary winding is approximately a sine wave so the appropriate formula for the area of the primary is

$$A_p = \frac{V_{peak}}{N_p B_{peak} 2\pi f_s} \tag{4.3}$$

The primary leg of the magnetic regulator was designed for the initial value of C_1; therefore, the value of V_{peak} used was 130 V. The actual value in the hardware using the latest value for C_1 of 3900 pF and the corresponding input voltage of 78 V results in B_{peak} = .024 T.

The cross-sectional area of the control legs of the core is set equal to the primary leg so that the control legs do not have excessive flux density if all of the primary flux should steer to the control legs. The number of turns on the control legs of the core should be large enough to reduce the required control current to a manageable value. There is one item to note in the selection of the control turns. Each half of the control winding acts as a transformer secondary to the magnetic regulator primary. The sum of the two control windings is zero due to the series-opposed connection, but each coil can individually have high voltage since the control winding normally has a step-up ratio with respect to the primary. In the example, the control windings were each chosen to have 21 turns on each coil. The bias current in the control winding with this choice of control winding turns is 500 to 600 mA. The magnetic regulator built to these specifications is shown in the photograph in Fig. 3.12. The measured parameters that go with this device are shown in Fig. 4.6.

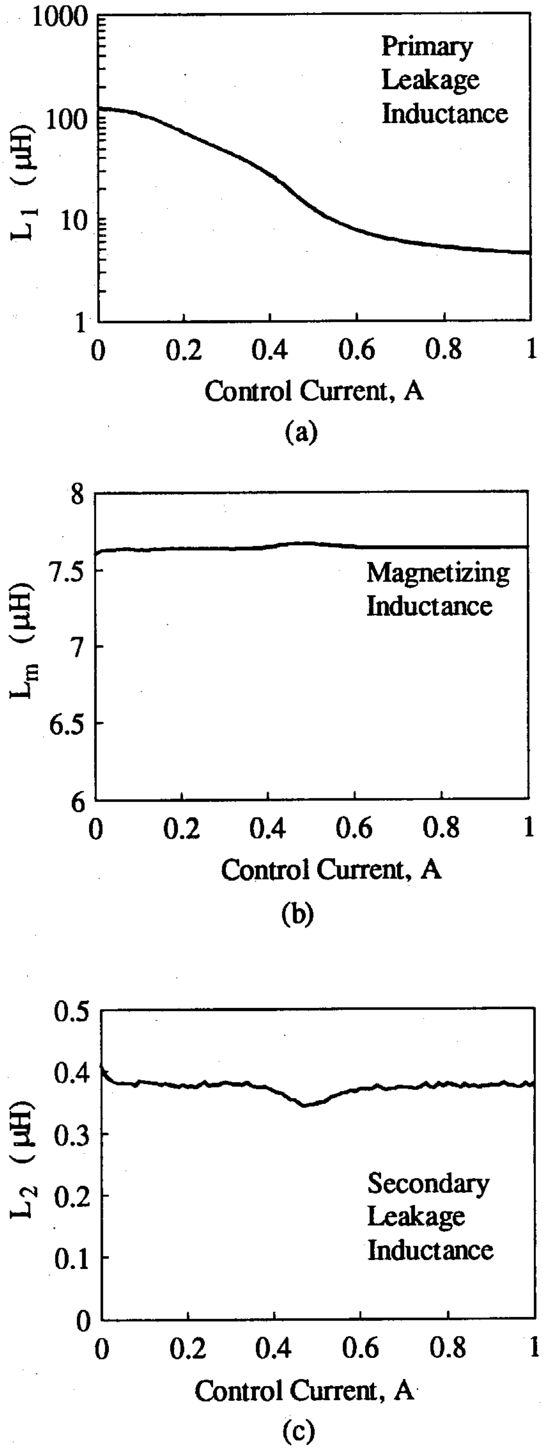


Figure 4.6: Measured Inductances of the Filament Power Supply's Magnetic Regulator. The designed values are 8.25 μH for L_1 and 7.0 μH for L_m. L_2 is a parasitic element and therefore should ideally be zero. The small actual value is easily accommodated in the filament supply's design.

SPICE Simulation and Measured Results of the Filament Power Supply

A useful tool in the design and evaluation of these resonant converters is the circuit simulation program SPICE. There are many effects in these converters that are simply too difficult to calculate by hand. The simulation provides useful insight into the operation of the real converter since various parasitic effects can be inserted into the model one at a time. Once the dominant effects are identified, an analytical solution can be attempted which accounts for these effects. It is important in simulations of switching power supply circuits to use the simplest equivalent circuit which will model the behavior desired. This is because a transient analysis of the power supply must be done for many cycles of the switching frequency in order that a steady-state condition is reached. The best approach is to begin with a very simple equivalent circuit and add refinements until the simulated performance is in acceptable agreement with the measured data. This process is not unlike the design-analyze-iterate sequence advocated in [16] except that the analysis process has an inner loop which is simulate-measure-iterate. This inner loop can save a significant amount of time and labor, especially when the circuit under consideration is difficult to fabricate or measure. As in hand analysis, it is not economical to put in the most detailed, general model known for the circuit being simulated since the results in circuits like this will take a fast workstation hours to complete if the solution converges at all. Even when the results of such an analysis are completed, it is difficult to separate the effects caused by the various elements in the model. In the beginning stages of a design, the simulation must be done without comparisons to the actual hardware. Once the first prototypes are fabricated, then the simulations can be compared with the measurements and refined as necessary. The resulting simulation after refinements becomes a valuable tool in the analysis of the circuit. This approach will be used in Part II so a good steady-state simulation is worthwhile at this point.

The circuit entered into SPICE to solve for the steady-state condition is shown in Fig. 4.7. In this circuit, the MOSFET switch is treated as an ideal switch with a shunt capacitance. All the diodes are ideal SPICE diodes which means that they have an exponential *v-i* characteristic but have no charge storage. The magnetic regulator is modeled by the equivalent time-invariant inductances since the control current is assumed to be constant for the steady-state solution. The losses of the tank circuit are included in this model as an equivalent series resistance in the primary of the magnetic regulator equal to 1.5 Ω. The large values of the input inductor L_{RFC} and the output filter capacitor C_L cause the circuit to have low-frequency dynamics. To reach an acceptable steady-state solution, the SPICE transient analysis is run for 100 cycles of the switching frequency before the data are saved. The SPICE simulation results are compared with measurements on the actual hardware in Fig. 4.8. The results show close agreement between the simulation and the measured performance giving a high degree of confidence in the accuracy of the SPICE model.

One undesirable effect that occurs in the filament DC-to-DC converter is the distortion of the tank current due to the switching action of the inverter and the components chosen to make up the tank circuit. Since the current in the tank circuit is not actually a symmetrical sine wave, the idealization of a sine wave tank current may be questioned. The Class E inverter is a single-ended inverter that can have even harmonic distortion which is apparent in both the measured and simulated circuits. The consequence of this distortion is an imbalance in the currents in the diode bridge which force a larger share of the average current through one pair of diodes. This leads to unwanted dissipation in two of the bridge diodes and also to higher than expected output ripple. This disadvantage of the Class E inverter is one of the motivating factors in the use of the Class D ZVS inverter circuit in higher power applications.

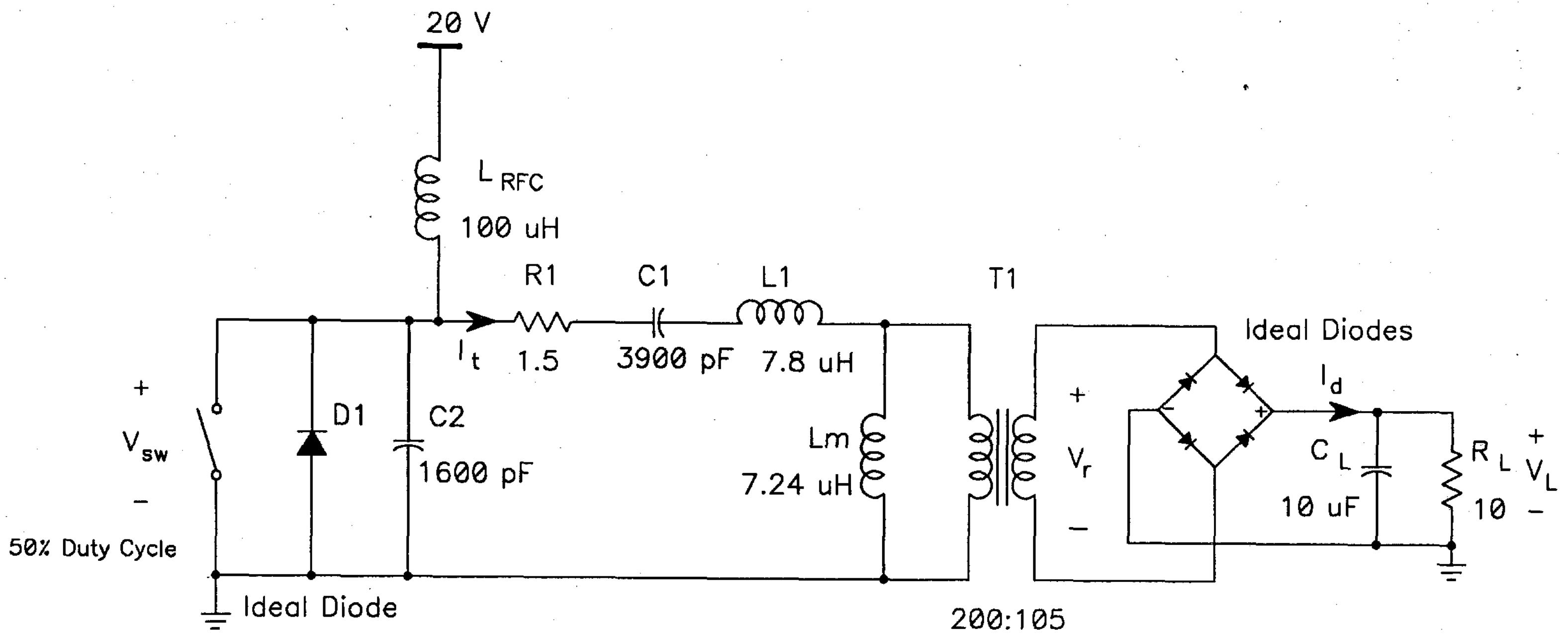
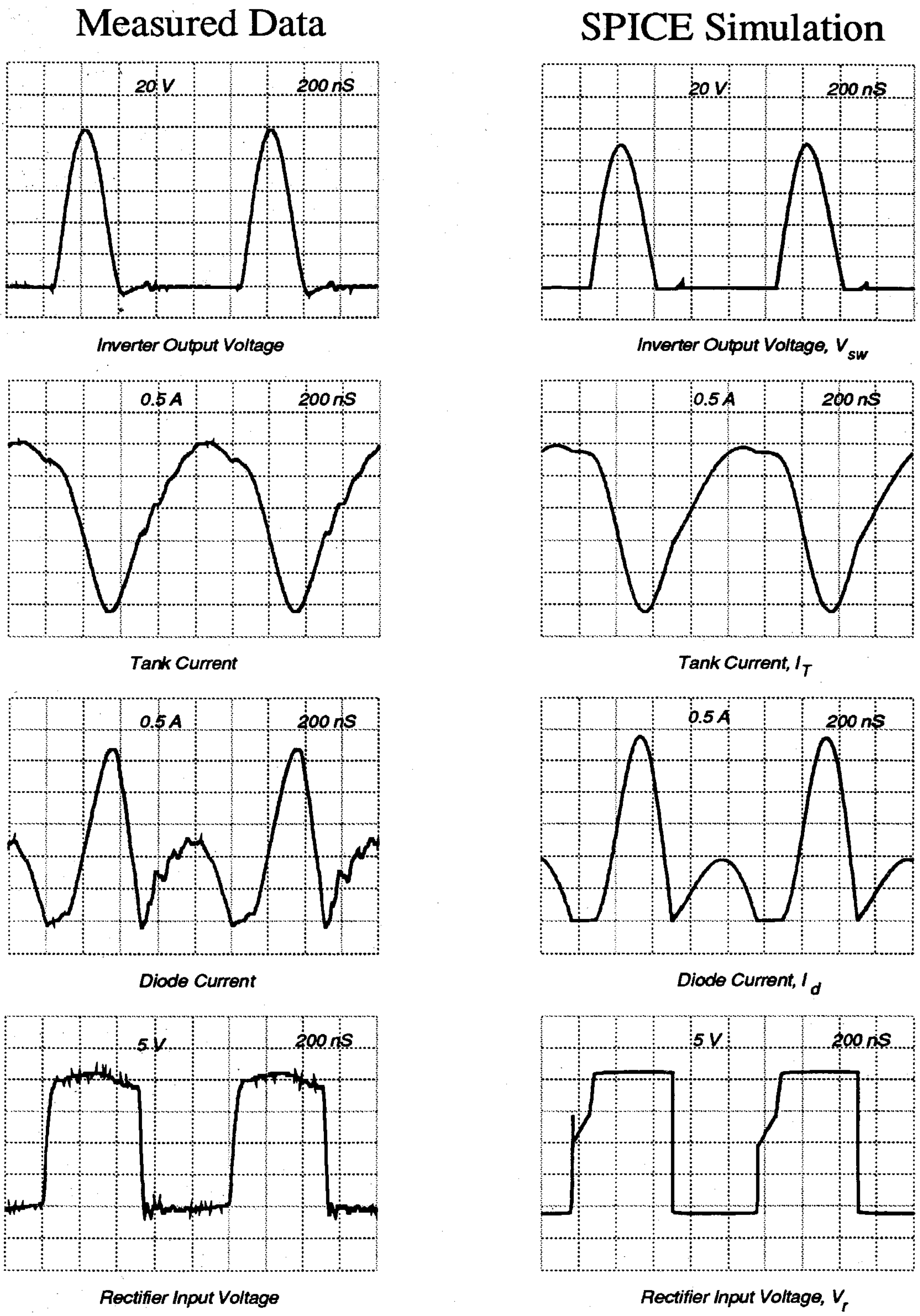


Figure 4.7: Equivalent Circuit of the Filament DC-to-DC Converter used for SPICE Simulation. The input inductor L_{RFC} and the output filter capacitor are given initial conditions to accelerate the convergence of the solution to the steady state. Even with the initial condition, the steady-state solution requires approximately 100 cycles of the switching frequency to be accurate.



Inverter Output Voltage

Inverter Output Voltage, V_{sw}

Tank Current

Tank Current, I_T

Diode Current

Diode Current, I_d

Rectifier Input Voltage

Rectifier Input Voltage, V_r

Figure 4.8: Comparison Between Measured and Simulated Performance of the Filament DC-to-DC converter.

4.2.2. The High Voltage Converter

Another application for the resonant DC-to-DC converter is in high voltage power supply design. One of the most significant challenges in the design of high voltage power supplies is that of the high voltage step-up transformer. This single component is usually the most expensive, heaviest and costliest item in the entire high voltage power supply. One time-honored method of eliminating this component is the voltage multiplier (VM) circuit. This circuit uses only capacitors and diodes to achieve the necessary high voltage, but in the past this circuit was restricted to low-power applications due to the high peak current stresses imposed on the diodes and the large capacitance values required for the capacitors. The former problem can be significantly reduced by supplying the VM circuit with a current source rather than the more conventional voltage source. The theory of operation of such a circuit has been recently published [17]. In addition, full-wave rectifier stages in the voltage multiplier further reduce the current requirements on the diodes. This variation on the basic VM is the subject of a patent [18] and a patent application [19].

The problem of the capacitance values in a VM circuit is greatly reduced by the high frequencies possible using the ZVS inverters as the power source. The capacitors in the VM that are nearest the source still have high AC currents in the improved designs, but the low capacitance values required make the use of monolithic ceramic or mica capacitors practical. These capacitor types have high current capabilities and low ESR losses.

The Capacitor Ladder High Voltage Converter

The improved voltage multiplier circuit described above can be synthesized by considering the characteristics of the normal bridge rectifier circuit. In the bridge rectifier the input current has no DC component which allows series capacitors to be added in each input line to the rectifier without changing the behavior of the circuit, as in Fig. 4.9. The AC output shown in the figure can be used to drive another stage exactly like the first

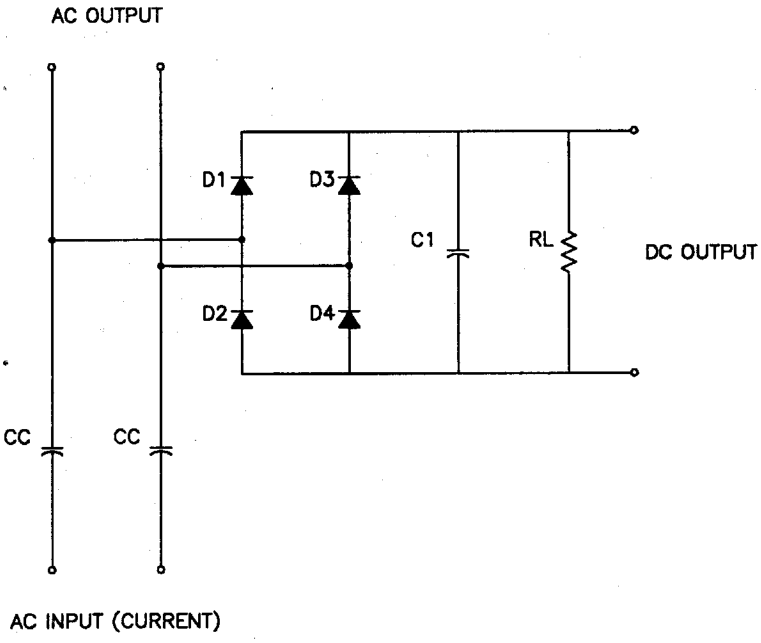


Figure 4.9: Bridge Rectifier with DC Isolation Between Input and Output. Since the current into a bridge rectifier has no DC component, the coupling capacitors do not alter the operation of the circuit if their reactance is made small compared to the other impedances in the circuit.

stage and so on. Since each stage has DC isolation between the input and the output grounds, the individual stages can be connected in series to form a high DC output voltage. An example of this technique is shown in Fig. 4.10 for three stages. This circuit can be a starting point to synthesize many other rectifier topologies. The only requirement for the rectifier circuit used in each stage of the capacitive ladder is that the input current must not have a DC component. The conventional VM circuit is a result if the rectifier used in each stage is a voltage doubler and some redundant components are eliminated. The voltage multiplier circuit shown above has difficulty in sharing the current equally between the stages as shown in [17]. One way to eliminate this problem is to insert a common-mode choke into each stage of the rectifier. The DC current in these chokes does not cause DC flux in the core because of the polarity of the windings, allowing these chokes to be made very small. The chokes force the current into each stage to remain sinusoidal, assuming that the input driving current is sinusoidal. It is possible to provide

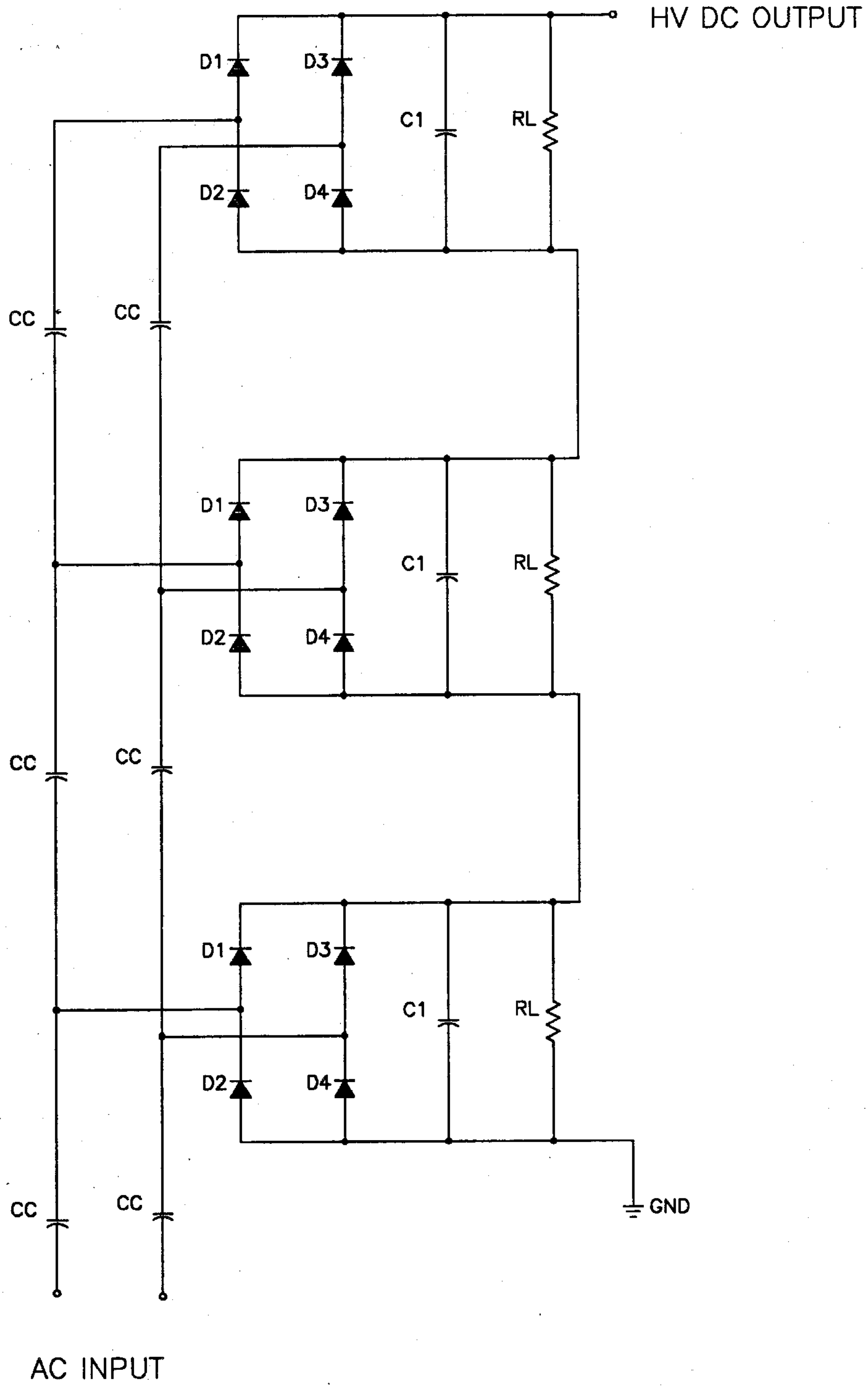


Figure 4.10: Three-Stage Capacitive Ladder Circuit. This circuit is a relative of the conventional voltage multiplier. The input coupling capacitors resemble a ladder which is the origin of the name of the circuit. This circuit has been built with as many as 13 stages.

intermediate output voltages from this circuit by connecting loads across the individual stages as required. If this is done, not all the stages will draw the same current from the source. Each stage will draw current proportional to the DC output current required from each stage. The resulting high performance capacitive ladder circuit is shown in Fig. 4.11.

The Inverter Selection

Since the goal is to generate high output voltage, the most reasonable design approach is to provide the highest output voltage from each stage as is possible, consistent with the voltage ratings of the components. This requirement usually makes the use of the Class E inverter unattractive for the main power source. In this example, the Class D ZVS inverter is much more appropriate because of the lower voltage applied to the switching transistors. In addition, the symmetrical nature of the Class D ZVS converter means the current imbalance problem observed in the filament power supply is greatly reduced.

The design of the inverter closely parallels the inverter design in the filament supply except that the load impedance on the inverter is chosen by using Fig. 2.8 (a). A working model high voltage power supply was constructed to meet the following requirements:

1. DC input Voltage: ±75 V
2. Output Voltage: 2,000 V
3. Output Power: 150 W
4. Switching Frequency: 800 kHz
5. Number of High Voltage Converter Stages: 8

The resulting design is shown in Fig. 4.12.

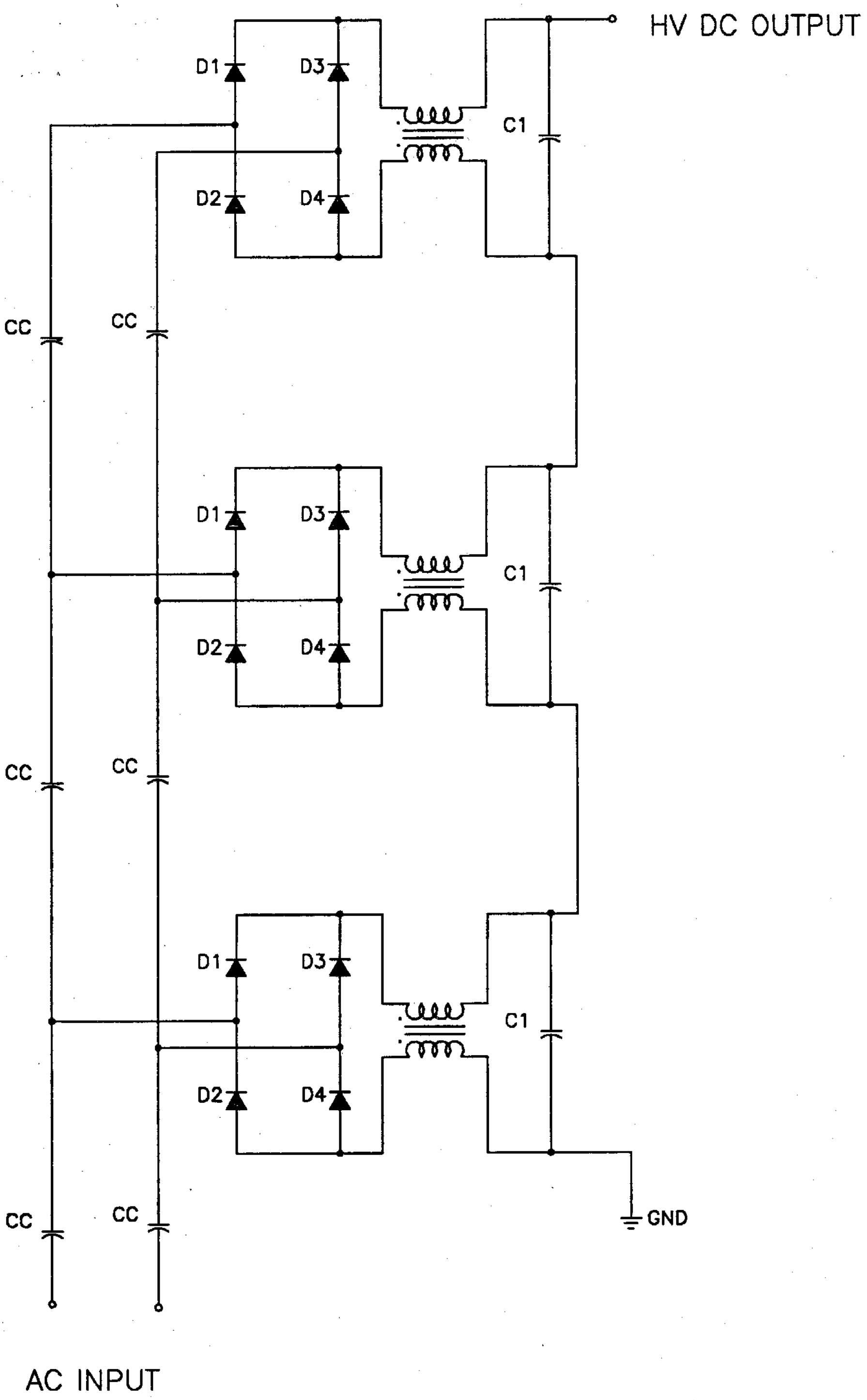


Figure 4.11: High Performance Capacitive Ladder High Voltage Converter. The common-mode chokes added to each stage force the stages to share the input current.

Measured Performance

Oscilloscope data showing the converter in several operation modes are presented in Fig. 4.13. The waveforms show the voltage across C_2 which is called V_{sw} and the tank current which is called I_T. The waveform in Fig. 4.13 (a) is the case for full output voltage of 2kV and full output current. Note that the current waveform has less even harmonic distortion than the filament supply had. The voltage waveform shows the ZVS condition. Figure 4.13 (b) is the same load as (a) but with the control current reduced to produce a 1 kV output voltage. This case still exhibits zero-voltage-switching. In Fig 4.13 (c), the load resistance was lowered well below the designed minimum value to demonstrate the behavior of the inverter in an overload condition. The jumps in the V_{sw} waveform clearly show that ZVS is not achieved. This condition does not result in a catastrophic failure of the inverter but the power dissipation in the MOSFET switches is high.

4.3 Conclusion

In this chapter, two applications of the resonant DC-to-DC converter utilizing a magnetic regulator have been presented. The unique characteristics of this family of converters makes them attractive for many applications, particularly those involving high voltage input-output isolation or high output voltage.

The theory of operation can be reduced to the case of the normal resonant DC-to-DC converter circuit for any particular value of the control current by inserting the magnetic regulator's equivalent circuit. The problem that remains is the dynamic model of such a system. The development of this model is the subject of Part II.

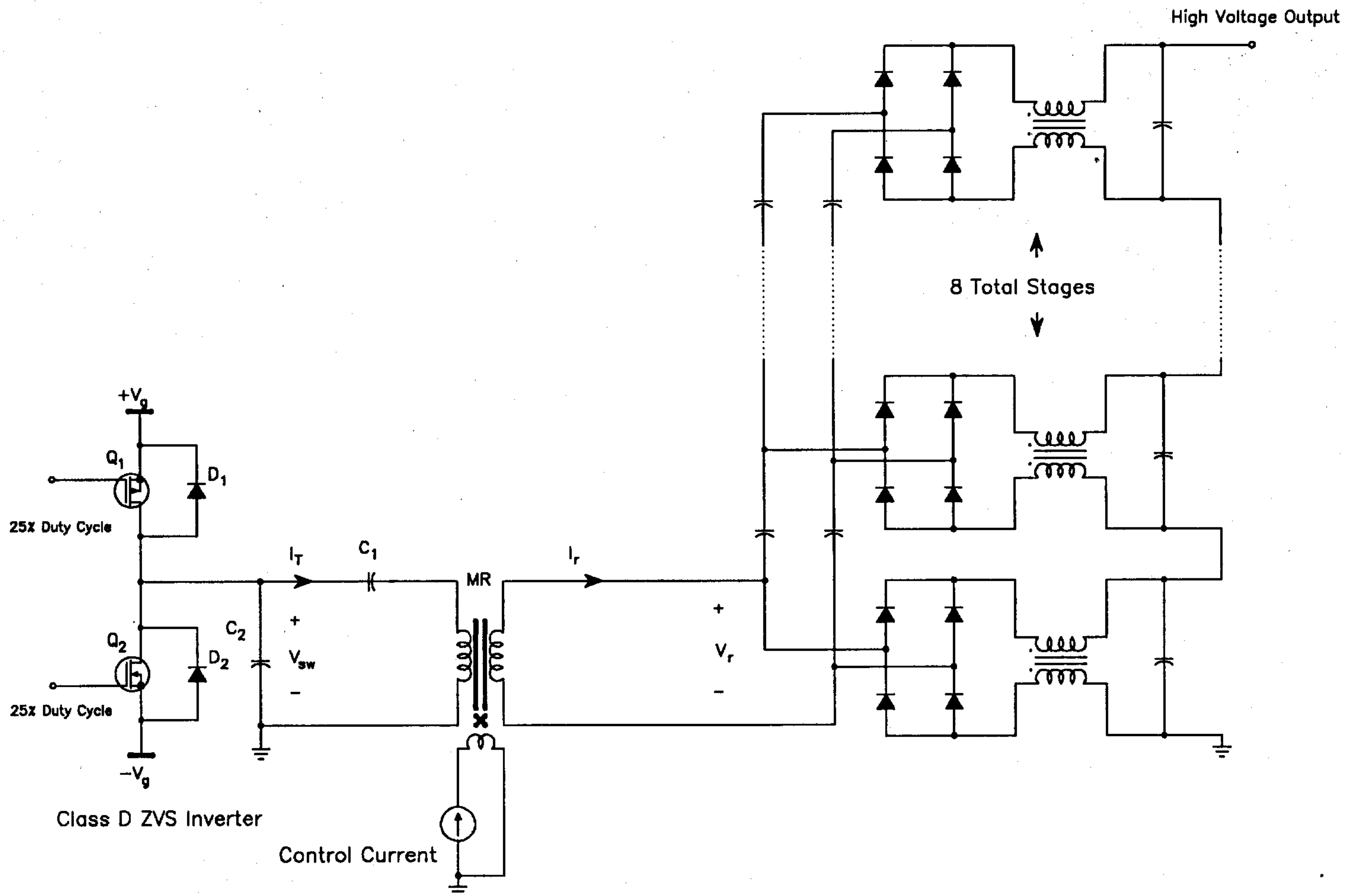
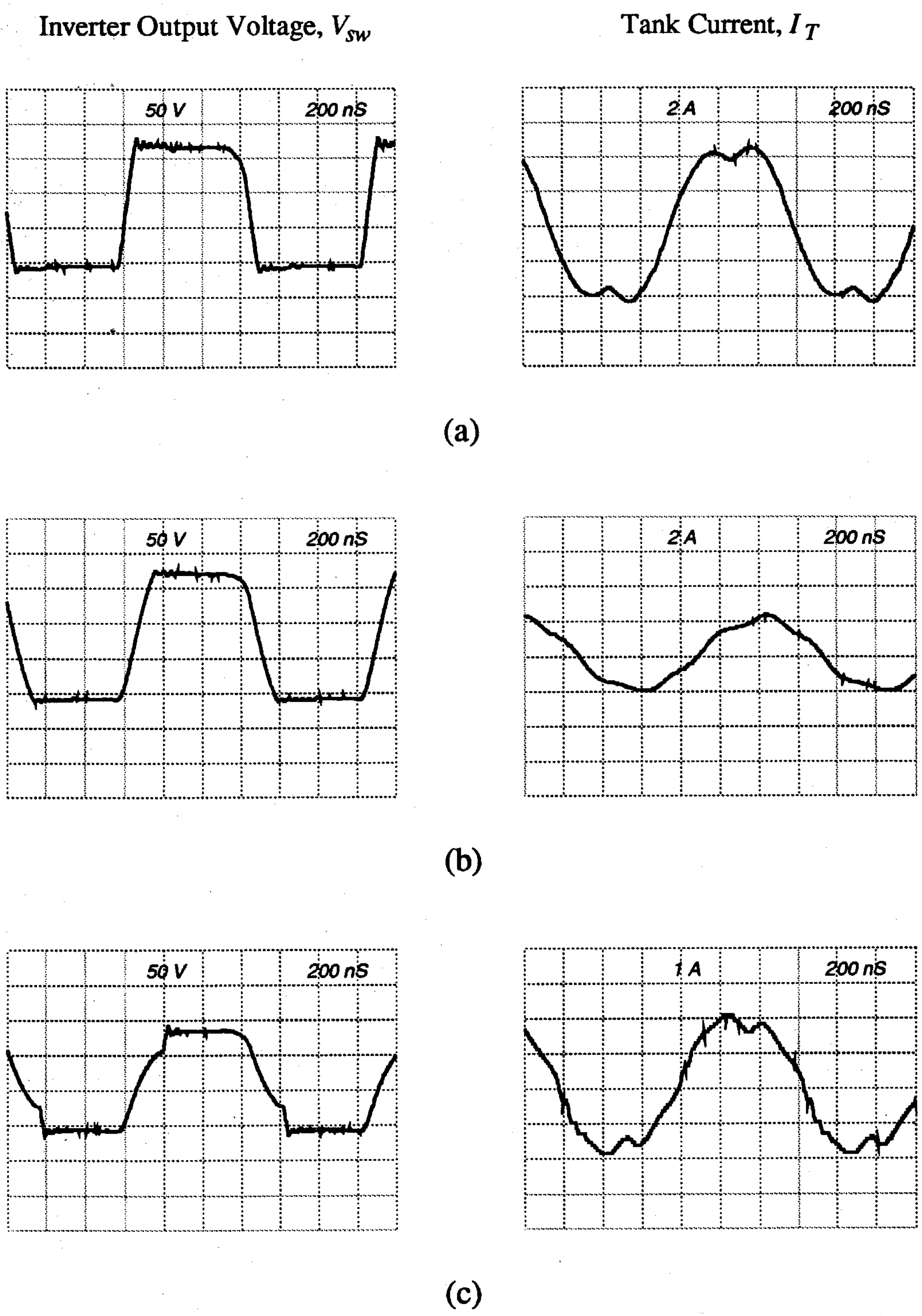


Figure 4.12: High Voltage Power Supply Using the Capacitive Ladder and the Class D ZVS Inverter.



Inverter Output Voltage, V_{sw}

Tank Current, I_T

Figure 4.13: Waveforms From the High Voltage Power Supply. (a) The control current is set to provide 2 kV output. This is the full output voltage condition. (b) The control is adjusted to provide 1 kV output. (c) The load is heavier than the designed maximum so ZVS is not achieved.

Part II

The Dynamic Solution

Chapter 5

The Envelope Problem

Introduction

In Part I the problem of the steady-state operation of the resonant DC-to-DC converter was addressed. This chapter begins the study of the dynamic characteristics of such a power system. In general, there are several functions which the designer will need to know in order to meet the design objectives. The control-to-output response is usually the first function of interest since it is the function which will be used to design a stable feedback loop. In the present case, the control port is the input current to the magnetic regulator's control winding and the output port is the DC output voltage. Clearly, the dynamic model of the magnetic regulator will be central to the feedback control problem. The other functions of interest are the input impedance (important in the design of any input filters), the output impedance (necessary to calculate the response to a step load change), and the line rejection ratio. The input here is the DC power input, not the control port. All these functions are used in the open-loop form since the closed-loop quantities are dependent upon the details of the compensation network. Therefore, the latter three functions do not depend upon the dynamic model of the magnetic regulator since they will be calculated with the control variable set to zero. In this chapter, the control-to-output transfer function will be considered with the discussion of the other functions being deferred to later chapters.

The magnetic regulator model developed in Part I will be the starting point for the dynamic magnetic regulator model. It is useful to consider the regulation of the

DC-to-DC qualitatively before any detailed calculations are carried out. Figure 5.1 illustrates the DC-to-DC converter in its simplest form: a source of sine wave energy (the inverter) driving a rectifier load through a series LC circuit. The L in this circuit may be a discrete inductor as in a conventional converter, in which case the regulation must be accomplished by varying the driving frequency. In the present case, the L may be the primary leakage inductance of the magnetic regulator. Then the regulation is accomplished by varying the value of the inductance thus changing the magnitude of the series impedance in the forward power path. The magnetizing inductance of the magnetic regulator has been absorbed into the rectifier block for the purposes of this discussion.

The tank current in Fig. 5.1 is approximated as a sine wave in the steady-state model and a low-frequency modulated sine wave in the dynamic case. The tank current is the 'link' in this circuit between the inverter and the rectifier. If the tank current is known, then the output voltage V_o can be determined. Likewise, a knowledge of the tank current will lead directly to the input current into the inverter. Since all the quantities of interest represent low frequency averages of the high frequency voltage and currents internal to the converter, it is the envelope of these internal signals that is important rather than the details of the high frequency waveform.

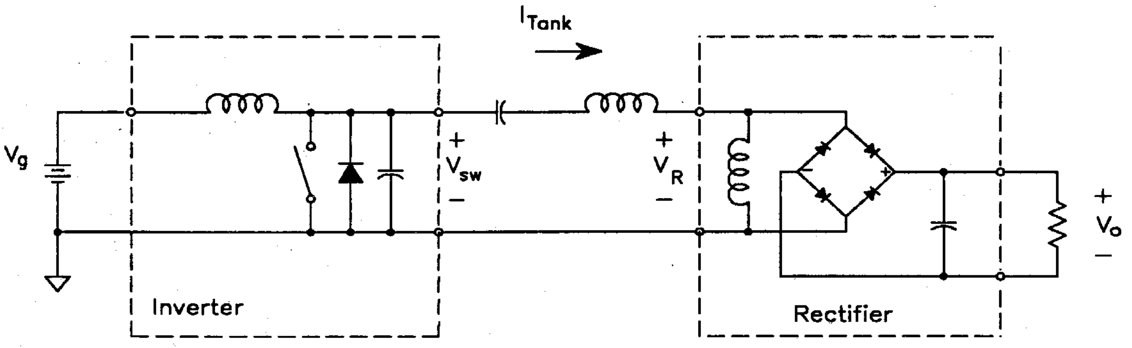


Figure 5.1: The DC-to-DC Converter Partitioned to Simplify the Calculation of the Tank Current.

The central problem of the dynamic solution of the DC-to-DC converter is the determination of the tank current and specifically its envelope. The tank current is immediately available if the voltages V_{sw} and V_R are known for the case of a linear, time-invariant inductor in the tank circuit. To solve for the tank current in the case of the magnetic regulator, a dynamic model for the *L*(*t*) inductance is required. In the following chapters the DC-to-DC converter model will be developed using progressively more accurate values for V_{sw} and V_R, coupled with the dynamic magnetic regulator model. Before undertaking the general case, simple linear components will replace the inverter and the rectifier so the dynamic model for the magnetic regulator can be separately derived and verified.

5.1 The *L*(*t*) Experiment

5.1.1 Verification of the *L*(*t*) Model

The magnetic regulator model derived in Part I contains a new type of circuit element: a time-varying inductor. This element makes the usual methods of circuit analysis difficult to apply since the Laplace transform depends upon the circuit being time-invariant. Special techniques are required to properly model the behavior of the magnetic regulator in an application like the sine wave HVPS.

Since the magnetic regulator is a new device with unknown properties, it would be best to construct a simple experiment to test the magnetic regulator under precisely controlled conditions. The simplest possible circuit to do this is illustrated in Fig. 5.2. In this circuit, V_c supplies a high frequency AC sine wave and R_s is the generator's source impedance. I_m supplies the control current to the magnetic regulator's control winding. The objective in this experiment is to vary the value of the DC control current and observe the behavior of the output voltage. As noted above, the output voltage V_o would be controlled by the magnitude of the tank current, which in turn is a function of the series impedance in the

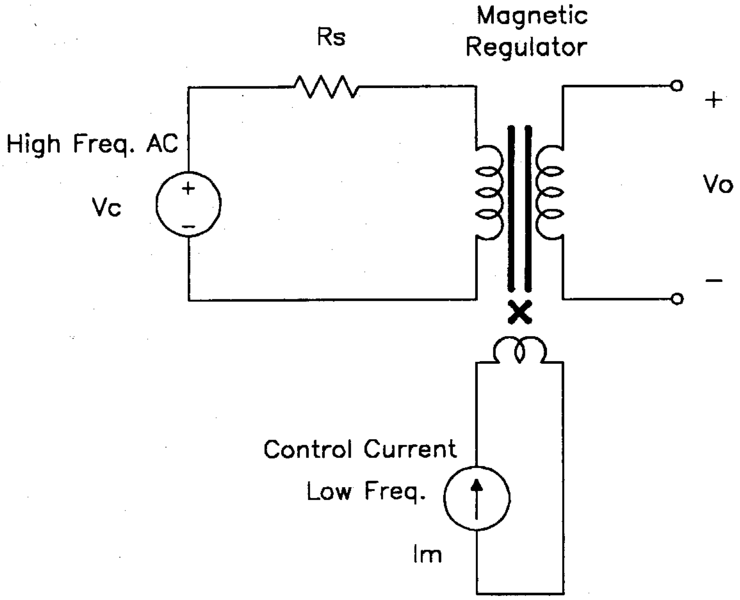


Figure 5.2: The Simplest Possible Test Circuit for the Magnetic Regulator. R_s is the generator's source impedance, V_s is a fixed source of sine waves and I_m is an input current. The output of interest is the amplitude of V_o.

tank circuit branch. Since the magnetic regulator's inductance appears like a normal inductance for a constant control current, one should expect the output voltage to be a function of this inductance and the DC current in the control winding.

If the equivalent circuit for the magnetic regulator is now inserted into Fig. 5.2, as shown in Fig. 5.3, the action of the control current is obvious at least for very low frequency variation of the control current. The output voltage is the result of a voltage divider between the magnetizing inductance L_m and the variable primary leakage inductance L_1. As the control current is increased, L_1 decreases which causes the output voltage to increase. In almost all practical cases, the inductor L_c is so large that its effect can be neglected. Further, since there is no output load, the secondary leakage inductance L_2 is not important.

The problem with the simple *L*(*t*) circuit as shown so far is that it is too simple; there will be no frequency dependence in the control-to-output transfer function at least until the

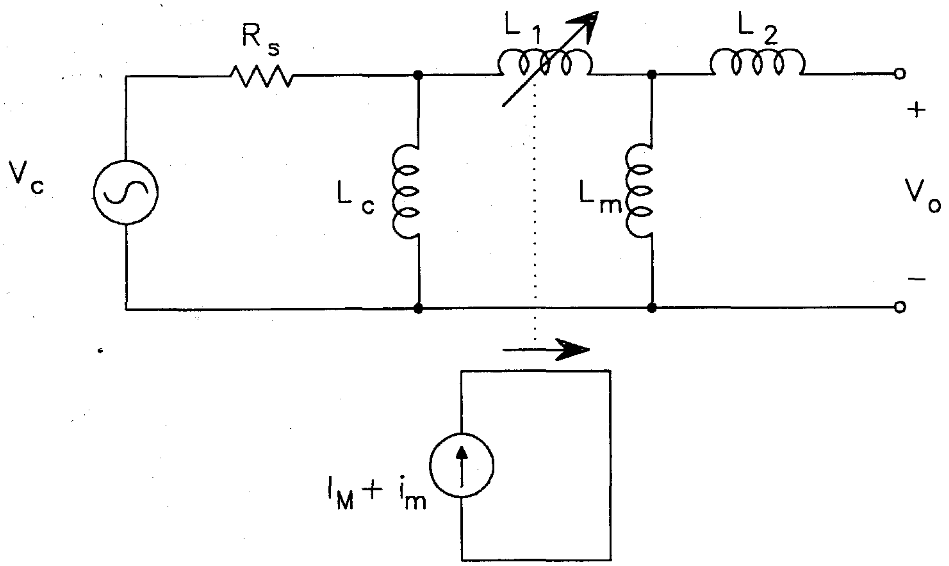


Figure 5.3: The Equivalent Circuit for the Simple $L(t)$ Circuit After Inserting the Model for the Magnetic Regulator Derived in Part I. The control current consists of a large DC value, I_M, and a small AC perturbation i_m. The source V_c is fixed in amplitude and relatively large (typically >10 VRMS).

control current modulation frequency gets very high. A more realistic test circuit is shown in Fig. 5.4. In this case an external capacitor has been placed across the secondary of the MR and the value chosen to resonate with the MR near the frequency of the input AC source V_c. Qualitatively, this circuit modulates the output by a somewhat different mechanism compared to the first circuit. The MR and capacitor combination can be thought of as a narrow bandpass circuit where the center frequency can be tuned by the MR's control current. If the AC source frequency is near the bandpass center frequency, one would expect that very small changes in the MR's control current would result in rapid changes in the output signal amplitude.

A few more qualitative observations can be made about this circuit. Since *increasing* the control current *decreases* the inductance in the MR, the resonant frequency of the network should *increase*. If the AC input frequency is below the network's resonant fre-

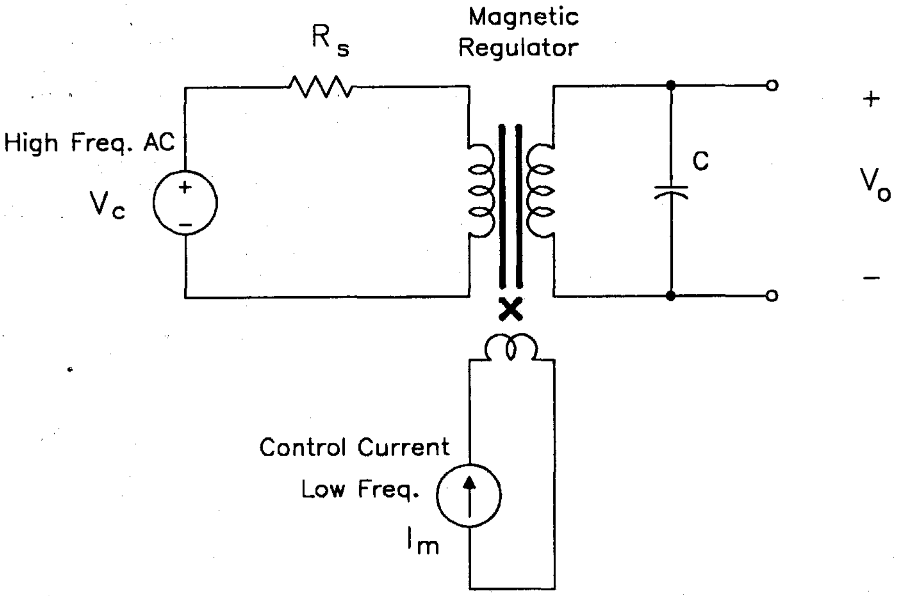


Figure 5.4: Prototype L(t) circuit. The addition of the capacitor C across V_0 will introduce a frequency dependence to the output-amplitude-to-control-current transfer function.

quency, *increasing* the control current should *decrease* the output signal amplitude. This means that the control to output characteristic is inverting. Similarly, if the input AC signal is above the network's resonant frequency, increasing the control current should increase the output signal amplitude which is a non-inverting control characteristic.

If the control current is slowly varied sinusoidally around a DC value, then the output signal will be a high frequency AC signal with a low frequency amplitude modulation. Because of this apparent AM modulation, the terminology used to describe this circuit will be borrowed from communications theory. This AC input source will hereafter be referred to as the carrier frequency input. As a more quantitative model is developed for this circuit, we should expect to find that the output signal consists not only of the carrier frequency, but also sidebands above and below the carrier by an amount equal to the modulation frequency.

5.1.2 Meaning of the Frequency Response

Since the circuit under consideration contains several frequencies, the question arises as to what is meant by the frequency response. Consider a concrete example where the carrier frequency is supplied by a signal generator at 100 kHz. The control current is modulated by a 100 Hz AC perturbation. The output from the MR would be expected to contain a large signal at 100 kHz (the carrier) plus much smaller signals at 100.1 kHz (the upper sideband) and 99.9 kHz (the lower sideband) as a result of the AM modulation of the carrier frequency. Normally the frequency response of a linear network would be the quotient of two complex phasors which contain the magnitude and phase information. These phasors each multiply a complex representation of the signal frequency usually of the form $\exp(j\omega t)$. But in this case there are at least four frequencies to choose from.

The resolution of this dilemma comes from a consideration of the final application. In the DC to DC converter, the output AC voltage will be rectified and filtered to provide DC power to the load. This DC voltage will also be sampled by a feedback circuit, and the result will be compared against a reference voltage to generate an error voltage. This error voltage will be used to generate the control current, so it is the rectified and filtered MR output voltage which will be of interest. A slightly more general approach will be used here. The AC output voltage will be detected (rectified) by some non-linear circuit, which is yet to be defined, and the resulting signal will have the carrier frequency and higher frequencies removed (filtered). The exact details of the filtering are unimportant since a simplifying assumption will be made that all frequencies near or above the carrier frequency will be completely removed by the filter. Since in the practical case the carrier frequency is usually an order of magnitude higher than the modulation frequency, this assumption is well justified. Figure 5.5 graphically illustrates the process described above.

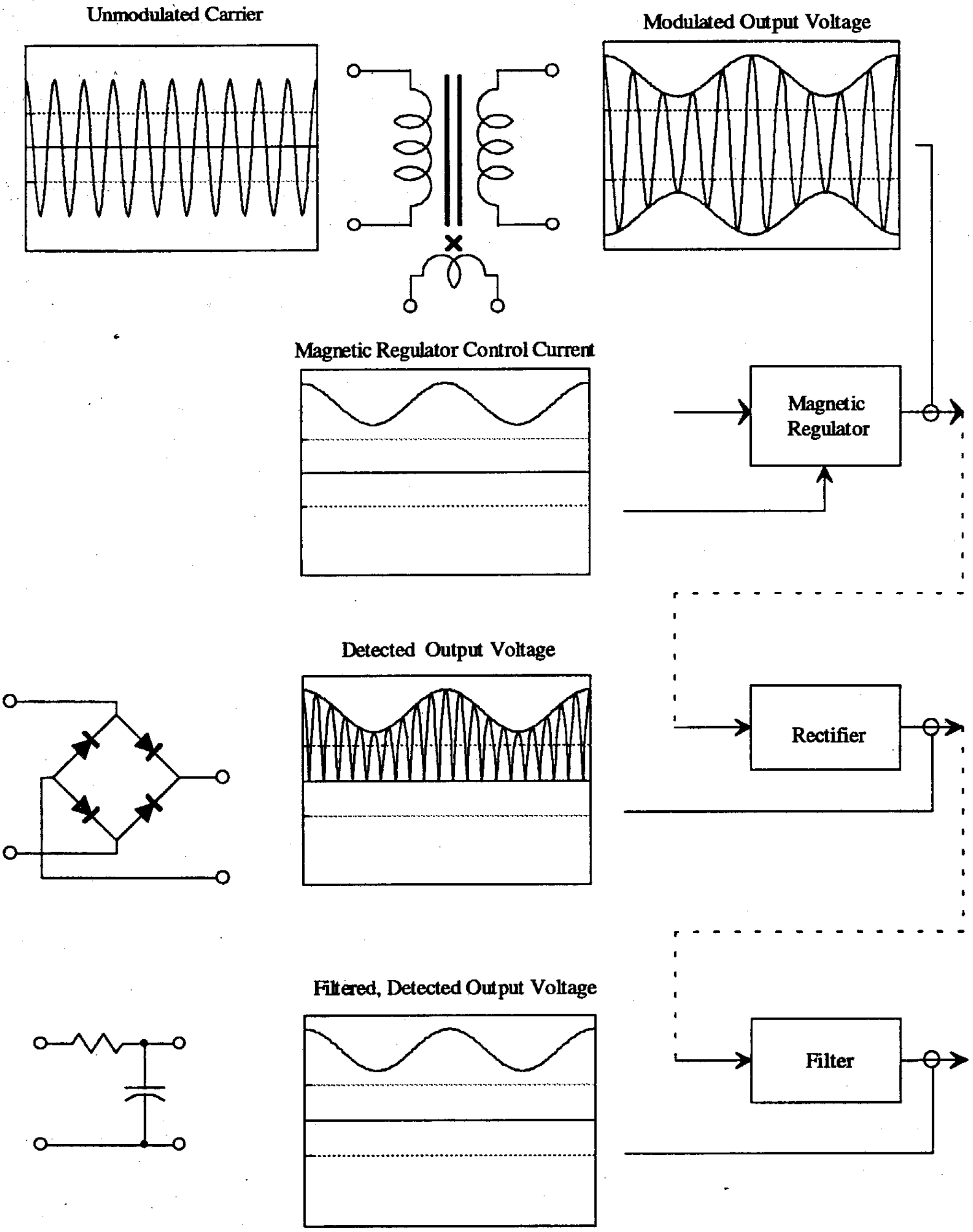


Figure 5.5: The basic signals involved in the $L(t)$ Experiment. The source signal is a fixed amplitude, high frequency sine wave and the control input is a DC signal with a small, low frequency modulation. This results in amplitude modulation at the secondary terminals of the magnetic regulator. The output of the magnetic regulator is rectified and filtered to produce a DC output with a small AC modulation.

As illustrated in the figure, if the output from the detector is considered the system output, and the input to the control winding is considered the system input, the frequency response can be unambiguously defined. Even though the magnetic regulator is not a linear, time-invariant circuit, the 'black box' containing the magnetic regulator and the rectifiers and filter can be viewed externally as a linear circuit and thus this 'box' can be included in a linear feedback regulator.

5.1.3 The Small-Signal Model for the Magnetic Regulator

In Chapter 3 the model for the MR was shown to contain four inductors, three of which are normal, linear inductors and one which is a current-controlled inductor. Since this current-controlled inductor is the only unusual element, the model development will focus on it first. Consider a single variable inductor whose inductance is dependent upon a control current I_m (modulation). Further assume that the control current is a large DC value with a small AC perturbation, $I_m = I_M + i_m$. The inductor will be represented as $L(t) = k_{DC} I_M + k_L i_m$ where the nonlinear relationship between the current and the inductance has been linearized about the DC operating point. Equivalently, the inductance can be represented as

$$L(t) = L_0 + \hat{L} \tag{5.1}$$

where $\hat{L}$ is a small AC perturbation in the inductance. The fundamental relationship for the inductor voltage comes from Faraday's law,

$$\oint_c \mathbf{E} \cdot d\mathbf{l} = \frac{d}{dt}\left(\iint_s \mathbf{B} \cdot d\mathbf{a}\right) \tag{5.2}$$

where c is a closed curve bounding the surface s. The surface integral on the right is equal to the magnetic flux φ. The voltage, *v*, on a coil of wire using *n* turns enclosing the flux φ, can be evaluated with the line integral on the left where the curve c is chosen to coincide with the wire. The voltage becomes

$$v = n\frac{d\varphi}{dt} \tag{5.3}$$

The usual relation for the voltage on an inductor is

$$v = L\frac{di}{dt} \tag{5.4}$$

From these two equations we can see that the inductance is

$$L = \frac{n\varphi}{i} \tag{5.5}$$

It is this definition of inductance that must be used if *L* is not a constant. The more general form for the inductor voltage law, which accounts properly for a variable inductance is then

$$v = \frac{d}{dt}(Li) \tag{5.6}$$

The chain rule transforms this equation into

$$v = L(t)\frac{di}{dt} + i(t)\frac{dL}{dt} \tag{5.7}$$

Note that the first term in this equation is still not the usual inductor voltage law since the inductance is a function of time. Now inserting 5.1 into 5.7 we get

$$\begin{aligned} v &= L_0\frac{di}{dt}+\hat{L}\frac{di}{dt}+i(t)\frac{d(L_0+\hat{L})}{dt} \\ &= L_0\frac{di}{dt}+\hat{L}\frac{di}{dt}+i(t)\frac{d\hat{L}}{dt} \\ &= L_0\frac{di}{dt}+\frac{d(\hat{L}\cdot i)}{dt} \end{aligned} \tag{5.8}$$

This equation can be further simplified by observing that $\hat{L} = k_L i_m$ to yield

$$v = L_0\frac{di}{dt}+k_L\frac{d(i_m\cdot i)}{dt} \tag{5.9}$$

This is the basic equation used to model the time-varying inductor. The first term is a normal, fixed inductor whose value is the average value of the time-varying case and the second term contains all the new effects caused by the time-varying inductance. A circuit model for this device is shown in Fig. 5.6. All the unusual effects caused by the time-varying inductance have been gathered together and included in the voltage source V_a. This voltage source is similar to an AM modulator since a multiplication of signals takes place.

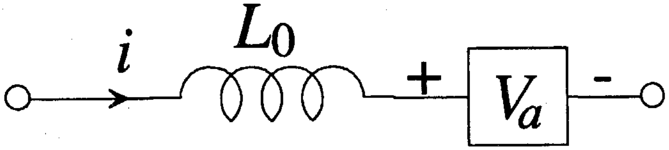


Figure 5.6: Equivalent Circuit for an L(t). All the special effects caused by the time-varying inductance have been collected into the dependent voltage source, V_a.

The complete model of the magnetic regulator can now be constructed as shown in Fig. 5.7. The time-varying inductance $L_1(t)$ has been replaced by an averaged inductance L_0 and the voltage source V_a.

$$V_a = k_L \frac{d(i_m \cdot i)}{dt} \tag{5.10}$$

The simple prototype circuit described above can now be solved by inserting this equivalent circuit in place of the magnetic regulator.

In equation 5.10, the current i is the total current flowing through the branch containing the time-varying inductor. This current will include not only the carrier frequency components, but also sidebands equally spaced above and below the carrier by integer multiples of the carrier frequency. Since the goal of the present analysis is a small-signal model suitable for a stability analysis, some simplifications can be made. With the modulation assumed to be small, the sideband amplitudes will be much smaller than the carrier amplitude.

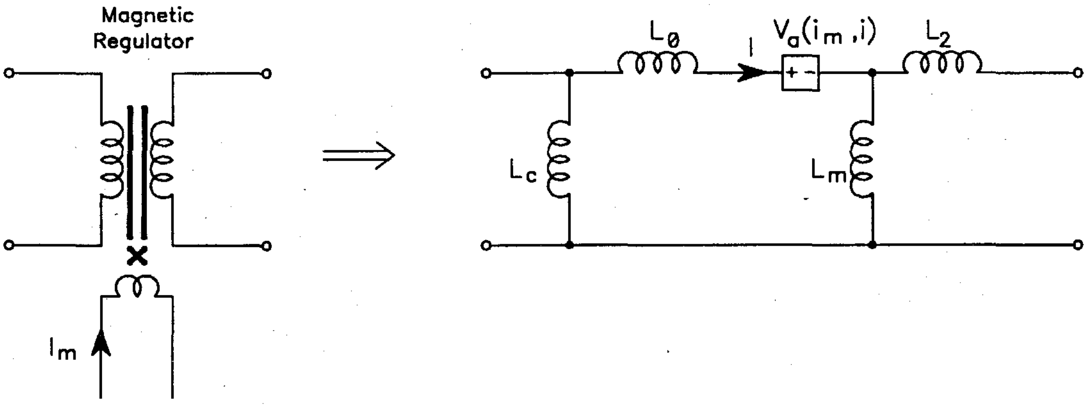


Figure 5.7: Schematic Symbol and Small-Signal Equivalent Circuit of the Magnetic Regulator. The dependent voltage source V_a accounts for the flux-steering action in the magnetic regulator's core.

Consider that the current i is composed of a carrier frequency signal and an upper and lower sideband signal,

$$i = i_c + i_{LSB} + i_{USB} \tag{5.11}$$

The equation for V_a becomes,

$$\begin{aligned} V_a &= k_L \frac{d(i_m \cdot (i_c + i_{LSB} + i_{USB}))}{dt} \\ &= k_L \frac{d}{dt}(i_m \cdot i + i_m \cdot i_{LSB} + i_m \cdot i_{USB}) \end{aligned} \tag{5.12}$$

where

$$\begin{aligned} i_{LSB} &= i_c - \hat{i}_m \\ i_{USB} &= i_c + \hat{i}_m \end{aligned}$$

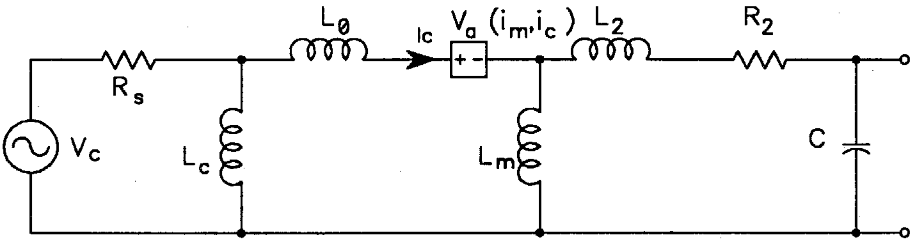
The signals at the upper and lower sidebands are assumed to be small, as is the modulating current so the second and third terms will be neglected. The equation for V_a is now simplified to read,

$$V_a = k_L \frac{d}{dt}(i_m \cdot i_c) \tag{5.13}$$

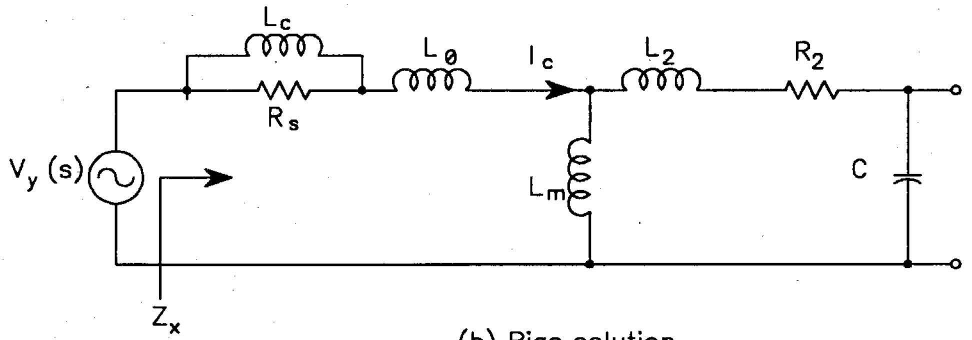
With this simplified form for V_a, the calculation does not involve the simultaneous solution of several equations as would be required in the general case since both i_m and i_c can be considered inputs.

5.1.4 Calculation of the Predicted Response Using the Equivalent Circuit Method

The analysis of the MR circuit follows several stages. First, the 'operating point' must be calculated which amounts to calculating the carrier-frequency current in the time-varying element $L_1(t)$. The AC current in L_1 can then be used to determine the amplitude of the source V_a. The source V_a then drives the narrowband circuit of Fig. 5.8 (a) which filters and couples the signal to V_o. Finally, V_o is detected and the resulting low-frequency envelope is presented at the output. The desired frequency response is the ratio of this detection to the input current perturbation.



(a) L(t) Circuit



(b) Bias solution

Figure 5.8: L(t) Experiment (a) Equivalent Circuit and (b) Circuit Used for the Operating Point Calculation.

Bias Point Calculation

The first step in the analysis is to determine the carrier frequency current in $L_1(t)$. For this part the modulation is turned off by setting $i_m = 0$, so that $L_1(t)$ becomes the normal inductor L_0. The current in L_0 is then determined from circuit analysis. The circuit of Fig. 5.8 includes one parasitic resistance which improves the agreement between measurements and calculations. This one parasitic resistance, R_2, could be considered winding resistance. This particular resistor was chosen to break up the undamped output L-C loop. Although other parasitic elements are present, they would be expected to have less effect since they would not be interrupting an undamped loop (a supposition supported by measurements as seen below).

The carrier frequency current in L_0 is given by

$$i_c = \frac{V_y}{Z_x} \tag{5.14}$$

where V_y is the Thevinin equivalent source voltage of V_c driving R_s and L_c, and Z_x is the load impedance seen by the Thevinin source (see Fig 5.8 (b)). V_y is given by

$$V_y = \frac{sL_c}{R_s + sL_c} \cdot V_c \tag{5.15}$$

and

$$Z_x = R_s \| L_c + sL_0 + sL_m \| \left(sL_2 + R_2 + \frac{1}{sC} \right) \tag{5.16}$$

$$Z_x = \frac{N_1 s + N_2 s^2 + N_3 s^3 + N_4 s^4}{(R_s + sL_c)\left[1 + sR_2C + s^2(L_m + L_2)C\right]} \tag{5.17}$$

where

$$N_1 = (L_c + L_0 + L_m)R_s$$

$$N_2 = L_0L_c + L_mL_c + R_sR_2C(L_c + L_0 + L_m)$$

$$N_3 = R_sC\left[(L_0 + L_c)(L_m + L_2) + L_mL_2\right] + R_2CL_c(L_0 + L_m)$$

$$N_4 = C\left[L_0L_c(L_m + L_2) + L_mL_2L_c\right]$$

For any given MR, this expression for Z_x should be simplified, but the complete expression is used here so that any numerical values for the inductances can be used. There are several limiting cases which can be tested using this complete formula.

The value for i_c is

$$\begin{aligned} i_c &= \frac{V_y}{Z_x(s)} = \frac{1}{Z_x(s)} \cdot \frac{sL_c}{R_s + sL_c} V_c \\ &= G_1(s) \cdot V_c \end{aligned} \tag{5.18}$$

where we must use $s = j\omega_c$ to get the current at the carrier frequency.

AM Source Amplitude

Given the value of the carrier current in $L_1(t)$, the value of the AM source V_a can be calculated from equation 5.13. Since this equation involves the derivative of a product of functions (a clearly non-linear operation), the phasor form of the signals is not appropriate. The true form of the signals must be used:

$$I_c = i_c \cos(\omega_c t + \varphi_c) \tag{5.19}$$

and

$$I_m = i_m \cos(\omega_m t) \tag{5.20}$$

The current I_m is considered an input so we are free to set its phase shift to zero. Now, using equation 5.13 to evaluate V_a, we find:

$$\begin{aligned} V_a &= k_L \cdot \frac{d}{dt}\left[i_m \cos(\omega_c t + \varphi_c) \cdot i_c \cos(\omega_m t)\right] \\ &= k_L \frac{d}{dt}\left\{\frac{i_m i_c}{2}\left[\cos\left[(\omega_c + \omega_m)t + \varphi_c\right] + \cos\left[(\omega_c - \omega_m)t + \varphi_c\right]\right]\right\} \\ &= k_L \frac{i_m i_c}{2}\left[-\omega_u \sin(\theta_u) - \omega_l \sin(\theta_l)\right] \end{aligned} \tag{5.21}$$

where

$$\begin{aligned} \theta_l &= (\omega_c - \omega_m)t + \varphi_c \\ \theta_u &= (\omega_c + \omega_m)t + \varphi_c \\ \omega_l &= \omega_c - \omega_m \\ \omega_u &= \omega_c + \omega_m \end{aligned}$$

It is useful to observe that the above equation can be written as

$$V_a = k_L \frac{i_m i_c}{2} \operatorname{Re}\left[j\omega_u e^{j\theta_u} + j\omega_l e^{j\theta_l}\right] \tag{5.22}$$

The complex exponential above forms the basis of using complex notation once again. From this point forward in the analysis, the circuit manipulations are done on linear, time-invariant circuits so phasor notation is justified. The computations are carried out separately for each frequency making it necessary to keep track of which frequency is being considered. This means that while normal circuit analysis would use the single complex variable s, this case will involve three such complex variables, s_c, s_u, and s_l corresponding to the carrier frequency, upper sideband frequency, and lower sideband frequency respectively. All three frequencies are present in the circuit simultaneously, but due to the linearity of the equivalent circuit, each frequency can be considered independently. With this in mind, the source voltage will be written as

$$V_a = k_L \frac{i_m \boldsymbol{i}_c}{2}(s_u + s_l) \tag{5.23}$$

where $\boldsymbol{i}_c$ is to be interpreted as the complex phasor carrier current with magnitude i_c and phase φ_c. This expression is analogous to phasor notation in ordinary linear circuit analysis. Consider the following example:

$$v_1(s) = Z_1(s) i_1(s) \tag{5.24}$$

The real-world current is

$$i_1(t) = \mathrm{Re}\left[i_1(j\omega) \cdot e^{j\omega t}\right] \tag{5.25}$$

The real current is calculated by multiplying an implicit complex frequency factor by a complex number which contains the magnitude and phase information about i_1 and then taking the real part. The voltage is similarly calculated from the real part of a complex product of i_1 and Z_1 multiplied by the same implicit complex frequency factor:

$$v_1(t) = \mathrm{Re}\left[Z_1(j\omega) \cdot i_1(j\omega) \cdot e^{j\omega t}\right] \tag{5.26}$$

By convention in normal circuit analysis, the complex frequency factor and the real-part function are omitted. The present situation is similar except that the implicit frequency factor must be chosen to coincide with the particular signal of interest. If one wanted the signal at the lower sideband frequency, the implicit complex frequency factor would be $e^{j\omega_l t}$.

Similarly, in the case of V_a in equation 5.13, if the lower sideband signal were of interest, the actual result would be

$$v_{LSB}(t) = \mathrm{Re}\left[k_L \frac{i_m i_c}{2} \cdot j\omega_l \cdot e^{j\omega_l t} \right] \tag{5.27}$$

Using linearity, the output voltage at each of the three frequencies can be determined.

Network Frequency Response

To determine the sideband components in the output, the transfer function from the source V_a to the output voltage V_o is required. A convenient way to determine V_o is to first determine i_1 as in Fig 5.9. Note that Z_x is the same as previously calculated above.

$$i_1(s) = -\frac{V_a(s)}{Z_x(s)} \tag{5.28}$$

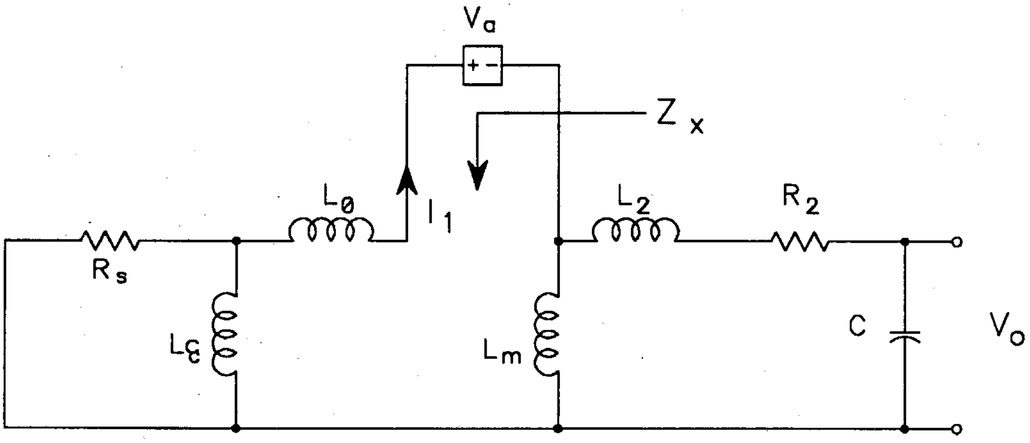


Figure 5.9: AC Equivalent Circuit for the *L*(*t*) Experiment. This circuit solves for the upper and lower sideband components in the output voltage V_0.

V_o can now be easily calculated from i_1:

$$V_o = \frac{1}{sC} \cdot \frac{sL_m}{sL_m + sL_2 + R_2 + \frac{1}{sC}} \cdot i_1 \tag{5.29}$$

$$V_o = \frac{sL_m}{1 + sR_2C + s^2C\,(L_m + L_2)} \cdot i_1 \tag{5.30}$$

or simply,

$$V_o = Z_a \cdot i_1 \tag{5.31}$$

The result of combining equations 5.13, 5.28, and 5.31 is:

$$V_o(s) = \frac{Z_a(s)}{Z_x(s)} \cdot \frac{k_L i_m}{2} \cdot s \cdot G_1(s_c) \cdot V_c \tag{5.32}$$

In this equation s will be set to s_u to evaluate the upper sideband component of V_o and to s_l to evaluate the lower sideband component. The total output voltage becomes

$$V_{total} = V_{USB} + V_{LSB} + V_{oc} \tag{5.33}$$

where

$$V_{USB} = V_o(s_u)$$

$$V_{LSB} = V_o(s_l)$$

V_{oc} represents the carrier frequency component at the output given by:

$$V_{oc} = Z_a(s_c) \cdot G_1(s_c) \cdot V_s \tag{5.34}$$

Output Detection

The total output voltage now resembles an amplitude modulated carrier signal with one difference: the upper sideband is not the same as the lower sideband. This adds considerable complexity to the process of detection (analytically) since no simple trigonometric transformation exists which can recover the low frequency envelope. To clarify this point consider the case of ordinary amplitude modulation:

$$V_{AM} = A \cdot \left[1 + m\cos(\omega_m t + \varphi_m)\right] \cdot \cos(\omega_c t) \tag{5.35}$$

In this form the amplitude of the carrier without modulation would be *A* and the modulation index would be *m*. The subscript m refers to modulation and the subscript c refers to the carrier. If *m* is small compared to one, this would look like a high frequency sine wave with a low frequency envelope of modulation as in Fig. 5.5. Recovering the low frequency modulation from this signal can be done by inspection; it is of magnitude *m* and phase shift φ_m. The phase shift is with respect to t = 0 and is easy to identify from this equation, but meaningless if one were observing the waveform on an oscilloscope. However, the phase shift is meaningful if there are several modulated waveforms that can be compared.

One can expand equation 5.35 to view the component frequencies by using a simple trigonometric identity:

$$\cos x \cos y = \frac{1}{2}\cos(x+y) + \frac{1}{2}\cos(x-y) \tag{5.36}$$

If we apply this identity to equation 5.35 we find:

$$V_{AM} = A\cos(\omega_c t) + \frac{mA}{2}\left\{\cos\left[(\omega_c + \omega_m)t + \varphi_m\right] + \cos\left[(\omega_c - \omega_m)t - \varphi_m\right]\right\} \tag{5.37}$$

This form shows that the sidebands are equal in magnitude with phases that are negatives of one another. If one had a signal containing a carrier frequency and two equal sidebands, the low frequency modulation could be easily recovered using this form. The condition that the sidebands be equal in magnitude is a requirement for this simple method and it is a condition that is not met in the *L*(*t*) problem, indicating a more involved analysis is in order.

The process of detecting the low frequency modulation in the output voltage is performed by a rectifier circuit when the MR is used in its intended application, DC to DC power conversion. Depending on the details of the rectifier, the low frequency output from the rectifier is sensitive to either the peak or average of the rectified high frequency signal. A bridge rectifier with a capacitive input filter is typical of a peak-responding detector while the same bridge rectifier with an inductive input filter is sensitive to the average value of the rectified waveform. Provided the modulation amplitude is small, the difference between a peak-responding detector and an average responding detector would be the peak-to-average ratio for a sine wave, which is 2/π.

The analytical equivalent of the rectification process is to first take the absolute value of the AC output voltage then either sample the peak values of the resulting unipolar waveform (in the case of the peak-responding rectifier) or average the waveform over each half cycle. Either approach yields a sampled-data representation of the low frequency modulation. If the solution to the *L*(*t*) circuit were simply amplitude modulated, either of these methods would be effective (although unnecessary since the trigonometric identity could be used in that case), but due to the unbalanced sidebands in the solution, there is phase modulation in addition to amplitude modulation. This causes the zerocrossing point to modulate around 2π thus making the absolute value difficult to calculate analytically.

A different approach to the detection step is useful. A common method of detecting an amplitude modulated signal in communications is to use a synchronous detector consisting of a balanced mixer and a local oscillator tuned to the carrier frequency, as shown in Fig. 5.10. The low pass filter (LPF) on the output of the mixer rejects the high frequency

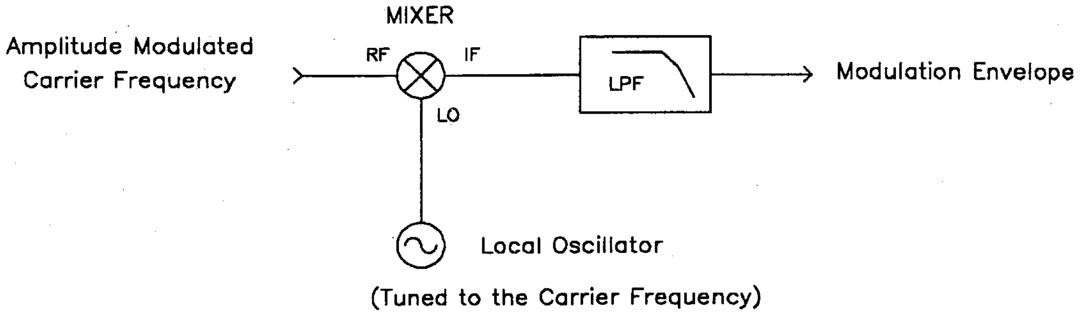


Figure 5.10: A Common Method used to Recover Low-Frequency Modulation from a High-Frequency Carrier. The local oscillator is at the same frequency as the carrier signal. For maximum signal out, the LO should also have the same phase as the carrier.

products out of the mixer (primarily twice the carrier frequency) and passes the low frequency modulation. This process will recover the same information as the other detectors described above, but has the added advantage that the analytical equivalent process can be carried out even on a waveform such as is produced by the $L(t)$ circuit.

The major drawback to using the synchronous detector is the requirement that the phase shift of the local oscillator be adjusted to match the carrier frequency phase at the input to the detector. (This procedure is not strictly necessary, but the signal strength is maximized if the carrier frequency and the local oscillator frequency are in phase.) There are receiver circuits which employ phase locked loops which will perform this function automatically. Nevertheless, for the present purpose an easier approach is shown below.

If the carrier frequency itself is used as the local oscillator to the mixer, then the phase shift is automatically equal to zero. This can also be thought of as taking the square of the modulating signal of interest. An x^2 detector is relatively simple to fabricate in the laboratory. For this reason, the x^2 detector will be used both analytically and experimentally in the $L(t)$ experiment.

The analytical equivalent of the x^2 detection process is first squaring the desired signal, then applying a low pass filter to the result. The LPF function can be conveniently performed by taking a Fourier series of the product and selecting the first harmonic (the DC term would be the DC output of the rectifier circuit which is not needed for the small-signal analysis). The result of the calculation is given below. Assume the signal is in the form of the following equation:

$$V_0(t) = v_{co}\cos(\omega_c t + \varphi_c) + v_{USB}\cos\left[(\omega_c + \omega_m)t + \varphi_{USB}\right] + v_{LSB}\cos\left[(\omega_c - \omega_m)t + \varphi_{LSB}\right] \tag{5.38}$$

This equation can also be considered to be in the complex form as in 5.39

$$V = V_{co} + V_{USB} + V_{LSB} \tag{5.39}$$

Where

$$V_{co} = v_{co}e^{j\varphi_c}$$

$$V_{USB} = v_{USB}e^{j\varphi_{USB}}$$

$$V_{LSB} = v_{LSB}e^{j\varphi_{LSB}}$$

Each term in this equation is a complex number representing the magnitude and phase of each respective component frequency. The detector computation uses the upper and lower sideband signals referenced to the carrier phase shift. The following equations define the characteristics of the detector:

$$\operatorname{Re} V_d(s_m) = \operatorname{Re}\left[V_{USBR}(s_u)\right] + \operatorname{Re}\left[V_{LSBR}(s_l)\right] \tag{5.40}$$

$$\operatorname{Im} V_d(s_m) = \operatorname{Im}\left[V_{USBR}(s_u)\right] - \operatorname{Im}\left[V_{LSBR}(s_l)\right] \tag{5.41}$$

where

$$V_{USBR} = V_{USB}\frac{|V_{co}|}{V_{co}}$$

$$V_{LSBR} = V_{LSB}\frac{|V_{co}|}{V_{co}}$$

$$s_u = s_c + s_m = j(\omega_c + \omega_m)$$

$$s_l = s_c - s_m = j(\omega_c - \omega_m)$$

The complex function $V_d(s)/i_m(s)$ can now be plotted as a bode plot and used for feedback loop design just as in a time-invariant network. Recall $i_m(s)$ is an input, so without loss of generality it can be assumed to have magnitude 1 and phase 0.

5.1.5 Frequency Response Measurements of the MR

The simple $L(t)$ circuit was measured using an actual MR employing the setup shown in Fig. 5.11. The x^2 detector is shown in Fig. 5.12. The MR used in this case was one of the three-leg structures as described in the original invention [10]. The capacitor was chosen to resonate with the MR for a moderate value of control current. This enables measurements to be made in two different operating regions. The dominant resonant peak in

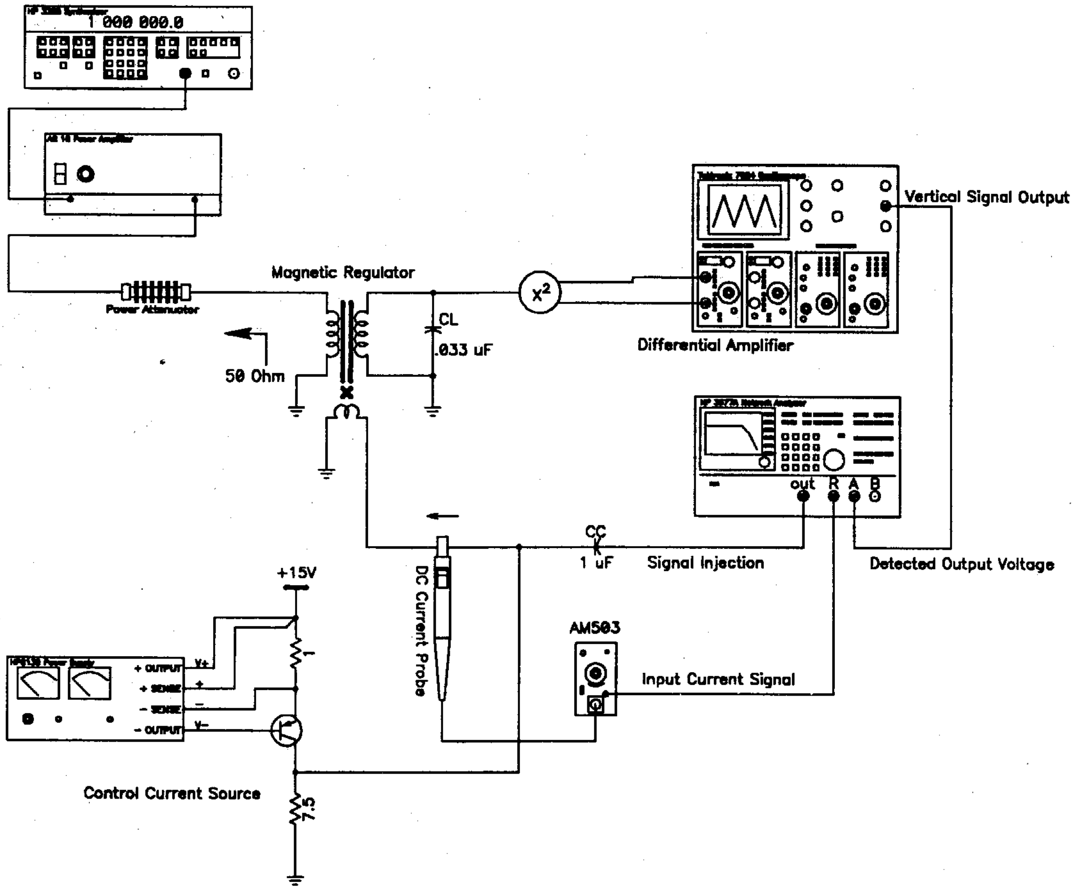


Figure 5.11: Experimental Setup for the $L(t)$ Experiment. The output impedance from the power amplifier is not a constant 50 Ω, so a power attenuator is used to buffer the magnetic regulator from the amplifier. The x^2 circuit has a high input impedance and therefore does not load the output of the magnetic regulator.

the network's input-output response can be above or below the amplifier's output frequency.

Three-Leg Magnetic Regulator Measurement Results

The equivalent circuit for the original three-leg MR contains two inductors that vary with control current, L_c and L_1, as established in Chapter 3. Since L_c is typically large in value and in parallel with the source, its modulation effect is minimal on the G_m transfer function and is ignored in the analysis.

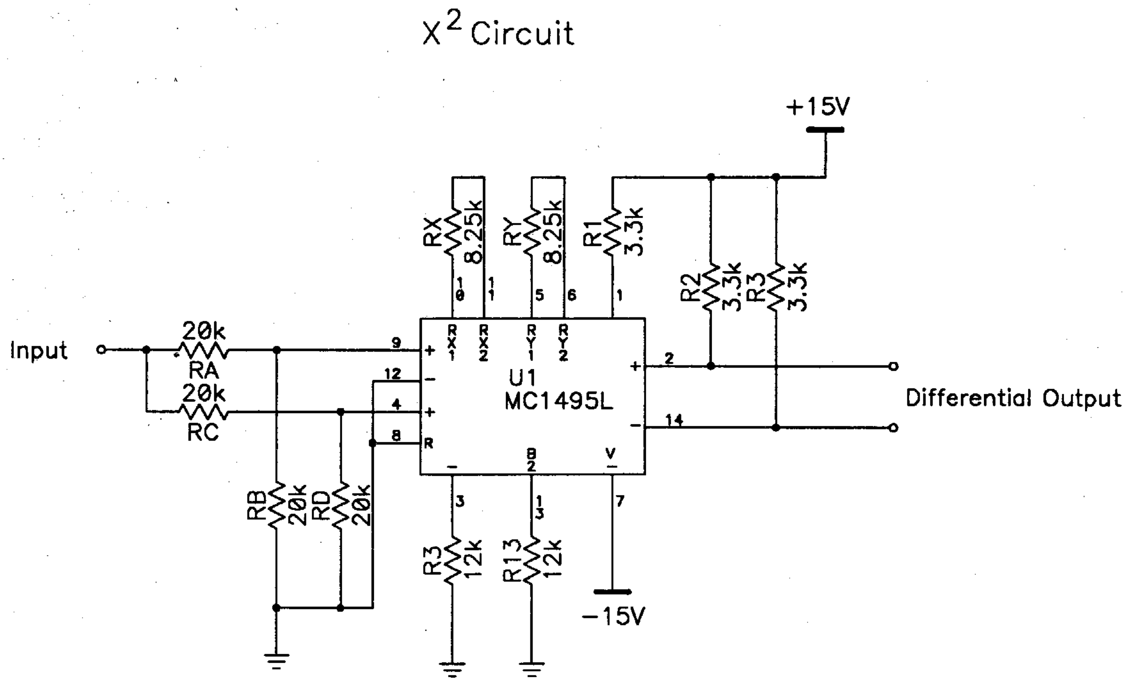


Figure 5.12: The x^2 Detector. The Motorola MC1495L is an analog multiplier. With the inputs tied together, the output is x^2. The output signal is differential so a differential amplifier must be used to observe the output.

The measurements on the three-leg MR are shown in the next several figures. Figure 5.13 shows the results of a low control current. In this case, the natural frequency of the network is below the carrier frequency. Figure 5.14 is a larger control current which results in a network with a natural frequency close to, but still below the carrier frequency. Figure 5.15 is a large control current. In this case the inductance L_0 has been driven to a low value so that the network frequency is now above the carrier frequency. Note the change of the DC phase shift to 180°. Since the DC control current changes L_0, the large signal resonant frequency is also changed. Note the qualitative differences between operation where the network resonant frequency ω_0 is above the source frequency and where it is below the source frequency. The prediction of the frequency response agrees well with the measurement to frequencies up to half the carrier frequency. This establishes the magnetic regulator's small-signal model which will be useful in the next chapter.

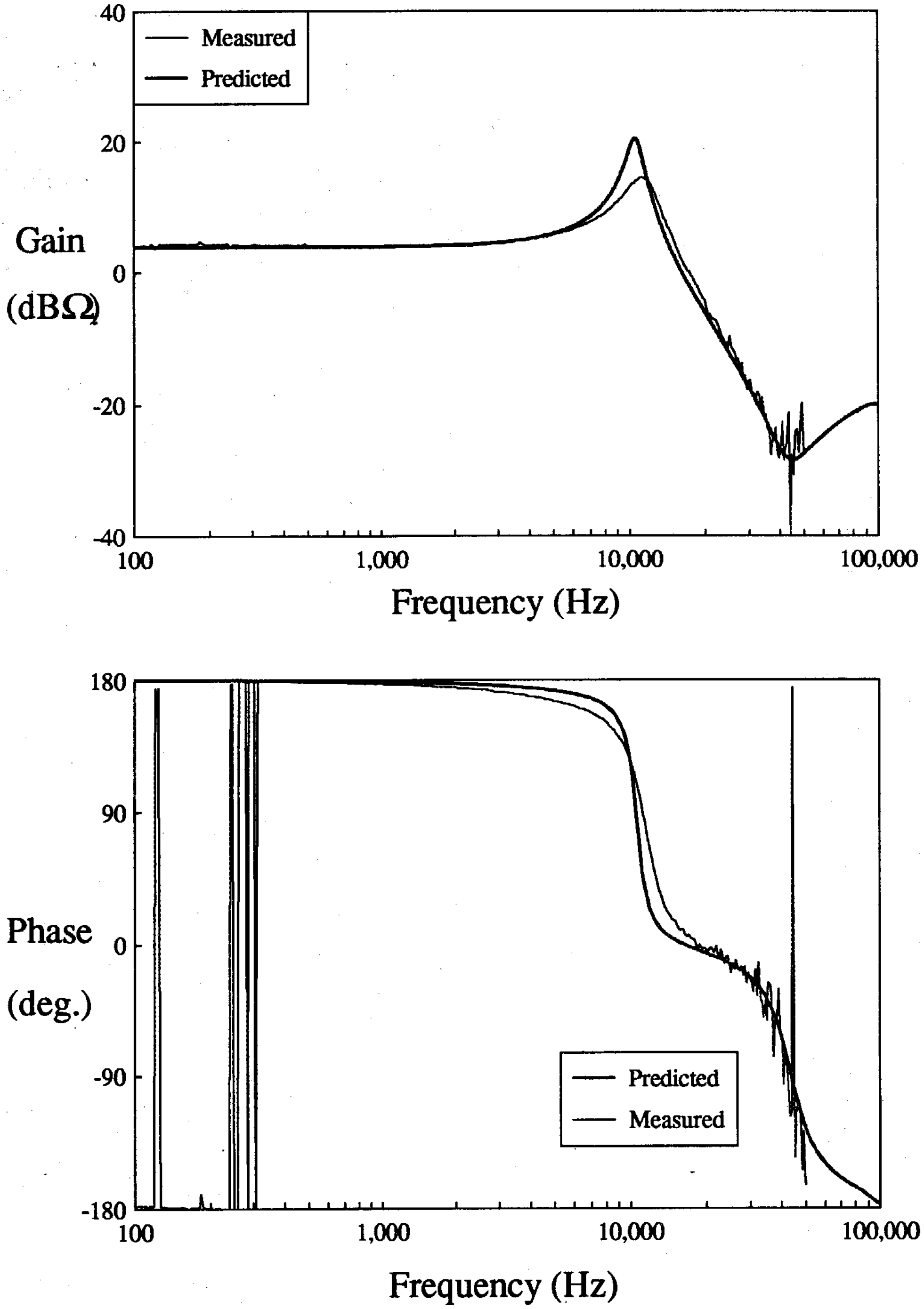
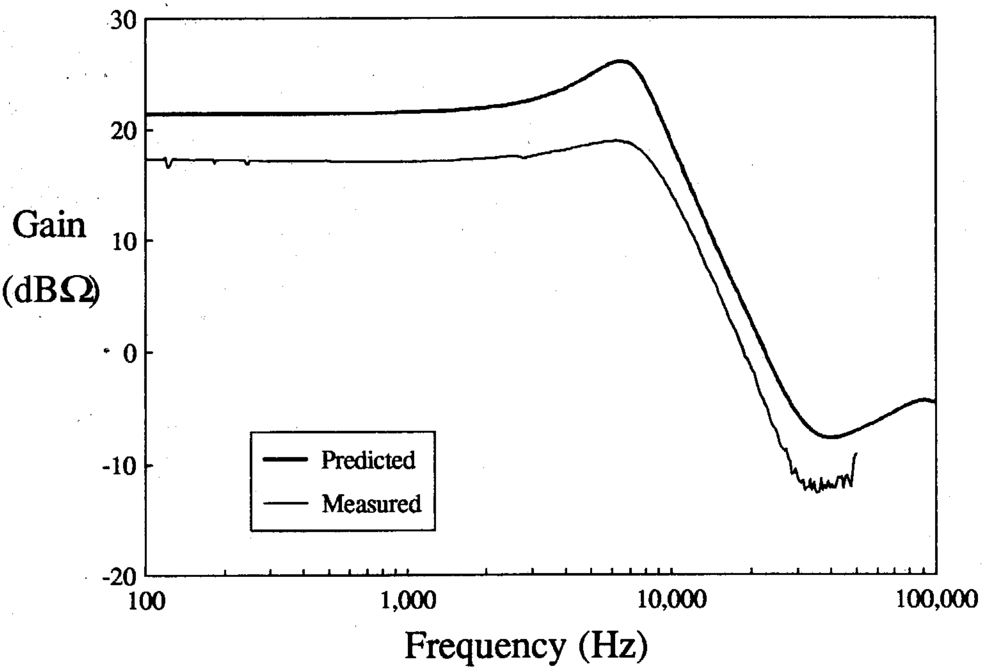


Figure 5.13: Measured Results for a Control Current of 0.1 A. This control current results in a network which resonates well below the carrier frequency.



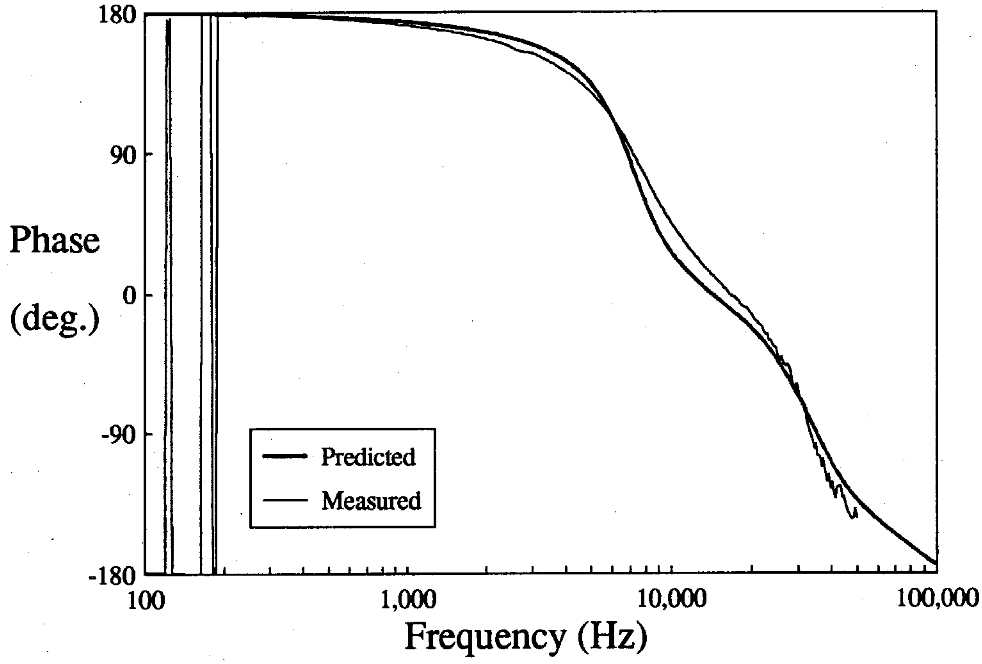
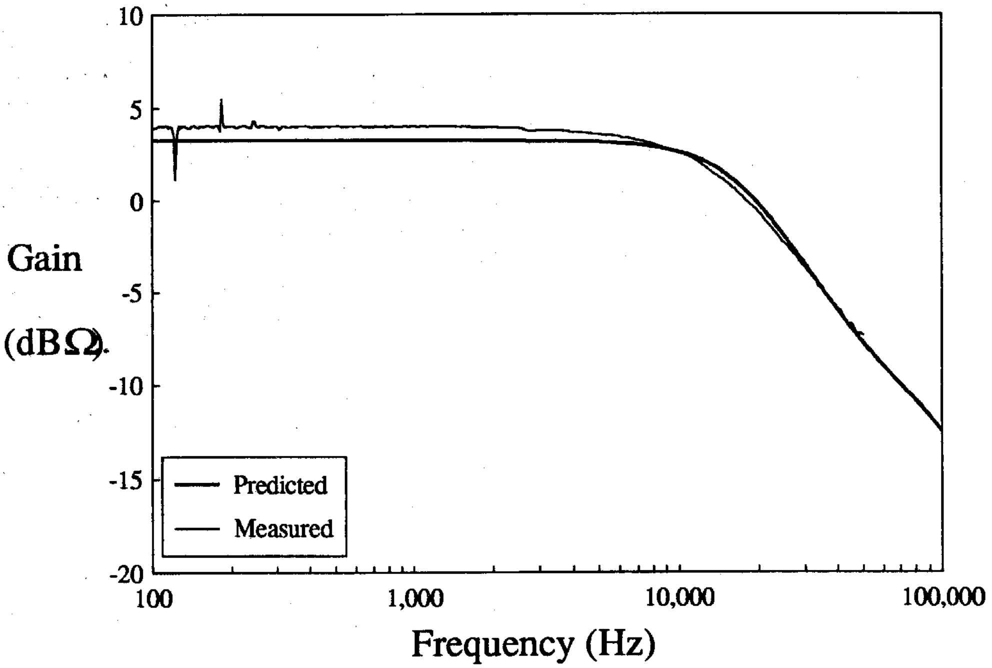


Figure 5.14: Measured Results for a Control Current of 0.2 A. This control current results in a network which resonates closer to, but still below, the carrier frequency. Note that as the network's resonant frequency approaches the carrier frequency, the apparent Q of the control-to-output response drops.



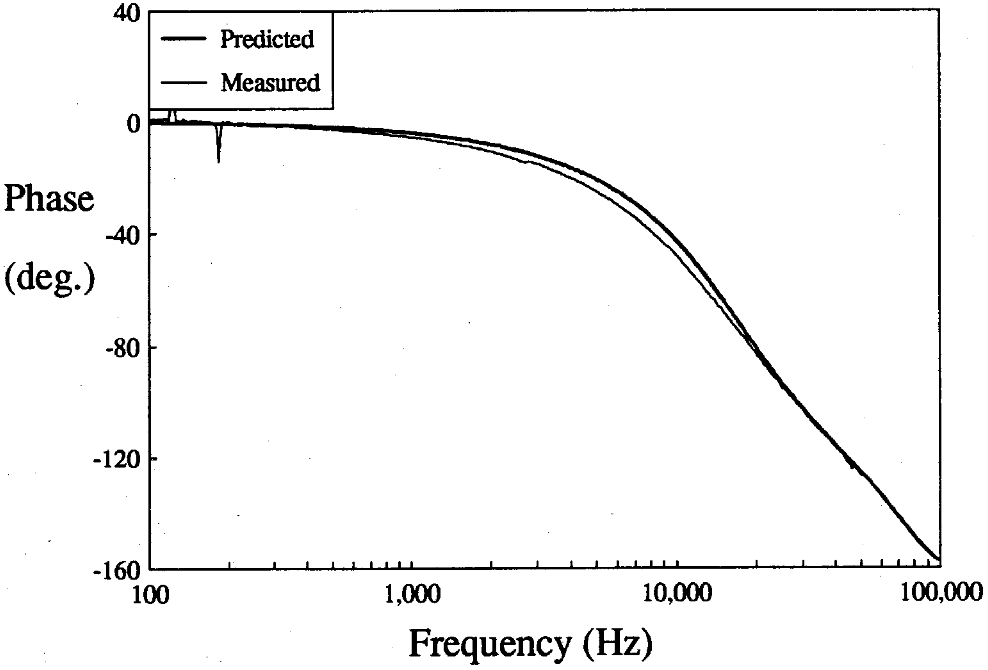


Figure 5.15: Measured Results for a Control Current of 0.4 A. This control current results in a network which resonates well above the carrier frequency. Note the starting phase shift has changed 180° from the previous curves.

Chapter 6

The Zero Order Model

Introduction

In Chapter 5 the model for the magnetic regulator (MR) was established as well as the overall problem of the DC-to-DC converter. The central problem in the dynamic model is that of finding the tank current with its low frequency modulation. It was previously pointed out that a knowledge of the tank current would lead to a complete solution of the dynamic response of the system. In principle, the solution focuses on finding the current in a very simple equivalent circuit such as in Fig. 6.1. In the figure, the voltage source V_{sw}

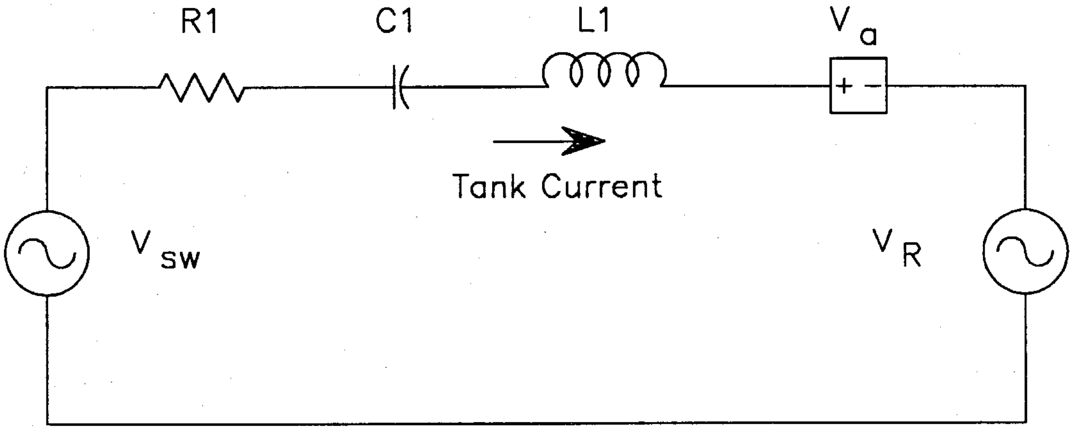


Figure 6.1: Equivalent Circuit for the DC-to-DC Converter. The central problem of the dynamic model for the converter is the solution of the tank current. This model expresses the nonlinear source and load circuits as independent voltage sources. The difficulty in this method is determining the sources V_{sw} and V_R.

is the voltage at the output of the inverter circuit and V_R is the voltage at the input to the rectifier circuit. The voltage source V_a represents the effect of the time-varying inductance in the MR as established in Chapter 5. Since the circuit contains only linear, time-invariant elements, the usual methods of linear circuit analysis are applicable. The problem in the present case will be to solve this equivalent circuit at the three frequencies of interest: the carrier frequency, the upper sideband and the lower sideband (the latter two frequencies are the result of the slow modulation of the carrier frequency by a low frequency control signal). Since the circuit is linear, the solution can be done separately for each frequency and then the results simply added.

The only difficulty in this approach is the knowledge of the signals V_{sw} and V_R. These voltages are dependent upon the tank current and other external conditions such as the load impedance and the source voltage, etc. In general these waveforms are far from sine waves and so it will be necessary to determine the spectrum of each and use the respective Fourier components in the solution at the carrier frequency and the sideband frequencies.

The model for the DC-to-DC converter will be developed using progressively more sophisticated models for V_{sw} and V_R. The simplest possible model for the converter would be to say that the V_{sw} and V_R sources are independent voltage sources which are unaffected by the modulation on the tank current. In this case, these sources would be non-zero only at the carrier frequency. The upper and lower sideband currents would only depend upon the injection source, V_a, and the tank components, L_1, C_1, and R_1 as shown in Fig. 6.1. This is obviously a crude approximation but it is useful to work out the consequences of such a simplified model to aid in the understanding of the more sophisticated models that result from more accurate accounting of the true signals.

6.1 The Rectifier Model in its Simplest Form

The conversion of the tank current modulation to the output AC modulation is the first element of the rectifier model: the forward conversion ratio. The 'rectifier' portion of the circuit for the present discussion is shown in Fig. 6.2 (a). The magnetizing inductance and the ideal transformer action of the magnetic regulator are included in the rectifier circuits because they are most easily accounted for in the rectifier model. The nonlinear behavior of the bridge rectifier and its effect on the waveform across the magnetizing inductance will be absorbed into the voltage source V_R. Figure 6.2 (b) depicts a simplified circuit which will be the basis of the rectifier model development. The ideal transformer has been moved to the output with a suitable change in the component values in the load.

When the large-signal, steady-state behavior of the converter is of interest, the model for the rectifier will contain an independent voltage source that represents the voltage at the input to the rectifier. The current that flows into the rectifier at the carrier frequency is approximated as a sine wave, and this current will determine the DC output voltage, as shown in equations derived below.

Once the DC operating point is known, the problem changes to the small-signal response. In this case, the rectifier is assumed to be a stiff source and therefore not dependent upon any modulation of the input current. Since the modulation terms are all carried in the sidebands above and below the carrier, the small-signal solution is only concerned with finding the upper and lower sideband currents. Therefore, the zero-order rectifier model has a short as its input. The conversion of the modulation on the AC carrier current input to the mostly DC average current out of the rectifier is accomplished with a dependent current source in the model. (This is analogous to the solution of circuits containing bipolar transistors. The operating point is found using a large-signal model for the BJT which has an independent voltage source V_{be} at the input. Once the operating point is

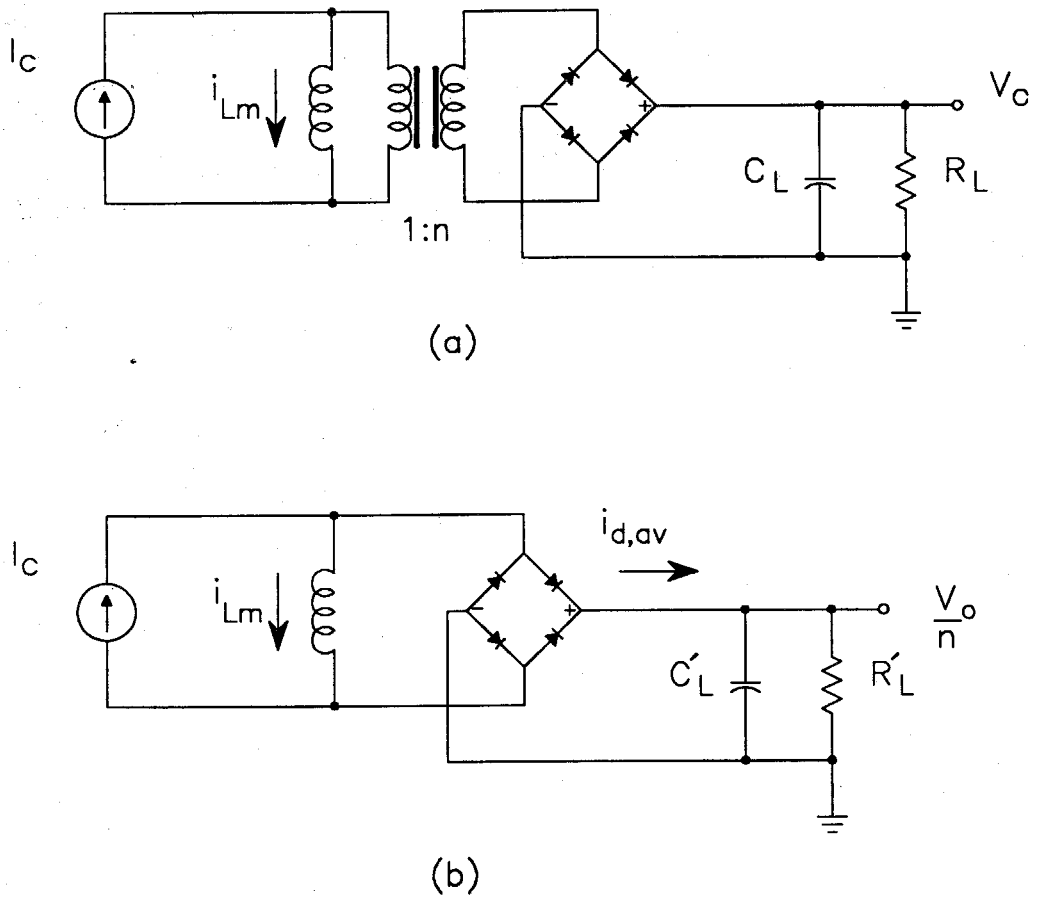


Figure 6.2: The Schematic Equivalent Circuit for the Rectifier (a). The ideal transformer is moved to the output by scaling the load components and the output voltage.

found, the small-signal model for the BJT is used which replaces the voltage source with an incremental impedance. In this example, the incremental impedance is being taken as zero.)

6.1.1 The Large-Signal Rectifier Equivalent Circuit

The equivalent circuit for the large-signal, steady-state case is illustrated in Fig. 6.4. The dependent current source $F(i)$ produces a DC current that is a function of the tank current amplitude into the rectifier, and the voltage source V_R is a square wave at the carrier frequency. The mathematical form for $F(i)$ will be derived below.

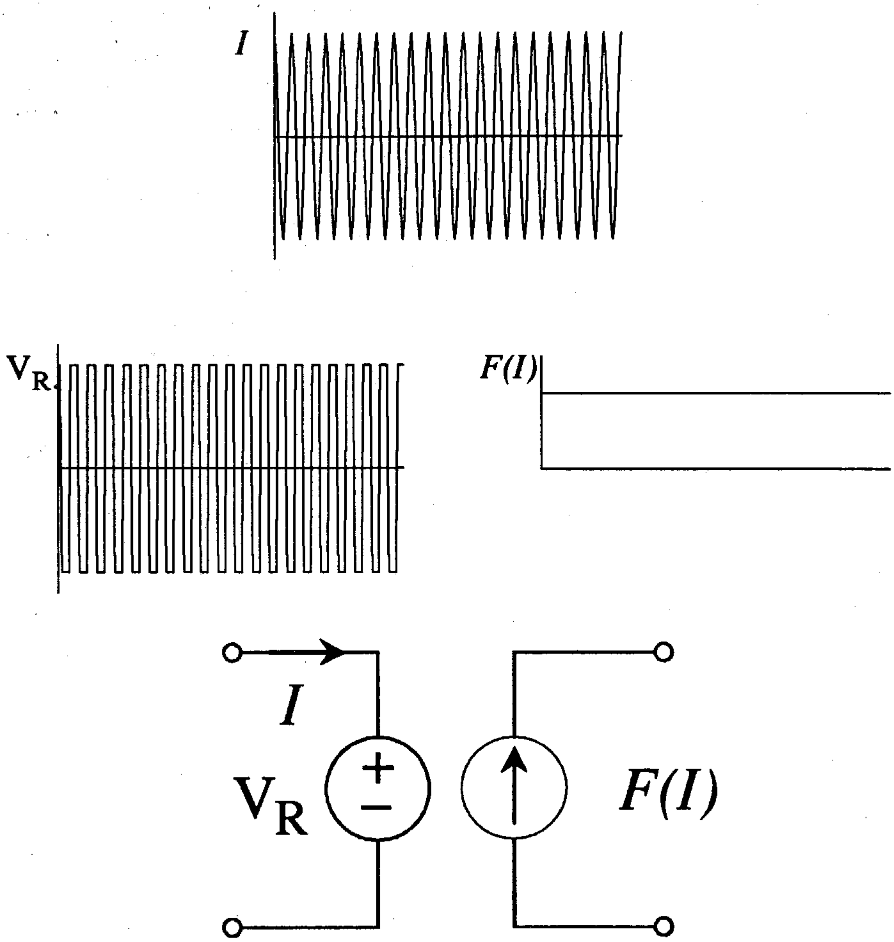


Figure 6.3: Steady-State Model for the Resonant Rectifier. The voltage source V_R is a square wave that switches in synchronism with the input current to the diode bridge. The output is a pulsating current which is represented here by its average value.

6.1.2 The Small-Signal Rectifier Equivalent Circuit

The equivalent circuit for the small-signal, dynamic case is illustrated in Fig. 6.4 along with some representative waveforms. The dependent current source $f(i)$ produces a low frequency current that is a function of the modulated tank current into the rectifier. The mathematical form for $f(i)$ will be derived below. The current out of the rectifier circuit will be proportional to the envelope of the input tank current for low modulation frequencies. At high modulation frequencies, the inductance L_m must be accounted for more accurately than is done here; this will be pursued in the next chapter.

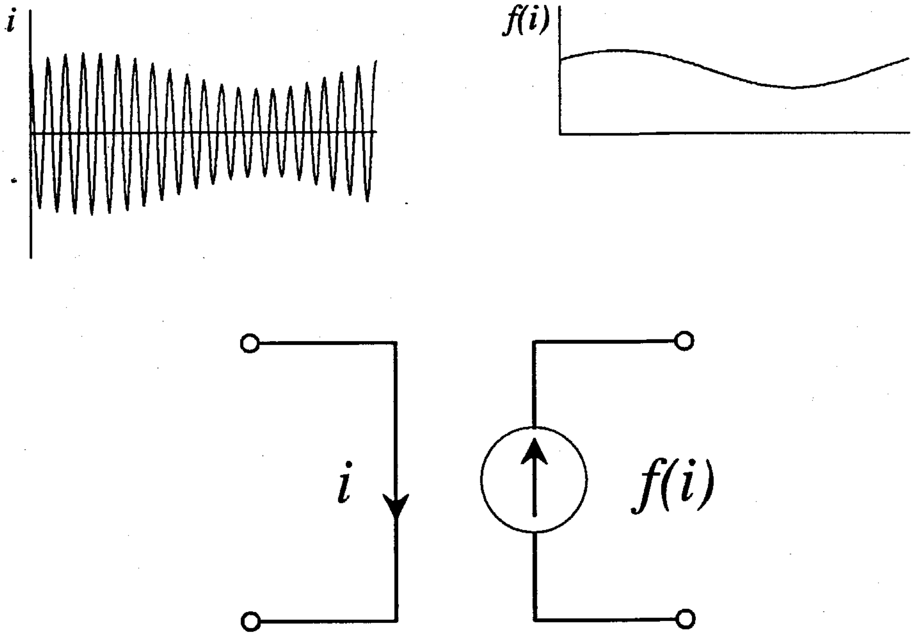


Figure 6.4: The Zero-Order Model for the Resonant Rectifier. The input current is a high frequency carrier signal modulated at low frequency. The output contains only the low frequency modulation superimposed on the average DC output current.

6.2 Control to Output Response

A circuit like the resonant DC-to-DC converter by itself is a rather poor power supply since small changes in the resonant components will result in rather large changes in the output voltage. In addition, the control current input is generally a very sensitive port with small changes in the control resulting in large changes in the inductance L_1. For these reasons and others, it is generally necessary to apply negative feedback to the converter to make it a stable regulator. With negative feedback, the control system will adapt to changing component values and conditions to assure a stable output quantity such as the

DC output voltage. To design a feedback regulator, one must have a knowledge of the frequency response of the control-to-output transfer function. This function will determine the nature of the control system and the final performance achievable for the regulator.

In the case of the control-to-output response, the input DC voltage and the load are held constant. An AC perturbation and a DC bias current is applied to the magnetic regulator's control winding. This will result in signal injection into the tank circuit through the nonlinear leakage inductance in the magnetic regulator. This generates signals at both the upper and lower sideband frequencies which will excite the equivalent circuit (this action is modeled by the voltage source V_a in the small-signal magnetic regulator model). Prior to calculating the value of the magnetic regulator parameters, it is necessary to calculate the steady-state operating point.

6.2.1 Determination of the Steady-State Tank Current

The calculation of the steady-state tank current, I_c, is the same as the calculation of the steady-state operating point of the system which was solved in section 4.2, under the assumption that the modulation is small signal and therefore does not disturb the large-signal operating conditions of the converter.

The circuit that is the basis for the operating point calculation is shown in Fig. 6.2 (a). For the moment it is unimportant how the tank current I_c is generated; we are only concerned with finding its magnitude (and possibly phase) to calculate the value of the dependent voltage source V_a and the average inductance L_0 in the small-signal model for the magnetic regulator. The magnetic regulator may be wound with a turns ratio between the primary and secondary which introduces an ideal transformer into the model with a 1:n ratio. To simplify the calculations, this transformer will be moved to the output with suitable scaling of the load components and the output voltage. The load components become

$$C_L' = C_L n^2$$

$$R_L' = \frac{R_L}{n^2} \tag{6.1}$$

The equation relating the output voltage from the rectifier to the tank current is found using 2.20 and accounting for the 1:n ideal transformer at the output:

$$V_o = \frac{2}{\pi} n R_L' \cos\varphi_d I_c \tag{6.2}$$

where

$$\varphi_d = \operatorname{atan} \frac{R_L'}{2\pi f_c L_m} \tag{6.3}$$

I_c is the amplitude of the tank current and f_c is the frequency of the tank (carrier) current. Normally the output voltage is well known since it is the regulated quantity; in this case, the tank current amplitude is given by 6.2. For the present analysis, the phase of the tank current will be taken as the reference phase for the circuit.

6.2.2 Magnetic Regulator Equivalent Circuit Determination

In much the same way that the rectifier circuit was solved by first finding the operating point and then inserting the small-signal model, the nonlinear magnetic regulator model is first solved for its operating point, then the small-signal model parameters are determined and used in the small-signal model.

The equivalent circuit for the magnetic regulator is shown in Fig. 6.5. The DC value of the control current I_m is used in conjunction with measured data on the magnetic regulator similar to that shown in Chapter 3 to obtain the element values for the small-signal model.

The data extracted for the magnetic regulator used in the experimental model is shown in Fig. 6.6, (a) to (d).

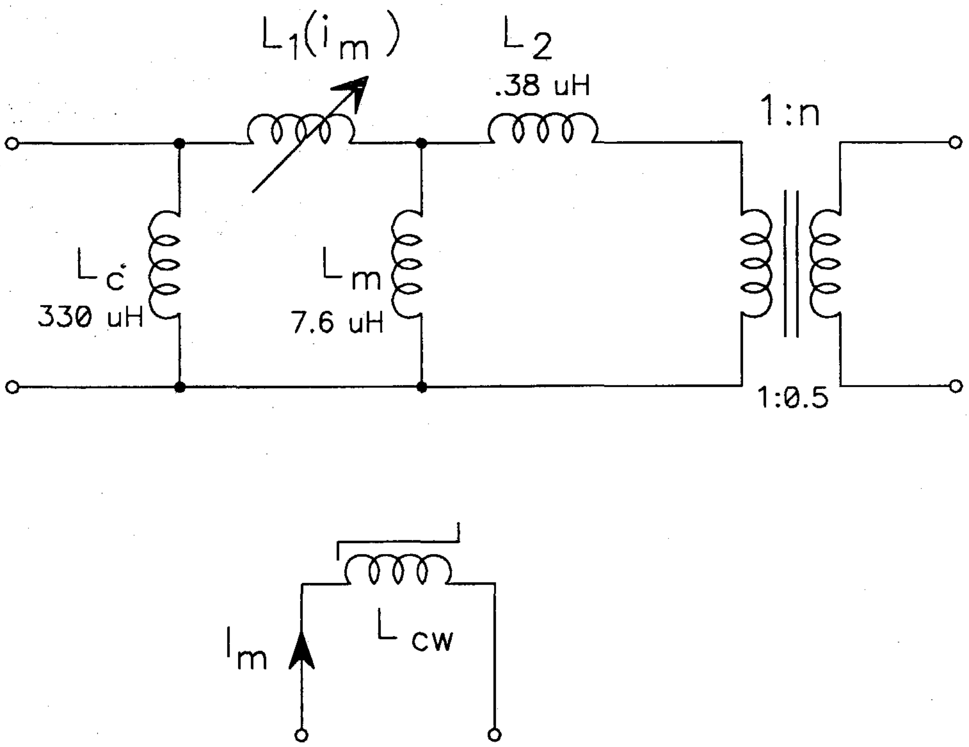
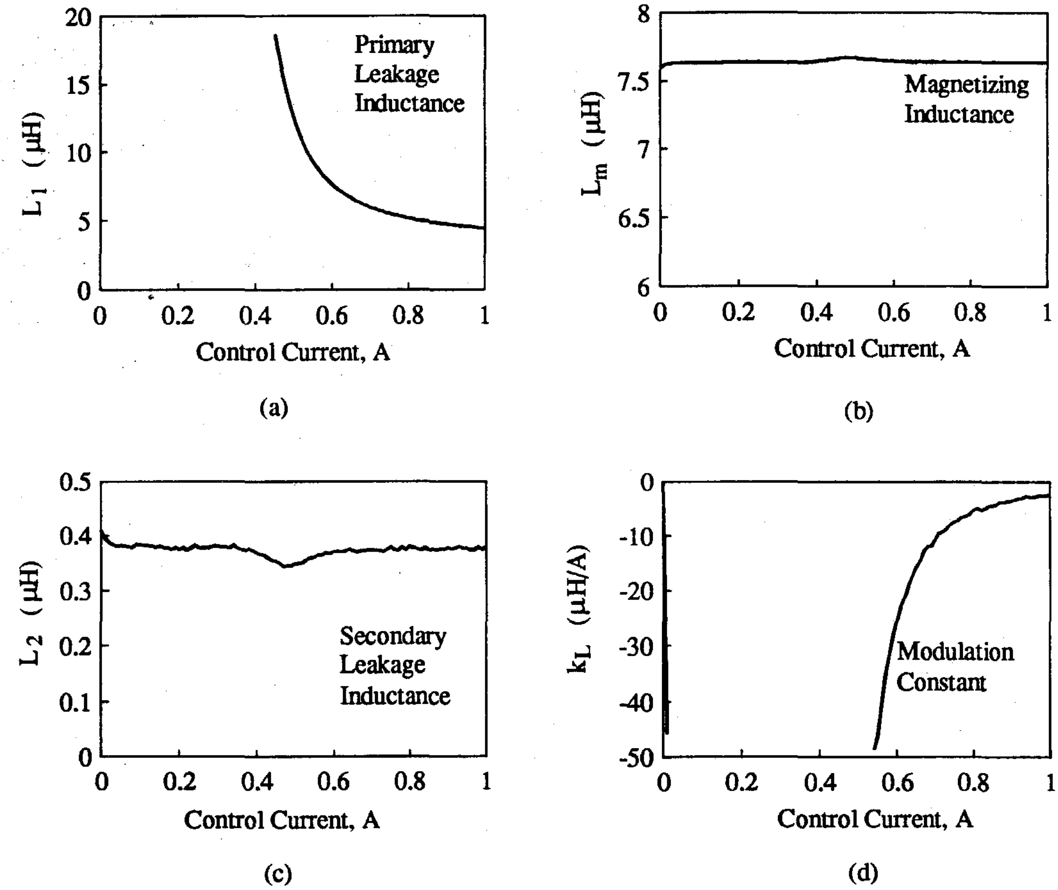


Figure 6.5: Equivalent Circuit of the Filament TWT Supply's Magnetic Regulator. The element values are determined from measurements on the magnetic regulator made prior to installation in the DC-to-DC converter and the DC value of the control current, I_m.

The equivalent circuit in Fig. 6.5 can be simplified to the small-signal model shown in Fig. 6.7. The inductor L_c is large compared to the other elements and is omitted. The variable inductor L_1 is replaced by its average value L_0 in series with the voltage source V_a which accounts for all the nonlinear effects in L_1.

The actual value for L_0 can be analytically determined if the input and output voltages are known. This method was developed in Chapter 2. Effectively, the series resonance composed of C_1L_0 is a 'pass element' which can be adjusted to accomodate changing load and line conditions. Given the input-output conversion ratio, the value of L_0 can be deter-



(a) (b) (c) (d)

Figure 6.6: Measurement of the Key Parameters of the TWT Filament Magnetic Regulator (a) to (c). Curve (d) is derived from curve (a) by using a numerical derivative. Both (a) and (d) have expanded scales to more clearly show the data near the intended operating point.

mined. The magnetic regulator data can then be used to determine the required control current. The control current will determine the other elements in the model. An alternative is to measure the control current at the steady-state operating point and then look up the value of L_0 from measured data on the magnetic regulator.

The secondary leakage inductance L_2 can be eliminated by a simple transformation which reverses the order of L_m and L_2, and introduces an ideal transformer. This transformation will replace L_m and L_2 with the elements L'_m and L'_2 in the reverse order where

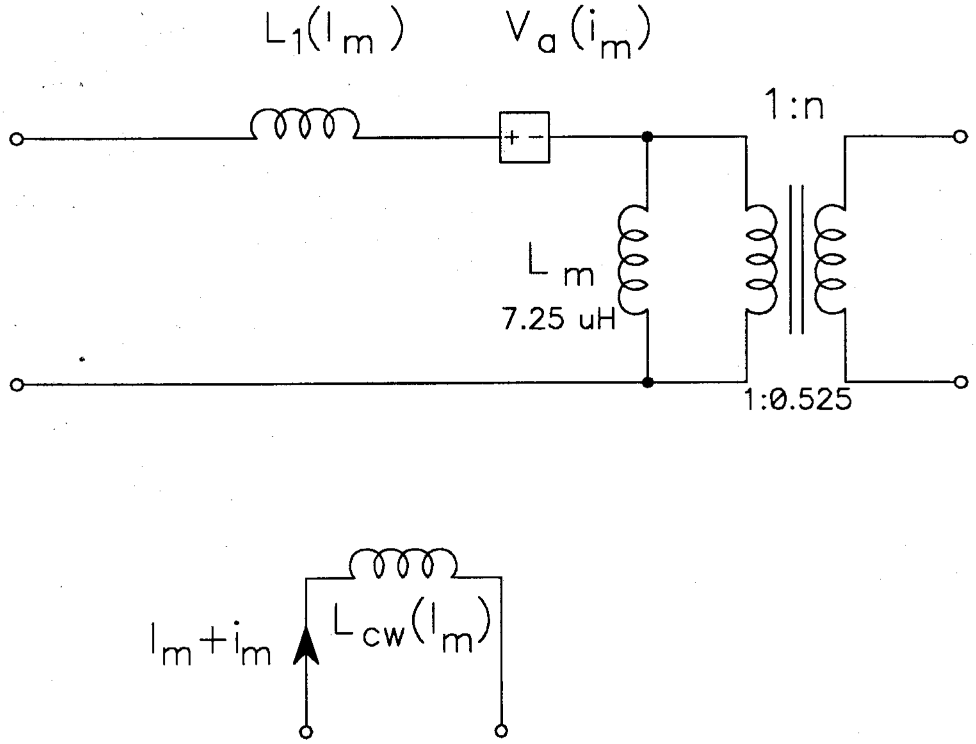


Figure 6.7: Small-Signal Model for the Magnetic Regulator. Several elements from the complete model in Fig. 6.5 have been eliminated. The small-signal quantities are shown in lower-case letters.

$$L'_m = \frac{L_m^2}{L_2 + L_m} \tag{6.4}$$

$$L'_2 = L_m \| L_2 \tag{6.5}$$

The ideal transformer will have a turns ratio x where

$$x = \frac{L_2 + L_m}{L_m} \tag{6.6}$$

L'_2 is absorbed into L_0 and the new value L'_m is used for the magnetizing inductance. For simplicity, the prime will be dropped in all subsequent work. The $1{:}x$ transformer is absorbed into the magnetic regulator's ideal transformer. The control winding is explicitly shown with a linearized inductance which represents the inductance of the control windings at the operating point.

Now that the tank current is known, the dependent voltage source V_a can be directly calculated. This is an important feature of this model: *the nonlinear characteristic of the magnetic regulator reduces to a simple voltage source in the dynamic model.*

6.2.3 Calculation of the Tank Current Modulation

The presence of the voltage source V_a in the magnetic regulator model is the mechanism by which controlled modulation of the tank current is accomplished. This source will generate currents in the tank circuit loop at the carrier frequency plus the modulation frequency (the upper sideband) and at the carrier frequency minus the modulation frequency (the lower sideband).

The currents at the upper and lower sidebands will be different in general owing to the frequency response of the tank components and V_a itself. We can calculate these currents as follows:

$$i_{USB} = \frac{V_a(s_u)}{z_x(s_u)} \tag{6.7}$$

$$i_{LSB} = \frac{V_a(s_L)}{z_x(s_L)} \tag{6.8}$$

Where

$$s_u = j(\omega_c + \omega_m)$$
$$s_L = j(\omega_c - \omega_m)$$

and

$$\begin{aligned} z_x(s) &= R_1 + \frac{1}{sC_1} + sL_1 \\ &= \frac{1}{sC_1}\left[1 + \frac{1}{Q}\frac{s}{\omega_0} + \left(\frac{s}{\omega_0}\right)^2\right] \\ \omega_0 &= \frac{1}{\sqrt{L_1C_1}} \\ Q &= \sqrt{\frac{L_1}{C_1}}\frac{1}{R_1} \end{aligned} \tag{6.9}$$

The voltage source V_a is related to the control current through 6.10 and 6.11:

$$V_a(s_L) = \frac{k_L}{2} \cdot s_L \cdot \boldsymbol{I}_c \cdot \boldsymbol{I}_m \tag{6.10}$$

$$V_a(s_u) = \frac{k_L}{2} \cdot s_u \cdot \boldsymbol{I}_c \cdot \boldsymbol{I}_m \tag{6.11}$$

Since the control current modulation I_m is an input, the phase of I_m can be taken as zero without loss of generality. I_c is also taken as a reference, so its phase shift is zero. In later models, the carrier frequency component of the tank current will be a complex number with a magnitude and phase. k_L is a proportionality constant which is derived from the characteristics of the magnetic regulator. This parameter will be determined from measurements on the magnetic regulator and the measured value of the control current at the operating point of the converter. Alternatively, if the DC control current is not known, the value of L_0 can be determined from the operating point, then the DC control current can be found from the magnetic regulator measurements. Due to the high sensitivity of the inductance to the control current, these two methods may give somewhat different values for L_0.

6.2.4 Determination of the Output Voltage from the Tank Current

The task in this section is to convert the known tank current into the output voltage. Along the way to the output voltage, the mathematical form for the functions $F(i)$ and $f(i)$ in the rectifier equivalent circuit will be derived. Under the small-signal assumption, the carrier frequency current will determine the DC output voltage. This computation will use the large-signal model for the rectifier containing $F(i)$ and the static model of the magnetic regulator. The modulation of the tank current will determine the output AC perturbation. The small-signal model of the rectifier containing $f(i)$ together with the small-signal model of the magnetic regulator, linearized about the operating point, solves the AC problem.

The calculation of the small-signal output voltage will follow two steps: first, the output current from the rectifier will be determined as a function of the input AC current and its modulation, then the output current will be averaged and applied to the output load impedance. The implicit assumption is that the load will perform this averaging step due to a low-pass frequency response characteristic.

The Large-Signal Forward Transfer Characteristic of the Rectifier

To derive the average current flowing into R'_L and C'_L, it is necessary to calculate the current in inductor L_m (refer to Fig. 6.2 (b)). The input voltage to a rectifier circuit like that of Fig. 6.2 (b) is a square wave, which switches between $+(V_o + V_f)/n$ and $-(V_o + V_f)/n$ where V_f is the forward voltage drop of the diodes (approximately 1.4 V for silicon diodes in a bridge rectifier). This will result in a triangular current in L_m which will subtract from the sinusoidal input current. The resulting waveform is a slightly distorted sine wave as illustrated in Fig. 6.8 (b). The current that flows into the load is a rectified version of $i_1 - i_{L_m}$. This current is illustrated in Fig. 6.9 (b) together with one half cycle of the input current i_1 (a). The average value of i_d is calculated as follows (see [9]):

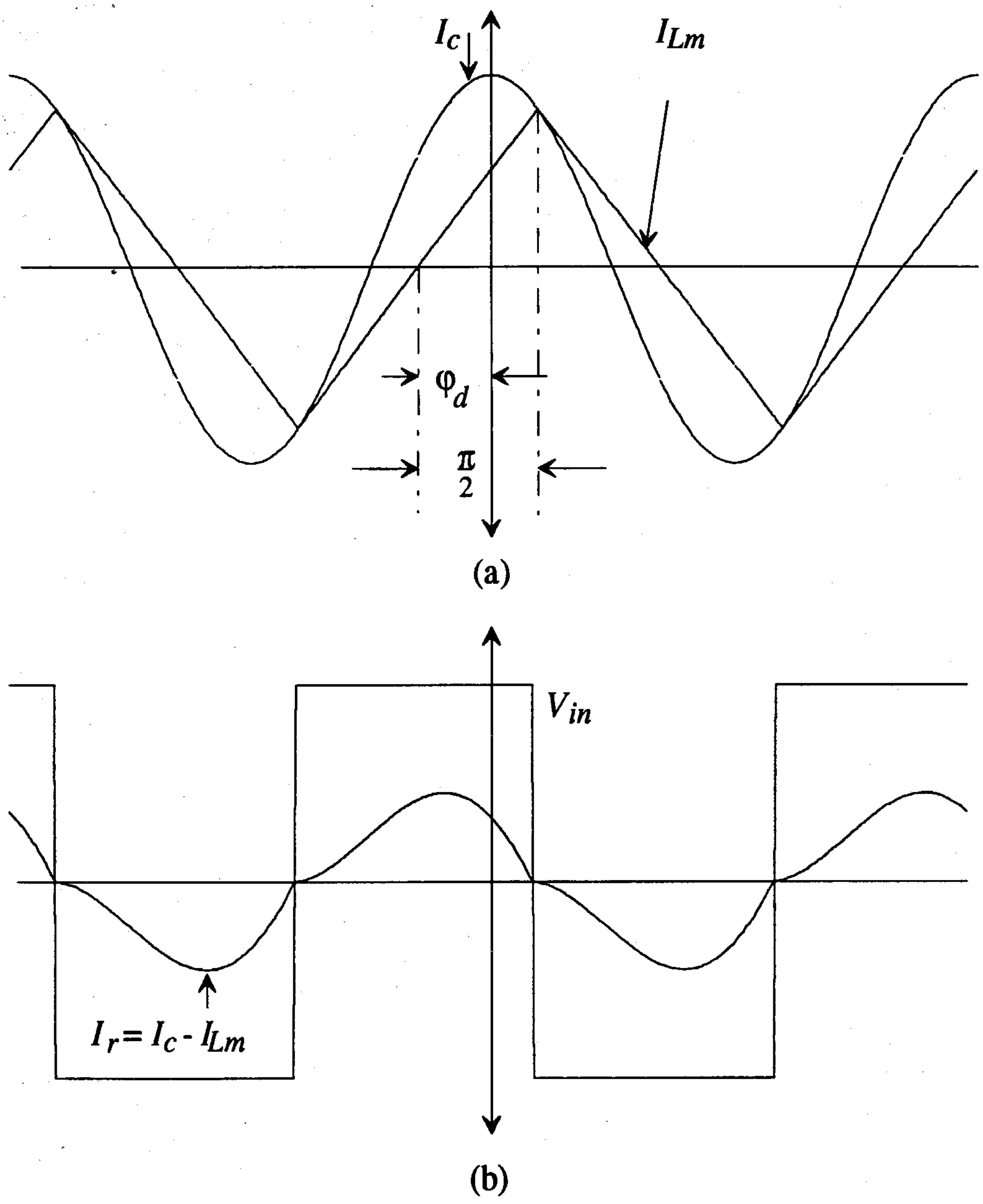


Figure 6.8: Current Waveforms (a) and Voltage Waveform (b) Associated with the Rectifier Circuit. The input current i_c is assumed to be a sine wave. The current in inductor L_m will be triangular in response to the input voltage v_{in} which is a square wave. The current which will be rectified and then fed to the load is the difference between the input current and the inductor current.

$$i_c(\theta) = I_c \cos\theta \tag{6.12}$$

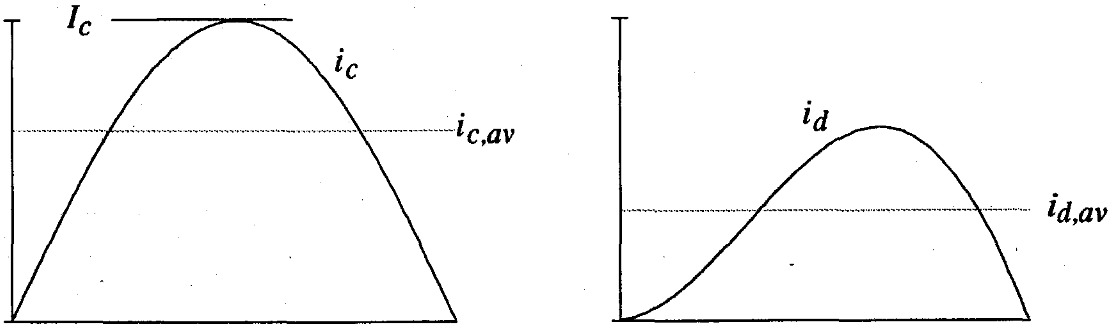
$$i_{Lm}(\theta) = I_c \frac{2}{\pi}(\theta - \varphi_d)\sin\varphi_d \tag{6.13}$$

$$i_{d,av} = \frac{1}{\pi} \int_{-\frac{\pi}{2}-\varphi_d}^{\frac{\pi}{2}-\varphi_d} i_c(\theta) - i_{Lm}(\theta) d\theta \tag{6.14}$$

$$i_{d,av} = \frac{2}{\pi} I_c \cos\varphi_d \tag{6.15}$$

Equation 6.15 relates the average current out of the bridge rectifier diodes to the amplitude of the input current for the large-signal case. Therefore, the large-signal forward transfer characteristic of the rectifier is

$$F(I) = \frac{2}{\pi}\cos\varphi_d I \tag{6.16}$$



(a)

(b)

Figure 6.9: Input Current Waveform to the Resonant Rectifier (a) and Output Current Waveform (b). The model for the rectifier relates the amplitude (I_c) of the input current (i_c) to the average value ($i_{d,av}$) of the output current i_d. The calculation accounts for the distortion of the i_d waveform.

The Small-Signal Forward Transfer Characteristic of the Rectifier

The same equation used in the large-signal diode model to relate the tank current to the average current into the load can be used to relate the *envelope* of the tank current to the AC modulation of the rectifier output current.

The tank current is formed from 6.7 and 6.8 together with the steady-state tank current, I_C:

$$i_T(t) = I_c \cos(\omega_c t + \varphi_c) + I_{USB} \cos(\omega_U t + \varphi_U) + I_{LSB} \cos(\omega_L t + \varphi_L) \tag{6.17}$$

As in Chapter 5, this equation contains the high frequency carrier frequency plus low frequency modulation, but in this form it is difficult to extract the modulation envelope from this equation. Previously the rectifier circuit was replaced with an x^2 circuit to make the envelope calculation easier. In this case the amplitude modulation can be extracted using the same method: Calculate the low frequency output from an imaginary x^2 circuit to reveal the amplitude modulation envelope, then use the envelope information to calculate the average forward current through 6.15. The static quantity I_c is replaced by the modulation envelope of the rectifier's input current and the result is a low-frequency modulated output current. The extraction of the modulation envelope from the carrier current by an x^2 circuit is illustrated in Fig. 6.10. The relationship between the average output current of the rectifier and the tank current amplitude is shown in Fig. 6.9.

The low-frequency output of an x^2 circuit was derived in Chapter 5. The result is

$$\mathrm{Re}\, i_{env}(s_m) = \mathrm{Re}\,[i_{USBR}(s_u)] + \mathrm{Re}\,[i_{LSBR}(s_L)] \tag{6.18}$$

$$\mathrm{Im}\, i_{env}(s_m) = \mathrm{Im}\,[i_{USBR}(s_u)] - \mathrm{Im}\,[i_{LSBR}(s_L)] \tag{6.19}$$

where

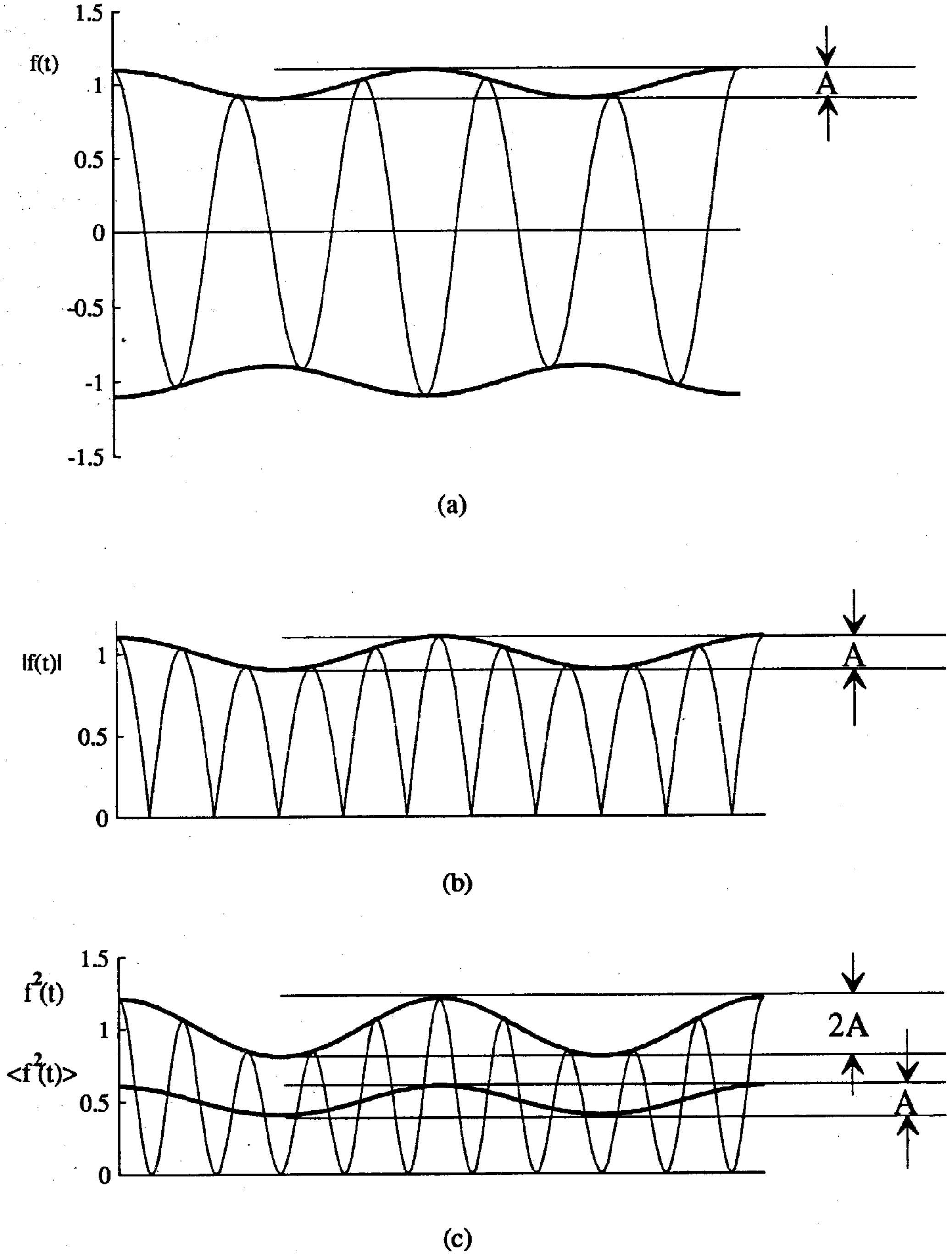


Figure 6.10: Illustration Showing How an x^2 Circuit Extracts the Envelope From a Modulated Signal. The function $f(t)$ in (a) is the input waveform with amplitude modulation. The absolute value of $f(t)$ is shown in (b). The function $f^2(t)$ is shown in (c). The peak-to-peak modulation on $f^2(t)$ is twice that on f, but the average of $f^2(t)$ has the same envelope as in (a) and (b).

$$i_{USBR}(s_u) = i_{USB}(s_u)\, e^{-j\varphi_c}$$
$$i_{LSBR}(s_L) = i_{LSB}(s_L)\, e^{-j\varphi_c}$$

$$i_{USB}(s_u) = I_{USB} e^{j\varphi_u}$$
$$i_{LSB}(s_L) = I_{LSB} e^{j\varphi_L}$$

Notice that 6.18 and 6.19 can be written in the more compact notation:

$$i_{env}(s_m) = i_{USBR}(s_u) + \overline{i_{LSBR}(s_L)} \tag{6.20}$$

The current $i_{env}(s_m)$ is the envelope of the current into the bridge rectifier. It is shown as dependent upon the modulation frequency to emphasize that the high frequency components have been removed and a low frequency perturbation remains. It should be emphasized that there is no actual x^2 circuit involved in the present analysis; it is simply a useful mathematical trick to extract the modulation envelope from a complex input signal.

Envelope to Average Conversion

In the next step, the envelope of the input current must be converted to the average current out of the rectifier to account for the current lost into the inductance L_m and the lowpass charcacteristic of the load. This is graphically illustrated in Fig. 6.9. Mathematically this conversion is accomplished using 6.15:

$$i_{d,av}(s_m) = \frac{2}{\pi} i_{env}(s_m) \cos\varphi_d \tag{6.21}$$

Output Voltage Transfer Characteristic

The output voltage can now be calculated by linear circuit analysis as follows:

$$V_o(s_m) = i_{\mathrm{d,av}}(s_m)\frac{R_L'}{1+s_m R_L' C_L'} \tag{6.22}$$

6.2.5 Predicted Results

The equivalent circuit of the rectifier can now be combined with the magnetic regulator model developed in Chapter 5. The resulting circuit will be the basis for the solution of the DC-to-DC converter under the assumptions outlined above. The equivalent circuit for the DC-to-DC converter including the zero-order rectifier model is illustrated in Fig. 6.11.

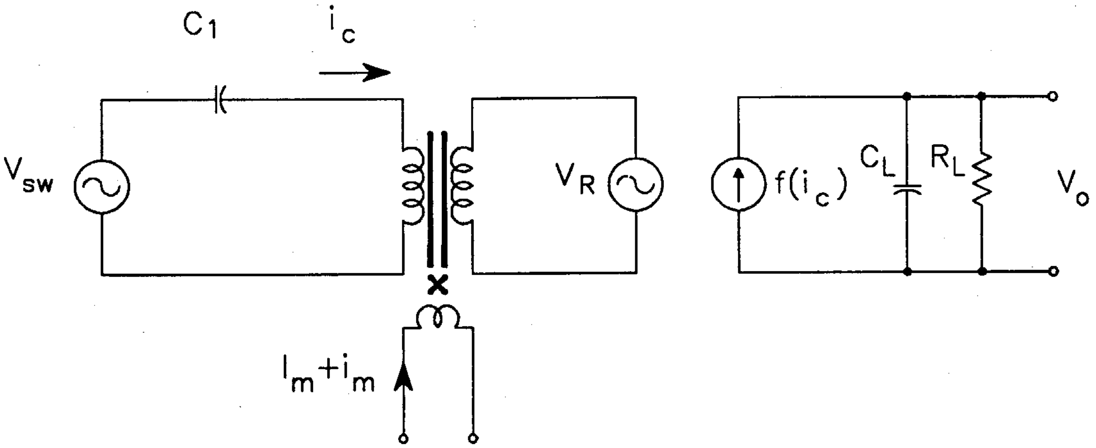


Figure 6.11: The Equivalent Circuit for the DC-to-DC Converter Using the Zero-Order Rectifier Model.

The MR's small signal model is inserted into the model for the DC-to-DC converter as shown in Fig. 6.12. In accordance with the zero order model, the inverter and rectifier are shown as stiff voltage sources. Simplification of this circuit leads to the AC modulation model shown in Fig. 6.13. Since the inverter and rectifier voltage sources are not modulated, they appear as shorts in this model. For simplicity, the ideal transformer has been moved to the output, with appropriate modifications to the load.

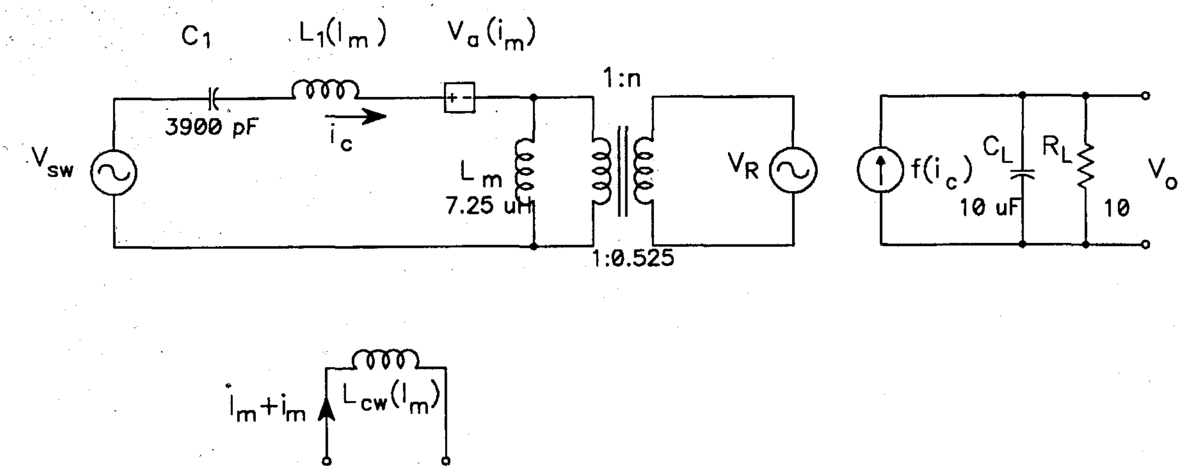


Figure 6.12: The Small-Signal Equivalent Circuit for the TWT Filament Power Supply. Note L_m is in parallel with an ideal voltage source and so can be eliminated.

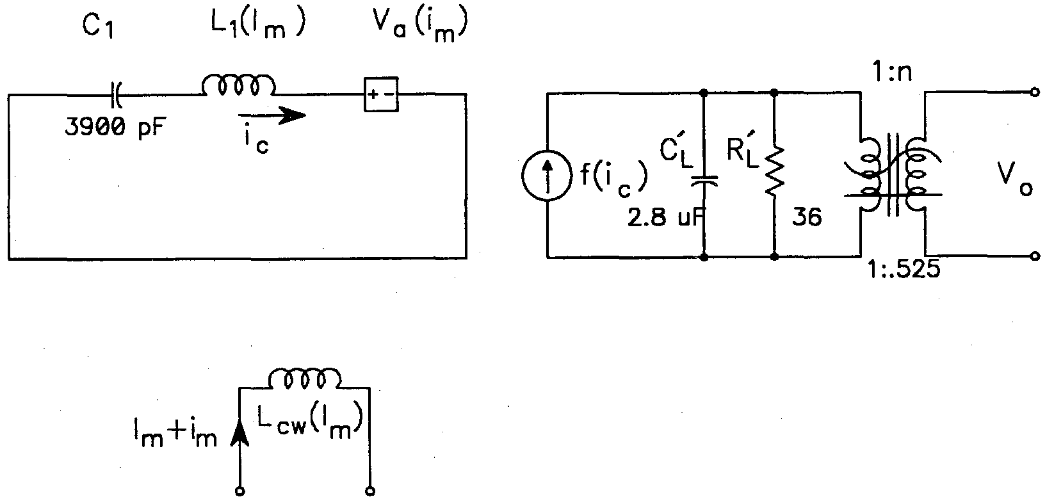


Figure 6.13: Final Small-Signal Model for the TWT Filament Supply. This model is valid for the calculation of the sideband responses only; the sources V_{sw} and V_R would be included if the solution at the carrier frequency were desired.

At this point, the tank circuit has no loss elements at all and so would have an infinite Q, which is certainly unrealistic. A measurement of the impedance looking into the primary of the magnetic regulator with the control current adjusted to the operating point and the secondary shorted was made to provide a realistic value for the series resistance in the tank circuit inductance. The resistance was found to be approximately 1.5 ohm. This resistance is included in the calculation for $z_x(s)$ as R_1.

The Salient Features of the Tank Current Response

The overall small-signal control-to-output response of the DC-to-DC converter can now be assembled from 6.20, 6.21, and 6.22:

$$V_o(s_m) = \frac{R_L'}{1+s_m R_L' C_L'} n \cdot \frac{2}{\pi} \cos\varphi_d \left[i_{USBR}(s_c+s_m) + \overline{i_{LSBR}(s_c-s_m)} \right] \tag{6.23}$$

Apart from the constants in 6.23, the output voltage is seen to be the product of two transfer functions, one relating the average output current to the output voltage (i.e., the load impedance) and the other relating the envelope of the tank current to the upper and lower sideband currents (the forward transfer characteristic of the rectifier). The former transfer function is that of a simple pole at low frequencies and will be the dominant characteristic up to moderately high frequencies. This function is a familiar result and will not be discussed further. The latter function will come into play at high frequencies and is the interesting function since it has not been encountered before. To construct a picture of the control-to-output response, we will focus on the envelope response, then at the end include the dominant pole from the load impedance.

Consider once again the relationships for the tank current sidebands:

$$i_{USB}(s_m) = \frac{V_a(s_u)}{z_x(s_u)} = \frac{\frac{k_L}{2} s_u I_c I_m(s_m)}{\frac{1}{s_u C_1}\left[1+\frac{1}{Q}\frac{s_u}{\omega_0}+\left(\frac{s_u}{\omega_0}\right)^2\right]} \tag{6.24}$$

$$i_{LSB}(s_m) = \frac{V_a(s_L)}{z_x(s_L)} = \frac{\frac{k_L}{2} s_L I_c I_m(s_m)}{\frac{1}{s_L C_1}\left[1 + \frac{1}{Q}\frac{s_L}{\omega_0} + \left(\frac{s_L}{\omega_0}\right)^2\right]} \tag{6.25}$$

The complex conjugate of 6.25 is required for the envelope. Since the complex variable *s* is purely imaginary, its conjugate is -*s*. The result is

$$\begin{aligned}\overline{i_{LSB}(s_m)} = \frac{V_a(-s_L)}{z_x(-s_L)} &= \frac{\frac{k_L}{2}(-s_L) I_c I_m(s_m)}{\frac{1}{-s_L C_1}\left[1 + \frac{1}{Q}\left(\frac{-s_L}{\omega_0}\right) + \left(\frac{-s_L}{\omega_0}\right)^2\right]} \\ &= \frac{\frac{k_L}{2} I_c I_m (s_c - s_m)^2 C_1}{\left[1 - \frac{1}{Q}\frac{s_c - s_m}{\omega_0} + \left(\frac{s_c - s_m}{\omega_0}\right)^2\right]}\end{aligned} \tag{6.26}$$

The lower sideband frequency s_L has been explicitly shown as the difference between the carrier frequency and the modulation frequency. Similarly, the upper sideband current signal is

$$i_{USB}(s_m) = \frac{\frac{k_L}{2} I_c I_m(s_m)(s_c + s_m)^2 C_1}{\left[1 + \frac{1}{Q}\frac{s_c + s_m}{\omega_0} + \left(\frac{s_c + s_m}{\omega_0}\right)^2\right]} \tag{6.27}$$

Equations 6.26 and 6.27 combine to form the envelope of the tank current:

$$i_{env}(s_m) = \frac{\frac{k_L}{2} I_c I_m(s_m)(s_c + s_m)^2 C_1}{\left[1 + \frac{1}{Q}\frac{s_c + s_m}{\omega_0} + \left(\frac{s_c + s_m}{\omega_0}\right)^2\right]} + \frac{\frac{k_L}{2} I_c I_m(s_m)(s_c - s_m)^2 C_1}{\left[1 - \frac{1}{Q}\frac{s_c - s_m}{\omega_0} + \left(\frac{s_c - s_m}{\omega_0}\right)^2\right]} \tag{6.28}$$

This equation must be manipulated to reveal its salient features clearly. The form in 6.28 can be written as

$$i_{env}(s_m) = \frac{k_L}{2} I_c I_m(s_m) \frac{N(s_m)}{D(s_m)} \tag{6.29}$$

In 6.29, the interesting part has been separated to the $N(s_m)$ and $D(s_m)$ factors to allow a separate discussion of the poles and zeros of the response.

Poles of the Tank Current Envelope

The denominator polynomial $D(s_m)$ contains the poles of the tank current envelope. $D(s_m)$ is formed when a common denominator in 6.28 is found. The poles occur when $D(s_m) = 0$.

$$D(s_m) = \left[1 + \frac{1}{Q}\frac{s_c + s_m}{\omega_0} + \left(\frac{s_c + s_m}{\omega_0}\right)^2\right]\left[1 - \frac{1}{Q}\frac{s_c - s_m}{\omega_0} + \left(\frac{s_c - s_m}{\omega_0}\right)^2\right] \tag{6.30}$$

In the form in 6.30, it is clear that a pole will occur when $s_c + s_m = j\omega_0$ or $s_c - s_m = j\omega_0$. Which of these two conditions will occur depends on the operating point of the system, since ω_0 may be above or below ω_c.

Zeros of the Tank Current Envelope

The numerator polynomial, $N(s_m)$, controls the location of the zero in the tank current envelope. The numerator polynomial is found to be

$$N(s_m) = C_1(s_c + s_m)^2\left[1 - \frac{1}{Q}\frac{s_c - s_m}{\omega_0} + \left(\frac{s_c - s_m}{\omega_0}\right)^2\right] + C_1(s_c - s_m)^2\left[1 + \frac{1}{Q}\frac{s_c + s_m}{\omega_0} + \left(\frac{s_c + s_m}{\omega_0}\right)^2\right] \tag{6.31}$$

which simplifies to

$$N(s_m) = C_1\left(s_c^2 + s_m^2\right)\left[1 - \frac{1}{Q}\frac{s_m}{\omega_0}\frac{s_c^2 - s_m^2}{s_c^2 + s_m^2} + \frac{\left(s_c^2 - s_m^2\right)^2}{\left(s_c^2 + s_m^2\right)\omega_0^2}\right] \tag{6.32}$$

While 6.32 is not in the standard factored pole-zero form, it is in a form that makes identification of the zeros easy. Clearly, the zero in 6.32 will occur when

$$\frac{\left(s_c^2 - s_m^2\right)^2}{\left(s_c^2 + s_m^2\right)\omega_0^2} = -1 \tag{6.33}$$

To solve 6.33 for s_m involves solving a quadratic equation for s_m^2 which results in

$$\omega_{m,zero}^2 = \left(\frac{2x + 1 \pm \sqrt{1 + 8x}}{2}\right)\omega_0^2 \tag{6.34}$$

where

$$x = \frac{\omega_c^2}{\omega_0^2}$$

The negative root in 6.34 is the solution of interest since $\omega_{m,zero} \ll \omega_c$. Typically this zero will be well above the poles discussed above and will be in the right half plane. The fact that a high frequency RHP quadratic double zero occurs in the control-to-output transfer function effectively sets an upper limit on the bandwidth of the regulation loop. It has been found experimentally that other considerations will be a stronger limiting condition on the system bandwidth, such as the sensitivity of the gain to the operating point.

6.3 Output Impedance

The great advantage to the equivalent circuit model for the DC-to-DC converter is quickly realized when calculating the output impedance. This function is normally of interest to power system designers since it is used to find the output voltage's response to a load change. However, in most practical power supplies the output impedance is dominated by the large output capacitance used to filter and store energy for the output. To avoid this pitfall the internal output impedance $z'_o(s)$ illustrated in Fig. 6.14 is used.

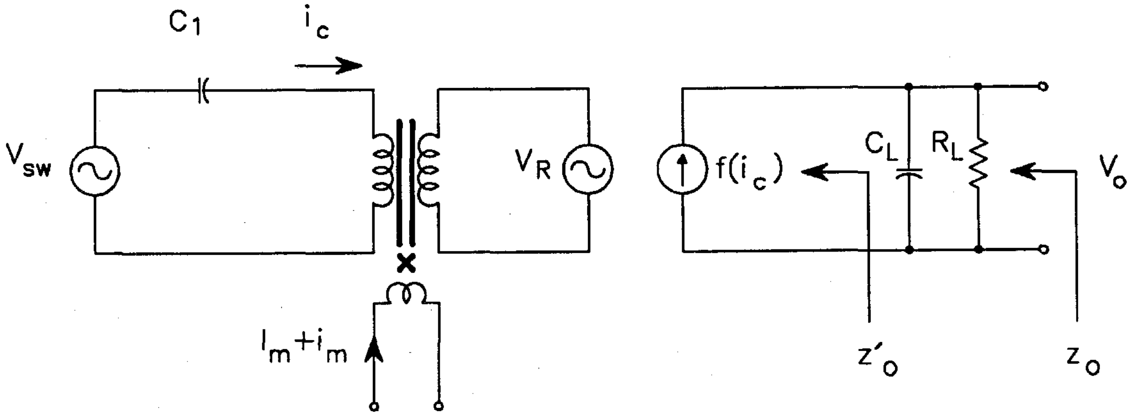


Figure 6.14: Illustration of the Internal Output Impedance z'_o. The normal output impedance z_o is dominated by the output filter capacitor C_L starting at relatively low frequency. The internal output impedance, z'_o, gives a clearer picture of the characteristics of the converter.

The output impedance in the case of the zero-order rectifier model can, by inspection, be determined to be infinity. This follows from the assumption that the tank current is independent of the output load. Measurements done below will show that this is an unre-

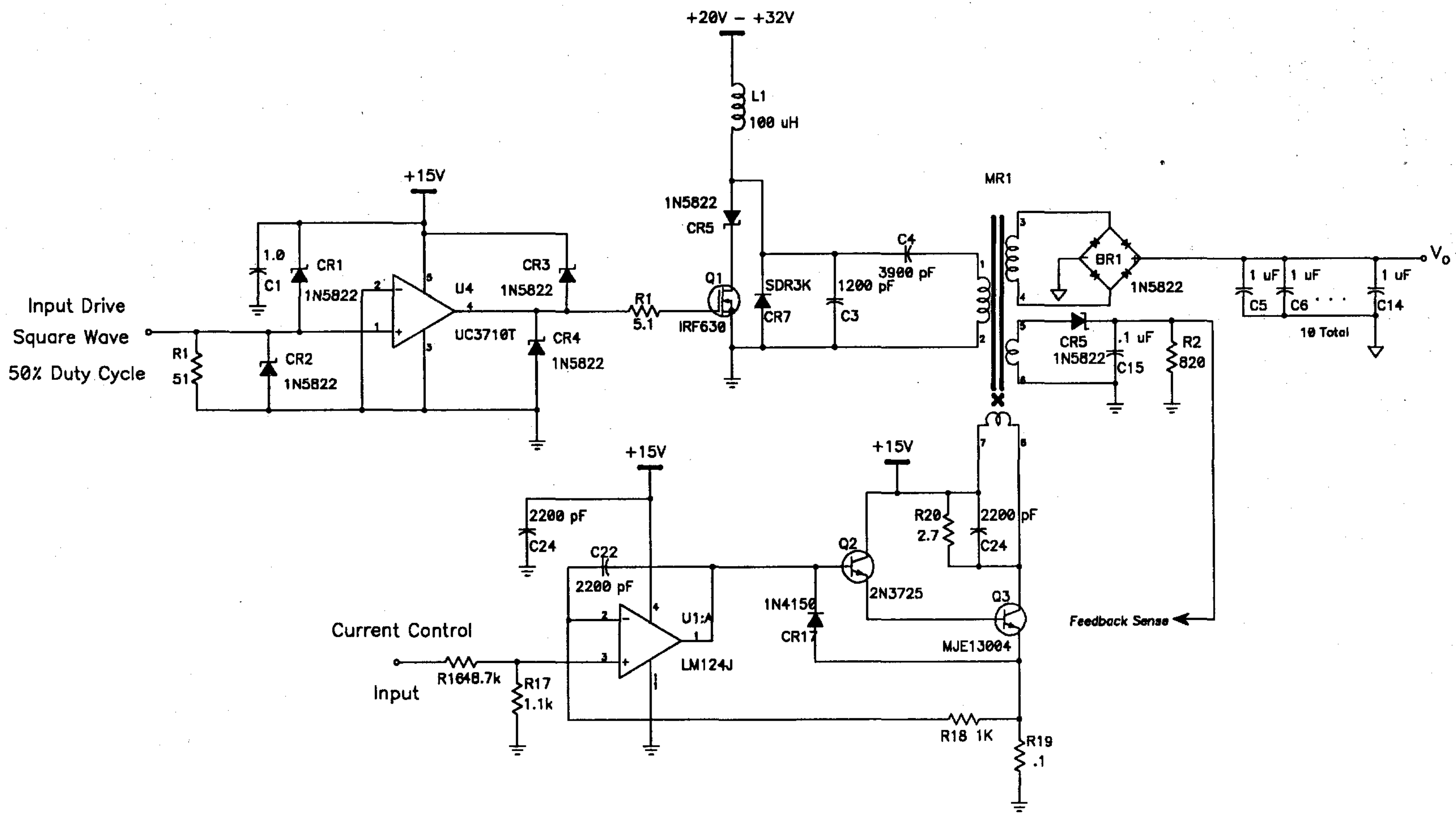


Figure 6.15: Schematic Diagram of the Experimental Prototype Used to Evaluate the DC-to-DC Converter Model.

alistic model and further refinements will be necessary to properly model the behavior of the resonant rectifier. It is precisely this flaw in the model which prompted the title "zero-order." Chapter 7 will develop a more realistic model.

6.4 Measured Results

6.4.1 Circuit Description

An experimental DC-to-DC converter was constructed as power supply to the filament of a Traveling Wave Tube (TWT). Figure 6.15 shows the schematic diagram of the power stage and control current drive circuitry.

In this application, the isolation between the input and output grounds must be able to withstand in excess of 4,000 V. This high voltage isolation is necessary since the TWT is normally operated with an anode voltage near ground and a negative cathode voltage [20]. In a conventional PWM power supply this isolation causes many problems, mainly due to the large leakage inductance in the power transformer. The Resonant DC-to-DC converter uses the power transformer (i.e., the magnetic regulator) leakage inductance as a part of the circuit and, in fact, actively controls its value to provide the output regulation. This makes the high leakage inductance associated with the primary-secondary isolation barrier unimportant.

A second serious problem for standard PWM circuits is transmitting the feedback information from the output to the control circuits. Usually the output voltage must be stabilized against variations in the ambient temperature, load resistance, input line voltage, etc., so the output voltage must be sensed and fed back to a feedback controller. When there is a large differential between the input and output grounds, this feedback voltage is difficult to arrange, usually requiring optical or AC-chopped coupling. The resonant DC-to-DC converter can be built so that the control circuits are all referenced to the secondary ground, thus eliminating the need to cross the isolation barrier. This approach can also have pitfalls in the case of a TWT filament supply.

One real-world inconvenience of the TWT is that it can arc between the cathode and the tube envelope (ground). This can be accurately modeled as a switch from the cathode to ground with zero impedance and zero closing time. (The arc's actual impedance will be much lower than the parasitic resistances in the circuit, and the arc occurs so rapidly, the waveform characteristics will be determined by the inductances and capacitances in the circuit rather than the characteristics of the arc.) This will result in extremely large transient currents and voltages occurring in the circuit. If the control circuits are referenced to the cathode potential, great care must be taken to avoid stray capacitance to ground from any of the nodes in the circuit which would be damaged by large transient voltages. Often even one or two picofarads is enough to cause a circuit failure in the inevitable arc. The usual solution to this problem is to enclose all the electronics at the cathode potential in a Faraday cage. (A Faraday cage is a conducting enclosure designed to shield the contents from external electric fields. It is based upon the fact that the electric field inside a conducting enclosure is zero when the enclosure is immersed in an external electric field.)

In the experimental circuit used here, the mechanical complexity of the Faraday cage was deemed unnecessary. Under the conditions of the laboratory, adequate regulation can be maintained with another approach. The approach used was to wind an auxiliary winding in close proximity to the secondary winding (still preserving the high-voltage isolation) and using this winding to provide a feedback voltage to the control circuits which are then referenced to the input ground. The approach is adequate to accommodate input line and most temperature changes but is rather poor in the case of load variations. Nevertheless, using a TWT filament, the load resistance is well-known and stable. A supply such as this, intended for high production volumes, would almost certainly use the more robust secondary-side regulator.

To test the models developed in this chapter, the feedback control circuits are unimportant since only open-loop quantities are of interest. (For this reason some of the control circuits have been omitted from Fig. 6.15.) The control-to-output transfer function is measured using the magnetic regulator control current as the input variable and the actual output as the output variable. In practice, the loop gain model would need to include a transfer function from the output voltage to the sense voltage.

A more complete discussion of the elements in the experimental circuit may be found in Chapter 4.

6.4.2 Control to Output Transfer Function Measurement

The experimental setup for measuring the control-to-output response is shown in Fig. 6.16. The network analyzer injects a test signal into the circuit which controls the magnetic regulator. Since an open-loop characteristic is desired, an external DC power supply is adjusted to provide the proper input voltage to the voltage-to-current converter circuit that controls the magnetic regulator. The AC perturbation is superimposed on this DC voltage through the use of a series transformer. However, the desired measurement has the current into the control winding as the input variable so the current is sensed at the control winding using a DC current probe. This measurement removes the dynamics of the control circuit from the measurement. The output for the measurement comes from the actual output voltage rather than the feedback as discussed above. The load is 10 Ω and the control current is adjusted manually until the output voltage is 10V.

The measured result from this experiment is shown in Fig. 6.17. The data becomes rather noisy at the higher frequencies due to the low currents injected into the magnetic regulator. The impedance looking into the magnetic regulator control winding is a rather large (and variable) inductance owing to the fact that the control winding is many turns on

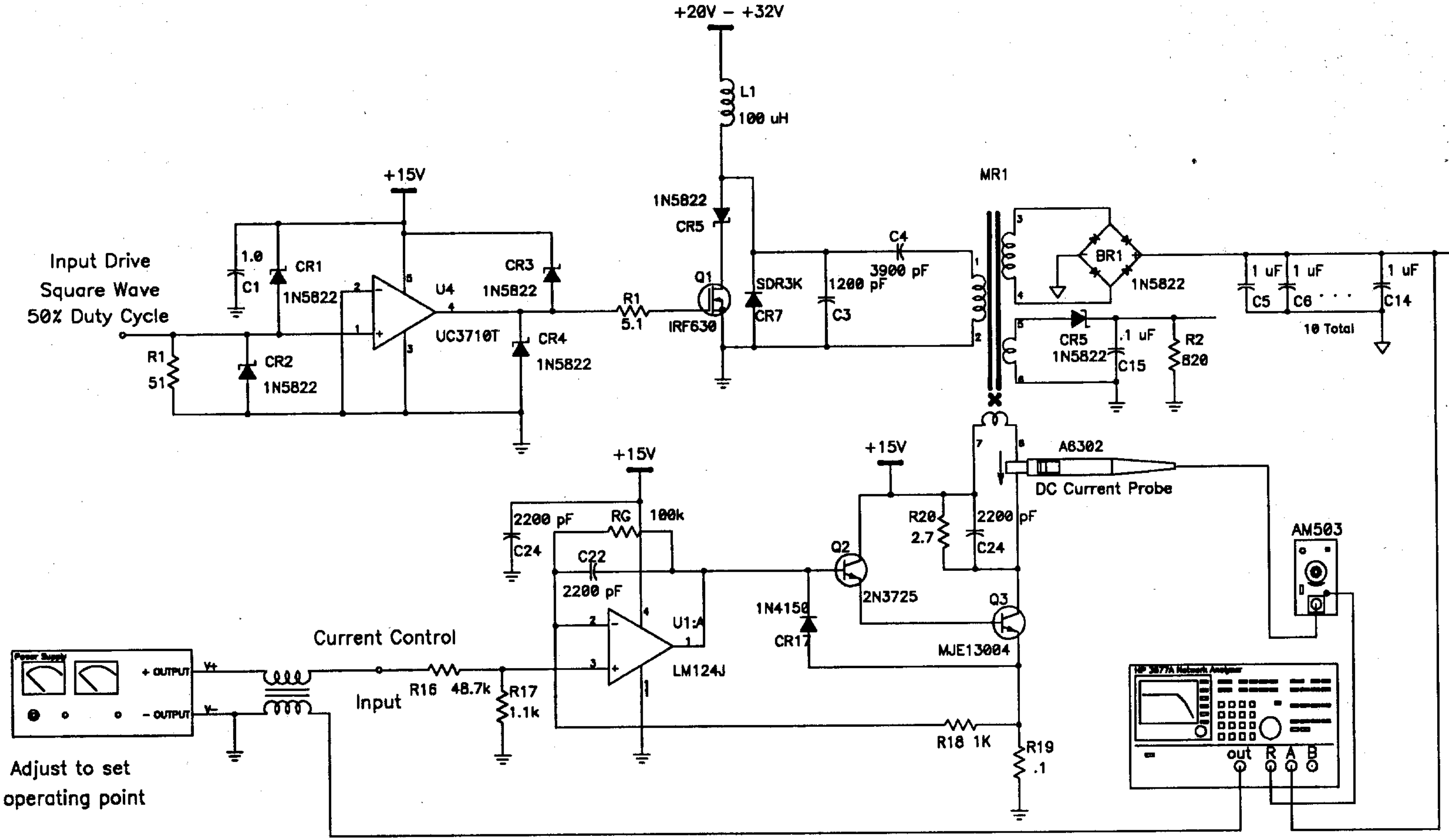


Figure 6.16: The Experimental Setup Used to Measure the Control-to-Output Transfer Function. A DC power supply is used to set the steady-state operation point. The ac injection signal is transformer coupled onto this bias input.

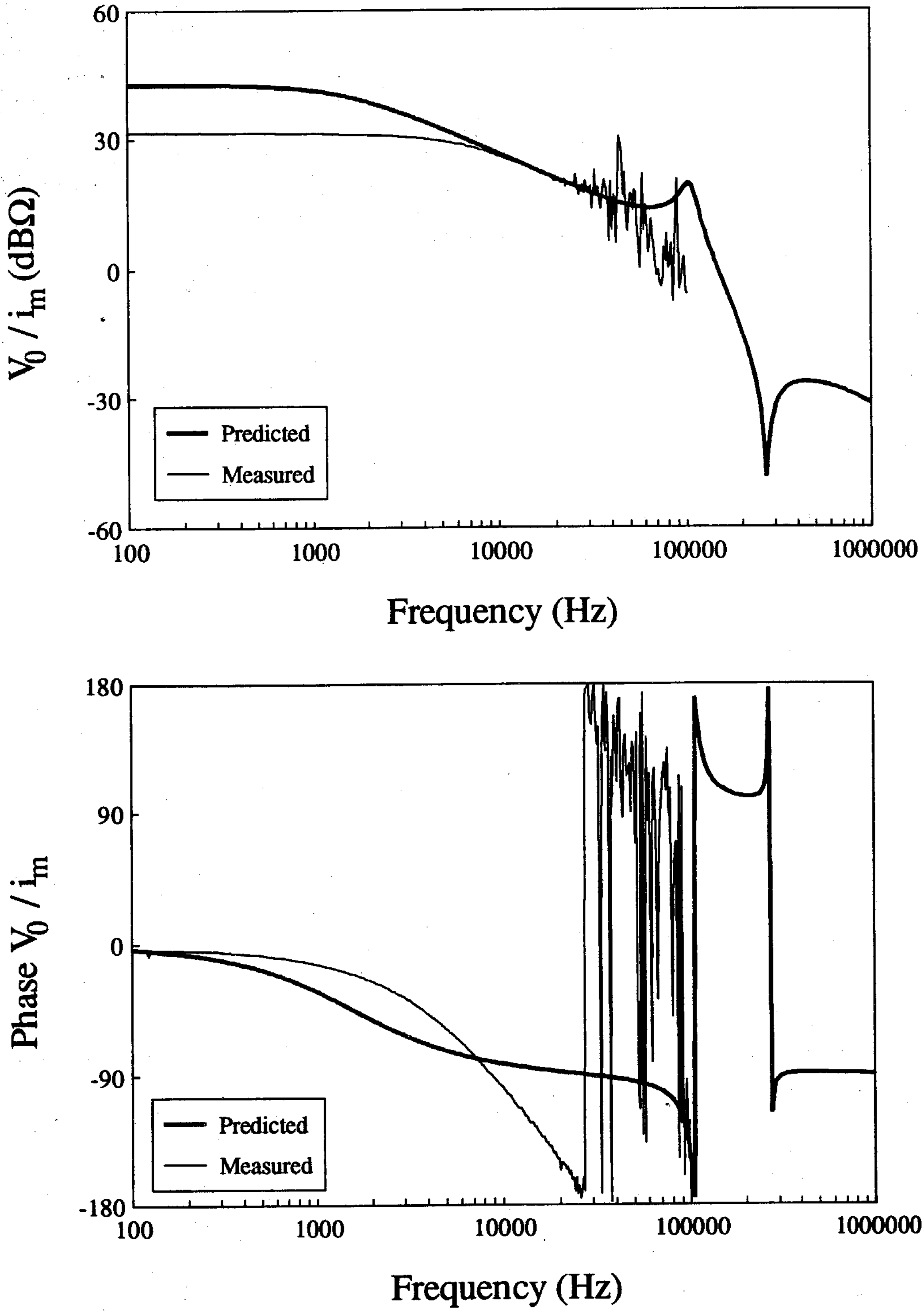


Figure 6.17: Measured Results from the TWT Filament Power Supply. The input voltage is 20 V, the output voltage is 10 V and the control current is 606 mA. The switching frequency of the power stage is 1 MHz.

an ungapped portion of the MR core. As the control current varies, the control winding saturate the portion of the core that they are wound on causing the variable inductance in the MR model as well as the variable inductance seen looking into the control winding. These two inductances are related but not the same value!

The highly nonlinear load that the control winding presents to the transistor current source will cause open loop oscillation of the control current unless R20 is present. Since the control winding has very low DC resistance, the power dissipated in R20 is very low. C24 is placed across the control winding also to bypass any leakage of the primary voltage into the control circuit. These two components together with the inductance of the control winding itself conspire to produce a lowpass filter which limits high frequency control currents.

6.4.3 Output Impedance Measurement

The output impedance exclusive of the output capacitance and load resistance, z'_o, can be measured using the circuit shown in Fig. 6.19. This measurement requires that the DC current probe be set to "AC" to avoid saturation of the current probe amplifier by the load current. In addition, it is necessary to use only the DC type current probes since the DC load current will saturate most AC current probes. The bias and MOSFET drive circuits have been omitted for clarity. This measurement is an open loop measurement so the control current to the magnetic regulator is adjusted manually using an external power supply to provide the necessary bias.

The measured z'_o is shown in Fig. 6.18. As one should expect, the output impedance is not infinite but is somewhat lower than the load impedance at low frequencies. The complex dynamics of the measured output impedance indicate a more refined model is in order.

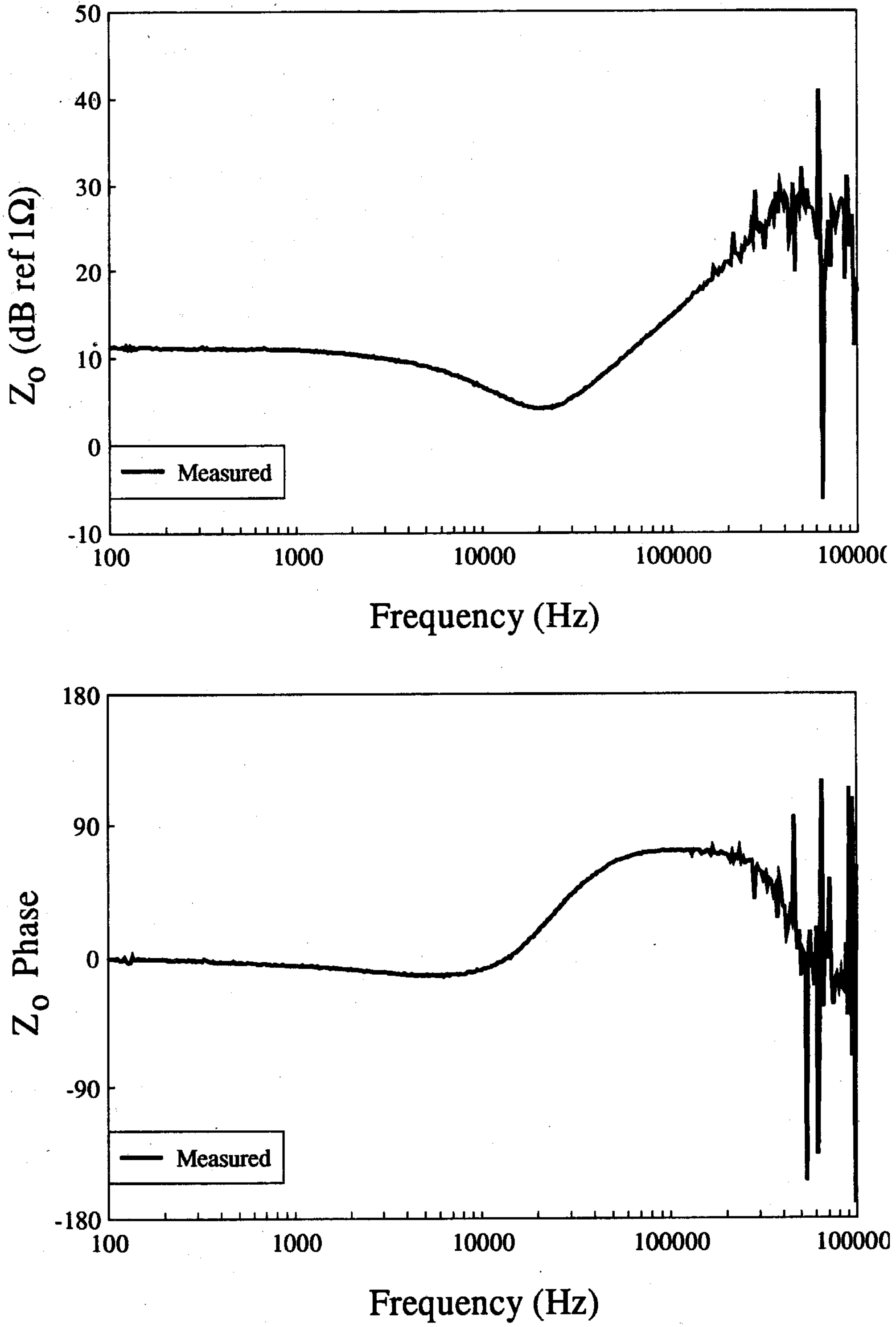


Figure 6.18: Measured Internal Output Impedance, z'_o. The present model for the resonant rectifier predicts an infinite output impedance so there is no predicted curve for comparison.

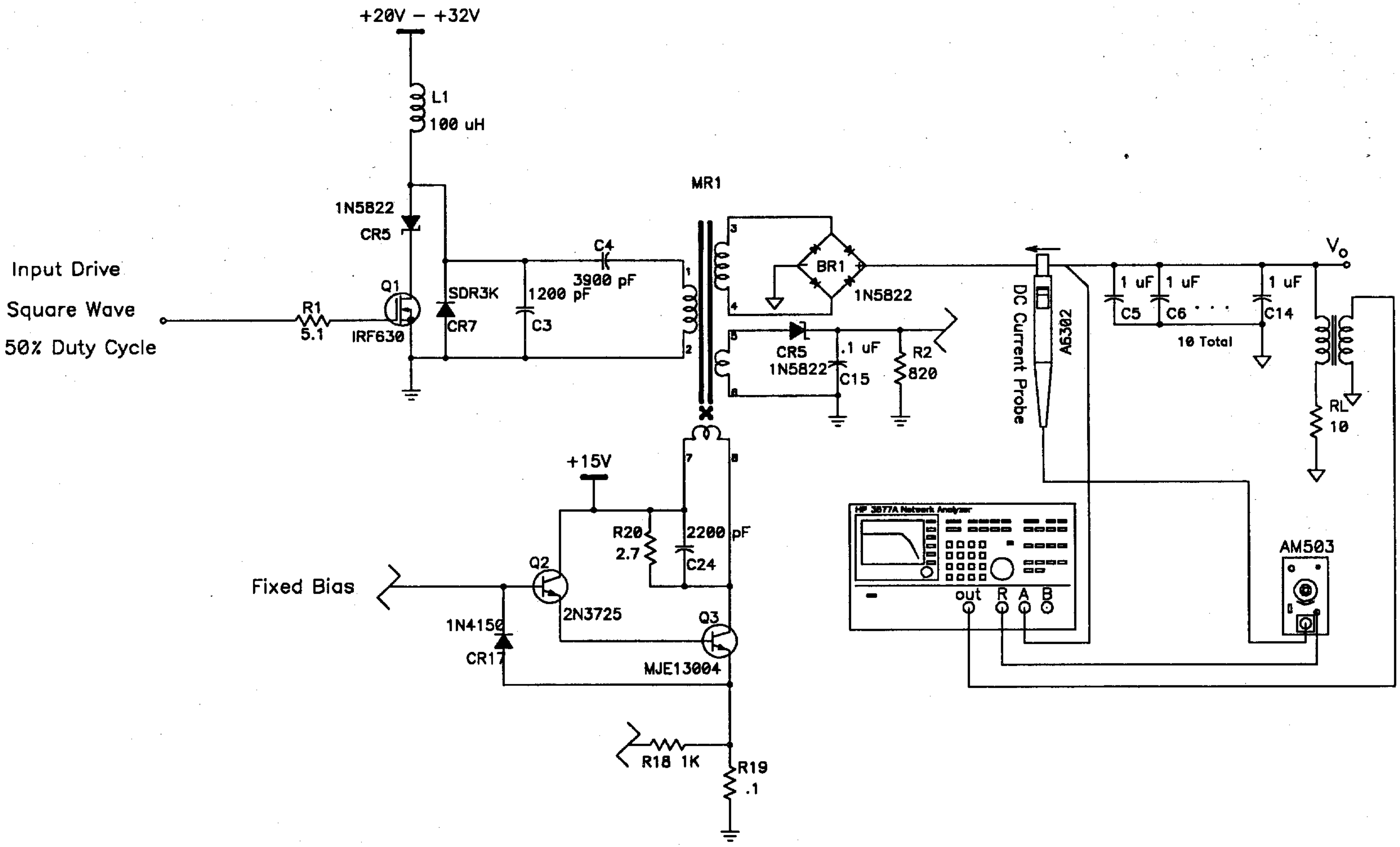


Figure 6.19: Experimental Setup Used to Measure z'_o. The HP 3577 Network Analyzer injects a test signal into the output of the DC-to-DC converter through a coupling transformer. A Tektronix DC current probe is used to sense the output current.

6.4.4 Interpretation of the Results

The predicted control-to-output transfer function is shown in Fig. 6.17 for comparison with the measurements. This model predicts an unrealistically high DC gain and low dominant pole frequency. The dominant pole shown is caused by the $R_L'C_L'$ time constant only which is a consequence of the infinite output impedance. Any finite value for the output impedance appears in parallel with the load resistance and hence raises the frequency of the dominant pole.

The model developed in this chapter has several severe limitations as shown in the results above. The low frequency control-to-output gain is quite inaccurate near DC and has a dominant pole significantly lower that the actual hardware. This stems from the fact that the predicted output impedance is infinite with this model. The problem of calculating a realistic value for the output impedance must begin with a rectifier model that couples disturbances in the output voltage back into the tank circuit. This will be the subject of the next chapter.

The features in the predicted response corresponding to the dynamics in the resonant tank circuit are predicted to be higher than it is possible to make control-to-output transfer function measurements. There are other useful transfer functions that can be measured to try to expose the high frequency dynamics of the tank circuit, such as the line-to-output transfer function. Obviously the simple model used here for the inverter precludes this calculation. A further verification of the model will appear in Chapter 8 where a more complete model for the inverter is developed.

The present model predicts an infinite output impedance when measured at z'_o which is clearly incorrect. This is because the simple rectifier model here is unilateral and therefore any perturbation applied to the output circuit is completely uncoupled from the tank circuit and the inverter. This deficiency in the model will be addressed in the next chapter.

Chapter 7

The First Order Model

Introduction

In this chapter the model for the DC-to-DC converter is refined to provide more accurate results for the control-to-output transfer function and the output impedance. In Chapter 6, the rectifier was modeled as a simple forward transfer characteristic with no reverse transfer. This is obviously unrealistic since changing loads will certainly affect the currents in the tank circuit. In the case of continuous diode conduction, the bridge rectifier is a bilateral network requiring a reverse transfer characteristic. Also including the reverse transfer characteristic has significant influence over the output impedance calculation.

In the previous chapter it was the output impedance that indicated the need for an improved rectifier model. The inclusion of the reverse transfer characteristic transforms the output impedance from a pure current source to one with a finite output impedance. In the development of the reverse-transfer model, it will be necessary to account not only for the amplitude modulation on the tank current but also any phase modulation that may be present. To deal with a waveform which contains both amplitude and phase modulation, a brief diversion is necessary to develop the mathematical relationships.

The new model developed in this chapter deals with phase modulation as well as amplitude modulation. Since phase modulation is very difficult to measure with conventional test equipment, the circuit simulation program SPICE is used to assist in the validation of the hand-calculated model. It was observed in Chapter 4 that the waveforms calculated by SPICE are quite close to those obtained from measurements. The model used by SPICE in this dynamic case is computationally intensive but practical to run for a few prototype circuits. The SPICE model is used mostly to validate the correctness of the calculations rather than to provide a practical tool for the analysis of this class of power system. The final test of the model will be the measured data from an actual circuit.

7.1 The Rectifier Dynamic Model

The model for the rectifier portion of the DC-to-DC converter done in Chapter 6 provides only part of the answer. That model addressed the forward transfer characteristic of the resonant rectifier. That is, given a known input current, what is the average current out of the bridge. This model is accurate if one knows the input current, knowledge which is not available *a priori*. To calculate the input current, there must be some model for the input port of the rectifier. In the previous chapter, that model was simply a voltage source whose waveform was unaltered by any modulation on the input current. It appeared as a short for all frequencies except the carrier frequency and its harmonics. A more accurate picture of the input port of the rectifier is needed.

The model for the input port of the rectifier will be developed first in words to provide a clear qualitative understanding of the model and its limitations. Prior to delving into the quantitative details of the rectifier model, two mathematical results need to be developed. The first is a general phasor form for low-frequency modulation of a carrier frequency which includes both amplitude and phase modulation. The second is a calculation to show the relationship between the modulating signal and the sidebands around the carrier frequency for the case of a non-sinusoidal carrier signal. With these two mathematical results and the qualitative model of the rectifier, the quantitative model will be easier to follow.

7.1.1 The Qualitative Rectifier Model

Figure 7.1 illustrates the circuit which will hereafter be referred to as the rectifier block. The shunt inductance L_m at the input serves to provide a pre-load to the driving circuit when the output load is removed. It also performs a kind of impedance matching function as more fully explained in Chapter 2. The terminal voltage applied to the inductor and the current through the inductor is controlled by the characteristics of the bridge rectifier and filter on the rectifier output so it is logical to include L_m with the rectifier circuits.

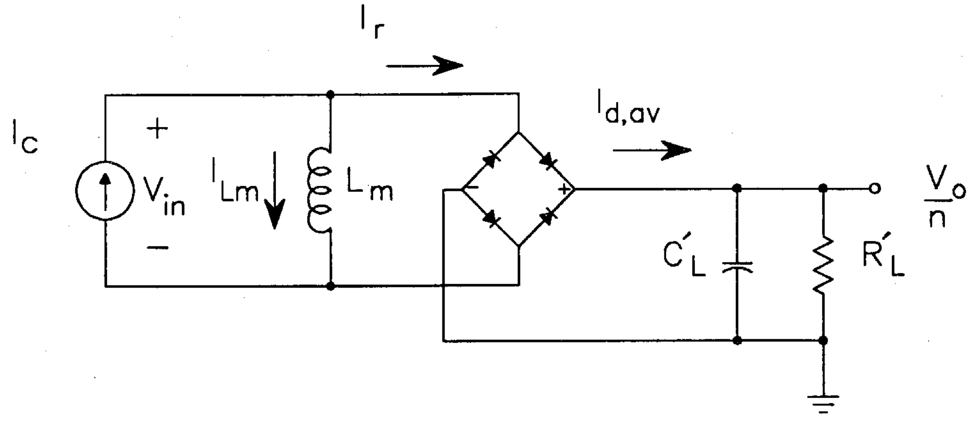


Figure 7.1: Schematic Diagram of the Rectifier Block. All the components are referred to the primary side of the magnetic regulator.

This model is only concerned with continuous diode conduction. Since the diodes are in continuous conduction, the input voltage is a square wave which switches between $+V_o/n$ and $-V_o/n$ (this is purposely neglecting the diode forward voltage drops for simplicity). The input current, I_c, to the rectifier block is assumed to be an ideal sine wave and the rectifier circuit is assumed to be symmetrical, so that the input square wave voltage has a 50% duty cycle. When the diodes are in conduction, they directly connect the input and output, thus any modulation of the output voltage will appear as pure amplitude modulation of the rectifier input voltage as illustrated in Fig. 7.2. For simplicity, the current I_r is shown with minimal distortion from the current in L_m. Note that the amplitude modula-

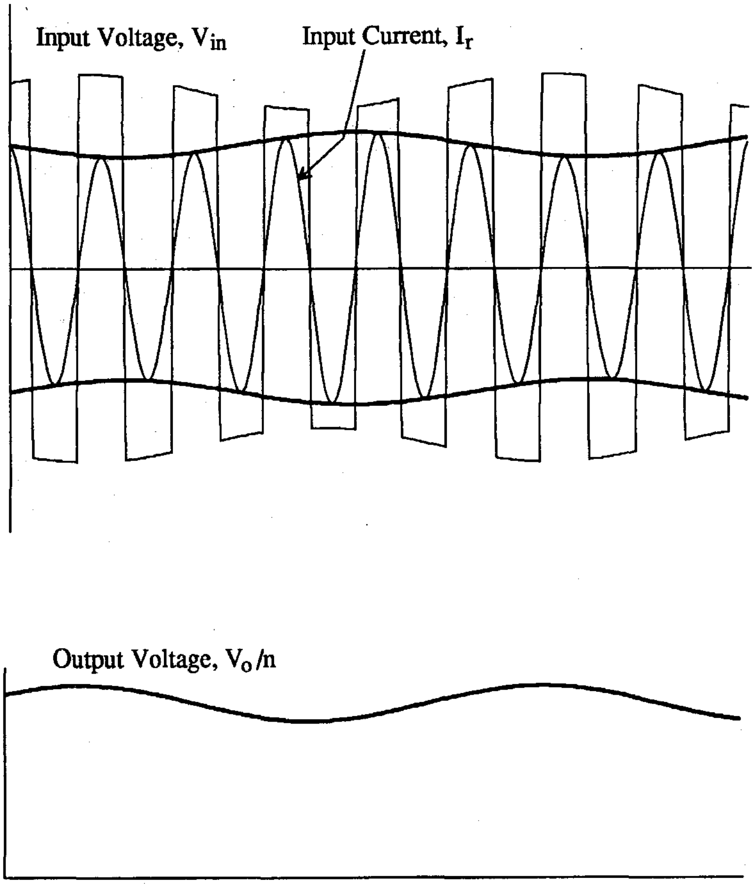


Figure 7.2: Voltage and Current Waveforms in the Rectifier Block with Amplitude Modulation Applied to the Input Current and Output Voltage. Note the envelope of the input voltage follows the output voltage while the phase of the carrier of the input voltage follows the input current.

tion on the input current is, in general, different from the amplitude modulation on the input voltage in magnitude and phase. The amplitude modulation on the input voltage will cause sidebands to appear on the input voltage which are readily computed below. In addition to the amplitude modulation of this square wave, there could also be phase modulation if the current into the bridge rectifier diodes should be phase modulated.

The diode bridge will switch when the polarity of the input current I_r changes; therefore, the input voltage to the rectifier will change polarity in precise phase with the input current *to the bridge diodes.* The current into the entire rectifier block is assumed to be a sine wave, but the input current to the rectifier bridge is a somewhat distorted waveform due to the action of the shunt inductance at the input. The current in the shunt inductor L_m is controlled by the voltage applied to the terminals of the inductor or, equivalently, to the input of the rectifier circuit. The input voltage is a square wave so the current in L_m will be a triangle wave. This triangle wave will subtract from the sine wave to produce the current that actually drives the diode bridge I_r. The waveforms in the rectifier are shown in 7.3 (a) and (b).

The Rectifier Forward Transfer Characteristic

In the rectifier model that was developed in Chapter 6, the envelope of the input current drive was converted into the average current from the diodes using a calculation based upon the static waveforms in Fig. 7.3. However, in the dynamic case, the inductor current will modulate in response to the input voltage. A more accurate model is to use the actual current into the diodes, I_r, in the calculation for the average output current from the bridge $I_{d,av}$. The simplest way to accomplish this is to say $I_{d,av}$ is a DC value with a modulation index that matches the modulation index of I_r. (The modulation index of a modulated DC signal is defined here as the amplitude of the modulation divided by the DC average value of the waveform. This corresponds to the parameter m in $A_c\,[1 + m\cos(\omega_m t)]$.) In this way the distortion of I_r is accounted for in the DC current calculation.

The Rectifier Reverse Transfer Characteristic

To contruct an accurate picture of the input voltage to the rectifier block, the reverse transfer characteristic of the rectifier must be considered. As mentioned above, any modulation on the output voltage will appear as amplitude modulation of the input voltage square wave. In addition, any phase modulation on the input current, I_r, will also appear as phase modulation on the input voltage. These two effects each create sidebands on the input voltage which must be combined to model the total effect. The amplitude modula-

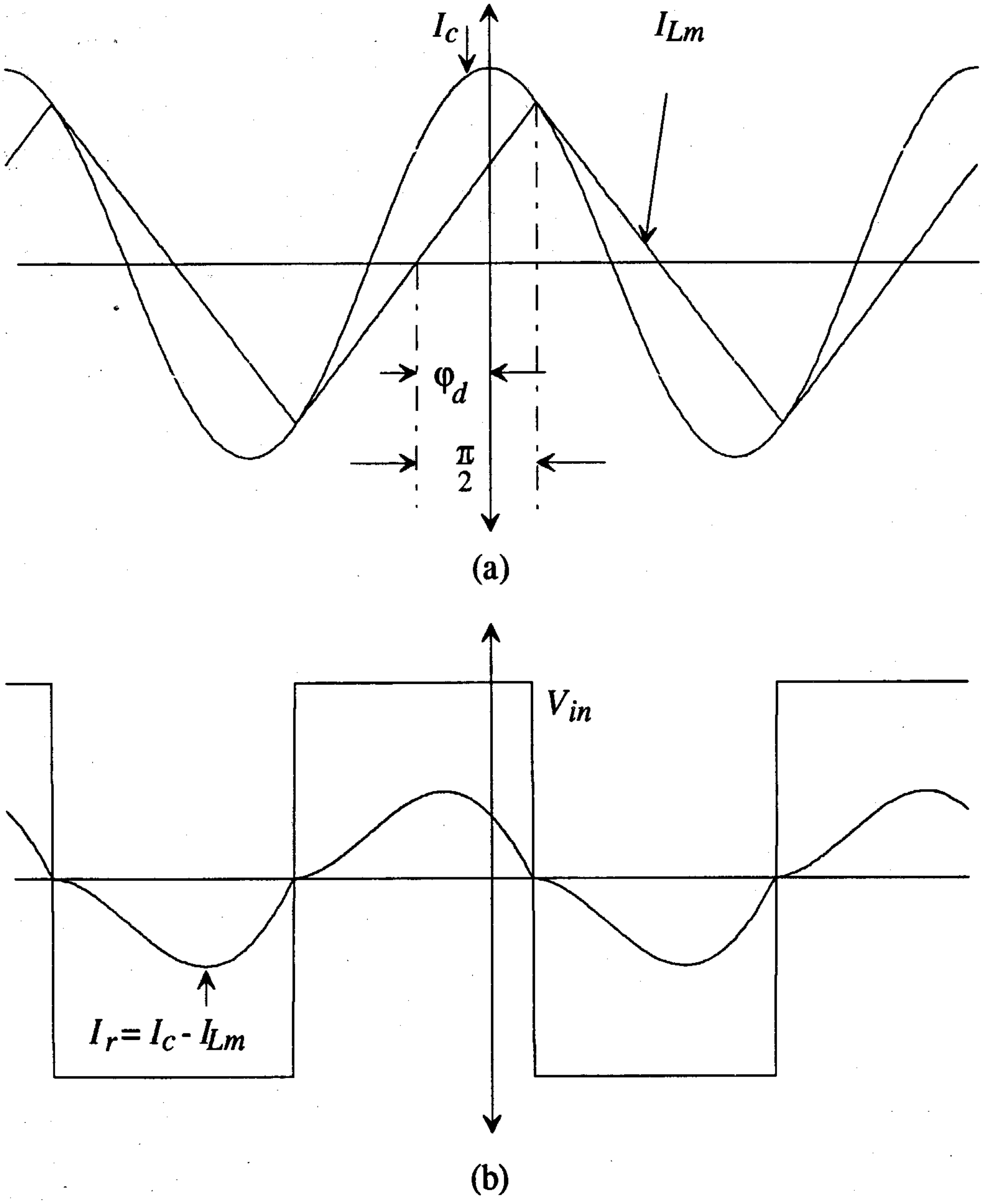


Figure 7.3: Steady-State waveforms in the Rectifier Block. The input current I_c and the inductor current I_{Lm} are shown in (a). The input voltage, V_{in}, and the current $I_r = I_c + I_{Lm}$ are shown in (b).

tion is accounted for by establishing that the modulation index of the output voltage is the same as the AM modulation index of the square wave input voltage. The phase modulation can also be handled in a similar fashion by saying that the phase modulation index on the input square wave is the same as the phase modulation index on the input current I_r.

For most practical cases the distorted waveform for I_r can be reasonably approximated by its fundamental waveform. This approximation will be less accurate as the boundary for discontinuous diode conduction is approached. Using the fundamental waveform of the input current results in a considerable simplification in the computation of the input characteristics of the rectifier.

To summarize, the qualitative model of the resonant rectifier is an input voltage that is a 50% duty-cycle square wave that switches between $+V_0/n$ and $-V_0/n$ with a phase shift that is in phase with the input current *to the bridge* (not to the rectifier block as a whole — see Fig. 7.3). The modulation on this input voltage is in two parts: 1) The amplitude modulation envelope is the same as the modulation of the output voltage and 2) the phase modulation is the same as the modulation of the fundamental of the current into the bridge rectifier. The output current is proportional to the amplitude modulation on the input current, I_r. Prior to using this description of the rectifier model for quantitative calculations, two useful mathematical results will be derived in the next sections.

7.1.2 General Modulation of a Carrier Signal

One of the essential tools required to construct the quantitative model for the resonant rectifier is the relationship between the modulation of a carrier signal, both in amplitude and phase, and the sidebands above and below the carrier frequency. The case of simple amplitude modulation was considered in Chapter 5 where it was shown that pure AM will cause sidebands above and below the carrier frequency that are equal in magnitude. In this section the more general case of AM and PM will be considered. Throughout this discussion the modulation signals are assumed to be small compared to the carrier signal. This assumption is well justified in the case of a small-signal analysis.

Consider a general modulation waveform in the form

$$f(t) = A_c [1 + m\cos(\omega_m t + \varphi_A)] \cos[\omega_c t + \varphi_c + K_p \cos(\omega_m t + \varphi_p)] \tag{7.1}$$

The subscript "c" refers to carrier-frequency related quantities, the subscript "m" refers to modulation-frequency related quantities, the subscript "p" refers to phase modulated quantities, and the subscript "A" refers to amplitude modulated quantities. By assumption, the parameters m and K_p are sufficiently small to ensure that only the sidebands immediately above and below the carrier frequency are of interest.

Next use the following definitions:

$$\begin{aligned} \theta_A &= \omega_m t + \varphi_A \\ \theta_p &= \omega_m t + \varphi_p \\ \theta_c &= \omega_c t + \varphi_c \end{aligned} \tag{7.2}$$

and consider the phase modulated part,

$$\cos(\theta_c + K_p \cos\theta_p) = \cos(\theta_c)\cos(K_p \cos\theta_p) - \sin(\theta_c)\sin(K_p \cos\theta_p) \tag{7.3}$$

The parameter K_p is small so the following approximations can be made:

$$\cos(K_p \cos\theta_p) \approx 1 \tag{7.4}$$

and

$$\sin(K_p \cos\theta_p) \approx K_p \cos\theta_p \tag{7.5}$$

These approximations transform 7.3 to

$$\cos(\theta_c + K_p \cos\theta_p) \approx \cos\theta_c - \sin(\theta_c) K_p \cos\theta_p \tag{7.6}$$

The trigonometric product rule provides

$$\sin x \cos y = \frac{1}{2}\sin(x+y) + \frac{1}{2}\sin(x-y) \tag{7.7}$$

and it follows that

$$\cos(\theta_c + K_p \cos\theta_p) \approx \cos\theta_c - \frac{K_p}{2}\sin(\theta_c + \theta_p) - \frac{K_p}{2}\sin(\theta_c - \theta_p) \tag{7.8}$$

This is the familiar result from communications theory for narrow-band PM, namely NBPM produces upper and lower sideband signals that are equal in magnitude but phase shifted from the carrier frequency. This signal is now multiplied by the AM envelope:

$$\begin{gathered}\frac{f(t)}{A_c} = \cos\theta_c - \frac{K_p}{2}\sin(\theta_c + \theta_p) - \frac{K_p}{2}\sin(\theta_c - \theta_p) + \\ m\cos\theta_A\cos\theta_c - \frac{K_p}{2}m\cos\theta_A\sin(\theta_c + \theta_p) - \frac{K_p}{2}m\cos\theta_A\sin(\theta_c - \theta_p)\end{gathered} \tag{7.9}$$

Since both the parameters K_p and m are small, the product $K_p m \approx 0$. This results in the following form for 7.9:

$$\frac{f(t)}{A_c} = \cos\theta_c + \frac{K_p}{2}\cos\left(\theta_c + \theta_p + \frac{\pi}{2}\right) + \frac{K_p}{2}\cos\left(\theta_c - \theta_p + \frac{\pi}{2}\right) + \left(\frac{m}{2}\cos(\theta_c + \theta_A) + \frac{m}{2}\cos(\theta_c - \theta_A)\right) \quad (7.10)$$

where

$$\sin\theta = \cos(\theta + (\pi/2)) \quad (7.11)$$

and

$$\cos x \cos y = (1/2)\cos(x+y) + (1/2)\cos(x-y) \quad (7.12)$$

were used. To best understand this result, consider the expanded form,

$$\begin{aligned}\frac{f(t)}{A_c} &= \cos\theta_c + \frac{K_p}{2}\cos\left((\omega_c + \omega_m)t + \varphi_c + \varphi_p + \frac{\pi}{2}\right)\\ &+ \frac{K_p}{2}\cos\left((\omega_c - \omega_m)t + \varphi_c - \varphi_p + \frac{\pi}{2}\right)\\ &+ \frac{m}{2}\cos((\omega_c + \omega_m)t + \varphi_c + \varphi_A)\\ &+ \frac{m}{2}\cos((\omega_c - \omega_m)t + \varphi_c - \varphi_A)\end{aligned} \quad (7.13)$$

This result is easy to interpret with the help of a graphical construction as shown in Fig. 7.4 and Fig. 7.5. These figures plot the magnitude and phase relationships of the various signals in 7.13, frozen in time at t=0. Notice that the inclusion of phase modulation with the amplitude modulation has resulted in a total signal where the upper sideband is different in magnitude from the lower sideband. Further, to work the process in reverse one must know both the magnitude and phase of the upper and lower sideband signals, a difficult requirement in practice since the ordinary swept spectrum analyzer is insensitive to

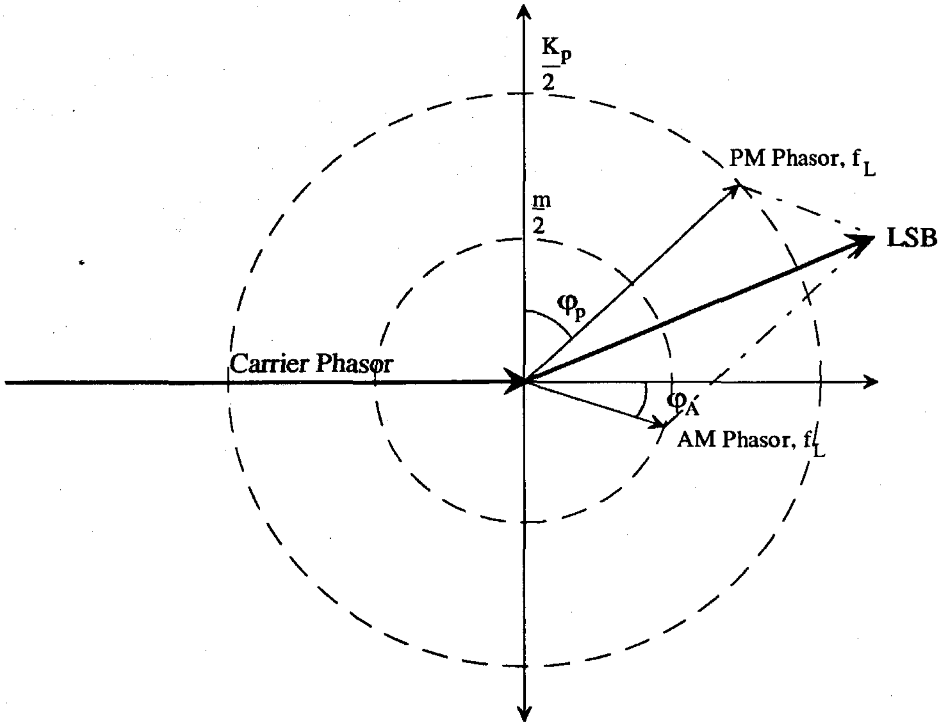


Figure 7.4: Phasor Relationship for the Signals at the Lower Sideband. The phase modulation of the carrier adds a component $90° - \varphi_p$ ahead of the carrier's phase. The amplitude modulation phasor has a phase that is $-\varphi_A$ with respect to the carrier.

phase. This shortcoming of the measured data is a significant handicap when the goal is to understand the response from the control input (or any low frequency input) to one of the modulated quantities such as the tank current. This problem motivated the use of the circuit simulation program SPICE to verify the models.

The use of complex notation will simplify the use of the above results. The nomenclature is:

$$me^{j\varphi_A} = \text{AM phasor} \tag{7.14}$$

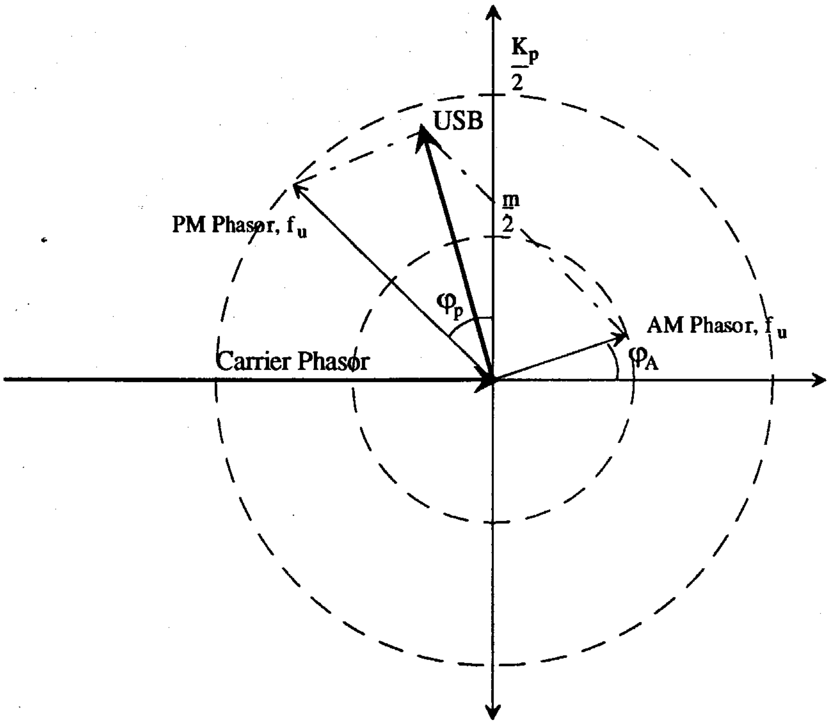


Figure 7.5: Phasor Relationship for the Signals at the Upper Sideband. The phase modulation of the carrier adds a component $90° + \varphi_p$ ahead of the carrier's phase. The amplitude modulation phasor has a phase that is φ_A with respect to the carrier.

$$K_p e^{j\varphi_p} = \text{PM phasor} \tag{7.15}$$

$$USB = \text{Upper Sideband Signal} = D_1 + jD_2 \tag{7.16}$$

$$LSB = \text{Lower Sideband Signal} = D_3 + jD_4 \tag{7.17}$$

The D_i are the real and imaginary parts of the sideband signals. From the graphical construction it can be seen that

$$\begin{aligned} USB &= \frac{m}{2}e^{j\varphi_A} + \frac{K_p}{2}e^{j\left(\frac{\pi}{2}+\varphi_p\right)} \\ &= \frac{m}{2}e^{j\varphi_A} + \frac{K_p}{2}e^{j\varphi_p}e^{j\frac{\pi}{2}} \\ &= \frac{m}{2}e^{j\varphi_A} + j\frac{K_p}{2}e^{j\varphi_p} \end{aligned} \tag{7.18}$$

$$\begin{aligned} LSB &= \frac{m}{2}e^{-j\varphi_A} + \frac{K_p}{2}e^{j\left(\frac{\pi}{2}-\varphi_p\right)} \\ &= \frac{m}{2}e^{-j\varphi_A} + \frac{K_p}{2}e^{-j\varphi_p}e^{j\frac{\pi}{2}} \\ &= \frac{m}{2}e^{-j\varphi_A} + j\frac{K_p}{2}e^{-j\varphi_p} \end{aligned} \tag{7.19}$$

It now follows that

$$USB + \overline{LSB} = me^{j\varphi_A} \tag{7.20}$$

and,

$$j(\overline{LSB} - USB) = K_p e^{j\varphi_p} \tag{7.21}$$

where the bar denotes complex conjugate.

The results 7.20 and 7.21 will prove to be key relationships in the model development that follows.

7.1.3 Spectrum of a Modulated Non-Sinusoidal Carrier Signal

AM Modulation of a General Carrier Waveform

Many of the signals in the resonant DC-to-DC converter are non-sinusoidal in the steady state, with slow modulation of either the amplitude or phase or both in the dynamic case. To properly account for these signals, it is necessary to extract the low-frequency modulation information and the fundamental information from the many harmonics present in the total signal. Since the goal of the analysis is to develop a small-signal model, only the first-order terms should be retained. For example, assume a general carrier frequency of 1 MHz is modulated by 10 kHz. The signals of interest would be:

1. The DC average.
2. The fundamental of the carrier frequency at 1 MHz.
3. The upper and lower sideband frequencies at 1.01 MHz and 990 kHz respectively.
4. The fundamental of the modulation at 10 kHz.

Items 1 and 2 are necessary to calculate the steady-state operating point and items 3 and 4 are used possibly in conjunction with 1 and 2 to derive the dynamic response. (As mentioned above, the modulation index of a mostly DC signal is defined as the ratio of the modulation amplitude to the DC average value.) With these requirements in mind, consider the following

$$F(t) = M(t)g(t) \tag{7.22}$$

where $M(t)$ is a general modulation function which is periodic with a period T_m and $g(t)$ is a general carrier-wave function which is periodic with period T_c. It will be assummed that $T_c << T_m$ to preserve the idea that $F(t)$ is a high-frequency signal with low-frequency modulation. In general, both $M(t)$ and $g(t)$ may be rich in harmonics and therefore the product will also be rich in harmonics. For the small signal case, it is only necessary to consider the four frequencies, DC, f_c, f_c+f_m, and f_c-f_m (these signals are the first-order signals). The spectrum of $F(t)$ is needed so the first order signals may be selected out. This is accomplished by decomposing $F(t)$ into a Fourier series:

$$F(t) = a_0 + \sum_{n=1}^{\infty} a_n \cos\omega_n t + b_n \sin\omega_n t \tag{7.23}$$

where

$$a_0 = \frac{1}{T}\int_0^T F(t)\,dt \tag{7.24}$$

$$a_n = \frac{2}{T}\int_0^T F(t)\cos\omega_n t\,dt \tag{7.25}$$

$$b_n = \frac{2}{T}\int_0^T F(t)\sin\omega_n t\,dt \tag{7.26}$$

The length of the integration interval is the only part of this problem that is not standard; the Fourier series coefficients must be evaluated by integrating over one cycle of the periodic function $F(t)$. This means that there must be an integer number of cycles of both the carrier signal and the modulation signal. This can be expressed as $T = pT_c = qT_m$ where p and q are integers. To determine p and q, the quotient p/q should be reduced to the lowest terms and these values used (a limit must be used if the relationship between the frequencies is irrational). For example, suppose $f_m = 1/T_m = 13$ kHz and $f_c = 180$ kHz. The quotient in lowest terms is

$$\frac{p}{q} = \frac{T_m}{T_c} = \frac{f_c}{f_m} = \frac{180}{13} \qquad (7.27)$$

so that $p = 180$ and $q = 13$. The period of integration would be $pTc = 180(1/180\ \mathrm{kHz})$ or 1 mSec. The signals of interest would be found from $n = 13$ for the fundamental of the modulation frequency, $n = 167$ for the lower sideband, $n = 193$ for the upper sideband and finally, $n = 180$ for the carrier frequency. This value of T will be implied in all subsequent Fourier series calculations.

The next task is to find a value for the upper and lower sidebands in terms of the known spectra of $M(t)$ and $g(t)$. Assume the Fourier series are known for each $M(t)$ and $g(t)$:

$$M(t) = a_{m0} + \sum_{n=1}^{\infty} a_{mn} \cos\omega_n t + b_{mn} \sin\omega_n t \qquad (7.28)$$

$$g(t) = a_{g0} + \sum_{n=1}^{\infty} a_{gn} \cos\omega_n t + b_{gn} \sin\omega_n t \qquad (7.29)$$

Any practical signals for $g(t)$ and $M(t)$ will be sufficiently well-behaved that the series may be multiplied term-by-term. The following shorthand notation is used:

$$a_{m0} = DC_m \qquad (7.30)$$

$$a_{g0} = DC_g \qquad (7.31)$$

$$a_{mi} \cos\omega_m t + b_{mi} \sin\omega_m t = f_m \qquad (7.32)$$

$$a_{m2i} \cos 2\omega_m t + b_{m2i} \sin 2\omega_m t = f_{2m} \ldots \text{etc.} \qquad (7.33)$$

The integer i is whatever is necessary so that $i\omega_i = \omega_m$. Similarly,

$$a_{gj}\cos\omega_c t + b_{gj}\sin\omega_c t = f_c \tag{7.34}$$

$$a_{g2j}\cos 2\omega_c t + b_{g2j}\sin 2\omega_c t = f_{2c}\ldots\text{etc.} \tag{7.35}$$

This enables the product to be written as:

$$F(t) = (DC_m + f_m + f_{2m} + f_{3m} + \ldots)\,(DC_g + f_c + f_{2c} + f_{3c} + \ldots) \tag{7.36}$$

By rearranging this representation of $F(t)$, the desired form is obtained:

$$F(t) = DC_m DC_g + DC_m f_c + DC_c f_m + f_m f_c + \ldots \tag{7.37}$$

In the case of the small-signal model the modulation is assumed to be a small, low-frequency modulation which is sinusoidal (or nearly so) and the carrier is a high frequency non-sinusoidal waveform. Under these conditions, the modulation function is

$$M(t) = 1 + m\cos(\omega_m t + \varphi_m) \tag{7.38}$$

The following result is obtained using 7.38 in 7.37:

$$F(t) = DC_c + DC_c(m\cos(\omega_m t + \varphi_m)) + f_c + f_c m\cos(\omega_m t + \varphi_m) + \ldots \tag{7.39}$$

The only term that needs further expansion is the last one,

$$\begin{aligned} f_c m\cos(\omega_m t + \varphi_m) &= A_g\cos(\omega_c t + \varphi_c)\, m\cos(\omega_m t + \varphi_m) \\ &= mA_g\cos\theta_c\cos\theta_m \\ &= \frac{mA_g}{2}\cos(\theta_c + \theta_m) + \frac{mA_g}{2}\cos(\theta_c - \theta_m) \end{aligned}$$

$$= \frac{mA_g}{2}\cos\left(\left(\omega_c+\omega_m\right)t+\varphi_c+\varphi_m\right)+\frac{mA_g}{2}\cos\left(\left(\omega_c-\omega_m\right)t+\varphi_c-\varphi_m\right) \qquad (7.40)$$

The assumption that the modulation signal is small and low frequency means that the additional terms not explicitly listed in 7.39 will not contribute any significant signals at any of the frequencies of interest. This result can be summarized as: The spectrum of a signal with small, low-frequency modulation consists of the DC of the carrier, the fundamental of the carrier, the DC value of the carrier times the amplitude of the modulating function at the modulation frequency, and equal upper and lower sidebands. The magnitude of the sidebands is equal to the modulation amplitude times the fundamental of the carrier signal times 1/2. The phase of the upper sideband is equal to the sum of the phases of the carrier and modulation signals while the phase of the lower sideband is the difference between the carrier signal's phase and the modulation signal's phase.

Example of AM Modulation

To illustrate the results derived above, consider the following example. Assume a carrier signal with the following characteristics: a square wave with a 20 V amplitude (peak-to-peak) at 1 MHz, phase shift of 10°, and DC value of 0.5 V. AM modulation with a modulation index m=.1, phase shift of 60°, and frequency 5 kHz is impressed upon the carrier. What are the amplitudes of the significant signals?

The fundamental of a square wave signal is 4/π times the 1/2 the peak-to-peak value or approximately $1.27 \times 10\ \mathrm{V} = 12.7\ \mathrm{V}$. The results for all the interesting signals are shown inTable 7.1.

Numerical Verification of the AM Modulation Example

A useful exercise is to numerically verify the results calculated above. This is accomplished by calculating the modulated waveform in the time domain then applying the fast

Table 7.1: Signal Magnitudes and Phases for the AM Modulation Example.

Signal	Amplitude (V)	Phase (°)	Frequency (MHz)
DC	0.5	-	-
Baseband	.05	60	.005
Carrier	12.73	10	1.0
Upper Sideband	.6366	70	1.005
Lower Sideband	.6366	-50	0.995

Fourier transform (FFT) to extract the signals of interest. This exercise serves two useful purposes: The hand calculation is checked for any error and, more importantly, the process of calculating the waveform numerically involves finding the values of $F(t)$ at discrete points in time and then applying a discrete Fourier transform through the FFT [21]. This calculation will result in aliasing since the spectrum of a square wave extends to infinite frequency. The best way to combat this problem is to sample at a sufficiently high frequency that the high-frequency harmonics which are folded into the low-frequency spectrum by the sampling process do not significantly alter the results. To determine an appropriate sampling frequency, several FFT's can be calculated with succesively larger numbers of samples. The minimum sample frequency is then determined from the spectra that result. When the signals of interest do not change significantly with higher sampling frequencies, the minimum value has been found.

The required sampling frequency will be relevant when circuit simulation is used to verify the rectifier model. The circuit simulation program SPICE calculates the voltages and currents in the circuit at discrete points in time and then uses an FFT to compute the spectrum. Even without errors in the calculation of the voltages and currents (not a good assumption in practice), the discrete-time nature of the SPICE calculation will lead to errors in the results. The simple mathematical calculation done in this section provides a lower bound on the errors found using SPICE.

The numerical calculation uses the program Mathcad™ [22] to calculate the values of $F(t)$ at $N = 2^n$ prescribed points in time then calculate the FFT. The equation used to generate the points is

$$F(t) = (A_c \{\mathrm{sgn}\,[\cos(\omega_c t + \varphi_c)]\} + DC)\,(1 + m\cos(\omega_m t + \varphi_{AM})) \tag{7.41}$$

where

A_c = Amplitude of the carrier = 10

$\omega_c = 2\pi f_c = 2\pi\,(1\mathrm{MHz})$

$\varphi_c = 10°$

DC = DC offset = 0.5

m = Modulation index = 0.1

$\omega_m = 2\pi f_m = 2\pi\,(1\mathrm{kHz})$

$\varphi_{AM} = 60°$

The results from Mathcad™ are shown in Table 7.2. Note that the most sensitive parameters are the phases of the various signals but even these are of reasonable engineering accuracy for the minimun number of samples, N=512. This should be contrasted with the results of the next section which is the case of phase modulation.

PM Modulation of a General Carrier Waveform

The second type of modulation in the DC-to-DC converter is in phase modulation. This is a natural consequence of the network and not directly under the control of the designer. The rectifier model needs to include this effect since it is present in the actual hardware. For the rectifier circuit, the waveforms that contain phase modulation are the input current and the input voltage. The current is the driving function and the voltage is the result. The input voltage is a square wave with phase modulation impressed upon it by

Table 7.2: Numerically Calculated Results for the AM Modulation Example

Signal	Calculated Value	Numerically Calculated values for $N=2^n$ data points			
		n=9	n=10	n=11	n=12
DC offset	0.5	0.500	0.500	0.500	0.500
Baseband Magnitude	0.05	0.050	0.050	0.050	0.050
Baseband Phase (°)	60	60	60	60	60
Carrier Magnitude	12.7324	12.7375	12.7337	12.7327	12.7325
Carrier Phase (°)	10	8.44	9.84	10.54	10.19
USB Magnitude	0.63662	0.63688	0.63668	0.63664	0.63662
USB Phase (°)	70	68.44	69.84	70.54	70.19
LSB Magnitude	.63662	0.63688	0.63668	0.63664	0.63662
LSB Phase (°)	-50	-51.56	-50.16	-49.45	-49.8

the input current. The goal in this section is to calculate the spectrum of a general carrier waveform that is undergoing phase modulation. The desired model is a small-signal model, so the phase deviation of the phase modulation will be assumed to be sufficiently small such that only the first-order terms are significant. The general plan of attack is to represent the general carrier waveform as a Fourier series and then apply narrowband phase modulation (NBPM) to each of the terms. The terms that are at DC, the modulation frequency, the carrier frequency, and the first-order sidebands will be selected and all others ignored.

The analysis begins with the general form for the phase modulation. Assume that a periodic function $g(\omega t)$ exists. This function depends on the variable ωt and is assumed to be periodic with period 2π. A phase shift in this function may be added by replacing ωt with the argument $\omega t + \varphi$. If φ is itself made a periodic function of time, then g will be phase modulated. The phase modulation will be assumed to be sinusoidal in nature so the argument of g becomes

$$\omega_c t + \varphi_c + K_p \cos(\omega_m t + \varphi_{PM}) \tag{7.42}$$

The subscript c has been added to emphasize that the function g is a high-frequency carrier signal and the subscript m denotes a low-frequency modulation signal. The parameter K_p is assumed to be small. The factors φ_c and φ_{PM} allow for the possibility that the carrier frequency may be phase-shifted as well as the modulation frequency. Assume $g(\omega t)$ prior to any modulation can be represented with a Fourier series,

$$g(\omega_c t) = a_{c0} + \sum_{n=1}^{\infty} a_{cn} \cos(n\omega_c t + \varphi_{cn}) \tag{7.43}$$

The phase modulation is added to 7.43 by inserting the phase-modulation argument 7.42 to get

$$g(\omega_c t) = a_{c0} + \sum_{n=1}^{\infty} a_{cn} \cos(n\omega_c t + \varphi_{cn} + nK_p \cos(\omega_m t + \varphi_{PM})) \tag{7.44}$$

The same method used in section 7.1.2 can now be used term-by-term on 7.44 to expand each modulated cosine into upper and lower sidebands. Each term may be expanded by using 7.8 which is repeated here as 7.45.

$$\cos(\theta_c + K_p \cos\theta_p) \approx \cos\theta_c - \frac{K_p}{2}\sin(\theta_c + \theta_p) - \frac{K_p}{2}\sin(\theta_c - \theta_p) \tag{7.45}$$

This result is used in 7.44 to obtain

$$\begin{aligned} g(\omega_c t) &= a_{c0} + a_{c1}\cos(\omega_c t + \varphi_{c1}) + \frac{a_{c1}K_p}{2}\cos\left(\omega_u t + \varphi_{c1} + \varphi_{PM} + \frac{\pi}{2}\right) \\ &\quad + \frac{a_{c1}K_p}{2}\cos\left(\omega_L t + \varphi_{c1} - \varphi_{PM} + \frac{\pi}{2}\right) + \ldots \end{aligned} \tag{7.46}$$

where

$$\omega_u = \omega_c + \omega_m$$

$$\omega_L = \omega_c - \omega_m$$

and

$$\sin\theta = \cos(\theta + (\pi/2))$$

Equation 7.46 contains the information desired. The effect of phase modulation on a non-sinusoidal carrier signal is the generation of an upper and lower sideband whose amplitudes are 1/2 times the amplitude of the fundamental of the carrier signal times the phase modulation deviation K_p. The upper sideband has a phase shift that is the sum of the carrier and modulation phase shifts plus an additional $\pi/2$. The lower sideband's phase shift is the carrier phase shift minus the modulation signal's phase shift plus the same additional $\pi/2$.

Example of PM Modulation

Assume a carrier signal is a square wave with a 20 V amplitude (peak-to-peak) at 1 MHz, phase shift of 10°, and DC value of .5 V . It has PM modulation with a modulation index K_p=.1, phase shift of 60°, and frequency 5 kHz is impressed upon the carrier. What are the amplitudes of the significant signals?

The results of this section show that the spectrum contains the signals in Table 7.1.

Table 7.3: Phase Modulation Example Results

Signal	Amplitude (V)	Phase (°)	Frequency (MHz)
DC	0.5	-	-
Baseband	0	-	.005
Carrier	12.73	10	1.0
Upper Side-band	0.636	160	1.005
Lower Side-band	0.636	40	0.995

Numerical Verification of the Phase Modulation Example

As in the previous example, the results calculated for the phase modulation can be checked numerically. The equation used in Mathcad™ is

$$F(t) = (A_c\{\operatorname{sgn}[\cos(\omega_c t + \varphi_c + K_p \cos(\omega_m t + \varphi_{PM}))]\} + DC) \qquad (7.47)$$

where

A_c = Amplitude of the carrier = 10

$\omega_c = 2\pi f_c = 2\pi\,(1\mathrm{MHz})$

$\varphi_c = 10°$

DC = DC offset = 0.5

K_p = Phase Modulation Index = 0.1

$\omega_m = 2\pi f_m = 2\pi\,(1\mathrm{kHz})$

$\varphi_{PM} = 60°$

The numerical results are shown in Table 7.2. In this case, the numerical calculation is checking one additional effect besides those mentioned in the AM example, and that is the accuracy of the NBPM approximation. The fact that the carrier amplitude never reaches the value of the prediction even for n=16 (over 65,000 data points) indicates the NBPM approximation is at fault. An exact analysis of phase modulation shows that the carrier amplitude is multiplied by $J_0(K_p)$ which is approximately 0.9975. This would predict a carrier magnitude of 12.7006 V which agrees with the numerical result. Notice that the results are more sensitive to the number of samples used than in the AM case. Reasonable engineering accuracy is obtained for n=10, and good accuracy is obtained for n=12. In this example there are 200 cycles of the carrier for one cycle of the modulation, and for n=12 there are 4096 samples per modulation cycle. This implies approximately 21 samples per carrier cycle are required to get good accuracy, but as few as 6 samples per modulation cycle give reasonable results. This illustrates the problem with SPICE simulations of this circuit: If the modulation frequency is low, a tremendous number of data points must be calculated to get a reasonable result (for example, if the response to modulation at 100 Hz were desired, 60,000 data points would be indicated). Once the Spice analysis is run at any particular modulation frequency, the results constitute one magnitude and phase point on a bode plot. The simulation would then need to be run 50 or 100 times to get just one bode plot. This is obviously impractical so SPICE calculations will be restricted to a few runs to get the frequency response at a small number of selected frequencies.

Table 7.4: Numerically Calculated Results for the PM Modulation Example

Signal	Calculated Value	Numerically Calculated values for $N=2^n$ data points			
		n=9	n=10	n=12	n=16
DC offset	0.5	0.421	0.4805	0.490	0.5006
Baseband Magnitude	0.0	0.051	0.037	0.011	0.0006
Carrier Magnitude	12.7324	12.703	12.7002	12.6997	12.7006
Carrier Phase (°)	10	9.84	10.02	10.02	10.01
USB Magnitude	0.63662	0.6122	0.6401	0.6425	0.6356
USB Phase (°)	160	165.8	159.2	159.5	160.1
LSB Magnitude	.63662	0.6125	0.6381	0.6430	0.6355
LSB Phase (°)	40	32.60	41.86	40.69	39.95

7.1.4 The Quantitative Rectifier Model

Model Assumptions

The results of the previous two sections together with the qualitative model for the rectifier can now be combined to give a quantitative model for the rectifier circuit. This model is bilateral; that is, changes in the input current affect the output current and changes in the output voltage affect the input voltage. This model also attempts to account for the dynamic current in the input shunt inductor. The diodes are assumed to be in continuous conduction and are further assumed to be ideal. This model also assumes that the input current is sinusoidal with small amplitude and/or phase modulation.

The Rectifier Mathematical Model

The equivalent circuit for the new rectifier model is shown in Fig. 7.6. It is important to keep a mental picture of the various signals involved in this model. The signals on the input side are large sinusoidal signals with small modulation while the signals on the output side are mostly DC with small AC perturbations. This model shown in Fig. 7.6 is a small-signal model, so the DC voltages and currents along with the carrier-frequency terms are omitted leaving only the perturbation terms.

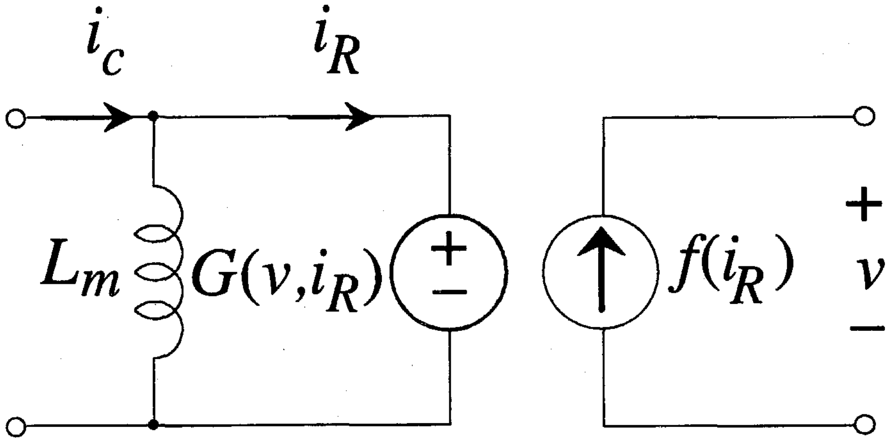


Figure 7.6: The New Model for the Rectifier Block. The output voltage in this model will affect the input through the voltage source $G(v)$. This model also accounts for the modulation of the inductor current by explicitly showing the inductor and its dependence upon $G(v)$.

The voltage source $G(v)$ represents the signals at the upper and lower sideband frequencies. The carrier waveform for $G(v)$ is a square wave so the fundamental of a square wave is used to determine the sidebands denoted by G_{USB} and G_{LSB}. The values are

$G_{USB}(v) \;=\; (\text{AM Mod. from } v_{out} + \text{PM Mod. from } i_R)$ @ the Carrier's Phase Shift

or, mathematically,

$$G_{USB}(v) \;=\; \left(\frac{m}{2}\frac{4}{\pi}V_{DC} + \frac{K_p}{2}\frac{4}{\pi}V_{DC}e^{j\frac{\pi}{2}}\right)e^{j\varphi_d} \tag{7.48}$$

The parameter m is the AM modulation index of the output voltage v. The output voltage v is assumed to contain a steady, DC value of V_{DC} with an AC perturbation $\hat{v}$. The parameter m is then $\hat{v}/V_{DC}$. Note that m is a complex number with magnitude and phase. The modulation index is divided by 2 since the modulation splits into an upper and lower sideband. The factor $4/\pi$ converts the amplitude of the square wave at the input into the fundamental at the input. The amplitude of the square wave at the input is equal to the DC output voltage. (More precisely, the amplitude of the square wave is the reflected DC output voltage plus any diode drops in the rectifier also scaled to the primary side of the ideal transformer.)

The second term in 7.48 is the PM term. K_p is the phase-modulation index of the input current i_R. The phase modulation on the current i_R can be expressed as

$$K_p \;=\; \left[\overline{\left(\frac{i_{r_L}}{i_{r_c}}\right)} - \frac{i_{r_u}}{i_{r_c}}\right]e^{j\frac{\pi}{2}} \tag{7.49}$$

where

i_{r_L} = Component of i_r at the lower sideband frequency

i_{r_u} = Component of i_r at the upper sideband frequency

i_{r_c} = Component of i_r at the carrier frequency

The parameter K_p in 7.48 is divided by 2 just as m was. Since the second term involves phase modulation, it is shifted ahead of the amplitude modulation by $\pi/2$. The phase modulation term is also scaled by the amplitude of the fundamental of the input voltage waveform which is the purpose of the $(4/\pi)V_{DC}$ term.

Equation 7.48 can be simplified by using the above definitions of m and K_p:

$$G_{USB}(v) = \frac{2}{\pi}\left\{\hat{v} + V_{DC}\left[\overline{\left(\frac{i_{r_L}}{i_{r_c}}\right)} - \frac{i_{r_u}}{i_{r_c}}\right]e^{j\pi}\right\}e^{j\varphi_d} \tag{7.50}$$

The signal at the lower sideband is very similar to that at the upper sideband except the phase shift of the lower sideband signal is $\varphi_c - \varphi_m$ rather than $\varphi_c + \varphi_m$ as it is for the upper sideband:

$$G_{LSB}(v) = \left(\frac{\overline{m}}{2}\frac{4}{\pi}V_{DC} + \frac{\overline{K_p}}{2}\frac{4}{\pi}V_{DC}e^{j\frac{\pi}{2}}\right)e^{j\varphi_d} \tag{7.51}$$

which simplifies to

$$G_{LSB}(v) = \frac{2}{\pi}\left\{\bar{\hat{v}} + V_{DC}\left[\frac{i_{r_L}}{i_{r_c}} - \overline{\left(\frac{i_{r_u}}{i_{r_c}}\right)}\right]\right\}e^{j\varphi_d} \tag{7.52}$$

The forward conversion characteristic can be described in words as a DC output current which is modulated with the same amplitude modulation index as the input current to the bridge rectifier. Mathematically this is represented as

$$f(i) = m_{i_r} i_{d,av} \tag{7.53}$$

where m_{i_r} is the AM modulation index of the input current i_r and $i_{d,av}$ is the average DC output current calculated at the steady-state operating point. The final result is

$$f(i) = i_{d,av}\left[\frac{i_{r_u}}{i_{r_c}} + \overline{\left(\frac{i_{r_L}}{i_{r_c}}\right)}\right] \tag{7.54}$$

Equations 7.50, 7.52 and 7.54 fully define the bilateral rectifier model. Prior to using this model in the DC-to-DC converter, however, it is useful to verify the model using circuit simulation. Since a complete bode plot of a circuit containing the resonant rectifier is rather impractical, the characteristics of the rectifier will be examined for only one selected modulation frequency.

SPICE Simulation of the Resonant Rectifier

The simulation of the resonant rectifer model is a computationally-intensive operation since several steps must be performed:

1. A transient simulation must be run using independent sources as inputs which have sinusoidal waveforms. Note that this is fundamentally different from the SPICE AC analysis mode. In the AC analysis mode, the program solves a nonlinear circuit for its operating point then linearizes all nonlinear elements about the operating point. This sort of analysis cannot be used in the present case since the waveforms of interest are large signal.
2. The transient simulation must be started from a guess of the steady-state solution and then simulated for many cycles of the carrier frequency to allow a true steady-state condition to evolve. Once the steady-state condition is found, then the simulation must run for a minimum of one complete modulation cycle. The program will step in time, calculating the voltages and currents in the circuit using a step size small enough to resolve any

changes in the state of the circuit. This means that many time points per carrier cycle must be calculated. (The amount of change in the voltages and currents in a circuit that may occur between time steps is set by a series of user-selected tolerance parameters. Typically the default values force SPICE to have less than 1% change in value from one time step to the next. For a waveform like the input voltage to the rectifier, which is ideally a square wave, the program may calculate hundreds of steps during the edge transition. This will lead to an accurate solution that has many thousands of time steps per modulation cycle.)

3. Once one cycle of the modulation is obtained where the starting state is the same (approximately) as the ending state, then a fast Fourier transform (FFT) is used to evaluate the spectrum of the signal. The result will contain magnitudes and phases at each of the harmonics of the signal of interest. The various transfer functions of interest may be calculated as ratios of the signals at the frequencies of interest. The DFT must use enough points to resolve the signals, requiring that samples be taken at least twice the carrier frequency. In practice, the signals must be sampled at 5-10 times the carrier frequency because of the non-sinusoidal nature of the carrier signals. The Mathcad™ result above indicated a sampling frequency at least 6 times the carrier frequency for reasonable accuracy.

Because of the computation time required to carry out all these steps, the simulation will be done at two modulation frequencies: one low (the most difficult) and one high compared to the corner frequency of the output filter. The circuit entered into SPICE is shown in Fig. 7.7. This circuit will result in non-sinusoidal waveforms for most signals except the input current sources and their sum i_c. The diodes are ideal SPICE diodes; that is, they have no charge storage or resistance but do exhibit an exponential forward-drop

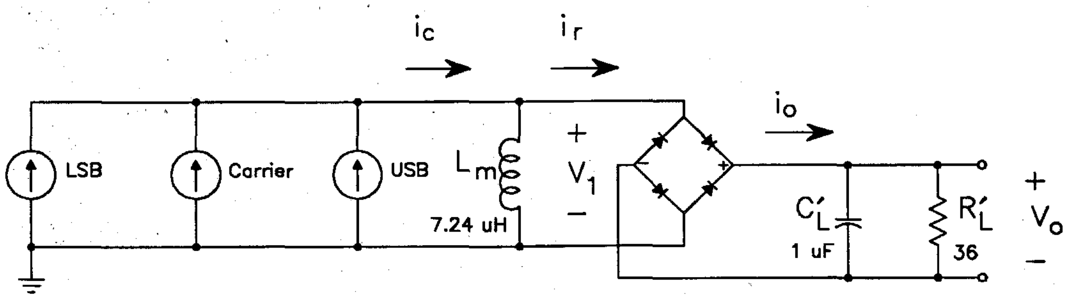


Figure 7.7: Circuit Entered into SPICE for Simulation. This circuit is used to verify the new rectifier model. The diodes in the bridge are ideal (exponential forward characteristic, no charge storage) and the input current sources are all ideal sine waves.

characteristic. The component values are chosen to be realistic values as are the input currents. The input currents are specified using three separate current sources so any arbitrary amplitude or phase modulation could be used. This model will accurately represent the performance of a real rectifier circuit under the assumptions stated above.

As important as what is modeled by a simulation of Fig. 7.7 is what is *not* modeled. This simulation will not model any effects caused by non-sinusoidal input currents which are present in the experimental circuit (see Chapter 4). Any effects caused by real diode behavior such as junction capacitance, bulk resistance or reverse recovery time will also not be accounted for in this SPICE simulation, although these effects can be modeled by SPICE. Any parasitic elements which do not explicitly appear in Fig. 7.7, such as lead inductance, are also neglected. The results of the SPICE simulation versus the model calculation are shown in Table 7.5. The table shows that the forward transfer characteristic is very accurate as is the AM portion of the reverse transfer. The PM portion of the reverse transfer is not nearly so accurate. In the example shown in the table, the signals from the phase modulation are off by as much as 4.1 dB. This is probably due to the difference between the phase of the fundamental of the input current and the zero-crossings of the input current (which determine the switching of the input voltage to the rectifier).

Table 7.5: SPICE Simulation results for the Rectifier Model versus Calculated Results

	Mod. freq. = 1 kHz		Mod. freq. = 100 kHz	
Model Element	Calculation (value x 0.001)	Simulation (value x 0.001)	Calculation (value x 0.001)	Simulation (value x 0.001)
$G(v)$ AM (m)	$93.3\angle -7.3^\circ$	$93.3\angle -7.4^\circ$	$3.52\angle -114^\circ$	$3.52\angle -109^\circ$
$G(v)$ PM (K_p)	$7.88\angle -239^\circ$	$13.1\angle -251^\circ$	$57.6\angle 142^\circ$	$71.0\angle 144^\circ$
$f(i_r)$ (mA)	$55.7\angle 5.1^\circ$	$55.7\angle 5.5^\circ$	$45.3\angle -26.6^\circ$	$46.5\angle -26.7^\circ$

7.2 The DC-to-DC Converter First Order Model

The results of the previous section demonstrate that the model for the rectifier block is reasonably accurate under the assumptions used in the derivation of the model. However, the actual circuit is under no such restrictions and may significantly violate some of the assumptions depending upon the actual design of the DC-to-DC converter. The assumption most likely to be violated is that the tank current is sinusoidal. The class E circuit by its nature produces a tank current that is composed of segments of sine waves of different frequencies joined together. The fact that the tank circuit is narrowband and that the output is relatively insensitive to the actual waveform details should justify the sinusoidal approximation. The only way to truly verify the model is to compare the predicted results to the measured performance of the hardware. The SPICE predictions done above are useful tools but cannot be considered proof of the model's validity. The same circuit that was examined in Chapter 6 will be re-examined in this chapter using the new rectifier model. The first function to examine will once again be the control-to-output transfer function.

7.2.1 The Control-to-Output Transfer Function

In Section 6.1, the control-to-output transfer function was considered using a model for the rectifier which was simplified compared to the present model. This same experimental circuit will be used once again, this time with the refined rectifier model. In this new model the inverter will still be treated as a hard voltage source. The schematic diagram for the experimental circuit is shown in Fig. 6.15 and the measurement setup is shown in Fig. 6.16. The new model for the calculation of the control-to-output transfer function is shown in Fig. 7.8. Once again the ideal transformer that is part of the magnetic regulator model will be translated to the output for simplicity. The small-signal model corresponding to Fig. 7.8 is shown in Fig. 7.9. The inverter voltage source V_{sw} has disappeared from this diagram since it is a stiff, unmodulated source. The control sources V_R and f are now shown with squares to emphasize their dependence upon other signals.

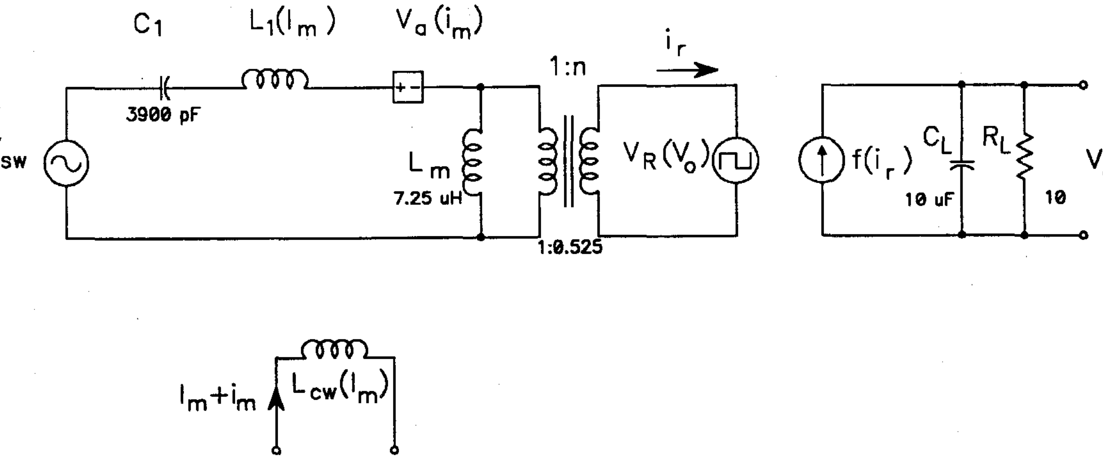


Figure 7.8: Equivalent Circuit for the DC-to-DC Converter Using the Bilateral Rectifier Model. In this circuit the controlling current for $f(i_R)$ has been moved past the magnetizing inductance L_m. Previously, V_R was a hard, independent voltage source and so L_m could be eliminated. In this case L_m will remain in the model.

Predicted Results

The equivalent circuit in Fig. 7.9 effectively represents two different circuits, one at the upper sideband frequency and one at the lower sideband frequency. The nonlinear nature of the circuit mixes the results of these two calculations so the circuits must be solved simultaneously. The subscript c refers to signals at the carrier frequency, the subscript u refers to signals at the upper sideband frequency, and L refers to signals at the lower sideband frequency. The tank current i_t is composed of i_{USB} and i_{LSB} at the upper and lower sidebands, respectively, in addition to the steady-state current I_C. The voltage source $G(v)$ is composed of G_{USB} and G_{LSB}. The equations that govern the circuit behavior are

$$i_{LSB} = \frac{-(v_{a_L} + G_{LSB})}{z_x(s_L)} \tag{7.55}$$

$$i_{USB} = \frac{-(v_{a_u} + G_{USB})}{z_x(s_u)} \tag{7.56}$$

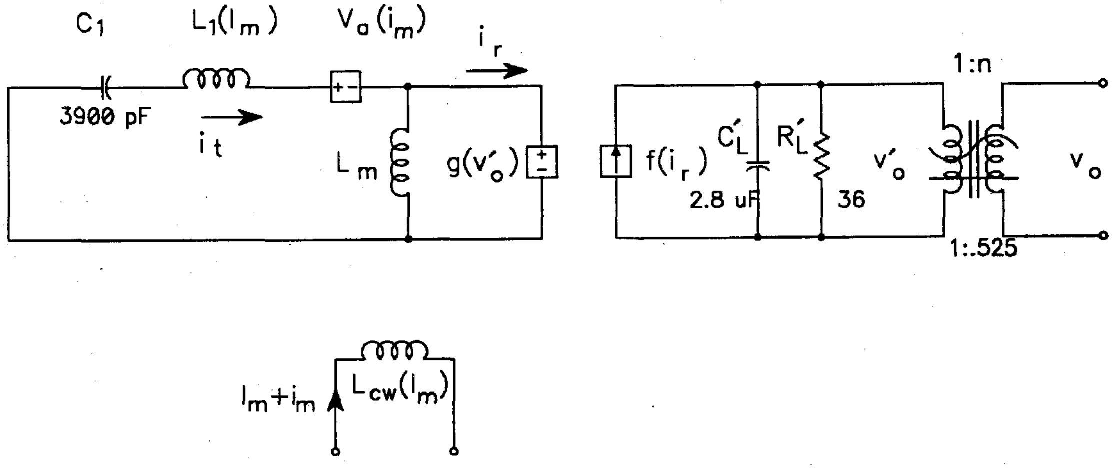


Figure 7.9: Small-Signal Equivalent Circuit for the DC-to-DC Converter. This circuit is suitable for calculating the modulation signals in the converter. The inverter is considered a stiff source and so appears as a short in this circuit.

$$G_{USB}(v) = \frac{2}{\pi}\left\{\frac{v_o}{n} + G_0\left[\overline{\left(\frac{i_{r_L}}{i_{r_c}}\right)} - \frac{i_{r_u}}{i_{r_c}}\right]e^{j\pi}\right\}e^{j\varphi_d} \tag{7.57}$$

$$G_{LSB}(v) = \frac{2}{\pi}\left\{\frac{\bar{v}_o}{n} + G_0\left[\frac{i_{r_L}}{i_{r_c}} - \overline{\left(\frac{i_{r_u}}{i_{r_c}}\right)}\right]\right\}e^{j\varphi_d} \tag{7.58}$$

$$i_{r_L} = i_{LSB} - \frac{G_{LSB}}{s_L L_m} \tag{7.59}$$

$$i_{r_u} = i_{USB} - \frac{G_{USB}}{s_u L_m} \tag{7.60}$$

$$v_o = i_{d,av}\left[\frac{i_{r_u}}{i_{r_c}} + \overline{\left(\frac{i_{r_L}}{i_{r_c}}\right)}\right]z'_L(s_m)\,n \tag{7.61}$$

Equations 7.55 to 7.61 must be solved for the voltages and currents to calculate the desired transfer functions. These equations can be simplified to equations containing $i_{USB}, i_{LSB}, i_{r_u}, i_{r_L}, G_{USB}, G_{LSB}$ and their complex conjugates. This results in a set of 12 equations in 12 unknowns. The equations can be written as one matrix equation for each value of the modulation frequency, then solved numerically to generate a bode plot. Commercially available software makes this approach quite simple. The individual matrix elements are entered as functions of s_m, then the matrix is inverted (symbolically). The result is plotted by using a set of values of s_m that are equally spaced on a log scale over the modulation frequencies of interest. The symbolic inverse is extremely complex precluding it from being written out.

The first step in the solution to the matrix equation is to define the matrix elements. These elements are based upon equations derived from 7.55 to 7.61:

$$z_x(s_L)\,i_{LSB}+G_{LSB} = -R_{1_L}s_L \tag{7.62}$$

$$z_x(s_u)\,i_{USB}+G_{USB} = -R_{1_u}s_u \tag{7.63}$$

$$\frac{i_{d,av}z'_L+G_0}{i_{r_c}}i_{r_u}-\frac{\pi}{2}e^{-j\varphi_d}G_{USB}+\frac{i_{d,av}z'_L-G_0}{\overline{i}_{r_c}}\overline{i}_{r_L} = 0 \tag{7.64}$$

$$\frac{i_{d,av}\bar{z}'_L+G_0}{i_{r_c}}i_{r_L}-\frac{\pi}{2}e^{-j\varphi_d}G_{LSB}+\frac{i_{d,av}\bar{z}'_L-G_0}{\overline{i}_{r_c}}\overline{i}_{r_u} = 0 \tag{7.65}$$

$$i_{LSB}-i_{r_L}-\frac{1}{s_mL_m}G_{LSB} = 0 \tag{7.66}$$

$$i_{USB}-i_{r_u}-\frac{1}{s_mL_m}G_{USB} = 0 \tag{7.67}$$

where

$$R_{1_L} = \frac{v_{a_L}}{s_L} = \frac{k_L}{2}I_c\overline{i}_m$$

$$R_{1_u} = \frac{v_{a_u}}{s_u} = \frac{k_L}{2}I_ci_m$$

Equations 7.62 through 7.67 define half the equations required to solve for the unknowns. Each variable and its complex conjugate constitute an unknown quantity (although the complex conjugate quantity is trivial to determine given the normal quantity, it is easier to solve the system by treating the conjugate as an independent variable) so there are a total of 12 unknowns. The additional 6 equations are determined by taking the conjugates of 7.62 through 7.67. The matrix form of the system of equations can be written as

$$A_1 = \begin{bmatrix} 0 & z_x(s_L) & 0 & 0 & 0 & 1 \\ z_x(s_u) & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & P_5(s_m) + P_6 & 0 & -\frac{\pi}{2}e^{-j\varphi_d} & 0 \\ 0 & 0 & 0 & \overline{P_{55}(s_m)} + P_6 & 0 & -\frac{\pi}{2}e^{-j\varphi_d} \\ 0 & 1 & 0 & -1 & 0 & -\frac{1}{s_L L_m} \\ 1 & 0 & -1 & 0 & -\frac{1}{s_u Lm} & 0 \end{bmatrix} \tag{7.68}$$

$$A_2 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & P_{55}(s_m) - P_{66} & 0 & 0 \\ 0 & 0 & \overline{P_5(s_m)} - P_{66} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{7.69}$$

where

$$P_5(s_m) = \frac{i_{\mathrm{d,av}} z'_L(s_m)}{i_{r_c}}$$

$$P_{55}(s_m) = \frac{i_{\mathrm{d,av}} z'_L(s_m)}{\overline{i}_{r_c}}$$

$$P_6 = \frac{G_0}{i_{r_c}}$$

$$P_{66} = \frac{G_0}{\overline{i}_{r_c}}$$

$$G_0 = \frac{V_{DC} + 2V_d}{n}$$

The final form of the matrix equation is

$$Ax = b \tag{7.70}$$

$$A = \begin{bmatrix} A_1 & A_2 \\ \overline{A_2} & \overline{A_1} \end{bmatrix} \tag{7.71}$$

$$x_1^T = \begin{bmatrix} i_{USB} & i_{LSB} & i_{r_u} & i_{r_L} & G_{USB} & G_{LSB} \end{bmatrix} \tag{7.72}$$

$$x^T = \begin{bmatrix} x_1^T & \overline{x_1^T} \end{bmatrix} \tag{7.73}$$

$$b_1^T = \begin{bmatrix} -R_{1_L} & -R_{1_u} & 0 & 0 & 0 & 0 \end{bmatrix} \tag{7.74}$$

$$b^T = \begin{bmatrix} b_1^T & \overline{b_1^T} \end{bmatrix} \tag{7.75}$$

The input i_m does not appear explicitly in these equations but is buried in the b vector. The most convenient way to solve this system is to assign i_m a value of 1 and then solve for the unknown quantities by using the matrix inverse

$$x = A^{-1} b \tag{7.76}$$

Since the input i_m is set to 1, the elements in the x vector contain the transfer functions from the input to the various unknown quantities. The control-to-output transfer function, H_c, is

$$H_c \equiv \frac{v_o}{i_m} = v_0 \Big|_{i_m = 1} = i_{d,av} \left[\frac{x_3}{i_{r_c}} + \overline{\left(\frac{x_4}{i_{r_c}} \right)} \right] z'_L n \tag{7.77}$$

Measured Results

The measured results that were presented in Chapter 6 for the control-to-output transfer function can now be compared to the predictions of this new model. The results are shown in Fig. 7.10. This measurement is the same measurement done in Chapter 6 on the TWT filament power supply. The input DC voltage is 20 V, the output DC voltage is 10 V, and the load is 10 Ω.

Interpretation

The new result illustrated in Fig. 7.10 comes much closer to correctly predicting the performance of the actual circuit (compare this result with fig 6.17). The previous measurement had a low-frequency gain which was much too high and a dominant pole which was too low in frequency. The new measurement has nearly the correct low-frequency gain but a dominant pole frequency that is too high. This is a preview that the new model has an output impedance that is lower than the actual circuit. As in the previous result, the high-frequency dynamics of the predicted curve cannot be verified due to noise in the

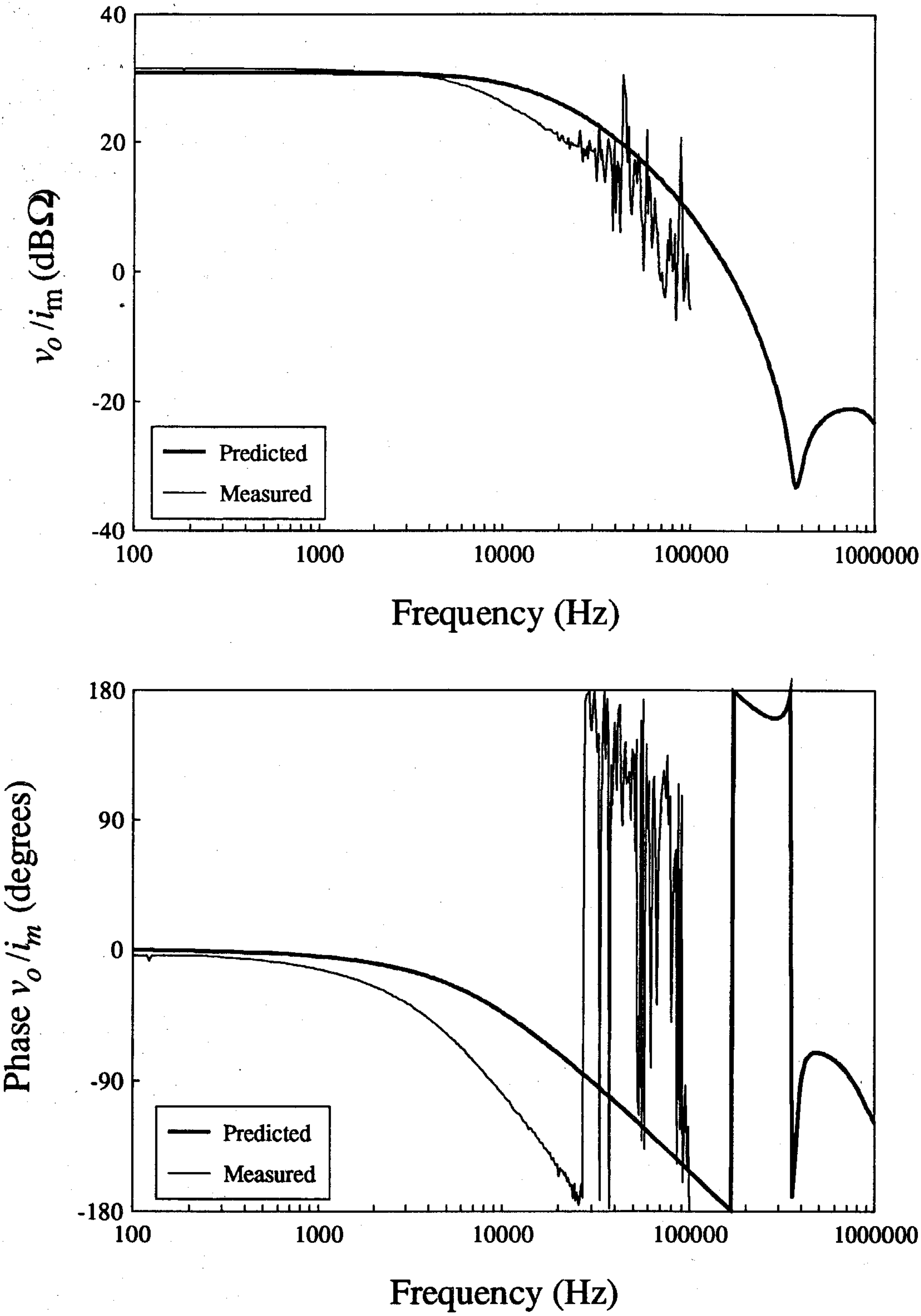


Figure 7.10: Measured Versus Predicted Results for the DC-to-DC Converter Using the Bilateral Rectifer Model. The measurement is the same measurement made in Chapter 6 on the TWT filament power supply.

measurement at high frequencies. To attempt to reveal the high-frequency character of the model, the output impedance measurement will be examined next.

7.2.2 The Output Impedance

The output impedance function is treated here much the same as in Chapter 6; the internal input impedance Z'_o which is the input impedance looking into the rectifier bridge is the most interesting function since it is not swamped by the low impedance of the output capacitor. The equivalent circuit for this measurement is shown in Fig. 7.11. The internal output impedance in this model must be calculated on the primary side of the ideal transformer at the output. The measurements are made at the secondary side of this transformer so the calculation must be scaled by n^2 at the end of the computation.

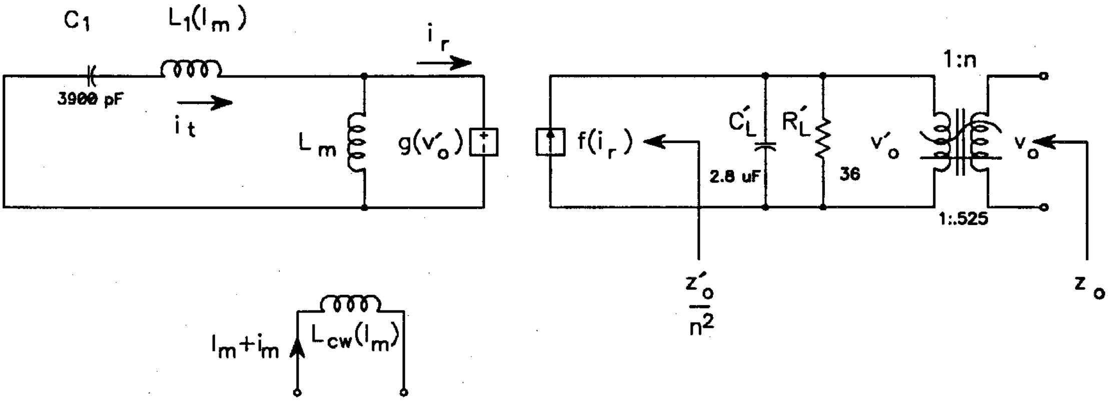


Figure 7.11: Equivalent Circuit for the Calculation of Z'_o. Z'_o is the impedance looking into the output of the bridge rectifier and therefore excludes the load impedance and the output filter capacitor. The calculation is referred to the output side of the ideal transformer to facilitate comparison with measurements.

Predicted Results

The same matrix equation that was used for the control-to-output response can be used to solve for the output impedance with some minor changes. The equations that must change are 7.61, 7.64 and 7.65. In addition, the modulation current into the magnetic regulator, I_m, should be set to zero which sets v_a to zero. The new equation for 7.61 is

$$v_o = nv_t \tag{7.78}$$

where v_t is a voltage source used to inject a test signal at the port where Z'_o/n^2 is to be measured. In the computations this source is set to 1 volt which provides convenient scaling of the results. The replacement equation for 7.64 is

$$\left(\frac{G_0}{i_{r_c}}\right) i_{r_u} - \frac{\pi}{2} e^{-j\varphi_d} G_{USB} + \left(\frac{-G_0}{\overline{i_{r_c}}}\right) \overline{i_{r_L}} = -v_t \tag{7.79}$$

and the replacement for 7.65 is

$$\left(\frac{G_0}{i_{r_c}}\right) i_{r_L} - \frac{\pi}{2} e^{-j\varphi_d} G_{LSB} + \left(\frac{-G_0}{\overline{i_{r_c}}}\right) \overline{i_{r_u}} = -v_t \tag{7.80}$$

These changes result in a new A matrix and b vector:

$$A_1 = \begin{bmatrix} 0 & z_x(s_L) & 0 & 0 & 0 & 1 \\ z_x(s_u) & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & P_6 & 0 & -\frac{\pi}{2} e^{-j\varphi_d} & 0 \\ 0 & 0 & 0 & P_6 & 0 & -\frac{\pi}{2} e^{-j\varphi_d} \\ 0 & 1 & 0 & -1 & 0 & -\frac{1}{s_L L_m} \\ 1 & 0 & -1 & 0 & -\frac{1}{s_u Lm} & 0 \end{bmatrix} \tag{7.81}$$

$$A_2 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -P_{66} & 0 & 0 \\ 0 & 0 & -P_{66} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{7.82}$$

$$A = \begin{bmatrix} A_1 & A_2 \\ \overline{A_2} & \overline{A_1} \end{bmatrix} \tag{7.83}$$

$$b_1^T = \begin{bmatrix} 0 & 0 & -v_t & -v_t & 0 & 0 \end{bmatrix} \tag{7.84}$$

$$b^T = \begin{bmatrix} b_1^T & \overline{b_1^T} \end{bmatrix} \tag{7.85}$$

The output current can be found from the solution to the matrix equation as

$$i_o = i_{\text{d,av}} \left[\frac{i_{r_u}}{i_{r_c}} + \overline{\left(\frac{i_{r_L}}{i_{r_c}} \right)} \right] = i_{\text{d,av}} \left[\frac{x_3}{i_{r_c}} + \overline{\left(\frac{x_4}{i_{r_c}} \right)} \right] \tag{7.86}$$

and from this the output impedance follows as

$$z'_o \equiv \frac{v_t}{i_o} n^2 = \frac{1}{i_0 \big|_{v_t = 1}} n^2 = \frac{1}{i_{\text{d,av}} \left[\frac{x_3}{i_{r_c}} + \overline{\left(\frac{x_4}{i_{r_c}} \right)} \right]} n^2 \tag{7.87}$$

Measured Results

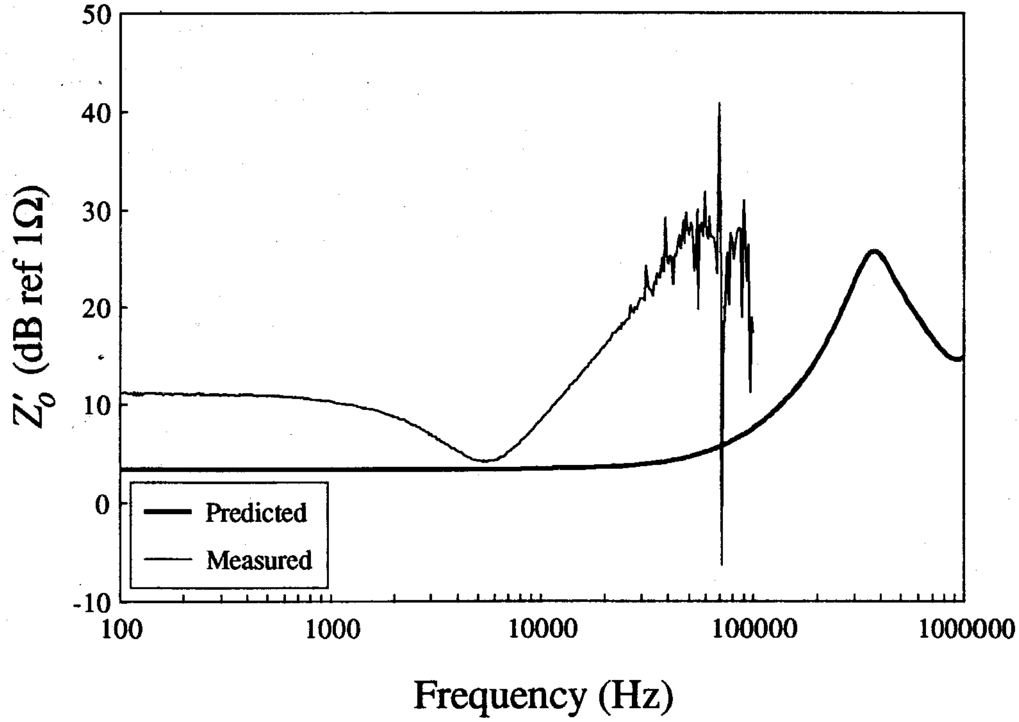
The same measured results as presented in Chapter 6 are shown together with the predicted result from 7.87 in Fig. 7.12. As expected, the low-frequency impedance is much lower than in the actual circuit. The higher frequency dynamics occur at a higher frequency in the model than in the measurement.

Interpretation

The bilateral rectifier model is a significant improvement over the previous model in that it predicts a finite output impedance rather than an infinite impedance in the zero-order model. Nevertheless, the actual value of the output impedance predicted is considerably different from the measured data. The fact that the model is now bilateral means that the dynamics associated with the tank circuit and the inverter play a role in determining the output impedance and the control-to-output transfer function. In the model used in this chapter, the inverter was represented as a stiff voltage source when in reality there is some non-zero output impedance. This suggests that an accurate picture of the performance of the DC-to-DC converter requires that the inverter be taken into account more accurately. The next step would be to develop a model for the inverter which is the subject of the next chapter.

7.2.3 The Input-to-Output Response

A transfer function of interest to any power system designer is the input-to-output response. In fact, the whole purpose of many power processing systems is to provide regulation of an unstable voltage to a sensitive load. The input-to-output response determines the natural ability of a power system to reject changes in the input voltage. Usually this rejection function will be augmented by negative feedback to produce an accurate regulator.



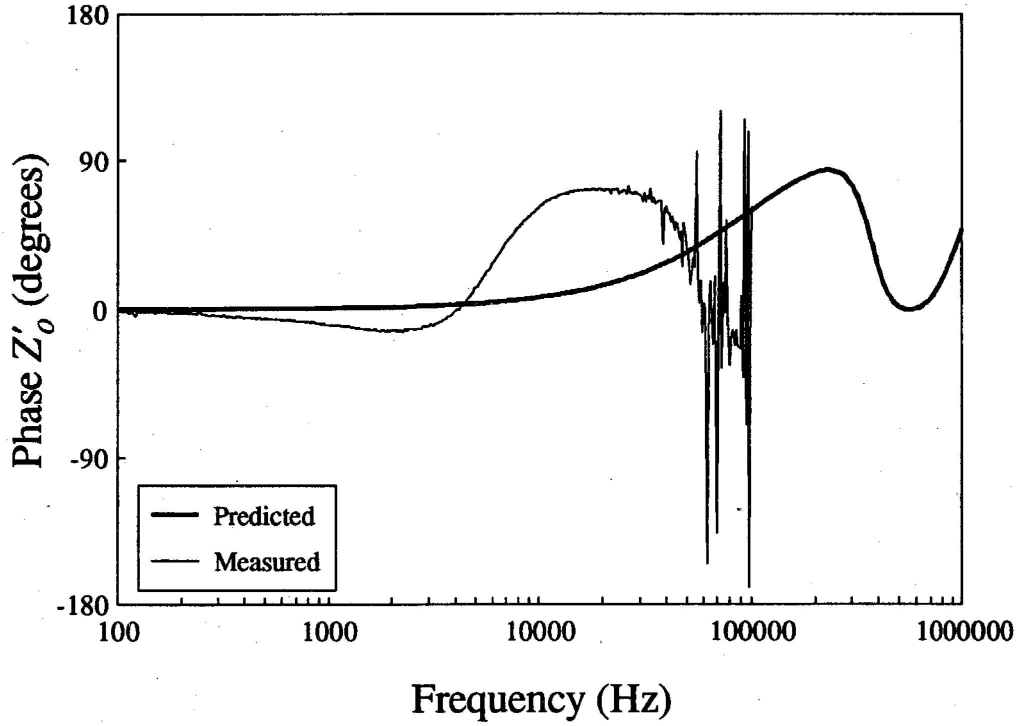


Figure 7.12: Predicted Versus Measured Output Impedance for the DC-to-DC Converter Using the Bilateral Rectifer Model. The measurement is the same measurement made in Chapter 6 on the TWT filament power supply.

Predicted Results

The present model assumes that the inverter is an ideal voltage source with the only information about the input-to-output transfer function supplied at zero frequency. This deficiency of the present model is further motivation for a dynamic inverter model as will be developed in Chapter 8.

Chapter 8

The Second Order Model

Introduction

The final result of the previous chapter was a model in which the rectifier and magnetic regulator portions of the DC-to-DC converter were modeled accurately but the inverter was treated as a simple voltage source. This model predicts an unrealistically low source output impedance and also has no provision for the calculation of either the input impedance or the input-output response. It is reasonable to expect that an ideal voltage source inverter would produce a power system with a low output impedance. The actual circuit, however, certainly does have some source impedance. These considerations motivate the next extension of the model: the dynamic model for the inverter. This model itself is developed in several stages beginning with the simplest model and ending with a rather complicated model that accounts for all the major effects. This model is tested against SPICE simulations at first since SPICE allows one to work on a circuit without undesirable parasitic elements. The model is developed to the point that the agreement between the model and the SPICE simulation is acceptable, then the dynamic inverter model is inserted into the DC-to-DC converter model and the results compared against measured data.

This chapter illustrates how circuit simulation can be used as an effective analytical tool. The usual method of model development is an iterative process where a proposed model is calculated then compared against measured data. If the predictions are not satisfactory, the model is refined and the process repeated. Circuit simulation can add an additional dimension to this process. The calculate-measure-iterate process can often times be a rather slow process because of parasitic effects in the real circuit that cloud the measured results. Particularly in modern systems with extreme miniaturization, the parasitic effects encountered in a breadboard circuit may not be relevant to a production design. In this case, the time spent understanding and accounting for the parasitic effects may be wasted. By using circuit simulation, the process of model development can be accelerated by simulating only the effects desired. For instance, the effect of leakage inductance can never be completely eliminated from a real circuit, but a SPICE simulation has no problem with a perfect transformer. While it may be necessary in the final model to account for the parasitics, a model that does not predict the performance of a simulation of an idealized circuit has no hope of working on a real circuit with parasitics. In addition, the simulation allows the addition of parasitic elements one at a time so the most significant ones can be identified. Of course the danger in using simulation alone is that it may not predict significant features of the actual circuit due to inadequate models or inaccurate model parameters. The measurement of an actual circuit should always be the final indication of a model's validity.

The new process now becomes (calculate-simulate-iterate)-measure-iterate. The inner loop in this process can be much faster than the overall loop so many simulations may be done before performing a measurement. In the model developed in this chapter, this approach is used to find an inverter model that at least predicts the performance of an idealized circuit, before the model is incorporated into the overall DC-to-DC converter. In fact, another loop is useful where a simple numerical calculator (Mathcad™) verifies the model even before SPICE is invoked.

8.1 The Inverter Dynamic Model

The inverter topology used in this section is the normal class E circuit [23] which is a current-fed topology. The circuit under consideration is shown in Fig. 8.1. The basic operation of this circuit was described in Chapter 2. The dynamic model for the inverter requires the voltage source V_{sw} under the condition that either the tank current is modulated or the input current is modulated. A simplified equivalent circuit to Fig.8.1 is shown in Fig. 8.2. The input inductor is replaced by a DC current source and the tank circuit is replaced by a sine wave current source. The goal in this circuit is for the voltage V_{sw} to be zero at the instant that the switch closes. This can only be achieved for certain values of

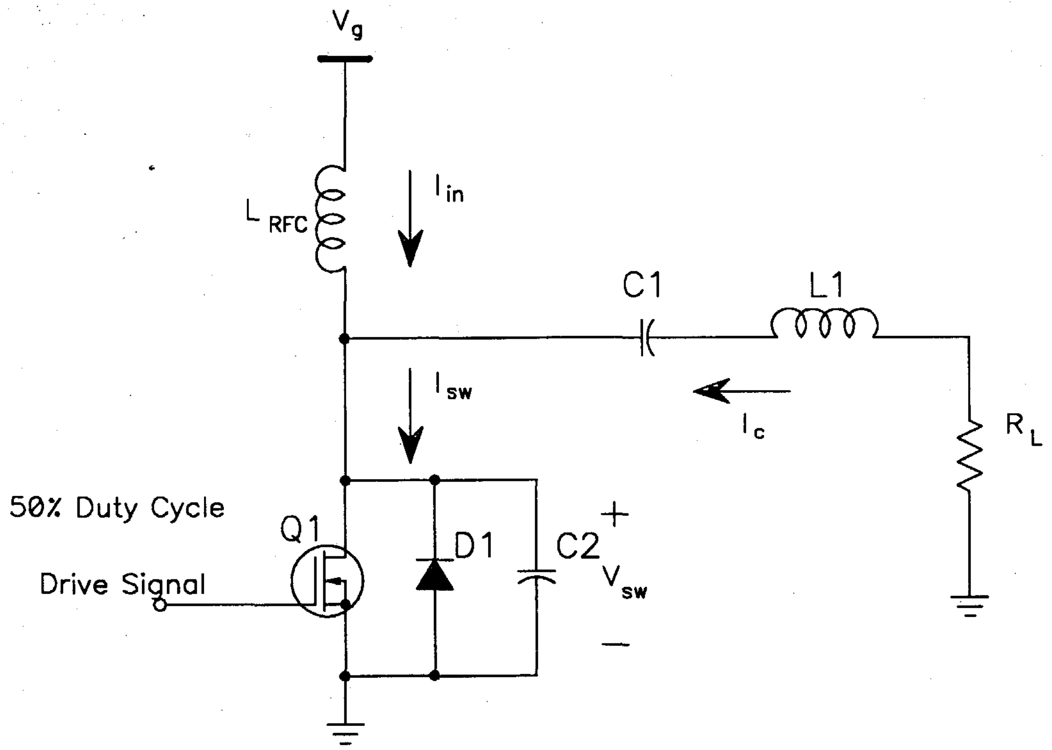


Figure 8.1: The Class E Inverter. This inverter topology is current fed through inductor L_{RFC}. The tank current I_c is assumed to be a sine wave. The task in this model is to calculate the voltage V_{sw} in the case that I_{in} and/or I_c is modulated.

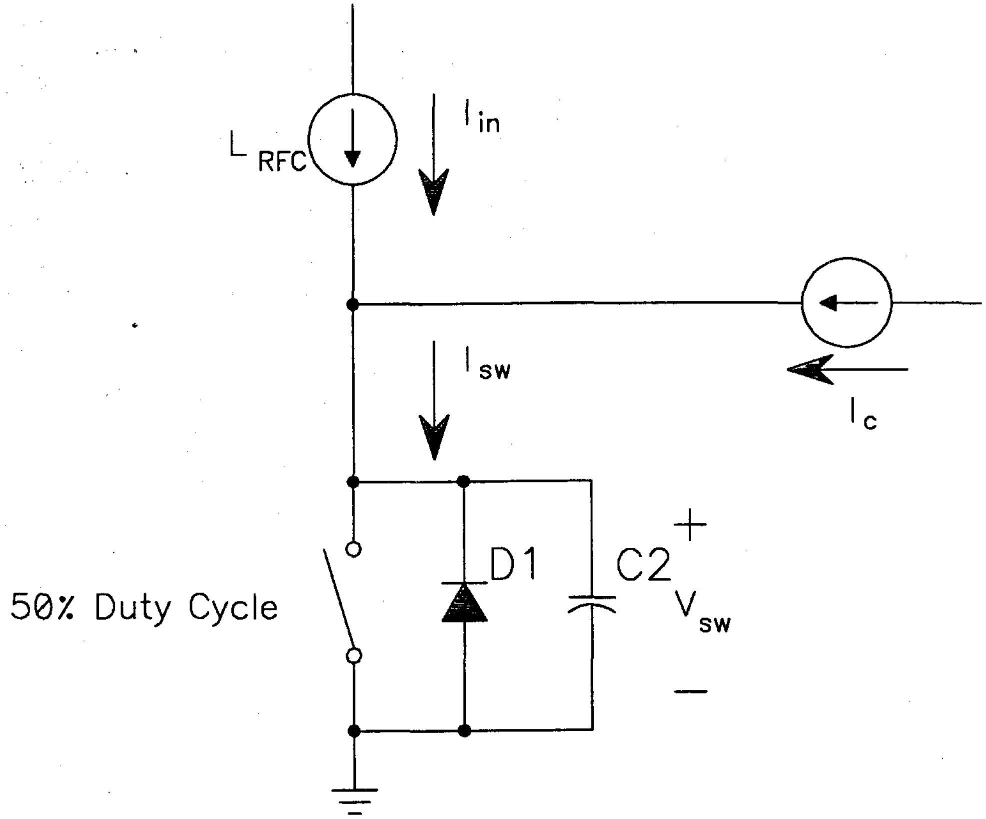


Figure 8.2: Simplified Equivalent Circuit for the Analysis of the Class E Inverter. The input current is assumed to be DC with a small AC perturbation and the tank current I_C is assumed to be a sine wave with small, low-frequency modulation.

the input and tank currents. These steady-state currents were determined in Chapter 2 for this topology. The dynamic problem assumes the proper steady-state currents are flowing and then perturbs them slightly about their operation points. Figure 8.3 shows representative waveforms for this circuit.

8.1.1 Input Current Modulation

The first inverter perturbation to be considered is the input current. In actual practice, the input current will modulate either directly through modulation applied at the input, or

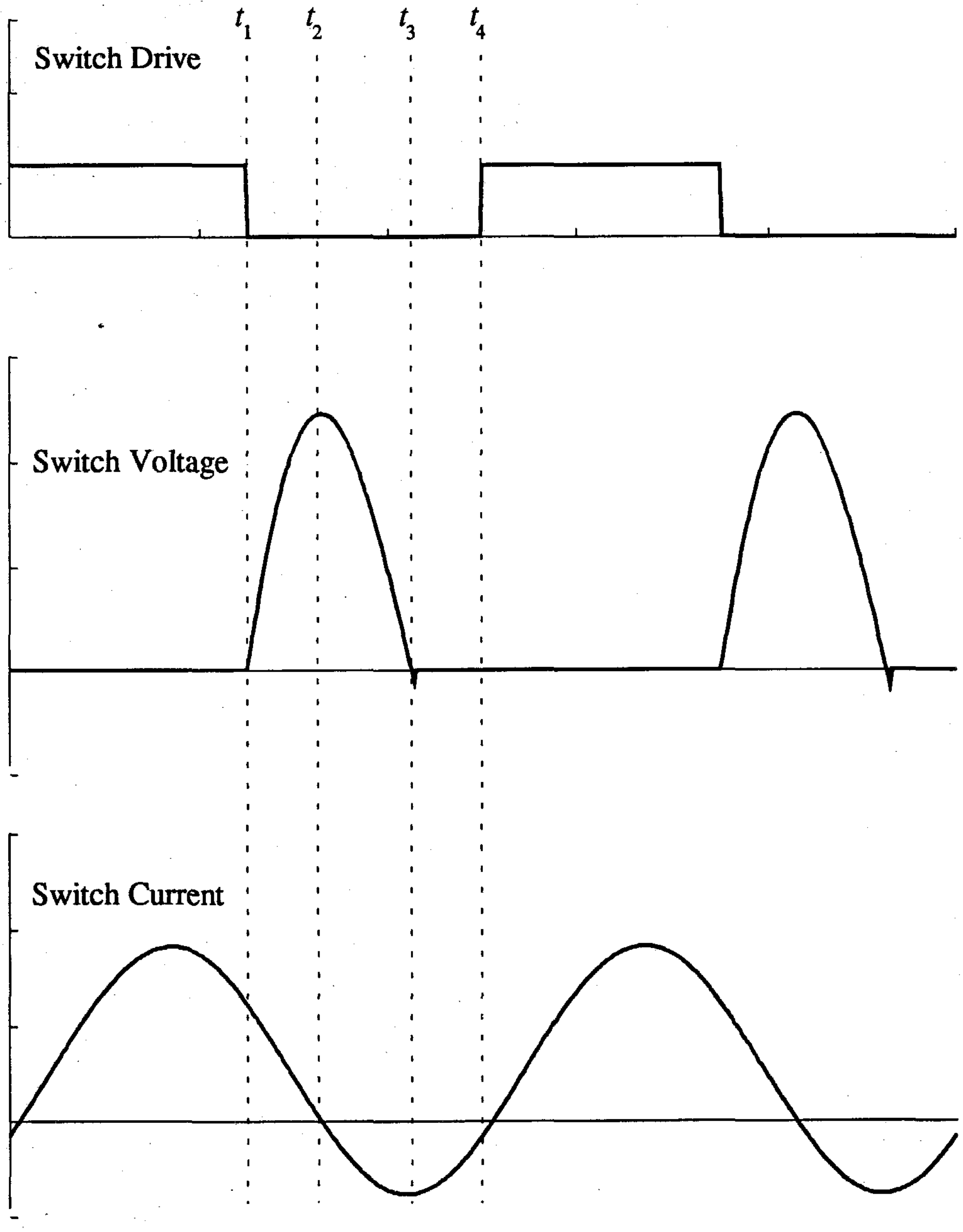


Figure 8.3: Representative Waveforms in the Class E Inverter. The power switch is turned off at t_1 which allows the switch voltage V_{sw} to rise. The switch voltage will be a maximum when the switch current goes through zero at t_2. At time t_3, the switch voltage returns to zero turning on the antiparallel diode across the switch. The switch is closed again at t_4 when the switch current is either negative or zero.

indirectly as a result of changes in the load or magnetic regulator characteristics. It is convenient for the calculations to take $t = 0$ to be at t_1. The switch voltage is:

$$V_{sw}(t) = \begin{cases} \dfrac{1}{C_2} \displaystyle\int_{nT_s}^{nT_s + t} (I_{in}(\tau) + I_c(\tau))\, d\tau & nT_s < t < DnT_s \\ 0 & DnT_s < t < (n+1)T_s \end{cases} \tag{8.1}$$

where n is an integer which counts cycles of the carrier frequency. The duty cycle D is the duty cycle of the switch voltage, *not* the input drive. This value is determined from the steady-state solution of the inverter. T_s is the switching period or, also, the period of the carrier frequency. The switch voltage has the following form:

$$V_{sw}(t) = A(t) + B(t) \tag{8.2}$$

where

$$A(t) = \begin{cases} \dfrac{1}{C_2} \displaystyle\int_{nT_s}^{(nT_s + t)} I_{in}(\tau)\, d\tau & nT_s < t < DnT_s \\ 0 & DnT_s < t < (n+1)T_s \end{cases} \tag{8.3}$$

and

$$B(t) = \begin{cases} \dfrac{1}{C_2} \displaystyle\int_{nT_s}^{(nT_s + t)} I_c(\tau)\, d\tau & nT_s < t < DnT_s \\ 0 & DnT_s < t < (n+1)T_s \end{cases} \tag{8.4}$$

If the input current is assumed to be modulated with a small, low-frequency modulation such as $I'_{in}(t) = (1 + m\cos\omega_m t)\, I_{in}$, the switch voltage becomes

$$V'_{sw}(t) = \begin{cases} \dfrac{1}{C_2} \displaystyle\int_{nT_s}^{nT_s+t} \left(I_{in}(1+m\cos\omega_m\tau) + I_c(\tau)\right) d\tau & nT_s < t < DnT_s \\ 0 & DnT_s < t < (n+1)T_s \end{cases} \tag{8.5}$$

The modulation term in this equation changes very little over the time interval of the integral, so it can be treated as approximately constant and therefore removed from the integrand:

$$V'_{sw}(t) = \begin{cases} (1+m\cos\omega_m t)\left(\dfrac{1}{C_2}\displaystyle\int_{nT_s}^{nT_s+t} I_{in}\,d\tau\right) + \dfrac{1}{C_2}\displaystyle\int_{nT_s}^{nT_s+t} I_c\,d\tau & nT_s < t < DnT_s \\ 0 & DnT_s < t < (n+1)T_s \end{cases} \tag{8.6}$$

$$V'_{sw}(t) = (1+m\cos\omega_m t)\, A(t) + B(t) \tag{8.7}$$

The spectrum of 8.7 can easily be determined from section 7.1.3. The spectrum is composed of the sum of the spectrum of the modulated $A(t)$ and of $B(t)$. The component of $A(t)$ at the modulation frequency is m times the DC average value of $A(t)$. There will be sidebands around all the harmonics of $A(t)$, but only those around the fundamental are of interest. These will have a magnitude of $m/2$ times the fundamental component, A_1, of $A(t)$. The total signal at the fundamental of V_{sw} will be the sum of A_1 and B_1. It is important to note that the signals at the upper and lower sideband are m times the fundamental of A_1, *not* the fundamental of V_{sw} (as it would be if the entire V_{sw} signal were modulated). Figure 8.4 shows the spectrum of V_{sw} as the sum of its component signals.

A representative waveform for $A(t)$ is shown in Fig. 8.5 together with the switch voltage for comparison. The DC average value of V_{sw} will be termed A_0 and is

$$A_0 = \frac{I_{in} D}{2C_1} \tag{8.8}$$

The fundamental of V_{sw} is termed A_1 and is computed as follows:

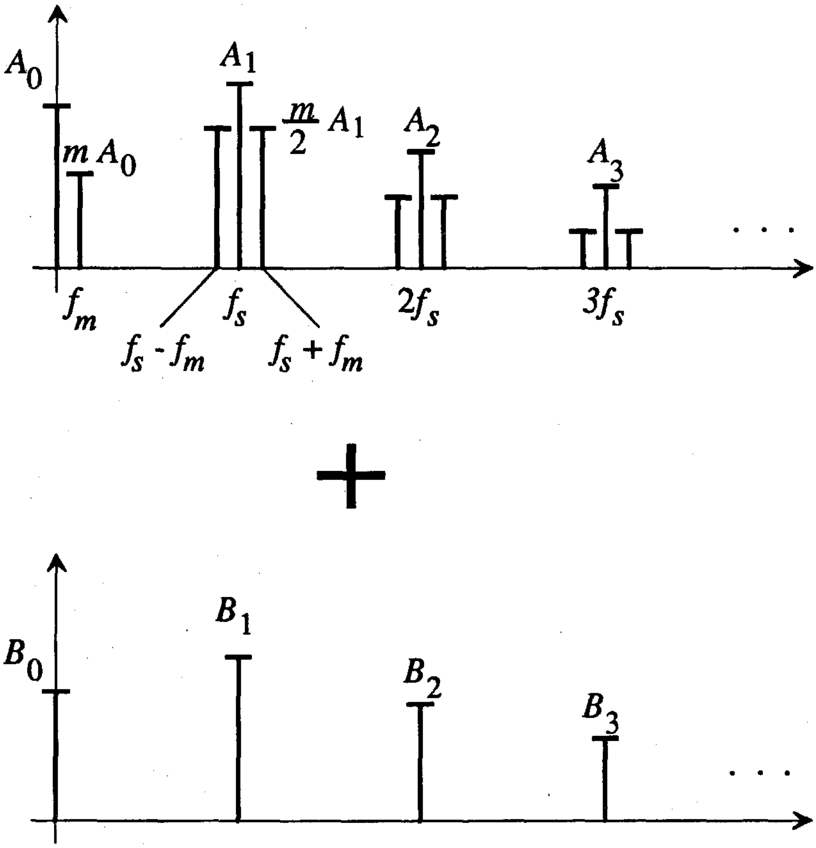


Figure 8.4: Spectrum of the Inverter Switch Voltage with Input Current Modulation. The spectrum is composed of the sum of two signals, $A(t)$ and $B(t)$, the former of which is AM modulated while the latter is not.

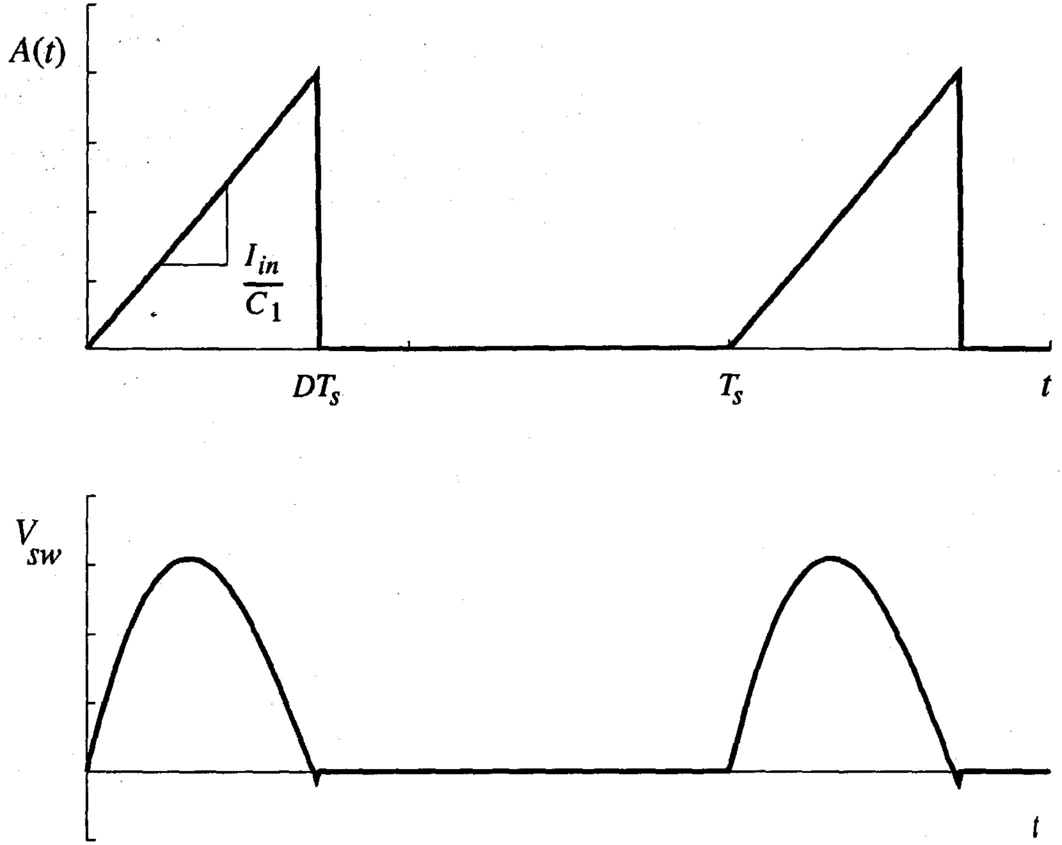


Figure 8.5: Inverter Waveforms. The $A(t)$ function from equation 8.7 is shown together with the inverter switch voltage V_{sw}. The function $A(t)$ is the portion of the switch voltage that is due to the input current. The fundamental of $A(t)$ determines the sidebands on V_{sw} when the input current is modulated. The DC average value of $A(t)$ determines the baseband component of V_{sw}.

$$
\begin{aligned}
A_1 &= \frac{2}{T_s}\int_0^{DT_s} A(\tau)\, e^{-j\frac{2\pi}{T_s}\tau}\, d\tau \\
&= \frac{T_s I_{in}}{2}\left(\frac{2j\pi D e^{-2j\pi D} + e^{-2j\pi D} - 1}{\pi^2 C_1}\right)
\end{aligned}
\tag{8.9}
$$

$$A_1 = \frac{I_{in}}{\pi \omega_c C_1} \left[(2j\pi D + 1) e^{-2j\pi D} - 1 \right] \tag{8.10}$$

The coefficient A_0 is a real constant and A_1 is a complex constant which will determine the modulation of the switch voltage due to the input current modulation.

8.1.2 Amplitude Modulation of the Tank Current

The other current that determines the switch voltage is the tank current. If this current is amplitude modulated, the voltage across the switch will also be modulated. This means that the modulation will come from the second term in 8.2. The same method as was used in section 8.1.1 can be used to find the modulation coefficients, this time termed B_0 and B_1 for the baseband and sideband coefficients respectively. While these coefficients can be calculated from the Fourier series for the function $B(t)$, the method demonstrated in the next paragraph is more accurate and efficient.

The assumption that the tank current is a sine wave at the switching frequency is a useful approximation, but in practice the actual waveform may be quite far from a sine wave as was observed in Chapter 2. SPICE can successfully simulate the true switch voltage and can also calculate the corresponding Fourier series. Since the Fourier series of V_{sw} is equal to the sum of the series for each of $A(t)$ and $B(t)$, the coefficients can alternatively be found from

$$B_0 = (\text{DC value of } V_{sw}) - A_0 \tag{8.11}$$

$$B_1 = (\text{Fundamental of } V_{sw}) - A_1 \tag{8.12}$$

The DC value of V_{sw} is simply equal to the input voltage to the inverter. By using 8.11 and 8.12, the distortion of the switch current can be accounted for in the inverter model.

The model for the inverter can be separated into two parts: 1) the signals that occur at the modulation or baseband frequency and 2) the signals that occur near the carrier frequency (the carrier itself and the upper and lower sidebands). Therefore, the equivalent circuit appears as a two-port with the baseband signals at the input and the carrier signals at the output. As far as the input current is concerned, the modulation index m is i_{in}/I_{DC}. The modulation index on the tank current is

$$m = \frac{i_{USB}}{i_{carrier}} + \overline{\left(\frac{i_{LSB}}{i_{carrier}}\right)} \tag{8.13}$$

The equivalent circuit is illustrated in Fig. 8.6.

Numerical Verification of the Inverter Model

A quick check on the above model can be done numerically. The idea is to write a mathematical equation which represents V_{sw} then use the FFT to compute the spectrum. (A suitably high sampling frequency must be used to avoid the effects of aliasing.) Aside from verifying that no simple errors have been made in the computations, this will also prove the validity of the slow-modulation assumption. The mathematical representation of V_{sw} is based upon an ideal sine wave current in the tank circuit at the carrier frequency (using 8.5.)

The example done below uses parameters from the actual hardware used in the TWT filament supply. The first calculation assumes modulation is applied to the input current. The parameters for the inverter are:

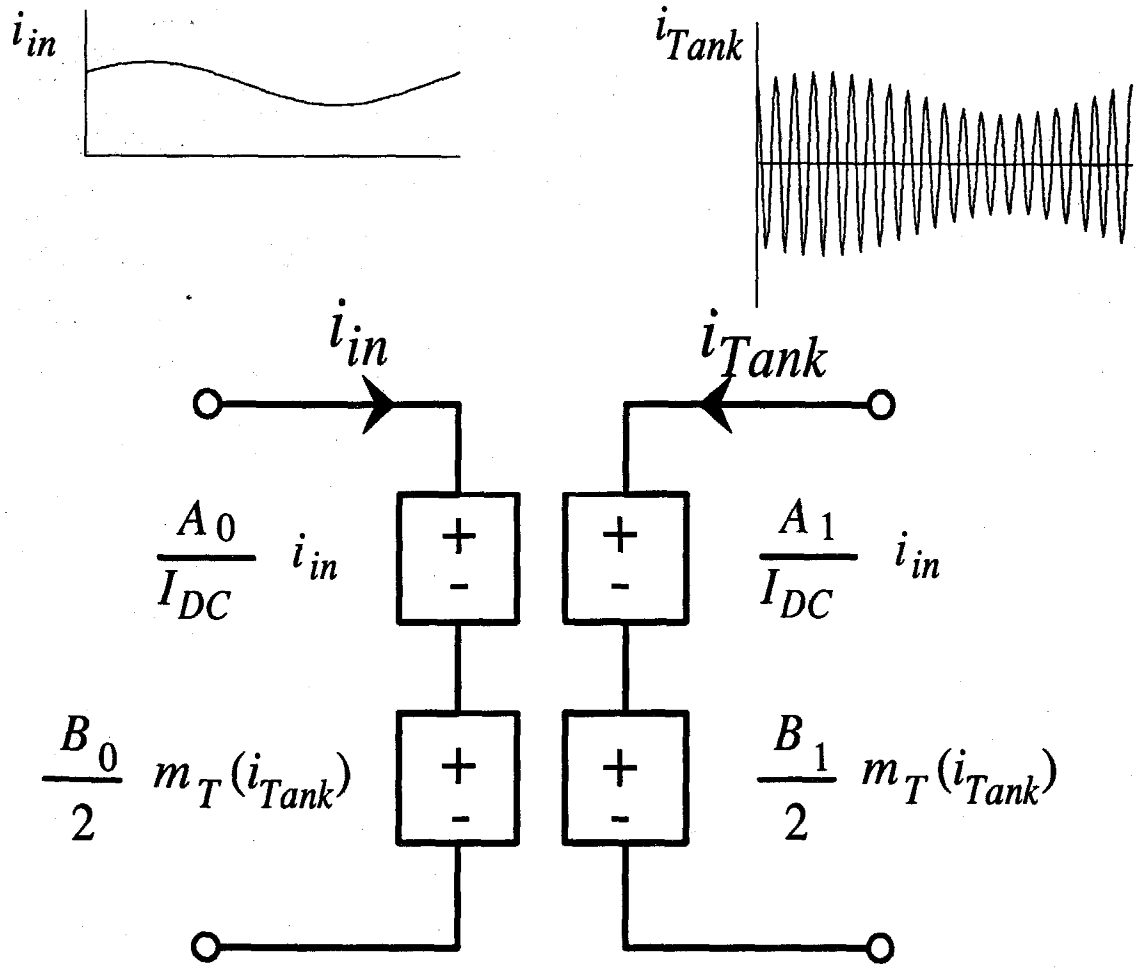


Figure 8.6: Small-Signal Model for the Class E Inverter. This model accounts for modulation on the input current and amplitude modulation on the tank current.

$$I_{in} = 538 \text{ mA}$$

$$m = 0.1$$

$$f_m = \frac{\omega_m}{2\pi} = 10 \text{ kHz}$$

$$D = 0.36$$

$$f_c = 1 \text{ MHz}$$

$$C_2 = 1600 \text{ pF}$$

These values give $A_0 = 21.79$ V (8.8) and $A_1 = 37.73 \text{ V } \angle{-87.3°}$ (8.10). The signal V'_{sw} will contain components at the modulation frequency, 10 kHz, at the upper sideband, 1.010 MHz, and at the lower sideband, 990 kHz. The term at 10 kHz arises from the fact that the carrier signal, $A(t)$, has a DC component which is amplitude modulated. From Fig. 8.6 the 10 kHz term will be 2.179 V. The upper and lower sidebands will have equal magnitudes equal to 1.88 V with phases of -87.3°. Additional information is required to carry out the numerical computation of the tank current. The simplest case will be used which is to assign an amplitude and phase for the tank current which gives a steady-state waveform for V_{sw} that closely approximates that in the actual hardware. This was done by visually approximating the tank current (which is rather far from a true sine wave) with an ideal sine wave and slightly adjusting the amplitude and phase to achieve an acceptable waveform for V_{sw}. In fact, this is how the V_{sw} waveform in Fig. 8.5 was generated. The parameters chosen were amplitude = 1.3 A and phase = 57.6°. The numerical results from Mathcad™ are listed in Table 8.1 together with results at a modulation frequency of 100 kHz. Rather surprisingly, the high modulation frequency case is more accurate than the lower frequency case which is probably due to reduced aliasing effects since both calculations involved the same number of data points. These results are from an FFT using $n = 2^{14}$ data points.

Table 8.1: Numerical Confirmation of the Inverter model with Input Current Modulation

Signal	Calculated Value (V)	Numerically Calculated Value (V)	
		$f_m = 10$ kHz	$f_m = 100$ kHz
DC	-	13.9	13.9
f_m	$2.179\angle 0°$	$2.175\angle 0.4°$	$2.173\angle 4.3°$
f_c	-	$24.7\angle{-59°}$	$24.8\angle{-60°}$
f_{USB}	$1.88\angle{-87.3°}$	$1.74\angle{-89°}$	$1.84\angle{-92°}$
f_{LSB}	$1.88\angle{-87.3°}$	$2.03\angle{-84°}$	$1.92\angle{-83°}$

The above results verify the model for input current modulation and the associated coefficients A_0 and A_1. To check the model for AM modulation of the tank current, and the associated coefficients B_0 and B_1, the same technique can be used. The coefficient B_0 from 8.11 and Table 8.1 is 13.9 - 21.79 = -7.9 V. The coefficient B_1 from 8.12 and Table 8.1 is $27.7\angle{-59°} - 37.7\angle{-87°} = 18.6\angle 49°$. Given these values, the signals of interest are easily calculated. The results are shown in Table 8.2.

Table 8.2: Numerical Confirmation of the Inverter model with Tank Current Modulation

Signal	Calculated Value (V)	Numerically Calculated Value (V)	
		f_m = 10 kHz	f_m = 100 kHz
DC	-	13.9	13.9
f_m	$0.790\angle 180°$	$0.785\angle 179.9°$	$0.790\angle 179.7°$
f_c	-	$24.75\angle{-59°}$	$24.75\angle{-60°}$
f_{USB}	$0.982\angle 57°$	$1.037\angle 65.7°$	$0.955\angle 57.6°$
f_{LSB}	$0.982\angle 57°$	$0.909\angle 49.9°$	$0.979\angle 57.1°$

In general, the results show very close agreement between the calculated and measured tank current modulation even for the rather high modulation frequency of 100 kHz. These calculations show that the low-frequency assumption regarding the integral in 8.5 is valid at least up to modulation frequencies of 100 kHz. These results do not validate the inverter model since the function used to calculate V_{sw} was constructed in accordance with several assumptions which have yet to be proven. The next logical step is to compare the predictions of the inverter model with a SPICE simulation of the actual circuit. The SPICE simulation will use non-sinusoidal voltages and currents which closely approximate the actual measured waveforms.

Inverter Model Comparison with SPICE

The inverter model is intended for use in a DC-to-DC converter and so it is logical to verify its performance installed in this type of converter rather than in an artificially contrived test circuit. To this end, the first step in the simulation is to construct a model for the DC-to-DC converter with the inverter as well as the magnetic regulator and the rectifier block. Such a model is illustrated in Fig. 8.7. The MOSFET switch in the actual circuit has been replaced by an ideal switch and the diodes have been modeled using ideal SPICE diodes. These diodes have an exponential *v-i* characteristic but no charge storage. The model is configured to provide an input AC perturbation through the source v_{in} which is an ideal sine wave source. This model should be a fairly accurate simulation of the actual circuit since the major parasitics are part of the circuit's function. (Examples of this are the shunt capacitance of the MOSFET switch and the leakage inductance of the transformer.) In this particular simulation, the control current in the magnetic regulator is held fixed so the magnetic regulator can be replaced by a simple transformer with a leakage and magnetizing inductance. The most significant effect that is *not* modeled by this circuit is the nonlinear shunt capacitance of the MOSFET; the capacitance C2 represents an average capacitance which yields a reasonably accurate switch voltage waveform in the steady state.

To provide frequency response data, the circuit of Fig. 8.7 must first be in a steady-state condition. This is accomplished by simulating the circuit for at least 100 µS (100 carrier cycles) and discarding the data prior to starting the simulation of one modulation cycle. This time interval was chosen empirically to be long enough for the circuit to settle into a periodic steady state. The time is so long because of the large inductance on the input and the large capacitance on the output. To further aid in reaching a steady-state condition quickly, these components were given an initial condition equal to the desired operating point. From this point, SPICE evolves a solution that is consistent with the circuit model.

(This is not exactly the same as the ideal operating point since SPICE is accounting for more effects than a hand calculation.) The steady-state solution for the signals of interest is shown in Table 8.3.

Table 8.3: Steady-State Solution to the DC-to-DC Converter Using SPICE.

Signal Name	Frequency	Magnitude (V or mA)	Phase (°)
I_{in}	DC	537	-
I_{tank}	f_c	1.14 A	57.9
V_{sw}	f_c	35.6	116

Once the steady-state condition is reached, the circuit is simulated for one complete cycle of the modulation frequency. This result typically contains 50 or more data points per *carrier* cycle since SPICE will only accept a value for a solution in a transient analysis if it is within a small tolerance from the last valid solution. At each point in time, SPICE is solving a nonlinear circuit for all the currents and voltages which requires many iterations to find a solution. If the timestep used by SPICE results in a change in any of the currents or voltages that is beyond the specified tolerance, the solution is rejected, the timestep is decreased and the solution is then repeated. This process continues until an acceptable solution is found or a preset minimum timestep is reached. This results in tremendous amounts of data being generated when a circuit contains many cycles of a waveform with abrupt transitions (as is the case in the rectifier part of the circuit). These data are then interpolated to give equally-spaced data points the number of which are a power of two so that the FFT can be used to extract the frequency domain data. It is this large volume of data that limits the usefulness of SPICE when calculating bode plots since the above procedure must be repeated for each modulation frequency in the bode plot.

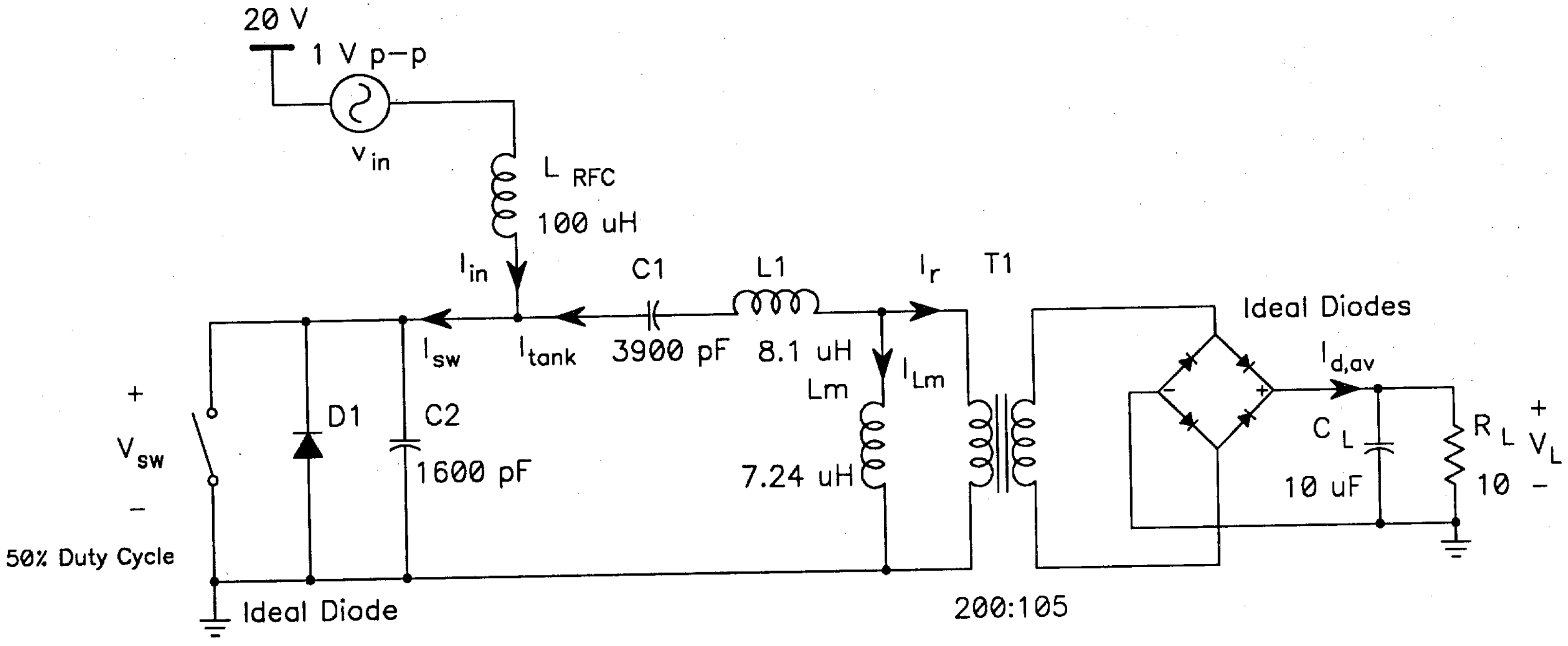


Figure 8.7: Schematic Diagram of a SPICE Model for the DC-to-DC Converter. The model uses an ideal switch for the MOSFET in the actual circuit. The diodes are all ideal SPICE diodes, i.e., they have no charge storage but do have exponential v-i characteristics.

To give the analytical inverter model the best chance for success, the coefficients B_0 and B_1 can be determined from the steady-state SPICE solution. The values are given below. (Note A_1 is shifted 180° to account for the phase in the SPICE simulation. In the simulation, the switch drive begins at $t = 0$.)

$$\begin{aligned} B_0 &= (\text{DC Average of } V_{sw}) - A_0 \\ &= 20 - 21.79 = -1.79\ \text{V} \end{aligned}$$

$$\begin{aligned} B_1 &= (\text{Fundamental of } V_{sw}) - A_1 \\ &= 35.6\angle 116^\circ - 37.73\angle 92.7^\circ = 14.95\angle{-158^\circ} \end{aligned}$$

The inverter coefficients together with the simulated input and tank currents predict a value for the switch voltage modulation as follows:

V_{sw} Modulation Due to I_{in}:

$$\text{Input current modulation index, } m_I = \frac{14.8\angle{-8.0^\circ}\ \text{mA}}{537\ \text{mA}} = 27.6 \times 10^{-3}\angle{-8.0^\circ}$$

$$\text{Modulation of } V_{sw} \text{ at } f_m = m_I A_0 = 0.60\angle{-8.0^\circ}\text{V}$$

$$\begin{aligned} \text{Modulation Sidebands on } V_{sw} &= \frac{m_I}{2}A_1 = 0.52\angle 84.7^\circ\ \text{V (upper sideband)} \\ &= \frac{\overline{m_I}}{2}A_1 = 0.52\angle 100.7^\circ\ \text{V (lower sideband)} \end{aligned}$$

V_{sw} Modulation Due to AM Modulation of the Tank Current:

$$\text{Tank current modulation index } m_T = \frac{i_{USB}}{i_c} + \overline{\left(\frac{i_{LSB}}{i_c}\right)} = 18.5 \times 10^{-3}\angle{-7.1^\circ}$$

$$\text{Modulation of } V_{sw} \text{ at } f_m = m_T A_0 = 33.2\angle{-172.9^\circ} \text{ mV}$$

$$\text{Modulation Sidebands on } V_{sw} = \frac{m_T}{2} B_1 = 0.138\angle{-165^\circ} \text{ V (upper sideband)}$$

$$= \frac{\overline{m_T}}{2} B_1 = 0.138\angle{-151^\circ} \text{ V (lower sideband)}$$

Total Modulation on V_{sw}:

$$f_m\text{: } 0.60\angle{-8.0^\circ} \text{ V} + 33.2\angle{-172.9^\circ} \text{ mV} = 0.568\angle{-8.9^\circ}$$

$$f_{USB}\text{: } 0.52\angle{84.7^\circ} \text{ V} + 0.138\angle{-165^\circ} \text{ V} = 0.490\angle{100^\circ}$$

$$f_{LSB}\text{: } 0.52\angle{100.7^\circ} \text{ V} + 0.138\angle{-151^\circ} \text{ V} = 0.494\angle{116^\circ}$$

The results from SPICE are compared with the calculations in Table 8.4. The results of this exercise show that the SPICE simulation predicts far less modulation on all of the above signals compared with the analytical model. This indicates a further refinement to

Table 8.4: SPICE Simulated Signals for Figure 8.7

Signal Name	Frequency	SPICE Simulation		Model Prediction	
		Magnitude (V or mA)	Phase (°)	Magnitude (V or mA)	Phase (°)
I_{in}	f_m	14.8	-8.0	-	-
I_{tank}	f_{USB}	11.3	80.3	-	-
	f_{LSB}	12.6	91.2	-	-
V_{sw}	f_m	128 m	-45.3	568 m	-8.9
	f_{USB}	78.4 m	106	490 m	100
	f_{LSB}	168 m	-174	494 m	116

the model is required. Note that the simulated tank current contains a small amount of phase modulation in addition to the amplitude modulation as evidenced by the fact that the sidebands are not equal in magnitude. If the phase modulation is the cause for the discrepancy, then the sensitivity to phase modulation must be high since the phase modulation index of the tank current is rather small ($K_p = 9.85 \times 10^{-3} \angle 0.4°$.) This refinement is the subject of the next section.

8.1.3 Phase Modulation of the Tank Current

The last effect to be accounted for in the inverter model is phase modulation on the tank current. The poor results of the previous section indicate the need for a refinement in the model and the current model does not account for phase modulation. Up to this point, the tank current waveform has been taken to be a sine wave at the carrier frequency to simplify the calculations. In anticipation of the high sensitivity of the model to phase modulation, this section will use a more accurate model of the tank current. The inverter is a piecewise linear circuit, which switches between two L-C networks which ring at different frequencies. Thus the tank current is, in reality, made up of segments of sine waves of different frequencies which are continuous at the switching instants. The SPICE simulation of the circuit clearly shows this behavior in Fig. 8.8. The figure illustrates the drive voltage to the MOSFET switch, the drain-source voltage of the MOSFET and the tank current. The tank current is added to the input current and integrated to get the switch voltage. The interval over which this integral is evaluated is shown as DT_s. During this interval it is fairly clear that a more accurate representation of the current is a sine wave with a DC offset whose frequency is $\omega_1 = \sqrt{L_1 C_e}$ where C_e is the series combination of C_1 and C_2. The inverter is designed such that this frequency is higher than the switching frequency. An analytical expression for this current is rather tedious to derive so a visual curve fit to

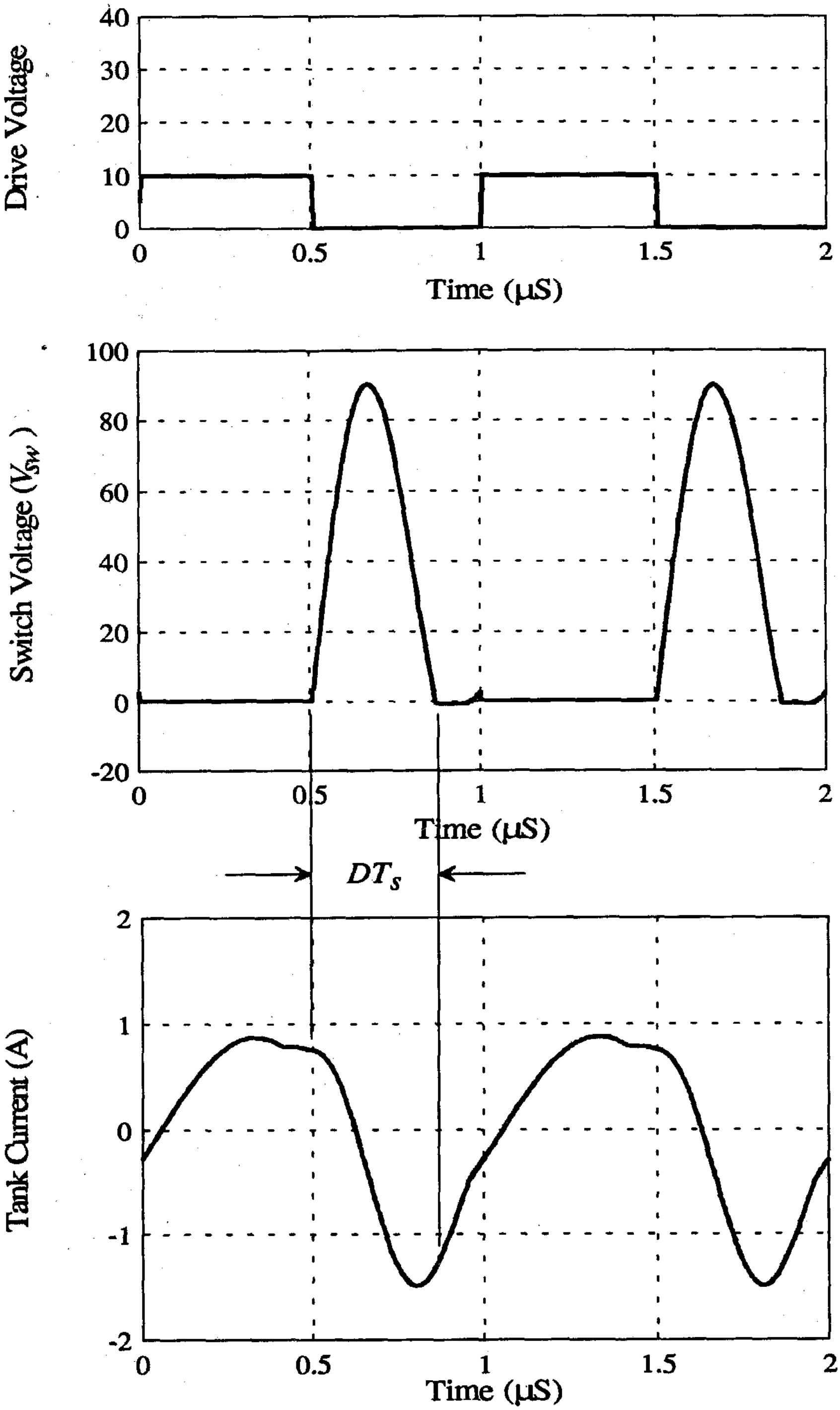


Figure 8.8: SPICE Simulation of the TWT Filament Supply. The interval marked as DT_s is the interval over which the tank current is integrated to get the switch voltage, V_{SW}. Note that during this interval, the tank current can be approximated as a sine wave with DC bias and frequency above the switching frequency.

the SPICE simulation will suffice for determining the amplitude, phase and DC offset of this current segment. Assume that the tank current is

$$I_{Tank} = I_b + I_T \cos\left[\omega_1 t + \varphi_1 + K_p \cos\left(\omega_m t + \varphi_m\right)\right] \tag{8.14}$$

where I_b, I_T, and φ_1 are to be determined from the SPICE simulation. The phase modulation parameters, K_p and φ_m, are assumed to be the same as those on the *fundamental* of the tank current. This last assumption makes the problem tractable. An alternative method would be to use the fundamental of the tank current in 8.14, which should be a good approximation in those inverter designs which have less distortion than the TWT filament power supply. The voltage on the switch can now be found from integrating 8.14:

$$V_{sw}(t) = \begin{cases} \dfrac{1}{C_2} \displaystyle\int_{nT_s}^{(t+nT_s)} I_{in} + I_{Tank}(\tau)\, d\tau & nT_s < t < nDT_s \\ 0 & nDT_s < t < (n+1)T_s \end{cases} \tag{8.15}$$

Once again the assumptions that the modulation is slow compared to the switching frequency and that it is small can be used to simplify the integrand of 8.15:

$$I_{Tank} \approx I_b + I_T \cos\left(\omega_1 t + \varphi_1\right) - I_T K_p \sin\left(\omega_1 t + \varphi_1\right) \cos\left(\omega_m t + \varphi_m\right) \tag{8.16}$$

Equations 8.16 and 8.15 together give the following form for the switch voltage:

$$V_{sw}(t) = V_{sw,DC}(t) - K_p \cos\left(\omega_m t + \varphi_m\right) g(t) \tag{8.17}$$

where $V_{sw,DC}$ is the switch voltage without any modulation and

$$g(t) = \begin{cases} \dfrac{I_T}{C_2} \displaystyle\int_{nT_s}^{(t+nT_s)} \sin(\omega_1\tau + \varphi_1)\, d\tau & nT_s < t < DnT_s \\ 0 & DnT_s < t < (n+1)T_s \end{cases} \tag{8.18}$$

Since the function $g(t)$ is not modulated, each cycle is the same as the next cycle and therefore $n = 0$ can be used to fully describe $g(t)$. It is useful to view a graph of $g(t)$ to keep in mind what it represents. The function $g(t)$ is shown in Fig. 8.9 together with V_{sw} for comparison. The sidebands on the switch voltage arise from the multiplication of $g(t)$ by the phase modulation factor, $K_p \cos(\omega_m t + \varphi_m)$. The resulting spectrum is shown in Fig. 8.10. The small-signal model for the inverter now picks up two additional voltage sources: a source that generates a voltage at the modulation frequency (coefficient g_0) and a source that generates upper and lower sidebands (coefficient g_1). The coefficients g_0 and g_1 are readily determined from the Fourier series of 8.18:

$$g_0 = \frac{I_T}{C_2 T_s} \int_0^{DT_s} \left[\int_0^t \sin(\omega_1\tau + \varphi_1)\, d\tau \right] dt \tag{8.19}$$

$$g_0 = \frac{I_T}{C_2 T_s} \left[\frac{-\sin(\omega_1 DT_s + \varphi_1) + \omega_1 DT_s \cos(\varphi_1) + \sin\varphi_1}{\omega_1^2} \right] \tag{8.20}$$

$$g_1 = \frac{2I_T}{C_2 T_s} \int_0^{DT_s} \left[\int_0^t \sin(\omega_1\tau + \varphi_1)\, d\tau \right] e^{-j\omega_c t}\, dt \tag{8.21}$$

It is best to use symbolic integration software to evaluate 8.21 since the result is lengthy. The integrals done above all assume $t = 0$ coincides with the switch turn-off for the convenience of the calculations. However, the SPICE model uses a time reference of

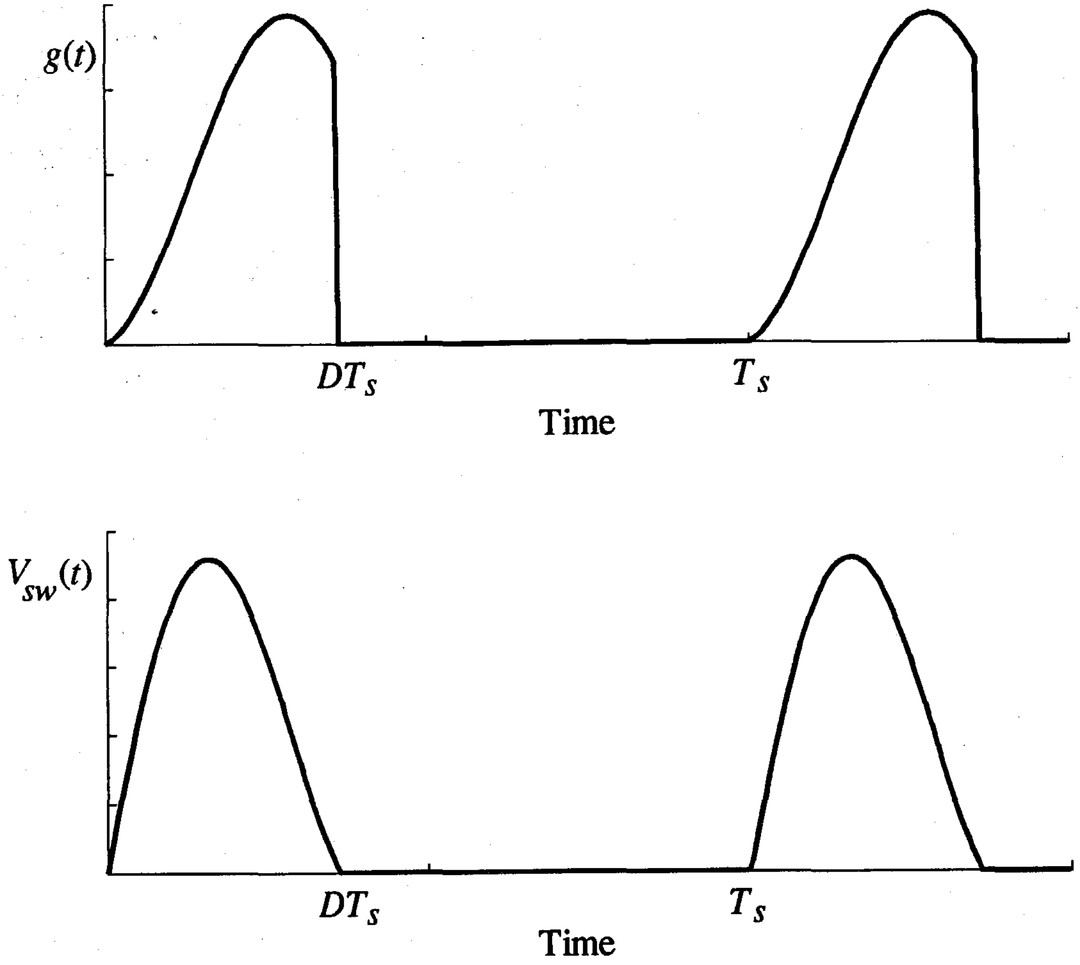


Figure 8.9: The Function $g(t)$ together with V_{sw}. The function $g(t)$ is multiplied by the phase modulation function to determine the sidebands on V_{sw} due to phase modulation of the tank current.

the switch turn-on point, so for the purpose of all subsequent model development, it is more convenient to use the SPICE time reference. Therefore, the inverter coefficients A_1, B_1, and g_1 must all be phase-shifted by 180°.

The phase-modulation coefficients can be calculated for the waveform shown in Fig. 8.8. The estimated parameters are:

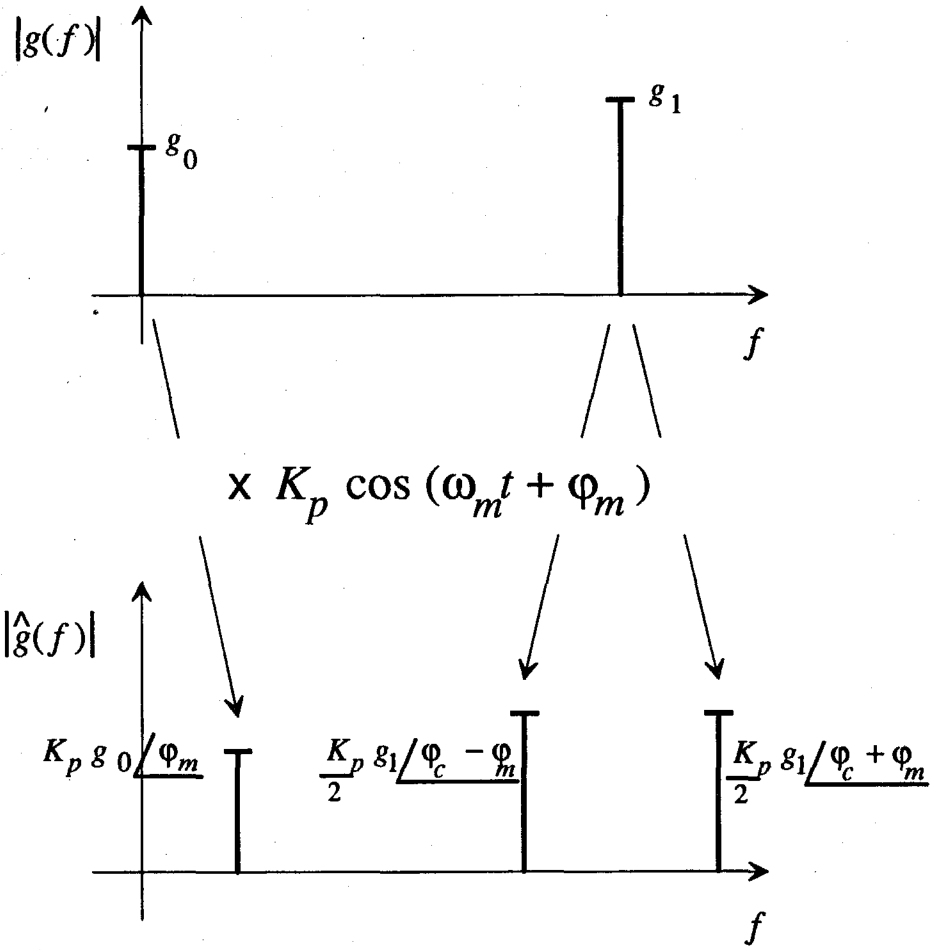


Figure 8.10: Spectrum of $g(t)$ before and after modulation. The modulating function does not contain a DC term, so there is no component at DC or at the carrier frequency in the result.

$$I_T = 1.3\ \text{A}$$
$$I_b = -0.22\ \text{A}$$
$$\varphi_1 = 11°$$
$$f_1 = 1.66\ \text{MHz}$$
$$C_1 = 3900\ \text{pF}$$
$$C_2 = 1600\ \text{pF}$$
$$D = 0.36$$

The corresponding coefficients are:

$$g_0 = 34.34\angle{-180°}\ \text{V}$$
$$g_1 = 60.7\angle{-85.4°}\ \text{V}$$

If the fundamental of the tank current is used for I_{Tank}, there is no DC term (i.e., $i_b = 0$) and the frequency is equal to the switching frequency. In this case the values are

$$g_0 = 39.37\angle{-180°}$$
$$g_1 = 68.22\angle{-84°}$$

These values for $g0$ and $g1$ illustrate the sensitivity of the model to the waveform used for V_{sw}. In the overall DC-to-DC converter model described below, these latter values actually gave better agreement with the measured results.

The new small-signal model for the inverter is illustrated in Fig. 8.11. The two additional voltage sources account for the effect on V_{sw} of phase modulation of the tank current. The magnitude of the g_0 and g_1 coefficients indicate that the inverter model is quite sensitive to phase modulation. The coefficients g_0 and g_1 themselves are rather sensitive to the form assumed for the switch current, meaning the overall results from the model are sensitive to the operating conditions of the inverter.

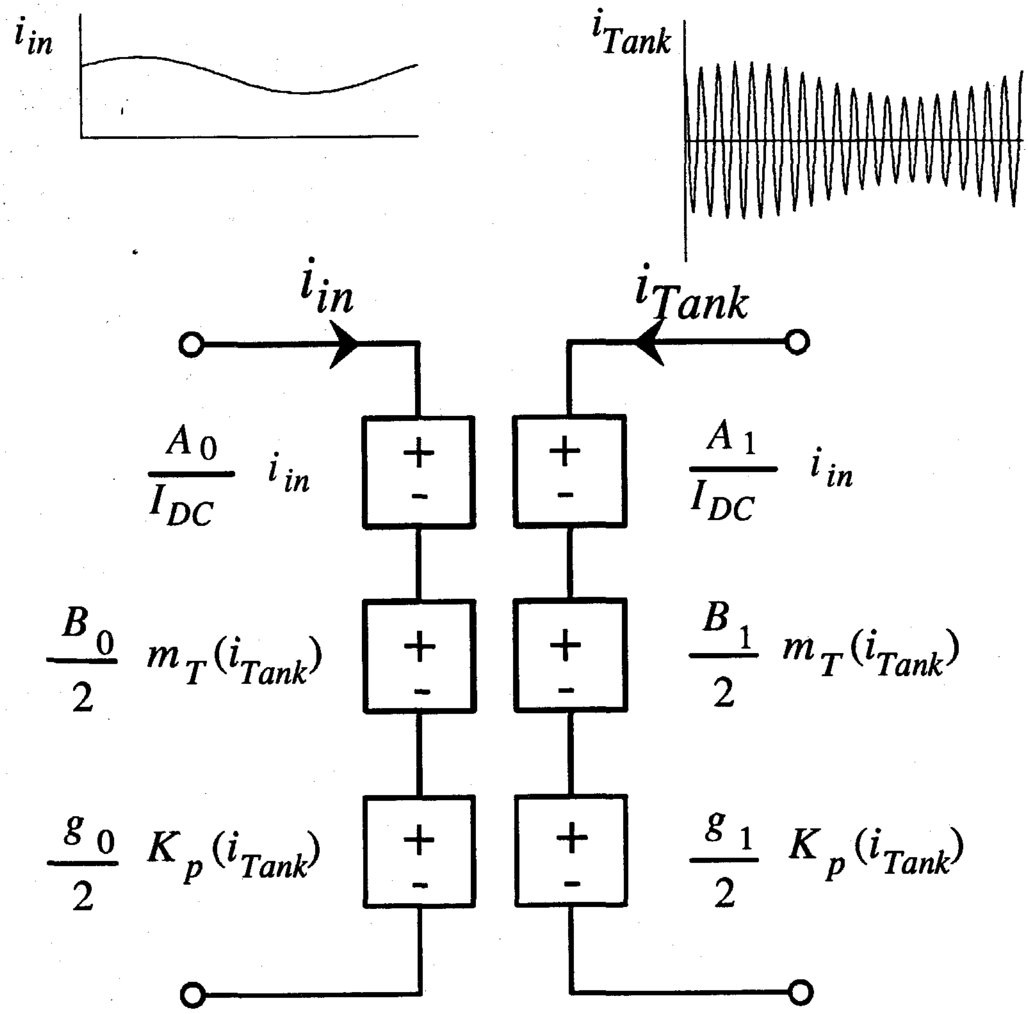


Figure 8.11:Small-Signal Model for the Class E Inverter. The model now includes phase modulation on the tank current in addition to amplitude modulation and modulation on the input current.

The model for the inverter is now complete. The inputs to the model are the input current and the tank current. The model responds to modulation on the input current and both amplitude and phase modulation on the tank current. In the next section, the model will be inserted into the DC-to-DC converter model and the resulting transfer functions derived.

Note that this model is capable of predicting the input impedance and the input-output transfer function for the first time in this model development.

8.2 The DC-to-DC Converter Model with the Full Inverter and Rectifier Models

Equipped with the new model for the inverter, the overall DC-to-DC converter model can now be examined. A new feature of this model is that it provides an explicit port for the DC input which makes the input impedance and input-output transfer function calculations possible. The first step, however, is to consider the control-to-output transfer function and the output impedance since they were the initial motivation for the refined model.

8.2.1 The Control-to-Output Transfer Function

The full small-signal model for the DC-to-DC converter is shown in Fig. 8.12. In the case of the control-to-output transfer function, the input voltage source v_{in} is set to zero effectively shorting the input. This does not short the input to the tank circuit since the input inductor together with the new elements in the inverter model will produce a non-zero voltage for V_{sw}. The new input port to the model requires that one additional equation be added over those in section 7.2.1 and also requires some changes to the existing equations. The new equation concerns i_{in}:

$$i_{in} = \frac{v_{in} - v_{sw,bb}}{s_m L_{RFC}} \tag{8.22}$$

where the subscript *bb* refers to baseband (i.e., the modulation frequency) and

$$v_{sw,bb} = \frac{i_{in}}{I_{DC}} A_0 + B_0 \left[\frac{i_{USB}}{i_c} + \overline{\left(\frac{i_{LSB}}{i_c} \right)} \right] + g_0 \left\{ j \left[\overline{\left(\frac{i_{LSB}}{i_c} \right)} - \frac{i_{USB}}{i_c} \right] \right\} \tag{8.23}$$

The other equations that are changed are 7.55 and 7.56. The new equations are:

$$i_{LSB} = \frac{V_{sw_L} - (G_{LSB} + V_{a_L})}{z_x(s_L)} \tag{8.24}$$

$$i_{USB} = \frac{V_{sw_u} - (G_{USB} + V_{a_u})}{z_x(s_u)} \tag{8.25}$$

These new equations result in a new A matrix and x and b vectors. The new submatrices that make up A are:

$$A_1 = \begin{bmatrix} 0 & z_x(s_L) + P_1 & 0 & 0 & 0 & 1 & 0 \\ z_x(s_u) + P_1 & 0 & 0 & 0 & 1 & 0 & P_3 \\ 0 & 0 & P_5(s_m) + P_6 & 0 & -\frac{\pi}{2}e^{-j\varphi_d} & 0 & 0 \\ 0 & 0 & 0 & \overline{P_{55}(s_m)} + P_6 & 0 & -\frac{\pi}{2}e^{-j\varphi_d} & 0 \\ 0 & 1 & 0 & -1 & 0 & -\frac{1}{s_L L_m} & 0 \\ 1 & 0 & -1 & 0 & -\frac{1}{s_u Lm} & 0 & 0 \\ P_7 & 0 & 0 & 0 & 0 & 0 & P_9 \end{bmatrix} \tag{8.26}$$

$$A_2 = \begin{bmatrix} P_2 & 0 & 0 & 0 & 0 & 0 & P_3 \\ 0 & P_2 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & P_{55}(s_m) - P_{66} & 0 & 0 & 0 \\ 0 & 0 & \overline{P_5(s_m)} - P_{66} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & P_8 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{8.27}$$

The new matrix coefficients are

$$P_1 = -\frac{1}{2}\left(-\frac{B_1}{I_c} + j\frac{g_1}{I_c}\right)$$

$$P_2 = -\frac{1}{2}\left(-\frac{B_1}{\overline{I_c}} + j\frac{g_1}{\overline{I_c}}\right)$$

$$P_3 = -\frac{1}{2} \cdot \frac{A_1}{I_{DC}}$$

$$P_7 = \left(\frac{B_0}{I_c} - j\frac{g_0}{I_c}\right)$$

$$P_8 = \left(\frac{B_0}{\overline{I_c}} + j\frac{g_0}{\overline{I_c}}\right)$$

$$P_9 = \frac{A_0}{I_{DC}} + s_m L_{RFC}$$

As before, the A_1 and A_2 submatrices and their conjugates combine to produce the total A matrix as in 7.71. The new x vector is

$$x_1^T = \left[i_{USB} \; i_{LSB} \; i_{r_u} \; i_{r_L} \; G_{USB} \; G_{LSB} \; i_{in} \right] \tag{8.28}$$

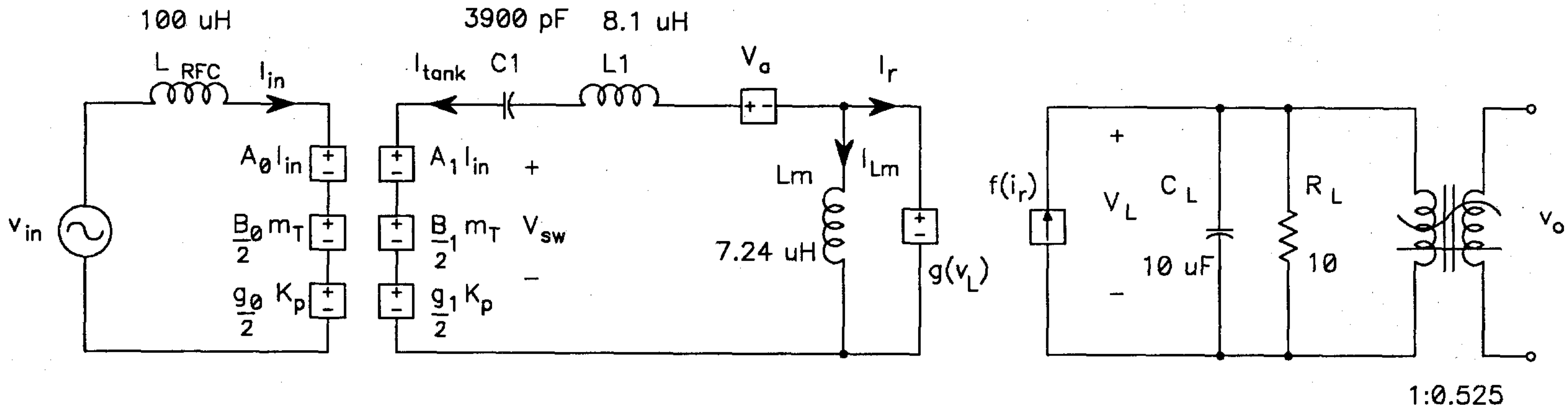


Figure 8.12: Final Small-Signal Model for the DC-to-DC Converter. The new inverter model has now replaced the short at the input that was present in all previous models.

The total x vector is still given by 7.73. The new b vector is

$$b_1^T = \left[-R_{1_L}\ -R_{1_u}\ 0\ 0\ 0\ 0\ v_{in}\right] \tag{8.29}$$

The total b vector is 7.75. The solution to the matrix equation follows the same path as before with these new elements. The control-to-output transfer function is calculated from the new matrix solutions using 7.77.

Measured Results

The new converter model can now be applied to the same experimental circuit as in Chapter 6. The results are shown in Fig. 8.14. If these results are compared to the results of Chapter 7, it is clear that the corner frequency is now essentially correct. The DC gain is now slightly off and the Q associated with the rolloff is too high. The fact that the Q is too high is the usual case in modeling power systems since there are always loss elements that are not accounted for. (For example, the core loss in the magnetic regulator is ignored in this case.) Small changes to the inverter coefficients can bring the measured and predicted data into closer agreement, but this is only one of several functions of interest. The other functions should be plotted before any adjustment of the parameters is made.

8.2.2 The Output Impedance

As in the previous chapters, it is the *internal* output impedance that is the function of interest. The equivalent circuit for this function is shown in Fig. 8.13.

Predicted Results

The matrix equation used to calculate the control-to-output transfer function can be used to calculate the output impedance by altering a few terms in the A_1 and A_2 submatrices and in the b_1 vector. The entries that must change are $(A_1)_{3,3}$, $(A_1)_{4,4}$, $(A_2)_{3,4}$, and

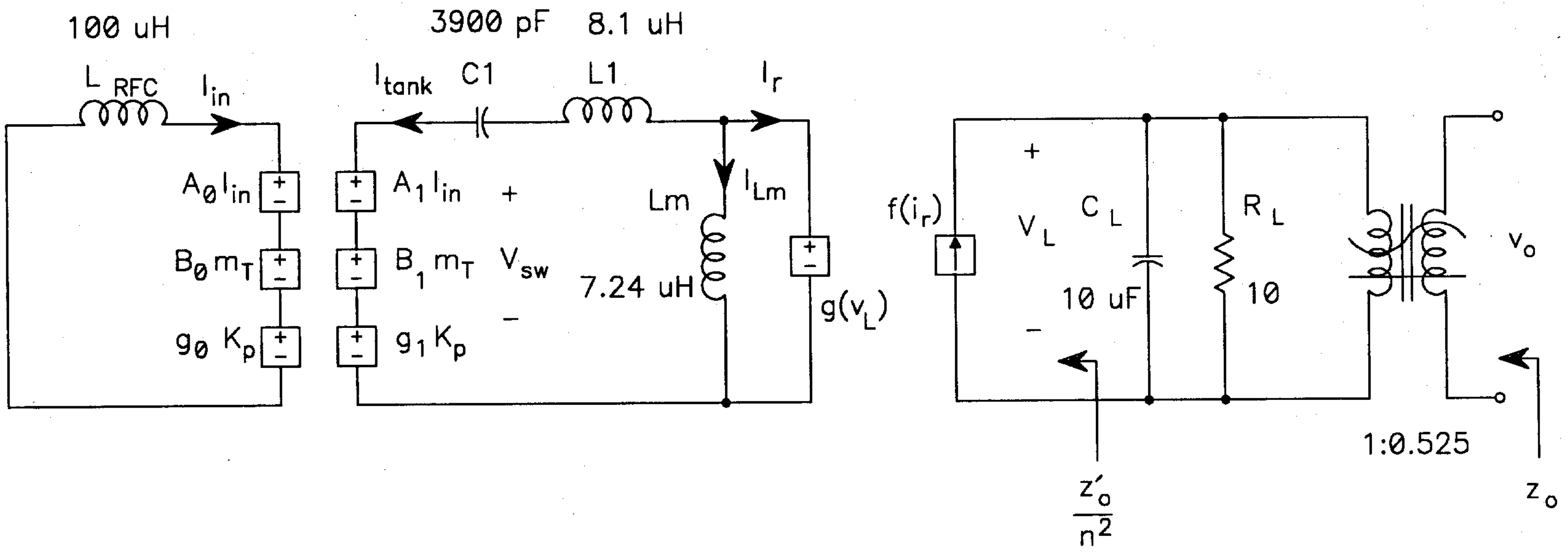


Figure 8.13: Equivalent Circuit of the DC-to-DC Converter Output Impedance calculation. The internal output impedance z'_o is of interest.

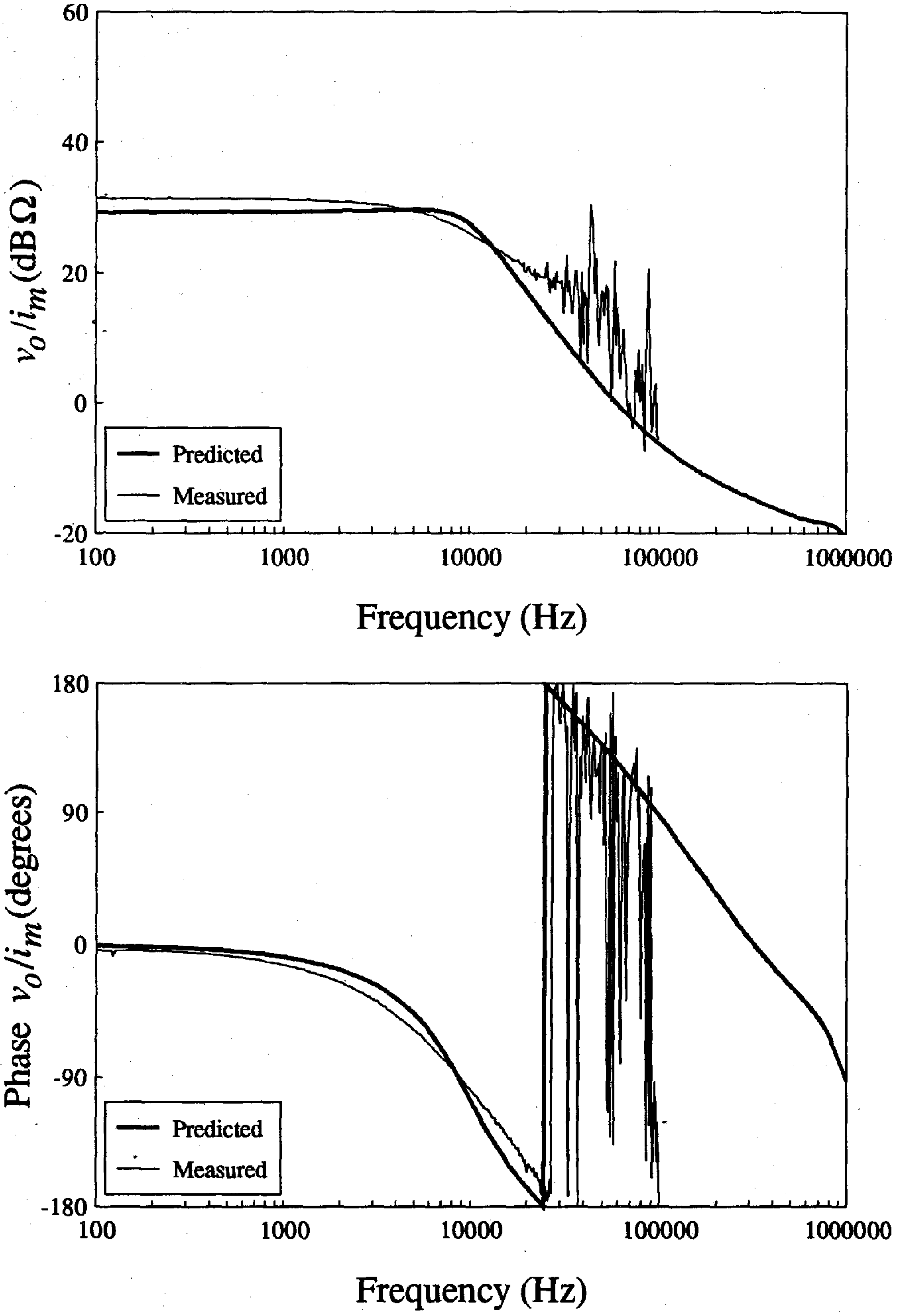


Figure 8.14: Control-to-Output Transfer Function for the TWT Filament Supply, with Predicted Results from the Full Model.

$(A_2)_{4,3}$ in the A matrix and $(b_1)_{3,1}$ and $(b_1)_{4,1}$ in the b vector. These changes are exactly the same as those made in Chapter 7.

Measured Results

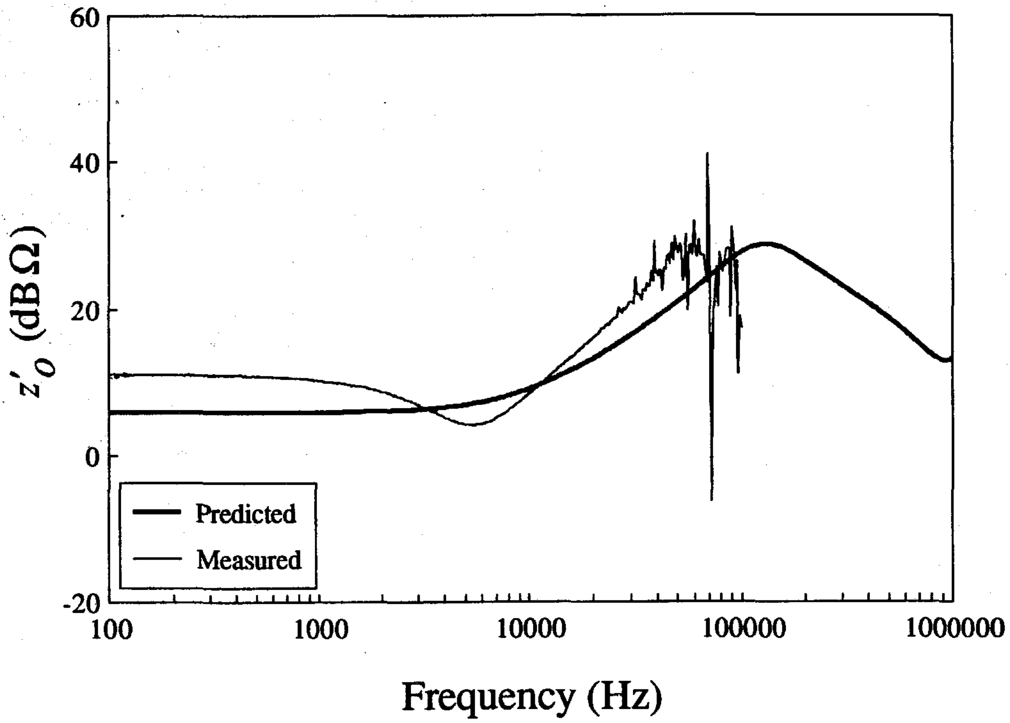
The measured versus predicted results are shown in Fig. 8.15. This result should be compared against Fig. 7.12. The actual output impedance is still higher than predicted although this could be expected since none of the resistances in either the magnetic regulator windings or the rectifiers are accounted for in the model. Nevertheless, the new result is somewhat closer to the measured data than that in Chapter 7. The break frequency observed in the output impedance is now nearly at the correct frequency. In the case of the output impedance, the measured circuit would appear to exhibit a higher Q than the prediction, an unexpected result especially in light of the control-to-output transfer function result.

8.2.3 Input Impedance

With this new model for the inverter, the input impedance can be calculated easily. The matrix equation derived in section 8.2.1 can be used directly to extract the input impedance by first setting the control input to zero and the v_{in} source to one. Given that the input voltage is one, the input impedance is simply

$$z_{in} \equiv \frac{v_{in}}{i_{in}} = \left.\frac{1}{i_{in}}\right|_{v_{in}=1} = \frac{1}{x_7} \tag{8.30}$$

where x_7 is the seventh element in the x vector.



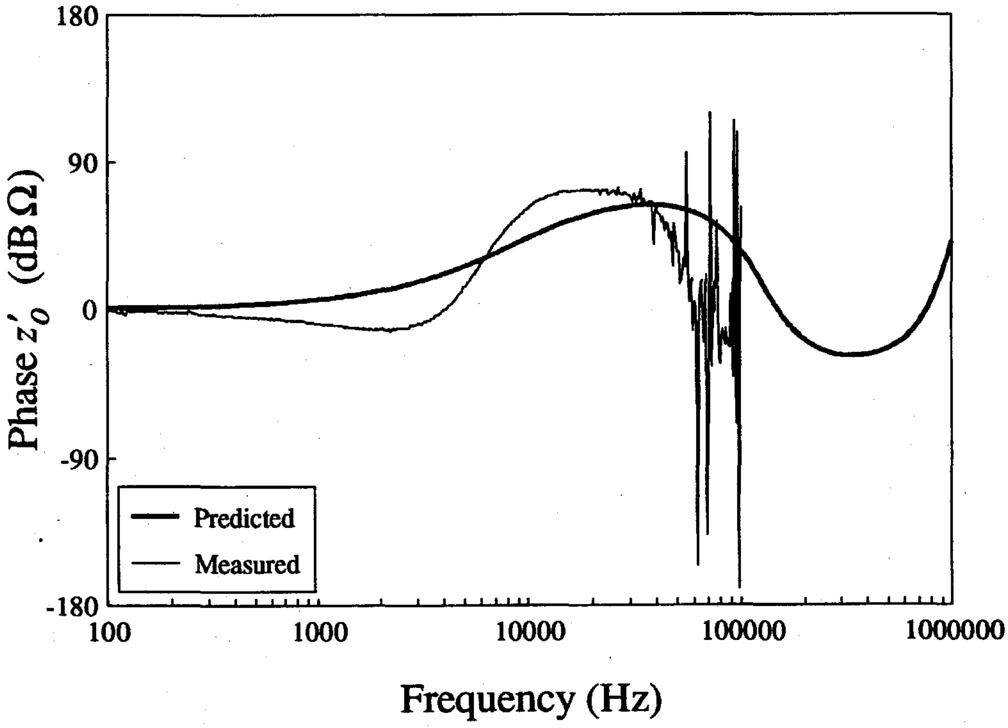


Figure 8.15: Predicted Versus Measured Output Impedance of the DC-to-DC converter Using the Full Inverter Model.

Measured Results

The input impedance is measured using a DC power supply to provide the input voltage to the experimental circuit and a series transformer to inject an AC signal into the converter's input. The AC signal is supplied by a network analyzer and the input voltage and current are sampled by the analyzer to form the input impedance measurement. The control current to the magnetic regulator is supplied by an externally-adjusted power supply to set the proper operating conditions. As in the case of the output impedance measurement, it is important to use a DC current probe to sample the input current to avoid saturating the measurement on the steady-state input current. The measured and predicted data are plotted for comparison in Fig. 8.16. In this measurement, as in the output impedance measurement, the actual circuit seems to have a higher Q than that predicted by the model. The predicted input impedance at low frequencies is too low but is nearly correct at high frequencies. The frequency of the minimum in $|z_{in}|$ is accurately predicted by the model.

8.2.4 The Input-Output Transfer Function

The input-output transfer function is the last function to be calculated for the DC-to-DC converter. Much like the input impedance, this function is predicted for the first time by the new converter model. This function can be measured to a much higher modulation frequency than the control-to-output transfer function because it does not involve driving the control current. (Recall that the large inductance of the control winding prevented high modulation frequencies from entering into the control current.) This makes the input-output response more useful than the control-to-output transfer function to investigate the high-frequency predictions of the model.

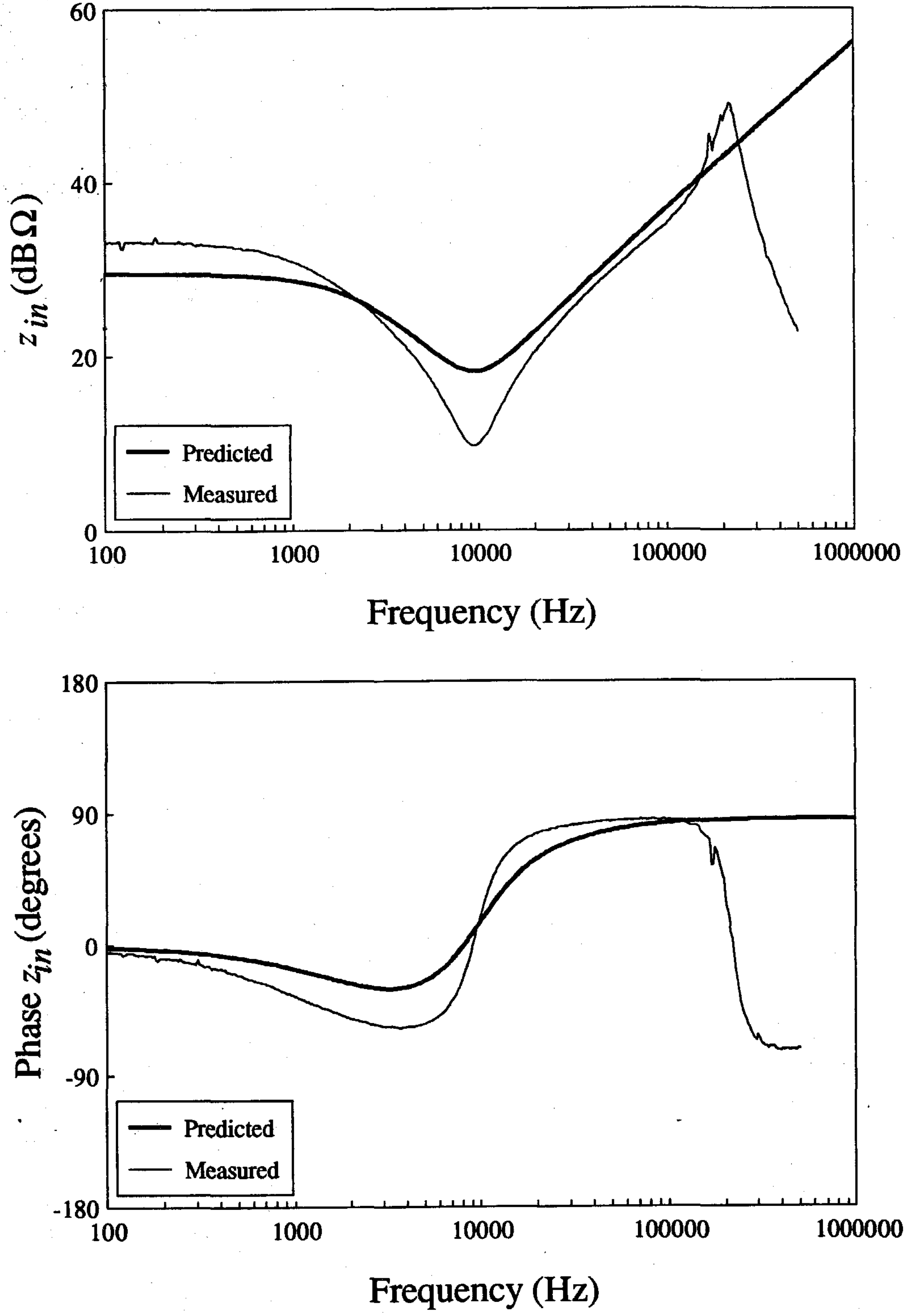


Figure 8.16: Input Impedance to the DC-to-DC Converter. This function can only be calculated using the new inverter model. Previous models did not predict this response.

Predicted Result

This function can be measured and calculated at the same time as the input impedance. The control current is set to zero and a biased AC signal is applied to the input of the converter. For the calculation it remains convenient to set the input voltage equal to one. Under this assumption, the input-output transfer function, H_o, is

$$H_o \equiv \frac{v_o}{v_{in}} = v_o\Big|_{v_{in}=1} = i_{d,av}\left[\frac{x_3}{i_{r_c}} + \overline{\left(\frac{x_4}{i_{r_c}}\right)}\right]z'_L n \tag{8.31}$$

Measured Result

The measured and predicted results for the input-output response are both plotted in Fig. 8.17 for comparison. Note that this function is much like the input impedance and output impedance in that the prediction has a lower Q than the measurement, although the frequency of the resonance is correct.

8.3 Small-Signal Model Evaluation

In three of the four previous results, the model predicts a lower Q than the actual circuit exhibits. Interestingly, these three transfer functions do not involve the control variable since in each case the control variable is set to zero. In the one case where the control variable is the input, the circuit Q is in fact lower that the predicted Q although in this case the entire model comes into play (i.e., the control-to-output response does not disable portions of the circuit that might be responsible for lowering the Q).

In the case of the functions which do not include the control variable, a greatly simplified model is possible which has better accuracy than the results presented here. The observation that the dynamics of this converter are dominated by the low-frequency elements L_{RFC} and C_L and that any dynamics associated with the tank circuit and the carrier

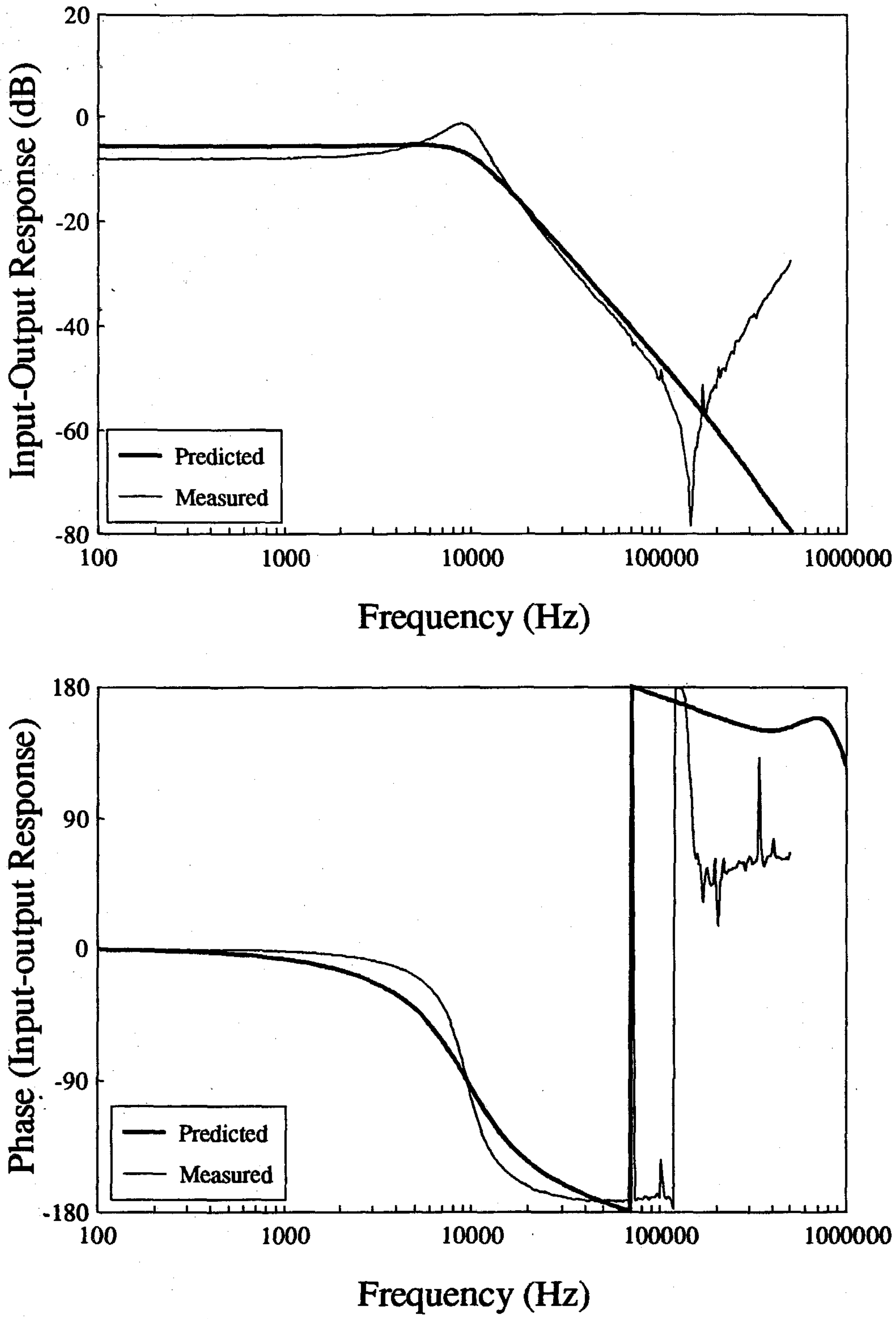


Figure 8.17: Measured Versus Predicted Results For the Input-Output Response of the TWT Filament Supply.

frequency path through the inverter are much higher in frequency suggests that the inverter-(tank circuit)-rectifier could be modeled as a frequency independent block, with low-frequency input and output currents and voltages. This is the approach taken in [24]. A diagram of this model is shown in Fig. 8.18.

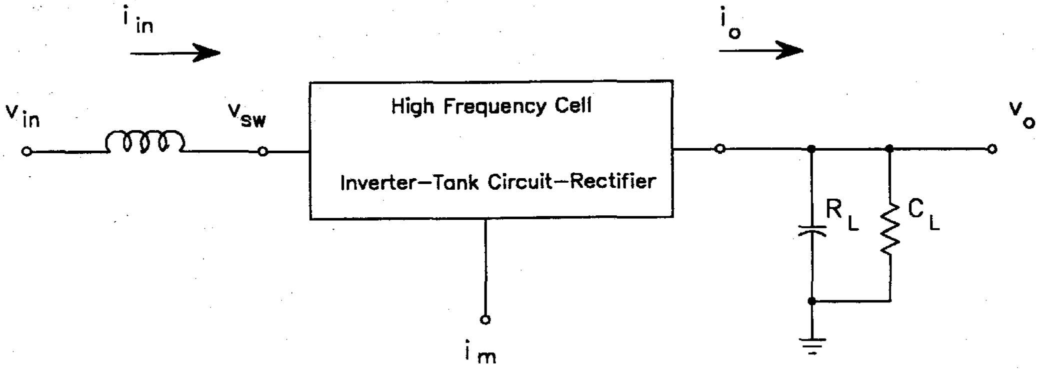


Figure 8.18: Model for the DC-to-DC Converter With all High-Frequency Circuits Combined into a Block. This is referred to a the external model since it looks at the high-frequency circuits from the outside.

This analytical approach also allows for the addition of the control variable to the high-frequency part of the model. This is accomplished through the use of mathematical expressions for the currents and voltages inside the cell and partial derivatives of the currents and voltages. This model can be thought of as an 'external' view where the details of the circuit are largely ignored and only the input and output low-frequency quantities are of interest. In contrast, the model developed in these last several chapters is an 'internal' model. It starts from the heart of the high-frequency cell and works outward to the low frequency quantities at the inputs and outputs. This model is the natural one when the control variable enters the circuit through an element inside the cell such as the magnetic regulator and its variable inductance. The fact that the external model more accurately predicts the input-output response, the input impedance, and the output impedance than the internal model is most likely due to the difficulty in determining the parameters associated with the inverter and rectifier portions of the circuit. This internal model by its very nature also is more susceptible to the distortion of the waveforms inside the cell since some of the required parameters are dependent upon the actual waveforms. The parameters determined for the inverter that were used in this chapter were determined using the sinusoidal approximation for the tank current. In Fig. 8.8 the tank current appears unlike a true sine wave. Even though the calculation of the inverter parameters took into account some of the distortion, the tank current distortion also affects the magnetic regulator and the rectifier models in ways not accounted for. Some converter designs have currents which much more closely conform to the sinusoidal tank current model. In these cases, the internal model parameters should yield more accurate results. (The present experimental circuit probably represents a worst-case for tank current distortion.)

The advantage to the internal model is that it does predict the conditions inside the cell and will account for the high-frequency effects of the tank circuit. The internal model also predicts the control-to-output response using a circuit-based model for the magnetic regulator. Recall that in Chapter 5 it was found that a quadratic double pole in the control-to-output response would occur at the switching frequency plus or minus the natural frequency of the tank circuit. This suggests that cell-related dynamics may appear in the frequency range of interest since the resonant frequency of the tank circuit is rather close to the switching frequency. Also these cell-related dynamics move significantly with the operating point of the converter. Note that the natural frequency of the tank circuit in an actual DC-to-DC converter is very difficult to determine since the tank capacitor has the output impedance of the inverter and the input impedance of the rectifier circuit in series with it (these impedances are highly nonlinear).

Other significant advantages to the internal model may appear when more sophisticated control means are considered. There may be some advantage to sensing and controlling some of the quantities that are internal to the high frequency cell such as the switch maximum voltage or maximum current (this would be analogous to current-mode programming [25] in PWM-type converters). This avenue of investigation could provide a fruitful topic for further research.

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