INVESTIGATIONS OF DEEP LEVEL DEFECTS IN SEMICONDUCTOR MATERIAL SYSTEMS

Thesis by

Arati Prabhakar

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To Raj, my mother

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ABSTRACT

In this thesis, we present the results of two groups of investigations of deep level defects in semiconductor material systems.

Chapter 1 consists of an overview of the thesis, background information on semiconductor impurities, and a description of deep level transient spectroscopy (DLTS).

Chapter 2 contains discussions of the experiments performed on transition metal silicide-silicon Schottky barrier structures to probe for the existence of deep levels. We investigated platinum, palladium, and nickel silicides on n-type silicon which were annealed at temperatures from 300 to 800 °C. The primary techniques used were DLTS, current-voltage (I-V), and capacitance-voltage (C-V) measurements for electronic characterizations, and Rutherford backscattering spectrometry (RBS) to determine the silicide phase and film condition. For our samples, 700 °C was the maximum temperature below which no significant degradation of the barrier or contamination of the underlying silicon were observed in platinum and palladium silicide structures. Nickel silicide structures could only withstand temperatures up to 500 °C. Cobalt, chromium, and erbium silicides were also studied using DLTS. These measurements constitute the first series of studies of deep level contamination of the silicon underlying a transition metal silicide thin film.

Chapter 3 details our DLTS studies of four different compositions of the alloy $In_{1-x}Ga_xAs_yP_{1-y}$. Our samples, with bandgaps of 0.75, 0.83, 0.95,

and 1.1 eV, covered the range of compositions that are lattice-matched to InP and are used for long-wavelength optoelectronic devices. No traps were observed above the detection limit of 5×10^{13} cm^{-3}. The only exception was one sample, which had a trap that was attributed to a lattice defect in the substrate. These DLTS experiments were the first attempt to investigate deep level defects in $In_{1-x}Ga_xAs_yP_{1-y}$.

Parts of this thesis have been or will be published under the following titles:

Platinum diffusion into silicon from PtSi, A. Prabhakar, T. C. McGill, and M-A. Nicolet, Appl. Phys. Lett. **43**, 1118 (1983).

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Thermally Induced Transition Metal Contamination of Silicide Schottky Barriers on Silicon — Physics of VLSI Conference, August, 1984.

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Deep Levels in Silicon from Transition Metal Silicides — Materials Research Society Meeting, November, 1983.

Silicide Silicon Structures Probed by DLTS — Electronics Materials Conference, June, 1983.

CONTENTS

CHAPTER 1

THE APPLICATION OF DEEP LEVEL TRANSIENT SPECTROSCOPY TO THE STUDY OF DEFECTS IN SEMICONDUCTORS

1.1 Overview of the Thesis

Because deep level defects can alter the electronic properties of a semiconductor significantly, a knowledge of their existence in materials for devices can be very important. In this thesis, the existence of deep traps is investigated in two different semiconductor systems.

Chapter 2 of this thesis details the first group of experiments. These experiments are examinations of structures consisting of a thin film transition metal silicide (TMS) on a silicon substrate. Transition metal silicides are used in integrated circuits and may also find future application in multilayer silicon molecular-beam-epitaxy (MBE) structures. They are typically formed by annealing a substrate with a pure metal overlayer. Any indiffused metal atoms could degrade and ruin devices. The purpose of our studies of a variety of TMS's was to determine the annealing temperatures at which this indiffusion becomes significant. The bulk of the analysis dealt with platinum, palladium, and nickel silicides on silicon which had been treated at temperatures from 300 to 800 °C for times from 30 to 180 min. We also investigated cobalt, chromium, and erbium silicides. Electronic characterizations were made using deep level transient spectroscopy (DLTS), current-voltage, and capacitance-voltage measurements. Rutherford backscattering spectrometry was also used to characterize the silicide layer. These measurements comprise the first investigations of the deep-level contamination of silicide-silicon structures.

Chapter 3 is a discussion of the second system in which we searched

for traps: the quaternary alloy $In_{1-x}Ga_xAs_yP_{1-y}$. Various compositions of this material are used to make long-wavelength lasers and detectors for fiber optic communications systems. Early attempts to fabricate high-quality lasers in the 1.3–1.5 μm range failed because threshold currents were too high and quantum efficiencies too low. In alloys across the range of compositions lattice-matched to InP, we used DLTS to investigate the existence of traps that could have been responsible for these difficulties. This set of DLTS measurements was the first attempt to search for deep levels in $In_{1-x}Ga_xAs_yP_{1-y}$.

The remainder of this introductory chapter is as follows: Section 1.2 contains background information on defects in semiconductors. Section 1.3 is a description of the main features of DLTS, the primary technique used in this work. Section 1.4 is a summary of the results of this thesis.

1.2 Defects in Semiconductors

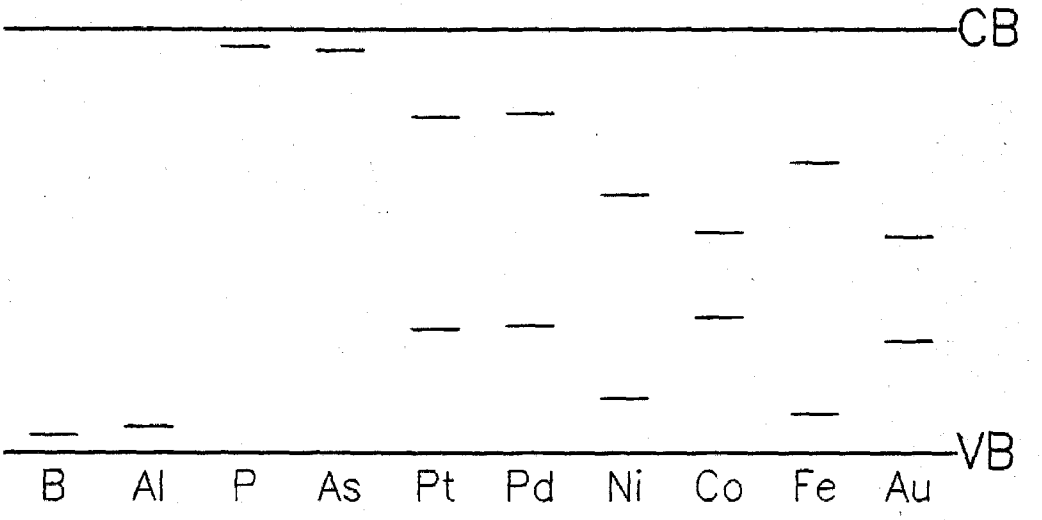
Of the many types of materials that are technologically important today, semiconductor crystals require the greatest level of impurity control. While a metal is considered extremely pure with contaminant concentrations as high as one part in ten thousand, or $\sim 10^{18}$ atoms cm^{-3}, semiconductor devices can require crystal materials with less than 10^{13} electrically active impurities cm^{-3}. The control of the type and amount of impurity in the various parts of a semiconductor material is key in the construction of any device. Electronic impurities in semiconductor crystals are generally grouped in two large catagories: shallow impurities and deep level defects. Figure 1.1 shows the location of several shallow and deep levels in the bandgaps of silicon and gallium arsenide, the two most common semiconductor materials. Each level is labeled according to the element with which it is correlated. The technologically important defect in GaAs known as $EL2^1$ is also shown.

1.2.1 Shallow Impurities

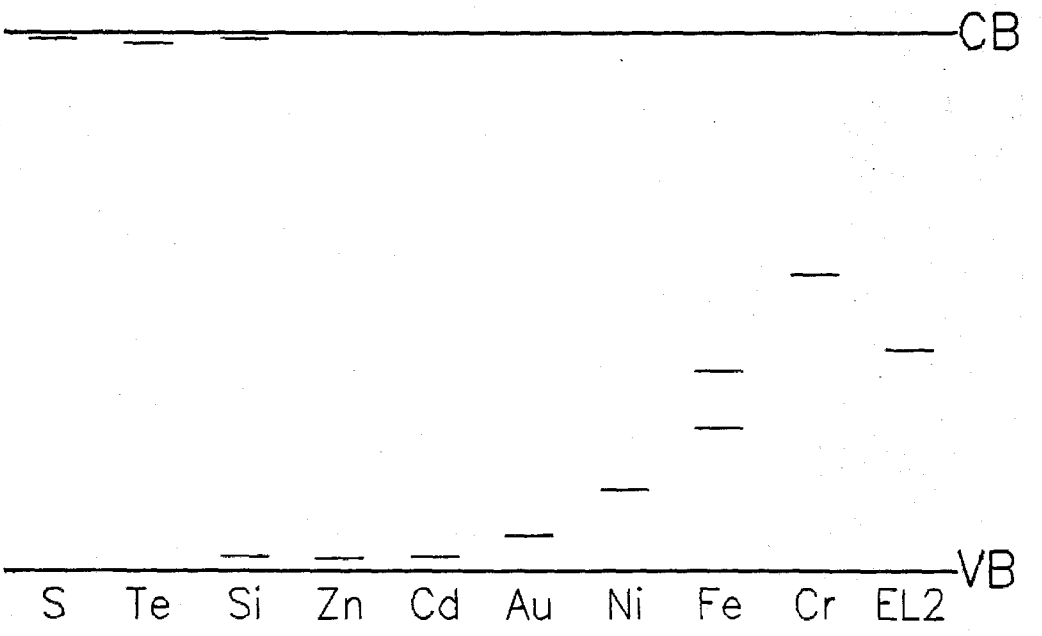
Physically, a shallow impurity consists of an atom which has one more valence electron (donor or n-type impurity) or one less valence electron (acceptor or p-type impurity) than the atom of the host semiconductor that would ordinarily occupy the lattice site. The result of this difference in valence for the case of the donor impurity is the introduction of an extra electron in addition to those used for tetrahedral bonding. If an acceptor atom is present, one of the four valence electrons for bonding is missing. Thus, in sili-

Figure 1.1: Impurity levels in silicon and gallium arsenide. (Primarily from Ref. 2.) CB and VB denote conduction band edge and valence band edge, respectively.

SILICON



GALLIUM ARSENIDE



con, a column IV material, elements from column III (e.g., boron, aluminum) form shallow acceptors, while column V elements (phosphorus, arsenic) act as shallow donors. In a compound semiconductor such as gallium arsenide, shallow impurities include zinc on a gallium site (acceptor) and sulfur on an arsenic site (donor). Since silicon has a valence between that of gallium and that of arsenic, the type of impurity depends on the lattice site on which the impurity atom lies: silicon on an arsenic site is an acceptor, while silicon on a gallium site is a donor.

An extra electron or a missing electron (hole) is coulombically bound to the impurity atom in a fashion similar to the binding of an electron to a proton in a hydrogen atom, with the primary difference that the impurity electron or hole is in a solid material which affects its motion. A modified hydrogen model can predict the energy levels E_n and the orbital Bohr radii a_n for these shallow impurities quite well:

$$E_n = \frac{m^*}{m_0 \epsilon^2 n^2} E_H; \tag{1.1}$$

$$a_n = \frac{m_0 \epsilon n^2}{m^*} a_H, \tag{1.2}$$

where m^* is the electron or hole effective mass, m_0 is the electron rest mass, ϵ is the relative dielectric constant of the semiconductor material, n designates the state, E_H is the hydrogen ground state energy (13.6 eV), and a_H is the hydrogen ground state Bohr radius (0.53 Å). The charge carriers have diffuse wavefunctions covering several tens of angstroms. Since the model is more accurate when the orbit size is large compared to the lattice spacing ($\sim$ 5Å), the energy level predictions are fairly reasonable for the carrier ground state

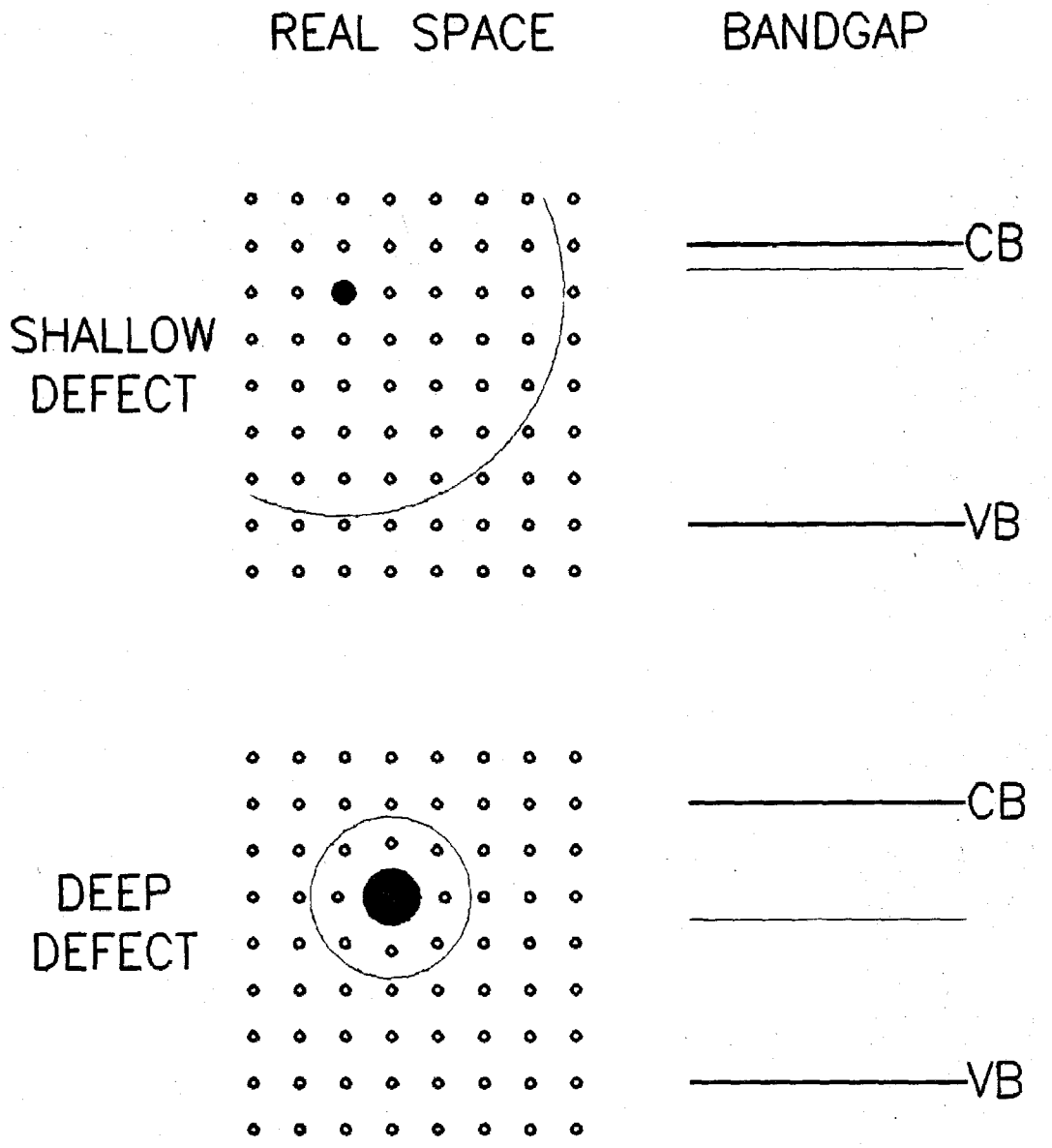
and very good for the excited states. The levels lie in the forbidden energy gap of the semiconductor. Donor states lie close to the conduction band edge and are composed of k-states from the conduction band minimum; acceptor states are close to the valence band edge and are composed of states from the valence band maximum. Because the wavefunctions are so diffuse in the crystal, these impurity levels are localized in k-space. The top portion of Fig. 1.2 shows a representation of a shallow impurity atom in a semiconductor lattice and the corresponding energy level in the bandgap. The level drawn is for a donor impurity.

1.2.2 Deep Level Defects

The other catagory of electronic semiconductor impurities, deep level defects, includes everything else. The physical configurations include substitutional defects, as in the case of shallow impurities, and interstitial defects. Self-interstitials, lattice vacancies, and defect complexes are also possible. These impurities and impurity complexes can have electronic energy levels which lie throughout the energy gap. Further, one impurity element can introduce more than one defect level in the bandgap.

Theoretical models for this group of defects are clearly less accessible than in the case of shallow impurities. Even in the simplest case of a single substitutional deep impurity, the hydrogenic model is not useful because the wavefunctions are too highly localized. Analysis is even more complicated for interstitial defects and defect complexes. However, several general trends are evident. The defect can bind carriers more strongly than a shallow level,

Figure 1.2: Descriptive diagrams showing shallow and deep defects in a crsytal lattice and their related energy levels in the bandgap of the semiconductor. The defects are filled circles in the real space drawings; carrier orbitals are indicated by light lines. CB and VB denote conduction band edge and valence band edge, respectively.


REAL SPACE
BANDGAP
SHALLOW DEFECT
CB
VB
DEEP DEFECT
CB
VB

so the energy level of the defect may be located closer to midgap. Since the orbital of an electron or hole bound to a deep level defect is smaller than that of a less tightly bound carrier orbiting a shallow impurity, the extent of the level in *k*-space is correspondingly greater. Thus, a single extremum is not sufficient for a theoretical description of a deep level defect. The bottom portion of Fig. 1.2 shows a schematic representation of these features.

1.2.3 Characteristics of Shallow and Deep Levels

The two types of impurities have several general characteristics which distinguish them and determine their different roles in semiconductor devices. Since shallow impurities reside on substitutional sites and form several bonds to neighboring atoms, they do not diffuse very easily — diffusion coefficients at 1200 °C are in the range of $10^{-11} - 10^{-12}$ cm^2 s^{-1}. Correspondingly, their solid solubilities can be as high as 10^{20} cm^{-3}, or a few at. %. Deep level impurities, on the other hand, can have diffusion coefficients at 1200 °C as much as six orders of magnitude higher than shallow species, with solid solubilities between 10^{15} and 10^{18} cm^{-3}. Even deep impurities which reside in substitutional sites may move through the lattice via interstitial sites; thus, these higher diffusivities (and related lower solubilities) are the result of transport of impurities from one interstitial site to another.

Essentially all the shallow impurities in a semiconductor are ionized at the typical device temperatures (around room temperature), so their contribution to the free carrier concentration in the semiconductor can be approximated to be the same as the concentration of impurity atoms. If there are

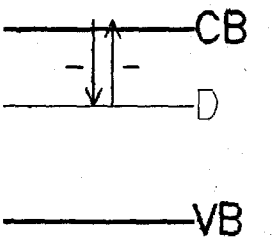
both donors and acceptors in the material, the number of free carriers can be approximated to be $|N_a - N_d|$, where N_a is the number of acceptors and N_d is the number of donors. The material will be p-type or n-type depending on which type of impurity is more numerous. The effect of a deep defect on the free carrier concentration depends not only on the defect concentration, but also on the activation energy (or position in the bandgap) of the deep level, its electron and hole capture cross sections, the shallow dopant type and concentration, and the temperature. Various deep levels may act as charge traps, recombination centers, or generation centers. These processes are illustrated in Fig. 1.3. For example, after a defect level captures an electron from the conduction band, two events are possible. The electron may be re-excited to the conduction band or it may drop to the valence band. The second process is equivalent to the level trapping a hole which annihilates the trapped electron. If re-excitation to the conduction band is more probable, the level is termed a trap; however, if the probability of dropping to the valence band is greater, it is called a recombination center. Conversely, if a defect is in a region with no free carriers, an electron may be excited from the valence band to the defect level and then to the conduction band. This process may be viewed as the emission of a hole and an electron from the defect level. In this case, the defect is referred to as a generation center.

1.2.4 Effects on Devices

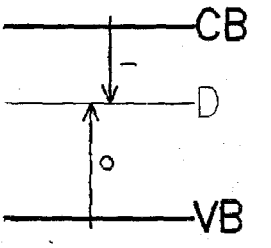
Shallow level impurities are used almost exclusively to provide the necessary carriers, n- or p-type, in semiconductor devices. However, several

Figure 1.3: A deep level defect acting as a charge trap, a recombination center, and a generation center. D designates the defect level. Hole transitions are denoted by circles, electron transitions by minus signs.

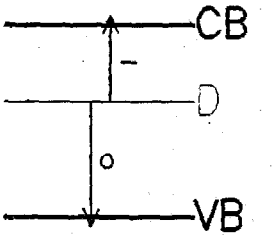
charge trap



recombination center



generation center



special cases exist in which deep level defects are also necessary for the operation of a device. For example, in fast switching junctions, deep level traps are used to kill free carrier lifetimes by pulling carriers out of the conduction or valence band. Deep levels are also used in gallium phosphide light-emitting diodes. Since GaP is an indirect semiconductor, transitions from the bottom of the conduction band to the top of the valence band are only possible with the addition of phonons, and therefore not as likely as a no-phonon process. Deep levels in the bandgap have large, overlapping extents in *k*-space, so level-to-level transitions are more probable. The light emitted by a GaP LED consists of photons emitted by this transition. A third example is the application of EL2, and to a lesser extent chromium, in making semi-insulating gallium arsenide for integrated circuit substrates. In this case, the deep defects pin the Fermi level near midgap. Nevertheless, deep level defects are undesirable in the vast majority of cases, since traps pose serious problems by eliminating free electrons and holes.

1.3 Deep Level Transient Spectroscopy

The primary tool used in the investigations discussed in this thesis was deep level transient spectroscopy (DLTS). This technique, which was developed about twelve years ago,[3,4] can be used to obtain information about traps in a depleted region of a semiconductor via the observation of carrier emission. This section contains general background and a description of the main features of DLTS; the Appendix has additional experimental details.

1.3.1 Depletion Width as Charge Transducer

DLTS measurements hinge on the use of the depletion width as a measure of the trapped charges in the region. Since almost all of the work in this thesis was performed on asymmetric p^+n junctions or Schottky barriers on n-type material, we will consider the n-type case here; analogous results are easily obtained for n^+p junctions or Schottky barriers on p-type material.

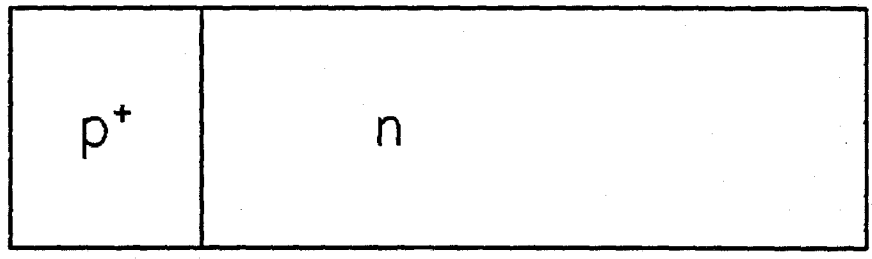
An asymmetric p^+n junction and the space charge in its depletion region are shown in Fig. 1.4. The depletion width W under a reverse bias V is

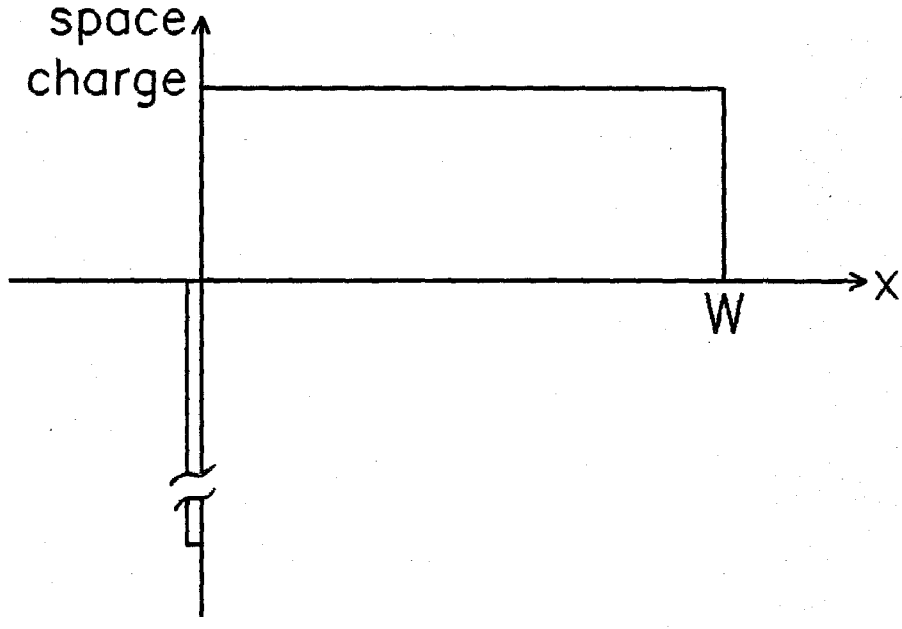
$$W = \sqrt{\frac{2\epsilon(V_{bi} + V)}{eN_+}}, \tag{1.3}$$

where ϵ is the dielectric constant of the material, V_{bi} is the built-in voltage (or barrier height in the Schottky case), e is the electronic charge, and N_+ is the shallow donor concentration in the n-type region. The corresponding junction capacitance C is given by

$$C = \frac{\epsilon A}{W}, \tag{1.4}$$

Figure 1.4: Space charge in the depletion region of an abrupt p^+n junction. The region extends much further on the n-type side since the density of donors there is so much less than the density of acceptors on the p^+ side. The distance from the junction is x.


p+
n


space
charge
W
x

A being the diode area. If we add at x $(0 < x < W)$ a small density $n(x)$ of fixed negative charges in a region of width Δx, the depletion region will expand slightly, thereby uncovering more ionized donors — fixed positive charges — to compensate for the negative charges and maintain charge neutrality. The junction capacitance will drop by an amount ΔC. It can be shown that this change is given by

$$\frac{\Delta C}{C} = -\frac{n(x)}{N_+ W^2} x \Delta x. \tag{1.5}$$

Thus, the capacitance change is proportional to the number of charges. Since it is also proportional to x, the change is smaller for charges introduced closer to the junction.

If we now assume that these fixed charges are actually carriers trapped by a defect level in the depletion region, we can relate the capacitance change to the number of traps (assuming all the traps in the region are filled). Integrating the expression for ΔC from $x = 0$ to $x = W$ yields

$$\frac{\Delta C}{C} = -\frac{N}{2N_+}. \tag{1.6}$$

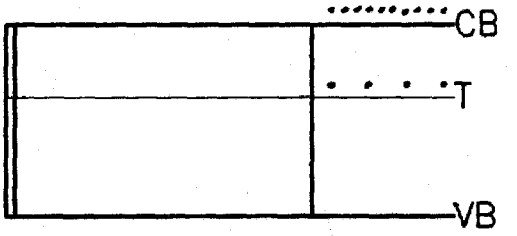
Here, N is the number of negative charge traps. We have assumed that the concentration of traps is uniform across the depletion region. This result means that if all the traps in the depletion region are filled, the relative change in the capacitance is proportional to the trap density in the depletion region. Thus, the depletion width, monitored via the junction capacitance, can be used to get information about charge traps.

1.3.2 Capacitance Transients

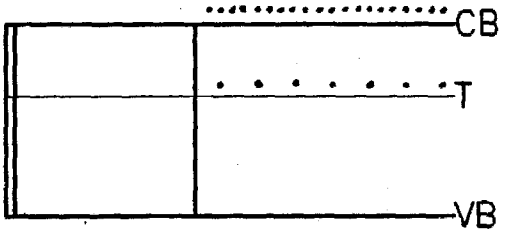
At a temperature T, the thermally activated release of carriers by a trap will occur at a rate proportional to $\exp(-E_a/k_BT)$, where E_a is the activation energy of the trap, and k_B is Boltzmann's constant. Thus, if we fill a trap in the depletion region and allow it to empty, the depletion width and junction capacitance will relax approximately exponentially back to their respective quiescent values. The most common technique for filling the traps is reducing the reverse bias for a time long enough for the traps to capture carriers. The process is illustrated in Fig. 1.5. First, we apply a reverse bias to the junction and wait until steady state has been reached. At this time, all traps in the depletion region are empty. We now apply a reduced bias pulse to the junction. Electron traps in the portion of the original depleted region which is now normal capture electrons from the conduction band. After the pulse, the bias is the same as that at the beginning of the process. However, the depletion width is slightly larger to compensate for all the electrons fixed to the traps in the region. As these electrons are thermally released, they are swept out of the region very quickly, so they are not available for re-trapping. The depletion width returns to its quiescent value as the traps are emptied. The junction capacitance is inversely proportional to the width; it therefore decreases after the pulse and rises back to the quiescent level.

This discussion applies for the case of trapped electrons. If we instead fill hole traps in the depletion region by some technique, the depletion width will decrease to compensate for the positive charges. The capacitance transient

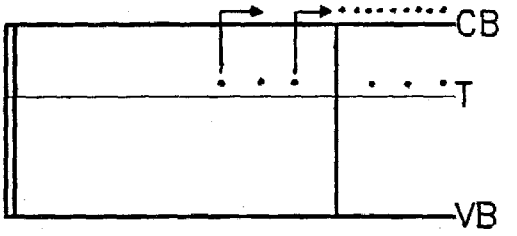
Figure 1.5: A capacitance transient from a deep level in an n-type depletion region. T designates the trap level. During the pulse, both the width W and the capacitance C are off scale.



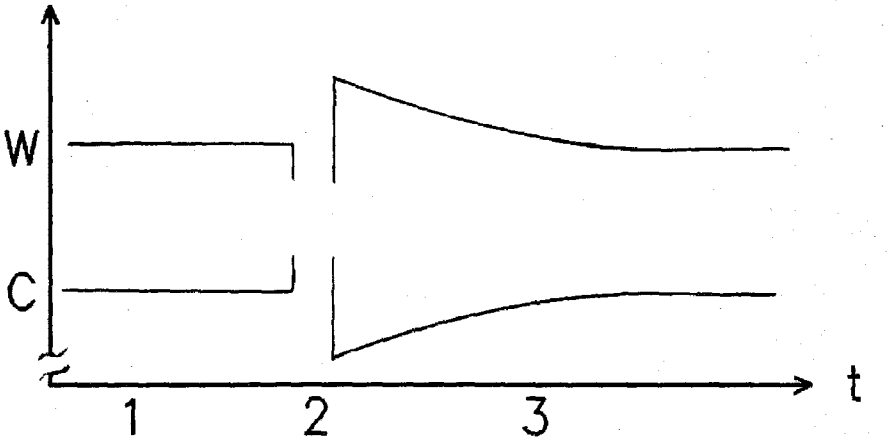
1
quiescent
reverse bias



2
capture during
pulse



3
thermal release



will then be positive. Thus, the sign of the transient is negative for an electron trap and positive for a hole trap. In general, the sign of the transient is *negative* for a *majority* carrier trap and *positive* for a *minority* carrier trap, regardless of whether the material is n- or p-type.

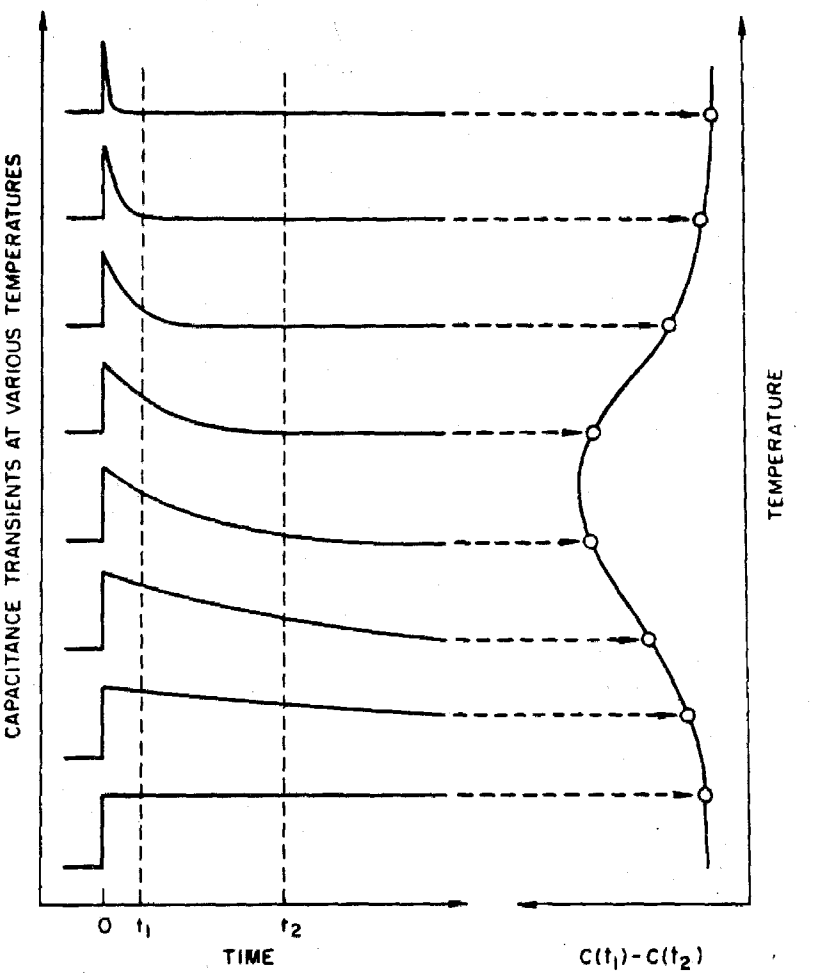
Free minority carriers may be introduced by forward biasing the junction if the sample used is a p-n diode. However, if a Schottky barrier is used, forward biasing will not provide these carriers. In this case the sample is often illuminated with photons of energy greater than the semiconductor bandgap to create free electrons and holes.

If we apply a train of pulses to the junction, a series of capacitance transients will result. By varying the sample temperature, we can then produce a number of transients which have different decay time constants — from essentially infinite at very low temperature to essentially zero at very high temperature. A DLTS spectrum is produced by analyzing such a train of transients.

1.3.3 DLTS Rate Window

The most common technique used for the analysis of these transients is the rate window. As the temperature is scanned, the rate window generates an output — the DLTS signal S — which peaks when the input transient rate matches the selected rate. A straightforward implementation of this method involves sampling each transient at times t_1 and t_2 and subtracting the sampled values. Figure 1.6 shows how this sampling technique produces a peak from a group of transients with different rates. At low temperature,

Figure 1.6: Capacitance transients sampled at t_1 and t_2 to produce a peak. (From Ref. 3.)


CAPACITANCE TRANSIENTS AT VARIOUS TEMPERATURES
TEMPERATURE
0
t_1
t_2
TIME
$C(t_1)-C(t_2)$

the transient decays very slowly, so its magnitude is essentially the same at t_1 and at t_2. At high temperature, the decay occurs so quickly that the signal is at its quiescent value before t_1, and again, the difference in magnitude of the signal at the two times is approximately zero. The difference in magnitude at t_1 and t_2 will go through a maximum at an intermediate temperature, when the signal is still large at t_1 but close to its quiescent value at t_2. The transient time constant τ that corresponds to the peak is determined by t_1 and t_2:

$$\tau = \frac{t_1 - t_2}{\ln(t_1/t_2)}. \tag{1.7}$$

Thus, we can select various rates by selecting different values of t_1 and t_2.

The DLTS signal is then

$$S = C(t_1) - C(t_2). \tag{1.8}$$

Note that S has the same sign as the transients themselves, since $C(t_1) > C(t_2)$ for a positive transient and $C(t_1) < C(t_2)$ for a negative transient. The sign of the DLTS signal is therefore determined by the type of trap observed: a majority carrier trap produces a negative signal, while a minority carrier trap produces a positive signal.

The discussion so far has assumed that we have only one deep level in the sample. However, the previous analyses also hold for the case of several traps in the sample, provided that they have sufficiently different activation energies. The capacitance transient is then a superposition of transients for the individual traps. The double-sampling scheme for analysis generates peaks at different temperatures, one for each deep level.

Thus, a DLTS spectrum is produced by *a*) applying a train of trap-filling pulses to the reverse-biased junction, *b*) scanning temperature, *c*) measuring the junction capacitance transients, *d*) analyzing the transients with a rate window, and *e*) plotting the rate window output (the DLTS signal S) as a function of the sample temperature.

1.3.4 Obtaining Trap Information from DLTS Spectra

A good deal of information about the deep level can be extracted from DLTS spectra. Here, we describe the most common measurements made.

In Sec. 1.3.1, we showed that the change in capacitance ΔC is proportional to N, the number of traps, if all the traps in the depletion region are filled. By relating the DLTS peak height to ΔC, we can obtain a simple formula to compute the trap concentration from a spectrum. For a transient of amplitude ΔC, the double-sampled peak amplitude S_{peak} is given by

$$S_{peak} = \Delta C\left(e^{-t_1/\tau} - e^{-t_2/\tau}\right), \tag{1.9}$$

where τ is as defined in Eq. 1.6. Combining Eqs. (1.6) and (1.9) yields

$$N = -\frac{2N_+}{C\left(e^{-t_1/\tau} - e^{-t_2/\tau}\right)} S_{peak}. \tag{1.10}$$

As before, C is the capacitance at the quiescent reverse bias and N_+ in the concentration of shallow donors in the n-type region. Thus, for fixed t_1 and t_2, the number of traps is proportional to the peak amplitude.

In addition to providing a convenient method for monitoring the occupation of charge traps, the depletion region affords another handy feature.

Since the depletion width is easily adjusted by varying the applied reverse bias, we can choose the portion of the material that we would like to probe. We can generate spectra at various quiescent biases using small filling pulses. Analysis of the peaks produced yields the trap concentration at the various distances from the interface. Alternatively, we can fix the reverse bias and take spectra with different filling-pulse amplitudes. The differences in peak amplitudes can then be used to calculate the trap concentration as a function of the distance from the junction x.

The activation energy E_a can be measured by taking spectra at a number of different rate settings. The peak will shift to higher temperature as the selected rate is increased. The transient rate α at any given temperature is given by[3]

$$\alpha = \frac{\sigma_n \overline{v}_n N_c}{g} \exp(-E_a/k_B T), \tag{1.9}$$

where σ_n is the trap capture cross section, $\overline{v}_n$ is the average electron thermal velocity, N_c is the effective density of states at the conduction band edge, and g is the degeneracy of the level. The exponential prefactor has a T^2 temperature dependence (if the capture cross section is temperature independent), so E_a can be found by plotting the logarithm of α/T^2 versus the inverse of the temperature. The values of α are the rates selected by t_1 and t_2 ($\alpha = 1/\tau$), and the temperatures are those at which the peak occurs for each selected rate. The slope of the line in this Arrhenius plot is then $-E_a/k_B$.

This activation energy is a well-defined property of the particular trap

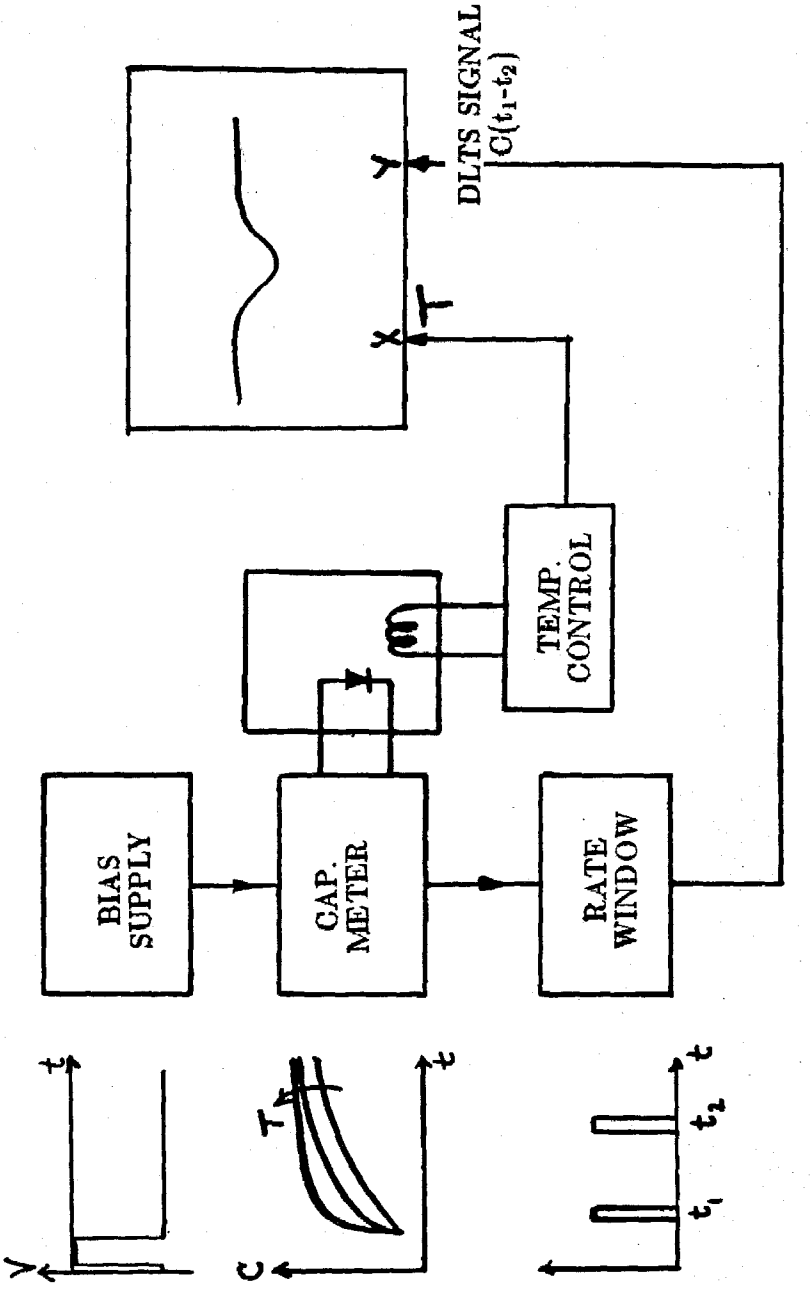
in question — it is the activation energy for thermally stimulated emission of charge carriers by the defect in a depletion region. As such, it is an excellent way of identifying the defect. However, the relationship between this energy and the position of the defect level in the bandgap is not so clear. In addition to the T^2 factor mentioned above, the exponential prefactor may have a temperature-dependent contribution from the capture cross section σ_n. This is the result of thermally-activated capture processes. Further, the measured level of the energy is that for a trap in a region of high electric field, since depletion region fields are of the order of 10^4 V cm^{-1}. This field may significantly alter the energy required to escape from the trap.

The primary measurements made by DLTS, then, are as follows: *a*) the activation energy is measured by varying the rate window; *b*) the average trap concentration is calculated from the peak height when the filling pulse is large enough to fill traps throughout the depletion region; and *c*) the spatial profile of the trap concentration is obtained by varying the reverse bias or the filling-pulse amplitude to probe different parts of the material.

1.3.5 Experimental Setup

A block diagram of the experimental setup for DLTS is shown in Fig. 1.7. The sample diode is mounted in a variable-temperature system. The pulsed bias voltage is applied to it, and the capacitance is measured across its terminals. The capacitance transients are fed into a rate window for analysis as the temperature is varied. The rate window output is plotted as a function of the sample temperature. For the DLTS measurements reported

Figure 1.7: Schematic experimental setup for DLTS.


DLTS SIGNAL
C(t1-t2)
Y
X
T
TEMP.
CONTROL
BIAS
SUPPLY
CAP.
METER
RATE
WINDOW
t
Y
T
C
t
t1
t2
t

in this thesis, a one-megahertz Boonton Model 72BD capacitance meter was used in most cases; a few of the measurements required the high speed response afforded by a home-made 20-MHz capacitance bridge (see Appendix for details). A PAR Model 162 double boxcar integrator served as the rate window. The temperature was measured by a copper-constantan (type T) thermocouple. The boxcar output and thermocouple voltage were read by a Hewlett-Packard desktop computer (either a Model 9825A or a Model 85) which converted the thermocouple voltages to temperatures, recorded data points approximately half a degree apart, plotted the data, and, upon completion of the spectrum, transferred the points to a PDP-11/34 computer for storage and analysis.

1.3.6 Guidelines for the Application of DLTS

DLTS as an experimental technique offers access to a number of trap parameters, including emission activation energy and trap concentrations, which are not easily obtained by other methods. However, there are several factors which limit its applicability in the investigation of semiconductor defect properties. In particular, DLTS data do not provide any information about the physical structure of a defect directly, thereby making accurate correlation between a defect and its level difficult. Also, DLTS parameters are difficult to compare to those obtained from other techniques. One problem is deducing the defect level from the measured value of the activation energy, as pointed out in Sec. 1.3.4. Another is that DLTS measures the number of electrically active traps, which may or may not be the actual

number of impurity atoms in the material. Comparing DLTS concentrations to the total number of impurity atoms measured by a technique such as Rutherford backscattering spectrometry is not straightforward.

The criteria for determining the applicability of the technique to any material or structure may be summarized as follows: *a*) A DLTS measurement of a material requires a p-n junction, Schottky barrier, or some other structure that allows the user to change the size of the depletion region by changing the applied bias. *b*) The experimental tools described in Sec. 1.3.5 are needed. *c*) The primary information obtained will be the activation energies and concentrations of the electrically active majority carrier traps in the depletion region. Minority carrier information may also be obtained, but requires additional equipment in the case of Schottky barrier samples.

1.4 Summary of Results of Thesis

Chapter 2:

Section 2.4: Platinum-on-silicon structures annealed at temperatures from 300 to 800 °C were characterized using Rutherford backscattering spectrometry (RBS), secondary ion mass spectrometry (SIMS), current-voltage (I-V) and capacitance-voltage (C-V) measurements, and DLTS.

RBS spectra indicated the presence of Pt_2Si at the surface of the 300 °C sample and PtSi for the higher temperature samples. They also showed tails at the low-energy end of the platinum signal in samples treated above 600 °C, indicating some intermixing or the formation of islands on the surface.

DLTS spectra exhibited no traps in samples treated below 700 °C. Platinum electron traps of activation energy 0.22 eV were observed in the 700 °C sample at a concentration of $\sim 10^{11}$ cm^{-3}. The concentration of the traps ranged from $0.5 - 2 \times 10^{13}$ cm^{-3} in the region from 7 to 0.5 μm from the interface in the sample treated at 750 °C for 30 min. The concentration range was $0.3 - 1.8 \times 10^{14}$ cm^{-3} for the samples annealed at 800 °C.

Section 2.5: Palladium- and nickel-on-silicon structures annealed at temperatures from 300 to 800 °C were characterized using RBS, DLTS, and, in some cases, I-V and C-V measurements.

RBS spectra indicated surface silicide compositions of Pd_2Si for all palladium samples and Ni_2Si (300 °C), NiSi (400–700 °C), and $NiSi_2$ (800 °C) for the various nickel samples. RBS also showed degradation of the silicide layers in all samples treated above 600 °C.

Only samples treated below 700 °C for palladium and 500 °C for nickel had sufficiently low reverse leakage currents for DLTS measurements. Of all these samples, DLTS showed traps above the detection limit of $\sim 10^{11}$ cm^{-3} only in the palladium sample treated at 700 °C. In that case, the DLTS spectrum exhibited a peak at a temperature consistent with that expected for a palladium electron trap at a concentration of a few times 10^{11} cm^{-3}. Samples were also prepared for DLTS by removing the top 5–10 μm layer of the palladium and nickel structures that had been annealed at 800 °C. DLTS probes of this region — 5 to 10 μm from the original interface — showed no traps in the nickel case. The spectrum for the palladium sample had three peaks, each of which corresponded to trap concentrations below 5×10^{11} cm^{-3}.

Section 2.6: Cobalt-on-silicon structures annealed at temperatures from 300 to 800 °C were characterized using RBS and DLTS. RBS indicated no silicide formation for the 300 and 400 °C samples; CoSi (500 °C) and $CoSi_2$ (600–800 °C) were seen in the spectra of the higher temperature samples. DLTS showed no traps in the samples annealed at or above 500 °C; however, a trap of concentration $\sim 10^{12}$ cm^{-3} was detected in the 400 °C sample.

Chromium-on-silicon samples which were annealed at temperatures from 300–800 °C were characterized by DLTS. Although reverse leakage currents were sufficiently low for DLTS measurements in all of these samples, no traps were detected.

Erbium silicide-silicon samples which were grown by annealing at 380 °C

for 50 min in vacuum or forming gas were characterized by DLTS. No traps were detected in either case.

Summary: These results indicate several conclusions: *a*) The maximum safe temperature (below which indiffusion is negligible) for platinum or palladium silicide on silicon is 700 °C; for nickel silicide on silicon, this temperature is only 500 °C. *b*) Cobalt indiffusion into silicon may be occurring prior to the formation of a silicide layer at the surface, but there is no evidence for contamination after the silicide has been formed or at high temperature. *c*) Chromium silicide-silicon structures exhibit no degradation or indiffusion of traps up to an annealing temperature of 800 °C. *d*) Erbium silicide-silicon samples show no indication of indiffused traps at 380 °C regardless of the annealing ambient. These investigations represent the first collection of deep level indiffusion studies of transition metal silicides on silicon.

Chapter 3:

DLTS measurements were carried out on p-n junctions made of four compositions of $In_{1-x}Ga_xAs_yP_{1-y}$. These samples, with bandgaps of 0.75, 0.83, 0.95, and 1.1 eV, covered the range of compositions that are lattice-matched to InP. Except in one case, DLTS spectra exhibited no traps above the detection limit of $\sim 5 \times 10^{13}$ cm^{-3}. The trap that was detected in one sample was attributed to a substrate lattice defect. These studies were the first attempt to investigate deep levels in this quaternary alloy.

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CHAPTER 2

CHARACTERIZATIONS OF THE DEGRADATION OF TRANSITION METAL SILICIDE – SILICON STRUCTURES

2.1 Introduction

In this chapter, we discuss the results of a collection of measurements on structures consisting of a thin film transition metal silicide on a substrate of silicon. The primary techniques used were deep level transient spectroscopy, Rutherford backscattering spectrometry, and capacitance-voltage and current-voltage measurements. We investigated platinum, palladium, and nickel silicides in detail. We also looked briefly at silicides of cobalt, chromium, and erbium.

2.1.1 Applications of Transition Metal Silicides

Transition metal silicides are playing a part in today's semiconductor technology by fulfilling requirements which cannot be met by other materials.[1–3] A great deal of attention has been given to the use of silicides in integrated circuits. A handful of silicides are also being investigated for their use in long-wavelength infrared detectors.

The heart of progress in silicon integrated circuitry in its several years has been the reduction of device size and the increase in packing densities. Present chips can have devices with dimensions in the 1–2 μm range and as many as several tens of thousands of circuits on a chip which has an area of only a square centimeter. This push to higher and higher levels of integration has been stimulated by the higher speed and lower power dissipation associated with smaller devices. Additionally, manufacturing volume can be maximized while costs are minimized.

One part of the effort to advance the level of integration in semiconductor chips is the introduction of new materials. An example is the case of materials for gates and interconnections. Polycrystalline silicon has been widely used in the past, but as device dimensions shrink to the submicron scale, the high resistivity and large grain size associated with this material begin to limit its applicability. The major requirements for a suitable material are: *a*) low resistivity, *b*) high-temperature processing compatibility, *c*) ability to withstand processing chemicals, and *d*) compatibility with present production technology. Several transition metal silicides (TMS's) can meet all these criteria. Their resistivities are typically on the order of 10 $\mu\Omega$ cm — quite comparable to metal resistivities. Melting temperatures are high, and unlike pure refractory metals, the oxide (SiO_2) formed on most TMS's is nonvolatile and compatible with the other parts of the device. TMS's are highly resistive to the common chemicals used during cleaning and processing. And, finally, these silicides fit conveniently into the present processing technology because they are silicon-based. In fact, TMS's are typically formed by a solid phase reaction between a pure metal layer and the silicon on which it is deposited. Thus, TMS's are now being used as gates and interconnects in recent chips.[4]

Another technology which may take advantage of the special properties of silicides is infrared detection. While several groups are pursuing relatively new material systems such as mercury telluride/cadmium telluride for band-to-band photodetection, others are investigating the possibility of using low-barrier Schottky detectors on silicon. HgCdTe detectors offer several

advantages over the Schottky barrier systems. The overriding advantage of the latter is that the materials difficulties of silicon are largely solved, while II-VI materials are still viewed as problematic virgin territory.

The operation of a Schottky barrier photodetector is based on the photoexcitation of a carrier over the barrier. Thus, the longest wavelength detectable is that with an energy equal to the barrier height. Since the region of interesting wavelengths is 3–5 μm, the detector barrier height must be $\sim$ 0.25 eV. Transition metal silicides offer a wide range of barrier heights on silicon. Of particular interest are platinum and palladium silicides, which have barrier heights of 0.23–0.34 eV on p-type silicon, and erbium silicide, with a barrier of 0.39 eV on n-type silicon. Platinum silicide-silicon Schottky barriers have been demonstrated as excellent detectors in the 1.2–4.7 μm wavelength region.[5]

2.1.2 Goal of Our Investigations

As described in Chap. 1, the majority of transition metals form one or more deep level defects in silicon. Gold is commonly used to kill carrier lifetimes in devices, and platinum has been investigated for this application also.[6] Clearly, any indiffusion of transition metals from the silicide layer in a device during annealing stages of the processing could alter the underlying silicon. A knowledge of the effects of annealing on the metal diffusion into silicon is therefore important in considering any silicide for use in a device.

However, the standard techniques presently used to study silicide-silicon structures cannot provide the sensitivity required to detect the small quan-

tity of transition metal contaminants which can poison the underlying silicon ($> 10^{11}$ cm^{-3}). The most common of these is Rutherford backscattering spectrometry (RBS), which is widely used to determine silicide composition. RBS has a sensitivity of ~ 0.1 at.% and is therefore not very useful for observing minute concentrations. Auger electron spectroscopy (AES) has an advantage over RBS in that it provides excellent lateral resolution, but its atomic sensitivity is approximately the same. Secondary ion mass spectrometry (SIMS) at its best can detect 1 ppm or $\sim 5 \times 10^{16}$ cm^{-3} in silicon, but it requires a calibration sample for the extraction of absolute numbers. The removal of the silicide layer is also necessary — a nontrivial process for most silicides, since they tend to be highly resistive to all etches except those which also consume the underlying silicon.

Deep level transient spectroscopy (DLTS) is a technique ideally suited for this application. This method can detect traps in the depletion region of the Schottky barrier, as opposed to the previously mentioned techniques, which measure atoms near the surface. Thus, DLTS gives a *direct* measure of the number of centers affecting the free carrier concentration. Its sensitivity is $10^{-3} - 10^{-4}$ times the shallow dopant concentration, so it is possible to detect in the interesting concentration range. In addition, DLTS can probe as far as several microns away from the interface, while the beam techniques are not useful more than about 0.3 μm from the surface.

The purpose of the investigations discussed in this chapter was to use DLTS to search for deep levels in the depletion regions of silicide-silicon samples annealed at various temperatures. We were thus able to simulate

the high-temperature processing steps which occur in the fabrication of an integrated circuit and determine the effects of indiffusion of the transition metal.

2.2 Measurements Used to Study Silicide Silicon Structures

Deep level transient spectroscopy (DLTS) and Rutherford backscattering spectrometry (RBS) were the primary techniques used to investigate the silicide-silicon structures. Characterizations of the Schottky barrier diodes used in the DLTS studies were carried out by current-voltage (I-V) and capacitance-voltage (C-V) measurements.[7]

DLTS observed traps in the depletion region of the reverse-biased Schottky barrier formed by the silicide-silicon structure, in our case, $\sim 0.5 - 7\ \mu m$ from the interface. For our samples, trap concentrations above $5 \times 10^{11}/cm^3$ could be detected by DLTS. RBS detects atom impurity concentrations greater than about 0.1 at.% (5×10^{19} atoms/cm^3 in silicon) within $\sim 0.3\ \mu m$ of the interface of the structures. It is important to note that the two techniques measure what are probably physically different configurations of platinum impurities, since RBS measures total atomic concentration and DLTS measures only the electron traps.

2.2.1 Rutherford Backscattering Spectrometry

An overview of the DLTS measurement was given in Chap. 1 of this thesis. Here, we provide a brief summary of the features of RBS which pertain to our measurements.

RBS is executed as follows:[8] a high-energy, monoenergetic beam of light ions (e.g., $^4He^+$) impinges on a sample perpendicular to the surface. The ions are scattered by the atoms of the sample — some backwards, out of

the sample, and others forward into the material. Ions backscattered at a fixed angle, typically 170° from the incident beam, are detected. An RBS spectrum is a plot of the number of ions as a function of their backscattered energy. Figure 2.1 shows the experimental setup.

Deducing qualitative information about the sample from the spectrum is quite simple; quantitative results require some analysis but are also straightforward. Since almost all of the RBS spectra to be discussed in this thesis are for silicon substrates with thin film overlayers of a mixture of silicon and a metal, we describe here a generic spectrum of this sort. Figure 2.2 is a representation of such a spectrum. M is a transition metal much heavier than silicon. The thin film overlayer has equal numbers of M and Si atoms. The spectrum has been taken with 2 MeV $^4He^+$ ions impinging on the surface and with the detector at 170°.

The following intuitive guidelines form the basis for understanding this spectrum: *a*) Helium ions scattered by M atoms at the surface have energies closer to 2 MeV than ions scattered by silicon atoms at the surface because the mass of the M atoms is greater than that of the silicon atoms. These surface scattering energies are marked by arrows in Fig. 2.2. *b*) The energy of ions scattered by M (or Si) atoms at the surface is higher than the energy of ions scattered by M (Si) atoms deeper in the material. This effect is the result of the energy loss of the ions as they travel through the material. Thus, signal at energies just below the surface scattering energy for M (Si) corresponds to M (Si) atoms just below the surface. This feature enables us to measure the film thickness from the spectrum. In addition, if the surface

Figure 2.1: Diagram of an RBS setup. The pathway of the ions must be a vacuum to prevent scattering by atoms other than those in the sample. (From Ref. 8.)

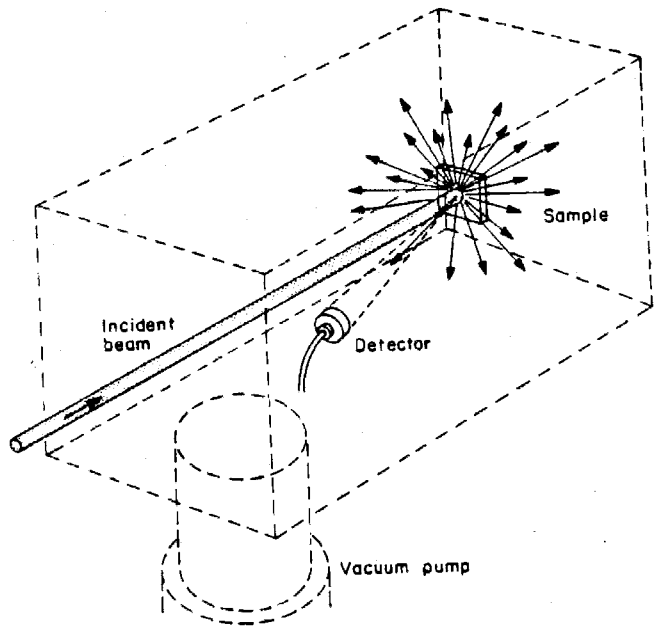
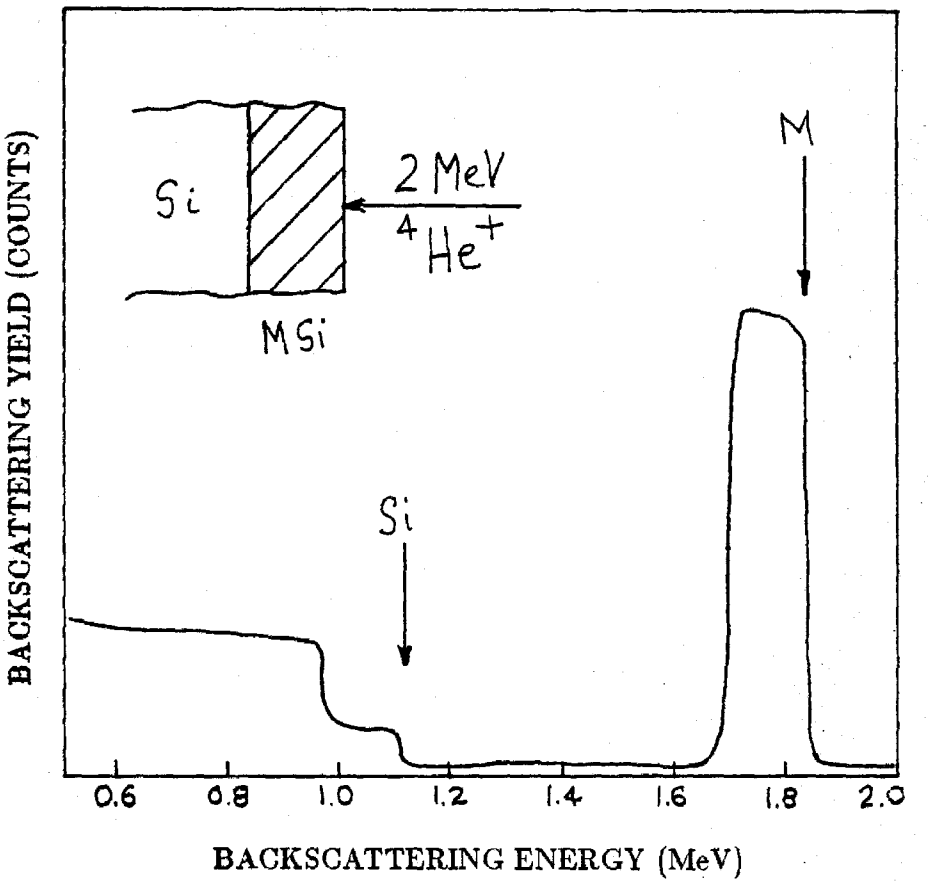

Sample
Incident
beam
Detector
Vacuum pump

Figure 2.2: Sample RBS spectrum. The inset shows the structure from which the spectrum is generated.


Si
2 MeV
4He+
MSi
M
Si
BACKSCATTERING YIELD (COUNTS)
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0
BACKSCATTERING ENERGY (MeV)

or interface of the sample is not smooth, the low-energy end of the metal signal and the step in the silicon signal will not be abrupt. *c*) The number of backscattered ions depends on the number of atoms present and their cross section for scattering. The silicon signal exhibits a step because the density of silicon atoms in the substrate is greater than that in the thin film. Also, while the thin film has equal numbers of M and Si atoms, the signal from the M atoms is greater because the larger M atoms scatter the ions more effectively. For samples in which the thin film composition is not known, it can be computed from the ratio of leading-edge signal heights.

The main items to be extracted from an RBS spectrum, then, are: *a*) the ratio of the number of metal atoms to the number of silicon atoms in the film; *b*) the thickness of the film; and *c*) the smoothness of the surface and interface. The chief limitations of RBS in our application were the short depth scale and low atomic sensitivity, which did not allow for reasonable comparisons between the DLTS and RBS diffusion data. Also, the lack of lateral resolution made it impossible to determine whether the blurred low-energy signals were caused by intermixing of silicon amd metal atoms at the interface or surface irregularities. Thus, in the discussions that follow, RBS was used primarily as a tool to determine the composition of the silicide and check for gross degradation.

2.3 Sample Preparation

The silicon substrates used to fabricate samples for these studies were 7-10 Ω cm n-type (100) silicon wafers from Wacker. Wafers were ultrasonically cleaned in organic solvents and then subjected to a standard chemical cleaning procedure in which the final step was etching in an HF solution. They were then immediately loaded into an ion-pumped vacuum system, where a thin (~ 500 Å) metal film was electron-beam deposited at a pressure less than 3×10^{-7} Torr. During the evaporation, a portion of each wafer was covered by a mechanical mask with 0.75-mm-diam holes to make diodes for the electrical measurements.

The wafers were diced, and pieces with broad-area metal coverage were annealed with diodes in a vacuum furnace at pressures below 10^{-6} Torr at temperatures from 300 to 800 °C. Ohmic contacts to the diodes were made by rubbing In-Ga onto the backs of the substrates. Diodes used for DLTS studies were mounted on headers and wire-bonded. The samples with broad-area silicide coverage were used for the backscattering analysis. Further, in some cases in which DLTS measurements could not be made on the silicide-silicon structure due to the degradation of the Schottky barrier, a corresponding broad-area piece was etched in $3HNO_3$:$1CH_3COOH$:0.4HF to remove a 5-10 μm layer. Gold dots were then evaporated onto the freshly exposed silicon, and these diodes were prepared as above for DLTS measurements.

2.4 Results for Platinum Silicides

We observed platinum diffusion into the silicon underlying various PtSi films. Silicon substrates covered with platinum films were annealed at temperatures from 300 °C to 800 °C for times between 30 and 180 minutes to form the silicide. RBS spectra showed no degradation of the silicide in the samples treated below 700 °C. DLTS electron trap concentrations in samples treated below 700 °C were below the DLTS detection limit of 5×10^{11} cm^{-3}. Trap concentration profiles revealed $\sim 5 \times 10^{11}$ to $\sim 10^{14}$ traps cm^{-3} in samples annealed between 700 and 800 °C.

2.4.1 RBS Measurements

Backscattering spectrometry using 2-MeV $^4He^+$ ions was carried out on these samples. Figure 2.3 shows three of the resulting spectra. Analysis of the spectra using the ratio of the Pt signal leading-edge height to the Si signal leading-edge height yields compositions consistent with Pt_2Si for the 300 °C sample and PtSi for all higher temperature samples. The film thickness for each of the PtSi samples is approximately 1000 Å. The solid line in Fig. 2.3 shows the spectrum for the PtSi sample which was annealed at 600 °C for 30 minutes. This and all samples treated at lower temperatures exhibit Pt signals which fall off sharply on the low energy end, indicating abrupt silicide-silicon interfaces and smooth silicide surfaces. These Pt signals fall off as sharply as do Pt signals in the case of unannealed samples (Pt on Si).

Samples annealed at 700 °C and at 750 °C (not shown in the figure)

Figure 2.3: RBS spectra for PtSi-Si structures plotted on a semilog scale. These spectra were taken with the beam of 2-MeV $^4He^+$ ions incident normal to the sample and with the detector at a scattering angle of 170°.

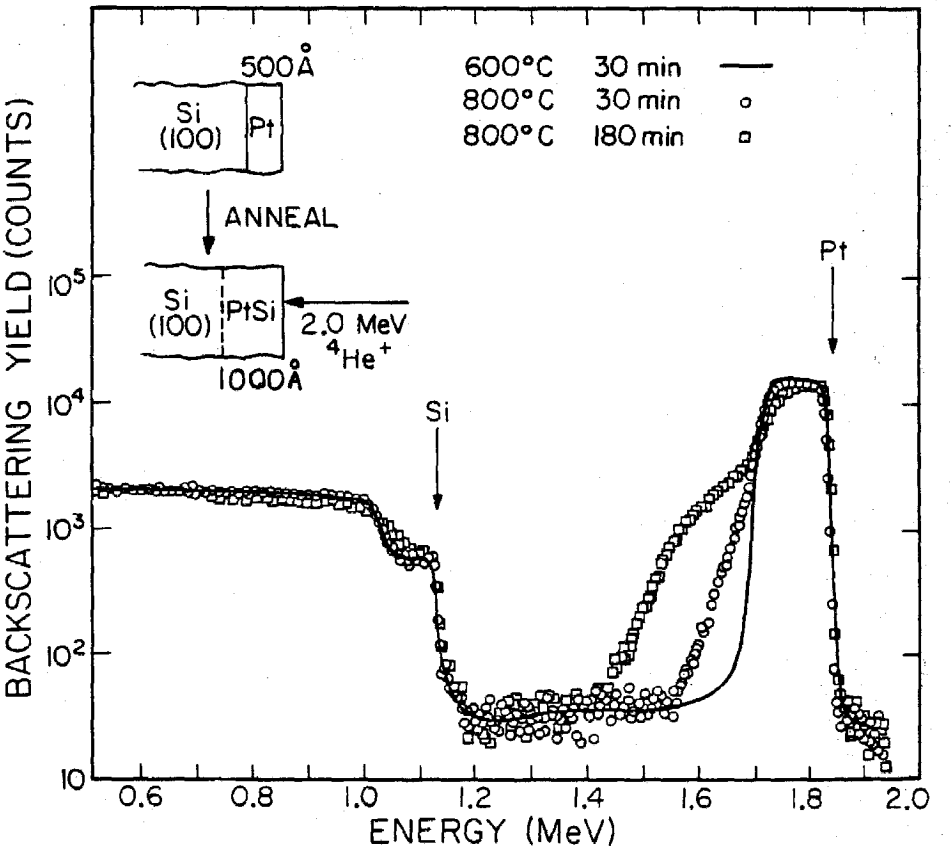
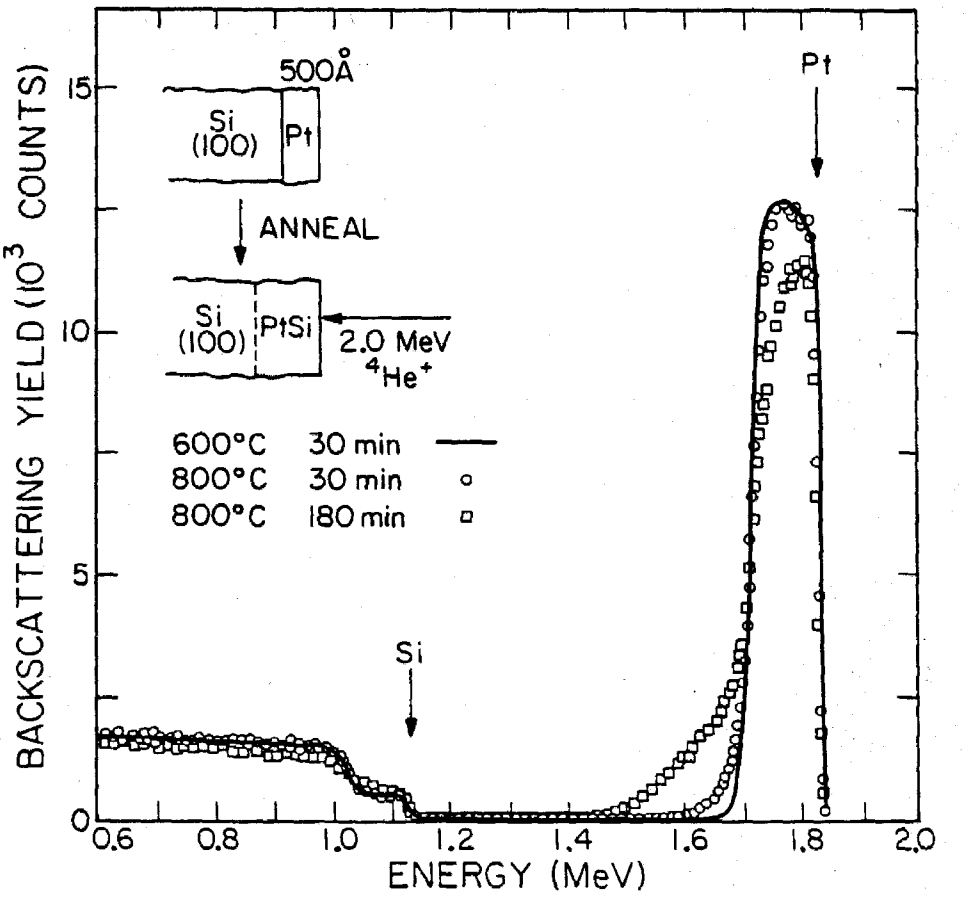

500Å
Si
(100)
Pt
ANNEAL
Si
(100)
PtSi
1000Å
2.0 MeV
4He+
600°C 30 min
800°C 30 min
800°C 180 min
Pt
Si
BACKSCATTERING YIELD (COUNTS)
10
10²
10³
10⁴
10⁵
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0
ENERGY (MeV)

exhibit very small tails at the low energy end of the Pt signal. However, a significant platinum tail is seen in the 800 °C samples. Inspection of the surface with a low-power optical microscope reveals a smooth topology, but SEM images reveal features approximately one micron wide. Thus the tail could correspond to a nonabrupt interface between the silicide layer and the substrate, or it could be a result of the surface roughness. The circles in Fig. 2.3 show the RBS spectrum for PtSi annealed at 800 °C for 30 minutes. The tail at the low energy end of the Pt signal for this case is almost a straight line on this semilog plot. If we assume that it results from a nonabrupt interface, the slope of the tail corresponds to a decrease in the Pt atomic concentration of approximately one order of magnitude for every 0.2 μm from the interface, with a Pt concentration of $\sim$ 3% at a distance of 500 Å from the interface. The squares in the figure represent the spectrum for the sample treated at 800 °C for 180 minutes. In this final case, the low energy end of the platinum signal exhibits a large tail which is not a straight line. Here, the onset of the disintegration of the PtSi film is evident, as the number of counts at the peak of the platinum signal is approximately ten percent less than in the samples which were treated for a shorter time. This effect is seen more clearly in Fig. 2.4, where the spectrum is shown plotted on a linear scale.

To date, few attempts have been made to measure transition metal diffusion into silicon from a silicide at the surface using RBS. Ishiwara *et al.*[9] have reported the observation of platinum diffusion by backscattering spectrometry for PtSi on (100) and (111) oriented silicon wafers. Our RBS spectra for (100) wafers show significantly less motion of the platinum atoms

Figure 2.4: RBS spectra for PtSi-Si structures plotted on a linear scale. These data are the same as those in Fig. 2.3.


500Å
Si
(100)
Pt
ANNEAL
Si
(100)
PtSi
2.0 MeV
4He+
600°C 30 min
800°C 30 min
800°C 180 min
Pt
Si
BACKSCATTERING YIELD (10^3 COUNTS)
ENERGY (MeV)
0
5
10
15
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0

than theirs. In our sample which was annealed at 800 °C for 3 hours, we measure 22% platinum diffusion in contrast to 53% for a 2-hour 800 °C treatment reported by Ishiwara. Here, the percentage of diffused metal atoms is defined as the ratio of the area under the Pt tail to the total area under the Pt signal, and we have assumed as they did that the tails correspond to diffusion of platinum. Their samples were prepared in a manner very similar to ours, with the exception that their evaporations were carried out at pressures about an order of magnitude lower. The doping level in their substrates may also have been different, as the only information given about their substrates is the orientation. These differences may account for the disparity in the results.

2.4.2 Secondary Ion Mass Spectrometry Results

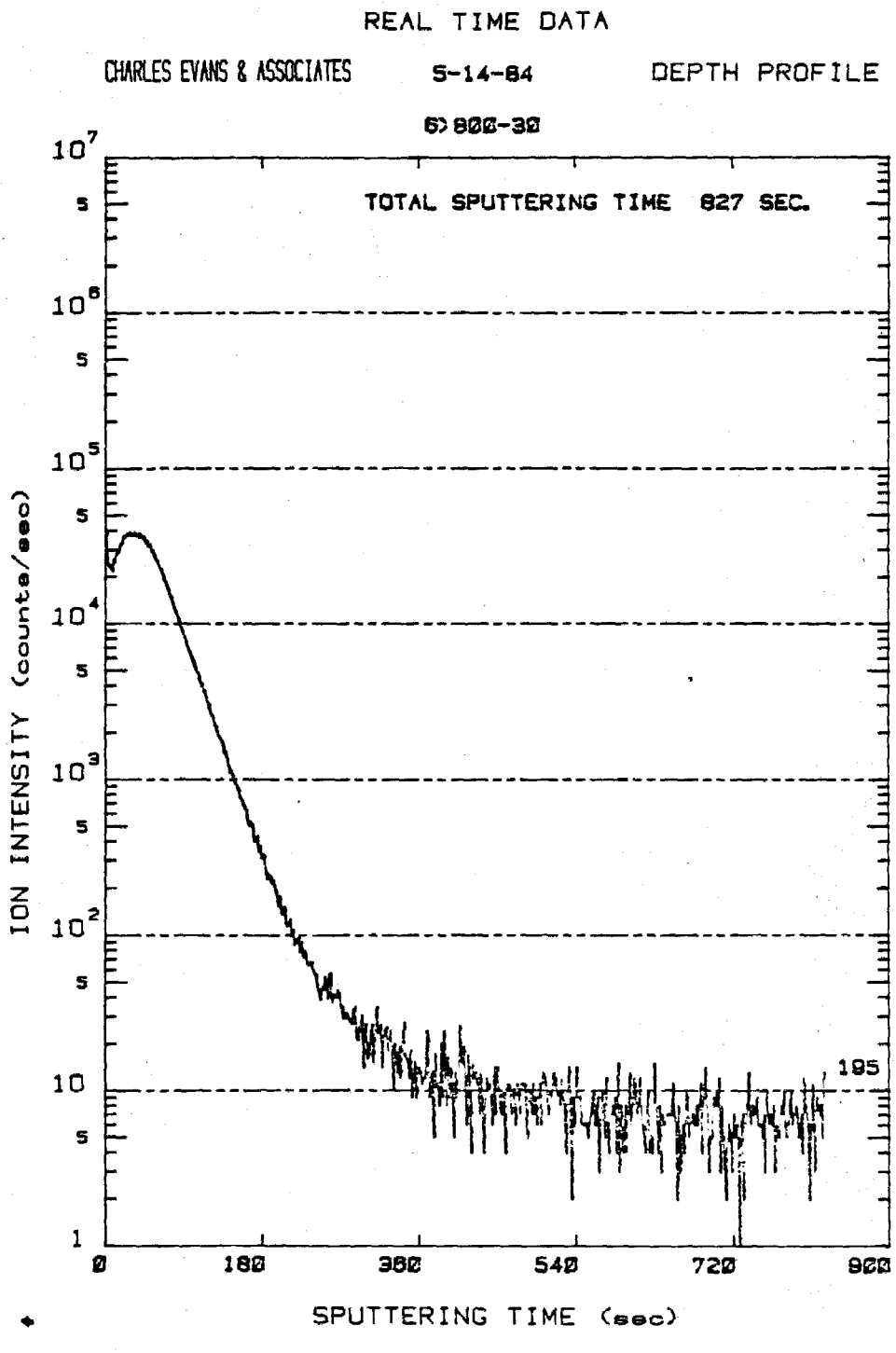
DLTS studies can provide information about traps in a region from approximately 0.5 to 7 μm from the interface, while the RBS spectra give insight about the silicide layer. In an attempt to obtain platinum concentration information in the portion of the material between these two regions, we turned to the secondary ion mass spectrometry (SIMS) technique.

SIMS is a method for the characterization of the atomic composition of a material. Energetic ions (typically oxygen or cesium) bombard a surface, causing secondary ions to be ejected from the material. These ions are mass-analyzed to determine their species. Since the incident ions sputter away a small crater on the surface, depth information is obtained by monitoring the signal as a function of time.

SIMS analyses were carried out on samples annealed for 30 min at 700, 750, and 800 °C, and samples annealed at 800 °C for 60 and 180 min. These samples consisted of a 1000 Å layer, in which the platinum concentration was 50 at.%, on top of a substrate which was almost entirely silicon. It was in the latter region that we wished to measure the platinum concentration. Thus, it was necessary to eliminate the silicide overlayer to prevent the large numbers of platinum atoms in that layer from travelling into the underlying silicon and affecting the measurements in that region. Unfortunately, PtSi is a material highly resistive to chemical etches. According to Murarka,[10] for example, PtSi is insoluable in aqua regia, HCl, HNO_3, H_2SO_4, HF, or $H_2SO_4 + H_2O_2$, and is only slightly soluable in $HF + HNO_3$. We required an etch that would not consume the silicon under the silicide film, so the $HF + HNO_3$ etch was not suitable. We therefore attempted to etch the silicide selectively by immersing each sample in a dilute HF solution and then immediately transferring it to a hot 2:1 $HCl + HNO_3$ solution. The role of the first etch was to consume the thin layer of native oxide, SiO_2, which grows on the silicide surface. The second etch then eliminated the silicide layer but did not etch the underlying silicon. This etching process resulted in a pitted and marred surface, but it did remove a large portion of the silicide.

Our SIMS measurements were made by Charles Evans and Associates of San Mateo, California. Both oxygen and cesium bombardment were used. Oxygen ion bombardment proved to be the better method, because cesium bombardment did not provide sufficient depth resolution. Figure 2.5 shows

Figure 2.5: Platinum ion intensity as a function of sputtering time for the etched PtSi sample annealed at 800 °C for 30 min — SIMS raw data. (From Charles Evans and Associates.)

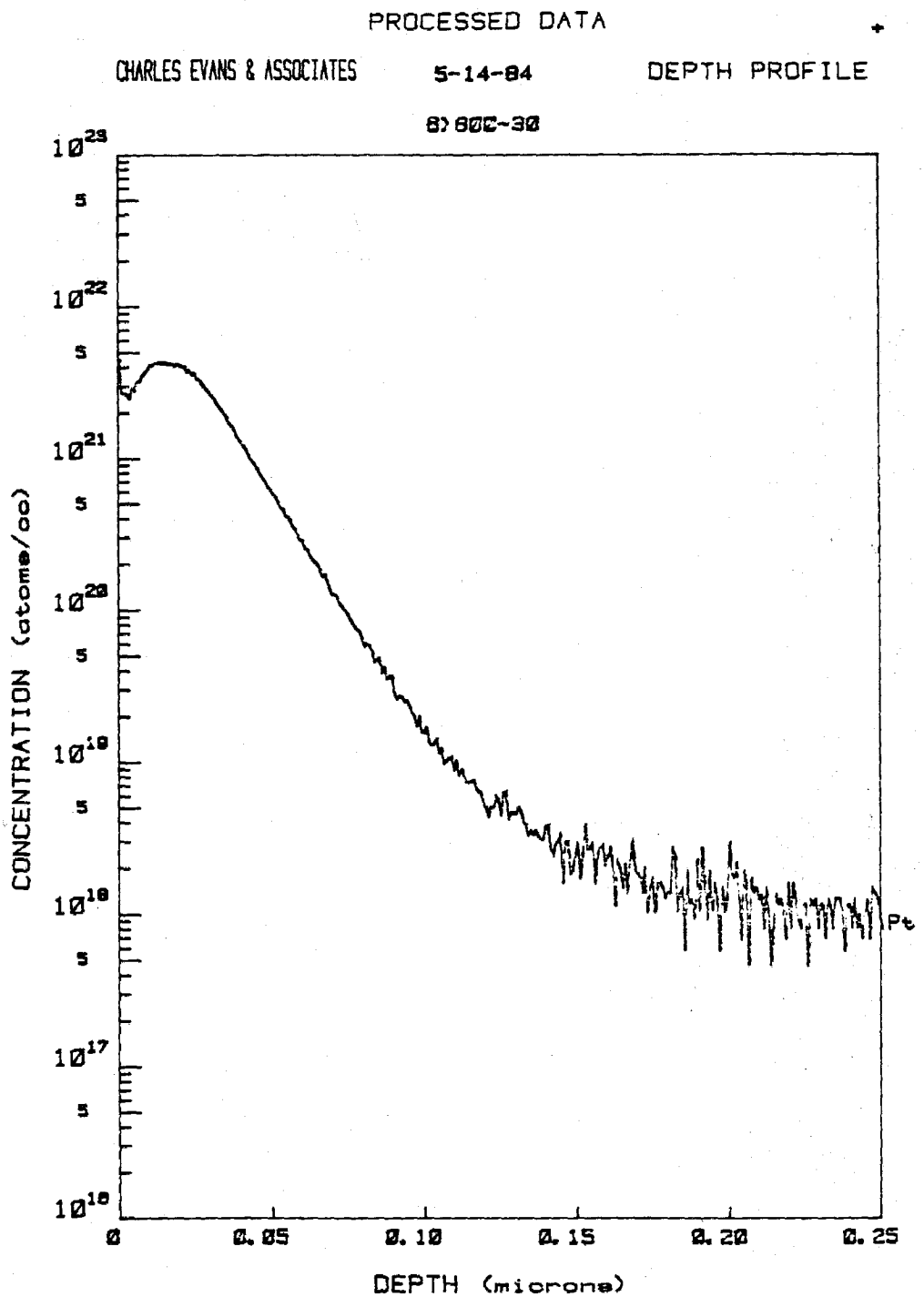

REAL TIME DATA
CHARLES EVANS & ASSOCIATES
5-14-84
DEPTH PROFILE
6) 800-30
TOTAL SPUTTERING TIME 827 SEC.
ION INTENSITY (counts/sec)
SPUTTERING TIME (sec)
195
0
180
360
540
720
900

the raw SIMS data for the sample which was annealed at 800 °C for 30 min. Here, the ion intensity is plotted as a function of the sputtering time. The signal drops by over three orders of magnitude in approximately 400 sec. The sputtering time is converted to a depth scale by using a Dektak stylus profilometer to measure the depth of the crater after sputtering. An RBS spectrum of the sample (taken after the etching procedure) provided information about the atomic percentage of platinum at the surface; this value was used to calibrate the ion intensity so that it would be possible to obtain a plot of the platinum concentration as a function of depth. Such a plot is shown in Fig. 2.6 for the raw data of Fig. 2.5.

All SIMS profiles for the five different samples were almost identical to the profile shown in Fig. 2.6. The initial spike in intensity and subsequent dip were caused by oxide contamination at the surface of the sample. It is therefore reasonable to assume that only data for depths greater than $\sim$ 200 Å were valid in these profiles. The peak (at 200 Å) corresponded to concentrations of 1 to 5×10^{21} cm^{-3} in all samples. Profiles indicated that the platinum concentration dropped to the detection limit of approximately 10^{18} at depths of 0.15 to 0.2 μm in all samples. There were no significant differences in the shapes of the profiles.

The primary problem in interpreting these SIMS results was that not all the platinum-rich silicide layer was removed from the samples. As mentioned previously, the higher temperature samples exhibited surface "islands" in SEM scans of the unetched silicide surface. Surface irregularities abounded in the etched samples as well, and were observed by optical microscopy. As

Figure 2.6: Platinum conentration as a function of depth from the (etched) surface. These data were obtained by processing the data of Fig. 2.5. (From Charles Evans and Associates.)


PROCESSED DATA
CHARLES EVANS & ASSOCIATES
5-14-84
DEPTH PROFILE
8)80C-30
CONCENTRATION (atoms/cc)
10^23
5
10^22
5
10^21
5
10^20
5
10^19
5
10^18
5
10^17
5
10^16
0
0.05
0.10
0.15
0.20
0.25
DEPTH (microns)
Pt

these islands were probably composed of platinum-rich material, they may have served as sources for platinum which was driven into the underlying regions during the sputtering process. Thus, platinum signal attributed to the platinum concentration in the silicon may actually have been the result of ion beam mixing of the materials. Also, since the islands varied in size and surface coverage, comparisons between the profiles of the various samples were difficult to make.

Thus, SIMS evaluations of our samples were severly limited by the lack of a good technique for the selective removal of the PtSi thin films. A possible solution to this problem might lie in the use of a plasma etching method. The results obtained on these samples indicate only that the platinum concentration in the region between the interface and the beginning of the DLTS profile region varies from 10 at.% to less than $\sim 10^{18}$ cm^{-3}.

2.4.3 I-V and C-V Measurements

Current-voltage measurements were made for two reasons: first to determine whether or not the device in question had sufficiently low reverse leakage currents for use in DLTS, and if so, to determine the barrier height from forward-bias plots of the logarithm of the current as a function of the voltage — $\log(I)$ vs V. In the case of our PtSi-Si samples, only those annealed at 800 °C had reverse leakage currents greater than or equal to 1 μA at a reverse bias of 5 V. Samples treated at 800 °C for 30, 60, and 180 min had average leakage currents of 1, 1.3, and 3.6 μA, respectively, at $V = 5$ V. All the devices were therefore suitable for DLTS measurements.

A typical forward-bias $\log(I)$ vs V plot is shown in Fig. 2.7. A fit of the region marked yields a built-in voltage of 0.78 V. This barrier height was obtained for essentially all of our samples. The value is consistent with the value reported in the literature for Pt_2Si on Si,[11] which is lower than that reported for PtSi on Si (0.87 V).[11] Thus, it is possible that our samples have a very thin interfacial layer composed of Pt_2Si which is fixing the barrier height at 0.78 V. Since this layer is not seen in the RBS spectra, it would have to be less than 200 Å thick. Since I-V data were taken only at room temperature, the ideality factor was not measured.

Capacitance-voltage measurements were made on each device used in the DLTS study to determine the shallow dopant concentration, N_+, and the capacitance at the DLTS reverse bias voltage, $C(V)$. These values are needed to compute the trap concentration from the DLTS peak amplitude (see Sec. 1.3.4). Since C is proportional to the square root of $N_+/(V_{bi}+V)$, N_+ can be extracted from the slope of a plot of $1/C^2$ vs V. Figure 2.8 shows a typical $1/C^2$ vs V plot for one of the PtSi-Si samples annealed at 800 °C for 30 min. N_+ has been calculated as a function of the reverse voltage also and is shown in Fig. 2.8; its average value is 6.6×10^{14} cm^{-3}. This C-V measurement was made at 130 K.

In addition, the Schottky barrier height was computed from the intercept on the voltage axis. The extrapolation of the data to this axis, shown as a dotted line in Fig. 2.8, yielded an intercept of 0.66 V. The barrier height was then calculated to be approximately 0.75 eV, in reasonable agreement with the value obtained by I-V.

Figure 2.7: $\log(I)$ vs V plot for a PtSi sample annealed at 800 °C for 30 min. These data were taken at room temperature. The vertical bars indicate the region used for the fit.

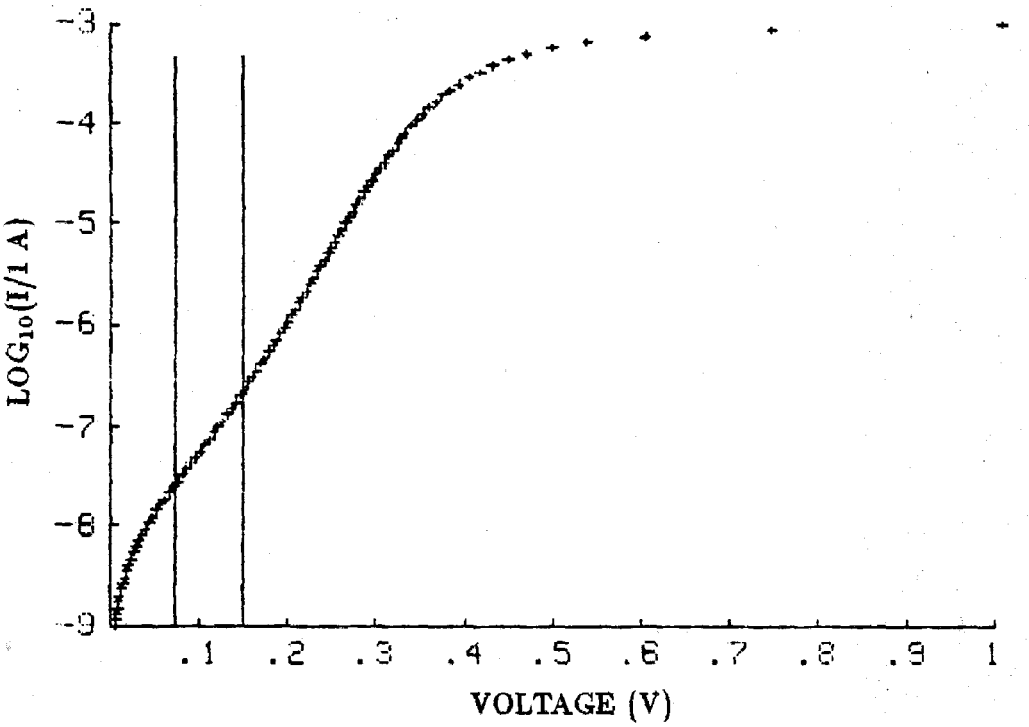
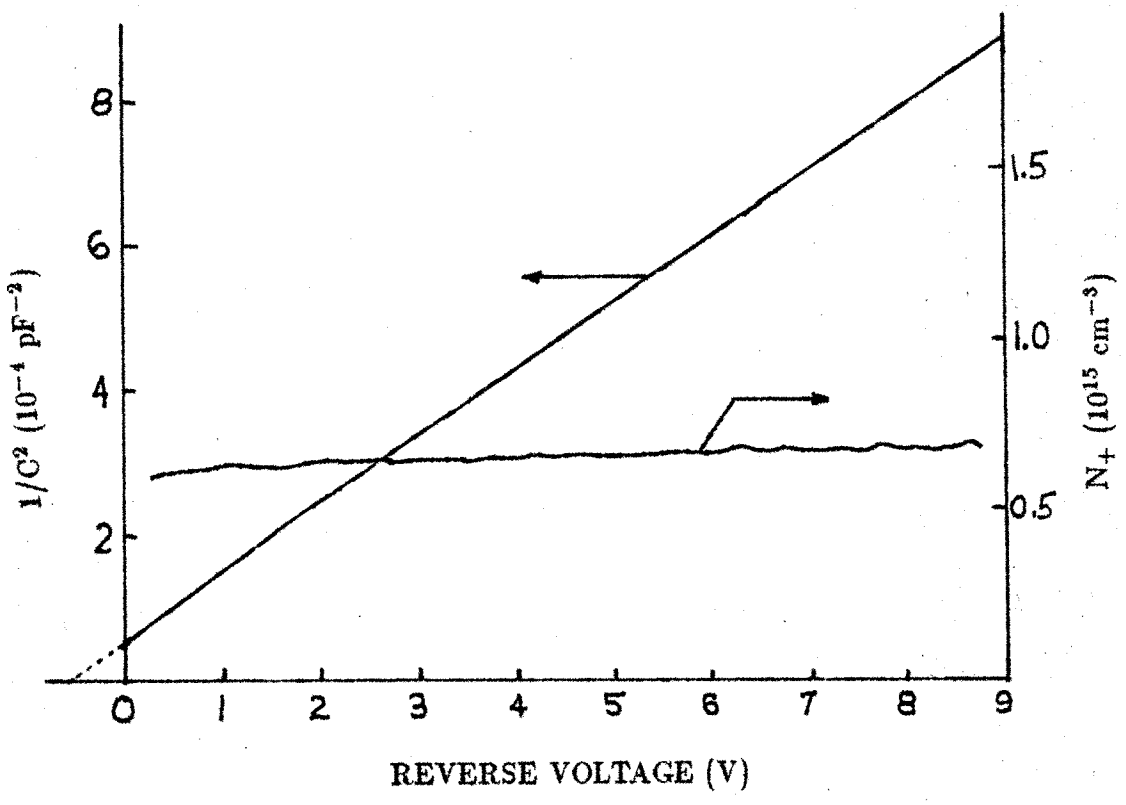

-3
-4
-5
-6
-7
-8
-9
LOG10(I/1 A)
.1
.2
.3
.4
.5
.6
.7
.8
.9
1
VOLTAGE (V)

Figure 2.8: $1/C^2$ vs V and N_+ vs V plots for a PtSi sample annealed at 800 °C for 30 min. The dashed line indicates the extrapolation of the data.


8
6
4
2
1.5
1.0
0.5
$1/C^2$ (10^{-4} pF^{-2})
N_+ (10^{15} cm^{-3})
0 1 2 3 4 5 6 7 8 9
REVERSE VOLTAGE (V)

2.4.4 DLTS Measurements

The DLTS trap measurements were made using a Boonton Model 72BD capacitance meter. A double boxcar gating scheme was used to analyze the capacitance transients of the Schottky barrier diodes. A typical DLTS spectrum for a sample with a detectable concentration of platinum traps is shown in Fig. 2.9. For a scanning time constant of 18.2 ms, no other traps were observed in the samples up to 350 K. The trap observed was found to have an activation energy of 0.22±0.015 eV, which is in excellent agreement with the value given by Brotherton *et al.*[12] for the platinum electron trap in silicon.

By applying reverse bias voltages from 2 to 25 V and changing the amplitude of the trap-filling pulses, we were able to observe electron emission from platinum traps in a region from 0.5–7 μm from the interface. The trap concentration profiles obtained by this method are shown in Fig. 2.10 for the samples which had detectable platinum trap concentrations. In the sample annealed at 700 °C for 30 minutes, we measure trap concentrations of $\sim 5 \times 10^{11}$ cm^{-3} which are just within our detection limit. Trap concentrations are approximately 10^{13} and 10^{14} for samples treated at 750 °C and 800 °C, respectively. The concentration profile for the sample which was annealed at 800 °C for 180 minutes falls off more slowly with distance from the interface than that for the sample annealed at the same temperature for 30 minutes, but the concentrations 0.5 μm from the interface are relatively close.

Figure 2.9: Platinum electron trap seen in DLTS spectrum taken with time constant of 18.2 ms. E_a is the trap activation energy measured relative to the conduction band (CB).

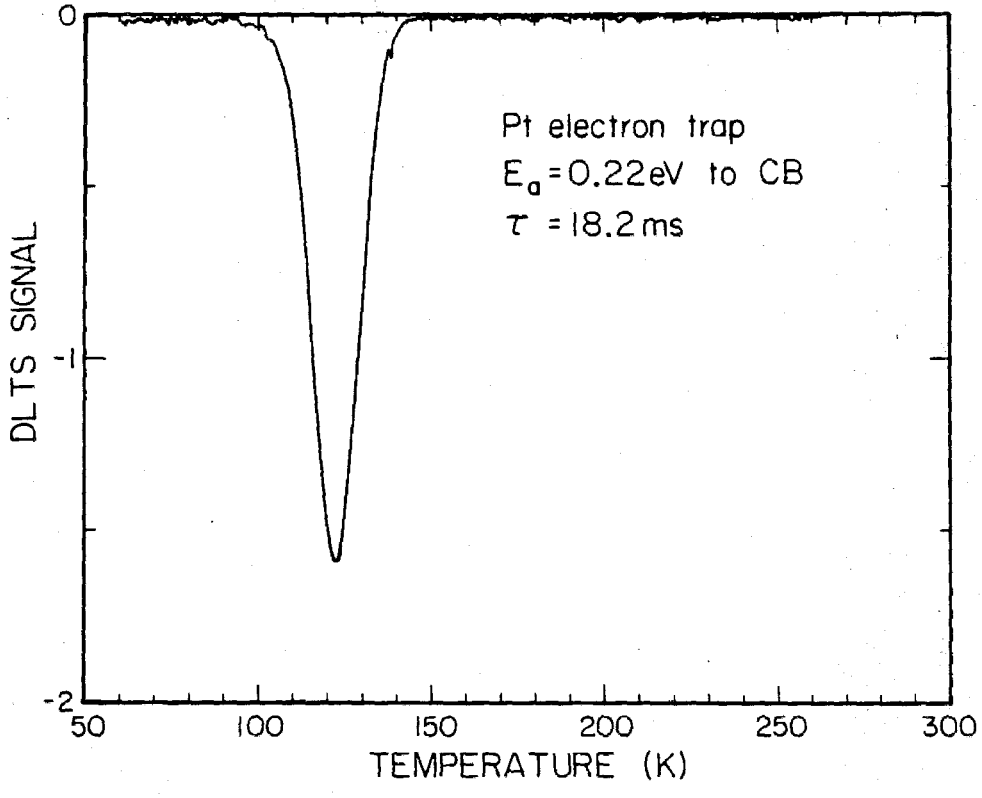
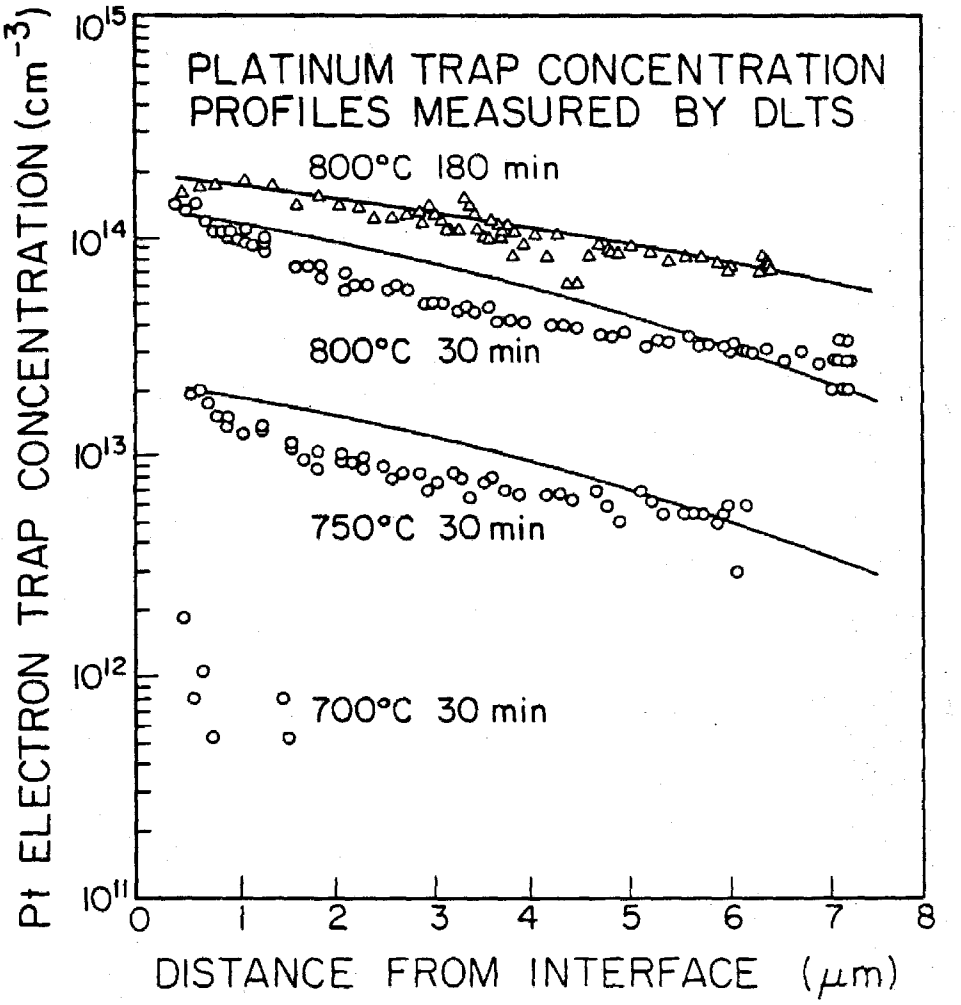

Pt electron trap
E_a=0.22eV to CB
τ =18.2ms
DLTS SIGNAL
0
-1
-2
50
100
150
200
250
300
TEMPERATURE (K)

Figure 2.10: Platinum trap concentration profiles obtained by DLTS. The solid lines are representative erfcs.


PLATINUM TRAP CONCENTRATION
PROFILES MEASURED BY DLTS
800°C 180 min
800°C 30 min
750°C 30 min
700°C 30 min
Pt ELECTRON TRAP CONCENTRATION (cm⁻³)
DISTANCE FROM INTERFACE (μm)
10¹⁵
10¹⁴
10¹³
10¹²
10¹¹
0
1
2
3
4
5
6
7
8

An extrapolation of the RBS data, discussed in Sec. 2.4.1, indicated that the platinum atom concentration falls off by an order of magnitude in 2000 Å (under the assumption that the RBS Pt tails were due to platinum at the interface). Since this fall off would correspond to an almost vertical line on the plot of Fig. 2.10, it is clear that the extrapolation of the RBS data is meaningless in the region of the DLTS measurements.

For simple diffusion of platinum from an infinite source at the surface, the concentration distribution at any temperature would be described by a complementary error function (erfc). The profiles we have measured are not in general described by complementary error functions, as our DLTS profiles bend in the opposite direction from erfcs. Thus, the distribution of platinum traps which we have observed is not due to simple diffusion. However, our profiles are similar in shape to the diffusion profile of gold in silicon, measured in Ref. 13 by radiotracer experiments. The profile in that case is thought to be a result of the interaction among Au atoms in substitutional sites, Au atoms in interstitial sites, and silicon self-interstitials.[14] A similar theory could explain our platinum trap diffusion profiles.

2.4.5 Summary of Platinum Results

Analyses of the RBS spectra of our samples yielded silicide compositions of Pt_2Si for the sample annealed at 300 °C for 30 min and PtSi for samples annealed from 400 to 800 °C. Noticeably nonabrupt low-energy fall-offs were observed for the platinum signals of samples annealed at 800 °C. The spectra showed that the PtSi phase is maintained at the surface at 800 °C for

annealing times less than 3 hours.

SIMS studies were thwarted by the need for a method to etch the PtSi films selectively and completely.

C-V measurements were used to obtain values for N_+ and $C(V)$ for making trap concentration measurements by DLTS. I-V measurements showed that all the PtSi samples had very low reverse leakage currents, and could therefore be used for DLTS. Also, barrier heights were measured using I-V techniques.

Our DLTS studies of platinum diffusion into (100) silicon substrates from PtSi showed that there is no observable diffusion at temperatures below 700 °C for our samples. The electron trap concentration measured by DLTS ranged from $2.0\text{–}0.5\times10^{13}$ cm^{-3} in the region from 0.5–7 μm from the interface for the sample treated at 750 °C for 30 minutes. In the 800 °C samples, the concentration range was $1.8\text{–}0.3\times10^{14}$ cm^{-3}. Thus, we conclude that 700 °C is a safe temperature below which the silicon is not poisoned by the diffusion of platinum electron traps.

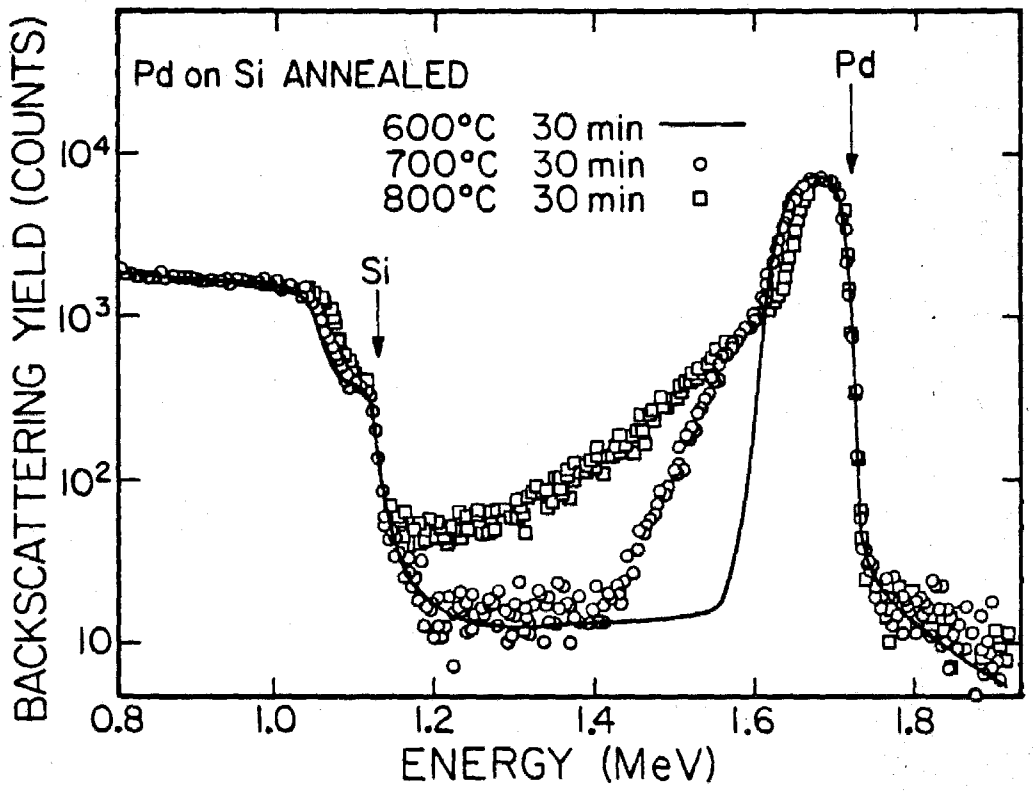
2.5 Results for Palladium and Nickel Silicides

In this section, we report the observation of the thermal degradation of several palladium silicide-silicon and nickel silicide-silicon structures. Silicon substrates covered with palladium or nickel films were annealed at temperatures from 300 °C to 800 °C for 30 minutes to form the silicides. RBS spectra showed no degradation of the silicide in the samples treated below 700 °C in either case; however, the degradation of the silicides was clear in samples annealed at 700 and 800 °C. Reverse-biased leakage currents increased with increasing annealing temperature in both cases. The degradation was almost negligible for palladium samples at temperatures which caused the nickel silicide barriers to become very leaky. A very small concentration ($\sim 5 \times 10^{11}$ cm^{-3}) of traps was detected for the high-temperature palladium samples. For the nickel samples which were still reasonable barriers, DLTS showed no traps.

2.5.1 RBS Measurements

RBS spectra were taken for the samples to determine the composition of the thin silicide layer and to check for surface smoothness and interface abruptness. Analysis yielded surface silicide compositions consistent with Pd_2Si for palladium samples annealed at 300–800 °C for 30 min. Figure 2.11 shows the results for palladium samples annealed at 600, 700, and 800 °C. The low-energy fall-off of the palladium signal is clearly less abrupt as temperature is increased. This blurring could be due to the interface growing

Figure 2.11: RBS spectra for palladium-on-silicon structures.


Pd on Si ANNEALED
600°C 30 min
700°C 30 min
800°C 30 min
Si
Pd
BACKSCATTERING YIELD (COUNTS)
10⁴
10³
10²
10
0.8
1.0
1.2
1.4
1.6
1.8
ENERGY (MeV)

less abrupt, the surface morphology becoming rough, or a combination of the two. Similar spectra for the nickel samples are shown in Fig. 2.12. RBS indicates that the phase is Ni_2Si for the 300 °C sample, NiSi for the 400–700 °C samples, and $NiSi_2$ for the 800 °C sample. Again, we see the a tail in the transition metal signal at its low-energy end. In comparison, spectra for the platinum silicide structures discussed in Sec. 2.4.1 showed relatively little blurring of the low-energy metal signal for samples annealed at these temperatures.

2.5.2 I-V and C-V Measurements

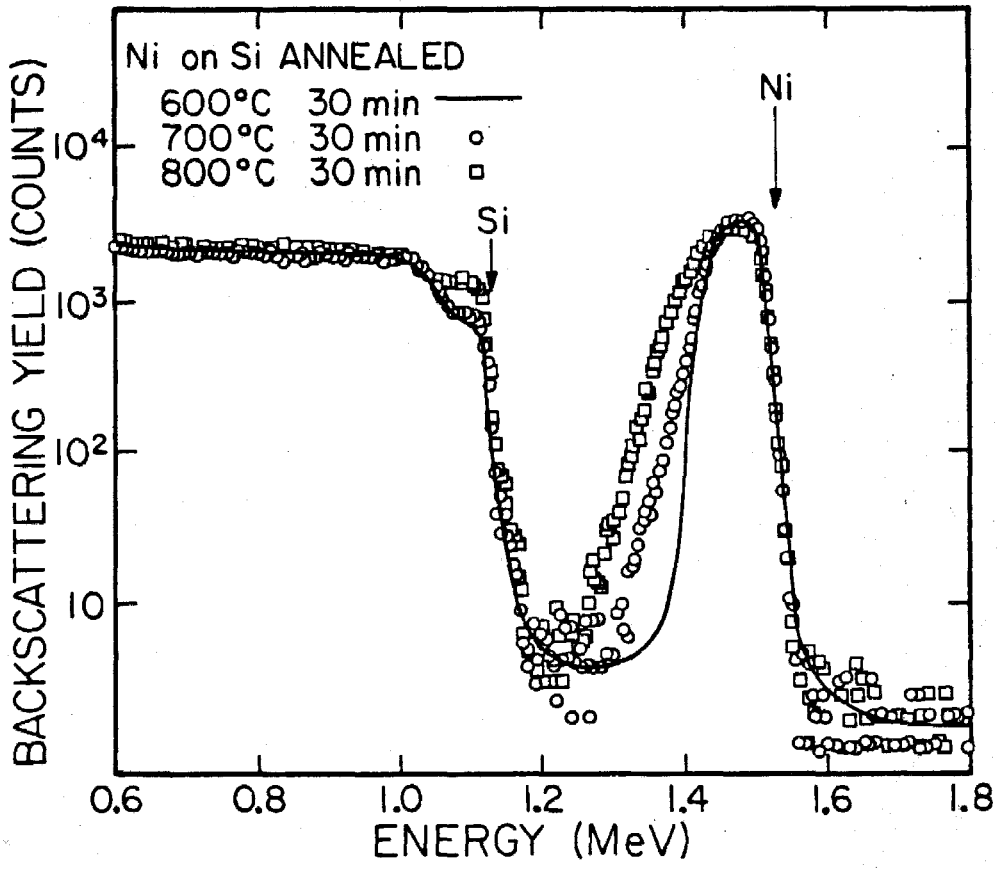
Reverse-biased leakage currents at 5 V for nickel and palladium silicide Schottky barriers annealed at various temperatures are given in Table 2.1. Values for platinum silicide barriers are also given for comparison. The degradation at a given temperature was more severe for palladium than for platinum, and even worse for nickel. Of the palladium samples, only those treated at 700 °C and below had leakage currents low enough for DLTS measurements. The highest temperature nickel sample that was suitable for DLTS was only annealed at 500 °C.

C-V measurements were only required for those samples used for DLTS. They yielded values of N_+ of $\sim 5 \times 10^{14}$ cm^{-3} as expected.

2.5.3 DLTS Measurements

DLTS spectra were generated with a rate window of 55 s^{-1} for the samples which had sufficiently low reverse leakage currents. The spectra

Figure 2.12: RBS spectra for nickel-on-silicon structures.


Ni on Si ANNEALED
600°C 30 min
700°C 30 min
800°C 30 min
Si
Ni
BACKSCATTERING YIELD (COUNTS)
10⁴
10³
10²
10
0.6
0.8
1.0
1.2
1.4
1.6
1.8
ENERGY (MeV)

	500 °C	600 °C	700 °C	800 °C
Ni	67 μA	330 μA	2.2 mA	14 mA
Pd	<1 μA	<1 μA	9.1 μA	370 μA
Pt	<1 μA	<1 μA	<1 μA	1 μA

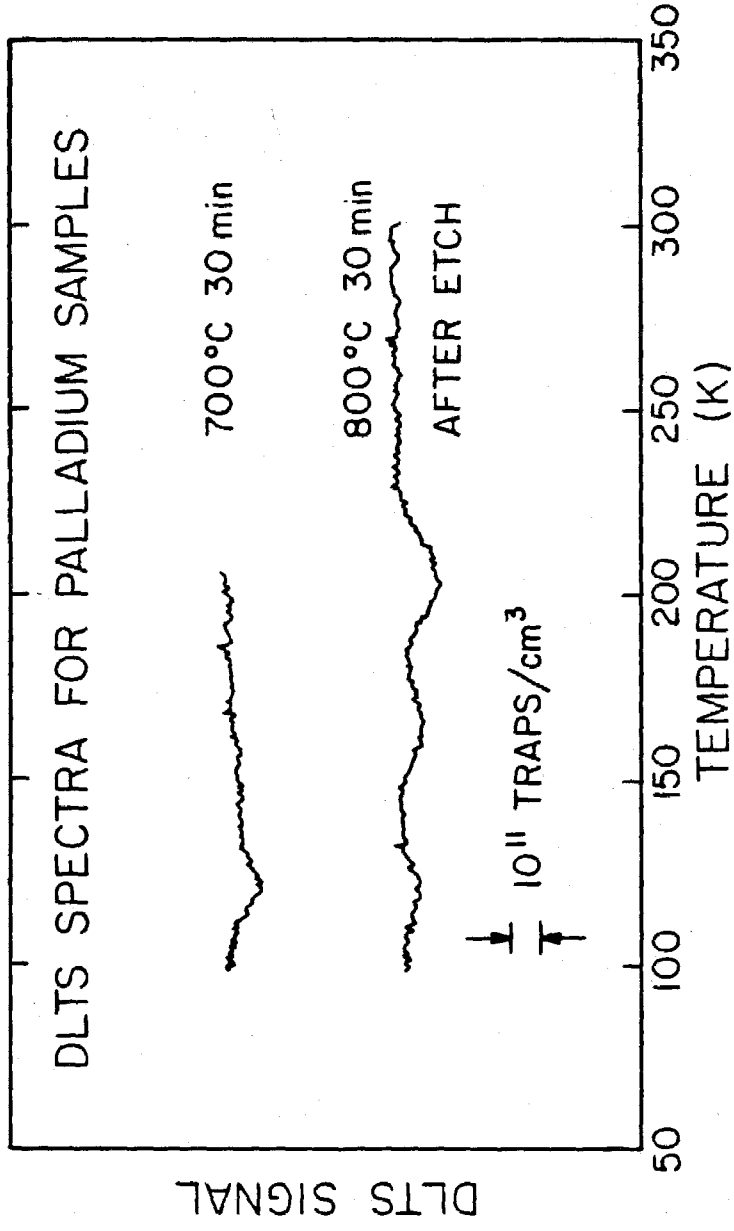
Table 2.1. Leakage currents at 5 V reverse bias in nickel, palladium, and platinum silicide samples annealed for 30 min.

exhibited no traps above a detection limit of $\sim 5\times10^{11}$ traps cm^{-3} in any nickel sample treated below 500 °C. Nickel samples which were treated at temperatures above 500 °C had reverse leakage currents which made DLTS measurements impossible. A piece of nickel material which was annealed at 800 °C was etched and prepared as described in Sec. 2.3 to make DLTS measurements in a region 5–10 μm below the original interface. Again, no traps were detected.

In the case of palladium samples, DLTS spectra exhibited no traps above the detection limit for the samples treated below 700 °C. A barely detectable peak at a temperature of 120 K appeared in the spectrum of the Pd_2Si sample annealed at 700 °C (shown in Fig. 2.13). Although the signal was so small that it was not possible to make a measurement of the trap activation energy, the location of this peak is consistent with the reported activation energy of 0.22 eV from the conduction band.[15] Thus, we believe that the peak represents a small concentration ($\sim 10^{11}$ cm^{-3}) of palladium electron traps.

Palladium samples which were treated at temperatures above 700 °C had high reverse leakage currents. As in the case of the high-temperature nickel samples, a piece of 800 °C palladium material was etched to make DLTS measurements below the original interface. The resultant spectrum is shown in Fig. 2.13. Again, we saw a very small peak at 120 K which was probably due to palladium electron traps. In addition, there were minute peaks at 165 and 200 K which were not observed close to the interface in the 700 °C sample. Nor were these peaks seen in the nickel samples which were

Figure 2.13: DLTS spectra of palladium silicide samples taken with boxcar gates at 5 ms and 45 ms for a rate window setting of 55 s^{-1}.


DLTS SPECTRA FOR PALLADIUM SAMPLES
700°C 30 min
800°C 30 min
AFTER ETCH
10^{11} TRAPS/cm^3
DLTS SIGNAL
50
100
150
200
250
300
350
TEMPERATURE (K)

etched and prepared in exactly the same fashion. These signals may represent the presence of a contaminant (such as iron, a fast diffuser in silicon) which could have been in the palladium charge material used to evaporate the metal onto the silicon substrate. All three peaks correspond to trap concentrations of $\sim 10^{11}$ traps cm^{-3}.

2.5.4 Summary of Palladium and Nickel Results

Our RBS studies showed a degradation of the silicide layers for nickel and palladium silicides annealed at temperatures above 600 °C. The I-V measurements indicated poor Schottky barrier behavior in nickel samples treated above 500 °C and palladium samples treated above 700 °C. DLTS measurements of the nickel samples with small leakage currents showed no traps. An extremely small number of traps were seen in the 700 and 800 °C palladium samples. Thus, we conclude that 700 °C may be regarded as the maximum safe temperature at which palladium silicides may be annealed before transition metal indiffusion begins to degrade the underlying silicon. For our nickel silicide samples, the maximum temperature for good Schottky barrier behavior is only 500 °C.

2.6 Results for Other Silicides

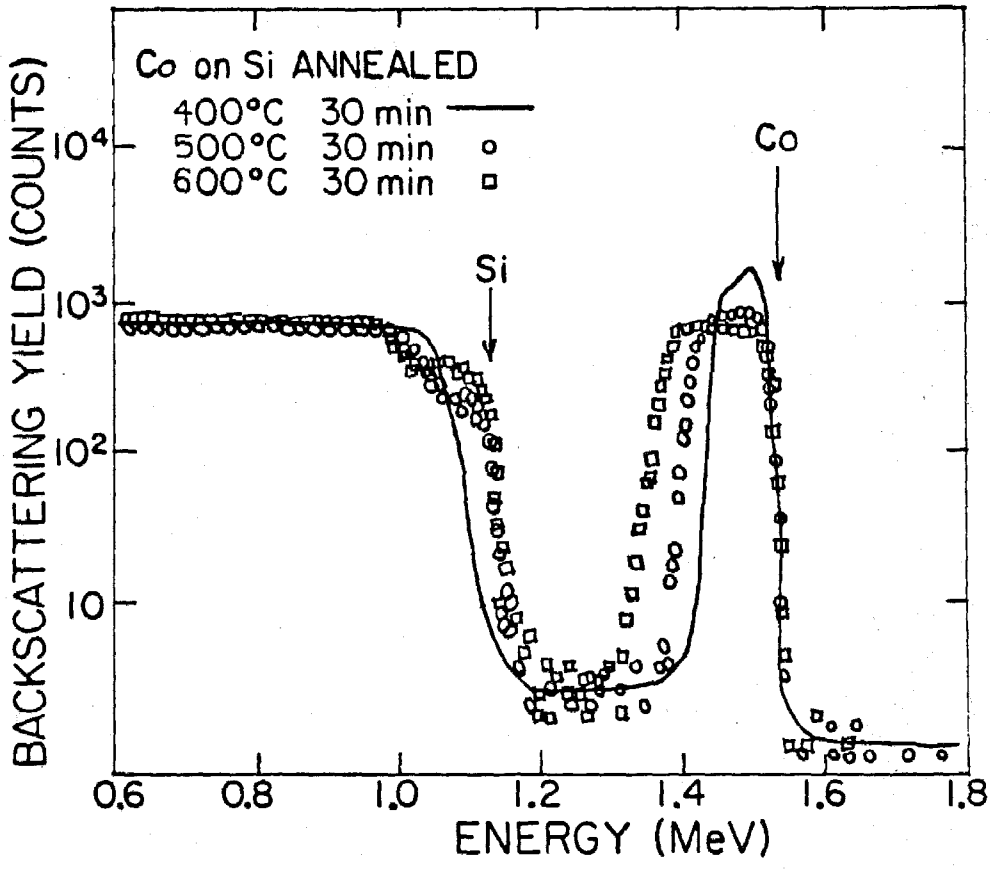
In this section, we describe the results of measurements of a group of cobalt, chromium, and erbium silicide samples. The cobalt and chromium samples were prepared as were the samples discussed in the previous sections, i.e., by vacuum annealing silicon substrates covered with pure metal overlayers. RBS spectra showed no silicide formation in cobalt samples annealed at 300 or 400 °C. The sample annealed at 500 °C was CoSi; samples annealed at temperatures from 600 to 800 °C were $CoSi_2$. DLTS spectra of these samples showed no traps for the structures annealed at temperatures above 500 °C; however, a trap of concentration $\sim 10^{12}$ cm^{-3} was seen in the sample annealed at 400 °C. DLTS spectra of the chromium silicide samples showed no traps in samples annealed at temperatures from 300 to 900 °C.

The erbium silicide samples were provided by S. S. Lau of the University of California at San Diego (UCSD). One set of these samples was prepared by annealing at 380 °C for 50 min in a vacuum furnace; the other set was treated similarly under a flow of forming gas (hydrogen + nitrogen). DLTS spectra exhibited no traps in either case.

2.6.1 Cobalt Silicides

RBS spectra were taken for the cobalt samples annealed at temperatures from 300 to 800 °C. Figure 2.14 shows the results for the samples treated at 400, 500, and 600 °C. The 300 °C spectrum was indentical to that for 400 °C, and spectra for samples annealed at 700 and 800 °C did not differ

Figure 2.14: RBS spectra for cobalt-on-silicon structures.


Co on Si ANNEALED
400°C 30 min
500°C 30 min
600°C 30 min
Si
Co
BACKSCATTERING YIELD (COUNTS)
10⁴
10³
10²
10
0.6
0.8
1.0
1.2
1.4
1.6
1.8
ENERGY (MeV)

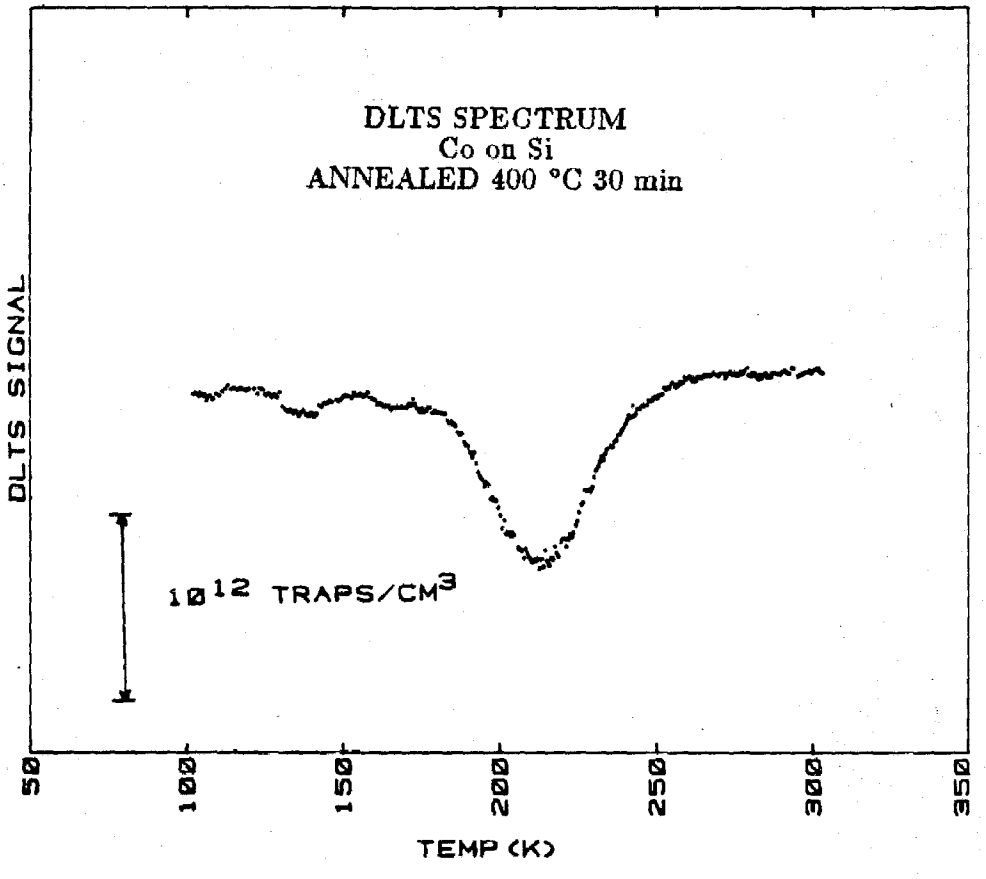
from the 600 °C case. No silicide formation was apparent in the 400 °C spectrum. Analysis yielded surface silicide compositions consistent with CoSi for the cobalt sample annealed at 500 °C, and $CoSi_2$ for the higher temperature samples. The low-energy fall-off of the cobalt signal did not appear to blur as temperature is increased.

DLTS spectra were taken with a rate window of 55 s^{-1}. The spectra exhibited no traps above a detection limit of $\sim 5 \times 10^{11}$ traps cm^{-3} in any sample treated at or above 500 °C. In addition, a piece of cobalt material which was annealed at 800 °C was etched and prepared as described in Sec. 2.3 to make DLTS measurements in a region 5–10 μm below the original interface. Again, no traps were detected.

However, the sample which was treated at 400 °C exhibited a peak corresponding to a trap concentration of $\sim 10^{12}$ cm^{-3}. This spectrum is shown in Fig. 2.15. Ransom *et al.*[16] have recently reported similar findings: for their cobalt-on-silicon samples annealed at 400 °C in helium or forming gas, they see a trap of concentration as high as 10^{12} cm^{-3} which is not present in higher temperature samples.

Our RBS spectrum for the 400 °C sample showed that no silicide formation had occurred yet. However, the high-energy end of the silicon signal was slightly blurred compared to the spectrum for unannealed cobalt on silicon. Thus, it is probable that some intermixing did occur without formation of a silicide. Ransom *et al.* did not mention any RBS or other results that would indicate the degree of silicide formation in their samples. Our results indicate the possibility that indiffused cobalt that has moved several thousands

Figure 2.15: DLTS spectrum of cobalt sample taken with boxcar gates at 5 ms and 45 ms for a rate window setting of 55 s^{-1}.


DLTS SPECTRUM
Co on Si
ANNEALED 400 °C 30 min
DLTS SIGNAL
10^{12} TRAPS/CM^3
50
100
150
200
250
300
350
TEMP (K)

of angstroms into the silicon becomes electrically inactive at higher annealing temperatures, perhaps because it precipitates out of the electrically active sites.

2.6.2 Chromium Silicides

We used DLTS to investigate chromium silicide samples which had been treated at temperatures from 300 to 800 °C for deep level contamination. All of these samples maintained low reverse leakage currents. No traps were seen above the detection limit of $\sim 10^{11}$ cm^{-3} in DLTS.

2.6.3 Erbium Silicides

DLTS measurements were carried out on erbium silicide samples annealed at 380 °C for 50 min under vacuum and under a flow of forming gas. I-V measurements on these samples, made at UCSD, showed significantly greater reverse leakage currents in the case of vacuum annealing: average leakage was only 0.87 μA at 20 V for the forming gas samples compared to 5.5 μA for the vacuum annealed samples. Deep level indiffusion was thought to be a possible cause of this discrepancy. However, DLTS measurements showed no traps in either case.

2.7 Summary of Silicide Results

Platinum-on-silicon structures that were annealed at temperatures from 300 to 800 °C were characterized using Rutherford backscattering spectrometry (RBS), secondary ion mass spectrometry (SIMS), current-voltage (I-V) and capacitance-voltage (C-V) measurements, and deep level transient spectroscopy (DLTS).

RBS spectra indicated the presence of Pt_2Si at the surface of the 300 °C sample and PtSi for the higher temperature samples. They also showed tails at the low-energy end of the platinum signal in samples treated above 600 °C, indicating some intermixing or the formation of islands on the surface. SIMS profiles were not very useful in our studies due to the difficulties involved in preparing the surface properly; however, they did yield Pt concentrations consistent with our other measurements.

I-V measurements showed very low reverse leakage currents and a barrier height of 0.78 eV in the PtSi samples annealed up to 800 °C. C-V measurements set the shallow donor level in the substrate at $\sim 5\times10^{14}$ cm^{-3}. DLTS spectra exhibited no traps in samples treated below 700 °C. Platinum electron traps of activation energy 0.22 eV were observed in the 700 °C sample at a concentration of $\sim 10^{11}$ cm^{-3}. The concentration of the traps ranged from $0.5 - 2\times10^{13}$ cm^{-3} in the region from 7 to 0.5 μm from the interface in the sample treated at 750 °C for 30 min. The concentration range was $0.3 - 1.8\times10^{14}$ cm^{-3} for the samples annealed at 800 °C.

Palladium- and nickel-on-silicon structures annealed at temperatures

from 300 to 800 °C were characterized using RBS, DLTS, and I-V and C-V measurements.

RBS spectra indicated surface silicide compositions of Pd_2Si for all palladium samples and Ni_2Si (300 °C), NiSi (400–700 °C), and $NiSi_2$ (800 °C) for the various nickel samples. They also showed a good deal of degradation of the silicide layers in all samples treated above 600 °C.

Only samples treated below 700 °C for palladium and 500 °C for nickel had sufficiently low reverse leakage currents for DLTS measurements. Of all these samples, DLTS showed traps above the detection limit of $\sim 10^{11}$ cm^{-3} only in the palladium sample treated at 700 °C. In that case, the DLTS spectrum exhibited a peak at a temperature consistent with that expected for a palladium electron trap at a concentration of a few times 10^{11} cm^{-3}. Samples were also prepared for DLTS by removing the top 5–10 μm layer of the palladium and nickel structures that had been annealed at 800 °C. DLTS probes of this region — 5 to 10 μm from the original interface — showed no traps in the nickel case. The spectrum for the palladium sample had three peaks, each of which corresponded to trap concentrations below 5×10^{11} cm^{-3}. One of these is the same as the palladium peak seen in the 700 °C sample; the others may be caused by indiffused impurities that were present in the palladium charge material.

Cobalt-on-silicon structures which were annealed at temperatures from 300 to 800 °C were characterized using RBS and DLTS. RBS indicated no silicide formation for the 300 and 400 °C samples; CoSi (500 °C) and $CoSi_2$ (600–800 °C) were seen in the spectra of the higher temperature samples.

DLTS showed no traps in the samples annealed at or above 500 °C; however, a trap of concentration $\sim 10^{12}$ cm^{-3} was detected in the 400 °C sample.

Chromium-on-silicon samples which were annealed at temperatures from 300–800 °C were characterized by DLTS. Although reverse leakage currents were sufficiently low for DLTS measurements in all of these samples, no traps were detected.

Erbium silicide-silicon samples which were grown by annealing at 380 °C for 50 min in vacuum or forming gas were characterized by DLTS. No traps were detected in either case.

These results indicate several conclusions: *a*) The maximum safe temperature (below which indiffusion is negligible) for platinum or palladium silicide on silicon is 700 °C; for nickel silicide on silicon, this temperature is only 500 °C. *b*) Cobalt indiffusion into silicon may be occurring prior to the formation of a silicide layer at the surface, but there is no evidence for contamination after the silicide has been formed or at high temperature. *c*) Chromium silicide-silicon structures exhibit no degradation or indiffusion of traps up to an annealing temperature of 800 °C. *d*) Erbium silicide-silicon samples show no indication of indiffused traps at 380 °C regardless of the annealing ambient.

These studies represent the first collection of investigations of deep level indiffusion from transition metal silicides on silicon. In addition to providing the specific results for the silicides mentioned here, our investigations have demonstrated the general applicability of DLTS to the characterization of silicide-silicon structures.

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CHAPTER 3

DLTS STUDIES OF $In_{1-x}Ga_xAs_yP_{1-y}$

3.1 Introduction

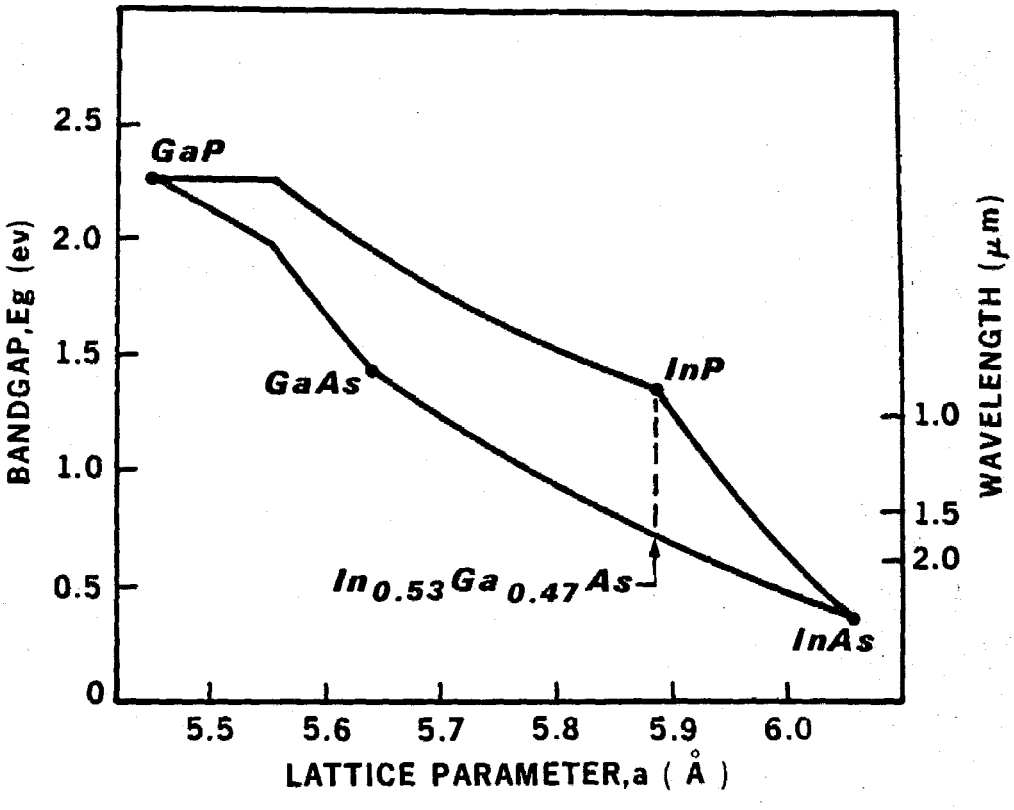
In this chapter, we describe the results of DLTS studies of four compositions of the quaternary alloy $In_{1-x}Ga_xAs_yP_{1-y}$.

This introduction discusses the material system and its laser applications — and limitations — that have been the subject of a great deal of interest in recent years. Section 3.2 explains how the samples were fabricated, and Sec. 3.3 describes the DLTS results and summarizes the conclusions of the study.

3.1.1 The $In_{1-x}Ga_xAs_yP_{1-y}$ Material System

The quaternary alloy $In_{1-x}Ga_xAs_yP_{1-y}$ is a relative newcomer to the world of semiconductor technology, having been grown in laboratories for only approximately 12 years.[1] Figure 3.1 shows the range of bandgaps and lattice parameters that are possible by varying x and y between 0 and 1. The four corners of the region represent the binary III-V materials GaP, InP, InAs, and GaAs. Some properties of these endpoints are given in Table 3.1. Each curve connecting these points represents a ternary alloy, e.g., $In_{1-x}Ga_xAs$ between InAs and GaAs. From the figure, it is clear that particular values of x and y may be chosen such that the alloy is lattice-matched to either GaAs or InP, and thus may be epitaxially grown on these materials with minimal strain and dislocations. Of greatest interest are the set of compositions matched to InP, because these alloys have bandgaps that cover a range that can be exploited for devices for lightwave communication

Figure 3.1: Bandgap as a function of lattice parameter for the possible compositions of $In_{1-x}Ga_xAs_yP_{1-y}$. The dashed line shows the compositions that are lattice-matched to InP. The points of discontinuous slope of the boundary curves approaching GaP correspond to the transition from direct to indirect bandgap. The scale on the right indicates the wavelength of a photon with energy equal to the bandgap shown on the left scale. (Courtesy of M. A. Pollack.)


GaP
GaAs
InP
$In_{0.53}Ga_{0.47}As$
InAs
2.5
2.0
1.5
1.0
0.5
0
BANDGAP,Eg (ev)
1.0
1.5
2.0
WAVELENGTH (μm)
5.5
5.6
5.7
5.8
5.9
6.0
LATTICE PARAMETER,a (Å)

	E_g (eV)	μ_{elec} ($cm^2V^{-1}s^{-1}$)	μ_{hole} ($cm^2V^{-1}s^{-1}$)	ϵ_r
InP	1.28	4000	100	12.4
InAs	0.36	22600	200	14.6
GaAs	1.43	8500	400	13.2
GaP	2.26	300	150	11.1
Si	1.11	1350	480	11.8

Table 3.1. Properties of the four binary endpoints of $In_{1-x}Ga_xAs_yP_{1-y}$. Values for silicon are also given for comparison. E_g is the energy of the bandgap, μ the carrier mobility, and ϵ_r the relative dielectric constant. (Taken from Ref. 2.)

systems. These bandgaps range from 0.75 ($In_{0.53}Ga_{0.47}As$) to 1.35 eV (InP); the corresponding wavelengths are from 1.66 to 0.92 μm. This region of the spectrum includes the wavelengths of lowest loss and dispersion in modern optical fibers.

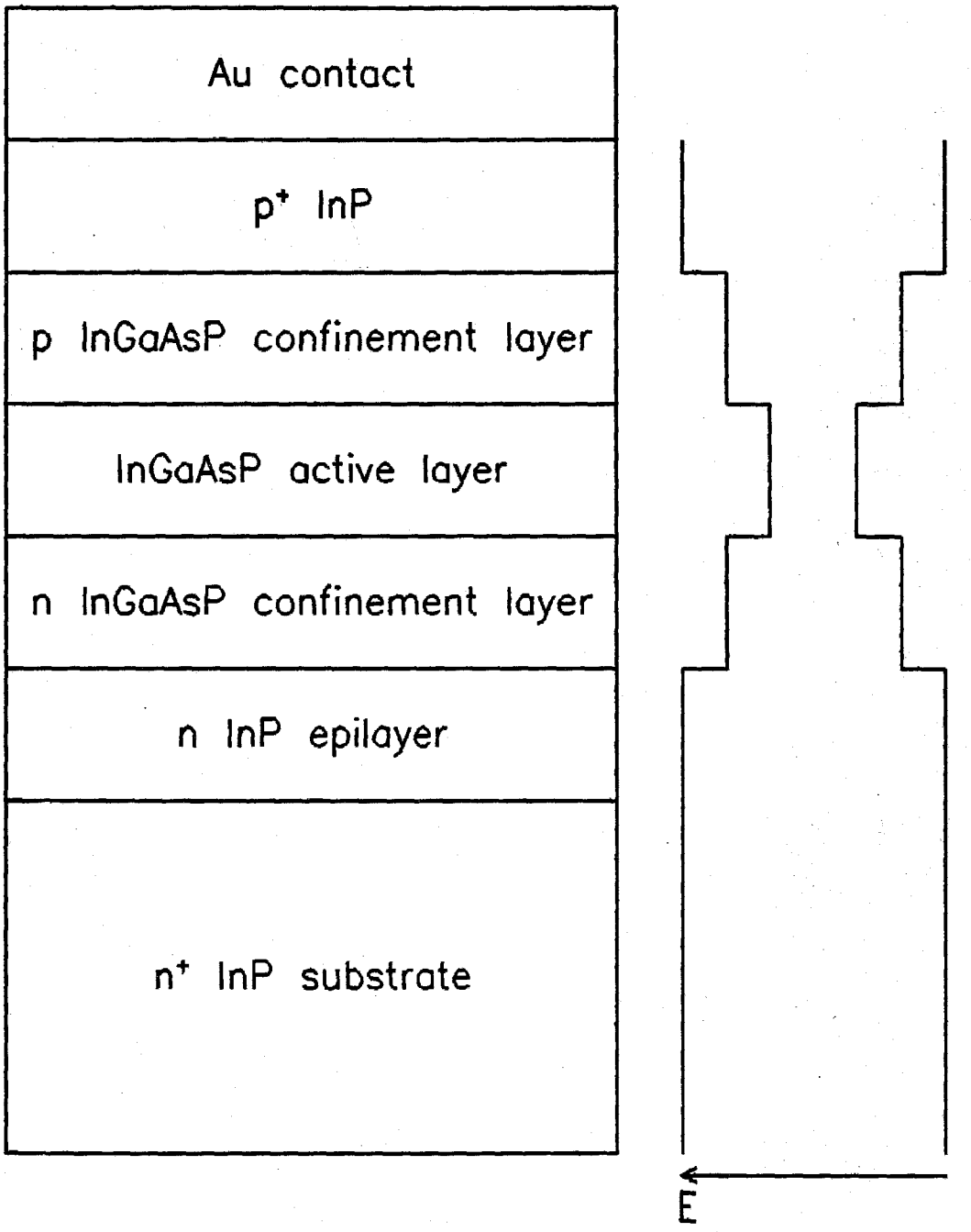
Among the other properties of $In_{1-x}Ga_xAs_yP_{1-y}$, its high electron mobility is the most attractive. Table 3.1 gives values of carrier mobilities, μ_{elec} and μ_{hole}, for each of the four endpoints of the system. The electron mobility of InAs is especially interesting because it is approximately *seventeen* times that of silicon. $In_{1-x}Ga_xAs_yP_{1-y}$ alloys have room temperature electron mobilities[3,4] from 3000 to $\sim$ 11000 $cm^2V^{-1}s^{-1}$. This fact has generated a great deal of interest in the possibility of making integrated optoelectronic circuits from $In_{1-x}Ga_xAs_yP_{1-y}$ and $In_{0.53}Ga_{0.47}As$.

Additionally, compositions of $In_{1-x}Ga_xAs_yP_{1-y}$ lattice-matched to InP have relative dieletric constants ϵ_r greater than or equal to that for InP. Thus, in $In_{1-x}Ga_xAs_yP_{1-y}$ heterostructure lasers with InP cladding layers, the sandwich structure acts as a waveguide, confining photons to the quaternary layer to provide high gain.

3.1.2 $In_{1-x}Ga_xAs_yP_{1-y}$ Lasers and Motivation for Studies

Semiconductor lasers are made from compositions of $In_{1-x}Ga_xAs_yP_{1-y}$ across the lattice-matched range. A typical laser structure is shown in Fig. 3.2. This step structure, with quaternary layers rather than InP adjacent to the active region, is used because it yields higher quality layers. Electrons and holes are injected into the active region by applying a bias to the device.

Figure 3.2: Layers of materials in a typical laser structure. The n-type InP epilayer is grown to provide a high-quality surface for subsequent layers. The diagram on the right shows the bandgap energy corresponding to each layer (without band bending).


Au contact
p+ InP
p InGaAsP confinement layer
InGaAsP active layer
n InGaAsP confinement layer
n InP epilayer
n+ InP substrate
E

They are confined there by the larger-gap quaternary material on either side. They recombine and emit photons with energy equal to the bandgap. If the injection current density in the region is sufficiently high, stimulated emission results.

The current density at which lasing begins is referred to as the threshold current density, J_{th}. J_{th} varies with the device temperature T. Empirically, this temperature dependence is given by $J_{th} \propto \exp(T/T_0)$, where $T_0 =\sim 100$ K for T below room temperature and $T_0 =\sim 60$ K for T above room temperature.[5,6] In addition, there is evidence that T_0 is even lower for longer wavelength (> 1.5 μm) quaternary lasers.[6] T_0 values for GaAs-$Al_xGa_{1-x}As$ lasers, a more established technology, are typically close to 200 K. Since low values of T_0 imply poor temperature stability, several attempts have been made to understand and eliminate the cause of the relatively low values obtained for $In_{1-x}Ga_xAs_yP_{1-y}$ lasers. One possible source of difficulties was thought to be the existence of deep traps in the material which could be acting as centers for nonradiative recombination, thereby killing the gain in the active region. This fact was one of the main motivations for our DLTS studies.

While many novel devices have been fabricated in this material, several basic materials problems still have not been addressed. Among these was the question of deep level impurities. Our DLTS investigations were among the first probes into this issue.

3.2 Samples

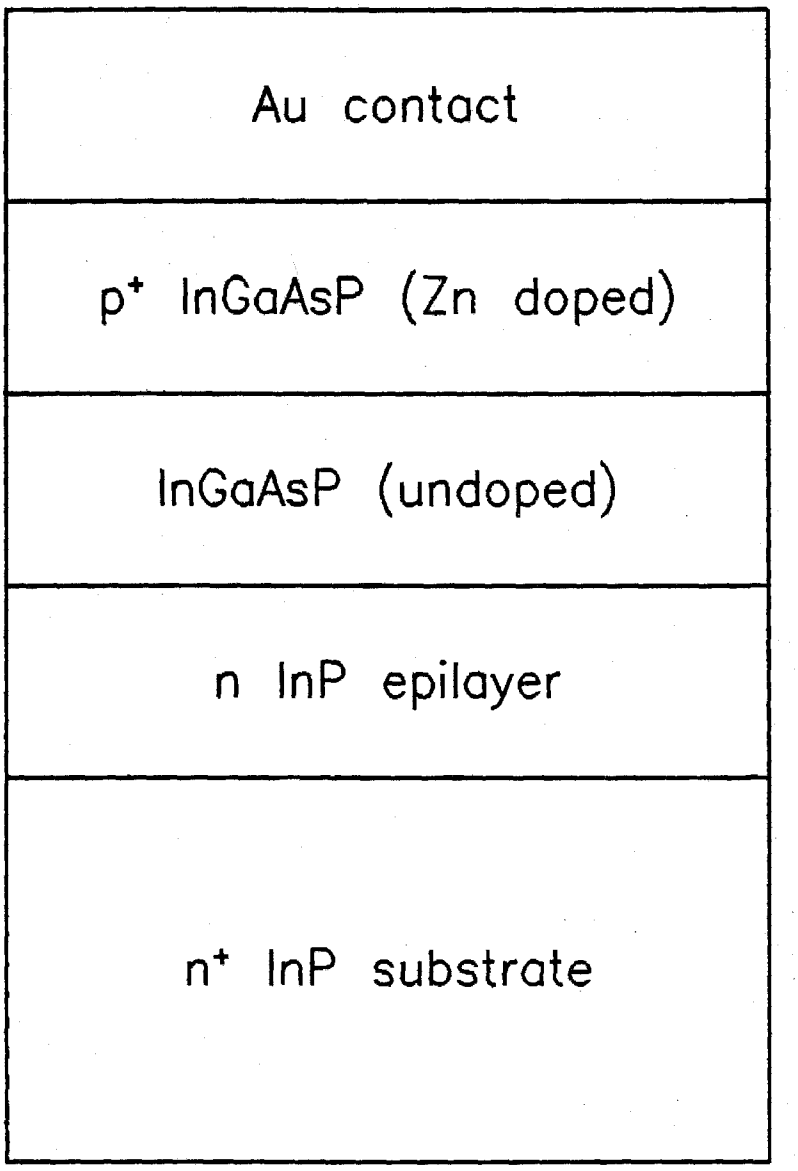
The four compositions of $In_{1-x}Ga_xAs_yP_{1-y}$ used for this study are listed in Table 3.2. These were selected to cover the most interesting range of bandgaps for quaternary devices. Each sample was a p^+-n homojunction grown by liquid-phase epitaxy (LPE) at approximately 640 °C as follows:[7,8] The sulfur-doped n-type (100) InP substrate was etched back by an undersaturated solution for 60 s. A buffer layer of tin-doped n-type InP was then grown. An unintentionally doped n-type ($N_+ =\sim 2-10\times10^{16}$ cm^{-3}) layer of the quaternary material followed. This layer was 0.75–3 μm thick in all but one sample; in that sample, it was 15.5 μm thick. The final layer was Zn-doped p^+-type InGaAsP. Gold was then electroplated onto the surface to provide contact. These layers are shown in Fig. 3.2. All semiconductor layers were lattice-matched to the InP substrate to 0.05% or less in the samples. Devices were defined by cleaving in most cases, although mesas were etched in a couple of cases. Individual devices were then mounted on TO-16 headers and wire-bonded to provide electrical contact. Altogether, there were four 1.1 μm wavelength samples, three 1.3 μm samples, three 1.5 μm samples, and four 1.66 μm samples.

These samples were supplied by R. E. Nahory and M. A. Pollack and fabricated by J. C. DeWinter, R. J. Martin, and E. D. Beebe of Bell Laboratories.

E_g (eV)	λ_g (μm)	x	y
1.1	1.1	0.17	0.37
0.95	1.3	0.26	0.60
0.82	1.5	0.41	0.88
0.75	1.66	0.47	1.00

Table 3.2. Compositions of samples used in this study. E_g is the energy of the bandgap. The wavelength listed for each case, λ_g, is for a photon of energy equal to the bandgap for that composition.

Figure 3.2: LPE-grown layers and gold contact in the samples used.


Au contact
p+ InGaAsP (Zn doped)
InGaAsP (undoped)
n InP epilayer
n+ InP substrate

3.3 Results and Conclusions

DLTS measurements were made using the Boonton Model 72BD capacitance meter. The double boxcar gating scheme was used to analyze the capacitance change after a positive pulse was applied to the reverse-biased p^+-n junction. The detection limit was approximately 5×10^{13} traps cm^{-3}. In all samples except one, no traps were observed above this limit.

The sample that did have a trap was made of the 1.3 μm material. Its shallow donor concentration in the n-type region was 8×10^{16} cm^{-3}. This region was 1 μm thick. The sample exhibited a majority-carrier (electron trap) DLTS peak at approximately 200 K. This peak was only seen with trap-filling pulses of durations longer than 100 μs, and a pulse duration of 10 ms was required to obtain the full peak magnitude. Since trap-filling pulse durations are typically only around 10 μs in normal DLTS scans, these times were extraordinarily long. They implied an extremely small capture cross section of approximately 10^{-22} cm^{-2}. The activation energy of the trap was 0.5 eV to the conduction band edge. The trap concentration fell off relatively quickly into the n-type region; it dropped from 3×10^{16} to 4×10^{15} cm^{-3} at a distance of 0.13 μm from the junction.

As mentioned, this trap was not seen in any other sample — even others made from material from the same growth. Thus, we conclude that it is probably caused by a lattice defect in the substrate that propagated up into the epitaxial layers. Such substrate lattice defects have been pinpointed as the cause of occasional dead lasers in otherwise good batches.

Aside from this trap, our measurements show that various compositions of $In_{1-x}Ga_xAs_yP_{1-y}$ across the range that is lattice-matched to InP can be grown on (100) with trap densities below 5×10^{13} traps cm^{-3}. Such low densities can not be the source of the low T_0 values found for quaternary lasers. Since the time of this study, several other mechanisms have been proposed and explored to explain the threshold temperature dependence. Chief among these are Auger processes, intervalence band absorption, and leakage currents over the confinement layers. At present, it is thought that various Auger processes are the dominant factors in the reduced radiative efficiency.[9,10]

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APPENDIX

EXPERIMENTAL DETAILS OF THE DLTS SYSTEM

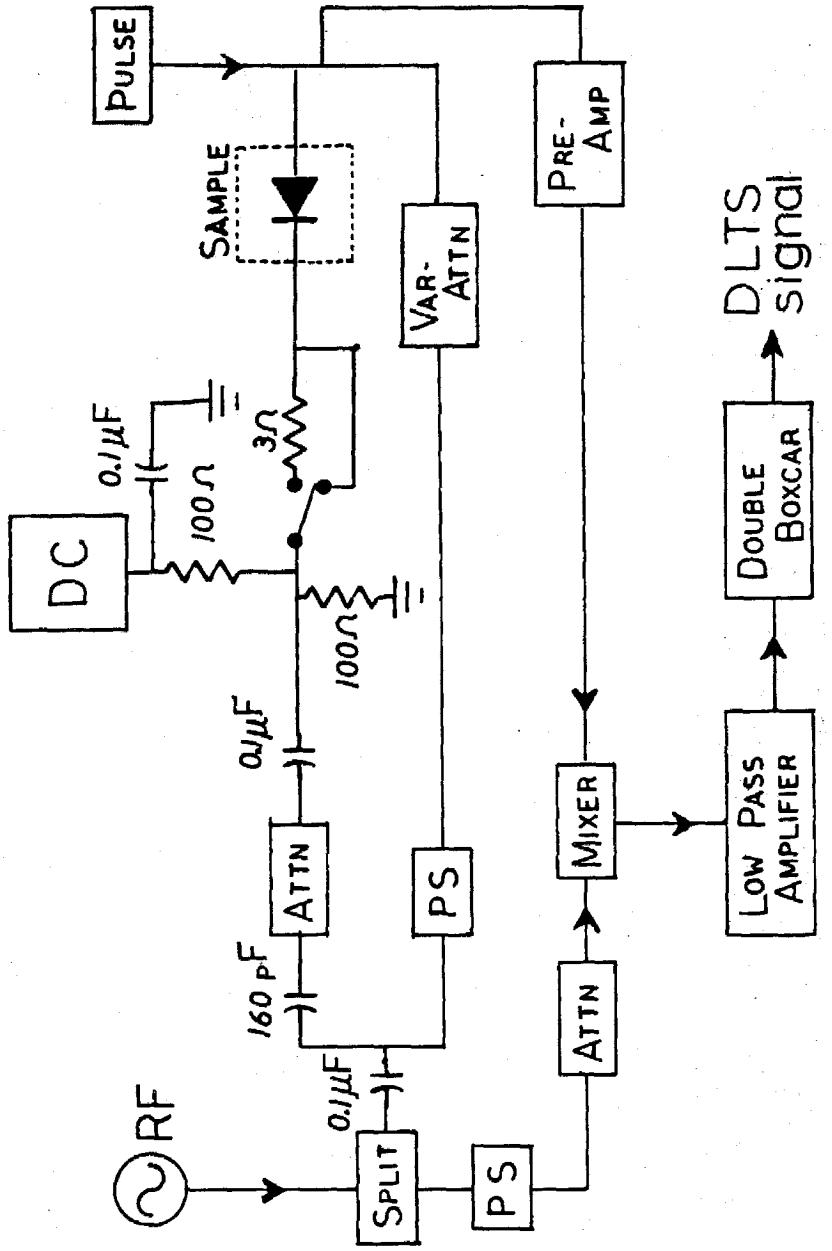
Experimental Details of the DLTS System

Section 1.3.5 of this thesis explained the basic DLTS setup and listed the equipment used for the system based on a commercial (Boonton Model 72BD) capacitance meter. The purpose of this Appendix is to provide the details of the setup used for the high-frequency capacitance transient measurements.

The one-megahertz Boonton meter takes approximately $1 - 2$ ms to recover from the overload that occurs during a DLTS trap-filling pulse. This limitation presents a problem when the user wishes to make an activation energy measurement, which requires the analysis of transients over a large range of decay times. For these measurements, a system with a faster response is necessary.

Figure A.1 is a diagram of our fast-response capacitance bridge. This circuit is a modified version of the original setup proposed by Lang.[1] The radio-frequency signal is divided and applied to two branches of the circuit: one contains the sample, and tho other is a reference branch. The sample diode is reverse biased by the DC supply. It is in series with an attenuator and in parallel with a phase shifter (PS) and variable attenuator. These are adjusted so that the parallel legs are 180° out of phase and have equal amplitude, resulting in minimal signal going into the first amplifier (pre-amp). When the impedance of the sample changes, e.g., after a trap-filling pulse, the amplitude of this signal increases. The output from the pre-amp is mixed with the signal from the other branch, which has been attenuated to

Figure A.1: Diagram of apparatus for fast capacitance transient measurements.


PULSE
SAMPLE
VAR-ATTN
PRE-AMP
DLTS signal
DOUBLE BOXCAR
0.1μF
100Ω
3Ω
DC
100Ω
0.1μF
ATTN
PS
160 pF
MIXER
LOW PASS AMPLIFIER
0.1μF
RF
SPLIT
PS
ATTN

the correct amplitude. Since we are only interested in the capacitive portion of the impedance change, the phase shifter in the reference branch is adjusted so that switching the 3 Ω resistor next to the sample into the circuit does not affect the mixer output. The mixer output is then amplified by a low-pass amplifier. The signal from this amplifier is proportional to the capacitance change of the sample (for the relatively small capacitance changes which are typical for DLTS); thus, this signal is sent to the double boxcar amplifier for transient analysis.

To operate this setup, the user begins by connecting the sample diode and minimizing the signal out of the pre-amp by adjusting the two attenuators and the phase shifter in the sample loop. Then the output of the low-pass amplifier is monitored while the 3 Ω resistor is switched into the circuit. The reference phase shifter is adjusted until the resistor has no effect on the signal. The system is typically operated at 20 MHz with the magnitude of the RF signal applied to the sample at approximately 0.2 V. It provides DLTS sensitivities similar to the Boonton system (occasionally better) and recovery times under 100 μs, an order of magnitude improvement over the commercial system.

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